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Study of SSIN Parallel Processing

Interconnection Networks

Final Report

by

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Study of SSIN Parallel Processing Interconnection Networks

Problem Studied:

In this work, we consider single stage interconnection networks (SSINs) which have only one stage of switches; in contrast to multistage interconnection networks (MINs), and use recirculation through processors to provide the desired source-destination permutations. The main objective of this work is to obtain an analytical probability model of SSINs and to do simulation for evaluation of the performance of SSINs. We focus our attention on SSINs using 2×2 switches. We have considered four SSINs and simulated different network sizes, loading and routing strategies. The four SSINs are the single stage Omega, the Modified Omega, the Zeta and the ROT networks. In resolving the conflicts, we use two possible cases of processors with and without buffers and three different routing strategies. The strategies are Shortest Remaining Path First, Longest Remaining Path First and Arbitrary Priority. The buffer size is assumed to be large enough to hold any number of requests. For cases without buffers, requests of lower priority are sent to available processors for further routing. The simulation software accepts network type, network size and switch size as inputs and produces the adjacency matrix and distance matrix of the network, the switch dependency graph, the randomly selected permutation samples and their routings, the average dynamic path length, the average conflict number and the maximum path length required to complete a permutation. In general, there is a close agreement between the analytical model and the simulation. Thus the model by itself could be used to study the performance of SSINs. The impact of single stack-at-faults on the dynamic full access capability and the dynamic average path lengths, has also been considered.

Summary of the important results:

The increase in dynamic average path length (DAPL) with network size is moderate while it is significantly less than $\log_2 N$, the number of stages needed in a MIN. The best performance in the case of no fault and single fault, is obtained for the modified Omega and the Zeta SSINs.

List of publications:

1. J. Richard Burke, Chienhua Chen, Tsung-Ying Lee and Dharma P. Agrawal, "*Performance Analysis of Single Stage Interconnection Networks*," accepted for presentation, Taiwan Conference, Dec. 1988.
2. J. Richard Burke, Chienhua Chen and Dharma P. Agrawal, "*Impact of faults on the performance of single stage Interconnection Networks*," under preparation.

Participating Scientific Personnel:

1. Dr. J. Richard Burke: Co-principal Investigator and ARO Staff Research Officer
2. Mr. T. Y. Lee: finished MS degree
3. Mr. Chienhua Chen: currently finishing MS degree