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EXPERIMENTAL INVESTIGATION OF HOT ELECTRON AND RELATED EFFECTS IN GALLIUM (ALUMINUM) ARSENIDE DEVICES

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The theoretical and experimental results from the heterostructure hot electron diode (HHED) a two-terminal device which exhibits S-shaped negative differential resistance, are presented, which shed new light on the transport processes involved in the tunneling, resonant tunneling and thermionic emission processes in semiconductor heterostructures. In support of some of the conclusions about the heterostructure hot electron diode, experiments involving transport of two-dimensional electrons in the negative resistance field effect transistor (NERFET) in

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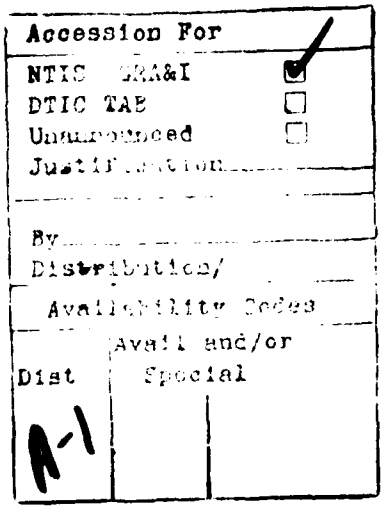

EXPERIMENTAL INVESTIGATION OF HOT ELECTRON AND RELATED EFFECTS IN GALLIUM (ALUMINUM) ARSENIDE DEVICES

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1. INTRODUCTION

With the maturity of the MOCVD[1] epitaxial crystal growth process, a host of GaAs/$Al_xGa_{1-x}As$ electron devices has become practically realizable with MOCVD technology. These include established device technologies such as heterojunction bipolar transistors (HBT's)[2] and high electron mobility transistors (HEMT's)[3] and a variety of resonant tunneling and hot carrier devices; some aspects of the last two are treated here. In the case of resonant tunneling, as in any hot carrier device involving heterostructure barriers, the ability to produce electrically heterostructure barriers is of paramount importance, often more important than more traditionally emphasized electrical parameters such as low field electron mobility.[4]
Two such devices are the heterostructure hot electron diode[5] and the negative resistance field effect transistor.[6] In both devices, high quality, electrically insulating barriers are essential. Since this work treats only devices in the GaAs/$Al_xGa_{1-x}As$ system (acknowledging that there are some attractive properties of other III-V, non-lattice matched materials yet to be incorporated into devices of this type), lattice matching is not of primary concern.

1.1 Relevant Physical Principles

There are several physical principles at work in the heterostructure hot electron diode and negative resistance field effect transistor. In both devices, cold (lattice temperature) electrons are confined by a tunneling barrier for a low electric field condition, and these electrons are subsequently emitted over the barrier in a high electric field condition. In addition, when under practical operating bias, both devices have sufficiently large electric fields in their tunneling barriers that the

aforementioned barriers can be considered triangular. This allows us to treat them with a combination of field emission and thermionic emission theories.

1.1.1 Thermionic emission

The problem of thermionic emission in the GaAs/$Al_xGa_{1-x}As$ system can be very straightforward or quite complicated, depending primarily on Al compostion x. In the simple case of an n+ GaAs/$Al_xGa_{1-x}As$/n+ GaAs structure, where electric fields are assumed to be confined to the $Al_xGa_{1-x}As$ and space charge effects are negligible, thermionic emission can be explained by the normal classical equation

$$J=A^{*}T^{2}\exp\left\{\frac{e\phi}{k_BT}\right\} \qquad (1.1)$$

where $A^* = em^*k_B^2/2\pi^2h^3$ is the effective Richardson constant (approximately 8 A/cm^2K^2 in GaAs), J is the current density in A/cm^2, ϕ is the heterostructure barrier height with respect to the Fermi energy in GaAs and T is the the absolute temperature. This equation fits the data as long as the Al content x is below 0.5, thereby restricting the $Al_xGa_{1-x}As$ barrier to either the direct gap regime or near the Γ-L-X crossover point (see Fig. 1 and Refs. 7 and 8).

Thermionic emission theory for $Al_xGa_{1-x}As$ barriers of $x > 0.5$ requires adjustment of Eq. (1.1) in order to accurately model bandstructure contributions. Solomon et al.[8] have done an empirical fit to thermionic emission current data for n+ GaAs/$Al_xGa_{1-x}As$ over a wide range of x and have suggested that, for indirect

materials, modification of the Richardson constant (essentially making it a function of x) for indirect barriers can account for the lower than expected thermionic emission current seen in indirect barriers. Their data suggest that, as an example, for an Al content $x > 0.8$ the effective Richardson constant is less than one percent of the theoretical value. Several theoretical objections can be made to such a simplification. Specifically, the problem of intervalley phonon absorbtion by Γ electrons spatially located in the barrier (due to Γ wavefunction penetration) seems unlikely to fit the temperature dependence of Eq. (1.1). The complicated process of intervalley phonon interaction would seem to become important at Al compositions near the Γ-L-X crossover (i.e., $x > 0.4$), but the data of Ref. 8 indicate that there are no significant deviations from the theoretical Richardson constant until $x > 0.5$. This behavior near the Γ-L-X crossover is probably due to significant Γ-L intervalley scattering (favorable over the X valley from both a density of states and energy standpoint) and the subsequent thermionic emission of the L valley electrons, since the L valley electrons in GaAs encounter almost no barrier for $Al_xGa_{1-x}As$ near the crossover. For the case of barrier Al content above $x = 0.5$, L valley thermionic emission is reduced due to the increasing L valley barrier height, and as a consequence the relatively weak X process dominates. In the case of AlAs barriers, one would expect this condition to exist at its extreme, with very low thermionic emission currents over a wide range of barrier electric fields. This has been demonstrated[9] to be the case with AlAs barrier devices showing very low currents for voltages below the field emission threshold. This Γ-X thermionic emission is also governed by the fact that E_{001} must be greater than ΔEc, where

$$E_{001} = \frac{h^2 k_{001}^2}{2m^*}, \tag{1.2}$$

k_{001} being the X valley propagating momentum. Only one of the three equivalent X valleys (in this case, the 001 valley for 100 growth planes) will dominate in this process due to conservation of k_{001} in the Γ-X transfer.[10,11]

1.1.2 Field emission and tunneling

Tunneling current in the GaAs/$Al_xGa_{1-x}As$ system as it applies to the devices such as the heterostructure hot electron diode and negative resistance field effect transistor can be treated as a field emission problem. The tunneling current in these devices at voltages below the field emission threshold (i.e., field emission being as in Fig. 2 where $eV_{app} >> \Delta Ec$, V_{app} being the voltage applied across the barrier) is negligible compared to actual device operating currents. For this region the tunneling current can be expressed as in Duke[12]

$$J_{001} = -e(2s+1)\int_0^{\infty} dk_{001} \frac{1}{h}\frac{\partial E}{\partial k_{001}} D(k_{001}) \int dk_{||} f(\mathbf{k}) \qquad (1.3)$$

where s is the electron spin (1/2), $D(k_{001})$ is the transmission probability, which from the WKB approximation for a triangular barrier is

$$D(k_{001}) = \left[1 + \exp\left\{ \frac{\sqrt{2m^*}}{3h|\mathbf{F}|}(\Delta E_c - E_{001}) \right\} \right]^{-1} \qquad (1.4)$$

where E_{001} is defined as before, $\mathbf{F}$ is the electric field in the barrier, ΔE_c is the conduction band offset for the appropriate conduction valley and m^* is the effective

mass in the $Al_xGa_{1-x}As$ for the same valley. This approach is well suited to numerical integration (see Ref. 13), particularly for Γ tunneling, but there is considerable information contained in the distribution term f(k) that can make the problem quite complicated in the case of indirect barriers. In this case, multiple integrals involving each of the Γ, L and X conduction band minima and their respective band offsets must be calculated, using the appropriate f(k) for each one.

Another method of computing tunneling current is that of Solomon et al.[8] which uses a Richardson-type tunneling prefactor (see Murphy and Good[14]) and, as in their thermionic emission results (see section 2.1), it requires scaling of the Richardson constant for indirect materials and has theoretical problems similar to their thermionic emission calculations. Other work on tunneling[15] shows similar experimental results but accounts for them in an entirely different way. Hase et. al[15] have characterized $GaAs/Al_xGa_{1-x}As$ samples in the region near the Γ-L-X crossover ($0.38 < x < 0.46$) and have found deviations from those for the idealized Γ tunneling (the samples used in the characterization were too thick and electric fields too low for field emission, but a similar theory applies). Their theory is that of Duke[12] and they have found good agreement with experiment for thin samples of low composition ($x = 0.38$, 134 Å). Other barriers, either thicker (300 A) or higher composition ($x = 0.46$), show deviations from the ideal, and Hase et al. have chosen to invoke Γ-X coupling which, "... suggests that the X-band minimum should merge with the Γ-band to result in a larger effective mass ...," to justify using the effective mass in the barrier as a parameter, choosing a value somewhere between the Γ and X values that provides the best fit to experimental data. This is in contrast to the work of Solomon et al. and ignores the intervalley phonon contribution.

There are several practical considerations of the tunneling current in the heterostructure hot electron diode and negative resistance field effect transistor. In both devices there exists the obvious problem of barrier doping and its resulting space charge and band bending (Ref. 16, Section 4.2). In addition, since these devices are operated well within the field emission regime with correspondingly thin effective barrier thicknesses, interface quality and impurity assisted tunneling become important considerations. The GaAs/$Al_xGa_{1-x}As$ system has the unfortunate quality of having the desirable highest band offset coincide with the undesirable high statistical disorder at x=0.45. It has been shown[17] that the disorder associated with the ternary system can have an effect on tunneling currents, both from the standpoint of interface states and donor-like states in the $Al_xGa_{1-x}As$ (see Ref. 18, which deals with GaAs but is applicable to the problem in $Al_xGa_{1-x}As$). This problem has manifested itself in the early heterostructure hot electron diode and the negative resistance field effect transistor where the barrier was constructed of x = 0.43 material.

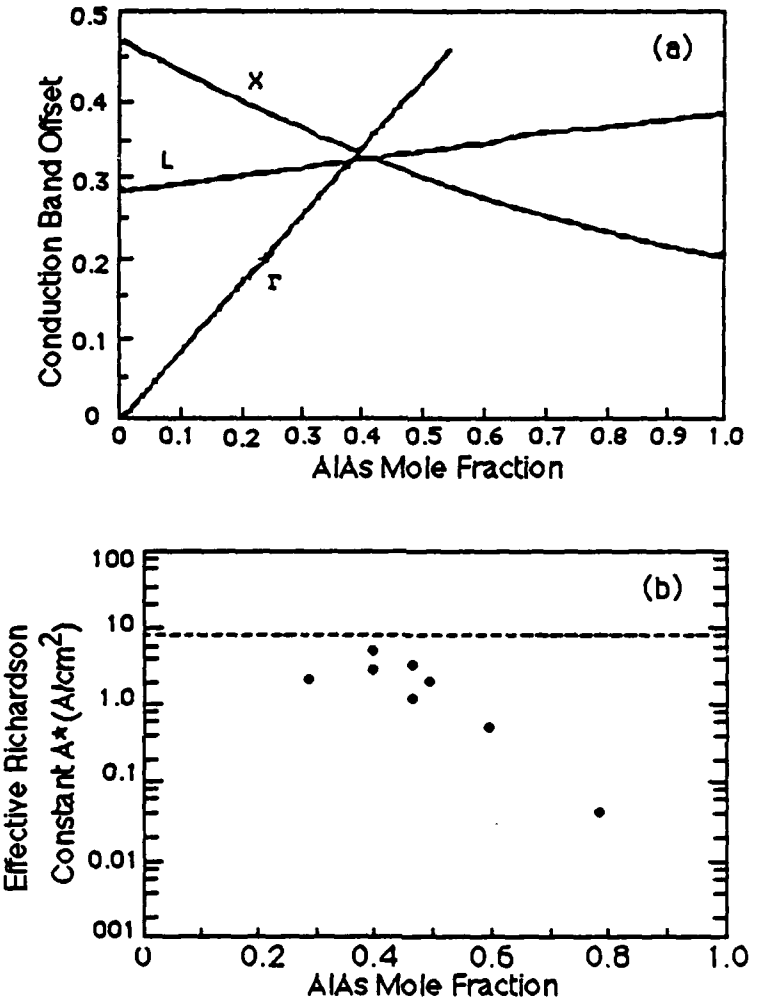

Figure 1. (a) Band offsets and (b) effective Richardson constant for GaAs/$Al_xGa_{1-x}As$ heterostructures as a function of Al content x.[8]

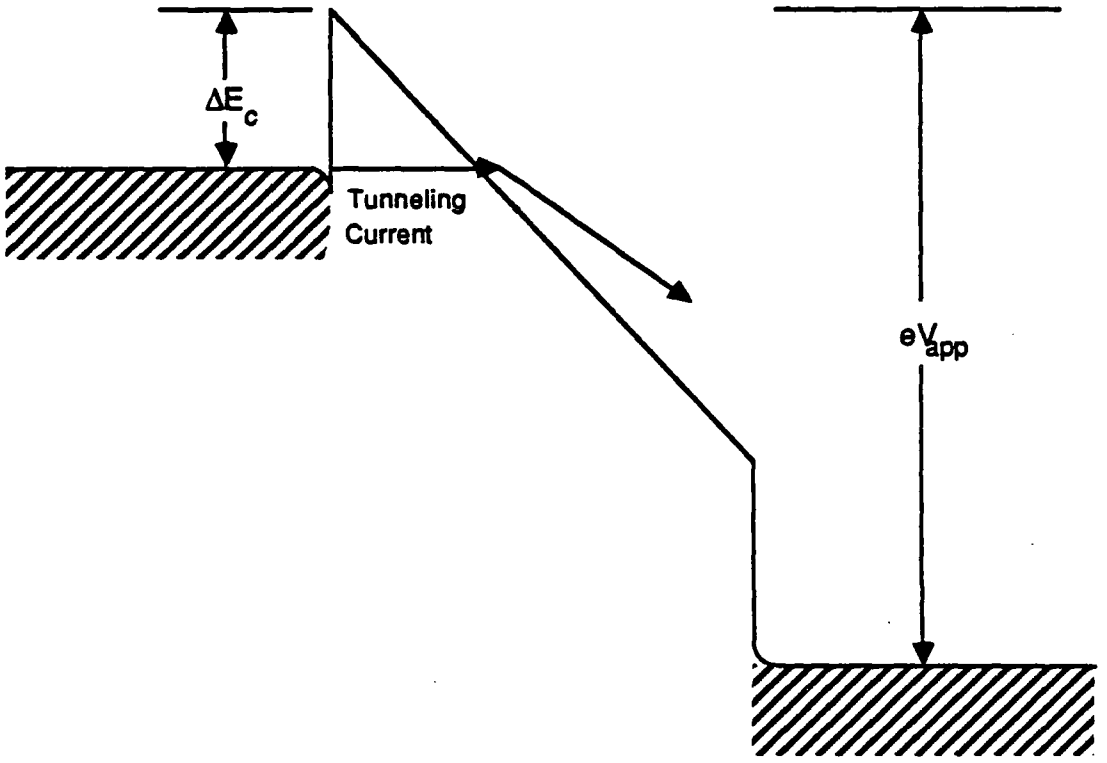

Figure 2. Conduction band edge diagram of n^+ GaAs/ Al_xGa_{1-x}/n^+ GaAs structure in field emission.

2. FABRICATION AND MEASUREMENT

All growth of the experimental devices in this report was done by MOCVD and all of the fabrication was done by standard optical photolithography. The following is not intended to be a complete guide to the fabrication of GaAs devices, but rather it's aim is to describe the important processing features which pertain to the fabrication of the negative resistance field effect transistor and the heterostructure hot electron diode.

2.1 MOCVD Growth Considerations

In the growth of electron devices by MOCVD,[1,16] growth parameters must be carefully tailored to a specific device application. In the case of the heterostructure hot electron diode and the negative resistance field effect transistor, the important consideration is the ability to grow lightly doped GaAs simultaneously with a semi-insulating $Al_xGa_{1-x}As$ barrier, unlike most transistor structures (either bipolar or field effect) which are doped throughout. Since both the heterostructure hot electron diode and the negative resistance field effect transistor utilize electrons injected from heavily doped contacts into an undoped region capable of supporting a carrier heating field, it is important that there is as little space charge in the undoped region as is practical. The barriers in the heterostructure hot electron diode and the negative resistance field effect transistor present the most challenging aspect of the growth of these devices. Since the material parameters of MOCVD $Al_xGa_{1-x}As$ vary greatly as a function of growth temperature,[1,16] generally the optimum temperature for the growth of the $Al_xGa_{1-x}As$ barrier was chosen, with the parameters of the other layers compromised somewhat.[16] It is important to note that not all of the material

parameters of the $Al_xGa_{1-x}As$ (e.g., optical parameters) are important to the operation of these devices, and as such, much of the existing literature on MOCVD growth of devices is not applicable. In general, heterostructure hot electron diode and negative resistance field effect transistor devices were grown at the lower end of the temperature range generally considered acceptable for $Al_xGa_{1-x}As$ (i.e., approximately 720°C). Initially $Al_xGa_{1-x}As$ barriers of $x \leq 0.45$ were incorporated to avoid material problems associated with higher Al compositions. [5,13,16] Eventually it was determined that certain bandstructure properties of the indirect ($x > 0.45$ in the AlxGa1-x As barrier)[8] heterojunctions could be used to enhance the switching in the heterostructure hot electron diode and ultimately barriers of AlAs were utilized[9] (see Sections 1.1 and 3.2). These indirect heterojunction devices with their enhanced performance characteristics generally produced working devices over a wider range of growth and operating temperatures.[9,16]

In the growth of NERFETs by MOCVD, the most important aspect has also been shown[16] to be the quality of the $Al_xGa_{1-x}As$ barrier. Reactor growth conditions should be tailored to obtaining the most resistive barrier possible while not allowing the subsequent (surface side) GaAs-$Al_xGa_{1-x}As$ interface to be degraded. If barriers are grown that contain significant impurities, the overall barrier shape can be affected. This is particularly evident in the case of p-type barriers where a two-dimensional hole gas can exist at the interface due to transfer of holes from their parent donors in the $Al_xGa_{1-x}As$. In this case, it becomes impossible to apply a substrate voltage large enough to cause any electron accumulation without creating an electric field in the barrier so large that the width of the trapezoidal barrier becomes too small for carrier confinement. In the case of n-type barriers - while there is probably a two-dimensional gas even at zero substrate bias - the remaining carriers in the barrier are confined due to the substrate side interface conduction

band offset and provide a parallel conduction path. With these facts known, it becomes apparent that the ideal NERFET should incorporate a semi-insulating barrier and the net impurity concentration should be kept as low as practical while still maintaining good overall crystal quality.

2.2 Fabrication

The devices fall into two broad categories. First are the simple mesa structures (the heterostructure hot electron diode) with a Au-Ni-Ge or Au-Ag-Ge based top ohmic contact and the second is the field effect device (negative resistance field effect transistors) which requires definition of source and drain contact pads separated by a narrow (approximately 2μm) channel region. In all cases the starting wafer was n^+ GaAs. Backside ohmic contacts were made by deposition of 1000Å of AuGe eutectic.

2.2.1 Lithography and wet chemical etch

For the case of the NERFET, a two-step optical lithography process was employed. First a positive photoresist liftoff metallization step was done for the definition of source and drain and then (following alloy) a wet chemical mesa etch for device isolation. For the liftoff step, a pair of source and drain contact holes (separated by approximately 3 μm on the photomask) was opened in the photoresist by the following process:

Photoresist Process For Liftoff Metallization

Photoresist: AZ4110, undiluted

Spin: 4000 rpm, 30 seconds

Bake: either 30 min at 90°C (for etch steps)
or 25 min at 70°C (for liftoff steps)

Expose: Mean time 20 s for bulb intensity of 11mW/cm^2 (adjust time proportional to bulb intensity)

Chlorobenzene soak: 10 min (for liftoff steps)

Develop: in solution of AZ400K:deionized water of 4:1 approximately 1.5 minutes

It was found that the above process gave acceptable results for wafers on the order of 1 cm^2. For smaller wafers edge pileup of the photoresist generally gave unsatisfactory results in high resolution applications. After metal deposition and liftoff in acetone the same photoresist procedure was used to define mesas.

The mesa etch was done by the H_2SO_4:H_2O_2:H_2O system in either a 5:1:1 ratio or a 1:8:57 ratio. The etch rate for this system is essentially independent of ratio over the range of these two mixtures and is approximately 1 μm/min. Of the two, the 5:1:1 mixture gives the most specular surface after etch, but it attacks the photoresist and generally requires a lengthy pre-etch post-bake (30 min at 120°C) of the photoresist in order to provide an adequate etch mask. The 1:8:57 mixture, on the other hand, leaves a pitted surface but has little or no effect on the photoresist and can be used without post-baking the photoresist. Occasionally a 1:1:1 mixture of

$K_2Cr_2O_7$:HCl:CH_3OOH was used, with the crystalline $K_2Cr_2O_7$ in solution at it's solid solubility limit in water. This mixture was also a 1μm/min etchant with very little photoresist damage to standard optical resists. The main drawback of this etchant solution was the eye irritation caused by the acetic acid (CH_3OOH), which could be quite bad in areas with inadequate ventilation. In addition, this etchant cannot be used with electron beam resists, which the potassium-based etchant dissolves immediately.

For the fabrication of the heterostructure hot electron diode and all other large area diodes (3 to 12 mil mesas with 2 to 8 mil metal top contacts), similar photolithographic methods were used with the added benefit that much wider tolerances could be allowed. In general, the diodes required taller mesas than those of the field effect devices (in excess of 1 μm, rather than 4000 Å for the field effect devices) with the preferred etchant being the 1:8:57 due to the longer etch times.

2.2.2 Ohmic contacts

Ohmic contacts were fabricated of either Au-Ni-Ge or Au-Ag-Ge with the Au-Ag-Ge system being ultimately preferred and exclusively used for reasons of contact morphology and shallow alloy depth. For the Au-Ni-Ge system, 1200Å of AuGe eutectic followed by 150Å of Ni and finally 1200Å of Au were thermally evaporated and subsequently alloyed at 420°C. This system was eventually abandoned in favor of the Au-Ag-Ge system which consists of a 400Å AuGe eutectic followed by 1000Å of Ag and 1200Å of Au. In the case of NERFETs, Au-Ni-Ge contacts proved to be unacceptable due to excessive alloy depth causing the shorting of the source and drain contacts through the $Al_xGa_{1-x}As$ barrier to the substrate. The Au-Ag-Ge contact, on the other hand, has been successfully used in the fabrication of negative

resistance field effect transistors (see Chapter 4) and has been shown to have a more shallow diffusion profile than the Au-Ni-Ge system.[19] In addition, the Au-Ag-Ge system seems to give better contact morphology (when viewed through an optical microscope) with a resulting improvement in ease of wire bonding. This improvement is especially noticeable when the top layer of the sample semiconductor contains aluminum (certainly in cases of 20% aluminum or more). The Au-Ag-Ge system has the added advantage that a stable alloy is formed quickly[19] and very little variation of structural or electrical characteristics is evident over a fairly wide range of alloy temperature (415°C to 430°C, the range over which all samples were alloyed). Ultimately all two-terminal structures were fabricated with this system, even though alloy depth in these structures is generally not a problem (due to a heavily doped cap layer) and the Au-Ni-Ge system would have sufficed.

2.3 Measurements

The dc current-voltage measurements of the heterostructure hot electron diode and negative resistance field effect transistor were done by standard laboratory methods, either by a Tektronix 577 curve tracer, Hewlett-Packard 4145 semiconductor parameter analyzer, or pulsed dc techniques. Each of these techniques is outlined below.

In the case of the 577 curve tracer, certain limitations are inherent in the measurement hardware. Since the 577 operates the swept voltage by rectifying a line voltage, providing an analog sweep rate fixed by the line frequency, two generally superimposed traces appear on the screen, one representing the outward going (from zero volts) voltage sweep and the other the return sweep. In the case of negative differential devices, this can lead to a hysteresis in the displayed current

voltage trace. In all negative differential resistance devices, the region of negative differential resistance can be represented by a load line of resistance -R, where R is the natural load line of the device as represented in Fig. 3. If a series load resistance, which is selectable on the 577 (see Fig. 4), is selected that exceeds the value of the natural load line R, oscillations will occur as the bias voltage is swept through the region of negative differential resistance. These oscillations will manifest themselves as noise on the screen of the 577. If a series load resistance is chosen that is smaller in magnitude than the natural load line R, the device will switch from the apex point on the low current branch to one on the high current branch or vice versa, depending on the direction of the trace. In all cases these two switching points can be connected by a line of slope $-R_L$ where R_L is the load resistance selected in the 577. This case of small load resistance will result in a hysteresis in the current voltage trace as is shown in Fig. 5. Caution should be exercised when selecting a load resistance; if an exceedingly small value is chosen, the device can switch to an excessively high current state which can in turn damage the device. This is particularly true of the heterostructure hot electron diode when it is in a state of very low dynamic resistance.

When making measurements on the heterostructure hot electron diode or any other negative differential resistance device with the 4145B semiconductor parameter analyzer, special attention must be paid to the choice of a proper load resistance. Since the 4145B is a digitizing device, averaging data at a specific dc operating point, the load line cannot cause excessive oscillations in the device if an accurate measurement is to be made. In addition, since the 4145B does not sweep its voltage in both a forward and reverse direction like the 577 (showing the total hysteresis), a load resistance that is too small will give an inaccurate picture of the device current-voltage trace. Ideally, as in the case of the 577, a load resistance as

close as possible to the natural load resistance R should be chosen. If a series load resistance that causes oscillation is used, a small capacitance placed in parallel with the device under test may reduce oscillations to the level that a measurement can be made. If a parallel capacitor is used, care should be taken to ensure that the RC time constant of the load resistance and shunt capacitance does not exceed the integration time of the 4145B. Since the 4145B has no internal loads available, the load resistance and shunt capacitance are best added to the external circuit via a decade resistance/capacitance box or similar device that facilitates easy adjustment.

In order to minimize device heating effects in samples with high current density pulsed dc techniques should be used, whereby a low duty cycle (approximately 100 Hz) short (approximately 100 ns) pulse is used to establish a quasi-dc operating point. For pulsed dc measurements, the device under test is placed in one of two modes, either at the end of a 50 ohm transmission line as in Fig. 6, or in a series configuration as in Fig. 7. For low impedance samples the series method of Fig. 7 is preferred, as it preserves the 50 ohm transmission line. The termination method can work for high impedance samples, particularly if a 50 ohm load is placed in parallel with the device under test and the current then shunted through this dummy load is then subtractedfrom the final result. The actual measurement is made by sampling the response at a point in the center of the voltage pulse (see Fig. 8), either via a sampling oscilloscope or some other digitizing unit. Since the system will seldom be a pure 50 ohm system, some oscillation will occur at the leading and trailing edges of the driving pulses; hence, it is best to set the trigger delay for the sampling unit to the center of the pulse. With this technique, pulses of less than 100 ns can be achieved, and an accurate measurement can be made for low pulse duty cycles (100 Hz or less). In setups with severe impedance mismatch, overshoot at the pulse edges can also cause extremely high voltages to

appear at the device under test, with a corresponding device failure at what would normally appear to be a safe operating voltage.

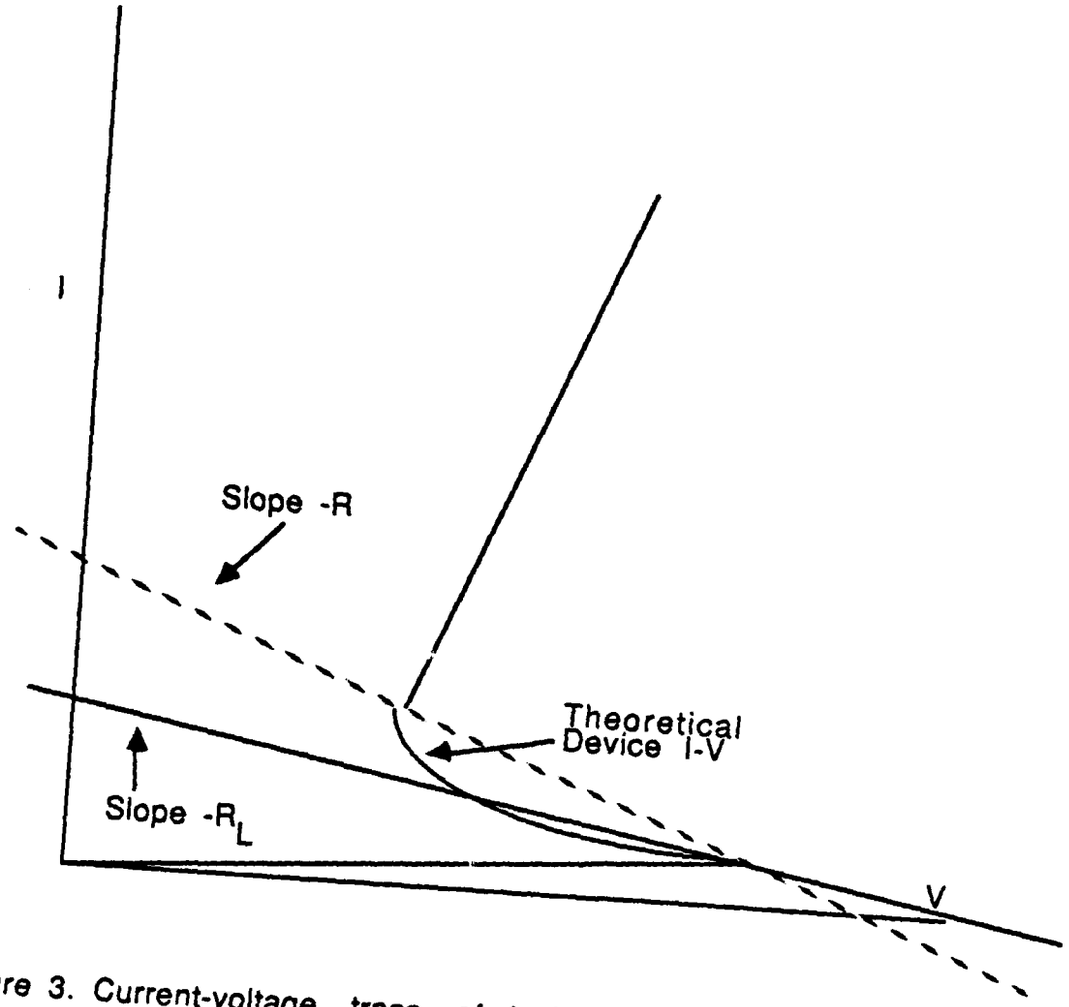

Figure 3. Current-voltage trace of device exhibiting S-shaped negative differential resistance with the effects of a load line, showing natural load line -R. In addition, the load line due to load resistance R_L exceeding the natural load line resistance is shown. Since this line cannot connect two stable points, oscillations will occur in the negative differential resistance region.

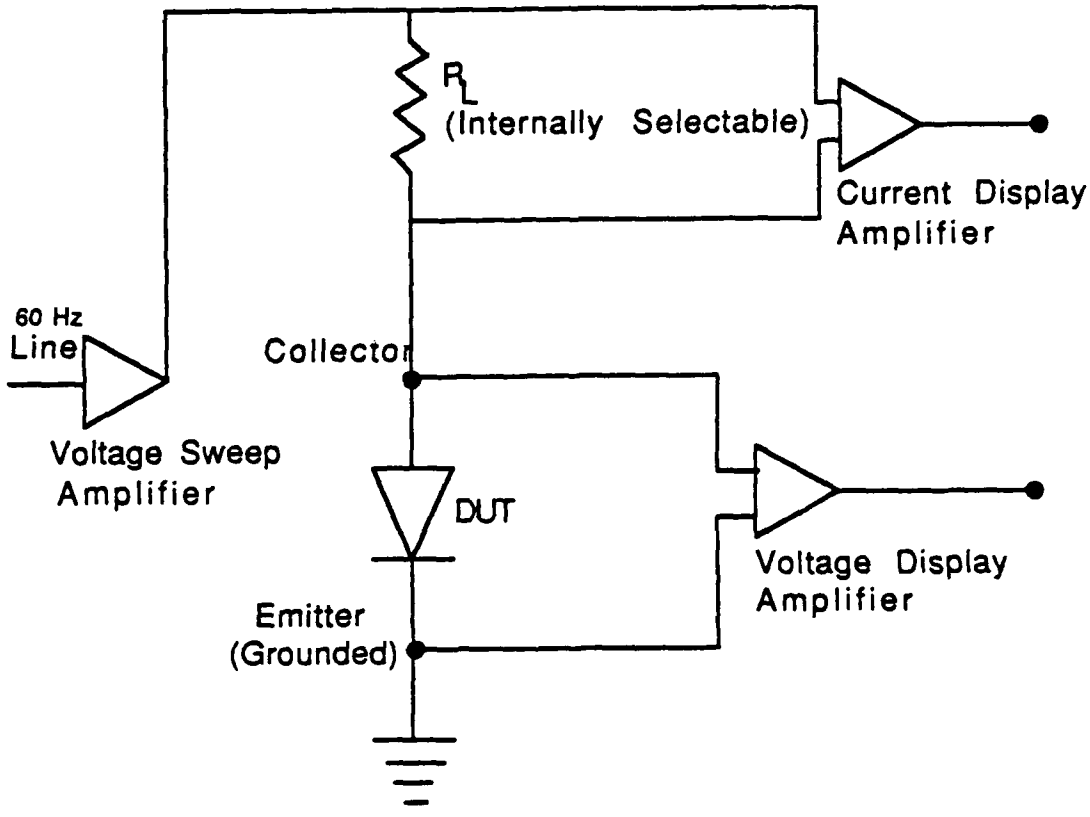

Figure 4. Schematic of Tektronix curve tracer in emitter grounded configuration showing internal load resistance.

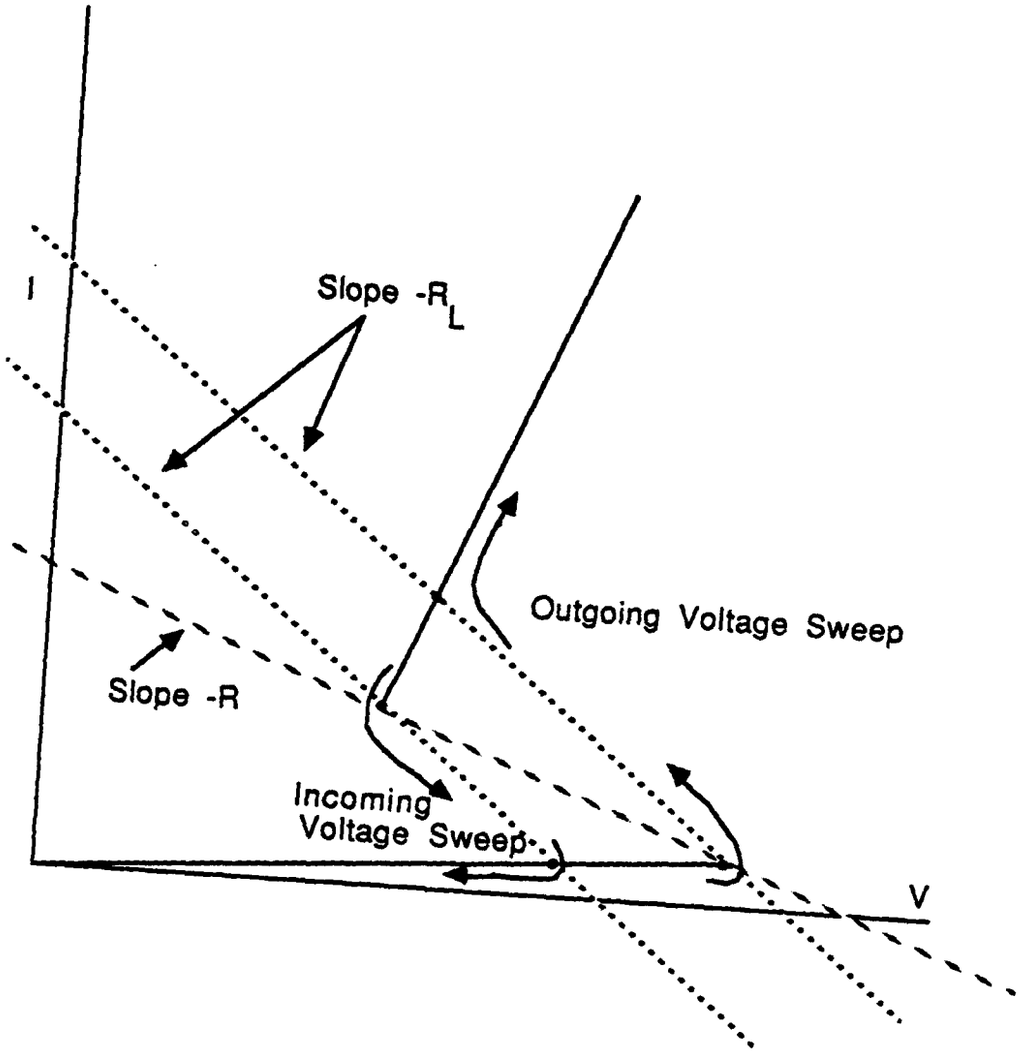

Figure 5. Current-voltage trace of device exhibiting S-shaped negative differential resistance with the effects of a load resistance R_L smaller than the natural load line resistance R. Note the hysteresis in the current-voltage trace.

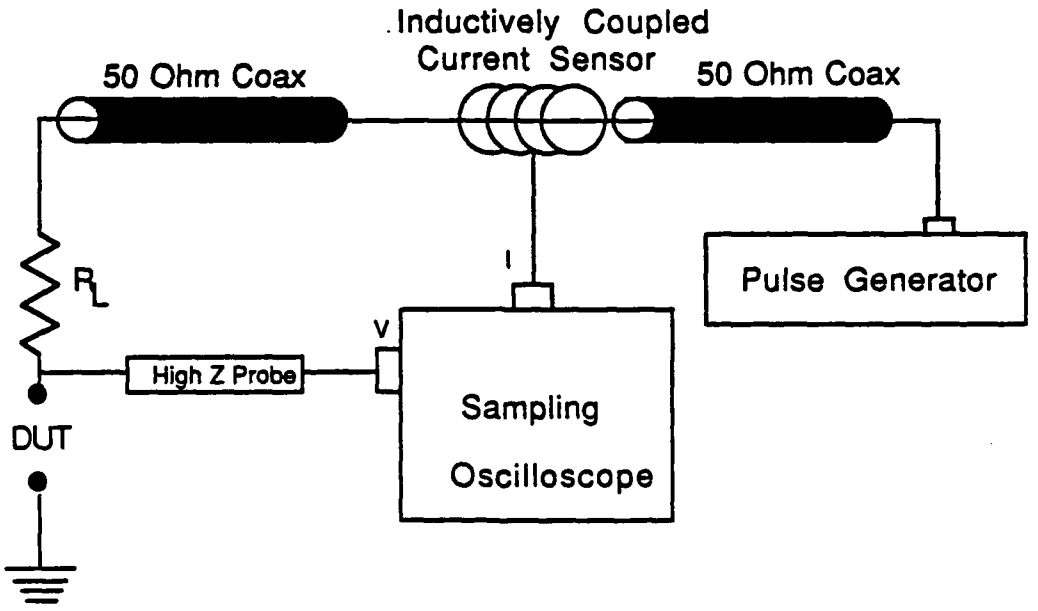

Figure 6. Pulsed current-voltage setup with test device at termination of transmission line.

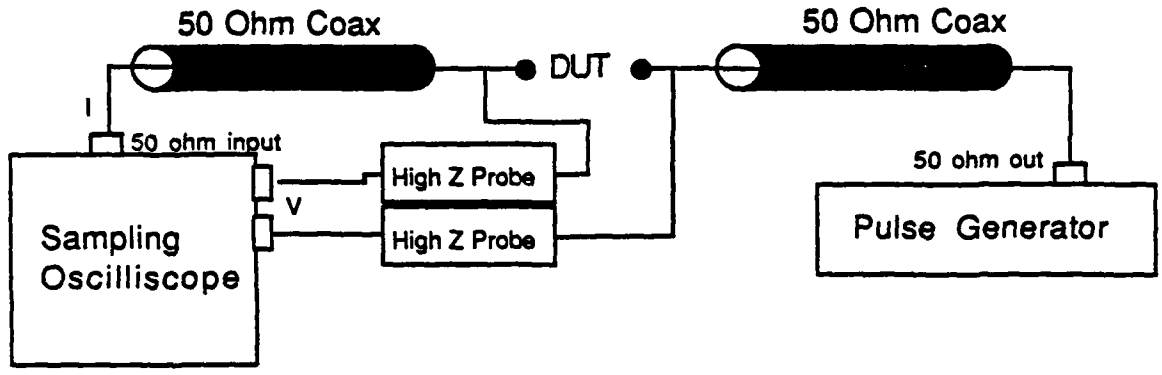

Figure 7. Pulsed current-voltage setup with test device in series.

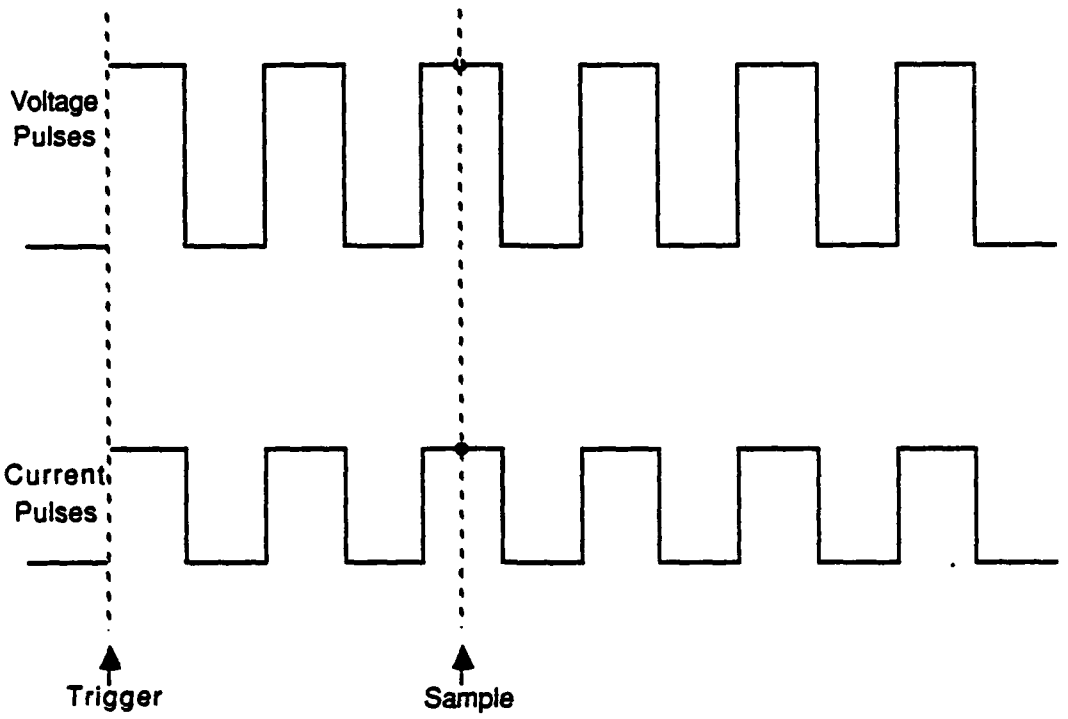

Figure 8. Pulsed current-voltage setup - time domain picture.

3. THE HETEROSTRUCTURE HOT ELECTRON DIODE

The heterostructure hot electron diode, or HHED, is a two-terminal heterostructure device that exhibits S-shaped negative differential resistance via the transition from electrons tunneling through a heterostructure barrier to being thermionically emitted over the barrier. This structure has been demonstrated to be capable of generating microwave oscillations[20] and has shown potential as a high speed two-state switch. The heterostructure hot electron diode, as shown in Fig. 9, is a simple structure consisting of a nominally undoped low bandgap semiconductor layer adjacent to a nominally undoped high bandgap barrier layer, sandwiched between two heavily doped low bandgap semiconductor layers with ohmic contacts placed on each end (see Section 2.2 for details of the construction). In practice, and for purposes of clarity here, the n^+ semiconductor layer contacting the barrier layer will be referred to as the starting substrate for epitaxial growth and all potentials will be referenced to this substrate as ground, although this order of growth is in no way necessary for fabrication or operation of the device.

Application of a negative bias to the top contact of the heterostructure hot electron diode causes electrons to accumulate at the tunneling barrier heterointerface after being supplied from the top contact and drifting through the low gap lightly doped drift region (see (a) in Fig. 9). Initially these electrons are confined by the potential step (conduction band offset) of the tunneling barrier and form a two-dimensional accumulation layer at the interface between the drift region and the tunneling barrier (henceforth this interface will be referred to as the tunneling interface) and the entire bias voltage is dropped across the tunneling barrier. There is a slight band bending in the drift region near the interface due to the accumulation of negative charge at the tunneling interface. This small potential well at the interface

gives rise to at least one energy subband at bias voltages in the region of operation of the HHED[21]. As bias voltage is increased the combined effects of increased electron accumulation at the tunneling interface and the effective thinning of the triangular barrier cause significant field emission to occur (see (a), (b), and (c) in Fig. 9) . At this point the increase in tunneling current density necessitates an electric field (the drift field) in the drift region in order to supply carriers to the tunneling interface. As bias potential continues to increase the tunneling barrier becomes thinner in profile, causing tunneling current and the subsequent electric field in the drift region to increase. This process causes the electrons traveling across the drift region to acquire energy from the drift field and impinge upon the tunneling interface at energies higher than the quantized subbands in the accumulation layer ((c) in Fig. 9) due to their kinetic energy perpendicular to the barrier that has been acquired from the field. Since electrons arriving at the tunneling interface at energies above the bottom of the band (or in this case the lowest subband in the accumulation layer) have a higher transmission probability than the cold, two-dimensional electrons, the heating action of the drift field gives rise to a second mechanism tending to increase the tunneling current, in addition to the thinning of the triangular barrier. This thermally assisted tunneling phenomenon gives rise to a feedback mechanism of electron heating in the drift region causing increased tunneling, and the increased tunneling causing more electron heating. This process continues until a current density is reached where the conduction path is primarily thermionic emission with no more to be gained from the tunneling process and the device behaves in an ohmic manner ((d) in Fig. 9). As one can see in the accompanying current voltage traces of Fig. 9 the enhanced thermionic emission/heating effect gives rise to a region of negative differential resistance. In order to visualize this it is important to note the redistribution of electric fields that takes place in the device, as in (b) and (d) in Fig. 9 which show the same total bias voltage but have different field distributions.

Note that in (d) in Fig. 9 the electric field in the tunneling barrier is reduced compared to (b) in Fig. 9, but the electric field is increased in the drift region, giving a higher current due to thermionic emission over the barrier and thermally assisted tunneling. The reduction of electric field in the tunneling barrier has little effect on the drift velocity of electrons in the barrier region since the fields in the tunneling barrier are well beyond the threshold value for the saturation velocity in the barrier;[22] a slight electric field reduction due to redistribution has virtually no effect on the rate at which charge is removed from the barrier region. The above velocity field relation holds true for any $Al_xGa_{1-x}As$ barrier of sufficient Al composition to be useful as a barrier in the heterostructure hot electron diode. Since the electric fields in the tunneling barrier are very high prior to switching (typically over 300,000 V/cm),[13] scattering into indirect minima in the GaAs drift region when in the on state (hot electron fields present in the drift region) is dominant, and most of the thermionic emission takes place via the indirect L valley.[23]

It should also be noted that the reverse bias (positive potential applied relative to the substrate) should not produce any switching via the transition to thermionic emission. In reverse bias the electrons, which would now be incident from the substrate side, impinge on the tunneling barrier from a heavily doped low bandgap semiconductor region. Since this bias lacks a lightly doped drift region for the electrons, there is no region to support a carrier heating electric field and hence no transition to thermionic emission. In this reverse, or non-switching, bias one should observe a monotonically increasing turn-on characteristic in the current-voltage trace as is associated with field emission current through a triangular (under bias) barrier.

3.1 Multiple Barrier Heterostructure Hot Electron Diode

Initial work with single barrier heterostructure hot electron diodes produced switching only at a very low temperature and in a pulsed dc configuration[5]. These unsatisfactory results led to experiments with multiple barrier devices[13] based on the notion that an enhanced switching effect could be obtained from a series application of the fundamental switching concept. The resulting multiple barrier device (Fig. 10) showed promise as a switching device and demonstrated dc operation in the device 'on' state, a characteristic that had not been previously observed in the single barrier devices. In addition to our work, a series of papers (Belyantsev et al. and others)[24,25,26] provided additional evidence supporting S-shaped negative differential resistance in multiple quantum wells, although with a completely different theoretical explanation of the switching behavior, as is presented below.

3.1.1 Other relevant S-shaped negative differential resistance devices

Several reports of S-shaped negative differential resistance in multiquantum well heterostructures have been made by workers in the Soviet Union[26], with an accompanying theory[24,25]. This structure differs from the heterostructure hot electron diode in several important ways: it relies on a multilayered structure (i.e., the theory requires the injection of an electron from a high-bandgap, high electric field region into a low-bandgap, low electric field region, with the gain in kinetic energy in the high field region being essential to the theory); the low-gap region must be heavily doped in order to have zero electric field in the low bandgap wells (although there seems to be some contradictory evidence in the papers as whether the experimental devices are heavily doped or not), and finally a graded bandgap at the exit heterointerface of the low-bandgap well seems to be necessary to actually derive S-shaped negative differential resistance from the theory. See Figs. 11 and 12 for descriptions of the current-voltage trace and structure of the theoretical device.

Following the development of Refs. 24 and 25, the theory of switching in this device is as follows. Quoting from Mezrin and Troskov:

"When the current flows across such a structure an electron acquires energy from the field only in a wide gap layer [see Fig. 12], *where the field is high and the electron density is low. When it reaches a 'well,' electrons become rapidly thermalized because of frequency* (sic) *electron-electron collisions. After the subsequent thermal release of the already thermalized electrons to the next wide gap layer the electron subsystem in the heavily doped well acquires an energy* ΔE *which the electron obtains in the wide gap layer. This increases the electron temperature in the well. Since the number of electrons crossing the well (i.e., those crossing the narrow-gap layer) in proportional to the current, the electron temperature in the well is a function of the current."*

Contained in the above theory is the energy balance equation

$$\frac{j}{e}\Delta E = \frac{3}{2}n^{+}L^{+}\frac{k_B(T_e-T_L)}{\tau_E}, n^{+} = N_D^{+} \qquad (3.1)$$

where ΔE is the energy transferred to the electron subsystem of a well by each electron that crosses it, L^+ is the thickness of the well, τ_E is the energy relaxation time in the well, T_e and T_L are the electron and lattice temperatures, respectively, and $n^+ = N_D^+$ are the doping and electron concentrations in the well. The theory also

includes the thermionic emission equation for the exit heterointerface of the well, expressed by

$$j = e\,\upsilon_R N_D^+ \left[\exp\left\{\frac{-e\phi_b}{k_B T_e}\right\} - \exp\left\{\frac{-e\phi_b}{k_B T_L}\right\}\right] \tag{3.2}$$

which can be approximated by

$$j = e\upsilon_R N_D^+ \exp\left\{\frac{-e\phi_b}{k_B T_e(j)}\right\} \tag{3.3}$$

for large bias, ignoring reverse current. In these two equations υ_R is proportional to the square root of the electron temperature T_e and is the rate of thermionic emission, which is close to the thermal rate, ϕ_b is the barrier height and $T_e(j)$ is the current dependent electron temperature. Quoting again from Mezrin and Troshkov:

"Since T_e on the current,m, it follows that in a certain range of voltages U (the voltage governs the energy ΔE which an electron acquires in the wide gap layer) Eq. 2 [Eq. 3.2] *has three solutions for the current for one value of the voltage, i.e., an S-type current voltage characteristic is observed. The first of these solutions corresponds to practically zero heating, when $T_e = T_L$, the second* [corresponds] *to a slight heating of the electrons (of the order T_e-$T_L = T_L$) and the third solution corresponds to a very strong heating (of the order $k_B T_e = e\phi_b$) when the current-voltage characteristic becomes practically ohmic"*

Using the more exact thermionic emission relation employing the T_L term (Eq. 3.2) one can solve for the low current (off) branch. Obviously for the trivial case of $T_e = T_L$, current is identically equal to zero, but this may be a good approximation over most of the low current branch. This solution occurs due to the necessity of including the third order terms in the thermionic emission equation at low electron temperatures (it also completely ignores the tunneling component under large bias).

Several additional objections to the above theory arise even if the substantial tunneling component is ignored, however. The general form of Eq. (3.3) (thermionic emission) seems to be inadequate for high electron temperatures ($k_B T_e = e\phi_b$), similar to the inadequacy of the Richardson constant thermionic emission equation. A more serious objection is the use of doping in the well of the order of $N_D = 10^{16}$ to 10^{17} and then neglecting depletion in the wells. This effect would seem to be much larger than the barrier lowering due to graded interfaces. In either case, significant carrier heating would be occurring in the wells (especially at $N_D = 10^{16}$), giving a net energy gain to the incident electrons, in a manner analogous to the heterostructure hot electron diode.

3.1.2 Observation of negative differential resistance in the multiple barrier heterostructure hot electron diode

As stated previously, early failures with single barrier devices resulted in experiments with devices containing multiple tunneling barriers and drift regions. The most successful of these were built as in Fig. 13, incorporating three drift regions and three barriers. However, since the lightly doped regions under bias would deplete (except for the one at a most negative potential, which has an accumulation layer of electrons screening any field from it) as in Fig. 10, this structure becomes

essentially a modified single barrier structure with a multiquantum well heterostructure barrier. The functions of these wells in the barrier are not completely understood (see the following section for some of the implications of the presence of these wells), but as is clear from the two biases shown in Fig. 10, only a negative bias relative to the substrate has the requisite drift region adjacent to a tunneling barrier, and hence an asymmetrical current voltage trace should be observed. This is indeed the case as is seen in Fig. 14, which is from a structure as pictured in Fig. 13, with GaAs wells and $Al_{0.45}Ga_{0.55}As$ barriers. This basic current-voltage was reproduced in a variety of structures similar to Fig. 13, with the Al content in the well areas varied. While the overall magnitude of the switching was variable as well composition changed (with no clear pattern emerging, implying that growth and fabrication variations were more responsible for variations in switching voltage than small variations in well composition), the important characteristic asymmetry in the current-voltage trace remained.

3.1.3 Parasitic effects in the multiple barrier heterostructure hot electron diode

The problem of impact ionization in the multiple barrier heterostructure hot electron diode was realized very early in its development. Since the structure of the multiquantum well heterostructure hot electron diode is similar to that for many multiquantum well avalanche photodiodes,[27] it would be a reasonable first guess to attribute the switching in the diode to the impact ionization. While impact ionization certainly occurs in the device (as evidenced by both infrared and visible light emissions), there is considerable evidence showing that the impact ionization does not play an important role in the switching of the diode. The theory predicts enhancement of the impact ionization coefficient α (defined as the inverse of the mean distance in the electric field direction a carrier travels before impact ionizing)

for multiquantum well devices. Following the development of Brennan et al.[28] for α_z in a z-axis orientation of electric field

$$\alpha_z = \frac{eF_0}{E_{th}} \exp\{\frac{-h}{eF}\int_{E_m}^{E_{th}} (\frac{dE}{dk})^{-1} \frac{1}{\tau_{tot}^{ph}(E)}\, dE\} \tag{3.4}$$

where E_m is the average electron energy, $1/t_{tot}^{ph}(E)$ is the energy dependent phonon scattering rate and F_0 is the overall average electric field.

$$E_{th} = \int_0^{l_i} eF(z)\, dz \tag{3.5}$$

where l_i is a function of the threshold energy for impact ionization and the electric field. Starting from this model, which is derived from Shockley[29], Brennan et al. have developed this theory for a spatially varying field, which can account for the kinetic energy gained when crossing the heterojunction from a wide-bandgap region into a narrow-bandgap region. This theory shows a clear enhancement of impact ionization for multiquantum well structures. Numerical solution of this problem yields impact ionization rates for $AlxGa_{1-x}As/GaAs$ multiquantum well structures that are potentially several times higher than the rates for these bulk materials.[28] This is an important result for the multiquantum well heterostructure hot electron diode. While it indicates some impact ionization in the device, it shows that impact ionization is a small effect

in the relatively short (approximately 0.5 mm or less) devices with ionization rates not near the avalanche breakdown threshold.

Despite the evidence cited above, a series of experiments were undertaken to determine whether avalanche breakdown and/or hole accumulation was occurring in the device active area. Optical emissions from devices of various Al contents in the well regions were studied (hence the various well compositions in Fig. 13) in order to see if any hole storage and subsequent carrier recombination were occurring in the well areas. If this effect is observed it would indicate the possibility that stored positive charge in the wells was changing the field profile in the device (screening the electric field from the well areas and causing increased field in the barriers). This effect is unlikely since the low current densities (a few amps per square centimeter) observed in the device would require excessively long hole storage times (on the order of microseconds) to accomplish any significant field perturbation. In general, however, since it is inaccurate to assume these low current densities that are based on device area due to the current channeling effects in devices with an S-shaped negative differential resistance region in their current-voltage trace,[30] experimental evidence was sought. If significant hole storage and recombination in the well was present, optical emission from the device with a wavelength corresponding to the well bandgap (and hence Al composition) should be observed at a magnitude on the order of other optical processes in the device, as illustrated in Fig. 15. In all cases, the optical emission from the heterostructure hot electron diode was seen which corresponded to the cap layer Al composition (in addition to a strong peak attributed to absorbtion and reemission from the substrate) and it was only when the well composition was coincidentally the same as that for cap layer or the GaAs substrate that any light corresponding in wavelength to its bandgap was observed. This t havior is consistent with any holes created in the multiquantum well area being

swept out of the high field region and into the heavily doped cap layer prior to recombination. This result was further corroborated by operating the device in reverse (non-switching) bias. Since the mechanism for enhanced ionization is still present in reverse bias, optical emissions are present, and in this case correspond to the substrate composition - again consistent with holes drifting out of the high field region prior to recombination.

3.2 Single Barrier Heterostructure Hot Electron Diode

Initial experiments on the heterostructure hot electron diode were done with single barrier devices, as in Fig. 9. In these devices, the drift region was GaAs and the barrier was $Al_{0.45}Ga_{0.55}As$, with a band offset as in (a) in Fig. 16. As is shown in this figure (data in Fig. 16 are taken from Ref. 7), the $Al_{0.45}Ga_{0.55}As$ is near the Γ-L-X crossover point, and as a consequence all barriers are of roughly equal height with respect to the Γ minimum in the GaAs, with the additional property that the L minimum in the GaAs is at the same energy as the Γ, L and X bands in the $Al_{0.45}Ga_{0.55}As$. This gives the interesting result that the threshold energy for intervalley transfer of electrons in the drift region is approximately equal to the perpendicular energy required for thermionic emission over any of the Γ, L or X barriers. This means that when the device is in a high current state the dominant scattering into the L valley in the GaAs drift region[23] causes electrons to drift into the AlGaAs with almost no heterojunction discontinuity and only a slight change of effective mass ($0.11m_o$ in the GaAs L valley versus $0.124m_o$ for the $Al_{0.45}Ga_{0.55}As$). The early devices, which were built with the original intention of maximizing the Γ conduction offset while remaining direct (in the mistaken notion that transfer via the Γ valley was dominant), inadvertently took advantage of the momentum spacer transfer

effect which would eventually prove to be the key to room temperature operation in the heterostructure hot electron diode.

The first successful heterostructure hot electron diode devices were fabricated out of wafers with a $Al_{0.45}Ga_{0.55}As$ barrier and a 2000 Å GaAs drift region. There was no heavily doped cap layer incorporated into this structure, with the AuGe/Ag ohmic contact (see Section 2.2.2 for details) applied directly to the drift region. This top ohmic contact, which is a shallow diffusing contact[19], did not penetrate all the way through the 2000 Å drift layer and by varying alloy time and temperature and thereby contact depth the effective width of the drift region could be changed, thereby finding the proper combination of drift region width and barrier width to observe the switching effect. This procedure yielded the first working devices[5] as shown in Fig. 17.

The first device to exhibit room temperature switching and dc operation in the high current state was the GaAs/AlAs single barrier heterostructure hot electron diode[9]. This device, with a single GaAs drift region and a single AlAs barrier (see Fig. 18) takes advantage of the high GaAs/AlAs Γ conduction band offset (see (b) in Fig. 16). This band structure provides both an effective tunneling barrier to the cold Γ electrons in the device off state and a lowered barrier to the energetic L and X electrons impinging on the barrier on the on state.

The GaAs/AlAs heterostructure, with its Γ conduction band offset of more than 1eV,[7] provides an excellent tunneling barrier to room temperature electrons, with very little thermionic emission via the X and L valleys, even though the Γ-X conduction band offset for GaAs/AlAs is only 0.2eV. This is due to the necessary intervalley phonon processes for this type of thermionic emission, and as a result

less than 1% of the thermionic emission current predicted by the standard thermionic emission theory, which ignores any phonon contribution, is observed[8] in these indirect barrier structures. This efficient barrier can be seen in the positive bias region of Fig. 19 where lattice (room) temperature electrons are incident on the AlAs barrier from the heavily doped GaAs substrate. The positive bias turn-on voltage of approximately 8.5 Volts represents an electric field across the AlAs tunneling barrier of over 250,000 V/cm. Note that the positive turn-on voltage is higher than the negative (switching) bias. This greater turn-on is due to additional voltage being dropped across the depleted 1300 Å lightly doped GaAs drift region in positive (non-switching) bias. In the negative bias, even though the overall device turn-on voltage is lower, turn-on occurs at approximately the same magnitude of electric field in the barrier. There is an interesting consequence of the on state, however. In the on state with an electric field in the drift region, most of the heated electrons have scattered into the L and X valleys.[23] These electrons then see the much lower X and L barriers (in the X valley the electron actually gains energy when crossing the heterojunction) in addition to a small (15%) increase in effective mass, which further enhances the effect of reduced impedance via the transmission to thermionic emission.

In Fig. 19, the total device current is shown rather than current density. In general, the switching current in the heterostructure hot electron diode is poorly correlated with the device area. This is due to the current channeling effect found in S-shaped negative differential resistance devices[30] which results in very small (on the order of a few square microns) areas of high current density while the surrounding device area is at essentially zero current density. We have made direct optical observation of the channeling effect of these structures. When the heterostructure hot electron diodes are operated at low temperature (15K), impact ionization, which is not necessarily a desirable effect in the heterostructure hot

electron diode, creates enough holes so that their spontaneous light emission upon recombination can be observed through an optical microscope (the device current voltage characteristics are essentially independent of temperature with only a slight increase in forward and reverse turn-on voltages at low temperature). Operating the devices at low temperature also decreases the band-to-band recombination wavelength, further aiding the direct visual observation. Such current channeling effects, which are a general property[30] of S-shaped negative differential resistance devices, provide a correlation between experimental switching current density and theory.

3.3 Superlattice Barrier Heterostructure Hot Electron Diode

A series of heterostructure hot electron diode devices were built which incorporated a GaAs/AlAs superlattice for a barrier, rather than a layer of bulk alloy material. These wafers showed a variety of surprising effects, all attributed to the superlattice. Devices were grown in the normal sequence for a single barrier heterostructure hot electron diode with the substitution of a GaAs/AlAs superlattice for the barrier, as in Fig. 20. In all cases, the superlattice was maintained at 1500 Å by adjusting the total number of periods. A first series of wafers was grown incorporating a 1300 Å GaAs drift region and the following different superlattice barriers: a 17-period superlattice, AlAs/GaAs, 75Å/50Å; a 10-period superlattice, AlAs/GaAs, 105A/50A; and a 12-period superlattice, AlAs/GaAs, 75Å/50Å. In all of these devices S-shaped negative differential resistance was observed in the normally nonswitching bias, i.e., for a positive bias with electrons incident on the drift region from the superlattice. Since S-shaped negative differential resistance in this bias cannot be explained by the normal theory, another explanation of this behavior

is in order. This problem is treated in Section 3.3.1, prior to the discussion of the negative (normal heterostructure hot electron diode switching) bias results.

3.3.1 Positive bias switching in the superlattice barrier heterostructure hot electron diode

Figure 21 shows the current-voltage trace of a superlattice barrier device (the drift region is 1300 Å of GaAs and the barrier is a 12-period superlattice, AlAs/GaAs, 75Å/50Å) in both negative, or normal switching bias (top trace), and positive bias (bottom trace).

In order to account for the S-shaped negative differential resistance in positive bias, the following theory was developed: Since the electrons in positive bias are incident on the drift region from the superlattice, if one can assume that the electrons gain a large amount of kinetic energy when crossing the heterojunction between the superlattice and the drift region, it is then plausible that nearly 100% of the incident electrons impact ionize in the drift region. This would cause the holes to drift toward the superlattice and accumulate in the valence band offset at the junction between the drift region and the superlattice and a subsequent screening of the electric field in the drift region. (See (a) in Fig. 22 for a description of the fields and terms in the following theory.)

Assuming that there is no charge at the interface of the heterostructure hot electron diode prior to positive bias switching, then the following relation holds:

$$\frac{F_D}{F_B} = \frac{\varepsilon_B}{\varepsilon_D} \tag{3.6}$$

where F_D,and F_B are the fields in the drift region and barrier, respectively, and ε_D, ε_B are the dielectric constants.

$$F_D = \frac{V_{tot}}{w_D + \frac{\varepsilon_D}{\varepsilon_B} w_B} \tag{3.7}$$

where V_{tot} is the total applied voltage. Then

$$Q_s = \varepsilon_B F_B \tag{3.8}$$

and

$$n_s = \frac{\varepsilon_B F_B}{e} \tag{3.9}$$

where Q_S is the sheet charge accumulated at the interface of the substrate and the superlattice barrier, and n_S is the sheet electron concentration. Then,

$$n_s = \frac{\varepsilon_B}{e}\left(\frac{V_{tot}}{w_D + \frac{\varepsilon_D}{\varepsilon_B} w_B}\right) \tag{3.10}$$

Corresponding to n_s is a depletion of the heavily doped cap layer. Once the current starts to flow, virtually all of the electrons incident in the drift region from the barrier impact ionize (assuming a high effective band offset, i.e., electrons incident from bound states high in energy in the superlattice). The holes resulting from the impact ionization then drift to the valence band notch at the superlattice/drift region interface (see Fig. 22 (b)). Assuming that n_s changes very little in this process (a good assumption since increased current requires very little increase in the barrier field F_B). The drift region field F_D will decrease proportionally to h_s, the sheet hole charge accumulated at the drift region/superlattice interface valence band discontinuity. Since the typical F_D prior to switching is approximately 500,000 V/cm for superlattices of this sort, it could be reduced to perhaps 10% of its preswitching value and still be large enough to drift electrons out to the cap layer. This would mean that the total switching would be proportional to the length of the drift region (assuming virtually all the field in the drift region is screened by the hole accumulation of Fig. 22 (b). A series of wafers were grown to test this assumption, and while the switching voltage was not directly proportional to the drift layer width (possibly due to differences in impact ionization efficiency in the different samples), there was a general trend of increased switching for increasing drift layer thickness, as shown in Fig. 23.

When calculating the approximate energy gained by an electron crossing the interface, if one assumes Γ tunneling through the superlattice miniband for the case of narrow (41Å) AlAs barriers[31] or Γ sequential tunneling for the thicker barriers and ignores the electric field perturbation on the states, an n=2 bound state near the top of the 1.04 eV Γ-confined well in the AlAs/GaAs (50 Å wells) superlattice is calculated. This 50 Å well system gives the highest incident energy practically

attainable for a heterojunction in the AlAs/GaAs system. This means that less than one half of one electron volt of additional energy is required to be supplied by the field in the drift region for the threshold energy for impact ionization, resulting in a minimum electric field of only 32,000 V/cm in a drift region of 1300 Å after switching to a high current reverse bias state, and even lower fields for the longer drift regions.

3.3.2 Negative bias switching in the superlattice barrier heterostructure hot electron diode

The negative (normal switching) bias in the superlattice barrier device results in a switching process similar to the switching in the single barrier devices, with S-shaped negative differential resistance observed (see negative bias of Fig. 21). This behavior was observed in all the samples except the devices with the 17-period, 41Å/51Å, AlAs/GaAs superlattice barrier. This device shows an N-shaped region of negative differential resistance prior to the S-shaped heterostructure hot electron diode effect. Resonant tunneling through AlGaAs superlattices generally manifests itself as tunneling via a narrow E_1 miniband with multiple negative differential resistance regions due to an expanding high field domain breaking the E_1 miniband coupling, with a resulting transition to E_1-E_2 tunneling in the region of the high field domain[31, 32,33] (see for example Refs. 31, 32 and 34, which deal with the original problem of Bloch oscillations in superlattices). This is due to the combined effects of the high Γ point conduction band offset in GaAs/AlAs heterostructures (1.04 eV AlAs barriers) and the relatively wide (41 Å) barriers incorporated into this structure. This results in an E_1 miniband with width ΔE_1 = 0.15 meV[35], which is narrow compared to the ΔE_1's of 5 meV and 0.4 meV of Refs. 31 and 33. This weak coupling of miniband states is essentially equivalent to that of isolated E_1 states, with no observable tunneling current from one E_1 state to the E_1 state of the next well, hence resonant

tunneling occurs only when the applied bias is such that all of the E_1 levels are aligned with the next E_2 levels on their cathode side.

Several single quantum well tunneling experiments have shown that it is the Γ point potential which governs the resonance levels in AlAs/GaAs/AlAs quantum well resonant tunneling structures, with some speculation that the X-point may play a role.[35,36,37] The results shown here support the Γ-point profile confinement, as is illustrated in Fig. 24, which details the energy levels defined by the Γ conduction band corresponding to the electric field distribution at resonance (peak current, V = 7.84 V) in the I-V trace of Fig. 25. In this device, the zero bias miniband levels occur at E_1 = 154 meV, width ΔE_1 = 0.15 meV and E_2 = 573 meV, ΔE_2 = 2.8 meV, with a center to center separation of 419 meV. Under bias, at resonance, the stark shift to E_1 can be calculated by straight-forward means due to the depth of the E_1 subband and the resulting long life time of the state.[38] Using the method of Ref. 38, the stark shift to E_1 is 32 meV, resulting in E_1 = 112 meV.

At resonance (V=7.84 V in the trace of Fig. 25) there is a 460 mV drop per SL period, which corresponds to a 460 meV separation between E_1 and E_2. Since the Stark shifted energy of E_1 = 112 meV at resonance, this implies E_2 = 572 meV, essentially equal to the zero bias miniband. Thus, this device shows almost no energy lowering to E_2 due to the stark shift in this sample. Since E_2 at resonance is strongly coupled to propagating states, the stark shift cannot be calculated by the usual perturbation methods, and a good correlation to theory cannot be presented. It is also important to note that the sample to sample variation of total applied voltage at peak resonance is a few hundred millivolts, making the $E_2 - E_1$ separation somewhat imprecise. In estimating tunneling time out of the E_2 level at resonance, the WKB approximation along with a classical attempt frequency yield tunneling

times out of E_2 and into propagating states on the order of 20 ps, which is long compared to the various intra- and interband processes.

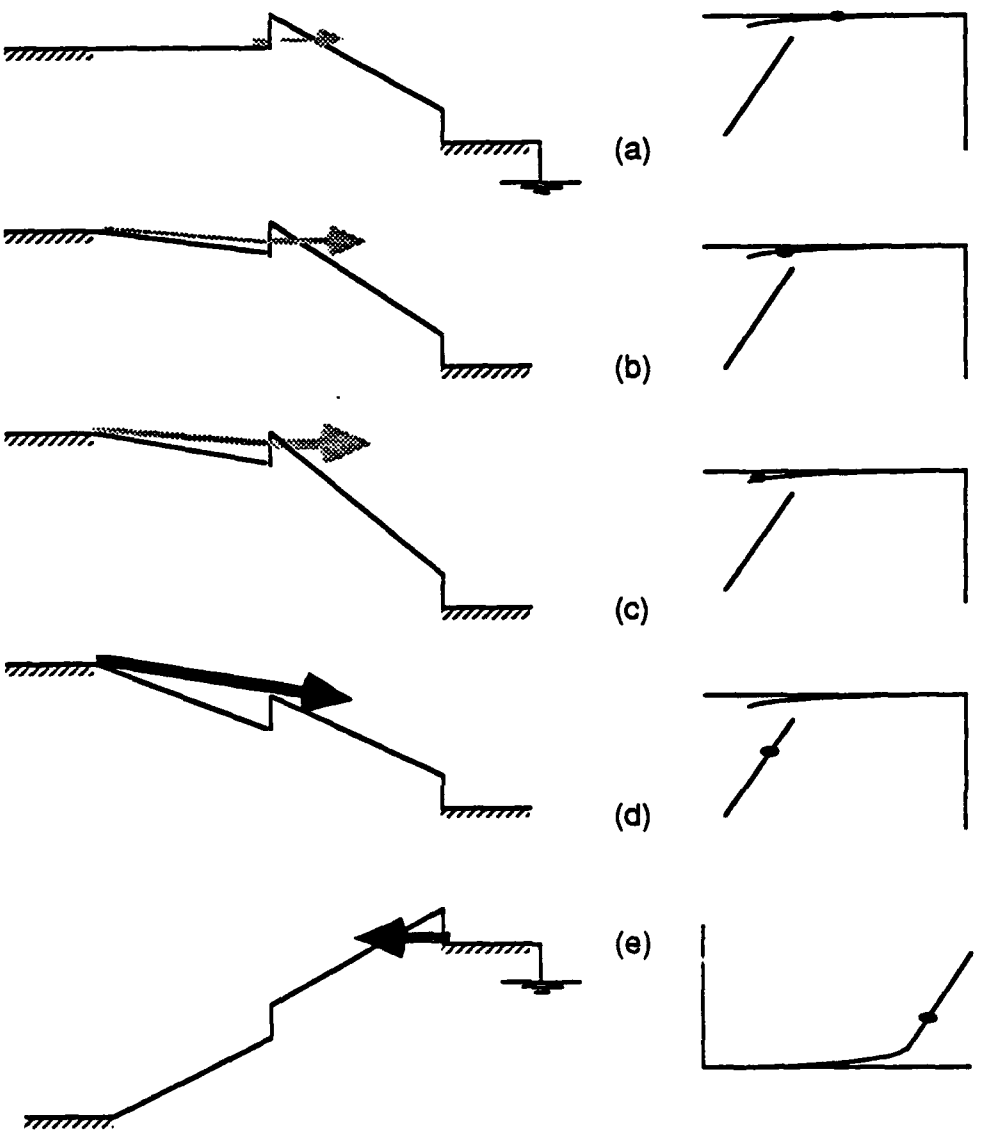

Figure 9. Conduction band-edge diagram of basic heterostructure hot electron diode showing: (a) initial low current state with low tunneling current and no electric field in the drift region, (b) and (c) increased current density with corresponding increased electric field in the drift region, (d) thermionic emission state and (e) reverse (nonswitching) bias.

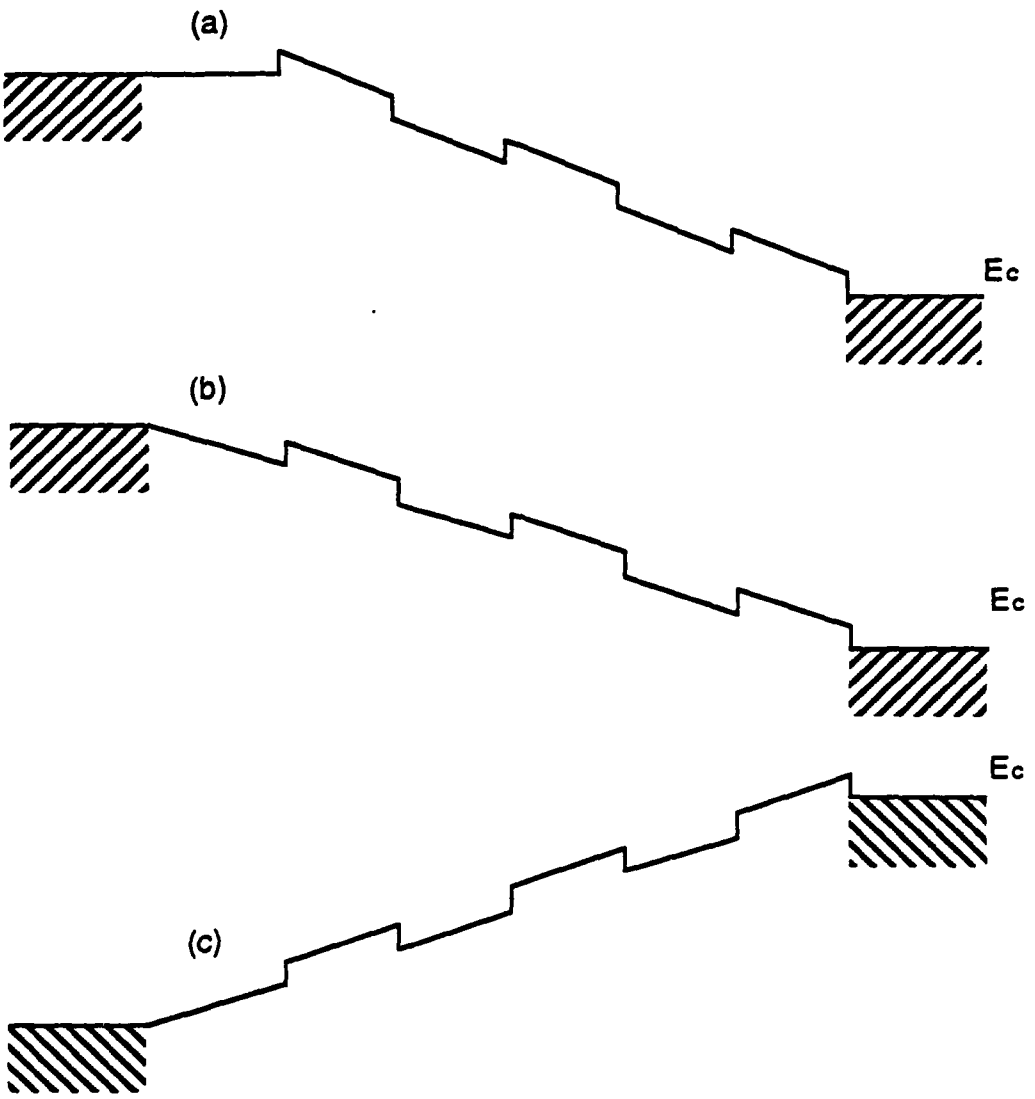

Figure 10. Conduction band-edge diagram of multiquantum well heterostructure hot electron diode under applied bias. (a) Switching (forward) bias in a low current state, (b) Switching bias in a high current state, and (c) Nonswitching (reverse) bias.

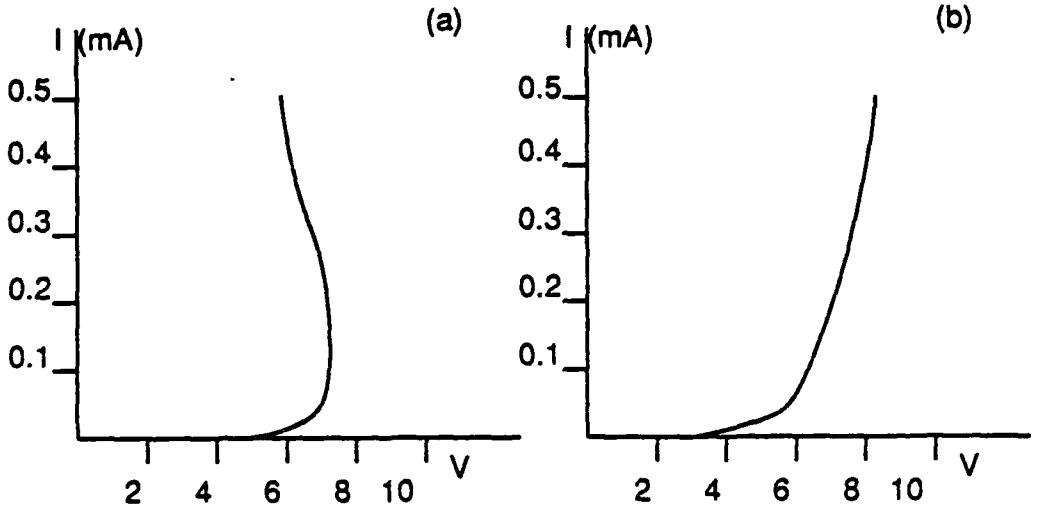

Figure 11. Current vs. voltage trace of switching in the device of Belyantsev et al. (Ref. 25), (a) eight-period structure, T=300K, (b) one-period structure, T=300K.

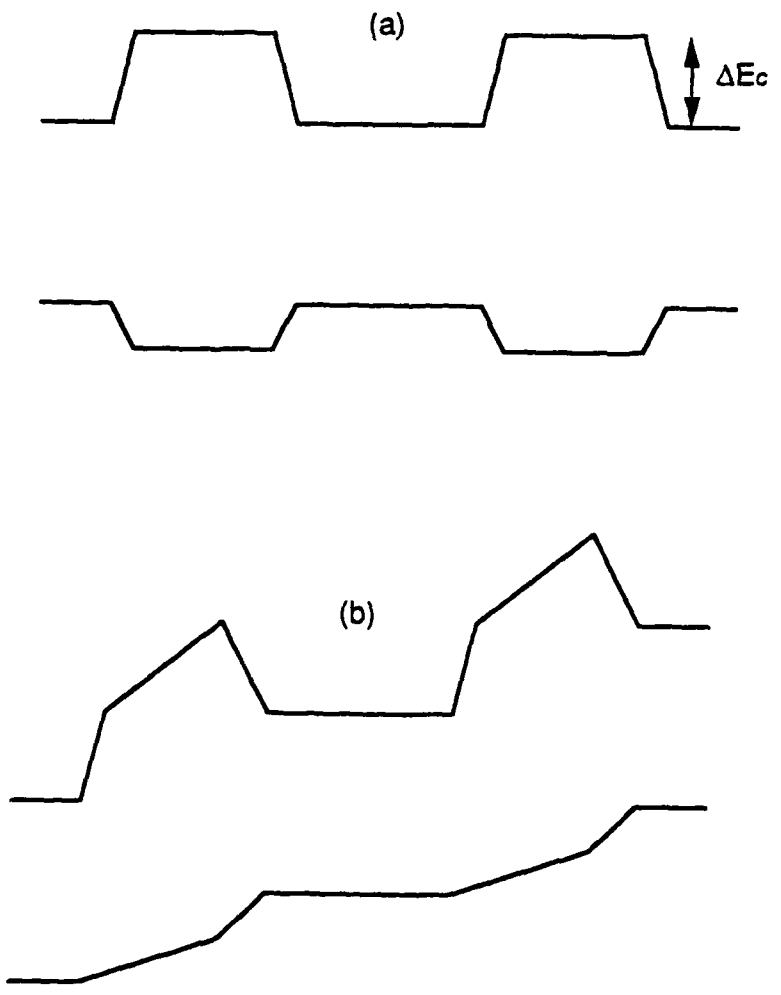

Figure 12. Conduction and valence band edge diagram of the device of Belyantsev et al. (Ref. 25) where ΔE_c is the barrier height in the conduction band showing (a) the zero bias case and (b) the switching bias. Note the nonabrupt interfaces necessary for device operation.

$Al_xGa_{1-x}As$

n^+cap	x=0,0.20
well	x=0,0.10
barrier	x=0.45
well	x=0,0.10
barrier	x=0.45
well	x=0,0.10
barrier	x=0.45
n^+buffer	x=0,0.10,0.20
n^+substrate	x=0

Figure 13. Structure of multiquantum well heterostructure hot electron diode showing various compositions utilized.

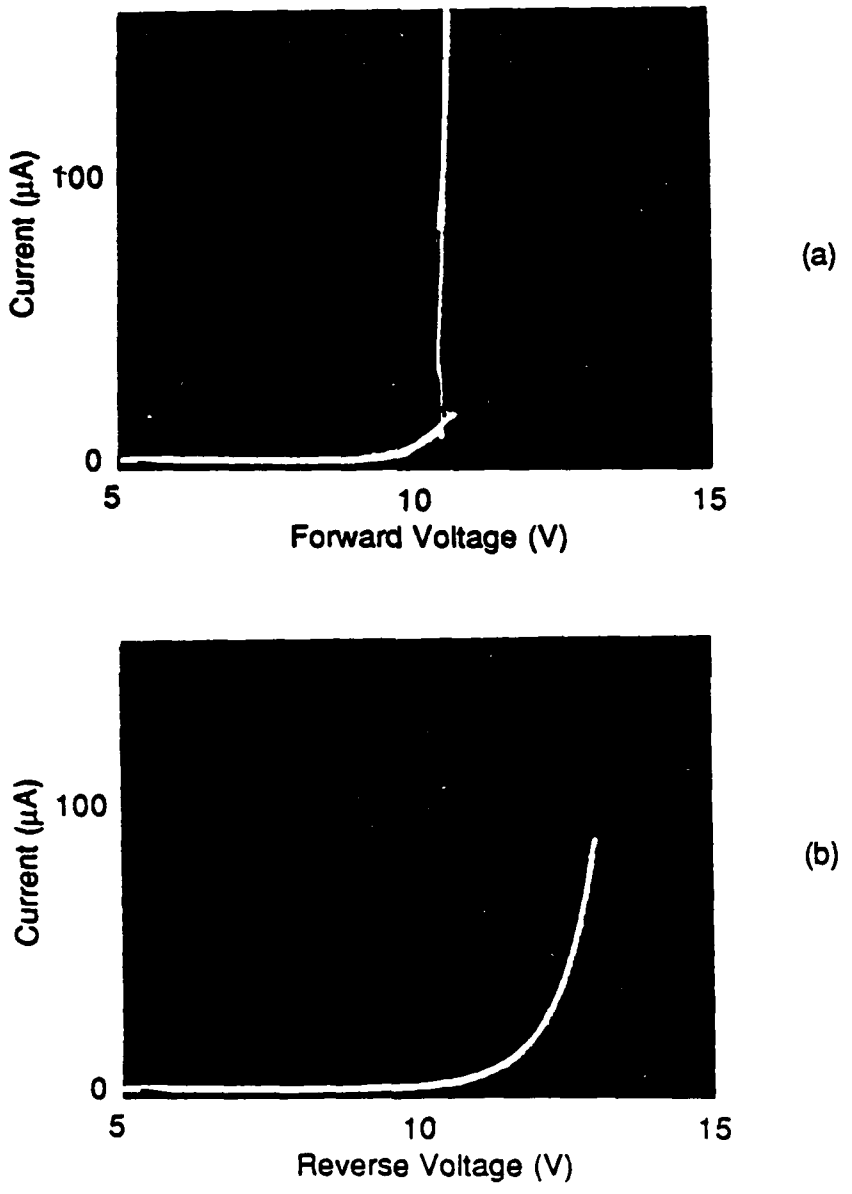

Figure 14. Current-voltage trace of the multiquantum well heterostructure hot electrondiode with GaAs wells and $Al_{0.45}Ga_{0.55}As$ barriers. (a) Forward voltage, (b) Reverse voltage.

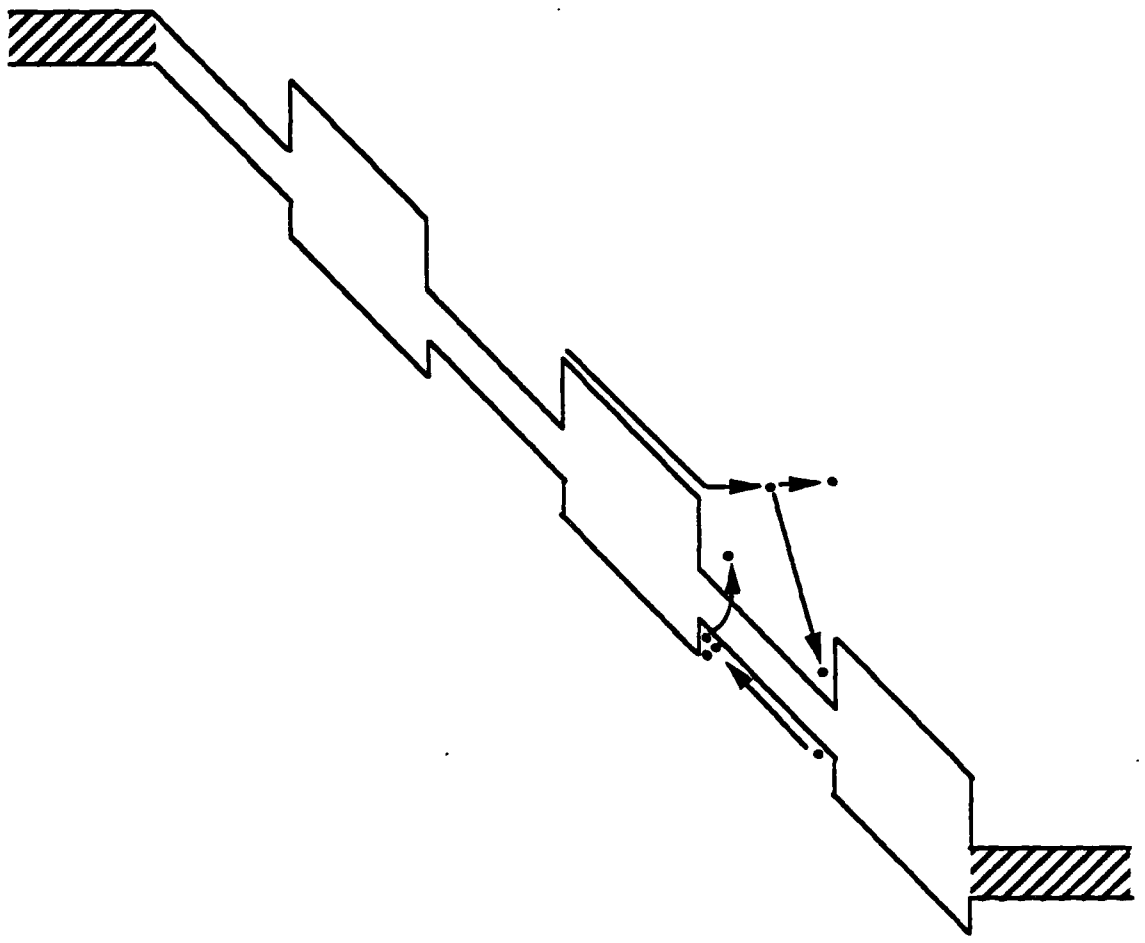

Figure 15. Conduction and valence band diagram of multiquantum well heterostructurehot electron diode under bias showing possible electron and hole recombination.

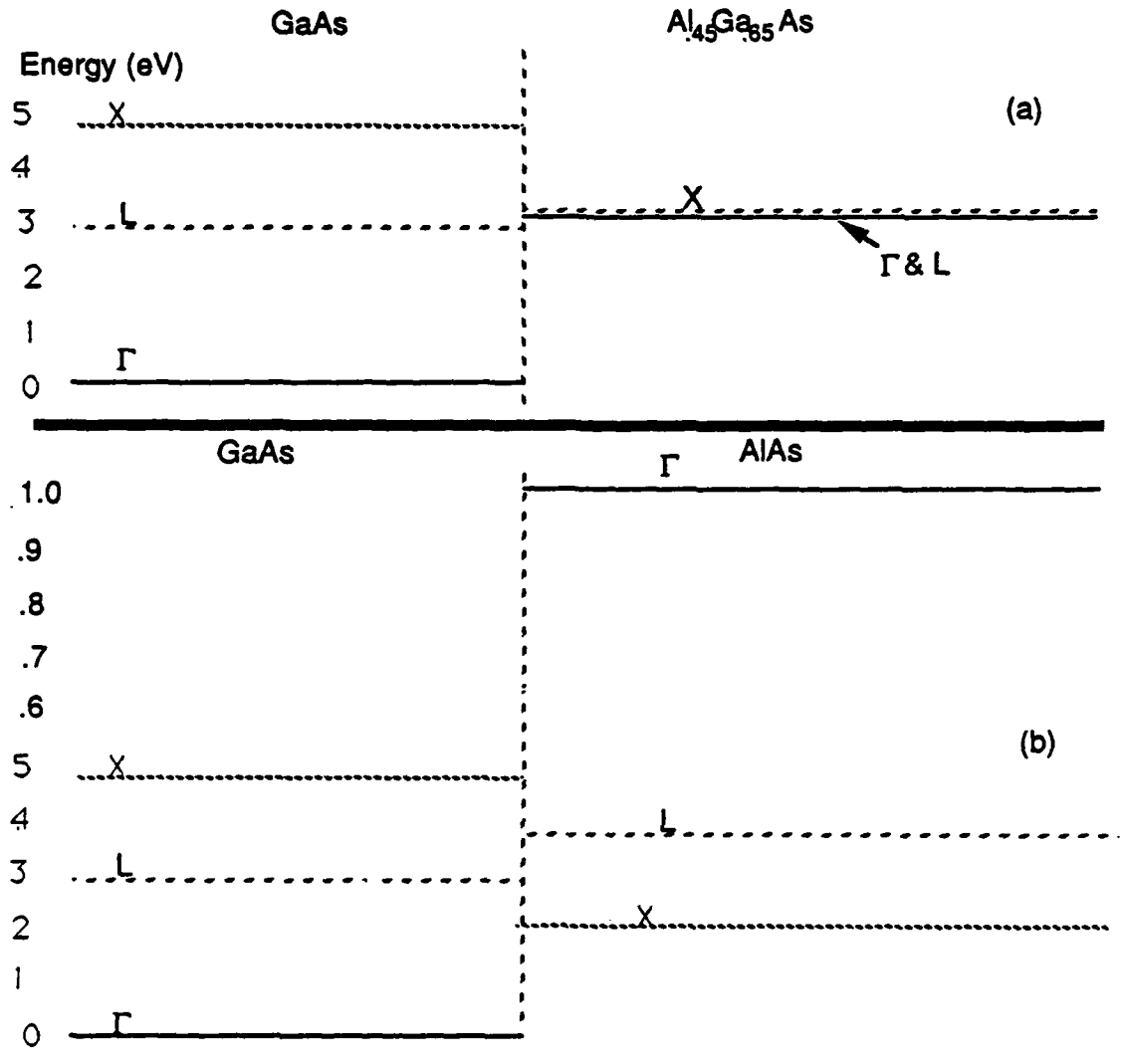

Figure 16. Conduction band edge offsets for: (a) GaAs/$Al_{0.45}GA_{0.55}As$ and (b) GaAs/AlAs interfaces.

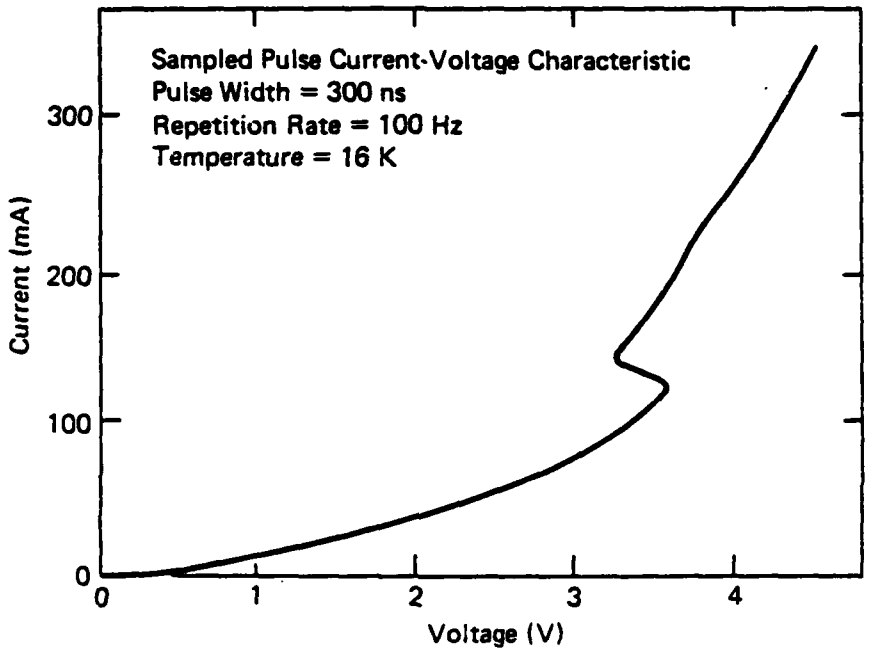

Figure 17. Current-voltage trace of single barrier heterostructure hot electron diode incorporating a single drift region and a single $Al_{0.45}Ga_{0.55}As$ barrier.

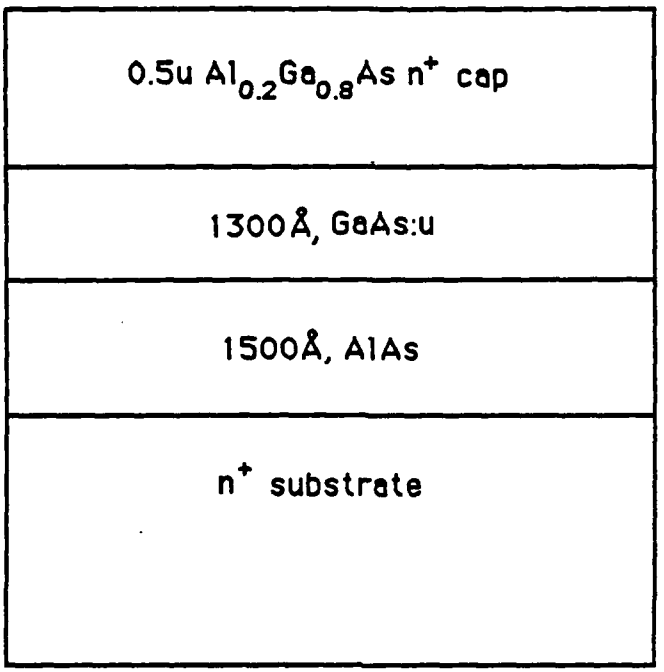

Figure 18. Structure of GaAs/AlAs heterostructure hot electron diode.

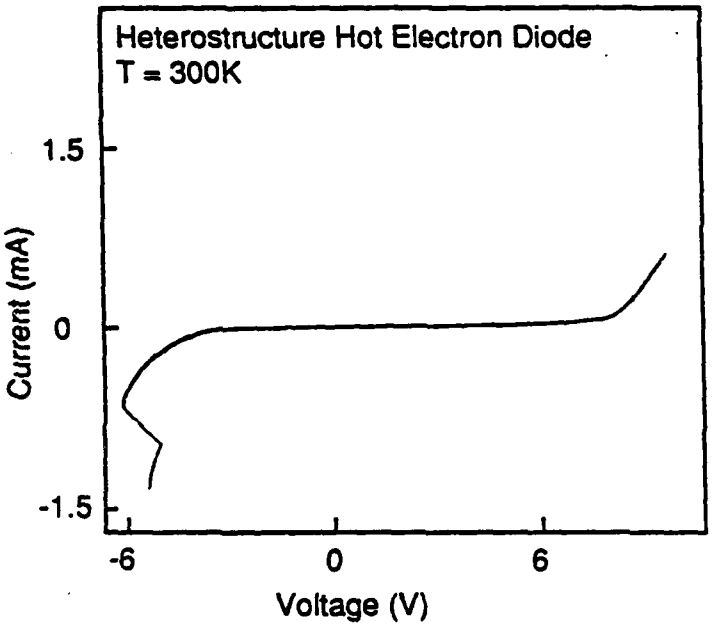

Figure 19. Current voltage trace of AlAs barrier heterostructure hot electron diode.

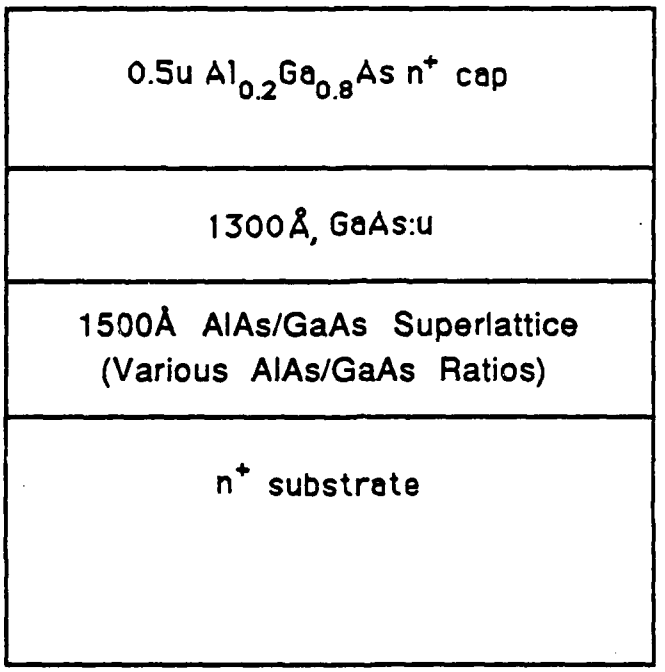

Figure 20. Structure of superlattice barrier heterostructure hot electron diode.

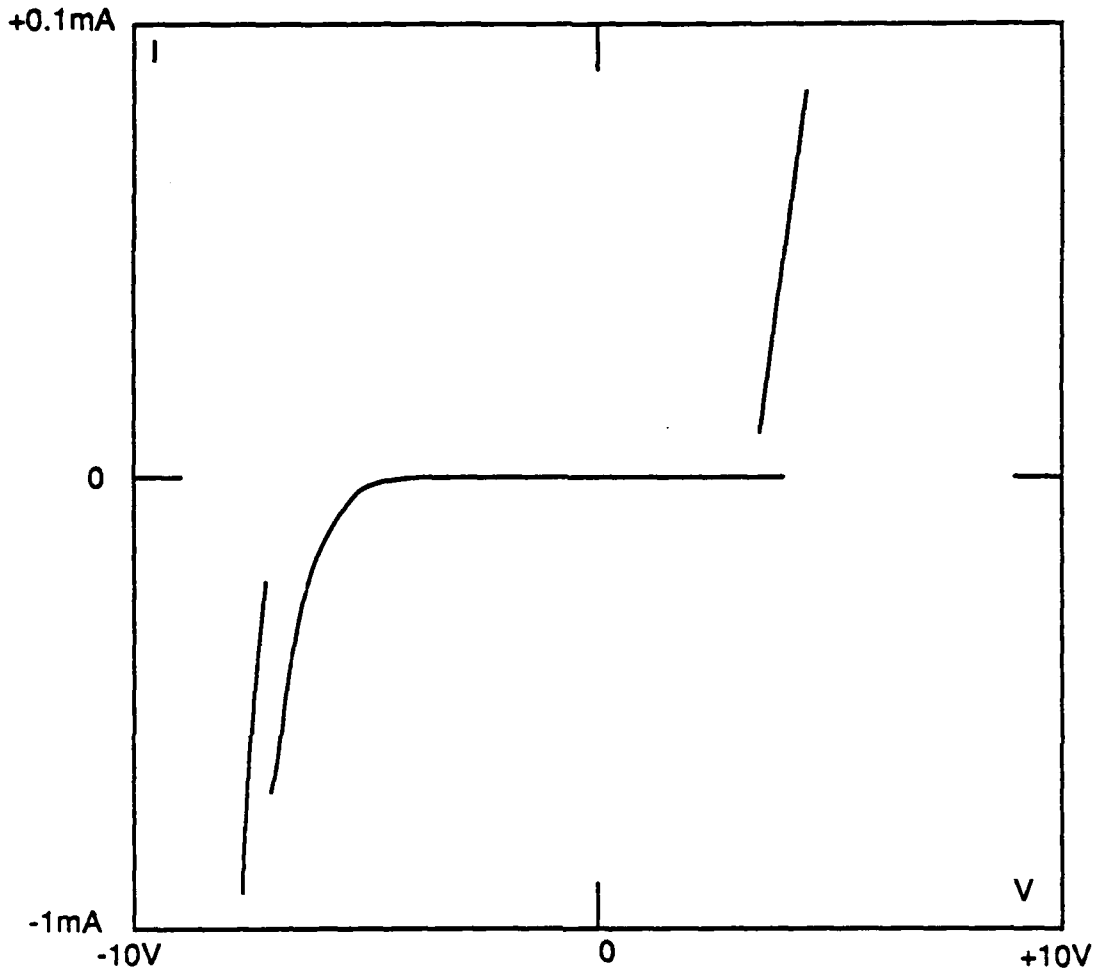

Figure 21. Current-voltage trace of superlattice heterostructure hot electron diode with1300 Å GaAs drift region and 17-period AlAs/GaAs (41Å/51Å) superlattice barrier. Note asymmetric current scale.

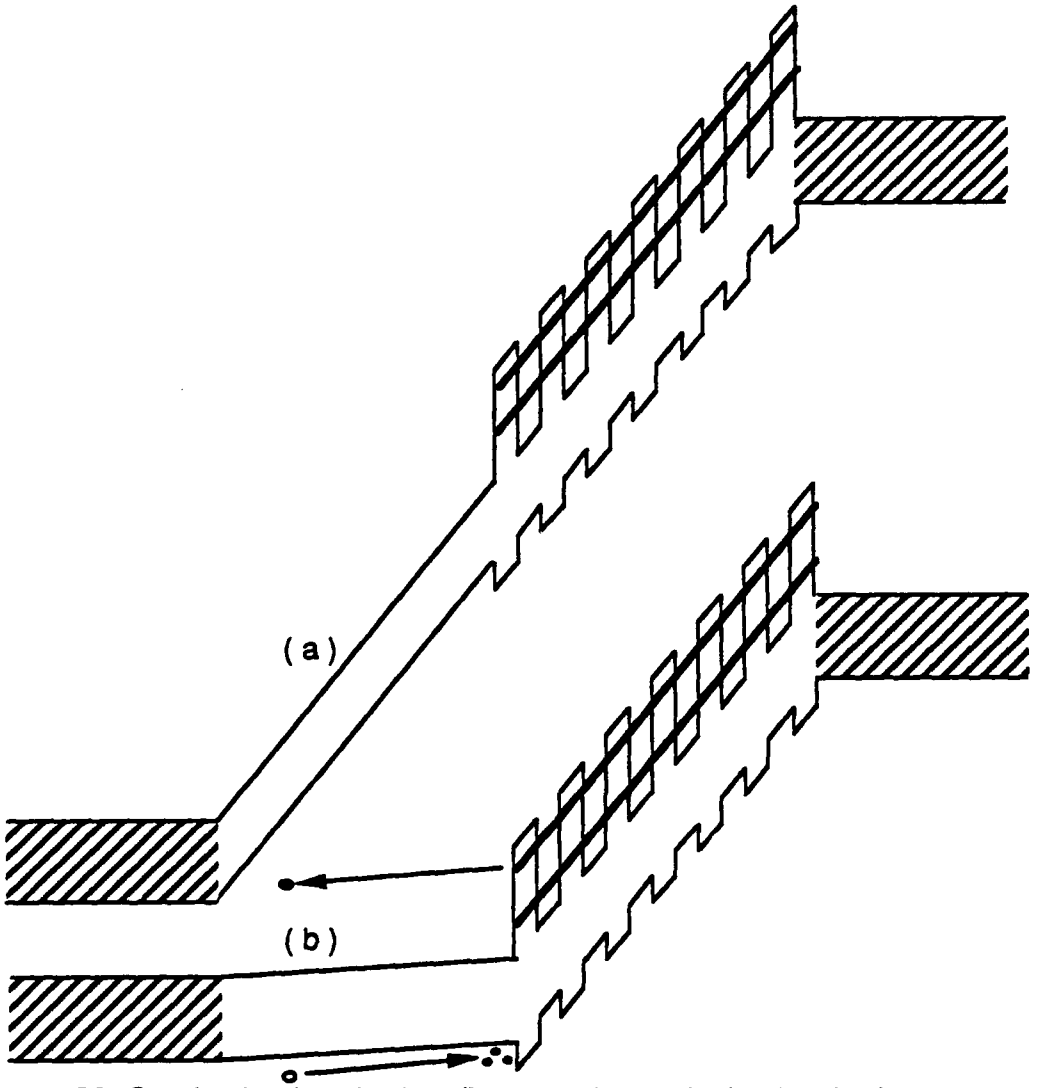

Figure 22. Conduction band edge diagram of superlattice barrier heterostructure hot electron diode including miniband states showing: (a) electric field prior to positive bias switching and (b) hole accumulation at tunneling interface after switching.

Device	Drift Region Length	Switchback (volts)
H71111-15-118	1300Å	4.5V
H71121-17-120	2600Å	6V
H71121-20-120	600Å	1.3V
H71122-20-120	325Å	2V

Figure 23. Data from positive bias switching in superlattice heterostructure hot electrondiode for different length drift regions.

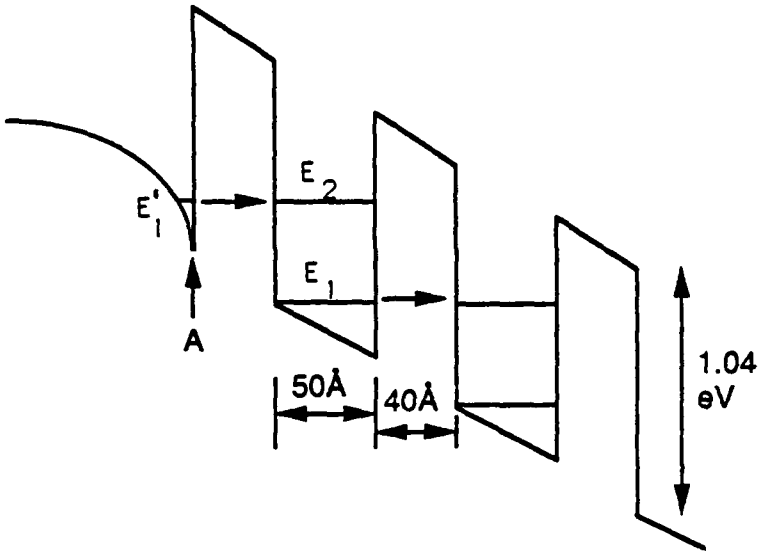

Figure 24. Details of 41Å/51Å AlAs/GaAs superlattice under applied (negative) bias showing the accumulation layer at point A plus two quantum wells.

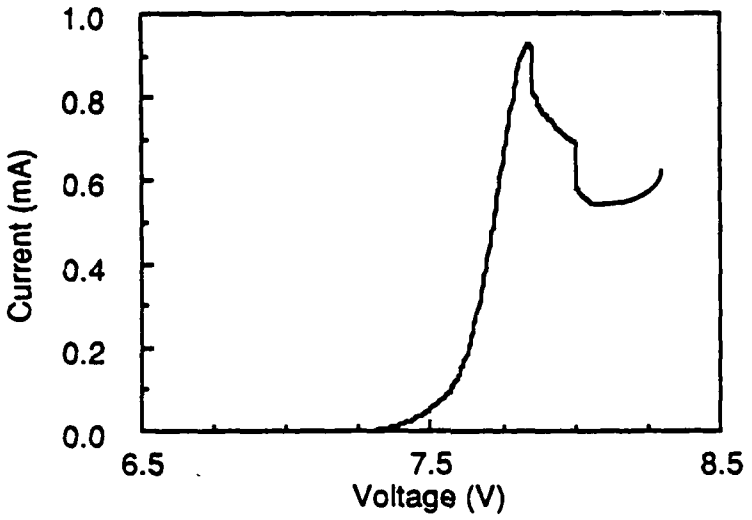

Figure 25. Current voltage trace of 41Å/51Å superlattice barrier device at T=4.2K

4. THE NEGATIVE RESISTANCE FIELD EFFECT TRANSISTOR

Real-space transfer as proposed[39] and later demonstrated[40,41] by Hess et al. has been shown to be an important mechanism influencing electronic transport in semiconductor heterolayers under the influence of high electric fields. The basic concept is that the temperature of an electron gas (two- or three-dimensional) will rise in high electric fields and the sufficiently energetic electrons can then be thermionically emitted (although in some cases the mechanism is thermally assisted tunneling) over interface barriers (band-edge discontinuities) oriented parallel to the high electric fields and thus populate other regions of the heterostructure. It is important to note that this transfer is perpendicular to the electric fields in the heterolayers and can result in depletion of a current carrying channel due to the attrition of electrons into surrounding regions of the heterostructure. As in any field effect device, channel electron density will vary as a function of distance along the source-drain electric field orientation.

The most successful device application of real-space transfer to date has been the negative resistance field effect transistor (NERFET).[6,42,43] The structure of this device is simply an undoped wide bandgap barrier deposited on a narrow gap n^+ substrate with an undoped narrow gap electron channel layer subsequently deposited on it; ohmic source and drain contacts are then made to the lightly doped layer along with a third ohmic contact to the n^+ substrate. In this device the single barrier provides two dimensional confinement for channel electrons (Fig. 26), which are induced into a potential well at the surface side interface by application of a positive substrate voltage (analogous to an inverted MOSFET with the high bandgap barrier acting as the oxide). A voltage applied between the source and drain contacts results in an electron heating field necessary for real-space transfer. The thermionic

emission of these two-dimensional electrons, which increases exponentially with electron temperature, is insignificant at low source-drain heating fields, but quickly becomes the dominant current path as the electric field is increased beyond a threshold value for thermionic emission. This sudden increase in the substrate current results in a concomitant decrease in the drain current and manifests itself as a region of negative differential resistance in the drain current vs. drain voltage trace (see Fig. 27). This N-shaped negative differential resistance can be quite significant, with peak to valley ratios as high as 160:1[43] in devices grown by MOCVD and having the same structure as Fig. 26.

It should be noted that as substrate voltage is increased in the NERFET, the high bandgap barrier becomes increasingly triangular and thermally assisted tunneling through the top of the barrier becomes significant. Tunneling, in fact, becomes the limiting factor in the operation of the NERFET, as can be illustrated as by the following. If we assume a simple capacitor relation for the barrier and neglect the small voltage dropped in the surface region, then the initial channel carrier concentration at the source end can be expressed by

$$(-e)n_{source} = \varepsilon_B F_B \qquad (4.1)$$

where F_B is the electric field in the barrier and ε_B is the dielectric constant in the barrier. Some limits can be inferred from this. If one assumes a barrier height of ΔE_c and ignores quantum subbands in the channel and one also assumes that when F_B is sufficiently strong for device operation the barrier is essentially triangular, we can

calculate the tunneling distance through the barrier for the cold electrons at the source as being

$$(-e)d_t = \frac{\Delta E_c}{F_B} \tag{4.2}$$

where d_t is the tunneling distance for cold electrons (the width of the trapezoidal barrier at its base). Assuming a barrier height of ΔE_C=300meV and a minimum d_t of 100 Å (at which point tunneling from the source-substrate diode limits the substrate voltage V_{sub}), we calculate a maximum allowable electric field in the barrier of F_B=300,000 V/cm; this results in an n_{source} of approximately $2x10^{12}$ electrons/cm^2. These numbers could be proportionately higher for increased ΔE_C but since the electric field in the barrier already approaches the value for dielectric breakdown at ΔE_C=300 meV, it can be safely assumed that n_{source} concentrations much above this value of $2x10^{12}$/cm^2 are unrealistic.

Interesting band structure consequences arise when considering devices such as that of Fig. 27. Since the barrier is constructed of $Al_{0.45}Ga_{0.55}As$ (near the Γ–L-X crossover point) and the top channel layer is GaAs, we see the interesting result (see Fig. 28) that Γ electrons in the GaAs channel layer which have enough energy to be thermionically emitted over the $Al_{0.45}Ga_{0.55}As$ barrier also have enough energy to be scattered into the indirect L valley. Due to the difference in effective masses between the Γ and L valleys the resulting density of states in the L valleys is some 70 times greater than that for the Γ valley, and which results in the intervalley scattering process from Γ to L being very efficient.[44,45,46] As a result, in this particular structure, virtually all electrons participating in the real-space transfer process do so from the indirect L valleys.

A fully analytical treatment of the NERFET by Grinberg et al.[21] reproduces many of the expected features of the NERFET, but the Monte-Carlo work of Kazilyalli et al.,[47] which provides a more precise solution of the electric fields present in the channel and also models the important role of the above-mentioned intervalley scattering as a mechanism of real-space transfer, shows results which are more consistent with the data presented here and elsewhere.[6,42]

4.1 Magnetic field experiment

In the NERFET with a positive substrate bias applied, the lattice temperature channel electrons are clearly confined to two-dimensional states at the $Al_xGa_{1-x}As$ interface (see the potential profile included in Fig. 26), but as soon as they gain enough energy from the source-drain heating field to be thermionically emitted over the $Al_xGa_{1-x}As$ barrier they are no longer confined in a potential capable of producing quantum confinement. In addition, in $Al_xGa_{1-x}As$ barriers of more than x=0.45 (indirect barriers) virtually all of the electrons scatter into the indirect L valleys prior to transfer across the barrier[47]. In other words, electrons are heated from two-dimensional states confined by the Γ potential into three-dimensional Γ states whereupon they scatter by means of longitudinal optical intervalley phonons into three-dimensional indirect L valley states prior to real-space transfer. While this change of dimensionality has always been assumed, no direct evidence was shown until the following magnetoresistance experiment was performed[48]. Structures grown and processed as in Fig. 26 were placed in a liquid helium dewar containing a superconducting magnet where they were cooled to 4.2K, and the effects of magnetic fields both perpendicular (B_Z) and para· (B_X) to the confining heterointerface were studied (see Fig. 26 for orientation). The effect of a magnetic

field perpendicular to the source-drain electron flow and perpendicular to the plane of the confining heterointerface (B_z) has been studied previously[49], and the expected low electric field magnetoresistance was observed. We have repeated this experiment and observed a similar reduction in drain current for increasing magnetic field strength when source-drain voltages are below the onset of real-space transfer. It should be noted, however, that with a width/length aspect ratio of approximately 200 in these devices, there is a significant Corbino resistance component (see, for example, Seeger[4]) at these low electric fields and the actual magnetoresistance of the sample in this orientation of magnetic field cannot be separated from the Corbino component without measurement of other geometry samples.

In addition, the effect of a high electric field on the magnetoresistance has not been thoroughly treated analytically. This is due to the shortcomings of the usual approximation of defining a momentum relaxation time, which is not appropriate in the high electric field regime. The high magnetic field behavior of the sample is, however, inconsistent with any magnetoresistance explanation that does not include the real space transfer effect. In the large source-drain heating field region we observe an increase in drain current as the strength of the magnetic field B_z is increased for drain voltages beyond the threshold for negative differential resistance (see (a) and (b) in Fig. 29). This increase in valley current with increasing magnetic field strength is observed until the negative differential resistance region is eliminated at approximately B_z=4 Tesla by the combined effects of increasing valley current and decreasing peak current. This raising of the valley current is due to the lengthening of the effective path of the electron travel and the resulting reduction of the rate energy is gained by the electron from the electric field. Since scattering rates are approximately independent of the transverse magnetic field, the resulting average energy of the electron distribution is lower and thermionic emission is

reduced.[50] At magnetic fields above 4 Tesla the entire current-voltage trace is suppressed as themagnetic field is increased ((c) in Fig. 29), again by a combination of Corbino and magnetoresistance effects.

The case of the magnetic field parallel to the heterointerface (B_x) but still perpendicular to the source-drain electric field (E_Y) is of particular interest. With this orientation we see clear evidence of a transition of the electron gas from the two-dimensional confined states to the three-dimensional propagating states.

For low electric fields only very small magnetoresistance effects associated with the distortion of the electron wave function (either biasing the electrons nearer to or farther away from the confining interface) by the magnetic field are expected.[51,52] In this case of a magnetic field parallel to the heterointerface but perpendicular to the electric field E_Y and for the case of two-dimensional confinement one would not expect to see any Corbino effect. However, one might expect to see a measurable Corbino effect if the electrons were not confined, i.e., assuming a device width of 2000Å (equivalent to the GaAs channel layer) and a length of 2μm (which would give a width/length aspect ratio of 0.1). Looking at the low field regions (a) and (b) of Fig. 30, we see evidence of only a small magnetoresistance which is dependent not only on the magnitude of the magnetic field but also its polarity, results which are consistent with two-dimensional confinement but not with any Corbino effect, which should be independent of the polarity of the magnetic field. While the polarity dependence is not clear from the curve tracer photographs in Fig. 30, it has been subsequently confirmed from measurements made by a Hewlett-Packard 4145B semiconductor parameter analyzer.

In the region of drain voltage (electric field) exceeding the critical voltage for negative differential resistance, dramatically different results are obtained. We observe a large dependence of drain current on both the polarity and strength of the magnetic field. The results agree at least qualitatively with the notion that the Lorentz force produced by (+/-) B_x exerts a significant force on the hot electrons. Given the classical equation of motion

$$h\frac{dK}{dt} = (-e)(F + (v \times B)) \tag{4.3}$$

magnetic fields in the Tesla range can apply (vxB) Lorentz forces to the confined electrons which are much larger than the forces exerted by the source drain heating field. This force can either aid or inhibit thermionic emission and the valley current can either be raised or lowered (with the opposite effect on the substrate current) depending on the polarity of B_X (see Fig. 30). This is in marked contrast to the small effect observed at low drain voltages and shows that electrons involved in real-space transfer can be subjected to a significant Lorentz force prior to transfer. This is consistent with confinement in a two-dimensional state where the Lorentz force has little effect as the electron gains energy (and therefore velocity parallel to the interface) until transition to a three-dimensional state where the electron experiences an (e)(vxB) perpendicular force, either aiding or hindering transfer, depending on the polarity of B_X. This is in marked contrast to the case of three-dimensional electrons which would have resonance orbit diameters of

$$d_n = 2\sqrt{\frac{h}{eB}}\sqrt{2n+1} = \frac{513}{\sqrt{B}}\sqrt{2n+1}\ \text{Å} \tag{4.4}$$

where B is in Tesla. For magnetic fields in the Tesla range Equastion (4.4) gives n=1 and n=2 orbits which are less than the typical thickness of 2000 Å in the GaAs channel layer. One would not expect to see such a pronounced polarity dependence for this case of no confinement.

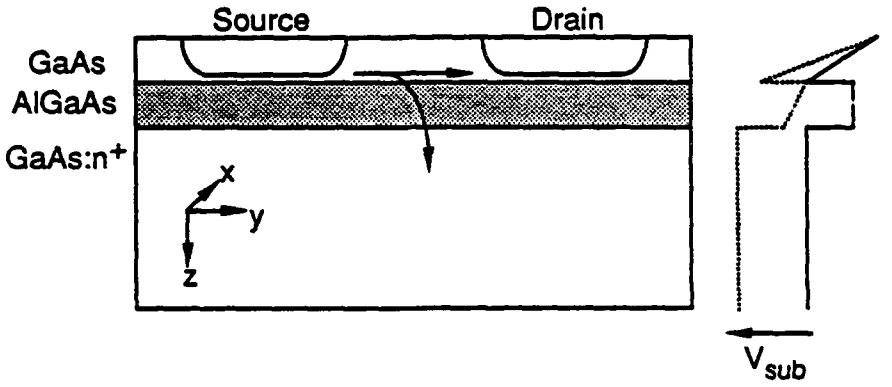

Figure 26. Schematic cross section and conduction band edge diagram (showing applied substrate bias V_{sub}) of negative resistance field effect transistor.

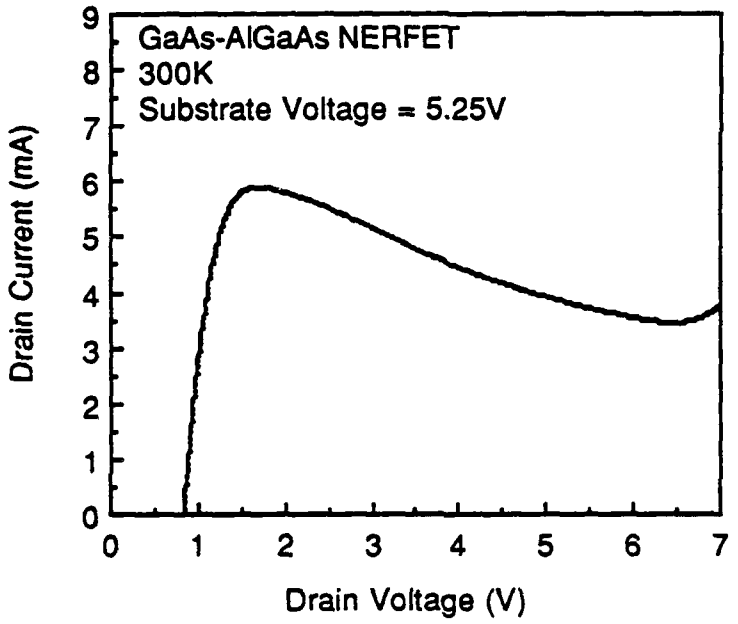

Figure 27. Current-voltage (I_D-V_D) trace of negative resistance field effect transistor.

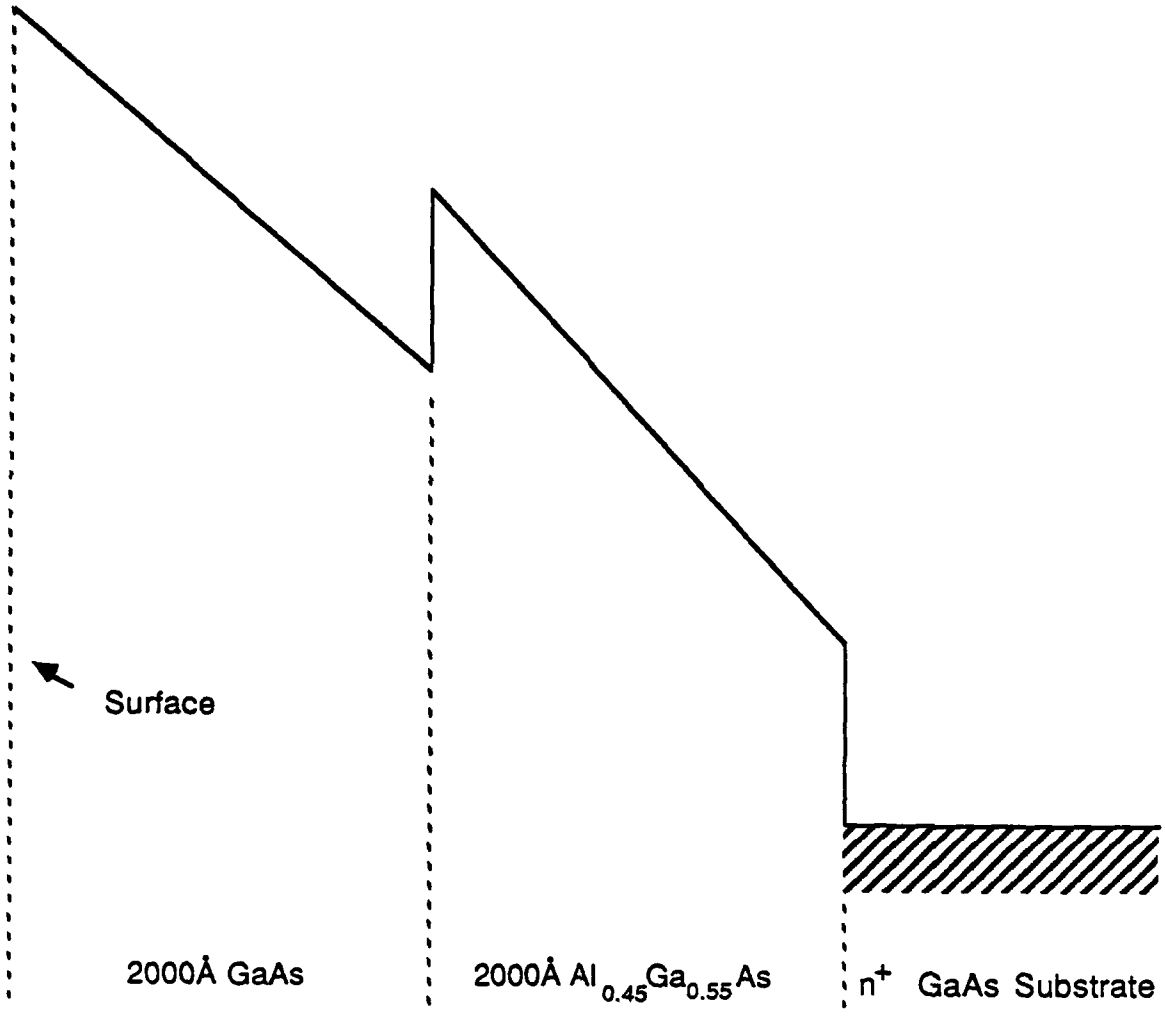

Figure 28. Conduction band edge diagram of a negative resistance field effect transistor with a GaAs channel and an x= 0.45 $Al_xGa_{1-x}As$ barrier.

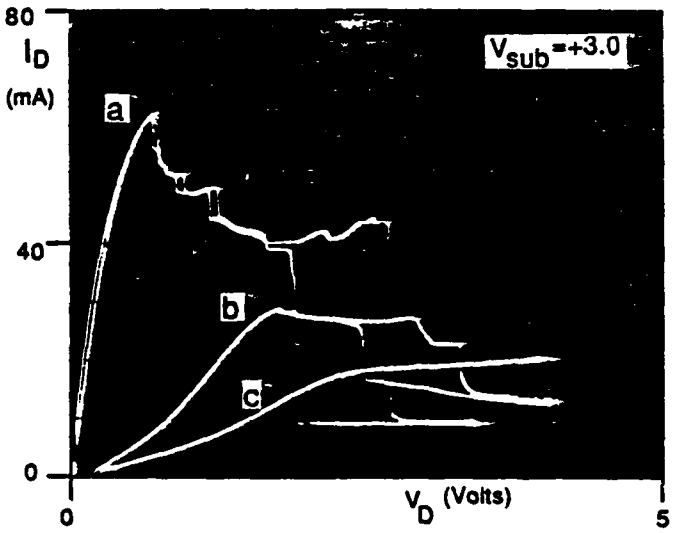

Figure 29. Effect of magnetic field on the negative resistance field effect transistor with magnetic field oriented perpendicularly to the epilayers where (a) B=0.6T, (b) B=4T and (c) B=8T.

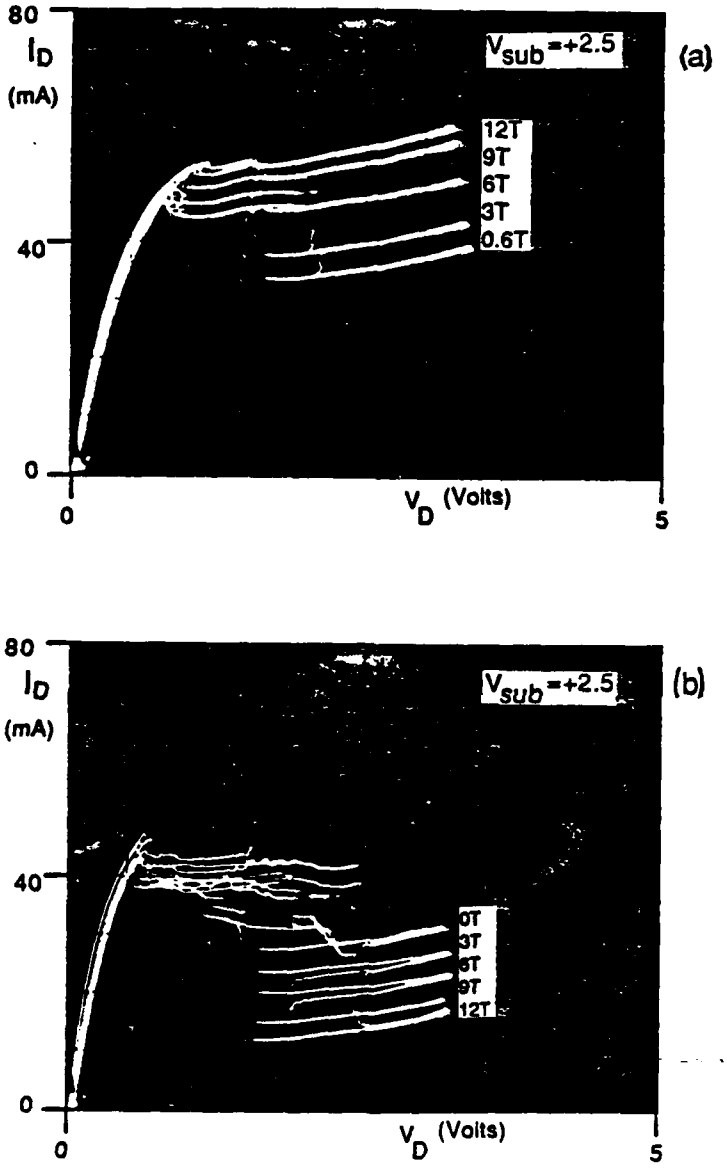

Figure 30. Multiple exposure of I_D vs. V_D at T=4.2K for various magnetic field strengths oriented along the axis parallel to the epilayers but perpendicular to the source-drain electric field (x axis of Fig. 26). (a) Negative B_x and (b) Positive B_x.

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