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AN/TAC-1 Demultiplexer Circuit Card Assembly

By

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This report describes the design, operation, and testing of the AN/TAC-1 demultiplexer subassembly. It demultiplexes the 6144 kb/s digital data stream received over fiber optic cable or tropo satellite support radio, and converts it into 2 digital groups and 16 digital channels. Timing recovery is accomplished by generating a 18432 kHz master clock synchronized to the incoming data. This master clock is divided modulo two to generate the proper group and loop timing.

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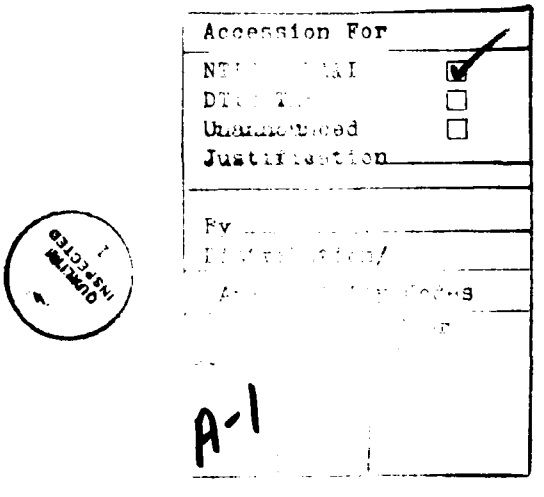
Robert D. Braun originally designed the AN/TAC-1 demultiplexer subassembly. The author took over the board where Bob left off, and made a number of modifications to correct minor problems and make the board easier to manufacture. This paper describes the design as it exists today.



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SECTION 1

INTRODUCTION

1.1 AN/TAC-1

This report describes the demultiplexer circuit card assembly (CCA) of the AN/TAC-1. The AN/TAC-1 is a 65-pound, throw-in-the-mud box designed to transmit multichannel telephone traffic over 6 kilometers of lightweight fiber optic cable. The unit is transported in a specially designed shipping container to field locations. The AN/TAC-1 will be used primarily to remote radio frequency transmitters, such as the AN/TRC-170 Troposcatter Radio, from the main operating location. This separates users from radiation seeking missiles fired at transmitting equipment by hostile aircraft.

1.2 DEMULTIPLEXER SUBASSEMBLY A1A1

The demultiplexer CCA is in the leftmost slot of card cage subassembly 1A1. Since the CCAs are numbered from left to right, the demultiplexer becomes CCA A1 in card cage assembly 1A1; therefore, the complete designation for the demultiplexer CCA is 1A1A1.

Figure 1 is a photograph of the demultiplexer card, which is 7.7 inches long by 6.6 inches wide by 0.064 to 0.070 inches thick. It is a multilayer board with a single plane for 5 V and another for ground. Signal-carrying traces have been placed on both outside layers for easy troubleshooting and isolation.

Two connectors are shown. On the right is a card edge connector with 2 rows of 50 pins each. It connects power and ground and provides all signal input and output connections to the board. This connector mates with another at the back of the card cage. The connector is uniquely keyed so that it will seat properly only when plugged into slot A1.

The smaller connector shown on the left is for test purposes. It consists of two rows of square 25 mil posts on 100 mil centers; the rows are spaced 100 mils apart. Each of the 24 pins is connected to a test point on the demultiplexer card. This connector is designed to mate with computer connectors that employ flat ribbon cable for automated testing.

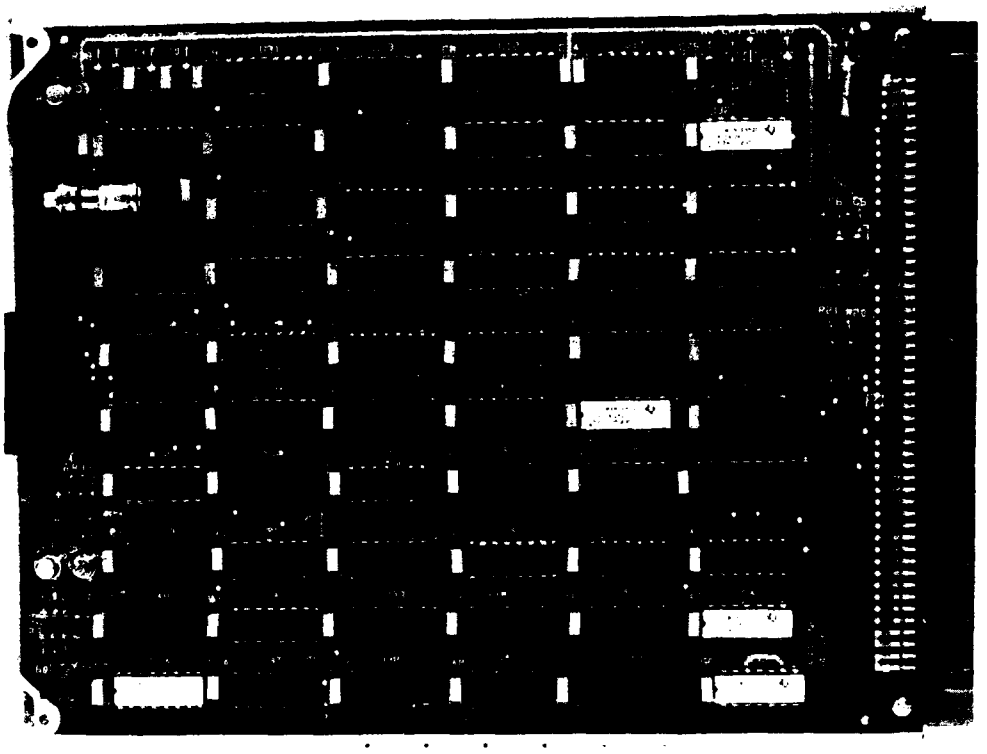


Figure 1. Demultiplexer Photograph

Appendix A is a schematic diagram of the demultiplexer card. All component designations, such as R3, C4, U11, will be referenced to this schematic. This CCA is probably the most complicated board inside the card cage. It contains the greatest number of active circuits (57) and has the least remaining space. Appendix B is the demultiplexer alignment procedure.

The demultiplexer CCA dissipates 1.5 watts. Table 1 below lists the demultiplexer CCA power requirements. Because of the close spacing of active components. the integrated circuits operate hot. During high temperature tests designed to simulate worst case operating conditions, the AN/TAC-1 was placed in an environmental chamber and the chamber temperature was raised to 73°C. After a few hours of operation, temperatures inside the AN/TAC-1 stabilized. An air temperature of 81°C was measured between the demultiplexer card and the adjacent card on its right. Active components on the card are rated to operate over the full military temperature range of -55°C to

125°C. This provides a margin of 44°C between the maximum expected CCA operating temperature and the upper device temperature limit and ensures good component reliability.

Table 1

Demultiplexer Power Requirements

Voltage	Current		Power
+ 5 V	0.238 A		1.19 W
+12 V	0.008 A		0.10 W
-12 V	0.017 A		0.20 W
		Total	1.49 W

Appendix C is the demultiplexer alignment procedure. Only one adjustment needs to be made: variable capacitor C2 needs to be trimmed to resonate the parallel-tuned circuit consisting of L1, C68, and C2 at 18432 kHz.

SECTION 2

FUNCTIONAL DESCRIPTION

2.1 INPUT DATA MODES

The demultiplexer CCA receives data to be demultiplexed, and a 6144 kHz clock synchronous with that data, from fiber optic subassembly 1A2. All input and output signals, as well as power and ground, connect to the demultiplexer board at the card edge connector.

The input data is named FODATARCV; the clock synchronous with it is named 6144CLK. The positive edges of the clock waveform are timed to occur in the middle of the data cell. The source of the input data, however, depends upon the AN/TAC-1 mode of operation: tropo satellite support radio (TSSR) or fiber optics (FO).

The mode of the input data is indicated by the state of the input named COAX3FOSEL. This input is connected to the optical power switch on the AN/TAC-1 control panel. This switch has three positions that select the mode of operation: H, L, and TSSR. The first two, H and L, are for the high and low power fiber optic modes of operation; the last, TSSR, stands for tropo satellite support radio. High and low power indicate the amount of optical power launched into the optical fiber by the transmitter. Low power is used for 0 to 3 kilometers of fiber optic cable, and high is used for 3 to 6 kilometers.

The wiper of the optical power switch is connected to the 5 V supply line, and the TSSR position throw is connected to the COAX3FOSEL line on the demultiplexer board. When the optical power switch is placed in the TSSR position, the COAX3FOSEL line is switched to 5 V. This logic 1 state enables the receiver on the demultiplexer board to receive data on the COAX3RCV input line. When the optical power switch is placed in either the L or H position, the COAX3FOSEL line is open-circuited. When COAX3FOSEL is open-circuited, a pull down resistor on the demultiplexer board will force it to a logic 0 and disable the receiver. When the receiver is disabled, its output will go to a logic 1 and stay there. This level output state is important because the absence of transitions is sensed by an activity detector on the fiber optic receiver board. This switches the fiber optic receiver data onto FODATARCV in place of TSSR data.

2.1.1 FO Mode

In the FO mode, light energy entering the fiber optic cable is routed to the fiber optic receiver module shown in figure 2. In the fiber optic receiver, light energy is first converted to electrical energy. This analog signal is then converted to digital data. A copy of the digital data is processed to derive a 6144 kHz clock. Because the clock is derived from the data itself, the clock and data signals are synchronous.

The recovered data and clock signals are then routed to fiber optic transmitter board 1A2A1. On this board the recovered clock retimes the data. This establishes a precise phase relationship between clock and data waveforms and also removes any residual noise and jitter from the data.

Data and clock signals are then routed to a line driver. The line driver provides a high level of drive to the transmission line connecting the fiber optic module and the demultiplexer card. This keeps the waveform rise and fall times short. The transmission lines are terminated in resistors on the demultiplexer board to prevent ringing. One resistor terminates the FODATARCV line, and another terminates the 6144CLK line.

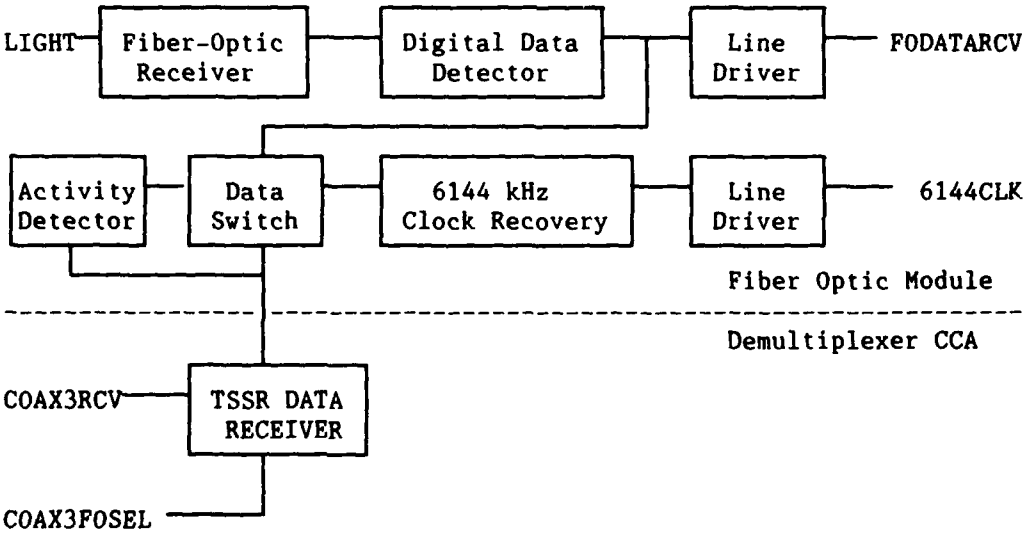


Figure 2. Input Data Flow

2.1.2 TSSR Mode

The TSSR mode is selected by a logic 1 on the COAX3FOSEL input. A logic 1 enables the TSSR data receiver to process data entering on the COAX3RCV input. The COAX3RCV input is wired directly to the COAX3 connector on the back panel of the AN/TAC-1. Digital data coming in on the CX-11230 dual-coaxial cable can be noisy and weak, or strong and relatively noise free. The situation depends upon the length of coaxial cable connected to COAX3. The TSSR data receiver detects noisy analog signals arriving at COAX3 and converts them to a 6144 kb/s digital data stream. This digital data is then passed over a transmission line to the fiber optic module as RDATAOUT.

On the receiver board, an activity detector circuit monitors the RDATAOUT line. When data transitions are present on this line, the activity detector disables data coming from the fiber optic receiver and substitutes the RDATAOUT stream in its place.

Then the TSSR data, RDATAOUT, is processed in an identical manner to that described for the fiber optic data in the fiber optic mode. The data and recovered clock are transmitted to the demultiplexer board for demultiplexing as FODATARCV and 6144CLK.

In summary, the fiber optic and TSSR modes of operation differ in the origin of 6144 kb/s data. In the fiber optic case, data comes in over the fiber optic cable to the FO connector in the form of light. In the TSSR case, data comes in on the coaxial cable to the COAX3 connector in the form of electrical energy. Fiber optic data is detected and converted to a digital data stream on fiber optic receiver board 1A2A2. TSSR data is detected and converted to a digital data stream on the demultiplexer board. To recover a 6144 kHz clock, the fiber optic receiver board processes either fiber optic or TSSR data. One is processed and transmitted to the demultiplexer board, depending upon the mode of operation. The data and clock always arrive at the demultiplexer for demultiplexing as FODATARCV and 6144CLK.

2.2 INPUT DATA STREAM COMPOSITION

The 6144 kb/s data stream is time division multiplexed. It consists of samples of other serial data streams that have been placed end to end like boxcars of a train. The samples come in two sizes: one or nine bits long.

2.2.1 Framing Pattern, Frame, and Subframe

A framing pattern is embedded in the serial stream to serve as a point of reference. It is eight bits long and consists of the string "10011111." This framing pattern is not received all at once; instead, only 1 bit out of 24 received is a framing bit.

The 24 successive bits will be referred to as a "subframe." Each subframe contains one framing bit. Figure 3 shows the composition of a single subframe.

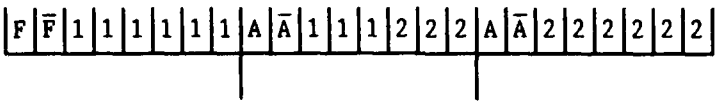


Figure 3. Demultiplexer Subframe Composition

The first bit on the left, labeled "F," is the framing bit. It is followed by its complement. Next come six bits of group 1 data. The first auxiliary channel data bit A and its complement *A come next followed by three bits of group 1 data and three bits of group 2 data. Another auxiliary data bit and its complement followed by six bits of group 2 data complete the subframe. The subframe is organized around three groups of eight bits because three eight-bit shift registers are used to demultiplex the subframe.

To see a complete framing pattern, one must look at 24 times 8, or 192 successive bits. The 192 successive bits will be referred to as a "frame." Each frame contains one framing pattern: "10011111."

The demultiplexer board hardware is organized around the subframe. Serial input data is processed 24 bits at a time as it is clocked into a 24-bit shift register. The first position in this shift register is intended for the framing bit. It is examined 6144 kHz divided by 24, or 256,000 times per second. If successive bits of the framing pattern 10011111 are present each time, the demultiplexer is said to be "in frame." When the demux is in frame, the 23 bit positions after the framing bit are determined as shown in table 2.

Notice that positions 2, 10, and 18 are reserved for the complement of existing bits. As complements, these bit positions contain no new data; they are wasted space and are not even demultiplexed. The reason, however, for using time slots this way is to facilitate recovery of the clock. Suppose that data in auxiliary group 1 and

Table 2. Determination of Bit Positions

Bit Position	Identification
1	Framing bit
2	Framing bit complement
3-8	Group 1 data bits (6)
9	Auxiliary data bit
10	Auxiliary data bit complement
11-13	Group 1 data bits (3)
14-16	Group 2 data bits (3)
17	Auxiliary data bit
18	Auxiliary data bit complement
19-24	Group 2 data bits (6)

group 2 channels was all at the logic 1 or logic 0 level. Then the composite bit stream would also be all 1s or 0s. If this were the case, the clock could not be recovered from the composite data stream because there would be no data transitions. Complements in the data stream, however, guarantee a data transition every eight bits. This is enough to recover the clock and maintain it independent of the state of the data inputs. That is why these three subframe positions are allocated to complements: to guarantee adequate transitions for clock recovery.

2.2.2 Group Data

Group 1 data is received and transmitted over a dual-coaxial cable terminated on the COAX1 connector. This connector is on the rear panel of the AN/TAC-1. Similarly, group 2 data comes from the COAX2 connector. The terms "group 1" and "COAX1," and "group 2" and "COAX2" are often used interchangeably.

Group 1 data occupies the time slots labeled "1" in figure 3; group 2 occupies the time slots labeled "2." There is a total of nine positions for group 1 and nine positions for group 2 data in each 24-bit subframe.

2.2.2.1 Group Data Content

Group 1 and 2 data are also composite. They usually consist of a stream of time division multiplexed digital telephone channels.

The AN/TAC-1, however, operates transparently. It treats the groups as simple serial data streams. It multiplexes them with other channels for long range transmission and demultiplexes them at the other end without caring about the contents. End devices using the group data never know that the AN/TAC-1 is in between. Although the AN/TAC-1 carries the data, it does not affect it.

2.2.2.2 Group Data Rates

Group 1 and 2 data may enter COAX1 and COAX2 connectors at many different data rates. Every rate is a multiple of 128 or 144 times 2 to the Nth power. The rates are shown in table 3.

Table 3. Group Data Rates

N	128×2^N (kb/s)	144×2^N (kb/s)
0	128	144
1	256	288
2	512	576
3	1024	1152
*	1536	
4	2048	2304
5**	4096	4608

*Note that the 1536 kb/s rate is not an integer N-multiple of 128. Instead, it is 12 X 128, halfway between 8 X 128 X 2^3 and 16 X 128 X 2^4. The value of N is approximately 3.588.

**Group 1 only.

Digital divider chains are used on the demultiplexer board to generate group clocks for all group rates. Two thumbwheel switches are located on the left front side of the AN/TAC-1 control panel. The switch on the left programs the AN/TAC-1 for group 1 rates, and

the one on the right programs the AN/TAC-1 for group 2 rates. Both switches output hexadecimal codes to the demultiplexer, multiplexer, and traffic cards. These codes configure chips on the cards to process traffic at the selected rate. On the demultiplexer card, the codes cause data selector chips to choose the proper group clock for the demultiplexer circuits.

2.2.3 Auxiliary Data

Auxiliary (AUX) data consists of 16 channels capable of carrying digital data at rates up to 32 kb/s: 4 channels are permanently dedicated to orderwire traffic, 2 are dedicated to telephone (TEL1, TEL2) but may be reconfigured for general use, and 10 are available for general use. General purpose channels are terminated on pins of the AUX connector, which is on the AN/TAC-1 back panel. A 32 kHz clock, 32KHZMUX, for clocking data into the auxiliary channels is available on the connector; 32KHZDMUX is available for clocking data out.

The 16 auxiliary channels are split into 2 groups of 8. One bit from each group of eight is present in each subframe. Therefore, each time a subframe is demultiplexed, one bit is generated for each group of auxiliary data channels. If 256,000 subframes per second are divided by 8 channels, the result is 32 kb/s per channel.

2.3 MASTER CLOCK GENERATION

The demultiplexer board also generates a master clock to synchronize the generation of group clocks, data clocks, and timing strobes. These required waveforms are derived from the same master, and are synchronized. The choice of master clock frequency is very important. First, it has to be higher than all of the frequencies needed so they can be generated by dividing it down. Second, divider chains require that generated frequencies be integer multiples of the master clock. The master clock frequency chosen was 18432 kHz. This is 3 times the incoming data rate of 6144 kb/s, 4 times the highest 144×2^N group rate of 4608 kb/s, and 4.5 times the highest 128×2^N group rate of 4096 kb/s. Notice that 4.5 is not an integer and violates the second principle. To eliminate this problem, we would have to double 18432 to get 36864 kHz. This would be 8 times 4608 and 9 times 4096. However, the 36864 kHz rate is in the very high frequency (VHF) radio range! This could cause unwanted radiation as well as undesirable radio frequency coupling to adjacent circuits. Additionally, the higher clock frequency would increase power dissipation in digital divider circuits, because the internal

dissipation of the transistor-transistor logic (TTL) used is proportional to the clock rate. The higher the clock rate, the more internal power is dissipated. Engineering trade-offs dictate that 18432 kHz be chosen.

This left the problem of how to obtain the 4096 kHz rate. There was no such thing as a divide-by-4.5 chip. The solution was to divide by 9 to get 2048 kHz, and then use a phase lock loop to multiply by 2 to get 4096 kHz. Most of the circuitry on the demultiplexer board is used to divide down the 18432 master clock to get group clocks, data clocks, and strobes that are needed to demultiplex incoming 6144 kb/s data.

An additional requirement is that the 18432 kHz clock be synchronized with the incoming data. To satisfy this requirement, the 18432 kHz master clock is derived directly from the incoming 6144CLK, which is synchronous to the data. A parallel-tuned circuit, tuned to 18432 kHz, filters out square wave 6144CLK. The resultant waveform is converted to a TTL-compatible 18432 kHz clock by a high speed comparator and then buffered and distributed for timing.

2.4 OUTPUT DATA

The demultiplexer output data consists of group 1 data and clock, group 2 data and clock, and auxiliary data and clock. Group data and clock may be at any of the rates listed in paragraph 2.2.2.2; each group may be different from the other. Group 1 data is labeled GR1DATAA, and group 1 clock, GR1CLKA. Group 2 data is GR2DATAA, and group 2 clock, GR2CLKA. Auxiliary clock 32KHZDMUX is always 32 kHz. The auxiliary data rate may be any rate up to a maximum of 32 kb/s. There is a total of 16 auxiliary channels that are organized in 2 banks of 8 channels each.

2.5 SINGLE GROUP OPERATION

The demultiplexer may be configured to carry a single group instead of two groups. This becomes automatic when either the 4096 or 4608 rate is chosen for group 1. When either of these rates is selected, logic circuits on the demultiplexer card connect group 1 and 2 demultiplex registers in series to handle the doubled data rate of group 1. Group 2 data no longer exists in this mode of operation because the group time slots in the composite data stream are all dedicated to group 1 data. The data is output on GR1DATAA. Although GR2DATAA outputs an identical copy delayed in time, it is not used.

2.6 INDICATOR OUTPUT

The demultiplexer card has a single indicator output, FRAMESYNC. This output is connected to the output of a logic gate on the demultiplexer board. The gate sinks the current for a light emitting diode mounted on the AN/TAC-1 control panel. That indicator is designated "Group 3 Receive." When the gate output is at logic 0, the indicator current is being carried to circuit ground and the light is on. This indicates that the demultiplexer card has achieved frame synchronization and the demultiplexed data is good.

SECTION 3

THEORY OF OPERATION

Section 3 discusses the theory of operation of the demultiplexer board. The discussion is based on the circuit schematic shown in appendix A. This schematic is Air Force drawing 84-53864. For discussion, the schematic has been divided into functional sections. Each section accomplishes a specific task in the process of demultiplexing the serial data stream.

3.1 TSSR DATA CONDITIONING

Composite data at 6144 kb/s arrives at the demultiplexer board for demultiplexing from one of two sources; reference paragraph 2.2. Composite serial data from the TSSR arrives on CX-11230 dual-coaxial cable. The coaxial cable is connected to the COAX3 connector on the rear panel of the AN/TAC-1. The output pin of this connector is wired to the COAX3RCV input to the demultiplexer board, edge card connector pin (ECCP) 46, 96. Data arriving on the coax cable is corrupted by noise and attenuated in amplitude. It must be converted to TTL compatible data.

A number of discrete components are used to condition the input data. The 56 ohm resistor R3 terminates the COAX3RCV line to prevent ringing and reflections. C1 provides alternating current (ac) coupling of the serial input data and removes any direct current (dc) component that could interfere with conversion to TTL data by U11. CR1 and CR2 protect U11 from high voltage transients by conducting to ground when the input voltage exceeds approximately 600 mV. The 1 kilohm resistor R4 biases the input of U11 at 0 V.

U11 is the National Semiconductor LM161 high speed differential voltage comparator. One of the differential inputs, pin 4, is grounded so the comparator is used in the single-ended mode rather than the differential. The inverted output, pin 9, has been selected for use; the noninverting output, pin 11, is not used. Strobe lines for both output stages, pins 8 and 13, are connected to COAX3FOSEL, ECCP 45, 95. COAX3FOSEL enables U11 when at a logic 1 and disables it when at a logic 0. The position of the optical power switch on the control panel determines the logic state of COAX3FOSEL. When it is in either the L (low power fiber optics) or H (high power fiber optics) position, COAX3FOSEL is at logic 0; when it is in the TSSR position, COAX3FOSEL is at logic 1. Therefore, U11 works only when the optical power switch is in the TSSR position; in the L or H position it is disabled.

The inverted output data from U11 is inverted again by U32-1, -2, -3, which serves as a line driver for the output signal RDATAOUT, ECCP 44, 94. RDATAOUT is true data. It is transmitted to the fiber optic module 1A2 for clock recovery and resynchronization.

3.2 INPUT DATA SYNCHRONIZATION

FODATARCV must be synchronized with the local 6144 kHz clock on the demultiplexer board. This synchronization is accomplished by U27, a 54LS74, dual D-type, positive-edge-triggered flip-flop. FODATARCV data is presented at the D input, pin 2. The positive edges of the local 6144 kHz clock on pin 3 sample the data and output a copy synchronized to the local clock on the Q output, pin 5. The second half of U27 delays the synchronized data stream by a single bit period and inverts it by using the *Q output. The output data on U27, pin 8, is then sent to fiber optic data registers U37, U38, and U41 for demultiplexing.

Test points are available to monitor the synchronization process. Test points J1-9 and J1-3 are the data and clock inputs, respectively. Test point J1-5 is the resynchronized data output.

3.3 DOUBLE GROUP DATA DEMULTIPLEXING

Two data groups, as well as auxiliary data channels, are demultiplexed by loading a 24-bit serial-in, parallel-out shift register with incoming composite data. Serial input data is loaded by presenting the composite data stream to the input of the 24-bit shift register and clocking the register string with a 6144 kHz clock that is synchronous to the data. When the 24-bit register is full, the 9 bits of group 1 data are parallel loaded into a separate 9-bit parallel-in, serial-out shift register. At the same time, the nine bits of group 2 data are parallel loaded into a second nine-bit shift register. This parallel loading of data in the 24-bit serial shift register across to the two nine-bit serial shift registers occurs in a small fraction of a 6144 kHz clock period. Therefore, the contents of the 24-bit register are not disturbed, and the process of clocking in the data bits of the composite input stream continues unabated. The nine-bit group registers are continuously clocked by their respective group clocks. This causes the group data that was parallel loaded to be serially shifted out at the proper group rate. This empties the nine-bit group registers just in time to prevent the data from being overwritten by the next nine bits.

The 24-bit serial register is sometimes referred to as the fiber optic register. It consists of U37, U38, and U41 connected output to input. Each of these is a 54LS164, eight-bit, serial-input, parallel-output shift register. The clock inputs, pin 8, are tied in parallel and driven by a 6144 kHz clock synchronous to the input data. The serial composite stream is connected to pins 1 and 2 of U37, the first register in the chain. The output of U37, pin 13, is connected to input pins 1 and 2 of U38, the second register in the chain. The output of U38, pin 13, is connected to input pins 1 and 2 of the last register in the chain, U41. Parallel data output pins carrying group 1 data are U37-5, -6, -10, -11, -12, -13, and U38-5, -6, -10. Parallel data output pins carrying group 2 data are U38-11, -12, -13, and U41-5, -6, -10, -11, -12, -13.

Group 1 data output pins are connected to the parallel-input pins of shift registers U40 and U39, which are sometimes referred to as group 1 demultiplex registers. U40 and U39 are connected in series to form a nine-bit register. U40 is a 54LS166 eight-bit shift register, and U39 is a 54LS194 four-bit bidirectional universal shift register. Both are being used in a parallel-in, serial-out mode of operation. U40 and U39 are clocked by GR1CLKA, ECCP 21, after it has been inverted by U50-11, -10. GR1CLKA is a square wave synchronous with group 1 data, and its frequency in hertz is equivalent to the data rate in bits per second. Therefore, group 1 data is continuously being clocked out of the nine-bit serial shift register formed by U40 and U39 at pin U39-13.

Data is actually demultiplexed by a load pulse that occurs at the rate of 256,000 times per second. The load pulse causes the parallel output data from the fiber optic register to be parallel-loaded into the nine-bit demultiplex register. The actual transfer is made when the positive edge of the clock occurs simultaneously with the load pulse. The load pulse is a positive going pulse at U39-10; however, U40 requires a negative going pulse at U40-15 so inverter U50-5, -6 is used to drive it. The pulse width of the load pulse is a fraction of that of the 6144CLK period, which in turn is shorter than the group 1 clock period. Therefore, parallel loading of the data from the fiber optic register to the demultiplex register does not disturb serial clocking of the data in either. Timing of the load pulse causes new data to be loaded into the demultiplex register at the end of the last data bit. This prevents any data bits in the demultiplex register from being overwritten.

Operation of the group 2 demultiplex register is identical to that described for group 1. Demultiplexing of group 1 and group 2 data occurs simultaneously because the single 24-bit fiber optic data register feeds 2 separate 9-bit demultiplex registers. Group 2 data

output pins are connected to the parallel-input pins of shift registers U35 and U42, which are sometimes referred to as group 2 demultiplex registers. U35 and U42 are connected in series to form a nine-bit register. U35 is a 54LS194 four-bit bidirectional universal shift register, and U42 is a 54LS166 eight-bit shift register. Both are used in the parallel-in, serial-out mode.

Both U35 and U42 are clocked by GR2CLKA, ECCP 19, 69, after it has been inverted by U57-4, -6. GR2CLKA is a square wave synchronous with group 2 data, and its frequency in hertz is equivalent to the data rate in bits per second. Therefore, group 2 data is continuously being clocked out of the nine-bit serial shift register formed by U35 and U42 at pin U42-13.

Data is actually demultiplexed by a load pulse that occurs 256,000 times per second. The load pulse causes the parallel output data from the fiber optic register to be parallel-loaded into the nine-bit demultiplex register. The actual transfer is made when the positive edge of the clock occurs simultaneously with the load pulse. The load pulse is a positive going pulse at U35-10. However, U42 requires a negative going pulse at U42-15 so inverter U50-5, -6 drives that. The pulse width of the load pulse is a fraction of that of the 6144CLK period, which in turn is shorter than the group 2 clock period. Therefore, parallel loading of the data from the fiber optic register to the demultiplex register does not disturb the serial clocking of the data in either. Timing of the load pulse causes the new data to be loaded into the demultiplex register at the end of the last data bit. This prevents any data bits in the demultiplex register from being overwritten.

Demultiplex registers have been sized to handle nine bits of data. Sometimes, however, only eight of the nine bits are used. This occurs when the group data rate has been chosen from the 128 X 2^N family of rates. The multiplex scheme chosen for the AN/TAC-1 causes this to happen. For example, the 2048 kb/s rate is from this family, but the 2304 kb/s rate is not. The fiber optic register is constantly shifting in composite data at 6144 kb/s. Since this register is 24 bits long, the time needed to shift in 24 bits is T = 24 X (1/6,144,000). The term in parentheses is the period for a single bit. A single load pulse will transfer group 1 and group 2 data to their respective demultiplex register in a fraction of the time in parentheses. Immediately after the transfer, group clocks will shift this data out at the group rate until T expires and another nine bits are loaded. Mathematics will show that if the group rate is 2048 kb/s, only eight bits will be shifted out before T expires (T s X 2,048,000 b/s = 8 bits) and another nine bits are loaded. However, if the group rate is the faster 2304 kb/s, this is enough time to shift out nine bits (T s X 2,304,000 b/s = 9 bits) in

the same time. What happens to the ninth bit loaded when only eight are shifted out? Nothing. It is a "don't care" bit that is overwritten when the next nine are loaded. It never makes it out of the demultiplex register into the group data stream.

Inverters U29-11, -10, U29-13, -12, U29-9, -8, U51-5, -6, and U51-3, -4 have been placed in series with every other data bit between the fiber optic register and the group 1 demultiplex register. Inverters U51-1, -2, U51-11, -10, U51-9, -8, and U51-13, -12 are in series between group 2 demultiplex registers. This provides true data output from the demultiplex registers because these same data bits were inverted during multiplexing. Every other fiber optic data register bit was inverted during multiplexing to provide transitions in the 6144 kb/s data stream when the group data were all ones or zeros.

3.4 SINGLE GROUP DATA DEMULTIPLEXING

The AN/TAC-1 will operate at group rates of 4096 or 4608 kb/s. However, when either of these rates is selected, only group 1 may be used. The 4096 rate is selected by setting the leftmost thumbwheel switch on the main control panel to "14," or the 4608 rate is selected by setting the switch to "15." Coaxial cable carrying traffic at either of these rates must be connected to the COAX1 connector on the rear panel of the AN/TAC-1; the COAX2 connector cannot be used.

Selecting either 14 or 15 on the group 1 thumbwheel switch means the MSEL1 output lines assume the logic state "0001" or "0000," respectively. Since these codes are read in "DCBA" order, MSEL1D, MSEL1C, and MSEL1B will always be at logic 0. MSEL1D (ECCP 32, 82), MSEL1C (ECCP 33, 83), and MSEL1B (ECCP 36, 86) are connected to pins 3, 5, and 4 of U17, respectively. U17 is a 54LS27 three-input NOR gate. By DeMorgan's law, a NOR gate is equivalent to a negative input AND gate. Therefore, output pin U17-6 will assume a logic 1 state if and only if U17's inputs are all logic 0s. This occurs only when 14 or 15 is selected on the group 1 thumbwheel switch.

When U17-6 is logic 1, U57-1, -12, -3 are also logic 1, and inverter U52-13, -12 places U57-5, -9, -10 at logic 0. The logic 1 on U17-1 and logic 0 on U52-12 cause the reconfiguration of group 1 and 2 demultiplex registers. The 9-bit group 1 demultiplex register and the 9-bit group 2 demultiplex register are connected in series to form a single 18-bit demultiplex register. The new 18-bit register consists of U40, U35, and U42 connected output to input.

Since the group 2 demultiplex register is normally clocked by GR2CLKA, this signal must be replaced by the same signal clocking the nine-bit group 1 demultiplex register, GR1CLKA. Both nine-bit halves must be clocked together. The logic 1 on U57-3 accomplishes this by selecting the GR1CLKA input at U57-2 to appear at U57-6. The logic 0 at U57-5 deselects the GR2CLKA input on pin U57-4 and keeps it from appearing at U57-6. The output of the new 18-bit register will be GR1DATAA. Since the output on U42-13 is now GR2DATAA, this signal must be connected to the GR1DATAA output. This is accomplished by the logic 1 at U57-1, -12, and the logic 0 on U57-9, -10. The logic 1 on U57-1, -12 selects the GR2DATAA input at U57-13 to appear at U57-8, while the logic 0 at U57-9, -10 deselects the GR1DATAA input at U57-11 and prevents it from appearing at U57-8.

3.5 FRAMING PATTERN DEMULTIPLEXING

Framing pattern "10011111" is demultiplexed by a 54LS164, eight-bit, serial-in, parallel-out, shift register U47. The shift register samples the data on pin U37-3, the first bit of the fiber optic register. The sample rate is 256,000 times per second, which provides a single sample every time the fiber optic register accumulates 24 bits. Each sample is shifted into the register on pins U47-1, -2 by the 256 kHz clock on pin U47-8.

3.6 FRAMING PATTERN DETECTION

Logic gates of the framing pattern detector constantly look at eight bits in the framing pattern demultiplex register U47 and compare them to a valid framing pattern. These gates are U49-13, -12, -10, -9, -8, U49-1, -2, -4, -5, -6, and U33-12, -11, -13. Together they act as an eight-input AND gate. When the eight bits that constitute a valid framing pattern exist at inputs U49-13, -12, -10, -9 and U49-1, -2, -4, -5, the detector output U33-13 will go to a logic 1. At all other times, U33-13 is a logic 0. U52-5, -6 and U52-9, -8 invert the two logic 0 bits in framing pattern "10011111." This changes it to "11111111," which can be detected by an eight-input AND gate.

The "in frame" indication is a 32 kHz square wave at the output of the framing pattern detector, U33-13. This square wave exhibits a 1:7 duty cycle: one logic 1 followed by seven logic 0s. This is caused by the framing pattern logic looking at every bit of the eight and finding one match and seven no matches. This single logic 1 will occur at the rate of 256 kHz divided by 8, or 32 kHz.

3.7 AUXILIARY DATA DEMULTIPLEXING

Auxiliary data is handled in a manner similar to the framing pattern; however, there are two eight-bit serial-to-parallel conversions rather than one. Each group of eight bits is demultiplexed by a 54LS164, eight-bit, serial-in, parallel-out shift register and a 54LS374 eight-bit latch. Shift register U46 and latch U45 demultiplex auxiliary channels 1 through 8. Shift register U43 and latch U44 demultiplex channels 9 through 16. Shift registers U46 and U43 sample the data on pins U38-3 and U41-3, respectively, of the fiber optic register.

The sample rate of 256,000 times per second provides a sample each time the fiber optic register accumulates 24 bits. Each sample is shifted into the serial register on pins 1 and 2 by the 256 kHz clock on pin 8.

Once eight bits have been shifted in, the positive edge of the 32 kHz clock present on pin 11 of U45 and U44 causes a parallel transfer of data from the serial shift registers into the eight-bit latches. The eight-bit latches will then hold the data until another eight bits have been shifted into the serial shift register and another positive edge of the 32 kHz clock occurs to transfer them. Therefore, the outputs of the eight-bit latches can change at a 32 kHz clock rate. This is equivalent to a maximum auxiliary data rate of 32 kb/s.

3.8 AUXILIARY DATA ALLOCATION AND BUFFERING

Auxiliary channel 1 through 10 data is transmitted from the demultiplexer board to the AUX I/O connector, J1. This connector is on the rear connector panel, subassembly A4, of the AN/TAC-1. Each channel is terminated on a single J1 connector pin.

Auxiliary channel 11 and 12 data is also transmitted from the demultiplexer board to the AUX I/O connector. Channels 11 and 12 are enabled by grounding CH11CONT, pin A4J1-b, and CH12CONT, pin A4J1-c, on the AUX I/O connector. These pins are connected to ECCP 30, 80 and ECCP 29, 79 on the demultiplexer board. Normally, CH11CONT and CH12CONT are left open-circuited. This disables channels 11 and 12, forces their output pins to a logic 0 state, and reroutes the demultiplexed data over an alternative path.

Discrete logic on the demultiplexer card switches channel 11 and 12 demultiplexed output to signal paths named TEL1XMT and TEL2XMT, respectively. These paths carry data to the circuit card assembly in

the last active position of the card cage, slot 7. Slot 7 will contain either one CVSD card or one loop modem card to process two channels of data. When CVSD or loop modem cards are used, auxiliary channels 11 and 12 are unavailable for use, and vice versa.

Auxiliary channel 13 through 16 data is dedicated to orderwire traffic and permanently connected to the two signal conditioner oederwire cards. Channel 14, GR1MOWA, and channel 16, GR1DOWA, ECCP 22, 72 and ECCP 24, 74, respectively, are connected to the signal conditioner orderwire card for group 1 in slot 5. Channel 13, GR2MOWA, and channel 15, GR2DOWA, ECCP 20, 70 and ECCP 23, 73, respectively, are connected to the signal conditioner orderwire card for group 2 in slot 6.

The 32 kb/s data outputs from U45, auxiliary channels 1 through 8, are buffered by 54128, 70-ohm, line drivers. These are U54-5, -6, -4, U54-9, -8, -10, U55-5, -6, -4, U55-2, -3, -1, U55-9, -8, -10, U55-12, -11, -13, U54-12, -11, -13, and U54-2, -3, -1. Notice that these line drivers are inverting. Therefore, to provide a true data output, inverter U50-1, -2 is used to invert the data before demultiplexing, and then subsequent line driver inversions make the data true just before it is output.

The 32 kb/s data output in parallel from U44 is handled differently. Only two of the eight channels are buffered by 54128 line drivers. These are channels 9 and 10. Inverter U52-3, -4 and driver U33-5, -6, -4 buffer channel 9, and inverter U52-1, -2 and driver U33-2, -3, -1 buffer channel 10. Since both gates are inverting, the data output is true.

Auxiliary channels 11 and 12 are normally dedicated to telephone communications between AN/TAC-1s. ECCP 30, 80, CH11CONT, and ECCP 29, 79, CH12CONT, are connected to auxiliary input/output (I/O) connector pins A4J1-b and A4J1-c, respectively. However, these pins are normally left open-circuited. Open-circuiting both pins selects TEL1 and TEL2 options, rather than CH11 and CH12 options. R21 pulls up U8-11 and U26-13 to a logic 1. Similarly, R20 pulls up U8-13 and U26-9 to a logic 1. Therefore, U44-6, the demultiplexed channel 11 output, is routed through the enabled AND gate U26-12, -13, -11 to the TEL1XMT output, ECCP 26, 76. The logic 0 at U53-9 disables NAND gate U53-10, -9, -8 and keeps its output pin at logic 1. The constant logic 1 on U32-8 forces U32-10 and CH11XMT, ECCP 43, 93, to a constant logic 0. Similarly, U44-9, the demultiplexed channel 12 output, is routed through the enabled AND gate U26-10, -9, -8 to the TEL2XMT output, ECCP 27, 77. The logic 0 at U53-13 disables NAND gate U53-12, -13, -11 and keeps its output pin at logic 1. The constant logic 1 on U32-5 forces U32-4 and CH12XMT, ECCP 42, 92, to a constant logic 0.

Auxiliary channels 13 through 16 are dedicated to support signal conditioner orderwire cards and are not connected to the outside world. Therefore, they are not buffered.

3.9 MASTER CLOCK GENERATION

The master clock frequency is 18432 kHz. It is derived from the 6144CLK signal, ECCP 5, 55. 6144CLK is a TTL-compatible square wave that contains the 6144 kHz fundamental frequency and all of the odd harmonics. The first odd harmonic is 18432 kHz, the desired frequency. It is selected by filtering the 6144 kHz square wave with a parallel resonant circuit composed of L1, C68, and C2; C2 is variable and is used to tune the parallel circuit to precisely 18432 kHz. Capacitors C3 and C69 lightly couple signals into and out of the resonant circuit. This keeps the effective Q of the resonant circuit high for greater selectivity.

The emitter-follower buffer formed by R37, R38, R39, and Q3 provides drive-to-load resistor R35 and test point J1-11. The output signal at J1-11 should, theoretically, be a sine wave at 18432 kHz. However, the physical implementation of the circuit exhibits undesirable coupling of harmonics higher than 18432 kHz around the filter. These combine with the desired output to alter and distort it. The result is a sequence of short pulses instead of a sine wave. Additional filtering would improve the quality of the waveform, but the existing quality has proven to be adequate. C70 removes any dc component in the output and makes the output signal symmetrical about circuit ground.

U30 is a high speed comparator that converts the analog 18432 kHz signal to a TTL compatible square wave. The resultant square wave is not symmetrical; however, this does not matter because only positive edges of the waveform affect the gates that follow. What is important is that the positive edges of the output waveform be evenly spaced in time. This requirement is met by the circuit.

The 18432 kHz output U30-11 is routed to J2-1, -2 on the circuit board. This jack is normally jumpered; however, if the jumper is removed, U30 is disconnected and an external 18432 kHz may be connected for test purposes. This jack was installed to facilitate testing and troubleshooting assisted by automatic test equipment (ATE).

The 18432 kHz output of U30 is buffered by inverter U10-5, -6, a 54LS04, and U29-5, -6, a 54S04. These two gates form a noninverting buffer and drive all of the gates in the master timing chain. U29-6 drives a circuit board trace that is connected to many counters. The length of this trace should be minimized by locating the counters as

close together as possible. This will keep the rise and fall times of the master clock waveform short for good performance.

3.10 TIMING CHAIN SYNCHRONIZATION

The serial input data at 6144 kb/s, FODATARCV, is synchronous with the incoming clock, 6144CLK. Since the 18432 kHz master clock is derived from 6144CLK, it is phase locked to both 6144CLK and FODATARCV. The first counter in the master timing chain, U23, divides the 18432 master clock by 3 to generate slave 6144 kHz clocks, which are used on the demultiplexer board. These are not phase locked to the FODATARCV, 6144CLK, and the master clock because the internal state of U23 after power-on is different each time. In fact, U23 may assume any one of three different states at power-on. Since the clocking of the counter by the 18432 master clock can occur from any one of these three states, the phase of the 6144 kHz output clock with respect to the master clock will change after every turn-on. This can cause problems with the 6144 kHz clock output from U23-13, for example, which is indirectly used to sample the incoming FODATARCV data on pin U27-2. Phase variations with the 18432 kHz master clock and FODATARCV, which is phase synchronous to it, could result in the data being sampled at the time it changes from one logic state to another. This would cause data errors. To prevent this, the local 6144 kHz clocks must also be phase locked to the 18432 master clock, 6144CLK, and FODATARCV. This means that the first counter in the timing chain must be synchronized. When the first counter is synchronized, the counters that follow it will also be synchronized.

U48-1, -2, -3 synchronizes U23. It is a 54LS112, negative edge-triggered flip-flop. Pin 1 of the flip-flop is being clocked by the 18432 kHz master clock, and so is pin 2 of divide-by-three counter U23. The master clock is a positive pulse, with a duty cycle of less than 50 percent, which occurs at a frequency of 18432 kHz. The flip-flop clocks on the negative edge of the master clock, and the counter clocks on the positive edge.

Pin 3 of the flip-flop, the J input, is connected to 6144CLK, ECCP 5, 55. This is a 50 percent duty cycle clock at a frequency of 6144 kHz. The flip-flop synchronizes the counter by forcing it to the "1101" state. This occurs whenever the negative edge of the 18432 kHz clock coincides with the logic 1 state of the 6144 kHz clock, and the Q output is reset. Each time these conditions are met, the Q output of the flip-flop is set. Since the Q output is connected to the K input, the next 18432 clock edge will find either the J input still high or the J input low and the K input high, depending upon the phase relationship between the 6144 and 18432 kHz

clocks. Whichever, the result is the same: the flip-flop Q output is reset. This immediately forces the K input low.

The third flip-flop clock pulse will find both flip-flop inputs low, and this will cause the output of the flip-flop to remain in its previous state: reset. The J input will be low because it is impossible for the 50 percent duty cycle 6144 kHz clock to remain high for three successive edges of the 18432 kHz clock, and the K input is low because the Q output to which it is connected is reset by the second clock.

The flip-flop implements a finite state machine with three states. The machine sequences from state 3 into state 1 on a JK/Q (inputs/output) combination of 10/1, from state 1 to state 2 on 11/0 or 01/0, and from state 2 to state 3 on 00/0. The negative edge of the 18432 kHz clock produces the actual change in state, but the inputs and present state uniquely determine what the next state will be.

The *Q output of flip-flop U48-6 is connected to the *LOAD pin of divide-by-three counter U23-9. The *Q output of the flip-flop provides the output sequence "011011011 . . ." to the load pin of the counter. The "0" causes the counter to load "1101," and the "11" allows it to count up "1110" and "1111" before the next "0" causes it to again load "1101." Therefore, the flip-flop forces the counter to synchronize its "1101" count with the "0" output from the *Q output of the flip-flop. Since both count modulo 3, the counter outputs are phased locked to the 18432 kHz master clock and 6144CLK signal.

3.11 MASTER TIMING CHAIN

The master timing chain is composed of counters U23, U22, U21, U31, and U12. Each of these is a synchronous, four-bit, binary counter. U23 is a 93S16M (direct replacement for 54S161); U22, U21, U31, and U12 are 54LS161s.

U23 is configured as a divide-by-3 stage. It divides the 18432 master clock by 3 to generate a 6144 kHz, look-ahead carry output on U23-15. The carry output becomes the input enable for the next stage U22, which normally divides by 8 to generate a 768 kHz carry on U22-15. This carry becomes the input enable for U21, which divides by 3 and produces a 256 kHz carry on U21-15. This carry becomes the input enable for U31, which divides by 8 and produces a 32 kHz carry on U31-15. This carry becomes the input enable for U12, which divides by 4 to produce an 8 kHz carry on U12-15. All counters are clocked by the 18432 kHz master clock; all state changes occur on a positive edge of this clock. Carries out enable succeeding counters to change state. The lack of a carry out from the preceding stage will cause a

counter to be frozen in its present state. Therefore, a counter cannot react to the master clock unless it is enabled by the carry out of the preceding stage.

All counters are configured as divide-by-n stages by parallel loading their data inputs, pins 6, 5, 4, and 3, with a number. For example, a divide-by-3 stage is preloaded with 13. Because these are binary counters, the number must be input in binary form. In binary, the decimal number 13 is "1101," which is in the standard form "DCBA." D is the most significant bit, and A is the least significant bit. D, C, B, and A are input on pins 6, 5, 4, and 3, respectively. This starting count is transferred to the counter when the load input, pin 9, is at logic 0, and a positive edge of the clock occurs on pin 2. Succeeding positive edges of the clock will cause the counter to count up from the number loaded. When count 15 is reached, the ripple carry output (RCO), pin 15, will go to a logic 1 state and stay there for the duration of this count. Therefore, a single logic 1 pulse will be output on the RCO pin for every n positive edge on the clock input pin.

U22 is different from the other counters because its start count is variable: it depends upon the output of NAND gate U26-4, -5, -6. If the output is logic 0, then "1000" is loaded; if the output is logic 1, then "0111" is loaded. This occurs because the output is passed to the "CBA" inputs of the counter unchanged, but it is inverted by U15-11, -10 before it is passed to the "D" input. The counter divides by 8 when "1000" is loaded (1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111) and divides by 9 when "0111" is loaded (0111, 1000, . . .). This difference is used to synchronize frames and will be discussed in detail in paragraph 3.17.

NAND gates, such as U19-1, -2, -3, are used to NAND the RCO of U22 with the 6144 kHz RCO from U23, and generate the logic 0 input pulse that will reload the counter with n at the next positive edge of the clock. Therefore, in the previous example the counter is forced to count 13, 14, 15, 13, 14, 15 over and over again. This produces a positive RCO pulse at the rate of the clock input divided by n. The RCO pulse has a width equal to the period of the clock input. Since the 18432 kHz master clock is clocking the counters, the RCO pulse width is approximately 54.25 nanoseconds.

Counters U22, U21, U31, and U12 are all constrained by NAND gates to reload during the conjunction of their respective RCO outputs and the RCO of U23. Since the RCO of U23 occurs at the 6144 kHz clock rate, the rest of the counters are forced to change on the positive 18432 kHz clock edge, which occurs during the 6144 kHz RCO. This synchronizes all of the counter starting states with the on-board 6144 kHz clock.

3.12 GROUP TIMING, 4096 kHz

As previously mentioned, group 1 and 2 data rates at the COAX1 and COAX2 connectors are multiples of either 128 or 144 times 2 to the Nth power. The 128 X 2^N family rates are 128, 256, 512, 1024, 2048, and 4096 kb/s. The demultiplexer board first generates the 4096 kHz clock and then derives the rest of the clock rates by repeatedly dividing by 2.

Generating a 4096 kHz clock is a difficult task. A master clock frequency of 18432 kHz requires division by 4.5 to obtain 4096, but the divisor must be a whole number. Therefore, the method adopted was to first divide by 9, and then multiply by 2. This technique works, but it requires quite a bit of circuitry. The additional requirement that the 4096 kHz clock have a 50 percent duty cycle increased the attractiveness of this approach, however, because the final multiplication by 2 achieves it automatically.

The 18432 kHz master clock is divided by 9 in U9. The count "0111" is loaded on the positive edge of the master clock when U56-8 is logic 0. U56-10, -9, -8 and U10-13, -12 synchronize U-9's output with those of the master timing chain. Once U9 has been loaded with the initial count "0111," it increments with each positive edge of the master clock on U9-2: 0111, 1000, 1001, 1010, 1011, 1100, 1101, 1110, 1111, 0111, 1000, 1001 . . . . At the beginning of count "1111," the ripple carry output, U9-15, rises to a logic 1. U10-13, -12 inverts it and provides a logic 0 at U56-9. This logic 0 forces the output U56-8 to logic 0. Since U56-8 is connected to counter load input U9-9, a logic 0 on this pin will cause the initial count "0111" to be reloaded on the next positive edge of the master clock. Therefore, the counter divides the master clock by 9. The output on U9-11 is 18432 kHz divided by 9, or 2048 kHz.

Notice that the AND gate is really being used as a negative logic OR gate. A logic 0 at U56-10 or U56-9 or both will result in a logic 0 at U56-8 and U9-9. This will cause the counter to be reloaded on the next positive edge of the master clock. Therefore, the counter can be reloaded by either the occurrence of the terminal count or through the arrival of a negative synchronizing pulse from the master timing chain at U56-10. When the board is first powered up, the initial synchronizing pulse arriving on U56-10 will force U9 to synchronize to the master timing chain. Once this has been accomplished, the negative pulses on U56-10 and U56-9 should overlap.

The 2048 kHz output from U9-11 is routed to inverter U10-3, -4. The inversion provides a positive edge with the proper phase relationship needed for the frequency doubler circuit that follows. The frequency doubler circuit is a phase lock loop circuit composed primarily of U36, Q1, Q2, and U34. The frequency reference for the phase lock loop is the 2048 kHz output from U10-4. This signal arrives at the clock input of the reference D flip-flop, U36-2, -3, -5, -6. This reference flip-flop, with an identical variable frequency flip-flop, U36-9, -11, -12, forms the phase detector circuit of the phase lock loop. The positive edges of the incoming 2048 kHz frequency reference set the Q output of the reference flip-flop. This raises one input of NAND gate U19-4, -5, -6 to a logic 1 and enables it. The *Q output of reference flip-flop U36-6 falls to a logic 0. This logic 0 state turns on transistor Q1. Q1 connects R27 to the +5 V supply, and R27 charges capacitor C65 through R32. Capacitor C65 and resistor R32 low pass filter the phase detector output voltage.

U34 contains two voltage-controlled oscillators (VCOs). Only one is used. The voltage-sensitive control input, pin U34-2, is connected to the low pass filter. When Q1 is on, the voltage on this input rises, which in turn increases the output frequency at pin U34-7. When the loop is locked, the output frequency of the VCO is 4096 kHz. It is routed to U19-11, -12, -13.

Inside the loop, the 4096 kHz signal on pin U34-7 is connected to the clock input of JK flip-flop U48-13, -7. This flip-flop is connected to divide the 4096 kHz by 2 to generate another 2048 kHz signal that is routed to the variable flip-flop. This flip-flop forms the other half of the phase detector. The positive edges of the 2048 kHz waveform set the Q output, U36-9. This output becomes the second logic 1 input to U19-4, -5, -6. U19-6 will then go to a logic 0, which clears both phase detector flip-flops. When the reference flip-flop clears, transistor Q1 turns off.

The previous discussion showed that when the positive edge on the reference flip-flop (U36-2, -3, -5, -6) occurred before the positive edge on the variable flip-flop (U36-9, -11, -12), Q1 was turned on for the time interval between the positive edges. This caused C65 and the voltage sensitive input of the VCO to charge toward a higher voltage level. This higher voltage level caused the VCO frequency to increase. The increase in frequency will cause the positive edge on the variable flip-flop to occur sooner than it would if the frequency had not increased. Therefore, the feedback around the loop is negative because it tends to oppose any change.

The opposite occurs when the positive edge on the variable flip-flop precedes the positive edge on the reference flip-flop. Suppose

a positive edge occurred on pin U36-11 first. This would set flip-flop output U36-9 to a logic 1, which would enable U19-4 and turn on transistor Q2. When transistor Q2 is on, it drains charge from C65, which decreases the voltage across it. This lower voltage level at the input of the VCO decreases the VCO frequency. This means that the positive edge will arrive at the variable flip-flop input later on the next cycle. Again, the feedback is negative. The positive edge arriving at the input of the reference flip-flop will terminate this cycle. It will set it, force output U19-6 to a logic 0, and clear both flip-flops. When both are cleared, Q2 will turn off.

In summary, the phase lock loop doubles the 2048 kHz output of U9, and provides a 50 percent duty cycle, 4096 kHz, square wave output at pin U19-11. U19 is used as a driver and as an inverter to provide the proper phase relationship.

3.13 GROUP TIMING, 4608 kHz

As previously mentioned, group 1 and 2 data rates at the COAX1 and COAX2 connectors are multiples of either 128 or 144 times 2 to the Nth power. The 144 X 2^N family rates are 144, 288, 576, 1152, 2304, and 4608 kb/s. The demultiplexer board is designed to generate the 4608 kHz clock first and then derive the rest of the clock rates by repeatedly dividing by 2.

Generating a 4608 kHz clock is an easy task. A master clock frequency of 18432 kHz only requires division by 4 to result in 4608. U25 divides the 18432 kHz master clock by 4. The count "1100" is loaded on the positive edge of the master clock when U56-11 is logic 0. U56-11, -12, -13 and U10-9, -8 are used to synchronize U-25's output with the outputs of the master timing chain. Once U25 has been loaded with the initial count "1100," it increments with each positive edge of the master clock on U25-2: 1100, 1101, 1110, 1111, 1100, 1101, 1110 . . . . At the beginning of count "1111," the ripple carry output U25-15 rises to a logic 1. U10-9, -8 inverts it and provides a logic 0 at U56-13. This logic 0 forces the output U56-11 to logic 0. Since U56-11 is connected to counter load input U25-9, a logic 0 on this pin will cause the initial count "1100" to be reloaded on the next positive edge of the master clock. Therefore, the counter divides the master clock by 4. The output of U25-13 is 18432 kHz divided by 4, or 4608 kHz.

Notice that the AND gate is really being used as a negative logic OR gate. A logic 0 at U56-12 or U56-13 or both will result in a logic 0 at U56-11 and U25-9. This will cause the counter to be reloaded on the next positive edge of the master clock. Therefore, the counter can be reloaded by either the occurrence of the terminal

count or through the arrival of a negative synchronizing pulse from the master timing chain at U56-12. When the board is first powered up, the initial synchronizing pulse arriving on U56-12 will force U25 to synchronize to the master timing chain. Once this has been accomplished, the negative pulses on U56-12 and U56-13 should overlap.

The 4608 kHz output from U25-13 is routed to inverter U10-11, -10. The inversion provides a 4608 kHz clock with the proper phase relationship needed for the circuits that follow.

3.14 GROUP TIMING, 1536 kHz

As previously mentioned, group 1 and 2 data rates at the COAX1 and COAX2 connectors are multiples of either 128 or 144 times 2 to the Nth power. One of the data rates available on the AN/TAC-1 cannot be derived by repeatedly dividing either 4096 kHz or 4608 kHz by 2. This is the 1536 kHz rate, which is 128 times 12. The demultiplexer board is designed to generate the 1536 kHz clock by dividing the 6144 kHz output of U23 by 4.

U24 divides the 6144 kHz clock by 4. The count "1100" is loaded on the positive edge of the master clock when U56-3 is logic 0. U56-1, -2, -3 and U10-1, -2 are used to synchronize U-24's output with those of the master timing chain. Once U24 has been loaded with the initial count "1100," it increments with each positive edge of the master clock on U24-2: 1100, 1101, 1110, 1111, 1100, 1101, 1110 . . . . At the beginning of count "1111," the ripple carry output, U24-15, rises to a logic 1. U10-1, -2 inverts it and provides a logic 0 at U56-1. This logic 0 forces output U56-3 to logic 0. Since U56-3 is connected to counter load input U24-9, a logic 0 on this pin causes the initial count "1100" to be reloaded on the next positive edge of the master clock. Therefore, the counter divides the master clock by 4. The output on U24-13 is 6144 kHz divided by 4, or 1536 kHz.

Notice that the AND gate is really used as a negative logic OR gate. A logic 0 at U56-1 or U56-2 or both will result in a logic 0 at U56-3 and U24-9. This will cause the counter to be reloaded on the next positive edge of the master clock. Therefore, the counter can be reloaded by either the occurrence of the terminal count or through the arrival of a negative synchronizing pulse from the master timing chain at U56-2. When the board is first powered up, the initial synchronizing pulse arriving on U56-2 will force U24 to synchronize to the master timing chain. Once this has been accomplished, the negative pulses on U56-1 and U56-2 should overlap.

The 1536 kHz output from U24-13 is routed to pin 2 on U1 and U2 where it may be selected as the group 1 or group 2 clock.

3.15 GROUP CLOCK SELECTION AND GENERATION

U1 and U2 are type 54S151 data selectors. Each chip is presented with seven input clocks from either the 4096 or 4608 family of rates and the 1536 kHz clock. Each chip has only one output. The output of U1 provides the group 2 clock for the rest of the board, and the output of U2 provides the group 1 clock. The digit selected with the right thumbwheel switch on the front panel controls U1, and the digit selected with the left thumbwheel switch controls U2.

Both thumbwheel switches are on the front control panel. The leftmost (group 1) switch has four outputs labeled MSEL1A, MSEL1B, MSEL1C, and MSEL1D. Each output will assume one of two states: a connection to circuit ground or an open circuit. The four lines are connected by a cable harness to the card cage backplane and card connector pins. The signal conditioning traffic modem circuit card assembly contains 10 kilohm pull-up resistors, which connect to each MSEL line. Therefore, a line switched to circuit ground assumes a logic 0 state, and a line switched open assumes a logic 1 state. If the state of each line is measured and recorded in the sequence "DCBA," the result will be the complement of the hexadecimal representation of the switch number selected. For example, if the measured "DCBA" code is "1111," the 1's complement of this is "0000," and the digit selected is "0." If the measured "DCBA" code is "0101," the 1's complement of this is "1010," and the digit selected is "10." The rightmost (group 2) switch has four outputs called MSEL2A, MSEL2B, MSEL2C, and MSEL2D. It is connected, pulled up, and coded in the same way as the leftmost switch.

The relationship between the digit selected on the thumbwheel switch and the group rate is shown in figure 4. Notice that the 128 family rates are all even numbers, the 144 family rates are all odd numbers, and the digits "10" and "11" are reserved for the special 1536 kb/s rate. With this scheme, the least significant bit output from thumbwheel switches "A" is used to select the rate family that will be routed to U1 and U2. The remaining three bits "DCB" are used to select one of the eight rates presented.

For example, selecting either 14 or 15 on the group 1 thumbwheel switch means the MSEL1 output lines assume the logic states "0001" or "0000," respectively. Since these codes are read "DCBA," MSEL1D, MSEL1C, and MSEL1B will always be at logic 0. MSEL1D (ECCP 32, 82),

Digit	128 Rate	144 Rate	Special	"DCBA"
0	64			1111
1		72		1110
2	128			1101
3		144		1100
4	256			1011
5		288		1010
6	512			1001
7		576		1000
8	1024			0111
9		1152		0110
10			1536	0101
11			1536	0100
12	2048			0011
13		2304		0010
14	4096			0001
15		4608		0000

Figure 4. Relationship of Thumbwheel Digit Selected to Group Data

MSEL1C (ECCP 33, 83), and MSEL1B (ECCP 36, 86) are connected on the demultiplexer board to pins 9, 10, and 11, respectively, of U2. For U2, pins 9, 10, and 11 are read "CBA," respectively, when determining which input to select and route to the output. The decimal "CBA" weight versus input pin and rate selected is shown in table 4.

Table 4

Weight Versus Rate

"CBA"	Pin	Rate (Even/Odd)
0	4	4096/4608
1	3	2048/2304
2	2	1536/1536
3	1	1024/1152
4	15	512/576
5	14	256/288
6	13	128/144
7	12	64/72

The rate selected column shows the even and odd rate. Which one is input on the designated pin depends upon whether MSEL1A, ECCP 28, 78 is logic 0 (even) or logic 1 (odd). The selected group 1 rate is always output on pin U2-5.

U1 provides the group 2 clock in the same way as U2, and the previous discussion applies. However, MSEL2D (ECCP 39, 89), MSEL2C (ECCP 40, 90), and MSEL2B (ECCP 41, 91) select "CBA" pins 9, 10, and 11, respectively, of U1. The decimal "CBA" weight versus input pin and rate selected is the same as that previously shown for U2. The group 2 rate is always output on U1-5.

U3 and U4 are 54S161, synchronous, four-bit counters. They are connected in series to form a total of eight divide-by-2 stages. Each of the eight stages is serially connected, output to input. The initial clock input is either 4096 or 4608 kHz. It is connected to pins U3-2 and U4-2 and is successively divided by 2 in each stage. The divisor, output pin, and resulting 4096 and 4608 output family rates are shown in table 5. Because these group rates are not allowed, outputs from U4-12 and U4-11 are "no connection." All of the other rates, however, are simultaneously available and are connected to U2 so that one may be selected as the group 1 clock. This clock is then used to clock the group 1 data out of the demultiplex registers formed by U39 and U40. It is also output on ECCP 21 as the signal GR1CLKA for use on the group 1 signal conditioner traffic card.

Table 5. U3 and U4 Rates

Divisor	Output	4096 Input (kb/s)	4608 Input (kb/s)
2	U3-14	2048	2304
4	U3-13	1024	1152
8	U3-12	512	576
16	U3-11	256	288
32	U4-14	128	144
64	U4-13	64	72

U5 and U6 function in the manner previously described for U3 and U4. The divisor, output pin, and resulting 4096 and 4608 rates are shown in table 6. The outputs from U6-12 and U6-11 are also "no connection." All other rates, however, are simultaneously available and are connected to U1 so that one may be selected as the group 2

clock. This clock is then used to clock the group 2 data out of the demultiplex registers formed by U35 and U42. It is also output on ECCP 19, 69 as the signal GR2CLKA for use on the group 2 signal conditioner traffic card.

Table 6. U5 and U6 Rates

Divisor	Output	4096 Input (kb/s)	4608 Input (kb/s)
2	U5-14	2048	2304
4	U5-13	1024	1152
8	U5-12	512	576
16	U5-11	256	288
32	U6-14	128	144
64	U6-13	64	72

U7 is a 54LS51; it contains a pair of AND-OR-INVERT gates. One AND-OR-INVERT gate, U7-2, -3, -4, -5, -6, selects either the 4096 or 4608 kHz clock and sends it to the group 1 divider chain consisting of U3 and U4. The other AND-OR-INVERT gate, U7-1, -8, -9, -10, -11, -12, -13, selects a clock for the group 2 divider chain consisting of U5 and U6.

The 4608 clock is always present on pin U7-1, -3, and the 4096 clock is always present on pin U7-4, -11. MSEL1A, ECCP 28, 78, is connected to U7-5; it is also inverted by U8-1, -2 and connected to U7-2. If the logic state of MSEL1A is 0, then U7-5 is 0 and U7-2 is 1. This selects the 4608 kHz clock on pin U7-3 and gates it out on pin U7-6. U7-6 is connected directly to U2-4 so that the 4608 kHz clock may be selected as the group 1 clock and output on U2-5. If the logic state of MSEL1A is 1, U7-5 is 1 and U7-2 is 0. This selects the 4096 kHz clock on pin U7-4 and gates it out on pin U7-6. U7-6 is connected directly to U2-4 so that the 4096 kHz clock may be selected as the group 1 clock and output on U2-5. U8-9, -8 inverts the 4608 or 4096 kHz output of U7-6 and sends it to group 1 dividers U3 and U4. Here the clock is successively divided by 2 to generate all submultiple clocks for selection by U2.

3.16 SYNCHRONIZATION STRATEGY

When the demultiplexer is out of synchronization, it will search the incoming bit stream and try to reacquire and align the "10011111" framing pattern. This is called the search mode of operation. The

synchronization strategy is to require three successive pulses from the framing pattern detector before leaving the search mode and going into the maintenance mode. A single pulse from the framing detector requires that the framing bit be in the first position of the fiber optic register, and that there be no framing bit errors. This means that each framing bit in 8 successive 24-bit subframes must be in the proper time slot and logic state.

In the maintenance mode, the demultiplexer requires one pulse from the framing pattern detector in four successive frames to maintain it. When there is no single pulse in four, the demultiplexer automatically drops into the search mode. It remains in the search mode until the three successive pulses from the framing pattern detector necessary to go into maintenance are received again. Therefore, the demultiplexer is either in the search mode trying to acquire synchronization or in the maintenance mode holding onto it.

U20 is a 54LS164, eight-bit, serial-in-parallel-out shift register. Pulses that arrive from the framing pattern detector are shifted into it and stored. The serial input, U20-1, -2, is connected directly to the framing pattern detector output U33-13. U20 is clocked by the positive edges of U13-6, which come from the 32 kHz ripple carry output of U31-15. The positive edges from U13-6 are synchronized by the 256 kHz and 6144 kHz ripple carry outputs on input U13-5. U20 is the framing pulse storage register. The outputs of U20 contain logic 1s if a proper in-frame pulse was received; otherwise, they contain logic 0s. The last four output pulses received are on outputs U20-3, -4, -5, and -6. U20-3 contains the pulse that was just received, while U20-4, -5, and -6 contain pulses received later.

Inverters U15-5, -6, U15-13, -12, and U15-9, -8 are connected to inputs U17-9, -10, and -11, respectively, of gate U17. This combination forms an AND gate that gates two outputs of the framing pulse storage register U20-3, -4 together, along with the input U20-1, -2 to provide a logical product at U17-8. This AND gate is the search detector. It provides a logic 1 output only when it detects three successive framing pulses. If any of the framing pulses is missing, the output will be logic 0. Note that the search detector looks at the two most recent states stored on pins U20-3, and -4, and the state that will be shifted next into U20. This "look-ahead" design eliminates the single frame delay that would be experienced if the states were all taken from shift register U20.

NOR gate U18 is the maintenance detector. It provides a logic 0 output when it detects a valid framing pulse on any one of its input lines. If all of the last four pulses were missing, it would provide

a logic 0 output. Inputs U18-9, -10, -12, and -13 are connected to the U20 outputs, which contain the last four framing pulses received.

The framing flip-flop, U28-2, -3, -5, indicates whether the demultiplexer is in the search mode or maintenance mode, and it latches that state and remembers it. If the Q output, U28-5, is at logic 0, then the demultiplexer, or demux, is in the maintenance mode and in frame. If it is at logic 1, the demux is in the search mode and out of frame. Notice that the *Q output, U28-6, drives inverter U52-1, -10, which in turn drives ECCP 71. ECCP 71 is connected to the frame sync indicator on the front control panel. The frame sync indicator is a light emitting diode with its anode connected to a resistor, which in turn is connected to +5 V. When the Q output is logic 0, ECCP 71 is logic 0 too. This means inverter output U52-10 will sink the current from the indicator and cause it to illuminate. When this front panel indicator is on, the demux is in frame. When the Q output is logic 1, the inverter output goes to a logic 1 and the indicator is extinguished signifying the demux is out of frame.

Assume the demultiplexer is out of frame. Then the framing pulses at the input of U20-1, -2 are missing and U20 fills with logic 0s. This causes the search detector output U17-8 to go to logic 0, and the maintenance detector output U18-8 to go to logic 1. The logic 1 on U18-8 will cause output U14-1 and input U14-11 to go to logic 0. This makes U14-11 and -12 inputs logic 0, which makes the demultiplexer output U14-13 logic 1. This makes the D input, U28-2, logic 1. Therefore, at the next positive edge of the 32 kHz clock on U28-3, the Q output of the framing flip-flop will assume a logic 1. As previously discussed, this indicates the demultiplexer is out of frame.

When the demultiplexer is out of frame, the logic 1 output of U28-5 is fed back to the input of U14-3. This causes the output U14-1 and the input U14-12 to go to logic 0. When the input U14-12 is at logic 0, the output U14-13 is totally dependent upon the input U14-11. This is the output of the search detector, U17-8. Therefore, once the demux is out of frame, the feedback ensures that only the search detector output can put it back into frame. The search detector requires three successive good frames before its output U17-8 will go to a logic 1. This will cause output U14-13 to go to a logic 0, and the next positive edge on U28-3 will clear the Q output of the framing flip-flop. When U28-5 is clear, the demux is in frame.

When the demux is in frame, the logic 0 output of U28-5 is fed back to the input of U14-3. Assuming it has just gone into frame, outputs U20-3 and -4 will be logic 1. Since these are connected to U18-13, -12, the output U18-8 will be logic 0. With both inputs

U14-2 and -3 at logic 0, output U14-1 is logic 1. Since U14-1 is connected to U14-12, it is logic 1 too. If U14-12 is logic 1, the output U14-13 is logic 0. This holds the Q output of the framing flip-flop in the reset state, which maintains frame synchronization. Therefore, the in-frame state will persist until the output of the maintenance detector, U18-8, goes to a logic 0. This requires that each of the last four framing pulses stored in U20 be missing, which would mean outputs U20-3, -4, -5, and -6 are logic 0.

3.17 SYNCHRONIZATION PROCESS

The synchronization process is where the demux acquires frame synchronization and holds it. When the demux is first turned on and serial data at 6144 kb/s begins to flow through the fiber optic register (U37/U38/U41), the demux does not know which bits belong to group 1, which belong to group 2, and which belong to auxiliary data. Therefore, it can't separate the bits from one another. To separate the bits, or demultiplex them, the circuit has to position the bits in the fiber optic register so that the group 1, group 2, and auxiliary bits occupy specific positions at a given instant. During this instant, the bits are separated by transferring them in parallel to another register where they will be shifted out serially at the appropriate clock rate.

The synchronization process begins when the maintenance detector output, pin U18-8, goes to logic 1 signifying an out of frame condition. This causes input U14-2 to go to logic 1 and output U14-1 to go to logic 0. U14-4, -5, -6 ANDs the output of the framing pattern detector on pin U14-6 with the inverted output of the maintenance detector on pin U14-5. When both are logic 0, output U14-4 becomes a logic 1, which starts the frame-search sequence.

The frame-search sequence is synchronized by divide-by-8 counter U31. Note that the maintenance detector output goes to logic 1 after U20-8 has been clocked by the negative edge of the ripple carry output of U31-15 via U13-4, -6. The negative edge of the ripple carry output would normally occur just as counter U31 is reloaded with the count "1000"; however, when the demux is out of frame, the framing pulses that reload the counter via input U13-13 are absent, and the counter free runs. Instead of being reloaded to "1000" after the terminal count of "1111," it continues to count up to the next state "0000." These bits are output on U31-11, -12, -13, -14 and are ANDed together by U18-5, -4, -2, -1. When U18-5, -4, -2, -1 are all logic 0, output U18-6 goes to logic 1. This logic 1 and the logic 1 output on U14-4 are ANDed together at U26-2, -1. The logic 1 output on U26-3 enables a single-frame search sequence.

A frame-search sequence is enabled by a logic 1 at U26-3. The search sequence commences when the RCO of U21-15 is logic 1. The RCO is ANDed with the search sequence authorization and produces a logic 1 at U26-6. This logic 1 starts the search sequence by causing counter U22 to divide by 9 rather than its usual 8. The logic 1 and inverter U15-11, -10 change the value that will be loaded into U22 from "1000" to "0111." This causes U22 to change from a divide-by-8 counter to a divide-by-9 counter. When U22 divides by 9, the RCO of U22-15 will occur after nine periods of the 6144 kHz ripple carry output of U23-15 rather than eight periods. After nine periods of the 6144 kHz RCO on U22-7, the RCO of U22 occurs on U22-15 and enables U21 to count up one state from "1111" to "1101." This causes the RCO of U21-15 to go to logic 0, and this in turn causes input U26-4 and output U26-6 to go to logic 0. Although the search is still enabled by a logic 1 level on U26-3, output U26-6 going to logic 0 restores U22 to a divide-by-8 counter. With U22 restored to divide-by-8, eight periods of 6144 kHz will occur before the RCO of U22-15 will go to logic 1 again. U22-15 high will enable U21, which will be clocked to state "1110." Since RCO U21-15 is still logic 0, another divide-by-8 cycle occurs before U21 is clocked to state "1111," and its RCO U21-15 goes to logic 1. At this point we have waited through 9 + 8 + 8 periods of 6144 kHz. This means that 25 bits have been clocked through the fiber optic register formed by U37/U38/U41.

The RCO of U21-15 is also used to sample the bit in the first position of the fiber optic register via U13-10, -8, U16-12, -9, and U47-8. Positive edge U47-8 causes the bit in the first position of the fiber optic register, U37-3, to be clocked into the eight-bit register U47 at pin U47-1. The eight bits stored in this register are presented to the framing pattern detector, which will output a logic 1 on U33-13 when the bits stored are equal to the framing pattern "10011111." Therefore, clocking through 25 bits, rather than 24, has resulted in a slippage of one bit in the 6144 kb/s data stream flowing through the fiber optic register. This means we have skipped a single bit and are now searching for the framing pattern one bit later in the serial stream. Now at least 8 subframes of 24 bits need to be sampled before another bit is skipped. This is because eight framing bits need to be accumulated in U47 before the framing pattern detector can develop a framing pulse on U33-13 to end the search process.

U31 samples the next eight subframes without skipping another bit in the serial stream. When the RCO of U21 goes to a logic 1, it enables U31, which is clocked to the next state "0001." This bit pattern causes outputs U18-6 and U26-3 to go to logic 0. Since a logic 1 at U26-3 enables a search, a logic 0 terminates a search. Although the demux is still out of frame, as evidenced by a logic 1

at output U14-4 and input U26-1, the serial stream is being sampled repeatedly in the same spot. This will continue for 16 subframes because U31 will be incremented "0010," "0011," . . ., "0111," at which time eight framing bits will have accumulated in U47. If at this time a framing pulse is output at U33-13, indicating the framing pattern has been located, this pulse will reload U31 with "1000" on the next clock via U13-12, -13. If a framing pulse is not output, U31 will count "1000," "1001,"
. . ., "1111" and accumulate eight more bits into U47 for another try at finding the framing pattern. This second chance is needed when there are bit errors in the serial data stream because a framing bit error will prevent a framing pulse from occurring. If the framing pulse is still not forthcoming, the next count of U31 will be "0000," which will cause the outputs of U18-6 and U26-3 to again go to a logic 1. This enables another search, allows another 25 bits to go by, and permits the entire process to be repeated.

Therefore, the slipping of 1 bit at a time and the sampling of 16 subframes continues until frame synchronization is achieved. Frame synchronization is achieved when three error-free frames have been detected in succession. This requires that the bit error rate of the serial stream be relatively low. When frame synchronization occurs, the demultiplexer transitions to the maintenance mode. In the maintenance mode, only one frame pattern in four is required to be error-free. This allows the demultiplexer to stay in frame with a relatively high bit error rate.

SECTION 4

PERFORMANCE REQUIREMENTS

The demultiplexer CCA performance will be specified for double group, auxiliary, and single group traffic. A set of stimulus signals will be specified along with the required responses.

4.1 DOUBLE GROUP PERFORMANCE

Double group performance will be specified with simulated traffic on group 1 and group 2; the traffic rates will be 2048 and 2304 kb/s, respectively.

4.1.1 Double Group Stimulus

The input stimulus signals for a double group will be as specified in table 7 and figures 5 and 6. Table 7 specifies both the static and dynamic input signals that will be applied to the demultiplexer CCA to ensure that performance requirements are being met. Figure 5 specifies the 6144 kb/s FODATARCV signal in greater detail. This signal contains the multiplexed group 1, group 2, and auxiliary traffic. Eight separate frames of 24 data bits are shown. The last data bit on the right-hand side of frame 1 (a logic 1) is labeled FBT; it will be the first bit transmitted. The last bit of frame 1 transmitted is the bit on the far left-hand side (a logic 1). The transmission of frame 1 will immediately be followed by the transmission of frame 2. As with frame 1, the last bit transmitted is the bit on the far left-hand side. Frame 2 is immediately followed by frames 3 through 8, in the bit order previously given for frames 1 and 2. When the bit on the far left-hand side of frame 8 (labeled LBT for last bit transmitted) has been sent, the process begins over again with frame 1. Therefore, the eight frames shown in figure 5 are continuously transmitted in the order previously described. This serial data stream will meet TTL amplitude and rise/fall time requirements while driving the multiplexer CCA.

Figure 6 specifies the phase relationship that will exist between the stimulus signals FODATARCV (CCA pins 6 and 56) and 6144CLK (CCA pins 5 and 55). The positive edge of 6144CLK must occur in the approximate center of the data bit cells of FODATARCV. The logic state of the data cell is irrelevant; therefore, the bit cell has

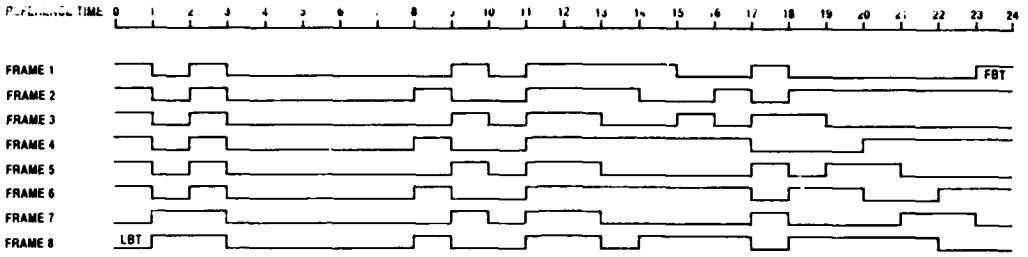


Figure 5. FODATARCV Double Group Stimulus

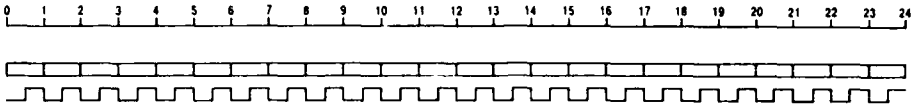


Figure 6. FODATARCV/6144CLK Phase Relationship

Table 7. Double Group Stimulus

Name	CCA Pins	Specification
+5V	1,2,49,50,51,52,99,100	+5 V dc power input
GND	3,4,47,48,53,54,97,98	+5/+12 V dc power ground
+12V	37,38,87,88	+12 V dc power input
-12V	34,35,84,85	-12 V dc power input
COAX3FOSEL	45,95	Logic 0
FODATARCV	6,56	Figure 5
MSEL2D	38,89	Logic 0
MSEL2C	40,90	Logic 0
MSEL2B	41,91	Logic 1
MSEL2A	25,75	Logic 0
MSEL1D	32,82	Logic 0
MSEL1C	33,83	Logic 0
MSEL1B	36,86	Logic 1
MSEL1A	28,78	Logic 1
6144CLK	5,55	Figure 6
CH11CONT	30,80	Logic 0
CH12CONT	29,79	Logic 0

NOTE: CCA pins not shown in this table will be left open-circuited and not connected.

been drawn as a rectangular box. The vertical lines represent the beginning and end of each data bit cell.

All signals must meet TTL amplitude and rise/fall time requirements while driving the multiplexer CCA inputs. Their phase relationship to one another should remain approximately constant. To maintain the fixed phase relationship between the two stimulus signals shown in figure 6, we could derive both from a single master clock, or FODATARCV from 6144CLK. The data rate of FODATARCV is 6144 kb/s.

4.1.2 Double Group Response

Double group performance is specified by documenting the static and dynamic output responses that must be exhibited by the demultiplexer CCA being stimulated. The absence of any of these, or a failure to conform to the requirements in the succeeding subparagraphs, constitutes unacceptable performance. The amplitude of all signals shown must, unless otherwise specified, meet the requirements for TTL.

1. Test point J1-1 response

   Figure 7 shows the required response at J1-1 with the stimulus of table 7 and figures 5 and 6. It is a logic 0 pulse with a 256 kHz repetition rate.

2. Test point J1-2 response

   Figure 8 shows the required response at J1-2. It is a logic 1 pulse with a 256 kHz repetition rate.

3. Test point J1-3 response

   Figure 9 shows the required response at J1-3. It is an asymmetrical 6144 kHz clock signal with a logic 1 to logic 0 ratio of approximately 1:2.

4. Test point J1-4 response

   Figure 10 shows the required response at J1-4. It is a logic 0 pulse with an 8 kHz repetition rate.

5. Test point J1-5 response

   Figure 11 shows the required response at J1-5. It is the external signal FODATARCV after it has been resynchronized to the internal 6144 kHz clock of the demultiplexer CCA.

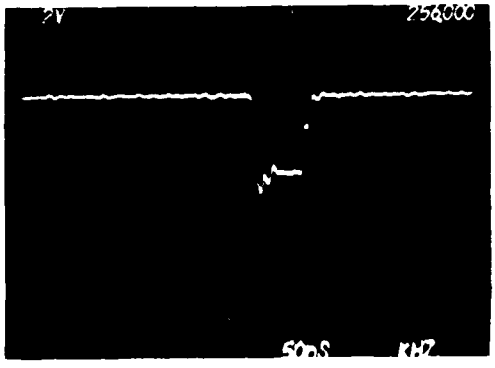


Figure 7. Test Point J1-1

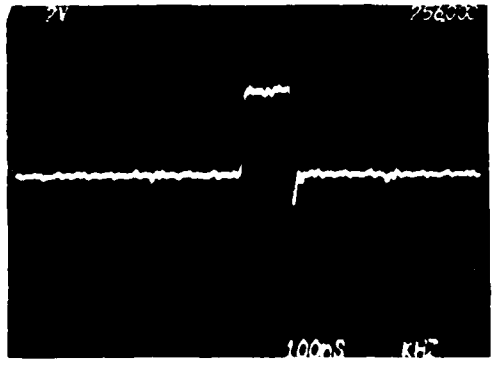


Figure 8. Test Point J1-2

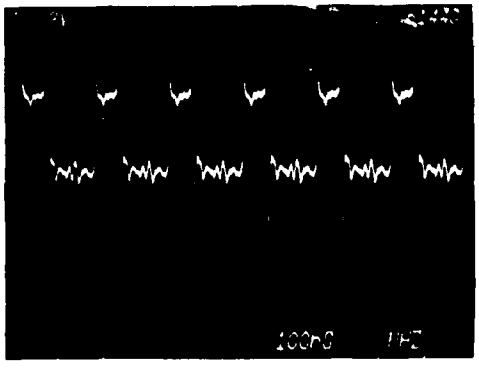


Figure 9. Test Point J1-3

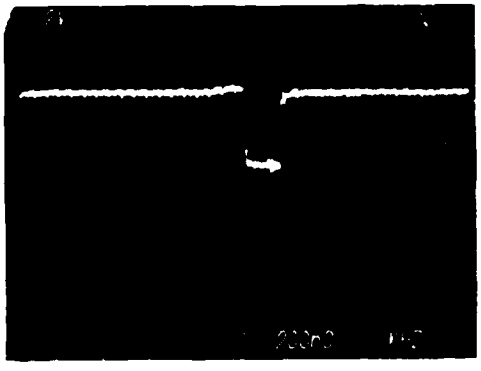


Figure 10. Test Point J1-4

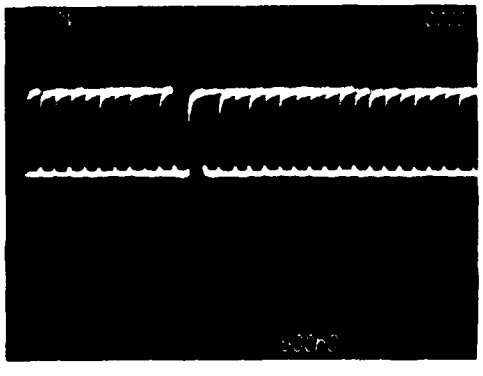


Figure 11. Test Point J1-5

Figure 12. Test Point J1-6

6. Test point J1-6 response

   Figure 12 shows the required response at J1-6. It is a logic 0 pulse with a repetition rate of 32 kHz.

7. Test point J1-7 response

   Figure 13 shows the required response at J1-7. It is a logic 1 pulse with a repetition rate of 32 kHz.

8. Test point J1-8 response

   Figure 14 shows the required response at J1-8. It is FODATARCV being shifted through the demultiplexer shift register at the internal 6144 kHz clock rate.

9. Test point J1-9 response

   Figure 15 shows the required response at J1-9. It is FODATARCV with the data levels inverted by the demultiplexer CCA logic.

10. Test point J1-10 response

    The response at J1-10 is a continuous TTL logic 0 level. This indicates the demultiplexer is in frame.

11. Test point J1-11 response

    Figure 16 shows the required response at J1-11. It is a train of sinusoidal pulses at a repetition rate of 18432 kHz, the demultiplexer CCA master clock frequency. The amplitude of the sinusoidal pulses is greater than 750 millivolts peak-to-peak.

12. Test point J1-12 response

    Figure 17 shows the required response at J1-12. It is a 4608 kHz square wave.

13. Test point J1-13 response

    Figure 18 shows the required response at J1-13. It is an asymmetrical square wave at a repetition rate of 18432 kHz.

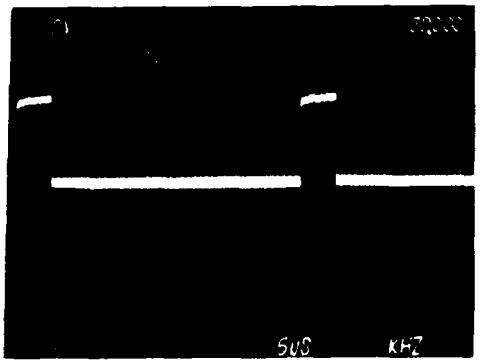


Figure 13. Test Point J1-7

Figure 14. Test Point J1-8

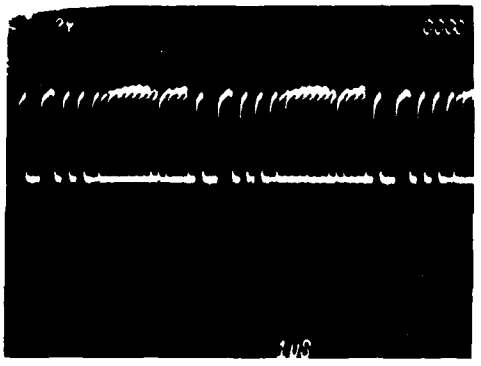


Figure 15. Test Point J1-9

Figure 16. Test Point J1-11

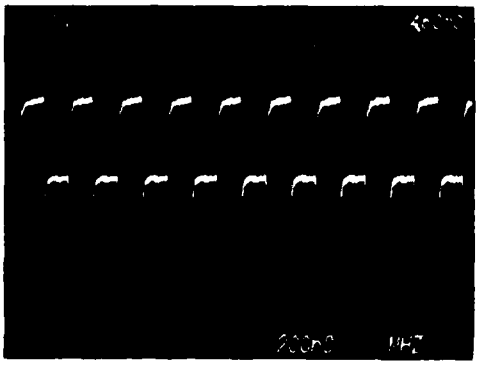


Figure 17. Test Point J1-12

Figure 18. Test Point J1-13

14. Test point J1-14 response

Figure 19 shows the required response at J1-14. It is a square wave at the group 2 clock rate, 2304 kHz.

15. Test point J1-15 response

Figure 20 shows the required response at J1-15. It is a 6144 kHz asymmetrical square wave with a logic 0 to logic 1 ratio of approximately 1:2.

16. Test point J1-16 response

Figure 21 shows the required response at J1-16. It is a square wave clock signal at the group 1 rate, 2048 kHz.

17. Test point J1-17 response

Figure 22 shows the required response at J1-17. It is a logic 0 pulse occurring at a repetition rate of 256 kHz.

18. Test point J1-18 response

Figure 23 shows the required response at J1-18. It is a 4096 kHz square wave clock signal.

19. Test point J1-20 response

Figure 24 shows the required response at J1-20. It is an asymmetrical 6144 kHz clock signal with a logic 1 to logic 0 ratio of 1:2.

20. Test point J1-21 response

Figure 25 shows the required response at J1-21. It is a series of logic 0 pulses at a 2048 kHz rate.

21. J1-22/J1-23 relationship

Figure 26 shows the relationship between the series of logic 1 pulses at J1-22 (top) and the 2048 kHz square wave at J1-23 (bottom). The phase relationship between positive going edges of the logic 1 pulses and the positive going edges of 2048 kHz square wave remains fixed, and the 50 percent amplitude point of the positive going edges of the 2048 kHz square wave occurs no later than 25 ns after the positive going edges of the logic 1 pulses.

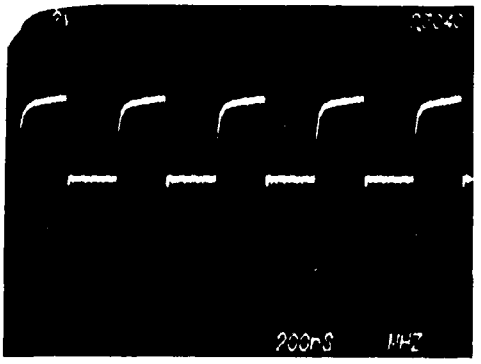


Figure 19. Test Point J1-14

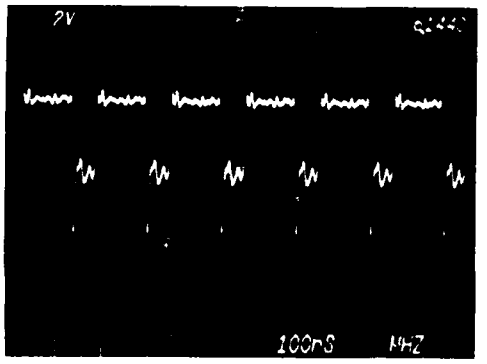


Figure 20. Test Point J1-15

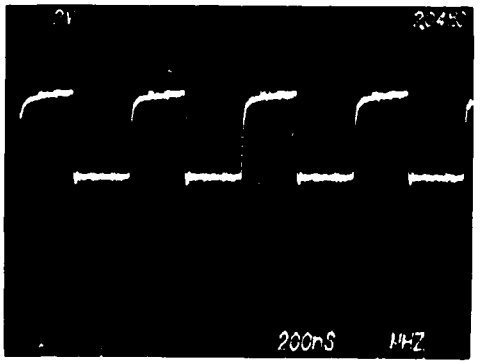


Figure 21. Test Point J1-16

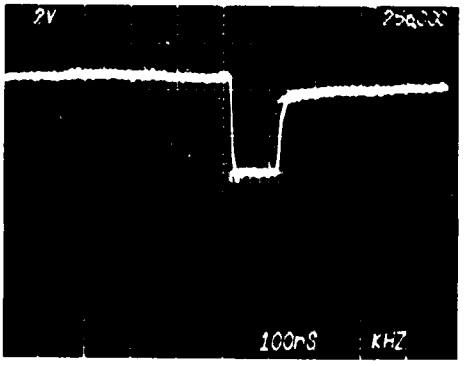


Figure 22. Test Point J1-17

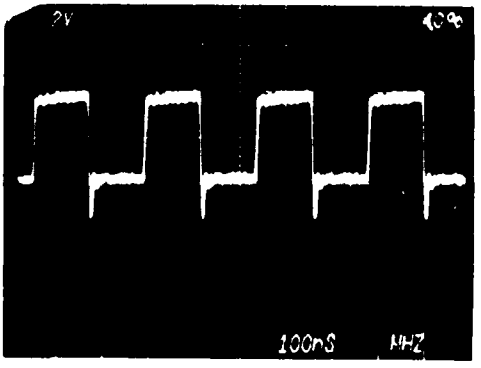


Figure 23. Test Point J1-18

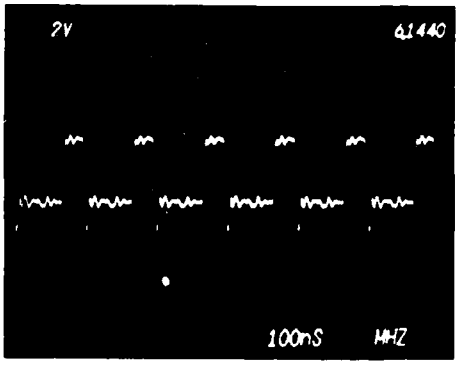


Figure 24. Test Point J1-20

22. Test point J1-24 response

Figure 27 shows the required response at J1-24. It is a series of logic 0 pulses repeating at 256 kHz rate.

23. J1-9/J1-3 relationship

Figure 28 shows the relationship between the FODATARCV data at J1-9 and the local 6144 kHz clock at J1-3. J1-9 is the top trace, and J1-3 is the bottom trace. The positive edges of the local 6144 kHz signal clock the data and resynchronize it to the signals on the demultiplexer board. The positive edges of the 6144 kHz clock occur inside the data cell; additionally, they occur at least 20 nanoseconds after the left-hand edge of the data cell.

24. J1-5/J1-15 relationship

Figure 29 shows the required relationship between J1-5, on top, and J1-15, on the bottom. J1-5 is the FODATARCV that has been resynchronized to the demultiplexer board clocks. J1-15 is the 6144 kHz clock used to shift the data into a 24-bit serial-in shift register for demultiplexing. The positive edges of the 6144 kHz clock occur inside the data cell. Additionally, they occur at least 15 nanoseconds before the left-hand edge and at least 5 nanoseconds before the right-hand edge of the data cell.

25. J1-15/J1-16/J1-2 relationship

Figure 30 shows J1-15 as the top trace, J1-16 in the middle, and J1-2 on the bottom. J1-15 is a 6144 kHz clock, J1-16 is a 2048 kHz clock, and J1-2 is a logic 1 pulse with a repetition rate of 256 kHz. The positive edge of J1-16 (middle) occurs during the time J1-2 (bottom) is at the logic 1 level. The positive edges of J1-15 (top) must be at least 30 nanoseconds removed from the positive edge of J1-16 (middle).

26. J1-15/J1-16/J1-17 relationship

Figure 31 shows J1-15 as the top trace, J1-16 in the middle, and J1-17 on the bottom. J1-15 is a 6144 kHz clock, J1-16 is a 2048 kHz clock, and J1-17 is a logic 0 pulse with a repetition rate of 256 kHz. The positive edge of J1-16 (middle) occurs during the time J1-17 (bottom) is at the logic 0 level. The positive edges of J1-15 (top) must be at least 20 nanoseconds removed from the positive edge of J1-16 (middle).

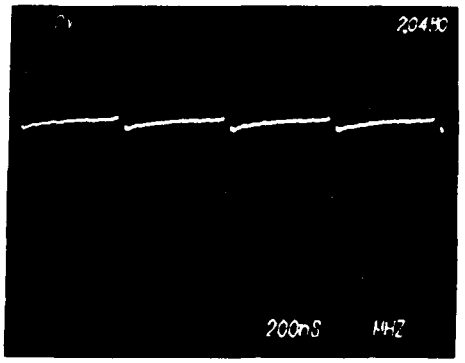


Figure 25. Test Point J1-21

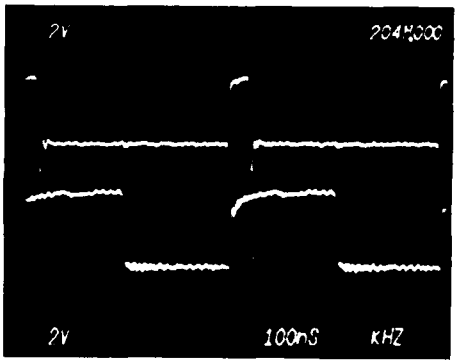


Figure 26. Test Points J1-22/J1-23

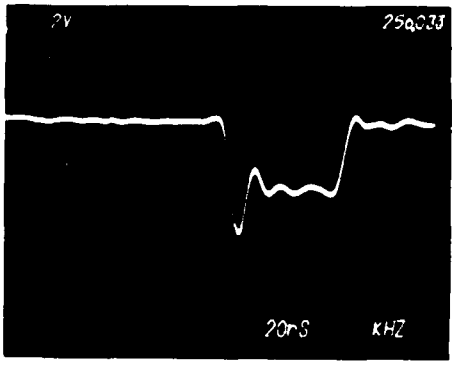


Figure 27. Test Point J1-24

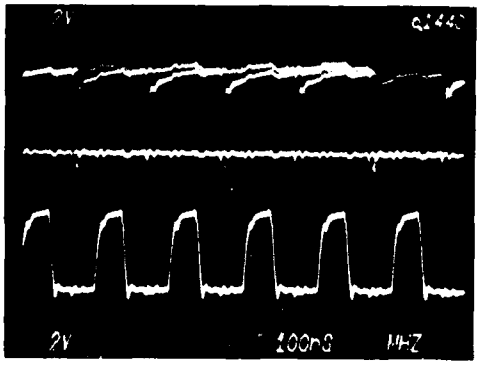


Figure 28. J1-9/J1-3 Relationship

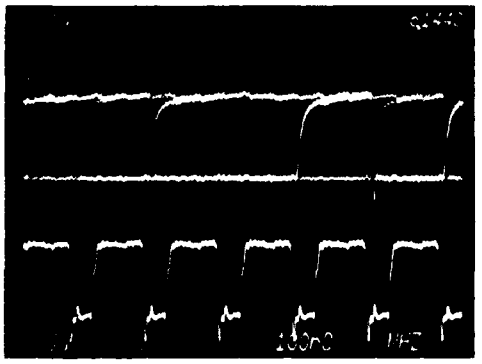


Figure 29. J1-5/J1-15 Relationship

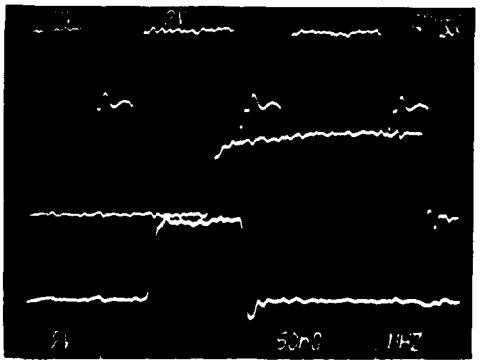


Figure 30. J1-15/J1-16/J1-2 Relationship

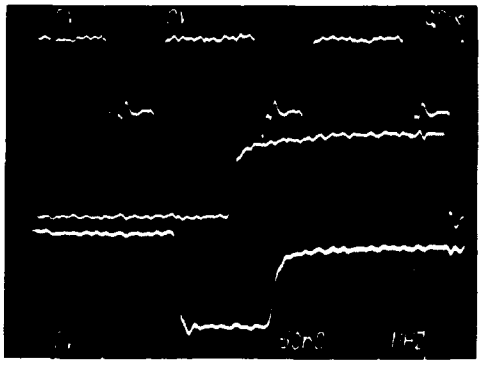


Figure 31. J1-15/J1-16/J1-17 Relationship

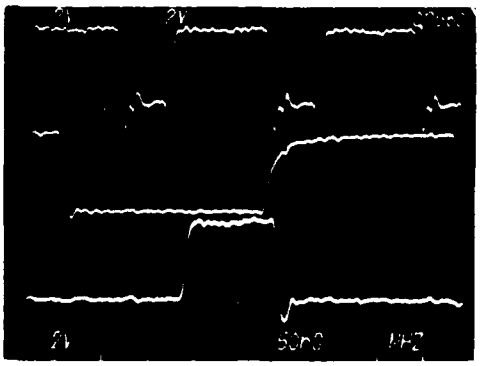


Figure 32. J1-15/J1-14/J1-2 Relationship

27. J1-15/J1-14/J1-2 relationship

Figure 32 shows J1-15 as the top trace, J1-14 in the middle, and J1-2 the bottom. J1-15 is a 6144 kHz clock, J1-14 is a 2304 kHz clock, and J1-1 is a logic 1 pulse with a repetition rate of 256 kHz. The positive edge of J1-14 (middle) occurs during the time J1-2 (bottom) is at the logic 1 level. The positive edges of J1-15 (top) must be at least 30 nanoseconds removed from the positive edge of J1-14 (middle).

28. J1-15/J1-14/J1-17 relationship

Figure 33 shows J1-15 as the top trace, J1-14 in the middle, and J1-17 on the bottom. J1-15 is a 6144 kHz clock, J1-14 is a 2304 kHz clock, and J1-17 is a logic 0 pulse with a repetition rate of 256 kHz. The positive edge of J1-14 (middle) occurs during the time J1-17 (bottom) is at the logic 0 level. The positive edges of J1-15 (top) must be at least 20 nanoseconds removed from the positive edge of J1-14 (middle).

29. J1-8/J1-1 relationship

Figure 34 shows J1-8 as the top trace and J1-1 as the bottom. J1-8 is internal data derived from FODATARCV, and J1-1 is a logic 0 pulse occurring at a repetition rate of 256 kHz. The positive edge of J1-1 (bottom) occurs inside a single data cell (top); the data cell in figure 33 is a logic 1 level with logic 0 levels on both sides. The positive edge of J1-1 (bottom) must occur at least 15 nanoseconds after the left-hand edge of the data cell, and at least 5 nanoseconds before the right-hand edge of the data cell.

30. J1-7/J1-6 relationship

Figure 35 shows J1-7 on the top trace and J1-6 on the bottom. J1-7 is a 32 kHz square wave and J1-6 is a logic 0 pulse with a repetition rate of 256 kHz. The positive edge of J1-6 (bottom) must occur at least 5 nanoseconds before the right-hand edge of J1-6 (top).

31. Group 1 data/group 1 clock output

Figure 36 shows the group 1 data output (CCA pins 7, 57) on the top trace, and the 2048 kHz group clock (CCA pin 21) on the bottom. The positive edges of the clock (bottom)

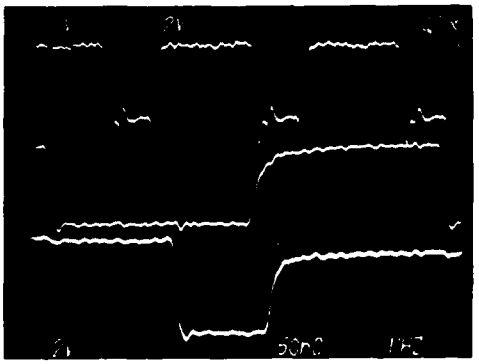


Figure 33. J1-15/J1-14/J1-17 Relationship

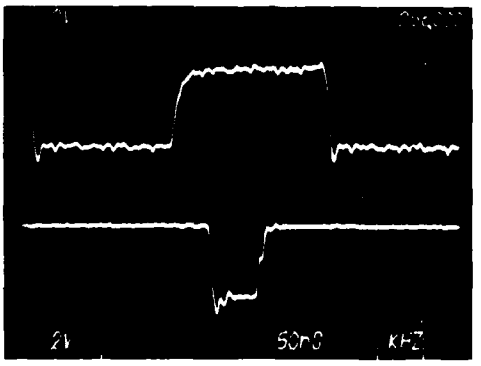


Figure 34. J1-8/J1-1 Relationship

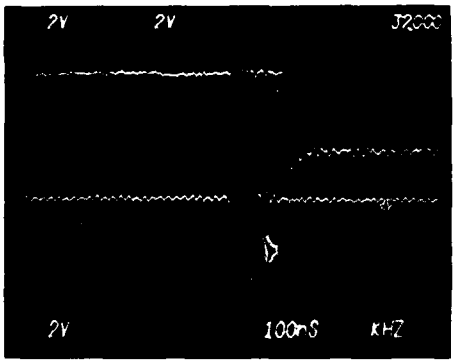


Figure 35. J1-7/J1-6 Relationship

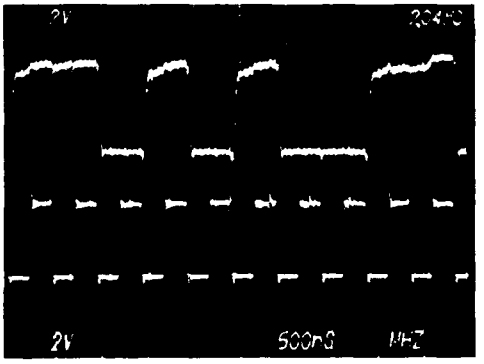


Figure 36. Group 1 Data/Clock Output

are approximately centered in each data cell (top). The group 1 data shown in figure 36 is the repeating sequence "11010100."

32. Group 2 data/group 2 clock output

Figure 37 shows the group 2 data output (CCA pins 8, 58) on the top trace, and the 2304 kHz group 2 clock (CCA pins 19, 69) on the bottom. The positive edges of the clock signal (bottom) shall be approximately centered in each data cell (top). The group 2 data shown in figure 37 is the repeating sequence "11010100."

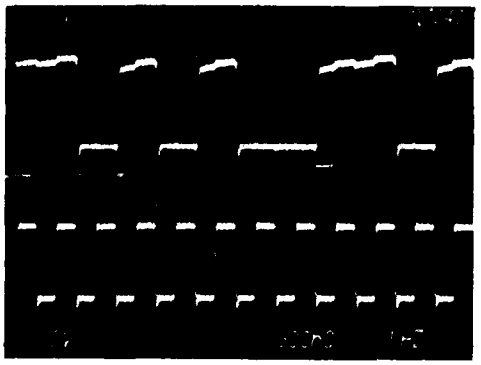


Figure 37. Group 2 Data/Clock Output

33. FRAMESYNC output

The FRAMESYNC output (CCA pin 71) is connected to a 2800 ohm, pull-up resistor. The logic level measured at FRAMESYNC should be a steady logic 0.

4.2 GROUP CLOCK 1536 kHz

To ensure the 1536 kHz group clock is performing properly, change the two signal inputs specified in table 7. These are MSEL1B (CCA pins 36, 86) and MSEL1C (CCA pins 33, 83). Change MSEL1B from the logic 1 level specified in table 2 to a logic 0 level. Change MSEL1C from the logic 0 level specified in table 7 to a logic 1 level. The output signal at J1-16 is now a 1536 kHz square wave.

4.3 32KHZDMUX OUTPUT

To ensure the 32KHZDMUX output (CCA pins 31, 81) is performing properly, connect it to a 133 ohm pull-up resistor. The signal waveform measured at the 32KHZDMUX output is a 32 kHz square wave. Stimulus signals specified in table 7 and figures 5 and 6 apply.

4.4 AUXILIARY TRAFFIC PERFORMANCE

Auxiliary traffic performance will be specified with simulated traffic on group 1 and group 2; the group 1 and 2 traffic rates will be 2048 and 2304 kb/s, respectively.

4.4.1 Auxiliary Traffic Stimulus

The input stimulus signals for auxiliary traffic are specified in table 7 and figures 5 and 6.

4.4.2 Auxiliary Traffic Response

The auxiliary traffic response is specified in table 8. Table 8 specifications are obtained with a 133 ohm, pull-up resistor connected to each pair of CCA pins listed.

Table 8

Auxiliary Traffic Response

Name	CCA Pins	Specification
CH1XMT	15, 65	Logic 0
CH2XMT	16, 66	Logic 1
CH3XMT	14, 64	Logic 0
CH4XMT	13, 63	Logic 1
CH5XMT	11, 61	Logic 0
CH6XMT	12, 62	Logic 1
CH7XMT	17, 67	Logic 0
CH8XMT	18, 68	Logic 1
CH9XMT	9, 59	Logic 0
CH10XMT	10, 60	Logic 1
CH11XMT	43, 93	Logic 0
CH12XMT	42, 92	Logic 1

To ensure the TEL1XMT (CCA pin 26, 76) and TEL2XMT (CCA pins 27, 77) meet requirements, change the two signal inputs specified in table 7. These are CH11CONT (CCA pins 30, 80) and CH12CONT (CCA pins 29, 79). Change both from the logic 0 levels specified in table 7 to logic 1. Simply disconnecting the wires to CH11CONT and CH12CONT would be sufficient, since pull-up resistors on the CCA will then be able to pull them up to a logic 1 level.

Under these conditions, with a 133 ohm pull-up resistor connected to TEL1XMT and TEL2XMT outputs, TEL1XMT is a logic 0 and TEL2XMT, a logic 1.

4.5 SINGLE GROUP PERFORMANCE

Single group performance will be specified with simulated traffic on group 1 only. The group 1 data rate will be 4608 kb/s.

4.5.1 Single Group Stimulus

The input stimulus signals for single group traffic are specified in table 9 and figures 38 and 39. Table 9 specifies both the static and dynamic input signals that should be applied to the demultiplexer CCA to ascertain that performance requirements are being met. Figure 38 specifies the 6144 kb/s COAX3RCV signal in greater detail, and figure 39 shows the phase relationship that exists between COAX3RCV and 6144CLK.

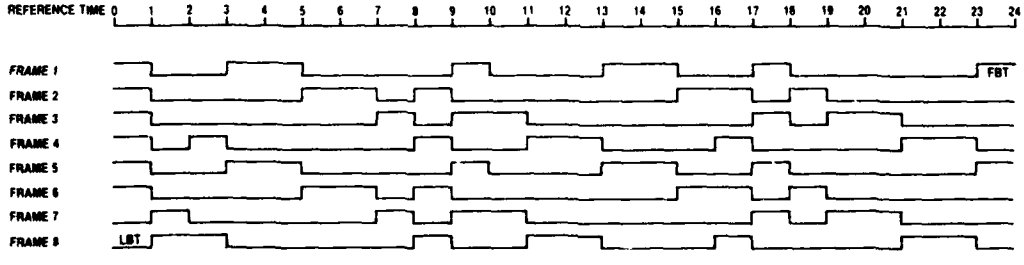


Figure 38. COAX3RCV Single Group Stimulus

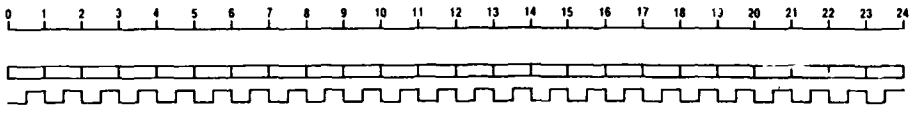


Figure 39. COAX3RCV/6144CLK Phase Relationship

Table 9. Single Group Stimulus Signals

Name	CCA Pins	Specification
+5V	1,2,49,50,51,52,99,100	+5 V dc power input
GND	3,4,47,48,53,54,97,98	+5 V, +12 V, -12 V Return
+12V	37,38,87,88	+12 V dc power input
-12V	34,35,84,85	-12 V dc power input
COAX3FOSEL	45,95	Logic 1
COAX3RCV	46,96	Figures 38 and 39
MSEL2D	39,89	Logic 0
MSEL2C	40,90	Logic 0
MSEL2B	41,91	Logic 1
MSEL2A	25,75	Logic 1
MSEL1D	32,82	Logic 0
MSEL1C	33,83	Logic 0
MSEL1B	36,86	Logic 0
MSEL1A	28,78	Logic 0
6144CLK	5,55	See figure 38
FODATARCV	6,56	Connect to COAX3RCV

4.5.2 Single Group Response

Single group performance is specified by stating the output response that must be exhibited by the demultiplexer CCA being stimulated. Failure to conform to the stated response requirements constitutes unacceptable performance. The amplitude of the response output signals must meet the requirements for TTL.

4.5.2.1 J1-16/J1-14 Response

J1-16 normally exhibits the group 1 clock, while J1-14 exhibits the group 2 clock; however, when the demultiplexer CCA is operating in the single group mode, both of these test points exhibit the same clock signal. For the stimulus signals specified in table 9, both J1-16 and J1-14 exhibit a 4608 kHz square wave.

4.5.2.2 GR2DATAA/GR1DATAA Response

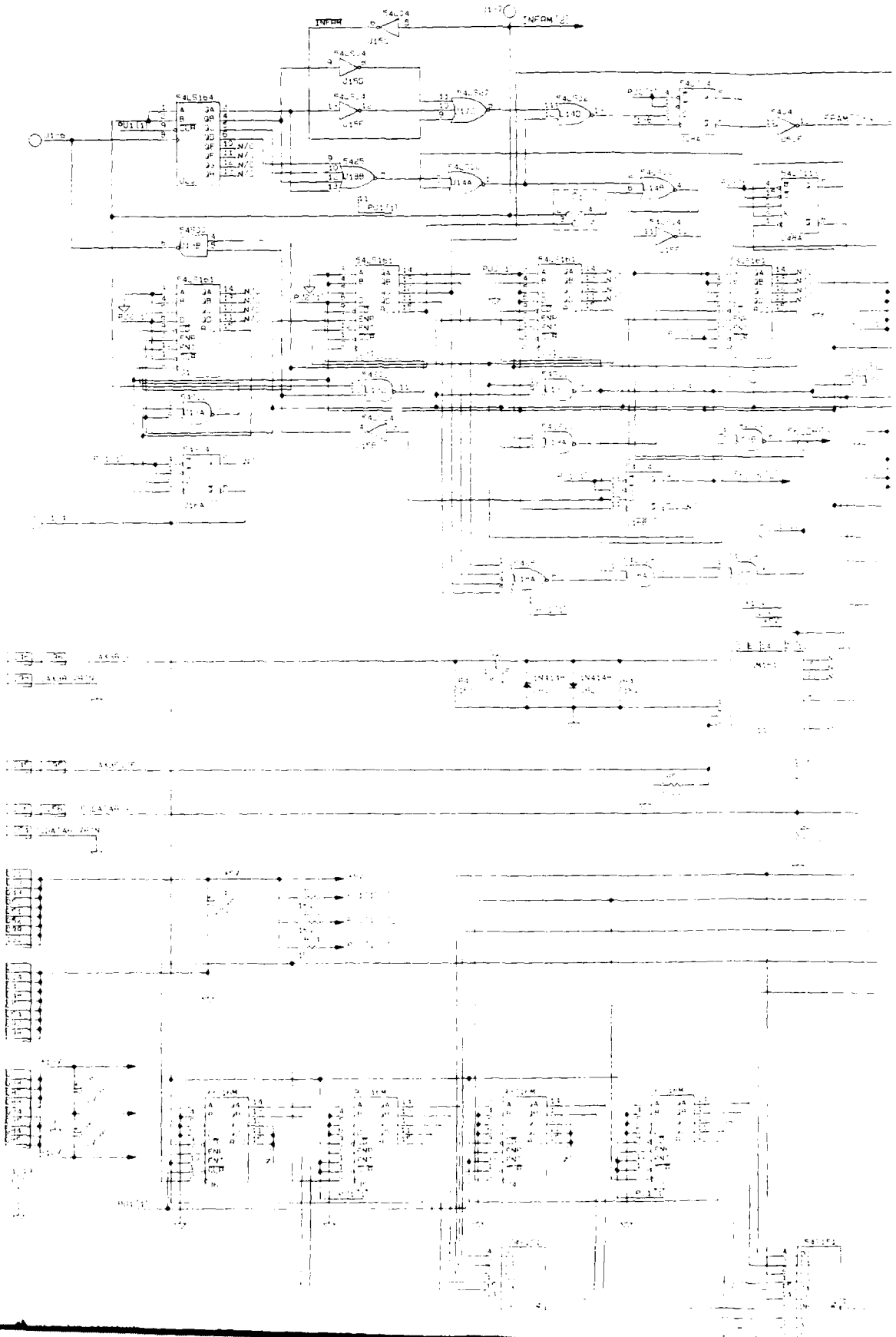
GR2DATAA (CCA pins 8, 58) and GR1DATAA (CCA pins 7, 57) must both exhibit an identical data output pattern; a slight difference in phase between the two is acceptable, but both data rates should be 4608 kb/s. Both pairs of CCA pins are connected to an 18000 ohm pull-up resistor before the responses are measured.

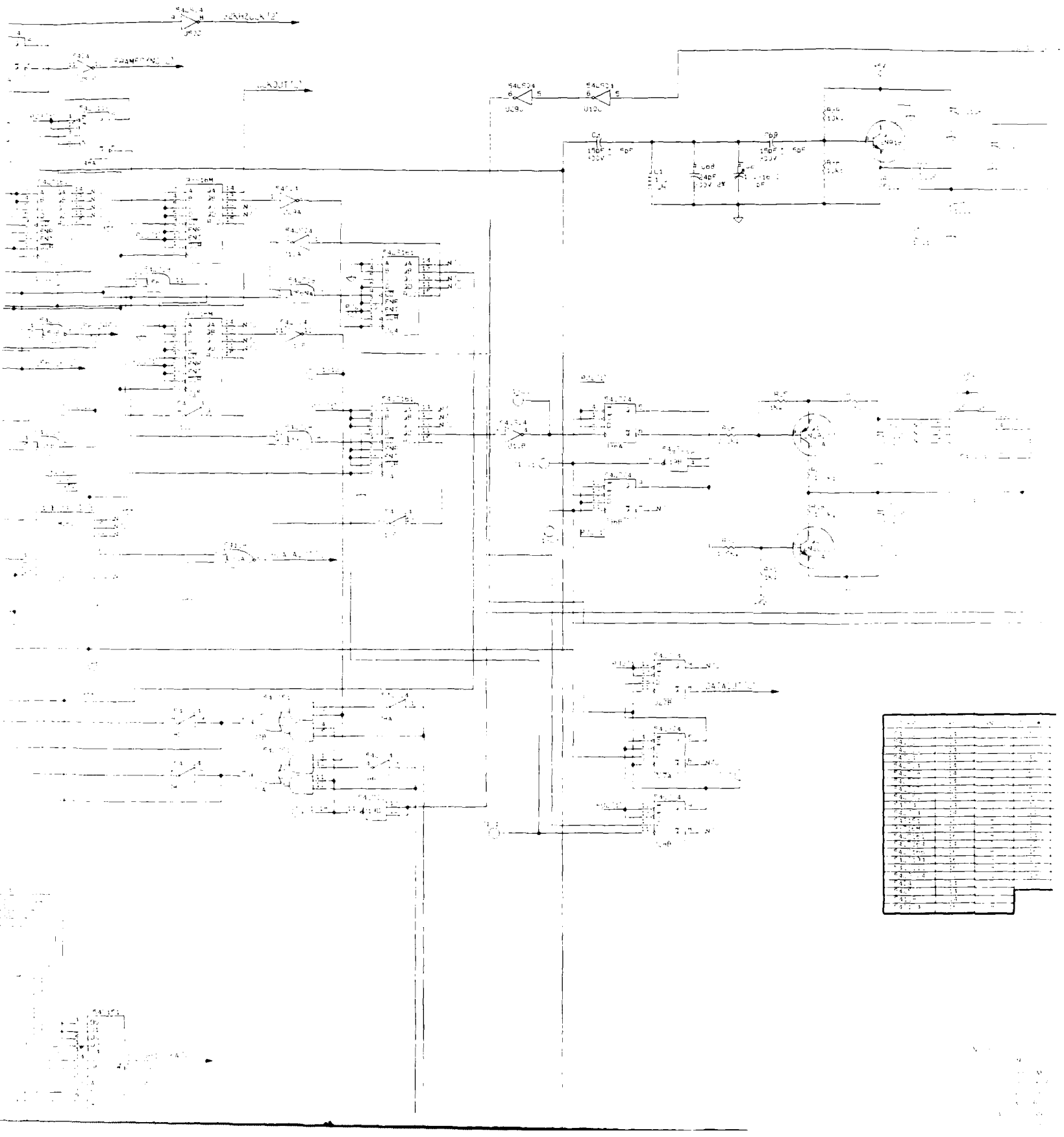
4.5.2.3 RDATAOUT Response

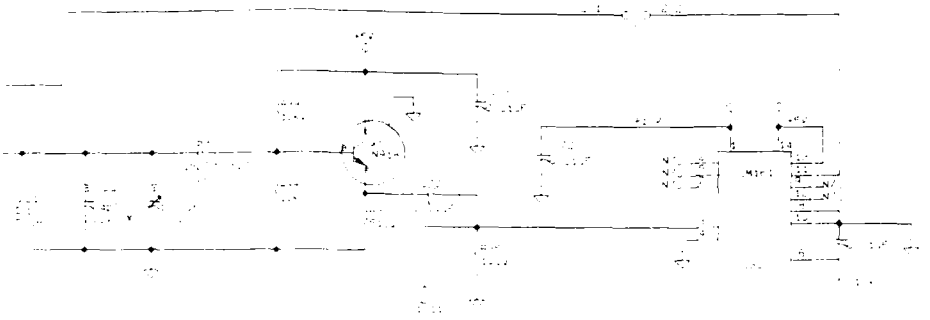
RDATAOUT (CCA pins 44,94) are connected to a 133 ohm pull-up resistor. The response at RDATAOUT is a delayed copy of the stimulus signal COAX3RCV specified in figure 38.

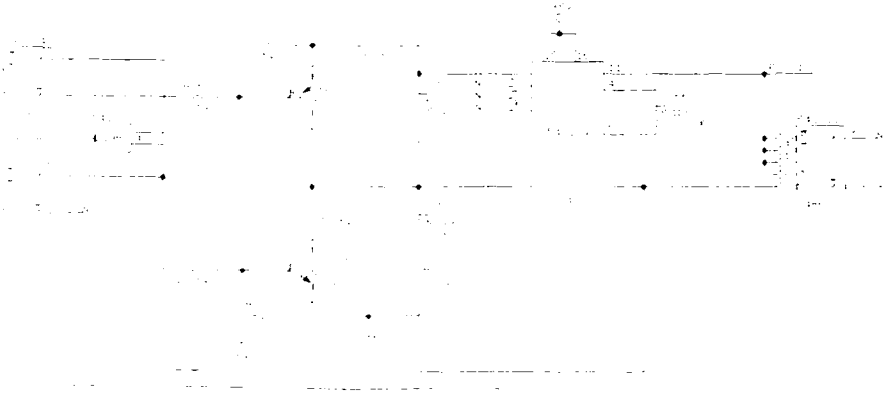
APPENDIX A

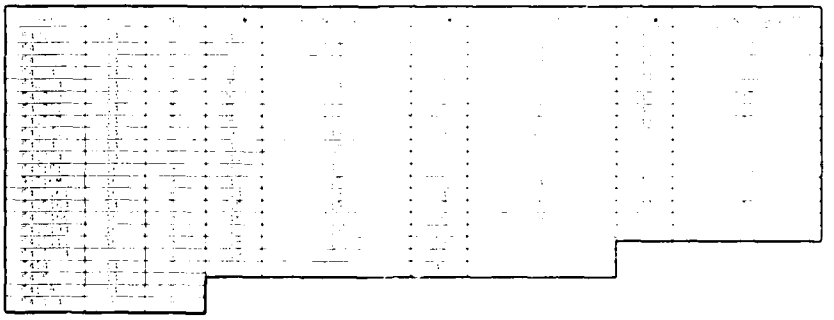
DEMULTIPLEXER SCHEMATIC

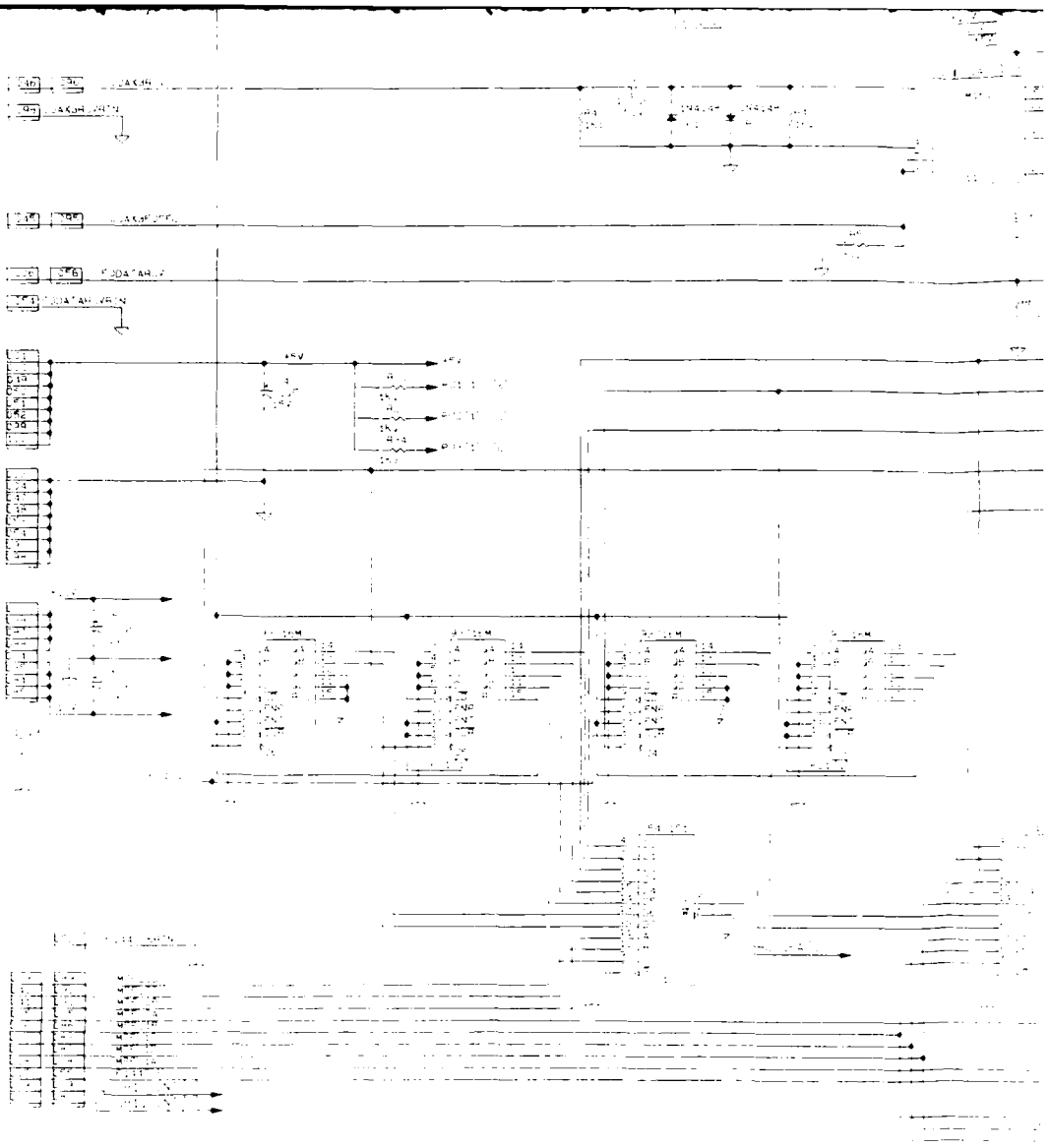


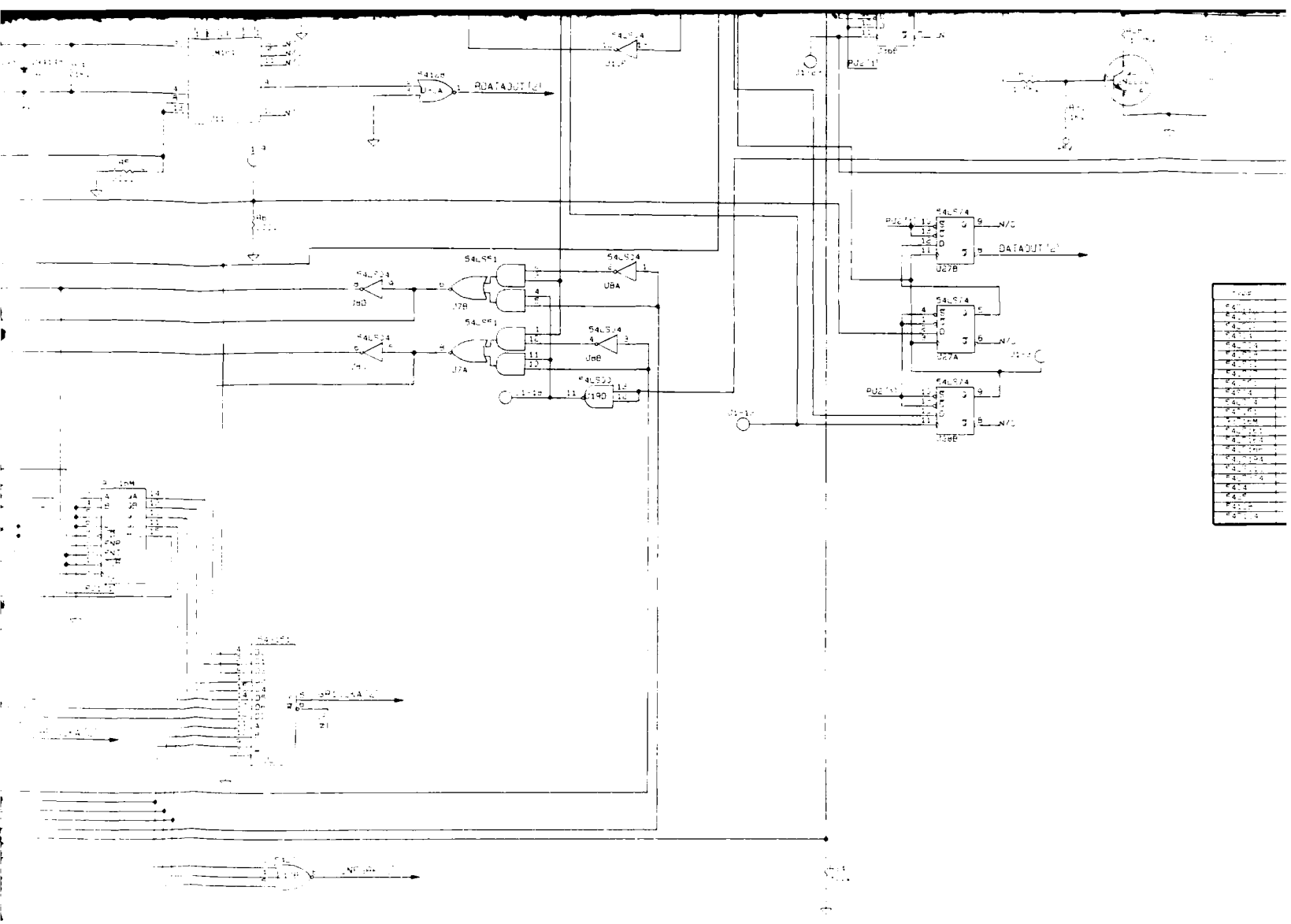


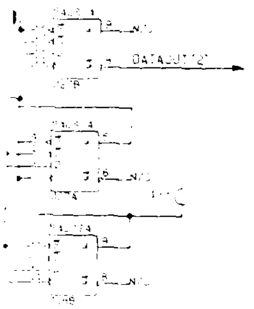


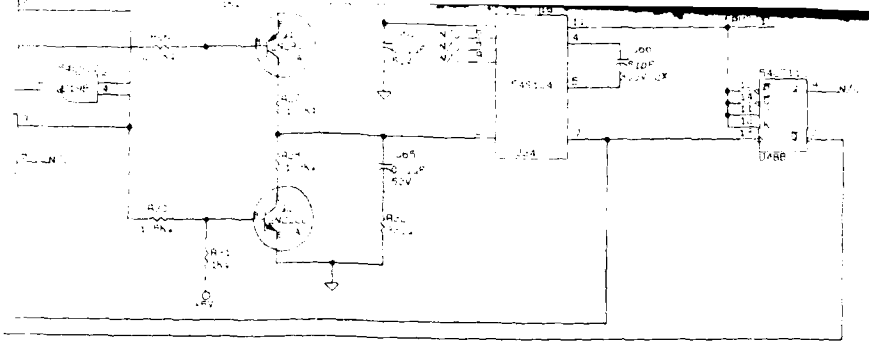







DATAOUT(2)
DATAOUT(1)
54LS74
54LS51
54LS04
54LS22
54LS00
N/C



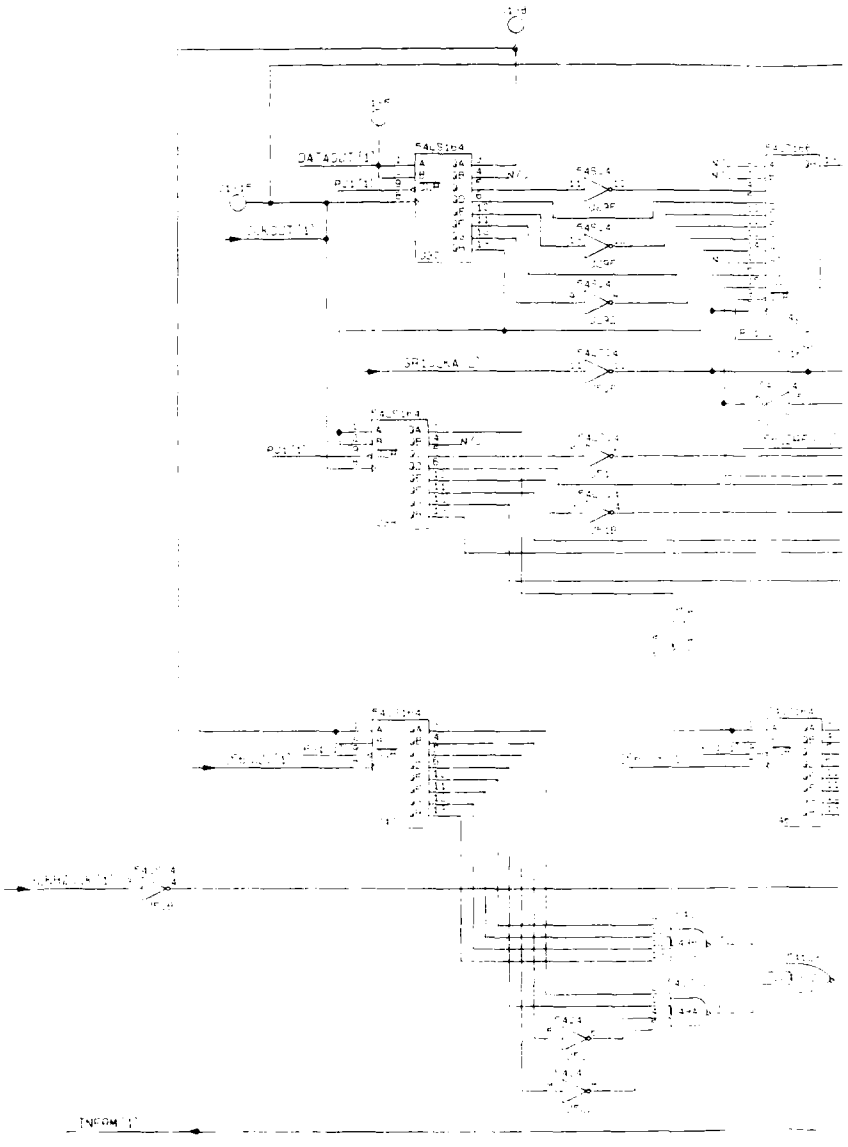


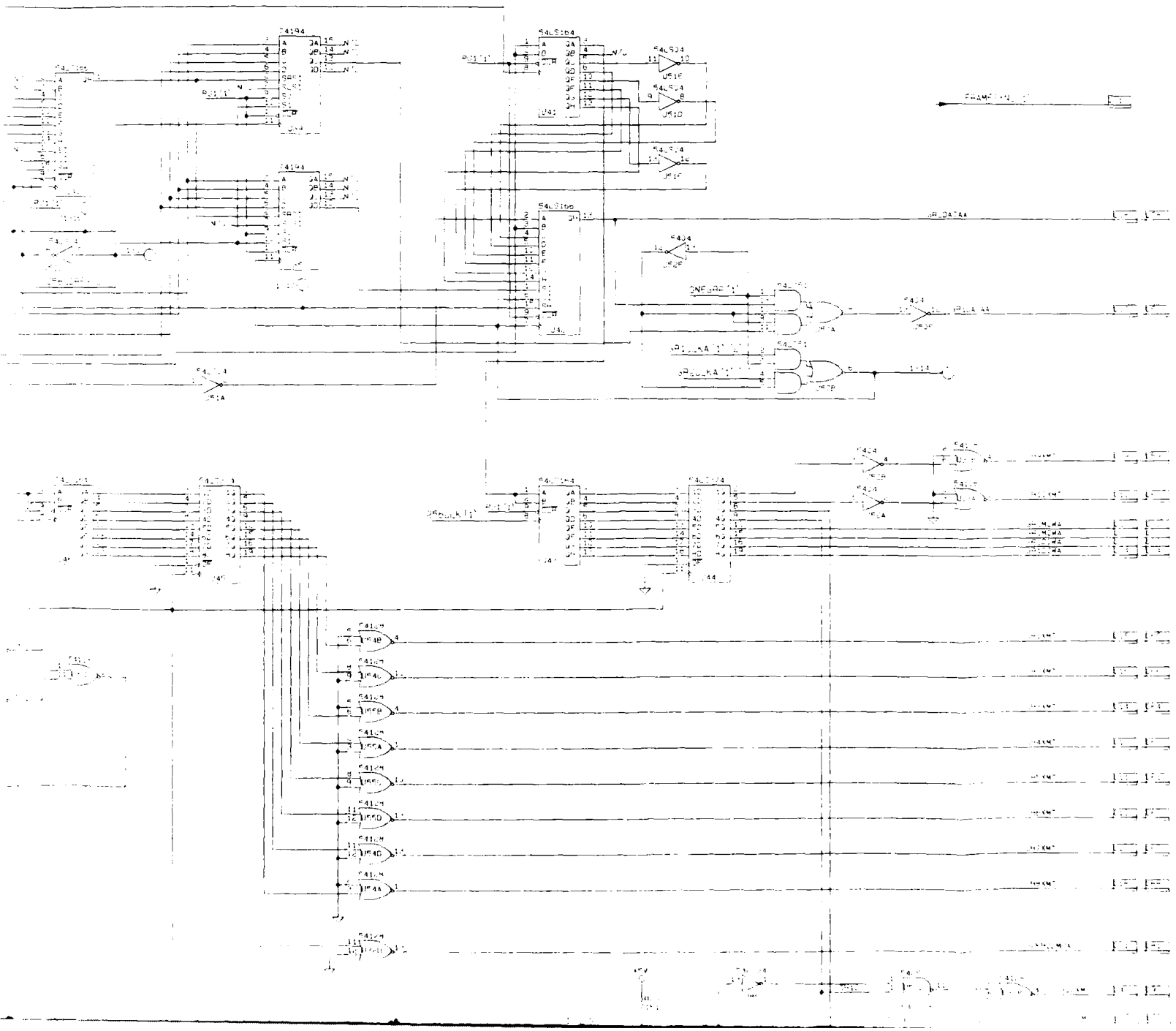
TYPE	+5	GND	IC #	DECOUPLING CAPACITOR	IC #	DECOUPLING CAPACITOR	IC #	DECOUPLING CAPACITOR
54S00	14	7	U1	C16	U21	[illegible]	U41	[illegible]
54LS00	14	7	U2	[illegible]	U22	[illegible]	U42	[illegible]
54LS02	14	7	U3	[illegible]	U23	C29	U43	[illegible]
54S01	14	7	U4	C24	U24	C48	U44	[illegible]
54LS04	14	7	U5	C14	U25	C47	U45	[illegible]
54LS08	14	7	U6	[illegible]	U26	[illegible]	U46	[illegible]
54LS20	14	7	U7	[illegible]	U27	[illegible]	U47	[illegible]
54LS27	14	7	U8	[illegible]	U28	[illegible]	U48	[illegible]
54LS51	14	7	U9	C49	U29	C41	U49	[illegible]
5474	14	7	U10	C55	U30	C40	U50	[illegible]
54LS74	14	7	U11	[illegible]	U31	[illegible]	U51	[illegible]
54S151	16	8	U12	[illegible]	U32	C11	U52	[illegible]
93S16	16	8	U13	C17	U33	C64	U53	[illegible]
54LS161	16	8	U14	C28	U34	[illegible]	U54	C46
54LS164	14	7	U15	C19	U35	[illegible]	U55	[illegible]
54LS166	16	8	U16	C21	U36	[illegible]	U56	[illegible]
54LS194	16	8	U17	[illegible]	U37	[illegible]	U57	[illegible]
54LS11	16	8	U18	[illegible]	U38	[illegible]		
54LS374	20	10	U19	[illegible]	U39	[illegible]		
5404	14	7	U20	[illegible]	U40	[illegible]		
5425	14	7						
54109	14	7						
54S124	16	8						

NOTES:

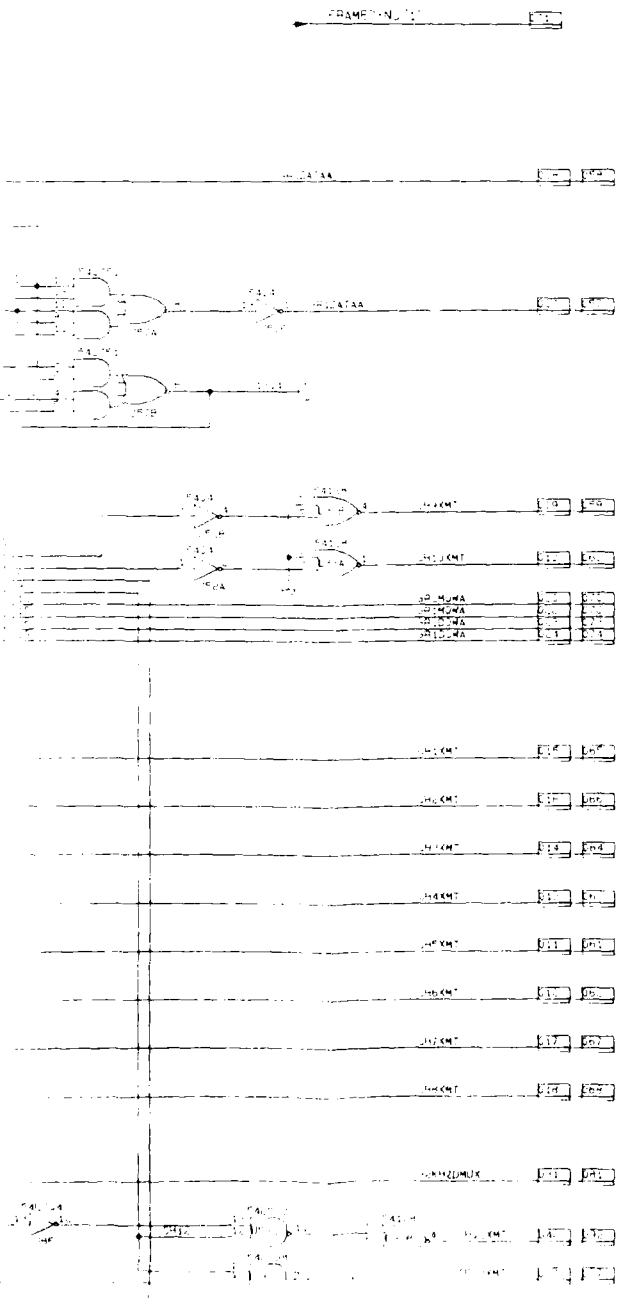
1. UNLESS OTHERWISE SPECIFIED CAPACITORS ARE IN UF, 100V, 10%.
2. SEE TABLES FOR VCC AND GND CONNECTIONS AND DECOUPLING CAPACITORS. DECOUPLE POWER SUPPLY VOLTAGES WITH A .1 UFD 100WVDC CAPACITOR BETWEEN VCC (+5VOLTAGE) AND COMMON FOR EACH IC. ALL RESISTORS ARE IN OHMS, 1/4W, 5%.
3. [illegible] AND R46 ARE THE LAST DESIGNATED COMPONENT.
4. [illegible] PINS NOT SHOWN ARE NO CONNECTION.
5. MINI [illegible] CONNECTOR [illegible]

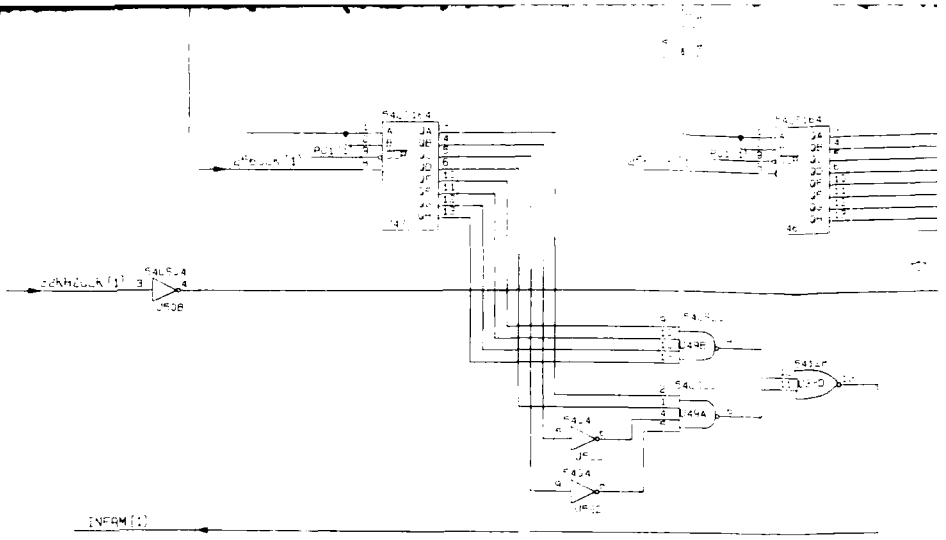
DRAFTER	DATE	MITRE CORP. BEDFORD, MA
CHECKED		TITLE: DEMULTIPLEXER
ENGINEER		
RELEASE		E — DRAWING NUMBER 84-R3364 1
PROJ		NEXT ASSEMBLY 84-[illegible]
FILE PKG		SHEET [illegible] OF [illegible]

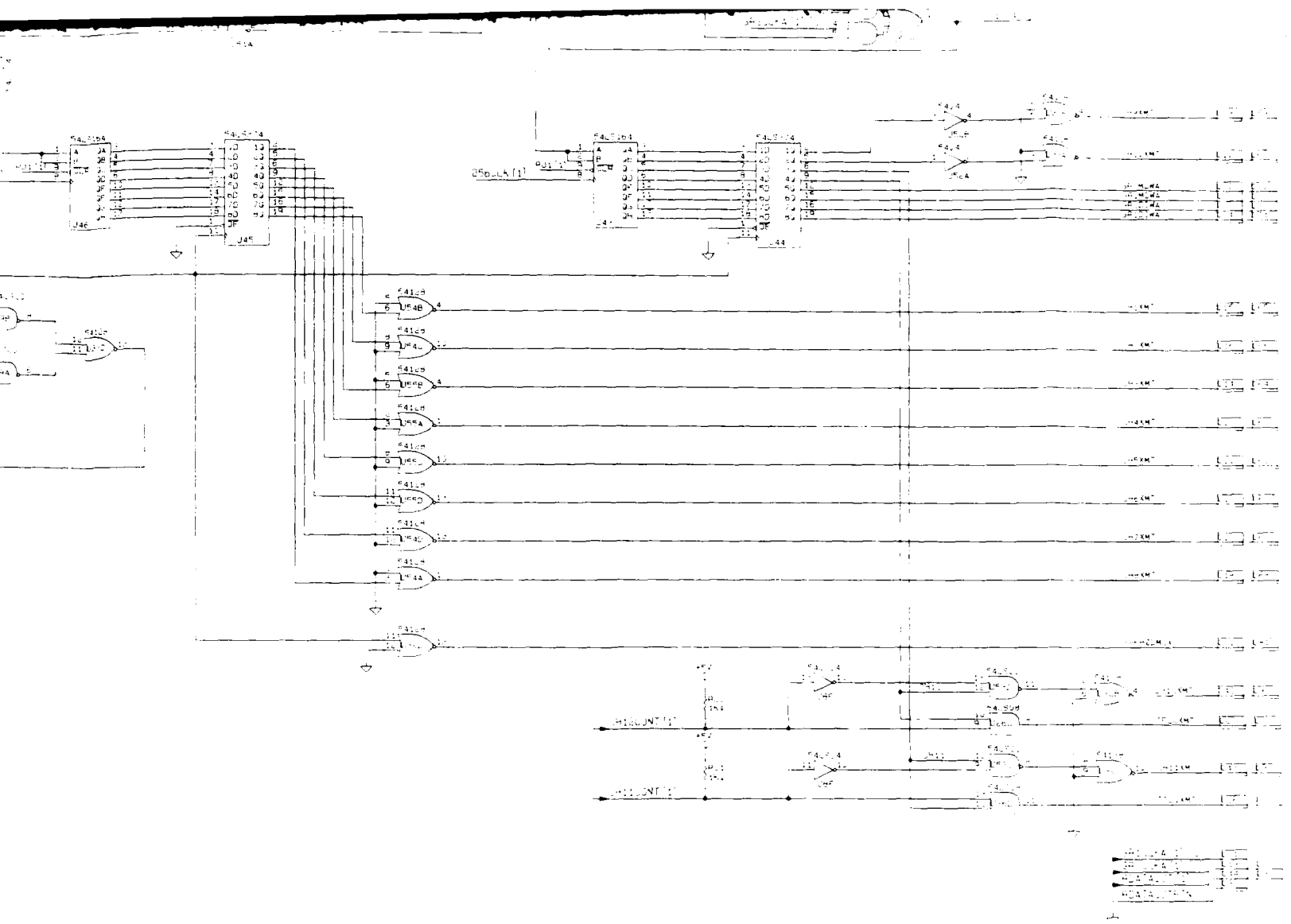


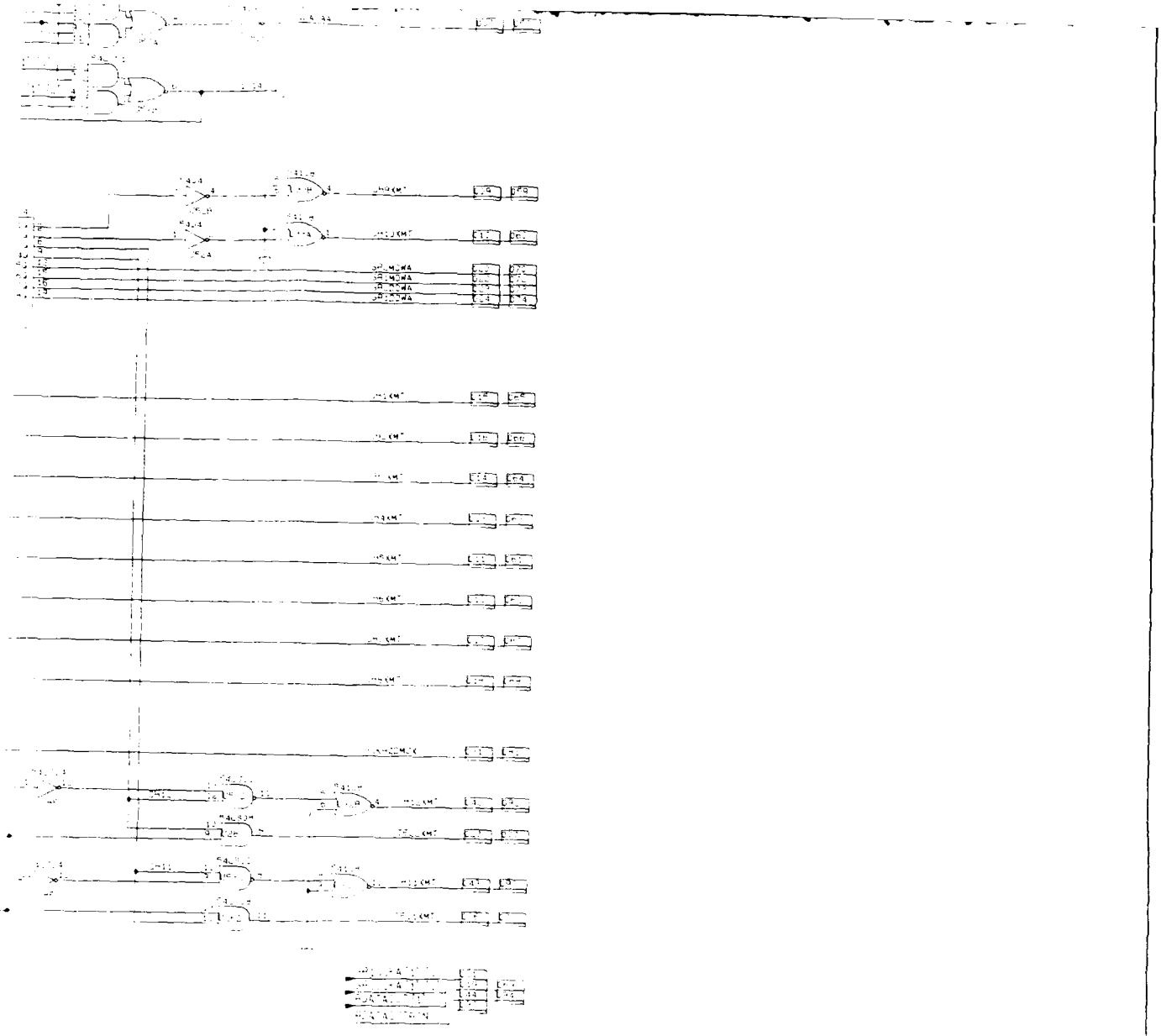


REV	DATE	
A	4/29	CHANGE PER ECN # TAC-1-004









APPENDIX B

DEMULTIPLEXER (A1A1) ALIGNMENT PROCEDURE

1. Provide the following signal inputs to the demultiplexer board being aligned:

Signal Name	Connector Pin(s)	Specification
+5V	1,2,49,50,51,99,100	+5 V dc +/- 0.25 V
GND	3,4,47,48,53,54,97,98	+5 V dc return
6144CLK	5,55	6144 kHz TTL square wave
6144CLKRTN	53	6144 kHz return

2. Connect an ac coupled oscilloscope to J1-11. Adjust the trimmer capacitor C2 until the time between two adjacent positive edges of the waveform is approximately 54 nanoseconds. This corresponds to a frequency of 18432 kHz.

3. Rotate the trimmer slightly to peak the amplitude of the waveform at J1-11.

GLOSSARY

A	ampere
Ā or *A	A's complement
ac	alternating current
ATE	automatic test equipment
AUX	auxiliary
b/s	bits per second
°C	degrees Celsius
CCA	circuit card assembly
CH	channel
CH11XMT	channel (number) transmit
CLK	clock
COAX 1, 2, or 3	coaxial cable 1, 2, or 3
COAX3FOSEL	coaxial (number) fiber optic select (input)
COAX3RCV	coaxial cable 3 receive
CVSD	continuously variable slope delta (modulation)
dc	direct current
demux	demultiplexer
ECCP	edge-card connector pin
FBT	first bit transmitted
FO	fiber optic
FODATARCV	fiber optic data receive (input signal)
GR1(2)CLKA	group 1 or 2 clock A
GR1(2)DATAA	group 1 or 2 data A output of the 18 bit register
GR1(2)MOWA	group 1 or 2 signal conditioner orderwire A
H	high power fiber optics (switch position)
Hz	hertz
IC	integrated circuit
I/O	input/output
kb/s	kilobits per second
kHz	kilohertz
32KHZMUX	32 kHz multiplexer (clock)
32KHZDMUX	32 kHz demultiplexer (clock)

GLOSSARY (Concluded)

L	low power fiber optics (switch position)
LBT	last bit transmitted
mA	milliamperes
mm	millimeter
MSEL1A (B, C, or D)	outputs of the leftmost thumbwheel switch
MSEL2A (B, C, D)	outputs of the rightmost thumbwheel switch
mV	millivolts
$\bar{Q}$ or *Q	Q's complement
RCO	ripple carry output
RDATAOUT	read data out
s	seconds
T	time
TEL	telephone
TEL1(2)XMT	telephone 1 (or 2) transmitter (names of signal paths)
TSSR	tropo satellite support radio
TTL	transistor-transistor logic
USA	United States Army
USAF	United States Air Force
V	volts
VCO	voltage-controlled oscillator
VHF	very high frequency
W	watts