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ABSTRACT

Superconductor-Insulator-Superconductor (SIS) tunnel junction mixers are known to provide ultra-high sensitivity in receiver applications above 30 GHz. In this two year (Phase II) program, HYPRES, in collaboration with the National Radio Astronomy Observatory, have developed novel fully integrated SIS mixer circuits, and demonstrated a unique high efficiency cooling system. The integrated SIS mixer chip contains, aside from the actual mixer elements, passive tuning components, an IF filter, a coplanar transmission line, and a waveguide coupler, necessary components heretofore realized off-chip. Fabrication of the integrated mixer required development of a nine level process and optimization of the process dependent electrical parameters of the SIS devices. The device performs efficiently in the range of 75-115 GHz. A novel dewar-based cooler, which makes use of the extremely low thermal conductivity of the fused silica chip substrate to achieve an incremental thermal load of 25 mW, was fabricated and demonstrated. Such a cryostat allows relatively long term unattended operation of SIS, or other, cryogenic devices.

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MM WAVECOMPONENTS - SIS MIXERS FINAL REPORT

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ABSTRACT

Superconductor-Insulator-Superconductor (SIS) tunnel junction mixers are known to provide ultra-high sensitivity in receiver applications above 30 GHz. In this two year (Phase II) program, HYPRES, in collaboration with the National Radio Astronomy Observatory, have developed novel fully integrated SIS mixer circuits, and demonstrated a unique high efficiency cooling system. The integrated SIS mixer chip contains, aside from the actual mixer elements, passive tuning components, an IF filter, a coplanar transmission line, and a waveguide coupler, necessary components heretofore realized off-chip. Fabrication of the integrated mixer required development of a nine level process and optimization of the process dependent electrical parameters of the SIS devices. The device performs efficiently in the range of 75-115 GHz. A novel dewar-based cooler, which makes use of the extremely low thermal conductivity of the fused silica chip substrate to achieve an incremental thermal load of 25 mW, was fabricated and demonstrated. Such a cryostat allows relatively long term unattended operation of SIS, or other, cryogenic devices.

MM WAVE COMPONENTS - SIS MIXERS FINAL REPORT

I. INTRODUCTION AND SUMMARY

By now it is well known that Superconductor-Insulator-Superconductor (SIS) tunnel junction mixers can provide superior noise temperature in receiver applications at frequencies above about 30 GHz. The fact that these devices can approach quantum limited performance has stimulated a great deal of interest in the radio astronomy community and SIS receivers are now in use at several facilities. HYPRES, in collaboration with the National Radio Astronomy Observatory (NRAO), have contributed to the advancement of this technology under the present program, by development of new SIS structures and cryogenics, as will be described in this report. HYPRES SIS devices have been employed in 115 GHz receivers, which functioned reliably in the course of actual utilization in the field.

Although simple in concept, like many high frequency devices SIS mixers are often difficult to fabricate. This is not only due to the small feature sizes, but to the uncertainty in the values and accuracy required of related passive circuit elements. HYPRES has developed an all-niobium processing technology suitable for small scale circuits, and have purchased or developed advanced CAD equipment and software. The goal of this program for HYPRES was to successfully bring this technology to bear on SIS mixer chip fabrication. The HYPRES process allows complicated multi-level device structures to be fabricated, and the CAD equipment allows many different chip designs, in this case about 100, each perhaps differing from the others by a slight change in the value of a particular inductance, to be arrayed on the same wafer. Each 3" wafer contains around 20,000 SIS mixers chips, thus the parameter spread virtually assures a yield of near optimum chips. HYPRES was the first to bring this type of CAD technology into SIS mixer fabrication. HYPRES intends to make available the expertise gained under this program to anyone interested in SIS mixers, either by supplying generic mixer components, or by custom design and fabrication. It is hoped that the availability of this service, at a reasonable price, will stimulate the proliferation of SIS receivers in radio astronomy, and perhaps open other application areas.

In addition to the main thrust of development and fabrication of SIS mixer chips, under this program a novel cryostat design was explored. One of HYPRES' proudest achievements was the invention and patenting of the spray cooling technique, used in the company's instrument products. With this technique, a jet of liquid helium is directed toward the corner of a fused silica substrate which contains superconducting circuitry. Due to the very low thermal conductivity of the substrate, one corner of the chip can be maintained at 4K in this manner, while the remainder of the chip is at room temperature. This facilitates wide bandwidth interconnections between the cryogenic and room temperature environments as the physical separation is less than 1 cm.

The spray cooling technique, although it has many desirable features, does consume helium at a rate faster than preferred for long term continuous operation. Under the present program, HYPRES investigated a dewar-based cooler, where one end of a long narrow chip, which contained an SIS mixer, was cooled, while the other end of the chip, maintained at room temperature, allowed electrical access to the mixer. The heat input was substantially limited to the thermal conduction through the substrate.

The following paragraphs summarize the work that was done under Phase II of the present contract, and the results obtained. This work will be described in detail in the later sections of this report.

1. In conjunction with A. R. Kerr and S. K. Pan of NRAO, four different SIS mixer cells were designed, and a mask set containing parameter variations of these four cells was produced. The four basic designs consisted of NRAO designed 5 x 10 mil mixer chips for 115 and 230 GHz, for use in their standard mixer mount, a NRAO designed integrated mixer chip for use in a mixer block designed under this program, and a HYPRES designed mixer chip for operation in a novel dewar-based cooling system.

2. The new chip designs required processing steps not previously required at HYPRES, and much process development effort was required. Three levels of the mask set were modified to facilitate processing at a particularly difficult step. In the end, these devices remain difficult to fabricate, as certain steps have very narrow processing margins. A lift-off junction fabrication process was developed, which has much lower parasitic capacitance than the anodization process previously employed. This process improves high frequency mixer performance, and is now widely used in many applications at HYPRES. It is necessary, for example, in NbN processing, as NbN does not anodize successfully.

3. RF evaluation of the mixers was carried out at NRAO, Charlottesville, VA. Results were among the best ever recorded for all-niobium SIS devices, and constitute the first performance measurements of a fully integrated (includes additional passive components) SIS mixer.

4. A Janis cryostat was modified to allow "poke through" cooling, whereby one end of the chip is cooled, the chip "pokes through" the radiation shield, and is bonded to the back of a (vacuum tight) wide bandwidth connector. The connector chosen was the widest bandwidth coaxial connector available at the time, and is also widely used in HYPRES instruments. The circuit area was cooled by contact to a flexible copper braid, which in turn was in thermal contact to the dewar cold finger 0.5 cm away. Although funds were exhausted before the performance of the cooler was entirely satisfactory, cooling of the chip to 6K was observed, with a boil-off rate differential indicating that about 25 milliwatts heat load was incurred by the chip and related parts.

II. SIS MIXER CHIP DESIGN

In order to achieve mixer dynamic range adequate for general purpose radio astronomy applications, multiple SIS junctions are employed. Although theoretically the dynamic range should scale as n^2, and the noise floor should be independent of n, small imbalances between the junctions could cause this potential not to be realized. In order to study the advantages of multiple junctions, mixers composed of 2-10 junctions were included.

One of the more interesting aspects of the designs implemented under this contract came about from the realization that parasitic inductance generally prevents a series array from being tuned collectively, that devices must be tuned individually. At a given signal frequency, the geometric capacitance of an SIS junction produces a susceptance which leads to a large impedance mismatch and reduced performance. In previous SIS mixer implementations which achieved high performance, conjugate matching is provided by mechanically adjustable turning screws in the SIS mixer waveguide coupler. One of the goals of the present program is to avoid the need for external tuning by providing on-chip (inductive) compensation. Previous attempts at on-chip compensation of series arrays failed due to the series inductance of the SIS junction string, which nullified the effect of a parallel compensating inductance placed between the ends of the string. In the present designs, each individual junction is compensated by its own parallel inductance. Although this is electrically advantageous, it requires a more complex fabrication process.

Of great concern is the actual value of the geometric capacitance of the SIS junctions. The compensating inductance must be chosen to resonate with this capacitance at the signal frequency, hence the value of this capacitance is of utmost importance. Measurement of junction capacitance received a great deal of attention during Phase I of this contract. Two different measurement approaches were taken, one involved measuring the Fiske mode spacing in a long junction, the other a direct measurement of the capacitance of a large junction with suppressed critical current by time domain reflectometry, noting the resonant frequency when the junction is paralleled with a known

inductance. Both measurements, as described in the Phase I (New York State SBIR matching funds) report[1], yielded a specific capacitance of 38 fF/μm^2. This value remains somewhat controversial, as Japanese workers publish a value of 60 fF/μm^2 for similar junctions[2]. Nevertheless, the HYPRES value was chosen for the present designs.

Given a well-defined junction capacitance, a suitable shunting inductance is not easy to implement accurately due to lithography variations. In the present design, the inductance is realized by a short (20 micron) length of microstripline over SiO_2 dielectric. The microstrip is terminated by a ¼ wave section of microstrip using Nb_2O_5 dielectric, which provides an RF short while maintaining d.c. isolation. In order to assure that the correct inductance value will appear after a given fabrication run, the length of the microstrip inductor is varied between similar devices over a range of 50%, in 2½ micron steps. Although this limits potential yield, the small chip size allows a huge number of chips to be included on a single wafer (20,000), so that a substantial number of "good" chips are provided by each wafer. Unfortunately, this degree of freedom does not exist for the larger chips, however information obtained from measurements on the smaller chips should narrow the range of variation needed for future designs. Table I summarizes the process dependent electrical parameters used in these designs.

TABLE I

C_j	Junction Capacitance	38 fF/μm^2
λ_L	London Penetration Depth	85 nm
C_d	Nb_2O_5 Capacitance	2.2 fF/μm^2
ϵ_d	Nb_2O_5 Dielectric Constant	29
L_L	3 μm M3 line inductance	.24 pH/μm

As shown in Figure 1, the mask set designed under this program divides the wafer into four quadrants, each populated by a fundamentally different type of chip. Quadrants I and II contain SIS mixer chips compatible with chip mounts in use at NRAO for several years, and are considered the "control" samples. Quadrant III contains the NRAO designed integrated mixer chips, and Quadrant IV the HYPRES-designed chip for a novel dewar-based cooler designed under this program.

a. NRAO Fully Integrated SIS Mixers

In addition to the SIS devices and compensation inductances, very similar to those of the smaller chips, the NRAO-designed fully integrated mixers of Quadrant III include an IF filter and waveguide coupling. The aim was to design a fully integrated SIS mixer with low noise over as much as possible of the 75-115 GHz waveguide band. Its design should be easily integrable with other components, e.g., planar antennas or IF processors, and the mixer requires no adjustable tuning elements.

The high capacitance of SIS junctions requires the use of an integrated tuning circuit if broad bandwidth is desired. At 100 GHz, parasitic inductance in a series array of SIS junctions makes it impractical to use a single tuning inductor for the whole array; rather, each junction has its own tuning circuit[3]. The configuration used in the present mixer is shown in Figure 2. The inductor which tunes out the junction capacitance is a short parallel-plate transmission line. To avoid short circuiting the junctions at DC, a quarter-wave superconducting parallel-plate transmission line stub is used in series with each inductor. The quarter-wave line has an Nb_2O_5 dielectric ($\epsilon_r = 29$) 100 nm thick, formed by anodization. The high dielectric constant combined with the effect of the penetration of the magnetic field into the superconductors ($\lambda = 85$ nm) results in a phase velocity 9.0 times smaller than that of free space. It is thus possible to keep the whole tuning circuit electrically and physically small.

The dynamic range of an SIS mixer with a series array of junctions is proportional to n^2, where n is the number of junctions in the array[4]-[6]. In broadband mixers particular attention must be paid to the possibility of saturation by broadband thermal emitters (e.g., the sun (~ 6000K), or even room temperature loads)[7]. For this reason the mixers described here use arrays of 4 or 8 junctions.

The series array of inductively tuned junctions naturally lends itself to incorporation in a coplanar transmission line circuit. The coplanar configuration is desirable for several reasons:

- All conductors are on the same side of the substrate, which simplifies fabrication and allows the use of thicker, less fragile substrates.
- Characteristic impedances in the range 50-100 ohms can be obtained on a quartz substrate (ϵ_r = 3.8) with reasonable dimensions. This impedance range is suitable for an SIS mixer.
- Because ground currents do not flow in the metal housing which supports the substrate, the circuit is independent of the dimensions of the housing.
- Coplanar lines are easily coupled to other TEM lines -- microstrip or suspended substrate stripline -- which may be used in other parts of a complex integrated subassembly.

The array of inductively tuned SIS junctions is located in a rectangular hole in the ground plane, as shown in Figure 3. The inductance L_h of the hole is tuned out by capacitor C_h in the figure. To the right of C_h a four element low-pass filter connects the junctions to an IF amplifier and a DC bias supply. An IF and DC ground return is required at the left of the mixer; this is provided in the RF input circuit and is not shown in this figure.

The mixers were tested using the suspended substrate stripline to waveguide transition described previously. This requires a coplanar line to suspended stripline transition as shown in Figure 4. The coplanar center conductor tapers sharply out to the full width of the suspended stripline while the gap in the ground plane tapers out to the full width of the substrate. Contact is maintained between the shoulder of the channel and the ground plane in the suspended stripline region by a soft gold wire gasket or by soldering the substrate into the block.

b. Quadrants I, II, and IV Chips

Quadrant I devices are optimized for 115 GHz, and Quadrant II devices for 230 GHz. The small chip size (5 x 10 mils) allows a large number of chips, and therefore great latitude for parameter variation. The layout of these chips is shown in Figure 5. Figure 6 shows the detail of a single mixer device. Variations in junction number of 2, 4, 6 and 8 as well as shunt inductance variation, occur between chips. A dot coding scheme identifies the chips after dicing. Although 3/4 of the wafer and the vast majority of time was spent on mixers designed to operate near 100 GHz, as required for this work, Quadrant II of the wafer was composed of mixers designed for 230 GHz operation. The higher frequency mixers could be compared directly with other similar designs, providing information on circuit parasitics and values not directly attainable at 100 GHz operation. These mixers required 2 micron diameter junctions, where the 100 GHz mixers used more easily fabricated 3 micron junctions.

Quadrant IV contains HYPRES-designed mixer circuits for integration into a cooler to be described. As shown in Figure 7, each mixer consists of a series array of 10 junctions, and the chip contains an IF filter and wide bandwidth coplanar transmission line. The chip was designed to be tuned by use of an ultrasonic cutter, by removing sections of ground plane over a coplanar compensating inductance.

Although the original intent of the work under this contract was to demonstrate the Quadrant IV chips in a mode where only the superconducting part of the chip was at 4K, subsequent conversations with A. R. Kerr of NRAO somewhat dampened enthusiasm for this approach. These chips are designed to interface with a wide bandwidth coaxial connector, which is vacuum tight. Although the connector (Wiltron K.) has a moding frequency of 46 GHz, it is known from experience that much higher frequencies, up to 100 GHz, are passed with low loss. The K-connector, however, is virtually unused in radio astronomy circles, and waveguide to K-connector couplers tend to be lossy. It was recommended strongly that a waveguide interface should be chosen. The Quadrant III chip design came about in response to this concern. The NRAO point of view is that the thermal loss constraint, i.e. 20 milliwatts or less heat load, could be met by taking the thermal gradient across thin walled stainless steel waveguide, instead of across the chip, as was our proposal. Work on the HYPRES scheme continued, as it was called for in the contract, and because it was felt that there may be other applications for the system, e.g,. in test and measurement, where the coaxial connector would be appropriate.

III. PROCESS DEVELOPMENT

The performance of a mixer system based upon SIS devices depends to a major extent on the electrical quality of such devices. For this reason, during the first year of this program a substantial effort was directed toward the fabrication of SIS tunnel junctions, and investigation of the processing parameters and how they affect electrical device properties. Fabrication of tunnel junctions that behave in the manner predicted by physical laws and not "dirt effects" require optimization of process parameters, and these parameters are heavily dependent upon specific laboratory conditions and equipment employed. In general, it is not possible to directly transfer a processing recipe from one laboratory to another and still maintain the highest quality devices desirable for SIS applications, although the devices might be more than adequate in other circuits. Published processes and process parameters, even for identical material systems, can only serve as a starting point.

The most important measure of junction quality as it pertains to SIS mixers is the steepness of the quasiparticle I-V conduction[8]. High Vm (the product of critical current and subgap resistance) and appropriate J_c are necessary but not sufficient requirements for a quality SIS device.

a. Device Optimization and Parameter Study of Junctions Defined by Anodization

The general approach taken to device optimization involves exploration of the process parameter space around a targeted critical current density through a series of fabrication runs. When a favorable trend is identified, further runs are initiated both to verify the trend and to iterate the parameters toward an optimized device at the chosen current density. The overall process is then repeated for a different current density target. In the work described here, we began with a known process optimized in previous work at a relatively low current density of 2000 A/cm^2, and iterated toward higher current densities. Suitable junctions were produced up to 8000 A/cm^2, however more work, and possibly a radical departure form our present process and material system ($Nb-Al_2O_3-Nb$) may be required to push the useful current density range higher.

The motivation for fabricating high current density junctions is the desire to reduce device capacitance. For a given device conductance or equivalently critical current density, by going to higher current density one can reduce junction area and hence capacitance. Reduced capacitance simplifies device impedance matching and increases potential bandwidth with fixed tuning.

The basic figure of merit for a Josephson tunnel junction is Vm, which we define as Vm = I(4mV)/I(2mV) for niobium. This is approximately numerically equal to the product of the subgap resistance and the critical current, if Rsub = 2mV/I(2mV), as Ic ~ I(4mV)/2, and the above form is taken for convenience. Prerequisite to the SIS optimization process is maximization of Vm. However, junctions with substantially equivalent Vm's would yield different performance due to the rounding of the quasiparticle current onset, minimization of which is the basis for further optimization.

Unfortunately, the mechanisms creating this rounding are not well understood, but it has been learned that it is a strong function of the anodization step used to form the insulating oxide which surrounds the junctions[9], and is mostly manifest in small area (5 micron diameter or less) junctions. It is believed that the effect is caused by encroachment of suboxides around the periphery of the junction, leading to a reduced gap around the edges. Small junctions, with a smaller total to peripheral area, exhibit the reduced gap current more than large junctions. It became evident that during anodization it is important to allow the anodization process to saturate for 5-8 minutes. To allow this, the photoresist must be hard baked at 120C for 20 minutes so that the resist maintains its integrity during the anodization process.

A similar effect is observed in devices fabricated using a lift-off SiO_2 dielectric process which does not use anodization. Again, smaller area junctions suffer most. The cause is unknown at this point, but film stress is believed to be involved. Stressed niobium may have local gap reduction. The lift-off dielectric process, developed in the course of this program, will be described elsewhere in this report.

Vm and critical current density generally have an inverse relationship, as shown in Figure 8, for a given oxidation time. The general explanation is that for a thinner barrier necessary for high current density, there are a larger number of ohmic point contacts through the barrier due to crystal defects. The actual percentage of oxide thickness change over the range in Figure 8 is about 15% given an effective barrier height of 2.3 eV, hence the above interpretation, as applied to the statistical coverage of defect inducing pinholes, is unlikely. More likely is the explanation that the aluminum deposited and subsequently oxidized to form the barrier tends to form clusters during deposition, with surface monolayers between the clusters[10]. The monolayer regions tend to resist oxidation, and in fact Nb suboxides may form through diffusion. As oxidation time and O_2 pressure is reduced to form high current density junctions, the underoxidized regions are left to provide leakage channels.

Cooling of the substrate holder during deposition is known to inhibit the formation of clusters, however this capability is not possible at present in this facility. The thickness of aluminum which produces the best junctions in our process has been found to be 15nm, whereas cooled substrate results show optimum thicknesses less than 5nm, which is further evidence that clustering is the limitation of our present process in achieving current density above 8000 A/cm^2. The highest Vm's achieved were near 40 mV, at 4.2K and at J_c = 3000 A/cm^2. It is believed that this could be substantially improved if substrate cooling during deposition was possible.

Accurate junction definition and therefore good predictability of the critical current of the junctions fabricated from trilayers formed at a given critical current density is important for fabrication of SIS devices at good yields. This is due to the requirement of correct impedance matching to the signal port in the mixer block, and SIS effective conductance scales as the critical current. Further, most practical applications of SIS mixers call for series arrays and not single junctions, due to system dynamic range requirements. The matching of junctions is crucial if the array is to act as a single element. Poor device matching can lead to reduced dynamic range, reduced conversion efficiency, and possibly excess noise. It was found that device quality as evidenced by the sharp quasiparticle

current onset was enhanced by factors favoring patterning accuracy in junctions defined by anodization. As stated previously, a hard bake photoresist process is required to withstand the long anodization time necessary to achieve saturation. SiO_2 was also used as a junction definition mask for anodization, with results not significantly better than the baked resist. Ease of removal of the photoresist (in acetone, followed by UV-O3 descum) favors this process, however for junctions approaching one micron in size, the SiO_2 might be preferred. With this process, patterning and uniformity are excellent to acceptable for junction sizes down to about 3 microns.

b. Parasitic Capacitance and the Lift-Off Process

The desirability of minimizing total device capacitance was discussed above. One undesirable feature of the anodization process is the high dielectric constant of Nb_2O_5 of about 29. Lithography limitations require a certain amount of overlap surrounding the junctions, which contributes parasitic capacitance. This capacitance would be reduced if a lower dielectric constant oxide could be substituted for Nb_2O_5. Perhaps one of the more significant results of the present program was the development of such a process. By avoiding anodization, one has the additional advantage of not requiring electrical connections between the base electrodes of series junctions, which must be subsequently etched away. Figure 9 shows a schematic of the lift-off process.

One starts with the usual Nb-Al_2O_3-Nb trilayer and applies a slightly re-entrant stencil. After reactively ion etching the counterelectrode using the residual Al in the barrier as an etch stop, the substrate is placed in ozone to etch back the photoresist by a few hundred angstroms. SiO_2 is then deposited in a dual ion beam system, followed by an acetone soak which removes the photoresist stencil. One is left with the junction surrounded by low dielectric constant oxide. In practice, the junction is then covered with photoresist and the ground plane anodized, which closes any pinholes in the thin (150nm) deposited dielectric without affecting the junctions. This anodization also allows one to create high value capacitors as with the previous process, which are actually quarter-wave stubs as described in the design section of this report.

This process was originally developed using evaporated SiO as the dielectric, and excellent definition, uniformity, and device yield was achieved due to the favorable collimation of the evaporation process. As this system is no longer available due to its dedication to YBCO film preparation, the lift-off process was migrated to the present dual ion beam SiO_2 system. Initially, device definition was poor, due to SiO_2 adhesion to the side of the stencil. By tailoring the resist profile, good definition was eventually achieved, but probably not to the levels that could be achieved using evaporation. The SiO_2 dielectric has lower dielectric constant than the SiO, however. Continued refinement of the lift-off process eventually yielded the capability of producing sub-two micron junctions suitable for SIS mixers. The original anodization junction definition process was abandoned in favor of the lift-off process for the remainder of work under this program.

c. Multi-Level Integrated SIS Mixer Process

The fabrication process which was developed to produce these devices is considerably different from that used to produce HYPRES instrument chips[9]. The SIS process is shown schematically in Figure 10. First, a $Nb/Al_2O_3/Nb$ trilayer is formed in-situ, then patterned. Patterning was by ion milling through the barrier, then etching through the base electrode with Reactive Ion Etching (RIE). Photoresist is then applied, exposed, and developed away outside junction regions. Using the barrier as an etch stop, the counter electrode is removed by RIE, with the photoresist in place. Finally, dual ion beam SiO_2 is deposited and lifted off the junction areas by removing the photoresist in acetone. This lift-off process, invented during Phase I and refined under Phase II, gives very good junction definition down to below 2 microns, far better than the anodization process more commonly employed. The SiO_2 provides much lower stray capacitance as well. Following lift-off, a Nb wiring level is DC magnetron sputtered and patterned by RIE. This is followed by a thick (350 nm) SiO_2 layer, which is used as the dielectric for the microstrip compensation inductors.

After patterning the second SiO_2 level, the base electrode is exposed and the counter electrode where capacitors are to be formed. The wafer is then anodized, growing 1000 Å of Nb_2O_5 (ϵ=29) in these regions. These "capacitors" are actually quarter-wave transmission lines, designed to terminate the

inductors with a low impedance. For anodization, all areas to be anodized must be connected. The following photoresist pattern and etch step removes the connections which were established for this purpose. Then, a final Nb level is deposited and patterned, which forms the compensating stripline. After photoresist patterning, a Ti-pd-Au lift-off is performed, which facilitates contacting of the bond pads. The actual flow sheet for this process is shown in Figure 11. Table II shows film thicknesses and materials used in this process.

TABLE II

MASK LEVEL	MATERIAL	THICKNESS (nm)	DEPOSITION METHOD
M1	Nb (base)	135	DC Magnetron
	Nb (counter)	45	DC Magnetron
I1A	SiO_2	150	DIBS
I1B	-	-	Anodize Pinholes
M2	Nb	300	DC Magnetron
I2	SiO_2	350	DIBS
I1C	Nb_2O_5	100	Anodization
B1	-	-	Line Etch
M3	Nb	700	DC Magnetron
R3	Ti	50	E-Beam Evap
	Pd	50	E-Beam Evap
	Au	1000	E-Beam Evap

In the course of processing, a number of difficulties were encountered. One of the most persistent was the notching shown in Figure 12. This occurs in the Nb base electrode, in the capacitor areas, during the etch step to expose these areas. Although the Al in the barrier serves as an excellent etch stop, the two levels of SiO_2 and the counter electrode which must be removed pose a problem. It is well known in RIE that mechanical etching (ion milling) tends to occur near boundaries, and in this case there is very little time between clearance of the desired materials and severance of the underlying layer due to ion milling. Although severance did occur on several wafers, causing the compensation network to be disconnected, most wafers did not suffer from this effect.

Another problem encountered was the reliability of the lift-off junction fabrication process. At times, the perpendicularity of the resist profile was inadequate and SiO_2 would adhere to the side of the resist, preventing lift-off on a large percentage of the junctions. In this process, resist perpendicularity is crucial. If the stencil is re-entrant, as is common in lift-off processes, short develop around the junction. Sloped edges prevent lift-off entirely. Through characterization of the resist and careful control of baking and developing, this problem was eventually solved.

IV. RF TEST RESULTS

Detailed RF testing and receiver noise measurements were carried out by S. K. Pan and A. R. Kerr of NRAO at Charlottesville, VA on the Quadrants I, II, and III chips. The RF performance of the Quadrant IV (HYPRES-designed) chips was not measured, due to mechanical difficulties encountered in chip cooling in the cooler to be described. The "conventional" (5 x 10 mil) Quadrant I and II chips, designed for 115 and 230 GHz, were tested in a suitable receiver block, and the resulting noise temperatures are plotted in Figures 13 to 15. In these figures, the "H" represents a point from the present devices. Other points represent similar devices fabricated elsewhere. In spite of the fact that the I-V curves of the HYPRES devices were in many cases superior to those of other devices which were based on IBM lead alloy technology, measured noise performance did not reflect this. It is believed that the normal state resistance of the HYPRES devices tested was a factor of two lower than optimum. This produces coupling losses which adversely affect noise performance. Further fabrication runs could produce the optimum normal state resistance, however by the time the test results were interpreted, funding for this phase was exhausted. These results calibrate the expected performance of the fully integrated (Quadrant III) mixers, however, and although the performance achieved was not clearly superior, it is among the best produced by all-niobium devices.

More significant is the performance of the fully integrated mixers, the first such mixers ever demonstrated. NRAO's SIS mixer test receiver uses a 2.4" long stainless steel WR-10 (75 - 110 GHz) input waveguide from room temperature to 4K. It was therefore necessary to design a waveguide mount for the coplanar mixer. The two obvious alternative waveguide mount designs use finline and suspended substrate stripline.

Initially a finline mount appeared well suited to the planar SIS mixer. A waveguide to finline transducer was envisioned, followed by a finline to coplanar line transition. However, unless the fins are on opposite sides of the (thick) substrate, the finline to TEM transition requires very precise control of the fin taper in the crossover region. If a thin-film dielectric layer separates the film, the pattern alignment is critical to less than one micron, making a broadband TEM transition very difficult to realize.

Additional limitations of the finline configuration are: (i) A thick substrate can support undesired modes in the waveguide; we found this to be particularly troublesome with a 0.010" quartz substrate in a WR-10 waveguide. (ii) Each mixer requires a relatively large area of substrate, limiting the number of mixers which can be produced on a single wafer.

A simple fixed-tuned waveguide to 50 ohm suspended substrate stripline transducer was designed with a VSWR $\leq$ 1.2 over the full WR-10 waveguide band (75 - 110 GHz). The transducer and its frequency response are shown in Figures 16 and 17. The only change required to convert the waveguide transducer of Figure 16 into an SIS mixer block is the addition of a DC and IF ground return. This is accomplished using a quarter-wave wire between the stripline and the metal block as shown in Figure 18.

The integrated mixers were measured in the NRAO WR-10 test dewar using the procedure described in[11]. The dewar has a stainless steel input waveguide, plated inside with 0.6 micron of copper to reduce its loss. A cryogenic HEMT IF amplifier at 1.4 GHz is connected to the mixer through a calibration switch and bias tee. The IF noise temperature is 3.2K referenced to the calibration switch.

Figure 19 shows the double-sided receiver noise temperature, referred to the mixer input flange, from 75-115 GHz. The mixer conversion loss was in the range 8-12 db, larger than expected for this type of mixer by 5-10 db. Measurement of the sideband ratio, (i.e., the ratio of conversion losses measured separately in the upper and lower sidebands) indicated unexpected variation over the RF tuning range.

At the time of this writing, we have only done initial tests on mixers from a single wafer. While the results for both noise temperature and bandwidth are encouraging, the relatively high conversion loss and unexpected variation of the sideband ratio with frequency require further investigation. It is interesting to note that the conversion loss of all mixers on this wafer, both integrated and of conventional design, appears to be 6-10 db larger than expected. We speculate that the M3 Nb interconnection metallization on this wafer may be responsible for the high loss; its color is peculiar -- a brownish orange -- and it has poor adhesion in many parts of the wafer. The origin of this problem with the M3 level, ordinarily one of the more trouble free levels in the process, is not known.

The conclusions drawn from this work on the fully integrated mixer may be summarized as follows:

(i) It is possible to construct a fully integrated SIS mixer for 75-110 GHz with no adjustable tuners and with low noise. The best receiver noise temperature ever reported using a cryogenic Schottky diode mixer (62K DSB) is about 50% higher than the minimum for the prototype SIS receiver described here.

(ii) Simple coplanar topology can be used. This eliminates the need for registering patterns on opposite sides of a wafer, and allows the use of a conveniently thick substrate (0.010") in the mixer.

(iii) The design is readily integrable with other components, such as planar antennas or future superconducting IF processors.

(iv) The design should be useful up to 300 GHz, and possibly to 600 GHz, with appropriate frequency scaling.

V. CRYOGENIC SYSTEM DEVELOPMENT

The goal of this effort was to demonstrate an SIS mixer in a dewar-based cryogenic system that used the SIS mixer chip itself to take the entire 300K thermal gradient, while allowing 20 milliwatts or lower heat load. The precedent for this approach can be found in HYPRES instrument products, which by use of a small, directed jet of liquid helium cool only the corner of a fused silica chip, while elsewhere the chip is maintained at room temperature[12]. This allows very wide bandwidth interconnection between the room temperature and cryogenic environments. As the flowing system is somewhat inefficient, it was proposed that somehow the cold end of an SIS chip would be clamped to a dewar cold finger, and after poking through a radiation shield, the other end of the chip would offer a room temperature interface point. A coplanar waveguide would connect the 4K and room temperature ends of the chip, providing a wide bandwidth interface. Such an approach was actually the first conception of HYPRES instrument architecture, and experiments early on with a 2"x.2" fused silica chip were successful. The present SIS chip is 1 cm x .2 cm, which should theoretically allow the specified heat load. The task was to design, construct, and measure the thermal performance of a cryostat designed to cool these chips in the above manner.

After reviewing alternatives, it became evident that the only viable approach was to modify an existing dewar to our needs and interpret the 20 mW heat budget as pertaining only to that contributed by the chip and associated components. The partition of resources available to this project did not support a complete in-house design meeting the specification as a total heat load. The development of the demonstration system went through several phases:

1. Commercial dewar selection and procurement
2. Dewar preparation and modification
3. "Poke through" design and construction
4. Bonding procedure development
5. Heat sinking method optimization
6. System evaluation

The criteria used in selecting the dewar from a commercial vendor included:

- Manageable size, approximately 5 liters
- Reasonably low cost
- Short delivery time
- Nitrogen cooled shield, for low liquid helium boil-off and reproducible heat load measurements.
- Reliability, ease of use

The selection was narrowed to two contenders, the Janis 8DT dewar body and the Precision Cryogenics detector dewar. The Janis dewar was more expensive and required considerably more in-house fabrication, so the Precision Cryogenics unit was ordered for evaluation. Although it was compact and mechanically suitable, internally it was sloppily constructed and it was refused after being returned to the vendor twice for vacuum leaks, which caused a five week delay. The Janis Research 8DT was ordered and kept. The 8DT is not a dewar but a portion of one and a tail section had to be designed and produced. It consisted of an inner helium vessel with cold finger, a radiation shield with access hole and an outer body with access port. The components which support the chip with access via a Wiltron K-connector were constructed and the assembly is mounted in the access port with an O-ring seal.

Due to the different chip geometry, the method by which the chip is bonded to the K connector as used in HYPRES products was not suitable, hence another method had to be developed. Although a direct solder junction using tin-lead solder had the required mechanical rigidity, the interface was not reproducible and generally electrically poor, as evidenced by TDR measurements. Indium solder was tried and although there was better control of the amount of solder in this highly critical area, mechanical rigidity was poor. A shelf, supporting the chip from the backside, was finally adopted, along with indium solder. This simplified the assembly procedure, provided the necessary mechanical rigidity and good electrical interface but shortened the effective thermal length of the chip by 20%.

The basic method of cooling the SIS part of the chip involved contacting the chip to a copper braid, which was then heat sunk to the cold finger. The braid must be long enough to absorb thermal motion and vibration, yet short enough to provide low thermal resistance. The type of braid used was New England Electric # NE2432448 99.9% pure Cu. Initial experiments utilized a "U" clamp of copper, soldered to the braid. The "U" would fit over the end of the chip and be packed with silicone grease. This method did not provide adequate thermal contact to the chip, and the "U" was prone to slip off of the chip during (or after) assembly. Attempts at clamping the chip were abandoned in favor of directly soldering the chip ground plane to the braid using low temperature indium solder. A solder mask of negative photoresist KTFR protected the actual circuits, exposing Au covered ground plane areas adjacent to the circuit area. At first, the chip was soldered to an small Cu block, which was soldered to the braid. This was accomplished by coating both chip and block with indium solder, placing the parts in proximity and heating on a hot plate until the pieces bonded together. This method was abandoned because chip damage often occurred, and there was concern that differential contraction during cool down would crack either the bond or the chip. Directly soldering small pieces of braid to the chip, which were then soldered to a larger piece of braid, was the most successful method of contracting the chip. The large braid was soldered to a copper block, which was screwed onto the cold finger, with indium gasketing. The braid-to-braid interface was eventually replaced by a small copper plate, to which each braid was soldered, which gave lower thermal resistance.

Early experiments were conducted without particular attention to radiation shielding and without success. Once the importance of radiation shielding was realized, careful attention was paid to this aspect and more successful results ensued.

After six experiments, without the observation of superconductivity, germanium resistance thermometers (GRT's) were soldered to both ends of the braid. Temperatures reached 11K at the chip, 9.75K at the cold finger. A GRT mounted directly on the cold finger block measured 8.5K, clearly indicating a problem. It seems that the cold finger was brazed onto the outside end of a 1/8"

thick stainless steel cup, which served as the lower part of the liquid helium reservoir. In spite of the diameter of the cold finger being 1.5", the stainless steel was effectively insulating the cold finger from the liquid helium. To solve this problem, a 1" diameter hole was milled through the stainless steel cup bottom, so that the liquid made contact with the copper cold finger. A repeat temperature measurement, with the chip in place, saw the cold finger temperature drop to 6.75K, a vast improvement, but still far from ideal. Without the chip, the cold finger reached 5.75K. With the addition of aluminized mylar superinsulation wrapped around the radiation shield and aluminum foil wrapped around the helium vessel/cold finger, 5K was measured at the cold finger. The remaining temperature difference is believed to be caused by thermal leakage from the leads into the GRT itself. The GRT's were removed from the braid and superconductivity was observed on the chip. The inductive compensation of this particular chip was shorted to ground and a superconducting short was observed, which could be driven normal with sufficient current.

After this initial observation of superconductivity on-chip, the observation of superconductivity was repeated several times. Initial thermal load measurements based of helium boil-off rate indicated an excess of 55 mw, much higher than expected. The supposition was that due to the room temperature shelf at the front of the chip and the large bond area maintained at low temperature at the near, only 1/3-1/2 of the chip was actually serving as a thermal insulator. As there was insufficient time and other resources to redesign the mask set to produce chips of greater length, another means of effectively lengthening the thermal path was needed. This was accomplished by using a dicing saw to cut away the SIS circuit portions of some chips, leaving only the transmission line. The doctored chips, .8 cm long, were bonded to unmodified chips, producing a structure 1.6 cm in length, while maintaining electrical access (but with terrible RF properties). The composite chips went superconducting, and the measured boil-off was reduced to 25 milliwatts. Junction I-V curves showed a reduced gap, indicating an operating temperature of about 6.5K. At this point funding was exhausted and manpower was switched to other programs. It is felt that this demonstration, although not perfectly successful, demonstrates feasibility, and that with further work this temperature could be reduced by 1K, which is adequate for Nb.

The cryogenic system discussed in the preceding paragraphs consists of two basic elements; the dewar and the chip assembly. The dewar consists of a Janis Research 8DT dewar body with a HYPRES made custom tail section. The 8DT is liquid nitrogen shielded and of all stainless steel construction. It holds 5 liters of liquid helium, and 1.5 liters of liquid nitrogen. The tail section has three parts: The helium vessel, a radiation shield, and an outer body. The helium vessel consists of a flange welded to a 3" length of 2" diameter stainless steel tube. The tube terminates in an OFHC copper cold finger. The flange bolts to the 8DT and is sealed for vacuum tightness with indium gasketing. The radiation shield is an aluminum tube that bolts to the base of the LN portion of the 8DT. It has a removable cap and a 1" diameter port with an adjustable copper plate. The Cu plate has in its center a section of 3/16 brass tubing through which the chip protrudes. The outer body is a cylindrical stainless steel section welded to a flange which bolts to the bottom of the 8DT. It has a 1" diameter window for the chip assembly, terminated in a removable vacuum sealed blank flange. Super-insulation covers the radiation shield, including the removable cap. The liquid helium vessel is also wrapped carefully in super-insulation. Two sets of four-wire sensor cables enter the dewar at the top and run down to the tail where they are wrapped around the cold finger. A GRT is inserted in the cold finger, and a carbon cryo-resistor is mounted on the braid interface block.

The chip assembly includes the O-ring sealed front mounting plate. The SIS mixer chip is prepared in the following sequence:

1. Apply KTFR solder mask.

2. Tin the exposed bonding areas.

3. Bond tinned Kapton IF leads to the rear pads (this was not required for these measurements)

4. Bond extension chip to coplanar line.

This assembly is then placed on the chip shelf and bonded to the connector plate using #2 indium solder. The connector plate and O-ring are screwed to the aluminum mounting flange. The K-connector protrudes out of the connector plate opposite the chip. After the aluminum flange is mounted on the dewar, the copper braid is carefully soldered to the chip ground plane through a bottom port. The port is then sealed, the dewar evacuated, and cryogens are added.

The major points learned from this exercise are summarized below:

1. Careful radiation shielding is essential for this type of cooling.

2. The best thermal contact is a solder joint, rather than a pressure contact.

3. Flexible copper braid has adequately high thermal conductivity in this application. It effectively provides mechanical isolation.

4. The chip should have been about twice as long as it was. This will reduce the bandwidth of the electrical interface somewhat, and produce additional loss. If higher thermal loss is tolerable, then this restriction need not apply.

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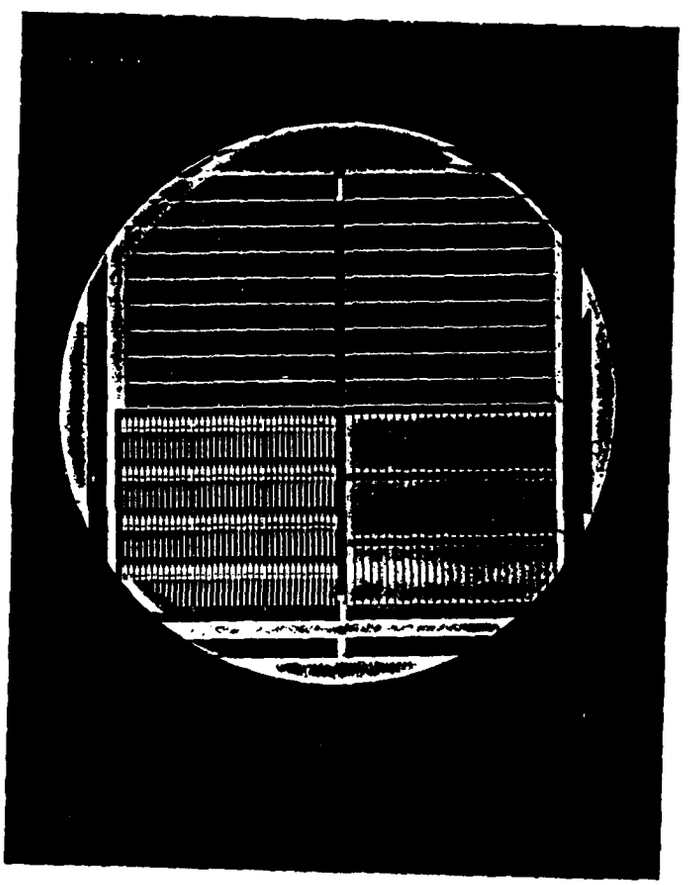
QUADRANT I

QUADRANT II



QUADRANT III

QUADRANT IV

Fig. 1 Photograph of undiced 3" substrate showing the four quadrants where the different style chips are located.

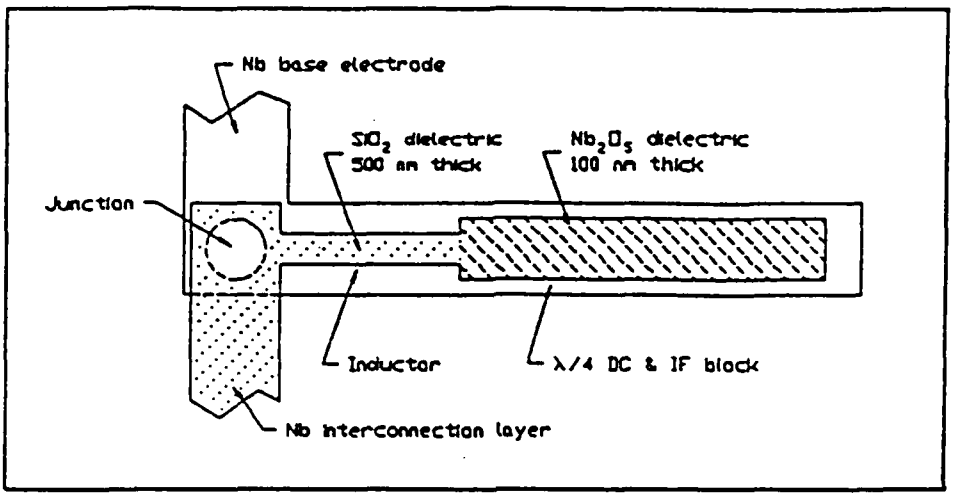
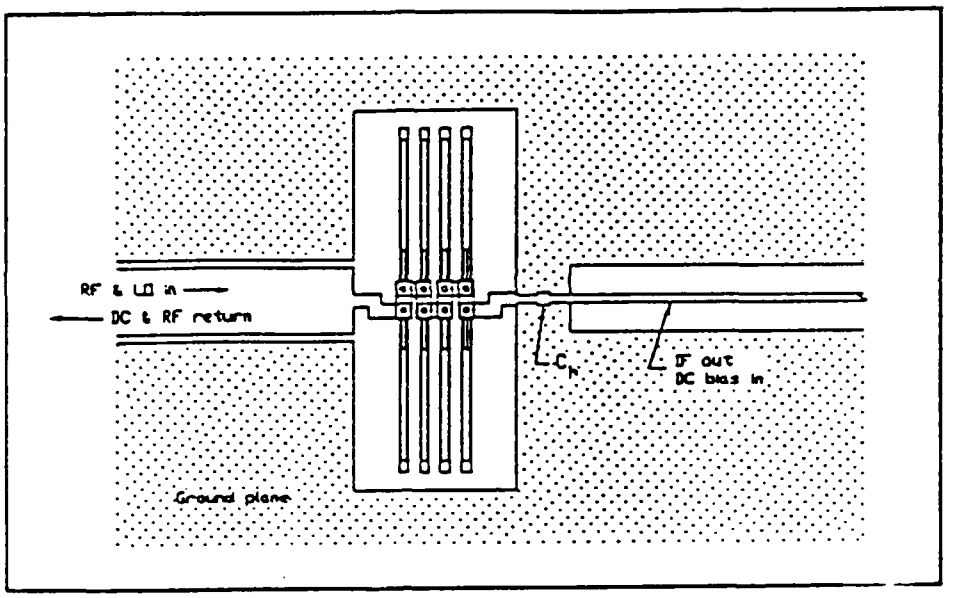


Fig. 2 Inductively tuned SIS junction with quarter-wave DC block.

a.



b.

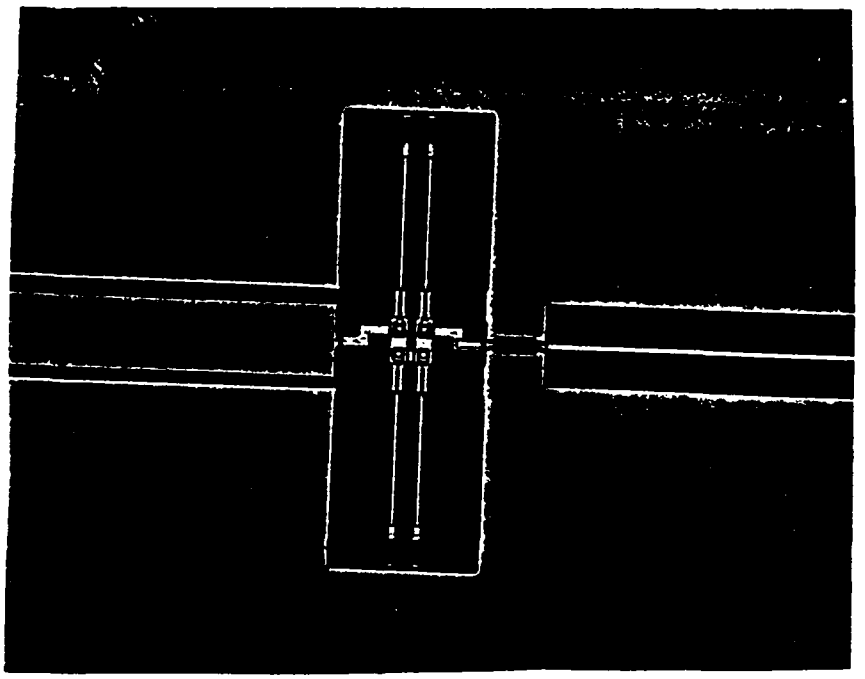


Fig. 3 **a.** Array of eight inductively tuned junctions coupled to a coplanar input line (at left). The inductance L_h of the hole in the ground plane in the vicinity of the array is tuned out by the capacitor C_h. **b.** Closeup of actual four-element array.

c.

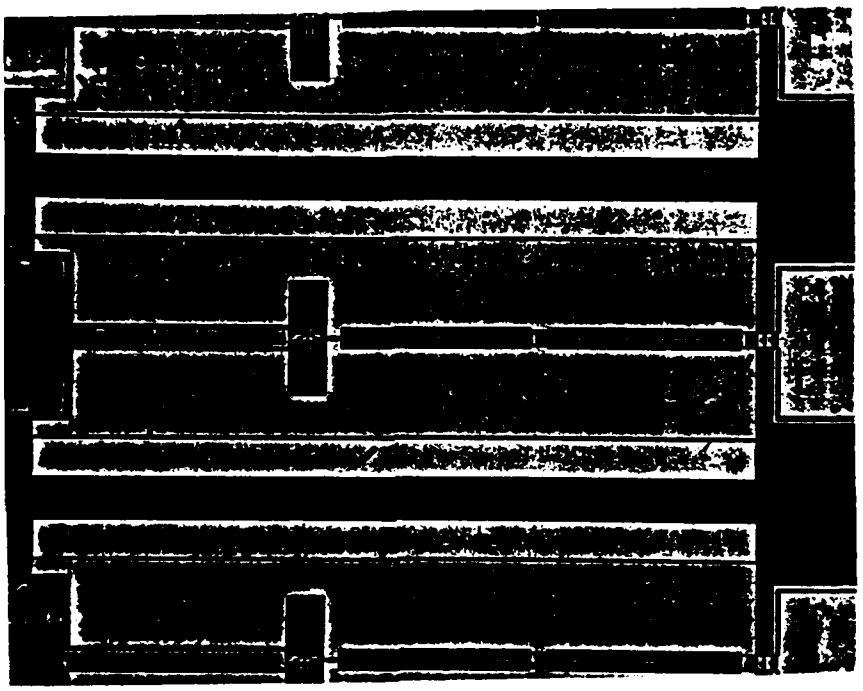


Fig. 3 c. Overview showing IF filter to the right and waveguide coupling probe terminus to the left.

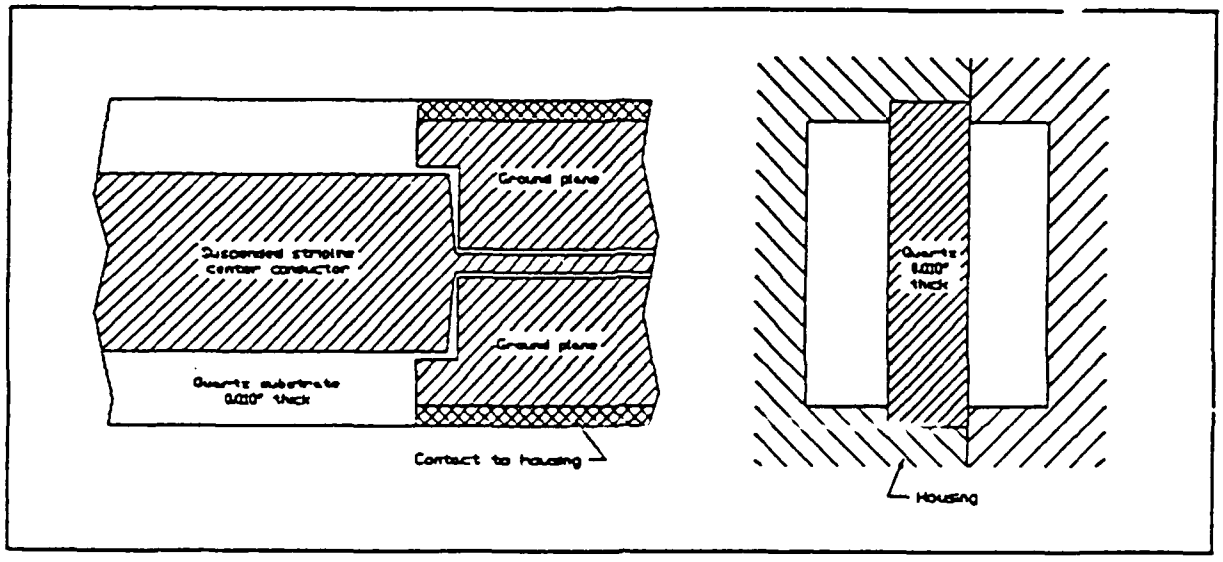


Fig. 4 The coplanar line to suspended substrate stripline transition.

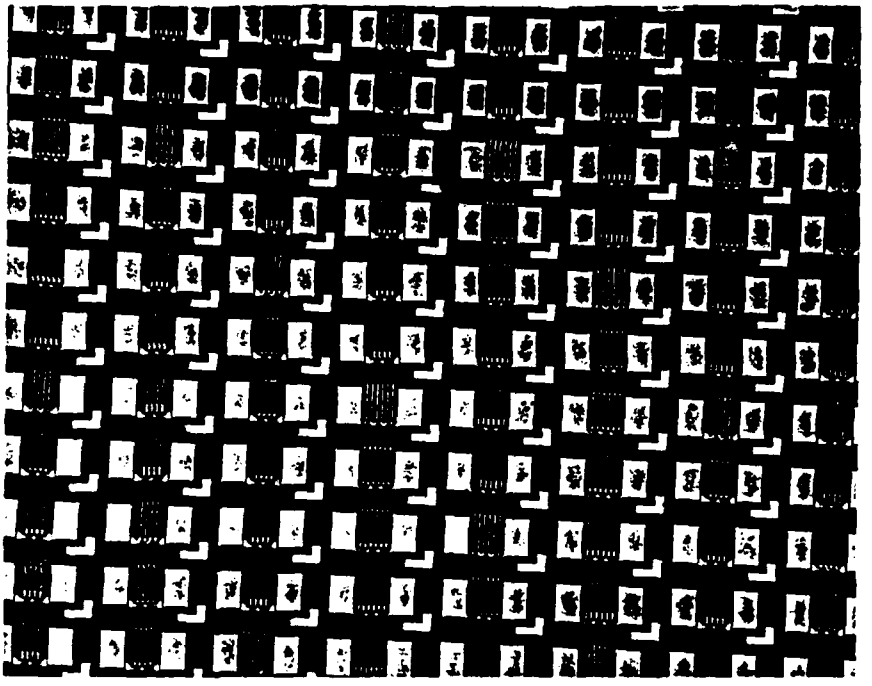


Fig. 5 An overview of the array. Each 5 x 10 mil cell contains a 2 - 8 element SIS array, with variation of compensation inductance.

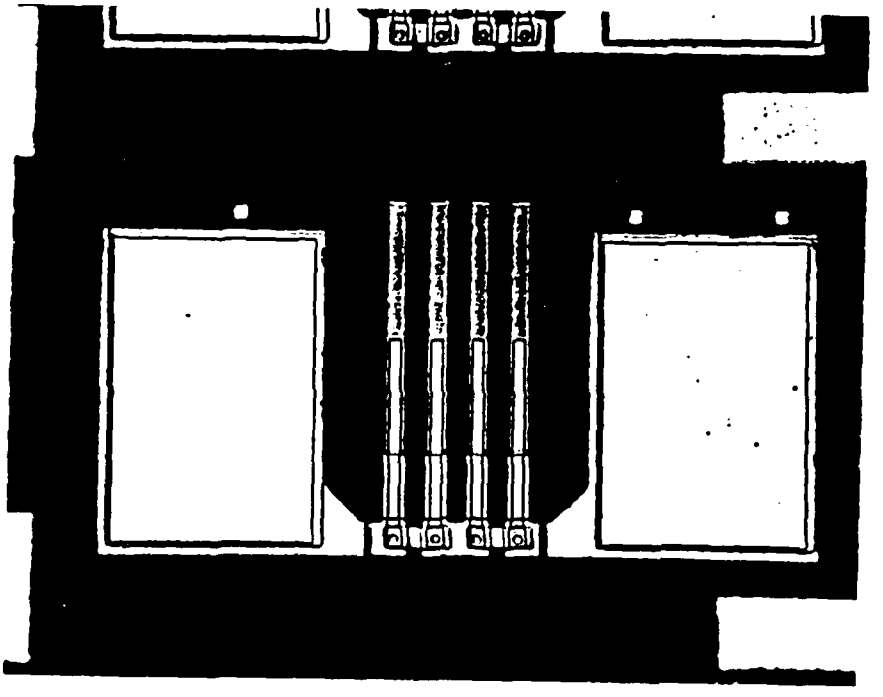
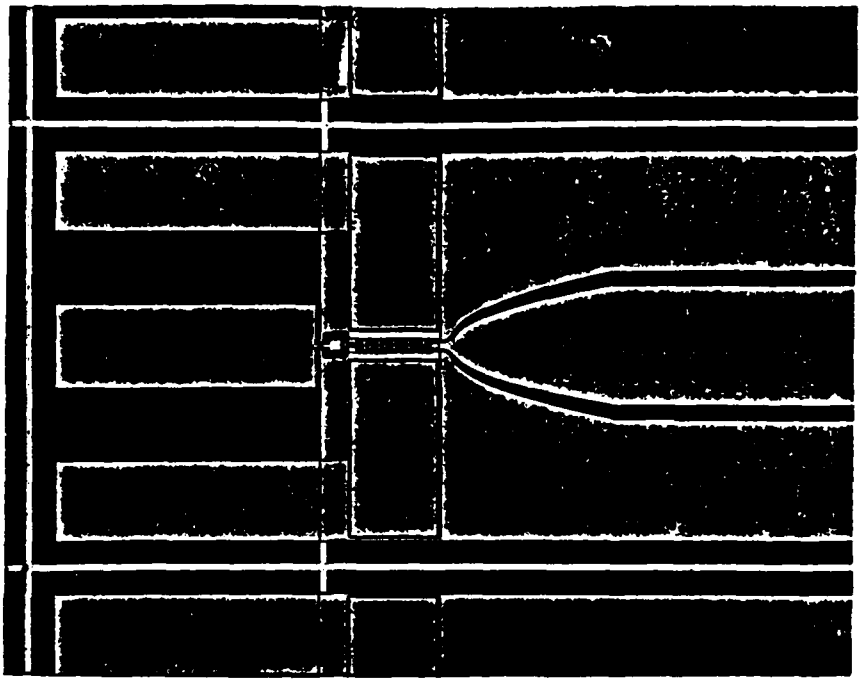


Fig. 6 Closeup of a four-element array showing individual compensation networks. Each stripline consists of an inductive component and quarter-wave ac grounding portion. The inductive element consists of microstrip over 350 nm of SiO_2, and the grounding section uses anodized Nb_2O_5 with a dielectric constant of 29.

a.



b.

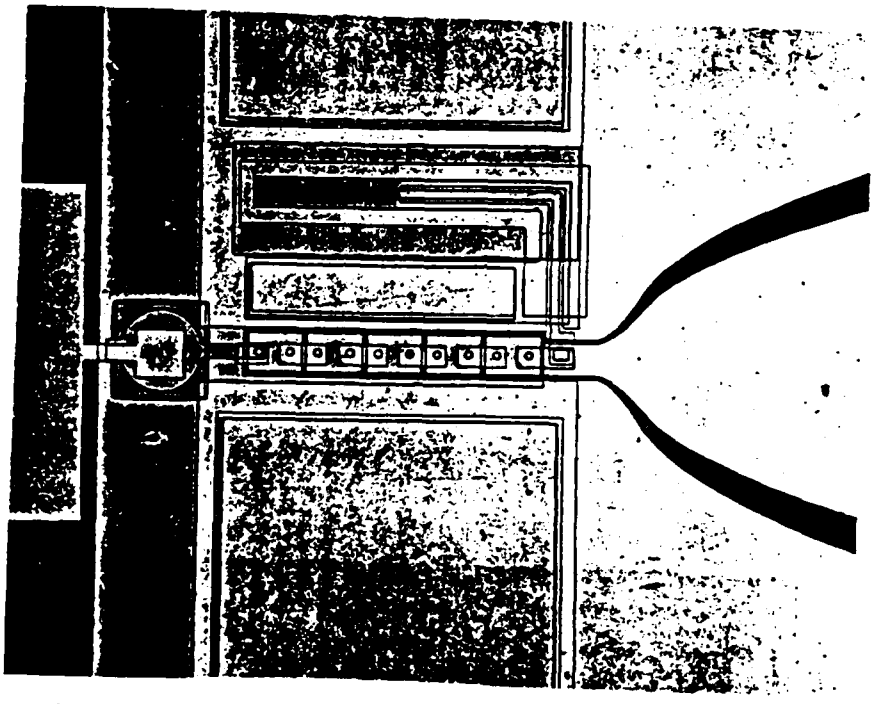


Fig. 7 a. View of end of HYPRES designed SIS mixer array chip. To the left are bonding pads for the IF port (1.5 GHz Kapton flexible substrate). To the right is the end portion of the coplanar waveguide input line, which is 1cm in length and fabricated in 1 μm thick Au. b. Closeup of the ten-element array showing the IF filter capacitance (to the left), and the alterable inductive compensation network (above the array). The inductance can be varied by removing portions of the Nb overlayer with an ultrasonic cutting tool.

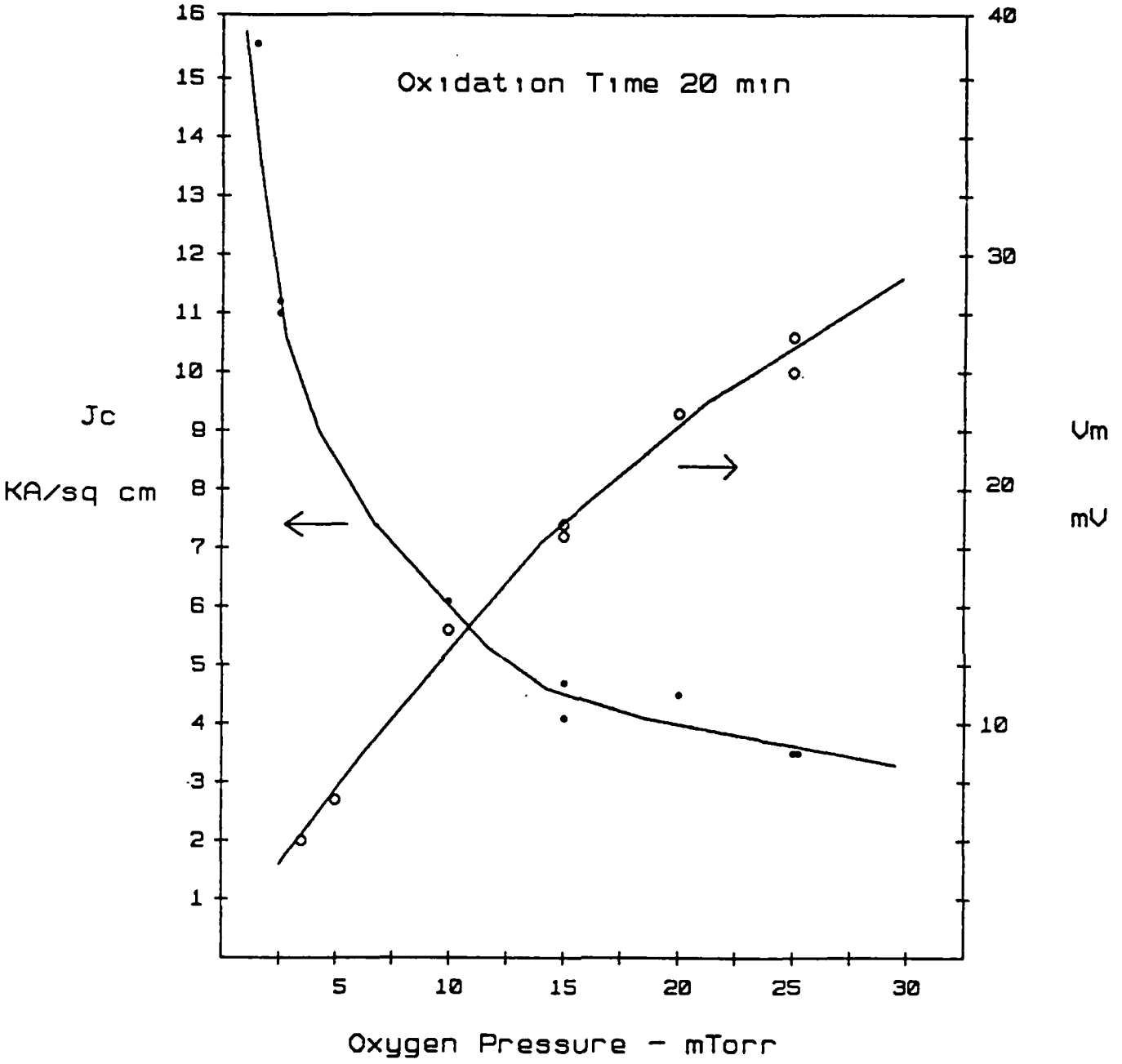


Fig. 8 J_c and Vm as a function of partial O_2 pressure for a fixed twenty minute oxidation time. Although J_c increases rapidly at low O_2 pressure, Vm is poor due to unoxidized defects in the barrier.

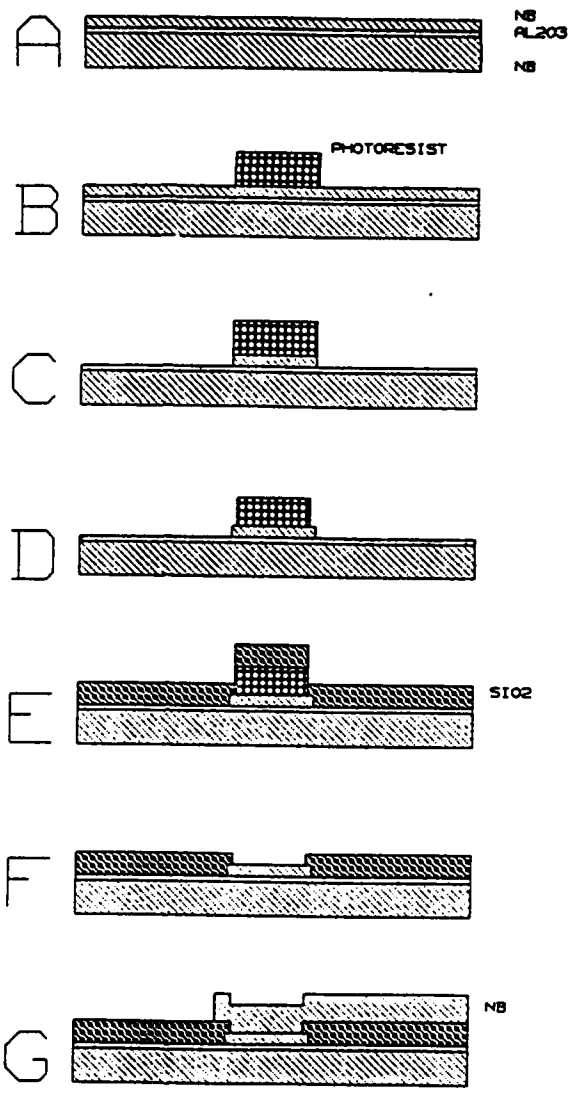


Fig. 9 Cross-section of the lift-off junction definition process developed under this program. a. Au Nb-Al_2O_3-Nb trilayer is deposited over the entire 3" substrate. b. A photoresist stencil is applied. c. Using the residual Al in the barrier region as an etch-stop, the counterelectrode is removed by reactive ion etching. d. The photoresist is etched back in an O_3-UV stripper. e. SiO_2 is then deposited in a dual ion-beam apparatus. f. The photoresist and overlying SiO_2 is removed in acetone. g. Contacting Nb metallization is deposited and patterned.

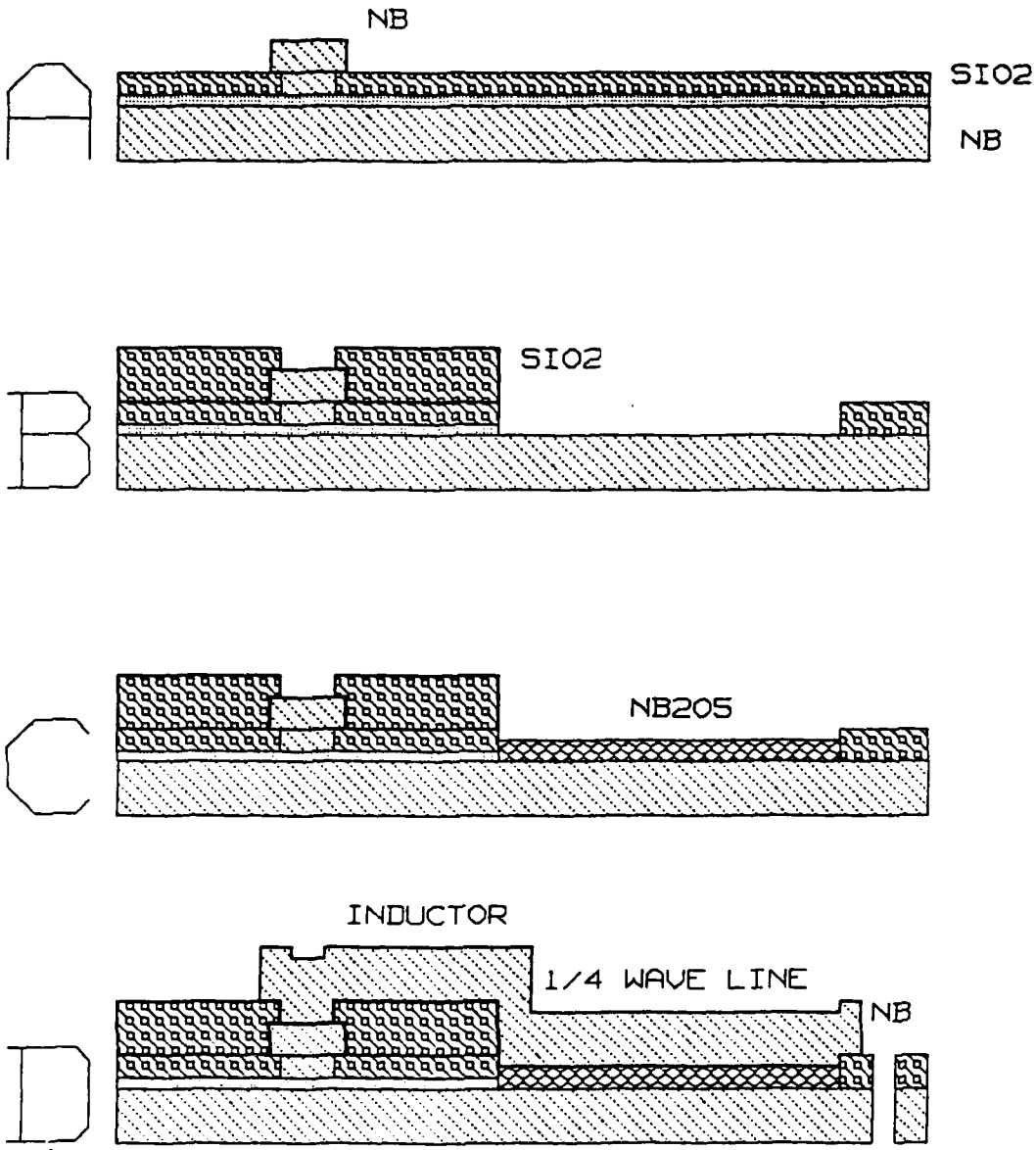


Fig. 10 a. After junction definition using the lift-off technique, a cap of M2 Nb contact metallization remains. b. A second SiO_2 dielectric (350 nm) is deposited and patterned surrounding the junctions, but exposing the base electrode as shown. c. The exposed base electrode is anodized, yielding high capacitance Nb_2O_5 dielectric. d. Third level Nb metallization is applied, completing the process. The SiO_2 provides the inductive compensation, while the region over Nb_2O_5 provides quarter-wave a.c. grounding.

	A	B	C	D	E	F
1	SPEC#	OPERATION	PROCESS DATA	DATE	VF#	COM #
2	1000	M1 DEPOSITION	**********	******	*****	******
3	T-01	M1 Dep. Run#	J1= Ka/cm2 , \r= mV			
4	T-01	M1 Dep. Run#	J1= Ka/cm2 , Vm= mV			
5	2000	M1 PHOTO - I1A PHOTO	**********	******	*****	******
6	P-02	Coat/Bake	5 minutes / 90° C			
7	P-03	Align/Expose M1	Tool# Mask# ExpT =			
8	P-04	Develop/Bake	5 minutes / 120° C Dev Time:			
9	P-06	M1 Wet Etch (Nb ETCH)	Time =			
10	P-07	Resist Strip	Acetone Ultasonic/ Scrub			
11	P-02	Coat/Bake	5 minutes / 90° C			
12	P-03	Align/Expose I1A	Tool# Mask# ExpT =			
13		USE LIFT OFF STENCIL	TRI-LAYER PROCESS			
14	P-04	Develop/Bake				
15	3000	I1A Etch	**********			
16	T-10	I1A Etch	Tool# Run#			
17	3500	SiO2 DEPOSITION	**********	******	*****	******
18	T-05	SiO2 deposition	1500 A SiO2 Lift-off			
19	3600	LIFT-OFF	**********	******	*****	******
20	P-07	Acetone Soak				
21	8000	M2 DEPOSITION	**********	******	*****	******
22	T-02	M2 Depostion (Nb only)	Thickness = 3000 A (No Al)			
23	9000	M2 PHOTO	**********	******	*****	******
24	P-02	Coat/Bake	5 minutes / 90° C			
25	P-03	Align/Expose M2	Tool# Mask# ExpT =			
26	P-04	Develop/Bake	5 minutes / 90° C Dev Time:			
27	10000	M2 (RIE) ETCH	**********	******	*****	******
28	T-03	M2 (RIE) Etch	Tool# Run#			
29	P-07	Resist Strip	Acetone Ultrasonic/Scrub			
30	P-05	ACI				
31	14000	I2 DEPOSITION	**********	******	*****	******
32	T-05	I2 Deposition SiO2	Thickness = 3500 A			
33	15000	I2 PHOTO	**********	******	*****	******
34	P-02	HMDS/Coat/Bake	5 minutes / 90° C			
35	P-03	Align/Expose I2	Tool# Mask# ExpT =			
36	P-04	Develop/Bake	5 minutes / 120° C Dev Time:			
37	16000	I2 (RIE) ETCH	**********	******	*****	******
38	T-06	I2 (RIE) Etch (SiO2)	Tool# Run#			
39	P-07	Resist Strip	Acetone Ultrasonic/Scrub			
40	P-05	ACI				
41	5000	I1B PHOTO	**********	******	*****	******
42	P-02	Coat/Bake	5 minutes / 90° C			
43	P-03	Align/Expose I1B	Tool# Mask# ExpT =			
44	P-04	Develop/Bake	5 minutes / 120° C Dev Time:			
45	3000	I1A Etch	**********			
46	T-10	I1A Etch	Tool# Run#			
47	6000	ANODIZATION #1	**********	******	*****	******
48	P-08	Anodization	Volt. = 50 V. Time = 8 min.			
49	P-07	Resist Strip	Acetone Ultasonic/ Scrub			

Fig. 11 The following two pages show a copy of the process flow document of the SIS mixer process developed under this program.

Fig. 11 (...continued)

51	7000	B1 PHOTO - B1 ETCH	**********	******	*****	******
52	P-02	Coat/BaRe	5 minutes / 90° C			
53	P-03	Align/Expose B1	Tool# Mask# ExpT =			
54	P-04	Develop/Bake	5 minutes / 120° C Dev Time:			
55	T-10	B1 Nb Etch (Nb ETCH)	Time =			
56	P-07	Resist Strip	Acetone Ultasonic/ Scrub			
57	19000	M3 DEPOSITION	**********	******	*****	******
58	T-02	Nb Depostion 5000 A	Tool# Run# Thk.= Ohm/□=			
59	20000	M3 PHOTO	**********	******	*****	******
60	P-02	Coat/Bake RPM=6000	5 minutes / 90° C			
61	P-03	Align/Expose M3	Tool# Mask# ExpT =			
62	P-04	Develop/Bake	5 minutes / 120° C Dev Time:			
63	21000	M3 (RIE) ETCH	**********	******	*****	******
64	T-03	M3 (RIE) Etch	Tool# Run#			
65	P-07	Resist Strip	Acetone Ultrasonic/Scrub			
66	P-05	ACI				
67	22000	R3 PHOTO	**********	******	*****	******
68	P-02	HMDS/Coat/Bake	RPM = 4500 5 minutes / 90° C			
69	P-02	Chlorobenzene Soak	Time = 15 minutes			
70	P-03	Align/Expose R3	Tool# Mask# ExpT =			
71	P-04	Develop/Bake	(Overdev. 10 sec) 5 min./90° C Dev Time:			
72	23000	R3 DEPOSITION	**********	******	*****	******
73	T-09	Ti/Pd/Au Evaporation	Tool# Run# Thk.= Ohm/□=			
74	24000	LIFT-OFF	**********	******	*****	******
75	P-07	Lift-off	Soak in Acetone for 2 hours			
76	26000	DICING/PACKAGING	**********	******	*****	******
77	D-01	Dicing/Packaging				
78	27000	TEST	**********	******	*****	******

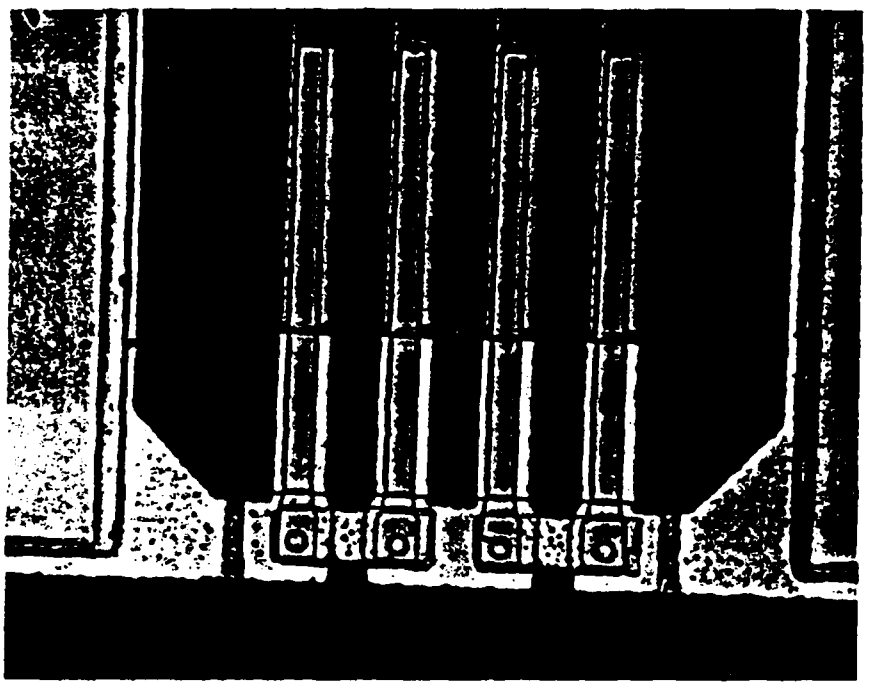


Fig. 12 Overetching causes discontinuities in the base electrode to the left and right of the array. To a lesser degree, the overetch disconnects the compensation network at the oxide boundary above the array.

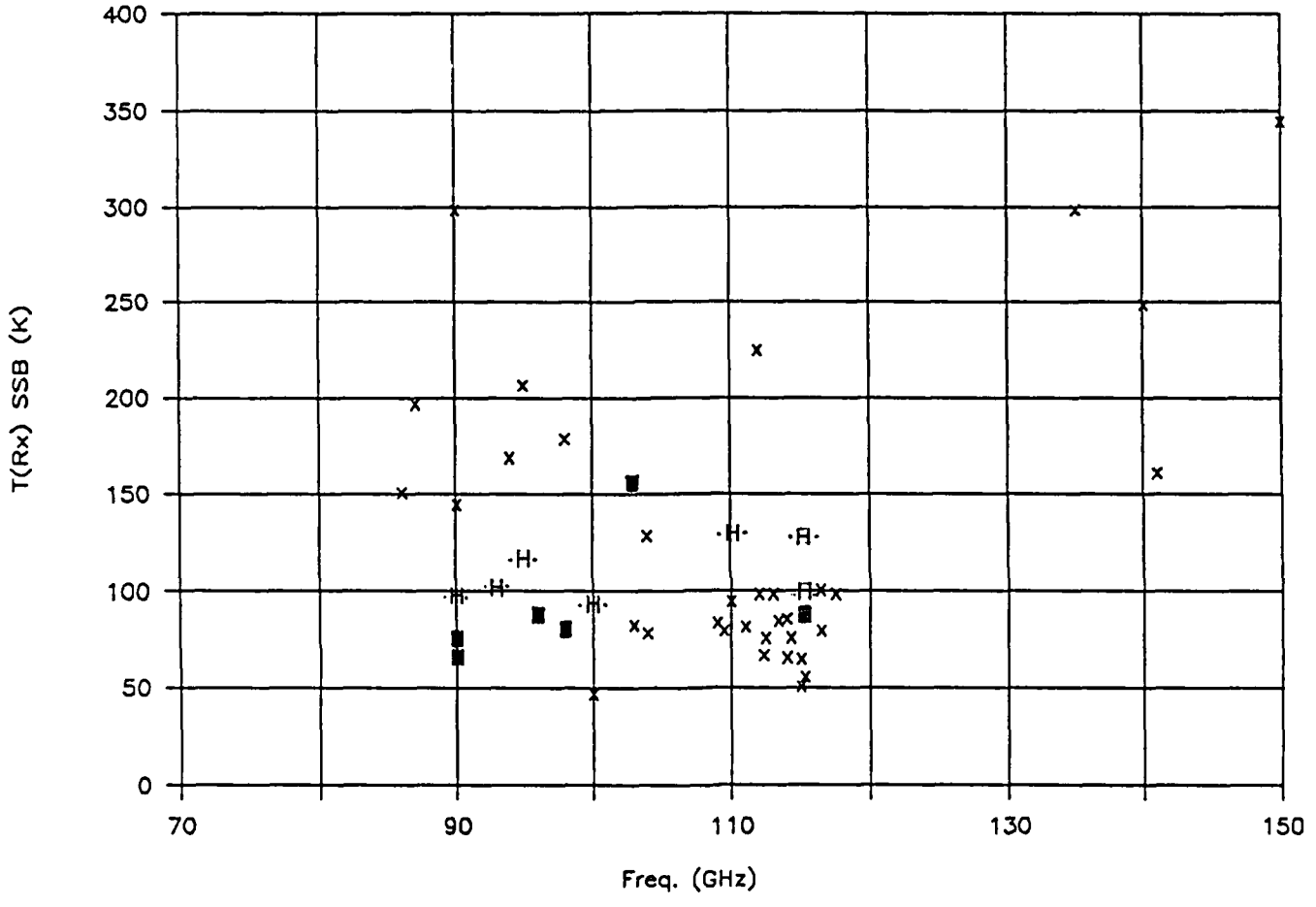


Fig. 13

Measured SSB receiver noise temperature near 100 GHz for HYPRES and similar SIS mixers. The temperature achieved with the shuuted junctions, as fabricated under the present program, was not quite as low as that achieved with a tunerless chip fabricated previously by HYPRES. This is believed to be due to the junction normal state resistance being too low on the shunted devices, producing poor (real part) inpedance matching.

red: = NRAO mixer with inductively shunted HYPRES junctions.
green: = NRAO mixer with un-shunted junctions from HYPRES wafer WN-430.

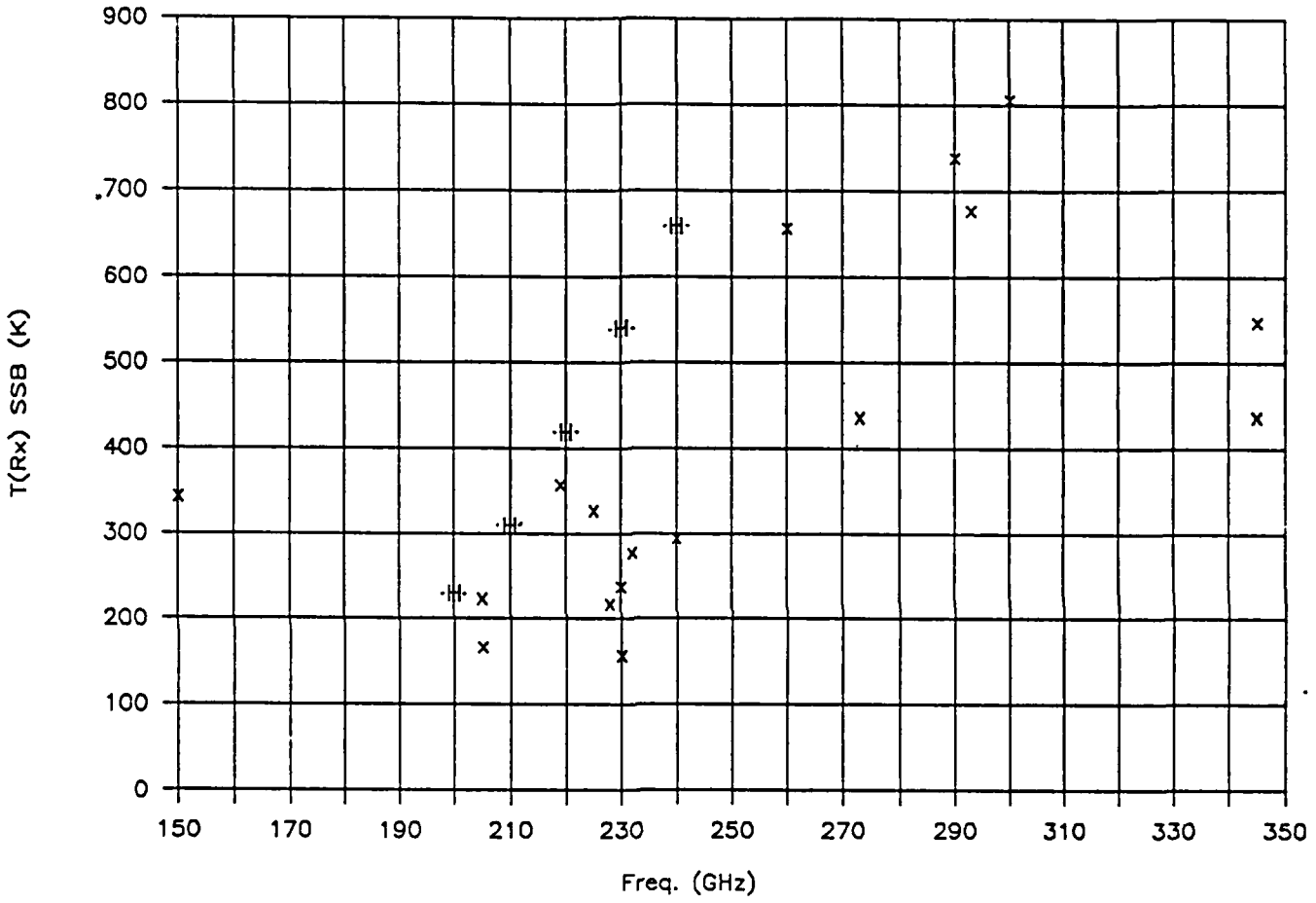


Fig. 14 Measured SSB receiver noise temperature near 215 GHz for HYPRES and similar SIS mixers.

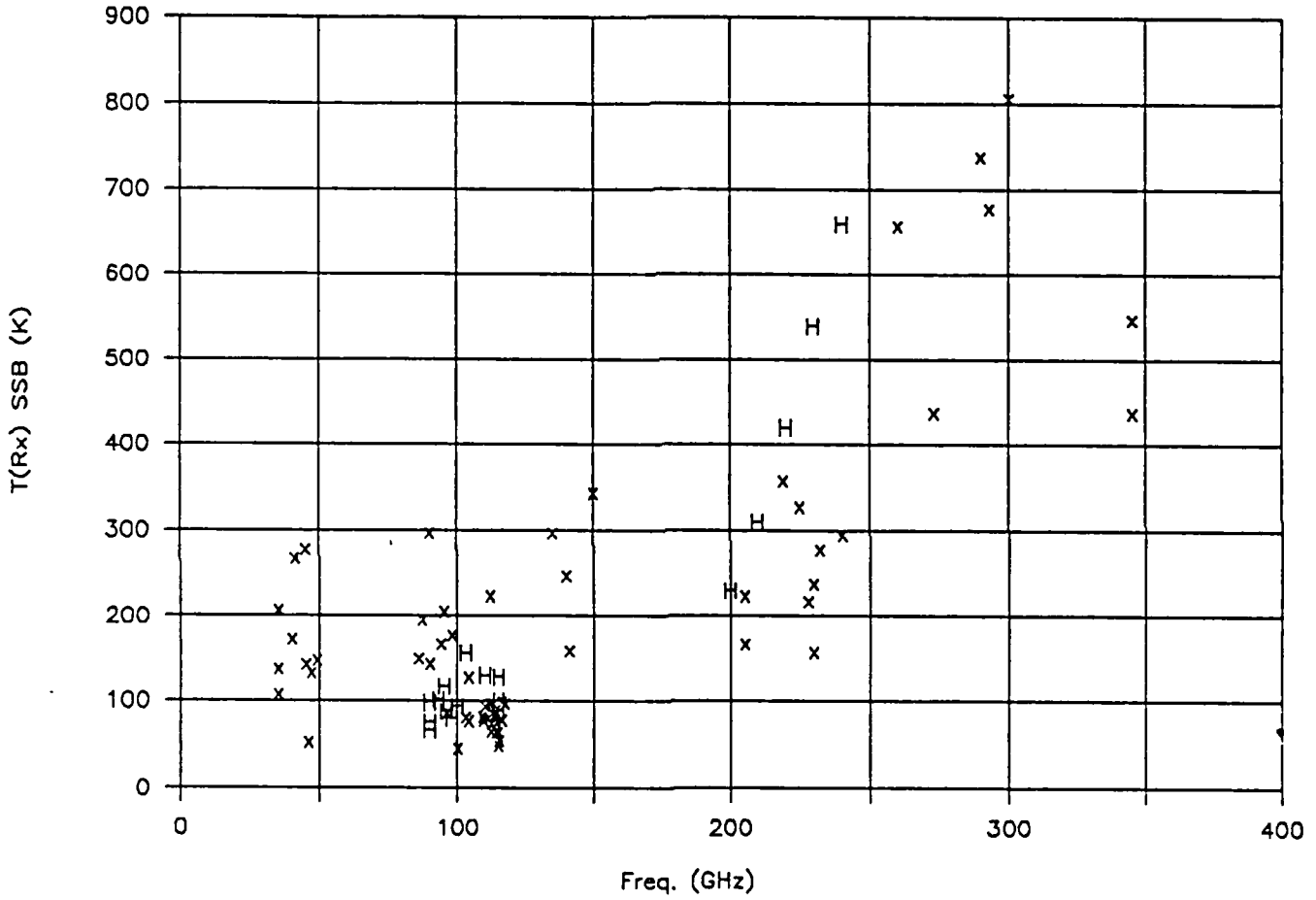


Fig. 15 The same data as shown in Figs. 13 and 14, combined on one scale. It should be stated that the non-HYPRES datapoints use Pb-alloy technology, which is more fragile mechanically. Figs. 13 - 15 were provided by NRAO.

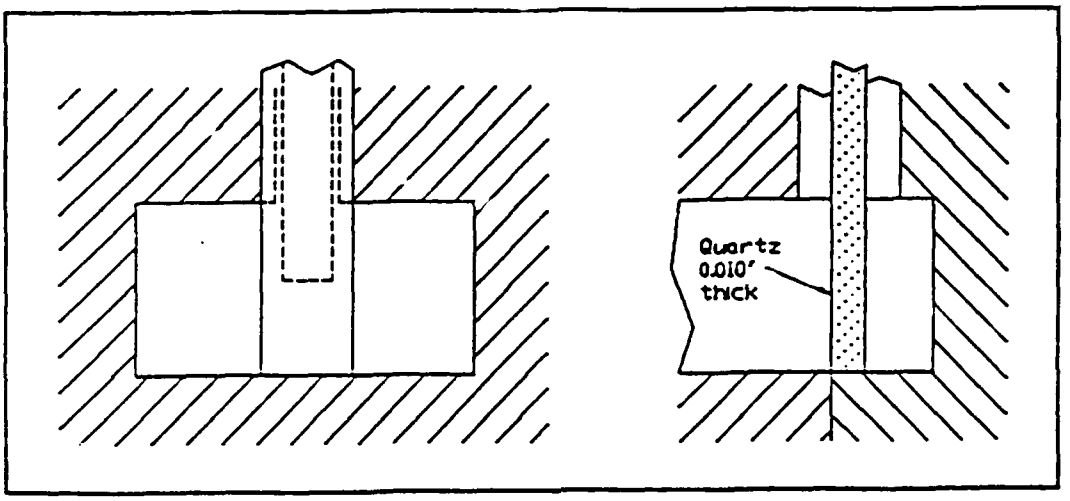


Fig. 16 Waveguide to suspended-substrate stripline transducer.

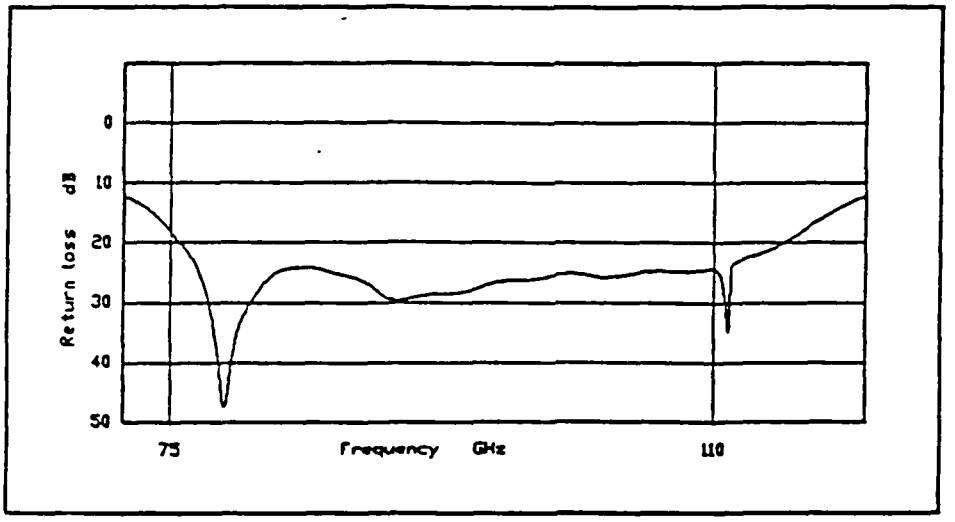


Fig. 17 Return loss of waveguide to suspended-substrate stripline transducer.

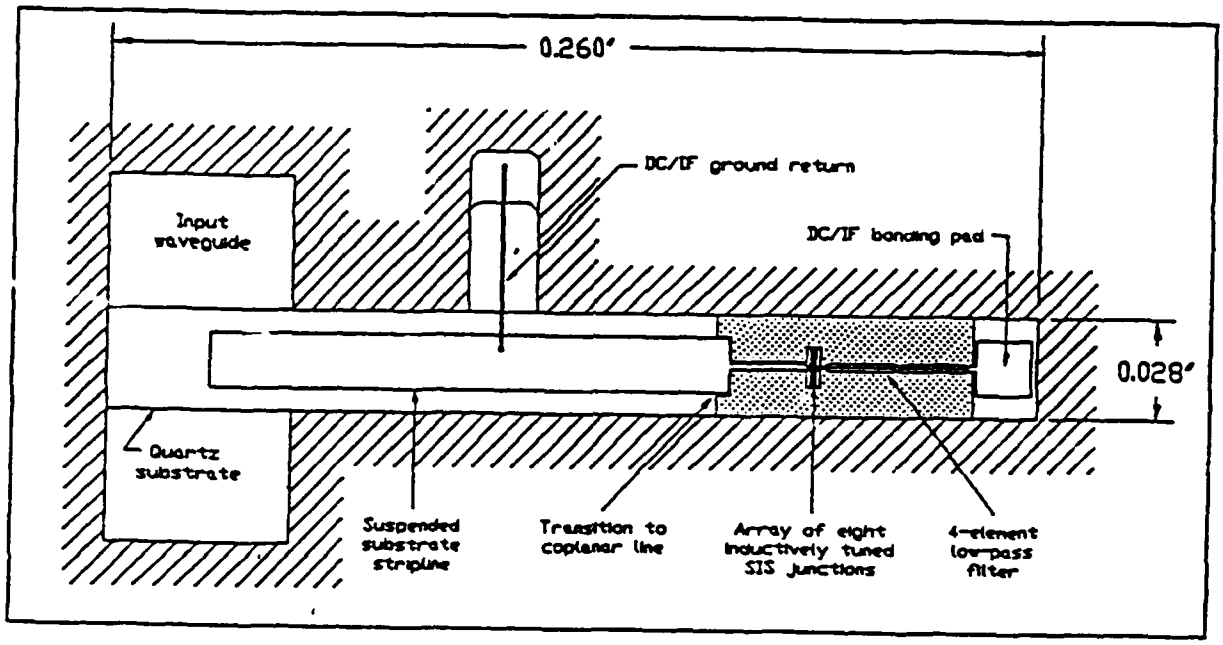


Fig. 18 The complete mixer, showing the waveguide to suspended-substrate stripline transducer, DC and IF ground return stub, and the coplanar mixer circuit.

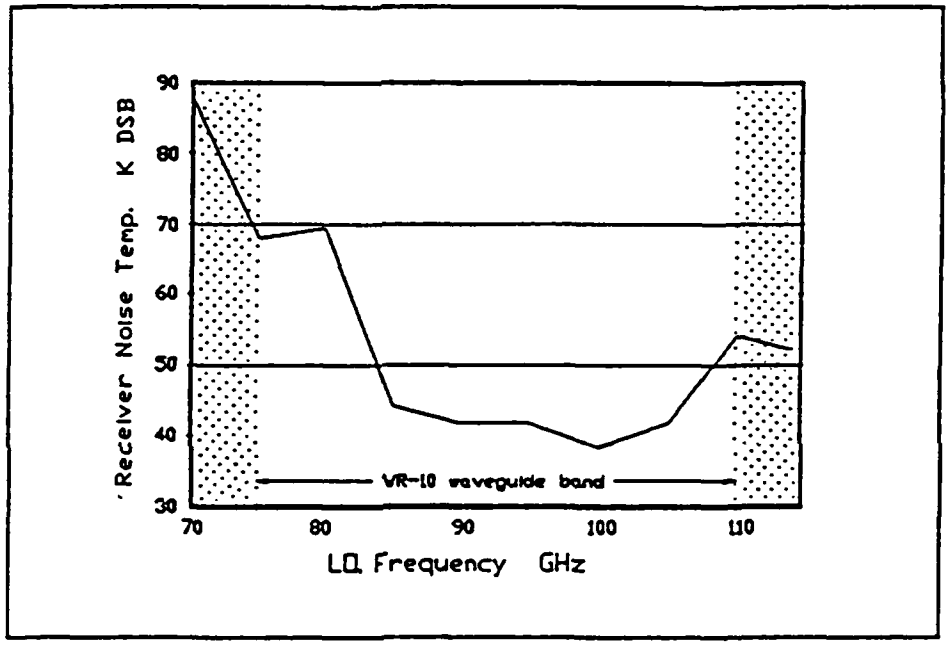


Fig. 19 DSB noise temperature of the SIS receiver with the fully integrated mixer. Measurements are referred to the mixer input flange.