



ORIGINAL FILE

4

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

VLSI PUBLICATIONS

A COHERENT VLSI DESIGN ENVIRONMENT

Final Technical Report for the period May 12, 1980 to December 31, 1987

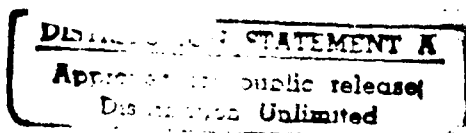
Massachusetts Institute of Technology
Cambridge, Massachusetts 02139

DTIC
ELECTE
AUG 02 1989
S D

Principal Investigators:

Paul Penfield, Jr. (617) 253-2506
Harold Abelson
Dimitri A. Antoniadis
William J. Dally
Clifton G. Fonstad
Lance A. Glasser
Thomas F. Knight, Jr.
F. Thomson Leighton
Charles E. Leiserson
Ronald L. Rivest
Michael F. Sipser
Gerald J. Sussman
Jacob K. White
John L. Wyatt, Jr.
Richard E. Zippel

AD-A210 953



This research was sponsored by Defense Advanced Research Projects Agency (DoD), through the Office of Naval Research under ARPA Order No. 3872, Contract No. N00014-80-C-0622.

89

Microsystems
Research Center
Room 39-321

Massachusetts
Institute
of Technology

Cambridge
Massachusetts
02139

Telephone
(617) 253-8138

TABLE OF CONTENTS

I.	Introduction	1
II.	Three-Dimensional Devices and Interconnections	2
III.	Heterostructure Logic Technology	3
IV.	VLSI Technology	4
V.	Timing Analysis of VLSI Interconnect	5
VI.	VLSI Architecture	6
VII.	SCHEME Chip	7
VIII.	VLSI Design Tools and Systems	8
IX.	PI: VLSI Placement and Routing	9
X.	The SCHEMA Design Environment	10
XI.	Integrated-Circuit Complexity Theory	11
XII.	VLSI Research Coordination	14
XIII.	Publications	16
Appendix A. VLSI Seminars, through December 1987		
Appendix B. Seminar Speaker Information Form		
Appendix C. Agendas, VLSI Research Reviews		
Appendix D. MIT VLSI Tools Release Information Letter and Form		
Appendix E. VLSI Memo Series, through December 1987		



Accession For	
NTIS CRA&I	☒
DTIC TAB	☐
Unannounced	☐
Justification	
By <i>per call ltr</i>	
Distribution/	
Availability Codes	
Dist	Avail and/or Special
<i>A-1</i>	

I. INTRODUCTION

The Microsystems Research Center of the Massachusetts Institute of Technology is pleased to submit this final report for contract N00014-80-C-0622, awarded by the Information Processing Technology Office (subsequently the Information Sciences Technology Office) of the Defense Advanced Research Project Agency, as monitored by the Office of Naval Research. The contract has been in force between May 12, 1980 and December 31, 1987. It was awarded to support research in several aspects of Very Large Scale Integrated (VLSI) systems.

The contract in question was a response to three successive, related proposals, as follows:

Advanced Research in VLSI, 12 May 1980 - 11 May 1982,
Theory and Practice for Large-Scale Systems, 12 May 1982 - 30 June 1984,
A Coherent VLSI Design Environment, 1 July 1984 - 31 December 1987.

During each of these three time periods a different underlying theme was emphasized, but the detailed technical work was carried out in several areas that continued throughout the life of the contract. This final report is organized according to those areas. In each case, the description below consists of a brief statement of the objectives of the work, a list of the major accomplishments, and some conclusions. A narrative style is not used, because of the scope of the contract and the large number of results. At the end of this report is a list of all publications that arose from work supported in part by this contract. The interested reader is referred to these publications for further information about any of the results listed below.

The following MIT faculty members helped perform the work done under this contract. The Principal Investigator for the entire time was Professor Paul Penfield, Jr.

Harold Abelson
Dimitri A. Antoniadis
William J. Dally
Clifton G. Fonstad
Lance A. Glasser
Thomas F. Knight, Jr.
F. Thomson Leighton
Charles E. Leiserson
Ronald L. Rivest
Michael F. Sipser
Gerald J. Sussman
Jacob K. White
John L. Wyatt, Jr.
Richard E. Zippel

II. THREE-DIMENSIONAL DEVICES AND INTERCONNECTIONS

This activity was carried out between 1980 and 1984. Contributions were made by Prof. Antoniadis and, to a small degree, Prof. Glasser.

Objective:

- To develop techniques for fabricating integrated circuits with more than one layer. It was thought that the circuits would provide increased density and, therefore, improved performance in integrated systems due to shorter average wire length.

Results:

- Partially self-aligned joint-gate CMOS transistor pair.
- Upside-down FET.
- Processes for recrystallization of amorphous silicon on an insulating substrate.
- Thermal analysis of recrystallization.
- Stacked CMOS latch.
- Silicon-on-insulator bipolar transistors.
- Design rules for stacked CMOS.
- Theoretical study of performance of stacked CMOS.
- Economic yield analysis of planar vs. two-layer circuits.

Conclusions:

- Two-layer MOS structures can be made and understood. Advances in our understanding of recrystallization are necessary. Apart for performance advantages, the economic motivation for two-layer processes is unclear, because the yield for an equivalent function is generally better if a one-layer process is used, even if this means partitioning the system into two chips.

III. HETEROSTRUCTURE LOGIC TECHNOLOGY

This activity was carried out between 1980 and 1984, but the work continues under other sponsorship. Professor Fonstad was responsible for this work.

Objective:

- To produce high-performance heterostructure transistors for logic applications. The speed advantage arises from the fact that high emitter efficiency can be maintained even with low-resistivity base material, through wider emitter bandgap. Quaternary compounds are used so that the band gap can be varied without changing the lattice spacing.

Results:

- Device simulator for heterojunction structures.
- Techniques for profiling of Be and Si ion implants into InGaAs.
- MBE-grown heterojunctions.
- Lateral pnp heterojunction transistors.
- Vertical npn heterojunction transistors.
- Argon arc lamp demonstrated for rapid thermal annealing of implanted III-Vs.
- Grown-junction npn transistors.
- Measurements of contact resistance on p-type (In,Ga)As.
- Triply implanted heterojunction npn bipolar transistors.
- Demonstration of polyimide passivation layer.

Conclusions:

- Grown-junction devices have better performance than triply implanted devices.
- Molecular beam epitaxy is a potentially superior growth technique for heterostructure devices.

IV. VLSI TECHNOLOGY

This activity was carried out through the entire length of the contract, from 1980 through 1987. Some related work continues under alternate sponsorship. The principal faculty contributors were Professors Glasser, and Knight.

Objective:

- To develop new circuit technology for high-performance digital systems.

Results:

- Transistor sizing program for optimizing size and speed.
- Generic CMOS pads, both 5 micron and 3 micron.
- High-speed digital CMOS FIR filter.
- High performance 32-word 24-bit content addressable memory.
- Chip with optical sensor array integrated with first stage of visual processing.
- Formal theory of tradeoff between noise margin and delay in digital circuits.
- Calibrated digital delay line implemented in VLSI.
- Continuous theoretical model of communication and computation in very massive, very fine grained computers.
- Spreadsheet for on-chip wire planning.
- Novel nonvolatile write-enabled UV PROM cell.
- Theory of fault-speed tradeoff in A/D converters.
- RELIC, circuit reliability simulators.
- Theory of fundamental limits of circuit high-frequency behavior (maximum frequency of oscillation).
- Zero-pin chip with magnetostatic power, clock, and signal coupling.

Conclusions:

- A variety of novel devices, circuits, and circuit simulation programs were developed. This activity provided a context in which the other work done under this contract could be done more imaginatively.
- Novel basic circuits can be invented, designed, and developed only in the context of associated with in devices and architectures.

V. TIMING ANALYSIS OF VLSI INTERCONNECT

This activity was carried out between 1981 and 1987. The faculty members involved were Professors Wyatt, Penfield, and Glasser.

Objective:

- To develop models, approaches, and CAD tools to analyze delay performance of VLSI chips and systems.

Results:

- RSIM, a program to estimate delay using switch-level models.
- Incorporation of capacitance and line delay into communication-cognizant gate-level simulators.
- Retiming technique for optimizing sequential circuits at the register level.
- RC tree model for on-chip MOS interconnect.
- Waveform bounding of signal propagation through RC trees.
- Extension of waveform bounding to RC meshes.
- Incorporation of slew rate limits into waveform bounding results.
- Extension of waveform bounding to ECL bipolar circuits.
- Extension to results to a large class of dynamic systems.
- Limited success in incorporation of distributed inductance in interchip PC-board interconnects.
- Analysis tool incorporating waveform relation along with waveform bounding.
- Transfer of waveform bounding tools to industry (Tangent Systems).
- Extension of waveform bounding to include leaky capacitors.
- Transfer of ECL timing analyzer to industry (Digital Equipment Corporation).

Conclusions:

- Waveform bounding is a useful tool in the VLSI CAD arena.
- Most designers prefer approximation, rather than bounding tools.

VI. VLSI ARCHITECTURE

This activity was carried out through the length of the contract, from 1980 through 1987.

The faculty members concerned with VLSI architecture were Professors Sussman, Knight, Dally, Leiserson, and Zippel.

Objective:

- To develop parallel architectures that take advantage of the capabilities of VLSI.

Results:

- The connection machine, a massively parallel architecture with small grain size and hypercube interconnection network.
- Transfer of the connection machine to industry (Thinking Machines, Inc.).
- Fat-trees, an interconnection network that is area-universal.
- Message-Driven Processor, a fine-grain, message-passing concurrent computer.
- Theory of performance of k-ary n-cube interconnection networks.
- Bidirectional Torus Router, a self-timed multicomputer communication chip.
- JOSS, an operating system for a large-scale message-passing multicomputer.
- Network Design Frame, a high-performance router incorporated into a chip pad frame.
- Reconfigurable Arithmetic Processor architecture, for nibble-serial arithmetic.
- Chip incorporating the reconfigurable arithmetic processor.

Conclusions:

- Many different highly parallel architectures are possible.
- To be useful, a parallel architecture must simultaneously address issues of communication topology, communication circuits, processor performance, operating system, and appropriate message or communication semantics.

VII. SCHEME CHIP

This activity took place between 1980 and 1984, under the supervision of Professor Sussman. Contributions were made by Professors Knight, Leiserson, Rivest, and Zippel.

Objective:

- To design and fabricate an integrated system that directly implements the Lisp dialect SCHEME.

Results:

- SCHEME-79 Microprocessor chip designed, fabricated, and tested.
- Concurrent efficient garbage collections algorithm.
- SCHEME-81 Microprocessor chip designed, fabricated, and tested.
- Prototype SCHEME single-board processor designed, fabricated, and tested.

Conclusions:

- The SCHEME-81 chip was designed using Lisp-based design tools and the project forced advances in all tool areas. The final chip was functional.
- Microcode design and generation was a significant part of the design, and new design tools were necessary.
- The philosophy behind the SCHEME chips is to embed much of the language supported in hardware. This is opposed to the RISC computer architecture strategy, in which the processor is made "lean and mean," and the language support is in compilers.

VIII. VLSI DESIGN TOOLS AND SYSTEMS

This activity occurred during the entire length of the contract, from 1980 through 1987.

Faculty members involved are Professors Sussman, Abelson, Glasser, Knight, Rivest, Wyatt, White, and Penfield.

Objective:

- To produce tools to support design of VLSI systems.

Results:

- LISPIC, Lisp-based data base for IC design data.
- DAEDALUS, interactive graphics editor for IC layouts.
- DPL, Design Procedure Language, tool to create and manage a representation of an IC design.
- PI, system for placement and interconnect (see section below).
- SCHEMA, IC design environment (see section below).
- DRC, design-rule check program.
- ESIM, switch-level simulator.
- AIDS, APL-based layout capture and editing system.
- RSIM, switch-level timing simulator.
- CMTPG, connection-machine based test pattern generator.
- RELIC, reliability simulator.

Conclusions:

- Many useful VLSI design tools have come out of this contract. Most have been installed and used elsewhere.
- Two of the design systems have been extensive and involved significant research as well as development. These are the PI and SCHEMA systems described in later sections of this report.

IX. PI: VLSI PLACEMENT AND ROUTING

This activity was performed between 1980 and 1984, under the supervision of Professor Rivest. Help came from Professors Knight, Leighton, Leiserson, Sipser, and Zippel. It culminated in the release of a tape incorporating the PI system, suitable for use on a Symbolics Lisp machine.

Objective:

- To develop new algorithms for placement and interconnect routing of VLSI chips.
- To incorporate the best algorithms available, including new ones, into a working placement and routing system.

Results:

- Implementation of existing routing algorithms in one framework.
- Heuristic approach to chip partitioning and module placement.
- Power and ground routing algorithm.
- A random circuit generator for testing PI algorithms.
- Pad placement algorithm.
- Polynomial-time algorithms for certain channel routing problems.
- Interfaces to other VLSI design and layout tools.
- Theory of efficient, optimal crossing placement.
- Technique for estimating routing channel densities.
- Efficient river-routing algorithm.
- Transfer of the PI system to industry.
- Tape made for PI system distribution to North American companies and universities.

Conclusions:

- A practical design system can motivate fundamental research in algorithms.
- Lisp is a fine language, and Lisp Machines are a fine environment, for research projects, but technology transfer of the tools themselves is difficult because not many potential target sites use Lisp machines for design of VLSI chips.

X. THE SCHEMA DESIGN ENVIRONMENT

The SCHEMA system was under development between 1982 and 1986. The principal faculty member behind this system was Professor Zippel. He was helped by Professor Glasser. An industrial visitor from Harris Corporation, George Clark, participated in the research and directed complementary developments in his company.

Objective:

- Design and develop an environment for VLSI CAD tools with extraordinarily ambitious capabilities for consistency maintenance in the face of design changes in any level.
- Demonstrate effectiveness of industrial partnerships in CAD software.

Results:

- Low-level databases designed and implemented, supporting hierarchical and semi-hierarchical design specifications and multiple views.
- Waveform language defined.
- Capsule system designed and implemented.
- Schematic capture tools integrated.
- Wirewrap/PC-board development tool designed at Harris.
- Temporal constraint tools incorporated into SCHEMA.
- Simulation interface installed in SCHEMA.
- CIF output module written.
- SCHEMA successfully used to design chips.
- Multiport circuit analysis package incorporated.
- Transfer to industry completed.

Conclusions:

- The system was, as originally planned, too complex and too ambitious for a university project.
- The basic structure and concepts were successfully transferred to Harris Corporation and subsequently to MCC.

XI. VLSI THEORY

A large portion of the contract dealt with VLSI theory in many forms -- VLSI complexity theory, routing theory and algorithms, the theoretical basis for CAD tools, parallel algorithms, etc. The faculty involved in the theoretical studies were Professors Abelson, Glasser, Leighton, Leiserson, Rivest, and Sipser.

Objective:

- To determine fundamental limits of operation of VLSI systems.
- To determine theoretical bounds for VLSI CAD tools.
- To devise improved routing algorithms and parallel algorithms for multiprocessor VLSI systems.

Results:

- Study of the capabilities of a dynamically reconfigurable tree structure.
- Area-time tradeoff limit for any circuit that computes a quadratic form.
- Information-transfer limits to distributed data bases, for both one-way and two-way communication.
- Incorporation of parasitic electrical parameters into Thompson's VLSI model.
- Minimum length of the longest edge in a VLSI layout.
- General transformation for improving performance of synchronous circuits by removing combinational rippling.
- Asymptotically optimal layout for the shuffle-exchange graph.
- Optimal layouts for small shuffle-exchange graphs.
- Register-minimization procedure.
- Limits on multilevel wiring complexity for interconnect.
- Algorithm for contact minimization in VLSI layouts.
- Fundamental limits of channel routing.
- Optimal organization of raster-graphics memory.
- Efficient algorithms for optimal clock phase assignment.
- One-dimensional systolic array wiring in wafer-scale integration with finite yield.
- Two-dimensional systolic array wiring in wafer-scale integration with finite yield.
- Fast algorithms for river routing.
- Fast algorithms for channel routing.
- Articulation of many high-level architectural transformations.
- Algorithm for estimating routing channel densities.
- Layout compactor with automatic jog insertion.
- Polynomial-time algorithm for orienting rectangles in slicing VLSI floorplans.
- Demonstration that ability to place transistors (as opposed to only wires) on multiple layers does not decrease the volume needed to embed a circuit in a chip.
- Linear-time approximation algorithm for Manhattan routing.
- Algorithm for determining routability from a sketch of the layer and fixed module placements.
- Compact layouts for complex arithmetic functions.

- Fast algorithms for data routing and sorting in large-scale networks.
- Efficient algorithm for single-layer routing of a VLSI chip.
- Space-efficient optimal time scanning algorithm for finding the connected components of rectangles in the plane.
- High-average-efficiency graph bisection algorithm.
- Class of universal networks that can simulate all other networks of the same size with logarithmically longer delay.
- Techniques for converting 2-dimensional layouts into 3-dimensional layouts with substantially less material volume.
- Analysis techniques for packing heuristics.
- Proof that any planar graph can be represented on 9 stacks.
- Fat-trees, a new class of universal routing networks for parallel processing.
- Algorithms designed specifically for execution on a fat-tree.
- Fat-tree software simulator.
- Systolic array simulator.
- Efficient algorithms for representing useful networks as a small number of stacks of wires.
- Efficient circuits for parallel division.
- Improved algorithms for two-layer channel routing.
- Probabilistic algorithm for on-line routing of messages on a fat-tree.
- Provably fast algorithm for solving constraint systems in VLSI layout compaction.
- Timing scheme for transmitting messages between processors in a fat-tree.
- Implementation of nMOS VLSI fat-tree network interface.
- Implementation of a hyperconcentrator switch for routing bit-serial messages in highly parallel routing networks.
- Good message-routing algorithms for various universal networks.
- Distributed Random-Access Machine (DRAM) model for routing networks for parallel computation.
- Compact barrel shifter.
- Efficient parallel algorithm for maximum flow on a network.
- Improved methods for graph bisection.
- Improved algorithm for routing 2-point nets on a channel, with vertical overlaps and knock-knees in two layers.
- Efficient embedding of arbitrary binary trees in a hypercube.
- Nearly optimal algorithms and bounds for multilayer channel routing.
- Methods to configure a functioning network from a larger network of the same kind that contains random faults.
- Efficient algorithm for verifying the correct operation of a computation on a level-clocked synchronous circuit.
- Modular layouts for area- and volume-universal fat-trees with constant size switches.
- Intelligent backtracking algorithms for pure Prolog.
- Parallel algorithms for graph coloring problems and maximal independent set problems.
- Efficient algorithms for creating systolic arrays from wafer-scale circuits with faults, useful for small to moderate size systems.

- Efficient hash functions for many-one routing on a hypercube.
- Embedding of a mesh-of-trees network in a hypercube.
- Parallel algorithm for contraction of n -node bounded-degree planar graphs.
- Algorithm for determining the minimum-cost flow in a network, based on a new successive-approximation technique.
- Simulation of a hypercube by a shuffle-exchange graph or butterfly network.
- Efficient parallel algorithms for symmetry-breaking in sparse graphs of processors.
- Efficient parallel algorithm for planarity.
- Technique to implement scan operations in hardware.
- Methods to analyze circuits with periodic clocking waveforms.
- Deterministic, on-line message-routing algorithm for a butterfly fat-tree network.
- Concurrent-read, concurrent-write DRAM algorithms that are faster than exclusive-read, exclusive-write DRAM algorithms.
- Improved algorithms for contraction of n -node bounded-degree planar graphs.
- Correspondence between bussed permutation architectures and difference covers for permutation sets.
- Rigorous treatment of general river routing problems, including necessary and sufficient conditions for routability, and efficient methods for constructing optimal routings.
- Improved algorithms for coloring and matching sparse graphs.
- Fast local deterministic algorithms for reconfiguration of the working nodes in a partially faulty hypercube where both nodes and edges may be faulty.
- Space-efficient techniques for queue management in very large scale networks.
- Algorithm to determine thepagenumber of a graph.
- Polynomial-time approximation algorithm for finding optimal separators in planar graphs.

Conclusions:

- Many advances in theory related to VLSI have been made.
- A theoretical basis for understanding message passing in a complex large parallel computer is beginning to exist.
- Models which account for the cost of communication as well as the cost of computation have been introduced and used.
- VLSI theory is best done in the context of an active effort in the theory of computation and an active effort in VLSI architecture and technology.

XII. VLSI RESEARCH COORDINATION AND OUTREACH

For the entire length of the contract, from 1980 through 1987, an explicit task was to coordinate the VLSI research on campus, promote new VLSI research, and generate technology transfer through outreach programs. This activity has been carried out by Professor Penfield with assistance from all the other faculty. During the length of this contract the total research volume in VLSI rose from an estimated \$3,000,000 to over \$10,000,000, and a state-of-the-art VLSI fabrication facility costing in excess of \$23,000,000 was established.

Objective:

- To foster VLSI research at MIT in a number of areas.
- To broaden the perspective of those doing VLSI research so they can seek connections to other research activities and applications.
- To instill a sense of community in those doing VLSI research on campus.
- To inform other universities and companies in North America about our research program and results.

Results:

- Weekly VLSI Seminar series. Appendix A gives a list of seminar speakers from the beginning of the series (just prior to the start of this contract) through the end of the contract. This series has attracted an outstanding set of speakers and an outstanding audience, and has an international reputation. The audience comes from MIT, local industry, local universities, and even from a distance. The latest version of the information sheet for authors is reproduced as Appendix B.
- Semiannual VLSI Research Review. This all-day affair covers all technical areas in VLSI, and is an excellent experience for the students who speak. A collection of agendas is reproduced as Appendix C.
- VLSI Tools tape. This Unix-based tape includes miscellaneous VLSI tools, many of which were developed under this contract. It is available to other universities and industry within North America. A description appears as Appendix D.
- VLSI Memo series. This series started in 1980 and, as of the termination date of this contract, included 96 memos from all areas of VLSI research. Support by this contract has permitted the distribution of single copies, for personal use, to people in North America, without charge. This series has been very effective in aiding technology transfer. A list of titles through the end of this contract appears as Appendix E.
- VLSI Conference. The university-oriented VLSI conference has been held at MIT in even-numbered years starting in 1980. Although the conference is financially self-sustaining and benefits from a small NSF grant, it is administered by the MIT Microsystems Research Center (MRC), which is the organization that carries out the rest of the outreach activities described in this section. The existence and stability of MRC has helped MIT serve a leadership and continuity role for this conference.

Conclusions:

- The presence of an organization charged with explicitly fostering VLSI research has helped the overall MIT research program in all areas of VLSI immensely.
- The outreach activities supported in part by this contract have been effective in acquainting people outside MIT with our overall research program.

XIII. PUBLICATIONS

L. A. Glasser and P. Penfield, Jr., "An Interactive PLA Generator as an Archetype for a New VLSI Design Methodology," *Proceedings, IEEE International Conference on Circuits and Computers*, Port Chester, New York, October 1-3, 1980; pp. 608-611; also MIT VLSI Memo No. 80-25, July 1980.

G. J. Sussman, J. Holloway, and T. F. Knight, Jr., "Design Aids for Digital Integrated Systems, an Artificial Intelligence Approach," *Proceedings, IEEE International Conference on Circuits and Computers*, Port Chester, New York, October 1-3, 1980; pp. 612-615.

P. Penfield, Jr., J. Rubinstein, and M. A. Horowitz "Signal Delay in RC Tree Networks," *Proceedings, Second Caltech Conference on Very Large Scale Integration*, Pasadena, California, January 19-21, 1981; also, MIT VLSI Memo No. 80-41, January 1981. Later version appeared in *IEEE Transactions on Computer-Aided Design*, Vol CAD-2, No. 3, July 1983; pp. 202-211.

J. J. Cherry and G. L. Roylance, "A One Transistor RAM for MPC Projects," *Proceedings, Second Caltech Conference on Very Large Scale Integration*, Pasadena, California, January 19-21, 1981; also, MIT VLSI Memo No. 81-43, February 1981.

J. C. Ong, *An Iterative Solution to Poisson's Equation for Doped Heterostructure Devices*, B.S. Thesis, MIT, Department of Electrical Engineering and Computer Science, June 1981; also MIT VLSI Memo No. 82-84, March 1982.

M. W. Geis, B.-Y. Tsaur, J. C. C. Fan, D. J. Silversmith, R. W. Mountain, J. P. Donnelly, E. W. Maby, and D. A. Antoniadis, "High-Quality MOSFETs on Silicon Films Prepared by Zone Melting Recrystallization of Encapsulated Polysilicon on SiO₂," *39th Annual Device Research Conference*, Santa Barbara, California, June 22-24, 1981; abstract also in *IEEE Transactions on Electron Devices*, vol. ED-28, no. 10, October 1981; pp. 1255-1256.

J. Allen and P. Penfield, Jr., "VLSI Design Automation Activities at MIT," *IEEE Transactions on Circuits and Systems*, vol. CAS-28, no. 7, July 1981; pp. 645-653; also MIT VLSI Memo No. 80-33, July 1981.

G. J. Sussman, J. Holloway, G. L. Steele, Jr., and A. Bell, "SCHEME-79--LISP on a Chip," *Computer*, Vol. 14, no. 7, July 1981; pp. 10-21. Preliminary version appeared as MIT VLSI Memo No. 80-6, January 1980.

J. Batali, N. Mayle, H. Shrobe, G. J. Sussman, and D. Weise, "The DPL/Daedalus Design Environment," *Proceedings, First International Conference on Very Large Scale Integration*, Edinburgh, U. K., August 18-21, 1981; pp. 183-292; and appeared in *VLSI, Very Large Scale Integration*, John P. Gray, ed., Academic Press, London, 1981.

F. T. Leighton and G. L. Miller, "Optimal Layouts for Small Shuffle-Exchange Graphs," *Proceedings, First International Conference on Very Large Scale Integration*, Edinburgh, U. K., August 18-21, 1981; pp. 289-299; and appeared in *VLSI, Very Large Scale Integration*, John P. Gray, ed., Academic Press, London, 1981; also MIT VLSI Memo No. 81-58, August 1981.

A. E. Baratz, *Algorithms for Integrated Circuit Signal Routing*, Ph.D. Thesis, MIT, Department of Electrical Engineering and Computer Science, August 1981; also MIT VLSI Memo No. 83-151, October 1983.

K. Tabatabaie-Alavi, R. Markunas, J. Ong, and C. G. Fonstad, "Fabrication and Characterization of Abrupt p+n InGaAs/InP Heterojunctions," *Proceedings, 1981 International Symposium on Gallium Arsenide and Related Compounds*, Oiso, Japan, September 21-23, 1981.

- F. T. Leighton, *Layouts for the Shuffle-Exchange Graph and Lower Bound Techniques for VLSI*, Ph.D. Thesis, MIT, Department of Mathematics, September 1981; also MIT VLSI Memo No. 82-103, June 1982.
- D. W. Weise, *Exploiting Hierarchy in the Analysis of VLSI Systems*, M.S. Thesis, MIT, Department of Electrical Engineering and Computer Science; also MIT VLSI Memo No. 82-104, June 1982.
- F. M. Rose, *Models for VLSI Circuits*, M.S. Thesis, MIT, Department of Electrical Engineering and Computer Science; also MIT VLSI Memo No. 82-114, July 1982.
- C. E. Leiserson and R. Y. Pinter, "Optimal Placement for River Routing," *CMU Conference on VLSI Systems and Computations*, Pittsburgh, Pennsylvania, October 19-21, 1981; pp. 126-142; Appeared in *VLSI Systems and Computations*, H. T. Kung, B. Sproull, and G. Steele, eds., Computer Science Press, Rockville, Maryland, 1981; also MIT VLSI Memo No. 81-66, 1981.
- R. L. Rivest, A. E. Baratz, and G. L. Miller, "Provably Good Channel Routing Algorithms," *CMU Conference on VLSI Systems and Computations*, Pittsburgh, Pennsylvania, October 19-21, 1981; pp. 153-159; Appeared in *VLSI Systems and Computations*, H. T. Kung, B. Sproull, and G. Steele, eds., Computer Science Press, Rockville, Maryland, 1981.
- R. Y. Pinter, "Optimal Routing in Rectilinear Channels," *CMU Conference on VLSI Systems and Computations*, Pittsburgh, Pennsylvania, October 19-21, 1981; pp. 160-177; Appeared in *VLSI Systems and Computations*, H. T. Kung, B. Sproull, and G. Steele, eds., Computer Science Press, Rockville, Maryland, 1981.
- D. J. Brown and R. L. Rivest, "New Lower Bounds for Channel Width," *CMU Conference on VLSI Systems and Computations*, Pittsburgh, Pennsylvania, October 19-21, 1981; pp. 175-185; Appeared in *VLSI Systems and Computations*, H. T. Kung, B. Sproull, and G. Steele, eds., Computer Science Press, Rockville, Maryland, 1981.
- P. Penfield, Jr., "AIDS, APL Integrated-Circuit Design System," *APL 1981 Conference Proceedings*, San Francisco, California, October 21-23, 1981; and *APL Quote Quad*, Vol. 12, no. 1, September 1981; pp. 240-247; also MIT VLSI Memo No. 81-57, July 1981.
- P. Penfield, Jr., "Principal Values and Branch Cuts in Complex APL," *APL 1981 Conference Proceedings*, San Francisco, California, October 21-23, 1981; and *APL Quote Quad*, Vol. 12, no. 1, September 1981; pp. 248-256; also MIT VLSI Memo No. 81-57, July 1981.
- F. T. Leighton, "New Lower Bound Techniques for VLSI," *Proceedings, 22nd Annual Symposium on Foundations of Computer Science*, Nashville, Tennessee, October 28-30, 1981; pp. 1-12; also MIT VLSI Memo No. 82-89, March 1982. Later version appeared in *Math Systems Theory*, Vol. 17, no. 1, April 1984; pp. 47-70.
- C. E. Leiserson and J. B. Saxe, "Optimizing Synchronous Systems," *Proceedings, 22nd Annual Symposium on Foundations of Computer Science*, Nashville, Tennessee, October 28-30, 1981; pp. 23-36; also MIT VLSI Memo No. 82-90, March 1982.
- E. W. Maby, M. W. Geis, Y. L. LeCoz, D. J. Silversmith, R. W. Mountain, and D. A. Antoniadis, "MOSFETs on Silicon Prepared by Moving Melt Zone Recrystallization of Encapsulated Polycrystalline Silicon on an Insulating Substrate," *IEEE Electron Device Letters*, Vol. EDL-2, no. 10, October 1981; pp. 241-243; also MIT VLSI Memo No. 81-49, May 1981.
- R. Y. Pinter, "On Routing Two-Point Nets Across a Channel," *Proceedings, 19th Design Automation Conference*, Las Vegas, Nevada, June 14-16, 1982; also MIT VLSI Memo No. 82-99, April 1982.

- N. J. Slater, A. N. M. M. Choudhury, K. Tabatabaie-Alavi, W. Rowe, C. G. Fonstad, K. Alavi, and A. Y. Cho, "Ion Implantation Doping of In,Ga As and In,Al As," *Proceedings of the 1982 International Symposium on Gallium Arsenide and Related Compounds*, September 1982, pp. 627-634; also MIT VLSI Memo No. 82-125, November 1982.
- N. J. Slater, *Ion Implantation of Be and Si for GaInAs/AlInAs/InP Bipolar Heterojunction Transistors*, M. S. Thesis, MIT, Department of Electrical Engineering and Computer Science; also MIT VLSI Memo No. 82-122, November 1982.
- L. A. Glasser and P. Penfield, Jr., "VLSI Circuit Theory," *Proceedings, Large Scale Systems Symposium*, Virginia Beach, Virginia, October 11-13, 1982, pp. 499-501; also MIT VLSI Memo No. 82-115, August 1982.
- K. Tabatabaie-Alavi, A. N. M. M. Choudhury, K. Alavi, J. Vlcek, N. J. Slater, C. G. Fonstad, and A. Y. Cho, "In,GaAs/In,AlAs Heterojunction Lateral PNP Transistors," *Technical Digest, 1982 International Electron Devices Meeting*, San Francisco, California, December 13-15, 1982, pp. 766-769; also MIT VLSI Memo No. 82-123, November 1982.
- K. Tabatabaie-Alavi, A. N. M. M. Choudhury, K. Alavi, J. Vlcek, N. J. Slater, C. G. Fonstad, and A. Y. Cho, "Ion-Implanted $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ Lateral PNP Transistors," *IEEE Electron Device Letters*, Vol. EDL-3, no. 12, December 1982, pp. 379-381; also MIT VLSI Memo No. 82-124, November 1982.
- T. Roussos, B. B. Mikic, D. A. Antoniadis, and E. W. Maby, "Temperature Distribution in a Plate Produced by a Moving Heat Source," *AIAA 21st Aerospace Sciences Meeting*, Reno, Nevada, January 10-13, 1983.
- K. Tabatabaie-Alavi, A. N. M. M. Choudhury, N. J. Slater, J. Vlcek, W. Lee, and C. G. Fonstad, "Heterojunction Bipolar Transistor Technology for InP Based Compounds," *Compendium of the Second NATO Workshop on the Materials Aspects of Indium Phosphide*, Lancaster, England, March 28-30, 1983.
- T. N. Bui, *On Bisecting Random Graphs*, M. S. Thesis, MIT, Department of Electrical Engineering and Computer Science; also MIT VLSI Memo No. 83-136, February 1983.
- D. Kleitman, F. T. Leighton, Margaret Lepley, and Gary L. Miller, "An Asymptotically Optimal Layout for the Shuffle-Exchange Graph," *Journal of Computer and System Sciences*, March, 1983.
- S. Bhatt, B. Baker, and F. T. Leighton, "An Approximation Algorithm for Manhattan Routing," *Proceedings of the 15th ACM Symposium on Theory of Computing*, Boston, April 1983; also MIT VLSI Memo No. 82-129, December 1982.
- R. E. Zippel, "Capsules," *Proceedings of SIGPLAN '83*, June 1983.
- F. Chung, F. T. Leighton, and A. Rosenberg, "Diogenes: A Methodology for Designing Fault-Tolerant VLSI Processor Arrays," *IEEE Fault-Tolerant Computing*, Italy, Summer 1983; also MIT VLSI Memo No. 83-142, April 1983.
- R. E. Zippel, "An Expert System for VLSI Design," *Proceedings of International Symposium on Circuits and Systems*, Newport Beach, California, May 1983; also MIT VLSI Memo No. 83-134, February 1983.
- F. T. Leighton, "Parallel Computation Using Meshes of Trees," *Proceedings, 1983 International Workshop on Graph Theoretic Concepts of Computer Science*, Osnabruck, West Germany, June, 1983; and *Proceedings, 1983 Workshop on Graph Theoretic Concepts in Computer Science*, ed., by M. Nagl and J. Perl, Trauner Verlag, Linz, W. Germany, October 1983; pp. 200-218; also MIT VLSI Memo No. 83-152, October 1983.

- M. Rodder and D. A. Antoniadis, "Silicon-On-Insulator Bipolar Transistors," *IEEE Electron Device Letters*, EDL-4, No. 6, June 1983, pp. 193-195.
- A. S. Moulton, "Laying the Power and Ground Wires on a VLSI Chip," *ACM IEEE 20th Design Automation Conference Proceedings*, Miami Beach, Florida, June 27-29, 1983, pp. 754-755.
- J. L. Wyatt, Jr., "A New Approach to Timing Analysis of Digital MOS IC's," *Twenty-Sixth Midwest Symposium on Circuits and Systems*, Puebla, Mexico, August 15-16, 1983; also MIT VLSI Memo No. 83-147, July 1983.
- A. N. M. M. Choudhury, W. Rowe, K. Tabatabaie-Alavi, C. G. Fonstad, K. Alavi and A. Y. Cho, "Ion Implantation of Si and Be in $\text{Al}_{0.48}\text{In}_{0.52}\text{As}$," *Journal of Applied Physics*, 54, No. 8, August 1983, pp. 4374-4377.
- A. N. M. M. Choudhury, K. Tabatabaie-Alavi, C. G. Fonstad, and J. C. Gelpey, "Rapid Thermal Annealing of Se and Be Implanted in InP Using an Ultrahigh Power Argon Arc Lamp," *Applied Physics Letters* 43, No. 4, August 15, 1983, pp. 381-383.
- F. T. Leighton, *Complexity Issues in VLSI: Optimal Layouts for the Shuffle-Exchange Graph and Other Networks*, MIT Press, Cambridge, MA, September 1983.
- M. Rodder, *Silicon-On-Insulator Bipolar Transistors*, M. S. Thesis, Department of Electrical Engineering and Computer Science, MIT, September 1983.
- E. W. Maby, H. A. Atwater, and A. L. Keigler, "Electron-Beam Induced Current Measurements in Silicon-On-Insulator Films Prepared by Zone-Melting Recrystallization," *Applied Physics Letters* 43, No. 5, September 1, 1983, pp. 505-507.
- F. T. Leighton and A. Rosenberg, "Automatic Generation of Three-Dimensional Circuit Layouts," *Proceedings, IEEE Conference on Computer Design*, November 1983, pp. 633-636; also MIT VLSI Memo No. 83-146, June 1983.
- R. M. Karp, F. T. Leighton, R. L. Rivest, C. D. Thompson, U. Vazirani, and V. Vazirani, "Global Wire Routing in Two-Dimensional Arrays," *Proceedings, 24th Conference on Foundations of Computer Science*, November 1983, pp. 453-459. Appeared in *Algorithmica*, Vol. 2, no. 2, 1987; pp. 113-129; also MIT VLSI Memo No. 83-153, October 1983.
- D. A. Antoniadis, "Three-Dimensional Integrated Circuit Technology," invited paper presented at MRS meeting, Boston, Massachusetts, November 1983; also MIT VLSI Memo No. 84-169, May 1984.
- A. Robinson, D. A. Antoniadis, and E. W. Maby, "A Fully-Self-Aligned Joint-Gate CMOS Technology," *Proceedings, International Electron Devices Meeting*, December 1983.
- S. N. Bhatt, *The Complexity of Graph Layout and Channel Routing for VLSI*, Ph.D. thesis, Department of Electrical Engineering and Computer Science, MIT, January 1984.
- W. Song and L. A. Glasser, "Power Distribution Techniques for VLSI Circuits," *Proceedings, 1984 Conference on Advanced Research in VLSI*, MIT, January 1984, pp. 45-52; also MIT VLSI Memo No. 83-156, November 1983.
- F. T. Leighton, "New Lower Bound Techniques for VLSI," *Math Systems Theory*, Vol. 17, No. 1, April 1984, pp. 47-70.

B. C. Williams, "Qualitative Analysis of MOS Circuits," to appear in *Artificial Intelligence*; also MIT VLSI Memo No. 84-165, April 1984.

E. W. Maby and D. A. Antoniadis, "Staggered CMOS: A Novel Three-Dimensional Technology," *Proceedings, Materials Research Society*, Albuquerque, New Mexico, February 27-29, 1984; also MIT VLSI Memo No. 84-170, May 1984.

C. G. Fonstad, "Consideration of the Relative Frequency Performance of Inverted Heterojunction npn Transistors," *IEEE Electron Device Letters*.

H. Kanbe, J. C. Vleck, and C. G. Fonstad, "(In,Ga)As/InP npn Heterojunction Bipolar Transistors Grown by Liquid Phase Epitaxy with High DC Current Gains," *IEEE Electron Device Letters*.

D. P. Christman, *Programming the Connection Machine*, M. S. and B. S. Thesis, Department of Electrical Engineering and Computer Science, MIT, January 1, 1984.

A. L. Ressler, *A Circuit Grammar for Operational Amplifier Design*, Ph.D. Thesis, Department of Electrical Engineering and Computer Science, MIT, January 7, 1984.

S. Bhatt and T. Leighton, "A Framework for Solving VLSI Graph Layout Problems," *Journal of Computer and System Sciences*, Vol. 28, No. 2, April 1984, pp. 300-343; also MIT VLSI Memo No. 84-167, April 1984.

T. Leighton, "Tight Bounds on the Complexity of Parallel Sorting," *Proceedings, 16th ACM Symposium of Theory of Computing*, April 1984, pp. 71-80; also MIT VLSI Memo No. 84-14, June 1984.

J. Bentley, D. Johnson, T. Leighton, C. McGeoch, and L. McGeoch, "Some Unexpected Expected Behavior Results for Bin Packing," *Proceedings, 16th ACM Symposium on Theory of Computing*, April 1984, pp. 279-288.

G. A. Kramer, *Brute Force and Complexity Management: Two Approaches to Digital Test Generation*, M. S. and B. S. Thesis, Department of Electrical Engineering and Computer Science, MIT, May 11, 1984.

A. S. Moulton, *Routing the Power and Ground Wires on a VLSI Chip*, M. S. Thesis, Department of Electrical Engineering and Computer Science, MIT, May 25, 1984; also MIT VLSI Memo No. 84-194, June 1984.

I. L. Bain, *Methodology Verification of Hierarchically Described VLSI Circuits*, M. S. Thesis, Department of Electrical Engineering and Computer Science, MIT, May 1984; also MIT VLSI Memo No. 84-195, July 1984.

H. Kanbe, J. C. Vleck, and C. G. Fonstad, "(In,Ga)As/InP n-p-n Heterojunction Bipolar Transistors Grown by Liquid Phase Epitaxy with High DC Current Gain," *IEEE Electron Device Letters*, Vol. EDL-5, No. 5, May 1984, pp. 172-175.

K. Tabatabaie-Alavi, *Ion Implanted (In,Ga)As/InP npn and (In,Ga)As/In,Al As Lateral pnp Heterojunction Transistors*, Ph.D. Thesis, Department of Electrical Engineering and Computer Science, MIT May 1984.

L. A. Glasser and L. P. J. Hoyte, "Delay and Power Optimization in VLSI Circuits," *Proceedings, ACM IEEE 21st Design Automation Conference*, Albuquerque, NM, June 25-27, 1984, pp. 529-535; also MIT VLSI Memo No. 84-171, May 1984.

T. Leighton, M. Lepley, and G. Miller, "Layouts for the Shuffle-Exchange Graph Based on the Complex Plane Diagram," *SIAM J. Algebraic and Discrete Methods*, Vol. 5, No. 2, June 1984, pp. 202-215; also MIT VLSI Memo No. 82-110, July 1982.

A. N. M. M. Choudhury, K. Tabatabaie-Alavi, and C. G. Fonstad, "Triple Implant (In,Ga)As/InP n-p-n Heterojunction Bipolar Transistors for Integrated Circuit Applications," *IEEE Electron Device Letters*, Vol. EDL-5, No. 7, July 1984, pp. 251-253.

Alan Bawden, "A Programming Language for Massively Parallel Computers," M. S. Thesis, Department of Electrical Engineering and Computer Science, MIT, August 31, 1984.

Anne H. Park, *CMOS LSI Design of a High-Throughput Digital Filter*, M. S. Thesis, Department of Electrical Engineering and Computer Science, MIT, August 31, 1984; also MIT VLSI Memo No. 84-204.

John T. Wroclawski, *DTOS - An Integrated VLSI System*, M. S. Thesis, Department of Electrical Engineering and Computer Science, MIT, September 1984.

C. E. Leiserson and J. B. Saxe, "A Mixed-Integer Linear Programming Problem Which is Efficiently Solvable," *21st Annual Allerton Conference on Communication, Control and Computing*, October, 1983; also MIT VLSI Memo No. 84-216, December, 1984.

T. Bui, S. Chaudhuri, F. T. Leighton and M. Sipser, "Graph Bisection Algorithms with Good Average Case Behavior," *Proceedings, 25th Conference on Foundations of Computer Science*, October, 1984, pp. 181-192; also MIT VLSI Memo No. 85-236, March 1985.

J. L. Wyatt, Jr., and Q. Yu, "Signal Delay in RC Meshes, Trees, and Lines," *Proceedings, 1984 IEEE International Conference on Computer-Aided Design*, Santa Clara, California, pp. 15-17, November, 1984; also MIT VLSI Memo No. 84-198, August 1984.

C. A. Zukowski and J. L. Wyatt, Jr., "Sensitivity of Nonlinear 1-port Resistor Networks," *IEEE Transactions on Circuits and Systems*, Vol. CAS-31, no. 12, pp. 1048-1051, December, 1984; also MIT VLSI Memo No. 83-155, October 1983.

J. Buss and P. Shor, "On the Pagenumber of Planar Graphs," *16th Annual Symposium on Theory of Computing*, pp. 98-100, 1984; also MIT VLSI Memo No. 84-173, May 1984.

P. Shor, "The Average-Case Analysis of some On-Line Algorithms for Bin Packing," *25th Symposium on Foundations of Computer Science*, pp. 193-200, 1984.

J. L. Wyatt, Jr., "Monotone Sensitivity of Nonlinear, Nonuniform RC Transmission Lines, with Application to Timing Analysis of Digital Integrated Circuits," *IEEE Transactions on Circuits and Systems*, Vol. CAS-32, no. 1, pp. 28-33, January, 1985; also MIT VLSI Memo No. 83-150, August 1983.

J. L. Wyatt, Jr., Q. Yu, C. Zukowski, H. N. Tan, and P. O'Brien, "Improved Bounds on Signal Delay in MOS Interconnect," *Proceedings, IEEE International Conference on Circuits and Systems*, Beijing, China, June, 1985, pp. 77-81 and *Proceedings, 1985 IEEE International Symposium on Circuits and Systems*, Kyoto, Japan, June 5-7, 1985, pp. 903-906; also MIT VLSI Memo No. 85-221, January 1985.

M. D. Matson, *Macromodeling and Optimization of Digital MOS VLSI Circuits*, Ph.D. thesis, Department of Electrical Engineering and Computer Science, MIT, January 24, 1985; also MIT VLSI Memo No. 85-231, February 1985.

F. T. Leighton, "Tight Bounds on the Complexity of Parallel Sorting," *IEEE Transactions on Computers*, Vol. C-34, no. 4, April 1985, pp. 71-80; also MIT VLSI Memo No. 84-172, May 1984.

L. A. Glasser, "A UV Write-Enabled PROM," *Proceedings of the 1985 Chapel Hill Conference on VLSI* (May 1985), Computer Science Press, pp. 61-65; also MIT VLSI Memo No. 85-239, March 1985.

F. M. Maley, "Compaction with Automatic Jog Introduction," *Proceedings of the 1985 Chapel Hill Conference on VLSI* (May 1985), Computer Science Press, pp. 261-283; also MIT VLSI Memo No. 85-267, October 1985.

L. A. Glasser, "Delay, Noise Margin, and Reliability in Digital Circuits," *Proceedings of the 1985 Chapel Hill Conference on VLSI* (May 1985), Computer Science Press, pp. 309-328; also MIT VLSI Memo No. 85-241, March 1985.

C. Zukowski, J. L. Wyatt, Jr., and L. A. Glasser, "Bounding Techniques and Applications for VLSI Circuit Simulation," *Proceedings, 1985 IEEE International Symposium on Circuits and Systems*, Kyoto, Japan, June 5-7, 1985, pp. 163-166; also MIT VLSI Memo No. 85-238, March 1985.

A. A. Berlin, *A Digital Gaussian Convolver for Visual Images*, B. S. Thesis, MIT, Department of Electrical Engineering and Computer Science; also MIT VLSI Memo No. 85-250, June 1985.

C. Phillips, "Space-Efficient Algorithms for Computational Geometry," M.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, August 1985; also MIT VLSI Memo No. 85-270, October 1985.

J. L. Wyatt, Jr., C. A. Zukowski, and P. Penfield, Jr., "Step Response Bounds for Systems Described by Matrices, with Application to Timing Analysis of Digital MOS Circuits," *Proceedings of the 24th IEEE Conference on Decision and Control*, Ft. Lauderdale, Florida, December 1985, pp. 1551-1557; also MIT VLSI Memo No. 85-257, September 1985.

P. D. Bassett, *A High-Speed Asynchronous Communication Technique for MOS Systems*, M.S. Thesis, Department of Electrical Engineering and Computer Science, May 1985; also MIT VLSI Memo No. 85-283, December 1985.

A. T. Ishii, *Interprocessor Communication Issues in Fat-Tree Architectures*, B.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, May 1985; also MIT VLSI Memo No. 85-268, October 1985.

B. M. Maggs, *Computing Minimum Spanning Trees on a Fat-Tree Architecture*, B.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, May 1985; also MIT VLSI Memo No. 85-269, October 1985.

B. Berger, *New Upper Bounds for Two-Layer Channel Routing*, M.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, January 1986; also MIT VLSI Memo No. 86-312, May 1986.

T. Bui, *Graph Bisection Algorithms*, Ph.D. Thesis, Department of Electrical Engineering and Computer Science, MIT, January 1986; also MIT VLSI Memo No. 86-310, April 1986.

R. I. Greenberg and C. E. Leiserson, "Randomized Routing on Fat-Trees," *Proceedings, Twenty-Sixth Annual Symposium on Foundations of Computer Science*, Portland, Oregon, October 21-23, 1985; pp. 241-249; also MIT VLSI Memo No. 85-260, September 1985.

C. E. Leiserson, "Fat-Trees: Universal Networks for Hardware-Efficient Super-Computing," *IEEE Transactions on Computers*, Vol. C-34, no. 10, pp. 892-901, October 1985. An early version appeared in the *1985 International Conference on Parallel Processing*.

G. C. Clark and R. E. Zippel, "Schema: An Architecture for Knowledge Based CAD," *Digest of Technical Papers, IEEE International Conference on Computer-Aided Design, ICCAD-85*, Santa Clara, California, pp. 50-52, November 18-21, 1985; also MIT VLSI Memo No. 85-271, October 1985.

B. Chor, C. E. Leiserson, R. L. Rivest, and J. Shearer, "An Application of Number Theory to the Organization of Raster-Graphics Memory," *JACM*, Vol. 33, no. 1, pp. 86-104, January 1986. An early version by the first three authors appeared in *Proceedings, Twenty-Third Annual Symposium on Foundations of Computer Science*, Chicago, Illinois, IEEE Computer Society, November 1982; pp. 92-99.

P. Bassett, L. A. Glasser, and R. Rettberg, "Dynamic Delay Adjustment: A Technique for High-Speed Asynchronous Communication," *Proceedings, Fourth MIT Conference on Advanced Research in VLSI*, Cambridge, Massachusetts, pp. 219-232, April 7-9, 1986.

P. R. O'Brien and J. L. Wyatt, Jr., "Signal Delay in ECL Interconnect," *Proceedings, 1986 International Symposium on Circuits and Systems*, Santa Clara, California, pp. 755-758, May 5-7, 1986; also MIT VLSI Memos No. 86-296, February 1986.

T. S. Hohol, *RELIC: A Reliability Simulator for Integrated Circuits*, M.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge, Massachusetts, May 1986; also MIT VLSI Memo No. 86-324, May 1986.

B. M. Maggs, *Communication-Efficient Parallel Graph Algorithms*, M.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge, Massachusetts, May 1986; also MIT VLSI Memo No. 86-349, December 1986.

F. M. Maley, *Compaction with Automatic Jog Introduction*, M.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge, Massachusetts, May 1986; also MIT VLSI Memo No. 86-316, May 1986.

T. Leighton and P. Shor, "Tight Bounds for Minimax Grid Matching, with Applications to the Average Case Analysis of Algorithms," *Proceedings, 18th ACM Symposium on Theory of Computing*, Berkeley, California, pp. 91-103, May 1986; also MIT VLSI Memo No. 86-320, June 1986.

A. V. Goldberg and R. E. Tarjan, "A New Approach to the Maximum Flow Problem," *Proceedings, 18th ACM Symposium on Theory of Computing*, Berkeley, California, pp. 136-146, May 1986; also MIT VLSI Memo No. 86-355, December 1986.

A. L. Robinson, L. A. Glasser, and D. A. Antoniadis, "A Simple Interconnect Delay Model for Multilayer Integrated Circuits," *VLSI Multilevel Interconnect Conference*, June 9-11, 1986; also MIT VLSI Memo No. 85-223, January 1985.

J. L. Wyatt, Jr., C. A. Zukowski, and Paul Penfield, Jr., "Step Response Bounds for Large-Scale Linear Systems Described by M-Matrices, with VLSI Application," *SIAM Conference on Linear Algebra in Signals, Systems and Control*, Boston, MA, August 12-14, 1986; abstract pp. A35-A36.

D. W. Weise, *Formal Hierarchical Multilevel Verification of Synchronous MOS VLSI Designs*, Ph.D. Thesis, MIT, Department of Electrical Engineering and Computer Science, August 1986; also MIT VLSI Memo No. 87-425, November 1987.

T. H. Cormen and C. E. Leiserson, "A Hyperconcentrator Switch for Routing Bit-Serial Messages," *Proceedings, 1986 IEEE International Conference on Parallel Processing*, St. Charles, Illinois, August 19-22, 1986; pp. 721-728; also MIT VLSI Memo No. 86-352, December 1986.

C. E. Leiserson and B. M. Maggs, "Communication-Efficient Parallel Graph Algorithms," *Proceedings, 1986 IEEE International Conference on Parallel Processing*, St. Charles, Illinois, August 19-22, 1986; pp. 861-868.

T. Leighton and A. Rosenberg, "Three-Dimensional Circuit Layouts," *SIAM Journal of Computing*, Vol. 15, no.3, August 1986; pp. 793-813; also MIT VLSI Memo No. 84-182, June 1984.

A. T. Sherman, *Cryptology and VLSI (a two-part dissertation): I. Detecting and Exploiting Algebraic Weaknesses in Cryptosystems; II. Algorithms for Placing Modules on a Custom VLSI Chip*, Ph.D. Thesis, Department of Electrical Engineering and Computer Science, MIT, October 1986; also MIT VLSI Memo No. 86-343, October 1986.

T. Leighton and C. E. Leiserson, "A Survey of Algorithms for Integrating Wafer-Scale Systolic Arrays," *Wafer Scale Integration*, G. Saucier and J. Trilhe, editors, Elsevier Science Publishers B. V., IFIP, 1986; pp. 177-195. Portions of this work are based on the paper "Wafer-Scale Integration of Systolic Arrays," *IEEE Transactions on Computers*, Vol. C-34, no. 5, May 1985; pp. 448-461. Portions appeared in *VLSI Systems Architecture*, E. Swartzlander, Jr., ed., Marcel-Dekker, Inc., 1987. An early version appeared as MIT VLSI Memo No. 82-101, April 1982 and a revised version appeared as MIT VLSI Memo No. 85-272, October 1985.

S. Bhatt, F. Chung, T. Leighton, and A. Rosenberg, "Optimal Simulations of Tree Machines," *Proceedings, 27th IEEE Conference on Foundations of Computer Science*, Portland, Oregon, October, 1986, pp. 274-282; also, MIT VLSI Memo No. 86-354, December 1986.

R. E. Zippel, P. Penfield, Jr., L. A. Glasser, C. E. Leiserson, J. L. Wyatt, Jr., F. T. Leighton, and J. Allen, "Recent Results in VLSI CAD at MIT," *Proceedings, 1986 Fall Joint Computer Conference*, Dallas, Texas, November 2-4, 1986, pp. 871-877; also, MIT VLSI Memo No. 86-341, October 1986.

T. S. Hohol and L. A. Glasser, "RELIC: A Reliability Simulator for Integrated Circuits," *Proceedings, International Conference on Computer-Aided Design*, Santa Clara, California, November 11-13, 1986. To appear (translated into Japanese) in *Nikkei Microdevices*; also, MIT VLSI Memo No. 87-360, January 1987.

F. Chung, T. Leighton, and A. Rosenberg, "Embedding Graphs in Books: A Layout Problem with Applications to VLSI Design," *SIAM Journal Algebraic and Discrete Methods*, Vol. 8, no. 1, Jan. 1987, pp. 33-58; also, MIT VLSI Memo No. 85-235, March 1985.

A. V. Goldberg, *Efficient Graph Algorithms for Sequential and Parallel Computers*, Ph.D Thesis, Department of Electrical Engineering and Computer Science, MIT, Cambridge, MA, February 1987; also MIT VLSI Memo No. 87-378, May 1987 and Laboratory for Computer Science Technical Memorandum MIT-LCS-TR-374, February 1987.

C. W. Selvidge, A. C. Malamy, and L. A. Glasser, "Power and Communication Techniques for Physically Isolated Integrated Circuits," *Proceedings, 1987 Conference on Advanced Research in VLSI*, Stanford, California, March 23-25, 1987, P. Losleben, ed., MIT Press, Cambridge, MA, 1987, pp. 231-247.

W. J. Dally, "Wire-Efficient VLSI Multiprocessor Communication Networks," *Proceedings, 1987 Conference on Advanced Research in VLSI*, Stanford, California, March 23-25, 1987, P. Losleben, ed., MIT Press, Cambridge, MA, 1987, pp. 391-415; also MIT VLSI Memo No. 86-345, October 1986.

C. W. Selvidge, *A Magnetic Communication Scheme for Integrated Circuits*, M. S. Thesis, MIT, Department of Electrical Engineering and Computer Science; also MIT VLSI Memo No. 87-379, May 1987.

L. A. Glasser, "Frequency Limitations in Circuits Composed of Linear Devices," to appear as "Frequency Limitations in Linear Circuits" in *Proceedings, 1987 IEEE International Symposium on Circuits and Systems*, Philadelphia, Pennsylvania, May 4-7, 1987; also, MIT VLSI Memo No. 86-348, November 1986.

A. V. Goldberg, S. Plotkin and G. Shannon, "Parallel Symmetry Breaking in Sparse Graphs," *Proceedings, 19th Annual ACM Symposium on the Theory of Computing*, New York, New York, May 1987, pp. 315-324.

A. V. Goldberg and R. E. Tarjan, "Solving Minimum Cost Flow Problems by Successive Approximation," *19th Annual ACM Symposium on the Theory of Computing*, New York, New York, May 1987, pp. 7-18.

J. Hastad, T. Leighton and M. Newman, "Reconfiguring a Hypercube in the Presence of Faults," *Proceedings, 19th Annual ACM Symposium on the Theory of Computing*, May 1987, pp. 274-284.

C. L. Kerstetter, *Supplying Constant Current to Drive the Two-Phase Clocking of a VLSI Circuit*, B.S. Thesis, Department of Electrical Engineering and Computer Science, May 1987.

J. Hastad, T. Leighton and B. Rogoff, "Analysis of Backoff Protocols for Multiple Access Channels," *Proceedings, 19th Annual ACM Symposium on the Theory of Computing*, May 1987, pp. 241-253.

J. Burroughs, *Reduction of Maximum Interconnect Length in Systolic Arrays*, B.S. Thesis, MIT, Department of Electrical Engineering and Computer Science, June 1987.

W. J. Dally, L. Chao, A. Chien, S. Hassoun, W. Horwat, J. Kaplan, P. Song, B. Totty, and S. Wills, "Architecture of a Message-Driven Processor," *Proceedings, 14th Annual Symposium on Computer Architecture*, Pittsburgh, Pennsylvania, June 2-5, 1987, pp. 189-196; also MIT VLSI Memo No. 87-420, November 1987.

T. M. King, *Automatic Generation of CMOS VLSI Clock Buffers*, M.S. Thesis, Department of Electrical Engineering and Computer Science, June 1987.

S. Rao, *Finding Small Edge Separators in Planar Graphs*, M.S. Thesis, Department of Electrical Engineering and Computer Science, June 1987.

F. Miller Maley, *Single-Layer Wire Routing*, Ph.D. Dissertation, MIT, Department of Electrical Engineering and Computer Science, August 1987; also Technical Report MIT/LCS, TR-403, Laboratory for Computer Science.

G. E. Blelloch, "Scans as Primitive Parallel Operations," *Proceedings, 1987 International Conference on Parallel Processing*, St. Charles, Illinois, August 1987; pp. 355-362.

T. H. Cormen, "Efficient Multichip Partial Concentrator Switches," *Proceedings, 1987 International Conference on Parallel Processing*, St. Charles, Illinois, August 1987; pp. 525-532.

A. C. Malamy, *A Magnetic Power and Communications Interface for Pinless Integrated Circuits*, B.S. Thesis, Department of Electrical Engineering and Computer Science, MIT, September, 1987; also MIT VLSI Memo No. 87-411, September 1987.

W. J. Dally, "A Fine-Grain, Message-Passing Processing Node," *Proceedings, 1987 Princeton Workshop on Algorithm, Architecture and Technology Issues for Models of Concurrent Computation*, Princeton, New Jersey, September 30 - October 1, 1987; also MIT VLSI Memo No. 87-421, November 1987.

W. J. Dally and P. Song, "Design of a Self-Timed VLSI Multicomputer Communication Controller," *Proceedings, IEEE International Conference on Computer Design 1987*, Rye Brook, New York, October 5-8, 1987; also MIT VLSI Memo No. 87-432, November 1987.

J. Kilian, S. Kipnis, and C. Leiserson, "The Organization of Permutation Architectures with Bussed Interconnections," *28th Annual Symposium on Foundations of Computer Science*, Marina Del Rey, California, October 12-14, 1987; pp. 305-315.

S. Rao, "Finding Near-Optimal Separators in Planar Graphs," *Proceedings, 1987 IEEE Symposium on Foundations of Computer Science*, October 1987; pp. 225-237.

T. N. Bui, S. Chaudhuri, F. T. Leighton and M. Sipser, "Graph Bisection Algorithms With Good Average Case Behavior," *Combinatorica*, Vol. 7, no. 2, 1987; pp. 171-191.

A. Goldberg and S. Plotkin, "Parallel $\Delta + 1$ Coloring of Constant-degree Graphs," *Information Processing Letters*, Vol. 15, no. 4, 1987; also MIT VLSI Memo No. 86-355, December 1986.

B. M. Maggs and S. A. Plotkin, "Minimum-cost Spanning Tree as a Path-finding Problem," *Information Processing Letters*, Vol. 26, no. 6, 25 January 1988, pp. 291-293.

W. J. Dally, "Performance Analysis of k -ary n -cube Interconnection Networks," to appear in *IEEE Transactions on Computers*; also MIT VLSI Memo No. 87-424, November 1987.

INTERNAL MEMORANDA

J. Batali and A. Harthstein, "The Design Procedure Manual," MIT VLSI Memo No. 80-31, September 1980; and MIT A.I. Memo No. 598, September 1980.

D. Kleitman, F. T. Leighton, M. Lepley, and G. L. Miller, "New Layouts for the Shuffle-Exchange Graph," MIT VLSI Memo No. 81-46, March 1981.

P. Penfield, Jr., and J. Rubinstein, "Signal Delay in MOS Interconnections," MIT VLSI Memo No. 81-48, April 1981.

G. T. Goeloe, E. W. Maby, D. J. Silversmith, R. W. Mountain, and D. A. Antoniadis, "Vertical Single-Gate CMOS Inverters on Laser-Processed Multilayer Substrates," MIT VLSI Memo No. 81-64, September 1981.

J. Batali, "An Introduction to DPL," MIT VLSI Memo No. 81-65, October 1981.

C. E. Leiserson and R. Y. Pinter, "Optimal Placement for River Routing," MIT VLSI Memo No. 81-66, October 1981.

P. Antognetti, C. Lombardi, and D. A. Antoniadis, "Use of Process and 2-D MOS Simulation in the study of Doping Profile Influence on S/D Resistance in Short Channel MOSFETs," MIT VLSI Memo No. 81-68, October 1981.

R. L. Rivest, "The PI (Placement and Interconnect) System," MIT VLSI Memo No. 82-74, February 1981.

S. N. Bhatt and C. E. Leiserson, "Minimizing the Longest Edge in a VLSI Layout," MIT VLSI Memo No. 82-86, March 1982.

S. N. Bhatt and C. E. Leiserson, "How to Assemble Tree Machines," MIT VLSI Memo No. 82-87, March 1982.

- F. T. Leighton, "A Layout Strategy for VLSI Which is Provably Good," MIT VLSI Memo No. 82-88, March 1982.
- R. Y. Pinter, "Optimal Layer Assignment for Interconnect," MIT VLSI Memo No. 82-98, April 1982.
- F. T. Leighton and A. L. Rosenberg, "Three-Dimensional Circuit Layouts," MIT VLSI Memo No. 82-102, April 1982.
- B. Chor, C. E. Leiserson, R. L. Rivest, "An Application of Number Theory to the Organization of Raster-Graphics Memory," MIT VLSI Memo No. 82-106, June 1982.
- L. A. Glasser, and W. S. Song, "Introductory CMOS Techniques," MIT VLSI Memo No. 82-117, September 1982.
- F. Berman, F. T. Leighton, and L. Snyder, "Optimal Tile Salvage," MIT VLSI Memo No. 82-119, September 1982.
- P. S. Whitney and C. G. Fonstad, "Manganese as a p-type Dopant for Liquid Phase Epitaxial $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$," MIT VLSI Memo No. 84-206, October 1984.
- F. Berman, T. Leighton, P. W. Shor, L. Snyder, "Generalized Planar Matching," MIT VLSI Memo No. 85-234, March 1985.
- T.-A. Chu and L. A. Glasser, "Synthesis of a Self-timed Controller for a Successive-approximation A/D Converter," MIT VLSI Memo No. 85-274, November 1985.
- L. A. Glasser, "Synchronizer Failure in A/D Converters," MIT VLSI Memo No. 85-276, November 1985.
- P. O'Brien and J. L. Wyatt, Jr., "Signal Delay in Leaky RC Mesh Models for Bipolar Interconnect," MIT VLSI Memo No. 85-278, November 1985.
- M. D. Matson and L. A. Glasser, "Macromodeling and Optimization of Digital MOS VLSI Circuits," MIT VLSI Memo No. 86-303, March 1986.
- D. Standley and J. L. Wyatt, Jr., "Improved Signal Delay Bounds for RC Tree Networks," MIT VLSI Memo No. 86-317, May 1986.
- I. L. Bain and L. A. Glasser, "Methodology Verification of Hierarchically Described VLSI Circuits," MIT VLSI Memo No. 86-327, June 1986.
- W. J. Dally, "A High-Performance VLSI Quaternary Serial Multiplier," MIT VLSI Memo No. 86-344, October 1986.
- W. J. Dally, "Lazy Event-Driven Simulation," MIT VLSI Memo No. 86-346, October 1986.
- T. Leighton, "A Survey of Problems and Results for Channel Routing," MIT VLSI Memo No. 86-350, December 1986.
- B. Berger, M. Brady, D. Brown, and T. Leighton, "Nearly Optimal Algorithms and Bounds for Multilayer Channel Routing," MIT VLSI Memo No. 86-351, December 1986.

J. L. Wyatt, Jr., "Nonlinear Dynamic Maximum Power Theorem," MIT VLSI Memo No. 87-371, March 1987.

A. V. Goldberg and S. A. Plotkin, "Efficient Parallel Algorithms for $(\Delta + 1)$ -Coloring and Maximal Independent Set Problems," MIT VLSI Memo No. 87-373, May 1987.

J. L. Wyatt, Jr., "The Practical Engineer's No-Nonsense Guide to On-Chip Signal Delay Calculations," MIT VLSI Memo No. 87-381, May 1987.

L. A. Glasser, "Frequency Limitations in Circuits Composed of Linear Devices," MIT VLSI Memo No. 87-415, October 1987.

S. N. Bhatt, F. R. K. Chung, J.-W. Hong, F. T. Leighton and A. Rosenberg, "Optimal Simulations by Butterfly Networks: Extended Abstract," MIT VLSI Memo No. 87-427, November 1987.

APPENDIX A. VLSI SEMINARS (through December 1987)

September 18, 1979

The MIT HI Lab/Xerox PARC SCHEME Chip or What I Did This Summer, Gerald J. Sussman, MIT.

September 25, 1979

Restructurable Logic Implementations, Jack I. Rafael, MIT, Lincoln Laboratory

October 2, 1979

Submicron DOS Technology, Dennis D. Buss, Texas Instruments

October 16, 1979

Theoretical Aspects of a VLSI Design, Ronald L. Rivest, Harold Abelson, and Andrea Laugh, MIT

October 23, 1979

Towards Structured Chip Design, J. Craig Mudge, DEC

November 6, 1979

The MU Design Automation System - Preliminary Results of Logic Synthesis from Behavioral Descriptions, Gary Live, Carnegie-Mellon University

November 13, 1979

The Design of the 8086, Peter Toll, Intel Corporation

November 20, 1979

The Impact of Integrated Circuits, Jack S. Kirby, Texas Instruments

November 27, 1979

Monolithic Power-Spectrum Centroid Detector: An Example for a Vertical Integration Approach, Levy Gerzberg, Stanford University

December 11, 1979

Introduction to the DAEDALUS Graphics Layout Editor, Howard E. Shrobe, MIT

February 12, 1980

VLSI: Models, Circuits, and Performance Limits, Clark Thompson, University of California, Berkeley

February 26, 1980

Current VLSI Designs for Real-Time Systems, David C. Barr, Simon Ullman, and John Batali, MIT

March 4, 1980

The SCHEME Chip Design Experience and Associated Design Tools, Jack Holloway, MIT

March 11, 1980

Integrated Sensing Devices using the Charge-Flow Transistor, Stephen D. Senturia, MIT

March 18, 1980

Cost-Effective Tradeoffs in Pipelined Function Units, Edward S. Davidson, University of Illinois

April 1, 1980

A Multiplexed Switched-Capacitor Filter Bank, Patrick Bosshart, MIT

April 8, 1980

Analog Circuits in DOS PSI, Yannis Tsividis, Columbia University

April 15, 1980

Computer Aids for the Logic Design of Microprocessors, Harold Shichman, Bell Laboratories

April 22, 1980

Unrestricted Clocks Considered Harmful..., Charles L. Spitz, California Institute of Technology

April 29, 1980

Scaling Limits of NMOS VLSI Circuits, K. Nirmal Ratnakumar, Stanford University

VLSI SEMINARS (continued)

May 6, 1980

***A Single Supply DAC and Future Linear Design Constraints*, Peter R. Holloway, Analog Devices**

May 13, 1980

***Symbolic Layout of MOS LSI Building-Blocks*, Min-Yu Hsueh, IBM**

September 16, 1980

***The Apiary Network for Knowledgeable Systems*, Carl E. Hewitt, MIT**

September 23, 1980

***Tessellation Architectures for VLSI*, Charles L. Seitz, California Institute of Technology**

September 30, 1980

***GaAs Integrated Circuits for Ultra High Speed LSI/VLSI*, Richard C. Eden, Rockwell International**

October 7, 1980

***Direct-Write Laser Processing for Microelectronics*, R. Osgood, D. Ehrlich, and T. Deutsch, MIT Lincoln Laboratory**

October 21, 1980

***The Role of Device Physics in MOS IC Development*, Laurence G. Walker, Hewlett-Packard Laboratories**

October 28, 1980

***Fast Algorithms for Design Checking (Based on Statistics on VLSI Design)*, Jon L. Bentley, Carnegie-Mellon University**

November 4, 1980

***Limits of Improvement of Silicon Integrated Circuits*, V. Leo Rideout, IBM**

November 18, 1980

***VLSI Device Phenomena in Dynamic Memory Devices*, Ronald R. Troutman, IBM**

November 25, 1980

***The Solution of a Restricted Routing Problem and Its Applications*, Andrea LaPaugh, Brown University**

December 2, 1980

***Signal Processing with VLSI*, Richard F. Lyon, Xerox PARC**

February 10, 1981

***Bubbles and VLSI*, Hsu Chang, IBM**

February 24, 1981

***1 Micron nMOS Technology for VLSI Circuit Design*, Dana Seccombe, Hewlett-Packard**

March 3, 1981

***VLSI-Fundamental Factors*, James M. Early, Fairchild**

March 10, 1981

***The Layout and Wiring of a VLSI Microprocessor*, M. Feuer, K. H. Khokhani, and D. A. Mekta, IBM**

March 17, 1981

***Design Automation at RCA: The Present and the Future*, Lawrence M. Rosenberg, RCA**

March 31, 1981

***An Algorithm for Optimal PLA Folding*, Gary D. Hatchel, IBM**

April 7, 1981

***High Performance Graphics for Personal Computers*, James Clark and Marc Hannah, Stanford University**

April 14, 1981

***Custom CMOS LSI Circuit Design Using Computer Aids*, Charles W. Gwyn, Sandia Laboratories**

April 28, 1981

***Techniques for Improving Engineering Productivity of VLSI Designs*, Joseph C. Logue, IBM**

VLSI SEMINARS (continued)

May 5, 1981

Systolic Systems, Charles E. Leiserson, MIT

May 12, 1981

SLIM: A Language for Microcode Specification and Simulation in VLSI, John Hennessy, Stanford University

September 15, 1981

Virtual Grid Symbolic Layout, Neil Weste, Bell Laboratories

September 22, 1981

Randomness and Complexity, Charles Bennett, IBM

September 29, 1981

New Concepts for Processing Ceramic Chip Carriers, H. Kent Bowen, MIT

October 6, 1981

Scalability Issues for Submicron MOS Integrated Circuits, Pallab Chatterjee, Texas Instruments

October 20, 1981

The BELLMAC-32: A Single-Chip, 32 Bit, CMOS Microprocessor; Part I: Architecture and Logic Design, J. A. Fields, T. D. Lovett, J. J. Molinelli, Bell Laboratories Methodology

October 27, 1981

BELLMAC-32: A Single-Chip, 32 Bit, CMOS Processor; Part II: Technology, Circuit & Chip-Design Methods, B. T. Murphy and L. C. Parrillo, Bell Laboratories

November 3, 1981

Direct Computer Modelling, Donald Greenspan, University of Texas

November 10, 1981

Research at the National Submicron Facility, Edward D. Wolf, Cornell University

November 17, 1981

Hierarchical Logic Simulation - or - Simulating Simulating, W. H. Sherwood, DEC

November 24, 1981

IDL (Interactive Design Language), H. Fleisher, L. Maissel, and R. Phoenix, IBM

December 1, 1981

A Businessman's Look at VLSI, James F. Riley, Dataquest

December 8, 1981

Routing for VLSI Layout Design, Ernest S. Kuh, University of California, Berkeley

February 9, 1982

Computer Aided Design: Its Role in the British SERC Microelectronics Initiative, M. J. Newman, Rutherford Laboratory

February 23, 1982

CMOS Technology for VLSI Design, K. Kokkonen, Intel Corporation

March 2, 1982

Topics in VLSI Testing, Sheldon Akers, General Electric

March 9, 1982

288K Bit Dynamic RAM, E. Thoma and B. Fitzgerald, IBM

March 16, 1982

The Role of Semiconductor Device Modeling in VLSI Design, L. W. Nagel, Bell Laboratories

March 30, 1982

Electronic Properties and Device Applications of Beam Crystallized Silicon-On-Insulators, J. F. Gibbons, Stanford University

VLSI SEMINARS (continued)

April 13, 1982

Computer-Aided Design with a View: VISTA, P. B. Weil, Hughes Aircraft Co.

April 27, 1982

Nial - Its Role as a Design Aid and as a Target in VLSI Design, M. A. Jenkins, Queen's University

May 4, 1982

The IBM Micro/370 Design, N. Tredennick, IBM

May 11, 1982

VLSI Tester and CAT Architecture, R. C. Albrow, GenRad Semiconductor Test Inc.

September 14, 1982

Design of High Voltage (Over 500V) Integrated Circuits, Peter W. Shackle, Harris Semiconductor

September 21, 1982

Switch-Level Simulation and the Verification of MOS Digital Systems, Randal E. Bryant, Caltech

September 28, 1982

Relaxation-Based Simulation of VLSI Circuits, Alberto Sangiovanni-Vincentelli, University of California, Berkeley, Joint with LIDS

October 5, 1982

SLA - A Structures Method for Digital IC Design, Suhas Patil, Patil Systems, Inc.

October 19, 1982

Modeling in Latchup Triggering in CMOS Circuits, Donald Nelsen, Digital Equipment Corporation

October 26, 1982

Automatic Logic Implementation Based on Fast Boolean Function Manipulation, Robert Brayton, IBM T. J. Watson Research Center, and Curt McMullen, Harvard University, Joint with LIDS

November 2, 1982

High Performance Heat Sinking for VLSI, Fabian Pease, Stanford University

November 9, 1982

Designing Efficient Parallel Algorithms, S. Rao Kosaraju, John Hopkins University

November 16, 1982

Statistical Mechanics for Optimal Design, Scott K Kirkpatrick and Dan Gelatt, IBM T. J. Watson Research Center

November 23, 1982

The LTC Integrated Circuit Facility - Its Design and Capabilities, Stuart M. Spitzer, ITT Advanced Technology Center

November 30, 1982

River Routing: Methodology and Analysis, Ron Pinter, Bell Laboratories, Murray Hill, NJ

December 7, 1982

Crystal: A Timing Analyzer for nMOS VLSI Circuits, John Ousterhout, University of California, Berkeley

February 8, 1983

A 32-Bit VLSI System, John Spencer and Mark Forsythe, Hewlett-Packard, Fort Collins, CO

February 15, 1983

RSIM: A Logic-Level Timing Simulator, Christopher J. Terman, MIT

March 1, 1983

Technology Issues in VLSI, Arnold Reisman, Microelectronics Center of North Carolina and North Carolina State University

VLSI SEMINARS (continued)

March 8, 1983

Multilevel MOSFET Circuit and Logic Analysis/Simulation, Albert E. Reuhli, IBM T. J. Watson Research Center, Yorktown Heights, NY

March 15, 1983

The CHIP Computer, Lawrence Snyder, Purdue University, W. Lafayette, IN

March 29, 1983

Size, Power, and Speed, Maurice V. Wilkes, Digital Equipment Corp. and MIT

April 5, 1983

Device Technology Comparison in the Context of Large Scale Digital Applications, Paul Solomon, IBM T. J. Watson Research Center, Yorktown Heights, NY

April 12, 1983

Total Fault Coverage by Digital Circuit Transformation, Richard J. Lipton, Princeton University

April 26, 1983

The Yorktown Simulation Engine: A Supercomputer for Logic Simulation, Greg Pfister, IBM T. J. Watson Research Center

May 3, 1983

Survey of Design for Testability, Thomas W. Williams, IBM, Boulder, CO

May 10, 1983

A CAD Design Framework and Interated Timing Analysis, A. Richard Newton, University of California, Berkeley

September 20, 1983

A High Performance Microprocessor Chip to be Used in Groups of Hundreds of More, H. T. Kung, Carnegie-Mellon University, Pittsburgh, PA

September 27, 1983

Managing the Chip Design Database, Randy Katz, University of California, Berkeley

October 4, 1983

Focused Ion Beam Technology and Applications, Robert L. Seliger, Hughes Research Laboratory, Malibu, CA

October 18, 1983

Strategic Computing and Survivability, Robert Kahn, Defense Advanced Research Projects Agency

October 25, 1983

Considerations in VLSI Graphics and Display Processor Design, Stephen L. Domenik, Intel Corporation, Santa Cruz, CA

November 1, 1983

A Methodology for the Design of Testable VLSI Circuits, Melvin A. Breuer, University of Southern California, Los Angeles, CA

November 8, 1983

CAPRI, Silicon Compiling for VLSI Circuits Specified by Algorithm, Francois Anceau and J. P. Schoellkopf, IMAG Computer Architecture Group, Grenoble, France

November 15, 1983

An Ada Program Talks to an Ada Chip, Elliott I. Organick, University of Utah, Salt Lake City, UT

November 22, 1983

Integrated Power Devices, M. S. Adler, General Electric Co., Corporate Research and Development, Schenectady, NY

November 29, 1983

A Monolithic Tactile Sensor Array, Bruce E. Wooley, Bell Laboratories, Holmdel, NJ

VLSI SEMINARS (continued)

December 6, 1983

Single Layer Routing Representations and Searches in TWIGY, a Production Router, Michel Foreau, Digital Equipment Corp., Andover, MA

December 13, 1983

Interconnections for CMOS Technology: Design and Process Considerations, Rick Davies, Texas Instruments, Dallas, TX

February 14, 1984

CMOS VLSI Two-Dimensional Array Processors, Dr. Paul Sullivan, NCR Corporation

February 28, 1984

A 32b Microprocessor with On-Chip Virtual Memory Management, Daniel Dobberpuhl, Digital Equipment Corporation, Hudson, MA

March 6, 1984

Wafer-Scale Design Using Restructurable VLSI, Jack I. Raffel, MIT, Lincoln Laboratory

March 13, 1984

An Overview of the PI System for Placement and Interconnect of Custom VLSI Design, Ronald L. Rivest, MIT

March 20, 1984

CAM for VLSI: An Industrial Perspective, Nicholas E. English, Jr., Harris Semiconductor, Melbourne, FL

April 2, 1984

Testability in VLSI, Constantin C. Timoc, Jet Propulsion Laboratory, Pasadena, CA

April 10, 1984

Physical Technology for Future VLSI Systems, Dr. Robert Hannemann, Digital Equipment Corp., Andover, MA

April 24, 1984

Compound Semiconductors, Sorab K. Ghandi, Rensselaer Polytechnic Institute, Troy, NY

May 1, 1984

Knowledge-Based Aids for VLSI Design, Tom Mitchell, Rutgers University, New Brunswick, NJ

May 8, 1984

Mosaic's WHIP Wafer-Scale Packaging Technology, R. R. Johnson, Mosaic Systems Inc., Troy, MI

May 15, 1984

The HITEST Generation System, Gordon D. Robinson, Cirrus Computers Ltd., Visiting MIT

September 18, 1984

Numerical Simulation of Complex VLSI Device Structures, Wolfgang Fichtner, AT&T Bell Laboratories, Murray Hill, NJ

September 25, 1984

An Electronic Design Interchange Format, A. Richard Newton, University of California, Berkeley

October 2, 1984

The State-of-the-Art and Near-Future in Bipolar Circuit Design, Barrie Gilbert, Analog Devices, Inc., Forest Grove, OR

October 16, 1984

Trends in VLSI Testing, J. Lawrence Carter, IBM T. J. Watson Research Center, Yorktown Heights, NY

October 23, 1984

Technologies for High-Performance Computing, Neil Lincoln, ETA Systems, St. Paul, MN

October 30, 1984

Applications of Statistical Process/Device Simulation for CAD/CAM of VLSI, Andrzej J. Strojwas, Carnegie-Mellon University, Pittsburgh, PA

VLSI SEMINARS (continued)

November 6, 1984

The Interaction of Physics and CAD in VLSI CMOS Design, Kim Kokkonen, Intel Corporation, Santa Clara, CA

November 13, 1984

The Magic IC Layout System, John K. Ousterhout, University of California, Berkeley, CA

November 20, 1984

Health and Safety in Microelectronics, Joseph LaDou, University of California, San Francisco, CA

November 27, 1984

A Systolic VLSI Engine for Real-Time Raster Graphics, Christopher Pottle, Cornell University, Ithaca, NY

December 4, 1984

MOSFET Miniaturization - From One Micron to the Limits, R. H. Dennard, IBM T. J. Watson Research Center, Yorktown Heights, NY

December 11, 1984

STAFAN: An Alternative to Fault Simulation, Sunil K. Jain, AT&T Bell Laboratories, Murray Hill, NJ

February 12, 1985

Design Aspects of Monolithic A/D and D/A Converters, Rudy van de Plassche, Phillips Research Laboratories Sunnyvale, Signetics Corporation, Sunnyvale, CA

February 26, 1985

The Implications of Scaling on VLSI Reliability, Murray H. Woods, Intel Corporation, Santa Clara, CA

March 5, 1985

How the New Mask Protection Law Fits Within the Legal Protection Methods for VLSI, Roger S. Borovoy, Sevin Rosen Management Co., Sunnyvale, CA

March 12, 1985

Submicron and Quantum Transport in Extremely Small MOSFETs, William J. Skocpol, AT&T Bell Laboratories, Holmdel NJ

March 19, 1985

Circuitry Used in the Design of a Fast NMOS Dynamic RAM, Robert Proebsting, United Technologies, Mostek Corp., Carrollton, TX

April 2, 1985

The Impact of VLSI on Telecommunication Architectures, Jeff Fried, GTE Laboratories, Waltham MA

April 9, 1985

Three Dimensional Integrated Circuits, Hon Wai Lam, Texas Instruments, Dallas, TX

April 23, 1985

MIPS-X: A New High Performance Microprocessor, Mark Horowitz, Stanford University, Stanford, CA

April 30, 1985

Metal-Silicon Reaction, King-Ning Tu, IBM T. J. Watson Research Center, Yorktown Heights, NY

May 7, 1985

The YORKTOWN Silicon Compiler, Robert K. Brayton, IBM T. J. Watson Research Center, Yorktown Heights, NY

May 14, 1985

Poly-crystalline Silicon Micromachining: A New Technology for Integrated Sensors, Roger T. Howe, Carnegie-Mellon University, Pittsburgh, PA

September 17, 1985

Design of a LISP Processor Chip, Patrick Bosshart, Texas Instruments, Dallas, TX

September 24, 1985

Plowing and Circuit Extraction in Magic, Walter S. Scott, University of California, Berkeley, CA

VLSI SEMINARS (continued)

October 1, 1985

Physics and Technology of Solid-State Image Sensors, Timothy J. Tredwell, Research Laboratories, Eastman Kodak Company, Rochester, NY

October 8, 1985

Rapid Thermal Processing—Where is it Going?, Carl Russo, Varian Associates, Extrion Division, Gloucester, MA

October 22, 1985

Symbolic Verification of MOS Circuits, Randy Bryant, Carnegie-Mellon University, Pittsburgh, PA

October 29, 1985

Trends in Commercial VLSI Microprocessor Design, Nick Tredennick, IBM T.J. Watson Research Center, Yorktown Heights, NY

November 5, 1985

An Integrated Approach to Modeling, E. J. Prendergast, AT&T Bell Laboratories, Allentown, PA

November 12, 1985

Symbolic Verification of Hardware Design, Harry G. Barrow, Schlumberger Palo Alto Research, CAS, Palo Alto, CA

November 1985

JAPAN: A Culture Optimized for VLSI Engineering, Jeffrey Frey, National Science Foundation and Cornell University

November 26, 1985

R & D Project of 3-D Integrated Circuits in Japan, Shoei Kataoka, Sharp Corporation, Tenri, Japan

December 3, 1985

VLSI Layout Programming, Ed Lien, Microelectronics and Computer Technology Corporation (MCC), Austin, TX

December 10, 1985

An Application of Knowledge-Based Expert Systems to Detailed Routing of VLSI Chips, Rostam Joobbani, Carnegie-Mellon University, Pittsburgh, PA February 11, 1986

A Short Guide to High-Speed IC Technology Comparisons, Stuart H. Wemple, AT&T Bell Laboratories, Murray Hill, NJ

February 25, 1986

A 4Mbit Dram with Cross-Point Trench-Transistor Cell, Ashwin Shah, Texas Instruments, Dallas, TX

March 4, 1986

The Rise and Fall of American Microelectronics, Charles H. Ferguson, MIT

March 11, 1986

Integrated Solid-State Sensors: Interfacing Electronics to a Non-Electronic World, Ken Wise, University of Michigan, Ann Arbor, MI

March 18, 1986

New Material Technologies for Integrated Circuits: Silicon on Insulator and Monolithic GaAs/Si, B. Y. Tsaur, Lincoln Laboratory, MIT

April 1, 1986

Nanostructures: A New Dimension in Electronic Research, Richard Howard, AT&T Bell Laboratories, Holmdel, NJ

April 15, 1986

Instruction Sets and Beyond: Computers, Complexity, and Controversy, E. Douglas Jensen, Carnegie-Mellon University, Pittsburgh, PA

VLSI SEMINARS (continued)

April 29, 1986

Simulated Annealing: Theory and Application to the Placement of Integrated Circuits, Alberto L. Sangiovanni-Vincentelli, University of California, Berkeley, CA

May 6, 1986

High Reliability CMOS Gate Array Design and Production, Charles W. Gwyn, United Technologies Corp., Colorado Springs, CO

May 13, 1986

Custom Wafer-Scale Interconnect and Packaging Technologies Being Developed at Lawrence Livermore National Laboratory, David E. Tuckerman, Lawrence Livermore National Laboratories, Livermore, CA

September 16, 1986

The VHSIC Hardware Description Language, Hal Carter, Air Force Institute of Technology, Wright-Patterson Air Force Base, OH

September 23, 1986

Scan Line Access Memories for High Speed Image Rasterization, Stefan Demetrescu, Stanford University, Stanford, CA

September 30, 1986

Structured Process Flow for Integrated Design, Manufacturing, and Test, Paul Losleben, Stanford University, Stanford, CA

October 7, 1986

Ballistic Transport and Electron Spectroscopy in Tunnelling Hot Electron Transfer Amplifiers (THETA), Marty Heiblum, IBM T.J. Watson Research Center, Yorktown Heights, NY

October 21, 1986

Graph Embeddings, Hypercubes, and Linear Algebra, Lennart Johnsson, Yale University

November 4, 1986

CEMU-MOS Timing Simulation on a Message Based Multiprocessor, Bryan Ackland, AT&T Bell Laboratories, Holmdel, NJ

November 18, 1986

NS: An Integrated Symbolic Design System, Jim Cherry, Symbolics, Cambridge, Mass.

November 25, 1986

A.I. (Analog Intelligence), Yanni Tsividis, Columbia University, New York, NY

December 2, 1986

The Semiconductor Industry (Losing Sight of Your Added Value), Jeff Kalb, Digital Equipment Corporation, Hudson, Mass.

December 9, 1986

Address Tracing Using Microcode, Richard Sites, Digital Equipment Corporation, Hudson, Mass.

February 10, 1987

Scanning Tunneling Microscopy -- The Ultimate VLSI Tool?, Joseph E. Demuth, IBM Thomas J. Watson Research Center

February 24, 1987

Circuit Design Tools, Simulation and Verification, Shawn Hailey, Meta-Software, Inc.

March 3, 1987

Automatic Transistor Sizing and Layout for High Performance Chips, Alfred Dunlop, AT&T Murray Hill, NJ.

March 10, 1987

Yield Planning for VLSI Chip Manufacturing, Charles Stapper, IBM, Essex Junction, VT.

VLSI SEMINARS (continued)

March 17, 1987

Algorithm-Based Fault Tolerance, Jacob Abraham, University of Illinois.

April 7, 1987

Integrated Microsensors: Critical Issues in Design and Fabrication, Rosemary Smith, MIT

April 14, 1987

ADAM Advanced Design AutoMation System, Alice Parker, University of Southern California

April 28, 1987

The U. S. Semiconductor Industry: A Formula for Success, Sandy Kane, IBM, White Plains, NY

May 5, 1987

World Class Technologies Mean World Class Manufacturing Challenges, Billy Crowder, IBM, T.J. Watson, Yorktown Heights, NY

September 15, 1987

So Who Needs Lattice-Matched Heterojunctions Anyway?, Jerry Woodall, IBM, T.J. Watson Research Center

September 22, 1987

Preliminary Design and Development of a Corporate-Level Production Planning System for the Semiconductor Industry, Robert Leachman, University of California, Berkeley

September 29, 1987

A 40-bit Tagged Architecture Lisp Microprocessor, Greg Efland and Bruce Edwards, Symbolics, Inc., Cambridge, MA

October 6, 1987

Chemical Beam Epitaxy, Won Tien Tsang, AT&T Bell Laboratories, Murray Hill, NJ

October 20, 1987

Performance-Directed Synthesis of Digital VLSI Circuits, Jonathan Allen, MIT

October 27, 1987

Pixel - Planes: An Example of VLSI Technology for Raster Graphics, Henry Fuchs, University of North Carolina

November 3, 1987

The Berkeley Synthesis System, Alberto Sangiovanni-Vincentelli, University of California, Berkeley, Visiting MIT Fall, 1987

November 10, 1987

The Aquarius Project, Al Despain, University of California, Berkeley

November 17, 1987

Inductive Fault Analysis of VLSI Circuits, John Shen, Carnegie-Mellon University

November 24, 1987

System Level Limits on VLSI: Interconnections and Packaging, Brian Bakoglu, IBM, Austin, TX

December 1, 1987

X-Ray v. Optical and E-Beam Lithography: A Comparative Study, Alan Wilson, IBM, T.J. Watson Research Center



Massachusetts Institute of Technology

VLSI SEMINAR

Information for VLSI Seminar Speakers

Since 1979 the MIT VLSI Seminar Series has formed an important part of the MIT microsystems program. We have been fortunate in attracting first-rate speakers, and as a result we have a loyal and enthusiastic audience. We are looking forward to your talk, which will continue this tradition, and trust that your visit to MIT will be beneficial both to us and to you. This letter provides general information about the series and specific instructions for you as a speaker.

The seminars are held Tuesday afternoons at 4:00 during the MIT academic year, normally in the Edgerton Lecture Hall, Room 34-101, at 50 Vassar Street, on the MIT campus. Simple refreshments are served at 3:30. The seminars are free and open to the public. Single-page notices on colorful paper, with an abstract of the announced talk, are sent to our mailing list one or two weeks before each seminar.

You should plan to speak for approximately 50 to 60 minutes, and then to answer questions for the next 10 to 20 minutes. The setting is informal, and you may entertain questions during your talk if you wish.

Typical attendance, between 30 and 70, includes MIT faculty, staff, and students, and people from other universities and local companies. Sometimes people in the audience travel hundreds of miles just to attend, or arrange a trip to the Boston area to coincide with a particular seminar.

Our audience normally includes people from many technical areas, such as electronic materials, devices, processing, submicron structures, CAD, parallel architecture, and VLSI theory. We realize you will not be able to address all these topics in depth. The bulk of your talk may be directed toward one group of specialists. However, we hope you can explain the context of your work and its importance, so that listeners in other areas can appreciate the significance of your work, even if not the details.

Your seminar will be videotaped and also transmitted live to MIT Lincoln Laboratory. The tapes are distributed to a group of companies that support our VLSI program, and we will make an extra tape for your personal use, as an expression of our appreciation. Experience shows that the cameras are not intrusive and the TV pickup does not alter the informal nature of the seminars. Aside from wearing a wireless mike, you will not have to do anything special; no extra effort is necessary in preparing slides, overhead foils, lecture demonstrations, etc. We will ask for a paper copy of your visuals to distribute with the tapes (if you use overhead foils, we can make the copies ourselves on the day of your talk).

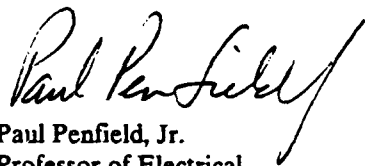
Arrangements for the seminar series are handled by Ms. Susan Peterson, Room 39-321, MIT. She will call you or you may call her at (617) 253-7308 regarding the following:

- We will need an exact title and your name and affiliation as you wish them to appear, approximately eight weeks before your talk. This much time is necessary because each talk is mentioned in the previous three notices.
- We will need your abstract, between 80 and 120 words, no later than four weeks before your talk, either in a letter, by electronic mail (to penfield@caf.mit.edu), or by facsimile, (617) 253-9622.

- As soon as convenient, please sign and return one copy of the attached VLSI Seminar Speaker Release Form (the other copy is for your records).
- We hope you can spend the entire day of your talk on campus, meeting faculty and students with related interests. If there are particular people you would like to see, please let Ms. Peterson know. As soon as we know your travel plans, we will arrange your appointments. On the day of your visit, come first to Room 39-321 to pick up your schedule. The street address is 60 Vassar Street.
- For audio-visual equipment, we routinely provide an overhead projector and a 35-mm slide projector. Also, with advance notice, we will do our best to accommodate any other needs, e.g., multiple screens, motion picture projector, TV monitors, or demonstration apparatus. When you send your abstract, please tell us your AV needs.
- Our budget permits us to reimburse travel costs of speakers from universities (but not companies). If you are from a university, please keep track of your expenses and send receipts to my office.

Some local companies like to invite speakers who come from a distance to visit the day before or the day after the MIT talk. Unless you advise us to the contrary, we will share information about future speakers with these companies, and you may hear directly from them.

If you have any questions about the series or about arrangements for your talk, please contact either me or Ms. Peterson.



Paul Penfield, Jr.
Professor of Electrical
Engineering and Director,
Microsystems Research Center

PP/srp

1/23/89

APPENDIX C.

SPRING 1980 M.I.T. VLSI RESEARCH REVIEW

Monday, May 19, 1980

9:00 a.m. to 5:30 p.m.

Room 10-250

AGENDA

Session I. Chairman: Gary L. Miller, Dept. of Mathematics

- 9:00 Welcome and Introduction. Paul Penfield, Jr.
- 9:20 Harold Abelson, "Communication Constraints in Parallel Computation".
- 9:40 Andrea LaPaugh, "Routing Algorithms for Integrated Circuits--An Analytic Approach".
- 10:00 Edward Fredkin, A. Ressler, T. Toffoli, and N. Margolus, "Interaction Logic".
- 10:20 Coffee Break

Session II. Chairman: Rafael Reif, Dept. of Elec. Eng. & Comp. Sci.

- 11:00 Ronald L. Rivest, "The RSA Encryption Chip".
- 11:45 Steven L. Garverick, "MOS Integrated Sensors".
- 12:05 David C. Shaver, "Novel Applications of Submicrometer Lithography".
- 12:30 Buffet Lunch in the Sala de Puerto Rico, second floor of the Stratton Student Center

Session III. Chairman: Clifton G. Fonstad, Dept. of Elec. Eng. & Comp. Sci.

- 2:00 Jonathan Allen, "Introduction and Overview of Modern Digital IC Design".
- 2:30 Howard Shrobe, "Constraint Propagation in VLSI Design: DAEDALUS and Beyond".
- 2:50 Lance A. Glasser and P. Penfield, Jr., "PLA Generation as a Case Study in Structured VLSI Design".
- 3:10 Randal Bryant, "Logic Simulation of MOS LSI".
- 3:30 Snack Break

Session IV. Chairman: Richard B. Adler, Dept. of Elec. Eng. & Comp. Sci.

- 4:00 Clark Baker, "Network Topology Via Node Extraction".
- 4:20 Arvind, V. Kathail, and K. Pingali, "A Multiple Processor Dataflow Architecture".
- 4:40 Clement Leung, "An Architecture Description Language".
- 5:00 Patrick Bosshart, "Computer Aided Design of NMOS Opamps".

12/9/80



DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE MASSACHUSETTS 02139

FALL 1980 M.I.T. VLSI RESEARCH REVIEW

Monday, December 15, 1980

9:00 a.m. to 5:00 p.m.

Room 10-250

AGENDA

9:00 Welcome and Introduction. Paul Penfield, Jr.

SESSION I. Chairman: Henry I. Smith, Dept. of Elec. Eng. & Comp. Sci.

9:20 Gary E. Kopec, "LSIAA: LSI Artwork Analysis Program"

9:40 Thomas Knight, "A VLSI Approach to Image Sensing and Processing"

10:00 Randal E. Bryant, "Theoretical Basis of Switch-Level Simulation"

10:20 Coffee Break

SESSION II. Chairman: Jonathan Allen, Dept. of Elec. Eng. & Comp. Sci.

11:05 August F. Witt, "Electronic Materials Processing in the Context of
Solid-State Device Research"

11:30 John Melngailis, "Submicron Structures Research at M.I.T."

11:55 Dimitri A. Antoniadis, "Status of the M.I.T. LSI Fabrication Facility"

12:20 Buffet Lunch in the Sala de Puerto Rico, second floor of the Stratton
Student Center

SESSION III. Chairman: Herbert H. Sawin, Dept. of Chemical Engineering

2:00 John Batali, "The Design Procedure Language"

2:30 Lance A. Glasser, "The Analog Behavior of Digital Integrated Circuits"

2:50 Thomas Leighton, Margaret Lepley, and Gary Miller, "Laying Out the
Shuffle-Exchange Graph"

3:10 Snack Break

SESSION IV. Chairman: Ronald L. Rivest, Dept. of Elec. Eng. & Comp. Sci.

3:50 Yannis Tsiividis and Dimitri A. Antoniadis, "A Multiproject Chip
Approach to the Teaching of Analog MOS LSI and VLSI"

4:20 Douglas D. Williams, "Compilation and Optimization of VLSI Finite-State
Machines"

4:40 Danny Hillis, "An Application of VLSI to Artificial Intelligence
(Computer Architecture for the New Wave)"

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, Massachusetts 02139

SPRING 1981 M.I.T. VLSI RESEARCH REVIEW
Monday, May 18, 1981
9:00 a.m. to 5:00 p.m.
Kresge Auditorium

AGENDA

9:00 Welcome and Introduction. Paul Penfield, Jr.

SESSION I. Chairman: Richard Zippel, Dept. of Elec. Eng. & Comp. Sci.

9:15 "SPECIAL PURPOSE HARDWARE FOR DESIGN RULE CHECKING," Larry Seiler.

9:35 "A CHOPPER-STABILIZED FEED-FORWARD NMOS OPERATIONAL AMPLIFIER," Michael C. Coln.

9:55 "THE PI SYSTEM FOR VLSI PLACEMENT AND INTERCONNECT," Alan E. Baratz.

10:15 "MOSFETS ON SILICON PREPARED BY MOVING MELT ZONE RECRYSTALLIZATION OF ENCAPSULATED POLY-CRYSTALLINE SILICON ON AN INSULATING SUBSTRATE," E. W. Maby, M. W. Geis, Y. L. LeCoz, D. J. Silversmith, R. W. Mountain, and D. A. Antoniadis.

10:35 COFFEE BREAK

SESSION II. THE DESIGNER'S ASSISTANT SYSTEM

Chairman: Stephen D. Senturia, Dept. of Elec. Eng. & Comp. Sci.

11:20 "PROCESSOR DESIGN IS A SOFTWARE ENGINEERING PROBLEM," Gerald Jay Sussman.

11:35 "A STATE MACHINE GENERATOR--THE CONTROL UNIT OF THE DESIGNER'S ASSISTANT SYSTEM," Edmund N. Goodhue.

12:00 "THE DATA PATH GENERATOR," Howard E. Shrobe.

12:25 Lunch in the Sala de Puerto Rico, Stratton Student Center

Agenda
Page two

SESSION III. Chairman: Peter Elias, Dept. of Elec. Eng. & Comp. Sci.

- 2:00 "TECHNIQUES FOR ELECTRON BEAM TESTING AND RESTRUCTURING OF INTEGRATED CIRCUITS," David C. Shaver.
- 2:20 "MINIMIZING THE LONGEST WIRE IN A VLSI LAYOUT," Sandeep N. Bhatt and Charles E. Leiserson**
- 2:40 "THE DYNAMICS OF OXYGEN INCORPORATING DURING CZOCHRALSKI SILICON GROWTH," D. F. Bliss.
- 3:00 "SIMULATION TOOLS FOR LSI DESIGN," Christopher J. Terman.

3:25

Snack Break

SESSION IV. Chairman: Arvind, Dept. of Elec. Eng. & Comp. Sci.

- 4:00 "USE OF TWO-DIMENSIONAL DEVICE MODELING IN THE SIMULATION OF SHORT-CHANNEL EFFECTS IN MOSFETS," C. Lombardi, V. Kwong, P. Antognetti, and D. Antoniadis.
- 4:20 "A STATIC ANALYZER FOR nMOS CIRCUITS," Clark M. Baker.
- 4:40 "AN INTEGRATED-CIRCUIT APPROACH TO THE MEASUREMENT OF THE INTRINSIC CAPACITANCES IN MOS TRANSISTORS," John Paulos, Dimitri Antoniadis, and Yannis Tsividis.

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, Massachusetts 02139

Fall 1981 M.I.T. VLSI RESEARCH REVIEW
Monday, December 14, 1981
9:00 a.m. to 5:30 p.m.
Room 10-250

AGENDA

SESSION I. Chairman: Gary Miller, Department of Mathematics

- 9:00 Welcome and Introduction. Paul Penfield, Jr.
- 9:20 Andrew Michael Hawryluk, "Transmission Diffraction Gratings for Soft X-Ray Spectroscopy and Spatial Period Division."
- 9:40 Lance A. Glasser and L. P. John Hoyte, "Automated Device Sizing for Integrated Circuit Designs."
- 10:00 David F. Day and Stephen D. Senturia, "High Contact Resistance in Polyimide Vias--An Auger Analysis."
- 10:20 COFFEE BREAK

SESSION II Chairman: Ronald Rivest, Dept. of Elec. Eng. and Comp. Sci.

- 10:55 Chairman's Introduction. Ronald L. Rivest
- 11:10 John E. Batali, "A Biologist's Approach to Routing."
- 11:30 Charles E. Leiserson and Ron Y. Pinter, "Optimal Placement for River Routing."
- 11:50 Ron Y. Pinter, "Routing Two-Point Nets Across a Channel."
- 12:10 Tom Leighton, "New Bounds for Channel Routing."
- 12:30 Buffet Lunch in the Sala de Puerto Rico, second floor of the Stratton Student Center

SESSION III Chairman: Arvind, Dept. Elec. Eng. and Comp. Sci.

- 2:15 R. Reif and J. E. Knott, "A Low-Temperature Process to Increase the Grain Size of Thin Polysilicon Films
- 2:35 C. H. Ferguson and D. M. Raff, "Technology, Strategic Choice, and the Future Structure of Semiconductor Production"
- 2:55 Chris M. Horwitz, "Reactive Sputter-Etch Process Control and the Fabrication of Fine Structures."
- 3:15 SNACK BREAK

SESSION IV Chairman: Richard Zippel, Dept. Elec. Eng. and Comp. Sci.

- 4:00 K. Tabatabaie-Alavi, N. Slater, A. N. M. M. Choudhury, and C. G. Fonstad, "InGaAs/InP Heterojunction Bipolar Logic Technology."
- 4:20 Steven McCormick, "Automated Circuit Extraction from Mask Descriptions."
- 4:40 E. W. Maby and D. A. Antoniadis, "Device Structures for Three Dimensional Integration."

Department of Electrical Engineering and Computer Science
Massachusetts Institute of Technology
Cambridge, MA 02139

Spring 1982 M.I.T. VLSI Research Review
Monday, May 17, 1982
9:00 a.m. to 5:00 p.m.
Kresge Auditorium

AGENDA

SESSION I. Chairman: Professor Clifton G. Fonstad, Department of Electrical Engineering and Computer Science

- 9:00 Welcome and Introduction. Paul Penfield, Jr.
- 9:15 Daniel Weise, "Interactive Analysis Tools"
- 9:35 R. F. Kwasnick, M. A. Kastner, J. Melngailis, and H. I. Smith,
"Quantum Size Effect in the Conductance of Sub-100nm
Wide FETs"
- 9:55 Arvind, "A Dataflow Architecture with Tagged Tokens"
- 10:25 COFFEE BREAK

SESSION II Chairman: Professor Jonathan Allen, Department of Electrical Engineering and Computer Science

- 11:10 Henry I. Smith, "Education in Submicrometer Structures"
- 11:30 Richard E. Zippel, "An Undergraduate Subject in MOS Digital
Circuits"
- 11:50 Herbert H. Sawin, "10.615 - An IC Processing Subject for
Chemical Engineers"
- 12:10 Lance A. Glasser, "A New Graduate Subject on the Design
and Analysis of VLSI Circuits"

12:30 LUNCH - Sala de Puerto Rico

SESSION III Chairman: Professor Gerald J. Sussman, Department of Electrical Engineering and Computer Science

2:00 Danny Hillis, "The Connection Machine Message Routing Chip,
Or How to Connect a Million Things"

2:20 Y. L. Le Coz, E. W. Maby, D. A. Antoniadis,
R. Roussos and B. Mikic, "Silicon-On-Insulator
Recrystallization Processes by a Moving Heat
Source: A Thermal Analysis"

2:40 Mark Sherred, "A Multi-Project Chip Tester"

3:00 Mark Johnson, "An NMOS Content-Addressable Memory
Chip for Virtual Address Translation"

3:20 SNACK BREAK

SESSION IV Chairman: Professor Gary Miller, Department of Mathematics

4:00 Charles E. Leiserson, "Digital Circuit Optimization"

4:20 Edward W. Maby and Dimitri A. Antoniadis, "Thin Zone-
Recrystallized Silicon Films on Silicon Dioxide"

4:40 William H. Evans, "A Digital Signal Processor for Speech
Synthesis Applications"

5:00 ADJOURN



DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASSACHUSETTS 02139

Fall 1982 VLSI Research Review
Friday, December 10, 1982
9:00 a.m. to 5:00 p.m.
Kresge Auditorium

AGENDA

9:00 Welcome and Introduction, Paul Penfield, Jr., Department
of Electrical Engineering and Computer Science

SESSION I. Chairman: Henry I Smith, Department of Electrical Engineering
and Computer Science

9:20 "The Advantages and Limits of 3-Dimensional VLSI," Thomson Leighton and
Arnold L. Rosenberg

9:40 "Silicon-on-Insulator Orientation Selection by Zone Melting Through
Constrictions," Harry Atwater.

10:00 "A Board Level Interface for the Scheme-81 Chip," Jonathan D. Taft.

10:20 COFFEE BREAK

SESSION II. Chairman: Lance A. Glasser, Department of Electrical Engineering
and Computer Science

11:10 "A Test Strategy for Packet Switching Networks," Willie Y.-P. Lim.

11:30 "Planar Ion-Implanted Heterojunction Bipolar Transistors for High Speed
IIL: The Lateral PNP's," K. Tabatabaie-Alavi, A.M.N.N. Choudhury, and
C. G. Fonstad.

11:50 "Designing a High-Level Silicon Compiler," Philip E. Agre.

12:10 BUFFET LUNCH, Sala de Puerto Rico, Stratton Student Center

SESSION III. Chairman: Marc Kastner, Physics Department

2:00 "Power Distribution Techniques for VLSI Circuits," William Song.

2:20 "Wafer-Scale Integration of Systolic Arrays," F. Thomson Leighton and
Charles E. Leiserson.

2:40 "Polyimide in VLSI - The Role of Mobile Ions," D. R. Day, H. Neunhaus, and
S. D. Senturia.

3:00 "Wave from Bounding for Fast Timing Analysis of Digital Integrated
Circuits," John L. Wyatt, Jr.

3:20 SNACK BREAK

SESSION IV. Chairman: Michael F. Sipser, Department of Mathematics.

4:00 "New Data-Path and Control Structures for the MacPitts Silicon Compiler,"
Jeffrey K. Fox.

4:20 "Plasma-Assisted CVD of Thin Polysilicon Films," Wayne R. Burger, Thomas
J. Donahue, and Rafael Reif.

4:40 "An Application of Number Theory to the Organization of Raster-Graphics
Memory," Benny Chor, Charles E. Leiserson, and Ronald L. Rivest.

Spring 1983 VLSI Research Review
Monday, May 16, 1983
9:00 a.m. to 5:00 p.m.
Kresge Auditorium

AGENDA

9:00 Welcome and Introduction, Paul Penfield, Jr., Department of
Electrical Engineering and Computer Science

SESSION I. Chairman: Lance A. Glasser, Department of Electrical Engineering
and Computer Science

9:20 "An Approximation Algorithm for Manhattan Routing" Brenda S. Baker,
Sandeep N. Bhatt, and F. Thomson Leighton

9:40 "A Process Design Language with Optimization," Nick English,
Dimitri A. Antoniadis, and Paul J. Tsang

10:00 "Computer-Aided Process Design (CAPD) - Methodology and Logics,"
Paul J. Tsang, Dimitri A. Antoniadis, and Nick English

10:20 COFFEE BREAK

SESSION II. Chairman: Charles Leiserson, Department of Electrical
Engineering and Computer Science

11:10 "Post Implant Annealing of GaAs and InP Using an Ultrahigh Intensity
Arc Lamp," K. Tabatabaie-Alavi, A.N.M.M. Choudhury, H. Kanbe,
and C. G. Fonstad

11:30 "A Digital Delay Line Implemented in VLSI," Jonathan Taft

11:50 "Silicon-on-Insulator Bipolar Transistors," Mark Rodder and
Dimitri A. Antoniadis

12:10 BUFFET LUNCH, Sala de Puerto Rico, Stratton Student Center

SESSION III. Chairman: Richard E. Zippel, Department of Electrical
Engineering and Computer Science

2:00 "Linear Approximations of MOS Transistor Networks,"
Christopher J. Terman

2:20 "The Effect of High Fields on MOS Device Performance,"
Charles G. Sodini

2:40 "Routing Power and Ground Wires," Andrew S. Moulton

3:00 SNACK BREAK

SESSION IV. Chairman: John L. Wyatt, Jr., Department of Electrical
Engineering and Computer Science

3:40 "Progress Toward the Development of a Novel Three-dimensional CMOS
Technology," Edward W. Maby and Dimitri Antoniadis

4:00 "Silicon-on-Insulator by Low Temperature Solid-State
Recrystallization," Carl Thompson and Eric Anderson

4:20 "The Connection Machine RAM Chip," Brewster Kahle



DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

C A M B R I D G E , M A S S A C H U S E T T S 0 2 1 3 9

Fall 1983 VLSI Research Review

AGENDA

9:00 Welcome and Introduction, Paul Penfield, Jr., Department of Electrical Engineering and Computer Science

SESSION I. Chairman: James K. Roberge, Department of Electrical Engineering and Computer Science

9:10 "Qualitative Analysis of MOS Circuits," Brian C. Williams

9:30 "A Circuit Grammar for Operational Amplifier Design," Andrew Ressler

9:50 "Methodology Verification of Hierarchically Described VLSI Circuits," Isaac Bain

10:10 "HPLA: A Design-by-Example PLA Generator," Cyrus Bamji

10:30 COFFEE BREAK

SESSION II. Chairman: Charles G. Sodini, Department of Electrical Engineering and Computer Science

11:00 "A Fully Self-Aligned Joint-Gate CMOS Technology," A. L. Robinson, D. A. Antoniadis, and E. W. Maby

11:20 "Fabrication of Periodic Submicron Structures," Erik H. Anderson

11:40 "Low-Temperature Silicon Epitaxy Using Low-Pressure Chemical Vapor Deposition with and without Plasma Enhancement," Thomas J. Donahue, W. R. Burger, and R. Reif

12:00 "Heterojunction Bipolar Transistors," James Vlcek, Hiroshi Kanbe, A. N. M. Masum Choudhury, Kamal Tabatabaie-Alavi, and Clifton G. Fonstad

12:20 BUFFET LUNCH, Sala de Puerto Rico, Stratton Student Center

SESSION III. Chairman: Jonathan Allen, Department of Electrical Engineering and Computer Science

1:45 "A Hardware-Assisted Methodology for VLSI Design Rule Checking," Larry D. Seiler

2:05 "Using Parallelism and Hierarchy in Automatic Test Pattern Generation," Glenn A. Kramer

2:25 "Phaselocking for Fun and Profit," Robert A. Iannucci

2:45 "The PI System's Algorithms for Placing Modules on Custom VLSI Chips," Alan T. Sherman

3:05 SNACK BREAK

SESSION IV. Chairman: Carl V. Thompson, II, Department of Materials Science and Engineering

3:30 "The Waveform-Bounding Approach to Digital MOS Circuit Simulation: The One-Way Gate Model," Charles A. Zukowski, Lance A. Glasser, and John L. Wyatt, Jr.

3:50 "Zone-Melting Recrystallization of InSb on Oxidized Silicon Wafers," C. C. Wong, C. J. Keavney, H. A. Atwater, C. V. Thompson, and H. I. Smith

4:10 "Modifying Polycrystalline Films through Ion Channeling," Ralph Iverson and Rafael Reif



DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASSACHUSETTS 02139

Spring 1984 VLSI Research Review

Agenda

9:00 Welcome and Introduction, Paul Penfield, Jr.

SESSION I. Chairman: Thomas F. Knight, Jr.

9:10 N. T. Quach, R. Reif and B-Y. Tsaur, "Solid-Phase Epitaxial Growth of Amorphized Low-Pressure Chemically Vapor-Deposited Polycrystalline Silicon Films."

9:30 Herbert H. Sawin, Albert D. Richards, and Brian E. Thompson, "Kinetics of the Plasma Etching of Polysilicon in Cl_2 Discharges."

9:50 Steven P. McCormick, "EXCL: A Circuit Extractor for IC Designs."

10:10 Jeff Arnold, "Parallel Simulation of Digital LSI Circuits."

10:30 COFFEE BREAK

SESSION II. Chairman: John L. Wyatt

11:00 George C. Clark, Jeff Eisen, and Richard E. Zippel, "Circuit Analysis in Schema."

11:20 M. Rodder, S. Madan, D. Antoniadis and T. Kikkawa, "Effects of Si_3N_4 and Al Films on the Passivation of Polysilicon Films."

11:40 I. H. Leventhal, R. R. Troutman and C. G. Sodini, "Comparison of DC Latchup Characterization Techniques for CMOS Technology."

12:00 John J. Paulos and Dimitri Antoniadis, "Measurement of Minimum-Geometry MOS Transistor Capacitances."

12:20 BAG LUNCH, Lobby 34-101. Seating and tables for lunch are available on the fourth floor of this building, Room 34-101.

SESSION III. Chairman: Ramesh S. Patil

1:45 Charles E. Leiserson and F. Miller Maley, "VLSI Routing of Planar Interconnections."

2:05 Herbert J. Neuhaus, David R. Day and Stephen D. Senturia, "Sodium Transport in Polyimide- SiO_2 Systems."

2:25 Denise D. Denton, David R. Day, Donald F. Priore, Stephen D. Senturia, Eugene S. Anolick and Donald Scheider, "Moisture Diffusion in Polyimide Film in Integrated Circuits."

2:45 Mark Shirley and Randall Davis, "Generating Distinguishing Tests Based on Hierarchical Models and Symptom Information."

3:05 SNACK BREAK

SESSION IV. Chairman: Lance A. Glasser

3:30 Ramin Khorram, "Functional Test-Pattern Generation for Integrated Circuits."

3:50 T. Yonehara, J. E. Palmer, Henry I. Smith and C. V. Thompson, "Grapho-epitaxy of Ge by Solid-State Surface-Energy-Driven Secondary Grain Growth."

4:10 M. Wong, R. Reif, and G. R. Srinivasan, "A Trapping Mechanism for Autodoping in Silicon Epitaxy."



DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASSACHUSETTS 02139

Fall 1984 VLSI Research Review

Agenda

9:00 Welcome and Introduction, Paul Penfield, Jr.

SESSION I. Chairman: Carl V. Thompson

9:10 A. C. Warren, D. A. Antoniadis, H. I. Smith, and J. Melngailis, "Superlattices and One-Dimensional Physics in Inversion Layers Using Submicron Period Gate Electrodes."

9:30 Tam-Anh Chu, "Design of a CMOS Self-Timed Two-by-Two Packet Router."

9:50 Thye-Lai Tung and D. A. Antoniadis, "Modeling Nonuniform Oxidation of Silicon."

10:10 Charles E. Leiserson, "FAT TREES: Universal Networks for Hardware-Efficient Supercomputing."

10:40 COFFEE BREAK

SESSION II: Chairman: Christopher J. Terman

11:10 Mark Matson and Lance A. Glasser, "Macromodeling and Optimization of Digital MOS VLSI Circuits."

11:30 Frank W. Smith III, Zeev Feit, David R. Day, T. J. Lewis and Stephen D. Senturia, "Conduction in Polyimide at Ordinary Device Temperatures."

11:50 Thang Bui, Soma Chaudhuri, Tom Leighton, and Mike Sipser, "Graph Bisection Algorithms with Good Average Case Behavior."

12:10 Mark S. Wrighton, "Electrochemical Microelectronic Devices: 'Transistors' Based on Redox Active Polymers."

12:30 BAG LUNCH

SESSION III. Chairman: Hae-Seung Lee

1:45 Prabha K. Tedrow, Vida Ilderem, and R. Reif, "Low Pressure Chemical Vapor Deposition of Titanium Silicide."

2:05 Cyrus S. Bamji, Charles E. Hauck, and Jonathan Allen, "Design-by-Example Regular Structure Generator."

2:25 Steven L. Garverick and Charles G. Sodini, "Large Signal Linearity of Scaled MOS Transistors."

2:45 John L. Wyatt, Jr., "Improved Bounds on Signal Delay in MOS Interconnect."

3:05 SNACK BREAK

SESSION IV. Chairman: Thomas F. Knight, Jr.

3:30 Charles E. Leiserson and Cynthia A. Phillips, "A Space-Efficient Algorithm for Finding the Connected Components of Rectangles in the Plane."

3:50 John S. Haggerty, John Flint and David Adler, "Laser Induced Chemical Vapor Deposition."

4:10 Daniel Weise, "Automatic Formal Verification of Synchronous MOS Designs."

4:30 Adjourn
MICROSYSTEMS PROGRAM OFFICE, Room 36-575 Telephone (617) 253-8138



DEPARTMENT OF ELECTRICAL ENGINEERING AND COMPUTER SCIENCE

MASSACHUSETTS INSTITUTE OF TECHNOLOGY

CAMBRIDGE, MASSACHUSETTS 02139

Spring 1985 VLSI Research Review

May 20, 1985

AGENDA

9:00 Welcome and Introduction, Paul Penfield, Jr.

SESSION I. Chairman: Charles G. Sodini

- 9:10 W. R. Burger, T. J. Donahue, and R. Reif, "Electrical Characterization of Epitaxial Silicon Films Deposited at Low Temperatures by the Plasma-Enhanced Chemical Vapor Deposition (PECVD) Technique."
- 9:30 Robert C. Armstrong, "Procedural Design of a Floating-Point Arithmetic Unit."
- 9:50 M. Rodder, D. A. Antoniadis, and S. Madan, "Comparison of Different Techniques for Passivation of Small-Grain Poly-Si MOSFETs."
- 10:10 Andrew A. Berlin, "A Digital Convolver for Visual Images."
- 10:30 COFFEE BREAK

SESSION II. Chairman: Christopher J. Terman

- 11:00 Rosemary Cartwright, Nagy El-Kaddah, and Julian Szekely, "The Effect of an Axial Magnetic Field on Fluid Flow and on Heat and Mass Transfer Close to the Interface of a Rotating Crystal During Czochralski Growth."
- 11:20 Ronald I. Greenberg and Charles E. Leiserson, "A Randomized Algorithm for Routing Bit-Serial Messages on Fat-Trees."
- 11:40 Andrew Tangborn and Anthony T. Patera, "Numerical Simulation of Czochralski System Bulk Flows."
- 12:00 Greg Waters, "A High-Performance Crossbar Switch for Multicomputers."
- 12:20 BAG LUNCH

SESSION III. Chairman: Donald E. Troxel

- 1:30 Paul D. Bassett and Lance A. Glasser, "A High-Speed Asynchronous Communication Technique for MOS VLSI Systems."
- 1:50 S. Y. Chou, D. A. Antoniadis, H. I. Smith, and J. Melngailis, "Sub-100 nm MOSFETs Fabricated Using X-Ray Lithography."
- 2:10 Charles A. Zukowski, Lance A. Glasser and John L. Wyatt, Jr., "Bounding Enhancements for VLSI Circuit Simulation."
- 2:30 H. M. Branz, B. T. Fiske, J. R. Flint, J. S. Haggerty, and D. Adler, "Doping of Hydrogenated Amorphous Silicon Films Prepared by Laser-Induced Chemical Vapor Deposition."
- 2:50 SNACK BREAK

SESSION IV. Chairman: Carl V. Thompson

- 3:20 M. A. Schmidt, F. L. Terry, B. P. Mathur, and S. D. Senturia, "Inversion-Layer Mobility of MOSFETs with Nitrided Oxide Gate Dielectrics."
- 3:40 Thomas H. Corman, and Charles E. Leiserson, "A Hyperconcentrator Switch for Routing Bit-Serial Messages."
- 4:00 Shahryar Motakef, "Factors Controlling the Generation of Thermally Induced Dislocations During Growth of III-V Compounds from Melt."



Massachusetts
Institute
of Technology

Microsystems
Research
Center

Room 39-321
Cambridge
Massachusetts
02139

Telephone
(617) 253-8128

Agenda
Fall 1985 VLSI Research Review
December 16, 1985

9:00 Welcome and Introduction, Paul Penfield, Jr.

SESSION I. Chairman: Professor Roger T. Howe

- 9:10 J. P. Wade and C. G. Sodini, "Dynamic Cross-Coupled Bitline Content Addressable Memory Cell for High Density Arrays"
- 9:30 H. A. Atwater, Henry I. Smith, and C. V. Thompson, "Enhancement of Grain Growth in Ultra-Thin Germanium Films by Ion Bombardment"
- 9:50 Margaret St. Pierre, "A Simulation Environment for Schema"
- 10:10 T. J. Garino, R. W. Adams, and H. K. Bowen, "New Ceramic Processes for Microelectronic Packaging"
- 10:30 COFFEE BREAK

SESSION II. Chairman: Professor Martin Schlecht

- 11:00 Jeffrey W. Scott, Wai Lee, Charles Giancarlo, and Charles G. Sodini, "A CMOS Slope Adaptive Delta Modulator"
- 11:20 Stephen Y. Chou, D. A. Antoniadis, and Henry I. Smith, "Application of the Shubnikov-de Haas Effect in Characterization of Sub-100-nm Channel Si MOSFETs"
- 11:40 Kenneth T-Y. Kung and Rafael Reif, "Implant-Dose Dependence of Seed Selection Through Ion Channeling to Enhance the {110} Texture of Low-Pressure Chemical-Vapor Deposited Polycrystalline Si Films on SiO₂"
- 12:00 Christian R. Musil, John Melngailis, and John L. Bartelt, "Focused Ion Beam Microsurgery for Electronics"
- 12:20 BAG LUNCH. Tables are set up in Room 34-401.

SESSION III. Chairman: Dr. John Melngailis

- 1:30 Duane Boning and Dimitri A. Antoniadis, "MASTIF—A Workstation Approach to Fabrication Process Design"
- 1:50 Denise D. Denton, Donald F. Priore, Herbert J. Neuhaus, Stephen D. Senturia, Eugene S. Anolick, and Donald Scheider, "An Integrated MOS Test Chip for Study of the Electrical Properties of Polyimide Films"
- 2:10 Bonnie A. Berger and Tom Leighton, "New Bounds and Algorithms for Channel Routing"
- 2:30 S. Motakef, A. Patera, J. Szekely, G. Stephanopoulos, and A. Witt, "Growth and Characterization of Large-Diameter Semiconductor Single Crystals"

SESSION IV. Chairman: Professor David J. Edell

- 3:20 Sching L. Lin, and Jonathan Allen, "MINPLEX—A Compactor that Minimizes the Bounding Rectangle and Individual Rectangles in a Layout"
- 3:40 Kenneth D. Allen and Herbert H. Sawin, "Polysilicon Plasma Etching in a Freon^(R)-13 Discharge: Modeling of Etching Rate and Directionality"
- 4:00 Joshua D. Marantz, "Exploiting Parallelism in VLSI CAD"
- 4:20 Wai Lee, Christine Lam, Tow Chong, and Clifton Fonstad, "Molecular-Beam Epitaxy of III-V Heterostructure Electronic Devices"
- 4:40 ADJOURN



Massachusetts
Institute
of Technology

Microsystems
Research
Center

Cambridge
Massachusetts
02139

Room 39-321
Telephone
(617) 253-8138

Agenda
Spring 1986 VLSI Research Review
May 19, 1986

9:00 Welcome and Introduction, Paul Penfield, Jr.

SESSION I. Chairman: Professor Charles G. Sodini

- 9:10 Darius Crenshaw and Rafael Reif, "Modeling and Simulation of Autodoping in CVD Silicon Epitaxy"
- 9:30 M. Rodder and D. A. Antoniadis, "Characteristics of Thin Film Poly-Si MOSFETs as a Function of Process Conditions and High Field Stress"
- 9:50 David J. Edell, "Biomedical Applications of Microfabrication Technology"
- 10:10 Jerome C. Licini, Marc A. Kastner, John Melngailis, and David J. Bishop, "Conductance Fluctuations in Narrow MOSFETs"
- 10:30 COFFEE BREAK

SESSION II. Chairman: Professor H. Kent Bowen

- 11:00 T. S. Hohol and L. A. Glasser, "RELIC: A Reliability Simulator for Integrated Circuits"
- 11:20 Gabriel R. Bitran and Devanath Tirupati, "Planning and Scheduling for Epitaxial Wafer Production Facilities"
- 11:40 Charles F. Ferguson, "Strategic Risk in the American Microelectronics and Computer Systems Industries"
- 12:20 BAG LUNCH. Tables are set up in Room 34-401

SESSION III. Chairman: Dr. Lenwood Heath

- 1:30 David Standley, and John L. Wyatt, Jr., "Improved Signal Delay Bounds for RC Tree Networks"
- 1:50 M. Mehregany, R. T. Howe, and S. D. Senturia, "Novel Microstructures for the Study of Residual Stress in Polyimide Films"
- 2:10 F. Thomson Leighton and Peter Shor, "Improved Algorithms for Wafer-Scale Integration of 2-D Systolic Arrays"
- 2:30 H.-J. Kim and Carl V. Thompson, "Effects of Dopants on Grain Growth in Thin Polycrystalline Silicon Films"
- 2:50 SNACK BREAK

SESSION IV. Chairman: Professor Christopher J. Terman

- 3:20 Charles E. Leiserson and Bruce M. Maggs, "Communication-Efficient Parallel Graph Algorithms"
- 3:40 Scott Chang and Roger T. Howe, "Resonant Microbridge Accelerometer"
- 4:00 Alan Sherman, "Algorithms for Placing Modules on a Custom VLSI Chip"
- 4:20 Thye-Lai Tung, Dimitri A. Antoniadis, and Jerome Connor, "Silicon Dioxide Flow during Oxidation: Boundary Value Formulation of an Incompletely Understood Physical Effect"

4:40 ADJOURN



Massachusetts
Institute
of Technology

Microsystems
Research
Center

Cambridge
Massachusetts
02139

Room 39-321
Telephone
(617) 253-8138

Agenda
Fall 1986 VLSI Research Review
December 15, 1986

9:00 Welcome and Introduction, Paul Penfield, Jr.

SESSION I. Chairman: Donald E. Troxel

9:10 G. M. Shedd, A. D. Dubner, H. Lezec, and J. Melngailis, "Focused Ion Beam Induced Deposition of Gold"

9:30 Johan Hastad, Tom Leighton, and Mark Newman, "Fault Tolerance in Hypercubes"

9:50 Martin A. Schmidt, Joseph H. Haritonidis, Roger T. Howe, and Stephen D. Senturia, "A Micromachined Floating-Element Shear Sensor"

10:10 A. D. Huelsman, E. Yoon, P. Parris, and R. Reif, "Epitaxial Growth of GaAs by Plasma-Enhanced Metal-Organic Chemical Vapor Deposition"

10:30 COFFEE BREAK

SESSION II. Chairman: Rosemary L. Smith

11:00 Mark W. Reichelt, Wayne H. Wolf, and Jonathan Allen, "An Improved Cell Model for Hierarchical Constraint Graph Compaction"

11:20 Charles Selvidge, and Adam Malamy, "Magnetostatic I/O Techniques for Integrated Circuits"

11:40 Brian E. Thompson, Albert D. Richards, and Herbert H. Sawin, "Continuum Modeling of Radio-Frequency Discharges for Plasma Etching"

12:00 Joe Kilian, Shlomo Kipnis, and Charles E. Leiserson, "The Organization of Permutation Architectures with Multiple-Pin Interconnections"

12:20 BAG LUNCH. Tables are set up in Room 34-401

SESSION III. Chairman: Emanuel Sachs

1:40 R. Jayaraman, W. Yang, and C. G. Sodini, "MOS Electrical Characteristics of Low Pressure Re-oxidized Nitrated-oxide"

2:00 Stanley B. Gershwin, "A Hierarchical Framework for VLSI Manufacturing Systems Scheduling"

2:20 Gahvam Shahidi, Dimitri Antoniadis, and Hank Smith, "Velocity Overshoot at Room Temperature Using Si Short Channel MOSFET's"

2:40 Andrew Goldberg, "A New Approach to the Maximum Flow Problem"

3:00 SNACK BREAK

SESSION IV. Chairman: William J. Dally

3:30 Tow C. Chong, and Clifton G. Fonstad, "Growth of High Quality GaAs Layers on Si Substrates by Molecular Beam Epitaxy"

3:50 Silvano A. Brewster, and Jeffrey H. Lang, "Probabilistic Analysis of Soft Errors in VLSI with Applications to Digital Control Systems"

4:10 Mark Shirley, "Generating Tests by Exploiting Designed Behavior"

4:30 Khalid Ismail, "Modeling of Compound Semiconductor Devices"

4:50 ADJOURN



Massachusetts
Institute
of Technology

Microsystems
Research
Center

Cambridge
Massachusetts
02139

Room 39-321
Telephone
(617) 253-8138

Agenda
Spring 1987 VLSI Research Review
May 18, 1987

8:55 Welcome and Introduction, Paul Penfield, Jr.

SESSION I. Chairman: Roger T. Howe

9:00 Thomas H. Cormen, "Efficient Multichip Partial Concentrator Switches"

9:20 Donald G. Baltus, "Generating Efficient Layouts from Optimized Circuit Schematics"

9:40 Wai L. Lee and Charles G. Sodini, "A Higher-Order Interpolative Modulator Topology for High-Resolution Oversampling A/D Converters"

10:00 Donald E. Troxel, "Computer-aided Fabrication of Integrated Circuits"

10:20 Michael B. McIlrath, "Representation of IC Manufacturing Process Flows"

10:40 COFFEE BREAK

SESSION II. Chairman: Jeffrey H. Lang

11:00 Christine S. Lam and Clifton G. Fonstad, "Improved MODFET Performance through Ion Implantation in the Gate Region"

11:20 Serge A. Plotkin, "Parallel Symmetry-breaking in Sparse Graphs"

11:40 Lynne Brocco, "Timing Simulation of VLSI Circuits Using Macromodels"

12:00 Tom Knight, "A Self Terminating Low Voltage Swing CMOS Output Driver"

12:20 BAG LUNCH. Tables are set up in Room 34-401

SESSION III. Chairman: Emanuel Sachs

1:30 Erik H. Anderson and Henry I. Smith, "Fabrication by Electron-Beam Lithography of X-Ray Masks with 50 nm Linewidths and Replication by X-ray Nanolithography"

1:50 Tam-Anh Chu, "Synthesis of Self-timed VLSI Circuits from Graph-Theoretic Specifications"

2:10 Joseph T. Kung, "A Digital Technique for Precise Measurement of Capacitor Differences, with Application to Capacitive Integrated Sensors"

2:30 Peter O'Brien, John L. Wyatt, Jr., Thomas Savarino, and James Pierce, "Fast On-Chip Delay Estimation for Cell-based Emitter Coupled Logic"

2:50 Mark G. Allen and Stephen D. Senturia, "Microfabricated Test Structures for Adhesion Measurement"

3:10 SNACK BREAK

SESSION IV. Chairman: Martin F. Schlecht

3:30 Vincent M. McNeil, Lloyd D. Clark, Jr., and David J. Edell, "Optimization of the Noise Performance of Active Neural Transducers"

3:50 William J. Dally, Linda Chao, Andrew Chien, Soha Hassoun, Waldemar Horvat, Jon Kaplan, Paul Song, Brian Totty, and Scott Wills, "Architecture of a Message-Driven Processor"

4:10 Roger C. Perkins, "Copper-Polyimide Interconnects for Ceramic Chip Carriers"

4:30 Lance A. Glasser and John L. Wyatt, Jr., "Frequency Limitations in Circuits Composed of Linear Devices"

4:50 ADJOURN



Massachusetts
Institute
of Technology

**Microsystems
Research
Center**

Cambridge
Massachusetts
02139

Room 39-321
Telephone
(617) 253-8138

Agenda
Fall 1987 VLSI Research Review
December 14, 1987

8:45 Welcome and Introduction, Paul Penfield, Jr.

SESSION I. Chairman: Martin F. Schlecht

- 8:50 Tom Leighton and Eric Schwabe, "Space-Efficient Queue Management Using Fixed-Connection Networks"
- 9:10 Guy E. Blelloch, "Scans as Primitive Parallel Operations"
- 9:30 William J. Dally and Paul Song, "Design of a Self-Timed VLSI Multicomputer Communication Controller"
- 9:50 Robert A. Iannucci, "von Neumann / Dataflow Processor"
- 10:10 Gregory M. Papadopoulos, "Monsoon Dataflow Processor"

10:30 COFFEE BREAK

SESSION II. Chairman: Charles G. Sodini

- 10:50 George Prueger, Emanuel Sachs, and Roberto Guerrieri, "Equipment Model for the Low Pressure Chemical Vapor Deposition of Polysilicon"
- 11:10 Silvano A. Brewster and Jeffrey H. Lang, "Probabilistic Analysis of Soft Errors in VLSI With Applications to Digital Control Systems"
- 11:30 Jon P. Wade and Charles G. Sodini, "The MIT Database Accelerator: 2K-trit Circuit Design"
- 11:50 Curtis Tsai, Kathleen Early, and Rafael Reif, "The MIT Database Accelerator: Process Integration"
- 12:10 Frederick P. Herrmann and Charles G. Sodini, "The MIT Database Accelerator: Ternary Logic and Algorithms"

12:30 BAG LUNCH. Tables are set up in Room 34-401

SESSION III. Chairman: Jacob K. White

- 1:30 M. A. Kastner, S. B. Field, J. C. Licini, and S. L. Park, "Anomalous Magnetoresistance of the Electron Gas in a Restricted Geometry"
- 1:50 Henri J. Lezec, Leonard J. Mahoney, Mark I. Shepard, and John Melngailis, "Focused Ion Beam Implantation"
- 2:10 G. G. Shahidi, D. A. Antoniadis, and Henry I. Smith, "Reduction of Channel-Hot-Electron-Generated Substrate Current in Sub-150 nm Channel Length Si MOSFETs"
- 2:30 M. L. Schattenburg, I. Tanaka, and Henry I. Smith, "Microgap X-Ray Nanolithography"
- 2:50 Erik H. Anderson and Henry I. Smith, "Progress in X-Ray Nanolithography Pattern Generation"

3:10 SNACK BREAK

SESSION IV. Chairman: Herbert H. Sawin

- 3:30 Keith E. Crowe and Rosemary L. Smith, "Investigation of Mechanical Properties of Stoichiometric LPCVD Silicon Nitride Films"
- 3:50 A. D. Huelsman and R. Reif, "Remote Plasma Deposition of GaAs and GaAsP by Metal-Organic Chemical Vapor Deposition"
- 4:10 Shih-Fang Chuang, Xiao-Ge Zhang, and Rosemary L. Smith, "Porous Silicon Layer Morphologies: Formation Parameters and Their Influences"
- 4:30 P. C. Searson, "Corrosion in Electronic Materials"
- 4:50 Herbert J. Neuhaus and Stephen D. Senturia, "History Effects in Polymeric Insulators: How Ions Can Complicate Characterization"

5:10 ADJOURN



APPENDIX D.

Massachusetts
Institute
of Technology

**Microsystems
Research
Center**

Cambridge
Massachusetts
02139

Room 39-321
Telephone
(617) 253-8138

Dear Colleague:

This letter is in response to your inquiry about the 1986 MIT VLSI Tools Release. The tools are available to the public within the United States and Canada and are designed or coerced to run on Berkeley VAX UNIX, version 4.2. The tape is written in tar format at 1600 bpi and requires about eight megabytes of disk space.

We require prepayment of the handling fee of \$500 and a letter stating that the tools will not be redistributed outside your organization or to foreign components of your organization, that the tools will not be used as the basis of a commercial software or hardware product, and that you understand that the tools are supplied "as is," without any warranty. You may sign the form letter enclosed or you may use similar wording on your own letterhead. The handling fee is waived for universities, government agencies, and members of the MIT Microsystems Industrial Group (as of October 1987: Analog Devices, AT&T, DEC, Eaton Ion Beam, GCA, GE, GM, GenRad, Sipex Corp., IBM, Keithley Instruments, NCR, Polaroid, Raytheon, and Teradyne). You will receive one tape and two copies of the manual. Additional manuals are available for \$15 each. Make your check payable to MIT-VLSI and send it and the agreement letter to:

VLSI Tools Release
Microsystems Research Center
Room 39-321
Massachusetts Institute of Technology
Cambridge, MA 02139
Telephone (617) 253-8138

The following MIT VLSI tools are included in the release:

Circuit Description and Simulation: NET, CNET, PRESIM, RSIM, RNL by
Chris Terman
HPEDIT, An LSI Artwork Editor, by Robert Armstrong
XDRC Programmer's Guide, by Robert Armstrong
RSG: Design-by-Example Regular Structure Generator, by Cyrus S. Bamji
The EXCL Circuit Extractor, by Stephen P. McCormick
The CNODE Transistor Network Extractor, by Stephen P. McCormick
NMOS and CMOS Models, by Lance A. Glasser

Most of the programs in the present software release are written either in C or CLU. A CLU compiler is not necessary to use these VLSI tools on an as-is basis, but is necessary if you want to change them. The Manual describes how to obtain more information on CLU.

If you have any questions, feel free to call the above number for information.

Sincerely,

Barbara Tilson

Barbara Tilson
Assistant to the Director



APPENDIX D. (continued)

Massachusetts
Institute
of Technology

**Microsystems
Research
Center**

Cambridge
Massachusetts
02139

Room 39-321
Telephone
(617) 253-8138

**Microsystems Research Center
Room 39-321
Massachusetts Institute of Technology
Cambridge, MA 02139**

Subject: 1986 MIT VLSI Tools Tape

I hereby request, on behalf of my organization _____,
a copy of the 1986 MIT VLSI Tools tape. I agree that:

The tools are supplied without the normal license fee, and that my organization will not incorporate any of them into a commercial product, or sell access to them, without prior written agreement from MIT.

Since some of the tools were developed under sponsorship that restricts worldwide distribution, my organization will not distribute the tools to other organizations, or to any other locations of my organization, and in no case to anywhere outside the United States and Canada.

The tools are supplied "as is," without any kind of warranty, and MIT does not promise to support them in any way.

Accepted:

Signature

Printed Name

Title

Date

Organization/Company Name

Address

City, State, Zip

Telephone No.

APPENDIX E. VLSI MEMO SERIES (through December 1987)

- 80-1 "Integrated Circuit Series," Paul Penfield, Jr., January 1980. (4 pp.)
- 80-2 "Using APL on the Speech System 20," Paul Penfield, Jr., January 1980. (7 pp.)
- 80-3 "Design Considerations for a Partial Differential Equation Machine," Arvind and Randal E. Bryant, January 1980. (10 pp.)
- 80-4 "Information Transfer and Area-Time Tradeoffs for VLSI Multiplication," Harold Abelson and Peter Andreac, January 1980. (9 pp.)
- 80-5 "A Monolithic Moisture Sensor," Kou Togashi and Stephen D. Senturia, January 1980. (9 pp.)
- 80-6 "The SCHEME-79 Chip," Jack Holloway, Guy L. Steele, Gerald J. Sussman, and Alan Bell, January 1980. (43 pp.)
- 80-7 "MOSSIM: A Logic-Level Simulator for MOS LSI. User's Manual Version 2," Randal E. Bryant, February 1980. (19 pp.)
- 80-8 "The Implementation of Regular Logic with Feedback Reduced PLAs," Lance A. Glasser, February 1980. (5 pp.)
- 80-9 "Reflections on AIDS-79," Paul Penfield, Jr., March 1980. (4 pp.)
- 80-10 "Student Guide to VLSI Research at M.I.T.," Paul Penfield, Jr., Revised yearly. (15 pp.)
- 80-11 "Introduction to the Design Rule Checker," Larry Seiler, March 1980. (3 pp.)
- 80-12 "Geometrical Primitive Objects for Integrated Circuit Specification," Larry Seiler, March 1980. (6 pp.)
- 80-13 "The Cost of Designing for Testability in Terms of Integrated Circuit Yield," Lance A. Glasser, March 1980. (9 pp.)
- 80-14 "AIDS-79 User's Manual," Paul Penfield, Jr., March 1980. (37 pp.)
- 80-15 "The Nature of VLSI Circuit Design," Lance A. Glasser, May 1980. (5 pp.)
- 80-16 "Artwork Analysis Tools for VLSI Circuits," Clark M. Baker, June 1980. (75 pp.)
- 80-17 "An Integrated Circuit Two-Phase Programmable Clock Generator," Fasal Abbas, June 1980. (81 pp.)
- 80-18 "A Microprocessor-Compatible Charge-Flow Transistor Oscillator," Harvey W. Jong, June 1980. (55 pp.)
- 80-19 "The Design of Integrated Distributed Amplifiers," Jeffrey C. McHarg, June 1980. (95 pp.)
- 80-20 "Documentation of the RSA Chip Assembler," Ronald L. Rivest, July 1980. (27 pp.)
- 80-21 "MOSSIM: A Logic-Level Simulator for MOS LSI - User's Manual," Randal E. Bryant, July 1980. (19 pp.)
- 80-22 "A VLSI Implementation of a Two-by-Two Packet Router," Paul S. Ries, July 1980. (98 pp.)
- 80-23 "A Test Generation Technique for Devices Without Gate-Level Descriptions," Robert A. Todd, July 1980. (50 pp.)
- 80-24 "An Algorithm for MOS Logic Simulation," Randal E. Bryant, July 1980. (16 pp.)
- 80-25 "An Interactive PLA Generator as an Archetype for a New VLSI Design Methodology," Lance A. Glasser and Paul Penfield, Jr., July 1980. (16 pp.)
- 80-26 "A Processing Element for a Large Multiple Processor Dataflow Machine," Arvind, Vinod Kathail, and Keshav Pingali, August 1980. (5 pp.)
- 80-27 "A Polynomial Time Algorithm for Optimal Routing Around a Rectangle," Andrea S. LaPaugh, August 1980. (28 pp.)
- 80-28 "Conversion of Algorithms to Custom Integrated Circuits: An M.I.T. Perspective," Jonathan Allen, August 1980. (3 pp.)
- 80-29 "Report on the NBS/JPL/USC-ISI Test Chip Workshop, Pasadena, California, August 20, 1980," Mark G. Johnson, September 1980. (28 pp.)

VLSI MEMO SERIES (continued)

- 80-30 "Tools for Verifying Integrated Circuit Designs," Clark Baker and Chris Terman, September 1980. (28 pp.)
- 80-31 "The Design Procedure Language Manual," John Batali and Anne Hartheimer, September 1980. (81 pp.)
- 80-32 "The Definition and Implementation of a Computer Programming Language Based on Constraints," Guy L. Steele, Jr., December 1980. (371 pp.)
- 80-33 "VLSI Design Automation Activities at M.I.T.," J. Allen and P. Penfield, Jr., Rev. July 1981. (30 pp.)
- 80-34 "Addendum to AIDS-79 User's Manual," Paul Penfield, Jr., October 1980. (9 pp.)
- 80-35 "LSIAA: LSI Artwork Analysis System," Gary E. Kopec, November 1980. (16 pp.)
- 80-36 "The Analog Behavior of Digital Integrated Circuits," Lance A. Glasser, December 1980. (10 pp.)
- 80-37 "Architectures for Analog LSI Implementations of Speech Processing Systems," Patrick W. Bosshart, December 1980. (186 pp.)
- 80-38 "Algorithms for Integrated Circuit Layout: An Analytic Approach," Andrea S. LaPaugh, December 1980. (179 pp.)
- 80-39 "The Apiary Network Architecture for Knowledgeable Systems," Carl Hewett, December 1980. (11 pp.)
- 81-40 "Signal Delay in RC Tree Networks," Jorge Rubinstein, Paul Penfield, Jr. and Mark A. Horowitz, January 1981. (7 pp.)
- 81-41 "Special Purpose Hardware for Design Rule Checking," Larry Seiler, February 1981. (20 pp.)
- 81-42 "Electron Beam Testing and Restructuring of Integrated Circuits," D. C. Shaver, February 1981. (17 pp.)
- 81-43 "A One Transistor RAM for MPC Projects," James J. Cherry and Gerald L. Roylance, February 1981. (13 pp.)
- 81-44 "A Multiproject Chip Approach to the Teaching of Analog MOS LSI and VLSI," Yannis P. Tsividis and Dimitri A. Antoniadis, February 1981. (17 pp.)
- 81-45 "The Scaling of Clock Noise in MOS Integrated Circuits," Lance A. Glasser, March 1981. (4 pp.)
- 81-46 "New Layouts for the Shuffle-Exchange Graph," Daniel Kleitman, Frank Thomson Leighton, Margaret Lepely and Gary L. Miller, March 1981. (15 pp.)
- 81-47 "MOSSIM: A Switch-Level Simulator for MOS LSI," Randal Bryant, April 1981. (15 pp.)
- 81-48 "Signal Delay in MOS Interconnections," Paul Penfield, Jr. and Jorge Rubinstein, April 1981. (15 pp.)
- 81-49 "MOSFETs on Silicon Prepared by Moving Melt Zone Recrystallization of Encapsulated Polycrystalline Silicon on an Insulating Substrate," E. Maby, M. Geis, Y. LeCoz, D. Silversmith, R. Mountain, and D. A. Antoniadis, May 1981. (13 pp.)
- 81-50 "A Switch-Level Simulation Model for Integrated Logic Circuits," Randal E. Bryant, June 1981. (219 pp.)
- 81-51 "A Hardware Compiler for Boolean Logic Functions," Douglas D. Williams, June 1981. (53 pp.)
- 81-52 "A Switch-Level Model of MOS Logic Circuits," Randal E. Bryant, June 1981. (10 pp.)
- 81-53 "MSHOW: Multi-Media Layout Display Program," Gary E. Kopec, July 1981. (13 pp.)
- 81-54 "The Impact of VLSI on Signal Processing Algorithms and Architectures," Gary E. Kopec, July 1981. (7 pp.)
- 81-55 "Principal Values and Branch Cuts in Complex APL," Paul Penfield, Jr., July 1981. (9 pp.)
- 81-56 "Chopper Stabilization of MOS Operation Amplifiers Using Feed-Forward Techniques," Michael C. W. Coln, July 1981. (16 pp.)
- 81-57 "AIDS, APL Integrated-Circuit Design System," Paul Penfield, Jr., July 1981. (8 pp.)

VLSI MEMO SERIES (continued)

- 81-58 "Optimal Layouts for Small Shuffle-Exchange Graphs," Frank T. Leighton and Gary L. Miller, August 1981. (10 pp.)
- 81-59 "A Low Temperature Process to Increase the Grain Size in Polysilicon Films," Rafael Reif and Jonathan E. Knott, August 1981. (12 pp.)
- 81-60 "A Low Temperature Process to Produce Large-Grain Uniformly-Oriented Polycrystalline Silicon Films on Amorphous Substrates," Jonathan E. Knott, August 1981. (50 pp.)
- 81-61 "HISDL - A Structure Description Language," Willie Y-P. Lim, September 1981. (16 pp.)
- 81-62 "The Syntactic Analysis of VLSI Systems Using Graphs," Lance A. Glasser, September 1981. (5 pp.)
- 81-63 "Clocking Semi-Groups for VLSI Circuit Analysis," Lance A. Glasser, September 1981. (4 pp.)
- 81-64 "Vertical Single-Gate CMOS Inverters on Laser-Processed Multilayer Substrates," G. T. Goeloe, E. Maby, D. J. Silversmith, R. W. Mountain, and D. A. Antoniadis, September 1981. (3 pp.)
- 81-65 "An Introduction to DPL," John Batali, October 1981. (24 pp.)
- 81-66 "Optimal Placement for River Routing," Charles E. Leiserson and Ron Y. Pinter, October 1981. (16 pp.)
- 81-67 "Oxidation Induced Point Defects in Silicon," Dimitri A. Antoniadis, October 1981. (24 pp.)
- 81-68 "Use of Process and 2-D MOS Simulation in the Study of Doping Profile Influence on S/D Resistance in Short Channel MOSFET's," P. Antognetti, C. Lombardi, and D. Antoniadis, October 1981. (4 pp.)
- 81-69 "Transmission Diffraction Gratings for Soft X-Ray Spectroscopy and Spatial Period Division," Andrew Michael Hawryluk, October 1981. (182 pp.)
- 81-70 "Dynamics of Oxygen Incorporation During Czochralski Silicon Growth," David Francis Bliss, November 1981. (69 pp.)
- 82-71 "New Lower Bounds for Channel Routing," Frank Thomson Leighton, January 1982. (9 pp.)
- 82-72 "Technology, Strategic Choice, and the Future Structure of Semiconductor Production," C. H. Ferguson and D. M. Raff, January 1982. (13 pp.)
- 82-73 "A Placement/Interconnect Channel Router: Cutting Your PI into Slices," James Joseph Koschella, February 1982. (45 pp.)
- 82-74 "The PI (Placement and Interconnect) System," Ronald L. Rivest, February 1981. (12 pp.)
- 82-75 "A 'Greedy' Channel Router," Ronald L. Rivest and Charles M. Fiduccia, February 1982. (11 pp.)
- 82-76 "DYCHAR: A Channel Router Which Uses Dynamic Channel Assignment," Seth D. Alford, February 1982. (92 pp.)
- 82-77 "Benchmark Channel-Routing Problems," Ronald L. Rivest, February 1982. (8 pp.)
- 82-78 "Electrical Properties of Line Defects in Thin Zone-Recrystallized Silicon Films on Silicon Dioxide," E. W. Maby and D. A. Antoniadis, February 1982. (13 pp.)
- 82-79 "A Canary Straw Bird," Lance A. Glasser, February 1982. (8 pp.)
- 82-80 "SPICE," Lance A. Glasser, March 1982. (113 pp.)
- 82-81 "Ion Implantation of Si in Be-Implanted $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$," A.N.M.M. Choudhury, N. J. Slater, K. Tabatabaie-Alavi, and C. G. Fonstad, March 1982. (10 pp.)
- 82-82 "Ion Implantation of Be in $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$," K. Tabatabaie-Alavi, A.N.M.M. Choudhury, N. J. Slater, and C. G. Fonstad, March 1982. (14 pp.)
- 82-83 "Very Low Resistance Ohmic Contacts on p-type InP by Direct Plating," K. Tabatabaie-Alavi, A.N.M.M. Choudhury, N. J. Slater, and C. G. Fonstad, March 1982. (13 pp.)
- 82-84 "An Iterative Solution to Poisson's Equation for Doped Heterostructure Devices," James Cheming Ong, March 1982. (46 pp.)

VLSI MEMO SERIES (continued)

- 82-85 "MOS Implementations of TTL Architectures: A Case Study," William H. Evans and Jonathan Allen, March 1982. (4 pp.)
- 82-86 "Minimizing the Longest Edge in a VLSI Layout," Sandeep N. Bhatt and Charles E. Leiserson, March 1982. (9 pp.)
- 82-87 "How to Assemble Tree Machines," Sandeep N. Bhatt and Charles E. Leiserson, March 1982. (8 pp.)
- 82-88 "A Layout Strategy for VLSI Which is Provably Good," Frank Thomson Leighton, March 1982. (14 pp.)
- 82-89 "New Lower Bound Techniques for VLSI," Frank Thomson Leighton, March 1982. (30 pp.)
- 82-90 "Optimizing Synchronous Systems," Charles E. Leiserson and James B. Saxe, March 1982. (24 pp.)
- 82-91 "A Hardware Assisted Design Rule Check Architecture," Larry Seiler, April 1982. (7 pp.)
- 82-92 "Plasma-Assisted Chemical Vapor Deposition of Crystalline Silicon," T. J. Donahue, R. Reif and W. R. Burger, April 1982. (3 pp.)
- 82-93 "Phosphorus Incorporation During Silicon Epitaxial Growth in a CVD Reactor," R. Reif, April 1982. (34 pp.)
- 82-94 "Small is Big: The Microelectronic Challenge," Paul Penfield, Jr., April 1982. (15 pp.)
- 82-95 "Orientation Selection by Zone Melting Silicon Films through Planar Constrictions," Henry I. Smith, H. A. Atwater and M. W. Geis, April 1982. (2 pp.)
- 82-96 "The Mechanism of Orientation in Si Graphoepitaxy Using a Strip-Heater Oven," Henry I. Smith and M. W. Geis, April 1982. (2 pp.)
- 82-97 "An Etch Pit Technique for Analyzing Crystallographic Orientation in Si Films," K. A. Bezjian, Henry I. Smith, J. M. Carter and M. W. Geis, April 1982. (10 pp.)
- 82-98 "Optimal Layer Assignment for Interconnect," Ron Y. Pinter, April 1982. (9 pp.)
- 82-99 "On Routing Two-Point Nets Across a Channel," Ron Y. Pinter, April 1982. (9 pp.)
- 82-100 "Digital Circuit Optimization," Charles E. Leiserson, Flavio M. Rose, and James B. Saxe, April 1982. (17 pp.)
- 82-101 "Wafer-Scale Integration of Systolic Arrays," Frank Thomson Leighton and Charles E. Leiserson, April 1982. (29 pp.)
- 82-102 "Three-Dimensional Circuit Layouts," Frank Thomson Leighton and Arnold L. Rosenberg, April 1982. (13 pp.)
- 82-103 "Layouts for the Shuffle-Exchange Graph and Lower Bound Techniques for VLSI," Frank Thomson Leighton, June 1982. (105 pp.)
- 82-104 "Exploiting Hierarchy in the Analysis of VLSI Systems," Daniel Wayne Weise, June 1982. (65 pp.)
- 82-105 "Implementation of a Displacement Processor Data Path," Brian C. Williams, June 1982. (38 pp.)
- 82-106 "An Application of Number Theory to the Organization of Raster-Graphics Memory," Benny Chor, Charles E. Leiserson, Ronald L. Rivest, June 1982. (15 pp.)
- 82-107 "VLSI Micro-Cell Layout Automation," Aki Fujimura, June 1982. (216 pp.)
- 82-108 "Schematic Diagram Plotter," Carol J. Chiang, June 1982. (26 pp.)
- 82-109 "The Structural Crisis of American Microelectronics: Analysis and Policy Implications," Charles H. Ferguson, June 1982. (36 pp.)
- 82-110 "Layouts for the Shuffle-Exchange Graph Based on the Complex Plane Diagram," Frank Thomson Leighton, Margaret Lepley and Gary L. Miller, July 1982. (21 pp.)
- 82-111 "A Functional Tester Design for the University Environment," Mark Sherred, July 1982. (36 pp.)
- 82-112 "User's Guide to NET, PRESIM, and RNL/NL," Christopher J. Terman, July 1982. (45 pp.)

VLSI MEMO SERIES (continued)

- 82-113 "Deep-UV Spatial-Period-Division Using An Excimer Laser," A. M. Hawryluk, H. I. Smith, R. M. Osgood, and D. J. Erlich, July 1982. (10 pp.)
- 82-114 "Models for VLSI Circuits," F. M. Rose, July 1982. (47 pp.)
- 82-115 "VLSI Circuit Theory," L. A. Glasser, and P. Penfield, Jr., August 1982. (3 pp.)
- 82-116 "Automated Calculation of Device Sizes for Digital IC Designs," Lennox P. John Hoyte, September 1982. (59 pp.)
- 82-117 "Introductory CMOS Techniques," Lance A. Glasser, and William S. Song, September 1982. (28 pp.)
- 82-118 "Orientation Selection by Zone Melting Silicon Films Through Planar Constrictions," H. A. Atwater, H. I. Smith, and M. W. Geis, September 1982. (14 pp.)
- 82-119 "Optimal Tile Salvage," Francine Berman, Frank Thomson Leighton, and Lawrence Snyder, September 1982. (21 pp.)
- 82-120 "An MOS LSI Digital Signal Processor for Speech Synthesis Applications," William Hall Evans, October 1982. (158 pp.)
- 82-121 "Electrical Parameter Extraction of MOSFETs Fabricated on Silicon-on-Insulator Films Using a Numerical Solution of Poisson's Equation," Yannick L. Le Coz, November 1982. (88 pp.)
- 82-122 "Ion Implantation of Be and Si for GaInAs/AlInAs/InP Bipolar Heterojunction Transistors," Nancy Jean Slater, November 1982. (142 pp.)
- 82-123 "(In,Ga)As/(In,Al)As Heterojunction Lateral PNP Transistors," K. Tabatabaie-Alavi, A.N.M.M. Choudhury, K. Alavi, J. Vlcek, N. J. Slater, C. G. Fonstad, and A. Y. Cho, November 1982. (4 pp.)
- 82-124 "Ion-Implanted $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}/\text{In}_{0.52}\text{Al}_{0.48}\text{As}$ Lateral PNP Transistors," K. Tabatabaie-Alavi, A.N.M.M. Choudhury, K. Alavi, J. Vlcek, N. J. Slater, C. G. Fonstad, and A. Y. Cho, November 1982. (10 pp.)
- 82-125 "Ion Implantation Doping of (In,Ga)As and (In,Al)As," K. Tabatabaie-Alavi, A.N.M.M. Choudhury, K. Alavi, J. Vlcek, N. J. Slater, C. G. Fonstad, A. Y. Cho, and W. Rowe, November 1982. (8 pp.)
- 82-126 "The Sensitivity of Inverter Delay to Details of the Input Waveform: A Variational Approach," J. L. Wyatt, November 1982. (9 pp.)
- 82-127 "Inequality Theorems for Nonlinear Differential Equations," J. L. Wyatt, November 1982. (12 pp.)
- 82-128 "Monotone Behavior of Nonlinear RC Meshes," J. L. Wyatt, November 1982. (12 pp.)
- 82-129 "An Approximation Algorithm for Manhattan Routing," B. S. Baker, S. N. Bhatt, and F. T. Leighton, December 1982. (16 pp.)
- 82-130 "The Impact of Layer Assignment Methods on Layout Algorithms for Integrated Circuits," Ron Yair Pinter, December 1982. (144 pp.)
- 83-131 "A Calibrated Digital Delay Line Implemented in VLSI," Jonathan D. Taft, January 1983. (58 pp.)
- 83-132 "Optimization of the MacPitts Silicon Compiler for Telecommunication Circuitry," J. R. Fox, January 1983. (21 pp.)
- 83-133 "Design of a Fully Associative Cache Memory Controller," John Chia Lin Hou, January 1983. (150 pp.)
- 83-134 "An Expert System for VLSI Design," Richard Zippel, February 1983. (3 pp.)
- 83-135 "The Design, Implementation and Testing of a Self-Timed Two by Two Packet Router," Tam-Anh Chu, February 1983. (41 pp.)
- 83-136 "On Bisecting Random Graphs," Thang Nguyen Bui, February 1983. (41 pp.)
- 83-137 "Test Generation Algorithms: Overcoming the Von Neumann Bottleneck," Glenn A. Kramer, April 1983. (10 pp.)
- 83-138 "A 4K x 1 Static Random Access Memory," Glenn A. Kramer, April 1983. (44 pp.)
- 83-139 "Waveform Bounding for Functional Timing Analysis of MOS Digital Integrated Circuits," John L. Wyatt, Jr., April 1983. (5 pp.)

VLSI MEMO SERIES (continued)

- 83-140 "Spatial Monotonicity and Positive Invariance for Nonlinear RC Lines and Trees," John L. Wyatt, Jr. and Paul Bassett, April 1983. (17 pp.)
- 84-141 "Size, Power and Speed," Maurice V. Wilkes, April 1983. (4 pp.)
- 83-142 "Diogenes: a Methodology for Designing Fault-Tolerant VLSI Processor Arrays," F. Thomson Leighton, Fan R. K. Chung, and Arnold L. Rosenberg, April 1983. (7 pp.)
- 83-143 "Zone-Melting Recrystallization of InSb on Oxidized Silicon Substrates," Christopher James Keavney, June 1983. (74 pp.)
- 83-144 "High Performance NMOS Operational Amplifier Design," Jason Redgrave, June 1983. (30 pp.)
- 83-145 "Partial Ordering and Monotone Sensitivity for Nonlinear RC Meshes and Lines," John L. Wyatt, Jr., June 1983. (14 pp.)
- 83-146 "Automatic Generation of Three-Dimensional Circuit Layouts," Frank Thomson Leighton and Arnold L. Rosenberg, June 1983. (4 pp.)
- 83-147 "A New Approach to Timing Analysis of Digital MOS IC's," John L. Wyatt, Jr., July 1983. (5 pp.)
- 83-148 "The Waveform Bounding Approach to Timing Analysis of Digital MOS IC's," John L. Wyatt, Jr., Charles Zukowski, Lance A. Glasser, Paul Bassett, and Paul Penfield, Jr., July 1983. (4 pp.)
- 83-149 "Control of Silicon Film Recrystallization Using Lithography with Application to Photovoltaics," Harry Albert Atwater, Jr., July 1983. (124 pp.)
- 83-150 "Monotone Sensitivity Theorem for Nonlinear, Nonuniform RC Transmission Lines," John L. Wyatt, Jr., August 1983. (9 pp.)
- 83-151 "Algorithms for Integrated Circuit Signal Routing," Alan Baratz, October 1983. (116 pp.)
- 83-152 "Parallel Computation Using Meshes of Trees," Tom Leighton, October 1983. (19 pp.)
- 83-153 "Global Wire Routing in Two-Dimensional Arrays," R. M. Karp, F. T. Leighton, R. L. Rivest, C. D. Thompson, U. Vazirani, and V. Vazirani, October 1983. (7 pp.)
- 83-154 "Simulation Tools for Digital LSI Design," Christopher Jay Terman, October 1983. (158 pp.)
- 83-155 "Sensitivity of Nonlinear 1-Port Resistor Networks," Charles A. Zukowski and John L. Wyatt, Jr., October 1983. (5 pp.)
- 83-156 "Power Distribution Techniques for VLSI Circuits," William S. Song and Lance A. Glasser, November 1983. (33 pp.)
- 83-157 "A Placement/Interconnect Channel Router: Cutting your PI into Slices," James J. Koschella, December 1983. (46 pp.)
- 84-158 "Lectures on Nonlinear Circuit Theory," John L. Wyatt, Jr., January 1984. (202 pp.)
- 84-159 "Circuit Simulation with Iterating Bounds," Charles A. Zukowski, January 1984. (4 pp.)
- 84-160 "Functional Test Pattern Generation for Integrated Circuits," Ramin Khorram, January 1984. (71 pp.)
- 84-161 "Plasma Enhanced Chemical Vapor Deposition of Silicon Epitaxial Layers," Rafael Reif, February 1984. (14 pp.)
- 84-162 "Low Temperature Silicon Epitaxy Using Low Pressure Chemical Vapor Deposition with and without Plasma Enhancement," T. Donahue, W. Burger, R. Reif, February 1984. (12 pp.)
- 84-163 "Abnormal Grain Growth in Ultra-Thin Films of Germanium on Insulator," T. Yonehara, C.V. Thompson, H.I. Smith, February 1984. (21 pp.)
- 84-164 "HPLA: A Design by Example PLA Generator," Cyrus Bamji, March 1984. (19 pp.)
- 84-165 "Qualitative Analysis of MOS Circuits," Brian C. Williams, April 1984. (90 pp.)
- 84-166 "Relaxing Bounds on Linear RC Mesh Circuits," Charles A. Zukowski, April 1984. (15 pp.)

VLSI MEMO SERIES (continued)

- 84-167 "A Framework for Solving VLSI Graph Layout Problems," Sandeep N. Bhatt and Frank Thomson Leighton, April 1984. (44 pp.)
- 84-168 "The Hitachi 2716 2K x 8 EPROM," Kevin D. Ball, April 1984. (37 pp.)
- 84-169 "Three-Dimensional Integrated Circuit Technology," Dimitri A. Antoniadis, May 1984. (11 pp.)
- 84-170 "Staggered CMOS: A Novel Three-Dimensional Technology," E. W. Maby and D. A. Antoniadis, May 1984. (6 pp.)
- 84-171 "Delay and Power Optimization in VLSI Circuits," Lance A. Glasser and Lennox P. J. Hoyte, May 1984. (7 pp.)
- 84-172 "Tight Bounds on the Complexity of Parallel Sorting," Tom Leighton, May 1984. (10 pp.)
- 84-173 "On the Pagenumber of Planar Graphs," Jonathan F. Buss and Peter W. Shor, May 1984. (3 pp.)
- 84-174 "Measurement of Minimum-Geometry MOS Transistor Capacitances," John J. Paulos and Dimitri A. Antoniadis, May 1984. (32 pp.)
- 84-175 "Solid-Phase Epitaxial Growth of Polycrystalline Silicon Films Amorphized by Ion Implantation," N. T. Quach and R. Reif, May 1984. (17 pp.)
- 84-176 "Bounding the Response of One-Way MOS Logic Gate Models," Charles A. Zukowski and Lance A. Glasser, May 1984. (22 pp.)
- 84-177 "Automatic Formatting of Logic Schematics," Ivan Oscar Tou, May 1984. (154 pp.)
- 84-178 "An Algorithm for Constructing Regions with Rectangles: Independence and Minimum Generating Sets for Collections of Intervals," Deborah S. Franzblau and Daniel J. Kleitman, May 1984. (13 pp.)
- 84-179 "Analytical and Numerical Study of the Sensitivity of Delay in a Typical MOS Inverter to the Shape of the Input Waveform," Pearl Yew and John L. Wyatt, Jr., May 1984. (34 pp.)
- 84-180 "Solid-Phase Epitaxial Regrowth of Ion-Implanted Low-Pressure Chemically Vapor Deposited Polycrystalline Silicon Films," Nhon Toai Quach, June 1984. (84 pp.)
- 84-181 "Plasma-Assisted Processing: The Etching of Polysilicon in a Cl_2 Discharge," Herbert H. Sawin, Albert D. Richards, and Brian E. Thompson, June 1984. (23 pp.)
- 84-182 "Three-Dimensional Circuit Layouts," Tom Leighton and Arnold L. Rosenberg, June 1984. (33 pp.)
- 84-183 "Optimizing the Dispersion Stabilization of Barium Titanate under Poly (Methyl Methacrylate-Styrene) Solution," H. D. Lee, R. L. Pober, and H. K. Bowen, June 1984. (28 pp.)
- 84-184 "Routing the Power and Ground Wires on a VLSI Chip," Andrew Strout Moulton, June 1984. (65 pp.)
- 84-185 "The Effect of High Fields on MOS Device and Circuit Performance," C. G. Sodini, P. K. Ko, and J. L. Moll, June 1984. (39 pp.)
- 84-186 "Contact Resistance and Interface Kinetics of RF Sputter Cleaned AlSi/TiW/Si Contacts in VLSI," Edward Ronald Equi, June 1984. (72 pp.)
- 84-187 "Formation and Processing of Monosized Borosilicate Powder," Lina V. Janavicius, June 1984. (73 pp.)
- 84-188 "Studies of Residual Stress in Amorphous Silicon," Peter Li-Ming Cheng, June 1984. (103 pp.)
- 84-189 "Mechanical Properties of Hydrogenated Amorphous Silicon Films," Leslie Virginia Atkins, June 1984. (46 pp.)
- 84-190 "Electrical Properties of Hydrogenated Amorphous Silicon Produced by Laser-Induced CVD," Christopher John Petti, June 1984. (61 pp.)
- 84-191 "EXCL: A Circuit Extractor for IC Designs," Steven P. McCormick, June 1984. (10 pp.)
- 84-192 "Polymerizable Monomers for Tape Casting of Ceramics," P. D. Calvert, July 1984. (17 pp.)
- 84-193 "A Distributed Bipolar Device for Monolithic Analog-to-Digital Conversion," Christopher Wood Mangelsdorf, July 1984. (284 pp.)

VLSI MEMO SERIES (*continued*)

- 84-194 "Autodoping in Silicon Epitaxy," Man Wong, July 1984. (54 pp.)
- 84-195 "Methodology Verification of Hierarchically Described VLSI Circuits," Isaac Leo Bain, July 1984. (77 pp.)
- 84-196 "Signal Delay in RC Mesh Networks," John L. Wyatt, Jr., August 1984. (8 pp.)
- 84-197 "Improved Bounds on Signal Delay in RC Trees Using Inequalities on the Derivatives of Node Voltages," Qingjian Yu and John L. Wyatt, Jr., August 1984. (60 pp.)
- 84-198 "Signal Delay in RC Meshes, Trees and Lines," John L. Wyatt, Jr., and Qingjian Yu, August 1984. (4 pp.)
- 84-199 "Measurement and Modeling of Small-Geometry MOS Transistor Capacitances," John James Paulos, August 1984. (307 pp.)
- 84-200 "Requirements for Computer-Aided Fabrication," P. Penfield, Jr., S. B. Gershwin, D. A. Hodges, C. M. Osborn, J. Reynolds, J. Shott, A. J. Steckl, and D. E. Troxel, August 1984. (16 pp.)
- 84-201 "Low Pressure Chemical Vapor Deposition of Titanium Silicide," P. Tedrow, V. Ilderem, and R. Reif, October 1984. (11 pp.)
- 84-202 "Silicon Epitaxy at 650-800°C Using Low Pressure Chemical Vapor Deposition Both With and Without Plasma Enhancement," T. J. Donahue and R. Reif, October 1984. (37 pp.)
- 84-203 "Low Temperature Silicon Epitaxy by Low Pressure Chemical Vapor Deposition With and Without Plasma Enhancement," Wayne R. Burger, October 1984. (119 pp.)
- 84-204 "CMOS LSI Design of a High-Throughput Digital Filter," Anne H. Park, October 1984. (88 pp.)
- 84-205 "Time Optimal Trajectories Associated with Voltage Bounds in RC Tree Networks," Han-Ngee Tan and John L. Wyatt, Jr., October 1984. (18 pp.)
- 84-206 "Manganese as a p-type Dopant for Liquid Phase Epitaxial $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$," Peter S. Whitney and Clifton G. Fonstad, October 1984. (22 pp.)
- 84-207 "Amorphous Silicon Produced by Laser Induced Chemical Vapor Deposition," Michel Meunier, October 1984. (114 pp.)
- 84-208 "Graphoepitaxy of Ge on SiO_2 by Solid-State Surface-Energy-Driven Grain Growth," T. Yonehara, Henry I. Smith, C. V. Thompson, and J. E. Palmer, October 1984. (11 pp.)
- 84-209 "Report on the Hardware Description Language Zeus," Karl J. Lieberherr, November 1984. (57 pp.)
- 84-210 "Heat Transfer Analysis for High Quality Liquid-Phase Recrystallization of Thin Silicon Films for Electronic Devices," Ioannis N. Miaoulis, November 1984. (135 pp.)
- 84-211 "A Circuit Grammar for Operational Amplifier Design," Andrew Lewis Ressler, November 1984. (92 pp.)
- 84-212 "Macromodeling of Digital MOS VLSI Circuits," Mark D. Matson, November 1984. (19 pp.)
- 84-213 "Optimization of Digital MOS VLSI Circuits," Mark D. Matson, November 1984. (16 pp.)
- 84-214 "A Design-by-Example Regular Structure Generator," Cyrus S. Bamji, Charles E. Hauck, and Jonathan Allen, November 1984. (14 pp.)
- 84-215 "Design of a CMOS Self-Timed Two by Two Packet Router," Tam-Anh Chu, November 1984. (13 pp.)
- 84-216 "A Mixed-Integer Linear Programming Problem Which is Efficiently Solvable," Charles E. Leiserson and James B. Saxe, December 1984. (11 pp.)
- 84-217 "Solid Phase Processes for Semiconductor-on-Insulator," Carl V. Thompson, December 1984. (9 pp.)
- 85-218 "The Systematic Exploration of Pipelined Array Multiplier Performance," Charles E. Hauck, Cyrus S. Bamji, and Jonathan Allen, January 1985. (4 pp.)
- 85-219 "Dispersion of Powders in Solutions of a Block Copolymer," H. D. Lee, R. L. Pober, and P. D. Calvert, January 1985. (15 pp.)

VLSI MEMO SERIES (continued)

- 85-220 "The Kinetics of Polysilicon Etching in Cl_2 Discharges," Herbert H. Sawin, Brian E. Thompson, and Albert D. Richards, January 1985. (12 pp.)
- 85-221 "Improved Bounds on Signal Delay in MOS Interconnect," John L. Wyatt, Jr., Qingjian Yu, Charles Zukowski, Han-Ngee Tan, and Peter O'Brien, January 1985. (5 pp.)
- 85-222 "Conversion of Silane Dissociation Reaction in a Mixed Flow Reactor of Silane Glow Discharge," S. Rhee and J. Szekely, January 1985. (13 pp.)
- 85-223 "A Simple Cost Model for Multilayer Integrated Circuits," A. L. Robinson, L. A. Glasser, and D. A. Antoniadis, January 1985. (32 pp.)
- 85-224 "Identification of Leakage Current Mechanisms in Thin Film Poly-Si SOI MOSFETs," Sudhir K. Madan and Dimitri A. Antoniadis, January 1985. (47 pp.)
- 85-225 "Finite Element Analysis of a Thermal-Capillary Model For Liquid Encapsulated Czochralski Growth," J. J. Derby, R. A. Brown, F. T. Geyling, A. S. Jordan, and G. A. Nikolakopoulou, February 1985. (48 pp.)
- 85-226 "Mass Transfer Analysis of Electrodeposition Through Polymeric Masks," Edward C. Hume III, William M. Deen, and Robert A. Brown, February 1985. (8 pp.)
- 85-227 "Mechanisms for Lateral Solute Segregation in Edge-Defined Film-Fed Crystal Growth," Hisham M. Ettouney and Robert A. Brown, February 1985. (8 pp.)
- 85-228 "Steady Solute Fields Induced by Differential Rotation in a Small Floating Zone," George M. Harriott and Robert A. Brown, February 1985. (16 pp.)
- 85-229 "Finite Element Analysis of Directional Solidification of Dilute and Concentrated Binary Alloys," Robert A. Brown, Chiechun J. Chang, and Peter M. Adornato, February 1985. (19 pp.)
- 85-230 "A Hardware Assisted Methodology for VLSI Design Rule Checking," Larry Dean Seiler, February 1985. (294 pp.)
- 85-231 "Macromodeling and Optimization of Digital MOS VLSI Circuits," Mark Douglas Matson, February 1985. (106 pp.)
- 85-232 "Low Temperature Silicon Epitaxy by Plasma Enhanced CVD," Rafael Reif, March 1985. (7 pp.)
- 85-233 "A Design by Example Regular Structure Generator," Cyrus S. Bamji, March 1985. (111 pp.)
- 85-234 "Generalized Planar Matching," Fran Berman, Tom Leighton, Peter W. Shor, and Larry Snyder, March 1985. (35 pp.)
- 85-235 "Embedding Graphs in Books: A Layout Problem with Applications to VLSI Design," Fan R. K. Chung, Frank Thomson Leighton, and Arnold L. Rosenberg, March 1985. (56 pp.)
- 85-236 "Graph Bisection Algorithms with Good Average Case Behavior," Thang Nguyen Bui, Soma Chaudhuri, F. Thomson Leighton, and Michael Sipser, March 1985. (25 pp.)
- 85-237 "How to Design Simulatable CMOS Integrated Circuits," William B. Ackerman, March 1985. (14 pp.)
- 85-238 "Bounding Techniques and Applications for VLSI Circuit Simulation," Charles A. Zukowski, John L. Wyatt, Jr., and Lance A. Glasser, March 1985. (9 pp.)
- 85-239 "A UV Write-Enabled PROM," Lance A. Glasser, March 1985. (5 pp.)
- 85-240 "The Design of a VLSI Self-timed Ring Buffer using Signal Transition Graphs," Tam-Anh Chu, March 1985. (23 pp.)
- 85-241 "Delay, Noise Margin, and Reliability in Digital Circuits," Lance A. Glasser, March 1985. (20 pp.)
- 85-242 "Communication Density Considerations in Multiprocessors," Lance A. Glasser and Charles A. Zukowski, April 1985. (10 pp.)
- 85-243 "Dynamic Production Scheduling in Computer-Aided Fabrication," Stanley B. Gershwin, April 1985. (3 pp.)
- 85-244 "A Review of Plasma Processing Fundamentals," Herbert H. Sawin, April 1985. (26 pp.)

VLSI MEMO SERIES (continued)

- 85-245 "Ultra-fine Grain Processing Architectures," Donald Scott Wills, May 1985. (84 pp.)
- 85-246 "Reactive-Ion Etching of Tungsten for Sub-50 Nanometer, High-Contrast X-Ray Mask Fabrication," Irving Plotnik, May 1985. (112 pp.)
- 85-247 "Comparison of Different Techniques for Passivation of Small Grain Polycrystalline-SI MOSFETs," M. Rodder and D. A. Antoniadis, June 1985. (14 pp.)
- 85-248 "Parametric Modeling of Plasma Etching Processes," Herbert H. Sawin, Kenneth D. Allen, Mary W. Jenkins, and Michael T. Mocella, June 1985. (33 pp.)
- 85-249 "Bounding Enhancements for VLSI Circuit Simulation," Charles Albert Zukowski, June 1985. (202 pp.)
- 85-250 "A Digital Gaussian Convolver for Visual Images," Andrew A. Berlin, June 1985. (40 pp.)
- 85-251 "Surface Gratings with Sub-100nm Linewidths," Erik Hyde Anderson, June 1985. (99 pp.)
- 85-252 "X-Ray Lithography for Sub 100-nm Channel Length Transistors Using Masks Fabricated with Conventional Photolithography, Anisotropic Etching and Oblique Shadowing," S. Y. Chou, H. I. Smith and D. A. Antoniadis, July 1985. (13 pp.)
- 85-253 "Surface Superlattices and Quasi-One-Dimensional Conduction in Silicon Inversion Layers," Alan Clark Warren, August 1985. (194 pp.)
- 85-254 "Plasma Enhanced Chemical Vapor Deposition for Microelectronics," Rafael Reif, August 1985. (14 pp.)
- 85-255 "Compensation of Grain Growth Enhancement in Doped Silicon Films," H.-J. Kim and C. V. Thompson, August 1985. (11 pp.)
- 85-256 "Ion Bombardment Energy Distributions in Radio Frequency Glow Discharge Systems," Brian E. Thompson, Kenneth D. Allen, Albert D. Richards, and Herbert H. Sawin, September 1985. (59 pp.)
- 85-257 "Step Response Bounds for Systems Described by M-Matrices, with Application to Timing Analysis of Digital MOS Circuits," J. L. Wyatt Jr., C. A. Zukowski, and P. Penfield, Jr., September 1985. (6 pp.)
- 85-258 "Comparison of Measured and Calculated SF₆ Breakdown in rf Electric Fields," Brian E. Thompson and Herbert H. Sawin, September 1985. (14 pp.)
- 85-259 "MASTIF - A Workstation Approach to Fabrication Process Design," Duane S. Boning and Dimitri A. Antoniadis, September 1985. (7 pp.)
- 85-260 "Randomized Routing on Fat-Trees," Ronald I. Greenberg and Charles E. Leiserson, September 1985. (9 pp.)
- 85-261 "The Plasma Etching of Polysilicon with CF₃CL/Argon Discharges: I. Parametric Modeling and Impedance Analysis," Kenneth D. Allen, Herbert H. Sawin, Michael T. Mocella, and Mary W. Jenkins, September 1985. (37 pp.)
- 85-262 "The Plasma Etching of Polysilicon with CF₃CL/Argon Discharges: II. Modeling of Ion Bombardment Energy Distributions," Kenneth D. Allen and Herbert H. Sawin, September 1985. (32 pp.)
- 85-263 "The Plasma Etching of Polysilicon with CF₃CL/Argon Discharges: III. Modeling of Etching Rate and Directionality," Kenneth D. Allen, Herbert H. Sawin, and Akimichi Yokozeki, September 1985. (40 pp.)
- 85-264 "Secondary Grain Growth in Ultrathin Films of Germanium on Silicon Dioxide," Joyce Ellen Palmer, September 1985. (147 pp.)
- 85-265 "The Characterization of Low-Temperature Silicon Epitaxy Deposited by Plasma Enhanced Chemical Vapor Deposition," Thomas Joseph Donahue, September 1985. (319 pp.)
- 85-266 "The Database Accelerator: Architecture," Richard Zippel, October 1985. (21 pp.)
- 85-267 "Compaction with Automatic Jog Introduction," F. Miller Maley, October 1985. (23 pp.)
- 85-268 "Interprocessor Communication Issues in Fat-Tree Architectures," Alexander Toichi Ishii, October 1985. (41 pp.)
- 85-269 "Computing Minimum Spanning Trees on a Fat-Tree Architecture," Bruce M. Maggs, October 1985. (37 pp.)

VLSI MEMO SERIES (continued)

- 85-270 "Space-Efficient Algorithms for Computational Geometry," Cynthia A. Phillips, October 1985. (34 pp.)
- 85-271 "Schema: An Architecture for Knowledge Based CAD," C. G. Clark and R. E. Zippel, October 1985. (3 pp.)
- 85-272 "Wafer-Scale Integration of Systolic Arrays," Frank Thomson Leighton and Charles E. Leiserson, October 1985. (29 pp.)
- 85-273 "The Focused Ion Beam as an Integrated Circuit Restructuring Tool," J. Melngailis, C. R. Musil, E. H. Stevens, M. Utlaut, E. M. Kellogg, R. T. Post, M. W. Geis, and R. W. Mountain, November 1985. (23 pp.)
- 85-274 "Synthesis of a Self-timed Controller for a Successive-approximation A/D Converter," Tam-Ahn Chu and Lance A. Glasser, November 1985. (14 pp.)
- 85-275 "Focused Ion Beam Technology," John Melngailis, November 1985. (13 pp.)
- 85-276 "Synchronizer Failure in A/D Converters," Lance A. Glasser, November 1985. (13 pp.)
- 85-277 "Secondary Grain Growth in Thin Films of Semiconductors: Theoretical Aspects," C. V. Thompson, November 1985. (9 pp.)
- 85-278 "Signal Delay in Leaky RC Mesh Models for Bipolar Interconnect," Peter O'Brien and John L. Wyatt, Jr., November 1985. (64 pp.)
- 85-279 "Electrical Characterization of Epitaxial Silicon Deposited at Low Temperatures by Plasma Enhanced Chemical Vapor Deposition," W. R. Burger and R. Reif, November 1985. (14 pp.)
- 85-280 "Polysilicon Etching in SF_6 rf Discharges: Characteristics and Diagnostic Measurements," Brian E. Thompson and Herbert H. Sawin, November 1985. (50 pp.)
- 85-281 "CMOS Design of a FDDI Serial Data Communication Circuit," Frank C. Park, November 1985. (80 pp.)
- 85-282 "An Automatic Programming Approach to Testing," Mark H. Shirley, November 1985. (21 pp.)
- 85-283 "A High-Speed Asynchronous Communication Technique for MOS Systems," Paul D. Bassett, December 1985. (104 pp.)
- 85-284 "American Microelectronics in Decline: Evidence, Analysis, and Alternatives," Charles H. Ferguson, December 1985. (143 pp.)
- 85-285 "A New Effective Field for Mobility Extraction in MOS Inversion Layers," L. J. Newell, P. Vande Voorde, S. Y. Oh, C. G. Sodini, J. L. Moll, December 1985. (12 pp.)
- 85-286 "Hot Carrier Effects in Hydrogen Passivated P-channel Polycrystalline-Si MOSFETs," M. Rodder and D. A. Antoniadis, December 1985. (11 pp.)
- 85-287 "Temperature Distribution of Silicon on Insulator (SOI) Systems During Recrystallization Processing," Ioannis N. Miaoulis and Bora B. Mikic, December 1985. (22 pp.)
- 85-288 "Heat Source Power Requirements for High Quality Recrystallization of Thin Silicon Films for Electronic Devices," Ioannis N. Miaoulis and Bora Mikic, December 1985. (24 pp.)
- 85-289 "Device Performance in Epitaxial Silicon Deposited at Low Temperatures by Plasma-Enhanced Chemical Vapor Deposition," W. R. Burger and R. Reif, December 1985. (11 pp.)
- 85-290 "Low-Temperature Silicon Epitaxy Deposited by Plasma Enhanced Chemical Vapor Deposition I. Kinetics," T. J. Donahue and R. Reif, December 1985. (40 pp.)
- 85-291 "Low-Temperature Silicon Epitaxy Deposited by Plasma Enhanced Chemical Vapor Deposition II. Autodoping," T. J. Donahue and R. Reif, December 1985. (31 pp.)
- 85-292 "Low-Temperature Silicon Epitaxy Deposited by Plasma Enhanced Chemical Vapor Deposition III. Pattern Transfer," T. J. Donahue and R. Reif, December 1985. (33 pp.)
- 85-293 "Submicron-Structures Research at M.I.T.," Henry I. Smith, December 1985. (14 pp.)

VLSI MEMO SERIES (continued)

- 85-294 "A Statistical Analysis of UV, X-Ray and Charged-Particle Lithographies," Henry I. Smith, December 1985. (23 pp.)
- 86-295 "Parallel Simulation of Digital LSI Circuits," Jeffrey M. Arnold, January 1986. (98 pp.)
- 86-296 "Signal Delay in ECL Interconnect," Peter R. O'Brien and John L. Wyatt, Jr., February 1986. (4 pp.)
- 86-297 "Time-Domain Perturbational Analysis of Nonuniformly Coupled Transmission Lines," Ying-Ching Eric Yang, Jin Au Kong, and Qizheng Gu, February 1986. (10 pp.)
- 86-298 "Transient Analysis of Single and Coupled Lines with Capacitively-Loaded Junctions," Qizheng Gu and Jin Au Kong, February 1986. (42 pp.)
- 86-299 "Transient Analysis of Strip Transmission Line Circuits with Perpendicularly Crossing Strips Geometry," Qizheng Gu, Jin Au Kong, and Ying-Ching Eric Yang, February 1986. (11 pp.)
- 86-300 "Design and Implementation of a GaAs 4-bit Arithmetic and Logic Unit," Wayne T. Chen, February 1986. (48 pp.)
- 86-301 "The Effect of Dopants on Grain Boundary Mobility in Silicon," H. -J. Kim and C. V. Thompson, February 1986. (8 pp.)
- 86-302 "Time Domain Analysis of Nonuniformly Coupled Lines," Qizheng Gu, Jin Au Kong, and Ying-Ching Eric Yang, February 1986. (4 pp.)
- 86-303 "Macromodeling and Optimization of Digital MOS VLSI Circuits," Mark D. Matson and Lance A. Glasser, March 1986. (41 pp.)
- 86-304 "Dynamic Production Scheduling in Computer-Aided Fabrication of Integrated Circuits," Christopher Lozinski and Stanley B. Gershwin, March 1986. (6 pp.)
- 86-305 "Object Flow for Facility Automation," Jeffrey B. Winner, March 1986. (101 pp.)
- 86-306 "Directional Plasma Etching of Polysilicon in $\text{SF}_6/\text{CFCl}_3$ Discharges," Michael T. Mocella, Brian E. Thompson, and Herbert H. Sawin, March 1986. (6 pp.)
- 86-307 "Monte Carlo Modeling of Ion Transport Through RF Glow Discharge Sheaths," Donald A. Fisher, Brian E. Thompson and Herbert H. Sawin, March 1986. (6 pp.)
- 86-308 "Concentration Measurements of Chlorine Atoms in a Plasma Reactor," Joda Wormhoudt, Alan C. Stanton, Albert D. Richards, and Herbert H. Sawin, March 1986. (6 pp.)
- 86-309 "Continuum Modeling of Charged Particle Transport: RF Breakdown and Discharges of SF_6 ," Brian E. Thompson, Herbert H. Sawin, and Aaron Owens, March 1986. (6 pp.)
- 86-310 "Graph Bisection Algorithms," Thang Nguyen Bui, April 1986. (72 pp.)
- 86-311 "Secondary Grain Growth and Graphoepitaxy in Thin Au Films," Chee Cheong Wong, April 1986. (283 pp.)
- 86-312 "New Upper Bounds for Two-Layer Channel Routing," Bonnie Anne Berger, May 1986. (66 pp.)
- 86-313 "Electronic Conduction in Ultra-Short Channel Si MOSFET's," Stephen Yu Chou, May 1986. (191 pp.)
- 86-314 "Stochastic Scheduling and Set-Ups in Flexible Manufacturing Systems," Stanley B. Gershwin, May 1986. (12 pp.)
- 86-315 "Investigation, Design Analysis of a High Performance CMOS Multiplier," Stephanie L. Scheidler, May 1986. (119 pp.)
- 86-316 "Compaction with Automatic Jog Introduction," F. Miller Maley, May 1986. (35 pp.)
- 86-317 "Improved Signal Delay Bounds for RC Tree Networks," David Standley and John L. Wyatt, Jr., May 1986. (32 pp.)
- 86-318 "Modeling of the Plasma Etching of Polysilicon with Chloro- and Bromo-Trifluoromethane Discharges," Kenneth Donald Allen, May 1986. (406 pp.)
- 86-319 "MACE: A Multiprocessing Approach to Circuit Extraction," Samuel M. Levitin, May 1986. (73 pp.)

VLSI MEMO SERIES (continued)

- 86-320 "Tight Bounds for Minimax Grid Matching, with Applications to the Average Case Analysis of Algorithms," Tom Leighton and Peter Shor, June 1986. (27 pp.)
- 86-321 "Logic Simulation using a Content-Addressable Memory System," Beng-Hong Lim, June 1986. (52 pp.)
- 86-322 "The Kinetics of Secondary Grain Growth in Rapidly Thermal Annealed Thin Silicon Films," Stephen Michael Garrison, June 1986. (66 pp.)
- 86-323 "The Coupled Depth/Slope Approach to Surface Reconstruction," John G. Harris, June 1986. (73 pp.)
- 86-324 "RELIC: A Reliability Simulator for Integrated Circuits," Teresa S. Hohol, June 1986. (66 pp.)
- 86-325 "MASTIF - A Workstation Approach to Integrated Circuit Process and Device Design," Duane S. Boning, June 1986. (39 pp.)
- 86-326 "Atomic Chlorine Concentration and Gas Temperature Measurements in a Plasma Etching Reactor," J. Wormhoudt, A. C. Stanton, A. D. Richards and H. H. Sawin, July 1986. (30 pp.)
- 86-327 "Methodology Verification of Hierarchically Described VLSI Circuits," Isaac L. Bain and Lance A. Glasser, June 1986. (16 pp.)
- 86-328 "MOS Hot Electron Resistance of Rapid Thermal Nitrided (RTN) and Reoxidized RTN Oxides," Patrice Parris, July 1986. (91 pp.)
- 86-329 "Annealing Experiments with MOS Structures," Corey Gee, July 1986. (37 pp.)
- 86-330 "Characterization of Errors in Circuit Simulation Programs," Andrew E. Stevens, July 1986. (57 pp.)
- 86-331 "Laser-Induced Chemical Vapor Deposition of Silicon Nitride Films: Film and Process Characterizations," E. T-S. Pan, J. H. Flint, D. Adler, and J. S. Haggerty, July 1986. (25 pp.)
- 86-332 "A Model for Gas-Laser Interaction: Application to Thermally-Activated Laser-Induced Chemical Vapor Deposition," E. T-S. Pan, J. H. Flint, J. M. Liang, D. Adler, and J. S. Haggerty, July 1986. (23 pp.)
- 86-333 "Laser-Induced Chemical Vapor Deposition of Silicon Nitride Films," Eric Ting-Shan Pan, July 1986. (61 pp.)
- 86-334 "Characterization and Modeling of Sulfur Hexafluoride Radio-Frequency Glow-Discharges for Etching Polysilicon," Brian Eric Thompson, July 1986. (33 pp.)
- 86-335 "Characterization and Modeling of Polysilicon Etching in a Chlorine Plasma," Albert Davidson Richards, July 1986. (35 pp.)
- 86-336 "Continuum Modeling of Argon Radio-Frequency Glow Discharges," Albert D. Richards, Brian E. Thompson, and Herbert H. Sawin, September 1986. (15 pp.)
- 86-337 "Atomic Chlorine Concentration Measurements in a Plasma Etching Reactor: I. A Comparison of Infrared Absorption and Optical Emission Actinometry," Albert D. Richards, Brian E. Thompson, Kenneth D. Allen, and Herbert H. Sawin, September 1986. (35 pp.)
- 86-338 "Atomic Chlorine Concentration Measurements in a Plasma Etching Reactor: II. A Simple Predictive Model," Albert D. Richards, and Herbert H. Sawin, September 1986. (41 pp.)
- 86-339 "Ion-Implant Compensation of Tensile Stress in Tungsten Absorber for Low Distortion X-Ray Masks," I. Plotnik, M. E. Porter, M. Toth, S. Akhtar, and Henry I. Smith, October 1986. (9 pp.)
- 86-340 "MOS Electrical Characteristics of Low Pressure Re-Oxidized Nitrided-Oxide," R. Jayaraman, W. Yang, and C. G. Sodini, October 1986. (5 pp.)
- 86-341 "Recent Results in VLSI CAD at MIT," R. E. Zippel, P. Penfield, Jr., L. A. Glasser, C. E. Leiserson, J. L. Wyatt, Jr., F. T. Leighton, and J. Allen, October 1986. (8 pp.)
- 86-342 "Characterization of Argon Ion Bombardment as a Surface Cleaning Technique for Silicon Epitaxial Deposition at Low Temperatures and Very Low Pressures," L. M. Garverick, J. H. Comfort, W. R. Burger, R. Reif, F. Baiocchi, and H. Luftman, October 1986. (12 pp.)

VLSI MEMO SERIES (continued)

- 86-343 "Cryptography and VLSI (a two-part dissertation): I. Detecting and Exploiting Algebraic Weaknesses in Cryptosystems II. Algorithms for Placing Modules on a Custom VLSI Chip," Alan Theodore Sherman, October 1986. (220 pp.)
- 86-344 "A High-Performance VLSI Quaternary Serial Multiplier," William J. Dally, October 1986. (6 pp.)
- 86-345 "Wire-Efficient VLSI Multiprocessor Communication Networks," William J. Dally, October 1986. (19 pp.)
- 86-346 "Lazy Event-Driven Simulation," William J. Dally, October 1986. (6 pp.)
- 86-347 "The Semiconductor Industry in the American Economy: Economic Analysis and Implications," Charles Ferguson, November 1986. (12 pp.)
- 86-348 "Frequency Limitations in Circuits Composed of Linear Devices," Lance A. Glasser, November 1986. (24 pp.)
- 86-349 "Communication-Efficient Parallel Graph Algorithms," Bruce MacDowell Maggs, December 1986. (33 pp.)
- 86-350 "A Survey of Problems and Results for Channel Routing," Tom Leighton, December 1986. (9 pp.)
- 86-351 "Nearly Optimal Algorithms and Bounds for Multilayer Channel Routing," Bonnie Berger, Martin Brady, Donna Brown, and Tom Leighton, December 1986. (20 pp.)
- 86-352 "A Hyperconcentrator Switch for Routing Bit-Serial Messages," Thomas H. Cormen and Charles E. Leiserson, December 1986. (8 pp.)
- 86-353 "A New Approach to the Maximum Flow Problem," Andrew V. Goldberg and Robert E. Tarjan, December 1986. (11 pp.)
- 86-354 "Optimal Simulations of Tree Machines," Sandeep Bhatt, Fan Chung, Tom Leighton, and Arnold Rosenberg, December 1986. (9 pp.)
- 86-355 "Parallel ($\Delta + 1$) Coloring of Constant-Degree Graphs," Andrew V. Goldberg and Serge A. Plotkin, December 1986. (7 pp.)
- 86-356 "A Proposal for Profile Interchange Format; Part I: Syntax; Part II: Semantics," Duane S. Boning and Thye-Lai Tung, December 1986. (32 pp.)
- 86-357 "Focused Ion Beam Induced Deposition of Gold," G. M. Shedd, H. Lezec, A. D. Dubner, and J. Melngailis, December 1986. (14 pp.)
- 87-358 "Focused Ion Beam Assisted Deposition of Gold," G. M. Shedd, January 1987. (76 pp.)
- 87-359 "Phase-locked Semiconductor Quantum Well Laser Arrays," Elias Towe, January 1987. (189 pp.)
- 87-360 "RELIC: A Reliability Simulator for Integrated Circuits," Teresa S. Hohol and Lance A. Glasser, January 1987. (7 pp.)
- 87-361 "Focused Ion Beam Technology and Applications," John Melngailis, January 1987. (69 pp.)
- 87-362 "Bipolar Transistor Fabrication in Low-Temperature (745° C) Ultra-Low Pressure Chemical Vapor Deposited Epitaxial Silicon," W. R. Burger, J. H. Comfort, L. M. Garverick, T. R. Yew, and R. Reif, January 1987. (10 pp.)
- 87-363 "BICMOS Circuit Design Techniques: An Overview," H.-S. Lee and C. G. Sodini, January 1987. (2 pp.)
- 87-364 "Low Pressure Nitrided Oxide in MOS Capacitors," Woodward Yang, January 1987. (80 pp.)
- 87-365 "I. Device Design Requirements for MOS Analog Circuits; II. Device Design Requirements for MOS Dynamic Logic Circuits," C. G. Sodini, P. K. Ko, and S. S. Wong, March 1987. (4 pp.)
- 87-366 "The Competitive Decline of the U.S. Semiconductor Industry," Charles H. Ferguson, March 1987. (9 pp.)
- 87-367 "Bulk-Quality Bipolar Transistors Fabricated in Low-Temperature ($T_{dep} = 800^\circ$ C) Epitaxial Silicon," W. R. Burger and R. Reif, March 1987. (13 pp.)

VLSI MEMO SERIES (continued)

- 87-368 "Scheduling Job Shops with Delays," Sheldon X. C. Lou, Garrett Van Ryzin, and Stanley B. Gershwin, March 1987. (5 pp.)
- 87-369 "A Viscoelastic Beam for Modeling Oxidation," Thye-Lai Tung, Jerome Connor, and Dimitri A. Antoniadis, March 1987. (8 pp.)
- 87-370 "Dynamic Scheduling and Routing for Flexible Manufacturing Systems That Have Unreliable Machines," Oded Z. Maimon and Stanley B. Gershwin, March 1987. (8 pp.)
- 87-371 "Nonlinear Dynamic Maximum Power Theorem," John L. Wyatt, Jr., March 1987. (18 pp.)
- 87-372 "Efficient Multichip Partial Concentrator Switches," Thomas H. Cormen, April 1987. (10 pp.)
- 87-373 "Efficient Parallel Algorithms for $(\Delta + 1)$ -Coloring and Maximal Independent Set Problems," Andrew V. Goldberg and Serge A. Plotkin, May 1987. (24 pp.)
- 87-374 "Silicon Surface Cleaning by Low Dose Argon Ion Bombardment for Low Temperature (750° C) Epitaxial Silicon Deposition. Part I: Process Considerations; Part II: Epitaxial Quality," James H. Comfort, Linda M. Garverick, and Rafael Reif, April 1987. (158 pp.)
- 87-375 "Speed, Power, and Resolution Limitations in Cyclic and Pipelined Analog-to-Digital Converters," Hae-Seung Lee, April 1987. (21 pp.)
- 87-376 "Kinetic Modeling of Grain Growth in Polycrystalline Silicon Films Doped with Phosphorus or Boron," H.-J. Kim and C. V. Thompson, May 1987. (37 pp.)
- 87-377 "In-Situ Doping for Low Temperature Silicon Epitaxy by PECVD," James H. Comfort and Rafael Reif, May 1987. (10 pp.)
- 87-378 "Efficient Graph Algorithms for Sequential and Parallel Computers," Andrew Vladislav Goldberg, May 1987. (123 pp.)
- 87-379 "A Magnetic Communication Scheme for Integrated Circuits," Charles William Selvidge, May 1987. (104 pp.)
- 87-380 "KOH:H₂O Etching of (110)Si, (111)Si, SiO₂, and Ta: An Experimental Study," Lloyd D. Clark and David J. Edell, May 1987. (8 pp.)
- 87-381 "The Practical Engineer's No-Nonense Guide to On-Chip Signal Delay Calculations," John L. Wyatt, Jr., May 1987. (36 pp.)
- 87-382 "An Optimized In-Situ Argon Sputter Clean For Device Quality Low Temperature ($T \leq 800^\circ \text{C}$) Epitaxial Silicon: Bipolar Transistor and PN Junction Characterization," W. R. Burger and R. Reif, May 1987. (44 pp.)
- 87-383 "Characterization of Silicon Epitaxy Deposited by Plasma-Enhanced Chemical Vapor Deposition at Low Temperatures and Very Low Pressures," Linda Mason Garverick, May 1987. (187 pp.)
- 87-384 "Macromodeling CMOS Circuits for Timing Simulation," Lynne Michelle Brocco, June 1987. (94 pp.)
- 87-385 "A Model for Comparing Process Latitude in UV, Deep-UV and X-Ray Lithography," Henry I. Smith, June 1987. (20 pp.)
- 87-386 "Use of a π -Phase-Shifting X-Ray Mask to Increase the Intensity Slope at Feature Edges," Y.-C. Ku, Erik H. Anderson, Mark L. Schattenburg, and Henry I. Smith, June 1987. (19 pp.)
- 87-387 "Ion Beam Enhanced Grain Growth in Thin Films," Harry Albert Atwater, Jr., June 1987. (224 pp.)
- 87-388 "Monte Carlo Simulation of Ion Transport through RF Glow-Discharge Sheaths," Brian E. Thompson, Herbert H. Sawin, and Donald A. Fisher, July 1987. (52 pp.)
- 87-389 "Optimization of Low-Pressure Nitridation/Reoxidation of SiO₂ for Scaled MOS Devices," W. Yang, R. Jayaraman, and C. G. Sodini, July 1987. (49 pp.)
- 87-390 "A Low-Temperature ($T_{\text{dep}} < 800^\circ \text{C}$) Epitaxial Silicon Process for the Fabrication of Bulk Quality Bipolar Transistors," W. R. Burger and R. Reif, July 1987. (4 pp.)

VLSI MEMO SERIES (continued)

- 87-391 "Characterization of n^+ Polysilicon Etching in CCL_4/He Discharges," Evangelos Gogolides, July 1987. (127 pp.)
- 87-392 "Electrical Quality of Low-Temperature ($T_{\text{dep}} \leq 800^\circ \text{C}$) Epitaxial Silicon: The Effect of Deposition Temperature," W. R. Burger and R. Reif, July 1987. (46 pp.)
- 87-393 "Quantum Conductance Fluctuations in Extremely Narrow Inversion Layers in Silicon," Jerome Carl Licini, July 1987. (89 pp.)
- 87-394 "Focused Ion Beam Induced Deposition," J. Melngailis, A. D. Dubner, J. S. Ro, G. M. Shedd, H. Leczec, and C. V. Thompson, July 1987. (9 pp.)
- 87-395 "Modeling the Effects of Si/SiO₂ Interface Proximity and Transverse Field on Carrier Mobility in MOSFETs," Jarvis Benjamin Jacobs, July 1987. (45 pp.)
- 87-396 "Radiation Effects in Low-Pressure Reoxidized Nitrided Oxide MOS Gate Dielectrics," G. J. Dunn, R. Jayaraman, W. Yang, and C. G. Sodini, July 1987. (13 pp.)
- 87-397 "A Boundary Element Method for Modeling Viscoelastic Flow in Thermal Oxidation," Thye-Lai Tung, Jerome Connor, and Dimitri A. Antoniadis, July 1987. (21 pp.)
- 87-398 "A Low-Temperature ($T < 800^\circ \text{C}$) Chemical Vapor Deposition Technique for the Deposition of Device Quality Epitaxial Silicon," Wayne Robert Burger, July 1987. (244 pp.)
- 87-399 "Characterization of a 'Solid State' Polyaniline-Based Transistor: Water Vapor-Dependent Characteristics of a Device Employing a Polyvinylalcohol/Phosphoric Acid Solid State Electrolyte," Shuchi Chao and Mark S. Wrighton, July 1987. (28 pp.)
- 87-400 "Preparation and Characterization of Molecule-Based Transistors with a 50 Nanometer Source-Drain Separation using Shadow Deposition Techniques: Towards Faster, More Sensitive Molecule-based Devices," E. Tracy Turner Jones, Oliver M. Chyan, and Mark S. Wrighton, July 1987. (11 pp.)
- 87-401 "Amplification of Electrical Signals with Molecule-based Transistors: Power Amplification up to a Kilohertz Frequency and Factors Limiting Higher Frequency Operation," Elizabeth Paul Lofton, James W. Thackeray, and Mark S. Wrighton, September 1987. (4 pp.)
- 87-402 "A Titanium Disilicide/ n^+ -Polysilicon Gate Electrode for Existing VLSI MOS Processes," Curtis Tsai, September 1987. (64 pp.)
- 87-403 "Microelectrochemical Transistors Based on Electrostatic Binding of Electroactive Metal Complexes in Protonated Poly(4-Vinylpyridine): Devices that Respond to Two Chemical Stimuli," Daniel Belanger and Mark S. Wrighton, September 1987. (7 pp.)
- 87-404 "Chemically Responsive Microelectrochemical Devices Based on Platinized Poly(3-Methylthiophene): Variation in Conductivity with Variation in Hydrogen, Oxygen, or PH in Aqueous Solution," James W. Thackeray and Mark S. Wrighton, September 1987. (6 pp.)
- 87-405 "Process Model Testing and Optimization Using Matrix Experimentation," Emanuel Sachs and George Prueger, September 1987. (13 pp.)
- 87-406 "A Hierarchical Framework for Discrete Event Scheduling in Manufacturing Systems," Stanley B. Gershwin, September 1987. (22 pp.)
- 87-407 "Solid State Microelectrochemistry: Electrical Characteristics of a Solid State Microelectrochemical Transistor Based on Poly(3-Methylthiophene)," Shuchi Chao and Mark S. Wrighton, September 1987. (3 pp.)
- 87-408 "Fabrication and Characterization of Hydrogen Passivated Thin Film Polychrystalline-Silicon MOSFETS," Mark Stephen Rodder, September 1987. (203 pp.)
- 87-409 "A Hierarchical Framework for Manufacturing Systems Scheduling: A Two Machine Example," Stanley B. Gershwin, September 1987. (7 pp.)
- 87-410 "Synthesis of Self-timed VLSI Circuits from Graph-Theoretic Specifications," Tam-Anh Chu, July 1987. (189 pp.)

VLSI MEMO SERIES (continued)

- 87-411 "A Magnetic Power and Communications Interface for Pinless Integrated Circuits," Adam Craig Malamy, September 1987. (69 pp.)
- 87-412 "PATH: A Simulation-Based Transistor Sizer," Jae K. Kim, September 1987. (56 pp.)
- 87-413 "3-D IC Technology: An Overview Based on the Japanese R and D Movement," Brian Eidson, September 1987. (28 pp.)
- 87-414 "The Effects of Oxide Traps on the Large-Signal Transient Response of MOS Circuits," T. L. Tewksbury, H.-S. Lee and G. A. Miller, October 1987. (21 pp.)
- 87-415 "Frequency Limitations in Circuits Composed of Linear Devices," Lance A. Glasser, October 1987. (27 pp.)
- 87-416 "Characterization of Nonidealities in Integrated Circuit Transistors and Capacitors," Theodore L. Tewksbury, October 1987. (143 pp.)
- 87-417 "Deadlock-Free Message Routing in Multiprocessor Interconnection Networks," William J. Dally and Charles L. Seitz, November 1987. (7 pp.)
- 87-418 "A High Performance VLSI Quaternary Serial Multiplier," William J. Dally, November 1987. (5 pp.)
- 87-419 "Architecture and Design of the MARS Hardware Accelerator," P. Agrawal, W.J. Dally, A.K. Ezzat, W.C. Fischer, H.V. Jagadish, and A.S. Krishnakumar, November 1987. (7 pp.)
- 87-420 "Architecture of a Message-Driven Processor," W.J. Dally, L. Chao, A. Chien, S. Hassoun, W. Horwat, J. Kaplan, P. Song, B. Totty and S. Wills, November 1987. (8 pp.)
- 87-421 "A Fine-Grain, Message-Passing Processing Node," William J. Dally, November 1987. (15 pp.)
- 87-422 "Concurrent Computer Architecture," William J. Dally, November 1987. (28 pp.)
- 87-423 "Design of a Self-Timed VLSI Multicomputer Communication Controller," William J. Dally and Paul Song, November 1987. (5 pp.)
- 87-424 "Performance Analysis of K-Ary N-Cube Interconnection Networks," William J. Dally, November 1987. (26 pp.)
- 87-425 "Formal Hierarchical Multilevel Verification of Synchronous MOS VLSI Designs," Daniel Wayne Weise, November 1987. (172 pp.)
- 87-426 "Space-Efficient Queue Management Using Fixed-Connection Networks," Tom Leighton and Eric Schwabe, November 1987. (10 pp.)
- 87-427 "Optimal Simulations by Butterfly Networks: Extended Abstract," Sandeep N. Bhatt, Fan R. K. Chung, Jia-Wei Hong, F. Thomas Leighton and Arnold Rosenberg, November 1987. (11 pp.)
- 87-428 "A Graph With E Edges Has Pagenumber $O(\sqrt{E \log E})$," Seth M. Malitz, November 1987. (8 pp.)