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TECHNICAL REPORT RD-AS-88-8

POWER UP MODIFICATION FOR VIDEO SWITCHER
MICROPROCESSOR INTERFACE FOR SENSOR SYSTEM
PROCESSING SYSTEM

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19. ABSTRACT (Continue on reverse if necessary and identify by block number) This report describes the Power-up Modification of the Video Switch Interface of the SSPS Lab. The Video Switcher Microprocessor Interface is used to interface between the SSPS VAX 11/785 and the Video Switcher. The modifications made are (1) creating a power-up circuit that resets the microprocessor, (2) changing the chip selects from the start-up program, and (3) programming the EPROM to run the start-up program and user interface program.					
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I. INTRODUCTION

The video switcher microprocessor interface is used in support of autonomous acquisition and processors for the sensor system processing system. The original interface configuration, consisting of the Motorola 6800 and support devices, experienced numerous failures attributable to power loss, power glitches and erroneous data which required the microprocessor system to be manually rebooted after each failure. There was evident need for a circuit that automatically rebooted the microprocessor interface that was used between the SSPS VAX 11/785 and the video switcher.

II. MODIFICATION

The reset modification for the Motorola 6800 microprocessor interface consisted of basically of three steps, (1) designing of a reset circuit, (2) changing the chip selects, and (3) modification of existing programs.

A. Power Up Circuit

Due to the randomness of power glitches and bad data, a simple circuit was designed that would reset the microprocessor continuously with a predetermined amount of time (4 minutes) between each reset and have a manual switch that could reset the microprocessor, if desired, when a failure occurred between resets. The reset circuit consists of an astable (NE 555), a monostable (74LS123), and a manual reset switch as shown in the figure. The astable produces a 4 minute digital cycle which stays high for 2 minutes and low for 2 minutes. The output from the astable is connected to the A input (see figure) of the monostable which creates a pulse of 12 msec. The inverted output of the monostable is connected to reset on the microprocessor. The microprocessor resets on low and starts running on the rising edge of the inverted pulse.

For this circuit, the pulse generated by the monostable is created two ways, one for the automatic reset and one for the manual reset switch. In the automatic circuit, the monostable requires a falling edge on input A to send out a pulse. Therefore, the monostable will send out a pulse on the falling edge of the astable cycle. In the manual circuit, the monostable requires that input A be low and a rising edge on the clear input. When the reset switch is depressed, the astable and monostable are reset. The reset causes the astable's output to go low and stay low until the next change of state two minutes later. On the release of the switch the clear input on the monostable goes high resulting in a rising edge. Since the output from the astable is connected to input A of the monostable and clear on the monostable is rising, a pulse is sent out.

B. Chip Selects

Changing the chip selects from the microprocessor's ROM startup program to an EPROM startup program was accomplished by wiring the chip select of the ROM to the chip select of the EPROM and removing the ROM.

C. Modification of Programs

Programming the EPROM with a startup program that would initialize the microprocessor devices and run the existing user interface program was accomplished by modifying the existing startup and user program, Data Table 1, and loading both into the EPROM.

III. DISCUSSION

The Motorola 6800 microprocessor, whenever reset, receives a restart interrupt and outputs the addresses \$FFFE and \$FFFF in order to bring in the starting address of the restart routine. Due to internal address mapping, these addresses exist in the top two locations of the JBUG ROM (\$E3FE and \$E3FF) and respond with the address \$E08D. Since the JBUG ROM is the startup ROM and will be removed, this address had to be loaded in the top addresses of the EPROM.

NOTE

The EPROM used was the MC68708.

The restart routine at \$E08D of the JBUG ROM was loaded and then a jump was inserted after the restart routine to proceed to the interface program. Subroutines used by the interface program were loaded and all addresses pointing to the old EPROM location (CXXX) had to be changed to the ROM addresses (EXXX) where the new EPROM is located. Also, some minor debugging had to be performed due to the new setup. Data Table 2 shows the EPROM user program written by Richard Sims. The modifications that were made to this user program are highlighted in bold and underlined. The EPROM startup program and other related data are shown in Data Table 1.

Further information regarding this program may be obtained by referring to the MEK6800D2 Evaluation Kit II Manual, Appendix 1.

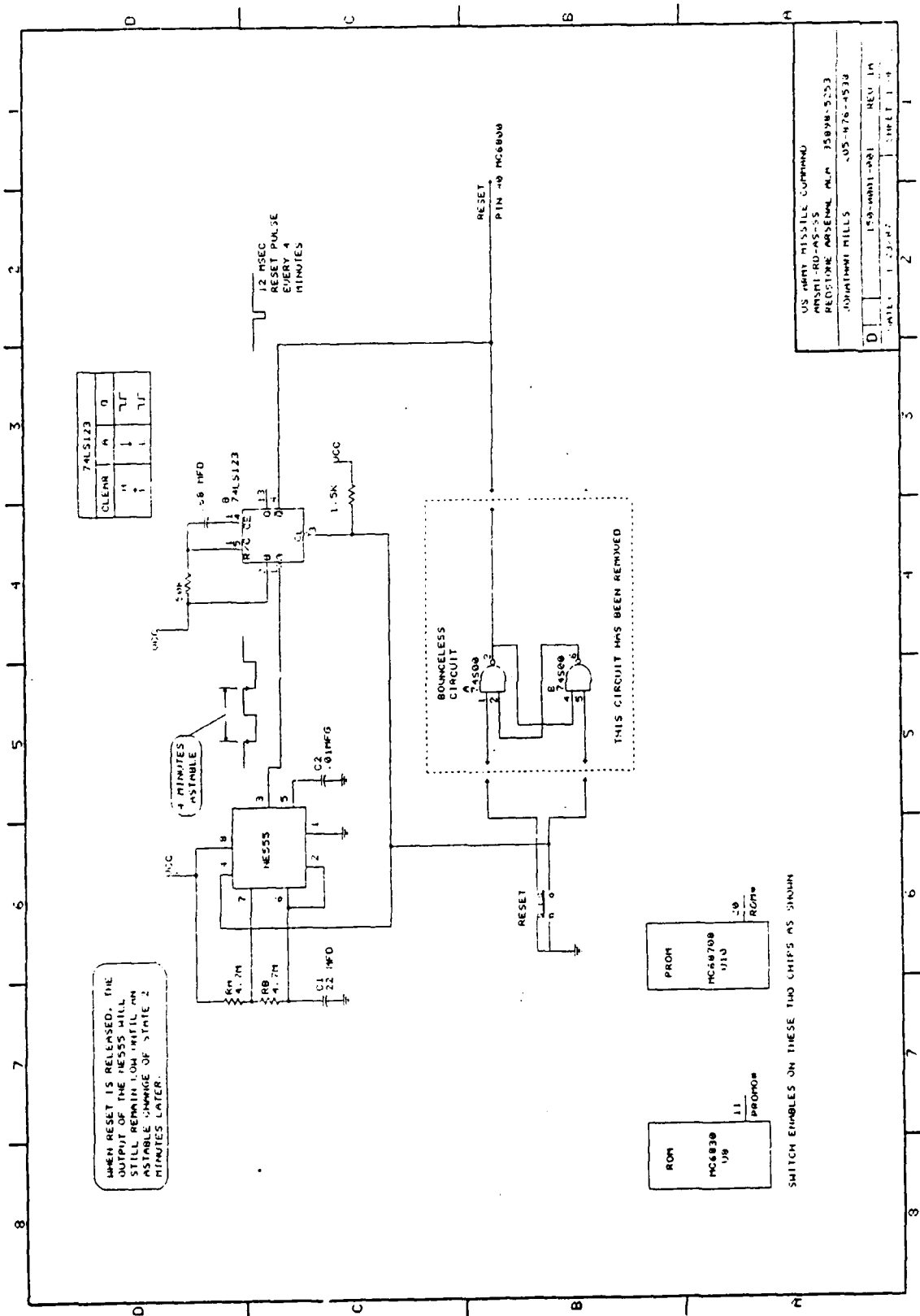


Figure. Power-up circuit.

DATA TABLE 1

ADDRESS	DATA	COMMAND	DESCRIPTION
084	86	LDAA	INTR MASKED CA1 ACTIVE LOW
085	3C		
086	B7	STAA	INTR MASKED CB1 ACTIVE LOW
087	80		
088	21		
089	B7	STAA	
08A	80		
08B	23		
08C	39	RTS	
08D	8E	LDS	
08E	A0		
08F	78		
090	BF	STS	INITIALIZE STACK POINTER
091	A0		
092	08		
093	CE	LDX	GO TO RESTART ROUTINE
094	<u>EO</u>		
095	<u>8D</u>		
096	FF	STX	INITIALIZE NMI INTERRUPT
097	A0		
098	06		
099	86	LDAA	
09A	FF		
09B	B7	STAA	PB0-PB7 OUTPUTS
09C	80		
09D	22		
09E	44	LSRA	
09F	B7	STAA	PA0-PA6 OUTPUTS, PA7 INPUT
0A0	80		
0A1	20		
0A2	8D	BSR	DISABLE KEYBOARD/TRACE
0A3	EO		
0A4	86	LDAA	
0A5	03		
0A6	B7	STAA	RESET THE ACIA
0A7	80		
0A8	08		
0A9	7F	CLR	INITIALIZE VFLAG
0AA	A0		
0AB	1D		
0AC	8D	BSR	CLEAR DISPLAY AND FLAGS
0AD	04		
0AE	<u>7E</u>	JMP	GOTO USER PROGRAM
0AF	<u>EO</u>		
0B0	<u>00</u>		
0B2	CE	LDX	
0B3	A0		
0B4	14		

DATA TABLE 1 (Cont'd)

ADDRESS	DATA	COMMAND	DESCRIPTION
OB5	4F	CLRA	CLEARs DIGIN4 AND DIGIN8
OB6	A7	STAA	CLEARs MFLAG AND RFLAG
OB7	00		
OB8	08	INX	CLEARs NFLAG AND TEMP2
OB9	8C	CPX	END?
OBA	A0		
OBb	1A		
OBC	26	BNE	NO LOOP BACK
OBd	F8		
OBf	CE	LDX	
OC0	A0		
OC1	0C		
OC2	FF	STX	INITIALIZE XKEYBF
OC3	A0		
OC4	1A		
OC5	86	LDAA	
OC6	7F		
OC7	B7	STAA	BLANK DISPLAY
OC8	80		
OC9	20		
OCA	86	LDAA	
Ocb	11		
OCC	CE	LDX	
OCd	A0		
OCe	0C		
OCf	A7	STAA	CLEAR OUT DISPLAY BUFFER
OD0	00		
OD1	08	INX	
OD2	8C	CPX	END?
OD3	A0		
OD4	14		
OD5	26	BNE	
OD6	F8		
OD7	39	RTS	
ODd	CE	LDX	START OFF A DELAY PROGRAM
ODE	06		
ODf	00		
OE0	09	DEX	
OE1	26	BNE	
OE2	FD		
OE3	39	RTS	
3FE	E0		RESTART INTERRUPT VECTOR
3FF	8D		

DATA TABLE 2

ADDRESS	DATA	COMMAND	DESCRIPTION
000	86	LDAA	
001	00		
002	B7	STAA	
003	80		
004	04		
005	86	LDAA	
006	38		
007	B7	STAA	
008	80		
009	05		
00A	86	LDAA	
00B	03		
00C	B7	STAA	
00D	80		
00E	08		
00F	86	LDAA	
010	1D		
011	B7	STAA	
012	80		
013	08		
014	B6	LDAA	LOAD ACIA STATUS
015	80		
016	08		
017	84	ANDA	MASK STATUS BIT
018	01		
019	27	BEG	GO BACK IF NO DATA
01A	F9		
01B	86	LDAA	
01C	FF		
01D	B7	STAA	SET PRA TO ALL OUTPUTS
01E	80		
01F	04		
020	B7	STAA	SET PRB TO ALL OUTPUTS
021	80		
022	06		
023	86	LDAA	CA2 STILL HIGH
024	3C		
025	B7	STAA	CRA NOW LOOKING AT PRA
026	80		
027	05		
028	86	LDAA	CRB DOES NOT COUNT
029	04		
02A	B7	STAA	CRB NOW LOOKING AT PRB
02B	80		
02C	07		
02D	B6	LDAA	ACIA DATA REGISTER
02E	80		
02F	09		

DATA TABLE 2 (Cont'd)

ADDRESS	DATA	COMMAND	DESCRIPTION
030	B7	STAA	PUT DATA ON PRA
031	80		
032	04		
033	B6	LDAA	LOAD ACIA STATUS
034	80		
035	08		
036	84	ANDA	CHECK DATA
037	01		
038	27	BEG	
039	F9		
03A	B6	LDAA	ACIA DATA REGISTER
03B	80		
03C	09		
03D	B7	STAA	PUT DATA ON PRB
03E	80		
03F	06		
040	86	LDAA	
041	30		
042	B7	STAA	CA2 LOW STROBE
043	80		
044	05		
045	CE	LDX	
046	06		
047	00		
048	<u>BD</u>	<u>JSR</u>	JUMP TO DELAY SUBROUTINE
049	E0		
04A	E0		
04B	86	LDAA	
04C	38		
04D	B7	STAA	
04E	80		
04F	05		
050	86	LDAA	
051	00		
052	B7	STAA	
053	80		
054	04		
055	7E	JMP	GO BACK AND LOOK FOR MORE DATA
056	<u>E0</u>		
057	14		

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