WRDC-TR-89-2040

TURBINE BLADE DATA ACQUISITION SYSTEM TECHNICAL REFERENCE

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This technical report has been reviewed and is approved for publication.

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19 ABSTRACT (Continue on reverse if necessary and identify by block number)

→ This report contains design and technical documentation on the non-contacting stress measurement system. This system is used as an analytical tool for s' ctural testing and research on bladed-disk components. This report shows artwork, schematics and block diagrams plus parts list. Keywords

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This report provides design and technical documentation on the Turbine Blade Data Acquisition System developed by the Electronic and Computer Development Laboratory, within the University of Dayton Research Institute. It was designed and fabricated as an analytical tool for structural testing and research on turbine components as part of the Noncontacting Stress Measurement System. This research effort was performed for the Aerospace Mechanics Group of the Research Institute. Michael Drake was the Principal Investigator and Robert Dominic was the Research Engineer in charge of daily activities for this project.

E&CD Lab personnel who contributed to this research and development effort were:

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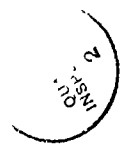
Documentation	Michael Gutman Steve Fuchs
Report Assembly	Sam Pietrantonio



FIGURES

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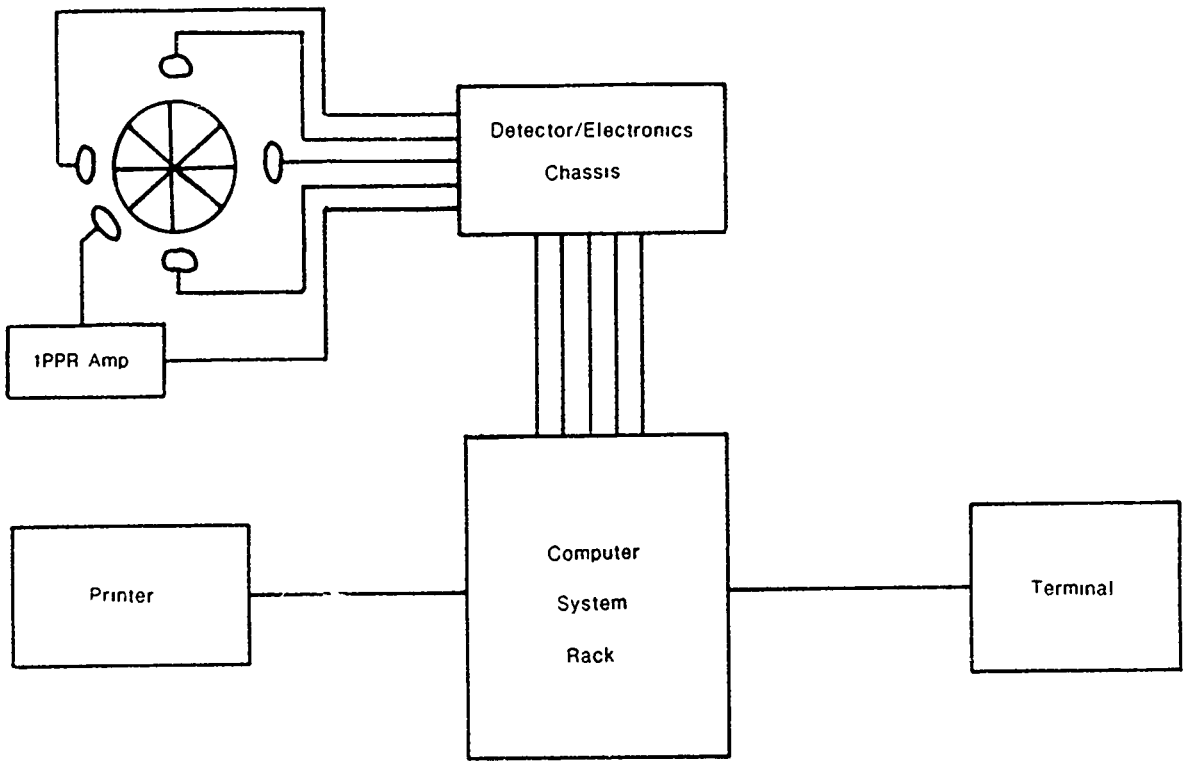


TITLE: TBDAS BLOCK DIAGRAM				FILENAME: BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
				FILEDATE: 07-Jul-1989	
FIGURE: 1	SHEET 1 OF 1	DESIGNER: ECD	DRAWN BY: MJG	FILETIME: 07 49 06	

Figure 1: TBDAS Block Diagram

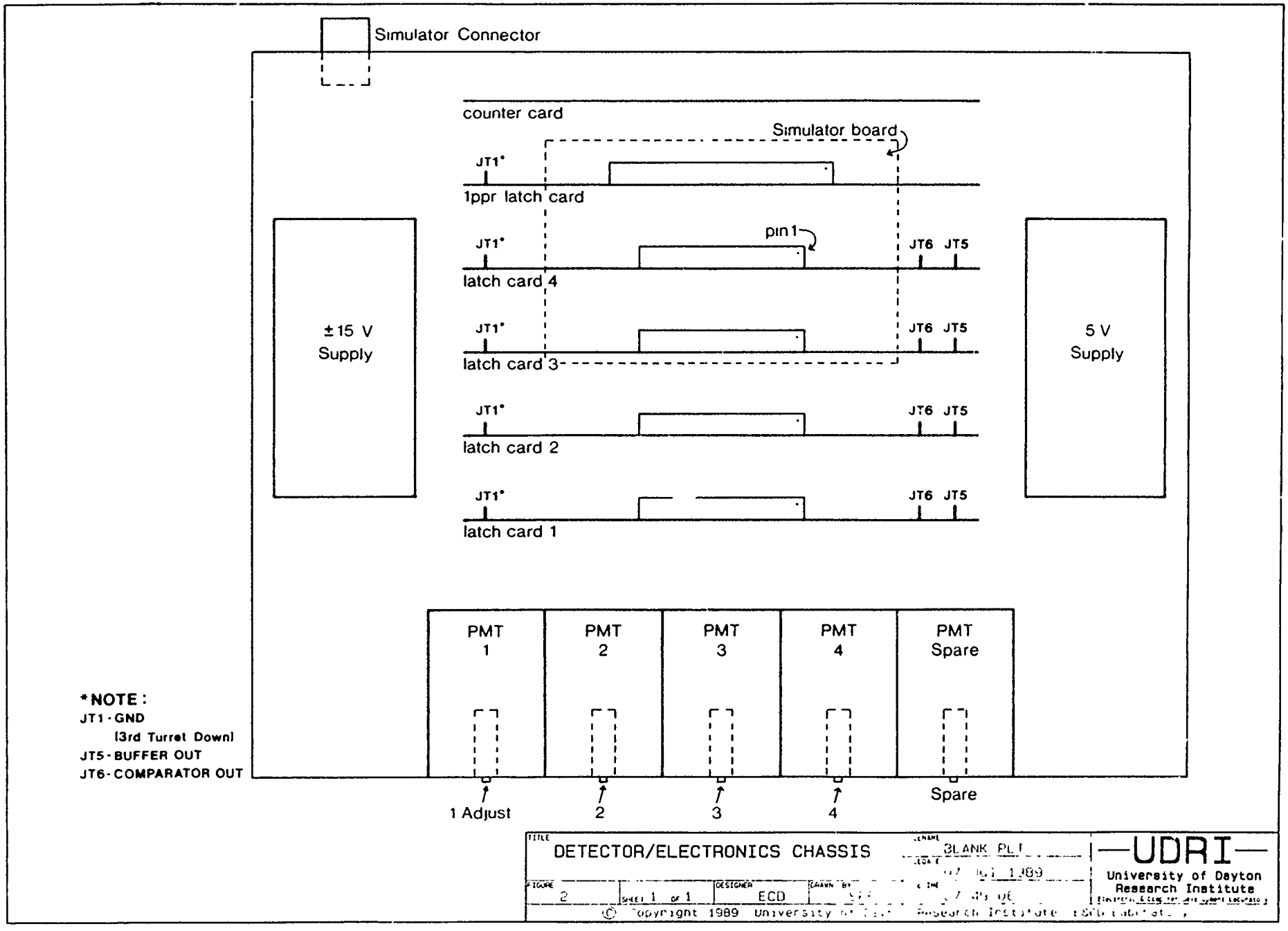


Figure 2: Detector/Electronics Chassis

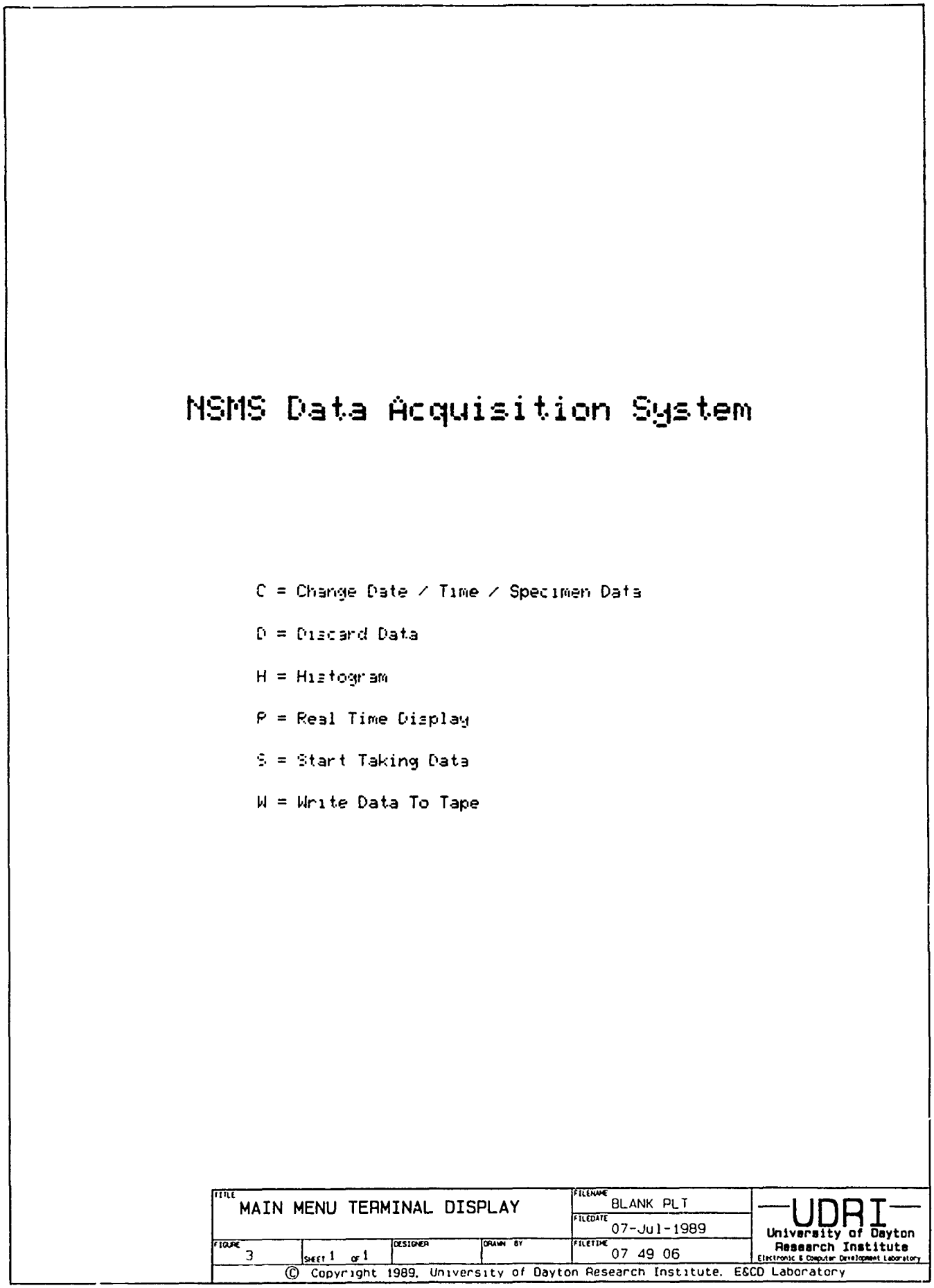
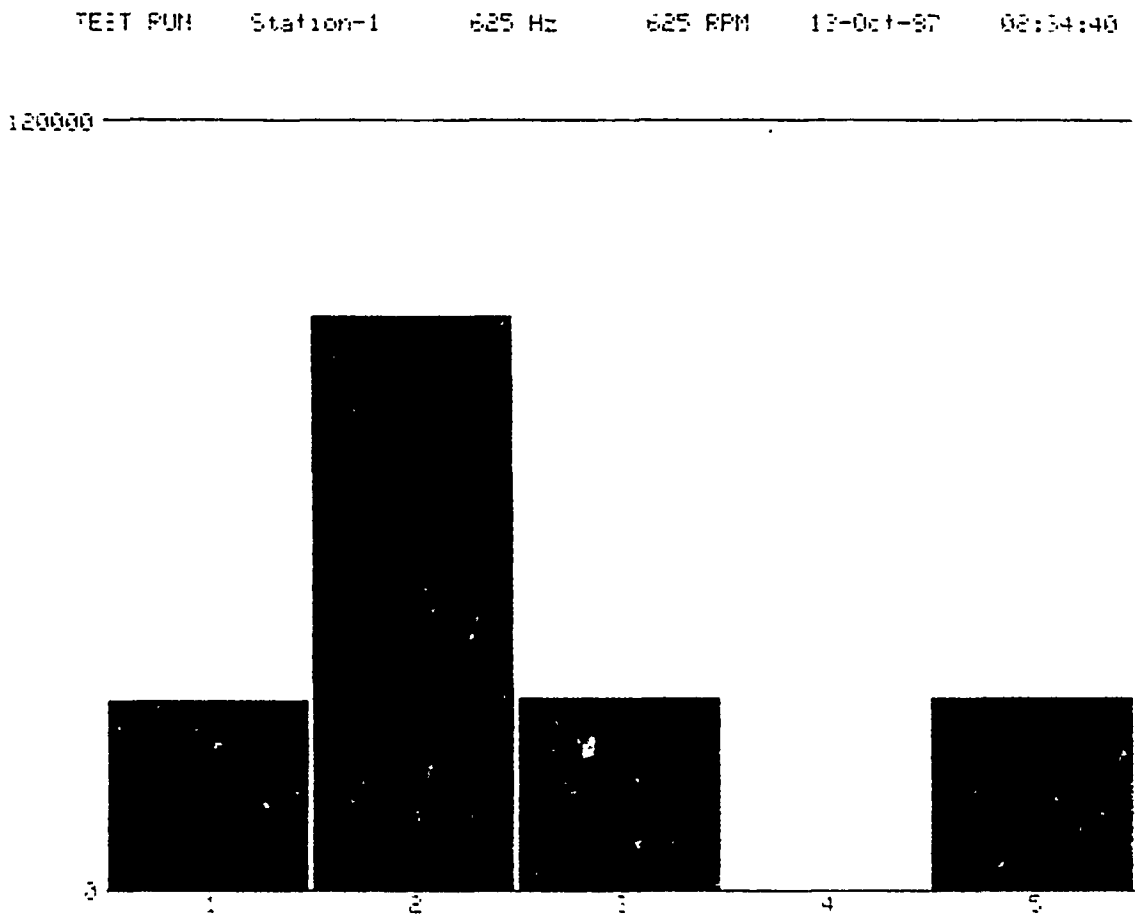
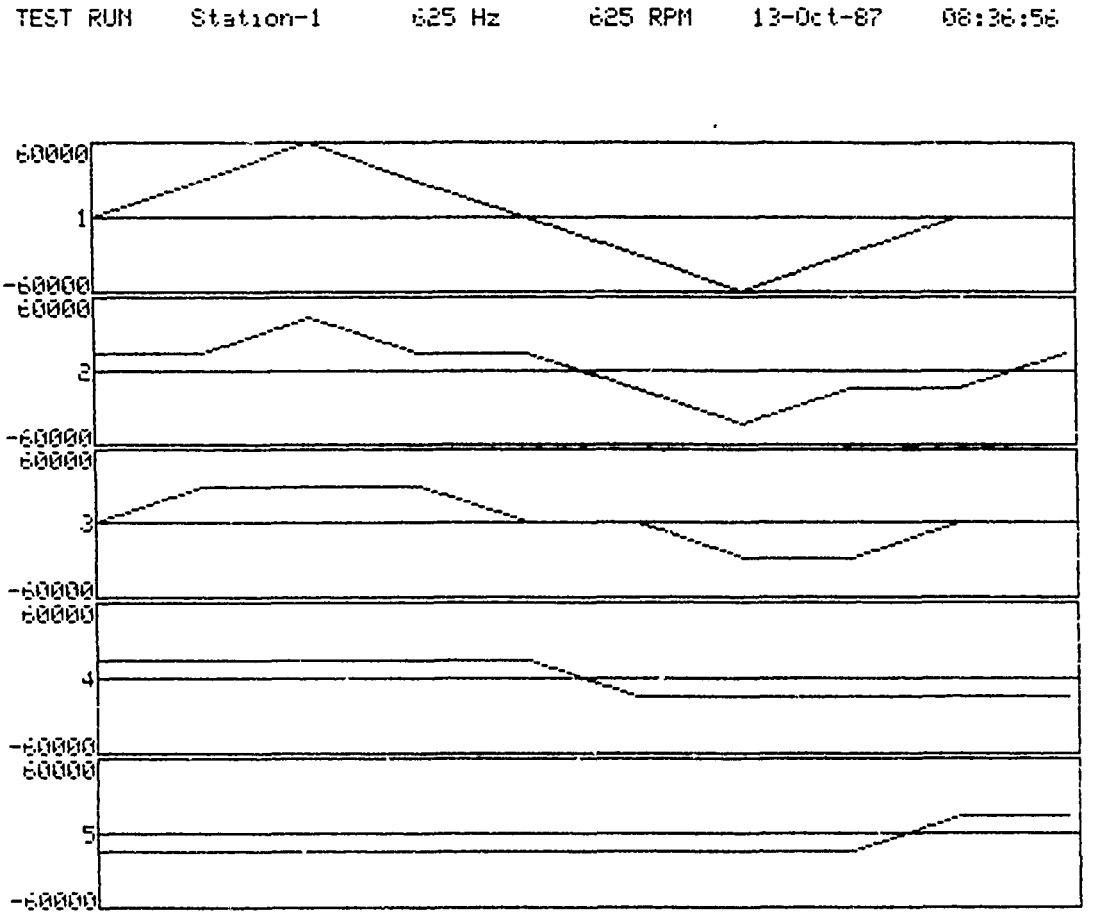


Figure 3: Main Menu Terminal Display



TITLE: HISTOGRAM TERMINAL DISPLAY				FILENAME: BLANK PLT FILEDATE: 07-Jul-1989	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE: 4	SHEET 1 OF 1	DESIGNER	DRAWN BY	FILETIME: 07 49 06	

Figure 4: Histogram Terminal Display



TITLE: REAL TIME TERMINAL DISPLAY				FILENAME: BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
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FIGURE: 5	SHEET 1 OF 1	DESIGNER	DRAWN BY	FILETIME: 07 49 06	

Figure 5: Real Time Terminal Display

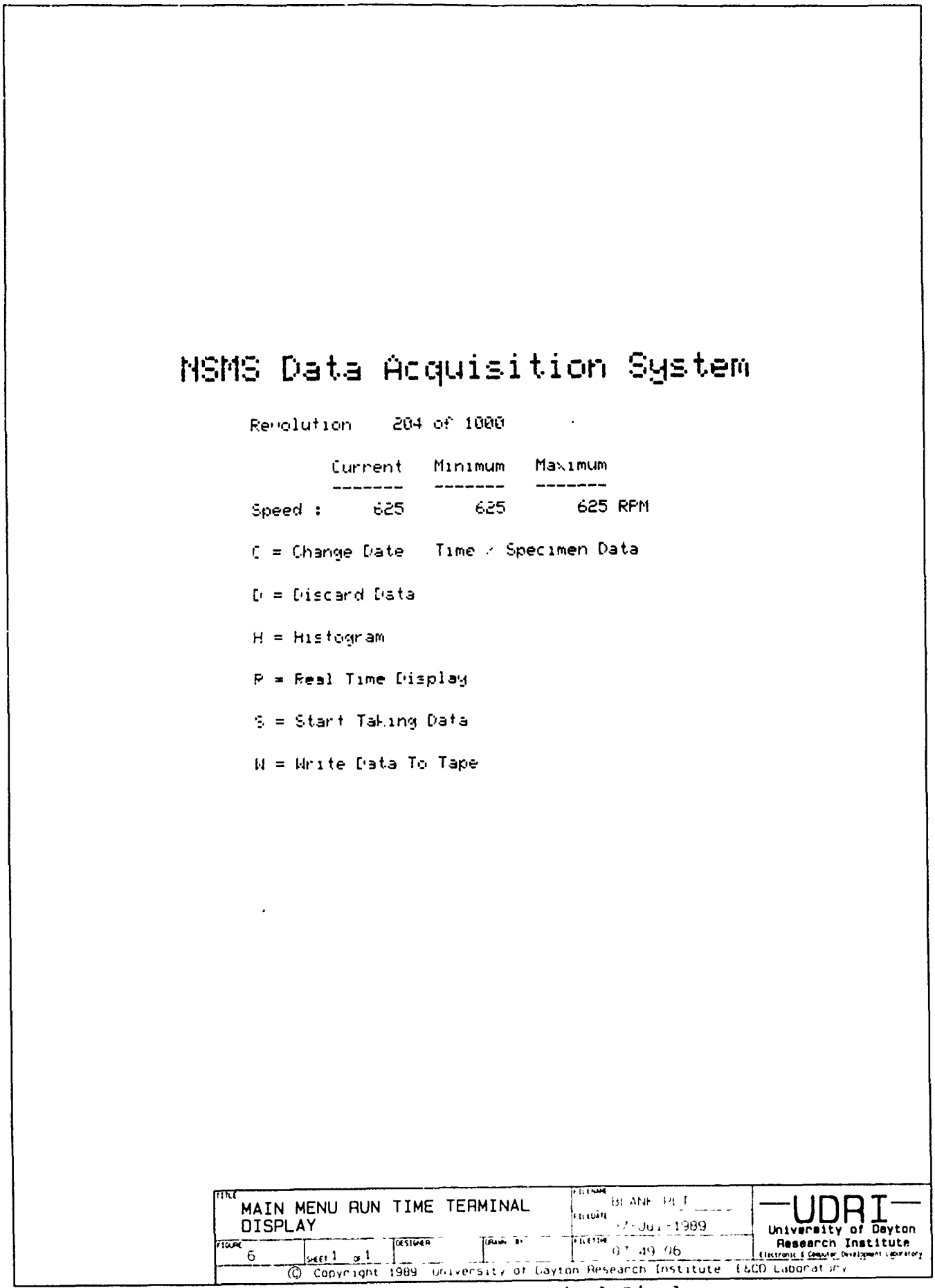


Figure 6: Main Menu Run Time Terminal Display

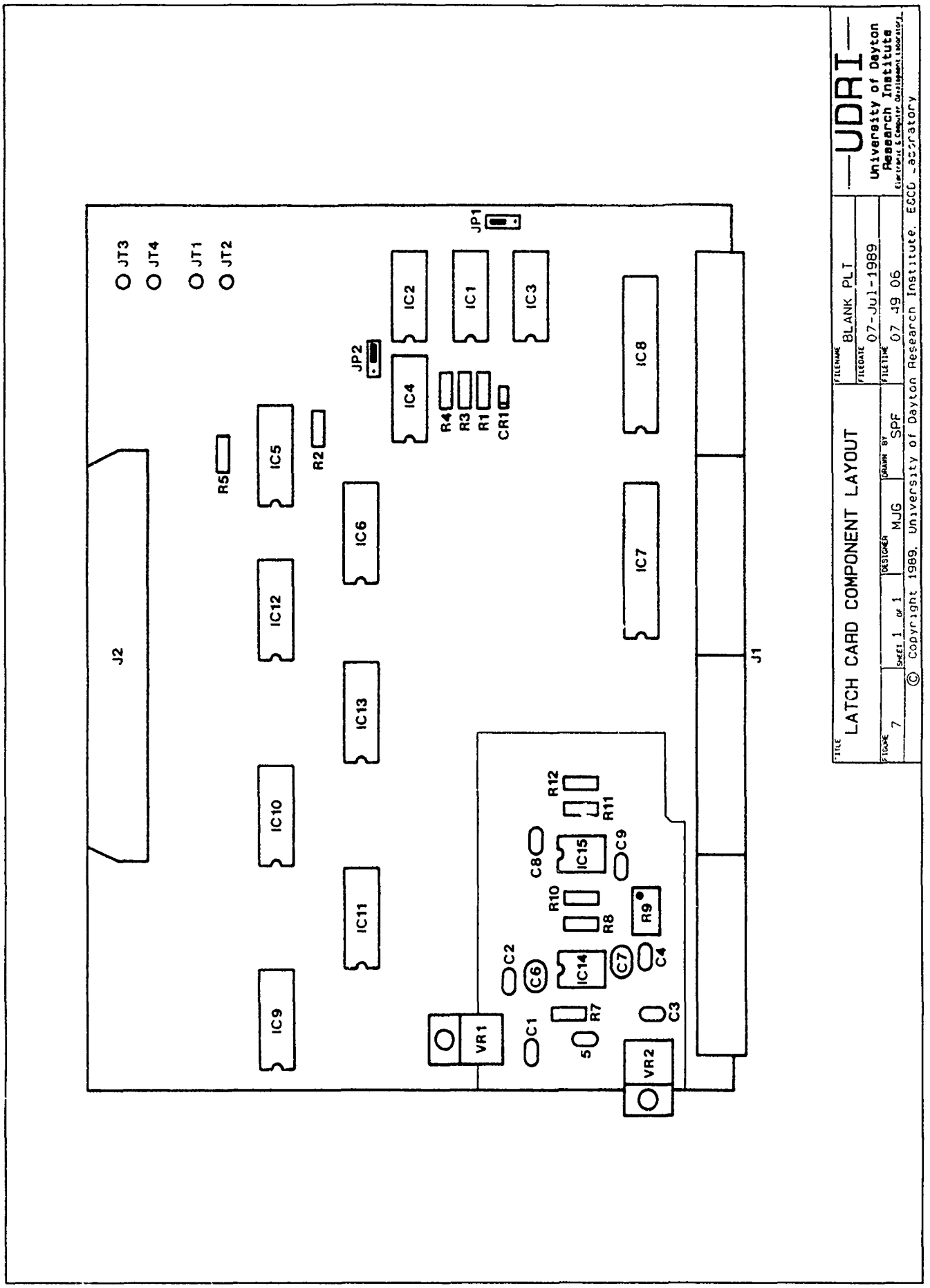


Figure 7: Latch Card Component Layout

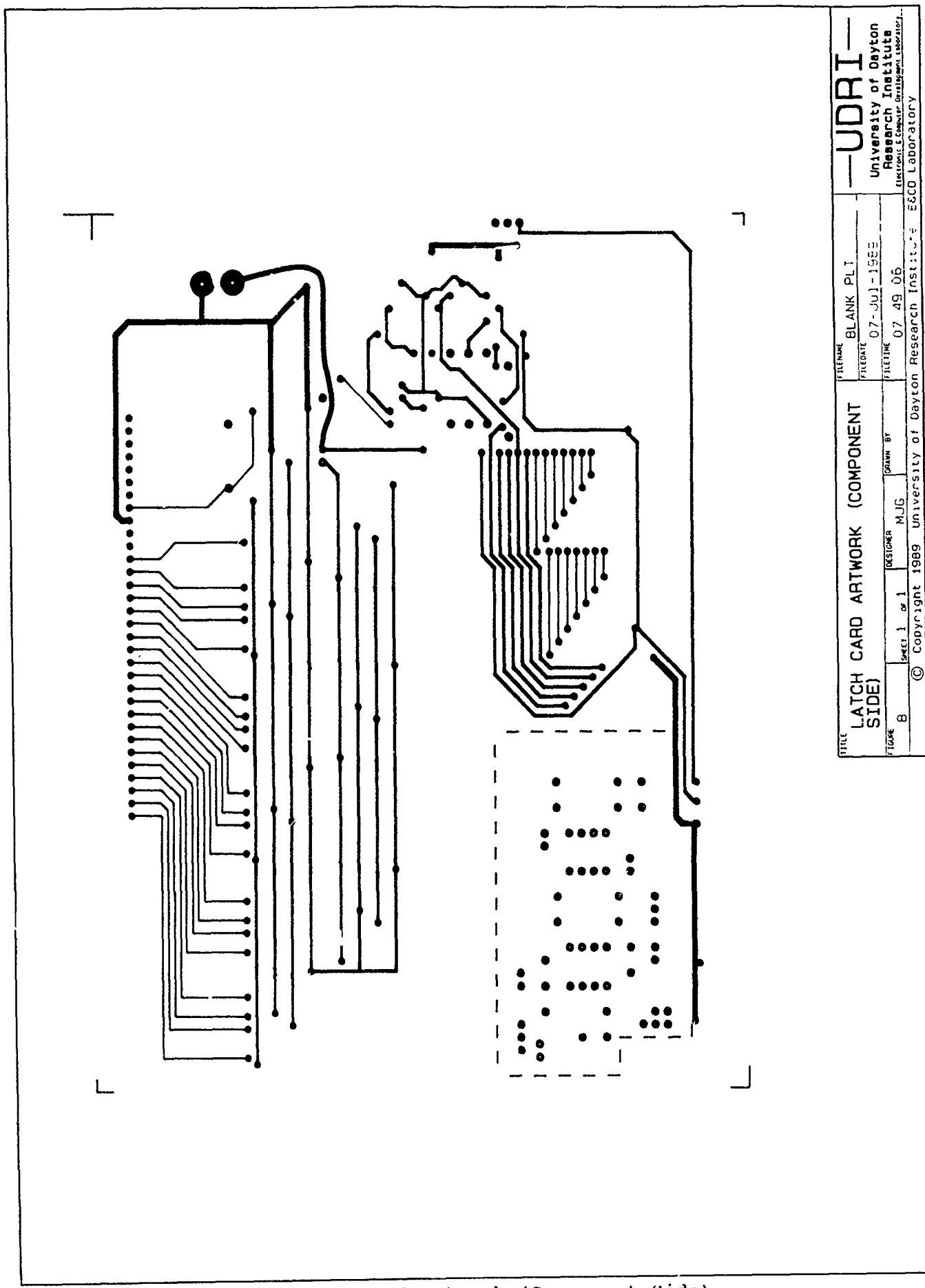


Figure 8: Latch Card Artwork (Component Side)

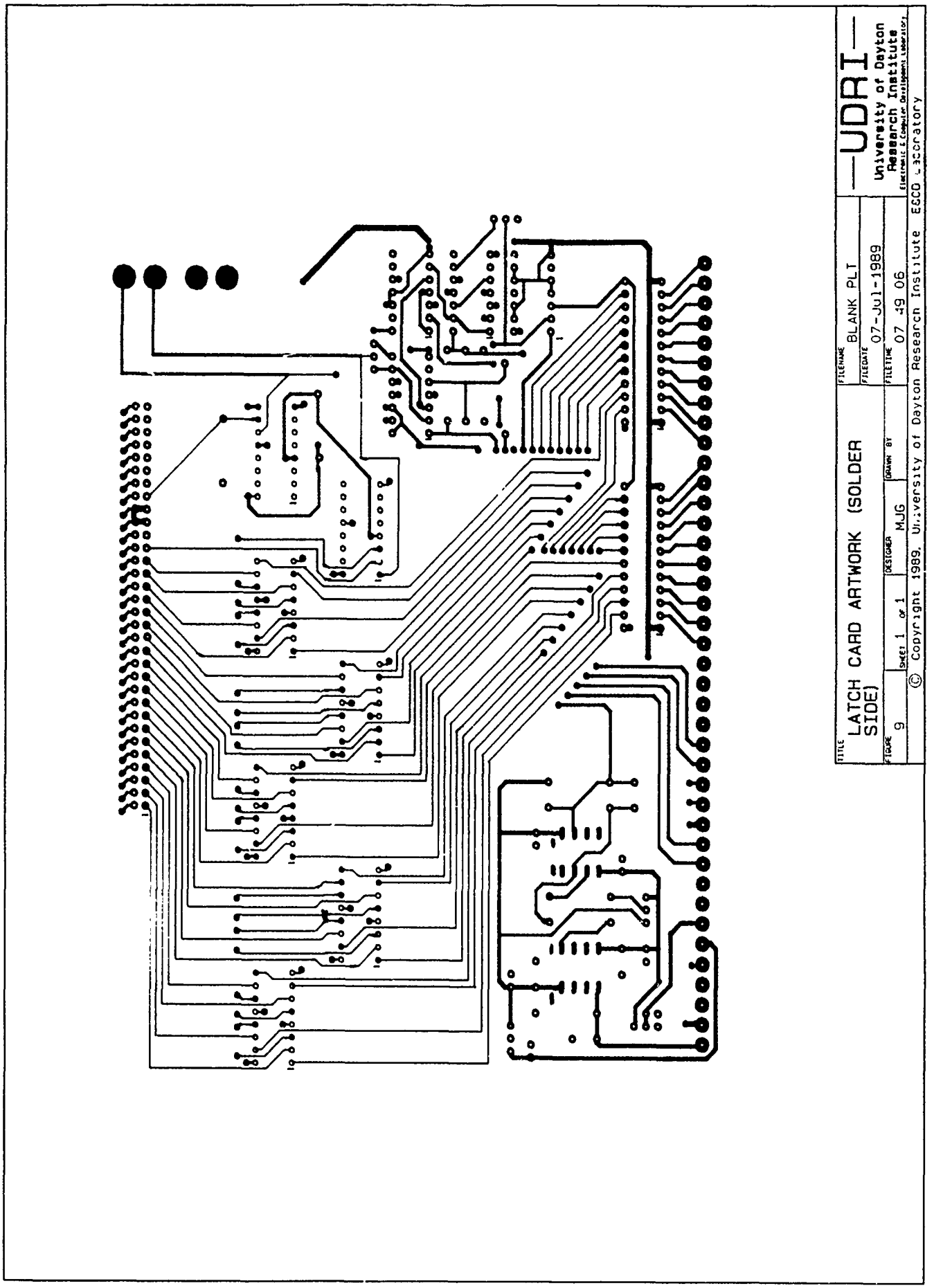


Figure 9: Latch Card Artwork (Solder Side)

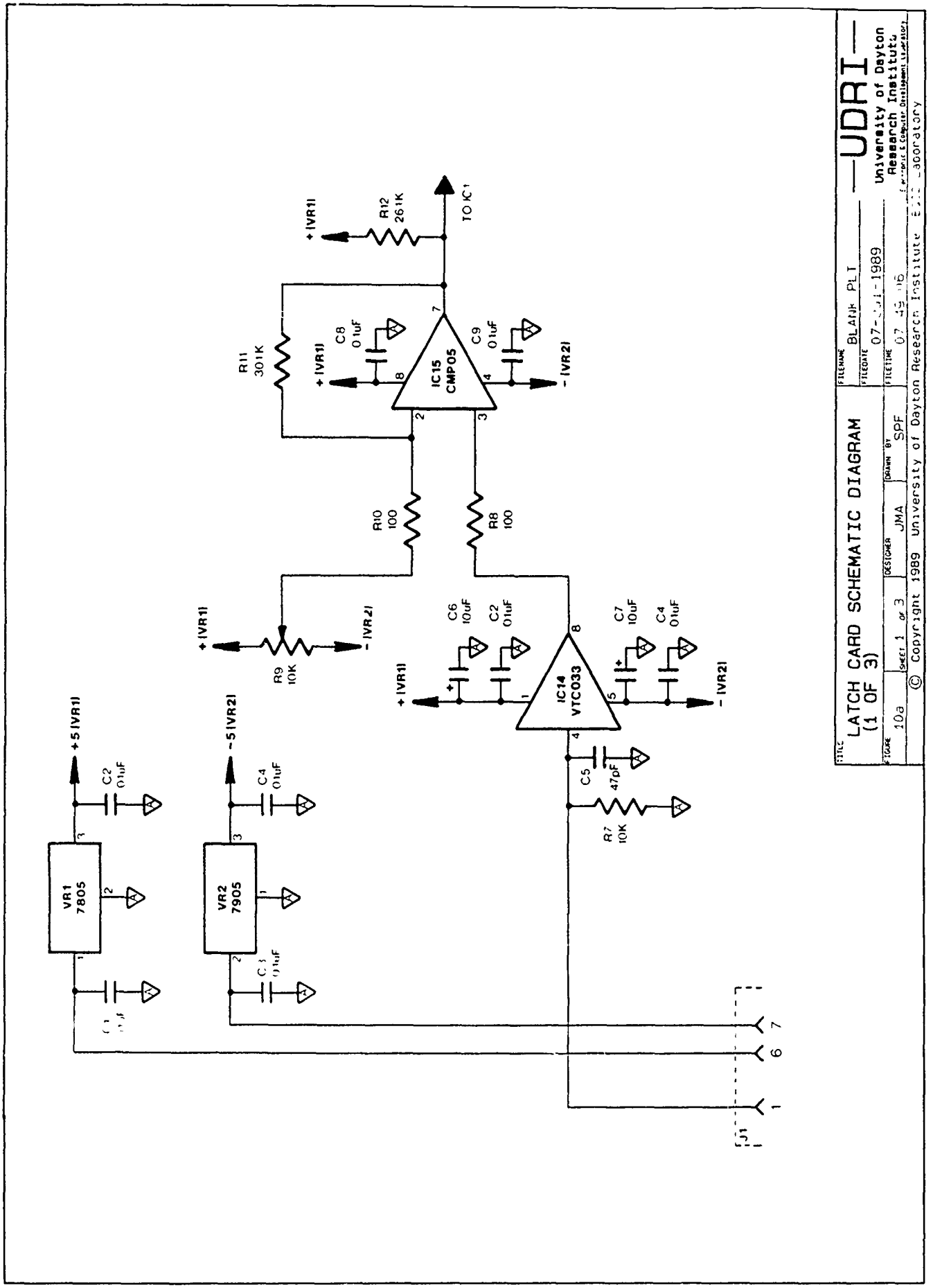


Figure 10a: Latch Card Schematic Diagram (1 of 3)

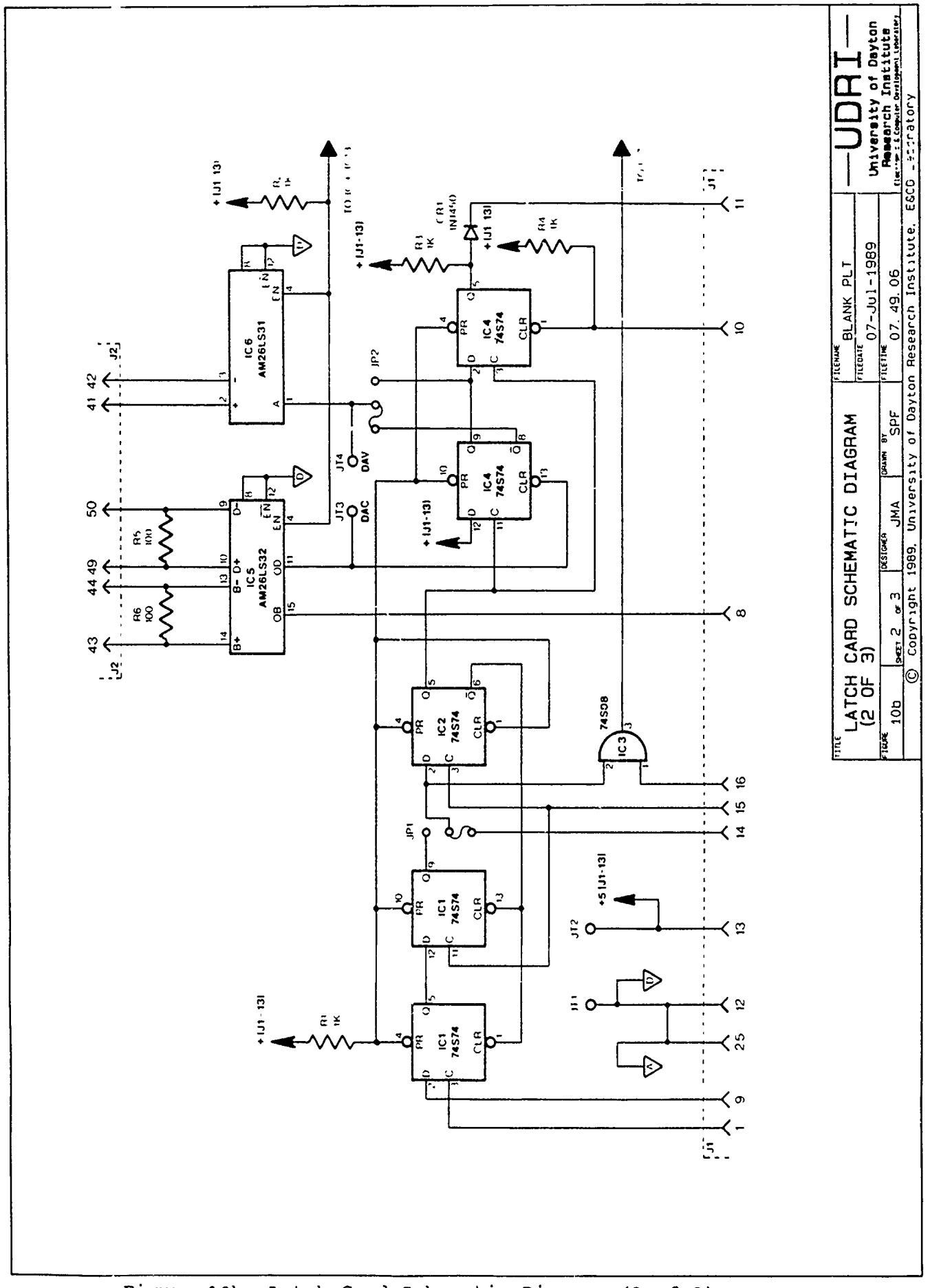


Figure 10b: Latch Card Schematic Diagram (2 of 3)

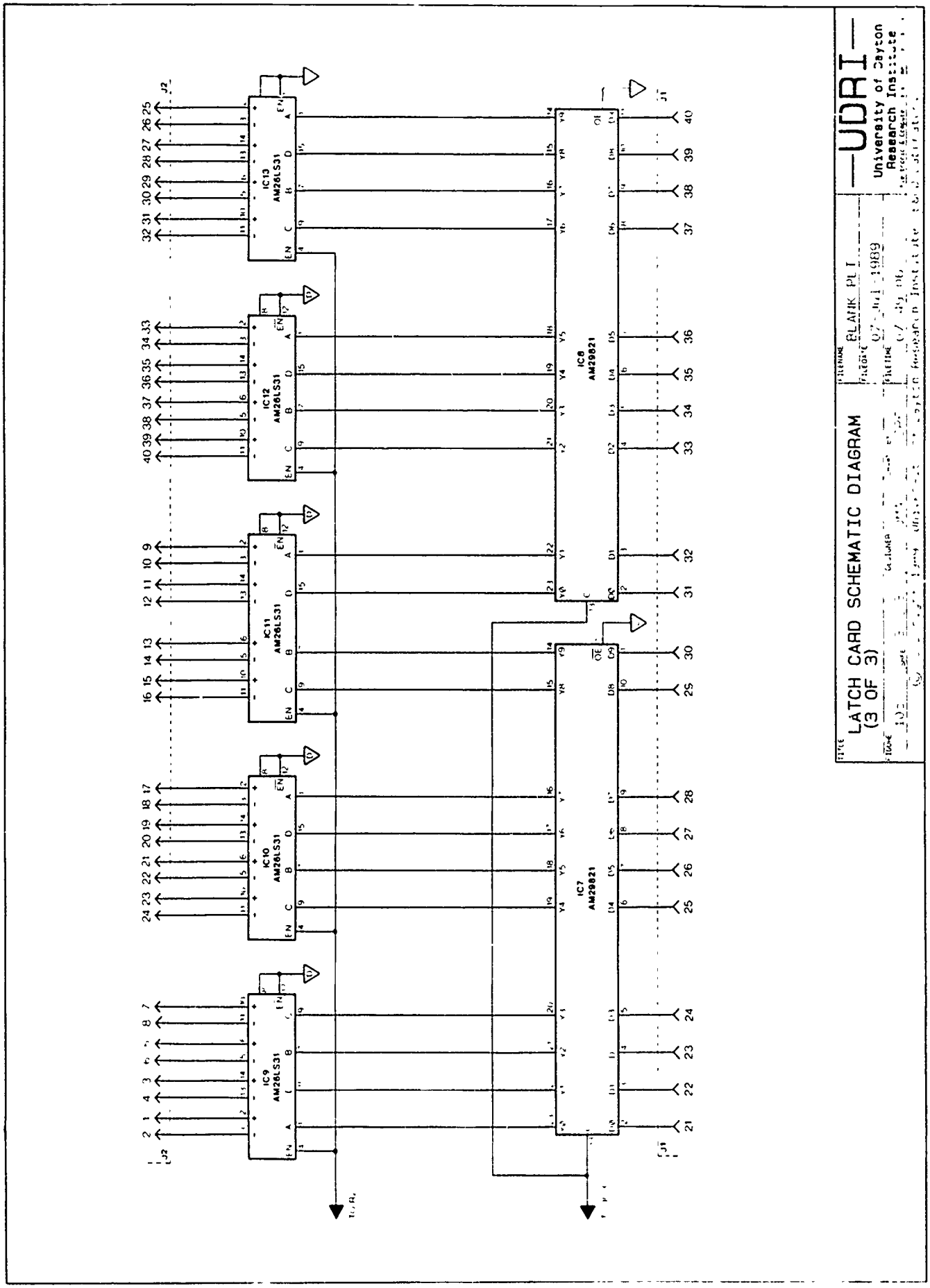


Figure 10c: Latch Card Schematic Diagram (3 of 3)

Latch Card Parts List

Part Number	Description
R1 - R5	1 KOhm
R7 10	KOhm
R8, R10	100 Ohm
R11	30.1 KOhm
R12	26.1 KOhm
R9	10KOhm Trimpot
C1 - C4, C8, C9	0.1 uF
C5	47 pF
C6, C7	10 uF Tantalum
IC1, IC2, IC4	74S74
IC3	74S08
IC5	Am26LS32
IC6, IC9 - IC13	Am26LS31
IC7, IC8	Am29821
IC14	VTC033
IC15	CMP05
VR1	7805
VR2	7905
CR1	1N4150
J1	Molex .156 10 position (x4)
J2	Ansley Blue Macs 50 pin male

Table 1: Latch Card Parts List

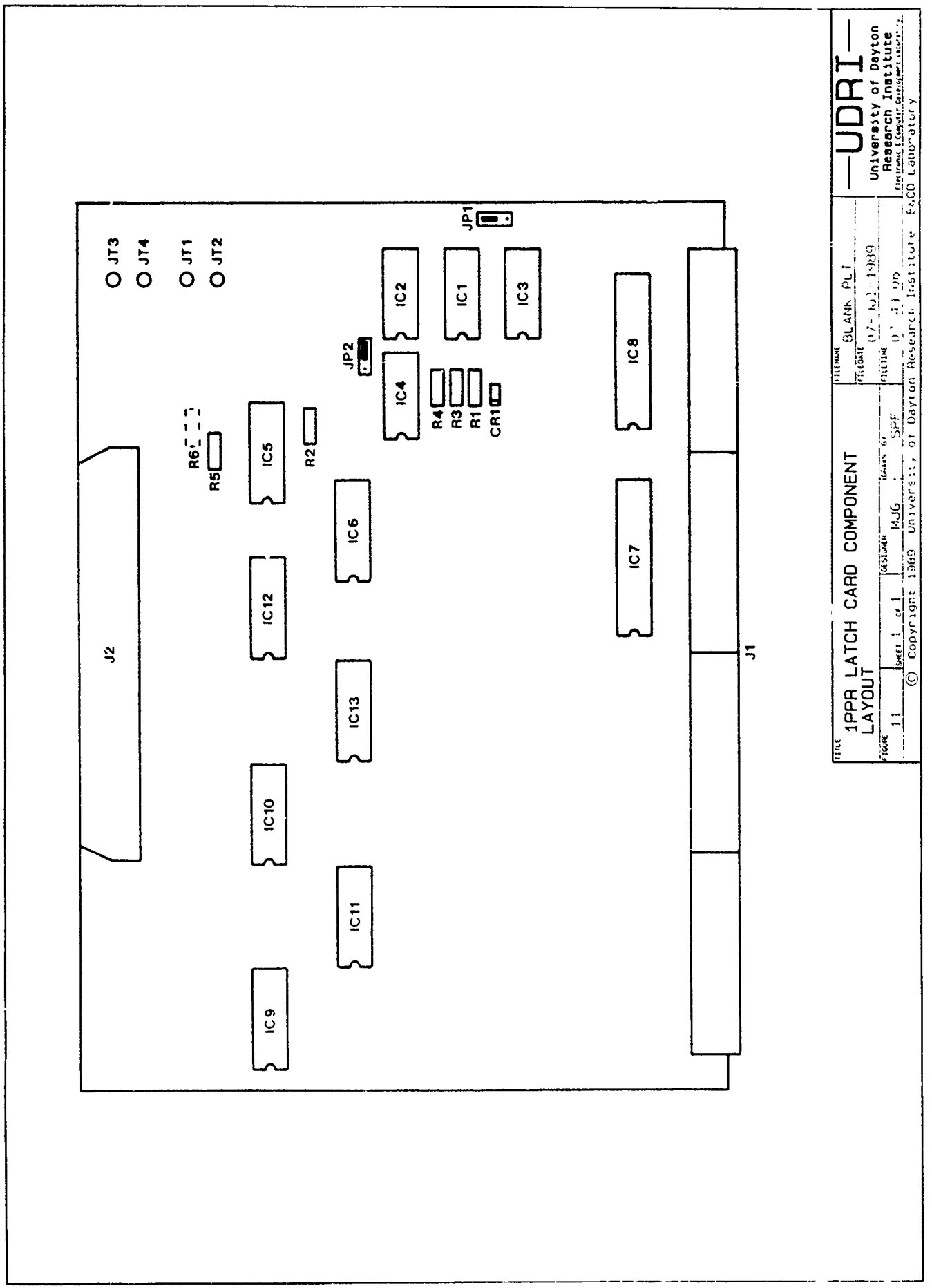


Figure 11: 1PPR Latch Card Component Layout

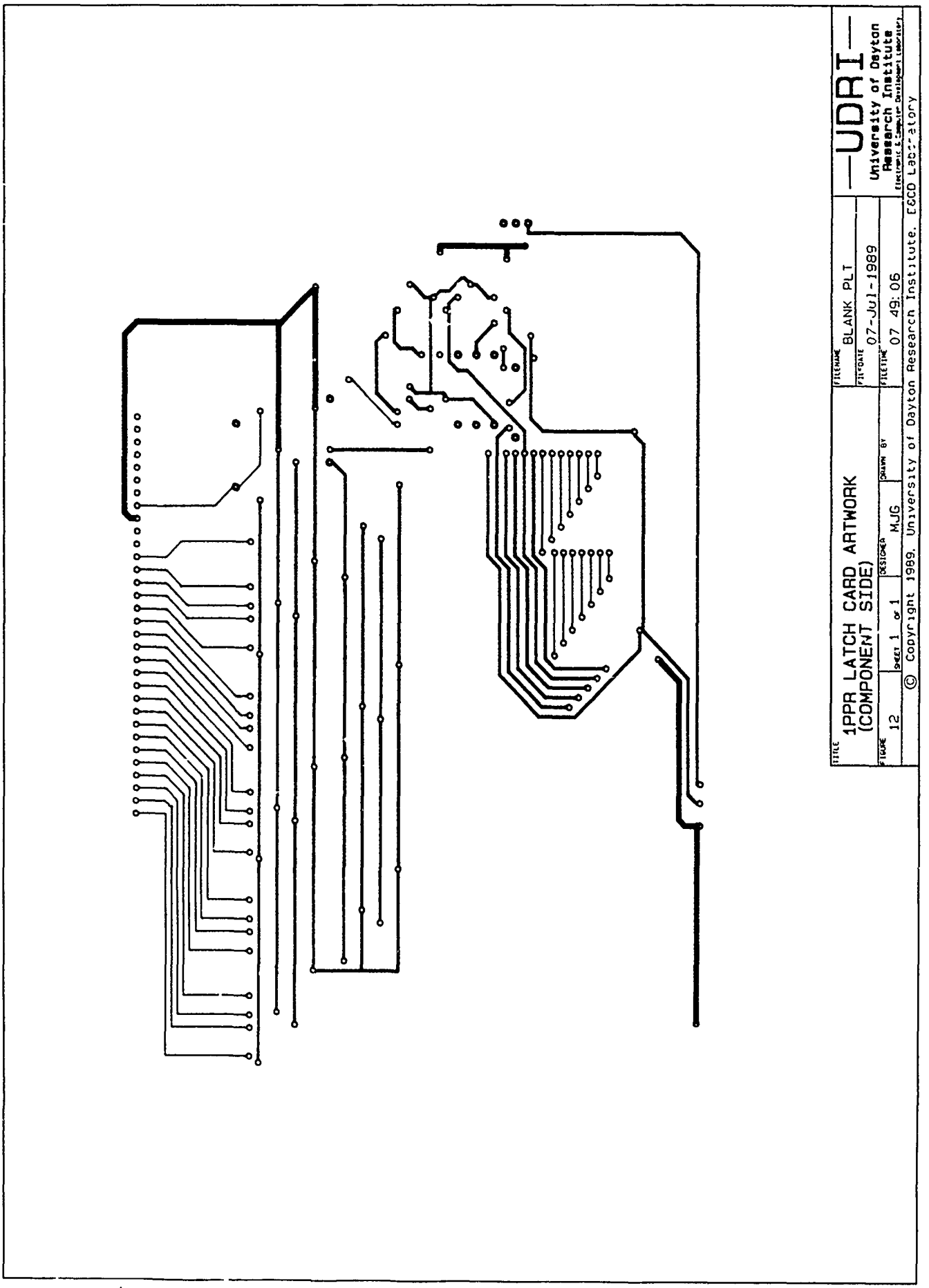


Figure 12: 1PPR Latch Card Artwork (Component Side)

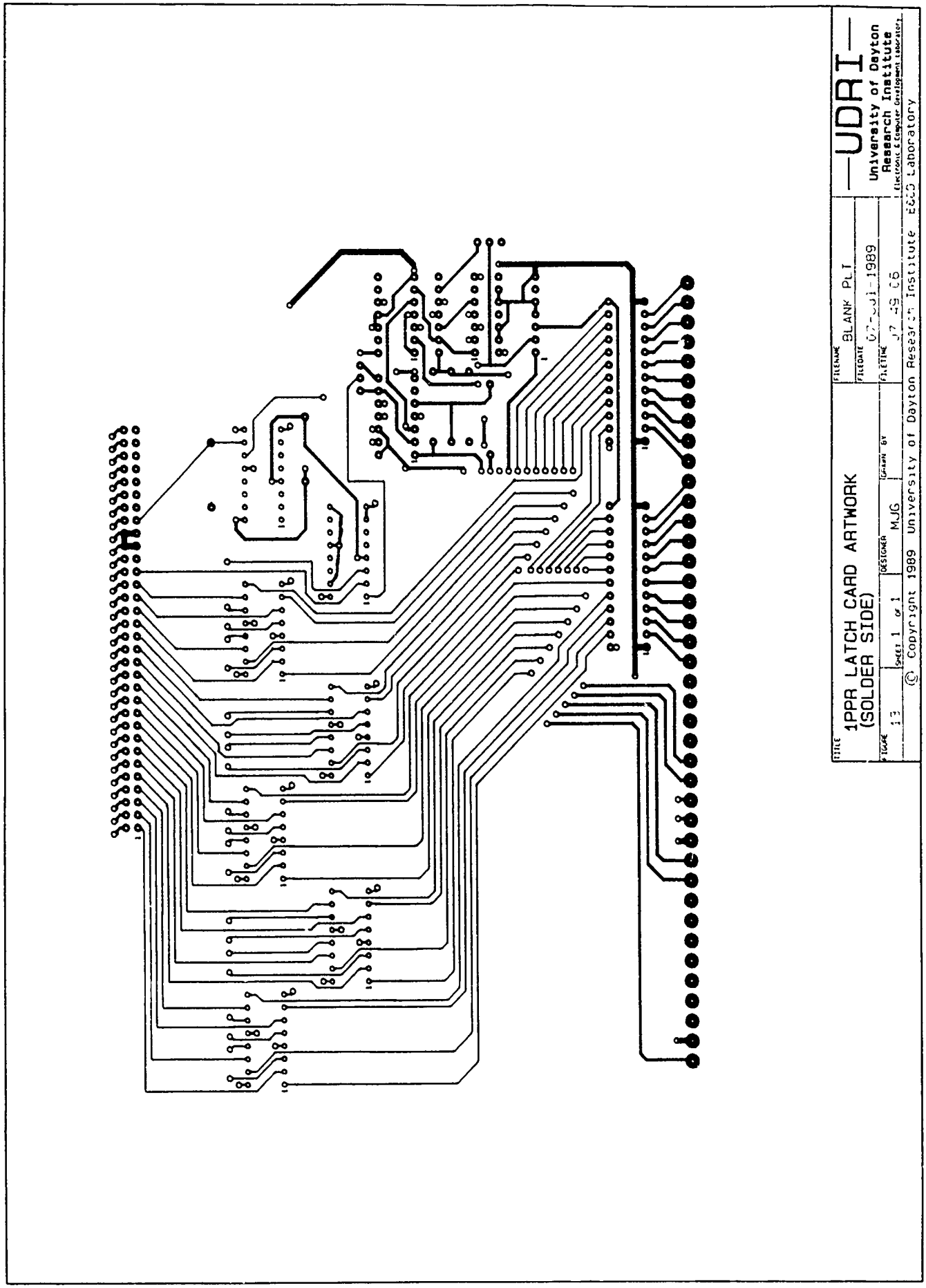


Figure 13: 1PPR Latch Card Artwork (Solder Side)

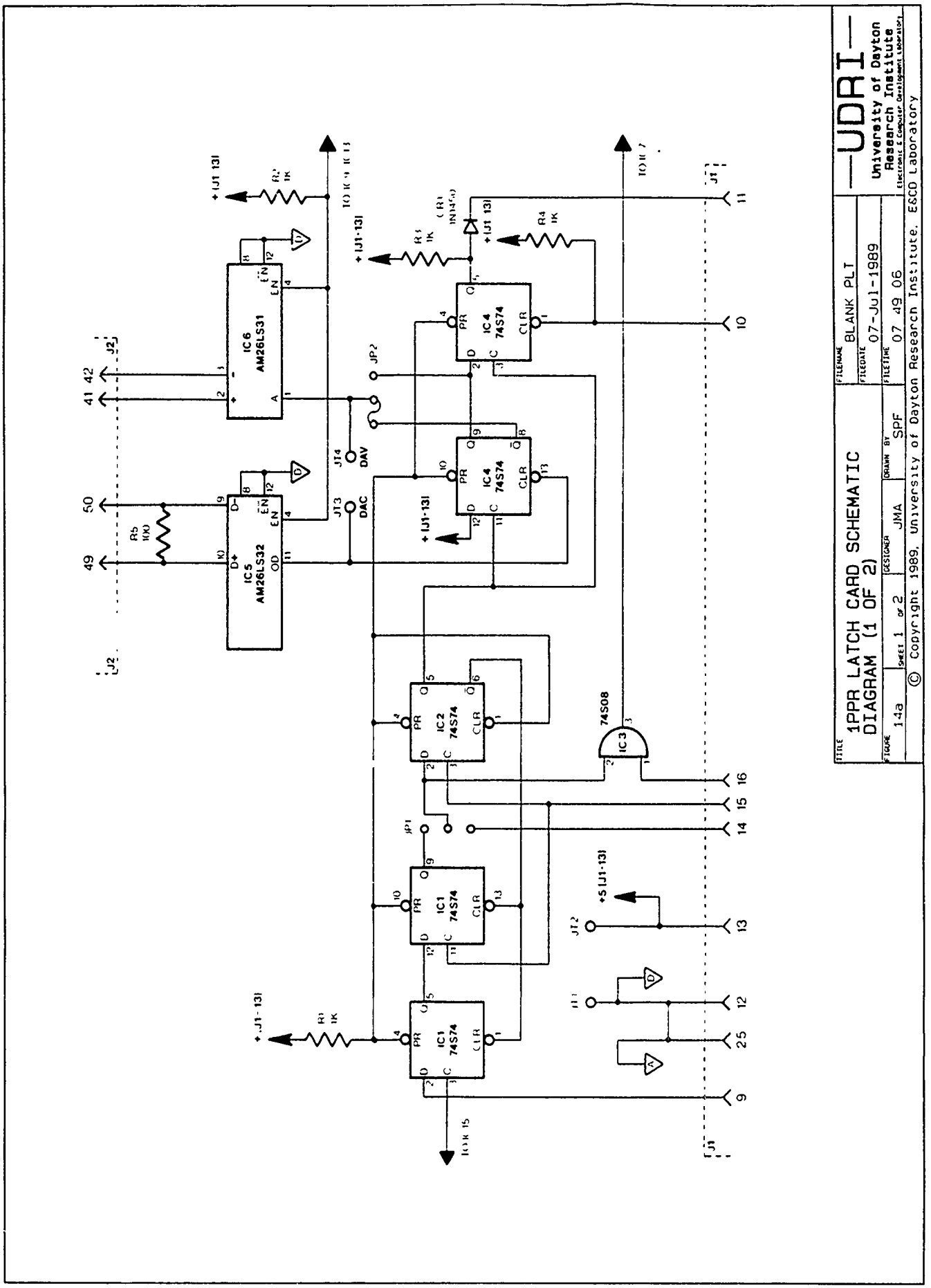


Figure 14a: 1PPR Latch Card Schematic Diagram (1 of 2)

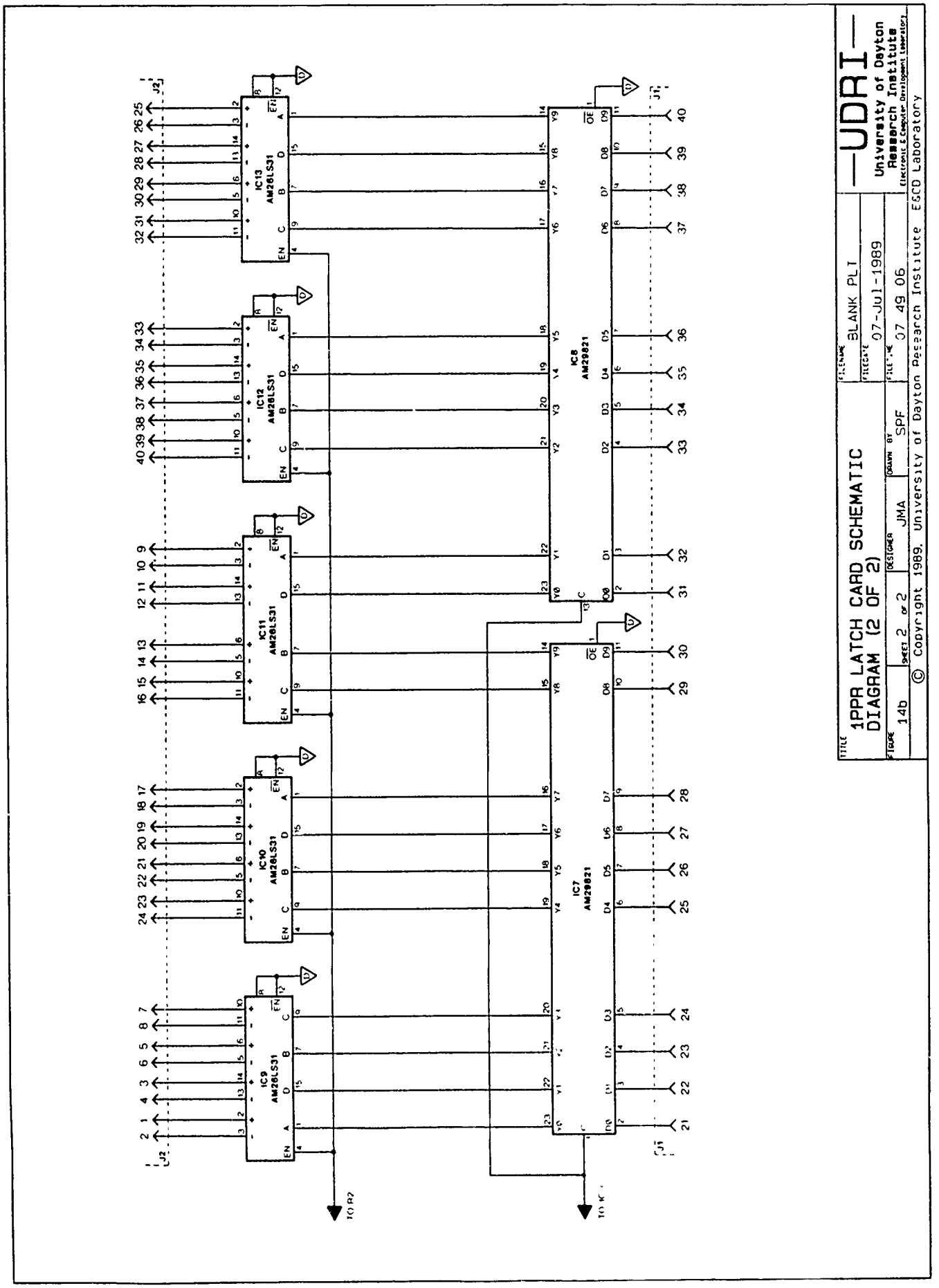


Figure 14b: 1PPR Latch Card Schematic Diagram (2 of 2)

1PPR Latch Card Parts List

Part Number	Description
R1 - R6	1 KOhm
IC1, IC2, IC4	74S74
IC3	74S08
IC5	Am26LS32
IC6, IC9 - IC13	Am26LS31
IC7, IC8	Am29821
CR1	1N4150
J1	Molex .156 10 position (x4)
J2	Ansley Blue Macs 50 pin male

Table 2: 1PPR Latch Card Parts List

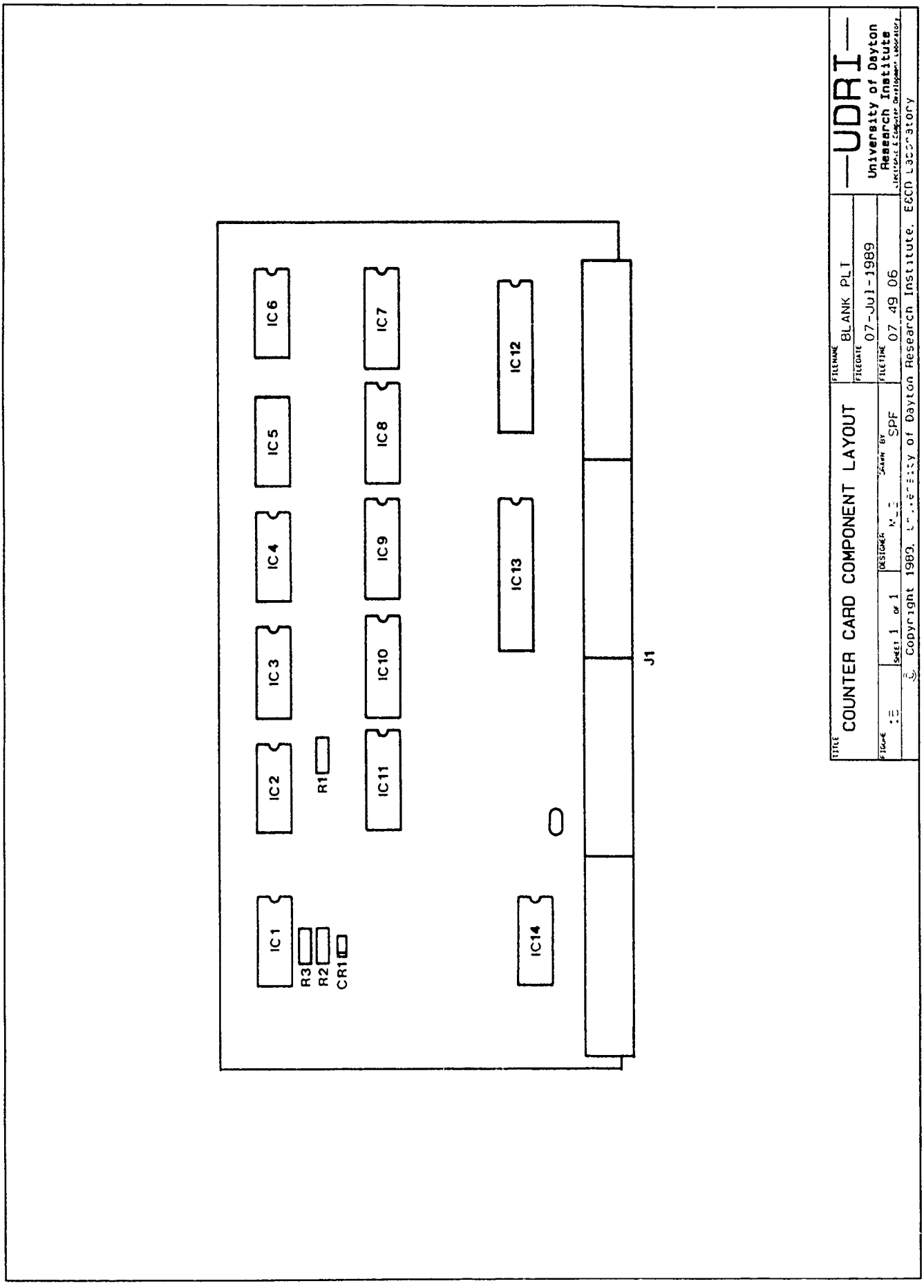


Figure 15: Counter Card Component Layout

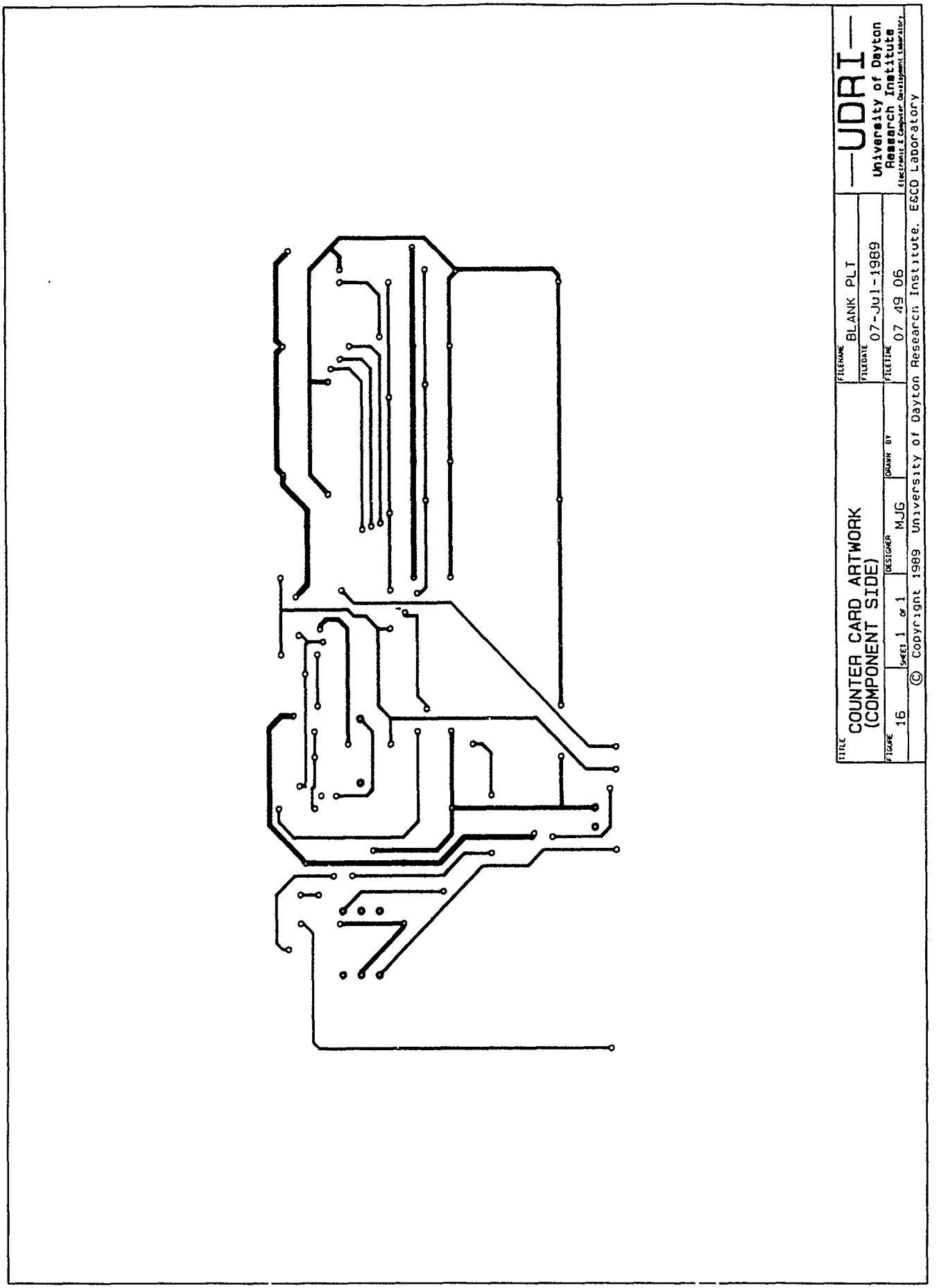


Figure 16: Counter Card Artwork (Component Side)

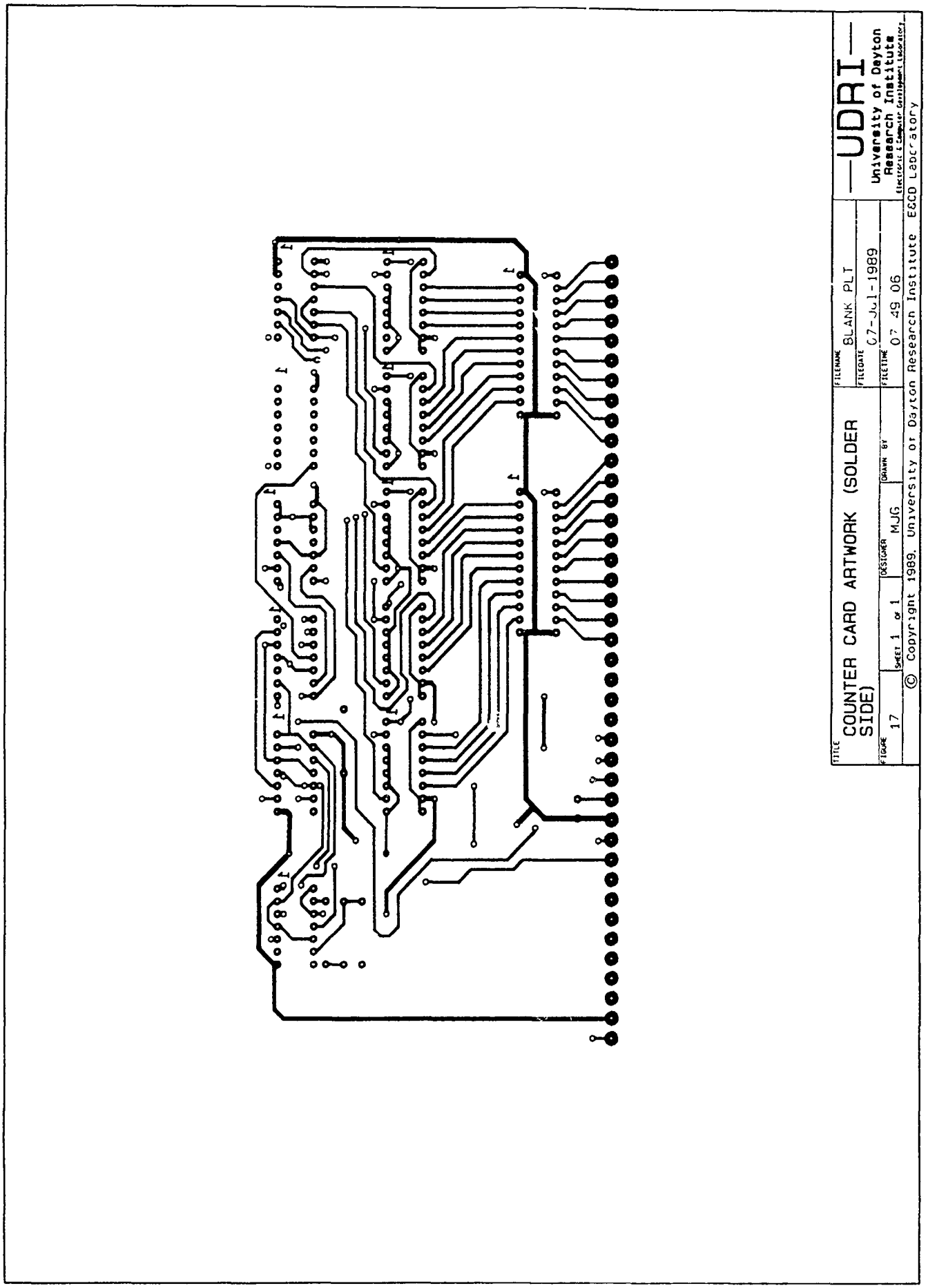


Figure 17: Counter Card Artwork (Solder Side)

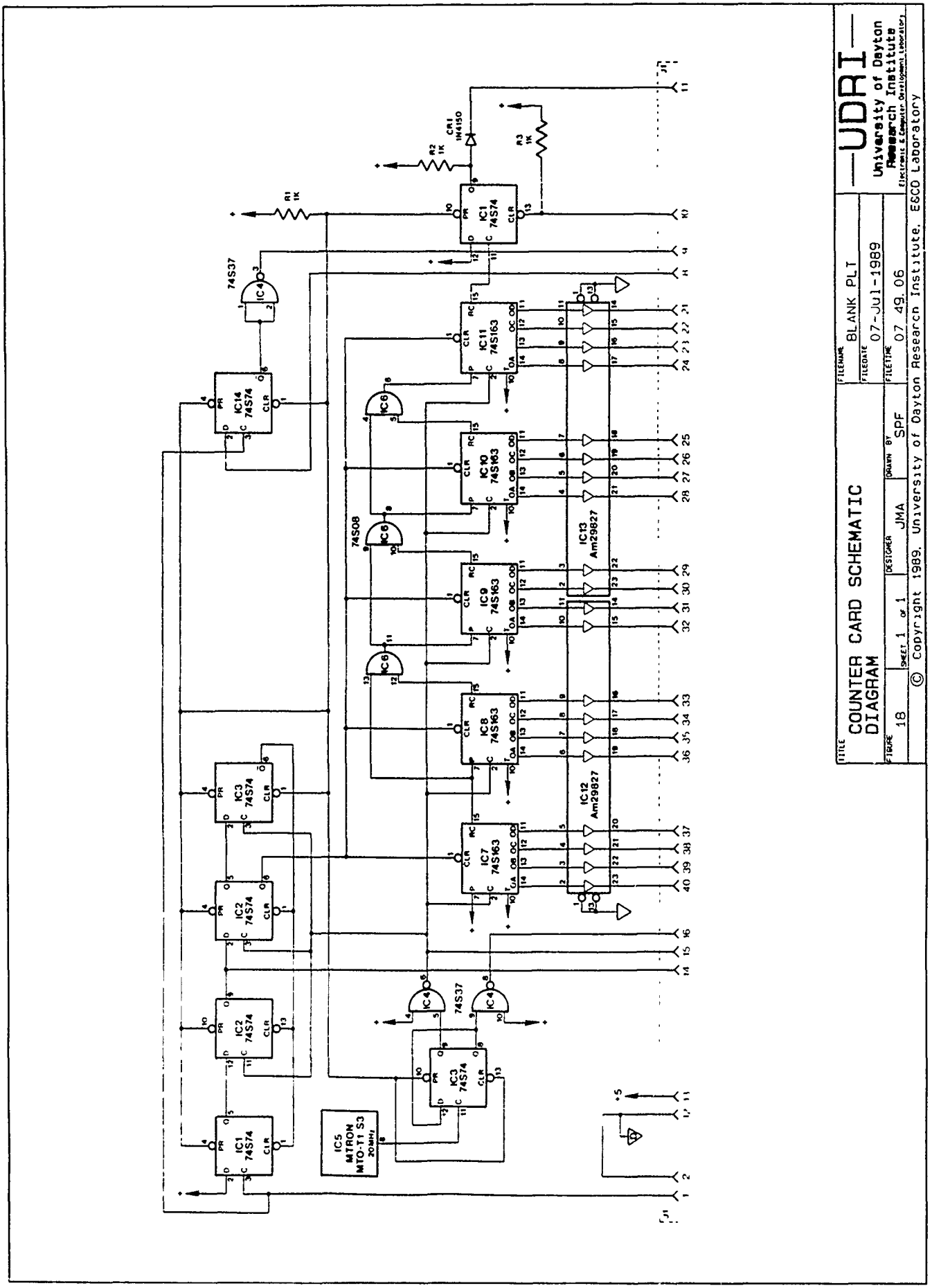
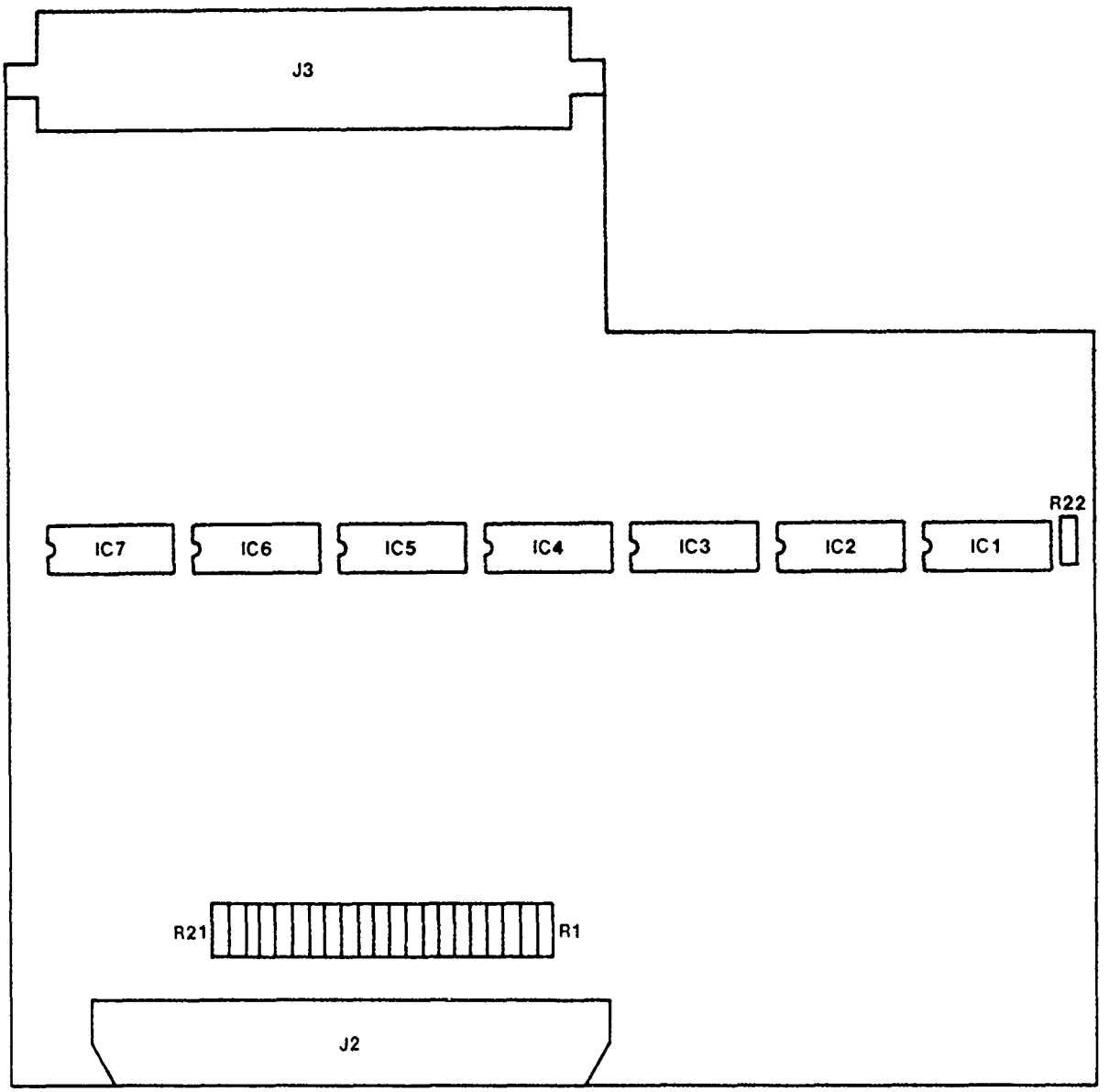


Figure 18: Counter Card Schematic Diagram

Counter Card Parts List

Part Number	Description
R1 - R3	1 KOhm
IC1 - IC3	74S74
IC4	74S37
IC5	MTO-T1-S3 (Mtron)
IC6	74S08
IC7 - IC11	74S163
IC12, IC13	Am29827
CR1	1N4150
J1	Molex .156 10 position (x4)

Table 3: Counter Card Parts List



TITLE: RECEIVER AND 1PPR RECEIVER CARDS COMPONENT LAYOUT				FILENAME: BLANK PLT	UDRI — University of Dayton Research Institute, Electronic & Computer Development Laboratory
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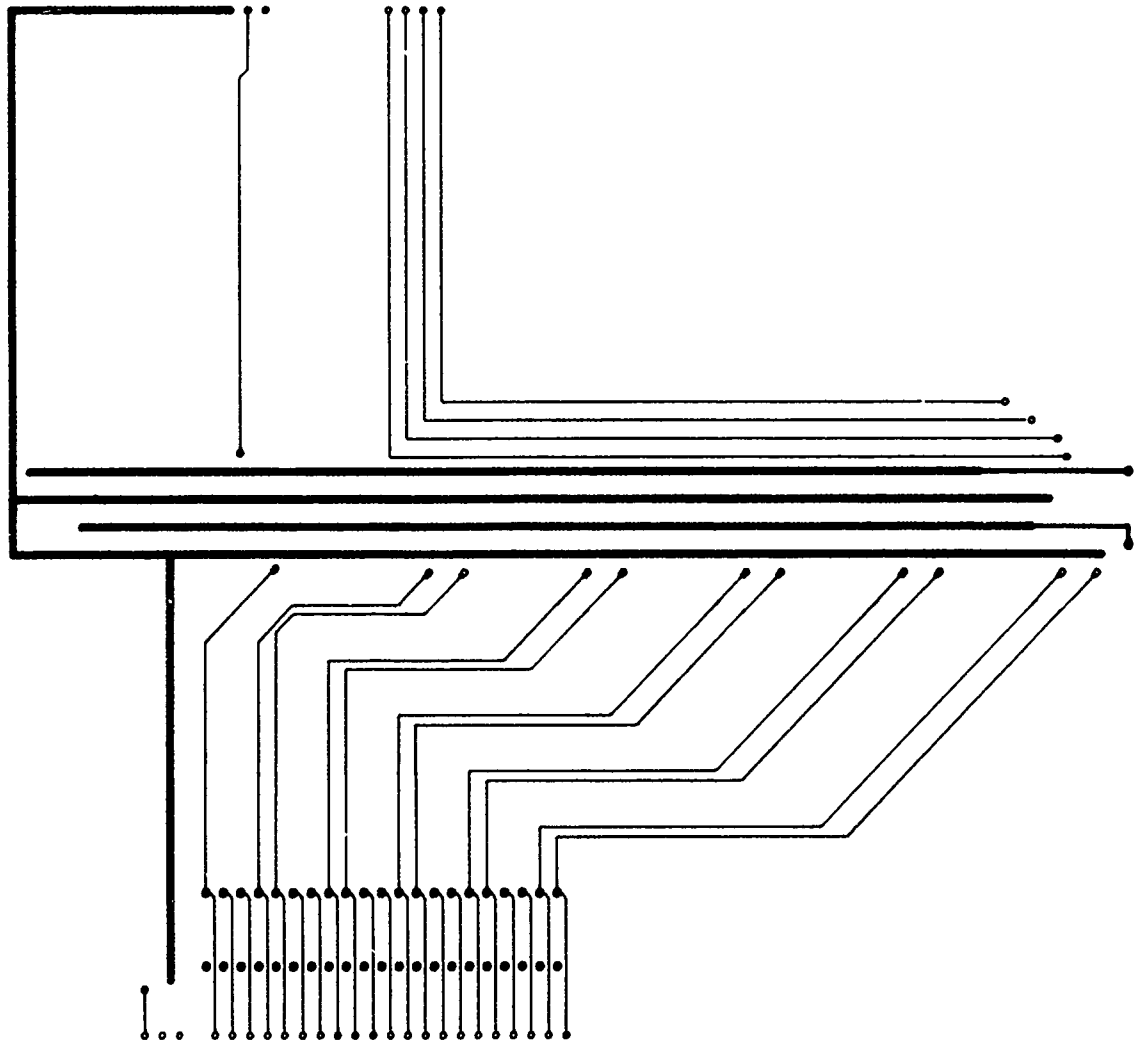
FIGURE: 19	SHEET 1 OF 1	DESIGNER: MJG	DRAWN BY: SPF	FILETIME: 07 49 06	

Figure 19: Receiver and 1PPR Receiver Cards Component Layout



TITLE: RECEIVER AND 1PPR RECEIVER CARDS ARTWORK (COMP. SIDE)		FILENAME: RCARD.PLT	UDRI — University of Dayton Research Institute, Electronic & Computer Development Laboratory
FIGURE: 20	SHEET 1 of 1	DESIGNER: MJG	DRAWN BY:
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Figure 20: Reciever and 1PPR Receiver Cards Artwork (Comp. Side)

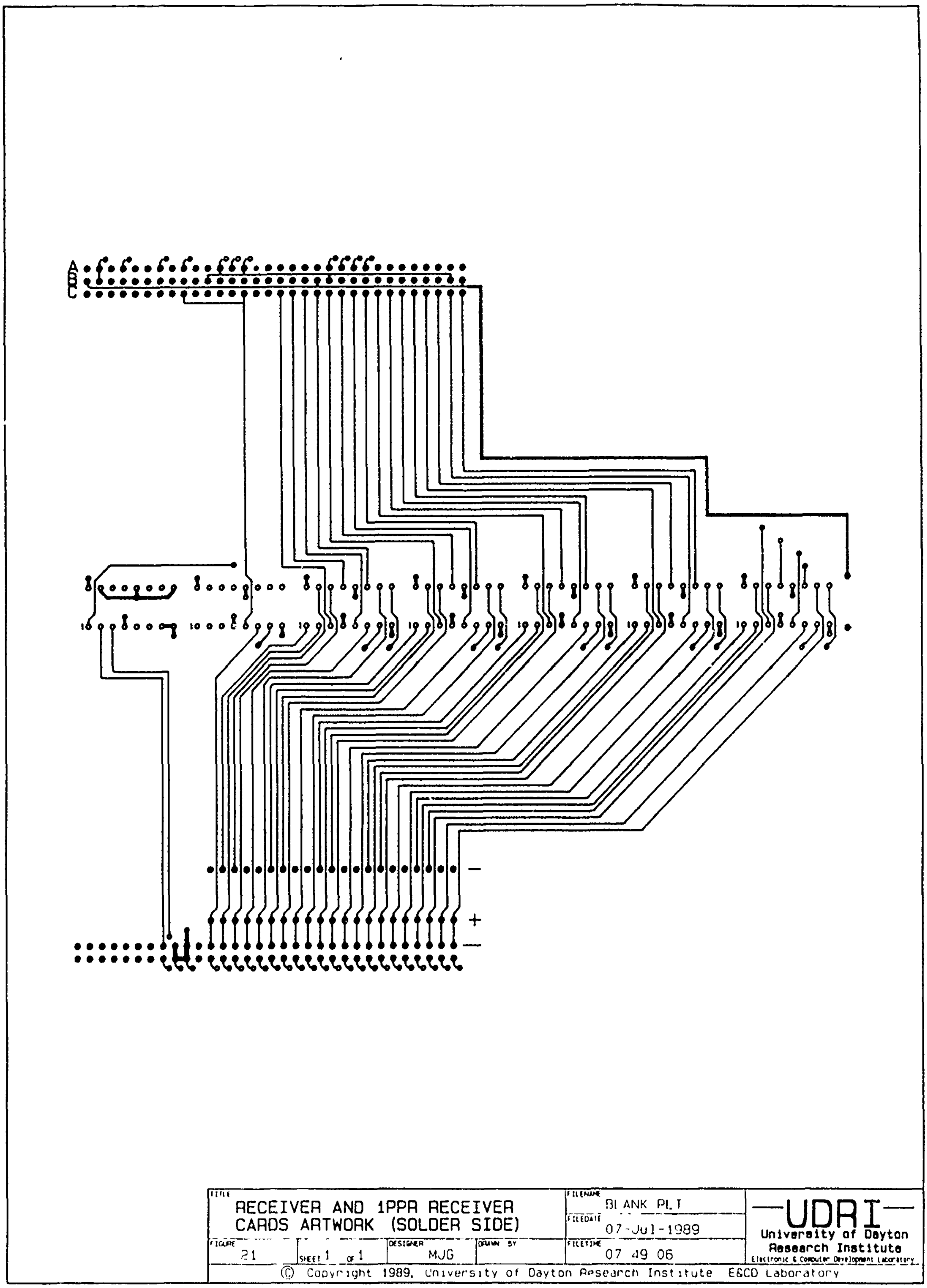
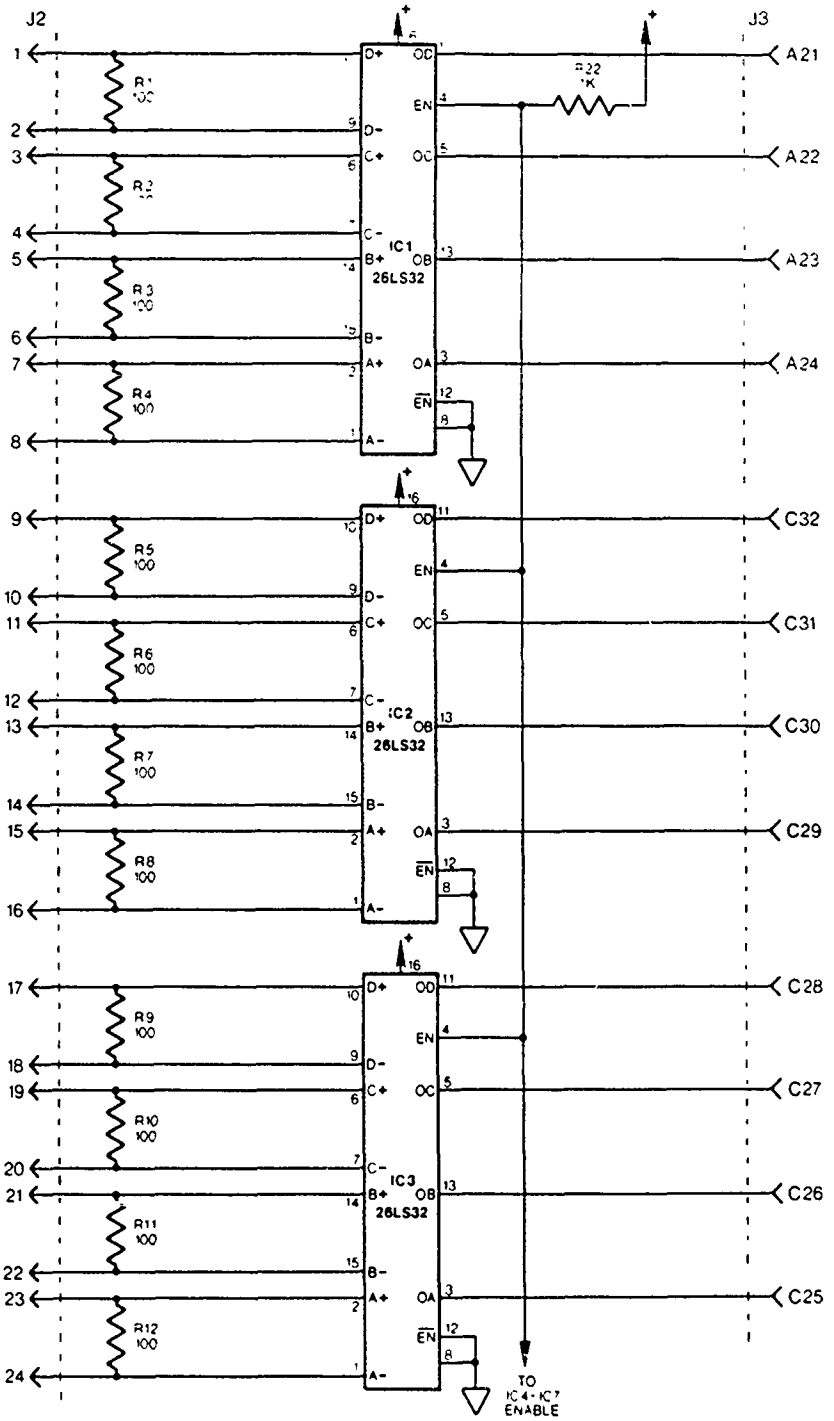
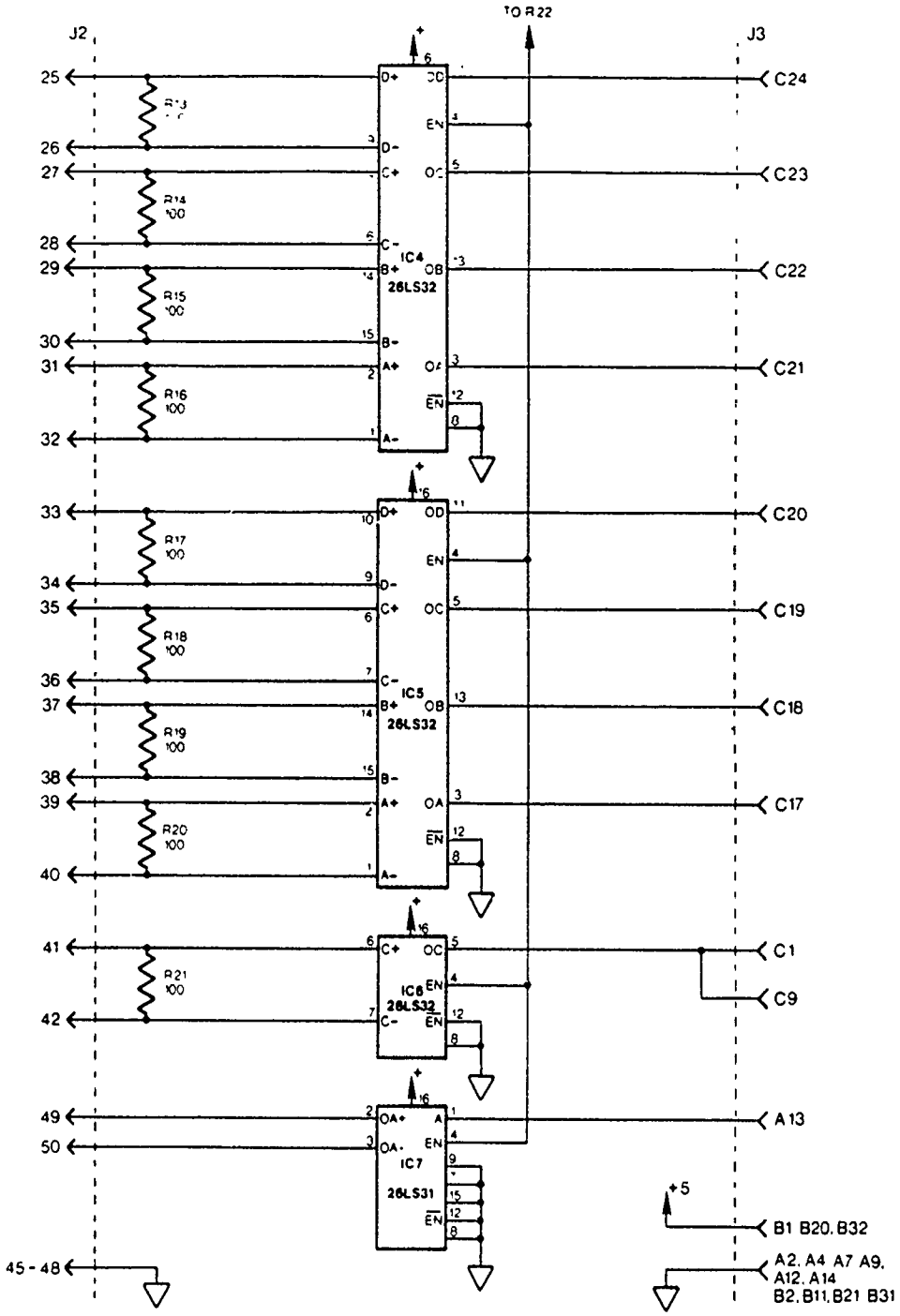


Figure 21: Receiver and 1PPR Receiver Cards Artwork (Solder Side)



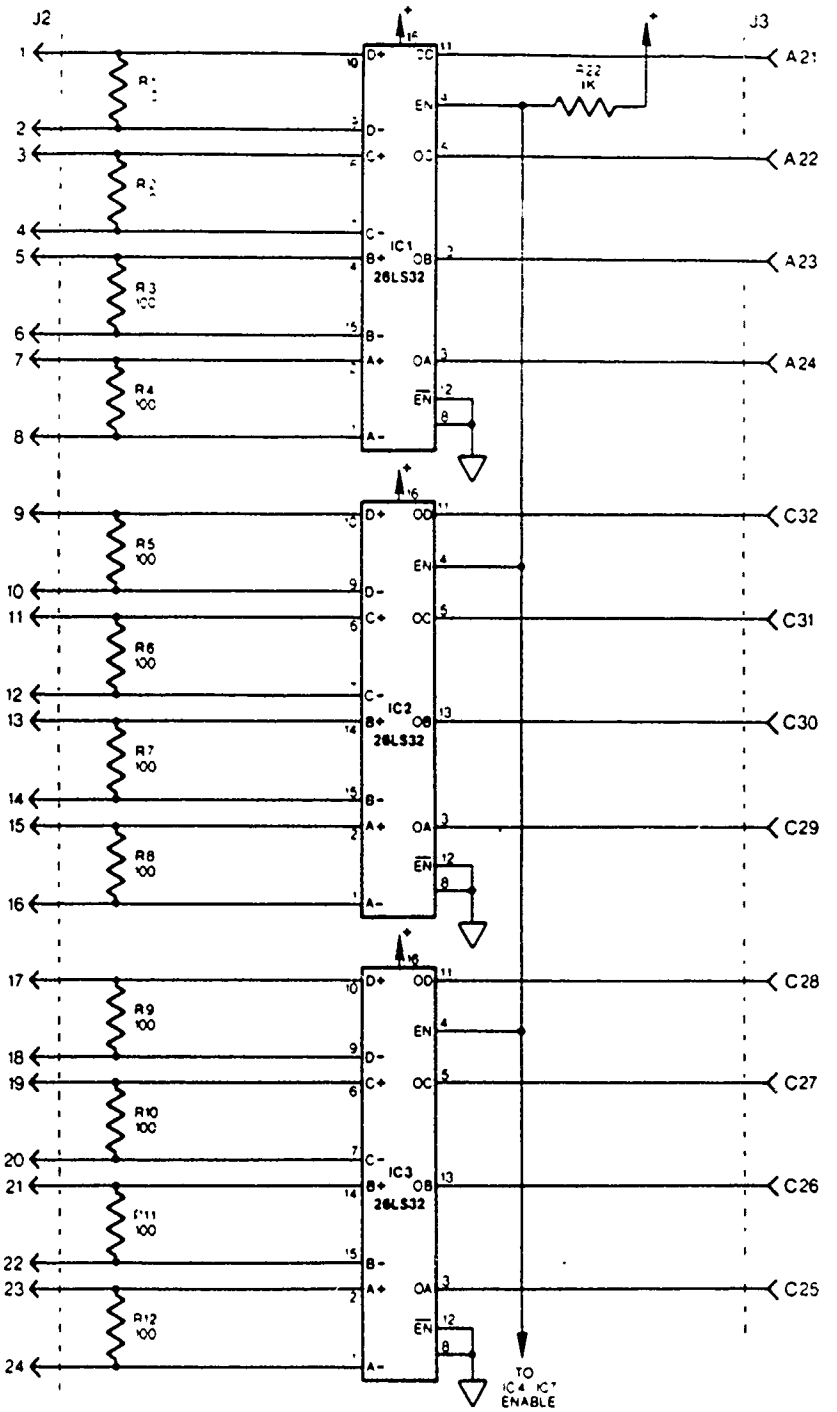
TITLE: RECEIVER CARD SCHEMATIC DIAGRAM (1 OF 2)				FILENAME: BLANK PLT	UDRI University of Dayton Research Institute (Electronic & Computer Development Laboratory)
FIGURE: 22a	SHEET 1 OF 2	DESIGNER: JMA	DRAWN BY: SPF	FILEDATE: 07 Jul 1989	
				FILETIME: 07 49 06	

Figure 22a: Receiver Card Schematic Diagram (1 of 2)



TITLE: RECEIVER CARD SCHEMATIC DIAGRAM (2 OF 2)				FILENAME: BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
				FILEDATE: 07-Jul-1989	
FIGURE: 22b	SHEET 2 OF 2	DESIGNER: JMA	DRAWN BY: SPF	FILETIME: 07 49 06	

Figure 22b: Receiver Card Schematic Diagram (2 of 2)



TITLE: 1PPR RECEIVER CARD SCHEMATIC DIAGRAM (1 OF 2)

FILENAME: BLANK PLT

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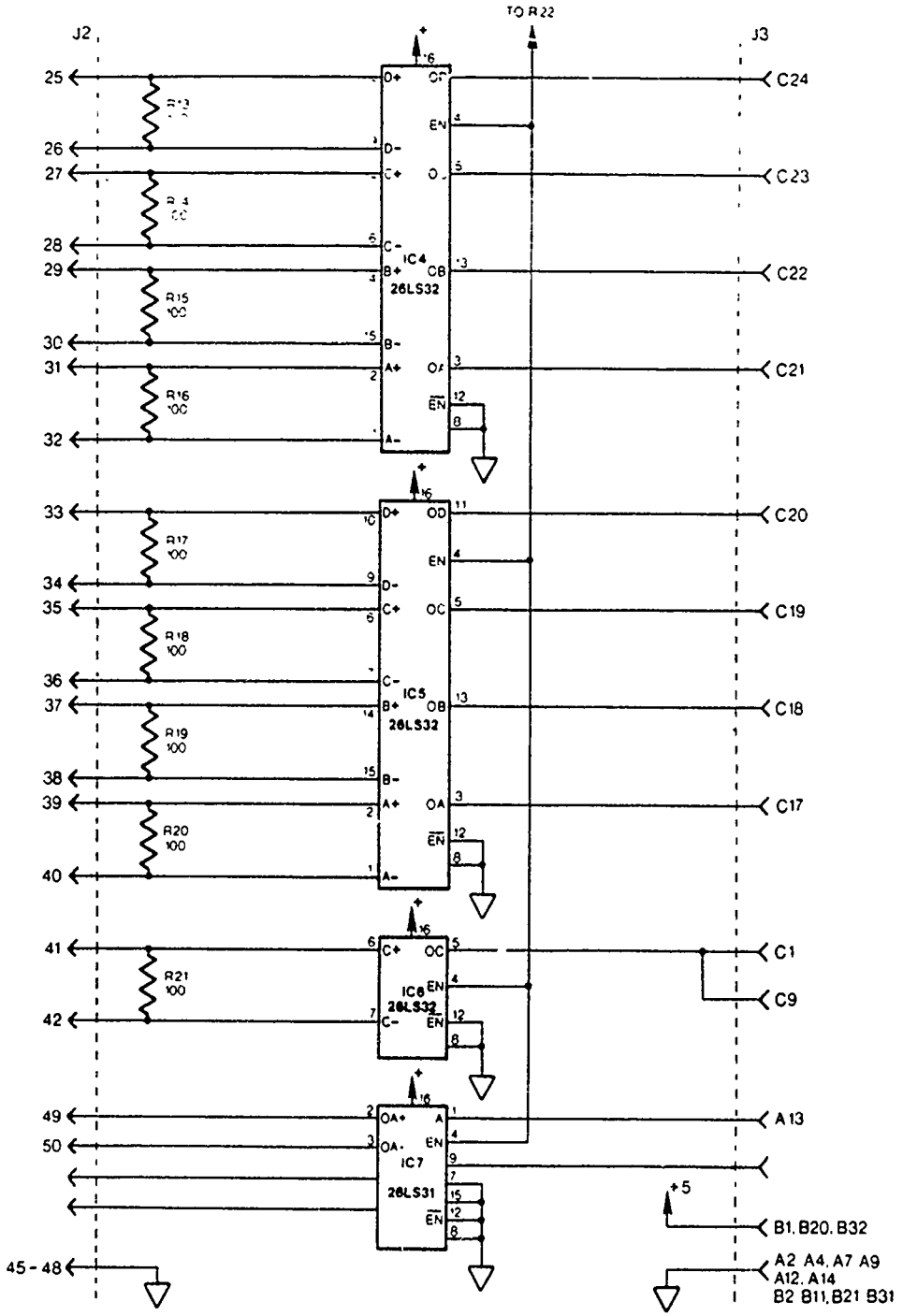
FIGURE 23a | SHEET 1 of 3 | DRAWN BY MA

Figure 23a: 1PPR Receiver Card Schematic Diagram (1 of 2)



TITLE: 1PPR RECEIVER CARD SCHEMATIC DIAGRAM (2 OF 2)				FILENAME: BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
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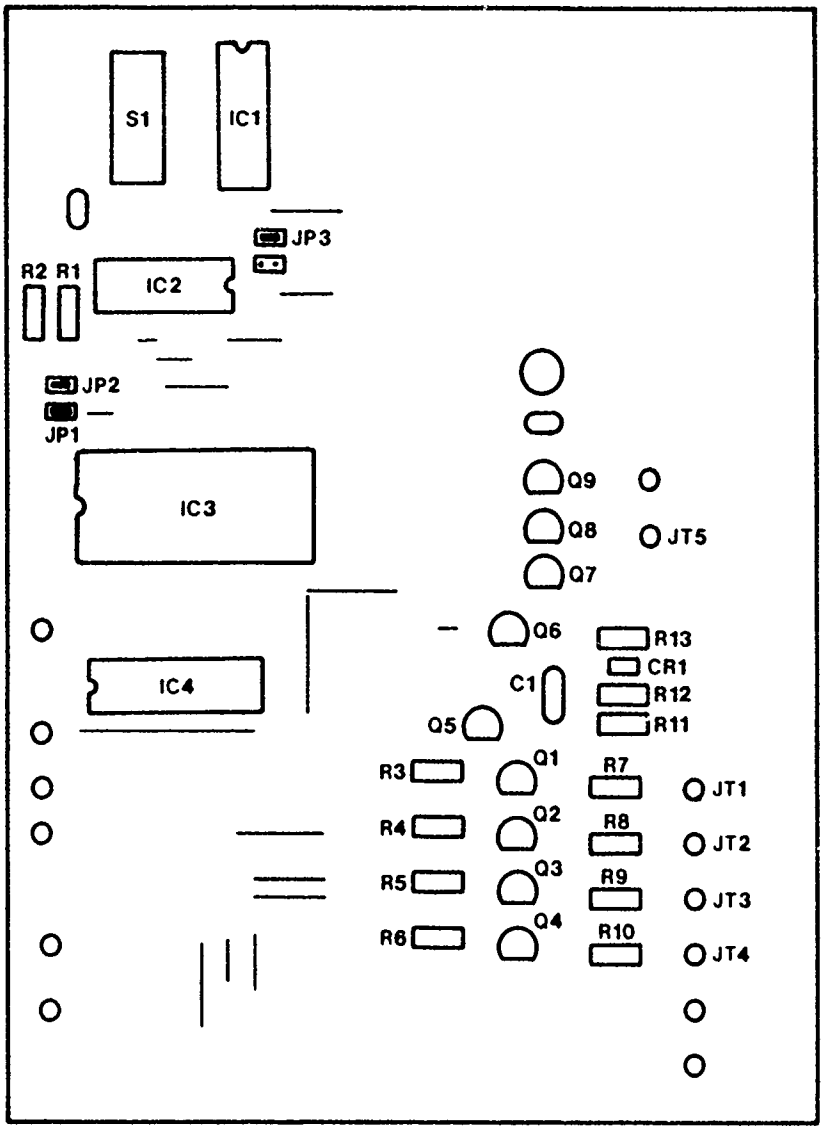
FIGURE: 23b	SHEET 2 OF 2	DESIGNER: JMA	DRAWN BY: SPF	FILETIME: 07 49 06	

Figure 23b: 1PPR Receiver Card Schematic Diagram (2 of 2)

Receiver and 1PPR Receiver Cards Parts List

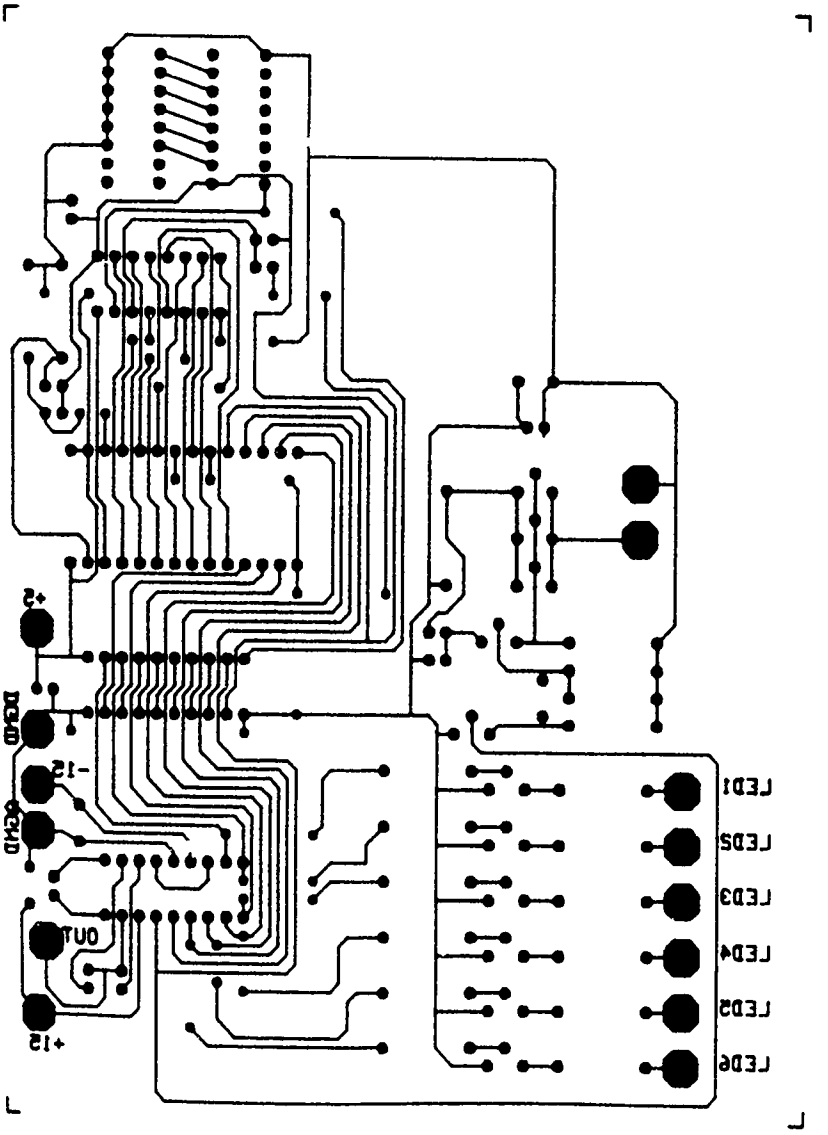
Part Number	Description
R1 - R21	100 Ohm
R22	1 KOhm
IC1 - IC6	Am26LS32
IC7	Am26LS31
J2	Ansley Blue Macs 50 pin male
J3	Ansley 64 Pin DIN VME

Table 4: Receiver and 1PPR Receiver Cards Parts List



TITLE: SIMULATOR BOARD COMPONENT LAYOUT				FILENAME: BLANK PLT FILEDATE: 07-Jul-1989	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE: 24	SHEET 1 OF 1	DESIGNER: JMA	DRAWN BY: SPF	FILETIME: 07 49 06	

Figure 24: Simulator Board Component Layout



TITLE: SIMULATOR BOARD ARTWORK			FILENAME: BLANK.PLT	UDRI University of Dayton Research Institute
FIGURE: 25	SHEET: 1 of 1	DESIGNER: JMA	DRAWN BY:	FILEDATE: [illegible]

Figure 25: Simulator Board Artwork

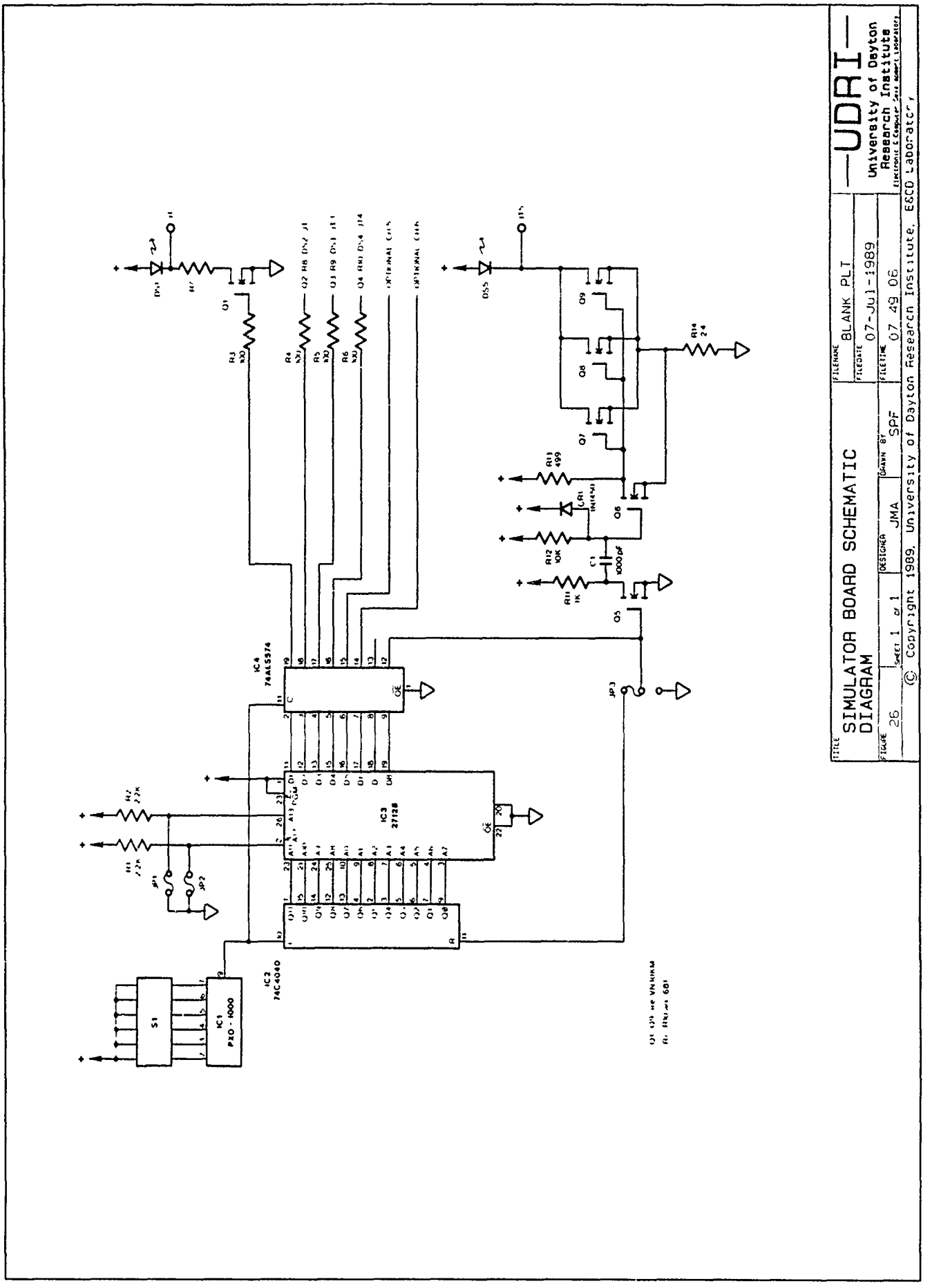


Figure 26: Simulator Board Schematic Diagram

Simulator Board Parts List

Part Number	Description
R1, R2	2.2 KOhm
R3 - R6	100 Ohm
R7 - R10	681 Ohm
R11	1 KOhm
R12	10 KOhm
R13	499 Ohm
R14	2.4 Ohm
C1	1000 pF
IC1	PXO-1000
IC2	74C4040
IC3	27128
IC4	74ALS574
Q1 - Q9	VN10KM
DS1 - DS5	LED
CR1	1N4150

Table 5: Simulator Board Parts List

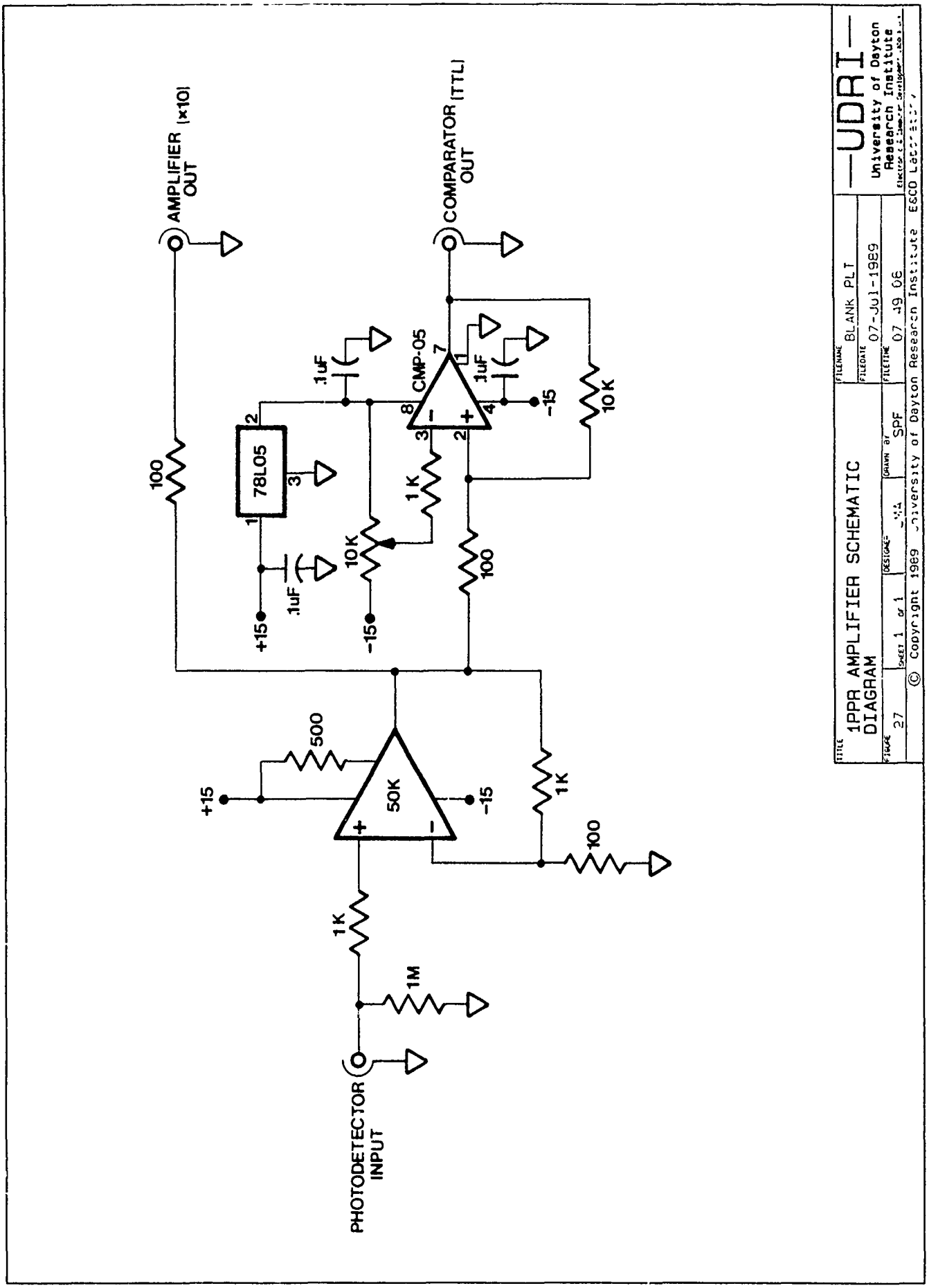


Figure 27: 1PPR Amplifier Schematic Diagram

TURBINE BLADE BACKPLANE

FRONT		CLOCK	CHAN 1	CHAN 2	CHAN 3	CHAN 4
1	INPUT	PHOTODIODE	PMT 1	PMT 2	PMT 3	PMT 4
2	ANA2	ANA GND	ANA GND	ANA GND	ANA GND	ANA GND
3	ANA3					
4	ANA4					
5	ANA GND	ANA GND	ANA GND	ANA GND	ANA GND	ANA GND
6	+15V	+15V	+15V	+15V	+15V	+15V
7	-15V	-15V	-15V	-15V	-15V	-15V
8	COMP EN	COMP EN	COMP EN	COMP EN	COMP EN	COMP EN
9	LATCH EN	LATCH EN	LATCH EN	LATCH EN	LATCH EN	LATCH EN
10	ERROR RESET	E RESET	E RESET	E RESET	E RESET	E RESET
11	ERROR	ERROR	ERROR	ERROR	ERROR	ERROR
12	DIG GND	DIG GND	DIG GND	DIG GND	DIG GND	DIG GND
13	+5V	+5V	+5V	+5V	+5V	+5V
14	CNT LATCH	CNT LATCH	CNT LATCH	CNT LATCH	CNT LATCH	CNT LATCH
15	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK	CLOCK
16	CLOCK/	CLOCK/	CLOCK/	CLOCK/	CLOCK/	CLOCK/
17	C23	COUNTER BIT 23	C23	C23	C23	C23
18	C22	COUNTER BIT 22	C22	C22	C22	C22
19	C21	COUNTER BIT 21	C21	C21	C21	C21
20	C20	COUNTER BIT 20	C20	C20	C20	C20
21	C19	COUNTER BIT 19	C19	C19	C19	C19
22	C18	COUNTER BIT 18	C18	C18	C18	C18
23	C17	COUNTER BIT 17	C17	C17	C17	C17
24	C16	COUNTER BIT 16	C16	C16	C16	C16
25	C15	COUNTER BIT 15	C15	C15	C15	C15
26	C14	COUNTER BIT 14	C14	C14	C14	C14
27	C13	COUNTER BIT 13	C13	C13	C13	C13
28	C12	COUNTER BIT 12	C12	C12	C12	C12
29	C11	COUNTER BIT 11	C11	C11	C11	C11
30	C10	COUNTER BIT 10	C10	C10	C10	C10
31	C9	COUNTER BIT 9	C9	C9	C9	C9
32	C8	COUNTER BIT 8	C8	C8	C8	C8
33	C7	COUNTER BIT 7	C7	C7	C7	C7
34	C6	COUNTER BIT 6	C6	C6	C6	C6
35	C5	COUNTER BIT 5	C5	C5	C5	C5
36	C4	COUNTER BIT 4	C4	C4	C4	C4
37	C3	COUNTER BIT 3	C3	C3	C3	C3
38	C2	COUNTER BIT 2	C2	C2	C2	C2
39	C1	COUNTER BIT 1	C1	C1	C1	C1
40	C0	COUNTER BIT 0	C0	C0	C0	C0

Table 6: Detector/Electronics Chassis Backplane Pinout

Simulator Connector Pinout

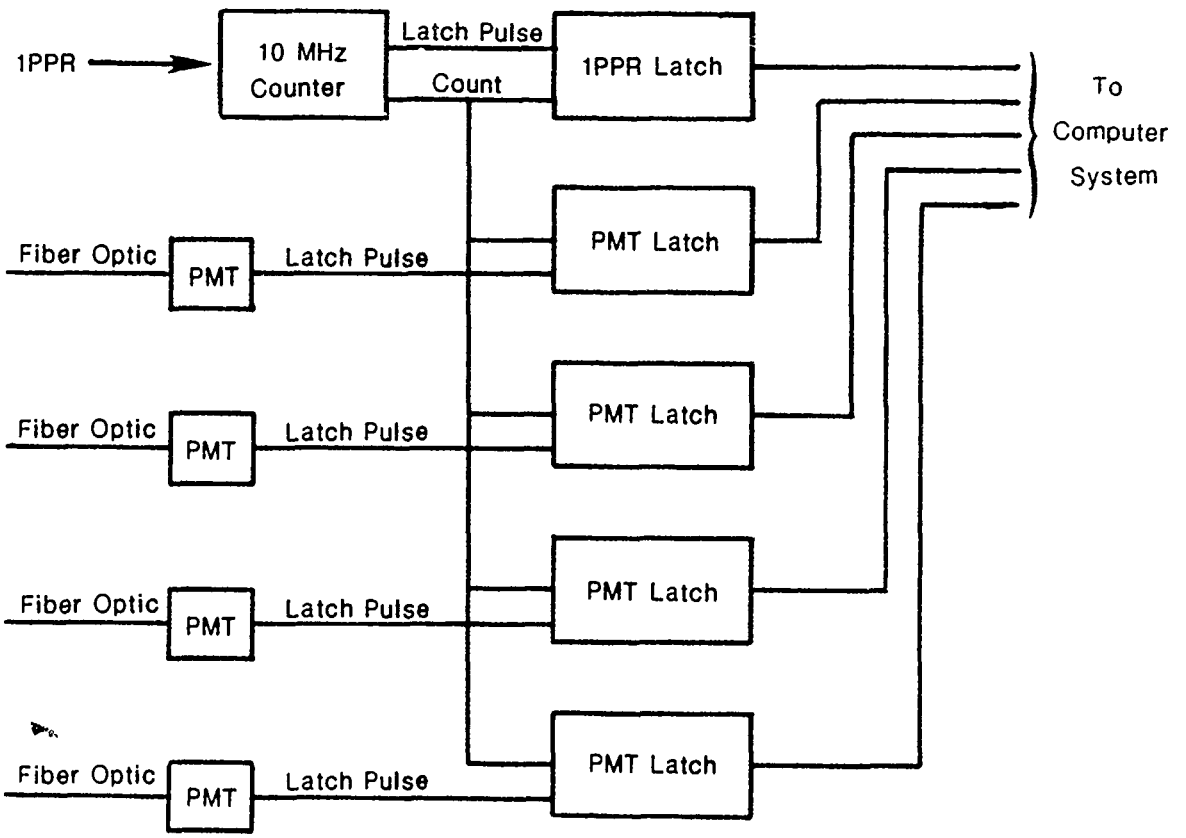
A	LED 1
B	LED 2
C	NC
D	LED 4
E	GND
F	1PPR LED
G	NC
H	GND
I	NC
J	GND
K	GND
L	NC
M	GND
N	LED 3

Table 7: Simulator Connector Pinout

RS-232 Connector Pinouts

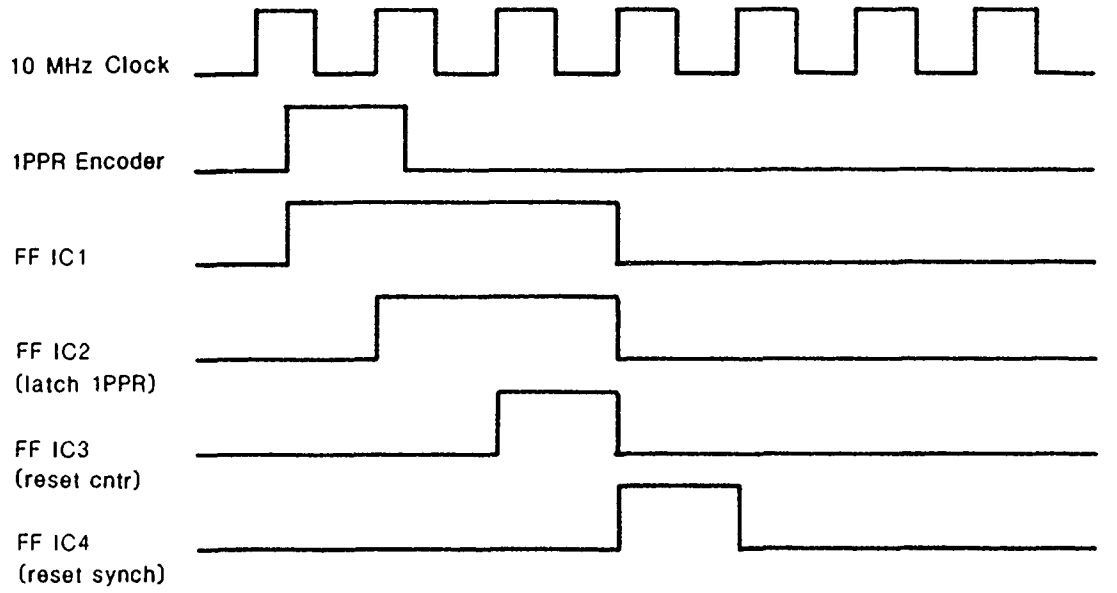
1	Shield
2	Transmit
3	Receive
4	NC
5	NC
6	NC
7	Signal Ground
8	NC
9	NC
10	NC
1	NC
12	NC
13	NC
14	NC
15	NC
16	NC
17	NC
18	NC
19	NC
20	NC
21	NC
22	NC
23	NC
24	NC
25	NC

Table 8: RS-232 Connection Pinouts



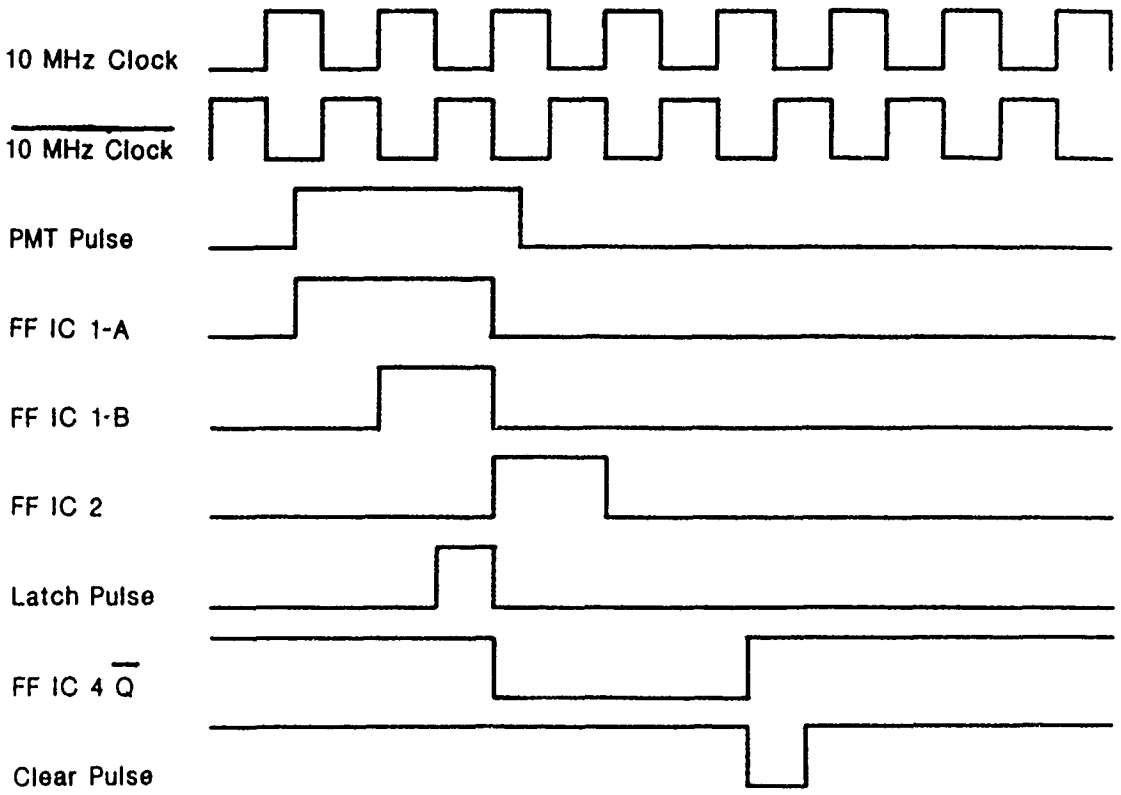
TITLE: DETECTOR/ELECTRONICS CHASSIS BLOCK DIAGRAM				FILENAME: BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
				FILEDATE: 07-Jul-1989	
FIGURE: 28	SHEET 1 of 1	DESIGNER: ECD	DRAWN BY: MJG	FILETIME: 07 49 06	

Figure 28: Detector/Electronics Chassis Block Diagram



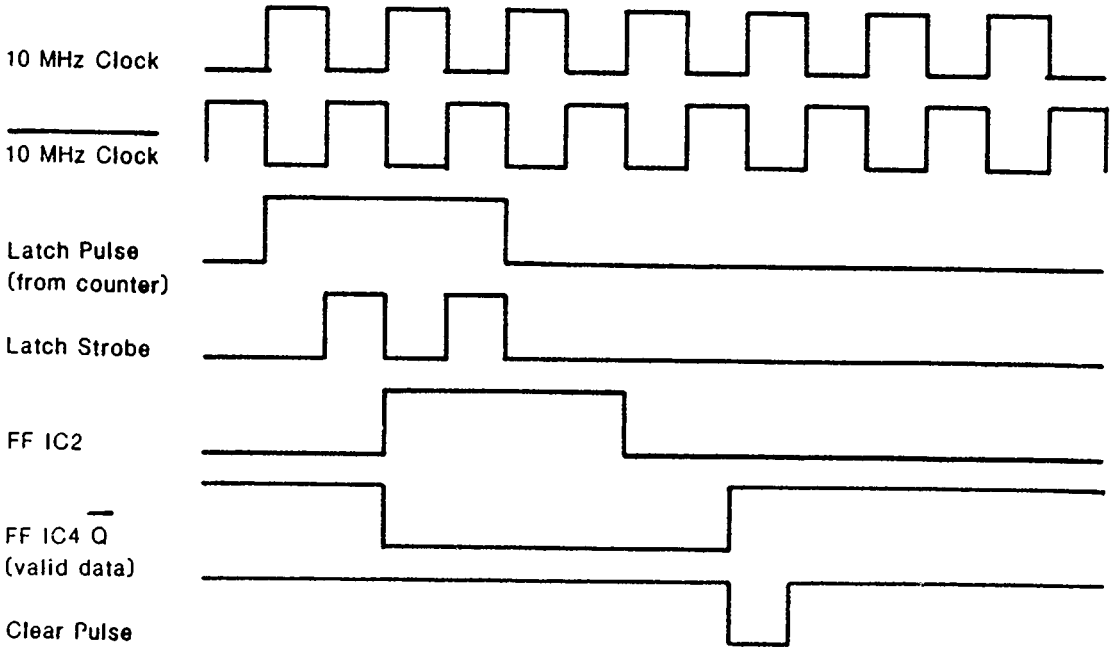
TITLE: COUNTER SYNCHRONIZATION TIMING DIAGRAM				FILENAME: BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
				FILEDATE: 07-Jul-1989	
FIGURE: 29	SHEET 1 OF 1	DESIGNER	DRAWN BY: MJG	FILETIME: 07 49 06	

Figure 29: Counter Synchronization Timing Diagram



TITLE: LATCH CARD TIMING DIAGRAM				FILENAME: BLANK PLT	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
				FILEDATE: 07-Jul-1989	
FIGURE: 30	SHEET 1 of 1	DESIGNER	DRAWN BY: MJG	FILETIME: 07 49 06	

Figure 30: Latch Card Timing Diagram



TITLE: 1PPR LATCH CARD TIMING DIAGRAM				FILENAME: BLANK PLT FILEDATE: 07-Jul-1989	UDRI University of Dayton Research Institute Electronic & Computer Development Laboratory
FIGURE: 31	SHEET 1 OF 1	DESIGNER	DRAWN BY: MJG	FILETIME: 07 49 06	

Figure 31: 1PPR Latch Card Timing Diagram

NSMS Data Acquisition System - Tape Format

Fixed length - 512 byte records

block 0

```
bytes   0..  3       : nb = number of blades
bytes   4..  7       : nr = number of revolutions
bytes   8.. 11       : ns = number of stations
bytes  12.. 15       : average speed
bytes  16.. 19       : minimum speed
bytes  20.. 23       : maximum speed
bytes  24..127       : unused
bytes 128..136       : run date (DD-MMM-YY)
bytes 137..141       : excitation frequency
bytes 142..149       : run time (HH:MM:SS)
bytes 150..165       : radius
bytes 166..245       : run description
bytes 246..261       : run id
bytes 262..421       : specimen description
bytes 422..437       : specimen id
bytes 438..511       : unused
```

nbrd = number blocks for rev data = int((nr + 127)/128)
nbbd = number blocks for blade data = int((nr*nb+127)/128)

block 1..nbrd

```
bytes 0..3           : rev 1 time for station 1
bytes 4..7           : rev 2 time for station 1
.
.
```

block nbrd+1..nbrd+nbbd

```
bytes 0..3           : rev 1 blade 1 time for station 1
bytes 4..7           : rev 1 blade 2 time for station 1
.
.
```

bytes nb*4-4..nb*4-1 : rev 1 blade nb time for station 1 bytes nb*4..nb*4+1 : rev 2 blade 1 time for station 1 .

.

repeat from block 1 for station 2, 3 and 4

tape mark

Table 9: Magnetic Tape Record Format

☆U.S.Government Printing Office: 1989 — 748-056/24065