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Interim Report
October 1989

SNEAK CIRCUIT ANALYSIS FOR THE COMMON MAN

SoHaR Incorporated

Jeff Miller

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Air Force Systems Command
Griffiss Air Force Base, NY 13441-5700

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This report presents the process known as sneak circuit analysis in a simple, easy to follow format. A listing of common design mistakes which led to sneak failures is given. This listing coupled with examples and descriptions of the design flaws, allow this document to be used not only to check an existing system, but more importantly, to correct a system in the design phase. This will save the expense of correcting a mistake discovered later in the development of a system.

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PREFACE

This report is an interim product of a two year study entitled Integration of Sneak Analysis with Design conducted by SoHaR Incorporated for the Rome Air Development Center, Griffiss AFB, NY, under contract F30602-87-C-0193. Technical direction for the stuoy, including this report on a simplified, manual procedure for sneak circuit analysis, has been provided by Mr. Bruce Dudley. The final report will include an automated version of the procedure.

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1. INTRODUCTION

Sneak circuits are unintended paths in a network that can cause undesirable actions. Sneak circuit analysis (SCA) is a procedure for avoiding these paths or detecting them. Rules, "clue lists" and semi-automated procedures have been developed to make SCA into a systematic activity. In the process, it has acquired the reputation of a "black art" which can only be practiced by specialists. This manual is an attempt to demystify the process and let the common man, such as a design engineer, perform SCA. This has the advantages of:

- advancing the conduct of the analysis to earlier design stages when changes to eliminate sneaks can be economically implemented
- insuring that problems have been correctly identified and solutions properly implemented
- providing insights into conditions that lead designers to sneak circuits so that in the future they can avoid the problems in the first place.

This manual is intended to be used as a circuit design guide for the design engineer to avoid commonly encountered sneak circuits and as a circuit analysis guide for the design engineer or reliability analyst to identify sneak circuits. It is not intended as a substitute for a conventional, comprehensive SCA procedure applied to a system late in the development cycle but instead serves as a simplified method for minimizing the occurrences of sneak circuits early in the design effort through application of the following items:

- Rules for avoiding sneak circuits during design.
- Guidelines for identifying sneak circuits at the functional level.
- Guidelines for identifying sneak circuits at the device level.

These aids are fully described in the remainder of this manual. The Sneak Circuit Design Rules are the most cost-effective of the three aids for addressing sneak problems and for this reason are emphasized by the procedure. It is far easier and less costly to avoid sneak circuits through proper design techniques than to identify and correct sneak circuits after the design has been completed.

Chapter 2 of this report briefly presents background material on conventional SCA covering its application, historical development, and deficiencies. The goal of overcoming these deficiencies motivated the development of the simplified SCA approach presented here. Instructions for applying this simplified procedure appear in Chapter 3. The design rules, functional guidelines and device guidelines are presented in chapters 4, 5 and 6, respectively. Suggestions for further reading, in addition to cited references, appear in the bibliography at the end of the report.

2. BACKGROUND

Sneak circuit analysis is defined in Mil-Std-785B, para. 50.2.3.2, as a procedure "to identify latent paths which cause occurrence of unwanted functions or inhibit desired functions, assuming all components are functioning properly," and is specified as Task 205 of that standard. The procedure has been in use for over 20 years, the first major computer aided version having been developed for the NASA Apollo program in 1967 by the Boeing Company [1]. The original application of SCA was for switching and relay networks for engagement and disengagement of control functions such as those used in automatic pilots and in missile and spacecraft systems. These applications are referred to as "electromechanical circuits" in MIL-STD-785B; in this report the shorter terms "switching circuits" or "relay circuits" are used (the two expressions are considered synonymous). The change in terminology also recognizes that relays are no longer exclusively electromechanical devices.

The primary objectives of SCA in switching circuit applications are to uncover sneak problems in four principal areas:

Sneak Paths	Unintended electrical paths within a circuit and its external interfaces.
Sneak Timing	Unexpected interruption or enabling of a signal due to switch circuit timing problems.
Sneak Indications	Undesired activation or de-activation of an indicator.
Sneak Labels	Incorrect or ambiguous labelling of a switch.

Because it was found that frequently encountered causes of sneak circuits were associated with distinct topological patterns on circuit diagrams, the identification of these patterns and the recording of specific circuit attributes applicable to each pattern were considered efficient means of using past experience to guide a current analysis. This conventional approach led to the development of semi-automated methods of isolating the topological patterns in relay circuits and to the generation of clue lists applicable to each type of topological pattern. The most significant of these patterns are the "Y" (power dome), inverted "Y" (ground dome), combined power/ground dome ("X"), and cross-tied paths ("H"). Examples of these are shown in Figure 1. Additional patterns covering analog and digital networks have also been developed.

A simple example of the conventional approach is demonstrated with the help of Figure 2. The functional circuit depicted in part A of the figure is intended to routinely open a cargo door unless the aircraft is not on the ground. For this reason, the primary switch that controls the door opening is energized through the Gear Down contactor. A secondary switch permits emergency operation of the door

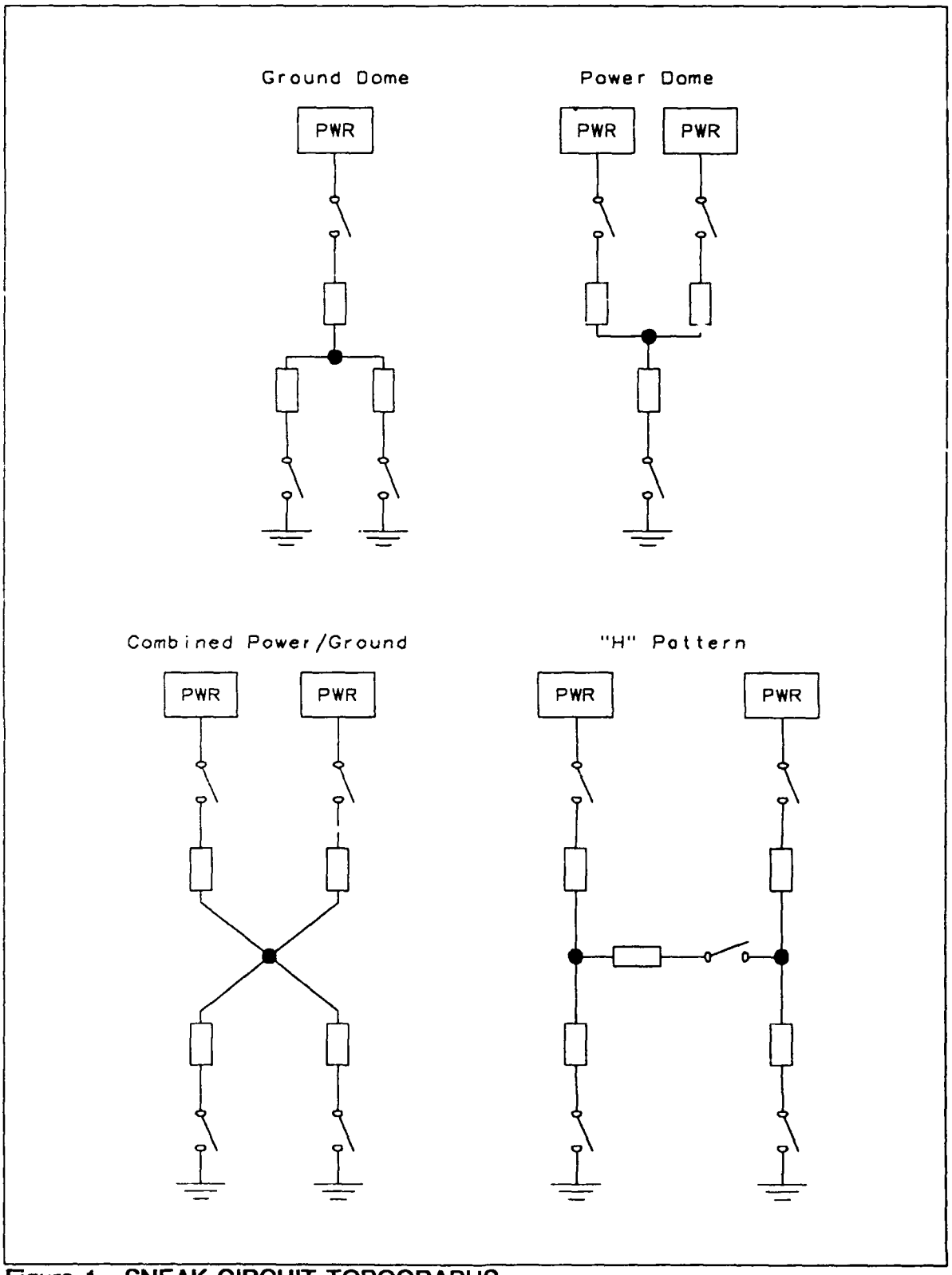

Figure 1. SNEAK CIRCUIT TOPOGRAPHS

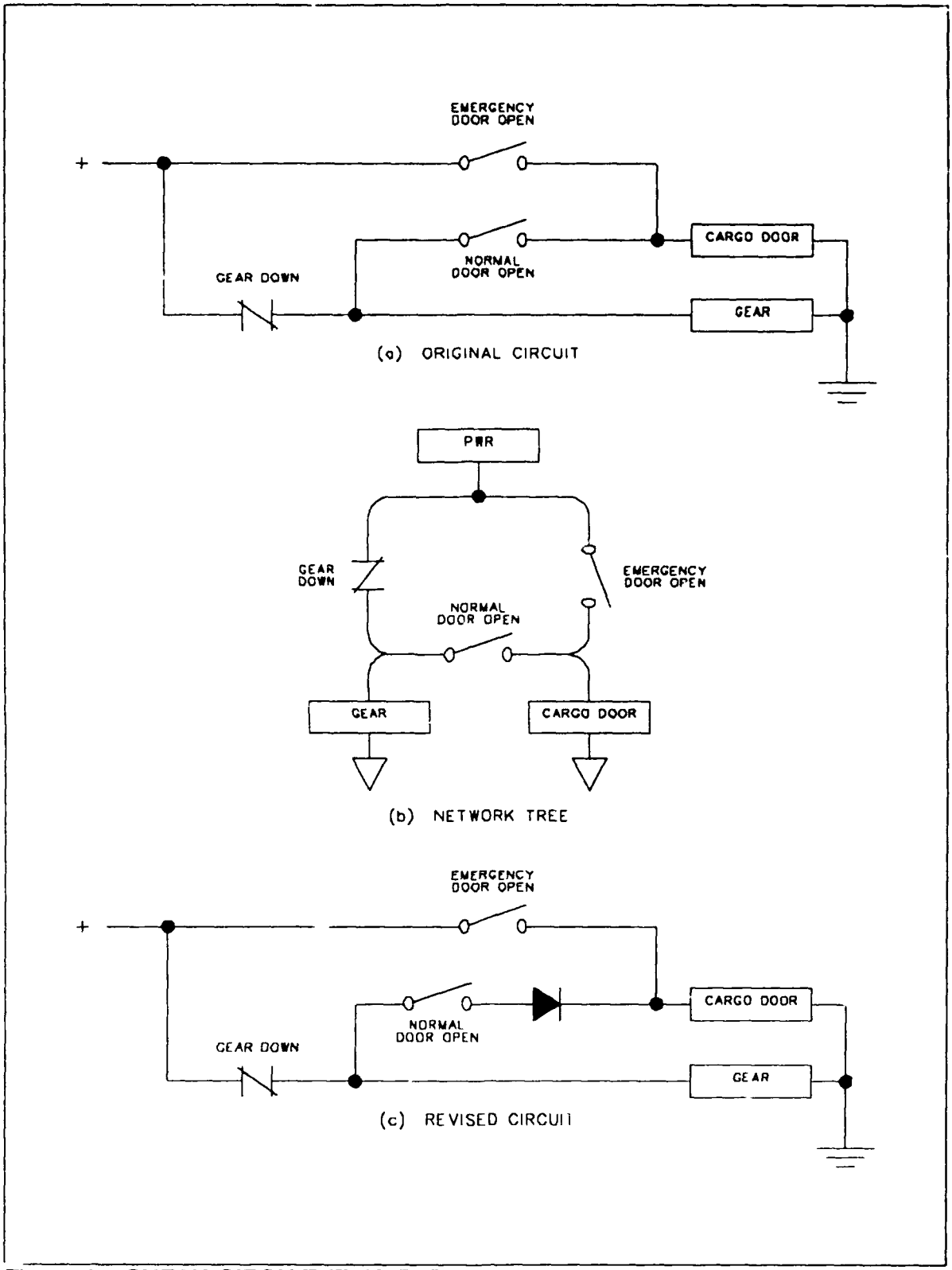

Figure 2. SNEAK CIRCUIT EXAMPLE

when the gear is not down. Due to a sneak path, closure of the emergency door switch when the primary switch is closed will inadvertently lower the landing gear.

In the conventional SCA approach, accurate, production-level drawings of the circuitry are required to insure all circuit paths are considered by the analysis. The circuit interconnection data are partitioned for constructing "network trees" to filter non-relevant schematic data and generate a visually simplified presentation of the circuit. Several versions of the trees may be required to analyze circuit switching configurations corresponding to specific timing sequences.

The topology of the network trees are analyzed for the appearance of the key patterns; for the cargo door example, an "H" pattern is recognized. The H pattern is more apparent from the network tree drawn in part B of Figure 2 than from the circuit schematic drawn in part A. Appropriate topologically oriented sneak clues are then applied to the pattern, and if an answer is affirmative, the sneak path is identified. It can be prevented by insertion of a diode in series with the primary switch as shown in part C of the figure.

The techniques for identifying sneak paths in switching or relay circuits are applicable to all functions that evaluate Boolean variables exclusively. Such circuits may comprise manual or sensor-operated switches, electromechanical or solid state relays, or combinatorial digital logic circuits (but not sequential or memory-dependent ones). The logic circuits are modeled by their switching circuit (switch and diode) equivalents. Functional paths such as those between relay coil and contact and between poles of a multiple pole switch are also modeled.

In recent years, the scope of SCA has been expanded to include clues for identifying design concerns in analog and digital circuitry. Some design concerns imply the existence of a sneak path or sneak timing while others are unrelated to sneak conditions and merely indicate a violation of good design practice. Design concern clues aid the analyst to identify potential problems affecting specific devices or circuit functions.

SCA is a highly labor intensive task requiring significant computer resources for support. For this reason, it is typically applied only to mission or safety critical areas of a system. The circuit interconnection data for these subsystems can be quite complex, with documentation spread over many drawings (e.g. circuit card schematics, inter-card wiring lists, and subsystem cabling diagrams). Automated techniques for capturing the circuitry and generating network tree interconnection data have been developed and have proved to be indispensable for efficient, accurate and thorough analysis of large systems. The software for performing the circuit data processing and tree generation is considered highly proprietary by those contractors that have developed an SCA capability. Furthermore, a team of specially trained analysts are required to apply sneak clue lists (many of the lists are considered highly proprietary) to the hundreds of network trees that are typically generated. For these reasons, performance of the analysis is limited to SCA contractors in all but the simplest of cases.

3. INSTRUCTIONS

The following instructions are provided for applying the Design Rules and Guidelines appearing in Chapters 4, 5 and 6. These aids primarily address power and ground distribution to analog and digital circuitry although some of the guidelines also address signal distribution. The aids are intended to be integrated with the circuit design effort early in the development process. Therefore, it is expected that the aids will be applied to a functional diagram or circuit schematic at the assembly (e.g. PC board) or subsystem (e.g. power distribution) level. The aids are applied to additional circuitry as the design progresses. For each application, it is important to account for all present or anticipated interfaces with other circuitry, particularly connections to sources of power and ground. If specific circuit paths are not defined at the time the aids are applied, represent these interfaces functionally and repeat the analysis when the interface definition becomes more refined. Specific instructions are as follows:

(1) During the early design phase follow the Sneak Circuit Design Rules found in Chapter 4. The rules are intended for the circuit designer during the concept and validation development phases. Adherence to these rules will avoid many common causes of sneak circuits.

(2) Apply the Sneak Circuit Functional Guidelines (Chapter 5) when functional diagrams are available at the subsystem level. The diagrams should depict power and ground distribution paths and power switching elements. The remaining functions can be depicted as power supply loads. For complex systems, focus the application of the rules on circuitry associated with critical system functions rather than attempt to analyze the entire system. Critical functions, for example those affecting loss of life or destruction of the system, may be identified by fault tree analysis or functional FMEA.

(3) Apply the Sneak Circuit Device Guidelines (Chapter 6) when the design has progressed to where circuit schematics are available at the assembly (i.e. circuit board) level. The schematics must include all power and signal paths, including connections across subsystem interfaces. Again, the extent of the analysis can be reduced by limiting it to the critical areas of the system.

4. SNEAK CIRCUIT DESIGN RULES

The Sneak Circuit Design Rules guide the circuit designer to avoid networks commonly associated with sneak conditions. Each rule is formatted as follows:

a. PROBLEM -- A statement of the sneak problem addressed by the rule.

b. SOLUTION -- a recommended approach for implementing the rule in practical situations.

c. Figures depicting circuitry violating and complying with the rule.

d. Supplementary information further explaining the rule.

The following is a selection guide for application of the design rules:

RULE	APPLICABLE CIRCUITRY	PAGE
1	Power distribution from two or more sources of power and/or ground	8
2	Power distribution with ground-side current interruption other than connectors	9
3	Power distribution with ground-side current interruption including connectors	10
4	Power connectors	11
5	Power distribution to two or more loads	12
6	Power distribution from two or more sources of power to essential loads (particularly volatile computer memory)	13
7	Manually controlled switching devices	14

Rule 1. MULTIPLE POWER SOURCES AND RETURNS

PROBLEM: Sneak paths involving multiple power sources and/or multiple ground returns.

SOLUTION: Structure circuits so that all current for a given load flows from one power source to one ground return. Where this is not possible, isolate power sources using diodes for DC power or relays (electromechanical or solid-state) for AC or DC power. Use Schottky diodes or relays for DC applications requiring very low voltage drop and power dissipation. Isolate returns by separating high and low current loads.

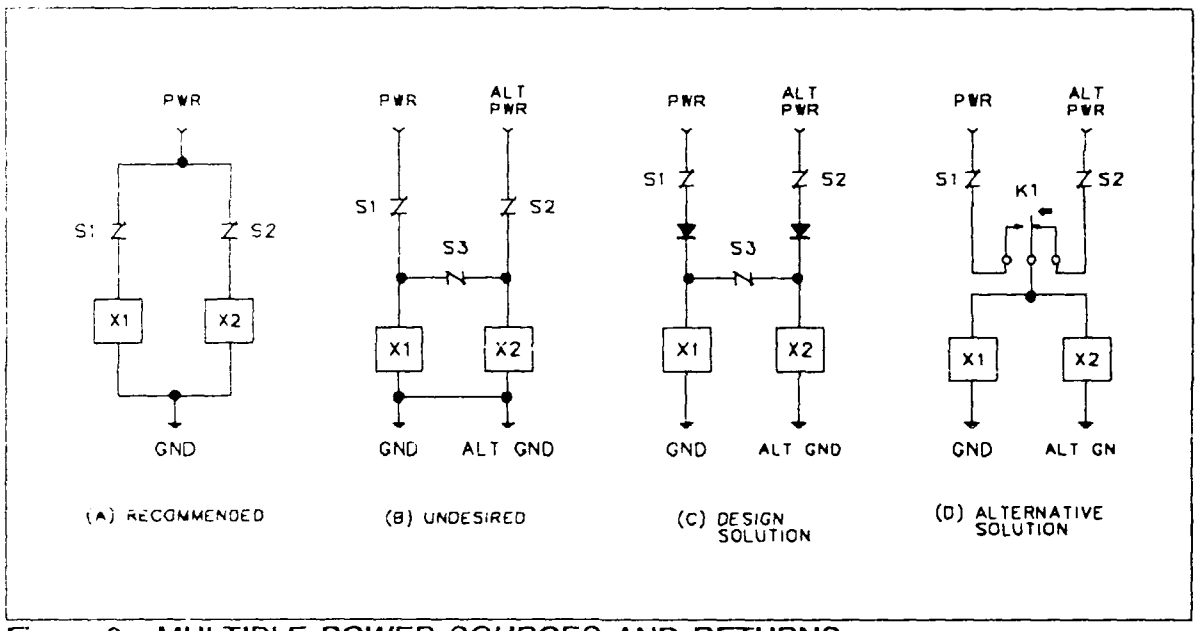

Figure 3. MULTIPLE POWER SOURCES AND RETURNS

Adherence to this rule avoids "Y," "X" and "H" circuit patterns associated with multiple power sources and sinks (see Chapter 2). This is a general rule to be followed wherever possible. An example of a network complying with this rule appears in Figure 3A, and an example of a network violating it appears in part B of the figure. The violations shown can result in power-to-power or ground-to-ground ties. Isolation must be provided to avoid the mixing of low current and high current ground returns. Examples are shown in parts C and D of the figure.

Rule 2. GROUND SIDE SWITCHING

PROBLEM: Sneak paths caused by interrupting current at the ground side of a load.

SOLUTION: Do not place current interrupting elements (e.g. switches, relays, circuit breakers, fuses) in ground return paths. If connectors are required, apply Rule 3.

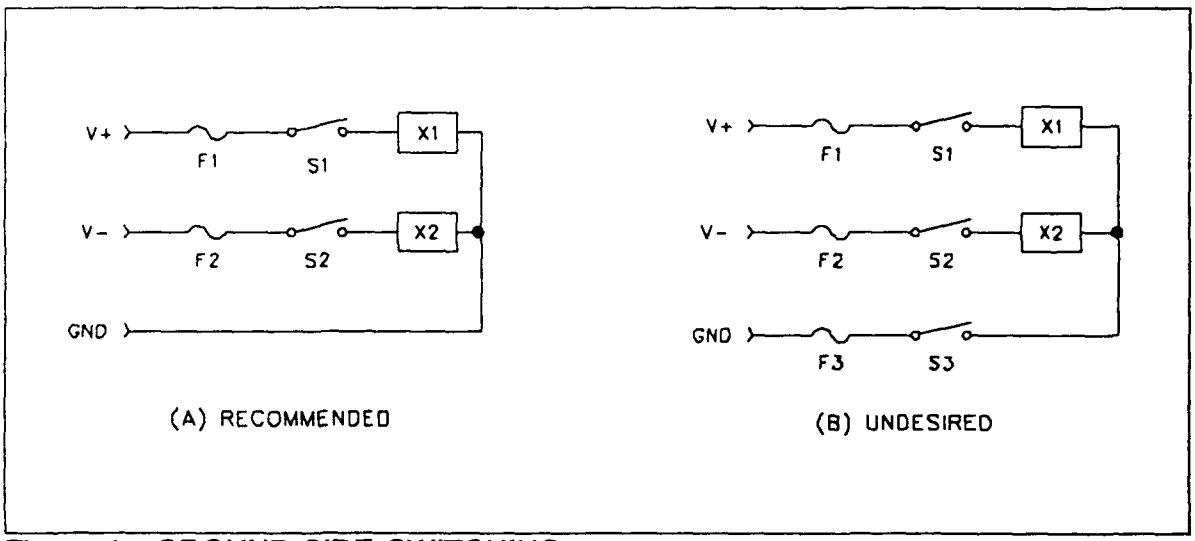

Figure 4. GROUND-SIDE SWITCHING

An arbitrary number of current interrupters (switches, relays, connectors, fuses, circuit breakers, etc.) can be placed on the supply side of the load without danger of causing reverse current flow. However, placement of switches on the ground side of the load can under some conditions cause a sneak circuit. The placement of switches on the ground side of loads is an undesirable practice (it is prohibited in most circumstances in the National Electrical Code), but connectors on the ground side may be necessary and can in principle cause the same sneak circuit.

An example of problems caused by ground-side switching is shown in Figure 4. In part A, loads X1 and X2 are powered respectively from positive and negative DC voltage supplies. In part B, if fuse F3 opens before F1 and F2 or if pole S3 opens before S1 and S2, a voltage equal to sum of V+ and V- will be distributed across the loads according to the ratio of their impedances for the duration of this condition.

Rule 3. CIRCUIT SYMMETRY

PROBLEM: Sneak paths caused by connectors (or other current interrupting devices) located on the ground side of a load.

SOLUTION: When placement of a connector at the ground side of the load is required, keep the supply and ground return paths symmetrical.

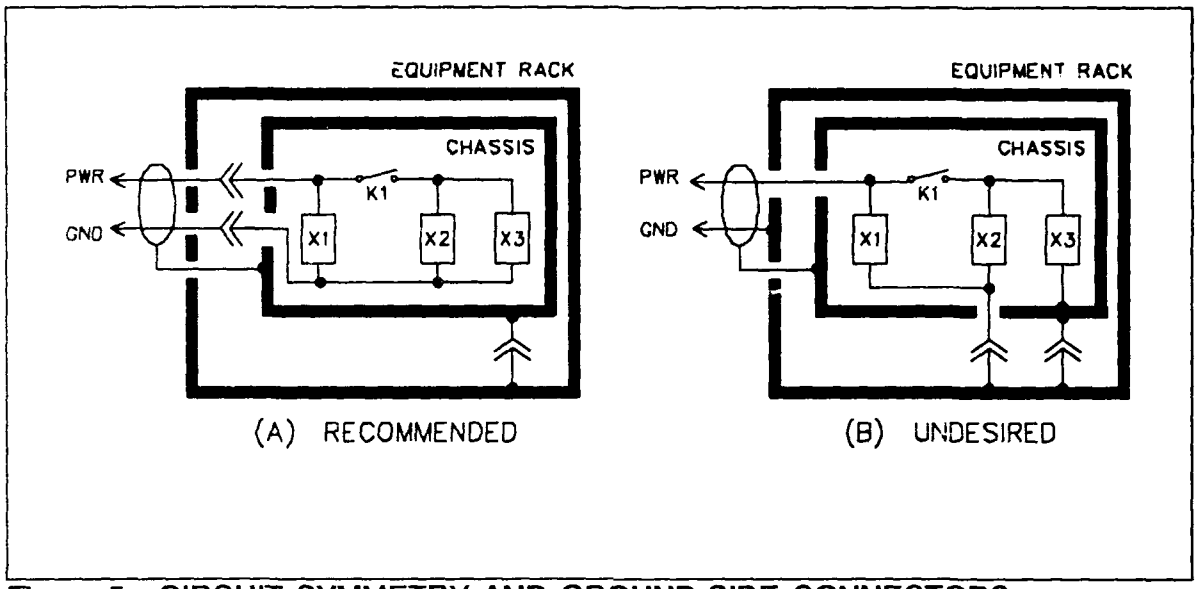

Figure 5. CIRCUIT SYMMETRY AND GROUND-SIDE CONNECTORS

The switching topology from the supply to a load should be duplicated from the load to ground. A "duplicated topology" implies identical branching but not necessarily the same number or type of switching elements per branch. Adhering to this rule will avoid inadvertent, topological H-patterns that are a common source of reverse current flow. A practical equipment configuration is shown in Figure 5. In part A of that figure all ground return paths share the same connector with the power source line. In part B loads X1 and X2 are directly connected to the equipment rack ground and the return for X3 is connected to the chassis ground to which the cable shield is also attached. The sneak path occurs when the equipment is powered up with contactor K1 open, and the chassis removed from the rack. The latter condition is frequently encountered during troubleshooting or when performing depot level maintenance. Sneak current flows from the power input through X1, through X2 in the reverse direction, through X3 and returns through the power cable shield. If the loads represent a low impedance, the current through the shield can reach sufficiently high values to cause excessive heat and in extreme cases fire. An important area of concern is possible latent damage due to the reverse current flow through X2 and the heating of the wire(s) surrounded by the shield.

Rule 4. POWER AND GROUND CONNECTORS

PROBLEM: Sneak paths caused by power and ground connectors.

SOLUTION: Avoid the use of separate connectors for providing power and ground return lines to a circuit.

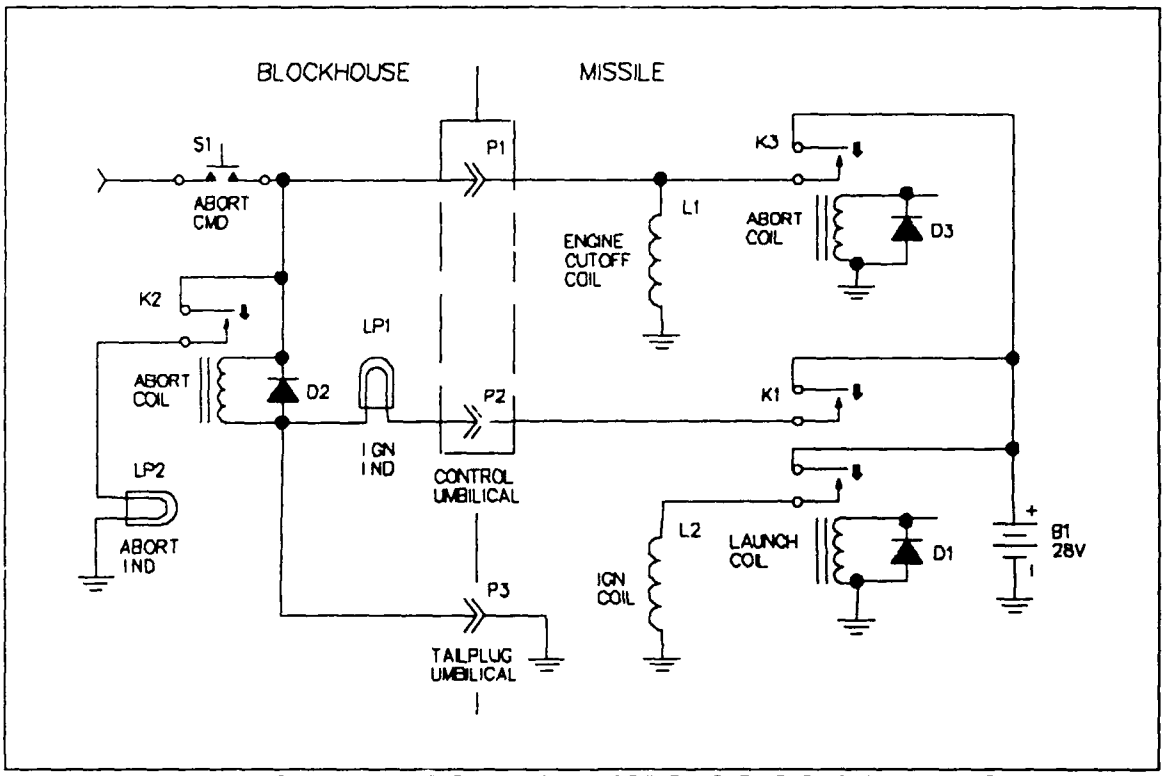

Figure 6. UNDESIRABLE CONSEQUENCES OF SEPARATE POWER AND GROUND CONNECTORS

The design solution for this rule occurs as a consequence of adhering to the symmetry rule (Rule 3) but is important enough to merit special consideration. Adherence to this simple rule would have prevented the Mercury-Redstone launch failure described in reference [1]. This is illustrated in Figure 6 which depicts the portion of the blockhouse and missile circuitry involving the sneak. As shown in the figure, the normal sequence of events is for launch command relay K1 to be triggered, enabling battery B1 to power the missile ignition coil and the blockhouse ignition indicator. However, if upon launch the tail plug umbilical carrying ground return P3 separated before the control umbilical, current flowing through the ignition indicator would continue through diode D2 and supply power to the engine cutoff coil. This sequence of events actually did occur. It could have been prevented by routing the power and return lines through the same connector.

Rule 5. WIRED-OR CIRCUITS

PROBLEM: Sneak paths caused by selecting alternate paths in "wired-OR" circuits.

SOLUTION: The "wired-OR" can be used only where the effect to be produced by the alternate conditions is exactly the same. When some conditions are intended to cause additional or modified effects, isolation must be provided.

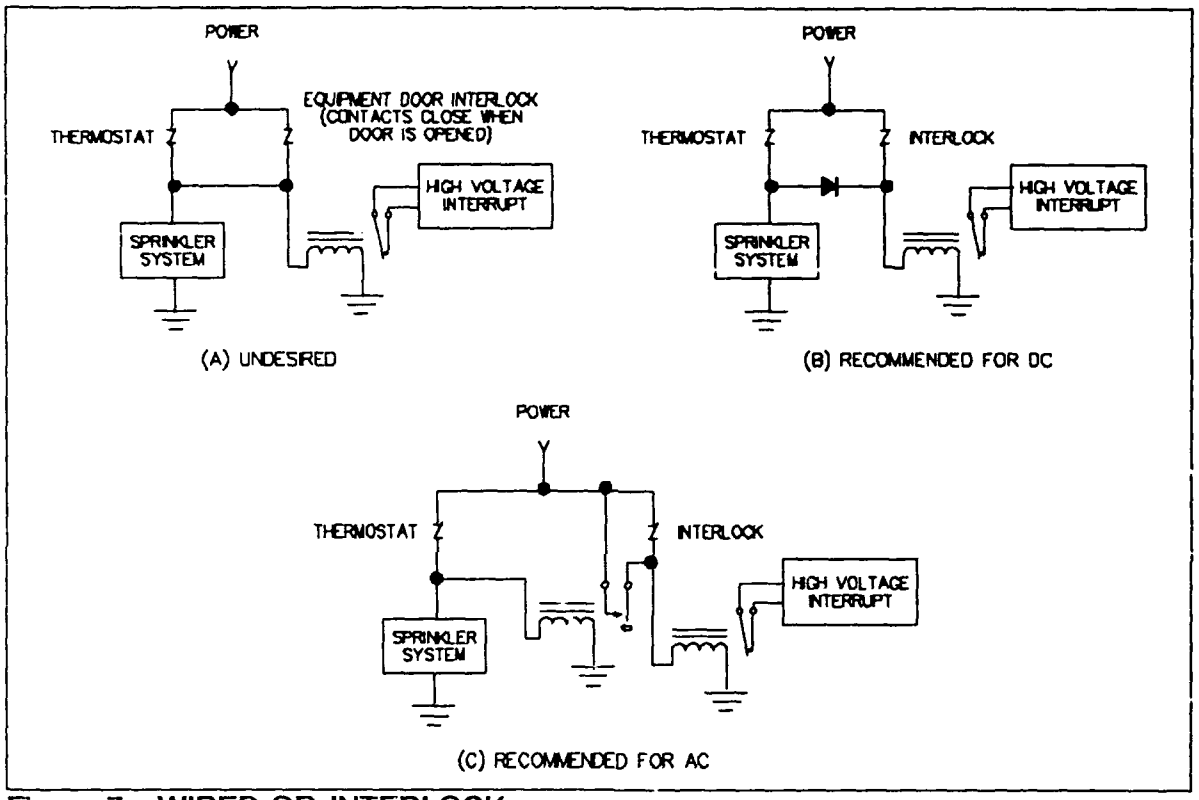

Figure 7. WIRED-OR INTERLOCK

This problem is frequently encountered in alarm and interlock circuits. A simple example is that of an interlock actuated by two or more conditions, as shown in Figure 7. A high voltage power supply is to be interrupted when either the equipment door is opened or when the ambient temperature exceeds a preset level. The temperature sensor is also intended to operate an automatic sprinkler system. In the implementation shown in Figure 7A, opening the equipment door will interrupt the high voltage as intended, but it will also unintentionally turn on the sprinkler system. If the protective circuit operates on DC the sneak path can be eliminated by the addition of a diode in the horizontal branch as shown in part B of the figure. If the circuit utilizes AC, or if the diode is not desired for other reasons, a relay having a normally open contact arrangement is added as shown in part C of the figure.

Rule 6. SNEAK TIMING IN MEMORY POWER SWITCHING

PROBLEM: Sneak timing due to momentary loss of power to volatile computer memory and other essential loads during switch-over to an alternate power source.

SOLUTION: For small memories, use break-before-make switching and sufficient capacitance to maintain the voltage during switch-over. For large memories or to protect against a short on the main supply, use make-before-break switching and diode isolation.

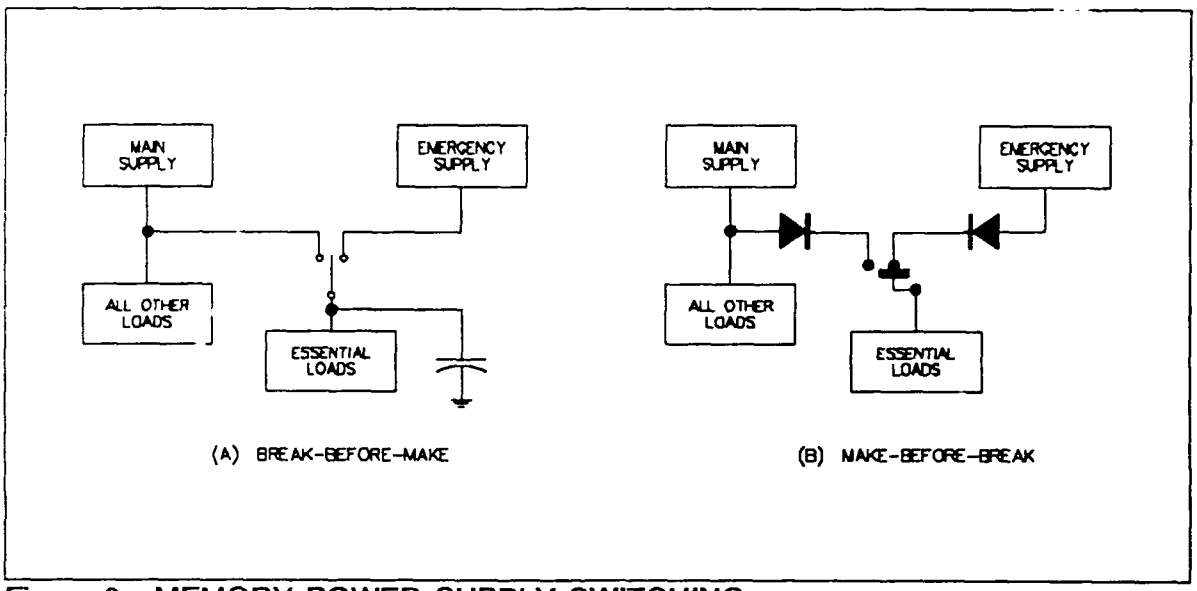

Figure 8. MEMORY POWER SUPPLY SWITCHING

This rule involves inappropriate selection of a break-before-make or make-before-break switch contact arrangement. As shown in Figure 8, an essential load is normally connected to the main supply but can be switched to an auxiliary supply when the main voltage drops below a set threshold. The implementation of Figure 8A uses break-before-make contacts and will subject the essential load to a brief power interruption. This interruption can cause complete or partial loss of all data stored in a volatile computer memory. If a computer is included in the sensitive load, protection against data loss must be provided. Where the computer memory is comparatively small, a capacitor across the memory power supply (Figure 8A) may be sufficient to maintain the voltage at a safe level during the switching interval when the break-before-make configuration is used. If this will not be adequate, the make-before-break switch must be used (Figure 8B) with further isolation of the non-essential load (either by diode or fast-acting switch) to protect against the case where the drop in the main voltage was due to a short circuit in the main supply or in the non-volatile load.

Rule 7. SWITCH LABELING

PROBLEM: Sneak label causing an action opposite to the one intended to occur when a switch is toggled.

SOLUTION: Label switches according to the action performed in addition to the object being controlled.

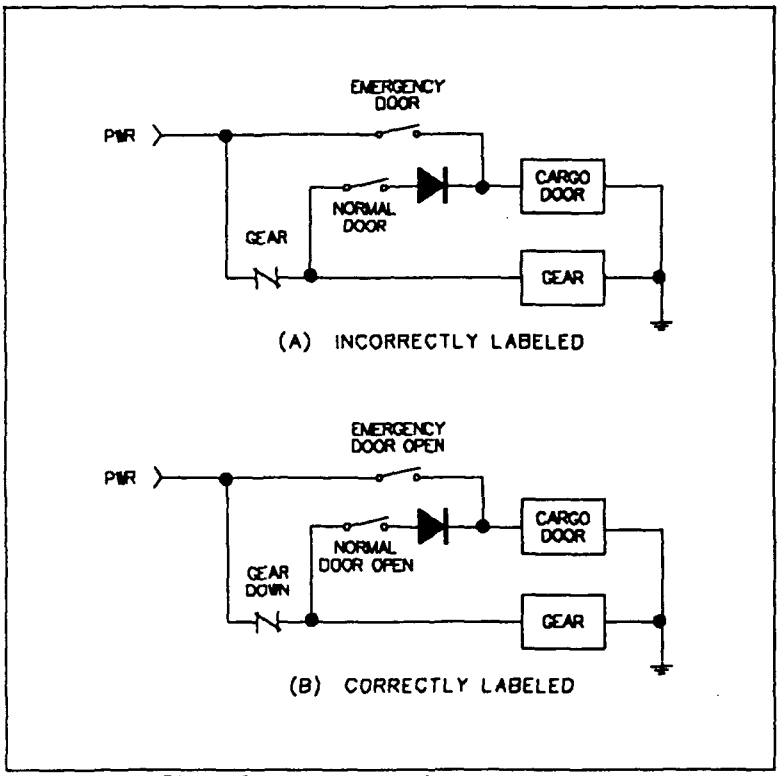

Figure 9. SWITCH LABELING

In Figure 9A, the labels EMERGENCY DOOR, NORMAL DOOR and GEAR are ambiguous as to whether closure of their corresponding switches occurs for "door open" or "door closed" or for "gear up" or "gear down". This ambiguity is eliminated by the labels shown in Figure 9B.

5. SNEAK CIRCUIT FUNCTIONAL GUIDELINES

The Sneak Circuit Functional Guidelines aid the circuit designer or reliability analyst to identify functional networks commonly associated with sneak conditions. Each guideline is formatted as follows:

a. TARGET -- The types of circuit functions targeted by the guideline.

b. PROBLEM -- A statement of the sneak problem addressed by the rule.

c. SOLUTION -- A recommended approach for implementing the rule in practical situations.

d. COMMENT -- Supplementary information further explaining the rule, in some cases accompanied by a figure.

The following is a selection guide for application of the functional guidelines:

APPLICABLE CIRCUITRY	PAGE
Power distribution	16
Power switching for multiple loads	23
Digital circuitry	25
Signal labeling	28
Indicators and drive circuitry	28

POWER DISTRIBUTION CIRCUITS

TARGET: Primary and secondary power distribution circuitry comprising power sources, ground returns, switches, contactors, relays, circuit breakers, fuses, solid state switches, connectors.

PROBLEM: Asymmetrical pattern of connections for power distribution and ground return circuitry.

SOLUTION: Use the same circuit connection topology for the supply side and ground side of a load. Use the same connector for symmetrical power and ground connections.

COMMENT: Circuit connection symmetry for power and ground distribution implies an identical number and location of power and ground connections feeding a load. Asymmetrical connections can cause sneak paths as shown in Figure 10. In part A of the figure, power connection J3 has no counterpart on the ground side of load X2. If connections J2 and J3 are open while the remainder are closed, current can unintentionally flow in the reverse direction through X2. This problem has been eliminated in part B of the figure by the inclusion of connection J3-2.

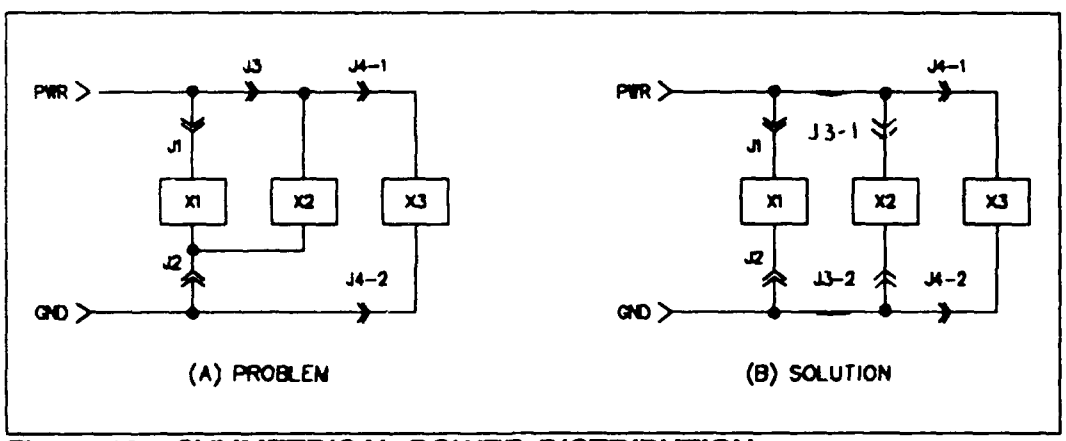

Figure 10. SYMMETRICAL POWER DISTRIBUTION

TARGET: Primary and secondary power distribution circuitry comprising power sources, ground returns, switches, contactors, relays, circuit breakers, fuses, solid state switches, connectors.

PROBLEM: Power-to-power tie between supplies providing power to a common load.

SOLUTION: For DC power, add diodes to isolate the supplies. For AC power or as an alternative for DC power, use a double-throw relay or switch having a break-before-make contact arrangement to select either supply, and provide adequate capacitance at the load to hold up the supply voltage during switch-over.

COMMENT: Referring to part A of Figure 11, PWR 1 and PWR 2 will be tied if switches S1 and S2 are simultaneously engaged. A make-before-break switch contact arrangement can cause a momentary power tie of this type. Part B shows the addition of isolation diodes. Schottky diodes can be used to minimize the diode voltage drop. Part C depicts the use of a single-pole, double-throw relay.

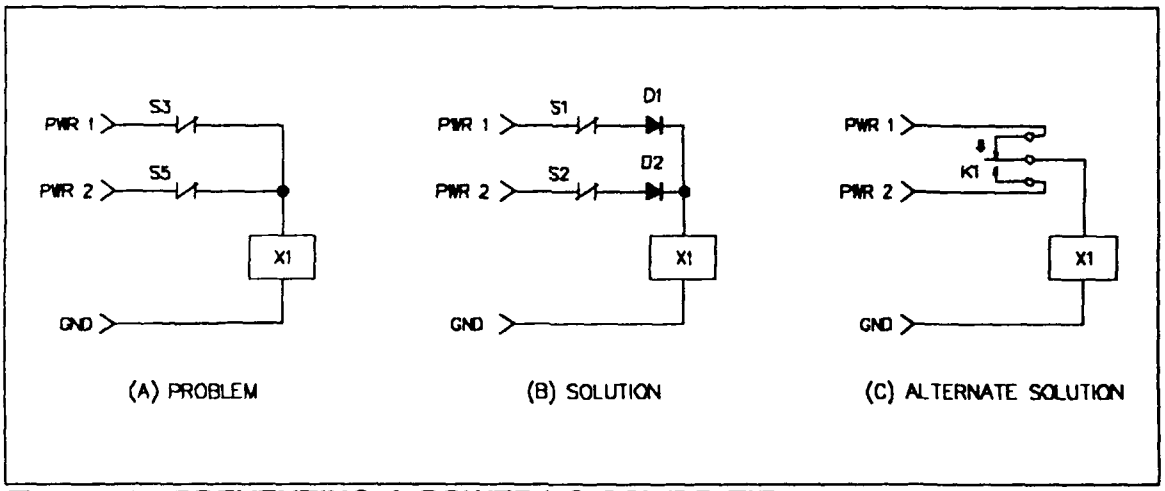

Figure 11. PREVENTING A POWER-TO-POWER TIE

TARGET: Primary and secondary power distribution circuitry comprising power sources, ground returns, switches, contactors, relays, circuit breakers, fuses, solid state switches, connectors.

PROBLEM: Power-to-power path between supplies providing power to loads sharing a common, independently switchable ground.

SOLUTION: Do not place switching elements other than those associated with circuit connections on the ground side of a load. For circuit connections, combine power and ground connections in the same connector.

COMMENT: The problem is two-fold. As can be seen from part A of Figure 12 below, loss of ground causes (1) a reverse current to flow through the load connected to the lower of the two supplies, and (2) the power-to-power voltage will divide according to the ratio of the load impedances, and the resulting voltage will appear on the ground side of the loads, presenting a potential safety hazard to personnel. The solution follows as a consequence of adhering to the general circuit symmetry guideline depicted in Figure 10. In part B of Figure 12, power and ground connections are combined in the same connector, thereby preventing loss of ground without loss of power.

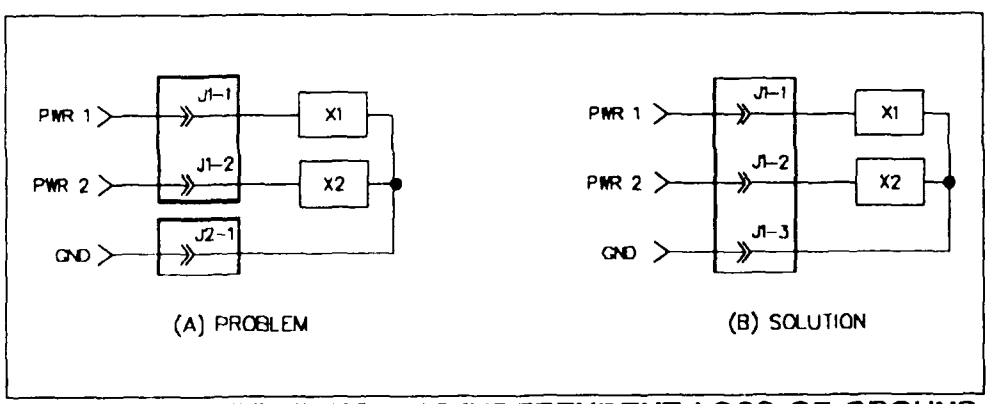

Figure 12. PREVENTING THE INDEPENDENT LOSS OF GROUND

TARGET: Primary and secondary power distribution circuitry comprising power sources, ground returns, switches, contactors, relays, circuit breakers, fuses, solid state switches, connectors.

PROBLEM: **Multiple supplies unintentionally enabling a shared load.**

SOLUTION: **Analyze the logic and timing of the power control circuitry to insure that all power sources sharing a common load are switched off when the load must be disabled.**

COMMENT: This problem can occur when supplies are OR'd (tied through diodes) as depicted earlier in Figure 11 or when supplies power a common system as depicted in Figure 13. In the latter, a low voltage power supply (LVPS) and a high voltage power supply (HVPS) provide DC power to a CRT display system. In part A of the figure, circuitry is provided to shutdown the LVPS in the event of an over-voltage or over-current condition at the power supply output. However, the protection circuitry does not shut down the HVPS. This can result in possible damage to the CRT screen (as the LVPS shuts down, the screen can be burned if the CRT deflection drives collapse before the video drive) and can also present a potential maintenance hazard (the absence of low voltage power may lead one to erroneously assume that all power is shut off).

Solutions to this problem are shown in parts B and C of Figure 13. In part B, the HVPS is provided with a fast shutdown function activated by the shutdown signal from the LVPS. In part C, the HVPS is replaced with one that is powered from the low voltage DC generated by the LVPS. As the LVPS shuts down, so does the HVPS. The actual implementation of this solution requires further analysis to determine if the HVPS will shut down fast enough to prevent screen burn.

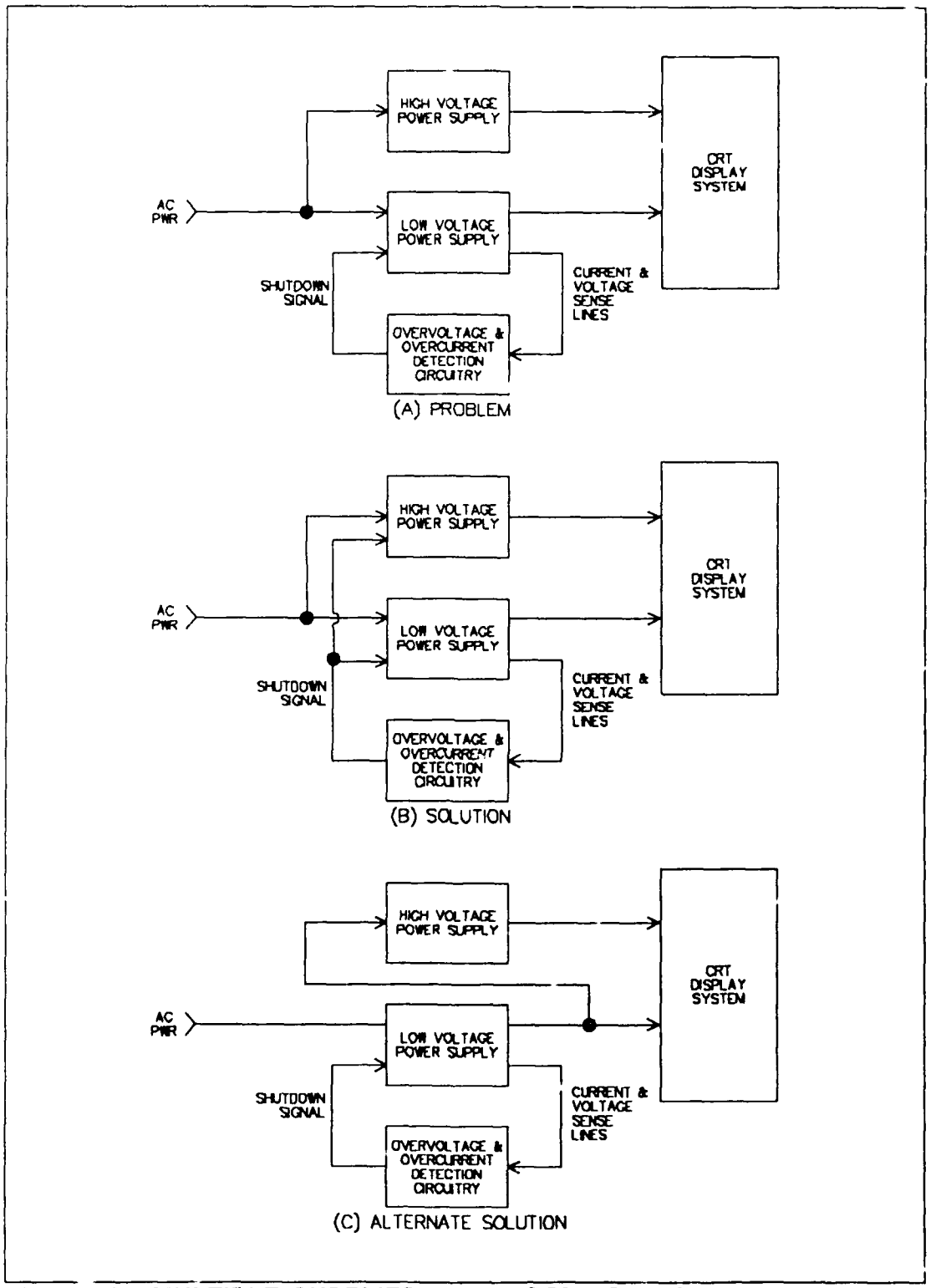

Figure 13. MULTIPLE SUPPLIES FOR A COMMON LOAD

PROBLEM: **A difference in ground potential between two interfacing assemblies (e.g. two PC boards).**

SOLUTION: **Insure interfacing circuitry share a common ground. Minimize voltage difference caused by IR drop by keeping ground return paths between assemblies as short as possible and by using adequate wire gauges or bus bars.**

COMMENT: Ground voltage differences between interfacing circuitry can cause IC input substrate diodes to become heavily forward biased, thereby damaging the device. This problem is shown in Figure 14. In part A of the figure, a logic gate drives a similar gate located 10 feet away. Diode D1 represents the chip substrate diode in the receiving gate. The receiving gate obtains its ground from the driver gate circuit. One amp of current flows through this ground return, and the wire gauge is 28 AWG or approximately 70 ohms per 1000 feet. The resulting ground potential difference (v_2 - v_1 in the figure) is 0.7 volts excluding transient voltages arising from the line inductance. This voltage difference is enough to forward bias D1 when the driver output is in its low state. In part B of the figure, the wire gauge has been increased to 18 AWG (approximately 3 times the overall diameter of the 28 AWG wire). This lowers the wire resistance (and therefore the ground potential difference) by a factor of 10. In addition, the gates have been replaced with transmission line driver and receiver devices that tolerate negative signals. Ground voltage differences also distort signal amplification in analog circuitry and lower input noise margin in digital circuitry. The layout of ground circuitry should anticipate the eventual increases in resistance of the ground path such as due to corrosion and electromigration. The selection of materials and layout should minimize these increases.

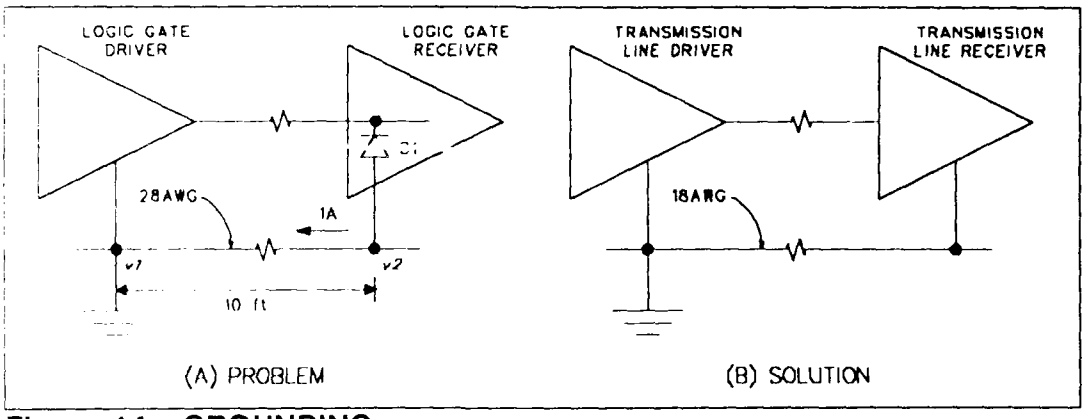

Figure 14. GROUNDING

PROBLEM: Mixing high current and low current grounds within a circuit.

SOLUTION: Provide separate ground return paths for high current and low current loads.

COMMENT: High current loads include drivers for displays, motor windings, relay coils. Low current loads include logic and low power analog circuitry. Separating the grounds for these two types of loads prevents voltage transients due to the resistance and inductance of the high current path from being introduced into the low current circuitry. This is depicted in Figure 15 where L1 and L2 represent high current inductive loads, Q1 and Q2 are the load drivers, and U1, U2 and U3 represent miscellaneous low current logic devices. In part A of the figure, a single ground is used for the high current drivers and the low current devices. In part B, separate grounds originating at the power supply are used. Separating analog from digital grounds and low frequency from high frequency grounds is also a good design practice.

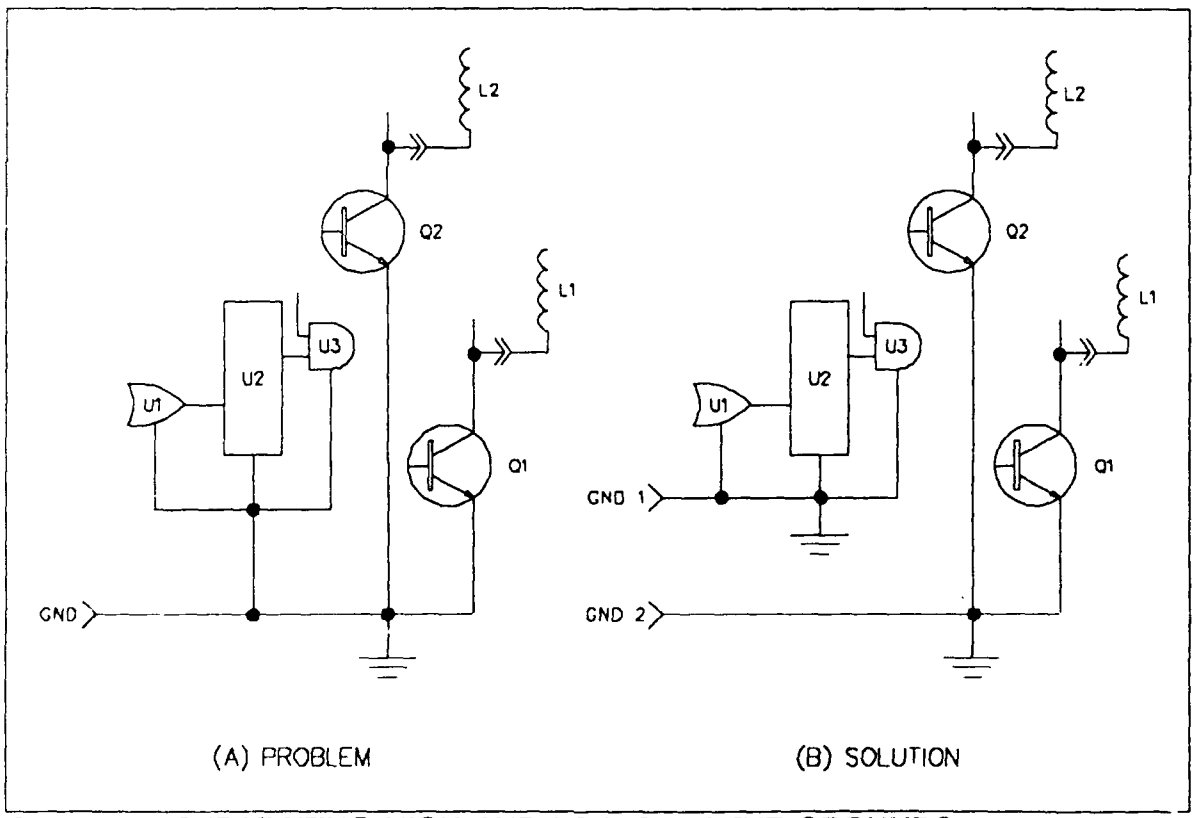

Figure 15. SEPARATING HIGH AND LOW CURRENT GROUNDS

SWITCHING CIRCUITRY

TARGET: Switching devices controlling shared loads.

PROBLEM: A load connected to more than one switch and unintentionally enabled by a switch being closed.

SOLUTION: Place a diode or relay between the load and the switch in question.

COMMENT: This problem is typically associated with paralleled switches connected to paralleled loads in an "X" pattern as shown in part A of Figure 16, and leads to the wired-OR problem presented in Design Rule 5. The solution is to replace the "X" with an "H" using a diode (D3 in part B of the figure) for the cross-bar.

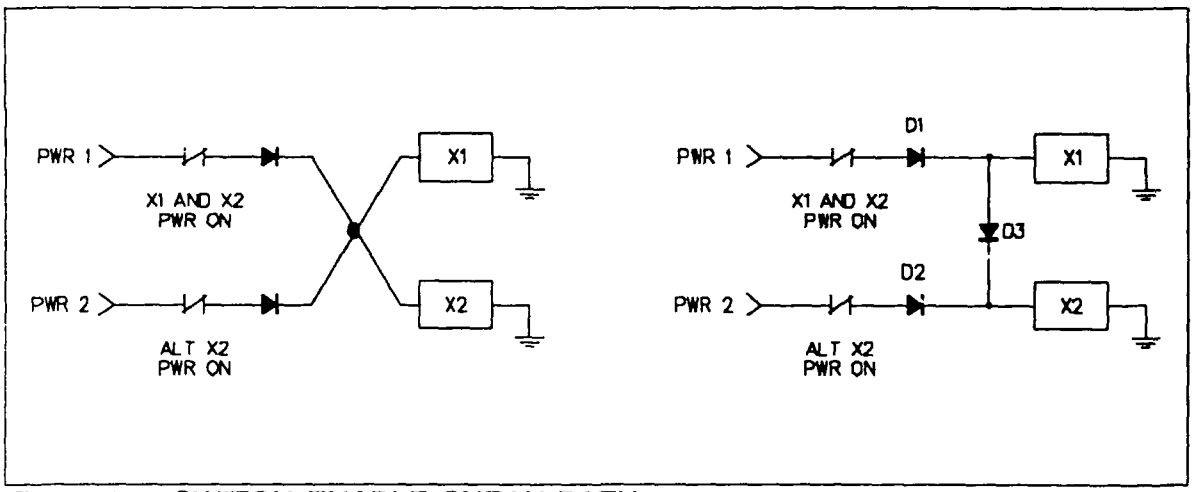

Figure 16. SWITCH ENABLE SNEAK PATH

TARGET: Switching devices controlling shared loads.

PROBLEM: A load controlled by more than one switch and unintentionally disabled by a switch being opened.

SOLUTION: Connect the load in question to a switch directly tied to the power source, or add a switch dedicated to controlling the load in question.

COMMENT: This problem is associated with switches in series connected to paralleled loads in a "Y" pattern, the stem being the switch string (S1 and S2 in part A of Figure 17). It is most desireable for the load in question to be controlled by the switch directly tied to the power source (switch S1 in the figure) so that the load in question can be connected directly to that switch instead of being directly connected in parallel with the remaining loads.

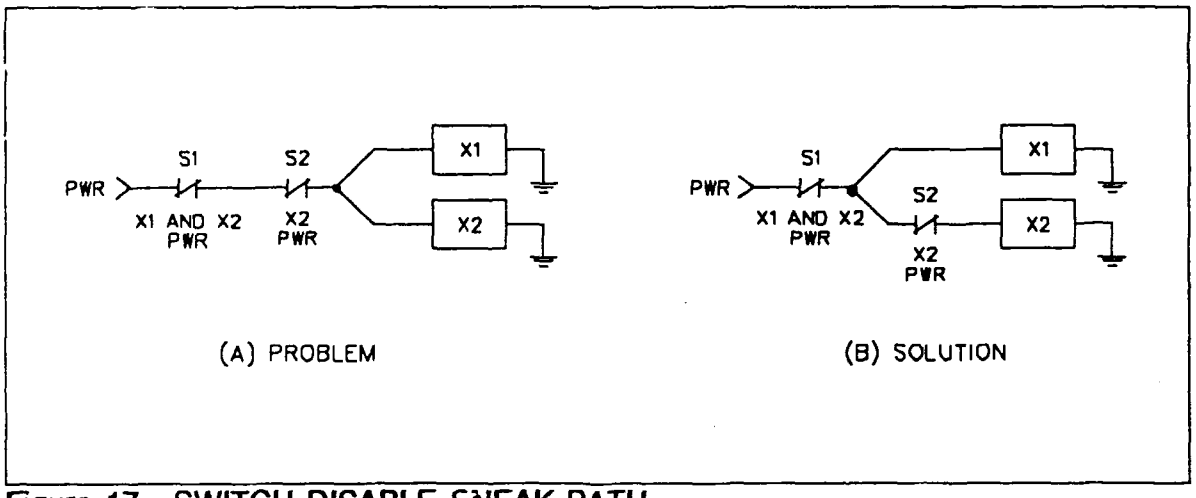

Figure 17. SWITCH DISABLE SNEAK PATH

SNEAK TIMING

TARGET: Digital circuitry.

PROBLEM: Logic and timing errors caused by a digital signal that splits and later recombines.

SOLUTION: Analyze the signal path through a complete cycle (e.g. ON-OFF-ON) to insure correct logic and timing. Correct timing skew problems by providing a clocked data buffer (e.g. latch) to sample stable data at the point where they recombine.

COMMENT: Recombined paths often lead to sneak timing as a result of the logic functions performed along each path. A specific example of sneak timing caused by an unanticipated logic state can be found in NAVSO P3634 (see reference [2]), section A.3.5. A more commonly encountered problem is a transient signal ("glitch") caused by differences in the signal propagation delay between paths. A clocked buffer reduces timing offset ("skew") by resynchronizing the signals. For example, in part A of Figure 18 a glitch occurs at the output of gate U4 during the brief interval that the skewed output signals at gates U2 and U3 are both high. The glitch is prevented as shown in part B of the figure by sampling the outputs of U2 and U3 with buffer U5 after the signals have completed their transitions.

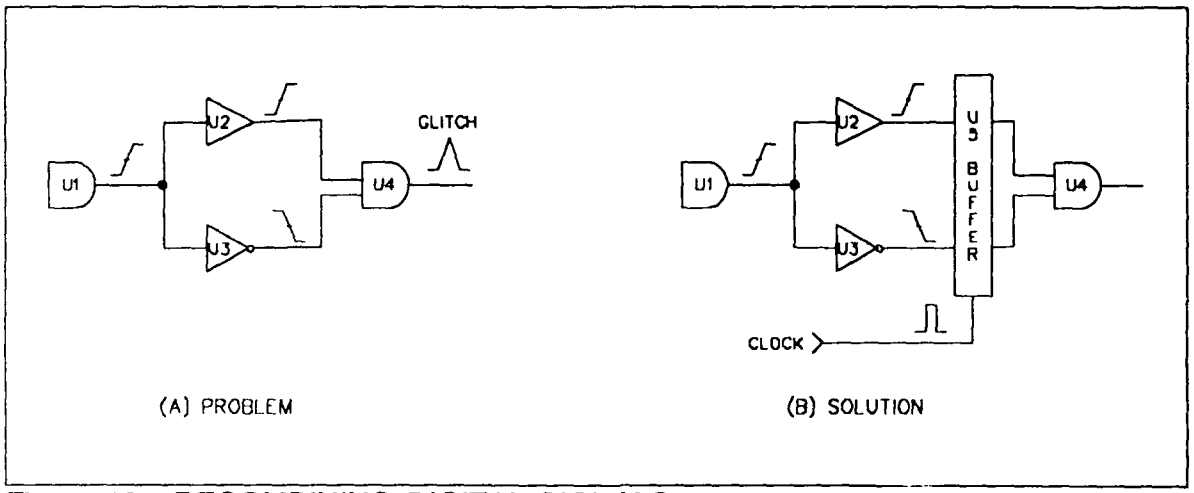

Figure 18. RECOMBINING DIGITAL SIGNALS

TARGET: Digital circuitry.

PROBLEM: **False data caused by interfacing digital devices powered from different supplies.**

SOLUTION: **Insure interconnected digital devices share a common power supply. If this is not possible, circuit outputs must be considered invalid until all supplies are powered up and all registers reset to their initial states.**

COMMENT: When the supply voltage is below some threshold value during power up or power down, the output of a digital device is unpredictable. During power down, a subsequent device powered from a supply which decays more slowly may therefore receive unpredictable data and produce false data. Similarly, during power up, a subsequent device powered from a supply which rises faster may create the same problem. As shown in Figure 19, this type of problem is likely to occur at an interface. Part A of the figure depicts an example of power-on and power-off waveforms for the +5 volt and +12 volt power supplies used in the circuit shown in part B. At time t_1 the +12 volt power has reached its operating value while the +5 volts is still below a level at which predictable operation of the logic devices is guaranteed (e.g. 4.5 volts for TTL logic families). In part C, a circuit has been added to inhibit gate U2 until the +5 volts has reached an operating level. The time delay for this circuit is set by the product of resistor R1 and capacitor C1 and the threshold of Schmitt triggered gate U4. A gate having a Schmitt triggered input is required to unambiguously sense the slowly rising voltage across C1 (see for example Figure 24 and its accompanying guideline). The inhibit function is not required at power-off for this example because the +12 volts powering U3 falls to a non-operative level before the +5 volt line has dropped significantly. Resistor R2 and diode D1 serve as a low impedance discharge path for C1.

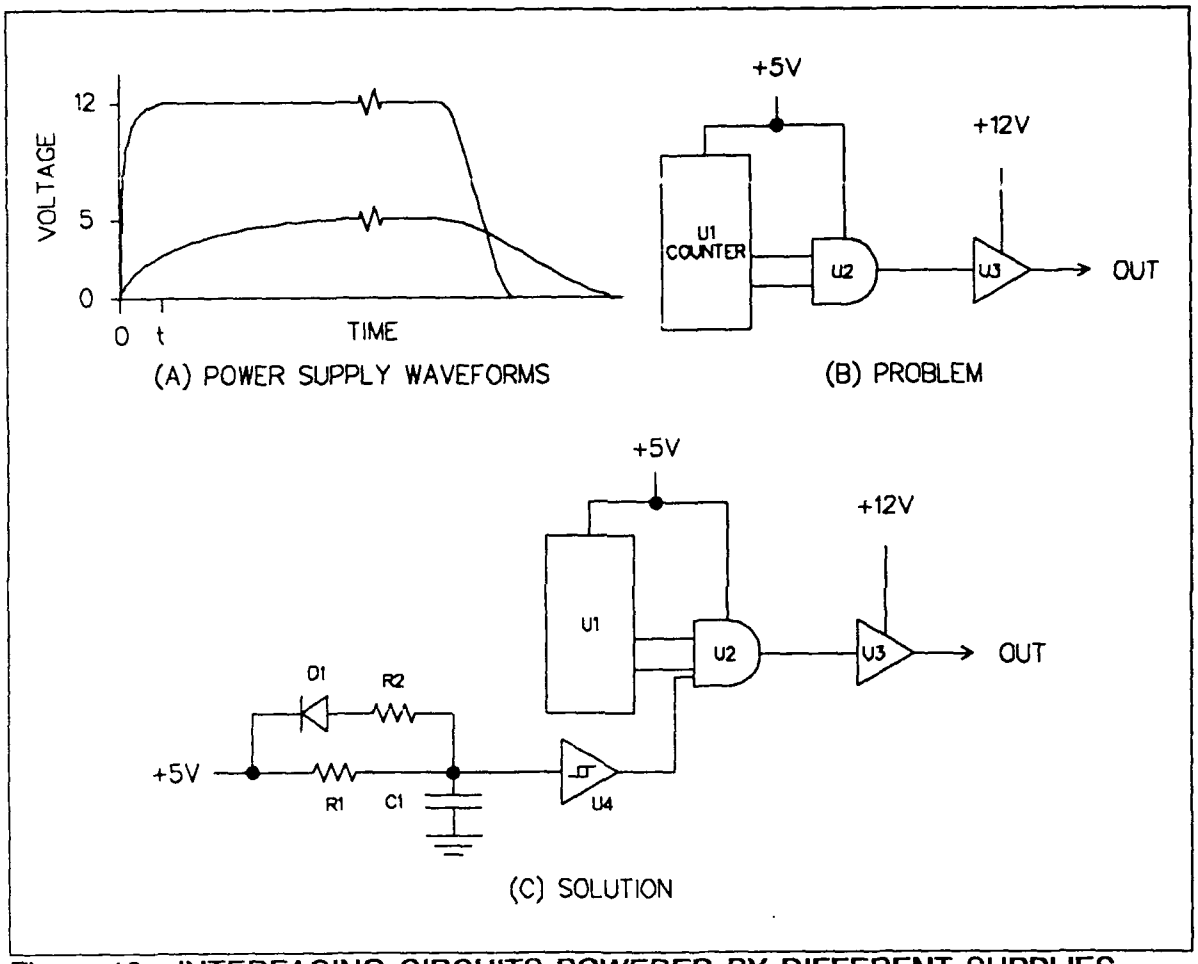

Figure 19. INTERFACING CIRCUITS POWERED BY DIFFERENT SUPPLIES

SNEAK LABELS AND INDICATIONS

TARGET: Signal labels.

PROBLEM: **Interface signals routed to unintended places.**

SOLUTION: **Check signal names on both sides of an interface.**

COMMENT: Unintended routing is a form of sneak path typically involving apparent reversal of polarity or phase between signals crossing a subsystem interface. For example, assume signals labeled TRIG+ and TRIG- appear in the output of subsystem A. A problem occurs if the input required for subsystem B is labeled TRIG IN. Instead, the label should clearly indicate the desired polarity (e.g. TRIG+ IN or TRIG- IN) to avoid errors during analysis, assembly or maintenance actions.

TARGET: Indicators and associated drive circuitry.

PROBLEM: **An indicator that monitors the commanded state of a function rather than the actual state.**

SOLUTION: **Insure that the indicator is monitoring the state of commanded function rather than the command signal.**

COMMENT: For example, an indicator monitoring the relay coil circuit in Figure 20A will only show the intended state of the relay. Instead, the indicator circuit should monitor the relay contact circuit as in Figure 20B to show the actual state of the relay.

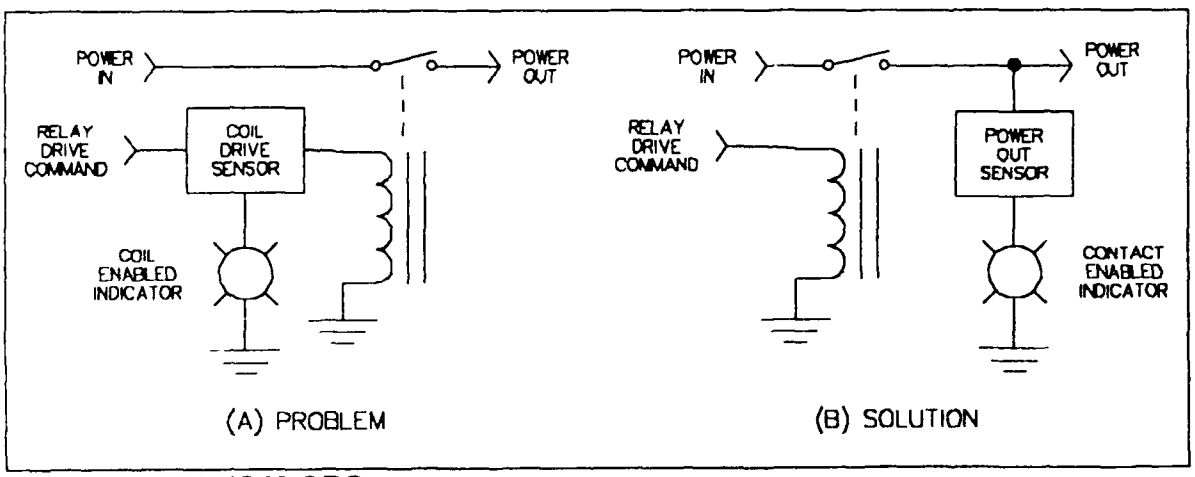

Figure 20. INDICATORS

TARGET: Indicators and associated drive circuitry.

PROBLEM: **An indicator circuit that depends upon the function it monitors for proper operation.**

SOLUTION: **Insure indicator power and drive signals are present even when the monitored function has been turned off, disconnected, or is inoperative due to a failure.**

COMMENT: If an indicator circuit depends upon the operation of the monitored function, improper or unexpected operation of the function may inhibit the indicator circuitry. An example is shown in Figure 21. In part A of the figure, assume heating element R1 has failed open. In this case, Heater Power lamp DS1 will indicate power off when in fact power is still available at the supply side of the heating element. This misleading indication presents a safety hazard to service personnel. A solution to this problem in shown in part B of the figure. To indicate heater failure without implying power off, the lamp circuit in part A should be used with DS1 labeled HEATER CURRENT. Alternatively, separate operations and maintenance indicators can be installed as shown in part C.

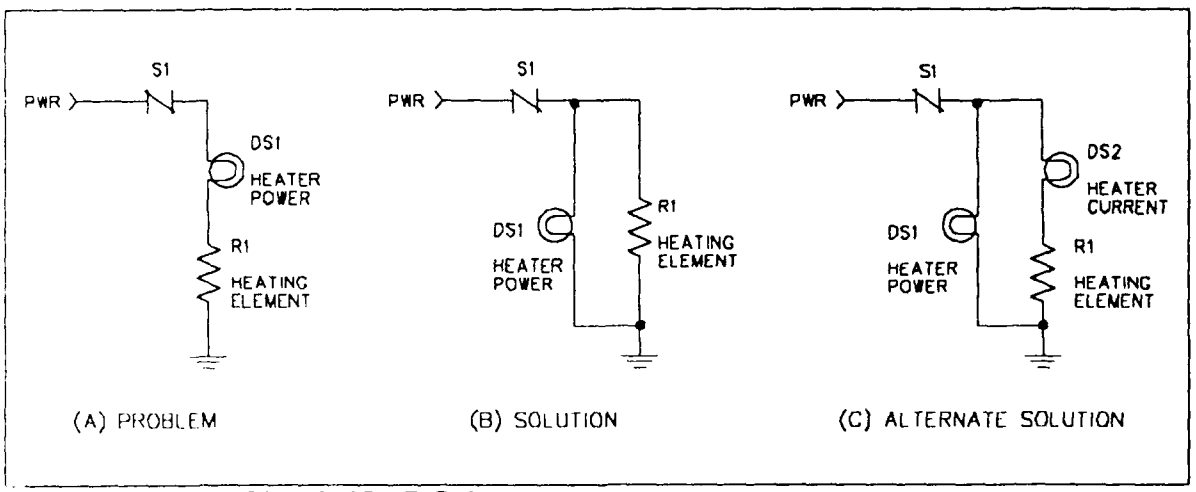

Figure 21. FALSE INDICATION

6. SNEAK CIRCUIT DEVICE GUIDELINES

The Sneak Circuit Functional Guidelines aid the circuit designer or reliability analyst to identify devices commonly associated with sneak conditions. Each guideline is formatted as follows:

a. TARGET -- The types of circuit devices targeted by the guideline.

b. PROBLEM -- A statement of the sneak problem addressed by the rule.

c. SOLUTION -- A recommended approach for implementing the rule in practical situations.

d. COMMENT -- Supplementary information further explaining the rule, in some cases accompanied by a figure.

The following is a selection guide for application of the device guidelines:

APPLICABLE DEVICES	PAGE
Bipolar transistors	31
Op-amps	32
Noise sensitive circuits (op-amps, one-shots, SCR's)	33
Relays	34
TTL or MOS digital circuitry	35

TARGET: Bipolar NPN or PNP transistors.

PROBLEM: Sneak path in the forward direction through a normally reversed biased base-collector junction.

SOLUTION: Analyze the circuit to determine if the base-collector junction can become forward biased. If so, use a diode to prevent current flow out of the collector, or redesign the circuit to avoid the forward bias condition.

COMMENT: This problem can occur if collector voltage V_{CC} is removed from the collector and a signal is applied at the transistor base. In part A of Figure 22, if collector bias voltage is removed from NPN transistor Q1 by opening switch S1, then signal generator current can flow through the base-collector junction of Q1 and into load X1. This current flow can be prevented as shown in part B of the figure by the addition of diode D1 or alternatively as shown in part C by powering the signal generator from the switched supply.

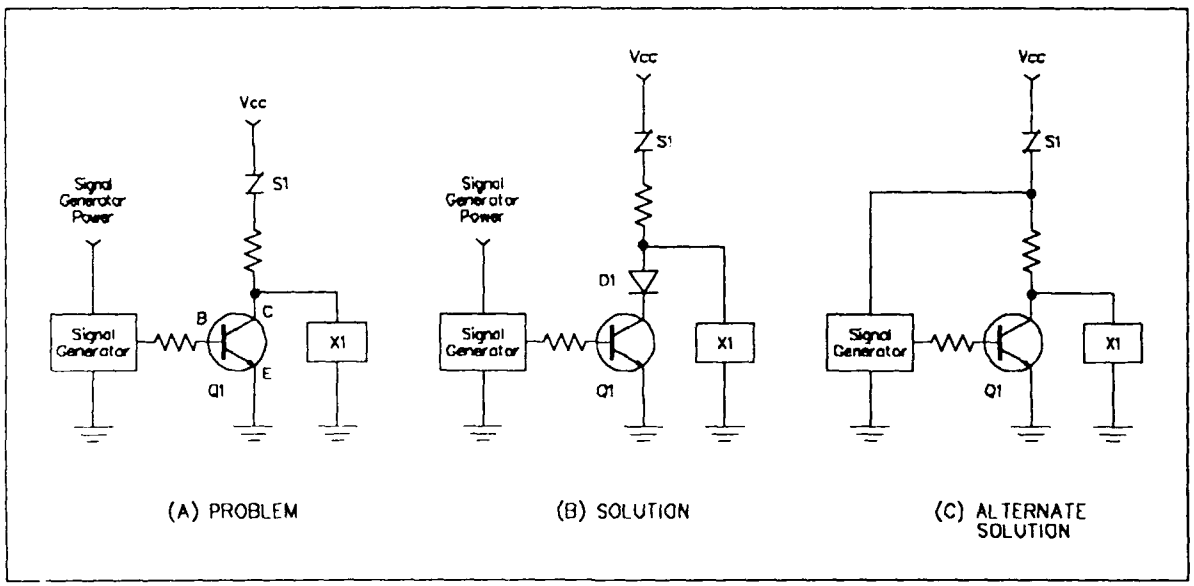

Figure 22. SNEAK PATHS THROUGH BIPOLAR TRANSISTORS

TARGET: Operational amplifiers.

PROBLEM: Presence of reverse current at the input summing point of an op-amp adder unintentionally driven into saturation.

SOLUTION: Limit the maximum amplitude of the input signal to the peak output swing of the amplifier divided by the closed loop gain or insure each input is capable of withstanding the highest voltage input source.

COMMENT: The summing point of an op-amp adder (node P in Figure 23) will remain at virtual ground so long as the op-amp is not driven into saturation. In part A of the figure, saturation will occur when input A exceeds 5v since the closed loop gain (-R3/R1 = -3) times the input voltage will exceed the op-amp negative supply (-15v). In this case current will flow from input A to input B, possibly damaging TTL gate U2. In part B of the figure, diode D1 clamps the signal to approximately 5.7 volts (5v plus one forward diode drop). Resistor R5 has been added to limit the current flowing through D1 when input A causes the diode to clamp. In addition, an LSTTL gate is substituted for the TTL version; the former can withstand up to 10 volts applied to its output while in a high state and can typically sink up to 8 milliamperes while in the low state.

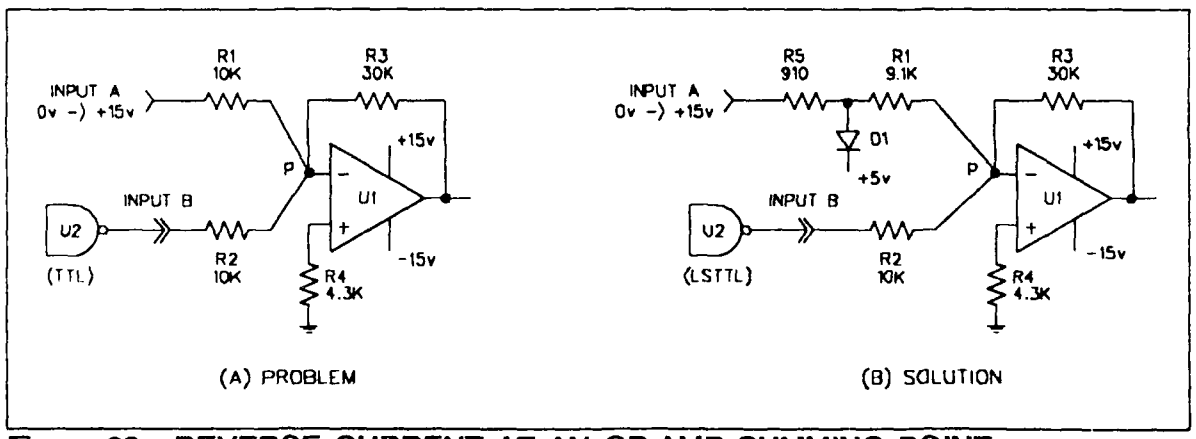

Figure 23. REVERSE CURRENT AT AN OP-AMP SUMMING POINT

ANALOG SEMICONDUCTOR DEVICES (Continued)

TARGET: Noise susceptible devices such as low level, high gain signal amplifiers, multivibrators (one-shots), thyristors (SCRs, triacs).

PROBLEM: Sensitive signal paths in close proximity to switched signal or power lines.

SOLUTION: Route sensitive paths away from noise sources. Shield sensitive signals using ground planes or guard bands on PC boards or cable shields for discrete wiring.

COMMENT: Noise can be capacitively or inductively coupled into a susceptible input from adjacent power lines or switched signal lines. Identify sneak electromagnetic paths by examining the physical layout of the circuitry. A schematic points to this problem if it depicts high current or high voltage devices on the same circuit board with susceptible devices. Examples of noise sources include:

a. power lines
b. brush-type motors
c. lamp, squib, stepper motor or other type of high current driver
d. Outputs of a digital counter (particularly when all bits change simultaneously)

Circuit elements that are particularly susceptible include:

a. op-amps
b. comparators (when an input is near the trip threshold)
b. one-shots
c. SCRs and triacs (gate input)
d. MOS type devices
e. clock lines

RELAY TIMING

TARGET: Relays, solenoids, contactors, stepper motors and other inductively actuated devices.

PROBLEM: Relay coils with single or double diode suppression networks have long current decay time constants which can cause timing problems.

SOLUTION: Place a zener diode in series with the standard diode, cathode to cathode with the standard diode's anode connected to the negative end of the coil.

COMMENT: When a relay is de-energized, a transient is induced in the coil. Because the transient could reduce the reliability of associated circuit components, transient suppression is normally required. A typical suppression technique shown in part A of Figure 24 is to add a diode (D1 in the figure) across the coil (cathode connected to the positive side). An optional second diode (D2 in part B of the figure) can be added between the coil and power to protect the first diode against burn-out due to accidental reverse application of power. Adding a zener diode (D3) in series with the standard diode across the relay coil provides good suppression while decreasing relay drop-out time. With no zener, the L/R time constant increases by a factor of 5 to 10, causing contact bounce and early wear-out.

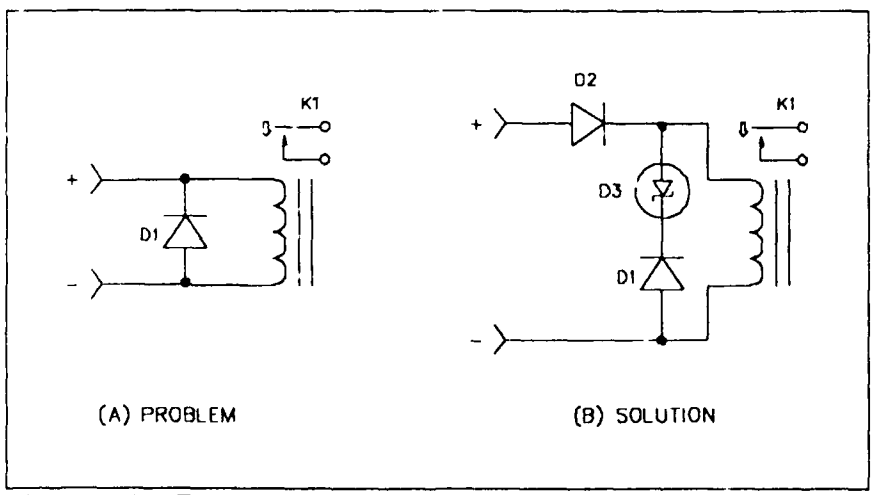

Figure 24. RELAY SUPPRESSION NETWORKS

TARGET: TTL and MOS logic, memory and processor devices.

PROBLEM: Slow rise or fall times for any input signal to a digital device.

SOLUTION: Use Schmitt triggered gates for decreasing signal transition times. Avoid placing capacitors on logic signal paths.

COMMENT: Input signal rise or fall times slower than 50 nsec for TTL or 15 usec for MOS can cause multiple false triggering of the device or excessive power dissipation. This is depicted in Figure 25. Part A of the figure shows a typical inverting gate with voltage V_{IN} applied to its input and V_{OUT} appearing at its output. The output waveform corresponding to an input signal having normal rise and fall times is shown in part B. When the input rise and fall times are excessively slow as shown in part C, an oscillation can occur at the output during the time interval that the input signal is between the unambiguous logic 0 and logic 1 states (i.e. for TTL, less than 0.8 volts and greater than 2 volts). As shown in part D, this oscillation is avoided when a Schmitt triggered gate is used. This type of gate employs positive feedback to virtually eliminate input signal level ambiguity.

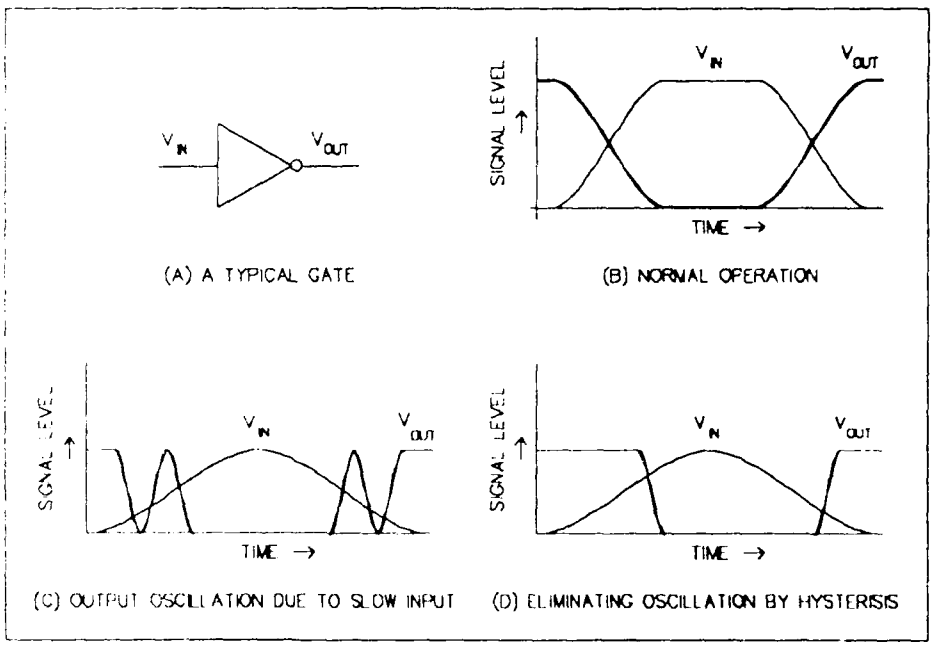

Figure 25. EFFECT OF SLOW RISE OR FALL TIMES

PROBLEM: **Undesired triggering caused by open (floating) inputs.**

SOLUTION: **Terminate unused inputs to power or ground. Tie TTL inputs (except diode-input LSTTL) to power through a series resistance of from 1K to 5K ohms. Tie diode-input LSTTL devices directly to power or ground.**

COMMENT: Floating inputs (particularly CMOS) can trigger a device because of charge coupling from nearby signals. Tying unused gate inputs with those that are used instead of to power or ground will increase input current and capacitive loading. This practice along with series resistance termination should be especially avoided for LSTTL devices with diode inputs because of their higher noise susceptibility (noise can enter through the parasitic capacitance associated with each diode).

PROBLEM: **Digital devices tied to a single, physically long clock signal path.**

SOLUTION: **Use separate, short, equal length runs from the clock source to each device.**

COMMENT: Propagation delay along a single clock path can cause timing skew between outputs of clocked devices. An example is shown in Figure 26. In part A of the figure, the path length from the source of the clock signal to the clock input of U1 is shorter than for U2, which in turn is shorter than for U*n*. The resulting timing skew among outputs O1, O2 and O*n* is shown in part B of the figure. This skew can be reduced by equalizing the clock path lengths as shown in part C. In general, path length equalization is necessary when the difference between the length of the signal path from the clock to the closest clocked device and the path from the clock to the farthest clocked device is greater than the following values:

Clock Frequency	Path Length
1 MHz	70 inches
10 MHz	7 inches
100 MHz	0.7 inches

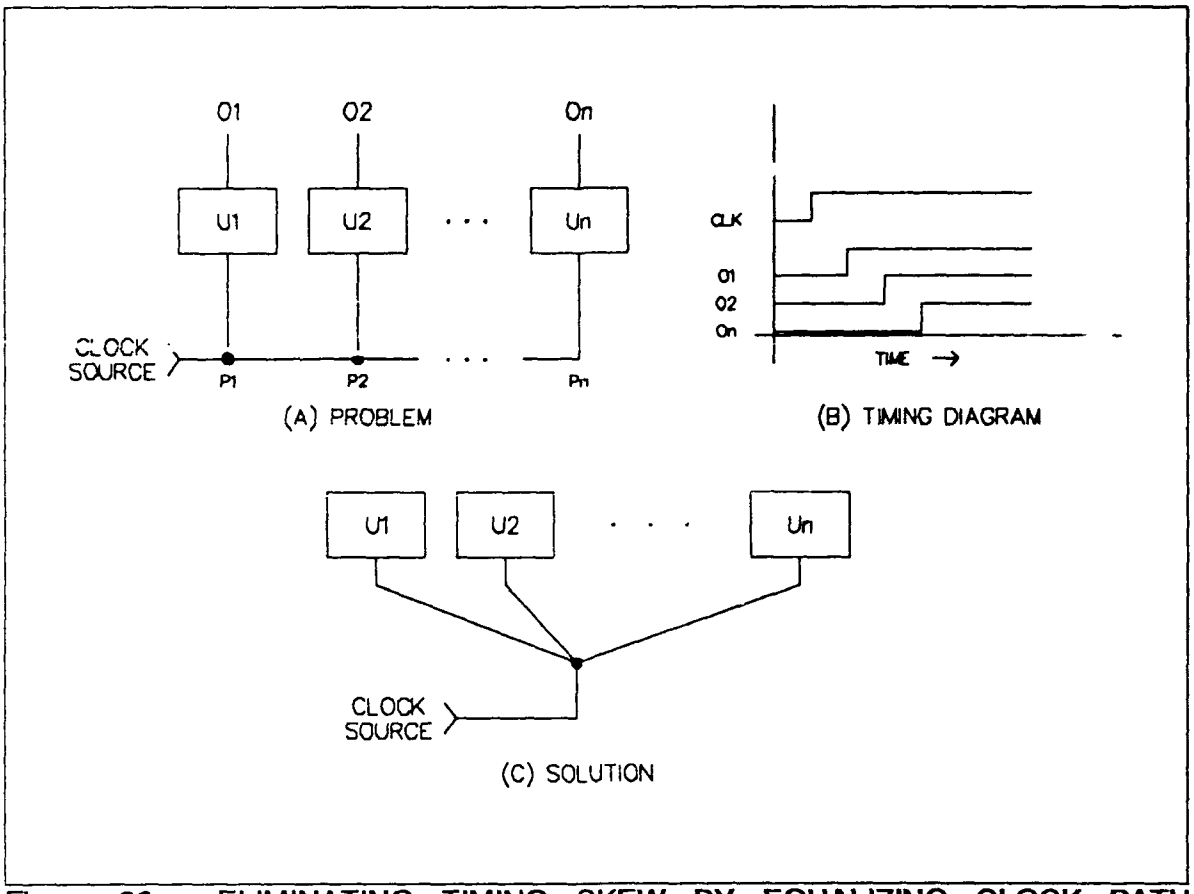

Figure 26. ELIMINATING TIMING SKEW BY EQUALIZING CLOCK PATH LENGTHS

TARGET: TTL and MOS logic, memory and processor devices.

PROBLEM: Erroneous signals generated by line drivers with outputs fed back to other on-board logic.

SOLUTION: Use line drivers only for interfacing with line receivers. Feed back signals from driver inputs, adding inverters if necessary. Do not use logic having internal feedback as a line driver.

COMMENT: Signal reflections on the transmission line can erroneously trigger logic either on a circuit board or on a driver chip that is tied to the driver output. Part A of Figure 27 depicts on-board logic susceptible to false triggering. In part B of the figure, the problem is avoided by driving the on-board circuitry with a signal derived from the driver U2 input. Inverter U3 is added both for obtaining the correct polarity and for buffering the signal so as not to overload signal source U1.

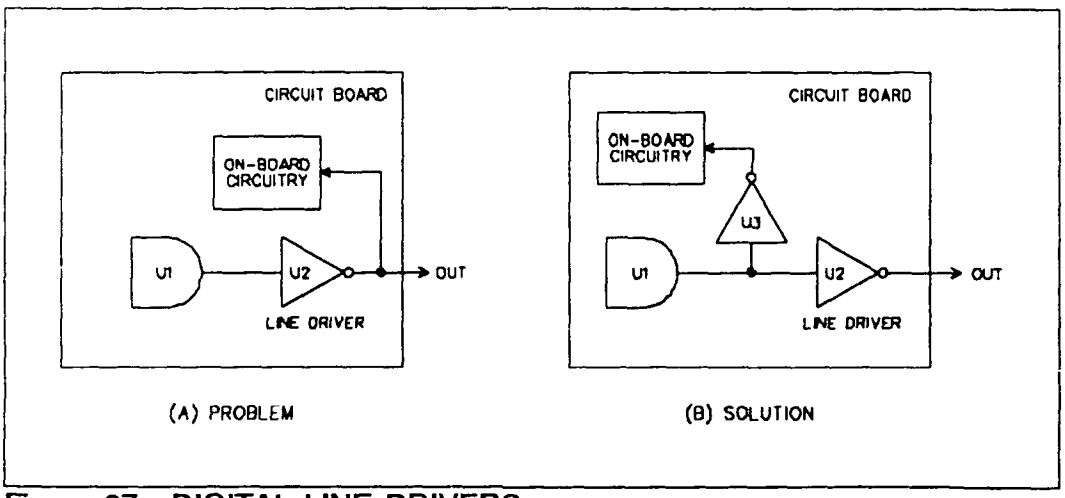

Figure 27. DIGITAL LINE DRIVERS

TARGET: TTL and MOS logic, memory and processor devices.

PROBLEM: Faulty operation or damage to a digital device due to high current flowing through the substrate diode at the device input.

SOLUTION: Insure inputs of digital devices are not driven below ground. Place fast recovery diodes at the device input (anode to input, cathode to one diode drop above ground) to prevent the input from going below ground.

COMMENT: The diodes supplement those that are on the chip; the latter are typically designed to handle short duration current transients while the former will protect against steady state currents. Negative going signals can occur on lines transmitting data from off the board or on lines coming from circuitry powered by a negative supply. The placement of the protection diode is shown in Figure 28.

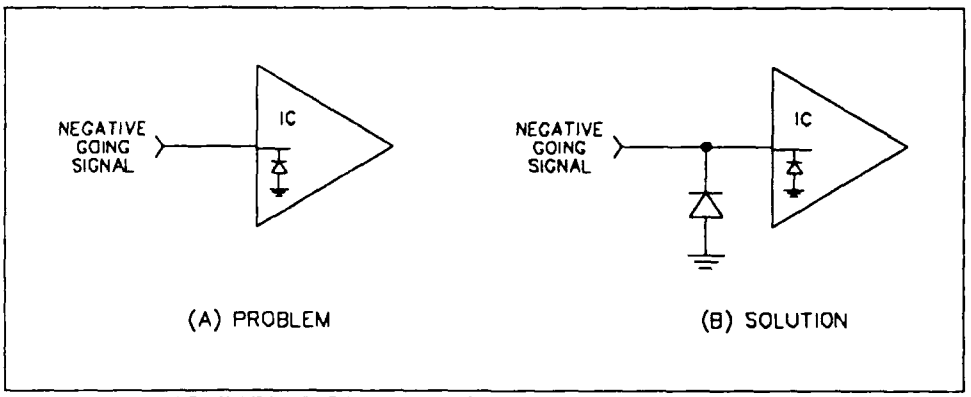

Figure 28. IC INPUT CLAMPING DIODE

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[1] R. C. Clardy, "Sneak Circuit Analysis Development and Application," *1976 Region V IEEE Conference Digest*, 1976, pp. 112-116.

[2] Dept. of Navy, *Sneak Circuit Analysis: A Means of Verifying Design Integrity*, NAVSO P3634 (stock no. 0518-LP-394-8000), July 1986.

Suggested Reading

1. Dept. of Navy, *Sneak Circuit Analysis*, R&M-STD-R00205, Naval Avionics Center Reliability & Maintainability Standard, 29 May 1986.

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