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Modeling the Gate I/V Characteristic of a GaAs MESFET for Volterra-Series Analysis

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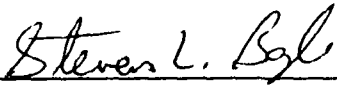
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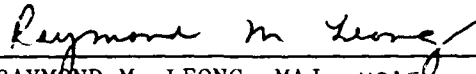
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This report shows that the Taylor-series coefficients of a FET's gate/drain I/V characteristic, which are used to model the I/V nonlinearity for Volterra-series analysis, can be derived from low-frequency rf measurements of harmonic output levels. The method circumvents many of the problems that occur when dc measurements are used to characterize this nonlinearity.					
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PREFACE

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I. INTRODUCTION

Volterra-series analysis¹⁻³ is an efficient and practical method for determining intermodulation levels in small-signal MESFET amplifiers. The Volterra series is particularly valuable when implemented in a general-purpose computer program,⁴ because it can be used to analyze very large or complex circuits, it does not require that the circuit topology be simplified, and it is significantly more efficient than time-domain or harmonic-balance methods.

Although much research has been directed at developing large-signal FET models for use with harmonic-balance analysis, very little work has been done to model GaAs MESFETs for Volterra-series analysis. Modeling GaAs MESFETS presents a number of subtle problems that occasionally have been noted by other authors (e.g. Refs. 5, 6); one of the most serious of these problems is the difficulty of modeling the FET's "nonlinear transconductance," or more precisely its nonlinear incremental gate/drain I/V characteristic. This report describes a method for determining the parameters of this characteristic by means of simple, low-frequency rf measurements.

II. THE MESFET MODEL

Figure 1 shows a small-signal nonlinear model of a MESFET. This model consists of a modified conventional small-signal linear model, in which three elements -- the gate/source capacitance C_{gs} , the drain/source resistance R_{ds} , and the drain current $i_d(v_g)$ -- are nonlinear. Although C_{gs} and R_{ds} are significant sources of intermodulation in small-signal FETs, in most cases the dominant nonlinearity is that of $i_d(v_g)$.

The nonlinear resistive elements are characterized by Taylor-series expansions of their I/V characteristics in the vicinity of the dc bias point. Thus, the nonlinearity $i_d(v_g)$ is

$$i_d = \left. \frac{dI_d(v_g)}{dv_g} \right|_{v_g=v_{g,0}} v_g + \frac{1}{2} \left. \frac{d^2 I_d(v_g)}{dv_g^2} \right|_{v_g=v_{g,0}} v_g^2 + \frac{1}{6} \left. \frac{d^3 I_d(v_g)}{dv_g^3} \right|_{v_g=v_{g,0}} v_g^3 + \dots \quad (1)$$

where $I_d(v_g)$ is the large-signal gate/drain characteristic and i_d and v_g are, respectively, the incremental (rf) drain and gate currents and voltages, i.e., the current and voltage deviations from the bias point $I_d(v_{g,0})$. Then i_d is expressed as

$$i_d = a_1 v_g + a_2 v_g^2 + a_3 v_g^3 + \dots \quad (2)$$

The traditional method of determining the series coefficients a_n is to measure the I/V characteristic at a fixed drain-bias voltage and to perform a least-squares fit of $i_d(v_g)$ to a polynomial of the desired degree. Although this process is usually adequate for determining a_1 (which is equivalent to the linear transconductance), it is often unsatisfactory for determining the higher-order coefficients: because of the ill-conditioned nature of the normal equation, the values of a_n determined in this manner are very sensitive to measurement inaccuracy, round-off errors, and the selection of data points.

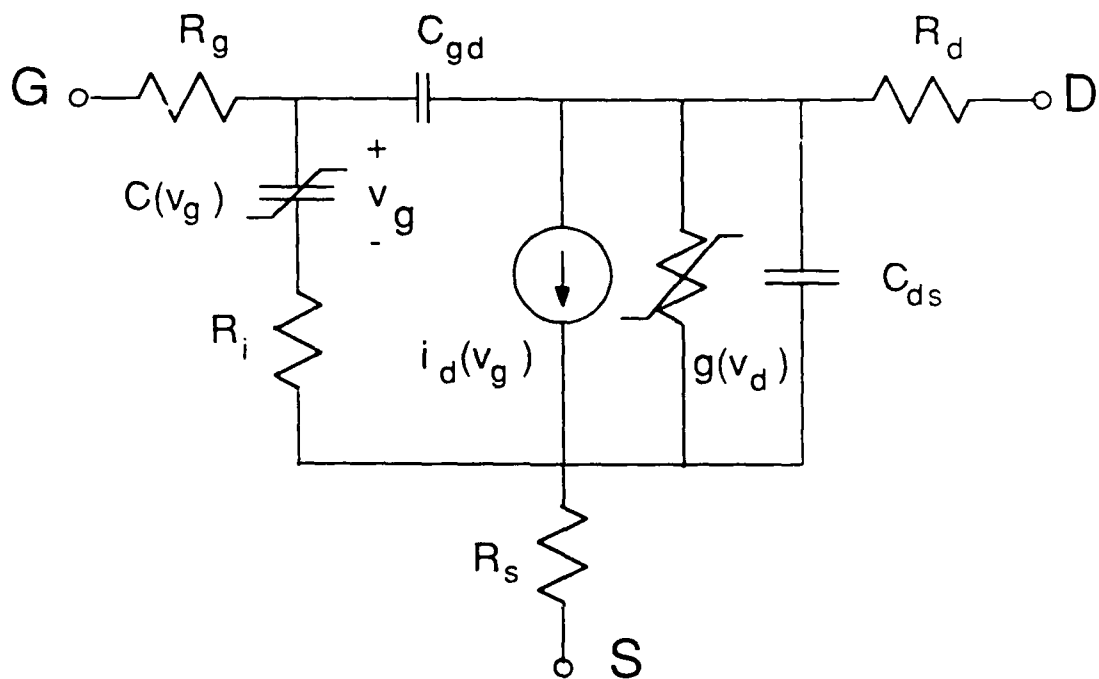


Fig. 1. Small-Signal, Nonlinear Equivalent Circuit of a GaAs MESFET

Differentiating the measured data directly is often adequate for determining a_1 and sometimes a_2 ; however, differentiation exacerbates the effects of round-off errors and thus makes the higher derivatives unreliable.

A more fundamental problem is related to traps in the FET's channel; these introduce long time constants into $i_d(v_g)$ and cause differences between the dc and rf I/V characteristics. Trapping effects are often not evident in a_1 or a_2 , but derivatives of higher order are very sensitive to them. This is particularly the case when automated equipment is used to measure $I_d(V_g)$; differences in stepping speed and dwell time at each data point affect the coefficients' values strongly.

An effective way of circumventing these problems is to derive the series coefficients from rf measurements instead of dc. The rf measurements are made at a frequency in the VHF range, at which both trapping effects and the FET's reactive parasitics are negligible. Under these conditions the levels of the harmonic output components are functions of only the input power, the FET's source resistance, and the series coefficients. It is a simple matter to measure the harmonic levels and to derive the coefficients from them.

III. DESCRIPTION OF THE MEASUREMENTS

When the rf frequency is very low, the equivalent circuit of Figure 1 can be simplified to form the circuit shown in Fig. 2. In Fig. 2 the FET is driven by an rf source at a frequency of approximately 50 MHz, and the drain is terminated in a load resistance R_L , where $R_L \ll R_{ds}$. R_L is a shunting resistor that reduces the current in R_{ds} to the point where its effects are negligible; one should make R_L as small as possible while still allowing harmonic output components to be observable on a spectrum analyzer. Because the series coefficients are derived from the relative levels of the harmonics, and not their absolute powers, the value of R_L does not affect the accuracy of the measurement.

Using the method of nonlinear currents,^{2,3} one can show that the first three harmonics of the drain current, I_{1-3} , are

$$I_1 = \frac{a_1 V_{gs}}{1 + a_1 R_s} \quad (3)$$

$$I_2 = \frac{a_2 (1 - a_1 R_s) V_{gs}^2}{2(1 + a_1 R_s)^2} \quad (4)$$

$$I_3 = \frac{(a_3 - 2a_2^2 R_s)(1 - a_1 R_s) V_{gs}^3}{4(1 + a_1 R_s)^3} \quad (5)$$

V_{gs} is the magnitude of $v_{gs}(t)$; i.e.,

$$v_{gs}(t) = V_{gs} \cos(\omega t) \quad (6)$$

and the available power P_a of the source is

$$P_a = \frac{V_{gs}^2}{8 R_{in}} \quad (7)$$

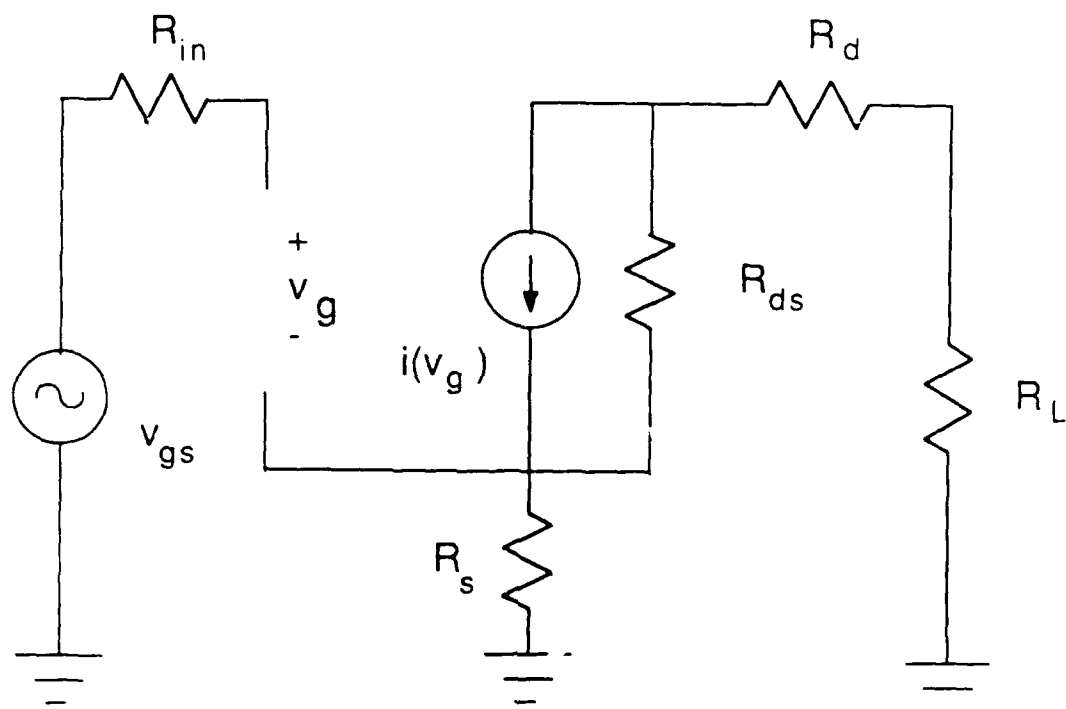


Fig. 2. FET-Equivalent Circuit Valid at Frequencies in the VHF Range. R_L is the output-shunting resistor used to minimize harmonic generation in R_{ds} .

where R_{in} is the source resistance.

Substituting Eq. (7) into Eqs. (3) and (4), dividing Eq. (4) by Eq. (3), and squaring the result gives the ratio of second-harmonic output power to fundamental output power, IMR_2 :

$$IMR_2 = \frac{2 a_2^2 R_{in} (1 - a_1 R_2)^2 P_a}{a_1^2 (1 + a_1 R_s)^2} \quad (8)$$

A similar process gives the ratio of third-harmonic output power to fundamental output power, IMR_3 :

$$IMR_3 = \left[\frac{2(a_3 - 2a_2^2 R_s)(1 - a_1 R_s) R_{in}}{a_1 (1 + a_1 R_s)^2} \right]^2 P_a^2 \quad (9)$$

When the FET is biased and excited by a low-frequency rf source, the values of a_n can be found by measuring the harmonic output power and solving Eqs. (7) through (9). The process is as follows:

1. a_1 is determined in the conventional manner, i.e., by dc or rf measurements.
2. IMR_2 is measured by means of a spectrum analyzer, and Eq. (8) is solved to determine a_2 .
3. IMR_3 is measured similarly, and Eq. (9) is solved to determine a_3 .

Equation (8) does not indicate whether a_2 is positive or negative. However, because a MESFET's transconductance invariably rises with v_g , a_2 is invariably positive (this is generally not the case in HEMTs, but even then the regions of positive and negative a_2 are clear from the transconductance curve). Because of the squared term in brackets, two values of a_3 satisfy Eq. (9). One can determine the correct root by measuring a few values of a_2 at nearby bias points and picking the value of a_3 that most closely matches $a_3 = 0.33 da_2/dv_g$. Usually the two values of a_3 have different signs; then, to select the correct value of a_3 , one need determine only whether a_2 rises or falls with v_g .

IV. EXPERIMENTAL RESULTS

This method was used to determine the incremental gate I/V characteristic of a packaged Avantek AT10650-5 MESFET biased at a drain voltage of 3 V and drain current of 20 mA. The FET's transconductance was measured at dc, and its small-signal equivalent circuit (including the package parasitics) was determined by adjusting its circuit-element values until good agreement between calculated and measured S parameters was obtained. The FET was then installed in a low-frequency test fixture having a shunting resistance R_L of 5 ohms. The input power P_a was -11 dBm at a frequency of 50 MHz.

The a_n coefficients were determined at 19, 20, and 21 mA, and the values in Table 1 were obtained. The coefficient a_2 was found to decrease with I_d , and the two roots of Eq. (9) had different signs; therefore the negative value of a_3 is the correct one.

Table 1. Taylor-Series Coefficients
for the Avantek AT10650-5

I_d	a_1	a_2	a_3
0.019	0.041	0.0188	-0.0148
0.020	0.041	0.0171	-0.0145
0.021	0.041	0.0158	-0.0128

The FET's gate/source capacitance was modeled as an ideal Schottky-barrier junction capacitance, and the nonlinear drain/source resistance was derived from low-frequency Y parameters measured at a variety of bias voltages. When the source and load terminations were 50 ohms, the program described in Ref. 4 predicted the FET's third-order intermodulation intercept point to be 20.8 dBm at 10 GHz. This result

agrees well with the measured value of the intercept point, which was 22.4 dBm. When the output port was conjugate matched, the calculated intercept point was 24.1 dBm, compared to a measured value of 23.0 dBm. Other tests have shown equal or superior agreement. These results imply that the intermodulation levels in small-signal amplifiers can be predicted within 2 to 3 dB. We believe that the major factor limiting accuracy is the linear part of the FET's equivalent-circuit model, especially the part that models the package. Thus, even better accuracy could be obtained with chip or MMIC circuits.

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