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Work by Prof. J. Allen and his collaborators is summarized here.

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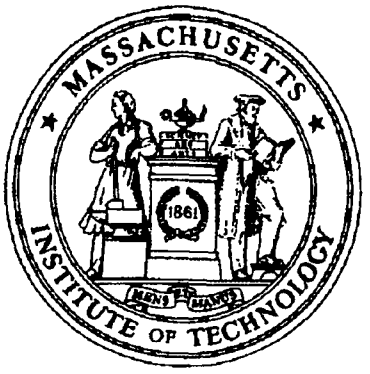

Final Report
to the
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for the Proposal
"The Design of High-Performance Circuits for Digital Signal Processing"
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Submitted by
Professor Jonathan Allen, Principal Investigator

January, 1990

Overview

A-1

In order to place the research done under this contract in perspective, we start by describing the view of integrated circuit design that motivates our work. Our goal is to provide CAD design tools that enable the production of high-performance chips quickly, correctly, and economically, with particular emphasis on digital signal processing. It is the high-performance aspect of the design that has been our particular emphasis. We consider performance to have two aspects. Aspects of performance associated with circuit style and technology are extremely important, since there is continuing improvement in integrated circuit technology, and also because of the constant invention of new circuit forms that provide for faster performance without excessive demands on power. Although it may not be thought of as performance directly, an additional goal at the circuit and layout level is the minimization of area, since this leads to small circuits with minimum length interconnect. In additional to circuit-oriented performance, however, there is also another aspect of performance that we call architectural performance. By this factor, we refer to the parallelism that is contained in a variety of different algorithms. Parallelism can be exploited through the use of pipelining, multiprocessing, and a variety of other architectural schemes. Since the emphasis in this contract is on digital signal processing algorithms, architectural performance is particularly important, since many digital signal processing algorithms have a very large amount of inherent parallelism. This parallelism has been studied a great deal, but there are still important DSP algorithms which have not been implemented in their most completely parallel form. Another important aspect of performance in design is the need to integrate circuit performance and architectural performance. In this contract, we have performed explicit studies which show the interaction between circuit technology and architectural parallelism. In general, it is always most desirable to achieve increased performance through improvements in technology and circuit style, since the introduction of parallelism always involves the use of increased control complexity. On the other hand, in important examples of digital signal processing, it is often necessary to exploit not only the best technology, but also significant amounts of parallelism inherent in the algorithmic specification. In fact, the cohesive integration of various optimization strategies within CAD is a major problem for the field, and one which we have attacked, not only in terms of specific digital signal processing examples, but also in terms of fundamental theoretic approach to overall CAD system design.

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Given that the goal is to produce a high-performance circuit for a particular task, a major problem is presented in terms of the input specification of the particular problem to be solved. It is an unfortunate fact that the specification of algorithms is inevitably confounded with the implication of a particular class of architectures, so that algorithms are inherently biased to the performance associated with this particular class of architectures. Ideally, we would like to be able to specify the input task in a functional way that is independent of architecture. At MIT, considerable progress on this task of functional language specification has taken place, not only in terms of basic data flow notions, but also in terms of languages that are appropriate for signal processing. It is important to point out that the first fundamental signal representation language, SRL, was done under this contract by Kopec, and that the fundamental ideas of data flow representation have been adapted more recently for the specification of systolic nearest neighbor communication architectures that are so important in the implementation of many DSP tasks.

Once a functional specification of the task is available, then a means is needed to compile this specification into at least one particular design, generally at the register transfer level of specification. Some optimization can be performed at this level, in terms of the allocation and utilization of register and ALU components of an architecture, but in the digital signal processing area, it is often important to have a very large component dedicated to architectural exploration. In the case of important DSP algorithms, such as nonrecursive filters and FFTs, there is a huge amount of

parallelism that can be exploited, and systematic means are needed to evaluate the space-time trade-offs inherent in these architectures. A general theory is needed for this purpose, but DSP algorithms present special opportunities and challenges for optimization at this level.

Once means are available for architectural exploration, then it is essential to be able to generate the cells corresponding to registers and ALU capability, as well as the interconnect associated with these architectures. A great deal of effort has been expended on such procedural design capability, and it is represented in two ways within the research taking place on this contract. First of all, the tension between specificity and efficiency of design has been specifically addressed. This problem arises from the fact that it is relatively easy to devise procedural design techniques for very general classes of architectures (such as PLAs), but the resulting designs are often not as efficient as they might be. On the other hand, when the architectural class becomes more specific, greater efficiency can be obtained, but there is a necessity for being able to characterize and generate these specific architectures quickly, correctly, and economically. The approach taken under this contract, which has subsequently been widely adopted in industry, is to provide a regular structure generator which furnishes a language for the specification of special purpose architectures. By use of the regular structure generator, local interconnections between modules are specified by examples, the modules themselves are provided through a library, and the architectural language specification is used to automatically compile the layout in a way that can be parameterized to particular attributes of the problem being solved. This approach has been outstandingly successful, and works well when a small library of predesigned cells is available for use by the compiler. A second approach has been to build general purpose algorithms that are capable of converting circuit net lists in any MOS technology to custom layout. This is particularly important when circuit optimization tools, such as sizing, are utilized, since the wide variety of transistor widths implied by these algorithms are often difficult to accommodate in an efficient way at layout. Furthermore, both NMOS and CMOS technologies can be used, and both normal restoring logic and pass transistor gates can be used in the most effective manner possible. Under this contract, a state-of-the-art tool for conversion from a net list to layout has been provided, and the goodness of this result has been recently verified at the IEEE Physical Design Workshop. This scheme uses high-quality compaction to convert a symbolic layout to a highly compacted mask geometry. Two studies of compaction algorithms have been performed under this contract, and are responsible for the production of high-quality geometry in the final layout.

Recently, two additional themes have been pursued under this contract. The first relates to the use of formal grammar techniques for the verification of circuit style and other attributes of circuit performance. We have introduced the notion of context-free graph grammars to characterize circuit style, and shown how to parse circuit net lists in a very efficient way to verify that any particular circuit style (or mixture of styles) is, in fact, appropriately implemented. In addition, circuit-related problems such as charge sharing and proper ratioing can be detected by more semantically oriented techniques that build on this graph grammar. Another important aspect of our work is the ability to automatically maintain consistency between various levels of representation. When a change is made at one level of representation, it is important to automatically propagate that change to other levels of representation, so that an overall consistent design is obtained. This process must also be coordinated with exploration techniques in order to obtain optimum design at all levels.

From the previous remarks, it is clear that there several main themes associated with our research on the design of high-performance circuits. First, we have devoted considerable attention to specification languages, which allow for the functional characterization of a task in a way that permits performance exploration. Secondly, a great deal of our research is focused on architectural exploration, whereby we use a variety of techniques to achieve several different architectures with different space-time properties. Thirdly, we have expanded upon techniques for the procedural generation of modules, so as to provide optimum layouts of modules that fulfill constraints or device size and interconnection points, as well as pass through busses. Next, a great deal of emphasis has been placed on the characterization of circuit performance through techniques such as macro-modelling and waveform bounding. As a result of this research, MIT is a leader in this field through widely recognized contributions. All of this CAD capability has been utilized to produce several special purpose architectures. Two studies under this contract have illustrated this capability. In one case, a special highly optimized building block has been developed for FFTs and digital filters. In another case, capability which was originally introduced for converting a circuit net list to a layout has been extended upwards to the architectural level to provide for automatic, high-performance compilation of systolic designs for digital signal processing. As mentioned earlier,

comprehensive verification of circuit style and circuit performance has been introduced to ensure the correctness of designs, and design representation of alignment methodologies provide for automatic consistency between all levels of representation. Finally, the principal investigator has recently completed a comprehensive journal article on performance-directed synthesis of VLSI systems which will appear soon in the *Proceedings of the IEEE.*

Statement of Work

In order to build an appropriate CAD environment for the design of high-performance digital signal processing circuits, we have initiated a wide variety of student projects aimed at the various aspects of design, as discussed in the previous section.

At the language level, we continue the development of special purpose languages for digital signal processing. The first work in this area was done by Kopec in his signal representation language (SRL), and this work was further extended in the direction of design exploration by Miranker's doctoral thesis. Kuo, also working under this contract, showed how to introduce the formal specification of systolic algorithms, and Baltus has combined this work with aspects of data flow specification languages to provide a new design specification language ideally suited for systolic implementations where circuit-level performance optimization must be performed.

In the area of architectural exploration, a variety of techniques are being explored. Miranker showed how to do systematic space-time trade-offs at the architectural level, and Hauck has used retiming transformations, originally introduced by Leiserson, to systematically investigate performance enhancements due to pipelining as a function of the circuit performance of the particular technology and circuit style being implemented. Signal flow graphs can be systematically converted to a variety of systolic implementations, as investigated by Kuo, and Prasanna has devised algorithms for investigating the performance of FFT and filter implementations at the architectural level in terms of space-time trade-offs. Recently, Kaplan showed how pass transistor circuit styles could improve the area and speed of CMOS circuits, providing yet another tool for the exploration of circuit performance. The circuit-to-layout program developed by Baltus has specific provision for the optimal specification of transistor width, thus allowing for the optimal layout of high-performance circuits with widely varying transistor size. Finally, work by Lin and Reichelt on compaction may be viewed as a particular form of exploration at the layout level, where minimum area is the goal.

The generation of compiled cells from a high-level specification has been a major theme of this work. The procedural generation of layout was first introduced at MIT using the Design Procedure Language (DPL). More recently, Bamji introduced a regular structure generator which permits the ready generation of layout from a module cell library, where special means are provided for the specification of local interconnect, as well as the overall architectural style. This tool has been very successful for the generation of programmed logic arrays, array multipliers, register files, and other structures which are quasi-regular, but which must be idiosyncratically parameterized according to the needs of the particular problem. Baltus has also demonstrated how to compile systolic specifications to the circuit level, and then to layout using his previously developed layout program. The use of the circuit level as an intermediate level of specification is useful because of the optimizations, largely of transistor size, which can be performed at that level.

Over several years, there has been consistent emphasis under this contract on the efficient and accurate characterization of circuit performance. Matson used Hamiltonian techniques for optimizing and predicting the delay of circuits, and a variety of workers (including Penfield and Wyatt) have introduced fundamental waveform bounding techniques for efficiently characterizing delay in interconnect structures as well as nonlinear circuits. More recently, there has been new emphasis on macromodelling of CMOS circuits, as evidenced by Brocco's work, and the extension of these techniques by McCormick, who also used the moment specification of waveforms to effectively characterize a variety of circuit properties, including the important case of noise coupling. McCormick has also introduced circuit characterization and exploration techniques for the systematic minimization of nodule capacitance, and hence, increase in circuit speed.

Verification techniques have been introduced by Bamji for circuit style, and have been extended by Van Aelten for a variety of nonstructural circuit constraints. This is the first work where formal grammars have been used for the efficient verification of VLSI circuits. For very high-performance circuits, Reichelt has introduced new simulation techniques which provide fundamental device-level simulation than can be incorporated into circuit-level simulators, where the closed-form characterization of devices is insufficient for specifying very high-performance circuit behavior.

Finally, the interaction of design at the various levels of representation (ranging from the high-level language specification through architecture, logic, circuit, and layout) has been systematically attacked by Armstrong. When incremental changes are made at one level of representation, it must be possible to consistently align all other levels of representation, so that each level is a correct projection of one overall design. Coupled with this process must also be the capability for performance optimization through design exploration at each representational level. This work has advanced a great deal, and will serve as the overall system backbone for a coherent and integrated CAD system that is capable of designing high-performance digital signal processing circuits.

Status of Research

Building on the previous section, the status of research associated with the various themes of this contract is characterized below.

In the area, of functional specification languages, we continue to build on the work by Kopec on signal representation languages. This work was the first to look carefully at the semantic foundations of such specification languages, and to clarify the nature of fundamental concepts such as signal and waveform. This work has been extended by Kuo, who treats the signal flow graph as a canonical form for digital signal processing circuits. He is then able to show how to systematically transform from any signal flow representation to a corresponding systolic implementation, and in fact, to even vary the systolic implementations along several performance specifications. The way in which these specifications can be changed is constrained by factors systematically studied by Miranker in his doctoral thesis. Now, in a continuing study, Baltus is showing how to build up from the circuit level to the architectural level of specification in a way that brings together the earlier work of functional language specifications with techniques of design exploration and coupling to the circuit level of representation, which can then be optimally transferred to layout.

At the level of design exploration, the overwhelming emphasis under this contract has been in the use of the retiming tool by Hauck et al. to improve throughput in digital signal processing tasks. It it interesting to see that this technique is now being exploited by people in the area of logic synthesis research, who are moving registers via retiming to the periphery of circuits in order to allow the use of combinatorial logic optimization techniques in designs that are initially presented in a sequential way. In addition, at the architectural level, Prasanna has been studying Fourier transform and filter specification under a variety of constraints of available processors and memory. Some architectures considered in this study are systolic, whereas other are shared memory implementations, which are becoming increasingly prevalent in multiprocessor architectures. This is an ongoing study, and one that promises to provide considerable general understanding. As design exploration progresses, it is important to verify that the designs are still characterized by the initial input functionality. Thus, changes at module boundaries may introduce differences in circuits which must be appropriately verified. Bamji has introduced formal grammar techniques for this purpose which are exceedingly efficient and fundamental. For example, the static CMOS circuit style can be characterized by no more than five simple grammatical rules which produce an infinite number of possible designs. Van Aelten has gone on to show how charge sharing, ratioing considerations, and races can be adequately detected by additional rules which are formulated by using techniques of denotational semantics. From these comments, it is clear that a wide variety of exploration and coupled verification techniques have been introduced and explained under this contract.

Cell generation techniques, as previously mentioned, have been introduced by Bamji in a way that builds naturally on the overall circuit hierarchy. VLSI designs, particularly for signal processing, are often quasi-regular, and hence, can be built from a small number of parameterized cells. The systematic design of a pipelined array multiplier is a good example of this application, and Bamji's regular structure generator has indicated how these layouts can be efficiently generated, as well as accommodate the use of retiming transformations which are essential for obtaining optimum circuit throughput in the context of a wide variety of circuit implementation technologies. In addition to Bamji's work, Baltus has introduced a program called SOLO which automatically converts any MOS circuit net list to an efficient layout, using state-of-the-art compaction techniques. This program is remarkable, since the input can be constrained in terms of the aspect ratio and the connection points, both NMOS and CMOS are accommodated, and the natural hierarchy of the design can be effectively used.

In order to design high-performance circuits, it is essential to be able to generate layouts automatically, as previously described, from high-level specifications. Only at the layout can circuit performance be adequately characterized. McCormick has devised a very high-accuracy circuit extraction algorithm with an easy coupling to SPICE for circuit simulation. Brocco has gone on to devise ways in which CMOS circuits can be macromodelled for delay, using a small number of parameters, and providing accuracies within 5% of SPICE results for restoring circuits, and less than 10% error from SPICE in the case of pass transistor circuits. McCormick has extended the macromodelling techniques in his recent doctoral thesis, and has also shown how to use the Taylor series moments corresponding to the Laplace transform of a waveform to efficiently characterize a wide variety of circuit properties, most significantly noise coupling between adjacent circuits by fringe capacitance. These techniques have also been unified with previous work on waveform bounding by Wyatt, so that macromodelling, waveform bounding, and circuit extraction are now theoretically cohesive.

The newest work under this contract involves the verification and consistency maintenance of multilevel design specifications. Earlier, it was pointed out that design is often carried out at several different levels of representation simultaneously. These include the high-level functional specification, architectural register transfer specifications, logic specifications, circuit design, and layout representation. Each of these levels permits optimizations of many sorts, but when an optimization is performed at one level, care must be taken to make certain that the other levels of representation are still consistent with the new optimization, so that each level is a consistent projection one, and only one, underlying design. Bamji, in his doctoral thesis, has introduced a tool called SCHEMILAR, which allows grammars for both layout and circuit representations to be coupled so that their consistency and proper alignment can be checked by parsing methodologies. This is a strikingly new technique that is exceedingly fundamental. Armstrong, in an ongoing study, is introducing basic formulations for all representational layers so that perturbations at one level of representation can automatically be projected to implied perturbations at other levels of representation. This work is sufficiently fundamental that new levels of abstraction, as yet not conceived, can be easily accommodated in the overall approach to this problem. We believe this consistency maintenance capability must be fundamental to any overall CAD scheme, where heretofore only *ad hoc* approaches to this problem have been available. Hence, the ability to consistently align representations, optimize the individual representations within this framework, and produce high-quality layout will be possible in a theoretically coherent way.

Much of the overall viewpoint of this project is presented in a large review paper by the principal investigator titled "Performance-Directed Synthesis for VLSI Systems," that will appear in the February 1990 issue of the *Proceedings of the IEEE*. This paper presents an overall, coordinated view of performance optimization within a synthesis paradigm, reviews the large amount of work that has taken place in this field, and presents an overall strategy for correct systems.

The impact of the research under this contract has been substantial, both through publications and through the many professional involvements of the principal investigator. He serves on the Program Committee of the Custom Integrated Circuit Conference, the Design Automation Conference, and the International Conference on Computer-Aided Design. In addition, he is on the Administrative Committee of the IEEE Circuits and Systems Society, and is also on the VLSI Technical Subcommittee of the Acoustics, Speech, and Signal Processing Society. These many involvements have ensured both a modern perspective in the research undertaken, as well as the opportunity to disseminate the results of this research to a broad industrial and academic audience.

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