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HETEROJUNCTION BIPOLAR TRANSISTOR TECHNOLOGY

FINAL TECHNICAL REPORT FOR THE PERIOD
September 15, 1984 through September 14, 1986

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TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

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LIST OF FIGURES

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1.0 INTRODUCTION AND SUMMARY

This document is the final report detailing progress realized during the period 9/15/84 to 9/15/86 under the program "Heterojunction Bipolar Transistor Technology for High-Speed, Low-Power MSI Digital Circuits," Contract No. N00014-84-C-0480, at Rockwell International.

Prior to the start of this program, the demonstrations of high-speed ECL-type circuits in GaAlAs/GaAs HBT technology had been limited to a few very small circuits such as ring oscillators and frequency dividers. The high operating frequency of those circuits, the prospects of relatively straightforward scale-up to higher integration levels, and the projections of much higher possible speeds according to simulations indicated that the ECL approach with HBTs was worthwhile exploring further. A key objective in the formulation of the present program was to identify any major stumbling blocks that might prevent the technology from being later inserted into systems, including major yield or uniformity problems, reliability or radiation hardness issues, excessive temperature sensitivity, etc. Another objective was to investigate whether HBT circuits could lead to major improvements in the speed/power/noise performance of interchip communication circuits (output drivers and receivers) with respect to GaAs MESFET circuits, by making use of the high drive capability of bipolars (particularly in conjunction with complementary output circuits to eliminate the common-ground inductance noise). A final objective was to demonstrate applications-oriented HBT circuits with state-of-the-art performance. Accordingly, there were three tasks within the program.

Task 1.   HBT Technology Development

Refine and develop HBT technology for the fabrication of circuits using the ECL approach, and characterize its associated yield, uniformity, reproducibility, temperature sensitivity, reliability and radiation hardness.

Task 2.   MSI Circuit Development

Design, fabricate and test two MSI-level circuits (containing more than 100 gates) based on HBT ECL.

Task 3.   Interchip Communication Development

Study interchip communication protocols, and design, fabricate and test two types of protocol test chips to demonstrate fast, low-power and low-noise communications. The chips are to include both an asynchronous and a synchronous circuit.

The objectives of the program were all successfully met. HBT process technology was improved significantly by introducing the use of projection lithography (to supplant the earlier contact lithography), and by developing the technology needed for uniform and reproducible selective etching, which proved superior to implantation for base contacting. Transistor f_t's as high as 40 GHz were measured. The uniformity of the threshold voltage V_{be} corresponded to a 2.5 mV standard deviation across a wafer. Yields on the best wafer were 30% for circuits with 108 equivalent NOR gate complexity. Preliminary total dose hardness was found to be on the order of 50 Mrads. Preliminary reliability demonstrations were made, with 1500 h at 100°C without failure.

A preferred circuit approach within the ECL family was adopted and studied extensively: differentially routed, series-gated current-mode logic (CML). This circuit family enables compact structures to be formed with considerable logic power, leading to savings in power and area with respect to conventional ECL. Its differential structure also makes it highly insensitive to temperature, power supply voltage, power supply variations, etc. A nominal macro with a complexity of three NOR gates used a total power of 4.5 mW (1.5 mW/gate).

With this approach, three MIS circuits were designed and simulated during the program: an 8-bit universal shift register; and 8:1 multiplexer (MUX); and a 1:8 demultiplexer (DEMUX). The first two designs were processed. The 8-bit universal shift register was fully functional (with a yield up to 30%) and operated with a clock frequency up to 3.2 GHz, the fastest universal shift register ever reported. Power consumption was 700 mW. The 8:1 MUX was not fully functional because of a layout error. The synchronization output was produced properly, which confirmed that the high-speed portion of the circuit operated at a 3.2 GHz clock rate.

A variety of output driver and input receiver designs were also studied by simulation. Three circuit types - two corresponding to ECL (-0.9 to -1.7 V) levels and one corresponding to CML (0 to -0.8 V) - were laid out. They were incorporated, among others, in protocol test chips, which were SSI circuits with 10-20 gates of logic. The

synchronous test chip was a 3-bit D-register. The asynchronous test chip was a gated full-adder circuit. The protocol test chips with the various driver circuits were all fully functional with yields above 50%, and produced the expected output voltage levels with risetimes as low as 200 ps for the fastest case.

The results of this program demonstrate that ECL circuits implemented with GaAlAs/GaAs HBTs must be considered one of the leading candidates for the implementation of very high-speed MSI digital functions. Moreover, there is still ample room for scaling and technology improvement over what has been demonstrated in this program.

The remainder of this report has the following organization: Section 2.0 reviews the HBT basic structure and operation; Section 3.0 describes MBE growth of HBT epitaxial structures; Section 4.0 describes HBT processing; Section 5.0 discusses methodology of HBT testing, characteristics and analysis; Section 6.0 covers HBT modeling; and Section 7.0 details the design and performance of ICs based on HBTs. Finally, Section 8.0 provides an overall summary of the status of HBT technology and indications of work remaining to be done.

2.0 HBT STRUCTURE

This section describes the structure of HBTs investigated in this program. Both the vertical (epitaxial) structure and the lateral geometry are described.

2.1 Vertical Structure

The epitaxial HBT layer structure used on this program is shown in Fig. 1. The device layers include the following: (a) Cap layers of GaAs, InAs or graded composition InGaAs to assist in forming ohmic contacts. The uppermost layer, for the emitter contact, is highly doped (2×10^{19} cm^{-3}). (b) An emitter layer of $Al_xGa_{1-x}As$ with $x = 0.25$ doped n-type with $N_D \approx 5 \times 10^{17}$ cm^{-3}. The composition chosen provides the benefit of high emitter injection efficiency from a wide band gap emitter, but does not incur problems from high deep-level concentration or indirect band gap associated with greater Al content. The composition near the emitter-base junction is carefully graded to avoid the formation of potential barriers. (c) A base layer of GaAs or InGaAs of thickness about 1200Å doped with Be acceptors at a concentration of 5×10^{18} cm^{-3}. (d) A collector drift region whose doping is chosen to avoid base pushout (Kirk effect) at the current densities of interest (10^4-10^5 A/cm^2) while maintaining low base-collector capacitance, and whose thickness is adjusted according to the desired operating voltage (> 0.5 µm for 10 V breakdown). (e) A heavily doped subcollector region to allow contacting the collector. (f) A semi-insulating substrate, which permits fully isolated transistors to be formed, and provides considerably greater circuit flexibility than reported I^2L structures.
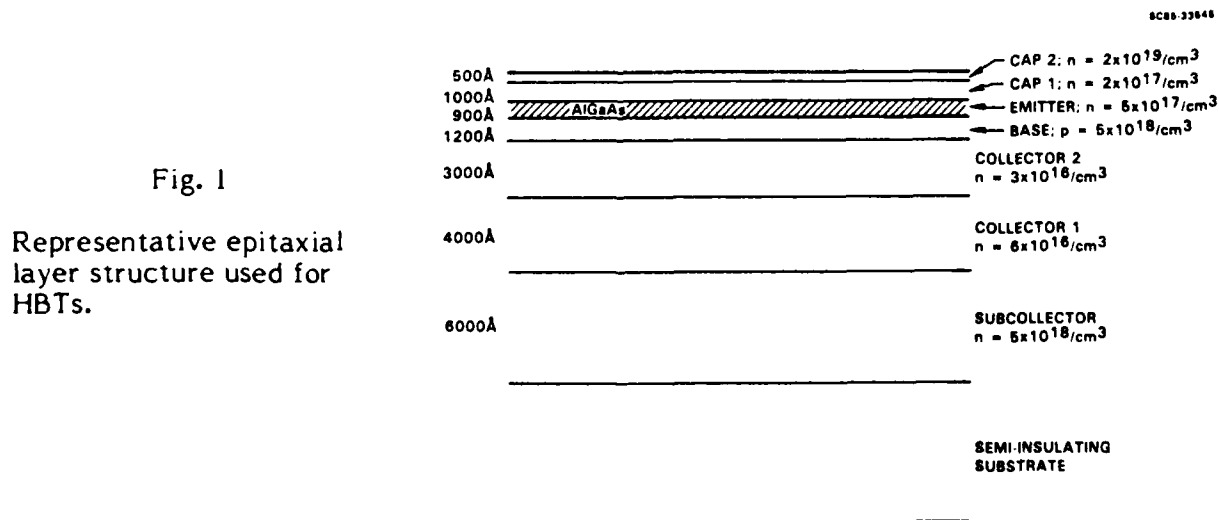
Fig. 1

Representative epitaxial layer structure used for HBTs.

500Å	CAP 2: n = 2×10^{19}/cm^3
	CAP 1: n = 2×10^{17}/cm^3
1000Å	
900Å	AlGaAs — EMITTER: n = 5×10^{17}/cm^3
1200Å	BASE: p = 5×10^{18}/cm^3
3000Å	COLLECTOR 2 n = 3×10^{16}/cm^3
4000Å	COLLECTOR 1 n = 6×10^{16}/cm^3
6000Å	SUBCOLLECTOR n = 5×10^{18}/cm^3
	SEMI-INSULATING SUBSTRATE

This structure is formed by MBE with excellent reproducibility. With this design, transistor operation is obtained in a manner similar to Si bipolar devices, but with reduced transit time, lower base sheet resistance, lower emitter-base capacitance, lower output conductance and higher current density. To appreciate the improvement obtainable, the factors affecting transit time (or f_t) are briefly considered. The overall electron transit time τ_{ec} is given by a sum of components corresponding to the different device layers:

$$\tau_{ec} = \tau_e + \tau_b + \tau_{cscl} + \tau_c \quad .$$

Here, τ_e is the emitter junction capacitance charging time, τ_b is the base transit time, τ_{cscl} is one-half the collector depletion region transit time, and τ_c is the collector capacitance charging time. In well-designed HBTs, all components tend to be important (otherwise, typically, tradeoffs may be used to reduce the largest). In comparison with homojunction devices, τ_e in HBTs is lower because of low emitter doping, and because of high operating current density (yielding low dynamic junction resistance); τ_b is lower because of high electron mobility, and because built-in drift fields based on AlAs or InAs concentration gradients may be used; τ_{cscl} is lower because of electron velocity overshoot effects as the electrons enter the base-collector junction region; and τ_c is lower, as is τ_e, due to the higher current density operation.

Quantitative estimates of τ_{ec} have been made, based on full solution in one dimension of the transport equations for electrons and holes. Figure 2 shows predicted f_t as a function of operating current density for some representative structures. It is of interest to note that different layer thicknesses and dopings are optimal in different regimes of current density (and thus power dissipation), implying somewhat different MBE structures for high complexity and low complexity quantizers.

2.2   Lateral Structure

There are two approaches to lay out emitters for bipolar transistors: the walled-emitter structure and the island-emitter structure. The walled-emitter approach is more advantageous because emitter contact fingers have no crossover with extrinsic bases, and therefore there is no need to passivate extrinsic bases to prevent emitter-base shorts. Interconnection metal can easily contact emitters without an additional

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Fig. 2

Predicted cutoff frequency, f_t, for HBTs vs collector current density showing effects of velocity overshoot and base doping.
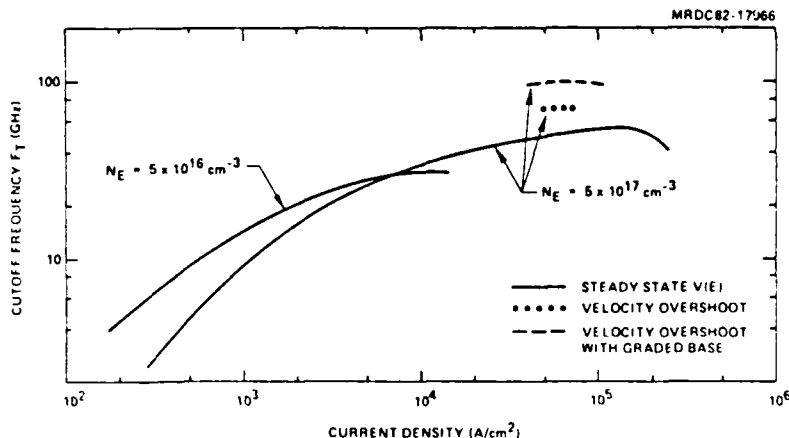
dielectric opening step, allowing small emitter dimensions and eliminating any step coverage issue. However, the straightforward walled-emitter HBT has an associated problem. Since the edges of emitters are partially shared by the damaged isolation regions, injected minority carriers can partially recombine at active/isolation interfaces. This leads to a problem of low current gain in HBTs with scaled emitter lengths. It is presently difficult to passivate these edges adequately. As a result, we have chosen an island-emitter structure to keep active emitter areas away from peripheral isolation edges.

Figure 3 illustrates schematically the walled-emitter and island-emitter layouts. Both were investigated as part of this program.

(a)

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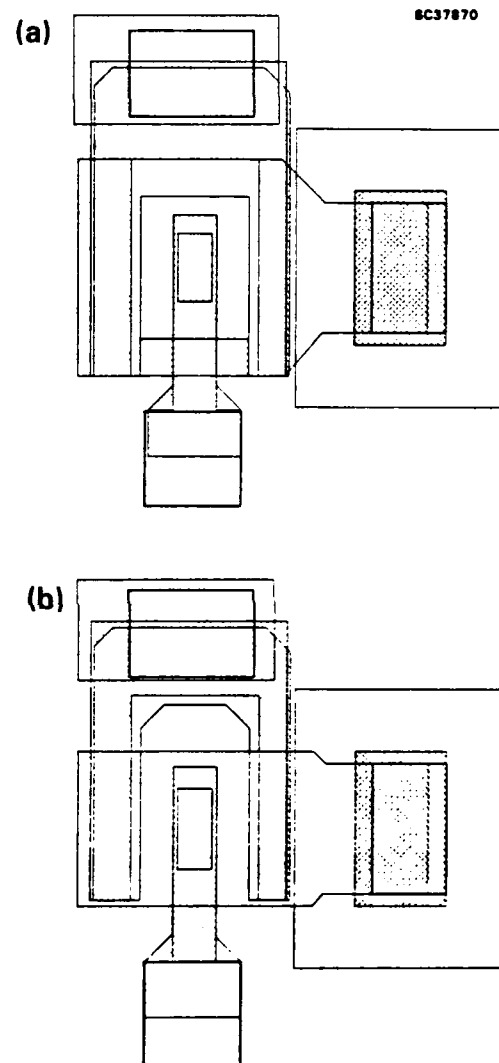
Fig. 3

Comparison of transistor layout for
devices with (a) walled-emitter
structure and (b) island emitter
structure.

(b)

3.0 HBT MATERIAL GROWTH

During this reporting period, 25 epitaxial HBT wafers were grown by MBE for this project. The wafers were grown for use in HBT circuit and process development, as well as experiments to investigate the effect of structural variations on device and circuit performance and yield.

3.1 HBT Epitaxial Layer Structures

Figure 1 shown previously illustrates the basic HBT structure grown for this project, which we have labeled SS4. This structure has been developed under other government contracts and company internal funding prior to the start of this project, and has been found to produce operating HBT devices and circuits. Several variations to this (SS4) structure were made in an attempt to optimize it for circuit development. These include variations in the degree of setback of the base doping from the emitter-base junction, the doping density in the base, and the ramp profile in the composition graded emitter-base junction region. Table 1 lists the wafers grown and the variations from SS4 that were made.

Table 1

Epitaxial Structures Grown

Structure	Run Numbers	Comments
SS4 for Censor, Lower Base Doping	1231,1235,1236,1238,1239 1241,1250,1251,1252,1253 1254,1255,1256,1257,1259	Base = $2.3 \times 10^{18}/cm^3$ 150Å base doping setback
SS4 Not for Censor	1233,1234,1237,1240	Base = $2.3 \times 10^{18}/cm^3$ 150Å base doping setback
SS4 Standard	1265,1266,1267,1268,1269	100Å base doping setback
Experimental SS4	1270 1271 1272	Base = $2 \times 10^{18}/cm^3$ Base = $2 \times 10^{19}/cm^3$ Base = $2 \times 10^{19}/cm^3$

Variations in base doping (from 2×10^{18} to $2 \times 10^{19}/cm^3$) and base doping setback (100 and 150Å) were made due to uncertainty in the amount of Be diffusion occurring during growth. We and others have found previously that significant diffusion of Be may occur during epitaxial growth and, in some cases, during subsequent processing. This can displace the emitter-base heterojunction into the wider gap aIGaAs, which can decrease device gain. The amount of diffusion depends strongly on Be concentration and growth conditions. The inclusion of a doping setback of 100 to 150Å is an attempt to minimize as well as study the effect of this diffusion. So far, however, processing variations appear to have masked the effect of setback variations, since device gain appears not to be correlated with it.

For these epitaxial layers, an improved emitter-base compositional ramp was used. Device electron and hole current simulations using the simulation program SEDAN suggested this more rapid grading profile, in comparison to the profile used previously. The grading profile is created in the MBE growth by holding the Ga flux at a constant value while rapidly increasing the Al over temperature in such a way as to create the desired Al flux profile, as calculated from the desired alloy composition profile. The Al oven temperature ramp is computer-controlled for repeatability (as are all aspects of the MBE growth). Figure 4 shows the desired flux profile compared to the actual Al flux profile as measured by the MBE beam flux monitor. The agreement is reasonably good. The grading corresponds to an $Al_xGa_{1-x}As$ composition increase from x = 0.00 to x = 0.20 in about 385Å.

For purposes of process development, the proper crystallographic orientation of the epitaxial wafers was needed to use the Censor 10X projection mask aligner. The epitaxial growths for this project are done on quarters of 3 in. GaAs wafers, created by cleaving the wafer in four pieces. The Censor mask aligner holds these pieces in a jig, in which the straight sides of the piece rest against alignment pins. Thus, the azimuthal orientation of each piece in the Censor aligner will be determined by the quadrant of the 3 in. wafer from which it was taken. Our HBT process relies on a direction-selective chemical etch to create collector contact wells with controllably sloped sidewalls. Thus, only two of the four possible azimuthal orientations of 3 in. wafer quadrants are usable on the Censor mask aligner. The azimuthal orientation of the 3 in. wafer could be determined from the location of the major and minor flats, and the cleaved quadrants were marked as suitable or unsuitable for use with the Censor aligner.

Fig. 4

Al flux profile for SS4 emitter.
Solid line: desired profile;
dashed line: profile measured.
Time is measured from the open-
ing of the Al shutter.
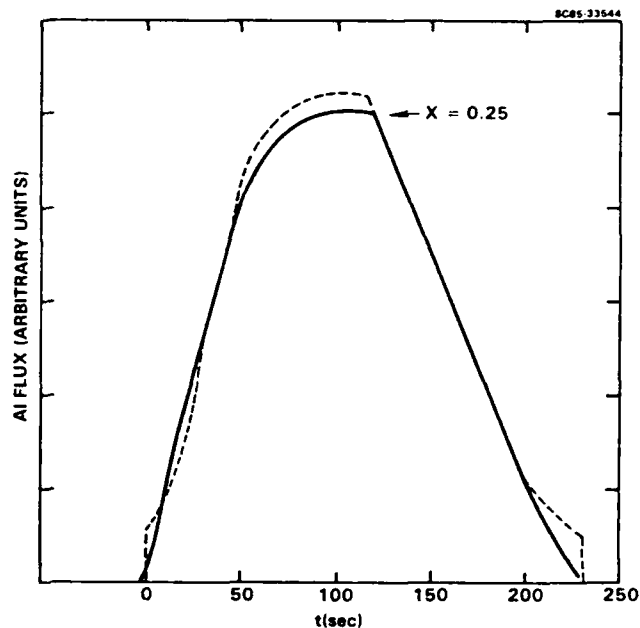
3.2   MBE Calibrations

The methods used for calibration of the MBE process are extremely important, since they determine the accuracy with which the actual epitaxy reproduces the desired structure. For these epitaxial layers, reflection high energy electron diffraction (RHEED) intensity oscillations were used to rapidly determine growth rates and alloy composition for HBT structures with very high accuracy.

The method of using RHEED intensity oscillations for growth rate calibrations has been developed elsewhere and described extensively in the literature. It takes advantage of the strong periodic oscillations in diffraction intensity which the layer-by-layer growth habit of MBE produces in the intensity of certain spots of the RHEED pattern during growth. The period of these oscillations corresponds exactly to the time for growth of a single GaAs (or AlAs) layer. The measurement of these oscillations is straightforward and rapid, so that a growth rate determination accurate to $\pm 3\%$ may typically be obtained in 30 min. This makes daily growth rate calibrations a practical procedure. $Al_xGa_{1-x}As$ alloy compositions may be determined from GaAs and AlGaAs growth rates. Since layer thicknesses are determined by growth rate multiplied by growth time, such calibrations result in extremely accurate epitaxial layer thicknesses.

An example of the epitaxial layer thickness accuracy is shown in Table 2. HBT structures were etched selectively by methods developed for device processing for this project. The etching stopped at the interface between the GaAs contact cap layers (nominal depth 1500Å) and the AlGaAs emitter for the CCl_2F_2 etch, and at the AlGaAs-base interface (nominal depth 2400Å). The average depths measured by surface profilometer were 1521Å and 2311Å, for errors of +1.4% and -3.7%, respectively. This indicates that not only were excellent selective etches developed, but that the epitaxial layer growth thickness was very accurate.

Table 2
Etch Depths of Selectively Etched SS4 HBT Structures

Stopping Point	Nominal Depth (Å)	Measured Depth (Å)	Deviation (ave.)
Cap 1-Emitter Interface	1500	1558 1497 1508	+1.4%
Emitter-Base Interface	2400	2292 2259 2380 2314	-3.7%

Doping densities for the epitaxial structures were measured by more traditional methods. Hall measurements of the free carrier concentrations of specially grown calibration layers were the primary method of calibrating both the n-type Si doping and the p-type Be doping. The n-type doping of layers within a device structure was checked by using an electrolytic profiles, the Polaron profile plotter, to profile the doping in special structures grown on conducting n^+ substrates. These structures were identical to HBT structures, with the exception that the base was undoped and the heaving doping in the topmost GaAs cap layer was omitted. These changes allowed accurate profiling of the n-type doping in the remaining layers. Figure 5 shows such a profile.
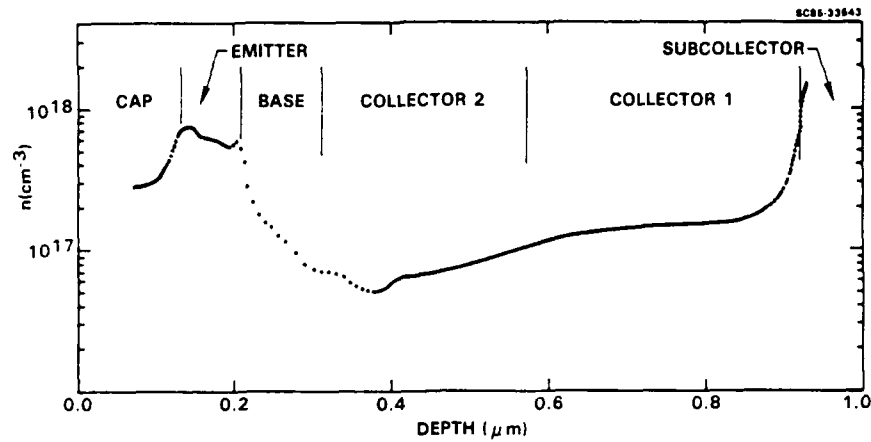
Fig. 5   Polaron profile plot of n-type doping as a function of depth from the surface of the wafer, for HBT structure SS4 without any intentional doping in the base layer. Resolution degrades with depth.

4.0 HBT PROCESSING

4.1 Process Approach

During the contract period, significant progress has been made in the fabrication technology of HBT ICs. Three mask sets, HB2, DB1 and DB2, have been used for circuit fabrication. The main reason for processing HB2 wafers was to improve the existing HBT process (the quasi-planar approach) and to experiment with new device ideas. Device and circuit design rules were revised based on the performance and yield information of those SSI circuits of HB2 wafers. The subsequent DB1 mask was the first mask set for HBT MSI circuits, and the new design rules were implemented. In the second MSI mask set (DB2) of HBTs, several layout errors found on DB1 masks were corrected and new circuits consisting of island emitter HBTs were included (in addition to circuits implemented with walled emitter HBTs). By using a recently developed self-aligned base contact process, we can fabricated both walled emitter and island emitter HBT circuits with the same masks, and therefore a direct comparison can be made between two circuits of the same architecture with transistors having different geometry. The difference in processing between the quasi-planar device (based extensively on ion implantation) and the self-aligned base contact device (based on selective etching) is explained below.

In the earlier stage of the program, devices were fabricated by a quasi-planar process based on ion implantations. A cross section of the device is shown in Fig. 6a. A shallow etch step was used to remove the top n^+ cap layer; Be implantation was used to assist in contacting the buried base layer. Oxygen implants were employed to decrease the extrinsic base-collector capacitance. The basic quasi-planar process did not have self-alignment features, insofar as three masking manipulation were used for base implant, emitter contact and base contact. However, an advanced self-aligned quasi-planar HBT process using a substitutional emitter process has also been successfully developed under a separate IR&D effort. The minimum linewidth of emitter fingers was 1.2 μm. The fastest nonthreshold ring oscillator made with quasi-planar transistors showed a propagation delay of 27.2 ps. A similarly fabricated CML ring oscillator had 33 ps per gate delay. The transistors also demonstrated good transconductance, cutoff frequency and excellent uniformity. The peak transconductance was higher than 7000 ms/mm, the cutoff frequency was 37 GHz, and the standard deviation of threshold

(a)

(b)

BE DOPED P REGIONS
OXYGEN IMPLANTED REGIONS
IMPLANT DAMAGE ISOLATION REGIONS

ADVANTAGES

* LOW BASE CONTACT RESISTANCE
* FLEXIBILITY OF LAYER STRUCTURE
* LOW C_{BC}

PROBLEMS

* DOPANT DIFFUSION
* ANNEAL UNIFORMITY
* PARASITIC BASE RESISTANCE

ADVANTAGES

* SIMPLER
* FASTER
* LOW TEMERATURE PROCESS ONLY

PROBLEMS

* ETCH CONTROL
* BASE CONTACT RESISTANCE
* CURRENT GAIN
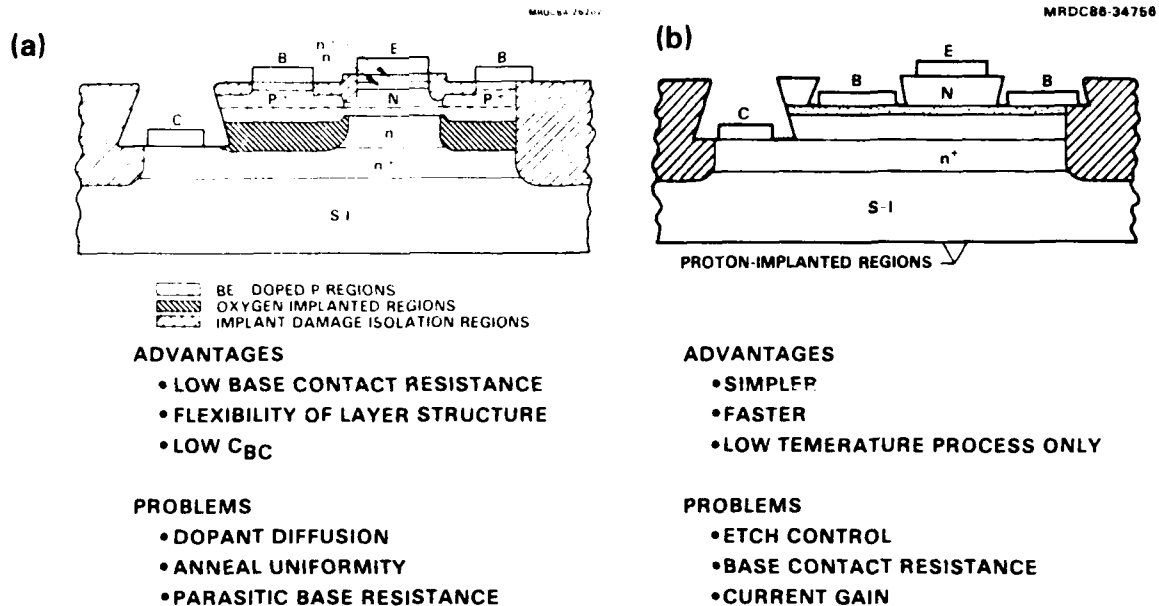
Fig. 6   Comparison of HBT structures produced with (a) quasi-planar, ion-implantation process; and (b) self-aligned base contact process.

voltages was less than 3 mV across a 1 in. wafer. The advantages of the quasi-planar process are low base contact resistance (lower 10^{-6} Ω-cm^2), flexibility in choice of base layer doping (the intrinsic base sheet resistance is about 1000 to 2000 Ω/sq, but the sheet resistance of extrinsic bases can be as low as 200 Ω/sq due to the p-implantation) and the low C_{oc}. The disadvantages of the quasi-planar process are the base dopand diffusion and redistribution during annealing, problems of activation uniformity, and reproducibility of the annealing. In our laboratory, annealing was carried out in a flash annealer manufactured by AG Associates.

Due to the complexity of the quasi-planar process, its manufacturability is lower than that of a self-aligned base contact process which was developed in the latter stage of the contract period. The cross-sectional structure of a self-aligned base contact transistor is shown in Fig. 6b. The self-aligned base contact process was made possible by a selective etching technique, which can self-stop precisely at the emitter/base interface. Excellent uniformity and reproducibility have been achieved by selective etching, as shown in Fig. 7. The etching depth target was 2300Å; the averaged etching depth fro Dektek measurements was 2433, 2492 and 2437Å for wafers 15E, 15F and 15G,

Fig. 7

Map of base etch depths measured
by surface profilometer techniques
for various HBT wafers.

15E
```
2442Å  2399Å  2410Å  2406Å
2494Å  2475Å  2431Å  2444Å
2426Å  2452Å  2416Å  2403Å
```
MEAN DEPTH $\bar{X}$ = 2433Å
σ = 29.7Å

15F
```
2511Å  2492Å  2448Å  2499Å
2437Å  2533Å  2500Å  2514Å
2476Å  2511Å  2489Å  2490Å
```
$\bar{X}$ = 2492Å
σ = 27.4Å

15G
```
2418Å  2398Å  2432Å  2430Å
2383Å  2447Å  2463Å  2530Å
2438Å  2412Å  2464Å
```
$\bar{X}$ = 2437Å
σ = 39.6Å
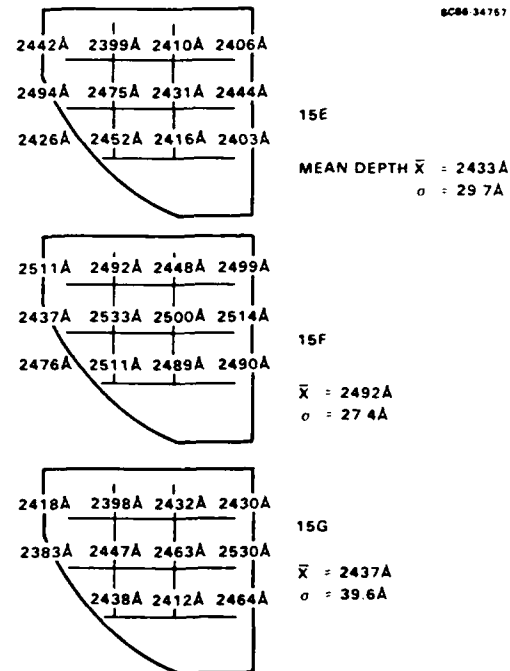
respectively. The largest standard deviation of etching depth measured across one-quarter of a 3 in. wafer is 39Å. It is noteworthy that we have overetched wafer 15F with an additional 60% of the required etching time to investigate the etching selectivity. Since the p^+ extrinsic base layer has been uncovered by a selective etching, the base ion implantation becomes optional in a self-aligned base contact scheme. For the sake of processing simplicity and due to the temperature limitation of the nonrefractory base ohmic metals, p-type implantation was not used in the self-aligned base contact process.

The baseline self-aligned base contact process has made fabrication of HBT ICs much simpler and more reproducible. There is no critical implantation/annealing; the highest processing temperature is the temperature of ohmic contact alloying (350°C). The standard deviation of threshold voltage distribution was less than 8 mV across a 3 in. wafer. Some changes in epitaxial layer structure are required for this process. The base doping was increased to 1×10^{19} to lower the base contact resistance. A compromise on the value of the base layer thickness is required to insure that the contact metallization does not penetrate into the collector region during alloying. These changes may result in a decrease in the gain of the devices. The detailed manufacturing steps of the self-aligned base contact process (which only requires eight mask levels) are illustrated in Fig. 8 and described as follows.

Fig. 8

Schematic processing steps
for self-aligned base,
island emitter HBTs.

(1) ISOLATION IMPLANT AND MESA ETCH THE N+ CAP LAYER.

(2) UNCOVER EXTRINSIC BASE REGIONS AND DEPOSIT BASE METAL

(3) DEFINE AND METALLIZE EMITTER CONTACT

(4) UNCOVER SUBCOLLECTOR AND DEPOSITE COLLECTOR METAL
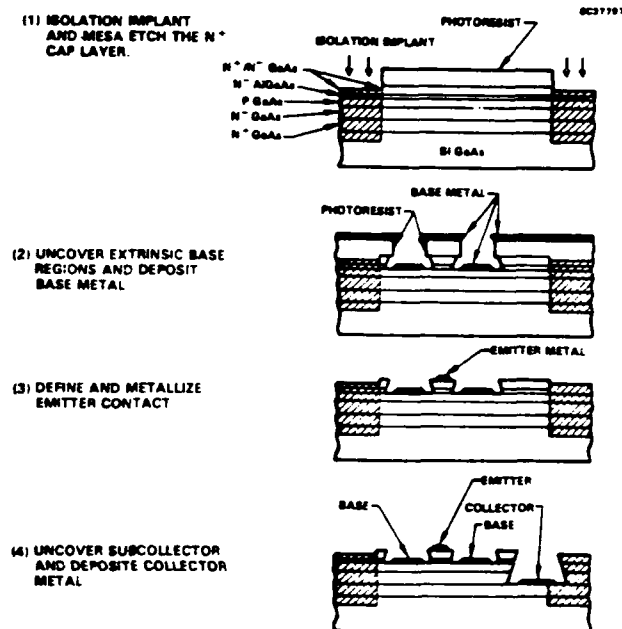
After device isolation by B/He bombardment, the cap GaAs layers and the AlGaAs emitter layer are removed by selective etching to uncover the extrinsic base region and define the active emitter region simultaneously. With the same photoresist pattern, base metals Au/ZnAu are evaporated and lifted off. Spatial separation between the deposited base metals and the emitter edge was achieved by undercutting (0.2 μm) during the base etching. The final emitter width was 2.0-2.5 μm in different devices and the total base width was 10 μm. After alloying, the base sheet resistance was 200 to 700 Ω/sq, corresponding to a base doping concentration of 2×10^{19} to 8×10^{19} cm^3. As previously shown with oxygen implant in the quasi-planar process, protons can be used for implantation into the extrinsic base region in the present process. Implantation-induced damage compensates the n-doping in the collector drift region below the base contacts. This decreases the extrinsic base-collector capacitance without any significant increase in base contact resistance. Via holes were etched into the wafer to make the contact to the buried collector layer. Circuits were completed with evaporated NiCr resistors and two levels of interconnector metal using an interlevel dielectric of PECVD Si_2Ni_4 or polyimide. Both first- and second-level metals (Ti/W/Au or Ti/Au) were sputtered to assure step coverage. The first-level metals were patterned with a liftoff method, but the second-level metals were delineated by an ion-milling process. Figure 9 illustrates the cross-section of a representative IC.

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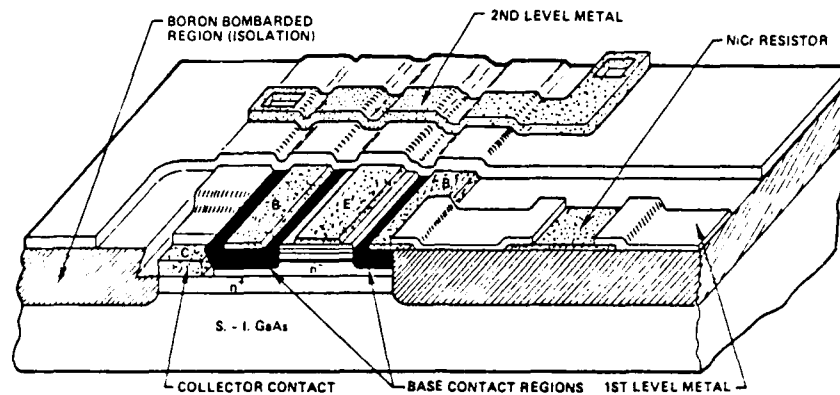
Fig. 9 IC cross-section for HBT process.

Transistors fabricated with the self-aligned base contact process have shown excellent transconductance, cutoff frequency and uniformity. Representative transistors had a peak transconductance higher than 10,000 ms/mm and a maximum current gain of 40. The best cutoff frequency f_t of baseline transistors (without proton implantation) was 35 GHz. By using proton-treated extrinsic base regions, the cutoff frequency has increased to 45 GHz. These results were derived from S-parameter measurements of HBTs with multiple emitter fingers of nominally 2.0 × 10 μm dimensions. The standard deviation of the threshold voltage distribution was 2.5 mV across a 1 in.^{2} wafer and 7.6 mV across a 3 in. wafer (Fig. 10a and 10b). Using 10X lithography with a Censor stepper, we have demonstrated MSI circuits of 290 transistors on a 3 in. MBE wafer. As mentioned earlier, transistor performance can be greatly improved by implanting protons into extrinsic base areas. We have so far tested this idea by demonstrating SSI circuits on 1 in.^{2} wafers with a contact aligner. Nevertheless, there should be no problem in applying the same idea using Censor lithography.

The earlier mask sets (HB2, DB1) employed walled emitter HBTs exclusively. The lateral structure of such transistors is shown in Fig. 3a. The advantages of a walled emitter structure are quite obvious: the emitter fingers have no crossover with extrinsic bases; therefore, there is no need for passivating extrinsic bases to prevent shorting to emitters. Furthermore, the metal electrode can easily contact the emitter without an additional dielectric opening step and without a step coverage problem. However, the walled emitter HBTs have their own disadvantages. The major problem is low current

gain. Since the top and bottom sides of the emitter are shared by the damaged isolation regions, injected minority carriers may partially recombine at the active/isolation region interfaces instead of flowing into the collector. To prevent carriers from such recombinations, the emitters should be kept far away from peripheral isolation edges. One of the possible arrangements is to lay out transistors with an island emitter geometry as shown in Fig. 3b. At the present time, a nonself-alignment process is used to fabricate MSI circuits made with island emitter transistors, as shown in Fig. 11. After the base metals were lifted off, a dielectric layer was deposited on the wafer surface. An additional masking operation is required to open windows for emitter contacts. The emitter metal can overlap the extrinsic base area or the base metal without any concern for emitter-base shorting because of the dielectric coverage. On the other hand, the development of the advanced self-alignment process (the dual-liftoff process) for island emitter transistors is an ongoing effort under DARPA millimeter-wave contract support. The initial success has been the demonstration of a high-performance 1/4 frequency divider with a maximum dividing frequency of 11.3 GHz. As the self-alignment technique becomes more mature, the process will be adopted for larger scale integrations.

4.2   Lithography

HBT fabrication processes developed at Rockwell have emphasized both performance and manufacturability. In the earlier stage of the program, most patterning work was based on optical lithography on relatively small wafers (0.75 to 1 in. on a side). Use of a 10X reduction projection mask aligner (Censor) has been developed with the support of the present contract, and wafers of a large size (~ 2 in. diagonal) have been employed routinely. More recently, we have also demonstrated the use of Censor lithography on a 3 in. MBE wafer with excellent device yield (100% functional HBTs of 88 devices sampled from 44 fields). The accuracy of Censor alignment on a representative 3 in. wafer is shown in a histogram of Fig. 12. In most of the fields, the misalignments were less than 2 μm. This value of alignment accuracy is also supported by the extensive work on MESFET-based ICs at Rockwell.

One problem associated with the Censor apparatus is the requirement for high contrast alignment marks which are viewed with monochromatic light (which can lead to interference effects). Alignment marks unique to each process must generally be

(a)

⁻22.123	6-SEP-85	VBE .1MA
.5.04		
.BE SCAN H4		AV=-1.164 V

2.5MM

VBE .1MA

AV=-1.164 V
SD=2.533E-03(.2%)
N=117/126

AV=-1.164 V
SD=2.533E-03(.2%)
N=117/126

1   2   3

20

≡ =-.50≠AV ··· =-.10≠AV ▨ =.20≠AV
≡ =-.40≠AV ··· =.00≠AV ▥ =.30≠AV
▨ =-.30≠AV ··· =.10≠AV ▥ =.40≠AV
·· =-.20≠AV ▥ >=.50≠AV

0   ·1.00E-03V   -2

VBE 1mA

AV=-1.247 V
SD=7.629E-03 V
N=83/??

(b) VBE SCAN H4 3 INCH

20

⊟<=-2.50≠Sd ▪ =-.50≠Sd ▪ =1.00≠Sd
⊟ =... ..≠Sd ▪ =.00≠Sd ⊞ =1.5 ≠Sd
⊟ =-1... ≠Sd ▪ =.50≠Sd ⊡ =. ...≠Sd
▪ =-1...≠Sd ▥ >=2.50≠Sd

-1.28   -1.26   -1.24   -1.22
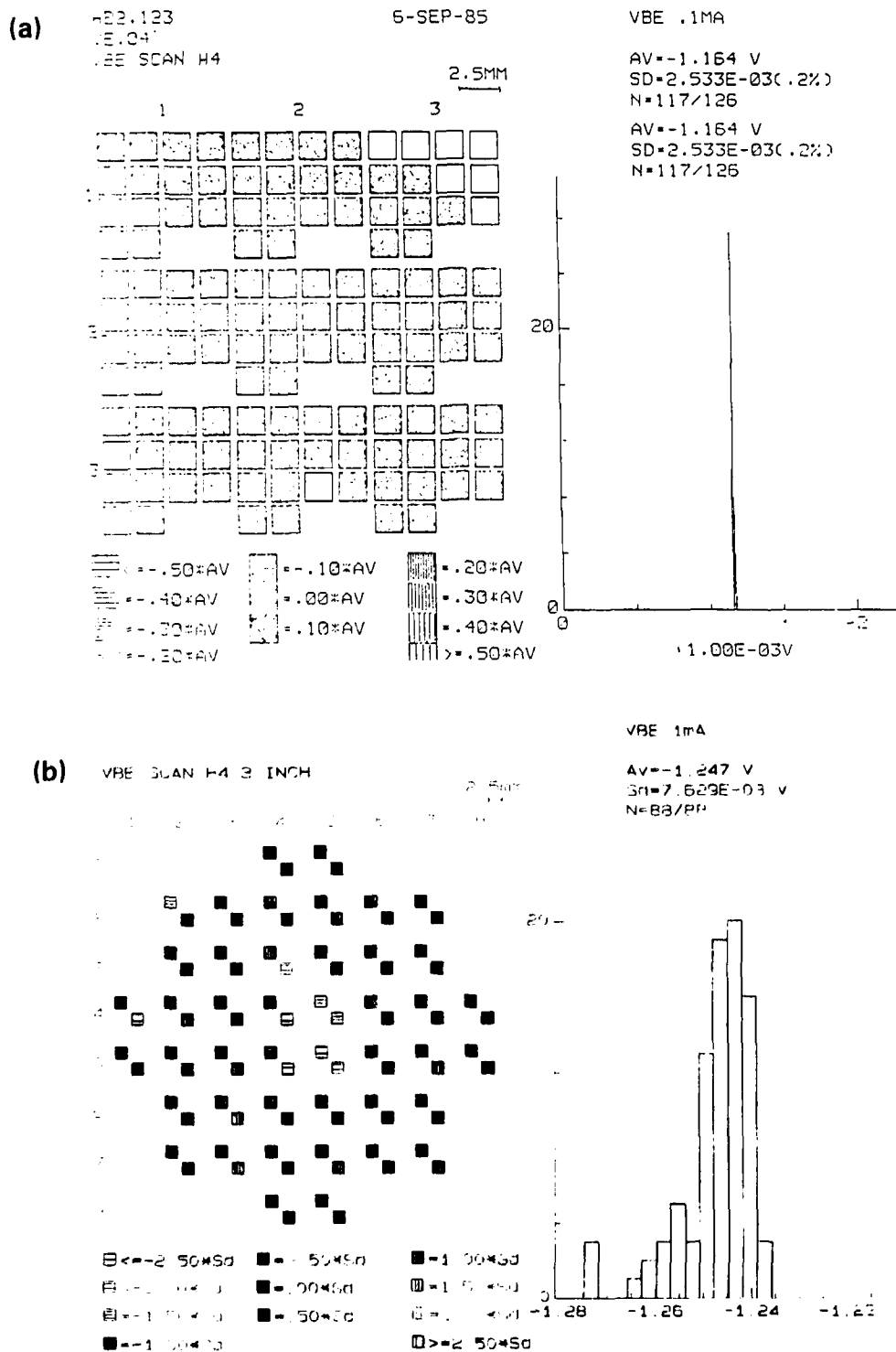
Fig. 10   Measured distribution of threshold voltage V_{BE} among HBTs fabricated with self-aligned base process across a 1 in² wafer (a) and across a 3 in. wafer (b).

(a)
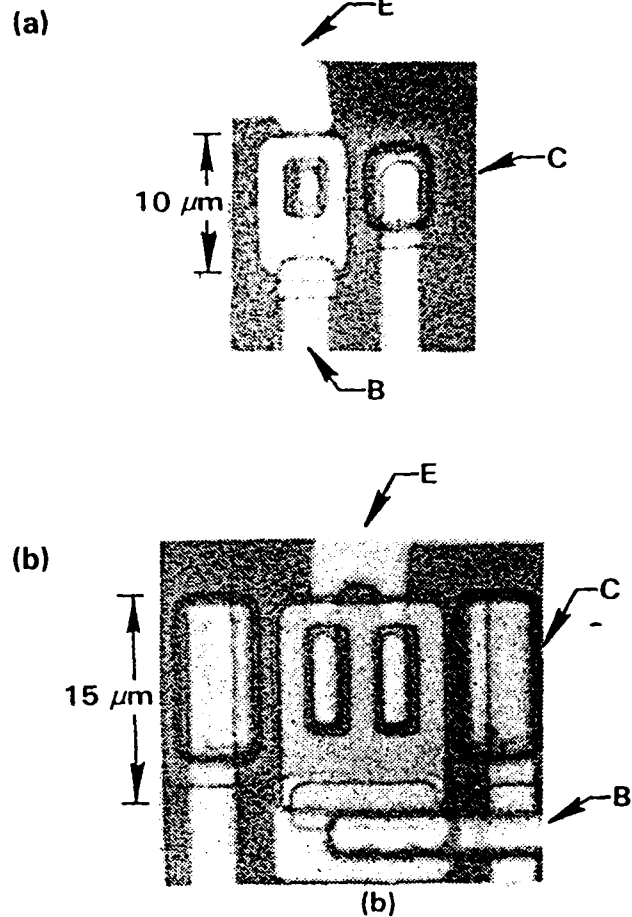
Fig. 11

Lateral structure of fabricated
island-emitter HBTs: (a) single
emitter switching transistor and
(b) dual-emitter output driver
transistor.

(b)

(b)

developed, since they must be compatible with all the processing steps. For example, alignment marks need to stand annealing temperatures (peak temperature 950°C) in a quasi-planar HBT approach. Some refractory metals or metalsilicides (such as W and WSi) may stand high temperature and not react with GaAs substrates; nevertheless, their optical reflectivities are not high enough for Censor operation. Our solution to this problem is to sandwich a highly reflective Au layer within dielectric layers: Si_3N_4 was first sputtered on the wafer surface. Alignment mark areas were defined by the photoresist. Ti/Au/Ti metal layers were evaporated, lifted off, thereby forming the alignment marks. Finally, another dielectric layer (usually CVD SiO_2) was deposited to cover the marks. Although the fabrication process was rather complex, we succeeded in building HBT circuits with these Si_3N_4/Ti/Au/Ti/SiO_2 marks. Figure 13 illustrates two extreme cases: the nonprotected alignment marks degraded during the rapid thermal annealing; however, the sandwiched marks remained intact.
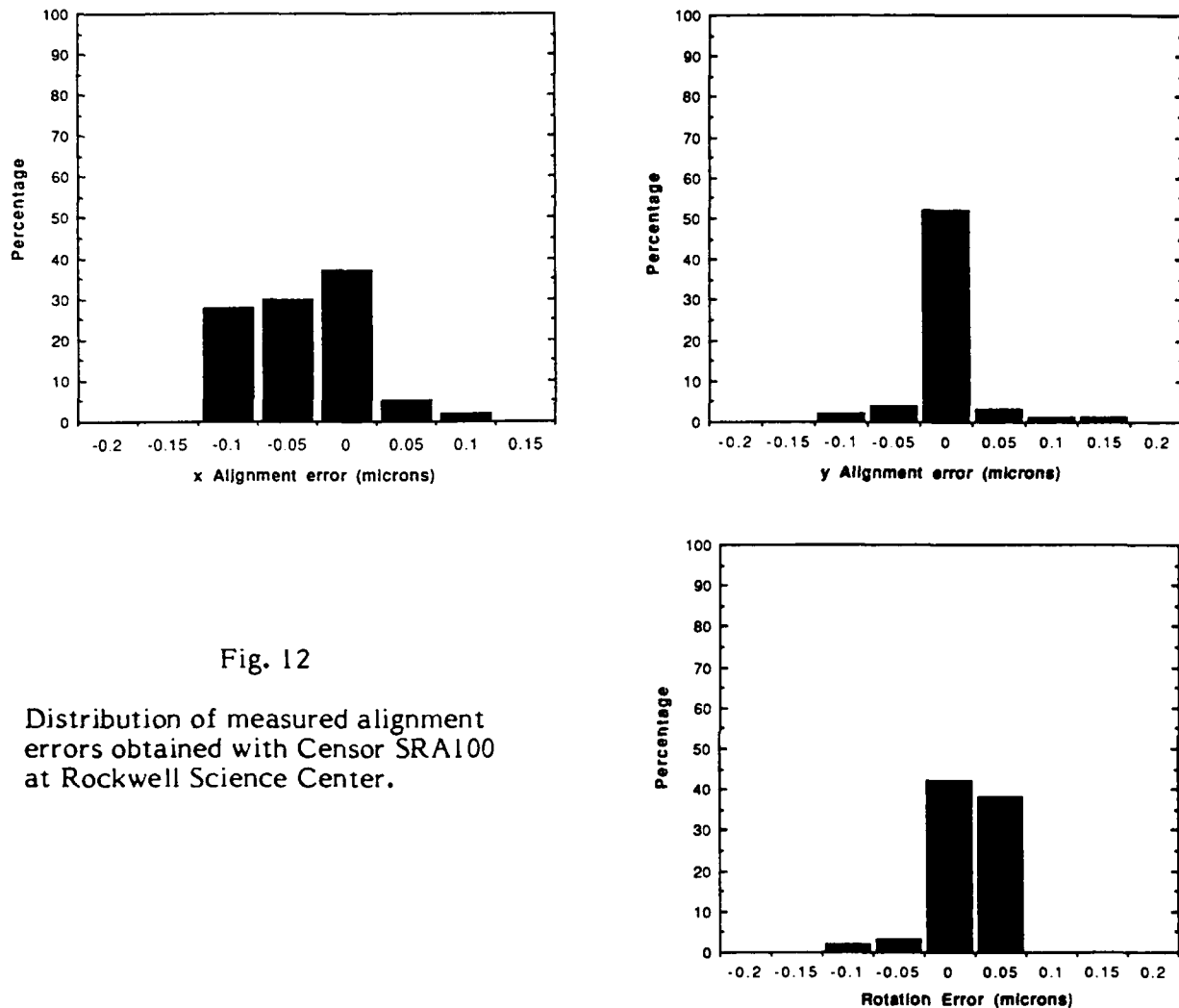
Fig. 12

Distribution of measured alignment
errors obtained with Censor SRA100
at Rockwell Science Center.

For a self-aligned base contact HBT process, we found Al is the best material
for alignment marks. Al has an excellent reflectivity and does not react with GaAs
during alloying (at 350°C, which is the highest processing temperature in the baseline
process for self-aligned base contact). Using Al marks, we have successfully processed
HBT MSI circuits on 3 in. wafers. The benefits of using Censor alignment have been
reflected not only in the alignment accuracy and the large wafer fabrication, but also in
the fast turnaround time. One example that indicates a six-week turnaround for baseline
processing is shown in Fig. 14.

HBT WAFER USED FOR PROJECTION LITHOGRAPHY (CENSOR SYSTEM)

(a)
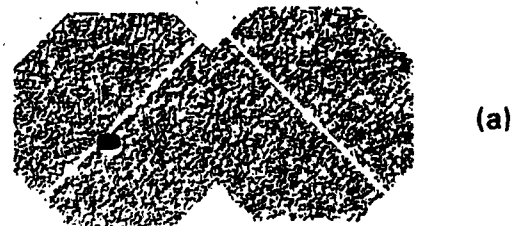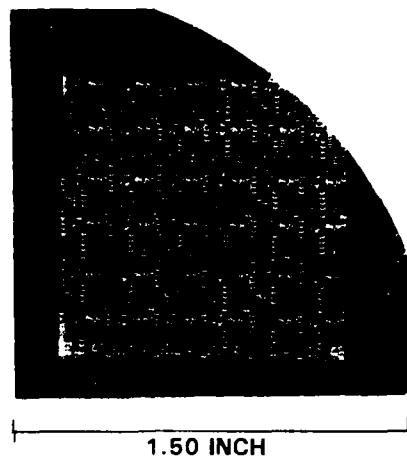
ALIGNMENT MARK DEGRADED DURING PROCESS

1.50 INCH

(b)

ALIGNMENT MARK PRESERVED THROUGH PROCESS

Fig. 13 Microphotographs of Censor alignment marks on HBT wafers after ion-implanted process with (a) inadequate and (b) adequate protection during anneal.

Wafer cleaning ⟶ IA alignment mark ⟶ Isolation mark ⟶ Isolation Implant ⟶
8/29/86　　　　　8/29/86　　　　　9/2/86　　　　　9/4/86

Cap layer etch back ⟶ Post annealing ⟶ Bext mask ⟶ Deep etching ⟶
9/12/86　　　　　9/15/86　　　　　9/18/86　　　　　9/19/86

Base metal depostion ⟶ E-con mask ⟶ Emitter metal ⟶ C-con mask ⟶
9/22/86　　　　　9/24/86　　　　　9/25/86　　　　　9/26/86

C-con etching and metallization ⟶ Transistor alloying & testing ⟶
9/26/86　　　　　　　　　　　　　9/29/86

NiCr resistor ⟶ 1st Metal ⟶ Via ⟶ 2nd Metal
10/6/86　　　　10/8/86　　　10/9/86　　10/10/86

Fig. 14 Process schedule and turn-around time demonstrated for a 3 in. HBT wafer lot.

4.3   Isolation

Semi-insulating GaAs substrates were used to allow full device isolation in the substrate region. Device isolation in epitaxial layers was obtained by B and He bombardment. After carefully adjusting the implanting energies, doses and dose rates, the isolation results were quite satisfactory. Using standard test patterns (70 μm wide and 10 μm spacing) and testing at 3 V, we found the averaged emitter-to-emitter resistance to be 3 MΩ, the base-to-base resistance 2.5 MΩ, and the collector-to-collector to be 6 MΩ. A 3 μm thick photoresist layer was used to protect active areas from implantation damage. To maintain the resolution and the sharpness of the photoresist, a recently developed contrast enhanced modulation (CEM) technique was successfully adapted for Censor lithography.

4.4   Contact Resistance

A major consideration for high-performance HBTs is the achievement of low contact resistances for the emitter, base and collector, as well as low extrinsic base resistance. These values were monitored in a series of transmission 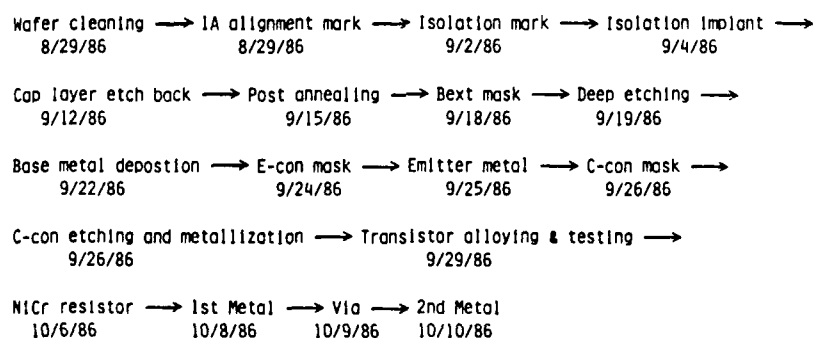line measurement patterns on each wafer. The emitter contacts were formed by using multiple metal layers of AuGe/Ni/Ti/Au (instead of AuGe/Ni/Au). Use of a Ti interlayer prevented the top Au layer from intermixing with the bottom AuGe/Ni layers during the alloying cycle, resulting in improved ohmic contact conductance. The values obtained for specific contact resistance of GaAs emitters were around 10×10^{-6} Ω-cm^2. Recently, we tried the same process on InAs emitters; the results are even more impressive. Without alloying, contact resistances as low as 2.9×10^{-7} Ω-cm^2 have been observed (Fig. 15). We believe that InAs cap material will be used extensively in future HBTs.

It is known that the base contact resistance strongly depends on the doping concentration in the p-layer. A summary of results for base contact resistance is shown in Fig. 16. We have recently achieved quite good results by using increased base layer doping. Using Au/Zn/Au as base contact metals, we have obtained 2×10^{-6} Ω-cm^2 at Pb = 2×10^{19}, 1.0×10^{-6} Ω-cm^2 at Pb = 5×10^{19}, and 5×10^{-7} Ω-cm^2 at Pb = 8×10^{19} cm^{-3}, respectively. In addition to Au/Zn/Au metals, we have also evaluated other metal systems to identify the best metallurgy/temperature combination. Results from this effort are summarized in Fig. 17.

Fig. 15

Measured resistances in an emitter
contact transmission line pattern
on an InGaAs contact wafer, showing
low resistance.

N_e = 3x10^{19} cm^{-3}
R_s = 40 $\Omega/\square$
R_c = 2.9x10^{-7} Ω-cm^2
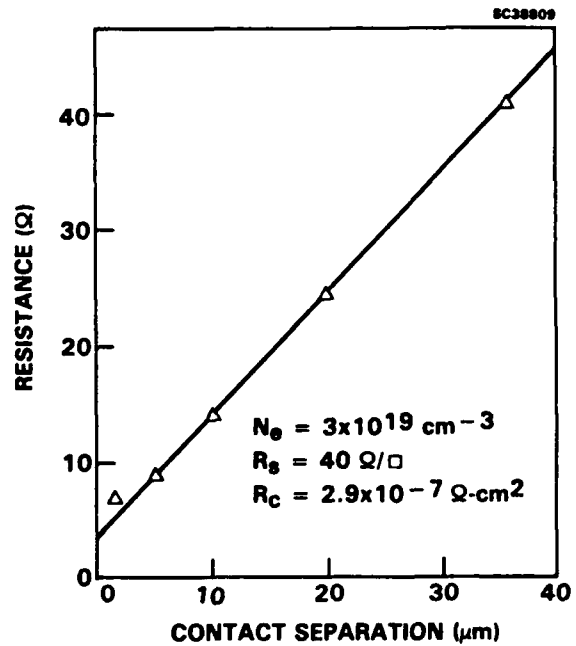
Fig. 16

Measured specific contact resistance
obtained with Au/Zn/Au contacts on
HBT base layers and p-type test
layers.

△ THIS WORK (TEST WAFERS)
□ THIS WORK (HBTs)
○ PUBLISHED WORK (TEST WAFERS)

THEORY
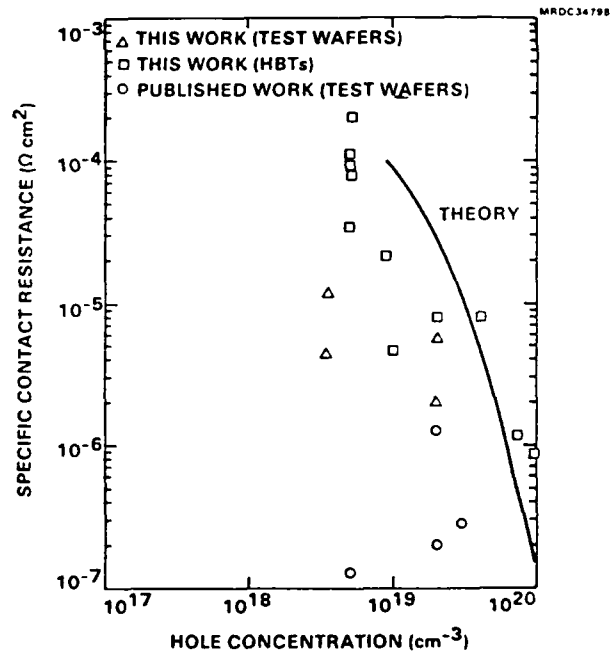
Contact to the collector is made by etching a via hole through the uppermost
epilayers down to the buried subcollector. By using orientation selective wet etching of
GaAs, via holes with properly sloped sidewalls are obtained, so that this process has

Fig. 17

Measured contact resistance for various candidate base contact metallization systems.

Legend:
- MnAu test wafer
- AuZnPdAu HBT
- AuZnAu HBT
- AuZnAu test wafer

Y-axis: Specific contact resistance (ohm cm2)
X-axis: Hole concentration (cm-3)

exhibited essentially 100% yield. AuGe/Ni was used as the ohmic contact metallization. The resulting collector contact resistance was usually measured to be in the 10^{-7} $\Omega\text{-cm}^2$ range as shown in Fig. 18. Representative sheet resistance of the n^+ subcollector layer is 12-15 Ω/sq.

4.5   Interconnects

To complete the ICs, resistors are formed by depositing NiCr layers on the semi-insulating GaAs surface and interconnecting the devices with two layers of metal separated by an interlayer dielectric. A schematic cross section of a completed IC is shown in Fig. 9 above. The NiCr used to data has had sheet resistances in the range 200-400 Ω/sq. Good control over the resistance has been obtained by in-situ monitoring of the resistance of a test sample during resistor deposition. The uniformity of the deposited NiCr film was confirmed by the sheet resistance measured from the resulting resistors. As shown in Fig. 19, a 2.1% standard deviation of NiCr resistance values has been demonstrated on one 3 in. wafer.

Transistors and NiCr resistors were connected by the sputtered first-level metal. A multilayer metal system of Ti/W/Au/Ti was chosen for good conductivity and good step coverage. A W layer was used to prevent the reaction of the Au layer with the underneath ohmic/resistor 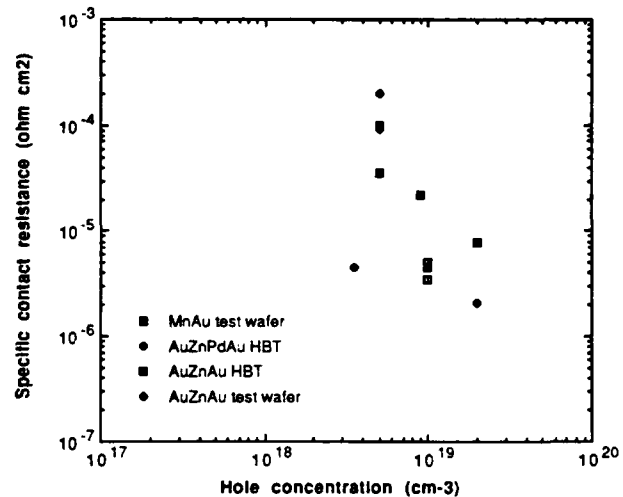films during the subsequent dielectric deposition cycles. Patterning of the first-level metal was achieved by photoresist liftoff. Since an extremely low-power sputtering was used, one can lift off metals by repeated acetone soaking and spraying. The typical sheet resistance of the first-level metal is 0.2 Ω/sq.

Fig. 18

Measured resistances in collector
contact transmission line pattern.

DB2.73   13-Oct-86   RS
OCR.01
OHMIC CONTACT RESISTOR 3 inch   Av=347.0 Ohms/sq
                                    2.5mm Sd=7.37(2.1%)
                                           N=44/44

    1   2   3   4   5   6   7   8   Av=344.6 Ohms/sq
                                             Sd=6.18(1.5%)
                                             N=32/32
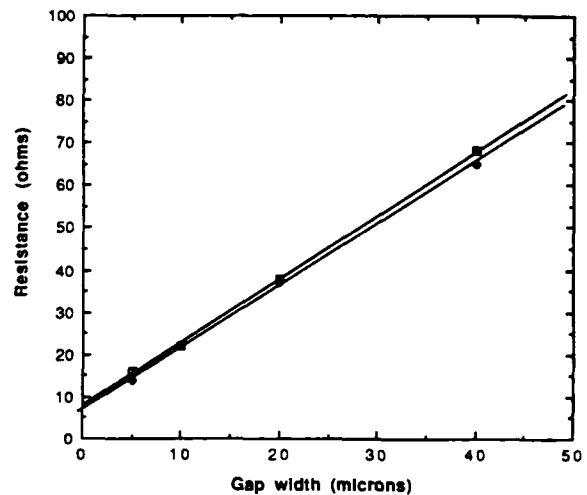
Fig. 19

Distribution of sheet
resistance of evapor-
ated NiCr film across
a 3 in. wafer.

<=-.50*Av   =-.10*Av   =.20*Av
=-.40*Av   =.00*Av   =.30*Av
=-.30*Av   =.10*Av   =.40*Av
=-.20*Av   >=.50*Av

*3.0Ohms/sq
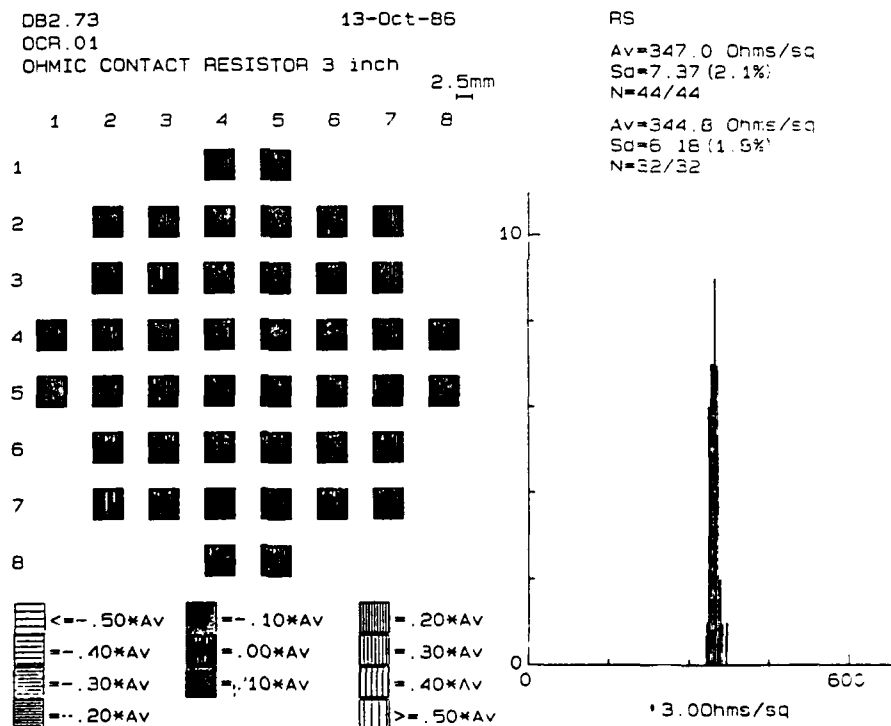
We have tried plasma-enhanced CVD Si_3N_4 and more recently polyimide as an
interlayer dielectric. The advantages of using polyimide include superior uniformity, side
coverage and low dielectric constant. The measured relative permittivity is around 4.0,
which is half of the value of the PECVD Si_3N_4. Once the vias were defined and etched
through, the polyimide (or Si_3N_4), a thick Ti/Au layer (8000Å) was sputtered as the
second-level metal and ion milling was used to pattern the metal. The typical sheet
resistance value of the second-level metal is 0.05 Ω/sq, which is one-quarter of the first-
level metal.

5.0 HBT CHARACTERIZATION

The principal figures-of-merit for HBT circuit performance are cutoff frequency, f_t; transconductance, g_m; current gain, β; and threshold voltage standard deviation, σ_v. Values attained during this program for the figures-of-merit are: $f_t = 40$ GHz; $g_m = 6000$ ms/mm; $\beta = 40$ in small devices (400 in larger HBTs); and $\sigma_v = 2.5$ mV across a wafer. Each parameter is highly favorable for a high-speed IC technology. Other subsidiary characteristics include parasitic resistances and capacitances, breakdown voltages, temperature dependences of I vs V, leakage and saturation characteristics. This section discusses the test methodology used to determine these transistor characteristics. The experimental values obtained and a brief analysis are then presented.

5.1   Test Patterns

A significant fraction of the mask sets HB2, DB1 and DB2 is devoted to parametric measurements. There are approximately ten patterns in each mask set devoted to measurements of transistors. Another ten patterns are used to determine process parameter values apart from the HBTs themselves.

The transistor test pattern distributed most widely across wafers is the QD1 pattern, shown in Fig. 20. It contains within it four transistors of different sizes and a resistor. The transistors include the minimum geometry transistor (known as Q1) with 3 μm × 4.5 μm emitters; this typifies the devices used in the ICs. Another transistor has even tighter dimensions (2 μm × 4.5 μm emitters) to explore the possibility of more aggressive designs; one more has much looser dimensions (8 μm × 20 μm emitters); and a final one has very large dimensions (72 μm × 72 μm emitters). This last device has such a large area-to-periphery ratio that, as will be shown below, its current gain is not limited by emitter edge recombination. It provides a measure of area-dependent recombination (principally determined by MBE growth characteristics). The probe-pad areas of QD1 are covered by contact metallization layers themselves. Thus, the measurements are possible as soon as all the transistor layers have been deposited - it is not necessary to finish the wafer processing (with resistors, vias and two levels of interconnect wiring) to determine transistor results.
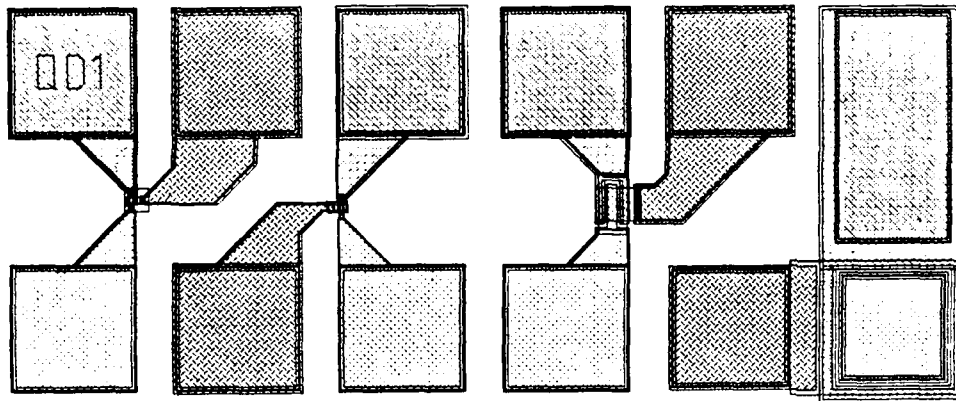
Fig. 20 QD1 test pattern for measurement of basic HBT characteristics.

The QD1 pattern is placed in a 3 × 3 array covering each lithographic field. Thus, in a representative Censor-processed wafer with nine fields exposed, there are 81 transistors of each of the above types forming a uniform array. These devices formed the basis of wafer mapping tests.

Many more test patterns examined the effect of transistor design rule changes. Most critical dimensions such as emitter width or length were varied in a systematic way. This permitted evaluation of, for example, the variation of current gain with emitter dimension, lithography limits, etc.

Finally, numerous transistor patterns were devoted to significant changes in transistor geometry, including comparisons of "island" vs "walled" emitter structures, devices with a single base contact, transistors with multiple fingers for use as output drivers, etc.

The test patterns for process monitoring included, among others, a variety of transmission line method (TLM) structures to evaluate layer resistivity and specific contact resistance for emitter, base and collector layers. Also present were isolation gaps, typically one of 5 μm width and one of 10 μm width, separating two active areas with only the emitter, base or collector layer contacted. Different gaps addressed each of the layer types, so that when leakage was detected, the faulty layer could be identified. Various patterns were present for capacitance measurements (large E-B or B-C junction diodes), metal line resistance (emitter metal, base metal, and first-and second-level interconnects), via chains, and line-to-line shorting at 2 μm and 3 μm design rules. Finally

a variety of patterns were implemented to examine metal coverage across regions of wafer nonplanarity. For example, in Fig. 21 is seen, among other patterns, a "collector contact chain" in which first-level metal is forced to go up and down the edges of holes etched to the collector n^+ layer (1 μm deep), 35 in all, to see if any breaks in the line occur. It is interesting to note that in testing on the order of 30 of these patterns distributed across many wafers, no open has yet been found, indicating the effectiveness of the orientationally sensitive etching procedure developed for the collector vias.
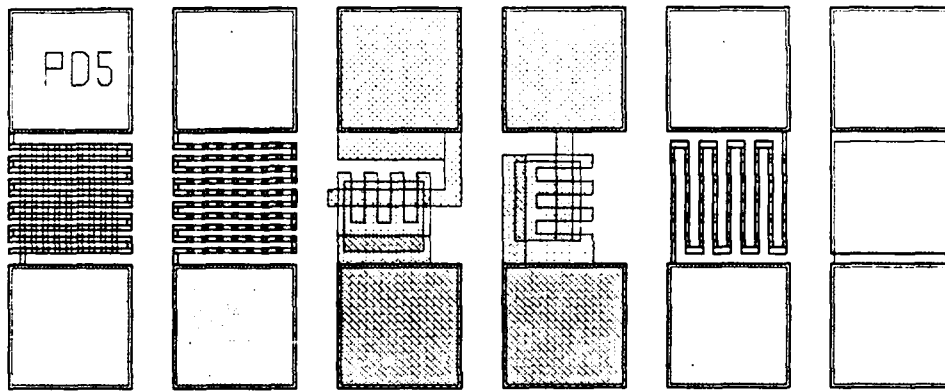
Fig. 21   Test pattern to determine connectivity of various metal lines (including first-level metal into collector vias) and other process characteristics.

To examine transistor f_t directly, S-parameter measurements were conducted using special test patterns. These patterns made use of larger area HBTs than the minimum geometry Q1, so that stray pad capacitance would incur proportionally less error. Connections were made to the device terminals in a way which minimized emitter lead inductance. Figure 22 shows the two types of microwave test patterns used.

5.2   Test System

For most purposes, manual probing of the test patterns was done using a Tektronix 576 curve tracer or HP 4145 semiconductor parametric analyzer to display the data. However, during the course of this program, an automated test capability was developed for HBT wafers. This capability is based on a previously developed system for testing GaAs MESFET wafers, to which software was added for the analysis of HBT data. The system makes use of an Electroglass prober, an HP semiconductor parameter

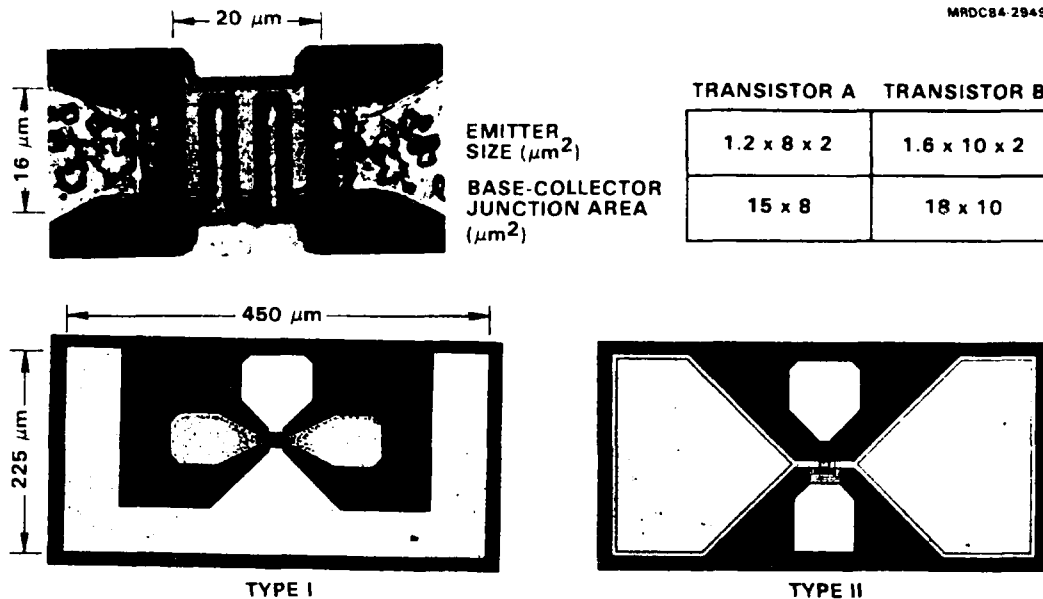|	TRANSISTOR A	TRANSISTOR B
EMITTER SIZE (μm^2)	1.2 x 8 x 2	1.6 x 10 x 2
BASE-COLLECTOR JUNCTION AREA (μm^2)	15 x 8	18 x 10

Fig. 22 Test patterns for microwave HBTs.

analyzer, a crosspoint switch matrix, a dedicated Micronova computer, and (on a time-shared basis) a Data General MV8000 computer. In a representative test, I_c and I_b are recorded vs V_{be} (at $V_{bc} = 0$) for a given transistor type all across the wafer. The 'raw' data can be examined for any given device, or the corresponding calculated values of current gain vs V_{be} or vs I_c can be plotted. For any chosen threshold current, a corresponding "threshold voltage" (i.e., the value of V_{be} that will produce a threshold output current) can be calculated. Finally, entire wafer statistics of any desired parameter (such as threshold voltage or current gain) can be computed and displayed as a table (mean and standard deviation), a histogram or a wafer map. Figures 23a and 23b illustrate some of the output types obtainable with this system.

5.3   Measured HBT Characteristics and Analysis

The basic I-V characteristics of minimum geometry transistors used in most of the ICs are shown in Fig. 24. The I_c-V_{be} and I_b-V_{be} characteristics for a related device are shown on a logarithmic scale (Gummel plot) in Fig. 25 for $V_{bc} = 0$. The forward current I_c varies exponentially with V_{be} with an ideality factor close to 1.0, up to a limit established by series resistance. The overall magnitude of the current is typically in

(a)

DB2.73ʊ

VBE.14

VBE SCAN H4 3 INCH

2.5mm

Av=7.24~2E-02 ⁿsM
Sd=7.9ᵐʊE-ʊ3 ⁿsM
N=8ʔ/8ʊ

Av=7.6ʊ.4E-02 ⁿsM
Sd=5.41̇7E-03 ⁿsM
N=64/64

⊟<=-2.50*Sd   ■=-.50*Sd   ▥=1.00*Sd
⊟=-2.00*Sd   ■=.00*Sd   ▯=1.50*Sd
⊟=-1.50*Sd   ■=.50*Sd   ▯=2.00*Sd
⊟=-1.00*Sd   ▯>=2.5.*Sd

4E-2   6E-2   8E-2   0.1

↦3.00E-03msM

(b)

DB2.73   13-Oct-85   RS

OC.01

OHMIC CONTACT BEXT 3 inch

2.5mm

Av=730.6 Ohms/sq
Sd=39.5 (5.4%)
N=44/44

Av=713.ʊ Ohms/sʊ
Sd=2ʊ.7 4.3%
N=32/3ʊ

▤<=-.50*Av   ■=-.10*Av   ▥=.20*Av
▤=-.40*Av   ■=.00*Av   ▥=.30*Av
▤=-.30*Av   ■=.10*Av   ▥=.40*Av
▤=-.20*Av   ▥>=.50*Av
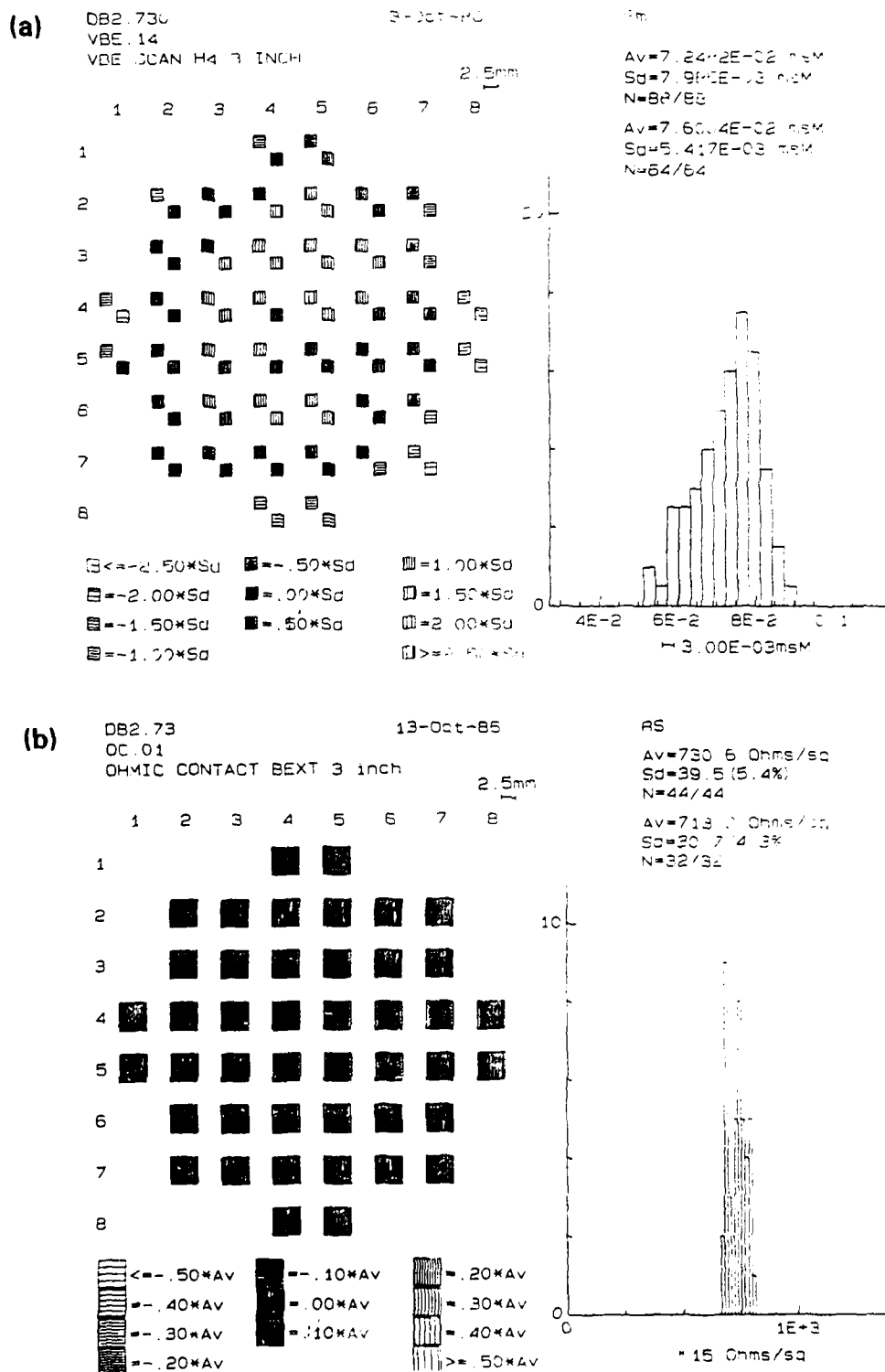
1E+3

↦15 Ohms/sq

Fig. 23   Representative output from automated test system; (a) map and histogram for transconductance g_m; (b) map and histogram of base sheet resistance.

close agreement with the predicted result for heterojunctions without potential barriers on the emitter-base junction region, as given by Kroemer:

$$I_c = \frac{qD_n n_{ib}^2}{P_b W_b} \exp \left(\frac{q\,V_{be}}{kT}\right) \quad .$$

(1)

Here, D_n, P_b, W_b and n_{ib} are the electron diffusion coefficient, hole concentration, thickness, and intrinsic carrier density in the base region of the device. A close comparison between experimental I-V curves and other parameters in Eq. (1) leads to an experimental determination of the quantity n_i appropriate to the heavily doped p-type base regions. The effective intrinsic carrier concentration is slightly higher than in undoped material as a result of band gap narrowing effects.

MRDC84-26200
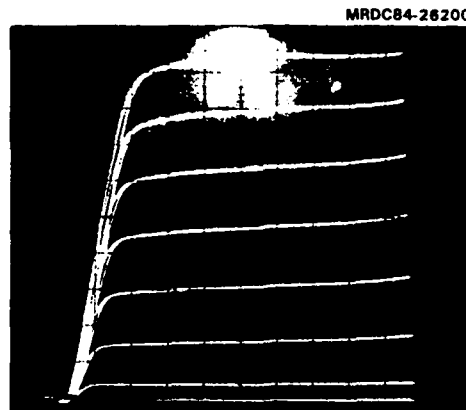
I_C : 1mA/div

V_{CE} : 0.5V/div

I_B : 50 μA/step

EMITTER DIMENSIONS : 1.6 μm x 5 μm

$$\frac{gm}{L} = 6000\ \frac{mS}{mm}$$

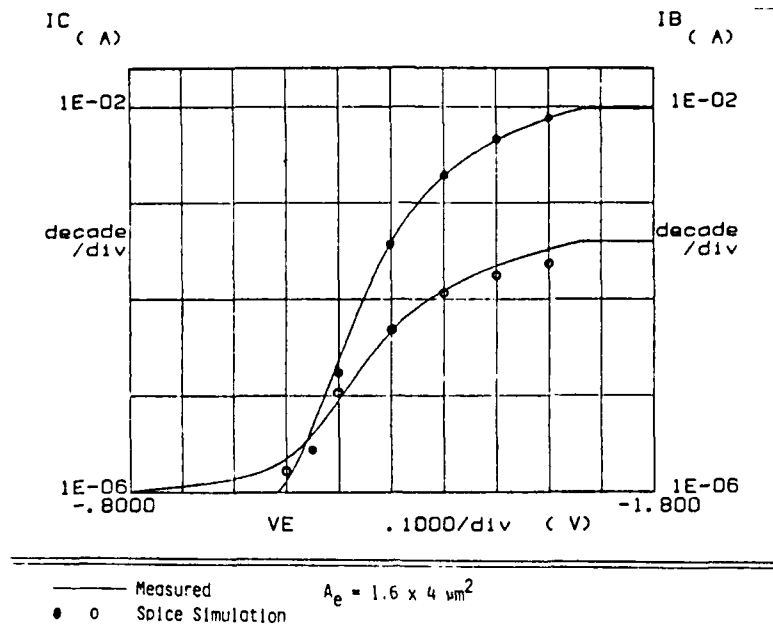Fig. 24 Common emitter I-V characteristics.

Fig. 25 I_C and I_B vs V_{BE} (Gummel plot) for a representative HBT.

In a significant fraction of the cases, however, the collector current is lower than that given by Eq. (1) by up to several orders of magnitude, and the ideality factor is somewhat larger than unity. This corresponds to the case where diffusion of acceptors from base to emitter has occurred. In this situation, with the p-n junction somewhat inside the higher band gap AlGaAs, a potential barrier is developed in the conduction band, and the junction turn-on voltage is increased accordingly. The retarding barrier for hole injection into the emitter is also decreased, so that the current gain drops significantly.

The two cases can be distinguished experimentally by comparing forward and reverse I-V characteristics, i.e., collector current vs V_{be} and emitter current vs V_{bc}, for a given device. As shown in Fig. 26a for a normal device, the two curves overlap up to the limit established by series resistance. This behavior is predicted by Eq. (1). For a diffused device, however, as depicted in Fig. 26b, the reverse current is actually greater (because the potential spike is diminished by the potential profile near the reverse-biased junction).
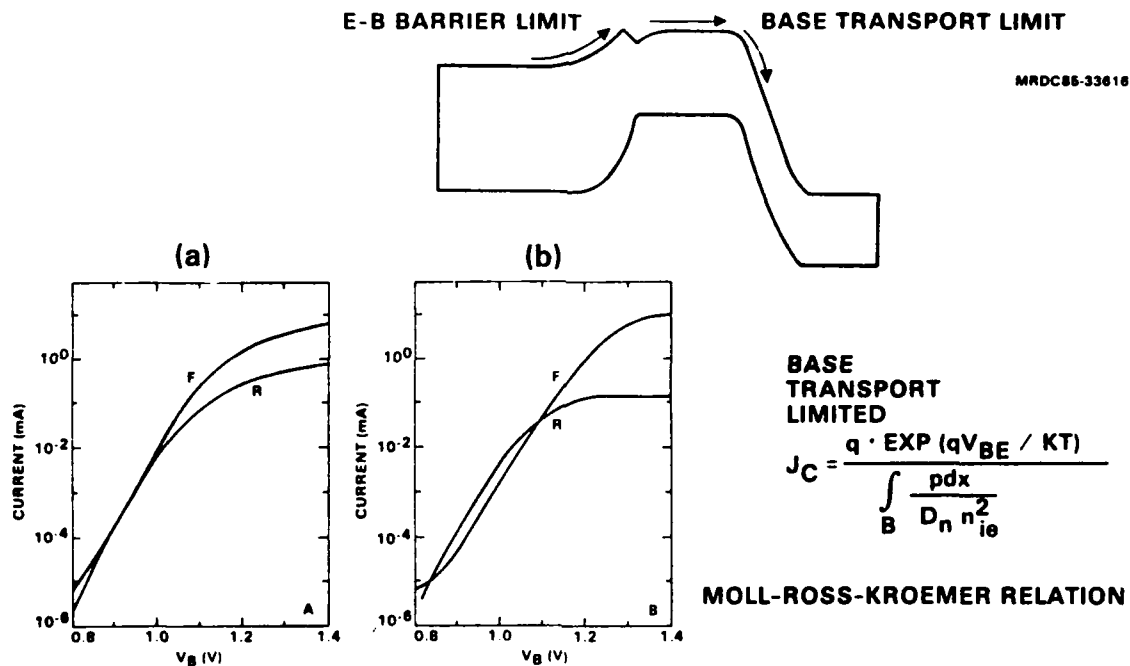
E-B BARRIER LIMIT ──────► BASE TRANSPORT LIMIT

MRDC85-33618

(a)   **(b)**

**BASE
TRANSPORT
LIMITED**

$$J_C = \frac{q \cdot EXP\,(qV_{BE} \,/\, KT)}{\int_B \frac{pdx}{D_n\, n_{ie}^2}}$$

MOLL-ROSS-KROEMER RELATION

Fig. 26   Plot of measured I_C vs V_{be} (forward characteristics) and I_e vs V_{bc} (reverse characteristics) for (a) normal device and (b) device with potential barrier at B-E junction.

It can be expected from Eq. (1) that V_{be} is highly uniform. In fact, the V_{be} value required to reach a current density J_m is given by

$$V_{be} = E_{gb}/q - (kT/q)\ell n \left(\frac{qD_n N_c N_v}{J_m P_b W_b}\right) \tag{2}$$

obtained from Eq. (1) by reexpressing n_i in terms of the base band gap E_{gb} and effective conduction and valence band densities of states, N_c and N_v. The practical value of the second term is 0.25 V; it changes by only 2.6 mV for a 10% change of any of the variables within.

If there is a conduction band potential spike present, the value of V_{be} at a given current is expected to be quite sensitive to the "details" of the spike, however, and the uniformity of the threshold voltage will be poorer.

Experimental results for a number of wafers are shown in Fig. 27. Blank boxes appearing in the wafer maps near the wafer edges are principally artifacts due to the
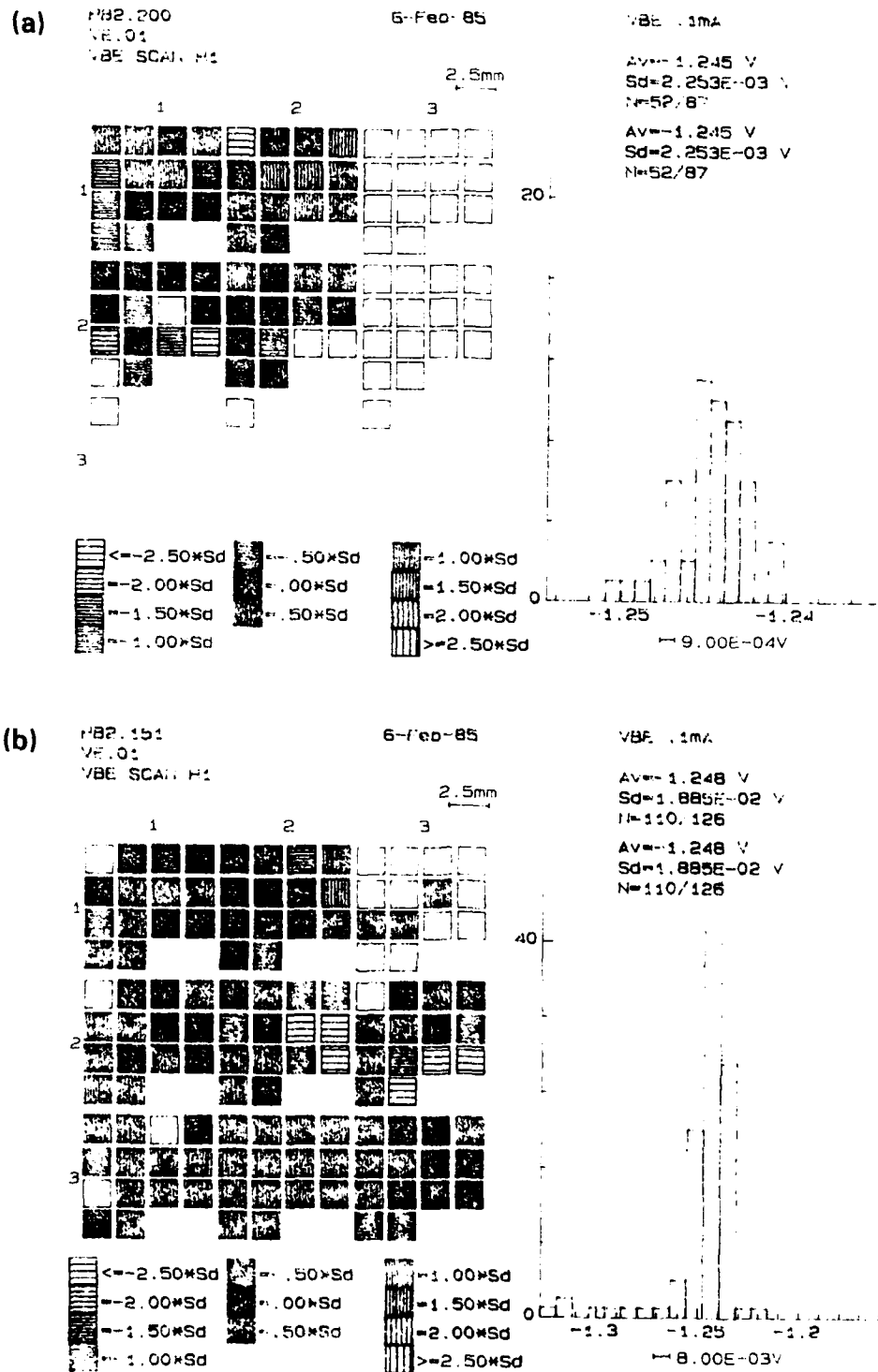
Fig. 27   Wafer maps of threshold V_{be} measured on (a) selectively etched HBT wafer, and (b) ion-implanted HBT wafer.

inability of the plotting routine to cope with wafers of variable sizes. The data correspond to measurements of the minimum geometry transistor (worst case). All the data show respectable uniformity, but the standard deviations obtained on the selectively etched wafers (2.3 and 4.1 mV) are lower than the corresponding result on the ion implanted and annealed structure (19 mV), probably due to a slight amount of dopant diffusion in the latter case.

The HBT transconductance g_m is given implicitly by the above behavior of I_c vs V_{be}. Thus, the intrinsic transconductance g_{mo} is given by

$$g_{mo} = \frac{qI_c}{kT} \tag{3}$$

as is well known for Si and Ge HBTs, while the extrinsic (terminal) transconductance g_m is further limited by emitter and base series resistances, R_e and R_b, as

$$1/g_m = 1/g_{mo} + R_e/\alpha + R_b/\beta \quad . \tag{4}$$

Here, β is the incremental current gain, and $\alpha = \beta/\beta+1$ is the current transport factor. Experimentally, g_m can rise to very high values (both absolutely and on a per-unit-area basis). In Fig. 28, $g_m = 70$ ms in devices with emitter dimensions 1.6 μm × 12.5 μm is seen. This corresponds to 3.5 ms/μm^2 of emitter area, or 5600 ms/mm of emitter length (to express it in the same units as used to characterize FETs). This value is approaching the practical limit of 13 ms/μm^2 set by the attainable current density (10^5 A/cm^2) and emitter-specific contact resistance (5×10^7 Ω-cm^2).

As can be seen in Fig. 24, the characteristic output conductance (i.e., the change in collection current at fixed I_b with varying V_{cb}) is remarkably low for HBTs. In other terms, the value of Early voltage, V_a, is remarkably high. This result also follows from Eq. (1); in low leakage HBTs, the principal way for V_{cb} to affect the output is to modulate the effective base width W_b in Eq. (1) due to the penetration of the base collector space-charge region into the base. For a given increment of voltage ΔV_{cb}, the charge depleted from the base is $\Delta Q = C_{bc}\Delta V_{cb} = (\epsilon/W_c)\Delta V_{cb}$, from which it may be found that

$$\frac{dI_c}{I_c} = -\frac{dW_b}{W_b} = -\frac{dQ_b}{qP_bW_b} = -\frac{C_{bc}dV_{cb}}{qP_bW_b} \quad . \tag{5}$$
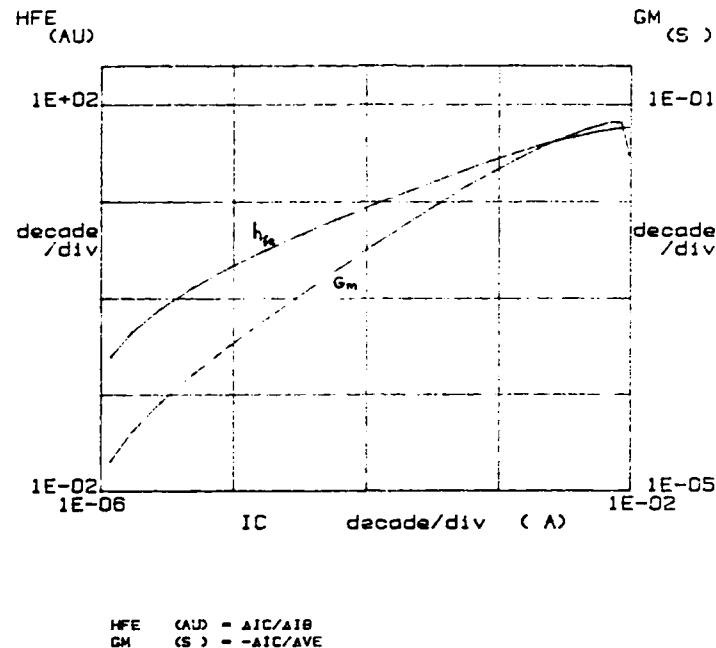
HFE   (AU) = ΔIC/ΔIB
GM   (S) = -ΔIC/ΔVE

Fig. 28 Measured transconductance vs I_c for a representative HBT.

From this, $V_a \approx I_c/(dI_c/dV_{cb}) = qP_bW_b/C_{bc}$. The total base sheet doping concentration (or Gummel number P_bW_b) is much higher in HBTs than in homojunction devices (on the order of 10^{14} cm^{-2}), while the collector doping is on the same order for two, leading to similar values of base-collector capacitance (near 0.4 fF/μm^2). The Early voltage of HBTs is thus expected to be much higher than in homojunction transistors, on the order of 200-400 V. Efforts to directly measure V_a from the HBT I-V characteristics have not been successful, however, since the effect is masked by the changes in junction temperature induced by changing V_{bs} coupled with the effects of heating. As described below, this frequently gives the net effect of negative output and conductance.

Another feature of the I_c curves evident in Fig. 24 is the fact that I_c attains positive values only after a finite value of V_{ce} is applied (0.25 V in this example). This voltage, commonly termed "offset" or "turn-on" voltage, corresponds in conventional bipolar nomenclature with V_{cesat}, inasmuch as this is the value of V_{ce} established under open-circuited collector (full saturation) conditions. A variety of physical mechanisms may affect V_{cesat}. The simplest physical picture, however, is the following: To maintain $I_c = 0$ with a forward-biased emitter-base junction, the forward current I_c predicted by

Eq. (1) is exactly cancelled by a current flowing out of the collector due to the forward-biased base-collector junction. V_{cesat} may then be identified as the difference between V_{be} and V_{bc} needed to establish I_c. It was noted that, for graded heterojunction devices in the absence of base dopant diffusion, the electron current flows are symmetric. This implies that V_{bc} is at most equal to, never greater than, the corresponding voltage V_{be} required to establish I_c. The base-collector junction current flow has a number of other important components, however. unlike forward operation, in reverse operation the current gain is much less than unity due to the large inverse doping ratio between the base and collector layers. The hole diffusion current into the quasi-neutral collector is larger than the electron flow in a ratio on the order of

$$I_n/I_e = D_p/D_n \times W_b/L_h \times P_b/n_c \times A_{bc}/A_e \quad , \tag{6}$$

where L_h is the hole diffusion length, n_c the collector doping, and A_{bc}, A_e are the respective areas of the base-collector junction and the emitter. For a representative case, this ratio is 250, and the hole diffusion current-limited V_{offset} is $kT/q \ln 250 = 145$ mV. In addition, there is an even larger hole current contribution from recombination in the base-collector space-charge region. This leads to an ideality factor $n = 2$ as observed in most experimental results. The resultant offset voltage is of the right magnitude, and it varies with current level, as observed experimentally.

To understand the magnitude of the HBT current gain, it is necessary to consider in detail the base current flow in normal operation. As depicted in Fig. 29, there are a number of contributions to the base current, corresponding to electron-hole recombination in the various device regions. The contribution I_{b1} from holes injected into quasi-neutral regions of the emitter is expected to be small, in light of the large band gap difference between emitter and base. In fact, $I_{b1}/I_c \approx \exp(-\Delta E_g/kt) \approx 10^{-6}$. Similarly, the effect of recombination within the base itself is not expected to be large because of the very short residence time of the electrons within the base. Here, $I_{b3}/I_c \approx \tau_b/\tau_{rec}$, where τ_b is the base transit time (on the order of 1 ps) and τ_{rec} is the minority carrier recombination lifetime within the base. For radiative recombination, τ_{rec} is approximately $1/Bp_b$, with $B = 10^{-10}$ cm^3 s^{-1}, leading to $\tau_{rec} \approx 500$ ps. Nonradiative recombination will further decrease the lifetime, but the overall magnitudes of the recombination is still not typically an important limitation of current gain. Accordingly,
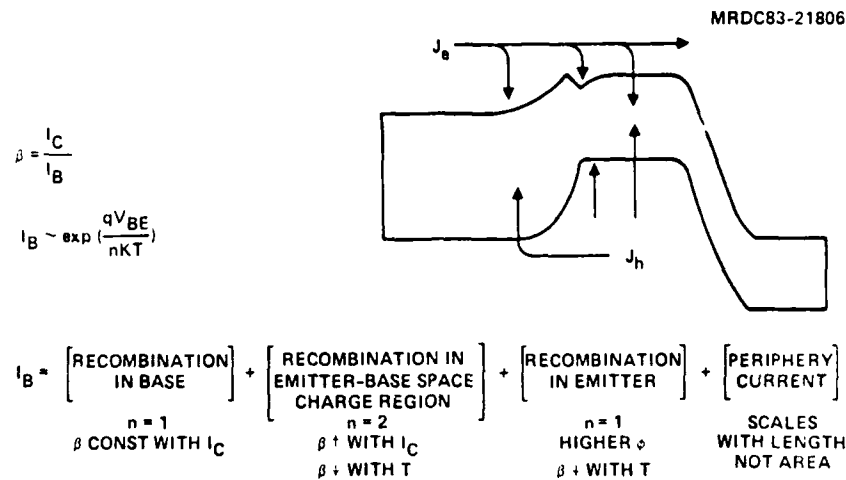
MRDC83-21806

$\beta = \dfrac{I_C}{I_B}$

$I_B \sim exp\left(\dfrac{qV_{BE}}{nKT}\right)$

$I_B = \begin{bmatrix} \text{RECOMBINATION} \\ \text{IN BASE} \end{bmatrix} + \begin{bmatrix} \text{RECOMBINATION IN} \\ \text{EMITTER-BASE SPACE} \\ \text{CHARGE REGION} \end{bmatrix} + \begin{bmatrix} \text{RECOMBINATION} \\ \text{IN EMITTER} \end{bmatrix} + \begin{bmatrix} \text{PERIPHERY} \\ \text{CURRENT} \end{bmatrix}$

n = 1	n = 2	n = 1	SCALES
β CONST WITH I_C	$\beta \uparrow$ WITH I_C	HIGHER ϕ	WITH LENGTH
	$\beta \downarrow$ WITH T	$\beta \downarrow$ WITH T	NOT AREA

Fig. 29 HBT band diagram indicating various sources of base current.

the n = 1 behavior of I_b vs V_{be} expected from contributions I_{b1} and I_{b3} is seldom seen experimentally.

The current I_{b2} corresponds to recombination in the emitter-base space-charge region, frequently a dominant source of base current. The net recombination rate U for the case of strong forward bias is easily found to be

$$U = N\sigma<v> \frac{pn}{p + n} \quad , \tag{7}$$

where N is the density of recombination centers, σ the carrier capture cross section (taken to be equal for electrons and holes) and $<v>$ an average carrier thermal velocity. For the homojunction case, as is well known, $pn = n_i^2 \exp(qV_{be}/kT)$ is constant across the p-n junction, and as a result U has a strong maximum at the plane where $p = n = n_i \exp(qV_{be}/2kT)$. The net recombination current density is

$$J_{b2} = qU = qN\sigma<v>W_r n_i \exp(qV_{be}/2kT) \quad , \tag{8}$$

where W_r is an effective width on the order of $kT/q\epsilon_m$, with ϵ_m the junction electric field. In the case of graded HBTs, n_i is a function of position, so that pn is not constant throughout the space-charge layer. U again reaches a sharp maximum, not where p = n, but rather where $n/p = |\epsilon_n/\epsilon_p|$.

ϵ_n and ϵ_p are the effective electric fields for electrons and holes, respectively, taking into account both the electrostatic potential and the gradients of the conduction and valence band energies. An expression approximately equivalent to Eq. (8) is typically expected, with ideality factor only approximately equal to 2, and with an intrinsic carrier concentration n_{ieff} that corresponds to a band gap greater than that of the emitter. An ideality factor n very close to 2.0 is observed experimentally over many orders of magnitude of current for most large area (72 μm × 72 μm) HBTs. As shown in Fig. 30, the current gain at a fixed collector current density tends to decrease with increasing base doping, approximately as $P_b^{-1/2}$. This roughly corresponds with the fact that I_c varies as P_b^{1}, so that higher V_{be} is required to attain a fixed current density with high doping. Through Eq. (8), the base current is then also increased, but by the square root of the base doping increase to correspond with the $V_{be}/2$ dependence.

MRDC34900

$P_b = 5 \times 10^{18}$ cm^{-3}	$P_b = 2 \times 10^{19}$ cm^{-3}	$P_b = 4 \times 10^{19}$ cm^{-3}
$h_{fe} = 55$	$h_{fe} = 30$	$h_{fe} = 20$
$\Delta I_B = 50$ μA/STEP	$\Delta I_B = 50$ μA/STEP	$\Delta I_B = 100$ μA/STEP

EMITTER SIZE: 2.5 μm × 12 μm

VERTICAL: I_C (1 mA/DIV)

HORIZONTAL: V_{CE} (0.2v/DIV)
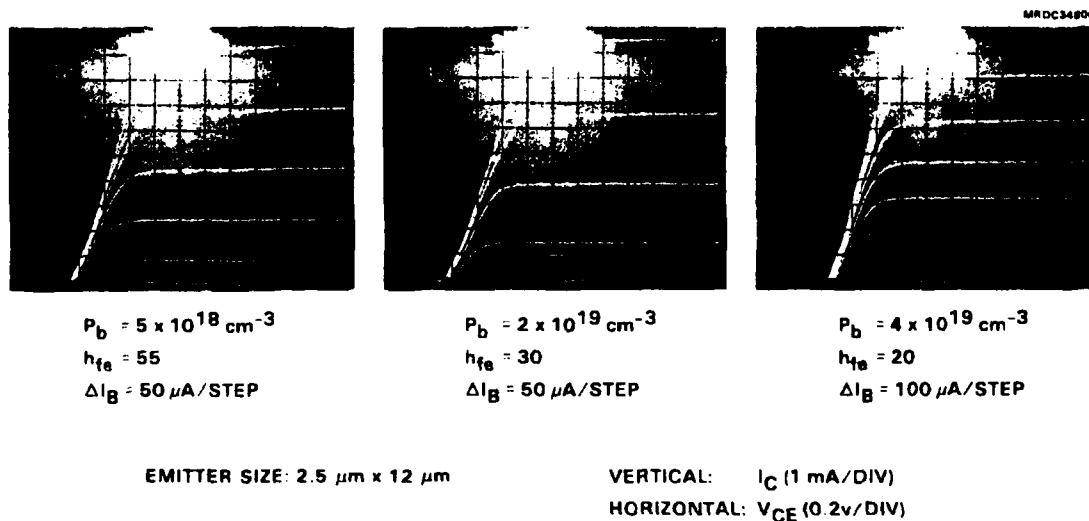
Fig. 30 I-V characteristics of a series of HBTs with varying base doping.

A final contribution to the base current, I_{b4}, is given by recombination at the edges of the emitter. In this work, two types of emitter edges were present: one edge where the emitter is limited by lattice-damaged isolation regions, as shown in Fig. 31 in line AA'; and another edge where the emitter is limited by extrinsic base regions (line BB' in Fig. 31). Both edges are important sources of recombination. To distinguish these

Base

A | A'

B

B'

Collector

Emitter

Fig. 31

Schematic HBT layout showing sources
of emitter periphery recombination,
along AA' for isolation edges and
along BB' for base contact edges.
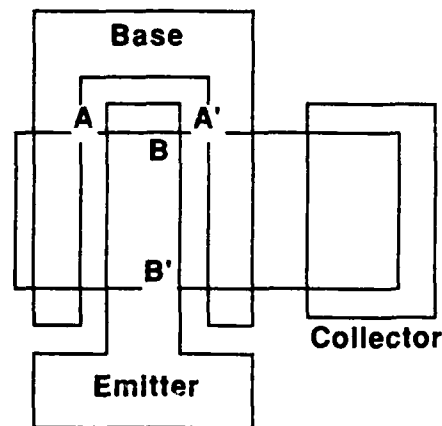
from area-dependent recombination, the most direct procedure is to compare I-V charac-teristics of devices with varying dimensions. For example, Fig. 32 plots I_c and I_b at a fixed V_{be} value for a number of devices differing only in emitter width, W_e. The results for I_c form a straight line passing through the origin. The corresponding I_b values also fit a straight line, but the data extrapolate to a nonzero intercept at $W_e = 0$. This intercept provides a measure of the periphery base current associated with the two emitter edges bordering the extrinsic base of length L_e. The periphery current is a sizable fraction of the total current for devices of less than 2 μm dimension. The severity of the periphery effect corresponds roughly with the very large value of surface recombination velocity in GaAs. By examining the I-V characteristics of the smallest periphery-dominated devices, it may be inferred that the edge recombination current has an ideality factor n near 2.0. This is in accord with the predictions of C. Henry[R] for the exposed edges of double heterostructure diodes.

The temperature dependences of the transistor characteristics are implicit in the expressions already discussed for I_c and I_b. From Eq. (1), for example, it is readily observed that I_c increases rapidly with temperature at a fixed V_{be}, or conversely, for a fixed I_c, V_{be} decreases by approximately 1 to 1.5 mV/°C. Similarly, I_b increases with temperature at a fixed V_{be}. If one examines the current gain at a fixed I_c, one finds the gain decreases with increasing temperature. This occurs because the rate of increase of I_b is proportionally greater than that of I_c, due to the fact that I_b depends on n_i at some point within the graded emitter-base junction, while I_c depends on n_i in the base region. Due to the higher band gap of the alGaAs, n_i in the junction region increases more rapidly with temperature. Experimental data for variations with temperature of V_{be} and β are shown in Figs. 33 and 34.

Fig. 32

Measured I_C and I_B at a fixed V_{BE} for a series of HBTs with varying emitter width, illustrating periphery recombination.
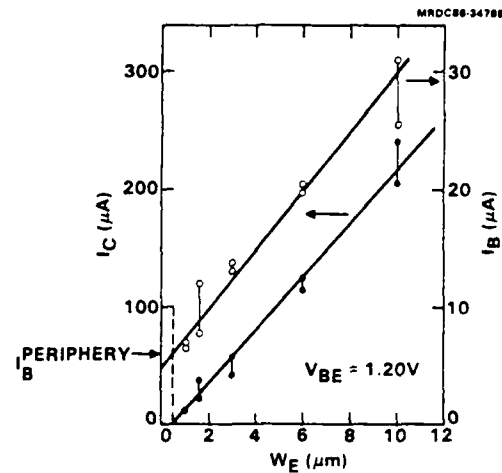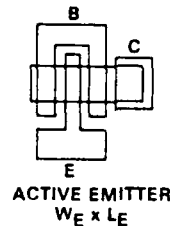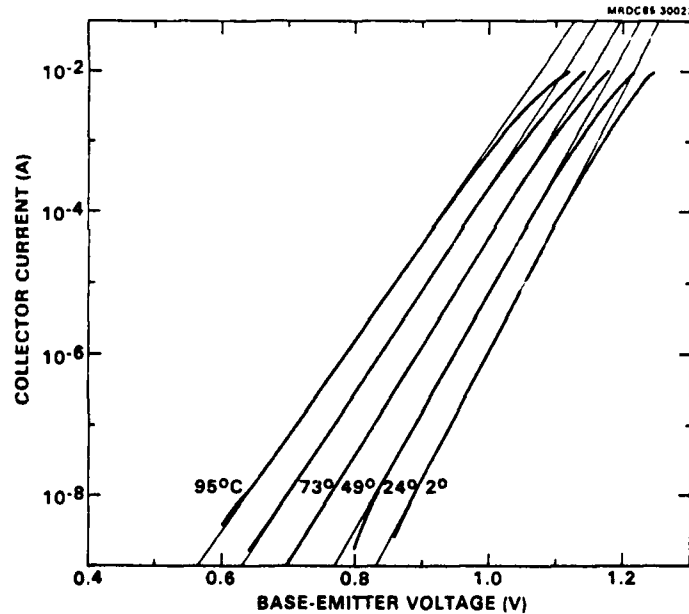

Fig. 33

Measured temperature variation of I_C vs V_{be} for representative HBT.

Microwave measurements were used to study the dynamic characteristics of the HBTs. The devices were probed with a Cascade Microtech probe system; S-parameters were measured with an HP8510 network analyzer. From the S-parameters, values of current gain h_{21}, maximum available gain MAG, and unilateral gain U were computed. Results are shown in Fig. 35 for a HBT wafer fabricated with ion implantation and in Fig. 36 for one processed with selective etching. f_t values for each are above 35 GHz; f_{max} values are of the same order.

Fig. 34

Measured current gain vs temperature
for representative HBTs.
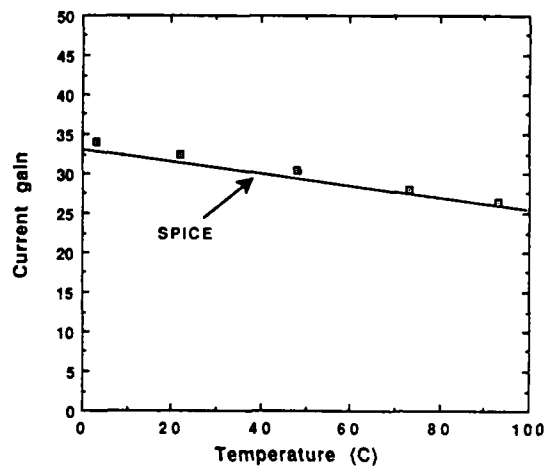
Fig. 35

Measured gain vs frequency inferred
from S parameter measurements of ion-
implanted HBT.
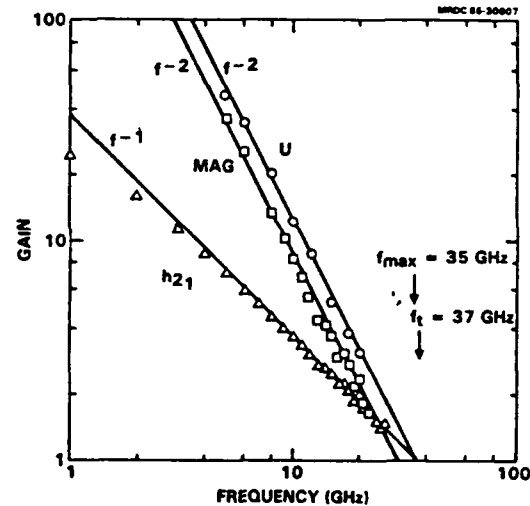
The cutoff frequency f_t is inversely related to τ_{ec}, the total transit time of electrons from emitter to collector. From $f_t = 35$ GHz, a transit time τ_{ec} of 4.5 ps is inferred. This value is in good accord with what is expected from consideration of the different components of τ_{ec}: the emitter capacitance charging time, the base transit time, and the contribution from the base-collector depletion region transit time (one-half of the total transit time) are each on the order of 1 ps. The remaining collector capacitance charging time, given by the product of base-collector capacitance (mostly extrinsic) with the sum of emitter and collector parasitic resistances, is on the order of 1.5 ps. This last contribution could be reduced significantly by superior fabrication. The "intrinsic f_t", which ignores the parasitic contributions, is on the order of 50 GHz.

Fig. 36

Microwave gain vs frequency for a
selectively etched HBT.
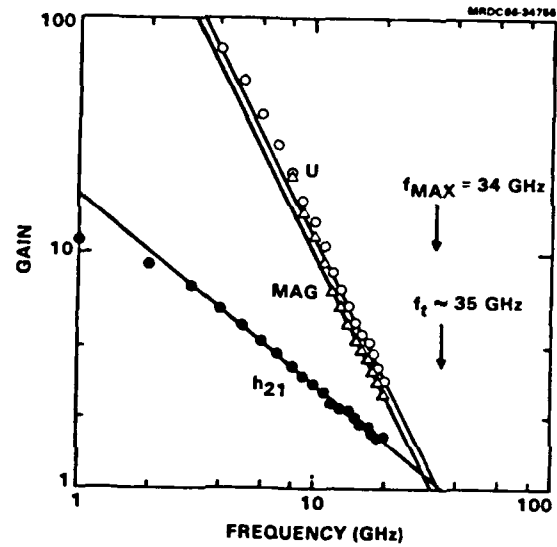
6.0 DEVICE MODELING

Accurate models are essential to guide device and circuit development efforts, particularly those involving new technologies without extensive data bases. At Rockwell, HBT modeling has been carried out at several levels. SPICE is a circuit simulation program for nonlinear circuit analysis. NODAL is a Rockwell-written program for linear circuit analysis. SEDAN is an one-dimensional modeling program, which predicts the device performance from the epitaxial layer structure. PARAM is also a Rockwell-written program that calculates the input parameters for SPICE and NODAL from the layer structure, transistor geometry, and measured I-V characteristics of HBTs. In addition, analytical approaches were developed to supplement the numerical calculations of SEDAN. These programs are described in the following.

SPICE

The SPICE program has been used extensively at Rockwell for the simulation of HBT digital and analog circuits. SPICE uses the modified Gummel-Poon model which represents well the HBT terminal characteristics. In particular, there are sufficient adjustable parameters in the SPICE representation that no changes in the SPICE code have been necessary, with the exception of a change in the implicit sign of the temperature dependence of the current gain. A set of input parameters describing a given transistor is required. For example, in Fig. 25 above, the Gummel plot for fabricated HBTs is compared to the result obtained by an appropriately fitted SPICE model. To adequately fit the temperature dependence of current gain, it is necessary to change the SPICE source code, allowing beta to decrease with temperature. Good fits with experiment may then be obtained, as illustrated in Figs. 33 and 34 above. For a given circuit, the program outputs the simulated circuit performance which have matched experimental results closely (typically within 20%). The plotting capability was enhanced with a Versatec plotter.

NODAL

NODAL is a program for linear circuit analysis. It calculates S-parameters, noise figure, input/output impedance, etc, for lumped element circuit models. For a given transistor model, the estimated values of the lumped elements are required as

inputs for the calculation. This analysis program forms the core of the high frequency, small signal transistor modeling. For example, the maximum frequency of oscillation, f_{max}, of a HBT can be estimated with NODAL.

SEDAN

The original one-dimensional SEDAN program for Si bipolar devices from Stanford University has been adapted for HBTs. For a given layer structure, doping and physical constants such as mobility, lifetime, etc., the program solves simultaneously Poisson's Equation, transport equations (drift and diffusion), and continuity equations. The band gap variation with composition is included properly. The solution that satisfies the boundary conditions imposed by the bias voltages V_{be} and V_{bc}, gives the electrostatic potential and the electron and hole concentrations as functions of depth. From these quantities, one can calculate the band diagram, current densities, current gain, junction capacitances, transit times and cutoff frequency f_t.

Since an HBT is a vertical device, this program is quite useful in predicting the above HBT characteristics. Predictions of the dependence of f_t on current density and emitter doping have been shown earlier in Fig. 2. Questions arising in the design of a MBE layer structure may be readily answered. For example, Fig. 37 shows the calculated band diagram for a MBE wafer actually grown at high forward bias operation. Figure 38 shows the associated hole concentration vs depth for the device. These calculations have been used for a variety of purposes, such as to estimate the amount of Al grading needed at the cap-emitter junction to avoid series resistance problems; to verify that the emitter AlGaAs layer is sufficiently thick to suppress recombination in the emitter; and to verify that the collector doping is enough to suppress base push out.

SEDAN is limited, since it is based on the conventional drift and diffusion expressions for electron current and it is only one-dimensional. Velocity overshoot effects were included in an ad hoc manner. It cannot model the effects of lateral device structure, such as contact resistance, extrinsic base collector capacitance, and emitter current crowding.

Fig. 37

Calculated band diagrams and carrier quasi-Fermi levels for Rockwell HBT structure under high forward bias ($J_c = 5 \times 10^4$ A/cm^2).
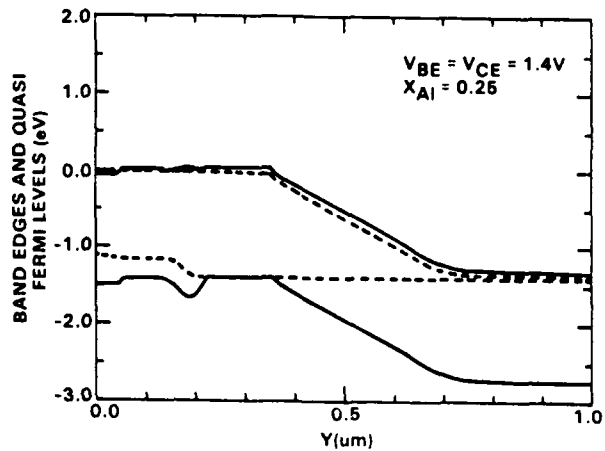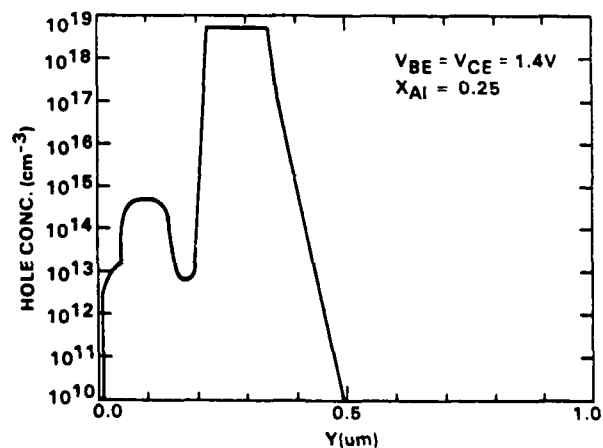

Fig. 38

Distribution of hole density in the device.

PARAM

To incorporate effects of lateral device structure on its terminal characteristics, a two or three-dimensional numerical model would be desirable. Currently, such programs for HBTs are not available at Rockwell. Instead, a program PARAM was developed to carry out limited calculations by evaluating analytic expressions, identical to those applicable to Si bipolar transistors. Inputs to the program are the three-dimensional structure of the transistor, its measured I-V characteristics, measured contact resistances, etc. PARAM then provides accurate estimate of terminal resistances and capacitances for SPICE and NODAL. It also estimate the cutoff frequency f_t and maximum oscillation frequency f_{max} from analytic expressions.

7.0 CIRCUIT DESIGN AND PERFORMANCE

Two mask sets, DB1 and DB2, were designed and laid out in this program. In each set, there were numerous test patterns, some small-scale ICs and MSI circuits specifically designed for this project. These test patterns were designed for studying discrete HBTs of different geometries, monitoring the processing techniques and experimenting with new ideas. The SSI circuits included nonthreshold logic (NTL) ring oscillators, CML ring oscillators and frequency dividers. These SSI circuits were used to test mainly the speed performance associated with each processing improvement. Several record-high speed performances were achieved with these circuits.

In DB1, we have implemented MSI circuits and protocol test chips. The MSI circuits included 8-bit universal shift registers and 8:1 MUXs. Three-bit registers and gated full adders were designed with different output protocols for comparison of speed-power performances. Each of these circuits were implemented with HBTs of different geometries.

In addition to these circuits included in DB1, we have added in DB2 1:8 DEMUXs, 2:1 MUXs and 1:2 DEMUXs. These DEMUXs were implemented with a new design as described below. The 2:1 MUXs and 1:2 DEMUXs have appropriate timing and control signals brought out to the pads, which allows cascading of each kind of circuits into higher numbers of bits in a tree-type architecture. In the following, the details of the design and performance are described.

7.1 Design Considerations

Circuit design closely resembles that of high-speed Si bipolar circuits. The circuits were based on CML in which current is steered between alternate load resistors depending on the inputs. The gate automatically produces complementary outputs. In most cases, both of these outputs were used to transmit signals differentiallly to succeeding gates, making the circuits insensitive to power supply and temperature variations. Series-gated CML gates were used, enabling two levels of logic to be accomplished with the same current source, as shown in Fig. 39. Typically, V_{cc} was held at 0 V and V_{ee} was -4.5 V. The source current, I_{ee}, controlled by V_s, was generally 1 mA. The on-chip logic swing was 0.4 V. A compound gate thus has a power dissipation of 4.5 mW,

and a logic capability of up to three equivalent NOR gates. V_{s2}, V_{s2} and reference voltages are generated on-chip, generally with provisions for off-chip voltage trimming. So far, no temperature compensation on the outputs has been used.

7.2   Input/Output Subcircuits and Protocols

The CML gate was also used as the input buffer, as shown in Fig. 40a. It accepts either differential inputs or a single input with a dc reference voltage V_{ref}. When the single input was used, V_{ref} was held at the mid-point of the input logic at -1.3 V. Due to to the current-steering nature of the CML circuits and the high transconductance of HBTs, input signals of very low voltage swing are acceptable.

• CURRENT-MODE LOGIC
  — SERIES-GATING
    (BILEVEL LOGIC)

• COMPLEMENTARY OUTPUTS
  — DIFFERENTIAL SIGNAL
    ROUTING

• LOW POWER
  — LOGIC SWING 0.4V
  — I_s = 1 mA
  — V_{ee} = -4.5V
    (4.5 mW FOR ABOUT 3
    EQUIVALENT NOR GATES)

• IDENTICAL "MINIMUM GEOMETRY" HBTs USED THROUGHOUT

• COMPATIBLE IN/OUT PROTOCOLS WITH Si DEVICES
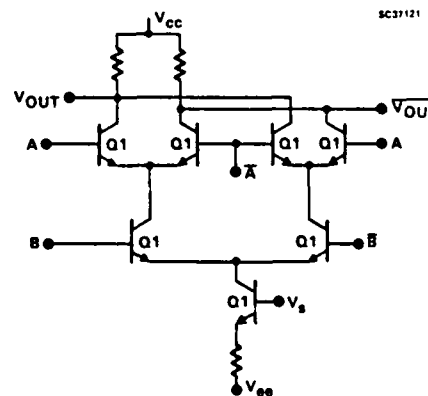
Fig. 39   Circuit diagram of a representative series-gated CML logic gate, as used for the HBT circuits.

One of the major concerns of circuit design is the design of output buffers, which bring the signals on-chip to the outside world. A proper output driver is necessary for a useful devices, especially for high-speed signals. Design considerations of such drivers include the impedance match, power consumption, speed (rise and fall time, propagation delay) and output voltage levels.

We have studied, with SPICE simulation, three kinds of output drivers for circuits implemented with HBTs. These are buffers of emitter-coupled logic (ECL), HBT

INPUT

Fig. 40

Circuit diagram for HBT input buffer.
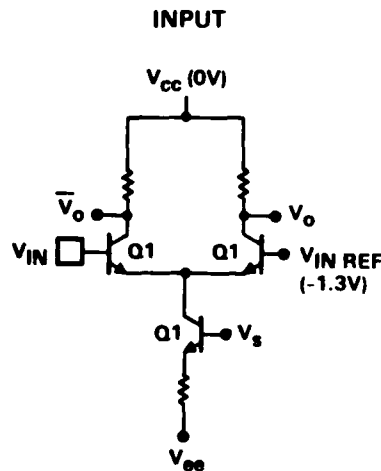
emitter-coupled logic (HECL) and CML. Figure 40b shows the representative circuit diagram for ECL/HECL and CML output drivers. The difference between ECL and HECL is the supply voltage V_{cc1}; 0 V for HECL and 1 V for ECL. The voltage levels of each protocol are listed in Table 3. The ECL driver is designed to be compatible with the Si world. HECL drivers are intended for signal transfer among HBT devices. CML outputs are terminated to ground via 50 Ω resistors. Thus, it does not require a pulldown circuit and is convenient to use. Output transistors (Q2) capable of carrying high current (up to 20 mA) were used. The output logic swing is adjustable via the voltage V_{s2} that controls the current through the gate. For ECL/HECL, the absolute output voltages can be determined via V_{cc1}. Using 50 Ω pulldowns to -2 V termination voltage, Ecl output levels were easily obtained. This allows direct communication between HBT circuits and Si ECL circuits. Complementary outputs are provided, which reduce noise generation due to ground and supply line inductance associated with packaging.

Table 3

Output Logic Levels of HBT Drivers

Protocols	High (V)	Low (V)
ECL	-0.9	-1.7
HECL	-1.5	-2.0
CML	0	-0.5

(a)

(b)
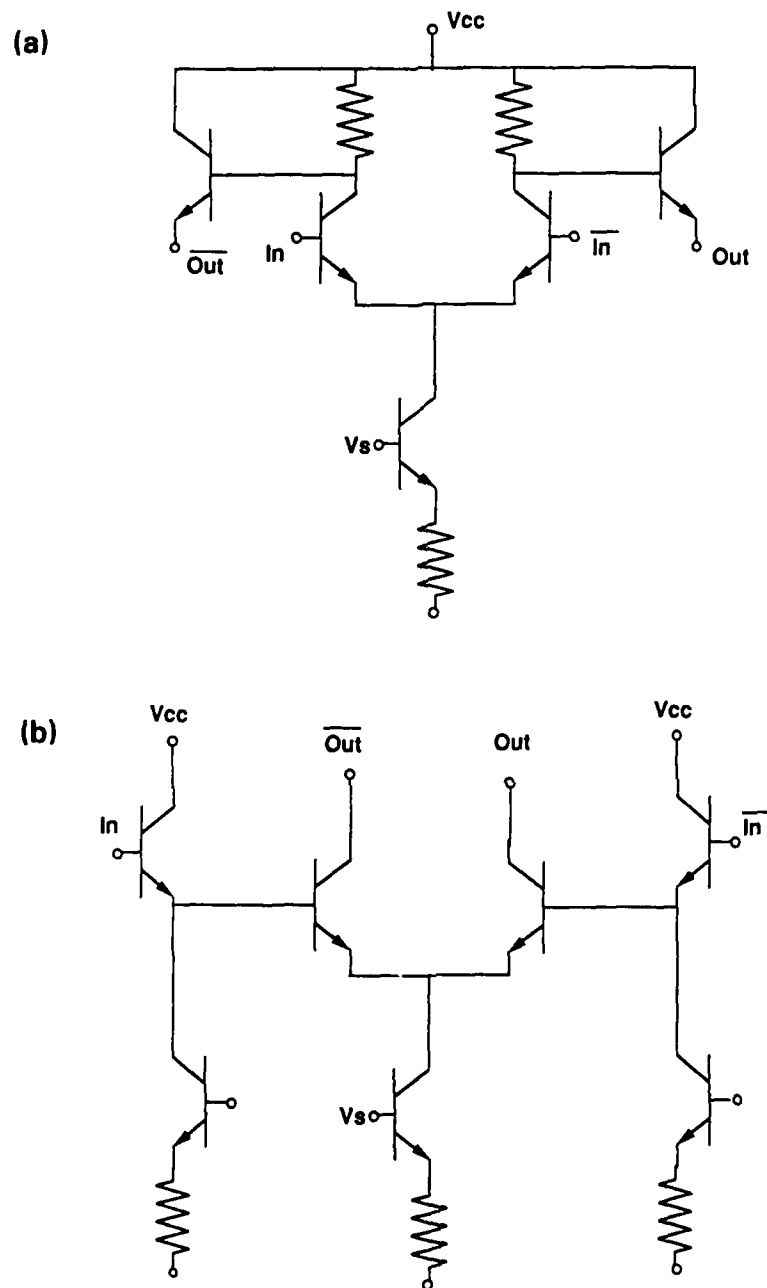
Fig. 41 Circuit diagram for (a) ECL/HECL output driver; (b) CML output driver.

Figure 42 shows the speed-power plots of the 20-80% risetime vs on-chip power consumption. HECL drivers provide best speed-power performance among the three protocols.

The ECL/HECL output was improved by adding emitter followers before the output emitter follower transistors, and adjusting V_{CC1} (for ECL). We have implemented both "old" and "new" ECL/HECL drivers on some of the circuits described below.

7.3   Reference Voltage Generators

There are two kinds of reference voltage involved in the HBT CML circuits. The first is for the inputs of a CML gate, V_{ref}. The second is to control the current through a CML gate, V_s. the V_{ref} for an internal CML gate should be set at the midpoint of the on-chip voltage swing, and that for an input buffer at the mid-point of the input voltage swing. Independent V_s generators are used for the internal CML gate and the output buffer, since they required different currents. Temperature compensation is not included.
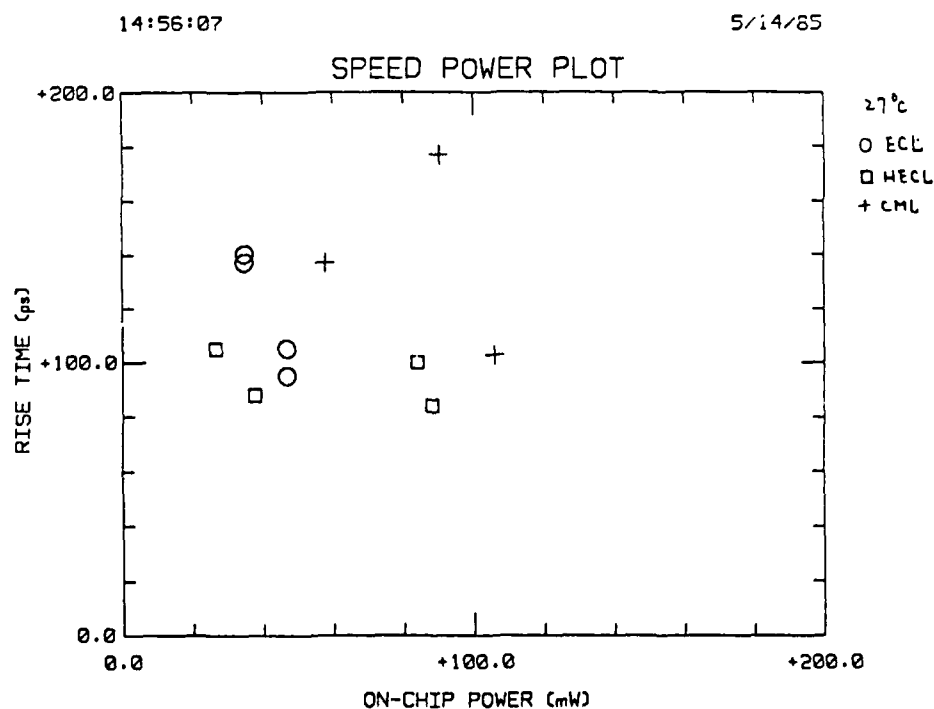
Fig. 42   Risetime vs power dissipation for various output driver circuits according to SPICE simulations.

The circuit diagram of the internal V_{ref} generator is shown in Fig. 43. The same source current as in the internal CML gate flowing through one-half the typical load resistor in a CML gate sets the V_{ref} at the mid-point of an on-chip voltage swing. This swing is typically from -0.4 V to 0 V. An example of the V_{ref} generator for an input buffer is shown in Fig. 44 for ECL input/output protocol. This circuit makes use of the V_{be} drop of a large HBT (transistor H4) to get a V_{ref} of about -1.3 V as needed here.

Fig. 43

Reference voltage generator for
internal circuits.
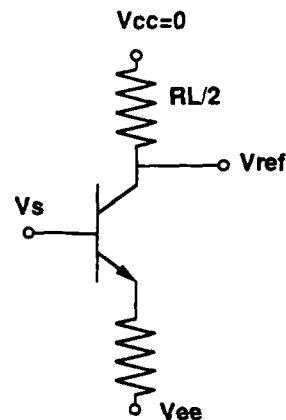
Fig. 44

Reference voltage generator for
external ECL inputs.
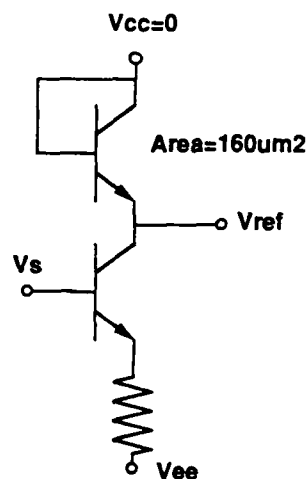
A current source is required for each CML gate. The current is controlled by a voltage reference, V_s, which is generated by a V_s generator. The current, I_s, that flows through each CML gate depends on the configuration of the V_s generator, the number of gates that share the same generator, and the supply voltages V_{cc}-V_{ee}. A SPICE simulation study was carried out to quantitatively evaluate this dependence.

The circuit diagram of the V_S generator and a typical current source load is shown in Fig. 45. Here, two V_S generators are connected in parallel as used in most of our HBT circuits to increase the driving capability. To take care of the loading of N-current sources, the HBT in the current source in the simulation was magnified in area by a factor of N, and the source resistor was reduced by a factor of N as shown in Fig. 45. In this way, N times of I_S flows through the 1 Ω resistor.

Fig. 45

Circuit diagram for V_S generator.
A representative current load equivalent to N gates is also included.
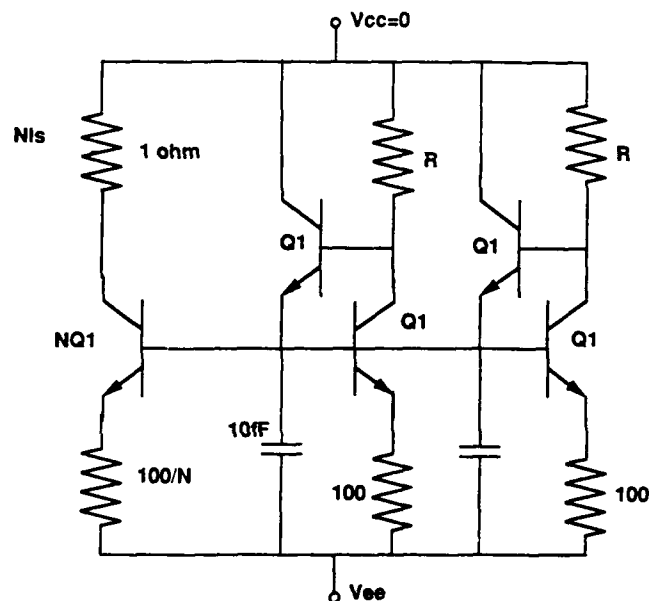
The DB2-Q1 SPICE parameters were used. The calculated current I_S for different R's in the V_S generators and for various numbers of load N are plotted in Fig. 46. We note that the current I_S depends on R more than on N; from detailed fitting one obtains approximately that I_S is proportional to $R^{-3/4}$. For a fixed number of loads, Fig. 46 is useful to determine the value of R to draw a specific current I_S through each CML gate.

Current pulldown circuits were added in the V_S generators. These additional circuits were intended for fast discharge for capacitance associated with the V_S voltage line. They may be useful for reducing the ac transient noise generated or induced on the V_S line when the number of load is small (so there is not enough total base current from the loading circuits to reduce such transient). In the dc only case, our simulation shows no change in current I_S due to these additional circuits.
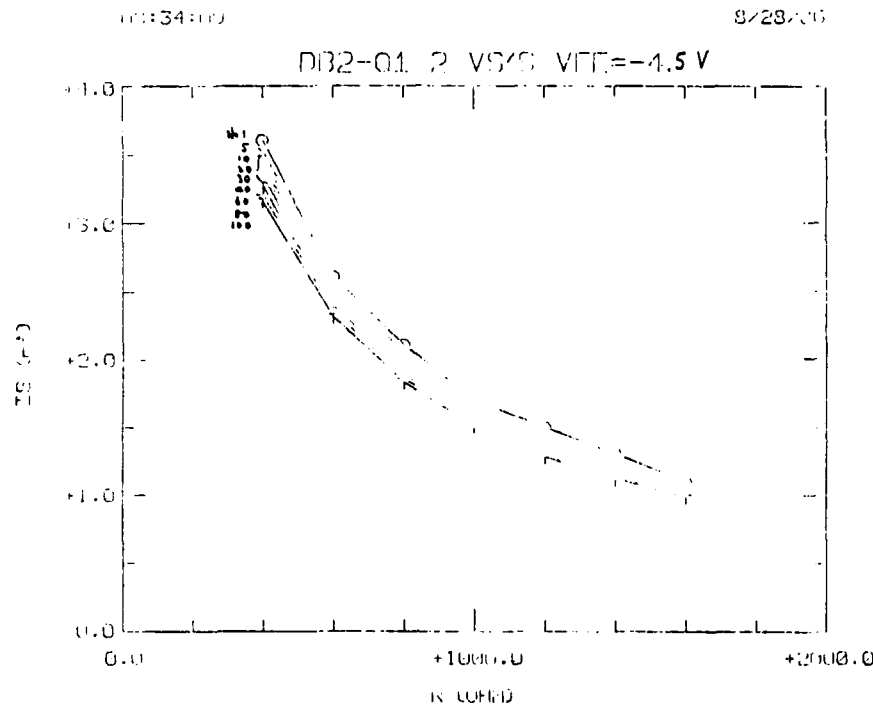
Fig. 46 Dependence of logic source current on resistor value in V_S generator, as a function of load number N.

Simulation showed that I_S varies linearly with V_{ee}, as expected. Throughout the study, V_{CC} was kept at 0 V. In the HBT circuits, we generally separate the V_{CC}'s for the V_S generators and the others, and bring them out separately to pads. This allows convenient adjustment of current I_S by changing V_{CC}'s of V_S generators.

7.4   SSI Circuits

Ring oscillators and frequency dividers were implemented in the mask sets to monitor the speed performance. On the best wafer, which includes proton implant to the collector layer just under the external base region to reduce C_{be}, the following high-speed results were obtained:[1,2] 17-stage NTL ring oscillators operated with propagation delays down to 16.5 ps per stage, with power consumption of about 11 mW per stage (Fig. 47); 19-stage CML ring oscillators operated at 27.6 ps/stage and 5.8 mW/stage (Fig. 48). HBT frequency dividers (÷ 4) were functional with input frequencies of up to 11 GHz, with power consumption of 300 mW (Fig. 49). These room-temperature high-speed performances are among the fastest ever reported on bipolar devices.

17 STAGES

MRDC84-27035

$\tau_d = 18.3$ pS
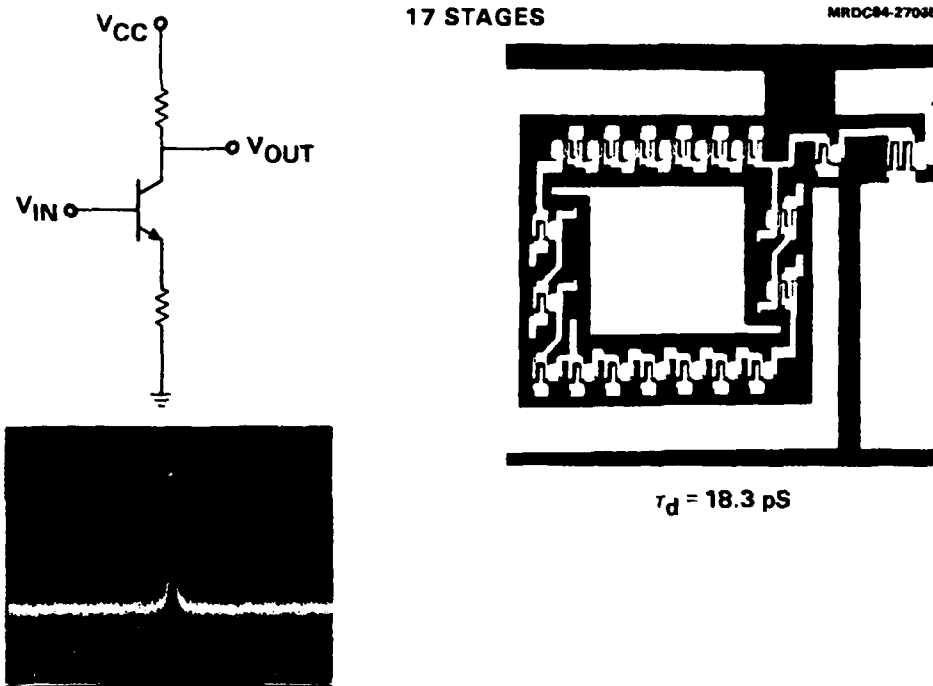
Fig. 47   Nonthreshold logic (NTL) gate, ring oscillator photograph and representative operating frequency.

7.5   MSI Circuits

7.5.1   Eight-Bit Universal Shift Register

Shift registers are common and important circuits in digital electronics. They are often used for data buffering, processing and storage. There are several types depending on the in/out mode (i.e., in parallel or in series). A universal shift register allows either parallel or series input determined by a mode selection (MODE). Parallel output from each bit and serial output from the last bit are available.

The design of an 8-bit universal shift register is shown schematically in Fig. 50. Each bit contains an input buffer, a 2:1 MUX, a CML master-slave latch, and an output buffer. The fabricated shift register is shown in Fig. 51. Figure 52 illustrates the operation of a fully functional shift register in the shifting mode at low frequency. To test the high-speed performance, it is worthwhile to have synchronized clock and input signals. A HBT frequency divider on a separate chip was used for this purpose.
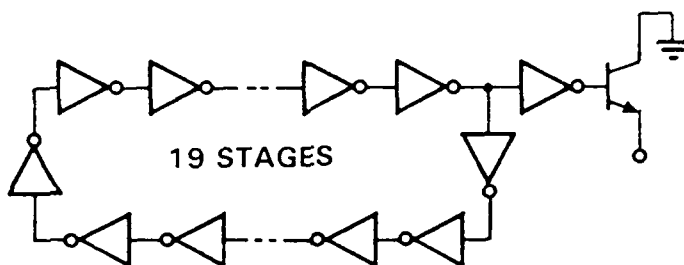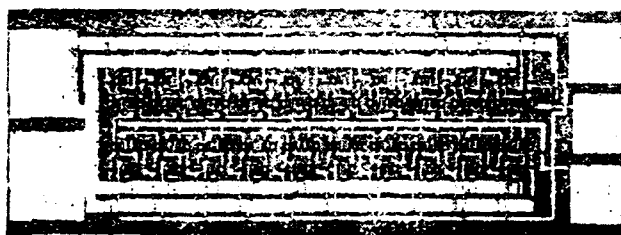
SC28956
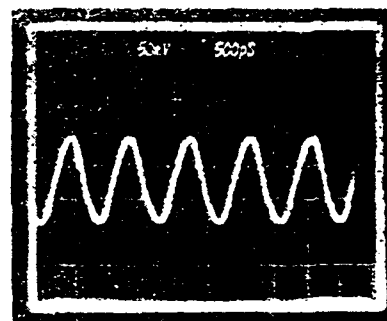
OUTPUT WAVEFORM (÷ 3)

MINIMUM DELAY PER STAGE:

$\tau_d = 23.6$ pS

SC27774

Fig. 48   Schematic CML ring oscillator, microphotograph and representative output waveform.

Figure 53a shows the clock at 3.2 GHz and its ÷ 4 signal used as the input to bit 0 of the shift register. Outputs of bits 0 and 1 are shown in Fig. 53b, with the expected relatively delay of one clock period. Only wafer-probe characterization was carried out; it is likely that output waveforms have been degraded somewhat by the probe inductance.

This circuit is the fastest reported universal shift register to date. It is worthwhile to note that the maximum clock frequency of a universal shift register of this design if $1/(3T_d)$, where T_d is the propagation delay of a compound CML gate. By comparison, the maximum frequency of a corresponding serial shift register (used in numerous DEMUX circuits) is $1/(2T_d)$.

The power dissipation of the shift register was 500 mW, exclusive of the power consumed in the output driver transistors. The circuit yield was outstanding. On the best wafer, on the order of 30% of the devices were fully dc functional.

MASTER SLAVE FLIP-FLOP
CONFIGURED AS 2
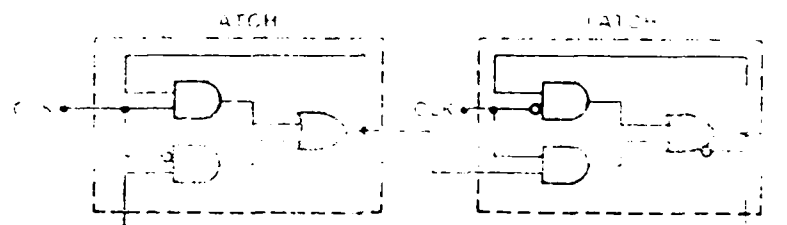
$$f_{max} = 1/2 \tau_d$$
SERIES - GATED CML LATCHES

$$f_{IN} = 11 \text{ GHz}$$

V_{OUT}
(÷ 4)

$$P = 270 \text{ mW}$$
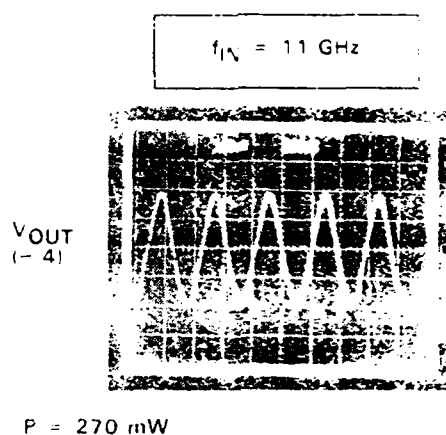
Fig. 49   Frequency divider logic diagram and representative output waveform for 11 GHz operation.
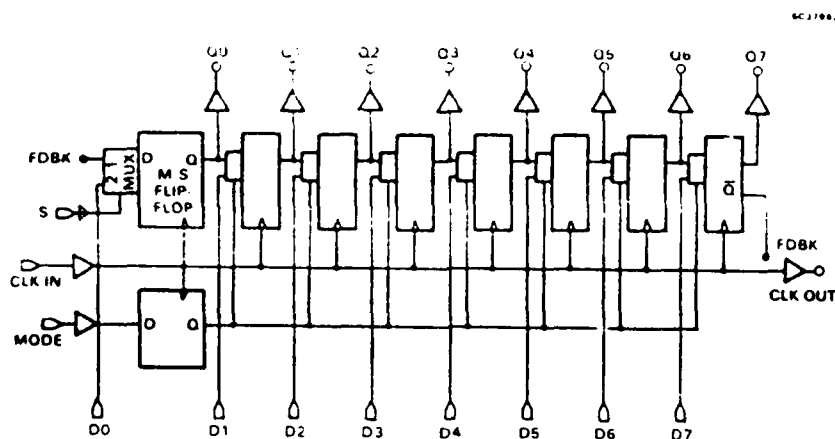
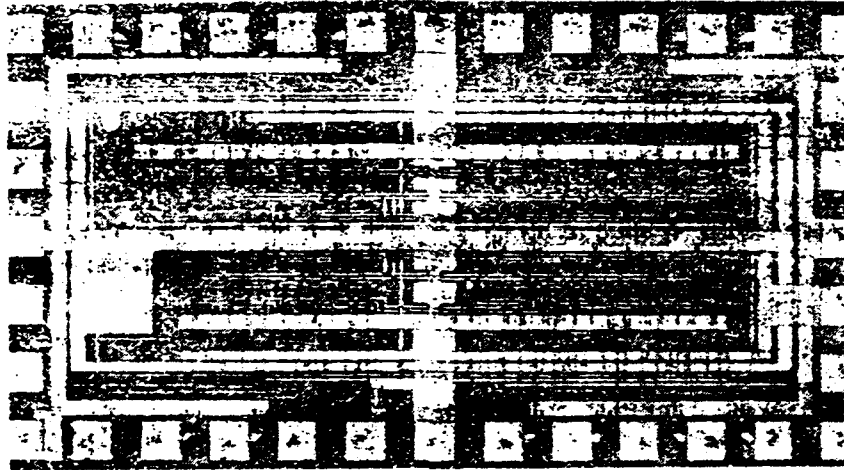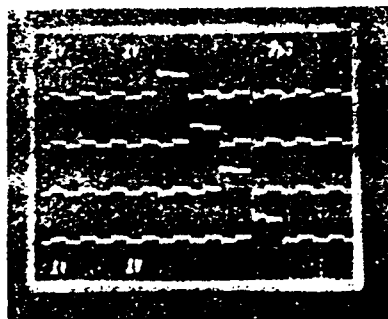Fig. 50 Schematic diagram of HBT 8-bit Universal shift register.
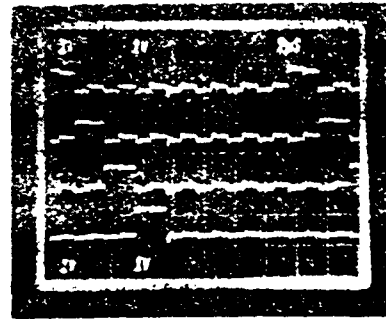
SC39112

Fig. 51 Fabricated Universal shift register with 280 transistors.

SC37122

OUT 0
OUT 1
OUT 2
OUT 3

(a)

OUT 4
OUT 5
OUT 6
OUT 7

(b)

Fig. 52 Low frequency operation of 8-bit shift register.

7.5.2   8:1 Multiplexer

A high-speed MUX is one of the key circuits for communication systems, particularly lightwave systems. The MUX has parallel inputs and one serial output that send out input data in sequence. It allows communication of several channels with only one communication line and data transmission via one channel. We chose to design and fabricate 8-bit MUXs for high speed lightwave applications, and for demonstration of feasibility and performance of MSI implementation of HBT circuits.

SC36590

(a)

200mV   200mV   500pS

INPUT (FROM HBT÷4
ON SEPARATE CHIP)

CLOCK (3.2 GHz)

REPRESENTATIVE OUTPUTS

OUTPUT 1

(b)

200mV   200mV   500pS
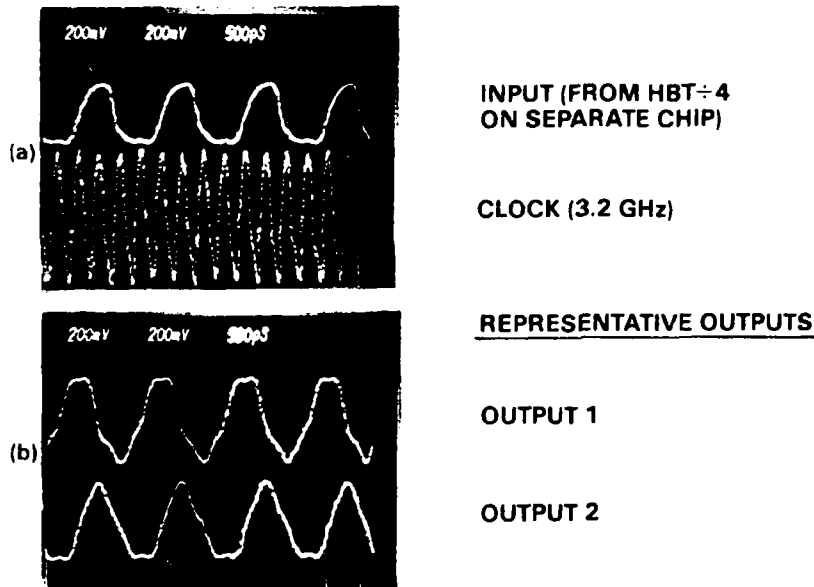
OUTPUT 2

Fig. 53   Input and output waveforms showing shift register operation with a 3.2 GHz clock.

The circuits diagram is shown in Fig. 54a. A free architecture used. The eight inputs are accepted by input buffers which shift the voltage levels to those of the on-chip logic. They are then latched to CML bilevel latches. A pipeline structure was chosen so that four out of eight bits are latched longer then others by a second group of latches. This allows fast performance. On the upper-right part of the diagram, there are seven 2:1 MUXs (Fig. 54b) in groups of four, two and one to carry out standard 8:1 multiplexing. On the lower part are the timing circuits to generate clock signals for latches and 2:1 MUXs. A synchronization signal (SYNC) is needed for initialization of the counters. The required timing signals are realized by ÷ 4, ÷ 2 and simple logic gates. One of the timing signals (S*) is sent out for timing purposes.

The timing diagram is shown in Fig. 54c. The relative timing of all the timing signals is clearly illustrated. The sequence of bit output is shown on the top, as well as the controlling logic for sending out each bit. Times for loading, latching and reading the data bits are indicated at the bottom for the application to data transmission.

The circuits were studied with SPICE simulation. Optimization of the circuits was achieved with the help of the simulation runs by selecting the clock signals for
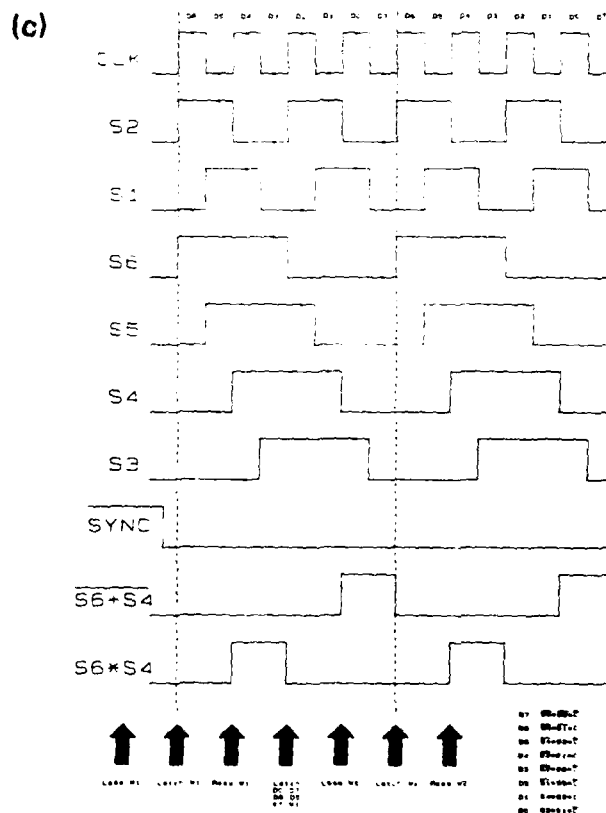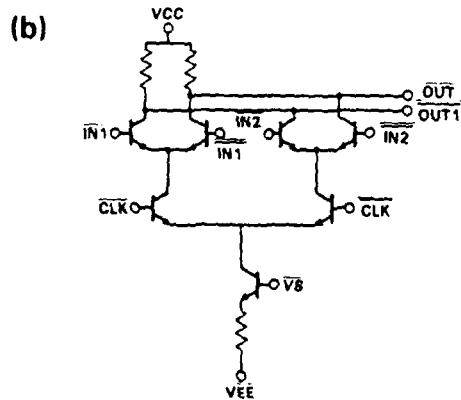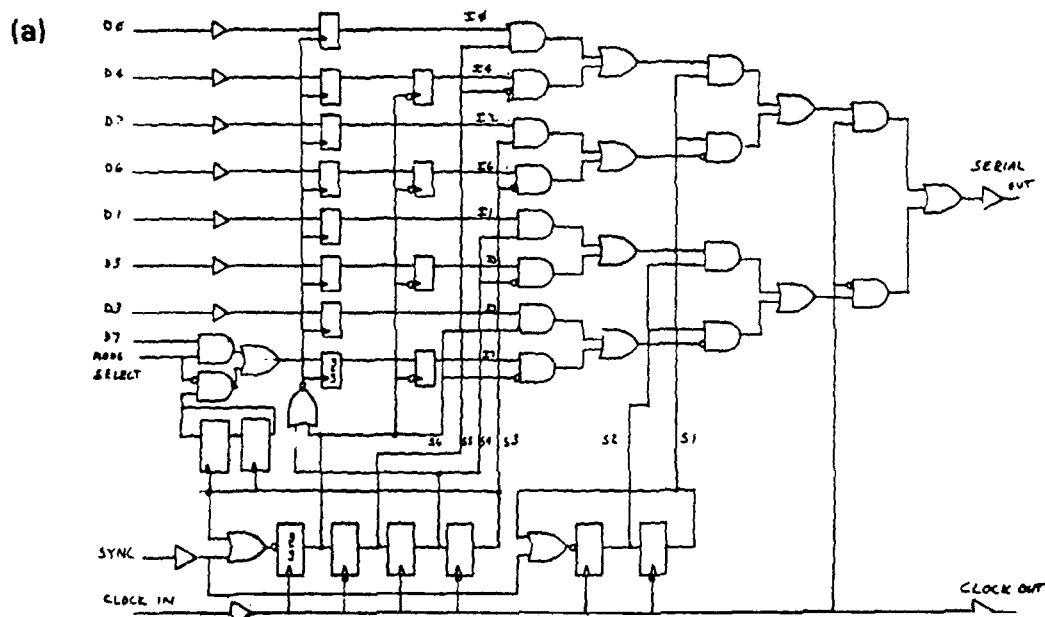
(a)

(b)

Fig. 54

(a) Block diagram of 8-bit MUX circuit.
(b) Circuit diagram of 2:1 MUX building
block. (c) Timing diagram for the MUX.

(c)

latches of the input data and by matching time of the 2:1 MUXs. The output and input signals are shown in Fig. 55. ECL logic levels were used for input and output signals in the simulation. The voltage levels of these signals in this figure were shifted for illustration only. The eight inputs shown in the bottom part were applied to the input ports. The clock and serial outputs of the simulation are shown on the top. Proper logic and timing were observed in the serial output for a clock rate of 5 GHz. This rate corresponds to a MUX rate of 10 Gb/s.

Fig. 55

Simulated performance of 8:1 MUX
according to SPICE modeling.
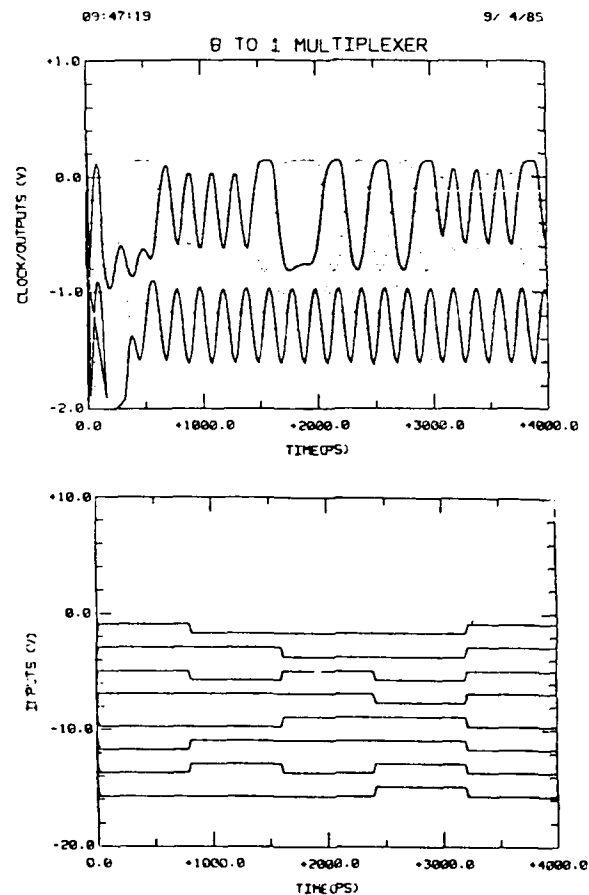
The fabricated 8:1 MUX is shown in Fig. 56. The timing and control circuits, input latches, and all but the last 2:1 MUXs worked properly. However, a mask error in the last 2:1 MUX prevented the full functionality of the 8:1 MUX. This work is being continued under IR&D support.
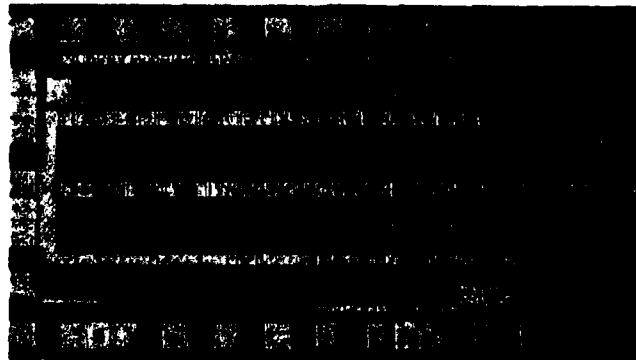
SC39109

Fig. 56 Fabricated 8:1 MUX circuit.

7.5.3 1:8 Demultiplexer

For the receiving end of data communications systems, we have designed and fabricated HBT 1:8 DEMUXs. We chose a tree-type architecture instead of shift register type or parallel latches with controlled timing. In a tree-type DEMUX, the speed requirement after the first 1:2 DEMUX is relatively relaxed, and at the same time the loading to the high-speed data input is minimized. The circuit diagram is shown schematically in Fig. 57. The circuit diagram of the 1:2 DEMUX building block used is shown in Fig. 58. Data flow is directed to either of the two output branches by steering of the source current in the bilevel series-gated CML circuits. There is a latch at each branch to immediately latch the data to allow a nonreturn-to-zero operation.

The results of the SPICE simulation of the 1:8 DEMUX operation is shown in Fig. 59. Data transfer rate of up to 10 Gb/s is anticipated. Figure 60 shows a fabricated 1:8 DEMUX. Testing of this circuit will be carried out under and IR&D program.

7.5.4 Expandable 2:1 Multiplexers and 1:2 Demultiplexers

We have designed, fabricated and partially tested HBT 2:1 MUXs and 1:2 DEMUXs. These circuits make use of the building blocks of the 8:1 MUX and 1:8 DEMUX described above. Input and output buffers are included so that these are stand-alone circuits. In addition, some timing and control signals are brought out to the pads so that the
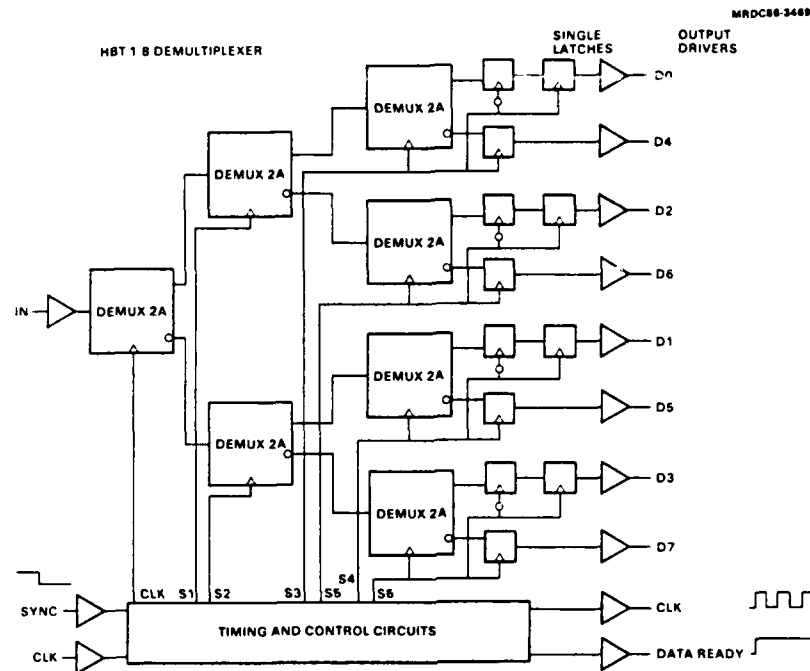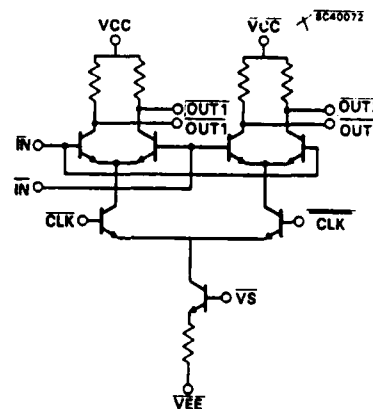
Fig. 57 Block diagram of 1:8 DEMUX circuit.

Fig. 58

Circuit diagram of 1:2 DEMUX building block.

circuits are expandable to higher number of bits by hybrid combining several units together. ECL in/out protocol is used. One may combine these HBT circuits with Si ECL circuits in designing a data communication system.

Two versions of 2:1 MUXs were designed, MU2C and MU2D, and also 1:2 DEMUX, DM2C and DM2D. MU2C and DM2C transmits and receives data, respectively,
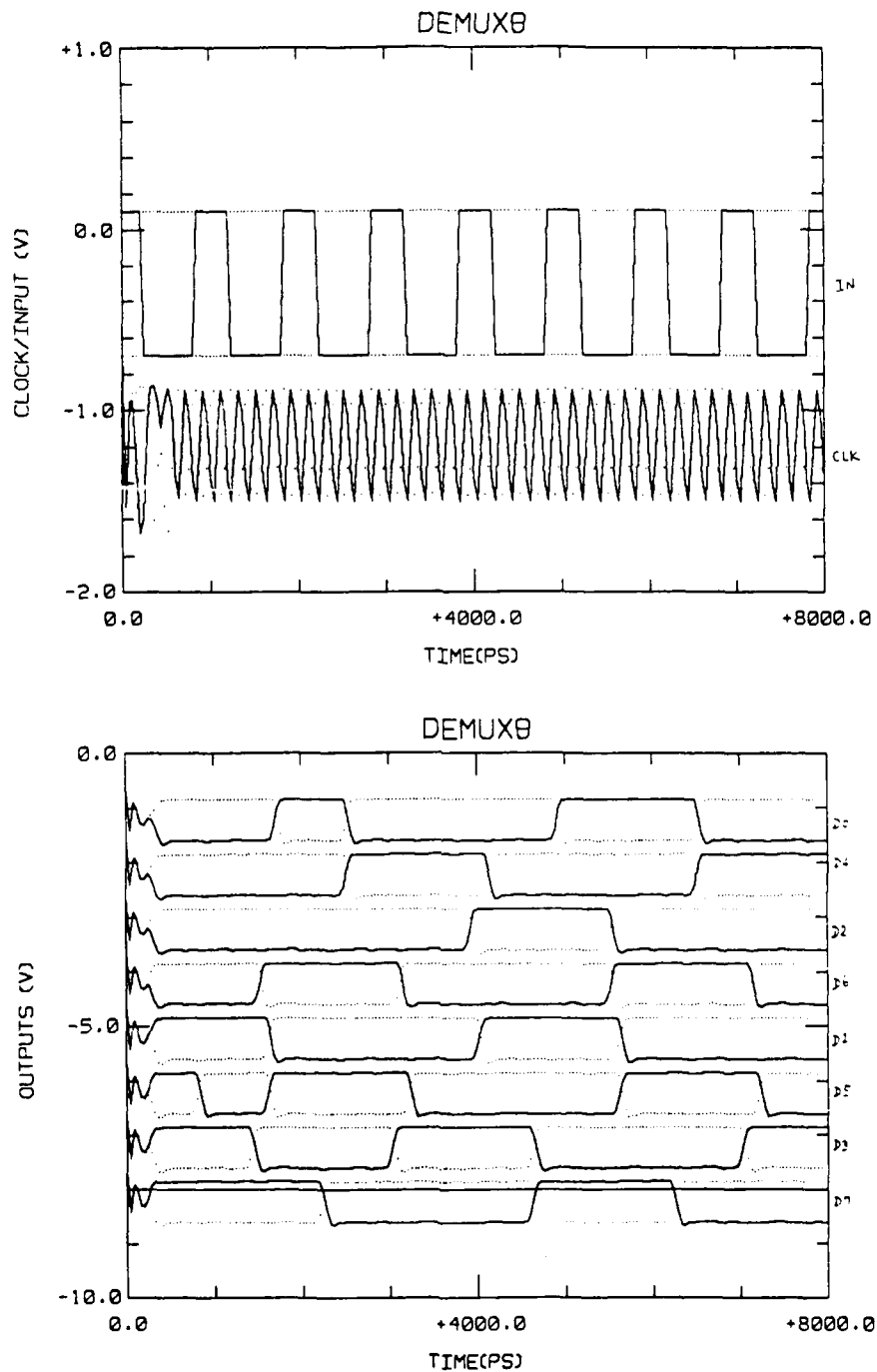
Fig. 59 Simulated operation of 1:8 DEMUX according to SPICE modeling.
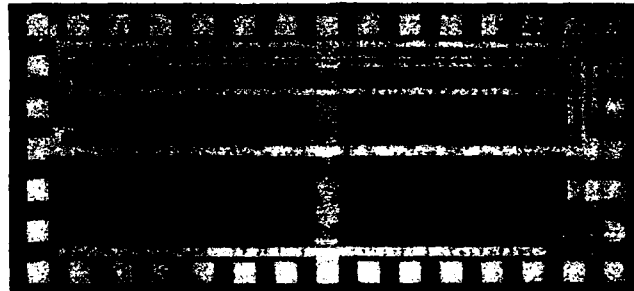
SC39108

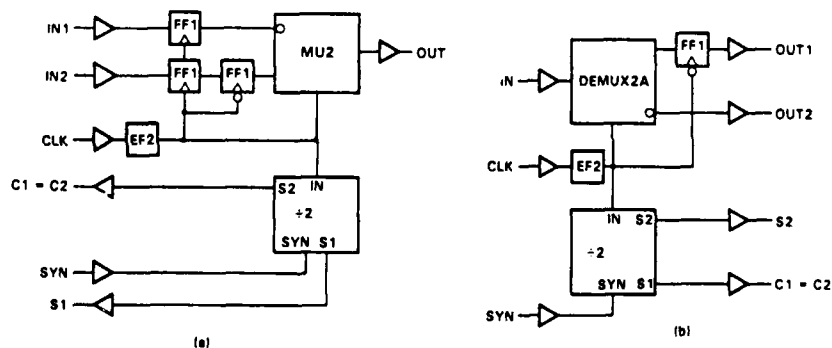Fig. 60 Fabricated 1:8 DEMUX circuit.

SC40073

Fig. 61 Block diagrams of 2:1 MUX and 1:2 DEMUX circuits.

at a rate of two bits per period of input clock, whereas MU2D and DM2D operate at a rate of one bit per period. The first kind allows higher data rate, and the second kind is more compatible with the conventional data communication system design. The circuit and timing diagrams and the scheme for expanding for these four circuits are shown in Figs. 61 through 64.

Microphotographs of these devices are illustrated in Fig. 65. These circuits were tested with an on-wafer probing setup. In quasi-static testing, they were all fully functional. High-speed test was carried out with a limited number of input variations. These circuits worked at input clock frequencies higher than 3 GHz. These results suggested that the data rate of higher than 6 Gb/s may be obtained with MU2C and DM2C. High-speed operation of MU2C is shown in Fig. 65a, and that of DM2C in Fig. 65b.
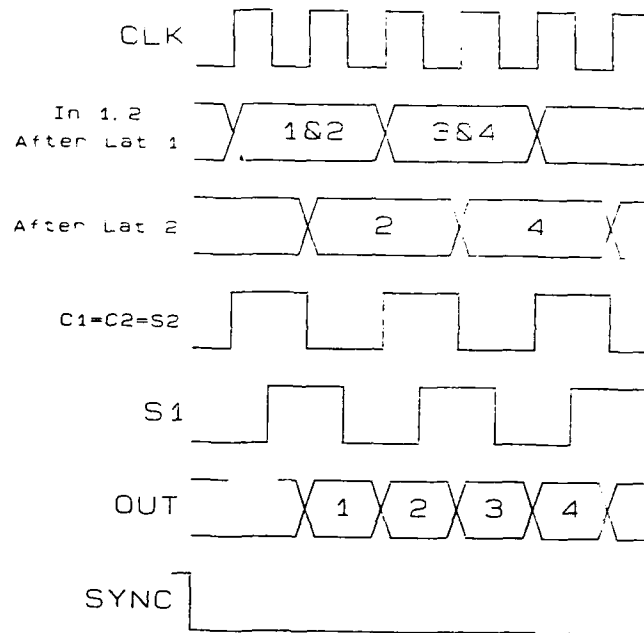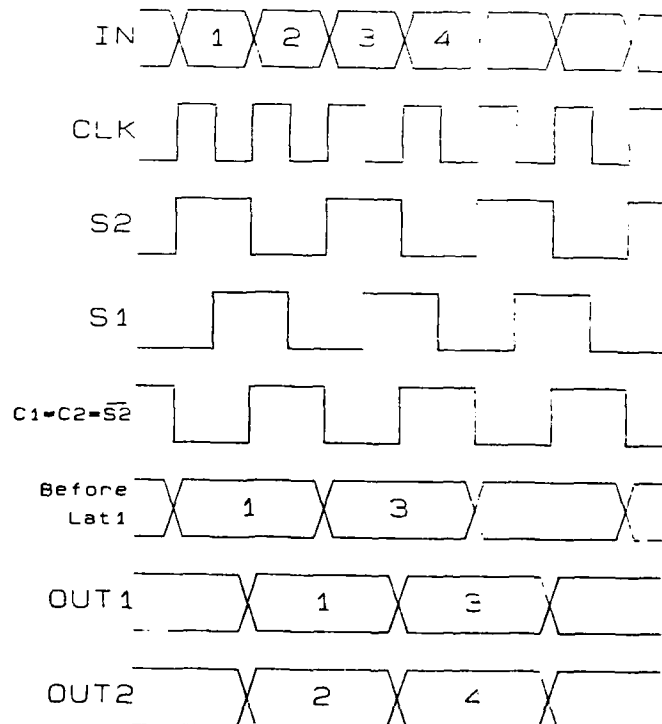
MUX2D

CLK

In 1.2
After Lat 1 — 1&2 / 3&4

After Lat 2 — 2 / 4

C1=C2=S2

S1

OUT — 1 / 2 / 3 / 4

SYNC

Fig. 62

Timing diagrams for operation
of 2:1 MUX and 1:2 DEMUX circuits.

DM2D

IN — 1 / 2 / 3 / 4

CLK

S2

S1

C1=C2=$\overline{S2}$

Before
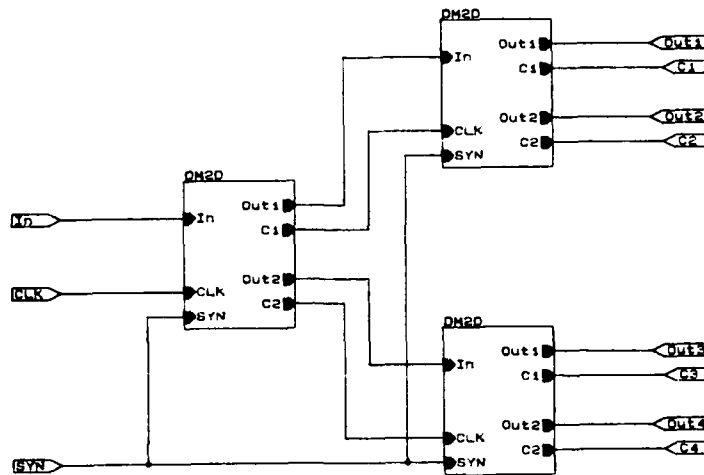Lat 1 — 1 / 3

OUT 1 — 1 / 3

OUT 2 — 2 / 4

DM2D

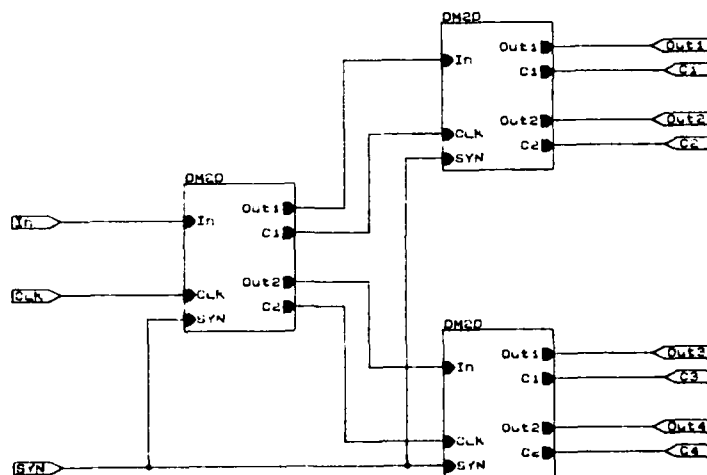Fig. 63 Block diagram showing formation of 4:1 MUX from 1:2 MUX building blocks.

DM2D

Fig. 64 Block diagram showing formation of 1:4 DEMUX from 1:2 DEMUX building blocks.
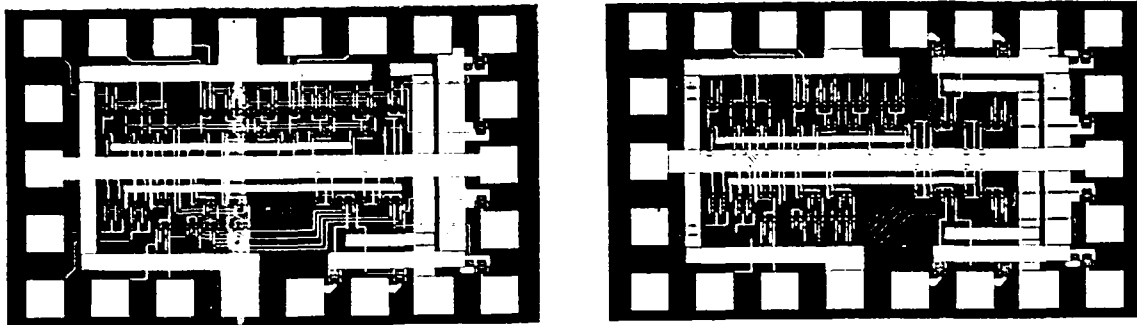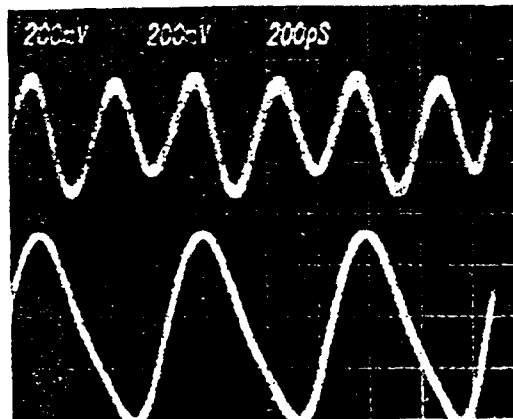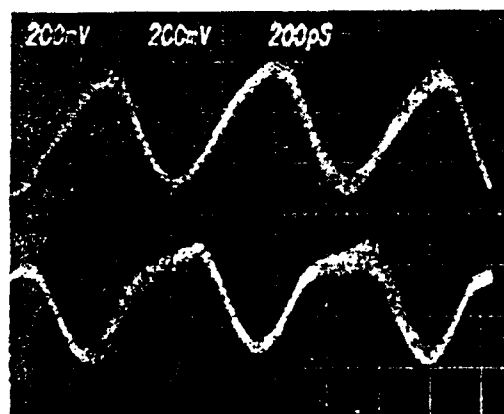
SC39114

Fig. 65 Microphotograph of fabricated 2:1 MUX and 1:2 DEMUX circuits.

(a) SC39107

(b)

OUT 2

OUT 1

Fig. 66 (a) High speed operation of 2:1 MUXC circuit; one input was high, the other low; (b) High speed operation of 1:2 DEMUX circuit. The input signal was clock ÷2.

To fully demonstrate the high-speed functionality of these circuits, further tests are required. The circuits need to be packaged and the study of system performance needs to be carried out.

7.6   Protocol Test Chips

7.6.1   Three-Bit Register

In addition to the MSI circuits reported above, we have designed a 3-bit general-purpose register. Data can be written to and read from it easily. The basic unit of each bit is the same as the shift register, i.e., the CML bilevel latches with master-slave configuration. Circuits for each bit also contain an input buffer and and output driver; there are eight different versions. The purpose of this is to study the speed-power performance of various output drivers, and the effect of different transistor geometry. Output drivers implemented are ECL/HECL and CML, with complementary outputs or single-side output. Transistors are used for the baseline processing and advanced processing (with smaller geometry).

Figure 67 shows a fabricated 3-bit register. On the best wafer, more than 50% of the fabricated 3-bit register were fully functional. An output waveform showing the fast transition is illustrated in Fig. 68.

7.6.2   Gated Full Adder

A full adder is one of the fundamental components in any computer CPU. An adder implemented with HBTs promises very high-speed performance. A gated full adder, which an be used as a basic component for an array multiplier, has been designed, simulated and fabricated. Eight versions were implemented for studies of output driver performance, transistor geometry and processing techniques.

A schematic diagram is shown in Fig. 69. A1*B1 and A2*B2 are added to carry bit CI. The results are the sum SO and carry CO. SPICE simulation was carried out with input waveforms of various frequencies, as shown in Fig. 70. The inputs as well as the outputs are of ECL protocol. DC voltage levels are shifted only on the figure for showing waveforms clearly on one plot. Proper outputs of SO and CO were observed. The timing of the inputs to each internal gate was found to be important for high-speed
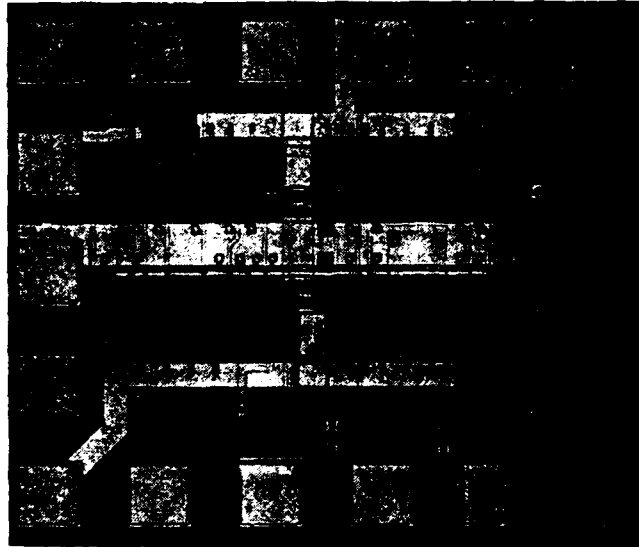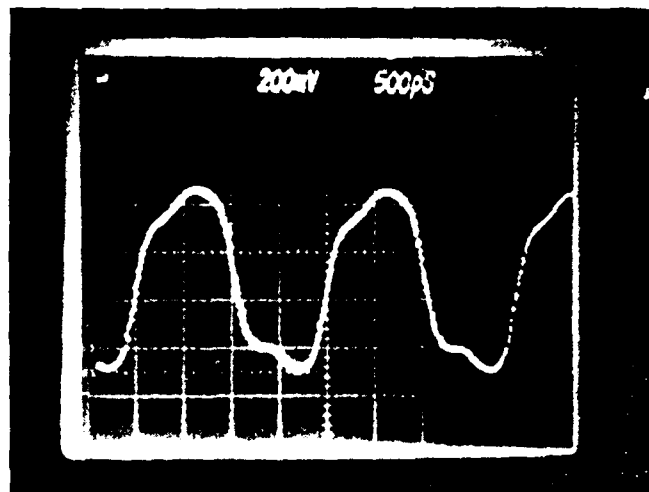
MRDC37124

Fig. 67 Fabricated register protocol test chip.

OUT 1

Fig. 68 Output waveform from register chip.

operation with the SPICE simulation. After implementing appropriate delay for signals I3-bar and I6-bar in Fig. 69 in the simulation, the adder was functional at B2-bar frequency of 5 GHz. The outputs at this speed are shown in Fig. 70.
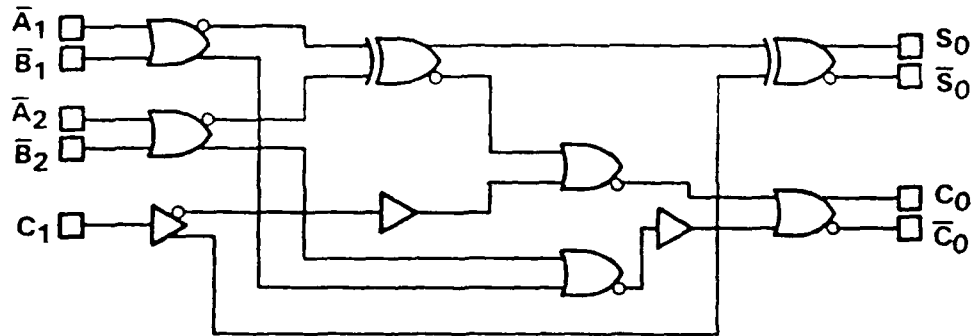
SC37126

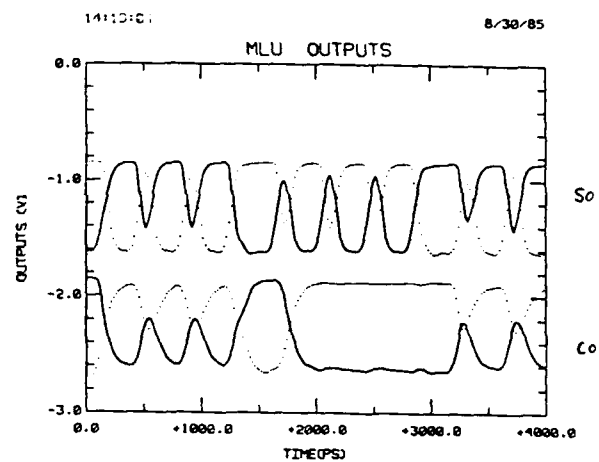Fig. 69 Schematic diagram of gated added protocol test chip.

Fig. 70

Simulated performance of gated adder.
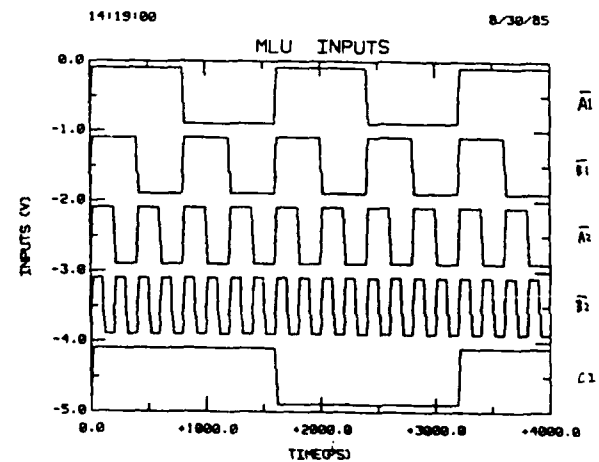
A fabricated adder is shown in Fig. 71. Most of the fabricated adders were fully functional. High-speed tests showed that the gated full adder worked properly at the fastest input of 3 GHz (Fig. 72).

MRDC37126

Fig. 71

Fabricated gated full adder test chip.
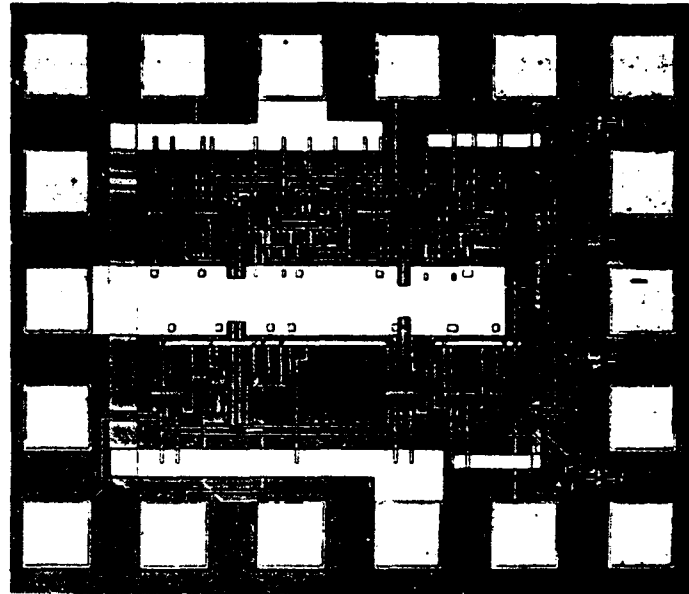
SC39115

$C_I = 1$ $\overline{A}_1 = 0$ $\overline{B}_1 = 1$
B_2 = SINEWAVE AT 3 GHz

$\overline{A}_2 = 0$ $\overline{A}_2 = 1$
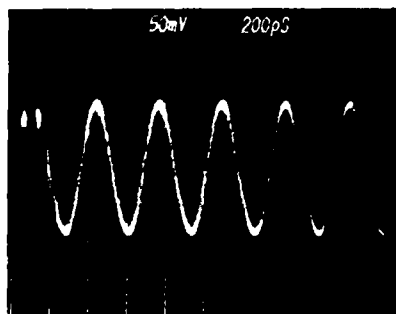
S_O S_O
(D.C. = -1.4V)   (D.C. = 0.8V)

Fig. 72 Operation of gated full adder test chip at 3 GHz.

7.7   Yield

Circuit yield of HBT technology has been significantly improved during the course of this program. The yield as a function of the number of HBTs for circuits on the best wafers is shown in Fig. 73. Data points are from the HB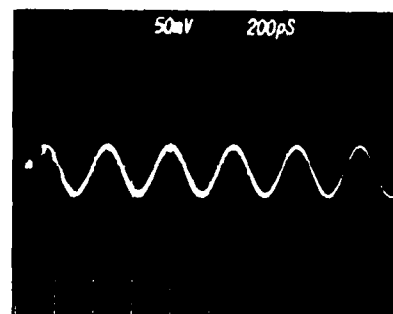T frequency divider, CML ring oscillator, 3-bit register and 8-bit universal shift register. Solid curves indicate the range of the expected yield with our baseline processing at the present time. We anticipate that the yield can be further improved as the HBT processing development continues.
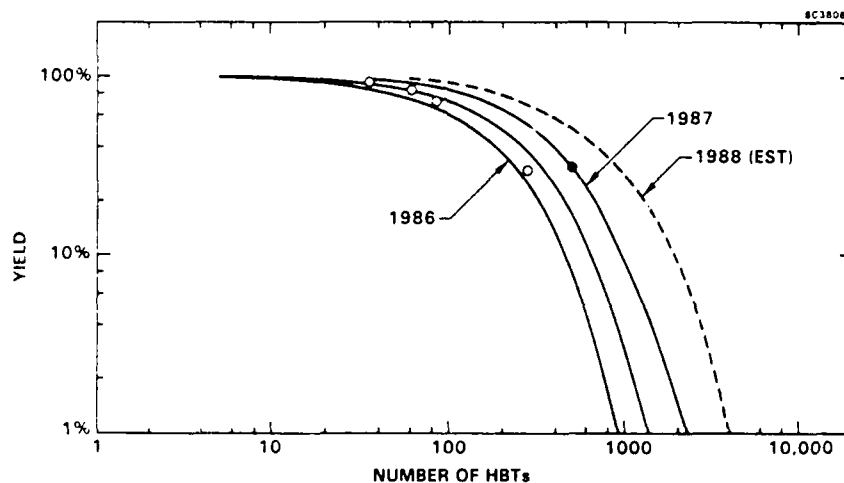
Fig. 73 Plot of experimental functional circuit yield vs circuit size, for best wafers.

7.8   Reliability

As a reliability test of HBT circuits, a NTL ring oscillator has been operating for five months at 100°C and five months at 150°C without failure. The frequency of the oscillation was decreased from 0.652 GHz to 0.548 GHz, as shown in Fig. 74.

7.9   Radiation Hardness

In regard to radiation hardness, a NTL ring oscillator with operating bias voltage on has withstood 55 Mrads total dose. Operation of the ring oscillator as a function of the bias voltage before and after radiation is shown in Fig. 75. Two NTL ring oscillators died during the test. It is possible, however, that at least one of them died due to improper handling of the circuit.

frequency (MHz)

Fig. 74   Measured variation of HTL ring-oscillator operating frequency as a function of
time during life testing at 100°C and 150°C.

Fig. 75   Operating characteristics (frequency vs bias voltage) of an NTL ring oscillator
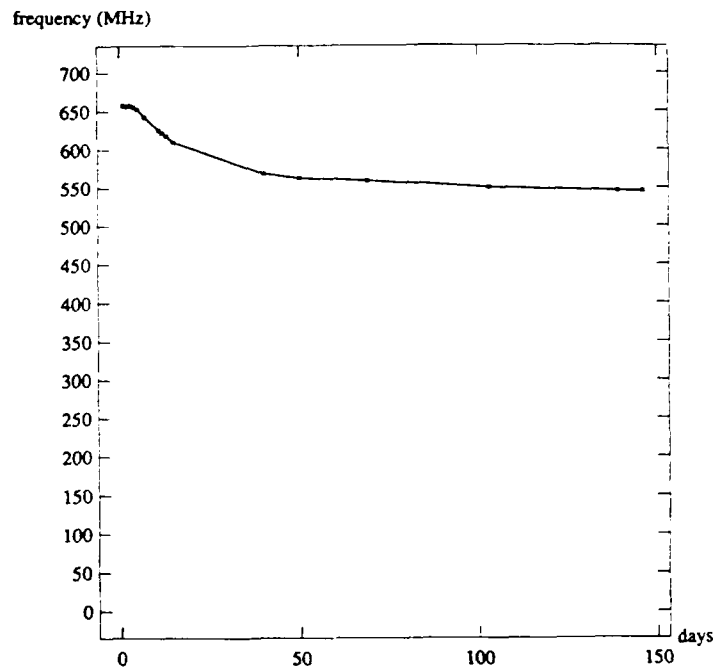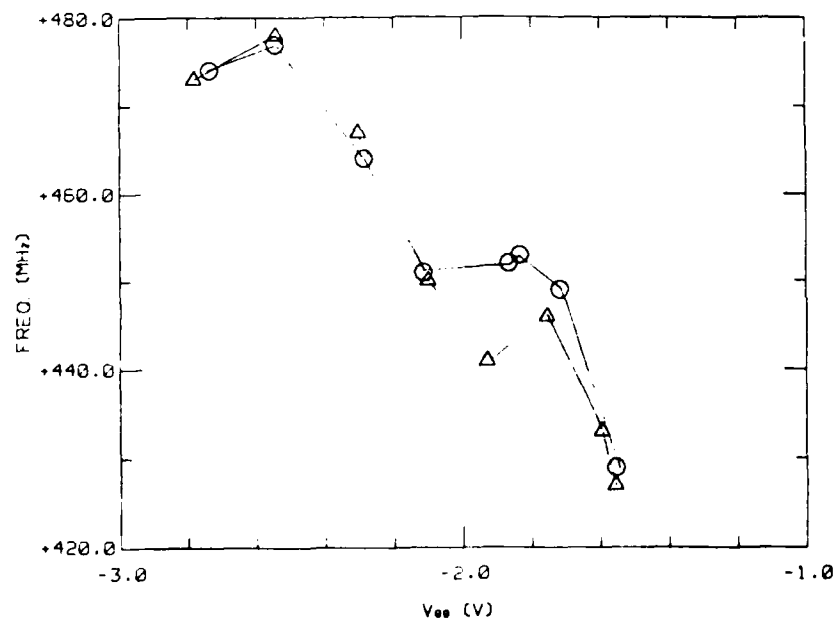before and after exposure to 55 Mrads.

8.0 PRESENT HBT TECHNOLOGY STATUS AND SUGGESTED FUTURE WORK

This section summarizes the status of HBT technology, and discusses its potential for the implementation of useful circuits. MSI digital circuits (which have been the principal focus of this project), as well as other types of circuits, including analog, microwave and mm-wave circuits, are discussed.

8.1 MSI Digital Circuits

For a variety of applications it is important to achieve exceptionally high operating speed in digital circuits. Such applications include high speed front ends to systems, where high data rates are slowed down for later processing by more conventional circuits. Prescalers and frequency dividers, and data multiplexers and demultiplexers are examples of this class. Other circuits incorporate an entire high-speed signal processing function such as encoding or scrambling; or bit-slice addition, logic or multiplication. HBTs are well suited to the fabrication of these circuits, because they provide exceptionally high f_t in a technology that is achievable with straightforward optical lithography.

Among Si technologies, bipolar transistors in ECL circuits have long been the leaders in high speed performance. The development of HBT ECL (or HECL) reflects the conviction that this will also hold true within the III-V technologies. Developments in the present program are beginning to bear this out.

- Values of cutoff frequency, f_t, as high as 150 GHz are predicted for HBTs even with 1 μm optical lithography. f_t values up to 40 GHz have been achieved in this program. By contrast, GaAs MESFETs with 1 μm channel lengths have $f_t \sim 15$ GHz and HEMTs have $f_t \sim 25$ GHz with similar dimensions. In Si bipolars, f_ts have reached 17 GHz only with ultranarrow (0.35 μm) dimensions.

- HBT ring-oscillator speeds have been steadily improving and recently, propagation time delays as low as 16.5 ps were obtained in this program for Nonthreshold Logic (NTL) circuits.

- HBT frequency dividers have operated with input frequencies up to 11 GHz. These circuits are the fastest reported to date (for any technology).

- MSI circuits with HBTs recently demonstrated at Rockwell are among the fastest circuits of their type ever reported. An eight-bit universal shift register operated at 3.2 GHz, while the fastest universal shift register previously reported corresponds to 1.5 GHz.

Beyond raw speed, a variety of characteristics must be demonstrated before a candidate technology can be considered for system applications. Among these are reliability, operation over temperature, radiation hardness, acceptability of input/output protocols, reproducibility and yield. This program has led to some important demonstrations:

- In regard to reliability, ring-oscillators have operated 1500 h at 100°C without failure, and 300 h at 150°C without failure.

- In regard to radiation hardness, a ring oscillator has withstood 50 Mrads total dose. (Device failure for uncertain causes occurred above this.)

- In regard to I/O protocols, HBT circuits were shown to provide high speed ECL outputs in a much more power efficient manner than MESFETs. Complementary outputs can be easily provided to eliminate ground inductance effects.

- In regard to yield, outstanding results were obtained on the MSI circuits with values on the order of 30% obtained on the best wafer.

These demonstrations are very promising. MSI circuit operation at even higher speeds is required, however, in a variety of systems envisioned at present. For example, data transmissions at 10 Gbits or above should be possible in fiber-optics communication systems. HBT technology is the most promising technology to provide the required MSI circuits for this.

8.2   LSI Digital Circuits

The ECL approach emphasizes high speed, but requires moderate or high power dissipation. For example, as Rockwell's technology has evolved, it has yielded progressively lower power values per gate, but power requirements still are in the range 2-5 mW/gate for CML. Further improvements will be obtainable, but it is not presently considered that circuits beyond 1-5K gate complexity will retain a significant performance advantage. For example, a 10K gate chip dissipating 4 W would require 200-300 μW/gate (after allowance for I/O dissipation). This range may be possible for HBT/CML circuits, but it is not evident that many of the performance advantages of HBTs over Si circuits will be preserved in this regime. In particular, in this "power-starved" regime, the power-delay product together with allowed power determines the gate speed. The HBT power-delay product in the VLSI limit is not much different from that of Si bipolar circuits. In fact, present HBTs suffer from a slightly higher value of turn-on voltage.

In contrast to CML circuits, HI^2L circuits are oriented toward low power operation. They can be used in the 200 μW/gate regime, and thus, are candidates for LSI applications. Unfortunately, the relationship between the power-delay product of GaAs and Si implementations of the circuits is similar to the case of CML and for the same reason (higher value of V_{BE}).

For long-term development of an appropriate LSI digital technology based on HBTs, with a significant power delay advantage over Si ECL, novel semiconductor systems must be considered. In particular, compounds with a relatively low energy gap should be employed in the base region of the device (while emitter and collector regions are composed of wide band gap materials). InGaAs (lattice matched to InP) is a candidate material for such applications.

8.3   mm-Wave Applications

Because of their vertical nature, tight controls over the primary HBT device dimensions are achieved during epitaxial growth, not during subsequent device processing. As a result, HBTs are promising for the achievement of very high values of f_t and f_{max}, and allow simple processing based on available optical lithography. Moreover, because of high current handling capability and high breakdown voltage, they

should be well suited to high power and high efficiency applications. Already, discrete devices with f_{max} above 40 GHz have been obtained. To attain high f_{max}, it is of great importance to minimize base resistance. This may be accomplished by using very high values of base doping on the order of 10^{20} cm^{-3}. Further increases in f_t and f_{max} are to be expected, through the optimization of the vertical structure of the transistor, increase in base doping, and minimization of device dimensions.

8.4   Microwave Power ICs

The high current handling capability of bipolar transistors is a significant advantage for microwave power applications. In addition, with HBTs it is straight-forward to tailor the breakdown voltage by appropriate choice of the thickness and doping of the collector drift region. Experimental devices show the expected high break-down voltages. Collector-emitter breakdown voltage above 12 V, and collector-base breakdown above 25 V is obtained in the same wafer that provides the highest f_{max}. It is expected that HBT amplifiers and oscillators will be capable of very high power-added efficiency in this frequency range. Experimental investigation of this area is just beginning. The principal areas of investigation include thermal modeling, understanding of breakdown and saturation behavior, interconnection geometry development, and large signal rf simulation.

8.5   Wideband Analog Circuits

It is believed that a significant opportunity exists to apply present or near-term HBT technology to improve performance of operational amplifiers and other dc coupled feedback amplifiers. The circuits will benefit from the high voltage and current gain obtainable with HBTs; their well-behaved characteristics from dc through the microwave regime; their well-matched I-V curves; and their low 1/f noise. Device requirements are similar to those needed for digital MSI circuits. The modeling/ simulation/device characterization requirements of these two areas also overlap extensively, and corresponding developments reinforce each other. The wideband analog application area, nonetheless, has to date received very little attention.

8.6 Analog-to-Digital Conversion

The threshold voltage control inherent to HBTs, as well as their high f_t, high transconductance, and absence of trapping effects, form the basis of substantial interest in this technology for high speed, high accuracy A/D converters. HBT comparators with low offset voltages (less than 4 mV) and high speed capability (2.5 GHz operation) have been reported. Prospects are good for the use of these prototype circuits in large, "flash" monolithic A/D converters to achieve resolution up to 8 bits, and speeds up to 1-2 GSps. Further advances, particularly in complexity and integration level, may be expected in this area. The principal technology development requirements are reproducibility and yield; speed, power dissipation, and transistor size have somewhat secondary roles.

In summary, significant opportunities exist for development and application of HBT to improve performance of defense systems. HBT devices in ECL/CML circuits have a natural role in ultrahigh speed SSI and MSI applications in the digital, analog microwave and combined analog/digital areas. With present technology, HBTs are competitive with other candidate technologies for highest speed operation. Further HBT technology improvements remain to be done that should propel HBT circuits to a leadership position.