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FINAL REPORT

15 July 1985 through 14 July 1987

Contract N00014-85-K-0700

STUDY OF CRYOGENIC MODFETS

CORNELL UNIVERSITY

Ithaca, New York 14853

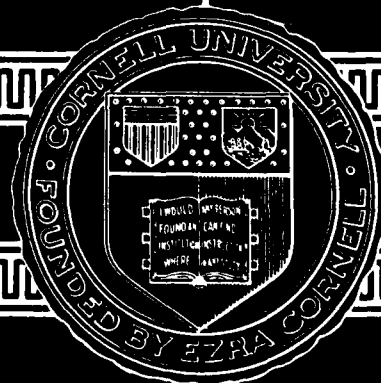
Principal Investigators

L.F. Eastman, G.W. Wicks, P.J. Tasker

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STUDY OF CRYOGENIC MODFET's

Report prepared by Lester F. Eastman

INTRODUCTION

When temperatures of operation of transistors are lowered, improved performance results. This program concentrated on means of improving heterojunction field effect transistors of the modulation doped variety, called MODFET's. The reduced temperature of 77 K was chosen for convenience, but 12-15 K was also tested in conjunction with a joint program with General Electric. As a follow-on of this joint effort, G.E. supplied low noise MODFET's to the Jet Propulsion Laboratory for the highly-successful probing of the planet Neptune.

This report is broken down into sections covering the technical background, MBE materials growth and characterization and MODFET fabrication and testing.

TECHNICAL BACKGROUND

Modulation-doped field effect transistors have a layered materials structure with a smaller bandgap, undoped channel, adjacent to a larger bandgap, doped barrier. Normally the barrier layer is on top. The most common early MODFET consisted of doped Al,GaAs barriers on GaAs undoped channels, all grown by MBE on GaAs semi-insulating substrates. In spite of major advances in room temperature low noise performance using In,GaAs alloys, the simpler GaAs channel has been shown to be superior for cryogenic low noise applications. An example¹ is that short-gate, GaAs-channel MODFET's operated at 15 K yielded 5.5 K noise temperature,

compared with the 20 K noise temperature in short-gate, strained $\text{In}_{0.22}\text{Ga}_{0.78}\text{As}$ -channel MODFETs, on GaAs substrates, operated at the same temperature.

What is required for low noise figure amplification at low temperature is very high unity current-gain frequency, f_t , and very low input resistance, composed of the source resistance, R_s , plus the gate resistance, R_g .

The equation for noise figure for MODFET's is:

$$\text{NF} = (10) \log_{10} (1 + 1/6 (f/f_t)(g_m(R_s + R_g))^{1/2})$$

where f is the operating frequency, f_t is the above-mentioned unity-current-gain frequency, g_m is the mutual transconductance, and R_s and R_g are as mentioned above. Both f_t and g_m are directly dependent on the average electron transit velocity. This velocity is $\sim 1.5 \times 10^7$ cm/s at room temperature for an undoped GaAs channel with a high AlGaAs barrier, and is 2.5×10^7 cm/s at 77 K for the same structure. These data were determined from SISFET performance with such structures.² Cooling the devices to 77 K, the rise in this velocity will give only moderate improvement, since the second term is proportional to $(v_e)^{-1/2}$.

The key to getting the lowest noise figure is obtaining both low R_s and R_g at low temperature, as well as a short gate and a high v_e . The gate metal resistance lowers in direct proportion to the temperature. Additionally, the use of gates with mushroom cross section, initially developed at Cornell, and used by GE, Hughes Research, and others, sharply reduces the gate resistance by increasing the cross sectional area by a factor of about 6-8. Should it be required, extra drive points to the gate, shortening individual gate fingers, is

of further benefit, since the gate resistance is equal to:

$$R_g = (W_g \rho_g) / 3n_f^2$$

where W_g is the gate periphery in mm, ρ_g is the longitudinal gate resistivity, in Ω -mm (typically 120 Ω - μ m for .25 μ m long mushroom gates at room temperature), and n_f is the number of fingers (2 for one gate drive point, 4 for two gate drive points, and 6 for three gate drive points) etc.

As can be seen from the mathematical form of the noise figure, both R_s and R_g must be reduced together to nearly the same magnitudes, in order to optimize noise figure. Thus it is essential to have the lowest possible R_s . Alloyed ohmic contacts yield .05 - .20 Ω -mm contact resistance to MODFET's, and these values are nearly independent of temperature, since they are determined by tunneling effects. Thus the key parameters are the channel sheet resistance, and geometry, when the ultimate cryogenic noise figure is required.

The channel sheet resistance is determined by the product of the two-dimensional electron gas (2DEG) sheet density, and the low field mobility. It is possible to get about $.8 \times 10^{12}/\text{cm}^2$ electrons in such 2DEG's in GaAs channels and about 90,000 $\text{cm}^2/\text{V-s}$ electron mobility at 77 K, with a thin (20-40 Å) spacer layer. The 300 K electron mobility is $\sim 6,000 \text{ cm}^2/\text{V-s}$. This spacer layer is an undoped region of the Al,GaAs barrier layer adjacent to the GaAs channel. If this spacer layer is raised to 150-200 Å, the 77 K electron mobility rises to $\sim 210,000 \text{ cm}^2/\text{V-s}$, but the electron sheet density is lowered to $2-3 \times 10^{11}/\text{cm}^2$. With thick spacer layers, the electron mobility gradually rises with lowered temperature, reaching over $1 \times 10^6 \text{ cm}^2/\text{V-s}$ at a few °K.

Thus the normalized source resistance, for a GaAs channel and for a $.5\text{ }\mu\text{m}$ spacing between source and gate, is lowered from $.65\text{ }\Omega\text{-mm}$ to about $.09\text{ }\Omega\text{-mm}$ at 77 K. These yield $6.5\text{ }\Omega$ and $.9\text{ }\Omega$ respectively for R_s , for $100\text{ }\mu\text{m}$ periphery. The $.25\text{ }\mu\text{m}$ mushroom gate resistance, for one gate drive point (2 fingers), and $100\text{ }\mu\text{m}$ periphery, is lowered from $\sim 1.0\text{ }\Omega$ to $\sim .25\text{ }\Omega$. It is clear that even more effort on the reduction of the source resistance would be fruitful in lowering the noise figure, since R_s of $.9\text{ }\Omega$ is still substantially larger than the $.25\text{ }\Omega$ gate resistance, although the latter has some small parasitic contribution from the drive line.

Other materials have been investigated in order to lower the channel sheet resistance. One approach is the use of pseudomorphic (strained-layer) $\text{In}_y\text{Ga}_{1-y}\text{As}$ channels on GaAs substrates. This raises the potential barrier height, allowing up to $2.4 \times 10^{12}/\text{cm}^2$ electron sheet density, for $y = .25$. The electron mobility at room temperature has a minor reduction in value, but this mobility at 77 K is reduced from the high value for GaAs channels, to $\sim 20,000\text{ cm}^2/\text{Vs}$. Because of the tripled density of electrons in the 2DEG, the room temperature sheet resistance is reduced. The source resistance can be lowered below $.5\text{ }\Omega\text{-mm}$, and $.35\text{ }\Omega\text{-mm}$ has been obtained³ in the highest performance device with 25% Indium in the channel. For cryogenic operation, however, these pseudomorphic devices have such a limited rise in electron mobility, as discussed below, compared to GaAs channel devices, that their low noise performance is worse than that for the GaAs channel devices.

Using lattice-matched $\text{In}_{.53}\text{Ga}_{.47}\text{As}$ channels on InP, the electron sheet density is raised to over $3 \times 10^{12}/\text{cm}^2$, but the mobility is experimentally limited to about $60,000\text{ cm}^2/\text{V-s}$ at 77 K. The sheet resistance of the latter is only .4 times that of GaAs channel MODFET's, 77 K and could eventually out

perform GaAs MODFET's. At extremely low temperature (~ 15 K), alloy scattering limits the mobility of the $\text{In}_y\text{Ga}_{1-y}\text{As}$, with this scattering rate dependent on $[y(1-y)]$. Thus the best channel for 15 K operation is a binary compound semiconductor, rather than a ternary alloy.

MBE Grown $\text{Al}_x\text{Ga}_{1-x}\text{As}/\text{In}_y\text{Ga}_{1-y}\text{As}/\text{GaAs}$ Materials

When $\text{Al}_x\text{Ga}_{1-x}\text{As}$ is grown with $x \geq .23$, any dopants are deep and cause difficulties. Any carriers in the barrier layer freeze out and are trapped, yielding a collapse of the $I(V)$ characteristics at low voltage and cryogenic temperatures. Even so, x values up to .30 can be used in doped barriers at room temperature, although the lower values of x ($\leq .25$) are necessary at 77 K. At very low temperatures, light can be used to untrap the carriers, if necessary, when $x > .23$ is used.

The use of GaAs channels was chosen for the initial part of this program, and layers with and without a $1 \mu\text{m}$ $\text{Al}_{.1}\text{GaAs}$ buffer layers were grown and processed into the devices. With $130 \text{ \AA}$ GaAs quantum wells, low device output conductance resulted, even with short gate devices, due to the confinement of the carriers below the 2DEG, as well as above the 2DEG, improving performance.

The device and layer structure used are shown schematically in Figure 1. It shows the $\text{Al}_{.3}\text{Ga}_{.7}\text{As}$ buffer layer, the $130 \text{ \AA}$ GaAs quantum well, the undoped $85 \text{ \AA}$ $\text{Al}_{.3}\text{Ga}_{.7}\text{As}$ spacer layer, as well as the remaining doped top layers. The structure was grown at 680°C by MBE. This structure yielded $120,000 \text{ cm}^2/\text{V-s}$ electron mobility at 77 K.

In order to achieve higher electron sheet density, with high electron mobility at 77 K, pseudomorphic $\text{In}_y\text{Ga}_{1-y}\text{As}$ channels on GaAs substrates were also grown, in hopes of improving performance. For comparison, GaAs

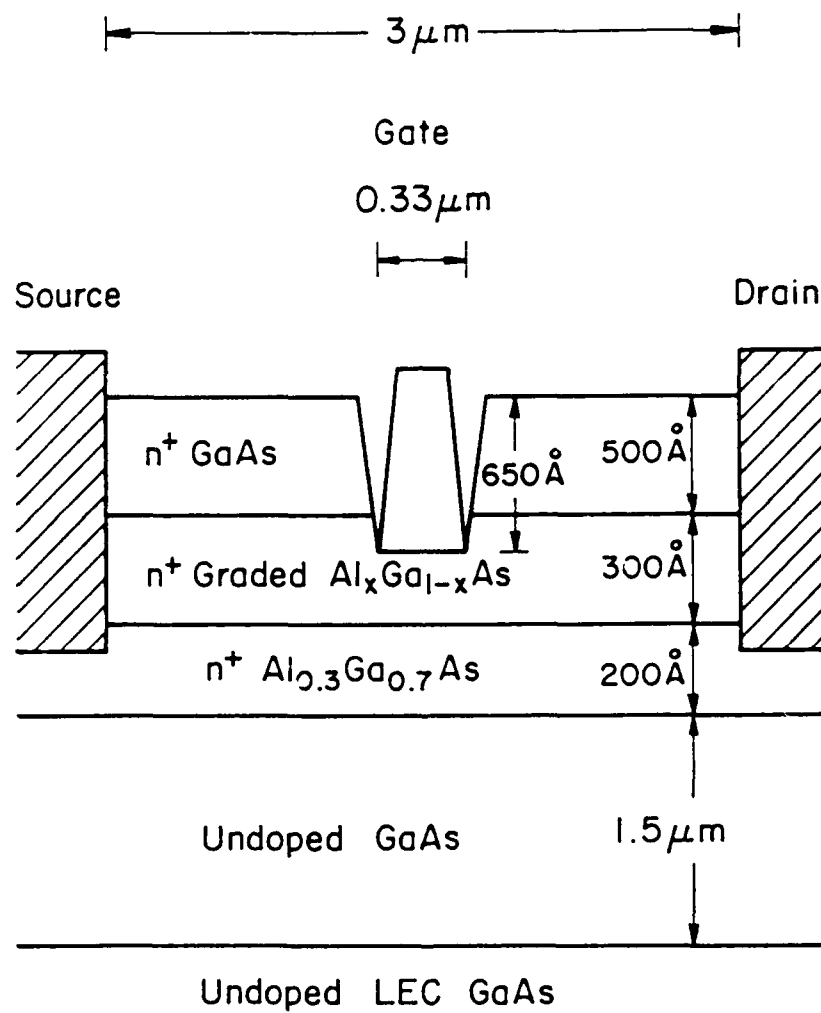


Figure 1. Schematic diagram of QW MODFET # 1250 (from L. Camnitz thesis).

channels grown with 200 Å spacers, yielded 95,000 - 210,000 cm²/V-s mobility at 77 K, depending on the condition of the MBE machine. Values of the electron mobility rises even much higher at much lower temperatures, for the best samples, reaching values of ~ 1,000,000 cm²/V-s. The mobility is 95,000 cm²/V-s for (001) surfaces, and 115,000 cm²/V-s for 4° misorientation toward (111)A, for 75 Å spacer layers. The electron sheet density for this high mobility was 8×10^{11} /cm². This yielded 80 Ω/□ 2DEG sheet resistivity for the (001) wafers, and 65 Ω/□ for the misoriented substrate. When much larger spacers (200 Å) were used, the world-record mobility values of 210,000 cm²/V-s were achievable at 77 K. The electron sheet density, however, was reduced to 3×10^{11} /cm², yielding sheet resistance of 100 Ω/□ at 77 K, which is not optimum. This latter layer should perform best at 12 K, however, with ~ 20 Ω/□ sheet resistance.

The use of Al_{0.3}Ga_{0.7}As and Al_{0.3}Ga_{0.7}As/GaAs superlattices were also studied, for improved output conductance and microwave performance. The best sheet conductances at 77 K were obtained with 150 Å quantum wells, and with 75 Å undoped Al_{0.3}Ga_{0.7}As spacers between the 2DEG and the atomic-planar doped portion of the barrier. Growth was best done at 620°C, and a superlattice of 15 Å of GaAs and 200 Å of Al_{0.3}Ga_{0.7}As yielded the best 2DEG mobility with confinement under the channel.

Using pseudomorphic In_yGa_{1-y}As channels, values of $y = .15$ and $.25$ were optimized. The sheet resistivity of these 2DEG's in the pseudomorphic In_yGa_{1-y}As channels, were worse than those in GaAs channels. At $y = .15$, with 75 Å spacer layer and atomic-planar-doping, the lowest sheet resistance at 77 K was 111 Ω/□. For $y = .25$, with 75 Å spacer, 182 Ω/□ was achieved, both with atomic planar doping.

These materials studies results were obtained by D. Radulescu, and are published in his Ph.D. thesis.

MODFET Fabrication and Testing

The MODFET shown in Figure 1 was processed using electron beam lithography with single-layer PMMA resist. The gate length is $.35\text{ }\mu\text{m}$, and the gate width is $300\text{ }\mu\text{m}$. The noise temperature was measured at 12.5 K physical temperature, as shown in Fig. 2. 10.5 K minimum noise temperature was obtained at 8.3 GHz at 2 ma, with about 10 dB associated gain. The noise temperature of a MESFET fabricated the same way was about twice as high as this quantum well MODFET result.

In spite of this short effort being an early, simple approach to Cryogenic MODFET's, the results were very encouraging, being twice as good as MESFET's. With optimized mushroom gate, device size and layout, the results were expected to become twice as good again. The Cornell technology was shared with GE, who had a contract to develop cryogenic ultra-low-noise MODFET's for NASA's earth receiver array to receive the Neptune probe data. GE ultimately obtained 5.5 K noise temperature at 12 K real sample temperature, at 8.3 GHz.¹

SUMMARY AND CONCLUSION

It was determined that MODFET channel's with single-sided doping, for 77 K operation, are optimum if they are made of GaAs (with no Indium). For short gates ($\ll .5\text{ }\mu\text{m}$), a barrier layer of superlattice $\text{Al}_{.3}\text{Ga}_{.7}\text{As}$ (200 Å), GaAs (15 Å) was best, grown by MBE at 620°C. The optimum quantum well was 150 Å, and the doping in the top $\text{Al}_{.3}\text{Ga}_{.7}\text{As}$ barrier is best done with a spacer

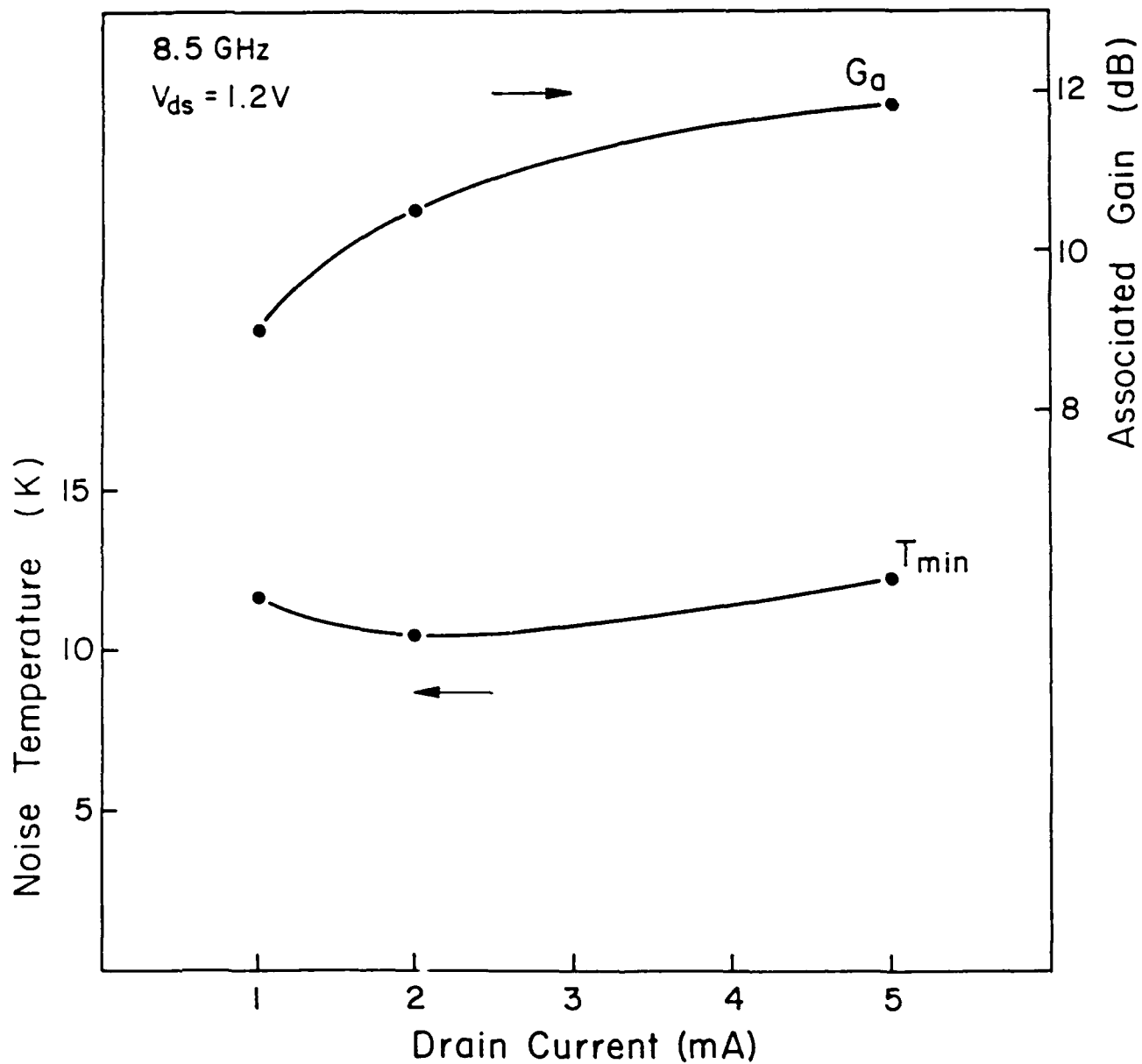


Figure 2. Bias Dependence to T_{min} and g_a for 0.35 μm E-mode QW MODFET #1250 at 12.5 K physical temperature. (from L. Camnitz thesis)

layer of 75 Å, and with the Si doping all placed in single atomic-planar doping at that location. The lowest 77 K 2DEG sheet resistance was 80 Ω for (001) substrate orientation and 65 Ω for a misorientation of 4° off (001) toward (111)A direction. The former has 95,000 cm²/V-s mobility and 8 × 10¹¹/cm² electron sheet density, while the latter has 20% higher electron mobility. For 12 K operation, a 200 Å spacer yields the best 2DEG sheet resistance of 20 Ω/□, with ~ 1 × 10⁶ cm²/V-s electron mobility, but with only 3 × 10¹¹/cm² electron sheet density.

It was determined that pseudomorphic In_yGa_{1-y}As channels for 2DEG yielded higher electron sheet density, but with substantially lower mobility, so that the 2DEG sheet resistivity monotonically rises with increased fraction y. At 25% Indium, the lowest sheet resistivity was 150 Ω/□. This effect is expected to continue to yield inferior performance for pseudomorphic MODFET's, compared to lattice matched GaAs MODFET's, at even lower temperatures than 77 K.

When MODFET's were fabricated at Cornell using GaAs quantum well channels (130 Å thick), with .35 μm gate length, a noise temperature of 10.5 K was obtained at 12 K physical temperature, at 8.3 GHz. These devices were not yet fully optimized since they used Al_{0.3}Ga_{0.7}As barriers under the channel, rather than superlattices, and were not yet optimized for the doping profile, nor did they yet have the low-resistance, mushroom-shaped cross section in the gate.

It is recommended that further optimization of the doping profile, to include doping under the channel, and further optimization of the 2DEG confinement, with acceptor atomic-planar-doping deeper in the superlattice buffer layer. Depending on the cryogenic temperature of choice (the spacer

layer can be enlarged for lower temperature operation), optimized designs can now be undertaken.

It is not understood why the optimum mobility is sharply lower in $\text{In}_y\text{Ga}_{1-y}\text{As}/\text{GaAs}$ pseudomorphic quantum wells at cryogenic temperatures. It is thus of interest to determine what physical (or technological) effect is causing this reduced performance, as compared to GaAs channels.

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DC AND RF CHARACTERIZATION OF A PLANAR-DOPED DOUBLE HETEROJUNCTION MODFET

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Abstract. A GaAs/AlGaAs double heterojunction MODFET structure with atomic planar doping layers prepared by Molecular Beam Epitaxy (MBE) was fabricated and characterized. FET structures of $0.5 \times 200 \mu\text{m}$ gate geometry demonstrated a DC transconductance of 135 mS/mm over a broad gate bias range and a zero gate bias current of 350 mA/mm with a maximum channel current of 430 mA/mm . Both are extrinsic values measured at room temperature. Results obtained from microwave measurements show the cut-off frequency of short circuit current gain (f_T) of 24 GHz , and the maximum oscillation frequency of 50 GHz been achieved. At 10 GHz , the device gave the maximum efficiency of 47 percent with 5.5 dB gain and 0.5 W/mm output power at a drain bias of 6.5 volts .

Introduction

Gallium arsenide MODFETs (Modulation-Doped Field-Effect Transistors) have demonstrated excellent microwave performance with very high cut-off frequency and very good noise performance [Camnitz 1984; Chao 1985; Berenz 1984; Smith 1985]. However, the current driving capability of conventional single heterojunction MODFETs is limited by the amount of sheet charge density in the two dimensional channel, usually less than $1 \times 10^{12}/\text{cm}^2$. Therefore, their power performance and switching speed, which are directly related to the current driving capability, were not much better than MESFETs. In order to achieve high sheet charge density, a high doping concentration in AlGaAs is generally used. This leads to problems such as low breakdown voltage, low activation efficiency of dopants, and process control problems such as poor pinch-off characteristics and threshold voltage uniformity. Double and multiple heterojunction devices were then investigated [Hikosaka 1986; Gupta 1985; Saunier 1986] to increase the current density. The highest maximum channel current reported so far is 600 mA/mm from a multiple heterojunction device [Saunier 1986]. However, all multiple heterojunction structures built so far, were still based on uniformly doped AlGaAs layers to support the two dimensional electron gases. So the problems with heavily doped AlGaAs layers still persist.

In 1979, Wood [1979] reported a GaAs power FET structure of which the dopants were deposited on one atomic plane by interrupting MBE growth. The ultra-thin doped layer resulted in a FET structure with very constant transconductance and gate-to-source capacitance over a wide bias range. We present here a double heterojunction MODFET structure which utilizes two Si planar-doped AlGaAs layers. This provides us with good charge control of the two-dimensional electron sheet charge density in comparison to the uniformly doped layers as well as better device performances. From those double planar-doped MODFET structures, we observed enhanced FET performance such as higher breakdown voltage, broader g_m and gate capacitance curves, reduced light sensitivity and threshold voltage shifts at low temperature.

Device Structure

The fabricated AlGaAs/GaAs structure is shown in Fig. 1, and the corresponding energy band diagram under the gate is shown in Fig. 2. Since the donor atoms are confined in a two-dimensional plane, the band bending is linear and resulting in broad g_m and C_{gs} characteristics. The structure is grown by MBE on top of a semi-insulating GaAs substrate in the following sequence: 5000 Å superlattice buffer layer, 200 Å undoped AlGaAs, Si planar doped layer of $4 \times 10^{12}/\text{cm}^2$, 100 Å undoped AlGaAs, 200 Å undoped GaAs channel, 50 Å undoped AlGaAs spacer layer, Si planar doped layer of $4 \times 10^{12}/\text{cm}^2$, 400 Å undoped AlGaAs, and 400 Å GaAs capping layer doped to $1 \times 10^{18}/\text{cm}^3$. The mole fraction of aluminum is 30% throughout all the AlGaAs layers.

Device Fabrication

The double heterojunction MODFETs were fabricated by using a deep-UV contact lithography and a lift-off technique. After mesa etching, source and drain ohmic contacts were formed with Ni/AuGe/Ag/Au alloyed at 750 C furnace temperature on the cap layer. Using the photoresist as mask, the gate recess was performed by wet chemical etching. Finally, Ti/Pt/Au gate metal was evaporated and lift-off to form complete FET structure. The gate length of FETs is either 1 μm or 0.5 μm measured on the mask with distance of 1.5 μm between gate and source and gate to drain.

Results and Discussion

Minimum breakdown voltage measured between two adjacent mesa pads placed 7 μm away on the superlattice buffer layers was 40 volts. Specific ohmic contact resistance obtained from transmission line patterns was typically 0.4 ohms-mm. Since a phosphoric acid/peroxide/DI aqueous solution was used for gate recess etching, it left residues underneath the Schottky gate metal and caused variations in gate breakdown voltages ranged from 3.5 to 19 volts as shown in Figs. 3 and 4. Despite this processing related problem, we demonstrated that the high gate breakdown voltages of 19 volts can be

400 Å n ⁺ - GaAs Si:1E18/cm ³
400 Å undoped Al _{0.3} Ga _{0.7} As
ATOMIC PLANAR DOPING Si:4E12/cm ²
50 Å undoped Al _{0.3} Ga _{0.7} As
200 Å GaAs QUANTUM WELL
100 Å undoped Al _{0.3} Ga _{0.7} As
ATOMIC PLANAR DOPING Si:4E12/cm ²
200 Å undoped Al _{0.3} Ga _{0.7} As
5,000 Å Superlattice Buffer: (15 Å GaAs/200 Å Al _{0.3} Ga _{0.7} As)
3.1 GaAs

Figure 1. Layer structure of an atomic planar doped double heterojunction MODFET.

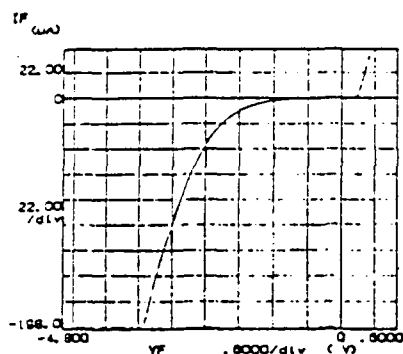


Figure 4. Breakdown characteristics of a bad Schottky diode.

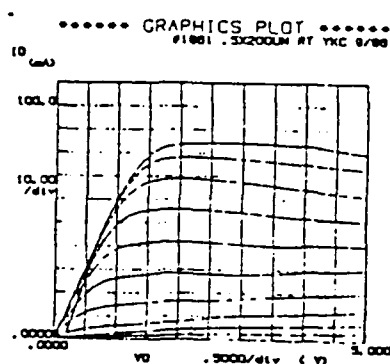


Figure 5. Drain current-voltage characteristics for a 0.5 x 200 μm MODFET.

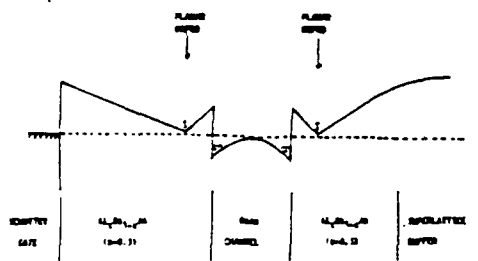


Figure 2. Band diagram of the APD double heterojunction MODFET.

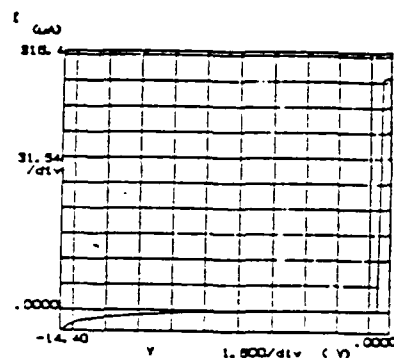


Figure 3. Breakdown characteristics of a good Schottky diode.

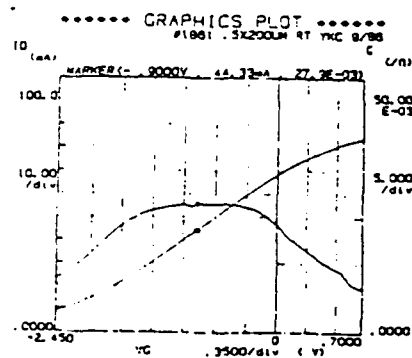


Figure 6. g_m , I_{DS} characteristics versus gate bias variation.

accomplished by the planar doping technique.

Figure 5 shows the drain current-voltage characteristics of a $0.5 \times 200 \mu\text{m}$ FET at room temperature. It shows very good pinch-off characteristics as well as very low output conductance. The relation of DC transconductance and drain current versus gate bias were plotted in Fig. 6 with drain biased at 2.5 volts. A very broad peak of transconductance over the bias variations was observed. By combining the flat gate-to-source capacitance curve in Fig. 7, this double planar doped technique will yield MODFETs with very good RF power performance in terms of high f_{max} , high efficiency, low intermodulation distortion, and fairly constant input impedance at different power levels. The maximum extrinsic g_m measured at room temperature is 139.5 mS/mm with a source resistance of 1.6 ohms-mm from the end-resistance measurement. This yields an intrinsic g_m of 179 mS/mm. Fig. 8 shows the drain I-V characteristics of a $1 \times 200 \mu\text{m}$ FET at 77K under the light and in the dark. Despite the oscillations from the probe station, we can see very little I-V collapse which is very pronounced and commonly seen in MODFETs with uniformly-doped AlGaAs layers. This can be seen better in the 77K transconductance and drain current curve as depicted in Fig. 9.

Data obtained from small signal s-parameter measurements from 1 to 19 GHz of a packaged FET with $0.5 \times 200 \mu\text{m}$ gate geometry shows a short-circuit current gain cut-off frequency (f_T) of 24 GHz with an associated maximum oscillation frequency (f_{max}) of 50 GHz. The data were extrapolated from the low frequency measurements with a slope of 6 dB per octave. Power measurements were performed at 10 GHz with the diced device mounted and wire-bonded in a microwave fixture. At a maximum efficiency of 47 percent, the tuned device delivered a corresponding power of 0.5 W/mm and 5.5 dB gain with the drain biased at 6.5 volts. The device also exhibited a soft output power compression curve as shown in Fig. 10, hence it was difficult to determine the 1 dB compression point. At low power level, the tuned device gave 12.4 dB gain. The maximum output power can be delivered by this device could not be measured on our test system which is limited by the low available input power level from the signal source.

Summary

We have demonstrated a double heterojunction MODFET structure that utilizes a MBE growth suspension technique to confine all the dopants within a ultra-thin plane in the otherwise unintentionally doped AlGaAs layers. The fabricated FETs with $0.5 \times 200 \mu\text{m}$ gate geometry shows an f_T of 24 GHz and corresponding f_{max} of 50 GHz. The room temperature DC characteristics shows a very broad g_m peak of 135 mS/mm with a maximum channel current of 350 mA/mm. Power measurements on this device at 10 GHz shows a maximum efficiency of 47 percent with 5.5 dB associated gain and 0.5 W/mm. At 77K, the fabricated MODFET showed very little light sensitivity and no

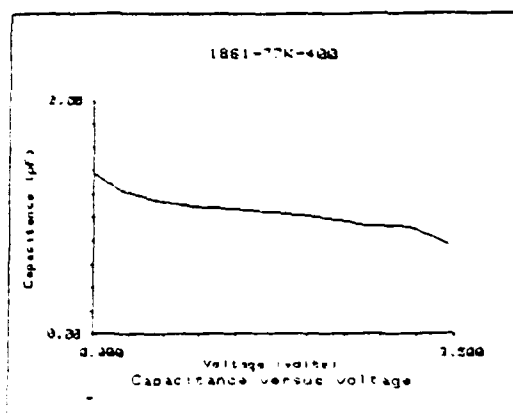


Figure 7. (a) 10MHz C-V characteristics of Schottky Gate Diode at 77°K.

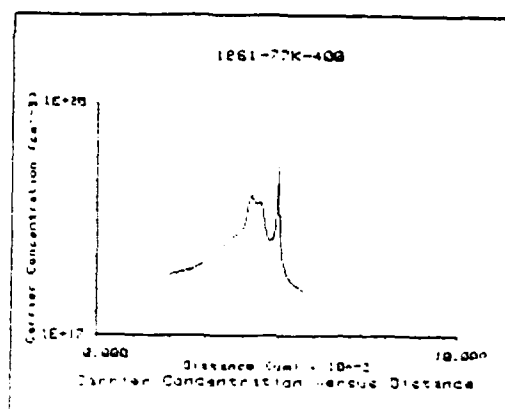


Figure 7. (b) Corresponding carrier concentration at 77°K.

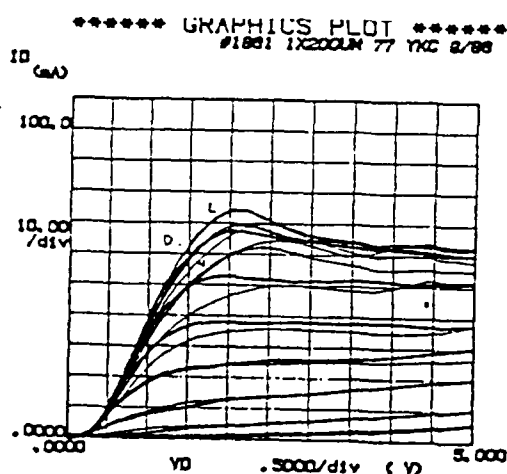


Figure 8. Drain current-voltage characteristics of 1 x 400 μ m FET at 77°K.

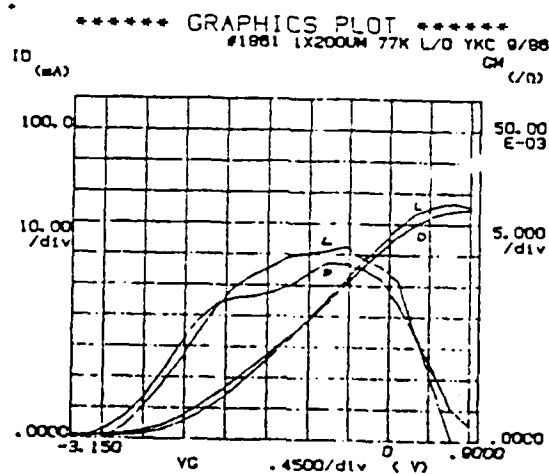


Figure 9. g_m , I_{DS} characteristics at 77°K with/without light.

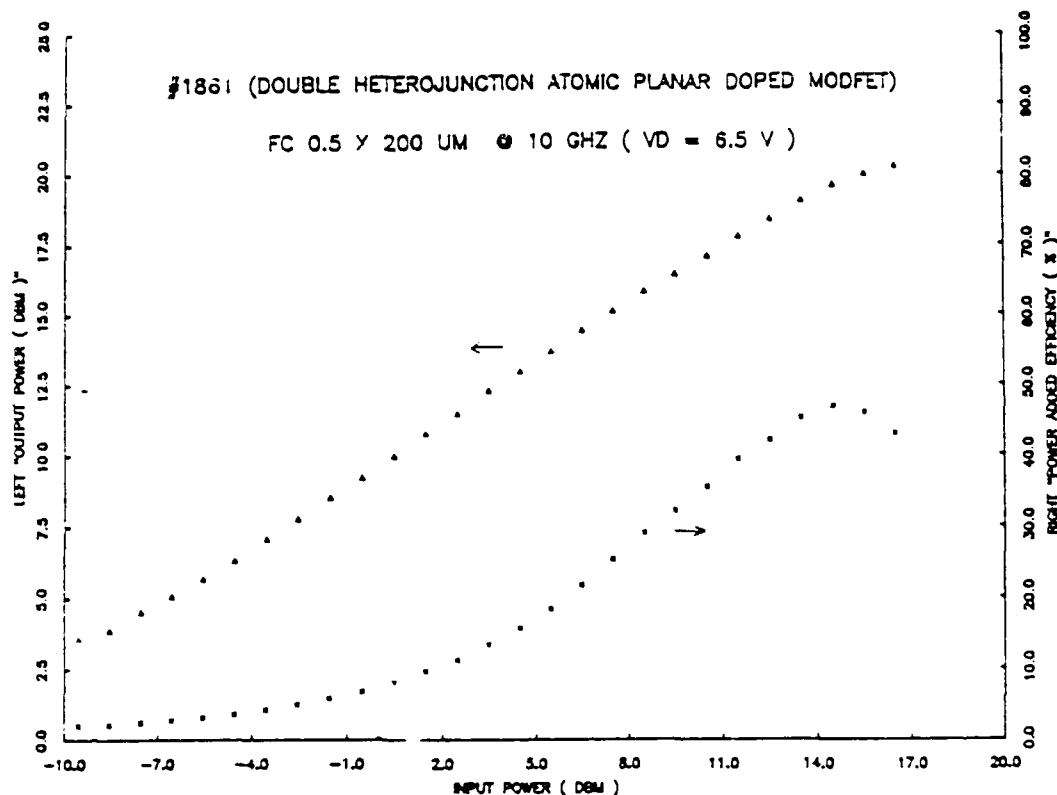


Figure 10. Power Performance of a
0.5 x 200 μm FET at 10 GHz.

I-V collapse was observed. Therefore, the double atomic planar doped structure will be a very good candidate for the high speed digital and high power microwave applications.

Acknowledgements

The authors wish to thank A. Lepore for E-beam mask generation, J. Berry for technical advise, NRFSS and the Electronics Laboratory (General Electric Co., Syracuse, NY) for facility usage. Some 1 μm MODFETs were evaluated at Cascade Corps. (Beaverton, OR) microwave probe station, help from D. Carlton, J. Marron, and K. Jones are deeply appreciated. The work was supported in part by JSEP, ONR, GE and McDonnell-Douglas Co.

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ANISOTROPIC TRANSPORT IN MODULATION DOPED QUANTUM WELL STRUCTURES

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Anisotropic electron transport has been observed in GaAs modulation doped quantum wells grown by molecular beam epitaxy (MBE) on a thick (001) $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer grown at 620°C . The anisotropy is a result of the growth of GaAs on $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ under growth conditions which provide an anisotropic inverted interface morphology. We observe that the degree of anisotropy is related to the thickness and growth parameters of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer grown just prior to the inverted interface. This communication summarizes our observation that the inverted interface has an anisotropic roughness which affects the 77K low-field electron transport parallel to the interface and gives rise to anisotropic electron scattering in the GaAs modulation doped quantum well [1].

The structure used in this study is shown in fig. 1. The epitaxial layers were grown by MBE in a Varian GEN II machine on undoped LEC grown GaAs substrates cut $2^\circ \pm 0.5^\circ$ off the (001) plane towards the (011) plane. The GaAs buffer is followed by a 500 Å graded $\text{Al}_x\text{Ga}_{1-x}\text{As}$ region ($0 < x < 0.3$) to minimize the contributions of an extra 2DEG at this interface in the transport measurements. The substrate temperature during growth was 620°C unless otherwise specified. The growth rate of GaAs and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ was 1.0 and $1.43 \mu\text{m/h}$ respectively for all structures grown in this study. The surface reconstruction determined by electron diffraction during growth of GaAs was an arsenic-stabilized $c(2 \times 8)$ mesh. The V/III beam equivalent pressure ratio determined by an ion gauge in the growth position was be-

tween 7 and 10. The same arsenic flux was used for both the GaAs and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ growth.

Fig. 2 shows the 77 K Van der Pauw-Hall mobility [2] measured in the dark as a function of quantum well width, L_z , for structures with both thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ and superlattice buffers. The data point at $L_z = \infty$ is obtained using GaAs only in the buffer layer. A monotonic decrease in mobility is observed with decreasing quantum well thickness using the thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer. Using the superlattice buffer, the mobilities remain constant above $95,000 \text{ cm}^2/\text{V}\cdot\text{s}$ for well widths of 150 Å or more.

In fig. 3 we plot the ratio $\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$ at 77 K versus the quantum well width for the structures

$n^+ - \text{GaAs}$	
$n^+ - \text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$	
$\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ Spacer	
L_z	GaAs Quantum Well
5000 Å Buffer	1) Thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ or
	2) Superlattice (15 Å GaAs / 200 Å $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$)
500 Å	graded $\text{Al}_x\text{Ga}_{1-x}\text{As}$
3000 Å	GaAs
(001) GaAs Substrate	

Fig. 1. Layer structure of modulation doped quantum wells.

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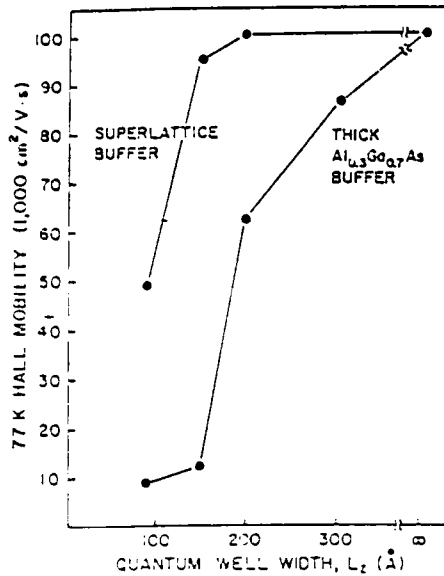


Fig. 2. 77 K Hall mobility as a function of quantum well width, L_z , for both thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ and superlattice buffered structures.

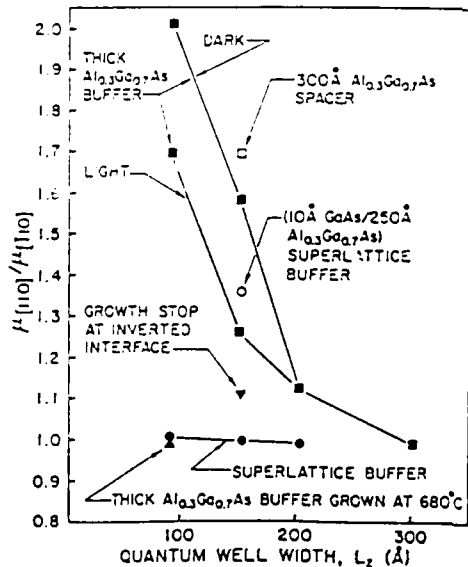


Fig. 3. The ratio of $\mu_{[110]}$ to $\mu_{[110]}$ as a function of quantum well width.

in fig. 2. This ratio is essentially unity for all well widths when a superlattice buffer (15 $\text{\AA}$ $\text{GaAs}/200 \text{\AA}$ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$) is used. For the thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffered structures the 77 K low field electron transport is observed to be anisotropic. As the well width is increased the anisotropy gets progressively smaller, and vanishes in the 300 $\text{\AA}$ quantum well. The effect of light is to reduce the degree of anisotropy by increasing the 2DEG sheet density (Fermi energy). Also shown in fig. 3 is a 90 $\text{\AA}$ quantum well structure with a thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer grown at a substrate temperature of 680°C instead of 620°C . The anisotropy is eliminated for this structure indicating that the temperature of growth of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer plays a role in determining the degree of anisotropy. The effect of a 300 s growth stop at the interface between a $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer and a 150 $\text{\AA}$ quantum well is to reduce the degree of anisotropy as shown in fig. 3. Also shown in fig. 3 is the mobility ratio for a 150 $\text{\AA}$ quantum well with a superlattice buffer (15 $\text{\AA}$ $\text{GaAs}/200 \text{\AA}$ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$) with a 300 $\text{\AA}$ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ spacer inserted between the superlattice buffer and the quantum well. The data indicates that the thickness of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ grown just prior to the inverted interface plays a role in determining the degree of anisotropy. Also shown in fig. 3 is the mobility ratio of a 150 $\text{\AA}$ quantum well with a superlattice consisting of 10 $\text{\AA}$ of GaAs and 250 $\text{\AA}$ of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$. The data indicates that the structure of the superlattice plays a role in determining the degree of anisotropy.

In conclusion, anisotropic low field electron transport has been observed in modulation doped GaAs single quantum wells at 77 K. It is a result of the growth of GaAs on $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ under growth conditions which provide an anisotropic interface morphology. The maximum conductivity is along $[110]$ and the minimum is along $[1\bar{1}0]$. The anisotropic effects are relaxed by interrupting MBE growth at the inverted interface. The effects are also reduced by growth of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer at high temperature (680°C). Replacing the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer with a superlattice consisting of 15 $\text{\AA}$ of GaAs and 200 $\text{\AA}$ of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ eliminates the anisotropy. Higher 2DEG sheet concentrations result in reduced amounts of aniso-

tropic transport. Thicker quantum wells also show reduced amounts of anisotropic transport. Employing a superlattice buffer at low growth temperature eliminates anisotropic transport and gives mobilities comparable to conventional non-inverted single heterointerface modulation doped structures for $L_z \geq 150 \text{ \AA}$. The 2DEG mobility is reduced in all cases when the quantum well width is less than $150 \text{ \AA}$.

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Anisotropic transport in modulation-doped quantum-well structures

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Anisotropic electron transport has been observed in GaAs modulation-doped quantum wells grown by molecular-beam epitaxy on a thick (001) $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer grown at 620 °C. The low-field electron mobility at 77 K in the [110] direction is a factor of 2 larger than the mobility in the $[\bar{1}\bar{1}0]$ direction for a 90-Å quantum well. Thicker quantum wells (150, 200, and 300 Å) show progressively less anisotropy, which vanishes for a 300-Å quantum well. The degree of anisotropy is also reduced or eliminated by suspending growth of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ for a period of 300 s prior to growing the GaAs quantum well. Growing the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer at higher temperatures (680 °C) also reduces the degree of anisotropy. Higher two-dimensional electron gas sheet densities result in less anisotropy. The anisotropy is eliminated by replacing the thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer with a periodic multilayer structure comprising 15 Å of GaAs and 200 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$. The degree of anisotropy is related to the thickness and growth parameters of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer grown just prior to the growth of the GaAs quantum well.

I. INTRODUCTION

Structures grown by molecular-beam epitaxy (MBE) with GaAs on AlGaAs (inverted interface) are known to differ from structures grown with AlGaAs on GaAs (normal interface).¹⁻¹² Poor structural, electronic, and optical properties have been associated with the inverted interface.¹⁻¹² The influence of growth conditions on these properties have been investigated by many authors.¹⁻¹² Parameters such as substrate misorientation from nominal (001), growth temperature, growth interruptions, III/V flux ratios, arsenic species (As_4/As_2), and surface impurity concentrations resulting from out-diffusion from the substrate, dopant fluxes, dopant surface segregation, and MBE machine contamination are all factors that determine heterointerface quality. Roughness and impurity trapping at the inverted heterointerface have been suggested as the contributing factors to the inferior structures.¹⁻¹² This paper discusses our observation that the inverted interface has an anisotropic roughness which affects the 77-K low-field electron transport parallel to the interface.

II. EXPERIMENT

The epitaxial layers were grown by MBE in a Varian GEN II machine on undoped liquid encapsulated Czochralski (LEC) grown GaAs substrates cut $2^\circ \pm 0.5^\circ$ off the (001) plane towards the (011) plane. The substrate temperature during growth was 620 °C unless otherwise specified. The growth rate of GaAs and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ was 1.0 and 1.43 $\mu\text{m}/\text{h}$, respectively, for all structures grown in this study. The surface reconstruction determined by electron diffraction during growth of GaAs was an arsenic-stabilized $C(2 \times 8)$ mesh. The V/III beam equivalent pressure ratio determined by an ion gauge in the growth position was between 7 and 10. The same arsenic flux was used for both the GaAs and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ growth.

The structure used in this study is shown in Fig. 1(a). The GaAs buffer is followed by a 500-Å graded $\text{Al}_x\text{Ga}_{1-x}\text{As}$ region ($0 < x < 0.3$) to minimize the contributions of an extra two-dimensional electron gas (2DEG) at

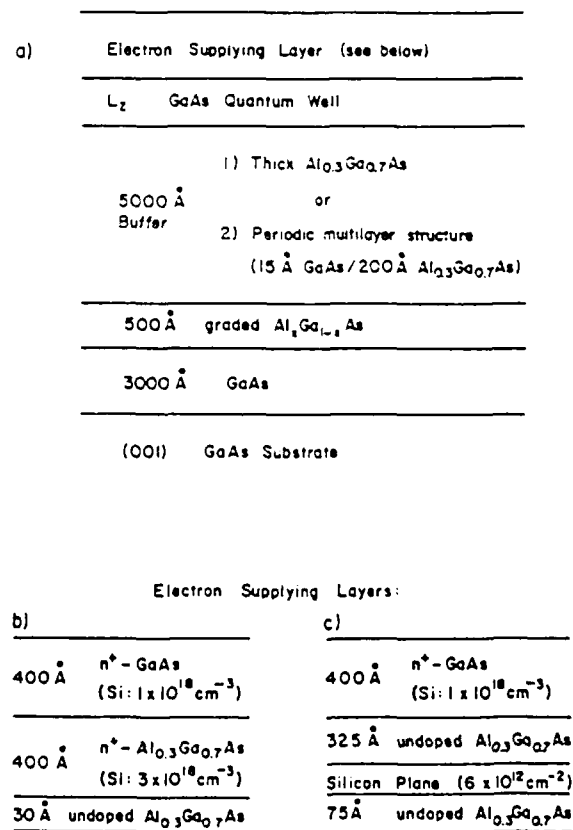


FIG. 1. (a) Layer structure of modulation-doped quantum wells. (b) Layer structure of uniformly doped electron supplying layer. (c) Layer structure of atomically planar doped electron supplying layer.

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this interface in the transport measurements. The periodic multilayer is hereafter referred to as a superlattice buffer. The two types of electron supplying layers used are outlined in Figs. 1(b) and 1(c). A 30-Å spacer was used in the case of uniform doping [Fig. 1(b)]. For the atomic planar doping case [Fig. 1(c)] a 75-Å spacer was required to give 2DEG mobilities and sheet densities equivalent to the uniformly doped structures. During silicon deposition for atomic planar doping, growth was suspended for 45 s with only silicon and arsenic impinging on the substrate to accumulate 6×10^{12} silicon atoms per square centimeter.

Table I summarizes the structural parameters of the layers presented in this study. Samples B1, B2, B3, and B4 are thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffered structures while SL1, SL2, and SL3 are superlattice buffered. Sample B5 contains a 300 s growth interruption between the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer and the 150-Å quantum well, otherwise it is identical to sample B2. During this growth interruption arsenic was impinging on the substrate. For sample B6, the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer was grown at 680 °C, otherwise it is identical to sample B1. Sample B7 is a replication of sample SL3 without the GaAs in the superlattice buffer. The growth was interrupted for 5.4 s every 200 Å which corresponds to the 15-Å GaAs deposition time. In other words, the buffer of B7 contains no GaAs, just 5000 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$. Sample SL4 is a superlattice buffered (15 Å/200 Å) structure with an extra 300-Å $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer inserted between the last 200 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ of the superlattice buffer and a 150-Å quantum well; otherwise it is identical to sample SL2. Sample SL5 is a 150-Å quantum well with a superlattice buffer comprising 10 Å of GaAs and 250 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$. The only difference between samples SL5 and SL2 is the superlattice structure.

Van der Pauw-Hall measurements were made using cloverleaf patterns and a square active area with edges

aligned along the (110) cleavage directions. These measurements were made in the dark at liquid-nitrogen temperature in a magnetic field of 2 kG. White light was used to vary the 2DEG sheet density. The sheet resistances were determined using transmission line model (TLM) patterns oriented in four nonequivalent crystal directions: [110], [010], $[\bar{1}10]$, and [100].

III. RESULTS

Figure 2 shows the 77-K van der Pauw-Hall mobility¹³ measured in the dark as a function of quantum-well width, L_z , for structures with both thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ (B1, B2, B3, B4) and superlattice buffers (SL1, SL2, SL3). Samples B5, B6, B7, SL4, and SL5, containing variations from the standard structures, are not included in Fig. 2. The data point at $L_z = \infty$ is obtained using GaAs only in the buffer layer. A monotonic decrease in mobility is observed with decreasing quantum-well thickness using the thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer. Using the superlattice buffer, the mobilities remain constant above 95 000 cm^2/Vs for well widths of 150 Å or more.

Figure 3 shows the orientation of contacts on the van der Pauw-Hall samples. The voltage-current ratio along the [110] direction, $R_{[110]} (= V_{CD}/I_{AB})$, is defined as the ratio of the potential difference V_{CD} between contacts *C* and *D* and the current through the opposite contacts *A* and *B*. Similarly, the voltage-current ratio along the $[\bar{1}10]$ direction is $R_{[\bar{1}10]} (= V_{BC}/I_{AD})$. In Fig. 4 we plot the ratio $R_{[\bar{1}10]}/R_{[110]}$ at 77 K versus the quantum-well width for the structures in Fig. 2. The electron sheet densities could be varied between about $7 \times 10^{11} \text{ cm}^{-2}$ and $12 \times 10^{11} \text{ cm}^{-2}$ by controlling the exposure of the layer to white light prior to a measurement. This light effect is caused by the photoexcitation of electrons from DX centers in doped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$.¹⁴ This ratio is essentially unity for all well widths when a superlattice buffer is used. For the thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffered

TABLE I. Structural parameters of modulation-doped quantum wells.

Sample	Type of buffer	Thickness of quantum well (Å)	Type of electron supplying layer ^a	Comment
B1	AlGaAs	90	APD	
B2	AlGaAs	150	UNF	
B3	AlGaAs	200	UNF	
B4	AlGaAs	300	APD	
B5	AlGaAs	150	UNF	300-s growth stop at inverted interface
B6	AlGaAs	90	APD	Buffer grown at 680 °C
B7	AlGaAs	200	APD	5.4-s growth stop every 200 Å in AlGaAs buffer
SL1	SL (15 Å/200 Å)	90	APD	
SL2	SL (15 Å/200 Å)	150	APD	
SL3	SL (15 Å/200 Å)	200	APD	
SL4	SL (15 Å/200 Å) + 300 Å	150	APD	Extra 300 Å undoped AlGaAs layer inserted between superlattice and quantum well
SL5	SL (10 Å/250 Å)	150	APD	

^a APD = Atomic planar doped, UNF = uniformly doped.

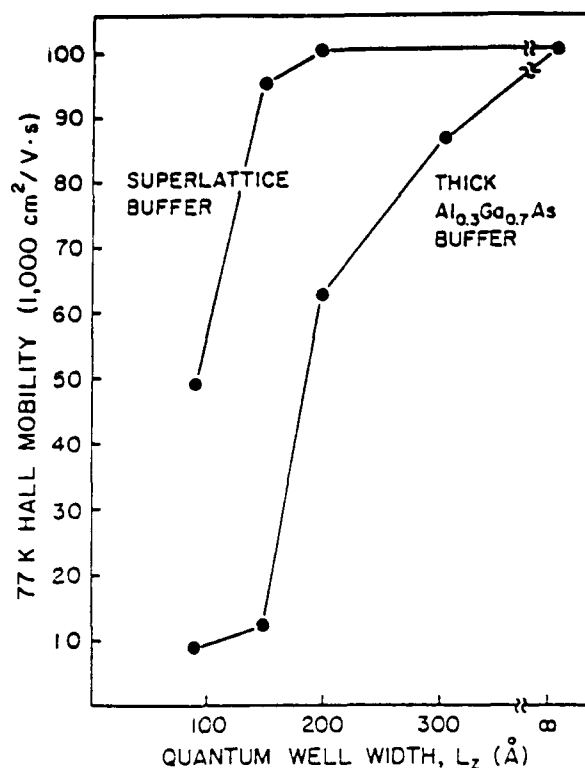


FIG. 2. 77 K Hall mobility as a function of quantum-well width, L_z , for both thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ (B1, B2, B3, B4) and superlattice buffered structures (SL1, SL2, SL3).

structures the 77-K low-field electron transport is observed to be anisotropic. As the well width is increased the anisotropy gets progressively smaller, and vanishes in the 300- $\text{\AA}$ quantum well. The effect of light is to reduce the degree of anisotropy. This effect will be discussed later. Also shown in Fig. 4 is a 90- $\text{\AA}$ quantum-well structure (sample B6) with a thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer grown at a substrate temperature of 680 $^\circ\text{C}$ instead of 620 $^\circ\text{C}$. The anisotropy is eliminated for this structure. The effect of a 300-s growth stop between a $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer and a 150- $\text{\AA}$ quantum well (sample B5) is to reduce the degree of anisotropy as shown in Fig. 4.

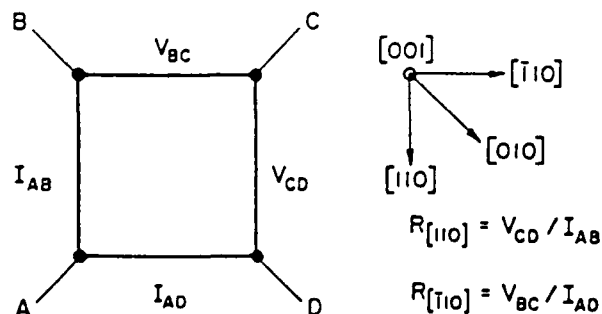


FIG. 3. The orientation of contacts on the van der Pauw-Hall samples. The definitions of $R_{[110]}$, $R_{[\bar{1}10]}$, and the crystal directions are also shown.

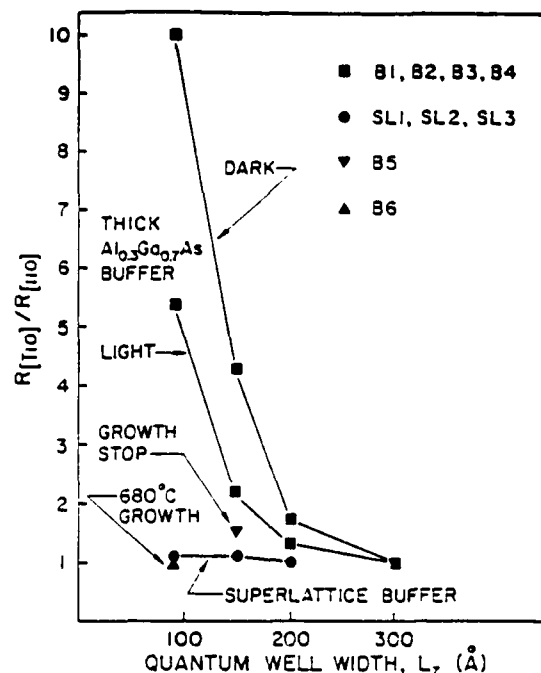


FIG. 4. The ratio of $R_{[110]}$ to $R_{[\bar{1}10]}$ as a function of quantum-well width.

The effect of electron sheet density (varied by light exposure) on the anisotropy is shown in Fig. 5, where the ratio of $R_{[\bar{1}10]}$ to $R_{[110]}$ is plotted versus Hall sheet density. For all structures investigated the degree of anisotropy is reduced as the electron sheet density is increased. Also shown in Fig. 5 are data on sample SL4. The presence of an additional 300 $\text{\AA}$ of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ above the superlattice is sufficient to produce the anisotropy. If the GaAs in the superlattice is too thin compared to the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ (samples SL5 and B7) conduction anisotropy is again observed.

Montgomery¹⁵ has developed a coordinate transformation which can be used to convert the measured ratio of voltage-current in orthogonal directions ($R_{[110]}/R_{[\bar{1}10]}$) to the corresponding mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}10]}$). Figure 6 is a plot of the voltage-current versus mobility anisotropy ratios. The solid curve represents the theoretical calculation from Ref. 15. The solid circles are data on some of the structures which exhibited anisotropic transport properties. The data were obtained after exposure to a large amount of white light which maximizes the 2DEG sheet density and minimizes the anisotropy. Sheet resistances from which mobility ratios were obtained, were measured by the TLM method¹⁶ in four nonequivalent crystal directions: $[110]$, $[010]$, $[\bar{1}10]$, and $[100]$. The maximum mobility was observed in the $[110]$ direction, while the minimum mobility was observed in the $[\bar{1}10]$ direction of all structures. Intermediate mobility values were measured in the $[010]$ and $[100]$ directions. Reversing polarity in the TLM measurements showed no dependence of the mobility on the sign of the applied electric field.

Hornstra *et al.*¹³ have shown that the van der Pauw

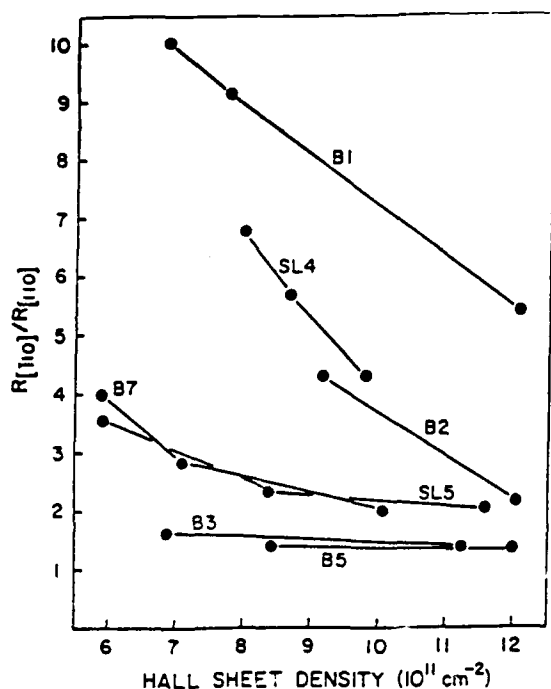


FIG. 5. The ratio of $R_{[110]}$ to $R_{[110]}$ as a function of Hall sheet density. The samples are described in Table I.

technique can be applied to anisotropic conductors. The mobility measured is the geometric mean mobility: $\mu = \sqrt{\mu_{[110]} \mu_{[110]}}$. The van der Pauw measurement gives

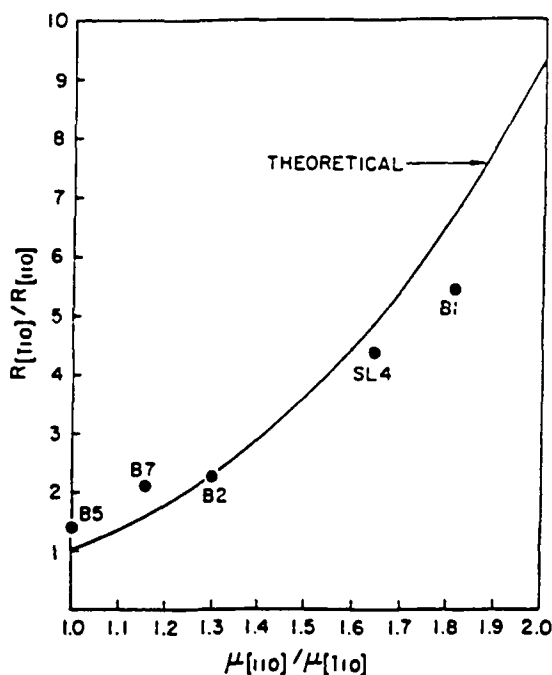


FIG. 6. The ratio of $R_{[110]}$ to $R_{[110]}$ as a function of the ratio of $\mu_{[110]}$ to $\mu_{[110]}$. The solid curve represents the theoretical calculation from Ref. 15. The solid circles represent experimental points. The samples are described in Table I.

the product of the mobilities, while a measurement of $R_{[110]}/R_{[110]}$ gives the quotient of the mobilities. These two measurements can be used to deduce the individual mobilities $\mu_{[110]}$ and $\mu_{[110]}$. For all structures investigated in this study, whenever anisotropic transport is observed, $\mu_{[110]}$ and $\mu_{[110]}$ are lower than 95 000 cm²/V s. Table II summarizes the van der Pauw-Hall measurements of the samples presented in this study.

IV. DISCUSSION

Figures 2 and 4 suggest that the inverted interface (GaAs grown on top of AlGaAs) is anisotropically rough. MBE grown (001) GaAs/AlGaAs structures possess several anisotropic properties where the two $\langle 110 \rangle$ directions are nonequivalent. Even a nominally flat (001) GaAs surface is anisotropic. For an arsenic-stabilized surface the bonds joining an (001) arsenic plane to the underlying plane of gallium atoms are all in the $(\bar{1}10)$ plane.¹⁷ As a result, the two $\langle 110 \rangle$ directions are nonequivalent. Reflection high-energy electron diffraction has been used to deduce that islands on the surface during MBE growth are elongated in the $[\bar{1}10]$ direction.¹⁸ This implies that step propagation is faster in the $[\bar{1}10]$ direction compared to the $[110]$ direction. Photoluminescence in GaAs has been observed to be strongly polarized.¹⁹ The luminescence spectra in the 1.504–1.511 eV region are different for emitted luminescence polarized parallel to the $[110]$ direction compared to that polarized parallel to the $[\bar{1}10]$ direction.¹⁹ Defect pairs preferentially oriented parallel to a $[110]$ direction due to faster step propagation in the $[\bar{1}10]$ direction have been suggested as the cause of the polarized photoluminescence.¹⁹ A step edge propagating in a $[\bar{1}10]$ direction will have an arsenic atom with a single dangling bond at the step edge (arsenic-type) while a step edge propagating in a $[110]$ direction will have a gallium atom with a single dangling bond at the step edge (gallium-type).²⁰ An arsenic-type step edge propagates faster than a gallium-type step edge. As a result, these two-step edges (arsenic-type, gallium-type) are fundamentally different. Tsui *et al.*^{1,21,22} have recently shown that the growth of AlGaAs on a surface with gallium-type step edges results in smooth surface and interface morphology and superior photoluminescence when compared to growth on a surface with arsenic-type step edges.

In this study the substrates were cut $2^\circ \pm 0.5^\circ$ off (001) towards (011). Single monomolecular steps at the inverted interface due to the 2° cut cannot account for the observed anisotropic and degraded mobilities. Had this been the case single heterojunction structures would also be expected to have anisotropic mobilities since monomolecular steps due only to the cut are bound to be present at this interface also.²³ We do not observe any such effects in our single heterojunction structures at 77 K. Other authors^{24–26} have observed anisotropic transport in single heterojunction structures. However, all observations have been made in structures with reduced phonon and remote impurity scattering achieved by using a low measurement temperature (≈ 4 K) and wide undoped AlGaAs spacers, respectively. Lin²⁶ has found no correlation between substrate misorien-

TABLE II. 77 K electron sheet densities, mobilities and voltage-current ratios before and after exposure to white light for the samples in Table I.

Sample	Sheet density ($1 \times 10^{11} \text{ cm}^{-2}$)		Mobility ($1 \times 10^4 \text{ cm}^2/\text{Vs}$)		$\frac{R_{(110)}}{R_{(1\bar{1}0)}}$	
	Dark	Light	Dark	Light	Dark	Light
B1	6.8	12.0	9.0	11.1	10.0	5.4
B2	9.1	12.1	12.2	30.0	4.3	2.2
B3	6.9	11.3	62.5	65.6	1.7	1.4
B4	7.4	12.1	87.1	72.3	1.0	1.0
B5	8.5	12.0	27.5	46.2	1.5	1.4
B6	6.6	11.9	24.1	35.9	1.0	1.0
B7	5.9	10.1	51.4	70.2	4.0	2.1
SL1	6.6	12.4	49.2	64.9	1.0	1.0
SL2	7.9	12.2	95.9	77.3	1.0	1.0
SL3	7.3	11.3	100.5	92.0	1.0	1.0
SL4	7.9	9.8	34.4	49.1	6.3	4.3
SL5	5.9	11.6	45.4	67.6	3.6	2.1

tation from nominal (001) and anisotropic transport at ≈ 4 K.

An inverted interface characterized by roughness on the order of multiple monolayers is a highly possible cause of the anisotropic and degraded mobilities in our structures. Roughness at this interface can be explained using a simple model²⁷ which accounts for the different migration length of aluminum and gallium on the surface of AlGaAs during MBE growth. Using our growth conditions we crudely estimate, according to the model of Ref. 27, the migration length of aluminum and gallium to be 35 and 150 Å, respectively. Since the migration length of aluminum is estimated to be smaller than the migration length of gallium, the inverted interface will be rougher than the normal interface where only the gallium atoms are present. Monte Carlo simulations²⁸ have predicted the inverted interface to get progressively rougher (many monolayers) as the thickness of the AlGaAs layer gets larger if the AlGaAs is grown under typical GaAs growth conditions (620 °C, 1 $\mu\text{m}/\text{h}$, $\text{As}_4/\text{Ga} = 10$). At higher substrate temperature the aluminum atom becomes more mobile and may only nucleate at step edges. The gallium atom is sufficiently mobile to do this at lower temperatures. Following this argument, the GaAs in the superlattice will periodically smooth out the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ growth front if the thickness of GaAs is large enough. This effect has been modeled by Singh *et al.*²⁹ using Monte Carlo simulations and shown to be an effective method of achieving smooth interfaces when the two cations (Al,Ga) of a ternary compound ($\text{Al}_x\text{Ga}_{1-x}\text{As}$) have significantly different migration lengths.

Since the (001) GaAs in this study was cut 2° off towards (011) both gallium-type and arsenic-type step edges will exist on the surface before growth is initiated. The anisotropies inherent in the growth process due to these fundamentally different step edges combined with multiple monolayer interface roughness due to a short aluminum migration length is believed to be the mechanism responsible for the effects observed in this study.

As shown in Fig. 4, we observe a reduction in the degree of anisotropy by inserting a growth stop at the inverted interface (sample B5). A growth stop at the inverted interface would reduce the roughness to single atomic steps where anisotropic transport becomes small. We do observe a reduction in the anisotropy due to a growth interruption but we also observe degraded mobilities. This could be related to impurity absorption at the interface and would be a function of MBE machine purity. Other authors^{3,30} have observed increased impurity incorporation while achieving smoother interfaces by interrupting MBE growth.

As shown in Fig. 4, growth of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer at 680 °C (sample B6) eliminates the observed anisotropy in electron transport at 77 K. This is consistent with the model that the inverted interface has a roughness of several monolayers due to a short aluminum migration length. Increasing the growth temperature increases the aluminum migration length.

Table II and Fig. 5 indicate that for structures with anisotropic transport, the 2DEG mobility increases with increasing sheet density. Theoretically,²⁶ as the 2DEG sheet density increases, the 2DEG mobility should decrease due to interface roughness scattering. The fact that we do not observe this may be an indication that more dominant scattering mechanisms³¹ are limiting the mobility or that the model of Ref. 26 is inadequate to explain the inverted interface roughness.³²

Throughout this paper our analysis ignores the effect of parallel electron transport through the electron supplying layer. Isotropic parallel conduction through the electron supply layer will result in an apparently lower anisotropic Hall mobility ratio. Parallel conduction is significant when the electron supplying layer concentration-mobility product is comparable to that of the 2DEG. There is one case in our structures where we believe this is significant. Sample B2 with a uniformly doped electron supplying layer, has slightly less anisotropy than sample SL4 which has an atomically planar doped layer. While the added 300 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$

before the GaAs quantum well is expected to roughen the interface slightly we do not expect it to be as rough as the thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer of sample B2. The higher apparent 2DEG sheet concentration in sample B2 indicates that significant isotropic parallel conduction may be occurring in the electron supplying layer of sample B2.

V. CONCLUSIONS

Anisotropic low-field electron transport has been observed in modulation-doped GaAs single quantum wells at 77 K. It is a result of the growth of GaAs on $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ under growth conditions which provide an anisotropic interface morphology. The maximum conductivity is along $[110]$ and the minimum is along $[\bar{1}10]$. The anisotropic effects are relaxed by interrupting MBE growth at the inverted interface. The effects are also reduced by growth of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer at high temperature (680 °C). Replacing the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ buffer with a superlattice comprising of 15 Å of GaAs and 200 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ eliminates the anisotropy. Higher 2DEG sheet concentrations result in reduced amounts of anisotropic transport. Thicker quantum wells also show reduced amounts of anisotropic transport because the interface roughness represents a smaller portion of the well. Employing a superlattice buffer at low growth temperature eliminates anisotropic transport and gives mobilities comparable to conventional noninverted single heterointerface modulation-doped structures for $L_z > 150$ Å. The 2DEG mobility is reduced in all cases when the quantum-well width is less than 150 Å.

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DC AND MICROWAVE PERFORMANCE OF SINGLE-GATE AND DUAL-GATE

AlGaAs/InGaAs DOUBLE-HETEROJUNCTION MODFET'S

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Single-gate Modulation-Doped Field-Effect Transistors (SG-MODFET) have demonstrated excellent microwave performance with lower noise, higher output power, and much higher cut-off frequency compared to the GaAs MESFETs of the same gate geometry [1-3]. However, there is another attractive and widely-utilized version of the FET, the Dual-Gate MODFET (DG-MODFET) which has not yet been studied extensively. Dual-gate FET's play an important role in a vast variety of high performance microwave circuits such as variable gain stages for both low noise and power amplification [4], active phase shifters [5], mixers [6], etc. The advantages of the dual gate structure comes with the increased functionalities by fabricating two independent FETs of identical characteristics in a compact manner, and higher power gain than the single gate structure. Detailed operating modes and analysis of GaAs dual-gate MESFETs have been studied in many journals [7-9].

We had grown and fabricated both single-gate and dual-gate Modulation-doped AlGaAs/InGaAs/GaAs Double-Heterojunction FETs with 0.7-micron gate length. The layered structures were grown by Molecular Beam Epitaxy (MBE) and utilized atomically planar-doped electron supplying layers [10,11]. The extrinsic DC transconductance from a fabricated single-gate FET is 270 mS/mm at room temperature, and increased to 322 mS/mm at 77K. The extrinsic DC transconductance of a nearby dual-gate FET is 285 mS/mm at room temperature, and increased to 396 mS/mm at 77K. A unity current-gain cut-off frequency (f_T) of 27 GHz and f_{max} of 50 GHz were obtained from the measured S-parameter data from 0.5 to 26.5 GHz of a single-gate FET. Different power-gain roll-off characteristics between SG-MODFETs and DG-MODFETs are observed at high frequency and will be discussed.

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BIAS-DEPENDENT MICROWAVE CHARACTERISTICS OF AN ATOMIC PLANAR-DOPED AlGaAs/InGaAs/GaAs DOUBLE HETEROJUNCTION MODFET

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ABSTRACT

A double heterojunction MODFET (Modulation-Doped Field Effect Transistor) employing lattice-strained AlGaAs/InGaAs/GaAs layer structure has been grown and evaluated at microwave frequencies. Fabricated FETs of $1 \times 200 \mu\text{m}$ gate geometry have demonstrated a room temperature extrinsic DC transconductance of 400 mS/mm with a full channel current of 610 mA/mm . Data extrapolated from small signal S-parameters shows a very high unity power gain cut-off frequency (f_{max}) of 85 GHz as well as a high current-gain cut-off frequency of 21.7 GHz . This is the highest f_{max} obtained yet for a FET with one-micron gate length. Bias-dependent equivalent circuit models are also presented and discussed.

INTRODUCTION

Gallium arsenide MODFETs (Modulation-Doped Field-effect Transistors) have demonstrated excellent microwave performance with very high cut-off frequency and very good low-noise performance [1-3]. However, the current driving capability of conventional single heterojunction MODFETs is limited by their sheet charge density of less than $1 \times 10^{12}/\text{cm}^2$; therefore their power performance and switching speed, which are directly related to current driving capability, were not much better than the MESFETs. Double or multiple heterojunction devices [4-6] were then investigated to increase the current density. So far, the highest maximum channel current reported is 600 mA/mm from six-fold GaAs/AlGaAs heterojunctions [4] and 430 mA/mm from strained-layer InGaAs/AlGaAs double heterojunctions [7]. However, all multiple heterojunction devices have relied on uniformly doped AlGaAs layers to supply the two dimensional electron gases. In order to achieve high sheet charge density, a high doping was introduced. That leads to problems such as low breakdown voltage, low activation efficiency of dopants, and processing problems which results in poor pinch-off characteristics and poor control of uniformity on threshold voltages.

We have reported double heterojunction MODFET structures [8] which utilize two silicon atomic planar-doped AlGaAs layers. By using the Mott barrier gate structure, it provides us with good charge control of the density of two-dimensional electron gases as well as maintaining good breakdown behavior. The threshold voltage of the FET is also less sensitive to the AlGaAs layer thickness across the wafer because the electrical field is constant in the undoped AlGaAs supply layer. Little light sensitivity were observed at low temperature (77K) due to the much reduced volume of heavily doped AlGaAs layers. In this paper, we report the fabrication and characterization of a lattice-strained AlGaAs/InGaAs/GaAs double hetero-junction MODFET of high two-dimensional electron sheet charge density and excellent charge confinement for high frequency applications.

DEVICE STRUCTURE AND FABRICATION

The structure is grown by MBE on top of a semi-insulating GaAs substrate with a few degrees of misorientation from (100) [9] in the following sequence: $5000 \text{ \AA}$ of superlattice buffer layer [10], $50 \text{ \AA}$ undoped GaAs, Si planar doped layer with density of $2 \times 10^{12} \text{ cm}^{-2}$, $85 \text{ \AA}$ undoped GaAs, $200 \text{ \AA}$ undoped InGaAs channel, $30 \text{ \AA}$ undoped AlGaAs spacer layer, Si planar doped layer of $6 \times 10^{12} \text{ cm}^{-2}$, $250 \text{ \AA}$ undoped AlGaAs, and $400 \text{ \AA}$ GaAs capping layer doped to $1 \times 10^{18} \text{ cm}^{-3}$. The mole fraction of aluminum and indium are 15% and 30% respectively.

The grown wafers were then fabricated with a conventional FET process: mesa etch, Ni/AuGe/Pd/Au patterning and lift-off, ohmic contacts formed by alloying at 450°C for 5 seconds, followed by the gate level lithography on a mid-UV contact aligner, recess etch of the capping layer, and evaporation of Ti/Pd/Au and lift-off. Palladium is used in the ohmic metal formation to improve the reliability of the alloyed contacts. A specific contact resistivity of 0.1 ohm-mm were obtained from transmission line measurements.

DC CHARACTERISTICS

Figure 1 shows the room temperature I-V characteristics of a fabricated FET with a $1 \times 100 \mu\text{m}$ gate dimension. The peak extrinsic DC transconductance is 400 mS/mm at room temperature and the dependence of the gate bias is shown in Fig. 2. Maximum channel current is 610 mA/mm at room temperature, and it is decreased to 560 mA/mm at 77K due to the reduction of parallel conducting current in AlGaAs layer. Figure 3 shows the conduction band diagram of the quantum well structure, and the threshold voltage can be derived by solving Poisson equation using the depletion approximation:

$$V_T = \phi_B - [qN_{d1}d_1/\epsilon_1 + (\epsilon_3/\epsilon_1)(d_1 + w_{sp1}) + \epsilon_3/\epsilon_2 L + w_{sp2}] \cdot qN_{d2}/\epsilon_3 - (\delta + \Delta E_{c1} - \Delta E_{c2} + E_g)/q$$

where ϕ_B is the Schottky barrier height, N_{d1} and N_{d2} are the sheet doping density in the AlGaAs and GaAs supplying layer, w_{sp1} and w_{sp2} are the corresponding spacer layer thickness, d_1 and L are the thickness for the undoped AlGaAs layer and well width, and ΔE_{c1} and ΔE_{c2} are the discontinuity at the conduction band edges. The threshold voltage is a linear function of d_1 in this Mott barrier structure in contrast to a conventional square law dependence for uniformly doped MODFET structures.

MICROWAVE CHARACTERIZATION

Microwave measurements have been performed from 0.5 to 26.5 GHz in 0.5 GHz steps with a pair of Cascade Microtech's microwave wafer probes and an HP 8510 automatic network analyzer. S-parameter data have been taken with the gate and drain biased at various voltages, and been fitted to the equivalent circuit model depicted in Figure 4 through a computer optimization program FETFITTER. Figure 5 shows the measured and modeled two-port S-parameters. It shows very smooth measured data as well as a very

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good fit from the equivalent circuit parameters. Various power gains taken at one set of bias combination are plotted in Fig. 6. An f_{max} of 72 GHz and f_T of 19 GHz are obtained by extrapolating the data with a 5 dB/octave slope. Since the FET parasitics are changing with the bias conditions, higher f_T of 21.6 GHz and higher f_{max} of 85 GHz are observed at other bias combinations as shown in Figs 7 and 8, respectively. The value of f_{max} shown in Fig. 8 is calculated from the fitted equivalent circuit parameters using the equation

$$f_{max} = f_T / \sqrt{4(R_{in} + R_s + R_G)/R_{ds} + 4\pi f_T C_{dg}(R_{in} + R_s + R_G)}$$

derived in Ref. [11], because the stability factor (K) may not always be greater than unity over the measured frequency range.

BIAS-DEPENDENT EQUIVALENT CIRCUIT MODEL

From the measured S-parameters at various gate and drain bias combinations, we can study the bias-dependent equivalent circuit model as shown in Fig. 8. The bias-dependent equivalent circuit parameters such as g_m , C_{gs} , C_{gd} , T_d , C_{ds} , R_{ds} , and R_{in} are depicted in Figs. 10 through 16. In general, the trend of dependence of the circuit parameters on the gate and drain voltages in the FET saturation region are similar to those reported for MESFETs [12]. However, the detailed functional dependence [13] are quite different than the MESFETs. The g_m curves are dominated by the gate biased and less sensitive to the V_{ds} variation before the two dimensional electron gas in the channel are fully established. The C_{gs} behaves like a parallel plate gate-to-channel capacitor with its size determined by the applied V_{gs} [13]. C_{ds} is much less sensitive to the changes in the gate and drain biases, and the value of the FET output impedance (R_{ds}) is very high due to the excellent carrier confinement through the quantum well structure. This kind of confinement is very essential for the devices of short gate length to deliver enough power gain at high operating frequencies. T_d shows the carrier transit time effect due to the longer effective gate length from the increased depletion region underneath the gate to accommodate the increased gate or drain potentials.

There are some abnormal behavior in Figures 10 through 16, particularly when the gate is forward-biased. These abnormalities are related to real-space transfer of the energetic electrons from the two-dimensional quantum well into the AlGaAs layer. Real-space transfer is one of the dominant high field transport mechanisms in MODFETs [14] in contrast to the inter-valley transfer mechanism commonly observed in the GaAs MESFETs. We reported the observation of high frequency (K-band) instability in these MODFETs due to the negative differential resistance induced by the real space transfer phenomenon [15]. This instability and related device characteristic is being studied and the details will be published later.

SUMMARY

In summary, we have fabricated a high performance one-micron MODFET which has high transconductance, high channel current, and high power gain cut-off frequencies. The one-micron gate length device is capable of driving oscillator up to 60 GHz. Bias-dependent equivalent circuit model were established to correlate the device performance such as power gains and cut-off frequencies. These bias-dependent device parameters are very useful tools to optimize the FET structures for higher power density and efficiency at millimeter-wave frequencies.

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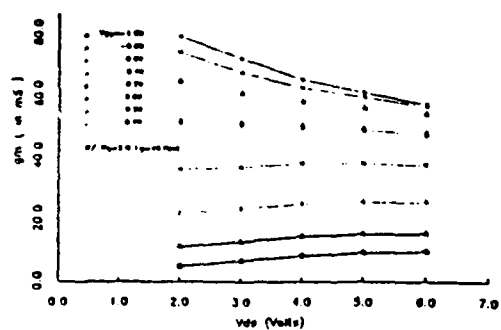


Fig. 9 g_m versus bias.

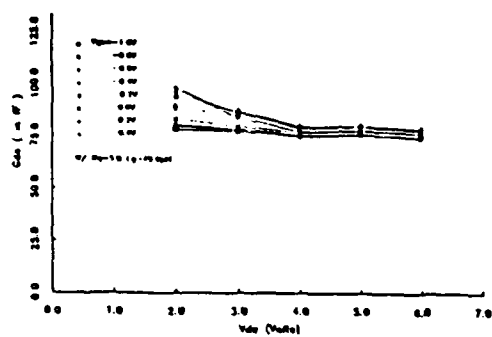


Fig. 13 C_{gs} versus bias.

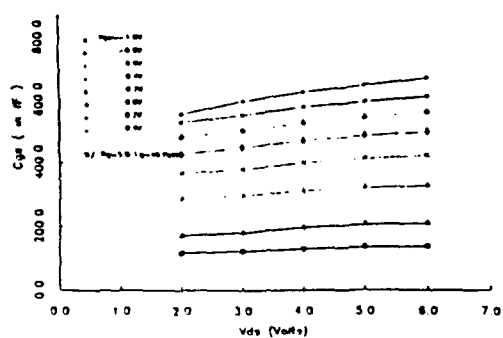


Fig. 10 C_{gd} versus bias.

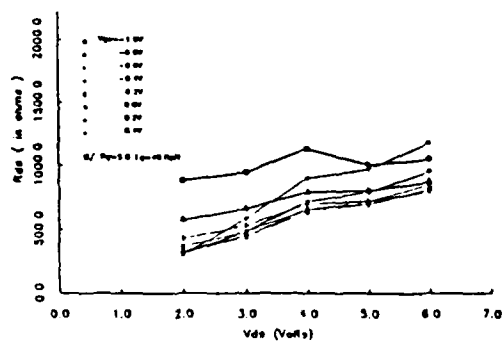


Fig. 14 R_{on} versus bias.

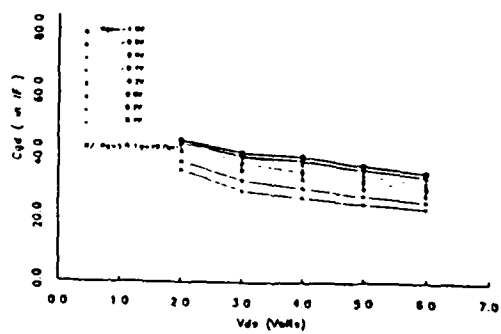


Fig. 11 C_{id} versus bias.

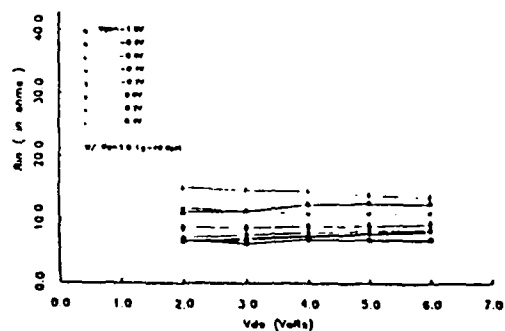


Fig. 15 R_m versus bias.

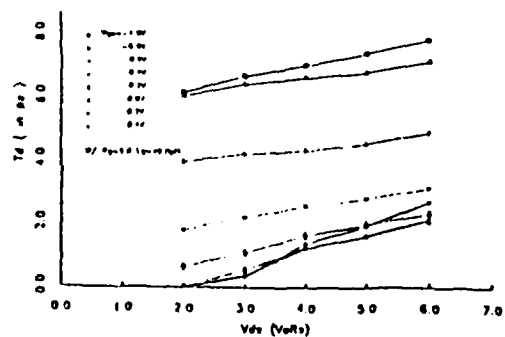
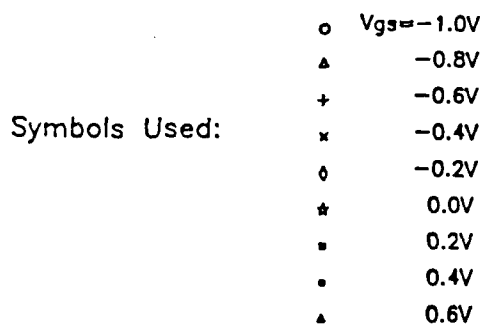


Fig. 12 T_d versus bias.



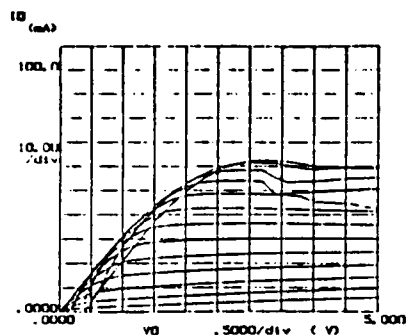


Fig. 1 Room temperature drain I-V characteristics of a 1 x 100 μm FET

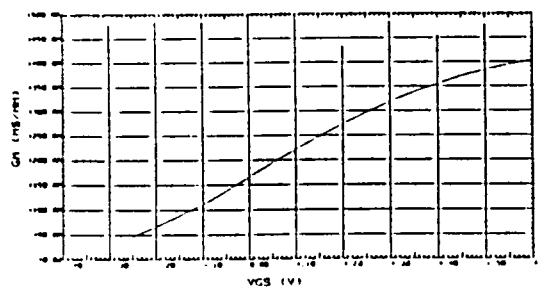


Fig. 2 Extrinsic DC transconductance at room temperature normalized to 1-mm gate width

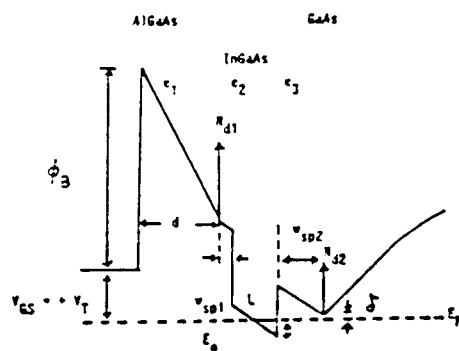


Fig. 3 Conduction band diagram of the double heterojunction structure.

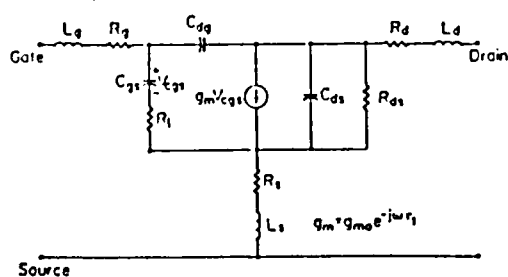


Fig. 4 Equivalent circuit model used in the bias dependent analysis

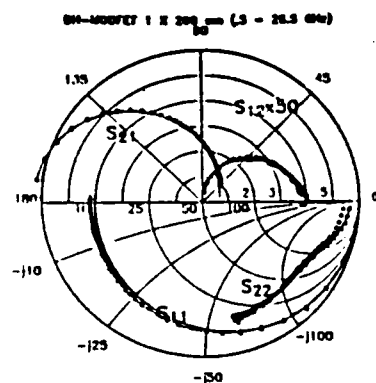


Fig. 5 Composite Smith chart/polar plot of the measured and modeled 2-port S-parameters.

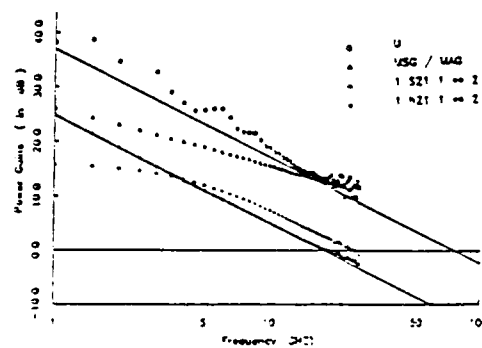


Fig. 6 Various power gains versus frequency.

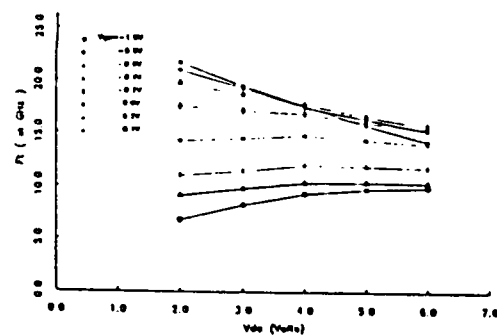


Fig. 7 Unity current-gain cut-off frequency (f_T) at various bias points.

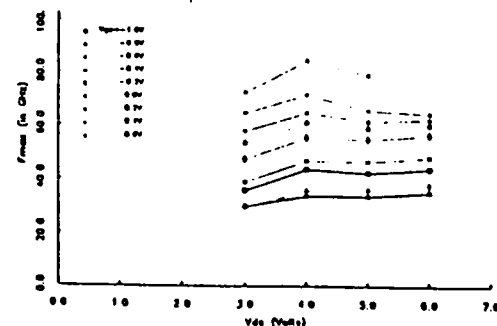


Fig. 8 Unity power gain cut-off frequency (f_{max}) at various bias points.

The Effect of Buried p-Doped Layers on the Current Saturation Mechanism in AlGaAs/InGaAs/GaAs MODFETs

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This abstract describes the first investigation of the effect of buried p-doped layers on the current saturation mechanism in short gate-length MODFETs.

Current saturation in conventional short gate-length MODFETs is observed to follow the gradual channel approximation of non-velocity saturated current typical of long gate devices. The phenomenon of substrate current due to deconfinement of carriers into the buffer has been offered as an explanation. The effective velocity of the carriers is reduced, which degrades the RF performance of the MODFET. Thus it is desirable to reduce substrate current. AlGaAs buffers have been used to increase the confinement of carriers in both GaAs MESFETs and AlGaAs/GaAs MODFETs[1]. More recently buried p-layers have been used in short gate-length GaAs MESFETs[2].

In this work we will discuss the first use of a buried beryllium-doped layer in the GaAs buffer of the pseudomorphic $n^+ \text{Al}_{0.2}\text{Ga}_{0.8}\text{As}/\text{In}_{0.15}\text{Ga}_{0.85}\text{As}/\text{GaAs}$ MODFET. Our modeling of the structure by a one-dimensional Poisson solution predicts improved confinement of carriers due to a built-in field induced in the buffer by the p-layer. Our experimental work includes the study of recessed-gate devices with gate lengths of 0.3 microns. Material is grown by MBE and includes MODFET structures where both the doping concentration and the depth of the Be-layer are varied, as well as an AlGaAs/InGaAs/GaAs structure with a conventional buffer for comparison. Our characterization techniques are DC IV, 77K, CV, and 2-18 GHz RF measurements.

Experimental results demonstrate that the buried p-layer provides a much sharper current saturation characteristic. We observe a very low knee voltage (channel voltage less than 0.3 volts) in the DC IV characteristic. We also observe very sharp pinchoff in the transconductance characteristic; the tail that is characteristic to conventional buffer devices is absent. In agreement with the improved DC characteristics, we observe significant improvements in RF performance at a very low drain potential. For example, at $V_{ds} = 0.8\text{V}$ and $I_{ds} = 33 \text{ mA/mm}$, we observe an increase in measured f_t from 28 GHz in the conventional buffer to 38 GHz in the p-layer buffer and a reduction in the RF output conductance from 40 mS/mm to 22 mS/mm. At $V_{ds} = 0.8\text{V}$ and $I_{ds} = 100 \text{ mA/mm}$ we observe an increase in measured f_t from 33 GHz to 38 GHz and a reduction in output conductance from 107 mS/mm to 40 mS/mm. This represents a 35 and 20% increase in effective velocity at the respective bias points.

The improved velocity observed in the p-layer devices supports the theory that substrate current due to deconfinement of carriers plays a significant role in the current saturation mechanism of short gate-length MODFETs. Since the buried p-layer provides improved RF performance at very low drain bias, these devices could be useful in low noise applications.

This work is supported by a National Science Foundation Graduate Fellowship, and in part by the Joint Services Electronics program, Office of Naval Research, Raytheon and IBM.

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ENHANCEMENT OF 2DEG DENSITY IN GaAs/InGaAs/AlGaAs DOUBLE HETEROJUNCTION POWER MODFET STRUCTURES BY BURIED SUPERLATTICE AND BURIED P⁺-GaAs BUFFER LAYERS

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GaAs/InGaAs/AlGaAs double heterojunction structures, employing atomic planar doping and high potential barrier buffer layers of either buried superlattice or buried beryllium-doped p⁺-GaAs layers, have been successfully fabricated for the first time. Improved two dimensional electron gas (2DEG) concentration, up to $1.7 \times 10^{12} \text{ cm}^{-2}$, is realized by effective charge control at both the top and bottom heterojunction interfaces.

To generate large output power in MODFETs, both high current density and high gate breakdown voltage are needed. Because of the limited 2DEG concentrations generated by a single heterojunction (SH) MODFET structure, usually less than $1 \times 10^{12} \text{ cm}^{-2}$, various workers have studied double or multiple heterojunction structures to improve the total sheet charge densities [1,2]. However, the electron transfer mechanism at the bottom inverted heterojunction interface is dominated by the barrier potential of the buffer layer. Since thick and undoped AlGaAs buffer layer were always used by the previous workers, the total donor density in the bottom electron supplying layers was kept low to avoid poor pinch-off characteristics and parasitic conduction in the bottom AlGaAs layer. This poor charge control by using the uniformly doped AlGaAs buffer layer resulted in less contribution to the total 2DEG charge density from the bottom hetero-interface compared to the top interface.

We have previously reported [3] improved AlGaAs/GaAs/AlGaAs MODFET performance and gate breakdown voltages by using atomic planar doped AlGaAs layers. Now we present the successful fabrication of GaAs/InGaAs/AlGaAs double heterojunction (DH) MODFET structures with enhanced 2DEG densities by using atomic planar doping in conjunction with either buried superlattices (BSL) or buried beryllium doped p⁺-GaAs (BP) buffer layers. With these structures, the bottom electron supplying layer can be doped much heavier as well as transferring more electrons into the 2DEG without generating parasitic conduction. Very low output conductance is also achieved because of the excellent electron confinement from these high barrier buffer layers. This will be a very important factor to realize high frequency, high power FETs with very short gate length.

The FET structures were grown by MBE with atomic planar doped electron supplying layers and either BSL or BP buffers. The fabricated FETs of 1.2-micron gate length have been characterized at both DC and RF frequencies. The room temperature extrinsic DC g_m is 408 mS/mm for the BSL-DHMODFETs, and is 300 mS/mm for the BP-DHMODFETs. The full channel currents are 610 mA/mm from a BSL-DHMODFET and 430 mA/mm from a BP-DHMODFET. The measured current gain cut-off frequency (f_c) is 21.5 GHz from a BSL-DHMODFET and 16 GHz from a BP-DHMODFET. From this RF information, we have obtained 2DEG densities of $1.5 \times 10^{12} \text{ cm}^{-2}$ for the BSL-DHMODFET and $1.7 \times 10^{12} \text{ cm}^{-2}$ for the BP-DHMODFET structure. A 12 dB MAG (maximum available gain) were measured at 20 GHz for both BSL-DHMODFET and BP-MODFET, which is translated into an excellent f_{max} (maximum available power gain cut-off frequency) of 80 GHz. The g_m , f_c , and f_{max} values are amongst the highest yet reported to date for GaAs MODFETs with one-micron gate length. Preliminary CW power measurements (limited by the sensitivity of power meters and tuning networks) of the BSL-DHMODFET show .45 W/mm power density with 36% power added efficiency and 11 dB linear gain at 10 GHz, and .36 mW/mm with 22% power-added efficiency and 7dB linear gain at 18 GHz. The BP-DHMODFET demonstrated .43 W/mm and 10.3 dB gain at 10GHz, and .26 W/mm and 4.6 dB gain at 18 GHz. Both power density and gain are comparable to the best power densities previously reported on a triple-heterojunction MODFET with a smaller gate length of 0.5-micron [2] and a DH-MODFET with higher breakdown voltages [1].

We have demonstrated for the first time the enhancement of 2DEG density as well as better electron confinement in a double heterojunction MODFET structure by using novel atomic planar doped electrons supplying layers in conjunction with buried superlattice or buried beryllium doped GaAs buffer layers. Very efficient charge control at the bottom inverted hetero-interface can also be accomplished by utilizing these structures. Our experiments show that further improvements in the 2DEG densities in inverted MODFETs and multiple heterojunction MODFETs can be achieved by using high barrier buffer layers, together with high atomic planar doping of the bottom electron supplying layer.

This work is supported by the Joint Services Electronics Program, GE, AMOCO, IBM, and the Office of Naval Research.

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Effects of substrate misorientation and background impurities on electron transport in molecular-beam-epitaxial grown GaAs/AlGaAs modulation-doped quantum-well structures

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Single GaAs quantum wells, clad with $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$, and modulation doped with silicon introduced in the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ after the quantum wells are grown have been grown by molecular-beam epitaxy on GaAs substrates tilted a few degrees from the nominal (001) plane towards either of the (111) planes. The low-field two-dimensional electron gas mobility is observed to be a function of the tilt angle (0° , 2° , 4° , 6.5°) and of the direction of tilt [towards (111)*A* or (111)*B*]. The two-dimensional electron gas mobilities in quantum-well structures grown on substrates tilted towards (111)*A* are larger than those in structures grown on nominally flat (001) substrates. The improvement in two-dimensional electron gas transport is attributed to an improvement in the quality of the inverted interface (i.e., GaAs grown on AlGaAs). Quantum wells grown on substrates tilted toward (111)*A* also exhibit larger two-dimensional electron gas mobilities than quantum wells grown on substrates tilted toward (111)*B* for a given angle of tilt. For quantum-well structures where interface scattering from the inverted interface is significant, the two-dimensional electron gas mobility is observed to be anisotropic and larger in the [110] direction in comparison to the $[\bar{1}10]$ direction. The anisotropy in electron transport in the GaAs quantum well is observed to be larger for structures where the substrate tilt is towards (111)*B* in comparison to (111)*A*. For quantum wells grown on substrates tilted toward (111)*A* the anisotropy in two-dimensional electron gas mobility gets progressively larger as the tilt angle gets smaller. Larger molecular-beam epitaxy machine background impurity concentrations are observed to significantly increase the magnitude of the anisotropy in two-dimensional electron gas mobility suggesting that impurities and/or defects introduced during MBE growth are the origin of the anisotropic transport.

I. INTRODUCTION

Structures grown by molecular-beam epitaxy (MBE) with GaAs on top of AlGaAs (inverted interface) are desirable for applications to high-speed electron devices in addition to optical devices. However, poor structural, electronic, and optical properties have been associated with inverted interfaces in comparison to interfaces resulting from the growth of AlGaAs on top of GaAs (normal interface).¹⁻¹² Roughness and impurity trapping at the inverted interface have been suggested as the contributing factors to the inferior properties.¹⁻¹² Optimization of MBE growth conditions and GaAs/AlGaAs layer structure of the material grown just prior to the inverted interface have resulted in improved electrical and optical properties but are still not comparable to the normal interface.¹⁻¹²

It has recently been shown by Tsui and co-workers^{1,13,14} that when MBE growth is performed on a GaAs substrate which is tilted a few degrees from (001) in an appropriate direction that the morphological and optical properties of thick AlGaAs and GaAs/AlGaAs single quantum wells can be improved. The observation of this effect has introduced a new parameter which may be varied to optimize the MBE growth of GaAs/AlGaAs heterostructures: the orientation of the GaAs substrate.

We have previously observed degraded and anisotropic electron transport in GaAs modulation-doped quantum wells grown on thick $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$.¹⁵ The two-dimensional electron gas (2DEG) mobility was observed to be highest in the [110] direction and lowest in the $[\bar{1}10]$ direction while intermediate directions had intermediate mobilities. The anisotropy is attributed to interface scattering from the inverted interface. We observed that the degree of anisotropy was related to the thickness and growth parameters of the $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ layer grown just prior to the inverted interface. The introduction of an appropriate superlattice structure just prior to the growth of the inverted interface eliminates the anisotropy and improves the 2DEG transport. In our previous work, all structures were grown on GaAs substrates tilted 2° off the (001) plane towards the (011) plane. The purpose of this work is to further investigate the effect of substrate orientation on the 2DEG transport in the GaAs modulation-doped quantum-well structures with inverted interfaces.

In this paper, we present 77-K low-field transport data on modulation-doped quantum-well structures grown by MBE on substrates oriented 0° , 2° , 4° , and 6.5° off the (001) plane towards either (111)*A* or (111)*B*. We show that the 2DEG mobility is a function of the angle and direction of the substrate orientation. In addition, we show that the 2DEG mobility is a function of the direction of the applied electric field in the GaAs quantum well (i.e., anisotropic). The an-

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isotropy in 2DEG mobility is also a function of the tilt angle and tilt azimuth direction of the substrate from the (001) plane. The dependence of the 2DEG transport on substrate orientation is attributed to interface scattering from the inverted interface. We show that the amount of interface scattering from the inverted interface is a sensitive function of the amount of background impurities in the MBE machine.

II. EXPERIMENT

The epitaxial layers were grown by MBE in a Varian GEN II machine on undoped liquid encapsulated Czochralski (LEC) grown GaAs substrates. The substrates were cut either 0° , 2° , 4° , or $6.5^\circ \pm 0.25^\circ$ off the (001) plane toward either (111)*A* (gallium face) or (111)*B* (arsenic face) unless otherwise specified. For each growth run three to five substrates with different orientations were mounted side by side, using indium, on the molybdenum mounting block. The substrates were rotated during growth at 7 rpm. The substrate temperature during growth was 620°C . The growth rate of GaAs and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ was 1.0 and $1.43 \mu\text{m/h}$, respectively, for all structures grown in this study. The surface reconstruction determined by electron diffraction during growth of GaAs was an arsenic-stabilized $C(2 \times 8)$ mesh. The V/III beam equivalent pressure ratio determined by an ion gauge in the growth position was 7 to 10. The same arsenic flux was used for both the GaAs and $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ growth.

The structure used in this study is shown in Fig. 1. The GaAs buffer is followed by a $500 \text{ \AA}$ graded $\text{Al}_x\text{Ga}_{1-x}\text{As}$ region of ($0 < x < 0.3$) to minimize the contributions of an extra 2DEG at this interface in the transport measurements. The thickness of the GaAs in the superlattice buffer L_{GSL} was either 5, 15, or $20 \text{ \AA}$ depending on the growth run. A quantum well of $150 \text{ \AA}$ thickness was chosen for this work so

400 $\text{\AA}$	GaAs:Si ($1 \times 10^{18} \text{ cm}^{-3}$)
325 $\text{\AA}$	undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$
Silicon Atomic Plane ($6 \times 10^{12} \text{ cm}^{-2}$)	
75 $\text{\AA}$	undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ spacer
150 $\text{\AA}$	GaAs Quantum Well
5,000 $\text{\AA}$	Superlattice Buffer (L_{GSL} GaAs/200 $\text{\AA}$ $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$) $L_{\text{GSL}} = 5, 15, \text{ or } 20 \text{ \AA}$
500 $\text{\AA}$	Graded $\text{Al}_x\text{Ga}_{1-x}\text{As}$
3,000 $\text{\AA}$	GaAs Buffer
GaAs S.I. Substrate (Cut θ off (001), $\theta = 0, 2, 4, \text{ or } 6.5^\circ$)	

FIG. 1. Layer structure of modulation-doped quantum wells.

TABLE I. Summary of growth runs.

Growth run	Thickness of GaAs in superlattice buffer ($\text{\AA}$)	Substrate tilt
A	5	0° nominally flat
A	5	2° towards (111) <i>A</i>
A	5	4° towards (111) <i>A</i>
A	5	6.5° towards (111) <i>A</i>
B	15	2° towards (111) <i>A</i>
B	15	2° towards (111) <i>B</i>
B	15	2° towards (011)
C	5	4° towards (111) <i>A</i>
C	5	4° towards (111) <i>B</i>
C	5	6.5° towards (111) <i>A</i>
C	5	6.5° towards (111) <i>B</i>
D	15	0° nominally flat
D	15	4° towards (111) <i>A</i>
D	15	4° towards (111) <i>B</i>
D	15	6.5° towards (111) <i>A</i>
D	15	6.5° towards (111) <i>B</i>
E	15	0° nominally flat
E	15	2° towards (111) <i>A</i>
E	15	4° towards (111) <i>A</i>
E	15	6.5° towards (111) <i>A</i>
F	20	0° nominally flat
F	20	2° towards (111) <i>A</i>
F	20	4° towards (111) <i>A</i>
F	20	6.5° towards (111) <i>A</i>

that the wave function of the electrons in the 2DEG would strongly interact with the inverted interface and be very sensitive to the quality of it.¹⁵ A $75\text{-\AA}$ undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ spacer was followed by an atomic planar-doped electron supplying layer as shown in Fig. 1. During silicon deposition for the atomic planar doping, growth was suspended for 45 s with only silicon and arsenic impinging on the substrate to accumulate 6×10^{12} silicon atoms per square centimeter.

Growth runs *A*, *B*, *E*, and *F* were performed when the maximum 2DEG 77-K mobility which could be achieved in the MBE machine in single heterojunction wide spacer ($200 \text{ \AA}$) $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}/\text{GaAs}$ modulation-doped structures was only $\approx 95\,000 \text{ cm}^2/\text{V s}$. During the growths of *C* and *D*, mobilities greater than $200\,000 \text{ cm}^2/\text{V s}$ could be obtained in the MBE machine. Growth runs *E* and *F* were performed with the flow of liquid nitrogen into the growth chamber liquid nitrogen shrouds but were insufficient to keep the shrouds at 77 K. The purpose of restricting the flow of liquid nitrogen was to intentionally increase the background impurity concentrations in the MBE machine. Growth runs *A*, *B*, *E*, and *F* are considered to be "low-purity" growths, while growth runs *C* and *D* are considered to be "high-purity" growths.

Table I summarizes the growth runs presented in this study. Growth run *D* contained an undoped LEC substrate cut $2^\circ \pm 0.5^\circ$ off the (001) plane towards the (011) plane for comparison with previous work.¹⁵ Except for this substrate, all other substrates were cut from the same LEC ingot.

Van der Pauw-Hall measurements were made using

cloverleaf patterns and a square active area with edges aligned along the $\langle 110 \rangle$ cleavage directions. These measurements were made in the dark at liquid-nitrogen temperature in a magnetic field of 2 kG.

III. RESULTS

Figure 2 shows the 77 K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[\bar{1}\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) determined using the van der Pauw method¹⁵⁻¹⁷ versus substrate tilt angle for growth run A (low purity). Growth run A (low purity) has a superlattice composed of 5 Å of GaAs and 200 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ grown on substrates tilted toward $(111)A$. The 2DEG transport is observed to be anisotropic since the ratio of $\mu_{[110]}$ to $\mu_{[\bar{1}\bar{1}0]}$ is not unity. We observe the degree of anisotropy to be a function of the tilt angle and to decrease as this angle is increased. As seen in Fig. 2, the geometric mean mobility is also a function of the substrate tilt angle and a maximum at 4° off the (001) plane. As seen in Fig. 2, growth on a nominally flat (001) GaAs substrate gives inferior 2DEG mobilities in comparison to substrates oriented a few degrees off (001) toward $(111)A$.

Figure 3 shows the 77-K geometric mean mobility and mobility ratio versus the tilt direction for growth run B (low purity) for (001) GaAs substrates cut 2° off the (001) plane. Growth run B (low purity) has a superlattice composed of 15 Å of GaAs and 200 Å of $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$. We observe that the geometric mean mobility and the degree of anisotropy is a function of the tilt direction of the substrate for a given tilt angle. As seen in Fig. 3, tilt towards $(111)A$ (gallium face) results in the maximum geometric mean mobility and the minimum degree of anisotropy when compared to tilts toward either $(111)B$ (arsenic face) or (011) . Structures grown on substrates tilted toward either $(111)B$ (arsenic

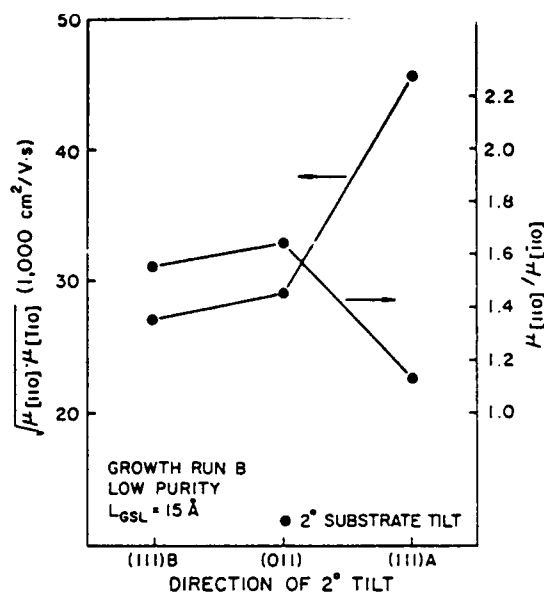


FIG. 3. 77-K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[\bar{1}\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) vs the direction of substrate tilt for a (001) GaAs substrate cut 2° off the (001) plane for growth run B.

face) or (011) give essentially equivalent 2DEG low-field transport.

A comparison between growth runs A (low purity) and B (low purity) shows that the structure of the superlattice (thickness of GaAs in the superlattice) plays a role in determining the quality of the inverted interface as previously reported.¹⁵ Superlattices composed of thicker GaAs layers result in superior inverted interface transport in comparison to superlattices with thinner GaAs layers. Growth runs A (low purity) and B (low purity) were both performed when

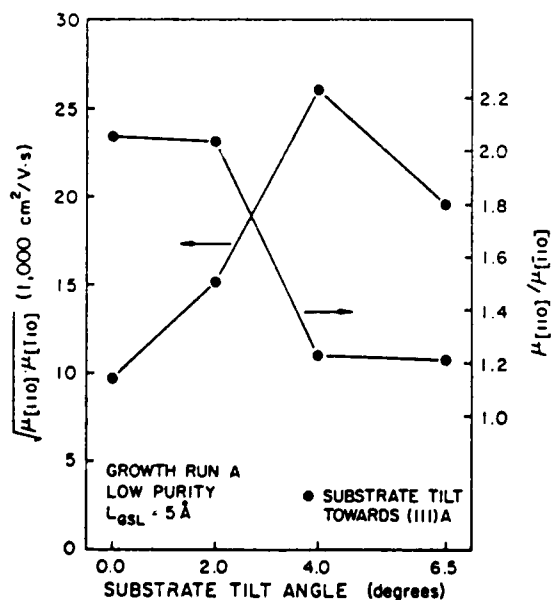


FIG. 2. 77-K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[\bar{1}\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) vs the amount of substrate tilt towards $(111)A$ for growth run A.

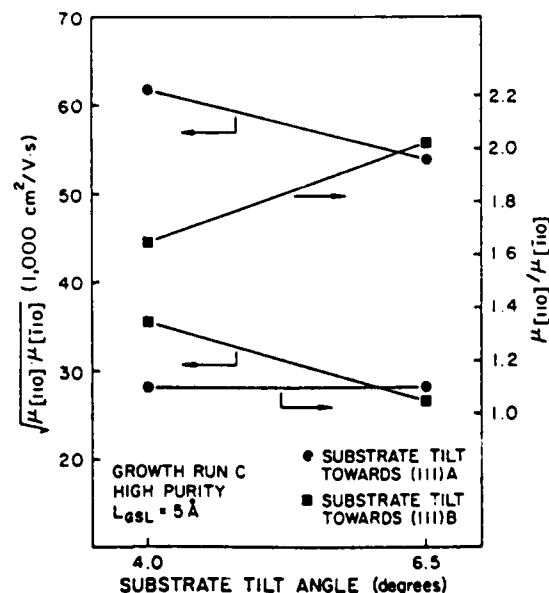


FIG. 4. 77-K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[\bar{1}\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) vs substrate tilt angle for growth run C.

a 77-K 2DEG mobility of only 95 000 cm²/V s could be obtained in the MBE machine in single heterojunction wide spacer GaAs/Al_{0.3}Ga_{0.7}As modulation-doped structures. Growth runs *C* (high purity) and *D* (high purity) were performed when greater than 200 000 cm²/V s could be obtained in the MBE machine. Figure 4 shows the geometric mean mobility and mobility ratio versus the substrate tilt angle for growth run *C* (high purity) which contained 5 Å of GaAs in the superlattice buffer as was the case in growth run *A* (low purity). Comparing Fig. 4 to Fig. 2 reveals that the mobilities are significantly higher and the anisotropies significantly lower for the similar structures. As was the case in Fig. 2, Fig. 4 indicates that the geometric mean mobility is larger for substrates cut 4° off the (001) plane in comparison to ones cut 6.5° off the (001) plane. Figure 4 also indicates that the 2DEG mobilities are larger on substrates cut off the (001) plane toward (111)*A* in comparison to substrates cut off (001) toward (111)*B*, consistent with growth run *B* (low purity).

Figure 5 shows the geometric mean mobility and mobility ratio versus the tilt angle for growth run *D* (high purity) which contained 15 Å of GaAs in the superlattice buffer as in growth run *B* (low purity). The transport is always isotropic, independent of the substrate angle and direction of misorientation which was not the case for growth run *B* (low purity) which contained an identical superlattice (15 Å of GaAs and 200 Å of Al_{0.3}Ga_{0.7}As). The 77-K 2DEG mobilities are significantly higher than those obtained in growth run *B* (low purity). Figure 5 also indicates that there is a slight dependence of the magnitude of the mobility on tilt angle and tilt direction. The mobility is larger for substrates cut 4° off the (001) plane than for substrates cut 6.5° off the (001) plane, as was the case in growth runs *A* (low purity) and *C* (high purity). In addition, the 2DEG transport is superior on substrates cut off the (001) toward (111)*A* in compari-

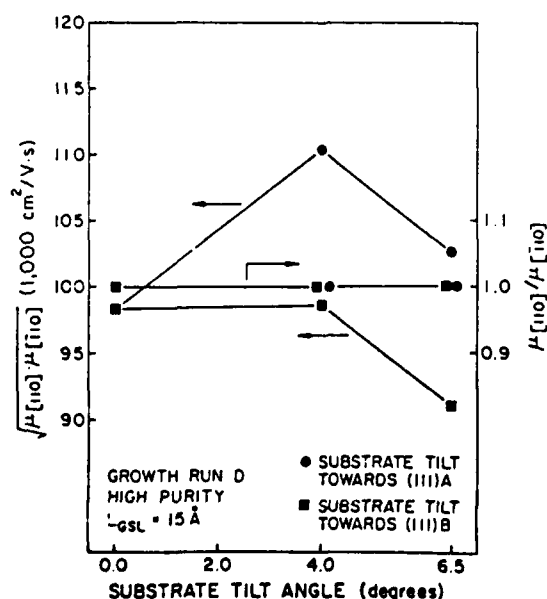


FIG. 5. 77-K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[1\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[1\bar{1}0]}$) vs substrate tilt angle for growth run *D*.

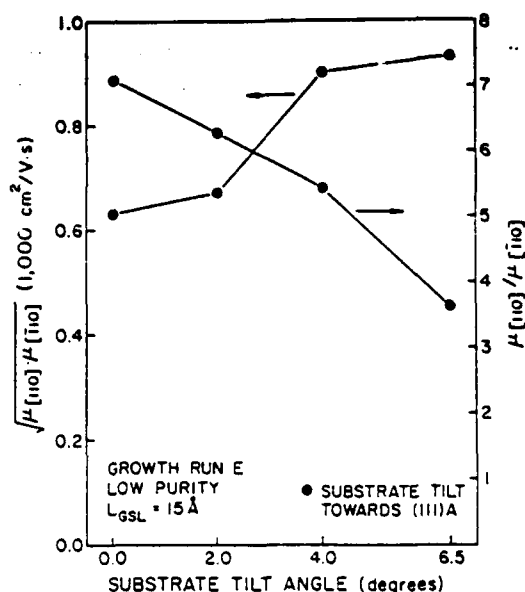


FIG. 6. 77-K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[1\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[1\bar{1}0]}$) vs the amount of substrate tilt towards (111)*A* for growth run *E*.

son to substrates cut off the (001) toward (111)*B* direction, as was observed in growth runs *B* (low purity) and *C* (high purity).

Growth runs *A*, *B*, *C*, and *D* suggest that background impurities in the MBE machine may have significant effects on the inverted interface in comparison to the normal interface. To investigate the role of impurities on the anisotropy in the 2DEG transport, growth runs *E* (low purity) and *F* (low purity) were performed with the growth chamber liq-

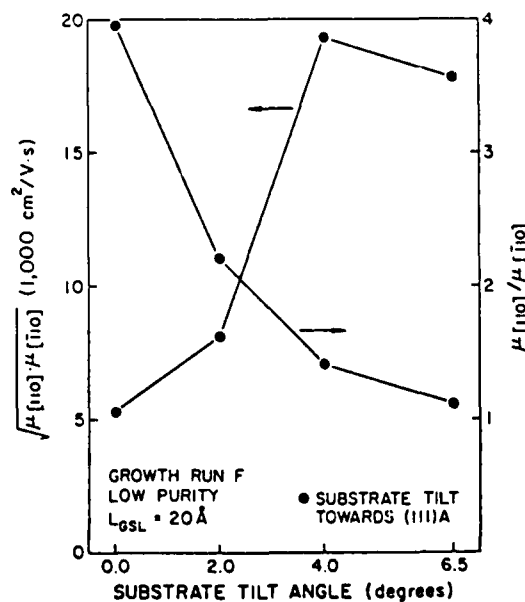


FIG. 7. 77-K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[1\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[1\bar{1}0]}$) vs the amount of substrate tilt towards (111)*A* for growth run *F*.

uid nitrogen shrouds not fully cold (> 77 K) in an attempt to intentionally increase the background impurity concentrations in the MBE machine. Figures 6 and 7 show the geometric mean mobilities and mobility ratios versus the substrate tilt angle from (001) towards the (111)*A* direction. Growth runs *E* (low purity) and *F* (low purity) contain 15 and 20 Å of GaAs in the superlattice, respectively. As seen in Figs. 6 and 7, anisotropies significantly higher than those previously observed are obtained, indicating that background impurities play a major role in determining the degree of anisotropy in 2DEG transport at the inverted interface. As seen in Figs. 6 and 7, the degree of anisotropy decreases as the angle of tilt increases, consistent with the previous growth runs. The electron sheet densities measured in the dark for growth runs *A*, *B*, *C*, *D*, *E*, and *F* are approximately 6×10^{11} , 6×10^{11} , 8×10^{11} , 8×10^{11} , 4×10^{11} , and 5×10^{11} cm $^{-2}$, respectively.

IV. DISCUSSION

Figures 2–7 indicate that substrate misorientation from (001) during MBE growth has significant effects on the quality of 2DEG transport at the inverted interface. Structures grown on substrates tilted off the (001) plane toward (111)*A* are found to give higher 2DEG mobilities than those toward either (111)*B* or (011). In addition, 4° of tilt is found to give larger 2DEG mobilities than 0°, 2°, or 6.5° for our given set of growth conditions and layer structure. Tsui *et al.*¹ have recently shown that the quality of the surface morphology and photoluminescence of AlGaAs/GaAs quantum wells grown on tilted (001) GaAs substrates depend upon the angle and direction of tilt for their given set of growth conditions and layer structure. It can be concluded that structural, optical, and electronic properties of GaAs/AlGaAs heterojunctions are all affected when MBE growth is performed on vicinal (misoriented) GaAs surfaces.

Vicinal GaAs surfaces have been studied by other authors using electron diffraction^{18,19} and electron spectroscopy.²⁰ Hottier *et al.*¹⁸ have shown, using electron diffraction from vicinal (001) GaAs surfaces, that monatomic steps are more ordered on vicinal surfaces cut 3° off (001) toward (111)*A* in comparison to vicinal surfaces cut 3° off (001) toward (111)*B*. Using electron spectroscopy, Ranke *et al.*²⁰ have studied oxygen adsorption on a cylindrical GaAs sample which exposed the main low index orientations (001), (111)Ga, and (111)As as well as their vicinal surfaces. They observe higher oxygen adsorption rates on vicinal surfaces cut off (001) toward (111)*B* in comparison to vicinal surfaces cut off (001) toward (111)*A*. They also observe the amount of adsorption to be a function of the angle of tilt (0°–20°) about (001). A vicinal GaAs substrate cut off (001) towards (111)*A* contains step edges with gallium atoms with single dangling bonds at the step edges (gallium-type), while a substrate cut off (001) towards (111)*B* contains step edges with arsenic atoms with single dangling bonds at the step edges (arsenic type).^{18,19} The data of Refs. 1, 18, 19, and 20 suggest that these two step edges (gallium type and arsenic type) are fundamentally different, resulting in vicinal surfaces which are fundamentally different. An island on a flat

(001) GaAs surface will have gallium-type step edges in the [110] direction while in the $\bar{[110]}$ direction arsenic-type step edges will exist.^{18,19} As a result, even a nominally flat (001) GaAs surface has two types of steps (gallium type [110] and arsenic type $\bar{[110]}$).

Anisotropies in MBE grown GaAs/AlGaAs structures have been previously observed. The transverse correlation length in the plane of the epitaxial layers of a GaAs/AlAs superlattice has been observed to be anisotropic in x-ray diffraction measurements.²¹ The correlation length in the direction of the arsenic-type step edges $\bar{[110]}$ was observed to be longer than the correlation length in the direction of the gallium-type step edges [110]. Reflection high-energy electron diffraction,²² photoluminescence,²³ and transport measurements^{15,24–26} have also revealed anisotropies in the $\bar{[110]}$ and [110] directions which are in the direction of the arsenic-type and gallium-type steps, respectively.

Other authors^{24–26} have observed anisotropic 2DEG transport in single heterojunction structures and have suggested that interface monomolecular steps due to a substrate tilt are responsible for the anisotropy in their structures. The anisotropies were observed in structures with reduced phonon and remote impurity scattering achieved by using a low measurement temperature (≈ 4 K) and wide undoped AlGaAs spacers, respectively. It is important to realize that the maximum mobility we observe is always in the [110] direction independent of the direction and angle of the substrate tilt. This implies that scattering due to single monomolecular steps at the inverted interface produced by the substrate tilt is not the origin of the anisotropic transport in our structures. Had this been the case, the anisotropy would be enhanced as the substrate tilt angle is increased, in contrast to the data presented in Figs. 2–7.

Figures 2–7 suggest that impurities and/or defects introduced during MBE growth in the epitaxial layers are responsible for the observed anisotropies in 2DEG transport at the inverted interface. There are two possible scattering mechanisms which could account for anisotropies in the electron transport in our structures. The impurities and/or defects could give rise to anisotropic impurity/defect scattering at the inverted interface. Skolnick *et al.*²³ have suggested that impurity and/or defect pairs can be preferentially oriented parallel to one of the $\langle 110 \rangle$ directions in MBE grown structures. This phenomenon could give rise to anisotropic impurity/defect scattering. A second possible anisotropic scattering mechanism could be the result of impurities and/or defects inducing anisotropic surface roughness during the growth of the inverted interface.²⁷ This mechanism would give rise to anisotropic interface scattering. Figures 2–7 suggest that the impurity and/or defect concentrations in the as-grown heterostructures can be reduced by reducing the background impurities in the MBE machine or by reducing the terrace length on the MBE growth front with respect to the migration length of the group III adatoms by intentionally orienting the substrate a few degrees off (001). These two seemingly independent mechanisms are observed to have the same effect on the 2DEG transport at the inverted interface: the 2DEG transport is improved, and the anisotropies due to impurities and/or defects are reduced.

We observe higher 2DEG mobilities on substrates oriented 4° off (001) toward (111)*A* than either 0° , 2° , or 6.5° for growth runs *A*, *C*, *D*, and *F*. The terrace length due to the substrate misorientation for 0° , 2° , 4° , and 6.5° of misorientation are ∞ , 80, 40, and 25 Å, respectively.^{18,19} If the improvement in 2DEG mobility was solely related to a reduction in the terrace length on the growth front then a substrate tilt angle of 6.5° would presumably give equivalent or higher 2DEG mobilities than 4° . The fact that a substrate tilt angle of 6.5° gives slightly inferior 2DEG mobilities than a substrate tilt of 4° indicates that a reduction in the terrace length on the growth front is not the only mechanism responsible for the 2DEG mobility to be a function of the angle of substrate tilt towards (111)*A*. Oxygen adsorption on a cylindrical GaAs sample showed that there is an optimum angle from 0° to 20° of substrate tilt for minimizing oxygen adsorption.²⁰ This fact suggests that impurity incorporation during MBE growth may be a function of the substrate orientation. Wang *et al.*²⁸ have observed that impurity incorporation during MBE growth was a function of the surface orientation when comparing the (001), (113)*A*, and (113)*B* surfaces of GaAs. In Fig. 6 we observe that the maximum mobility occurs at 6.5° tilt when the background impurities are high enough to give extremely low 77 K mobilities ($< 1000 \text{ cm}^2/\text{V s}$). This may be an indication that the optimum angle of misorientation is a function of the growth conditions and/or environment.

Comparing growth run *A* (low purity) to growth run *B* (low purity), we see that thick (15 Å) GaAs layers in the superlattice buffer give higher 2DEG mobilities and smaller amounts of anisotropy than thin (5 Å) GaAs layers. The same statement can be made when comparing growth run *C* (high purity) to growth run *D* (high purity). Comparing the "low-purity" growths (*A* and *B*) to the "high-purity" growths (*C* and *D*), we see that the 2DEG mobilities and anisotropies are a sensitive function of the MBE machine purity. The above effects may be explained by either periodic smoothing of the superlattice growth front during MBE growth or periodic trapping of impurities and/or defects in the superlattice buffer, both of which could be accomplished through periodic deposition of GaAs in the superlattice buffer.^{1-12,15}

The 2DEG mobilities obtained in growth run *D* (high purity) are comparable to structures grown without AlGaAs in the buffer (i.e., single heterojunction).¹⁵ This is an indication that the inverted interface is of reasonable quality. It is important to realize that these 2DEG mobilities are only obtainable when very high 77-K 2DEG mobilities ($> 200\,000 \text{ cm}^2/\text{V s}$) are achieved in single heterojunction wide spacer (200 Å) structures in our MBE machine and thick (15 Å) GaAs layers are used in the superlattice buffer of quantum-well modulation-doped structures.

V. CONCLUSIONS

The effects of substrate misorientation from (001) and background impurities on electron transport in MBE grown GaAs/AlGaAs modulation-doped superlattice-buffered quantum-well structures have been investigated. The quality of 2DEG transport is a function of the thickness of the GaAs

layers in the superlattice buffer. The substrate orientation has been observed to have effects on the 2DEG transport for a GaAs/AlGaAs superlattice buffered quantum well grown at 620°C . The 2DEG mobility has been observed to be a function of the tilt angle and of the tilt direction of the substrate relative to the (001) surface. The dependence of 2DEG mobility on the tilt angle and direction is believed due to the quality of the inverted interface being a function of the substrate orientation. The inverted interface structure has been observed to give rise to anisotropic 2DEG transport in the GaAs quantum well. We observe that the degree of anisotropy is a function of the angle and direction of the substrate misorientation. Impurities and/or defects introduced during MBE growth are the origin of the observed anisotropies in 2DEG transport. Background impurities in the MBE machine are observed to significantly affect the quality of the 2DEG transport in the GaAs quantum well.

The 2DEG mobilities in quantum wells grown on substrates tilted toward (111)*A* are observed to be larger than 2DEG mobilities on substrates tilted toward (111)*B*. The anisotropy in 2DEG mobility is also larger for substrates tilted toward (111)*B* in comparison to (111)*A*. For quantum wells grown on substrates tilted toward (111)*A*, the 77-K 2DEG mobility is highest for substrates cut 4° off (001) in comparison to 0° , 2° , or 6.5° . In addition, the anisotropy in 2DEG mobility is smaller the larger the angle of substrate tilt. Smaller background impurity concentrations in the MBE machine produce larger 2DEG mobilities and smaller amounts of anisotropic transport. In addition, thicker GaAs layers in the superlattice buffer produce larger 2DEG mobilities and smaller amounts of anisotropic transport. We have observed three ways to increase 2DEG mobilities and decrease 2DEG anisotropies: tilting the substrate a few degrees off (001) towards (111)*A*, decreasing the background impurities in the MBE machine, and employing thicker GaAs layers in superlattice buffers.

ACKNOWLEDGMENTS

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THE EFFECT OF SUBSTRATE ORIENTATION ON DEEP LEVELS IN N-AlGaAs GROWN BY MOLECULAR BEAM EPITAXY

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ABSTRACT

Deep electron traps in Si-doped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ grown by molecular beam epitaxy (MBE) on GaAs substrates deliberately misoriented (tilted 0 to 6 degrees) off the (001) plane towards either (111)A, (111)B or (011) have been investigated using deep-level transient capacitance spectroscopy (DLTS). Of the three dominant traps observed in AlGaAs, the concentrations of two of these are observed to be a direct function of the substrate tilt, while the concentration of the third dominant trap, which is related to the DX-center, is independent of the substrate misorientation.

INTRODUCTION

Recently, it has been shown that a deliberate substrate misorientation of a few degrees off (001) towards (111)A during MBE can improve the electron transport, optical and morphological properties of AlGaAs/GaAs heterostructures [Tsui et al 1986, 1986a, 1985b, Radulescu et al 1987, 1987a]. However, deep electron traps in doped AlGaAs dominate the optical and electrical characteristics of heterojunction devices, while the impact of the misoriented substrate on these traps has not been investigated at all. This paper discusses the effect of substrate misorientation on deep electron traps in MBE grown AlGaAs. We have varied the substrate tilt angle and tilt direction in addition to the substrate temperature (610°C to 650°C) during growth. The dependence of deep-level concentrations on these MBE growth parameters will help in identifying which impurities and/or defects are affected by substrate misorientation during MBE growth.

EXPERIMENTAL

The structures used in this study were grown by MBE in a Varian GEN II on semi-insulating liquid encapsulated Czochralski (LEC) grown GaAs substrates cut either 0, 2, 3 or 6 ± 0.5 degrees off the (001) plane towards either (111)A, (111)B, or (011). The structures consist of a 7500Å GaAs buffer layer doped with silicon at $1 \times 10^{18} \text{ cm}^{-3}$ followed by 2000Å of $2 \times 10^{17} \text{ cm}^{-3}$ silicon-doped GaAs, 2500Å of $1.5 \times 10^{17} \text{ cm}^{-3}$ silicon-doped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$, and finally a 100Å undoped GaAs cap.

For each growth run (D1, D2, D3 and D4), three substrates with different orientations were mounted side by side, using indium on the molybdenum mounting block. The substrate temperature during growth of the AlGaAs was either 610, 625 or 650°C, while the GaAs was grown at 610°C for all growth runs.

The growth rate of GaAs and AlGaAs was 1.0 and 1.33 $\mu\text{m/h}$, respectively. Reflection high energy electron diffraction patterns taken along the $\langle 110 \rangle$ azimuth exhibited second and third order reconstructions for the GaAs and AlGaAs, respectively. Two arsenic sources (As_4) were used for the GaAs growth, while one was used for AlGaAs growth. Table 1 summarizes the substrate orientations and the AlGaAs growth temperatures used for the four growth runs presented in this study. Following epitaxial growth, conventional 600 μm diameter diodes were fabricated. DLTS measurements were performed with a system described previously [Kirchner et al 1981]. The diodes were reversed biased at 2.5V with a trap filling pulse of 3.0V for 2.5 mS. DLTS spectra were generated using the capacitance transient data at 4 and 20 mS, resulting in a rate window of 100 Hz.

RESULTS AND DISCUSSION

Fig. 1 shows typical DLTS spectra of electron traps in the silicon-doped AlGaAs structures from growth run D1 as a function of the substrate misorientation: 6° towards (111)A, 6° towards (111)B, and 2° towards (011). The spectra show the existence of seven electron trap levels labeled ME1 through ME7. The dependence of these commonly seen seven traps (ME1-ME7) on aluminum mole fraction, growth temperature, and V/III flux ratio have been previously reported [Yamanaka et al 1987, 1987a, Naritsuka et al 1985, Mooney et al 1985]. In addition, their capture cross sections and thermal activation energies have been thoroughly studied. However, their fundamental origins not completely understood. In this paper we concentrate on the properties of the three dominant traps (ME3, ME5, ME6) observed in the spectra and their dependence on substrate tilt angle and tilt direction in addition to growth temperature. The trap labeled ME3 in Fig. 1 is attributed to the DX-center commonly observed in silicon doped AlGaAs [Yamanaka 1987, Lang 1979, Yamanaka 1984a]. As seen in the figure, its concentration is independent of the substrate misorientation. In contrast, the concentrations of the other two dominant traps (ME5 and ME6) are observed to be a function of the substrate misorientation. The concentrations of these traps are smallest for the substrate misoriented 6° towards (111)A and largest for the substrate misoriented 6° towards (111)B. A substrate misorientation of

Growth Run	Substrate Orientation Off (001)	AlGaAs Growth Temperature
D1	6° Toward (111)A 2° Toward (011) 6° Toward (111)B	625°C
D2	0° Nominally flat 3° Toward (111)A 6° Toward (111)A	610°C
D3	3° Toward (111)A 2° Toward (011) 3° Toward (111)B	625°C
D4	0° Nominally Flat 3° Toward (111)A 6° Toward (111)A	650°C

Table 1
Summary of the growth runs, substrate orientations, and AlGaAs growth temperatures used for this study.

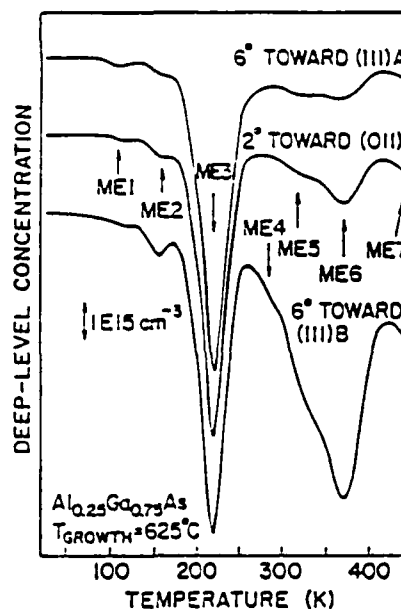


Fig. 1. Typical DLTS spectra showing electron traps for growth run D1 as a function of the intentional substrate misorientation off a nominal (001) surface.

Fig. 1 indicates that a substrate tilt toward (111)A results in a lower concentration of deep-levels than tilt toward (111)B. To investigate the significance of the angle of tilt toward (111)A growth run D2 was performed. In Fig. 2 the concentrations of levels ME3, ME5, and ME6 are plotted as a function of substrate tilt angle toward (111)A. As seen in the figure, the concentration of level ME3, which is related to the DX-center, is independent of substrate tilt angle consistent with growth run D1. However, the concentrations of levels ME5 and ME6 progressively decrease as the tilt angle increases. Fig. 2 indicates that a substrate tilt toward (111)A can improve the electrical quality of MBE grown AlGaAs in comparison to material grown on a nominally flat substrate at 610°C.

A comparison between the effect of the tilt angle and tilt direction on the deep-level concentrations can also be made for a higher growth temperature of 625°C by plotting the deep-level concentrations for growth runs D1 and D3 versus substrate tilt. This is done in Fig. 3. As can be seen in the figure, trap level ME3 is again independent of substrate tilt, while trap levels ME5 and ME6 are dependent on the tilt angle and tilt direction. As the tilt angle toward (111)B progressively increases, the deep-level concentrations of ME5 and ME6 also progressively increase. This effect is in contrast to tilt toward (111)A where a larger tilt angle improves the electrical quality of MBE-grown AlGaAs.

In Figs. 4a,b, and c the dependence of the deep-level concentrations of ME3, ME5 and ME6, respectively, on $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ growth temperature and tilt angle toward (111)A are plotted. As can be seen in the figures, all three trap concentrations are a minimum at 625°C in comparison to 610°C or 650°C. In addition, even at the highest growth temperature (650°C), the trap concentrations (ME5 and ME6) are still a function of the substrate tilt angle.

CONCLUSION

The influence of a substrate tilt off (001) during MBE on the incorporation of deep electron traps has been investigated. Tilt toward (111)A reduces the incorporation of ME5 and ME6, whereas tilt toward (111)B increases the incorporation of these deep levels, in comparison to nominally flat substrates. The DX-center (ME3) concentration is independent of substrate tilt.

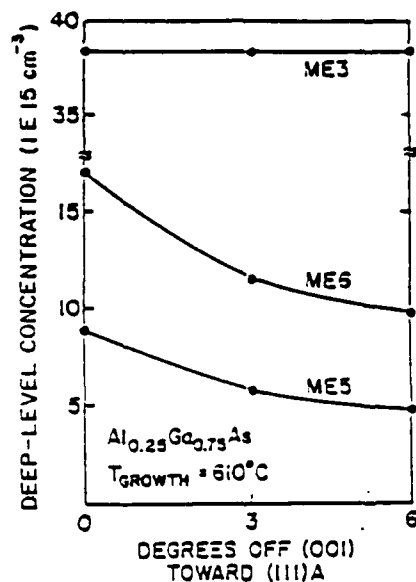


Fig. 2. Electron trap concentrations of ME3, ME5 and ME6 for growthrun D2 as a function of the angle of tilt off (001) toward (111)A.

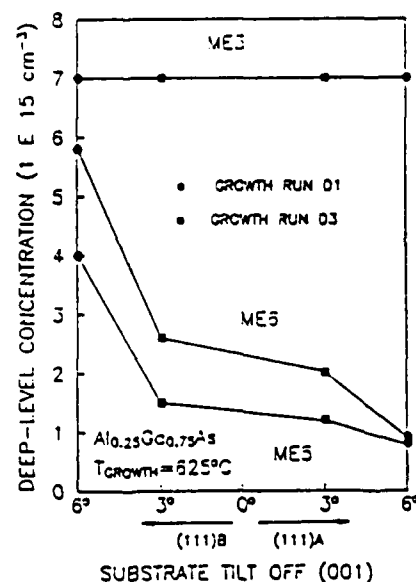
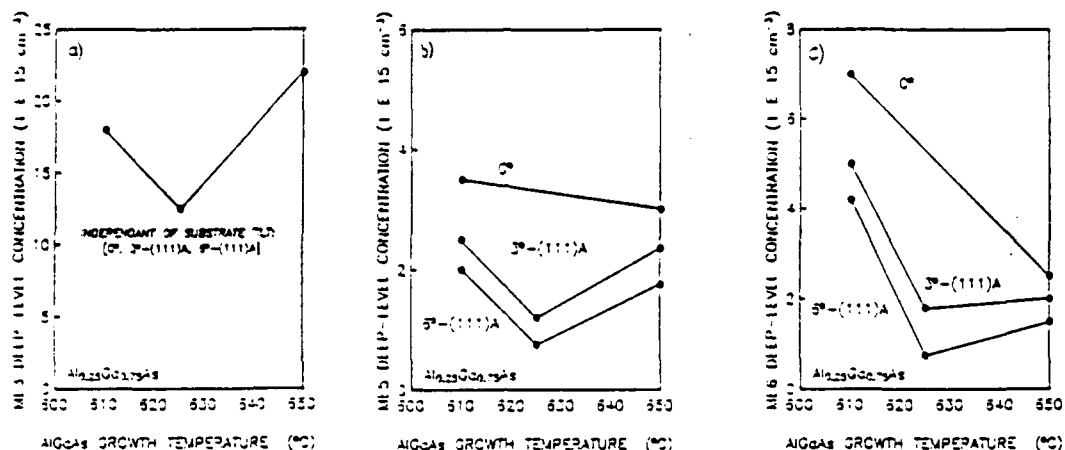


Fig. 3. Electron trap concentrations of ME3, ME5 and ME6 for growth runs D1 and D3 as a function of the substrate tilt angle and tilt direction off (001).



Figs. 4a, b, and c. Concentrations of ME3, ME5 and ME6, respectively, as a function of AlGaAs growth temperature and substrate tilt angle off (001) toward (111)A.

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A high-gain short-gate AlGaAs/InGaAs MODFET with 1 amp/mm current density

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ABSTRACT

Quadruple heterojunction MODFETs (Modulation Doped Field Effect Transistor) with a planar-doped lattice-strained AlGaAs/InGaAs structure have been fabricated and characterized at DC and microwave frequencies. At 300 K the 0.3- μ gate devices show a full channel current of 1100 mA/mm with a constant extrinsic transconductance of 350 mS/mm over a broad gate voltage range of 1.6 volts. Excellent microwave performance is also achieved with a maximum available gain cut-off frequency (f_{mag}) of 110 GHz and a current gain cut-off frequency (f_T) of 52 GHz. This is the highest current density ever reported for either GaAs MESFETs or MODFETs along with excellent high frequency performance.

Single heterojunction AlGaAs/GaAs modulation doped field-effect transistors (MODFETs) have shown excellent microwave performance especially for low noise application [Berenz 1984]. Because of a limited sheet charge concentration of less than 10^{12} cm⁻² per heterojunction, multiple heterojunction MODFETs [Saunier, et al. 1986, Gupta 1985] were then investigated to increase the current driving capability and consequently improve the power performance and switching speed. Recently the AlGaAs/InGaAs pseudomorphic MODFET has shown better performance than the AlGaAs/GaAs MODFET [Chen, et al 1987]. The larger band discontinuity and better transport characteristics in the AlGaAs/InGaAs system have resulted in higher two-dimensional electron gas (2DEG) concentrations and higher current density. Among the highest current densities reported to date are 600 mA/mm from six-fold AlGaAs/GaAs heterojunctions [Saunier et al 1986] and 610 mA/mm from strained-layer AlGaAs/InGaAs double heterojunctions [Chen et al 1987].

We reported double heterojunction AlGaAs/GaAs/AlGaAs MODFET structures with two silicon planar-doped layers [Chen et al. 1986a]. This planar doping technique provides good charge control of the 2DEG sheet density. Little light sensitivity at 77K is observed due to the much reduced heavily doped AlGaAs region. In this paper, we report the fabrication and characterization of planar-doped AlGaAs/InGaAs pseudomorphic quadruple heterojunction MODFETs with high current density and high cut-off frequencies suitable for microwave and millimeter-wave power applications.

As shown in Fig. 1, the device layer structure is grown by MBE on a semi-insulating undoped LEC GaAs substrate. The structure consists of two AlGaAs/InGaAs/AlGaAs quantum wells with three silicon planar-doped AlGaAs layers. The silicon sheet densities are 6×10^{12} cm⁻², 3×10^{12} cm⁻² and 1×10^{12} cm⁻² respectively. The details of the growth conditions were similar to those reported in [Chen et al 1987].

The grown wafers were fabricated with a recess-gate FET process. Mesa isolation was performed by wet chemical etching. The source and drain of the device were defined by optical lithography with a mid-UV contact aligner. Ni/AuGe/Ag/Au contacts were subsequently evaporated and alloyed at 475°C for 15 seconds with a rapid thermal annealer. A specific contact resistivity of 0.05 ohm-mm was obtained from the transmission line measurement. T-shape gates with 0.3- μ m footprints were defined by electron beam lithography and followed by Ti/Pd/Au metalization. A PMMA/P(MMA-MAA)/PMMA triple layer electron beam resist system has been developed to obtain fine line width, high aspect ratio, and good lift-off profile [Wang, et al 1987]. These lead to a T-shaped gate with small gate length and low gate resistance which improves the high frequency performance of the device. The measured DC end-to-end resistance is typically 120 ohm-mm.

The room temperature current-voltage characteristics of a 0.3 x 100 μ m device is shown in Fig. 2. A drain saturation current of 1100 mA/mm is obtained at a gate voltage of 1V. The high current density is the result of the high 2DEG concentration in the InGaAs channels. The MODFET of 0.3- μ m gate length shows very good output conductance owing to good carrier confinement in the pseudomorphic quantum-well structure. A constant DC transconductance of 350 mS/mm is obtained over the gate voltage from -1V to 0.6V as shown in Fig. 3. The low transconductance variation is essential for low intermodulation distortion in power applications as reported in [Gupta et al 1985]. The gate-drain breakdown voltage is 6 to 7 V. Further optimization of the layer structure is required to achieve high current and high breakdown voltage simultaneously.

400 Å	GaAs:Si (2×10^{18} cm $^{-3}$)
300 Å	undoped Al $_{0.3}$ Ga $_{0.7}$ As
Si planar-doped (8×10^{12} cm $^{-2}$)	
30 Å	undoped Al $_{0.3}$ Ga $_{0.7}$ As spacer
175 Å	In $_{0.15}$ Ga $_{0.85}$ As Quantum Well
50 Å	undoped Al $_{0.3}$ Ga $_{0.7}$ As spacer
Si planar-doped (3×10^{12} cm $^{-2}$)	
30 Å	undoped Al $_{0.3}$ Ga $_{0.7}$ As spacer
175 Å	In $_{0.15}$ Ga $_{0.85}$ As Quantum Well
50 Å	undoped Al $_{0.3}$ Ga $_{0.7}$ As spacer
Si planar-doped (1×10^{12} cm $^{-2}$)	
100 Å	undoped Al $_{0.3}$ Ga $_{0.7}$ As spacer
10,000 Å	Al $_{0.3}$ Ga $_{0.7}$ As/GaAs superlattice
GaAs S.L. substrate	

Fig. 1. Layer structure of the quadruple heterojunction AlGaAs/InGaAs MODFET.

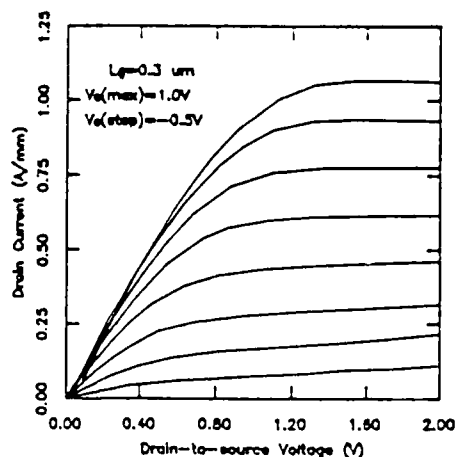


Fig. 2. Current-voltage characteristics of a 0.3- μ m gate MODFET.

Microwave S-parameter measurements have been performed for various bias conditions from 0.5 to 26.5 GHz with microwave wafer probes and an HP 8510 automatic network analyzer. Fig. 4 shows the close agreement between measured and modeled S-parameters at $V_{gs} = 0$ V and $V_{ds} = 2$ V. Power gains from measured S-parameters are depicted in Fig. 5. A current gain cut-off frequency (f_{MAG}) of 110 GHz can be extrapolated. Intrinsic f_T calculated by using the equivalent circuit and $f_T = g_m/2\pi C_{gs}$ is 57 GHz, which is reasonably close to the one by extrapolation. The stability K factor is less than unity over the whole measurement frequency range. A carrier density as high as $6.5 \times 10^{12} \text{ cm}^{-2}$ can be derived from a drain current of 870 mA/mm at a gate bias of 0.65 V where an f_T of 44 GHz is measured.

In summary, we have demonstrated that extremely high current as well as excellent microwave characteristics can be achieved from a short-gate quadruple heterojunction pseudomorphic MODFETs. The 0.3 μm gate device shows a full channel current of 1100 mA/mm with an f_T of 52 GHz and an f_{MAG} of 110 GHz. This is the highest current density ever reported for microwave FETs. It indicates that short-gate multiple-heterojunction pseudomorphic MODFETs may be of great importance in millimeter-wave power applications.

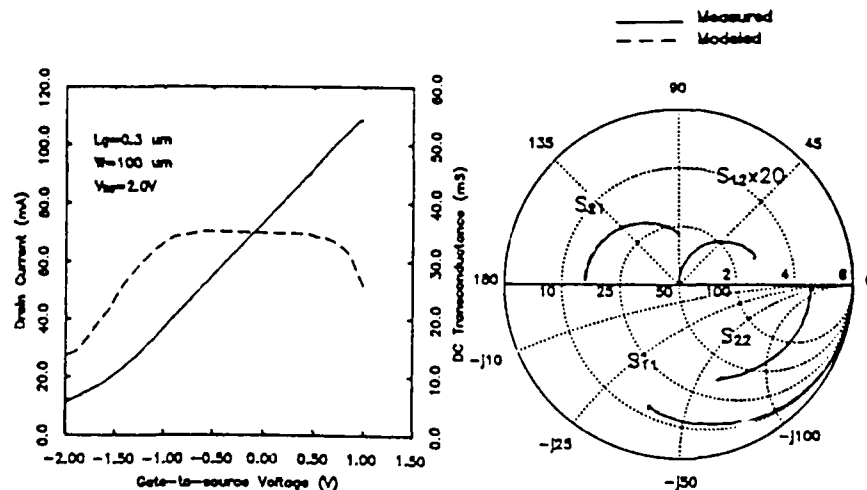


FIG. 3. Transconductance and current vs. V_{gs} at $V_{ds} = 2$ V.

Fig. 4. Measured and modeled S-parameters at $V_{gs} = 0$ V and $V_{ds} = 2$ V.

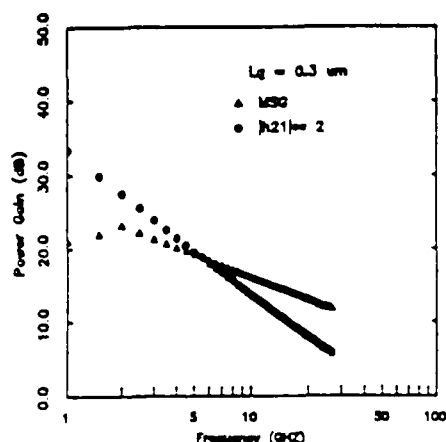


Fig. 5. Power gains vs. frequency at $V_{gs} = 0V$ and $V_{ds} = 2V$.

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Influence of an intentional substrate misorientation on deep electron traps in AlGaAs grown by molecular beam epitaxy

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Deep level transient capacitance spectroscopy has been used to investigate deep level electron traps in thick silicon-doped AlGaAs grown by molecular beam epitaxy (MBE) on GaAs substrates intentionally misoriented (tilted) a few degrees from a nominally (001) surface. Of the three dominant traps observed in AlGaAs, the concentrations of two of these are observed to be a direct function of the substrate tilt angle and tilt direction. The concentration of the third dominant trap, which is related to the *DX* center, is independent of substrate misorientation during MBE. These observations will help in identifying which impurities and/or defects are affected by substrate misorientation during MBE growth in addition to identifying the origin of deep levels in AlGaAs.

Recently, there has been interest in the study of the effect of an intentional substrate misorientation of a few degrees (0° – 12°) off (001) during molecular beam epitaxy (MBE) on the resulting material properties of AlGaAs/GaAs heterostructures.^{1–5} It has been shown that the optical, electron transport, and morphological properties of AlGaAs/GaAs heterostructures can be improved if the GaAs substrate is misoriented a few degrees toward (111)*A*, in comparison to nominally flat (001) substrates.^{1–5} However, the effects of such a misorientation on the deep level electron trap concentrations have not been investigated although they are a fundamental and important material parameter in AlGaAs/GaAs heterostructures. In this letter we use deep level transient capacitance spectroscopy to investigate deep level electron traps in thick silicon-doped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$ grown by MBE on GaAs substrates misoriented (tilted) from nominally (001) surfaces. We have varied the substrate tilt angle (0° , 2° , 3° , and 6°) and tilt direction [off (001) toward (111)*A*, (111)*B*, and (011)] and have observed that deep level concentrations can depend upon the substrate tilt in a consistent manner. This observation will help in identifying the origin of deep levels in AlGaAs since only recently have their origins been investigated/discussed.^{6,7} In addition, the dependence of deep level concentrations on substrate tilt will help in identifying which impurities and/or defects are affected by substrate misorientation during MBE growth.⁵

The structures used in this study were grown by MBE on semi-insulating liquid encapsulated Czochralski (LEC) grown GaAs substrates cut either 0° , 2° , 3° , or $6^\circ \pm 0.5^\circ$ off the (001) plane towards either (111)*A*, (111)*B*, or (011). The structures consist of a 7500-Å GaAs buffer layer doped with silicon at $1 \times 10^{18} \text{ cm}^{-3}$ followed by 2000 Å of $2 \times 10^{17} \text{ cm}^{-3}$ silicon-doped GaAs, 2500 Å of 1.5×10^{17} silicon-doped $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$, and finally a 100-Å undoped GaAs cap. For each growth run (*A* and *B*), three substrates with different orientations were mounted side by side, using indi-

um on the molybdenum mounting block. The substrate temperature during growth of the AlGaAs was 610 and 625 °C for growth runs *A* and *B*, respectively, while the GaAs was grown at 610 °C for both growth runs. The growth rates of GaAs and AlGaAs were 1.0 and 1.33 $\mu\text{m/h}$, respectively. Reflection high-energy electron diffraction (RHEED) patterns taken along the (110) azimuth exhibited second- and third-order reconstructions for the GaAs and $\text{Al}_{0.25}\text{Ga}_{0.75}\text{As}$, respectively. Two arsenic sources (As_4) were used for GaAs growth, while one was used for AlGaAs growth, resulting in V/III beam equivalent pressure ratios determined by an ion gauge in the growth position of ≈ 19 and 11, respectively. Growth runs *A* and *B* were performed within a 4-h period under identical growth and vacuum conditions except for the specified growth temperature. Following epitaxial growth, conventional 600- μm -diam diodes were fabricated. Deep level transient spectroscopy (DLTS) measurements were performed with a system described previously.⁸ The diodes were reverse biased at 2.5 V with a trap filling pulse of 3.0 V for 2.5 ms. DLTS spectra were generated using the capacitance transient data at 4 and 20 ms.

Typical DLTS spectra of electron traps in the silicon-doped AlGaAs structures from growth run *A* are shown in Fig. 1 for three different substrate misorientations: 6° towards (111)*A*, 6° towards (111)*B*, and 2° towards (011). The spectra show the existence of seven electron trap levels labeled ME1–ME7. These traps have been previously observed⁹ and the labels (ME1–ME7) have been adopted from Ref. 6. In this letter we concentrate on the properties of the three dominant electron traps (ME3, ME5, and ME6) observed in the spectra. The trap labeled ME3 in Fig. 1 is related to the commonly observed *DX* center in AlGaAs.^{6,9,10} As shown, its concentration is independent of the substrate misorientation. In contrast, the concentrations of the other two dominant traps (ME5, ME6) shown in Fig. 1 are observed to be a function of the substrate misorientation. The concentration of these traps is smallest for the substrate misoriented 6° towards (111)*A* and largest for the substrate misoriented 6° towards (111)*B*. A substrate misorientation of 2° towards (011) is seen to result in an intermediate concentration.

Figure 2 shows the trap concentrations of ME3, ME5,

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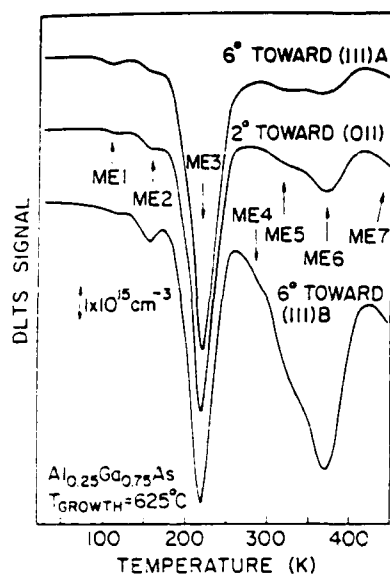


FIG. 1. Typical DLTS spectra showing electron traps for growth run *A* as a function of the intentional substrate misorientation off a nominal (001) surface.

and ME6 versus substrate tilt angle (0° – 6°) toward (111)*A* for growth run *B*. The substrate temperature during this growth run was 625°C , in contrast to growth run *A* where it was 610°C . The three dominant traps for growth run *B* are still ME3, ME5, and ME6. Traps ME1, ME2, ME4, and ME7 show up in concentrations similar to growth run *A*. As shown in Fig. 2, the concentration of trap ME3, which is related to the *DX* center, is independent of substrate tilt angle, consistent with growth run *A*. Also, the concentrations of traps ME5 and ME6 progressively decrease as the tilt angle toward (111)*A* increases, indicating that a substrate misorientation toward (111)*A* during MBE growth of AlGaAs can reduce the deep level electron trap concentrations.

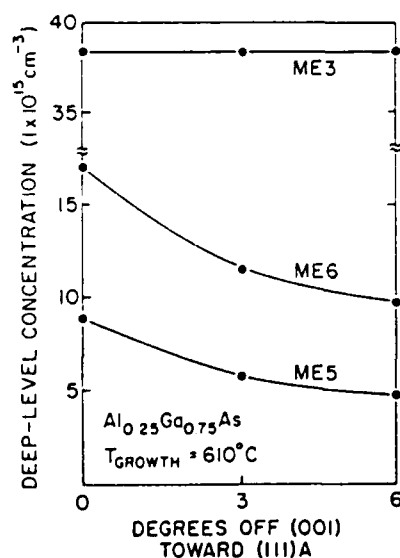


FIG. 2. Electron trap concentrations of ME3, ME5, and ME6 for growth run *B* as a function of the angle of the intentional substrate misorientation off (001) toward (111)*A*.

It should be pointed out that the free-electron densities determined by capacitance-voltage measurements at 300 K for both growth runs (*A* and *B*) were independent of substrate tilt angle and tilt direction. This is an indication that silicon incorporation during MBE growth of AlGaAs does not depend upon the surface step structure for our given doping densities, growth conditions, and tilt angles/directions.

The trends observed in Figs. 1 and 2 as the tilt angle and tilt direction are varied are consistent with the previous studies of the effect of a substrate misorientation on the optical, electron transport, and morphological properties of AlGaAs/GaAs heterostructures.^{1–5} The growth of AlGaAs on substrates misoriented toward (111)*A* resulted in higher purity material in comparison to material grown on nominally flat (001) substrates or substrates misoriented toward (111)*B*. In contrast to photoluminescence and electron transport measurements, we do not observe there to be an optimum angle of substrate tilt toward (111)*A* (between 0° and 6°) to minimize defect/impurity incorporation during MBE growth. This may be an indication that the optimum angle of substrate tilt toward (111)*A* during growth is a function of the layer structure, growth conditions, and/or background impurity concentration in the MBE machine.^{1–5} The identification of the defects and impurities which are affected by a substrate misorientation during MBE growth is not fully understood.⁵ In addition, the fundamental origin of the deep electron traps (ME1–ME7) observed in AlGaAs is also not fully understood.⁶ As a result, the trends observed in Figs. 1 and 2 will help in identifying the defects and impurities which are affected by substrate misorientation during MBE growth in addition to identifying the origin of deep electron traps in AlGaAs.

It has been suggested^{6,7} that electron trap ME5 is associated with oxidation of the arsenic source material. It is important to realize that we observe the concentration of trap ME5 to be a function of the substrate misorientation. As a result, if trap ME5 is associated with oxidation of the arsenic source material, then the incorporation of the impurities/defects which result from the arsenic oxide would have to be a function of the substrate misorientation. Substrate misorientation towards (111)*A* would have to decrease the incorporation of the impurities/defects which result from the arsenic oxide in comparison to nominally flat (001) substrates, or substrates misoriented towards (111)*B*.

It has been suggested that electron trap ME6 is associated with a complex of a gallium vacancy and an oxygen atom^{6,7} or a gallium interstitial.¹¹ As was the case with trap ME5, we observe the concentration of ME6 to be a function of the substrate misorientation. As a result, if trap ME5 is associated with a complex of a gallium vacancy and oxygen atom or a gallium interstitial, then the incorporation of these defects would have to be a function of the substrate misorientation. It is interesting to note that we have previously observed, using photoluminescence, that the incorporation of a defect/impurity complex at 60 meV from the band edge was a function of the substrate misorientation.⁵ It would not be unreasonable to expect that substrate tilt during MBE would affect the concentration of interstitials since the average ter-

race length on the surface during growth can be altered by the tilt.^{12,13} However, one would expect the concentration of aluminum interstitials to be affected more by a substrate tilt than gallium interstitials since the aluminum migration length is smaller than the gallium migration length.¹⁴

Figures 1 and 2 indicate that the concentration of the trap associated with the *DX* center (ME3) in AlGaAs is not dependent upon the substrate misorientation. If the *DX* center is associated with a complex involving a silicon donor atom and an impurity or defect,^{6,9,10} then the concentration of that impurity or defect would have to be independent of substrate misorientation. There are two possible consequences of the above statements: either the incorporation of the impurity or defect associated with the silicon donor atom of the *DX* center complex is independent of substrate misorientation, or the *DX* center is not a complex involving an impurity or defect and a silicon donor but simply a substitutional donor in a complicated multivalley conduction-band system.^{15,16}

In conclusion, we have used deep level transient capacitance spectroscopy to study the influence of an intentional substrate misorientation off (001) during MBE growth on the deep level electron trap concentrations in AlGaAs. We have observed that the deep level concentrations can depend on the substrate tilt angle and tilt direction off (001) in a consistent manner. Our observations will help in identifying which impurities and/or defects are affected by substrate misorientation during MBE growth in addition to identifying the origin of deep levels in AlGaAs.

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**A HIGH PERFORMANCE 0.12 μm T-SHAPE GATE $\text{Ga}_{0.5}\text{In}_{0.5}\text{As}/\text{Al}_{0.5}\text{In}_{0.5}\text{As}$ MODFET
GROWN BY MBE LATTICE MIS-MATCHED ON A GaAs SUBSTRATE**

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ABSTRACT

We report on the first successful fabrication of high performance GaInAs/AlInAs MODFETs of 0.12 μm gate length grown lattice mismatched on a GaAs substrate. A peak extrinsic DC transconductance of 585 mS/mm and a saturated channel current of 370 mA/mm are achieved at room temperature. A high unity current gain cut-off frequency f_T of 107 GHz has been demonstrated. Parasitic conduction which may be the result of the dislocations present under the large-area FET bonding pads and possibly under the active FET channel, however, severely limits the peak f_{max} to 125 GHz.

INTRODUCTION

Gallium arsenide MODFETs (Modulation-Doped Field-Effect Transistors) have demonstrated excellent microwave performance with very high cut-off frequency and very good low-noise performance [1]. On the other hand, $\text{Al}_{0.5}\text{In}_{0.5}\text{As}/\text{Ga}_{0.5}\text{In}_{0.5}\text{As}$ MODFET structures lattice matched to InP have many advantages over the AlGaAs/GaAs or the strained AlGaAs/InGaAs systems, such as superior electronic transport [2], larger conduction band discontinuity at the hetero-interface [3], higher doping capability in AlInAs [4], and hence higher sheet electron concentration at the interface. A high DC transconductance of 650 mS/mm and a very high unity current gain cut-off frequency (f_T) of 85 GHz in a 0.3- μm MODFET have been reported [5]. Since most commercially available semi-insulating InP substrates are heavily compensated by ions and too fragile to be incorporated into the more established GaAs integrated circuit processes, it would be desirable to integrate high performance GaInAs/AlInAs devices on GaAs substrates.

Lattice mismatched growth has been avoided in the traditional heterostructures to prevent large numbers of dislocations from deteriorating the electrical properties of the grown epitaxial layers. We have studied the feasibility of MBE grown GaInAs/AlInAs structures on GaAs substrates [6]. A GaInAs/AlInAs superlattice buffer layer was used to reduce the propagation of dislocations resulting from the 3.8% mismatch in the lattice constants between the buffer layer and GaAs substrate. Dramatic reduction in sheet

dislocation densities was observed after growing a 0.5- μm thick superlattice buffer layer. In this work, GaInAs/AlInAs MODFETs of 0.12 μm T-shape gates were grown and fabricated on a lattice mismatched GaAs substrate with a 1.8 μm superlattice buffer layer. Their performance was evaluated through DC and microwave tests. It was found that very good MODFET performance could be demonstrated with the combination of short gate-length and the excellent electronic property of the GaInAs/AlInAs material system without the constraint of growing on a lattice-matched substrate.

MATERIAL GROWTH AND LAYER STRUCTURE

The MODFET layer structure, as shown in Fig. 1, was grown by MBE on a semi-insulating GaAs substrate in the following sequence: 1.8- μm AlInAs/GaInAs (30Å/10Å) superlattice buffer, 300Å undoped GaInAs channel, 25Å undoped AlInAs spacer, silicon planar doping layer with a density of $4 \times 10^{12} \text{ cm}^{-2}$, 250 Å undoped AlInAs layer, silicon planar doping layer of $2 \times 10^{12} \text{ cm}^{-2}$, 10Å AlInAs layer, and 150 Å GaInAs cap layer with a silicon doping density of $1 \times 10^{19} \text{ cm}^{-3}$. The thick superlattice buffer layer is needed to reduce the dislocations penetrating into the active channel region from the lattice-mismatched buffer/substrate interface. The 250Å AlInAs layer is undoped to reduce the gate leakage current. The highly doped GaInAs cap layer was initially designed to provide possible non-alloyed ohmic contacts for the source and drain of MODFET and demonstrated previously [6]. However, the potential barrier from the ungraded n+-GaInAs/AlInAs hetero-interface together with the undoped AlInAs region made the ohmic alloy necessary.

A small number of dislocations from the lattice mismatched buffer/substrate interface do propagate into the top active MODFET layers. Fig. 2 shows the micro-photograph taken near a local dislocation cluster by a Transmission Electron Microscope (TEM). As can be seen clearly in Fig. 3 some of the dislocation clusters gather together to form micro-cracks on the surface of the grown wafer in the fabricated MODFET bonding pad areas with an optical Nomarski microscope.

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DEVICE FABRICATION

The grown wafers were fabricated by a recess-gate FET process. Device isolation was achieved by boron implantation. Leakage current as low as 80 μ A was measured between two undamaged islands under an applied potential of 40V. After the source and drain regions of the device were defined by optical lithography with a contact aligner, Ni/AuGe/Ag/Au contacts were subsequently evaporated. The specific contact resistivity was measured to be 0.7 $\text{ohm}\cdot\text{mm}$ by transmission line measurements before the alloy process. This non-alloy ohmic contact was made possible by the highly doped GaInAs capping layer and the silicon doping plane just 10Å below the GaInAs/AlInAs heterointerface. To further reduce the contact resistance, the wafer was alloyed at 400°C for 10 sec with a rapid thermal annealer. The specific contact resistivity decreases to 0.02 $\text{ohm}\cdot\text{mm}$. After the short low-temperature alloy cycle the ohmic metals still maintain good surface morphology and sharp edges which are essential for electron beam lithography used for gate definition in later steps.

T-shaped gates with 0.12 μm footprints were defined by electron beam lithography with a PMMA/P(MMA-MAA)/PMMA triple layer resist system [7]. Fig. 4 shows the T-shaped gate after evaporation and lift-off of Ti/Pd/Au. The footprint of the gate is 120 nm while height is more than 1 μm . The end-to-end gate resistance of the device is 160 ohm/mm which is determined by DC resistance measurement and verified by microwave S-parameter measurements. The reduction of gate resistance is very important for the gain and noise performance of MODFETs at high frequencies.

DC RESULTS

Fig. 5 shows the drain I-V characteristics of a 0.12 x 25 μm MODFET at room temperature. The maximum channel current is 370 mA/mm at a V_{DS} of 3V. Fig. 6 shows the plots of g_m and I_d versus V_{GS} at a drain bias of 3.4V. The maximum extrinsic g_m of 585 mS/mm is demonstrated at a gate bias of -0.3V. However, there is a small amount of substrate current, on the order of about 7% of the full channel current, which can not be modulated by the Schottky gate. When the device is cooled down to 77K, this current is reduced but not eliminated completely.

This substrate current is probably the result of the combined leakage currents through the remaining dislocations underneath the active MODFET channel and the dislocations/microcracks surfaced in the large bonding pad area. Microwave measurements, as described in the next paragraph, also reveal the existence of these leakage paths which lower the available power gains delivered by the intrinsic MODFET at high frequency.

MICROWAVE PERFORMANCE

Scattering parameters were measured on an 0.12 x 100 μm MODFET by an HP8510 automatic network analyzer with a pair of wafer probes from 0.5 to 26.5 GHz in 0.5

GHz steps at various gate bias voltages and a V_{DS} of 1.5V. The microwave behavior of the MODFET can be represented by the equivalent circuit model (Fig. 7) derived from the measured S-parameters. Because of the very small gate dimension of 0.12 x 100 μm , extrinsic device parasitics such as bonding pad capacitance could be significant compared to the intrinsic device parameters such as C_{gs} . By fitting bias-dependent S-parameter sets of the MODFET to the equivalent circuits, we are able to separate the bias-independent device parasitics, such as L_g , L_d , L_s , C_g , C_d and R_g , from those bias-dependent elements easily and accurately. Fig. 8 shows the plots of the measured and modeled S-parameters at a V_{GS} of 0.0V and V_{DS} of 1.5V. It shows a very smooth measured data and the errors of fitting is within 3% over the 5 to 26 GHz frequency range. Table 1 shows two sets of equivalent circuit parameters, where the data in set A is taken at high g_m bias and the data in set B is taken near MODFET pinch-off. Two shunt parasitic resistors have to be added to the gate and drain bonding pads in order to give a good fit to the measured S_{11} and S_{22} data. This represents the physical existence of parasitic leakage paths described previously.

From the measured S-parameters and fitted equivalent circuit model parameters, various figure-of-merits such as the unity current gain cut-off frequency (f_T) and maximum available gain cut-off frequency (f_{max}) [8] can be derived. Because those figure-of-merits are bias dependent [9], Fig. 9 shows f_T , f_{max} and the calculated intrinsic f_{max} at various gate biases. A maximum f_T of 107 GHz is obtained at a gate bias of 0 V where the DC transconductance is also maximized. Because the MODFET is not stable over the measurement range up to 26 GHz, f_{max} is extrapolated from the fitted equivalent circuit model. The intrinsic device f_{max} without external parasitics can be calculated with the equation

$$f_{\text{max}} = f_T / \sqrt{4(R_g + R_s + R_d)/R_{\text{DS}} + 4\pi f C_{\text{dg}}(R_g + R_s + R_d)}$$

which is derived from the equivalent circuit model in Fig. 7 [8]. A maximum f_{max} of 125 GHz and a calculated maximum intrinsic f_{max} of 139 GHz are obtained. These numbers are exceptionally high for these greatly mismatched materials and non-optimized lattice-mismatched growth conditions. This work demonstrates the potential of fabricating high performance devices or any novel high quality heterojunction structures without locating a high quality substrate of similar lattice constant.

SUMMARY AND CONCLUSIONS

We have grown and fabricated InGaAs/AlInAs MODFETs lattice mismatched on a GaAs substrate. Substantial reduction in the amount of dislocations propagated to the top epi-layers is achieved by growing a 1.8- μm thick superlattice buffer layer, and the device-quality wafers are resulted. Developments of new processing technologies, such as using planar boron implantation and tri-level electron-beam resist system, yield much improved device performance of the fabricated 0.12- μm MODFETs through the reduced gate leakage current and gate resistance. A peak extrinsic DC transconductance of 585 mS/mm and

a saturated channel current of 370 mA/mm are achieved at room temperature with a very high f_T of 107 GHz from microwave measurements.

The maximum available gain cut-off frequency, f_{max} of 125 GHz, is probably limited by dislocations and micro-cracks present under the active channel and large bonding pads. Nevertheless, an intrinsic device f_{max} of 139 GHz can be calculated from the fitted equivalent circuit model. The future improvements in the growth techniques with further reduction in the dislocation density in the active epi-layers would bring various theoretical heterojunction devices to life and integrate them with the existing high quality substrates such as GaAs and Si.

ACKNOWLEDGEMENTS

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20 Å	GaInAs II	$1 \times 10^{18} \text{ cm}^{-3}$
10 Å	AlInAs	$2 \times 10^{18} \text{ cm}^{-3}$
150 Å	AlInAs	undoped
25 Å	AlInAs	$4 \times 10^{18} \text{ cm}^{-3}$
100 Å	GaInAs channel	
1.3 µm	AlInAs/GaInAs superlattice	10Å/10Å
GaAs Substrate		

Fig. 1. GaInAs/AlInAs layer structure of a grown lattice-mismatched on a GaAs substrate by MBE.



Fig. 2. TEM microphotograph near a local dislocation cluster.



Fig. 3. Microphotograph of a fabricated MODFET with visible micro-cracks under a Nomarski microscope.



Fig. 4. SEM microphotograph of a T-shaped gate with a 0.12-μm foot-print.

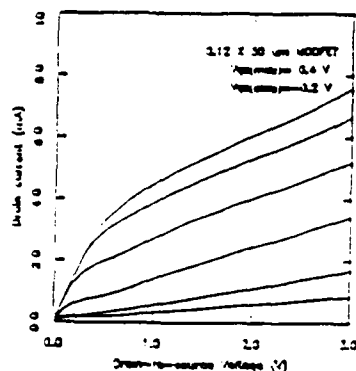


Fig. 5. DC drain I-V characteristics of a 0.12x50 μm MODFET.

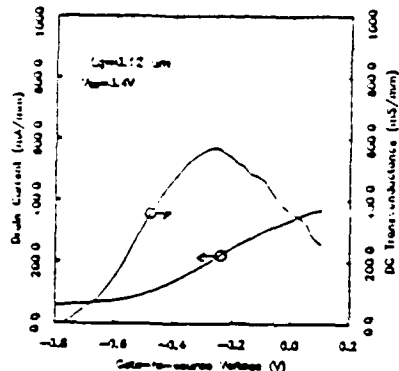


Fig. 6. Normalized DC g_m and I_{dss} versus gate bias.

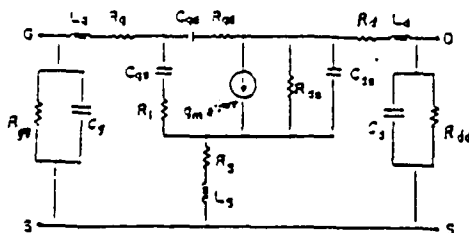


Fig. 7. Microwave small signal circuit model of a MODFET.

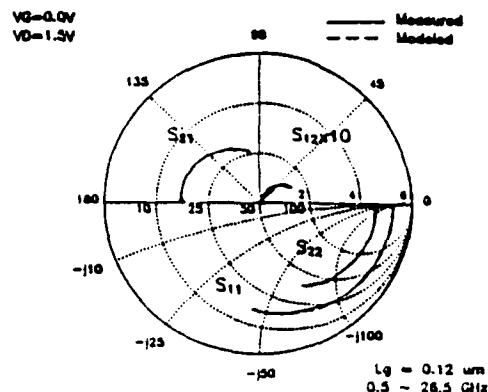


Fig. 8. Plots of measured and modeled S-parameters of a 0.12 x 100 μm MODFET.

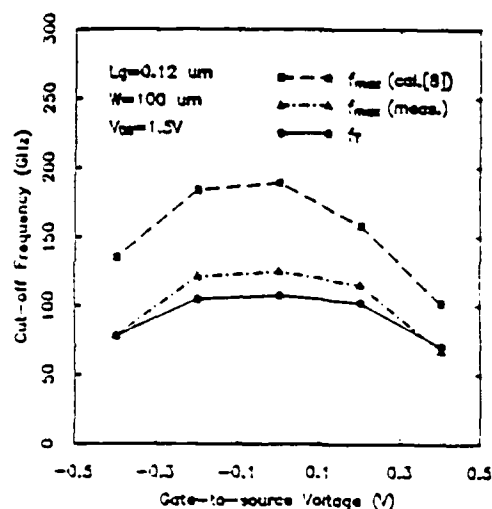


Fig. 9. Gate-bias dependence of f_r , measured f_{max} and calculated intrinsic f_{max} .

Bias Independent Parasitics		Bias Dependent Parameter at $V_{DS} = 1.5V$		
			$V_{GS} = 0V$	$V_{GS} = -0.4V$
L_g	39.57 pH	$R_{gg}(\Omega)$	780	1014
L_d	21.08 pH	$R_{dd}(\Omega)$	433	841
L_s	0.98 pH	$R_s(\Omega)$	2.58	3.26
C_g	16.76 FF	$R_i(\Omega)$	8.21	9.76
		$R_d(\Omega)$	12.4	17.63
C_d	22.75 FF	$R_{ds}(\Omega)$	1978	1116
R_g	4.48 Ω	$C_{gs}(fF)$	71.4	57.56
		$C_{ds}(fF)$	16.87	16.30
		$C_{gg}(fF)$	14.07	15.77
		$g_m(mS)$	48.2	28.2
		$\tau(pS)$	0.175	0.198

Table 1. Bias dependent equivalent circuit parameters

Comparisons of Microwave Performance Between Single-Gate and Dual-Gate MODFET's

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Abstract—1.2- μm and 0.3- μm gate length $n^+\text{-GaAs/InGaAs/n^+-AlGaAs}$ double-heterojunction MODFET's have been fabricated with single-gate and dual-gate control electrodes. Extrinsic dc transconductance of 500 mS/mm has been achieved from a 0.3- μm single-gate MODFET. The device also has an f_T of 43 GHz and 14-dB maximum stable gain (MSG) at 26 GHz with the stability factor k as low as 0.6 from the microwave S -parameter measurements. At low frequency, dual-gate MODFET's demonstrate higher gain than the single-gate MODFET's. However, the stability factor of dual-gate MODFET's reach unity at a faster rate. Power gain roll-off slopes of -3 , -6 , and -12 dB/octave have been observed for the dual-gate MODFET's.

I. INTRODUCTION

GaAs dual-gate MESFET's play very important roles in various high-performance microwave circuits such as variable gain control stages for both low noise and power amplifiers [1], active phase shifters [2], and mixers [3]. The advantage of the dual-gate structure comes from the added functionalities obtained by integrating two independent FET's in a compact manner. Compared to the single-gate FET, a dual-gate FET of the same gate length provides the same input impedance with higher output impedance, higher RF power gain, and much reduced feedback parasitics [4]–[6].

Single-gate MODFET's have demonstrated excellent microwave performance with lower noise and higher cutoff frequency than GaAs MESFET's [7]. However, the dual-gate MODFET has not been studied widely for microwave circuit applications. In this paper, we report the fabrication and characterization of single-gate and dual-gate MODFET's on the same wafer. Their dc and microwave performances are also compared and analyzed.

II. LAYER STRUCTURE AND DEVICE FABRICATION

The pseudomorphic double-heterojunction structure is grown by MBE on top of a semi-insulating LEC substrate in the following sequence: 5000 Å of superlattice buffer layer, 50-Å undoped GaAs, silicon doping plane with a density of $2 \times 10^{12} \text{ cm}^{-2}$, 85-Å undoped GaAs, 200-Å undoped InGaAs channel, 30-Å undoped AlGaAs spacer, silicon doping plane of $6 \times 10^{12} \text{ cm}^{-2}$, 250-Å undoped AlGaAs, and 400-Å GaAs capping layer with a silicon doping density of $1 \times 10^{18} \text{ cm}^{-3}$. The mole fractions of aluminum and indium are 30 and 15 percent, respectively. The superlattice buffer in this

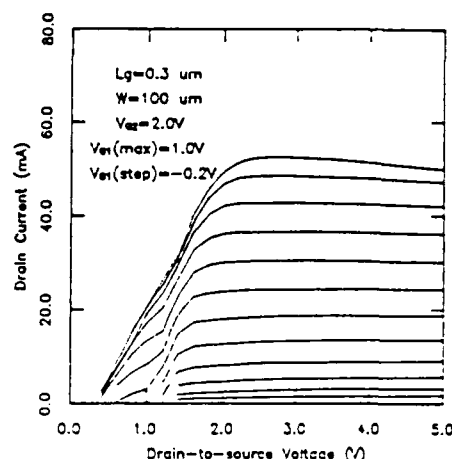


Fig. 1. Drain current-voltage characteristics of a $0.3 \times 100\text{-}\mu\text{m}$ dual-gate MODFET with $V_{g2} = 2.0 \text{ V}$.

structure has been found to be very effective in reducing the short-channel effects [8].

The grown layers were then fabricated with a conventional recess-gate FET process: mesa etch, Ni/AuGe/Ag/Au ohmic contact alloyed at 450°C for 10 s, gate level lithography, recess etch of the capping layer, and Ti/Pd/Au gate metallization. A specific ohmic contact resistance R_c of $0.05 \Omega\cdot\text{mm}$ was obtained from the transmission line measurements. The gate lithography was performed by using either a mid-UV contact aligner for 1.2- μm gate length or electron beam direct writing for 0.3- μm gate length. A PMMA/P (MMA-MAA)/PMMA triple-layer resist system has been developed to reduce the resistance of submicrometer gates [9]. The gate₁-to-source, gate₂-to-drain, and gate₁-to-gate₂ spacings are 0.75, 0.75 and 2.5 μm , respectively. The large separation between two control gates is necessary to reduce the proximity effect in the electron beam lithography.

III. DC CHARACTERISTICS

Fig. 1 shows the dc drain I - V characteristics of a $0.3 \times 100\text{-}\mu\text{m}$ dual-gate MODFET with the second gate biased at 2 V. It shows a very good dc output conductance, similar to dual-gate MESFET's [5]. When the drain is biased below 1.3 V, the forward conduction current through the second gate causes abnormal behaviors in the I - V characteristics. The dependence of dc transconductance g_m and drain current I_d on V_{g1} and V_{g2} with the drain biased at 4 V is shown in Fig. 2. The envelope of the g_m curves corresponds to the g_m versus V_g curve of a single-gate MODFET. g_m of the dual-gate

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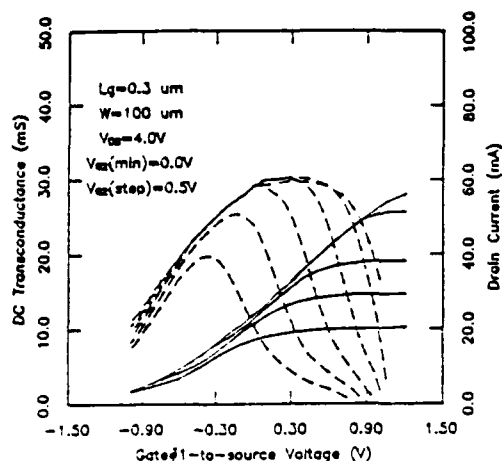


Fig. 2. Dependence of dc transconductance and drain current on V_{g1} and V_{g2} of a $0.3 \times 100\text{-}\mu\text{m}$ dual-gate MODFET with $V_g = 4\text{ V}$.

MODFET increases as the bias of the second gate becomes more positive. g_m can be approximated as

$$g_m = g_{m1} \left(1 - \frac{1}{1 + g_{m2} R_{ds2} + R_{ds1}/R_{ds2}} \right) \quad (1)$$

from the equivalent circuit model [5], where g_{m1} , g_{m2} , R_{ds1} , and R_{ds2} are the transconductances and output resistances of the FET1 and FET2. From (1), g_m of the dual-gate MODFET is always lower than that of the corresponding single-gate MODFET. A peak g_m of 303 mS/mm and a full channel current of 535 mA/mm are obtained from a $0.3 \times 100\text{-}\mu\text{m}$ dual-gate MODFET while the single-gate MODFET shows a peak g_m of 500 mS/mm. To obtain a precise current-voltage relation, $I_d(V_{g1}, V_{g2}, V_{ds})$, a computer program is usually required [5].

IV. MICROWAVE PERFORMANCE

S-parameters from a $0.3\text{-}\mu\text{m}$ dual-gate MODFET are plotted in Fig. 3 together with those from a single-gate MODFET on the same wafer. The S-parameter measurements were performed from 0.5 to 26.5 GHz with microwave wafer probes. The second gate of the dual-gate MODFET is RF terminated by a $50\text{-}\Omega$ load for broad-band two-port characterization. This avoids the potential instability of the device over the whole measuring frequency range. It shows almost identical S_{11} curves because the input impedance is dominated by the first gate. The magnitude of the S_{12} curve of dual-gate MODFET's is reduced dramatically from those of single-gate MODFET's because of good isolation between input and output by the second gate. The magnitude of S_{21} curves of dual-gate MODFET's is higher because of improved overall output impedance. Greater phase shift of S_{21} is introduced by the extra delay from the second FET. Improved output impedance causes the S_{22} of dual-gate MODFET to shift toward the infinite resistance circle of the Smith chart. The output resistance of a dual-gate MODFET at low frequency can be derived as

$$R_{ds} = R_{ds1} + R_{ds2} + g_{m2} R_{ds1} R_{ds2}. \quad (2)$$

Maximum stable gain (MSG), maximum available gain

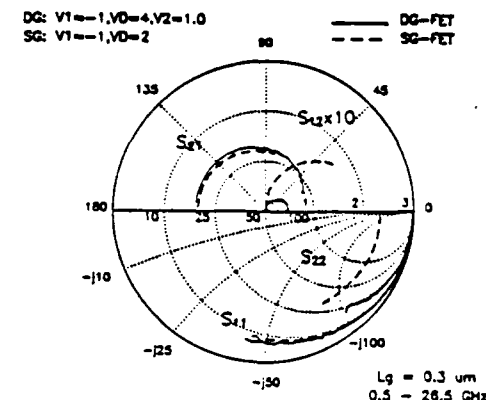


Fig. 3. Measured S parameters from dual-gate (DG) and single-gate (SG) MODFET's of $0.3\text{-}\mu\text{m}$ gate length.

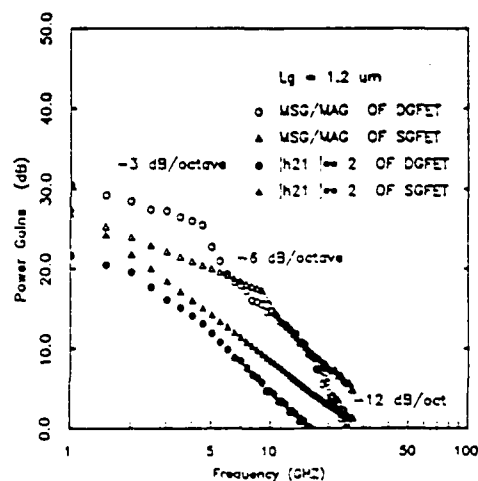


Fig. 4. Power gains versus frequency of single-gate (SG) MODFET and dual-gate (DG) MODFET of $1.2\text{-}\mu\text{m}$ gate length.

(MAG), and short-circuit current gain ($|h_{21}|$) are calculated from S parameters and are depicted in Fig. 4 for both single-gate and dual-gate MODFET's with $1.2\text{-}\mu\text{m}$ gate length. Current gain cutoff frequency f_T as high as 21.5 GHz and an MAG cutoff frequency f_{MAG} of 57 GHz can be extrapolated from the $1.2\text{-}\mu\text{m}$ single-gate MODFET. At frequencies below 5 GHz, the stability factor k of the dual-gate MODFET is less than unity and the MSG is higher than the single-gate MODFET and is decreasing with a -3 dB/octave slope. Moreover, the dual-gate MODFET is stable above 5 GHz with the MAG decreasing with -6 dB/octave slope until 12 GHz. The MAG slope switches to -12 dB/octave above 12 GHz. The k factor of the single-gate MODFET becomes greater than unity at 9 GHz, and then the MAG decreases with a -6 dB/octave slope. In short, the dual-gate MODFET is more stable and provides higher gain than the single-gate MODFET over the frequency range from 5 to 19 GHz. This feature makes dual-gate MODFET's very useful for applications from low frequency up to f_T . The dual-gate MODFET with $0.3\text{-}\mu\text{m}$ gate length exhibits the same frequency dependence of power gains as shown in Fig. 5. Because of the improved performance from shorter gate length, the frequency for unity k factor is displaced to higher frequency. As a result, the -12 dB/

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INFLUENCE OF SUBSTRATE MISORIENTATION ON DEFECT AND IMPURITY
INCORPORATION IN GAAS/ALGAAS HETEROSTRUCTURES GROWN BY MOLECULAR
BEAM EPITAXY

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ABSTRACT

GaAs/AlGaAs heterostructures have been grown by molecular beam epitaxy on GaAs substrates intentionally oriented (tilted) a few degrees (0 to 6.5) off the (001) plane towards either (111)A, (111)B or (011). We observe that the 4K photoluminescence and low-field electron transport properties of these structures may be functions of the substrate tilt angle and tilt direction depending on the concentration of impurities incorporated during growth. A substrate tilt during molecular beam epitaxy is observed to have the largest effect on these properties when the background impurity concentration in the molecular beam epitaxial machine is high. This supports our contention that the observed changes in material characteristics are due to differences in incorporation of defects and impurities. The incorporation of defects and impurities are reduced by using substrates tilted toward (111)A in comparison to nominally flat (001) substrates or substrates tilted toward (111)B.

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I. INTRODUCTION

The substrate misorientation from nominally (001) during molecular beam epitaxy (MBE) has recently emerged as an MBE growth parameter which can play an important role in determining the quality of AlGaAs/GaAs heterostructures.¹⁻⁵ It has been shown that the morphological, optical, and electron transport properties of these structures can be improved if they are grown under specific conditions on GaAs substrates which are intentionally misoriented (tilted) from nominally (001) in a correct manner.¹⁻⁵ However, the role of the misorientation in reducing the defect and impurity concentrations in these structures, in addition to the identification of the defects and impurities which are effected by a substrate misorientation during MBE has not yet been investigated.

The effects of substrate misorientation and background impurities on the two dimensional electron gas (2DEG) transport properties of AlGaAs/GaAs modulation-doped quantum-well structure have been investigated.⁵ In general, (001) substrates tilted in the (111)A direction during MBE growth improves the quality of GaAs grown on top of AlGaAs (inverted interface) and consequently improves the 2DEG transport properties of modulation-doped quantum-well structures. An anisotropy in the 2DEG mobility^{5,6} was observed and attributed to interface scattering at the inverted interface. The 2DEG mobility was observed to be highest with the carrier transport in the [110] direction and lowest in the $\bar{1}10$ direction, while intermediate directions had intermediate mobilities. The degree of anisotropy was related to the thickness and growth parameters of the AlGaAs layer grown just prior to the inverted interface, to the misorientation of the substrate from nominally (001) and to the background impurity concentration in the MBE machine. It was suggested that impurities and/or defects introduced during MBE growth of AlGaAs are the origin of the anisotropy in electron transport.

In this paper we use 4K photoluminescence (PL) to investigate the influence of an intentional substrate misorientation on defect and impurity incorporation in AlGaAs/GaAs heterostructures. 77K Hall effect measurements on the structures reported in this paper have been previously published.⁵ These 77K Hall effect measurements in conjunction with the present PL data clearly shows that there is a preferential incorporation of impurities/defects which form complexes during MBE growth of AlGaAs. These complexes are observed to give rise to the anisotropic 2DEG transport previously reported.⁵ The concentrations of these complexes are observed to be a function of the substrate angle and tilt direction in addition to the background impurity concentration in the MBE machine. We suggest that a primary effect of substrate misorientation during MBE growth of AlGaAs is to alter the concentration of impurity/defect-related complexes.

II. EXPERIMENTAL

The epitaxial layers were grown by MBE in a Varian GEN II machine on undoped liquid encapsulated Czochralski (LEC) grown GaAs substrates. The substrates were cut either 0, 2, 4 or 6.5 degrees $\pm$ 0.25 degrees off the (001) plane towards either (111)A (gallium face), (111)B (arsenic face) or (011). For each growth run three to five substrates with different orientations were mounted side by side, using indium, on a molybdenum mounting block. The substrates were rotated during growth at 7 revolutions per minute. The substrate temperature during growth was 620 degrees C and the growth rate of GaAs was $\sim 1.0 \mu\text{m/hr}$. The aluminium mole fraction for all structures was ~ 0.3 . The surface reconstruction determined by electron diffraction during growth of GaAs was an arsenic-stabilized $c(2 \times 8)$ mesh. The V/III beam equivalent pressure ratio determined by an ion gauge in the growth position was 7 to 10. The same arsenic flux (As_4) was used for both the GaAs and AlGaAs growth.

The superlattice-buffered modulation-doped quantum-well structure shown in Figure 1, was used for this study. The GaAs buffer is followed by a 500 Å graded composition $\text{Al}_x\text{Ga}_{1-x}\text{As}$ region ($0 < x < 0.3$) to minimize the contributions of an unintentional 2DEG at this interface in the transport measurements. The thickness of the GaAs in the superlattice buffer, L_{SSL} , was either 5 or 15 Å. A quantum well of 150 Å thickness was chosen for this work so that the wave function of the electrons in the 2DEG would strongly interact with the inverted interface and be very sensitive to the quality of it.⁶ A 75 Å undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ spacer was followed by an atomic planar doped electron supplying layer. During the silicon deposition for the atomic planar doping, growth was suspended for 45 seconds with only silicon and arsenic impinging on the substrate to accumulate 6×10^{12} silicon atoms per square centimeter.

The 2DEG 77K mobility in a single heterojunction wide (200 Å) spacer AlGaAs/GaAs modulation doped structure was used as a measure of the MBE machine residual background impurity concentration.⁷ A mobility of $< 100,000$ $\text{cm}^2/\text{V-s}$ is considered low, and is indicative of a high level of residual impurities. Mobilities of 100,000 to 150,000 are intermediate and indicative of a moderate level of residual impurities and mobilities in excess of 150,000 $\text{cm}^2/\text{V-s}$ are obtained when the system is relatively clean.

Growth runs LP1, LP2, and LP3 were performed when the maximum 2DEG 77K mobility which could be achieved in the MBE machine in single heterojunction, wide spacer (200 Å), AlGaAs/GaAs modulation doped structures was only $\sim 95,000$ $\text{cm}^2/\text{V-s}$. During the time the growth of HP1 was performed, mobilities in excess of 200,000 $\text{cm}^2/\text{V-s}$ could be obtained in the MBE machine. During growth run LP3 the flow of liquid nitrogen into the growth chamber liquid nitrogen shrouds was intentionally reduced such that it was insufficient to keep the shrouds at 77K. The purpose of this was to enhance the impurity effect by intentionally increasing

the background impurity concentration in the MBE machine. Growth runs LP1, LP2 and LP3 are considered to be "low purity" growths, while growth run HP1 is considered to be a "high purity" growth. Table I summarizes the growth runs presented in this study.

Photoluminescence measurements were performed at 4K using the 6328Å line from a He-Ne laser with an excitation power of 0.5 W/cm² and a spectral resolution of better than 0.1 meV. Care was taken to ensure that PL intensity comparisons could be made between structures of various orientations for a given growth run. Van der Pauw-Hall measurements were made using cloverleaf patterns and a square active area with edges aligned along the <110> cleavage directions. These measurements were made in the dark at liquid nitrogen temperature in a magnetic field of 2kG.

III. RESULTS

Figure 2 shows 4K PL in the spectral region of the AlGaAs bandgap as a function of substrate tilt angle towards (111)A for growth run LP1. Growth run LP1 has a superlattice buffer composed of 5Å of GaAs and 200Å of AlGaAs. The PL is from the AlGaAs in the superlattice buffer. The shape of the PL spectra is observed to be dependent on the substrate tilt angle. The broad PL emission band far below the band edge at ~ 1.85 eV for the nominally flat (001) substrate is attributed to a defect/impurity-related complex.^{8,9} This band is observed to vanish at a substrate tilt of 4 or more degrees. This type of PL will be the only feature in the PL spectra from the various growth runs which will be discussed/characterized in this paper. 77K Hall data determined using the van der Pauw method^{5,10,11} are also included in the figure. Since the mobilities are anisotropic we define a geometric mean mobility $\sqrt{\mu_{[110]} \cdot \mu_{[\bar{1}\bar{1}0]}}$ and a mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) to characterize the conduction in anisotropic systems. As seen in the figure since the mobility ratio is not equal to unity, the 2DEG

transport is observed to be anisotropic.^{5,6} The anisotropy also decreases as the substrate tilt angle increases. We also note that lower 2DEG mobilities are always observed in films that exhibit broad defect/impurity - related PL. The data of Figure 2 show that the broad PL disappears as the substrate is tilted a few degrees off (001) towards (111)A, a corresponding increase in 2DEG mobility is also observed.

Figure 3 shows the 4K PL spectra of the GaAs multiple quantum wells in the superlattice buffer of growth run LP2. The superlattices in growth run LP2 have 15Å of GaAs wells compared to the 5Å wells in growth run LP1. The substrates were cut 2 degrees off the (001) plane towards the (111)A, (111)B and (011) directions. We observe that the multiple quantum well PL is a function of the substrate tilt direction. The broad luminescence between 1.72 eV and 1.79 eV is attributed to the same defect/impurity-related complex observed in growth run LP1. The incorporation of these states progressively increases as the substrate tilt direction changes from (111)A to (011) to (111)B. The PL intensity from the superlattice buffer grown on a substrate tilted toward (111)A is a factor of 3 larger than for that grown on a substrate tilted towards the (111)B direction. The Hall data indicates that the 2DEG mobilities are also higher for layers grown on substrates tilted towards (111)A rather than towards (011) or (111)B, consistent with less impurity/defect luminescence seen in the PL data. The fact that the mobilities in Figure 3 are higher and more isotropic than the mobilities in Figure 2 is related to the thickness of the GaAs wells in the different superlattices.^{5,6}

Growth runs LP1 and LP2 show the influence of the substrate tilt angle and tilt direction, respectively on defect/impurity incorporation. Growth runs HP1 and LP3, to be discussed below, show the influence of a low and high background impurity concentration in the MBE machine, respectively, on the effect of a substrate tilt during MBE growth. The 4K PL spectra from the superlattice buffer of layers

grown when the machine impurity level was low are shown in Figure 4 for growth run HP1. The layer structure is identical to that of growth run LP2. The only difference between LP2 and HP1 is the level of residual impurities in the MBE machine at the time that the growths took place. Run HP1 was grown when the machine background impurity level was low and consequently the layers are expected to be of higher quality than those of run LP2. The broad defect/impurity-related PL which was observed in LP2 is non-existent in HP1. The data show that substrate misorientation for growth run HP1 had only minor effects on the emitted quantum well PL. As a result, the data from growth runs LP2 and HP1 indicate that "broad" PL comes from defect/impurity states and that impurity incorporation during MBE does depend on substrate orientation. The Hall data in Figure 4 indicates that the mobilities are significantly higher than in growth run LP2 (Figure 3) indicating that the material is of higher purity. In addition, no anisotropy in 2DEG transport is seen. The data also indicates that there is only a slight dependence of 2DEG mobility on substrate orientation, consistent with the PL data.

From the above data, it is clear that impurities are needed to produce the defect/impurity related PL, the decrease in 2DEG mobilities and the anisotropy in the 2DEG mobilities. In an attempt to enhance this effect growth run LP3 was performed with the growth chamber liquid nitrogen shrouds not fully cooled (>77 K) thereby intentionally increasing the background impurity concentration in the MBE machine. The structure for the LP3 layers is identical to that of LP2 and HP1. The 4 K PL spectra as a function of substrate tilt angle towards (111)A is shown in Figure 5. The defect/impurity-related PL at ~ 100 meV below the band edge is observed in all of the spectra. The relative luminescence intensity of this PL peak, however, still decreases with increasing substrate tilt angle. The impurity incorporation throughout the layers is however, over-shadowing the effects of

substrate misorientation, but the tendency toward less impurity incorporation with increasing tilt angle toward the (111)A direction is still evident in the PL and in the transport data. The 77K Hall data in Figure 5 shows an order of magnitude reduction in the 77K mobilities from that of layers in HP1. Note, however, that significantly larger mobility anisotropies exist than previously observed, further confirming that impurities and/or defects introduced during MBE growth are the origin of the anisotropic transport.

IV. DISCUSSION

Growth runs LP1 and LP2 show the influence of the substrate tilt angle and tilt direction, respectively, on defect/impurity incorporation in our AlGaAs/GaAs structures. In addition, growth runs HP1 and LP3 show the influence of a low and high background impurity concentration, respectively, on the effect of a substrate tilt during MBE growth. The major effect of substrate misorientation during MBE growth on the optical properties of AlGaAs/GaAs heterostructures is that the broad defect/impurity related PL emission far below the band edge is a function of the substrate tilt angle and tilt direction. A careful comparison of the magnitude of this emission peak with the magnitude of the mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) for all growth runs indicates that whenever the anisotropy is large, the PL height of this broad peak is also large. This trend is illustrated in Figure 6 which plots the height of the defect/impurity-related PL peak versus mobility ratio, $\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$ for growth runs LP1, LP2 and LP3. The main point of Figure 6 is to show that for a given growth run the mobilities become more anisotropic as the height of the defect/impurity-related PL becomes larger. As a result, it is very probable that the defect/impurity which gives rise to the mobility anisotropy is the same defect/impurity which gives rise to the defect/impurity related PL. It is reasonable to conclude that the defect/impurity related PL is likely related to a "complex" since an isolated point defect or impurity even at high concentrations would not

exhibit such a broad PL spectrum. In addition, the electric field distribution around a point defect is spherical whereas that around a defect/impurity complex would be elongated and as a result an anisotropic electron scattering cross section would be expected. Since the 2DEG mobilities are always greater in the $[110]$ direction in comparison to the $[\bar{1}10]$ direction, the defect complex would have to be elongated in the $[110]$ direction. It is interesting to note that "defect pairs" preferentially aligned parallel to this same $[110]$ direction have been used to explain the observation of polarized PL from undoped MBE grown GaAs.¹²

The observations cited in this paper are summarized below:

- 1) Broad defect/impurity-related PL, low 2DEG mobilities, and mobility anisotropy are only observed when impurities are present during the MBE growth of the layers.
- 2) The incorporation of defects/impurities decreases using (001) substrates tilted towards the (111)A direction and increases using (001) substrates tilted towards the (111)B direction. For tilt directions between the (111)A and (111)B, such as the (011) direction, the defect/impurity incorporation is intermediate between these two.
- 3) The observed anisotropy and defect/impurity-related PL is growth temperature dependant and disappears at growth temperatures greater than 680°C in the growth of AlGaAs.^{6,13}

To explain these results we postulate that tilting the substrate towards the (111)B direction exposes surface sites which have a high affinity for defect/impurity incorporation. Tilting towards the (111)A reduces these sites. The sites appear to incorporate complexes which are uniformly aligned to give anisotropic electron scattering centers. Because of the correlation between the magnitude of the broad defect/impurity related PL and anisotropic electron mobilities seen in Figure 6 it is reasonable to conclude that the defect/impurity-related PL is

likely due to a "complex". The suggestion that the broad PL emission far below the band edge is related to a defect/impurity complex is consistent with the observation of other authors. Mihara et. al.^{8,9} have systematically studied the effects of aluminium mole fraction, growth temperature and V/III flux ratio on the PL properties of MBE grown AlGaAs grown on nominally flat (001) substrates. They have suggested that the defect/impurity complex is closely related to a carbon impurity paired with some other type of defect or impurity. They have studied the defect/impurity complex emission as a function of aluminium mole fraction and have pointed out that the emission occurs in the 1.471 eV to 1.491 eV spectral region for GaAs. Briones and Collins¹⁴ have observed that the defect/impurity complex band in GaAs can be resolved into nine distinct peaks. They have suggested that the defect/impurity complex band is related to carbon impurities paired with some other impurity or defect. Of the nine distinct peaks in the defect/impurity complex band some complexes were attributed to a carbon impurity paired with an arsenic vacancy while others were attributed to a carbon impurity paired with a gallium vacancy.

The improvement of the quality of MBE grown AlGaAs on (001) substrates tilted towards the (111)A direction has previously been reported.¹⁻⁴ In general, it was found that the PL spectra and surface morphology are degraded when AlGaAs is grown on nominal (001) GaAs particularly at low growth temperature and high As_4 flux. Some improvement in AlGaAs quality was observed as the substrate temperature was increased and as the As_4 flux was lowered but the major improvement occurred on the tilted substrates. The critical angle of misorientation which produced the smoothest morphology was 6 degrees off (001) towards (111)A. In the study of the effect of tilt angle on the mobility of the 2DEG in modulation-doped structures⁵ an optimum tilt angle of about 4 degrees towards

(111)A was observed. The optimum substrate angle for growth, if one indeed exists may depend on growth parameters and environment.⁵

It is tempting to say that the migration length of Al ad-atoms on the step terraces formed by the tilted substrate plays a significant role in determining the crystal quality. There is no reason to believe that step terraces formed by tilting the (001) substrate towards the (111)A would differ from those of (111)B tilts. The difference lies solely in the step edges. Substrate tilt towards (111)A exposes gallium-type step edges (gallium dangling bonds) while substrate tilt towards (111)B exposes arsenic-type step edges (arsenic dangling bonds).^{15,16} To explain our data the sticking coefficient of impurities to arsenic-type step edges would have to be higher than the sticking coefficient of impurities to gallium-type step edges. The sticking coefficient to nominally flat substrates would have to be intermediate to arsenic-type and gallium-type step edges. Early reports on the growth of GaAs on (111)B GaAs substrates showed poor surface morphology, poor PL and poor electronic transport properties.¹⁷ Wang et. al.¹⁸ have observed that impurity incorporation during MBE growth of GaAs was a function of the surface orientation when comparing (001), (113)A and (113)B surfaces of GaAs. Vina and Wang¹⁹ also recently confirmed that GaAs grown on exactly (111)B oriented substrates (even with $1 \times 10^{18} \text{ cm}^{-3}$ doping) was highly resistive. They however found a significant improvement by tilting the (111)B substrate 2 degrees towards the (001) direction. In addition, Ranke et. al.²⁰ have studied oxygen adsorption on a cylindrical GaAs sample which exposed the main low index orientations (001), (111)A and (111)B as well as their vicinal surfaces. They observe higher oxygen adsorption rates on vicinal surfaces cut off (001) towards (111)B in comparison to vicinal surfaces cut off (001) towards (111)A. They also observe the amount of adsorption to be a function of the angle of tilt (0 to 20 degrees) about (001). It seems clear that dangling bonds and/or vacancies on the (111)B surface are

where the major defect/impurity-related complexes are generated and that these complexes are least generated on (111)A surfaces. Because of the temperature dependance, As_4 flux dependance and tilt angle dependance it would appear that the Al migration also plays a role. The low migration of Al would be expected to create Al vacancies where defect/impurities could be trapped. The molecule CO usually found in MBE growth chambers at detectable levels has a dipole moment which may attract it to the Al vacancy in the highly polar (111)B surface. N_2 also has a strong dipole moment and may be incorporated. It is interesting to note that these molecular defects would be electrically neutral but would create anisotropic stress centers. Clearly more work is required to identify the defect/impurity complexes responsible for the many observed effects.

V. CONCLUSIONS

The effects of substrate misorientation from (001) and background impurities on the PL and electron transport properties of MBE grown AlGaAs/GaAs structures have been investigated. Broad defect/impurity related PL, low 2DEG mobilities and mobility anisotropy are observed only when impurities are present during MBE growth of the layers. The incorporation of these impurities/defects decrease using (001) substrates tilted toward the (111)A direction and increases using (001) substrates tilted toward (111)B direction. For tilt directions between (111)A and (111)B, such as the (011) direction, the impurity/defect incorporation is intermediate between these two. A correlation exists between the magnitude of the broad defect/impurity related PL and anisotropic electron transport suggesting that the PL emission is from a "defect/impurity complex" having an anisotropic electron scattering cross-section and not from isolated point defects. As a practical consideration the data herein clearly indicates that less background impurities will be incorporated on (001) substrates tilted 4 to 6 degrees towards the (111)A direction in comparison to nominally flat (001) substrates.

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Figure Captions

Fig. 1. Layer structure of the superlattice-buffered modulation-doped quantum-well structures grown on misoriented substrates.

Fig. 2. 4K PL spectra as a function of substrate tilt angle towards (111)A for growth run LP1. 77K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[\bar{1}\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) are also shown. The PL is from the 5,000Å thick superlattice (5Å GaAs/200Å AlGaAs) buffer while the transport is in the 150Å quantum-well of a modulation-doped superlattice-buffered quantum-well structure.

Fig. 3. 4K PL spectra as a function of substrate tilt direction for a (001) GaAs substrate cut 2 degrees off the (001) plane for growth run LP2. 77K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[\bar{1}\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) are also shown. The PL is from the 5,000Å thick superlattice buffer (15Å GaAs/200Å AlGaAs) while the transport is in the 150Å quantum-well of a modulation-doped superlattice-buffered quantum-well structure.

Fig. 4. 4K PL spectra as a function of substrate orientation for growth run HP1. 77K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[\bar{1}\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) are also shown. The PL is from the 5,000Å thick superlattice buffer (15Å GaAs/200Å AlGaAs) while the transport is in the 150Å quantum-well of a modulation-doped superlattice-buffered quantum-well structure.

Fig. 5. 4K PL spectra as a function of substrate tilt angle towards (111)A for growth run LP3. 77K geometric mean mobility ($\sqrt{\mu_{[110]}\mu_{[\bar{1}\bar{1}0]}}$) and mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) are also shown. The PL is from the 5,000Å thick superlattice buffer (15Å GaAs/200Å AlGaAs) while the transport is in the 150Å quantum-well of a modulation-doped superlattice-buffered quantum-well structure.

Fig. 6. Defect/impurity-related PL peak height at 4K versus mobility ratio ($\mu_{[110]}/\mu_{[\bar{1}\bar{1}0]}$) at 77K for the growth runs indicated. The PL is from the 5,000Å thick

superlattice buffer while the transport is in the 150Å quantum-well of a modulation-doped superlattice-buffered quantum-well structure.

400 Å	GaAs:Si ($1 \times 10^{18} \text{ cm}^{-3}$)
325 Å	undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$
Silicon Atomic Plane ($6 \times 10^{12} \text{ cm}^{-2}$)	
75 Å	undoped $\text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$ spacer
150 Å	GaAs Quantum Well
5,000 Å Superlattice Buffer ($L_{\text{GSL}} \text{ GaAs} / 200 \text{ Å } \text{Al}_{0.3}\text{Ga}_{0.7}\text{As}$) $L_{\text{GSL}} = 5 \text{ or } 15 \text{ Å}$	
500 Å	Graded $\text{Al}_x\text{Ga}_{1-x}\text{As}$
3,000 Å	GaAs Buffer
GaAs S. I. Substrate (Cut θ off (001), $\theta = 0, 2, 4, \text{ or } 6.5^\circ$)	

Fig. 1

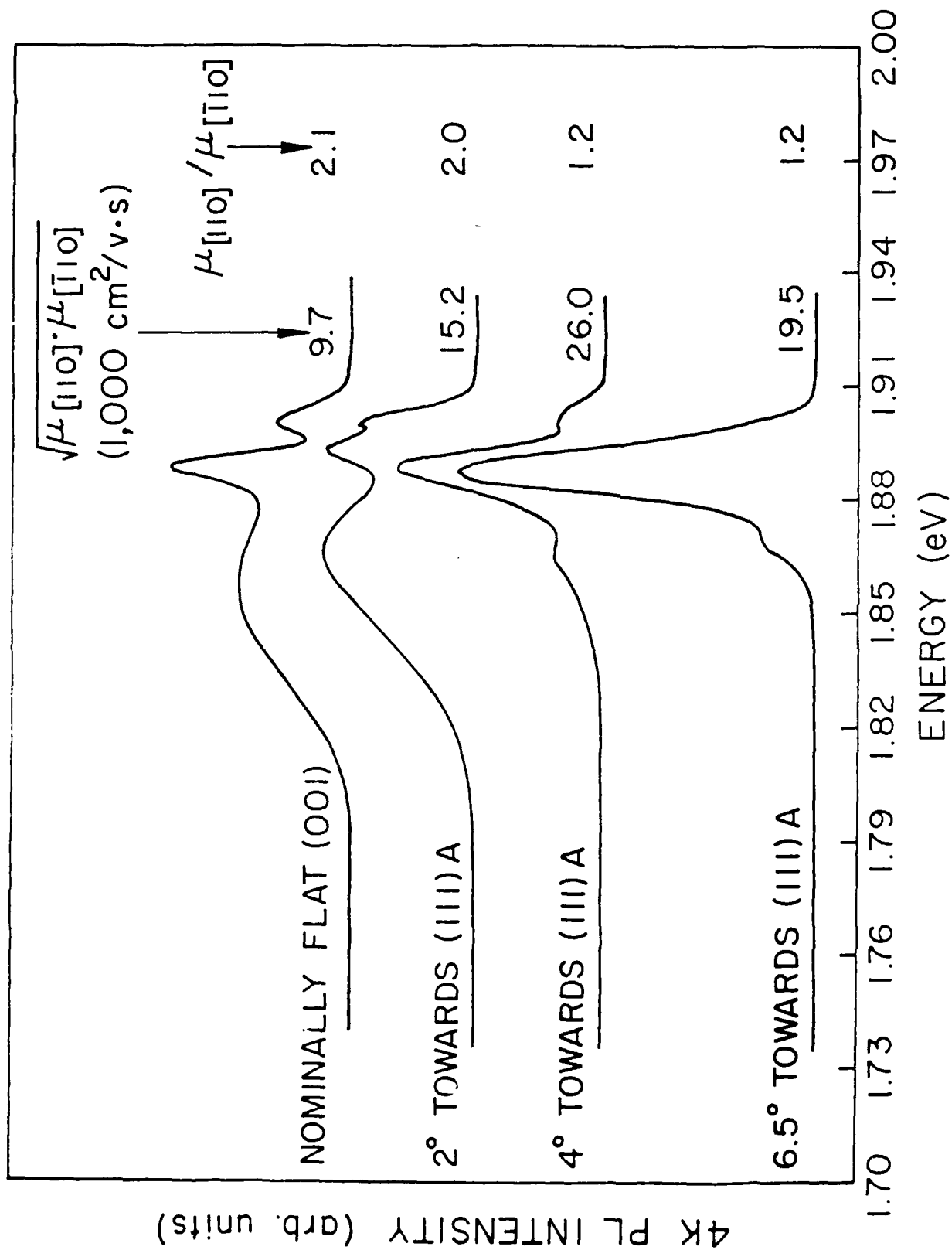


Fig. 2

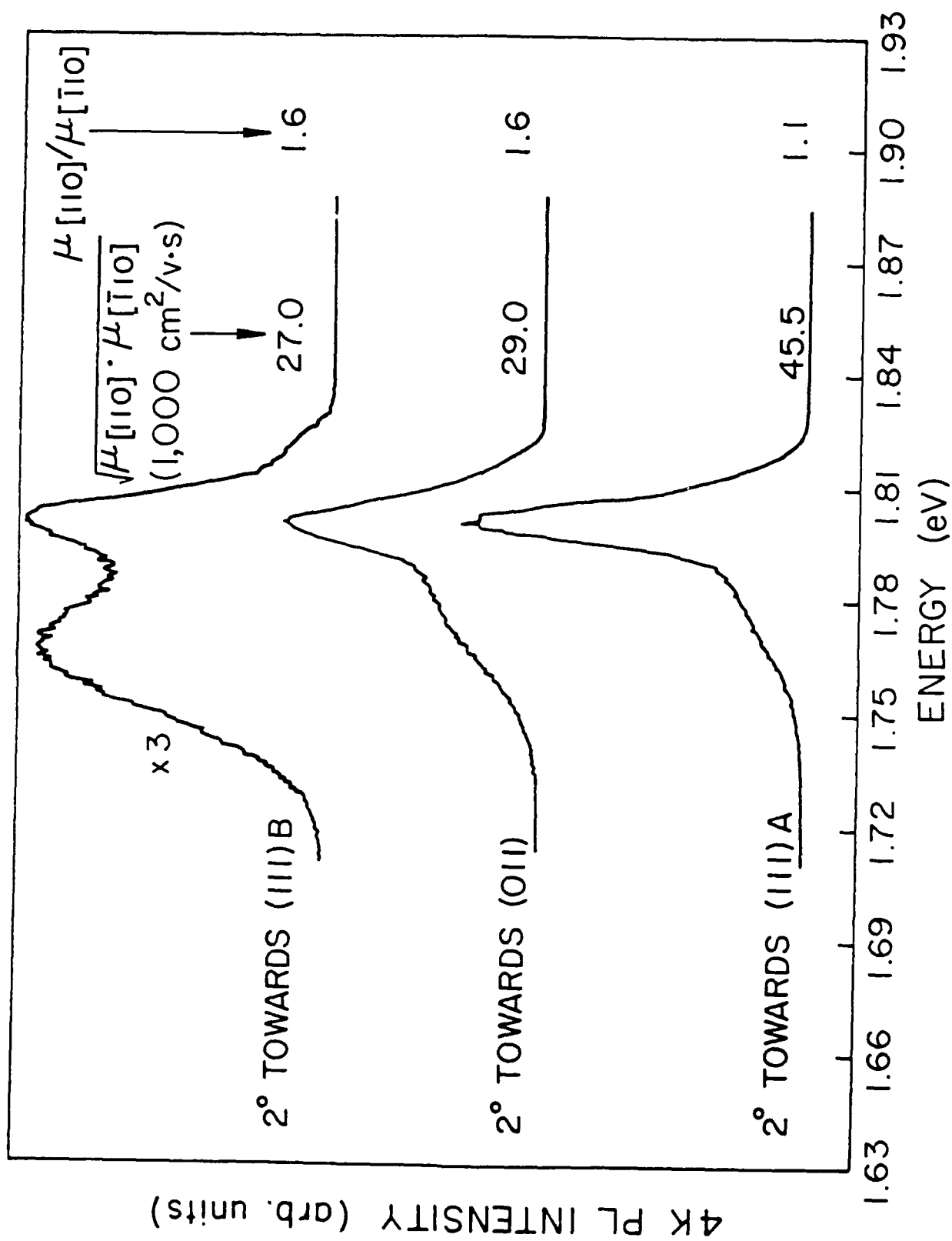


Fig. 3

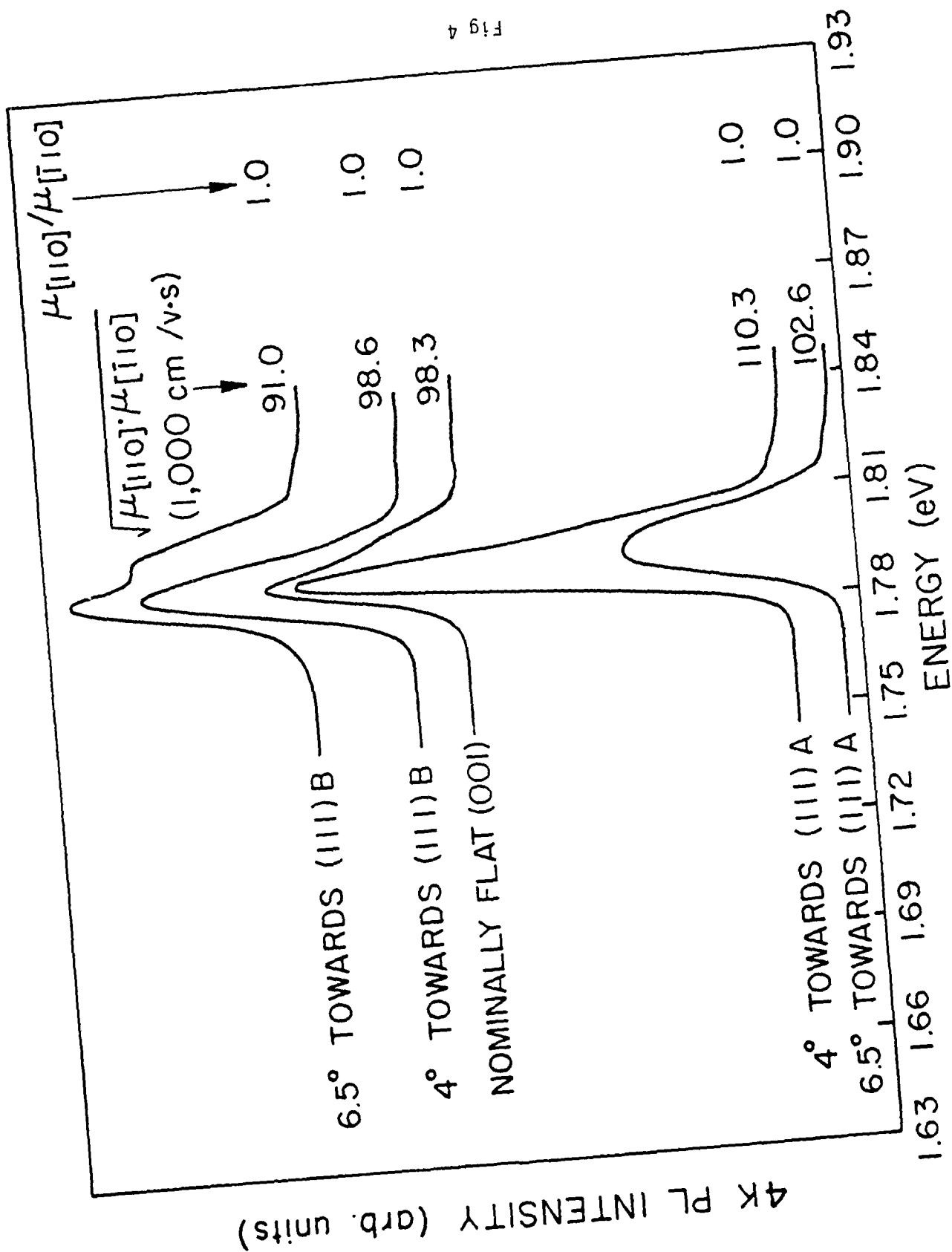


Fig 4

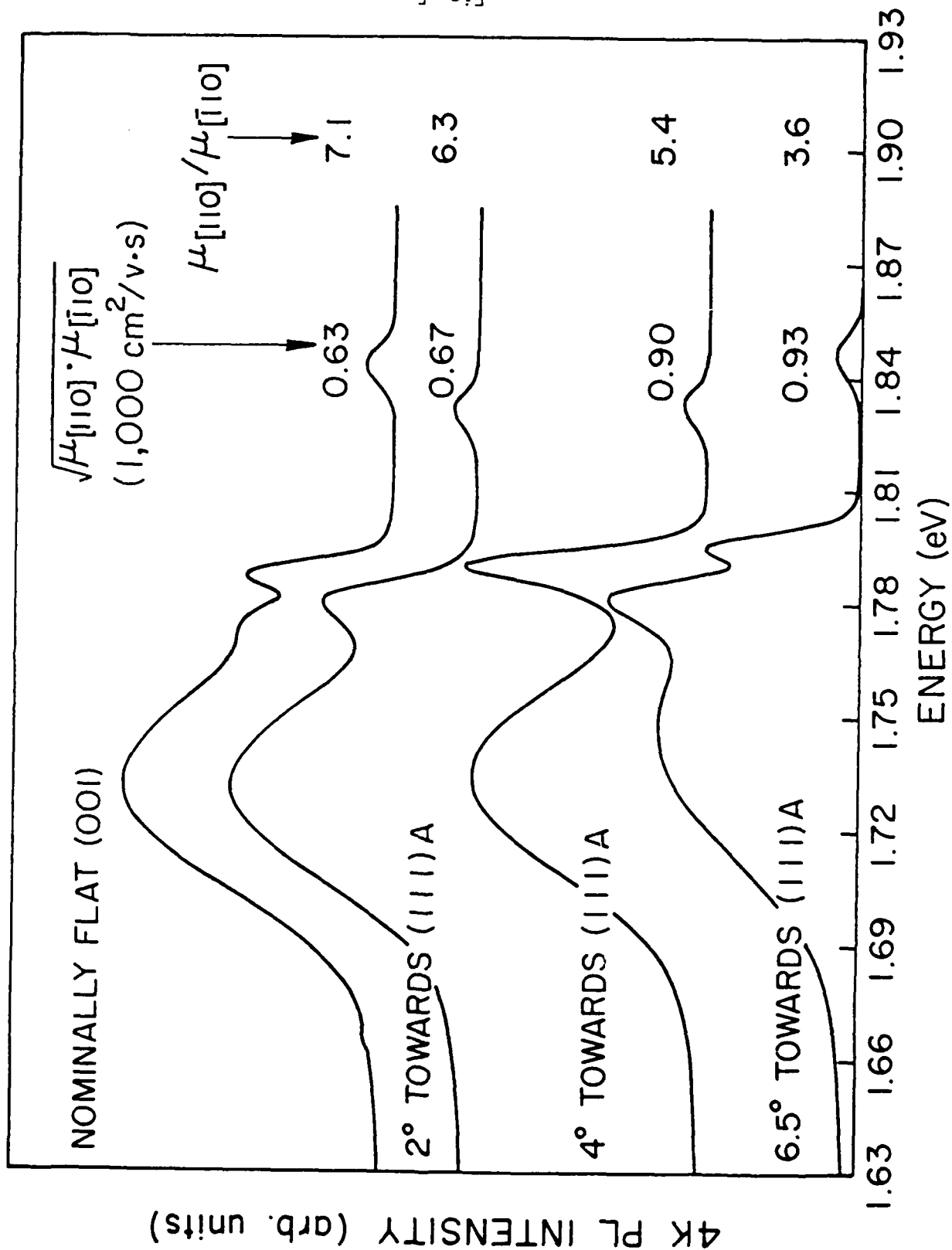


Fig. 5

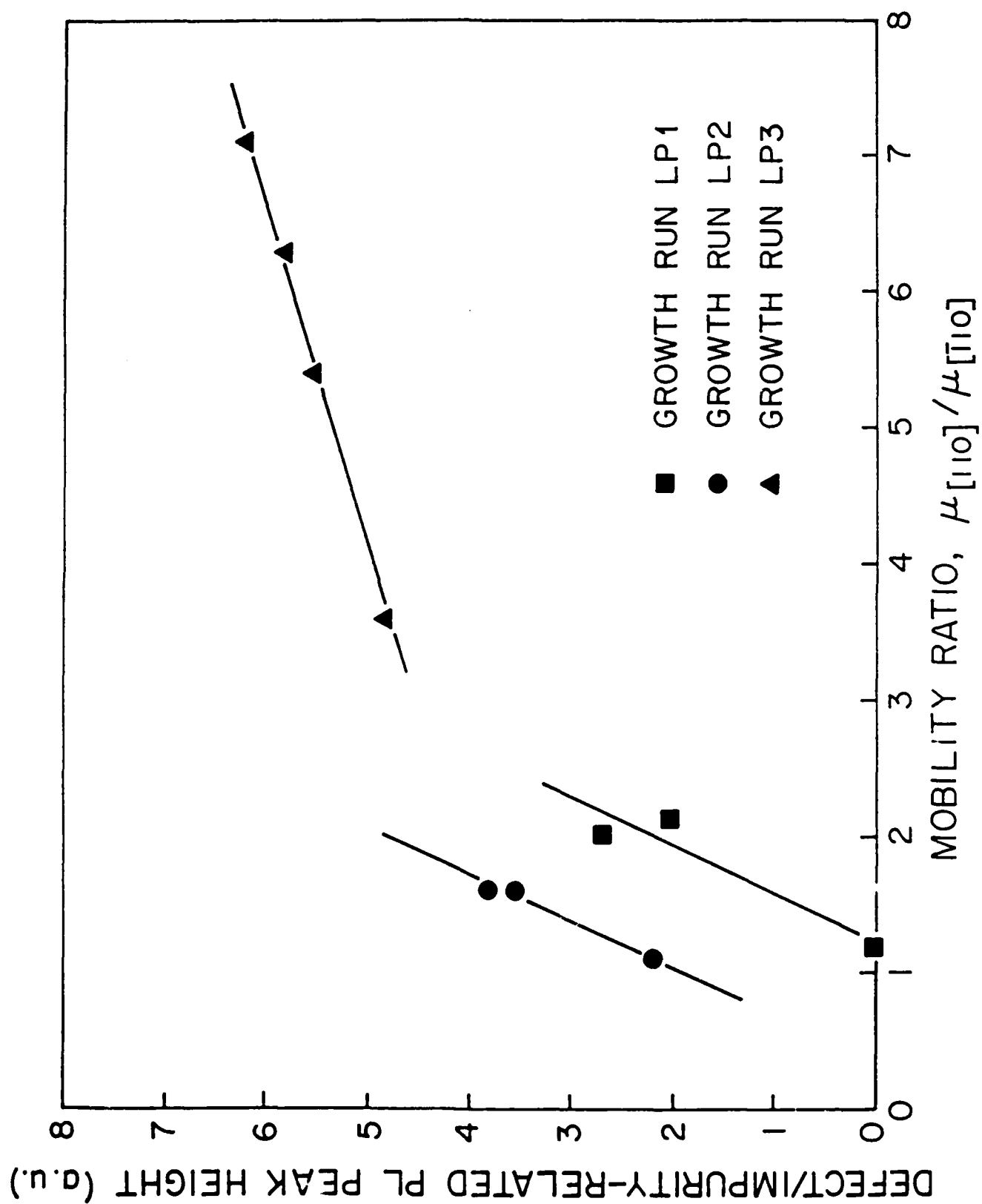


Fig. 6

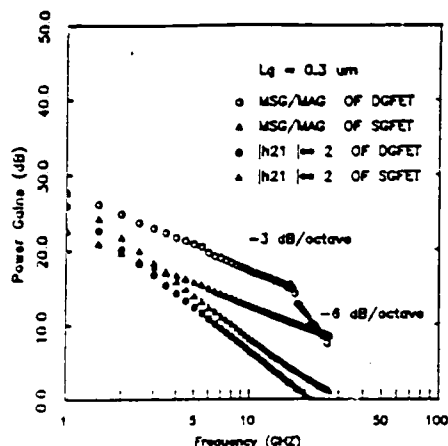


Fig. 5. Power gains versus frequency of single-gate (SG) MODFET and dual-gate (DG) MODFET of 0.3- μ m gate length.

octave slope cannot be observed over the measuring frequency range. Since both f_T and f_{MAG} depend on the gate and drain biases, a peak f_T of 57 GHz and an MSG of 14 dB with k factor equal to 0.6 at 26 GHz were obtained from the 0.3- μ m single-gate MODFET under other bias conditions. An f_{MAG} of 180 GHz can then be extrapolated with a -6 -dB/octave slope.

V. CONCLUSION

Dual-gate MODFET's of either 1.2- or 0.3- μ m gate length have been successfully fabricated and characterized for the first time. Observed power gain slopes for dual-gate MODFET's are -3 dB/octave for MSG at low frequency, -6 dB/octave for MAG at intermediate frequency, and -12 dB/octave at high frequency. Dual-gate MODFET's are more stable and provide higher gain than single-gate MODFET's

over most of the operating frequency range. Dual-gate MODFET's are very promising for millimeter-wave circuit appliances such as gain control blocks, mixers, and active phase shifters.

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