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RELIABILITY ANALYSIS/ASSESSMENT OF ADVANCED TECHNOLOGIES

Westinghouse Electric Corporation

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This report has been prepared to summarize the technical study performed to determine the reliability characteristics of advanced technologies. The study covered existing reliability models and the development of new models. The devices that were investigated were: Very Large Integrated Circuits (VLSI), Memory Circuits, Hybrid Circuits, Microprocessors, and Gallium Arsenide Microwave Monolithic Integrated Circuits (GaAs MMIC). Packaging, environmental quality, and maturity were other factors that were considered in this investigation. The results of the study are: reliability models that extend the range of MIL-HDBK 217, end of life prediction models for in-depth circuit and packaging design and new factors quality assessment. These data will be transitioned from the report to MIL-HDBK 217 for use by government and contractor personnel in estimating the reliability of new equipments.

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1.0 INTRODUCTION

1.1 OBJECTIVES

The main objectives of this study have been: (1) to examine the existing failure rate prediction models in the Microcircuit Section of MIL-HDBK-217E, to determine if they are applicable to state-of-the-art devices; (2) to revise or extrapolate the existing models as necessary to reflect current and future device reliability; (3) to perform a reliability assessment of device types, being designed into state-of-the-art systems, for which no models presently exist; and (4) to develop new reliability prediction models for emerging technology devices. These objectives support the goal of developing accurate, user-friendly models for possible inclusion in a future revision to MIL-HDBK-217.

1.2 BACKGROUND

MIL-HDBK-217 has been used as a guide for predicting system reliability for many years. The consistent approach used by the authors of the handbook (RADC) has been to examine field and life test component failure data to identify key elements to which this data best fits. These key elements are then combined in an additive and multiplicative form to develop a component failure rate value dependent upon the type and application of the specific component. Component failure rate values can be combined, according to the specified system architecture, to obtain a predicted value of the system failure rate. Using this approach, the authors have been successful in maintaining a usable model. However, because of increasing microcircuit complexities and new component types, there is a need for an improved, updated prediction model for advanced microcircuits.

To develop a set of requirements for a reliability prediction model, it is necessary to understand the intended use of the model. Reliability prediction models, such as MIL-HDBK-217E, are used extensively to determine the reliability trade-offs between various system designs, in order to produce the

optimum reliable design. The requirement to deliver systems with higher reliability is being pursued aggressively by DOD. The seriousness with which the Air Force views system reliability is demonstrated in the goals of R&M 2000, with similar initiatives being pursued by the Army and Navy. In order to achieve these goals, it is imperative that the major reliability risks in the system design be accurately identified and eliminated without unnecessary reliability design complications, such as over-redundancy or the use of inappropriate cooling system strategies. The reliability prediction model must be capable of realistically approximating the reliability of each component comprising the system, including the advanced microcircuits. The methods of reliability prediction modeling investigated address the requirements of accuracy of the predicted failure rate, comprehensiveness of microcircuit types, integration with microcircuit screening, and model maintainability, all with minimal impact on usability.

1.3 LIST OF ACRONYMS

A list of acronyms with their associated meanings as used in this report is as follows:

AC - Assignable Cause
Ag - Silver
Al - Aluminum
ALSTTL - Advanced Low-power Schottky Transistor-Transitor Logic
ASIC - Application Specific Integrated Circuit
ASTTL - Advanced Schottky Transistor-Transistor Logic
Au - Gold
B - Boron
BIMOS - Bipolar/Metal Oxide Semiconductor
BIR - Built-in Reliability
CCD - Charge Coupled Device
CERDIP - Ceramic Dual Inline Package
CGA - Configurable Gate Array
CHE - Channel Hot Electron
CI - Charge Injection

Cl - Chlorine

CML - Current-Mode Logic

CMOS - Complementary Metal Oxide Semiconductor

CPU - Central Processing Unit

CVD - Chemical Vapor Deposition

DIP - Dual In-line Package

DOD - Department of Defense

DRAM - Dynamic Random-Access Memory

DTL - Diode-Transistor Logic

Ea - Activation Energy

ECL - Emitter-Coupled Logic

EEPROM - Electrically Eraseable Programmable Read-Only Memory

EM - ElectroMigration

EMI - Electromagnetic Interference

EMP - Electromagnetic Pulse

EPROM - Eraseable Programmable Read-Only Memory

ESD - ElectroStatic Discharge

eV - Electron Volt

F - Fluorine

FET - Field-Effect Transistor

FGMOS - Floating Gate Metal-Oxide Semiconductor

FLOTOX - Floating Gate Tunnel-Oxide

FPMH - Failures Per Million Hours

FR - Failure Rate

FTTL - Fast Transistor-Transistor Logic

GaAs - Gallium Arsenide

Ge - Germanium

H - Hydrogen

HAL - Hard Array Logic

HBT - Heterojunction Bipolar Transistor

HEMT - High-Electron Mobility Transistor

HMOS - High-performance Metal-Oxide Semiconductor

HTRB - High Temperature Reverse Bias burn-in

IC - Integrated Circuit

IEEE - Institute of Electrical and Electronics Engineers

IIL - Integrated Injection Logic

In - Indium

IRPS - International Reliability Physics Symposium

K - Boltzman's constant

K - Potassium

K - Thermal conductivity

KÅ - Kilo Angstroms

LCC - Leadless Chip Carrier

LEFM - Linear Elastic Fracture Mechanics

LSI - Large-Scale Integration (1,001 to 10,000 logic gates)

LSTTL - Low-power Schottky Transistor-Transistor Logic

LTTL - Low-power Transistor-Transistor Logic

MDR - Microcircuit Device Reliability (RAC publicatons)

MESFET - Metal Semiconductor Field-Effect Transistor

MHP - Multichip Hybrid Package

MIL-HDBK - Military Handbook

MIL-STD - Military Standard

MIMIC - Millimeter-wave Monolithic Integrated Circuit

MLA - Masked-Logic Array

MLO - Multi-level Oxide

MMIC - Monolithic Microwave Integrated Circuit

MNOS - Metal-Nitride-Oxide Semiconductor

MOS - Metal-Oxide Semiconductor

MOSFET - Metal-Oxide Semiconductor Field-Effect Transistor

MSI - Medium-Scale Integration (101 to 1,000 logic gates)

MTBF - Mean Time Between Failures

MTTF - Mean Time To Failure

N - Nitrogen

Na - Sodium

NDP - Numerical Data Processor

NMOS - N-channel Metal-Oxide Semiconductor

O - Oxygen

P - Phosphorous

P-DIP - Plastic Dual In-line Package

PAL - Programmable Array Logic

PCB - Printed Circuit Board
PGA - Pin Grid ArrayPLA - Programmable Logic Array
PMOS - P-channel Metal-Oxide Semiconductor
PPM - Parts Per Million
PROM - Programmable Read-Only Memory
PSG - Phosphosilicate Glass
RAAAT - Reliability Analysis/Assessment of Advanced Technologies
RAC - Reliability Analysis Center
RADC - Rome Air Development Center
RAM - Random-Access Memory
RH - Relative Humidity
RMC - Representative Microcircuit Configuration
ROM - Read-Only Memory
SAW - Surface Acoustic Wave
SF - Screening Factor
Si - Silicon
SIA - Semiconductor Industry Association
PHP - Power Hybrid Package
SRAM - Static Random-Access Memory
SSI - Small-Scale Integration (1 to 100 logic gates)
STTL - Schottky Transistor-Transistor Logic
Tch - Channel Temperature
TDDB - Time Dependent Dielectric Breakdown
Tj - Junction Temperature
TTL - Transistor-Transistor Logic
ULSI - Ultra Large-Scale Integration (greater than 100,000 logic gates)
UVEPROM - Ultra-violet Eraseable Programmable Read Only Memory
VHSIC - Very High-Speed Integrated Circuit
VLSI - Very Large-Scale Integration (10,000 to 100,000 logic gates)
WEC - Westinghouse Electric Corporation
WSI - Wafer-Scale Integration

2.0 REPORT ORGANIZATION

Section 3.0 presents the approach which was taken in the conduct of this study

contract. It lists the microcircuit types which were the subject of study, and it summarizes the methodology employed, the types of models which were developed, and their intended usage.

Section 4.0 is the main body of the report. It discusses the model development for each of the primary categories of devices, as listed below:

- VLSI/ULSI Devices (including microprocessors and gate array devices) - Section 4.1
- Memory Devices (including programmable logic devices) - Section 4.2
- Monolithic GaAs Devices (including microwave and digital devices) - Section 4.3
- Hybrid Microcircuits (including all styles of multi-chip hybrids) - Section 4.4
- Packaging Models (including corrosion, cracking, and wire-bond failure models) generic to all packages - Section 4.5

In addition, the development of failure rate adjustment factors (π factors) to account for different quality levels, product maturity, device functions and operating environments, is presented in Section 4.6.

Section 5.0 discusses predictive model validation, where it was possible to validate the models. Section 6.0 presents our conclusions and recommendations for follow-on analysis and study, and section 7.0 is the combined bibliography for the report.

Appendix A is a page-for-page replacement for Section 5.1.2 of MIL-HDBK-217E.

Appendices B and C are, respectively, mathematical derivations and Fortran programs supporting the development of the VLSI/ULSI models.

Appendix D contains tables of probability of sucess and hazard rate at 10,000 operating hours for the predominant wearout failure mechanisms, electromigration and time-dependent dielectric breakdown. Appendix E contains memory devices life test data.

Appendices F, G and H are detailed summaries of the work performed in the development of the deterministic package failure models, presented in the format of technical papers.

Appendix I provides the derivation of ΔT default values to be used for various part usage environments.

3.0 APPROACH

The approach which was pursued in assessing the reliability of advanced technology microcircuits consisted of a five-step process.

1. A review of MIL-HDBK-217 identified the component styles and the device technologies which needed to be addressed. If the validity of the existing model was questionable, or if no model existed, it was added to the list. The following areas were selected for research and analysis:

Application Specific ICs (ASIC)
Very Large-Scale Integration (VLSI)
Ultra Large-Scale Integration (ULSI)
Very High-Speed Integrated Circuits (VHSIC)
Random-Access Memory (RAM)
Read-Only Memory (ROM)
Programmable Read-Only Memory (PROM)
Programmable Array Logic, Logic Array, Hard Array Logic (PAL, PLA, HAL)
Configurable Gate Array (CGA)
Current-Mode Logic (CML)
Pin Grid Array (PGA)
Monolithic Microwave IC, Gallium Arsenide (MMIC, GaAs)
Hybrids (MHP, PHP)
Packaging (Materials, Seals, Die Attach, Wire Bonds, Corrosion)

2. A literature search was conducted to determine if the reliability of these component/technology types had been documented. Emphasis was placed on device failure mechanisms and data relative to failure physics, because it was

intended to develop deterministic models to the maximum extent possible. A partial listing of the references is included in the bibliography and the appendices.

3. Data was collected from several sources, including the Reliability Analysis Center (RAC) Microcircuit database, technical journals, technical periodicals, manufacturers' device data books, and the Westinghouse Failure Analysis and Field Failure databases. In addition, an industry survey was made, by mail and by telephone, of 227 suppliers and users of advanced microelectronic devices. The data was categorized for the primary model development areas, and each of these databases is discussed in the appropriate paragraphs of Section 4.0 of this report.

4. The data was analyzed for applicability to the model development effort.

5. Predictive models were developed, based on the data collected. Where possible, the models were validated by using additional sources of information and/or by comparison of the results with MIL-HDBK-217E.

3.1 METHODOLOGY

Initially, the attempt was made to develop only deterministic models for all of the component types identified for study. However, several pitfalls became evident in this approach. First, the resultant form of the model, a combination of all failure distributions, although inherently accurate and mathematically correct, is not user-friendly. It is not possible to improve model accuracy and comprehensiveness without adversely affecting the model development and use. Second, the resulting model form does not readily lend itself to inclusion in MIL-HDBK-217, which is an ultimate goal. And third, deterministic models cannot account for the early and middle life microcircuit failures - those which typically occur within the useful life of the components, and which appear to occur randomly. Since these failures are of significance to the user of the model, they must be included.

Therefore, the reliability prediction model which was developed for advanced

microcircuits estimates the early, middle, and end-life of these microcircuits. In general, early and middle-life microcircuit failures are "assignable cause" failures. These failures are premature failures whose causes can be "assigned" to specific random defects or events. The early and middle-life failures typically exhibit a substantially greater failure rate than do end-life failures. The end-life failures of microcircuits are "common cause" failures. These failures are material wearout failures whose causes are "common" because of the common materials used in the fabrication of the microcircuits. MIL-HDBK-217E and its predecessors only considered assignable cause failures in the development of prediction models, since common cause failures did not typically occur within the lifetimes of military systems. However, the geometry scaling required to attain the complexity of the advanced microcircuits in question may result in common cause failures that contribute significantly to the overall failure rate of the microcircuits under standard operating conditions.

Much of the prediction modeling effort was dedicated to distinguishing between assignable cause failures and common cause failures. Since the failure models for early, middle and end life are not typically the same, a generic model was developed to combine these individual failure models. This Superposition Model is described in detail in section 4.1.1, but it is also described briefly below.

As previously mentioned, the early and middle-life failures, or "assignable cause" failures, are defect-related, and they can be accurately modeled by a constant (time-independent) failure rate, as was done in MIL-HDBK-217. If there are n independent assignable cause failure mechanisms operating on a component population, then

$$\lambda_{AT} = \sum_{i=1}^{n} \lambda_{Ai}, \qquad (3.1.1)$$

where:

λ_{AT} = the total component failure rate due to assignable causes

λ_{Ai} = the component failure rate due to the ith assignable cause

Further, the reliability of the component, or the probability of its operating without failure for some time, τ, may be expressed as

$$\bar{R} = e^{-\lambda_{AT}\tau} \qquad (3.1.2)$$

However, this model does not account for the end of life (wearout) failure mechanisms, which are typically distributed log-normally - implying non-constant failure rates. Equation 3.1.2 may be expanded to include these failure mechanisms, and thus becomes

$$\bar{R} = e^{-\lambda_{AT}\tau} \times \prod_{i=1}^{m} (1 - F_i(\tau)), \qquad (3.1.3)$$

where:

$F_i(\tau)$ is the time-dependent probability of failure for the ith failure mechanism, and

m is the number of independent wearout mechanisms.

The problems presented by this model are: (1) the non-constant (time dependent) failure rate of the wearout mechanisms, implying that the time in the component's life used to evaluate the reliability will alter the result; and (2) the fact that failure rates of components can no longer be added to derive a total system failure rate. The first problem is overcome if a common time is chosen for comparative analysis of the reliability of all components. Ten thousand operating hours is a common design criteria for avionics systems (programs such as ALQ-165 and APG-68), and it has been chosen in our modeling effort. A failure rate for each wearout mechanism can then be calculated, as described in section 4.1. The second problem is overcome by using reliability, rather than failure rate, as the figure of merit, or by ignoring the common causes (by reverting to use of equation 3.1.2). The latter may be done legitimately if the calculated value of the effective failure rate of the common cause failure mechanisms is much less than the failure rate due to

assignable causes. Even then, the common cause models are useful as design tools, both in the assessment of inherent reliability (failure free operating period) and in the verification of adequate derating margins.

3.2 MODELS

Models have been developed for the primary categories of advanced technology devices as shown in Table 3.2-1.

Table 3.2-1 NEW MICROCIRCUIT MODELS

DEVICE CATEGORY	ASSIGNABLE CAUSE[1] (EARLY-MIDDLE-LIFE)	COMMON CAUSE (END-LIFE/WEAROUT)	REMARKS
VLSI/ULSI	E	N	E = extrapolated or modified 217 model based on new data
Memories	E	N	N = new model
GaAs	N	-	Insufficient data for commone cause model development
Hybrids	N	N	Common causes addressed in chip, package models
Packages	E	N	

[1] Quality, learning, environment and hybrid function failure rate adjustment factors are modifiers of the assignable cause failure rates only.

With the exception of the hybrid model, which has been greatly simplified, the assignable cause models are similar in form to the models in MIL-HDBK-217E. A comparison is presented in Table 3.2-2.

Table 3.2-2 ASSIGNABLE CAUSE MODEL COMPARISON

DEVICE CATEGORY	MIL-HDBK-217E	NEW MODEL
VLSI/ULSI (LSI)	$\lambda_P = \pi_Q (C_1 \pi_T \pi_V + C_2 \pi_E) \pi_L$	$\lambda_P = \pi_Q (C_1 \pi_T + C_2 \pi_E) \pi_L$
MEMORIES	$\lambda_P = \pi_Q (C_1 \pi_T \pi_V + C_2 \pi_E) \pi_L$	$\lambda_P = \pi_Q (C_1 \pi_T + C_2 \pi_E + \lambda_{CYC}) \pi_L$
GaAs	NONE	$\lambda_P = \pi_Q ((C_{1A} \pi_{TA} + C_{1P} \pi_{TP}) \pi_A + C_2 \pi_E) \pi_L$
HYBRIDS	$\lambda_P = [\Sigma N_C \lambda_C \pi_G + (N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S) \pi_F \pi_E] \pi_Q \pi_D$	$\lambda_P = \pi_Q (\Sigma N_C \lambda_C (1 + .2 \pi_E)) \pi_L \pi_F$
PACKAGES	$C_2 \pi_E$	$C_2 \pi_E$

LEGEND TO TABLE 3.2-2

λ_p	is the device failure rate in $F/10^6$ hours
π_Q	is the quality factor
π_T	is the temperature acceleration factor (MOS and Bipolar)
π_{TA}	is the GaAs temperature acceleration factor (active devices)
π_{TP}	is the GaAs temperature acceleration factor (passive devices)
C_1	is the circuit complexity factor (MOS and Bipolar)
C_{1A}	is the GaAs circuit complexity factor (active devices)
C_{1P}	is the GaAs circuit complexity factor (passive devices)
π_E	is the application environment factor
π_L	is the device learning factor
C_2	is the package complexity factor
λ_{CYC}	is the EEPROM cycling-induced failure rate
π_F	is the circuit function factor (hybrids)
N_C	is the number of each particular component (within hybrids)
λ_C	is the component failure rate (for each component within hybrids)
π_G	is the die correction factor
N_R	is the number of chip or substrate resistors
λ_R	is the failure rate of the chip or substrate resistor
N_I	is the sum of the hybrid interconnections
λ_I	is the failure rate per interconnect
π_D	is the hybrid density factor
λ_S	is the failure rate of the hybrid package
Π_A	GaAs MMIC application factor

4.0 MODEL DEVELOPMENT

4.1 VLSI/ULSI MICROCIRCUITS AND MICROPROCESSORS

The device list which was considered for an updated VLSI/ULSI prediction model included bipolar and MOS digital devices (including shift registers, programmable logic arrays (PLA) and programmable array logic (PAL)), bipolar and MOS linear devices, bipolar and MOS digital microprocessor devices (including controllers), bipolar and MOS analog microprocessor devices, charge coupled devices (CCD), and wafer scale integration (WSI). For the end-life failure model, several class modifications were made (see Table 4.1-1). The first two classes of devices were renamed bipolar digital and linear devices (including gate/logic arrays) and MOS digital and linear devices (including gate/logic arrays), since the wearout mechanisms are similar within these classes. From discussions with microprocessor suppliers,[8] bipolar VLSI/ULSI microprocessor devices do not have a moderate to high probability of being used in near future military systems; therefore, the next two classes of devices were renamed MOS digital microprocessors (including controllers) and MOS analog microprocessors (including controllers). Because of insufficient data on the manufacturing technology of MOS analog microprocessor devices and CCDs, adequate life-prediction models could not be developed. WSI was not modeled as a separate category since it comprises many different microcircuit types whose failure rates can be calculated separately and then combined using the model of section 4.1.1.

During the development of the prediction model for VLSI/ULSI microcircuits, several assumptions were made that could not be fully substantiated during the course of the contract. The assumptions are highlighted in section 6.0 with possible direction in verifying these assumptions.

The literature search for the VLSI/ULSI model development spanned the RAC database, the Proceedings of the International Reliability Physics Symposia (IRPS), the Proceedings of the Reliability and Maintainability Symposia, the Transaction of the Reliability Society of the IEEE, and numerous other technical journals. The data collected for the end-life model development was sparse.

Table 4.1-1

VLSI/ULSI Device Category Changes

OLD	NEW
Monolithic Bipolar & MOS Digital Devices	Bipolar Digital & Linear Devices [1] (Including Gate/Logic Arrays)
Monolithic Bipolar & MOS Linear Devices	MOS Digital & Linear Devices [1] (Including Gate/Logic Arrays)
Monolithic Bipolar & MOS Digital Microprocessor Devices	Bipolar Digital Microprocessors [1] (Including Controllers)
	MOS Digital Microprocessors [1] (Including Controllers)
Monolithic Bipolar & MOS Analog Microprocessor Devices	Bipolar Analog Microprocessors [2] (Including Controllers)
	MOS Analog Microprocessors [3] (Including Controllers)
	Charge Coupled Devices (CCDs) [3]
	Wafer Scale Integration (WSI) [4]

[1] Model developed

[2] Model not viable

[3] Insufficient data

[4] End of life models for VLSI/ULSI can be used by extrapolation

Except for sources such as the IRPS (papers identified in the references), very little information was available to understand why system failures occur. Trend analysis of system data is not appropriate for developing values for the parameters in the wearout models developed. Therefore, sources such as the RAC database, the WEC field database, most industry contacts, and the bulk of the available literature on failures, all of which heavily depend on trend analysis, lack the detail necessary to pinpoint the failure mechanism, parametric stress conditions and the time-to-failure.

4.1.1 Model Overview - The Superposition Model

The approach to the updated VLSI/ULSI reliability prediction model development initially concentrated on the types and causes of system failures. By definition, a system failure is that event in which the specification of a performance parameter of the system is exceeded due to physical processes operating on the system that proceed naturally during the life of the system. Table 4.1-2 outlines the results of a recent survey[40] of system failures with respect to percent contribution of component replacement for a particular component type. The survey shows that the microcircuit is still the leading component to which many system failures are attributed.

Table 4.1-2 Summary of Parts Replacement Distributions[40]

	% Contribution		
Source:	Hughes Aircraft Company	Collins Avionics	GE
Part Type			
ICs	27	32	33
Transistors	14	14	15
Hybrid Circuits	12	**	**
Capacitors	12	19	6
Resistors	12	**	16
Diodes	10	**	**
Solder Joints (and interconnections)	3	**	5
Others (** included)	10	35	22

A survey[36] of the causes of VLSI/VHSIC microcircuit failures specifically, outlined in Table 4.1-3, shows VLSI/VHSIC microcircuits of similar complexity

failing for totally different reasons. A VLSI/VHSIC prediction model that cannot account for this inconsistency in observed failure mode/mechanisms may result in a grossly inaccurate prediction. To address this inconsistency, microcircuit failures were classified into two categories: common cause failures and assignable cause failures. These two categories of failures were then modeled separately.

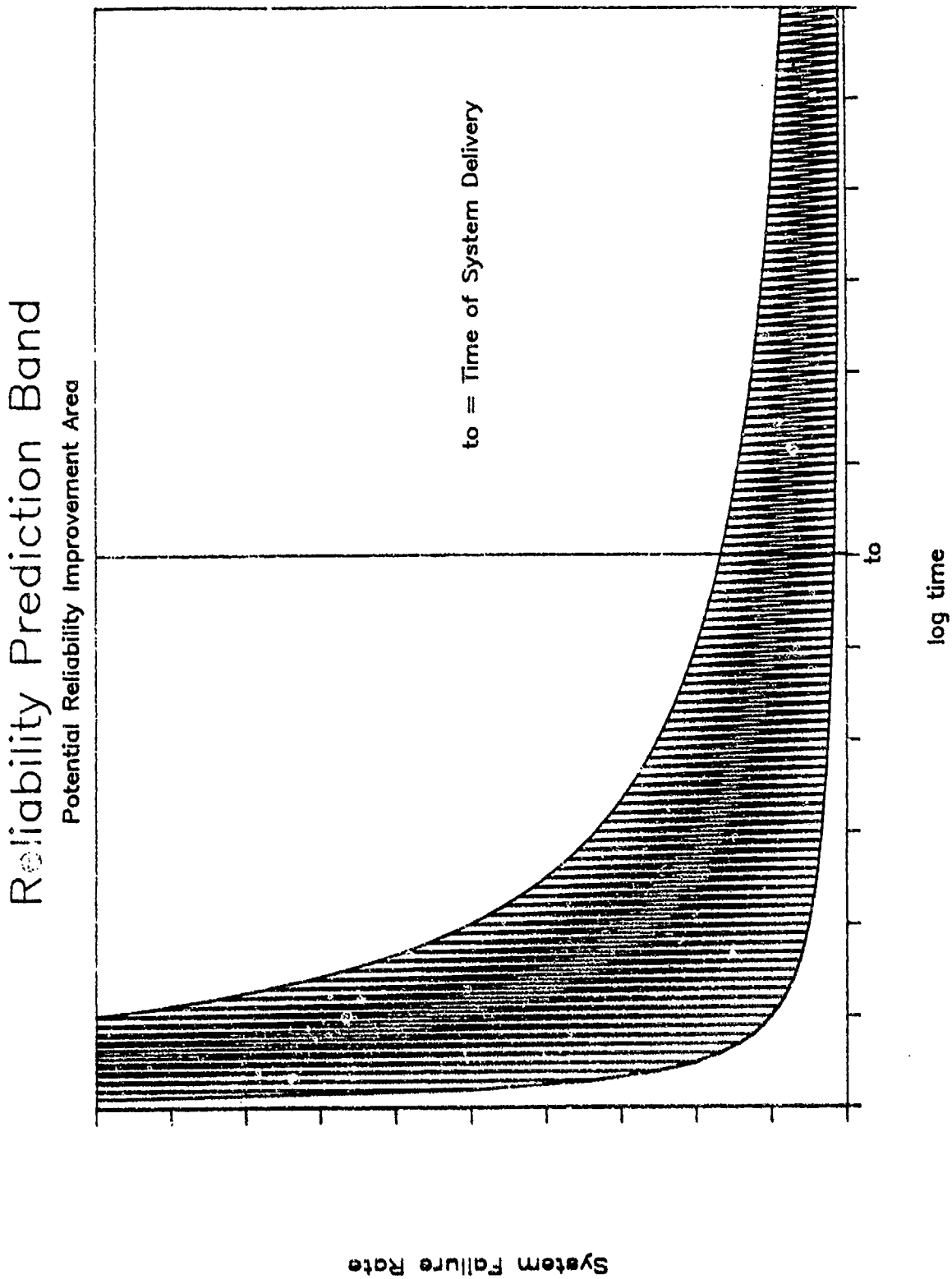
Table 4.1-3 Vendor Data[36]

	Survey Responses					
Failure Mode / Mech	1	2	3	4	5	6
Electromigration						13%
Dielectric Breakdown	X	50%	<.1%	98%		2%
Soft Errors						
Parametric Drift	X		1%			38%
Hot Electrons	X					
Latch-Up	X	10%	.1%		X	
Electrical Overstress		20%		2%	X	
Package Related		20%	<.1%		X	28%
Other					X	19%

X = failure mode occurs but no percentage given in survey response.

By modeling the common cause microcircuit failure rate separately from the total microcircuit failure rate, it is possible to evaluate the system reliability improvement due to the use of mature microcircuits which have minimized the assignable causes of failure. It is noted that these assignable cause failures can be minimized or eliminated by use of built-in-reliability (BIR) techniques or screening. The "band" of potential reliability improvement is displayed graphically in Figure 4.1-1. Assuming a bathtub-like system failure rate curve, it is reasonable for the failure rate of a system that has not eliminated the assignable causes of component failures to be an order of magnitude (or more) greater than the common cause system failure rate. Therefore, the failure rate value that should be used to predict the system reliability depends on the maturity of the microcircuits and the effectiveness of the microcircuit and system screens prior to system delivery. In the early- and middle-life defect model, these effects are addressed by the learning and quality factors.

Figure 4.1-1


Reliability Prediction Band
Potential Reliability Improvement Area
to = Time of System Delivery
to
log time
System Failure Rate

A general reliability prediction model, the Superposition Model, was developed to combine the early-, middle- and end-life prediction models. In addition, this model is used to combine the individual failure mechanism models developed as part of the end-life prediction model. This model can also be used to address end-life failure rates of WSI devices by making the assumption that the WSI device is composed of many different device styles competing to cause failure of the total WSI device.

The Superposition Model is a modified competing-risk model used to combine the early-, middle- and end-life failure distributions, as well as the individual failure mechanism distributions. According to the competing-risk model,[37] the probability of failure at time t for a microcircuit has the form

$$F(t) = 1 - \prod_{i=1}^{k} (1 - F_i(t)), \tag{4.1.1}$$

where $F_i(t)$ is the probability of failure for the ith failure distribution of k total failure distributions identified at time t.

$$F_i(t) = \int_0^t f_i(t), \tag{4.1.2}$$

where $f_i(t)$ is the ith failure probability density function. Rearranging terms in equation 4.1.1, and making the substitution that the probability of success at time t, P(t), is the complement of the probability of failure at time t,

$$P(t) = 1 - F(t), \tag{4.1.3}$$

equation 4.1.1 can be rewritten

$$P(t) = \prod_{i=1}^{k} P_i(t). \tag{4.1.4}$$

This model is not limited to specific types of failure distributions and does not require that the failure distributions be of the same type; however, the model does require independence of the failure distributions.

The Superposition Model can be used to estimate the lifetime of a microcircuit given the early-life, middle-life and end-life failure models. Since early-and middle-life failures are assignable cause failures, the model used to approximate these failures is the exponential probability density function. The functional form is given by

$$f(t) = \lambda \exp[-\lambda t] \tag{4.1.5}$$

where λ can be shown to be the hazard (time-independent) rate. Given λ_{early} and λ_{middle}, the hazard rates for early and middle-life respectively, the probability of success for the microcircuit is defined as

$$P(t) = \exp[-\lambda_{early} t] * \exp[-\lambda_{middle} t] * P_{end}(t), \tag{4.1.6}$$

where:

$P_{end}(t)$ = probability of success of the end-life failure distribution.

Equation 4.1.6 can also be written in the form of a microcircuit hazard rate at time t_0:

$$\lambda(t_0) = \lambda_{early} + \lambda_{middle} - \ln (P_{end}(t_0))/t_0 \tag{4.1.7}$$

It must be noted that $-\ln(P_{end}(t_0))/t_0$ is not a true hazard rate for end-life at time t_0 since the end-life failure distribution is not necessarily an exponential distribution; however, this "effective hazard rate" transforms properly to a worst-case probability of success using the standard equation

$$P = \exp[-\lambda t]. \tag{4.1.8}$$

A log-normal distribution is a wear-out distribution in which the hazard rate increases with time; therefore, the hazard rate at time t_0 will be greater than the hazard rate at time t_1 for $t_1 < t_0$. The associated probability of success at time t_0 will be less than the probability of success at time t_1; therefore, for all time less than t_0, a worst-case probability is derived.

All end-life probability of successes, hazard rates, and effective hazard rates are calculated for t_0 = 10,000 hours, a standard avionics system lifetime requirement which is typically specified in the contract statements of work for avionic equipment.

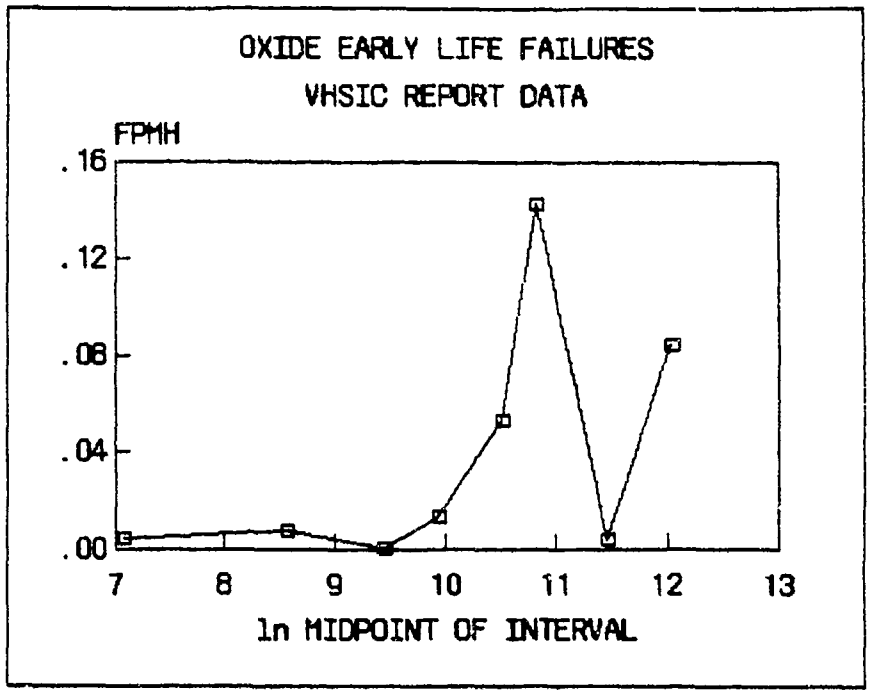
4.1.2 Early- and Middle-Life Prediction Models

Early- and middle-life of VLSI/ULSI microcircuits are limited by random failure that similarly plague non-VLSI/ULSI microcircuits. Random failures can be due to pinholes or particles in dielectrics resulting in electrical shorts, ionic contamination causing shifts in transistor parameters, and many other types of random defects. MIL-HDBK-217E is based upon exponential failure distributions which describe random failures. The exponential model is appropriate for these failures because in aggregate (at the system level where failures are reported) they appear random even though they have physical causes. This is due to the overlap of many distinct defect distributions, each having its own MTTF and standard deviation. Furthermore, the temperature dependence of the failure rate is defensible because the predominant defect failure mechanisms - dielectric breakdown and metallization failure - are accelerated by temperature. This has been shown in the literature and through life testing. While it is true that perfectly made IC's would not experience these "random" defects, it is also true that periodically flawed components go undetected in environmental screening and later manifest themselves as field failures. The literature search did not discover any failure mechanisms for VLSI/ULSI devices which do not also pertain to SSI, MSI and LSI devices. A reasonable approximation of early and middle-life for VLSI/ULSI microcircuits would therefore be an extrapolation of MIL-HDBK-217E to the complexity of these advanced technology components. From an evaluation of available VHSIC data, the extrapolation for MOS VLSI devices seems reasonable, but the activation energy requires modification.

The IITRI/Honeywell SSED VHSIC Report[36] endeavored to create time-dependent failure rates (hazard rates) for early- and middle-life failure mechanisms. The mechanisms addressed included oxide failures, metal failures, hot carrier effects, ESD effects, and miscellaneous defect failures. In the

present study efforts, that data was analyzed to determine the actual shape of the distributions (as opposed to assuming a decreasing exponential based upon two points). The three primary defect areas contributing to the early-life failure rate were found to be oxide, metal, and miscellaneous; all others were at least an order of magnitude smaller in contribution. The oxide data is plotted in figure 4.1-2, the metal data in figure 4.1-3, and the miscellaneous data in figure 4.1-4. The intervals were those given in the IITRI/Honeywell VHSIC report, and were so chosen because in many cases sources reported failures occurring within a time interval. The failure rates were determined by dividing the number of failures in each interval by the accelerated part-hours from operating life tests, burn-in, and various environmental tests (adjusted to 25°C based on the Arrhenius relationship) for that interval. As can be seen, the defects are not distributed as decreasing exponentials which would be straight lines with negative slope on a logarithmic scale. Instead, since the failures are assumed to be random, an average failure rate was calculated at 25°C as shown in the figures. The failure rates were then adjusted for temperature by use of the appropriate activation energy for the failure mechanism, as extracted from the VHSIC report, and summed to get a total failure rate. Once this was done, a combined activation energy, (E_a) was calculated by using the Arrhenius relationship (see Table 4.1-4) and weighting according to the partial contribution of each mechanism to the total failure rate. The activation energy is not constant, but increases with temperature; the range is .31 eV at 30°C to .325 eV at 150°C. However, for MOS devices, a value of .35 has been selected because this value is conservative (all errors are positive), and it is equal to the value calculated in derivation of the early-life MOS microprocessor model (.35 eV). The failure rate using .35 eV is presented over temperature in the column "FR using EA =0.35." The value at 25°C is .029 failures per million hours, implying a C1 complexity value (in the format of the MIL-HDBK-217E model) of .29 for VLSI/ULSI microcircuits (C_1 is equal to ten times the failure rate at 25°C). MIL-HDBK-217E may be considered accurate if (a) the .29 value is used for VLSI/ULSI complexity levels, and (b) the activation energy for MOS devices, (HMOS, NMOS, CMOS, etc) is changed to 0.35 eV. Insufficient data was available for this contract to develop VLSI/ULSI bipolar failure rates.

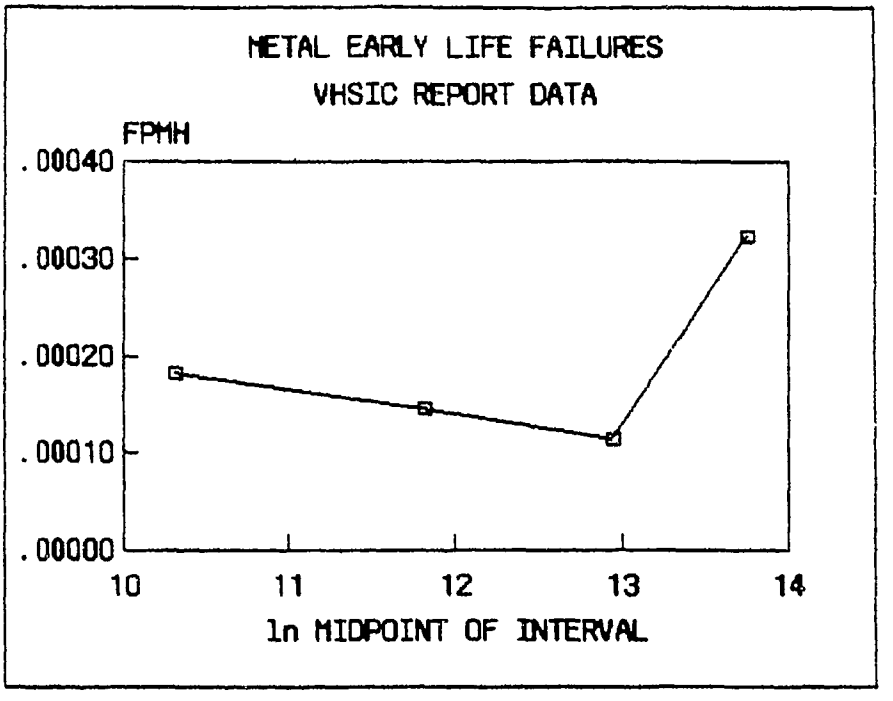
FIGURE 4.1-2



OXIDE EARLY-LIFE FAILURE DATA[36], e_A = 0.3 eV

RANGE (HOURS)	MIDPOINT	ln MIDPOINT	LAMBDA (25°C)
0 - 2,344	1,172	7.0665	.004652
2,345 - 8,204	5,275	8.5707	.008119
8,205 - 16,950	12,578	9.4397	.000606
16,951 - 24,417	20,684	9.9371	.013848
24,418 - 48,834	36,626	10.5085	.053133
48,835 - 49,224			
	49,640	10.8126	.142502
49,225 - 50,446			
50,447 - 138,452	94,450	11.4558	.003812
138,453 - 193,123	165,788	12.0185	.084240
AVERAGE LAMBDA			.0269

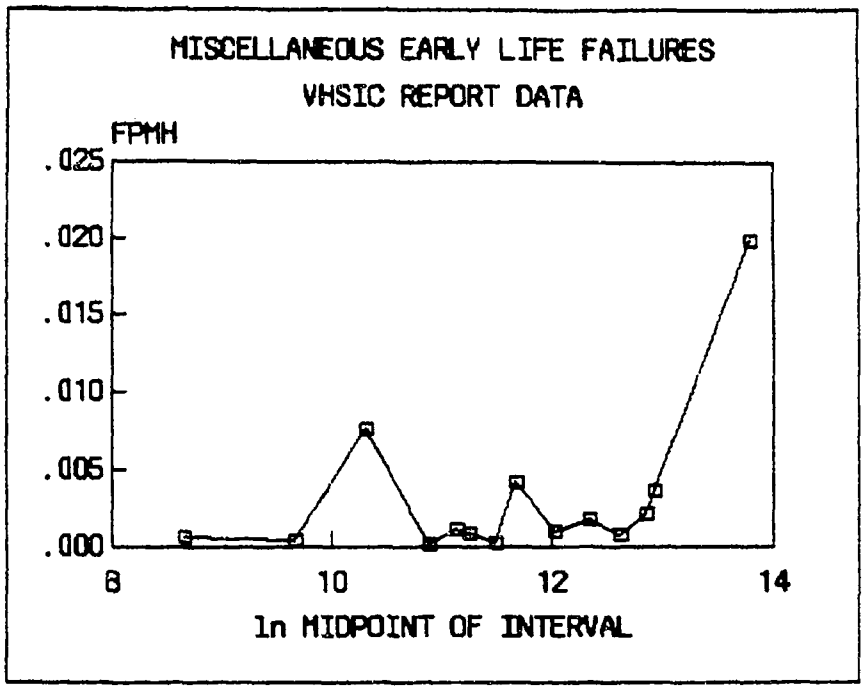
FIGURE 4.1-3



METAL EARLY-LIFE FAILURE DATA[36], e_A = 0.55 eV

RANGE (HOURS)	MIDPOINT	ln MIDPOINT	LAMBDA (25°C)
0 - 59,872	29,936	10.3068	.000182
59,873 - 209,553	134,713	11.8109	.000146
209,554 - 623,669	416,612	12.9399	.000115
623,670 - 1,247,337	935,504	13.7488	.000323
AVERAGE LAMBDA			.000219

FIGURE 4.1-4



MISCELLANEOUS FAILURE DATA[36], e_A = 0.423 eV

RANGE (HOURS)	MIDPOINT	ln MIDPOINT	LAMBDA (25°C)
0 - 11,543	5,572	8.6607	.000630
11,544 - 20,183	15,864	9.6718	.000422
20,184 - 40,402	30,293	10.3187	.007634
40,403 - 66,083	53,243	10.8826	.000202
66,084 - 70,642	68,363	11.1326	.001151
70,643 - 82,514	76,579	11.2461	.000910
82,515 - 112,394	97,455	11.4871	.000286
112,395 - 120,244	116,320	11.6641	.004195
120,245 - 210,243	165,244	12.0152	.000984
210,244 - 240,488	226,328	12.3297	.001777
240,489 - 242,412			
242,413 - 355,239	289,826	12.6076	.000796
355,240 - 393,352	374,296	12.8328	.002183
393,353 - 420,487	406,920	12.9164	.003678
420,488 - 1,510,862	965,675	13.7806	.019915
AVERAGE LAMBDA			.001872

Table 4.1-4
VLSI/VHSIC MODEL

TEMP (C)	TEMP (K)	FR-METAL (FPMH)	FR-OXIDE (FPMH)	FR-MISC. (FPMH)	FR-TOTAL (FPMH)	FR/.0290	E SUB A AVG=.317	FR USING EA=0.35	% ERROR EA=0.35
25	298	.0002	.0269	.0019	.0290	1.000	----	.0290	0.0
30	303	.0003	.0326	.0025	.0353	1.220	.310	.0363	2.61
35	308	.0004	.0393	.0032	.0429	1.480	.311	.0451	5.13
40	313	.0005	.0470	.0041	.0517	1.786	.311	.0557	7.57
45	318	.0006	.0560	.0053	.0621	2.143	.312	.0682	9.92
50	323	.0011	.0663	.0067	.0741	2.559	.312	.0832	12.18
55	328	.0015	.0781	.0084	.0881	3.041	.313	.1007	14.34
60	333	.0021	.0916	.0105	.1042	3.597	.313	.1213	16.39
65	338	.0028	.1069	.0131	.1227	4.237	.314	.1453	18.34
70	343	.0035	.1242	.0162	.1440	4.971	.314	.1731	20.19
75	348	.0047	.1436	.0199	.1682	5.808	.315	.2051	21.93
80	353	.0061	.1655	.0243	.1959	6.762	.315	.2420	23.55
85	358	.0079	.1898	.0295	.2272	7.844	.316	.2842	25.06
90	363	.0101	.2170	.0356	.2627	9.069	.317	.3322	26.46
95	368	.0128	.2472	.0428	.3027	10.451	.317	.3867	27.75
100	373	.0161	.2805	.0511	.3478	12.007	.318	.4484	28.91
105	378	.0202	.3173	.0609	.3984	13.754	.319	.5178	29.97
110	383	.0252	.3578	.0721	.4551	15.710	.319	.5958	30.91
115	388	.0312	.4022	.0850	.5184	17.897	.320	.6830	31.73
120	393	.0385	.4508	.0998	.5891	20.336	.320	.7802	32.44
125	398	.0472	.5037	.1168	.6677	23.049	.321	.8883	33.04
130	403	.0575	.5614	.1360	.7550	26.063	.322	1.0082	33.54
135	408	.0699	.6240	.1579	.8518	29.404	.323	1.1407	33.92
140	413	.0845	.6918	.1826	.9588	33.100	.323	1.2867	34.20
145	418	.1015	.7650	.2105	1.0771	37.182	.324	1.4473	34.37
150	423	.1215	.8440	.2418	1.2075	41.683	.325	1.6233	34.44

MIL-HDBK-217E does not distinguish between MOS and bipolar devices in the C1 terms for SSI, MSI and LSI devices. The predominant failure mechanism for MOS devices is TDDB which, as is well documented in the literature, has an activation energy of 0.3 eV, whereas the most common bipolar mechanisms are metallization defects and electromigration which have activation energies ranging from 0.42 to 0.9 eV. This implies that bipolar devices, having higher activation energies, will have higher failure rates than will MOS devices of similar maturity and complexity. This would be plausible if the failure rates of the two technologies were similar at 25°C; however, reliability data published by British Telecom[101] indicates that, for each level of IC complexity, the intrinsic failure rate of MOS devices is approximately 3.6 times higher than that of bipolar devices in benign environments. Assuming that this ratio holds for ICs at 25°C, the value of C1 for bipolar VLSI devices should be .08, rather than .29. Using the complexity progression of MIL-HDBK-217E yields C1 values ranging from .0025 (SSI) to .08 (VLSI) for bipolar devices. The failure rates of bipolar devices will thus be lower than those of CMOS devices up to a temperature of 109°C (assuming the MIL-HDBK-217E energy of 0.5 eV for LSTTL).

To develop the microprocessor failure rates, data was compiled from two sources,[97, 104] and a summary is presented in Table 4.1-5. As was done in MIL-HDBK-217E, the devices were grouped by bit complexity although some of the assignments were subjective (based upon device description). Several points need to be made concerning the data for these devices:

1. The database was very small.
2. Some manufacturers' data show no distinction in failure rate due to device complexity.
3. Very little, if any, correlation was found between device package type and die-related failure mechanisms for hermetic versus molded plastic packages. The reason for this is that microcircuit manufacturers today employ die passivation in non-hermetic applications. Corrosion will not be a problem, particularly for the short duration and controlled environment of a burn-in or life test from which this data was derived.

Table 4.1-5 Microprocessor Data

TECHNOLOGY	TYPE	D level λ @ 70°C (FPMH)	B level λ @ 70°C (FPMH)	E_A (AVG) (eV)	B level λ @ 25°C (FPMH)	C1 Computed	C1 Proposed
HMOS	8 Bit Microprocessor	.190	.0576	.4	.0075	.07	
NMOS	8 Bit Controller	.324	.0982	.3	.0212	.21	
HMOS	8 Bit Controller	.313	.0948	.3	.0205	.20	
	8 Bit Average (MOS)	.275	.833	.33	.0154	.15	.14
TTL	8 Bit Controller (Bipolar)	.214	.0648	.62	.0027	.03	.06
HMOS	16 Bit CPU	.757	.2294	.4	.0297	.30	
HMOS	16 Bit Coprocessor	.566	.1715	.42	.0201	.20	
HMOS	16 Bit Microprocessor	.510	.1545	.3	.0334	.33	
HMOS	16 Bit Microprocessor	.577	.1748	.38	.0251	.25	
	16 Bit Average (MOS)	.603	.1827	.37	.0276	.28	.28
TTL	16 Bit Controller (Bipolar)	.595	.1803	.54	.0114	.11	.12
HMOS	32 Bit Controller	1.147	.3476	.3	.0751	.75	
HMOS	32 Bit Microprocessor	1.069	.3239	.45	.0325	.33	
HMOS	50 Process Numerical Data Processor (NDP)	1.333	.4039	.36	.0642	.64	
	32 Bit Average (MOS)	1.183	.3585	.37	.0541	.54	.56
TTL	Bus Arbiter (Bipolar)	1.213	.3676	.5	.0286	.29	.24
	MOS Average			.35			
	Bipolar Average			.55			

4. The assignment of complexity factors to devices such as CPUs, controllers, coprocessors, clock-drivers, bus arbiters, and other microprocessor peripherals is difficult to do.
5. A microprocessor comprised of one or two microcircuit chips will be more reliable than one comprised of more, but lower-complexity, microcircuits.

As shown in Table 4.1-5, the data was presented in the form of failure rates from life tests of commercial devices (D quality level) at 70°C. These failure rates were then adjusted to B-level by dividing by 3.3, the value of π_Q for the D quality level (see paragraph 4.6.1 for derivation of this value). The database provided activation energies for each failure mechanism experienced by each device type listed. Failure rates were also presented for each failure mechanism. Average activation energies were obtained by weighting according to their percentage contribution to the total failure rate at 70°C. An example calculation is given below:

mechanism A: .3 eV .04 fpmh
mechanism B: .5 eV .20 fpmh
mechanism C: .4 eV .56 fpmh
average E_A: ((.3 x .04) + (.5 x .20) + (.4 x .56)) / .80 = .42 eV

Using the average activation energies, the failure rates at 25°C were calculated by employing the Arrhenius relationship:

$\lambda 25 = \lambda 70 * \exp [E_A / K (1/343 - 1/298)]$, where
$\lambda 25$ is the failure rate at 25°C
$\lambda 70$ is the failure rate at 70°C
E_A is the average activation energy
K is Boltzman's constant (8.617E-5 eV/°Kelvin)
343 is 70°C in Kelvin, and 298 is 25°C in Kelvin

The C_1 values for these devices were derived to be consistent with the MIL-HDBK-217 convention (a π_T value of 0.1 at 25°C) by multiplying the failure rates at 25°C by 10. It should be noted that the failure rates and

C_1 values approximately double for each increase in microprocessor bit complexity. Consequently, the proposed values of C_1 to be used are presented in the last column of Table 4.1-5. The values for bipolar devices are less than half the MOS values at 25°C. This is because the failure rates of the two technology devices at 70°C were similar, but the bipolar devices had higher activation energies.

Two factors which had been considered for inclusion in the models were omitted. The first is a voltage-acceleration factor for MOS devices. While it is true that the predominant MOS failure mechanism, oxide failure, is accelerated by higher voltages, most MOS devices now operate at 5 volts. To attempt to correct for nigher voltages in a defect model is inconsistent with ease of use, and that level of accuracy is not supported by the database. Furthermore, devices made to operate at higher voltages should have thicker oxides; the end-life model presented in section 4.1.3.1 should be used to assess the voltage effect.

The second factor is an electrostatic-discharge factor to reflect the device susceptibility to ESD damage. While the susceptibility can be quantified, the probability of failure due to that susceptibility cannot because it is dependent upon how the device is handled. From our experience in the Westinghouse Reliability Analysis Laboratory, approximately 0.1% of all failures are attributable to ESD; therefore, if an ESD factor was desired, a value of 1.001 could be used. It has been omitted from our models in the interest of simplicity, and also because it is "in the noise" of the accuracy of the early-middle-life models. Other electrical overstress failure rates, which are purely secondary events, should not be included in any early-mid-life prediction model.

4.1.3 End-Life Failure Mechanism Models

Figure 4.1-5 shows graphically how the Superposition Model is developed for modeling end-life failure prediction. With three failure mechanisms competing on a particular microcircuit, it is necessary to know the failure rate of the microcircuit at a particular time, t1. If the values of the cumulative

failure distributions (probability of failure functions) for each mechanism (appropriately scaled) at time t1 are small (i.e., less than 1% - a reasonable assumption at the time the microcircuit is delivered as part of a system), then the value of the total cumulative failure distribution is approximately the sum of the cumulative failure distributions of each mechanism. Although many potential failure mechanisms can be identified, their impact on the total cumulative failure distribution may not be significant. An understanding of which mechanisms must be modeled for each VLSI/ULSI technology was pursued.

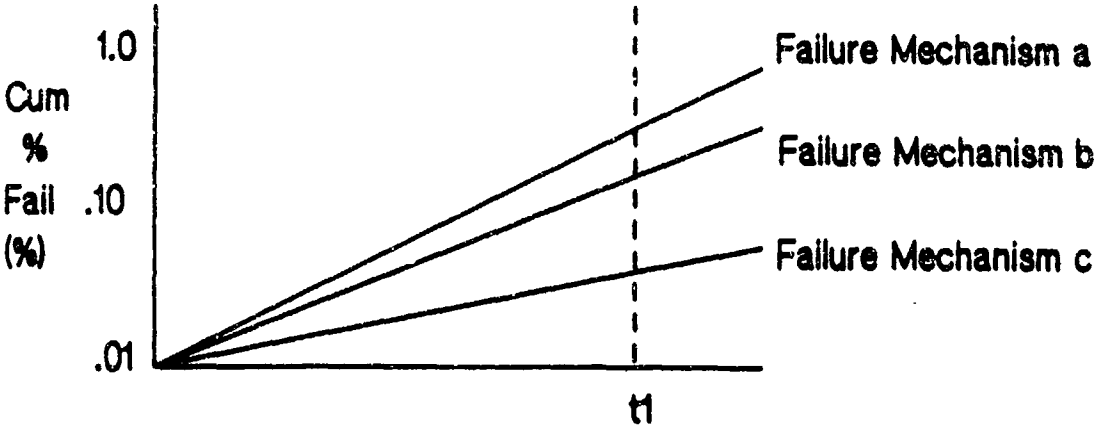
From literature searches and in-house failure analyses, a list of failure mechanisms affecting VLSI/ULSI microcircuits was developed. The electrical mechanisms are outlined in Table 4.1-6. Of those fai'ure mechanisms, it was necessary to identify those which are related to common cause failures. The list was reduced to three failure mechanisms: time dependent dielectric breakdown (TDDB), electromigration (EM), and charge injection (CI). The latter mechanism was further discounted as being a design consideration rather than an inherent physical property and therefore should not contribute to the total end-life failure distribution (see section 4.1.3.3). With the common cause failure mechanisms identified, each mechanism was quantified using available data from literature and in-house reliability analysis programs. A survey of these microcircuits was performed to make the model user-friendly. The methodology for applying the end-life failure mechanism models to specific microcircuits can be found in section 4.1.4.

4.1.3.1 TDDB Model

According to the literature on time-dependent dielectric breakdown (TDDB),[16] failure occurrences are distributed normally with the logarithm of time. The general form of the failure density function is

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} \exp\left[(-1/2)\left(\frac{\ln t - (A_A * \ln (t_{50\%} / (A_T * A_{EF})))}{\sigma}\right)^2\right], \quad (4.1.9)$$

Superposition: An Example



$$F(t) = 1-[(1-Fa(t1))(1-Fb(t1))(1-Fc(t1))]$$

$Fa(t1) = 0.0100$

$Fb(t1) = 0.0020$ $\longrightarrow$ $F(t1) = 0.0128$

$Fc(t1) = 0.0008$

Note: $F(t1) \approx Fa+Fb+Fc$

Figure 4.1-5

Table 4.1-6 Potential Electrical Failure Mechanisms for Advanced Technologies

Mechanism	Failure Mode	Accelerating Conditions
Time Dependent Dielectric Breakdown	Gate shorts, interlayer shorts in interconnection system	Voltage, increased temperature
Electromigration	Interlayer or intralayer shorts in interconnection system, and open circuits	Current, increased temperature
Hot Carriers	Threshold shifts, g_m shifts	Source/drain voltage, decreased temperature
Mobile Ions	Threshold shifts	Gate/source voltage, decreased temperature
Surface State Movement	Leakage	Radiation, current
Latent ESD Damage	Gate shorts, protection network shorts	Voltage, current
Corrosion	Opens in interconnections	Humidity, increased temperature
Unequal Metal Diffusion Rates	Contact resistance change	Current, increased temperature

where:

$t_{50\%}$ = median of the reference distribution
σ = standard deviation of the reference distribution
A_A = acceleration factor due to area
A_T = acceleration factor due to temperature
A_{EF} = acceleration factor due to an electric field.

Area Acceleration Factor

Dielectrics are inherently defective because of their amorphous structure. Defects will always exist no matter how small an area is being stressed. It is assumed that dielectric defects are randomly distributed along two dimensions and are indistinguishable. Bose-Einstein statistics allow the determination of the defect density,[38] D(t), knowing the area of the structure in question, A, and the probability of failure function, F(t). For this uniform defect density,

$$D(t) = (1/A)(F(t) / (1 - F(t))). \tag{4.1.10}$$

From this expression, the probability of failure function can be obtained for structures of different areas, assuming the defect density and the failure mechanism are the same. That is,

$$(1/A_0)(F_0(t) / (1 - F_0(t))) = D(t) = (1/A_S)(F_S(t) / (1 - F_S(t))), \tag{4.1.11}$$

where A_0 = area of the reference structure
A_S = area of the new structure

Rearranging terms gives

$$F_0(t) = [1 + (A_S / A_0)((1 / F_S(t)) - 1)]^{-1}. \tag{4.1.12}$$

This equation describes the relationship between the probability of failure for the new structure, $F_S(t)$, and the probability of failure for the reference structure, $F_0(t)$, at any time t.

The area acceleration factor, A_A, is defined by

$$A_A = \mu_S / \mu_O = \ln(t_{S\ 50\%}) / \ln(t_{O\ 50\%}). \qquad (4.1.13)$$

where $t_{S\ 50\%}$ = median of the distribution of the new structure
$t_{O\ 50\%}$ = median of the distribution of the reference structure.

Although μ_O is known, μ_S must be determined to calculate the value of A_A for the new structure. One method for determining the value of μ_S is to realize that $F_S(t=t_{S\ 50\%}) = 0.5$, by definition. Substituting this value into equation 4.1.12 gives

$$F_O(t_{S\ 50\%}) = A_O / (A_O + A_S). \qquad (4.1.14)$$

$F_O(t_{S\ 50\%})$ is the probability of failure of the reference structure at the time in which 50% of the new structures would fail. Since the $F_O(t)$ function is known, and the associated number of sigmas away from the reference median, Z, can be approximated by the area under the normal (gaussian) density function provided by tables in most comprehensive statistics texts or by the software program in Appendix C, it is possible to determine μ_S directly by

$$\mu_S = \mu_O + (Z * \sigma). \qquad (4.1.15)$$

The variance, σ^2, for a uniform defect density is 1, and equation 4.1.15 can be rewritten

$$\mu_S = \mu_O + Z. \qquad (4.1.16)$$

Substituting equation 4.4.16 into equation 4.1.13 gives

$$A_A = 1 + (Z / \mu_O) \qquad (4.1.17)$$

where $\mu_O = \ln(t_{O\ 50\%})$.

For convenience, Table 4.1-7 provides Z values for some values of $F_O(t)$.

Table 4.1-7 Common Z-Values

$F_0(t)$	Z-Value
0.0013	3.00
0.0228	2.00
0.1587	1.00
0.5000	0.00
0.8413	-1.00
0.9772	-2.00
0.9987	-3.00

Temperature Acceleration Factor

The acceleration factor due to temperature, A_T, is given by the well-known Arrhenius relationship:[16]

$$A_T = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_0} - \frac{1}{T_S}\right)\right], \qquad (4.1.18)$$

where:

E_a = experimentally determined activation energy (0.3 eV)
k = Boltzmann's constant = 8.617 E-5 eV/°K
T_S = operating stress temperature, user supplied (°K)
T_0 = reference temperature (295°K)

Electric Field Acceleration Factor

The acceleration factor due to the applied electric field, A_{EF}, is given by[16]

$$A_{EF} = \exp\left[B * (E_S - E_0)\right], \qquad (4.1.19)$$

where:

E_S = operating electric field stress (user supplied Mv/cm)
E_0 = reference electric field stress (2.222 Mv/cm)
B = experimentally determined electric field constant (4.5 cm/Mv)

Reference Distribution

A literature review identified reasonably consistent values for the acceleration coefficients, E_a and B while accelerated life data on Westinghouse test structures was used to develop the reference distribution statistics, μ_0 and σ.

Table 4.1-8 lists the pertinent parameters and references from which the values of E_a and B were derived. The value of E_a = 0.3 eV was consistent for dielectric thickness between 100 Å and 1100 Å. The value of B varied considerably between authors. Crook[16] identified a B of 16.1 for known defective oxides of 400 Å to 1100 Å. Abadeer[17] identified a B of 6.4 for oxides of 150 A to 450 A. Baglee[12] identified a B of approximately 4.5 for 100 A oxides. Hokari[13] identified a B of 4.0 for 600 A to 1000 A. The value of B is apparently dependent on the type of dielectric defect; however, since the end-life failure distribution is defined as wear out of the dielectric, not random defects, the value of B = 4.5 was most consistent for dielectric thickness between 100 Å and 1000 Å.

The test structure used in the accelerated life test had total gate area, field oxide periphery and polycrystalline silicon gate periphery comparable to a 4k SRAM. The gate area, specifically, was 1.782E5 um^2 (5.25 log um^2). The thermally grown oxide thickness was 225 angstroms. The life test was a ramped voltage-breakdown test where the voltage on the gate was ramped at 5V/second, starting at 0 volts with the silicon substrate at 0 volts. The breakdown voltage was the voltage at which >1 uA of current was measured between the gate and substrate. Subsequent isolation tests of the structures verified catastrophic breakdown had occurred. All testing was performed at 22°C on a Keithley 350 tester.

Because of the linear relationship between breakdown voltage and the normal distribution of cumulative percent failure, a linear least squares fit to the data was performed to obtain the median breakdown voltage, $V_{b\ 50\%}$, and the standard deviation, σ_b. Table 4.1-9 shows the results of the life tests of seven wafers of 15 test structures each.

Table 4.1-8 Observed Dielectric Breakdown Parameter Values

dielec type	dielec thick (A)	dielec area (cm2)	cap	dielec temp (C)	stress temp (C)	brkdwn cond (Mv/cm)	stress cond (Mv/cm)	defect type	defect density	Ea (eV)	B (cm/Mv)	mu (hrs)	sig	ref
thermal SiO2	32	0.1	4000 A poly Si	1000	25	<1	constant field time vary	Si surface	>65%					11
						1 to 8		Si u defect	0%					
						>8		intrinsic	<25%					
	110	0.1		1000	25	<1			<15%					
						1 to 8			0%					
						>8			<55%					
	348	0.1		1000	25	<1			<5%					
						1 to 8			<75%					
						>8			<25%					
	621	0.1		1000	25	<1			<5%					
						1 to 8			<25%					
						>8			<50%					
oxide1	198	0.1	poly Si				7.5							
oxide2	198	0.1										3.04	1.54	
thermal SiO2	100	0.0097	5000A LPCVD poly	900	25	10-11v	stress votage short duration	electric breakdown	45%					12
	100	0.0097		900	25	11-12v			55%					
	100	0.0097		900	25		8			0.3		2.02	0.93	
	100	0.0097		900	85		8			0.3		1.11	0.12	
	100	0.0097		900	150		8			0.3		0.34	-1.63	
	100	0.0097		900	150		5				4.25-4.61	5.42	4.3	
	100	0.0097		900	150		6				4.25-4.61	4.03	2.37	
	100	0.0097		900	150		7				4.25-4.61	2.37	1.38	
	100	0.0097		900	150		8				4.25-4.61	0.38	-1.7	
										1	4.01			13

Table 4.1-8 Observed Dielectric Breakdown Parameter Values CONTD

dielec type	dielec thick (A)	dielec area (cm2)	cap	dielec temp (C)	stress temp (C)	brkdwn cond (Mv/cm)	stress cond (Mv/cm)	defect type	defect density	Ea (eV)	B (cm/Mv)	mu (hrs)	sig	ref
thermal SiO2	<50A	doesn't matter	doesn't matter			~12	voltage ramp but doesn't matter	enlarged weak spot and increased leakage						14
					-196 to 250					0.9				
fet	700	0.0012	poly Si		150		8.5v					7.07	2.25	15
	700	0.0012			150		12v					6.25	2.25	
	700	0.0012			150		17v					4.89	2.25	
	700	0.0012			150		20v					3.86	2.22	
	700	0.0012			150		25v					3.27	2.27	
	700	0.0072			150		2.4					13.96	6.01	
	700	0.00503			150		2.4					12.21	4.98	
	700	0.000852			150		2.4					9	5.34	
	700	.0000529			150		2.4					7	5.42	
SiO2	700		Al								6.09			
	1000										3.5			
	2400										8.64			
	4400										3.96			
	13000										5.2			
	27000										5.4			
	900		poly Si								2.97			

Table 4.1-8 Observed Dielectric Breakdown Parameter Values CONTD

dielec type	dielec thick (A)	dielec area (cm2)	cap	dielec temp (C)	stress temp (C)	brkdwn cond (Mv/cm)	stress cond (Mv/cm)	defect type	defect density	Ea (eV)	B (cm/Mv)	mu (hrs)	sig	ref
thermal SiO2	660	0.015	n-type poly				const volt until brkdwn			0.3	16.12	5.44	12.84	16
	850	0.017								0.3	16.12	14.34	11.54	
	390	0.015								0.3	16.12	9.24	6.24	
	1100	0.0035								0.3	16.12	41.64	21.34	
	1100		mos		25		5			0.3	16.12	21.44	20.44	
	1100				25		4			0.3	16.12	25.44	18.44	
	1100				25		3			0.3	16.12	40.44	23.44	
	400				25		2			0.3	16.12	15.44	12.94	
	400				70		2			0.3	16.12	14.64	13.04	
	400				125		2			0.3	16.12	14.04	13.44	
	400				160		2			0.3	16.12	13.24	13.44	
	150				30						6.45			17
	300				30						6.45			
	450				30						6.45			

Table 4.1-9 TDDB Experiment Results

Lot	Wafer	$V_{b\ 50\%}$(V)	σ_b(V)	r^2
6424	- 11	20.73	0.15	0.84
6424	- 12	20.36	0.17	0.96
6424	- 17	20.76	0.11	0.91
6424	- 19	20.74	0.08	0.83
6424	- 24	20.42	0.25	0.90
6431	- 10	20.39	0.26	0.80
6431	- 13	20.21	0.35	0.85
			----	----
Average		20.52	0.20	
Error		0.21	0.09	

Worst case estimates of $V_{b\ 50\%}$ and σ_b were obtained using

$$V_{b\ 50\%} = \text{average}(V_{b\ 50\%}) - 3 * \text{error}(V_{b\ 50\%}) \qquad (4.1.20)$$

$$\sigma_b = \text{average}(\sigma_b) + 3 * \text{error}\ (\sigma_b) \qquad (4.1.21)$$

The conservative estimates of V_b and σ_b were calculated to be 19.90 volts and 0.47 volts, respectively.

The relationship between breakdown voltage under ramped voltage stress and time at a constant voltage stress is given by[17]

$$t = (t_{ox}/BR) \exp [B(E_R - E_O)] \qquad (4.1.22)$$

where:

t = the time required to attain a probability of failure under a constant electric field stress, E_O, that is the same as the probability of failure obtained by ramping when electric field reaches a value, E_R.

t_{ox} = dielectric thickness

R = ramp rate

E_R = breakdown electric field when ramping

E_O = electric field at desired constant operating voltage

B = experimentally determined constant.

Using this relationship, the values of μ_O and σ were determined to be 8.4 and 0.4 log hours, respectively, for a constant operating voltage of 5 volts.

With the TDDB reference distribution statistics identified, the user must determine the acceleration factors for total transistor gate area, dielectric temperature, and electric field stress to obtain the TDDB distribution statistics for the microcircuit in question. Figures 4.1-6 through 4.1-8 are plots of equations 4.1.17-4.1.19 and may be used instead of equations 4.1.17-4.1.19 to determine the area acceleration factor, A_A, the temperature acceleration factor, A_T, and the electric field acceleration factor, A_{EF}, respectively. From the TDDB distribution statistics for the microcircuit, the user can calculate probability of success, hazard rate, and effective hazard rate at any time t for TDDB. Alternatively, the user can use the tables in Appendix D to determine the probability of success at 10,000 hours and the hazard rate at 10,000 hours given total transistor gate dielectric area, junction temperature and electric field stress.

Note: Tables 4.1-10 and 4.1-11 provide one example of each of the TDDB probability of success and effective hazard rate distributions, respectively. The comprehensive associated tables for TDDB effective hazard rate may be found in Appendix A.

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99983	.99216	.89461	.53442
5.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99949	.98298	.83009	.41663
10.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99864	.96661	.74796	.30961
15.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99675	.94022	.65233	.21964
20.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99985	.99295	.90141	.54957	.14906
25.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99961	.98598	.84886	.44690	.09705
30.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99907	.97423	.78289	.35084	.06080
35.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99795	.95596	.70558	.26614	.03676
40.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99582	.92947	.62050	.19537	.02152
45.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99983	.99203	.89351	.53204	.13904	.01223
50.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99960	.98578	.84757	.44473	.09611	.00677
55.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99917	.97606	.79199	.36254	.06467	.00366
60.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99834	.96181	.72809	.28842	.04244	.00194
65.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99690	.94201	.65794	.22417	.02722	.00101
70.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99990	.99450	.91582	.58413	.17040	.01710	.00051
75.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99978	.99071	.88273	.50945	.12686	.01054	.00026
80.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99957	.98501	.84262	.43654	.09262	.00639	.00013
85.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99920	.97682	.79588	.36766	.06641	.00381	.00006
90.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99858	.96552	.74331	.30452	.04682	.00224	.00003
95.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99756	.95052	.68613	.24821	.03251	.00131	.00001
100.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99599	.93133	.62580	.19925	.02225	.00075	.00001
105.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99987	.99363	.90757	.56392	.15766	.01504	.00043	.00000
110.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99977	.99024	.87906	.50210	.12307	.01004	.00024	.00000
115.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99959	.98551	.84582	.44182	.09486	.00663	.00014	.00000
120.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99932	.97912	.80810	.38432	.07226	.00434	.00008	.00000
125.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99888	.97075	.76634	.33062	.05444	.00282	.00004	.00000
130.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99823	.96006	.72118	.28140	.04060	.00181	.00002	.00000
135.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99728	.94677	.67339	.23707	.03000	.00116	.00001	.00000
140.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99592	.93065	.62384	.19781	.02198	.00074	.00001	.00000
145.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99988	.99405	.91151	.57340	.16354	.01597	.00047	.00000	.00000
150.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99981	.99152	.88927	.52296	.13405	.01153	.00029	.00000	.00000
155.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99970	.98819	.86394	.47334	.10899	.00827	.00018	.00000	.00000
160.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99953	.98389	.83561	.42526	.08795	.00589	.00011	.00000	.00000
165.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99928	.97845	.80449	.37932	.07047	.00418	.00007	.00000	.00000
170.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99894	.97172	.77085	.33600	.05609	.00295	.00004	.00000	.00000
175.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99845	.96352	.73503	.29565	.04438	.00207	.00003	.00000	.00000

Table 4.1-10 TDDB: PROBABILITY OF SUCCESS AT 10000. HOURS FOR AREA = 4.00 LOG SQUARE MICRONS

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.017	.787	11.137	62.658
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.051	1.717	18.622	87.556
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.002	.136	3.396	29.040	117.243
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.005	.325	6.164	42.720	151.579
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.015	.708	10.380	59.862	190.339
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.039	1.412	16.386	80.542	233.252
30.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.093	2.610	24.477	104.743	280.018
35.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.003	.205	4.504	34.873	132.372	330.328
40.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.007	.419	7.314	47.724	163.284	383.873
45.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.017	.800	11.259	63.104	197.301	440.353
50.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.040	1.432	16.539	81.029	234.226	499.480
55.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.084	2.423	23.320	101.465	273.850	560.985
60.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.002	.166	3.894	31.733	124.333	315.965	624.611
65.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.005	.311	5.974	41.864	149.537	360.363	690.121
70.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.010	.552	8.793	53.763	176.958	406.845	757.294
75.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.022	.934	12.474	67.442	206.466	455.217	825.928
80.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.043	1.510	17.123	82.887	237.924	505.299	895.833
85.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.080	2.346	22.831	100.059	271.195	556.917	966.834
90.	.000	.000	.000	.000	.000	.000	.000	.000	.002	.143	3.509	29.664	118.903	306.143	609.913	999.000
95.	.000	.000	.000	.000	.000	.000	.000	.000	.003	.244	5.074	37.669	139.349	342.634	664.134	999.000
100.	.000	.000	.000	.000	.000	.000	.000	.000	.007	.402	7.114	46.873	161.319	380.540	719.441	999.000
105.	.000	.000	.000	.000	.000	.000	.000	.000	.015	.639	9.698	57.284	184.732	419.737	775.705	999.000
110.	.000	.000	.000	.000	.000	.000	.000	.000	.023	.981	12.890	68.895	209.499	460.109	832.804	999.000
115.	.000	.000	.000	.000	.000	.000	.000	.000	.041	1.460	16.745	81.686	235.535	501.543	890.627	999.000
120.	.000	.000	.000	.000	.000	.000	.000	.001	.069	2.110	21.307	95.627	262.753	543.936	949.070	999.000
125.	.000	.000	.000	.000	.000	.000	.000	.001	.112	2.969	26.613	110.679	291.066	587.190	999.000	999.000
130.	.000	.000	.000	.000	.000	.000	.000	.002	.177	4.076	32.687	126.799	320.394	631.212	999.000	999.000
135.	.000	.000	.000	.000	.000	.000	.000	.004	.273	5.470	39.543	143.938	350.655	675.917	999.000	999.000
140.	.000	.000	.000	.000	.000	.000	.000	.007	.408	7.188	47.187	162.046	381.773	721.225	999.000	999.000
145.	.000	.000	.000	.000	.000	.000	.000	.012	.597	9.266	55.617	181.068	413.676	767.061	999.000	999.000
150.	.000	.000	.000	.000	.000	.000	.000	.019	.851	11.736	64.824	200.954	446.294	813.355	999.000	999.000
155.	.000	.000	.000	.000	.000	.000	.000	.030	1.188	14.626	74.794	221.649	479.561	860.043	999.000	999.000
160.	.000	.000	.000	.000	.000	.000	.000	.047	1.624	17.959	85.506	243.102	513.416	907.065	999.000	999.000
165.	.000	.000	.000	.000	.000	.000	.001	.072	2.178	21.755	96.938	265.261	547.800	954.364	999.000	999.000
170.	.000	.000	.000	.000	.000	.000	.001	.106	2.869	26.027	109.065	288.076	582.659	999.000	999.000	999.000
175.	.000	.000	.000	.000	.000	.000	.002	.155	3.716	30.785	121.858	311.501	617.940	999.000	999.000	999.000

Table 4.1-11 TDDB: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 4.00 LOG SQUARE MICRONS

Figure 4.1-6 Area Acceleration Factor for TDDB

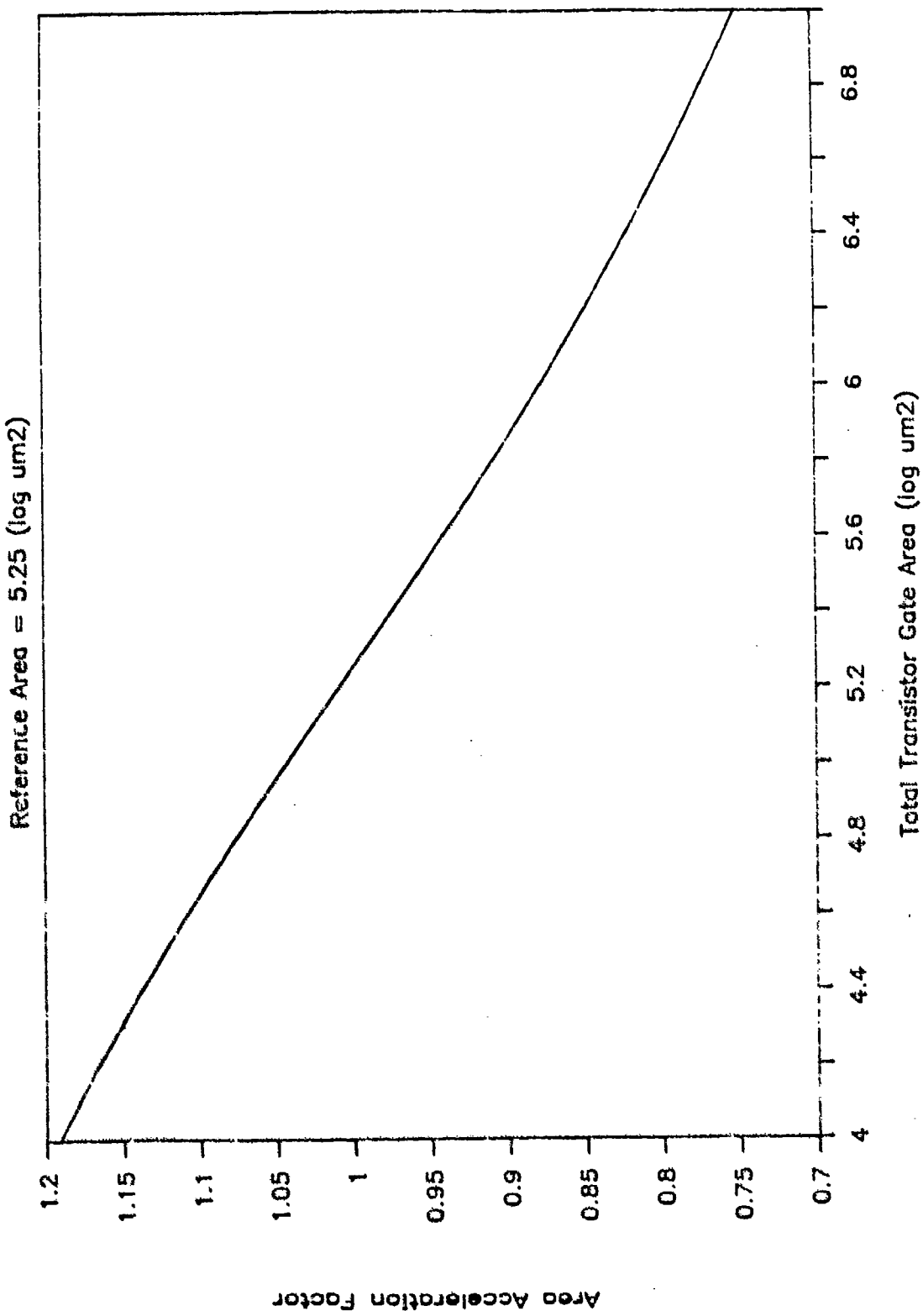


Figure 4.1-7 Temperature Acceleration Factor for TDDB

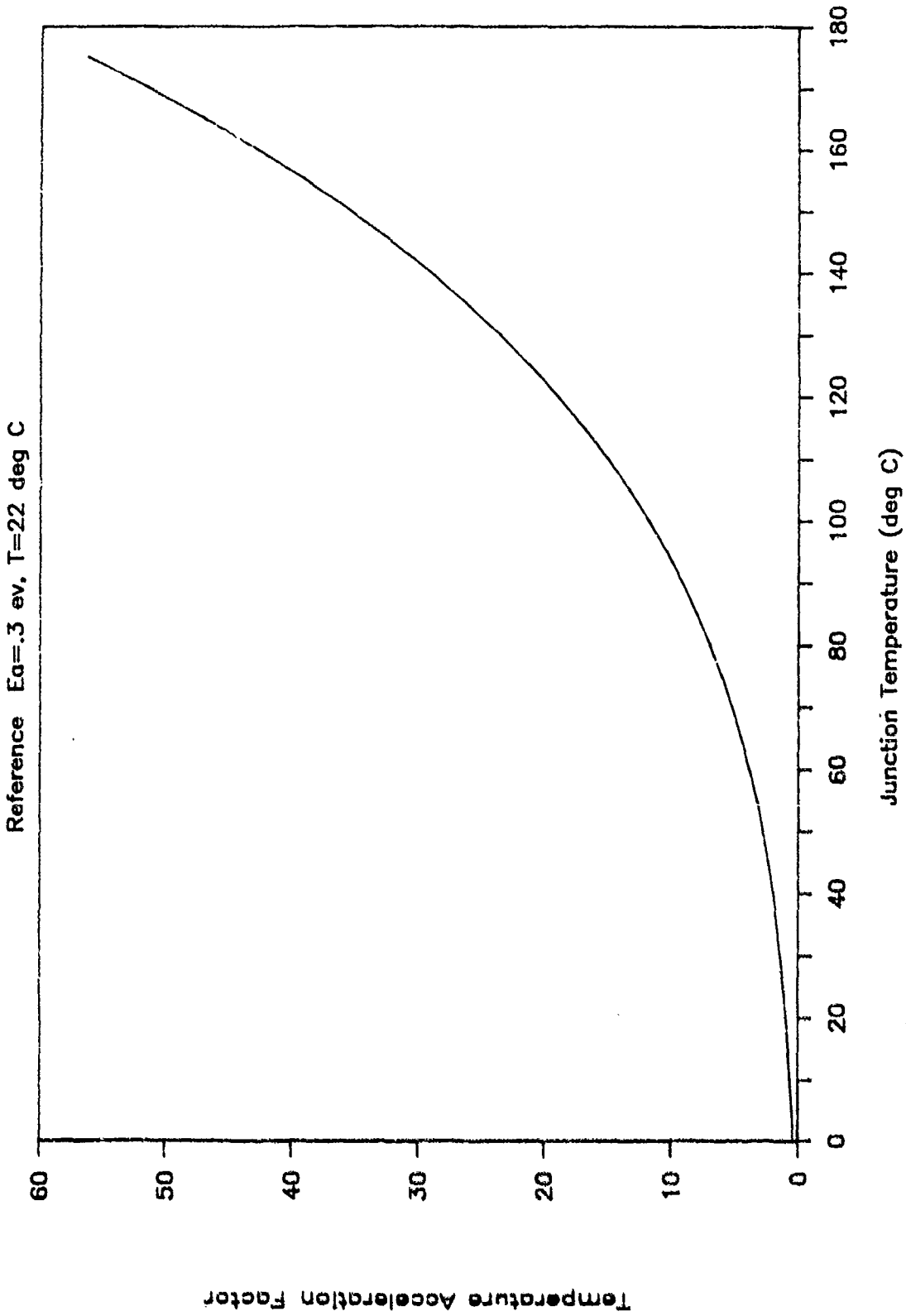
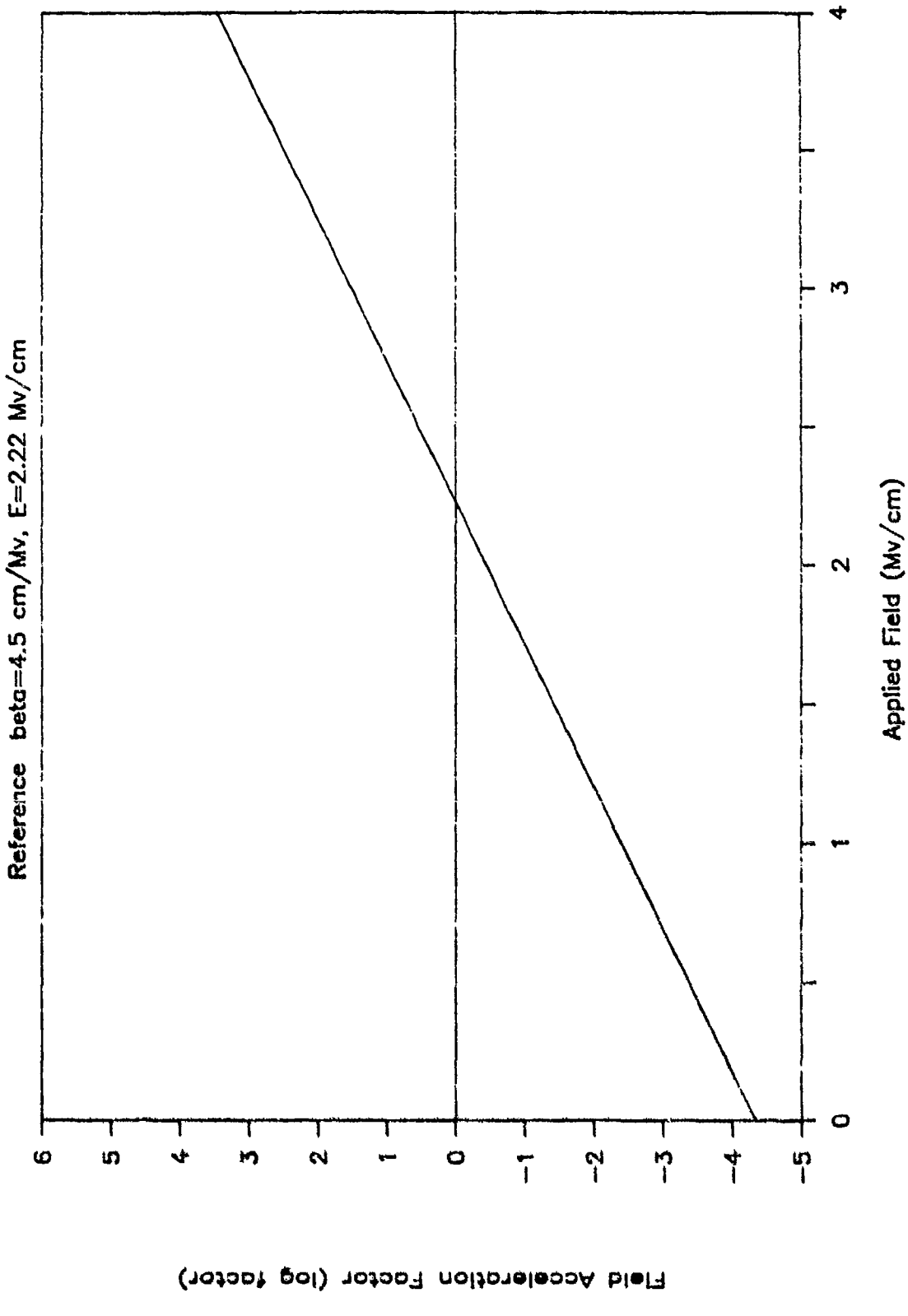


Figure 4.1-8 Electric Field Acceleration Factor for TDDB



4.1.3.2 Electromigration Model

According to the literature on electromigration (EM),[23] failure occurrences are distributed normally with the logarithm of time, similar to TDDB. The general form of the failure density function is

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} \exp\left[(-1/2)\left(\frac{\ln t - (\ln(t_{50\%} / (A_T * A_J)))}{\sigma}\right)^2\right], \quad (4.1.23)$$

where:

$t_{50\%}$ = median of the reference distribution
σ = standard deviation of the reference distribution
A_T = acceleration factor due to temperature
A_J = acceleration factor due to current density.

Temperature Acceleration Factor

The acceleration factor due to temperature, A_T, is given by the well-known Arrhenius relationship:[16]

$$A_T = \exp\left[\frac{E_a}{k}\left(\frac{1}{T_0} - \frac{1}{T_S}\right)\right], \quad (4.1.24)$$

where:

E_a = experimentally determined activation energy (.5 eV)
k = Boltzmann's constant = 8.617 E-5 eV/K
T_S = operating stress temperature (user supplied K)
T_0 = reference temperature (488 K)

Current Density Acceleration Factor

The acceleration factor due to current density, A_J, is given by [18]

$$A_J = (J_S / J_0)^n \quad (4.1.25)$$

where:

J_S = effective operating current density (user supplied MA/cm^2)
J_O = reference current density (1 MA/cm^2)
n = experimentally determined exponent (2)

Reference Distribution

A literature review identified consistent values for the acceleration coefficients, E_a and n, and the reference distribution statistics, μ_O and σ. Table 4.1-12 lists the pertinent parameters and references from which the values of E_a and n were derived. The most thorough work in understanding electromigration was done by Schafft[22] and associates. From this work, consistent values of E_a and n were determined to be 0.5 eV and 2, respectively. These values were determined for Al-1% Si metallization. This metallization system is expected to be the worst-case system for interconnect on VLSI/ULSI microcircuits, since pure Al is never used because of process considerations such as over-sintering of shallow junctions. Other metal systems, such as Ti-AL-TiW, do not readily electromigrate because of the heavier metal ions. (There is, however, concern that resistance changes may occur to cause performance problems which are difficult to quantify.)

In addition to the values of the acceleration coefficients, Schafft also developed the reference distribution statistics, $t_{O\ 50\%}$ and σ. The values of these statistics were determined to be 32.12 and 0.33 hours with associated errors of 2.38 and 0.04 hours, respectively, for an operating temperature of 175°C, a current density of 1 MA/cm^2, for all interconnect lengths greater than 800 μm. Worst-case estimates of $t_{O\ 50\%}$ and σ were obtained using

$$t_{O\ 50\%}\ (\text{worst case}) = t_{O\ 50\%} - 3 * \text{error}\ (t_{O\ 50\%}) \qquad (4.1.26)$$

$$\sigma\ (\text{worst case}) = \sigma + 3 * \text{error}\ (\sigma). \qquad (4.1.27)$$

Table 4.1-12
Observed Electromigration Parameter Values

Conditions	J (A/cm2)	n	Ea	t50 (hrs)	σ (hrs)	Temp (deg C)	ref
Al-Cu-Si Films	1E5 - 2E6	2	.5		.2 - .5	150 - 250	24
Al-Ti-W Stripes							25
w/thermal gradient	2.5E6				.52	185	
wo/thermal gradient	2.5E6				.34	185	
Constant Current		2	.43			125	26
	2E6			174	.79	150	27
				167	.73	150	
				465	1.1	150	
				126	.67	150	
				175	.8	150	
				120	.78	150	
				644	1.04	150	
				127	.84	150	
				175	.8	150	
				144	.77	150	
				567	1.12	150	
				126	.76	150	
			.4			150 - 250	20
Al-Si Alloy Films	6.6E5		.54		.23 - .65	< 230	28
Al-Cu-Si Films	1.6E6 - 2E6	2	.5		.2 - .5	195 - 250	24
Au-Cu Alloys	2E6			1600	1.4	220	41
				819	.42	220	
				525	.7	220	
				354	.73	220	
				15	.4	220	
Al-Poly Si Metal			.9			150 - 220	29
Al-Si Films							30
leakage		2.3	.9 +/- .1				
open		2.3	.5				
Al	2E6		.56 +/- .04			125 - 300	31
Ti-W / Al	1E6 - 4E6	2.06	.53			...	
Al /.5% Cu / 1% Si	2E6	1.7	.55			125	32
	< 1E5	1					33
	1E5 - 1E6	1.5					
	.45E6 - 2.88E6	2					
	1E6 - 2E6	4.5					

Observed Electromigration Parameter Values (CONTD)

Conditions	J (A/cm2)	n	Ea	t50 (hrs)	σ (hrs)	Temp (deg C)	ref
Small Grain	.55E6 - 2.08E6		.48			180	33
Large Grain	.5E6 - .2E6		.84			180	
Glassed Large Grain	.45E6 - .9E6		1.2			180	
Al	4E6	2			.56	125	34
Al	.333E6 & .242E6	2	.511	1039	.7	191	35
	.283E6 & .189E6	2	.525	2318	1	173	
	.268E6 & .179E6	2	.529	2672	.8	175	
Al / 1% Si	1E6	2	.5	32.12	.33	175	22

The conservative estimates of $t_{0\ 50\%}$ and σ were calculated to be 24.98 hours and 0.45 hours, respectively.

Since metals do not have an intrinsic defect density, the variance in lifetime is most probably due to process variations. It is noted that the variance for EM is much smaller than the variance for TDDB.

With the EM reference distribution statistics identified, the user must determine the acceleration factors for metal film temperature and current density to obtain the EM distribution statistics for the microcircuit in question. Figures 4.1-9 and 4.1-10 may be used to determine the temperature acceleration factor, A_T, and the current density acceleration, A_J, respectively. From the EM distribution statistics for the microcircuit, the user can calculate the probability of success, hazard rate, and effective hazard rate at any time t for EM. Alternatively, the user can use tables 4.1-13 and 4.1-14 to determine the probability of success and effective hazard rate at 10,000 hours given junction temperature and effective current density.

Figure 4.1-9 Temperature Acceleration Factor for EM

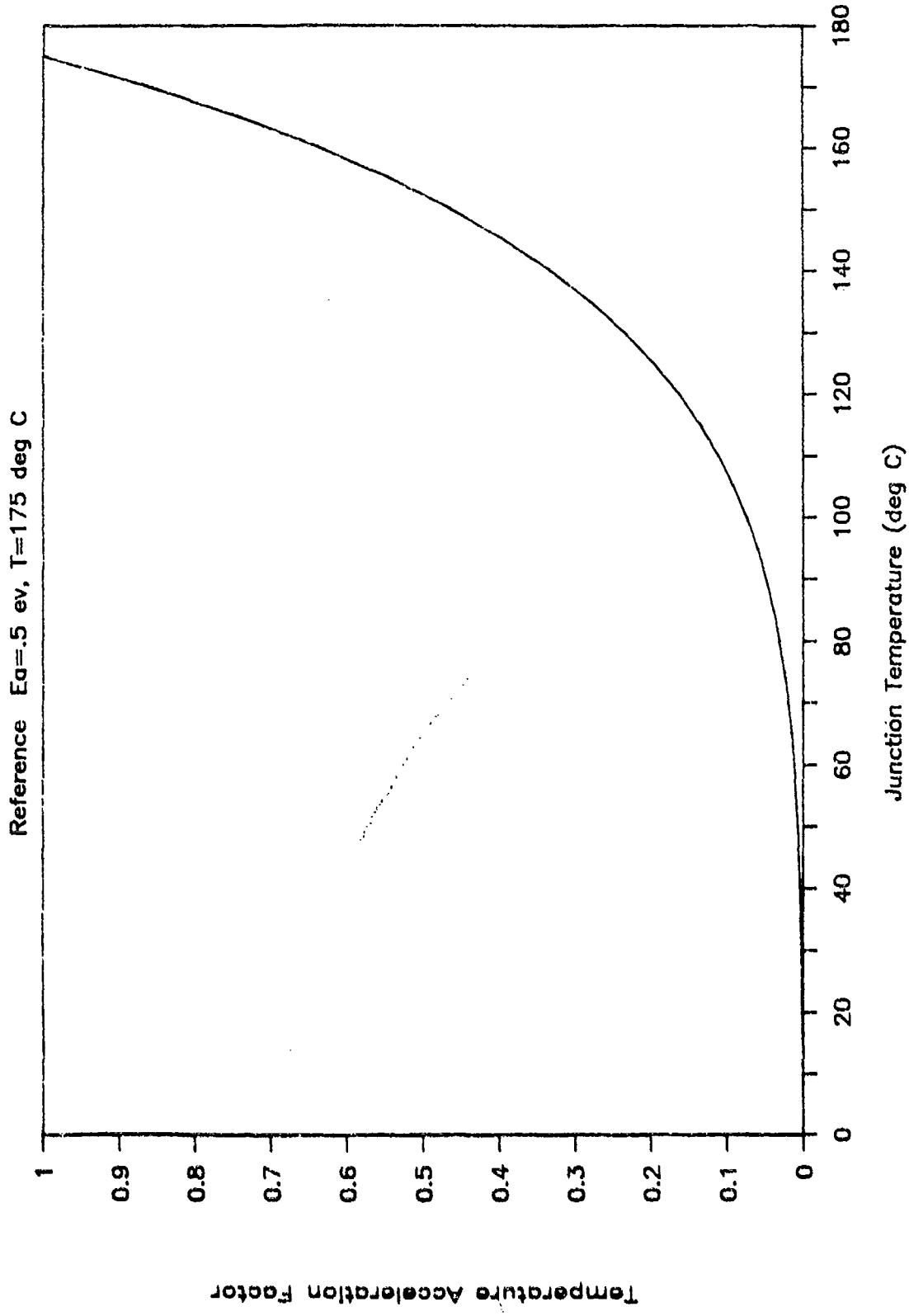
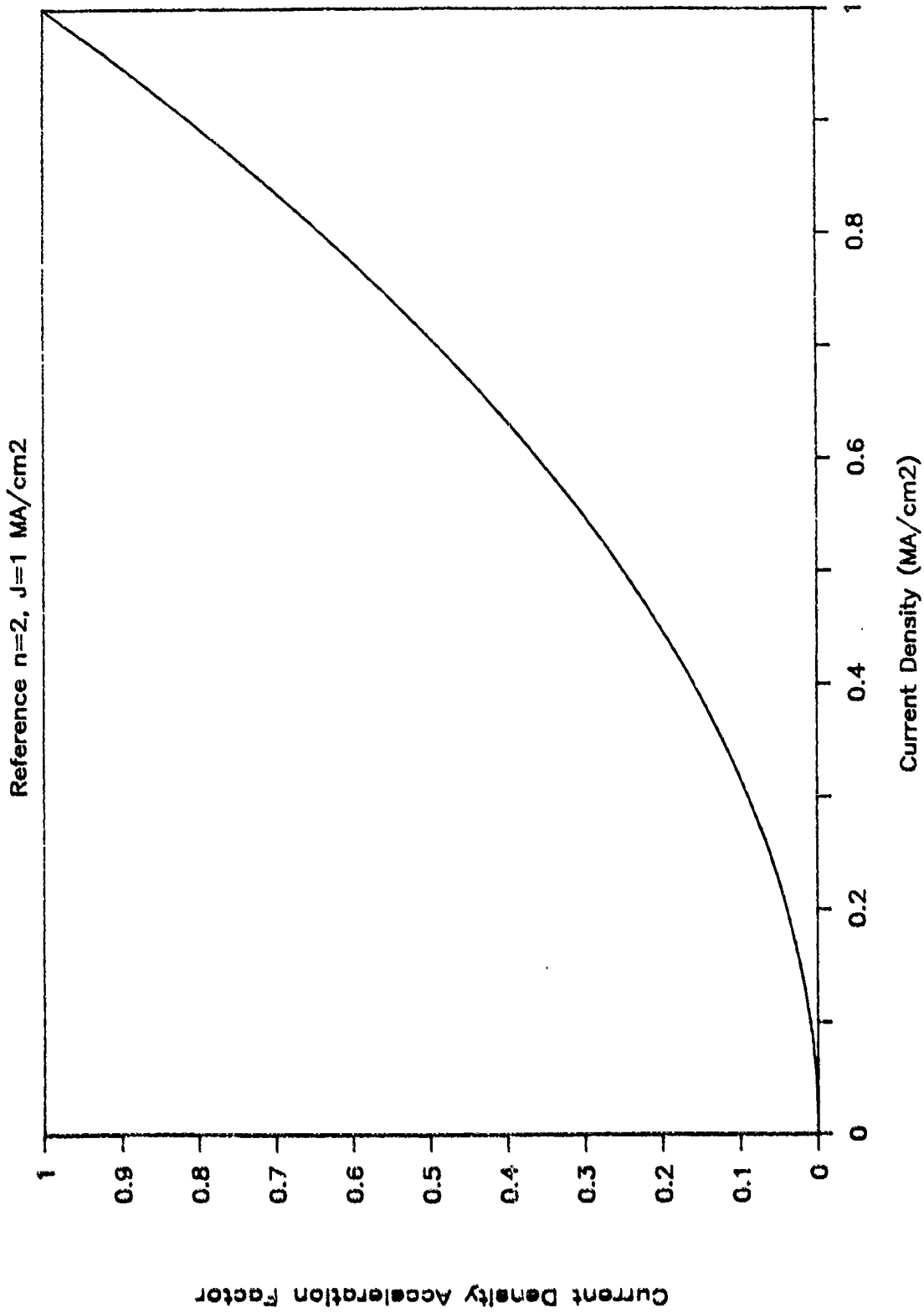


Figure 4.1-10 Current Density Acceleration Factor for EM



	Current Density (MA/cm2)														
T(C)	.04	.05	.06	.08	.10	.13	.17	.20	.25	.30	.40	.50	.60	.80	1.00	1.30
0.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
5.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
10.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
15.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
20.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
25.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.57309
30.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000
35.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000
40.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.98748	.00000	.00000
45.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000
50.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.98977	.00000	.00000	.00000
55.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000
60.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000
65.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99890	.00000	.00000	.00000	.00000	.00000
70.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000
75.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000
80.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000
85.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.97869	.00000	.00000	.00000	.00000	.00000	.00000	.00000
90.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
95.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99049	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
100.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
105.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00397	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
110.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
115.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
120.	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
125.	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
130.	1.00000	1.00000	1.00000	1.00000	.99945	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
135.	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
140.	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
145.	1.00000	1.00000	1.00000	.28800	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
150.	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
155.	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
160.	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
165.	1.00000	1.00000	.00009	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
170.	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
175.	1.00000	.50299	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000

Table 4.1-13 ELECTROMIGRATION: PROBABILITY OF SUCCESS AT 10000. HOURS

	Current Density (MA/cm2)															
T(C)	.04	.05	.06	.08	.10	.13	.17	.20	.25	.30	.40	.50	.60	.80	1.00	1.30
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	55.671
30.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000
35.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000
40.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	1.260	999.000	999.000
45.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000
50.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	1.028	999.000	999.000	999.000
55.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000
60.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000
65.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.110	999.000	999.000	999.000	999.000	999.000
70.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000
75.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000
80.	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
85.	.000	.000	.000	.000	.000	.000	.000	.000	2.155	999.000	999.000	999.000	999.000	999.000	999.000	999.000
90.	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
95.	.000	.000	.000	.000	.000	.000	.000	.956	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
100.	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
105.	.000	.000	.000	.000	.000	.000	552.893	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
110.	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
115.	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
120.	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
125.	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
130.	.000	.000	.000	.000	.055	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
135.	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
140.	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
145.	.000	.000	.000	124.481	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
150.	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
155.	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
160.	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
165.	.000	.000	927.293	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
170.	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
175.	.000	68.718	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000

Table 4.1-14 ELECTROMIGRATION: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS

4.1.3.3 Charge Injection/Hot Carrier Model

A literature review of articles written on charge injection/hot carrier failure modes resulted in three conclusions. First, charge injection is only a concern for MOS transistor channel lengths less than 1.5 um. Second, many authors make the distinction that charge injection is a design consideration rather than a reliability consideration. Third, the inconsistency in reported failures due to charge injection, either reported as microcircuit failures or laboratory test structure failures, reflects the inconsistency of microcircuit failures due to ionic contamination 15 years ago. At present, charge injection is not considered a wearout mechanism, but a quality/design factor.

4.1.3.4 Other Mechanism Models

The other mechanisms outlined in Table 4.1-3, including mobile ions, surface state shift, leakage, and latent ESD are considered assignable cause mechanisms. These mechanisms contribute to the early and middle life failure rate, outlined in section 4.1.2.

4.1.4 End-Life Prediction Models

With the contributing end-life failure mechanism models identified, these models must be addressed in terms familiar to the user. Figure 4.1-11 is a breakdown of the end-life failure mechanism models and the parameters which must be supplied to complete the model. The parameters highlighted by bold outlined boxes must be supplied by the user. The parameters shown in the remaining boxes have default values available if the user does not have sufficient knowledge about the microcircuit to supply actual values. Table 4.1-15 identifies the failure mechanisms that apply to the microcircuits in question. Only time-dependent dielectric breakdown (TDDB) and electromigration (EM) are considered end-life limiting failure mechanisms; therefore, the effective hazard rate for end-life predictions has the form

$$\lambda_{end}(t_0) = \lambda_{TDDB}(t_0) + \lambda_{EM}(t_0) \qquad (4.1.28)$$

where: $\lambda_{TDDB}(t_0)$ = effective hazard rate for TDDB at time t_0

$\lambda_{EM}(t_0)$ = effective hazard rate for EM at time t_0.

Figure 4.1-11

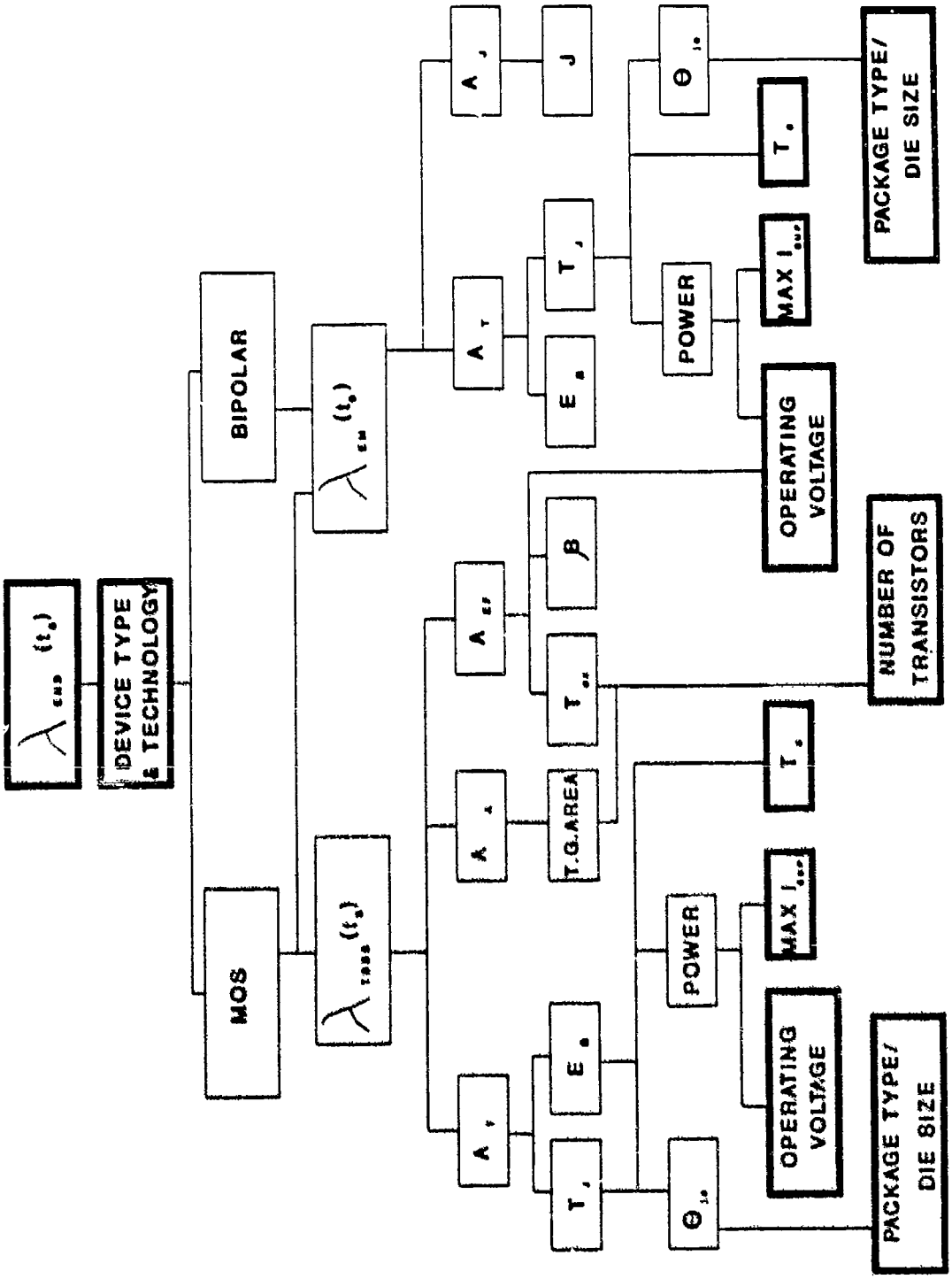

DEVICE TYPE & TECHNOLOGY
BIPOLAR
MOS
OPERATING VOLTAGE
NUMBER OF TRANSISTORS
POWER
MAX
PACKAGE TYPE/ DIE SIZE
T.G.AREA
J
β

Table 4.1-15 Electrical Failure Mechanisms

	Microprocessors		Gate Logic Arrays	
	MOS	BIPOLAR	MOS	BIPOLAR
1) Time Dependent Dielectric Breakdown	C		C	
2) Electromigration	C	C	C	C
3) Charge Injection	D		D	
4) Mobile Ions	A	A	A	A
5) Surface State Shifts	A	A	A	A
6) Latent ESD	A	A	A	A
7) Contact Resistance Change	A	A	A	A
8) Other Random Defects	A	A	A	A

Key: C indicates common cause failure mechanism
D indicates design consideration
A indicates assignable cause mechanism

For those microcircuits whose lifetimes are limited by TDDB, the user will use representative sample Tables 4.1-10 and 4.1-11 (more comprehensive tables are available in Appendix D). To identify which tables are appropriate, the user must know the total transistor gate oxide area on the microcircuit. If the user does not know total gate area, Table 4.1-16 provides default area values dependent upon the number of transistors in the microcircuit. Alternatively, the dependence of total gate area on transistor count is shown graphically in figures 4.1-12 and 4.1-13 for MOS microprocessor devices and MOS digital and linear devices, respectively. The data in these figures is bounded by an upper (worst-case) limit defined by

$$A = \log\left(4 * TR * 10^{-0.744 * (\log(TR) - 5.50)}\right) \ (\log\ \mu m^2), \qquad (4.1.29)$$

for MOS microprocessor devices, and

$$A = \log\left(6 * TR * 10^{-0.580 * (\log(TR) - 5.78)}\right) \ (\log\ \mu m^2), \qquad (4.1.30)$$

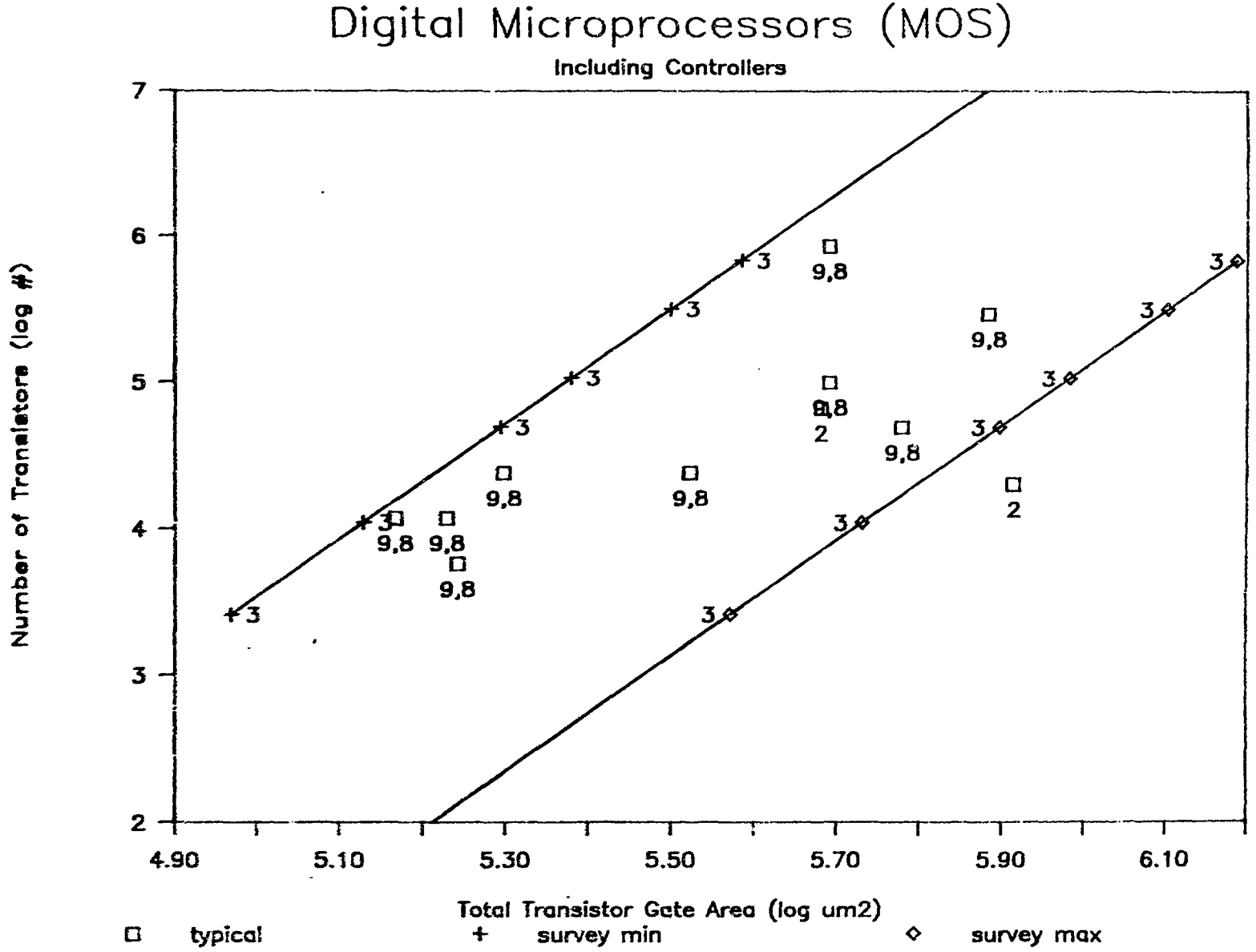
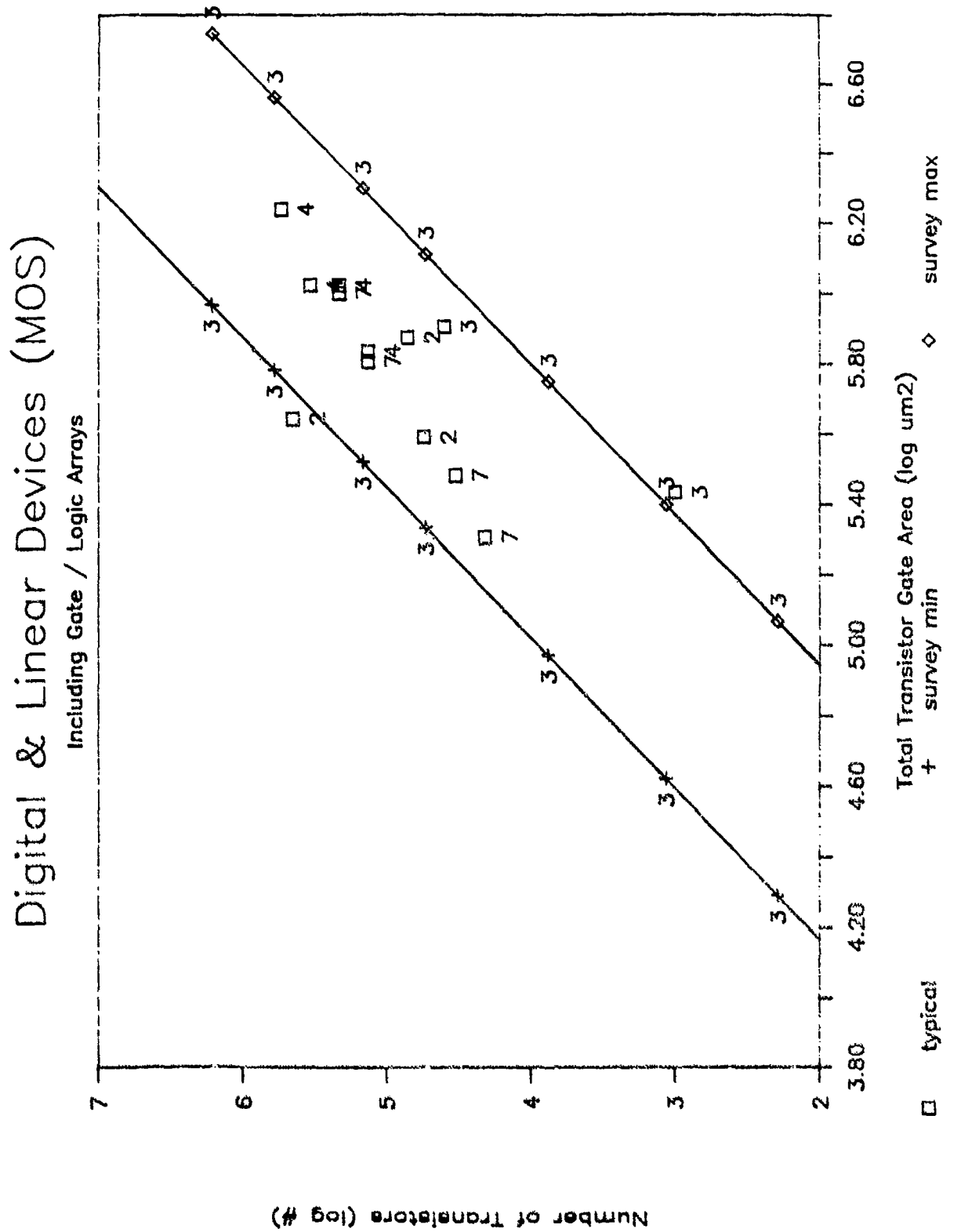

Digital Microprocessors (MOS)
Including Controllers
Number of Translators (log #)
7
6
5
4
3
2
4.90
5.10
5.30
5.50
5.70
5.90
6.10
Total Transistor Gate Area (log um2)
□ typical
+ survey min
◇ survey max

Figure 4.1-12

Figure 4.1-13


Digital & Linear Devices (MOS)
Including Gate / Logic Arrays
Number of Tranelators (log #)
Total Transistor Gate Area (log um2)
3.80
4.20
4.60
5.00
5.40
5.80
6.20
6.60
2
3
4
5
6
7
□ typical
+ survey min
◇ survey max

for MOS digital and linear devices,

where TR = number of transistors on the device in question.

Next the user must determine the electric field stress given the operating voltage. The electric field stress, E_S, is given by

$$E_S = .1(V_{op}/t_{ox}) \text{ (Mv/cm)}, \tag{4.1.31}$$

where:

V_{op} = operating voltage (user supplied V)

t_{ox} = oxide thickness (user supplied K$\mathring{A}$)

Again, if the user does not know oxide thickness, by knowing the number of transistors in the microcircuit, the user can obtain a default value for oxide thickness from Table 4.1-17. Alternatively, the dependence of oxide thickness on transistor count is shown graphically in figures 4.1-14 and 4.1-15 for MOS microprocessor devices and MOS digital and linear devices, respectively. The data in these figures is bounded by a lower (worst-case) limit defined by

$$T_{ox} = 10^{-0.406 * (\log(TR) - 3.68)} \text{ (K}\mathring{A}\text{)}, \tag{4.1.32}$$

for microprocessor devices, and

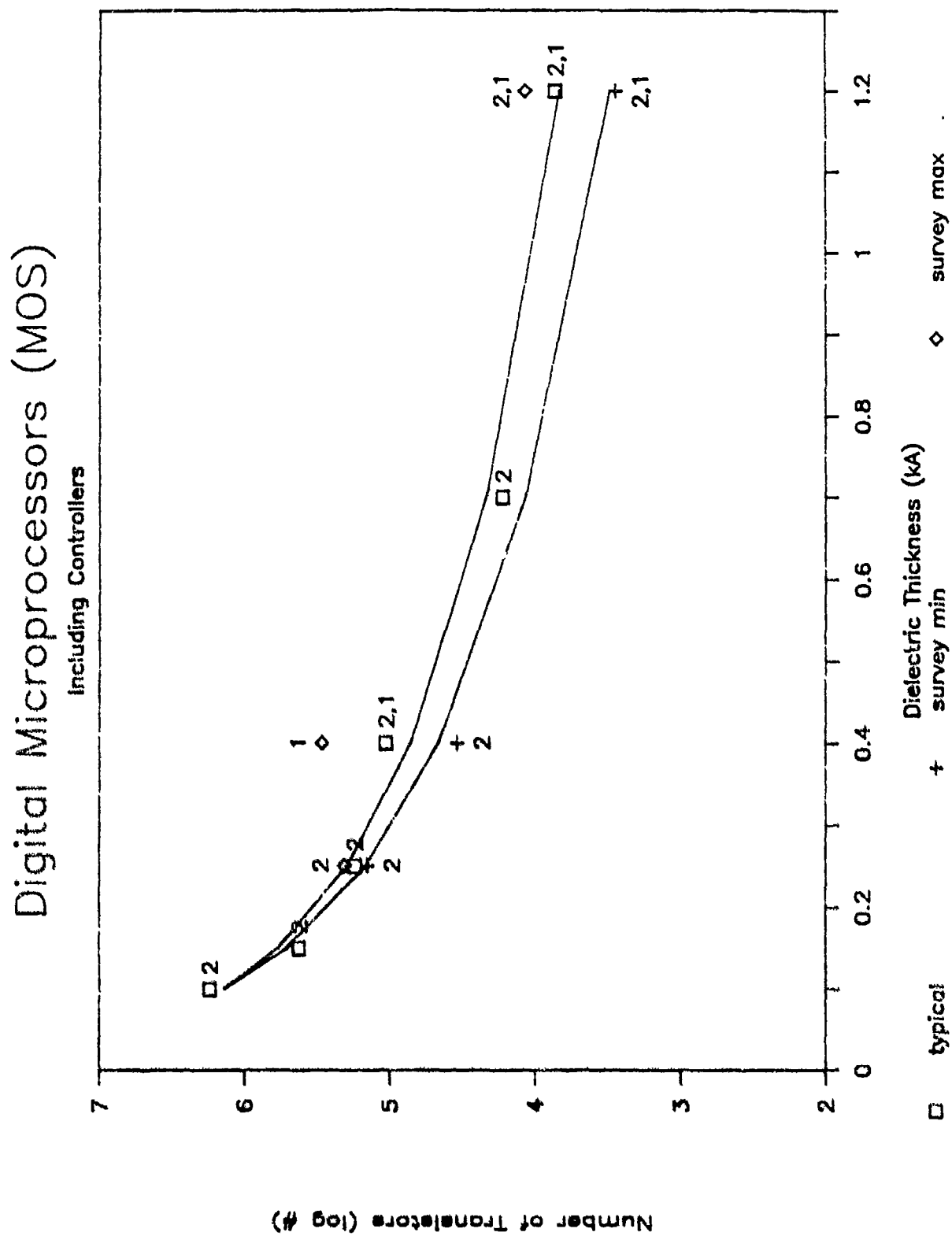
$$T_{ox} = 10^{-0.296 * (\log(TR) - 3.14)} \text{ (K}\mathring{A}\text{)}, \tag{4.1.33}$$

for MOS digital and linear devices,

where TR = number of transistors on the device in question.

After identifying the electric field stress, the user must determine the appropriate dielectric temperature stress. A calculated junction temperature, T_J, results in the worst-case approximation of the dielectric

Figure 4.1-14


Digital Microprocessors (MOS)
Including Controllers
Number of Tranelators (log #)
Dielectric Thickness (kA)
typical
survey min
survey max
7
6
5
4
3
2
0
0.2
0.4
0.6
0.8
1
1.2

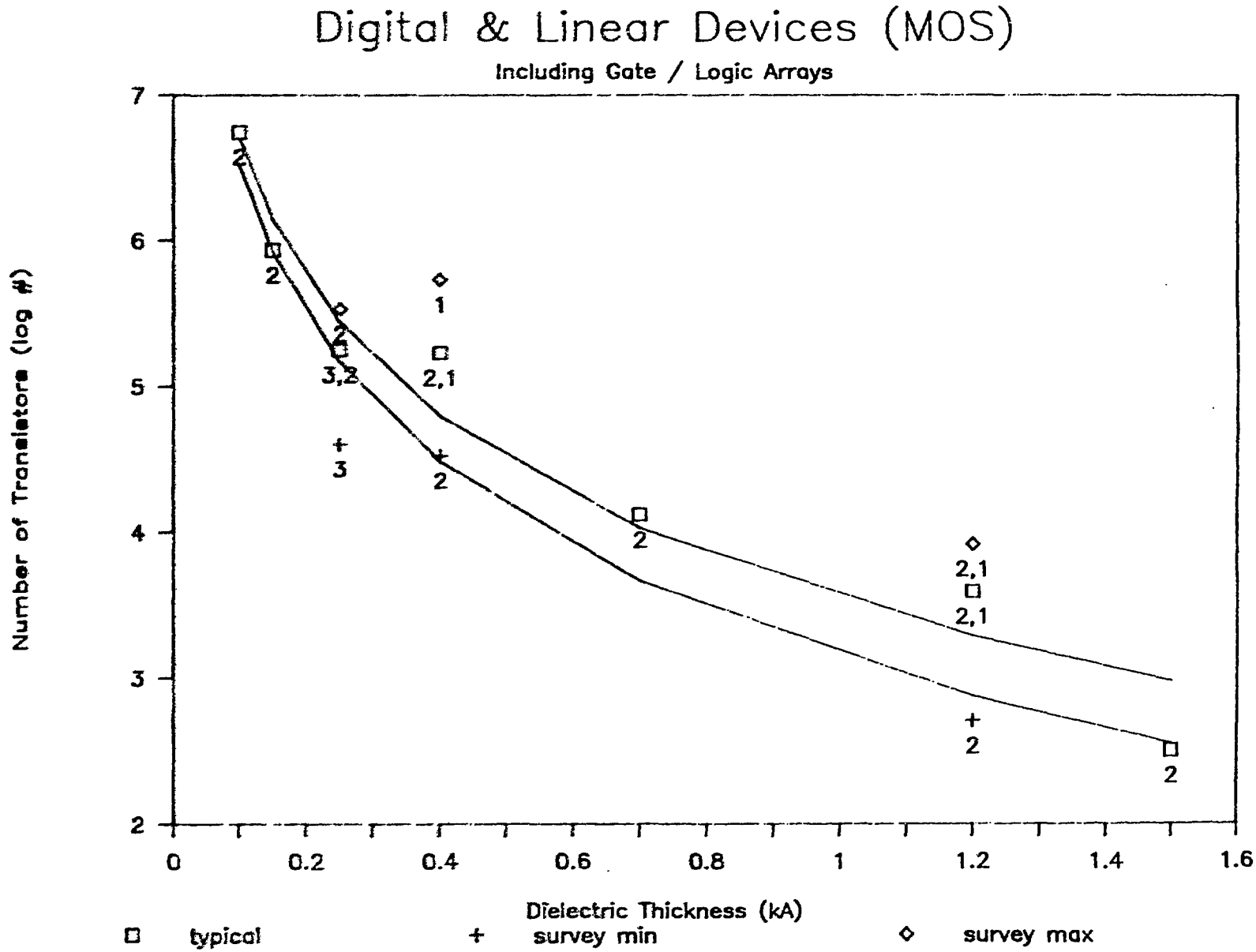

Digital & Linear Devices (MOS)
Including Gate / Logic Arrays
Number of Translators (log #)
7
6
5
4
3
2
0
0.2
0.4
0.6
0.8
1
1.2
1.4
1.6
Dielectric Thickness (kA)
typical
survey min
survey max

Figure 4.1-15

temperature. The value of the junction temperature may be supplied by the manufacturer or may be developed in a standard fashion, where

$$T_J = T_{case} + \theta_{JC} * P \ (°C), \qquad (4.1.34)$$

where:

T_{case} = operating case temperature (user supplied °C)
θ_{JC} = junction to case thermal resistance (user supplied °C/W)
P = worst-case power (user supplied W).

Once the total transistor gate oxide area, oxide thickness, and junction temperature have been identified, the user can determine the associated probability of success or hazard rate for the microcircuit due to TDDB.

For those microcircuits whose lifetimes are limited by electromigration, the user will use Tables 4.1-13 and 4.1-14. If the user does not know the maximum current density through the metal on the microcircuit, a default value of 0.125 MA/cm^2 should be used. (See Appendix B for the derivation of this default value.) The appropriate metal film temperature stress is determined in a similar fashion as the temperature stress for TDDB. Once the current density and junction temperature have been identified, the user can determine the associated probability of success or hazard rate for the microcircuit due to electromigration.

It is noted here that many microprocessors utilize on-chip static RAM. The contribution of the failure rate of this SRAM to the total microprocessor failure rate is insignificant. Since the technology used to fabricate the SRAM transistors is similar to the technology used to fabricate the processor transistors, the mechanisms which result in end-life failures are similar; therefore, the SRAM, which comprises only 1% to 5% of the total active circuitry of the microprocessor, has minimal impact when predicting the total failure rate of the microprocessor.

Table 4.1-16 Total Transistor Gate Area (log μm^2)

Complexity (# of trans.)	Digital Microprocessors (including Controllers)	Digital and Linear Gate / Logic Arrays
100 - 500	5.39	5.24
500 - 1k	5.47	5.37
1k - 5k	5.64	5.67
5k - 10k	5.72	5.80
10k - 50k	5.90	6.10
50k - 100k	5.97	6.23
100k - 500k	6.15	6.52
500k - 1M	6.23	6.65
1M - 5M	6.41	6.95
5M - 10M	6.48	7.08

Table 4.1-17 Dielectric Thickness (KÅ)

Complexity (# of trans.)	Digital Microprocessors (including Controllers)	Digital and Linear Gate / Logic Arrays
100 - 500	4.81	2.17
500 - 1k	2.50	1.35
1k - 5k	1.89	1.10
5k - 10k	0.98	0.68
10k - 50k	0.74	0.56
50k - 100k	0.39	0.35
100k - 500k	0.29	0.28
500k - 1M	0.15	0.17
1M - 5M	0.11	0.14
5M - 10M	0.06	0.09

4.2 MEMORY DEVICES

4.2.1 Database

Literature Survey - This was one of the first activities conducted for the modeling task, and, although most sources were identified early in this effort, it continued throughout the program. A total of 63 articles and papers from trade journals and symposiums were identified as being relevant to memory reliability modeling. They were reviewed and filed. Most of the literature was related to non-volatile memories (e.g., EPROMs and EEPROMs), which is appropriate since these device types were recognized from the start of the modeling task as ones that required the most study. Others were specific to device types such as SRAMs and DRAMs, or were directed towards various technology areas (for example, CMOS and BiMOS). Relatively little literature on older, less complex technologies and devices such as MOS ROMs, bipolar ROMs/PROMs/PLAs/PALs was found during the search. Direct and indirect contributions by this literature to the memory model development will be noted, as appropriate, throughout this section of the report.

The primary use of the literature was to aid in determining the true failure modes and mechanisms of the device types investigated and the relative contribution of these modes and mechanisms to the overall failure rates of these devices. The literature was used to a limited degree in the evaluation of the sensitivity of device failure rates to parameters such as temperature and complexity.

Industry Contacts - A key source of information for the modeling task was the semiconductor industry. At the start of the program, questionnaires were sent to a large number of companies requesting whatever support that could be provided. For memory devices, 11 companies expressed initial interest in the project, with 9 of them ultimately providing various degrees of information. These companies were exclusively semiconductor device manufacturers. The industry information was used in conjunction with the literature data to identify the applicable failure modes and mechanisms for memory devices. This information included life test data and device parameter information, and was

also helpful during development of the actual models.

The following is a list of the industry contacts that provided data and answered questions regarding memory devices:

Raytheon	National Semiconductor
Intel	Advanced Micro Devices
Seeq	Signetics
Xicor	Atmel
Inmos	

Most of the data collected from the various manufacturers was in the form of already published data books, reliability reports and pamphlets. The life test data that was gained from the manufacturers was collected and put on a computer database for reference throughout the project. See Appendix E for the life test results. It should be noted that a significant amount of requested information could not be provided by the manufacturers because of manpower and/or data confidentiality constraints. As with the literature search, the largest portion of the information gained from the manufacturers related to non-volatile memories.

4.2.2 Model

4.2.2.1 Approach/Mechanism Identification

In the development of the memory model, the various sources of information described earlier in this section (literature, manufacturer data, in-house experience) were used to identify the applicable failure mechanisms involved with the various device types. These mechanisms were then evaluated individually to determine whether they are defect-related or intrinsic to the device. This information provided guidance in the overall approach to the development of the actual model in addition to the form that the model ought to take. Table 4.2-1 presents the results of the failure mechanism investigation task that is documented in this section.

Table 4.2-1 Memory Failure Mechanisms

	Flash EEPROMs UVEPROMs FG MOS PROMs FG MOS PALs	FLOTOX & Tex-Poly EEPROMs	MNOS EEPROMs	Bipolar ROMs/PROMs and PALs	MOS ROMs	MOS SRAMs	Bipolar SRAMs**	DRAMs
Electron Trapping in Oxide	I*	I	I*	*	*	*	*	*
Time Dep. Dielectric Breakdown	I	I	I	*	I	I	*	I
Oxide Defect - Contamination	D	D	D	*	D	D	*	D
Oxide Defect - Pinholes, faults	D	D	D	*	D	D	*	D
Silicon Defect	D	D	D	D	D	D	D	D
Metallization Defect	D	D	D	D	D	D	D	D
Electromigration	I	I	I	I	I	I	I	I
Intrinsic Charge Loss	I*	I*	I*	NA	NA	NA	NA	NA
Hot Carrier Injection	*	*	*	NA	NA	I*	NA	I*
Soft Errors	*	*	*	NA	NA	See Text	NA	See Text

I - Intrinsic failure mechanism
* - Not a significant contributor
** - See discussion for BiMOS

D - Defect induced failure mechanism
NA - Not Applicable
FG MOS - Floating Gate Metal Oxide Semiconductor

UVEPROMs, Flash EEPROMs

Flash EEPROMs are treated similarly to EPROMs in this analysis. Flash EEPROMs use the same CHE (Channel Hot Electron) programming mechanism as do UVEPROMs, and use the same one transistor/cell approach. The primary difference between the two is that Flash cells incorporate a thin floating gate-source or - drain gap to allow for a Fowler-Nordheim tunneling erase mechanism (UVEPROMs use a UV light photocurrent erase mechanism).[45,67]

The life test data reviewed for UVEPROMs showed the primary failure mode to be storage gate charge loss, with a secondary mode of charge gain. These modes result in the lowering or raising of the cell threshold voltage, thus narrowing the cell read margin. The literature search also supported the selection of these modes as the most prevalent.[47,48,49,71] Either of the two modes can be caused by ionic contaminants or defects in the gate oxide. A defect in the oxide or an induced breakdown of the oxide can cause a pathway for stored charge to leak off, or it can attract unwanted electrons under read bias. Charge gain or loss are the primary causes of retention failures (a cell changing state on its own over time) in these devices. The only other failure modes found in the UVEPROM life test data collected were parametric test failures, with no hint as to the mechanism(s) involved. The small amount of Flash EEPROM life test data found also indicated charge loss as the primary failure mode.[45] Charge gain can be caused by the trapup of electrons in the gate oxide as a consequence of movement of electrons through the gate oxide during programming and erasure. This must be considered for devices (standard EEPROMs) that experience a high number of erase/reprogram cycles. However, UVEPROMs and Flash EEPROMS are expected to experience a much lower number of cycles during their lifetime; therefore the failure rate contribution by charge trapup is considered to be negligible.

The phenomenon of intrinsic charge loss in UVEPROMS/Flash EEPROMs has been identified in literature,[45,47] and may be due to the detrapping of electrons trapped during erase;[47] however, evidence strongly suggests that the amount of degradation is limited in nature (the total charge lost by a storage transistor in this manner is not enough to cause a failure in an

otherwise good cell) and is a negligible contributor to UVE/Flash failure rates.

The failure modes of spurious programming and erasure have been identified in literature[45,49] for both UVEPROMs and Flash EEPROMs. Spurious programming is a defect-induced failure mode resulting in unwanted cells being programmed. Spurious erasure is also defect-induced and results in unwanted cells being erased during the program cycle.

As mentioned, charge loss may be caused by a breakdown in the oxide. A high electric field is present across the gate dielectric during the programming step for both UVEPROMs and Flash EEPROMs. Time Dependent Dielectric Breakdown (TDDB) is greatly accelerated by increased voltage and has been identified by a number of sources as being a contributing failure mechanism for all MOS devices, particularly as geometries get smaller and smaller. This mechanism was therefore identified for further analysis during the development of the model. Electromigration, the other intrinsic failure mechanism, was also selected for further study. Both of these mechanisms influence the reliability of the peripheral circuitry, as do the defect-related mechanisms found in other IC types.

Because of the information found in the various literature sources, the reliability of Flash EEPROMs and UVEPROMs was considered to be equal during the initial stages of the model development task, at least when the total number of reprogram cycles during the life of the part is 100 cycles or fewer.

Refer to the SRAM paragraphs in this section for a more general discussion regarding HCI (Hot Carrier Injection). None of the literature researched named this as a significant failure mode for Flash and UVEPROMs. This can be compared to the charge trapup mechanism as (at least for the array storage transistors) these devices use hot injection as a programming mechanism. For this modeling effort, HCI was considered to be an insignificant contributor, provided that a limit is placed on the number of reprogram cycles (about 100 cycles).

Soft errors like HCI have become more of an issue with memories as geometries have been reduced. See the DRAM paragraphs in this section for a further discussion on this mechanism. None of the literature reviewed considered this to be a relevant failure mechanism for nonvolatile memories. An alpha particle striking the floating gate loses little of its energy there and creates fewer carriers, and few of these escape over the floating gate's high energy barrier.[44]

MOS PLAs, PALs, and PROMs using UVEPROM style cells in place of fuses were considered equivalent to UVEPROMs with respect to reliability during the development of the model, the primary difference being that these devices are one - time programmable.

EEPROMS

This class of device consists of all EEPROMs except for "Flash" (discussed earlier), and MNOS (Metal Nitride Oxide Semiconductor), which will be discussed later. It can further be broken down into two types: FLOTOX (Floating gate Tunnel Oxide), and Textured Polysilicon (Tex-Poly). Both types store charge on a floating gate that is isolated by oxide and use Fowler-Nordheim (F-N) tunneling for both programming and erasure. FLOTOX devices use a thin tunnel oxide (generally less than 100 Å) to achieve the F-N tunneling. Textured-Poly devices use a thicker tunnel oxide (greater than 150 Å) and achieve tunneling through enhanced localized E-fields created by a textured ("bumpy") Si-SiO2 interface. The cell structures for these two EEPROM types also differ: FLOTOX generally uses two transistors per cell (one for storage and one for a support transistor), whereas Tex-poly cells use a single, more complex storage transistor.[44,67,68] Both of these EEPROMs may experience thousands of reprogram cycles during their lifetime. The literature search indicated a strong relationship between reprogram cycling and device failure rate. Two primary failure mechanisms are associated with this cycling: oxide breakdown and charge trapping in the tunnel oxide (trapup). Both of these mechanisms can result in memory retention failures or stuck bit failures in the memory array, depending upon the degree of degradation. The literature also indicated that the two EEPROM types have very different sensitivities to

reprogram cycling and the associated failure mechanisms.[44,68,72] For this reason, part of the EEPROM modeling approach was to treat these two EEPROM types separately and incorporate a cycling relationship into the model. Other failure mechanisms such as oxide breakdown can occur with little or no cycling and can be caused by things such as oxide pinholes or contaminants, just as with other IC types. This was supported by a small amount of life test data (it does not include any reprogram cycling) that was collected. The failures that occurred during this testing (for which the cause could be determined) were caused by either contaminants or oxide breakdown. Time dependent dielectric breakdown was incorporated into the modeling approach for EEPROMs, as was electromigration. These two mechanisms are intrinsic to EEPROMs by the nature of their construction and may be significant under certain circumstances (for instance, very small geometry devices). Intrinsic charge loss was not mentioned by any of the literature researched, nor did it appear in any life test data. It is therefore being treated as it is for UVEPROMs and is not considered to be a significant contributor to the failure rate of the device.

MNOS Metal Nitride Oxide Semiconductor EEPROMs

This device type gained early popularity at the start of EEPROM device development but has in recent years been used much less frequently by industry as compared to FLOTOX and Textured-Poly. MNOS devices store charge at a nitride layer as opposed to storage on a floating gate. This permits a simpler cell structure than that of either FLOTOX or Textured-Poly. The tunnel oxide used for MNOS is thinner than that of FLOTOX, making the device more susceptible to any defects or contaminants in that oxide layer, and it also results in loss of data retention over a period of time. The literature also indicates that MNOS EEPROM retention characteristics are degraded by repeated reprogram cycles and are more susceptible to corruption of cell contents by read operations (read disturb)[74] than to other EEPROMs. Because the tunnel oxide is very thin, charge trapup in the oxide should not be a contributing mechanism, and none of the literature researched considered trapup in the oxide to be a significant problem; however, cycling can introduce electron migration into the nitride layer after being trapped at the $Si-SiO_2$ interface,[75] although this effect seems to be significant only at very high levels of

cycling (in excess of 1x10E6 cycles) and is influenced by device design and process parameters. The other failure mechanisms such as silicon defects, time-dependent dielectric breakdown, and electromigration were considered to be contributing failure mechanisms during the model development program just as they were for the other device types. No MNOS life test data was found during the model development program.

Bipolar ROMs, PROMs, PALs

This group includes PALs (Programmable Array Logic), PLAs (Programmable Logic Array), and HALs/MLAs which are hard-wired versions of the first two. Together with bipolar ROMs/PROMs, these devices are very similar in that they consist of an array of fuses (if programmable) supported by conventional bipolar logic. Very little literature data was found that directly addresses the reliability of these devices. The initial approach during the memory model development program was to separately treat two aspects of the programmable versions of these devices: the fuses that make up the array, and the peripheral logic. A substantial amount of life test data was found from manufacturer sources. There were zero failures (due to either a defect-induced or intrinsic failure mechanism) attributed to fuses. Conversations with representatives from device manufacturers also supported the assertion that fuses are not significant contributors to device failure rate. For this reason, a failure rate for fuses was not considered during the development of the model. This left the supporting peripheral circuitry in addition to the simple diode structures that reside in the array. No failures due to oxide defects were found in the life test data, which is appropriate since these are bipolar devices. The failure mechanisms of electromigration, silicon defects, and metal defects were judged to be the contributors to the overall device failure rate. This was supported by the life test data, and these mechanisms were considered during the development of the model.

MOS ROMs

Members of this class of devices are MOS-based with a hard-wired array and

are the simplest of the memory devices modeled. As with PROMs/PLAs, virtually no literature regarding the reliability of this device type was available; however, the life test data collected indicated that the failure modes of silicon, oxide, and metal defects were contributors to the failure rate of the device. Electromigration and TDDB were also chosen for evaluation during the development of the model as these are intrinsic to the structures found on MOS ROMs.

Static RAMs

These devices are implemented using bipolar, MOS, and (more recently) BiMOS (which combines the two technologies on one chip). Memory contents are stored as memory-cell transistors that are constantly biased "on" or "off". They do not incorporate exotic charge storage structures as are found in UVEPROMs or EEPROMs, and in that respect they may be compared to more conventional logic devices. MOS versions of these devices can fail because of defects in the oxide (causing threshold shifts or leaky/shorted FETs), silicon or metal defects, or contaminants.[76,77] This is supported by the life test data collected, which identified FET leakage, oxide and metal defects among the failure causes. Time Dependent Dielectric Breakdown was considered to be a possible contributor to the MOS SRAM failure rate because it is intrinsic to the technology. For both bipolar and MOS technologies, electromigration was selected for further analysis during the model development task, as it was for all memories.

The phenomenon of Hot Carrier Injection (HCI) has been identified in literature as a potential MOS SRAM failure cause.[50,76] HCI occurs when available carriers gain energy as they move through the E-field associated with the FET channel. A sufficiently high field may cause some of these carriers to be injected into the gate dielectric, thus influencing the threshold voltage of the FET. This mechanism is accelerated by lower temperatures and higher voltages and becomes an issue as device geometries are scaled down without any scaling of the supply voltage used to operate the device. None of the literature contained data hinting at the percent contribution of HCI failures to the overall failure rate of the device, and the life test data collected

showed no HCI failures. Although this can be considered an intrinsic mechanism, it can be minimized or eliminated by special design or processing techniques.[50] There is also evidence that HCI has a self-limiting effect, at least for NMOS structures,[60] which makes it difficult to accurately model any failure rate contribution by the mechanism. This mechanism was not considered for modeling during the modeling task. Also refer to the VHSIC/logic section of this report.

Although no failure rate data was found either in the literature search or in the available life test data regarding BiMOS reliability, for the purposes of the modeling effort, this technology was considered to have some failure rate contribution by the failure mechanisms identified independently for both MOS and bipolar SRAMs.

DRAMs

These devices store data as parasitic capacitance in a specialized one-transistor memory cell. This charge-storage structure has built-in leakage, and therefore requires frequent "refreshing" or voltage pulse application, which is done automatically on the device. The simplicity of the DRAM cell allows it to be much smaller than a SRAM cell, which requires 4 or 6 transistors to implement a cell. The available literature indicated that the various defect mechanisms identified for other devices are also valid for DRAMs.[78,79] Time Dependent Dielectric Breakdown was also considered to be a potential contributor; this is also supported by the literature.[78]

Hot Carrier Injection is an issue with DRAMs, as it is for SRAMs. DRAMs are more susceptible than SRAMs because some internal circuitry can temporarily raise the voltage on part of the chip to relatively high levels.[58] The literature indicated that hot carrier stress can potentially affect parameters such as retention time, subthreshold leakage currents, and substrate current, which may cause device failure depending upon the application and degree of degradation.[57,58] Life test data that was collected was very limited for DRAMs but did not identify HCI as a failure cause. As with SRAMs, HCI effects can be minimized or eliminated by careful design and process techniques. Also

refer to logic/VHSIC section of this report. During the model development task, HCI was not modeled as a contributing mechanism because of its dependence on design, process, and application parameters.

Soft Errors (non-permanent failures) are also an issue with DRAMs. They are caused by electrical transients or particle radiation that upset charge levels within the device, typically affecting one bit.[80,81,82] This mechanism is more of a problem for DRAMs than SRAMs because of the simplicity of the memory cell and the need to constantly refresh the parasitic capacitance in each cell. It has become progressively more of a problem as DRAM geometries have been decreased to permit 2 Mbit and larger device capacities, which in turn results in decreased normal operating charges within the device. The difficulty of modeling the soft-error failure rate is due to the number and nature of influencing parameters and the lack of any empirical data. Soft errors may be caused by solar or cosmic radiation particle strikes, alpha particles emitted by the package of the device, or electrical transients. The factors that need to be accounted for when modeling this mechanism include:

- System application (Space, Airborne, Etc.)
- If airborne, system operating altitude, and possibly latitude
- Degree of external radiation shielding related to the system
- Memory cell dimensions
- Cell construction technique (specialized design to minimize susceptibility)
- Type of packaging used in the memory device
- Any error correction circuitry internal or external to the device

Because of the large amount of effort required to adequately model soft-error failures, they were not modeled during this project.

4.2.2.2 Model Development

Development of reliability prediction models for memory devices commenced once the applicable memory failure mechanisms were identified in the first phases

of the program. Two objectives were kept in mind during the development process:

- Make the model representative of what is physically causing failure.
- Make the model user-friendly, i.e., require only easily-found user input parameters.

A few observations regarding the memory devices to be modeled were made that helped to define the form of the model. One observation is that the basic technologies and processes used to fabricate memory devices are very similar to those of logic devices, especially when one looks at the peripheral circuitry of the memory as opposed to the array. Based on this, close coordination with the logic/VHSIC model development task was deemed to be desirable. Another observation is that the primary functions required to be performed on a memory circuit are basically the storage of data and the transfer of this data into and out of the storage. These two functions are segregated physically on the device in the form of the memory array and the interface or peripheral circuitry.

A basic approach used in the development of the model was to use the superposition approach. For the memory model, this requires analysis of the causes of failure individually, determining the contribution of each of these causes to the overall device failure rate, then adding the contributions together, which yields the device failure rate. It should be noted here that, for the purposes of the memory model discussion, the term "device" actually refers only to the "die", or chip, failure rate. This failure rate is added to the package failure rate in the final memory model. Refer to the package model section for the package failure rate determination.

This section will address the modeling of the applicable failure mechanisms individually and then present the final form of the model.

Electromigration

This failure mechanism was identified as being a potential failure rate

contributor for all memory devices. As part of the logic/VHSIC modeling task, a deterministic model representing electromigration was developed (see section 4.1.3.2). This same model is used to represent the electromigration failure rate for memory devices.

Because of the failure distribution determined as part of the electromigration modeling task, it is used here as essentially a "go-no go" check. Given a current density (such as the default value of .125 MA/cm^2), the resultant probability of success is basically either 1.000 or zero. Therefore, it is not considered an additive contributing failure rate to the overall model. The user must only check the operating junction temperature in addition to either the known current density or the default value in order to determine the acceptability of using the device in that application.

Time Dependent Dielectric Breakdown

Earlier in the approach/failure mechanism section, this was identified as a contributing failure mechanism for all MOS devices. To model the effect of this failure mechanism on memory device reliability, the TDDB modeling effort as part of the logic/VHSIC model development task was used as a basis (also see section 4.1.3.1). A basic assumption made here is that the oxides used for memory devices are the same as the oxides used for logic devices, which is a reasonable assumption. To determine λ_{TDDB} (the failure rate due to TDDB), some physical parameters of the device must be known. These are: total gate oxide area, gate oxide thickness, oxide electric field, and temperature of the oxide (or T_J).

At the start of the λ_{TDDB} modeling effort for memories, the approach was taken to evaluate the memory array and peripheral circuitry separately. This was done because for some memory devices the physical parameters required differ significantly between the array and periphery. So, for some device types, the total λ_{TDDB} equals the λ_{TDDB} (array) added to the λ_{TDDB} (periphery). For FLOTOX and Tex-Poly EEPROMs, only the λ_{TDDB} for the periphery was considered, since the array oxide failure rate due to voltage stress is assumed to be accounted for by the reprogram cycling failure rate

model (see the Trapup section). The various manufacturer sources were asked to provide data regarding oxide thickness and area. Based on the data provided by the manufacturers, tables were developed that show the parameter values to be used for each memory device. A range is given for each device capacity value. If the user does not know the value for the device, then the most conservative value in the range provided is used (thinnest oxide, or largest gate oxide area). These values are shown in Tables 4.2-2 through 4.2-3.

TDDB Discussion

In most cases for memory devices, the resultant failure rate due to TDDB turns out to be negligibly small (for the typical 5 V operation). The exception to this is for the thinner oxide devices that experience relatively high field stress. In general, the memory TDDB failure rate is insignificant for an applied voltage of 5 V or less.

The TDDB model presented here was determined to be inadequate for modeling the oxide failure rate due to programming stress. This affects the UVEPROM, Flash, MNOS, and FG PROM arrays, and the portion of EEPROM periphery circuitry that is exposed to a high programming voltage. The programming stress condition is characterized by a very high field stress for a very short period of time. Using the TDDB model to calculate the failure rate due to programming results in very high hazard rate values that are not valid when compared to the actual experience that the industry has with reprogrammable devices.

The evidence gained during the memory reliability modeling effort suggests that oxide failures due to programming on UVEPROMs, Flash EEPROMs, and MNOS EEPROMs are primarily due to either contaminants in the oxides, or microscopic physical faults in the oxide itself that precipitate failure upon repeated pulses of high electric fields. For this model, the cycling failure rate for the devices just mentioned will be considered to be zero, providing that a limit of 100 cycles is not exceeded. The great majority of UVEPROM, Flash EEPROM, and MNOS EEPROM applications do not require in excess of 100 cycles during the life of the system.

Table 4.2-2 Total Gate Oxide Area - Memories

UVEPROMs, Flash EEPROMs, MNOS EEPROMs, Floating Gate PROMs - ARRAY ONLY
MOS PALs/PLAs - ARRAY ONLY*

Capacity (# bits)	Total Gate Oxide Area (um^2) Lower Limit	Upper Limit
2K	8192	16384
4K	16384	32768
8K	32768	65536
16K	65536	131072
32K	131072	262144
64K	147456	327680
128K	294912	655360
256K	589,824	1,310,720
512K	1,179,648	2,621,440
1M	2,359,296	5,242,880
2M	4,718,592	10,485,760

* - For MOS PAL/PLA devices, determine the number of bits in the programmable array, then use next highest bit count category listed in the above table.

UVEPROMs, Flash and MNOS EEPROMs, Float. Gate PROM/PAL/PLA - PERIPHERY ONLY
MOS ROMs/HALs/MLAs - ENTIRE DEVICE

For all devices memory capacities, use range of 260,000 - 1,209,000 um^2.

Table 4.2-2 Total Gate Oxide Area - Memories (Continued)

FLOTOX and Textured-Poly EEPROMs - PERIPHERY EXPOSED TO PROGRAMMING STRESS

For all devices, use 103,000 - 602,500 um^2.

FLOTOX and Textured-Poly EEPROMs - PERIPHERY EXPOSED TO SUPPLY VOLTAGE STRESS

For all devices, use 260,000 - 1,209,000 um^2.

MOS SRAMs - ENTIRE DEVICE
BiMOS SRAMs - ENTIRE DEVICE*

Capacity (# bits)	Total Gate Oxide Area (um^2) Lower Limit	Upper Limit
1K	99,176	497,056
2K	149,352	798,112
4K	45,864	192,888
8K	82,728	358,776
16K	156,456	690,552
32K	303,912	1,354,104
64K	598,824	2,482,600
128K	1,188,648	2,681,208
256K	1,052,576	4,730,592
512K	3,101,152	9,449,184
1M	4,198,304	18,886,368
2M	8,392,608	37,760,736

* - For BiMOS SRAMs, multiply oxide area by .667

MOS DRAMs - ENTIRE DEVICE

Capacity (# bits)	Total Gate Oxide Area (um^2) Lower Limit	Upper Limit
1K	98,588	394,352
2K	123,676	494,704
4K	31,932	95,796
8K	50,364	151,092
16K	87,228	261,684
32K	160,956	482,868
64K	308,412	925,236
128K	603,324	1,809,972
256K	530,288	1,590,864
512K	1,054,576	3,163,728
1M	2,103,152	6,309,456
2M	4,200,304	12,600,912

Table 4.2-3 Gate Oxide Thickness - Memories

UVEPROMs, Float. Gate PROMs - ARRAY ONLY
MOS ROMs/PLAs/PALs/MLAs/HALs - ENTIRE DEVICE*

Capacity (# bits)	Gate Oxide Thickness (Angstroms) Lower Limit	Upper Limit
2K	600	700
4K	600	700
8K	600	700
16K	600	700
32K	600	700
64K	400	600
128K	400	500
256K	400	500
512K	400	500
1M	250	400
2M	250	400

* - For MOS ROMs/PLAs/PALs/MLAs/HALs determine number of bits in array, then use above table, rounding up to the next highest bit category.

Flash EEPROMs - ARRAY ONLY

Capacity (# bits)	Gate Oxide Thickness (Angstroms) Lower Limit	Upper Limit
32K	250	250
64K	250	250
128K	250	250
256K	105	250
512K	105	250
1M	105	250
2M	105	250

MNOS EEPROMs - ARRAY ONLY

Use Range of 15 - 30 Angstroms.

Table 4.2-3 Gate Oxide Thickness - Memories (Continued)

UVEPROMs, MNOS/Flash EEPROMs, Float. Gate PROMs - PERIPHERY ONLY

Capacity (# bits)	Gate Oxide Thickness (Angstroms) Lower Limit	Upper Limit
2K	600	700
4K	600	700
8K	600	700
16K	600	700
32K	600	700
64K	400	600
128K	300	400
256K	300	400
512K	235	400
1M	235	400
2M	235	400

FLOTOX and Tex-Poly EEPROMs - PERIPHERY ONLY

Capacity (# bits)	Gate Oxide Thickness (Angstroms) Lower Limit	Upper Limit
8K	600	750
16K	600	750
32K	600	750
64K	400	600
128K	340	500
256K	340	500
512K	300	500
1M	300	500
2M	300	500

Table 4.2-3 Gate Oxide Thickness - Memories (Continued)

MOS SRAMs, DRAMs - ENTIRE DEVICE
BiMOS SRAMs - ENTIRE DEVICE

Capacity (# bits)	Gate Oxide Thickness (Angstroms) Lower Limit	Upper Limit
1K	1200	1500
2K	1200	1500
4K	410	1000
8K	410	1000
16K	250	410
32K	250	410
64K	250	410
128K	250	410
256K	200	300
512K	200	300
1M	200	300
2M	200	300

Charge Trapping

This was identified as an intrinsic failure mechanism for FLOTOX and Textured-Poly EEPROM devices. The literature information showed that the Tex-Poly device type is more susceptible to failures caused by trapup than FLOTOX devices (by virtue of the fact that the threshold voltage change due to trapup is related to oxide thickness).[44] On the other hand, the very thin tunnel oxide used for FLOTOX devices makes them more sensitive to defect-related oxide breakdown failures. A number of papers have been written on the subject of charge trapping. The point at which a failure actually occurs because of charge trapping is determined by a number of variables such as the trap density of the oxide (influenced by the intrinsic characteristics of the oxide), charge injected into the oxide, E-field within the oxide, threshold voltage of the memory cell, and even the time duration between reprogram cycles. Based on the nature of these variables, a decision was made not to try to model this mechanism using strictly deterministic methods. Instead, this contribution to the overall failure rate of EEPROM devices was modeled using empirical data from device manufacturer sources as well as information provided as part of the literature search.

Charge trapup is an issue only when the EEPROM is repeatedly reprogrammed. Reprogramming also accelerates certain defect-induced failure mechanisms within the tunnel/gate oxides. Indeed, high voltage stress is one method used to screen out such defects, although the voltage used in such a screen must be carefully chosen so as not to damage good oxide. EEPROM manufacturers perform "endurance" testing (read/erase/write cycling) to evaluate the failure rate of a device type due to reprogramming. Failures that occur during this testing are basically due to either oxide failures caused by defects, or failures caused by excessive charge trapping. A typical failure mode during such endurance testing is a single-bit failure in the memory array. Vendor endurance test data was used to derive a reprogram cycling portion of the overall memory device failure rate model.

The EEPROM read/erase/write failure rate, or λ_{cyc}, is the following:

$$\lambda_{cyc} = [A_1B_1 + (A_2B_2/\pi_Q)]\ \pi_{ECC}$$

where:

A_1 and A_2 represent the cycling base failure rate (dependent on total number of cycles and EEPROM type)

B_1 and B_2 represent the multipliers which modify the base failure rate for temperature and device complexity

π_Q is the quality factor

π_{ECC} is the on-chip error correction factor

Endurance test results for two EEPROM device types, each from a different manufacturer (a 16K FLOTOX device and a 64K Tex-Poly device), were used for the analysis. The test results were in the form of percent failures for a given number of cumulative reprogram cycles. For the FLOTOX device, the test results showed a constant failure rate of .0225% failures per 1000 cycles. This indicates that all failures are defect-induced, which is supported by literature data.[44] Although some trapup could be occurring, the data indicates that FLOTOX failures caused by trapup are not significant until very high cycling rates (on the order of 1×10^6 cycles) are achieved. The Textured-Poly endurance test data was more complex. Two separate test results were used. One test evaluated cycling reliability at the lower region of total cycles (up to 10K cycles) by using a cycling method that enhances defect-induced failures. The second test evaluates cycling reliability at the upper region of total cycles (more than 100K cycles) using a method that enhances trapup related failures. The results of the two tests are presented in figures 4.2-1 and 4.2-2.

From these test results, a failure rate expression in failures per million hours was derived using the following relationships:

$$\text{MTBF} = (\#\ \text{Parts} \times \text{F.R. \%} / 1000\ \text{Hrs.})^{-1} \times (1 \times 10^5)$$

$$\text{F.R. \%} / 1000\ \text{Hrs.} = (\text{F.R. \%} / 1000\ \text{cycles}) \times (\#\ \text{Cycles/Hr.})$$

$$\text{F.R. \%} / 1000\ \text{cycles} = \frac{\text{Cumulative \% F.R. at Total \# Cycles}}{(\text{Total \# cycles}) / 1000}$$

Figure 4.2-1

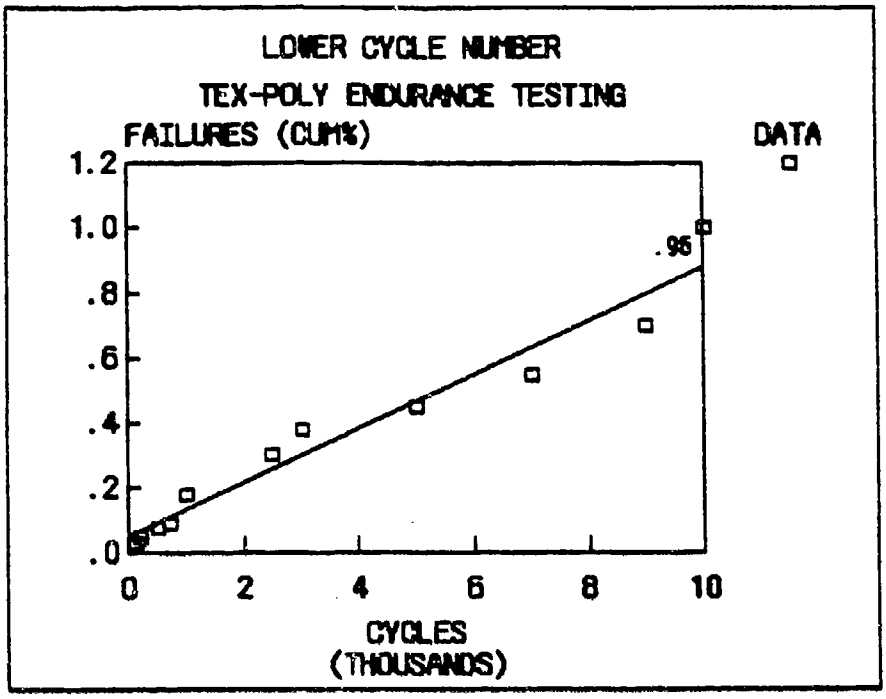
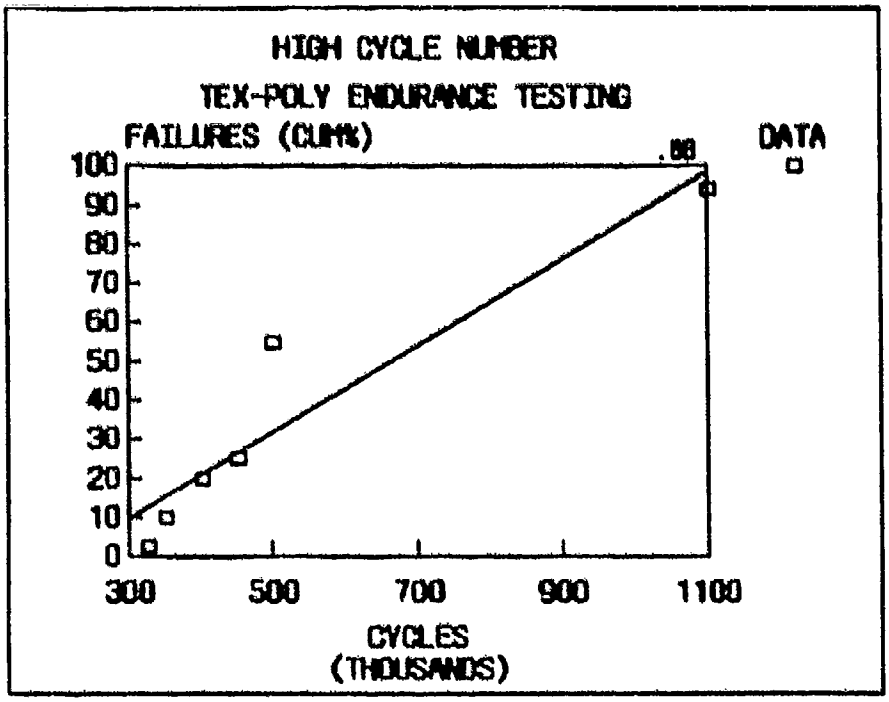


Figure 4.2-2



Then:

$$\text{F.R. \% / 1000 Hrs.} = \frac{(\text{Cumulative \% F.R. at Total \# Cycles}) \times (\text{\# Cycles/Hr})}{(\text{Total \# cycles}) / 1000}$$

$$\text{MTBF} = \left(\frac{(\text{Cumulative \% F.R. at Total \# Cycles}) \times (\text{\# Cycles/Hr.})}{(\text{Total \# cycles}) / 1000}\right)^{-1} \times (1 \times 10^5)$$

The failure rate is taken to be the reciprocal of the calculated MTBF. It can be shown that for a 10,000 hour system lifetime, the failure rate equals the cumulative percent failure rate at the total number of cycles. See Tables 4.2-4 and 4.2-5 for the resulting A_1 and A_2 values. Note that "base" and "B Normalized" values are given for A_1. The test data that yields A_1 values per the above formulas are for commercial grade parts, which correspond to "D" quality. The π_Q factor developed for all models in this project is normalized to a B-level quality. Therefore, the A_1 values must be adjusted to be consistent with "B" quality. Using the π_Q values developed in this project, this adjustment is a 3.3 divisor. These adjusted values (to be used when calculating device failure rates) are the "B" normalized numbers. These values are provided for a baseline system operating lifetime of 10,000 hours. For different assumed lifetimes, the user must multiply A_1 or A_2 by (10,000)/(system lifetime). The A_2 table addresses only the upper region of cycling for Tex-Poly devices. It is divided by the π_Q factor in the final model because it is related to an intrinsic mechanism that is <u>not</u> influenced by screening. This π_Q divisor negates the influence of the π_Q multiplier on the overall defect failure rate of the device. The next paragraph details an example of how the "A" factors were derived.

Determine the A_1 cycling factor for a FLOTOX device experiencing between 100 and 200 reprogram cycles during its lifetime.

1) Two initial assumptions are made here. One is that the worst case number of cycles (200) is used to derive an A_1 factor applicable to the 100-200 cycle category. Also assumed is a 10,000 hour system lifetime.

2) Note the relationship that is used to derive "MTBF" due to cycling:

$$MTBF = \left(\left(\frac{\text{Cumulative \% F.R. at Total \# Cycles}}{\text{(Total \# Cycles) / 1000}}\right) \times (\text{\# Cycles/Hr})\right)^{-1} \times (1 \times 10^5)$$

3) The FLOTOX endurance test data used (figure 4.2-1) gives a constant failure rate of .0225% per 1000 cycles.

At 200 cycles, .0225 x 200/1000 yields .0045 cumulative percent F.R. and # cycles/hr. = 200/10000 hrs. = .02 cycles/hr. Then,

$$MTBF = ((.0045) \times (.02))^{-1} \times (1 \times 10^5) = 2.222 \times 10^8 \text{ hrs.}$$

This equals .0045 failures/million hrs.

The vendor endurance testing was performed on devices screened to D-level quality. To be compatible with the π_Q factors developed for all microcircuit models, the A factors needed to be normalized to B-level quality. To do this, the derived A factors need to be divided by 3.3, which is the B-level to D-level quality factor ratio.

This yields .0045/3.3 = .0014 for the A_1 factor.

This same process was used to derive A values for Tex-Poly devices; however, the Tex-Poly endurance data does not yield a flat cumulative percent failure rate per 1000 cycles. Rather, the data consisted of a curve from which a percent failure rate could be found once the number of cycles is known.

The A factor must now be modified to account for the effects of temperature and complexity. The A-table values are normalized at 60°C T_J for a 16K device for FLOTOX and 30°C T_J for a 64K device for Tex-Poly. The temperature sensitivity was derived using a combination of vendor and literature data. The endurance test data taken from the FLOTOX manufacturer is based on the testing done at 60° T_J. The Tex-Poly endurance test data used is based on testing done at 30° T_J. Therefore, normalization for the A tables was done at both temperatures depending on whether the part is Tex-Poly or FLOTOX. The

available information indicated an E_a of between .12 and .15 eV for FLOTOX.[43,44,67] A .15 value was chosen. The E_a for Tex-Poly endurance failures is dependent on the total number of cycles. For high number of cycles, trapup dominates the Tex-Poly failure rate. The available data[44,68] indicates -.1 eV as being appropriate (negative because of the detrapping effects of elevated temperature) for more than 300K total cycles. For the lower region of endurance (< 300K cycles), .12 eV was selected, because it represents the lower range of the E_a found for EEPROM defect-related endurance failures. An E_a lower than that of FLOTOX was deemed appropriate because any latent defects in the thicker Tex-Poly oxide should be less sensitive to increasing temperature.

No empirical data was available showing the relationship of cycling failure rate to the complexity of the EEPROM device (number of reprogram cycles). All relevant sources of data indicated that FLOTOX was more sensitive to scaling effects than Textured-Poly because the thinner oxide for FLOTOX is more difficult to scale down than Tex-Poly. The same sensitivity to complexity as the MIL-HDBK-217E MOS PROM model was chosen for FLOTOX as this is consistent with the fact that the failures are defect-driven and is supported by literature data.[44] A complexity sensitivity of half the FLOTOX sensitivity was chosen for Tex-Poly EEPROM types. This assumption is also supported by literature data.[44] The temperature/complexity multipliers (B_1, B_2) are shown in tables 4.2-6 through 4.2-8.

Error Correction Factor

A few EEPROM manufacturers have incorporated on-chip error correction circuitry into some or all of their devices. One objective of the memory model effort was to develop a factor in the model which takes this into account. Two error correction schemes were found during the literature search and manufacturer survey activities: a Hamming code approach using 4 correct bits for 8 data bits, and a redundant cell approach which uses an extra storage transistor in every cell. The approach taken was to evaluate the failure rate improvement for a single memory cell and apply this improvement factor to the memory-array failure rate.

Table 4.2-4 A_1 Cycling Factor

Total Number Of Cycles (X)	FLOTOX Base	FLOTOX "B" Normalized	Textured-Poly Base	Textured-Poly "B" Normalized
up to 100	.0023	.0007	.0320	.0097
100 < X ≤ 200	.0045	.0014	.0460	.0139
200 < X ≤ 500	.0113	.0034	.0760	.0230
500 < X ≤ 1K	.0225	.0068	.110	.033
1K < X ≤ 3K	.0675	.0204	.200	.061
3K < X ≤ 5K	.1125	.0341	.300	.091
5K < X ≤ 7K	.1575	.0478	.450	.136
7K < X ≤ 9K	.2025	.0614	.700	.212
9K < X ≤ 10K	.2250	.0682	1.000	.303
10K < X ≤ 15K	.3375	.1023	1.000	.303
15K < X ≤ 20K	.4500	.1364	1.000	.303
20K < X ≤ 30K	.6750	.2045	1.000	.303
30K < X ≤ 50K	1.125	.3409	1.000	.303
50K < X ≤ 100K	2.250	.6818	1.000	.303
100K < X ≤ 200K	4.500	1.364	1.000	.303
200K < X ≤ 300K	6.750	2.045	1.000	.303
300K < X ≤ 325K	7.313	2.216	0*	
325K < X ≤ 350K	7.875	2.386	0*	
350K < X ≤ 400K	9.000	2.727	0*	
400K < X ≤ 450K	10.13	3.070	0*	
400K < X ≤ 500K	11.25	3.409	0*	

If using a system life of other than 10000 hours, multiply A1 by $\frac{10000}{\text{Sys. Life}}$.

* - See A2 Table 4.2-5

Table 4.2-5 A_2 Cycling Factor

For FLOTOX, $A_2 = 0$

For Tex - Poly:

Total # of Cycles	A2
Up to 300K	0.0
$300K < X \leq 325K$	2.50
$325K < X \leq 350K$	10.0
$350K < X \leq 400K$	20.0
$400K < X \leq 450K$	30.0
$450K < X \leq 500K$	40.0

If using a system life of other than 10000 hours, multiply A1 by $\frac{10000}{\text{Sys. Life}}$.

Table 4.2-6

B_i for FLOTOX (.15 eV)

T_J (°C)

Memory Capacity (bits)	20	30	40	50	60	70	80	90	100	110	120	130	140	150	160
	25	35	45	55	65	75	85	95	105	115	125	135	145	155	165
4k	.245	.298	.358	.425	.500	.582	.672	.770	.876	.989	1.111	1.240	1.376	1.521	1.672
	.270	.327	.391	.462	.540	.626	.720	.822	.932	1.049	1.174	1.307	1.448	1.596	1.750
8k	.343	.417	.501	.575	.699	.814	.940	1.077	1.225	1.384	1.553	1.734	1.925	2.126	2.338
	.378	.457	.546	.646	.755	.876	1.007	1.150	1.303	1.467	1.642	1.828	2.024	2.231	2.449
16k	.490	.596	.716	.851	1.000	1.165	1.345	1.540	1.752	1.979	2.221	2.480	2.753	3.041	3.344
	.541	.654	.782	.923	1.080	1.253	1.441	1.644	1.863	2.098	2.349	2.614	2.895	3.191	3.502
32k	.695	.845	1.015	1.206	1.418	1.651	1.907	2.184	2.484	2.806	3.150	3.516	3.903	4.312	4.742
	.767	.928	1.108	1.307	1.532	1.776	2.043	2.332	2.642	2.975	3.330	3.707	4.105	4.525	4.965
64k	.980	1.192	1.432	1.701	2.000	2.329	2.688	3.081	3.504	3.958	4.443	4.959	5.506	6.083	6.689
	1.082	1.308	1.563	1.847	2.161	2.506	2.881	3.288	3.727	4.196	4.697	5.228	5.790	6.382	7.003
128k	1.384	1.683	2.022	2.402	2.824	3.289	3.798	4.350	4.947	5.588	6.273	7.002	7.774	8.589	9.445
	1.528	1.848	2.207	2.608	3.051	3.538	4.068	4.643	5.262	5.925	6.632	7.383	8.176	9.012	9.888
256k	1.960	2.384	2.864	3.402	4.000	4.659	5.379	6.162	7.007	7.915	8.886	9.918	11.011	12.165	13.378
	2.165	2.617	3.126	3.694	4.322	5.011	5.762	6.576	7.453	8.392	9.394	10.457	11.581	12.764	14.006
512k	2.777	3.378	4.059	4.821	5.668	6.602	7.622	8.731	9.929	11.216	12.591	14.054	15.603	17.238	18.956
	3.068	3.708	4.430	5.234	6.124	7.101	8.165	9.319	10.561	11.892	13.311	14.817	16.410	18.087	19.846
1M	3.919	4.768	5.729	6.804	8.000	7.318	10.758	12.323	14.014	15.830	17.771	19.836	22.022	24.330	26.755
	4.330	5.234	6.252	7.387	8.643	10.022	11.525	13.153	14.906	16.785	18.788	20.914	23.162	25.529	28.012

Table 4.2-7

B_i for TEX-POLY (.12 eV)

T_j (°C)

Memory Capacity (bits)	20	30	40	50	60	70	80	90	100	110	120	130	140	150	160
	25	35	45	55	65	75	85	95	105	115	125	135	145	155	165
4k	.454	.531	.615	.706	.803	.907	1.018	1.135	1.257	1.386	1.521	1.660	1.805	1.955	2.110
	.491	.572	.659	.754	.854	.965	1.075	1.195	1.321	1.453	1.590	1.732	1.880	2.032	2.188
8k	.529	.619	.717	.823	.937	1.058	1.187	1.323	1.467	1.617	1.773	1.936	2.105	2.280	2.400
	.573	.667	.769	.879	.996	1.125	1.254	1.394	1.541	1.694	1.854	2.020	2.192	2.370	2.552
16k	.623	.729	.844	.968	1.102	1.245	1.397	1.557	1.726	1.903	2.087	2.279	2.478	2.684	2.896
	.675	.785	.905	1.034	1.173	1.324	1.476	1.640	1.814	1.994	2.182	2.378	2.580	2.789	3.004
32k	.730	.855	.990	1.136	1.293	1.460	1.638	1.827	2.024	2.232	2.448	2.673	2.906	3.147	3.396
	.791	.921	1.061	1.213	1.375	1.553	1.731	1.924	2.127	2.339	2.559	2.789	3.026	3.271	3.523
64k	.855	1.000	1.158	1.329	1.513	1.709	1.917	2.138	2.369	2.612	2.865	3.128	3.401	3.683	3.974
	.926	1.077	1.242	1.420	1.609	1.818	2.026	2.252	2.489	2.737	2.995	3.263	3.541	3.828	4.123
128k	1.031	1.206	1.397	1.603	1.825	2.061	2.312	2.578	2.857	3.150	3.455	3.773	4.102	4.442	4.793
	1.116	1.299	1.498	1.712	1.941	2.192	2.443	2.716	3.002	3.301	3.612	3.936	4.271	4.616	4.972
256k	1.246	1.457	1.688	1.937	2.204	2.490	2.794	3.115	3.452	3.805	4.174	4.556	4.956	5.367	5.791
	1.349	1.570	1.810	2.068	2.345	2.649	2.952	3.281	3.627	3.988	4.364	4.755	5.160	5.577	6.008
512k	1.505	1.761	2.039	2.341	2.664	3.010	3.376	3.764	4.172	4.599	5.045	5.508	5.989	6.486	6.998
	1.630	1.897	2.187	2.500	2.834	3.201	3.568	3.965	4.383	4.819	5.274	5.747	6.236	6.740	7.260
1M	1.815	2.124	2.459	2.822	3.212	3.628	4.071	4.538	5.330	5.544	6.082	6.641	7.221	7.820	8.437
	1.965	2.287	2.637	3.014	3.417	3.859	4.301	4.781	5.284	5.810	6.359	6.928	7.518	8.127	8.753

Table 4.2-8

B_2 for TEX-POLY (-.1 eV)

T_J (°C)

Memory Capacity (bits)	20	30	40	50	60	70	80	90	100	110	120	130	140	150	160
	25	35	45	55	65	75	85	95	105	115	125	135	145	155	165
4k	.608	.531	.468	.415	.372	.335	.303	.276	.253	.233	.215	.200	.186	.174	.163
	.567	.498	.440	.393	.353	.318	.289	.264	.243	.224	.207	.192	.180	.168	.158
8k	.709	.619	.546	.485	.434	.390	.354	322	.295	.272	.251	.233	.217	.202	.190
	.662	.580	.514	.458	.411	.371	.337	.308	.283	.260	.241	.224	.209	.196	.184
16k	.834	.729	.642	.570	.510	.460	.416	.379	.347	.320	.295	.274	.255	.238	.223
	.779	.683	.605	.539	.484	.437	.397	.363	.333	.307	.284	.580	.246	.231	.216
32k	.978	.855	.753	.669	.598	.539	.488	.445	.407	.375	.346	.321	.299	.278	.262
	.913	.801	.709	.632	.568	.513	.466	.425	.390	.360	.333	.310	.289	.280	.254
64k	1.145	1.000	.881	.783	.700	.631	.572	.521	.477	.439	.405	.376	.350	.327	.306
	1.069	.938	.830	.740	.664	.600	.545	.798	.457	.421	.390	.363	.338	.316	.970
128k	1.381	1.206	1.063	.944	.845	.761	.689	.628	.575	.489	.453	.422	.394	.394	.670
	1.289	1.131	1.001	.892	.801	.724	.657	.601	.551	.508	.470	.437	.408	.382	.358
256k	1.668	1.457	1.284	1.141	1.020	.919	.833	.759	.695	.639	.712	.548	.510	.476	.446
	1.557	1.366	1.209	1.078	.968	.874	.794	.726	.666	.614	.568	.528	.493	.461	.433
512k	2.016	1.761	1.552	1.378	1.233	1.111	1.006	.917	.839	.772	.714	.662	.616	.576	.540
	1.882	1.651	1.461	1.303	1.169	1.056	.960	.877	.805	.742	.687	.638	.595	.570	.523
1M	2.430	2.123	1.871	1.662	1.487	1.339	1.213	1.105	1.012	.931	.860	.798	.743	.694	.651
	2.269	1.991	1.761	1.570	1.410	1.274	1.157	1.057	.970	.894	.828	.770	.718	.672	.630

For a redundant cell approach, the conventional M out of N reliability for Time = infinity relation was used:

$$\text{MTBF} = \text{Sum from } J=0 \text{ to } J=K \text{ the term } \frac{1}{(N-J)L}$$

where:

N = Number of active assemblies (N=2)

M = Min. number of assemblies required (M=1)

L = Assembly Failure Rate (L normalized to 1)

J = Number of assembly failures

K = N-M

$$\text{This becomes MTBF} = \frac{1}{(2-0)} + \frac{1}{(2-1)} = 3/2 \text{ MTBF improvement, or 2/3 Fail. Rate reduction}$$

This .6667 factor is multiplied by the cycling failure rate to determine the equivalent failure rate.

For the Hamming code approach, the failure rate improvement factor (π_{ECC}) is derived as follows:

Ordinary 8 bit word failure rate = (λ_w) = 8 X Bit failure rate = 8 X λ_b

"New" word reliability = $R_w = R^{12} + 12R^{11}Q = R^{12} + 12R^{11}(1-R)$

$= R^{12} + 12R^{11} - 12R^{12} = 12R^{11} - 11R^{12} = 12e^{-11\lambda t} - 11e^{-12\lambda t}$

Integrating the above expression from zero to infinity yields an effective "new" word failure rate of:

$$\frac{n(n-1)}{2n-1} = \frac{(12)(11)}{23} = 5.74\,\lambda_b$$

This yields an improvement factor (π_{ECC}) of :

$$\frac{\lambda w'}{\lambda w} = \frac{5.74\lambda b}{8\lambda b}$$

where

$\lambda w'$ = New word failure rate

λw = Old word failure rate

λb = bit failure rate

This factor is applied to the cycling failure rate. It is a conservative approach because it affects only the cycling failure rate portion of the model. If device types other than EEPROMs incorporate on-chip error correction in the future, this factor can also be applied to the defect failure rate (although careful judgment must be made regarding the percentage of defect failures that are correctable).

Defect Failure Rate

Earlier in this section, defects were identified as a very significant contributor to the overall device failure rate for all memory device types. This was evident from the literature search in addition to the life test data collected. The life test data provided much information regarding failure modes and mechanisms that basically were defect-related. The life test data was then used to determine the defect failure rate of the devices.

Table 4.2-9 is a summary of the life test data collected as part of this study. All of the life tests were conducted at 125°C. The column titled "Hrs (M)" indicates the total number of millions of device hours at 125°C for all devices of the designated type and complexity. The column titled "Hrs (M) @ 25°C" indicates the equivalent part hours at 25°C, assuming an activation energy of 0.8 eV for memories. "FPMH @ 25°C" is the calculated failure rate in failures per million hours using the Chi-square distribution at 50% confidence. The column "217E @ 25°C" is the MIL-HDBK-217E base failure rate ($C_1\pi_T$) at 25°C, and the final column is a ratio of the calculated value to the MIL-HDBK-217E value.

The 0.8 eV value was derived by analyzing the published activation energy distributions for different memory failure mechanisms provided by the memory model literature search; these were categorized as metallization, oxide, and

Table 4.2-9
Derived Failure Rates - Memories

TYPE	TECH	NBITS	HRS(M) @125C	FAILURE MECHANISM	EA(eV)	#FAIL	Q-LVL	FPMH @25C	217E @25C	NEW/217E (%)@25C
PROM	CMOS	65.5K	.187	N/A	.8	0	D	.001494	.24	.6
"	ECL	1K	.095	N/A	.8	0	D	.001291	.06	2.2
"	TTL	256	1.051	N/A	.8	0	D	.000266	.06	.4
"	"	1K	1.093	VAR	.8	3	D	.001354	.06	2.3
"	"	2K	1.349	UNK	.8	1	D	.000502	.06	.8
"	"	4K	1.747	VAR	.8	3	D	.000847	.06	1.4
"	"	8K	1.167	VAR	.8	4	D	.001614	.06	2.7
"	"	16K	1.414	UNK	.8	5	D	.001617	.06	2.7
"	"	32K	.477	VAR	.8	3	D	.003104	.12	2.6
PROM	NMOS	32K	3.47	VAR	.8	4	D	.000543	.12	.5
"	"	64K	8.94	N/A	.8	0	D	.000312	.12	.3
"	"	128K	5.636	N/A	.8	7	D	.000549	.24	.2
"	"	256K	4.669	VAR	.8	14	D	.001267	.48	.3
UVPROM	CMOS	65.5K	2.947	UNK	.8	2	D	.000366	.12	.3
"	"	65.5K	1.513	UNK	.8	2	D	.000713	.12	.6
"	"	256K	3.243	UNK	.8	2	D	.000332	.24	.1
UVPROM	CMOS	64K	18.15	VAR	.8	13	D	.003293	.12	2.7
"	"	128K	.49	VAR	.8	1	D	.001381	.24	.6
"	"	256K	5.705	VAR	.8	6	D	.000471	.24	.2
UVPROM	NMOS	32K	12.66	VAR	.8	26	D	.000839	.12	.7
"	"	64K	13.902	VAR	.8	33	D	.000957	.12	.8
"	"	128K	13.068	VAR	.8	40	D	.001245	.24	.5
"	"	256K	3.533	VAR	.8	21	D	.002436	.24	1.0
"	"	512K	20.901	VAR	.8	67	D	.001267	.48	.3
"	"	1M	2.102	UNK	.8	6	D	.001279	.48	.3

Table 4.2-9 (CONTD)

Derived Failure Rates - Memories

TYPE	TECH	#BITS	HRS(M) @125C	FAILURE MECHANISM	EA(eV)	#FAIL	Q-LVL	FPMH @25C	217E @25C	NEW/217E (%)@25C
SRAM	MOS	16K	12.423	VARIOUS	.8	80	D	.002575	.1	2.6
DRAM	MOS	64K	5.109	VARIOUS	.8	10	D	.000842	.05	1.7
SRAM	TTL	576	.75	N/A	.8	0	D	.000373	.05	.7
"	"	64	1.726	VARIOUS	.8	11	D	.002635	.05	5.3
"	"	256	.638	UNKNOWN	.8	2	D	.00169	.05	3.4
"	"	2000	.482	UNKNOWN	.8	2	D	.002238	.05	4.5
EEPROM	MOS	16K	1.456	UNKNOWN	.8	2	D	.000741	.06	1.2
"	"	64K	.658	UNKNOWN	.8	1	D	.001028	.12	.9
EEPROM	NMOS	4K	1.49	VARIOUS	.8	2	D	.000724	.06	1.2
"	"	16K	1.26	UNKNOWN	.8	2	D	.000856	.06	1.4
"	"	16K	7.73	VARIOUS	.8	0	B	.000036	.006	.6
"	"	64K	3.29	UNKNOWN	.8	5	D	.000695	.12	.6
FPLA	TTL/NiCr	297	.05	N/A	.8	0	D	.005589	.12	4.7
"	"	564	.099	VARIOUS	.8	1	D	.006823	.12	5.7
"	"	1832	.096	N/A	.8	0	D	.002852	.24	1.2
"	"	1842	.236	UNKNOWN	.8	1	D	.002869	.24	1.2
"	"	1852	.209	N/A	.8	0	D	.001338	.24	.6
"	"	1928	1.202	UNK	.8	1	D	.000563	.24	.2
"	"	2011	.094	N/A	.8	0	D	.002975	.24	1.2
"	"	2016	.095	N/A	.8	0	D	.002937	.24	1.2
"	"	3360	.05	N/A	.8	0	D	.005589	.24	2.3
"	"	3552	.489	VARIOUS	.8	3	D	.003028	.24	1.3
ROM	NMOS	16K	.211	N/A	.8	0	D	.001325	.035	3.8
"	"	32K	2.009	N/A	.8	0	D	.000139	.07	.2
"	"	64K	2.799	UNKNOWN	.8	4	D	.000673	.07	1.0
"	"	128K	1.896	VARIOUS	.8	4	D	.000993	.14	.7
"	"	256K	1.482	VARIOUS	.8	2	D	.000728	.14	.5

miscellaneous defect-related mechanisms. The average E_as were computed to be .84, .37, and .85, respectively. RAC-MDR-21 was consulted to determine the weighting factors to be associated with each of these mechanisms for bipolar and MOS memories. Table 4.2-10 provides the results. Interestingly, the results for the two technologies were nearly the same, hence the value of 0.8 eV for all memory devices. This relatively high activation energy is driven by the preponderance of oxide step coverage metallization defects in the MDR-21 database. If oxide defects had been predominant, the activation energy would have been much lower.

From the life test analysis, a defect failure rate model (similar to MIL-HDBK-217E) was derived that uses two factors: a temperature acceleration factor (π_T) and a base failure rate/complexity modifier (C_1). The π_T relationship is taken from MIL-HDBK-217E and is as follows:

$$\pi_T = 0.1(e^X) \qquad \text{where:} \quad x = -A \left(\frac{1}{(T_J + 273)} - \frac{1}{298} \right)$$

In most instances, insufficient test data was available to make a detailed evaluation of the impact of device complexity on failure rate. The complexity factors of MIL-HDBK-217E were therefore used as guidance in the C_1 factor development. The following paragraphs describe the defect failure rate model for each memory device category. Refer to Appendix E for the life test data, and Table 4.2-9 for the derived failure rates.

MOS PROMs (Including UVEPROMs, EEPROMs, Floating gate MOS PALs/PLAs)

The data collected did show some correlation between device complexity (capacity in bits) and failure rate. The average failure rate of the 64K, 128K, and 256K UVEPROM test data was used as a baseline failure rate. This value is .00112 FPMH (Failures Per Million Hours) at 25°C for D-level quality. This equals .000339 FPMH after normalizing to B-level quality. The .8 eV activation energy is used to determine the failure rates at temperatures other than 25°C. This activation energy yields an A value of 9270. The FLOTOX and Tex-Poly derived failure rate data is consistent with the UVEPROM

calculations, and the 16K EEPROM resultant failure rate (together with the UVEPROM calculated values) supports the 217E complexity relationship. A complexity relationship equal to that of MIL-HDBK-217E is used, which results in the following C_1 values (these are multiplied by π_E to determine the overall defect failure rate):

	C_1
Up to 16K bits	.00085
16K < X ≤ 64K	.00169
64K < X ≤ 256K	.00339
256K < X < 1M	.00678

(Note: the 25°C normalized failure rates have been multiplied by 10 to get C_1 values - this is to compensate for the 0.1 multiplier in the π_T expression.)

Bipolar PALs/PLAs

The 0.8 eV activation energy (9270 "A" value) is used for π_T. Very little correlation between programmable array bit count and defect failure rate was found for these device types; however, the devices for which life test data was available all contained 200 gates or less. The average failure rate for these devices was determined to be .003456 FPMH at 25°C for D-level quality. This is .001047 after normalizing to B-level quality. A complexity relationship similar to MIL-HDBK-217E is assumed for higher gate count devices, which yields the following complexity factors:

	C_1
Up to 200 gates	.01047
200 < X ≤ 1000 gates	.02094
1000 < X ≤ 2000 gates	.04188

Bipolar PROMs

Most of the life test data available was for low complexity (less than 16K bit) devices. The derived failure rates for $\leq$ 16K devices are roughly equal; the 32K part failure rate was about triple this. The average failure rate for the $\leq$ 16K group was .003104 at 25°C for D-level quality or .000941 when normalizing to B quality. The 32k bit device test data was deemed insufficient to warrant departure from the 217E complexity relationship. Using the 217E relationship yields the following C_1 values:

	C_1
Up to 16K bits	.0094
16K < X $\leq$ 64K	.0188
64K < X $\leq$ 256K	.0376
256K < X < 1M	.0753

MOS ROMs

A weak correlation of complexity to failure rate was found. The 128K and 256K device failure rate data was used to develop an average failure rate of .0008605 FPMH for that device category at 25°C and D-level reliability. This yields .000261 FPMH when normalizing for B-level quality. Using the 217E complexity relationship results in the following:

	C_1
Up to 16K bits	.00065
16K < X $\leq$ 64K	.0013
64K < X $\leq$ 256K	.0026
256K < X < 1M	.0052

Bipolar SRAMs

Test data for low complexity SRAMs of this type were available (under

16K bits). The average failure rate was calculated to be .001734 FPMH at 25°C for D-level quality, or .000525 for B-level quality. The C_1 values are:

	C_1
Up to 16K bits	.0052
16K < X ≤ 64K	.0105
64K < X ≤ 256K	.0210
256K < X < 1M	.0420

MOS SRAMs

Life test data for 16K MOS SRAMs was used and is .002575 FPMH for that complexity at 25°C and D-level quality. Normalizing for B-level quality gives .000780 FPMH. The same C_1 values as are used for bipolar SRAMs are then applied.

	C_1
Up to 16K bits	.0078
16K < X ≤ 64K	.0156
64K < X ≤ 256K	.0312
256K < X < 1M	.0624

DRAMs

Data for 64K DRAMs was available. The average failure rate is .000842 FPMH for this device at 25°C and D-level quality. This equals .000255 for B-level quality. The 217E complexity relationship yields:

	C_1
Up to 16K bits	.0013
16K < X ≤ 64K	.0025
64K < X ≤ 256K	.0051
256K < X < 1M	.0100

Table 4.2-10

FAILURE MECHANISM	REPORTED FAILURE MECHANISM ACTIVATION ENERGIES FROM SIX VENDORS							FAILURE MECHANISM QUANTITY	
	VEN-DOR 1	VEN-DOR 2	VEN-DOR 3	VEN-DOR 4	VEN-DOR 5	VEN-DOR 6	MECHANISM $E^{(4)}$ AVERAGE	FAILURE EVENTS BIP	FAILURE EVENTS MOS
Metallization(1)	.9	.7	.75	1.0	.7	1.0	.84	34	202
Oxide(2)	.52	.3	.35	.45	.3	.3	.37	3	37
Miscellaneous(3)	.9	1.06	.95	.62	.62	1.0	.85	3	18
							Event Total	40	257
							Average Activation Energy *(E_A avg.) (5)	0.806	0.773

Notes: (1) Metallization includes metallization/mask defects, open tracks, electromigration.

(2) Oxide includes all dielectric defects.

(3) Miscellaneous includes bulk defects, package-related defects, latch-up defects and various lesser-occurring events.

(4) The mechanism E_A average is the arithmetic mean of the six reported values for each mechanism. Since the six vendors did not report numbers of failure events, these values could not be weighted by vendor.

(5) $E_A = \frac{\text{(Mechanism Ea Average)} \times \text{(Mechanism \# Failure Events)}}{\text{Event Total}}$

MOS Memory: $\frac{(202 \times .84) + (37 \times .37) + (18 \times .85)}{257} = 0.773$ eV

Bipolar Memory: $\frac{(34 \times .84) + (3 \times .37) + (3 \times .85)}{40} = .806$ eV

4.2.2.3 Memory Model Form

Based on the information and data just presented, the memory device model form that has been developed for this project is as follows:

$$\lambda_P = \lambda_{EM} + \lambda_{TDDB} + [(C_1)(\pi_T) + \lambda_{cyc} + (C_2)(\pi_E)]\ (\pi_Q)(\pi_L)$$

where:

λ_P is the device predicted failure rate in failures per million hours.

λ_{EM} is the "go - no go" failure rate due to electromigration. Also refer to section 4.1.3.2.

λ_{TDDB} is the failure rate due to Time dependent dielectric breakdown. Also refer to section 4.1.3.1.

C_1 is the base failure rate for defect-related failures.

π_T is the temperature multiplier for the defect-related failure rate.

λ_{cyc} is the EEPROM* read/write cycling induced failure rate and is:

$$\lambda_{cyc} = [A_1B_1 + A_2B_2/\pi_Q]\ \pi_{ECC}$$

where:

A_1 and A_2 are the base cycling failure rates.

B_1 and B_2 are the temperature/complexity multipliers.

π_{ECC} is the on-chip error correction factor:
- = .7174 for Hamming Code with 8 data bits and 4 correct bits.
- = .6667 for a two-needs-one redundant cell approach.
- = 1.0 for any device not using on-chip error correction.

* - λ_{cyc} = 0 for all devices other than Flotox or Textured Poly EEPROMs.

C_2 is the package base failure rate.

π_E is the environmental factor. Refer to sect. 4.6.4.

π_Q is the quality factor. Refer to sect. 4.6.1.

π_L is the learning factor. Refer to sect. 4.6.2.

4.3 MONOLITHIC GaAs DEVICES

4.3.1 GaAs Database - Summary of Sources and Data

The GaAs model database relied on information from an industry survey, telephone contacts with additional companies, and published literature. The published literature includes papers, articles, books, company data books, and company application notes. The GaAs industry survey by mail was largely unsuccessful since only one useful set of data was obtained from the thirteen companies that responded (see Table 4.3-1). General Electric supplied accelerated life test data on a power MMIC amplifier through the survey format. Litton and Harris formally withdrew from the survey after receiving specific instructions for the type of data that would be required. Seven additional companies (see Table 4.3-1) were contacted independently of the industry survey and NEC Corp. supplied useful accelerated life test data from an application note. Other data in the form of accelerated life test reports on discrete GaAs field effect transistors and diodes was obtained from Alpha, Sanders, Avantek, Fujitsu, Harris, NEC Corp., and Texas Instruments although the data was not useful for this study. There appears to be a tendency among the GaAs integrated circuit manufacturers to carefully guard specific process details and reliability test results especially in this area where emerging technology is being built. This tendency is understandable since much of the technology is considered proprietary and many of the company contacts from the industry survey expressed this view. The most useful data was obtained from published papers and data books which discussed the results of accelerated life tests on GaAs integrated circuits and other circuit elements.

Approximately ninety six papers, articles, and books were reviewed during the literature search for failure mechanism information and this source also provided most of the data for the development of models. The results of accelerated life test studies from the six most useful papers or articles and three company data books are summarized in Tables 4.3-2, 4.3-3 and 4.3-4. The integrated circuit element summary data (see Table 4.3-4) was developed from a paper by Roesch and Stunkard[92]. The other papers are referenced in Tables 4.3-2 and 4.3-3.

Table 4.3-1

GaAs Data Collection and Industry Contacts

COMPANIES RESPONDING TO SURVEY	BUILDS MMIC GaAs	BUILDS DIGITAL GaAs	WITH-DREW FROM SURVEY	DOES NOT BUILD GaAs	SENT DATA	DATA USEFUL
Litton Electron Devices Microwave Solid State			X			
Harris Microwave Semiconductor	X	X	X			
Mostek				X		
Pacific Monolithics	X					
Tachonics Corp.	X					
TriQuint Semiconductor	X	X				
Watkins Johnson Co.	X					
Vitesse Semiconductor		X				
Gain Electronics		X				
Anadigics	X	X				
M/A-COM AAD	X					
Microwave Semiconductor Corp.	X					
Alpha	X	X			X	
G.E.	X				X	X
Avantek	X					
Sanders Microelectronic Center	X				X	
ADDITIONAL TELEPHONE CONTACTS						
NEC Corp.	X	X			X	X
David Sarnoff Research Center				X		
Raytheon Special Microwave Devices Operation	X					
Adams Russell Electronics	X	X				
Eaton-AIL-Division	X					

Table 4.3-2

GaAs MMIC Data Summary

MANUFACTURER	TEST TYPE	DEVICE TYPE	TEST TEMP (°C)	SAMPLE SIZE	ACTIVATION ENERGY (ev)	FAILURE RATE REFERENCED TO 150°C	REFERENCE NO.
TriQuint Semiconductor	Accelerated Life Test	TW9111U Amplifier	225	131	1.6	4.26×10^{-7}	83 & 84
Harris Microwave Semiconductor	Accelerated Life Test	HMM-11810 Amplifier	200	31	1.6	4.36×10^{-7}	83 & 85
General Electric Co.	Accelerated Life Test	MMIC Power Amplifier	200	17	1.5	1.29×10^{-6}	89
NEC Corporation	Accelerated Life Test	Amplifiers & Interface ICs	220	30	1.17	7.85×10^{-7}	90
M/A-COM Inc.	Accelerated Life Test	MA4GM201 MA4GM211 SPST Switches	250	20	1.35	2.06×10^{-7}	91
WEIGHTED AVERAGES					1.5	4.51×10^{-7}	

Table 4.3-3

GaAs Digital Data Summary

MANUFACTURER	TEST TYPE	DEVICE TYPE	TEST TEMP (°C)	SAMPLE SIZE	ACTIVATION ENERGY (ev)	FAILURE RATE REFERENCED TO 150°C	REFERENCE NO.
NEC Corporation	Accelerated Life Test	ECL Compatible OR-NOR Gates, T&D Flip-Flops	220	30	1.4	3.33×10^{-8}	86
TriQuint Semiconductor	Accelerated Life Test	MSI Circuits	225	130	1.6	3.51×10^{-7}	83
Giga Bit Logic Inc.	Accelerated Life Test	SSI, MSI, LSI Circuits	150	658	1.4	4.58×10^{-6}	PP
WEIGHTED AVERAGE					1.4	2.53×10^{-6}	

Table 4.3-4

GaAs Integrated Circuit Element Data Summary

INTEGRATED CIRCUIT ELEMENT	TEST TYPE	TEST TEMP (°C)	SAMPLE SIZE	ACTIVATION ENERGY (ev)	FAILURE RATE REFERENCED TO 150°C
Implanted Resistors & Ohmic Contacts	Accelerated Life Test	203	~90	--	1.57×10^{-7}
Thin Film Resistors	Accelerated Life Test	125 150 175 200	70	1.0	3.05×10^{-7}
First Level Metallization	Accelerated Life Test	250 275 300	80	1.8	0.059×10^{-7}
Air Bridge Metallization	Accelerated Life Test	170	~70	0.43	0.68×10^{-7}

4.3.2 GaAs Failure Rate Models

No GaAs integrated circuit models currently exist in MIL-HDBK-217E. The only reference to GaAs in MIL-HDBK-217E is in the discrete semiconductor FET section where an application factor and a quality factor are applied to GaAs FETs. The 217E model is basically a silicon model. Significant material and processing differences[88,93,94] exist between silicon and GaAs (see Table 4.3-5) and these differences result in different failure mechanisms for the two materials and require different failure rate models.

The literature search revealed that the primary failure mechanism affecting GaAs integrated circuits centers around metallization and GaAs interdiffusion[83,93,95]. In particular Au-GaAs interdiffusion involves a slow degradation in the GaAs contact regions and in the Schottky gate regions of the MESFET components. The MESFET channel regions become reduced and hot spots can develop. Ohmic contact resistance will increase in the drain and source contacts on the MESFETs and in the other contacts in the integrated circuit. Failures will initially involve parametric changes in performance but will eventually involve catastrophic damage. Other failure mechanisms including electromigration, corrosion, backgating, and capacitor dielectric defects have been reported to occur rarely in comparison to the Au-GaAs interdiffusion failure mechanism[83].

The circuits selected for failure rate modeling were the GaAs MMIC (Monolithic Microwave Integrated Circuit) and the GaAs digital circuits. Significant processing differences exist between the two circuit types and the differences resulted in two different models. GaAs MMICs use depletion mode MESFETs with fewer transistors dissipating more power than on digital circuits which use larger numbers of smaller size depletion or enhancement mode MESFETs that dissipate less power[83]. MMICs use many capacitors (metal insulator metal, interdigited, stub, Schottky barrier), inductors (lumped or distributed), resistors (implanted or thin film), and Au based air bridge interconnects[93]. Digital GaAs circuits make limited use of implanted resistors and Schottky diodes. No air bridge interconnects are used on

digital GaAs circuits. Higher frequency GaAs MMIC devices require more control of interconnect and substrate dimensions to maintain good quality transmission line interconnections. MMIC devices use more extensive backside processing steps because of the low inductance ground connections that are required[93]. This step can also serve to increase the thermal conductivity through the MMIC substrate and this is not applicable on digital GaAs circuits.

Accelerated life test studies in industry indicate that the MESFETs (active devices) used in MMIC and digital GaAs devices fail at higher rates than the other components on the integrated circuits. This requires that the failure rate models must be dominated by the MESFET failure mechanism (Au-GaAs interdiffusion). Since the failure mechanism of the MESFET is based on a diffusion process, temperature was determined to be the driving factor in the active device failure rate model (λ_A in figures 4.3-1 and 4.3-2) which was then based on the modified Arrhenius equation[96] as follows:

$$\lambda_2 = \lambda_1 e^{\frac{E_A}{K}\left(\frac{1}{T1} - \frac{1}{T2}\right)} \qquad (4.3.1)$$

where:

Ea = Activation energy (ev)

T1 & T2 = Temperatures (Kelvin)

λ_1 & λ_2 = failure rates at T1 & T2

K = Boltzmann's constant

The complete GaAs MMIC and digital failure rate models are presented in figures 4.3-1 and 4.3-2 with all of the symbols and equations defined except for $C_2\pi_E$, π_L, and π_Q which are found in other sections of this report. The active device base failure rate (λ_A) for both MMICs and digital GaAs devices were developed from equation 4.3.1 by calculating weighted averages (based on sample size) of the MMIC and digital GaAs accelerated life test failure rates and activation energies that were listed in Tables 4.3-2 and 4.3-3. The reference temperature is 150°C (423°K) and the only remaining unknown is the channel temperature T_{CH} (see figures 4.3-1 and

4.3-2). The application factor for MMICs (π_A) was developed by comparing the ratio of the 150°C failure rates (see Table 4.3-2) for a known low noise MMIC (π_A = 1) made by Harris Semiconductor and a power amplifier MMIC made by General Electric (π_A = 3.0 for power devices). The General Electric MMIC was also used to establish the maximum power range (3000 mw) for the application factor. The MMIC active device complexity factor (π_{CA}) was derived from a set of MMIC failure rate data from NEC Corporation[90] (see Table 4.3-6). A ratio of failure rate data was found by dividing the data with greater than one hundred transistors at three given quality levels by data with less than one hundred transistors. This ratio was then averaged and used as the MMIC active device complexity factor (π_{CA}). The digital GaAs active device complexity factor (π_{CA}) was derived from failure rate data in a paper by Venkataraman, Kotz, and Welch[87] (see Table 4.3-7). Small scale and medium scale integration failure rates were averaged together as a group and compared to large scale integration failure rates to develop the digital complexity factor (π_{CA} = 2.0). The passive device failure rates (λ_p in figures 4.3-1 and 4.3-2) for MMICs and digital GaAs devices were derived from a paper by Roesch and Stunkard[92] (see Table 4.3-8) where accelerated life tests were performed on GaAs integrated circuit elements. Composite digital passive failure rates were developed by summing the failure rates for the implanted resistors, ohmic contacts, and first level metallization used in digital GaAs circuits. The failure rates of thin film resistors and air bridge metallization (used in MMICs) was added to the digital composite failure rate to establish a passive MMIC failure rate since all of the passive circuit elements are used on MMIC devices. The failure rate data for integrated circuit elements in Table 4.3-8 (75% current level) were derated from the maximum current levels (100%) given in the referenced paper to represent a more typical operating level for the circuit elements. A composite activation energy (.43 eV) was used for both MMIC and digital GaAs passive failure rate models. The complexity factor (π_{CP}) appearing in the MMIC failure rate model was derived from an engineering estimate based on the much wider use of passive components in MMIC devices when compared to digital GaAs devices. The digital passive device GaAs model does not have a complexity factor because of the more limited use of passive devices on

digital circuits and because this information is more difficult to determine on digital circuits. When information for the model factors is unknown, the default values revert to the maximum numbers listed for each factor. The temperature term (T) required for the passive failure rate models (see figures 4.3-1 and 4.3-2) is meant to apply to the maximum passive device temperature on each circuit. If this temperature is unknown, the default value becomes the active device channel temperature (T_{CH}) which must be known. Also, the weighted averages of the failure rates listed in Tables 4.3-2 and 4.3-3 which determine λ_A for both models and the failure rates developed from Table 4.3-4 for λ_p were based on B-level quality devices to correspond to a quality factor π_Q of "one". Table 4.3-9 contains calculated values for active and passive base failure rates from 25°C to 175°C for both MMIC and digital GaAs devices. The failure rates are carried to four places (failures/10^6 hours) which results in zero values for the active device failure rates at the lower temperatures. The maximum channel temperature listed in Table 4.3-9 is 175°C which was the highest maximum operating temperature reported by any of the manufacturers.

The original proposed form for MMIC devices is shown in equation 4.3.2.

$$\lambda p(MMIC) = \sum_{i=1}^{n} (\lambda_{mi}\pi_{Ai}\pi_{CLi}) + (\lambda_R\pi_{CR} + \lambda_L\pi_{CL} + \lambda_C\pi_{CC})\pi_Q \qquad (4.3.2)$$

The base failure rate (λ_{mi}) was designed to account for different size active device operating at different channel temperatures on the same chip. This would require a careful thermal survey of the device and this information was not available for this study. Individual integrated circuit element failure rate terms for resistors (λ_R), inductors (λ_L), and capacitors (λ_C) were also proposed but the minimal amount of data on circuit elements made this concept difficult to implement and the resulting composite or lumped passive failure rates were developed in this study.

The final model equations and symbols were modified in order to make them compatible with MIL-HDBK-217E.

A temperature factor (π_T) was defined by including only the exponential terms from λ_A and λ_P.

The modified equations are shown in equations 4.3-3 and 4.3-4 below.

$$\lambda_M = [(C_{1A}\ \pi_{TA} + C_{1P}\ \pi_{TP})\ \pi_A + C_2\ \pi_E]\ \pi_L\ \pi_Q \qquad (4.3.3)$$

$$\lambda_D = [C_{1A}\ \pi_{TA} + C_{1P}\ \pi_{TP} + C_2\ \pi_E]\ \pi_L\ \pi_Q \qquad (4.3.4)$$

where:

- λ_M = MMIC GaAs Part Failure Rate
- λ_D = Digital GaAs Part Failure Rate
- C_{1A} = GaAs Active Device Complexity Factor (For transistors and diodes)
- C_{1P} = GaAs Passive Device Complexity Factor (For resistors, capacitors, inductors)
- π_{TA} = GaAs Active Device Temperature Factor
- π_{TP} = GaAs Passive Device Temperature Factor
- π_A = MMIC Application Factor
- $C_2\pi_E$ = Package Failure Rate
- π_L = Experience or Learning Factor
- π_Q = Quality Factor

FIGURE 4.3-1

GaAs MMIC FAILURE RATE MODEL

$$\lambda_M = [(\lambda_A \pi_{CA} + \lambda_P \pi_{CP}) \pi_A + C_2\pi_E] \pi_L \pi_Q \quad \frac{\text{failures}}{10^6 \text{ hours}}$$

λ_M = MMIC PART FAILURE RATE

λ_A = MMIC ACTIVE DEVICE BASE FAILURE RATE

π_{CA} = MMIC ACTIVE DEVICE COMPLEXITY FACTOR

λ_P = MMIC PASSIVE DEVICE BASE FAILURE RATE

π_{CP} = MMIC PASSIVE DEVICE COMPLEXITY FACTOR

π_A = MMIC APPLICATION FACTOR

$C_2\pi_E$ = PACKAGE FAILURE RATE

π_L = EXPERIENCE OR LEARNING FACTOR

π_Q = QUALITY FACTOR

$$\lambda_A = 0.4506\, e^{-17380 \left(\frac{1}{T_{CH} + 273} - \frac{1}{423}\right)} \frac{\text{failures}}{10^6 \text{ hours}} \; ; \; E_A = 1.5 \text{ ev}$$

π_A = 1.0 FOR LOW NOISE AND LOW POWER LESS THAN OR EQUAL TO 100 mw
3.0 FOR DRIVER AND HIGH POWER GREATER THAN 100 mw TO 3000 mw

π_{CA} = 1.0 FOR LESS THAN 100 ACTIVE DEVICES
1.6 FOR 100 TO 1000 ACTIVE DEVICES

π_{CP} = 1.0 FOR LESS THAN OR EQUAL TO 10 PASSIVE DEVICES
1.2 FOR 11 TO 100 PASSIVE DEVICES
1.3 FOR 101 TO 1000 PASSIVE DEVICES

$$\lambda_P = 0.2263\, e^{-4980 \left(\frac{1}{T + 273} - \frac{1}{423}\right)} \frac{\text{failures}}{10^6 \text{ hours}} \; ; \; E_A = 0.43 \text{ ev}$$

FIGURE 4.3-2

GaAs DIGITAL FAILURE RATE MODEL

$$\lambda_D = [(\lambda_A \pi_{CA} + \lambda_P) + C_2\pi_E]\, \pi_L\, \pi_Q \quad \frac{\text{failures}}{10^6 \text{ hours}}$$

λ_D = DIGITAL GaAs PART FAILURE RATE

λ_A = DIGITAL GaAs ACTIVE DEVICE BASE FAILURE RATE

π_{CA} = DIGITAL GaAs ACTIVE DEVICE COMPLEXITY FACTOR

λ_P = DIGITAL GaAs PASSIVE DEVICE BASE FAILURE RATE

$C_2\pi_E$ = PACKAGE FAILURE RATE

π_L = EXPERIENCE OR LEARNING FACTOR

π_Q = QUALITY FACTOR

$$\lambda_A = 2.5303\, e^{-16220\left(\frac{1}{T_{CH} + 273} - \frac{1}{423}\right)} \frac{\text{failures}}{10^6 \text{ hours}} \; ; \; E_A = 1.4 \text{ ev}$$

π_{CA} = 1.0 FOR LESS THAN 1000 ACTIVE DEVICES (1)
2.0 FOR 1000 TO 10,000 ACTIVE DEVICES (2)

$$\lambda_P = 0.0687\, e^{-4980\left(\frac{1}{T + 273} - \frac{1}{423}\right)} \frac{\text{failures}}{10^6 \text{ hours}} \; ; \; E_A = 0.43 \text{ ev}$$

(1) THIS FACTOR INCLUDES SMALL SCALE AND MEDIUM SCALE INTEGRATION PARTS.

(2) THIS FACTOR INCLUDES LARGE SCALE INTEGRATION PARTS.

Table 4.3-5

GaAs Material and Process Comparison With Si

MATERIAL PROPERTIES (300 K)	GaAs	Si	COMMENTS
Electron Mobility ($cm^2/v.s$)	8500	1500	GaAs has higher mobility (5.7 times) which translates to at least twice the speed of Si
Carrier Drift Velocity (cm/s)	2.2×10^7	6.5×10^6	GaAs has a faster switching speed.
Electric Field at Peak Electron Velocity (v/cm)	7×10^3	3×10^4	GaAs has potential for lower power dissipation.
Intrinsic Resistivity (ohm-cm)	2.3×10^5	1×10^8	A semi-insulating substrate for GaAs means no problems with oxide or junction isolation.
Energy Bandgap (ev)	1.42	1.12	GaAs has special optical properties and a better radiation tolerance.
Intrinsic Temp (°C at 10^{13} cm^{-3} background concentration)	300	130	At more than twice the intrinsic temperature of Si, GaAs has potential to operate at higher temperatures.
Linear Coefficient of Thermal Expansion ($°C^{-1}$)	6.86×10^{-6}	2.6×10^{-6}	Thermal mismatches between materials will be a more difficult problem on GaAs.
Thermal Conductivity (W/cm°C)	0.46	1.5	The higher thermal resistance (more than 3 times greater) of GaAs means that heat sinks are usually required and other thermal management issues are a serious concern.
Melting Point (°C)	1238	1415	--

Table 4.3-5 (cont)

GaAs Material and Process Comparison With Si

PROCESSING STEPS	GaAs	Si	COMMENTS
Transistor Structures	Schottky Barrier	Bipolar & MOS	GaAs MESFETs are free from the surface effects, ionic contamination, charge trapping, and time dependent dielectric breakdown problems seen in Si.
Metallization	Au, Ti, Pt Based	Al and Polysilicon Based	GaAs is less susceptible to the electromigration and corrosion mechanisms on Si products.
Native Oxide	None Stable	SiO_2	Construction of MOS devices and use of traditional processing techniques is not possible on GaAs.
Backside Processing	Required	Minimal	Thinner wafers and backside processing creates more handling problems (breakage and damage) on GaAs.

Table 4.3-6

NEC GaAs MMIC Failure Rates at 125°C[90]

QUALITY LEVEL	$n \leq 100$	$100 < n \leq 1000$	RATIO $\frac{100 < n \leq 1000}{n \leq 100}$
JAN-S Equivalent	50	100	2.0
JANTXV Equivalent	200	300	1.5
JANTX Equivalent	300	400	1.33
AVERAGE RATIO FOR MMIC COMPLEXITY			1.61

Table 4.3-7

Venkataraman's Digital GaAs Failure Rates at 100°C[87]

PART TYPES		FAILURE RATES (Failures/10^9 Hours)	AVERAGE FAILURE RATE (Failures/10^9 Hours)
SSI	NOR Gate	77	75
	Exclusive OR Gate	82	
	Buffer	91	
	Comparator	90	
	Flip-Flop	50	
MSI	COUNTERS	80	
	MULTIPLEXER/ DEMULTIPLEXER	55	
LSI	1 K STATIC RAM	153	153
RATIO OF LSI/MSI & SSI FAILURE RATES FOR DIGITAL GaAs COMPLEXITY			2.04

Table 4.3-8

GaAs Passive IC Element Failure Rates[92]

PASSIVE INTEGRATED CIRCUIT ELEMENT	FAILURE RATE AT 150°C DERATED TO 75% CURRENT LEVEL	COMPONENT USE ON MMIC	COMPONENT USE ON DIGITAL
Implanted Resistors and Ohmic Contacts	6.62×10^{-8}	X	X
Thin Film Resistors	1.29×10^{-7}	X	
First Level Metallization	2.48×10^{-9}	X	X
Air Bridge Metallization	2.86×10^{-8}	X	
Composite Passive Failure Rates	--	2.26×10^{-7}	6.87×10^{-8}

Table 4.3-9

GaAs MMIC & Digital Base Failure Rate Table

(Failures/Million Hours)

	GaAs MMIC		GaAs DIGITAL IC	
$T_{CHANNEL}$ (°C)	λ_A	λ_p	λ_A	λ_p
25	0.0000*	0.0016	0.0000*	0.0005
35	0.0000*	0.0028	0.0000*	0.0008
45	0.0000*	0.0046	0.0000*	0.0014
55	0.0000*	0.0075	0.0000*	0.0023
65	0.0000*	0.0117	0.0002	0.0036
75	0.0000*	0.0179	0.0007	0.0054
85	0.0003	0.0267	0.0024	0.0081
95	0.0010	0.0389	0.0082	0.0118
105	0.0034	0.0557	0.0263	0.0169
115	0.0111	0.0782	0.0796	0.0237
125	0.0341	0.1080	0.2275	0.0328
135	0.0995	0.1468	0.6178	0.0445
145	0.2757	0.1966	1.5993	0.0596
155	0.7283	0.2597	3.9605	0.0788
165	1.8406	0.3387	9.4095	0.1028
175	4.4633	0.4367	21.5088	0.1325

* Value carried to four places only

GaAs MMIC

$$\lambda_A = 0.4506\, e^{-17380\left(\frac{1}{T_{CH}+273}-\frac{1}{423}\right)}$$

$$\lambda_p = 0.2263\, e^{-4980\left(\frac{1}{T+273}-\frac{1}{423}\right)}$$

GaAs Digital IC

$$\lambda_A = 2.5303\, e^{-16220\left(\frac{1}{T_{CH}+273}-\frac{1}{423}\right)}$$

$$\lambda_p = 0.0687\, e^{-4980\left(\frac{1}{T+273}-\frac{1}{423}\right)}$$

4.4 HYBRIDS

4.4.1 Database

The data collected came from two sources: field data on the APG-68 radar system, and data from life testing conducted both in-house and in the industry. Table 4.4-1 lists the hybrid part types used on the APG-68 radar and the cumulative removal rate based on 263,990 hours of system operation over the period studied.

Table 4.4-2 lists the data collected from the life tests. Part of this data was collected as the result of the survey conducted. Both 1000 hour life (extended burn-in) and extended temperature cycling tests are included.

Table 4.4-1 APG-68 Hybrid Cumulative Removal Rate
(Nov 1984 - June 1988)

PART NUMBER	NAME	CLASS	QTY USED /SYS	QTY REMOVED	CUMULATIVE FIELD REMOVAL RATE (/MILLION HRS)
583R379A01	Digibus	Digital	3	49	61.87
585R927A02	Dumped Intg.	Digital	2	14	26.52
585R928A02	RAM	Digital	2	9	17.05
586R291A01	µP/RAM	Digital	1	1	3.79
586R517A01	Mux	Digital	1	8	30.30
12604356	10 Bit D/A	Linear	2	5	9.47
583R352H01	A/D	Linear	1	15	56.82
583R505H01	D/A	Linear	1	117	443.18
583R979H01	D/A	Linear	2	4	7.58
585R056H01	S/D Conv	Linear	1	20	75.76
585R150A03	SW Driver	Linear	1	32	121.21
585R209A01	BORAM I/O	Linear	20	61	11.55
585R587A01	Timing	Linear	1	95	359.85
585R588H01	A/D	Linear	1	116	439.39
585R972H01	D/A	Linear	2	12	22.73
585R974H02	S/D	Linear	2	7	13.26
586R290A01	RAM I/O	Linear	1	60	227.27
586R292A01	Monitor	Linear	1	10	37.88
635A870H01	A/D	Linear	1	0	
583R407H01	Buffer	Linear	2	31	58.71

Table 4.4-1 APG-68 Hybrid Cumulative Removal Rate (contd.)

(Nov 1984 - June 1988)

PART NUMBER	NAME	CLASS	QTY USED /SYS	QTY REMOVED	CUMULATIVE FIELD REMOVAL RATE (/MILLION HRS)
583R412H01	Amp	Linear	2	9	17.05
583R495H02	Volt. Ref.	Linear	1	0	
584R032H03	Driver	Linear	1	0	
584R353H03	Amp	Linear	1	2	7.58
584R353H04	Amp	Linear	1	12	45.45
584R548H03	Sample/Hold	Linear	2	41	77.65
585R149A02	Control	Linear	1	19	71.97
583R504H04	Reg-5V,3.5A	PHP	2	19	35.98
583R504H23	Reg-5V,2V,19A	PHP	1	13	49.24
583R504H24	Reg-15V,9.5A	PHP	1	14	53.03
583R511H12	Reg--5.3V,29A	PHP	1	32	121.21
583R511H13	Reg--15V,4.4A	PHP	1	5	18.94
583R512H01	Reg-+15V,-15V,2A	PHP	3	26	32.83
583R512H10	Reg-28V,3A	PHP	1	15	56.82
583R520H03	Reg-15V,0.5A	PHP	5	23	17.42
584R550A04	INV, PreReg	PHP	2	138	261.36
584R551A04	INV, Bridge	PHP	2	124	234.85
585R151A03	Reg-20V, 1.5A	PHP	1	9	34.09
586R508A01	Reg-	PHP	1	8	30.30
586R509A02	Reg-2.75V	PHP	1	6	22.73
586R509A03	Reg-5.45V,21A	PHP	1	13	49.24
12604360-6	Switch	µwave	1	7	26.52
583R405H01	Switch	µwave	2	19	35.98
583R405H02	Switch	µwave	1	2	7.58
584R422H01	Switch	µwave	1	4	15.15
585R736H04	Amp	µwave	2	11	20.83
585R736H05	Amp	µwave	1	8	30.30
585R736H09	Amp	µwave	1	4	15.15
12604361-1	Switch	Video	1	0	
12604427	Amp	Video	2	16	30.30
583R154H16	Amp	Video	5	16	12.12
583R154H30	Amp	Video	1	2	7.58
583R154H31	Amp	Video	3	5	6.31
583R154H53	Amp	Video	2	7	13.26
583R154H56	Amp	Video	4	9	8.52
583R154H61	Amp	Video	5	6	4.55
583R161H21	Amp	Video	1	11	41.67
584R213H01	Switch	Video	2	2	3.79

Table 4.4-2
Life Test Data

TYPE	P/N	QTY	FAILURES	FAILURE MECHANISM	TEST CONDITIONS	CASE	COMMENTS
Digital	586R291	22	0		1000 Hr. Life, T = 125°C	1	Teledyne
Linear	586R292	5	0		1000 Hr. Life, T = 125°C	1	Teledyne
Video Amp	12604427	38	1 @ 504	Unknown	1000 Hr. Life, T = 125°C	1	Teledyne
Linear	586R587	22	0		1000 Hr. Life, T = 125°C	1	Teledyne
Linear	586R290	22	0		1000 Hr. Life, T = 125°C	1	Teledyne
Digital	585R927	22	1 @ 1000	Al/Au intermetallic	1000 Hr. Life, T = 125°C	1	Teledyne; improper test, T_C = 200°C
Digital	585R927	16	0		1000 Hr. Life, T = 125°C	1	Teledyne
Digital	586R517	5	0		1000 Hr. Life, T = 125°C	1	Teledyne
Digital	585R928	22	1 @ 504 6 @ 1000	Al/Au intermetallic	1000 Hr. Life, T = 125°C	1	Teledyne; PR 1216; improper test, T_C = 200°C
Digital	585R928	22	0		1000 Hr. Life, T = 125°C	1	Teledyne
Linear	587R322	5	0		1000 Hr. Life, T = 125°C	1	Teledyne
Digital	587R323	7	2 @ 1000	Overstressed in test	1000 Hr. Life, T = 125°C	1	Teledyne
Digital	583R379	5	0		1000 Hr. Life, T = 125°C	1	Teledyne
Power Inv	584R550	3	1 @ 504	Cracked die	1000 Hr. Life, T = 125°C	2	WEC
Power Inv	584R550	5	0		1000 Hr. Life, T = 125°C	2	Solitron
Power Inv	584R550	2	1 @ 115	Cracked substrate	Temp Cycle/Thermal Shock 115 Cycles	2	WEC
Power Inv	584R550	1	1 @ 115	Detached substrate	Temp Cycle/Thermal Shock 115 Cycles	2	WEC, FA M30487
Power Inv	584R551	5	0		1000 Hr. Life, T = 125°C	2	Solitron
Power Inv	584R551	2	1 @ 15 shock	Cracked die	Temp Cycle/Thermal Shock 115 Cycles	2	WEC
Linear	581R772	2	0		Temp Cycle/Thermal Shock 1120 Cycles	1	WEC, FA M24087 Leads damaged due to mishandling
Linear	581R772	2	2 @ 1500	Al/Au intermetallic	3000 Hr. Life, T = 125°C	1	WEC, FA M20287
Linear	584R555	2	0		Temp Cycle/Thermal Shock 1120 Cycles	2	WEC, Test terminated @ 675
Linear	581R555	2	1 @ 750	Lifted bond wire	2500 Hr. Life, T = 125°C	2	WEC, FA M00188
Linear	585R149	2	0		1000 Hr. Life, T = 125°C	2	WEC
Linear	585R149	1	1 @ 15 shock	Leak	Temp Cycle/Thermal Shock 115 Cycles	2	WEC
Linear	585R150	3	1 @ 1000	Overstressed in test	1000 Hr. Life, T = 125°C	2	WEC, FA M18387

Table 4.4-2 (contd)

TYPE	P/N	QTY	FAILURES	FAILURE MECHANISM	TEST CONDITIONS	CASE	COMMENTS
Linear	585R150	2	1 @ 115	Cracked solder lid seal	Temp Cycle/Thermal Shock 115 Cycles	2	WEC, FA M26187
Power Reg	581R082	2	1 @ 2500	Substrate attach	3000 Hr. Life, T = 125°C	2	WEC, FA M29287
Power Reg	584R082	2	2 @ 75	Overstressed in test	Temp Cycle/Thermal Shock 1120 Cycles	2	WEC, FA M14687
Power Reg	585R151	2	0		1000 Hr. Life, T = 125°C	2	WEC
Power Reg	585R151	2	0		Temp Cycle/Thermal Shock 115 Cycles	2	WEC
Power Reg	586R508	1	0		Temp Cycle/Thermal Shock 115 Cycles	2	WEC
Power Reg	586R509A02	2	1 @ 168	Unknown	1000 Hr. Life	2	WEC
Power Reg	586R509A02	2	1 @ 15 shock	Unknown	Temp Cycle/Thermal Shock 115 Cycles	2	WEC
Power Reg	586R509A03	2	1 @ 15 shock	Substrate attach, cracked solder	Temp Cycle/Thermal Shock 115 Cycles	2	WEC, FA M26787
			1 @ 115	Lid seal			
Power Reg	586R508	2	1 @ 504	Poor die attach	1000 Hr. Life, T = 125°C	2	WEC
Video Amp	Several	941	2 @ 1000	Wire-wire short on torroid	1000 Hr. Life, T = 125°C	3	Q-Bit, No failures after insulation change
Video Amp	Several	9	0		1000 Hr. Life, T = 125°C	3	Q-Bit
Video Amp	Several	76	0		1000 Hr. Life, T = 125°C	1	Q-Bit
Video Digitizer	20858	3	0 @ 5760		Life, T = 125°C	4	Anaren
Video DC Restorer	20864	5	1 @ 1440	Seal	Life Test, T = 125°C	4	Anaren
			1 @ 3600	Seal			
			0 @ 2160				
			0 @ 2880				
			60				
Video Digitizer	24552	6	1 @ 720	Seal	Life Test, T = 125°C	4	Anaren
			1 @ 1440	Electrical			
			1 @ 2943	Electrical			
			1 @ 5281	Electrical			
Video Blanking	22106	6	1 @ 720	Seal	Life Test, T = 125°C	4	Anaren
			1 @ 1440	Electrical			
Video Threshold	22078	4	2 @ 6323	Electrical	Life Test, T = 125°C	4	Anaren

4.4.2 Model Development

The present version of the hybrid model as it appears in MIL-HDBK-217E is unnecessarily complex. It invokes failure rate dependency on the number of interconnects within the hybrid, the failure rates of the chips and film resistors, the substrate density, the seal perimeter and several multipliers. Some of the equations - such as the one indicating a temperature-dependence of the seal failure rate - have no physical basis. Therefore, the current effort has focused on simplifying the model while retaining reasonable accuracy. The new model presents the early life failure rate as being equal to the sum of the chip failure rates multiplied by π factors. The contributions due to wearout mechanisms are computed separately. The preliminary form of the model is therefore:

$$\lambda = [\ \lambda_C + \lambda_S\ ]\ \pi_i \ \ldots\ \pi_n \qquad (4.4.1)$$

See Sections 4.1 - 4.3 for VLSI chip failure rate calculations and 4.5 for packaging models. For all other semiconductor devices, the models in MIL-HDBK-217E are to be used. The chip capacitor model in MIL-HDBK-217E is to be used also.

No contributions to the hybrid failure rate from resistors, either chip or substrate, are considered. These failure rates are considered insignificant based on failure analysis experience and the life test data available. Published data on field reliability for hybrids (a paper published in the 1984 ISHM Proceedings, "Demonstrated Field Failure Rate for Custom Hybrids" by Murphy and Sainer, page 95) showed the failure rates for chip and substrate resistors to be 0.0008 and 0.000053 failures per million hours at 99% C.L.

The π_G factor has been eliminated from the model. The additional process steps and handling that the die are exposed to during the construction of a hybrid compensate for any reduction in failure rate due to the absence of the discrete package.

The package failure rate, as explained in section 4.5, is comprised of a base failure rate and failure rates which represent several wearout mechanisms. The

base package failure rate for hybrids, λ_S, is represented as being equal to a percentage of the total failure rate. The basis for this is that several studies have shown that packaged related failures represent approximately 40% of the total hybrid failures. MDR 14, "Hybrid Circuit Data, Winter 79/80" lists 40.6% of the field failures and 45.2% of the equipment test failures as being caused by package related defects. The previously referenced paper, "Demonstrated Field Failure Rate for Custom Hybrids" lists 39% of the verified hybrid failures to be package related. Furthermore, 40% is consistent with the percentage of hybrid failures attributable to package failures at Westinghouse. If the percentage of package failures is represented as K, then

$$\lambda = [\ \lambda_C + \frac{K}{1-K}\ \lambda_C\ ]\ \pi_i \ \ldots\ \pi_n \qquad (4.4.2)$$

$$= [\ \lambda_C\ (1 + \frac{K}{1-K})\ ]\ \pi_i \ \ldots\ \pi_n$$

Since the system environment will accelerate the failure of devices with point defects, an environmental factor is necessary to modify the base package failure rate.

To determine the relationship between the portion of failures due to package defects and the application environment, the data in MDR-14 was grouped by the application environment. The results are shown in Table 4.4-3 below.

Table 4.4-3: MDR-14 Data Summary

APPLICATION ENVIRONMENT	PACKAGE DEFECTS	TOTAL ANALYZED DEFECTS	$\frac{K}{1-K}$	π_E (FROM SECTION 4.6.4)
AU	18	32	1.2	5.5
AI	5	10	1.0	4.4
GF	24	63	0.6	2.5

A relationship of $K = 0.2\ \pi_E$ was established by plotting the data. The general form of the model now becomes

$$\lambda = [\lambda_C\ (1 + .2\ \pi_E)]\ \pi_i \ \ldots\ \pi_n \qquad (4.4.3)$$

It is our experience that, excluding secondary failures and erroneous removals,

the majority of hybrid failures experienced during life testing and field usage are caused by process related defects such as die attach and wire bonding. Therefore, the sum of the chip and package failure rates are multiplied by factors which are related to the difficulty of the process (π_F), the experience with the process (π_L), and the degree of screening employed to remove process related defects (π_Q).

The final form of the model is

$$\lambda_P = [\sum \lambda_C N_C (1 + .2 \pi_E)] \pi_Q \pi_L \pi_F \qquad (4.4.4)$$

where:

λ_C is the chip failure rate
N_C is the number of each chip
π_Q is the quality factor
π_F is the circuit function factor
π_L is the learning factor

The quality factor will be determined as detailed in section 4.6.1, the learning factor will be determined as detailed in section 4.6.2, and the function factor will be determined as detailed in section 4.6.3.

Additionally, the end of life package models of section 4.5 should be used to assess the mean time to failure (or cycles to failure) for the hybrid package, including the wirebonds, substrate and die attach, and hermeticity.

4.4.3 Chip Junction Temperature Calculation

Since the hybrid model is so heavily dependent upon the failure rates of the chips, it is imperative that the operating junction temperatures be calculated accurately. The best way to do this is through actual measurement (thermal survey) or finite element analysis, but this may not be practical for the reliability analyst. The following is a reasonable alternative for estimating the operating junction temperatures of the chips in a hybrid device.

A hybrid is normally made up of one or more substrate assemblies mounted within a sealed package. Each substrate assembly consists of active and passive chips with thick or thin film metallization mounted on the substrate, which in turn may have multiple layers of metallization and dielectric on the surface. Figure 4.4-1 is a cross-sectional view of a hybrid with a single multi-layered substrate. The layers within the hybrid are made up of various materials with different thermal characteristics. Table 4.4-4 provides a list of commonly used hybrid materials with typical thicknesses and corresponding thermal conductivities (K). The thermal resistance of each layer is determined by the expression.

$\Theta = (1/K)(L/A)$, where: (4.4.5)

Θ is the thermal resistance of a layer in °C/Watt (°C/W).
K is the material thermal conductivity from Table 4.4-4 (or user provided).
L is the material thickness in inches from Table 4.4-4 (or user provided).
A is the top surface area of the chip (user provided).

An estimated thermal resistance value for junction to case (Θ_{JC}) can be developed for each chip in the hybrid by summing the resistances of all the material layers of the hybrid structure from the chip down to the case:

$$\Theta_{JC} = \frac{\sum_{i=1}^{n} (1/K_i)\, L_i}{A}, \qquad (4.4.6)$$

where n is the number of material layers. Then,

$T_J = T_C + 0.9\ (\Theta_{JC})(P_D)$, where (4.4.7)

T_J is the junction temperature of the chip (°C)
T_C is the case temperature of the hybrid (°C)
Θ_{JC} is defined as above (°C/W), and
P_D is the power dissipated by the chip (W)

The factor of 0.9 in equation 4.4.7 represents the cosine of 26°. This angle accounts for the fact that the heat is not all conducted vertically from the chip to the case, but rather "spreads" radially as well as downward.

Figure 4.4-1

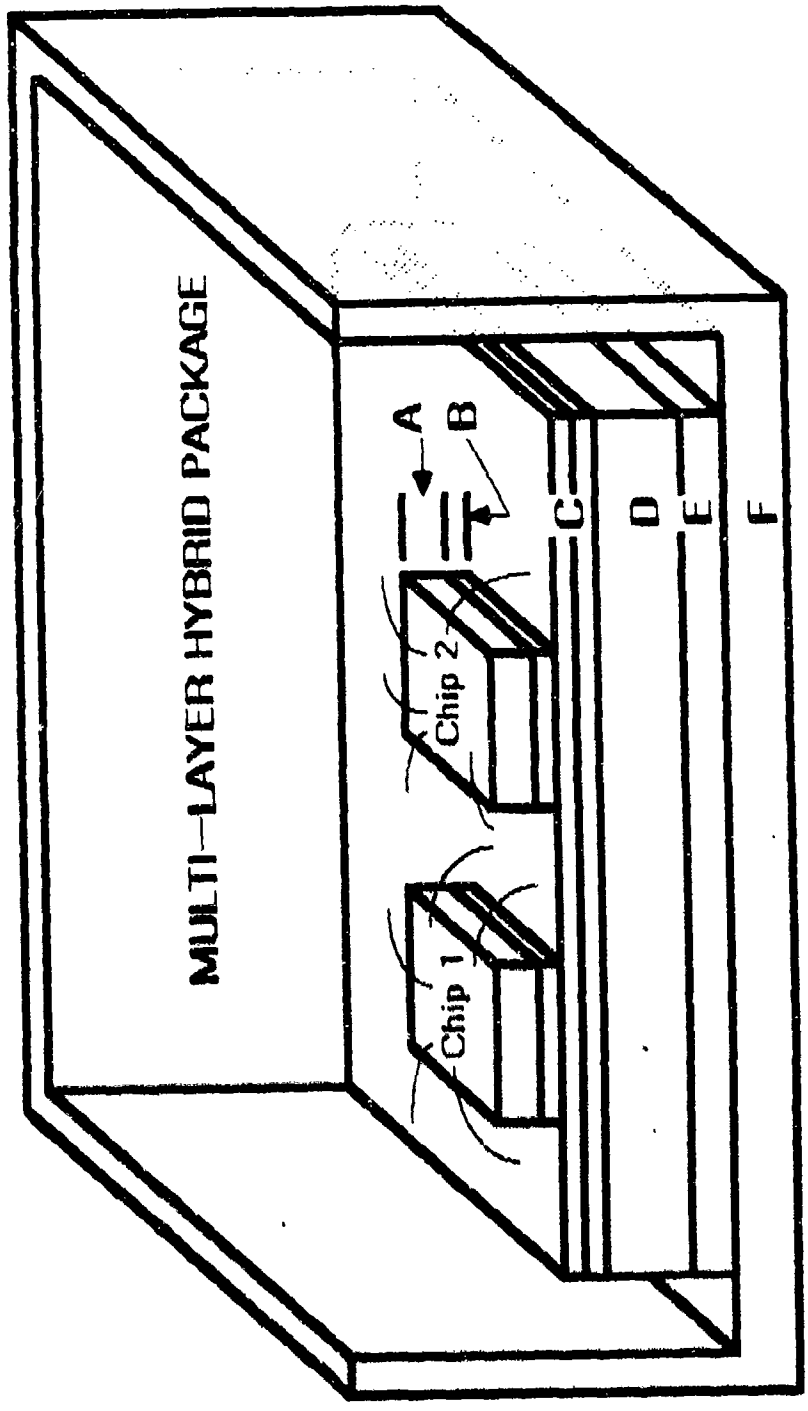


Table 4.4-4 Hybrid Materials

MATERIAL	TYPICAL USAGE	TYPICAL THICKNESS (")	FEATURE FROM FIGURE 4.4-1	K (W/°C-in)
Silicon	chip device	0.01	A	2.20
GaAs	chip device	0.007	A	0.76
Au Eutectic	chip attach	0.0001	B	6.91
Solder	chip/substrate attach	0.003	B/E	1.27
Epoxy (diel)	chip/substrate attach	0.0035	B/E	0.006
Epoxy (conductive)	chip attach	0.0035	B	0.15
Thick film dielectric	glass insulating layer	0.003	C	0.66
Alumina	Substrate, MHP	0.025	D	0.64
BeO	Substrate, PHP	0.025	D	6.58
Kovar	Case, MHP	0.02	F	0.425
Aluminum	Case, MHP	0.02	F	4.58
Copper	Case, PHP	0.02	F	9.96

4.5 FAILURE MECHANISMS OF MICROELECTRONIC PACKAGES

4.5.1 Introduction

The non-electrical failure mechanisms of a microelectronic device can be classified into package related failures, die failures and failures due to interconnects. Based on data from MDR-21, die failures constitute about 25-30% of the total failures, the package accounts for 40-50% of the failures, and interconnects involve 20-30% of the non-electrical failures in microelectronic packages.

In this section of this report we are concerned with package, interconnect and thermo-mechanical die, die attach and substrate attach failures. The package related failure sites include the package seal, package lid, package body, the lead frame, external leads and the package encapsulant. The die failure sites include the die, the die attach and the substrate attach. The interconnect failure sites include the wire, the wire bond and the conductor paths in the die and the substrate.

For simplicity we define all these failures as package failures. Package failures can be divided into two categories. The first includes failures that result from poorly controlled or poorly designed manufacturing processes. The second category consists of the failures caused during the normal operation of the device. This approach is justified when failures in the first category are removed during quality control inspection and screening processes. The package modeling effort has concentrated on the latter category, and the derived models are deterministic in nature.

In general, early and middle life failures are premature failures where causes can be "assigned" to specific defects or events. The early life failures typically exhibit a greater failure rate than do middle life failures. End of life failures are considered "common cause" failures. These failures are attributable to wire bond failure mechanisms, corrosion related failure mechanisms, and die attach related failure mechanisms.

MIL-HDBK-217E and its predecessors only consider assignable cause failures in the development of prediction models, since common cause failures do not typically occur within the life-times of military systems. The $C_2 \pi_E$ term as presented in Table 5.1.2.7-6 of MIL-HDBK-217E will continue to be used for the early and middle life failure predictions for the different package types. In addition, the pin grid array (PGA) package has been added to this table under the column "Hermetic Dual-In Line Package (DIP) with Solder Weld Seal."

For the most part, the DIP pin counts are in the 14 to 18 leads range (80 percent of devices produced annually) with the balance going up to 64 leads. However, when more than 40 external pins are needed, the conventional DIP becomes impractical because of increased internal density, pin spacing, increased weight and thermal limitations. At this point, the PGA becomes more practical, typically having pin counts of 14 or more, with 128, 224 and 525 being common variants, reference [98].

The justification for including the PGA packages with the DIP and LCC packages may be reviewed in references [99 and 100]. Briefly, it has been observed that the PGA packages are on a par with the industry standard DIP as to reject rate and failure modes during equivalent environmental screening. Many thousands of these packages have been tested by several different vendors. The recorded data indicate that the same controls and assembly techniques used for DIP's have been successfully transferred to PGA's with similar reliable results. Furthermore, no new failure modes characteristic to these packages have emerged. The thermal performance (junction to case thermal resistance) of a PGA package is equal to or less than that for a DIP, when selected package material, chip attach material, and heatsink attach epoxy and heatsink configurations are employed. The use of "fin" heatsinks configurations and aluminum-filled heatsink-attach epoxy with a lower bulk thermal resistance have produced thermal resistances less than 6°C/watt in PGA applications.

Therefore, based on these facts it would appear that the logical choice is to include the PGA packages under the DIP column in the C_2 table.

In the following paragraphs we discuss the end of life, or wearout, failure mechanisms and failure life models for the package, the interconnects and the die due to mechanical, thermo-mechanical and other environmental stresses.

Mathematical models developed used material properties which were in some cases estimated due to lack of experimental data. The accuracy of the models can be improved by using properties obtained from more extensive experiments on the material properties.

The failure prediction models recommended in this report can be described in generic terms as power law relationships between the mean cycles to failure and the local state of stress/strain in the specimen. This approach can be implemented either for crack initiation, as in Basquin's or Coffin-Manson equations, or for fatigue crack propagation, as in Paris's power law. The latter method is preferred when the material is likely to experience brittle crack propagation. In either situation the stress amplitude in the specimen has to be monitored and expressed in terms of the fatigue life of the material. Estimating the stress amplitude in the specimen can be a non-trivial task and needs a numerical scheme such as the finite element method. However, since the aim of the failure models cited below is to identify simple closed-form expressions for quick, on-line stress/strain analysis and for fatigue failure predictions, only approximate models are presented, with appropriate simplifications. For more accurate stress analysis, the user will need to employ the finite element or other appropriate numerical methods.

It is reiterated at this point that the accuracy of all the models depends on the simplifying assumptions about the material properties and associated constitutive equations. Due to the lack of appropriate data on electronic materials, simplified linear elastic behavior has been assumed in many cases, and the temperature dependence of all the material properties is ignored. It is clearly understood that material property data is essential for accurate life predictions and it is recommended that an extensive experimental program be undertaken to determine all the required data.

4.5.1.1 Wire-Wire Bond Related Failure Mechanisms

Fatigue is the dominant phenomenon causing the failure of the wire bond during normal life of microelectronic devices. Temperature and electrical power cycling can induce failure of the bond due to flexure and shear fatigue.

Repeated flexure of the wire due to temperature cycling can cause cracking of the wire at the heel due to bending fatigue. The differential thermal expansion of the bond pad and the substrate can result in a detachment of the bond pad from the substrate or the cracking of the substrate as a result of stresses generated. The differential thermal expansion between the bond pad and the wire can cause shear fatigue of the bond pad resulting in detachment of the wire from the substrate or cratering of the substrate. In plastic encapsulated packages, differential thermal expansion between the encapsulant and the wire can cause axial fatigue of the wire, resulting in tensile fatigue failure of the wire.

4.5.1.2 Corrosion Related Failure Mechanisms

Moisture and other contaminants can ingress into a package through flaws in the construction material or permeation through the wall of the package. Moisture can also be inherently trapped in the cavity of the package before being sealed. An extreme drop in temperature will cause the sealed cavity to attain its dew point and the moisture can condense on the surface of the chip and the wire bond. The condensed vapor together with other ionic contaminants will form an electrolyte for the transfer of ions essential for the wet corrosion process to occur.

The use of a passivation layer on integrated circuits has greatly reduced the corrosion problem although an imperfect passivation layer would promote pitting and eventually lead to corrosion of the metallization. In addition, due to the necessity of wire bonding, bond pads remain unpassivated and consequently are exposed to the package environment. Bond wires and bonds between dissimilar metal bond wires and bond pads or lead frames are

especially susceptible to corrosive attack. In practice, the die and die attach are not significantly affected by corrosion.

4.5.1.3 Die Related Failure Mechanisms

Another failure site in the microelectronic packages is the die assembly consisting of the die, die attach and the substrate attach. The major concern here is the mechanical failure, fracture and fatigue of the die die attach and substrate attach. Thermal stresses are induced in the die, the substrate and the case as a result of temperature fluctuations. Typically, microcracks present on the top surface or edges of the die or the edges of the die attach or the substrate attach can propagate under the influence of thermal stresses produced due to temperature cycling. This can cause the failure of the die due to horizontal or vertical cracking. A vertical crack is the result of large tensile stresses in the central portion of the top surface of the die. A horizontal crack of the die is the result of high shear stresses at the edges of the die. A failure of the die attach or the substrate attach is often the result of the presence of voids or microcracks near the edges, which propagate towards the center resulting in failure of the attach.

The die attach and substrate attach models delineated herein assume that the attach failure occurs in the bulk of the attach material. Each attach material forms an adhesive bond to the adjacent layer, i.e., an adhesive bond is formed between the die and the die attach and between the substrate and the die attach. Similarly, adhesive bonds are formed between the substrate attach and the adjacent substrate and package base surfaces. Failure of these adhesive bonds is not addressed in this report because it is felt that such failures are fabrication process related and will be detected during screen testing.

4.5.2 Fatigue Failure Models of Wire and Wire Bonds

4.5.2.1 Description of the Models

Failure of the wire bond occurs predominantly as a result of fatigue caused by

repeated flexure of the wire, shear stresses generated between the bond pad and the wire and shear stresses generated between the bond pad and the substrate, all resulting from temperature or power cycling.

Flexure of the wire will produce stresses at the heel of the bond in the case of wedge bonds and stitch bonds. Reversals in the bending stresses cause the eventual fatigue (breakage) of the wire at the heel. Due to the absence of any reduced section on the ball bond, failure due to flexure is uncommon for the ball bonds.

Shear stresses between the bond pad and the substrate result from the differences in the coefficients of thermal expansion between the substrate and the bond pad. This in turn results in the eventual detachment of the bond pad from the substrate, an increase in the thermal resistance between the die and the substrate, or the cratering of the substrate.

Shear stresses between the wire and the bond pad result from the differential thermal expansion between the wire and the substrate.

In encapsulated packages, if the encapsulant is in contact with the wire, the differential thermal expansion between the encapsulant and the wire can cause axial fatigue of the wire. This failure mechanism will not occur in encapsulated packages with a low modulus buffer coating between the wire and the encapsulant.

The number of cycles to failure of the wires and wire bonds in a microelectronic package depends on the environmental conditions, the geometry of the wire bond and the materials of the substrate, wire and bond pad. The fatigue failure prediction models take into account the environmental conditions and the geometry of the bond, which is consistent with the fact that the number of failures vary with the environmental conditions to which the wire bond is subjected. The stresses generated are a function of the geometry of the wire bond, the temperature fluctuation and the material properties.

The development of the models for wire and wire bond failure mechanisms are more fully discussed in Appendix F.

4.5.2.2 Wire and Wire Bond Failure Models

As discussed in 4.5.2.1, models have been developed for one bond wire and two bond pad failure mechanisms, as follows:

(1) Bond Wire Flexure Fatigue

The model for the number of cycles to flexure fatigue failure is defined by equation F5.8 as follows:

$$N_{f(flex)} = A_1 (\varepsilon_f)^{n_1} \qquad \text{(F5.8)}$$

where:

$N_{f(flex)}$ is the number of cycles to failure for the wire in flexure.

A_1 is a material property dependent coefficient for the wire material obtained from Table 4.5-4.

N_1 is a material property dependent exponent for the wire material obtained from Table 4.5-4.

ε_f is the wire strain magnitude and is defined by equation F5.7a as follows:

$$\varepsilon_f = \frac{r}{35.1} \left| \frac{\text{Cos}^{-1}(0.966\ (1 - (\alpha_w - \alpha_s)\ \Delta T))}{15} - 1 \right| \qquad \text{(F5.7a)}$$

where:

r is the radius of the wire, mm.

α_w is the coefficient of thermal expansion of the wire obtained from Table 4.5-1.

α_s is the coefficient of thermal expansion of the substrate obtained from Table 4.5-2.

ΔT is the temperature difference obtained from Table 4.5-17.

(2) Shear Fatigue at Bond Pad/Substrate Interface

The model for the number of cycles to shear fatigue failure is defined by equation F5.10 as follows:

$$N_{f(shear)s} = A_2(\varepsilon_{fs})^{n_2} \qquad (F5.10)$$

where:

$N_{f(shear)s}$ is the number of cycles to failure in shear at the bond pad/substrate interface.

A_2 is a material property dependent coefficient for the bond pad material obtained from Table 4.5-5.

n_2 is a material property dependent exponent for the bond pad material obtained from Table 4.5-5.

ε_f is the bond pad shear strain magnitude and is defined by equation F5.9 as follows:

$$\varepsilon_{fs} = K\,\Delta T \qquad (F5.9)$$

where:

K is a constant for a particular pad/substrate combination obtained from Table 4.5-6.

ΔT is the temperature difference encountered, obtained from Table 4.5-17.

(3) Shear Fatigue at Bond Pad/Wire Interface

The model for the number of cycles to shear fatigue failure at the bond pad/wire interface is identical to the model for shear fatigue failure at the bond pad/substrate interface and is defined by equation F5.10 as follows:

$$N_{f(shear)w} = A_2(\varepsilon_{fs})^{n_2} \quad \text{(F5.10)}$$

where:

$N_{f(shear)w}$ is the number of cycles to failure for the wire in shear at the bond pad/wire interface.

A_2 is a material property dependent coefficient for the wire material obtained from Table 4.5-5.

n_2 is a material property dependent exponent for the wire material obtained from Table 4.5-5.

ε_f is the wire shear strain magnitude and is defined by equation F5.14 as follows:

$$\varepsilon_{fs} = (1/2)\ |\alpha_w - \alpha_s|\ \Delta T \quad \text{(F5.14)}$$

where:

α_w is the coefficient of thermal expansion of the wire obtained from Table 4.5-1.

α_s is the coefficient of thermal expansion of the substrate obtained from Table 4.5-2.

ΔT is the temperature difference encountered by the component obtained from Table 4.5-17.

4.5.2.3 Application Examples for Wire/Wire Bond Failure Models

(1) Bond Wire Flexure Fatigue

(A) Assume a microcircuit with a Represetative Microcircuit Configuration (RMC) as defined in paragraph 4.5.6 and used in a MIL-HDBK-217 ground-fixed (G_F) application environment. Then the mean number of cycles to failure due to bond wire flexure fatigue is found from equations F5.7a and F5.8, which are combined following:

$$N_{f(flex)} = A_1 \left\{ \frac{r}{35.1} \left[\frac{\cos^{-1}\left(0.966(1-(\alpha_w - \alpha_s)\Delta T)\right) - 1}{15} \right] \right\}^{n_1} \qquad \begin{matrix}(F5.7a \\ \& \\ F5.8)\end{matrix}$$

The variables in this equation are defined in paragraph 4.5.2.2(1) and data are obtained from the following sources:

VARIABLE	VALUE	UNITS	SOURCE
A_1	3.9323×10^{-10}	N/A	Table 4.5-4
n_1	-5.134	N/A	Table 4.5-4
r	1.6×10^{-2}	mm	RMC-Para 4.5.6
α_w	23.2×10^{-6}	m/m/°c	Table 4.5-1
α_s	4.67×10^{-6}	m/m/°c	Table 4.5-2
ΔT	55	°c	Table 4.5-17

Substituting in equations F5.7a and F5.8:

$$N_{f(flex)} = 3.9323\times10^{-2}\left\{\frac{1.6 \times 10^{-2}}{35.1}\left[\frac{\cos^{-1}(0.966(1-(23.2\times10^{-6}-4.67\times10^{-6})55))-1}{15}\right]\right\}^{5.134}$$

$$= 5.6 \times 10^{7} \left[\frac{\cos^{-1}(0.9650155011)-1}{15} \right]^{-5.134}$$

$$= 2.357 \times 10^{17} \text{ cycles}$$

(B) Assume the same conditions as paragraph 4.5.2.3(1)(A) except bond wire diameter is 0.127mm (5 mils). Then $r = 0.127/2 = 6.35 \times 10^{-2}$mm and all other variables remain the same. Substituting in equations F5.7a and F5.8:

$$N_{f(flex)} = 3.9323\times10^{-10}\left\{\frac{6.35 \times 10^{-2}}{35.1}\left[\frac{\cos^{-1}(0.966(1-(23.2\times10^{-6}-4.67\times10^{-6})55))-1}{15}\right]\right\}^{-5.134}$$

$$= 1.987 \times 10^{14} \text{ cycles}$$

(C) Assume the same conditions as 4.5.2.3(1)(B) except bond wire material is gold. Then $A_1 = 3.5844 \times 10^{-11}$ and $n_1 = -4.9828$ from Table 4.5-4, and all other variables remain the same. Substituting in equations F5.7a and F5.8:

$$N_{f(flex)} = 3.5844 \times 10^{-11} \left\{ \frac{6.35 \times 10^{-2}}{35.1} \left[\frac{\cos^{-1}(0.966(1-(23.2 \times 10^{-6} - 4.67 \times 10^{-6})55))_{-1}}{15} \right] \right\}^{-4.9828}$$

$$= 3.636 \times 10^{12} \text{ cycles}$$

(2) Bond Pad/Die Interface Shear Fatigue

(A) Assume a microcircuit with a Representative Microcircuit Configuration (RMC) as defined in paragraph 4.5.6 and used in a MIL-HDBK-217 ground-fixed (G_F) application environment. Then the mean number of cycles to failure due to bond pad/die interface shear fatigue is found from equations F5.9 and F5.10, which are combined following:

$$N_{f(shear)s} = A_2 (K\Delta T)^{n_2} \qquad \text{(F5.9 \& F5.10)}$$

The variables in this equation are defined in paragraph 4.5.2.2(2) and data are obtained from the following sources:

VARIABLE	VALUE	UNITS	SOURCE
A_2	4.3386×10^{-11}	N/A	Table 4.5-5
n_2	-5.134	N/A	Table 4.5-5
K	1.46×10^{-5}	N/A	Table 4.5-6
ΔT	55	°C	Table 4.5-17

Substituting in equations F5.9 and F5.10:

$$N_{f(shear)s} = 4.3386 \times 10^{-11} (1.46 \times 10^{-5})(55))^{-5.134}$$

$$= 3.377 \times 10^{5} \text{ cycles}$$

(B) Assume the same conditions as paragraph 4.5.2.3(2)(A) except bond pad material is gold. then from Table 4.5-5, $A_2 = 4.2948 \times 10^{-12}$ and $n_1 = -4.9828$, and from Table 4.5-6, $K = 0.90 \times 10^{-5}$. All other variables remain the same. Substituting in equations F5.9 and F5.10:

$$N_{f(shear)s} = 4.2948 \times 10^{-12} \, (0.90 \times 10^{-5}(55))^{-4.9828}$$
$$= 1.268 \times 10^{5} \text{ cycles}$$

(3) Bond Pad/Wire Interfare Shear Fatigue

(A) Assume a microcircuit with a Representative Microcircuit Configuration (RMC) as defined in paragraph 4.5.6 except wire material is gold. The device is used in a MIL-HDBK-217 ground-fixed (G_F) application environment. Then the mean number of cycles to failure is found from equations F5.10 and F5.14, which are combined following:

$$N_{f(shear)w} = A_2 \left[\frac{|\alpha_w - \alpha_s| \Delta T}{2} \right]^{n_2} \qquad \text{(F5.10 \& F5.14)}$$

The variables in this equation are defined in paragraph 4.5.2.2(3) and data are obtained from the following sources:

VARIABLE	VALUE	UNITS	SOURCE
A_2	4.2948×10^{-12}	N/A	Table 4.5-5
n_2	-4.9828	N/A	Table 4.5-5
α_w	14.2×10^{-6}	m/m/°c	Table 4.5-1
α_s	4.67×10^{-6}	m/m/°c	Table 4.5-2
ΔT	55	°c	Table 4.5-17

Substituting in equations F5.10 and F5.14:

$$N_{f(shear)w} = 4.2948 \times 10^{12} \left[\frac{\left|14.2 \times 10^{-6} - 4.67 \times 10^{-6}\right| (55)}{2} \right]^{-4.9828}$$

$$= 3.014 \times 10^{6} \text{ cycles}$$

(B) Assume the same conditions as paragraph 4.5.2.3 except pad material is gold and wire material is aluminum. Then the following data is obtained:

VARIABLE	VALUE	UNITS	SOURCE
A_2	4.3386×10^{-11}	N/A	Table 4.5-5
n_2	-5.134	N/A	Table 4.5-5
α_w	23.2×10^{-6}	m/m/°C	Table 4.5-1
α_s	4.67×10^{-6}	m/m/°C	Table 4.5-2

Substituting in equations F5.10 and F5.14:

$$N_{f(shear)w} = 4.3386 \times 10^{-11} \left[\frac{\left|23.2 \times 10^{-6} - 4.67 \times 10^{-6}\right| (55)}{2} \right]^{-5.134}$$

$$= 3.488 \times 10^{6} \text{ cycles}$$

4.5.2.4 Evaluation

The results from the application examples given in paragraph 4.5.2.3 are summarized following:

FAILURE MECHANISM	MICROCIRCUIT CONFIGURATION*	N_f (cycles)
Bond Wire	RMC	2.4×10^{17}
Flexure	RMC except: 5 mil bond wire	2.0×10^{14}
Fatigue	RMC except: 5 mil bond wire : gold bond wire	3.6×10^{12}
Bond Pad/Die Interface Shear Fatigue	RMC	3.4×10^{5}
	RMC except: gold bond pad	1.3×10^{5}
Bond Pad/Wire Interface Shear Fatigue	RMC except: gold bond wire	3.0×10^{6}
	RMC except: gold bond pad	3.5×10^{6}

*RMC is defined in paragraph 4.5.6

These failure predictions are consistent with the fact that flexure failures are less often seen as compared to the failures do to shear fatigue. Nevertheless, this does not rule out the possibility of failure due to flexure. Given a different set of environmental conditions, flexure could be the dominant mechanism, since the stress due to flexure depends not only on the temperature conditions and the materials in consideration but also on the geometry of the bond wire e.g. wire diameter, radius of curvature at the bond, the angle of the bond wire with the substrate, etc. Therefore, a change in wire diameter for the same environmental conditions may cause an increase in the flexure stresses without significantly changing the shear fatigue stresses. The relative importance of each of these failure mechanisms is subject to the various factors on which each of the mechanisms depend.

From the summary table it is seen that the bond pad material has negligible effect on the bond pad/die interface shear fatigue mechanism. This supports existing knowledge gained from failure analysis that the failure usually occurs in the bulk die material immediately below the pad due to bulk defects in the die acting as failure initiation sites.

The bond pad/wire interface shear fatigue mechanism can occur only when the pad and the wire are of dissimilar materials. The summary table shows that the choice of material for either member has little effect on life when the same two materials are paired.

4.5.3 Failure Models for the Die, Die Attach and Substrate Attach, Fracture and Fatigue

4.5.3.1 Description of the Models

The die attach unit of microelectronic component packages consists of the die or chip and the substrate and the case, which are usually made of different materials and therefore have different thermal expansion coefficients. During environmental thermal and power cycling, as the temperature fluctuates, longitudinal and shear stresses are introduced in the package.

Microcracks are typically introduced in the die during manufacturing operations and are present at the edges of the die. If a microcrack is large enough, i.e. if it is equal to or greater than a critical crack size, the die may fail in the first power cycle. If the microcrack is less than the critical crack size, then during temperature cycling, it may propagate and eventually the die would fail when this crack reaches the critical size.

Different thermal expansion coefficients of the die, substrate and case and the presence of edge voids in the attach materials introduce high stresses and are responsible for the failure of the die attach and the substrate attach. The voids in the attach materials may act as microcracks, which may propagate during temperature cycling and eventually cause delamination of the die or the substrate.

A fracture mechanics approach is taken to calculate the critical crack size in the die. If the initial crack size is smaller than the critical crack size then Paris's power law of fatigue crack propagation is used to calculate the number of cycles for the crack to grow to critical size. The die attach and substrate attach materials fail by ductile mechanisms and hence the linear elastic fracture mechanics (LEFM) approach is not appropriate in this situation. The Manson-Coffin relationship is used therefore, to calculate the number of cycles to failure in die attach and substrate attach.

The development of the models for die, die attach and substrate attach fracture and fatigue are more fully discussed in appendix G.

4.5.3.2. Die, Die Attach and Substrate Attach Failure Models

As discussed in 4.5.3.1, models have been developed for die brittle cracking, die fatigue cracking, die attach fatigue and substrate attach fatigue and fatigue failure mechanisms, as follows:

(1) Die Brittle Cracking

Brittle failure of a die with a vertical edge crack can occur upon first application of thermomechanical stress when the criterion defined in equation G.4 is satisfied:

$$a_i \geq a_c \tag{G.4}$$

where

a_i is the initial crack length, meters

a_c is the critical crack length, meters, required to cause rapid propagation of the crack through the die, and is defined by equation G.5 as follows:

$$a_c = \frac{K_{IC}^2}{\pi \sigma_{app}^2} \tag{G.5}$$

where

K_{IC} is the fracture toughness of the die material obtained from Table 4.5-7.

σ_{app} is the maximum applied tensile stress in the die and is defined by equation G.6 as follows:

$$\sigma_{app} = 2 \times 10^{-7} \mid \alpha_s - \alpha_d \mid \Delta T \sqrt{E_s E_a L/x} \tag{G.6}$$

where

α_s is the coefficient of thermal expansion of the substrate to which the die is mounted, obtained from Table 4.5-9.

α_d is the coefficient of thermal expansion of the die obtained from Table 4.5-7.

ΔT is the temperature difference encountered, obtained from Table 4.5-17.

E_s is the tensile (Young's) modulus of the substrate obtained from Table 4.5-9.

E_a is the tensile (Young's) modulus of the die attach obtained from Table 4.5-8.

x is the die attach thickness, meters obtained from Table 4.5-18.

L is the diagonal length of the die, meters, and may be approximated by equation G.7 as follows:

$$L = 1.5 \times 10^{-3} + 1.0 \times 10^{-4} P \qquad (G.7)$$

where P is the number of active pin terminals in the microcircuit.

(2) Die Fatigue Cracking

The model for the number of cycles to die fatigue cracking failure is defined by equation G.10e as follows:

$$N_f = \frac{2}{(n-2)\, A\, \sigma_{app}^{n}\, \pi^{n/2}} \left[\frac{1}{a_i^{((n-2)/2)}} - \frac{1}{a_f^{((n-2)/2)}} \right] \qquad (G.10e)$$

for $n \neq 2$

where

N_f is the number of cycles to die fatigue cracking failure.

n is a material property dependent exponent for the die material obtained from Table 4.5-7.

A is a material property dependent coefficient for the die material obtained from Table 4.5-7.

a_i is the initial crack length, meters

a_f is the final crack length at failure, meters

MIL-STD-883, Method 2010 visual criteria for die cracks prohibits any surface cracks in an active circuit area of the die and prohibits any edge cracks with a total length greater than tabulated below, or edge cracks with a total length greater than tabulated below, or edge cracks of lesser length that extend more than 1 mil past the scribe grid line along the die edge:

Quality Level	Maximum Crack Length
B	5 mils
S	3 mils

It can be expected than any population of microcircuit dice will contain a

proportion of cracks up to the limit of acceptability. It can be further expected that these cracks will propagate during operational use of the completed microcircuits due to thermomechanically induced stress. The increase in crack length required for an allowable crack to enter active areas of the die and cause failure will vary depending upon the inital directional orientation of the crack and its proximity to the die active area pattern geometry. It is believed that it is conservative to assume that crack propagation to a total length of 15 mils is the maximum that can be permitted before penetration of an active area is imminent. From the visual acceptance criteria and this assumption, appropriate values for a_i and a_f are proposed as follows:

Quality Level	a_i	a_f
B	1.3×10^{-4}m (5 mils)	3.8×10^{-4}m (15 mils)
S	7.6×10^{-5}m (3 mils)	3.8×10^{-4}m (15 mils)

(3) Die Attach Fatigue

The model for the number of cycles to die attach fatigue failure is defined by equations G.11 and G.12 which are combined as follows:

$$N_f = 0.5 \left| \frac{L \, |\alpha_s - \alpha_d| \, \Delta T}{x \, \gamma_f} \right|^{1/c} \qquad \text{(G.11) \& (G.12)}$$

where:

N_f is the number of cycles to die attach fatigue failure.

α_s is the coefficient of thermal expansion of the substrate obtained from Table 4.5-9.

α_d is the coefficient of thermal expansion of the die obtained from Table 4.5-7.

ΔT is the temperature difference encountered, obtained from Table 4.5-17.

x is the height of die attach, meters, obtained from Table 4.5-18.

γ_f is the fatigue ductility coefficient (defined as the shear strain required to cause failure in one load reversal) obtained from Table 4.5-8.

c is the Manson-Coffin fatigue exponent (slope of low cycle fatigue curve of log shear strain vs. log cycles to failure) obtained from Table 4.5-8.

L is the diagonal length of the die, meters, and may be approximated by equation G.7 as follows:

$$L = 1.5 \times 10^{-3} + 1.0 \times 10^{-4} P \qquad (G.7)$$

where P is the number of active pin terminals in the microcircuit.

(4) Substrate Attach Fatigue

The model for the number of cycles substrate attach fatigue failure is similar to the die attach fatigue failure model and is defined by equation (G.13) as follows:

$$N_f = 0.5 \left[\frac{L_s \left| \alpha_c - \alpha_s \right| \Delta T}{x_{sa} \, Y_f} \right]^{1/c} \qquad (G.13)$$

where:

L_s is the diagonal length of substrate, meters.

α_c is the coefficient of thermal expansion of the case obtained from Table 4.5-10.

α_s is the coefficient of thermal expansion of the substrate obtained from Table 4.5-9.

ΔT is the temperature difference encountered obtained from Table 4.5-17.

x_{sa} is the thickness of the substrate attach, meters obtained from Table 4.5-18.

Y_f' is the fatigue ductility coefficient of substrate attach (defined as the shear strain required to cause failure in one load reversal) obtained from Table 4.5-8

c is the Manson-Coffin fatigue exponent (slope of low cycle fatigue curve of log shear strain vs. log cycles to failure) obtained from Table 4.5-8

4.5.3.3 Application Examples for the Die, Die Attach and Substrate Attach Failure Models.

(1) Die Brittle Cracking

(A) Assume a micrccircuit with a Representative Microcircuit Configuration (RMC) as defined in paragraph 4.5.6 and use in a MIL-HDBK-217 ground-fixed (G_F) application environment. Brittle failure of a die will occur upon first application of thermomechanical stress if criterion equation G.4 is satisfied. Evaluation of this criterion requires solution of equations G.5 and G.6, which are combined following:

$$a_c = \frac{K_{IC}^2}{\Pi(2 \times 10^{-7} \, |\alpha_s - \alpha_d| \, \Delta T \sqrt{E_s E_a \, L/x})^2} \qquad \text{(G.5 \& G.6)}$$

The variables in this equation are defined in paragraph 4.5.3.2(1) and data are obtained from the following sources:

VARIABLE	VALUE	UNITS	SOURCE
K_{IC}	0.82	M Pa $\sqrt{m}$	Table 4.5-7
α_s	7.3×10^{-6}	m/m/°c	Table 4.5-9
α_d	4.67×10^{-6}	m/m/°c	Table 4.5-7
E_s	255×10^{9}	Pa	Table 4.5-9
E_a	2.8×10^{9}	m	RMC
x	5.1×10^{-5}	m	RMC
ΔT	55	°c	Table 4.5-17
L	3.22×10^{-3}	m	RMC

Substituting in equations G.5 and G.6:

$$a_c = \frac{(0.82)^2}{\Pi(2\times10^{-7}|7.3\times10^{-6}-4.67\times10^{-6}|(55)\sqrt{(255\times10^{9})(2.8\times10^{9})(3.22\times10^{-3})5.1\times10^{-5})^2}}$$

$$= \frac{0.6724}{\Pi(37.7295)} = 5.673 \times 10^{-3}\text{m (223 mils)}$$

From the specified MIL-STD-883 quality level for the RMC it is found from paragraph 4.5.3.1(2) in the discussion following equation G.10e that a_i = 1.3×10^{-4}m (5 mils). Applying the criterion equation G.4:

$$a_i \geq a_c \qquad (G.4)$$

Substituting in equation G.4:

$$1.3 \times 10^{-4} < 5.673 \times 10^{-3}$$

Hence, die brittle cracking will not occur.

(B) Assume the same conditions as 4.5.3.3(1)(A) ewxcept the die attach material is Au-Si eutectic and the die diagonal length is 0.01m (400 mils) and all other variables remain the same. Then from Table 4.5-18, x = 2.5×10^{-6}m (0.1 mil) and from Table 4.5-8, $E_a = 59.2 \times 10^9$ Pa. Substituting in equations G.5 and G.6:

$$a_c = \frac{(0.82)^2}{[(2\times10^{-7}|7.3\times10^{-6}\underline{4}.67\times10^{-6}|(55)\sqrt{(255\times10^9)(59.2\times10^9)(1\times10^{-2})/(2.5\times10^{-6})})^2}$$

$$= \frac{0.6724}{\pi(50538)} = 4.235 \times 10^{-6}\text{m (0.17 mils)}$$

Substituting in criterion equation G.4:

$$1.3 \times 10^{-4} > 4.2 \times 10^{-6}$$

Hence, die brittle cracking will occur upon first application of thermomechanical stress (provided a maximum acceptable size crack from MIL-STD-883 visual criteria is present).

(2) Die Fatigue Cracking

(A) Assume a microcircuit with a Representative Microcircuit Configuration (RMC) as defined in paragraph 4.5.6 and use in a MIL-HDBK-217

ground-fixed (G_F) application environment. Then the mean number of cycles to failure due to die fatigue cracking is found from equation G.10e:

$$N_f = \frac{2}{(n-2)A\,\sigma_{app}^{\,n}\,\Pi^{n/2}}\left[\frac{1}{a_i^{((n-2)/2)}} - \frac{1}{a_f^{((n-2)/2)}}\right],\ n \neq 2 \qquad \text{(G.10e)}$$

where σ_{app} is found from equation G.6:

$$\sigma_{app} = 2 \times 10^{-7}|\alpha_s - \alpha_d|\Delta T\sqrt{E_s E_a\, L/x} \qquad \text{(G.6)}$$

The variables in these equations are defined in paragraphs 4.5.3.2(1) and 4.5.3.2(2) and data are obtained from the following sources:

VARIABLE	VALUE	UNITS	SOURCE
n	4	N/A	Table 4.5-7
A	1×10^{-12}	N/A	Table 4.5-7
a_i	1.3×10^{-4}	m	RMC
a_f	3.8×10^{-4}	m	Para 4.5.3.2(2)
K_{IC}	0.82	M Pa $\sqrt{m}$	Table 4.5-7
α_s	7.3×10^{-6}	m/m/°C	Table 4.5-9
α_d	4.67×10^{-6}	m/m/°C	Table 4.5-7
E_s	255×10^{9}	Pa	Table 4.5-9
E_a	2.8×10^{9}	Pa	Table 4.5-8
x	5.1×10^{-5}	m	RMC
L	3.22×10^{-3}	m	RMC
ΔT	55	°C	Table 4.5-17

Substituting in equation G.6:

$$\sigma_{app} = 2\times10^{-7}|7.3\times10^{-6}-4.67\times10^{-6}|(55)\sqrt{(255\times10^{9})(2.8\times10^{9})(3.22\times10^{-3})/(5.1\times10^{-5})}$$

$$= 6.142 \text{ MPa}$$

Applying this result to equation G.10e:

$$N_f = \frac{2}{(2)(1 \times 10^{-12})(6.142)^4 \Pi^2}\left[\frac{1}{1.3 \times 10^{-4}} - \frac{1}{3.8 \times 10^{-4}}\right] \qquad \text{(G.10e)}$$

$$= 3.603 \times 10^{11} \text{ cycles}$$

(B) Assume the same conditions as paragraph 4.5.3.3(2)(A) except the die attach material is Au-Si eutectic and the die diagonal length is 1×10^{-2}m (400 mils) and all other variables remain the same. Then from Table 4.5-18, $x = 2.5 \times 10^{-6}$m (0.1 mil) and from Table 4.5-8, $E_a = 59.2 \times 10^9$ MPa. Substituting in equation G.6:

$$\sigma_{app} = 2\times10^{-7}\left|7.3\times10^{-6}-4.67\times10^{-6}\right|(55)\sqrt{(255\times10^9)(59.2\times10^9)(1\times10^{-2})/(2.5\times10^{-6})}$$

$$= 212.5 \text{ MPa}$$

Applying this result to equation G.10e:

$$N_f = \frac{2}{(2)(1 \times 10^{-12})(212.5)^4 \Pi^2}\left[\frac{1}{1.3 \times 10^{-4}} - \frac{1}{3.8 \times 10^{-4}}\right]$$

$$= 2.515 \times 10^5 \text{ cycles}$$

(C) Assume the same conditions as paragraph 4.5.3.3(2)(B) except the MIL-STD-883 quality level is Class S. This implies that $a_i = 7.6 \times 10^{-5}$m (3 mils) and all other variables remain the same. Applying the previous result for equation G.6 and substituting in equation G.10e:

$$N_f = \frac{2}{(2)(1 \times 10^{-12})(212.5)^4 \Pi^2}\left[\frac{1}{7.6 \times 10^{-5}} - \frac{1}{3.8 \times 10^{-4}}\right]$$

$$= 5.230 \times 10^5 \text{ cycles}$$

(3) Die Attach Fatigue

(A) Assume a microcircuit with a Representative Microcircuit Configuration (RMC) as defined in paragraph 4.5.6 and used in a MIL-HDBK-217 ground-fixed (G_F) application environment. Then the mean number of cycles to failure due to die attach fatigue is found from equations G.11

and G.12, which are combined following:

$$N_f = \frac{1}{2}\left[\frac{L|\alpha_s - \alpha_d|\,\Delta T}{x\gamma_f}\right]^{1/c} \qquad \text{(G.11 \& G.12)}$$

The variables in this equation are defined in paragraph 4.5.3.2(3) and data are obtained from the following sources:

VARIABLE	VALUE	UNITS	SOURCE
L	3.22×10^{-3}	m	RMC
α_s	7.3×10^{-6}	m/m/°c	Table 4.5-9
α_d	4.67×10^{-6}	m/m/°c	Table 4.5-7
ΔT	55	°c	Table 4.5-17
x_i	5.1×10^{-5}	m	RMC
γ_f	1.1	N/A	Table 4.5-8
c	-0.49	N/A	Table 4.5-8

Substituting in equations G.11 and G.12:

$$N_f = \frac{1}{2}\left[\frac{(3.22 \times 10^{-3})|7.3 \times 10^{-6} - 4.67 \times 10^{-6}|(55)}{(5.1 \times 10^{-5})(1.1)}\right]^{1/-0.49}$$

$$= 8.820 \times 10^{3} \text{ cycles}$$

(B) Assume the same conditions as paragraph 4.5.3.3(3)(A) except the die attach material is Au-Si eutectic, and all other variables remain the same. Then from Table 4.5-18, $x = 2.5 \times 10^{-6}$m (0.1 mil). Substituting in equations G.11 and G.12:

$$N_f = \frac{1}{2}\left[\frac{(3.22 \times 10^{-3})|7.3 \times 10^{-6} - 4.67 \times 10^{-6}|(55)}{(2.5 \times 10^{-6})(1.1)}\right]^{1/-0.49}$$

$$= 19 \text{ cycles}$$

(4) Substrate Attach Fatigue

(A) Assume a hybrid microcircuit used in a MIL-HDBK-217 ground-fixed (G_F) application environment with the following configuration:

Package Material - Copper
Substrate Material - Alumina Ceramic
Substrate Attach - Au-Si eutectic
Substrate Size - 1.91×10^{-2}m square (.75 in square)

Then the mean number of cycles to failure due to substrate attach fatigue is found from equation G.13:

$$N_f = \frac{1}{2}\left[\frac{L_s \mid \alpha_c - \alpha_s \mid \Delta T}{x_{sa}\, Y_f'}\right]^{1/c} \qquad (G.13)$$

The variables in this equation are defined in paragraph 4.5.3.2(4) and data are obtained from the following sources:

VARIABLE	VALUE	UNITS	SOURCE
L_s	2.7×10^{-2}	m	configuration: $(\sqrt{2}\,(1.91 \times 10^{-2}))$
α_c	16.9×10^{-6}	m/m/°c	Table 4.5-10
α_s	7.3×10^{-6}	m/m/°c	Table 4.5-9
ΔT	55	°c	Table 4.5-17
x_{sa}	2.5×10^{-6}	m	Table 4.5-18
Y_f	1.1	N/A	Table 4.5-8
c	-0.49	N/A	Table 4.5-8

Substituting in equation G.13:

$$N_f = \frac{1}{2}\left[\frac{(2.7 \times 10^{-2}) \mid 16.9 \times 10^{-6} - 7.3 \times 10^{-6} \mid (55)}{(2.5 \times 10^{-6})(1.1)}\right]^{1/-0.49}$$

$= 1.7 \times 10^{-2}$ cycles i.e. will not survive the first thermal cycle.

(B) Assume the same conditions as paragraph 4.5.3.3(4)(A) except the die attach material is 70-30 In-Pb solder, and all other variables remain the

same. Then from Table 4.5-18, $x_{sa} = 1.5 \times 10^{-4}$m (6 mils). Substituting in equation G.13:

$$N_f = \frac{1}{2}\left[\frac{(2.7 \times 10^{-2})|16.9 \times 10^{-6} - 7.3 \times 10^{-6}|(55)}{(1.5 \times 10^{-4})(1.1)}\right]^{1/-0.49}$$

$$= 74 \text{ cycles}$$

(C) Assume the same conditions as paragraph 4.5.3.3(4)(A) except the package material is Kovar, and all other variables remain the same. Then from Table 4.5-10, $\alpha_c = 5.2 \times 10^{-6}$ m/m/°c. Substituting in equation G.13:

$$N_f = \frac{1}{2}\left[\frac{(2.7 \times 10^{-2})|5.2 \times 10^{-6} - 7.3 \times 10^{-6}|(55)}{(2.5 \times 10^{-6})(1.1)}\right]^{1/-0.49}$$

$= 3.9 \times 10^{-1}$ cycles i.e. will not survive the first thermal cycle.

(D) Assume the same conditions as paragraph 4.5.3.3(4)(A) except the package material is Kovar and the die attach material is 70-30 In-Pb solder, and all other variables remain the same. Then from Table 4.5-10, $\alpha_c = 5.2 \times 10^{-6}$ m/m/°c and from Table 4.5-18, $x_{sa} = 1.5 \times 10^{-4}$m (6 mils). Substituting in equation G.13:

$$N_f = \frac{1}{2}\left[\frac{(2.7 \times 10^{-2})|5.2 \times 10^{-6} - 7.3 \times 10^{-6}|(55)}{(1.5 \times 10^{-6})(1.1)}\right]^{1/-0.49}$$

$= 1646$ cycles

(E) Assume the same conditions as paragraph 4.5.3.3(4)(D) except the substrate size is 1.27×10^{-2}m square (0.5 in square). Then $L_s = \sqrt{2}(1.27 \times 10^{-2}) = 1.8 \times 10^{-2}$m. Substituting in equation G.13:

$$N_f = \frac{1}{2}\left[\frac{(1.8 \times 10^{-2})|5.2 \times 10^{-6} - 7.3 \times 10^{-6}|(55)}{(1.5 \times 10^{-4})(1.1)}\right]^{1/-0.49}$$

$= 3765$ cycles

4.5.3.4 Evaluation

The results from the application examples given in paragraph 4.5.3.3 are summarized following:

FAILURE MECHANISM	MICROCIRCUIT CONFIGURATION*	N_f (cycles)
Die Brittle Cracking	RMC	Note 1
	RMC except: Au-Si eutectic die attach : L = 1 x 10^{-2} (400 mils)	Note 2
Die Fatigue Cracking	RMC	3.6 x 10^{11}
	RMC except: Au-Si eutectic die attach : L = 1 x 10^{-2}m(400mils)	2.5 x 10^{5}
	RMC except: Au-Si eutectic die attach : L = 1 x 10^{-2}m(400 mils) : MIL-STD-883, Class S	5.2 x 10^{5}
Die Attach Fatigue	RMC	8.8 x 10^{3}
	RMC except: Au-Si eutectic die attach	19
Substrate Attach Fatigue	Case: Cu; Substrate: Al_2O_3 Substrate Attach: Au-Si eutectic Substrate size: 1.91 x 10^{-2}m square (.75 in square)	will not survive first cycle
	Same except 70-30 In-Pb solder attach	74
	Same except Kovar case	will not surive first cycle
	Same except Kovar case, 70-30 In-Pb solder attach	1646
	Same except Kovar case, 70-30 In-Pb solder attach, substrate 1.3 x 10^{-2}m square substrate (0.5 in square)	3765

*RMC is defined in paragraph 4.5.6

Note 1. Die brittle cracking will not occur.
2. Die brittle cracking during first thermal cycle will occur.

From the summary table it is clear that the microcircuit designer's choice of materials, fabrication processes and geometry strongly influence the presence and severity of the failure mechanisms considered in this section.

Die brittle cracking is not normally seen in typical microcircuits. However, it could become a frequently occurring problem if the trend to larger die sizes is accompanied by the use of thin layer eutectic attach materials. Thick layer attach materials are preferable for larger die sizes.

Die fatigue cracking is rarely experienced in most current production microcircuits. However, mean cycle life can be reduced by 6 or more orders of magnitude if the trend to larger die sizes is accompanied by the use of thin layer eutectic atach materials. It is noted that upgrading the quality level from MIL-STD-883, Class B to Class S has negligible effect on life cycle improvement.

Die attach fatigue is frequently seen in power microcircuits and hybrids, and will become of greater prevalence if thin layer eutectic attach materials are employed. This failure mechanism frequency can be reduced by using thick layer low modulus of elasticity attach materials.

Substrate attach fatigue is found only in hybrid or multi-chip microcircuits where microcircuit components are mounted on substrates. The summary table deomonstrates the extreme importance of evaluation of package materials and substrate attach materials to optimize mean cycles to failure. Additionally, this mechanism can be further reduced by the strategy of using several smaller substrates in lieu of a single large substrate.

4.5.4 Failure Models of Metallization and Wire Bond Corrosion

4.5.4.1 Description of Models

The time to failure of a microelectronic package due to corrosion is dependent upon the package type, corroding material, and environmental conditions. The

package type is defined in terms of package geometry, encapsulating materials and lid and lead seals. These attributes together with the environmental conditions (relative humidity and temperature) determine the rate of moisture ingress, hermeticity and the moisture induction time for the package. The properties of the corroding material, contaminant and condensed moisture will control the rate of the corrosion process. For example, corrosion is less likely to occur in a cool, dry environment while a hot and humid environment will shorten the induction time and promote the galvanic transfer of ions for the corrosion process.

As the temperature increases, the rate of moisture ingress increases which leads to a shorter induction time. However, if the microelectronic device is electrically activated such that the temperature surrounding a potential corroding material is high enough to prevent moisture condensation, then corrosion will not occur. Thus the non-operating environment of the package is more severe than the operating environment for the corrosion failure mechanism.

The induction time between hermetic and non-hermetic packages can differ by four orders of magnitude. However, with new encapsulating package materials, such differences are being minimized and permeation is playing a smaller role on moisture ingression as compared to moisture flow.

Corrosion of metallization and bonding materials occurs predominantly on aluminum subjected to a chlorine or other halogen ionic contaminant. However, as the component dimensions are miniaturized and the current densities are increased, even gold will corrode provided there is an electrolyte for galvanic transfer. Furthermore a high quality and contaminant-free passivation layer can extend the time to failure by as much as 4 orders of magnitude compared to an unprotected counterpart.

The development of the model for corrosion induced failure is more fully discussed in Appendix H.

4.5.4.2 Metallization and Wire Bond Corrosion Failure Models

As discussed in 4.5.4.1, models have been developed for conductor metallization and bond pad corrosion failure. The total time to corrosion failure is the sum of two terms as defined by equation (H2.1):

$$\tau = \tau_1 + \tau_2 \qquad \text{(H2.1)}$$

where

τ is the time to corrosion failure.

τ_1 is the induction time necessary for the internal package volume to reach the threshold moisture content to support the corrosion process.

τ_2 is the time required for the corrosion process to terminate in failure.

In Appendix H it is shown that $\tau_2 >> t_1$. Therefore, the total time to corrosion failure can be effectively approximated by equation (H2.1a), as follows:

$$\tau = \tau_2 \qquad \text{(H2.1a)}$$

It is useful to evaluate t_1 to compare the effect of varying package leak rates for hermetically sealed packages, or to compare the effectiveness of alternate encapsulation materials for a non-hermetic package. Figure 4.5-2 delineates τ_1 for hermetic packages as a function of the package volume and the allowable leak rate of the package from MIL-STD-883. The induction time for a non-hermetic package is defined by equation (H2.2) as follows:

$$\tau_1(\text{non-hermetic}) = \frac{12L^2}{w^2 D} \qquad \text{(H2.2)}$$

where:

L is the effective thickness of the package barrier between the microcircuit and the external ambient, cm, which may be approximated by one-half of the overall package thickness.

D is the permeability of the encapsulant material, cm^3-cm/cm^2-sec-bar (i.e. cubic centimeter volume of permeant at standard temperature and pressure per square centimeter of barrier area per second bar differential pressure across the barrier per centimeter of barrier thickness).

The two principal sites for corrosion failure are discussed below.

(1) Conductor Metallization Corrosion Failure

The model for the time required for conductor metallization failure is defined by equation (H3.8).

$$\tau_{2m} = 8 \times 10^{11} \frac{k_1 k_2 k_3}{k_4} \frac{w^2 h n d \rho}{MV} \quad \text{(sec)} \qquad \text{(H3.8)}$$

where:

τ_{2m} is the time to failure for conductor metallization, seconds.

k_1 is the physical properties index of the conductor material obtained from Table 4.5-12.

k_2 is the coating integrity factor obtained from Table 4.5-13.

k_3 is the equipment operating time factor obtained from Table 4.5-14.

k_4 is the temperature-humidity environment acceleration factor obtained from figure 4.5-1.

w is the width of the conductor metallization, cm.

h is the height of the conductor metallization, cm.

n is the chemical valence of the conductor material obtained from Table 4.5-12.

d is the density of the conductor material obtained from Table 4.5-12.

M is the atomic weight of the conductor material obtained from Table 4.5-12

V is the applied or galvanic electrical bias, volts, chosen as described in Table 4.5-16.

ρ is the resistivity of the electrolyte, ohm-cm, Table 4.5-15.

(2) Bond Pad Corrosion Failure

The model for the time required for bond pad metallization failure is defined by equation (H3.10) as follows:

$$\tau_{2w} = 8 \times 10^{11} \frac{k_1 k_2 k_3}{k_4} \frac{V_C n d \rho}{MV} \qquad \text{(H3.10)}$$

where:

τ_{2w} is the time to failure for conductor metallization, seconds.

k_1 is the physical properties index of the bond pad material obtained from Table 4.5-12.

k_2 is the coating integrity factor obtained from Table 4.5-13, which for an uncoated bond pad is equal to unity.

k_3 is the equipment operating time factor obtained from Table 4.5-14.

k_4 is the temperature-humidity environment acceleration factor obtained from Figure 4.5-1.

V_C is the bond pad volume, cm^3, obtained from Table 4.5-11.

n is the chemical valence of the anodic member of the bond pad/bond wire combination, obtained from Table 4.5-16 and 4.5-12.

d is the density of the anodic member of the bond pad/bond wire combination, obtained from Tables 4.5-16 and 4.5-12.

M is the atomic weight of the anodic member of the bond pad/bond wire combination, obtained from Tables 4.5-16 and 4.5-12.

V is the applied or galvanic electrical bias, volts, chosen as described in Table 4.5-16.

ρ is the resistivity of the electrolyte, ohm-cm, obtained from Table 4.5-15.

4.5.4.3 Application Examples for Conductor and Bond Pad Metallization Corrosion Failure Models

(1) Conductor Metallization Corrosion

(A) Assume a microcircuit with a Representative Microcircuit Configuration

(RMC) as defined in 4.5.6 and used in a MIL-HDBK-217 ground-fixed (G_F) application environment in which the equipment is operated an average of three hours per day. Then the mean time to failure due to conductor metallization corrosion is found from equation H3.8:

$$\tau_{2m} = 8 \times 10^{11} \frac{k_1 k_2 k_3}{k_4} \frac{w^2 h n d \rho}{MV} \qquad \text{(H3.8)}$$

The variables in this equation are defined in paragraph 4.5.4.2(1) and data are obtained from the following sources:

VARIABLE	VALUE	UNITS	SOURCE
k1	0.1	N/A	Table 4.5-12
k2	10	N/A	Table 4.5-13
k3	1.14	N/A	Table 4.5-14
k4	0.34	N/A	Figure 4.5-1
w	1.5×10^{-4}	cm	RMC
h	7.5×10^{-5}	cm	RMC
n	3	N/A	Table 4.5-12
d	2.7	gm/cc	Table 4.5-12
ρ	7.3×10^{6}	ohm-cm	Table 4.5-15
M	27	amu	Table 4.5-12
V	5	volts	RMC

Substituting equation H3.8:

$$\tau_{2m} = (8 \times 10^{11}) \frac{(0.1)(10)(1.14)}{(0.34)} \frac{(1.5 \times 10^{-4})^2 (7.5 \times 10^{-5})(3)(2.7)(7.3 \times 10^{6})}{(27)(5)}$$

$$= 1.983 \times 10^{6} \text{ seconds} = 551 \text{ hours}$$

(B) Assume the same conditions as paragraph 4.5.4.3(1)(A) except the conductor metallization is gold. Then from Table 4.5-12, $K_1 = 1.0$, M = 197, d = 19.32, n = 3 and all other variables remain the same. Substituting in equation H3.8:

$$\tau_{2m} = (8 \times 10^{11})\frac{(1.0)(10)(1.14)}{(0.34)}\ \frac{(1.5 \times 10^{-4})^2(7.5 \times 10^{-5})(3)(19.32)(7.3 \times 10^{6})}{(197)(5)}$$

$= 1.944 \times 10^{7}$ seconds = 5400 hours

(C) Assume the same conditions as in paragraph 4.5.4.3(1)(A) except the conductor metallization line width is 5×10^{-5}m (0.5 microns). The $w = 5 \times 10^{-5}$m and all other variables remain the same. Substituting in equation H3.8:

$$\tau_{2m} = (8 \times 10^{11})\frac{(0.1)(10)(1.14)}{(0.34)}\ \frac{(5 \times 10^{-5})^2(7.5 \times 10^{-5})(3)(2.7)(7.3 \times 10^{6})}{(27)(5)}$$

$= 2.203 \times 10^{5}$ seconds $\approx$ 61 hours

(D) Assume the same conditions as in paragraph 4.5.4.3(1)(A) except the microcircuit will be used in an environment with a significantly higher chlorine content than normal. Then from Table 4.5-15, $\rho = 2.3 \times 10^{6}$ ohm-cm and all other variables remain the same. Substituting in equation H3.8:

$$\tau_{2m} = (8 \times 10^{11})\frac{(0.1)(10)(1.14)}{(0.34)}\ \frac{(5 \times 10^{-4})^2(7.5 \times 10^{-5})(3)(2.7)(2.3 \times 10^{6})}{(27)(5)}$$

$= 6.246 \times 10^{5}$ seconds = 174 hours

(E) Assume the same conditions as in paragraph 4.5.4.3(1)(A) except the signal power supply voltage is 1.5 volts and all other variables remain the same. Substituting in equation H3.8:

$$\tau_{2m} = (8 \times 10^{11})\frac{(0.1)(10)(1.14)}{(0.34)}\ \frac{(1.5 \times 10^{-4})^2(7.5 \times 10^{-5})(3)(2.7)(7.3 \times 10^{6})}{(27)(1.5)}$$

$= 6.609 \times 10^{6}$ seconds = 1836 hours

(F) Assume the same conditions as paragraph 4.5.4.3(1)(A) except the microcircuit metallization has been covered by a protective coating that has been demonstrated to provide a strong chemcical bond to the metallization that is inherently free from cohesive or bulk defects and is not detrimentally affected by a G_F environment e.g. silicon gel or equivalent. Then from Table 4.5-13, $K_2 = 100$ and all other variables remain the same. Substituting in equation H3.8:

$$\tau_{2m} = (8 \times 10^{11}) \frac{(0.1)(100)(1.14)}{(0.34)} \frac{(1.5 \times 10^{-4})^2 (7.5 \times 10^{-5})(3)(2.7)(7.3 \times 10^{6})}{(27)(5)}$$

$$= 1.983 \times 10^{7} \text{ seconds} = 5507 \text{ hours}$$

(G) Assume the same conditions as paragraph 4.5.4.3(1)(A) except the equipment is operated an average of 16 hours per day. Then from Table 4.5-14, $K_3 = 3$ and all other variables remain the same. Substituting in equation H3.8:

$$\tau_{2m} = (8 \times 10^{11}) \frac{(0.1)(10)(3)}{(0.34)} \frac{(1.5 \times 10^{-4})^2 (7.5 \times 10^{-5})(3)(2.7)(7.3 \times 10^{6})}{(27)(5)}$$

$$= 5.217 \times 10^{6} \text{ seconds} = 1449 \text{ hours}$$

(2) Bond Pad Corrosion

(A) Assume the same conditions as paragraph 4.5.4.3(1)(A). Then the mean time to failure due to bond pad corrosion is found from equation H3.10:

$$\tau_{2w} = 8 \times 10^{11} \frac{k_1 k_2 k_3}{k_4} \frac{C^V n d \rho}{MV} \qquad \text{(H3.10)}$$

The variables in this equation are defined in paragraph 4.5.4.2(2) and the data values and data sources for this equation are the same as tabulated in paragraph 4.5.4.3(1)(A), except V_C is obtained from Table 4.5-11. For the assumed conditions V_C is defined as the least value of equations H.8a and H.8b:

$$V_c = 0.3 \, s^2 \, t_b \qquad \text{(H.8a)}$$

$$V_c = 0.236 \, D_3 \qquad \text{(H.8b)}$$

The variables in these equations are defined in Table 4.5-11. From the RMC definition in paragraph 4.5.6 the following values are obtained:

VARIABLE	VALUE	UNITS	SOURCE
D	3.2×10^{-3}	cm	RMC
S	1×10^{-2}	cm	RMC
t_b	7.5×10^{-5}	cm	RMC

Substituting in equations H.8a and H.8b and choosing the least value:

$$V_C = 2.25 \times 10^{-9} \text{ cm}^3$$

Substituting in equation H3.10:

$$\tau_{2w} = (8 \times 10^{11}) \frac{(0.1)(10)(1.14)}{(0.34)} \frac{(2.25 \times 10^{-9})(3)(2.7)(7.3 \times 10^{6})}{(27)(5)}$$

$$= 2.643 \times 10^{9} \text{ seconds} = 7.343 \times 10^{5} \text{ hours}$$

(B) Assume the same conditions as paragraph 4.5.4.3(1)(A) except the bond wire material is gold. Since the bond wire and bond pad are dissimilar metals, from Table 4.5-16, it is determined that the bond pad material (aluminum) is anodic to gold and that

$$V_{galvanic} = 1 + (V_{cathode} - V_{anode}) = 1 + (1.5 - (-1.66))$$
$$= 4.16 \text{ volts}$$

Since $V_{galvanic} < V = 5$ volts, the latter value is used in equation H3.10. From Table 4.5-11 it is determined that the corrosively attacked member is the bond pad and that equation H.8a defines the corrosion volume:

$$V_C = 0.3 \, s^2 \, t_b \qquad \text{(H.8a)}$$

The variables for this equation are defined in Table 4.5-11 and the variable values are determined from the RMC definition in paragraph 4.5.6. The values tabulated in paragraph 4.5.4.3(2)(A) apply. Substituting these values in equation H.8a:

$$V_C = (0.3)(1 \times 10^{-2})^2(7.5 \times 10^{-5}) = 2.25 \times 10^{-9} \text{ cm}^3$$

Since the corrosively attacked member is the bond pad all the applicable variable values tabulated in paragraph 4.5.4.3(1)(A) apply to this condition. Substituting these values in equation H3.10:

$$\tau_{2w} = (8 \times 10^{11}) \frac{(0.1)(10)(1.14)}{(0.34)} \frac{(2.25 \times 10^{-9})(3)(2.7)(7.3 \times 10^{6})}{(27)(5)}$$

$$= 2.643 \times 10^{9} \text{ seconds} = 7.343 \times 10^{5} \text{ hours}$$

(C) Assume the same conditions as paragraph 4.5.4.3(1)(A) except the bond pad is gold and the bond wires are attached with wedge bonds. Since the bond wire and bond pad are dissimilar metals, from Table 4.5-16, it is determined that the bond pad material is cathodic to the bond wire material (aluminum) and that

$$V_{galvanic} = 1 + V_{cathode} - V_{anode} = 1 + 1.5 - (-1.66)$$
$$= 4.16 \text{ volts}$$

Since $V_{galvanic} < V = 5$ volts, the latter value is used in equation H3.10. From Table 4.5-11 it is determined that the corrosively attacked member is the bond wire and for wedge bonds equation H.8b defines the corrosion volume:

$$V_C = 0.236\ D^3 \qquad \text{(H.8b)}$$

The variable for this equation is defined in Table 4.5-11. From the RMC definition in paragraph 4.5.6 the value $D = 3.2 \times 10^{-3}$ cm is obtained. Substituting in equation H.8b:

$$V_C = (0.236)(3.2 \times 10^{-3})^3 = 7.733 \times 10^{-9} \text{ cm}^3$$

Since the corrosively attacked member is the bond wire, all the applicable variable values tabulated in paragraph 4.5.4.3(1)(A) apply to this condition. Substituting these values in equation H3.10:

$$\tau_{2w} = (8 \times 10^{11}) \frac{(0.1)(10)(1.14)}{(0.34)} \frac{(7.733 \times 10^{-9})(3)(2.7)(7.3 \times 10^{6})}{(27)(5)}$$

$$= 9.085 \times 10^{9} \text{ seconds} = 2.524 \times 10^{6} \text{ hours}$$

4.5.4.4 Evaluation

The results from the application examples given in paragraph 4.5.4.3 are summarized following:

FAILURE MECHANISM	MICROCIRCUIT CONFIGURATION*	N_f (hours)
Conductor Metallization Corrosion	RMC: operating 3 hrs/day	551
	RMC except: Au conductors - operating 3 hrs/day	5400
	RMC except: 0.5 micron line width - operating 3 hrs/day	61
	RMC - operating in corrosive environment - operating 3 hrs/day	174
	RMC except: 1.5v power supply - operating 3 hrs/day	1836
	RMC - exceptional conductor protective coating - operating 3 hrs/day	5507
	RMC - operating 16 hrs/day	1449
Bond Pad Corrosion	RMC - operating 3 hrs/day	7.3×10^5
	RMC except: Au bond pad - operating 3 hrs/day	7.3×10^5
	RMC except: Au bond pad : wedge bonds - operating 3 hrs/day	2.5×10^6

* RMC is defined in paragraph 4.5.6

Comparison of the mean time to failure for the two corrosion sites described in the summary table clearly demonstrates that conductor metallization corrosion is predicted to be much more prevalent than bond pad corrosion.

The conductor metallization corrosion mechanism can cause three or more orders of magnitude variation in mean time to failure, dependent on design, materials, fabrication processes and operating conditions. Significant improvement in microcircuit resistance to this failure mechanism can be achieved by two steps, either separately or in combination viz3.

- develop improved conductor protective coatings (passivation)(order magnitude increase)

- use of more corrosion resistant conductor metals (order of magnitude increase)

The trend to higher density microcircuits has contradictory effects on conductor metallization corrowion. On one hand narrower conductor widths can reduce mean time to failure by an order of magnitude. On the other hand the lower signal voltage levels can increase mean time to failure by a factor up to three. This suggests that the overall effect of higher density microcircuits will be an increasing susceptability to the corrosion mechanism. Thus it is emphasized that it will become increasingly important to implement the reliability improvement steps highlighted above.

Finally, it is observed that increasing equipment operating time per day will increase the mean time to failure from corrosion mechanisms. Continuously operating equipment will not experience corrosion failure. Not only do the models predict this result, but it is in agreement with experience. Corrosion is an electrochemical process and liquid phase moisture is a necessary condition for the process to occur. Under the thermal conditions of equipment operation only vapor phase moisture is present within microcircuit enclosures.

4.5.5 Differential Temperature for Use in Failure Models

Transient differential temperature at the failure site is the principal source of stress that drives the failure mechanisms discussed in paragraphs 4.5.2 and 4.5.3. The models developed for these mechanisms utilize the differential temperature raised to a power. Hence, the model predictions are sensitive to the differential temperature value employed. Development of realistic delta temperature values for use in the models is discussed in Appendix I.

4.5.6 Representative Microcircuit Configuration (RMC)

The objective for the failure mechanism models developed in this report was to obtain "easy to use" models with variables that are reasonable and accessible for use by reliability analysts and that accurately predict the time or number of cycles to failure. This dual objective is self-contradictory in that accuracy requires inclusion of all variables with significant effect on the failure mechanisms and simplicity requires minimization of variables. Our solution to this dilemma is two-fold:

(1) Develop models in accordance with the applicable laws of physics, chemistry and engineering that fully and accurately relate all significant variables to their effect on component life.

(2) Simplify the models for use by reliability analysts using the concept of a Representative Microcircuit Configuration (RMC), as further described.

When mature technology microcircuits are produced to established performance and package standards by numerous manufacturers, competitive pressures ensure that a high degree of similarity will exist between parts of equivalent performance housed in interchangeable packages. Hence, many of the failure mechanism variables will be approximately equal for all MIL-M-38510 microcircuits. Production efficiency requirements will ensure repetitive usage of materials and certain geometric features throughout a complete technology product line. The RMC concept exploits this similarity.

Westinghouse experience in application, reliability characterization and

failure analysis of microcircuits and design and manufacturing of multichip hybrids, combined with discussions with the microcircuit suppliers[102,103] has resulted in the following definition of an RMC:

- PACKAGE : Hermetically sealed
  : Al_2O_3 Alumina ceramic base and lid
- DIE : Silicon
  : Diagonal length = 3.23×10^{-3}m (127 mils)
  : Thickness = 3.7×10^{-4}m (14.5 mils)
- DIE ATTACH : Mounted to package base
  : Ag-glass epoxy
  : After cure thickness = 5.1×10^{-5}m (2 mils)
- CONDUCTORS : Aluminum
  : Passivation coated
  : Width = 1.5×10^{-4}cm (1.5 microns)(0.06 mils))
  : Thickness = 7.5×10^{-5}cm (7500 Å)(0.03 mils)
- BOND PADS : Aluminum
  : Not passivation coated
  : Size = 1×10^{-2}cm x 1×10^{-2}cm (4 mils x 4 mils)
  : Thickness = 7.5×10^{-5}cm (7500 Å)(0.03 mils)
- BOND WIRE : Aluminum
  : Diameter = 3.2×10^{-2}mm (1.25 mils) = 3.2×10^{-3}cm
- APPLIED VOLTAGE : 5 Volts
- QUALITY LEVEL : MIL-STD-883, Level B
  : Allowable vertical edge crack length = 1.3×10^{-4}m (5 mils)
- AMBIENT : Temperature = 70°C
  : Humidity = 90% RH

4.5.7 Model Simplification

4.5.7.1 Failure Mechanism Models

The following non-electrical (package related) failure mechanism models have been developed in Section 4.5 of this report.

(1) Bond Wire Flexure Fatigue (Equations F5.7a and F5.8, Paragraph 4.5.2.2(1)).
(2) Shear Fatigue at Bond Pad/Substrate Interface (Equations F5.9 and F5.10, Paragraph 4.5.2.2(2)).
(3) Shear Fatigue at Bond Pad/Bond Wire Interface (Equations F5.10 and F5.14, Paragraph 4.5.2.2(3)).
(4) Die Brittle Cracking (Equations G.4, G.5 and G.6, Paragraph 4.5.3.2(1)).
(5) Die Fatigue Cracking (Equations G.5, G.6 and G.10e, Paragraph 4.5.3.2(2)).
(6) Die Attach Fatigue (Equations G.11 and G.12, Paragraph 4.5.3.2(3)).
(7) Substrate Attach Fatigue (Equation G.13, Paragraph 4.5.3.2(4)).
(8) Conductor Metallization Corrosion (Equations H2.1a and H3.8, Paragraph 4.5.4.2(1)).
(9) Bond Pad Corrosion (Equations H2.1a and H3.10, Paragraph 4.5.4.2(2)).

4.5.7.2 Failure Mechanisms Present in an RMC

Using the parenthetical numbers assigned to the failure mechanisms in paragraph 4.5.7.1, only the following mechanisms are potentially present in an RMC:

(1) Bond Wire Flexure Fatigue
(2) Shear Fatigue at Bond Pad/Substrate Interface
(4) Die Brittle Cracking
(5) Die Fatigue Cracking
(6) Die Attach Fatigue
(8) Conductor Metallization Corrosion
(9) Bond Pad Corrosion

The mechanisms which are not included in an RMC, and the reasons for their

omission, are discussed below.

(3) Shear Fatigue at Bond Pad/Bond Wire Interface

This mechanism is not present because the bond pad and bond wire are made from the same material, thus eliminating the cause of the mechanism (differential thermal expansion). Single-metal bonds have greater industry usage than do bi-metallic bonds, so the former is used in the RMC.

(7) Substrate Attach Fatigue

This mechanism is not present because the predominant practice in microcircuit construction is to directly attach the die to the package base. This mechanism can be of significance in hybrids, however.

4.5.7.3 Simplified Failure Mechanism Models for an RMC

The applicable fully delineated failure mechanism models defined in paragraphs 4.5.2, 4.5.3 and 4.5.4 have been simplified by the Representative Microcircuit Configuration (RMC) concept described in paragraph 4.5.6 and are presented below. The simplification applies only to the seven applicable models discussed in paragraph 4.5.7.2.

4.5.7.3.1 Bond Wire Flexure Fatigue

The fully delineated model for this mechanism is defined by equations F5.7a and F5.8 given in paragraph 4.5.2.2(1). Following is a list of the variables in this model for which numerical values are obtained from the sources noted, using the RMC concept:

VARIABLE	VALUE	UNITS	SOURCE
A_1	3.9232×10^{-10}	N/A	Table 4.5-4
n_1	-5.134	N/A	Table 4.5-4
r	1.6×10^{-2}	mm	RMC
α_w	23.2×10^{-6}	m/m/°c	Table 4.5-1
α_s	4.67×10^{-6}	m/m/°c	Table 4.5-2

Incorporating these values provided the following simplified model:

$$N_{f(flex)} = 5.6 \times 10^{7} \left[\frac{\cos^{-1} (9.66 - 1.79 \times 10^{-5} \Delta T)}{15} - 1 \right]^{-5.134} \qquad (4.5.1)$$

where

ΔT is the temperature difference encountered in the application, obtained from Table 4.5-17, or user supplied.

4.5.7.3.2 Shear Fatigue at Bond Pad/Substrate Interface

The fully delineated model for this mechanism is defined by equations F5.9 and F5.10 given in paragraph 4.5.2.2(2). Following is a list of the variables in this model for which numerical values are obtained from the sources noted, using the RMC concept:

VARIABLE	VALUE	UNITS	SOURCE
A_2	4.3386×10^{-11}	N/A	Table 4.5-5
n_2	-5.134	N/A	Table 4.5-5
K	1.46×10^{-5}	N/A	Table 4.5-6

Incorporating these values provides the following simplified model:

$$N_{f(shear)s} = 2.9078 \times 10^{14} \Delta T^{-5.134} \qquad (4.5.2)$$

where

ΔT is the temperature difference encountered in the application, obtained from Table 4.5-17, or user supplied.

4.5.7.3.3 Die Brittle Cracking

The fully delineated model for this mechanism is defined by equations G.4, G.5 and G.6 given in paragraph 4.5.3.2(1). Following is a list of the variables in this model for which numerical values are obtained from the sources noted, using the RMC concept:

VARIABLE	VALUE	UNITS	SOURCE
K_{Ic}	0.82	MPa $\sqrt{m}$	Table 4.5-7
α_s	7.3×10^{-6}	m/m/°c	Table 4.5-9
α_d	4.67×10^{-6}	m/m/°c	Table 4.5-7
E_s	255×10^{9}	Pa	Table 4.5-9
E_a	2.8×10^{9}	Pa	Table 4.5-8
X	5.1×10^{-5}	m	RMC
L	3.22×10^{-3}	m	RMC
a_i	1.3×10^{-4}	m	RMC

Incorporating these values provides the following simplified criterion for the presence of this failure mechanism:

$$a_c = \frac{17.2}{\Delta T^2} \leq a_i = 1.3 \times 10^{-4} \qquad (4.5.3)$$

where

ΔT is the temperature difference encountered in the application, obtained from Table 4.5-17, or user supplied.

The maximum value of ΔT obtainable from Table 4.5-17 is $\Delta T = 55°C$. Substituting this value in equation 4.5.3 yields the following:

$$a_c = \frac{17.2}{(55)^2} = 5.67 \times 10^{-5}m > a_i = 1.3 \times 10^{-4}m$$

Since a_c is two orders of magnitude greater than a_i, this failure mechanism will not occur in any MIL-HDBK-217 application environment defined in Table 4.5- 17 for the Representative Microcircuit Configuration presented in paragraph 4.5.6.

4.5.7.3.4 Die Fatigue Cracking

The fully delineated model for this mechanism is defined by equations G.5, G.6 and G.10e given in paragraph 4.5.3.2(2). Following is a list of the variables in this model for which numerical values are obtained from the sources noted, using the RMC concept:

VARIABLE	VALUE	UNITS	SOURCE
n	4	N/A	Table 4.5-7
A	1×10^{-12}	N/A	Table 4.5-7
a_i	1.3×10^{-4}	m	RMC
a_f	3.8×10^{-4}	m	Para. 4.5.3.2(2)
K_{Ic}	0.82	MPa$\sqrt{m}$	Table 4.5-7
α_s	7.3×10^{-6}	m/m/°c	Table 4.5-9
α_d	4.67×10^{-6}	m/m/°c	Table 4.5-7
E_s	255×10^{9}	Pa	Table 4.5-9
E_a	2.8×10^{9}	Pa	Table 4.5-8
X	5.1×10^{-5}	m	RMC
L	3.22×10^{-3}	m	RMC

Incorporating these values provides the following simplified model:

$$N_f = 3.3 \times 10^{18} / \Delta T^4 \qquad (4.5.4)$$

where

ΔT is the temperature difference encountered in the application, obtained from Table 4.5-17, or user supplied.

4.5.7.3.5 Die Attach Fatigue

The fully delineated model for this mechanism is defined by equations G.11 and G.12 given in paragraph 4.5.3.2(3). Following is a list of the variables in this model for which numerical values are obtained from the sources noted, using the RMC concept:

VARIABLE	VALUE	UNITS	SOURCE
α_s	7.3×10^{-6}	m/m/°c	Table 4.5-9
α_d	4.67×10^{-6}	m/m/°c	Table 4.5-7
X	5.1×10^{-5}	m	RMC
$\gamma'f$	1.1	N/A	Table 4.5-8
c	-0.49	N/A	Table 4.5-8
L	3.22×10^{-3}	m	RMC

Incorporating these values provides the following simplified model:

$$N_f = 3.217 \times 10^7 \, \Delta T^{-2.041} \qquad (4.5.5)$$

where

ΔT is the temperature difference encountered in the application, obtained from Table 4.5-17, or user supplied.

4.5.7.3.6 Conductor Metallization Corrosion

The fully delineated model for this mechanism is defined by equations H2.1a and H3.8 given in paragraph 4.5.4.2(1). Following is a list of the variables in this model for which numerical values are obtained from the sources noted, using the RMC concept:

VARIABLE	VALUE	UNITS	SOURCE
k_1	0.1	N/A	Table 4.5-12
k_2	10	N/A	Table 4.5-13
k_4	0.34	N/A	Figure 4.5-1
w	1.5×10^{-4}	cm	RMC
h	7.5×10^{-5}	cm	RMC
n	3	N/A	Table 4.5-12
d	2.7	gm/cc	Table 4.5-12
M	27	amu	Table 4.5-12
V	5	Volts	RMC
ρ	7.3×10^{6}	ohm-cm	Table 4.5-15

Incorporating these values provides the following simplified model:

$$\tau_{2m} = 1.7 \times 10^{6} K_3 \text{ seconds} \qquad (4.5.6)$$

or $$\tau_{2m} = 483 K_3 \text{ hours} \qquad (4.5.6a)$$

where

K_3 is the equipment operating time factor obtained from Table 4.5-14.

4.5.7.3.7 Bond Pad Corrosion

The fully delineated model for this mechanism is defined by equations H2.1a and H3.10 given in paragraph 4.5.4.2(2). Following is a list of the variables in this model for which numerical values are obtained from the sources noted, using the RMC concept:

VARIABLE	VALUE	UNITS	SOURCE
k_1	0.1	N/A	Table 4.5-12
k_2	10	N/A	Table 4.5-13
k_4	0.34	N/A	Figure 4.5-1
V_c	2.2×10^{-9}	cm^3	Table 4.5-11
n	3	N/A	Table 4.5-12
d	2.7	gm/cc	Table 4.5-12
M	27	amu	Table 4.5-12
V	5	Volts	RMC
ρ	7.3×10^6	ohm-cm	Table 4.5-15

Incorporating these values provides the following simplified model:

$$\tau_{2w} = 2.3 \times 10^9 K_3 \text{ seconds} \quad (4.5.7)$$

or $$\tau_{2w} = 6.3 \times 10^5 K_3 \text{ hours} \quad (4.5.7a)$$

where

K_3 is the equipment operating time factor obtained from Table 4.5-14.

4.5.7.4 Other Simplified Failure Mechanism Models

Two failure mechanisms are identified in paragraph 4.5.7.2 that are not present in an RMC, and hence would be expected to form a minor part of the total package-related failures experienced in military electronic equipment. These mechanisms can be simplified for evaluation purposes by assuming probable material combinations and construction practices that would cause the mechanisms to be activated. The two remaining mechanisms are discussed below.

4.5.7.4.1 Shear Fatigue at Bond Pad/Bond Wire Interface

The fully delineated model for this mechanism is defined by equations F5.10 and F5.14 given in paragraph 4.5.2.2(3). This mechanism can be activated in a microcircuit only when the bond pad and bond wire are made from dissimilar

materials. If these two elements are made from dissimilar materials, the most probable combination would be gold wire bonded to aluminum pads. Assuming the bond pad is on a silicon die and that this combination is chosen, following is a list of the variables in this model for which numerical values are obtained from the sources noted:

VARIABLE	VALUE	UNITS	SOURCE
A_2	4.2948×10^{-12}	N/A	Table 4.5-5
n_2	-4.9828	N/A	Table 4.5-5
α_w	14.2×10^{-6}	m/m/°c	Table 4.5-1
α_s	4.67×10^{-6}	m/m/°c	Table 4.5-2

Incorporating these values provides the following simplified model:

$$N_{f(shear)w} = 1.4 \times 10^{15} \Delta T^{-4.983} \qquad (4.5.8)$$

where

ΔT is the temperature difference encountered in the application, obtained from Table 4.5-17, or user supplied.

4.5.7.4.2 Substrate Attach Fatigue

The fully delineated model for this mechanism is defined by equations G.13 given in paragraph 4.5.3.2(4). This mechanism can be activated only when a substrate is inserted between a microcircuit die and the package base. Normally, this type of construction is employed in hybrid/multichip microcircuits. The substrate will usually be a base for conductor metallization to provide interconnections between passive and active leadless (chip) components. Hybrid circuits dissipating several watts of power are typically housed in hermetically sealed copper alloy packages with aluminum nitride substrates, employing 70 - 30 In - Pb solder for efficient heat transfer. Assuming this type of construction, following is a list of the

variables in this model for which numerical values are obtained from the sources noted:

VARIABLE	VALUE	UNITS	SOURCE
α_s	4.5×10^{-6}	m/m/°c	Table 4.5-9
α_c	16.9×10^{-6}	m/m/°c	Table 4.5-10
x_{sa}	1.5×10^{-4}	m	Assumed
γ_f	1.1	N/A	Table 4.5-8
c	-0.49	N/A	Table 4.5-8

Incorporating these values provides the following simplified model:

$$N_f = 98.4 \, (L_s \, \Delta T)^{-2.041} \qquad (4.5.9)$$

where

L_s is the diagonal length of the substrate, meters.

ΔT is the temperature difference encountered in the application, obtained from Table 4.5-17, or user supplied.

4.5.8 Relationship Between Cycles and Time

The reliability analyst requires knowledge of the time to failure for the various failure mechanisms that may be present in an electronic component being analyzed. However, seven of the nine models developed in this report for package related failure mechanisms are a function of temperature change magnitude and can only predict the number of stress/strain cycles to fatigue or cracking failure. The duration of the temperature change cycles has negligible effect on these mechanisms, as discussed in Appendix I.

Temperature change cycles are caused by the following conditions:

(1) Air transportation in non-temperature controlled cargo compartments while the equipment is not operating.

(2) Climatic diurnal temperature variations when the equipment is not operating.
(3) Temperature increase above ambient due to internal heat dissipation during equipment operation.

The first condition is infrequently encountered and the second is of negligible temperature magnitude, as discussed in Appendix I and delineated in Table I-5. Hence, the third condition is the principal source of temperature variation.

In the context of this report an equipment operating cycle is defined to be the time elapsed between equipment turn-on and turn-off. Some types of equipment have varying power levels during an operating cycle while other types have a constant power level. The operating power level directly affects the temperature change magnitude at each component.

Equipment operating cycles vary from nearly continuous for certain types of equipment to short intermittent periods for other types. Hence, accurate determination of mean time to failure for these mechanisms depends upon accurate determination of operating cycle duration for the type of equipment being analyzed.

Little published data exists on the relationship between operating cycle duration and equipment type. Accumulation and analysis of such data are beyond the scope of this report. Time and temperature analysis of specified equipment mission profiles are the best source of data for operating temperature cycle magnitude and duration.

Appendix I, Table I-1, records the results of measured temperature variation during a flight mission for an unidentified airborne electronic equipment. This data suggests that the major temperature variations recorded had an average duration of 1.1 hours per cycle. When more accurate information is not available, it is conservative to assume a short thermal cycle duration. Based on this data the following relationship between temperature cycles and

time is tentatively offered:

$$T_f = 1.25N_f \qquad (4.5.10)$$

where

T_f is the mean time to failure, hours

N_f is the mean number of cycles to failure obtained from equations 4.5.1, 4.5.2, 4.5.4, 4.5.5 and 4.5.8 through 4.5.9 (or the fully delineated equations from which these are derived).

4.5.9 Failure Mechanism Model Assessment

Operational use of electronic equipment subjects the microcircuits employed therein to various levels of electrical, mechanical, thermal, chemical and environmental stresses. These stresses activate latent failure mechanisms that have not been removed by microcircuit quality control inspections, tests and screens. Many of these mechanisms are wearout type which cause the microcircuit probability to increase with time. In general the probability increase rate is different for each mechanism. Hence, meany mechanisms are simultaneously competing to cause device failure. Evaluation of the mean time to failure for each competing mechanism permits ranking to identify the most probable mechanisms.

The nine package related failure mechanisms modeled in this report are ranked following, based on the following assumptions:

(1) The microcircuits conform to the Representative Microcircuit Configuration (RMC) defined in paragraph 4.5.6.

(2) The relationship between the mean number of cycles to failure and the mean time to failure conforms to equation 4.5.11.

(3) The two mechanisms not present in an RMC conform to the probable configuration discussed in paragraph 4.5.7.4.

(4) The microcircuits are used in an equipment used in an application environment, as delineated in Table 4.5-17, for which a maximum ΔT

is expected, i.e. either A_U, G_B or N_U, for which $\Delta T = 55°C$ is expected.

(5) While substrates are not utilized in an RMC, for ranking purposes, a substrate size of 2.5×10^{-2}m square (1 inch square) attached with 70 - 30 In - Pb solder with an attach thickness of 1.5×10^{-4}m (6 mils) is assumed.

Tabulated following are these nine mechanisms listed in order of increasing mean time to failure:

FAILURE MECHANISM	T_f MEAN TIME TO FAILURE HOURS	YEARS
(1) Substrate Attach Fatigue	30	-
(2) Conductor Metallization Corrosion	724	-
(3) Die Attach Fatigue	1.1×10^4	1.25
(4) Bond Pad/Die Interface Shear Fatigue	4.2×10^5	48
(5) Bond Pad/Wire Corrosion	9.4×10^5	107
(6) Bond Pad/Bond Wire Interface Shear Fatigue	3.0×10^6	433
(7) Die Fatigue Cracking	4.5×10^{11}	5.1×10^7
(8) Bond Wire Flexure Fatigue	2.9×10^{17}	3.4×10^{13}
(9) Die Brittle Cracking	∞	-

4.5.9.1 Discussion

The package related failure mechanism models contain material dependent coefficients and exponents. The values utilized in these models are based upon available data for materials similar to those used in microcircuit construction, due to the unavailability of data for the actual materials. Hence, it is emphasized that the mean time to failure values predicted above are useful only for ranking the mechanisms relative to each other. When data on the actual materials of construction are available, the models will be capable of estimating the mean time to failure for microcircuits used in various application environments.

Table 4.5-1

Wire Properties

Wire Material	α_w m/m/c	E P_a
Aluminum	23.2×10^{-6}	69×10^9
Copper	17.6×10^{-6}	118×10^9
Gold	14.2×10^{-6}	Up to 82×10^9
Palladium	11.7×10^{-6}	124×10^9

Table 4.5-2

Bond Pad Substrate Properties

Bond Pad Substrate Material	α_s m/m/c
Gallium Arsenide	5.73×10^{-6}
Silicon	4.67×10^{-6}

Table 4.5-3

Encapsulant Properties

ENCAPSULANT	α_e m/m/c
Epoxy	
Rigid, Unfilled	55×10^{-6}
Rigid, Filled	30×10^{-6}
Flexible, Unfilled	100×10^{-6}
Flexible, Filled	70×10^{-6}
Polyester	
Rigid, Unfilled	75×10^{-6}
Flexible, Unfilled	130×10^{-6}
Silicone	
Flexible, Unfilled	400×10^{-6}
Urethane	
Flexible, Unfilled	150×10^{-6}

Table 4.5-4

Constants for Fatigue Stress in Bending and Axial Loading

MATERIAL	A_i^*	n_i^*
Aluminum	3.9323×10^{-10}	-5.134
Copper	1.0133×10^{-21}	-9.1169
Gold	3.5844×10^{-11}	-4.9828

* Values are engineering estimates

Table 4.5-5

Constants for Fatigue Stress in Shear

MATERIAL	A_2^*	n_2^*
Aluminum	4.3386×10^{-11}	-5.134
Copper	1.9897×10^{-23}	-9.1169
Gold	4.2948×10^{-12}	-4.9828

* Values are engineering estimates

Table 4.5-6

Bond Pad-Substrate Shear Constant

BONDPAD MATERIAL	K	
	SUBSTRATE MATERIAL	
	S_i	GaAs
Aluminum	$1.46 \times 10^{-5*}$	$1.56 \times 10^{-5*}$
Gold	$0.90 \times 10^{-5*}$	$1.02 \times 10^{-5*}$

* Values are engineering estimates

Table 4.5-7

Die properties

DIE MATERIAL	E Pa	α m/m/c	K_{Ic} MP$\sqrt{m}$	A	n
Silicon	128×10^9	4.67×10^{-6}	0.82	$*10^{-12}$	*4
Gallium Arsenide	89×10^9	5.73×10^{-6}	0.31	$*10^{-12}$	*4

* Values are engineering estimates

Table 4.5-8

Die attach properties

Die Attach Material	Percentage of different constituents	T_g or melting temperature °C	E_a Pa	Y'f	c
Eutectic	Au-3% Si	280	59.2×10^9	*1.1	*-.49
	Au-12% Ge	363	83.0×10^9	*1.1	*-.49
	Au-40% Ge	356	69.3×10^9	*1.1	*-.49
Solder	In-70% Pb -30%	175	$*11.7 \times 10^9$	*1.1	*-.49
	Sn-40% Pb -60%	*100	$*3.8 \times 10^9$	*1.1	*-.49
	Sn-5% Pb -95%	*170	3.8×10^9	*0.18	*-.13
	Sn-10% Pb -90%	200	3.8×10^9	*1.1	*-.49
Epoxy - Conductive	---	155	4.1×10^9	*1.1	*-.49
Non Conductive	---	155	2.8×10^9	*1.1	*-.49
Polyimide	---	275	4.5×10^{-9}	*1.1	*-.49

* Values are engineering estimates

Table 4.5-9

Substrate properties

Type of substrate Material	α_s m/m/c	E_s P_a
Silicon	4.67×10^{-6}	164×10^9
Alumina	7.3×10^{-6}	255×10^9
Copper	16.9×10^{-6}	118×10^9
Beryllium Oxide	8.3×10^{-6}	265×10^9
Aluminum Nitride	4.5×10^{-6}	2.75×10^9
Silicon Carbide	3.7×10^{-6}	$>331 \times 10^9$

Table 4.5-10

Package Case properties

Package Material	α_c m/m/c
Kovar	5.2×10^{-6}
Copper	16.9×10^{-6}
Aluminum	23.0×10^{-6}

Table 4.5-11

BOND PAD CORROSION VOLUME

GALVANIC RELATIONSHIP OF BOND PAD MATERIAL TO BOND WIRE MATERIAL (FROM TABLE 4.5-16)	BOND TYPE	CORROSION VOLUME V_c cm^3	Equation Number	CORROSIVELY ATTACKED MEMBER
ANODIC	ALL	$V_c = 0.3s^2\ t_b$	H.8a	BOND PAD
CATHODIC	WEDGE OR CRESCENT	$V_c = 0.236\ D^3$	H.8b	BOND WIRE
	BALL	$V_c = 3.77\ D^3$	H.8c	
	UNKNOWN	$V_c = 0.236\ D^3$	H.8b	
NONE (ie. same material for pad and wire)	ALL	LEAST VALUE OF $V_c = 0.3s^2\ t_b$ and $V_c = 0.236\ D^3$	H.8a H.8b	MEMBER WITH LEAST V_c

NOTE: D = Bond wire diameter, cm
s = Bond pad size, cm (for a square pad)
t_b = Bond pad thickness, cm

Table 4.5-12

Corrosion Properties of Metals

Material	Physical Property Index (k_1)	Atomic Weight (M)	Density (d) gm/cc	Chemical Valence (n)
Aluminum	0.1	27	2.7	3
Copper	0.5	64	8.93	2
Gold	1.0	197	19.32	3

Table 4.5-13

Coating Integrity Index

COATING TYPE	COATING INTEGRITY INDEX (k_2)
No Coating	1
Partially Bonded	10 - 50 (NOTE 1)
Completely Bonded	100

NOTE 1: When a metallization passivation layer is present and the defect level is unknown, use $K_2 = 10$.

Table 4.5-14

Equipment Operating Time Factor

Number of Operating Hours Per Day	K_3
1	1.04
2	1.09
3	1.14
4	1.20
5	1.26
6	1.33
7	1.41
8	1.50
9	1.60
10	1.71
11	1.85
12	2.00
13	2.18
14	2.40
15	2.67
16	3.00
17	3.43
18	4.00
19	4.80
20	6.00
21	8.00
22	12.00
23	24.00
24	Infinity

Table 4.5-15

Electrolyte Resistivity

ENVIRONMENT	ρ (ohm/cm)
Normal	7.3×10^6
Corrosive	2.3×10^6

NOTE: Assume a normal environment unless there is compelling reason to assume a corrosive environment.

Table 4.5-16

Galvanic Electrochemical Potential

Material	Standard Electrode Potential, Volts
Gold	1.5 More Cathodic
Palladium	0.95
Silver	0.8
Copper	0.34
Chromium	-0.74
Aluminum	-1.66 More Anodic

NOTE: The electrical bias voltage shall be chosen as follows:

(1) For dissimilar bond wire/bond pad metals use the larger of the applied signal or power supply voltage or the galvanic potential determined from the Table as follows:

$$V_{galvanic} = 1 + (V_{cathode} - V_{anode})$$

(2) For similar metals use the applied signal or power supply voltage.

Table 4.5-17

Recommended Value for Component Operating ΔT (See Note 1)

USAGE ENVIRONMENT CLASSIFICATION		ΔT
MIL-HDBK-217E	PROPOSED	°C
A_{IA} A_{IB} A_{IC} A_{IF} A_{IT} A_{RW}	A_I	30
A_{UA} A_{UB} A_{UC} A_{UF} A_{UT}	A_U	55
C_L	C_L	NOTE 2
G_B G_{MS}	G_B	30
G_F	G_F	55
G_M M_P	G_M	NOTE 3
M_{FA} M_{FF} M_L	M_F	NOTE 2
N_H N_S N_{SB}	N_I	50
N_U	N_U	55
U_{SL}	N_{UL}	NOTE 2
N_{UU}	N_{UU}	35
S_F	S_F	35

NOTE 1. Table 4.5-17 ΔT values are for use when thermal analysis or test data are not available.

2. Application environments referring to this note are of short duration and have negligible effects on the package (non-electrical) related failure mechanisms, for which the pre-launch storage conditions will have the dominant effect. Use ΔT = 5°C for storage under controlled storage conditions and ΔT = 20°C for uncontrolled storage conditions.

3. Use G_B application environment for equipment mounted in temperature controlled compartments and G_F for uncontrolled compartments.

Table 4.5-18

Typical Values for Die/Substrate Attach Thickness

ATTACH MATERIAL	TYPICAL THICKNESS	
	METERS	MILS
Au - Si Eutectic	2.5×10^{-6}	0.1
Au - Ge Eutectic	2.5×10^{-6}	0.1
Au - Ge Solder	7.6×10^{-5}	3
Sn 62 Solder	7.6×10^{-5}	3
80 - 20 Au - Sn Solder	7.6×10^{-5}	3
Dielectric Epoxy (Die)	8.9×10^{-5}	3.5
Conductive Epoxy (Die)	8.9×10^{-5}	3.5
Dielectric Epoxy (Substrate)	1.3×10^{-4}	5
70 - 30 In - Pb Solder	1.5×10^{-4}	6

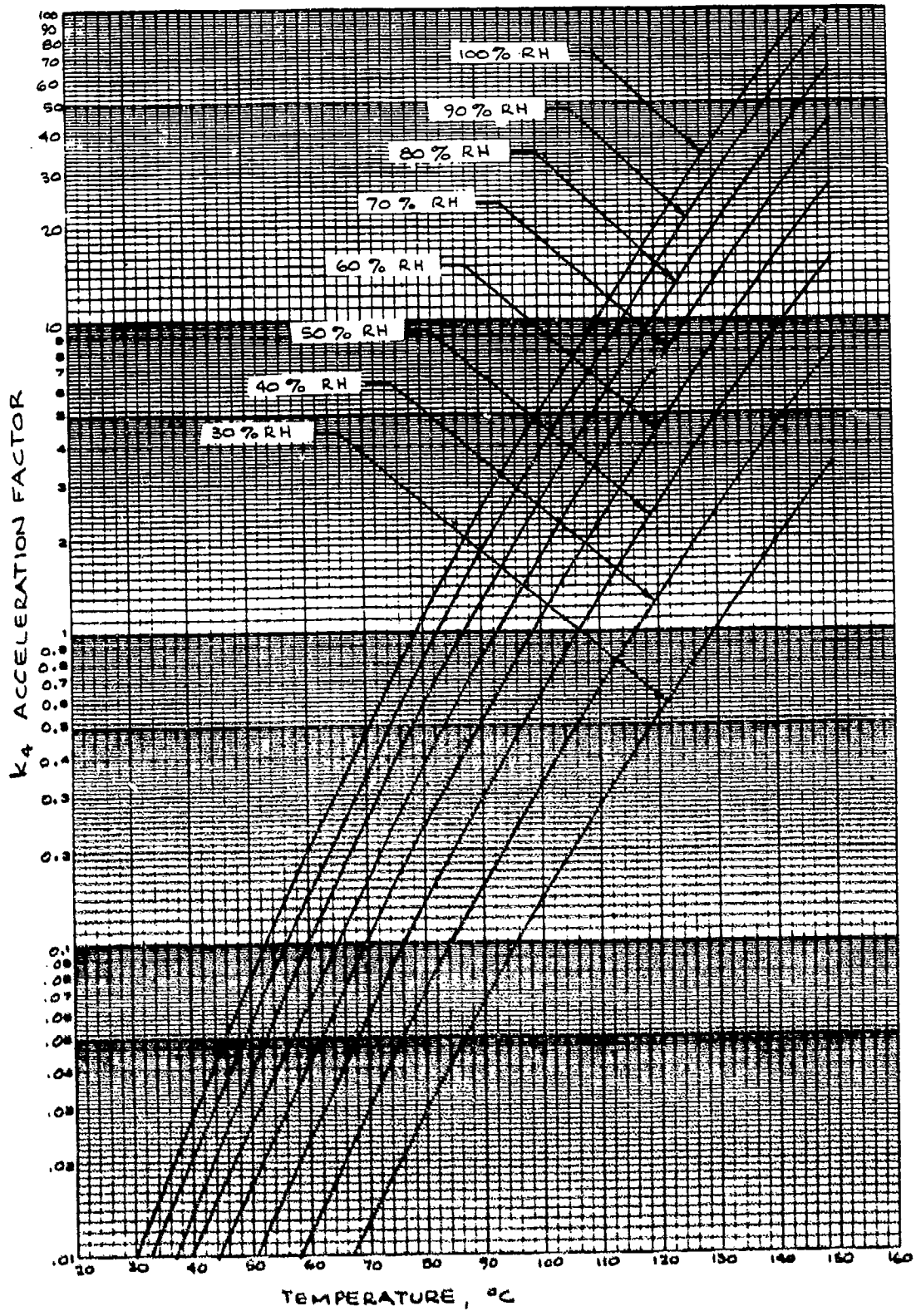
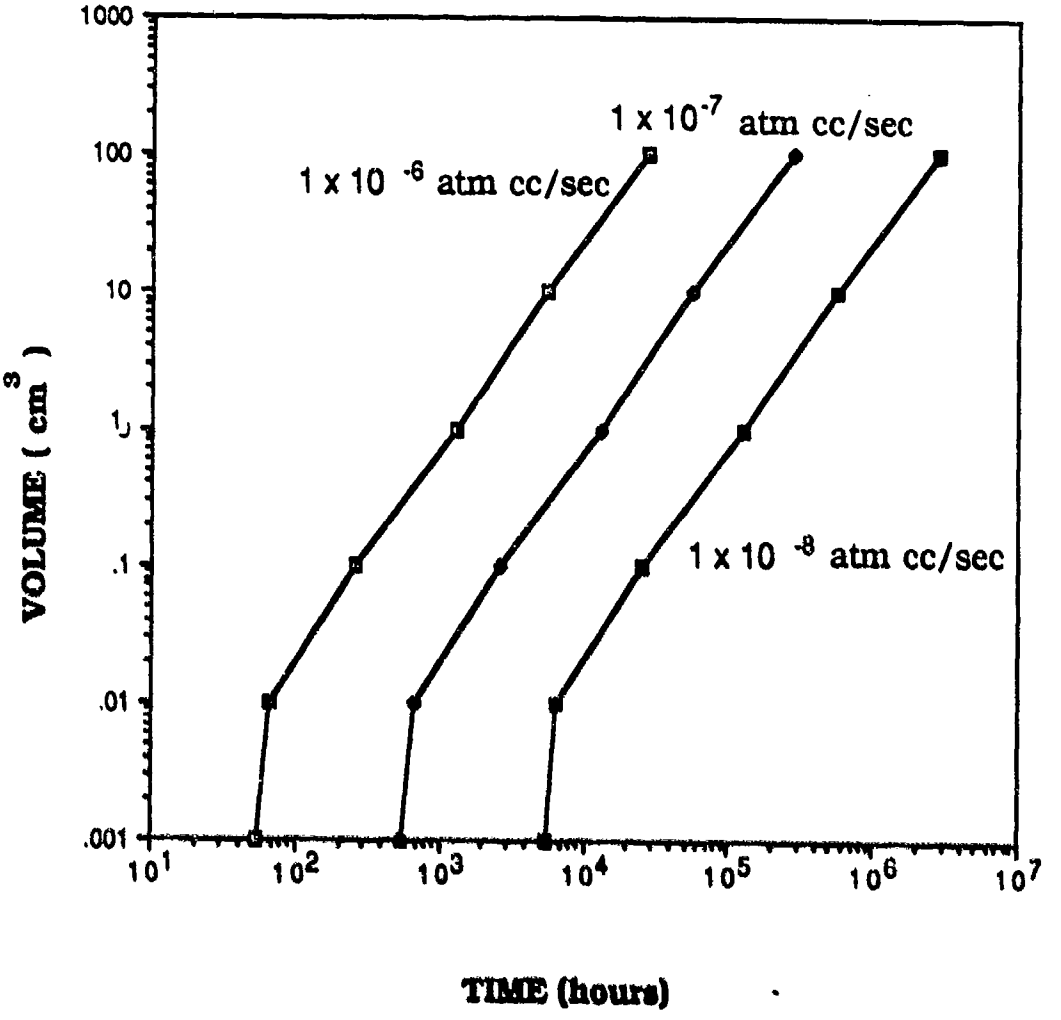


Figure 4.5-1 TEMPERATURE-HUMIDITY ENVIRONMENT ACCELERATION FACTOR

Figure 4.5-2

Time to Reach 3 Monolayers of H^2O as a Function of Package Internal Volume and Air Leak Rate



4.6 ADJUSTMENT (Pi) FACTORS

4.6.1 Quality Factor (π_Q)

The quality factors for microcircuits found in MIL-HDBK-217E are multipliers of the base failure rate, and they are intended to reflect the differences in quality to be found in parts made to differing process controls. However, the factor descriptions reflect part qualification, screening performed, procurement practices, and package material. In reality, the quality of an IC is dependent upon the manufacturer's process controls alone, and that information cannot be quantified in a reliability model. However, there is good correlation between the amount of screening performed and the ultimate field reliability of the parts: the more screening, the less probability of infant mortality failures in the field. Consequently, the approach taken in developing the quality factors has been to concentrate on the effects of screening and to quantify the effectiveness of MIL-STD-883 screens. The quality factors are modifiers of the early-mid life failure rate only and do not affect the failure rates associated with common cause (wearout) failure mechanisms.

At a meeting held in Monterey, California as part of this contract, several IC manufacturers* stated that there is no difference between their commercial lines and their military lines, but the military product is screened more. Others stated that their screening of commercial product in some cases exceeds the military requirements, and they should be given credit in a model for more rigorous screening. The π_Q model developed in the following paragraphs is flexible in allowing for variations in the amount of screening performed.

* Attendees included representatives from the following companies: Anadigics; LSI Logic; Intel Corp.; Teledyne Microelectronics; SEEQ Technology; D. Steward Peck Consulting; and Westinghouse.

Adjusted failure mechanism quantities for all technology types listed in MDR-21 (1985) were itemized and totaled; the percentage contribution of each failure mechanism was computed. See Table 4.6-1. The MIL-STD-883 screens which are effective at precipitating the various failure mechanisms were identified by analysis of MDR-22 (1987) and are presented in Table 4.6-2. Table 4.6-3 lists the failure mechanisms, their distributions, and the associated screens. The percentages of each failure mechanism which are precipitated by the screens were summed, then normalized to form a total of 100; each screen's percentage of the total was then calculated, as in Table 4.6-4, and these percentages are referred to as "weighting factors" for their respective screens. The screening methods which are associated with the S, B, D and D-1 quality levels were also identified, and the weighting factors for each were summed to provide the "screening factor" for that quality level. The weighting factor for burn-in was adjusted to differentiate between S- and B- level burn-in. This was accomplished by calculating the expected fallout using the two time - temperature combinations and an average activation energy of 0.37 ev, which was derived from the MIL-STD-883 burn-in curves, as in Table 4.6-5 (high temperature reverse bias (HTRB) is an optional replacement for S-level burn-in). The screening factors for S, B, D and D-1 are 100.0, 71.3, 21.8 and 10.9, respectively. To develop π_Q, the value for B-level was chosen as unity because (1) it is consistent with the current value, and (2) most of the data collected in the model development activity was on B-level product. Two points on the curve were thus known: $\pi_Q = 1.0$ for B-level (screening factor = 71.3), and $\pi_Q = .7$ for maximum screening, S-level. The relationship π_Q = 71.3/screening factor (S.F.) was easily established. This relationship is depicted graphically in figure 4.6-1. It is intuitive that the most benefit is achieved with the first screens applied, and that the marginal improvement with succeeding screens is lower; the shape of the π_Q curve reflects that fact.

In order to calculate π_Q, the user must identify which of the Table 4.6-4 screens apply to the product, sum the weighting factors associated with those screens to compute the screening factor, and then use the expression π_Q = 71.3/S.F. to determine the value of the quality factor.

Table 4.6-1: Failure Totals vs Failure Mechanisms By Device Types*

	DEVICE TYPES					SUM	PERCENT OF
FAIL - MECH	DIGITAL	LINEAR	INTERFACE	MEMORY	VLSI	TOTAL	TOTAL
METALLIZATION	89	27	16	236	10	378	10.7
DIFFUSION	23	7	3	0	2	35	< 1
OXIDE FAULT	386	38	6	40	4	474	13.5
BULK	48	56	0	3	2	109	3.2
SURFACE	405	313	16	8	17	759	21.5
INTERCONNECTS	260	19	10	7	2	298	8.5
WIREBOND	3	21	6	0	6	36	1.1
PACKAGE	1341	42	10	35	8	1436	40.5
FAILURE TOTALS:	2555	523	67	329	51	3525	100

*Source: RAC MDR-21

Table 4.6-2

Recommended Screens/Tests for Various Failure Mechanisms*

SURFACE DEFECTS	
☐ Contamination/Leakage	- 1008, 1015/5005
☐ Foreign Material/Particles	- 2001, 2012, 2020, 2010
☐ Inversion/Channelin	- 1008, 1015/5005, HTRB
BULK DEFECTS	
☐ Crystal Imperfections	- 1008, 1010, 1015/5005, 5007
☐ Cracked Die	- 1010, 1015/5005
OXIDE DEFECTS	- 1010, 1015/5005, HTRB
DIFFUSION DEFECTS	
☐ Isolation Defects	- 1015/5005
☐ Mask Faults	- 1015/5005
METALLIZATION DEFECTS	
☐ Open At Oxide Step/ Contact Window	- 1010, 1015/5005
☐ Short In Interlayer	- 1010, 1015/5005
☐ Pitted/Corroded	- 2010/2017
☐ Smeared/Scratched	- 2010/2017
☐ Electromigration	- 1015/5005
BOND DEFECTS	
☐ Die Attach Defect	- 1010, 2001, 1015/5005, 2012, 2020, 2023
☐ Intermetallic Formation	- 1015/5005
INTERCONNECT DEFECTS	
☐ Broken Wire	- 1010, 1015/5005
☐ Shorted Wire	- 1015/5005
☐ Poor Lead Dress	- 1010, 2001
☐ Corroded Wire	- 1010, 1015/5005
PACKAGE DEFECTS	
☐ Non Hermetic Seal	- 1010, 2001, 1014
☐ Solder Balls (Excessive Seal Material	- 2009, 2020, 2012
☐ External Lead Defect	- 2009

* Source References MIL-STD-883C and RAC MDR-22

Table 4.6-3: IC Failure Mechanisms/Screening Methods

FAILURE MECHANISM	DISTRIBUTION	ASSOCIATED SCREENS
Metallization	11%	1015/5005, 2010/2017, 1010
Diffusion	1%	1015/5005
Oxide Faults	14%	1015/5005, HTRB
Bulk	3%	5007, 1008, 1010, 1015/5005
Surface	21%	2010, 2012, 2020, 2001, 1008, 1015/5005, HTRB
Interconnect	9%	1010, 1015/5005, 2001
Wirebond	1%	2023, 1008, 1010, 2001, 2010, 1015/5005, 2012, 2020
Package	40%	2020, 2012, 1014, 2009, 1010, 2001

Table 4.6-4: Weighting Factor Determination

SCREEN	METHOD	883 ∑%	W.F. %	S	B	D	D-1
Wafer Lot Accept	5007	3	0.05	X			
N.D. Bond Pull	2023	1	0.2	X			
Internal Visual	2010/17	33	6.0	X	X		
Stabilization Bake	1008	25	4.5	X	X		
Temp Cycling	1010	64	11.6	X	X		
Constant Acceleration	2001	71	12.8	X	X		
Pind	2020	62	11.3	X			
Burn-In (S/B)	1015	90/60	16.3/10.9	X	X	X	
Final Electrical	5005	60	10.9	X	X	X	X
Seal Test	1014	40	7.3	X	X		
Radiography	2012	62	11.3	X			
External Visual	2009	40	7.3	X	X		
SUM		551	100.0	100.0	71.3	21.8	10.9

W.F. = Weighting Factor

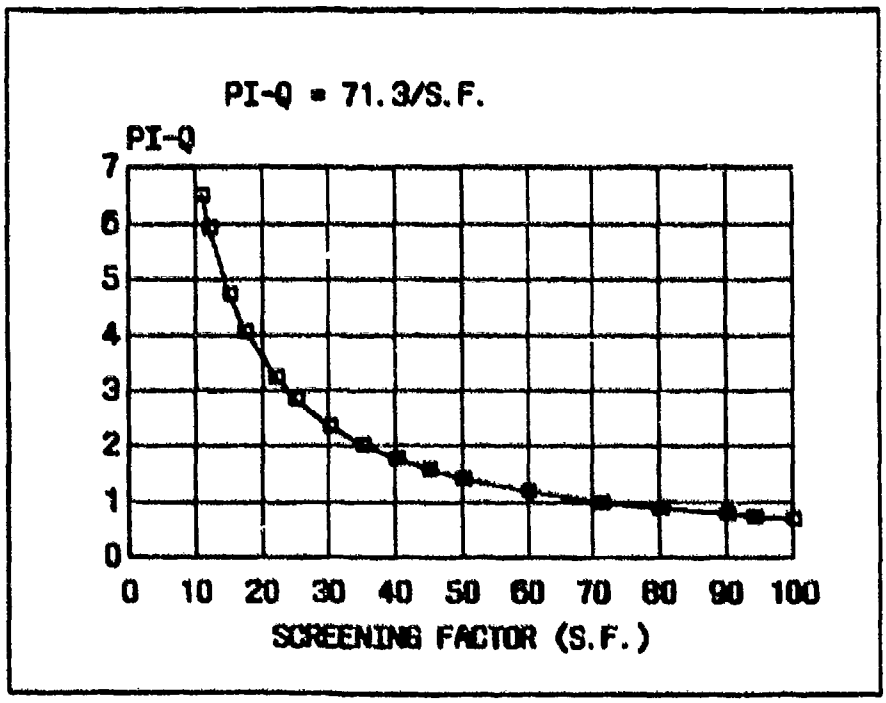
Table 4.6-5: Calculating Burn-In Effectiveness (Fallout)
With E_A = 0.37 eV

Burn-In Level	Time/Temp (Hrs)/(°C)	F(FPMH)	Expected Fallout (Failures x 10^{-6})	Ratio To B-Level
B	160/125	20.84	3334.4	1.0
S	240/125	20.84	5001.6	1.5
HTRB	72/150	39.41	2837.5	0.85

$$F = e^{-(0.37/((273 + temp) * 8.625 \times 10^{-5}))}$$

Expected Fallout = F x Time

Figure 4.6-1 π_Q vs. Screening Factor (S.F.)



4.6.2 Learning Factor (π_L)

U.S. military integrated circuit manufacturers, through the Semiconductor Industry Association's Government Procurement Committee (GPC), established an ongoing quality statistics program to monitor and report industry data on various quality control indices and parameters. The data indicates that there has been a steady improvement in the level of American quality such that today, for every 10,000 parts shipped, there averages only one part with electrical defects (approximately 100 parts per million or PPM).

Military quality reporting procedures are strictly defined. Companies supplying data utilize the JEDEC Standard No. 16 (Assessment of Microcircuit Outgoing Quality Levels in Parts Per Million) guidelines for reporting outgoing quality levels. The procedures for accumulating and summarizing the data are carefully defined and follow accepted statistical quality control methods. Data reported represents Joint Army-Navy (JAN), Standard Military Drawing (SMD), 883C complaint and military source control drawing (SCD) products. Defect levels are calculated on first submission data only, covering room, hot and cold temperature extremes. The final PPM calculations use a weighted average technique. The PPM and sampling techniques are stated on conservative, statistically sound methods and are described in the JEDEC standard.

Currently there are nine SIA member companies reporting into the system, and these companies supply approximately 90% of all military microcircuits, providing a significant sample of total product consumed by the military.

These companies are:

- Advanced Micro Devices
- General Electric/RCA
- Harris
- Intel
- Motorola
- National Semiconductor
- Rockwell
- Signetics
- Texas Instruments

Data is reported on the following technology groups:

Linear:	Op Amp Based A/D, D/A Converters Other Linear
Bipolar Digital:	Memory Logic Processor/Peripheral
MOS Digital:	Memory Logic Processor/Peripheral

For each product category, reported data includes (a) number of firms responding, (b) total samples tested, and (c) mean defect density levels. Summaries are provided for the three principal product sectors, as well as a total across all products. Hermeticity and visual/mechanical results are reported as aggregate measures. See Table 4.6-6.

In order to develop the learning factor (π_L) from this data, the following assumptions were made:

1. The data presented in Table 4.6-6 represents a mix of mature and immature product for each of the technology lines specified.
2. Mature product may be defined as reaching the 100 PPM level.
3. The definition of mature product will change as the PPM defect density continues to drop, which provides flexibility in the learning factor.
4. The data can be used to represent the "learning curve" experienced by IC manufacturers in general.
5. Although a quality index, PPM defect densities can be used validly to scale failure rates since any defect represents a potential screening escape and future field failure.

Table 4.6-6

SEMICONDUCTOR INDUSTRY ASSOCIATION
QUARTERLY REPORT FOR MILITARY PRODUCTS
MEAN DEFECT DENSITIES

ELECTRICAL QUALITY LEVELS	1Q86	2Q86	3Q86	4Q86	1Q87	2Q87	3Q87	4Q87	1Q88	2Q88
Total Linear	431	486	180	192	191	104	165	106	172	86
Total Digital Bipolar	73	65	65	159	43	35	111	27	87	44
Total MOS Digital	338	259	469	332	223	237	179	294	211	152
Grand Total: All ICs	191	168	169	203	111	93	136	81	133	76
Product Type: All ICs										
Electrical Defects	191	168	169	203	111	93	136	81	133	76
Mean Defect Density							434	344	304	254
Hermeticity Density							278	234	378	260

The data in Table 4.6-6 was linearly regressed both as PPM vs. time and as ln (PPM) vs. time. The latter yielded better correlation coefficients (0.6 for the composite "all integrated circuits" case). See figure 4.6-2. The composite data was used instead of the individual technology data for two reasons. First, not all technology areas are addressed, e.g., there is no GaAs data. Second, the PPM levels for digital bipolar are already below the value assumed for mature product, presumably because the technology is mature and testing requirements are well defined. However, a new IC manufacturer or one introducing a new line of components would still have to develop his processes in order to realize 100 PPM, and two years is a reasonable amount of time in which to do so.

Invoking assumption 2 above, mature product is achieved after 2.129 years, or during the first quarter of 1988 (ln 100 = 4.605). Since this time-frame is coincident with the data being collected on the RAAAT program, failure rates can be normalized to the 100 PPM point on the learning curve. When this is done, the value of π_L is unity at time = 2.129 yrs. Then, π_L can be defined as the ratio of the PPM defect density at any time Y to 100 PPM. The equation for π_L becomes:

$$\pi_L = EXP\ (-0.35Y + 5.35)/100 = 0.01 * EXP\ (5.35 - 0.35Y)$$

where Y is in years. A plot of π-L vs. time is shown in figure 4.6-3.

The curve indicates that the failure rates of ICs will drop by an order of magnitude over a seven year interval, which seems reasonable. The learning curve factor (π_L), as with the quality and environmental factors, is a modifier of the early life (defect-related) IC failure rate; it does not affect the wearout mechanisms.

Figure 4.6-2 SIA Data Plot

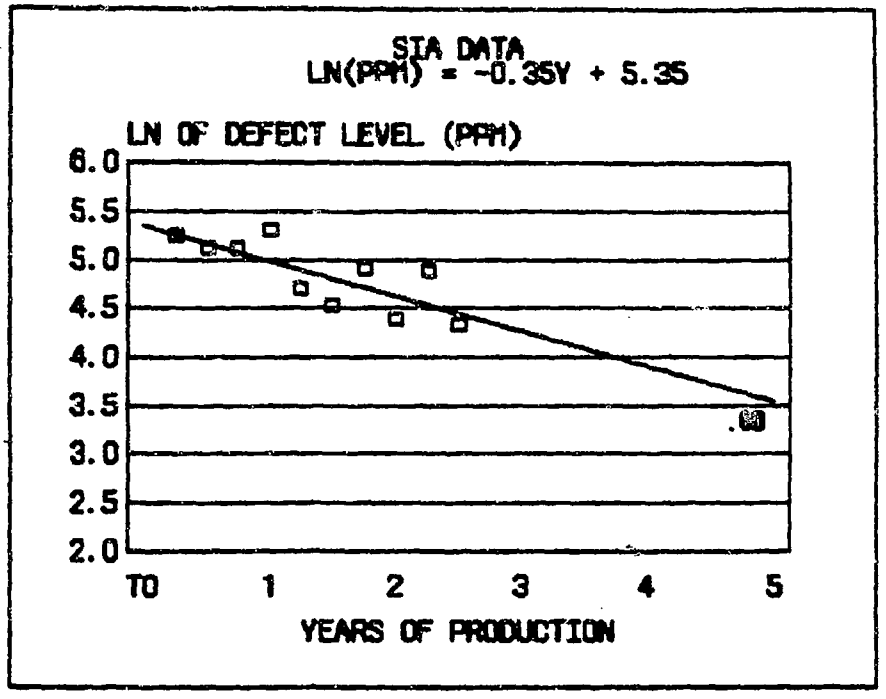
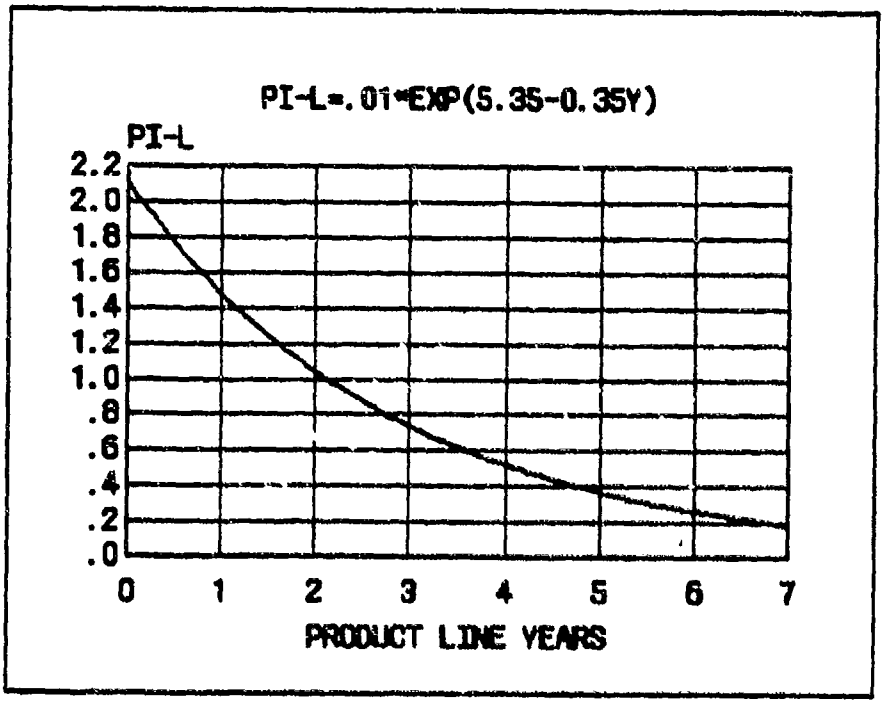


Figure 4.6-3 π_L vs. Product Line Years



4.6.3 Hybrid Function Factor (π_F)

The concept of an application function factor was retained in the hybrid model. The basis for this factor is the variations in the processes used in different types of hybrids and the relative difficulty of these processes. Listed below are the hybrid technology groups and some examples of their unique features.

Digital - Standard packaging techniques. Base line for factor.
Linear - More custom package styles.
Video - Higher frequency packaging techniques, use of discrete inductors.
Microwave - Packaging techniques, use of transmission line structures, greater variety of materials, small-geometry.
Power - Die attach critical, layout based on voltage considerations.

Data collected from field experience on the APG-68 radar and from 1000 hour life tests of various hybrid types were used to determine the function factors. A summary of the field data which was presented in Table 4.4-1 is shown in Table 4.6-7 below. The averages have been computed by adding the total number of failures within a family and dividing by the total number of device hours for the time in which the data was accumulated (263,990 system hours). This data along with the life test data is plotted in figure 4.6-4.

The life test data was taken from the data in Table 4.4-2 of section 4.4.1. Only the 125°C life test data was used. The only data omitted from the calculation of failure rates was improper test temperatures or devices which were overstressed in test. The data used is shown in Table 4.6-8. The point estimates of failure rates for each family were calculated at 50% confidence using the Chi-square distribution. The results are shown in Table 4.6-7.

It should be noted that the number of secondary failures and erroneous removals cannot be separated from the field data. The relative family ranking within the two sets of data seems to verify differences between most of the classes defined. Since the life test is the more accurate of the two, the π_F factor is based on these failure rates. The π_F factors chosen are shown in Table 4.6-7. They have been normalized to the digital family since this is the more standardized technology and is also the reference point in the present model. The number for the microwave family was obtained by interpolating the relative ranking in the field data and applying the same percentage to the life test ranking.

Table 4.6-7
Failure Rates By Hybrid Types

	FIELD DATA (REMOVAL RATE/MILLION HR.)	LIFE TEST DATA (FAILURE RATE/MILLION HR)· 50% CONFIDENCE
Digital	34.1	9.9
Video	11.2	12.4
μWave	23.1	--
Linear	52.7	57.2
Power	73.3	205

	π_F NORMALIZED TO DIGITAL
Digital	1.0
Video	1.2
μWave	2.6 (interpolated using field data)
Linear	5.8
Power	21

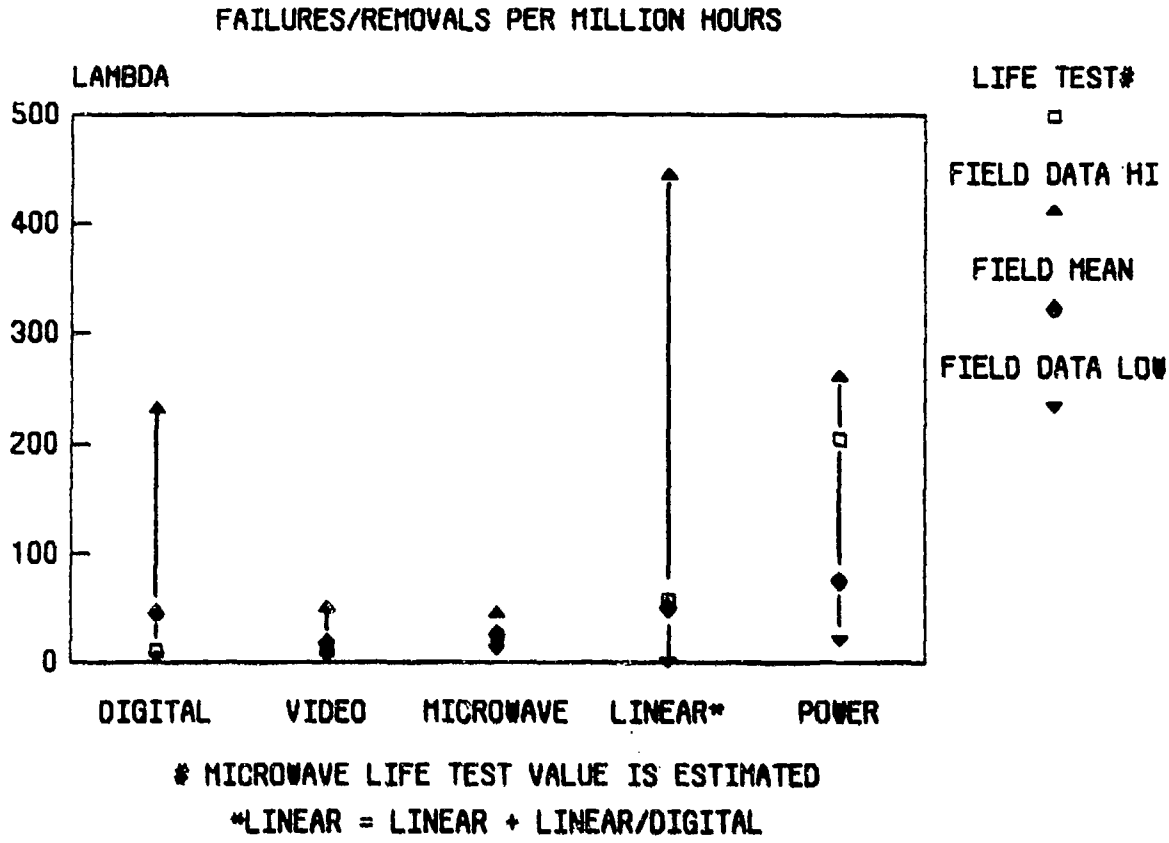
Table 4.6-8
Life Test Data

QTY TYPE	P/N	SAMPLE QTY	TEST HOURS	DEVICE HOURS	FAIL	FAILURE	VENDOR
Digital	586R291	22	1000	22,000	0		WEC
	585R927	16	1000	16,000	0		WEC
	586R517	5	1000	5,000	0		WEC
	585R928	22	1000	22,000	0		WEC
	583R379	5	1000	5,000	0		WEC
			TOTALS	70,000	0		
Linear	586R292	5	1000	5,000	0		Teledyne
	586R587	22	1000	22,000	0		Teledyne
	586R290	22	1000	22,000	0		Teledyne
	581R772	2	1500	3,000	2	Al/Au intermetallic	WEC
	587R322	5	1000	5,000	0		Teledyne
	584R555	1	750	750	1	Lifted wire bond	WEC
	584R555	1	1500	1,500	0		WEC
	585R149	2	1000	2,000	0		WEC
	585R150	2	1000	2,000	0		WEC
			TOTALS	64,250	3		
Video	24552	1	2880	2,880	0		Anaren
	24552	1	5760	5,760	0		Anaren
	24552	1	720	720	1	Seal	Anaren
	24552	1	1440	1,440	1	Electrical	Anaren
	24552	1	2943	2,943	1	Electrical	Anaren
	24552	1	5281	5,281	1	Electrical	Anaren
	22306	3	1440	4,320	0		Anaren
	22306	1	720	720	1	Seal	Anaren
	22306	2	1440	2,880	2	Electrical	Anaren
	22078	1	5760	5,760	0		Anaren
	22078	2	6323	12,646	2	Electrical	Anaren
	20858	3	5760	17,280	0		Anaren
	20864	1	2880	2,880	0		Anaren
	20864	1	5760	5,760	0		Anaren
	20864	1	2160	2,160	0		Anaren
	20864	1	1440	1,440	1	Seal	Anaren
	20864	1	3600	3,600	1	Seal	Anaren
	12604427	37	1000	37,000	0		Teledyne
	12604427	1	504	504	1	Unknown	WEC
	Various	9	1000	9,000	0		Q-Bit
	Various	76	1000	76,000	0		Q-Bit
	Various	939	1000	939,000	0		Q-Bit
	Various	2	1000	2,000	2	Wire-wire shorts	Q-Bit
			TOTALS	1,185,884	14		

Table 4.6-8 (cont)
Life Test Data

TYPE	P/N	SAMPLE QTY	TEST HOURS	DEVICE HOURS	QTY FAIL	FAILURE	VENDOR
Power	584R550	2	1000	2,000	0		WEC
	584R550	1	504	504	1	Cracked die	WEC
	584R550	5	1000	5,000	0		Solitron
	584R551	5	1000	5,000	0		Solitron
	581R082	1	3000	3,000	0		WEC
	581R082	1	2500	2,500	1	Substrate attach	WEC
	585R151	2	1000	2,000	0		WEC
	586R509	1	1000	1,000	0		WEC
	586R509	1	168	168	1	Unknown	WEC
	586R508	1	1000	1,000	0		WEC
	586R508	1	504	504	1	Die Attach	WEC
			TOTALS	22,676	4		

Figure 4.6-4
Hybrid Failure Rates



MICROWAVE LIFE TEST VALUE IS ESTIMATED
*LINEAR = LINEAR + LINEAR/DIGITAL

4.6.4 Environmental Factor (π_E)

The environment influences the failure rate of integrated circuit dice by accelerating the precipitation of package related defects in the early life model. In the long term, the magnitude and frequency of temperature cycling has a pronounced effect upon the package related mean time to failure, as discussed in section 4.5.

The development of environmental factors for advanced technology devices was hampered by the fact that there are not many of these devices in the field. In addition, part of the tasking was to develop a new set of factors such as would be compatible with the current MIL-HDBK-217E models for SSI, MSI and LSI packaged devices. These constraints dictated the use of the $C_2\pi_E$ term to model the contribution of package related defects to the early life failure rate.

In order to satisfy the requirement for fewer environmental factors, the environments were grouped by usage environment based on equipment classifications. The environmental temperature ranges and the military specifications from which they were derived are presented in Table 4.6-9. These groupings accounted for 25 of the 27 environments listed in MIL-HDBK-217E. Default values for the average component case temperature and the worst case temperature excursion for each of the grouped environments were calculated, and these values are used in the package wearout models of section 4.5

The early life environmental factors were derived by calculating the geometric mean of the MIL-HDBK-217E values given for the grouped environments. These values are presented in Table 4.6-10.

Table 4.6-9 Environmental Temperature Ranges

USAGE ENVIRONMENT CLASSIFICATION			EQUIPMENT SPECIFICATIONS				
MIL-HDBK-217E	PROPOSED	TCASE°C					
			MIL-E-5400				
			CLASS 1/1A	CLASS 1B	CLASS 2	CLASS 3	CLASS 4
A_{UA} A_{UB} A_{UC} A_{UF} A_{UT}	A_U	95°C	-54/+55°C		-54/+71°C	-54/+95°C	-54/+125°C
A_{IA} A_{IB} A_{IC} A_{IF} A_{IT} A_{RW}	A_I	95°C		-40/+55°C			
			MIL-E-16400				
			UNSHELTERED		SHELTERED		
			SHORE	SHIP	SHORE	SHIP	
N_U	N_U	80°C	-54/+65°C	-28/+65°C			
N_{UU}	N_{UU}	25°C					
U_{SL}	N_{UL}	40°C			-40/+50°C	0/+50°C	
N_H N_S N_{SB}	N_I	45°C					
			DOD-E-8983				
M_{FA} M_{FF} M_L	M_F	60°C	-51/+49°C				
S_F	S_F	45°C	-34/+71°C				
			MIL-E-4158				
			COLD		TEMPERATE		DESERT/TROPICAL
G_B G_{MS}	G_B	35°C	-54/+52°C		-40/+52°C		0/+81°C
G_M M_P	G_M	50°C					
G_F	G_F	45°C					
C_L	C_L	45°C					

Table 4.6-10

Integrated Circuit Environmental Factors

MIL-HDBK-217 E ENVIRONMENT	PROPOSED ENVIRONMENT	GEOMETRIC MEAN VALUE
A_{UA} = 6.0 A_{UB} = 7.5 A_{UC} = 3.0 A_{UF} = 9.5 A_{UT} = 4.0	A_U (AIRBORNE UNINHABITED)	5.5
A_{IA} = 4.0 A_{IB} = 5.0 A_{IC} = 2.5 A_{IF} = 6.0 A_{IT} = 3.0 A_{RW} = 8.5	A_I (AIRBORNE INHABITED)	4.4
N_U = 5.7	N_U (NAVAL UNSHELTERED)	5.7
N_{UU} = 6.3	N_{UU} (NAVAL UNDERSEA UNSHELTERED)	6.3
U_{SL} = 11.0	N_{UL} (NAVAL UNDERSEA LAUNCH)	11.0
N_H = 5.9 N_S = 4.0 N_{SB} = 4.0	N_I (NAVAL INHABITED)	4.6
M_{FA} = 5.4 M_{FF} = 3.9 M_L = 13	M_F (MISSILE FLIGHT)	6.5
S_F = 0.9	S_F (SPACE FLIGHT)	0.9
G_B = 0.38 G_{MS} = 0.65	G_B (GROUND BENIGN)	0.5
G_M = 4.2 M_P = 3.8	G_M (GROUND MOBILE)	4.0
G_F = 2.5	G_F (GROUND FIXED)	2.5
C_L = 220	C_L (CANNON LAUNCH)	220

5.0 MODEL VALIDATION

Data to model the failure rates of new technology devices was sparse since most of these devices have only recently become available commercially. The collection of data was further hampered by the proprietary nature of much of the data. Consequently, all of the data which was collected was used in the development of the models and could not be used for validation. The alternative validation methodology was to compare the predicted early life failure rates of representative microcircuits with the observed range of values from the database. The resulting values of the predicted to observed ratio were then evaluated for model accuracy. When only one data point was found, the high, low, and average values are the same. In addition, a comparison to the extrapolated MIL-HDBK-217 model has been made where appropriate. Table 5-1 presents the results of this effort. Some of the models are optimistic, some conservative; some yield higher failure rates than MIL-HDBK-217, some lower. All average failure rates are within the realm of acceptability, and most are conservative. No models for GaAs microcircuits exist in the current version of the MIL-HDBK. However, figure 5-1 compares the integrated circuit digital and MMIC GaAs models to the silicon based 217E GaAs driver FET model, the 217E Notice-1 GaAs low noise FET model, and the 217E Silicon ALS digital integrated circuit model. The higher activation energies for the GaAs integrated circuit models are apparent and indicate a higher temperature dependence of the failure rate at higher temperatures where the active device failure rates dominate the models. The effect of the passive failure rate term of the model is observed at the lower temperature. The comparison also indicates that the integrated circuit GaAs model failure rates lie between the discrete GaAs models and the silicon ALS digital integrated circuit model.

The hybrid model was validated by calculating several hybrid examples and comparing results with MIL-HDBK-217E. The calculations and results are shown below. For these calculations, it was assumed that the effects of the wearout failure mechanisms for the die and package were negligible.

Table 5-1

MODEL VALIDATION

DEVICE TYPE	λ_O (HIGH)	λ_O (AVG.)	λ_O (LOW)	T_O (°C)	λ_{217E}* (at T_O)	λ_p (at T_O)	λ_p/λ_O (HIGH)	λ_p/λ_O (AVG)	λ_p/λ_O (LOW)
CMOS VLSI (30K-60K Gates)	.1627	.0290	.0009	25	.0320	.0290	.18	1.00	32.2
CMOS VLSI (30K-60K Gates)	.6677	.6677	.6677	125	.6942	.06942	1.03	1.03	1.03
16 bit µp (MOS)	.2294	.1827	.1545	70	.0768	.1456	.63	.80	.94
16 bit mp (TTL)	.1803	.1803	.1803	70	.0768	.1188	.66	.66	.66
GaAs MMIC	1.29	.515	.206	150	--	.451	.35	.88	2.19
GaAs Digital	4.58	.391	.033	150	--	2.53	.55	6.47	76.0
GaAs Passive	.305	.0424	.0059	150	--	.125	.41	2.94	21.1
DRAM, NMOS, 64K bit D level	2.09	2.09	2.09	125	6.5	2.05	.98	.98	.98
SRAM, NMOS, 16K bit D level	6.39	6.39	6.39	125	13.0	6.38	.998	.998	.998
SRAM, TTL, 2K bit D Level	5.55	5.55	5.55	125	5.0	4.25	.766	.766	.766
EEPROM, Tex-Poly NMOS 16K bit, D level	2.12	2.12	2.12	125	7.8	.717	.338	.338	.338
EEPROM, FLOTOX NMOS 16K bit, D level	1.83	1.83	1.83	125	7.8	.697	.38	.38	.38

λ_O = λ Observed λ_p = λ Predicted, New Model λ_{217E} = λ Predicted Per MIL-HDBK-217E (Extrapolated As Necessary)

Table 5-1 (cont)

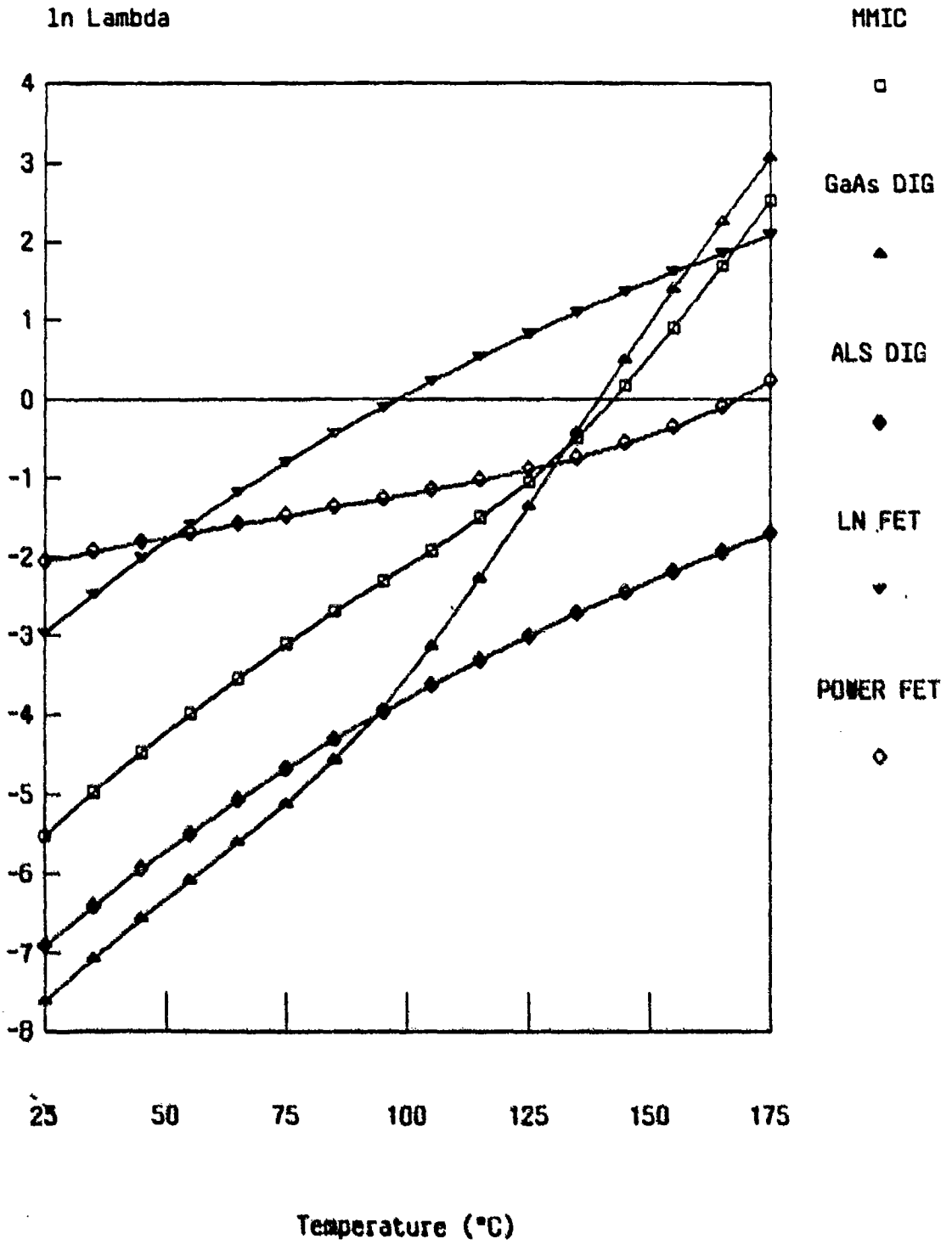
MODEL VALIDATION

DEVICE TYPE	λ_O (HIGH)	λ_O (AVG.)	λ_O (LOW)	T_O (°C)	λ_{217E}* (at T_O)	λ_p (at T_O)	λ_p/λ_O (HIGH)	λ_p/λ_O (AVG)	λ_p/λ_O (LOW)
EEPROM, Tex-Poly NMOS 64K bit, D level	1.72	1.72	1.72	125	15.6	1.41	.82	.82	.82
EEPROM, FLOTOX 64K bit, D Level	2.55	2.55	2.55	125	15.6	1.39	.54	.54	.54
UVEPROM, CMOS 64K, D Level	8.16	4.53	.91	125	26.4	1.38	.17	.30	1.51
UVEPROM, NMOS 256K, D Level	6.04	6.04	6.04	125	52.8	2.77	.46	.46	.46
UVEPROM, NMOS 512K, D Level	3.14	3.14	3.14	125	105.6	5.55	1.76	1.76	1.76
FPLA, TTL < 100 gates D Level	13.86	7.62	1.39	125	3.0	8.57	.62	1.12	6.16
ROM, NMOS 32K, D Level	.34	.34	.34	125	9.1	1.06	3.12	12	3.12
ROM, NMOS 64K, D Level	1.67	1.67	1.67	125	9.1	1.06	.63	.63	.63
ROM, NMOS 256K	1.80	1.80	1.80	125	18.2	2.13	1.18	1.18	1.18
PROM, TTL 8K, D Level	4.00	4.00	4.00	125	3.0	7.69	1.92	1.92	1.92
PROM, TTL 16K, D Level	4.01	4.01	4.01	125	3.0	7.69	1.92	1.92	1.92
PROM, TTL 32K, D Level	7.70	7.70	7.70	125	6.0	15.4	2.0	2.0	2.0
LS TTL Linear Hybrid	2200.0	57.2	31.5	125	12.3	36.2	.016	.63	1.15

λ_O = λ Observed λ_p = λ Predicted, New Model λ_{217E} = λ Predicted Per MIL-HDBK-217E (Extrapolated As Necessary)

Figure 5-1

GaAs Model Comparison with 217E Models



Example 1

Hybrid Microcircuit Description: RAM I/O, Digilog
Part Number: 586R290
Package: Hermetic, Butterfly; 1.0 x 2.0 in seal; 1.75 x 0.8 in. substrate
Interconnections: Bimetal 165; single metal 74
Active Components: 4-54LS374; 1-54LS154; 1-54LS175; 1-54LS74; 1-54LS04; 1-54LS08; 1-7820
Passive Components: 2-Ceramic chip capacitors, 15% stress ratio, 0.1 μf
1-Ceramic chip capacitor, 15% stress ratio, .001 μf
4-Thick film resistors
Environment: AUF; 45°C package temperature screened to MIL-STD-883, Method 5008, π_Q = 1.0

Calculation per MIL-HDBK-217E:

Failure rate of ICs ($\lambda_C \pi_G$) = 0.0584
Failure rate of chip capacitors (includes π_G) = 0.0594
Failure rate of resistors = 0.0004
Failure rate of interconnects = 0.1141
Failure rate of package = 0.1016
Density factor (π_D) = 2.10
Function factor (π_F) = 1.25
Environmental factor (π_E) = 4.0
Quality factor (π_Q) = 1.0

$$\lambda = ((\Sigma N_C \lambda_C \pi_G) + [N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S] \pi_F \pi_E) \pi_Q \pi_D$$
$$= ([(0.0584) + (0.0594)] + [0.0004 + 0.1141 + 0.1016](1.25)(4.0))(1.0)(2.10)$$
$$= (0.1178 + 1.0805)(1.0)(2.10)$$
$$\approx 2.52 \text{ failures}/10^6 \text{ hours}$$

Calculation - per equation 4.4.4:

$$\lambda = (\Sigma N_C \lambda_C (1 + .2\pi_E)) \pi_Q \pi_L \pi_F$$

$= \{[.0584 + (.0594 / 0.8)](1 + (.2)(4.0)\} (1.0)(1.0)(5.8)$

$= \{(.13265)(1.8)\}5.8$

$= 1.38$ failures/10^6 hours

Example 2

Hybrid Microcircuit Description: Inverter Bridge, Power
Part Number: 584R551
Package: Hermetic, PHP, 1.3 x 1.7 in seal; 1.5 x 1.0 in. substrate
Interconnections: Bimetal 14; single metal 36
Active Components: 4-Si NPN Darlington transistors (MJ10009)
27% stress ratio for voltage,
12.7% stress ratio for power;
Switching application, 175 W rating
4-Si General purpose diodes (Solitron ZLX-C-101);
54% stress ratio, switching application 10 A rating
Passive Components: 4-Tantalum chip capacitors, 10% stress ratio, 0.27 μf
8-Thick film substrate resistors
Environment: AUF; 100°C package temperature screened to MIL-STD-883,
Method 5008, $\pi_Q = 1.0$

Calculation per MIL-HDBK-217E:

Failure rate of transistors (includes π_G) = 0.0196
Failure rate of diodes (includes π_G) = 0.0029
Failure rate of capacitors (includes π_G) = 0.4307
Failure rate of resistors = 0.0016
Failure rate of package = 1.1336
Failure rate of interconnects = 0.1712
Density factor (π_D) = 1.02
Function factor (π_F) = 1.25
Environmental factor (π_E) = 4.0
Quality factor (π_Q) = 1.0

$\lambda = \{(\Sigma N_C \lambda_C \pi_G) + [N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S] \pi_F \pi_E \} \pi_Q \pi_D$

$= \{ 0.4532 + [0.0016 + 0.1712 + 1.1336] (1.25)(4.0)\} (1.0)(1.02)$

$= (0.4532 + 6.532) (1.02)$

= 7.125 failures/10^6 hours

Calculation per equation 4.4.4:

$$\lambda = \{ \Sigma N_C \lambda_C (1 + .2\pi_E)\} \pi_Q \pi_L \pi_F$$
$$= \{[(.0196 / .4)+(.0029 / .2)+(.4307 / .8)][1+.2 (4.0)]\}(1.0)(1.0)(21)$$
$$= (.6019)(1.8)(21)$$
$$= (1.083)(21)$$
$$= 22.75 \text{ failures} / 10^6 \text{ hours}$$

Example 3

Hybrid Microcircuit Description: Dumped Integrator, Digital
Part Number: 585R927
Package: Hermetic, Butterfly, 1.0 x 2.0 in seal; 1.75 x 0.8 in. substrate
Interconnections: Bimetal 212; single metal 58
Active Components: 4-10581; 1-10579; 3-10576
Passive Components: 4-Ceramic chip capacitors, 10% stress ratio, 1000 pf
8-Chip resistors
Environment: AUF; 80°C package temperature screened to MIL-STD-883, Method 5008, π_Q = 1.0

Calculation per MIL-HDBK-217E:

Failure rate of ICs ($\lambda_C \pi_G$) = 0.176
Failure rate of chip capacitors (includes π_G) = 0.0365
Failure rate of resistors = 0.0012
Failure rate of interconnects = 0.6077
Failure rate of package = 0.5143
Density factor (π_D) = 2.24
Function factor (π_F) = 1.0
Environmental factor (π_E) = 4.0
Quality factor (π_Q) = 1.0

$$\lambda = ((\Sigma N_C \lambda_C \pi_G) + [N_R \lambda_R + \Sigma N_I \lambda_I + \lambda_S] \pi_F \pi_E) \pi_Q \pi_D$$
$$= \{ 0.2125 + [0.0012 + 0.6077 + 0.5143] (1.0)(4.0)\} (1.0)(2.24)$$

$= (0.2125 + 4.4928)\ (2.24)$

$= 10.540$ failures/10^6 hours

Calculation per equation 4.4.4:

$$\lambda = \{ \Sigma N_C \lambda_C\ (1 + .2\pi_E)\}\ \pi_Q\ \pi_L\ \pi_F$$
$$= \{[0.176 + (0.0365 / .8)][1 + (.2)(4.0)]\}(1.0)(1.0)(1.0)$$
$$= \{(.2216)(1.8)\}\ 1.0$$
$$= 0.39 \text{ failures}/10^6 \text{ hours}$$

6.0 CONCLUSIONS AND RECOMMENDATIONS

The base failure rate of a VLSI/ULSI microcircuit is due to common cause failures. The final failure rate is adjusted for the lack of ability to eliminate assignable causes of failure from the device population. Development of the failure distributions, early in the life cycle of the microcircuit, by use of test structures designed explicitly for reliability stress testing should be evaluated. It is realized that the test structure stress tests initially only consider the intrinsic reliability of the microcircuit. However, available life test data indicates that many microcircuit failures are due to random point defects. The ability to model this defect density is imperative in the development of an accurate, comprehensive early and middle life VLSI/ULSI reliability prediction model. Therefore, the development of a succinct set of test structures to evaluate the failure rates due to random defects is needed. These structures may have a form similar to those structures used in the generic MIL-M-38510/605 qualifications of product lines.

For the end life prediction models developed, two follow-on efforts were identified: determining the current density dependence on microcircuit complexity, and determining the cause of variability in the TDDB electric field constant β.

If the user does not know the maximum current density in the microcircuit, he must use a default value of 0.125 MA/cm^2, regardless of technology. It is realized that VLSI/ULSI microcircuits approach the MIL-M-38510 current density

limit of 0.5 MA/cm^2 more than the earlier technologies because of the greater circuit densities. A review of metal interconnect widths and thicknesses should be performed to determine the relationship between current density and microcircuit complexity.

From a review of papers which develop the TDDB electric field acceleration constant, ß, it is observed (with one exception[13]) that different oxide thicknesses have different values for ß. The cause of the "variability" in this "constant" should be identified.

The scope of the memory reliability modeling project necessitated limitations on certain aspects of the model development. In addition, information gained regarding some areas of memory suggest the desirability of continuing analysis in specific areas.

Perhaps the most important area that requires further evaluation in UVEPROM, and Flash/NMOS EEPROM is endurance (the failure rate contributed by erase/write cycling). The Time Dependent Dielectric Breakdown model was found to be inadequate for representing the effect of reprogramming. The available data suggest that the combination of high electrical stress and thin oxides precipitate failure in "non-perfect" oxides, and does not lend itself to modeling using deterministic methods. A recommendation in this area is to gather endurance test data for these devices, or generate such data in the event that sufficient test results are not available. An approach similar to that taken for Flotox/Textured-Poly EEPROMs (see section 4.2.2.2) may then be used.

Soft Errors (see section 4.2.2.1) were found to be a significant failure mechanism, at least for certain MOS RAMs under certain circumstances. Further investigation should be devoted to this area. A suggested approach is to use deterministic methods, evaluating the influencing factors outlined in 4.2.2.1 in conjunction with data regarding the sensitivities of different devices. No field data was found during this modeling task that could be used to derive soft error failure rates, and it is likely that such data is not available in sufficient quantity to derive failure rates using probabilistic methods.

Other recommendations relative to memories are as follows:

(1) Refine gate oxide thickness and area charts for all memories. This will permit a more accurate representation of the contribution of time dependent dielectric breakdown.

(2) Collect more life test data to develop a refined model of the defect related failure rate.

MDR-21 was used in the development of several models for this contract. However, MDR-21 needs to be updated to reflect the latest data in the RAC database. This will allow for more accurate determination of screening effectiveness (π_Q values) and activation energies for assignable cause failure mechanisms. The RAC database itself needs to be evaluated for its format and content: it is difficult to read and it contains fields with little or no data of use.

Recommendations for follow-on activities in the packaging area are contained in appendices F, G and H of this report.

The MMIC and digital GaAs failure rate models are believed to be reasonably representative of failure rates for GaAs integrated circuits using MESFET technology and gold based metallization because the models are based on current GaAs integrated circuit failure data. Although the data was limited in quantity, a consensus appeared in the data with regard to the dominant failure mechanism, failure rates, and activation energies especially in the case of the MMIC model. The failure rate data came from published accelerated life test reports and could therefore be relatively optimistic although the data should be representative of good processes under control.

The GaAs models developed in this contract should be continually refined and updated based on new data sources as new data becomes available. The application and complexity factors can be updated as new and more varied applications and higher complexity GaAs devices appear. As field data becomes available on devices with a high number of operating hours, new failure

mechanisms may appear and will have to be added to the models. Careful observation of the passive element failures may improve the passive device factors in the models. More digital GaAs failure rate data should be monitored and compared to the failure rates appearing in the digital model since the model is strongly influenced by a large sample of devices from one manufacturer (GigaBit).

Additional failure rate model efforts should also include new technology GaAs devices which are beginning to emerge. Microwave/Millimeter-wave Integrated Circuits (MIMICs) are higher frequency (30 - 300 GHz) GaAs devices and will be using high electron mobility transistors (HEMT) or heterojunction bipolar transistors (HBT) as the active devices on these integrated circuits. Linear GaAs integrated circuits (op amps, comparators, ...) are also emerging and their failure rates should be monitored for possible model development or the inclusion of an application term.

Due to the experiences encountered on this contract with regard to proprietary information, limited reliability testing and data, and limited or questionable reliability analysis (for failure mechanisms) on advanced emerging technologies, it is highly recommended that independent accelerated life tests be performed by a single contractor to address these concerns. For companies building and selling emerging devices, reliability issues are often a secondary concern. The single contractor would have to have excellent failure analysis capabilities (for determination of failure mechanisms), adequate environmental facilities (for accelerated temperature exposure), adequate electrical testing (for proper biasing, protection, and parametric measurements), and extensive experience in reliability data analysis (for correct interpretation of results and modeling). The major advantage of this recommendation is complete control of part section (all applicable devices can be purchased and covered), conditions (all applicable electrical and environmental conditions can be explored), and analysis (failure mechanism, data, and model analysis). The effort would be expensive but would be the best way to get complete, accurate, and timely failure rate models for emerging technologies.

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MIL-HDBK-217(REV)
MICROELECTRONIC DEVICES

APPENDIX A

5.1.2 MIL-HDBK-217 (REV) Microelectronic Devices
5.1.2.1 Monolithic Bipolar Digital and Linear Gate/Logic Array Devices
5.1.2.2 Monolithic MOS Digital and Gate/Logic Array Linear Devices
5.1.2.3 Monolithic Bipolar and MOS Digital Microprocessor Devices
5.1.2.4 Monolithic Bipolar and MOS Memory Devices
5.1.2.5 Monolithic GaAs Digital Devices
5.1.2.6 Monolithic GaAs MMIC Devices
5.1.2.7 Tables for Monolithic Model Parameters
5.1.2.8 Example Failure Rate Calculations (Monolithic)
5.1.2.9 Multi-chip Hybrid Microcircuits
5.1.2.10 Magnetic Bubble Memory Devices
5.1.2.11 Surface Acoustic Wave (SAW) Devices

5.1.2 Microelectronic Devices. This section presents updated MIL-HDBK-217 failure rate prediction models for nine major classes of microelectronic devices, which are denoted by an asterisk (*).

Monolithic Bipolar Digital and Linear Gate/Logic Array Devices (*)	Section 5.1.2.1
Monolithic MOS Digital and Linear Gate/Logic Array Devices (*)	Section 5.1.2.2
Monolithic Bipolar and MOS Digital Microprocessor Device (Including Controllers) (*)	Section 5.1.2.3
Monolithic Bipolar and MOS Memory Devices (*)	Section 5.1.2.4
Monolithic GaAs Digital Devices (*)	Section 5.1.2.5
Monolithic GaAs MMIC Devices (*)	Section 5.1.2.6
Tables for Monolithic Models Parameters	Section 5.1.2.7
Example Failure Rate Calculations	Section 5.1.2.8
Hybrid Microcircuits (*)	Section 5.1.2.9
Magnetic Bubble Memories (*)	Section 5.1.2.10
Surface Acoustic Wave Devices (*)	Section 5.1.2.11

This revision of MIL-HDBK-217 addresses these technologies and provides new prediction models for bipolar and MOS VLSI microcircuits with gate counts up to 60,000, linear microcircuits with up to 3000 transistors, bipolar and MOS digital microprocessors and co-processors up to 32 bits, memory devices with up to 2 million bits, GaAs monolithic microwave integrated circuits (MMICs) with up to 1,000 active elements, and GaAs digital ICs with up to 10,000 transistors. A major departure from previous versions of the handbook is made in the monolithic bipolar and MOS models by the inclusion of effective hazard rates for the two predominant wearout failure mechanisms, electromigration and time-dependent dielectric breakdown. The early life, or assignable cause, failure rate continues to be represented by C_1 and C_2 factors which account for the contributions of the die and package, respectively, as functions of complexity. The C_1 factors have been extensively revised to reflect new technology devices with improved reliability, and the activation energies representing the temperature sensitivity of the dice (π_T) have been changed for MOS devices and for memories. The C_2 factor remains unchanged from the previous version, but includes pin grid arrays using the same model as hermetic, solder-sealed dual in-line packages. New values have been included for the quality factor (π_Q), the learning factor (π_L), and the environmental factor (π_E). The model for hybrid microcircuits has been revised to be simpler to use, to delete the temperature dependence of the seal and interconnect failure rate contributions, and to provide a method of calculating chip junction temperatures.

In the title description of each monolithic device type, Bipolar represents all TTL, ASTTL, DTL, ECL, CML, ALSTTL, HTTL, FTTL, LTTL, STTL, LSTTL, IIL, I^3L and ISL devices. MOS represents all metal-oxide microcircuits, which includes MNOS, PMOS, CMOS and MNMOS fabricated on various substrates such as sapphire, poly crystalline or single crystal silicon. The hybrid model is structured to accommodate all of the monolithic chip device types and various complexity levels.

Monolithic memory complexity factors are expressed in the number of bits in accordance with JEDEC STD 21A. This standard, which is used by all government and industry agencies that deal with microcircuit memories, states that memories of 1024 bits and greater shall be expressed as K bits, where 1K = 1024 bits. For example, a 16K memory has 16,384 bits, a 64K memory has 65,536 bits and a 1M memory has 1,048,576 bits. Exact numbers of bits are not used for memories of 1024 bits and greater.

The monolithic device models, along with parameter descriptions and instructions for quantifying the parameters are presented in Sections 5.1.2.1 through 5.1.2.6. The tables used for quantifying the model parameters are presented in Section 5.1.2.7.

Models for magnetic bubble memories and model for Surface Acoustic Wave (SAW) devices are listed after the hybrid section.

For devices having both linear and digital functions not covered by MIL-M-38510, use the linear model. Line drivers and line receivers are considered linear devices. For linear devices not covered by MIL-M-38510, use the transistor count from the schematic diagram of the device to determine circuit complexity.

Microprocessors (including controllers) are classified by the number of bits in the data word. This notation is used in data sheets and application notes. For example, the 8080 is an 8 bit microprocessor, the 8086 is a 16 bit microprocessor, etc.

For digital devices not covered by MIL-M-38510, use the gate count as determined from the logic diagram. A J-K to R-S flip flop is equivalent to 6 gates when used as part of an LSI circuit. For the purpose of this Handbook, a gate is considered to be any one of the following functions; AND, OR, exclusive OR, NAND, NOR and inverter. When a logic diagram is unavailable, use device transistor count to determine gate count using the following expressions:

Bipolar: No. Gates = No. Transistors ÷ 3.0

CMOS: No. Gates = No. Transistors ÷ 4.0

Other MOS: No. Gates = No. Transistors ÷ 3.0

The prediction models for monolithic VLSI/ULSI microcircuits have the form

$$\lambda_p(t_0) = \lambda_{AC} + \lambda_{TDDB}(t_0) + \lambda_{EM}(t_0)$$

where

$\lambda_p(t_0)$ = the total part failure rate (at time = t_0) in failures per 10^6 hours

λ_{AC} = the probabilistic (constant failure rate) model for assignable cause (defect-related) failures

$\lambda_{TDDB}(t_0)$ = the end of life model for time-dependent dielectric breakdown

$\lambda_{EM}(t_0)$ = the end of life model for electromigration

t_0 = 10,000 operating hours

5.1.2.1 Monolithic Bipolar Digital and Linear Devices (Including Gate / Logic Arrays)

$$\lambda_P(t_0) = \lambda_{AC} + \lambda_{EM}(t_0) + \lambda_{TDDB}(t_0)$$

$$\lambda_{AC} = \pi_Q (C_1 \pi_T + C_2 \pi_E) \pi_L \qquad \text{(in Failures / } 10^6 \text{ hours)}$$

where:

π_Q is the quality factor, Table 5.1.2.7-1

π_T is the temperature acceleration factor, Table 5.1.2.7-4

π_E is the application environmental factor, Table 5.1.2.7-3

π_L is the device learning factor, Table 5.1.2.7-2

C_1 is the circuit complexity failure rate based on gate or transistor count as follows:

DIGITAL		LINEAR	
# GATES	C_1	# TRANSISTORS	C_1
1 TO 100	.0025	1 TO 100	.01
101 TO 1,000	.005	101 TO 300	.02
1,001 TO 3,000	.01	301 TO 1,000	.04
3,001 TO 10,000	.02	1,001 TO 10,000	.06
10,001 TO 30,000	.04		
30,001 TO 60,000	.08		

C_2 is the package complexity failure rate, Table 5.1.2.7-15.

$\lambda_{EM}(t_0)$ is taken from Table 5.1.2.7-17 (in Failures / 10^6 hours)

$\lambda_{TDDB}(t_0)$ = 0 for bipolar devices due to the thick oxides used in the bipolar fabrication process.

5.1.2.2 Monolithic MOS Digital and Linear Devices (Including Gate / Logic Arrays)

$$\lambda_P(t_0) = \lambda_{AC} + \lambda_{EM}(t_0) + \lambda_{TDDB}(t_0)$$

$$\lambda_{AC} = \pi_Q (C_1 \pi_T + C_2 \pi_E) \pi_L \qquad \text{(in Failures / } 10^6 \text{ hours)}$$

where:

π_Q is the quality factor, Table 5.1.2.7-1

π_T is the temperature acceleration factor, Table 5.1.2.7-4

π_E is the application environmental factor, Table 5.1.2.7-3

π_L is the device learning factor, Table 5.1.2.7-2

C_1 is the circuit complexity failure rate based on gate or transistor count as follows:

DIGITAL		LINEAR	
# GATES	C_1	# TRANSISTORS	C_1
1 TO 100	.01	1 TO 100	.01
101 TO 1,000	.02	101 TO 300	.02
1,001 TO 3,000	.04	301 TO 1,000	.04
3,001 TO 10,000	.08	1,001 TO 10,000	.06
10,001 TO 30,000	.16		
30,001 TO 60,000	.29		

C_2 is the package complexity failure rate, Table 5.1.2.7-15.

$\lambda_{EM}(t_0)$ is taken from Table 5.1.2.7-17 (in Failures / 10^6 hours)

$\lambda_{TDDB}(t_0)$ is taken from Table 5.1.2.7-16 (in Failures / 10^6 hours)

5.1.2.3 Monolithic Bipolar and MOS Digital Microprocessors (Including Controllers)

$$\lambda_p(t_0) = \lambda_{AC} + \lambda_{EM}(t_0) + \lambda_{TDDB}(t_0)$$

$$\lambda_{AC} = \pi_Q (C_1 \pi_T + C_2 \pi_E) \pi_L \qquad \text{(in Failures / } 10^6 \text{ hours)}$$

where:

π_Q is the quality factor, Table 5.1.2.7-1
π_T is the temperature acceleration factor, Table 5.1.2.7-4
π_E is the application environmental factor, Table 5.1.2.7-3
π_L is the device learning factor, Table 5.1.2.7-2
C_1 is the circuit complexity failure rate based on bit count as follows:

# BITS	BIPOLAR	MOS
Up to 8 Bits	0.06	0.14
Up to 16 Bits	0.12	0.28
Up to 32 Bits	0.24	0.56

C_2 is the package complexity failure rate, Table 5.1.2.7-15.

$\lambda_{EM}(t_0)$ is taken from Table 5.1.2.7-17 (in Failures / 10^6 hours)

$\lambda_{TDDB}(t_0)$ is taken from Table 5.1.2.7-16 (in Failures / 10^6 hours)

5.1.2.4 Monolithic Bipolar and MOS Memory Devices

Read Only Memories (ROMs) - MOS and Bipolar
Programmable ROMS (PROMs) - MOS and Bipolar including:
- Ultraviolet Eraseable
- "Flash", MNOS, and Floating gate Electrically Eraseable
- (UVE, Flash, MNOS models valid up to 100 reprogram cycles)

RAMs - including:
- MOS, Bipolar, and BiMOS Static RAMs (SRAMs)
- Dynamic RAMs (DRAMs)

Programmable Array Logic (PALs) - MOS and Bipolar including:
- Programmable Logic Arrays (PLAs)
- Masked Logic Arrays (MLAs), and Hard Array Logic (HALs)

The Model Form is:

$$\lambda_p(t_0) = \lambda_{AC} + \lambda_{EM}(t_0) + \lambda_{TDDB}(t_0)$$
$$= \pi_Q[C_1\pi_T + \lambda_{cyc} + C_2\pi_E]\,\pi_L + \lambda_{EM}(t_0) + \lambda_{TDDB}(t_0)$$

where:

$\lambda_p(t_0)$ is the predicted failure rate in failures per million hours.

$\lambda_{EM}(t_0)$ is the failure rate due to electromigration, taken from Table 5.1.2.7-17.

$\lambda_{TDDB}(t_0)$ is the failure rate due to Time Dependent Dielectric Breakdown, from Table 5.1.2.7-16. Refer to section 5.1.2.4.1.

C_1 is the base failure rate for assignable cause failures. Refer to Table 5.1.2.4-1.

π_T is the temperature multiplier for the assignable cause failure rate. Refer to Table 5.1.2.7-10.

λ_{cyc} is the EEPROM* read/write cycling induced failure rate, and is:

$$\lambda_{cyc} = [A_1B_1 + A_2B_2/\pi_Q]\ \pi_{ECC}$$

where:

A_1 and A_2 are the base cycling failure rates.
Refer to Tables 5.1.2.4-2 and 5.1.2.4-3.

B_1 and B_2 are the temperature/complexity multipliers.
Refer to Tables 5.1.2.4-4 through 5.1.2.4-6.

π_{ECC} is the on-chip error correction factor:
- = .7174 for Hamming Code with 8 data bits and 4 correct bits
- = .6667 for a two-needs-one redundant cell approach
- = 1.0 for any device not using on-chip error correction

* λ_{cyc} = 0 for all devices other than Flotox or Textured Poly EEPROMs.

C_2 is the package base failure rate. Refer to Table 5.1.2.7-15
π_E is the environmental factor. Refer to Table 5.1.2.7-3
π_Q is the quality factor. Refer to Table 5.1.2.7-1
π_L is the learning factor. Refer to Table 5.1.2.7-2

5.1.2.4.2 C_1 Factor (Memories)

Table 5.1.2.4-1 C_1 Factors

MOS PROMs (Including UVEPROMs, EEPROMs, Floating gate MOS PALs/PLAs)

MOS PROMs	C1
Up to 16K bits	.00085
16K < X ≤ 64K	.00169
64K < X ≤ 256K	.00339
256K < X < 1M	.00678

Bipolar SRAMs	C1
Up to 16K bits	.0052
16K < X ≤ 64K	.0105
64K < X ≤ 256K	.0210
256K < X < 1M	.0420

Bipolar PALs/PLAs	C1
Up to 200 gates	.01047
200 < X ≤ 1000 gates	.02094
1000 < X ≤ 2000 gates	.04188

MOS, BiMOS SRAMs	C1
Up to 16K bits	.0078
16K < X ≤ 64K	.0156
64K < X ≤ 256K	.0312
256K < X < 1M	.0624

Bipolar PROMs	C1
Up to 16K bits	.0094
16K < X ≤ 64K	.0188
64K < X ≤ 256K	.0376
256K < X < 1M	.0753

DRAMs	C1
Up to 16K bits	.0013
16K < X ≤ 64K	.0025
64K < X ≤ 256K	.0050
256K < X < 1M	.0100

MOS ROMs	C1
Up to 16K bits	.00065
16K < X ≤ 64K	.0013
64K < X ≤ 256K	.0026
256K < X < 1M	.0052

Table 5.1.2.4-2 A_1 Factor

Total Number Of Cycles (X)	FLOTOX	Textured-Poly
up to 100	.0007	.0097
100 < X ≤ 200	.0014	.0139
200 < X ≤ 500	.0034	.0230
500 < X ≤ 1K	.0068	.033
1K < X ≤ 3K	.0204	.061
3K < X ≤ 5K	.0341	.091
5K < X ≤ 7K	.0478	.136
7K < X ≤ 9K	.0614	.212
9K < X ≤ 10K	.0682	.303
10K < X ≤ 15K	.1023	.303
15K < X ≤ 20K	.1364	.303
20K < X ≤ 30K	.2045	.303
30K < X ≤ 50K	.3409	.303
50K < X ≤ 100K	.6818	.303
100K < X ≤ 200K	1.364	.303
200K < X ≤ 300K	2.045	.303
300K < X ≤ 325K	2.216	*
325K < X ≤ 350K	2.386	*
350K < X ≤ 400K	2.727	*
400K < X ≤ 450K	3.070	*
400K < X ≤ 500K	3.409	*

* - See Table 5.1.2.4-3

Table 5.1.2.4-3 A_2 Factor

For FLOTOX, $A_2 = 0$

For Tex - Poly:

Total # of Cycles	A_2*
Up to 300K	0.0
300K < X ≤ 325K	2.50
325K < X ≤ 350K	10.0
350K < X ≤ 400K	20.0
400K < X ≤ 450K	30.0
450K < X ≤ 500K	40.0

* If using a system life of other than 10000 hours, multiply A_2 by $\frac{10000}{\text{Sys. Life}}$.

If the EEPROM type is not known, assume FLOTOX

Table 5.1.2.4-4

B_1 for FLOTOX

T_j (°C)

Memory Capacity (bits)	20	30	40	50	60	70	80	90	100	110	120	130	140	150	160
	25	35	45	55	65	75	85	95	105	115	125	135	145	155	165
4k	.245	.298	.358	.425	.500	.582	.672	.770	.876	.989	1.111	1.240	1.376	1.521	1.672
	.270	.327	.391	.462	.540	.626	.720	.822	.932	1.049	1.174	1.307	1.448	1.596	1.750
8k	.343	.417	.501	.575	.699	.814	.940	1.077	1.225	1.384	1.553	1.734	1.925	2.126	2.338
	.378	.457	.546	.646	.755	.876	1.007	1.150	1.303	1.467	1.642	1.828	2.024	2.231	2.449
16k	.490	.596	.716	.851	1.000	1.165	1.345	1.540	1.752	1.979	2.221	2.480	2.753	3.041	3.344
	.541	.654	.782	.923	1.080	1.253	1.441	1.644	1.863	2.098	2.349	2.614	2.895	3.191	3.502
32k	.695	.845	1.015	1.206	1.418	1.651	1.907	2.184	2.484	2.806	3.150	3.516	3.903	4.312	4.742
	.767	.728	1.108	1.307	1.532	1.776	2.043	2.332	2.642	2.975	3.330	3.707	4.105	4.525	4.965
64k	.980	1.192	1.432	1.701	2.000	2.329	2.688	3.081	3.504	3.958	4.443	4.959	5.506	6.083	6.689
	1.082	1.308	1.563	1.847	2.161	2.506	2.881	3.288	3.727	4.196	4.697	5.228	5.790	6.382	7.003
128k	1.384	1.683	2.022	2.402	2.824	3.289	3.798	4.350	4.947	5.588	6.273	7.002	7.774	8.589	9.445
	1.528	1.848	2.207	2.608	3.051	3.538	4.068	4.643	5.262	5.925	6.632	7.383	8.176	9.012	9.888
256k	1.960	2.384	2.864	3.402	4.000	4.659	5.379	6.162	7.007	7.915	8.886	9.918	11.011	12.165	13.378
	2.165	2.617	3.126	3.694	4.322	5.011	5.762	6.576	7.453	8.392	9.394	10.457	11.581	12.764	14.006
512k	2.777	3.378	4.059	4.821	5.668	6.602	7.622	8.731	9.929	11.216	12.591	14.054	15.603	17.238	18.956
	3.068	3.708	4.430	5.234	6.124	7.101	8.165	9.319	10.561	11.892	13.311	14.817	16.410	18.087	19.846
1M	3.919	4.768	5.729	6.804	8.000	7.318	10.758	12.323	14.014	15.830	17.771	19.836	22.022	24.330	26.755
	4.330	5.234	6.252	7.387	8.643	10.022	11.525	13.153	14.906	16.785	18.788	20.914	23.162	25.529	28.012

Table 5.1.2.4-5

θ_j for TEX-POLY

T_j (°C)

Memory Capacity (bits)	20	30	40	50	60	70	80	90	100	110	120	130	140	150	160
	25	35	45	55	65	75	85	95	105	115	125	135	145	155	165
4k	.454	.531	.615	.706	.803	.907	1.018	1.135	1.257	1.386	1.521	1.660	1.805	1.955	2.110
	.491	.572	.659	.754	.854	.965	1.075	1.195	1.321	1.453	1.590	1.732	1.880	2.032	2.188
8k	.529	.619	.717	.823	.937	1.058	1.187	1.323	1.467	1.617	1.773	1.936	2.105	2.280	2.400
	.573	.667	.769	.879	.996	1.125	1.254	1.394	1.541	1.694	1.854	2.020	2.192	2.370	2.552
16k	.623	.729	.844	.968	1.102	1.245	1.397	1.557	1.726	1.903	2.087	2.279	2.478	2.684	2.896
	.675	.785	.905	1.034	1.173	1.324	1.476	1.640	1.814	1.994	2.182	2.378	2.580	2.789	3.004
32k	.730	.855	.990	1.136	1.293	1.460	1.638	1.827	2.024	2.232	2.448	2.673	2.906	3.147	3.396
	.791	.921	1.061	1.213	1.375	1.553	1.731	1.924	2.127	2.339	2.559	2.789	3.026	3.271	3.523
64k	.855	1.000	1.158	1.329	1.513	1.709	1.917	2.138	2.369	2.612	2.865	3.128	3.401	3.683	3.974
	.926	1.077	1.242	1.420	1.609	1.818	2.026	2.252	2.489	2.737	2.995	3.263	3.541	3.828	4.123
128k	1.031	1.206	1.397	1.603	1.825	2.061	2.312	2.578	2.857	3.150	3.455	3.773	4.102	4.442	4.793
	1.116	1.299	1.498	1.712	1.941	2.192	2.443	2.716	3.002	3.301	3.612	3.936	4.271	4.616	4.972
256k	1.246	1.457	1.688	1.937	2.204	2.490	2.794	3.115	3.452	3.805	4.174	4.556	4.956	5.367	5.791
	1.349	1.570	1.810	2.068	2.345	2.649	2.952	3.281	3.627	3.988	4.364	4.755	5.160	5.577	6.008
512k	1.505	1.761	2.059	2.341	2.664	3.010	3.376	3.764	4.172	4.599	5.045	5.508	5.989	6.486	6.998
	1.630	1.897	2.187	2.500	2.834	3.201	3.568	3.965	4.383	4.819	5.274	5.747	6.236	6.740	7.260
1M	1.815	2.123	2.459	2.822	3.212	3.628	4.071	4.538	5.330	5.544	6.082	6.641	7.221	7.820	8.437
	1.965	2.287	2.637	3.014	3.417	3.859	4.301	4.781	5.284	5.810	6.359	6.928	7.518	8.127	8.753

Table 5.1.2.4-6

B_2 for TEX-POLY (B_2 = 0 for FLOTOX)

T_j (°C)

Memory Capacity (bits)	20 / 25	30 / 35	40 / 45	50 / 55	60 / 65	70 / 75	80 / 85	90 / 95	100 / 105	110 / 115	120 / 125	130 / 135	140 / 145	150 / 155	160 / 165
4k	.608	.531	.468	.415	.372	.335	.303	.276	.253	.233	.215	.200	.186	.174	.163
	.567	.498	.440	.393	.353	.318	.289	.264	.243	.224	.207	.192	.180	.168	.158
8k	.709	.619	.546	.485	.434	.390	.354	322	.295	.272	.251	.233	.217	.202	.190
	.662	.580	.514	.458	.411	.371	.337	.308	.283	.260	.241	.224	.209	.196	.184
16k	.834	.729	.642	.570	.510	.460	.416	.379	.347	.320	.295	.274	.255	.238	.223
	.779	.683	.605	.539	.484	.437	.397	.363	.333	.307	.284	.580	.246	.231	.216
32k	.978	.855	.753	.669	.598	.539	.488	.445	.407	.375	.346	.321	.299	.278	.262
	.913	.801	.709	.632	.568	.513	.466	.425	.390	.360	.333	.310	.289	.280	.254
64k	1.145	1.000	.881	.783	.700	.631	.572	.521	.477	.439	.405	.376	.350	.327	.306
	1.069	.938	.830	.740	.664	.600	.545	.798	.457	.421	.390	.363	.338	.316	.970
128k	1.381	1.206	1.063	.944	.845	.761	.689	.628	.575	.489	.453	.422	.394	.394	.670
	1.289	1.131	1.001	.892	.801	.724	.657	.601	.551	.508	.470	.437	.408	.382	.358
256k	1.668	1.457	1.284	1.141	1.020	.919	.833	.759	.695	.639	.712	.548	.510	.476	.446
	1.557	1.366	1.209	1.078	.968	.874	.794	.726	.666	.614	.568	.528	.493	.461	.433
512k	2.016	1.761	1.552	1.378	1.233	1.111	1.006	.917	.839	.772	.714	.662	.616	.576	.540
	1.882	1.651	1.461	1.303	1.169	1.056	.960	.877	.805	.742	.687	.638	.595	.570	.523
1M	2.450	2.123	1.871	1.662	1.487	1.339	1.213	1.105	1.012	.931	.860	.798	.743	.694	.651
	2.269	1.991	1.761	1.570	1.410	1.274	1.157	1.057	.970	.894	.828	.770	.718	.672	.630

5.1.2.4.1 $\lambda_{TDDB}(t_O)$

For Bipolar memory devices, $\lambda_{TDDB} = 0$

For MOS/BiMOS memories:

1) Determine the following parameters of the device:
   Total gate oxide area in square microns (DRAMs, SRAMs, ROM/HAL/MLAs only)
   Total periphery circuitry gate oxide area in square microns (PROM/PAL/PLAs, EEPROMs, UVEPROMs only)
   Gate oxide electric field stress due to normal operating voltage (in MV/cm)
   Operating junction temperature of the device in degrees celsius

If these values cannot be derived, refer to the following tables in selecting values:

   Table 5.1.2.7-20 for gate oxide area
   Table 5.1.2.7-21 for gate oxide thickness

2) Once the parameters have been determined, find λ_{TDDB} by referring to Table 5.1.2.7-16.

Note that the λ_{TDDB} values are valid only for a 10000 hour assumed system lifetime.

5.1.2.5 Monolithic GaAs Digital Devices.

Includes small scale, medium scale, and large scale integrated circuits using MESFET transistors and gold based metallization.

Digital GaAs part failure rate model:

$$\lambda_D = \pi_Q [C_{1A} \pi_{TA} + C_{1P} \pi_{TP} + C_2 \pi_E] \pi_L \text{ (failures/}10^6\text{ hrs)}$$

where the C_1 factors are shown in Table 5.1.2.5-1.

λ_D = Digital GaAs Part Failure Rate in failures/10^6 hours
C_{1A} = Active Device Complexity Factor (For transistors and diodes)
C_{1P} = Passive Device Complexity Factor (For resistors, capacitors, and inductors)
π_{TA} = Active Device Temperature Acceleration Factor, Table 5.1.2.7-13
π_{TP} = Passive Device Temperature Acceleration Factor, Table 5.1.2.7-14
π_L = Learning Factor, Table 5.1.2.7-2
π_Q = Quality Factor, Table 5.1.2.7-1
C_2 = Package Complexity factor, Table 5.1.2.7-15
π_E = Environmental Factor, Table 5.1.2.7-3

Table 5.1.2.5-1: C_{1A} and C_{1P} FOR MONOLITHIC GaAs DIGITAL DEVICES

COMPLEXITY (NO. OF IC ELEMENTS)	C_{1A}	C_{1P}
1 - 1000 (SSI & MSI)	25.3	.687
1001 - 10,000 (LSI)	50.6	.687
Unknown	50.6	.687

5.1.2.6 Monolithic GaAs MMIC Devices.

Includes GaAs MMIC devices using MESFET transistors and gold based metallization.

GaAs MMIC part failure rate model:

$$\lambda_M = \pi_Q [(C_{1A} \pi_{TA} + C_{1P} \pi_{TP}) \pi_A + C_2 \pi_E] \pi_L \text{ (failures/}10^6\text{ hours)}$$

where the C_1 factors are shown in Table 5.1.2.6-1, the π_T factors are shown in Table 5.1.2.7-12 and 5.1.2.7-14, and the π_A factor is shown in Table 5.1.2.6-2. The π_Q, π_L and π_E factors are shown in Tables 5.1.2.7-1, 5.1.2.7-2 and 5.1.2.7-3. C_2 is shown in Table 5.1.2.7-15.

λ_M = MMIC GaAs Part Failure Rate
C_{1A} = GaAs Active Device Complexity Factor (For transistors and diodes)
C_{1P} = GaAs Passive Device Complexity Factor (For resistors, capacitors, inductors)
π_{TA} = GaAs Active Device Temperature Factor
π_{TP} = GaAs Passive Device Temperature Factor
π_A = MMIC Application Factor
π_L = Experience or Learning Factor
π_Q = Quality Factor
C_2 = Package Complexity Factor
π_E = Environmental Factor

Table 5.1.2.6-1: C_{1A} and C_{1P} FOR MONOLITHIC GaAs MMIC DEVICES

COMPLEXITY (NO. OF IC ELEMENTS)	C_{1A}	C_{1P}
1 - 10	4.51	2.26
11 - 100	4.51	2.71
101 - 1000	7.22	2.94
Unknown	7.22	2.94

Table 5.1.2.6-2
π_A FOR MONOLITHIC GaAs MMIC DEVICES

APPLICATION	π_A
Low noise & low power less than or equal to 100 mw	1.0
Driver & high power greater than 100 mw to 3000 mw	3.0
Unknown	3.0

5.1.2.7 Tables for Monolithic Model Parameters

Table 5.1.2.7-1

π_Q Quality Factors

QUALITY LEVEL	DESCRIPTION	π_Q
S	Procured in full accordance with MIL-M-38510, Class S requirements. Class S listing on QPL-38510.	0.7
B	Procured in full accordance with MIL-M-38510 Class B requirements. Class B listing on QPL-38510.	1.0
D	Parts with normal reliability screening and manufacturer's quality assurance practices. Burn-in per MIL-STD-883 Method 1015 (Series), Class B, and final electrical test required.	3.3
D-1	Commercial (or non-MIL standard) parts with no screening other than final electrical test at temperature extremes*	6.5
OTHER	Parts screened to intermediate quality levels per screening methods of MIL-STD-883. Screening factor and π_Q as determined below.	-

* Non-hermetic parts should be used only in controlled environments(G_B)

MIL-STD -883 METHOD	SCREEN	POINT VALUATION
5007	Wafer lot acceptance testing	0.5
2023	Non-destructive bond pull	0.2
2010/17	Internal visual examination	6.0
1008	Stabilization bare, condition B minimum	4.5
1010	Temperature cycling, condition B minimum	11.6
2001	Constant acceleration, condition B minimum	12.8
2020	PIND (particle impact noise detection)	11.3
1015	Burn-in (S-level/B-level)	16.3/10.9
5005	Final Electrical	10.9
1014	Seal Test (test conditions A, B or C)	7.3
2012	Radiography	11.3
2009	External visual inspection	7.3

Note 1: The screening factor is the sum of the point valuations of all MIL-STD-883 screens conducted on the parts in question.

Note 2: π_Q = 71.3 ÷ screening factor.

Table 5.1.2.7-2 Experience Factor π_L

YEARS IN PRODUCTION	π_L FACTOR
0	2.1
.25	1.9
.5	1.8
.75	1.6
1	1.5
2	1.05
3	0.67
4	0.52
5	0.37

$$\pi_L = [0.01 \exp (5.35 - 0.35 Y)]$$

where Y = no. years in production

Table 5.1.2.7-3 Application Environment Factor π_E

ENVIRONMENT	π_E
G_B	0.5
G_F	2.5
G_M	4.0
N_I	4.6
N_U	5.7
N_{UU}	6.3
N_{UL}	11.0
A_I	4.4
A_U	5.5
M_F	6.5
S_F	0.9
C_L	220

Table 5.1.2.7-4 Technology Temperature Factor Tables

TECHNOLOGY	EFFECTIVE ACTIVATION ENERGY	π_T TABLE NUMBER	A
ASTTL, CML, TTL, HTTL, FTTL, DTL, ECL & ASTTL	.4 ev	5.1.2.7-5	4635
LTTL & STTL	.45 ev	5.1.2.7-6	5214
LSTTL	.5 ev	5.1.2.7-7	5794
IIL, I3L, ISL & MNOS	.6 ev	5.1.2.7-8	6952
DIGITAL MOS	.35 ev	5.1.2.7-9	4060
MEMORIES (BIPOLAR & MOS)	.8 ev	5.1.2.7-10	9270
LINEAR (BIPOLAR & MOS)	.65 ev	5.1.2.7-11	7532
GaAs MMIC ACTIVE DEVICES	1.5 ev	5.1.2.7-12	17380
GaAs DIGITAL ACTIVE DEVICES	1.4 ev	5.1.2.7-13	16220
GaAs PASSIVE DEVICES	.43 ev	5.1.2.7-14	4980

NOTE 1. $\pi_T = 0.1\ (e^x)$ (5.1.2.7.3)

where

$$x = -A\left(\frac{1}{T_J + 273} - \frac{1}{298}\right) \text{ For Silicon Devices}$$

$$x = -A\left(\frac{1}{T_{CH} + 273} - \frac{1}{423}\right) \text{ For GaAs Devices}$$

A = value from above Table
T_J = device worst case junction temperature (°C)
T_{CH} = average active device channel temperature (°C)
e = natural logarithm base, 2.718

(Notes continued for Table 5.1.2.7-4)

NOTE 2. T_j, the worst case junction temperature, shall be measured or estimated using the following expression:

$$T_j = T_C + \Theta_{JC}P \qquad (5.1.2.7.4)$$

where:

T_C is case temperature (°C).

Θ_{JC} is junction to case thermal resistance (°C/watt) for a device soldered into a printed circuit board. If Θ_{JC} is not available, use a value contained in a specification for the closest equivalent device or use the Tables on pages 5.1.2.7-5 through 5.1.2.7-7.

P is the worst case power realized in a system application. If the applied power is not available, use the maximum power dissipation from the specification for the closest equivalent device.

If T_C cannot be determined, use the following:

ENVIRONMENT	A_U	A_I	N_U	N_I	N_{UU}	N_{UL}
T_C (°C)	76	60	80	45	25	40
ENVIRONMENT	M_F	S_F	G_B	G_M	G_F	C_L
T_C (°C)	50	35	35	50	45	45

Table 5.1.2.7-4a

θ_{JC} Values for MIL-M-38510 Devices (from MIL-M-38510G, Appendix C)

JAN P/N LETTER 1/	SPECIFICATION DESIGNATION OUTLINE NO. 1/	MAX θ_{JC} (°C/W) 3/, 4/	DESCRIPTION 5/
A	F-1	22	14-lead FP
B	F-3	22	14-lead FP
C	D-1	28	14-lead DIP
D	F-2	22	14-lead FP
	F-2A	22	14-lead FP
E	D-2	28	16-lead DIP
F	F-5	22	16-lead FP
	F-5A	22	16-lead FL
G	A-1	70	8-lead can
H	F-4	22	10-lead FP
I	A-2	65	10-lead can
J	D-3	28	24-lead DIP
K	F-6	22	24-lead FP
	F-6A	22	24-lead FP
L	D-9	28	24-lead DIP
M	A-3	65	12-lead can
P	D-4	28	8-lead DIP
Q	D-5	28	40-lead DIP
R	D-8	28	20-lead DIP
S	F-9	22	20-lead FP
	F-9A	22	20-lead FP
V	D-6	28	18-lead DIP
W	D-7	28	22-lead DIP
	F-8	22	24-lead FP
	F-10	22	18-lead FP
	F-11	22	28-lead FP
	F-11A	22	28-lead FP
	D-10	28	28-lead DIP
	D-11	28	24-lead DIP
	D-12	28	50-lead DIP
	D-13	28	64-lead DIP

See footnotes at end of table.

Table 5.1.2.7-4a (continued)

JAN P/N LETTER 1/	SPECIFICATION DESIGNATION OUTLINE NO. 1/	MAX Θ_{JC} (°C/W) 3/, 4/	DESCRIPTION 5/
	C-1	20	16-terminal SQ. LCC
	C-1A	20	16-terminal SQ. LCC
2	C-2	20	20-terminal SQ. LCC
	C-2A	20	20-terminal SQ. LCC
	C-3	20	24-terminal SQ. LCC
	C-3A	20	24-terminal SQ. LCC
3	C-4	20	28-terminal SQ. LCC
	C-4A	20	28-terminal SQ. LCC
	C-5	20	44-terminal SQ. LCC
	C-6	20	52-terminal SQ. LCC
	C-7	20	68-terminal SQ. LCC
	C-8	20	84-terminal SQ. LCC
	C-9	20	18-terminal RECT. LCC
	C-9A	20	18-terminal RECT. LCC
	C-10	20	18-terminal RECT. LCC
	C-11	20	28-terminal RECT. LCC
	C-11A	20	28-terminal RECT. LCC
	C-12	20	32-terminal RECT. LCC
	C-12A	20	32-terminal RECT. LCC
	C-13	20	20-terminal RECT. LCC
	C-13A	20	32-terminal RECT. LCC
	C-J1	20	44-terminal JCC
	C-J2	20	68-terminal JCC
	C-J3	20	84-terminal JCC
	C-J4	20	44-terminal JCC
	C-J5	20	68-terminal JCC
	C-J6	20	84-terminal JCC
	C-G1	20	44-terminal GCC
	C-G2	20	68-terminal GCC
	C-G3	20	84-terminal GCC
	C-G4	20	44-terminal GCC
	C-G5	20	68-terminal GCC
	C-G6	20	84-terminal GCC

See footnotes at end of table.

Table 5.1.2.7-4a (continued)

JAN P/N LETTER 1/	SPECIFICATION DESIGNATION OUTLINE NO. 1/	MAX θ_{JC} (°C/W) 3/, 4/	DESCRIPTION 5/
	P-AA	6	81-pin SQ PGA
	P-AB	6	100-pin SQ PGA
	P-AC	6	121-pin SQ PGA
	P-AD	6	144-pin SQ PGA
	P-AE	6	169-pin SQ PGA
	P-AF	6	196-pin SQ PGA
	P-AG	6	225-pin SQ PGA
	P-AH	6	256-pin SQ PGA
	P-AJ	6	289-pin SQ PGA
	P-AK	6	324-pin SQ PGA
	P-AL	6	361-pin SQ PGA
	P-AM	6	400-pin SQ PGA
	P-BA	6	81-pin SQ PGA
	P-BB	6	100-pin SQ PGA
	P-BC	6	121-pin SQ PGA
	P-BD	6	144-pin SQ PGA
	P-BE	6	169-pin SQ PGA
	P-BF	6	196-pin SQ PGA
	P-BG	6	225-pin SQ PGA
	P-BH	6	256-pin SQ PGA
	P-BJ	6	289-pin SQ PGA
	P-BK	6	324-pin SQ PGA
	P-BL	6	361-pin SQ PGA
	P-BM	6	400-pin SQ PGA

1/ The letters in this column may be alphabetic or numeric and are used in paragraph 1.2.3 of detail specifications and are dedicated to specific case outlines. Where there are no letters, the letters S, Y, Z, U, T and N are used (in the order shown) but are not dedicated until they appear in the detail specification. Thus a letter X, for example, can be used to label more than one type of case outline provided each application is in a different detail specification.

Notes to Table 5.1.2.7-4a

2/ The chip carrier case outline drawing describes features which are optional. These options enhance the utility of the chip carrier, not only for end use but also for manufacturing and testing. Specific case outline configurations are designated by a single letter which is used in the JAN part no. The following excerpt from a typical detail specification shows how the option is added.

3/ Values shown are worst case (MEAN + 2σ) for 60 x 60 mil die and applicable for devices with die sizes up to 14400 sq. mil.

4/ For devices die sizes greater than 14400 sq. mil. use the following values:

Dual-in-line	11°C/W
Flat pack	10°C/W
Chip carrier	10°C/W
Pin grid array	3°C/W

5/ LCC = Leadless chip carrier, ceramic; GCC = Gullwing leaded chip carrier, ceramic; JCC = J bend loaded chip carrier, ceramic; PGA = Pin grid array, ceramic; FP = Flat pack; DIP = Dual-in-line package.

6/ Caution: Some outline configurations listed in this column are prohibited for new equipment design or redesign on and after 29 November 1986 (see 3.5.1 and case outline drawings and notes).

Table 5.1.2.7-5 π_T vs Junction Temperature for ASTTL, CML, TTL, HTTL, FTTL, DTL, ECL & ALSTTL

T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T
25	.10	65	.63	105	2.69	145	8.69
30	.13	70	.77	110	3.16	150	9.91
35	.17	75	.93	115	3.69	155	11.26
40	.21	80	1.13	120	4.29	160	12.77
45	.27	85	1.36	125	4.98	165	14.42
50	.33	90	1.62	130	5.75	170	16.25
55	.41	95	1.93	135	6.62	175	18.27
60	.51	100	2.28	140	7.60		

Table 5.1.2.7-6 π_T vs Junction Temperature for LTTL & STTL

T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T
25	.10	65	.79	105	4.06	145	15.19
30	.13	70	.99	110	4.86	150	17.60
35	.18	75	1.24	115	5.79	155	20.32
40	.23	80	1.53	120	6.87	160	23.39
45	.30	85	1.88	125	8.11	165	26.84
50	.39	90	2.29	130	9.55	170	30.70
55	.50	95	2.79	135	11.19	175	35.01
60	.63	100	3.37	140	13.06		

Table 5.1.2.7-7 π_T vs Junction Temperature for LSTTL

T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T
25	.10	65	1.00	105	6.12	145	26.55
30	.14	70	1.28	110	7.48	150	31.28
35	.19	75	1.63	115	9.09	155	36.71
40	.25	80	2.07	120	10.99	160	42.92
45	.34	85	2.60	125	13.23	165	50.00
50	.45	90	3.25	130	15.85	170	58.05
55	.59	95	4.04	135	18.90	175	67.18
60	.77	100	4.99	140	22.45		

Table 5.1.2.7-8 π_T vs Junction Temperature for IIL, I^3L, ISL & MNOS

T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T
25	.10	65	1.58	105	13.94	145	81.02
30	.15	70	2.13	110	17.72	150	98.6
35	.21	75	2.86	115	22.39	155	119.5
40	.31	80	3.79	120	28.13	160	144.1
45	.43	85	4.99	125	35.13	165	173.1
50	.61	90	6.52	130	43.63	170	207.1
55	.84	95	8.46	135	53.90	175	246.8
60	1.16	100	10.89	140	66.24		

Table 5.1.2.7-9 π_T vs Junction Temperature for MOS Digital Gate/Logic Array and MOS Digital Microprocessor Devices

T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T
25	.10	65	.50	105	1.79	145	5.00
30	.13	70	.60	110	2.06	150	5.60
35	.16	75	.71	115	2.36	155	6.27
40	.19	80	.84	120	2.69	160	6.99
45	.24	85	.98	125	3.07	165	7.78
50	.29	90	1.15	130	3.48	170	8.64
55	.35	95	1.34	135	3.94	175	9.57
60	.42	100	1.55	140	4.44		

Table 5.1.2.7-10 π_T vs Junction Temperature for Memories, Bipolar, MOS & BIMOS

T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T
25	.10	65	3.97	105	72.31	145	755.8
30	.17	70	5.92	110	99.6	150	982
35	.27	75	8.73	115	136.1	155	1269
40	.44	80	12.73	120	184.4	160	1629
45	.71	85	18.37	125	248.0	165	2081
50	1.11	90	26.25	130	331.1	170	2642
55	1.72	95	37.14	135	438.9	175	3337
60	2.63	100	52.05	140	577.8		

Table 5.1.2.7-11 π_T vs Junction Temperature for Linear

T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T
25	.10	65	1.99	105	21.04	145	141.7
30	.15	70	2.75	110	27.30	150	175.3
35	.23	75	3.78	115	35.17	155	215.8
40	.34	80	5.13	120	45.02	160	264.5
45	.49	85	6.91	125	57.28	165	322.5
50	.71	90	9.24	130	72.44	170	391.6
55	1.01	95	12.25	135	91.09	175	473.5
60	1.42	100	16.11	140	113.9		

Table 5.1.2.7-12 π_T vs Channel Temperature for GaAs MMIC Active Devices

T_{CH}(°C)	π_T	T_{CH}(°C)	π_T	T_{CH}(°C)	π_T	T_{CH}(°C)	π_T
25	3.274E-9	65	3.255E-6	105	7.511E-4	145	6.117E-2
30	8.571E-9	70	6.888E-6	110	1.369E-3	150	1.000E-1
35	2.175E-8	75	1.427E-5	115	2.457E-3	155	1.616E-1
40	5.357E-8	80	2.894E-5	120	4.344E-3	160	2.583E-1
45	1.283E-7	85	5.756E-5	125	7.571E-3	165	4.084E-1
50	2.989E-7	90	1.123E-4	130	1.301E-2	170	6.391E-1
55	6.788E-7	95	2.153E-4	135	2.208E-2	175	9.903E-1
60	1.504E-6	100	4.055E-4	140	3.698E-2		

Table 5.1.2.7-13 π_T vs Channel Temperature for GaAs Digital Active Devices

T_{CH}(°C)	π_T	T_{CH}(°C)	π_T	T_{CH}(°C)	π_T	T_{CH}(°C)	π_T
25	1.034E-8	65	6.488E-6	105	1.041E-3	145	6.321E-2
30	2.539E-8	70	1.306E-5	110	1.823E-3	150	1.000E-1
35	6.055E-8	75	2.576E-5	115	3.146E-3	155	1.565E-1
40	1.404E-7	80	4.985E-5	120	5.355E-3	160	2.424E-1
45	3.172E-7	85	9.471E-5	125	8.994E-3	165	3.718E-1
50	6.986E-7	90	1.768E-4	130	1.491E-2	170	5.647E-1
55	1.502E-6	95	3.244E-4	135	2.442E-2	175	8.498E-1
60	3.156E-6	100	5.857E-4	140	3.952E-2		

Table 5.1.2.7-14 π_T vs Junction Temperature for GaAs Passive Devices

T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T	T_J(°C)	π_T
25	7.166E-4	65	5.178E-3	105	2.462E-2	145	8.686E-2
30	9.442E-4	70	6.419E-3	110	2.924E-2	150	1.000E-1
35	1.233E-3	75	7.908E-3	115	3.458E-2	155	1.147E-1
40	1.596E-3	80	9.685E-3	120	4.071E-2	160	1.312E-1
45	2.050E-3	85	1.179E-2	125	4.773E-2	165	1.497E-1
50	2.612E-3	90	1.429E-2	130	5.575E-2	170	1.702E-1
55	3.305E-3	95	1.721E-2	135	6.487E-2	175	1.929E-1
60	4.151E-3	100	2.064E-2	140	7.520E-2		

Table 5.1.2.7-15 C_2, Package Complexity Failure Rates in Failures Per 10^6 Hours

	PACKAGE TYPE*				
Number of Functional Pins	Hermetic DIPs w/Solder or Weld Seal Leadless Chip Carriers (LCC) Pin Grid Array (PGA)	Hermetic DIPs with Glass Seal	Nonhermetic DIPs	Hermetic Flatpacks with Axial Leads on 50 Mil Centers	Hermetic Cans
3	---	---	---	---	0.0003
4	---	---	---	0.0004	0.0005
6	0.0019	0.0013	0.0018	0.0008	0.0011
8	0.0026	0.0021	0.0026	0.0013	0.0020
10	0.0034	0.0029	0.0034	0.0020	0.0031
12	0.0041	0.0038	0.0043	0.0028	0.0044
14	0.0048	0.0048	0.0051	0.0037	0.0060
16	0.0056	0.0059	0.0061	0.0047	0.0079
18	0.0064	0.0071	0.0070	0.0058	---
22	0.008	0.010	0.009	0.008	---
24	0.009	0.011	0.010	0.010	---
28	0.010	0.014	0.012	---	---
36	0.013	0.020	0.016	---	---
40	0.015	0.024	0.019	---	---
64	0.025	0.048	0.033	---	---
80	0.032	---	---	---	---
128	0.053	---	---	---	---
180	0.076	---	---	---	---
224	0.097	---	---	---	---
525	0.243	---	---	---	---

*If seal type for hermetic DIP is unknown, assume glass seal.

The tabulated values are determined by the following equations:

Hermetic DIPs with solder or weld seals, Leadless Chip Carrier (LCC) & PGAs.	$C_2 = 2.8 \times 10^{-4}(N_p)^{1.08}$	(5.1.2.7.5)
Hermetic DIPs with glass seals	$C_2 = 9.0 \times 10^{-5}(N_p)^{1.51}$	(5.1.2.7.6)
Nonhermetic DIPs	$C_2 = 2.8 \times 10^{-4}(N_p)^{1.23}$	(5.1.2.7.7)
Hermetic Flatpacks	$C_2 = 3.0 \times 10^{-5}(N_p)^{1.82}$	(5.1.2.7.8)
Hermetic Cans	$C_2 = 3.0 \times 10^{-5}(N_p)^{2.01}$	(5.1.2.7.9)

where: N_p is the number of pins on a device package which are connected to some substrate location.

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.017	.787	11.137	62.658
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.051	1.717	18.622	87.556
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.002	.136	3.396	29.040	117.243
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.005	.325	6.164	42.720	151.579
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.015	.708	10.380	59.862	190.339
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.039	1.412	16.386	80.542	233.252
30.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.093	2.610	24.477	104.743	280.018
35.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.003	.205	4.504	34.873	132.372	330.328
40.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.007	.419	7.314	47.724	163.284	383.873
45.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.017	.800	11.259	63.104	197.301	440.353
50.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.040	1.432	16.539	81.029	234.226	499.480
55.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.084	2.423	23.320	101.463	273.850	560.985
60.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.002	.166	3.894	31.733	124.333	315.965	624.611
65.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.005	.311	5.974	41.864	149.537	360.363	690.121
70.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.010	.552	8.793	53.763	176.958	406.845	757.294
75.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.022	.934	12.474	67.442	206.466	455.217	825.928
80.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.043	1.510	17.123	82.887	237.924	505.299	895.833
85.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.080	2.346	22.831	100.059	271.195	556.917	966.834
90.	.000	.000	.000	.000	.000	.000	.000	.000	.002	.143	3.509	29.664	118.903	306.143	609.913	999.000
95.	.000	.000	.000	.000	.000	.000	.000	.000	.003	.244	5.074	37.669	139.349	342.634	664.134	999.000
100.	.000	.000	.000	.000	.000	.000	.000	.000	.007	.402	7.114	46.873	161.319	380.540	719.441	999.000
105.	.000	.000	.000	.000	.000	.000	.000	.000	.013	.639	9.698	57.284	184.732	419.737	775.705	999.000
110.	.000	.000	.000	.000	.000	.000	.000	.000	.023	.981	12.890	68.895	209.499	460.109	832.804	999.000
115.	.000	.000	.000	.000	.000	.000	.000	.000	.041	1.460	16.745	81.686	235.535	501.543	890.627	999.000
120.	.000	.000	.000	.000	.000	.000	.000	.001	.069	2.110	21.307	95.627	262.753	543.936	949.070	999.000
125.	.000	.000	.000	.000	.000	.000	.000	.001	.112	2.969	26.613	110.679	291.066	587.190	999.000	999.000
130.	.000	.000	.000	.000	.000	.000	.000	.002	.177	4.076	32.687	126.799	320.394	631.212	999.000	999.000
135.	.000	.000	.000	.000	.000	.000	.000	.004	.273	5.470	39.543	143.938	350.655	675.917	999.000	999.000
140.	.000	.000	.000	.000	.000	.000	.000	.007	.408	7.188	47.187	162.046	381.773	721.225	999.000	999.000
145.	.000	.000	.000	.000	.000	.000	.000	.012	.597	9.266	55.617	181.068	413.676	767.061	999.000	999.000
150.	.000	.000	.000	.000	.000	.000	.000	.019	.851	11.736	64.824	200.954	446.294	813.355	999.000	999.000
155.	.000	.000	.000	.000	.000	.000	.000	.030	1.188	14.626	74.794	221.649	479.561	860.043	999.000	999.000
160.	.000	.000	.000	.000	.000	.000	.000	.047	1.624	17.959	85.506	243.102	513.416	907.065	999.000	999.000
165.	.000	.000	.000	.000	.000	.000	.001	.072	2.178	21.755	96.938	265.261	547.800	954.364	999.000	999.000
170.	.000	.000	.000	.000	.000	.000	.001	.106	2.869	26.027	109.065	288.076	582.659	999.000	999.000	999.000
175.	.000	.000	.000	.000	.000	.000	.002	.155	3.716	30.785	121.858	311.501	617.940	999.000	999.000	999.000

TABLE 5.1.2.7-16 TDDB: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 4.00 LOG SQUARE MICRONS

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.005	.262	4.607	32.157	117.543
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.015	.601	8.171	47.032	152.364
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.042	1.252	13.463	65.532	191.676
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.104	2.399	20.826	87.701	235.185
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.004	.234	4.261	30.533	113.486	282.572
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.012	.488	7.082	42.774	142.762	333.508
30.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.028	.942	11.105	57.656	175.354	387.668
35.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.064	1.703	16.553	75.211	211.060	444.739
40.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.002	.135	2.895	23.610	95.412	249.661	504.420
45.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.005	.266	4.663	32.418	118.188	290.931	566.431
50.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.012	.495	7.156	43.068	143.433	334.648	630.509
55.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.025	.870	10.517	55.609	171.019	380.592	696.408
60.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.051	1.453	14.880	70.049	200.806	428.554	763.905
65.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.099	2.318	20.354	86.364	232.644	478.335	832.790
70.	.000	.000	.000	.000	.000	.000	.000	.000	.003	.180	3.547	27.027	104.506	266.384	529.747	902.873
75.	.000	.000	.000	.000	.000	.000	.000	.000	.006	.314	5.225	34.961	124.408	301.876	582.614	973.977
80.	.000	.000	.000	.000	.000	.000	.000	.000	.013	.524	7.439	44.192	145.988	338.975	636.773	999.000
85.	.000	.000	.000	.000	.000	.000	.000	.000	.024	.840	10.269	54.735	169.157	377.541	692.072	999.000
90.	.000	.000	.000	.000	.000	.000	.000	.000	.044	1.298	13.789	66.586	193.820	417.439	748.368	999.000
95.	.000	.000	.000	.000	.000	.000	.000	.001	.077	1.939	18.061	79.723	219.881	458.543	805.533	999.000
100.	.000	.000	.000	.000	.000	.000	.000	.002	.129	2.808	23.134	94.113	247.242	500.733	863.445	999.000
105.	.000	.000	.000	.000	.000	.000	.000	.004	.210	3.952	29.045	109.714	275.808	543.897	921.993	999.000
110.	.000	.000	.000	.000	.000	.000	.000	.007	.331	5.419	35.818	126.473	305.484	587.928	981.075	999.000
115.	.000	.000	.000	.000	.000	.000	.000	.012	.505	7.255	43.465	144.337	336.181	632.730	999.000	999.000
120.	.000	.000	.000	.000	.000	.000	.000	.021	.749	9.503	51.989	163.247	367.813	678.210	999.000	999.000
125.	.000	.000	.000	.000	.000	.000	.000	.034	1.083	12.202	61.381	183.142	400.296	724.284	999.000	999.000
130.	.000	.000	.000	.000	.000	.000	.001	.055	1.527	15.385	71.628	203.962	433.553	770.873	999.000	999.000
135.	.000	.000	.000	.000	.000	.000	.001	.086	2.105	19.081	82.707	225.647	467.510	817.903	999.000	999.000
140.	.000	.000	.000	.000	.000	.000	.002	.131	2.840	23.310	94.593	248.137	502.097	865.306	999.000	999.000
145.	.000	.000	.000	.000	.000	.000	.003	.196	3.758	28.087	107.256	271.374	537.250	913.020	999.000	999.000
150.	.000	.000	.000	.000	.000	.000	.006	.285	4.883	33.423	120.663	295.302	572.906	960.986	999.000	999.000
155.	.000	.000	.000	.000	.000	.000	.009	.405	6.238	39.322	134.780	319.867	609.008	999.000	999.000	999.000
160.	.000	.000	.000	.000	.000	.000	.014	.566	7.846	45.782	149.571	345.019	645.503	999.000	999.000	999.000
165.	.000	.000	.000	.000	.000	.000	.022	.775	9.727	52.800	165.001	370.707	682.340	999.000	999.000	999.000
170.	.000	.000	.000	.000	.000	.000	.033	1.043	11.900	60.366	181.031	396.884	719.473	999.000	999.000	999.000
175.	.000	.000	.000	.000	.000	.001	.048	1.381	14.379	68.468	197.628	423.507	756.858	999.000	999.000	999.000

TABLE 5.1.2.7-16 (CONT) TDDB: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 4.50 LOG SQUARE MICRONS

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.004	.188	3.057	21.672	82.806	212.505
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.013	.417	5.411	32.033	108.537	258.653
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.033	.851	8.938	45.128	137.940	308.569
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.078	1.606	13.908	61.054	170.827	361.898
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.004	.169	2.830	20.552	79.831	206.974	418.299
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.010	.341	4.690	29.050	101.409	246.139	477.445
30.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.023	.645	7.362	39.528	125.692	288.077	539.028
35.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.049	1.148	11.016	52.053	152.552	332.541	602.763
40.	.000	.000	.000	.000	.000	.000	.000	.000	.002	.100	1.932	15.804	66.644	181.836	379.291	668.385
45.	.000	.000	.000	.000	.000	.000	.000	.000	.005	.191	3.094	21.852	83.279	213.381	428.101	735.648
50.	.000	.000	.000	.000	.000	.000	.000	.000	.010	.346	4.738	29.256	101.907	247.020	478.754	804.329
55.	.000	.000	.000	.000	.000	.000	.000	.000	.020	.597	6.970	38.079	122.449	282.583	531.049	874.223
60.	.000	.000	.000	.000	.000	.000	.000	.001	.040	.983	9.889	48.354	144.814	319.906	584.796	945.141
65.	.000	.000	.000	.000	.000	.000	.000	.001	.074	1.553	13.587	60.087	168.897	358.829	639.820	999.000
70.	.000	.000	.000	.000	.000	.000	.000	.003	.131	2.360	18.141	73.264	194.591	399.200	695.961	999.000
75.	.000	.000	.000	.000	.000	.000	.000	.006	.223	3.464	23.612	87.851	221.782	440.874	753.068	999.000
80.	.000	.000	.000	.000	.000	.000	.000	.011	.366	4.926	30.042	103.801	250.360	483.717	811.004	999.000
85.	.000	.000	.000	.000	.000	.000	.000	.020	.577	6.805	37.461	121.056	280.215	527.602	869.644	999.000
90.	.000	.000	.000	.000	.000	.000	.001	.034	.881	9.157	45.880	139.553	311.240	572.408	928.872	999.000
95.	.000	.000	.000	.000	.000	.000	.001	.058	1.303	12.034	55.297	159.223	343.333	618.028	988.580	999.000
100.	.000	.000	.000	.000	.000	.000	.002	.096	1.875	15.479	65.700	179.994	376.396	664.358	999.000	999.000
105.	.000	.000	.000	.000	.000	.000	.003	.152	2.627	19.527	77.069	201.796	410.338	711.303	999.000	999.000
110.	.000	.000	.000	.000	.000	.000	.006	.235	3.592	24.206	89.372	224.555	445.072	758.776	999.000	999.000
115.	.000	.000	.000	.000	.000	.000	.010	.353	4.804	29.534	102.577	248.203	480.514	806.697	999.000	999.000
120.	.000	.000	.000	.000	.000	.000	.017	.517	6.295	35.522	116.643	272.671	516.589	854.991	999.000	999.000
125.	.000	.000	.000	.000	.000	.000	.027	.738	8.094	42.173	131.530	297.893	553.225	903.589	999.000	999.000
130.	.000	.000	.000	.000	.000	.001	.043	1.032	10.229	49.484	147.194	323.806	590.354	952.427	999.000	999.000
135.	.000	.000	.000	.000	.000	.001	.065	1.412	12.724	57.447	163.590	350.350	627.915	999.000	999.000	999.000
140.	.000	.000	.000	.000	.000	.002	.097	1.896	15.599	66.049	180.675	377.468	665.848	999.000	999.000	999.000
145.	.000	.000	.000	.000	.000	.003	.142	2.499	18.869	75.272	198.404	405.105	704.101	999.000	999.000	999.000
150.	.000	.000	.000	.000	.000	.005	.203	3.239	22.547	85.097	216.734	433.210	742.624	999.000	999.000	999.000
155.	.000	.000	.000	.000	.000	.008	.286	4.132	26.642	95.502	235.623	461.735	781.369	999.000	999.000	999.000
160.	.000	.000	.000	.000	.000	.012	.394	5.195	31.157	106.462	255.029	490.636	820.294	999.000	999.000	999.000
165.	.000	.000	.000	.000	.000	.018	.534	6.444	36.094	117.952	274.916	519.869	859.359	999.000	999.000	999.000
170.	.000	.000	.000	.000	.000	.026	.712	7.892	41.451	129.947	295.240	549.395	898.528	999.000	999.000	999.000
175.	.000	.000	.000	.000	.001	.037	.935	9.552	47.223	142.419	315.969	579.176	937.765	999.000	999.000	999.000

TABLE 5.1.2.7-16 (CONT) TDDB: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 5.00 LOG SQUARE MICRONS

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.010	.274	3.328	20.130	71.661	178.761	355.080
5.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.026	.557	5.593	29.041	93.004	216.742	412.079
10.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.059	1.052	8.859	40.148	117.308	257.813	471.877
15.	.000	.000	.000	.000	.000	.000	.000	.000	.004	.125	1.861	13.323	53.525	144.432	301.693	534.139
20.	.000	.000	.000	.000	.000	.000	.000	.000	.009	.249	3.103	19.156	69.187	174.207	348.112	598.556
25.	.000	.000	.000	.000	.000	.000	.000	.000	.020	.466	4.909	26.490	87.100	206.445	396.806	664.843
30.	.000	.000	.000	.000	.000	.000	.000	.001	.042	.822	7.413	35.414	107.192	240.953	447.529	732.740
35.	.000	.000	.000	.000	.000	.000	.000	.002	.084	1.376	10.739	45.978	129.365	277.537	500.047	802.009
40.	.000	.000	.000	.000	.000	.000	.000	.005	.157	2.198	15.000	58.197	153.504	316.007	554.145	872.432
45.	.000	.000	.000	.000	.000	.000	.000	.010	.278	3.364	20.286	72.055	179.482	356.181	609.624	943.814
50.	.000	.000	.000	.000	.000	.000	.000	.021	.472	4.956	26.666	87.512	207.169	397.885	666.298	999.000
55.	.000	.000	.000	.000	.000	.000	.001	.039	.767	7.050	34.185	104.511	236.432	440.955	723.999	999.000
60.	.000	.000	.000	.000	.000	.000	.002	.070	1.198	9.723	42.867	122.981	267.141	485.239	782.574	999.000
65.	.000	.000	.000	.000	.000	.000	.004	.120	1.805	13.039	52.716	142.842	299.168	530.594	841.880	999.000
70.	.000	.000	.000	.000	.000	.000	.007	.200	2.633	17.053	63.720	164.010	332.391	576.886	901.788	999.000
75.	.000	.000	.000	.000	.000	.000	.012	.320	3.727	21.810	75.854	186.398	366.696	623.995	962.181	999.000
80.	.000	.000	.000	.000	.000	.000	.022	.495	5.134	27.339	89.082	209.918	401.972	671.807	999.000	999.000
85.	.000	.000	.000	.000	.000	.001	.037	.744	6.897	33.661	103.360	234.484	438.116	720.219	999.000	999.000
90.	.000	.000	.000	.000	.000	.002	.061	1.085	9.058	40.782	118.639	260.010	475.031	769.134	999.000	999.000
95.	.000	.000	.000	.000	.000	.003	.098	1.542	11.653	48.702	134.867	286.416	512.629	818.466	999.000	999.000
100.	.000	.000	.000	.000	.000	.005	.151	2.139	14.714	57.409	151.987	313.624	550.825	868.134	999.000	999.000
105.	.000	.000	.000	.000	.000	.008	.228	2.901	18.264	66.889	169.943	341.559	589.541	918.065	999.000	999.000
110.	.000	.000	.000	.000	.000	.013	.334	3.852	22.323	77.117	188.681	370.151	628.705	968.190	999.000	999.000
115.	.000	.000	.000	.000	.000	.021	.480	5.018	26.904	88.068	208.143	399.334	668.252	999.000	999.000	999.000
120.	.000	.000	.000	.000	.001	.033	.674	6.423	32.013	99.711	228.277	429.045	708.119	999.000	999.000	999.000
125.	.000	.000	.000	.000	.001	.050	.927	8.087	37.652	112.015	249.029	459.225	748.251	999.000	999.000	999.000
130.	.000	.000	.000	.000	.002	.074	1.251	10.030	43.818	124.945	270.350	489.820	788.593	999.000	999.000	999.000
135.	.000	.000	.000	.000	.003	.107	1.658	12.270	50.504	138.468	292.191	520.779	829.100	999.000	999.000	999.000
140.	.000	.000	.000	.000	.005	.153	2.161	14.819	57.700	152.548	314.506	552.054	869.725	999.000	999.000	999.000
145.	.000	.000	.000	.000	.007	.214	2.773	17.690	65.393	167.151	337.252	583.601	910.429	999.000	999.000	999.000
150.	.000	.000	.000	.000	.011	.294	3.507	20.889	73.566	182.243	360.386	615.378	951.174	999.000	999.000	999.000
155.	.000	.000	.000	.000	.017	.398	4.375	24.422	82.203	197.790	383.871	647.348	991.925	999.000	999.000	999.000
160.	.000	.000	.000	.000	.024	.529	5.390	28.292	91.285	213.760	407.669	679.475	999.000	999.000	999.000	999.000
165.	.000	.000	.000	.001	.034	.694	6.562	32.499	100.793	230.122	431.746	711.726	999.000	999.000	999.000	999.000
170.	.000	.000	.000	.001	.048	.898	7.901	37.042	110.707	246.846	456.069	744.071	999.000	999.000	999.000	999.000
175.	.000	.000	.000	.002	.066	1.146	9.417	41.915	121.005	263.902	480.608	776.481	999.000	999.000	999.000	999.000

TABLE 5.1.2.7-16 (CONT) TDDB: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 5.50 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm)															
	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.001	.031	.518	4.488	22.021	69.887	164.147	315.649	530.680
5.	.000	.000	.000	.000	.000	.000	.000	.002	.068	.953	7.071	30.629	88.977	197.008	364.242	596.104
10.	.000	.000	.000	.000	.000	.000	.000	.006	.138	1.651	10.604	41.088	110.476	232.371	415.106	663.388
15.	.000	.000	.000	.000	.000	.000	.000	.013	.265	2.705	15.230	53.433	134.262	270.008	467.969	732.251
20.	.000	.000	.000	.000	.000	.000	.001	.028	.477	4.222	21.064	67.657	160.193	309.700	522.581	802.438
25.	.000	.000	.000	.000	.000	.000	.002	.056	.817	6.306	28.189	83.719	188.116	351.234	578.709	873.720
30.	.000	.000	.000	.000	.000	.000	.004	.105	1.333	9.061	36.659	101.553	217.872	394.408	636.140	945.889
35.	.000	.000	.000	.000	.000	.000	.009	.188	2.082	12.575	46.496	121.072	249.305	439.035	694.682	999.000
40.	.000	.000	.000	.000	.000	.000	.017	.320	3.127	16.927	57.698	142.180	282.259	484.939	754.156	999.000
45.	.000	.000	.000	.000	.000	.001	.032	.525	4.531	22.174	70.242	164.772	316.589	531.957	814.403	999.000
50.	.000	.000	.000	.000	.000	.002	.057	.826	6.359	28.358	84.087	188.742	352.152	579.940	875.275	999.000
55.	.000	.000	.000	.000	.000	.004	.097	1.255	8.669	35.503	99.183	213.981	388.817	628.750	936.642	999.000
60.	.000	.000	.000	.000	.000	.007	.160	1.846	11.514	43.616	115.467	240.383	426.459	678.261	998.382	999.000
65.	.000	.000	.000	.000	.000	.013	.256	2.635	14.940	52.692	132.873	267.845	464.961	728.359	999.000	999.000
70.	.000	.000	.000	.000	.001	.022	.395	3.659	18.981	62.714	151.331	296.270	504.218	778.937	999.000	999.000
75.	.000	.000	.000	.000	.001	.037	.591	4.955	23.664	73.657	170.769	325.562	544.129	829.900	999.000	999.000
80.	.000	.000	.000	.000	.002	.060	.861	6.559	29.003	85.486	191.117	355.634	584.602	881.160	999.000	999.000
85.	.000	.000	.000	.000	.004	.094	1.223	8.503	35.008	98.164	212.303	386.401	625.553	932.638	999.000	999.000
90.	.000	.000	.000	.000	.006	.143	1.695	10.815	41.678	111.648	234.259	417.786	666.904	984.262	999.000	999.000
95.	.000	.000	.000	.000	.010	.214	2.299	13.521	49.007	125.894	256.919	449.716	708.584	999.000	999.000	999.000
100.	.000	.000	.000	.000	.016	.311	3.054	16.638	56.980	140.857	280.221	482.122	750.527	999.000	999.000	999.000
105.	.000	.000	.000	.001	.025	.442	3.981	20.182	65.582	156.490	304.104	514.942	792.674	999.000	999.000	999.000
110.	.000	.000	.000	.001	.039	.615	5.100	24.163	74.791	172.747	328.510	548.117	834.969	999.000	999.000	999.000
115.	.000	.000	.000	.002	.058	.839	6.429	28.586	84.582	189.583	353.387	581.594	877.363	999.000	999.000	999.000
120.	.000	.000	.000	.003	.084	1.123	7.986	33.452	94.932	206.955	378.683	615.321	919.810	999.000	999.000	999.000
125.	.000	.000	.000	.005	.120	1.479	9.784	38.757	105.811	224.820	404.352	649.253	962.268	999.000	999.000	999.000
130.	.000	.000	.000	.008	.168	1.917	11.837	44.498	117.192	243.138	430.349	683.348	999.000	999.000	999.000	999.000
135.	.000	.000	.000	.011	.232	2.447	14.154	50.664	129.047	261.868	456.633	717.566	999.000	999.000	999.000	999.000
140.	.000	.000	.000	.017	.314	3.081	16.745	57.245	141.346	280.975	483.165	751.871	999.000	999.000	999.000	999.000
145.	.000	.000	.001	.024	.419	3.827	19.613	64.229	154.062	300.423	509.909	786.230	999.000	999.000	999.000	999.000
150.	.000	.000	.001	.034	.551	4.698	22.764	71.601	167.167	320.178	536.831	820.613	999.000	999.000	999.000	999.000
155.	.000	.000	.002	.047	.713	5.701	26.198	79.346	180.633	340.209	563.901	854.992	999.000	999.000	999.000	999.000
160.	.000	.000	.002	.064	.912	6.845	29.915	87.448	194.434	360.487	591.090	889.341	999.000	999.000	999.000	999.000
165.	.000	.000	.003	.087	1.152	8.138	33.912	95.891	208.546	380.982	618.371	923.637	999.000	999.000	999.000	999.000
170.	.000	.000	.005	.116	1.439	9.585	38.186	104.657	222.943	401.670	645.720	957.858	999.000	999.000	999.000	999.000
175.	.000	.000	.007	.152	1.777	11.194	42.732	113.730	237.602	422.524	673.113	991.984	999.000	999.000	999.000	999.000

TABLE 5.1.2.7-16 (CONT) TDDB: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 6.00 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm) 2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.004	.081	.915	5.974	24.462	69.883	154.718	287.596	473.740	716.222
5.	.000	.000	.000	.000	.000	.000	.009	.159	1.550	8.909	32.928	87.348	183.764	329.827	530.098	787.267
10.	.000	.000	.000	.000	.000	.001	.020	.293	2.495	12.747	42.977	106.799	214.853	373.910	587.971	859.405
15.	.000	.000	.000	.000	.000	.002	.039	.512	3.837	17.587	54.618	128.128	247.798	419.622	647.128	932.410
20.	.000	.000	.000	.000	.000	.004	.075	.852	5.662	23.505	67.827	151.212	282.416	466.756	707.357	999.000
25.	.000	.000	.000	.000	.000	.007	.134	1.356	8.055	30.550	82.559	175.921	318.533	515.122	768.470	999.000
30.	.000	.000	.000	.000	.001	.015	.231	2.073	11.089	38.747	98.749	202.125	355.984	564.545	830.295	999.000
35.	.000	.000	.000	.000	.001	.027	.381	3.054	14.830	48.101	116.322	229.692	394.613	614.863	892.677	999.000
40.	.000	.000	.000	.000	.002	.048	.604	4.354	19.326	58.598	135.193	258.495	434.277	665.932	955.478	999.000
45.	.000	.000	.000	.000	.004	.083	.925	6.024	24.614	70.209	155.273	288.414	474.841	717.618	999.000	999.000
50.	.000	.000	.000	.000	.008	.136	1.369	8.113	30.715	82.895	176.474	319.331	516.183	769.803	999.000	999.000
55.	.000	.000	.000	.000	.013	.216	1.968	10.664	37.637	96.606	198.704	351.139	558.188	822.376	999.000	999.000
60.	.000	.000	.000	.001	.023	.333	2.751	13.713	45.378	111.289	221.877	383.735	600.754	875.240	999.000	999.000
65.	.000	.000	.000	.002	.038	.497	3.750	17.289	53.925	126.887	245.908	417.024	643.786	928.304	999.000	999.000
70.	.000	.000	.000	.003	.061	.723	4.996	21.411	63.257	143.339	270.715	450.917	687.197	981.489	999.000	999.000
75.	.000	.000	.000	.005	.094	1.025	6.516	26.095	73.350	160.586	296.222	485.333	730.907	999.000	999.000	999.000
80.	.000	.000	.000	.008	.142	1.420	8.338	31.345	84.170	178.569	322.354	520.197	774.846	999.000	999.000	999.000
85.	.000	.000	.000	.013	.210	1.924	10.484	37.162	95.684	197.229	349.045	555.438	818.947	999.000	999.000	999.000
90.	.000	.000	.001	.020	.302	2.554	12.972	43.539	107.855	216.509	376.230	590.994	863.152	999.000	999.000	999.000
95.	.000	.000	.001	.031	.426	3.329	15.817	50.467	120.644	236.356	403.849	626.805	907.406	999.000	999.000	999.000
100.	.000	.000	.002	.047	.588	4.265	19.032	57.930	134.013	256.716	431.845	662.817	951.661	999.000	999.000	999.000
105.	.000	.000	.003	.068	.797	5.378	22.621	65.911	147.924	277.542	460.169	698.982	995.872	999.000	999.000	999.000
110.	.000	.000	.005	.098	1.060	6.683	26.590	74.390	162.337	298.785	488.771	735.254	999.000	999.000	999.000	999.000
115.	.000	.000	.008	.138	1.387	8.193	30.938	83.346	177.216	320.403	517.607	771.592	999.000	999.000	999.000	999.000
120.	.000	.000	.012	.191	1.787	9.918	35.661	92.755	192.525	342.354	546.636	807.959	999.000	999.000	999.000	999.000
125.	.000	.001	.017	.260	2.269	11.869	40.756	102.595	208.228	364.599	575.820	844.321	999.000	999.000	999.000	999.000
130.	.000	.001	.024	.347	2.842	14.053	46.213	112.839	224.291	387.101	605.125	880.646	999.000	999.000	999.000	999.000
135.	.000	.001	.034	.457	3.516	16.476	52.024	123.466	240.684	409.827	634.518	916.906	999.000	999.000	999.000	999.000
140.	.000	.002	.047	.594	4.298	19.141	58.177	134.450	257.375	432.746	663.970	953.074	999.000	999.000	999.000	999.000
145.	.000	.003	.065	.762	5.196	22.049	64.660	145.767	274.335	455.827	693.454	989.129	999.000	999.000	999.000	999.000
150.	.000	.004	.087	.964	6.218	25.202	71.460	157.395	291.537	479.043	722.944	999.000	999.000	999.000	999.000	999.000
155.	.000	.006	.116	1.206	7.370	28.597	78.564	169.312	308.956	502.370	752.419	999.000	999.000	999.000	999.000	999.000
160.	.000	.009	.152	1.492	8.657	32.233	85.957	181.495	326.567	525.783	781.856	999.000	999.000	999.000	999.000	999.000
165.	.000	.012	.196	1.827	10.085	36.105	93.625	193.924	344.347	549.260	811.237	999.000	999.000	999.000	999.000	999.000
170.	.001	.016	.252	2.215	11.656	40.209	101.553	206.579	362.275	572.782	840.545	999.000	999.000	999.000	999.000	999.000
175.	.001	.022	.319	2.660	13.374	44.540	109.727	219.440	380.331	596.330	869.762	999.000	999.000	999.000	999.000	999.000

TABLE 5.1.2.7-16 (CONT) TDDB: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 6.50 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm)															
	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.001	.013	.173	1.430	7.489	26.567	69.628	146.569	264.384	427.472	638.520	899.187
5.	.000	.000	.000	.000	.001	.026	.310	2.272	10.696	34.827	85.689	172.501	301.519	476.625	700.190	973.685
10.	.000	.000	.000	.000	.003	.050	.529	3.456	14.746	44.449	103.409	200.124	340.184	527.026	762.756	999.000
15.	.000	.000	.000	.000	.006	.092	.861	5.056	19.705	55.426	122.691	229.282	380.194	578.484	826.030	999.000
20.	.000	.000	.000	.001	.012	.160	1.344	7.141	25.622	67.725	143.429	259.822	421.376	630.821	889.842	999.000
25.	.000	.000	.000	.001	.022	.268	2.021	9.775	32.524	81.301	165.512	291.598	463.571	683.879	954.041	999.000
30.	.000	.000	.000	.002	.039	.429	2.935	13.012	40.418	96.094	188.829	324.472	506.632	737.515	999.000	999.000
35.	.000	.000	.000	.004	.067	.664	4.132	16.896	49.300	112.035	213.270	358.315	550.425	791.599	999.000	999.000
40.	.000	.000	.000	.007	.110	.995	5.655	21.458	59.147	129.051	238.729	393.006	594.829	846.015	999.000	999.000
45.	.000	.000	.001	.013	.175	1.444	7.545	26.718	69.929	147.066	265.104	428.433	639.733	900.658	999.000	999.000
50.	.000	.000	.001	.022	.270	2.038	9.838	32.684	81.609	166.004	292.299	464.495	685.036	955.435	999.000	999.000
55.	.000	.000	.002	.036	.405	2.803	12.564	39.356	94.142	185.790	320.223	501.096	730.647	999.000	999.000	999.000
60.	.000	.000	.003	.058	.590	3.767	15.746	46.726	107.480	206.350	348.790	538.151	776.484	999.000	999.000	999.000
65.	.000	.000	.006	.089	.839	4.954	19.403	54.776	121.572	227.612	377.922	575.578	822.473	999.000	999.000	999.000
70.	.000	.000	.009	.134	1.164	6.389	23.544	63.486	136.369	249.509	407.544	613.308	868.546	999.000	999.000	999.000
75.	.000	.001	.015	.196	1.581	8.092	28.175	72.830	151.819	271.977	437.590	651.272	914.642	999.000	999.000	999.000
80.	.000	.001	.023	.281	2.104	10.081	33.295	82.779	167.872	294.955	467.995	689.412	960.709	999.000	999.000	999.000
85.	.000	.002	.035	.395	2.748	12.373	38.901	93.302	184.479	318.386	498.701	727.673	999.000	999.000	999.000	999.000
90.	.000	.003	.052	.543	3.528	14.979	44.983	104.367	201.592	342.217	529.657	766.005	999.000	999.000	999.000	999.000
95.	.000	.005	.075	.733	4.459	17.907	51.528	115.940	219.167	366.397	560.812	804.364	999.000	999.000	999.000	999.000
100.	.000	.007	.107	.971	5.553	21.162	58.523	127.990	237.159	390.880	592.122	842.708	999.000	999.000	999.000	999.000
105.	.000	.011	.149	1.267	6.821	24.747	65.949	140.482	255.527	415.624	623.546	881.002	999.000	999.000	999.000	999.000
110.	.001	.016	.204	1.627	8.276	28.660	73.789	153.385	274.234	440.589	655.046	919.211	999.000	999.000	999.000	999.000
115.	.001	.022	.274	2.061	9.924	32.900	82.023	166.666	293.241	465.737	686.589	957.307	999.000	999.000	999.000	999.000
120.	.002	.032	.364	2.575	11.774	37.461	90.631	180.297	312.516	491.034	718.142	995.260	999.000	999.000	999.000	999.000
125.	.002	.044	.475	3.178	13.830	42.336	99.591	194.247	332.025	516.449	749.678	999.000	999.000	999.000	999.000	999.000
130.	.004	.060	.613	3.877	16.098	47.516	108.884	208.488	351.738	541.953	781.170	999.000	999.000	999.000	999.000	999.000
135.	.005	.081	.779	4.679	18.578	52.992	118.487	222.994	371.627	567.520	812.596	999.000	999.000	999.000	999.000	999.000
140.	.007	.108	.980	5.590	21.271	58.754	128.382	237.740	391.667	593.124	843.933	999.000	999.000	999.000	999.000	999.000
145.	.010	.142	1.218	6.616	24.178	64.789	138.548	252.701	411.832	618.744	875.162	999.000	999.000	999.000	999.000	999.000
150.	.014	.183	1.497	7.761	27.296	71.086	148.965	267.855	432.101	644.358	906.266	999.000	999.000	999.000	999.000	999.000
155.	.019	.235	1.823	9.030	30.623	77.632	159.615	283.180	452.451	669.947	937.228	999.000	999.000	999.000	999.000	999.000
160.	.025	.297	2.198	10.426	34.155	84.416	170.480	298.656	472.863	695.495	968.035	999.000	999.000	999.000	999.000	999.000
165.	.033	.373	2.626	11.951	37.888	91.424	181.541	314.265	493.320	720.985	998.673	999.000	999.000	999.000	999.000	999.000
170.	.043	.463	3.111	13.607	41.815	98.645	192.783	329.988	513.804	746.403	999.000	999.000	999.000	999.000	999.000	999.000
175.	.055	.568	3.657	15.396	45.932	106.064	204.190	345.809	534.300	771.736	999.000	999.000	999.000	999.000	999.000	999.000

TABLE 5.1.2.7-16 (CONT) TDDB: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 7.00 LOG SQUARE MICRONS

(Notes for Table 5.1.2.7-16)

NOTE 1: Temperature axis refers to T_J as detailed in note of Table 5.1.2.7-4.

NOTE 2: Electric Field Stress axis refers to worst case voltage applied to the thinnest transistor gate oxide using the following expression:

$$E_S = .1(V_{op} / t_{ox}) \quad \text{(in MV / cm)}$$

where:

V_{op} = operating voltage (in volts)

t_{ox} = oxide thickness (in KA)

If oxide thickness is not known, Table 5.1.2.7-19 gives default values based on the number of transistors on the device in question.

NOTE 3: The correct page for use is determined by the total amount of active transistor gate oxide area. If total amount of active transistor gate oxide area is not known, Table 5.1.2.7-18 gives default values based on the number of transistors on the device in question.

	Current Density (MA/cm2)															
T(C)	.04	.05	.06	.08	.10	.13	.17	.20	.25	.30	.40	.50	.60	.80	1.00	1.30
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	55.671
30.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000
35.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000
40.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	1.260	999.000	999.000
45.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000
50.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	1.028	999.000	999.000	999.000
55.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000
60.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000
65.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.110	999.000	999.000	999.000	999.000	999.000
70.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000
75.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000
80.	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
85.	.000	.000	.000	.000	.000	.000	.000	.000	2.155	999.000	999.000	999.000	999.000	999.000	999.000	999.000
90.	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
95.	.000	.000	.000	.000	.000	.000	.000	.956	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
100.	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
105.	.000	.000	.000	.000	.000	.000	552.893	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
110.	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
115.	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
120.	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
125.	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
130.	.000	.000	.000	.000	.055	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
135.	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
140.	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
145.	.000	.000	.000	124.681	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
150.	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
155.	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
160.	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
165.	.000	.000	927.293	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
170.	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
175.	.000	68.718	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000

TABLE 5.1.2.7-17 ELECTROMIGRATION: EFFECTIVE HAZARD RATE (x 10E-6) AT 10000. HOURS

(Notes for Table 5.1.2.7-17)

NOTE 1: Temperature axis refers to T_J as detailed in note of Table 5.1.2.7-4 ($T_J = T_C + \Theta_{JC} \times P$).

NOTE 2: Current Density axis refers to worst case current density on device. The default value is .13 MA / cm^2.

Table 5.1.2.7-18 Total Transistor Gate Area (log μm^2)

Complexity (# of trans.)	Digital Microprocessors (including Controllers)	Digital and Linear Gate / Logic Arrays
100 - 500	5.39	5.24
500 - 1K	5.47	5.37
1K - 5K	5.64	5.67
5K - 10K	5.72	5.80
10K - 50K	5.90	6.10
50K - 100K	5.97	6.23
100K - 500K	6.15	6.52
500K - 1M	6.23	6.65
1M - 5M	6.41	6.95
5M - 10M	6.48	7.08

NOTE Total Transistor Gate Area refers to the total amount of active transistor gate oxide area on the device based on the number of transistors on the device using the following expression:

$$A = \log(4*TR*10^{-0.744*(\log(TR)-5.50)}) \quad (\text{in } \log \mu m^2)$$

for MOS Digital Microprocessors (Including Controllers), and

$$A = \log(6*TR*10^{-0.580*(\log(TR)-5.78)}) \quad (\text{in } \log \mu m^2)$$

for MOS digital and Linear Devices (Including Gate / Logic Arrays)

TR is the number of transistors on the device in question

Table 5.1.2.7-19 Dielectric Thickness (kÅ)

Complexity (# of trans.)	Digital Microprocessors (including Controllers)	Digital and Linear Gate / Logic Arrays
100 - 500	4.81	2.17
500 - 1K	2.50	1.35
1K - 5K	1.89	1.10
5K - 10K	0.98	0.68
10K - 50K	0.74	0.56
50K - 100K	0.39	0.35
100K - 500K	0.29	0.28
500K - 1M	0.15	0.17
1M - 5M	0.11	0.14
5M - 10M	0.06	0.09

NOTE 1: Dielectric Thickness refers to the thinnest transistor gate oxide on the device based on the number of transistors on the device using the following expression:

$$t_{ox} = 10^{-0.406*(\log(TR)-3.68)} \quad (\text{in } kÅ)$$

for MOS Digital Microprocessors (Including Controllers), and

$$t_{ox} = 10^{-0.296*(\log(TR)-3.14)} \quad (\text{in } kÅ)$$

for MOS Digital and Linear Devices (Including Gate / Logic Arrays)

TR is the number of transistors on the device in question

NOTE 2: The electric field stress, E_S, is given by

$$E_S = 11\ V_{op}/t_{ox} \quad (\text{Mv/cm}), \qquad (5.1.2.7.14)$$

where:

V_{op} = operating voltage (user supplied V)

t_{ox} = oxide thickness (user supplied kÅ)

Table 5.1.2.7-20 Gate Oxide Area, Memories

MOS SRAMS AND BIMOS SRAMS*		
Capacity (# bits)	Total Gate Oxide Area (μm^2) Lower Limit	Upper Limit
1K	99,176	497,056
2K	149,352	798,112
4K	45,864	192,888
8K	82,728	358,776
16K	156,456	690,552
32K	303,912	1,354,104
64K	598,824	2,482,600
128K	1,188,648	2,681,208
256K	1,052,576	4,730,592
512K	3,101,152	9,449,184
1M	4,198,304	18,886,368
2M	8,392,608	37,760,736

*For BiMOS SRAMs, multiply oxide area by .667

MOS DRAMS		
Capacity (# bits)	Total Gate Oxide Area (μm^2) Lower Limit	Upper Limit
1K	98,588	394,352
2K	123,676	494,704
4K	31,932	95,796
8K	50,364	151,092
16K	87,228	261,684
32K	160,956	482,868
64K	308,412	925,236
128K	603,324	1,809,972
256K	530,288	1,590,864
512K	1,054,576	3,163,728
1M	2,103,152	6,309,456
2M	4,200,304	12,600,912

UVEPROMS, EEPROMS, FLOATING GATE PROMS, PALS, PLAS, MOS ROMS, HALS, MLAS For all device capacities: 260,000-1,209,000μm^2

NOTE: If gate oxide area is unknown, assume upper limit.

Table 5.1.2.7-21 Gate Oxide Thickness, Memories

MOS ROMs/PLAs/PALs/MLAs/HALs*		
Capacity (# bits)	Gate Oxide Thickness (Angstroms) Lower Limit	Upper Limit
2K	600	700
4K	600	700
8K	600	700
16K	600	700
32K	600	700
64K	400	600
128K	400	500
256K	400	500
512K	400	500
1M	250	400
2M	250	400

*For MOS ROMs/PLAs/PALs/MLAs/HALs determine number of bits in the array, then use above table, rounding up to the next highest bit category.

UVEPROMs, MNOS/Flash EEPROMs, Float. Gate PROMs		
Capacity (# bits)	Gate Oxide Thickness (Angstroms) Lower Limit	Upper Limit
2K	600	700
4K	600	700
8K	600	700
16K	600	700
32K	600	700
64K	400	600
128K	300	400
256K	300	400
512K	235	400
1M	235	400
2M	235	400

Table 5.1.2.7-21 Gate Oxide Thickness, Memories (continued)

FLOTOX and Tex-Poly EEPROMs		
Capacity (# bits)	Gate Oxide Thickness (Angstroms) Lower Limit	Upper Limit
8K	600	750
16K	600	750
32K	600	750
64K	400	600
128K	340	500
256K	340	500
512K	300	500
1M	300	500
2M	300	500

MOS SRAMs, DRAMs BiMOS SRAMs		
Capacity (# bits)	Gate Oxide Thickness (Angstroms) Lower Limit	Upper Limit
1K	1200	1500
2K	1200	1500
4K	410	1000
8K	410	1000
16K	250	410
32K	250	410
64K	250	410
128K	250	410
256K	200	300
512K	200	300
1M	200	300
2M	200	300

NOTE: If gate oxide thickness is unknown, assume lower limit.

Table 5.1.2.7-22: Cross Reference for Commercial Type to MIL-M-38510 Type

COMMERCIAL	M38510/	COMMERCIAL	M38510/	COMMERCIAL	M38510/
REF10	12403	LM139	11201	PAL16R6A-2	50409
LM101A	10103	LM140H-05	10702	PAL16L8A	50401
LM102	10601	LM140H-12	10703	PAL16R8A	50402
10501	06001	LM140H-15	10704	PAL16L8A-2	50407
10502	06002	LM140H-24	10705	PAL16R8A-2	50408
10504	06201	LM140K-05	10706	1802D	47001
10505	06003	LM140K-12	10707	DG181A	11101
10506	06004	LM140K-15	10708	DG182A	11102
10507	06005	LM140K-24	10709	1832	47201
10509	06006	14013B	05151	DG184A	11103
10524	06301	14023B	05053	DG185A	11104
10525	06302	14093B	17701	1853	47401
10531	06101	PAL14H4	50303	DG187-A	11105
10535	06104	PAL14L4	50308	DG188A	11106
10576	06103	LM141H-05	10702	DG190A	11107
10597	06202	LM141H-12	10703	DG191A	11108
LM106	10303	LM141H-15	10704	LM193	11202
10631	06102	LM141H-24	10705	LF198	12501
LM108A	10104	14502	17403	LM199A	12401
PAL10H8	50301	MC14069	17401	LM199	12404
PAL10L8	50306	LF147	11906	DG200	12301
LM109	10701	LM148	11001	HI200	12301
LM110	10602	LM149	11002	2003	14103
LM111	10304	LM150K	11705	DG201	12302
LM117H	11703	LF151	11904	HI201	12302
LM117K	11704	1524	12601	PAL20R4A	50504
LM118	10107	LM1524	12601	PAL20R6A	50503
LM120H-05	11501	LF153	11905	PAL20L8A	50501
LM120H-12	11502	15482	00601	PAL20R8A	50502
LM120H-15	11503	LF155	11401	LH2101A	10105
LM120H-24	11504	LF155A	11404	LH2108A	10106
LM120K-05	11505	1558	10108	LH2110	10603
LM120K-12	11506	LF156	11402	LH2111	10305
LM120K-15	11507	LF156A	11405	2114	23002
LM120K-24	11508	LF157	11403	2114A	23804
DAC1221LD	12707	LF157A	11406	2117	24001
LM124	11005	PAL16C1	50305	2117	24002
PAL12H6	50302	PAL16H2	50304	2117	24003
PAL12L6	50307	PAL16L2	50309	2147	23801
LM129A	12402	PAL16R4A	50404	2147H	23803
LM129B	12406	PAL16X4	50405	2147H-3	23805
LM137H	11803	PAL16A4	50406	2147H-2	23807
LM137K	11804	PAL16R4A-2	50410	2148H	23806
LM138K	11706	PAL16R6A	50403	2164	24401

Table 5.1.2.7-22: Cross Reference for Commercial Type to MIL-M-38510 Type (continued)

COMMERCIAL	M38510/	COMMERCIAL	M38510/	COMMERCIAL	M38510/
2164	24402	DG300	11601	4014B	05752
2164	24403	DG301A	11602	4015A	05703
2316E	40301	3018A	10801	4015B	05753
24401	24401	DG302A	11603	4016A	05801
2500	12204	DG303A	11604	4016B	05851
2510	12205	DG304A	11605	4017A	05601
2516	22101	3045	10802	4017B	05651
25LS174	33106	DG305A	11606	40174B	17505
25LS175	33107	DG306A	11607	4018A	05602
2520	12206	DG307A	11608	4018B	05652
2532	22201	MC3101	15501	4019A	05302
0026	03501	MC3106	15502	4019B	05352
DS0026	03501	MC3111	15503	4020A	05603
MH0026	03501	MK34000	40301	4020B	05653
2600	12202	34069	17401	4021A	05704
2616	40301	3516E	40301	4021B	05754
2620	12203	3636	21002	4022A	05604
OP27A	13503	4000A	05201	4022B	05654
2700	12201	40008	05251	4023A	05003
2708	22001	4001A	05202	4023B	05053
2716	22101	40018	05252	4024A	05605
27S180	20903	4002A	05203	4024B	05655
27S181	20904	40028	05253	4025A	05204
27S191	21002	4006A	05701	4025B	05254
2732	22202	40068	05751	4027A	05102
NMC2816	22601	4007A	05301	4027B	05152
28S166A	21002	4007UB	05351	4028A	05901
28S166A	21004	4008A	05401	4028B	05951
2901A	44001	40088	05451	4030A	05303
2901C	44001	4009A	05501	4030B	05353
2905	44101	4009UB	05551	4031A	05705
2906	44102	4010A	05502	4031B	05755
2907	44103	40108	05552	4034A	05706
2915A	44104	40106B	17702	4034B	05756
2916A	44105	40107B	17402	4041A	05505
2917A	44106	40109B	17404	4041UB	05555
2918	44201	4011A	05001	4043A	05103
29611	20402	40118	05051	4043B	05153
29621	20805	4012A	05002	4048A	05304
29631	20904	40128	05052	4048B	05354
29651	20902	4013A	05101	4049A	05503
29651	20908	40138	05151	4049UB	05553
29681	21002	4014A	05702	4050A	05504

Table 5.1.2.7-22: Cross Reference for commercial Type to MIL-M-38510 Type (continued)

COMMERCIAL	M38510/	COMMERCIAL	M38510/	COMMERCIAL	M38510/
4050B	05554	4564	24401	53S841	20902
TMS4050	23502	4564	24402	53S841	20908
TMS4050	23504	4564	24403	5400	00104
4060A	05X01	4741	11003	54L00	02004
TMS4060	23501	506	19001	54H00	02304
TMS4060	23503	506A	19002	54S00	07001
4066A	05802	507	19003	54LS00	30001
4066B	05852	507A	19004	54F00	33001
4067B	17801	508A	19005	54ALS00	37001
4069UB	17401	509A	19006	54HC00	65001
4070B	17203	HPROM512	20101	5401	00107
4070B	05353	51C67	29103	54L01	02006
4071B	17101	51C67	29106	54H01	02306
4072B	17102	52116	40301	5402	00401
4073B	17003	MM5280	23505	54L02	02701
4075B	17103	MM5280	23506	54S02	07301
4076B	17501	5300-1	20301	54LS02	30301
4077B	17204	5301-1	20302	54F02	33301
4081B	17001	MCM5303	20101	54ALS02	37301
4082B	17002	MCM5304	20102	5403	00109
4085B	17201	5305-1	20401	54L03	02006
4086B	17202	5306-1	20402	54S03	07002
4093B	17701	53S1680	21001	54LS03	30002
4095B	17502	53S1681	21002	5404	00105
4096B	17503	AD532S	13903	54C04	17401
MK84096	23602	5330	20701	54L04	02005
MK84096	23604	5331	20702	54H04	02305
4097B	17802	AD534T	13901	54S04	07003
4098B	17504	AD534S	13902	54LS04	30003
4099B	17601	5340-1	20801	54F04	33002
4116	24001	5341-1	20802	54ALS04	37006
4116	24002	53S440	20601	5405	00108
4116	24003	53S441	20602	54S05	07004
4136	11004	5348-1	20804	54LS05	30004
4156	11003	5349-1	20805	5406	00801
4213	13904	5352-1	20601	5407	00803
4502B	17403	5353-1	20602	5408	01601
4508B	17602	5380-1	20903	54S08	08003
4514B	17301	5380-2	20903	54H08	15501
4515B	17302	5381-1	20904	54H08	15504
4532B	17303	5381-2	20904	54LS08	31004
4555B	17304	53S840	20901	54F08	34001
4556B	17305	53S840	20907	54ALS08	37401

Table 5.1.2.7-22: Cross Reference for Commercial Type to MIL-M-38510 Type (continued)

COMMERCIAL	M38510/	COMMERCIAL	M38510/	COMMERCIAL	M38510/
5409	01602	54116	01503	54F151	33901
54S09	08004	5412	00106	54153	01403
54LS09	31005	54LS12	30006	54S153	07902
5410	00103	54121	01201	54LS153	30902
54L10	02003	54L121	04201	54F153	33902
54H10	02303	54122	01202	54154	15201
54S10	07005	54L122	04202	54155	15202
54LS10	30005	54LS122	31403	54LS155	32601
54F10	33003	54123	01203	54156	15203
54ALS10	37002	54LS123	31401	54LS156	32602
54HC10	65002	54LS124	31701	54157	01405
54ALS1000	38401	54125	15301	54S157	07903
54ALS1002	38402	54LS125	32301	54LS157	30903
54ALS1003	38403	54LS125A	32301	54F157	33903
54ALS1004	38409	54126	15302	54S158	07904
54ALS1005	38410	54LS126	32302	54LS158	30904
54ALS1008	38404	5413	15101	54F158	33904
54H101	02205	54LS13	31301	5416	00802
54ALS1010	38405	54132	15103	54160	01303
54ALS1011	38406	54LS132	31303	54LS160	31503
54ALS1020	38407	54HC132	65005	54LS160A	31503
54H103	02206	54S133	07009	54161	01306
54ALS1032	38408	54ALS133	37005	54LS161	31504
54ALS1034	38411	54S134	07010	54LS161A	31504
54ALS1035	38412	54S135	07502	54162	01305
54107	00203	54S138	07701	54LS162	31511
54LS107	30108	54LS138	30701	54LS162A	31511
54LS109	30109	54ALS138	37701	54163	01304
54F109	34102	54S139	07702	54LS163	31512
54ALS109	37102	54LS139	30702	54LS163A	31512
54S11	08001	5414	15102	54164	00903
54H11	15502	54LS14	31302	54L164	02902
54LS11	31001	54S140	08101	54LS164	30605
54F11	34002	54145	01005	54165	00904
54ALS11	37402	54147	15601	54LS165	30608
54S112	07102	54148	15602	54LS165A	30608
54LS112	30103	54LS148	36001	54LS166	30609
54F112	34103	54S15	08002	54LS168	31505
54ALS112A	37103	54LS15	31002	54LS169	31506
54S113	07103	54150	01401	54LS169A	31506
54LS113	30104	54151	01406	5417	00804
54S114	07104	54S151	07901	54170	01801
54LS114	30105	54LS151	30901	54LS170	31902

Table 5.1.2.7-22: Cross Reference for Commercial Type to MIL-M-38510 Type (continued)

COMMERCIAL	M38510/	COMMERCIAL	M38510/	COMMERCIAL	M38510/
54LS173	36101	54H21	15503	54LS273	32501
54174	01701	54LS21	31003	54LS279	31602
54S174	01705	54H22	02307	5428	16201
54LS174	30106	54S22	07007	54LS28	30204
54F174	34107	54LS22	30008	54ALS28	38402
54ALS174	37201	54LS221	31402	54LS280	32901
54175	01702	5423	00402	54F280	34901
54S175	07106	54LS240	32401	54LS283	31202
54LS175	30107	54F240	33201	54F283	34201
54F175	34104	54ALS240	38301	54S287	20302
54ALS175	37202	54LS241	32402	54S288	20702
54180	01901	54F241	33202	54LS290	32003
54181	01101	54ALS241	38302	54LS293	32004
54S181	07801	54ALS242	38506	54LS295B	30606
54LS181	30801	54ALS243	38507	54LS298	30909
54182	01102	54LS244	32403	5430	00101
54S182	07802	54F244	33203	54L30	02001
54LS190	31513	54ALS244	38303	54H30	02301
54LS191	31509	5425	00403	54S30	07008
54192	01308	54S251	07905	54LS30	30009
54LS192	31507	54LS251	30905	54ALS30	37004
54193	01309	54F251	33905	54HC30	65004
54L193	02503	54S253	07908	5432	16101
54LS193	31508	54LS253	30908	54LS32	30501
54194	00905	54F253	33908	54F32	33501
54S194	07601	54ALS253	3XX01	54ALS32	37501
54LS194	30601	54S257	07906	54LS324	31702
54LS194A	30601	54LS257	30906	54LS348	36002
54F194	33601	54LS257B	30906	54F352	33909
54195	00906	54F257	33906	54F353	33910
54S195	07602	54S258	07907	54365	16301
54LS195	30602	54LS258	30907	54LS365	32201
54LS195A	30602	54LS258B	30907	54366	16302
54LS196	32001	54F258	33907	54LS366	32203
54LS197	32002	54LS259	31603	54367	16303
5420	00102	54LS259B	31605	54LS367	32202
54L20	02002	5426	00805	54368	16304
54H20	02302	54LS26	32102	54LS368	32204
54S20	07006	54LS261	31801	5437	00302
54LS20	30007	54LS266	30303	54LS37	30202
54F20	33004	5427	00404	54ALS37	38401
54ALS20	37003	54LS27	30302	54LS373	32502
54HC20	65003	54ALS27	37302	54LS374	32503

Table 5.1.2.7-22: Cross Reference for Commercial Type toi MIL-M-38410 Type (continued)

COMMERCIAL	M38510/	COMMERCIAL	M38510/	COMMERCIAL	M38510/
54F374	34105	54S51	07401	54H74	02203
54LS375	31604	54LS51	30401	54S74	07101
54LS377	32504	54F521	34701	54LS74	30102
54F378	34108	5453	00503	54F74	34101
54F379	34109	54H53	04003	54ALS74	37101
5438	00303	54F534	34106	5475	01501
54LS38	30203	5454	00504	54LS75	31601
54LS390	32701	54H54	04004	5476	00204
54LS393	32702	54L54	04102	54H76	02204
54LS395A	30607	54LS54	30402	54LS76	30110
5440	00301	54LS540	32404	54LS76A	30110
54H40	02401	54LS541	32405	5477	01502
54S40	07201	54H55	04005	54L78	02104
54LS40	30201	54L55	04103	5479	00207
54ALS40	38407	54S570	20401	5480	00604
54S412	42101	54S571	20402	5482	00601
5442	01001	54S572	20601	5483	00602
54L42	02901	54S573	20602	54LS83A	31201
54LS42	30703	54ALS574	37104	54S85	08201
54LS424	42201	54ALS576	37105	5485	15001
54S428	42301	54S64	07402	54LS85	31101
5443	01002	54F64	33401	54ALS857	37901
54L43	02902	54LS640	32804	5486	00701
5444	01003	54ALS640	38501	54L86	02601
54L44	02903	54ALS641	38502	54S86	07501
5445	01004	54ALS642	38503	54L86	30502
5446	01006	54ALS643	38504	54F86	34501
54L46	02904	54ALS645	38505	54ALS874	37106
5447	01007	54LS646	32804	54ALS876	37107
54L47	02905	54LS648	32805	5490	01307
54LS47	30704	54S65	07403	54L90	02501
54S472	20805	54LS670	31901	54LS90	31501
54S473	20804	5470	00206	5492	01301
54S474	20802	54L71	02101	54LS92	31510
54S475	20801	5472	00201	54C929	23901
5448	01008	54L72	02102	5493	01302
5449	01009	54H72	02201	54L93	02502
54LS490	32703	5473	00202	54LS93	31502
5450	00501	54L73	02103	54L93A	02502
54H50	04001	54H73	02202	54C930	23902
5451	00502	54LS73	30101	5495	00901
54H51	04002	5474	00205	54L95	02801
54L51	04101	54L74	02105	54LS95	30603

Table 5.1.2.7-22: Cross Reference for Commercial Type to MIL-M-38510 Type (continued)

COMMERCIAL	M38510/	COMMERCIAL	M38510/	COMMERCIAL	M38510/
54LS95B	30603	6208	19008	7611	20302
5496	00902	6216	19003	76160	21001
54LS96	30604	064	11903	76161	21002
55107	10401	6504	24501	76165	21005
55108	10402	6508	23901	7620	20401
55113	10405	6514	24502	7621	20402
55114	10403	6516	29102	76321	21101
55115	10404	65162	29101	7640	20801
SMJ5517	29101	65162	29104	7641	20802
SMJ5517	29105	65162	29105	76L42A	02906
5532A	13102	6518	23902	7642	20601
55325	13001	65262	29103	7643	20602
55326	13002	MCM6604A	23602	7644	20603
55327	13003	MCM6604A	23604	76L70	02805
5534A	13101	MCM6605	23601	7680	20903
SE5537	12502	MCM6605	23603	7681	20904
55450	12901	IM6654	21901	7684	20901
55451	12902	6665	24401	7685	20902
55452	12903	6665	24402	771	11904
55453	12904	6665	24403	77S180	20903
55454	12905	6800	40001	77S181	20904
55460	12906	6810	40201	77S184	20901
55461	12907	S68318	40301	77S185	20902
55462	12908	68A316E	40301	77S190	21001
55463	12909	68316E	40301	77S191	21002
55464	12910	071	11904	772	11905
555	10901	710	10301	774	11906
556	10902	LM710	10301	78MG	11701
557	10903	711	10302	78G	11702
IM5603A	20201	LM711	10302	78M05	10702
A0561	13301	714	13502	7805	10706
IM5623	20202	7181	01101	NC7810LC	22501
S68318	40301	072	11905	78M12	10703
A0571	13401	LM723	10201	7812	10707
A0584S	12801	MM7280	23505	78M15	10704
A0584T	12802	MM7280	23506	7815	10708
061	11901	074	11906	78M24	10705
6108	19007	LM741A	10101	7824	10709
6116	19001	LM747A	10102	7831	10406
6116	29101	7558	10108	7832	10407
6116	29104	7602	20701	79MG	11801
6116	29105	7603	20702	79G	11802
062	11902	7610	20301	79M05	11501

Table 5.1.2.7-22: Cross Reference for Commercial Type to MIL-M-38510 Type (continued)

COMMERCIAL	M38510/	COMMERCIAL	M38510/	COMMERCIAL	M38510/
7905	11505	82S185	20902	93L01	02907
79M12	11502	82S190	21001	9301	15206
7912	11506	82S191	21002	9304	00603
79M15	11503	82S191B	21004	9308	01503
7915	11507	82S23	20701	93L08	04502
79M24	11504	8224	42201	9309	01404
7924	11508	82S2708	20905	93L09	04601
DAC-08	11301	8228	42301	93L10	02504
DAC-08A	11302	8250	15204	9311	15201
Z-80	48002	8251	15205	9312	01402
Z-80A	48001	8252	15206	93L12	04602
Z80ACPU	48001	8264	24401	9314	01504
Z-80B	48003	8264	24402	93L14	04501
Z80CPU	48002	8264	24403	93L16	02505
Z80BCPU	48003	9093	03304	9317	15802
Z8001	52001	AM9130CFC	23701	93L18	04301
Z8001A	52003	AM9130AFC	23702	9318	15603
Z8002	52002	AM9130CDM	23703	932	03101
Z8002A	52004	AM9130CFM	23703	9321	15801
8080A	42001	AM9130ADM	23704	9322	01405
82S10	23101	AM9130AFM	23704	93L22	04603
82S10	23107	AM91L30CF	23705	93L24	04401
82S11	23102	AM91L30AF	23706	9324	15002
82S11	23108	AM91L30CDM	23707	93L28	02803
82S115	20803	AM91L30CFM	23707	9328	15902
8212	42101	AM91L30ADM	23708	933	03105
82S123	20702	AM91L30 AFM	23708	9334	16001
82S126	20301	AM9140CFC	23709	9338	15701
82S126A	20303	AM9140AFC	23710	9341	01101
82S129	20302	AM9140CDM	23711	93410	23001
82S129A	20304	AM9140CFM	23711	93411	23003
82S130	20401	AM9140ADM	23712	93412	23109
82S130A	20403	AM9140AFM	23712	93L412	23111
82S131	20402	AM91L40CDC	23713	93415	23101
82S131A	20404	AM91L40AFC	23714	93L415	23103
82S136	20601	AM91L40CDM	23715	93415	23105
82S137	20602	AM91L40CFM	23715	93415	23107
82S137A	20604	AM91L40ADM	23716	93417	20301
82S140	20801	AM91L40AFM	23716	93419	23201
82S141	20802	9218	40301	9342	01102
82S180	20903	930	03001	93L420	23004
82S181	20904	93L00	02804	93421	23002
82S184	20901	9300	15901	93422	23110

Table 5.1.2.7-22: Cross Reference for Commercial Type to MIL-M-38510 Type (continued)

COMMERCIAL	M38510/	COMMERCIAL	M38510/	COMMERCIAL	M38510/
93L422	23112	93453	20602	946	03004
93422A	23114	93460	20906	948	03302
93L422A	23115	93461	20905	950	03303
93425	23102	935	03002	951	03201
93L425	23104	93510	21001	9LS51	30401
93425	23106	93Z510	21003	9LS54	30402
93425A	23108	93511	21002	957	03103
93L425A	23113	93Z511	21002	958	03104
93427	20302	93Z511	21004	9601	01204
93436	20401	936	03003	9602	01205
93438	20801	9380	06604	9614	10403
93446	20402	9382	00601	9615	10404
93448	20802	9383	00602	962	03005
93450	20903	940	03002	SBP9900A	46001
93451	20904	944	03102	SBP9989	46501
93452	20601	945	03301		

Table 5.1.2.7-23: Microelectronic Parameters

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np	M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
TTL					TTL				
00101-A	7.	0.04	1G	14	00203-C	7.	0.22	16G	14
00101-B	7.	0.04	1G	14	00204-E	7.	0.22	16G	16
00101-C	7.	0.04	1G	14	00204-F	7.	0.22	16G	16
00101-D	7.	0.04	1G	14	00205-A	7.	0.22	12G	14
00102-A	7.	0.08	2G	14	00205-B	7.	0.22	12G	14
00102-B	7.	0.08	2G	14	00205-C	7.	0.22	12G	14
00102-C	7.	0.08	2G	14	00205-D	7.	0.22	12G	14
00102-D	7.	0.08	2G	14	00206-A	7.	0.11	11G	14
00103-A	7.	0.12	3G	14	00206-B	7.	0.11	11G	14
00103-B	7.	0.12	3G	14	00206-C	7.	0.11	11G	14
00103-C	7.	0.12	3G	14	00206-D	7.	0.11	11G	14
00103-D	7.	0.12	3G	14	00207-A	7.	0.22	12G	14
00104-A	7.	0.16	4G	14	00207-B	7.	0.22	12G	14
00104-B	7.	0.16	4G	14	00207-C	7.	0.22	12G	14
00104-C	7.	0.16	4G	14	00207-D	7.	0.22	12G	14
00104-D	7.	0.16	4G	14	00301-A	7.	0.20	2G	14
00105-A	7.	0.24	6G	14	00301-B	7.	0.20	2G	14
00105-B	7.	0.24	6G	14	00301-C	7.	0.20	2G	14
00105-C	7.	0.24	6G	14	00301-D	7.	0.20	2G	14
00105-D	7.	0.24	6G	14	00302-A	7.	0.40	4G	14
00106-A	7.	0.12	3G	14	00302-B	7.	0.40	4G	14
00106-B	7.	0.12	3G	14	00302-C	7.	0.40	4G	14
00106-C	7.	0.12	3G	14	00302-D	7.	0.40	4G	14
00106-D	7.	0.12	3G	14	00303-A	7.	0.40	4G	14
00107-A	7.	0.16	4G	14	00303-B	7.	0.40	4G	14
00107-B	7.	0.16	4G	14	00303-C	7.	0.40	4G	14
00107-C	7.	0.16	4G	14	00303-D	7.	0.40	4G	14
00107-D	7.	0.16	4G	14	00401-A	7.	0.24	4G	14
00108-A	7.	0.24	6G	14	00401-B	7.	0.24	4G	14
00108-B	7.	0.24	6G	14	00401-C	7.	0.24	4G	14
00108-C	7.	0.24	6G	14	00401-D	7.	0.24	4G	14
00108-D	7.	0.24	6G	14	00402-E	7.	0.12	2G	16
00109-C	7.	0.16	4G	14	00402-F	7.	0.12	2G	16
00201-A	7.	0.11	8G	13	00403-A	7.	0.12	2G	14
00201-B	7.	0.11	8G	13	00403-B	7.	0.12	2G	14
00201-C	7.	0.11	8G	13	00403-C	7.	0.12	2G	14
00201-D	7.	0.11	8G	13	00403-D	7.	0.12	2G	14
00202-A	7.	0.22	16G	14	00404-A	7.	0.18	3G	14
00202-B	7.	0.22	16G	14	00404-B	7.	0.18	3G	14
00202-C	7.	0.22	16G	14	00404-C	7.	0.18	3G	14
00202-D	7.	0.22	16G	14	00404-D	7.	0.18	3G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np	M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
TTL					TTL				
00501-A	7.	0.10	6G	14	00803-B	7.	0.32	6G	14
00501-B	7.	0.10	6G	14	00803-C	7.	0.32	6G	14
00501-C	7.	0.10	6G	14	00803-D	7.	0.32	6G	14
00501-D	7.	0.10	6G	14	00804-A	7.	0.32	6G	14
00502-A	7.	0.10	6G	14	00804-B	7.	0.32	6G	14
00502-B	7.	0.10	6G	14	00804-C	7.	0.32	6G	14
00502-C	7.	0.10	6G	14	00804-D	7.	0.32	6G	14
00502-D	7.	0.10	6G	14	00805-A	7.	0.22	4G	14
00503-A	7.	0.07	5G	13	00805-B	7.	0.22	4G	14
00503-B	7.	0.07	5G	13	00805-C	7.	0.22	4G	14
00503-C	7.	0.07	5G	13	00805-D	7.	0.22	4G	14
00503-D	7.	0.07	5G	13	00901-A	7.	0.42	37G	14
00504-A	7.	0.07	4G	14	00901-B	7.	0.42	37G	14
00504-B	7.	0.07	4G	14	00901-C	7.	0.42	37G	14
00504-C	7.	0.07	4G	14	00901-D	7.	0.42	37G	14
00504-D	7.	0.07	5G	14	00902-E	7.	0.40	39G	16
00601-A	7.	0.28	21G	14	00902-F	7.	0.40	39G	16
00601-B	7.	0.28	21G	14	00903-A	7.	0.32	36G	14
00601-C	7.	0.28	21G	14	00903-B	7.	0.32	36G	14
00601-D	7.	0.28	21G	14	00903-C	7.	0.32	36G	14
00602-E	7.	0.55	36G	16	00903-D	7.	0.32	36G	14
00602-F	7.	0.55	36G	16	00904-E	7.	0.37	62G	16
00603-E	7.	0.30	22G	16	00904-F	7.	0.37	62G	16
00603-F	7.	0.30	22G	16	00905-E	7.	0.36	47G	16
00604-A	7.	0.17	14G	14	00905-F	7.	0.36	47G	16
00604-B	7.	0.17	14G	14	00906-E	7.	0.37	41G	16
00604-C	7.	0.17	14G	14	00906-F	7.	0.37	41G	16
00604-D	7.	0.17	14G	14	01001-E	7.	0.23	18G	16
00701-A	7.	0.26	4G	14	01001-F	7.	0.23	18G	16
00701-B	7.	0.26	4G	14	01002-E	7.	0.23	18G	16
00701-C	7.	0.26	4G	14	01002-F	7.	0.23	18G	16
00701-D	7.	0.26	4G	14	01003-E	7.	0.23	18G	16
00801-A	7.	0.32	6G	14	01003-F	7.	0.23	18G	16
00801-B	7.	0.32	6G	14	01004-E	7.	0.34	18G	16
00801-C	7.	0.32	6G	14	01004-F	7.	0.34	18G	16
00801-D	7.	0.32	6G	14	01005-E	7.	0.34	18G	16
00802-A	7.	0.32	6G	14	01005-F	7.	0.34	18G	16
00802-B	7.	0.32	6G	14	01006-E	7.	0.47	44G	16
00802-C	7.	0.32	6G	14	01006-F	7.	0.47	44G	16
00802-D	7.	0.32	6G	14	01007-E	7.	0.47	44G	16
00803-A	7.	0.32	6G	14	01007-E	7.	0.47	44G	16

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np	M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
TTL					TTL				
01008-E	7.	0.47	37G	16	01305-F	7.	0.50	60G	16
01008-F	7.	0.47	37G	16	01306-E	7.	0.50	57G	16
01009-A	7.	0.47	34G	14	01306-F	7.	0.50	57G	16
01009-B	7.	0.47	34G	14	01307-A	7.	0.27	15G	14
01009-C	7.	0.47	34G	14	01307-C	7.	0.27	15G	14
01009-D	7.	0.47	34G	14	01307-D	7.	0.27	15G	14
01101-J	7.	0.80	63G	24	01308-E	7.	0.49	50G	16
01101-K	7.	0.80	63G	24	01308-F	7.	0.49	50G	16
01101-L	7.	0.80	63G	24	01309-E	7.	0.49	48G	16
01101-Z	7.	0.80	63G	24	01309-F	7.	0.49	48G	16
01102-E	7.	0.80	19G	16	01401-J	7.	0.38	26G	24
01102-F	7.	0.80	19G	16	01401-K	7.	0.38	26G	24
01201-A	7.	0.22	8G	14	01401-L	7.	0.38	26G	24
01201-B	7.	0.22	8G	14	01401-Z	7.	0.38	26G	24
01201-C	7.	0.22	8G	14	01402-E	7.	0.27	17G	16
01201-D	7.	0.22	8G	14	01402-F	7.	0.27	17G	16
01202-A	7.	0.17	10G	14	01403-E	7.	0.29	16G	16
01202-B	7.	0.17	10G	14	01403-F	7.	0.29	16G	16
01202-C	7.	0.17	10G	14	01404-E	7.	0.25	16G	16
01202-D	7.	0.17	10G	14	01404-F	7.	0.25	16G	16
01203-E	7.	0.38	20G	16	01405-E	7.	0.28	19G	16
01203-F	7.	0.38	20G	16	01405-F	7.	0.28	19G	16
01204-A	7.	0.14	8G	14	01406-E	7.	0.27	17G	16
01204-B	7.	0.14	8G	14	01406-F	7.	0.27	17G	16
01204-C	7.	0.14	8G	14	01501-E	7.	0.28	24G	16
01204-D	7.	0.14	8G	14	01501-F	7.	0.28	24G	16
01205-E	7.	0.29	14G	16	01502-A	7.	0.28	24G	14
01205-F	7.	0.29	14G	16	01502-B	7.	0.28	24G	14
01301-A	7.	0.27	26G	14	01502-C	7.	0.28	24G	14
01301-B	7.	0.27	26G	14	01502-D	7.	0.28	24G	14
01301-C	7.	0.27	26G	14	01503-J	7.	0.63	56G	24
01301-D	7.	0.27	26G	14	01503-K	7.	0.63	56G	24
01302-A	7.	0.27	25G	14	01503-L	7.	0.63	56G	24
01302-B	7.	0.27	25G	14	01503-Z	7.	0.63	56G	24
01302-C	7.	0.27	25G	14	01504-E	7.	0.33	25G	16
01302-D	7.	0.27	25G	14	01504-F	7.	0.33	25G	16
01303-E	7.	0.50	60G	16	01601-A	7.	0.20	4G	14
01303-F	7.	0.50	60G	16	01601-B	7	0.20	4G	14
01304-E	7.	0.50	58G	16	01601-C	7.	0.20	4G	14
01304-F	7.	0.50	58G	16	01601-D	7.	0.20	4G	14
01305-E	7.	0.50	60G	16	01602-A	7.	0.20	4G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
TTL				
01602-B	7.	0.20	4G	14
01602-C	7.	0.20	4G	14
01602-D	7.	0.20	4G	14
01701-E	7.	0.44	36G	16
01701-F	7.	0.44	36G	16
01702-E	7.	0.26	24G	16
01702-F	7.	0.26	24G	16
01801-E	7.	0.77	100G	16
01801-F	7.	0.77	100G	16
01901-A	7.	0.27	14G	14
01901-B	7.	0.27	14G	14
01901-C	7.	0.27	14G	14
01901-D	7.	0.27	14G	14
LTTL				
02001-A	8.	0.00	1G	14
02001-B	8.	0.00	1G	14
02001-C	8.	0.00	1G	14
02001-D	8.	0.00	1G	14
02002-A	8.	0.01	2G	14
02002-B	8.	0.01	2G	14
02002-C	8.	0.01	2G	14
02002-D	8.	0.01	2G	14
02003-A	8.	0.01	3G	14
02003-B	8.	0.01	3G	14
02003-C	8.	0.01	3G	14
02003-D	8.	0.01	3G	14
02004-A	8.	0.02	4G	14
02004-B	8.	0.02	4G	14
02004-C	8.	0.02	4G	14
02004-D	8.	0.02	4G	14
02005-A	8.	0.02	6G	14
02005-B	8.	0.02	6G	14
02005-C	8.	0.02	6G	14
02005-D	8.	0.02	6G	14
02006-A	8.	0.02	4G	14
02006-B	8.	0.02	4G	14
02006-C	8.	0.02	4G	14
02006-D	8.	0.02	4G	14
02101-A	8.	0.01	8G	14

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LTTL				
02101-B	8.	0.01	8G	14
02101-C	8.	0.01	8G	14
02101-D	8.	0.01	8G	14
02102-A	8.	0.01	8G	14
02102-B	8.	0.01	8G	14
02102-C	8.	0.01	8G	14
02102-D	8.	0.01	8G	14
02103-A	8.	0.02	14G	14
02103-B	8.	0.02	14G	14
02103-C	8.	0.02	14G	14
02103-D	8.	0.02	14G	14
02104-A	8.	0.02	16G	14
02104-B	8.	0.02	16G	14
02104-C	8.	0.02	16G	14
02104-D	8.	0.02	16G	14
02105-A	8.	0.02	12G	14
02105-B	8.	0.02	12G	14
02105-C	8.	0.02	12G	14
02105-D	8.	0.02	12G	14
HTTL				
02201-A	7.	0.14	8G	14
02201-B	7.	0.14	8G	14
02201-C	7.	0.14	8G	14
02201-D	7.	0.14	8G	14
02202-A	7.	0.27	16G	14
02202-B	7.	0.27	16G	14
02202-C	7.	0.27	16G	14
02202-D	7.	0.27	16G	14
02203-A	7.	0.27	12G	14
02203-B	7.	0.27	12G	14
02203-C	7.	0.27	12G	14
02203-D	7.	0.27	12G	14
02204-E	7.	0.27	16G	16
02204-F	7.	0.27	16G	16
02205-A	7.	0.21	10G	14
02205-B	7.	0.21	10G	14
02205-C	7.	0.21	10G	14
02205-D	7.	0.21	10G	14
02206-A	7.	0.42	12G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
HTTL				
02206-B	7.	0.42	12G	14
02206-C	7.	0.42	12G	14
02206-D	7.	0.42	12G	14
02301-A	7.	0.20	1G	14
02301-B	7.	0.20	1G	14
02301-C	7.	0.20	1G	14
02301-D	7.	0.20	1G	14
02302-A	7.	0.40	2G	14
02302-B	7.	0.40	2G	14
02302-C	7.	0.40	2G	14
02302-D	7.	0.40	2G	14
02303-A	7.	0.59	3G	14
02303-B	7.	0.59	3G	14
02303-C	7.	0.59	3G	14
02303-D	7.	0.59	3G	14
02304-A	7.	0.80	4G	14
02304-B	7.	0.80	4G	14
02304-C	7.	0.80	4G	14
02304-D	7.	0.80	4G	14
02305-A	7.	1.20	6G	14
02305-B	7.	1.20	6G	14
02305-C	7.	1.20	6G	14
02305-D	7.	1.20	6G	14
02306-A	7.	0.79	4G	14
02306-B	7.	0.79	4G	14
02306-C	7.	0.79	4G	14
02306-D	7.	0.79	4G	14
02307-A	7.	0.40	2G	14
02307-B	7.	0.40	2G	14
02307-C	7.	0.40	2G	14
02307-D	7.	0.40	2G	14
02401-A	7.	0.27	2G	14
02401-B	7.	0.27	2G	14
02401-C	7.	0.27	2G	14
02401-D	7.	0.27	2G	14
LTTL				
02501-A	8.	0.07	15G	14
02501-B	8.	0.07	15G	14
02501-C	8.	0.07	15G	14

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LTTL				
02501-D	8.	0.07	15G	14
02502-A	8.	0.06	25G	14
02502-B	8.	0.06	25G	14
02503-C	8.	0.06	25G	14
02503-E	8.	0.13	48G	16
02503-F	8.	0.13	48G	16
02504-D	8.	0.06	25G	16
02504-E	8.	0.17	38G	16
02504-F	8.	0.17	38G	16
02505-E	8.	0.17	38G	16
02505-F	8.	0.17	38G	16
02601-A	7.	0.04	4G	14
02601-B	7.	0.04	4G	14
02601-C	7.	0.04	4G	14
02601-D	7.	0.04	4G	14
02701-A	7.	0.02	4G	14
02701-B	7.	0.02	4G	14
02701-C	7.	0.02	4G	14
02701-D	7.	0.02	4G	14
02801-A	8.	0.02	37G	14
02801-B	8.	0.02	37G	14
02801-C	8.	0.02	37G	14
02801-D	8.	0.02	37G	14
02802-A	7.	0.12	36G	14
02802-B	7.	0.12	36G	14
02802-C	7.	0.12	36G	14
02802-D	7.	0.12	36G	14
02803-E	7.	0.27	72G	16
02803-F	7.	0.27	72G	16
02804-E	7.	0.12	40G	16
02804-F	7.	0.12	40G	16
02805-A	7.	0.05	36G	14
02805-B	7.	0.05	36G	14
02805-C	7.	0.05	36G	14
02805-D	7.	0.05	36G	14
02901-E	7.	0.12	18G	16
02901-F	7.	0.12	18G	16
02902-E	7.	0.12	18G	16
02902-F	7.	0.12	18G	16
02903-E	7.	0.12	18G	16
02903-F	7.	0.12	18G	16

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LTTL				
02904-E	7.	0.24	44G	16
02904-F	7.	0.24	44G	16
02905-E	7.	0.24	44G	16
02905-F	7.	0.24	44G	16
02906-E	7.	0.03	18G	16
02906-F	7.	0.03	18G	16
02907-E	7.	0.07	18G	16
02907-F	7.	0.07	18G	16
DTL				
03001-A	8.	0.05	2G	14
03001-B	8.	0.05	2G	14
03001-C	8.	0.05	2G	14
03001-D	8.	0.05	2G	14
03002-A	8.	0.14	6G	14
03002-B	8.	0.14	6G	14
03002-C	8.	0.14	6G	14
03002-D	8.	0.14	6G	14
03003-A	8.	0.14	6G	14
03003-B	8.	0.14	6G	14
03003-C	8.	0.14	6G	14
03003-D	8.	0.14	6G	14
03004-A	8.	0.09	4G	14
03004-B	8.	0.09	4G	14
03004-C	8.	0.09	4G	14
03004-D	8.	0.09	4G	14
03005-A	8.	0.07	3G	14
03005-B	8.	0.07	3G	14
03005-C	8.	0.07	3G	14
03005-D	8.	0.07	3G	14
03101-A	8.	0.13	2G	14
03101-B	8.	0.13	2G	14
03101-C	8.	0.13	2G	14
03101-D	8.	0.13	2G	14
03102-A	8.	0.10	2G	14
03102-B	8.	0.10	2G	14
03102-C	8.	0.10	2G	14
03102-D	8.	0.10	2G	14
03103-A	8.	0.13	4G	14
03103-B	8.	0.13	4G	14

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
DTL				
03103-C	8.	0.13	4G	14
03103-D	8.	0.13	4G	14
03104-A	8.	0.17	4G	14
03104-B	8.	0.17	4G	14
03104-C	8.	0.17	4G	14
03104-D	8.	0.17	4G	14
03105-A	8.	0.02	2G	14
03105-B	8.	0.02	2G	14
03105-C	8.	0.02	2G	14
03105-D	8.	0.02	2G	14
03201-A	8.	0.18	6G	14
03201-B	8.	0.18	6G	14
03201-C	8.	0.18	6G	14
03201-D	8.	0.18	6G	14
03301-A	8.	0.07	8G	14
03301-B	8.	0.07	8G	14
03301-C	8.	0.07	8G	14
03301-D	8.	0.07	8G	14
03302-A	8.	0.07	8G	14
03302-B	8.	0.07	8G	14
03302-C	8.	0.07	8G	14
03302-D	8.	0.07	8G	14
03303-A	8.	0.07	8G	14
03303-B	8.	0.07	8G	14
03303-C	8.	0.07	8G	14
03303-D	8.	0.07	8G	14
03304-A	8.	0.14	16G	14
03304-B	8.	0.14	16G	14
03304-C	8.	0.14	16G	14
03304-D	8.	0.14	16G	14
03501-C	22.	0.80	18T	14
03501-G	22.	0.80	18T	8
03501-M	22.	0.80	18T	12
HTTL				
04001-A	7.	0.14	6G	14
04001-B	7.	0.14	6G	14
04001-C	7.	0.14	6G	14
04001-D	7.	0.14	6G	14
04002-A	7.	0.14	6G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
HTTL				
04002-B	7.	0.14	6G	14
04002-C	7.	0.14	6G	14
04002-D	7.	0.14	6G	14
04003-A	7.	0.14	5G	14
04003-B	7.	0.14	5G	14
04003-C	7.	0.14	5G	14
04003-D	7.	0.14	5G	14
04004-A	7.	0.14	5G	14
04004-B	7.	0.14	5G	14
04004-C	7.	0.14	5G	14
04004-D	7.	0.14	5G	14
04005-A	7.	0.08	3G	14
04005-B	7.	0.08	3G	14
04005-C	7.	0.08	3G	14
04005-D	7.	0.08	3G	14
LTTL				
04101-A	7.	0.01	6G	14
04101-B	7.	0.01	6G	14
04101-C	7.	0.01	6G	14
04101-D	7.	0.01	6G	14
04102-C	7.	0.01	5G	14
04103-A	7.	0.01	3G	14
04103-B	7.	0.01	3G	14
04103-C	7.	0.01	3G	14
04103-D	7.	0.01	3G	14
04201-A	8.	0.11	8G	14
04201-B	8.	0.11	8G	14
04201-C	8.	0.11	8G	14
04201-D	8.	0.11	8G	14
04202-A	8.	0.08	10G	14
04202-B	8.	0.08	10G	14
04202-C	8.	0.08	10G	14
04202-D	8.	0.08	10G	14
04301-E	7.	0.12	24G	16
04301-F	7.	0.12	24G	16
04401-E	7.	0.12	28G	16
04401-F	7.	0.12	28G	16
04501-E	7.	0.18	30G	16
04501-F	7.	0.18	30G	16

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LTTL				
04502-J	7.	0.34	60G	24
04502-K	7.	0.34	60G	24
04601-E	7.	0.15	16G	16
04601-F	7.	0.15	16G	16
04602-E	7.	0.14	17G	16
04602-F	7.	0.14	17G	16
04603-E	7.	0.13	19G	16
04603-F	7.	0.13	19G	16
CMOS				
05001-C	13.	0.20	4G	14
05001-D	13.	0.20	4G	14
05002-A	13.	0.20	2G	14
05002-C	13.	0.20	2G	14
05002-D	13.	0.20	2G	14
05003-A	13.	0.20	3G	14
05003-C	13.	0.20	3G	14
05003-D	13.	0.20	3G	14
05051-A	15.	0.20	4G	14
05051-C	15.	0.20	4G	14
05051-D	15.	0.20	4G	14
05052-A	15.	0.20	2G	14
05052-C	15.	0.20	2G	14
05052-D	15.	0.20	2G	14
05053-A	15.	0.20	3G	14
05053-C	15.	0.20	3G	14
05053-D	15.	0.20	3G	14
05101-A	13.	0.20	24G	14
05101-C	13.	0.20	24G	14
05101-D	13.	0.20	24G	14
05102-A	13.	0.20	30G	16
05102-C	13.	0.20	30G	16
05102-D	13.	0.20	30G	16
05103-A	13.	0.20	24G	15
05103-B	13.	0.20	24G	15
05103-D	13.	0.20	24G	15
05151-A	15.	0.20	24G	14
05151-C	15.	0.20	24G	14
05151-D	15.	0.20	24G	14
05152-A	15.	0.20	30G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np	M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
CMOS					CMOS				
05152-C	15.	0.20	30G	14	05353-A	15.	0.20	4G	14
05152-D	15.	0.20	30G	14	05353-C	15.	0.20	4G	14
05153-A	15.	0.20	24G	14	05353-D	15.	0.20	4G	14
05153-C	15.	0.20	24G	14	05354-E	15.	0.20	3G	16
05153-D	15.	0.20	24G	14	05354-F	15.	0.20	3G	16
05201-A	13	0.20	3G	12	05401-E	13.	0.20	58G	16
05201-C	13.	0.20	3G	12	05401-F	13.	0.20	58G	16
05201-D	13.	0.20	3G	12	05451-E	15.	0.20	58G	16
05202-A	13.	0.20	4G	14	05451-F	15.	0.20	58G	16
05202-C	13.	0.20	4G	14	05501-E	13.	0.20	6G	16
05202-D	13.	0.20	4G	14	05501-F	13.	0.20	6G	16
05203-A	13.	0.20	2G	12	05502-E	13.	0.20	6G	16
05203-C	13.	0.20	2G	12	05502-F	13.	0.20	6G	16
05203-D	13.	0.20	2G	12	05503-E	13.	0.20	6G	16
05204-A	13.	0.20	3G	14	05503-F	13.	0.20	6G	16
05204-C	13.	0.20	3G	14	05504-E	13.	0.20	6G	16
05204-D	13.	0.20	3G	14	05504-F	13.	0.20	6G	16
05251-A	15.	0.20	3G	14	05505-A	13.	0.20	12G	14
05251-C	15.	0.20	3G	14	05505-C	13.	0.20	12G	14
05252-D	15.	0.20	4G	14	05505-D	13.	0.20	12G	14
05253-A	15.	0.20	2G	14	05551-E	15.	0.20	6G	16
05253-C	15.	0.20	2G	14	05551-F	15.	0.20	6G	16
05253-D	15.	0.20	2G	14	05552-E	15.	0.20	6G	16
05254-A	15.	0.20	3G	14	05552-F	15.	0.20	6G	16
05254-C	15.	0.20	3G	14	05553-E	15.	0.20	6G	16
05254-D	15.	0.20	3G	14	05553-F	15.	0.20	6G	16
05301-A	13.	0.20	3G	14	05554-E	15.	0.20	6G	16
05301-C	13.	0.20	3G	14	05554-F	15.	0.20	6G	16
05301-D	13.	0.20	3G	14	05555-A	15.	0.20	12G	14
05302-E	13.	0.20	12G	16	05555-C	15.	0.20	12G	14
05302-F	13.	0.20	12G	16	05555-D	15.	0.20	12G	14
05303-A	13.	0.20	4G	14	05601-E	13.	0.20	47G	16
05303-C	13.	0.20	4G	14	05601-F	13.	0.20	47G	16
05303-D	13.	0.20	4G	14	05602-E	13.	0.20	57G	16
05304-E	13.	0.20	24G	16	05602-F	13.	0.20	57G	16
05304-F	13.	0.20	24G	16	05603-E	13.	0.20	132G	16
05351-A	15.	0.20	3G	14	05603-F	13.	0.20	132G	16
05351-C	15.	0.20	3G	14	05604-E	13.	0.20	39G	16
05351-D	15.	0.20	3G	14	05604-F	13.	0.20	39G	16
05352-E	15.	0.20	12G	14	05605-A	13.	0.20	81G	14
05352-F	15.	0.20	12G	14	05605-C	13.	0.20	81G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
CMOS				
05605-D	13.	0.20	81G	14
05651-E	15.	0.20	47G	16
05651-F	15.	0.20	47G	16
05652-E	15.	0.20	57G	16
05652-F	15.	0.20	57G	16
05653-E	15.	0.20	132G	16
05653-F	15.	0.20	132G	16
05654-E	15.	0.20	39G	16
05654-F	15.	0.20	39G	16
05655-A	15.	0.20	81G	14
05655-C	15.	0.20	81G	14
05655-D	15.	0.20	81G	14
05701-A	13.	0.20	109G	14
05701-C	13.	0.20	109G	14
05701-D	13.	0.20	109G	14
05702-E	13.	0.20	55G	16
05702-F	13.	0.20	55G	16
05703-E	13.	0.20	58G	16
05703-F	13.	0.20	58G	16
05704-E	13.	0.20	55G	16
05704-F	13.	0.20	55G	16
05705-E	13.	0.20	263G	16
05705-F	13.	0.20	263G	16
05706-J	13.	0.20	56G	24
05706-K	13.	0.20	56G	24
05751-A	15.	0.20	109G	14
05751-C	15.	0.20	109G	14
05751-D	15.	0.20	109G	14
05752-E	15.	0.20	55G	16
05752-F	15.	0.20	55G	16
05753-E	15.	0.20	58G	16
05753-F	15.	0.20	58G	16
05754-E	15.	0.20	55G	16
05754-F	15.	0.20	55G	16
05755-E	15.	0.20	263G	16
05755-F	15.	0.20	263G	16
05756-J	15.	0.20	56G	24
05756-K	15.	0.20	56G	24
05801-A	13.	0.20	4G	14
05801-C	13.	0.20	4G	14
05801-D	13.	0.20	4G	14
05802-A	13.	0.20	4G	14
05802-C	13.	0.20	4G	14
05802-D	13.	0.20	4G	14
05851-A	15.	0.20	4G	14
05851-C	15.	0.20	4G	14
05851-D	15.	0.20	4G	14
05852-A	15.	0.20	4G	14
05852-C	15.	0.20	4G	14
05852-D	15.	0.20	4G	14
05901-E	13.	0.20	38G	16
05901-F	13.	0.20	38G	16
05951-E	15.	0.20	38G	16
05951-F	15.	0.20	38G	16
ECL				
06001-E	7.	0.22	4G	16
06001-F	7.	0.22	4G	16
06002-E	7.	0.22	4G	16
06002-F	7.	0.22	4G	16
06003-E	7.	0.16	3G	16
06003-F	7.	0.16	3G	16
06004-E	7.	0.16	3G	16
06004-F	7.	0.16	3G	16
06005-E	7.	0.16	3G	16
06005-F	7.	0.16	3G	16
06006-E	7.	0.11	2G	16
06006-F	7.	0.11	2G	16
06101-E	7.	0.16	24G	16
06101-F	7.	0.16	24G	16
06102-E	7.	0.19	24G	16
06102-F	7.	0.19	24G	16
06103-E	7.	0.11	42G	16
06103-F	7.	0.11	42G	16
06104-E	7.	0.20	24G	16
06104-F	7.	0.20	24G	16
06201-E	7.	0.22	4G	16
06201-F	7.	0.22	4G	16
06202-E	7.	0.33	6G	16
06202-F	7.	0.33	6G	16
06301-E	7.	0.15	4G	16

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
ECL				
06301-F	7.	0.15	4G	16
06302-E	7.	0.13	4G	16
06302-F	7.	0.13	4G	16
STTL				
07001-A	7.	0.20	4G	14
07001-B	7.	0.20	4G	14
07001-C	7.	0.20	4G	14
07001-D	7.	0.20	4G	14
07002-A	7.	0.20	4G	14
07002-B	7.	0.20	4G	14
07002-C	7.	0.20	4G	14
07002-D	7.	0.20	4G	14
07003-A	7.	0.30	6G	14
07003-B	7.	0.30	6G	14
07003-C	7.	0.30	6G	14
07003-D	7.	0.30	6G	14
07004-A	7.	0.30	6G	14
07004-B	7.	0.30	6G	14
07004-C	7.	0.30	6G	14
07004-D	7.	0.30	6G	14
07005-A	7.	0.15	3G	14
07005-B	7.	0.15	3G	14
07005-C	7.	0.15	3G	14
07005-D	7.	0.15	3G	14
07006-A	7.	0.10	2G	14
07006-C	7.	0.10	2G	14
07006-D	7.	0.10	2G	14
07006-D	7.	0.10	2G	14
07007-A	7.	0.10	2G	14
07007-B	7.	0.10	2G	14
07007-C	7.	0.10	2G	14
07007-D	7.	0.10	2G	14
07008-A	7.	0.06	1G	14
07008-B	7.	0.06	1G	14
07008-C	7.	0.06	1G	14
07008-D	7.	0.06	1G	14
07009-E	7.	0.06	1G	16
07009-F	7.	0.06	1G	16
07010-E	7.	0.14	1G	16
07010-F	7.	0.14	1G	16
07101-A	7.	0.27	12G	14
07101-B	7.	0.27	12G	14
07101-C	7.	0.27	12G	14
07101-D	7.	0.27	12G	14
07102-E	7.	0.27	16G	16
07102-F	7.	0.27	16G	16
07103-A	7.	0.27	16G	14
07103-B	7.	0.27	16G	14
07103-C	7.	0.27	16G	14
07103-D	7.	0.27	16G	14
07104-A	7.	0.27	16G	14
07104-B	7.	0.27	16G	14
07104-C	7.	0.27	16G	14
07104-D	7.	0.27	16G	14
07105-E	7.	0.79	36G	16
07105-F	7.	0.79	36G	16
07106-E	7.	0.52	24G	16
07106-F	7.	0.52	24G	16
07201-A	7.	0.24	2G	14
07201-B	7.	0.24	2G	14
07201-C	7.	0.24	2G	14
07201-D	7.	0.24	2G	14
07301-A	7.	0.25	4G	14
07301-B	7.	0.25	4G	14
07301-C	7.	0.25	4G	14
07301-D	7.	0.25	4G	14
07401-A	7.	0.12	6G	14
07401-B	7.	0.12	6G	14
07401-C	7.	0.12	6G	14
07401-D	7.	0.12	6G	14
07402-A	7.	0.09	5G	14
07402-B	7.	0.09	5G	14
07402-C	7.	0.09	5G	14
07402-D	7.	0.09	5G	14
07403-A	7.	0.09	5G	14
07403-B	7.	0.09	5G	14
07403-C	7.	0.09	5G	14
07403-D	7.	0.09	5G	14
07501-A	7.	0.55	4G	14
07501-B	7.	0.55	4G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
STTL				
07501-C	7.	0.55	4G	14
07501-D	7.	0.55	4G	14
07502-E	7.	0.42	8G	16
07502-F	7.	0.42	8G	16
07601-E	7.	0.70	47G	16
07601-F	7.	0.70	47G	16
07602-E	7.	0.70	41G	16
07602-F	7.	0.70	41G	16
07701-E	7.	0.33	16G	16
07701-F	7.	0.33	16G	16
07702-E	7.	0.41	18G	16
07702-F	7.	0.41	18G	16
07801-J	7.	0.99	63G	24
07801-K	7.	0.99	63G	24
07801-L	7.	0.99	63G	24
07801-Z	7.	0.99	63G	24
07802-E	7.	0.99	19G	16
07802-F	7.	0.99	19G	16
07901-E	7.	0.39	17G	16
07901-F	7.	0.39	17G	16
07902-E	7.	0.39	16G	16
07902-F	7.	0.39	16G	16
07903-E	7.	0.43	15G	16
07903-F	7.	0.43	15G	16
07904-E	7.	0.34	15G	16
07904-F	7.	0.34	15G	16
07905-E	7.	0.47	17G	16
07905-F	7.	0.47	17G	16
07906-E	7.	0.55	15G	16
07906-F	7.	0.55	15G	16
07907-E	7.	0.48	15G	16
07907-F	7.	0.48	15G	16
07908-E	7.	0.55	16G	16
07908-F	7.	0.55	16G	16
08001-A	7.	0.23	3G	14
08001-B	7.	0.23	3G	14
08001-C	7.	0.23	3G	14
08001-D	7.	0.23	3G	14
08002-A	7.	0.23	3G	14
08002-B	7.	0.23	3G	14
08002-C	7.	0.23	3G	14
08002-D	7.	0.23	3G	14
08003-A	7.	0.31	4G	14
08003-B	7.	0.31	4G	14
08003-C	7.	0.31	4G	14
08003-D	7.	0.31	4G	14
08004-A	7.	0.31	4G	14
08004-B	7.	0.31	4G	14
08004-C	7.	0.31	4G	14
08004-D	7.	0.31	4G	14
08101-A	7.	0.48	2G	14
08101-B	7.	0.48	2G	14
08101-C	7.	0.48	2G	14
08101-D	7.	0.48	2G	14
08201-E	7.	0.60	31G	16
08201-F	7.	0.60	31G	16
LINEAR				
10101-A	22.	0.35	23T	14
10101-B	22.	0.35	23T	14
10101-C	22.	0.40	23T	14
10101-D	22.	0.35	23T	14
10101-G	22.	0.33	23T	8
10101-H	22.	0.33	23T	10
10101-P	22.	0.40	23T	8
10102-A	22.	0.35	46T	14
10102-B	22.	0.35	46T	14
10102-C	22.	0.40	46T	14
10102-D	22.	0.35	46T	14
10102-I	22.	0.35	46T	10
10103-C	22.	0.40	21T	14
10103-G	22.	0.33	21T	8
10103-H	22.	0.33	21T	10
10103-P	22.	0.40	21T	8
10104-C	22.	0.40	29T	14
10104-G	22.	0.33	29T	8
10104-H	22.	0.33	29T	10
10104-P	22.	0.40	29T	8
10105-E	22.	0.40	42T	16
10105-F	22.	0.40	42T	16
10106-E	22.	0.40	58T	16

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np	M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LINEAR					LINEAR				
10106-F	22.	0.40	58T	16	10407-F	7.	0.22	9T	16
10107-C	22.	0.40	36T	14	10601-C	36.	0.40	19T	14
10107-G	22.	0.33	36T	8	10601-G	36.	0.35	19T	8
10107-H	22.	0.33	36T	10	10601-G	36.	0.35	19T	8
10107-P	22.	0.40	36T	8	10601-H	36.	0.33	19T	10
10108-G	22.	0.33	46T	8	10602-C	36.	0.40	19T	14
10201-A	40.	0.35	20T	14	10602-G	36.	0.35	19T	8
10201-B	40.	0.35	20T	14	10602-H	36.	0.33	19T	7
10201-C	40	0.40	20T	14	10603-E	36.	0.40	38T	16
10201-D	40.	0.35	20T	14	10603-F	36.	0.40	38T	16
10201-H	40.	0.35	20T	10	10701-X	35.	0.89	19T	3
10201-I	40.	0.35	20T	10	10701-Y	35.	3.60	19T	3
10301-C	21.	0.40	9T	14	10702-X	35.	0.89	18T	3
10301-G	21.	0.33	9T	8	10703-X	35.	0.89	18T	3
10301-H	21.	0.33	9T	10	10704-X	35.	0.89	18T	3
10302-C	21.	0.40	18T	14	10705-X	40	0.89	18T	3
10302-F	21.	0.35	18T	16	10706-Y	35.	3.60	17T	3
10302-H	21.	0.33	18T	10	10707-Y	35.	3.60	17T	3
10303-A	30.	0.35	13T	14	10708-Y	35.	3.60	17T	3
10303-G	30.	0.33	13T	8	10709-Y	40.	3.60	17T	3
10304-G	36.	0.33	23T	8	10801-A	15.	0.35	4T	14
10304-H	36.	0.33	23T	10	10801-C	15.	0.40	4T	14
10305-E	36.	0.40	46T	16	10801-D	15.	0.35	4T	14
10305-F	36.	0.35	46T	16	10801-M	15.	0.35	4T	14
10401-A	7.	0.55	29T	14	10802-A	15.	0.35	5T	14
10401-B	7.	0.55	29T	14	10802-C	15.	0.40	5T	14
10401-C	7.	0.55	29T	14	10802-D	15.	0.35	5T	14
10401-D	7.	0.55	29T	14	10901-C	18.	0.40	23T	14
10402-A	7.	0.55	25T	14	10901-G	18.	0.30	23T	8
10402-B	7.	0.55	25T	14	10901-P	18.	0.37	23T	8
10402-C	7.	0.55	25T	14	10902-C	18.	0.40	46T	14
10402-D	7.	0.55	25T	14	10903-C	18.	0.40	23T	14
10403-E	7.	0.40	6T	16	11001-A	22.	0.35	88T	14
10403-F	7.	0.40	6T	16	11001-C	22.	0.40	88T	14
10404-E	7.	0.40	35T	16	11001-D	22.	0.35	88T	14
10404-F	7.	0.40	35T	16	11002-A	22.	0.35	88T	14
10405-E	7.	0.40	8T	16	11002-C	22.	0.40	98T	14
10405-F	7.	0.40	8T	16	11002-D	22.	0.35	88T	14
10406-E	7.	0.22	9T	16	11003-A	22.	0.35	68T	14
10406-F	7.	0.22	9T	16	11003-C	22.	0.40	68T	14
10407-E	7.	0.22	9T	16	11003-D	22.	0.35	68T	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LINEAR				
11004-C	22.	0.40	60T	14
11005-A	36.	0.35	102T	14
11005-C	36.	0.40	102T	14
11005-D	36.	0.35	102T	14
11101-A	36.	0.35	22T	14
11101-C	36.	0.40	22T	14
11101-D	36.	0.35	22T	14
11101-I	36.	0.35	22T	10
11102-A	36.	0.35	22T	14
11102-C	36.	0.40	22T	14
11102-D	36.	0.35	22T	14
11102-I	36.	0.35	22T	10
11103-A	36.	0.35	30T	14
11103-D	36.	0.35	30T	14
11103-E	36.	0.40	30T	16
11104-A	36.	0.35	30T	14
11104-D	36.	0.35	30T	14
11104-E	36.	0.40	30T	16
11105-A	36.	0.35	15T	14
11105-C	36.	0.40	15T	14
11105-D	36.	0.35	15T	14
11105-I	36.	0.35	15T	10
11106-A	36.	0.35	15T	14
11106-C	36.	0.40	15T	14
11106-D	36.	0.35	15T	14
11106-I	36.	0.35	15T	10
11107-A	36.	0.35	30T	14
11107-C	36.	0.40	30T	14
11107-D	36.	0.35	30T	14
11108-A	36.	0.35	30T	14
11108-C	36.	0.40	30T	14
11108-D	36.	0.35	30T	14
11201-A	36.	0.35	32T	14
11201-C	36.	0.40	32T	14
11201-D	36.	0.35	32T	14
11202-G	36.	0.33	16T	8
11202-P	36.	0.40	16T	8
11301-E	36.	0.40	84T	16
11302-E	36.	0.40	84T	16
11401-G	22.	0.33	19T	8
11401-H	22.	0.33	19T	10
11401-P	22.	0.40	19T	8
11402-G	22.	0.33	19T	8
11402-H	22.	0.33	19T	10
11402-P	22.	0.40	19T	8
11403-G	22.	0.33	19T	8
11403-H	22.	0.33	19T	10
11403-P	22.	0.40	19T	8
11404-G	22.	0.33	19T	8
11405-G	22.	0.33	19T	8
11405-H	22	0.33	19T	10
11405-P	22.	0.40	19T	8
11406-G	22.	0.33	19T	8
11406-H	22.	0.33	19T	10
11406-P	22.	0.40	19T	8
11501-X	10.	0.89	23T	3
11502-X	17.	0.89	23T	3
11503-X	20.	0.89	23T	3
11504-X	29.	0.89	23T	3
11505-Y	10.	3.60	21T	3
11506-Y	17.	3.60	21T	3
11507-Y	20.	3.60	21T	3
11508-Y	29.	3.60	21T	3
CMOS				
11601-C	15.	0.40	42T	14
11601-D	15.	0.35	42T	14
11601-I	15.	0.25	42T	10
11602-C	15.	0.40	27T	14
11602-D	15.	0.35	27T	14
11602-I	15.	0.25	27T	10
11603-C	15.	0.40	54T	14
11603-D	15.	0.35	54T	14
11604-C	15.	0.40	54T	14
11604-D	15.	0.35	54T	14
11605-C	15.	0.40	38T	14
11605-D	15.	0.35	38T	14
11605-I	15.	0.25	38T	10
11606-C	15.	0.40	25T	14
11606-D	15.	0.35	25T	14
11606-I	15.	0.25	25T	10

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
CMOS				
11607-C	15.	0.40	50T	14
11607-D	15.	0.35	50T	14
11608-C	15.	0.40	50T	14
11608-D	15.	0.35	50T	14
LINEAR				
11701-X	40.	0.89	17T	4
11702-X	40.	3.60	17T	4
11703-X	40.	0.89	26T	3
11704-Y	40.	3.60	26T	3
11801-X	40.	0.89	23T	4
11802-Y	40.	3.60	23T	4
11803-X	40.	0.89	30T	3
11804-Y	40.	3.60	30T	3
11901-G	36.	0.33	33T	8
11901-P	36.	0.40	33T	8
11902-C	36.	0.40	66T	14
11902-G	36.	0.33	66T	8
11902-P	36.	0.40	66T	8
11903-C	36.	0.40	132T	14
11903-D	36.	0.35	132T	14
11904-G	36.	0.33	28T	8
11904-P	36.	0.40	28T	8
11905-C	36.	0.40	54T	14
11905-G	36.	0.33	54T	8
11905-P	36.	0.40	54T	8
11906-C	36.	0.40	124T	14
11906-D	36.	0.35	124T	14
12201-G	40.	0.30	50T	8
12201-H	40.	0.30	50T	14
12202-G	40.	0.30	40T	8
12202-H	40.	0.30	40T	8
12203-G	40.	0.30	40T	8
12203-H	40.	0.30	40T	8
12204-G	40.	0.30	30T	8
12204-H	40.	0.30	30T	8
12205-G	40.	0.30	30T	8
12205-H	40.	0.30	30T	8
12206-G	40.	0.30	31T	8
12206-H	40.	0.30	31T	8

M38510/ XXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
CMOS				
12301-C	15.	0.40	36T	14
12301-I	15.	0.35	36T	10
12302-E	30.	0.40	72T	16
12303-C	15.	0.40	18T	14
12303-I	15.	0.35	18T	10
12304-E	15.	0.40	18T	16
LINEAR				
12401-X	30.	0.12	19T	2
12401-Y	30.	0.14	19T	4
12401-G	30.	0.18	19T	8
12402-X	30.	0.12	8T	2
12402-Y	30.	0.14	8T	4
12402-G	30.	0.18	8T	8
12403-X	30.	0.12	21T	2
12403-Y	30.	0.14	21T	4
12403-G	30.	0.18	21T	8
12404-X	30.	0.12	19T	2
12404-Y	30.	0.14	19T	4
12404-G	30.	0.18	19T	8
12406-X	30.	0.12	8T	2
12406-Y	30.	0.14	8T	4
12406-G	30.	0.18	8T	8
12501-G	15.	0.33	62T	8
12501-P	15.	0.33	62T	8
12502-P	15.	0.40	61T	8
12601-E	40.	0.40	71T	16
12801-G	30.	0.33	16T	8
12802-G	30.	0.33	16T	8
12901-C	7.	0.27	10T	14
12901-P	7.	0.21	10T	8
12902-C	7.	0.27	10T	14
12902-P	7.	0.21	10T	8
12903-C	7.	0.27	14T	14
12903-P	7.	0.21	14T	8
12904-C	7.	0.27	14T	14
12904-P	7.	0.21	14T	8
12905-C	7.	0.27	18T	14
12905-P	7.	0.21	18T	8
12906-C	7.	0.27	10T	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LINEAR				
12906-P	7.	0.21	10T	8
12907-C	7.	0.27	10T	14
12907-P	7.	0.21	10T	8
12908-C	7.	0.27	14T	14
12908-P	7.	0.21	14T	8
12909-C	7.	0.27	14T	14
12909-P	7.	0.21	14T	8
12910-C	7.	0.27	18T	14
12910-P	7.	0.21	18T	8
13001-E	25.	1.40	32T	16
13002-E	7.	1.40	32T	16
13003-E	7.	1.40	32T	16
13101-G	22.	0.33	21T	8
13101-P	22.	0.40	21T	8
13102-G	22.	0.33	42T	8
13102-P	22.	0.40	42T	8
13301-E	16.5	0.50	96G	16
13301-Z	16.5	0.50	96G	16
13401-V	7.	0.80	173G	19
13901-I	22.	0.33	49T	10
13901-C	22.	0.40	49T	14
13902-I	22.	0.33	49T	10
13902-C	22.	0.40	49T	14
13903-I	22.	0.33	28T	10
13903-C	22.	0.40	28T	14
14103-E	50.	1.00	7T	16
TTL				
15001-E	7.	0.49	31G	16
15001-F	7.	0.49	31G	16
15002-E	7.	0.49	32G	16
15002-F	7.	0.49	32G	16
15101-A	7.	0.18	2G	14
15101-B	7.	0.18	2G	14
15101-C	7.	0.18	2G	14
15101-D	7.	0.18	2G	14
15102-A	7.	0.18	6G	14
15102-B	7.	0.18	6G	14
15102-C	7.	0.18	6G	14
15102-D	7.	0.18	6G	14

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
TTL				
15103-A	7.	0.18	4G	14
15103-B	7.	0.18	4G	14
15103-C	7.	0.18	4G	14
15103-D	7.	0.18	4G	14
15201-J	7.	0.27	21G	24
15201-K	7.	0.27	21G	24
15201-L	7.	0.27	21G	24
15201-Z	7.	0.27	21G	24
15202-E	7.	0.20	15G	16
15202-F	7.	0.20	15G	16
15203-E	7.	0.20	15G	16
15203-F	7.	0.20	15G	16
15204-A	7.	0.14	15G	14
15204-B	7.	0.14	15G	14
15204-C	7.	0.14	15G	14
15204-D	7.	0.14	15G	14
15205-E	7.	0.19	18G	16
15205-F	7.	0.19	18G	16
15206-E	7.	0.19	18G	16
15206-F	7.	0.19	18G	16
15301-C	7.	0.30	4G	14
15301-D	7.	0.30	4G	14
15302-C	7.	0.35	4G	14
15302-D	7.	0.35	4G	14
HTTL				
15501-A	7.	0.35	4G	14
15501-B	7.	0.35	4G	14
15501-C	7.	0.35	4G	14
15501-D	7.	0.35	4G	14
15502-A	7.	0.26	3G	14
15502-B	7.	0.26	3G	14
15502-C	7.	0.26	3G	14
15502-D	7.	0.26	3G	14
15503-A	7.	0.18	2G	14
15503-B	7.	0.18	2G	14
15503-C	7.	0.18	2G	14
15503-D	7.	0.18	2G	14
15504-A	7.	0.35	4G	14
15504-B	7.	0.35	4G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
HTTL				
15504-D	7.	0.35	4G	14
TTL				
15601-E	7.	0.39	31G	16
15601-F	7.	0.39	31G	16
15602-E	7.	0.33	29G	16
15602-F	7.	0.33	29G	16
15603-E	7.	0.42	24G	16
15603-F	7.	0.42	24G	16
15701-E	7.	0.74	98G	16
15701-F	7.	0.74	98G	16
15801-E	7.	0.28	18G	16
15801-F	7.	0.28	18G	16
15802-E	7.	0.40	46G	16
15802-F	7.	0.40	46G	16
15901-E	7.	0.47	40G	16
15901-F	7.	0.47	40G	16
15902-E	7.	0.42	72G	16
15902-F	7.	0.42	72G	16
16001-E	7.	0.47	59G	16
16001-F	7.	0.47	59G	16
16101-A	7.	0.21	4G	14
16101-B	7.	0.21	4G	14
16101-C	7.	0.21	4G	14
16101-D	7.	0.21	4G	14
16201-A	7.	0.32	4G	14
16201-B	7.	0.32	4G	14
16201-C	7.	0.32	4G	14
16201-D	7.	0.32	4G	14
16301-E	7.	0.28	7G	16
16301-F	7.	0.28	7G	16
16302-E	7.	0.55	7G	16
16302-F	7.	0.55	7G	16
16303-E	7.	0.28	8G	16
16303-F	7.	0.28	8G	16
16304-E	7.	0.16	8G	16
16304-F	7.	0.16	8G	16

M38510/ XXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
CMOS				
17001-A	15.	0.20	4G	14
17001-C	15.	0.20	4G	14
17001-D	15.	0.20	4G	14
17002-C	15.	0.20	2G	14
17002-D	15.	0.20	2G	14
17003-C	15.	0.20	3G	14
17003-D	15.	0.20	3G	14
17101-A	15.	0.20	4G	14
17101-C	15.	0.20	4G	14
17101-D	15.	0.20	4G	14
17102-A	15.	0.20	2G	14
17102-C	15.	0.20	2G	14
17102-D	15.	0.20	2G	14
17103-A	15.	0.20	3G	14
17103-C	15.	0.20	3G	14
17103-D	15.	0.20	3G	14
17201-A	15.	0.20	6G	14
17201-C	15.	0.20	6G	14
17201-D	15.	0.20	6G	14
17202-A	15.	0.20	5G	14
17202-C	15.	0.20	5G	14
17202-D	15.	0.20	5G	14
17203-A	15.	0.20	4G	14
17203-C	15.	0.20	4G	14
17203-D	15.	0.20	4G	14
17204-A	15.	0.20	4G	14
17204-C	15.	0.20	4G	14
17204-D	15.	0.20	4G	14
17301-J	15.	0.20	120G	24
17301-K	15.	0.20	120G	24
17301-X	15.	0.20	120G	24
17301-Y	15.	0.20	120G	24
17302-J	15.	0.20	104G	24
17302-K	15.	0.20	104G	24
17302-X	15.	0.20	104G	24
17302-Y	15.	0.20	104G	24
17303-E	15.	0.20	34G	16
17303-F	15.	0.20	34G	16
17304-E	15.	0.20	34G	16
17304-F	15.	0.20	34G	16

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
CMOS				
17305-E	15.	0.20	26G	16
17305-F	15.	0.20	26G	16
17401-A	15.	0.20	6G	14
17401-C	15.	0.20	6G	14
17401-D	15.	0.20	6G	14
17402-A	15.	0.20	6G	14
17402-C	15.	0.20	6G	14
17402-D	15.	0.20	6G	14
17403-E	15.	0.20	12G	16
17403-F	15.	0.20	12G	16
17404-E	15.	0.20	32G	16
17404-F	15.	0.20	32G	16
17501-E	15.	0.20	52G	16
17501-F	15.	0.20	52G	16
17502-C	15.	0.20	20G	14
17502-D	15.	0.20	20G	14
17503-C	15.	0.20	21G	14
17503-D	15.	0.20	21G	14
17504-E	15.	0.20	20G	16
17504-F	15.	0.20	20G	16
17505-E	15.	0.20	36G	16
17505-F	15.	0.20	36G	16
17601-E	15.	0.20	76G	16
17601-F	15.	0.20	76G	16
17602-J	15.	0.20	56G	24
17602-K	15.	0.20	56G	24
17602-Z	15.	0.20	56G	24
17701-A	15.	0.20	4G	14
17701-C	15.	0.20	4G	14
17701-D	15.	0.20	4G	14
17702-A	15.	0.20	6G	14
17702-C	15.	0.20	6G	14
17702-D	15.	0.20	6G	14
17801-J	15.	0.20	80G	24
17801-K	15.	0.20	80G	24
17801-Z	15.	0.20	80G	24
17802-J	15.	0.20	92G	24
17802-K	15.	0.20	92G	24
17802-Z	15.	0.20	92G	24
17803-E	15.	0.20	41G	16
17803-F	15.	0.20	41G	16

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
CMOS				
19001-X	30.	1.20	52T	28
19002-X	30.	1.20	52T	28
19003-X	30.	1.20	36T	28
19004-X	30.	1.20	36T	28
19005-E	30.	0.73	28T	16
19006-E	30.	0.73	18T	16
TTL PROM				
20101-J	7.	0.58	512B	24
20101-K	7.	0.58	512B	24
20101-Z	7.	0.58	512B	24
20102-J	7.	0.58	512B	24
20102-K	7.	0.58	512B	24
20102-Z	7.	0.58	512B	24
20201-E	7.	0.72	1024B	16
20201-F	7.	0.72	1024B	16
20202-E	7.	0.72	1024B	16
20202-F	7.	0.72	1024B	16
STTL PROM				
20301-E	7.	0.74	1024B	16
20301-F	7.	0.74	1024B	16
20302-E	7.	0.74	1024B	16
20302-F	7.	0.74	1024B	16
20303-E	7.	0.74	1024B	16
20303-F	7.	0.74	1024B	16
20304-E	7.	0.74	1024B	16
20304-F	7.	0.74	1024B	16
20401-E	7.	0.79	2048B	16
20401-F	7.	0.79	2048B	16
20402-E	7.	0.79	2048B	16
20402-F	7.	0.79	2048B	16
20601-V	7.	0.79	4096B	18
20601-Z	7.	0.79	4096B	18
20602-V	7.	0.79	4096B	18
20602-Z	7.	0.79	4096B	18
20603-E	7.	0.79	4096B	16
20603-F	7.	0.79	4096B	16
20701-E	7.	0.74	256B	16

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
STTL PROM				
20701-F	7.	0.74	256B	16
20702-E	7.	0.74	256B	16
20702-F	7.	0.74	256B	16
20801-J	7.	1.00	4096B	24
20801-K	7.	1.00	4096B	24
20801-X	7.	1.00	4096B	24
20802-J	7.	1.00	4096B	24
20802-K	7.	1.00	4096B	24
20802-X	7.	1.00	4096B	24
20803-J	7.	1.00	4096B	24
20803-K	7.	1.00	4096B	24
20803-X	7.	1.00	4096B	24
20804-Y	7.	1.00	4096B	20
20805-Y	7.	1.00	4096B	20
20901-V	7.	0.72	8192B	18
20902-V	7.	0.72	8192B	18
20903-J	7.	1.40	8192B	24
20903-K	7.	1.40	8192B	24
20904-J	7.	1.40	8192B	24
20904-K	7.	1.40	8192B	24
20905-J	7.	1.40	8192B	24
20905-K	7.	1.40	8192B	24
20906-J	7.	1.40	8192B	24
20906-K	7.	1.40	8192B	24
20907-J	7.	1.40	8192B	24
20907-K	7.	1.40	8192B	24
20908-J	7.	1.40	8192B	24
20908-K	7.	1.40	8192B	24
21001-J	7.	1.00	16384B	24
21001-K	7.	1.00	16384B	24
21002-J	7.	1.00	16384B	24
21002-K	7.	1.00	16384B	24
21003-J	7.	1.00	16384B	24
21003-K	7.	1.00	16384B	24
21004-J	7.	1.00	16384B	24
21004-K	7.	1.00	16384B	24
21005-J	7.	1.00	16384B	24
21005-K	7.	1.00	16384B	24

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
CMOS EPROM				
21901-J	8.	1.80	4096B	24
NMOS EPROM				
22001-J	30.	1.80	8192B	24
22101-J	6.	1.90	16384B	24
22201-J	6.	1.00	32768B	24
22202-J	6.	1.00	32768B	24
22601-J	6.	1.00	16384B	24
TTL RAM				
23001-E	7.	0.80	256B	16
23001-F	7.	0.80	256B	16
23002-E	7.	0.80	256B	16
23002-F	7.	0.80	256B	16
23003-E	7.	0.80	256B	16
23003-F	7.	0.80	256B	16
23004-E	7.	0.41	256B	16
23004-F	7.	0.41	256B	16
23101-E	7.	0.94	1024B	16
23101-F	7.	0.94	1024B	16
23101-Y	7.	0.94	1024B	24
23102-E	7.	0.94	1024B	16
23102-F	7.	0.94	1024B	16
23102-Y	7.	0.94	1024B	24
LSTTL RAM				
23103-E	7.	0.41	1024B	16
23103-F	7.	0.41	1024B	16
23103-Y	7.	0.41	1024B	24
23104-E	7.	0.41	1024B	16
23104-F	7.	0.41	1024B	16
23104-Y	7.	0.41	1024B	24
STTL RAM				
23105-E	7.	0.94	1024B	16
23105-F	7.	0.94	1024B	16
23105-Y	7.	0.94	1024B	24

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
STTL RAM				
23106-E	7.	0.94	1024B	16
23106-F	7.	0.94	1024B	16
23106-Y	7.	0.94	1024B	24
23107-E	7.	0.94	1024B	16
23107-F	7.	0.94	1024B	16
23107-Y	7.	0.94	1024B	24
23108-E	7.	0.94	1024B	16
23108-F	7.	0.94	1024B	16
23108-Y	7.	0.94	1024B	24
23109-W	7.	0.94	1024B	22
23109-X	7.	0.94	1024B	24
23109-Y	7.	0.94	1024B	24
23110-W	7.	0.94	1024B	22
23110-X	7.	0.94	1024B	24
23110-Y	7.	0.94	1024B	24
LSTTL RAM				
23111-W	7.	0.50	1024B	22
23111-X	7.	0.50	1024B	24
23111-Y	7.	0.50	1024B	24
23112-W	7.	0.50	1024B	22
23112-X	7.	0.50	1024B	24
23112-Y	7.	0.50	1024B	24
23113-E	7.	0.41	1024B	16
23113-F	7.	0.41	1024B	16
STTL				
23114-W	7.	0.94	1024B	22
23114-Y	7.	0.94	1024B	24
LSTTL				
23115-W	7.	0.50	1024B	22
23115-Y	7.	0.50	1024B	24
23115-X	7.	0.50	1024B	24
STTL RAM				
23201-X	7.	0.94	576B	28
23201-Y	7.	0.94	576B	28
23201-Z	7.	0.94	576B	28
NMOS RAM				
23501-U	20.	1.00	4096B	24
23501-W	20.	1.00	4096B	22
23502-U	20.	1.00	4096B	24
23502-V	20.	1.00	4096B	18
23502-U	20.	1.00	4096B	24
23503-W	20.	1.00	4096B	22
23504-U	20.	1.00	4096B	24
23504-V	20.	1.00	4096B	18
23505-W	20.	1.00	4096B	22
23506-W	20.	1.00	4096B	22
23601-W	20.	1.00	4096B	22
23602-E	20.	1.00	4096B	16
23603-W	20.	1.00	4096B	22
23604-E	20.	1.00	4096B	16
23701-X	7.	0.60	4096B	22
23702-X	7.	0.60	4096B	22
23703-W	7.	0.69	4096B	22
23703-X	7.	0.69	4096B	22
23704-W	7.	0.69	4096B	22
23704-X	7.	0.69	4096B	22
23705-X	7.	0.39	4096B	22
23706-X	7.	0.39	4096B	22
23707-W	7.	0.44	4096B	22
23707-X	7.	0.44	4096B	22
23708-W	7.	0.44	4096B	22
23708-X	7.	0.44	4096B	22
23709-X	7.	0.60	4096B	22
23710-X	7.	0.60	4096B	22
23711-W	7.	0.69	4096B	22
23711-X	7.	0.69	4096B	22
23712-W	7.	0.69	4096B	22
23712-X	7.	0.69	4096B	22
23713-X	7.	0.39	4096B	22
23714-X	7.	0.39	4096B	22
23715-W	7.	0.44	4096B	22
23715-X	7.	0.44	4096B	22

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
NMOS RAM				
23716-W	7.	0.44	4096B	22
23716-X	7.	0.44	4096B	22
23801-V	7.	1.20	4096B	18
23801-Z	7.	1.20	4096B	18
23802-V	7.	1.00	4096B	18
23802-Z	7.	1.00	4096B	18
23803-V	7.	1.20	4096B	18
23804-V	7.	1.00	4096B	18
23805-V	7.	1.20	4096B	18
23806-V	7.	1.20	4096B	18
23807-V	7.	1.20	4096B	18
CMOS RAM				
23901-E	7.	0.20	1024B	16
23901-F	7.	0.20	1024B	16
23902-V	7.	0.20	1024B	18
NMOS RAM				
24001-E	20.	1.00	16384B	16
24001-F	20.	1.00	16384B	16
24001-Z	20.	1.00	16384B	18
24002-E	20.	1.00	16384B	16
24002-F	20.	1.00	16384B	16
24002-Z	20.	1.00	16384B	18
24003-E	20.	1.00	16384B	16
24003-F	20.	1.00	16384B	16
24003-Z	20.	1.00	16384B	18
24401-E	7.	1.00	65536B	16
24401-Z	7.	1.00	65536B	18
24402-E	7.	1.00	65536B	16
24402-Z	7.	1.00	65536B	18
24403-E	7.	1.00	65536B	16
24403-Z	7.	1.00	65536B	18
CMOS				
24501-V	7.	0.20	4096B	18
24502-V	7.	0.20	4096B	18
29101-J	7.	1.00	16384B	24

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
CMOS				
29101-X	7.	1.00	16384B	32
29102-J	7.	1.00	16384B	24
29102-X	7.	1.00	16384B	32
29103-R	7.	1.00	16384B	20
29103-Y	7.	1.00	16384B	20
29104-J	7.	1.00	16384B	24
29104-X	7.	1.00	16384B	32
29105-J	7.	1.00	16384B	24
29105-X	7.	1.00	16384B	32
29106-R	7.	1.00	16384B	20
29106-Y	7.	1.00	16384B	20
LSTTL				
30001-A	7.	0.02	4G	14
30001-B	7.	0.02	4G	14
30001-C	7.	0.02	4G	14
30001-D	7.	0.02	4G	14
30002-A	7.	0.02	4G	14
30002-B	7.	0.02	4G	14
30002-C	7.	0.02	4G	14
30002-D	7.	0.02	4G	14
30003-A	7.	0.04	6G	14
30003-B	7.	0.04	6G	14
30003-C	7.	0.04	6G	14
30003-D	7.	0.04	6G	14
30004-A	7.	0.04	6G	14
30004-B	7.	0.04	6G	14
30004-C	7.	0.04	6G	14
30004-D	7.	0.04	6G	14
30005-A	7.	0.02	3G	14
30005-B	7.	0.02	3G	14
30005-C	7.	0.02	3G	14
30005-D	7.	0.02	3G	14
30006-A	7.	0.02	3G	14
30006-B	7.	0.02	3G	14
30006-C	7.	0.02	3G	14
30006-D	7.	0.02	3G	14
30007-A	7.	0.01	2G	14
30007-B	7.	0.01	2G	14
30007-C	7.	0.01	2G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np	M38510/ XXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LSTTL					LSTTL				
30007-D	7.	0.01	2G	14	30201-C	7.	0.03	2G	14
30008-A	7.	0.01	2G	14	30201-D	7.	0.03	2G	14
30008-B	7.	0.01	2G	14	30202-A	7.	0.07	4G	14
30008-C	7.	0.01	2G	14	30202-B	7.	0.07	4G	14
30008-D	7.	0.01	2G	14	30202-C	7.	0.07	4G	14
30009-A	7.	0.01	1G	14	30202-D	7.	0.07	4G	14
30009-B	7.	0.01	1G	14	30203-A	7.	0.07	4G	14
30009-C	7.	0.01	1G	14	30203-B	7.	0.07	4G	14
30009-D	7.	0.01	1G	14	30203-C	7.	0.07	4G	14
30101-A	7.	0.05	16G	14	30203-D	7.	0.07	4G	14
30101-B	7.	0.05	16G	14	30204-A	7.	0.07	4G	14
30101-C	7.	0.05	16G	14	30204-B	7.	0.07	4G	14
30101-D	7.	0.05	16G	14	30204-C	7.	0.07	4G	14
30102-A	7.	0.05	12G	14	30204-D	7.	0.07	4G	14
30102-B	7.	0.05	12G	14	30301-A	7.	0.03	4G	14
30102-C	7.	0.05	12G	14	30301-B	7.	0.03	4G	14
30102-D	7.	0.05	12G	14	30301-C	7.	0.03	4G	14
30103-E	7.	0.05	16G	16	30301-D	7.	0.03	4G	14
30103-F	7.	0.05	16G	16	30302-A	7.	0.04	3G	14
30104-A	7.	0.05	16G	14	30302-B	7.	0.04	3G	14
30104-B	7.	0.05	16G	14	30302-C	7.	0.04	3G	14
30104-C	7.	0.05	16G	14	30302-D	7.	0.04	3G	14
30104-D	7.	0.05	16G	14	30303-A	7.	0.07	4G	14
30105-A	7.	0.05	16G	14	30303-B	7.	0.07	4G	14
30105-B	7.	0.05	16G	14	30303-C	7.	0.07	4G	14
30105-C	7.	0.05	16G	14	30303-D	7.	0.07	4G	14
30105-D	7.	0.05	16G	14	30401-A	7.	0.02	6G	14
30106-E	7.	0.15	36G	16	30401-B	7.	0.02	6G	14
30106-F	7.	0.15	36G	16	30401-C	7.	0.02	6G	14
30107-E	7.	0.10	24G	16	30401-D	7.	0.02	6G	14
30107-F	7.	0.10	24G	16	30402-A	7.	0.01	5G	14
30108-A	7.	0.05	16G	14	30402-B	7.	0.01	5G	14
30108-B	7.	0.05	16G	14	30402-C	7.	0.01	5G	14
30108-C	7.	0.05	16G	14	30402-D	7.	0.01	5G	14
30108-D	7.	0.05	16G	14	30501-A	7.	0.06	4G	14
30109-E	7.	0.05	16G	16	30501-B	7.	0.06	4G	14
30109-F	7.	0.05	16G	16	30501-C	7.	0.06	4G	14
30110-E	7.	0.05	16G	16	30501-D	7.	0.06	4G	14
30110-F	7.	0.05	16G	16	30502-A	7.	0.06	4G	14
30201-A	7.	0.03	2G	14	30502-B	7.	0.06	4G	14
30201-B	7.	0.03	2G	14	30502-C	7.	0.06	4G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np	M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LSTTL					LSTTL				
30502-D	7.	0.06	4G	14	30903-E	7.	0.09	15G	16
30601-E	7.	0.13	47G	16	30903-F	7.	0.09	15G	16
30601-F	7.	0.13	47G	16	30904-E	7.	0.04	15G	16
30602-E	7.	0.12	41G	16	30904-F	7.	0.04	15G	16
30602-F	7.	0.12	41G	16	30905-E	7.	0.07	17G	16
30603-A	7.	0.12	37G	14	30905-F	7.	0.07	17G	16
30603-B	7.	0.12	37G	14	30906-E	7.	0.11	15G	16
30603-C	7.	0.12	37G	14	30906-F	7.	0.11	15G	16
30603-D	7.	0.12	37G	14	30907-E	7.	0.11	15G	16
30604-E	7.	0.11	39G	16	30907-F	7.	0.11	15G	16
30604-F	7.	0.11	39G	16	30908-E	7.	0.08	16G	16
30605-A	7.	0.15	36G	14	30908-F	7.	0.08	16G	16
30605-B	7.	0.15	36G	14	30909-E	7.	0.12	15G	16
30605-C	7.	0.15	36G	14	30909-F	7.	0.12	15G	16
30605-D	7.	0.15	36G	14	31001-A	7.	0.04	3G	14
30606-A	7.	0.16	48G	14	31001-B	7.	0.04	3G	14
30606-B	7.	0.16	48G	14	31001-C	7.	0.04	3G	14
30606-C	7.	0.16	48G	14	31001-D	7.	0.04	3G	14
30606-D	7.	0.16	48G	14	31002-A	7.	0.04	3G	14
30607-E	7.	0.16	48G	16	31002-B	7.	0.04	3G	14
30607-F	7.	0.16	48G	16	31002-C	7.	0.04	3G	14
30608-E	7.	0.20	62G	16	31002-D	7.	0.04	3G	14
30608-F	7.	0.20	62G	16	31003-A	7.	0.02	2G	14
30609-E	7.	0.21	68G	16	31003-B	7.	0.02	2G	14
30609-F	7.	0.21	68G	16	31003-C	7.	0.02	2G	14
30701-E	7.	0.06	16G	16	31003-D	7.	0.02	2G	14
30701-F	7.	0.06	16G	16	31004-A	7.	0.04	4G	14
30702-E	7.	0.06	18G	16	31004-B	7.	0.04	4G	14
30702-F	7.	0.06	18G	16	31004-C	7.	0.05	4G	14
30703-E	7.	0.07	18G	16	31004-D	7.	0.05	4G	14
30703-F	7.	0.07	18G	16	31005-A	7.	0.04	4G	14
30704-E	7.	0.07	44G	16	31005-B	7.	0.04	4G	14
30704-F	7.	0.07	44G	16	31005-C	7.	0.04	4G	14
30801-J	7.	0.19	63G	24	31005-D	7.	0.04	4G	14
30801-K	7.	0.19	63G	24	31101-E	7.	0.11	31G	16
30801-L	7.	0.19	63G	24	31101-F	7.	0.11	31G	16
30801-Z	7.	0.19	63G	24	31201-E	7.	0.21	42G	16
30901-E	7.	0.06	17G	16	31201-F	7.	0.21	42G	16
30901-F	7.	0.06	17G	16	31202-E	7.	0.21	42G	16
30902-E	7.	0.06	16G	16	31202-F	7.	0.21	42G	16
30902-F	7.	0.06	16G	16	31301-A	7.	0.04	2G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np	M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LSTTL					LSTTL				
31301-B	7.	0.04	2G	14	31510-A	7.	0.08	26G	14
31301-C	7.	0.04	2G	14	31510-B	7.	0.08	26G	14
31301-D	7.	0.04	2G	14	31510-C	7.	0.08	25G	14
31302-A	7.	0.12	6G	14	31510-D	7.	0.08	26G	14
31302-B	7.	0.12	6G	14	31511-E	7.	0.18	60G	16
31302-C	7.	0.12	6G	14	31511-F	7.	0.18	60G	16
31302-D	7.	0.12	6G	14	31512-E	7.	0.18	58G	16
31303-A	7.	0.08	4G	14	31512-F	7.	0.18	58G	16
31303-B	7.	0.08	4G	14	31513-E	7.	0.19	62G	16
31303-C	7.	0.08	4G	14	31513-F	7.	0.19	62G	16
31303-D	7.	0.08	4G	14	31601-E	7.	0.07	24G	16
31401-E	7.	0.11	20G	16	31601-F	7.	0.07	24G	16
31401-F	7.	0.11	20G	16	31602-E	7.	0.04	8G	16
31402-E	7.	0.15	16G	16	31602-F	7.	0.04	8G	16
31402-F	7.	0.15	16G	16	31603-E	7.	0.20	59G	16
31403-A	7.	0.06	10G	14	31603-F	7.	0.20	59G	16
31403-B	7.	0.06	10G	14	31604-E	7.	0.07	24G	16
31403-C	7.	0.06	10G	14	31604-F	7.	0.07	24G	16
31403-D	7.	0.06	10G	14	31605-E	7.	0.20	59G	16
31501-A	7.	0.08	15G	14	31605-F	7.	0.20	59G	16
31501-B	7.	0.08	15G	14	31801-E	7.	0.21	46G	16
31501-C	7.	0.08	15G	14	31801-F	7.	0.21	46G	16
31501-D	7.	0.08	15G	14	31901-E	7.	0.28	305G	16
31502-A	7.	0.08	25G	14	31901-F	7.	0.28	305G	16
31502-B	7.	0.08	25G	14	31902-E	7.	0.22	100G	16
31502-C	7.	0.08	25G	14	31902-F	7.	0.22	100G	16
31502-D	7.	0.08	25G	14	32001-A	7.	0.08	43G	14
31503-E	7.	0.18	60G	16	32001-B	7.	0.08	43G	14
31503-F	7.	0.18	60G	16	32001-C	7.	0.08	43G	14
31504-E	7.	0.18	57G	16	32001-D	7.	0.08	43G	14
31504-F	7.	0.18	57G	16	32002-A	7.	0.08	42G	14
31505-E	7.	0.19	63G	16	32002-B	7.	0.08	42G	14
31505-F	7.	0.19	63G	16	32002-C	7.	0.08	42G	14
31506-E	7.	0.19	60G	16	32002-D	7.	0.08	42G	14
31506-F	7.	0.19	60G	16	32003-A	7.	0.08	19G	14
31507-E	7.	0.19	50G	16	32003-B	7.	0.08	19G	14
31507-F	7.	0.19	50G	16	32003-C	7.	0.08	19G	14
31508-E	7.	0.19	48G	16	32003-D	7.	0.08	19G	14
31508-F	7.	0.19	48G	16	32004-A	7.	0.08	25G	14
31509-E	7.	0.19	59G	16	32004-B	7.	0.08	25G	14
31509-F	7.	0.19	59G	16	32004-C	7.	0.08	25G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LSTTL				
32004-D	7.	0.08	25G	14
32102-A	7.	0.02	4G	14
32102-B	7.	0.02	4G	14
32102-C	7.	0.02	4G	14
32102-D	7.	0.02	4G	14
32201-E	7.	0.13	7G	16
32201-F	7.	0.13	7G	16
32202-E	7.	0.12	7G	16
32202-F	7.	0.12	7G	16
32203-E	7.	0.13	8G	16
32203-F	7.	0.13	8G	16
32204-E	7.	0.12	8G	16
32204-F	7.	0.12	8G	16
32301-C	7.	0.11	4G	14
32301-D	7.	0.11	4G	14
32302-C	7.	0.12	4G	14
32302-D	7.	0.12	4G	14
32401-R	7.	0.28	10T	20
32401-S	7.	0.28	10T	20
32402-R	7.	0.30	10T	20
32402-S	7.	0.30	10T	20
32403-R	7.	0.30	10T	20
32403-S	7.	0.30	10T	20
32404-R	7.	0.30	12T	20
32404-S	7.	0.30	12T	20
32405-R	7.	0.30	12T	20
32405-S	7.	0.30	12T	20
32501-R	7.	0.15	80G	20
32501-S	7.	0.15	80G	20
32502-R	7.	0.22	74G	20
32502-S	7.	0.22	74G	20
32503-R	7.	0.22	80G	20
32503-S	7.	0.22	80G	20
32504-R	7.	0.15	90G	20
32504-S	7.	0.15	90G	20
32601-E	7.	0.06	15G	16
32601-F	7.	0.06	15G	16
32602-E	7.	0.06	15G	16
32602-F	7.	0.06	15G	16
32701-E	7.	0.14	60G	16
32701-F	7.	0.14	60G	16
32702-A	7.	0.14	66G	14
32702-B	7.	0.14	66G	14
32702-C	7.	0.14	66G	14
32702-D	7.	0.14	66G	14
32703-E	7.	0.14	82G	16
32703-F	7.	0.14	82G	16
32801-C	7.	0.30	10G	14
32801-D	7.	0.30	10G	14
32802-C	7.	0.30	10G	14
32802-D	7.	0.30	10G	14
32803-R	7.	0.52	18G	20
32803-S	7.	0.52	18G	20
32901-A	7.	0.15	46G	14
32901-B	7.	0.15	46G	14
32901-C	7.	0.15	46G	14
32901-D	7.	0.15	46G	14
ASTTL				
33001-A	7.	0.06	4G	14
33001-B	7.	0.06	4G	14
33001-C	7.	0.06	4G	14
33001-D	7.	0.06	4G	14
33001-X	7.	0.06	4G	20
33001-Y	7.	0.06	4G	20
33002-A	7.	0.08	6G	14
33002-B	7.	0.08	6G	14
33002-C	7.	0.08	6G	14
33002-D	7.	0.08	6G	14
33002-X	7.	0.08	6G	20
33002-Y	7.	0.08	6G	20
33003-A	7.	0.04	3G	14
33003-B	7.	0.04	3G	14
33003-C	7.	0.04	3G	14
33003-D	7.	0.04	3G	14
33003-X	7.	0.04	3G	20
33003-Y	7.	0.04	3G	20
33004-A	7.	0.03	2G	14
33004-B	7.	0.03	2G	14
33004-C	7.	0.03	2G	14
33004-D	7.	0.03	2G	14

Table 5.1.2.7-23: Microelectronic Parameters (continued)

M38510/ XXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
ASTTL				
33004-X	7.	0.03	2G	20
33004-Y	7.	0.03	2G	20
LSTTL				
33106-E	7.	0.15	36G	16
33106-F	7.	0.15	36G	16
33107-E	7.	0.10	24G	16
33107-F	7.	0.10	24G	16
ASTTL				
33201-R	7.	0.41	10G	20
33201-S	7.	0.41	10G	20
33202-R	7.	0.50	10G	20
33202-S	7.	0.50	10G	20
33203-R	7.	0.50	10G	20
33203-S	7.	0.50	10G	20
33301-A	7.	0.07	4G	14
33301-B	7.	0.07	4G	14
33301-C	7.	0.07	4G	14
33301-D	7.	0.07	4G	14
33401-A	7.	0.03	5G	14
33401-B	7.	0.03	5G	14
33401-C	7.	0.03	5G	14
33401-D	7.	0.03	5G	14
33501-A	7.	0.09	4G	14
33501-B	7.	0.09	4G	14
33501-C	7.	0.09	4G	14
33501-D	7.	0.09	4G	14
33601-E	7.	0.25	47G	16
33601-F	7.	0.25	47G	16
33901-E	7.	0.12	17G	16
33901-F	7.	0.12	17G	16
33902-E	7.	0.11	16G	16
33902-F	7.	0.11	16G	16
33903-E	7.	0.13	19G	16
33903-F	7.	0.13	19G	16
33904-E	7.	0.08	15G	16
33904-F	7.	0.08	15G	16
33905-E	7.	0.13	17G	16
33905-F	7.	0.13	17G	16
33906-E	7.	0.13	15G	16
33906-F	7.	0.13	15G	16
33907-E	7.	0.14	15G	16
33907-F	7.	0.14	15G	16
33908-E	7.	0.12	16G	16
33908-F	7.	0.12	16G	16
34001-A	7.	0.07	4G	14
34001-B	7.	0.07	4G	14
34001-C	7.	0.07	4G	14
34001-D	7.	0.07	4G	14
34002-A	7.	0.05	3G	14
34002-B	7.	0.05	3G	14
34002-C	7.	0.05	3G	14
34002-D	7.	0.05	3G	14
34101-A	7.	0.09	12G	14
34101-B	7.	0.09	12G	14
34101-C	7.	0.09	12G	14
34101-D	7.	0.09	12G	14
34102-E	7.	0.09	16G	16
34102-F	7.	0.09	16G	16
34103-E	7.	0.11	16G	16
34103-F	7.	0.11	16G	16
34501-A	7.	0.15	4G	14
34501-B	7.	0.15	4G	14
34501-C	7.	0.15	4G	14
34501-D	7.	0.15	4G	14
34501-X	7.	0.15	4G	20
34701-R	7.	0.18	26G	20
34701-S	7.	0.18	26G	20
LSTTL				
36001-E	7.	0.11	29G	16
36001-F	7.	0.11	29G	16
36002-E	7.	0.14	30G	16
36002-F	7.	0.14	30G	16
ALSTTL				
37001-A	7.	0.07	4G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np	M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
ALSTTL					ALSTTL				
37001-B	7.	0.07	4G	14	37302-A	7.	0.07	3G	14
37001-C	7.	0.07	4G	14	37302-B	7.	0.07	3G	14
37001-D	7.	0.07	4G	14	37302-C	7.	0.07	3G	14
37002-A	7.	0.04	3G	14	37302-D	7.	0.07	3G	14
37002-B	7.	0.04	3G	14	37401-A	7.	0.09	4G	14
37002-C	7.	0.04	3G	14	37401-B	7.	0.09	4G	14
37002-D	7.	0.04	3G	14	37401-C	7.	0.09	4G	14
37003-A	7.	0.02	2G	14	37401-D	7.	0.09	4G	14
37003-B	7.	0.02	2G	14	37402-A	7.	0.04	3G	14
37003-C	7.	0.02	2G	14	37402-B	7.	0.04	3G	14
37003-D	7.	0.02	2G	14	37402-C	7.	0.04	3G	14
37004-A	7.	0.00	1G	14	37402-D	7.	0.04	3G	14
37004-B	7.	0.00	1G	14	37501-A	7.	0.11	4G	14
37004-C	7.	0.00	1G	14	37501-B	7.	0.11	4G	14
37004-D	7.	0.00	1G	14	37501-C	7.	0.11	4G	14
37005-E	7.	0.00	1G	16	37501-D	7.	0.11	4G	14
37005-F	7.	0.00	1G	16	37701-E	7.	0.06	16G	16
37006-A	7.	0.14	6G	14	37701-F	7.	0.06	16G	16
37006-B	7.	0.14	6G	14	37901-K	7.	0.20	44G	24
37006-C	7.	0.14	6G	14	37901-L	7.	0.20	44G	24
37006-D	7.	0.14	6G	14	38301-R	7.	0.14	10G	20
37101-A	7.	0.01	6G	14	38301-S	7.	0.14	10G	20
37101-B	7.	0.01	6G	14	38302-R	7.	0.17	10G	20
37101-C	7.	0.01	6G	14	38302-S	7.	0.17	10G	20
37101-D	7.	0.01	6G	14	38303-R	7.	0.17	10G	20
37102-E	7.	0.01	8G	16	38303-S	7.	0.17	10G	20
37102-F	7.	0.01	8G	16	38401-A	7.	0.03	4G	14
37103-E	7.	0.01	8G	16	38401-B	7.	0.03	4G	14
37103-F	7.	0.01	8G	16	38401-C	7.	0.03	4G	14
37104-R	7.	0.02	42G	20	38401-D	7.	0.03	4G	14
37104-S	7.	0.02	42G	20	38402-A	7.	0.04	4G	14
37105-R	7.	0.02	42G	20	38402-B	7.	0.04	4G	14
37105-S	7.	0.02	42G	20	38402-C	7.	0.04	4G	14
37106-L	7.	0.02	62G	24	38402-D	7.	0.04	4G	14
37106-K	7.	0.02	62G	24	38403-A	7.	0.03	4G	14
37107-L	7.	0.02	62G	24	38403-B	7.	0.03	4G	14
37107-K	7.	0.02	62G	24	38403-C	7.	0.03	4G	14
37301-A	7.	0.09	4G	14	38403-D	7.	0.03	4G	14
37301-B	7.	0.09	4G	14	38404-A	7.	0.04	4G	14
37301-C	7.	0.09	4G	14	38404-B	7.	0.04	4G	14
37301-D	7.	0.09	4G	14	38404-C	7.	0.04	4G	14

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
ALSTTL				
38404-D	7.	0.04	4G	14
38405-A	7.	0.03	3G	14
38405-B	7.	0.03	3G	14
38405-C	7.	0.03	3G	14
38405-D	7.	0.03	3G	14
38406-A	7.	0.03	3G	14
38406-B	7.	0.03	3G	14
38406-C	7.	0.03	3G	14
38406-D	7.	0.03	3G	14
38407-A	7.	0.02	2G	14
38407-B	7.	0.02	2G	14
38407-C	7.	0.02	2G	14
38407-D	7.	0.02	2G	14
38408-A	7.	0.06	4G	14
38408-B	7.	0.06	4G	14
38408-C	7.	0.06	4G	14
38408-D	7.	0.06	4G	14
38409-A	7.	0.07	6G	14
38409-B	7.	0.07	6G	14
38409-C	7.	0.07	6G	14
38409-D	7.	0.07	6G	14
38410-A	7.	0.07	6G	14
38410-B	7.	0.07	6G	14
38410-C	7.	0.07	6G	14
38410-D	7.	0.07	6G	14
38411-A	7.	0.08	6G	14
38411-B	7.	0.08	6G	14
38411-C	7.	0.08	6G	14
38411-D	7.	0.08	6G	14
38412-A	7.	0.08	6G	14
38412-B	7.	0.08	6G	14
38412-C	7.	0.08	6G	14
38412-D	7.	0.08	6G	14
38501-R	7.	0.26	18G	20
38501-S	7.	0.26	18G	20
38502-R	7.	0.25	18G	20
38502-S	7.	0.25	18G	20
38503-R	7.	0.15	18G	20
38503-S	7.	0.15	18G	20
38504-R	7.	0.29	18G	20
38504-S	7.	0.29	18G	20
ALSTTL				
38505-R	7.	0.35	18G	20
38505-S	7.	0.35	18G	20
38506-C	7.	0.18	10G	14
38506-D	7.	0.18	10G	14
38507-C	7.	0.18	10G	14
38507-D	7.	0.18	10G	14
NMOS				
40001-Q	7.	1.00	1300G	40
40201-J	7.	1.00	1024G	24
40301-J	7.	1.00	16384G	24
42001-Q	20.	1.70	1100G	40
STTL				
42101-J	7.	0.80	70G	24
42101-K	7.	0.80	70G	24
42101-L	7.	0.80	70G	24
42201-E	7.	0.79	70G	16
NMOS				
42301-Z	7.	1.20	120G	28
LSTTL				
44001-Q	7.	1.60	537G	40
44001-Z	7.	1.60	537G	42
44101-T	7.	1.00	77G	24
44101-Z	7.	1.00	77G	24
44102-J	7.	1.00	85G	24
44102-Z	7.	1.00	85G	24
44103-R	7.	1.00	77G	20
44103-S	7.	1.00	77G	20
44104-J	7.	1.00	77G	24
44104-Z	7.	1.00	77G	24
44105-J	7.	1.00	85G	24
44105-Z	7.	1.00	85G	24
44106-R	7.	1.00	77G	20
44106-S	7.	1.00	77G	20

Table 5.1.2.7-23: Microelectronic Parameters
(continued)

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
LSTTL				
44201-E	7.	0.83	24G	16
44201-F	7.	0.83	24G	16
IIL				
46001-Y	6.	0.75	3100G	64
CMOS				
47001-Q	11.	0.50	1375G	40
47201-J	11.	0.50	4096G	24
47201-K	11.	0.50	4096G	24
47401-E	11.	0.50	27G	16
47401-F	11.	0.50	27G	16
NMOS				
48001-Q	5.	1.00	2833G	40
48002-Q	5.	1.00	2833G	40
48003-Q	5.	1.00	2833G	40
STTL				
50301-R	12.	2.00	34G	20
50301-Y	12.	2.00	34G	20
50203-R	12.	2.00	36G	20
50302-Y	12.	2.00	36G	20
50303-R	12.	2.00	34G	20
50303-Y	12.	2.00	34G	20
50304-R	12.	2.00	34G	20
50304-Y	12.	2.00	34G	20
50305-R	12.	2.00	35G	20
50305-Y	12.	2.00	35G	20
50306-R	12.	2.00	34G	20
50306-Y	12.	2.00	34G	20
50307-R	12.	2.00	34G	20
50307-Y	12.	2.00	34G	20
50308-R	12.	2.00	34G	20
50208-Y	12.	2.00	34G	20
50309-R	12.	2.00	34G	20
50309-Y	12.	2.00	34G	20

M38510/ XXXXXXX	Vcc (V.)	Pd (W.)	Complexity	Np
STTL				
50401-R	12.	0.10	98G	20
50401-Y	12.	0.10	98G	20
50407-R	12.	0.10	98G	20
50407-Y	12.	0.10	98G	20
50501-L	12.	1.20	100G	24
50501-3	12.	1.20	100G	28
NMOS				
52001-Q	7.	2.20	5833G	40
52001-X	7.	2.20	5833G	48
52002-Q	7.	2.20	5833G	40
52002-X	7.	2.20	5833G	48
52003-Q	7.	2.20	5833G	40
52003-X	7.	2.20	5833G	48
52004-Q	7.	2.20	5833G	40
52004-X	7.	2.20	5833G	48
CMOS				
65001-C	7.	0.30	4G	14
65001-2	7.	0.30	4G	20
65002-C	7.	0.30	3G	14
65002-2	7.	0.30	3G	20
65003-C	7.	0.30	2G	14
65003-2	7.	0.30	2G	20
65004-C	7.	0.30	1G	14
65004-2	7.	0.30	1G	20
65005-C	7.	0.30	4G	14
65005-2	7.	0.30	4G	20

5.1.2.8 Example Failure Rate Calculations for Monolithic Devices.

Example One: Bipolar VLSI

Description: A custom gate array with 54,000 gates implemented in a five year old TTL bipolar process. The package is a 64-pin hermetic DIP with solder seal for use in a space application at an average case temperature of 45°C. The device dissipates 150mW at 5 volts, and the die size is 130,000 square mils. The part is screened to S-level quality per MIL-M-38510.

From Section 5.1.2.1, the operating failure rate model is:

$$\lambda_P(t_0) = \lambda_{AC} + \lambda_{EM}(t_0)$$

$$\lambda_{AC} = \pi_Q (C_1 \pi_T + C_2 \pi_E) \pi_L$$

Table 5.1.2.7-1 Quality Level S: $\pi_Q = 0.71$

Section 5.1.2.1 $C_1 = 0.08$

Equation 5.1.2.7.4 $T_J = T_C + \Theta_{JC} \times P$

Table 5.1.2.7-4a $= 45°C + (28°C/W) \times 0.150W = 49.2°C$

Table 5.1.2.7-5 $\pi_T = 0.32$

Table 5.1.2.7-15 $C_2 = 0.025$

Table 5.1.2.7-3 $\pi_E = 0.9$

Table 5.1.2.7-2 $\pi_L = 0.37$

$\lambda_{AC} = (0.71)[(0.08)(0.32) + (0.025)(0.9)](0.37)$

$= 0.0126$ failures/10^6 hours

Table 5.1.2.7-17, Note 2 $J = .13$ Ma/cm^2 (default value)

Table 5.1.2.7-17 λ_{EM} (10K hours) = 0 failures/10^6 hours

λ_P (10K hours) = 0.0126 failures/10^6 hours

Example Two: CMOS MSI

Description: A CMOS digital timing chip (4046) in an airborne inhabited application, case temperature of 45°C, 75mW power consumption at 10 volts. The device is procured with normal manufacturer's screening consisting of final electrical test, temperature cycling, B-level burn-in and seal test. The package is a 24 pin CERDIP with glass seals. The die size is 48.4K square mils, has 1000 transistors, and an 800 angstrom gate oxide in a seven year old process.

From Section 5.1.2.2 $\lambda_p(t_0) = \lambda_{AC} + \lambda_{TDDB}(t_0) + \lambda_{EM}(t_0)$

$\lambda_{AC} = \pi_Q (C_1\pi_T + C_2\pi_E) \pi_L$

Table 5.1.2.7-1 Quality level calculated by:

Temp Cycling	- 11.6 points
Burn-in	- 10.9 points
Electrical Test	- 10.9 points
Seal Test	- 7.8 points
Total	- 40.7 points

$\pi_Q = 71.3/40.7 = 1.75$

Section 5.1.2.2 $C_1 = .02$ (1000 transistors ≈ 250 gates)

Equation 5.1.2.7.4 $T_J = T_C + \Theta_{JC} \times P$

Table 5.1.2.7-49 $= 45°C + (28°C/W) \times 0.075W = 47.1°C$

Table 5.1.2.7-9 $\pi_T = 0.26$

Table 5.1.2.7-15 $C_2 = 0.011$

Table 5.1.2.7-3 $\pi_E = 4.4$

Table 5.1.2.7-2 $\pi_L = 0.01 \exp (5.35 - 0.35 (Y)) = 0.18$

$\lambda_{AC} = (1.75)[(.02)(.26) + (.011)(4.4)](.18)$

$= 0.0169$ failures/10^6 hours

Table 5.1.2.7-16, Note 1 $E_S = .1 V_{op}/t_{ox}$

$V_{op} = 10$ volts

Table 5.1.2.7-19	t_{ox} = 1.10KÅ (worst case for 1000 transistors) E_S = 0.9 Mv/cm
Table 5.1.2.7-18, Note 1	$A = \log(6(TR)10^{-.58(\log(TR)-5.78)})$ $= 5.39 \log \mu m^2$
Table 5.1.2.7-16	λ_{TDDB} (10K hours) = 0.0 failures/10^6 hours
Table 5.1.2.7-17, Note 2	J = .13 Ma/cm^2 (default value) λ_{EM} (10K hours) = 0.0 failures/10^6 hours
	λ_P (10K hours) = 0.0169 failures/10^6 hours

Example 3: MOS Digital Microprocessor

Description: A CMOS 80386 microprocessor (three year old process) in a 124-pin pin grid array used in an office environment and screened to D-1 level. The average junction temperature is 60°C, and average power consumption is 2 watts at 5 volts. The die size is 76K $mils^2$ and it contains 275K transistors.

From Section 5.1.2.3, the part failure rate model is:

$$\lambda_p(t_0) = \lambda_{AC} + \lambda_{EM}(t_0) + \lambda_{TDDB}(t_0)$$

Section 5.1.2.3	$\lambda_{AC} = \pi_Q (C_1\pi_T + C_2\pi_E)\pi_L$
Table 5.1.2.7-1	π_Q for D-1 quality level = 6.5
Section 5.1.2.3	C_1 for > 16 bits = 0.56
Table 5.1.2.7-9	π_T for 60° T_J = 0.42
Table 5.1.2.7-15	C_2 (124 pin PGA) = 0.051
Table 5.1.2.7-3	π_E = 0.5
Table 5.1.2.7-2	π_L = 0.67
	$\lambda_{AC} = (6.5)[(.56)(.42) + (.051)(.5)](.67)$ = 1.1353 failures/10^6 hours

Table 5.1.2.7-17	$J = .125$ Ma/cm^2 (default value)
Table 5.1.2.7-17	λ_{EM}(10K hours) = 0.0 failures/10^6 hours
Equation 5.1.2.7.14	$E_S = .1\ V_{op}/t_{ox}$
Table 5.1.2.7-19	$t_{ox} = 10^{-0.405(\log(TR)-3.68)}$
	$= 1.931$ KÅ
	$E_S = 2.59$ Mv/cm
Table 5.1.2.7-18	$A = \log(4(TR)^{-.774(\log(TR)-5.5)})$
	$= 6.09 \log \mu m^2$
Table 5.1.2.7-16	λ_{TDDB}(10K hours) = 0.0
	λ_p(10K hours) = 1.1353 failures/10^6 hours

Example Four:

Description: A 128K FLOTOX EEPROM that is expected to have a T_j of 80°C, and experience 10000 read/write cycles during its lifetime. The part is exposed to an operating voltage of 5v, is "B" level quality, and has been in production for three years. It is packaged in a hermetic 28 pin DIP (glass seal), and will operate in an uninhabited aircraft environment.

1) Determine the Electromigration failure rate (λ_{EM}) from Table 5.1.2.7-17. Using the default value of .125 MA/cm^2 yields a failure rate of 0 for 90°C.

2) Determine λ_{TDDB}:
Obtain the oxide area value from Table 5.1.2.7-20. Choosing the most conservative value (largest area) yields 1,209,000 μm^2 (6.1 Log μm^2).
Obtain the gate oxide thickness from Table 5.1.2.7-21. Choosing the most conservative value (smallest thickness) yields 340 Angstroms, or 340 X 10^{-8} cm.
Determine the field stress by dividing the operating voltage by the oxide thickness. The result is 1.5 MV/cm.
Determine the λ_{TDDB} by referring to Table 5.1.2.7-16 (estimate using the 6.0 log μm^2 table). The result is 0.

3) Determine the defect failure rate $C_1\pi_T$
Refer to section 5.1.2.3.2 for C_1. Checking the appropriate table provides a value of .00339 for a 128K EEPROM.
Refer to Table 5.1.2.7-10 for π_T. This equals 12.73 for 80°C
The total defect failure rate is (.00339)(12.73) = 0.0432.

4) Determine λ_{cyc}
For a Flotox device, we need only consider the A_1B_1 term

Refer to Table 5.1.2.4-4. For a Flotox device that will be reprogrammed 10000 times, the A_1 value is .0682
Refer to Table 5.1.2.4-6. For 80°C and a 128K device, B_1 = 3.7977
λ_{cyc} = (.0682)(3.7977) = .2590

5) Determine C_2 value from 5.1.2.7-15. For a hermetic 28 pin DIP, the value is .014

6) Determine the π_E value from Table 5.1.2.7-3. π_E is 5.5 for an uninhabited aircraft environment.

7) Determine π_Q from Table 5.1.2.7-1. π_Q = 1.0 for a "B" level part

8) Determine π_L from Table 5.1.2.7-2. π_L = 0.67

9) Determine the total device failure rate:

$$\lambda_P = [(C_1)(\pi_T) + \lambda_{cyc} + (C_2)(\pi_E)] (\pi_Q)(\pi_L) + \lambda_{TDDB} + \lambda_{EM}$$

$$= [(.0432) + (.2590) + (.077)] (1.0) (0.67) + 0 + 0$$

$$= .2541 \text{ Failures Per Million Hours}$$

Example Five:

Description: A 64K MOS SRAM "D" level quality part, has been in production for 2 years, has an operating voltage of 5v, and is expected to operate at a T_j of 90°C. It is packaged in a hermetic 24 pin DIP (glass seal), and will operate in an uninhabited aircraft environment.

1) Determine the Electromigration failure rate (λ_{EM}) from Table 5.1.2.7-17. Using the default value of .125 MA/cm^2 yields a failure rate of 0 for 90°C.

2) Determine λ_{TDDB}:
Obtain the oxide area value from Table 5.1.2.7-20. Choosing the most conservative value (largest area) yields 2,482,600 μm^2 (6.4 Log μm^2)
Obtain the gate oxide thickness from Table 5.1.2.7-21. Choosing the most conservative value (smallest thickness) yields 250 Angstroms, or 250 X 10^{-8} cm
Determine the field stress by dividing the operating voltage by the oxide thickness. The result is 2.0 MV/cm
Determine the λ_{TDDB} by referring to Table 5.1.2.7-16 (estimate using the 6.5 log μm^2 table). The result is 0.

3) Determine the defect failure rate $C_1\pi_T$
Refer to Table 5.1.2.4-1 for C_1. Checking the appropriate table provides a value of .0105 for a 64K SRAM
Refer to Table 5.1.2.7-10 for π_T. This equals 26.25 for 90°C
The total defect failure rate is (.0105)(26.25) = 0.2756

4) λ_{CYC} value is 0.

5) Determine C_2 value from 5.1.2.7-15. For a hermetic 24 pin DIP, the value is .011

6) Determine the π_E value from 5.1.2.7-3. π_E is 5.5 for an uninhabited aircraft environment.

7) Determine π_Q from Table 5.1.2.7-1. π_Q = 3.3 for a "D" level part

8) Determine π_L from Table 5.1.2.7-2. π_L = 1.05

9) Determine the total device failure rate:

$$\lambda_P = [(C_1)(\pi_T) + \lambda_{cyc} + (C_2)(\pi_E)] (\pi_Q)(\pi_L) + \lambda_{TDDB} + \lambda_{EM}$$

$$= [(.2756) + (0) + (.0605)] (3.3) (1.05) + 0 + 0$$

$$= 1.1646 \text{ Failures Per Million Hours}$$

Example Six: PAL

Description: A data book shows a PAL to have 150 gates, and 24 pins. The operating junction temperature is 100°C, and operates in a ground benign environment. It is "B" Level Quality, and has been in production for four years. It is hermetically packaged in a DIP with a glass seal.

1) Determine the electromigration failure rate (λ_{EM}) from Table 5.1.2.7-17. Using the default value of .125 mA/cm^2 yields a failure rate of 0 for 100°C.

2) $\lambda_{TDDB} = 0$

3) Determine the defect failure rate $C_1 \pi_T$. Refer to Table 5.1.2.4-1 for C_1. $C_1 = 0.01047$ for a 150 gate PAL. Refer to Table 5.1.2.7-10 for π_T. $\pi_T = 52.05$ at 100°C. The total defect failure rate is (.01047)(52.05) = .5450

4) $\lambda_{CYC} = 0$

5) Determine the C_2 value from Table 5.1.2.7-15 for a hermetic 24 pin DIP, $C_2 = .011$.

6) Determine π_E from Table 5.1.2.7-3. $\pi_E = 0.5$ for a ground benign environment.

7) Determine π_Q from Table 5.1.2.7-1. $\pi_Q = 1.0$

8) Determine π_L from Table 5.1.2.7-2. $\pi_L = 0.52$

9) Determine total device failure rate.

$$\lambda_p = [(C_1)(\pi_T) + \lambda_{CYC} + (C_2)(\pi_E)] (\pi_Q)(\pi_L) + \lambda_{TDDB} + \lambda_{EM}$$
$$= [(.5450) + 0 + (.011)(0.5)] (1.0)(0.52) + 0 + 0$$
$$= .2863 \text{ Failures Per Million Hours}$$

Example Seven: GaAs Digital

Description: 10G000A Quad 3 Input Nor Gate, SSI, P_D = 875 mw, 36 I/O LCC package, maximum T_{CH} = 125°C in a ground benign environment. The process is three years old and the device is a B-level part.

$$\pi_{TA} = 0.1e^{-16220\left(\frac{1}{125+273}-\frac{1}{423}\right)} = 8.994 \times 10^{-3}$$

Table 5.1.2.7-13

$$\pi_{TP} = 0.1e^{-4980\left(\frac{1}{125+273}-\frac{1}{423}\right)} = 4.773 \times 10^{-2}$$

Table 5.1.2.7-14

Table 5.1.2.7-15 C_2 = 0.013
Table 5.1.2.7-3 π_E = 0.5
Table 5.1.2.7-1 π_Q = 1.0
Table 5.1.2.7-2 π_L = 0.67
Table 5.1.2.5-1 C_{1A} = 25.3
Table 5.1.2.5-1 C_{1P} = 0.687

$\lambda_D = [(C_{1A}\ \pi_{TA} + C_{1P}\ \pi_{TP} + C_2\ \pi_E]\ \pi_Q\ \pi_L$ (From Section 5.1.2.5)

$= [25.3\ (8.994 \times 10^{-3}) + 0.687\ (4.773 \times 10^{-2}) + 0.013\ (0.5)](1.0)(0.67)$

$= .1788$ failures/10^6 hours

Example Eight: GaAs MMIC

Description: MA4GM212 SPDT Switch, DC-12 GHz, 4 transistors, 4 inductors, 4 resistors, Maximum Input P_D = 30 dbm, 4 pin hermetic can, Maximum T_{CH} = 145°C in a ground benign environment. The process is three years old and the device is a B-level part.

Table 5.1.2.7-12 $\pi_{TA} = 0.1e^{-17380\left(\frac{1}{145+273}-\frac{1}{423}\right)} = 6.117 \times 10^{-2}$

Table 5.1.2.7-14) $\pi_{TP} = 0.1e^{-4980\left(\frac{1}{145+273}-\frac{1}{423}\right)} = 8.686 \times 10^{-2}$

Table 5.1.2.7-15 $C_2 = 0.0005$
Table 5.1.2.7-3 $\pi_E = 0.5$
Table 5.1.2.7-1 $\pi_Q = 1.0$
Table 5.1.2.7-2 $\pi_L = 0.67$
Table 5.1.2.6-2 $\pi_A = 3.0$
Table 5.1.2.6-1 $C_{1A} = 4.51$
Table 5.1.2.6-1 $C_{1P} = 2.26$

$\lambda_M = [(C_{1A}\,\pi_{TA} + C_{1P}\,\pi_{TP})\,\pi_A + C_2\,\pi_E]\,\pi_L\,\pi_Q$ (From Section 5.1.2.6)

$= [\{4.51(6.117\times10^{-2}) + 2.26\,(8.686\times10^{-2})\}\,3.0 + 0.5\,(0.0005)]\,0.67\,(1)$

$= .9492$ failures/10^6 hours

5.1.2.9 Hybrid Microcircuits

The hybrid failure rate model is:

$$\lambda_P = [\Sigma\lambda_C N_C (1 + .2\pi_E)] \pi_Q \pi_L \pi_F$$

where:

λ_P is the hybrid failure rate in failures/10^6 hours
N_C is the number of each particular component
λ_C is the specific component failure rate
π_L is the experience (learning factor) from Table 5.1.2.7-2
π_F is the circuit function factor from Table 5.1.2.9-1
π_Q is the quality factor from Table 5.1.2.7-1
π_E is the environmental factor from Table 5.1.2.7-3

5.1.2.9.1 Active Components and Capacitors

The sum of the adjusted failure rates for the active components and capacitors shall be calculated as follows:

N_C is the number of each particular component
λ_C is the failure rate contribution for a particular component predicted using the correct model from the following sections in this handbook:

Integrated Circuits	Section 5.1.2
Discrete Semiconductors	Section 5.1.3
Capacitor	Section 5.1.7

Note: Inductor and Resistor failure rates are insignificant and are not included.

When calculating λ_C for integrated circuits, use quality factor "B". For discrete semiconductors, use quality factor "JANTXV." For capacitors, use quality factor level "M." Use the environmental factor corresponding to the application environment of the hybrid, and assume a component ambient temperature equal to the temperature of the hybrid package. For IC dice let C2 = 0 when calculating λ_C.

If the maximum rated stress for a die is unknown, it shall be assumed to be the same as that for a discretely packaged die of the same type. If the same die has several ratings based on the discrete package type, the lower value will be assumed. Power rating used should be based on case temperature for discrete semiconductors.

Table 5.1.2.9-1

Circuit Function Factor

TYPE	π_F
Digital	1.0
Video, 10 MHz < f < 1 GHz	1.2
Microwave, f < 1 GHz	2.6
Linear, f < 10 MHz	5.8
Power	21

5.1.2.9.2 Chip Junction Temperature Calculation

A hybrid is normally made up of one or more substrate assemblies mounted within a sealed package. Each substrate assembly consists of active and passive chips with thick or thin film metallization mounted on the substrate, which in turn may have multiple layers of metallization and dielectric on the surface. Figure 5.1.2.9-1 is a cross-sectional view of a hybrid with a single multi-layered substrate. The layers within the hybrid are made up of various materials with different thermal characteristics. Table 5.1.2.9-2 provides a list of commonly used hybrid materials with typical thicknesses and corresponding thermal conductivities (K). The thermal resistance of each layer is determined by the expression,

$\Theta = (1/K)(L/A)$, where:

Θ is the thermal resistance of a layer in °C/Watt (°C/W)

K is the thermal conductivity of the material in watts/°C-in

L is the material thickness in inches from Table 5.1.2.9-2 (or user provided)

A is the top surface area of the chip (user provided or estimated by the following expression:

$$A=[27.8(1.5\times10^{-3} + 10^{-4}P)]^2 \text{ (square inches)}, \qquad (5.1.2.9.1)$$

where P is the number of active device pin/wire terminals)

An estimated thermal resistance value for junction to case (Θ_{JC}) can be developed for each chip in the hybrid by summing the resistances of all the material layers of the hybrid structure from the chip down to the case:

$$\Theta_{JC} = \frac{\sum_{i=1}^{n} (1/K_i)\, L_i}{A}, \qquad (5.1.2.9.2)$$

where n is the number of material layers. Then,

$$T_J = T_C + 0.9\,(\Theta_{JC})(P_D), \text{ where} \qquad (5.1.2.9.3)$$

T_J is the junction temperature of the chip (°C)
T_C is the case temperature of the hybrid (°C)
Θ_{JC} is defined as above (°C/W), and
P_D is the power dissipated by the chip (W)

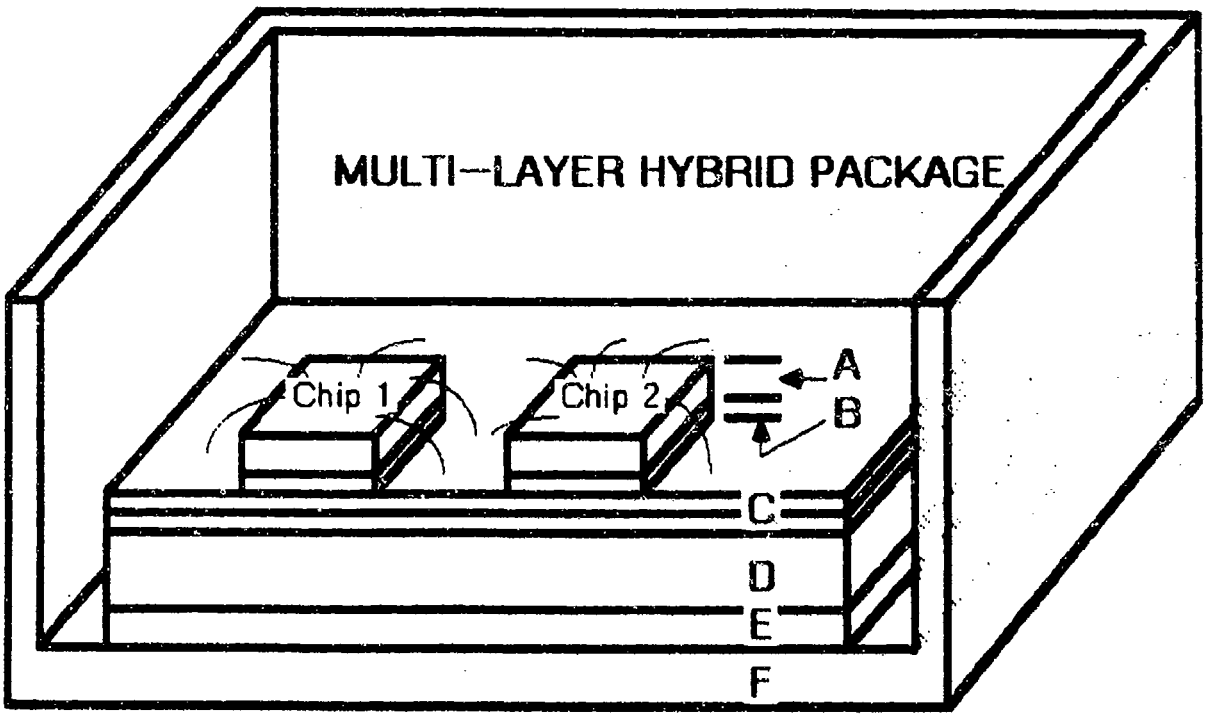
The factor of 0.9 in equation 5.1.2.9.3 represents the cosine of 26°. This angle accounts for the fact that the heat is not all conducted vertically from the chip to the case, but rather "spreads" radially as well as downward.

Table 5.1.2.9-2 Hybrid Materials

MATERIAL	TYPICAL USAGE	TYPICAL THICKNESS (")	FEATURE FROM FIG. 5.1.2.9-1	K (W/°C-in)
Silicon	chip device	0.01	A	2.20
GaAs	chip device	0.007	A	0.76
Au Eutectic	chip attach	0.0001	B	6.91
Solder	chip/substrate attach	0.003	B/E	1.27
Epoxy (diel)	chip/substrate attach	0.0035	B/E	0.006
Epoxy (Conductive)	chip attach	0.0035	B	0.15
Thick film dielectric	glass insulating layer	0.003	C	0.66
Alumina	Substrate, MHP	0.025	D	0.64
BeO	Substrate, PHP	0.025	D	6.58
Kovar	Case, MHP	0.02	F	0.425
Aluminum	Case, MHP	0.02	F	4.58
Copper	Case, PHP	0.02	F	9.96

If the hybrid internal structure cannot be determined, use the following default values for the temperature rise from case to junction: microcircuits, 10°C; transistors, 25°C; diodes, 20°C. Assume capacitors are at T_C.

Figure 5.1.2.9-1



5.1.2.9.3 Example Failure Rate Calculations for a Hybrid Device.

Microcircuit Description: Driver, Linear MHP in a hermetically sealed Kovar package. The substrate is alumina and there are two dielectric layers. The die- and substrate- attach materials are conductive epoxy and solder, respectively.

Active Components:	1 - LM106
	1 - LM741A
	2 - Si NPN Transistor, 60% stress ratio (power and voltage), linear application < 1 watt.
	2 - Si PNP Transistor, 60% stress ratio (power and voltage), linear application < 1 watt.
	2 - Si General Purpose Diodes, 60% stress ratio (power and voltage), small signal, metallurgically bonded.
Passive Components:	2 - Ceramic Chip Capacitors, 60% stress ratio, 1000 pf.
	17 - Thick Film Resistors
Environment:	Naval Unsheltered, 65°C package case temperature
Maturity:	2.1 Years in production, $\pi_L = 1.0$

Screened to MIL-STD-883, Method 5008, in accordance with Appendix G to MIL-M-38510. From Table 5.1.2.7-1, $\pi_Q = 1.0$

Example Calculation:

1. Calculate Active Device Junction Temperatures.

Since all chips are silicon, $\sum_{i=1}^{n} L_i/K_i$ is the same for each. From Table 5.1.2.9-2,

Layer	L_i/K_i	($°C\text{-}in^2/W$)
Chip	0.01/2.20	= .0045
Epoxy (Cond)	0.0035/0.15	= .0233
Dielectric(2)	(2)(0.003/0.66)	= .0091
Substrate	0.025/0.64	= .0391
Solder	0.003/1.27	= .0024
Kovar case	0.02/0.425	= .0471
Total		= .1255

	LM106	LM741A	SiNPN	SiPNP	SiDIODE
No. Pins from Tables 5.1.2.7-22/23	8	14	3	3	2
P_D (max) from Table 5.1.2.7-23	.33W	.35W	.6W	.6W	.42W
Area of Chip (sq. in.) from equation 5.1.2.9.1	.004	.0065	.0025	.0025	.0022
Θ_{JC} (°C/W), from equation 5.1.2.9.2	31.4	19.3	50.2	50.2	51.1
T_J (°C) from equation 5.1.2.9.3	74.3	71.1	92.1	92.1	84.3

2. Calculate Failure Rates.

$$\lambda_p = [\Sigma N_C \lambda_C (1 + .2\,\pi_E)]\,\pi_Q \pi_L \pi_F$$

Failure Rates for Components (λ_C):

LM106 die, 13 transistors, page 5.1.2.2-1:

$$\pi_Q\,[C_1\pi_T + C_2\pi_E]\,\pi_L$$

$$1.0\,[(0.01 \times 3.6) + (0 \times 5.7)]\,1 = \underline{0.036}$$

LM741A die, 23 transistors, page 5.1.2.2-1 (same model as LM106 above):

$$1.0\ [(0.01 \times 2.9) + (0 \times 5.7)]\ 1 = 0.029$$

Si NPN transistor die, 60% stress ratio, Section 5.1.3, where $T + \Delta T(S) = 92.1°C$:

$$\lambda_b\ (\pi_E \pi_A \pi_Q \pi_R \pi_{S2} \pi_C)$$

$$(.0019)(21)(1.5)(0.12)(1.0)(0.88)(1.0) = \underline{0.0063}$$

Si PNP transistor die, 60% stress ratio, Section 5.1.3: (same model as NPN transistor above):

$$(.0018)(21)(1.5)(0.12)(1.0)(0.88)(1.0) = \underline{0.0060}$$

Si general purpose diode die, 60% stress ratio, Section 5.1.3 where $T + \Delta T(S) = 84.3°C$:

$$\lambda_b\ (\pi_E \pi_Q \pi_R \pi_A \pi_{S2} \pi_C)$$

$$(.0005)(21)(.15)(1.0)(1.0)(0.7)(1.0) = \underline{0.0011}$$

Ceramic chip capacitor, 60% stress ratio, 1000 pf., Section 5.1.3, where T=65°C case temperature:

$$\lambda_b\ (\pi_E \pi_Q \pi_{CV})$$

$$(.0063)(12.4)(1.0)(1.0) = \underline{0.075}$$

$\pi_E = 5.7$, Table 5.1.2.7-3
$\pi_Q = 1.0$, Table 5.1.2.7-1
$\pi_L = 1.0$, Table 5.1.2.7-2
$\pi_F = 5.8$, Table 5.1.2.9-1

$$\lambda_p = \{[.36 + .029 + 2\ (.0063) + 2(.0060) + 2\ (.0011) + 2\ (.075)]$$
$$[1 + (.2)(5.7)\}\ (1.0)(1.0)(5.8)$$
$$= 3.00 \text{ failures}/10^6 \text{ hours}$$

5.1.2.10 Magnetic Bubble Memories*. The magnetic bubble memory device in its present form is a non-hermetic assembly of two major structural segments:

a. A basic bubble chip or die consisting of a memory or a storage area (e.g., an array of minor loops), and required control and detection elements (e.g., generators, various gates and detectors), and,

b. A magnetic structure to provide controlled magnetic fields consisting of permanent magnets, coils, and a housing.

These two structural segments of the device are interconnected by a mechanical substrate and lead frame. The interconnect substrate in the present technology is normally a printed circuit board. It should be noted that this model does not include external support microelectronic devices required for magnetic bubble memory operation. The general form of the operating failure rate model is:

$$\lambda_p = \lambda_1 + \lambda_2$$

where:

λ_p = operating failure rate in failures/10^6 hrs.

λ_1 = failure rate of the control and detection structure.

λ_2 = failure rate of the memory storage area.

*See Bibliography Item No. 60

5.1.2.10.1 Failure Rate of the Control and Detection Structure (λ_1).

The expansion of λ_1 is:

$$\lambda_1 = \pi_Q \left[N_C C_{11} \pi_{T1} \pi_W + (N_C C_{21} + C_2) \pi_E \right] \pi_D \pi_L$$

where:

π_Q = quality factor, Table 5.1.2.7-1

N_C = number of bubble chips per packaged device

C_{11} & C_{21} = device complexity failure rates for the control and detection elements, Table 5.1.2.10-1

C_2 = package complexity failure rate, Table 5.1.2.7-16

π_{T1} = temperature acceleration factor. Use the values in Table 5.1.2.7-12. Use $T_J = T_{CASE} + 10$ (all in ^oC.)

π_W = write duty cycle factor, Table 5.1.2.10-4

π_E = application environment factor Table 5.1.2.7-3

π_D = duty cycle factor, Table 5.1.2.10-3

π_L = device learning factor, Table 5.1.2.7-2. Because this is a relatively new technology, justification should be given for use of $\pi_L = 1$.

5.1.2.10.2 Failure Rate of the Memory Storage Area (λ_2).

The expansion of λ_2 is:

$$\lambda_2 = \pi_Q N_C (C_{12} \pi_{T2} + C_{22} \pi_E) \pi_L$$

where:

π_Q = quality factor, Table 5.1.2.7-1

N_C = number of bubble chips per packaged device

C_{12} & C_{22} = device complexity failure rates Table 5.1.2.10-2.

π_{T2} = temperature acceleration factor. Use the values in Table 5.1.2.7-8. Use $T_J = T_{CASE} + 10$ (all in ^oC.)

π_E = application environment factor, Table 5.1.2.7-3

π_L = device learning factor, Table 5.1.2.7-2. Because this is a relatively new technology, justification should be given for use of π_L = 1.

TABLE 5.1.2.10-1: C_{11} & C_{21}, DEVICE COMPLEXITY FAILURE RATES FOR CONTROL & DETECTION STRUCTURE IN MAGNETIC BUBBLE DEVICES IN FAILURES PER 10^6 HOURS.

N_1	C_{11}	C_{21}	N_1	C_{11}	C_{21}
4	.0017	.00014	500	.011	.00041
50	.0045	.00024	550	.012	.00042
100	.0060	.00028	600	.012	.00042
150	.0070	.00031	650	.013	.00043
200	.0079	.00033	700	.013	.00044
250	.0086	.00035	750	.013	.00045
300	.0093	.00036	800	.014	.00046
350	.0099	.00038	850	.014	.00046
400	.010	.00039	900	.014	.00047
450	.011	.00040	950	.015	.00047
			1000	.015	.00048

Tabulated values are determined from the following equations:

$$C_{11} = .00095(N_1)^{.40} \text{ \& } C_{21} = .0001\,(N_1)^{.226}$$

where:

N_1 = the number of dissipative elements on a chip (gates, detectors, generators, etc.) and is $\leq$ 1000.

TABLE 5.1.2.10-2: C_{12} & C_{22} DEVICE COMPLEXITY FAILURE RATES FOR MEMORY STORAGE STRUCTURE FOR MAGNETIC BUBBLE DEVICES IN FAILURES PER 10^6 HOURS.

NO. BITS IN (10^3)	C_{12}	C_{22}	NO. BITS IN $(10)^3$	C_{12}	C_{22}
66	.0020	.00028	1049	.0045	.00064
92	.0022	.00031	2097	.0055	.00079
131	.0024	.00035	4194	.0068	.00097
262	.0030	.00042	8389	.0084	.0012
524	.0036	.00052			

Tabulated values are determined from the following equations:

$$C_{12} = .00007\ (N_2)^{.3} \text{ \& } C_{22} = .00001\ (N_2)^{.3}$$

where:

N_2 = the number of bits and is $\leq 9\ (10)^6$.

TABLE 5.1.2.10-3: π_D, DUTY CYCLE FACTOR, FOR MAGNETIC BUBBLE DEVICES

D*	0	.1	.2	.3	.4	.5	.6	.7	.8	.9	1.0
π_D	.10	.19	.28	.37	.46	.55	.64	.73	.82	.91	1.0

* - The tabulated values are determined from

$$\pi_D = .90 + 0.1 \text{ for } 0 \leq D \leq 1.0$$

D is the device duty cycle and is application dependent. It is a function of the usage the bubble device experiences during the time the power is applied to the equipment using the device.

$$D = \frac{\text{Average device data rate for the application}}{\text{manufacturer's maximum rated data-rate}} \leq 1.$$

where: the application data rate is averaged over the time that the power is applied to the using equipment.

TABLE 5.1.2.10-4. π_W, WRITE-DUTY CYCLE FACTOR FOR MAGNETIC BUBBLE DEVICES.

D	R/W				
	1	10	100	1000	>2154
1.0	10	5.0	2.5	1.3	1
.9	9.1	4.6	2.4	1.2	1
.8	8.2	4.2	2.2	1.2	1
.7	7.3	3.8	2.1	1.2	1
.6	6.4	3.4	1.9	1.2	1
.5	5.5	3.0	1.8	1.1	1
.4	4.6	2.6	1.6	1.1	1
.3	3.7	2.2	1.5	1.1	1
.2	2.8	1.8	1.3	1	1
.1	1.9	1.4	1.2	1	1
.05	1.5	1.2	1.1	1	1
<.03	1	1	1	1	1

Tabulated values are determined from the following equations:

$$\pi_W = \left(D \frac{10}{(R/W)^{.3}} - 1 \right) + 1 \quad \text{for } 1 \leq R/W < 2154$$

$$= 1 \text{ for } R/W < 1 \text{ and } R/W \geq 2154$$

where:

R/W = no. of reads per write

D = device duty cycle (see footnote in Table 5.1.2.10-3)
For seed-bubble generator use table value divided by 4, or use 1, whichever is greater.

5.1.2.10.3 Example Failure Rate Calculations.

Example One: Find the operating failure rate for a single chip 92K bit magnetic bubble memory, 40°C case temperature, ground benign environment. The device has a 14 pin nonhermetic DIP enclosure with 10 pins connected, one major loop, three dissipative control elements (generate, replicate and detector bridge), and 144 transfer gates. Device has been in continuous production for two years and is used at D = 1.0 and R/W = 10.

For control and detection structure, Section 5.1.2.10.1,

$$\lambda_q = \pi_Q [N_C C_{11} \pi_{T1} \pi_W + (N_C C_{21} + C_2) \pi_E] \pi_D \pi_L$$

Table 5.1.2.7-1 Quality level D-1, $\pi_Q = 6.5$

Section 5.1.2.10.1 $N_C = 1$

N_1 = 1 major loop + 3 dissipative elements + 144 gates
= 148,

Table 5.1.2.10-1 $C_{11} = .007$, $C_{21} = .00031$

Table 5.1.2.10-5 $T_J = 40 + 10 = 50°C$, $\pi_{T1} = 1.1$

Table 5.1.2.10-4 D = 1, R/W = 10; $\pi_W = 5$

Table 5.1.2.7-15 Nonhermetic, 10 pins, $C_2 = .0034$

Table 5.1.2.7-3 For G_B, $\pi_E = .5$

Table 5.1.2.10-3 D = 1, $\pi_D = 1$

Table 5.1.2.7-2 $\pi_L = 1.05$

$$\lambda_1 = 6.5 \{[(1)(.007)(1.1)(5)] + [(1)(.00031) + .0034](.5)\}(1)(1.05)$$
$$= 6.5 (.0385 + .0019) 1.05$$
$$= 0.28 \text{ failures}/10^6 \text{ hours.}$$

For magnetic storage area, Section 5.1.2.10.2,

$$\lambda_2 = \pi_Q N_C (C_{12}\pi_{T2} + C_{22}\pi_E)\pi_L$$

Table 5.1.2.7-1 Quality level D-1, $\pi_Q = 6.5$

Section 5.1.2.10.1 $N_C = 1$

No. of bits = 92,000,

Table 5.1.2.10-2 $C_{12} = .0022$, $C_{22} = .00031$

Table 5.1.2.10-6 $T_J = 40 + 10 = 50°C$, $\pi_{T2} = .53$

Table 5.1.2.7-3 For G_B, $\pi_E = .5$

Table 5.1.2.7-2 $\pi_L = 1.05$

$$\pi_2 = (6.5)(1)[(.0022)(.53) + (.00031)(.5)](1.05)$$
$$= 6.5\ [.001166 + .000155]1.05$$
$$= .009 \text{ failures}/10^6 \text{ hours.}$$

From Section 5.1.2.10,

$$\lambda_p = \lambda_1 + \lambda_2$$
$$= .28 + .009$$
$$= .29 \text{ failures}/10^6 \text{ hours.}$$

Example Two: Find the operating failure rate for a single chip one megabit magnetic bubble memory at 40°C case temperature in a benign ground environment. The device has two generators, eight detector elements, 512 replicate/swap gates, four boot loop gates and is contained in a nonhermetic DIP with 19 pins connected. The application requires 10 reads per write and a data rate equal to the maximum rated value of 100kHz. The device uses a seed generator and is in early production.

For control and detection structure, Section 5.1.2.10.1,

$\lambda_1 = \pi_Q [N_C C_{11} \pi_{T1} \pi_W + (N_C C_{21} + C_2) \pi_E] \pi_D \pi_L$

Table 5.1.2.7-1 Quality level D-1, $\pi_Q = 6.5$

Section 5.1.2.10.1 $N_C = 1$

N_1 = 2 generators + 8 detector elements + 512 replicate /swap gates + 4 boot loop gates = 526

Table 5.1.2.10-1 $C_{11} = .012$ $C_{21} = .00041$.

Table 5.1.2.10-5 $T_J = 40 + 10 = 50°C$, $\pi_{T1} = 1.1$

Table 5.1.2.10-4 D = 100kHz./100kHz. = 1, R/W = 10

$\pi_W = 5/4 = 1.25$ for seed bubble generator

Table 5.1.2.7-15 Nonhermetic, 19 pins, $C_2 = .0075$

Table 5.1.2.7-3 For G_B, $\pi_E = .5$

Table 5.1.2.10-3 D = 1, $\pi_D = 1$

Table 5.1.2.7-2 Early production, $\pi_L = 2.1$

$\lambda_1 = 6.5 \{[(1)(.012)(1.1)(1.25)] + [(1)(.00041) + .0075](.5)\}(1)(2.1)$

$= 6.5 (.0165 + .004) 2.1$

$= 0.28$ failures/10^6 hours.

For magnetic storage area, section 5.1.2.10.2,

$\lambda_2 = \pi_Q N_C (C_{12}\pi_{T2} + C_{22}\pi_E)\pi_L$

Table 5.1.2.7-1 Quality level D-1, $\pi_Q = 6.5$

Section 5.1.2.10.1 $N_C = 1$

Table 5.1.2.10-2 $C_{12} = .0045$, $C_{22} = .00064$

Table 5.1.2.10-6 $T_J = 40 + 10 = 50°C$, $\pi_{T2} = .53$

Table 5.1.2.7-3 For G_B, $\pi_E = .5$

Table 5.1.2.7-2 Early production, $\pi_L = 2.1$

$\lambda_2 = (6.5)(1)[(.0045)(.53) + (.00064)(.5)](2.1)$

$= 6.5\ (.002385 + .00032)2.1$

$= .037$ failures/10^6 hours.

From Section 5.1.2.10,

$\lambda_p = \lambda_1 + \lambda_2$

$= 0.28 + .037$

$= 0.32$ failures /10^6 hours.

5.1.2.11 Surface Acoustic Wave (SAW) Devices. The part operating failure rate model (λ_p) is:

$$\lambda_p = 2.1\pi_Q\pi_E \text{ failures}/10^6 \text{ hours.}$$

where:

π_E = environmental factor (Table 5.1.2.11-1)

π_Q = 0.1 for high quality part, subjected to 10 temperature cycles, (-55°C to 125°C) with end point electrical test

π_Q = 1.0 commercial part

TABLE 5.1.2.11-1 Environmental Mode Factor

Environment	π_E
A_U	15.0
A_I	11.7
N_U	16.0
N_I	8.8
N_{UU}	17.0
N_{UL}	31.0
M_F	18.0
S_F	1.6
G_B	1.2
G_M	10.5
G_F	3.9
C_L	600.0

APPENDIX B

MATHEMATICAL DERIVATIONS

B.1 Probability of Success for Ln-Normal Failure Distributions

The failure density functions for many failure mechanisms are modeled by ln-normal distributions. This density function is described mathematically by

$$f(t) = \frac{1}{\sigma t\sqrt{2\pi}} \exp\left[(-1/2)\left(\frac{\ln t - \mu}{\sigma}\right)^2\right], \tag{B.1.1}$$

where:

$$\mu = \ln\left(t_{50\%}\right) \tag{B.1.2}$$

$$\sigma = \ln\left(t_{50\%}\right) - \ln\left(t_{16\%}\right) = \ln\left(t_{50\%}/t_{16\%}\right). \tag{B.1.3}$$

The probability of failure at time t, F(t), is

$$F(t) = \int_0^t f(x)\,dx. \tag{B.1.4}$$

The probability of success at time t, P(t), is

$$P(t) = 1 - F(t) = 1 - \int_0^t f(x)\,dx. \tag{B.1.5}$$

The probability of success at time t for the ln-normal probability density function is the same as the probability of success at ln(t) for the normal density function. By making the substitution

$$y = \ln x;\ dy = (1/x)\,dx \tag{B.1.6}$$

equation B.1.5 can be rewritten

$$P(t) = 1 - \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{\ln t} \exp\left[(-1/2)\left(\frac{y - \mu}{\sigma}\right)^2\right] dy, \qquad (B.1.7)$$

which is the probability of success for the normal density function, $N(\mu,\sigma)$, with random variable ln(t). The integral in equation B.1.7 can be approximated by use of tables provided by a comprehensive statistics text, or by the computer software program in appendix C.

The mechanism models that are described by ln-normal density functions are often described in terms of log(t) instead of ln(t). It is again possible to use the probability of success for the normal distribution to evaluate the probability of success for the ln-normal distribution in terms of log(t). Using the relationships between ln(t) and log(t),

$$\ln(t) = \ln(10) * \log(t) \qquad (B.1.8)$$

$$\mu = \ln(t_{50\%}) \qquad (B.1.2)$$
$$= \ln(10) * \log(t_{50\%})$$
$$= \ln(10) * m \qquad (B.1.9)$$

$$\alpha = \ln(t_{50\%}/t_{16\%}) \qquad (B.1.3)$$
$$= \ln(10) * \log(t_{50\%}/t_{16\%})$$
$$= \ln(10) * s, \qquad (B.1.10)$$

and the substitution

$$z = \log(x);\ dz = (1/\ln(10)) * (1/x)\ dx, \qquad (B.1.11)$$

an expression similar to B.1.7 can be derived,

$$P(t) = 1 - \frac{1}{\sigma\sqrt{2\pi}} \int_{-\infty}^{\log t} \exp\left[(-1/2)\left(\frac{z - m}{\sigma}\right)^2\right] dz. \qquad (B.1.12)$$

which is probability of success for the normal density function, N(m,s), with random variable log(t). Again, the integral in equation B.1.12 can be approximated by use of tables provided by a comprehensive statistics text, or by the computer software program in appendix C. Note that μ, σ, and upper evaluation limit of the integral, ln(t), of equation B.1.7 have been changed to m, s, and log(t), respectively in equation B.1.12.

B.2 Hazard (Failure) Rate Determination for Ln-Normal Failure Distributions

The hazard rate at time t for any failure distribution is given by

$$h(t) = f(t) / (1 - F(t)) = f(t) / P(t). \qquad (B.2.1)$$

For the ln-normal distribution, the functions f(t) and P(t) are given by equations B.1.1 and B.1.5, respectively. These equations must be evaluated in terms of ln(t), not log(t).

In order to evaluate these equations in terms of log(t), the relationships of B.1.8 to B.1.10 must be used to develop f(t) in terms of log(t),

$$f(t) = \frac{1}{\ln(10)} \frac{1}{st\sqrt{2\pi}} \exp\left[(-1/2)\left(\frac{\log t - m}{s}\right)^2\right]. \qquad (B.2.2)$$

Equations B.2.2 and B.1.12 can be used to determine hazard rate for the ln-normal distribution evaluated using log(t).

B.3 Derivation of Worst Case (Maximum) Current Density

According to Mil-M-38510, the maximum current density allowed, by design, is 0.5 MA/cm^2. Assuming a microcircuit was designed to this limit, and also realizing the worst case step coverage would be 50% of the flat coverage, the maximum current density not at a step would be 0.25 MA/cm^2. Since electromigration does not occur at a step, or any other location on a microcircuit where there is a change in metal direction, because of electron flux divergence in these areas, the worst case current density is 0.25 MA/cm^2. Since most integrated circuits operate with complementary logic, on average only half the metallization is affected by a current pulse in any one instance of time. The effective duty cycle is <= 50%. Assuming a worst case duty cycle of 50%, it has been shown[26] that the effective current density is decreased by 0.5. Therefore, the maximum effective current density for a microcircuit designed to the 0.5 MA/cm^2 limit is actually 0.125 MA/cm^2.

APPENDIX C

FORTRAN PROGRAMS FOR TDDB AND ELECTROMIGRATION CALCULATIONS

```
      PROGRAM TDDB_TABLE
C
C*********************************************************************
C
C       Generates a one page table of probability of success
C       values, another of hazard rate values and one of effective
C       hazard rate values for a user supplied amount of total gate
C       area.  Each page has a temperature and electric field axis.
C
C*********************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
      DIMENSION TS(36),ES(16),PS(16),HR(16),EHR(16)
C
      OPEN (10,FILE=' ',STATUS='NEW')
      OPEN (20,FILE=' ',STATUS='NEW')
      OPEN (30,FILE=' ',STATUS='NEW')
C
C       NOTE: LIMITS ON DO STATEMENTS ARE ARRAY DIMENSIONS
C
      DO 400 J = 0,35
         TS(J+1) = 0.D0 + 5.D0 * DBLE(J)
400   CONTINUE
      DO 300 K = 0,15
         ES(K+1) = 2.D0 + 0.2D0 * DBLE(K)
300   CONTINUE
      WRITE (*,*) 'ENTER TIME, HOURS'
      READ (*,*) TIME
      WRITE (*,*) 'ENTER AREA, LOG SQ. MICRONS'
      READ (*,*) A
      AS = 10.D0**A
C
      WRITE (10,200) ES
      WRITE (20,200) ES
      WRITE (30,200) ES
C
      DO 2 J=1,36
         DO 1 K=1,16
            CALL TDDB(AS,TS(J),ES(K),TIME,U,S,PS(K),HR(K),EHR(K))
            HR(K) = HR(K) * 1.D6
            EHR(K) = EHR(K) * 1.D6
            IF (HR(K).GE.999.D0) HR(K) = 999.D0
      IF (EHR(K).GE.999.D0) EHR(K) = 999.D0
1        CONTINUE
C
         WRITE (*,20) TS(J),PS
         WRITE (10,1000) TS(J),PS
         WRITE (20,2000) TS(J),HR
         WRITE (30,2000) TS(J),EHR
C
         I = (J / 10) * 10
         IF (J.EQ.I) THEN
            WRITE (10,100)
            WRITE (20,100)
            WRITE (30,100)
         ENDIF
C
2     CONTINUE
C
      write(10,500)time,a
      write(20,600)time,a
      write(30,700)time,a
c
      STOP
20    FORMAT (25X,F5.0,16F4.2)
200   FORMAT (//////25X,57('-'),'  Electric Field Stress (MV/cm)  ',43
     * ('-')/25X,'T(C)',F7.1,15(1X,F7.1)/25X,'------',16(1X,'--------')//)
100   FORMAT (25X,'------',16(1X,'--------'))
500   FORMAT (///65X,'TDDB:  PROBABILITY OF SUCCESS AT',F7.0,' HOURS ',
     *  'FOR AREA = ',F5.2,' LOG SQUARE MICRONS')
600   FORMAT (///65X,'TDDB:  HAZARD RATE (x 10E-6) AT',F7.0,
     *  ' HOURS FOR AREA = ',F5.2,' LOG SQUARE MICRONS')
700   FORMAT (///60X,'TDDB:  EFFECTIVE HAZARD RATE (x 10E-6) AT',F7.0,
     *  ' HOURS FOR AREA = ',F5.2,' LOG SQUARE MICRONS')
1000  FORMAT (25x,F5.0,15F8.5)
2000  FORMAT (25x,F5.0,16F8.3)
      END
```

```
      PROGRAM EM_TABLE
C
C*********************************************************************
C
C     Generates a one page table of probability of success
C     values, another of hazard rate values and one of effective
C     hazard rate values.  Each page has a temperature and
C     current density axis.
C
C*********************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
      DIMENSION TS(36),CDS(16),PS(16),HR(16),EHR(16)
C
      OPEN (10,FILE=' ',STATUS='NEW')
      OPEN (20,FILE=' ',STATUS='NEW')
      OPEN (30,FILE=' ',STATUS='NEW')
C
      DATA CDS/.04D0,.05D0,.06D0,.08D0,.1D0,.13D0,.17D0,.2D0,
     *  .25D0,.3D0,.4D0,.5D0,.6D0,.8D0,1.D0,1.3D0/
C
C     NOTE: LIMITS ON DO STATEMENTS ARE ARRAY DIMENSIONS
C
      DO 400 J = 0,35
         TS(J+1) = 0.D0 + 5.D0 * DBLE(J)
400   CONTINUE
      WRITE (*,*) 'ENTER TIME, HOURS'
      READ (*,*) TIME
C
      WRITE (10,200) CDS
      WRITE (20,200) CDS
      WRITE (30,200) CDS
C
      DO 2 J=1,36
         DO 1 K=1,16
            CALL EM(TS(J),CDS(K),TIME,U,S,PS(K),HR(K),EHR(K))
            HR(K) = HR(K) * 1.D6
            EHR(K) = EHR(K) * 1.D6
            IF (HR(K).GE.999.D0) HR(K) = 999.D0
            IF (EHR(K).GE.999.D0) EHR(K) = 999.D0
1        CONTINUE
C
         WRITE (*,20) TS(J),PS
         WRITE (10,1000) TS(J),PS
         WRITE (20,2000) TS(J),HR
         WRITE (30,2000) TS(J),EHR
C
         I = (J / 10) * 10
         IF (J.EQ.I) THEN
            WRITE (10,100)
            WRITE (20,100)
            WRITE (30,100)
         ENDIF
C
2     CONTINUE
C
      write (10,500)time
      write (20,600)time
      write (30,700)time
c
      STOP
20    FORMAT (25X,F5.0,16F4.2)
200   FORMAT (//////25X,57('-'),'  Current Density (MA/cm2)  ',48('-')/
     *  25X,'T(C)',F7.2,15(1X,F7.2)/25X,'------',16(1X,'--------')///)
100   FORMAT(25X,'------',16(1X,'--------'))
500   FORMAT (///70X,'ELECTRONIGRATION:  PROBABILITY OF SUCCESS AT',
     *  F7.0,' HOURS')
600   FORMAT (///70X,'ELECTRONIGRATION:  HAZARD RATE (x 10E-6) AT',F7.0,
     *  ' HOURS')
700   FORMAT (///65X,'ELECTRONIGRATION:  EFFECTIVE HAZARD RATE ',
     *  '(x 10E-6) AT',F7.0,' HOURS')
1000  FORMAT (25x,F5.0,16F8.5)
2000  FORMAT (25x,F5.0,16F8.3)
      END
```

```
      SUBROUTINE AA(AO,AS,UO,ACC)
C
C*****************************************************************************
C
C     SUBROUTINE AA
C
C     PURPOSE:
C
C        Calculate the acceleration factor due to dielectric area
C        relative to a reference area.
C
C     USAGE:
C
C        CALL AA (AO,AS,UO,ACC)
C
C     DESCRIPTION OF PARAMETERS:
C
C        AO  - reference area (square microns)
C        AS  - operating area (square microns)
C        UO  - log of median time of reference distribution (hours)
C        ACC - acceleration factor
C
C     SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C        ZVAL - calculates number of sigmas from the mean
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
      F = AO / (AO + AS)
      CALL ZVAL(F,Z)
      ACC = 1.D0 + (Z / UO)
      RETURN
      END
```

```
      SUBROUTINE AEF(EO,ES,B,ACC)
C
C*****************************************************************************
C
C       SUBROUTINE AEF
C
C       PURPOSE:
C
C          Calculate the acceleration factor due to electric field
C          stress relative to a reference electric field.
C
C       USAGE:
C
C          CALL AEF (EO,ES,B,ACC)
C
C       DESCRIPTION OF PARAMETERS:
C
C          EO  - reference electric field
C          ES  - applied electric field
C          B   - mechanism constant
C          ACC - acceleration factor
C
C SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C          NONE
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
      ACC = DEXP(B*(ES - EO))
      RETURN
      END
```

```
      SUBROUTINE AJ(CDO,CDS,N,ACC)
C
C*****************************************************************************
C
C       SUBROUTINE AJ
C
C       PURPOSE:
C
C          Calculate the acceleration factor due to current density
C          stress relative to a reference current density.
C
C       USAGE:
C
C          CALL AJ (CDO,CDS,N,ACC)
C
C       DESCRIPTION OF PARAMETERS:
C
C          CDO  - reference current density
C          CDS  - applied current density
C          N    - experimentally determined constant
C          ACC - acceleration factor
C
C SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C          NONE
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
      ACC = (CDS / CDO) ** N
      RETURN
      END
```

```
      SUBROUTINE AT(TO,TS,Ea,ACC)
C
C*****************************************************************************
C
C       SUBROUTINE AT
C
C       PURPOSE:
C
C          Calculate the acceleration factor due to temperature stress
C          relative to a reference temperature
C
C       USAGE:
C
C          CALL AT (TO,TS,Ea,ACC)
C
C       DESCRIPTION OF PARAMETERS:
C
C          TO  - reference temperature
C          TS  - operating temperature
C          Ea  - activation energy (eV/deg K)
C          ACC - acceleration factor
C
C       SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C          NONE
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
      B = 8.617D-5
      ACC = DEXP((Ea/B)*(1.D0/(TO+273.D0) - 1.D0/(TS+273.D0)))
      RETURN
      END
```

```
      SUBROUTINE CNDA(Z,F,IFLAG)
C
C*****************************************************************************
C
C       SUBROUTINE CNDA
C
C       PURPOSE:
C
C          Calculates the value of the cumulative normal distribution at
C          a given number of sigmas away from the mean.  This subroutine
C          uses a series expansion of the normal distribution to perform
C          the integration.
C
C       USAGE:
C
C          CALL CNDA (Z,F,IFLAG)
C
C       DESCRIPTION OF PARAMETERS:
C
C          Z     - number of sigmas from the mean = (x - u) / s
C          F     - area under the normal distribution at Z
C          IFLAG - error flag =  0  OK
C                             = -1  Z is less than -5.5
C                             =  1  Z is greater than 5.5
C
C       SUBROUTINES AND SUBPROGRAMS REQUIRED:
C
C          NONE
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
      N = 0
      F = 0.D0
C
      IFLAG = 0
      IF (Z.GT.5.5D0) IFLAG = 1
      IF (Z.LT.-5.5D0) IFLAG = -1
      IF (IFLAG.NE.0) RETURN
C
1     FACT = 1.D0
      DO 3 N=0,135
           RN = N
           IF (N.EQ.0) GO TO 2
           FACT = FACT * RN
2          SUMN = (-1.D0)**N * Z**(2*N+1)
           SUMD = (2.D0*RN+1.D0) * 2.D0**N * FACT
           SUM = SUMN / SUMD
          F = F + SUM
3     CONTINUE
      F = F / DSQRT(2.D0 * 3.141592653589793) + 0.5D0
      RETURN
      END
```

```
      SUBROUTINE EM(TS,CDS,TIME,U,S,PS,HR,EHR)
C
C*****************************************************************************
C
C       SUBROUTINE EM
C
C       PURPOSE:
C
C          Calculate u, s, probability of success, hazard rate and
C          effective hazard rate at any time t, given operating
C          temperature, and current density.
C
C       USAGE:
C
C          CALL EM (TS,CDS,TIME,U,S,PS,FR,EFR)
C
C       DESCRIPTION OF PARAMETERS:
C
C          TS   - operating temperature (degrees C)
C          CDS   - current density stress (MA/cm2)
C          TIME - time at which probaility of success, hazard rate and
C                 effective hazard rate is to be calculated
C          U    - log of failure distribution median
C          S    - square root of the variance of the failure
C                 distribution (log hours)
C          PS   - probability of success calculated at time TIME
C          FR   - hazard rate calculated at time TIME
C          EHR  - effective hazard rate calculated at time TIME by the
C                 equation:  EHR = -ln(TIME)/PS
C
C       SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C          AT   - temperature acceleration calculation
C          AJ   - current density acceleration calculation
C          CNDA - cumulative normal distribution approximation
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
C
      UO = 1.39800
      SO = 0.00800
      TO = 175.00
      Ea = 0.500
      CDO = 1.00
      N = 2
C
      STIME = DLOG10(TIME)
C
      CALL AT(TO,TS,Ea,ACCAT)
      CALL AJ(CDO,CDS,N,ACCAJ)
C
      U = UO - DLOG10(ACCAT*ACCAJ)
      S = SO
C
      Z = (STIME - U) / S
      CALL CNDA(Z,F,IFLAG)
C
      IF (IFLAG) 2,2,1
C
1     CONTINUE
      PS = 0.00
      HR = 999.00
      EHR = 999.00
      RETURN
C
2     CONTINUE
      PS = 1.00 - F
      IF (IFLAG.EQ.-1) PS = 1.000
      COEF = 1.00 / (DSQRT(2.00*3.14159265358979)*TIME*DLOG(10.00))
      Ht = COEF*DEXP(-.500*Z**2)
      HR = Ht / PS
      EHR = -1.00*DLOG(PS)/TIME
      RETURN
C
      END
```

```
      SUBROUTINE TDDB(AS,TS,ES,TIME,U,S,PS,HR,EHR)
C
C*****************************************************************************
C
C       SUBROUTINE TDDB
C
C       PURPOSE:
C
C          Calculate u, s, probability of success, hazard rate and
C          effective hazard rate at any time t, given total gate area,
C          operating temperature, and electric field stress.
C
C       USAGE:
C
C          CALL TDDB (AS,TS,ES,TIME,U,S,PS,FR ,EHR)
C
C       DESCRIPTION OF PARAMETERS:
C
C          AS   - total gate area (square microns)
C          TS   - operating temperature (degrees C)
C          ES   - electric field stress
C          TIME - time at which probability of success, hazard rate and
C                 effective hazard rate is to be calculated
C          U    - log of failure distribution median
C          S    - square root of the variance of the failure
C                 distribution (log hours)
C          PS   - probability of success calculated at time TIME
C          FR   - hazard rate calculated at time TIME
C          EHR  - effective hazard rate calculated at time TIME by the
C                 equation:  EHR = -ln(TIME)/PS
C
C       SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C          AA   - area acceleration calculation
C          AT   - temperature acceleration calculation
C          AEF  - electric field acceleration calculation
C          CNDA - cumulative normal distribution approximation
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
C
      UO = 8.4D0
      SO = 0.4D0
      AO = 1.7816D5
      TO = 22.0D0
      Ea = 0.30D0
      EO = 2.222D0
      BETA = 4.50D0
C
      STIME = DLOG10(TIME)
C
      CALL AA(AO,AS,UO,ACCAA)
      CALL AT(TO,TS,Ea,ACCAT)
      CALL AEF(EO,ES,BETA,ACCAEF)
C
      U = ACCAA * (UO - DLOG10(ACCAT*ACCAEF))
      S = SO
C
      Z = (STIME - U) / S
      CALL CNDA(Z,F,IFLAG)
C
      IF (IFLAG) 2,2,1
C
1     CONTINUE
      PS = 0.D0
      HR = 999.D0
      EHR = 999.D0
      RETURN
C
2     CONTINUE
```

```
      PS = 1.D0 - F
      IF (IFLAG.EQ.-1) PS = 1.000
      COEF = 1.D0 / (DSQRT(2.D0*3.141592653589793)*TIME*DLOG(10.D0))
      Ht = COEF*DEXP(-.5D0*Z**2)
      HR = Ht / PS
      EHR = -1.D0*DLOG(PS)/TIME
      RETURN
C
      END
```

```
      SUBROUTINE ZVAL(F,Z)
C
C*****************************************************************************
C
C       SUBROUTINE ZVAL
C
C       PURPOSE:
C
C          Calculates the number of sigmas away from the mean of a
C          normal distribution for a given probability of failure
C          (cumulative percent failure in decimal).  This subroutine
C          uses the Newton-Raphson method of finding roots.
C
C       USAGE:
C
C          CALL ZVAL(F,Z)
C
C       DESCRIPTION OF PARAMETERS:
C
C          F - probability of failure (cumulative percent failure in
C              decimal)
C          Z - number of sigmas from the mean of the normal distribution
C
C       SUBROUTINES AND FUNCTION SUBPROGRAMS REQUIRED:
C
C          CNDA - cumulative normal distribution approximation
C
C*****************************************************************************
C
      IMPLICIT REAL*8 (A-H,O-Z), INTEGER*4 (I-N)
C
      IF (F.LE.0.5D0) ZNEW = -0.5D0
      IF (F.GT.0.5D0) ZNEW = 0.5D0
      Z = ZNEW
C
      DO 5 N=1,100
         CALL CNDA(Z,FNEW,IFLAG)
         IF (IFLAG.EQ.-1) FNEW = 0.D0
         IF (IFLAG.EQ.1) FNEW = 1.D0
         PHI = FNEW - F
         PHIPRI = 1.D0/(DSQRT(2.D0*3.141592653589793)*DEXP(.5D0*Z**2))
         ZNEW = Z
         Z = Z - PHI / PHIPRI
         IF (DABS(Z-ZNEW)/DABS(Z).LT.0.0000001D0) RETURN
5     CONTINUE
      RETURN
      END
```

APPENDIX D

PROBABILITY OF SUCCES AND HAZARD RATE TABLES

T(C)	Electric Field Stress (MV/cm) 2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99983	.99216	.89461	.53442
5.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99949	.98298	.83009	.41663
10.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99864	.96661	.74796	.30961
15.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99675	.94022	.65233	.21964
20.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99985	.99295	.90141	.54957	.14906
25.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99961	.98598	.84886	.44690	.09705
30.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99907	.97423	.78289	.35084	.06080
35.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99795	.95596	.70558	.26614	.03676
40.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99582	.92947	.62050	.19537	.02152
45.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99983	.99203	.89351	.53204	.13904	.01223
50.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99960	.98578	.84757	.44473	.09611	.00677
55.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99917	.97606	.79199	.36254	.06467	.00366
60.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99834	.96181	.72809	.28842	.04244	.00194
65.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99690	.94201	.65796	.22417	.02722	.00101
70.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99990	.99450	.91582	.58413	.17040	.01710	.00051
75.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99978	.99071	.88273	.50945	.12686	.01054	.00026
80.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99957	.98501	.84262	.43654	.09262	.00639	.00013
85.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99920	.97682	.79588	.36766	.06641	.00381	.00006
90.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99858	.96552	.74331	.30452	.04682	.00224	.00003
95.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99756	.95052	.68613	.24821	.03251	.00131	.00001
100.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99599	.93133	.62580	.19925	.02225	.00075	.00001
105.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99987	.99363	.90757	.56392	.15766	.01504	.00043	.00000
110.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99977	.99024	.87906	.50210	.12307	.01004	.00024	.00000
115.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99959	.98551	.84582	.44182	.09486	.00663	.00014	.00000
120.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99932	.97912	.80810	.38432	.07226	.00434	.00008	.00000
125.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99888	.97075	.76634	.33062	.05444	.00282	.00004	.00000
130.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99823	.96006	.72118	.28140	.04060	.00181	.00002	.00000
135.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99728	.94677	.67339	.23707	.03000	.00116	.00001	.00000
140.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99592	.93065	.62384	.19781	.02198	.00074	.00001	.00000
145.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99988	.99405	.91151	.57340	.16354	.01597	.00047	.00000	.00000
150.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99981	.99152	.88927	.52296	.13405	.01153	.00029	.00000	.00000
155.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99970	.98819	.86394	.47334	.10899	.00827	.00018	.00000	.00000
160.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99953	.98389	.83561	.42526	.08795	.00589	.00011	.00000	.00000
165.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99928	.97845	.80449	.37932	.07047	.00418	.00007	.00000	.00000
170.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99894	.97172	.77085	.33600	.05609	.00295	.00004	.00000	.00000
175.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99845	.96352	.73503	.29565	.04438	.00207	.00003	.00000	.00000

TDDB: PROBABILITY OF SUCCESS AT 10000. HOURS FOR AREA = 4.00 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm)															
	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99738	.95498	.72501	.30869
5.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99985	.99401	.92154	.62480	.21792
10.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99958	.98755	.87404	.51928	.14708
15.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99897	.97630	.81200	.41602	.09519
20.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99766	.95828	.73688	.32147	.05927
25.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99988	.99514	.93163	.65198	.23988	.03561
30.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99972	.99062	.89489	.56183	.17316	.02072
35.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99936	.98312	.84745	.47137	.12117	.01171
40.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99865	.97146	.78970	.38515	.08236	.00645
45.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99734	.95444	.72312	.30670	.05451	.00347
50.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99988	.99506	.93094	.65007	.23827	.03521	.00183
55.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99975	.99134	.90017	.57345	.18083	.02224	.00095
60.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99949	.98558	.86175	.49634	.13425	.01377	.00048
65.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99901	.97709	.81584	.42162	.09764	.00837	.00024
70.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99820	.96515	.76317	.35167	.06968	.00500	.00012
75.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99994	.99687	.94909	.70496	.28821	.04886	.00295	.00006
80.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99987	.99478	.92831	.64280	.23227	.03372	.00172	.00003
85.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99976	.99164	.90240	.57848	.18423	.02293	.00099	.00001
90.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99956	.98711	.87119	.51383	.14396	.01538	.00056	.00001
95.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99923	.98080	.83476	.45057	.11093	.01020	.00032	.00000
100.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99871	.97231	.79347	.39018	.08438	.00669	.00018	.00000
105.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99790	.96125	.74793	.33383	.06341	.00434	.00010	.00000
110.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99670	.94725	.69895	.28231	.04713	.00280	.00005	.00000
115.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99988	.99496	.93002	.64749	.23613	.03467	.00179	.00003	.00000
120.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99979	.99254	.90934	.59459	.19545	.02527	.00113	.00002	.00000
125.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99966	.98923	.88513	.54128	.16019	.01826	.00072	.00001	.00000
130.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99945	.98485	.85740	.48857	.13008	.01309	.00045	.00000	.00000
135.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99914	.97917	.82629	.43733	.10472	.00932	.00028	.00000	.00000
140.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99869	.97200	.79208	.38832	.08363	.00660	.00017	.00000	.00000
145.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99805	.96312	.75512	.34213	.06629	.00464	.00011	.00000	.00000
150.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99994	.99716	.95234	.71589	.29920	.05218	.00325	.00007	.00000	.00000
155.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99991	.99595	.93952	.67488	.25981	.04082	.00227	.00004	.00000	.00000
160.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99986	.99436	.92454	.63266	.22409	.03174	.00157	.00003	.00000	.00000
165.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99978	.99228	.90731	.58978	.19205	.02455	.00109	.00002	.00000	.00000
170.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99967	.98962	.88781	.54681	.16360	.01890	.00075	.00001	.00000	.00000
175.	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99952	.98629	.86607	.50425	.13858	.01448	.00052	.00001	.00000	.00000

TDDB: PROBABILITY OF SUCCESS AT 10000. HOURS FOR AREA = 4.50 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm) 2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99812	.96989	.80515	.43690	.11943
5.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99987	.99584	.94733	.72591	.33778	.07528
10.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99967	.99153	.91450	.63681	.25173	.04570
15.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99923	.98407	.87016	.54306	.18118	.02681
20.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99831	.97210	.81423	.45009	.12622	.01525
25.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99990	.99659	.95419	.74789	.36273	.08532	.00844
30.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99977	.99357	.92903	.67349	.28453	.05609	.00456
35.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99951	.98859	.89569	.59421	.21751	.03596	.00241
40.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99900	.98087	.85382	.51354	.16229	.02253	.00125
45.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99809	.96953	.80371	.43483	.11839	.01383	.00064
50.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99990	.99654	.95372	.74635	.36093	.08457	.00833	.00032
55.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99980	.99405	.93268	.68332	.29391	.05926	.00494	.00016
60.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99960	.99022	.90584	.61660	.23501	.04080	.00289	.00008
65.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99926	.98459	.87295	.54833	.18471	.02765	.00166	.00004
70.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99869	.97668	.83409	.48064	.14286	.01846	.00095	.00002
75.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99994	.99777	.96595	.78969	.41540	.10885	.01217	.00054	.00001
80.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99989	.99635	.95194	.74050	.35416	.08179	.00793	.00030	.00000
85.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99980	.99425	.93422	.68756	.29803	.06068	.00511	.00017	.00000
90.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99966	.99123	.91250	.63204	.24770	.04449	.00327	.00009	.00000
95.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99942	.98705	.88662	.57524	.20347	.03228	.00207	.00005	.00000
100.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99904	.98143	.85660	.51840	.16531	.02319	.00130	.00003	.00000
105.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99848	.97408	.82261	.46270	.13293	.01652	.00081	.00002	.00000
110.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99994	.99765	.96472	.78501	.40913	.10587	.01167	.00051	.00001	.00000
115.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99990	.99648	.95309	.74428	.35852	.08357	.00819	.00031	.00000	.00000
120.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99983	.99485	.93899	.70102	.31148	.06543	.00571	.00019	.00000	.00000
125.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99973	.99264	.92225	.65591	.26839	.05085	.00396	.00012	.00000	.00000
130.	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99957	.98973	.90277	.60967	.22948	.03924	.00273	.00007	.00000	.00000
135.	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99935	.98598	.88052	.56300	.19478	.03009	.00188	.00004	.00000	.00000
140.	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99903	.98122	.85557	.51660	.16419	.02294	.00128	.00003	.00000	.00000
145.	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99858	.97532	.82804	.47108	.13751	.01740	.00088	.00002	.00000	.00000
150.	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99797	.96813	.79814	.42700	.11448	.01314	.00060	.00001	.00000	.00000
155.	1.00000	1.00000	1.00000	1.00000	1.00000	.99992	.99715	.95952	.76612	.38481	.09478	.00988	.00040	.00001	.00000	.00000
160.	1.00000	1.00000	1.00000	1.00000	1.00000	.99988	.99607	.94937	.73230	.34486	.07806	.00740	.00027	.00000	.00000	.00000
165.	1.00000	1.00000	1.00000	1.00000	1.00000	.99982	.99467	.93759	.69702	.30743	.06398	.00552	.00019	.00000	.00000	.00000
170.	1.00000	1.00000	1.00000	1.00000	1.00000	.99974	.99290	.92411	.66067	.27268	.05221	.00411	.00013	.00000	.00000	.00000
175.	1.00000	1.00000	1.00000	1.00000	.99999	.99963	.99069	.90890	.62361	.24070	.04244	.00305	.00008	.00000	.00000	.00000

TDDB: PROBABILITY OF SUCCESS AT 10000. HOURS FOR AREA = 5.00 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm)															
	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99990	.99726	.96727	.81767	.48840	.16736	.02870
5.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99974	.99445	.94560	.74796	.39454	.11447	.01623
10.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99941	.98953	.91522	.66933	.30941	.07592	.00893
15.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99875	.98156	.87526	.58552	.23591	.04895	.00479
20.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99991	.99751	.96945	.82567	.50064	.17516	.03077	.00251
25.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99980	.99535	.95209	.76728	.41853	.12689	.01891	.00130
30.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99958	.99182	.92855	.70178	.34235	.08986	.01139	.00066
35.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99916	.98634	.89817	.63142	.27427	.06233	.00673	.00033
40.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99843	.97826	.86071	.55880	.21545	.04242	.00392	.00016
45.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99990	.99722	.96691	.81639	.48648	.16616	.02839	.00225	.00008
50.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99979	.99529	.95165	.76593	.41681	.12597	.01871	.00128	.00004
55.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99961	.99236	.93193	.71045	.35165	.09401	.01216	.00072	.00002
60.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99930	.98810	.90735	.65138	.29235	.06915	.00781	.00040	.00001
65.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99880	.98211	.87776	.59028	.23969	.05020	.00496	.00022	.00000
70.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99800	.97401	.84321	.52877	.19396	.03601	.00312	.00012	.00000
75.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99988	.99681	.96341	.80405	.46835	.15505	.02555	.00195	.00007	.00000
80.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99978	.99506	.94996	.76079	.41032	.12256	.01796	.00121	.00004	.00000
85.	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99963	.99259	.93335	.71419	.35572	.09586	.01251	.00074	.00002	.00000
90.	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99939	.98921	.91340	.66510	.30532	.07427	.00865	.00046	.00001	.00000
95.	1.00000	1.00000	1.00000	1.00000	1.00000	.99997	.99902	.98470	.89000	.61446	.25959	.05703	.00594	.00028	.00001	.00000
100.	1.00000	1.00000	1.00000	1.00000	1.00000	.99995	.99849	.97884	.86318	.56321	.21874	.04345	.00405	.00017	.00000	.00000
105.	1.00000	1.00000	1.00000	1.00000	1.00000	.99992	.99773	.97141	.83307	.51228	.18279	.03286	.00275	.00010	.00000	.00000
110.	1.00000	1.00000	1.00000	1.00000	1.00000	.99987	.99666	.96221	.79993	.46247	.15156	.02469	.00186	.00006	.00000	.00000
115.	1.00000	1.00000	1.00000	1.00000	1.00000	.99979	.99521	.95106	.76411	.41450	.12475	.01844	.00125	.00004	.00000	.00000
120.	1.00000	1.00000	1.00000	1.00000	.99999	.99967	.99328	.93779	.72606	.36894	.10200	.01370	.00084	.00002	.00000	.00000
125.	1.00000	1.00000	1.00000	1.00000	.99999	.99950	.99077	.92231	.68625	.32623	.08289	.01013	.00056	.00001	.00000	.00000
130.	1.00000	1.00000	1.00000	1.00000	.99998	.99926	.98757	.90456	.64521	.28666	.06697	.00746	.00038	.00001	.00000	.00000
135.	1.00000	1.00000	1.00000	1.00000	.99997	.99893	.98356	.88453	.60348	.25041	.05383	.00547	.00025	.00001	.00000	.00000
140.	1.00000	1.00000	1.00000	1.00000	.99995	.99847	.97862	.86226	.56158	.21752	.04306	.00400	.00017	.00000	.00000	.00000
145.	1.00000	1.00000	1.00000	1.00000	.99993	.99786	.97265	.83787	.52000	.18796	.03430	.00292	.00011	.00000	.00000	.00000
150.	1.00000	1.00000	1.00000	1.00000	.99989	.99706	.96554	.81149	.47919	.16163	.02722	.00213	.00007	.00000	.00000	.00000
155.	1.00000	1.00000	1.00000	1.00000	.99983	.99603	.95719	.78331	.43954	.13836	.02152	.00154	.00005	.00000	.00000	.00000
160.	1.00000	1.00000	1.00000	1.00000	.99976	.99472	.94753	.75358	.40138	.11794	.01696	.00112	.00003	.00000	.00000	.00000
165.	1.00000	1.00000	1.00000	.99999	.99966	.99308	.93649	.72253	.36497	.10014	.01333	.00081	.00002	.00000	.00000	.00000
170.	1.00000	1.00000	1.00000	.99999	.99952	.99106	.92403	.69045	.33053	.08472	.01045	.00059	.00001	.00000	.00000	.00000
175.	1.00000	1.00000	1.00000	.99998	.99934	.98861	.91012	.65761	.29818	.07143	.00818	.00042	.00001	.00000	.00000	.00000

TDDB: PROBABILITY OF SUCCESS AT 10000. HOURS FOR AREA = 5.50 LOG SQUARE MICRONS

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99969	.99483	.95611	.80235	.49715	.19370	.04257	.00496
5.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99932	.99051	.93173	.73617	.41075	.13945	.02619	.00258
10.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99994	.99862	.98363	.89938	.66307	.33129	.09791	.01575	.00132
15.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99987	.99736	.97331	.85873	.58606	.26116	.06720	.00928	.00066
20.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99972	.99524	.95866	.81007	.50836	.20151	.04518	.00538	.00033
25.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99944	.99186	.93888	.75436	.43292	.15241	.02983	.00307	.00016
30.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99895	.98676	.91338	.69310	.36221	.11319	.01937	.00173	.00008
35.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99991	.99813	.97939	.88183	.62816	.29798	.08266	.01240	.00096	.00004
40.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99983	.99680	.96922	.84428	.56159	.24128	.05945	.00783	.00053	.00002
45.	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99968	.99477	.95570	.80112	.49539	.19249	.04218	.00489	.00029	.00001
50.	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99943	.99177	.93839	.75308	.43133	.15146	.02955	.00303	.00016	.00000
55.	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99903	.98752	.91696	.70116	.37090	.11768	.02048	.00186	.00009	.00000
60.	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99840	.98171	.89124	.64652	.31516	.09037	.01406	.00113	.00005	.00000
65.	1.00000	1.00000	1.00000	1.00000	1.00000	.99987	.99745	.97399	.86122	.59042	.26481	.06867	.00957	.00069	.00002	.00000
70.	1.00000	1.00000	1.00000	1.00000	.99999	.99978	.99606	.96407	.82711	.53412	.22018	.05168	.00646	.00041	.00001	.00000
75.	1.00000	1.00000	1.00000	1.00000	.99999	.99963	.99410	.95166	.78928	.47875	.18128	.03856	.00433	.00025	.00001	.00000
80.	1.00000	1.00000	1.00000	1.00000	.99998	.99940	.99142	.93651	.74824	.42534	.14791	.02854	.00289	.00015	.00000	.00000
85.	1.00000	1.00000	1.00000	1.00000	.99996	.99906	.98784	.91849	.70463	.37470	.11967	.02098	.00192	.00009	.00000	.00000
90.	1.00000	1.00000	1.00000	1.00000	.99994	.99857	.98319	.89749	.65916	.32743	.09608	.01533	.00127	.00005	.00000	.00000
95.	1.00000	1.00000	1.00000	1.00000	.99990	.99787	.97728	.87354	.61259	.28395	.07660	.01114	.00084	.00003	.00000	.00000
100.	1.00000	1.00000	1.00000	1.00000	.99984	.99690	.96992	.84672	.56564	.24449	.06068	.00806	.00055	.00002	.00000	.00000
105.	1.00000	1.00000	1.00000	.99999	.99975	.99559	.96097	.81724	.51902	.20911	.04779	.00580	.00036	.00001	.00000	.00000
110.	1.00000	1.00000	1.00000	.99999	.99961	.99387	.95028	.78534	.47336	.17773	.03744	.00416	.00024	.00001	.00000	.00000
115.	1.00000	1.00000	1.00000	.99998	.99942	.99165	.93773	.75137	.42920	.15019	.02919	.00298	.00015	.00000	.00000	.00000
120.	1.00000	1.00000	1.00000	.99997	.99916	.98883	.92325	.71568	.38700	.12624	.02267	.00213	.00010	.00000	.00000	.00000
125.	1.00000	1.00000	1.00000	.99995	.99880	.98531	.90679	.67870	.34711	.10559	.01754	.00151	.00007	.00000	.00000	.00000
130.	1.00000	1.00000	1.00000	.99992	.99832	.98101	.88837	.64084	.30977	.08792	.01352	.00108	.00004	.00000	.00000	.00000
135.	1.00000	1.00000	1.00000	.99989	.99768	.97582	.86802	.60252	.27514	.07290	.01040	.00076	.00003	.00000	.00000	.00000
140.	1.00000	1.00000	1.00000	.99983	.99686	.96966	.84582	.56414	.24330	.06022	.00797	.00054	.00002	.00000	.00000	.00000
145.	1.00000	1.00000	.99999	.99976	.99582	.96245	.82190	.52609	.21425	.04958	.00610	.00038	.00001	.00000	.00000	.00000
150.	1.00000	1.00000	.99999	.99966	.99451	.95411	.79641	.48870	.18793	.04069	.00466	.00027	.00001	.00000	.00000	.00000
155.	1.00000	1.00000	.99998	.99953	.99289	.94459	.76953	.45228	.16426	.03330	.00356	.00019	.00001	.00000	.00000	.00000
160.	1.00000	1.00000	.99998	.99936	.99092	.93384	.74145	.41708	.14308	.02719	.00271	.00014	.00000	.00000	.00000	.00000
165.	1.00000	1.00000	.99997	.99913	.98854	.92185	.71240	.38331	.12425	.02215	.00206	.00010	.00000	.00000	.00000	.00000
170.	1.00000	1.00000	.99995	.99884	.98571	.90860	.68259	.35114	.10759	.01801	.00157	.00007	.00000	.00000	.00000	.00000
175.	1.00000	1.00000	.99993	.99848	.98239	.89410	.65226	.32068	.09292	.01462	.00119	.00005	.00000	.00000	.00000	.00000

TDDB: PROBABILITY OF SUCCESS AT 10000. HOURS FOR AREA = 6.00 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm)															
	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99919	.99090	.94201	.78301	.49717	.21285	.05636	.00876	.00078
5.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99991	.99841	.98462	.91476	.71944	.41750	.15919	.03695	.00499	.00038
10.	1.00000	1.00000	1.00000	1.00000	1.00000	.99999	.99980	.99707	.97535	.88032	.65066	.34370	.11666	.02378	.00280	.00019
15.	1.00000	1.00000	1.00000	1.00000	1.00000	.99998	.99961	.99489	.96236	.83872	.57916	.27768	.08391	.01505	.00155	.00009
20.	1.00000	1.00000	1.00000	1.00000	1.00000	.99996	.99926	.99151	.94495	.79053	.50749	.22044	.05936	.00940	.00085	.00004
25.	1.00000	1.00000	1.00000	1.00000	1.00000	.99993	.99866	.98653	.92261	.73676	.43798	.17218	.04136	.00579	.00046	.00002
30.	1.00000	1.00000	1.00000	1.00000	.99999	.99985	.99769	.97949	.89503	.67877	.37251	.13249	.02844	.00353	.00025	.00001
35.	1.00000	1.00000	1.00000	1.00000	.99999	.99973	.99620	.96992	.86217	.61816	.31248	.10057	.01933	.00214	.00013	.00000
40.	1.00000	1.00000	1.00000	1.00000	.99998	.99952	.99398	.95739	.82426	.55656	.25874	.07540	.01300	.00128	.00007	.00000
45.	1.00000	1.00000	1.00000	1.00000	.99996	.99917	.99080	.94154	.78181	.49555	.21167	.05590	.00867	.00076	.00004	.00000
50.	1.00000	1.00000	1.00000	1.00000	.99992	.99864	.98640	.92207	.73554	.43651	.17123	.04104	.00573	.00045	.00002	.00000
55.	1.00000	1.00000	1.00000	1.00000	.99987	.99784	.98051	.89885	.68635	.38058	.13710	.02986	.00377	.00027	.00001	.00000
60.	1.00000	1.00000	1.00000	.99999	.99977	.99668	.97287	.87186	.63522	.32861	.10874	.02155	.00246	.00016	.00001	.00000
65.	1.00000	1.00000	1.00000	.99998	.99962	.99504	.96319	.84123	.58319	.28115	.08551	.01545	.00160	.00009	.00000	.00000
70.	1.00000	1.00000	1.00000	.99997	.99939	.99279	.95127	.80726	.53122	.23850	.06673	.01101	.00104	.00005	.00000	.00000
75.	1.00000	1.00000	1.00000	.99995	.99906	.98980	.93692	.77032	.48023	.20072	.05170	.00780	.00067	.00003	.00000	.00000
80.	1.00000	1.00000	1.00000	.99992	.99858	.98590	.92000	.73092	.43098	.16768	.03981	.00551	.00043	.00002	.00000	.00000
85.	1.00000	1.00000	1.00000	.99987	.99790	.98095	.90047	.68962	.38411	.13914	.03049	.00387	.00028	.00001	.00000	.00000
90.	1.00000	1.00000	.99999	.99980	.99698	.97478	.87834	.64701	.34009	.11474	.02323	.00271	.00018	.00001	.00000	.00000
95.	1.00000	1.00000	.99999	.99969	.99575	.96726	.85370	.60371	.29926	.09409	.01762	.00190	.00011	.00000	.00000	.00000
100.	1.00000	1.00000	.99998	.99953	.99413	.95825	.82670	.56029	.26181	.07675	.01332	.00132	.00007	.00000	.00000	.00000
105.	1.00000	1.00000	.99997	.99932	.99206	.94764	.79755	.51731	.22781	.06232	.01003	.00092	.00005	.00000	.00000	.00000
110.	1.00000	1.00000	.99995	.99902	.98946	.93535	.76652	.47526	.19723	.05040	.00754	.00064	.00003	.00000	.00000	.00000
115.	1.00000	1.00000	.99992	.99862	.98622	.92134	.73390	.43454	.16996	.04060	.00565	.00045	.00002	.00000	.00000	.00000
120.	1.00000	1.00000	.99988	.99809	.98229	.90558	.70004	.39552	.14584	.03260	.00423	.00031	.00001	.00000	.00000	.00000
125.	1.00000	.99999	.99983	.99741	.97756	.88808	.66527	.35846	.12465	.02610	.00316	.00022	.00001	.00000	.00000	.00000
130.	1.00000	.99999	.99976	.99653	.97198	.86889	.62994	.32355	.10615	.02084	.00235	.00015	.00001	.00000	.00000	.00000
135.	1.00000	.99999	.99966	.99544	.96545	.84810	.59438	.29093	.09010	.01660	.00176	.00010	.00000	.00000	.00000	.00000
140.	1.00000	.99998	.99953	.99408	.95793	.82580	.55891	.26067	.07625	.01320	.00131	.00007	.00000	.00000	.00000	.00000
145.	1.00000	.99997	.99935	.99241	.94936	.80213	.52382	.23278	.06435	.01048	.00097	.00005	.00000	.00000	.00000	.00000
150.	1.00000	.99996	.99913	.99041	.93971	.77723	.48939	.20722	.05418	.00831	.00072	.00004	.00000	.00000	.00000	.00000
155.	1.00000	.99994	.99884	.98801	.92895	.75128	.45583	.18394	.04552	.00658	.00054	.00002	.00000	.00000	.00000	.00000
160.	1.00000	.99991	.99848	.98519	.91707	.72446	.42334	.16285	.03817	.00521	.00040	.00002	.00000	.00000	.00000	.00000
165.	1.00000	.99988	.99804	.98190	.90407	.69694	.39210	.14381	.03195	.00412	.00030	.00001	.00000	.00000	.00000	.00000
170.	.99999	.99984	.99749	.97809	.88998	.66892	.36221	.12672	.02671	.00325	.00022	.00001	.00000	.00000	.00000	.00000
175.	.99999	.99978	.99682	.97375	.87482	.64057	.33378	.11143	.02230	.00257	.00017	.00001	.00000	.00000	.00000	.00000

TDDB: PROBABILITY OF SUCCESS AT 10000. HOURS FOR AREA = 6.50 LOG SQUARE MICRONS

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	1.00000	1.00000	1.00000	1.00000	.99999	.99987	.99827	.98580	.92784	.76669	.49844	.23092	.07109	.01392	.00169	.00012
5.	1.00000	1.00000	1.00000	1.00000	.99999	.99974	.99690	.97753	.89856	.70591	.42448	.17817	.04904	.00851	.00091	.00006
10.	1.00000	1.00000	1.00000	1.00000	.99997	.99950	.99473	.96603	.86290	.64115	.35555	.13517	.03331	.00514	.00049	.00003
15.	1.00000	1.00000	1.00000	1.00000	.99994	.99908	.99143	.95070	.82115	.57450	.29320	.10098	.02233	.00307	.00026	.00001
20.	1.00000	1.00000	1.00000	.99999	.99988	.99840	.98665	.93108	.77397	.50801	.23828	.07441	.01479	.00182	.00014	.00001
25.	1.00000	1.00000	1.00000	.99996	.99978	.99733	.98000	.90688	.72236	.44352	.19107	.05415	.00970	.00107	.00007	.00000
30.	1.00000	1.00000	1.00000	.99998	.99961	.99572	.97108	.87799	.66752	.38253	.15133	.03898	.00631	.00063	.00004	.00000
35.	1.00000	1.00000	1.00000	.99996	.99933	.99338	.95953	.84454	.61079	.32617	.11852	.02779	.00407	.00036	.00002	.00000
40.	1.00000	1.00000	1.00000	.99993	.99890	.99010	.94502	.80688	.55351	.27513	.09188	.01964	.00261	.00021	.00001	.00000
45.	1.00000	1.00000	.99999	.99987	.99825	.98567	.92732	.76554	.49694	.22977	.07058	.01378	.00167	.00012	.00001	.00000
50.	1.00000	1.00000	.99999	.99978	.99730	.97983	.90630	.72120	.44216	.19013	.05377	.00961	.00106	.00007	.00000	.00000
55.	1.00000	1.00000	.99998	.99964	.99596	.97236	.88193	.67465	.39007	.15600	.04067	.00666	.00067	.00004	.00000	.00000
60.	1.00000	1.00000	.99997	.99942	.99411	.96303	.85431	.62672	.34137	.12701	.03056	.00460	.00042	.00002	.00000	.00000
65.	1.00000	1.00000	.99994	.99911	.99165	.95167	.82364	.57824	.29650	.10268	.02284	.00316	.00027	.00001	.00000	.00000
70.	1.00000	1.00000	.99991	.99866	.98843	.93811	.79023	.53001	.25571	.08249	.01698	.00217	.00017	.00001	.00000	.00000
75.	1.00000	.99999	.99985	.99804	.98432	.92227	.75447	.48273	.21911	.06589	.01258	.00148	.00011	.00000	.00000	.00000
80.	1.00000	.99999	.99977	.99719	.97918	.90410	.71680	.43702	.18661	.05236	.00928	.00101	.00007	.00000	.00000	.00000
85.	1.00000	.99998	.99965	.99606	.97290	.88362	.67773	.39337	.15806	.04143	.00683	.00069	.00004	.00000	.00000	.00000
90.	1.00000	.99997	.99948	.99459	.96533	.86089	.63774	.35216	.13320	.03264	.00501	.00047	.00003	.00000	.00000	.00000
95.	1.00000	.99995	.99925	.99270	.95639	.83605	.59733	.31367	.11173	.02563	.00367	.00032	.00002	.00000	.00000	.00000
100.	1.00000	.99993	.99893	.99033	.94599	.80927	.55698	.27807	.09333	.02006	.00268	.00022	.00001	.00000	.00000	.00000
105.	1.00000	.99989	.99851	.98741	.93406	.78078	.51711	.24541	.07767	.01567	.00196	.00015	.00001	.00000	.00000	.00000
110.	.99999	.99984	.99797	.98386	.92057	.75081	.47812	.21570	.06442	.01221	.00143	.00010	.00000	.00000	.00000	.00000
115.	.99999	.99978	.99726	.97960	.90552	.71964	.44033	.18888	.05327	.00949	.00104	.00007	.00000	.00000	.00000	.00000
120.	.99998	.99968	.99637	.97458	.88893	.68756	.40401	.16481	.04393	.00737	.00076	.00005	.00000	.00000	.00000	.00000
125.	.99998	.99956	.99526	.96872	.87083	.65484	.36939	.14335	.03614	.00572	.00055	.00003	.00000	.00000	.00000	.00000
130.	.99996	.99940	.99389	.96197	.85131	.62178	.33661	.12432	.02968	.00443	.00040	.00002	.00000	.00000	.00000	.00000
135.	.99995	.99919	.99224	.95428	.83046	.58865	.30578	.10753	.02432	.00343	.00030	.00002	.00000	.00000	.00000	.00000
140.	.99993	.99892	.99025	.94563	.80839	.55570	.27698	.09279	.01991	.00266	.00022	.00001	.00000	.00000	.00000	.00000
145.	.99990	.99859	.98790	.93598	.78523	.52315	.25020	.07990	.01627	.00206	.00016	.00001	.00000	.00000	.00000	.00000
150.	.99986	.99817	.98514	.92532	.76112	.49122	.22545	.06866	.01329	.00159	.00012	.00001	.00000	.00000	.00000	.00000
155.	.99981	.99765	.98194	.91366	.73621	.46009	.20267	.05891	.01084	.00123	.00009	.00000	.00000	.00000	.00000	.00000
160.	.99975	.99703	.97826	.90099	.71067	.42992	.18181	.05046	.00884	.00095	.00006	.00000	.00000	.00000	.00000	.00000
165.	.99967	.99628	.97408	.88736	.68463	.40082	.16277	.04317	.00720	.00074	.00005	.00000	.00000	.00000	.00000	.00000
170.	.99957	.99539	.96937	.87278	.65826	.37290	.14546	.03689	.00587	.00057	.00003	.00000	.00000	.00000	.00000	.00000
175.	.99945	.99433	.96409	.85731	.63171	.34623	.12978	.03149	.00478	.00045	.00003	.00000	.00000	.00000	.00000	.00000

TDDB: PROBABILITY OF SUCCESS AT 10000. HOURS FOR AREA = 7.00 LOG SQUARE MICRONS

	Current Density (MA/cm2)														
T(C)	.04	.05	.06	.08	.10	.13	.17	.20	.25	.30	.40	.50	.60	.80	1.00	1.30
0.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
5.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
10.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
15.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
20.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000
25.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.57309
30.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000
35.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000
40.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.98748	.00000	.00000
45.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000
50.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.98977	.00000	.00000	.00000
55.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000
60.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000
65.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99890	.00000	.00000	.00000	.00000	.00000
70.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000
75.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000
80.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
85.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.97869	.00000	.00000	.00000	.00000	.00000	.00000	.00000
90.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
95.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.99049	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
100.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
105.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00397	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
110.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
115.	1.00000	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
120.	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
125.	1.00000	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
130.	1.00000	1.00000	1.00000	1.00000	.99945	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
135.	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
140.	1.00000	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
145.	1.00000	1.00000	1.00000	.28800	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
150.	1.00000	1.00000	1.00000	.00002	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
155.	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
160.	1.00000	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
165.	1.00000	1.00000	.00009	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
170.	1.00000	1.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000
175.	1.00000	.50299	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000	.00000

ELECTROMIGRATION: PROBABILITY OF SUCCESS AT 10000. HOURS

	Electric Field Stress (MV/cm)														
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.028	.942	8.851	32.299
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.079	1.865	13.235	40.674
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.003	.194	3.340	18.531	49.459
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.009	.428	5.486	24.599	58.492
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.025	.858	8.368	31.282	67.647
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.061	1.574	11.989	38.425	76.832
30.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.002	.137	2.672	16.301	45.891	85.976
35.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.005	.282	4.232	21.218	53.566	95.032
40.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.013	.538	6.310	26.639	61.358	103.964
45.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.029	.956	8.928	32.460	69.198	112.748
50.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.062	1.594	12.076	38.584	77.030	121.368
55.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.002	.124	2.508	15.715	44.925	84.814	129.812
60.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.004	.232	3.747	19.792	51.411	92.519	138.074
65.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.009	.411	5.347	24.242	57.982	100.123	146.151
70.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.018	.688	7.325	28.999	64.592	107.609	154.042
75.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.035	1.096	9.683	33.999	71.202	114.967	161.747
80.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.067	1.669	12.405	39.186	77.782	122.188	169.267
85.	.000	.000	.000	.000	.000	.000	.000	.000	.002	.119	2.439	15.465	44.507	84.310	129.268	176.601
90.	.000	.000	.000	.000	.000	.000	.000	.000	.003	.202	3.433	18.826	49.921	90.769	136.204	183.747
95.	.000	.000	.000	.000	.000	.000	.000	.000	.006	.330	4.673	22.451	55.390	97.144	142.995	190.695
100.	.000	.000	.000	.000	.000	.000	.000	.000	.012	.518	6.169	26.298	60.884	103.427	149.641	197.419
105.	.000	.000	.000	.000	.000	.000	.000	.000	.022	.784	7.926	30.329	66.379	109.610	156.143	203.859
110.	.000	.000	.000	.000	.000	.000	.000	.000	.038	1.145	9.937	34.506	71.856	115.689	162.501	209.878
115.	.000	.000	.000	.000	.000	.000	.000	.001	.064	1.620	12.192	38.797	77.297	121.659	168.717	215.179
120.	.000	.000	.000	.000	.000	.000	.000	.001	.103	2.227	14.673	43.173	82.691	127.519	174.793	219.128
125.	.000	.000	.000	.000	.000	.000	.000	.002	.162	2.981	17.360	47.607	88.028	133.269	180.728	220.429
130.	.000	.000	.000	.000	.000	.000	.000	.004	.247	3.893	20.230	52.078	93.300	138.907	186.518	216.638
135.	.000	.000	.000	.000	.000	.000	.000	.007	.365	4.972	23.259	56.568	98.501	144.434	192.158	203.835
140.	.000	.000	.000	.000	.000	.000	.000	.012	.525	6.221	26.424	61.060	103.626	149.851	197.630	999.000
145.	.000	.000	.000	.000	.000	.000	.000	.020	.737	7.641	29.703	65.541	108.673	155.160	202.899	999.000
150.	.000	.000	.000	.000	.000	.000	.000	.031	1.010	9.227	33.075	70.002	113.639	160.361	207.898	999.000
155.	.000	.000	.000	.000	.000	.000	.000	.049	1.354	10.973	36.521	74.432	118.523	165.456	212.501	999.000
160.	.000	.000	.000	.000	.000	.000	.001	.073	1.777	12.870	40.025	78.825	123.324	170.447	216.471	999.000
165.	.000	.000	.000	.000	.000	.000	.001	.108	2.289	14.908	43.570	83.175	128.042	175.334	219.380	999.000
170.	.000	.000	.000	.000	.000	.000	.002	.155	2.896	17.072	47.144	87.477	132.676	180.118	220.478	999.000
175.	.000	.000	.000	.000	.000	.000	.004	.218	3.603	19.352	50.735	91.727	137.228	184.798	218.515	999.000

TDDB: HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 4.00 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm) 2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.009	.352	4.312	19.987	49.543
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.026	.742	6.904	26.362	58.687
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.065	1.418	10.283	33.326	67.947
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.003	.151	2.486	14.420	40.720	77.226
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.008	.318	4.041	19.234	48.405	86.454
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.020	.616	6.147	24.622	56.267	95.582
30.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.045	1.105	8.831	30.467	64.218	104.574
35.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.002	.097	1.851	12.084	36.661	72.190	113.407
40.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.004	.193	2.918	15.863	43.107	80.131	122.064
45.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.009	.358	4.356	20.107	49.722	88.003	130.537
50.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.020	.624	6.199	24.744	56.439	95.778	138.818
55.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.041	1.029	8.457	29.700	63.202	103.435	146.906
60.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.079	1.613	11.122	34.905	69.969	110.961	154.799
65.	.000	.000	.000	.000	.000	.000	.000	.000	.003	.145	2.414	14.169	40.297	76.707	118.346	162.499
70.	.000	.000	.000	.000	.000	.000	.000	.000	.006	.251	3.464	17.562	45.821	83.390	125.584	170.007
75.	.000	.000	.000	.000	.000	.000	.000	.000	.011	.415	4.788	21.257	51.431	90.000	132.671	177.323
80.	.000	.000	.000	.000	.000	.000	.000	.000	.022	.656	6.398	25.208	57.088	96.520	139.605	184.444
85.	.000	.000	.000	.000	.000	.000	.000	.000	.039	.998	8.297	29.369	62.762	102.941	146.386	191.360
90.	.000	.000	.000	.000	.000	.000	.000	.001	.068	1.462	10.479	33.699	68.426	109.256	153.015	198.043
95.	.000	.000	.000	.000	.000	.000	.000	.002	.115	2.071	12.927	38.157	74.061	115.458	159.493	204.430
100.	.000	.000	.000	.000	.000	.000	.000	.004	.185	2.843	15.620	42.711	79.652	121.545	165.822	210.375
105.	.000	.000	.000	.000	.000	.000	.000	.007	.288	3.794	18.533	47.330	85.184	127.514	172.003	215.567
110.	.000	.000	.000	.000	.000	.000	.000	.012	.435	4.934	21.638	51.990	90.650	133.365	178.038	219.343
115.	.000	.000	.000	.000	.000	.000	.000	.021	.635	6.269	24.908	56.669	96.041	139.097	183.924	220.367
120.	.000	.000	.000	.000	.000	.000	.000	.034	.902	7.798	28.316	61.350	101.353	144.712	189.659	216.155
125.	.000	.000	.000	.000	.000	.000	.001	.054	1.248	9.516	31.837	66.017	106.581	150.211	195.229	202.838
130.	.000	.000	.000	.000	.000	.000	.001	.084	1.685	11.416	35.448	70.658	111.721	155.594	200.609	999.000
135.	.000	.000	.000	.000	.000	.000	.002	.128	2.222	13.485	39.128	75.265	116.774	160.863	205.750	999.000
140.	.000	.000	.000	.000	.000	.000	.004	.188	2.871	15.710	42.858	79.829	121.737	166.021	210.555	999.000
145.	.000	.000	.000	.000	.000	.000	.006	.270	3.637	18.075	46.622	84.344	126.610	171.069	214.844	999.000
150.	.000	.000	.000	.000	.000	.000	.010	.380	4.526	20.565	50.407	88.805	131.394	176.008	218.285	999.000
155.	.000	.000	.000	.000	.000	.000	.016	.522	5.541	23.164	54.200	93.207	136.088	180.838	220.289	999.000
160.	.000	.000	.000	.000	.000	.000	.024	.703	6.681	25.857	57.991	97.549	140.694	185.559	219.852	999.000
165.	.000	.000	.000	.000	.000	.000	.035	.930	7.945	28.629	61.771	101.828	145.213	190.168	215.391	999.000
170.	.000	.000	.000	.000	.000	.001	.052	1.208	9.329	31.467	65.533	106.041	149.645	194.658	204.767	999.000
175.	.000	.000	.000	.000	.000	.001	.074	1.544	10.828	34.358	69.270	110.190	153.992	199.019	185.815	999.000

TDDB: HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 4.50 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm)															
	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.008	.260	3.056	14.864	39.159	72.499
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.022	.536	4.928	19.930	46.992	81.896
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.001	.052	1.010	7.423	25.591	55.025	91.203
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.003	.116	1.760	10.549	31.718	63.156	100.377
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.007	.236	2.862	14.274	38.192	71.311	109.388
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.017	.447	4.377	18.536	44.909	79.432	118.218
30.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.037	.790	6.344	23.253	51.779	87.477	126.853
35.	.000	.000	.000	.000	.000	.000	.000	.000	.002	.076	1.313	8.774	28.341	58.734	95.415	135.287
40.	.000	.000	.000	.000	.000	.000	.000	.000	.004	.146	2.065	11.657	33.719	65.717	103.225	143.516
45.	.000	.000	.000	.000	.000	.000	.000	.000	.008	.264	3.087	14.958	39.312	72.686	110.892	151.539
50.	.000	.000	.000	.000	.000	.000	.000	.000	.017	.453	4.415	18.633	45.056	79.607	118.407	159.359
55.	.000	.000	.000	.000	.000	.000	.000	.001	.034	.737	6.067	22.629	50.897	86.456	125.763	166.975
60.	.000	.000	.000	.000	.000	.000	.000	.001	.063	1.147	8.050	26.890	56.790	93.214	132.956	174.391
65.	.000	.000	.000	.000	.000	.000	.000	.003	.111	1.709	10.358	31.365	62.700	99.868	139.986	181.604
70.	.000	.000	.000	.000	.000	.000	.000	.005	.188	2.452	12.971	36.005	68.597	106.408	146.852	188.610
75.	.000	.000	.000	.000	.000	.000	.000	.010	.305	3.396	15.864	40.767	74.460	112.827	153.556	195.391
80.	.000	.000	.000	.000	.000	.000	.000	.018	.476	4.559	19.005	45.615	80.270	119.122	160.100	201.900
85.	.000	.000	.000	.000	.000	.000	.001	.032	.715	5.949	22.360	50.515	86.013	125.289	166.486	208.034
90.	.000	.000	.000	.000	.000	.000	.001	.055	1.041	7.569	25.897	55.442	91.680	131.328	172.716	213.568
95.	.000	.000	.000	.000	.000	.000	.002	.089	1.468	9.412	29.582	60.375	97.263	137.239	178.790	218.020
100.	.000	.000	.000	.000	.000	.000	.004	.141	2.012	11.470	33.386	65.294	102.755	143.023	184.709	220.400
105.	.000	.000	.000	.000	.000	.000	.006	.215	2.686	13.726	37.282	70.186	108.154	148.680	190.466	218.805
110.	.000	.000	.000	.000	.000	.000	.011	.319	3.502	16.164	41.245	75.038	113.457	154.212	196.049	209.999
115.	.000	.000	.000	.000	.000	.000	.018	.461	4.466	18.765	45.254	79.842	118.661	159.622	201.430	189.827
120.	.000	.000	.000	.000	.000	.000	.028	.648	5.582	21.507	49.292	84.591	123.766	164.911	206.552	999.000
125.	.000	.000	.000	.000	.000	.001	.044	.891	6.851	24.371	53.343	89.277	128.773	170.082	211.308	999.000
130.	.000	.000	.000	.000	.000	.001	.067	1.197	8.271	27.338	57.393	93.898	133.681	175.136	215.498	999.000
135.	.000	.000	.000	.000	.000	.002	.099	1.574	9.836	30.389	61.432	98.449	138.491	180.074	218.753	999.000
140.	.000	.000	.000	.000	.000	.004	.143	2.031	11.539	33.509	65.451	102.929	143.205	184.895	220.424	999.000
145.	.000	.000	.000	.000	.000	.006	.202	2.574	13.370	36.682	69.442	107.336	147.824	189.598	219.415	999.000
150.	.000	.000	.000	.000	.000	.009	.280	3.209	15.319	39.895	73.398	111.669	152.350	194.177	214.046	999.000
155.	.000	.000	.000	.000	.000	.014	.381	3.938	17.374	43.135	77.315	115.928	156.784	198.619	202.101	999.000
160.	.000	.000	.000	.000	.000	.020	.509	4.765	19.525	46.392	81.189	120.112	161.127	202.905	181.640	999.000
165.	.000	.000	.000	.000	.000	.029	.668	5.690	21.760	49.657	85.016	124.221	165.382	206.998	999.000	999.000
170.	.000	.000	.000	.000	.001	.042	.863	6.712	24.068	52.922	88.793	128.257	169.551	210.836	999.000	999.000
175.	.000	.000	.000	.000	.001	.059	1.098	7.830	26.439	56.180	92.520	132.220	173.633	214.319	999.000	999.000

TDDB: HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 5.00 LOG SQUARE MICRONS

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.018	.367	3.283	14.050	35.460	65.009	99.243
5.	.000	.000	.000	.000	.000	.000	.000	.000	.001	.041	.693	5.065	18.531	42.371	73.400	108.425
10.	.000	.000	.000	.000	.000	.000	.000	.000	.003	.090	1.217	7.369	23.517	49.477	81.733	117.410
15.	.000	.000	.000	.000	.000	.000	.000	.000	.007	.180	1.999	10.199	28.908	56.693	89.967	126.186
20.	.000	.000	.000	.000	.000	.000	.000	.000	.016	.337	3.094	13.526	34.607	63.951	98.072	134.744
25.	.000	.000	.000	.000	.000	.000	.000	.001	.033	.591	4.546	17.300	40.530	71.197	106.029	143.082
30.	.000	.000	.000	.000	.000	.000	.000	.002	.066	.979	6.379	21.459	46.604	78.393	113.824	151.200
35.	.000	.000	.000	.000	.000	.000	.000	.004	.124	1.539	8.599	25.937	52.766	85.510	121.448	159.100
40.	.000	.000	.000	.000	.000	.000	.000	.009	.221	2.307	11.192	30.668	58.970	92.526	128.896	166.784
45.	.000	.000	.000	.000	.000	.000	.000	.018	.372	3.314	14.133	35.594	65.176	99.427	136.167	174.255
50.	.000	.000	.000	.000	.000	.000	.001	.034	.598	4.582	17.386	40.661	71.354	106.200	143.260	181.512
55.	.000	.000	.000	.000	.000	.000	.002	.061	.921	6.124	20.909	45.823	77.479	112.839	150.177	188.551
60.	.000	.000	.000	.000	.000	.000	.003	.105	1.363	7.942	24.660	51.042	83.536	119.340	156.920	195.354
65.	.000	.000	.000	.000	.000	.000	.007	.173	1.947	10.027	28.597	56.288	89.509	125.700	163.491	201.877
70.	.000	.000	.000	.000	.000	.000	.012	.275	2.692	12.366	32.681	61.533	95.389	131.919	169.893	208.018
75.	.000	.000	.000	.000	.000	.000	.021	.422	3.612	14.936	36.877	66.758	101.169	137.996	176.129	213.551
80.	.000	.000	.000	.000	.000	.001	.036	.624	4.718	17.714	41.154	71.946	106.844	143.933	182.199	218.002
85.	.000	.000	.000	.000	.000	.002	.059	.896	6.015	20.673	45.485	77.083	112.411	149.733	188.100	220.394
90.	.000	.000	.000	.000	.000	.003	.093	1.251	7.503	23.786	49.848	82.160	117.868	155.396	193.824	218.859
95.	.000	.000	.000	.000	.000	.005	.143	1.699	9.176	27.028	54.223	87.169	123.214	160.926	199.349	210.236
100.	.000	.000	.000	.000	.000	.009	.213	2.254	11.025	30.375	58.594	92.104	128.450	166.324	204.631	190.488
105.	.000	.000	.000	.000	.000	.014	.310	2.923	13.039	33.805	62.948	96.961	133.575	171.595	209.587	999.000
110.	.000	.000	.000	.000	.000	.022	.439	3.713	15.203	37.298	67.274	101.737	138.591	176.738	214.052	999.000
115.	.000	.000	.000	.000	.001	.035	.607	4.630	17.502	40.836	71.564	106.429	143.499	181.756	217.727	999.000
120.	.000	.000	.000	.000	.001	.052	.821	5.675	19.921	44.403	75.810	111.036	148.302	186.647	220.074	999.000
125.	.000	.000	.000	.000	.002	.077	1.089	6.846	22.443	47.988	80.006	115.558	153.001	191.409	220.164	999.000
130.	.000	.000	.000	.000	.004	.111	1.416	8.142	25.054	51.577	84.149	119.995	157.598	196.034	216.522	999.000
135.	.000	.000	.000	.000	.006	.156	1.809	9.558	27.739	55.161	88.235	124.347	162.095	200.505	207.069	999.000
140.	.000	.000	.000	.000	.009	.216	2.273	11.087	30.484	58.733	92.261	128.615	166.495	204.795	189.618	999.000
145.	.000	.000	.000	.000	.013	.293	2.813	12.721	33.277	62.285	95.225	132.800	170.798	208.857	999.000	999.000
150.	.000	.000	.000	.000	.019	.391	3.431	14.453	36.107	65.811	100.126	136.902	175.008	212.607	999.000	999.000
155.	.000	.000	.000	.001	.028	.513	4.131	16.273	38.965	69.306	103.964	140.924	179.125	215.913	999.000	999.000
160.	.000	.000	.000	.001	.039	.663	4.912	18.174	41.840	72.767	107.738	144.866	183.150	218.555	999.000	999.000
165.	.000	.000	.000	.001	.054	.843	5.775	20.144	44.726	76.190	111.447	148.730	187.082	220.192	999.000	999.000
170.	.000	.000	.000	.002	.074	1.058	6.719	22.177	47.615	79.573	115.093	152.518	190.921	220.296	999.000	999.000
175.	.000	.000	.000	.003	.099	1.311	7.741	24.263	50.501	82.913	118.674	156.231	194.663	218.116	999.000	999.000

TDDB: HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 5.50 LOG SQUARE MICRONS

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.000	.002	.050	.650	4.220	15.046	34.850	61.566	92.463	125.712
5.	.000	.000	.000	.000	.000	.000	.000	.005	.103	1.116	6.139	19.279	41.121	69.133	100.765	134.427
10.	.000	.000	.000	.000	.000	.000	.000	.010	.197	1.802	8.512	23.915	47.549	76.651	108.895	142.904
15.	.000	.000	.000	.000	.000	.000	.001	.022	.355	2.755	11.326	28.873	54.064	84.084	116.841	151.143
20.	.000	.000	.000	.000	.000	.000	.002	.045	.604	4.010	14.545	34.075	60.611	91.406	124.597	159.148
25.	.000	.000	.000	.000	.000	.000	.004	.085	.974	5.590	18.124	39.454	67.147	98.598	132.158	166.922
30.	.000	.000	.000	.000	.000	.000	.008	.153	1.497	7.504	22.009	44.951	73.638	105.649	139.525	174.467
35.	.000	.000	.000	.000	.000	.000	.015	.260	2.202	9.745	26.146	50.519	80.061	112.550	146.699	181.786
40.	.000	.000	.000	.000	.000	.001	.028	.422	3.115	12.295	30.483	56.118	86.396	119.297	153.682	188.873
45.	.000	.000	.000	.000	.000	.002	.050	.657	4.253	15.126	34.972	61.716	92.629	125.887	160.477	195.711
50.	.000	.000	.000	.000	.000	.004	.087	.984	5.628	18.205	39.572	67.288	98.752	132.320	167.088	202.253
55.	.000	.000	.000	.000	.000	.007	.142	1.421	7.242	21.498	44.245	72.814	104.758	138.597	173.518	208.391
60.	.000	.000	.000	.000	.000	.012	.225	1.986	9.089	24.970	48.963	78.279	110.642	144.718	179.769	213.890
65.	.000	.000	.000	.000	.001	.022	.344	2.694	11.157	28.588	53.698	83.671	116.401	150.688	185.841	218.247
70.	.000	.000	.000	.000	.001	.036	.510	3.556	13.431	32.320	58.430	88.981	122.036	156.509	191.727	220.442
75.	.000	.000	.000	.000	.002	.058	.731	4.582	15.890	36.138	63.143	94.204	127.545	162.183	197.413	218.539
80.	.000	.000	.000	.000	.004	.091	1.021	5.773	18.513	40.019	67.822	99.335	132.931	167.714	202.863	209.296
85.	.000	.000	.000	.000	.007	.138	1.389	7.130	21.278	43.940	72.456	104.371	138.193	173.105	208.008	188.712
90.	.000	.000	.000	.000	.011	.204	1.845	8.647	24.164	47.883	77.037	109.309	143.335	178.358	212.711	999.000
95.	.000	.000	.000	.001	.017	.293	2.397	10.318	27.149	51.834	81.558	114.150	148.357	183.473	216.719	999.000
100.	.000	.000	.000	.001	.027	.411	3.053	12.132	30.215	55.779	86.014	118.892	153.264	188.450	219.566	999.000
105.	.000	.000	.000	.001	.041	.563	3.817	14.078	33.344	59.706	90.402	123.537	158.056	193.285	220.443	999.000
110.	.000	.000	.000	.002	.061	.757	4.692	16.143	36.520	63.608	94.717	128.085	162.738	197.965	218.017	999.000
115.	.000	.000	.000	.004	.088	.997	5.679	18.314	39.730	67.477	98.959	132.537	167.310	202.470	210.334	999.000
120.	.000	.000	.000	.006	.125	1.289	6.777	20.578	42.961	71.307	103.127	136.895	171.776	206.762	195.099	999.000
125.	.000	.000	.000	.009	.173	1.639	7.982	22.922	46.202	75.094	107.218	141.160	176.138	210.775	999.000	999.000
130.	.000	.000	.000	.013	.236	2.051	9.290	25.333	49.445	78.832	111.235	145.334	180.397	214.399	999.000	999.000
135.	.000	.000	.001	.019	.315	2.529	10.695	27.801	52.681	82.520	115.176	149.420	184.553	217.449	999.000	999.000
140.	.000	.000	.001	.028	.415	3.076	12.192	30.314	55.904	86.156	119.042	153.419	188.607	219.630	999.000	999.000
145.	.000	.000	.001	.039	.538	3.693	13.773	32.863	59.108	89.737	122.834	157.332	192.556	220.483	999.000	999.000
150.	.000	.000	.002	.053	.686	4.383	15.430	35.439	62.289	93.262	126.553	161.162	196.396	219.319	999.000	999.000
155.	.000	.000	.003	.073	.864	5.145	17.157	38.034	65.441	96.731	130.200	164.912	200.117	215.184	999.000	999.000
160.	.000	.000	.004	.097	1.074	5.978	18.944	40.640	68.563	100.143	133.776	168.581	203.705	206.878	999.000	999.000
165.	.000	.000	.006	.129	1.318	6.881	20.786	43.253	71.650	103.498	137.283	172.174	207.136	193.318	999.000	999.000
170.	.000	.000	.009	.167	1.600	7.852	22.675	45.866	74.702	106.797	140.721	175.690	210.374	999.000	999.000	999.000
175.	.000	.000	.012	.215	1.921	8.887	24.604	48.474	77.717	110.039	144.093	179.131	213.363	999.000	999.000	999.000

TDDB: HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 6.00 LOG SQUARE MICRONS

	Electric Field Stress (MV/cm)															
T(C)	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.000	.000	.007	.121	1.076	5.347	16.293	34.848	59.270	87.388	117.681	149.261
5.	.000	.000	.000	.000	.000	.001	.016	.224	1.707	7.403	20.340	40.609	66.159	94.946	125.632	157.449
10.	.000	.000	.000	.000	.000	.001	.032	.390	2.571	9.850	24.706	46.490	72.999	102.351	133.370	165.387
15.	.000	.000	.000	.000	.000	.003	.062	.644	3.701	12.664	29.325	52.435	79.762	109.592	140.896	173.081
20.	.000	.000	.000	.000	.000	.007	.112	1.011	5.116	15.809	34.134	58.401	86.425	116.664	148.212	180.534
25.	.000	.000	.000	.000	.000	.013	.192	1.520	6.824	19.242	39.080	64.351	92.972	123.562	155.320	187.742
30.	.000	.000	.000	.000	.001	.025	.314	2.194	8.821	22.917	44.115	70.258	99.394	130.286	162.226	194.691
35.	.000	.000	.000	.000	.002	.044	.494	3.053	11.093	26.790	49.202	76.101	105.681	136.836	168.934	201.340
40.	.000	.000	.000	.000	.004	.075	.746	4.114	13.618	30.817	54.308	81.866	111.831	143.216	175.447	207.593
45.	.000	.000	.000	.000	.007	.123	1.087	5.384	16.370	34.961	59.407	87.539	117.841	149.426	181.768	213.234
50.	.000	.000	.000	.000	.013	.194	1.532	6.864	19.319	39.188	64.479	93.113	123.710	155.472	187.895	217.801
55.	.000	.000	.000	.001	.023	.296	2.098	8.551	22.437	43.470	69.508	98.582	129.438	161.357	193.820	220.350
60.	.000	.000	.000	.002	.037	.437	2.794	10.433	25.693	47.781	74.480	103.942	135.028	167.084	199.521	219.059
65.	.000	.000	.000	.003	.060	.627	3.631	12.498	29.061	52.102	79.386	109.191	140.480	172.657	204.951	210.854
70.	.000	.000	.000	.005	.092	.875	4.613	14.728	32.515	56.415	84.219	114.329	145.799	178.079	210.014	191.714
75.	.000	.000	.000	.009	.138	1.190	5.742	17.106	36.034	60.706	88.973	119.353	150.986	183.352	214.530	999.000
80.	.000	.000	.001	.014	.202	1.581	7.018	19.613	39.598	64.965	93.644	124.267	156.045	188.474	218.155	999.000
85.	.000	.000	.001	.022	.288	2.057	8.435	22.229	43.190	69.182	98.230	129.070	160.979	193.441	220.274	999.000
90.	.000	.000	.002	.033	.401	2.623	9.987	24.939	46.795	73.350	102.728	133.764	165.790	198.241	219.828	999.000
95.	.000	.000	.002	.050	.546	3.284	11.665	27.724	50.402	77.464	107.139	138.351	170.482	202.851	215.152	999.000
100.	.000	.000	.004	.072	.728	4.044	13.458	30.569	53.998	81.519	111.462	142.834	175.058	207.229	204.027	999.000
105.	.000	.000	.006	.103	.953	4.903	15.357	33.460	57.577	85.511	115.697	147.214	179.519	211.299	184.297	999.000
110.	.000	.000	.009	.144	1.225	5.862	17.349	36.386	61.130	89.439	119.846	151.493	183.866	214.936	999.000	999.000
115.	.000	.001	.014	.197	1.550	6.919	19.423	39.334	64.652	93.301	123.907	155.676	188.101	217.929	999.000	999.000
120.	.000	.001	.020	.264	1.930	8.069	21.569	42.294	68.137	97.096	127.885	159.762	192.220	219.936	999.000	999.000
125.	.000	.001	.028	.349	2.371	9.310	23.775	45.259	71.582	100.824	131.778	163.756	196.219	220.423	999.000	999.000
130.	.000	.002	.039	.454	2.873	10.636	26.032	48.222	74.983	104.483	135.590	167.659	200.088	218.599	999.000	999.000
135.	.000	.003	.054	.581	3.439	12.040	28.330	51.175	78.339	108.075	139.322	171.474	203.812	213.389	999.000	999.000
140.	.000	.004	.073	.734	4.070	13.517	30.661	54.113	81.647	111.599	142.975	175.202	207.364	203.534	999.000	999.000
145.	.000	.006	.098	.916	4.766	15.061	33.017	57.032	84.906	115.057	146.552	178.845	210.702	187.885	999.000	999.000
150.	.000	.008	.129	1.127	5.526	16.664	35.391	59.928	88.115	118.449	150.053	182.405	213.762	999.000	999.000	999.000
155.	.000	.011	.167	1.372	6.349	18.320	37.776	62.798	91.273	121.776	153.482	185.881	216.448	999.000	999.000	999.000
160.	.001	.015	.214	1.651	7.236	20.022	40.168	65.639	94.379	125.039	156.839	189.275	218.614	999.000	999.000	999.000
165.	.001	.020	.271	1.968	8.178	21.765	42.561	68.449	97.435	128.239	160.126	192.585	220.051	999.000	999.000	999.000
170.	.001	.027	.339	2.322	9.177	23.543	44.951	71.226	100.440	131.378	163.346	195.809	220.463	999.000	999.000	999.000
175.	.002	.036	.420	2.716	10.230	25.351	47.334	73.969	103.393	134.456	166.499	198.943	219.448	999.000	999.000	999.000

TDDB: HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 6.50 LOG SQUARE MICRONS

T(C)	Electric Field Stress (MV/cm)															
	2.0	2.2	2.4	2.6	2.8	3.0	3.2	3.4	3.6	3.8	4.0	4.2	4.4	4.6	4.8	5.0
0.	.000	.000	.000	.000	.001	.022	.242	1.591	6.433	17.338	34.760	57.235	83.006	110.796	139.823	169.620
5.	.000	.000	.000	.000	.003	.042	.410	2.373	8.571	21.197	40.083	63.551	89.935	118.099	147.358	177.293
10.	.000	.000	.000	.000	.005	.078	.662	3.390	11.044	25.314	45.499	69.820	96.727	125.210	154.668	184.709
15.	.000	.000	.000	.000	.011	.135	1.020	4.659	13.822	29.631	50.963	76.017	103.371	132.129	161.758	191.860
20.	.000	.000	.000	.001	.020	.225	1.508	6.188	16 [illegible]	34.098	56.438	82.124	109.862	138.857	168.634	198.718
25.	.000	.000	.000	.002	.036	.359	2.146	7.976	20	38.672	61.893	88.126	116.197	145.399	175.301	205.213
30.	.000	.000	.000	.004	.061	.549	2.952	10.011	23.652	43.314	67.307	94.014	122.375	151.757	181.760	211.183
35.	.000	.000	.000	.007	.101	.811	3.938	12.278	27.265	47.993	72.662	99.782	128.396	157.936	188.012	216.274
40.	.000	.000	.001	.013	.160	1.158	5.111	14.752	31.020	52.682	77.945	105.426	134.262	163.940	194.047	219.744
45.	.000	.000	.001	.022	.244	1.605	6.472	17.411	34.864	57.361	83.145	110.943	139.975	169.774	199.843	220.129
50.	.000	.000	.002	.036	.362	2.162	8.017	20.229	38.772	62.011	88.255	116.333	145.538	175.443	205.349	214.778
55.	.000	.000	.004	.057	.521	2.839	9.739	23.179	42.720	66.620	93.270	121.596	150.956	180.948	210.461	199.866
60.	.000	.000	.006	.088	.730	3.644	11.624	26.239	46.687	71.176	98.187	126.733	156.231	186.290	214.976	999.000
65.	.000	.000	.010	.131	.997	4.581	13.659	29.385	50.657	75.672	103.003	131.747	161.367	191.467	218.517	999.000
70.	.000	.001	.016	.191	1.330	5.650	15.829	32.597	54.616	80.101	107.718	136.638	166.368	196.470	220.396	999.000
75.	.000	.001	.025	.271	1.736	6.849	18.117	35.858	58.552	84.459	112.332	141.410	171.238	201.280	219.445	999.000
80.	.000	.002	.038	.376	2.221	8.175	20.507	39.151	62.457	88.741	116.845	146.066	175.979	205.860	213.833	999.000
85.	.000	.004	.056	.510	2.791	9.621	22.984	42.462	66.322	92.947	121.257	150.608	180.595	210.143	201.211	999.000
90.	.000	.006	.080	.678	3.449	11.180	25.532	45.781	70.141	97.073	125.572	155.039	185.085	214.014	999.000	999.000
95.	.000	.008	.113	.885	4.197	12.841	28.138	49.095	73.911	101.120	129.789	159.363	189.450	217.275	999.000	999.000
100.	.001	.013	.155	1.135	5.034	14.597	30.789	52.398	77.627	105.087	133.910	163.581	193.688	219.603	999.000	999.000
105.	.001	.018	.210	1.432	5.961	16.436	33.474	55.682	81.286	108.975	137.939	167.697	197.790	220.481	999.000	999.000
110.	.001	.026	.280	1.780	6.979	18.350	36.183	58.941	84.887	112.784	141.877	171.714	201.745	219.128	999.000	999.000
115.	.002	.037	.367	2.183	8.073	20.327	38.907	62.169	88.427	116.515	145.726	175.633	205.531	214.459	999.000	999.000
120.	.003	.051	.473	2.641	9.251	22.360	41.637	65.364	91.907	120.169	149.488	179.458	209.110	205.115	999.000	999.000
125.	.005	.069	.602	3.158	10.503	24.439	44.367	68.521	95.326	123.747	153.166	183.188	212.427	189.953	999.000	999.000
130.	.007	.092	.755	3.734	11.825	26.556	47.092	71.638	98.683	127.250	156.761	186.826	215.391	999.000	999.000	999.000
135.	.009	.121	.935	4.369	13.211	28.703	49.806	74.713	101.978	130.681	160.277	190.371	217.867	999.000	999.000	999.000
140.	.013	.157	1.143	5.063	14.654	30.874	52.504	77.745	105.213	134.041	163.714	193.821	219.656	999.000	999.000	999.000
145.	.017	.201	1.383	5.814	16.151	33.063	55.182	80.731	108.387	137.330	167.075	197.173	220.468	999.000	999.000	999.000
150.	.023	.255	1.656	6.622	17.693	35.262	57.839	83.672	111.501	140.552	170.363	200.422	219.899	999.000	999.000	999.000
155.	.031	.319	1.964	7.484	19.277	37.469	60.470	86.567	114.556	143.707	173.578	203.557	217.414	999.000	999.000	999.000
160.	.040	.395	2.306	8.398	20.896	39.677	63.075	89.416	117.554	146.796	176.722	206.564	212.350	999.000	999.000	999.000
165.	.052	.484	2.686	9.361	22.546	41.883	65.650	92.218	120.494	149.823	179.798	209.421	204.031	999.000	999.000	999.000
170.	.067	.587	3.102	10.370	24.221	44.084	68.195	94.973	123.378	152.788	182.805	212.097	191.807	999.000	999.000	999.000
175.	.084	.706	3.555	11.422	25.918	46.276	70.708	97.683	126.208	155.692	185.745	214.546	999.000	999.000	999.000	999.000

TDDB: HAZARD RATE (x 10E-6) AT 10000. HOURS FOR AREA = 7.00 LOG SQUARE MICRONS

	Current Density (MA/cm2)															
T(C)	.04	.05	.06	.08	.10	.13	.17	.20	.25	.30	.40	.50	.60	.80	1.00	1.30
0.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
5.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
10.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
15.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
20.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000
25.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	29.723
30.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000
35.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000
40.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	1.425	999.000	999.000
45.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000
50.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	1.193	999.000	999.000	999.000
55.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000
60.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000
65.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	.160	999.000	999.000	999.000	999.000	999.000
70.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000
75.	.000	.000	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000
80.	.000	.000	.000	.000	.000	.000	.000	.000	.000	211.909	999.000	999.000	999.000	999.000	999.000	999.000
85.	.000	.000	.000	.000	.000	.000	.000	.000	2.268	999.000	999.000	999.000	999.000	999.000	999.000	999.000
90.	.000	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
95.	.000	.000	.000	.000	.000	.000	.000	1.119	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
100.	.000	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
105.	.000	.000	.000	.000	.000	.000	128.728	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
110.	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
115.	.000	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
120.	.000	.000	.000	.000	.000	206.955	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
125.	.000	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
130.	.000	.000	.000	.000	.085	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
135.	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
140.	.000	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
145.	.000	.000	.000	51.451	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
150.	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
155.	.000	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
160.	.000	.000	.001	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
165.	.000	.000	172.552	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
170.	.000	.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000
175.	.000	36.445	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000	999.000

ELECTROMIGRATION: HAZARD RATE (x 10E-6) AT 10000. HOURS

APPENDIX E

MEMORY LIFE TEST DATA

TYPE	PARTNUM	TECH	MBITS	ARRAYTECH		TEST	YR	DUR	DEVHRS	MTEST	NFAIL	FDESC	FMECHNSM
EEPROM	2816A	-MOS	16K	FLGATE SV	FLGA FX	125DLIFE	84		7.72E5		1		
EEPROM	S2813	-MOS	16K	FLGATE SV	FLGA FX	125DLIFE	84		6.84E5		1		
EEPROM	S2833	-MOS	64K	FLGATE SV	FLGA FX	125DLIFE	84		6.58E5		1		
EEPROM	X2816A	NMOS	16K	FLGATE SV	FLGA TP	125DLIFE	87		1.26E6		2	?, 1 RETENTION	1 IONCONTAM, ?
EEPROM	X2816B	NMOS	16K	FLGATE SV	FLGA TP	125DLIFE	87		7.73E6		0		
EEPROM	X2404	NMOS	4K	FLGATE SV	FLGA TP	125DLIFE	87		1.49E6		2	?, ?	2 OXIDE BRKDWN
EEPROM	X2864A	NMOS	64K	FLGATE SV	FLGA TP	125DLIFE	87		3.29E6		5	?,?,?,?, 1 RETENTION	4 IONCONTAM, ?
FPGA	82S103	TTL	297	NiCr FUSE	NiCr	DNTLIFE	80	1000		50	0		
FPLA	82S101	TTL	1832	NiCr FUSE	NiCr	DNTLIFE	84	1000		48	0		
FPLA	82S101	TTL	1832	NiCr FUSE	NiCr	DNTLIFE	84	1000		50	0		
FPLA	82S153	TTL	1842	NiCr FUSE	NiCr	DNTLIFE	83	1000		48	1	1 SHORTED WIRE	1 ASSY ERROR
FPLA	PLS153	TTL	1842	NiCr FUSE	NiCr	DNTLIFE	86	1000		100	0		
FPLA	PLS153	TTL	1842	NiCr FUSE	NiCr	DNTLIFE	87	1000		88	0		
FPLA	PLS153	TTL	1852	NiCr FUSE	NiCr	DNTLIFE	87	1000		100	0		
FPLA	PLS153	TTL	1852	NiCr FUSE	NiCr	DNTLIFE	87	1000		109	0		
FPLA	82S100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	80	1000		53	0		
FPLA	82S100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	82	1000		50	0		
FPLA	82S100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	84	1000		50	0		
FPLA	82S100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	85	1000		99	0		
FPLA	PLS100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	85	1000		100	0		
FPLA	PLS100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	88	1000		100	0		
FPLA	PLS100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	88	1000		100	0		
FPLA	PLS100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	88	1000		100	0		
FPLA	PLS100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	88	1000		100	0		
FPLA	PLS100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	88	1000		100	0		
FPLA	PLS100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	88	1000		100	1	1 ACPARAM	?
FPLA	PLS100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	88	1000		51	0		
FPLA	PLS100	TTL	1928	NiCr FUSE	NiCr	DNTLIFE	88	1000		99	0		
FPLA	PLS173	TTL	2618	NiCr FUSE	NiCr	DNTLIFE	86	1000		100	0		
FPLA	PLS151	TTL	564	NiCr FUSE	NiCr	DNTLIFE	86	1000		99	1	1 ACFUNC	?
FPLS	PLS159	TTL	2011	NiCr FUSE	NiCr	DNTLIFE	86	1000		94	0		
FPLS	PLS157	TTL	2016	NiCr FUSE	NiCr	DNTLIFE	86	1000		95	0		
FPLS	82S167	TTL	3360	NiCr FUSE	NiCr	DNTLIFE	84	1000		50	0		
FPLS	82S105	TTL	3552	NiCr FUSE	NiCr	DNTLIFE	82	1000		40	0		
FPLS	82S105	TTL	3552	NiCr FUSE	NiCr	DNTLIFE	83	1000		50	0		
FPLS	82S105	TTL	3552	NiCr FUSE	NiCr	DNTLIFE	83	1000		50	0		
FPLS	82S105	TTL	3552	NiCr FUSE	NiCr	DNTLIFE	83	1000		50	0		
FPLS	82S105	TTL	3552	NiCr FUSE	NiCr	DNTLIFE	83	1000		50	0		
FPLS	82S105	TTL	3552	NiCr FUSE	NiCr	DNTLIFE	83	1000		50	2	2 SHORTED WIRE	2 ASSY ERROR
FPLS	82S105	TTL	3552	NiCr FUSE	NiCr	DNTLIFE	84	1000		50	0		

TYPE	PARTNUM	TECH	#BITS	ARRAYTECH		TEST	YR	QUR	DEVHRS	NTEST	NFAIL	FDESC	FMECHNSM
FPLS	82S105A	TTL	3552	NICr FUSE	NICr	DNTLIFE	84	1000		50	1	1 OPEN WIRE	1 DEFECT WIREBOND
FPLS	PLS105	TTL	3552	NICr FUSE	NICr	DNTLIFE	86	1000		99	0		
PROM	82HS6618			FUSE	FUSE	HTOLIFE	87	1000		88	0		
PROM	P/N27C256	CMOS	256K	FLGATE 12.5V	FLGA	1250LIFE	87		1.29E5		0		
PROM	P/N27C256	CMOS	256K	FLGATE 12.5V	FLGA	1250LIFE	87		9.53E5		5	4 GROSSFUNC, 1 LEAKAGE	?, ?
PROM	10149	ECL				SNTLIFE	80	1000		46	0		
PROM	10149	ECL				SNTLIFE	80	1000		50	0		
PROM	P27128A	NMOS	128K	FLGATE 12.5V	FLGA	1250LIFE	84		8.51E5		0		
PROM	P27128A	NMOS	128K	FLGATE 12.5V	FLGA	125VDLIFE	87		4.68E6		7	1 SPEED, 1 NBCG, 3 NBCL, 2 SBCL	?, ?, ?, ?
PROM	P27128A	NMOS	128K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		1.05E5		0		
PROM	P27256	NMOS	256K	FLGATE 12.5V	FLGA	1250LIFE	87		3.56E6		8	2 SBCL, 3 DECODE, 2 SBCG, 1 NBCG	?, ?, ?, ?
PROM	P27256	NMOS	256K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		4.75E4		1	1 SBCL	?
PROM	P2732A	NMOS	32K	FLGATE 21V	FLGA	1250LIFE	84		3.67E6		4	1 TY DECODE, 3 RSB CHARGE LOSS	?,?
PROM	P2764A	NMOS	64K	FLGATE 12.5V	FLGA	1250LIFE	84		8.94E6		0		
PROM	82S187A	TTL		FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82HS641	TTL		FUSE	FUSE	HTOLIFE	88	1000		99	0		
PROM	82S114	TTL		FUSE	FUSE	DNTLIFE	81	1000		63	0		
PROM	82S115	TTL		FUSE	FUSE	DNTLIFE	80	1000		50	0		
PROM	82S115	TTL		FUSE	FUSE	DNTLIFE	81	1000		50	0		
PROM	82S115	TTL		FUSE	FUSE	DNTLIFE	84	1000		40	0		
PROM	82S135	TTL		FUSE	FUSE	HTOLIFE	87	1000		96	0		
PROM	82S141	TTL		FUSE	FUSE	DNTLIFE	84	1000		90	0		
PROM	82S167	TTL		FUSE	FUSE	DNTLIFE	84	1000		50	0		
PROM	82S167A	TTL		FUSE	FUSE	DNTLIFE	84	1000		54	0		
PROM	82S191	TTL	16K	FUSE	FUSE	DNTLIFE	81	1000		44	0		
PROM	82S191	TTL	16K	FUSE	FUSE	DNTLIFE	82	1000		45	0		
PROM	82S191	TTL	16K	FUSE	FUSE	DNTLIFE	84	1000		50	0		
PROM	82S191	TTL	16K	FUSE	FUSE	DNTLIFE	84	1000		50	0		
PROM	82S191	TTL	16K	FUSE	FUSE	DNTLIFE	84	1000		66	0		
PROM	82S191	TTL	16K	FUSE	FUSE	DNTLIFE	85	1000		100	0		
PROM	82S191	TTL	16K	FUSE	FUSE	HTOLIFE	87	1000		71	0		
PROM	82S191	TTL	16K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S191A	TTL	16K	FUSE	FUSE	DNTLIFE	84	1000		50	0		
PROM	82S191A	TTL	16K	FUSE	FUSE	DNTLIFE	85	1000		100	0		
PROM	82S191A	TTL	16K	FUSE	FUSE	DNTLIFE	85	1000		100	0		
PROM	82S191A	TTL	16K	FUSE	FUSE	DNTLIFE	85	1000		90	0		
PROM	82S191A	TTL	16K	FUSE	FUSE	DNTLIFE	85	1000		90	1	1 PARAM FAIL	?
PROM	82S191A	TTL	16K	FUSE	FUSE	DNTLIFE	85	1000		99	0		
PROM	82S191A	TTL	16K	FUSE	FUSE	DNTLIFE	86	1000		90	2	2 LIMIT FAILURES (ICC MARG)	?
PROM	82S191B	TTL	16K	FUSE	FUSE	DNTLIFE	85	1000		89	0		

TYPE	PARTNUM	TECH	BITS	ARRAYTECH		TEST	YR	QUR	DEVHRS	NTEST	NFAIL	FDESC	FMECHNSM
PROM	82S191B	TTL	16K	FUSE	FUSE	DNTLIFE	85	1000		90	0		
PROM	82S191B	TTL	16K	FUSE	FUSE	DNTLIFE	85	1000		90	2	2 PARAM (MARG ICC)	?
PROM	82S126A	TTL	1K	FUSE	FUSE	HTOLIFE	87	1000		90	0		
PROM	82S129	TTL	1K	FUSE	FUSE	HTOLIFE	87	1000		100	0		
PROM	82S129	TTL	1K	FUSE	FUSE	HTOLIFE	87	1000		95	0		
PROM	82S129	TTL	1K	FUSE	FUSE	HTOLIFE	88	1000		94	0		
PROM	82S129A	TTL	1K	FUSE	FUSE	HTOLIFE	87	1000		100	0		
PROM	82S129A	TTL	1K	FUSE	FUSE	HTOLIFE	87	1000		99	0		
PROM	82S129A	TTL	1K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S129A	TTL	1K	FUSE	FUSE	HTOLIFE	88	1000		100	1	1 AC PARAM	?
PROM	82S185	TTL	1K	FUSE	FUSE	HTOLIFE	88	1000		165	2	2 ACFUNC SLOPATT	?
PROM	82S185A	TTL	1K	FUSE	FUSE	HTOLIFE	88	1000		150	0		
PROM	82S123	TTL	256	FUSE	FUSE	DNTLIFE	83	1000		50	0		
PROM	82S123	TTL	256	FUSE	FUSE	DNTLIFE	83	1000		50	0		
PROM	82S123	TTL	256	FUSE	FUSE	DNTLIFE	84	1000		100	0		
PROM	82S123	TTL	256	FUSE	FUSE	DNTLIFE	84	1000		50	0		
PROM	82S123A	TTL	256	FUSE	FUSE	DNTLIFE	85	1000		100	0		
PROM	82S123A	TTL	256	FUSE	FUSE	DNTLIFE	85	1000		99	0		
PROM	82S123A	TTL	256	FUSE	FUSE	HTOLIFE	87	1000		100	0		
PROM	82S123A	TTL	256	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S123A	TTL	256	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S23	TTL	256	FUSE	FUSE	DNTLIFE	80	1000		54	0		
PROM	82S23	TTL	256	FUSE	FUSE	DNTLIFE	84	1000		49	0		
PROM	82S23	TTL	256	FUSE	FUSE	DNTLIFE	86	1000		100	0		
PROM	82S23A	TTL	256	FUSE	FUSE	DNTLIFE	85	1000		99	0		
PROM	82S126A	TTL	2K	FUSE	FUSE	DNTLIFE	85	1000		99	0		
PROM	82S126A	TTL	2K	FUSE	FUSE	DNTLIFE	86	1000		90	0		
PROM	82S129	TTL	2K	FUSE	FUSE	DNTLIFE	86	1000		100	0		
PROM	82S129A	TTL	2K	FUSE	FUSE	DNTLIFE	86	1000		95	0		
PROM	82S129A	TTL	2K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S129A	TTL	2K	FUSE	FUSE	HTOLIFE	88	1000		97	1	1 ACFUNC SLOPATT	?
PROM	82S130	TTL	2K	FUSE	FUSE	DNTLIFE	81	1000		40	0		
PROM	82S130A	TTL	2K	FUSE	FUSE	HTOLIFE	87	1000		100	0		
PROM	82S131	TTL	2K	FUSE	FUSE	DNTLIFE	80	1000		50	0		
PROM	82S131	TTL	2K	FUSE	FUSE	DNTLIFE	81	1000		60	0		
PROM	82S131	TTL	2K	FUSE	FUSE	DNTLIFE	81	1000		69	0		
PROM	82S131	TTL	2K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S131	TTL	2K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S131A	TTL	2K	FUSE	FUSE	DNTLIFE	85	1000		90	0		
PROM	82HS321	TTL	32K	FUSE	FUSE	DNTLIFE	85	1000		100	1	1 FUNC FAIL	1 METAL DEFECT
PROM	82HS321	TTL	32K	FUSE	FUSE	DNTLIFE	85	1000		99	1	1 FUNC FAIL	1 DEF ZENER
PROM	82HS321	TTL	32K	FUSE	FUSE	HTOLIFE	87	1000		90	0		
PROM	82HS3218	TTL	32K	FUSE	FUSE	HTOLIFE	87	1000		100	0		
PROM	82S321	TTL	32K	FUSE	FUSE	DNTLIFE	85	1000		88	1	1 AC FUNC	?
PROM	82HS147A	TTL	4K	FUSE	FUSE	HTOLIFE	88	1000		176	0		
PROM	82S137	TTL	4K	FUSE	FUSE	DNTLIFE	81	1000		45	0		
PROM	82S137	TTL	4K	FUSE	FUSE	DNTLIFE	81	1000		52	0		
PROM	82S137	TTL	4K	FUSE	FUSE	DNTLIFE	81	1000		52	1	1 FUNC FAIL	1 EOS
PROM	82S137	TTL	4K	FUSE	FUSE	DNTLIFE	84	1000		100	1	1 LEAKAGE FAIL	1 JUNC DAMAGE

TYPE	PARTNUM	TECH	BITS	ARRAYTECH		TEST	TR	DUR	DEVHRS	NTEST	NFAIL	FDESC	FMECHNSM
PROM	82S137	TTL	4K	FUSE	FUSE	ONTLIFE	86	1000		100	0		
PROM	82S137	TTL	4K	FUSE	FUSE	ONTLIFE	86	1000		99	0		
PROM	82S137	TTL	4K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S137	TTL	4K	FUSE	FUSE	HTOLIFE	88	1000		100	1	1 AC PARAM SLO PATT	?
PROM	82S137A	TTL	4K	FUSE	FUSE	ONTLIFE	83	1000		50	0		
PROM	82S137A	TTL	4K	FUSE	FUSE	ONTLIFE	83	1000		50	0		
PROM	82S137A	TTL	4K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S137A	TTL	4K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S137A	TTL	4K	FUSE	FUSE	HTOLIFE	88	1000		100	2	2 ACFUNC SLOPATT	?
PROM	82S147A	TTL	4K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
PROM	82S147A	TTL	4K	FUSE	FUSE	HTOLIFE	88	1000		94	0		
PROM	82S147A	TTL	4K	FUSE	FUSE	HTOLIFE	88	1000		99	0		
PROM	82LS181	TTL	8K	FUSE	FUSE	ONTLIFE	80	1000		50	0		
PROM	82LS181	TTL	8K	FUSE	FUSE	ONTLIFE	80	1000		50	1	1 FUNC FAIL	?
PROM	82S181	TTL	8K	FUSE	FUSE	ONTLIFE	83	1000		45	0		
PROM	82S181	TTL	8K	FUSE	FUSE	ONTLIFE	84	1000		49	2	1 INTERMIT BIT, 1 UNK	?, 1 ELECTROMIG
PROM	82S181A	TTL	8K	FUSE	FUSE	ONTLIFE	84	1000		50	0		
PROM	82S181A	TTL	8K	FUSE	FUSE	ONTLIFE	86	1000		90	1	1 AC FUNC (BAKE RECOV)	?
PROM	82S181C	TTL	8K	FUSE	FUSE	HTOLIFE	87	1000		89	0		
PROM	82S181C	TTL	8K	FUSE	FUSE	HTOLIFE	88	1000		120	0		
PROM	82S183	TTL	8K	FUSE	FUSE	ONTLIFE	84	1000		95	0		
PROM	82S183	TTL	8K	FUSE	FUSE	ONTLIFE	84	1000		96	1	1 FAILS AC	?
PROM	82S185	TTL	8K	FUSE	FUSE	ONTLIFE	81	1000		50	0		
PROM	82S185	TTL	8K	FUSE	FUSE	ONTLIFE	84	1000		50	0		
PROM	82S185A	TTL	8K	FUSE	FUSE	ONTLIFE	83	1000		50	0		
PROM	82S185A	TTL	8K	FUSE	FUSE	HTOLIFE	87	1000		83	0		
PROM	82S185A	TTL	8K	FUSE	FUSE	HTOLIFE	88	1000		100	0		
ROM	2643A	NMOS		NMOS	NMOS	OPTLIFE	83	1000		100	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		100	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		100	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		100	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		100	1	1 IN LEAK FAIL	1 THR VOLT SHIFT
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		102	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		98	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		98	1	1 FUNC FAIL	1 THR VOLT SHIFT
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		99	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		99	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	85	1000		100	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	85	1000		99	1	1 FUNC FAIL	1 OXIDE DEFECT
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	86	1000		100	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	86	1000		100	0		
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	86	1000		100	1	1 VCCSUB SHORT	1 JUNC LEAK MONION
ROM	23128	NMOS	128K	NMOS	NMOS	ONTLIFE	86	1000		101	0		
ROM	23128A	NMOS	128K	NMOS	NMOS	ONTLIFE	84	1000		100	0		
ROM	23128A	NMOS	128K	NMOS	NMOS	ONTLIFE	85	1000		100	0		
ROM	23128A	NMOS	128K	NMOS	NMOS	ONTLIFE	86	1000		100	0		
ROM	23128A	NMOS	128K	NMOS	NMOS	ONTLIFE	86	1000		100	0		
ROM	2616	NMOS	16K	NMOS	NMOS	ONTLIFE	82	1000		111	0		
ROM	2616	NMOS	16K	NMOS	NMOS	ONTLIFE	80	1000		100	0		

TYPE	PARTNUM	TECH	NBITS	ARRAYTECH		TEST	YR	QUR	DEVHRS	NTEST	NFAIL	FDESC	FMECHNSM
ROM	23256	NMOS	256K	NMOS	NMOS	DNTLIFE	86	1000		100	0		
ROM	23256	NMOS	256K	NMOS	NMOS	DNTLIFE	86	1000		100	0		
ROM	23256	NMOS	256K	NMOS	NMOS	DNTLIFE	86	1000		90	1	1 FAIL	1 IONIC LEAKAGE
ROM	23256	NMOS	256K	NMOS	NMOS	DNTLIFE	86	1000		98	0		
ROM	23256	NMOS	256K	NMOS	NMOS	DNTLIFE	86	1000		99	0		
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	84	1000		100	0		
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	84	1000		100	0		
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	84	1000		100	0		
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	84	1000		99	0		
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	84	1000		99	0		
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	85	1000		100	0		
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	85	1000		98	0		
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	85	1000		99	1	1 FUNC FAIL	1 ELECTRONIC
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	86	1000		100	0		
ROM	23256A	NMOS	256K	NMOS	NMOS	DNTLIFE	86	1000		100	0		
ROM	2332	NMOS	32K	NMOS	NMOS	DNTLIFE	84	1000		100	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	80	1000		100	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	80	1000		104	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	80	1000		83	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	80	1000		99	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	81	1000		102	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	81	1000		102	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	81	1000		105	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	81	1000		119	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	81	1000		90	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	82	1000		101	0		
ROM	2632	NMOS	32K	NMOS	NMOS	DNTLIFE	82	1000		103	0		
ROM	2632A	NMOS	32K	NMOS	NMOS	DNTLIFE	83	1000		101	0		
ROM	2632A	NMOS	32K	NMOS	NMOS	DNTLIFE	83	1000		100	0		
ROM	2632A	NMOS	32K	NMOS	NMOS	DNTLIFE	83	1000		100	0		
ROM	2632A	NMOS	32K	NMOS	NMOS	DNTLIFE	83	1000		100	0		
ROM	2632A	NMOS	32K	NMOS	NMOS	DNTLIFE	83	1000		100	0		
ROM	2632A	NMOS	32K	NMOS	NMOS	DNTLIFE	83	1000		100	0		
ROM	26M32	NMOS	32K	NMOS	NMOS	DNTLIFE	82	1000		100	0		
ROM	26M32	NMOS	32K	NMOS	NMOS	DNTLIFE	82	1000		106	0		
ROM	2364	NMOS	64K	NMOS	NMOS	DNTLIFE	85	1000		100	0		
ROM	2364	NMOS	64K	NMOS	NMOS	DNTLIFE	85	1000		200	0		
ROM	2364	NMOS	64K	NMOS	NMOS	DNTLIFE	86	1000		100	0		
ROM	2364	NMOS	64K	NMOS	NMOS	DNTLIFE	86	1000		100	0		
ROM	2364	NMOS	64K	NMOS	NMOS	DNTLIFE	86	1000		100	0		
ROM	2364	NMOS	64K	NMOS	NMOS	DNTLIFE	86	1000		109	0		
ROM	2364	NMOS	64K	NMOS	NMOS	HTOL	87	1000		100	0		
ROM	2364	NMOS	64K	NMOS	NMOS	HTOL	87	1000		100	0		
ROM	2664	NMOS	64K	NMOS	NMOS	DNTLIFE	80	1000		100	0		
ROM	2664	NMOS	64K	NMOS	NMOS	DNTLIFE	80	1000		100	0		
ROM	2664	NMOS	64K	NMOS	NMOS	DNTLIFE	80	1000		80	0		
ROM	2664	NMOS	64K	NMOS	NMOS	DNTLIFE	81	1000		100	0		
ROM	2664	NMOS	64K	NMOS	NMOS	DNTLIFE	81	1000		105	0		
ROM	2664	NMOS	64K	NMOS	NMOS	DNTLIFE	81	1000		105	1	1 PARAM	1 CONTAM?

TYPE	PARTNUM	TECH	NBITS	ARRAYTECH		TEST	YR	DUR	DEVHRS	NTEST	NFAIL	FDESC	FMECHNSM
ROM	2664	NMOS	64K	NMOS	NMOS	DHTLIFE	81	1000		122	0		
ROM	2664	NMOS	64K	NMOS	NMOS	DHTLIFE	81	1000		84	1	1 OUTLEAK	?
ROM	2664	NMOS	64K	NMOS	NMOS	DHTLIFE	82	1000		106	0		
ROM	2664	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		100	0		
ROM	2664	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		99	0		
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		100	0		
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		100	0		
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		100	0		
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		100	0		
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		100	2	2 IN LEAK FAIL	?
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		63	0		
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		99	0		
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	83	1000		99	0		
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	84	1000		45	0		
ROM	2664A	NMOS	64K	NMOS	NMOS	DHTLIFE	84	1000		90	0		
UVEPROM	27C256					DHTLIFE	86	1000		100	0		
UVEPROM	27C256					DHTLIFE	86	1000		199	0		
UVEPROM	27C256					DHTLIFE	86	1000		50	0		
UVEPROM	27C256					DHTLIFE	86	1000		50	0		
UVEPROM	27C256					DHTLIFE	86	500		100	0		
UVEPROM	27C256					DHTLIFE	86	500		100	0		
UVEPROM	27C256					DHTLIFE	86	500		100	0		
UVEPROM	27C256					DHTLIFE	86	500		47	0		
UVEPROM	27C256					DHTLIFE	86	500		99	0		
UVEPROM	27C256					HTOLIFE	87	1000		100	0		
UVEPROM	27C256					HTOLIFE	87	1000		48	1	1 PARAM FAIL	1 OXIDE DEFECT
UVEPROM	27C256					HTOLIFE	87	1000		50	0		
UVEPROM	27C256					HTOLIFE	87	1000		50	0		
UVEPROM	27C256					HTOLIFE	87	1000		50	0		
UVEPROM	27C256					HTOLIFE	87	1000		90	0		
UVEPROM	27C256					HTOLIFE	87	1000		90	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		100	0		
UVEPROM	27C256					HTOLIFE	88	1000		50	0		
UVEPROM	27C256					HTOLIFE	88	1000		75	1	1 BIT FAIL	1 CHARGE LOSS
UVEPROM	27C256					HTOLIFE	88	1000		80	0		

TYPE	PARTNUM	TECH	MBITS	ARRAYTECH	TEST	YR	DUR	DEVHRS	NTEST	NFAIL	FDESC	FMECHNSM
UVEPROM	27C256				HTOLIFE	88	1000		90	0		
UVEPROM	27C256				HTOLIFE	88	1000		99	0		
UVEPROM	27C256				HTOLIFE	88	1000		99	0		
UVEPROM	27C64				OHTLIFE	85	1000		25	0		
UVEPROM	27C64				OHTLIFE	85	1000		54	0		
UVEPROM	27C64				OHTLIFE	85	1000		55	1	1 SINGLE BIT	1 JUNC LEAKAGE
UVEPROM	27C64				OHTLIFE	85	1000		89	0		
UVEPROM	27C64				OHTLIFE	86	1000		100	0		
UVEPROM	27C64				OHTLIFE	86	1000		106	0		
UVEPROM	27C64				OHTLIFE	86	1000		54	0		
UVEPROM	27C64				OHTLIFE	86	1000		54	0		
UVEPROM	27C64				OHTLIFE	86	1000		55	0		
UVEPROM	27C64				OHTLIFE	86	1000		55	0		
UVEPROM	27C64				OHTLIFE	86	1000		55	0		
UVEPROM	27C64				OHTLIFE	86	1000		55	0		
UVEPROM	27C64				OHTLIFE	86	1000		55	0		
UVEPROM	27C64				OHTLIFE	86	1000		55	0		
UVEPROM	27C64				OHTLIFE	86	1000		55	0		
UVEPROM	27C64				OHTLIFE	86	1000		55	0		
UVEPROM	27C64				OHTLIFE	86	1000		55	0		
UVEPROM	27C64				OHTLIFE	86	1000		94	0		
UVEPROM	27C64				OHTLIFE	86	1000		99	0		
UVEPROM	27C64				OHTLIFE	86	1000		99	0		
UVEPROM	27C64				OHTLIFE	86	500		99	0		
UVEPROM	27C64				HTOLIFE	87	1000		100	0		
UVEPROM	27C64				HTOLIFE	87	1000		100	0		
UVEPROM	27C64				HTOLIFE	87	1000		100	0		
UVEPROM	27C64				HTOLIFE	87	1000		48	0		
UVEPROM	27C64				HTOLIFE	87	1000		50	0		
UVEPROM	27C64				HTOLIFE	88	1000		100	0		
UVEPROM	27C64				HTOLIFE	88	1000		100	0		
UVEPROM	27C64A				OHTLIFE	86	500		50	0		
UVEPROM	27C64A				OHTLIFE	86	500		96	0		
UVEPROM	27C64A				OHTLIFE	86	500		98	0		
UVEPROM	27C64A				OHTLIFE	86	500		99	0		
UVEPROM	27C64A				HTOLIFE	87	1000		100	0		
UVEPROM	27C64A				HTOLIFE	87	1000		100	1	1 BIT FAIL	1 CHARGE LOSS
UVEPROM	27C64A				HTOLIFE	87	1000		50	0		
UVEPROM	27C64A				HTOLIFE	87	1000		96	0		
UVEPROM	27C64A				HTOLIFE	88	1000		100	0		
UVEPROM	27C64A				HTOLIFE	88	1000		100	0		
UVEPROM	27C64A				HTOLIFE	88	1000		100	0		
UVEPROM	27C64A				HTOLIFE	88	1000		100	0		
UVEPROM	27C64A				HTOLIFE	88	1000		100	0		
UVEPROM	27C64A				HTOLIFE	88	1000		100	0		
UVEPROM	27C64A				HTOLIFE	88	1000		100	0		
UVEPROM	27C64A				HTOLIFE	88	1000		80	0		

TYPE	PARTNUM	TECH	MBITS	ARRAYTECH		TEST	YR	DUR	DEVHRS	NTEST	NFAIL	FDESC	FMECHNSM
UVEPROM	27C64A					HTOLIFE	88	1000		84	0		
UVEPROM	27C64A					HTOLIFE	88	1000		97	0		
UVEPROM	27C64A					HTOLIFE	88	1000		99	0		
UVEPROM	27HC641					DHTLIFE	86	1000		967	1	1 UNK	1 FAB DEFECT
UVEPROM	27HC641					DHTLIFE	86	1000		99	1	1 UNK	1 FAB DEFECT
UVEPROM	27HC641					DHTLIFE	86	500		49	0		
UVEPROM	27HC641					DHTLIFE	86	500		50	0		
UVEPROM	27HC641					HTOLIFE	88	1000		106	0		
UVEPROM	27HC641					HTOLIFE	88	1000		96	0		
UVEPROM	27HC641					HTOLIFE	88	1000		97	0		
UVEPROM	27HC641					HTOLIFE	88	1000		99	0		
UVEPROM	21C12B	CMOS	128K	FLGATE 12.5V	FLGA	125DLIFE	87		4.9E5		1	1 SBIT CHRGE LOSS	1 OXIDE BRKDWN
UVEPROM	27C256	CMOS	256K	FLGATE 12.5V	FLGA	125DLIFE	87		4.51E6		5	1 GRSSFUNC, 2 SBIT CHRGELOSS, 1 OUTLEAK, 1 MBIT CHRGEGAIN	1 OPEN CONTACT, ?, 1 OXIDE BRKDWN, ?
UVEPROM	27C256	CMOS	256K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		4.05E5		0		
UVEPROM	87C257	CMOS	256K	FLGATE 12.5V	FLGA	125DLIFE	87		7.9E5		1	1 ICC STBY PWR	?
UVEPROM	27C64	CMOS	64K	FLGATE 12.5V	FLGA	125DLIFE	84		1.36E6		2	1 SBIT CHRGE GAIN, 1 ROW FAILURE	?,?
UVEPROM	27C64	CMOS	64K	FLGATE 12.5V	FLGA	125DLIFE	87		4.25E6		5	1 MBCHRGELOSS, 1 GRSSFUNC, 3 SBIT CHRGE LOSS	?, ?, 1 PASS HOLE
UVEPROM	27C64	CMOS	64K	FLGATE 12.5V	FLGA	6.5VDLIFE	84		9.63E6		4	2 CHRGE GAIN, 1 CHRGE LOSS, 1 OUTPUT FAIL	?,?,?
UVEPROM	27C64	CMOS	64K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		4.06E5		0		
UVEPROM	P/N2764	CMOS	64K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		2.84E5		0		
UVEPROM	P/N27C64	CMOS	64K	FLGATE 12.5V	FLGA	125DLIFE	87		2.22E6		2	2 SBCL	1 OXIDE BRKDWN
UVEPROM	27128	NMOS	128K	FLGATE 21V	FLGA	125DLIFE	83		8.23E6		31	14 INP LKGE, 8 CHRGE GAIN, 2 FUSE LKGE, 1 DECOD, 3 CGLOSS, 2 INLEV, 1FUSERG	14 CONTAM, 8 CONTAM,?,?, 1 CONTAM,?,?
UVEPROM	27128A	NMOS	128K	FLGATE 12.5V	FLGA	125DLIFE	84		1.28E6		0		
UVEPROM	27128A	NMOS	128K	FLGATE 12.5V	FLGA	125DLIFE	87		2.17E6		4	2 MBIT CHRGE LOSS, 2 UNK	?, 2 CONTAM
UVEPROM	27128A	NMOS	128K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		5.0E4		0		
UVEPROM	27128B	NMOS	128K	FLGATE 12.5V	FLGA	125DLIFE	87		1.22E6		4	4 MBIT CHRGE GAIN	4 CONTAM
UVEPROM	27128B	NMOS	128K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		1.18E5		1	1 UNK	1 OXIDE DEFECT
UVEPROM	27010	NMOS	1M	FLGATE 12.5V	FLGA	125DLIFE	87		9.04E5		3	1 ROWFAIL, 1 SPEED, 1 UNK	?, ?, 1 PASSDEFECT
UVEPROM	27010	NMOS	1M	FLGATE 12.5V	FLGA	6.5VDLIFE	87		7.74E4		0		

TYPE	PARTNUM	TECH	MBITS	ARRAYTECH		TEST	YR	DUR	DEVHRS	NTEST	NFAIL	FDESC	FMECHNSM
UVEPROM	27210	NMOS	1M	FLGATE 12.5V	FLGA	125DLIFE	87		9.48E5		3	2 SBCL, 1 SBCL	?, ?
UVEPROM	27210	NMOS	1M	FLGATE 12.5V	FLGA	6.5VDLIFE	87		1.73E5		0		
UVEPROM	27256	NMOS	256K	FLGATE 12.5V	FLGA	125DLIFE	84		3.36E6		20	3 INP LKGE, 15 CHRGE GAIN, 1 OPEN VCC, 1 CHARGE LOSS	?, 15 CONTAM, ?, 1 CONTAM
UVEPROM	27256	NMOS	256K	FLGATE 12.5V	FLGA	6.5VDLIFE	84		1.73E5		1	1 CHRGE LOSS	?
UVEPROM	2732A	NMOS	32K	FLGATE 21V	FLGA	125DLIFE	84		4.38E6		7	2 INPUT LEVEL, 1 GROSS FUNC, 2 LEAKAGE, 1 OUTPUT FAIL, 1 INP LEAKAGE	?,?,?,?,?
UVEPROM	2732A	NMOS	32K	FLGATE 21V	FLGA	125DLIFE	86		6.84E6		19	1 SBIT CHRGE LOSS, 13 FAIL, 3 DECODE	?, 13 CONTAM, ?
UVEPROM	2732A	NMOS	32K	FLGATE 21V	FLGA	6.5VDLIFE	86		1.44E6		0		
UVEPROM	27512	NMOS	512K	FLGATE 12.5V	FLGA	125DLIFE	85		4.21E5		2	1 COL FAIL, 1 MB CHRGE GAIN	?, 1 CONTAM
UVEPROM	27512	NMOS	512K	FLGATE 12.5V	FLGA	125DLIFE	87		9.23E6		44	9 MBCL, 19 SBCL, 8 UNK, 8 SBCG	?, ?, 2CONTAM 3OXDEFECT 2DEFECT, ?
UVEPROM	27512	NMOS	512K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		7.67E4		1	1 SBIT CHARGE LOSS	?
UVEPROM	27512XX	NMOS	512K	FLGATE 12.5V	FLGA	125DLIFE	87		3.27E6		16	4 SBCL, 2 SBCG, 9MBCL, 1 GROSSFUNC	?, ?, 9PASSDEFECT, ?
UVEPROM	27512XX	NMOS	512K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		3.10E5		4	1 UNK, 3 SBCL	1 OXIDEBRKDN, ?
UVEPROM	Z764A	NMOS	64K	FLGATE 12.5V	FLGA	125DLIFE	84		5.89E6		21	3 SB CHARGE LOSS, 1 VCC CNTCT SHRT, 14 CHRGE LOSS, 2 SNSE AMP, 1 DECODER	
UVEPROM	Z764A	NMOS	64K	FLGATE 12.5V	FLGA	125DLIFE	87		7.94E6		12	1 FAIL, 3 SBCL, 3 SBCG, 3 UNK, 2 SPEED	1 OXIDE DEFECT, ?, ?, 1 CRACKPASS 2CONTAM, 2 CONTAM
UVEPROM	Z764A	NMOS	64K	FLGATE 12.5V	FLGA	6.5VDLIFE	87		7.2E4		0		

TYPE	PARTNUM	TECH	NBITS	ARRAYTECH	TEST	YR	TSTDURA	NTEST	NFAIL	FAILDESCR	FAILMECNSM
SRAM	IMS1400	MOS	16K	MOS	125OPLIFE	84	2000	362 3S	3	1 GRSFUNC, 1 WEAK MULTI COL, 1 FULL ADJ COL	?,?,?
SRAM	IMS1400	MOS	16K	MOS	125OPLIFE	84	2000	369 3S	11	3 DEAD ARRAY, 2 FULL ADJ COL, 2 SING BIT, 1 STUK ADRS, 3 GROSS FUNC	?,?,1 xstr leakage,?,?
SRAM	IMS1400	MOS	16K	MOS	125OPLIFE	84	2000	389 3S	10	5 SINGLE BIT, 5 DEAD ARRAY	2 xstr leakage, ?
SRAM	IMS1400	MOS	16K	MOS	125OPLIFE	84	2000	387 3S	4	1 SINGLE BIT, 3 UNK	1 xstr leakage, ?
SRAM	IMS1400	MOS	16K	MOS	125OPLIFE	84	2000	538 5S	6	3 SINGLE BIT, 1 CLUSTER BITS, 2 DEAD ARRAY	?,?,?
SRAM	IMS1400	MOS	16k	MOS	125OPLIFE	84	2000	351 3S	6	2 DEAD ARRAY, 1 PART COL, 1 PINHOLE, 2 UNK	?,?,?,?
SRAM	IMS1400	MOS	16k	MOS	125OPLIFE	84	2000	392 3S	0		
SRAM	IMS1420	MOS	16K	MOS	125OPLIFE	84	2000	380 3S	9	1 CLUSTER BITS, 2 SING BIT, 2 STK ADR, 1 ARRAY, 1 PART COL, 1 IN THR, 1 UNK	?, 1 xstr leakage, ?,?,?,?,?,?,
SRAM	IMS1420	MOS	16K	MOS	125OPLIFE	84	2000	521 5S	1	1 WEAK MULTIBIT	?
SRAM	IMS1420	MOS	16K	MOS	125OPLIFE	84	2000	753 7S	12	4 DEAD ARRAY, 4 SINGLE BIT, 4 UNK	?, 1 xstr leakage, ?
SRAM	IMS1420	MOS	16K	MOS	125OPLIFE	84	2000	308 3S	5	5 UNK	?
SRAM	IMS1420	MOS	16K	MOS	125OPLIFE	84	2000	524 5S	3	1 DEAD ARRAY, 2 UNK	?,?
SRAM	IMS1420	MOS	16K	MOS	125OPLIFE	84	2000	575 5S	7	1 SING BIT, 1 CLUSTER BITS, 4 UNK, 1 IN THRESH	?,?,?,?
SRAM	IMS1420	MOS	16K	MOS	125OPLIFE	84	1000	725 7S	3	1 DEAD ARRAY, 2 UNK	?,?
DRAM	IMS2600	MOS	64K	MOS	125OPLIFE	84	2000	105 1D	0		
DRAM	IMS2600	MOS	64K	MOS	125OPLIFE	84	2000	210 2D	0		
DRAM	IMS2600	MOS	64K	MOS	125OPLIFE	84	2000	147 1D	2	2 FULL COLUMN	?
DRAM	IMS2600	MOS	64K	MOS	125OPLIFE	84	2000	393 3D	0		
DRAM	IMS2600	MOS	64K	MOS	125OPLIFE	84	2000	348 3D	1	1 FULL COLUMN	?
DRAM	IMS2600	MOS	64K	MOS	125OPLIFE	84	2000	247 2D	1	1 FULL COLUMN	?
DRAM	IMS2600	MOS	64K	MOS	125OPLIFE	84	2000	366 3D	1	1 FULL COLUMN	?
DRAM	IMS2620	MOS	64K	MOS	125OPLIFE	84	2000	189 1D	1	1 GROSS FUNC	?
DRAM	IMS2620	MOS	64K	MOS	125OPLIFE	84	2000	356 3D	2	2 GROSS FUNC	?
DRAM	IMS2620	MOS	64K	MOS	125OPLIFE	84	1000	387 3D	2	2 GROSS FUNC	?
RAM	82S09	TTL	576	TTL	D/SNTLIFE	80	1000	50 5R	0		
RAM	74S189	TTL	64	TTL	D/SNTLIFE	80	1000	54 5R	0		
RAM	82S25	TTL	64	TTL	D/SNTLIFE	81	1000	44 4R	1	1 GROSS FUNC	1 BAD WIREBOND
RAM	82S16	TTL	256	TTL	D/SNTLIFE	81	1000	47 4R	0		
RAM	82S16	TTL	256	TTL	D/SNTLIFE	81	1000	52 5R	0		
RAM	82S09	TTL	576	TTL	D/SNTLIFE	81	1000	50 5R	0		
RAM	82S09	TTL	576	TTL	D/SNTLIFE	81	1000	51 5R	0		
RAM	82S16	TTL	256	TTL	D/SNTLIFE	81	1000	51 5R	0		
RAM	82S09	TTL	576	TTL	D/SNTLIFE	82	1000	52 5R	0		
RAM	82S09	TTL	576	TTL	D/SNTLIFE	83	1000	52 5R	0		

TYPE	PARTNUM	TECH	NBITS	ARRAYTECH	TEST	YR	TSTDURA	NTEST	NFAIL	FAILDESCR	FAILMECHSM
RAM	82S212	TTL	2K	TTL	D/SNTLIFE	83	1000	50 5R	2	2 AC FUNCTIONAL	?
RAM	82S09	TTL	576	TTL	D/SNTLIFE	83	1000	50 5R	0		
RAM	82S09	TTL	576	TTL	D/SNTLIFE	83	1000	50 5R	0		
RAM	74S189	TTL	64	TTL	D/SNTLIFE	83	1000	50 5R	0		
???	10155	ECL	??	ECL	SNTLIFE	79	1000	52 5?	0		
???	10155	ECL	??	ECL	SNTLIFE	81	1000	40 4?	0		
RAM	82S16	TTL	256	TTL	D/SNTLIFE	84	1000	50 5R	0		
RAM	3101A	TTL	??	TTL	D/SNTLIFE	84	1000	45 4R	0		
RAM	74S189	TTL	64	TTL	D/SNTLIFE	84	1000	49 4R	1	1 AC FUNC	?
RAM	82S09	TTL	576	TTL	D/SNTLIFE	84	1000	48 4R	0		
RAM	82S16	TTL	256	TTL	D/SNTLIFE	84	1000	50 5R	0		
RAM	3101A	TTL	??	TTL	D/SNTLIFE	84	1000	45 4R	0		
RAM	74S189	TTL	64	TTL	D/SNTLIFE	84	1000	49 4R	2	2 AC FUNC	?
RAM	74S189	TTL	64	TTL	D/SNTLIFE	84	1000	49 4R	0		
RAM	3101A	TTL	??	TTL	D/SNTLIFE	84	1000	81 8R	0		
RAM	3101A	TTL	??	TTL	D/SNTLIFE	84	1000	100 1R	0		
RAM	82S25	TTL	64	TTL	D/SNTLIFE	84	1000	50 5R	0		
RAM	82S09	TTL	576	TTL	D/SNTLIFE	84	1000	48 4R	0		
RAM	82LS16	TTL	256	TTL	D/SNTLIFE	84	1000	94 9R	0		
RAM	3101A	TTL	??	TTL	D/SNTLIFE	84	1000	45 4R	0		
RAM	82LS16	TTL	256	TTL	D/SNTLIFE	84	1000	96 9R	2	2 AC PARAM	?
RAM	82S25	TTL	64	TTL	D/SNTLIFE	84	1000	49 4R	0		
RAM	74S189	TTL	64	TTL	D/SNTLIFE	84	1000	94 9R	0		
RAM	82S212A	TTL	2K	TTL	D/SNTLIFE	85	1000	64 6R	0		
RAM	82S09	TTL	576	TTL	D/SNTLIFE	85	1000	100 1R	0		
RAM	82S212A	TTL	2K	TTL	D/SNTLIFE	85	1000	64 6R	0		
RAM	82S212A	TTL	2K	TTL	D/SNTLIFE	85	1000	64 6R	0		
RAM	3101	TTL	??	TTL	D/SNTLIFE	85	1000	95 9R	1	1 AC FUNC	?
RAM	3101A	TTL	??	TTL	D/SNTLIFE	85	1000	89 8R	1	1 AC PARAM	?
RAM	3101A	TTL	??	TTL	D/SNTLIFE	85	1000	100 1R	1	1 FUNC	OXIDE PINHOLES
RAM	3101A	TTL	??	TTL	D/SNTLIFE	86	1000	100 1R	0		
RAM	82S09	TTL	576	TTL	D/SNTLIFE	86	1000	99 9R	0		
RAM	82S212	TTL	2K	TTL	D/SNTLIFE	86	1000	64 6R	0		
RAM	74S189	TTL	64	TTL	D/SNTLIFE	86	1000	99 9R	1	1 AC SLOW PATT	?
RAM	74S189	TTL	64	TTL	D/SNTLIFE	86	1000	99 9R	1	1 AC FUNC	?
RAM	74S189	TTL	64	TTL	D/SNTLIFE	86	1000	100 1R	2	2 FUNC	2 METAL DEFECT
RAM	74S189	TTL	64	TTL	D/SNTLIFE	86	1000	150 1R	0		
RAM	82S16	TTL	256	TTL	D/SNTLIFE	86	1000	98 9R	0		
RAM	74S189	TTL	256	TTL	D/SNTLIFE	87	1000	100 1R	0		
RAM	82S212	TTL	2K	TTL	D/SNTLIFE	87	1000	176 1R	0		
RAM	82S09A	TTL	576	TTL	D/SNTLIFE	88	1000	100 1R	0		
RAM	74S189	TTL	64	TTL	D/SNTLIFE	88	1000	100 1R	0		

APPENDIX F

WIRE AND WIRE BOND FAILURES IN MICROELECTRONIC PACKAGES

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F1. INTRODUCTION

Wire bonding is a process which is accomplished by bringing two conductors to be joined into intimate contact such that the atoms of the materials diffuse together. The materials used for wires include silver, copper, aluminum and palladium. The materials used for pads are aluminum, gold, silver, nickel, copper and chromium. The wires serve to connect the small pads on the die to the external package leads (figure F-1).

Large compressive stresses along with ultrasonic vibrations or thermal energy are applied at the wire-pad interface during the bonding process. Cracks in the bond pad or in the substrate may result if the bonding stress is exceedingly high.[1] Cracks are difficult to detect visually unless the bond is detached and must prevented before such parts are utilized in electronic equipment. Proper control of the bonding parameters usually assures reliable wire bonds. When bonding is achieved by a wire from the package lead to the cavity metallization, it is known as a substrate bond.[3] When one lead is connected to another without going through the substrate metallization, it is called a control bond. Both destructive and non-destructive tests are used to ensure good performance. The first is the destructive Bond pull test. The purpose of this test is to measure the bond strengths, evaluate the bond strength distribution or to determine compliance with specified bond strength. In this test an external force is applied to the bond until failure occurs. If the bonding parameters are discrepant the bond would fail below the specified value as a result of the bond pull test. The location of the failure is an important clue for the initiation of the corrective action to prevent failure recurrence. The failure could be a wire break at the neckdown point due to a reduction of the cross-sectional area as a result of the bonding process. The failure could also be a break at a wire defect site other than the neckdown region, a failure at the interface between wire and metallization at the substrate or the package post, an interface failure between the pad metallization and the substrate, fracture of the die beneath the bond pad, or fracture of the substrate.

Another test is the non-destructive bond pull test. The purpose of this

method is to reveal unacceptable wire bonds. This procedure is usable for bonds made by either ultrasonic or thermal compression techniques. Any bond pull which results in separation of the bonds at the bond interface or breakage of the wire or interconnect anywhere along the entire length including the bond heels, at an applied force less than the specified force for the applicable material and wire diameter, constitutes a failure. The magnitude of the non-destructive pull force is around 80% of the minimum bond strength for the particular material unless otherwise specified.

A variation of the destructive or non-destructive bond pull test is the bond pull after bake test. In this test the devices are baked at a high temperature and then subjected to the bond pull test. The exposure to temperature accelerates crack propagation if microcracks in the die or substrate already exist.

A common destructive test is the "etch back analysis" test, whereby an aqua-regia solution is used to etch away the ball and metallization, exposing the underlying layers of the bond pad. Any cracks on the oxides or substrate are revealed by such a test.

Wire bond failures are a result of shear of the bond pad and the wire, flexure of the wire, excessive intermetallics, manufacturing parameters, galvanic corrosion and chip outs in Si/SiO_2. Plastic encapsulated packages also fail as result of stresses resulting from the differential expansion of the epoxy encapsulation and the wire if a low modulus buffer coating is not placed between the encapsulant and the wire.

MIL-HDBK-217E was developed by the Department of Defense in order to standardize the methods employed for reliability prediction procedures. The handbook provides uniform methods for predicting the reliability of military electronic equipment and systems and estabilishes a common basis for compering and evaluating reliability predictions of designs.

The "Part Stress Analysis" prediction method of MIL-HDBK-217E is applicable during the later design phase where actual hardware and circuits have been

designed. The part operating failure rate model λ_p is based on the following equation

$$\lambda_p = \pi_Q (C_1 \pi_T + C_2 \pi_E) \pi_L$$

where C_1 is the circuit complexity factor, C_2 is the package complexity factor and the π terms account for the influences of environment, application, complexity, quality, production maturity of the process and relative stress level.

MIL-HDBK-217E does not explicitly discuss how wire bond failure contributes to the device failure rate. The package related term (C_2) of the model depends only on the number of operational terminal pins in the microelectronic device. This term is not affected by any other factors such as temperature change or the rate of temperature change, manufacturing process, fatigue or thermal cycling differential expansion between the wire and the pad; but these factors have been found to affect the wire bond failures. This report presents an alternative to the MIL-HDBK-217E model. A statistical deterministic approach to failure modeling has been used for reliability prediction. This can then be used for design of microelectronic packages.

F2. THE WIRE BOND

F2.1. The Wire.

Wire is usually made of gold or aluminum. The wire bonding process may be thermocompression or ultrasonic. The thermocompression process typically uses a gold wire while the aluminum wire is utilized in the ultrasonic process. Gold tends to age in the amorphous state with a consequential decrease in tensile strength. The hard drawn gold wire ages significantly at room temperature so the softer and relatively more stable stress-relieved wire is recommended. Pure aluminum cannot be hardened sufficiently to allow it to be drawn to a diameter of 1 mil. Therefore aluminum is usually hardened by adding about 1% of an alloying element such as silicon or, less frequently, magnesium.

F2.2. Wire Materials.

Wire materials include gold, copper, aluminum and palladium, with gold and aluminum being the more commonly used. The characteristics of the wire materials are of vital importance to the strength of the wire bond. These include wire dimensions, tensile strength, elongation and contamination.

It is important to have a wire of constant dimensions and known cross-sectional area because the bonding process conditions depend on the mass of the wire involved in making the bond. The tensile strength is an important specification both for ultrasonic as well as for thermocompression bonds. A bond wire is attached at two or more conductor pad or lead frame locations. After formation of the final bond, the continuously fed wire must be broken to permit moving the bonding head to the initial location of the next bond. Breaking the wire induces a very high tensile stress that could cause bond failure. A lower tensile strength wire would reduce the bonding time for satisfactory bonding. Also a softer wire is more difficult to align under the tool. Elongation is required so that the wire may be broken off after the second bond of the wire bond is made. A large elongation would result in an undue deformation of the wire which is used in the first bond of the next wire. This would cause the bond to be inferior. Too great a elongation may result in an excessively long tail in the second bond. Contamination would cause the corrosion of aluminum metallization or later device degradation due to water or ionic contaminants that may be included in the lubricants.

F2.3. Bonding Surface.

The materials for pads on the semiconductor die include gold, aluminum, silver, nickel, copper and chromium. Aluminum is the most commonly used material in semiconductor dice. Gold is used to avoid problems in the formation of gold-aluminum intermetallics. Gold does not adhere well to silicon dioxide and a direct contact between gold and silicon is avoided. Therefore, other metals are used to form a multilayer metallization system.Bonding to the die and the terminal is affected by many film related factors which include surface smoothness, film hardness and thickness, film

preparation and surface contamination. Howell and Slemmons[27] indicated that for thermocompression bonds the uniformity, composition and the thickness of metallization were important and that, in particular, surface irregularities could prevent adequate diffusion across the wire-metallization interface and hence interfere in the bonding process. Hill[28] reported that by improving the uniformity of the metallization the reliability of the bond was increased. The hardness of the aluminum metallization is also said to be important. The metallization should be somewhat softer than the wire so that the surface irregularities may be easily smeared out to better conform to the wire. Too soft a metallization may cause other problems. The thickness of the metallization can have an effect on the bondability and the subsequent reliability of the bond. An excessively thick metallization may be very soft which would be very difficult to bond. To avoid subsequent bond failure due to intermetallic compound growth and metallurgical (Kirkendall, see F4.2) voids at the interface, Philofsky[29] suggested that the thickness of the metal film be minimized, consistent with good bonding and device design. This suggestion applied both when bonding gold wire to aluminum on the semiconductor and when bonding aluminum wire to gold plated terminals.

When the device is subjected to thermal or power cycling, wire flexing at the heel will occur. Philofsky[29] suggested that under these circumstances the thickness of the aluminum metallization should be less than one sixth the wire thickness at the heel of the gold wire wedge or stitch bonds to avoid the growth of intermetallic compounds into this region and the consequent failure of the wire at the heel of the bond. For the case of aluminum wire bonds to gold plated terminals it was suggested that the plating thickness be less than one third the wire thickness at the heel of the bond.

Excessive roughness of the bonding surfaces has been demonstrated to influence the quality of the wire bonds. The bonding surface roughness should be such that the area of the bond be large compared to the peak to peak variations in the surface.[24]

Contamination on the wire bonding surface should be avoided. For thermocompression bonding, it interfers with the intimate contact and the

interdiffusion of the wire and the metal film and contributes to making poorer bonds. The problem of contamination may be considered less for ultrasonic bonding because of the ultrasonic agitation. The contaminants could include residues of chemicals used in the photoresist and packaging plating operations, water spots, silicon monoxide, silicon dust and aluminum oxide.[24]

F2.4. Gold-Aluminum Intermetallics.

In bimetallic bonds, a gold-aluminum interface exists at the wire/bond pad interface. Gold-aluminum compounds form at this interface at a rate which increases with temperature . Above a temperature of about 125-150°C the growth becomes significant with respect to long term reliability of the wire bonds.[24]

The compounds are formed by diffusion of gold and aluminum across the interface. Gold has a greater diffusion rate and as a result will leave behind vacancies on the gold side. The process of the Kirkendall void formation can lead to two types of failure: a mechanical stress-induced failure along the locus of the voids, and an electrical open circuit caused by the coalescence of the voids. Five different compounds appear in the region where the interface exits. These include Au_2Al_2, Au_5Al_2, Au_2Al, AuAl, and $AuAl_2$.[24]

The kind of reliability problems which appear from gold/aluminum interactions depend on the wire bond type and whether a direct or expanded contact is used. Electrical failure occurs when gold wire ball bonds are made to aluminum bond pads because of the formation of an annular Kirkendall opening about the bond. The development of voids at the perimeter of the bond is accompanied by increases in the electrical resistance of the bond with time. The rate of increase in resistance with the exposure to elevated temperature is larger for thinner aluminum metallization. The bond adherence of these ball bonds is unimpaired by intermetallic compounds which react to the oxide. The intermetallic compounds adhere well to the silicon dioxide and, though brittle, can sustain a greater tensile stress than either gold or aluminum.

Mechanical failure can occur when gold ball bonds are made to thick aluminum films. This is because the supply of aluminum for reaction with the gold ball is practically unlimited. The process of void formation therefore continues uninterrupted. In this case the void formation at the interface results in a mechanically fragile bond after high temperature storage. Similar degradation can occur if an aluminum wire bond is made to a gold plated terminal where gold plating is too thick.[24]

Thus to minimize the degradation effects due to gold aluminum interactions, bonding to thick films and excessive bond deformation should be avoided.

F2.5. Bond Types.

There are several different type of wire bonds including wedge bond, ball bond, and stitch bond.[4] Wedge bonds (figure F-3), are made with a wedge or chisel-shaped tool. The end of this tool is rounded with a radius one to four times that of the wire being bonded and is made of sapphire or similar hard material. This tool is used to apply pressure to the lead wire located on the bonding pad which has been heated to the bonding temperature. Different methods are provided for precisely coaligning the bonding pad, wire, and wedge. Difficulties with wedge bonding include imprecise temperature control, poor wire quality, inadequately mounted silicon chips, or a poorly finished bonding tool.

Ball bonding is a process in which a small ball is formed on the end of the wire and deformed under pressure against the pad area on the silicon chip (figure F-5). The lead wire is perpendicular to the silicon chip as it leaves the bond area. The number of steps in this bonding operation are few and the strength of the bond obtained is strong. Aluminum wire cannot be used because of its inability to form a ball when severed with a flame. However, gold wire is an excellent electric conductor, is more ductile than aluminum, and is chemically inert. For ball bonding, hard gold wire may be used since the balling process determines the ductility of the gold to be deformed. Among the disadvantages of ball bonding is the fact that a relatively large bonding pad is required (see Appendix H-5).

Stitch bonding combines some of the advantages of both wedge and ball bonding. The wire is fed through the bonding capillary, the bonding area is smaller than for ball bonds, and no hydrogen flame is required. Either gold or aluminum wires can be bonded at a high rate.

F3. MANUFACTURING METHODS

There are several manufacturing methods for wire bonding to thick-film circuits. The most common are thermocompression bonding, ultrasonic bonding and combination of both. All these lead-bonding techniques depend upon obtaining intimate contact between the materials to obtain an atomic interface at the connection.[5]

F3.1. Thermocompression Wire Bonds.

Thermocompression wire bonding, as the name indicates, depends upon heat and pressure. In general, the bonding equipment contains a microscope, a heated stage, and a heated wedge or capillary that will apply pressure to the wire at the interface of the bonding surface as shown in figure F-4. In addition, a wire-feed mechanism is required, as is some method for manipulation and control. Bonds can be accomplished utilizing thermocompression techniques which will exceed the wire-breaking point in strength, i.e., instead of the bond breaking, the wire will break during a pull test.

Three primary conditions in thermocompression bonding are force, temperature and time. The primary conditions are interdependent and are effected by other conditions and factors. Minor changes in these variables can cause significant differences in the bonding characteristics. It is necessary to optimize the primary conditions to obtain a satisfactory bond. Short bonding time is desirable for production purposes. Low bonding temperature is desirable to avoid the degradation of the wire bonds due to gold/aluminum interactions of the device resulting from alloying effects. Low pressures are desirable to avoid fracturing or otherwise damaging the silicon beneath the bond. Too large a force may damage the semiconductor substrate or excessively deform the wire and too small a force may prevent adequate bonding. In

addition to the bond, the wire may also be the weaker link. In the ball bond the weakest link occurs in the high temperature annealed wire leading to the bond. In the stitch and wedge bonds it occurs in the region of the wire in which the cross-section has been reduced by the bonding tool. The bonding tool used in the process may of tungsten carbide, titanium carbide, sapphire and ceramics.[24]

F3.2. Ultrasonic Wire Bonds.

Ultrasonic wire bonding also involves heat and pressure, but the heat is supplied by ultrasonic energy rather than by heated stage or capillaries as shown in figure F-6. In addition, with aluminum wire, the ultrasonic energy and the acoustical high-frequency movement of the wire against the conductor pad breaks the refracting oxides surrounding the aluminum wire. Pressure is also used but is incidental to the effect of the ultrasonic energy. The ultrasonic vibratory energy causes a temperature rise at the wire-conductor interface that can approach 30 to 50 percent of the melting point of the metal. One of the advantages of ultrasonic aluminum wire bonding is the absolute avoidance of purple plague. Purple plague, which is the embrittlement of the bond, has been found to be a result of the combination of aluminum, gold, silicon, and heat. Hence it is avoided by eliminating gold and heat.

The three primary conditions are force, time and ultrasonic power. The ultrasonic power available to make the bond is dependent on the power setting of the oscillator power supply and the frequency adjustment of the tool. The force used is large enough to hold the wire in place without slipping and to couple the ultrasonic energy into the bonding site without causing deformation of the wire. It is generally of the order of tens of grams force. The specific values selected depends on the size and the design of the bonding tool face, the size and the hardness of the wire and the sensitivity of the substrate. High power and a short bonding time is usually preferred to avoid metal fatigue and to prevent the initiation of internal cracks. Lower power nevertheless gives a large pull strength when a good surface finish exists.[24]

F3.3. Combination of Thermocompression and Ultrasonic Bonding.

The third method is the combination of ultrasonic and thermocompression wire bonding. In ultrasonic ball bonders the ultrasonic heat is identical to the usual type except a straight-wire capillary is used, as on a thermocompression bonder. Also included is the flame-off device necessary to form the ball on the gold wire. Whereas in straight ultrasonic gold-wire bonding it is difficult to bond gold wire of less than 0.002 in. diameter, on an ultrasonic ball bonder 0.001 in. diameter gold wire is usually used. The differences are in the capillary design and the fact that, in general, a heated stage is used. This process is almost a complete combination of both thermocompression and ultrasonic bonding, i.e., a heated stage, a capillary-type tool, and an ultrasonic transducer. The only thing missing is the heated capillary, which becomes unnecessary with an ultrasonic transducer.

F4. BOND FAILURE MECHANISMS

Wire bonds involve 20-30% of the microelectronic package failures.[14] Wire bond failures can be divided into two categories. The first are the failures that result from a poorly controlled or poorly designed manufacturing process that may result in an early device failure. The second category consists of the failure modes that cause adequately made bonds to fail by contamination and/or environmental stresses during the operating life of the device.

F4.1. Failure Mechanisms Due to the Manufacturing Process.

The bond strength depends on the materials and process variables associated with the substrate-metallization-wire composite structure. For example an adequate gold bond requires a bonding load large enough to produce a good interfacial conformity and a bond interface temperature high enough to effect contaminant dispersal. The purpose of compression in the bonding process is always to increase the area of contact, so as to produce a bond between area elements of fresh metal. The surface films get disrupted during the process and the bond occurs between patches of fresh metal. In the process of thermocompression bonding English[22] discovered that the bonding

temperature or the tool load substantially lower than optimum values resulted in an inadequate bond. It was found that if bonding was attempted at an extra low temperature with a corresponding load increase, little or no bonding took place. It was found that heating was not required for welding of very clean surfaces. These observations are consistent with the view that heating is required for dispersing surface contaminants. Alternatively, use of very low tool loads and high bond temperatures also resulted in bond failure and/or low bond strength. The bonding process was found to be due to a shear displacement at the intended bond interface which disrupted the contaminant layers and contributed to the bond formation. English[22] noted that leads and metallized substrates were stored in air typically for days, prior to interconnection. The surface therefore carried many adsorbed gases and, in particular, water vapor. When the substrate and the lead frame were heated the bond strength increased with temperature and the time of bake. Post-bond baking did not increase the bond strength significantly if the tool load was too low. It, however, did increase the bond strength of bonds made at low bonding temperatures.

Lang and Pinamaneni[16] identified parameters affecting wire bond strength during manufacture. These included cleaning and copper plating of the lead frames, die attach cure conditions, atmosphere during bonding, surface finish of the lead frame, bonding time, bonding force, bonding pressure, and temperature. They identified that the presence of an inert atmosphere was essential to prevent oxidation of the lead frame. Further, it was found that a lead frame with a coarse surface finish gave greater bond strengths compared to that with a smooth surface.

Weiner and Clatterbaugh[18] defined those machine parameters that could affect the shear strength of ball bonds. It was found that an increase in the ultrasonic power resulted in an increase in the shear strength of the bond. The substrate temperature was also found to affect the bond shear strength. The pedestal which supports the substrate during bonding is heated to enhance the formation of metallurgically sound bonds. The increase in pedestal temperature increases the shear strength. Occasionally it was found necessary to leave the substrate on the heated pedestal for periods longer than can be

considered normal. The effect of the extended residence on the pedestal was determined. The results indicated that that even with times up to three hours, there was no significant change in the bond shear strength. The effect of contamination, cleaning techniques and burn in on the ball shear strength was observed. It was observed that an increase in the contaminant concentration resulted in a decrease in the shear strength. The cleaning procedures used to remove the contaminants were found to vary in effectiveness, as measured by the restoration of the shear strength, depending on both the metallization and the contaminant type. Solvent cleaning was found to be the least effective method for restoring the ball shear strength to uncontaminated levels. UV-ozone used for the cleaning process was found to improve the bond shear strength most significantly. The shear strength of the bonds was found to increase after burn-in. The change in the bond shear strength, as a result of burn-in, was found to be highly dependent on both the type of the contaminant and the substrate metallization.

Poonawala[20] identified the failure of wire bonds in cannon launched devices as result of long wire distances, which caused large wire bonds and die misalignment from the center of the package cavity, skewing the wire routing and bringing some wires too close to the adjacent bond pads on the package. Two failures mechanisms were discovered during the centrifugal testing: wires collapsed straight down and created a possibility of shorting to the cavity bottom, and wires collapsed sideways and created a possibility of shorting to adjacent bond pads or adjacent wire bonds.

Deroian[17] stated that a low bond pull force could result from bonding tool pressure not uniformly compressing the wire onto the pad. Further, the organic films on the bonding surfaces were found to impair the bond strength. Koch, Richling, Whitlock and Hall[2] conducted experiments on the molding process of epoxy encapsulation of a 28 lead DIP package using a chase mold. The molding parameters considered were transfer time, mold temperature, mold compound preheat temperature and transfer pressure. Other factors considered included material flow characteristics and the kinetics of the molding compound. The experimental data showed that too fast a transfer time as measured with the mold compound in the mold increases the number of bond

failures. Further it was evident that high material preheat temperatures and high transfer pressure increased the number of bond failures. The results showed that the temperature variations across the cavities increased the variation of bond failures from one cavity to the next. It was also found that these parameters were interdependent because viscosity and flow characteristics are dependent on heat transfer and hydrostatic pressure. Also, the analysis of the material inside the mold showed that greater than 90% of the failures occurred on the opposite side of the die from the mold gate (figure F-7).

Ching and Schroen[1] Reported a theoretical bond stress model developed by Dr. L.T. Beng. The model is based on the Hertz theory of contact pressure between two spheres modified to represent the geometry of a ball bond/bond pad interface, as depicted in figure F-8. The following simplifying assumptions were made to facilitate solution:

(1) The ball was assumed to be in contact with a silicon pad.
(2) The ball was assumed to be fully formed to a spherical shape at point of first contact with the pad.
(3) The ball was assumed to maintain a spherical shape during application of the bonding force and resultant deformation of the bond pad surface.
(4) The Al-Si diffusion zone was assumed to be .001 inch thick and fully formed at time of inital contact.
(5) The ball/pad contact area was assumed to be circular and equal in diameter to either 2 or 3 times the wire diameter.
(6) Both ball and intermetallic were assumed to be elastic and to possess the mechanical properties of the gold wire.
(7) The intermetallic diffusion zone was assumed to form a spherical interface with the underlying silicon.
(8) The effects of applied ultrasonic energy on local bulk temperature and stresses were neglected.

The magnitude of the compression, tension and shear stress as a function of depth below the contact surface was evaluated at two values of bond force. As

expected, the maximum compressive and tensile stresses occurred at the surface and the maximum shear stress occurred at a depth below the surface that was considerably less than the assumed thickness of the intermetallic diffusion zone, i.e. all maximum stresses occurred in the intermetallic zone. The model predicted the existence of significant shear stress levels at the interface between the intermetallic zone and the underlying silicon, suggesting that excessive bonding force was a probable source of microcracks in the silicon. The data obtained from the model at 5 grams and 50 grams bonding force are shown in figure F-8.

The conclusion drawn from this model was that to reduce bond pad cracking the bonding force must be minimized to the lowest feasible value. The manufacturing data included parameters such as time to reach touchdown after ball formation, the moisture content, etc. It was shown that hardness of the gold ball at touch down also contributed to stress exerted on the pad. The factors that contributed to the hardness of the gold ball were the wire impurity level, the temperature of the gold ball at touch down, and the grain size as determined by the rate of cooling.

F4.2. Failure Mechanisms Due to Environmental Stresses and Other Conditions During Operating Life.

One of the failure mechanisms is the cracking of the bond pad. The bond failure in this mechanism is characterized by cracking of the underlying pad structure. Koch and Richling found that silicon nodule precipates from the metallization in the pad acted as points of high stress during the bonding of wire to the pad regions. Si nodules with about 1 μm-diameter, which grew by annealing after metal deposition, were distributed uniformly before bonding. After the bonding process was complete it was observed that Si nodules decreased in the area of bonding and damage on the insulator was observed.

Another failure mechanism is the lifting of the bond. In this mechanism the gold aluminum intermetallic that has been formed during bonding continues its growth during baking and consumes all the aluminum that is left on the pad into a solid solution. The bond pads have oxides below the metallization

which act as insulating media. This permits the MLO (multi-level-oxide) to come into direct contact with the Au-Al intermetallic. As the devices are subject to additional shear stress during temperature cycling, the adhesion between these two materials weakens, the ball is lifted during bond pull test or other loading conditions, and the oxide is exposed.

Metallurgical cracks in the heel of the first bond of the Al ultrasonic bonds was found to be a failure mechanism in bonds by Harman.[21] Cracks were found to be a result of excessively flexed wire during loop formation especially when the second bond was significantly lower than the first. The flexure was caused by operator motion of the micropositioner or by bonding machine vibration just before or during bonding tool lift-up from the first bond. The sharp metallurgical microcracks were hypothesized to propagate through the wire and cause failure during device operating life. Another metallurgical failure identified by Harman was crystallographic damage to silicon under the bonding pad caused as a result of overbonding. This is often referred to as cratering because in severe cases a hole is left in the silicon substrate after a bond is removed. Cratering in thermocompression bonding was found to result from using too high a bonding force or too great an impact velocity of the tool with respect to the substrate. Cratering could also be caused by too small a ball which allows the hard bonding tool to contact the metallization. In ultrasonic bonding, cratering was found to be a result of too hard a wire which required high power and large bonding force. Wire bond failures resulting from poor process control during wafer fabrication were found to occur if bond pad metallization was poorly adherent or was far too soft or too hard. Poor metallization adherence was found to be a result of improper sintering time and temperature and lack of substrate cleanliness. Another cause for poor bond adhesion was found to be incomplete removal of glassivation or other surface contamination from the bonding pads. Thermocompression bonds were found to be more susceptible to failure from this cause than ultrasonic bonds.

Panousis and Bonham[23] reported thermocompression bondability degradation with tantalum nitride-chromium-gold metallizations after a two hour air stabilization bake at a temperature of over 250°C. The problem was traced to

a layer of chromium-oxide resulting from diffusion of chromium through the 3 μm layer gold and its subsequent oxidation at the surface.

Electrical leakage failure during functional test constitutes another failure mechanism of wire bonds. Bonds with no visible evidence of damage or mechanical weakness were found to have intermittent electrical leakage. Leakage failure became significant in devices with an MLO-free bond pad. Failure analysis of these leakage failures revealed that there were no cracks on the pad. The leakage problem is the result of poor insulation from the Si substrate due to the lack of an MLO layer underneath the bond pad.

Cunningham[25] suggested that metallurgical (Kirkendall) voids, were a cause of bond failure. These voids were formed by the different diffusion rates of gold and aluminum as each diffuses into the other. Under various circumstances the voids may appear on either the gold or on the aluminum side of the bond region.

Aluminum wire bonded to a conventional gold metallization cavity in cerdips (ceramic dual in-line packages)[9] has been a well known reliability hazard due to "Purple plague" which is a brittle gold aluminum intermetallic which sometimes forms at an interface of a gold-aluminum thermocompression bond. This intermetallic appears purple in the crystalline form. Two types of plague-induced bond failures have been observed. In the first, the bond may be mechanically strong, but it can have a high electrical resistance or even be open circuited. In this case, which typically occurs with gold-wire bonded to thin aluminum metallization, voids form around the periphery limiting the available conduction paths. In the second type of failure, the voids lie beneath the bond. In this case the bond can fail due to mechanical weakness.

The Ag-Al system failure is very different in nature compared to Au-Al system, which is known to fail due to Kirkendall voiding of the diffusion front.[9] The high resistance in the Ag-Al bond occurs due to oxidation of the Ag-Al alloy, resulting in a thin, insulating oxide layer which completely envelops the alloyed zone.

According to Griffith's theory of brittle fracture, the fracture stress is directly related to Young's modulus of the material. The phospho-silicate glass (PSG) layer beneath the bond pad has a lower Young's modulus than the thermal oxide layer due to the inherently lower density and high impurity concentration of phosphorous in the PSG oxide (figure F-9). The number of bond failures increases as a function of phosphorous concentration in the PSG film. The PSG layer will fracture and the cracks will propagate through the PSG at a lower applied stress compared to the thermally grown SiO_2 layer.

A failure mechanism in dry air was found to be due to selective oxidation of the Ag-Al alloy and activation energies were measured for various atmospheres.[3] Moisture was shown to decrease the activation energy. When the package absorbs much water before soldering, soldering heat stress causes a peeling off phenomenon of the wire ball from the Si substrate or insulator. The quality of bond will affect the bond failure rate. The Ag-Al substrate bond system has been studied and demonstrated to show an increasing resistance with time. This process is a thermally activated process and was used to assess the long term reliability of microcircuits. The resistance of the bond in this system was shown to change from negligible (0.1 ohm) to 20 ohms or higher. Forrest[8] found that there was no discernable resistance change until a critical time is reached when it rises in a dramatic manner to bond resistance values ranged as high as 20 ohms or more.

Shukla and Deo[3] found that the failure mechanism in dry air to be due to selective oxidation of the Ag-Al alloy. The expression for critical time was given as

$$t_{cr} = t_o^* \exp(\Delta H/KT)$$

where:

t_o : a temperature independent constant
ΔH : activation energy
K : Boltzmann constant
T : absolute temperature

The change in the resistivity of the Ag-Al binary system was found to be negligible till a particular critical time is reached, after which it rose to a very large value.

Koyama and Shiozaki[6] stated that the number, size of the damage and cratering were affected by the applied ultrasonic energy which caused Si nodule damage to the insulator material.

Forrest[8] noted that another failure mechanism was that of corroded wire bonds. Corrosion opened one end of the wire completely and occasionally both ends of the wire permitting the wire to move freely within the package volume causing intermittent electrical short circuits. It was found that chlorine ions had concentrated around wire bonds during the high purity water rinse. Capillary action of the wire bond to water interface concentrated any dissolved chlorine at that point causing the formation of $AlCl_3$ during elevated temperature encountered during burn-in. Exposure of the conductor material to a chlorine environment caused a replacement chemical reaction converting copper oxide to copper chloride at the substrate interface, the presence of which caused the Al wire bonds to corrode or develop high resistance intermetallics. Another failure mechanism noted was electrical noise in the output of the circuit. The cause was detected to be the formation of intermetallics due to high chlorine concentration around bonds in a ball and socket configuration. This type of bond exhibits high mechanical strength in conjunction with low conductivity due to formation of resistive compounds at the interface. When such a bond was subjected to non-destructive bond pull test, an apparent healing of noise occurred due to reduction of the bonding resistance by motion of the wire relative to the bonding surface.

Moore[19] found that hybrid circuit metallization was very susceptible to aqueous corrosion. A few contributing factors include the applied potential of the circuit power source to drive the corrosion reaction, the close proximity of the biased circuit conductors, ionic process residuals, microscopic and macroscopic galvanic couples and the small mass or the conductors. It was stated that under these conditions any quantity of electrolyte to provide ionic transport could present a significant reliability

problem. The corrosion reaction, dissolution and plating, was found to proceed at a distance up the wire from the die surface. The effect was due to a thin layer of die coat which had wicked up the wire surface. Another failure mechanism was that of silver dendrite growth from the wire bond pads of an integrated circuit. An epoxy was used to attach the gold backed die to the chip carrier die pad. After the epoxy cure the package was oxygen plasma cleaned and rinsed in DI water. The wet package was then placed in an oven to dry. It was at the drying stage that silver dendrite growth was observed. The dendrites extended out over the glass passivation layer. Another site for the corrosion was the copper winding of the chip coil. This was a type of the localized attack called pitting. The ionic process residues participated in the localized attack of the copper at the pitting sites.

Harman[21] found that vibration forces that occur in the field are seldom severe enough to cause metallurgical fatigue or other bond damage. In general, large components of assembled systems were found to fail before such forces were sufficient to damage the bonds. Schafft[24] calculated the resonant frequency as well as centrifuge induced forces for gold and aluminum wire bonds having various geometries. The minimum excitation frequency that might induce resonance and thus damage to gold wire bonds having typical geometries was found to be in the range of 3 to 5 kHz. For most aluminum wire bond geometries, the resonant frequencies required to damage the bonds were found to be greater than 10 kHz. Excitation frequencies encountered in military electronic equpment during ground operation and transportation are between 5 Hz and 55 Hz, and in airborne operation and transportation are between 5 Hz and 2000Hz. Hence, for usually employed bond wire materials, diameters and span lengths, the wire resonance is unlikely to be excited.

Harman[21] stated that in the case of hermetic devices, even if the package does not contain any corrosive materials, metallurgical bond failure modes may result from the effect of high temperature or cyclic temperature changes. If the external temperature is greater than about 150°C for long periods of time, the wire bond will partially anneal, producing a bond that is mechanically weaker in a bond pull test. Coucoulas[35] however found that in the case of ultrasonic bonds, the work hardening and other strains in the thinned layer

were partially annealed, resulting in a more reliable bond.

Wire bond failures due to temperature cycling were studied by Gaffney,[31] Villella,[32] Ravi,[33] and Phillips.[34] All of them worked on 0.001 in diameter aluminum, 1% silicon, wire bond metallurgical flexure-fatigue failures that resulted from repeated wire flexing due to the different coefficient of thermal expansion between the aluminum wire and the header as the device heated up and cooled down. The maximum flexure, and therefore the failure, was found to occur at the thinned bond heels. The heel of the chip bond was found to experience a greater temperature excursion and therefore was more prone to fail than the heel of the pad bond. Villella[32] ran extensive statistical tests with cycled devices and determined that aluminum ultrasonic bonds were more reliable in this service than aluminum thermocompression bonds. Ravi[33] experimentally investigated the metallurgical flexure fatigue of a number of aluminum alloy wires and showed that aluminum, .1% magnesium alloy wires was superior to the commonly used aluminum, 1% silicon alloy. Phillips[34] calculated wire bond geometry effects and recommended that the loop height be at least 25% of the bond to bond spacing to minimize the bond flexure.

Another wire bond metallurgical failure mode was identified by Adams[26] for gold wire in plastic encapsulated devices. A typical case of metal fatigue was encountered when the device was made to undergo thermal cycling. Adams calculated that for a ΔT of 100°C the stress due to different expansion coefficients of the wire and plastic would almost equal the breaking load of the wire, assuming that the plastic was bonded to the wire. At Westinghouse, this falure mode has been observed in packages which have been epoxy-filled.

Mantese and Alcini[15] found that accelerated Al oxidation occurs as the temperature of the bond material is elevated causing the degradation of contact. Al melts at 660°C and oxidizes readily at lower temperatures, making it unsuitable for devices which experience high temperature. Other parameters found to affect bond quality are the bonding time, ultrasonic power, tool length, tool wear and type of substrate material.

It is clear that a considerable effort has been expended to analyze bond failure mechanisms. Yet, in spite of all the work done, a unifying deterministic failure rate model for wire bonds has not been proposed. Presently, MIL-HDBK-217E serves as a standard for reliability prediction of microelectronic packages but, except in the case of hybrid microcircuits, it does not account for the role of wire bonds in device failure. This report presents an alternative to the MIL-HDBK-217E model. A deterministic approach to failure modeling has been used so that the model can be used to predict the reliability of microelectronic packages during the design phase. This will permit reliability optimization prior to the committal of a design to production.

F5. MODEL DEVELOPMENT

In this study wire bond failure models have been developed. The models address single metal bonds and the fatigue related damage which occurs when bonds between two dissimilar materials (bi-metal bonds) are formed. The models determine the number of cycles to failure as a result of the various bond failure mechanisms. The failure mechanism for which the predicted number of cycles to failure is the least value is the probable failure mechanism for the wire bond being analyzed.

F5.1. Concept of Failure Prediction Using the Cycles to Failure Approach.

Failure of the wire bond occurs predominantly as a result of fatigue caused by repeated flexure of the wire, shear stresses generated between the bond pad and the wire and shear stresses generated between the bond pad and the substrate, all resulting from temperature cycling. Flexure of the wire will produce stresses at the heel of the bond in the case of wedge bonds and stitch bonds. Reversals in the bending stresses cause the eventual fatigue (breakage) of the wire at the heel. Due to the absence of any reduced section on the ball bond failure due to flexure is uncommon for the ball bond (figure F-10).

Shear stresses between the bond pad and the substrate result from the

differences in the coefficients of thermal expansion between the substrate and the bond pad. This in turn results in the eventual detachment of the bond pad from the substrate, increase in the thermal resistance between the die and the substrate or the cratering of the substrate.

Shear stresses between the wire and the bond pad result from the differential thermal expansion between these two elements.

In encapsulated packages, if the encapsulant is in contact with the wire, the differential thermal expansion between the encapsulant and the wire can cause axial fatigue of the wire. This failure mechanism will not occur in encapsulated packages with a low modulus coating covering the wire. Since encapsulation without a low modulus buffer coating is an unacceptable practice, this mechanism is not further considered. The number of cycles to failure of a microelectronic package depends on the environmental conditions, the geometry of the wire bond and the materials of the substrate, wire and the bond pad. The fatigue failure prediction models take into account the environmental conditions and the geometry of the bond, which is consistent with the fact that the number of failures vary with the environmental conditions to which the wire bond is subjected. The stresses generated are a function of the geometry of the wire bond, the temperature fluctuation and the material properties.

The number of cycles to failure as a result of each of these mechanisms are calculated, compared, and the lowest value is the dominant failure mechanism. Any component subjected to temperature change would be acted upon by each of these failure modes simultaneously. These failure mechanisms act independent of each other. A component failure would result if the bond fails due to any of these mechanisms. The dominant mechanism would depend on the operating environment, the materials in consideration and the condition of the bond which is an implicit function of the the operating conditions.

F5.2. Failure Prediction Models for Wire Bonds.

F5.2.1. Flexure Induced Failure Prediction Model for Wire Bonds.

A wire bond subjected to temperature cycling undergoes flexure fatigue. An increase or decrease in temperature causes the wire to expand and contract. This, coupled with the differential expansion between the wire and the bond pad, would cause the wire to flex as result of temperature cycling. Inherent as it is in the process, the cross-section of the wire is greatly reduced near the bond site. This makes it the weakest point on the wire and hence the most probable site for failure due to flexing in the wire.

Consider a wedge bond as shown in figure F-11. The two positions shown in the figure indicate the bond wire orientation before and after being subjected to the temperature change, ΔT. If the curved length of the wire considered was to be assumed the same before and after flexure, then

$$\rho \psi = \rho_o \psi_o \qquad \text{(F5.1)}$$

where:

- ρ is the initial radius of curvature
- ρ_o is the final radius of curvature
- ψ is the initial angle subtended by the wire with the substrate.
- ψ_o is the final angle subtended by the wire with the substrate.

The theory of curved bending was applied to evaluate the stresses in the wire. The stresses would be maximum in the outer portion of the wire towards the center of curvature. The stresses at this inner portion of the surface of the wire would be

$$\sigma = \frac{E\,(\bar{r} - \rho)\,d\psi}{\rho_o \psi_o} \qquad \text{(F5.2)}$$

$$\sigma = \frac{E\,r\,(\psi - \psi_o)}{\rho_o \psi_o} \qquad \text{(F5.3)}$$

where:

$\bar{r}$ is the radius of the centroidal axis.

ρ is the radius at a desired section of the wire.

r = the radius of the wire (figure F-12)

$$= \bar{r} - \rho$$

Schafft[24] derived the relation between the initial angle and the final value of the angle subtended by the wire.

$$\text{Cos } \psi = (\text{Cos } \psi_o)(1 - (\alpha_w - \alpha_s)\Delta T) \qquad \text{(F5.4)}$$

On substituting equation (5.4) into equation (5.3) we get,

$$\sigma = \frac{E\, r\, ((\text{Cos}^{-1}\, ((\text{Cos } \psi_o)(1 - (\alpha_w - \alpha_s)\, \Delta T))) - \psi_o)}{\rho_o \psi_o} \qquad \text{(F5.5)}$$

where E, α_w, α_s and ΔT are defined following equation F5.8.

$$\varepsilon_f = \frac{r\, ((\text{Cos}^{-1}\, ((\text{Cos } \psi_o)(1 - (\alpha_w - \alpha_s)\, \Delta T))) - \psi_o)}{\rho_o \psi_o} \qquad \text{(F5.6)}$$

where ε_f = wire strain

$$= \sigma / E$$

This can be simplified into

$$\varepsilon_f = \frac{r}{\rho_o} \left[\frac{\text{Cos}^{-1}\, ((\text{Cos } \psi_o)(1 - (\alpha_w - \alpha_s)\, \Delta T))}{\psi_o} - 1 \right] \qquad \text{(F5.7)}$$

Examination of the geometry of typical bond wire installations suggests that a value of ψ_o = 15 degrees suitably represents this parameter for most microcircuit wire bond configurations. In Appendix F-1 it is shown that ρ_o = 35.1mm (1.382 in) suitably represents this parameter.

Incorporating the above values simplifies equation F5.7 as follows:

$$\varepsilon_f = \frac{r}{35.1}\left[\frac{\cos^{-1}\left(0.966\left(1-(\alpha_w-\alpha_s)\,\Delta T\right)\right)}{15}-1\right] \qquad \text{(F5.7a)}$$

If $\Delta\alpha = \alpha_w - \alpha_s = 0$, then $\varepsilon = 0$

If $\Delta T = 0$, then $\varepsilon = 0$

The strains reduce to zero when the temperature difference or the difference in the coefficients of thermal expansion reduce to zero. This is a $\Delta\alpha$, ΔT driven failure mechanism.

The number of cycles to failure can be related to the stress in fatigue calculated using this cycles to failure model, by Basquin's relation[37]:

$$N_{f(flex)} = A_1\,(\varepsilon_f)^{n_1} \quad \text{(cycles to failure)} \qquad \text{(F5.8)}$$

where:

$N_{f(flex)}$ is the number of cycles to failure in flexure.
ε_f is the strain computed from equation (F5.7)
A_1 is a constant for a particular material.
n_1 is a constant for a particular material.
A_1 is the constant for a particular material combination, Table 4.5-4
n_1 is a constant for particular material combination, Table 4.5-4.
E is Young's modulus, from Table 4.5-1.
r is the radius of the wire.
ψ_o is the angle of the wire with the substrate.
α_w is the coefficient of thermal expansion of wire from Table 4.5-1.
α_s is the coefficient of thermal expansion of the substrate from Table 4.5-2
ΔT is the temperature difference encountered from Table 4.5-17.
ρ_o is the initial radius of curvature of the wire.

F5.2.2. Failure Prediction Model for Shear Between the Bond Pad and the Substrate.

A component subjected to a temperature change would experience shear stresses between the bond pad and the substrate as a result of the differential expansion. These shear stresses are a result of the large difference in the coefficients of thermal expansion.

Ravi and Philofsky[30] related the shear strain in fatigue to the temperature change encountered by the relation

$$\varepsilon_{fs} = K\,\Delta T \qquad \text{(F5.9)}$$

where:

- ΔT is the temperature change encountered by the component, Table 4.5-17.
- K is the material constant from Table 4.5-6.
- ε_{fs} is the strain as a result of shear between the bond pad and the substrate.

The constant K is an experimental value which was estimated for other bond pad material-substrate combinations. The value of K was calculated theoretically for the aluminum-silicon dioxide combination, for which the experimental value was given in [30]. A ratio of the theoretical value to the experimental value would therefore factor out the parameters which were not accounted for in the theoretical calculation. The calculated factor, if applied to the theoretically calculated value for other material combinations, would yield a value close to the true experimental value. This strategy was used to calculate the value of the constant K for the various bond pad material and substrate combinations as shown in Table 4.5-6.

The shear stress in fatigue can be related to the number of cycles to failure using Basquin's relation.

$$N_{f(shear)s} = A_2\,(\varepsilon_{fs})^{n_2} \quad \text{(cycles to failure)} \qquad \text{(F5.10)}$$

where:

$N_{f(shear)s}$ is the number of cycles to failure as result of shear between the bond pad and the substrate.

A_2 is a constant for a particular material, Table 4.5-5.

ε_{fs} is the shear strain calculated from the equation (F5.9).

n_2 is a constant for a particular material, Table 4.5-5.

F5.2.3. Failure Prediction Model for Shear Between the Wire and the Bond Pad.

Bi-metal bonds experience large stresses as a result of differential thermal expansion between the wire and the bond pad. The bond is thus subjected to large shear stresses (figure F-13). The shear stresses vary in magnitude along the surface of the bond pad. They are maximum on the boundary of the bond pad and sharply decrease to more or less a constant value a short distance from the edge. The complex mechanics of the shear mechanism and the lack of experimental data forced the modeling effort to use a uniaxial model for the situation. From classical thermal analysis,

$$l_{sub}\,(\Delta T)\,\alpha_{sub} - \frac{p l_{sub}}{A_{sub}\,E_{sub}} = l_{wire}\,(\Delta T)\,\alpha_{wire} + \frac{p l_{wire}}{A_{wire}\,E_{wire}} \qquad (F5.11)$$

The substrate being in the bulk, the stresses are evaluated between the substrate and the wire instead.

where:

l_{sub} is the contacting length of the bond.

l_{wire} is the contacting length of the wire with the bond pad.

p is the force generated as a result of the differential expansion between the bond pad and the wire.

A_{wire} is the area of contact of the wire and the bond pad.

A_{sub} is the area on which the force due to differential expansion acts on the substrate.

E_{wire} is Young's modulus of the material of the wire.

E_{sub} is Young's modulus of the material of the substrate.

ΔT is the temperature change encountered due to the operating conditions.

α_{sub}, α_{wire} are the thermal coefficients of expansion of the substrate and wire, respectively.

$$\sigma_{wire} = \frac{(\Delta T)(\alpha_{wire} - \alpha_{sub})(1/A_{wire})}{(1/(A_{wire}E_{wire})) + (1/(A_{sub}E_{sub}))} \qquad \text{(F5.11a)}$$

Young's modulus of silicon is 15.5 x 10^6 psi and the silicon being in bulk $A_{sub}E_{sub} >>> A_{wire}E_{wire}$. The second term in the denominator is therefore neglected. Since $E=\sigma/E$, the expression for the strain in the wire is reduced to

$$\varepsilon_{wire} = \Delta T\ (\alpha_{wire} - \alpha_{sub}). \qquad \text{(F5.12)}$$

The strain generated in the wire can be given as

$$\varepsilon = |\ \alpha_w - \alpha_s\ |\ \Delta T \qquad \text{(F5.13)}$$

where $\alpha_w = \alpha_{wire}$ and $\alpha_s = \alpha_{sub}$.

This strain is a tensile strain therefore the shear strain from the Mohr circle is

$$\varepsilon_{fs} = (1/2)\ |\ \alpha_w - \alpha_s\ |\ \Delta T \qquad \text{(F5.14)}$$

The number of cycles to failure can be calculated from Basquin's relation using equation F5.10.

The model in usable form is:

$$N_{fshear} = A_2(\varepsilon_{fs})^{n_2} \quad \text{(cycles to failure)} \qquad \text{(F5.10)}$$

where:

$$\varepsilon_{fs} = (1/2)\ |\ \alpha_w - \alpha_s\ |\ \Delta T \qquad \text{(F5.14)}$$

where:

N_{fshear} is the number of cycles to failure due to shear.

ε_{fs} is the shear strain in fatigue.

A_2 is a constant depending on the material from Table 4.5-5.

n_2 is a constant depending on material from Table 4.5-5.

E is Young's modulus of the material from Table 4.5-1.

α_w is the coefficient of thermal expansion of the wire from Table 4.5-1.

α_s is the coefficient of thermal expansion of the substrate from Table 4.5-2.

ΔT is the temperature difference encountered by the component from Table 4.5-17.

F6. FAILURE PREDICTION STRATEGY FOR WIRE BONDS.

The number of cycles to failure as a result of each of these mechanisms is calculated, and compared. The lowest value represents the dominant failure mechanism. All these mechanisms act simultaneously and independent of each other; nevertheless, a failure as result of any of these mechanisms would constitute a failure of the wire bond. The dominant mechanism would depend on the operating environment, the materials in consideration and the condition of the bond which is an implicit function of the operating conditions. The dominant mechanism would, therefore, shift with a change in operating environment and the materials under consideration. The analysis methodology is illustrated in Figure F-14.

F7. FUTURE WORK

1. The manufacturing parameters need to be evaluated to account for their effect on the failure prediction.
2. Coffin-Manson relations, parameters that need to be evaluated are A_1, A_2, n_1 and n_2
3. Evaluation of the constant K for the biaxial stress state.
4. Finite element methods are required for more detailed analysis.
5. Fracture mechanics concepts are required to address interface failures.

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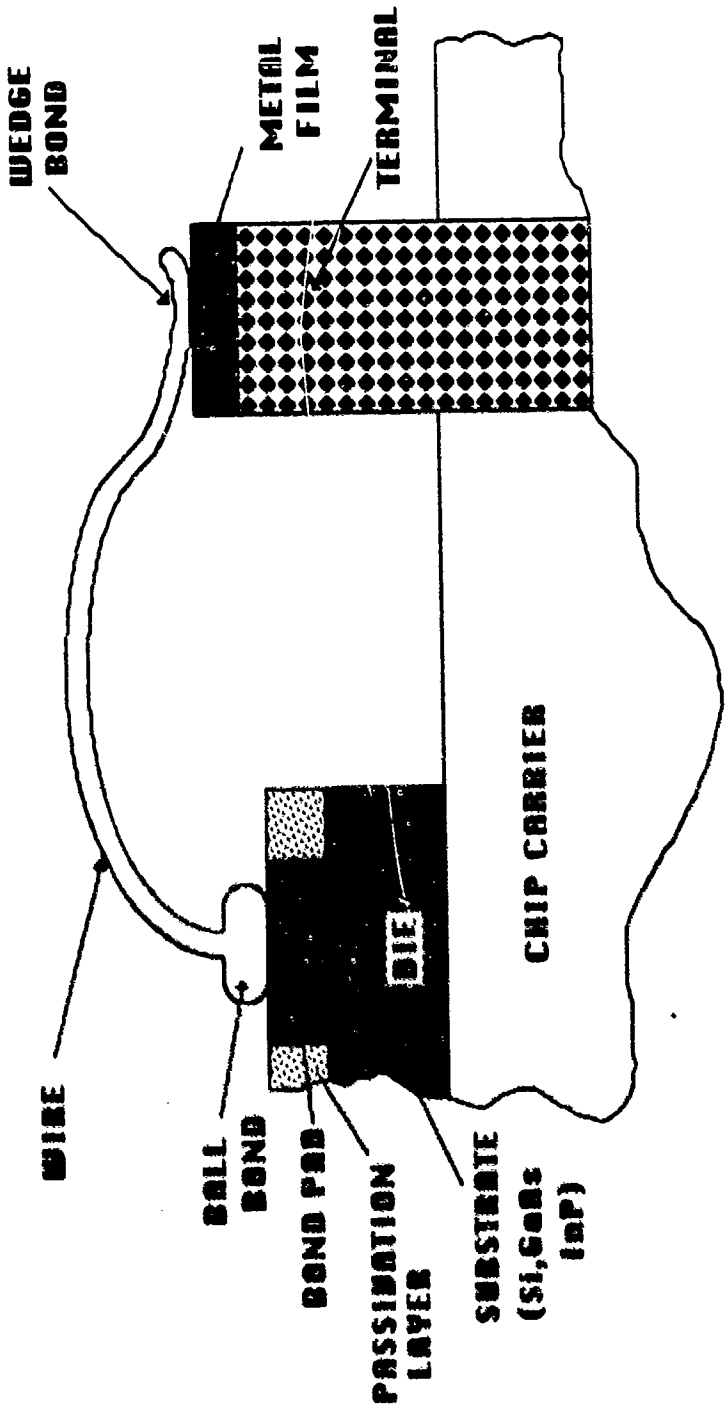
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Figure F-1



THE WIRE-WIRE BOND ASSEMBLY

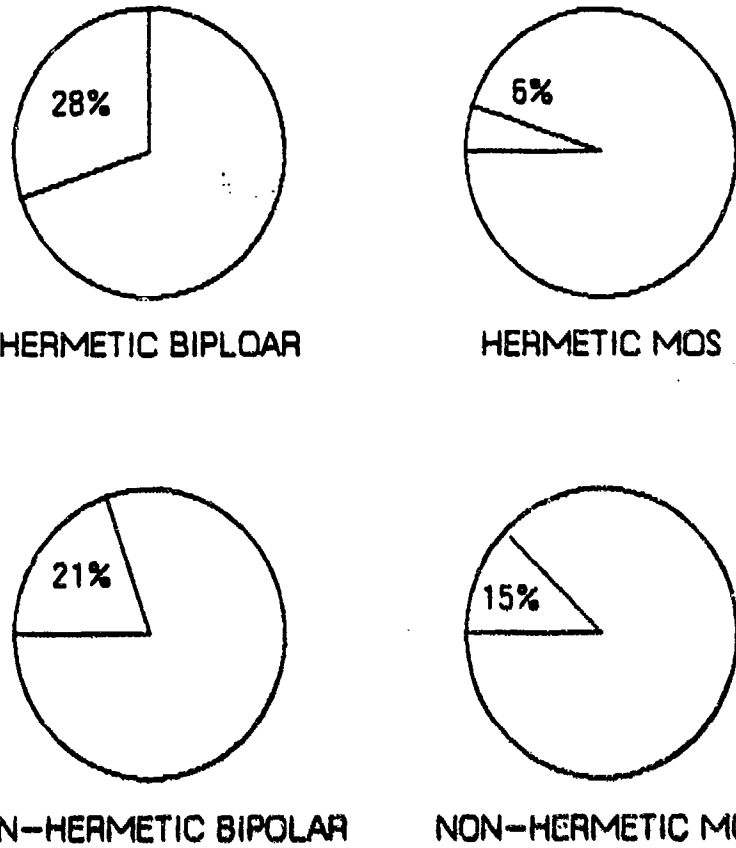

28%
6%
HERMETIC BIPLOAR
HERMETIC MOS
21%
15%
NON-HERMETIC BIPOLAR
NON-HERMETIC MOS
PER CENT OF PACKAGE FAILURES ATTRIBUTABLE TO INTERCONNECTS

Figure F-2

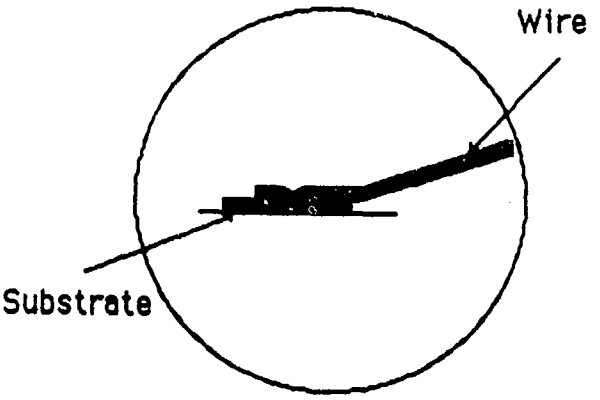


Figure F-3 The Wedge Bond

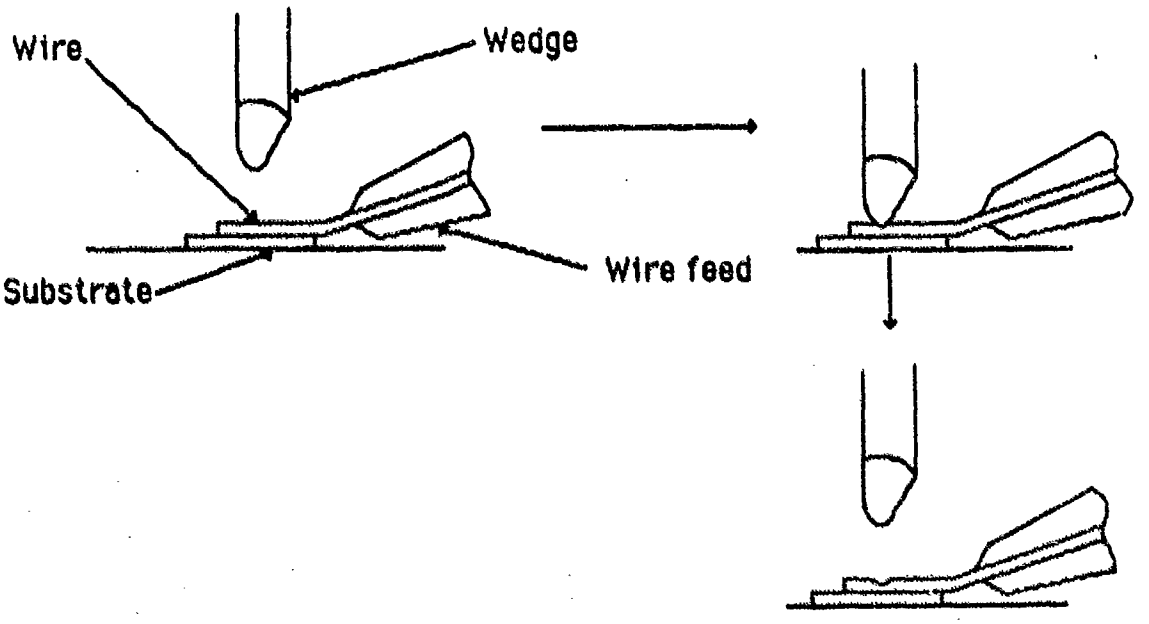
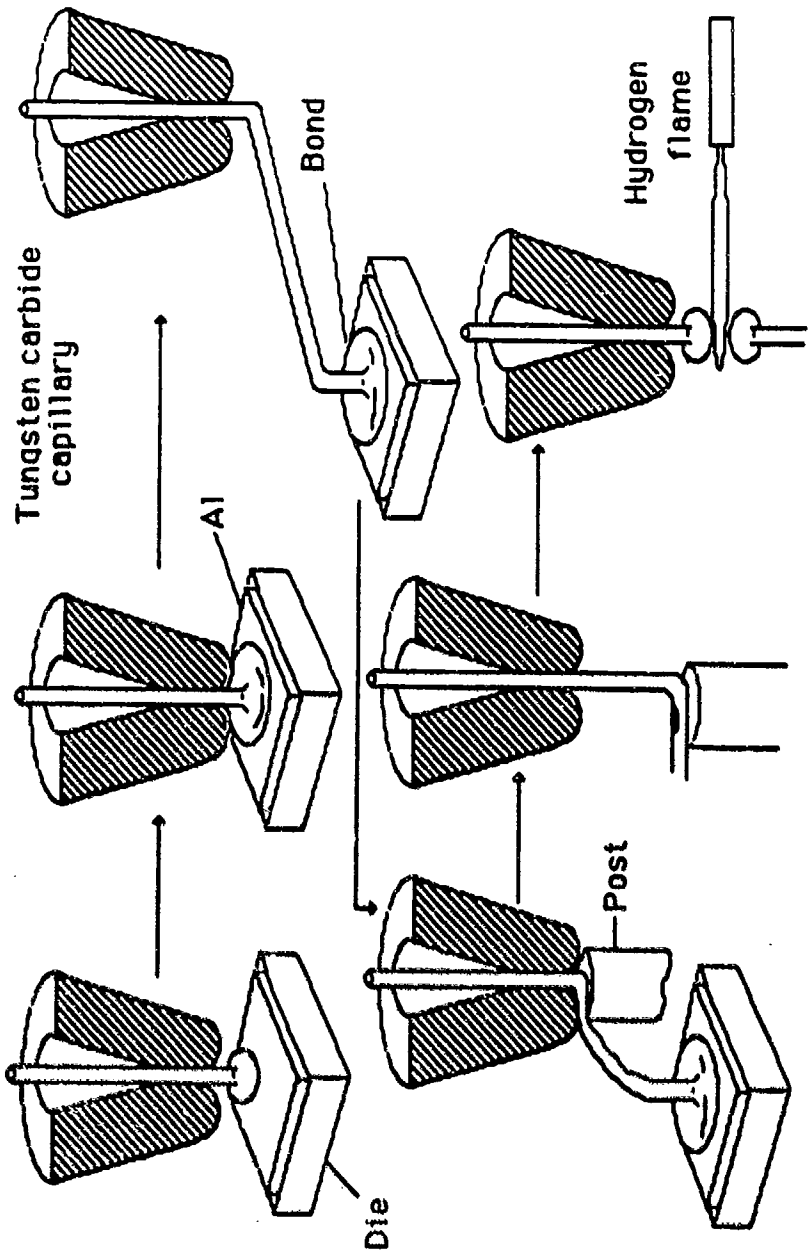


Figure F-4 Thermocompression Wedge Bonding

Figure F-5 THE BALL BONDING OPERATION



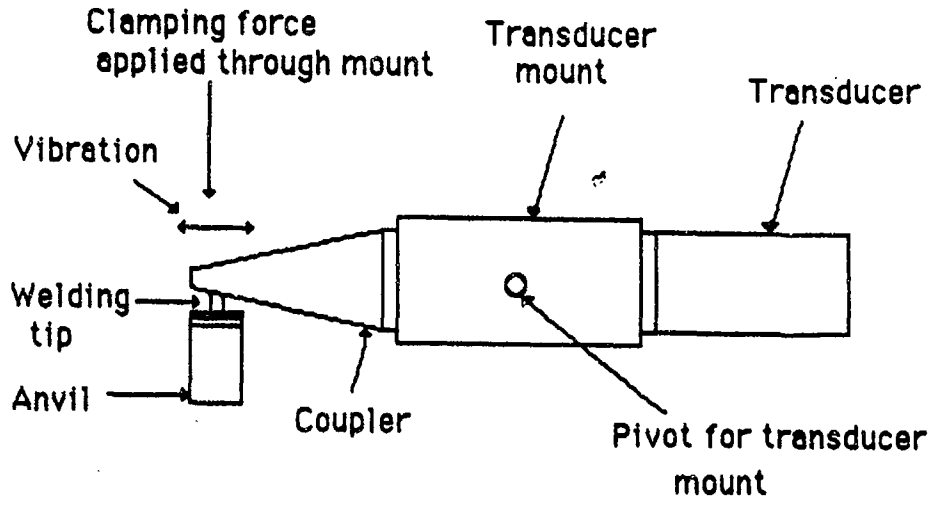


Figure F-6 Ultrasonic wedge bonding

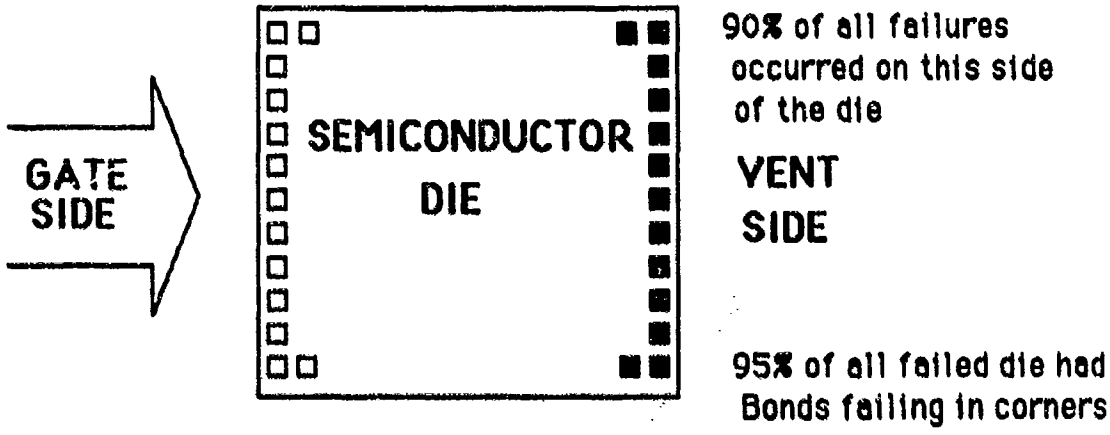
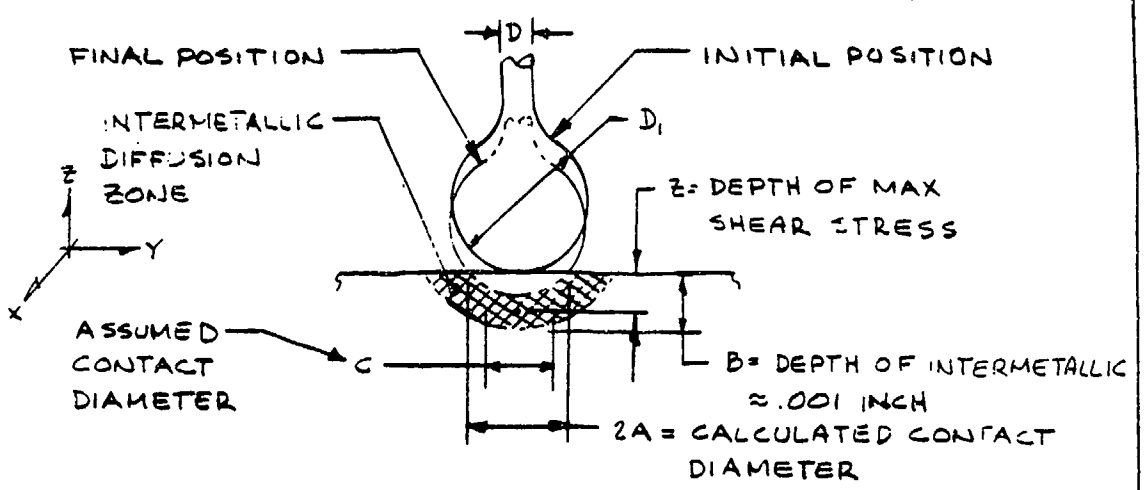


Fig. F-7 Location of failed bonds in relation to the incoming material flow during molding. Most of the failures occured on the Vent side of the die.



$z \approx 0.3\, P_{max}$ $\quad P_{max} = 2F/2\pi A^2$

$$A = \left[\frac{3FD_1(1-\mu^2)}{4E}\right]^{1/3} \qquad D_1 = B + C^2/4B$$

WHERE E = YOUNG'S MODULUS (GOLD)
P_{max} = MAXIMUM HERTZ STRESS
F = BONDING FORCE
μ = POISSON'S RATIO (GOLD)

PRINCIPAL STRESSES:

$$\sigma_x = \sigma_y = -P_{max}\left\{\left[1 - \frac{z}{A} + \tan^{-1}\left(\frac{A}{z}\right)\right](1+\mu) - \frac{1}{2(1+z^2/A^2)}\right\}$$

$$\sigma_z = -P_{max}/(1+z^2/A^2)$$

SHEAR STRESSES: $\tau_{xy} = 0$, $\tau_{xz} = \tau_{yz} = \dfrac{\sigma_x - \sigma_z}{2} = \dfrac{\sigma_y - \sigma_z}{2}$

BOND FORCE F GRAMS	C = 2D					C = 3D				
	MAX σ_z 10^3 PSI	MAX $\sigma_x = \sigma_y$ 10^3 PSI	MAX τ 10^3 PSI	z 10^{-3} IN	τ@B DEPTH 10^3 PSI	MAX σ_z 10^3 PSI	MAX $\sigma_x = \sigma_y$ 10^3 PSI	MAX τ 10^3 PSI	z 10^{-3} PSI	τ@B DEPTH 10^3 PSI
5	76	60	24	0.12	3	45	36	14	0.17	~0
50	186	130	52	0.30	20	*	*	*	*	*

* OMITTED IN REF [1]

FIGURE F-8

HERTZ STRESS DURING BALL BOND FORMATION

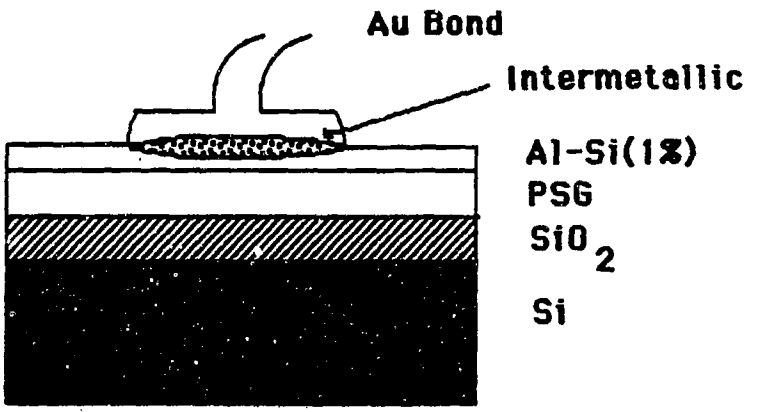


Figure F-9 SCHEMATIC CROSS-SECTION OF THE BOND PAD STRUCTURE

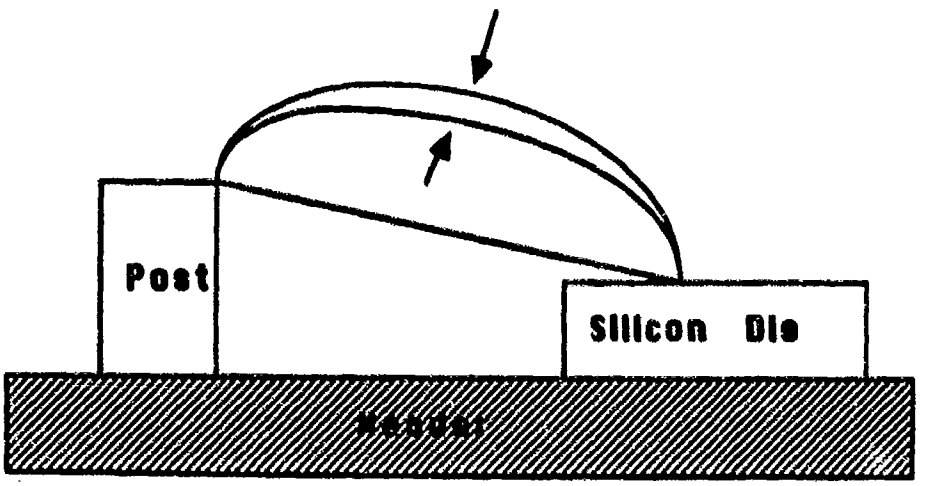


Figure F-10 SCHEMATIC REPRESENTATION OF WIRE BOND FLEXURE
DUE TO
DEVICE TEMPERATURE / POWER CYCLING

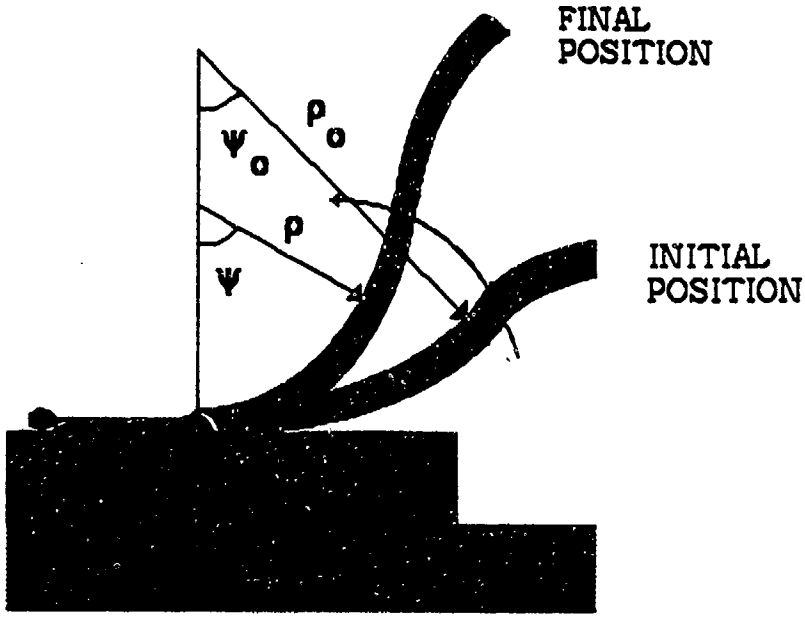


Figure F-11 FLEXURE OF THE WIRE DUE TO TEMPERATURE/POWER CYCLING

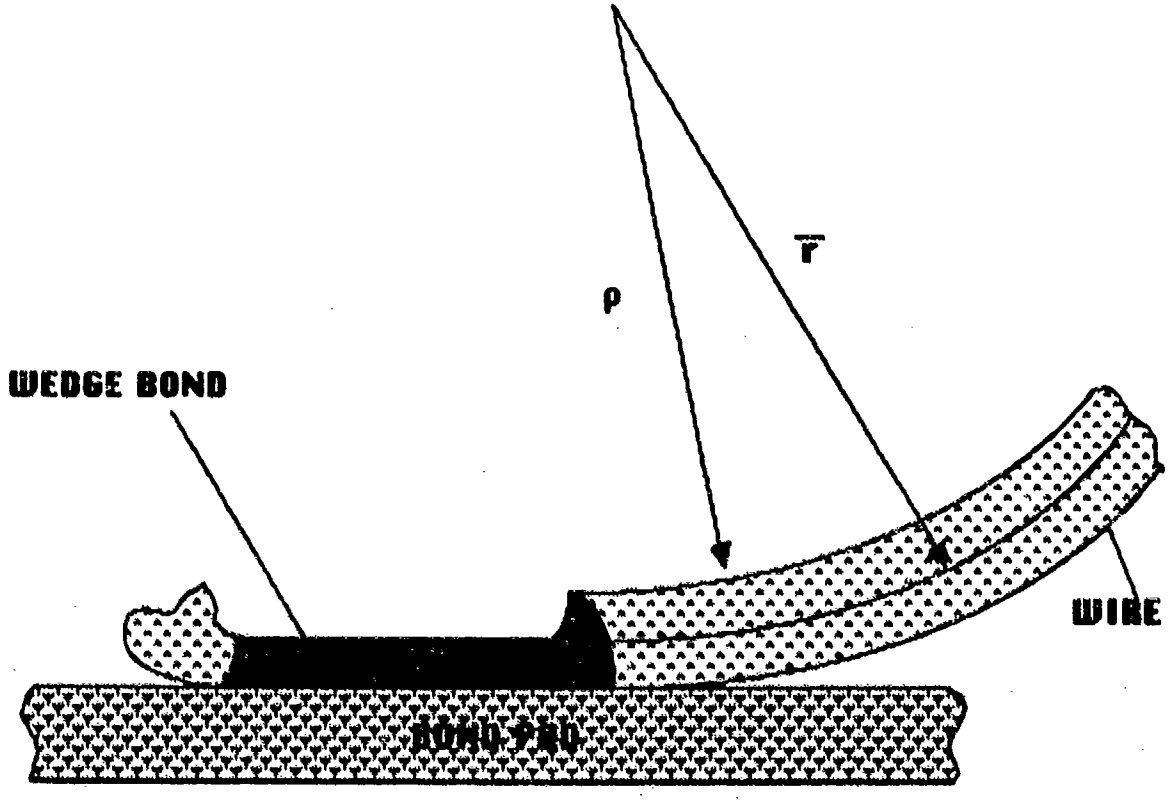


Figure F-12 THEORY OF CURVED BEAMS APPLIED TO THE WIRE BOND

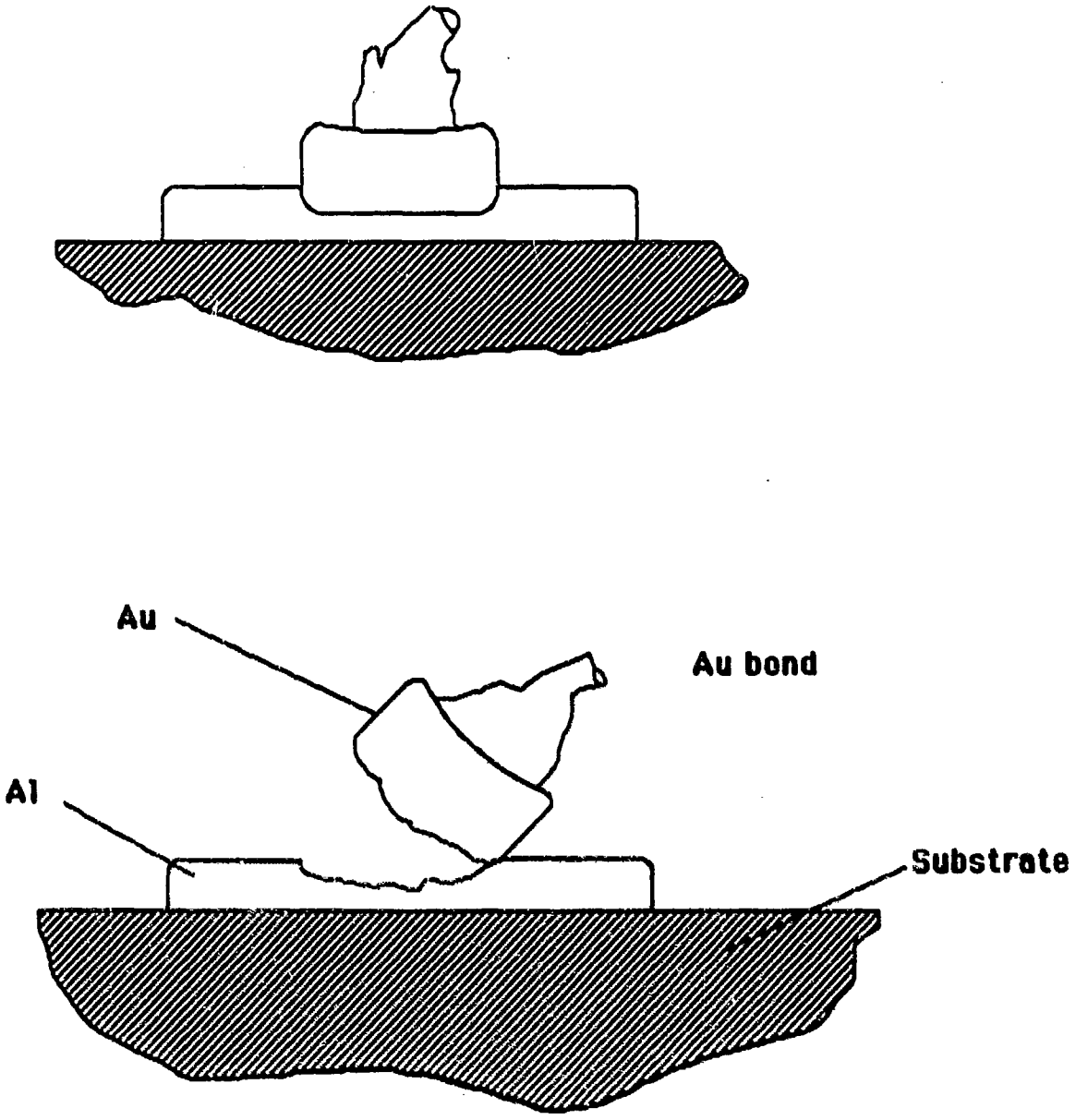


Fig. F-13 Schematic for the shearing of the gold ball bonds on Al-Au thin film diffusion couples

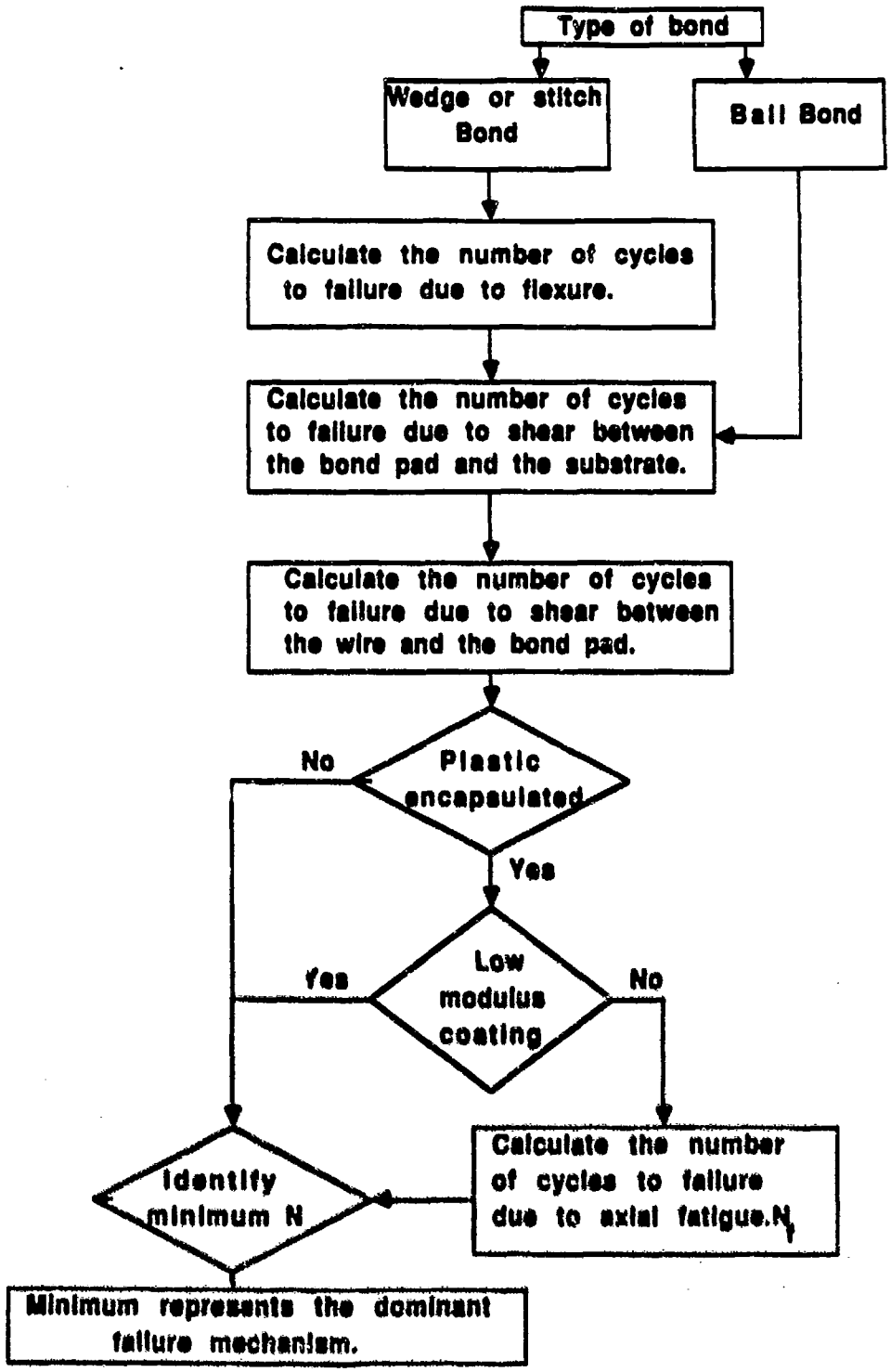


Figure F-14 **Failure prediction strategy for wire assemblies**

APPENDIX F-1

EVALUATION OF BOND WIRE BEND RADIUS ρ_o

Consider a wire of length 2L, cross-sectional moment of inertia I, made of an elastic material of stiffness E, bonded at two points separated by a span distance 2D, with a loop height h and wire diameter d, as shown in Figure F-15. When the second attachment bond is completed the curvilinear configuration of the wire induces elastic strain energy in the wire as it settles to a stable configuration. The elastic strain energy stored in the wire is principally due to bending of the wire. It is required to determine the radius of curvature ρ_o at the wire ends and the stress relief height h.

The profile of the wire in its stable configuration can be approximated with a polynominal series. The coefficients in this series will be determined by satisfying all geometric contraints and minimizing the strain energy of the wire. The minimization can be accomplished by using a standard variational scheme such as the Raleigh-Ritz method. Geometric constraints can be imposed by specifying closed form constrairts between constant coefficients in the polynominal series and by introducing Lagrange parameters when closed-form constraints are infeasible.

The wire profile is assumed to be approximated by:

$$y = \sum_{i=0}^{n} a_i u^{2i} \qquad \text{(F5.16)}$$

where $u = x/D$

Only even powers of x are considered to ensure symmetry about the y-axis.

Then $$y' = \frac{dy}{dx} = \frac{dy}{du} \cdot \frac{du}{dx} = \left[\sum_{i=0}^{n} (2i)\, a_i u^{2i-1} \right] \frac{1}{D}$$

$$= \sum_{i=0}^{n} (2i)\, b_i u^{(2i-1)} \qquad \text{(F5.17)}$$

where $b_i = \frac{a_i}{D}$

Therefore $y'' = \frac{d^2y}{dx^2} = \frac{d}{dx}(y') = \frac{d}{du}(y')\frac{du}{dx}$

$$= \left[\sum_{i=0}^{n} (2i)(2i-1)\, b_i\, u^{(2i-2)}\right] 1/D \qquad \text{(F5.18)}$$

The potential energy of the system can be written as:

$$\pi_p = U - W = \frac{1}{2}\int_V E\,\epsilon_{xx}^2\, dV - \int_x u_x\, F_x^*\, dx \qquad \text{(F5.19)}$$

where

U = strain energy
W = work done by applied tractions F_x^*

but $W = 0$ since $F_x^* = 0$

Therefore $\pi_p = U = \frac{1}{2}\int_V E\,\epsilon_{xx}^2\, dV = \frac{EI_{xx}}{2}\int_{-L}^{L} K^2\, ds \qquad \text{(F5.20)}$

where $K = \text{curvature} = \dfrac{y''}{\left[1+(y')^2\right]^{3/2}}$

$$ds = \sqrt{1+(y')^2}\, dx$$

Then

$$\pi_p = \frac{EI_{xx}}{2}\int_{-D}^{D} \frac{(y'')^2}{\left[1+(y')^2\right]^3}\left[1+(y')^2\right]^{1/2} dx \qquad \text{(F5.21)}$$

$$= \frac{EI_{xx}}{2}\int_{-1}^{1} \frac{\frac{1}{D^2}\left[\sum_{i=0}^{n}(2i)(2i-1)\, b_i\, u^{(2i-2)}\right]^2}{\left\{1+\left[\sum_{i=0}^{n}(2i)\, b_i\, u^{(2i-1)}\right]^2\right\}^{5/2}} \qquad \text{(F5.22)}$$

$$\text{or} \quad \frac{2\pi_p D}{E I_{zz}} \int_{-1}^{1} \frac{V_1(b_i, u)}{V_2(b_i, u)}\, du \qquad \text{(F5.23)}$$

Where V_1 and V_2 are functions of b_1 and u as given in equation F5.22.

Integration of equation F5.23 is done numerically using a fifteen point Gaussian Quadrature scheme. We note that minimizing π_p is the same as minimizing the fuctional;

$$\frac{2\pi_p D}{EI_{zz}}$$

The following geometric constraints are applicable:

$y = 0$ at $x = 0$ (F5.24a)

which implies that $B_0 = a_0 = 0$

$y' = 0$ at $x = 0$ (F5.24b)

which is automatically satisfied

$y' = 0$ at $x = \pm D$, or $u = \pm 1$ (F5.24c)

which implies that $\sum_{i=1}^{n} (2i)\, b_i = 0$ when equation 5.24c is imposed on b_i

The following displacement boundary conditions are applicable:

$$2L = \int_{-L}^{L} ds = \int_{-D}^{D} \sqrt{1 + (y')^2}\, dx \qquad \text{(F5.25)}$$

$$= \int_{-1}^{1} \sqrt{1+\left[\sum_{i=1}^{n} (2i) b_i u^{(2i-1)}\right]^2}\, D\, du \qquad \text{(F5.26)}$$

$$\text{or } 2\left(\frac{L}{D}\right) - \int_{-1}^{1} \sqrt{1+\left[\sum_{i=1}^{n} (2i) b_i u^{(2i-1)}\right]^2}\, du = G = 0.$$

The functional G (=0) can now be introduced into our variational formulation through a Lagrange parameter λ. Thus, the new functional to be minimized is the functional H, where

$$H = \frac{2d}{EI_{zz}} \pi_p + \lambda G \qquad \text{(F5.27)}$$

It is noted that λ has the physical interpretation of being the force along the x axis at the bond.

The function H is minimized by seeking its stationary value.

Therefore $\delta H = 0$ (F5.28)

Which implies that $\frac{\partial H}{\partial b_i} = 0$, i=1 to n (F5.29a)

and $\frac{\partial H}{\partial \lambda} = 0 = G$ (F5.29b)

However, noting from equation F5.24c that the b_i are not independent, we rewrite equation F5.29a as follows:

$$\frac{\partial H}{\partial b_i} = \frac{\partial H}{\partial b_i} + \frac{\partial H}{\partial b_n} \frac{\partial b_n}{\partial b_i} = 0, \quad i=1 \text{ to } (n-1) \qquad \text{(F5.29c)}$$

Equations F5.29b and F5.29c now constitute a set of n coupled non-linear algebraic equations in b_i (i=1 to n-1) and λ. These can be solved

iteratively for the unknowns b_1 and λ, using any standard solver software. The routine used in this study is the NEQNF subroutine from the IMSL math library.[35] This subroutine utilizes the Levenberg-Marquardt algorithm.

When the unknowns are determined, ρ_o and h can be computed as follows:

$$\frac{\rho_o}{D} = \frac{1}{DK_o} = \frac{1}{D}\left[\frac{1 + (y')^2]^{3/2}}{y''}\right|_{@\ u = \pm 1}$$

$$= \frac{\{1 + [\sum_{i=1}^{n} (2i)b_i]^2\}^{3/2}}{\{\sum_{i=1}^{n} (2i)(2i-1)b_1\}} \qquad \text{(F5.30)}$$

Values of $(\frac{\rho_o}{D})$ are plotted vs $(\frac{L}{D})$ in Figure F-15.

We note that $\frac{h}{D} = \frac{y}{D}\Big|_{@\ u = \pm 1} = \sum_{i=1}^{n} b_i$ (F5.31)

Noting that y is negative everwhere for our choice of coordinate frame, the absolute value of $(\frac{h}{D})$ is plotted vs $(\frac{L}{D})$ in Figure F-17.

It is now necessary to obtain a geometric perspective of the range of h and D. We observe that for typical microcircuit package geometry:

$$2.54\text{mm} < 2D < 10.16\text{mm}\ (0.100\ \text{in} < 2D < 0.400\ \text{in})$$
$$\text{or}\quad 1.3\text{mm} < D < 5.1\text{mm} \qquad \text{(F5.32)}$$

We also note that MIL-STD-883 visual inspection criteria prohibits a bond wire atachment without a visible loop height h, and establishes an effective maximum loop height for a specific package size by requiring a 0.127mm (5 mil) minimum clearance between the package lid inside surface and the wire. No minimum loop height is specified. However, differential thermal expansion of the wire, die and package materials effectively establishes a desireable minimum loop height to prevent axial stress in the wire at maximum temperature

difference. It is common practice for visual inspection purposes to express bond wire clearances and loop height in multiples of the wire diameter, as follows:

$$h = kd \quad (k > 1) \qquad \text{(F5.33)}$$

where d and h are defined in Figure F-15.

It can be shown that axial stress will not occur in typical microcircuits for the span distance range shown in equation F5.32 when $3 < k < 8$. This result suggests that the typical loop height range is:

$$0.08\text{mm} < h < 0.25\text{mm} \quad (0.003\text{ in} < h < 0.010\text{ in}) \qquad \text{(F5.34)}$$

Then the ratio h/D range will be approximately as follows:

$$0.016 < h/D < 0.192 \qquad \text{(F5.35)}$$

From Figure F-16 we obtain an L/D range for equation F5.35 as follows:

$$1.00016 < L/D < 1.0229 \qquad \text{(F5.36)}$$

Then from Figure F-17:

$$1.00 < \rho_o/D < 13.5 \qquad \text{(F5.37)}$$

Substituting equation F5.32 into equation F5.37:

$$1.3\text{mm} < \rho_o < 68.85\text{mm} \quad (0.051\text{ in} < \rho_o < 2.711\text{ in}) \qquad \text{(F5.38)}$$

Choosing a median value: $\rho_o = 35.1\text{mm}$ (1.382 in)

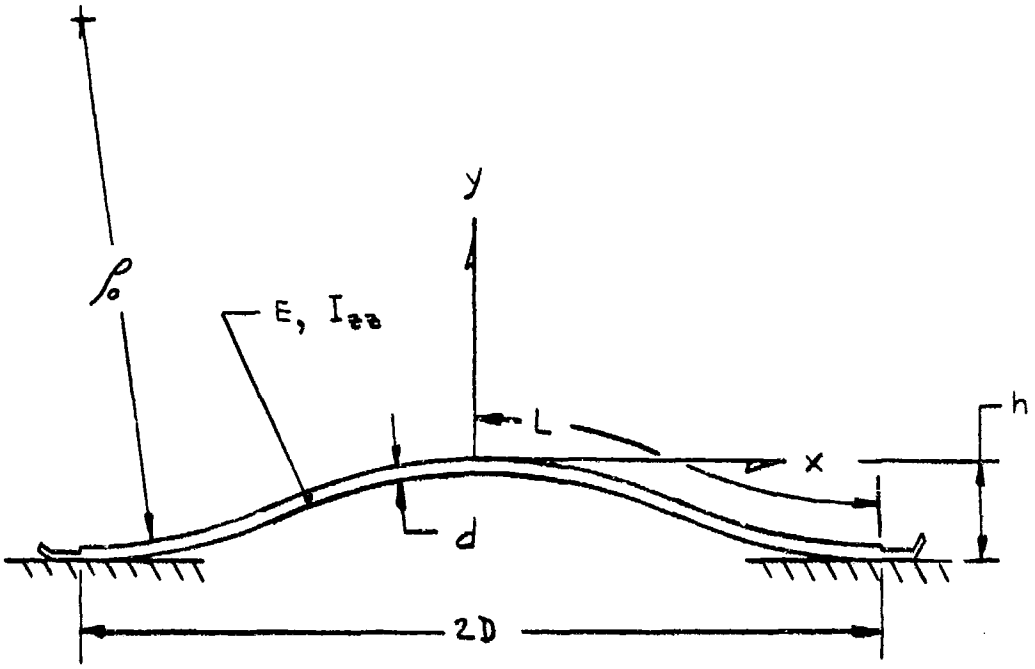


FIGURE F-15

BOND WIRE GEOMETRY

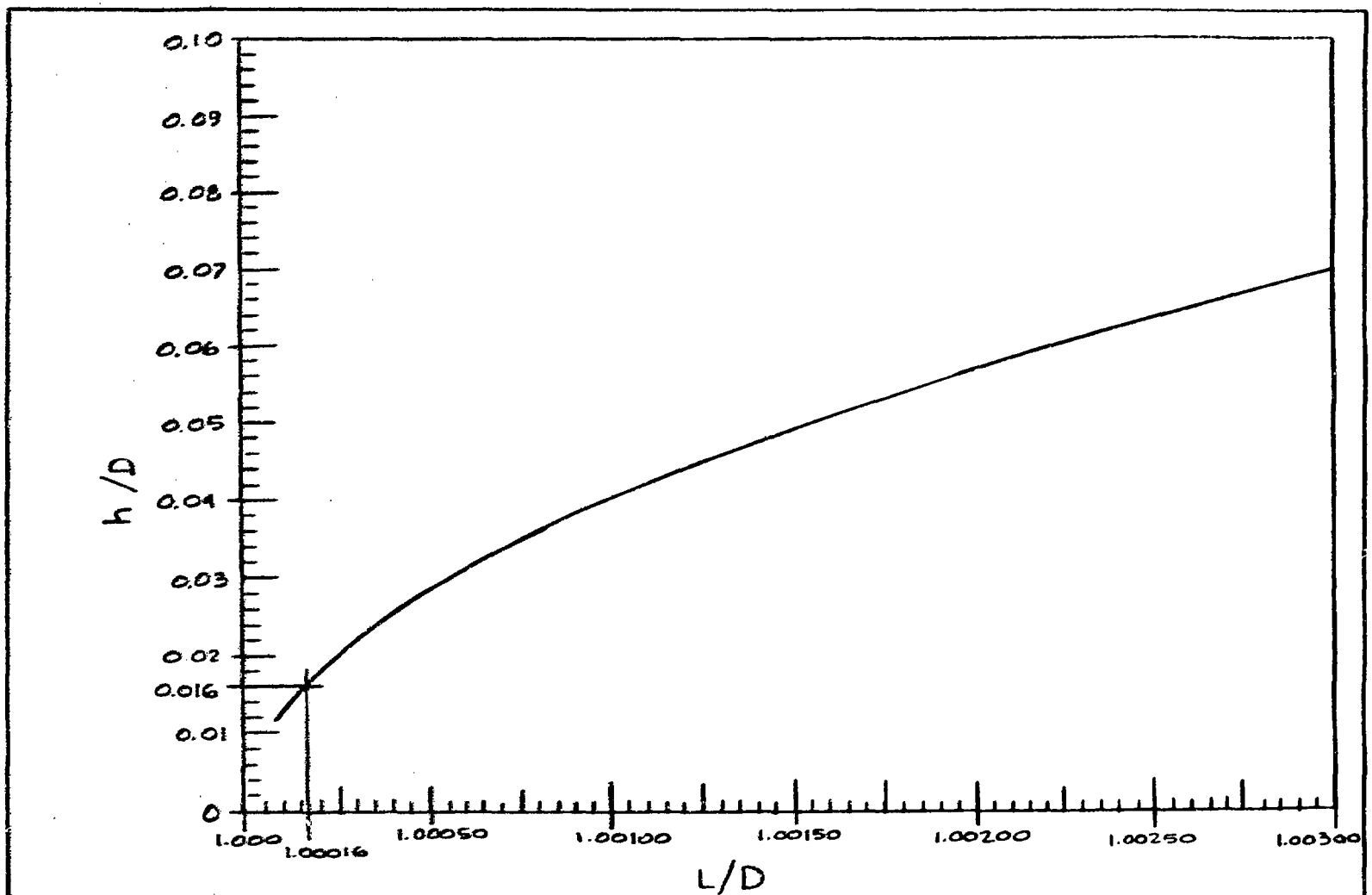


FIGURE F-16A

L/D DETERMINATION FROM h/D

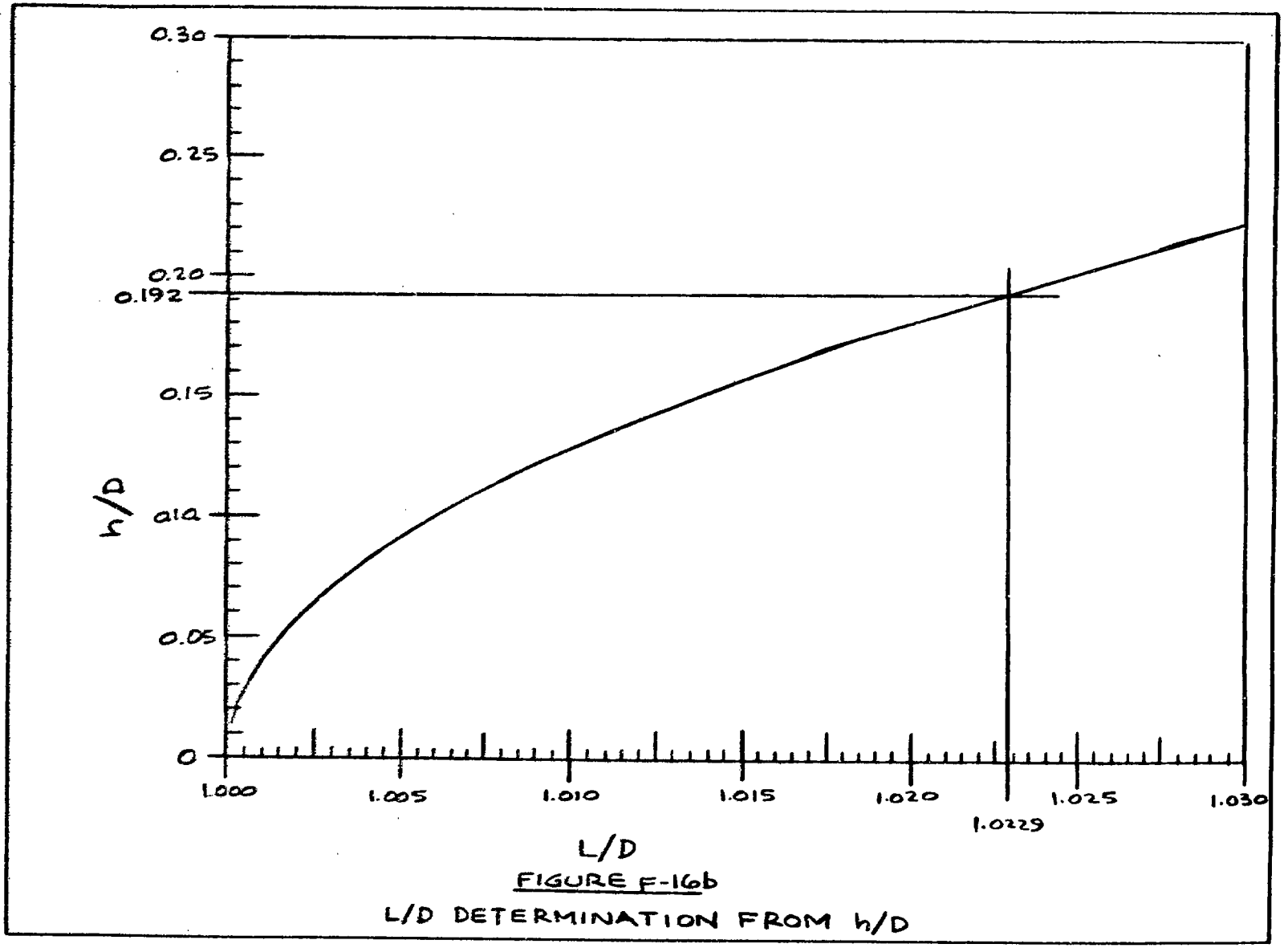


FIGURE F-16b

L/D DETERMINATION FROM h/D

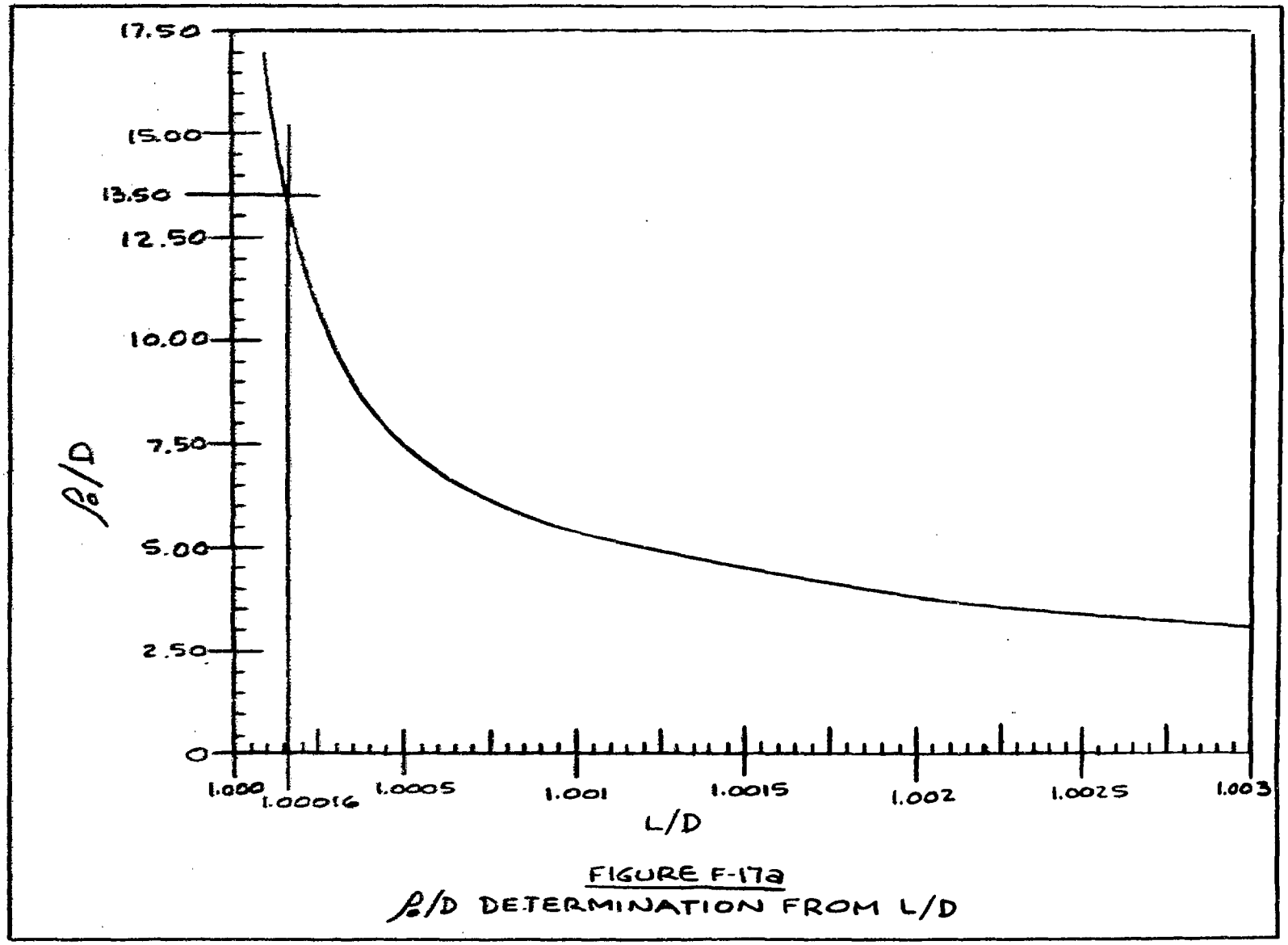


FIGURE F-17a
ℓe/D DETERMINATION FROM L/D

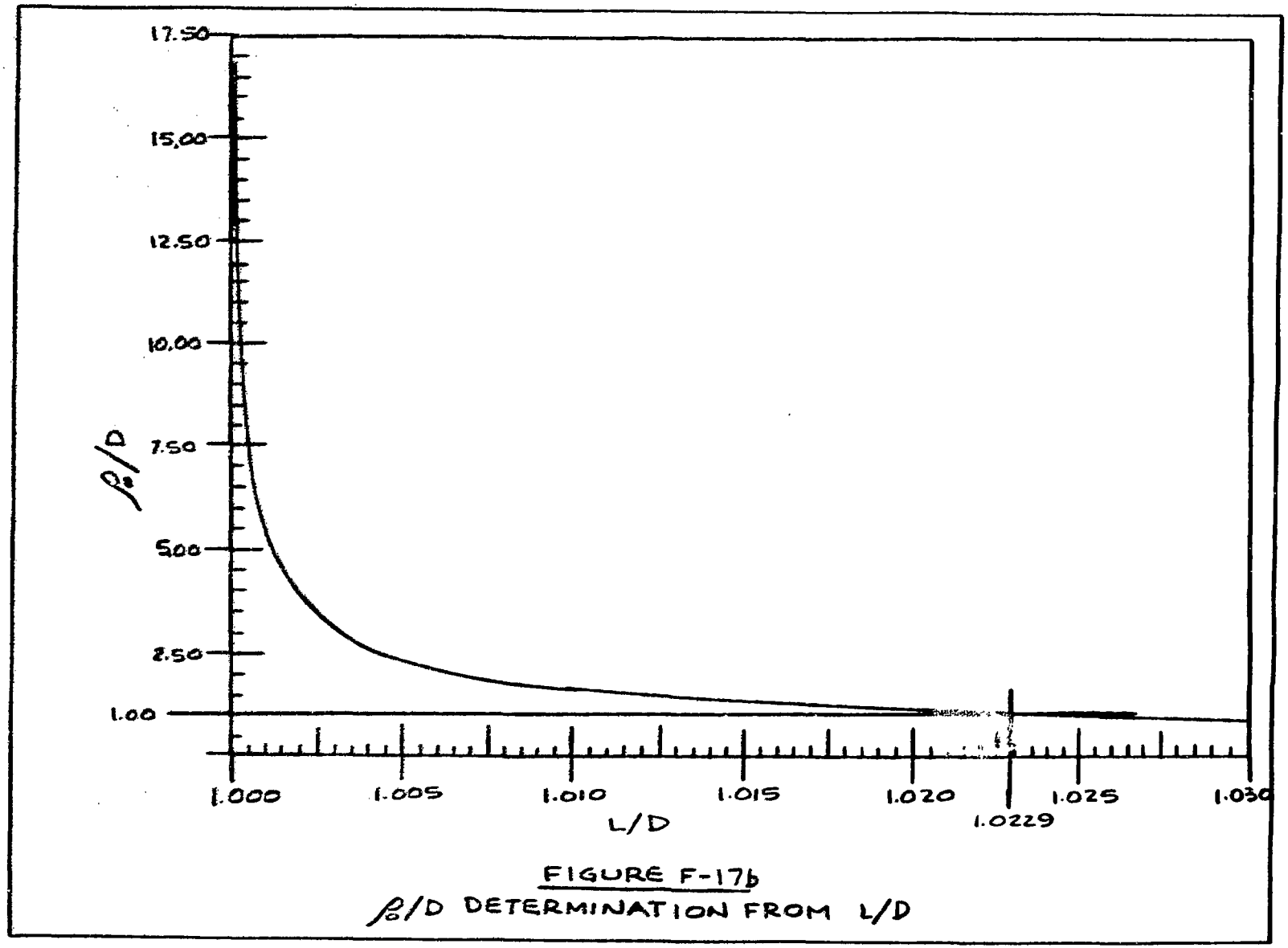


FIGURE F-17b

ρ/D DETERMINATION FROM L/D

APPENDIX G

MECHANICAL FAILURES OF DICE, DIE-ATTACH AND SUBSTRATE ATTACH IN MICROELECTRONIC PACKAGES

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G1. INTRODUCTION

The die attach unit (figure G-1) of a microelectronic component package consists of the die or chip, the die attach, the substrate, the substrate attach and the case. The die is the medium which houses the integrated circuit. Silicon, gallium arsenide and indium phosphide are common die materials. The die attach material bonds the die to the substrate. Common die attach and substrate attach materials include gold-silicon and gold-germanium eutectics, epoxies, polyimides and many solder alloys. Common case materials are ceramic, kovar, aluminum and copper. Most frequently, the die is attached directly to the case. Occasionally, a substrate is used to provide mechanical support for the die, and to provide a thermal path for heat dissipation from the die to the die package case. Common materials used for substrates are alumina, silicon, copper and beryllium dioxide. The failure mechanisms in the die, die attach and substrate attach are interdependent and are governed by the component materials, dimensions, temperature range of thermal cycles, environments and assembly processes.

The die, the substrate and the case have different thermal expansion coefficients. As the temperature rises during manufacture and power cycling, tensile stresses are developed in the central portion and shear stresses are developed at the edges of the die. Therefore, microcracks nucleate at the top surface and at the edges of the die. If the initial crack, after the manufacture of the die, is equal to or greater than the critical crack size, then the die would fail in the first cycle. If the initial crack size is smaller than the critical crack size, then it may propagate during power and thermal cycling due to fluctuations in temperature. Brittle failure of the die follows when this crack reaches the critical size. Vertical cracking of the die is caused by tensile stresses and horizontal cracking is caused by the high shear stresses at the edges.

The most common die attach defects are voids. The presence of edge voids in the die attach induces high longitudinal (shear) stresses during thermal cycling. These voids may act as microcracks, which may propagate during power and thermal cycling resulting in debonding of the die from the substrate or

the substrate from the case. This appendix discusses the failure mechanisms of the die, die attach and substrate attach and the parameters which contribute to the failure of the die attach unit.

Failure rate prediction models for die, die attach and substrate attach are then developed which consider the failure factors from a coupled mechanistic, empirical and statistical approach. The fracture mechanics approach is taken to calculate the critical crack size in the die. If the initial crack size is smaller than the critical crack size then Paris's law is used to calculate the number of cycles to failure. The die attach and substrate attach materials fail by ductile mechanisms and hence the fracture mechanics approach is not very appropriate in this situation. The Manson-Coffin relationship is used to calculate the number of cycles to failure in die attach and substrate attach.

G2. FAILURE MODELS

The development of a useful prediction model which can aid in design requires an evaluation of the of the fatigue life of the die, die attach and substrate attach due to stresses induced by thermal mismatch.

G2.1 The die failure model

G2.1.1 Stresses due to thermal mismatch

Die materials such as silicon or gallium arsenide have different thermal expansivities than commonly used substrate and case materials. Thus at manufacture, during cool down after the die attachment or during power cycling, the die attach becomes thermally stressed as shown in figures G-2(a), (b) and (c).[1] Tensile stresses are developed at the top central portion of the die and shear stresses are developed near the edges of the die. These stresses increase with the size of the chip and are responsible for the initiation and propagation of microcracks. Ultimate fracture of the brittle die can occur suddenly, without any plastic deformation, when surface cracks at the center of the die or at the edge of the die propagate during thermal cycling and become equal to the critical crack size.

Figure G-3 shows the tensile force in the die and how it drops to zero near the edge of the joint.[2] Figure G-4 shows the maximum shear stresses for different joint thicknesses of .051, .076, .127 and .178 mm.[2] It illustrates that as the thickness increases by 3.5 times, the shear stress decreases by a factor of 1.8 only. The tensile stresses in the die are responsible for vertical cracking of the die due to surface cracks and vertical edge cracks and the shear stresses in the die are responsible for the horizontal cracking of the die as shown in Figure G-2.

G2.1.2 Effect of thickness of the die

The thickness of the die affects the stress distribution inside the die. For a silicon die attached to an alumina substrate, increasing the thickness of a die increases the average stresses inside the die.[3] The total tensile stress near the interfacial voids also increases as the thickness of the die increases. These results indicate that a thin die is less likely to fail either due to tensile stress in the active circuit region or due to voids at the die attach interface as shown in figure G-5.[3]

Lowering the die thickness clearly reduces die cracking. However, excessive reduction of die thickness lowers the mechanical strength of the die and the die becomes prone to cracking during fabrication and handling.[3]

Die and substrate attach thickness varies dependet upon the attach material type and fabrication process used to apply it. The values given in Table 4.5-18 are obtained from reference [27] and can be considered to be typical practice for die and substrate attachment in hybrid microcircuit design.

G2.1.3 Brittle fracture of the die

Three separate modes of crack surface displacement are recognized in fracture mechanics methodology[20] and are illustrated in figure G-12. Surface displacements in Mode I cracks are perpendicular to the crack plane. Tensile stresses in the material open the crack and stress concentrations at the crack tip cause crack propagation when the local allowable yield stress is exceeded.

Modes II and III cracks are caused by shearing displacements in the crack plane. Mode II is caused by an in-plane shearing force in which the crack surfaces slide perpendicular to the crack front, and Mode III is caused by an out-of-plane shearing force in which the crack surfaces produce tearing displacements that slide parallel to the crack front. Only Mode I crack displacements are of concern in microelectronic dice.

MIL-STD-883 , Method 2010 visual inspection criteria define three types of Mode I cracks viz: surface cracks, vertical edge cracks and horizontal edge cracks as illustrated in Figure G-2 and in MIL-STD-883, Figure 2010-8. The inspection criteria specifies examination of die surfaces and edges at magnification and rejection of surface cracks in active circuit areas and of edge cracks that exceed specified geometry limits. The greatest allowable crack is a Mode I vertical edge crack (see Figures G-2 and G-12) extending more than 3 mils (7.6×10^{-5} cm) from the edge for Class S devices, and 5 mils (1.3×10^{-2} cm) for Class B devices. This magnitude of allowable crack will propagate to die fracture earlier than any other acceptable crack.

In his classic 1939 paper on cracks in a two dimensional infinite solid, Westergaard[22] used a complex variable approach to show that

$$K_I = \sigma_{app} (\pi a)^{1/2} \qquad \text{(G-1a)}$$

where:

K_I = Mode I crack stress intensity factor
σ_{app} = Mode I nominal far-field applied stress
a = 1/2 crack penetration depth

In 1946 Sneddon[23] showed that for a circular penny-shaped surface crack in an infinite three dimensional solid

$$K_I = \frac{2}{\pi} \sigma_{app} (\pi a)^{1/2} \qquad \text{(G-1b)}$$

George Irwin[24] used energy methods in 1962 to extend Sneddon's results to

semi-elliptical surface flaws on a three dimensional solid to demonstrate that

$$K_{I_{max}} = \frac{1.12}{(Q)^{1/2}} \sigma_{app} (\pi a)^{1/2} \qquad \text{(G-1c)}$$

where

$$Q = \phi^2 - 0.212 \left(\frac{\sigma_{app}}{\sigma_{ys}}\right)^2 \qquad \text{(G-2a)}$$

The geometry of the crack considered by Irwin was a surface flaw of 2c length along the surface with a semi-elliptical shape penetrating to depth "a" below the surface as shown in figure G-13, section A-A.

For a brittle solid it was shown that

$$Q = \phi^2 \qquad \text{(G-2b)}$$

where

$\phi = f\left(\frac{a}{c}\right)$ and is given in terms of elliptic integrals.

In 1982 Brock[25] derived the result

$\phi^2 = 1.41$ when $a/c \simeq 0.4$

Expressing the ratio $(Q)^{1/2} / 1.12$ as a surface elliptical flaw shape parameter, m_1, we obtain $m_1 = 1.06$ when $a/c \simeq 0.4$. Hence for surface flaws approximating this geometry equation G-1c becomes

$$K_{I_{max}} = \frac{\sigma_{app}}{m_1} (\pi a)^{1/2} \qquad \text{(G-1d)}$$

A final correction factor M_K was introduced in 1965 by Kobayashi et. al.[8] to account for the free surface ahead of the crack to the far surface of the body in the thickness dimension, resulting in the following expression for the crack stress intensity factor:

$$K_{I_{max}} = \frac{M_K}{m_1} \sigma_{app} (\pi a)^{1/2} \qquad \text{(G-1e)}$$

where

$$M_K = 0.953 - 2.369\ (a/h) + 2.74\ \mathrm{Tan}\ (a/h) \qquad \text{(G-3)}$$

and

h = Thickness of die

Note that equation G-3 is valid for semi-elliptical surface cracks for which a/c is approximately equal to 0.4.

Figure G-13 is based on figures 1 and 2 from[21] and demonstrates the concept of a critical crack size. When repeated stress cycles cause a crack of initial penetration depth a_i to reach a critical penetration depth a_c (or critical surface length c_c), the crack will rapidly propagate to complete fracture of the die. The rapid propagation stage can be considered to be instantaneous.

Required visual screening of dice used in military microelectronic devices assures that all surface cracks of visually detectable size under magnification will be rejected. However, the acceptance criteria also assures that vertical edge cracks will be present in most dice. The acceptance criteria for horizontal edge cracks is much smaller than for vertical edge cracks. Hence, the model for prediction of the number of cycles to fracture for the die cracking mechanism need consider only Mode I vertical edge cracks as depicted in Section B-B of figure G-13.

The brittle failure criterion can be represented by the size of the critical crack on the external die edge. Microcracks are developed in the die during manufacture. In some cases these microcracks may be large enough to cause brittle failure of the die. Fracture of the die would occur when the crack size is equal to or greater than the critical crack size. Hence, brittle failure of the die will occur in the first stress cycle if

$$a_i \geq a_c \qquad \text{(G-4)}$$

where:

a_i = initial crack length

a_c = critical crack size needed to cause the brittle failure of the die

$$a_c = \frac{K_{Ic}^2}{\sigma_{app}^2 \pi} \qquad \text{(G-5)}$$

where:

K_{Ic} = fracture toughness of the die material, Table 4.5-7

σ_{app} = maximum applied stress

The thermomechanical stress level σ_{app} in the die has been investigated by many authors[1,2,4-6] who have derived equations for stresses developed in the die. An equation proposed by Bolger[1] is:

$$\sigma_{app} = 10^{-6}\, k\, |\alpha_s - \alpha_d|\, \Delta T \sqrt{E_s\, E_a\, L/x} \quad \text{MPa} \qquad \text{(G-6)}$$

where:

k = geometric constant, dimensionless

α_s = thermal coefficient of expansion of substrate or case, Table 4.5-9 or Table 4.5-10

α_d = thermal coefficient of expansion of die, Table 4.5-7

E_a = adhesive tensile modulus, Table 4.5-8

E_s = substrate or case tensile modulus, Table 4.5-9 or Table 4.5-10

x = adhesive bond thickness, Table 4.5-18

L = diagonal length of die

ΔT = maximum temperature change, Table 4.5-17

The geometric constant K is a function of die shape and the amount of die attach filleting. A preliminary finite element study of a square die with normal production filleting practices was conducted to evaluate K. The study suggested that K = 0.2 was a reasonable value.

It has been found that a highly correlated functional relationship exists between the die diagonal length L and the number of I/O connections on the

die.[19] A Reliability Analyst will usually know the number of active pins for a packaged microcircuit, and it can be reasonably assumed that the number of active pins is approximately equal to the number of I/O connections on the die. Reference [19] provides the following relationship:

$$L = 1.5 \times 10^{-3} + 1.0 \times 10^{-4} P \text{ meters} \qquad \text{(G-7)}$$

where: P = number of microcircuit active pins

Using equation G-7 for L, equation G-6a becomes:

$$\sigma_{app} = 2 \times 10^{-7} |\alpha_s - \alpha_d| \Delta T \sqrt{E_s E_a (1.5 \times 10^{-3} + 1.0 \times 10^{-4} P)/x} \qquad \text{(G-6b)}$$

Equations G-5 and G-6b assume that the adhesive bond thickness is less than the thickness of either the die or the substrate, the die shape is rectangular, the die and substrate are at the same temperature, and the moduli and thermal coefficients of expansion are not temperature dependent. In this equation the shear modulus of the adhesive G_a has been replaced by the tensile modulus E_a because it is very difficult to measure the shear modulus of the adhesives as compared to the tensile modulus.[1] It is assumed that the numerical differences can be absorbed into the geometric constant k.

Many terms in equation G-5 are temperature dependent. Young's modulus for two typical die attach adhesives, a silver filled epoxy and a polyimide as a function of temperature are shown in figure G-7.[7] If the die size is constant, but the adhesive type is varied, then:

$$\frac{\sigma_{app1}}{\sigma_{app2}} = \frac{T_{g1} - T}{T_{g2} - T} \frac{\sqrt{E_{a1} X_{a2}}}{\sqrt{E_{a2} X_{a1}}} \qquad \text{(G-8)}$$

where:

σ_{app} = applied stress in die using adhesive die attach
T_g = glass transition temperature for adhesive die attach
T = ambient temperature (°C)

Subscripts 1 and 2 identify the adhesive die attach materials being evaluated.

Figure G-8 shows the use of equation G-8 to compare the stresses produced for different adhesives.[1] Highest stresses are produced by glass adhesives and lowest stresses are produced by epoxy.

G2.1.4 Fatigue crack propagation in the die

A pre-existing defect may develop into a crack under the influence of thermal cycling in the die. This crack may not be of critical size at the applied service stress, but may grow to critical size gradually by stable fatigue propagation.

In 1961, Paris et. al.[9] proposed a power law to predict fatigue crack propagation based on the stress intensity factor K at or near the crack tip in the plane of propagation. As the stress varies during thermomechanical cycling, K will proportionately vary as follows:

$$\Delta K = K_{max} - K_{min} \qquad \text{(G-9)}$$

Then the rate of fatigue crack propagation, da/dN, will be given by Paris's law:

$$\frac{da}{dN} = A\,(\Delta K)^n$$

where

a = instaneous crack size
N = number of cycles
A = material dependent coefficient
n = material dependent exponent

Assuming that equation G-6b expresses the magnitude of the stress amplitude at the crack tip in completely reversed loading and equation G-1a describes the proportionate ΔK, then equation G-10 becomes:

$$\frac{da}{dN} = A\,(\sigma_{app}\,(\pi a)^{1/2})^{n} \qquad \text{(G-10a)}$$

rearranging: $$dN = \frac{da}{A(\sigma_{app}\,(\pi a)^{1/2})^{n}} \qquad \text{(G-10b)}$$

integrating: $$\int_{a_i}^{a_f} \frac{da}{A(\sigma_{app}\,(\pi a)^{1/2})^{n}} = \int_{0}^{N_f} dN = n_f \qquad \text{(G-10c)}$$

where

a_i = initial flaw size

a_f = final flaw size

N_f = number of cycles to catastrophic failure

The final flaw size a_f is seen to be identical to the critical flaw size a_c defined in equation G-5 for the given σ_{app}. Hence

$$a_f = a_c = \frac{K_{IC}^2}{\sigma_{app}^2\,\pi} \qquad \text{(G-5)}$$

$$\text{Then } N_f = \left(\frac{1}{A}\right)^{n} \frac{1}{\pi^{n/2}} \frac{1}{\sigma_{app}^{n}} \int_{a_i}^{a_c} \frac{da}{a^{n/2}} \qquad \text{(G-10d)}$$

$$= \left(\frac{1}{A}\right)^{n} \frac{1}{\pi^{n/2}} \frac{1}{\sigma_{app}^{n}} \left[\frac{a^{1-n/2}}{(1-n/2)}\right]_{a_i}^{a_c}$$

$$\text{or} \quad N_f = \frac{2}{(n-2)\,A\,\sigma^{n}\,\pi^{n/2}} \left[\frac{1}{a_i^{(n-2)/2}} - \frac{1}{a_f^{(n-2)/2}}\right] \qquad \text{(G-10e)}$$

for $n \neq 2$

where:

A = die material coefficient, Table 4.5-7

n = die material exponent, Table 4.5-7

σ = stress range, same as σ_{app}, equation G-6b

a_i = initial crack size, for MIL-STD-883, Class S

a_f = the final crack length at failure, which may be taken to be equal to the critical crack size defined by equation G-5

G2.2 The die-attach failure model

A common reason for failure of the die attach is fatigue resulting from power

cycling and environmental temperature cycling. In a typical power cycle, when the die is energized, the junction temperature rises. Later the device is turned off and cooled down. Because the die, the die attach, the die substrate and the package experience temperature differences and have different coefficients of thermal expansion, the die attach bonding the die to the substrate can experience cumulative fatigue damage.

G2.2.1 Stresses due to the presence of voids

The most common die attach and substrate attach defects are voids. Voids are responsible for weak adhesion, die lifting (figure G-9a), increased thermal resistance, and poor power cycling performance. Voids can form from melting anomalies associated with oxides or organic films on the bonding surfaces, outgassing of the die attach, trapped air in the bonds, and shrinkage of solder during solidification. Insufficient plating, improper storage, lack of cleaning, or even diffusion of oxidation prone elements from an underlying layer can generate voids during melting of die attaches. In other instances, dewetting of solder results in excessive voiding, especially when a solderable surface, a poor solderable underlying metal, or excess soldering time produces an intermetallic compound not readily wetted by the solder. Even under ideal production conditions, voids are often present due to solvent evaporation or normal outgassing during cooling of organic adhesives. Although voids can form from a number of sources, they are normally limited to an acceptable level through process control. The package construction, the die attach materials and the overall void concentration determine the actual effect of voiding on device reliability.

The formation of randomly distributed voids at the die substrate interface is generally unavoidable during the die attach process. The local stresses introduced in the die due to voids are very much dependent on the location of the voids. A finite element study done by Chiang and Shukla[3] reveals that an edge void at the interface experiences tensile longitudinal stresses while a center void experiences compressive stresses, less in magnitude than the average stress obtained in the absence of the voids, as shown in figure G-10. It is shown that the edge voids are most likely to produce die cracking due to

high longitudinal stresses. The compressive nature of the stress near the center void greatly reduces the possibility for the crack to propagate. Die cracking statistics results for two samples of equal size with edge and center voids subjected to 10 cycles of thermal shock are summarized in reference [3]. The devices with center voids show no cracks, while devices with edge voids show nearly 50% failure rate due to die cracks.

The size of the voids may reduce the thermal performance of the device by creating a large temperature gradient.[10] In poorer performing thermal packages, small concentrations of random voids have little effect on the peak junction temperature. When a relatively large contiguous void is present, the heat must flow around the void creating a large temperature gradient in the silicon and severely degrading the package's thermal performance. If a large void is instead broken up into many smaller voids, the perturbation to heat flow is less with a much smaller temperature gradient induced in the silicon surface. Figure G-11 shows the temperature drop across the silicon chip, the die bond and the package materials.

Van Kessel[26] pointed out the potential benefit of a small controlled amount of voids formed due to solvents in the die attach adhesive. Small voids formed during cure may reduce stresses by reducing the modulus of adhesive by an expansion effect, which increases the bond thickness as shown in figure G-9b. Fig G-9c shows the case with no voids, resulting in high modulus.[7]

G2.2.2 Fatigue failure in die attach materials

Epoxy, solder, polyimide and silver filled glass materials are commonly used as die-attach materials. In today's market 80% of the materials used are epoxies, 10% are gold-eutectic solders and the remaining 10% are other materials. The response of a die attach material to the thermal stresses introduced during die bonding, power and temperature cycling is directly related to its mechanical properties. Therefore, an understanding of the mechanical behavior of each die-attach material as a function of temperature is essential because both the properties and responses of the die-attach change dramatically over a typical temperature range. The mechanisms by which

a die attach adhesive can contribute to the failure of a hermetic microcircuit are by the release of Cl^-, Na^+, K^+ or other extractable ions, by the release of NH_3, BF_3, or other corrosive vapors, by die cracking or distortion due to thermal stresses and by void formation under the die due to outgassing of solvents or other volatiles.

G2.2.2.1 Epoxy and polyimide die attaches

The mechanisms by which an epoxy die attach adhesive can cause or contribute to the failure of a plastic encapsulated component are discussed in paragraph G2.2.2. Some of these failures show up during production. Most, however, introduce the more serious possibility of causing failure after final packaging and inspection.

The gold and silver-filled epoxy die attach adhesives which were introduced during the 1970's offered important cost savings and process improvements over gold eutectic solders. These generally gave excellent bond strengths, good toughness and thermal shock resistance and could be cured rapidly, in one step, at temperatures of 150°C or below. These early epoxies were sold as "100 percent solids" adhesives. They contained little or no organic solvent which had to be driven off during cure. However, these first generation epoxy die attach adhesives contained relatively high concentrations of water extractable ionic contaminants. These impurities, whether generated from the die attach adhesive or from the encapsulation compound, can severely shorten the operating lifetime of a microcircuit. Silver-filled epoxies used for die attach can be responsible for corrosion failure which occurs during humid conditions. Ions present in the epoxy can migrate in the presence of water vapor to the die surface and initiate a corrosion reaction with aluminum metallization which leads to electrical failure.

Unlike epoxy resins, which are made by a process which yields Na^+, Cl^- and H_2O as undesirable by-products, polyimide resins are made by a process which does not include ionic impurities. Silver filled polyimide die attach adhesives can be made to a very high degree of ionic purity. Polyimides yield no other corrosive gases, such as NH_3, as by-products of cure. Hence the

use of conductive polyimides for die attach, together with a parallel effort to convert to cleaner epoxy molding compounds, can essentially eliminate the previous possibility that a plastic encapsulated component will fail in service by a corrosion or dielectric breakdown mechanism.

G2.2.2.2 Gold-eutectic solders

Gold-based eutectics Au-Si, Au-Sn and Au-Ge are expensive hard solders which do not degrade from fatigue or creep damage during thermal cycling. They are still widely used in military applications and most hermetic packages, where the demand for high performance and reliability overrides the cost, but their high residual stresses lead to cracked dies.

The rigid gold-eutectic systems can not absorb the dimensional changes due to different thermals expansion rates between the die and the substrate material, causing cracks in the die and eventually device failures, mostly during thermal cycling. Fracture in Au-Si eutectic mounting of large chips in ceramic packages have been reported in the literature by several workers.[11-14] Contributing factors such as voids, non-wetting, improper anneal techniques and preform thickness are discussed and several solutions have been proposed.

G2.2.3 Fatigue failure of die attach

The Manson-Coffin equation[15-18] relates the number of cycles to failure and the plastic strain per cycle,

$$N_f = 0.5 \left[\frac{\gamma_a}{\gamma'_f} \right]^{1/c} \qquad \text{(G-11)}$$

where:

N_f = number of cycles to failure

γ_a = plastic strain amplitude, equation G-12

γ'_f = fatigue ductility coefficient, defined as shear strain required to cause failure in one load reversal, (Table 4.5-8)

c = Manson-Coffin fatigue exponent
= slope of low cycle fatigue curve of log shear strain vs. log cycles to failure, (Table 4.5-8)

γ_a is given by,

$$\gamma_a = \frac{L\,|\alpha_s - \alpha_d|\,\Delta T}{x} \qquad \text{(G-12)}$$

where:

L = diagonal die length, meters, (see paragraph G2.1.3 and equation G-7)
α_s = substrate expansion coefficient, (Table 4.5-9)
α_d = die expansion coefficient, (Table 4.5-7)
ΔT = temperature excursion per cycle, (Table 4.5-17)
x = height of the die attach

G2.3 The substrate attach failure model

Fatigue failure of the substrate attach is similar to the fatigue failure of die attach, except that in this case the dimensions and the materials are different.

Number of cycles to failure in the substrate attach is given by the Manson-Coffin relationship,

$$N_f = 0.5\,\left[\frac{L_s\,|\alpha_c - \alpha_s|\,\Delta T}{x_{sa}\;\gamma'_f}\right]^{1/c} \qquad \text{(G-13)}$$

where:

L_s = diagonal length of substrate, meters
α_c = thermal expansion coefficient of the case, (Table 4.5-10)
α_s = thermal expansion coefficient of substrate, (Table 4.5-9)
ΔT = temperature excursion per cycle, (Table 4.5-17)
x_{sa} = thickness of the substrate attach, meters

γ'_f = fatigue ductility coefficient of substrate attach defined by shear strain intercept at one load reversal, (Table 4.5-8)

c = slope of low cycle fatigue curve of log shear strain vs. log cycles to failure, (Table 4.5-8)

G3. CONCLUSIONS

1. The stresses in the die can be reduced by reducing the size of the die, by increasing the die attach thickness, by choosing the substrate to match thermal expansion coefficients, by reducing the temperature fluctuations, and by reducing the tensile modulus of die attach, and substrate.

2. The stresses in the die attach can be reduced by reducing the die size, increasing the die attach thickness, by matching the thermal expansion coefficients of die and substrate, and by reducing the edge voids.

3. Traditionally, the substrate covers more than 90% of the area of the case and therefore it has a large diagonal length, resulting in the smallest number of cycles to failure of the substrate attach. Therefore, the substrate should be divided into many small pieces to reduce the diagonal length of substrate. Also thermal expansion coefficients of the case and the substrate must be matched.

G4. RECOMMENDATIONS

1. TESTING THE MATERIAL PROPERTIES

DIE MATERIALS:

FRACTURE TOUGHNESS K_{1c}

A, n (FOR FATIGUE CRACK PROPAGATION LAW EQN. FOR DIE)

$\alpha_d(T)$, ν_d (TO COMPUTE STRESSES IN THE DIE)

DIE ATTACH MATERIALS:

$E_a(T)$, ν_a (T) (TO COMPUTE STRESSES IN DIE)

γ_f, c (FOR LOW CYCLE FATIGUE IN DIE ATTACH)

SUBSTRATE MATERIALS:

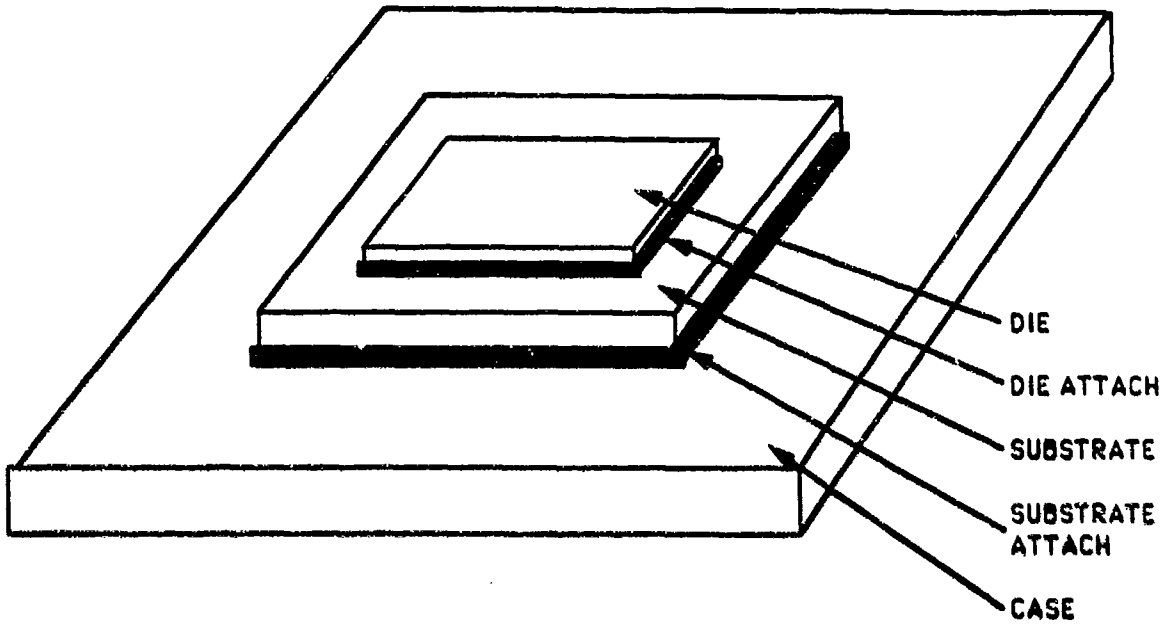
$E_s(T)$, ν_s (T), α_s (T)

2. FINITE ELEMENT STUDY
    1. TO PREDICT THE INDUCED STRAINS
    2. TO STUDY THE EFFECT OF DIE THICKNESS DUE TO BENDING-STRETCHING COUPLING
    3. TO STUDY THE EFFECT OF TEMPERATURE GRADIENTS

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DIE MATERIALS: Si, FeAs, InP

DIE ATTACH AND SUBSTRATE ATTACH

MATERIALS: Epoxies, Polyimides, Gold-eutectics, Silver Filled Glass

SUBSTRATE MATERIALS: Alumina, Aluminium

CASE MATERIALS: Kover, Aluminium, Copper

FIGURE G-1

DIAGRAM SHOWING THE DIE AND THE SUBSTRATE MOUNTED IN A HYBRID CASING

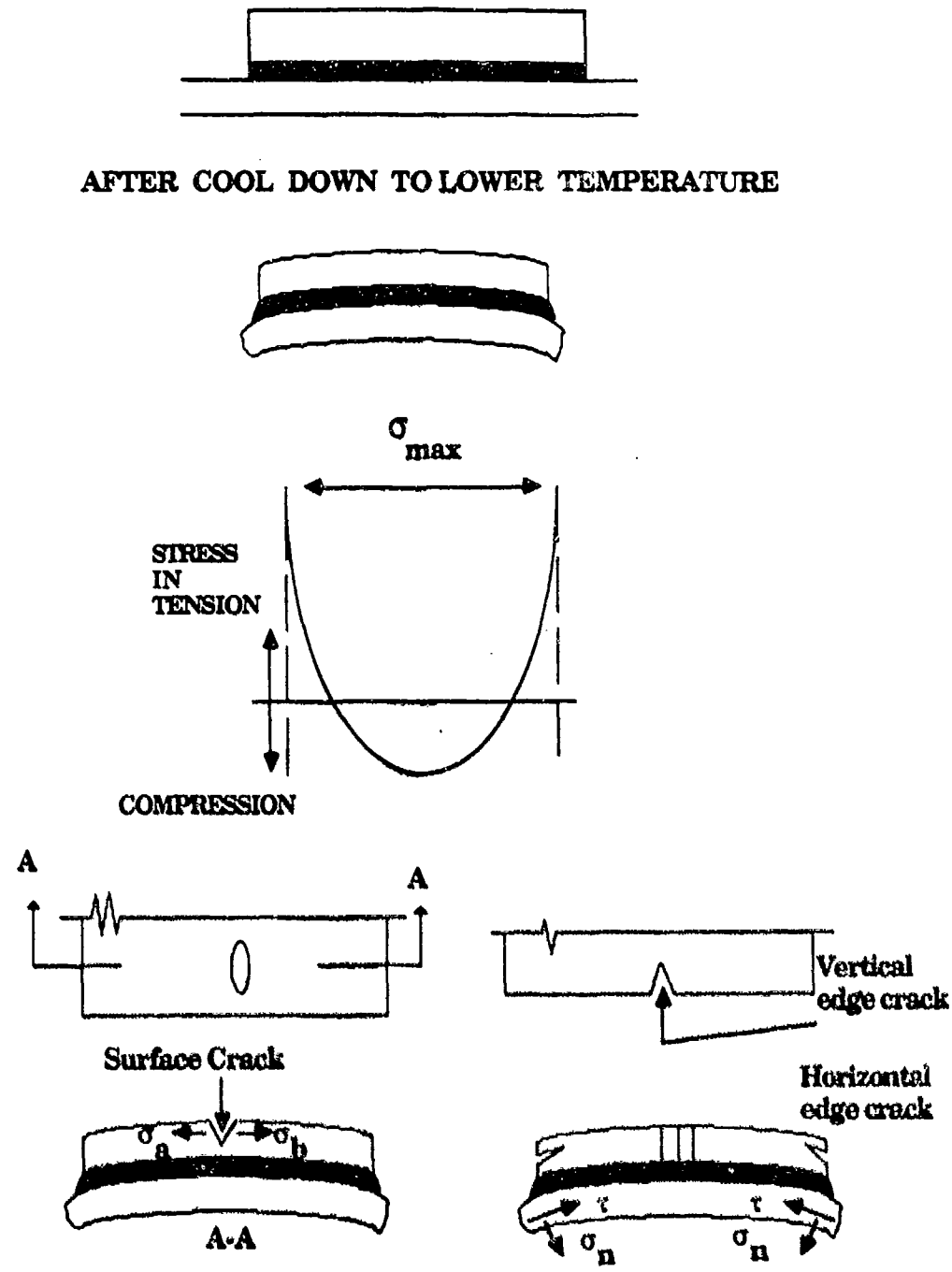


FIGURE G-2

THERMAL STRESSES IN BONDED DIE DEVELOPED AFTER CURE

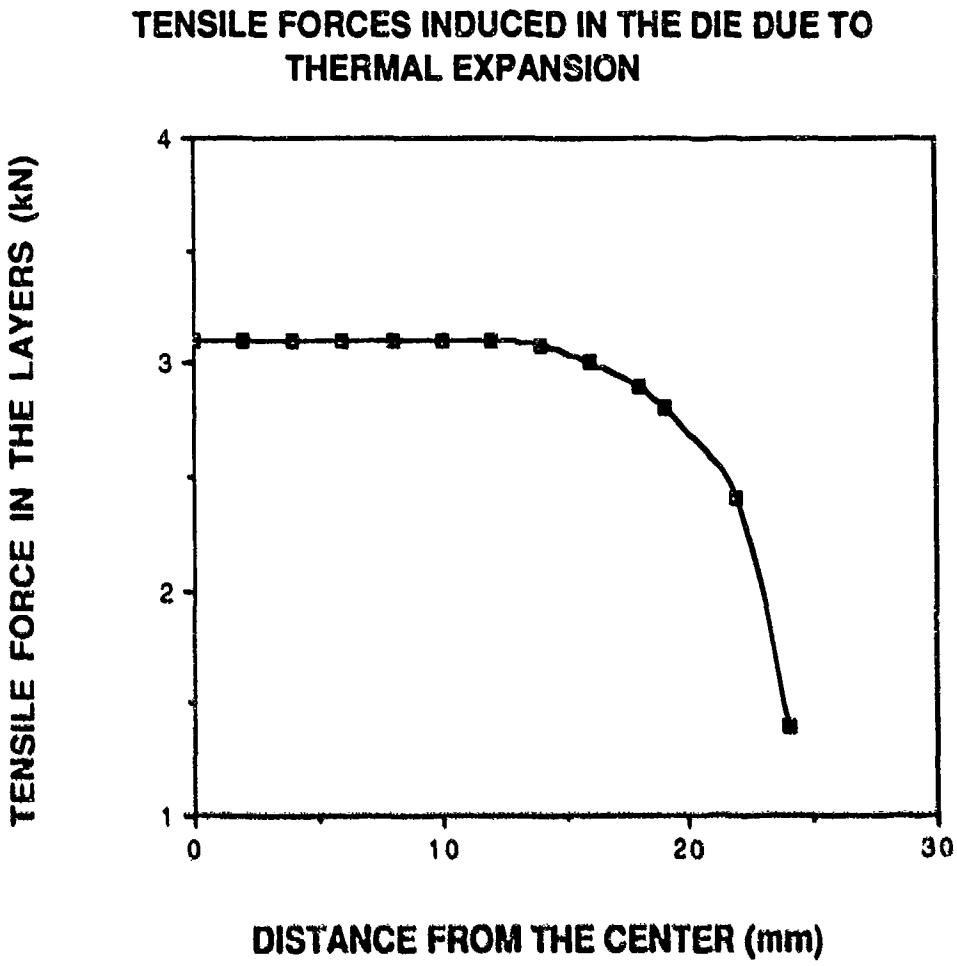


FIGURE G-3

TENSILE FORCES INDUCED IN THE DIE DUE TO THERMAL EXPANSION

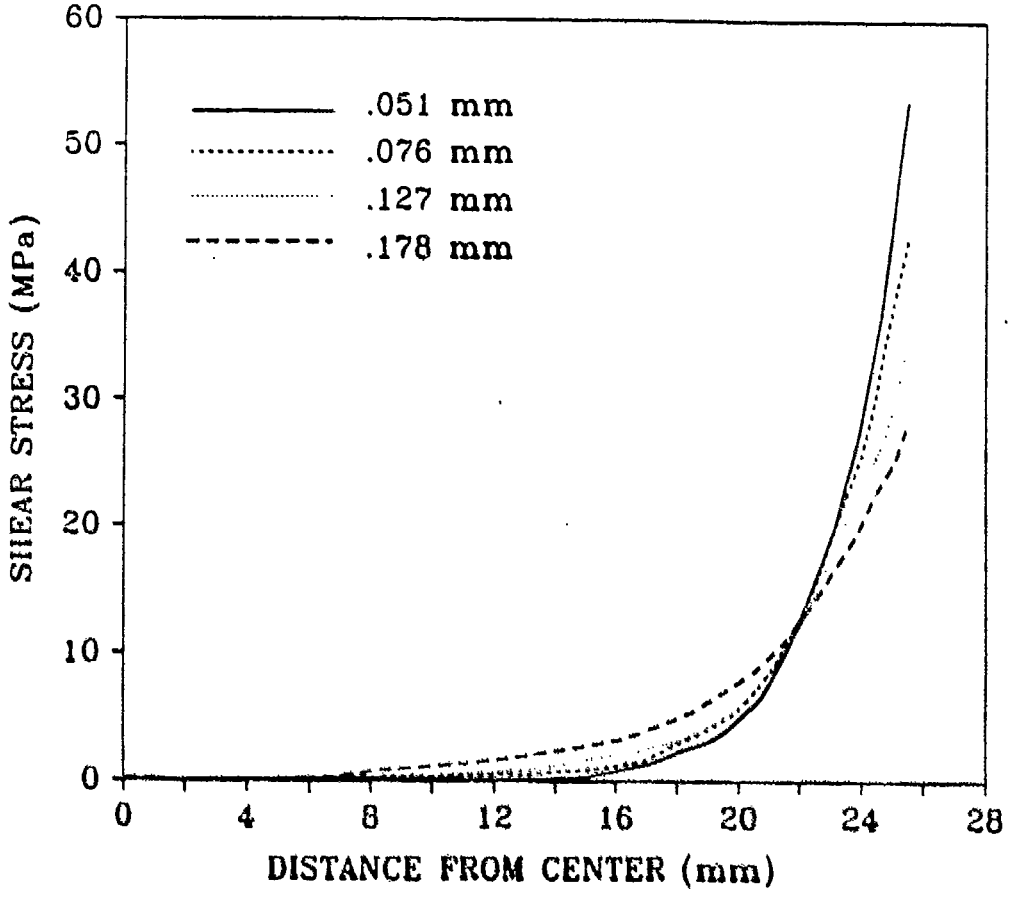
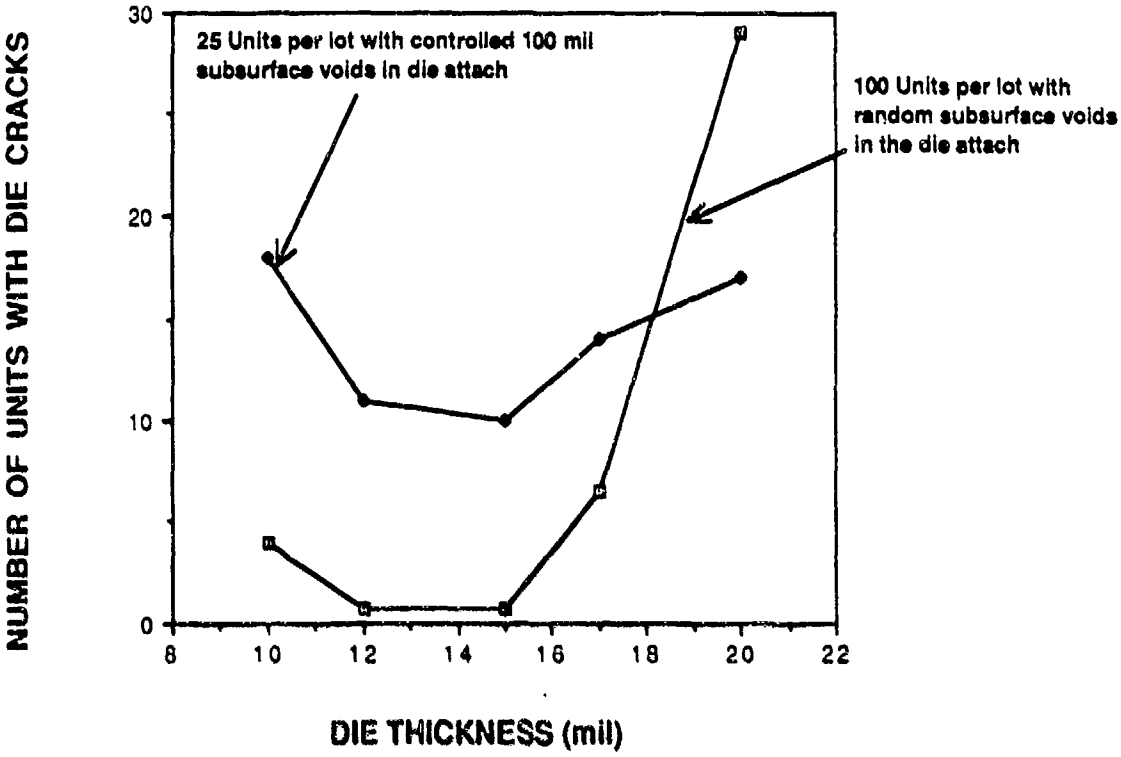


FIGURE G-4

SHEAR STRESS DISTRIBUTION OVER WIDTH OF JOINT
FOR DIFFERENT JOINT THICKNESSES



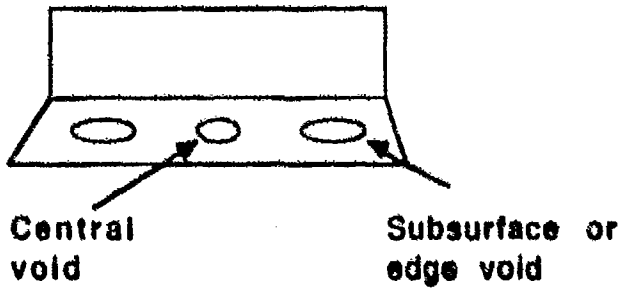


FIGURE G-5

VARIATIONS IN THE NUMBER OF DIE CRACKS AS A FUNCTION OF DIE THICKNESS

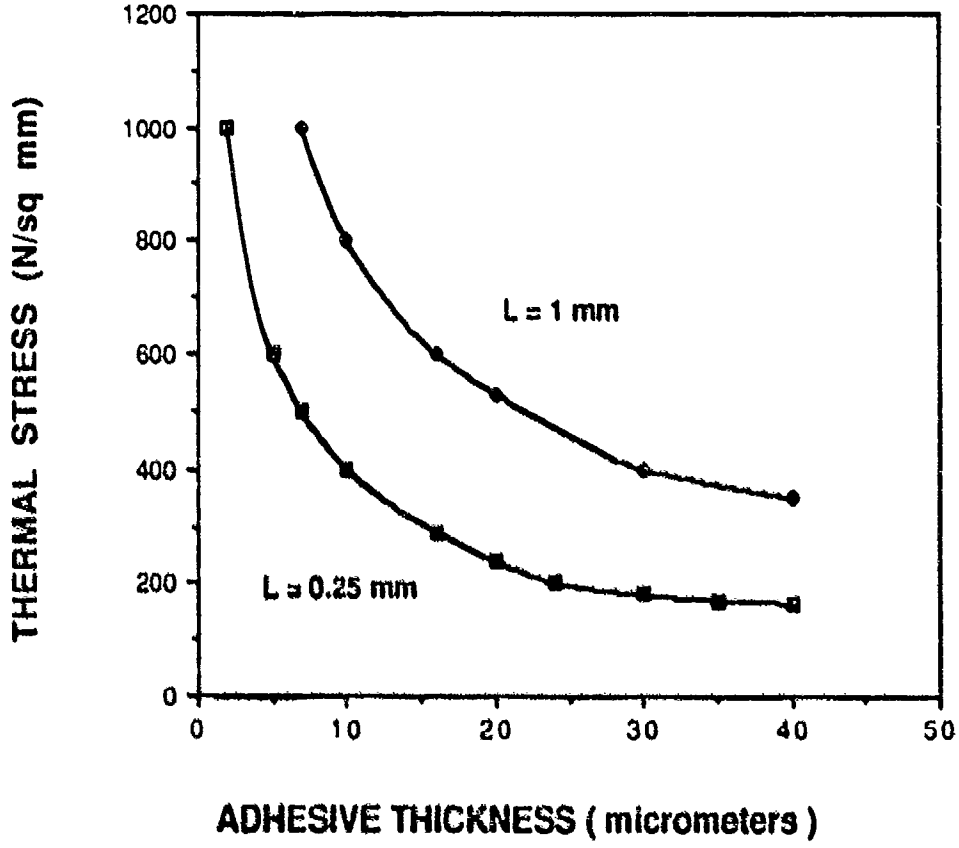


FIGURE G-6

EFFECT OF DIE DIAGONAL LENGTH (L) AND
ADHESIVE THICKNESS ON THERMAL STRESS OF DIE

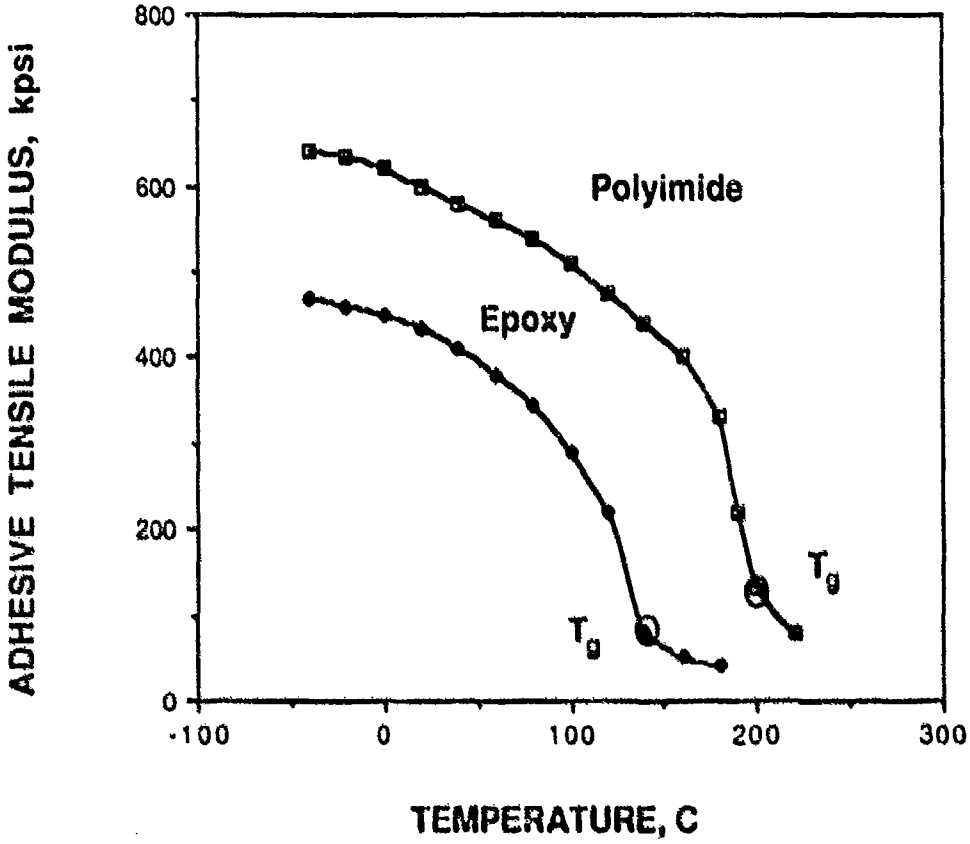


FIGURE G-7

ADHESIVE TENSILE MODULUS VS. TEMPERATURE

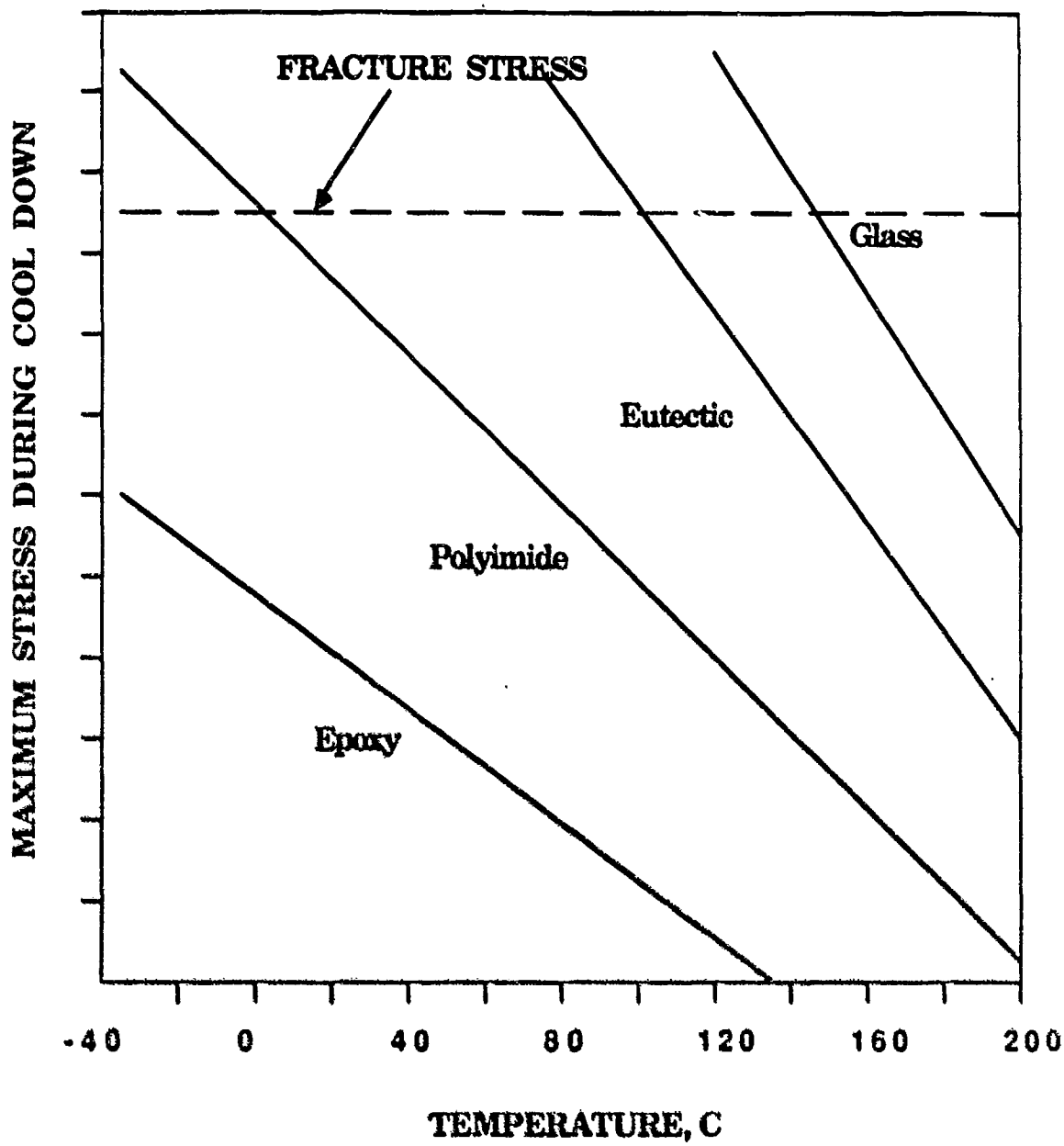


FIGURE G-8

MAXIMUM STRESSES FROM EQUATION 2(a)



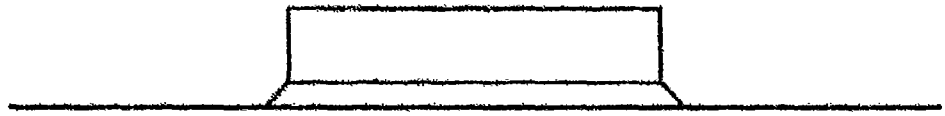
Excessive voids, low shear strength, low thermal conductivity, die cracking or "popping"

(a)



Small uniform voids, adequate strength, thermal & electrical conductivity, less stress on large dies

(b)



No voids, high modulus, high strength adhesive, possible failure by die cracking with large dies

(c)

FIGURE G-9

EFFECT OF VOID CONTENT AND SIZE ON DIE LIFT, DIE STRENGTH AND DIE CRACKING

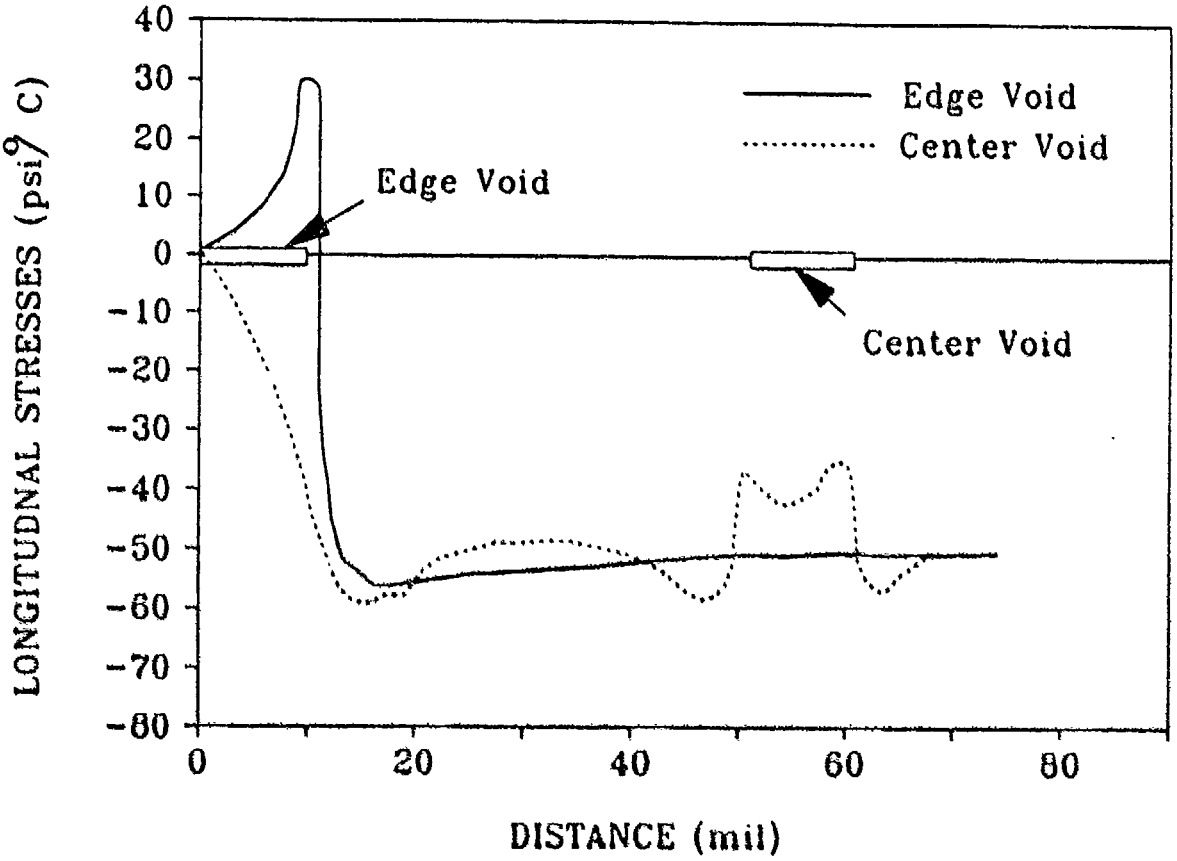


FIGURE G-10

VARIATIONS OF THE LONGITUDINAL TENSILE STRESSES, ALONG THE DIE ATTACH INTERFACE FOR THE SITUATIONS OF A 10 MIL EDGE AND A 10 MIL CENTER VOID

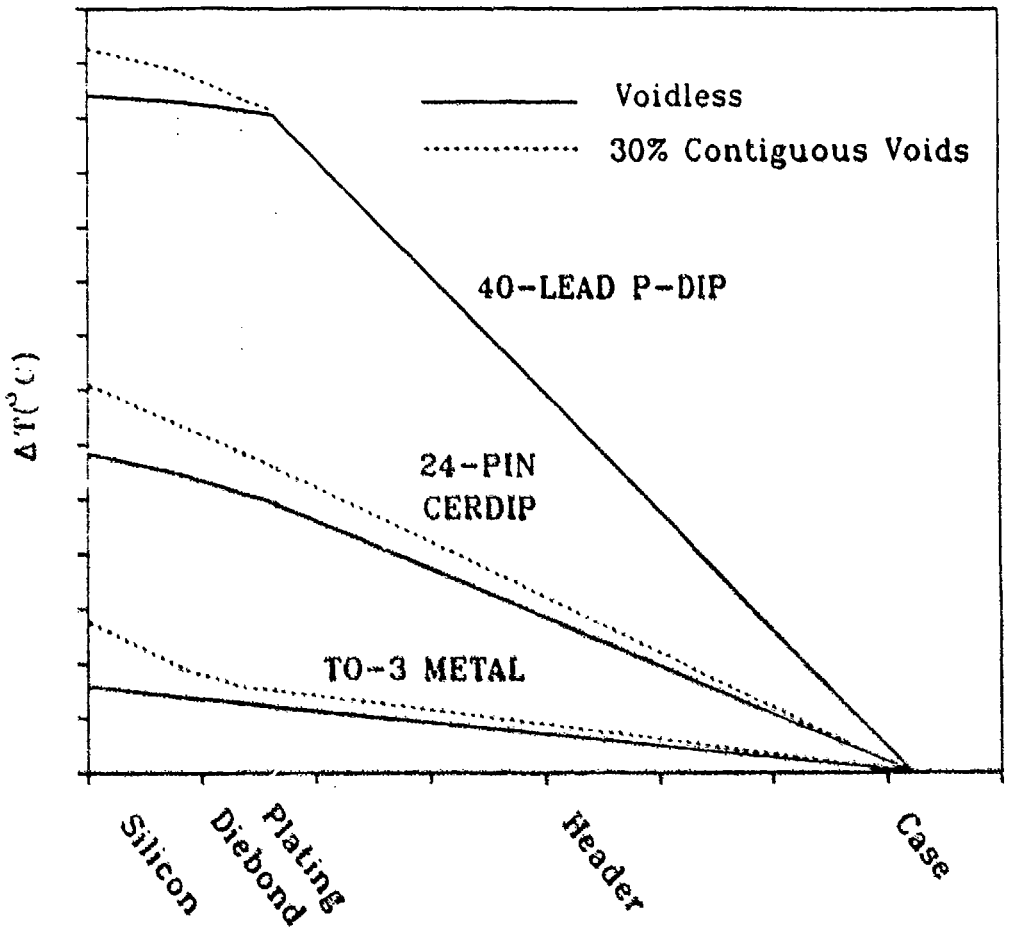
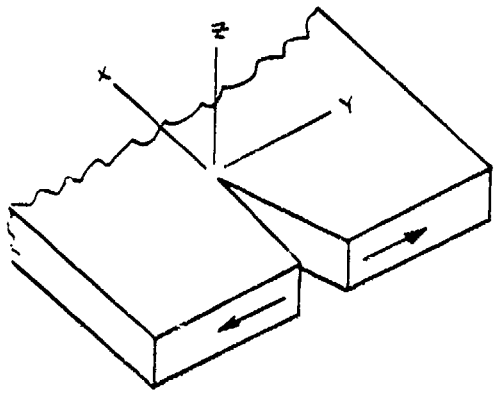
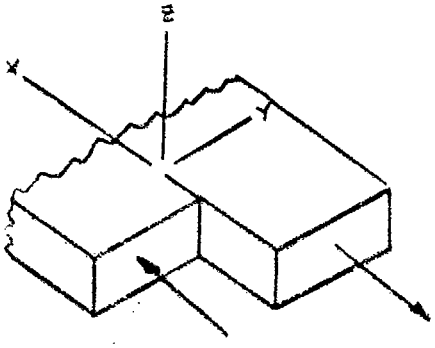


FIGURE G-11

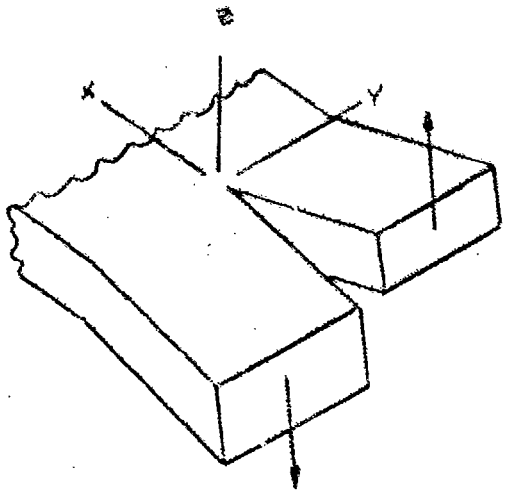
SCHEMATIC DIAGRAM SHOWING TEMPERATURE DROPS ACROSS THE SILICON CHIP, THE DIE BOND AND THE PACKAGE MATERIALS.



MODE I



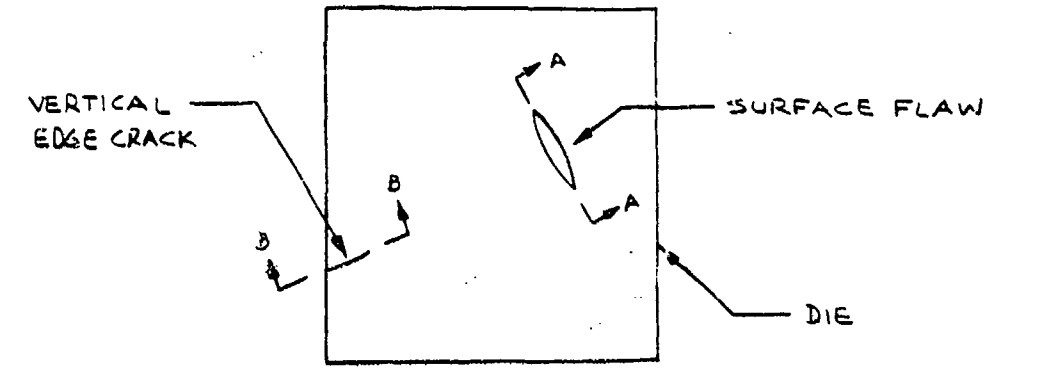
MODE II

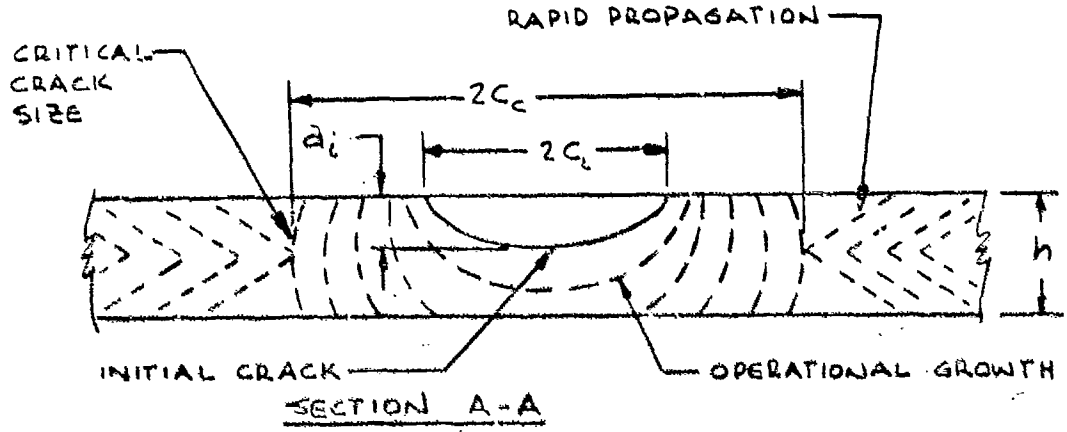


MODE III

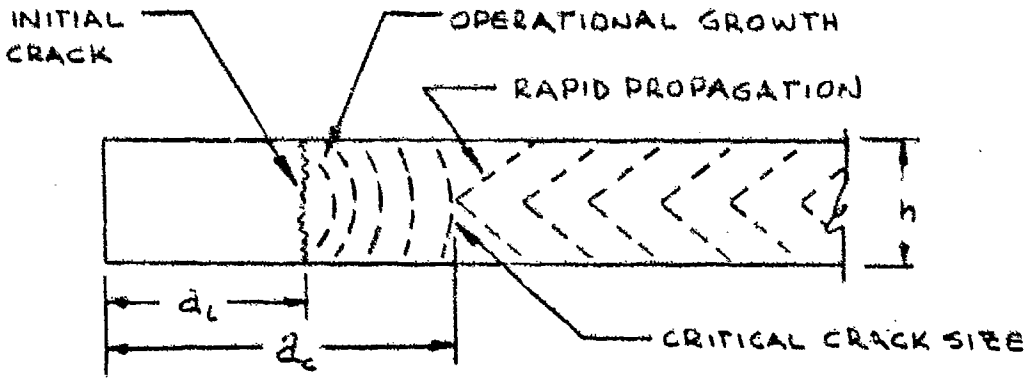
FIGURE G-13

BASIC CRACK SURFACE DISPLACEMENT MODES





SECTION A-A



SECTION B-B

FIGURE G-13

SCHEMATIC VIEW OF DIE CRACK GROWTH

APPENDIX H

CORROSION IN MICROELECTRONIC PACKAGES

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APPENDIX H

CORROSION IN MICROELECTRONIC PACKAGES

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H1. BACKGROUND

H1.1 Introduction

The corrosion failure mechanism has become more significant as component sizes have been miniaturized with increased functionality, higher component density and faster signal processing, resulting in smaller components with closer spacings and thinner metallic sections. With width, separations, and thicknesses of components measured in micrometers; even small amounts of corrosion can cause problems and device failure.

The presence of water, one of the necessary elements for corrosion, is often a consequence of the materials and processes used for packaging integrated circuits. Consequently, controlling the access of moisture to and ionic contamination of integrated circuit chips has been the chief means of minimizing corrosion as a circuit failure mode. Water vapor may be entrapped within the cavity of hermetic parts at sealing. It may also be released within the cavity by package materials after sealing. At a constant temperature, most hermetic package cavities will contain a moisture level in equilibrium with the cavity walls. Temperature excursions will shift the equilibrium. In particular, an extreme drop in temperature will cause the sealed cavity to attain its dew point, and condensation will form on the inner surfaces of the cavity.

In recent years there has been a rapid increase in the use of plastic encapsulated semiconductor devices. This is primarily because plastics serve as a rugged, durable and low-cost packaging material. However, most plastic molding compounds offer less resistance to moisture ingress from the outside environment than their hermetic counterparts.[1]

In the following sections, the corrosion mechanisms in microelectronic packages are modeled mathematically to provide the time to failure, τ, of the metallization and bond pad in a package. The results provide a prediction of the reliability of the package in actual operation.

H1.2 Corrosion In Microelectronic Packages

Corrosion is broadly defined as material deterioration caused by chemical or electro-chemical attack. Although direct chemical attack can occur with most materials, electro-chemical attack usually occurs only with metals. In microelectronic packages, the three most common forms of corrosion mechanisms are uniform, galvanic and pitting corrosion.

H1.2.1 Uniform Corrosion

Uniform corrosion is defined as a heterogeneous chemical reaction which occurs at a metal-electrolyte interface and involves the metal itself as one of the reactants. It occurs uniformly over the surface of a material. The process can either be time dependent or self limiting. If the reaction products are soluble, such as $Al(OH)_3$ or $Al(OH)_2Cl$, the corrosion process will continue linearly with time until all the materials are being corroded. If these products do not dissolve readily in the corrodant, the process becomes a self limiting phenomenon. Since the corrosion rate is proportional to the current which flows from anode to cathode via the electrolyte and if the corrosion products are electrically resistive and eventually the current magnitude decrease as the corrosion product film thickness increases. The corroded material is typically in the form of an oxide which adheres to the corrosion surface and acts as a protective layer to retard further corrosion from occurring. The rate of corrosion will depend upon the stability of this corroded layer. For example, aluminum oxide will protect aluminum from corrosion.

Most commonly, uniform attack occurs on metal surfaces which are homogeneous in chemical composition or which have homogeneous microstructure. The access of the corrosive environment to the metal surface must also be present.[2]

H1.2.2 Galvanic Corrosion

Electronic component design is unique in the wide variety of metals used

because of particular physical and electrical properties. Some of the more common metals and their uses in an electronic system are given in Table H-1.[17] These metals are combined to form a myriad of dissimilar metal couples in electronic equipment. In the presence of moisture, destructive galvanic corrosion can take place.

Galvanic corrosion can occur in metallization when dissimilar metals, such as, the molybdenum-gold system, or in aluminum metallizations with gold bond wire, are used. Corrosion occurs at exposed regions such as bonding pads and can proceed along the passivation-metal interface. An electrical potential difference will usually exist between two dissimilar metals exposed to a corrosive solution. When these two metals are electrically connected the more active metal will become the anode in the resulting corrosion cell, and its corrosion rate will be increased. The extent of this increase in corrosion will depend upon several factors. A high resistance in the electrical connection between the dissimilar metals will tend to decrease the rate of attack. On the other hand if a large area of the more noble metal is connected to a smaller specimen of the more active metal, attack of the more active metal will be greatly accelerated.

The conductivity of the corrosion medium will also affect both the rate and the distribution of galvanic attack. In solutions of high conductivity the corrosion of the more active alloy will be dispersed over a relatively large area. In solutions having a low conductivity, on the other hand, most of the galvanic attack will occur near the point of electrical contact between the dissimilar metals. This latter situation is usually the case, for example, under atmospheric corrosion conditions.[3]

H1.2.3 Pitting Corrosion

In pitting corrosion, attack is highly localized to specific areas which develop into pits. Active metals such as aluminum, as well as alloys which depend on Al-rich passive oxide films for resistance to corrosion are prone to this form of attack. These pits usually show well defined boundaries at the

surface, but pit growth can often change direction as penetration progresses. When solid corrosion products are produced, the actual corrosion cavity may be obscured but the phenomenon can still be recognized from the well defined nature of the corrosion product accumulations. Pitting corrosion is usually the result of localized, autocatalytic corrosion cell action. Thus, the corrosion conditions produced within the pit tend to accelerate the corrosion process. As an example of how such autocatalysis works, consider the pitting attack of aluminum in an oxygenated solution of sodium chloride. Assume that there exists a weak spot in the oxide film covering the aluminum surface so that the corrosion process initiates at this point. The local accumulation of Al^{3+} ions will lead to a local increase in acidity due to the hydrolysis of these ions. That is, the hydrolysis of aluminum ions gives as the overall anodic reaction:

$$Al + 3\ H_2O \Longrightarrow 3\ H^+ + Al(OH)_3 + 3\ e^+$$

If the cathodic oxygen reduction, which produces alkali, occurs at a region removed from this anodic reaction; the localized corrosion of the aluminum will produce an accumulation of acid. This acid destroys the protective oxide film and produces an increase in the rate of attack. In addition, the accumulation of a positive charge in solution will cause the migration of Cl^- ions to achieve solution neutrality. This increased Cl^- concentration can then further increase the rate of attack. This process is illustrated schematically in figure H-2.[37] Since the oxygen concentration within the pit is low, the cathodic oxygen-reduction reaction occurs at the mouth of the pit, thus limiting its lateral growth. In most cases pits tend to be randomly distributed and of varying depth and size.[4]

H1.3 Factors Affecting the Rate of Corrosion

There are several mechanisms by which a microelectronic package can be contaminated. Contaminants may be sealed within a microelectronic package depending on the properties of the structural materials and fabrication methodology. Contaminants can also permeate into a package according to the

permeability of the package. When corroding contaminants are coupled with the appropriate environmental conditions such as temperature and temperature cycling, moisture content, electrical bias (either applied or galvanic bias), and ionic contamination levels, corrosion occurs.

H1.3.1 Properties of the structural materials

The materials used to fabricate an electronic package will determine the inherent resistance of the package against corrosion, and its capability to minimize the moisture ingress rate and the amount of impurities which enter the package.

To minimize moisture access to the metallization layer in a package, a passivation layer is often applied. The passivation layer is frequently a glass, silicon nitride, silicon dioxide or other dielectric layer deposited onto the device surface. Plasma-deposited silicon nitride is used as a passivating layer because it is an effective barrier for alkali ions which may be left on the device surface after the final wash. However, silicon nitride can give rise to a change in the surface potential, which can introduce charge trapping and storage effects, and give rise to interface conduction due to the activation of traps. These effects can contribute to corrosion as well as contribute to device electrical performance degradation.[3]

Failures due to corrosion of the metallization are frequently associated with defects in the passivation, such as cracks and pinholes. These defects act as sites for the entrapment of contaminants or moisture which are instrumental in corrosion. The chemical vapor deposition (CVD) process deposits films which are in tensile stress, resulting in localized lifting or cracking of the passivating layer in regions of poor adhesion. This mechanism creates sites at which contaminants can penetrate to protected metallization patterns and initiate corrosive attack.

Aluminum, which is the most common interconnect material, has a stable oxide and is therefore self-passivating in the absence of ionic surface

contamination. In the presence of water combined with ionic contaminants such as sodium and chlorine, the oxide can be broken down and the aluminum attacked when an electrical bias is applied. The phosphorous content of the silicon dioxide layers used in the passivation is an important factor in the reliability of the devices. The phosphorous is added both to provide mechanical stability of the glass coating and as a getter for mobile sodium ions. However, too little phosphorus causes cracks in the passivation layer due to tensile stress of the film while too much phosphorus results in aluminum corrosion. Cracking of the passivation increases the susceptibility of the underlying aluminum to corrosion by impurities.

Die attach materials can affect the contaminant level in a package. When epoxies are used as adhesive, they can act as a source of ionic contamination since the epoxide resin itself is a mixture of hydrolizable chlorine, bromine and sodium.

Moisture, which is required for corrosion to occur, is often trapped in the cavity of a hermetically sealed microelectronic during the assembly process. Additionally, certain materials that are used in the microelectronic fabrication and assembly process inherently contain adsorbed moisture --- polymers used for the die attachments, gold plated surfaces, and even the plastic used for the package itself. Moisture can ingress a package by permeation through polymers used in the seals and the package material, or by leakage through cracks or small voids between the plastic material and lead frame in molded plastic packages. Furthermore moisture may induce crack growth in package materials, destroying the hermetic seal.[5]

H1.3.2 Fabrication Methodology

Fabrication methodologies affect the amount of contaminants inherent in the package, the potential for contaminant ingression, and the rate at which corrosive damage will lead to a failure.

Throughout the fabrication process, wafers are cleaned with various acids and

solvents. Like water, these chemicals contain other elements that function as contaminants to integrated circuits and thus impact wafer ecology. Wafers are also exposed to industrial and specialty gases at every process step. As dry processing becomes more prevalent, gases are now one of the major raw materials employed in the manufacture of microelectronic packages.

Another factor to consider during the fabrication process is the recontamination of baked out parts during handling. That is, properly baked out parts can be recontaminated by the re-exposure to moisture at ambient environment. Research[6] indicates that a dry surface will absorb many monolayers of moisture during exposure in less than one second. Therefore, baked out parts should be handled cautiously.

Soldering is a frequently used method in bonding the lid to the package. For high reliability applications, gold is preferred for soldering surfaces since it is more resistive to corrosion. It is usual to deposit a thin layer of gold onto both the lid and package using a plating technique. At the melting temperature, the solder melts and wets both surfaces to form the joint. When wetting occurs, sufficient solder volume must be available to compensate for manufacturing variations in lid and package flatness. Corners of domed lids and sealing edges are typical sites for out-of-flat build up.

Lid sealing process also affects the final moisture content of the package through the silicon used in the chip bonding eutectic.

The amount of silicon available is dependent on the temperature and duration of the sealing process. As the sealing time and, therefore, temperature increases, the amount of silicon diffused from the eutectic bond increases and the silicon produced will react with the water vapor to produce silicon oxide. Hence the level of moisture decreases.

H1.3.3 Permeability

Microelectronic packages are the exterior portions of the device which provide

protection to the internal die and a mating surface to the external circuitry. The permeability of a package determines the ingress rate of contaminants from the ambient environment.

The oxide coating and the seal structure are important in corrosion of the die. In particular, the oxide coating on the lead frame conductor must be sufficiently thick to allow a good chemical bond to the sealing glass, and second, the design of the seal and the residual stress present in the seal must be able to withstand the rigors of thermal shock.

Package enclosures are referred to as hermetic or non-hermetic, which relates to the package's ability to resist moisture intrusion. Hermetic packages are enclosed with inorganic moisture resistant material such as metal, glass and ceramic. Non-hermetic packages are made of organic materials such as plastics which are permeable to moisture. Plastic packages are typically molded from silicone, phenolic or epoxy. Due to their cost, plastic packages are very popular in recent years. However, they offer reduced resistance to ingress of moisture and are not acceptable for military application, but efforts are being made to improve their moisture protection characteristics.

In general, for a non-hermetic package, moisture ingress is dominated by permeation through the package body. For a hermetic package, moisture ingress is by leakage through defect induced leak paths in the lead and lid seal with insignificant diffusion through the housing material. The quantity of the permeated or leaked contaminants is dependent on the construction processes and materials.

The leakage of contaminants into a package is dependent on the leak rate of the package, assuming the package processing was proper. All packages leak at some rate, but a package is defined to be hermetic if its leak rate is less than a specified value. For military microelectronic packages this value ranges from $\leq 1 \times 10^{-8}$ atm cc/sec for package volume < 0.01 cc to $\leq 5 \times 10^{-7}$ atm cc/sec for package volume > 0.4 cc as defined in MIL-STD-883 method 1014. The leak rate is also dependent on the shape of the leak path.

In general, the leak rate decreases as the cross section decreases or as it becomes more elongated and the flow changes from viscous to molecular. Generally, leaks into packages arise due to stress cracks which have elongated rather than circular cross sections. The differential pressure of the leaking medium, and the properties of leaking medium, including viscosity, density, and molecular mean path will also affect the leak rate.

A fluid arrives at one side of a barrier material, such as a seal, and leaves at the other side by the following steps: (1) condensation on or adsorption by the membrane, (2) solution in the membrane, (3) diffusion, (4) dissolution, (5) evaporation or desorption from the membrane. All of these processes together make up permeation. Gases must go through all five steps; liquid are already condensed so that they only go through step 2, 3 and 4. Usually, though not always, step 3, diffusion, the process by which a fluid moves through a membrane, is rate controlling.[7] When the flow rate is different from the prediction, an argument invariably arises that permeation is not occurring, but leakage.

Permeation is a direct function of the partial pressure differential of the permeating species and to a lesser extent temperature changes. In the following sections, the contribution of moisture ingress will be mathematically modeled and interpreted to provide the platform for developing the time to failure (τ).

H1.3.3.1 Permeation

The ingress rate of the contaminants into a package can be expressed as a function of the partial pressure of the permeating species, and can be mathematically written as follows:

$$P(L,t) = P_1 + (P_0 - P_1)\, e^{-\left(\frac{\pi^2 D_p t}{4L^2}\right)} \qquad \text{(H1.1)}$$

where:

$P(L,t)$	is the inside partial pressure at time = t
P_1	is the outside partial pressure
P_o	is the initial inside partial pressure
Dp	is the permeation rate
L	is the wall thickness
t	is the time

The development of equation H1.1 from fundamental principles is given in Appendix H-1.

H1.3.3.2 Leakage

The sources of moisture in the hermetically sealed packages have been delineated in various papers [8],[9],[10] and may be categorized as follows: 1) adsorbed water due to poor bake-out procedures; 2) generated internally by decomposition, desorption, or devitrification of sealing glasses; and 3) penetration of cracks and/or faulty seals.[11]

A review of the fundamental gas flow equations[12] delineates three definable areas of flow regime for leakage flow; namely, viscous, transitional, and molecular. Each regime has its own equation (see Appendix H-2) describing the effects of the geometric considerations of the leak path along with various gas parameters. Among the three mechanisms, molecular flow is the dominant phenomenon since leakage pin-holes or tortuous capillaries have such small dimensions that, except for quite high pressure differentials, the mass transport will be controlled by wall collision rather than viscous drag.[7]

Assuming molecular flow, and an external partial pressure, P_1, of a gaseous species of molecular weight M, and a hermetic package possessing a leak rate Q_S equal to the maximum value allowed by its performance specification, the rate of ingress of the gaseous species into the package is

$$\text{Rate of Ingress} = \frac{P_1 \, Q_S}{P_a} \left(\frac{M_a}{M}\right)0.5 \qquad \text{(H1.2)}$$

where:

P_a is the atmospheric pressure

M_a is the molecular weight of the gas inside the package

The gaseous species which enters the package through the leak is also able to escape via the leak. For a partial pressure, P_o, inside the package, the rate of loss is

$$\text{Rate of Loss} = \frac{P_o \, Q_S}{P_a} \left(\frac{M_a}{M}\right)0.5 \qquad \text{(H1.3)}$$

By combining equation H1.2 and H1.3, the rate at which the gaseous species builds up inside the internal cavity is

$$V \frac{dP}{dt} = \frac{(P_1 - P_o) \, Q_S}{P_a} \left(\frac{M_a}{M}\right)0.5 \qquad \text{(H1.4)}$$

where V is the internal volume of the package. Solving the differential equation H1.4 for the internal partial pressure gives

$$P(t) = P_1 \left(1 - e^{-D_L t}\right) \qquad \text{(H1.5)}$$

where t is the duration of the exposure to the gaseous species, and

$$D_L = \frac{Q_S}{V \, P_a} \left(\frac{M_a}{M}\right)0.5 \qquad \text{(H1.6)}$$

is a leakage coefficient. It should be noted that from the time of fabrication, contamination of the package occurs, even though the device is not in operation or powered. Thus, the shelf life of the device cannot be ignored.

H1.3.4 Environmental Conditions

H1.3.4.1 Temperature and Temperature Cycling

The permeation and the corrosion rates are affected by the surrounding environment, and in particular, temperature combined with moisture is the most deteriorating. Chemical reaction rates are greatly enhanced at elevated temperature. Thus the rate of galvanic corrosion, when a liquid phase electrolyte is present, will increase accordingly due to a more rapid rate of electron transfer.

The primary components of the microelectronic package are the mold epoxy, lead frame, die, and die attach material. Each of these components has its own coefficient of thermal expansion, which determines how great the expansion or contraction of the material will be in response to changes in temperature. Large differences or mismatches in expansion coefficient between components can increase susceptibility of a given device to cracking initiated at the region of maximum stress under thermal cycling.

A microelectronic package undergoes numerous duty cycles in its life and the application and removal of power will subject the package to thermal cycling. This temperature fluctuation will also influence the actual duration of the corrosion process. For example, when a non-operating sealed package is exposed to a temperature below the dew point, the moisture inside the package will condense and the liquid combines with any ionic contaminant present which will provide a conductive path for an electrical leakage path between adjacent metallic conductors. When the package is operating, the heat dissipated by the chip will elevate the temperature inside to above the dew point, consequently the electrolyte will evaporate to the vapor phase and will no longer permit leakage between conductors.

H1.3.4.2 Humidity

Humidity, one of the necessary elements for corrosion to occur, is the largest single risk factor concerning reliability and expected life of the device.[13] Moisture ingress occurs through leak paths in the lid and lead seal resulting from cracks or flaws and by permeation through organic

encapsulant. Flaws result from manufacturing process deviations as well as mechanical and thermally induced stresses.

H1.3.4.3 Electrical bias

When sufficient moisture is present to act as an electrolyte and a bias is applied, ions are carried to the anode or cathode (depending on the electrical charge of the impurities involved). The bias may simply be the varying voltage levels on different conductors caused by normal operation of the integrated circuits, or a galvanic bias may be present.

Corrosion kinetics greatly depends on the applied bias as shown in figure H-3 which gives the corrosion rate versus the applied voltage for epoxy encapsulated chips.[42]

H1.3.4.4 Ionic contamination

Studies[43] have shown that parts per billion levels of selected pollutants are sufficient under proper conditions of temperature and humidity to accelerate corrosion reactions in electronic equipment. Corrosion can occur during manufacturing, storage, shipping and service. Moisture and corrosive agents such as chlorides, fluorides, hydrogen sulfide, sulfur dioxide, nitrogen compounds such as ammonia, and other airborne contaminants are the major culprits.[44] Sources of chlorine ions in a package include the chlorine-based dry etches used for microcircuit metallization, or if epoxy is used in the package, the outgassing of the surrounding epoxy. Sodium ions can be produced from the epoxy or glass used in the package.

In decreasing order of importance, the three sources for the ionic contaminants that may reside on the chip of hermetically sealed devices are [33].

1) Die-handling operations post fabrication and pre-sealing. The chip has its highest vulnerability to uncontrolled environment during mechanical

and human handling.

2) Wafer fabrication. The environment is clean, but inadequate cleaning and rinsing of slices can leave contaminants.

3) Package hermeticity failure, allowing the ingress of ions from external sources along with moisture. During subsystem and system assembly, many parts receive detergent washes and/or conformal coatings at the board level. Many of these materials are notorious sources of both positive and negative ions.

One of the standard methods of cooling an electronic enclosure is the use of forced ventilation, with air generally drawn from the surrounding atmosphere. In sites with aggressive atmospheres, this type of cooling will greatly accelerate corrosion because the circulating contaminated air comes in intimate contact with sensitive electronics. Unless the outside environment is benign, the introduction of outside air into an electronic equipment cabinet should be controlled.

Ionic contamination accelerates the corrosion process. Figure H-4 gives a comparison of the corrosion results of unencapsulated chips between chips doped with 10 ppm NaCl and cleaned test chips. The mean time between failure (MTBF) of 50 hours for the doped chips compares poorly to 850 hours for the undoped chips, indicating the strong effect of a small concentration of mobile impurities.[42]

H2. DEVELOPMENT OF THE FAILURE RATE MODEL FOR CORROSION

H2.1 General Model For Corrosion Failure

Three major failure sites in a microelectronic package are identified in 4.5.1, viz: the wire bond, the die and die attach, and the metallization. An accelerated test was performed at 85°C/85% RH with encapsulated packages and the percentage failure was reported[15] and is shown in figure H-5. The reliability of the package in a corrosive environment was then plotted and best fitted with a Weibull curve as shown in figure H-6. The failure rate was also calculated using the Weibull model (figure H-7) which indicated that the

failure mechanism is an increasing function of time, thus is a wear out phenomenon.

The time to failure (τ) of a component due to corrosion can be modeled as the sum of the induction time and the time for the corrosion process to deplete bond pad metallization or segments or conductor metallization. Induction time is an indication of time required for moisture to penetrate the package and for initiation of the corrosion process. Mathematically,

$$\tau = \tau_1 + \tau_2 \qquad \text{(H2.1)}$$

where:

τ is the time to failure

τ_1 is the induction time to reach the threshold moisture content

τ_2 is the time for completion of the corrosion process

Figure H-8 delineates τ_1 for a hermetic package as a function of the package volume and the allowable leak rate from MIL-STD-883, Method 1011, Table II, which provides the following data:

Volume $< 0.01\ cm^3$, Allowable leak rate $\leq 1 \times 10^{-8}$ atm cc/sec
$0.01\ cm^3 \leq$ Volume $\leq 0.4\ cm^3$, Allowable leak rate $\leq 5 \times 10^{-8}$ atm cc/sec
Volume $> 0.4 cm^3$, Allowable leak rate $\leq 5 \times 10^{-7}$ atm cc/sec

From Figure H-8 it is seen that as the leak rate increases, $\tau_{1(hermetic)}$ approaches zero. Hence, if a microcircuit is subjected to environmental or handling stresses before installation which cause a latent flaw to develop into a leak, such as failure of a lid seal, then $\tau_{1(hermetic)}$ will decrease and

$$\tau_2 >>> \tau_1$$

Under this circumstance

$$\tau_2 \simeq \tau_2 \qquad \text{(H2.1a)}$$

Typically, for any type of package, the time required for the corrosion process to culminate in a falure far exceeds the moisture induction time, and

$$\tau_2 > 10\ \tau_1$$

Therefore, equation H2.1a effectively approximates the total time to corrosion failure. Evaluation of τ_2 is useful for comparison of competing packaging materials and package designs.

H2.2 Moisture Induction Time Model

The time for the corrosion process varies between different mechanisms and sites while the time to reach the threshold moisture content depends only on the package type.

To determine the induction time for a hermetic package, the internal volume and maximum allowable leak rate of the package have to be defined. With these two package parameters defined, $\tau_{1\ \text{hermetic}}$ can be read directly from figure H-8.

For a nonhermetic package, the permeability rate, Table 4.5-18, and effective thickness, figure H-9, of the package have to be identified. The time for the internal partial pressure of a package to reach 95% of the external partial pressure is derived in Appendix H-1 (equation H4.35). The induction time for a nonhermetic package is governed by the following equation:

$$\tau_{1\text{nonhermetic}} = \frac{12L^2}{\pi^2 D} \qquad \text{(H2.2)}$$

where:

L is the effective thickness of the package (cm)

D is the permeability rate of the encapsulant material, cm^3-cm/cm^2-sec-bar

Uhlig[16] states that a critical relative humidity exists, below which corrosion is negligible. Koelmans[20] presented data that shows a drastic reduction in surface conductivity, as a function of RH, takes place at about 5% RH. It appears that the condensed film must reach a critical thickness in order to dissolve contaminants and support ionic conduction. The absolute minimum of moisture has been described as three monolayers of condensed or adsorbed water molecules.[32] Table H-2 summarizes the amount of internal water vapor that could result in three monolayer coverage. Figure H-10[33] shows the same information graphically with a comparison to the allowed leakage rate from MIL-STD-883. Note that the larger the internal volume, the less moisture is required to produce the three monolayers. This is because with the decreasing area-to-volume ratio, there is less package surface area competing for water molecules, and thus the more likely they are to reside on the chip.

After the critical moisture content is reached inside a package, corrosion will take place once the inside temperature is dropped below the saturation temperature for the moisture to condense to form a liquid electrolyte with other ionic contaminants. Therefore, the inside temperature functions as a "switch" to activate or deactivate the corrosion process. The temperature activation function, $f^*(T)$, has a value of 0 when the inside temperature is above saturation temperature or below the freezing point, and has a value of 1 when the inside temperature is below saturation temperature and above freezing. Hence, the function can be expressed as:

$$f^*(T) = \begin{cases} 0 & \begin{cases} T_{inside} > T_{saturation} \\ T_{inside} < T_{freezing} \end{cases} \\ 1 & T_{freezing} < T_{inside} < T_{saturation} \end{cases} \quad \text{(H2.3)}$$

H3. APPLICATION OF THE CORROSION FAILURE RATE MODEL

H3.1 Metallization Corrosion

Corrosion is a potential failure mechanism in electronic modules because of inherent susceptibility of the metal conductor lines. To reduce the occurrence of corrosion in the metallization, a passivation layer is applied

to protect it from contact with the environment. The ideal protective coating serves to prevent formation of the moisture film. It should form high energy bonds with the substrate which cannot be broken by moisture adsorption within the coating or by thermomechanically induced shear stress at the coating-substrate interface. It should have a low solubility for water to suppress conductivity in the film itself and have a low sorption coefficient. The passivation should also be chemically stable. However, defects on the passivation layer will promote pitting corrosion and eventually lead to a corrosion failure as shown in figure H-11. For metallization without the passivation layer, a mathematical model can be developed by using Faraday's and Ohm's laws, following the work of Howard.[22]

H3.1.1 Model for metallization failure due to corrosion

Given the conditions shown in figure H-12, corrosion at the anode will proceed until a length of the electrode, approximately equal to its width, is corroded to an open condition. Dendritic growth (electrochemical metal migration from the cathode to the anode), which can cause shorts between conductors, is often an accompanying effect of corrosion. Steppan, et. al.[48] reviewed numerous studies initiated to understand and model dendritic growth and described the numerous conditions that contribute to this phenomenon. Zamanzadeh, et. al.[49] compared theoretical predictions with experimental observations and found differences in dendritic growth rates of several orders of magnitude between the predictions and observations. Dendritic growth has not been considered in this model due to its relative infrequency as a cause of catastrophic failure in microelectronic devices and the difficulty in accurately modeling its mechanism. Initially, the leakage current is given by

$$I = \frac{V}{R} = \frac{V}{\rho S/A} \qquad \text{(H3.1)}$$

where A is the cross section of the current path through the electrolyte
S is the separation of conductors connected by the electrolyte

Therefore,

$$A = Lt \tag{H3.2}$$

and t is the electrolyte thickness (centimeters) in the direction parallel to conductor length

L is the length of the conductor edge exposed to the electrolyte and perpendicular to S:

$$\text{then} \qquad i = \frac{VL}{(\rho/t)S} \tag{H3.3}$$

The term ρ/t is the sheet resistance of the electrolyte. The number of squares is given by S/L and can be quite low. The current is thus summed over S/L parallel paths of which the unit current is given by

$$i_j = \frac{V}{(\rho/t)} \tag{H3.4}$$

Thus if the surface resistivity is lowered due to a higher ionic concentration, or if the potential field is increased, a dominant local corrosion will occur. The quantity of material corroded is given by Faraday's Law:

$$\frac{w^2hndF}{M} = \int_\tau i_j \, d\tau = \frac{V\tau}{\rho/t} \tag{H3.5}$$

where M is the atomic weight of the metal conductor and d is its density in gm/cm^3, n is the chemical valence, F is Faraday's constant, 96500 coulombs/mol, and w and h are width and height of the conductor in cm respectively. The time to failure, in seconds, is therefore

$$\tau = \frac{w^2hndF}{MV\, f^*(T)} \left(\frac{\rho}{t} \right) = \text{constant} \times \frac{\rho}{\tau\, f^*(T)} \tag{H3.6}$$

The constant is dependent entirely upon the geometry and composition of the corroding electrode, and it can be calculated from design parameters. The time to failure τ is clearly dependent on the sheet resistivity and thickness of the electrolyte and the value of the function $f^*(T)$, as defined

in equation H2.3. Since this function is discontinuous, the evaluation of τ is facilitated by replacing this function with a continuous equipment operating time factor defined as follows:

$$k_3 = \frac{24}{24-\tau^*} \qquad \text{(H3.7)}$$

where τ^* is the number of equipment operating hours per day. When the equipment is energized, the power dissipated in each microelectronic device is transformed to heat which will raise the package inside temperature aboe the saturation temperature. The liquid electrolyte which supports the ion transfer necessary for the corrosion process to continue will evaporate, and the corrosion process will become inactive.

As discussed in paragraph H2.3, it has been postulated that the minimum water film thickness required to provide the ion mobility necessary to support electrochemical corrosion is 3 monolayers of water molecules. A water molecule can be considered to be enclosed by a rectangular prism wth a base of 2.08 x 1.32 angstroms and a height of 1.53 angstroms. Hence a 3 monolayer film thickness can be considered to be approximately 6 angstroms thick (6 x 10^{-8} cm). However, Der Marderosian[37] has reported that a 3 monolayer film thickness is 1.2 x 10^{-7} cm. It is conservative to use this value for τ in equation H3.6.

From the above considerations, the following metallization corrosion model is derived:

$$\tau^2_m = 8 \times 10^{11} \; \frac{k_1 k_2 k_3}{k_4} \; \frac{w^2 h n d \rho}{MV} \qquad \text{(H3.8)}$$

where:

τ_{2m} is the time to failure, seconds

k_1 is the physical properties index of the material, Table 4.5-12

k_2 is the coating integrity factor, Table 4.5-13

k_3 is the operating time factor, Table 4.5-14

k_4 is the temperature-humidity environment acceleration factor, figure 4.5-1

w is the width of the metal conductor (cm)

h is the height of the metal conductor (cm)

n is the chemical valence of the material, Table 4.5-12

d is the density of the material (g/cc), Table 4.5-12

M is the atomic weight of the metal conductor, Table 4.5-12

V is the voltage bias, volts (see Appendix H-4)

ρ is the resistivity of the electrolyte (ohm-cm), Table 4.5-15

The metallization corrosion model was developed based on gold bond pads without protection at 85°C/ 85 RH for a continuous corrosion process. To compensate for condition restraints, four correction factors are introduced. The physical properties index, k_1, is a corrosion resistance factor. Since aluminum corrodes ten times faster than gold,[13] k_1 is 0.1 for aluminum and 1 for gold.

The coating integrity factor k_2 accounts for the existence and integrity of a passivation layer covering the metallization on a microcircuit die. Sbar[45] has experimentally demonstrated that a void and pin hole free completely bonded passivation layer will reduce the metallization corrosion rate by 2 to 3 orders of magnitude. This suggests that a value of $k_2 = 1$ can be assigned to unpassivated metallization, indicating that under this condition, corrosion proceeds without inhibition. A conservative value of $k_2 = 100$ can be assigned to represent a defect free, completely bonded passivation layer. Between these two limits, k_2 can assume values varying from 10 to 50 to account for varying defect levels. For conservatism, a default value of 10 can be assigned when a passivation layer exists and the defect level is unknown. Further investigation should be conducted to develop definitions for passivation layer defect types and magnitudes and associated values for k_2 between the two limits.

The temperature-humidity environment acceleration factor, k_4, is required to determine the time to failure for conditions other than 85°C/85 RH.

Many temperature-humidity correlation relationships have been proposed. [24 to 28] Peck[29] evaluated these previous models and proposed a modified Arrhenius model based on analysis of published data from 61 tests conducted over the period from 1970 to 1985. He subsequently discarded the less reliable data prior to 1979 and evaluated new data.[30, 47] He proposed the following acceleration model based on over 90 tests:

$$k_4 = \frac{(RH_1)^n \exp (Ea/kT_1)}{(RH_2)^n \exp (Ea/kT_2)} \qquad \text{(H3.9)}$$

where RH is test chamber relative humidity, percent
Ea is activation energy, electron volts
k is Boltzman's constant, eV/°K
T is test chamber temperature, °K

Peck found that n = -3.0 and Ea = 0.90 eV provided excellent correlation between the test data and the predicted acceleration factor over the range of 25% < RH < 100% and T $\leq$ 150C. Prior to applying equation H3.9, it is necessary to assure that the glass transition temperature (Tg) of the encapsulant is not less than 150C. By using RH_1 = 85% and T_1 = 85C, the following relationship is obtained:

$$k_4 = \frac{7.6 \times 10^6}{(RH)^{-3} \exp (10444/(T + 273)} \qquad \text{(H3.9a)}$$

where T is in °C.

This equation is plotted as figure 4.5-1.

The resistivity of the electrolyte, ρ, is calculated based on the amount of contaminants in average indoor environment across the country as discussed in Appendix H-3.

H3.2 Bond Pad Corrosion

Recent advances in device passivation technology have resulted in protective films of high integrity and moisture imperviance. The use of these films on integrated circuits has greatly reduced the corrosion of aluminum conductors when these devices are placed on temperature, humidity, and bias stress. However, for microelectronic devices which incorporate wire bonding, the aluminum bond pads remain unpassivated and consequently are exposed to the packaging environment.[23]

Figure H-13 is taken from reference[23] and depicts a typical bond pad structure where the edges of the pad and the remainder of the chip are protected by a multi-layer passivation structure.

Bond pad corrosion can be considered to be principally due to three separate mechanisms:

(1) chemical corrosion due to phosphoric acid formation from P_2O_5 leached from phosphosilicate glass passivation by liquid phase moisture.[35, 36]

(2) electrolytic corrosion due to current leakage across a wetted surface between adjacent bond pads having different applied electrical potential.[14, 34]

(3) galvanic corrosion due to the galvanic potential difference between dissimilar bond wire and bond pad metals, as discussed in Appendix H-4.[23]

Mechanism (1) results in open circuit failure and can be minimized by appropriate choice of passivation materials, and will not be considered further in this study. Mechanism (2) will most likely result in microcircuit performance degradation before significant corrosion can develop. However, to assure conservatism in the corrosion model, this mechanism is considered in Appendix H-4 when choosing the appropriate bias voltage magnitude. Mechanism (3) also results in open circuit failure and requires corrosion of a finite

volume of bond wire or bond pad material as discussed in Appendix H-5.

The process whereby contaminants can enter along the plastic/lead frame interface is discussed in reference[23] and is depicted in figure H-14. The interface gap is shown enlarged for clarity. The effects of temperature, humidity, bias and perhaps capillary action can cause the migration of these contaminants along the interface to the bond wire. As this occurs, the chloride ions and moisture can corrode the bare metal, with iron and nickel ions being dissolved. These ions can then travel along with the water/chloride contamination to the bond wire, up the wire and eventually reach the aluminum bond pad, whereby corrosion of the pad can proceed.

The corrosion chemistry of aluminum is basically a four step process that can be summarized as follows[41]:

1) Adsorption of an aggressive anion (Cl^-) on to the protective anodic aluminum oxide film
2) Chemical reaction of Cl^- with Al^{3+} in the oxide lattice
   $Al^{3+} + 2\ OH^- + Cl^- \Rightarrow Al(OH)_2Cl$
3) Thinning of the oxide by electro-chemical dissolution
4) Direct attack of exposed Al by Cl^- ions:
   $Al^{3+} + 4\ Cl^- \Rightarrow AlCl_4^-$
   $AlCl_4^- + 2\ H_2O \Rightarrow Al(OH)_2Cl + 2\ H^+ + 3\ Cl^-$

As can be seen from the last equation, chloride ions are both a reactant and a product during this process. As such, once the chlorine ions participate in the corrosion of aluminum, they are "re-cycled" and can start the process all over again. The implication is that a small amount of chloride ions can consume a much larger amount of aluminum.

H3.2.1 Model for Bond Pad Failure Due to Corrosion

Equation H3.8 for metallization corrosion can be applied to bond pad corrosion by replacing the metallization corrosion volume by the bond pad corrosion

volume. Appendix H-5 discusses the evaluation of the bond pad corrosion volume and provides the following conclusions:

(1) When the bond pad is anodic to the bond wire in a dissimilar metal coupling:

$$V_c = 0.3\ s^2 t_b \qquad \text{(H-8a)}$$

where s = bond pad size, cm (for a square pad)
t_b = bond pad thickness, cm

(2) When the bond wire is anodic to the bond pad in a dissimilar metal coupling:

a) for a wedge or crescent bond:

$$V_c = 0.236\ D^3 \qquad \text{(H-8b)}$$

where D = bond wire diameter, cm

b) for a ball bond:

$$V_c = 3.77\ D^3 \qquad \text{(H-8c)}$$

c) for unknown bond type use equation H-8b.

3) When the bond wire and bond pad are made from similar materials, use the smaller of equations H-8a and H-8b.

Then equation H3.8 can be rewritten for bond pad corrosion by replacing the terms w^2h with V_c, as follows:

$$\tau^2 w = 8 \times 10^{11} \frac{k_1 k_2 k_3}{k_4} \frac{V_c n d \rho}{MV} \qquad \text{(H3.10)}$$

where:

τ_{2w} is the time to failure, seconds

k_1 is the physical properties index of the anodic, member of the bond pad-bond wire combination, Table 4.5-12

k_2 is the coating integrity factor, table 4.5-13

k_3 is the operating time factor, Table 4.5-14

k_4 is the temperature-humidity environment acceleration factor, figure 4.5-1

V_c is the corrosion volume as discussed in Appendix H-5 and summarized above, cm^3

n is the chemical valence of the anodic member of the bond pad-bond wire combination, Table 4.5-12

d is the density of the anodic member of the bond pad-bond wire combination, Table 4.5-12

M is the atomic weight of the anodic member of the bond pad-bond wire combination, Table 4.5-12

V is the voltage bias, volts (see Appendix H-4)

ρ is the resistivity of the electrolyte, ohm-cm, Table 4.5-15

Note: When the bond pad and bond wire are made from similar materials, the choice of values for k_1, n, d and M is obvious and V_c is chosen as discussed in (3) above.

H4. SUMMARY

Performance over time is key to the reliability of the package and must be predictable to aid in design and trade off studies. The time to failure of different sites in a package due to corrosion was mathematically modeled. The result can be used either to determine the reliability of the package, improve proposed designs or to function as a guide line for maintenance.

The models were developed based on fundamental concepts and validated with existing experimental data. However, more extent experiments are required to further improve the accuracy of the models by reducing the assumptions taken during the model development.

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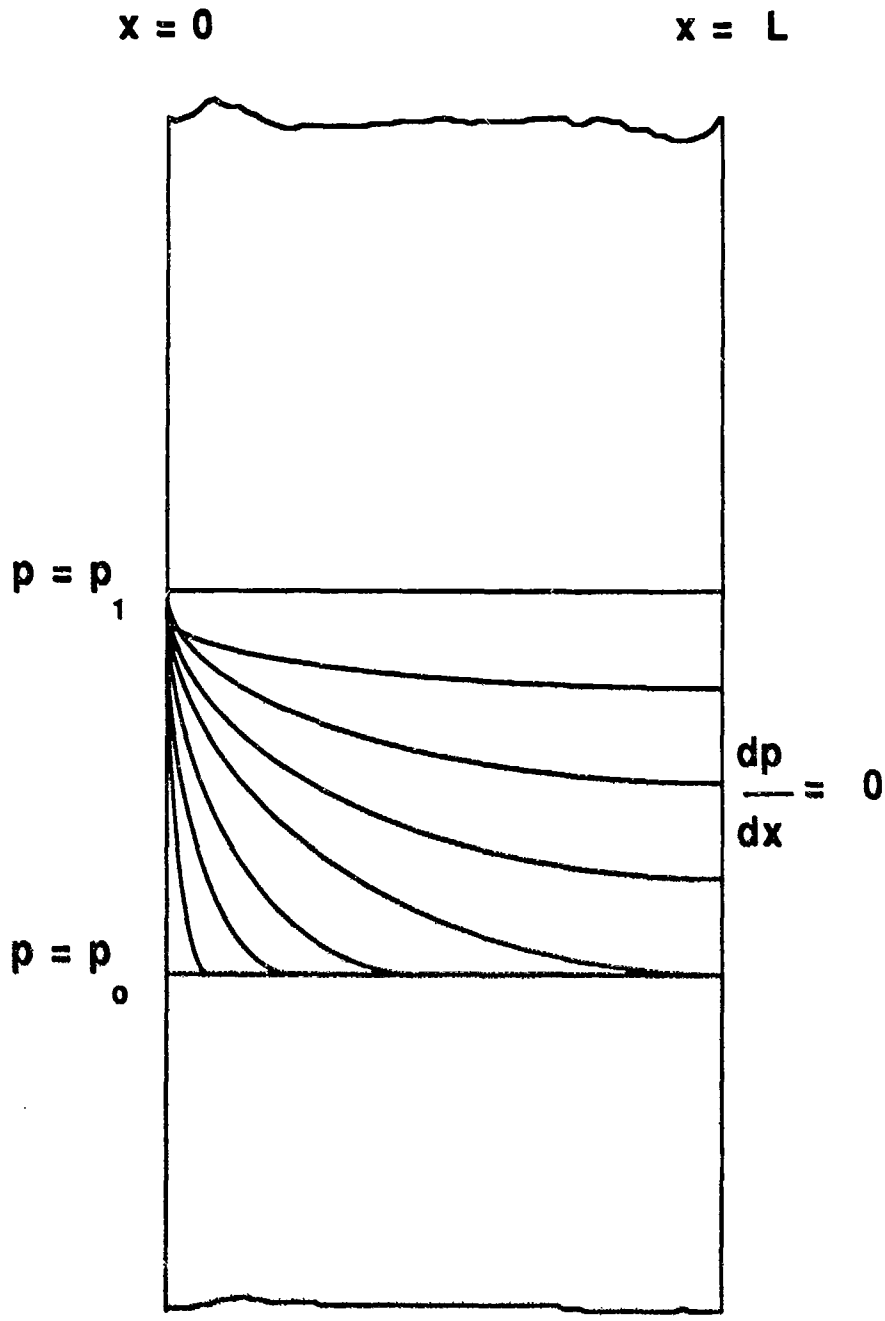


FIGURE H-1

DIFFUSION PRESSURE GRADIENTS ACROSS A BARRIER

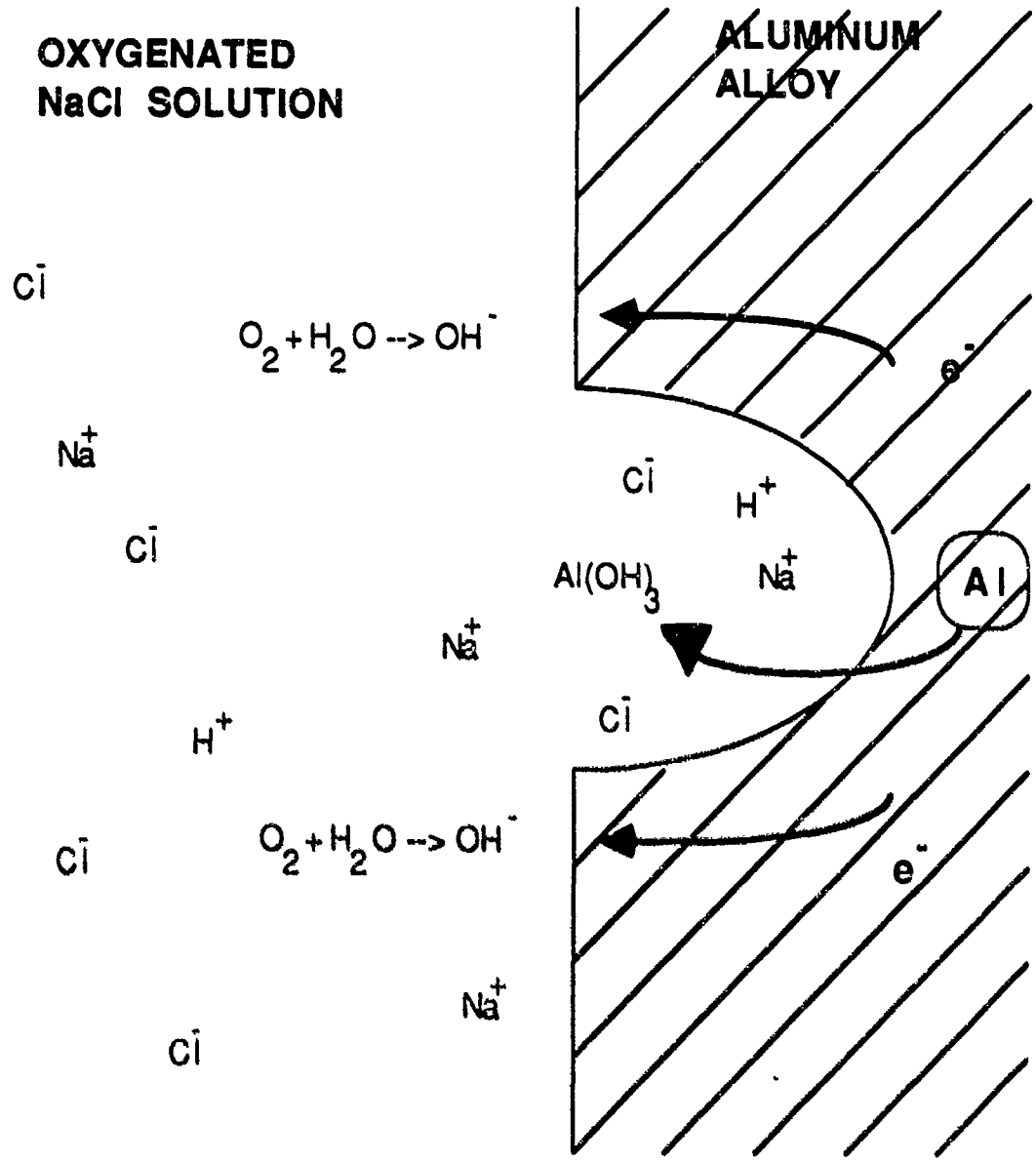


FIGURE H-2

Schematic drawing illustrating the autocatalytic nature of pitting attack on aluminum in oxygenated sodium chloride solution

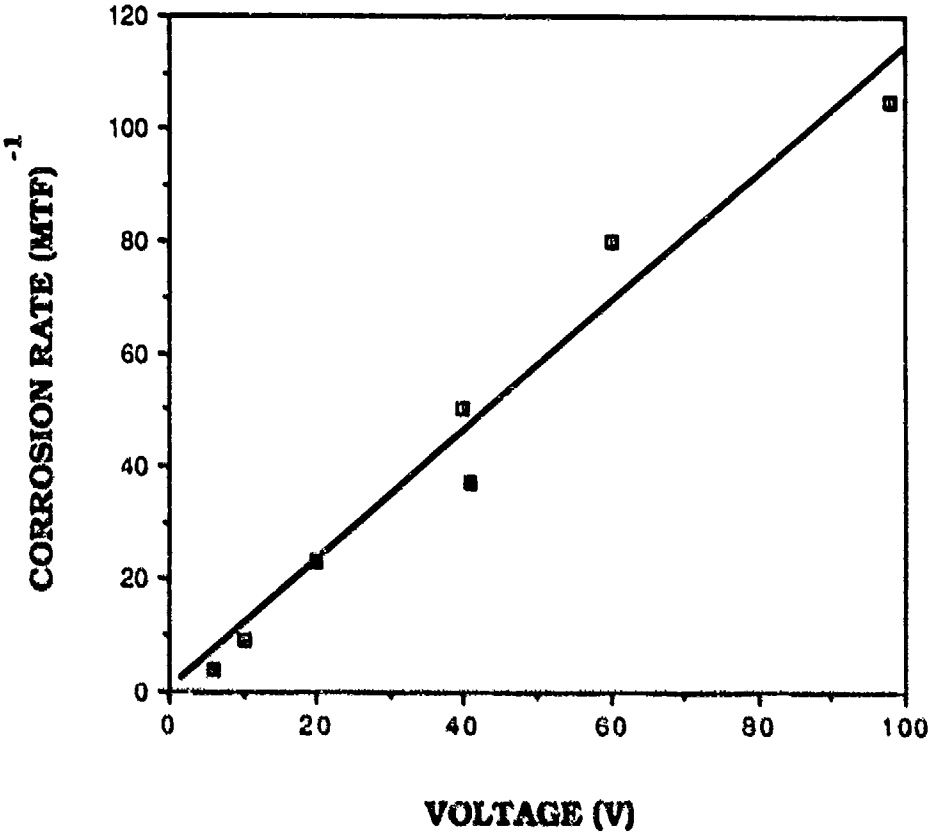


FIGURE H-3

Corrosion Rate Versus Voltage For Epoxy Encapsulated Devices

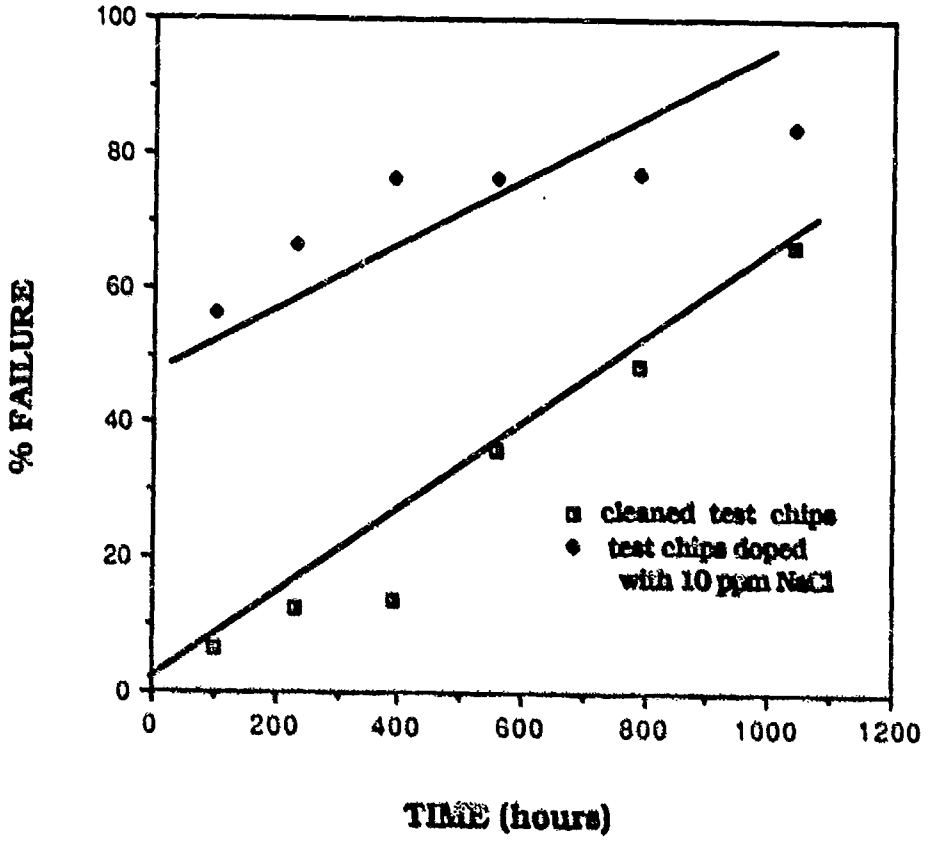


FIGURE H-4

Influence of Ionic Contamination on the Corrosion Result

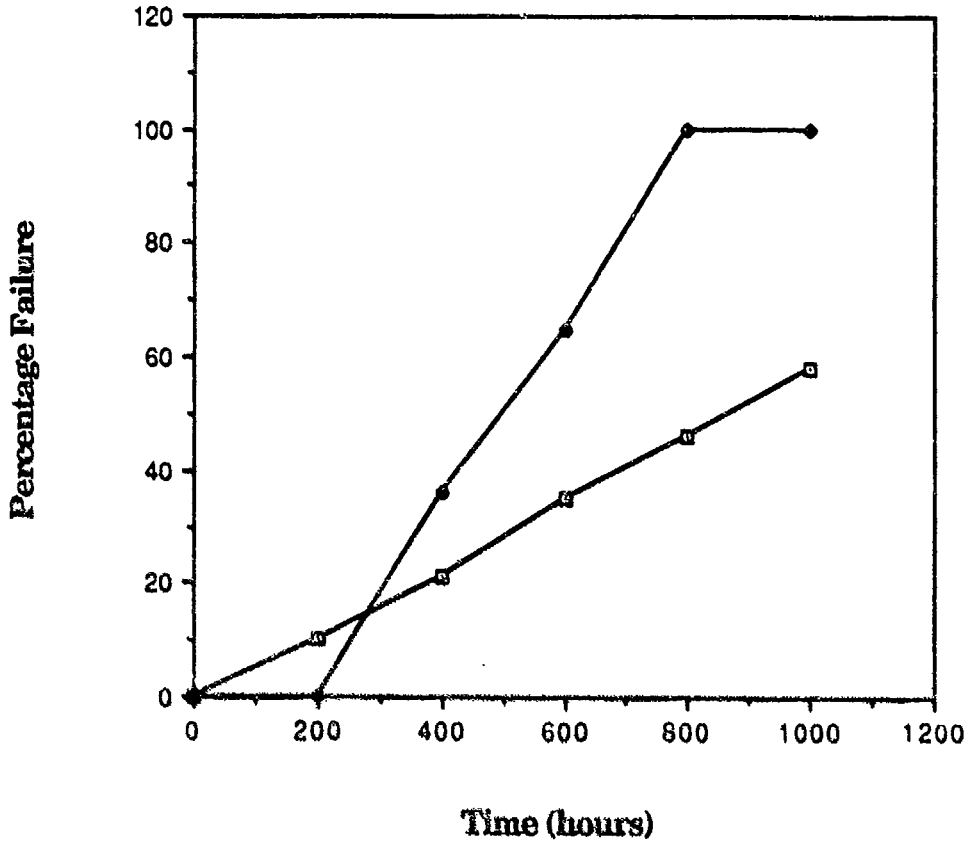


FIGURE H-5

Percentage Failure of Encapsulated and Unencapsulated Packages Under Corrosion

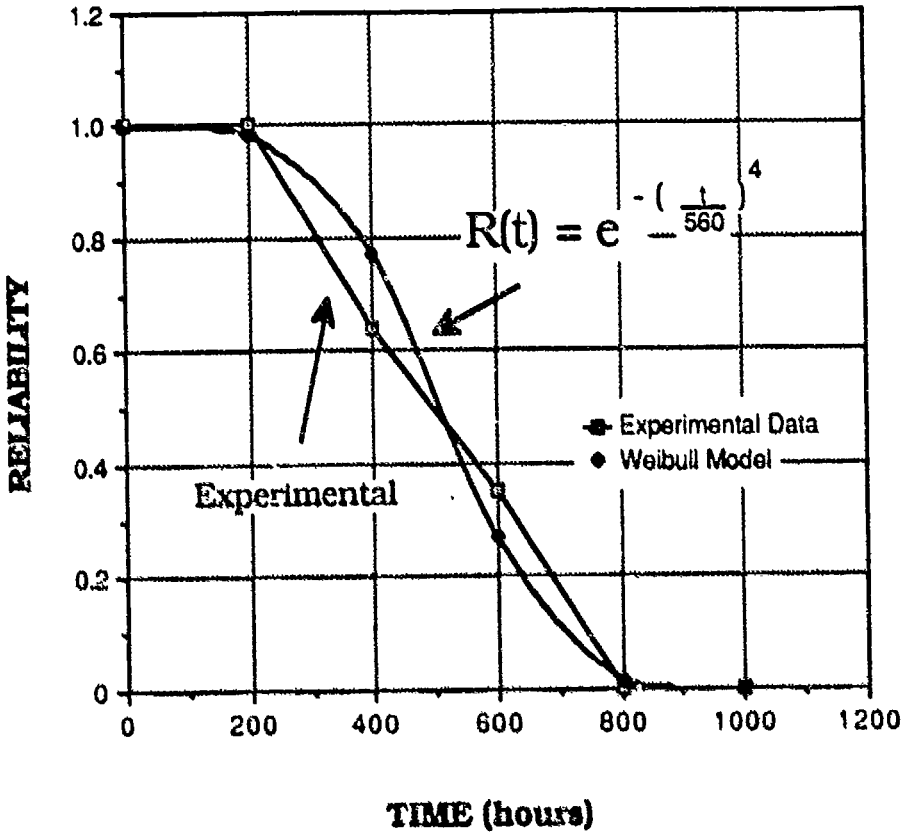


FIGURE H-6

Reliability of Encapsulated Package in a Corrosive Environment

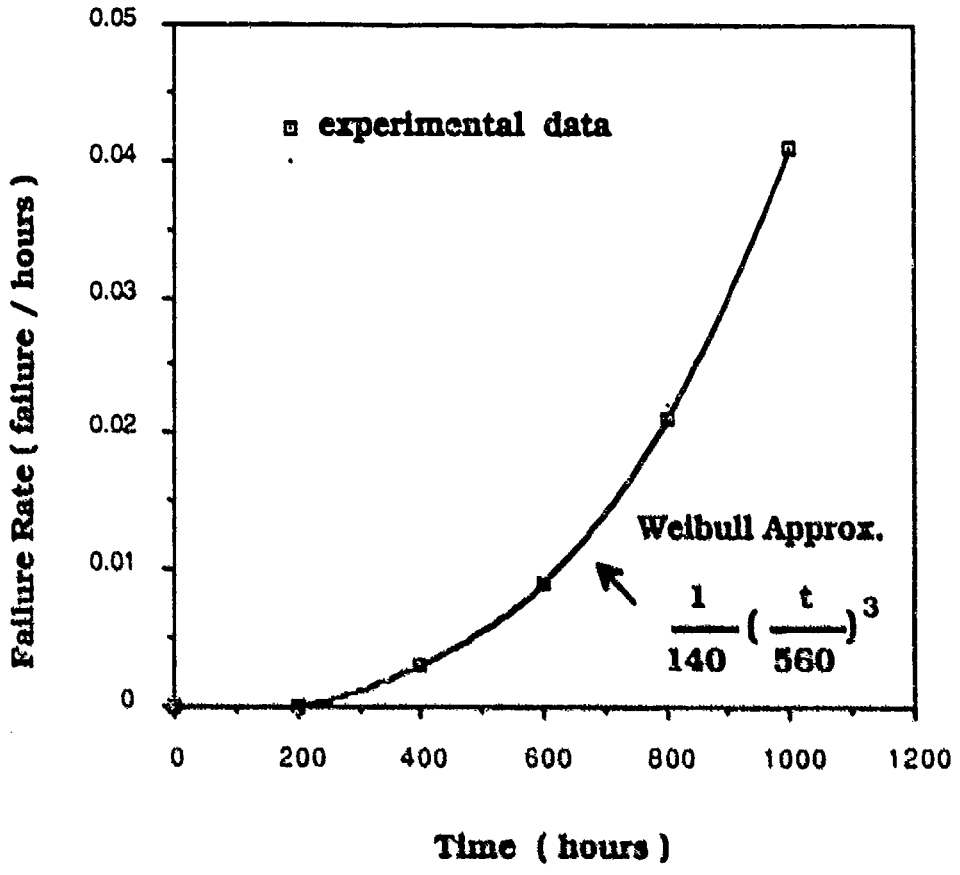


FIGURE H-7

Failure Rate of Encapsulated Package in a Corrosive Environment

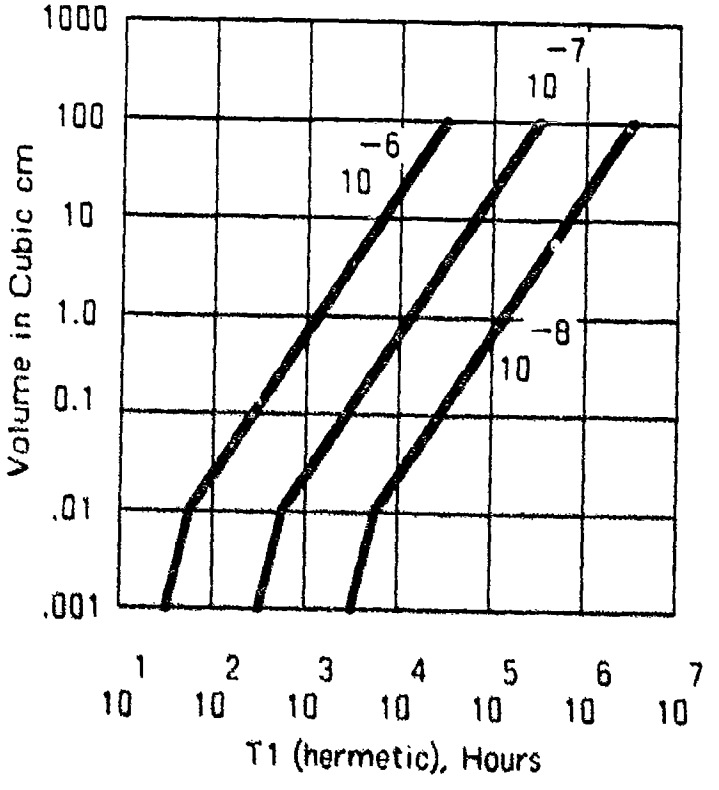
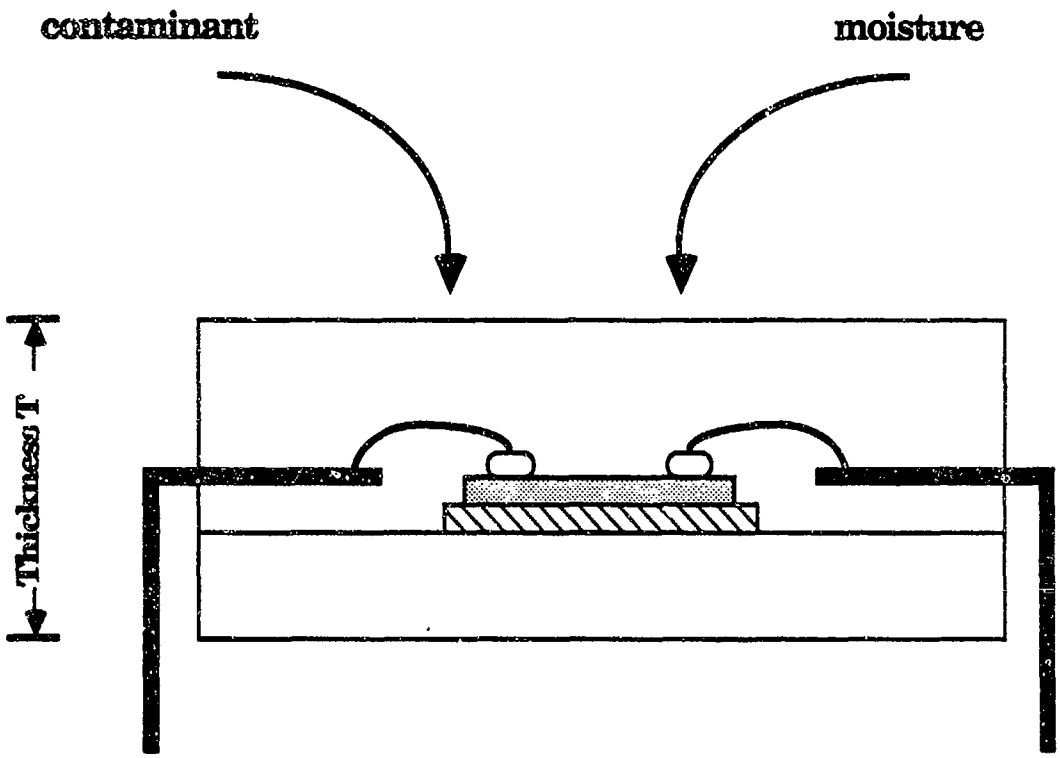


FIGURE H-8

Time to Reach 3 Monolayers of H_2O as a Function of Package Internal Volume and Air Leak Rate



Effective Thickness = T/2

FIGURE H-9

Typical Plastic Encapsulated Package

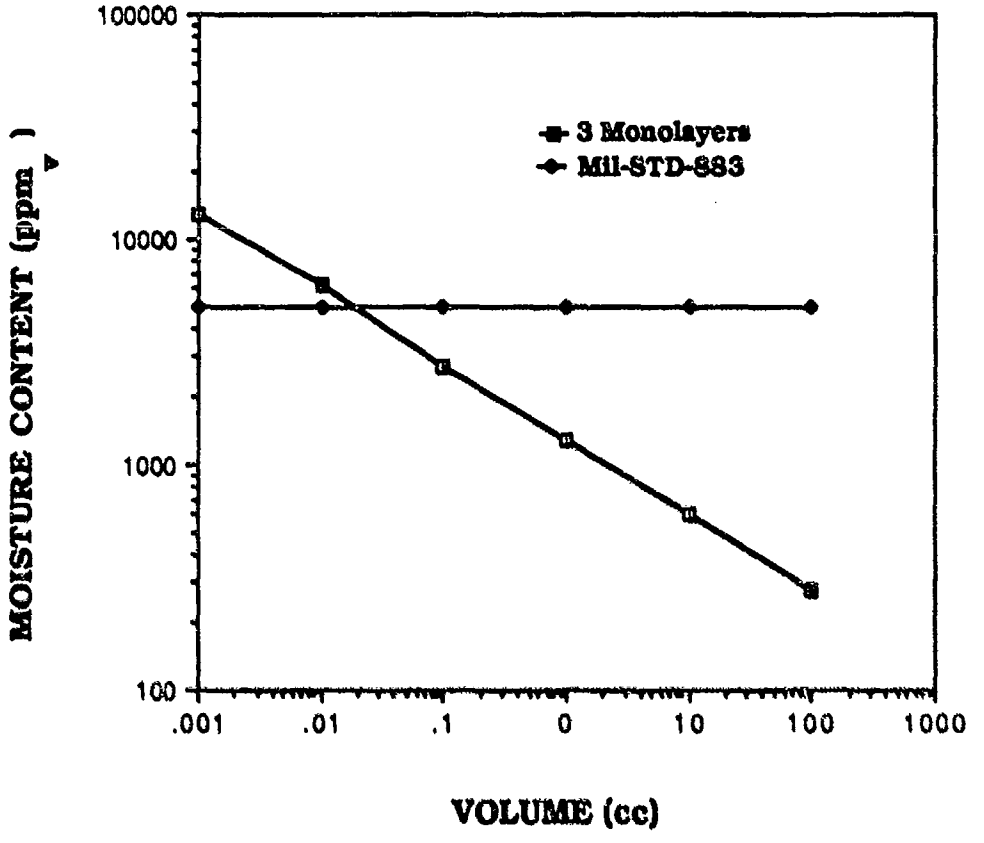


FIGURE H-10

Maximum Allowable Moisture Content as a Function of Internal Package Volume

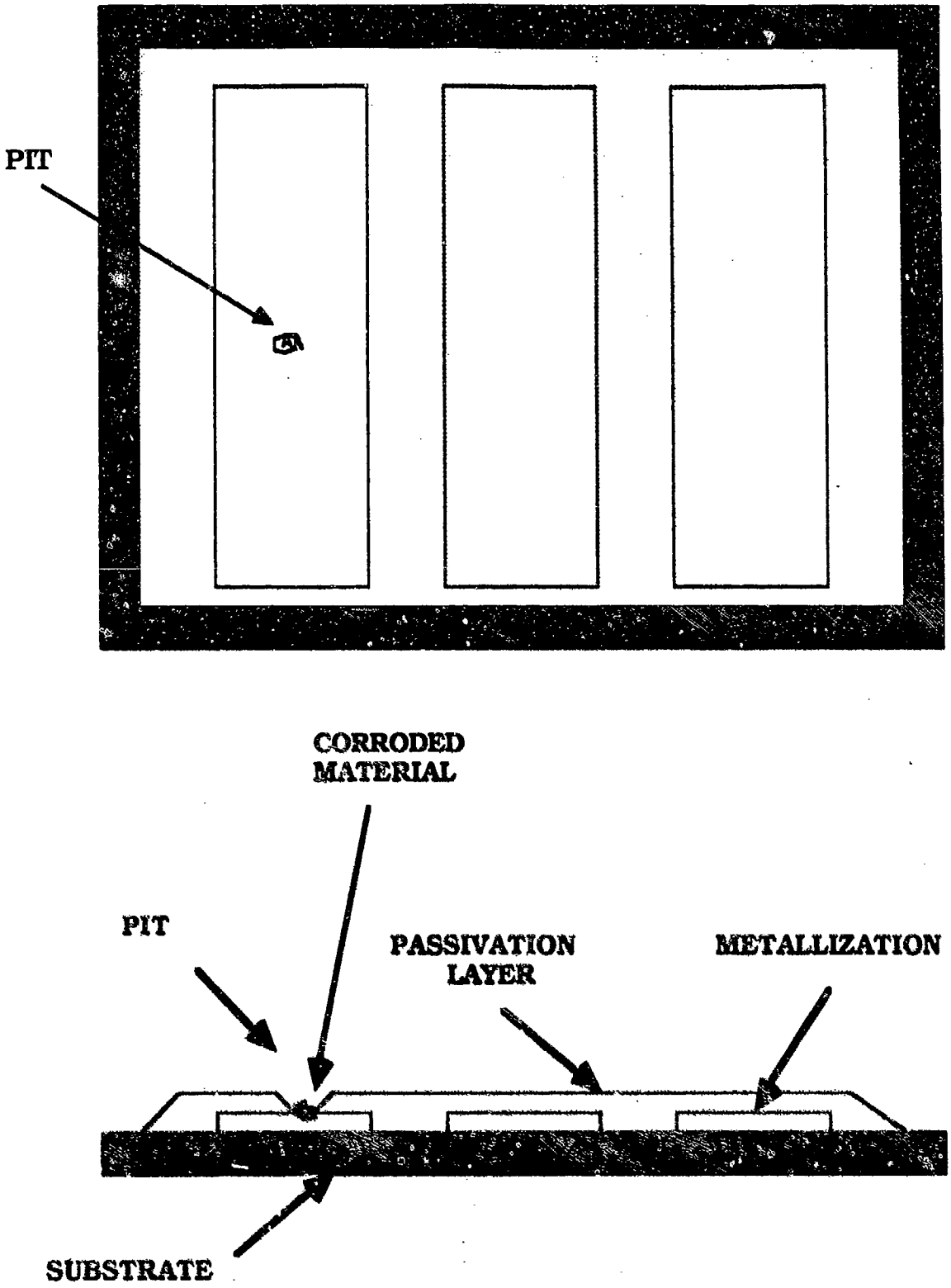


FIGURE H-11

Pitting in Passivated Metallization Layer

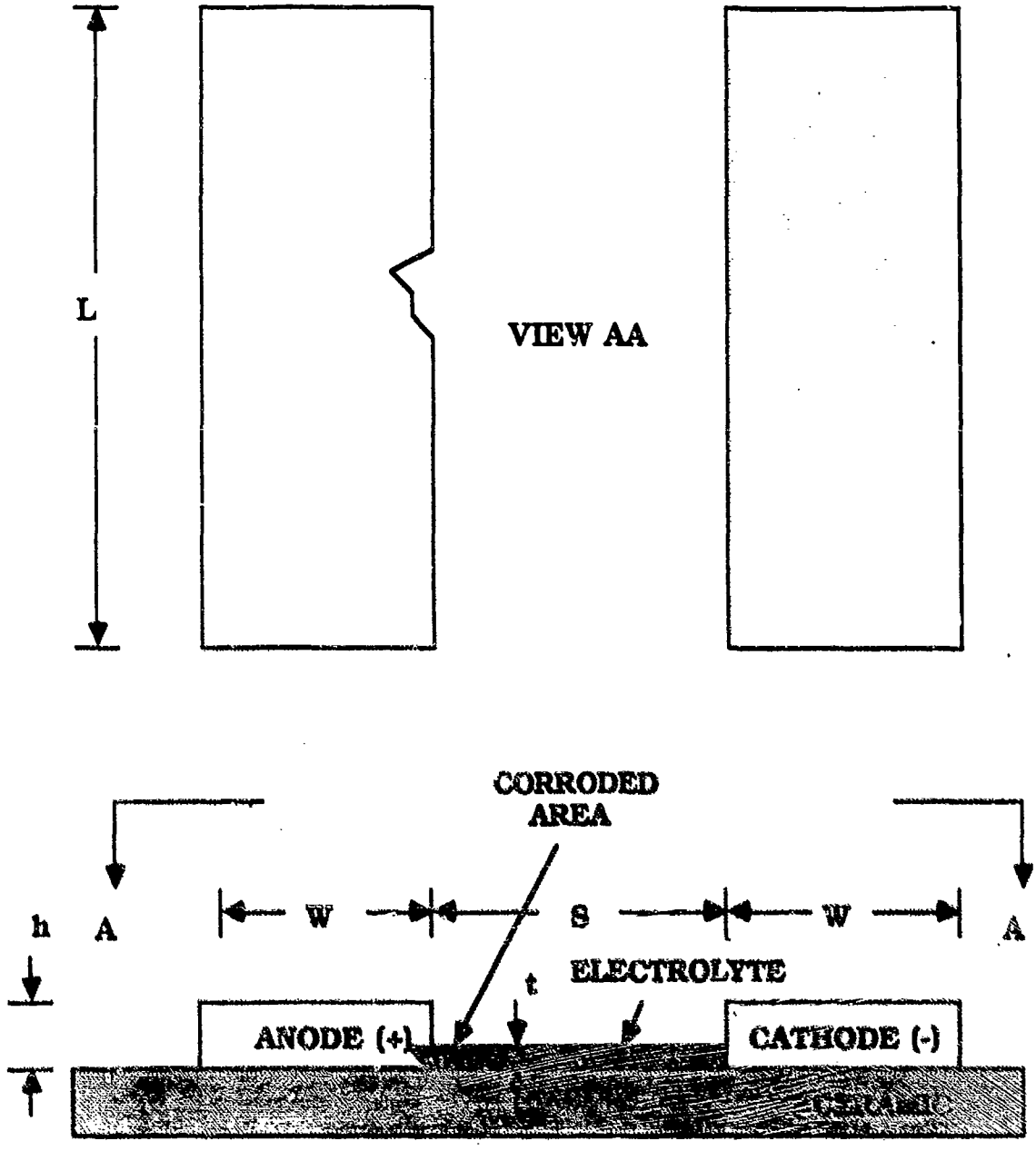


FIGURE H-12

Schematic Diagram for Metallization Corrosion

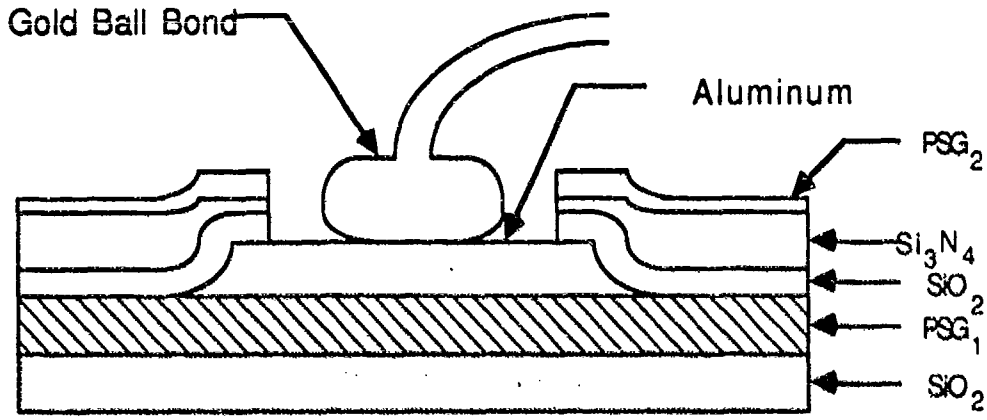


FIGURE H-13

Typical Bond Pad Structure

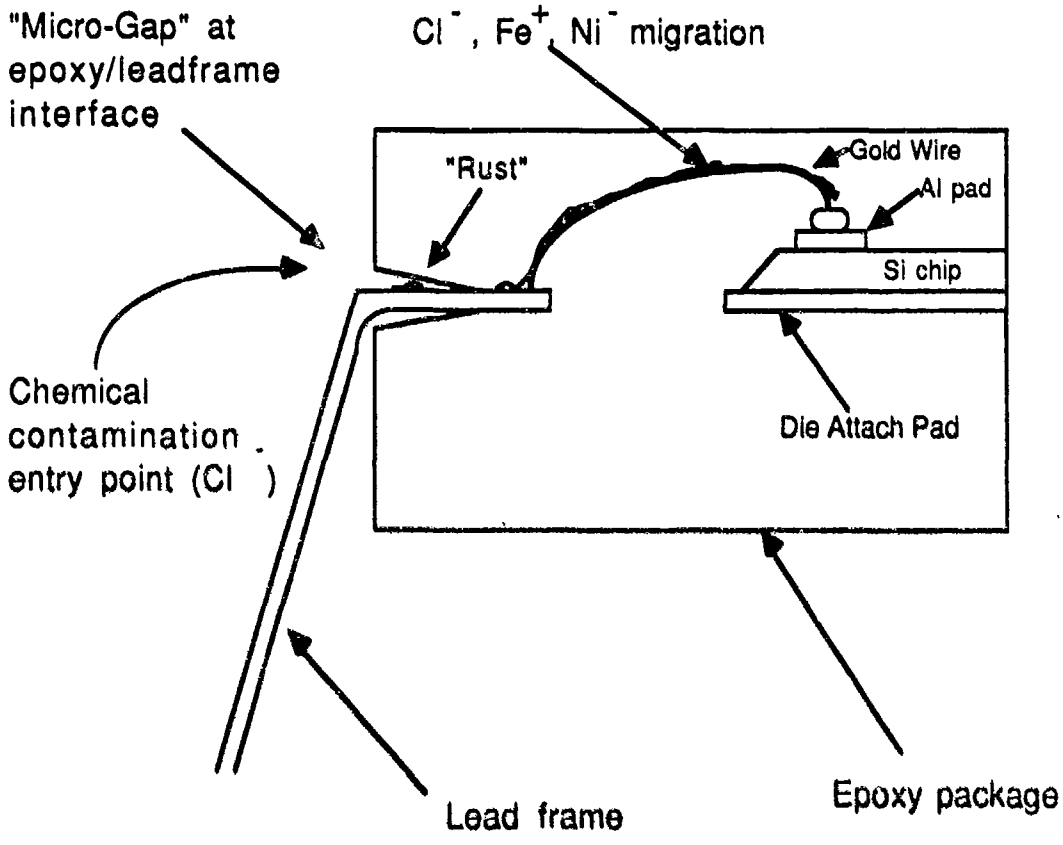
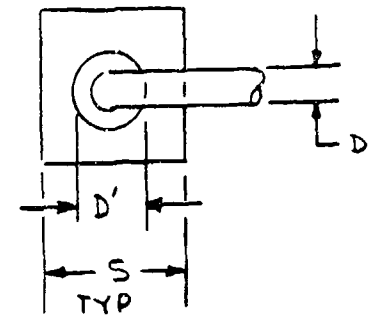
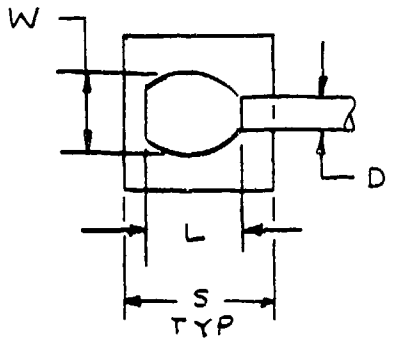


FIGURE H-14

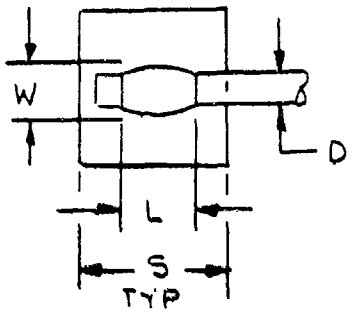
Path for Contaminants Entering the Package to the Pad



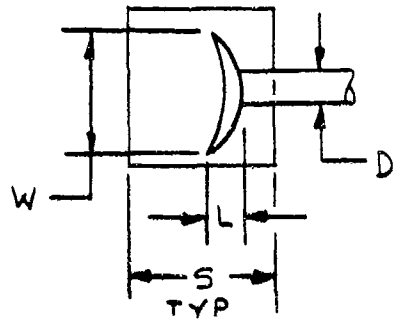
BALL BOND



ULTRASONIC
WEDGE BOND



THERMOCOMPRESSION
WEDGE BOND

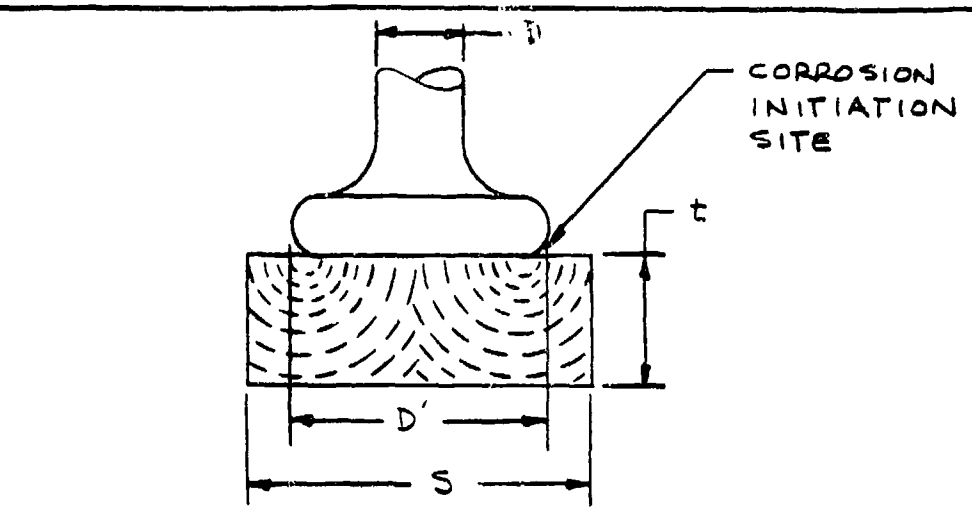


CRESCENT
BOND

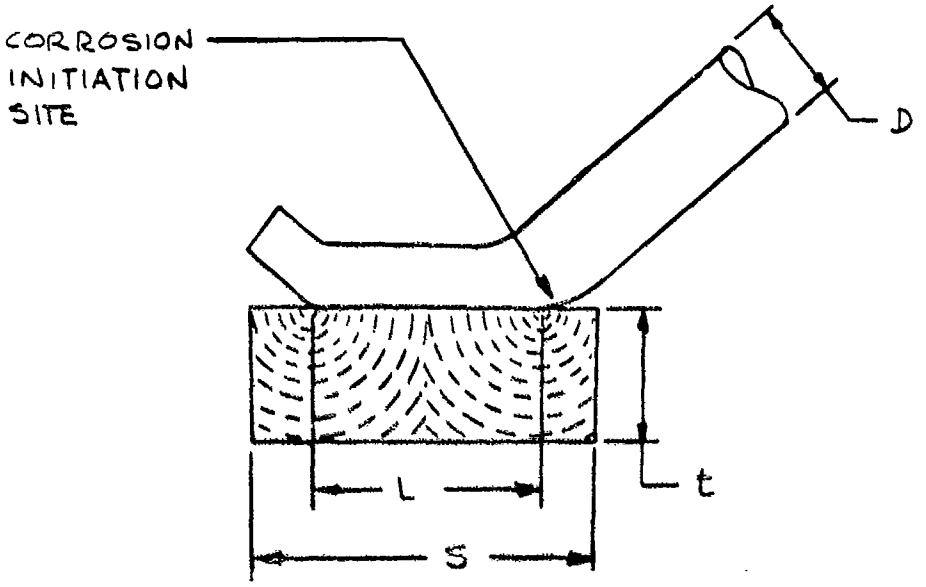
BOND TYPE	D' OR L			W		
	MIN	NOM	MAX	MIN	NOM	MAX
BALL	2D	4D	6D	-	-	-
U/S WEDGE	1.5D	3.25D	5D	1.2D	2.1D	3D
T/C WEDGE	1.5D	3.25D	5D	1.5D	2.25D	3D
CRESCENT	0.5D	1.75D	3D	1.2D	3.1D	5D

FIGURE H-15

FORMED BOND GEOMETRY LIMITS



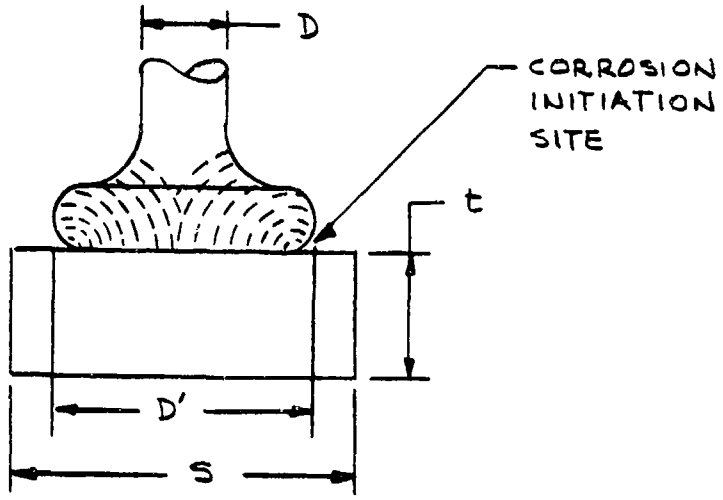
BALL BOND



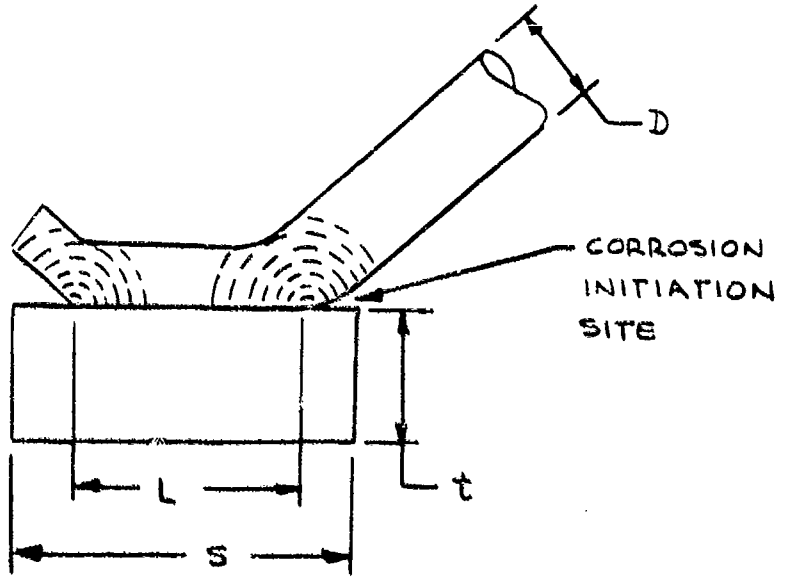
WEDGE BOND

FIGURE H-16

CORROSION VOLUME GEOMETRY -
BOND PAD ANODIC TO WIRE



BALL BOND



WEDGE BOND

FIGURE H-17

CORROSION VOLUME GEOMETRY -
WIRE ANODIC TO BOND PAD

Table H-1

METAL	USES
Gold	Electrical connector contacts, printed circuit board edge connectors, leaf-type relays, miniature coaxial connectors, semiconductor leads, and microminiature and hybrid circuits
Silver	Protective coating on relay contacts, wave guide interiors, wire, high frequency cavities, EMI/EMP shields, and EMI gaskets
Magnesium Alloys	Radar antenna dishes and light weight structure, such as chassis, support and frames
Iron, Steel and Ferrous Alloys	Component leads, magnetic shields, magnetic coatings on memory disks, transformers, brackets, racks, hermetic electrical connector shells and fastener hardware
Aluminum Alloys	Equipment housing, chassis, mounting racks, support, frames, electrical connector shell, and printed circuit board heat sinks
Copper and Copper Alloys	Wire, PCB circuitry and heat sinks, component leads, terminals, bus bars, nuts and bolts, and radio frequency gaskets.
Cadmium Plating	Sacrificial protective coating on ferrous fastener hardware and on electrical connectors
Nickel Plating	Barrier-type layer between copper and gold in electrical contacts, for corrosion protection on electrical connectors, PCB heat sinks, electrical bonds in EMI applications and for compatibility in dissimilar-metal junctions

Table H-1 (CONTD)

METALS	USES
Tin Plating	For corrosion protection, solderability, and compatibility between dissimilar metals, on electrical connectors, radio frequency shields, filters, small enclosures, component leads and automatic switching devices
Solder and Solder Plating	For joining, solderability and corrosion protection
Beryllium	Inertial guidance instruments

Table H-2

Moisture Content vs. Volume (PPM)

Volume (cc)	Surface Area (cm)	Ratio of Area to Volume	Water Thickness (cm)	Number of Monolayers	Moisture Content
0.001	0.08	80			13000
0.01	0.38	38			6200
0.1	1.7	17	1.2×10^{-7}	3	2700
1	8.2	8.2			1300
10	38	3.8			600
100	175	1.75			280

APPENDIX H-1

DEVELOPMENT OF A PERMEATION MODEL

In order to develop a mathematical model, the validity of Fick's Laws have to be assumed as a beginning. This development assumes constant temperature conditions unless specifically noted otherwise. Recall that Fick's Laws are:

$$F = -D \left(\frac{\partial C}{\partial x} + \frac{\partial C}{\partial y} + \frac{\partial C}{\partial z} \right) \tag{H4.1}$$

$$\frac{dC}{dt} = D \left(\frac{\partial^2 C}{\partial x^2} + \frac{\partial^2 C}{\partial y^2} + \frac{\partial^2 C}{\partial z^2} \right) \tag{H4.2}$$

Assuming the permeation is one dimensional and occurs along the x axis, as shown in figure H-1 based on a semi-infinite mathematical model, in uni-dimensional terms; i.e.,

$$F = -D \frac{dC}{dx} = D \frac{(C_1 - C_2)}{L} \tag{H4.3}$$

$$\text{and } \frac{\partial^2 C}{\partial x^2} = \frac{1}{D} \frac{\partial C}{\partial t} \tag{H4.4}$$

where:

- C is the concentration
- x is the membrane thickness
- D is the diffusion constant
- t is the time

In some practical systems, the surface concentration may not be known but only the gas or vapor pressure P_1, P_2 on the two sides of the membrane is known. The rate of transfer in the steady state is then sometimes written

$$F = D_p \frac{(P_1 - P_2)}{L} \tag{H4.5}$$

and the constant D_p is referred to as the permeability constant. Assuming the diffusion coefficient, D, is constant, and there is a linear relationship

between the external vapor pressure and the corresponding equilibrium concentration within the membrane, then equation H4.3 and H4.5 are equivalent, but not otherwise.

$$\text{Then } F = -D_p \frac{dP}{dx} \tag{H4.6}$$

$$\text{and } \frac{\partial^2 P}{\partial x^2} = \frac{1}{D_p} \frac{\partial P}{\partial t}$$

Consider the following conditions as in figure H-1:

$$\frac{\partial^2 P}{\partial x^2} = \frac{1}{D_p} \frac{\partial P}{\partial t}, \quad 0 < x < L, \; t > 0 \tag{H4.8}$$

$$P(x,0) = f(x), \qquad 0 < x < L \tag{H4.9}$$

$$P(0,t) = P_1, \qquad t > 0 \tag{H4.10}$$

$$\frac{\partial P}{\partial x}(L,t) = 0 \qquad t > 0 \tag{H4.11}$$

It is easy to verify that the steady-state solution of this problem is $P(x) = P_1$. Using this information, this boundary value-initial value problem can be solved by the transient concentration $w(x,t) = P(x,t) - P_1$

$$\frac{\partial^2 w}{\partial x^2} = \frac{1}{Dp} \frac{\partial w}{\partial t}, \qquad 0 < x < L, \; t > 0 \tag{H4.12}$$

$$w(x,0) = f(x) - P_1 = g(x), \qquad 0 < x < L \tag{H4.13}$$

$$w(0,t) = 0, \qquad t > 0 \tag{H4.14}$$

$$\frac{\partial w}{\partial x}(L,t) = 0 \qquad t > 0 \tag{H4.15}$$

Since this problem is homogeneous, it can be solved by the method of separation of variables. The assumption that $w(x,t)$ has the form of a product, $\phi(x)T(t)$, and insertion of w in that form into the partial differential equation H4.12 leads to the separated equations

$$\phi''(x) + \lambda^2 \phi = 0, \quad 0 < x < L \tag{H4.16}$$

$$T' + \lambda^2 kT = 0, \quad t > 0 \tag{H4.17}$$

Moreover, the boundary conditions take the form

$$\phi(0)T(t) = 0, \quad t > 0 \tag{H4.18}$$

$$\phi'(L)T(t) = 0, \quad t > 0 \tag{H4.19}$$

It has been shown that $\phi(0)$ and $\phi'(L)$ should both be zero:

$$\phi(0) = 0, \quad \phi'(L) = 0 \tag{H4.20}$$

Now, the general solution of the differential equation H4.16 is

$$\phi(x) = a'\cos \lambda x + b'\sin \lambda x \tag{H4.21}$$

The boundary condition, $\phi(0) = 0$, requires that $a' = 0$, leaving

$$\phi(x) = b'\sin \lambda x \tag{H4.22}$$

The boundary condition at $x = L$ now takes the form

$$\phi'(L) = b'\lambda \cos \lambda L = 0 \tag{H4.23}$$

The three choices are $b' = 0$, which gives the trivial solution; $\lambda = 0$, and $\cos \lambda L = 0$. The third alternative requires that λL be an odd multiple of $\pi/2$, which can be expressed as

$$\lambda_n = (2n - 1)\, \pi / 2L, \qquad n = 1, 2, \ldots. \tag{H4.24}$$

The eigenfunctions are given by the formula

$$\phi_n(x) = \sin \lambda_n x \tag{H4.25}$$

With the eigenfunctions and eigenvalues determined, the solution to equation

H4.17 becomes

$$T_n(t) = \exp\left(-\lambda_n^2 D_p t\right) \tag{H4.26}$$

By adopting the Fourier sine series, the solution to the problem is

$$P(x,t) = P_1 + \Sigma\, b_n \sin \lambda_n x \exp\left(-\lambda_n^2 D_p t\right) \tag{H4.27}$$

Suppose that the initial condition H4.9 is

$$P(x,0) = P_o, \qquad 0 < x < L \tag{H4.28}$$

Then equation H4.13 becomes

$$g(x) = P_o - P_1 \qquad 0 < x < L \tag{H4.29}$$

and

$$b_n = (P_o - P_1)\,\frac{4}{\pi(2n-1)} \tag{H4.30}$$

The complete solution of the boundary value-initial value problem with initial condition $P(x,0) = P_o$ would be

$$P(x,t) = P_1 + (P_o - P_1)\,\frac{4}{\pi}\,\Sigma\,\frac{1}{2n-1}\sin \lambda_n x \exp\left(-\lambda_n^2 D_p t\right) \tag{H4.31}$$

For $x = L$, $t =$ infinity, $p(L,\infty) = P_1$
For $x = L$, $t = 0$

$$P(L,0) = P_1 + (P_o - P_1)\,\frac{4}{\pi}\,\Sigma\,\frac{1}{2n-1}\sin \lambda_n L$$

$$= P_1 + (P_o - P_1)\,\frac{4}{\pi}\,\Sigma\,\frac{1}{2n-1}\sin \frac{(2n-1)\pi}{2L} L$$

$$= P_1 + (P_o - P_1)\frac{4}{\pi}\left(1 - \frac{1}{3} + \frac{1}{5} - \frac{1}{7} + \ldots\right)$$

$$= P_1 + (P_o - P_1)\frac{4}{\pi}\frac{\pi}{4}$$

$$= P_o \qquad \text{(H4.32)}$$

Now, for any time t at the boundary x = L, the partial pressure is

$$P(L,t) = P_1 + (P_o - P_1)\frac{4}{\pi}\sum\frac{1}{N}\sin\frac{N\pi}{}\exp\left[-\frac{(N\pi)^2}{2L}D_p t\right]$$

$$= P1 + (\rho_o - \rho_1)\frac{4}{\pi}\sum\frac{1}{N}\sin\frac{N\pi}{2}e^{-\left[\frac{N^2\pi^2}{4L^2}\right.}D_p t]$$

$$P(L,t) = P_1 + (P_o - P_1)\frac{4}{\pi}\left[e^{-\left[\frac{\pi^2 D_p t}{4L_2}\right.} - \frac{1}{3}e^{-\left[\frac{9\pi^2 D_p t}{4L_2^2}\right.} +\right.$$

$$\left.\frac{1}{5}e^{-\left[\frac{25\pi^2 D_p t}{4L^2}\right.} - \frac{1}{7}e^{-\left[\frac{49\pi^2 D_p t}{4L^2} + \ldots\ldots\right.}\right]$$

$$\simeq P_1 + (P_o - P_1)\,e^{-\left[\frac{\pi^2 D_p t}{4L^2}\right.} \qquad \text{(H4.33)}$$

Let $P_o = 0$

$$\text{Then } \frac{P(L,t)}{P1} \simeq 1 - e^{-\left(\frac{\pi^2 D_p t}{4\,L^2}\right)} \qquad \text{(H4.34)}$$

as $t \to \infty$, $P(L, t)/P \simeq 1$

$$\text{Let } \frac{P(L,t)}{P_1} = 0.95$$

$$\text{Then } 1 - e^{-\left(\frac{\pi^2 D_p t}{4\,L^2}\right)} = 0.95$$

$$\text{and } e^{-\left(\frac{\pi^2 D_p t}{4 L^2}\right)} = 0.05$$

Taking logarithms

$$-\left(\frac{\pi^2 D_p t}{4 L^2}\right) = -3$$

$$t = \frac{12 L^2}{\pi^2 D_p} \qquad \text{(H4.35)}$$

APPENDIX H-2

DEFINING EQUATIONS FOR LEAKAGE FLOW REGIMES

Viscous flow occurs when the mean free path of the gas is smaller than the cross-section dimension of the physical leak. Poiseuille's Law for viscous flow through a cylindrical tube is shown.

$$Q = \frac{\pi r^4}{8 \eta l} \times 10^{-3} \bar{P} (P_1 - P_o) \qquad (H5.1)$$

where

Q is the flow rate, in micrometer liters per second

r is the radius of tube, in centimeters

η is the viscosity of gas in poise

l is the length of tube, in centimeters

$\bar{P}$ is the average pressure, $(P_1 + P_o)/2$, in micrometers Hg

P_1 is the outside partial pressure, in micrometers Hg

P_o is the inside partial pressure, in micrometers Hg

Transition flow occurs when the mean free path of the gas is approximately equal to the cross-section dimension of the leak and it occurs under conditions intermediate between viscous flow and molecular flow. Again for a long tube, the flow may be expressed as shown below[39]:

$$Q = \frac{30.48 r^3}{l} \sqrt{\frac{T}{M}} (P_1 - P_o) \left[\frac{0.1472 r \bar{P}}{La} + \frac{1 + 2.507 r \bar{P}/La}{1 + 3.095 r \bar{P}/La} \right] \qquad (H5.2)$$

where:

Q is the flow rate, in micrometer liters per second

r is the radius of the tube, in centimeters

l is the length of the tube, in centimeters

M is the molecular weight of gas, in amu

P_1 is the outside partial pressure, in micrometers Hg

P_o is the inside partial pressure, in micrometers Hg

T is the temperature, in degrees kelvin

La is the mean free path, in centimeters, at the average pressure $(P_1 + P_o)/2$

Molecular flow occurs when the mean free path of the gas is greater than the longest cross-section dimension of the physical leak. Knudsen's Law for molecular flow neglecting the end effect is shown[40]:

$$Q = \frac{30.48r^3}{l}\sqrt{\frac{T}{M}} \qquad \text{(H5.3)}$$

where:

Q is the flow rate, in micrometer liters per second
r is the radius of the tube, in centimeters
l is the length of the tube, in centimeters
M is the molecular weight of gas, in amu
T is the temperature, in degrees kelvin

APPENDIX H-3

DEVELOPMENT OF ELECTROLYTE RESISTIVITY VALUES

From Rice's data,[19] the arithmetic mean of chlorine gas concentration within electronic equipment locations is $0.51 \times 10^{-6} gm/m^3$.

$$0.51 \times 10^{-6} \text{ gm } Cl_2 \times \frac{1 \text{ mole } Cl_2}{71 \text{ gm}} \times \frac{0.0224 \text{ m}^3}{1 \text{ mole } Cl_2}$$

$$= 1.6 \times 10^{-10} \text{ m}^3 \text{ } Cl_2$$

Therefore, the concentration of chlorine gas is 1.6×10^{-4} ppm_v. Consider the reaction of Cl_2 with water.

$$Cl_2 \text{ (g)} + H_2O \leftrightarrow H^+ + Cl^- + HOCl \qquad \text{(H6.1)}$$

This equation can be derived by adding the standard electrode reactions:

$$Cl_2 \text{ (g)} + 2 e^- = 2 Cl^- \qquad E° = +1.3583 \qquad \text{(H6.2)}$$

$$H_2O + Cl^- = H^+ + HOCl + 2 e^- \qquad E° = -1.49 \qquad \text{(H6.3)}$$

Applying the Nernst equations,

$$E_{12} = E_{12}° - \frac{RT}{2F} \ln \frac{[Cl^-]^2}{[Cl_2]} \qquad \text{(H6.4)}$$

and

$$E_{13} = E_{13}° - \frac{RT}{2F} \ln \frac{[H^+][HOCl]}{[H_2O][Cl^-]} \qquad \text{(H6.5)}$$

Adding equations H6.4 and H6.5:

$$E_{11} = E_{12}° + E_{13}° - \frac{RT}{2F} \ln \frac{[Cl^-][H^+][HOCl]}{[Cl_2][H_2]} \qquad \text{(H6.6)}$$

The activities of the H^+ and Cl^- ions are close to their concentration in dilute solution and the activities of Cl_2 is its partial pressure in atmospheres (1.6×10^{-10}). The activities of water and HOCl are unity. Therefore equation H6.6 becomes

$$E_{11} = 1.3583 - 1.49 - \frac{(8.314)(358)}{(2)(96500)} \ln \frac{[H^+][Cl^-]}{1.6 \times 10^{-10}}$$

$$= 0$$

$$\Rightarrow \quad 0.1317 = -0.01542 \ln \frac{[H^+][Cl^-]}{1.6 \times 10^{-10}}$$

from which

$$[H^+][Cl^-] = 3.125 \times 10^{-14}$$

$$[H^+] \text{ or } [Cl^-] = 1.77 \times 10^{-7}$$

Equivalent conductivity is defined as

$$\Lambda = \frac{1000}{C\rho}$$

where C is the ionic concentration.

From the CRC Handbook of Chemistry and Physics,[21] combined equivalent conductivity of H^+ and Cl^- is 775 at 85°C, hence

$$\rho = \frac{1000}{1.77 \times 10^{-7} \times 775}$$

For a corrosive environment, the amount of Cl_2 existing is assumed to be ten times the normal environment, or 5.1×10^{-6} gm/m^3. By going through the same calculations as above, the resistivity of the electrolyte for this condition at 85°C/85 RH is found to be 2.3×10^6 ohm-cm.

APPENDIX H-4
SELECTION OF BIAS VOLTAGE FOR EQUATIONS H3.7 & H3.10

Corrosion of metals is an electrochemical phenomenon and its rate is proportional to the electrical potential difference between the anodic and cathodic regions of the corrosion site. Hence the time to failure of conductor and bond pad metallization due to corrosive attack, as modeled in equations H3.7 and H3.10, is directly proportional to a voltage bias. The applied voltage difference between adjacent signal or ground metallizations on a microcircuit is the usual driving force in electrochemical corrosion. However, when two dissimilar metals are in contact, such as gold wire bonded to an aluminum pad, corrosion will proceed without an applied electrical bias when an electrolyte is present. The corrosion process is then driven by the galvanic potential difference existing between the two metals. The magnitude of the galvanic potential depends upon the electrolyte concentration, pH, flow, aeration and temperature.[31] The anodic member of the dissimilar metal pair is usually corrosively attacked, but secondary effects such as varying ion concentration, relative anode/cathode area, electrolyte resistivity, polarization of the wetted metal surfaces by oxide films or gas evolution and the formation of insoluble corrosion products on the metal surfaces can change the corrosion rate or reverse the process to corrosive attack of the cathodic member. Since exact knowledge of the conditions actually present in a microelectronic device during corrosive attack is not feasible, a first approximation to the differing corrosion rates of various dissimilar metal couples can be achieved by assuming the corrosion rate is proportional to the electrochemical galvanic potential difference between the two metals, and by assuming that the anodic member receives the corrosive attack.

Table 4.5-16 has been abstracted from reference [46] and lists the electrochemical galvanic potential for materials commonly used in proximity to each other in microelectronic devices. The galvanic potential difference for any two metals is defined as the algebraic difference between their electrode potentials listed in the table. However, the galvanic potential difference for use in equations H3.7 and H3.10 is defined as follows:

$$V_{galvanic} = 1 + (V_{cathode} - V_{anode}) \qquad (H7.1)$$

For example, the galvanic potential difference for a gold wire bonded to an aluminum pad is:

$$V_{galvanic} = 1 + (1.5 - (-1.66)) = 4.16 \text{ V}$$

The value for the bias voltage V for use in equations H3.7 and H3.10 shall be chosen as follows:

(1) for dissimilar bond wire and bond pad metals - use the larger of the applied signal or power supply voltage as compared to the galvanic voltage from Table 4.5-16

(2) for similar metals - use the applied signal or power supply voltage.

APPENDIX H-5
BOND PAD/BOND WIRE CORROSION VOLUME

The time to failure of microcircuit metallization due to corrosive attack is directly proportional to the quantity of material that must be corroded before the electrical continuity of the circuit is disrupted. As discussed in paragraph H3.1.1, Faraday's Law relates time to the volume of material consumed in an electrochemical reaction. For a metallization conductor, the minimum volume, and consequently the minimum time to failure, is obtained by assuming active corrosion occurs along a conductor length equal to its width, which leads to the simple geometry contribution shown in equation H3.6. However, for corrosion occurring at a bond pad-bond wire interface, the corrosion volume geometry is more complex.

The corrosion volume considered in this study is a function of the bond pad geometry (length, width, thickness), the bond-wire size, the bond type (ball, wedge, crescent), the bond process (ultrasonic, thermocompression), and the position of the bond pad material and the bond wire material in the galvanic electrode potential series (Table 4.5-16). As discussed in Appendix H-4, it is assumed that the anodic member of a dissimilar metal couple will be corroded. Hence, determination of the corrosion volume to be used in equation H3.10 begins with identification of the anodic member of the couple from Table 4.5-16.

MIL-STD-883, Method 2010, paragraphs 3.2.4.1 through 3.2.4.3 delineates acceptable geometry variation limits for four bond types. These data are shown in figure H-15. Typical corrosion volume geometry is shown in figures H-16 and H-17. The following observations are applicable to the relationship between the completed bond geometry and bond pad geometry:

(1) Microcircuit bond pads are typically of equal width and length, with the pad size bearing a restricted relationship to bond wire diameter that is dictated by bond process positioning tolerance limitations and MIL-STD-883 position acceptance criteria.

(2) For a square bond pad of side S, the relationship of S to bond wire diameter D may vary between $3D \leq S \leq 6D$, with a predominant value of $S = 4D$.[38]

(3) Review of figure H-15 indicates that acceptable geometry for formed ultrasonic and thermocompression wedge bonds are nearly identical. Also, the width of a crescent bond is nearly identical to the length of a wedge bond.

(4) From (2) and (3), it follows that maximum acceptable wedge and crescent bond geometry is greater than the typical bond pad size.

(5) Acceptable ball bond geometry is greater than acceptable wedge/crescent bond geometry. Hence, a larger pad size is required for ball bonds to permit reasonable bond process positioning tolerances, and the relationship $S = 5D$ is required.

(6) From (3) and (4), the complexity of bond pad geometry requirements can be reduced by concluding that all wedge and crescent bonds can be considered as approximately equal with respect to the effective corrosion volume associated with each type.

(7) MIL-STD-883, Method 2023, delineates bond strength acceptance criteria for bond wire diameters from 1.8×10^{-3} cm (0.0007 in) to 7.6×10^{-2} cm (0.030 in). Low power digital microcircuits typically utilize bond wire diameters from 1.8×10^{-3} cm (0.0007 in) to 3.8×10^{-3} cm (0.0015 in).

(8) Bond pad thickness for microcircuits typically range from 5000 angstroms to 10000 angstroms (5×10^{-5}cm to 1×10^{-4}cm) (2×10^{-5}in to 4×10^{-5}in).

(9) From (7) and (8) the relationship between bond wire diameter D and bond pad thickness t is $13\,D \leq t \leq 57\,D$.

From the above, it is clear that for any bond type, when the bond pad material is anodic to the bond wire material, the entire bond pad volume must be consumed before the corrosion process results in an open circuit failure. Since corrosion time is proportional to corrosion volume, a subsidiary conclusion is that a ball bond will have approximately 50% longer corrosion life than other bond types, due to the larger bond pad required, when the pad is anodic to the wire material.

Kiely[18] has suggested that depletion of 30% of the bond pad volume be considered as corrosion failure. This is not only conservative but also realistic, considering the mechanical and thermomechanical stresses present during military equipment operation. Such stresses could cause premature failure of a corrosion weakened bond pad. Hence, when the bond pad is the anode of a dissimilar metal couple, the corrosion volume is:

$$V_c = 0.3\ S^2 t_b \qquad \text{(H.8a)}$$

where V_c = corrosion volume, cm^3
S = bond pad size, cm (for a square pad)
t_b = bond pad thickness, cm

When the bond wire is anodic to the bond pad material, the corrosion volume geometry is shown in figure H-17. For a wedge or crescent bond, the minimum corrosion volume is at the heel of the bond, and can be approximated as:

$$V_c = 0.3 \pi D^3/4 = 0.236D^3 \qquad \text{(H.8b)}$$

where D = bond wire diameter, cm

For a bond bond, assuming that the formed ball height is approximately equal to the wire diameter and using the nominal formed ball diameter from figure H-15, the corrosion volume can be approximated as:

$$V_c = 0.3 \pi (4D)^2 D/4 = 3.77\ D^3 \qquad \text{(H.8c)}$$

Comparison of equations H.8b and H.8c suggests that a ball bond will have approximately 16 times longer corrosion life than other bond types, when the wire is anodic to the pad material.

APPENDIX I

OPERATIONAL ΔT VALUES FOR APPLICATION ENVIRONMENT CATEGORIES

The microelectronic device reliability prediction models developed in this report for die fracture, die attach fatigue, bond pad shear fatigue, bond wire flexure fatigue and bond wire axial fatigue evaluate the number of cycles to failure for each failure mechanism. Each of these mechanisms is induced by differential thermal expansion during exposure of the device to thermal cycling. The models developed can be described in generic terms as power law relationships between the mean number of cycles to failure and the local state of stress or strain in the device. In all cases, the temperature difference (ΔT) between the maximum and minimum temperatures of the thermal cycle is raised to a power. Hence, the choice of ΔT for use in the model equations has a significant effect on the predicted cycle life magnitude.

The environmental temperature extremes delineated in Military Specifications for various classes of electronic equipment forms an upper boundary for ΔT. A list of these specifications and the extreme operating temperature for each equipment type is given in Table 4.6-9. From this data it can be seen that the ΔT upper boundary limit varies from 30°C to 179°C for different types of electronic equipment used in various application environments.

For electronic equipment used in any application environment, the temperature at the device is principally determined by factors other than the ambient temperature, e.g. power dissipated in the device, thermal resistance of the heat transfer path to the ambient, availability of supplementary cooling, etc. The heat transfer thermal resistance path includes the thermal effects of boundary layer air flow for avionic equipment, and for all equipment the path includes the thermal effects of second and third level packaging materials and structures, shelters, protective cases, vibration/shock isolators and vehicle structures. The thermal capacitance of metallic

structural elements contributes massively to attenuation and time lag of ambient temperature effects on individual microelectronic device cyclic operating temperature. Hence, it is unrealistic to assume that the specified environmental temperature extremes bear any defineable relationship to cyclic device operating temperature.

Very little published test data exists that provides a basis for determining the cyclic ΔT at device locations in equipment. Most test programs usually monitor temperatures on equipment surfaces or at selected internal locations. Such data, if available, would provide a realistic first order estimate of ΔT at device locations. Reference [1] reported temperatures recorded in the equipment bay of an A-7C aircraft during a 5 hour mission. Most likely the recorded temperature was the bay ambient and not the equipment surface. This data is summarized in Table I-1.

Early in 1989, the Institute for Interconnecting and Packaging of Electronic Circuits (IPC) formed a task group to establish criteria for, among other things, accelerated testing of surface mount technology solder joints. During its deliberations the task group defined 12 electronic product use categories, and for each category defined the extreme operating temperature range, the probable cyclic ΔT experienced under normal operating conditions, and the number of cycles per year that could be expected for each ΔT. Table I-2 summarizes the data from reference [2].

The IPC data was generated by a task group with representation from companies with experience in military avionic, military ground, commercial aviation, computer, telecommunication, industrial and consumer electronic components and equipment. The task group proposal was then circulated to the IPC member companies for concurrence. Hence the data in Table I-2 represents the most realistic evaluation of probable ΔT magnitudes available at this time.

Adaptation of the IPC data to the reliability prediction models developed in this report requires two steps, viz:

(1) Determination of a single equivalent ΔT for the IPC use categories for which more than one combination of ΔT/no. of cycles/cycle duration groupings exist.

(2) Matching of the IPC use categories with the new MIL-HDBK-217 application environments proposed in 4.6.4 and listed in Table 4.6-10.

The materials to which the prediction models will be applied range in mechanical characteristics from nearly plastic (60-40 solder) through elastic to nearly brittle (ceramics). For near-plastic materials, the temperature cycle duration is unimportant, since plastic creep quickly reduces the level of applied thermomechanical stress. The creep-induced damage in the internal structure of the bulk material occurs during the temperature change portion of the cycle, and the cyclic accumulation of damage is the mechanism of failure. At low temperature and high strain rates the mechanism is drastically accelerated. On the other hand, the failure mechanisms for elastic and near-brittle materials involve intensification of stress fields around local flaws above the average thermomechanical stresses induced in the bulk material. Stress intensification above the yield point of elastic materials and above a critical value for near-brittle materials causes crack initiation at the flaw sites and propagation throughout the bulk material. For these material types, practical thermal cycle durations, i.e. > 3 seconds, are sufficient for activation of the mechanism. Hence the variation of cycle duration for various IPC use categories in Table I-2 need not be considered for the step (1) development noted above.

It is reasonable to assume that stress/strain magnitude (and hence ΔT) has a significantly greater influence on the failure mechanisms modeled in this report than does number of cycles. As an appoximation to determining an equivalent ΔT, let a weighting function be derived as follows:

$$\Delta T_{eq}^{m} \sum_{i=1}^{n} (N_i) = \sum_{i=1}^{n} (\Delta T_i^{m} N_i), \; m > 1 \qquad \text{(I-1)}$$

where m = arbitrary constant

N_i = number of cycles for the ith $\Delta T/N$ pair

ΔT_i = ΔT for ith $\Delta T/N$ pair

ΔTeq = equivalent ΔT

The data given in Table I-3 is derived from Table I-2 using equation I-1 with $m = 3$ to determine an equivalent ΔT and the data in Table I-4 is derived from Tables I-2 and I-3 with the following considerations in matching the IPC use categories to the proposed MIL-HDBK-217 application elements:

(1) A_I: This environment is for aircrew inhabited compartments of air vehicles in which temperature and pressure is controlled. Comparable IPC use categories are commercial aircraft and military aircraft-I. For conservatism the higher value is recommended.

(2) A_U: This environment is for uninhabited air vehicles or compartments of air vehicles with uncontrolled temperature and pressure. Comparable IPC use categories are military aircraft-II and military aircraft-III. For conservatism the higher value is recommended.

(3) C_L: This environment is for the severe inertial conditions associated with electronically actuated cannon launched projectiles. The duration of this environment is extremely short and will have negligible effect on the failure mechanisms modeled in this report, assuming that the components chosen have been qualified for the inertial conditions. The storage environment prior to launch will have the greatest influence on the modeled failure mechanisms. The existing instructions in MIL-HDBK-217E, paragraph 5.1.1.3 for segmented reliability analysis when multiple application environments are applicable. See Note 2 of table I-4 and the discussion under (7) following for the M_F application environment.

(4) G_B: This environment is for instruments, computers and test, business,

medical and laboratory electronic equipment housed in temperature controlled buildings or shelters. Comparable IPC use categories are computers and telecommunication. The recommended value of ΔT lies between the IPC values and is chosen for similarity to the A_I application environment.

(5) G_F: This environment is for equipment housed in buildings or shelters without temperature control. Comparable IPC use category is military (ground/ship).

(6) G_M: This environment is for equipment mounted on powered or unpowered vehicles or for manually transported portable equipment. Comparable IPC use categories are military (ground/ship) for equipment mounted in compartments without temperature control and transportation (passenger compartment for temperature controlled vehicles or trailers.

(7) M_F: This environment is for missile powered or unpowered flight and the severe inertial conditions associated with missile launch, space vehicle boost and re-entry, rocket powered flight and parachute landing. There are no comparable IPC use categories. The contribution of this environment to the package (non-electrical) failure mechanism is negligible because the environment is of short duration e.g. missile launch, missile flight, manned space vehicled boost to orbit and re-entry, etc. For this reason, the storage environment prior to launch or flight has the dominant influence on the package related failure mechanisms. The principal source of thermally related stress during storage is the diurnal temperature cycle. Table I-5 summarizes the diurnal cycle temperature range data given in reference [3], which suggests that ΔT=20°C is a conservative choice for use in the failure mechanism model equations to represent storage under uncontrolled temperature conditions. Ambient climatic temperature changes have a neglibible effect on

temperature cycle range experienced by equipment stored under temperature controlled conditions. The temperature control system sensitivity of approximately ±3°C is the major contributor to controlled storage temperature cycle variation. For equipment constantly stored under controlled conditions it may be concluded that package related failure mechanisms can be considered as inactive. Assessment of combined controlled and uncontrolled conditions can use $\Delta T = 5°C$ for the controlled segments. See MIL-HDBK-217E, paragraph 5.1.1.3 for segmented multiple application environment reliability analysis instructions.

(8) N_I: This environment is for equipment sheltered from weather exposure and accessible by naval vehicle or shore crew members. In some instances the sheltered volume may be temperature controlled e.g. submarine installations, surface vessel combat information center, etc. When actual installation conditions are known, the reliability analyst may utilze such data in lieu of the table I-4 value. Comparable IPC use category is military (ground/ship). The recommended value of ΔT is chosen to reflect the modifying effect of N_I usage as compared to N_U usage.

(9) N_U: This environment is for unsheltered ship and shore equipment exposed to weather conditions. Comparable IPC use category is military (ground/ship.). The recommended value of ΔT is chosen at the conservative higher level.

(10)N_{UL}: This environment is for undersea missile launch and torpedo mission equipment. The short duration of this environment will have negligible effect on package related (non-electrical) failure mechanisms. The pre-launch and pre-mission storage conditions determine the thermal stresses driving these mechanisms. There is no comparable IPC use category for this environment. From the discussion under (7) for the M_F application environment,

uncontrolled storage temperature conditions should use $\Delta T = 20°C$ and the effect of controlled storage conditions on component reliability can be ignored or a value of $\Delta T = 5°C$ may be used.

(11)N_{UU}: This environment is for equipment immersed in sea water. There is no comparable IPC use category. The ambient temperature is relatively benign and constant. The recommended value of ΔT is chosed for compatibility with N_U conditions, taking into account the ambient temperature stability of the N_{UU} environment and the excellent heat transfer to the ambient.

(12)S_F: This environment is for equipment in earth orbiting space vehicles. The comparable IPC use category is space.

TABLE I-1

THERMAL CYCLE DATA FROM REFERENCE [1]

Cycle Temperature		Cycle Duration Minutes	Number Cycles	ΔT °C
Min	Max			
17	60	64	3	43
38	58	6	6	20

Table I-2

Thermal Cycle Data from Reference [2]

IPC USE CATEGORY	OPERATING TEMP. RANGE, °C		CYCLIC ΔT °C	NUMBER CYCLES/ YEAR	CYCLE DURATION HOURS
	MIN.	MAX			
CONSUMER	0	60	35	365	12
COMPUTERS	15	60	20	1460	2
TELECOMMUNICATIONS	-40	85	35	365	12
COMML. AIRCRAFT	-55	95	20	3000	2
INDUSTRIAL	-55	65	20	185	12
			40	100	12
			60	60	12
			80	20	12
TRANSPORTATION (Passenger Compt)	Same as Industrial				
TRANSPORTAION (Engine Compt)	-55	125	60	1000	1
			100	300	1
			140	40	2
MILITARY (Ground/Ship)	-55	95	40	100	12
			60	265	12
MILITARY (Aircraft - I)	-55	95	20	1000	1
			40	500	2
MILITARY (Aircraft - II)	-55	95	20	1000	1
			60	500	2
MILITARY (Aircraft - III)	-55	95	20	1000	1
			80	500	2
SPACE	-40	85	35	3650	2

Table I-3

Equivalent ΔT

IPC USE CATEGORY	ΔT_{eq} °C
CONSUMER	35
COMPUTERS	20
TELECOMMUNICATION	35
COMMERCIAL AIRCRAFT	20
INDUSTRIAL/TRANSPORTATION (PASSENGER COMPARTMENT)	44
TRANSPORTATION (ENGINE COMPARTMENT)	78
MILITARY (GROUND/SHIP)	56
MILITARY (AIRCRAFT - I)	30
MILITARY (AIRCRAFT - II)	43
MILITARY (AIRCRAFT - III)	56
SPACE	35

Table I-4

Recommended Value for Component Operating ΔT (see note 1)

MIL-HDBK-217 APPLICATION ENVIRONMENT		ΔT °C
PRESENT	PROPOSED	
A_{IA}, A_{IB}, A_{IC}, A_{IF}, A_{IT}, A_{RW}	A_I	30
A_{UA}, A_{UB}, A_{UC}, A_{UF}, A_{UT}	AU	55
C_L	C_L	Note 2
G_B, G_{MS}	G_B	30
G_F	G_F	55
G_M, M_P	G_M	Note 3
M_{FA}, M_{FF}, M_L	M_F	Note 2
N_H, N_S, N_{SB}	N_I	50
N_U	N_U	55
U_{SL}	N_{UL}	Note 2
N_{UU}	N_{UU}	35
S_F	S_F	35

Note 1. Table I-4 ΔT values are for use when thermal analysis or test data are not available.

Note 2. Application environments referring to this note are of short duration and have negligible effects on the package (non-electrical) related failure mechanisms, for which the pre-launch storage conditions will have the dominant effect. Use $\Delta T = 5°C$ for storage under controlled temperature conditions and $\Delta T = 20°C$ for uncontrolled storage conditions.

Note 3. Use G_B application environment for equipment mounted in temperature controlled compartments and G_F for uncontrolled compartments.

Table I-5

Diurnal Cycle Temperature Range

REGIONAL SURFACE CLIMATIC TYPE			DIURNAL ΔT, °C
Basic	Hot		13
	Cold		11
	Constant High Humidity		0
	Variable High Humidity		9
	Cold-Wet		10
Hot	Dry		17
	Humid		10
Cold			9
Severe Cold			0
World Wide Long Term High Temperature Extremes		10 yr.	20
		20 yr.	21
		30 yr.	22

REFERENCES

[1] E. Edwards, J. Steinkirchner, S. Flint, "Avionic Environmental Factors for MIL-HDBK-217", Rome Air Development Center, U.S. Air Force, RADC-TR-81-374, Figure 3-5.

[2] "Minutes of the Surface Mount Solder Joint Reliability Task Group Meeting" dated 31 July/1 August 1989; Institute for Interconnecting and Packaging Electronic Circuits (IPC).

[3] "Climatic Information to Determine Design and Test Requirements for Military Systems and Equipment", MIL-STD-210C, 9 January 1987.

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