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Microsensors find applications in many important areas of U.S. military hardware. Advances in aircraft and internal combustion engines are placing increasing demands on the electronics which play an increasingly important role in engine control. Complexity of control circuits has demanded increases in the scale of integration and in reliability, and have suggested the placement of high levels of functionality near the point of use. Engine performance must be evaluated with sensors and used intelligently to maintain optimum efficiency. Recent advances in microsensor technology have provided smaller, more economical sensors for these applications. With smaller sensors the need for signal conditioning electronics in close proximity to the sensor has become an increasingly important issue.

The proposed three-phase project addresses the development of smart sensors for applications under high temperature ambients (up to 350°C). The approach proposed here is the demonstration of the usefulness of the SOI material obtained by the Isolated Silicon Epitaxy (ISE) process for high temperature sensor applications. This would couple with process development of sensor elements. RNC

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SMART MICROSENSORS FOR HIGH TEMPERATURE APPLICATION - PHASE I

FINAL REPORT

DR. PAUL M. ZAVRACKY

JUNE 28, 1990

U. S. ARMY RESEARCH OFFICE

CONTRACT NO. DAAL03-89-C-0024

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I. EXECUTIVE SUMMARY

Pressure Sensors fabricated in SOI materials offer significant advantages over existing technologies including:

1. High Temperature Operation.
2. At least two orders of magnitude decrease in diaphragm size with equivalent sensitive to conventional backetch silicon devices.
3. 10 x lower cost with greater functionality.
4. Chip level integration with high temperature SOI electronics.

A Phase I SBIR was awarded to Kopin Corporation, of Taunton, Massachusetts to explore the application of ISE SOI processing techniques in this important field.

The goal of this program was to establish the feasibility of creating high temperature smart microsensors in ISE SOI material. Demonstration of feasibility concerned the evaluation of stress in the layers and the questions of whether a fabrication technique could be developed which would be capable of yielding free beams, bridges, and diaphragms. In Phase I, all of the above concerns were eliminated and successful processing of micromechanical structures ensued. Examples of these structures are shown in the Figures 2 thru 5. Figure 1 shows the processing sequence used to generate these devices and is summarized as follows. A bulk silicon wafer was oxidized to a thickness of 2 μm. Subsequently, a deposited silicon oxide layer was grown. The total oxide thickness now measured 3μm. This oxide was patterned to define the base regions of the various structures. Polysilicon was deposited and capped in the usual ISE process sequence. The poly was then recrystallized in a production ISE system. After the cap was removed, the single crystal epitaxial layer was patterned to define the mechanical structures. The 3μm oxide layer was then chemically etched away leaving an air gap between the mechanical structures and the original substrate surface.

Figure 2 shows free standing beam structures. These beams have been fabricated in ISE epitaxial layers and are therefore single crystal silicon. Their bases are attached to the silicon substrate and their free ends are approximately 3μm off the substrate surface. Beams such as these can be used for accelerometer.

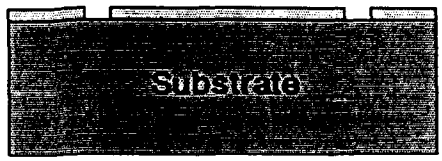
Figure 3 shows a number of bridge structures. These particular bridges were fabricated with slots through their centers. Such structures are ideal candidates for resonant mechanical sensor applications.

Figure 4 shows a topview of a portion of a 0.6 mm x 0.6mm x 1.0μm diaphragm. A cross-section of the center of a silicon diaphragm is shown in Figure 5. Diaphragms such as these could be used for pressure sensor applications.

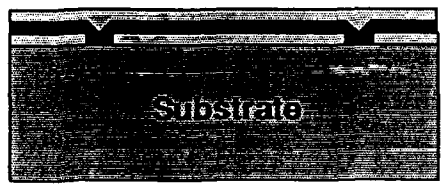
This successful Phase I SBIR program has demonstrated a potential for high temperature silicon sensors with the good electrical and mechanical properties of single crystal silicon. The piezoresistive effect in silicon which has been exploited for years in accelerometer and pressure sensor applications is not sacrificed in the process. A new and exciting approach for the reduction in the size of current silicon sensor technology has been established. An important aspect of this achievement stems from the fact that SOI materials have recently demonstrated an extended operational temperature range in CMOS circuits (to 300°C and beyond). For the first time a clear path to high temperature smart silicon sensors has been realized.

A Phase II proposal promises to exploit the technology and develop a high temperature smart microsensor. This device will contain multiple diaphragms and the circuitry to provide fault tolerance, redundancy, and rangeability. The completed device will communicate with the world in digital format to significantly improve it noise immunity. The successful completion of this program has broad application in the defense and commercial arenas.

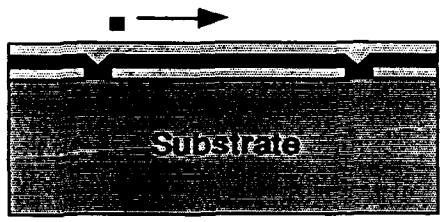
Oxidize and pattern wafer to define regions for the bases of the beam structures.



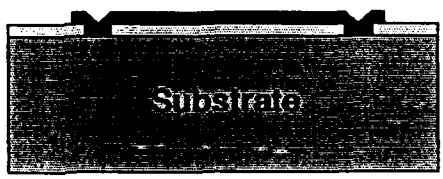
Deposit polysilicon and capping layer over entire wafer.



Recrystallize the polysilicon layer, forming a single crystal silicon film over the entire wafer.



Pattern Single Crystal Silicon film to define beam structure.



Etch oxide from beneath single crystal silicon film to complete beam structure.

Figure 1

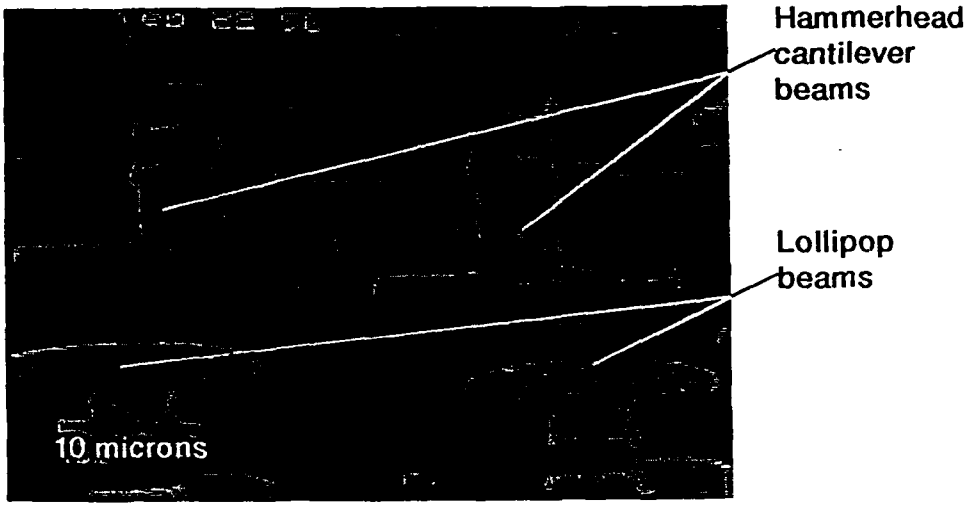


Figure 2

This picture shows free cantilever beams fabricated using in SOI material using the ISE process. The beams are separated from the substrate by about 3 microns. Structures like these would be useful in accelerometer applications.

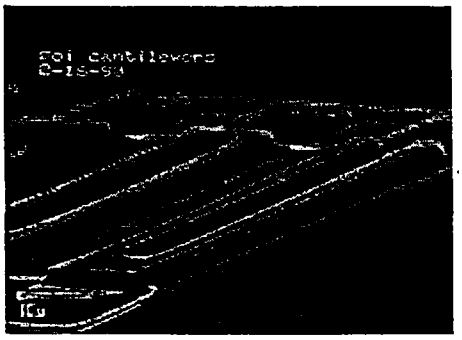
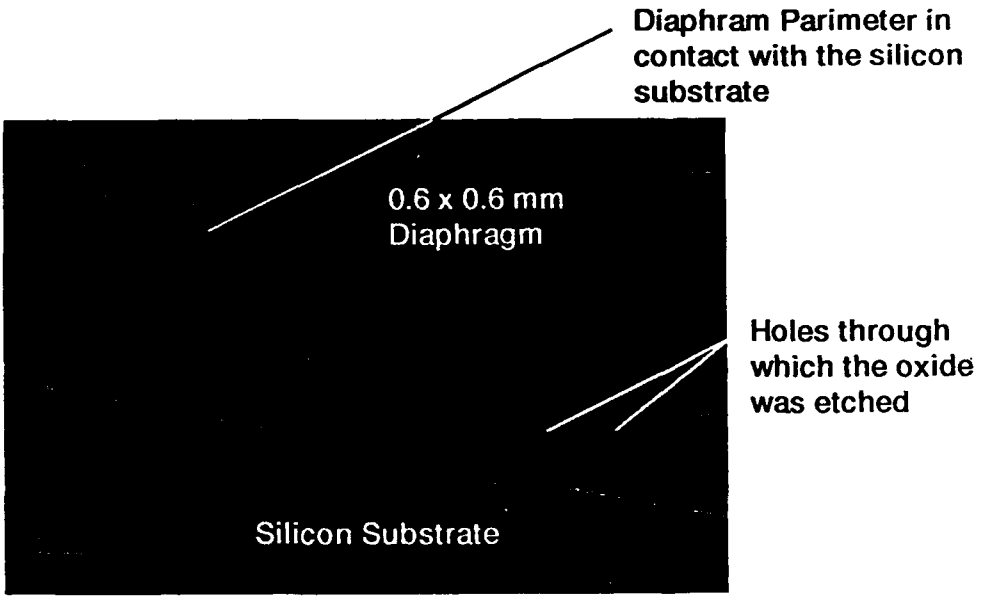


Figure 3


Diaphram Parimeter in contact with the silicon substrate
0.6 x 0.6 mm Diaphragm
Holes through which the oxide was etched
Silicon Substrate

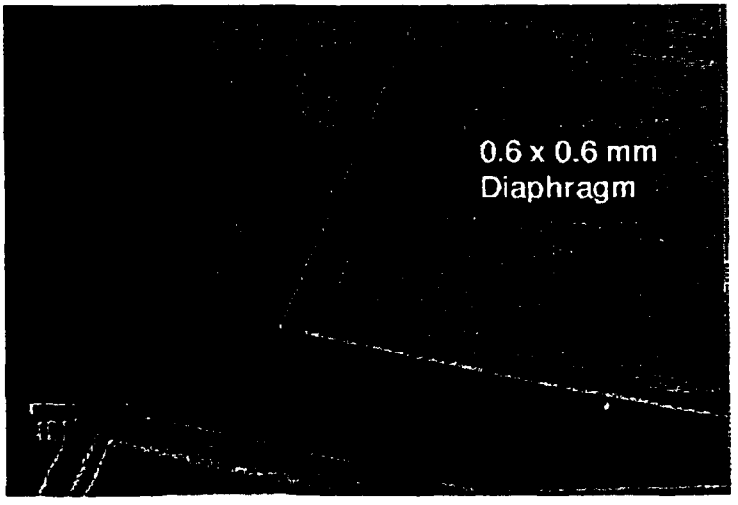

0.6 x 0.6 mm Diaphragm

Figure 4

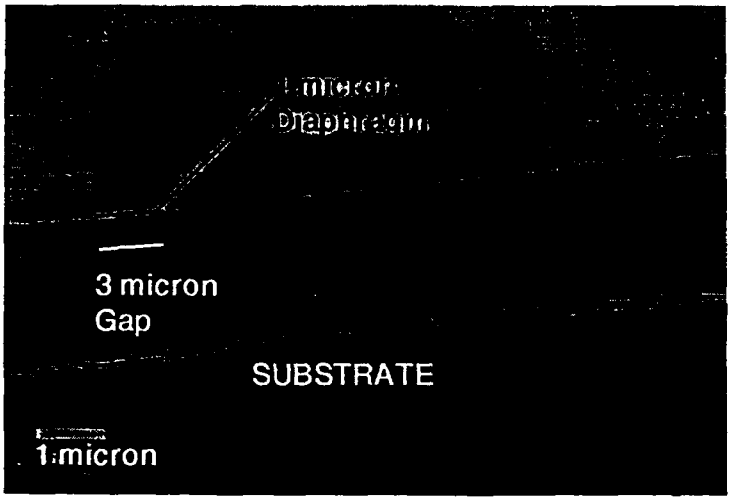


Figure 5

The center of a 0.6 mm x 0.6 mm diaphragm is shown. The diaphragm, which is single crystal silicon, has been created in ISE SOI material with a 3 micron initial oxide. The oxide has been completely etched away leaving a freely suspended silicon diaphragm. These structures have applications in pressure sensors.

II. RESULTS OF PHASE I

2.1 Introduction

During Phase I, Kopin successfully demonstrated the feasibility of using the ISE process to fabricate micromechanical devices. During this phase the following microstructures were demonstrated.

TABLE 1
MECHANICAL STRUCTURES DEMONSTRATED IN ISE
(All Structures are Single Crystal Silicon)

1. Cantilever Beams.

2. Bridges.

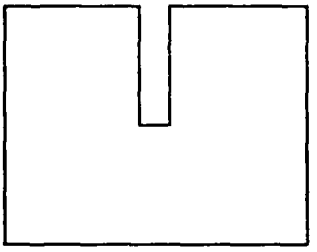
3. Diaphragms.

With the microstructures demonstrated above the objectives of Phase II are realizeable. The following section details the objectives and achievements of the Phase I effort. We conclude from this work that a Phase II program will have a high probability of success.

2.2 Phase I Technical Objectives

The goal of this three phase program is the development of smart high temperature microsensors ISE technology has on inherent flexibility that allows a designer to vary the process in order to easily obtain structures that would be difficult to achieve in other technologies. This can be visualize with the following example. Cantilever beams can be fabricated by simply etching the silicon into the pattern illustrated below.

Cantilever Pattern



This shape represents the area where the ISE film is to be etch off the underlying oxide. When exposed to an HF etchant, the silicon oxide around and beneath the beam will be etched away. The oxide etching continues until the silicon cantilever section is completely undercut. Kopin had performed initial experiments on this simple idea with the results are shown in Figure 6. As can be seen in this SEM photograph, the silicon cantilever is completely separated from the underlying silicon substrate. An unfortunate drawback of this technique is that the surrounding silicon film has also been undercut. This would most certainly effect the performance of this structure if it were to be used as a resonant sensor, for instance. However, the result does demonstrates how easily mechanical structures can be obtained. During the Phase I project, a two level process was developed. This process overcame the previous problem by allowing us to pattern the oxide ahead of time. In this way, silicon cantilevers were fabricated such that their bases were directly connected to the substrate. In this case, all the oxide was removed from around the beam and the beams were completely isolated. Such a simple structure would have immediate application in accelermeters.

The overall objective of Phase I was concerned with establishing the feasibility of fabricating high temperature microsensors in ISE SOI material. The specific objectives of each task are summarized in Table 2.

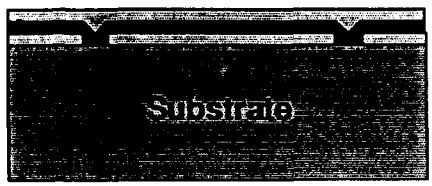
TABLE 2
GOALS OF PHASE I

ESTABLISH FEASIBILITY OF FABRICATING HIGH TEMPERATURE MICROSENSORS

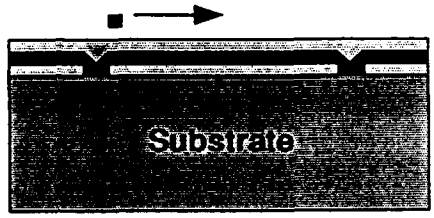
Task	Objective
1. Identification of Processing Flows.	To identify key process techniques required for the fabrication of microsensor devices and specially for the creation of free standing beams and diaphragms.
2. Evaluation of Processing Techniques	The evaluation of the processing techniques described above through the use of simple test structures using available existing mask sets, if possible.
3. Analysis of Results.	After fabricating the test structures above, an analysis of the success of the fabrication techniques will be conducted and alternative or improve techniques will be proposed for Phase II.
4. Identification of Problem Areas.	Any problem areas will be identified and examined for their impact on the project objectives. A Phase II research plan will be formulated.
5. Reports	Document the Phase I research findings.

Oxidize and pattern wafer to define regions for the bases of the beam structures.

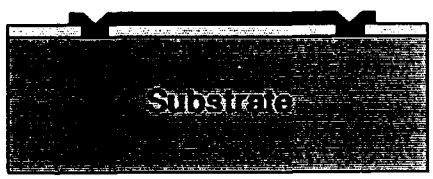
Deposit polysilicon and capping layer over entire wafer.



Recrystallize the polysilicon layer, forming a single crystal silicon film over the entire wafer.



Pattern Single Crystal Silicon film to define beam structure.



Etch oxide from beneath single crystal silicon film to complete beam structure.

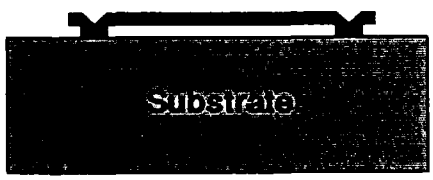


Figure 6

Beam Process

III. SUMMARY OF FINDINGS

3.1 Task 1: Identification of Process Flows

Process techniques need to be developed which can be used to fabricate free standing structures, specifically beams and diaphragms. Beam structures can be used to evaluate the built in stresses in the ISE epitaxial layers.

In Figure 6, a simple process for producing free standing single crystal silicon beams is shown. In this process, the oxide is first etched to define openings which will allow the subsequent deposited polysilicon layer to contact the substrate. The wafer then undergoes normal ISE processing which would include depositing a cap oxide, crystallizing the poly layer and stripping off the cap. At this point, the now single crystal silicon film will be contacting the silicon substrate in all regions where the oxide layer had been cut. Next, the silicon will be patterned to define the beams. Naturally, the base of the cantilever beam structure would be the point at which the silicon epitaxial layer contacts the substrate. Beams could be fabricated as double ended structures or as single ended structures. A simple two level mask set was designed which allowed the implementation of this process sequence.

A similar process can be used to create single crystal silicon diaphragms as shown in Figure 7. In this case, the oxide is cut to define the perimeter of the diaphragm. The substrate is then re-oxidized with only 1000Å or 2000Å angstroms of oxide. This oxide is then re-patterned and etched in small regions where the silicon epi is to contact the substrate. Again, the ISE process proceeds as usual through recrystallization and cap stripping. At this point, the now single crystal silicon is patterned and etched to define the diaphragms. Each diaphragm will be supported by the underlying oxide layer. The edge of the diaphragm is touching the substrate at the points were the second oxide was cut, but elsewhere around the perimeter is separated from the substrate by a thin oxide layer. As has been shown by Henry Guckel, et al, at the University of Wisconsin, the oxide under the diaphragm can be removed by chemical etching in concentrated HF. After the etching is completed, the HF drips out from under the diaphragms aided by surface tension (de-wetting). A final step in this process is to refill the gaps left under the edges of the diaphragm. This can be accomplished by oxidizing the wafer. The oxide will then grow together and seal the opening.

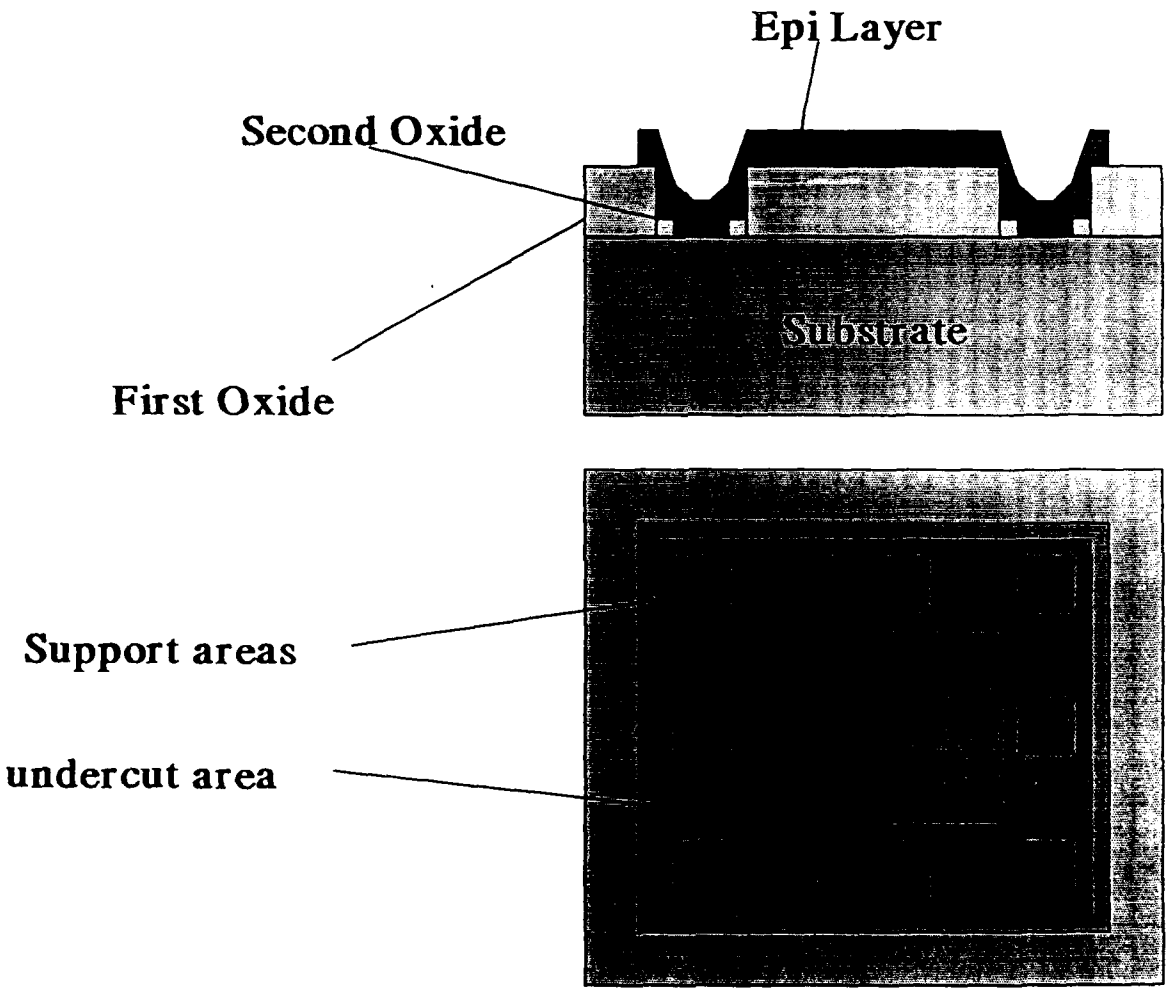


Figure 7

Diaphragm Process 1

A final process for diaphragm fabrication which was chosen is shown in Figure 8. Here oxide is patterned only once, to the perimeter of the diaphragm, and the poly is allowed to contact the silicon around the entire perimeter. The ISE process again proceeds as usual through the stripping of the capping layer. This time, the poly is pattered with tiny holes just inside the perimeter of the diaphragm. These holes are then used for the entrance and exit of the HF in a similar manner as has been previously discussed.

During the Phase I contract period, we completed the design of a mask set for fabricating silicon diaphragms. Figure 9 shows an composite view of the mask set. The process for generating diaphragms is shown in the Table 3.

3.2 Task 2: Evaluation of Processing Techniques

Process techniques described above were implemented during the course of Phase I contract. Mechanical structures including various types of beams have been demonstrated. The Phase I SBIR proposal calls for the determination of the adequacy of process flows described above.

During Phase I, wafers were prepared in the following manner. Prime silicon wafers from Monsanto were thermally oxidized to a thickness of approximately 1μm. These wafers were then photolithographically patterned to a mask which opened holes where the base of the beam would finally reside. Polysilicon and a capping oxide were deposited and the wafers were recrystallized using standard production techniques. The cap was subsequently removed and the polysilicon was photolithographically patterned to the beam mask. Beams were aligned to the previously defined holes in the oxide. The silicon film was then etched using a nitric/HF solution commonly used for polysilicon etching. The underlying oxide was then removed using a concentrated HF solution at room temperature for 30 minutes. This period was sufficient to completely undercut the silicon beam structures. Wafers were then washed in DI water and dipped in Isopropyl Alcohol (IPA) for 1 min. The IPA was evaporated in an oven at 100° C for 60 minutes.

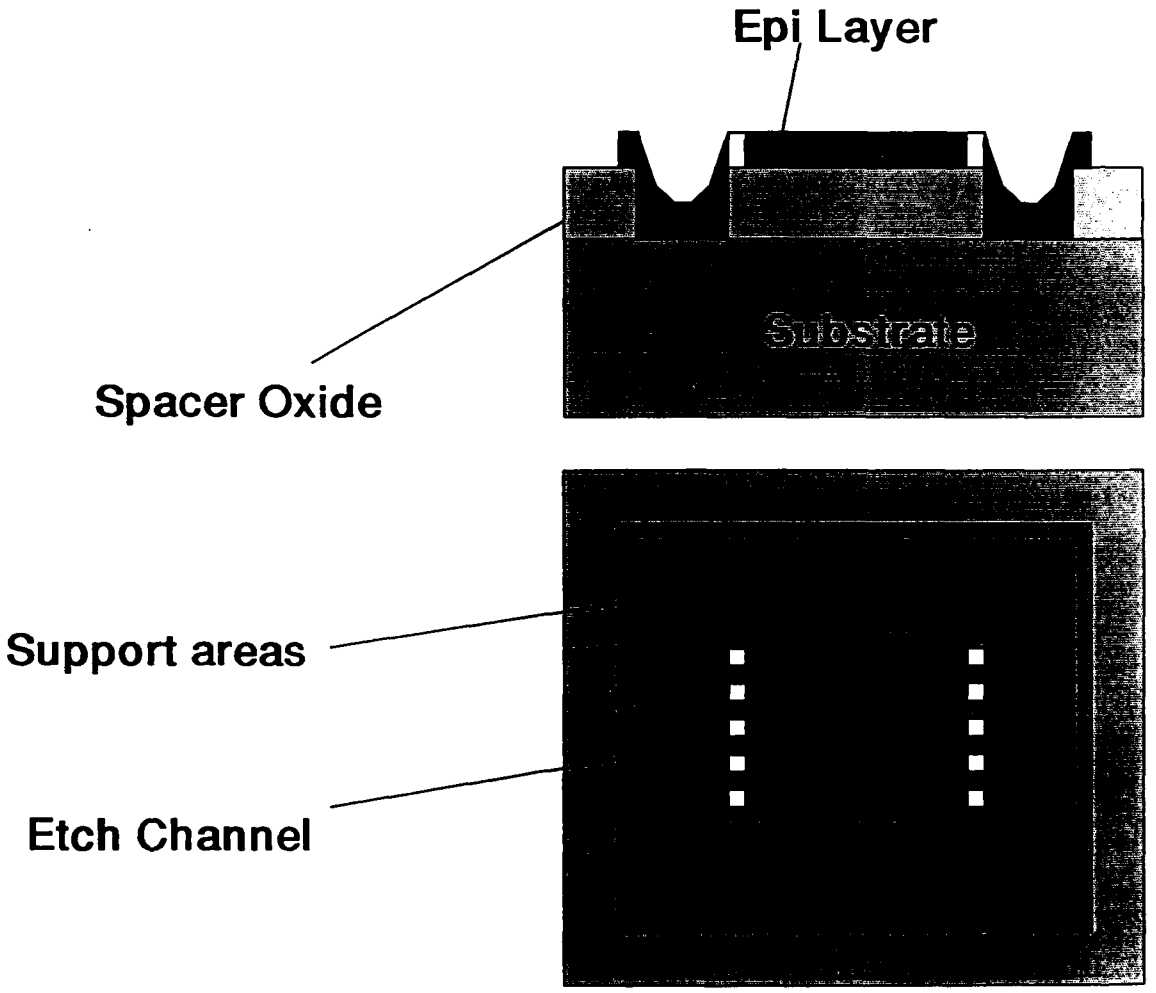


Figure 8

Diaphragm Process 2

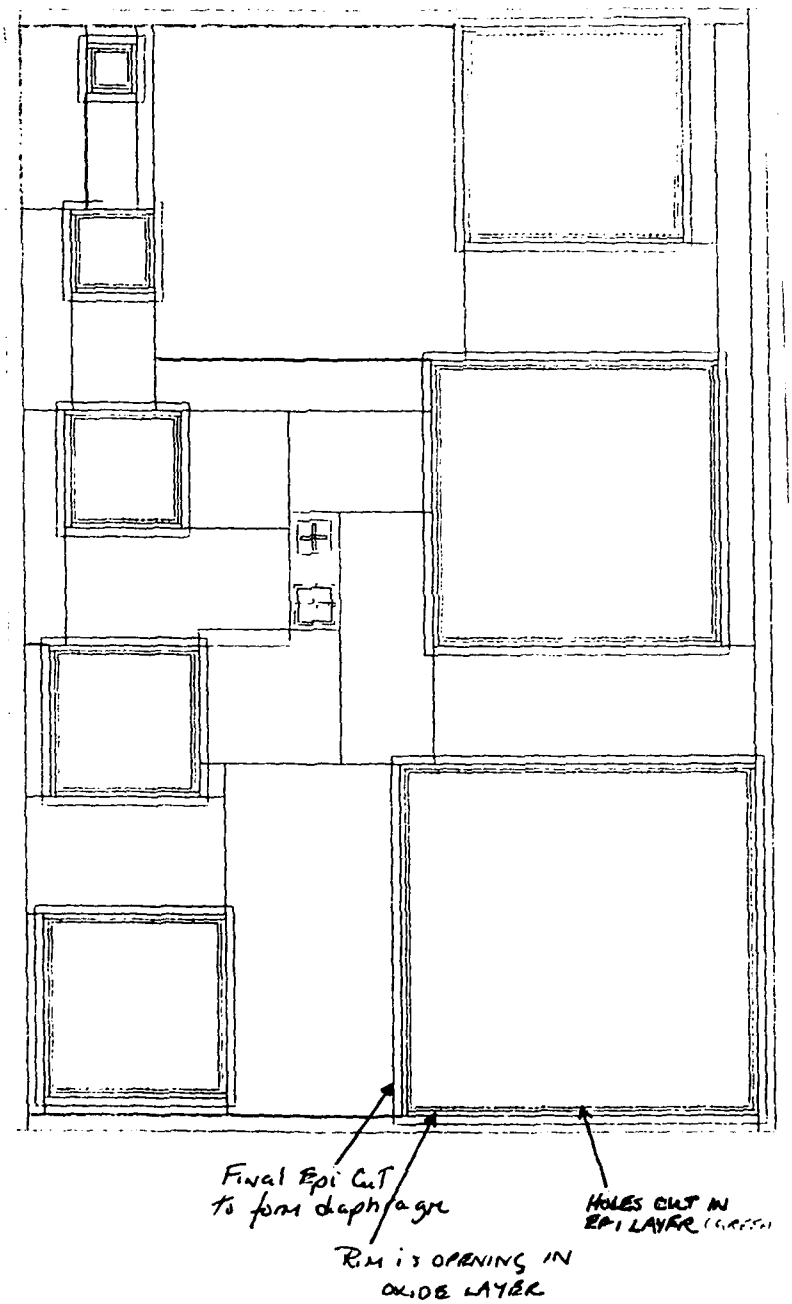


Figure 9

Composite View of the Mask Set

TABLE 3
DIAPHRAGM PROCESS

1. Deposit a thick silicon oxide layer (3μm).
2. Pattern oxide with grooves that run around the periphery of the area upon which the diaphragm will be created. This effectively will leave a square post of oxide surrounded by a trench.
3. Deposit polysilicon and proceed with normal ISE processing.
4. Pattern the silicon with holes that align to the edges of the diaphragms.
5. Etch the underlying oxide with HF through the holes in the silicon epitaxial layer.
6. Seal the holes with a subsequent polysilicon or CVD oxide deposition.

Photographic results are shown in Figures 10 and 11. As can be seen in Figure 10, the beam has indeed been completely undercut by the HF etching. This picture was taken with an SEM after cleaving the silicon die in half and locating a beam structure near the cleaved edge. This particular beam was designed with holes in its length, one of which is indicated in the picture. Also apparent is the fact the beam is dropping toward the substrate as it extends away from its base. This is shown more clearly in the optical micrograph of Figure 11. In this figure, a series of beams of differing lengths is shown. Interferences fringes are visible for a portion of each beam near the base. These are caused by light which is reflected by the underside of the beam and the substrate beneath it. When the beam and the substrate come into contact the interference pattern disappears. The shortest beam in the photograph is found to be completely free of the substrate.

Examination of the curvature of some of the beams suggested that the problem was related to electrochemical forces as described in the Phase I proposal. These forces can cause the beams to collapse onto the substrate during etching and cleaning. Figure 12 shows an outstanding example. In this photograph two beams are visible. These particular beams have ends that form large circular areas. In order to picture this more clearly, a copy of the silicon mask level (Figure 13). The two beams

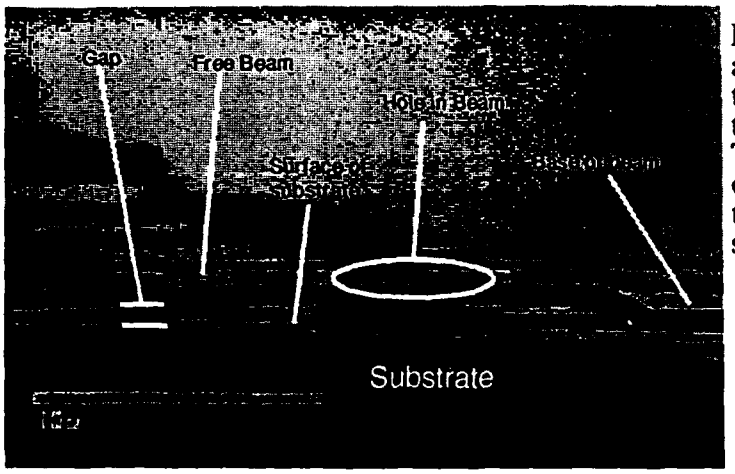


Figure 10 Side view a cantilever structure is shown in this SEM photograph. The beam slopes downward and eventually touches the substrate.

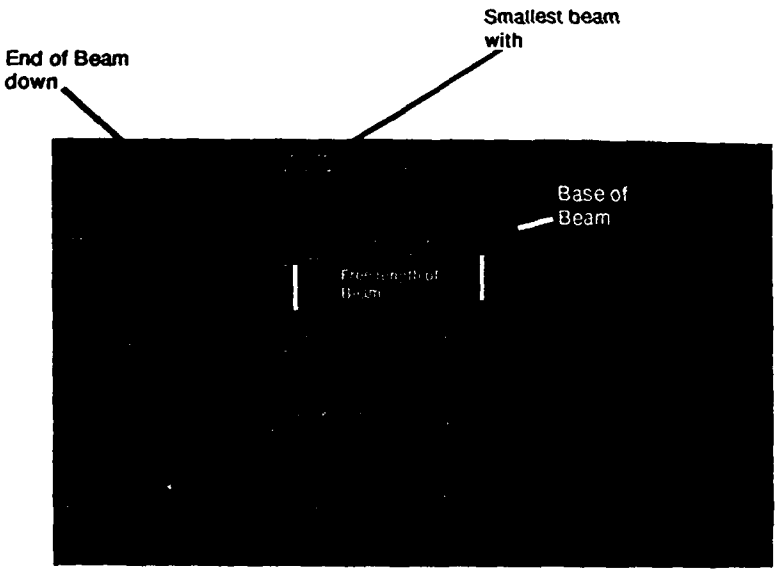


Figure 11 Optical Micrograph of cantilever structures. The interference fringes show that the smallest beam is the only one that is free of the substrate.

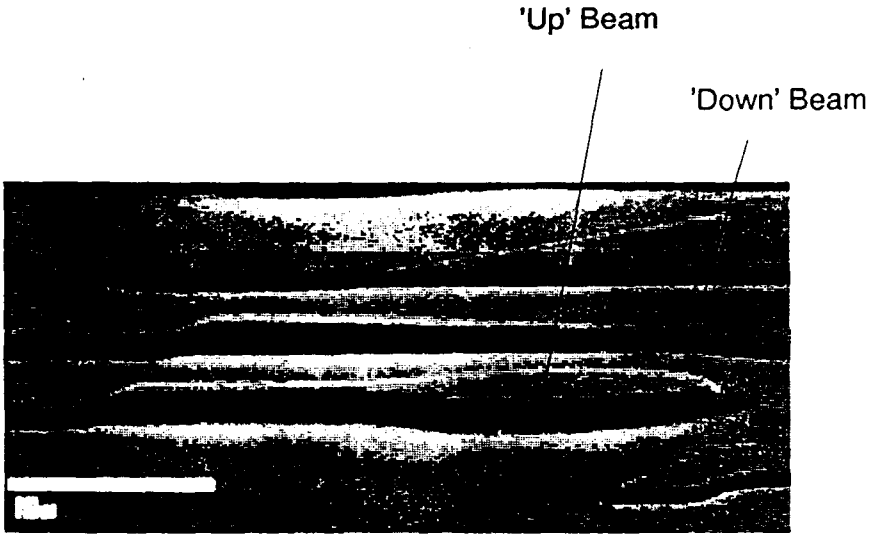


Figure 12

Two beams are shown in this semi photograph. The closer one is up off the substrate and therefore 'free'. The second one is stuck down in the substrate. Looking at the curvature closely, the 'free' beam is flat and straight indicating no built in stresses.

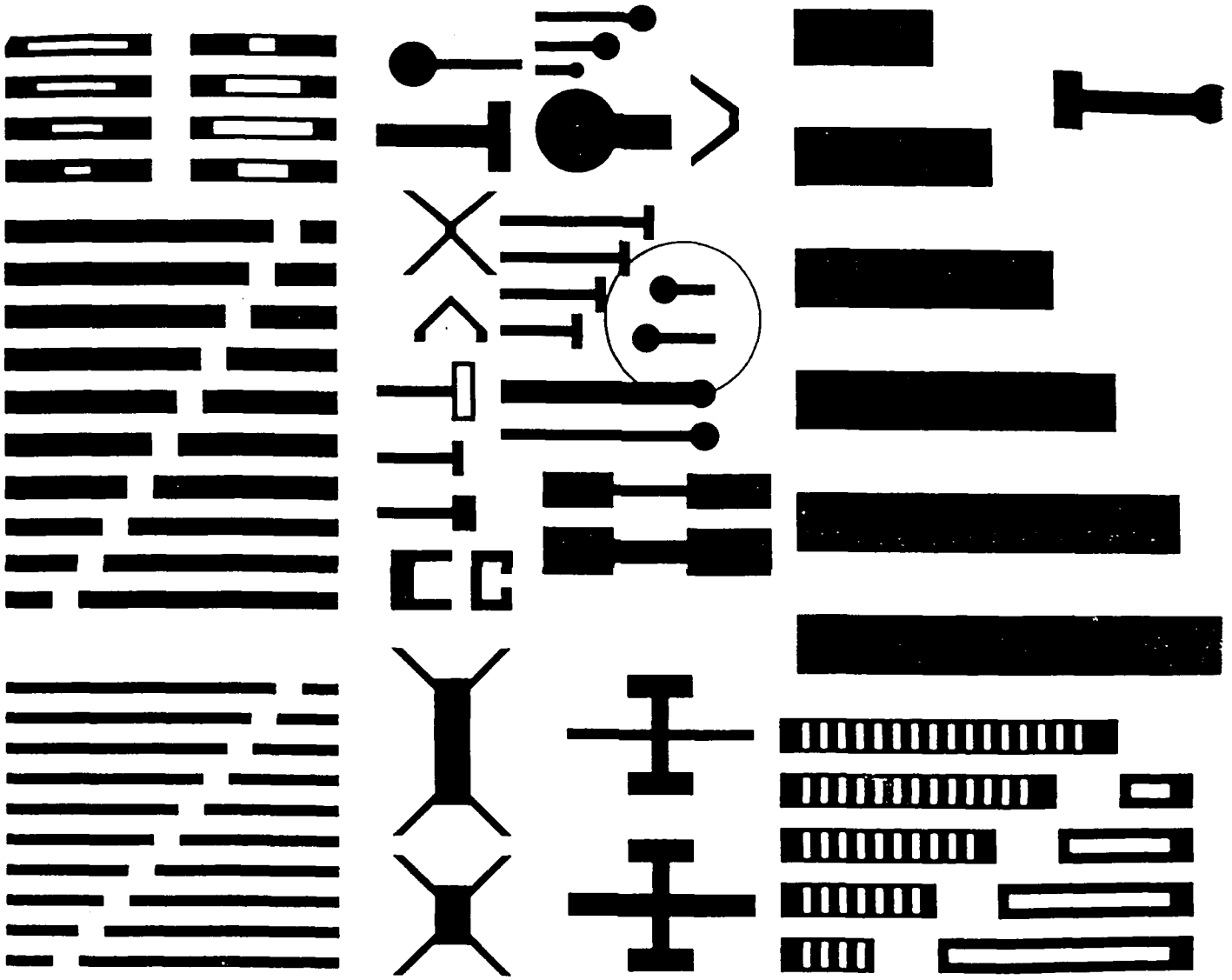


Figure 13

Silicon Mask Level

circled are the ones shown in the SEM micrograph of Figure 12. What is observed is that one beam is down and the other is up. The fact that one is up suggests strongly that silicon film stress is not causing the second beam to be stuck down.

It occurred to us that the sticking problem may be related to the surface tension of the liquid used just prior to drying. After examination of available literature, it was found that Alcohols have significantly lower surface tension than water (73 dynes/cm for water as compared to 24 for Isopropyl alcohol). We tested alcohol using the following process sequence listed in the Table 4.

TABLE 4
DRYING SEQUENCE

1. Dilute HF with water without removing wafers.
2. Dilute water with Isopropyl Alcohol without removing wafers.
3. Remove wafers from Isopropyl Alcohol and dry.

Before testing this sequence, a third lot of bridges and cantilevers was fabricated along with a first lot of diaphragms. The diaphragm mask contains 8 different size diaphragms ranging in size from .1 mm on a side to 1 mm on a side. With such large structures, one would anticipate a low yield based on the results presented above. In order to optimize our chances for success, a 3μm lower oxide was chosen. With this larger gap and the final drying technique, we hoped to obtain some yield. In fact, as will be shown, we obtained good yield on diaphragms (>90%) as large as 0.6 mm on a side.

3.3 Task 3 Analysis of Results

Figure 14 shows examples of cantilever beam structures fabri cated using the process described previously. The beams are at tached to the silicon substrate at their bases and project out 3μm above the substrate. Beam shapes were chosen to match shapes that might be used for accelerometer applications, where extra mass would be deposited on the end of the beam. Figure 15 shows a number of slotted bridge structures. This type of structure has resonant properties similar to a tuning fork. If the tines were excited in the plane of the wafer, the stresses induced at the crotch would balance, and energy loss out to the support would be minimized.

The mask set (See Figure 13) used to produce these structures also has a pattern consisting of 10 beams and bridges ranging in length from 10 m to 100 m in steps of 10 m. These structures are useful in determining the stress in the film. On examining the wafers produced from this lot, it was found that all the bridges were free standing. The beams from 60μm down were free standing while those above 60μm were down on the substrate. This can be seen in the micrograph of Figure 16. The microscope was focused on the substrate, so any features out of focus are free while those in focus are down on the substrate. On this particular grouping, the 50μm beam is down, while the 60μm beam is up. This suggests that the cause for the down beams is not stress related, but process related. As indicated earlier, variations in our process did improve the numbers of free beams.

Very encouraging results were obtained on the diaphragm structures. Figure 17 shows a top SEM view of a 0.6mm x 0.6mm x 1μm diaphragm. The perimeter of the diaphragm is in contact with the silicon. Holes were etched through the diaphragm around its edge in such a way that the oxide could be etched out from beneath the diaphragm in order to free it. Figure 18 shows an SEM cross-section of the center of a similar diaphragm. As is clearly seen, the diaphragm is freely supported above the silicon substrate.

3.4 Task 4: Identification of Problem Areas

During the course of this Phase I effort, no significant problems arose in the fabrication of micromechanical structures in ISE SOI films.

IV. CONCLUSIONS

Our initial concern about creating free micromechanical structures was studied during Phase I of this program. Based on the results obtained on cantilever beams, it appears that this may be a valid concern. For bridges and diaphragms, however, the problem does not exist, even for diaphragms as large as 0.6mm x 0.6mm. In Phase II, we will propose a program to develop smart high temperature pressure sensors. In this application, the results presented on SOI diaphragms suggest a high probability of success. A typical silicon back-etched diaphragm designed for 0 - 30 psi, would typically be about 25 μm thick and have a linear dimension of approximately 2 or 3 mms. The sensitivity of a diaphragm sensor is proportional to the square of its thickness and approximately proportional to the square of the linear dimension of the device. Therefore, a 1μm diaphragm is roughly equivalent sensitivity, would have a linear dimension of only 0.014 mm on a side! Based on this analysis there appears to be a tremendous latitude for successful fabrication of very sensitive pressure sensors using the proposed approach.

Our analysis of the process for creating bridges and diaphragms suggests that even for low pressure sensors, in the range 0-32 psi, a high yield can be expected. As has been shown, >90% of the 600 μm x 600 μm diaphragms were free standing. Since a 0-32 psi sensor requires a 14 μm x 14 μm diaphragm, the yield of good mechanical components can be expected to be nearly 100%. Pressure sensors designed for higher pressure ranges will require smaller diaphragms. We, therefore, anticipate no difficulty in successfully fabricating high pressure sensors.

A reduction in diaphragm size provides significant advantages over conventional back-etched bulk technology. Firstly, the die size can be reduced. A diaphragm of only 14 μm on a side is considerably smaller than the required wire bond pads (typically 100 μm on a side). For a piezo resistive sensor, 6 bond pads are normally used. The minimum die size is, therefore, 200 μm x 300 μm = 0.2mm x 0.3mm or approximately one tenth the size of a conventional bulk back etched 32psi pressure sensor. Secondly, yield can be improved with redundancy. Several 14 μm sensors could be placed on a single die with minimal increase in die area. These could be tested and the best device could be chosen for bonding. In a similar way, a range of diaphragm sizes could be fabricated on a single die. A single die would satisfy the needs of several pressure ranges and products. At packaging, a particular device would be bonded out in accordance with sales requirements, or a special package with higher pin count could be used to cover multiple pressure ranges.

The above discussion addresses the successful completion of a Phase I SBIR program which demonstrated micromechanical structures suitable for sensor application. It also addresses the size advantage of this technology relative to bulk.

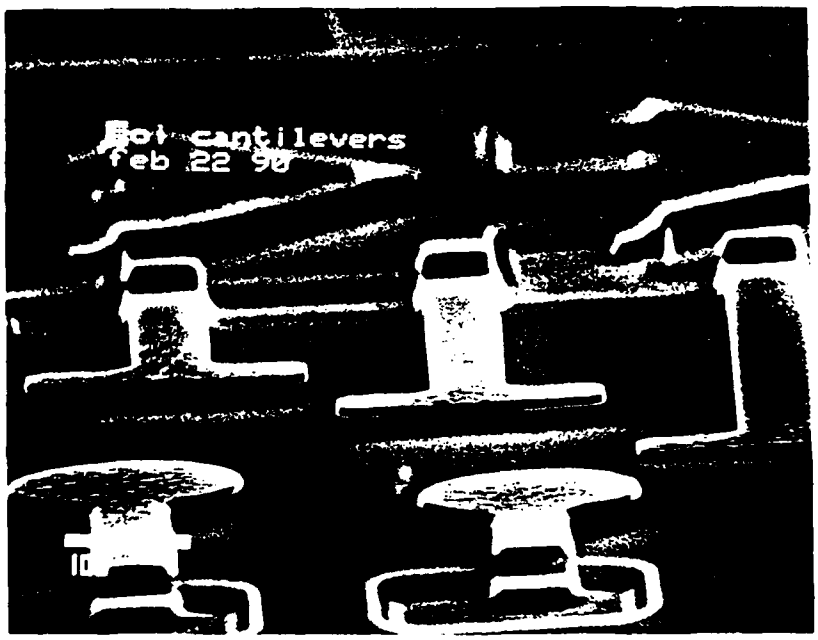


Figure 14

Cantilever Beam Structure

This picture shows free cantilever beams fabricated using in SOI material using the ISE Process. The beams are separated from the substrate by about 3 microns. Structures like these would be useful in accelerometer applications.

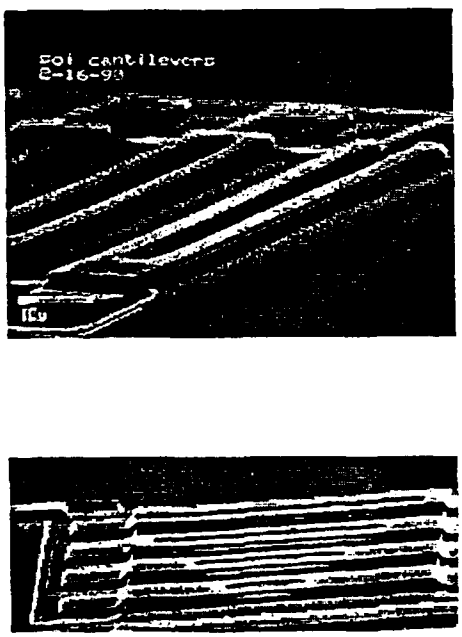


Figure 15

Slotted Bridge Structures

The bridge structures shown above were created in ISE SOI material. Each structure has a slot through its center. These types of structures could be very useful for resonant sensor applications.

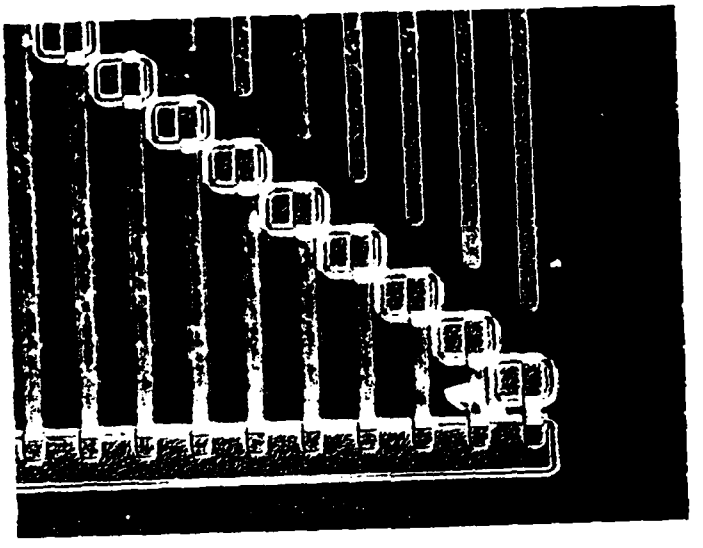


Figure 16

Micrograph of Bridge and Beam Array

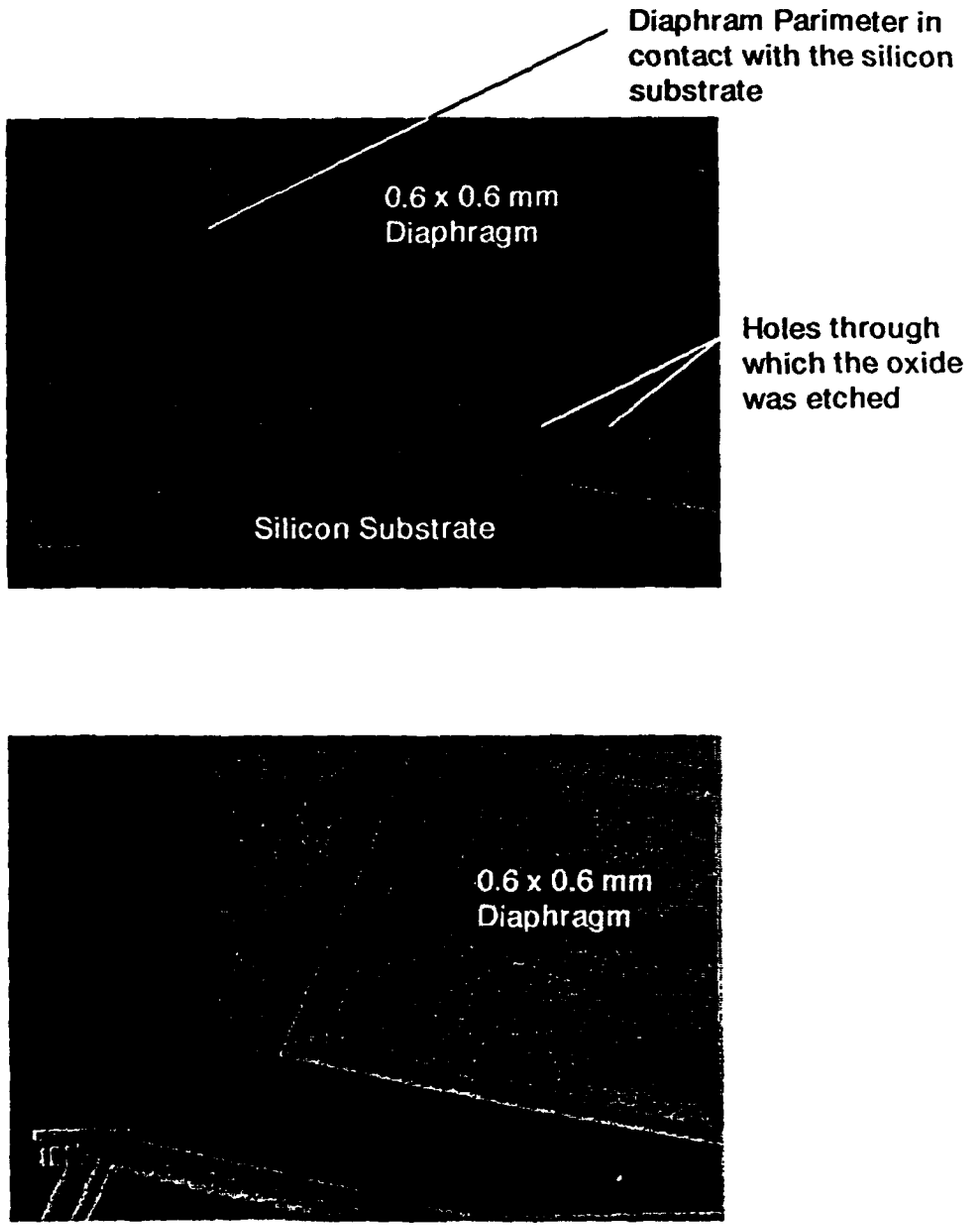


Figure 17

Top SEM View of a 0.6 mm x 0.6mm x 1μm Diaphragm

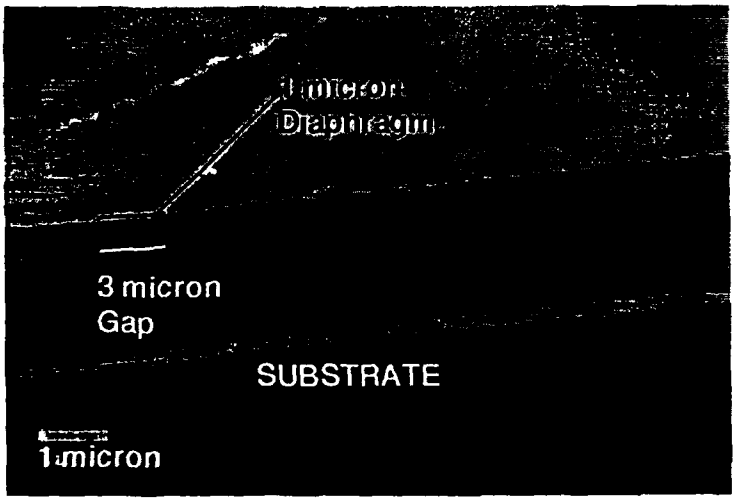


Figure 18

SEM View of a 0.6 mm x 0.6mm x 1μm Diaphragm

The center of a 0.6 mm x 0.6mm diaphragm is shown. The diaphragm, which is single crystal silicon, has been created in ISE SOI material with a .3 micron initial oxide. The oxide has been completely etched away leaving a freely suspended silicon diaphragm. These structures have applications in pressure sensor.