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14th Annual Electronics Manufacturing Seminar Proceedings

Sponsored by
Electronics Manufacturing Productivity Facility
and
Soldering Technology Branch

21 and 22 February 1990

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CHINA LAKE, CA 93555-6001



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FOREWORD

The proceedings contained herein are compiled and published by the Engineering Department, Naval Weapons Center, as supporting documentation for the 14th Annual Electronics Manufacturing Seminar to be held on 21 and 22 February 1990 at NWC, China Lake, Calif. This document is a compilation of information that was provided by both nongovernment and government sources.

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January 1990

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 IPA extraction technique
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 Military electronics
 Printed circuit board solderability
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INTRODUCTION

The ever-changing, fast-paced technological advances being made today in electronics manufacturing present a challenge to us all. To help meet this challenge, we must work together. This Seminar—the 14th Annual Electronics Manufacturing Seminar—gives us an excellent opportunity to do just that. This Seminar promotes an open exchange of information on all issues of electronics manufacturing. It provides a forum for all persons involved in this technology, whether from government, industry, or academia. Here we can openly discuss these issues and share our ideas. Here we can work together toward our common goal: to improve the U.S. electronics industrial base.

To help make this improvement we must continue to work toward the goals of productivity, producibility, and quality. We must maintain a concerted effort to resolve production-line problems. Then, we must develop process controls and methods to solve them. Because productivity, producibility, and quality are inseparable, it is critical that our designers learn from past problems and that they design for ease of manufacturing. The Navy is continuing to work with industry through the efforts of the Electronics Manufacturing Productivity Facility (EMPF) and the Naval Weapons Center Soldering Technology Branch.

The Soldering Technology Branch is continually working to ensure that we meet the goals of producibility and quality. We evaluate soldering requirements and provide these evaluations to government and industry facilities. The Navy's work to consolidate its soldering requirements has resulted in WS-6536E, and we are continuing to work with DOD-STD-2000.

Another approach to improve our electronics industrial base is coordinated by the Naval Industrial Resources Support Activity (NAVIRSA) Detachment EMPF. The EMPF is leading the cooperative effort between electronic equipment manufacturers, product manufacturers, and government agencies to research, develop, and demonstrate electronics manufacturing processes and materials. The EMPF coordinates the cooperative work of these groups to develop high-quality processes and to demonstrate manufacturing disciplines in a production environment. The EMPF documents this cooperative work and develops an accessible information source for electronics manufacturing productivity. Our goal is to gain information, share information, and use information to help produce high-quality products at lower cost in less time.

We are indeed looking forward to working with you to improve our electronics industrial base.

We appreciate your interest in electronics manufacturing and thank you for joining us at this Seminar.

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**STANDARD ELECTRONIC CIRCUIT CARD ASSEMBLY SYSTEM
(SECAS PROJECT)**

by

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ABSTRACT

In May of 1988, the company embarked on a program to standardize and automate the processes of Circuit Card Assembly. A three phase plan, extending through 1993, was presented to management by the process engineering group, and given approval. The subject of this paper is the execution and completion of Phase I, the automation of surface mounted "flatpack" I.C. preparation, kitting, and assembly.

Initial project steps involved the development of a new strategy for SMT device packaging. The "old method", including considerable manual handling and storage of parts in "waffle trays", caused sufficient part damage to require considerable re-forming and "tweaking" of individual leads just to create acceptable hand soldered joints. While it was evident that a "mass reflow" process offered the greatest cost savings of the project, greatly improved device handling methods had to be implemented before anything other than hand soldering could be considered.

The "new method" utilized recyclable plastic device carriers in combination with aluminum tubes to protect the devices and feed them to the new equipment. This change in combination with developing the capability to screen solder paste onto a circuit card; use of a vision-assisted pick+place machine to mount parts; and an in-line oven to mass reflow solder, made this new process possible. In addition, heater-bar soldering technology was developed to attach surface mounted IC's to the bottom side of the circuit cards (after wave soldering).

Several major processing issues were addressed during the implementation of the project:

1) WS-6536 requirements for component body-to-board stand-off height were addressed by the implementation of floating-anvil forming dies. Hands-off part feeding and carrier loading was incorporated into the machine at the same time.

2) Since our new "common process flow" involved a form and trim operation AFTER tinning, each lead had exposed base metal on the toe which was challenging to solder. Developing a special solder cream with maximum "RMA" halide content and enhanced surfactants dropped non-wetting defects from 30% to less than 1%.

3) Developing computerized process controls and monitoring of the heater bar process (meeting WS-6536 and DOD-STD-2000 requirements for soldering irons) allowed us to determine optimum preheat/pressure/ temperature profiles for each part on each assembly.

RESULTS:

The current labor standard for preparation and assembly of surface-mounted IC's is 25% of the previous hand-assembly method. The performance factor (actual ass'y time/std time) has dropped from a 2.75 average to a .95 average. Thus assembly labor costs have already decreased approximately 87%, and the assembly personnel are still perfecting their techniques. The next phase of the project will be to achieve comparable results for thru-hole assembly operations.

SECAS PROJECT PHASE I

I. INTRODUCTION

Sanders manufactures several varieties of electronic countermeasures systems, with designs dating from the late 1970's to the mid 1980's. Circuit cards are primarily double sided, mixed technology designs using multilayer polyimide boards. Surface mount I.C.'s are typically used on both top and bottom sides, with wave soldered discrete and dual-in-line components on the topside. Typical product mix calls for approximately 103 different circuit cards, using 228 unique surface mounted I.C.'s. Board design, product mix, and volume were major factors in defining the scope and cost of the project.

The guiding principles behind the project plan are threefold: reduce labor costs, enhance manufacturing response time, and ensure line flexibility. When a "window of opportunity" for new business becomes available, the transition from design to assembly should be as short as possible. With this in mind, a flexible, automated circuit card assembly line was planned, where a computer-controlled routing could select the machines/processes required for each unique product.

By comparing our current assembly processes to the projected "to-be" state, a chart of Technology Needs was assembled (Figure 1). This was arranged in a decending ROI fashion, so that the areas for highest potential savings would be implemented first. Since all circuit card assembly operations (other than wave soldering) were performed manually, the list of needs was considerable. It was easy to determine that the assembly and soldering of surface mount I.C.'s should be the first process automated. A new process routing, eliminating many in-process steps, was planned. (Figure 2)

II. MATERIAL HANDLING DECISIONS

Prior to this time, a conductive plastic matrix tray, capable of holding 50 I.C.'s, was in general use for storage, kitting, sequencing, and assembly. This method, while an improvement on past practice, had a number of shortcomings: lead damage (both coplanarity and skew defects) was commonplace; part locational

tolerance was .200" x .800" within a tray partition; pin 1 orientation was not maintained; required .010" minimum part-to-board stand-off spacing was not maintained/protected.

Three technologies were evaluated for parts handling/storage for the new system:

Surface Mount Tape & Reel
Redesigned Waffle Trays
Plastic Carriers and Tubes

Milton-Ross carriers, similar to those used at IBM, Westinghouse, and Hughes first appeared to be the best choice for our volume and mix. Tape and reel packaging would require random access feeders at each assembly station, whether machine or manual. While both trays and carriers could support part sequencing or random access, it was determined that no waffle tray system could provide the lead integrity needed for totally automated assembly. During the study, we became aware of a new carrier development project. Westinghouse MAC, in conjunction with HMM Design Group, had engineered a new carrier concept to achieve several benefits: (Figure 3)

- Opening range of .080" vs. .015", thus requiring only 4 carrier sizes instead of 10 Milton-Ross sizes
- Same opening-jaw dimension regardless of carrier size, thus standardizing the feeding equipment requirements
- Higher percentage of part retention when dropped from 3-5 ft.
- 1000+ opening cycles before the I.C. is no longer safely retained, compared to 20 openings with other carriers (Reference 1)
- Protection of coplanarity, skew, and stand-off dimension
- Orientation of pin #1.

All parts currently in use could be processed in carriers with a standard outside dimension of 3/4"x1", enabling a single type of handling mechanism at all levels of the new process.

Orders were placed for the following configurations:

white 1/4 body x 16 lead
black 1/4 body x 20 lead
gray 5/16 body x 20 lead
blue 3/8 body x 24 lead

At the same time, 18" long aluminum magazines were ordered, which would be capable of containing up to 100 carriers. (Reference 2)

A major step in any automation project is to standardize processes and routings whenever possible. To enable our project

to go forward, a "Common Flatpack Process Flow" was implemented across all contracts and programs. (Figure 4)

To begin the transition from matrix trays, pneumatically operated feeder/openers were procured, operators were trained to use the new system, and visual aids denoting proper pin #1 orientation were distributed. For the first time, assembly personnel and supervision were made aware of factors such as coplanarity, skew, and stand-off height.

III. LEADFORMING AUTOMATION

Prior to this project, flatpack I.C. leadforming was accomplished using pneumatically operated, hand-fed fixed anvil die sets. Finished stand-off height complied with a company specification that allowed standoff of .002" +/- .005". This condition failed to meet the WS-6536 requirement of .010" minimum after assembly, and prevented a mass reflow soldering operation since leads could be .003" above the board. (Figure 5)

A new lead-to-pad geometry was developed, and finished height was changed to .015" +/- .005". Foot length was changed to .035" nominal, to allow adequate centering and space for heel and toe fillets on a .100" pad length. To aid in toe wetting at the soldering operation, a slight toe-down condition was added to the design. (Figure 6)

Three leadforming technologies were evaluated for the project:

- 1) hand-fed adjustable anvil dies in air presses;
- 2) semi-automated equipment using floating anvil dies and automated carrier handling;
- 3) fully automated equipment capable of removing the I.C. from vendors carriers, forming and trimming the leads, then loading into Westinghouse-style carriers.

Balancing optimum parts handling against cost became a deciding factor. Study indicated that 80% of our parts exceeded coplanarity requirements (2T) as received from the vendor. After leadforming, acceptable coplanarity could be achieved if the input parts exhibited a maximum of 5T. To deal with the wide variety of packaging methods employed during the transition, a flexible, semi-automated trim and form machine was specified as follows:

- Carrier input via stack tube and/or vibratory bowl
- Floating anvil die for acceptable stand-off height

- Continuous and single-cycle modes, for preloaded or hand fed
- Production rate of 5 parts/minute
- Automatic centering and lead skew elimination

Discussions with potential suppliers led to us to the selected source, who provided a unique design, (Figure 7) extra functionality, and a competitive price. The completed machine uses a miniature hydraulic system to control the floating anvil operating rate was as requested, and the entire operation is hands-off if parts are preloaded into carriers. A feeder for incoming parts accommodates most styles of Gibson Egan, Milton Ross, and Barnes carriers in plastic magazines. An area is also provided for incoming parts in the old-style matrix trays. The operator transfers each part into an opened carrier at the front of the machine and presses the start control. A pick + place arm removes the part from the carrier, places it into a centering jaw, retrieves it in the centered position, and places it into the die set. The vacuum tip of the arm remains firmly attached to the part as the form and trim operation occurs, enabling accurate placement of the I.C. back into the carrier. The final two cycles of the machine slide the carrier to the magazine loading station then push the carrier up into the aluminum magazine.

The dies are constructed with separate replaceable clamping, forming, and shearing blades. Shear blades typically last for 15,000 to 20,000 parts before sharpening is required. Since each blade can be flipped to use the opposite shearing side, the maintenance cycle is 30,000 to 40,000 parts, or about once monthly. Since an Omron micro PLC controls the equipment, changes to cycle time and function can be made easily through a programming panel.

The success of this machine led to the purchase of a similar unit, but benchtop mounted, to add increased throughput and response time.

IV. COMPUTERIZED SEQUENCING

Prior to this project, flatpack I.C.'s were sequenced for assembly into waffle trays, one board side to a tray. This was done both robotically and with a hand-operated carousel system. Both of these systems had numerous drawbacks:

- Manual handling of parts on the carousel reduced the required component stand-off height, and failed to provide any parts orientation. A pick and place machine would be unable to acquire and orient parts kitted in this manner.

- The carousel was limited to kitting 20 assemblies of a given number. Frequent kits of 26 boards made for time-consuming set-ups.
- The carousel was only an operator assist, thus leaving the process open to many human error factors, such as wrong or missing parts, incorrect quantities, or heavy-handed handling of fragile leads.
- The robotic kitting cell was limited to handling 50 parts of given part number, and had to move each part input from a storage tray to in-process tray before beginning operation.
- Neither of the systems could be easily converted to handling parts in carriers, so this would become the first automation project to delete the use of a robot.

A machine specification was written to describe a computer-driven sequencer, with features as follow: (Figure 8)

- Parts to be presented to the equipment in carriers, stacked into aluminum magazines (exactly as they come from the leadform station)
- Sequenced parts to be output from the machine in the same format magazines, with multiple sequences per magazine when possible
- A total of 35 input stations for parts, plus one station with green carriers (start-of-sequence indicator), and one station with red carriers (end-of-sequence indicator)
- DOS based controller and file structure for easy off-line sequence creation and editing
- Real time graphics display to indicate all machine functions, sensor states, and operating rate
- Bar code checking of all parts at input stations to verify integrity of operator set-up
- Minimum production speed of 500 parts/hr

When requests for quotations were circulated to prospective vendors, an unusually wide range of designs, prices, and lead times became evident. The lowest bid also came from the same vendor whose engineering approach seemed the soundest, so the order was placed. We arranged to have the sequence-creation software completed and delivered while the sequencer was under construction. By the time the machine was ready for its ATP 12 weeks later, programmed sequences for both sides of all critical assemblies were ready.

During the same time, bar code systems were evaluated in preparation for use of the sequencer's part and tube verification option. The acquisition of menu-driven PC software for bar code label printing, in conjunction with an Inkjet printer, gave us the capability to generate quality labels at low cost. (Figure 9)

Within two days of the sequencer's arrival at our plant, preliminary Manufacturing Control Spec was released and kit sequencing was underway. Hand soldering operators were trained use carrier feeders at their benches.

At this point the first portion of the project (parts handling and prep) was complete.

V. PICK & PLACE

Manual Pick and Place

The decision to employ parts sequencing, rather than multiple random access feeders on a pick and place machine, added a great deal of flexibility to the overall system. Sequenced tubes of parts could be distributed to hand-assembly JIT lines, manual pick and place machines, and an automatic pick and place machine simultaneously. This provided a built-in backup system and flexible surge capacity.

Because of the high cost, customized features, long lead time, and extensive study needed to procure the ideal pick and place machine, it was decided to purchase two manual pick and place machines during the interim. This decision enabled the immediate start-up of mass reflow soldering, process development and inherent labor savings over hand soldering.

A set of evaluation criteria was developed for use in judging competitive manual pick and place equipment, including:

- Type, clarity, and functionality of vision system
- Ease of operation, potential production rates
- Ability to place 50 mil pitch I.C.'s with no pad overlap
- Potential to incorporate carrier feeding mechanisms
- Cost and delivery, with customization required

Although the market offered many so-called manual assist pick and place machines, most at that time were repair stations with little potential to place 50 mil I.C.'s with the required accuracy on a production basis. Microscopes mounted at an angle to a pickup quill created such a parallax error that leads were typically 50% off their pads. Systems that could handle chip components in a commercial environment would not stand up to our application. One machine, designed and built by a local New Hampshire firm, took a novel approach using a prism to see the board land pattern and I.C. leads simultaneously. An evaluation of placement accuracy and ease of operation was conducted using assembly personnel. With a few hours experience, operators became fairly fast and confident at placing I.C.'s onto wet solder-paste.

boards. Typical boards with 65 I.C.'s, which required 5 hours to hand solder, were being assembled in approximately 45 minutes. As the evaluation proved successful, two machines were ordered immediately. A customized version was designed to incorporate carrier feeder, a sequence counter on the front panel, and integrated logic to cycle the functions using a foot pedal. (Figure 10)

Automated Pick and Place

The need to assemble double-sided, mixed technology circuit cards forced some choices regarding pick and place. While the topside process using screenprinting, pick + place, and convection I/R reflow was fairly well defined, soldering I.C.'s to the bottomside after wavesolder was as yet undefined. A great deal of process evaluation time was spent to consider all the possible options. These evaluations are described in the paragraphs later in the paper describing Hot Bar Technology.

As a result of the evaluations conducted, it was decided to pursue a pick & place machine with integral Hot Bar capability. A comprehensive machine specification was developed, to include a WS-6536 and Mil-Std-2000 requirements for soldering, as well as our specific processing needs such as sequenced carrier feeding. Responses to our RFQ fell into three categories: a nearby New Hampshire firm, with a good machine design but little process engineering knowledge; a Canadian firm, with a high-cost product exhibiting excellent engineering but a small installed customer base; two major Pick & Place manufacturers, interested in the concept but lacking any design/product.

The final machine specification and ATP included the following criteria, which we considered critical to our application:

- Ability to feed a sequenced stack of carriers, with the ability to eject the first and last place-holding carriers
- A fiducial correction system capable of adjusting to artwork shifts, without requiring a board redesign to add fiducial marks to all the boards
- A part registration scheme, using second camera vision or nesting, to align parts within a .002" tolerance
- Hot Bar Technology, meeting the WS-6536 spec requirements for resistance-to-ground, voltage across leads, and temperature stability

Nesting vs. Second Camera Alignment

When retrieved from a carrier, part locational tolerance within .002 in the X dimension and .008 in the Y dimension. To place a .017" wide I.C. lead on a .025" wide pad, a tolerance greater than .004 will cause an off-pad placement. To correct this situation at run-time, two systems were evaluated: 1) use an upward-looking camera with vision processor; 2) mechanical nesting.

Vision solution: The type of vision system supplied with the pi + place used a raster scan technique to interpret data seen by the camera. Evaluation of this system with 50 mil pitch I.C.'s led to the following results:

- registration across the leads could be calculated properly, yielding acceptable results in one direction, if the leads exhibited the same visual qualities
- registration in the opposite plane was ineffective, since there was little visual information to compare. With quadpacks, having leads exiting on all four sides, the system performed much better.
- Variations in lead shininess and body centering, as a result of different tinning and forming processes, caused the system to reject a high percentage of parts.

Mechanical Nesting: As a result of the vision evaluation, mechanical nests were suggested by the Pick + Place vendor. The original design used stainless rails to center the part under the "knee" bend, and tapered lead-ins to center across the lead frame width. This centering method performed well only if the knee bends exhibited the same bend radius and spring-back. Parts with only a small change in this dimension (less than .001") would stick in the nest, and the vacuum quill could not pick them up. Lead material, solder coating thickness, and forming die differences had too much control over the nesting performance.

Pneumatic Nesting: The final solution, after many design revisions, was a series of pneumatic nests and individual air flowmeters. (Figure 11) Parts are picked from the feeder (offset by approximately .025"), placed into the nest, driven into an X and Y origin point by air jets, then re-picked by the placement head. This concept can be applied to both quadpacks and flatpacks, since the component body rests on a raised boss, and no force is applied to the leads.

VI. CONVECTION I/R REFLOW, SOLDER PASTE

REFLOW PROCESS EVALUATIONS

Initial evaluations with a two zone vapor-phase reflow machine demonstrated good solder joints. Thermal process analysis indicated a temperature gradient of approximately 50 degrees C/sec during the ramp-up to reflow. This was in excess of the vendor-recommended limit of 2-4 degrees C/sec. (Reference 3) Based on these observations, the decision was made to evaluate Convection I/R reflow equipment in more detail.

Evaluation criteria for convection i/r reflow systems were as follows: (Reference 4)

- temperature difference across the belt with random product loading
- ability to cool one side of a board while reflowing the opposite side
- time to change from one stabilized heat profile to another
- ability to provide a Nitrogen processing environment if desired
- provision for Computer-Integrated-Manufacturing links in the future
- product and process support, knowledge, adaptability, and track record

Performance testing was conducted on two systems we determined to represent the competitive technologies available: 1) panel Convection I/R systems 2) Quartz lamp Convection I/R systems. Techniques recommended by Steve Dow (Reference 5) and Ray Rua (Reference 6) were employed using representative circuit cards, a M.O.L.E. datalogging device, type K thermocouples, and personal computer. After extensive testing at vendors facilities and our own, it was clear that Lamp I/R technology combined with controllable gas flows was the "best fit" for our needs. Temperature uniformity, quick profile changes, and single-sided reflow potential were excellent with the Lamp I/R system. Panel I/R systems exhibited across-the-belt temperature variations of degrees C, profile changing required up to 30 minutes, and one-sided reflow was not possible with our board designs. A machine specification was written, sole sourcing was used based on performance testing, and the equipment was ordered. (Figure 12)

SOLDER PASTE EVALUATION

The initial cost constraints of the project prohibited the ideal process flow for gullwing leads - tinning after leadforming to cover the exposed Kovar lead toes. When I/R reflow failed to achieve complete wetting to the gullwing toes, two process improvements were implemented: 1) leadforming was modified to create a "toe - down" formation, so that the tip of each lead would be buried into the solder joint; 2) solder paste chemistry was explored to achieve improved wetting.

With the cooperation of a solder paste vendor and the vendor's chemist, a series of process evaluations were conducted. To closely replicate the production process, pretinned parts were procured, passed through the leadforming process, then stored on the floor for a time equal to our normal production cycle, about a week. Electrically defective circuit cards were obtained from our board vendor, with the same design, plating and solderability characteristics as the production material. Beginning with a standard "RMA" type solder paste formulation, repetitive reflow processes were conducted, increasing the activity level of the flux with each run. Chloride content and surfactants were added until acceptable wetting to the exposed Kovar toes was achieved. Additional test runs with the final formulation confirmed a reduction in non-wetting from approximately 30% to less than 1%. The total halide content was then calculated by both known chemical composition and chemical analysis. A review of the latest Mil F-14256 total halide limit indicated that the new formulation was just slightly below the maximum limit for an RMA type product. Each vendor we interviewed seemed to have their own definition of what constituted an "RA" level of activation, and most considered "RA" to be anything above their standard paste. Several months were wasted by trying sample pastes from all the well-known suppliers, but the real solution was to empirically derive the proper formulation.

VII. BOTTOMSIDE SOLDER BUMPING, SOLDER MASKING

To automatically solder I.C.'s to the bottom side of circuit cards after wave solder, a method for applying solder to the board had to be found. The following options were evaluated for use with Hot Bar Reflow:

- 1) Applying solder mask over the bottomside land areas, to protect the pads during wave solder. This would be followed by using only the plated solder on the pads and leads for later reflow
- 2) Same as above, but dot dispensing solder paste on the pads before reflow
- 3) Leaving the bottomside pads unmasked, allowing the wavesolder process to deposit solder in the areas to be reflowed
- 4) Stencil printing solder paste onto the board and reflowing it BEFORE all other topside and thru-hole processes; the solder pads would then be masked during wavesolder to maintain consistency.

Experimentation led to these results:

- 1) Solder plated to leads and pads was insufficient to form acceptable heel and toe fillets.
- 2) Unmasked solder pads entering the wavesolder would pick up solder amounts varying from .001" to .010", no consistency could be achieved.
- 3) Dispensed solder paste performed poorly with the Hot Bar Reflow process; inconsistency, solder balling, and solder splatter was prevalent.
- 4) Stencil printing and reflow initially produced excellent results:

In this process, the key to providing consistent solder bumping has not been the solder application, but the consistent solder masking during wavesolder. Experience has shown that chemical changes implemented by the solder mask vendor have contributed significantly to poor solder bump quality after the wave soldering process. Thermode soldering depends heavily on the smooth and accurate condition of solder to the applicable pads. Consistent, machine applied soldermask that does not break down at the wavesolder operation is the most critical factor.

Through experimentation, it was determined that a .008" deposition of solder paste, using a stencil opening identical to the pad geometry, would yield the optimum solder bump after I/R reflow. Various brass stencil thicknesses from .002" to .010" were evaluated, while solder paste formulation was held constant at 88% metal, 900 KCPS viscosity, RMA flux. The optimum amount of solder had to compensate for slight loss due to runoff along connected circuit traces, and still produce a joint mid-way between excess and insufficient conditions.

VIII. WAVE SOLDERING

One key to make the double-sided, mixed technology process possible was "thru-hole wavesoldering without reflowing topside SMT". To gain an in-depth understanding of the process and sufficient process control, a separate study was conducted. While this will be available as a technical paper, the following is a summary of the techniques used.

Approximately 275 test runs over the wave soldering line were conducted, using a M.O.L.E. to record temperatures across the topside of the circuit cards. Eighteen unique boards were included in the evaluation. Data was measured and recorded to include: board mass, component mass, solder pot temperature, # of board layers, conveyor speed, emissivity, preheat temperatures, board size, etc. After all information had been loaded into a data matrix, a personal computer with a statistics

software package was used for analysis. Multiple linear regression was used to determine the significant variables and their coefficients. The result is an equation that determines proper wavesolder settings by inputting only board size, component mass, and board mass.

IX. HOT BAR SOLDERING TECHNOLOGY

INITIAL EVALUATIONS

Several in-depth evaluations were conducted to determine the optimum process for soldering bottom-side I.C.'s on Sanders designs.

A standard inverted SMT process was evaluated, with poor results. Screenprinting to the bottom surface was not possible due to through-hole lead protrusion, and dot dispensing was a process that lacked speed and repeatability. Developing I/R profiles to reflow the bottom (inverted) without losing the through-hole parts proved to be high risk and time consuming. A small change in board thickness could cause a 15 degree delta T causing parts to fall out of the board. Almost every board (approximately 75 unique cards) would need it's own reflow profile.

I.C. attachment using adhesive, followed by wave soldering was a process that initially looked favorable. After considerable evaluation, the following factors made that process less desirable:

- The optimum profile for wave soldering these SMT devices gave poor results on the through-hole leaded solder joints.
- Bridging of the last two I.C. leads that exited the wave could be minimized, but not completely eliminated.
- Board design oriented I.C.'s both parallel and perpendicular to the wave, creating additional defects due to shadowing.
- Adhesive to mount the components was not on the drawings, and program office was unwilling to make a change.

The final process evaluated, Hot Bar Technology, would eliminate the drawbacks of the other processes, but had several areas of challenge.

- Few companies offered pick + place equipment with integrated Hot Bar soldering, and budget constraints eliminated the possibility of two separate machines.
- Previous experience at Sanders had indicated the repeated introduction and deletion of this method, dating back to the early 1970's. Management reluctance was prevalent.

- The solder deposition method would require considerable engineering, as explained in the solder bumping section.

PROCESS DEVELOPMENT

Approximately 75 circuit cards and 1000 I.C.'s were required to develop a knowledge base around the Hot Bar Process. Materials and equipment used were as follows: 8-layer polyimide circuit cards; tinned and preformed I.C.'s from 14 to 24 pin; Unitek reflow soldering controller and transformer, integrated into an EPE 20/20 pick and place machine; type K thermocouples; analog-to-digital conversion board; strain gages and fixturing; personal computer with data collection and analysis software.

Initial process development was conducted using folded-bar thermode technology. To meet the soldering requirements of WS-6536E concerning resistance to ground and current at the contact point, a new technology was developed. The final thermode design employs a straight blade, coated with an insulative adhesive, and covered with a thin titanium "shoe" which is grounded to the machine base. Not only did this modification meet the specification requirements, but the increase in efficiency and mass improves soldering results. Using thermocouples and data logging, we have shown that the delta T from one bar to its mate is within 5 deg. F; from one end to the center of a single bar, delta T is typically within 2 deg. F.

After conducting the evaluations in conjunction with the equipment vendor, the following process and parameters were determined to be optimum:

- pick up required Hot Head Tool from 20/20 toolholder
- pick part from carrier feeder
- place & retrieve part at centering nest
- place part lightly onto solder pads, using "soft touch" (1/2 the normal Z-direction stepper motor speed)
- preheat the thermodes for 430 cycles (about 7 seconds)
- drop down .025" to depress the leads into the molten solder
- heat the joint for 230 cycles (about 4 seconds)
- maintain an average temperature of 340 deg. C
- retract thermodes from leads until bar temperature is 275 deg. C, while continuing to hold part in place
- retract placement head from the part

This sequence requires a total of 30 seconds per part, and produces a defect rate less than 1% if solder bumping and component forming is proper. Parameters for FR-4 boards call for slightly lower temperature and shorter dwell time at liquidus state. A datalog program, running on a personal computer

connected to the Unitek controller, creates a disk file record the minimum, maximum, and average temperature seen at each part reflowed. Data is also recorded to log dwell time and percent current values used for each reflow operation.

COMPATIBLE FLUX EVALUATION

During engineering evaluation runs, a liquid RMA flux was applied to the pads just prior to reflow. If an entire board was fluxed at once, by the time the third solder joint was made, the flux had run off the pad areas.

A separate evaluation was conducted to test the performance of Paste Flux, a product new to the market at that time. Samples were requested from three vendors, after we explained our processing parameters to their product engineers. One test, using thermocouples embedded under solder pads, proved that the flux paste was responsible for forming a heat bridge. A delta T of 25 degrees C was typical between boards with and without Paste Flux. Soldering characteristics found between different Paste Flux formulations were:

- Solder peaks formed on the top of the I.C. "foot" as the hot bars retracted from the joint
- Burnt flux entrapment in the surface of the solder joints
- Low melting temperature, allowing all the flux to liquify when a nearby part was soldered
- Crystallization of the flux in the syringe, causing lumpiness of the product; this led to poor parts placement as the lumps acted like "ball bearings" when the parts approached the solder pads.

As a result of the evaluation, one product was selected as the closest fit to our process needs. This product's specifications are as follows:

Formula	Flux	Flash	Solids	Tack	Viscosity	Max.
Designator	Type	Point	Content	Strength @ 25 deg.C	@ 25 deg.C	Temp.
Tacflux 005	RMA	66 C	69%	10 psi	324,000 CPS	340 C

X. WORKCELL INTEGRATION

While the completion of the project yielded a NET LABOR REDUCTION OF 87%, the final stage, computer integration, will achieve the required flexibility and responsiveness. The workcell integration will take advantage of the barcode labeling of parts and sequences accomplished in the first phase of the project, and

control the processes with the help of a "where-used" part database. (Figure 13)

Physical layout of the workcell and related equipment is shown on Figure 14.

REFERENCES

1. Charles J. Meyer, "Westinghouse Carrier Program 16 lead, 1/4 wide Carrier Testing", Westinghouse Material Acquisition Center Glen Burnie, Md.
2. Universal Alloy Inc, 281 La Mesa Ave., Anaheim, CA.
3. Raymond W. Rua, "Surface Mounting Technology", Ray Rua Associates, Inc. Big Rapids, Michigan
4. Harlan Leonard and Dick Bolin, "SMT Component Stress During Board Processing", Bourns, Inc. Riverside, California, ISHM '87 Proceedings
5. Steve Dow, "Reflow Soldering Equipment Specification, Acceptance, and Process Qualification", Colorado Surface Mount Technology, Colorado Springs, Co.
6. Raymond W. Rua, "Surface Mounting Technology"

Technology Needs

Phase I	Phase II	Phase III
0 - 1-1/2 YR	1-1/2 - 3 YR	3 - 5 YR
F/P Handling	DIP Insertion	Programming Cente
F/P Leadforming	Axial VCD	Central Controller
F/P Sequencing	Radial Insertion	Oddball Inserter
Pick + Place	Rework Stations	Robotic Staking
Mass Reflow	Communications:	SMT Pick/Place
Automatic Tinning	CAE/CAD to Pick+Place	
	Test to Rework	

FIGURE 1. Chart of SECAS Technology Needs

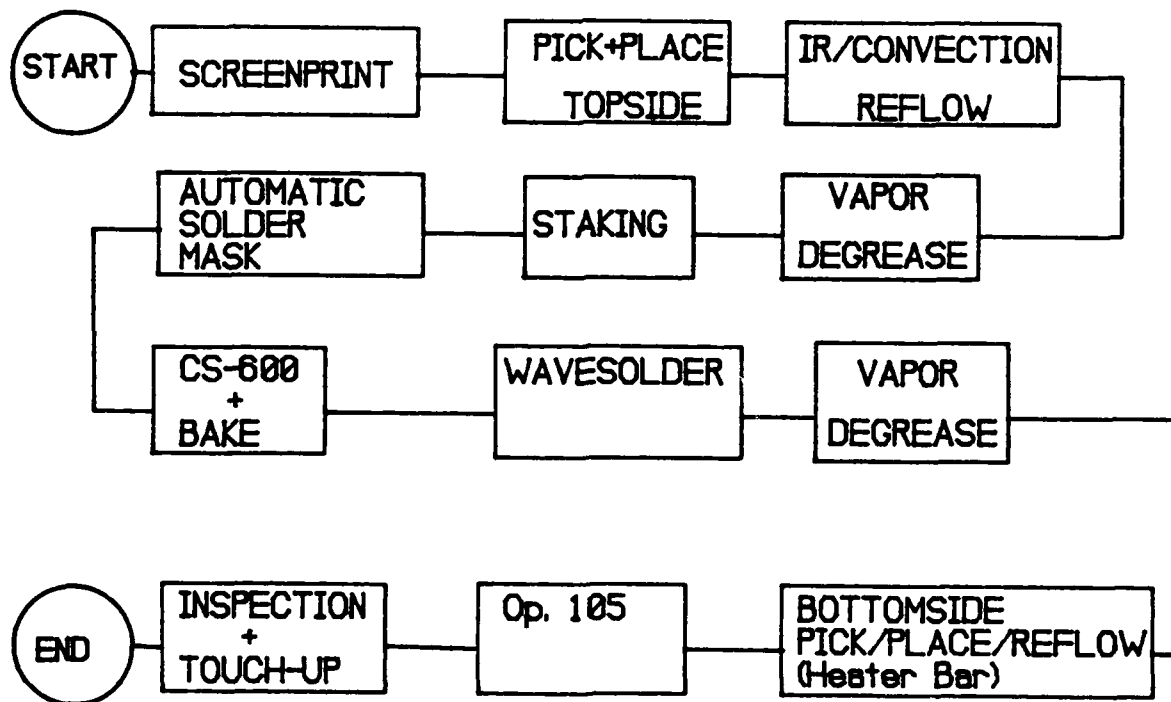


FIGURE 2. New Process Flow Chart

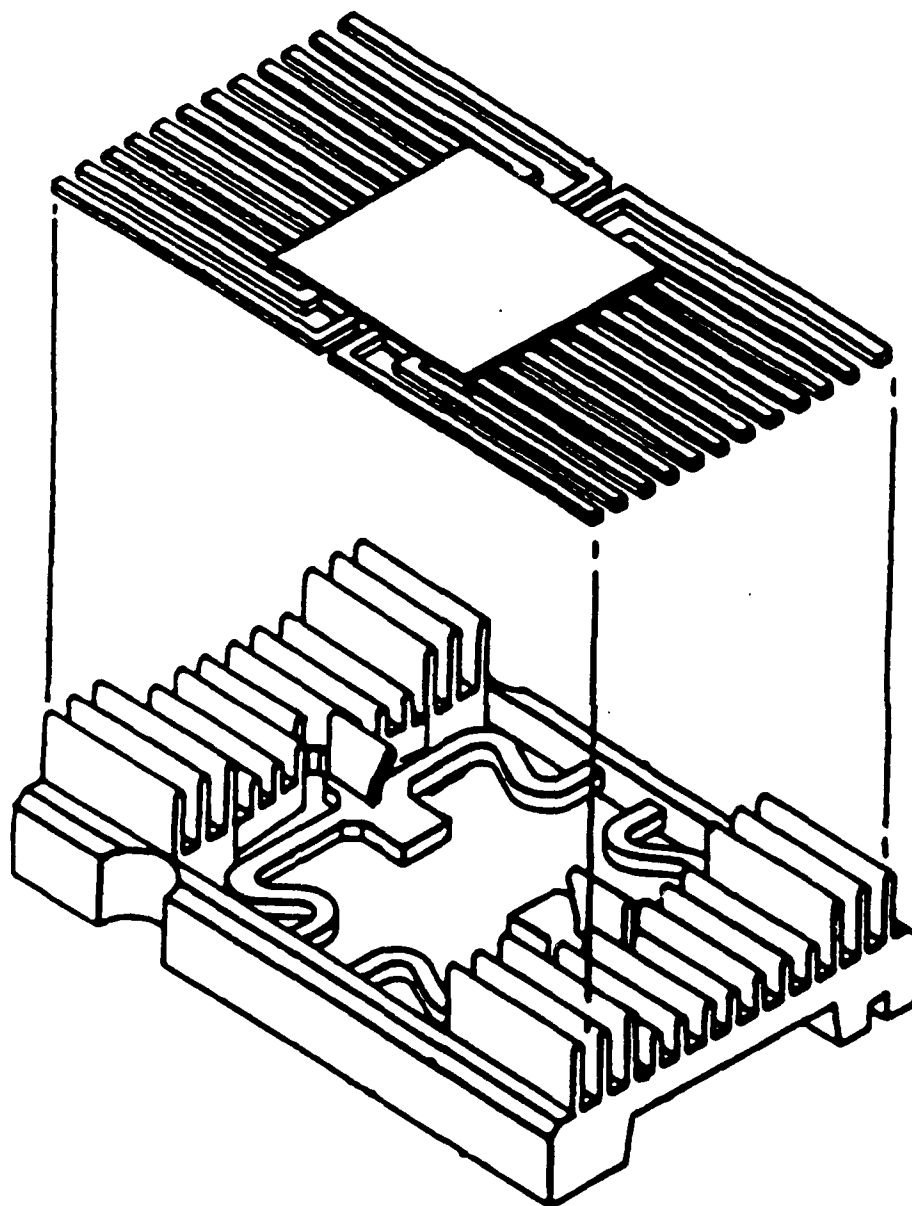


FIGURE 3. Westinghouse-Style Flatpack Carrier

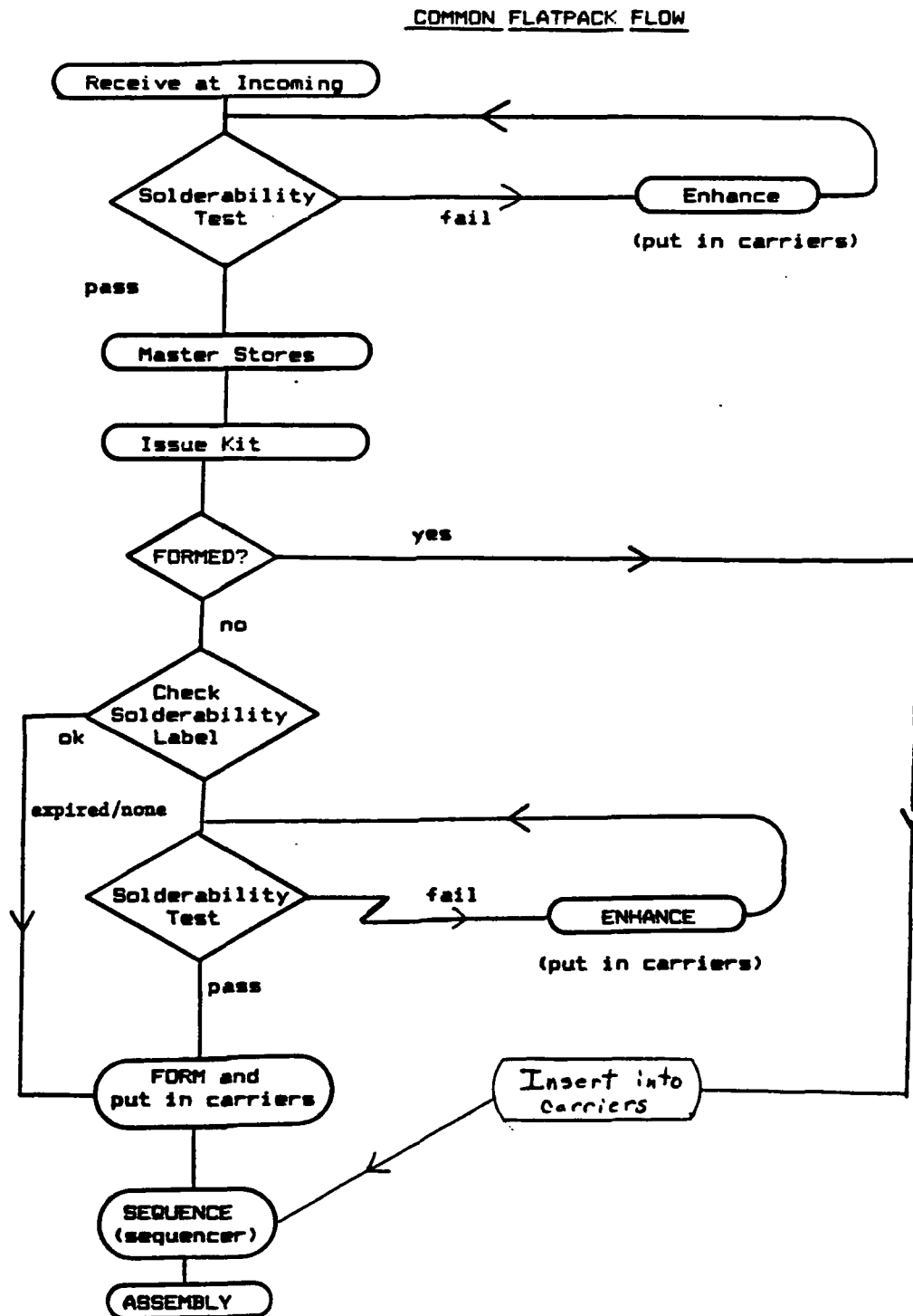


FIGURE 4. Common Flatpack Process Flow Chart

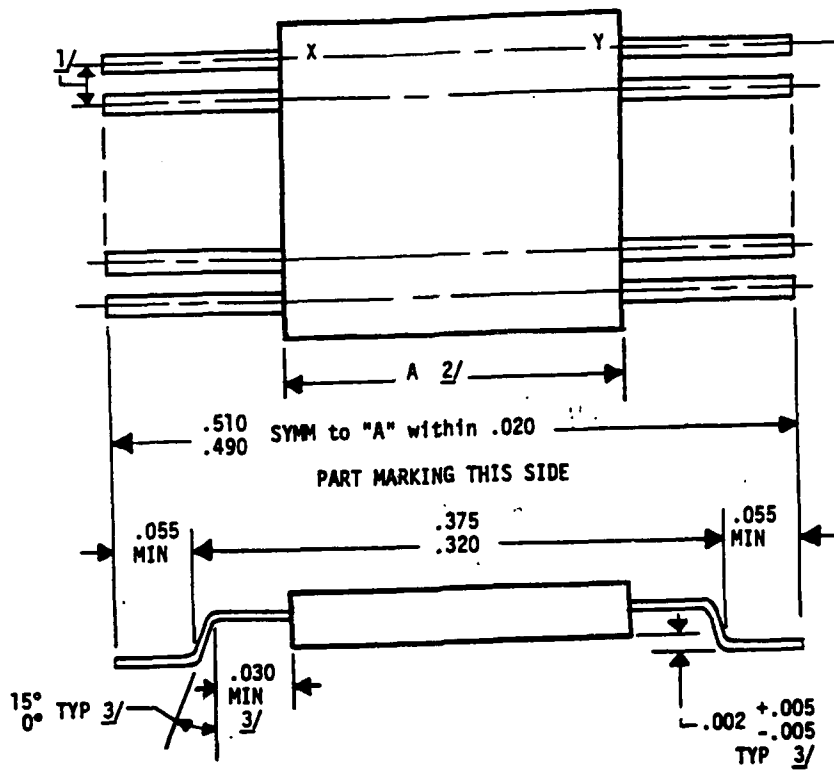


FIGURE 5. Old Leadform Dimensions

Flatpack Form and Mount Dimensions

small footprint for .250" case, 14,16,20 lead

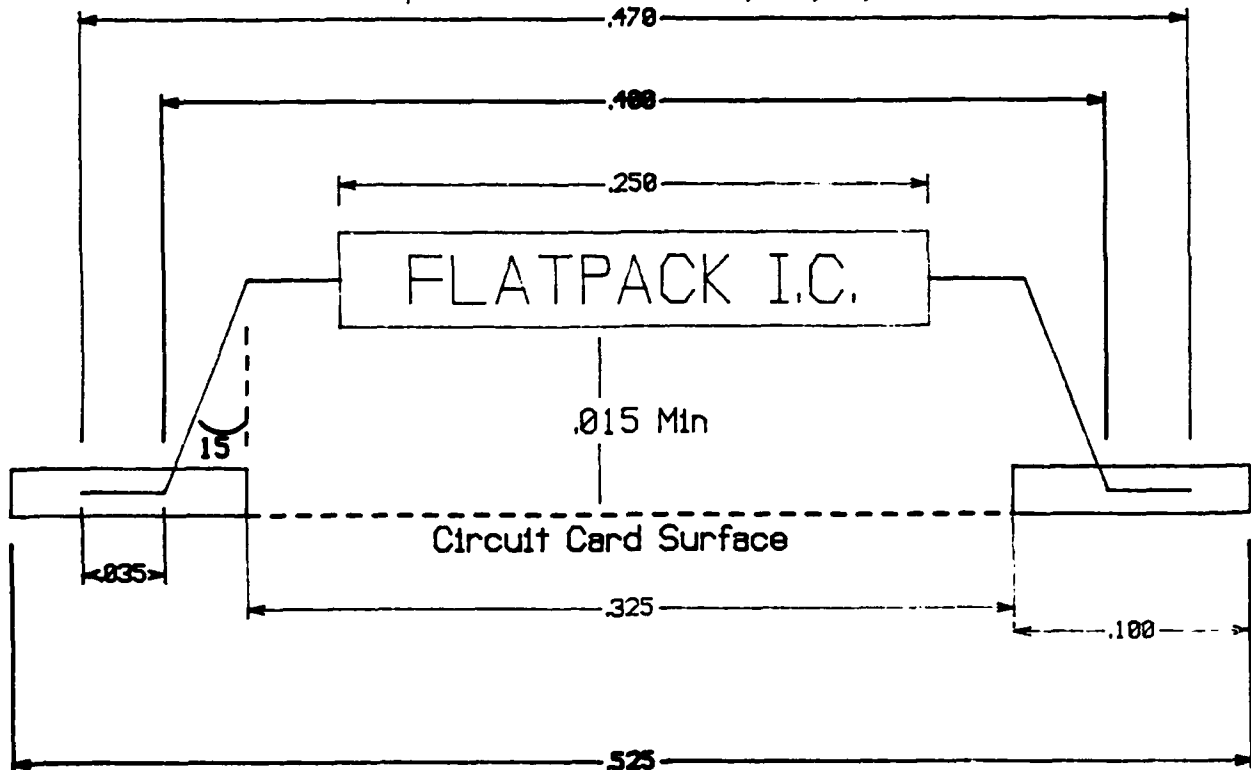


FIGURE 6. New Leadforming Dimensions

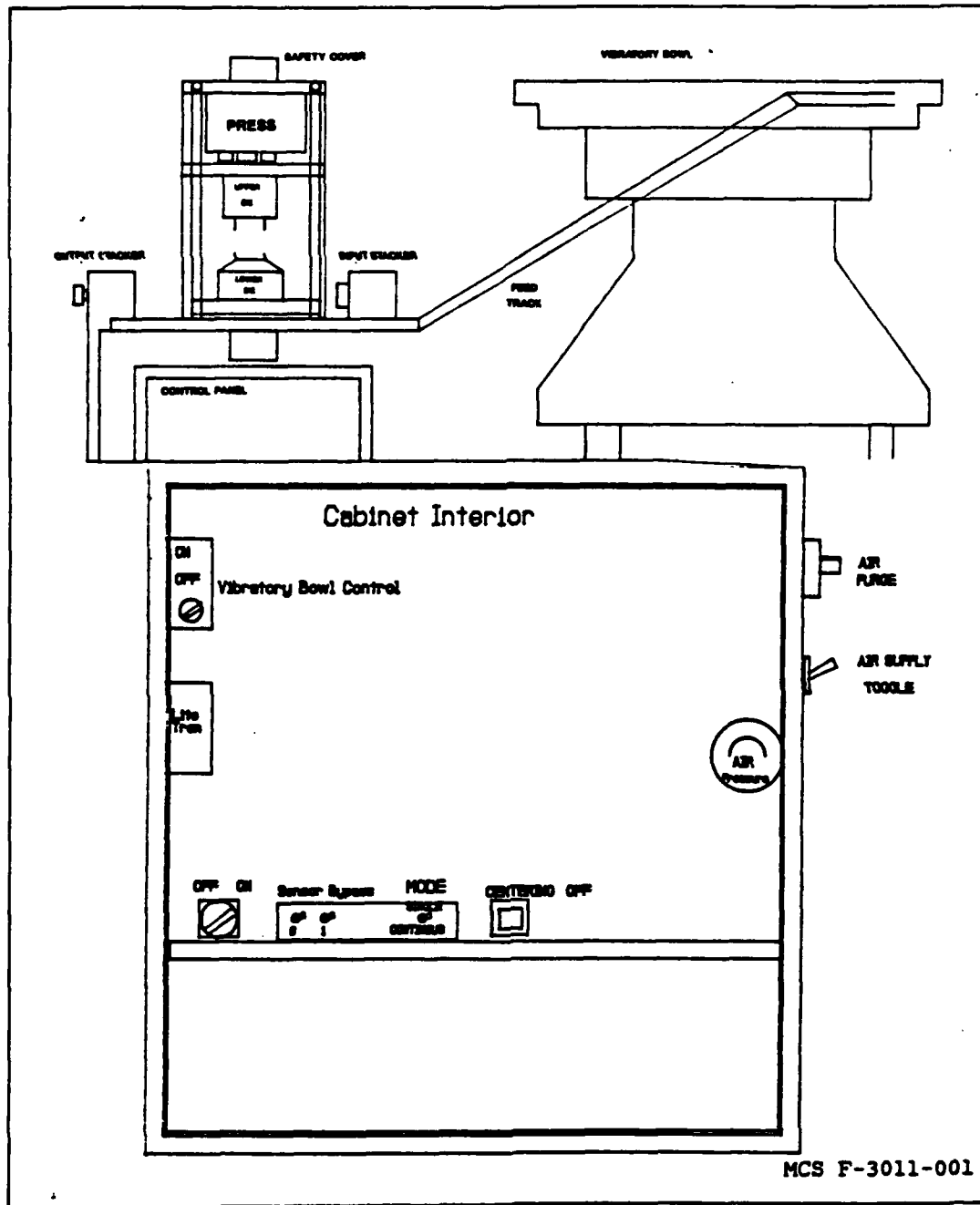


FIGURE 7. Leadformer Block Diagram

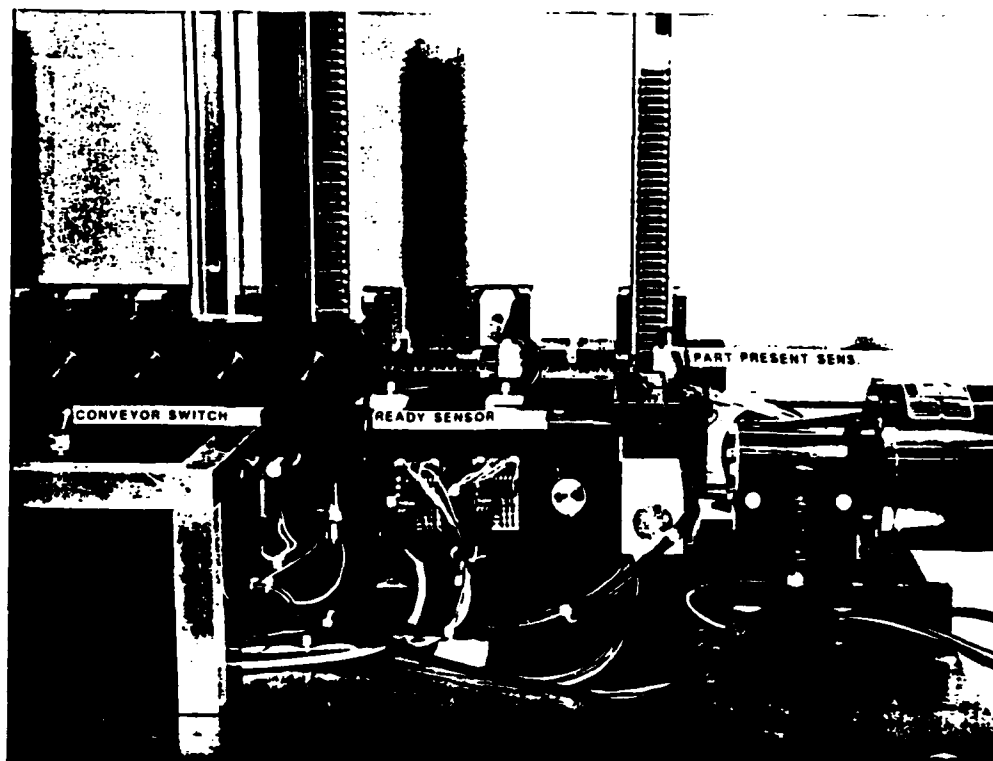
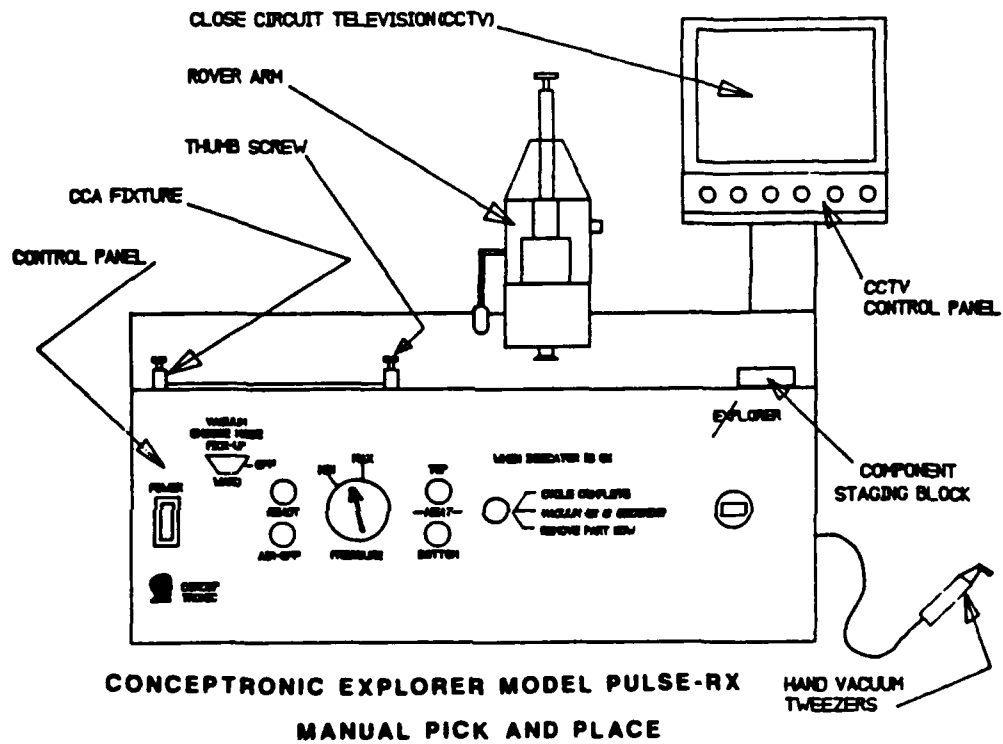


FIGURE 8. Flatpack Sequencer



FIGURE 9. Sample Bar Code Label For Flatpack Magazines



CONCEPTRONIC EXPLORER MODEL PULSE-RX
MANUAL PICK AND PLACE

FIGURE 10. Manual Pick & Place Machine

- 14, 16, 20 PIN F/P NEST
- DIMENSIONS IN PARENTHESES APPLY TO 24-PIN F/P NEST
- DRILL 2 PLCS. FOR P.F. $\frac{1}{16}$ DOWEL PINS

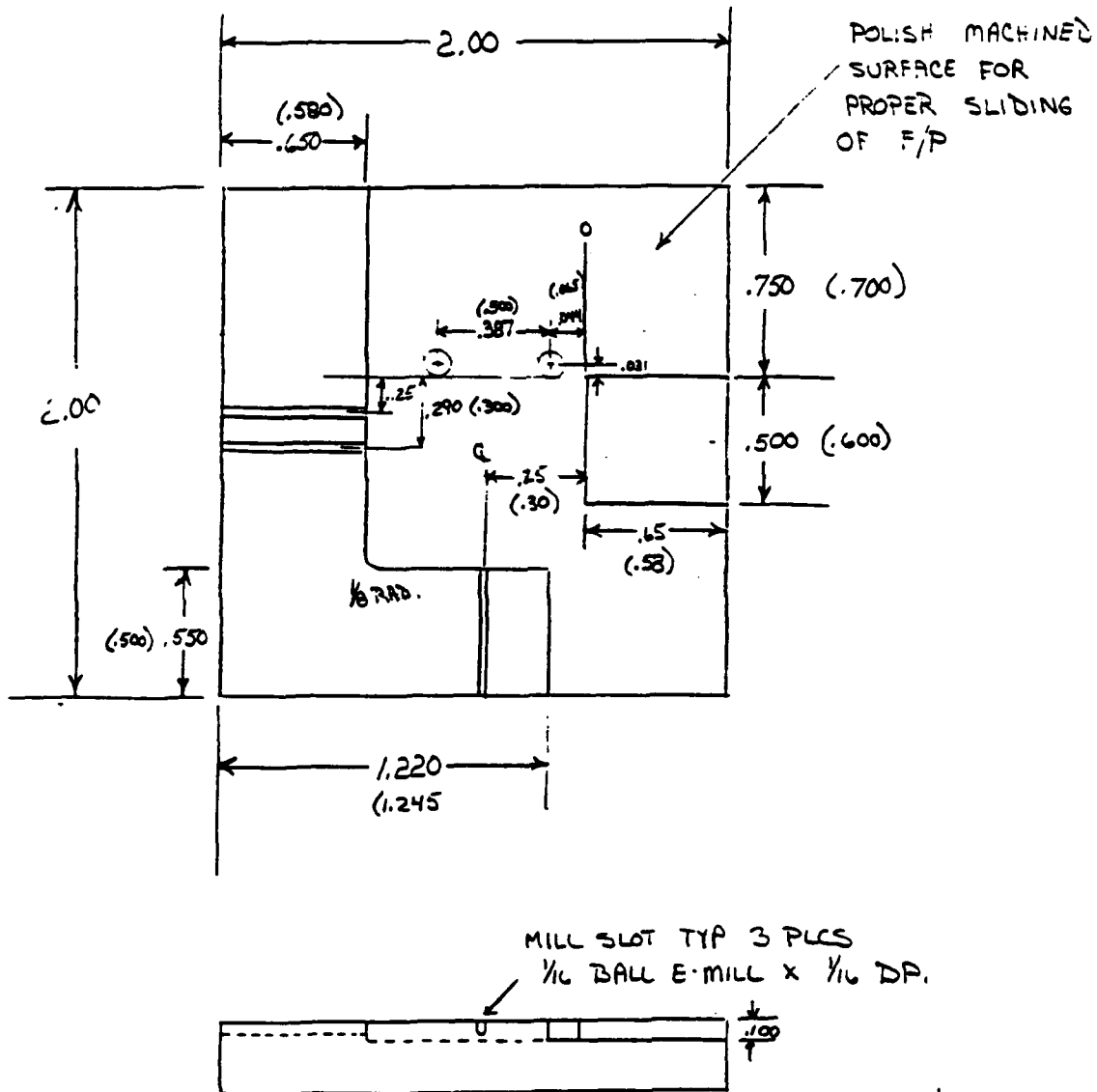


Figure 11. Pneumatic Flatpack Centering Nest

MAT L
303 SS

Infrared Solder Reflow Systems for the Attachment of Surface Mounted Devices

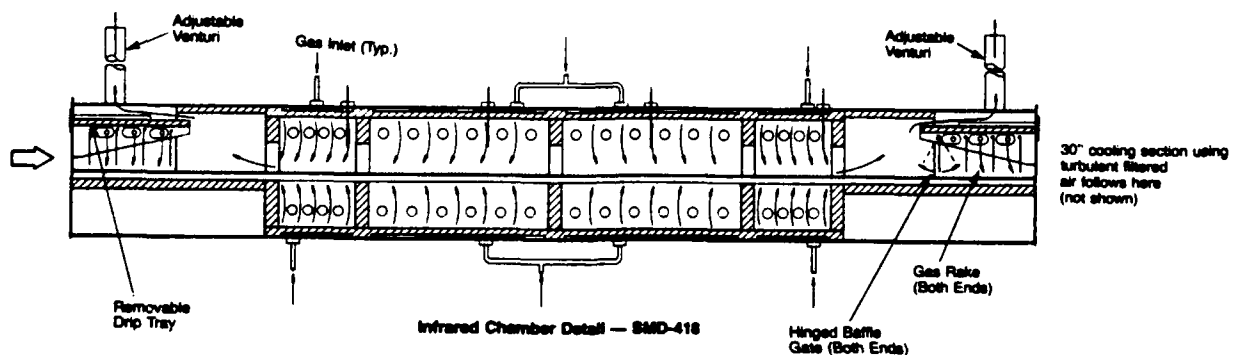
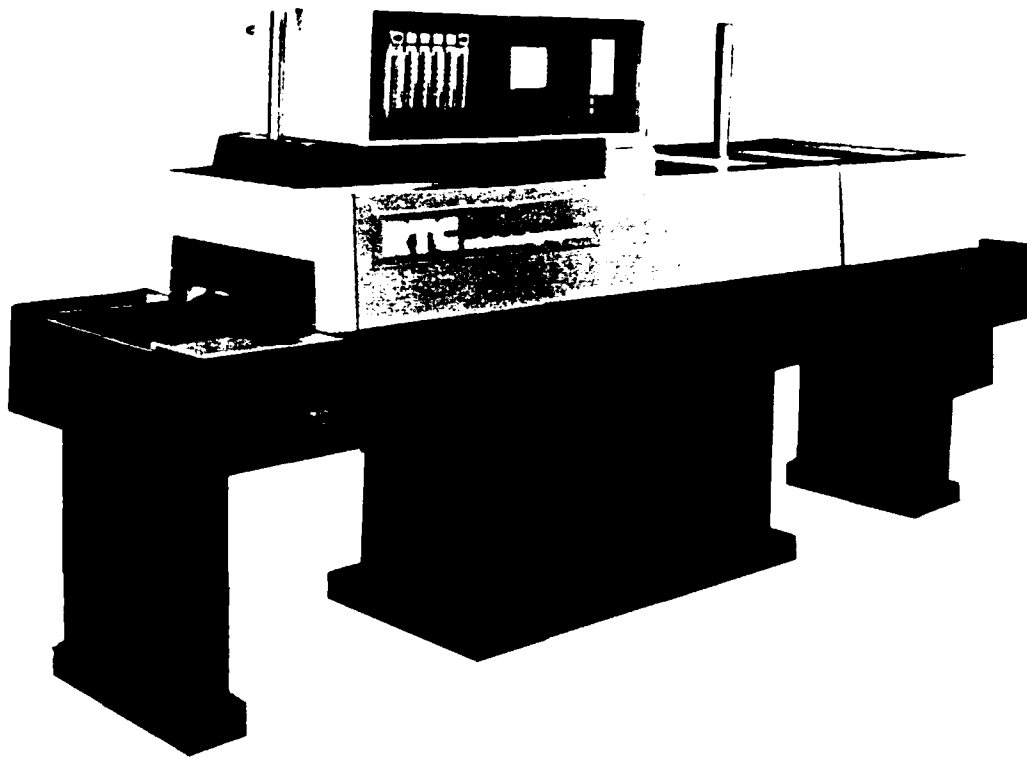


Figure 12. RTC Quartz Lamp I/R Tunnel Oven

WORKCELL CONTROL

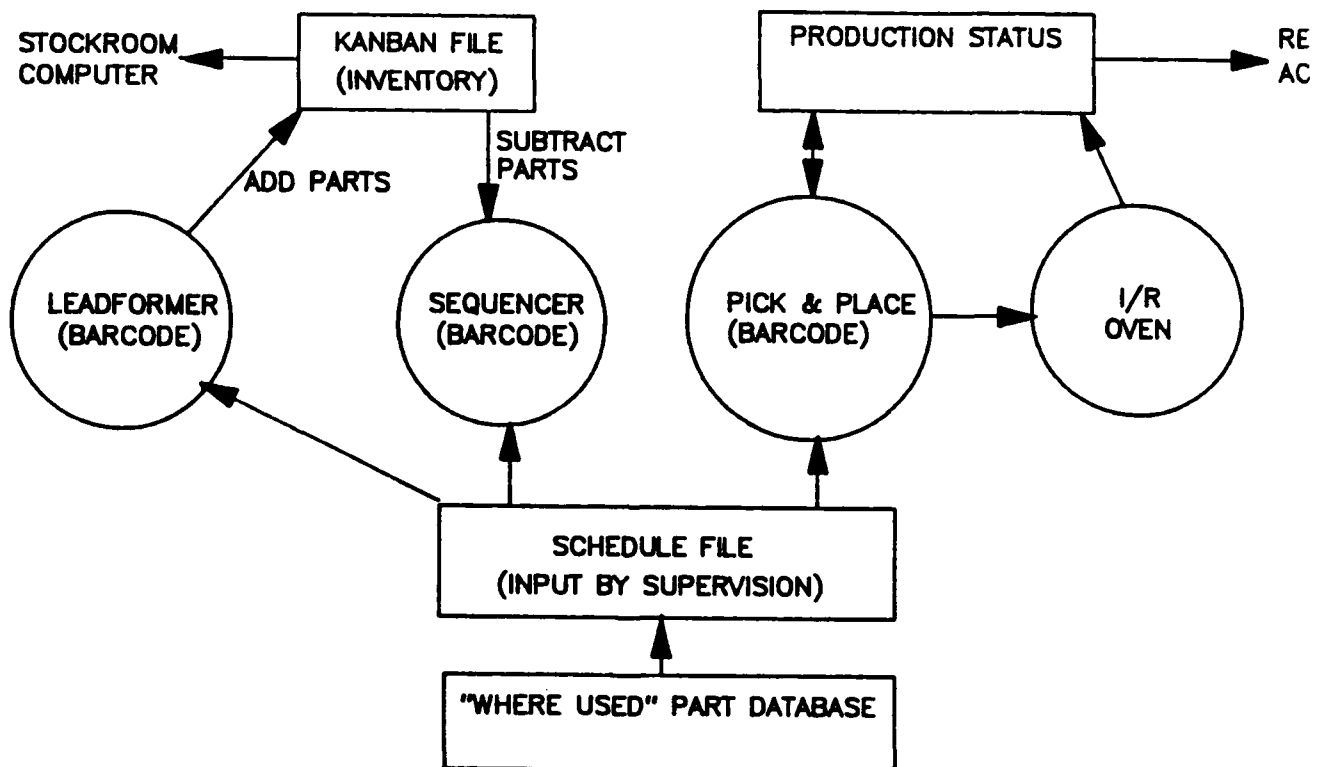


Figure 13. Workcell Integration Chart

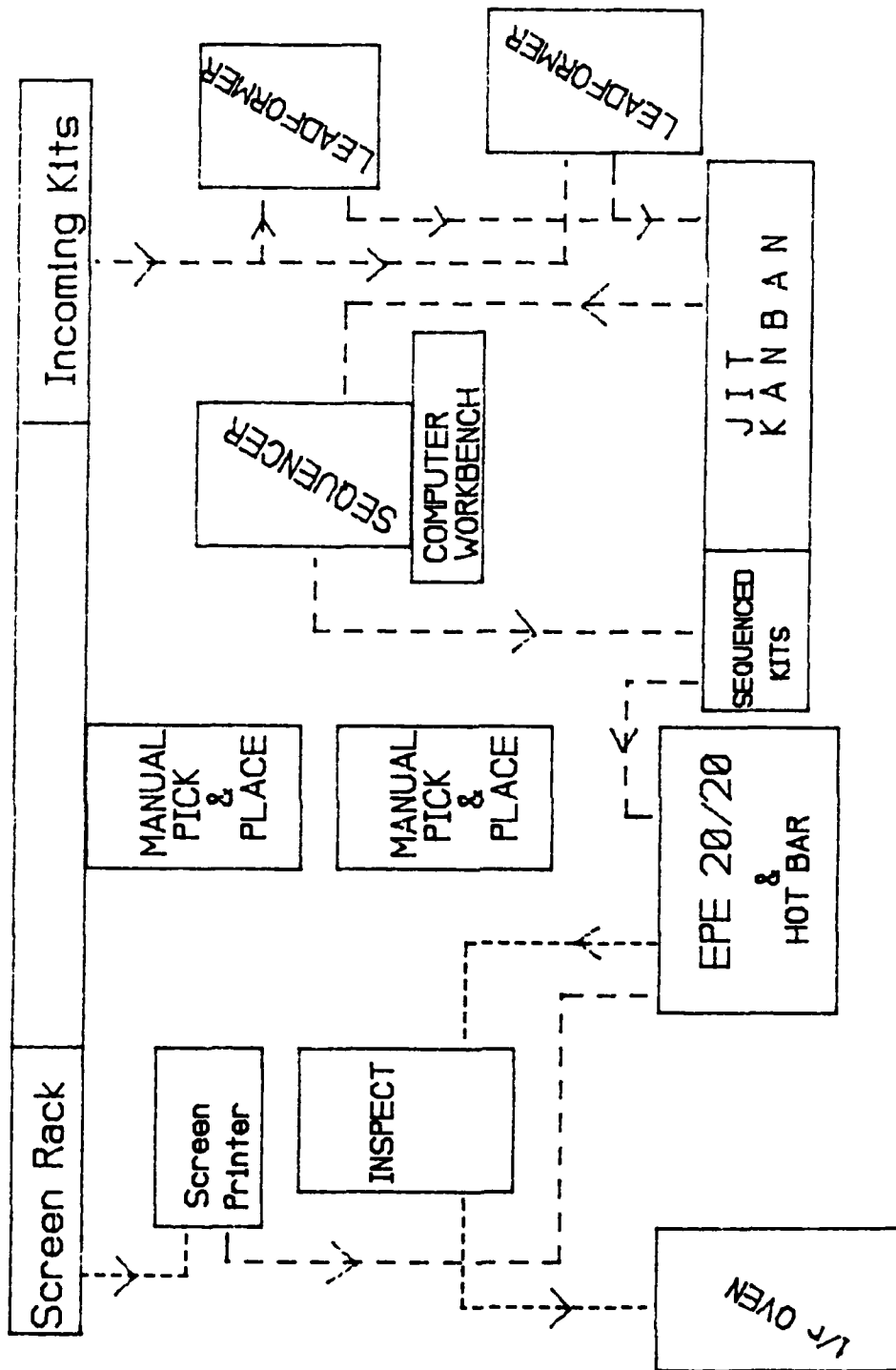


Figure 14. Secas Equipment Layout

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Doug received a BS degree in Physics from the University of Massachusetts and is a Computer Science major at the Worcester Polytechnic Institute. He is a senior member of SME and a member of the staff of the W. Edwards Deming Institute of Manufacturing Productivity and Quality at M.I.T.

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CONFORMAL COATING SPC
A CASE STUDY

by
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ABSTRACT

The conformal coating process of printed wiring boards in a mil-spec environment is a standard practice. Being able to accurately and precisely apply the coating to a large number of different pwb's is sometimes not that standard.

In this case study there are six major steps taken to bring this process under statistical control using an X-bar and R chart. Some were planned and some were a result of assignable causes. The process is still being improved, but the benefits after eight months are impressive.

This study was performed from January 1989 to August 1989 in the Cedar Rapids facility which manufactures HF and UHF Communications Equipment for the Military.

INTRODUCTION

In December of 1988 a group of five people were tasked with improving the conformal coating process with the use of statistical methods. Statistical Process Control (SPC) had been used to study the defects from this process for about a year. Measurements of conformal coating thickness have been taken by inspection for many years as another form of process control. The major emphasis of this paper is to focus on the use of statistical methods to bring about continuous improvement.

The initial question to the group was, where in the process was the area that created, or had the propensity to create, the most problem. The initial answer was that there were no problems. A process flow chart was made to identify all the major steps of the process. During this exercise the question was asked again (where is the greatest potential for problems?), this time the pwb board thickness was identified.

BACKGROUND

This conformal coating process is a machine process which passes the pwb's on a paper conveyor belt underneath six spray heads (figure 7). Prior to using SPC an inspector measured one 1 inch by 3 inch aluminum coupon once a day. The inspector measured whether or not the thickness was in specification. The measurement was recorded, but feedback was rarely given to the operator (since the inspector made the check) and people felt the measurements had too much variation to be totally reliable.

Upon implementing SPC the same micrometer was used and the data was kept manually on a control chart. The number of coupons taken per production run was changed to take advantage of the central limit theorem and increase the confidence in estimating the average of the data. The sampling procedure was changed to the following:

- 1) The operator takes three samples every production run one at the beginning, one in the middle and one at the end.
- 2) These three samples are averaged and plotted on the average chart and the range between the parts are plotted on the range chart.
- 3) The charts are continually monitored by the operator and the support people review them bi-weekly unless the operator asks the support people for help.

The sample/subgroup size of three was chosen since it is the most economical subgroup size. It was hoped that this would give a good representation of the process and it was known that it would increase the accuracy of the average thickness by reducing the variation of the readings.

IMPLEMENTATION

The initial chart went on the factory floor in January of 1988. The first major discovery was that as the paper take up reel accumulated more and more paper the conveyor speed increased which caused the conformal coating thickness to get thinner and thinner (figure 1). Theoretically the take up reel should never change speed, but actually it did and trying to adjust the clutch on the take up reel to work properly has never worked since loosening the clutch causes it to slip and tightening it causes it to stick. Therefore emptying the paper roller after every run is a very important aspect of this process. It is one that has been adhered to faithfully since this discovery was made in the first week of using the chart. Until this time no one really knew whether or not the take up reel made any difference, and some people believed that the clutch kept the speed constant. One of the main goals of the SPC team was to increase the average to 2.5 thousandths of an inch from previously running at 2.2 thousandths of an inch. This

was accomplished very quickly after the take up reel discovery.

The second discovery was the slipping of the take up reel (figure 2 and 3) as stated above. Some washers were replaced and the reel was repaired, but still there remained a fine line between adjusting too loose or too tight. In order to prevent the slippage tightening very tight was chosen. The effects of the clutch being too tight was an increase in the conveyor speed due to the paper accumulating on the take up reel which is controlled by emptying the reel after every run.

The third discovery was that the conveyor speed setting would drift (figure 2) over time. It was therefore necessary to check it when the chart exhibited an out of control condition and correct it if necessary.

The fourth discovery was one that we did not find intentionally. Off and on throughout the years the different operators on the conformal coating machine have mixed the coating material at different times. Prior to March the operators were mixing the material for the next shift. Which means a 12 to 6 hour idle time when the solids can settle. On March 23rd the decision was made to mix the material just prior to running (figure 3). The range chart on (page 8) indicates a large decrease in the variation between coupons. It was then understood that mixing the material just prior to the run would decrease the thickness variation by 50%, because the solids would not have a chance to settle to the bottom of the storage tank.

By April the engineers felt comfortable that they could control the process instead of the process controlling them. The next step was to learn how much pump pressure would affect thickness. The pump pressure was increased (figure 4) and the thickness increased to 2.7 thousandths of an inch of an inch from 2.5 thousandths of an inch. This allowed the engineers to increase the conveyor speed to bring the average down to the desired 2.5 thousandths of an inch, which increased capacity. The advantage of averaging three coupon was really evident here. It was very easy to see a small shift in the average from 2.5 thousandths of an inch to 2.7 thousandths of an inch, because of averaging the three coupons. This would have been very difficult with individual values under the present measurement methods.

In May a study started on the effect of viscosity, humidity, and temperature on the thickness (figure 5). Multiple regression analysis was used to analyze the data and viscosity was found to be most important factor to control. Temperature and humidity had very little effect on the thickness within the range that it changes in the Cedar Rapids facility.

RESULTS

The following summarizes the improvement since SPC was implemented on

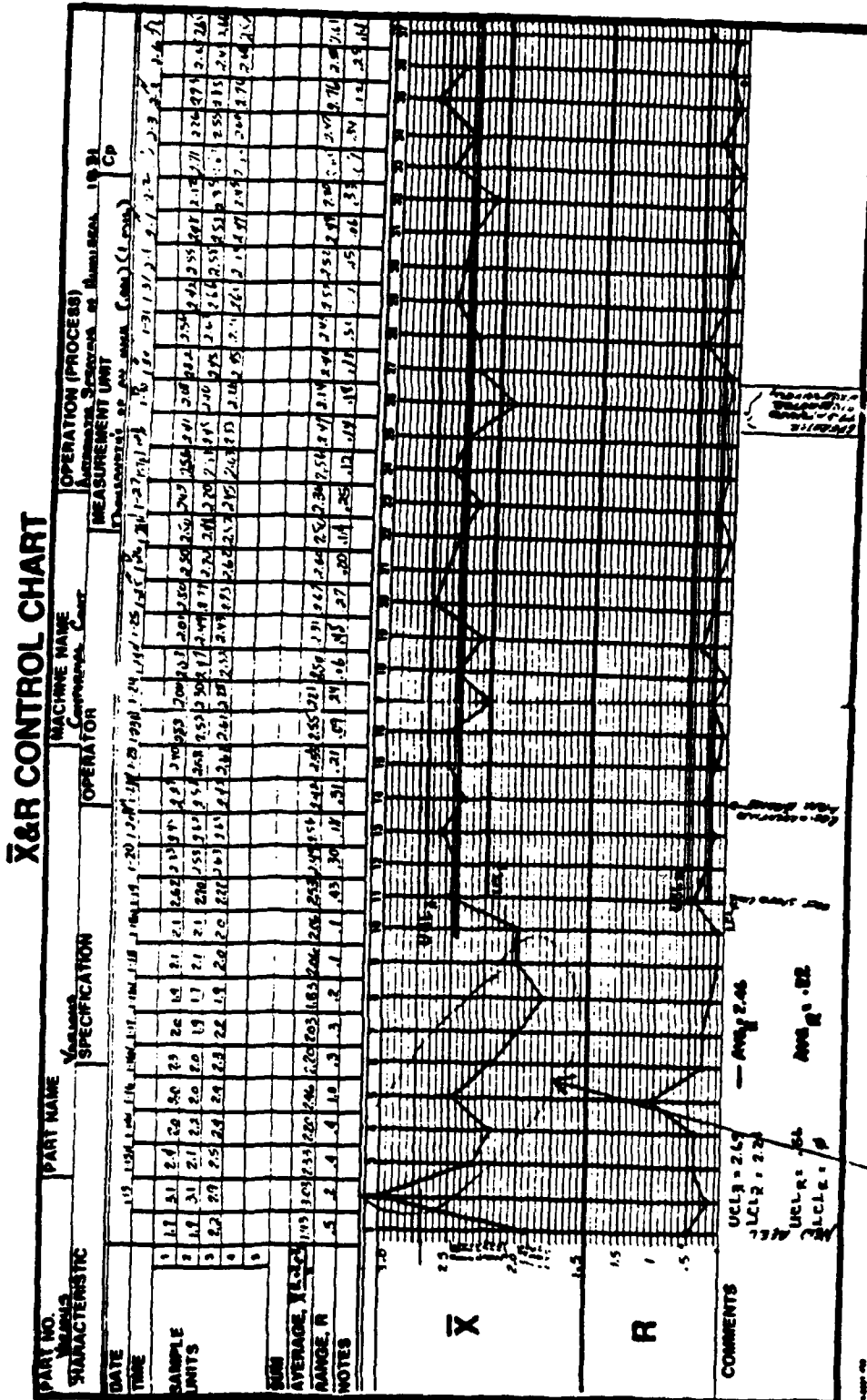
this process. The mean was successfully targeted at 2.5 thousandths of an inch. This reduced the variation by 50%, provided new knowledge of what causes problems in conformal coating thickness and knowledge of how different factors effect the thickness as the increase or decrease. Throughput time was improved, one specific equipment that has a lower specification of 2.0 thousandths of an inch now is running at .038% out of specification from 16.5% out of specification prior to using SPC. Operators get feedback to see shifts, trends, and significant changes in the mean and range. Industrial engineering has improved diagnostics and control of the process. The number of conformal coat rework operators was reduced from three to one. The number of defects per thousand possible has decreased from 8 per thousand to 3 per thousand (figure 6).

CONCLUSION

SPC can be a very powerful tool to improve Quality and Productivity with very little or no capital expense. It was used in this case study as a tool to promote control and continuous improvement.

ACKNOWLEDGEMENTS

The author is grateful to Harley White, Jim Lorenz, Mike Sebeny, Bob Lewis, June Detwiler, Eva Kriegermeier and Kay Sloan for their support in making the changes needed to implement SPC on this process.



② TAKE-UP REEL SLIPPING

(3) CONVEYOR
RETIMED

Figure 2

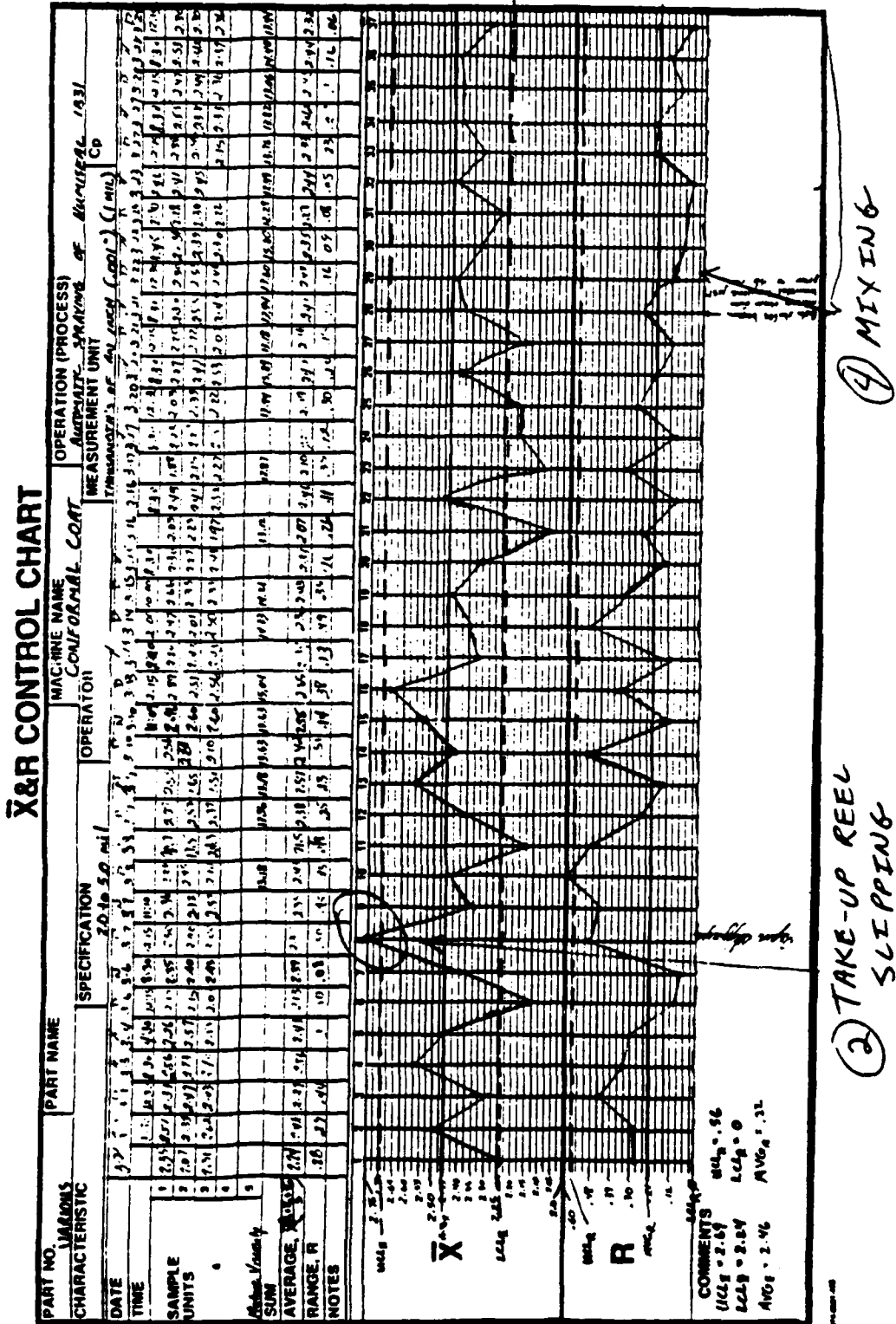


Figure 3

$\bar{X}$ & R CONTROL CHART

[illegible]

5

PUMP PRESSURE	CONVEYOR SPEED
INCREASED	INCREASED

Figure 4

$\bar{X}$ & R CONTROL CHART

[illegible]

⑥ TEMPERATURE HUMIDITY + VISCOSITY

Figure 5

TOTAL WORKMANSHIP DEFECTS

SECTION 537 (CONFORMAL COAT) DETWILER

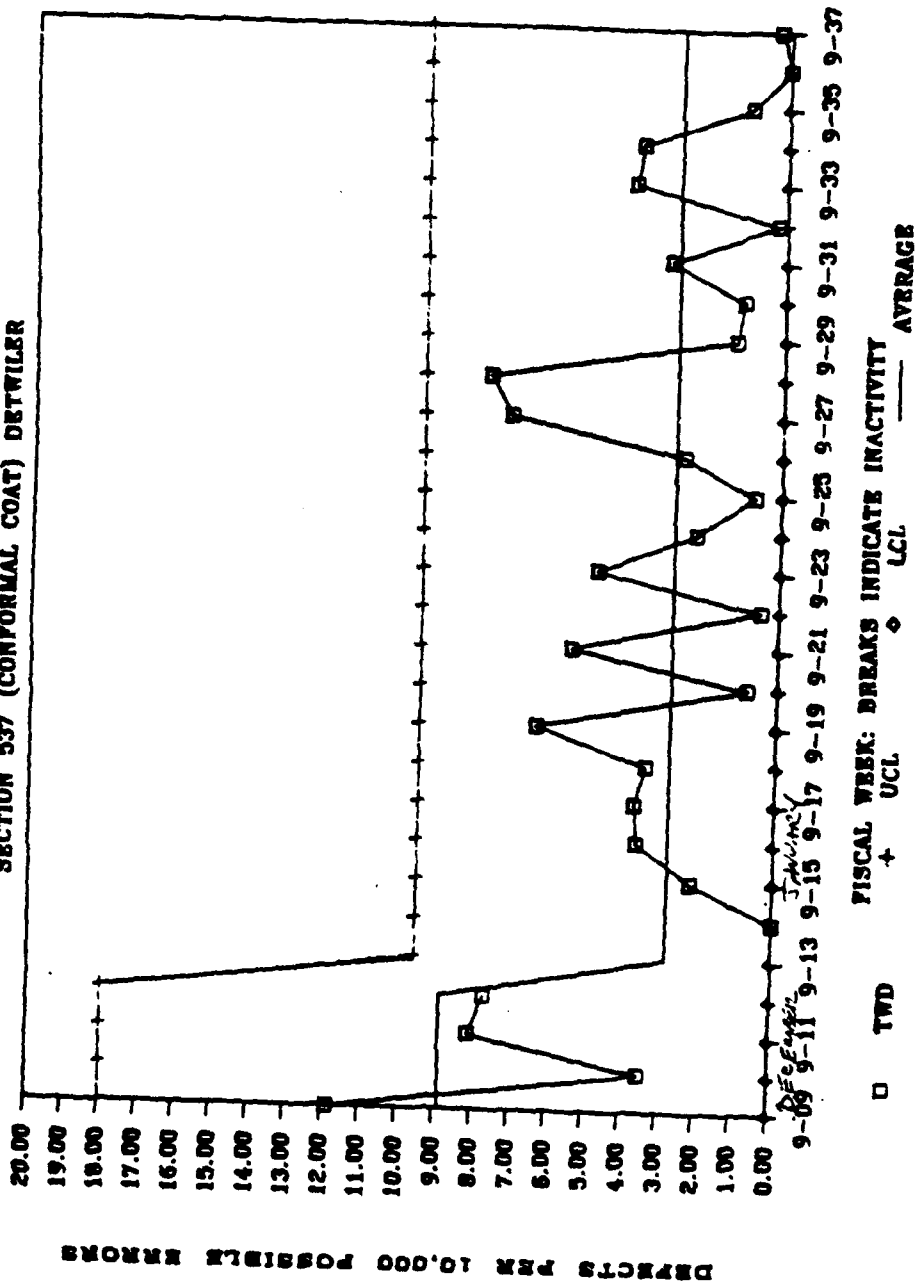


Figure 6



Figure 7

CONFORMAL COATING MACHINE

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**A PATH TOWARDS PROCESS CONTROL
IN THE GOVERNMENT ELECTRONICS
MANUFACTURING ENVIRONMENT**

by

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ABSTRACT

Establishing process control on electronics manufacturing lines is not an easy task. First, management must fully support a process control mission statement and the resulting process control plan. Then, the entire manufacturing process has to be characterized, inputs and outputs listed, attributes highlighted, process variables identified and typed, and controlled experiments conducted.

The results of the controlled experiments establish the target variable values and the allowed variation around the target values. Action plans are then developed for the excursions of the process from control. This information is then used as a basis for a complete process control implementation.

When the line is a typical Government electronics manufacturer, the task becomes even more complicated, due to the high product mix and the low volume of these manufacturers.

This paper discusses the path towards process control and suggests ways of achieving process control even in a Government electronics manufacturing environment. Process variable data and defect data from several Government and commercial electronics manufacturing lines will be presented and discussed.

INTRODUCTION

With declining budgets for Defense Electronics, with the increasing possibility that consumer electronics manufacturers in the far east will begin military electronics manufacturing, with cost and efficiency becoming paramount in world electronics manufacturing, it has become necessary for the Defense Electronics Industry to re-evaluate their classical methods of Design and Production. The key to achieving higher quality, at lower production costs, in the consumer electronics industry, was continual process improvement through the use of Statistical Process Control (SPC). This same methodology can work in Defense Electronics.

Establishing process control on electronics manufacturing lines is not an easy task. First, management must fully support a process control mission statement and the resulting process control plan. Everyone in the organization needs to be involved. The entire manufacturing process has to be characterized, inputs and outputs listed, attributes highlighted, process variables identified and typed, and controlled experiments conducted.

The results of the controlled experiments establish the target variable values and the allowed variation around the target values. Action plans are then developed for the excursions of the process from control. This information is then used as a basis for a complete process control implementation.

When the line is a typical Government electronics manufacturer, the task becomes even more complicated, due to the high product mix and the low volume of these manufacturers.

This paper discusses the path towards process control and suggests ways of achieving process control even in a Government electronics manufacturing environment. In particular, the use of an automated Scanned-Beam X-Ray Laminography system for obtaining process variable measurement data in both the design experimentation stage and the normal production runs is discussed. Process variable data and defect data from several Government and commercial electronics manufacturing lines will be presented and discussed.

It is not the purpose of this paper to discuss Dr. Deming's quality concepts, nor to criticize our neighbors on the Pacific rim for adopting an efficient way to manufacture quality electronics. This paper hopes to illustrate the use, application, and value of a precision measurement instrument in a total SPC program for Defense electronic manufacturers.

PROCESS CONTROL VS PART CONTROL

Defense Electronics Manufacturer "A" (Reference 1) has been manufacturing electronic printed wiring circuit boards since their invention, and before that, wire and post construction. Manufacturer "A" considers itself to be "world class" in Defense Electronics.

This manufacturer has several major contracts and a number of smaller ones. He has the typical high-mix and low-volume manufacturing requirements, producing boards to the Weapons Spec and Mil-Std. He has various waivers on some of the contracts. Every board seems to be different—in design, in technology, in production methods, and in accept/reject criteria. To get the boards out the back door is a major accomplishment.

This manufacturer has for years practiced "PART CONTROL" in his manufacturing process. Part Control consists of having "Accept-Reject" limits for every part in the process, and then selecting the part to use in manufacturing from a large "stockpile" of parts. Parts that are unable to be re-worked are scrapped, and those that can be are re-worked so that they fall within the "acceptable" limits.

In this world of part control, the "INSPECTOR" becomes god-like. He controls the entire future of the company, based upon his pronouncements. Entire sections of the manufacturing floor space are devoted to Inspection and Re-Work (euphemistically called "touch-up"). A large number of parts and assemblies are scrapped. Product is tied up in this "Inspect-Test-and-Repair" Cycle for an unpredictable amount of time. (The author likes to refer to this cycle as the "Inspect-Test-and-Destroy" Cycle.)

Manufacturer "A" will be hopelessly lost and left behind unless drastic actions are taken to break this vicious cycle. His only hope is to convert to total quality management through continual process improvement and control.

Manufacturer "B" has fully embraced "PROCESS CONTROL." This manufacturer knows that quality is the responsibility of management. Management is actively involved and committed to Overall Quality System and understands that quality is designed and achieved by controlling and reducing variability in the process. Everyone in the organization is trained in the quality plan and has a role to play in continuous process improvement. Customer satisfaction has become the key objective. Statistical Evaluation of the process with designed experimentation provides tools to achieve the continuous process improvement.

Manufacturer "B" is using Statistical Process Control (SPC). SPC is defined as a management philosophy directed towards the prevention of defects, as opposed to detection, through continual reduction in process and product variation. Variation is the real enemy in the manufacturing process. By establishing target values for all variables in a process and by striving to minimize the variation around the "target" value, the full benefits of process control can be realized.

Figure 1 illustrates the basic difference between part-control and process-control. Here we look at the output of a certain manufacturing step in both manufacturers' processes. Manufacturer "A" has produced the lot of widgets with the size distribution as shown. For the widgets to be useful, he must have them between his upper and lower limits. The widgets that are below size, must be scrapped. Those that are over-sized are scheduled to be re-worked. To produce the required 100 units for the next stage in the process, Manufacturer "A" must build 150 units, inspect all 150 units, scrap 25 units, and re-work 25 units.

Meanwhile, Manufacturer "B" has already achieved control of this single step in the process and has produced the lot of widgets with the distribution as shown. Manufacturer "B" has only had to make 100 widgets to get 100 widgets to the next stage in the process. He has no re-work, no scrap, and has only sample inspected the 100 units.

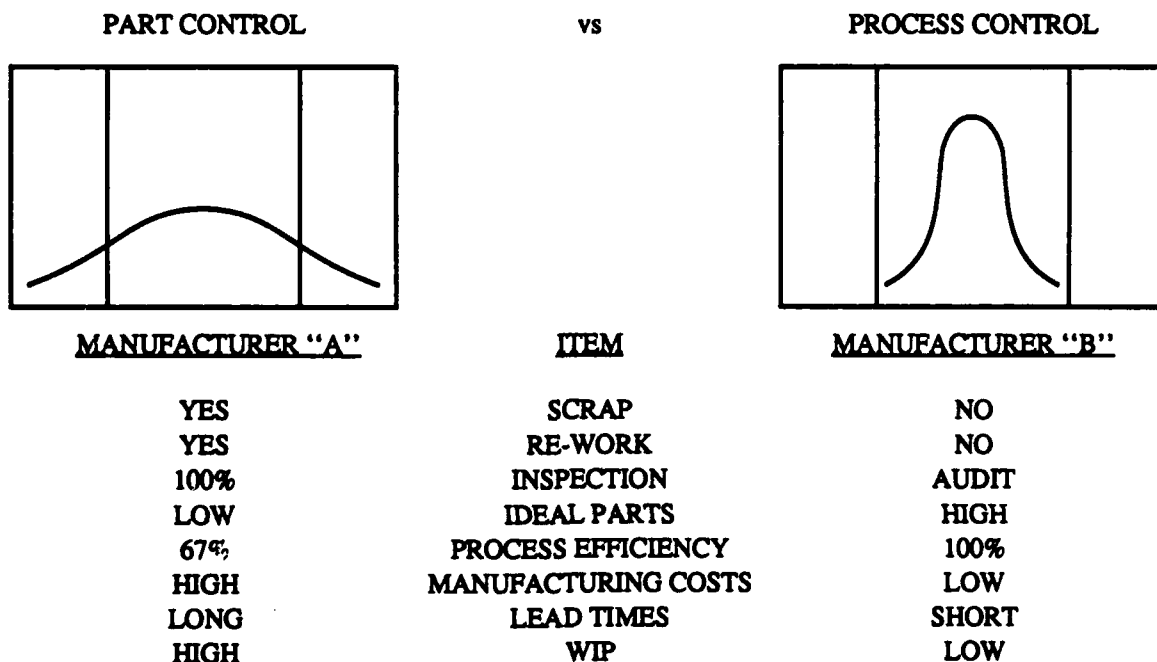


FIGURE 1. Part Control vs Process Control.

The management of Manufacturer "A" reacts to the high scrap rate and demands that it be reduced. The production personnel, using part control, shift the target size from the middle of the upper and lower limits towards the upper side. Now, manufacturer "A" produces only 105 widgets, inspects 105 widgets, scraps 5, but reworks 50 widgets. Not only has this manufacturer increased the re-work, but the number of actual widgets that are at the ideal size has been greatly reduced, while the number near the marginal upper limit has been increased. Clearly Manufacturer "B" has the advantage in cost, time, and quality.

CHANGING THE WAY WE DO BUSINESS

To be successful in the ever-changing world market, it is essential that manufacturing must be more efficient. SPC has been shown to provide just the efficiencies required. Successful implementation of SPC in manufacturing demands a strong commitment and involvement from company management. Fundamentally, this requires a change in the basic way we do business, changing from Manufacturer type "A" to Manufacturer type "B."

For this change to take place, it is essential that management must provide the mission statement, fund the planning, provide for personnel training in SPC methodology, and fund the continual process improvement. In many cases, additional capital equipment expenditures are necessary, along with establishing the total quality team.

Table 1 lists the basic steps in establishing and implementing an SPC program. A very significant part of the SPC plan is that it is an on-going and continuous process.

TABLE 1. Steps in Establishing and Implementing an SPC Program.

1. Obtain Management Commitment	8. Select a Process Improvement Project
2. Assign Responsible Personnel for Implementation	9. Quantify the Problem
3. Develop Strategic Plan	10. Do Problem Solving Using Measurement Tools, AND Controlled Experimentation
4. Determine Cost of Quality	11. Implement Corrective Action
5. Institute On-going Training Company-wide	12. Recognize and Publish Success
6. Establish All Employees as Part of the Quality Team	13. Identify Other Projects
7. Establish Problem Solving Hit Teams	14. Loop Continuously Items 7 Through 13

AUTOMATED INSPECTION AND PROCESS VARIABLE MEASUREMENT

When a manufacturer decides to change to SPC, and execute the steps necessary, it is important that a precise set of measurement tools are used. Measurement of belt-speed, pre-heat temperature profile, placement accuracy, and solder paste application are but a few of the variables that need to be quantified. Scanned-Beam Laminography has proven to be very useful in characterizing a number of process variables.

Scanned-Beam Laminography was invented in 1986 by Four Pi Systems and has been previously described (References 1 and 2). By generating cross-sectional X-ray slice images of solder connections, detailed measurements can be taken for both process monitoring and controlled experimentation. The 3-DX system can inspect solder paste application and parts placement—before reflow and immediately following the soldering process. After reflow, solder joints and components are ready for a final examination of the completed assembly. Other manufacturing problems created before soldering are often discovered here.

The automated 3-Dimensional X-ray inspection system for solder connections can generate up to 27 gigabytes of data per day in the normal course of inspecting circuit boards, enough to fill a small truck full of floppy disks. This number represents 13,500 X-ray images per hour, each image containing 245,760 8-bit bytes (one byte per pixel), during an 8-hour shift. This large amount of data is unmanageable unless it is reduced in real time, by a fully automated computer system, to a readable inspection report and a set of process measurements. The system therefore provides a variety of high-level reports to answer the need for on-line process knowledge.

Defects Reporter		
Version 1.2	Four Pi Systems	July 12, 1989
Inspection Results for PC Motherboard PVS-2h-4518 Total Test Time 3.4 minutes		
Device	Pin	Defect
C6	1	Lifted
C23	1	Insufficient
R43	2	Excess
R57	1	Insufficient
R102	2	Lifted
U13	66	Lifted
U27	1	Device Misaligned
U111	24	Misaligned Lead
U123	3	Bridging
U123	8	Solder Balls
U123	10	Voids
<SPACE BAR> to scroll results or <ESC> to stop display.		

FIGURE 2. Defects Reporter.

DEFECTS REPORT

The Scanned-Beam Laminography system first analyzes image data automatically, in real time, using feature recognition algorithms to detect any defects or out-of-tolerance conditions. These are then listed in an inspection report for each board (Figure 2). Defective conditions are identified by device name and pin number (these are known from the CAD data input during initial board programming of the system), and by defect classification. The Defect Report is the most basic reporting requirement, and is used primarily for accept/reject screening, attribute measurement, and repairs. Table 2 gives the basic defects detected and the general correlation to process variables.

TABLE 2. Defects Correlated to Process Variables.

DEFECTS	PROCESS VARIABLES
Bridging	Solder volume, placement, paste type, wave height, air knife
Poor Fillet Quality	Part wetting, board wetting, reflow temp., poor flux, wave height, contamination
Open	Lead bending, solder volume, wave height, air knife, non-coplanarity
Solder Balls	Paste drying, pre-heat, paste viscosity
Insufficient Solder	Screening plugged, wrong paste, wave height, belt speed, screen design
Voiding	Paste drying, trapped organics, outgassing, contamination
Excess Solder	Wrong screen, wrong paste, wave height, paste viscosity, screen design
Lifted Lead	Parts handling, parts specification, non-coplanarity
Tombstoning	Poor placement, excess solder, poor heating, wrong pad size, poor wetting (oxidization)
Misaligned	Poor placement, movement during reflow, mismatch between component and land pattern

PROCESS CONTROL DATA AND REPORTS

Although the defect report has great value for quality control and represents a great improvement over inconsistent, subjective human inspection results—it does not provide the kind of knowledge needed to monitor and control process variables before defects are generated. To enable process control, the automated inspection system must also analyze and report trends in process variables that occur before defects are generated. Additionally, when used in a controlled experiment, the 3DX provides detailed data for use in the correlation studies.

Table 3 shows a partial list of the process parameters measurements generated by the system. These measurements cover a wide range of characteristics relating to solder joint formation and integrity, including effects of component and paste placement. The amount of measurement information is approximately 100 bytes of information to be reported for each and every solder joint. In producing 160 typical circuit boards per day, each containing 2000 solder joints, 32 megabytes of measurement data is produced each day.

TABLE 3. Process Control Measurements Performed by Automated Scanned-Beam Laminography.

DEFECT TYPE	MEASUREMENTS
Bridging	Width and X,Y location of any solder bridges found
Balls	Diameter and X,Y location of any solder balls found
Solder Splash	Area and X,Y location
Voids	Diameter and location of any voids; also, total amount of voiding present, expressed as a percentage of solder joint volume.
Lead/Pad Alignment	X,Y distance of offset between lead and pad
Insufficient?Excess	Volume of solder, as a percentage of nominal solder volume
Stand-off Height	Thickness of the solder layer under the chip or chip carrier
Lifted Lead	Magnitude of lead lift
Solder Spikes	Length and location of any spikes found
Device Joint Uniformity	Average and standard deviation of solder joint volumes for a given device, measured as a percentage of nominal solder joint volume.

CONTROL REPORTS

The ability to generate immediate reports with lots of data is one of the great advantages of automated inspection. With manual methods, using human vision, the feedback loop is too long. It may take days or weeks to accumulate and compile raw data from human inspectors and interpret the results. By that time, many components may have been soldered.

Due to the subjective inconsistency of humans, real-time knowledge for the feedback loop is hard to obtain. Three different inspectors can come up with six different descriptions of any particular solder defect. What looks like "cold" solder on Monday may look to be good on Friday, and what looks like "insufficient solder" to one inspector may look like "lifted lead" to another inspector. This inherent inconsistency slows the feedback loop because the inspection results must be questioned and rechecked. In most cases, these

subjective human inconsistencies are so difficult to overcome that process control reports are not even worth the effort. Because the automated 3-D X-ray system provides consistent quantitative measurements of solder joint structure, in real-time, it allows scientific statistical process control methods to be used.

Many companies have identified the learning cycle, during production prototype, to be the most difficult and lengthy process for their new products. This learning cycle can lead to a undesirably long time-to-market for these new products. By use of an inspection system, such as Scanned-Beam Laminography, and conducting controlled experimentation during the crucial start-up phase, the time-to-market may be substantially reduced with the real-time process control knowledge obtained through laminography, and the subsequent optimization of the process.

SAMPLE CASE STUDIES

The following section provides some results of the use of the 3DX Laminography System to characterize some aspects of manufacturing.

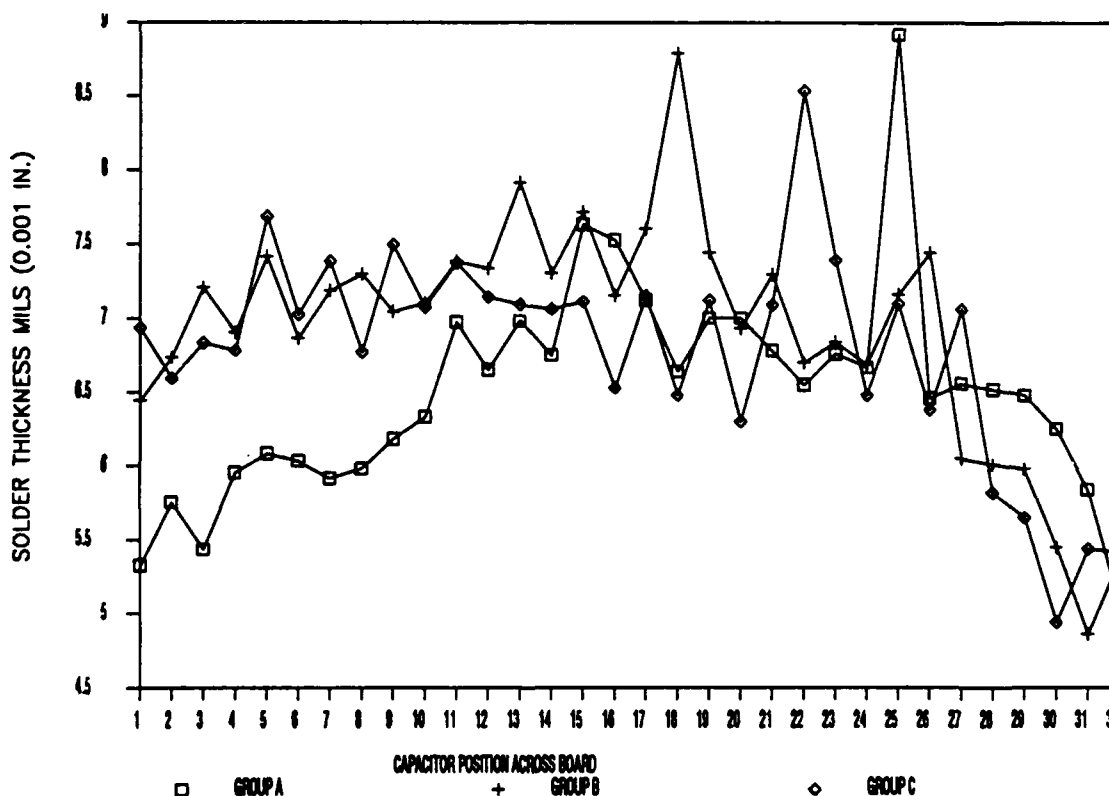


FIGURE 3. Solder Thickness - Board 2t101 (Capacitor Groups A, B, and C)

SOLDER PASTE STUDY

The feasibility of measuring the uniformity and alignment of the solder paste was examined by using the data from the 3DX Laminography System. This manufacturer intends to sample the first up article after paste application, after parts placement, and after reflow. This manufacturer hopes to minimize the time it takes to check that his line is set up to run a board type after changeover. What has normally taken him hours to check can be accomplished in a few minutes with the data from the 3DX Laminography System. In addition, this manufacturer will use the 3DX system to characterize his new product designs.

SOLDER VOLUME AND UNIFORMITY STUDY

The Insufficient/Excess Solder Algorithm returns the average solder joint thickness as a process control variable. The manufacturer in this study was in the process of evaluating and setting up a wave flow solder machine for soldering chip resistors and capacitors to the bottom of a double-sided surface-mount board. The manufacturer produced a number of test boards soldered under various conditions in the wave solder machine under study. These boards were then quantitatively analyzed on the 3DX Laminography System. Figure 3 shows the solder thickness plot across several rows of capacitors for one of the test boards. Note that the plot shows a trend of thicker solder deposited in the center of the board than at the edges. Also note that there is a trend of "excessive" solder on several central joints. Several machine variables were adjusted and the results show in Figure 4. Here note that the average solder thickness is about the same as Figure 3 but that the uniformity across the board is much better. The adjustments were made in wave height and in the air knife.

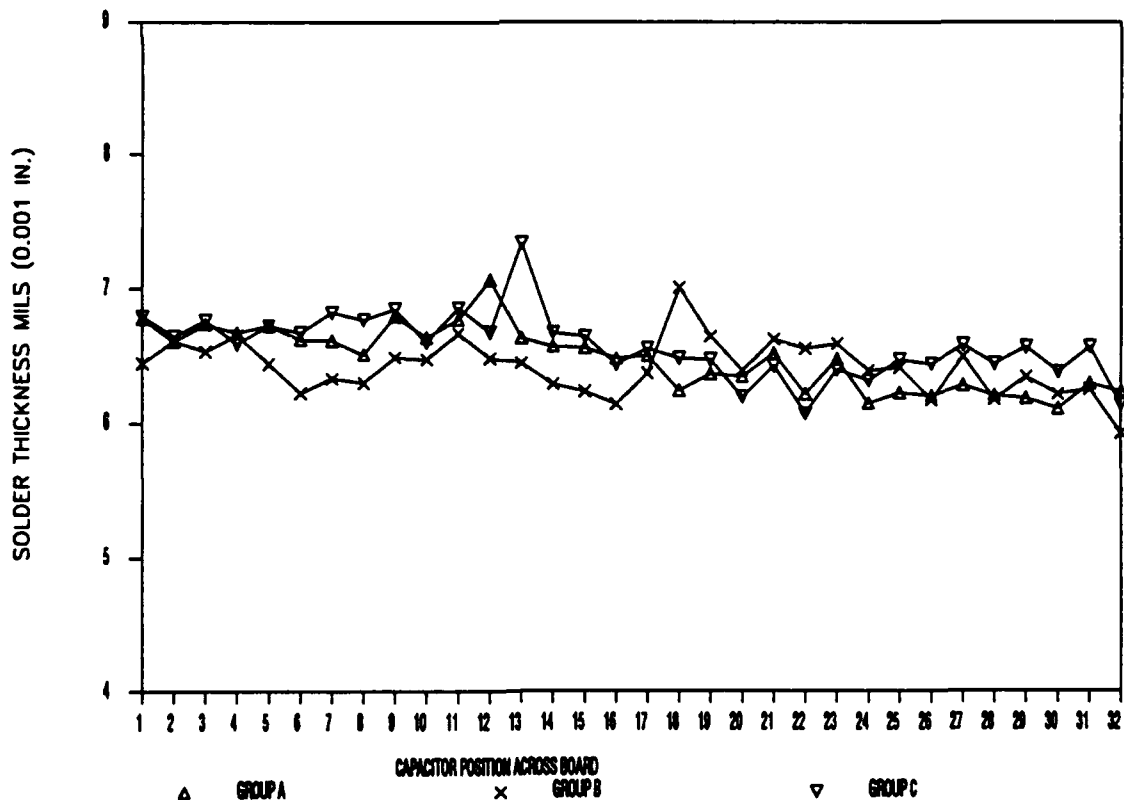


FIGURE 4. Solder Thickness - Board 3t104 (Capacitor Groups A, B, and C)

DEVICE STAND-OFF DISTANCE

A manufacturer of surface mount boards using leadless chip carriers was experiencing difficulty in controlling the stand-off of the device from the board. The algorithm for device solder joint uniformity indicated that the problem was not just one component or one area of the board. The manufacturer then went to a controlled stand-off method and the corresponding devices on the boards were quite uniform. This manufacturer achieved a controlled standoff of 0.005 inch, as opposed to an average of 0.0015 inch without controlled stand-off.

VOIDING STUDY

Voids in SOIC heal fillets and J-Lead heal and toe fillets was evidenced by one manufacturer. This manufacturer conducted a series of controlled experimentation by varying paste dry times, dwell times, and reflow conditions. Through this experimentation and the detailed data provided by the 3DX laminography, this manufacturer was able to virtually eliminate this problem with his SOIC and J-Lead components, going from around 1 percent voids to less than 10 parts per million voids.

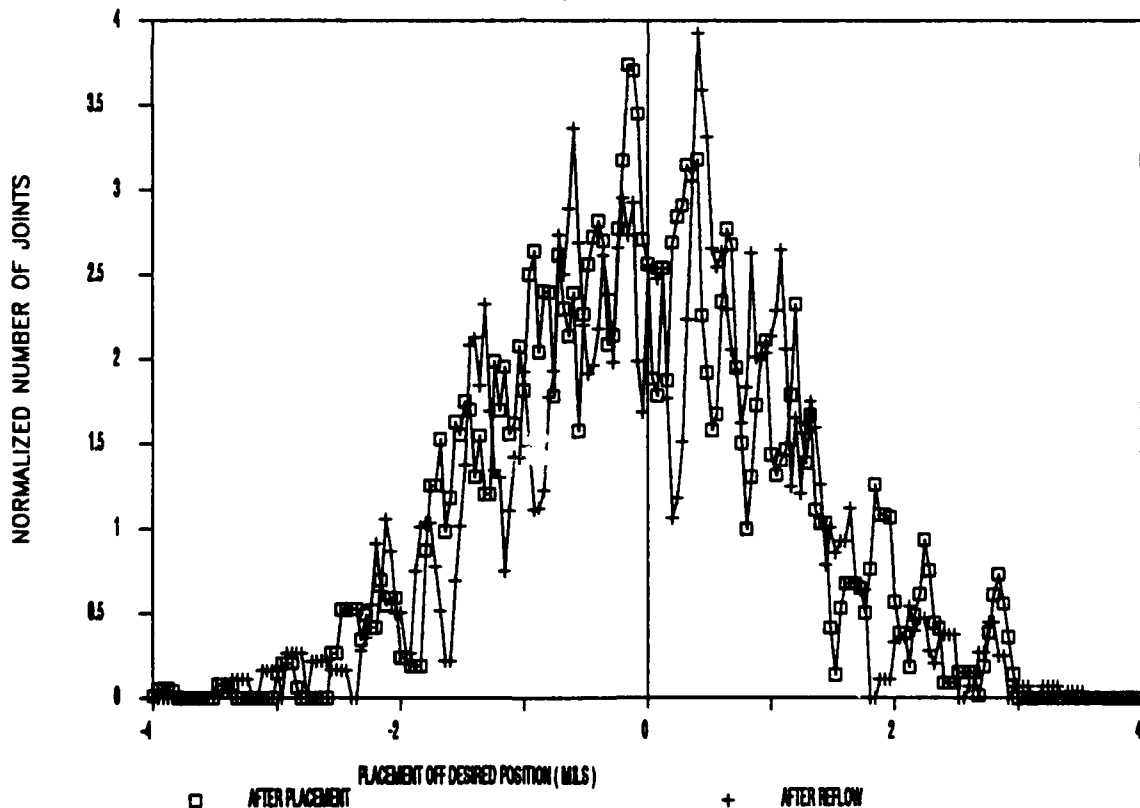


FIGURE 5. Device Alignment Study (After Placement and Re-flow)

DEVICE ALIGNMENT STUDY

This manufacturer was concerned with the placement accuracy of his new pick and place machine, before solder reflow as compared to post reflow placement. A set of boards was examined after placement in solder paste and then re-flowed and examined again. The alignment data for J-Leads is shown in Figure 5. Note that no significant difference was determined between the recently placed board and after reflow.

RECENT DEVELOPMENTS IN NATIONAL STANDARDS

In an article by William C. Ross (Reference 3), a number of recent developments in the area of Standards and General Requirements for process improvement have been described and discussed. These developments show that both industry and government are rapidly moving towards implementation of SPC methods for defense electronics. Table 4 lists these recent standards.

TABLE 4. Recent Developments in Process Improvements.

The Department of Defense	<i>"Total Quality Management (TQM) Initiative"</i>
The Tri-Service Process Control Document	<i>"MIL-STD-2000"</i>
Joint Electronic Device Engineering Council	<i>JEDEC Standard No. 19"</i>
Electronics Industries Association	<i>"ANSI/EIA-557 Statistical Process Control Systems"</i>
Institute for Interconnecting and Packaging Electronic Circuits	<i>"IPC-PC-90"</i>

These publications serve as tools and "cookbooks" for establishing a total quality management plan and for providing continuous process improvement through SPC. The author highly recommends their review.

SUMMARY

"I often say that when you can measure what you are talking about and express it in numbers, you know something about it; but when you cannot measure it, when you cannot express it in numbers, your knowledge is of a meagre and unsatisfactory kind."

--Lord Kelvin (Reference 4)

The new world of manufacture of precision circuit board assemblies is very difficult, with the large numbers of hidden connections, with connections becoming smaller and smaller, with Pin Grid Arrays (PGAs) and Pad Grid Array packages coming into common usage, with J-Leads, Leadless Chip Carriers (LCCs) and fine pitch SMDs being used. In this new world, the attempt to measure and monitor quality through human vision alone becomes a tedious process and, according to Lord Kelvin, results in knowledge

of a meagre and unsatisfactory kind. With the proper automated measurement tools, we can begin to know something about the process. Only after we know about the process, its variables, attributes, and cause and effect relationships, can we then implement changes to assure zero defects.

The use of detailed measurement tools, such as a fully automated post-solder inspection system with both inspection and process control reporting, has a high pay back rate in the highly competitive world of 1990.

REFERENCES

1. J. Adams, *Real Time Laminography - Slicing Solder Inspection Down to Size*, Naval Weapons Center, China Lake, CA, March 1989, NWC TP 6986, 13th Annual Electronics Manufacturing Seminar Proceedings.
2. J. Adams, *Scanned-Beam Laminography Breaks Through the 3-D Barrier*, Proceedings, NEPCON WEST '89, March 6-9, 1989, Anaheim California, Cahners Exposition Group.
3. William C. Ross, *National Standards For Total Quality Through SPC*, PC FAB, November 1989.
4. Wadsworth et al, *Modern Methods for Quality Control and Improvement*, John Wiley & Sons, 1986. ISBN 0-471-87695-X.

NOTE 1. Author's Disclaimer--Manufacturers "A" and "B" are the author's fictional combinations of many manufacturers and not any individual manufacturer or company.

John Adams is the Chief Scientist at Four Pi Systems, a corporation he helped found in 1986. Prior to that time, he had worked for more than 8 years developing fully automated measurement, inspection, and analysis equipment for a broad range of applications. He is one of the principal inventors of a fully automated, X-ray based, inspection system for circuit boards and is also one of the inventors of Scanned-Beam Laminography. John holds a Ph.D. degree in Physics from Arizona State University and has published various articles on automation in the United States and Europe.

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A NEW TECHNIQUE FOR MONITORING SOLDER PASTE CHARACTERISTICS

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ABSTRACT

As electronics manufacturing comes to rely more heavily on statistical process control, new methods of monitoring process parameters will be needed. One area that requires attention is the monitoring of solder paste characteristics during surface mount circuit assembly. This presentation proposes a new technique for in-process monitoring of solder paste characteristics.

Alternating current electrical impedance measurements have been used to monitor micro-structural changes in a wide range of materials. Techniques for monitoring AC impedance changes are compatible with requirements for statistical process control of surface mount assembly. The techniques yield quantitative results, and in-process monitoring of solder paste characteristics is feasible using this approach. Furthermore, the basic constituents of solder paste possess the types of micro-structural elements readily resolved by AC impedance measurements.

This report describes the results of a study which investigated the use of AC impedance measurement and analysis techniques to monitor the physio-chemical changes that occur in solder paste during activation. Results indicate that changes in solder paste caused by heating and aging can be non-destructively monitored using AC impedance measurements. Specifically, the techniques appear to be

capable of monitoring solder power oxidation and flux activation. Significantly, it is shown that the existing body of knowledge pertaining to the analysis and interpretation of AC impedance measurements is directly applicable to solder paste materials.

STATEMENT OF THE PROBLEM

Currently, there is considerable activity in the area of solderability testing and standards for surface mount technology. Much of this work has centered on surface mount components and circuit substrates, the intent of the work being to establish conditions that will produce a high yield of reliable solder joints. The properties of the solder pastes used for vapor phase and infra-red reflow processes also have a major impact on the creation of reliable solder joints. To insure a high yield of reliable joints, solderability test methods and standards for solder paste are also necessary.

(The concept of "solderability of solder paste" as used here refers to the degree to which solder paste facilitates the creation of a reliable surface mount solder joint. The concept includes such factors as the ability of the flux component of the paste to enhance wetting of the surfaces participating in the joint, but does not include factors such as solder pad print definition.)

General quality control tests for solder paste are well known (Reference 1). The two widely used tests which relate most directly to solderability are the solder ball test, which reflects the level of oxidation of the solder powder in the paste, and the wetting test, which tests the activity of the paste flux.

There are several issues that must be addressed regarding these tests. First, standard procedures and acceptance criteria for these tests must be established for both military and non-military customers and suppliers. Second, a means of enhancing the significance of these tests must be developed; the variables measured by these tests must be related to actual solder process variables, yields, and ultimately, solder joint reliability.

In addition to these issues, special attention must be given to the development of solder paste testing methods that are suitable for statistical process control of soldering processes. Specifically, solder paste tests should be capable of providing quantitative results

which can be directly related to variations in significant solder paste characteristics. Furthermore, the tests should not be sensitive to minor variations in test procedures or to variations in non-significant characteristics.

There is another desirable trait of tests designed for statistical process control. Ideally, a test should be capable of being performed "in vivo" as well as "in vitro". The tests should be capable of being performed directly on products or materials while various manufacturing processes are performed, as well as on samples of products or materials removed from the manufacturing flow specifically for testing. To encourage use as process control tools, the tests should also be fast and easy to perform.

Finally, it is generally desirable to devise tests of solder paste solderability that provide direct indications of conditions within the paste. Wetting, for example, is a complex process relying on many factors, one of which is flux activity. Similarly, solder balling is a complex phenomenon depending, in part, on solder paste powder oxidation. It would be desirable to have tests that directly indicate the degree of solder paste flux activity and solder powder oxidation, as well as tests that reflect general wetting and solder balling behavior.

Such tests would address both the causes of solder paste solderability problems (e.g., solder powder oxidation) as well as tests directed at symptoms of these problems (e.g., solder balling). What is needed are tests which reveal changes occurring at the microscopic level within the significant solder paste constituents (e.g., thickening of the oxide layer on solder particles), as well as changes in the macrostructural properties of the material (e.g., solder balling).

To emphasize the previous points, consider how the solderability of solder paste might currently be monitored during the solder paste printing operation. The most widely accepted techniques for testing solder balling and wetting of solder paste require: that small samples be removed from the mass of solder being printed; that the samples be printed onto specially prepared substrates that may bear little resemblance to the materials actually participating in the actual solder joint being created; and that the samples be reflowed under conditions that are often different from those encountered during production. These tests are often performed at a location both physically and temporally remote from the printing operation.

Given this situation, to what degree can these tests provide unequivocal information on the yield and reliability of the actual solder joints being produced? To what extent can the results of these tests be used to fine-tune assembly processes to improve solder joint yield and reliability?

Consider also that new solder paste formulations allow for periods of several days between solder paste printing and reflow. How should the solderability of the printed solder paste be evaluated after this interval of time? How can solderability measurements made at reflow time be correlated with those made at print time? How does one use current tests to predict the allowable interval between print and reflow for a mass of solder currently being printed?

In summary, the issue being addressed here is two-fold. First, new solder paste tests should generate on-line real-time quantitative solderability data. Second, the tests should produce information on the microscopic changes within solder paste which cause variations in solder joint yield and reliability.

A POTENTIAL SOLUTION

There exist a number of techniques for studying changes in the properties of materials at the microscopic level. For example, the scanning electron microscope can be used to examine both the microstructure and chemical composition of materials. Unfortunately, this approach requires extensive, time-consuming sample preparation techniques which can modify the properties of many types of materials, making the approach poorly suited to on-line production monitoring applications. Other techniques which are better suited to on-line monitoring are often not as sensitive to microscopic changes, which limits the amount of useful information provided by these techniques. Furthermore, many of these techniques require complex, expensive equipment.

Alternating current electrical impedance measurement techniques have the ability to produce real-time information concerning the microscopic physio-chemical processes which determine the properties of a variety of materials. AC impedance techniques have provided such information for a wide range of applications. For example, polycrystalline zinc oxide, calcia, and zirconia have been studied extensively using these techniques (Reference 2-8). At the other end of the spectrum of applications, AC impedance techniques have been used to monitor "in vivo" changes in a wide variety of living plant and animal systems (References 9-12).

The theories describing the phenomena responsible for the AC impedance characteristics of materials are well established (References 13-15), and a number of experimental techniques have been developed (References 16-18). Typically, no extensive sample preparation is required, and automated systems can perform measurements over wide ranges of values in a matter of seconds.

AC impedance techniques are best suited to monitoring changes in materials of heterogeneous composition. These techniques have yielded information on changes in the dimensions and physical properties of microscopic structural elements such as interfacial barrier layers which occur in heterogeneous materials. In addition, the techniques have been used to obtain information on the nature of grain boundaries in polycrystalline ceramics, and the behavior of cell walls and membranes within living systems.

The techniques have also shown themselves to be well-suited to monitoring changes in the structure, composition, and concentration of polar molecules and ionic charge carriers found in these materials. The breakdown of large polar molecules into smaller elements is a type of change suitable for examination by this technique. Solder paste is a heterogeneous material consisting of oxide-coated spheres of material mixed into a matrix containing large polar molecules. The types of changes which occur at microscopic levels within the constituents of solder paste are similar to those that have already been shown to be suited to monitoring by AC impedance techniques. However, it appears that these techniques have not yet been applied to the study of solder paste. The purpose of this document is to describe how these techniques can be applied in the area of solder paste solderability, and to present a demonstration of such an application.

RESULTS AND DISCUSSION

The manner in which impedance spectroscopy can be used to evaluate solder pastes can be illustrated by a simple example. Figure 1 shows a physical model of a heterogeneous material system consisting of spheres of a material 'a' suspended in a matrix of material 'b'. Each sphere is encapsulated in a shell of material 'c'. For this example, the resistivity of material 'c' is much greater than that of material 'b', which is in turn much greater than that of material 'a'. Also, the spheres are closely-spaced within the matrix. Since the resistivity of matrix material 'b' is very high, the situation is analogous to what has been seen for insulating grain boundaries in polycrystalline

ceramics. This model provides a first-order approximation of a solder paste, where material 'a' represents the metallic solder particle, material 'b' is the flux vehicle, and material 'c' is the oxide layer surrounding the solder particle.

A lumped parameter AC electrical equivalent circuit for this system may be approximated as is seen in Figure 2a. The resistors R_a , R_b , and R_c represent the resistances of materials a, b, and c, respectively. Similarly, the capacitors C_b and C_c represent charge storage and polarization processes in the insulating materials 'b', and 'c'. These resistances and capacitances may be related to the respective path lengths, L , conduction cross sectional areas, A , materials resistivities, ρ , and permittivities, ϵ , as follows:

$$R_a = \frac{\rho_a L_a}{A_a}, \quad R_b = \frac{\rho_b L_b}{A_b}, \quad R_c = \frac{\rho_c L_c}{A_c},$$

$$C_b = \frac{\epsilon_b A_b}{L_b}, \quad \text{and} \quad C_c = \frac{\epsilon_c A_c}{L_c}.$$

Figure 2b shows the frequency response of the impedance of the circuit of Figure 2a, graphed as a complex impedance plot with the abscissa representing the real or resistive component of impedance, and the ordinate representing the imaginary or capacitive component of the impedance. If the same scale is used for both axes, then the plot of the series-measured impedance would trace semicircular paths in this plane with the centers lying on the x-axis. The values of the parameters R_a , R_b , and R_c can be obtained from the impedance plot of figure 2b in a direct manner. The capacitive quantities can be obtained from the critical frequencies, f_b , and f_c , where the reactive components of the impedance reach their maximum values, since:

$$f_b = \frac{1}{2\pi R_b C_b}, \quad \text{and} \quad f_c = \frac{1}{2\pi R_c C_c}.$$

The products of the resistance and capacitance quantities are independent of the geometrical factors of the associated regions, since

$$\tau_b = R_b C_b = \left(\frac{\rho_b L_b}{A_b} \right) \left(\frac{\epsilon_b A_b}{L_b} \right) = \rho_b \epsilon_b, \quad \text{and}$$

$$\tau_c = R_c C_c = \left(\frac{\rho_c L_c}{A_c} \right) \left(\frac{\epsilon_c A_c}{L_c} \right) = \rho_c \epsilon_c .$$

Further, the resistivities of the regions are functions of the type, concentration, and mobility of the charge carrying species in the media, while the permittivities of the regions are functionally related to the operative polarization processes, and the type and concentration of polar molecules in the media.

AC electrical impedance data has been obtained as a function of frequency (5 Hz to 13 MHz) using a HP-4192 impedance analyzer. Here, samples of solder paste were loaded into a specimen holder such that data could be recorded on disk shaped samples having a diameter of 1 cm and a thickness of 2mm. Data for solder pastes consisting of varying volume ratios of solder particles and flux vehicle are shown in Figures 3 and 4. The semicircular trace designated as $\tau_2 = \text{Tau}_2$ could be associated with the flux vehicle, while the semicircular trace designated as $\tau_1 = \text{Tau}_1$ was associated with the solder particles. It was noted that these relaxation times were functionally dependent upon the amount of flux vehicle present, as is shown in Figure 5. In addition, it was found that the conduction/polarization process responsible for the τ_2 relaxation time in the unaged paste is thermally-activated, where an Arrhenius behavior of the form,

$$\tau_2 = \tau_0 \exp \left(E_A/kT \right)$$

is observed below 60°C, (see Figure 6). Samples of fresh solder paste and vehicle, respectively, were then aged in an accelerated fashion in a sealed environment, and examined at room temperature. In both cases, the relaxation time associated with the vehicle increased as is summarized in Table I.

Two additional investigations were conducted to establish the nature of the kinetics associated with the activation of fresh solder paste at elevated temperatures. In these studies, the paste was loaded into the test fixture, and the electrical response was evaluated in-situ during the course of the elevated temperature run. As is illustrated in Figure 7, the relaxation time associated with the vehicle decreased as a function of time at 50°C. It is of interest to note that this decrease exhibited a series of rate constants, indicating that the

physio-chemical changes within the vehicle that accompany the aging process are readily observed via AC electrical measurements. In contrast, a similar study conducted at 80°C revealed that this relaxation time, while decreasing initially, increased thereafter as is noted in Figure 8. Further, although not evident at 50°C or at time zero at 80°C, the relaxation time associated with the particle oxide layer (τ_1) emerged within the first hour of aging at 80°C, as is shown in Figure 9, and subsequently decreased as a function of time, per Figure 10. It is felt that this decrease may reflect a slow reduction of the oxide layers surrounding the metal particles.

CONCLUSION

These results indicate that the microstructural and physio-chemical processes inherent in metal particle/flux vehicle solder pastes can be measured utilizing AC small-signal impedance techniques. These features can be interpreted in terms of an equivalent electrical circuit representation via lumped parameter/complex plane analysis of the AC data. Further, it is found that the physio-chemical processes and/or microstructural changes accompanying aging of these materials can be monitored using these methods.

REFERENCES

1. B. Roos-Kozel. "Solder Pastes," in Surface Mount Technology, Silver Spring, Maryland, Int. Soc. for Hybrid Microelectronics, (1984), p. 115.
2. J. Volger, "Dielectric Properties of Solids In Relation to Imperfections" Progress In Semiconductors, Edited by A.F. Gibson, Wiley and Sons, N.Y. 4, (1960), p. 207.
3. M. Seitz, F. Hampton, W. Richmond, "The Influence of Chemisorbed Oxygen on the AC Electrical Behavior of Polycrystalline ZnO", Advances in Ceramics - Vol. 7 Edited by M.F. Yan and A.H. Heuer, American Ceramics Society, Columbus, OH (1983), p. 60.
4. M. Alim, M. Seitz, and R. Hirthe "Complex Plane Analysis of Trapping Phenomena in Zinc Oxide Based Varistor Grain Boundaries", Journal of Applied Physics, Vol. 63, (1988) p. 2337.
5. W. Richmond, and M. Seitz. "ZnO - based Varistor: A Model and Characteristics," Advances in Ceramics - Vol. 1, Edited by L.M. Levinson, American Ceramics Society Columbus, OH, (1981), p. 425.
6. J. Bauerle. "Study of Solid Electrolyte Polarization by a Complex Admittance Method" Journal of Phys. Chem Solids, Vol. 30 (1969), p. 2657.
7. M. Seitz, and W. Orlow. "Influence of Grain Boundaries on Electrical Behavior of Polycrystalline $ZrO_2-Y_2O_3$ ", Advances in Ceramics - Vol. 1, Edited by L.M. Levinson American Ceramics Society, Columbus, OH (1981), p. 124
8. S. Chu, and M. Seitz. "The AC Electrical Behavior of Polycrystalline ZrO_2-CaO " Sol. State Chem., Vol. 2 (1978), p. 297.

9. H. Schwan. "Alternating Current Spectroscopy o Biological Substances," Proc. IRE, Vol 47 (1954), p 1841.
10. R. Hayden, et al.. "Electrical Impedance Studies o Potato and Alfalfa Tissue," Journal Exp. Bot., Vol. 2 (1969), p. 177.
11. M. Polczynski. "Monitoring Kinetic Processes i Biological Systems Using AC Impedance Measurements, doctoral dissertation, Marquette University, Milwaukee Wisconsin, 1978.
12. J. Ackman, C. Dawson, M. Seitz, and A. Sances. "Comple Bioelectric Impedance Measurements for the Detection o Pulmonary Edema" Digest of the 11th International Conference on Medical and Biological Engineering, Ottawa Canada, 1976.
13. M. Seitz, "Study of Heterogeneous Composite Materials vi Lumped Parameter/Complex Plane Analysis," Int. J. Hybri Microelectronics, Vol. 3 (1980) p. 1.
14. K. Cole, and R. Cole. "Dispersion and Absorption i Dielectrics," J. Chem. Phys., Vol 9 (1941), p. 341.
15. F. Grant. "Use of Complex Conductivity in th Representation of Dielectric Phenomena." J. Appl. Phys. Vol 29 (1958), p. 76.
16. J. Ackmann, and M. Seitz. "Methods of Complex Impedanc Measurements in Biologic Tissue," CRC Critical Review in Biomedical Engineering, Vol. 11, No. 4 (1984), p. 281
17. H. Schwan, and C. Ferris. "Four-Electrode Nul Techniques for Impedance Measurement with Hig Resolution," Rev. Sci. Instrum, Vol. 39 No. 4 (1968) p. 481.
18. M. Polczynski, and M. Seitz. "Low-frequency 4-Prob Impedance Measuring System" Med. Biol. Eng. & Comp., Vo 15 (1977), p. 573.

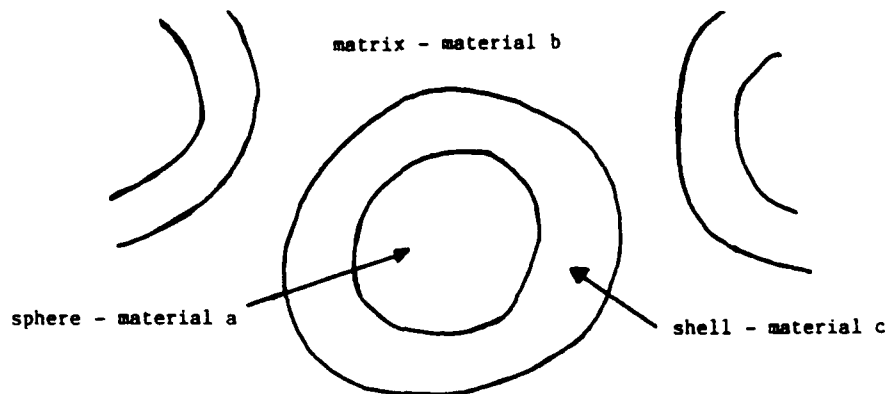


FIGURE 1. Physical Model of a Heterogeneous Material Having a Microstructure Analogous To Solder Paste.

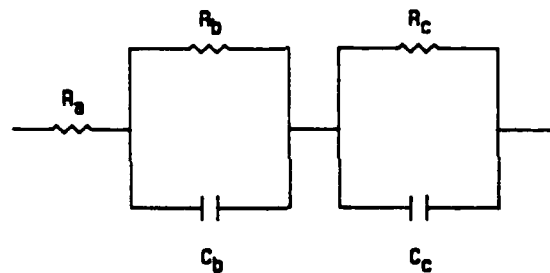


FIGURE 2a. Lumped Parameter Equivalent Circuit Model For The Physical Situation Shown in FIGURE 1.

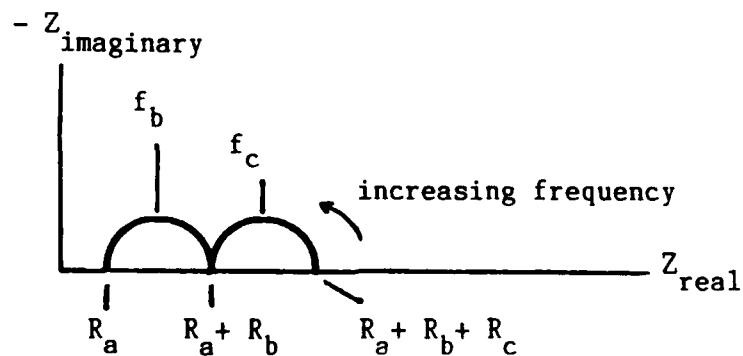


FIGURE 2b. Complex Plane Impedance Plot For The Circuit Shown in FIGURE 2a.

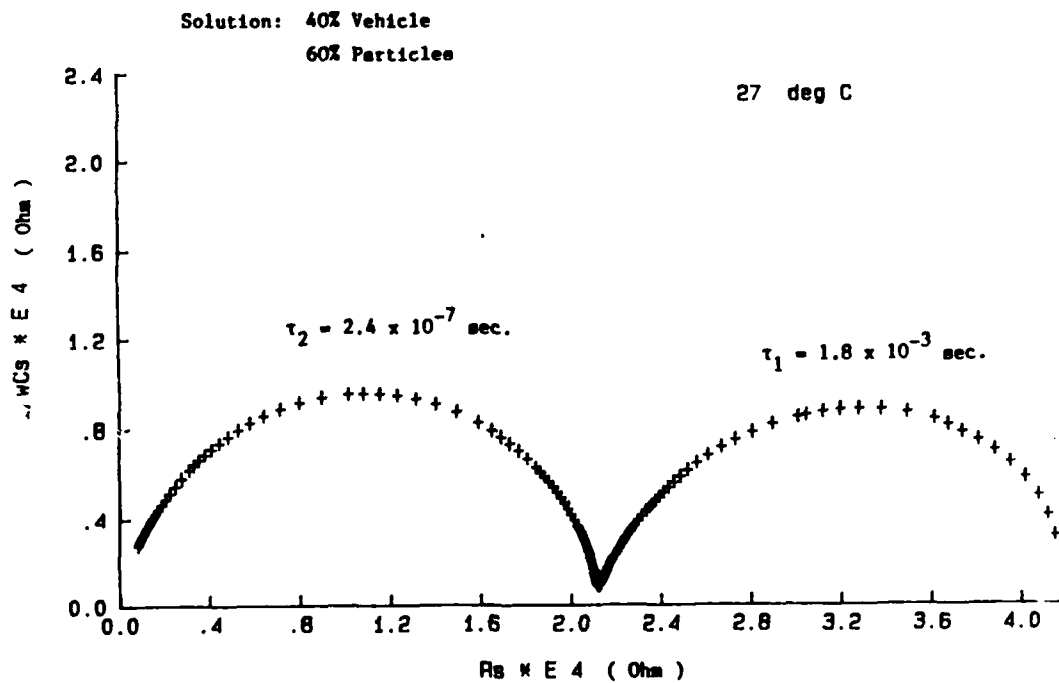
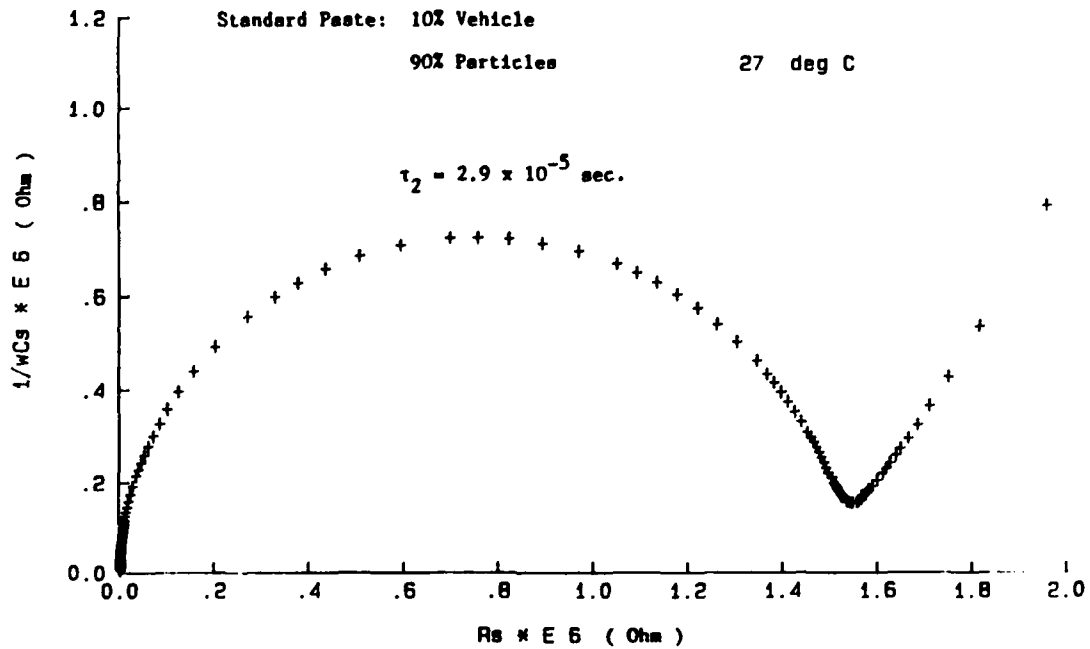


FIGURE 3. Complex Impedance Plots For Solder Paste
Compositions Containing 10% and 40% Vehicle.

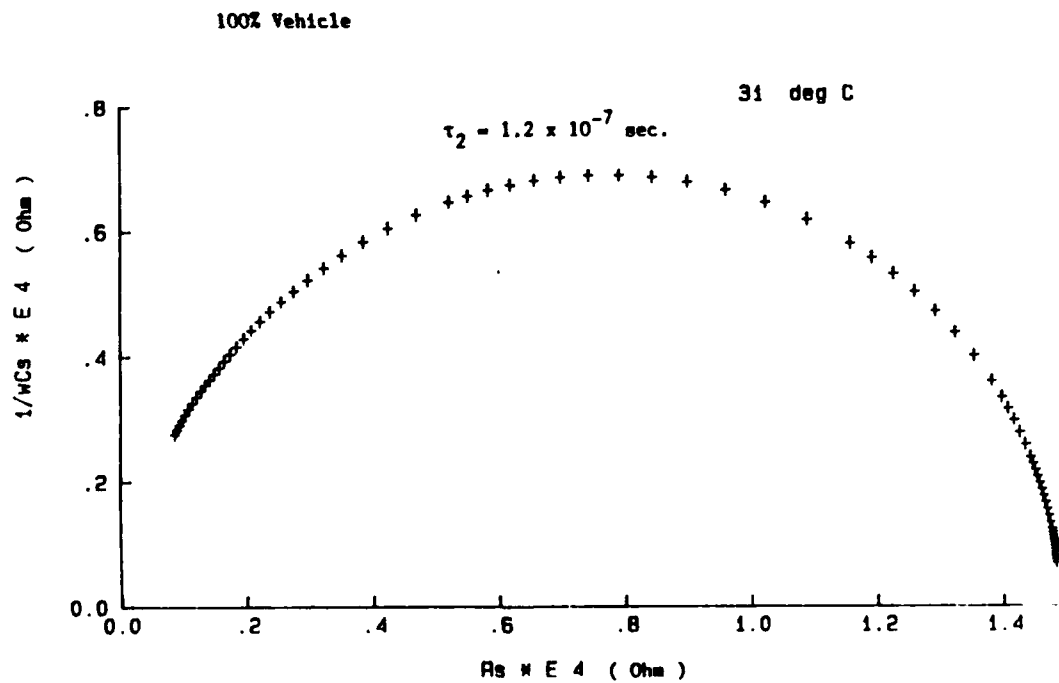
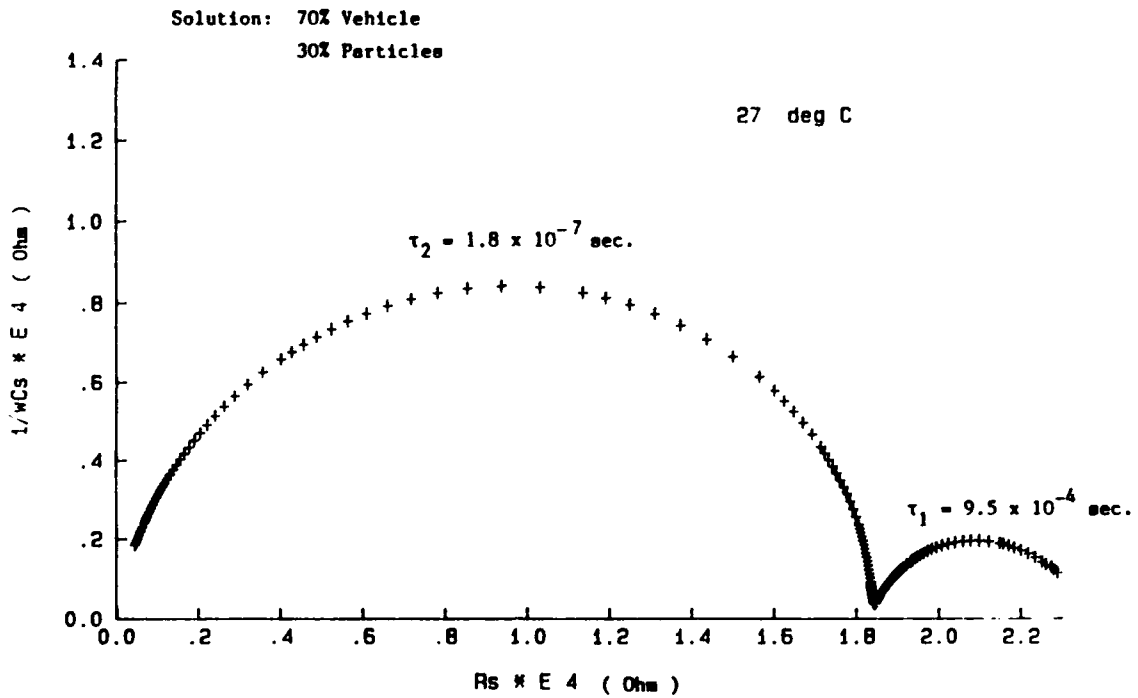


FIGURE 4. Complex Impedance Plots For The Solder Paste Composition Containing 70% Vehicle, and Unaged Vehicle.

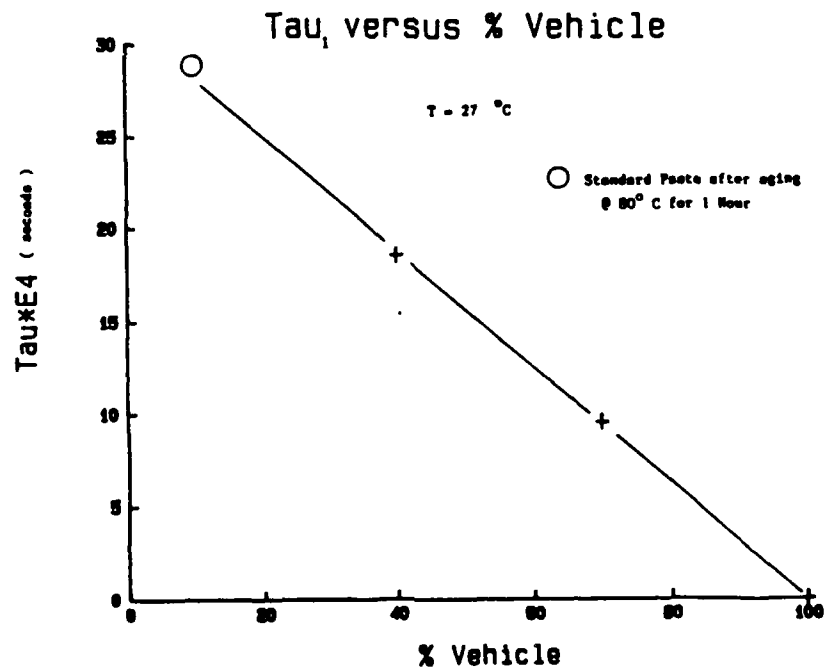
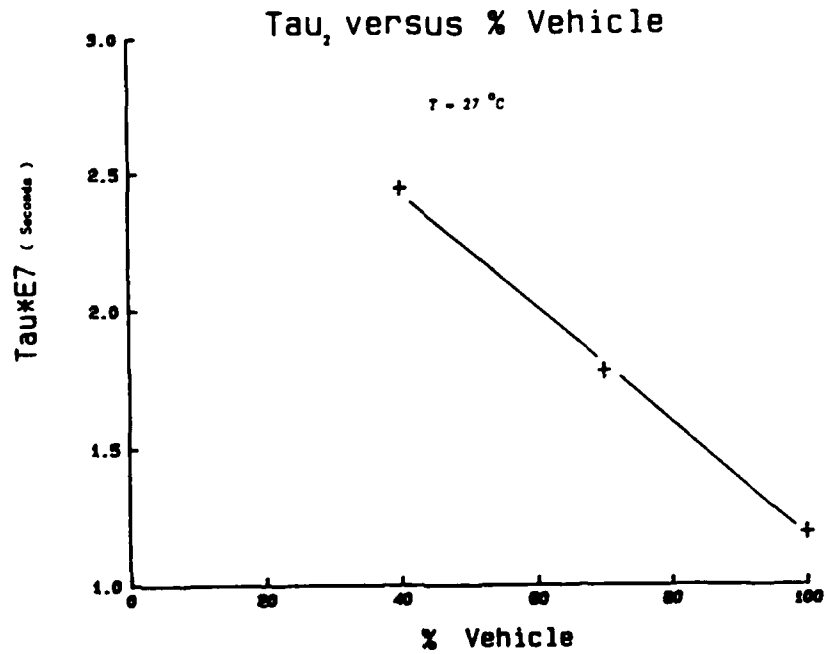


FIGURE 5. Relaxation Time, τ , as a
Function of Volume Percent Vehicle.

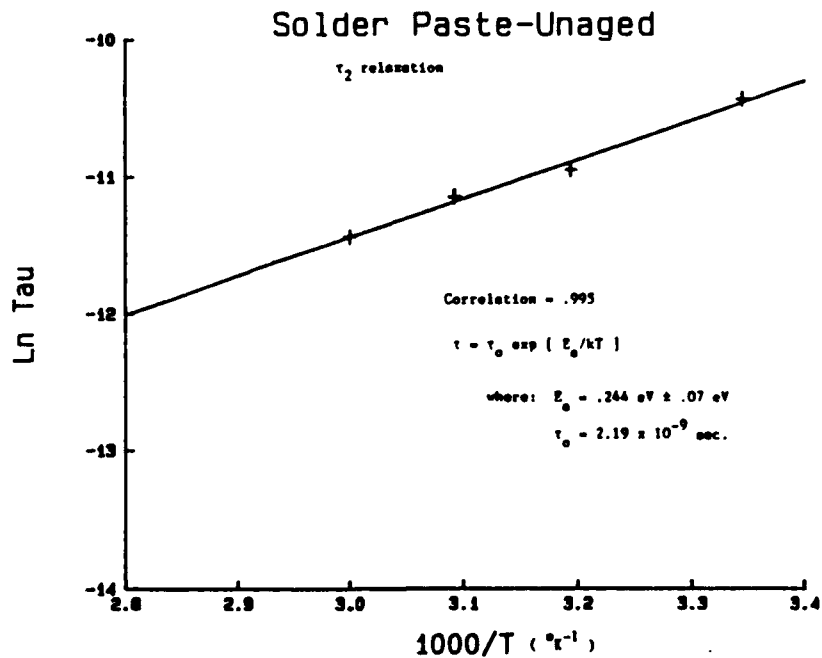


FIGURE 6. Relaxation Time, τ_2 , versus
Inverse Absolute Temperature For Unaged Paste.

TABLE I

STANDARD PASTE: @ 27° C . (τ_2 relaxation)

	<u>τ (sec)</u>	<u>C_p (Farad)</u>	<u>R_p (Ohms)</u>
Unaged:	2.92×10^{-5}	1.9×10^{-11}	1.5×10^6
Aged 5 Hrs @ 50° C	6.11×10^{-5}	2.0×10^{-11}	3.1×10^6

THINNER: @ 27° C (τ_2 relaxation)

	τ (sec)	C_p (Farad)	R_p (Ohms)
Unaged:	1.2×10^{-7}	8.3×10^{-12}	1.4×10^4
Aged 5 Hrs @ 50° C	3.2×10^{-7}	9.1×10^{-12}	3.5×10^4

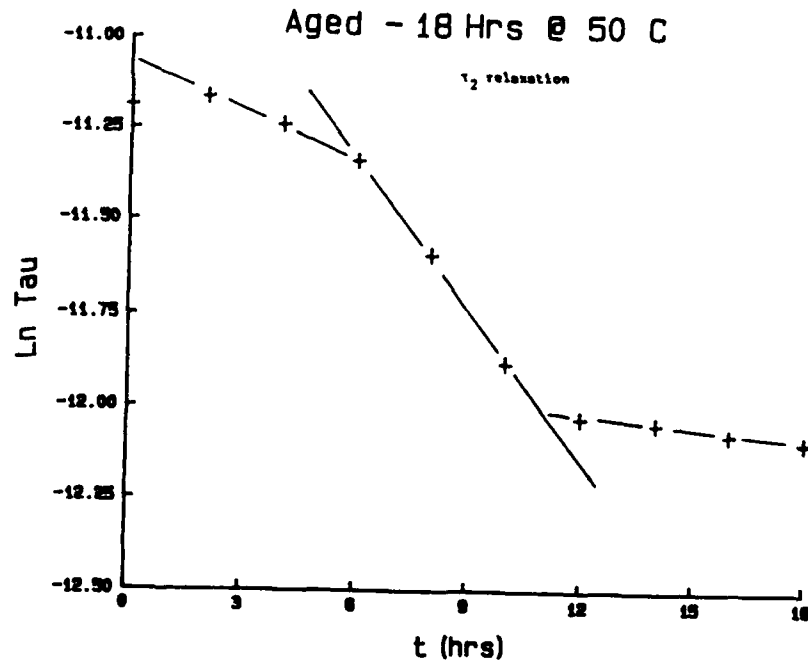


FIGURE 7. Relaxation Time, τ_2 , versus Aging Time at 50 °C.

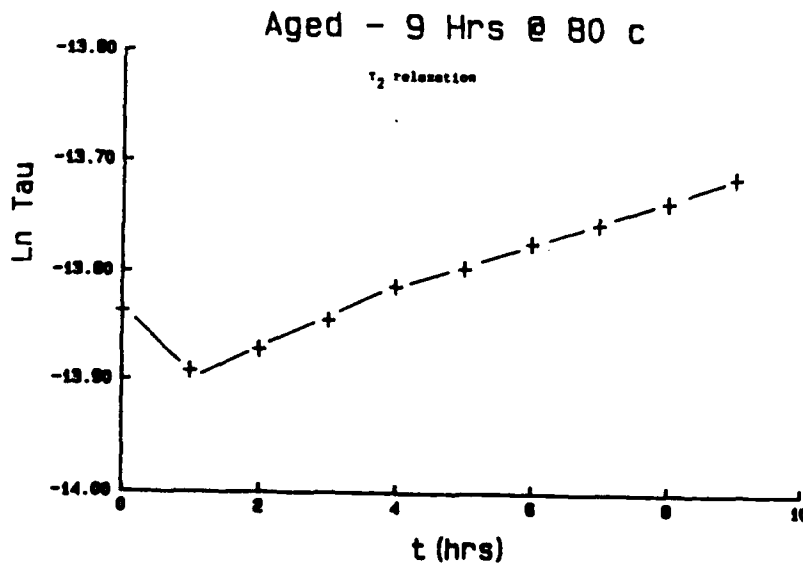


FIGURE 8. Relaxation Time, τ_2 , versus Aging Time at 80 °C.

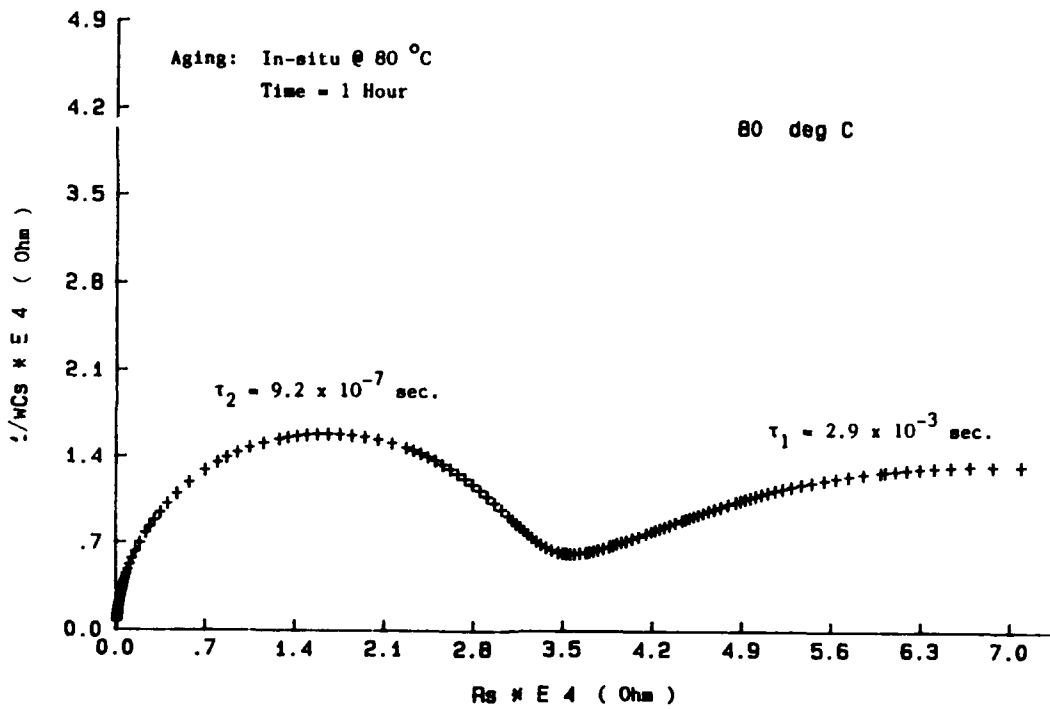


FIGURE 9. Complex Impedance Plot For Standard Paste after Aging at 80 °C For 1 Hour.

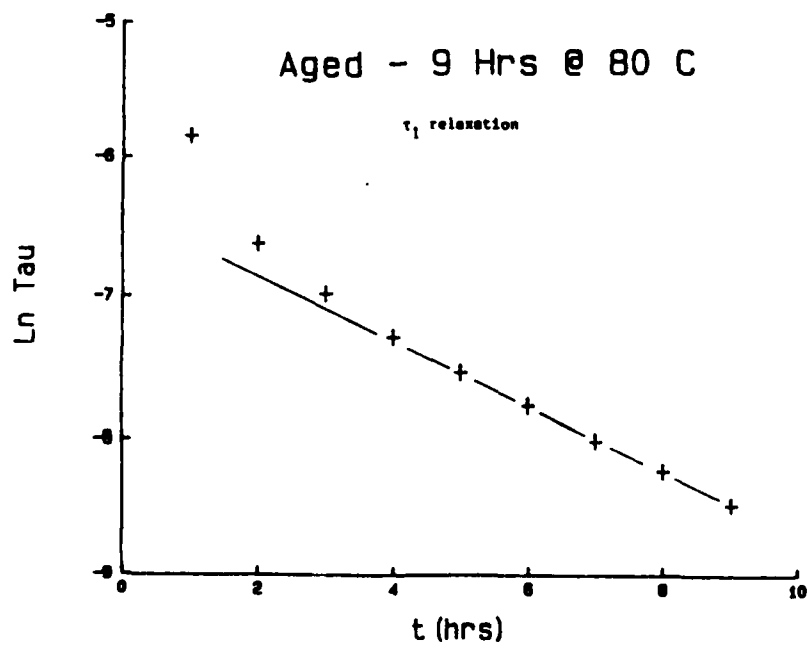


FIGURE 10. Relaxation Time, τ_1 , versus Aging Time at 80 °C.

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The Metallurgy and Mechanisms of Failure
in
Surface Mount Solder Joints

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Abstract

The difference in processing procedures used in through hole and surface mount soldering results in differences in the metallurgy of the solder joints. Lower temperatures, cooling rates and exotic base metal systems go to make up these differences. This paper describes the metallurgy of solder joints made to leadless and leaded chip carriers with several different solders. These are compared to standard through hole wave soldered joints. The effect on solder joint morphology by the soldering process is included. Described are laser, vapor phase, and infrared process influences. Also described are the changes in the solder joint morphology as a result of thermal cycling of the joints.

As a result of thermal cycling all solder joints wear out; the question is 'How soon?'. The life of the solder joint, especially in surface mount, is related to a variety of mismatches in coefficients of expansion. These result in planes of strains whose location is related to the mismatches. Therefore fracture will occur in various locations in the solder joints depending on the degree and direction of the controlling plane of strain. These fractures can be classified as either threatening or non-threatening with respect to the functional life of the solder joint. The second part of this paper describes the metallurgy and mechanics involved with the failure of surface mount solder joints during thermal cycling. The development of planes of maximum strain and the influence of various solder joint geometries and defects are discussed. Their relationship to a failure mode are explained.

Introduction

Over the years the role of the solder joint in electronics has changed dramatically. When point to point wiring was king, a mechanical connection was made secure first and then the solder joint was made to ensure the reliability of the electrical connection. This philosophy was carried over to the first printed wiring designs (clinch joints). Straight through joints were only used in commercial electronics. DIP's were clinched on at least two pins to 'make them secure'. Slowly the solder joints role has been changing, with the advent of true surface mount designs, from a metallurgically based electrical connection to the dual role of mechanical and electrical connection. What this means is that the solder joint not only has to reliably maintain an electrical path but it also had to keep the component from physically falling off the board. This change requires that our engineering designs and design philosophy has also has to undergo some dramatic changes.

It is the purpose of this paper to discuss the makeup, reliability and failure characteristics of solder joints which are required to fulfill the dual mechanical and electrical roles. This will include the metallurgy and morphology of such joints, failure modes, failure mechanisms and what one can do to enhance the life of such solder joints. Also discussed is the impact of soldering processes and solderability defects have on the life of solder joints.

Solder Joint Metallurgy

Solders bond or wet to the metals which they are joining by metallurgical reaction with the base metal. This is a totally different mechanism than why water wets a surface. This bonding mechanism results in the formation of an intermetallic compound layer between the solder and the base metal. For example, if a molten Sn based solder is placed in contact with clean Cu, the metallurgical reaction between the Sn and the Cu will result in the formation of a layer of Cu_6Sn_5 . This intermetallic layer is the glue that holds the solder joint together. In normal soldering, the thickness of this intermetallic layer is on the order of 0.5 to 1 micrometer. It will rarely grow thicker than this in a liquid-solid reaction. However solid state metallurgical reactions can progress after solidification of the solder joint: especially at elevated temperatures. In the Sn-Cu system a second intermetallic compound can form between the Cu and the Cu_6Sn_5 layer. This is Cu_3Sn which has quite different properties than the Cu_6Sn_5 compound.

Intermetallic compounds have much different physical and mechanical properties than the metals which make them up. Typical intermetallics are very brittle and have poor electrical conductivity. In addition if they are exposed to air they will passivate (oxidize) very readily. Chemically, these passivated intermetallic surfaces are very stable and cannot be reduced by the typical fluxes used in electronic soldering. Therefore it is usually advisable to keep the layers as thin as possible; generally between 1 and 2 micrometers and protected from the atmosphere by a layer of solder. The reaction rates involved in intermetallic formation during solder wetting vary considerably in the different metal systems. For example the Sn-Ni intermetallic formation rate is slower than the Sn-Cu formation rate while the Sn-Au and Sn-Ag formation rates are orders of magnitude faster. Stability of the different intermetallic compounds also varies between the metal systems.

Intermetallic compounds can be found in two places in a solder joint. Preferably they are in thin a continuous layer between the solder filler metal and the base metals. Sometimes intermetallic compounds can be found as particles, needles or other such form within the solder matrix of the joint. This is not mechanically or metallurgically desirable and process conditions leading to such intermetallic inclusions should be avoided.

In surface mount technology (SMT) the majority of interconnections are made between active or passive components, leaded or leadless, and printed wiring boards. The PWB metallization is typically copper which has been solder coated. Therefore the bond will actually be made between the solder and the copper. Leaded chip components will typically have kovar or alloy 42 leads. Therefore the bond will be one between the solder and a nickel containing alloy with the main intermetallics that are formed being Sn-Ni. In leadless parts today's technology dictates that all silver metallization be coated with a barrier layer of nickel. Again the solder bond will be between the Sn in the solder and the nickel barrier forming Sn-Ni intermetallics.

Due to intermetallic compound formation both the Sn from the solder and Cu or Ni from the base metal will be used to form the intermetallics. This process can literally use up one of the two metals making up the intermetallic compound. If the base metal becomes used up then the process is commonly known as leaching. On a chip component this can lead to exposed ceramic or a underlying, non-solderable refractory metallization. If a solder coating is used up this can lead to exposure of the intermetallic to the atmosphere and non-solderability of the surface. This is the cause of 'weak knees' in printed wiring boards.

The microstructure of a solder in a solder joint is controlled by the cooling rate and its composition. Subsequent thermal exposure can and does alter the 'as cooled' microstructure. Also different solders develop different microstructures based on composition. In eutectic or near eutectic solders, fast cooling will result in a 'fine grained' structure. Slow cooling will result in a 'coarse grained' structure. Most sources agree that the 'fine grained' structure is more desirable from a strength and fatigue resistance standpoint.

The microstructure in solder alloys is becoming more important as the applications become more severe. A basic principle in physical metallurgy is that the properties of an alloy are dependent on the microstructure and solders are no exception.

Sn/Pb solders are binary alloys with a strong two phased microstructure. Figure 1 shows a normal eutectic structure in fairly rapidly cooled 63/37 Sn/Pb solder. Cooling the solder more slowly results in a coarser structure (Figure 2). Thermal cycling the structure shown in Figure 1 results in solid state diffusion which also coarsens the structure (Figure 3). This is important in fatigue resistance. Due to the mechanism of fatigue (Reference 1) the finer the structure that you start with, the longer will be the life (Reference 2). In terms of process, rapid cooling such as obtained in wave or infrared soldering should be better than the slow cooling often seen in vapor phase soldering, considering that all other parameters are kept equal.

Departure from the eutectic composition results in increased proeutectic phases. Figure 4 is the microstructure found in 50/50 Sn/Pb solder. These will, if on the Pb side of the eutectic, increase the ductility and lower the creep resistance of the solder. If on the Sn side of the eutectic the creep resistance and hardness will increase slightly. The jury is still out on the effect of off-eutectic microstructures on the fatigue resistance of solders (References 1, 3 & 4).

In contrast, 96/4 Sn/Ag and 95/5 Sn/Sb are mainly single phase solders which contain lattice pinning intermetallic compound particles. Being basically single phased the microstructure does not significantly change during thermal cycling and thermal exposure. For this reason they are stronger, lower in ductility and more creep resistant. In some cases they also have improved fatigue properties since most fatigue (plastic strain) damage occurs at phase boundaries (Reference 1). Figure 5 shows the microstructure of an as cast 96/4 Sn/Ag solder.

Effect of Stress and Strain on Solder Joints

Stress and strain on solder joints produce significant changes in the morphology of the solder. These changes can be either localized or general in nature. Most stresses are developed from differential coefficients of expansion between components and substrates. Most damage and changes to the solder microstructure are related to the strain developed by the applied stress.

The most common general effect is caused by elevated temperatures, either from high ambient temperatures or thermal cycling. The effect is a coarsening of the microstructure (Reference 5). Thermal cycling will also result in the same coarsening. The higher the temperature in the cycling the greater will be the effect. In other words, cycling from -55 to +125°C will cause greater coarsening than cycling between -55 and +85°C. Coarsening of the microstructure is related to the life in terms of the number of cycles to failure (Reference 6).

Figure 6 shows a 63/37 Sn/Pb solder joint made by Laser soldering. Figure 7 shows a similar joint made by a vapor phase process. Figures 8 and 9 show these joints after 1000 thermal cycles (-55 to +125°C). Notice that while the starting microstructures are quite different that after the 1000 cycles there is little difference. Cycling at a lower maximum temperature would result in the laser solder joint having a somewhat finer structure after the 1000 cycles. This would indicate that the life of the laser soldered joint versus the vapor phase soldered joint is highly dependent of the thermal environment.

Strain on a solder joint, whether it be through hole or surface mount, causes a similar coarsening of the microstructure but through a different mechanism and on a localized scale. Figure 10 shows the coarsening in a through hole solder joint. Figure 11 shows a similar coarsening in a solder joint to a leadless chip carrier. This coarsening occurs along the plane of maximum strain in the solder joint. The cause of this type of coarsening is a function of work hardening and recrystallization (Reference 7). It has been found that low strain and a higher number of cycles will result in significant coarsening where high strain and a lower number of cycles will result in less coarsening. Also the size of the coarsened area is representative of the stress causing the strain. The spacing between the lead and plated through hole wall or the bottom of the LCC and the substrate has a significant effect on the intensity of the strain along the plane of maximum strain. This usually occurs closest to the more highly stressed member; usually the component lead or termination. The closer the spacing, the greater will be the stress intensity and consequently the strain. Therefore areas of high strain tend to be more localized than areas of lower strain.

The source of strain in a solder joint comes from one of two sources. The least common, in today's electronic hardware, is from external stress such as 'G' forces. The most common, especially in SMT designs, is from a mismatch of coefficients of thermal expansion (CTE). The following table gives some typical values for the CTE of materials involved in solder joint technology. Values greater than 2 to 1 can cause excessive strain in a solder joint.

Solder	- 23 ppm
Kovar	- 6 ppm
FR4	- 30 - 50 ppm
Ceramic	- 6 - 7 ppm
Kevlar/Epoxy	- 9 ppm
Copper	- 19 ppm

From this it can be seen that solder on copper is less than 2 to 1 but solder on ceramic or kovar is much greater than 2 to 1. Fatigue is a plastic strain dependent mechanism. Therefore one can expect early cracking in a solder to ceramic joint if the delta 'T' is high and the length of the mismatch is long. This type of combination causes a high percent strain to develop. Figure 12 shows a typical fatigue plot which relates amount of strain to number of cycles to failure (in this case until a 90% load drop was achieved).

In a surface mount situation, such as a leadless ceramic chip carrier mounted to an organic substrate, a certain amount of strain can develop due the CTE mismatch as described above. This can be intensified by having unequal solder joints opposite each other (**Figure 13**). Such a situation is not uncommon and affects the neutral stress axis. Normally one would think than the neutral axis would be centered in the chip carrier. Unequal sized joints, joint thickness or tilt of the LCC will cause the neutral axis to shift and intensify the stress (and strain) on the side with the smaller joint or thinner joint. This effect is even seen in fatigued joints in plated through hole technology (**Figure 14**).

Solder Joint Failure Modes

Solder joints can fail in several modes but the most common is fatigue in today's electronic hardware. Other modes that are seen are overload and creep. The fatigue failures are usually due to a mismatch in coefficients of expansion and therefore are thermally induced failures. Overload failures are usually in shear and are due to some excessive applied load such as mechanical shock. Creep failures most often occur in such things as connector systems where there are significant torque or dead weight load conditions that remain applied over an extended period of time. The time to failure is related to both stress intensity and temperature.

Overload failures are rare in electronic solder joints. If they occur they are most often related to either high 'G' forces in the operating or test environment or to mishandling. The overload failure is usually by ductile microvoid coalescence either in tension or shear.

Creep failures occur more often in electronic solder joints but not so often that they can be easily recognized from experience. The mechanism of creep follows normal theory but can occur at very low stresses (100 PSI) if operated at high enough temperatures (125 to 150°C). A classic case often involves a surface mount gull wing lead that was forced down and held in place while the solder froze (**Reference 8**). The spring force created in the lead by this action is enough to result in a solder joint creep failure as there is little or no relaxation in the lead. In most cases this is a 'time bomb' type of failure mode as the stresses are low enough to delay the failure for hundreds or thousands of hours after the solder joint was made.

The most common failure mechanism as stated previously is fatigue. The next section will discuss the mechanisms in detail. Fatigue is a property of its own and when testing for susceptibility for fatigue it is not possible to use overload tests or even creep tests in order to determine this susceptibility.

Fatigue Mechanisms in Detail

Fatigue is a mechanism which is plastic strain dependent. This strain causes work hardening and recrystallization in the solder joint. It matters not what the source as long as plastic deformation is present. The rate of strain becomes very important. **Figure 15** show a plot of rates of strain versus number of cycles to failure. The higher the rate the greater the number of cycles to failure. The reason for this is that low rates of strain allow creep to play a roll while maximizing plastic strain. Therefore the creep properties are an important part of the fatigue equation. Creep manifests itself by controlling the amount of stress relaxation that will take place in a given time and at a given

temperature. The greater the stress relaxation through creep in the solder the greater will be the mechanical damage to the solder structure. Conversely, high rates of strain have a significant elastic strain component and a minimum effect of creep. The number of cycles to failure can increase dramatically under high strain rate conditions. When testing for fatigue properties this must be taken into account. The mode of failure can change with a change of strain rates.

Fatigue failures are very sensitive to microstructure. The actual crack may be initiated at a grain boundary and will typically follow the phase boundaries (in a eutectic or near eutectic solder). **Figure 16** shows a typical crack path. This following of phase boundaries is due to slip at the interface between the phases with a resultant dislocation stackup. The disproportionate hardness of the phases enhances the slip at the phase interfaces. Its a little like bowling balls (high Sn phase) rolling around in silly putty (high Pb phase).

In real solder joints two kinds of cracks are likely to develop. These often can be classified as threatening and non-threatening. Most threatening cracks will develop rapidly where the CTE mismatch is high. These are the cracks that will continue to propagate and cause ultimate failure. This type of crack may also be known as primary (first order) crack and is associated with a plane of maximum strain. Non-threatening cracks usually develop where the CTE mismatch is low. As the crack progresses it will also act as somewhat of a strain relief and the crack may even stop. These are also known as secondary (second order) cracks. A typical example of a non-threatening type crack is a toe crack (**Figure 17**) in a leadless solder joint.

Voids in solder joints actually are two faced in terms of cracks. Voids in general are stress risers. You will often notice that fatigue cracks are attracted to voids and nearly always pass through them. This indicates that a void is a definite stress riser as cracks will always seek out the plane of maximum stress. A large void will however temporarily relieve the stress once a crack enters it. Studies have shown the once a crack enters a large void a number of small cracks will form on the opposite side of the void (**Figure 18**). If the void is in the plane of maximum strain one of these cracks will assume a primary roll and the crack propagation will continue as before. It is thought that the crack stopping power of a void only lasts for a cycle or two if the strain is high. Small voids will pass cracks through them as if they didn't even exist. The only effect of small voids is the stress riser aspect in which cracks are attracted to them. Therefore the life of a solder joint as related to voids may be by how much they reduce the length of the solder joint in the crack path. Usually this is a minimum amount and probably accounts for the fact that there is no hard data that says that voids significantly reduce solder joint life in a fatigue situation. The effect is probably in the range of experimental error and would never be evaluable in real solder joints. The case for extensive flat voids such as shown in **Figure 19** is different. These so significantly reduce the soldered length that they have a strong negative effect on the cycles to failure.

Fatigue life is strongly affected by cycle rate as mentioned previously. Roger Wild (**Reference 9**) showed in the middle 70's the effect of strain rate on life. Typically the lower the strain rate the shorter the life in number of cycles to failure. Most of our electronic equipment operates in the worst case with respect to strain rate. This is one cycle per hour or greater. The other factor associated with strain rate is the impact on such things as failure initiation sites. For example, high rate mechanical cycling may initiate cracks at the heel (**Figure 20**) while the normal thermal cycling rate of 1 CPH will initiate the cracks at the corner (**Figure 21**) in a castellated leadless chip carrier configuration.

Component size also plays a roll in the fatigue failure mechanism. This is a function of CTE and strain relief. In the case of a ceramic leadless chip carrier (LCC) the larger the chip carrier the greater the potential for solder joint failure, all other things being equal. The greater the CTE mismatch between the chip carrier and the substrate the greater will be the effect. In the case of leadless chip resistors and capacitors the same rule holds true. The mechanical strength of the chip component also comes into play here.

Chip capacitors and some chip resistors are made from low strength ceramics. The most common are the ceramics based on barium titanate. These ceramics have no where near the mechanical strength of such materials as alumina and beryllia. The designer may spend much of his time making the strongest and most strain resistant solder joint possible only to have the component crack in the application. The solution to the problem is to either use leaded parts or make a compromise between strain relief in the solder joint, solder joint strength and component strength. Remember that solder has no endurance limit and either it or the component will fail. The idea is to design for a specific life and not forever.

Solder Joint Life Enhancement

There are a number of ways to enhance the life of a surface mount solder joint or for the matter of fact any solder joint. These are:

- * Reduce CTE Mismatches
- * Strain Reduction by Solder Joint Geometry
- * Leaded Components (Strain Reduction)
- * Solder Alloy Selection

These are listed, generally, in overall effectiveness and take into account producibility plus thermal considerations.

Reduction of CTE mismatches is most often approached at the board to package level. The use of kevlar[™] or quartz fabric in the laminate material has been one approach. A second common approach is to incorporate a stabilizing layer such as copper-invar-copper (CIC) in the substrate sandwich. New approaches are being tried on almost a daily basis. This type of CTE mismatch reduction works well on reduction of first order failure mechanisms but does not consider the second order effects. As the life of the solder joint increasingly becomes enhanced the more the second order effects limit further life enhancement.

Second order fatigue failures most often occur due to solder package/lead mismatches. Solutions include conversion from leadless to leaded package styles, a change from ceramic to plastic packages, changing leads from nickel-iron alloy to copper or a combination of these. All will provide a closer match between the solder and the soldered material.

Strain reduction by solder joint geometry is most effective in leadless design. Where the package/board CTE is matched then a design such as shown in **Figure 22** is most effective. There is also some evidence that a non-castellated package will have better life than a castellated on due to the elimination of the second order cracking along the castellation. Where the package/board CTE is not matched then a solder joint design such as shown in **Figure 23** will have the best life. This is known as a bulbous joint. The theory behind the use of this joint design

is that it will provide a longer crack path length in the lower stress portion of the joint. Therefore there will be a significant increase in the number of cycles to failure. The 'H' dimension is also important in life enhancement. In nearly all cases it is best to have an 'H' dimension of greater than 5 mils. For maximum life the PWB pad width and length should match that of the lead or package termination. Normally the lead or package termination has always been smaller than the pwb pad. This design increases the stress concentration near the lead and at the heel.

In terms of strain reduction one of the most effective, as already mentioned, is a change from a leadless design to a leaded style. This has some thermal drawbacks but will increase life. The lead size and shape also has a major impact. Small, flexible, low modulus material leads are best.

The last item is a change in solder alloy. The latest data from two Air Force programs indicates that use of a 50/50 Sn/Pb alloy instead of a near eutectic alloy will increase life. The drawbacks are the availability of materials and the producibility issues with present production equipment.

Summary

The metallurgy of a surface mount solder joint is basically no different from any solder joint. The main differences are in the formation of the joint and the effect of temperature on the microstructure. Surface mount solder joints are a planar type joint with poor solder flow dynamics. This, added to the lower soldering temperatures often used and the incorporation of solder paste into the process, makes sound joints more difficult to achieve and increases the potential for void formation. The microstructure is strongly affected by cooling rate from the melt and post freezing temperature exposure. Processes such as vapor phase soldering tend to result in coarse microstructures.

There are three main failure modes that surface mount solder joints may be susceptible. The most common is fatigue of the solder joint. Creep and overload failures may also occur. Creep is found mostly in solder joints to leaded devices and in connector systems where there is a possibility of having a constant load applied to the joint. Overload is less common and can often be traced to mishandling.

In surface mount technology fatigue failures of the solder joints are related to a number of factors. Solder being the material it is, any cyclic strain on the solder joints will ultimately result in failure. The question is when and will the product useful life be less than the number of cycles to failure.

There are a number of measures that can be taken to enhance the life of surface mount solder joints. First CTE mismatches can be minimized. If they cannot be minimized then strain relief designs can be utilised. Secondly the geometry and the thickness of the solder joint can be tailored to the application. Lastly a change in solder alloys may provide some enhancement. In most cases to achieve significant enhancement of life a combination of measures should be taken.

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References

- 1- DeVore, John A., "Fatigue Resistance of Solders", National Electronic Packaging & Production Conference, Anaheim CA, February 1982.
- 2- Wild, R.N., "Some Factors Affecting Leadless Chip Carrier Solder Joint Fatigue Life", 28th National SAMPE Symposium, Anaheim, CA, April 12-14, 1983.
- 3- Jarboe, D.M., "Thermal Fatigue of Solder Alloys", Report BDX-613-2341, Bendix Corp., Kansas City, February 1980.
- 4- Pearson, R. and Burke, M., "Solder Alloy Development For Electronic Chip Carriers", Report AFWAL-TR-88-4215, Air Force Wright Aeronautical Laboratories, WPAFB, Ohio, November 1988.
- 5- Zakraysek, L., DeVore, J., & Kelsey, D., "Microstructures of Solders", 9th Annual Soldering Technology Seminar, Naval Weapons Center, China Lake, CA, February 1985.
- 6- Wild, R.N., "Some Factors Affecting Leadless Chip Carrier Solder Joint Fatigue Life II", 12th Annual Electronics Manufacturing Seminar, Naval Weapons Center, China Lake, CA, February 1988.
- 7- Wild, R.N., "Some Fatigue Properties of Solders and Solder Joints", Internecon, Brighton, England, October 1975.
- 8- Wild, R.N., "Page Flat Pack Solder Joint Failures", IBM Report 77PA0021, IBM Corp, Owego, N.Y., April 1977.
- 9- Wild, R.N., "Fatigue Properties of Solder Joints", Report 72Z000404, IBM Corp., Owego, N.Y., April 1972.

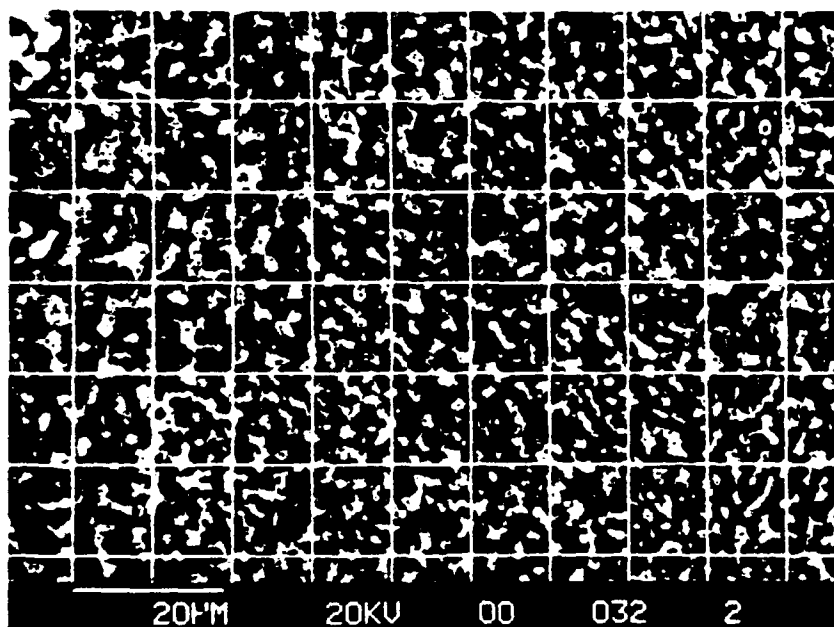


Figure 1

Rapidly Cooled 63/37 Sn/Pb

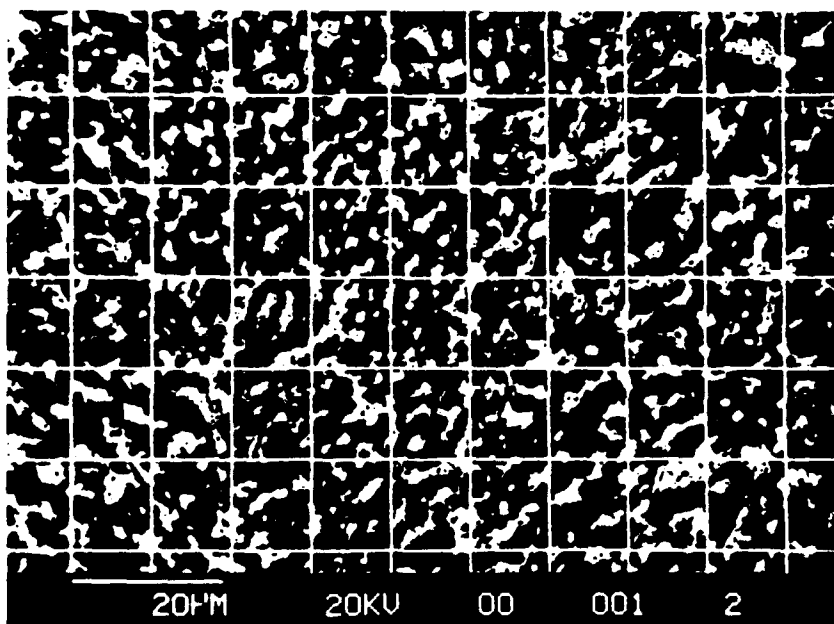


Figure 2

Slowly Cooled 63/37 Sn/Pb

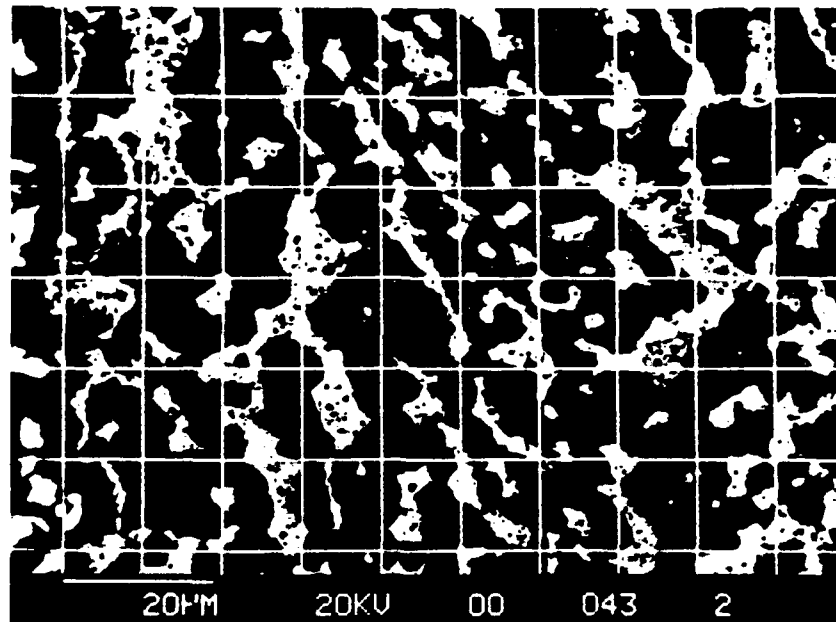


Figure 3

Thermally Cycled Rapidly Cooled 63/37 Sn/Pb Microstructure

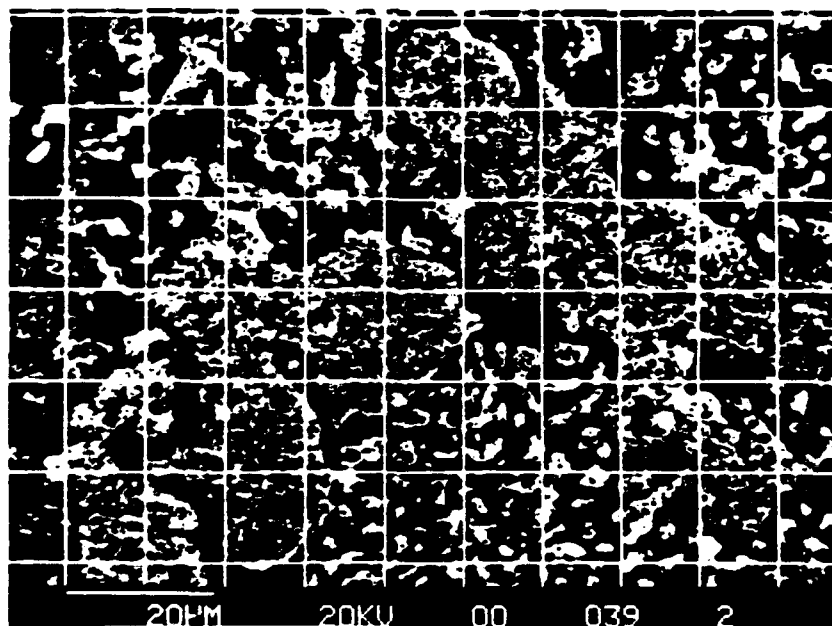


Figure 4

Microstructure of As-Cooled 50/50 Sn/Pb

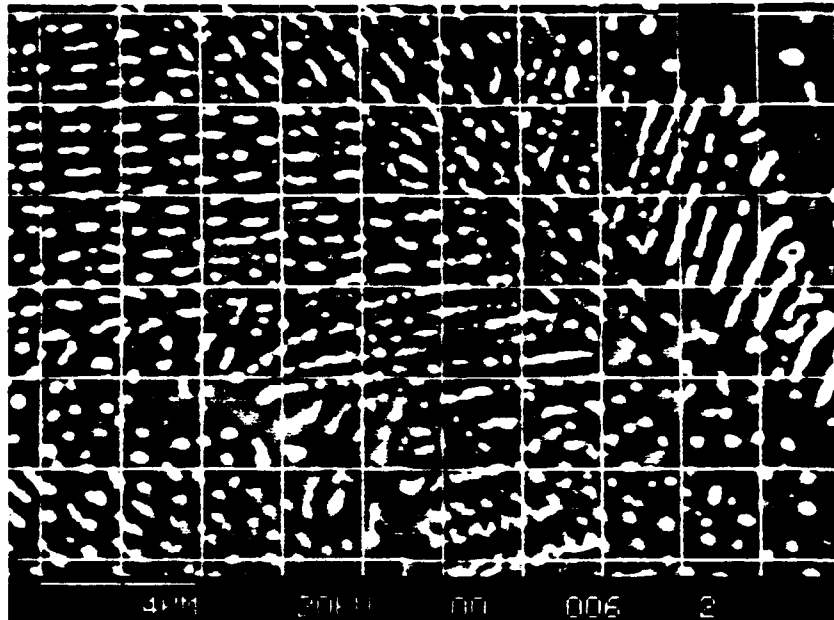


Figure 5
Microstructure of As-Cast 96/4 Sn/Ag

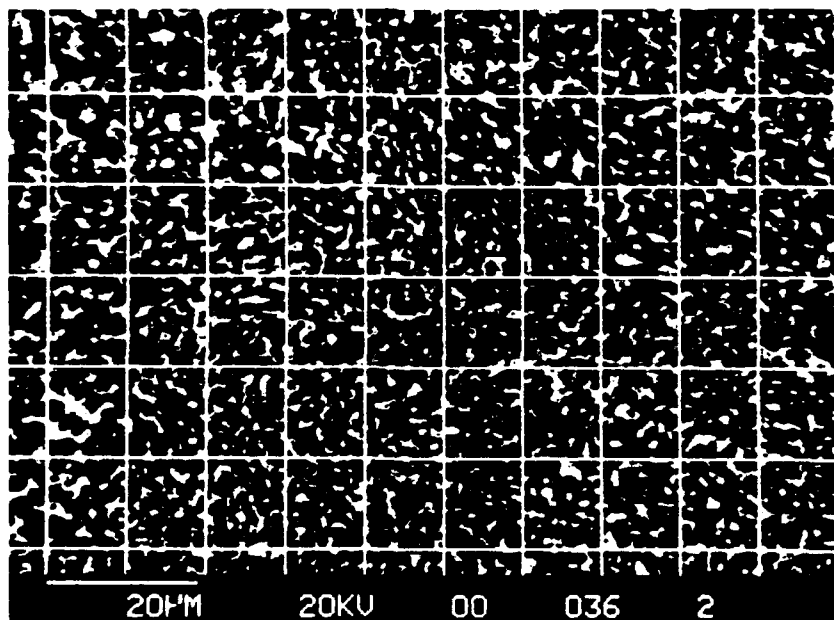


Figure 6
Microstructure of Laser Made 63/37 Sn/Pb Solder Joint

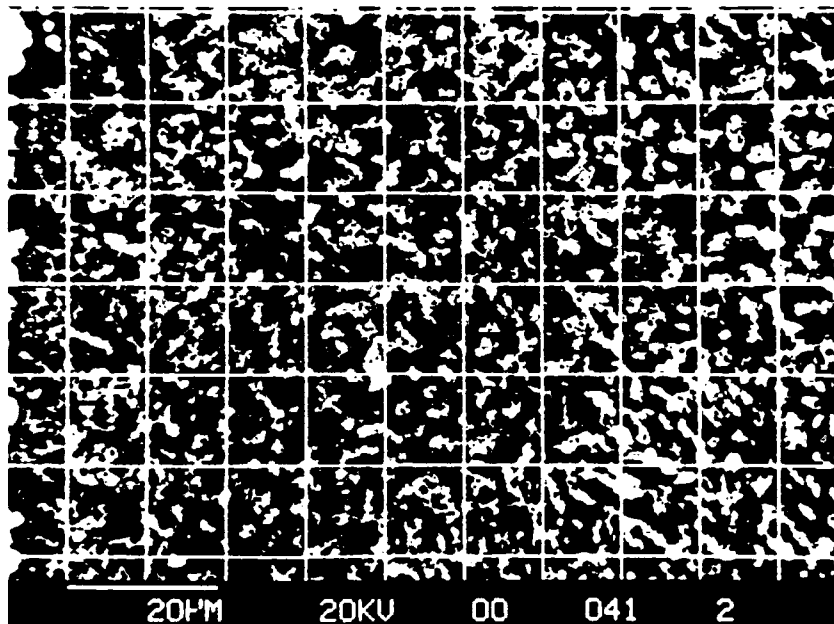


Figure 7
Microstructure of Vapor Phase Made 63/37 Sn/Pb Solder Joint

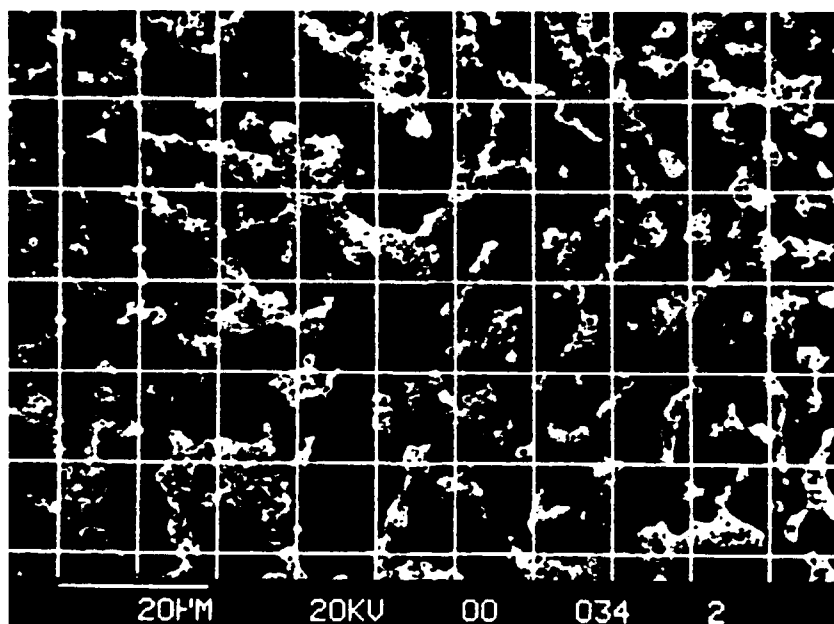


Figure 8
Thermal Cycled Vapor Phase Made 63/37 Sn/Pb Solder Joint

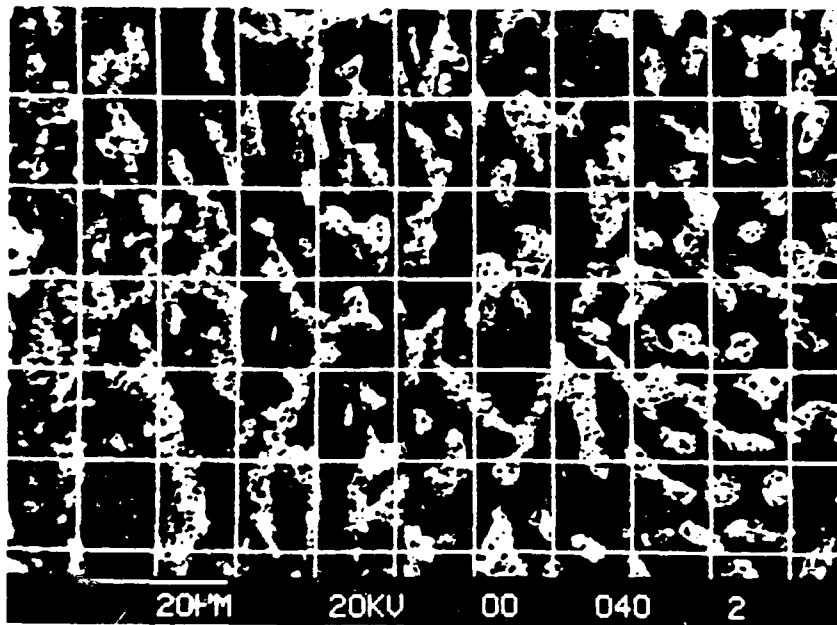


Figure 9
Thermal Cycled Vapor Phase Made 63/37 Sn/Pb Solder Joint

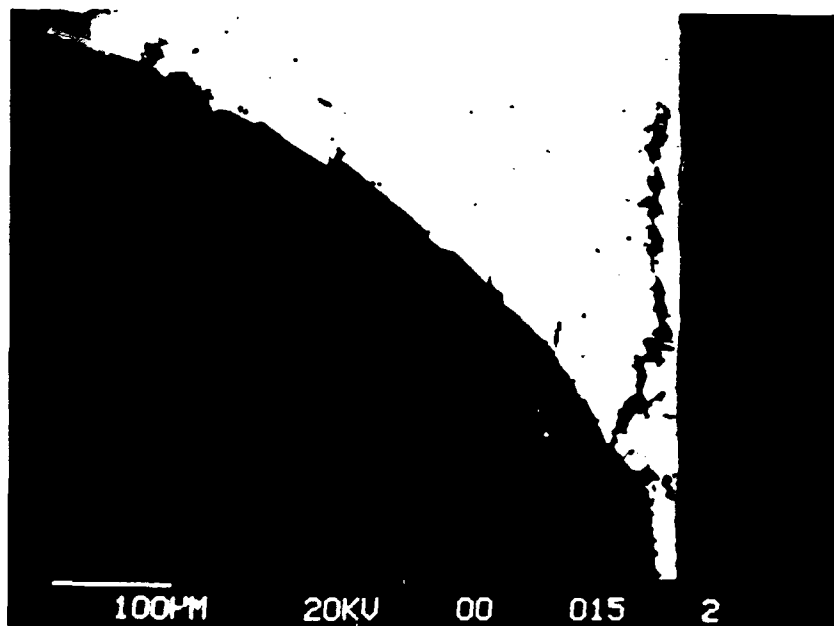


Figure 10
Microstructure Coarsening - Through Hole Joint

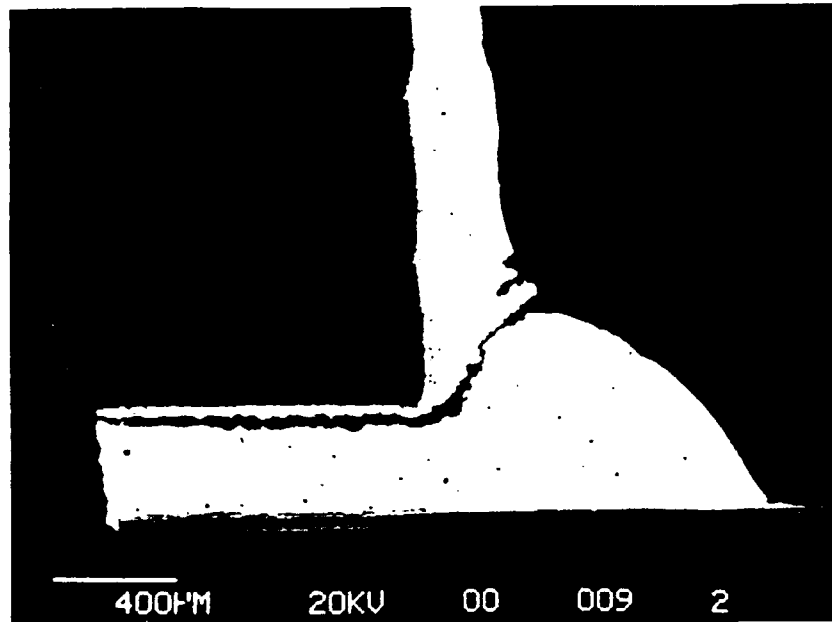


Figure 11
Stress Coarsened Microstructure - LCC Solder Joint

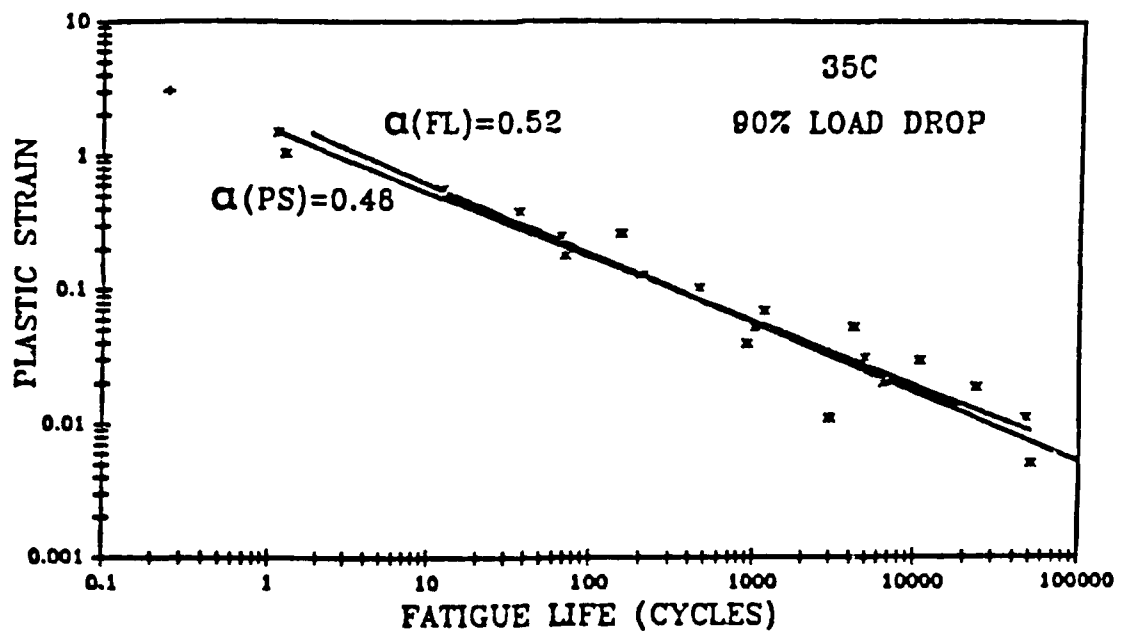


Figure 12
Amount of Strain vs Number of Cycles to Failure
Source: H. Solomon - GE Co.

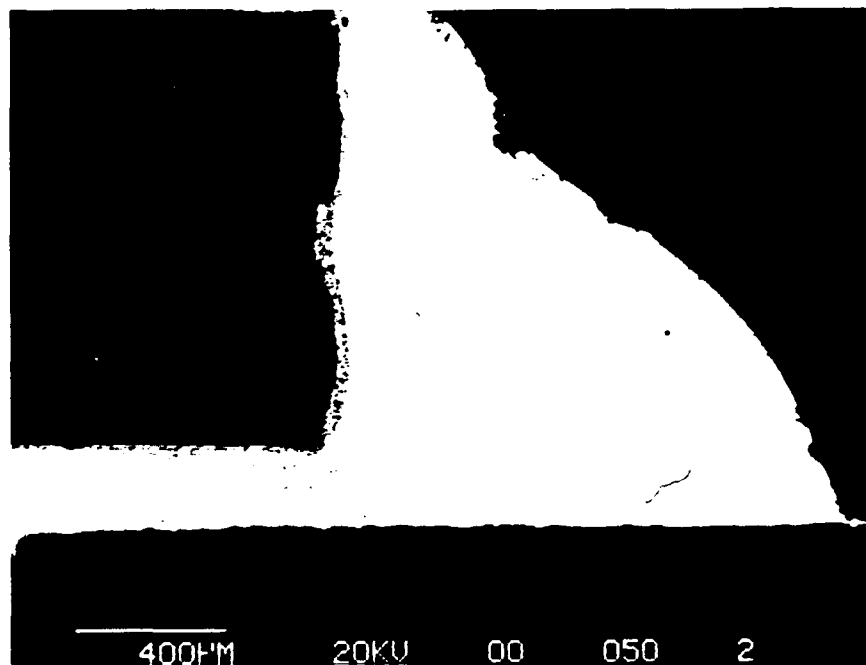


Figure 13a
LCC - Unequal Solder Joints on Opposite Sides

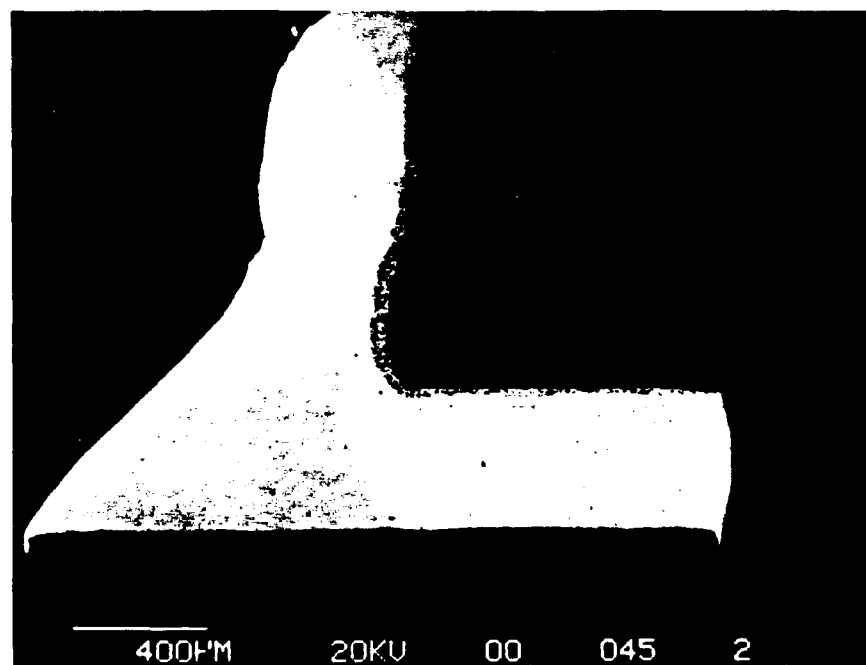


Figure 13b
LCC - Unequal Solder Joints on Opposite Sides

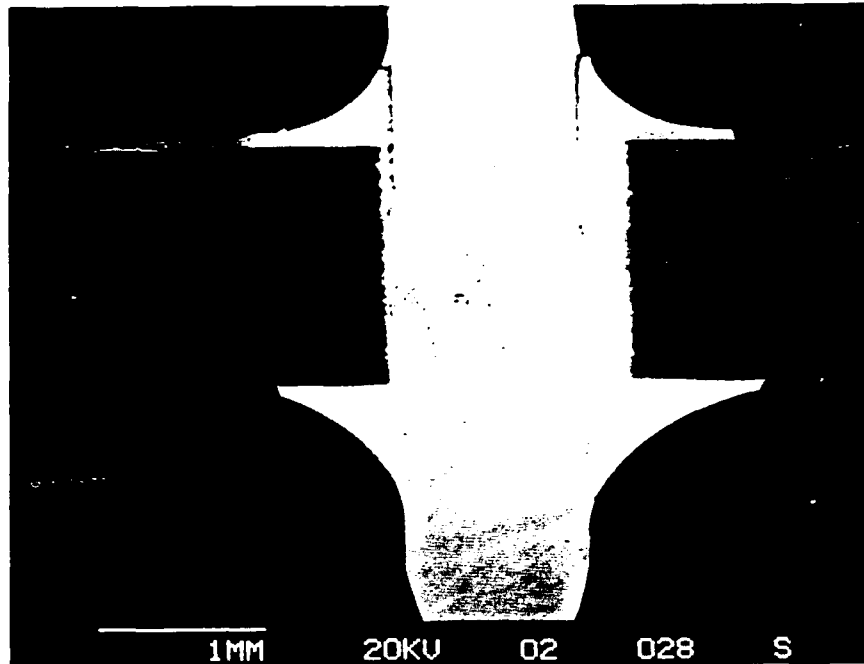


Figure 14
PTH Solder Joint - Unequal Spacing

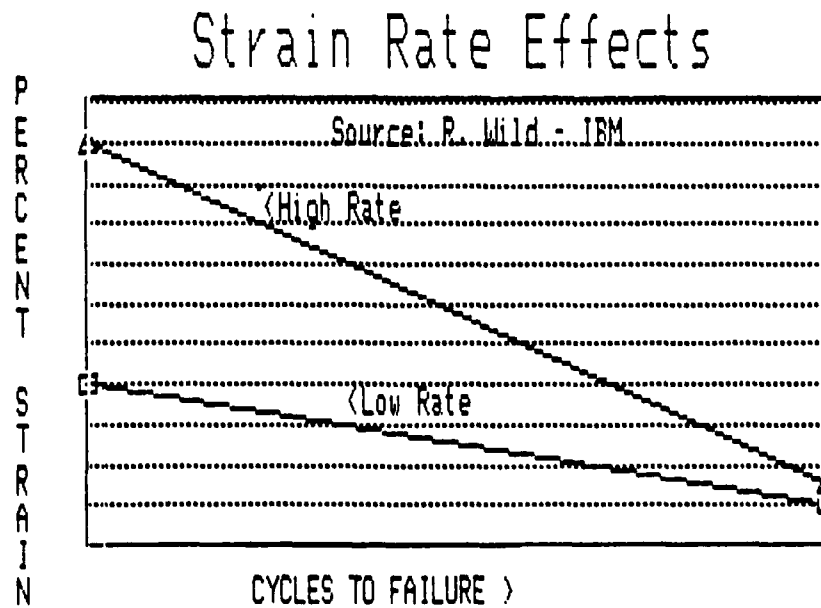


Figure 15
Rate of Strain vs Number of Cycles to Failure

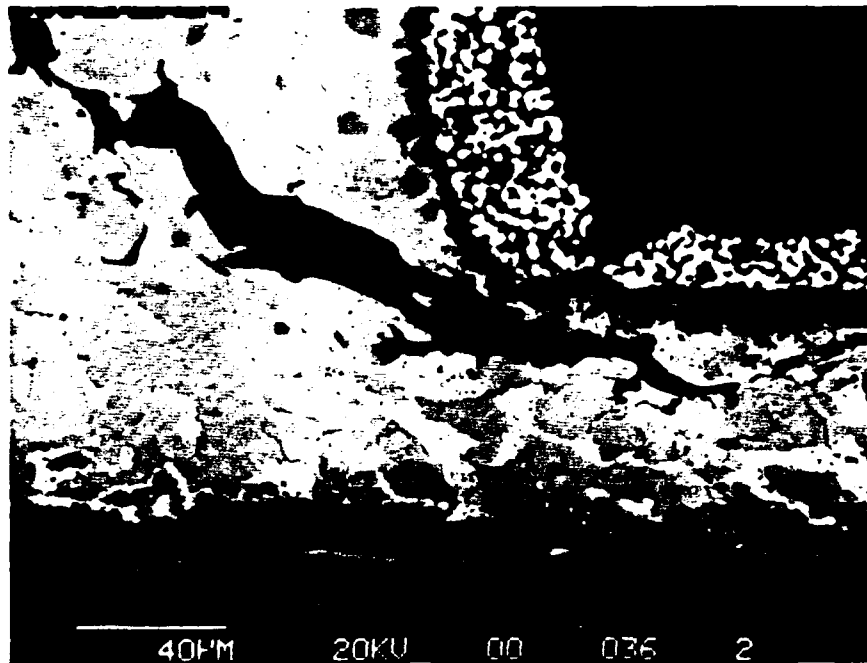


Figure 16
Typical Fatigue Crack Path Through Microstructure

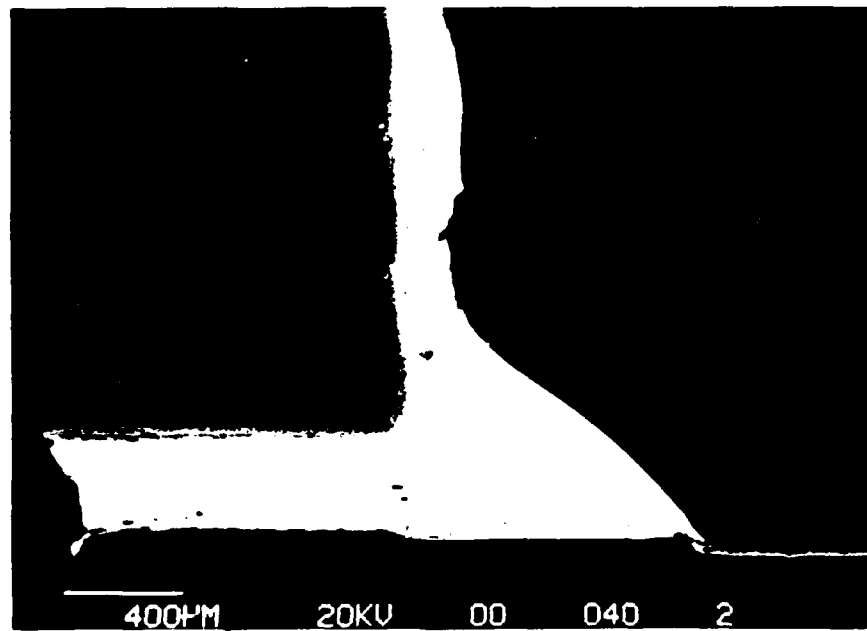


Figure 17
Non-Treatening Toe Crack in LCC Solder Joint

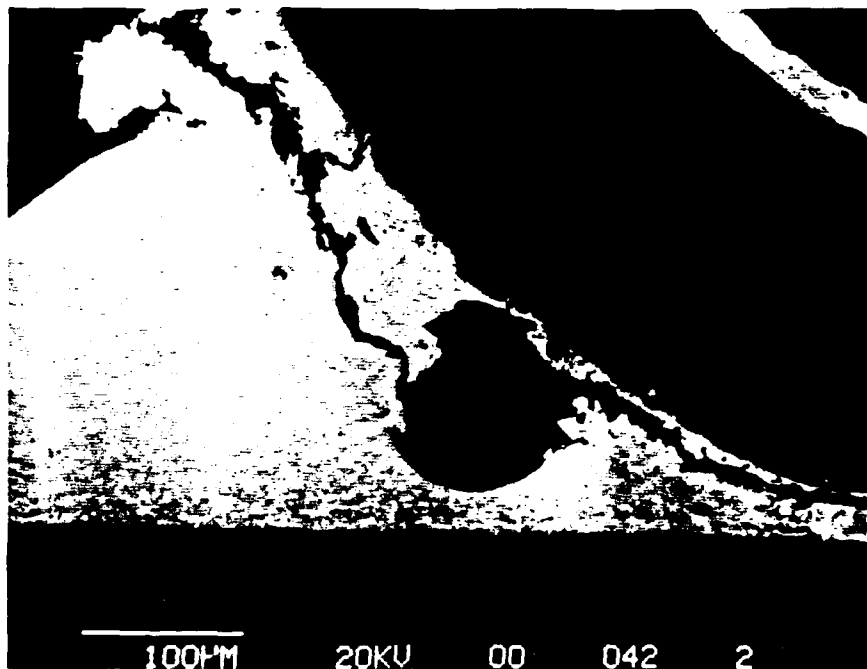


Figure 18
Fatigue Cracking Through a Spherical Void

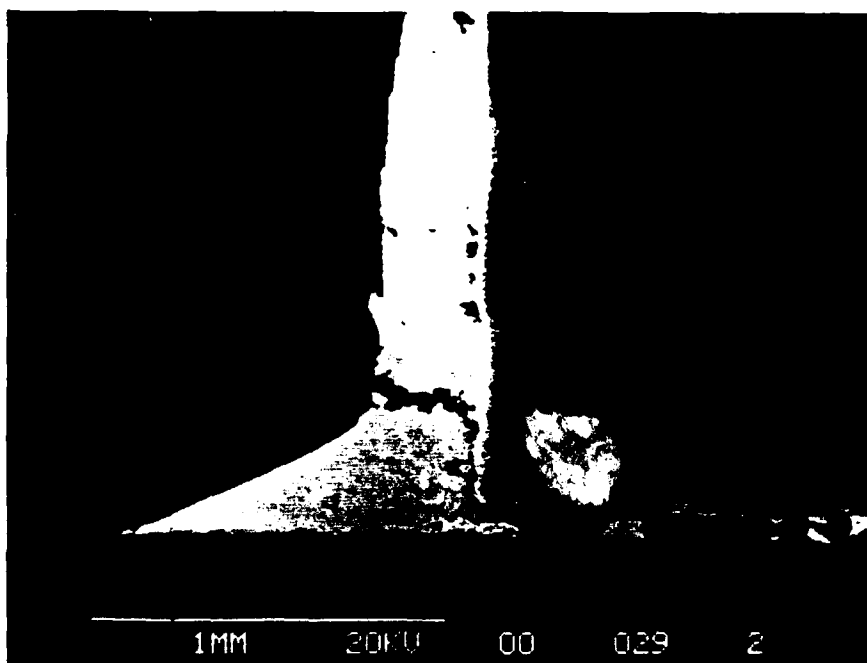


Figure 19
Fatigue Cracking Through Large Flat Voids

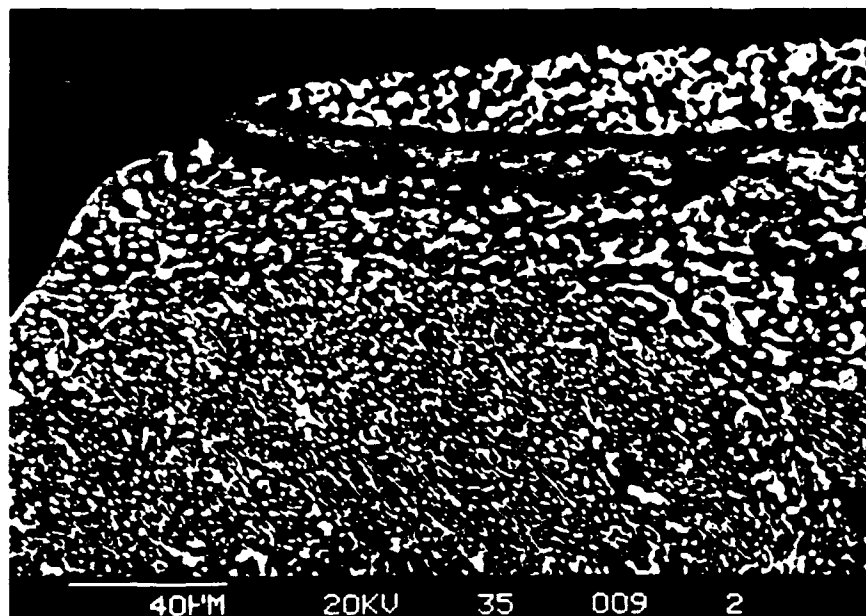


Figure 20
High Strain Rate, Heel Initiated Crack

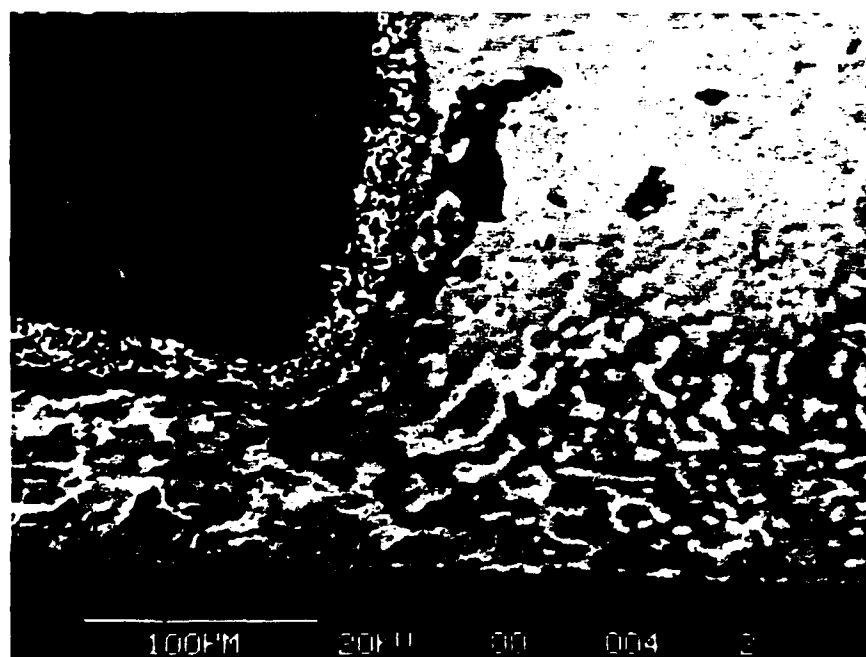


Figure 21
Low Strain Rate, Corner Initiated Crack

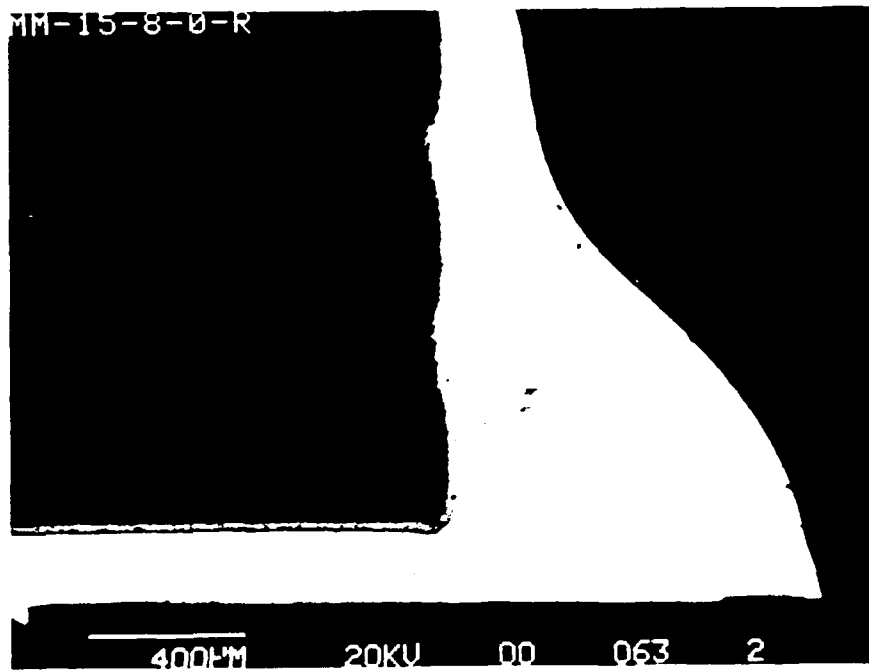


Figure 22
Matched Package/Board CTE Solder Joint Design

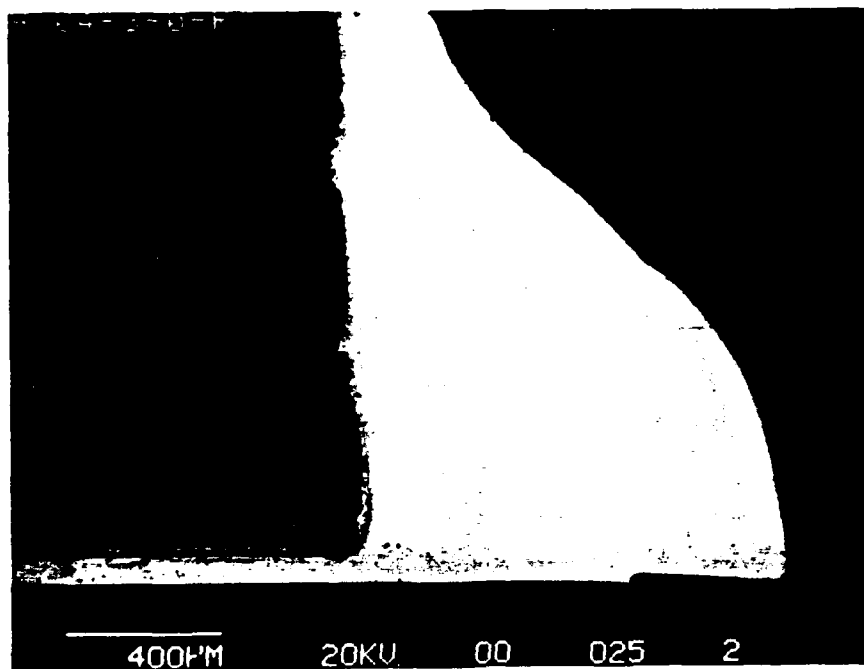


Figure 23
Unmatched Package/Board CTE Solder Joint Design

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He received his BS degree in Metallurgical Engineering in 1959, was elected to the national honorary fraternity Alpha Sigma Mu, and is an active member of ASM. His most recent work in soldering technology has been in the refinement of wetting balance solderability testing; he also has extensive experience in solder joint failure mechanisms and the fatigue properties of solders. He is co-author of the first Solder and Solder Joint Properties Handbook, and is active in the development of government, national, and international standardization in soldering and printed wiring boards.

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NEW HOT BAR DESIGN ADDRESSES FLATNESS AND THERMAL UNIFORMITY ISSUES FOR FPD AND TAB SOLDERING

by

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ABSTRACT

Contact or "hot bar" soldering is used with the intention of providing force to insure lead to pad contact during soldering. A primary benefit of contact soldering is realized at lead pitch of 0.015" and lower, with contact heating becoming a primary means of solder attachment for devices with lead pitch under 0.010".

The most common form of hot bar heating has been an electrically heated resistive element or "thermode". Intrinsic design issues limit the ability to address thermal uniformity and flatness through thermode design. Application of thermode heating to fine pitch devices (FPDs) and Tape Automated Bonded (TAB) devices of large pin-out is often limited by the inability of thermode heaters to achieve sufficient flatness, co-planarity and thermal uniformity.

This paper describes a new hot bar design, a "convector", which addresses straightness, element to element planarity, and thermal uniformity for the specific purpose of FPD and TAB single site soldering, whether for initial soldering during device placement or for the purpose of rework and repair.

INTRODUCTION

The ability to achieve uniform lead to pad contact during single site soldering is adversely affected by lack of co-planarity. Non co-planarity is the combined result of:

1. The planarity of device leads with respect to each other. (Fig. 1a)
2. Flatness or planarity of the board at the placement site. (Fig. 1b) and
3. Co-planarity between the device and lands. (Fig. 1c)

As lead fragility accompanies decreasing lead pitch, a point is reached where the combination of co-planarity issues and lead fragility make it difficult to insure lead to pad contact by simply applying force to the device package and transmitting that force through the leads. At this point some form of force application to the leads is required to insure contact. This typically occurs at lead pitch under 0.015"; but, the specific point at which it may occur is a combined function of non co-planarity, lead fragility, and lead count.

Contact or hot bar heating is one way to provide force application to component leads during soldering. Correct use of contact soldering must overcome the combined co-planarity issues and simultaneously meet thermal uniformity requirements so that effective and controlled soldering is accomplished.

This paper describes a new form of contact heating designed to address the combined requirements of co-planarity and thermal uniformity for FPD and TAB soldering. Tests to determine individual heater straightness and heater assembly co-planarity will be described, and results of those tests reported. Thermal testing was structured to measure individual heater and heater assembly uniformity under load conditions to determine linear (along one heater) and side-to-side (from heater to heater) temperature uniformity of lead-to-pad interfaces during a soldering operation. These results will be shown along with results on the same test setup for a comparable thermode system.

The results will be summarized, conclusions presented and further work in the field proposed.

CONVECTOR DESIGN

Figure 2 shows the design of a single convector heater. Hot gas emanating from the heater cartridge heats the conductive member, with the exhaust gas deflected away from the site being soldered. The conductive member thus becomes solely a transmitter of energy and its design is independent of electrical characteristics. This permits the choice of a hot bar material for its desirable thermal characteristics, in particular for high thermal conductivity. It also permits design of the convector blade to optimize thermal uniformity by allowing sufficient blade thickness to maximize heat flow.

The achievement of thermal uniformity throughout the convector blade is a major step toward eliminating warpage due to differential expansion. Additionally, since few conformation restrictions apply, the blade may also be designed for structural rigidity and a mounting scheme which permits compliance.

The individual heater cartridges are mounted onto a stage which permits adjustment of heater patterns to rectilinear arrays to conform to different lead conformations. (Fig. 3 and Fig. 4) Thus, within a range, convectors may be adjusted to various heating patterns without requiring tooling changes.

THE TEST SYSTEM

The test system used for convectors incorporates the assembly described above and shown in Fig. 3. The convectors used for the test were 0.060" aluminum. A convector length of 1.7" was used for straightness and co-planarity measurements; a 1.1" convector, which matches the lead outline of a 132 lead, 0.025" pitch device, was used for thermal measurements.

Microprocessor control is provided for the process control functions. The system tested used a single channel control scheme, with the thermocouple from one heater used to control all four heaters; thus, the results are comparable to those obtained with a thermode system which uses the same method of control.

An independently controlled bottom heater is provided, and either single-stage heating without pre-heat or two-stage cycles incorporating controlled pre-heat are used. When two-stage heating is used, top and bottom heater temperatures are independently controlled for the pre-heat and for the reflow cycles; time settings for pre-heat and reflow are independently set and controlled.

The system uses vision through the open center of the heater assembly to permit viewing all four sides of the device during the act of placement, and split imaging is used to provide sufficient magnification for fine pitch device placement.

The thermode system tested was equipped with 5-pole thermodes for the 132 lead, 0.025" device. The thermode was titanium, 0.025" wide x 1.065" long.

MECHANICAL TESTING FOR PLANARITY

It is of first importance to understand the elements which lead to even contact between the heaters, the leads of a device, and the underlying substrate or circuit.

Using the definitions in Fig. 5, "straightness" is a linear function; it applies to the contacting edge of each conductive member in that the blade must be straight or linear. Then, to the degree that the contacting portion of the blade has any surface width, the plane of that surface is referred to as its "flatness". "Co-planarity" applies to the relationship of the various planes involved to operate in the same or parallel planes; this includes the planes of the four heater blades, the leads of the device with respect to themselves and, also, to the placement site. The placement site is then judged as to its "flatness" and then as to its co-planarity with respect to the device leads and the surfaces of the contact heaters.

Tests were structured to measure the straightness of the convector blades under varying conditions. Then the co-planarity of the four convector blades in the assembly were tested.

CONVECTOR STRAIGHTNESS

Test Conditions:

For Convector straightness and heater assembly measurements, the convector to be measured was mounted to an 8" Brown and Sharpe leveling table on a granite surface plate. Height measurements were made with a Federal Model 432 Indicator with Model EHE-1048 Electronic Gauge Head. The points for lateral positions where height measurements were to be made were simply marked in 0.10" increments on the side of the convector blade for individual blade straightness measurements. For measurements of the assembly, the positions for measurement on each of the blades were marked in their centers and 0.10" in from each end.

The convector blade was first measured "as machined". A second test was performed after lapping the blade with a standard grade ceramic lapping disc, flat to 50 microinches; Abrasive Sales Company, Grade WAL-40 lapping paste was used. The assembly was tested only after lapping.

Results

Convactor Straightness Data for convactor blade straightness were normalized by plotting the linear regression for each set of data, then subtracting the corresponding linear regression value from each data point. This has the effect of correcting for tilt of the convactor blade during measurement and of analyzing each set of data around a common reference plane.

Individual convactor straightness on an 0.060" aluminum convactor, as machined was shown to be $< \pm 44$ microinches (Fig. 6). When lapped, the blade improved only slightly to ± 38.5 microinches (Fig. 7).

The straightness testing under heat was performed by heating the convactor blade to 230°C; measurements were taken with the convactor blade in free air.

The heated blade was tested in two ways. Firstly, the assembly was held by its normal mounting; secondly, to minimize effects of assembly growth and resolve the straightness to just that of the blade itself, a mounting was devised to hold the blade below its tip and let the body of the heater expand freely. Straightness worsened slightly to ± 160 and ± 119 microinches respectively. Fig. 8 shows the comparison of hot to cold convactor straightness measurements.

Fig. 9 shows the combined results of straightness measurements.

Compliant Mounting In order to compensate for lack of co-planarity from heater to heater in the completed heater assembly and to permit individual heater planarity adjustment with its corresponding lead/pad site, the convactor blades are attached to a compliant mount. The mount uses beam flexure to achieve compliance. In this manner interference between moving parts is avoided, particularly desirable when operating in the relatively hostile environment of heat and flux fumes.

The mount is designed to provide a ± 0.010 " compliance with 8 lbs. total force application on the assembly. Fig. 10 shows the effect of a single blade contacting a 0.010" wire on a flat surface.

Heater Assembly Co-Planarity Fig. 11 shows the vertical height measurements performed on the complete heater assembly. The assembled heaters showed co-planarity within ± 1176 microinches (1.176 mils).

TEMPERATURE UNIFORMITY

Test Conditions

Test Board The test board was an 8" x 12", 0.062", FRP, 4-layer multilayer circuit assembly. The measurement site was prepared by removing solder from the specific pads where thermocouples were to be located on a 132 lead, 0.025" pitch site. The sites used were the center lead of each side and, additionally, the 4th and 29th lead on one side (front). (Fig. 12)

The device was attached to the site using high temperature epoxy (Epoxy Technology single component epoxy, B/9121-5, 390°C degradation temperature) under the package body to prevent movement during repeated temperature exposure. The package was soldered in place on a Sierra FPD system, with repeated heat cycles from the soldering operation used to cure the high temperature epoxy.

Unsoldered leads at the specific T/C attachment sites were lifted, 0.002" Type J thermocouples were placed on the measurement pads, and high temperature solder (10%Sn/88%Pb/2%Ag) applied. Leads were brought into contact over the T/C, then soldered in place using a soldering iron with high temperature tip. A straight edge was used under magnification to check planarity of thermocoupled leads with the balance of leads on the device; contact soldering further ensured the relative straightness of each side.

Each T/C was terminated in a sub-miniature, compensated T/C jack mounted onto the circuit assembly. The completed measurement assembly is shown in Fig. 13.

The same board was used for all temperature measurements on all systems.

Instrumentation Temperatures were measured using a multipoint data logger comprised of a 286 AT computer, LabTech Notebook LTN-03 software, Metrabyte EXP-16, 16 channel multiplexer board. Data acquisition interval was 1 second.

Test Systems The convector test system was used with a convector idle of 150°C; the convector was brought to 250°C prior to lowering the assembly onto the test board. After reflow, power was shut off and the convectors remained in contact until solidus was achieved. 8 lb. force was used to achieve contact.

The thermode system was used with a thermode idle temperature of 100°C. The thermode was brought into contact with the test board simultaneously with power application. Thermode temperature was 320°C. The thermode remained in contact until solidus was achieved. 5-10 lbs force was used during initial contact, increasing to 25-45 lbs. after approximately 5 seconds.

RESULTS

Thermode

Temperature uniformity of a single side was measured as $\pm 13.5^\circ\text{C}$. (Fig. 14a) Uniformity of the four sides was $\pm 13^\circ\text{C}$. (Fig. 14b) The combined uniformity, including temperature differential along one side as well as side to side differential was $\pm 26.5^\circ\text{C}$. (Fig. 14c)

Convector

Temperature uniformity of a single side was measured as $\pm 2.2^\circ\text{C}$ (Fig. 15a); side to side uniformity was $\pm 6.3^\circ\text{C}$. (Fig. 15b) Combined uniformity, including single side and side-to-side uniformity was $\pm 7.25^\circ\text{C}$. (Fig. 15c)

ACKNOWLEDGEMENTS

The author would like to acknowledge the efforts of Mr. Robert Cushman in performing mechanical and thermal testing in support of this paper.

CONCLUSION

A new form of hot bar heating applicable to Fine Pitch and TAB soldering has been described. Individual convector blade straightness measured under worst case conditions show no more than 160 microinch variation. With a four convector assembly, a 1,176 microinch variation was shown; the designed compliant mounting scheme allowing 0.010" compliance of each of the four convectors under a total 8 lb. load is sufficient to overcome the variation shown.

Temperature uniformity testing along a single side and in a four sided assembly shows that convector heating can provide uniformity within $\pm 7.25^{\circ}\text{C}$ as compared to $\pm 26.5^{\circ}\text{C}$ in an equivalent thermode assembly.

The convector design achieves significant straightness. When combined with compliant mounting, assembly co-planarity, and significant improvement in temperature uniformity, the convector hot bar technology appears to offer process control improvements over thermode heating.

When utilized in an adjustable assembly, automation is facilitated. The inherent design simplicity appears cost effective both in reducing the number of different blades required for a variety of device sizes and types as well as in the lower cost of the blades themselves.

The implication of these results is that assembly automation not readily achievable with thermode technology may be facilitated with a new and economical hot bar design.

Future work is proposed to test the convector technology in a production situation for fuller understanding of its effectiveness in producing solder joints predictably and reliably and of testing its use in a production machine with regard to system reliability.

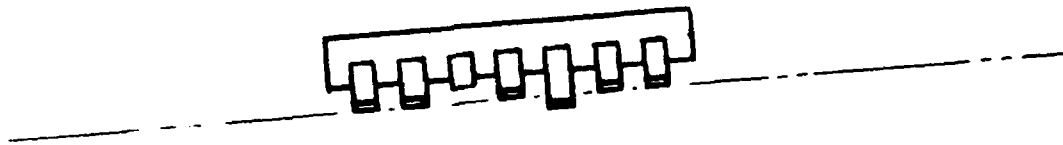


Fig. 1a. Planarity of device leads with respect to each other.

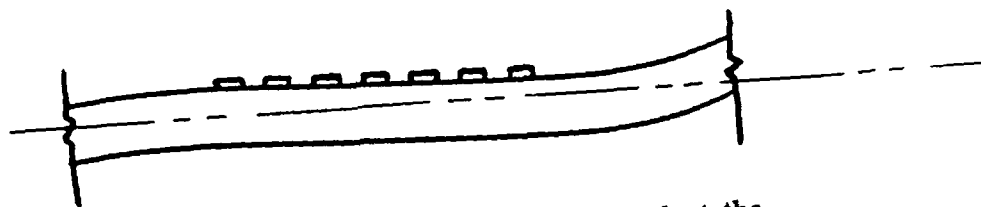


Fig. 1b. Flatness or planarity of the board at the placement site.

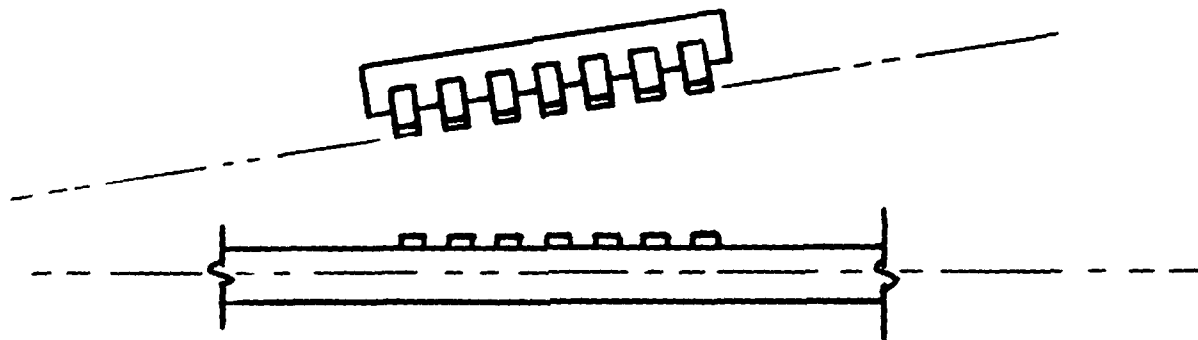


Fig. 1c. Co-planarity between the device leads and the lands on the board.

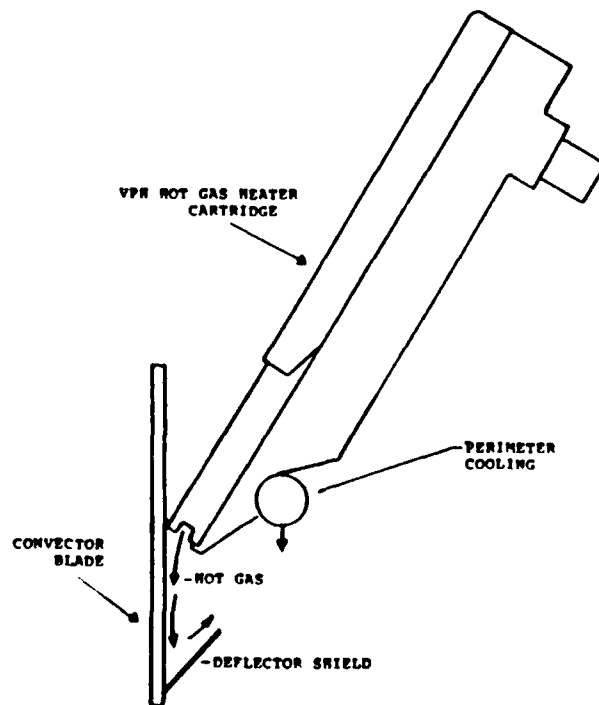


Fig. 2. The convector design combines a hot gas heater cartridge with a highly conductive blade for energy transfer.

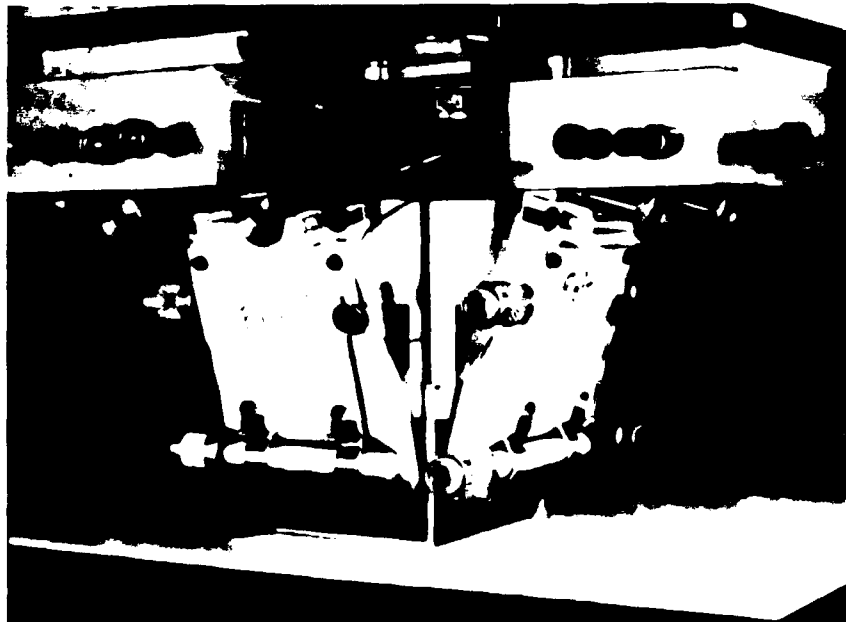


Fig. 3. Convector assembly for four-sided heating.

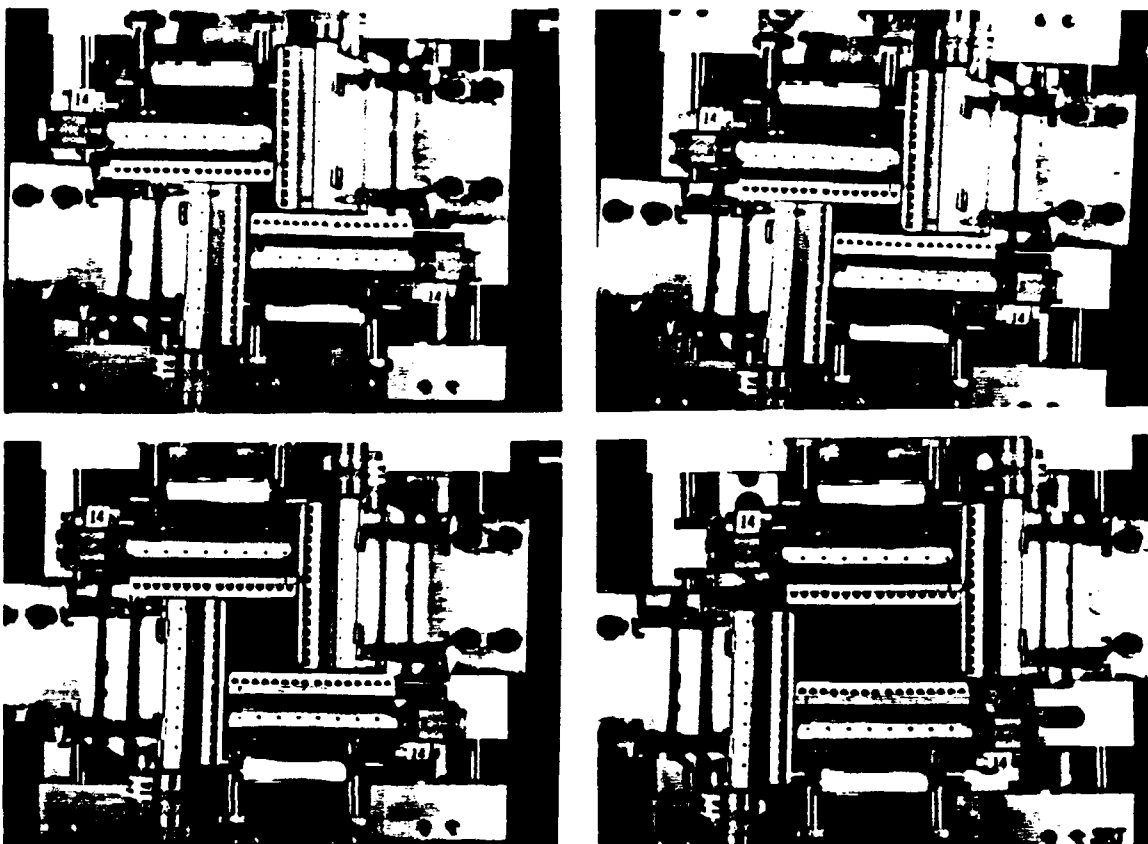


Fig. 4. Programmable array permits adjusting the heating pattern for different device outlines.

<u>straight</u>	without a bend, angle or curve (of a line).
<u>flat</u>	having a surface that is without marked projections or depressions.
<u>co-pla-nar</u>	being or operating in the same plane.

FIG. 5. Definitions provided by "The Random House Dictionary of the English Language, Second Edition, 1987.1

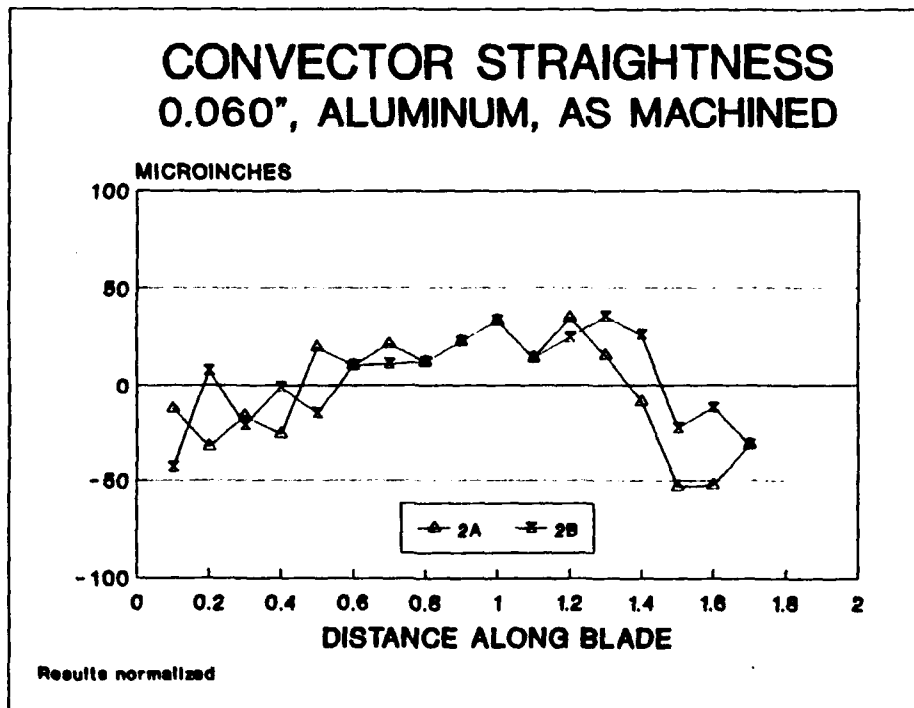


Fig. 6. Convector blade straightness "as machined".

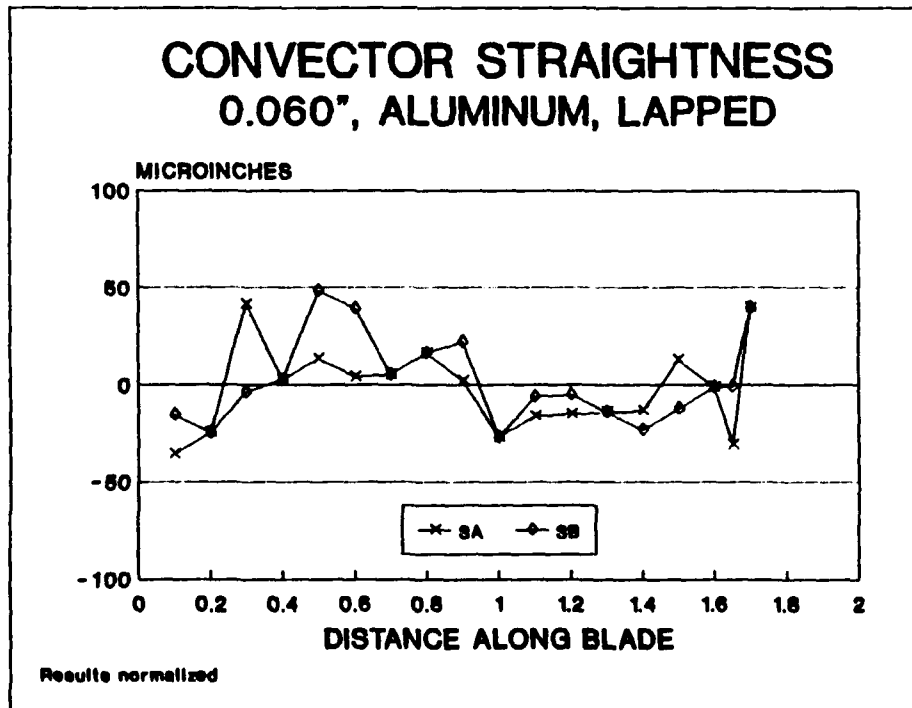


Fig. 7. Convector blade straightness "lapped".

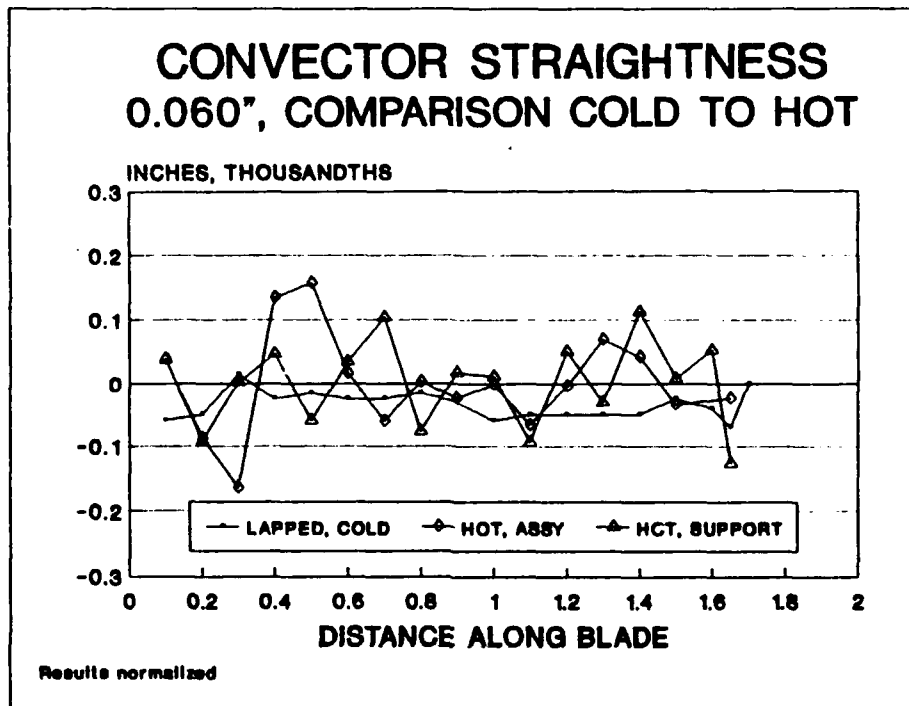


Fig. 8. Comparison of convector blade straightness from cold to hot.

	MACHINED	HEATED LAPPED	NORMAL	SUPPORT
STRAIGHTNESS (microinches)	+/_ 43.9	38.5	160	119
STD. DEV. (microinches)	26.9	20.1	75.3	65.7

Fig. 9 RESULTS OF CONVECTOR STRAIGHTNESS MEASUREMENTS.

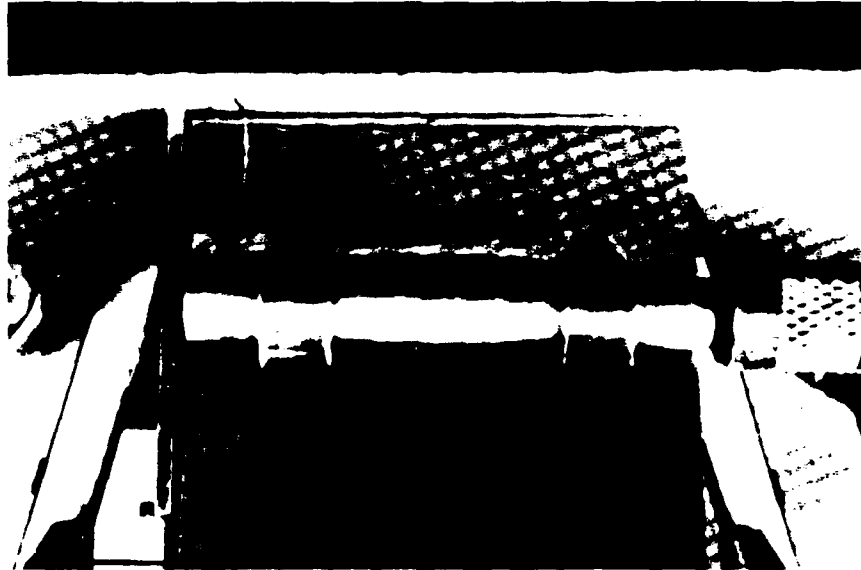


Fig. 10 The convector assembly is compliant to $\pm 0.010''$ with 2 lbs. force (8 lbs for a four blade assembly).

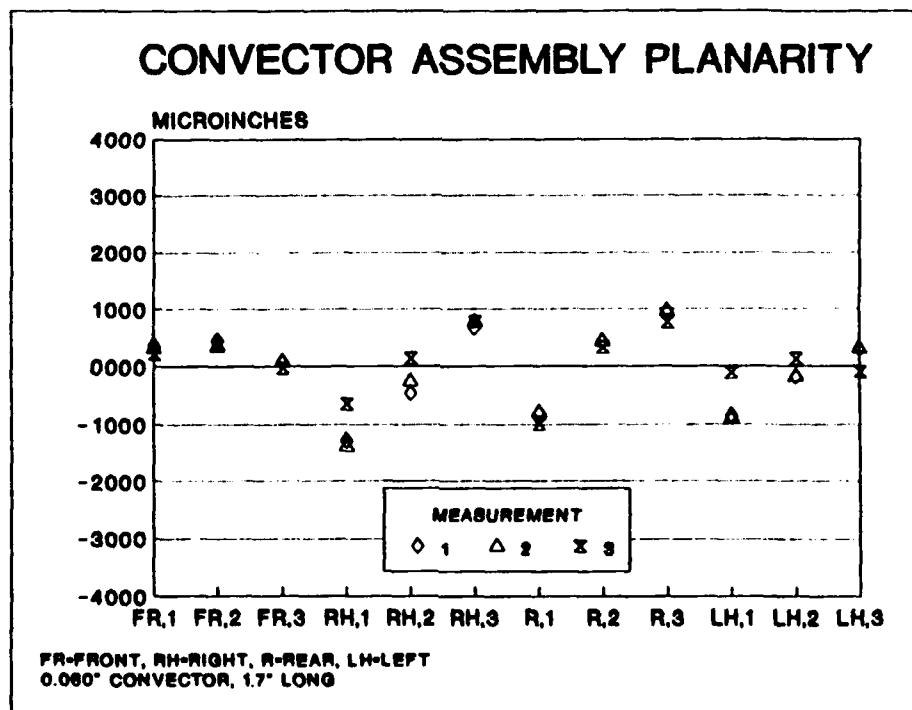


Fig. 11. Convector assembly co-planarity.

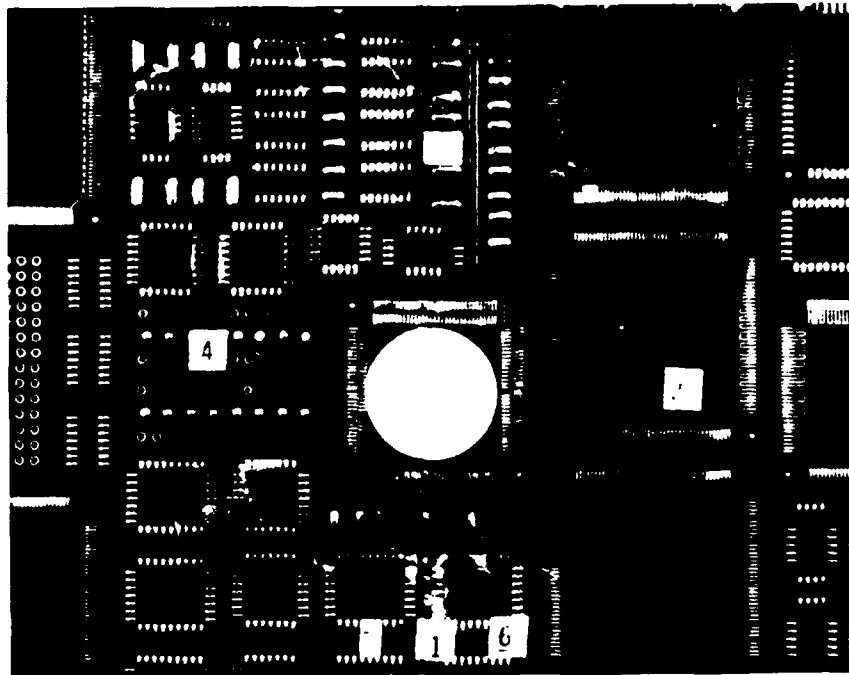


Fig. 12. Thermocouple locations on thermal test assembly.

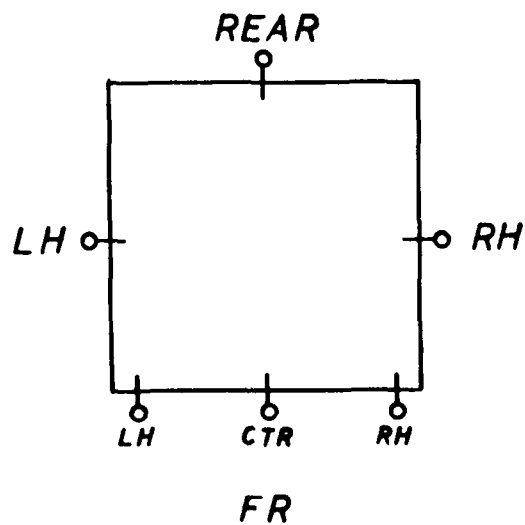


Fig. 13. Completed thermal test assembly.

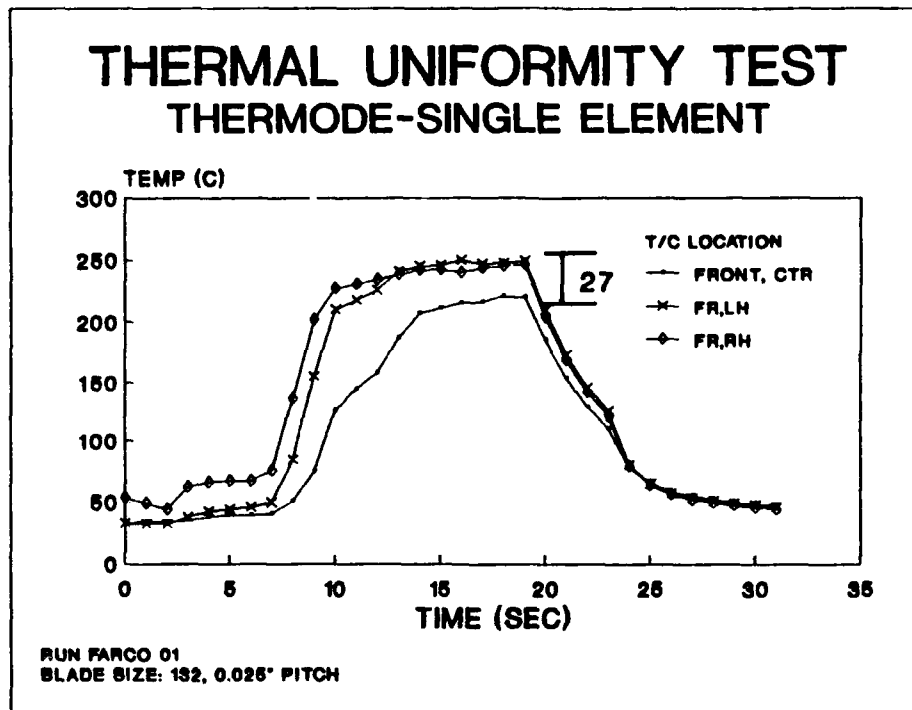


Fig. 14a. Thermode uniformity along one side of the thermal test assembly.

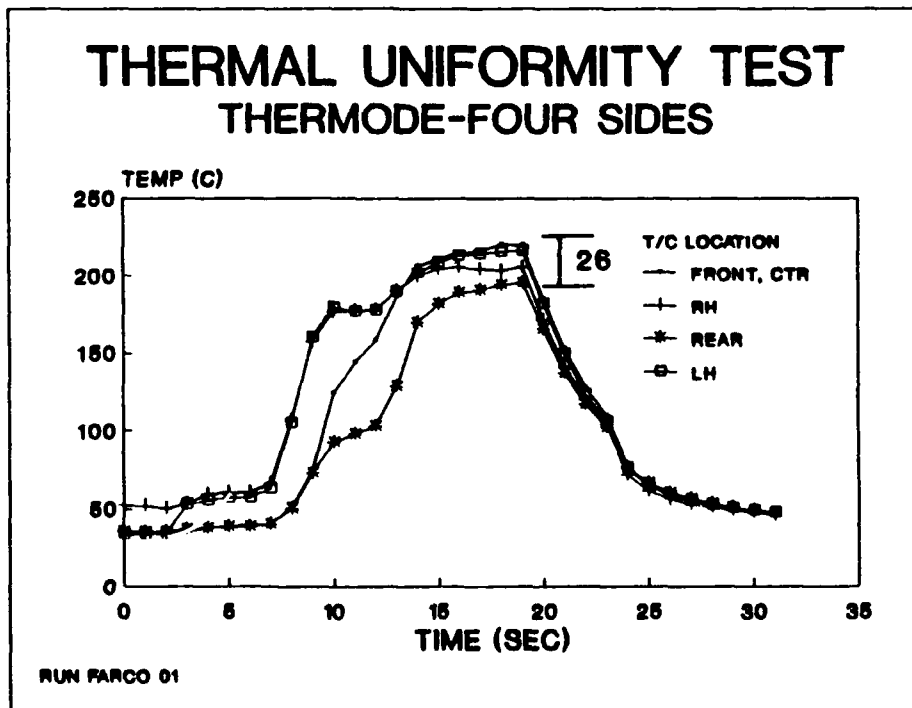


Fig. 14b. Thermode uniformity side-to-side on a four heater array.

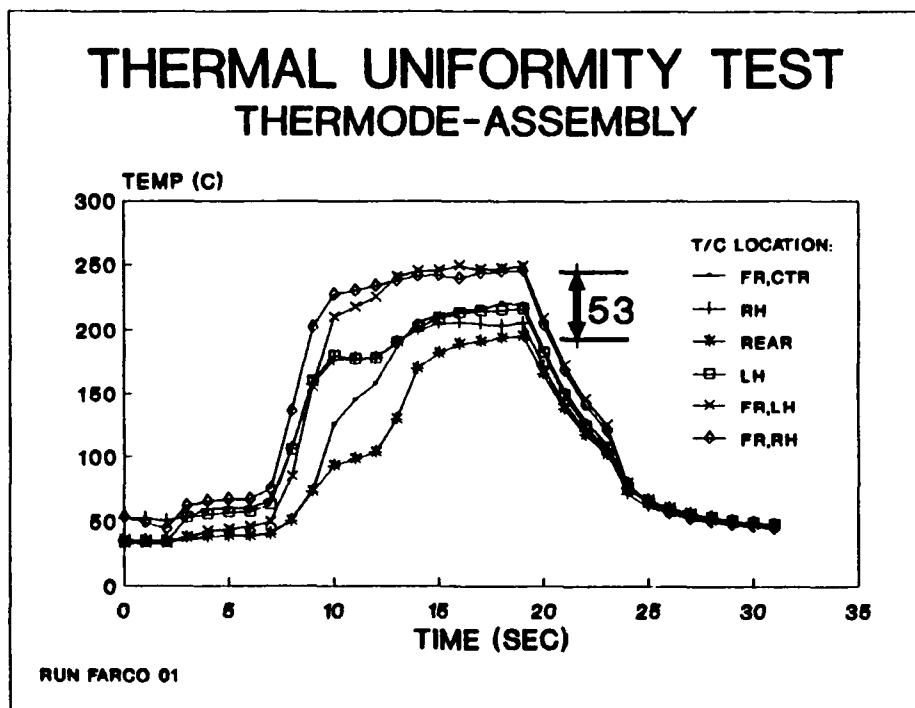


Fig. 14c. Thermode uniformity of an assembly, combining side-to-side and linear (along one side) measurements.

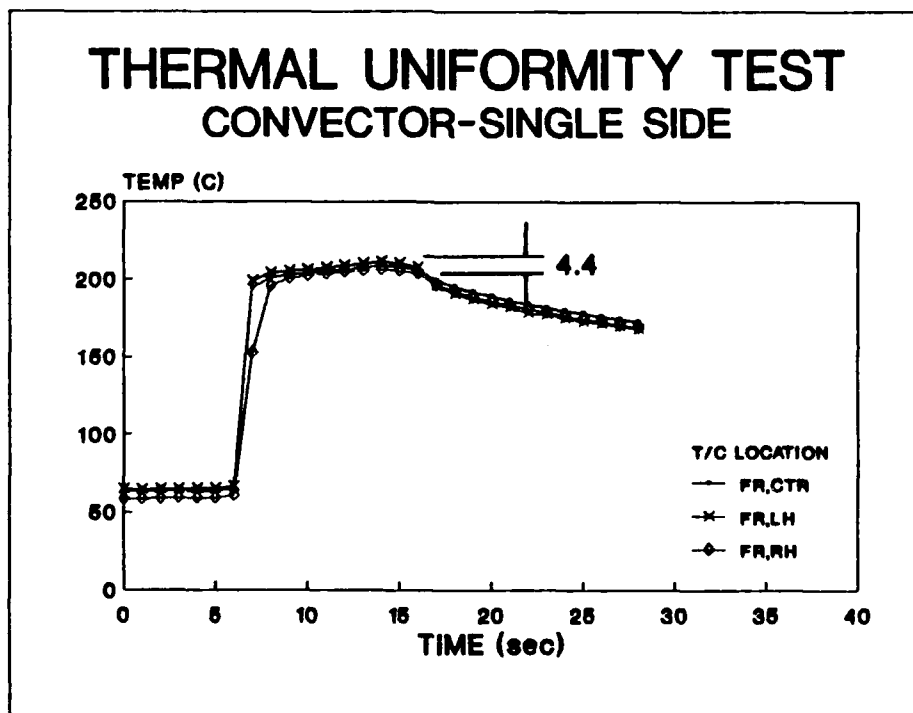


Fig. 15a. Convector uniformity along one side of the thermal test assembly.

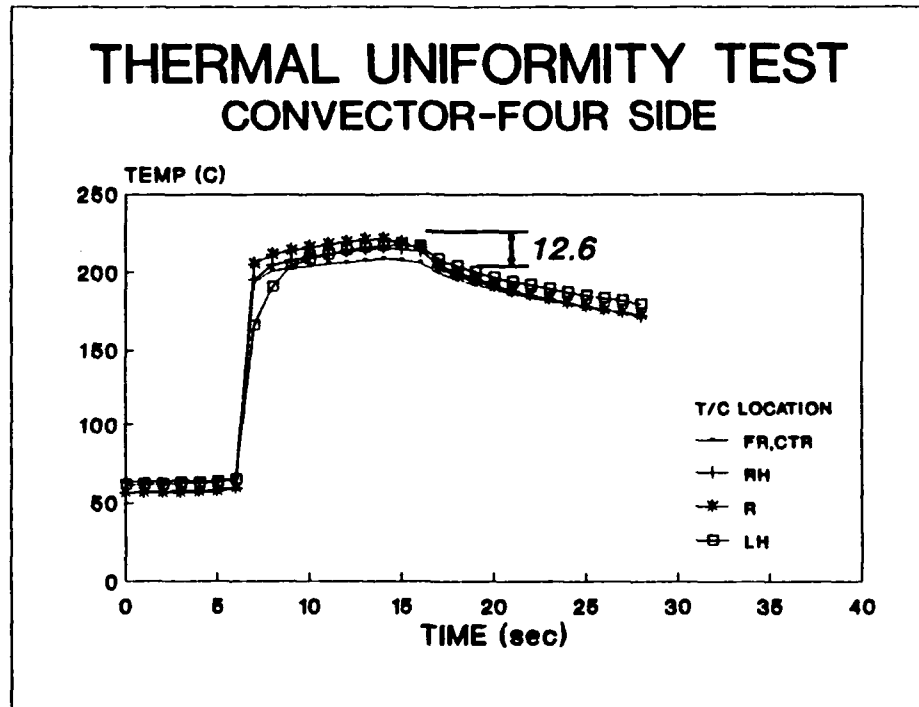


Fig. 15b. Convector uniformity side-to-side on a four heater array.

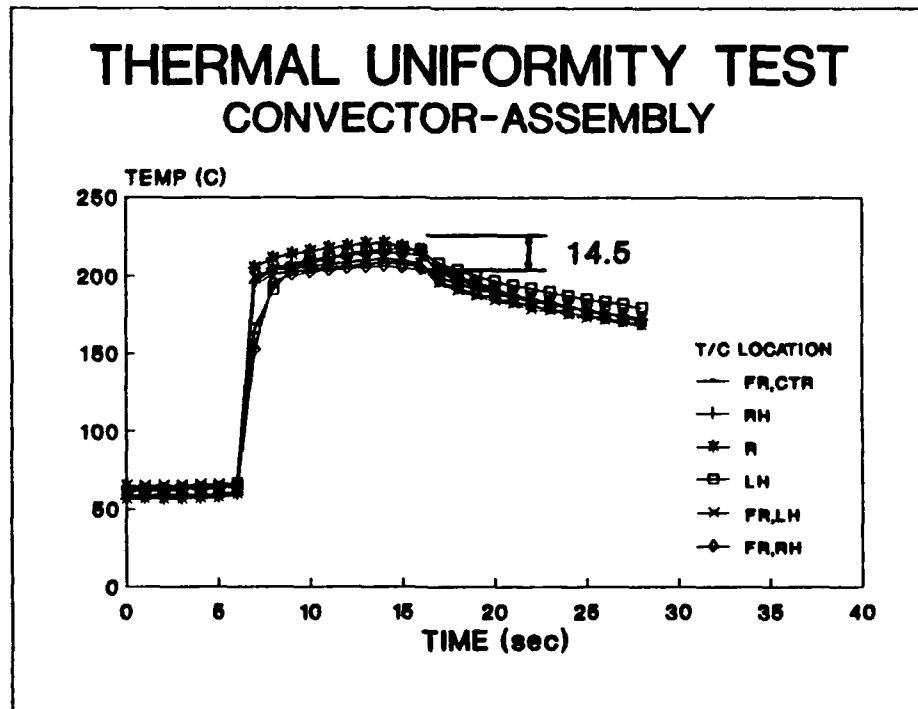


Fig. 15c. Convector uniformity of an assembly, combining side-to-side and linear (along one side) measurements.

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A USER'S EXPERIENCE WITH LASER SOLDERING

by

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ABSTRACT

This paper is an overview of our experience in the use of laser soldering on electronic assemblies, with the accent on surface mounted assemblies. This work was carried out during the period October 1988 to January 1989 using a "Vanzetti ILS 7000 Series" laser solder/inspect system on loan from Vanzetti agents in the UK.

INTRODUCTION TO LASER SOLDERING

The electronics industry is increasingly replacing conventional board techniques with surface mount technology (SMT). Among the most promising advantages of this technology are:

- (1) Shorter signal transmission times.
- (2) Space saving:-
Chips and components take up less real estate than the equivalent conventional components.
- (3) Increase in equipment functionality.

The new technology, however, also requires new or modified production processes. One critical process step, for instance, is the soldering of the surface mounted devices.

Generally within the commercial/military assembly sector wave soldering, infra-red reflow, vapour phase and laser reflow soldering are available. Compared with the aforementioned techniques, laser soldering offers other substantial advantages.

During the soldering process the board and the component remain cold, i.e. heat sensitive devices can be soldered. Furthermore, owing to the low temperature, no mechanical stress is induced between the board and the component.

As the laser is a very intense heat source, soldering is carried out very rapidly (in the case of our substrate 1000ms) and the intermetallic zone (IMZ) remains small. On account of the fast solidification of the solder, a fine grain structure results. The electrical and mechanical properties of such a joint are superior to those of other joints. Boards equipped with surface mounted devices only and mixed technology devices can be assembled and soldered.

A laser soldering system can be fully automated. All the necessary soldering operations can be carried out using a CAD system which would download component data and positions etc. to drive the system. Laser soldering takes place under normal atmosphere with no inert gases or additional chemicals required to protect solderability.

Both CO² and Nd:YAG Lasers are available with pulsed and continuous output. The first laser soldering machines, exclusively CO² laser systems have been in existence since 1976, while tests with Nd:YAG Lasers have been undertaken since 1982. A disadvantage of all of these systems was that the laser beam was fixed and the board had to be moved pad to pad, by means of an "X"- "Y" table or manipulator. This was time consuming and soldering of components with leads on all four sides difficult. The soldering time and energy per pad was also high (.5 Sec, 6 joules).

Nd:YAG Lasers emit radiation at a wavelength of 1.6 μ m and CO² lasers at 10.6 μ m, metals absorb 1.6 μ m better than the longer wavelength radiation (i.e. 79% at 1.6 μ m and only 26% at 10.6 μ m). The opposite is true, however, for the board material, in which case 78% of the 1.6 μ m radiation is absorbed compared with 98% of the 10.6 μ m.

The laser beam must be optically manipulated, i.e. deflected and focused. Nd:YAG Laser optics can be made of glass, whereas CO² optics must be made of I-R materials (ZnSe, GE, CdTe). As there are more optical glasses than I-R materials available, Nd:YAG Laser optics can be corrected more easily and in general this is less expensive. See Figure 1. The system used had a continuous Nd:YAG Laser though a machine is now available as a full blown laser soldering system with pulsed laser fitted.

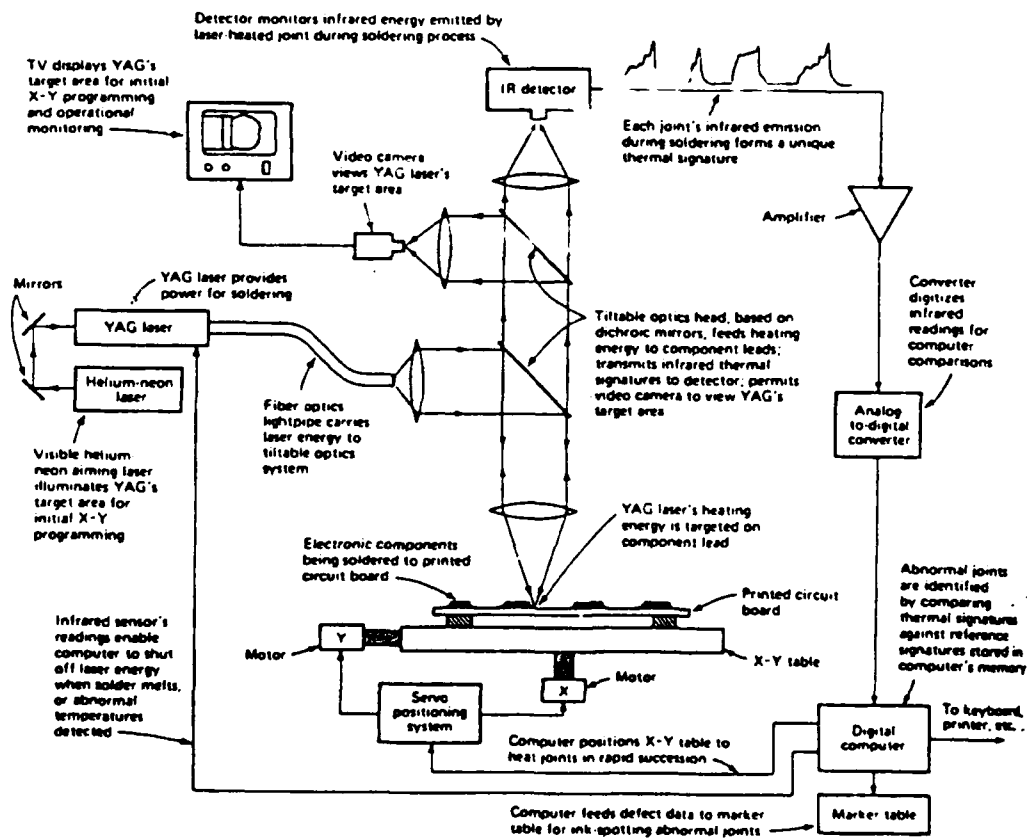


Figure 1

PROCEDURE

The two main areas in the experiment were PCB surface mounted assemblies and a metal cored Backplane assembly used on a military radar contract.

The following is a description of the parts used in this investigation.

PCB The standard type of PCB used during this investigation was approximately 9" x 6" 8 layer multilayer surface mount board built to the following complexity:

2 layer .006" Copper/Invar/Copper (C.I.C) used as a Power, Ground/Thermal plane and as a CTE mismatch, bonded to Polyimide laminate to make an assembly as per Figure 2.

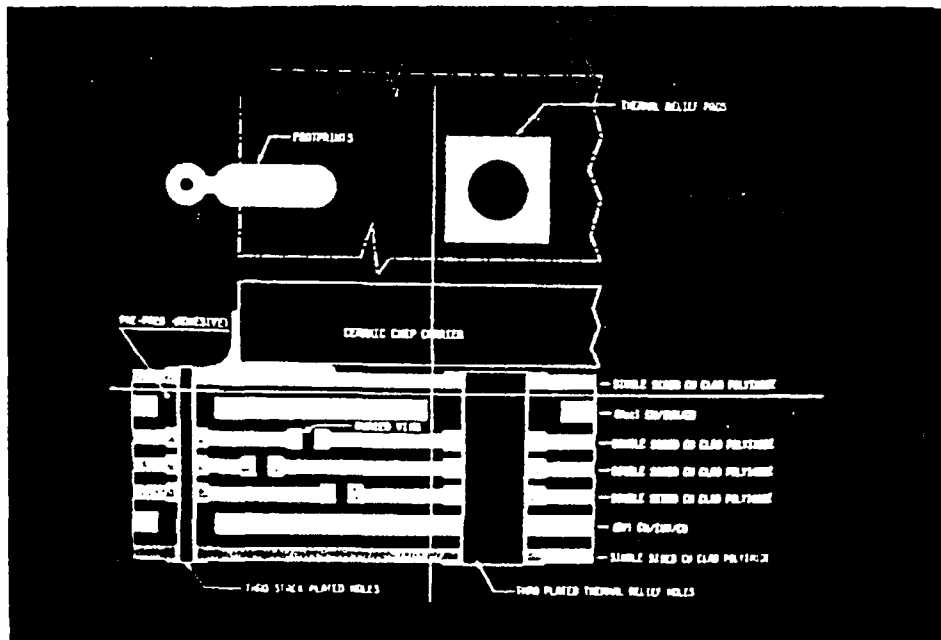


Figure 2

This consists of a footprint only layer on the top side of the PCB as shown in Figure 3.

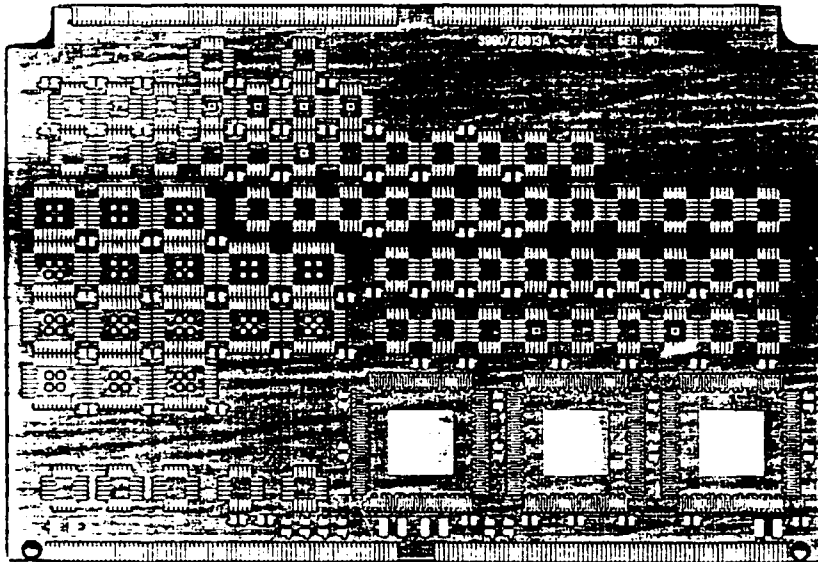


Figure 3

The selection of components used in the assembly varies from 20 Pin LCC up to and including 68 Pin LCC plus 132, 148, 196 quad flat packs as can be seen in Figure 4

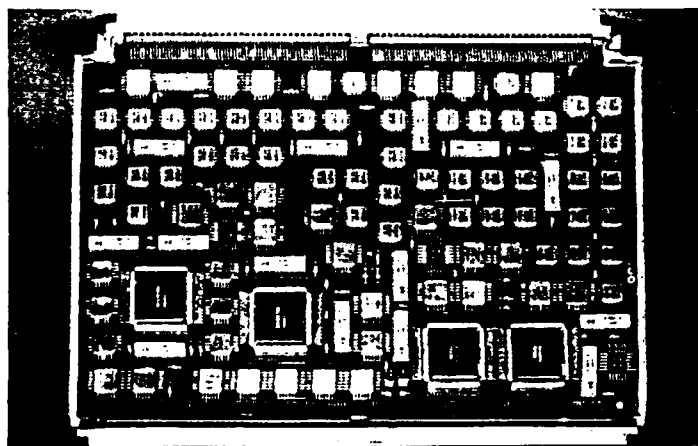


Figure 4 - Typical Signal Processor Board

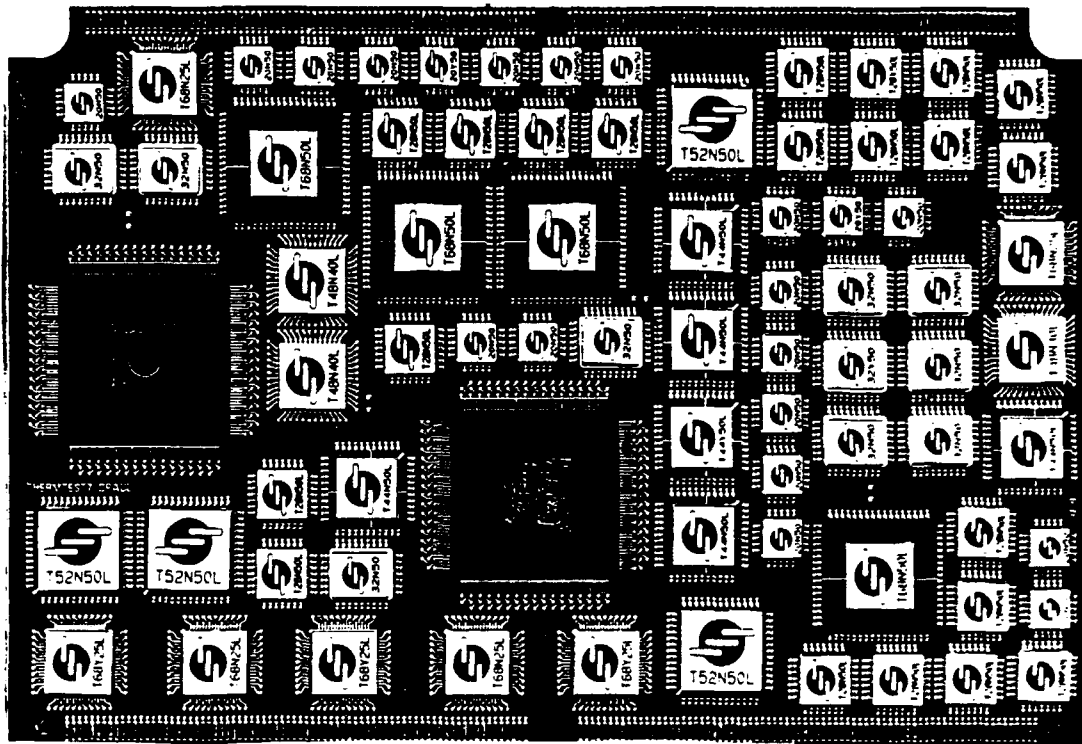


Figure 5 - Thermal Evaluation Assembly

This also includes a mixture of Hybrids and surface mounted components - see Figure 6.

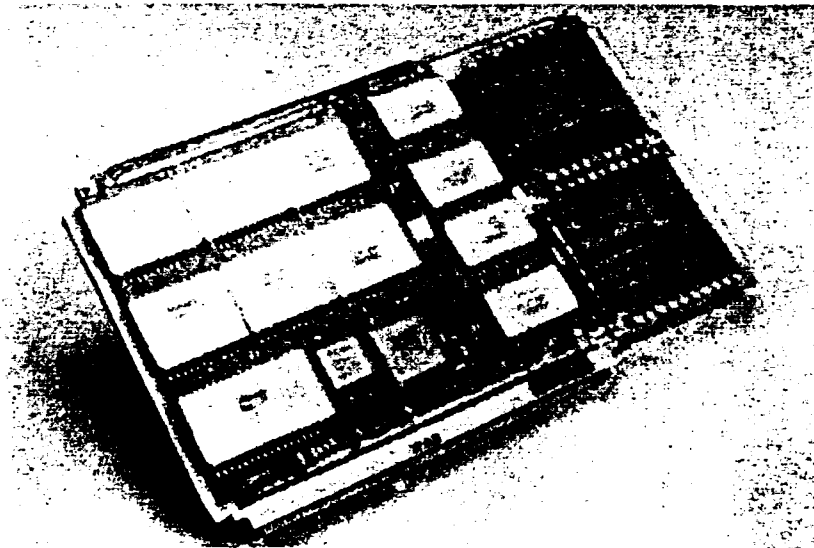


Figure 6

These PCB's are then mounted onto a cold wall/heat exchanger in order to achieve the high density packaging concept required in this contract. (Figure 7).

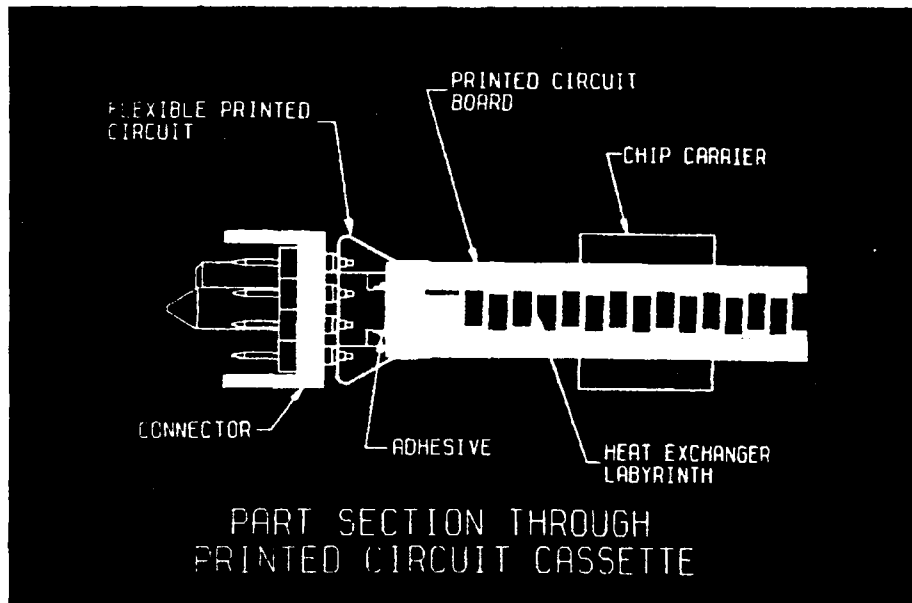


Figure 7

The laser soldering system was also used to investigate the problems associated with polyimide flexible connections (Figure 8)



Figure 8

and aluminium Backplane assemblies incorporated within this packaging concept. (Figure 9)

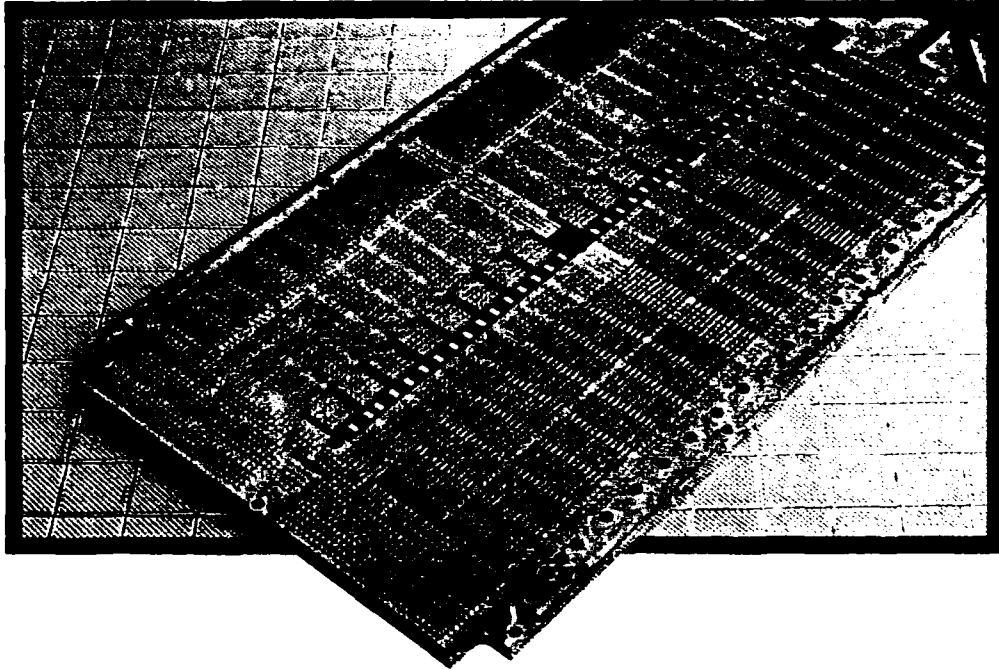


Figure 9

EQUIPMENT:

Vanzetti ILS7000 series laser soldering/inspection system. As described earlier, we were not interested in the inspection system and the equipment was used solely to evaluate laser soldering on certain of our specialised product range. Typical power settings were as follows:-

<u>Time</u>	<u>Pk Value</u>	<u>Laser Power</u>	<u>Results</u>
4000ms	3000 Pk	10W	Joint Good - Grainy (3874ms)
3000ms	" "	10W	Joint Good - Still Grainy (2994ms)
2000ms	" "	10W	" " (1962ms)
1000ms	" "	10W	" " (330ms)
1000ms	" "	11W	Joint Good - Better (996ms)
1000ms	" "	13W	Best Solder Joint (996ms)
1000ms	" "	13.5W	Not as good (996ms)
500ms	" "	13.5W	Poorer (24ms)

Against other reports and papers this appears to be extended as times of 20-50ms are quoted. This is probably due to the C.I.C. acting as a heat sink or because little work has been done around military PCB's and LCCC (Ceramic) type devices. The laser has to be calibrated through a power check and listed overleaf are some typical settings for this type of laser.

AMPS	10	11	12	13	14	15	16	17	Max
WATTS	3	4.4	6	7.8	9.4	11	13.2	15.2	Max 26.5

Setting up a board for assembly meant walking the machine through each sequence in a self teach mode using a C.C.T.V. screen with cross hairs to accurately target the laser onto the component and, or pad, though this operation could easily be achieved by interlinking with a CAD CAM system but due to time scales, this was not possible. Laser targeting was critical and appeared to vary with each component type. A library of target positions for each component would need to be built up to interlink with the CAD CAM data.

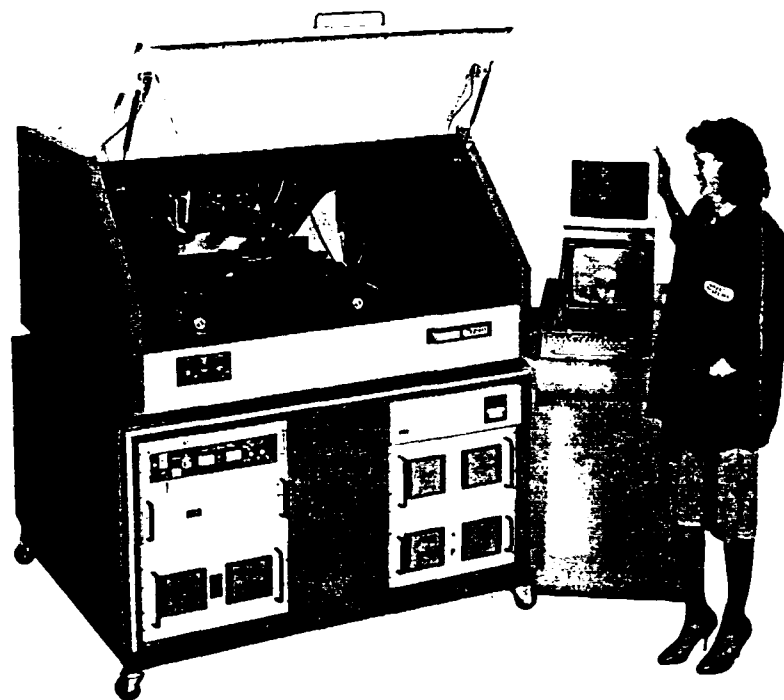


Figure 10 shows intelligent laser soldering system
 ILS 7210

PROCESS

The following popular ways of applying solder to the PCB surface prior to reflow are:

- (1) Solder paste, applied by a screen mesh or micro dispensing.
- (2) Unfused solder, electroplated to the PCB PAD layout by the PCB manufacture.
- (3) Solder pre-forms.
- (4) Solder Quick
- (5) Solder wire feed.

Processes 1 to 4 were used to evaluate the laser system during the course of the investigations.

Process 1 Solder Paste This was applied using a screen which deposited 300um onto a land pattern of a solder levelled PCB. The solder paste used was 63/37 tin lead in an effort to meet MIL requirements.

Process 2 Unfused solder electroplated onto the PCB to a thickness of 50um. This was 60/40 tin lead, screen printable flux was applied to a thickness of 20 m.

Process 3 Solder preforms, these rings of (.075" x .045" x .030") which consist of 63/37 tin lead and are hand placed onto the appropriate pins of the Backplane assembly.

Process 4 Solder quick (trademark for Raychem product) consists of a solder preform which is delivered in a tape format in pitches, ranges from .020" to .050". The tape is cut to the required length and aligned to the PCB land pattern before assembly of the flex.

Results

Process 1 Solder Paste:- Due to the rapid rise in temperature of the solder paste during the laser soldering process, problems were encountered with solder balling causing potential shorts on the assembly (see Figure 11)

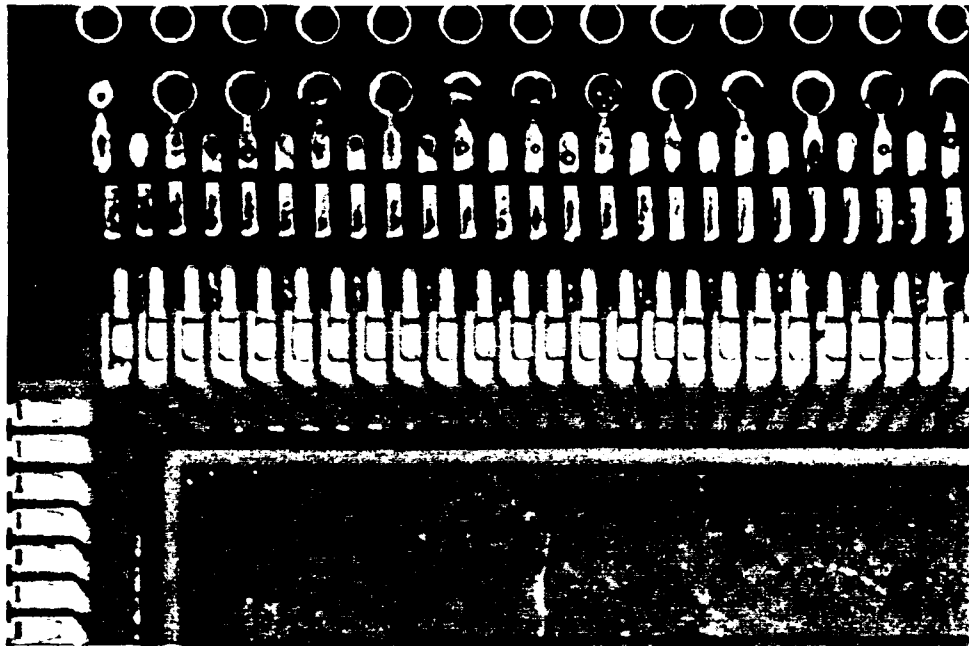


Figure 11

and also no reflow of solder paste due to the land pattern configuration resulting in non-wetting see Figure 12.



Figure 12

Process 2 Unfused Tin Lead. Due to partial contact of components to land pattern on PCB, solder joints were not always complete, this resulted in an unexceptable joint. Figure 13.

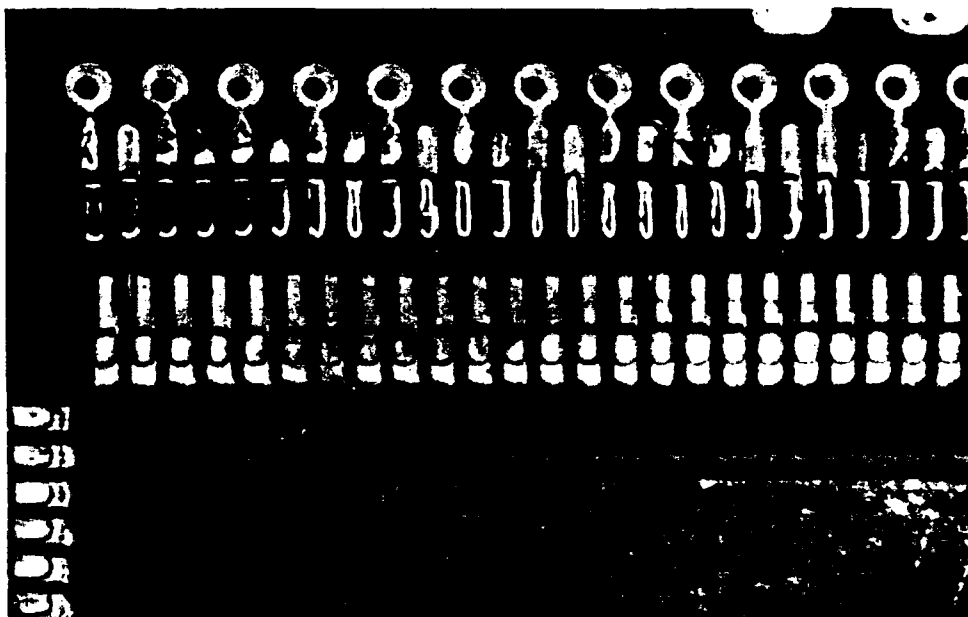


Figure 13

Process 3 Solder Preform and laser soldering were used because of the length of pins protruding from the Backplane and the requirement of the assembly to be wire wrapped after soldering. The pitch of adjacent pins (.100") restricted hand soldering operations due to the accessibility of the soldering bolt, Figure 14

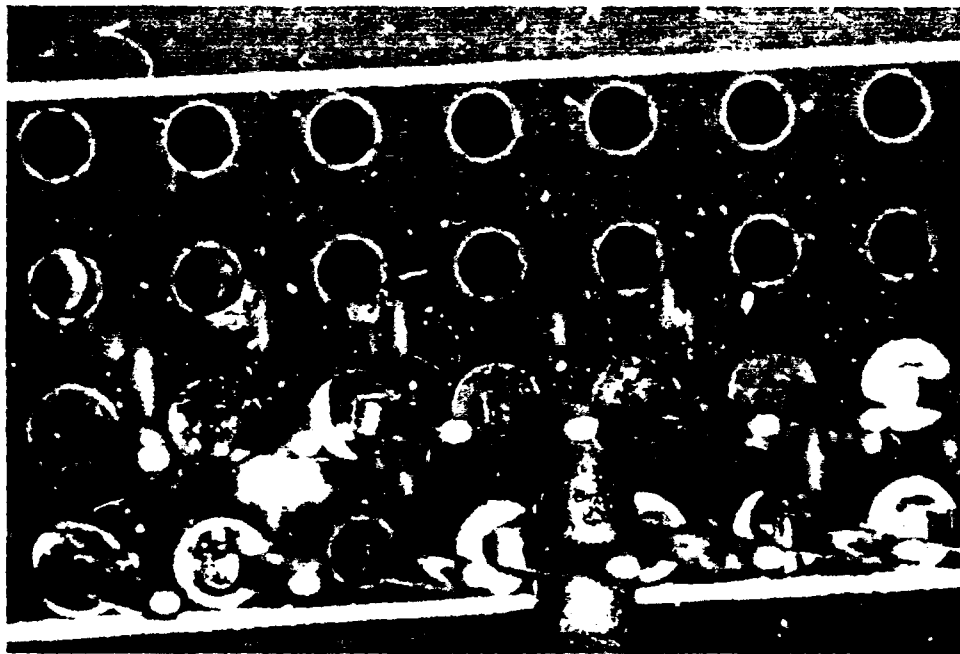


Figure 14

wave soldering was also impracticable due to the requirement to wire wrap the pins. Vapour-phase soldering could not be used because the insulation on the pins would not withstand the temperature, hence the requirement for laser soldering and a measured amount of solder. The results were very encouraging.

Process 4 Solder Quick was used in conjunction with flex-rigid and quadflat packs as this concept guaranteed a controlled amount of solder during reflow and was also seen as an alignment aid. Without fuller investigation into the tooling required to successfully align the tape, results proved inconclusive.

CONCLUSION

Advantages:

1. Laser soldering is ideal for dense packaging of components on a PCB as the beam (typically .018"-.024") can reach without disturbing other adjacent devices. It is also ideal for soldering pins etc. on a tight pitch .050"-.100". Very accurate pin point of heat.
2. Both sides of a double sided PCB can be populated without subjecting the assembly to multiple thermal shocks.
3. Rapid solidification of the solder joint results in a fine microstructure, though the way in which this benefit alters with time at temperature, storage or service is yet to be qualified. Further experimentation is yet required on this subject.
4. As was seen with the hybrid assemblies laser soldering is ideal for soldering heat sensitive devices.

5. Thermal expansion of the PCB in the 'Z' axis during laser soldering is minimal which creates a product with higher reliability.
6. Laser soldering forms solder joints that are low stress as the PCB is at room temperature during the soldering operation (except for very localised heat input as each joint is formed typically 1000MS).
7. For high reliability products, PCB's can be part assembled and completed at a later date. This is in contrast to all other soldering assembly processes.
8. The board can be inspected as it is built by measuring the infra red emission before and during soldering of each joint.
9. The level of additional intermetallic compound formed in the joint is kept minimal.
10. Can be linked into CAD CAM system and board generation data down-loaded to the laser soldering machine to make up a program for laser soldering.
11. Ideal as an aid to fit a few surface mount specialist components onto a mixed technology or part assembled surface mounted assembly.

DISADVANTAGES:

1. Initial cost of production equipment.
2. Specialised tooling may be required to hold specialised components in place, i.e. quad flat packs. Intimate contact between parts being soldered is critical.

3. Slow in comparison to other assembly processes, i.e. wave soldering V/P, I/R reflow especially on our product type.
4. At present only appears to work well with solder preforms and unfused tin lead. Solder paste spatters or balls causing potential problems even after pre-bake and raises a quality question mark.
5. The laser soldering process can cause problems normally associated with traditional surface mount soldering processes, i.e. that one side of a component can "tombstone" due to the surface tension of the solder.
6. Critical setting of the laser to the component and pad, if not in exactly the right position then the solder joint was not made. Safety detector trips out.
7. Continuous solder paste strip did not work successfully and left particles of solder (solder balling) all around the device.
8. We found components pad layout/sizes are critical and that heat did not travel or reflow solder at the outer points, despite attempts to increase laser heat input and time etc.
9. Height from work platten to laser is critical. Special fixtures are required to hold PC board and components so that the laser beam is focused.
10. Higher level of engineering expertise and skill required to operate and tool up for production.
11. Contamination and accurate targeting a factor in no joints made situation.

REFERENCES

1. Handbook of surface mount technology by Stephen W. Hinch.
2. Lasers light way to better PCB solder joints by Richard I. Alper, Vanzetti Systems Inc. "Research and Development" March 1987.
3. Intelligence comes to laser soldering "Electronics" July 10, 1986.
4. Soldering in electronics (second edition) by R. J. Klein Wassink. Electrochemical Publications Limited.
5. A scientific guide to surface mount technology by C. Lea. Electrochemical Publications Limited.
6. Laser soldering - production and microstructural benefits for SMT by C. Lea. "Soldering and Surface Mount Technology" Number 2 (Pages 1321), June 1989.
7. Wave soldering vs reflow soldering metallurgical consequences or the choice between the two methods by R. Strauss. "Brazing and Soldering" No. 14 Spring 1988 (Page 5-8).
8. Soldering of surface mounted devices new tasks and their solutions by R. Strauss. "Brazing and Soldering" No. 10 Spring 1986 (Page 21-23).
9. Laser soldering of surface mounted devices by F. G. Meyer. "Brazing and Soldering" No. 12 Spring 1987 (Page 40-41).

10. Inner layer or post cracking on multilayer printed circuit boards by M. W. Gray. "Circuit World" January 1989 (Page 22-29).
11. Substrates for the new generation of SMT by D. Kingsley "Circuit World" January 1989 (Page 4-5).

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CLOSED-LOOP SOLDERING

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ABSTRACT

This paper discusses some basic ideas about process development and control in Part I and applies them to soldering in Part II. Because it is possible to understand how design, materials and process affect the product, it is unnecessary and inappropriate to resort to the statistical-correlation methods that are applied to complex processes. A process qualifies for the label "closed loop" only if the design and materials going into it are controlled. The types, degree, and sophistication of control needed for a process are to be judged by consistency of the product. For soldered assemblies, the product is evaluated by visual inspection, and the adequacy of process development and control depends on the adequacy of inspection.

Inspection can be improved if it is regarded as a process. It can also be improved if inspectors understand which features are important and which can be ignored safely, i.e. by understanding their causes and associated risks. Much of the criticism of visual inspection, and perception of need for automated inspection, derive from a failure to distinguish clearly enough between material and process variables, between the two types of inspection (product-oriented and materials/process-oriented) and between appearance and risk.

Properly controlled visual inspection is well suited for evaluating the soldering process. The most important visual attribute to look for in solder inspection is the contour of the fillet, because this is what reveals the quality of wetting, and wetting is the most important physical attribute of the connection in determining its strength and reliability. Wetting depends on just two basic requirements, heat transfer and solderability, and these are discussed in some detail. Causes of nonideal texture and luster of the solder are given, but these attributes do not affect reliability, nor is measuring solder purity important.

Additional factors which do affect reliability relate more to design and materials than to process. Failures to deal with these factors can result in solder defects that are undetectable by any inspection technique. The answer to this problem is therefore not automated inspection to find more kinds of defects than visual inspection can, but control of design and materials, as well as process, to prevent them entirely.

PART I - BASIC IDEAS

PROCESS DEVELOPMENT AND CONTROL

Development: Understanding or Statistics?

When a chemical process such as baking a cake or refining petroleum is being developed, process variables (time, temperature, pressure, flow rates, etc.) on the product are investigated. There are also material variables: the composition, viscosity, etc. of the feedstock. For consistent results, material variables need to be controlled, or at least measured, and compensated for (to the extent possible).

A process may be regarded as developed as soon as a recipe can be written that tells how to produce the desired product. For a process to be well developed, the permissible range of material and process variables must be established. For example, the effect of changes in the bake temperature and in the amount of leaven and pan grease should be determined, to establish how sensitive the product is to them. (The less sensitive, the wider the "process window".)

In the case of a simple process, these effects can be understood easily: lack of leaven makes the cake too dense, lack of pan grease makes it stick, too high a bake temperature produces a cake that is incompletely baked inside, dry or burned outside.

Some processes like petroleum refining are too complex to understand in this fashion. For such processes changes in the product caused by changes in material and process variables are studied using statistical methods. The product is measured for yield when produced by selected combinations of variables, and correlations are found and interpreted.

How should the soldering process be developed - by understanding the process, as for cake baking, or by statistical experiment, as for petroleum refining? The answer depends on whether cause-effect relationships can be found and understood. Ralph Woodgate makes the point effectively¹: "The [statistical] methods are useful in developing new or complex process parameters, but our soldering processes are simple, and well understood. If the theory and documented facts of the process are understood, [such] experiments will be unnecessary."

In numerous published accounts of the statistical approach as applied to machine soldering, it appears that statistics was used as a substitute for understanding the process. No mention is made about the accuracy or reproducibility of the defect calls, nor is any differentiation made of the kinds of defects that are found. Instead, since the implicit assumption is that the process is too complicated to understand, the soldered assembly is turned over to an inspector who looks for defects. The defects associated with each combination of process variables are simply summed, and the combination with the lowest defect rate is called the winner. The corresponding process yield (1-rate) is called the process capability. If this method were applied to cake baking, cakes would be baked using various combinations of leaven, pan grease and bake temperature, and submitted to an expert cake taster to rate on a scale of one to ten.

Just as the effect of not greasing the pan can be shown to be sticking, so the effects of lack of solderability, time in solder, etc. can also be demonstrated. The similarities and differences in the two methods of process development (statistical-correlation vs. defect cause determination) as applied to circuit card assemblies (CCA's) are shown in Appendix I.

Control: Close the Loop?

A process is controlled by controlling the independent variables. These variables include material properties. The term "process control" is sometimes used as if it included materials control, but to do so is unwise. The process variables can be adjusted independently at the beginning of, and often during, the process. Material variables are inherent in the materials: they can be measured before the process begins, but not readily changed. Some changes in a material variable can be compensated for in the process, but not all. For example, if too much water has been added to cake batter, the bake time can be extended, but if rotten eggs have been added, there's nothing that can be done except to reject the batter and start over.

The process variables can be controlled according to a set prescription ("open loop"), or by adjusting them based on what happens to the product, i.e. by monitoring and responding to the dependent variables ("closed loop"). The loop can be characterized by two separate attributes: adequacy of response and speed of response. The adequacy depends on how well all of the dependent variables are monitored, and on how effective the response to these variables is in controlling them. It can be thought of as the extent of loop closure. The speed is a measure of the delay between some deviation in a monitored variable and the response that is needed to bring it back. This is the tightness of loop closure.

It is commonly assumed that the tighter the process variables are controlled, the better. Is this true? The answer depends on the product. The assumption that "tighter is better" neglects the law of diminishing returns.

For example, one could imagine a microprocessor-controlled closed-loop cake baker, complete with expert system, that monitored the cake for taste and moisture at various locations and changed the shelf height or oven temperature as it baked. Could good cakes be guaranteed, and would this baker produce cakes better than any known today? The answer is that such a sophisticated system, even though it could detect rotten eggs, still couldn't do anything about them, and therefore the loop, though tight, wouldn't be fully closed! If the loop were more fully closed by ensuring that only good eggs went into the batter, the cakes would be consistently good, but they would taste no better than those baked in an ordinary home oven with its crude (but adequate) thermostat. Therefore the loop would be tighter than needed or useful.

While it is unlikely that anyone would seriously propose to build a closed-loop cake baker, a comparable suggestion for machine soldering can be found in several published articles. The suggestion is for an automated solder defect inspection system that will watch during machine soldering, notice the connections that aren't turning out right, identify the cause of these defects, and change the process in some way (examples are never given) so as to tighten the loop and ensure that the connection ends up OK, or at least that the next connections to be made are OK.

To be sure, this is what skilled hand solderers try to do, and a laser soldering machine can be purchased that imitates this "closed-loop" control as connections are soldered one at a time. But it should be clear that the assemblies, regardless of how they are soldered, will not be defect-free if the design is bad or the leads are unsolderable. The machine soldering process is shown schematically in Figure 1, with the factors affecting the outcome indicated with labeled arrows. The machine can be adjusted and modified in many ways, but there are limits to what can be achieved. Failure on the part of many people to comprehend this has caused process engineers and machine operators to be held accountable for factors outside their control, and has allowed problems to go unresolved. Appealing as it may be to have a machine soldering system with a built-in defect detector, process variables cannot be expected to compensate for uncontrolled material variables. Until material problems are prevented, the loop cannot be fully closed, no matter how fast the response.

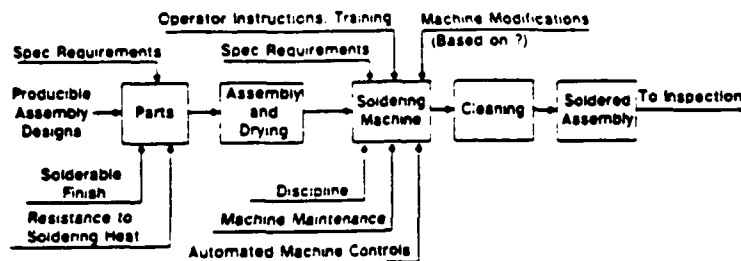


FIGURE 1 - THE MACHINE SOLDERING PROCESS

Assuming design and materials are controlled, would tight-loop automated inspection improve product quality, or can good soldering be achieved simply by holding the process variables fixed? The question can be answered if a single company can be found that solders successfully on a machine without built-in inspection. Ralph Woodgate reports that many companies are achieving rates below 100 defects per million connections. Presumably none of these companies would have any interest in tightening the loop with more hardware. At any rate, it is difficult to imagine how the remaining occasional defects could be eliminated by any real-time process enhancement.

This is not to suggest that inspection is not needed, but that the need is more for increasing the extent rather than the tightness of loop closure. For complete loop closure, a deviation in any significant product attribute (the stimulus) must be detected, and whatever adjustment is needed to bring it back into line (the response) must be determined and must be made. There is no benefit to the product if the information is not accurate or is not used. The inspection that is done must assign causes to defects that are found. If the causes are related to design, materials, or assembly, then the organizations responsible for these must be notified and they must respond by removing them (see Figure 2). These preventive actions are much more difficult, and take much longer, than running experiments on the soldering machine to find the best settings. However, because they are the right thing to do for improved loop closure, they are also much more rewarding, as these successful companies have shown.

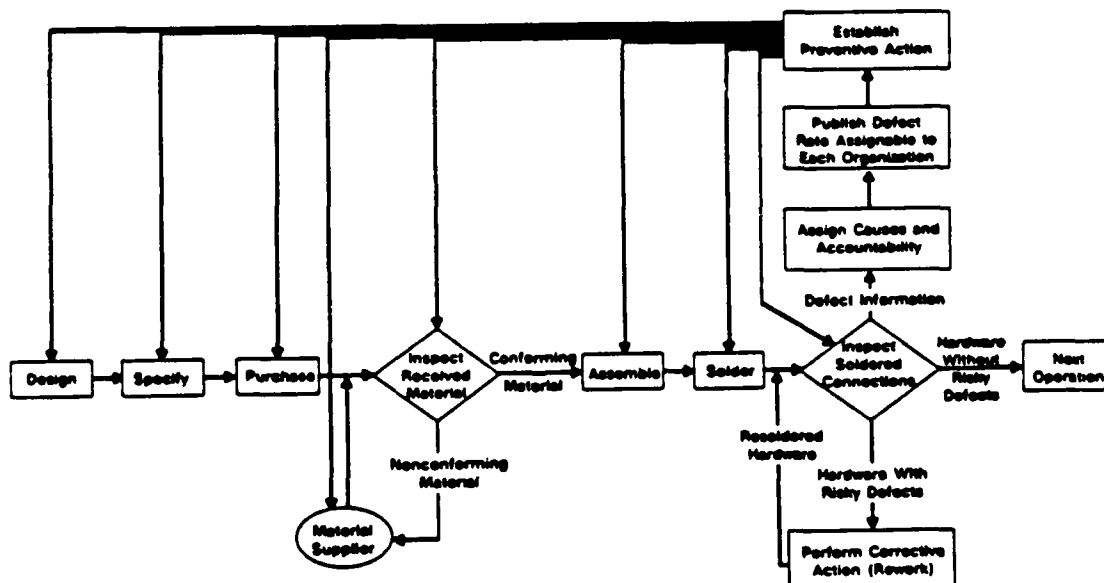


FIGURE 2 - CLOSED-LOOP SOLDERING

Is Inspection A Process?

For a process to be developed and controlled, one must be able to identify the effects of changes in the materials and process. For soldering, these effects are anomalies in the solder connection found by visual inspection. We can call these "defects" for the moment, although later it will be seen that there is more to this term than is usually recognized.

The defect rate data must be accurate and reproducible. It is curious that while many people doubt the accuracy and reproducibility of inspection, dismissing it as "subjective" and searching earnestly for a machine to replace the inspector, soldering processes continue to be established based on the inspector's data. If the data are suspect, it would seem more logical to fix arbitrarily the soldering process variables until after the inspection process was controlled.

If inspection is regarded as a process, then ordinary process-development efforts can be made to improve it². The visual inspection process is shown schematically in Figure 3, and a proposal for its development is shown in Appendix II. For this process, the measure is the disagreement rate. The disagreement rate can be reduced by ensuring that each discrepancy is understood (this is the topic of Part II), and that in turn comes from understanding the soldering process. Thus improvements in either process help in improving the other.

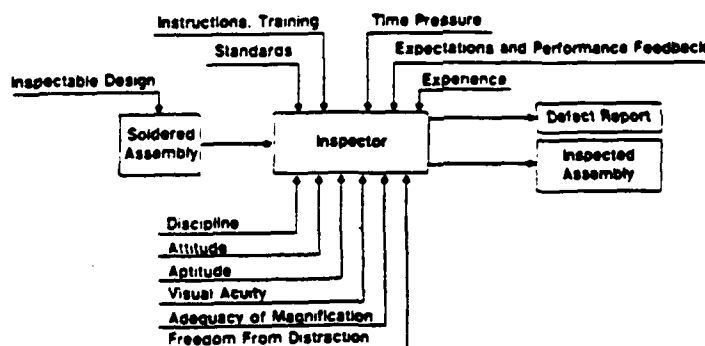


FIGURE 3 - THE VISUAL INSPECTION PROCESS

THE PURPOSES OF DEFECT INSPECTION

Soldering standards have for many years required that all solder connections be visually inspected, and any defects reworked. Now the Department of Defense has expressed concern that all this inspection is "neither effective more efficient". Proposals for process control are being sought as an alternative³.

The place to begin is with the clearest possible description of the problem. Until a problem can be stated clearly, it is unlikely that the answer will be found. Why have the standards required one hundred percent visual inspection? Since inspection does not add value to the product, why do it at all?

Significantly, the standards themselves do not provide a clear answer. However, if inspection is so important, then it is surely important to understand the intent. Otherwise, it would be possible to slavishly conform to the letter of the law and miss the spirit.

History

Before machine soldering, all soldering was done by hand, and operators needed a guide to distinguish good soldering from bad. Terms such as "cold joint" were given to connections that had been made improperly; it was hoped that people would be able to figure out the cause of the problem (joint didn't get hot enough) so in future soldering they would avoid the mistake (process deficiency) that produced it. Material deficiencies were scarcely addressed.

When machines became available, they soldered assemblies so much faster than people could that they were quickly adopted, even though not all the connections were "good" (looked like what the hand soldering operator aimed for). Inspecting for these "defects" and reworking them ("touch-up") still cost much less than hand soldering, and so there was no major objection to doing this⁴.

A new soldering process was being used, but the old list of defects, including "cold joint" remained, even though a cold joint by machine soldering was impossible (the solder was, after all, liquid). Now the problem of preventing solder defects was more difficult. If hundreds of connections are made within a few seconds by a process that had to have been virtually the same for all of them, but some of them ended up looking bad, how to determine what had gone wrong? Perhaps it was just random occurrences?

In any case, the requirement was clear: they needed to be made to look like the rest and so they were. The reason given for why they had to be made to look like the rest, whenever the question was raised, was to ensure the reliability of the connection. This answer, however, appealed to intuition, not data, because few data were available. Certainly it is not easy to determine whether or not a connection that looks different in some way is any less reliable than one that looks normal.

Solder connections in the 1960's and early 1970's were not very reliable. Cracks in the solder and in the copper barrel plating occurred, as revealed by failure reports and recollections today of older engineers. What seems not to have been recognized clearly is that the failures were almost entirely due to inadequate design (no stress relief) or lack of material control (poor solderability, brittle copper plating, co-deposited organics), not inadequate soldering. Had this been recognized, then presumably more of the emphasis in the standards and elsewhere would have been on design reviews and receiving inspection and less on solder defect inspection and rework, i.e. there would have been a clearer focus on prevention instead of detection and correction.

In the mid-1970's the Army commissioned a study of the reliability of solder connections by Lockheed Electronics⁵. Both field failures and environmental stress screening of "good" and "bad" solder connections were reviewed. Predominant in the stress screening studies was work by Joe Keller, then at Martin Marietta in Orlando. Keller was particularly interested in whether it made sense to require that plated-through holes be filled with solder.

While the Army/Lockheed report is long, the findings relevant to this discussion were that connections between leads and plated-through holes did not have to be very good by prevailing visual inspection standards to be as reliable as, or even more reliable than, connections judged to be acceptable. Only two causes of premature failure were found:

- Less than 55 percent of the area of land and lead on the solder side showed good wetting.
- Plated-through holes were less than 25 percent filled with solder.

All other visible "defects" studied were found to be unrelated to reliability!

The results of the Army/Lockheed study, through carefully researched and documented, seem to have been completely ignored. The findings were not challenged, at least not in print, but neither have they ever been accepted, even by the Army for its own soldering standard.

It may be that much less severe defects are still required to be reworked (e.g. holes in through-hole assemblies must be full of solder) because of a concern for process control. It isn't enough that the connections be reliable. They have to have been produced by a controlled process, or else made to look as if they had. In this line of reasoning, if the standard were relaxed, then perhaps so would be the contractor's efforts to control the soldering process, and the defect rate on machine-soldered assemblies would drift upward. But if people must be paid to find and fill the holes that didn't fill on the machine, wouldn't this provide incentive for ensuring proper machine operation? If hasn't quite worked out that way, and prevention by solving the problems not related to process has not been as common as it might have been.

Two Reasons for Inspection

Whether the above speculation is true or not, this much certainly is: There are two reasons for inspection of the product²:

- 1) ensure product integrity
- 2) identify design problems, and provide information for material and process control

The problem with visual inspection of solder connections is that these two reasons have not been distinguished clearly enough, so that the task has been conducted in a way that attempts to combine them, with uncertain guidance provided to the person assigned to do it.

It is this lack of clarity, and not the need for human judgment, that explains the repeated charges of "subjectivity". It also explains the inconsistency of on the one hand requiring inspectors to have good visual acuity, and providing the visual quality standards at magnification factors of 30X and up, and on the other hand restricting the magnification power of the optics used to 10X. If one isn't sure which features are important and which are not, then any irregularity at all may cause rejection, particularly if the decisions are subject to review. Therefore, if inspection and soldering are not understood, magnification must be limited to prevent small features from being seen.

Until the two reasons for inspection are more widely understood, the subjectivity of inspection will remain, even if it is performed by a machine, because there cannot be a clear statement of what it is expected to accomplish. On the other hand, if the two reasons are understood, then it can be performed effectively by people. At last, they can be told what to look for, and how to respond, in a way that involves the mind.

The inspection for risky defects covers all the connections, but is fast because the list is short, they are easy to find, and there aren't many of them. The inspection for material and process deficiencies need only be applied to a small sample (just enough to get a reasonably good figure for the rates of the various defect categories). Even though the defect list is longer, and it takes more time per connection to assign probable causes, it still doesn't take very long. As soon as no new defect types are being found for a given batch of assemblies, this inspection is complete.

Is it a worthy goal to eliminate inspection of the product (i.e. to run open loop)? Yes and no! Yes, it should be a goal to reduce the rate of risky defects to the point where they are real rarities (Philip Crosby talks about defects being so rare that when one is found, people come from all around just to look at it⁶.) When this happy state has prevailed for some time, the hundred percent search can cease. No, periodic audits should be an accepted part of any enterprise. The product is, after all, the reason for the process, and it is only right to check it from time to time. Besides, the product provides information about design, materials and process that can be obtained in no other way. Finally, as the sampling frequency drops, so does the economic benefit of decreasing it further. Product auditing remains as an appropriate part of the cost of quality.

Stimulus and Response: Choosing action appropriate to the defect.

In a previous paper on inspection² the meaning of the word "defect" was discussed at length. This word, like the word "quality", is one for which everyone has an intuitive grasp, but when a rigorous definition is attempted, it proves elusive. The discussion in the section above provides what is needed. Just as inspection has two purposes, "defect" has two meanings, one related to product, the other to design, materials, and process.

The product has a short list of major requirements. MIL-STD-1520 defines these by requiring that the hardware:

- not be dangerous
- perform the way it was intended
- be interchangeable, reliable, and maintainable
- in some instances, weight and appearance may be a factor.

Also, the product must be inspectable for its compliance with those reliability requirements for which inspection is the most practical means of verification.

The product-related (risky) defect definition is a nonconformance to the major requirement of reliability. The design-, materials-, and process-related (indicator) defect definition is any significant departure from the normal and expected.

Since there are two definitions and two kinds of defects, it should seem clear that there are two responses:

- 1) Rework of risky defects (only). This is appropriately called corrective action.
- 2) Identification and elimination of the causes of indicator defects. This is appropriately called preventive action.

If the two reasons were more clearly recognized in the standards, then the required response to any particular defect would be based on whether product integrity was at stake (i.e. whether the defect was risky). Rework is itself risky; it should seem clear that risking damage to an assembly to remove a condition that is not risky is an inappropriate response to the stimulus. Rework destroys the evidence of lack of control. Instead of motivating control, permission to destroy the evidence can actually reduce the incentive to prevent future defects.

SUMMARY OF PART I

The soldering process can be understood; the method selected for process development and control is based on being able to identify the causes of defects that are seen. Those defects may be caused by deficiencies in the design or the materials rather than the process, and many of those cannot be compensated for by any change in the process. "Closing the loop" really means determining causes, identifying the responsible organization (Design, Purchasing, Receiving Inspection, Assembly, Soldering) and having all of these organizations respond by eliminating the causes. This means preventive action.

Visual inspection is itself a process; the inspection process yield or inspection defect rate can be measured, and improvements can be made. The so-called subjectivity of visual inspection disappears when it is understood that there are two reasons for inspection, two classes of defects, and two responses to defects. Since many risky defects are the result of deficiencies in design or materials rather than process, reworking them by "touch up" does not correct their causes. Indicator defects are not risky; reworking them is an inappropriate response and destroys the evidence. One hundred percent inspection is needed for risky defects only, and can be eliminated when such defects disappear. Sample or auditing inspection is sufficient for indicator defects; when design, materials, and process are controlled, this inspection does not take long because the defect rate is so low. Guidance for determining causes is given in Part II.

PART II - SOLDERING AND RELIABILITY

WETTING

The function of solder is to conduct electricity between, and to bond mechanically, metal members of the connection (component termination and board land). These metals, which do not melt during soldering, are called basis metals. In electronics the most common basis metals are copper, nickel, and an alloy of iron and nickel called Alloy 42. As long as at least a little solder is present, the strength and reliability of the connection depends mainly on how well the solder sticks to the basis metals, that is, how well it wets them⁵.

Inspection for Wetting

It is sometimes claimed that solder connections can best be judged by cross sections or X-ray imaging. While these methods have their uses, the only additional information about the adequacy of a solder connection they provide is whether hidden voids are present. Since that condition for a CCA can be inferred from the presence of visible holes in the solder of nearby connections⁷, that isn't much of a benefit. (X-ray imaging is, however, the only inspection method available for connections and solder balls that are hidden.) The quality or degree of wetting on a component termination or a PWB test area can be measured with a wetting balance, and this fact is exploited for solderability testing, but the way to judge the wetting of solder in a connection is to look at it. Since wetting is the most important physical attribute of the solder in a connection, the most important visual attribute is the one that reveals wetting quality: the contour⁸ (see Table I).

TABLE I - VISUAL ATTRIBUTES OF THE SOLDER FILLET

<u>Attribute</u>	<u>Ideal</u>	<u>Reliability of connection with nonideal attribute</u>
Contour (shape)	Concave	Convex reveals poor wetting (see text for exceptions)
Texture	Smooth	Unsmooth due to conditions during freezing - not risky
Luster	Shiny	Unshiny only at low magnification - not risky

Look for the angles of contact between the solder and the surfaces of the basis metals in the connection. If the contact angle is small, the nearby fillet shape is concave (curved away from you), and this indicates good wetting. If the contact angle is large, the nearby fillet shape is convex (curved toward you), and this (except as discussed below) indicates poor wetting. The poorer the wetting the less the strength and the greater the risk that the connection will fail in service (results: an intermittent open circuit). It is neither practical nor necessary to measure contact angles on a soldered assembly: connections with poor wetting look very different than those with good wetting.

There are two situations for which the appearance of the fillet requires extra interpretation. For through-hole connections, since solder is supplied from one side (the underside for machine soldering), poor wetting causes a second visual attribute: less solder in the connection when viewed from the destination (component) side. Depending on which cause (see below), the poor wetting may be at the top of the fillet only (low risk) or throughout the connection (high risk). For machine soldering, a convex fillet on the supply side does not imply poor wetting, but rather a combination of good wetting and an inadequate opportunity for the solder to drain away.

The other situation is for reflowed connections. Here, the volume of solder is fixed before soldering, so it is unrelated to wetting. Above a certain volume, the fillet will be convex because there is nowhere for the solder to go. The wetting for that connection can't be judged. However, nearby connections with less solder allow one to infer with reasonable confidence the wetting quality of a connection with an extra-large convex fillet.

What are the factors that determine whether solder will wet a connection? Assuming that solder and flux are available, there are only two: heat transfer (design and process), and solderability (materials).

1. The metal surface must at least be hot enough so the solder doesn't freeze when it comes in contact with it, because for there to be wetting there must be something wet (i.e. liquid). If the solder and the surface are hotter than the solder melting temperature, then the wetting can occur faster.
2. Since metals (solder as well as basis metals) react with oxygen to form oxides (oxidize), and since solder doesn't wet oxides, any existing oxide must be removed, and competition of oxidizing with wetting must be prevented. These are the functions of flux: remove oxides and prevent oxidation. Basis metals differ in the ease of solder wetting by how hard it is for flux to remove the oxide.

While there are many implications of these two factors, it is important to see the underlying simplicity, because then, regardless of the details, one can relate wetting back to the basics: adequate heating and adequate contact of solder to bare basis metal.

Heat Transfer

Many of the soldering requirements have been in the standards for a long time. Some of these need to be reconsidered because the product has changed dramatically in its heat transfer characteristics.

When a circuit card assembly of modern design is compared to an old design, the difference in component density is immediately obvious. Components are much closer together and there are many more of them. What is not as obvious is that the PWB is also much denser. While an old board may have circuitry on both sides, modern boards have many internal layers too. The result of the increase in board density is an increase in heat capacity, or as engineers often refer to it, thermal mass. Heat capacity is a measure of how much heat must be supplied to produce a given increase in temperature. The importance of heat capacity for soldering is factor number one for wetting: the metal surface must rise above the melting (liquidus) temperature of solder. Hence, modern CCA's are harder to solder because it is harder to get them hot enough. "Harder" really means "takes longer", because there is a limit on how fast heat can be supplied to a board without scorching it.

Preheat. While one often reads or hears three reasons for preheat (activate the flux, evaporate the flux solvent, and prevent thermal shock to the board), the real reason is none of these. It is to get the lands on the board hot enough so that combined with the additional heat supplied during soldering the solder has a chance to form an equilibrium fillet shape before it freezes⁹.

For reflow soldering, preheat can be used for three subsidiary functions. Preheating a CCA to just below the solder solidus temperature minimizes temperature differences, and the time needed, in the reflow zone. Also if the volatile constituents of solder paste have not been removed previously, this can be done in the solder machine. Finally, if (as has been common) a low-boiling solvent fluid is used to provide a secondary vapor blanket for vapor-phase soldering, then heating the CCA above the fluid's boiling temperature before it enters this zone will prevent vapor condensation. Condensed solvent can rinse away the flux prematurely.

For through-hole machine soldering, discussions of preheat have not until recently emphasized the most important temperature to monitor and control: the temperature of the coolest land on the component side as the CCA exits the solder¹⁰. It is not easy to find even a highly automated solder machine that so much as monitors this most important variable, let alone uses it to control the process.

While for any given CCA style it is useful to monitor the component-side temperature during preheat, this is not as important as the temperature reached during soldering. Some soldering standards set a limit on preheat temperature for wave (or drag) soldering. It seems to have been overlooked that if the same assembly were to be reflow soldered, there would be no such prohibition! If it is not necessary to set a preheat limit below the soldering temperature for reflow soldering, then there appears to be no reason for setting a preheat limit lower than this for wave soldering either. The bare board is, after all, required to be able to survive a ten-second float on very hot solder (290°C, 550°F) with no preheat! It should be clear that limiting the preheat temperature only increases the amount of heat the board must receive from the solder. While both sides of a CCA can be preheated, the solder can heat the component side only by conduction through the board. The CCA's with high heat capacity, this is not only less efficient and less uniform, but increases the risk of heat damage to the solder side.

In wave soldering, the trailing edge of the board gets hotter than the leading edge¹⁰, and the edges get hotter than the center, due to heat transfer in the plane of the board. Therefore the place to measure land temperature is near the middle at the leading edge. In drag and reflow soldering, the influence of in-plane heat transfer is to make the center of the board the slowest to heat (apart the local influence of high-heat-capacity components).

Design. There are three ways that the design of a high-density through-hole CCA can increase the producibility by assisting heat transfer. Components incapable of withstanding intense topside preheating should be avoided, pads and lands should restrict heat loss to power and ground planes¹¹, and the correct difference (not ratio!) between diameters of hole and lead should be picked.

Part of the heat reaching the component side of a through-hole CCA is carried by the solder itself. If a lead is in a hole only a few thousandths of an inch larger, there isn't much room, and the solder can't carry much heat. Offsetting this factor is the additional capillary force at work in small spaces, so there is a best range for the difference between the diameters of hole and lead for fast fillet formation. (Of course, a small space also makes it hard to insert component leads and a large hole reduces circuit density.)

Freezing. There have been many discussions about whether the soldering standard should require that the solder be "bright and shiny", "smooth and bright", smooth and lustrous", etc. Actually, except for high levels of contamination (e.g. from gold plating), the texture and luster of the solder in a connection indicate freezing speed, not reliability.

Quickly frozen solder, in the presence of adequate flux to prevent oxidation, has a smooth texture and a bright, shiny luster. Slowly frozen solder, in a fillet or in a solder pot, looks different. In a fillet, the surface is bumpy (from projections of lead dendrites) and may have a grid of slight depressions (the trace of the last solder to freeze)¹². The resulting bumped or gridded appearance is often termed "grainy". The latter surface appearance is sometimes called "crystalline", although of course solid solder is always crystalline. With adequate magnification one can see that the solder really is still shiny. The connection is almost as strong as a quickly frozen one.

CCA's with high heat capacity not only take longer to heat - they take longer for the solder to freeze. If smoothness and shininess were inherently important instead of indicators of freezing speed, then forced cooling of the connections should be required for the purpose of producing the desired result (along with a slight, though temporary, increase in strength). Inexplicably, until 1989 U.S. soldering standards prohibited forced cooling. MIL-STD-2000 now allows "controlled cooling".

Solderability

While various definitions of solderability can be found, some fail to address rate of wetting, and most do not distinguish between the contributions of heat transfer and the condition of the surface, although it is the latter that is nearly always intended. For any specimen (component termination, board land or hole), its solderability can be thought of as the rate and degree of wetting with solder, under specified conditions, compared to the ideal. Ideal solderability for a specimen is good wetting at a rate established by heat transfer alone.

The definitions also do not usually distinguish between solderability for a single specimen and for an entire population. The distinction is important because unlike material properties such as density or resistivity, solderability is strongly influenced by the test conditions and specimen history. The solderability for a population of nominally identical pieces may have a significant range in value. Since the solderability of the population is judged from the results of tests on only a sample, a test that mimics production soldering conditions could fail to predict problems. The solderability test method needs to provide a safety margin, or guard band, between what is used for measurement of the sample and what will be needed to wet the worst piece in the population.

When the solderability of a sample is tested, the guard band is provided two ways:

- 1) The test temperature is lower than that typically used for machine soldering. For component leads, 245°C (475°F) is used in U.S. tests such as Method 208 of MIL-STD-202, and 235°C is specified in standards elsewhere. For PWB's, IPC-S-804 uses 245°C, MIL-P-55110 uses 260°C.
- 2) The flux for the test is weaker than that typically used for machine soldering. Type R flux (rosin without activator) is now specified in solderability test methods worldwide. To ensure that the test results are reproducible, the solids content of the flux needs to be specified (IPC uses 25 percent).

There are two ways to measure solderability: judge the degree of wetting after a specified time in solder, or measure the time to reach a specified degree of wetting. Table II summarizes the criteria for these tests.

TABLE II - SOLDERABILITY TEST CRITERIA

Test Type	Criterion	
	Component Leads and PWB Lands	PWB Holes
Degree of wetting after specified time	95% solder coverage after immersion in solder bath. Leads: 5 sec (large terminations 7 sec); PWB's: 3 sec. "Dip and look" test.	Fraction of holes filled (or wet) after PWB is floated on solder bath 10 sec.
Time to reach specified degree of wetting	Wetting force (as measured by wetting balance): zero force, 2/3 maximum force, 1/2 or 3/4 of maximum theoretical force have all been proposed. Rotary dip test measures minimum time in solder for good wetting.	Filling of hole by a solder globule beneath.

Difficulties with the solderability tests. For components which are to be reflow soldered, the typical machine soldering temperature is less than the test temperature. Two responses to this loss of guard band are being considered:

- 1) No change, because typical reflow soldering times are so much longer than the solderability test time that it more than compensates for the lower temperature.
- 2) Dropping the test temperature (say to 205°C) with an increase in time.

If production soldering is done with a flux of low solids content, use of 25 percent flux for the test may also mean a loss of guard band. There are not yet any plans to reduce flux solids content for solderability testing.

Solderability tests normally do not provide preheat. However, without preheat or else hotter solder, filling some of the holes in boards with high heat capacity may be slow or even impossible, regardless of solderability.

The wetting balance test gives the most information, but it has not been widely used long enough for it to become standardized or referenced in procurement documents. For PWB's, heat transfer effects have been addressed by a proposal that the permissible wetting time increase with board thickness¹³. So far there have been no proposals for adjusting permissible wetting times for heat transfer effects for component terminations (although the military standard dip-and-look test method does provide for a longer immersion time for large terminations).

The solder globule test for plated-through holes must be performed one hole at a time, with enough holes measured to develop valid statistics; if it is desired to use the board for assembly after it is tested, the solder plugs must be removed.

There are subtleties in the dip-and-look test for component leads that have led to correlation problems between vendor and customer¹⁴. The EIA, IPC, and military component solderability test methods are all being revised to make the test conditions (and results) consistent.

Tests for leadless components (chip carriers and passive chips) are only now being introduced into the component solderability test methods.

The pass-fail criteria in the IPC solderability test for PWB's (which are also invoked by MIL-P-55110D) need clarification, and may not provide a guard band for assembly soldering.

Validation of the solderability tests, i.e. demonstrating a correlation between results of the test and results after assembly soldering, is difficult in part because of the common lack of accuracy in solder defect inspection that was discussed in Part I of this paper. As discussed under dewetting, the dip and look test may not correlate well even with good inspection.

Finish. Most explanations of solder wetting are written for bare basis metals. For assembly soldering, it is quite common for the copper lands and hole walls on PWB's to be covered with solder or electroplated tin-lead, and component lead basis metals are nearly always covered with a coating: solder, electroplated tin or tin-lead, and sometimes gold. The purpose of these coatings (finishes) is to help ensure that wetting will occur, by preventing oxidation of the basis metal. Properly applied finishes produce ideal solderability by prewetting the basis metal surface. Tin or tin-lead plating, properly applied, provides an interface comparable to that obtained by molten solder.

However, use of a finish introduces new problems: problems with the plated material and problems with the electroplating process. The problem with tin is the same property that makes it such a good solder: it reacts with nearly all basis metals. The result is not only wetting, but formation of intermetallic compounds. These compounds, though composed entirely of metal atoms, are not alloys but have fixed stoichiometric composition. They are not shiny like metals, and most are brittle. It is as if they were nonmetals. The intermetallic compound does not itself cause a solderability problem, however, as long as it remains covered with tin or solder.

The problem with gold is that it reacts so quickly with the tin in solder; the resulting large amount of intermetallic compound, being brittle, renders the connection vulnerable to fracture. This is particularly true for small connections because the gold-to-solder ratio is higher. Gold is the only common cause of nonideal solder texture that implies risk to the connection.

The problem with electroplating is that the process is much more likely to get out of control than is solder dipping. The thickness may be insufficient for good shelf life. Also, it is possible to plate an oxidized basis metal. Such plating, instead of preventing oxidation, prevents fluxing and wetting.

The coating may be porous or contain organic inclusions. Bright acid tin plating has been found particularly prone to these problems. Inclusions are the remains of organic compounds that are added to the plating bath to make it work better. The worst inclusions are those which do not reveal their presence by any visual cue but cause loss of adhesion and fracture by migrating to the interface between basis metal and solder¹⁵. This failure may not occur until months after the connection is made, as "infant mortality". The presence of organics in the connection is a materials problem for which there is no process cure, and no sure inspection method to detect. Fortunately, as for all other defects, it can be prevented.

The role of the finish in protecting the basis metal below is analogous to a raincoat's function of keeping its wearer dry. If the raincoat has holes in it, it is worse than no raincoat, because it must be removed for the wearer to dry off. A porous gold coating, instead of protecting, actually promotes galvanic corrosion of the basis metal in a moist environment. A porous tin-containing finish allows easy access of oxygen and water vapor to the intermetallic compound. It now appears that this is the mechanism for loss of solderability. Because the oxidized compound in a porous coating is below the surface, the remaining finish prevents effective removal, no matter how strong the flux. It is also possible that once the compound reaches the surface, it provides an entry path for oxidation to proceed below.

Dewetting. This term has been used to refer to the appearance of solder on a basis metal when the sample is removed from the solder. Upon removal, the solder accumulates in irregularly shaped mounds with large contact angle; the area between the mounds is covered with a thin layer of solder. It is discussed extensively by Klein Wassink¹⁶. Dewetting can vary in severity; the term has also been used to refer to more than one phenomenon. For example, the failure of solder to wet an oxidized ("passivated") basis metal that has been covered by a plated finish has also been referred to as dewetting, but would better be referred to as delayed nonwetting: the finish is first wet by the solder but as the finish melts or dissolves into the solder, nonwetting begins.

The dip-and-look solderability test method has never required distinguishing between nonwetting and dewetting, and for some purposes, such a distinction may be unneeded. However, if the purpose of the test is to predict whether, for a particular batch of parts, rework of solder connections on an assembly will be needed, then the distinction is important.

If the solderability test shows slow or incomplete wetting, then the assembly fillets will probably prove defective. However, leads with major dewetting have, after assembly and wave soldering, had ordinary looking fillets. The reason for the difference is that for the assembly, there is nothing equivalent to the removal of the lead from solder in the test, and since dewetting doesn't begin until removal from solder, it doesn't ever begin. The assertion that lead dewetting need not result in assembly solder defects may or may not seem obvious; it is a recent discovery for the author. The accuracy of the assertion can be tested easily by experiment.

Composition and purity

In the discussion of wetting, nothing has been said about the influence of solder composition or purity. Nearly all of the solder used for electronic soldering is tin-lead solder, and nearly all of that is eutectic (63 percent tin by weight) or near-eutectic (60 percent tin). Eutectic means that melting of the alloy occurs at a fixed temperature and not over a temperature range. It does not mean that melting (or freezing) occurs instantaneously. For a given volume, the time required depends on the heat of fusion of the solder and the ease of heat transfer. It is the tin in the solder that does the wetting. Lead lowers the melting temperature below that of pure tin but otherwise just goes along for the ride.

As for solder purity, there have been several studies of the effects of metallic elements and two nonmetals in solder¹⁷. (Most nonmetals, including solder fluxes, neither dissolve nor become suspended in solder and so can't contaminate it.) The effects, which depend on the concentration of the element are, in the order of occurrence with increasing concentration:

- 1) a deterioration in the appearance of the solid solder, in the pot and on the basis metal, from the normal smooth or semi-smooth to gritty. (The "grit" is suspended particles of intermetallic compounds, their oxides, and tin oxide.)
- 2) an increase in the time to wet, presumably due to the sluggishness of liquid flow.
- 3) an increase or decrease in the strength of the solder connection, due to the inclusion of the particles in the metal matrix.

For hand and reflow soldering, purity of the starting material is not an issue since fresh solder is used. For wave and drag soldering, where there is a reservoir, the most important thing to know about impurities in solder is that unless creep is expected to be a problem the first effect is, with one known exception, visual: the surface texture of the solder connection changes at an impurity concentration below that for which the more important effects are observed¹⁸. (The one exception is gallium. This uncommon metal, which melts at room temperature, never gets into solder unintentionally.)

If the solder is smooth, one can be sure it is pure enough, although soldering standards require that the solder be chemically analyzed periodically anyway. If the solder isn't smooth, one can't conclude that it's because of an impure solder supply. In addition to the formation of intermetallic compound by reaction with gold plating, and the bumps and grids that form with slow cooling, the surface may have wrinkles, sometimes referred to as "quilting". Wrinkles are due to formation of an oxide skin on the molten solder because of loss of flux protection; the wrinkling occurs during freezing shrinkage of the solder.

Of all the things to be concerned about in soldering, measuring solder purity is the least important, both because (unless bare copper boards are being soldered) impurity limits in soldering machine reservoirs are rarely exceeded, and because the surface texture provides a warning before the product is at risk.

DESIGN, MATERIALS, AND PROCESS
FOR OTHER RELIABILITY ISSUES

Design: Mechanical compliance and residual stress

Design for producibility of CCA's was mentioned in the discussion of heat transfer's role in wetting. While this need can be met in straightforward ways, there are design issues relating to reliability that are more complex. For a connection with good wetting, the minimum solder volume that is necessary for it to be reliable depends on the design and the service environment.

The reason why plated-through-hole connections don't require much solder is that their design is conservative, with a large safety factor. On the other hand, some assembly designs are inherently unreliable - there is no volume of solder great enough to prevent early fracture. The extreme example is a large leadless ceramic chip carrier on a conventional epoxy-glass board, with anticipated large and frequent temperature changes. The strains resulting from expansion mismatch will cause early fracture of the corner connections, regardless of the solder alloy. If a very strong (strain-resistant) attachment medium were found, then some other part of the connection (the land or the termination) would have to give¹⁹.

This is one example of how failure to design enough stress relief into a connection can result in fracture. Even for leaded components, the mounting can be improperly designed (or executed) so that there isn't enough opportunity for mechanical compliance (flexibility). This, rather than solder defects, is probably the biggest cause of field failure of solder connections.

The NASA soldering standard²⁰ provides some insight:

Reliable soldered joints require proper design. Particular attention must be given to stress relief, solder reinforcement when stress relief is not possible, material selection, and inspectability...

The most frequent problem encountered in maintaining a reliable soldered connection is the solder cracking phenomenon. This condition often occurs on perfectly soldered interconnections which pass all inspection criteria and initially function normally. Solder cracking and failure may occur within weeks or even years after installation and operation in the intended use.

Solder-copper separation is another problem that has caused failures on NASA hardware. It has a failure mechanism entirely different from solder cracking. Both failure mechanisms are evasive and time-temperature dependent... When solder fatigue or creep is present, a solder connection will ultimately crack with a small load that is only a fraction of that required to reach its nominal ultimate strength.

Since the cause of these defects is not the process, remelting the connection is at best a temporary fix.

Another important cause of field fracture is residual stress in a surface-mount gull-wing lead²¹. This occurs if:

- 1) when the package is placed, the foot sits above the land, and
- 2) the foot is held down on the land during solder reflow and freezing by a tool or heater bar.

The solder in the resulting connection is in tension, with a stress on the order of tens of pounds per square inch.

The yield strength of solder in tension is only a few hundred pounds per square inch, and this value drops with increasing temperature. The stress level, at a few percent of the yield strength, is not high enough to cause immediate failure; fracture due to creep may occur weeks or years after the connection is made.

Unlike the defect conditions of poor wetting, inadequate solder volume, and insufficient stress relief, there is no inspection method, visual or instrumental, that can detect whether solder is in tension. The only clue is the mark left on the top of the foot by the hold-down tool. This defect has been shown to cause field failures of solder connections, yet except for the NASA standard²², most discussions have not adequately emphasized it.

Materials: Resistance to soldering heat

Printed wiring boards are subject to three materials problems besides lack of solderability that show up after soldering. All can be revealed by a solder float test, but unlike the float used for assessing solderability, the guard band is provided by hotter solder and longer exposure than that used in production soldering. The test will reveal:

Holes in the solder plugs of plated-through holes. These are caused by hydrated copper salts in cavities behind the copper barrel. The cavities are caused by rough drilling²³ and the salts are trapped during electroplating. The soldering heat drives off the water of hydration. This can be demonstrated by holding a crystal of copper sulfate with forceps in molten solder. Given the Army/Lockheed findings on the reliability of incompletely-filled through-hole connections, this defect seems unlikely to be risky unless the hole is very large, in which case many of the connections will exhibit the condition.

It has been suggested that incompletely filled holes are risky because they can trap contaminants that may later get out onto the board and cause corrosion. It is not known whether this has ever occurred, but this mechanism seems unlikely if the assembly is conformally coated.

Improperly formulated or cured resin or solder mask. This condition is revealed by the adhesion of solder.

Delamination or measling. This condition is due to deficient adhesion of the resin to the fiber reinforcement. Minor deficiencies can be compensated for by oven drying; it is the forceful evolution of dissolved water as vapor that causes the separation. The tendency to measle seems not to be revealed by the solder float test as well as by simulated hand soldering. This difference may be because of the less uniform heating or possibly the higher tip temperature. Measling has never been known to cause a CCA failure²⁴, but a gap that bridges two conductors provides an opportunity for moisture condensation and a resultant leakage current path. This mechanism is well established for unprotected integrated circuits²⁵.

There is no provision in the military specification for printed wiring boards for rejecting because of holes in solder, solder adhesion, or measling during simulated hand soldering; these requirements can however be added by a company to its own procurement specification.

Components. Components may also be tested for resistance to soldering heat. The component category most likely to have a problem here is ironically the one subjected to the greatest stress: the passive chip (capacitor or resistor), since it is often soldered by iron or by direct immersion. Chip capacitor manufacturers have been specifying preheating very slowly until the temperature is close to the that of molten solder, to prevent cracks from thermal shock. The problem is not simply a matter of different expansion coefficients, as some company's capacitors are much more resistant to cracks than others²⁶.

Radial or standup capacitors are often the tallest component of an assembly, so designers like to mount them as close to the board as they can. The capacitor manufacturers, however, exempt the first fifty thousandths of an inch from solderability requirements because they don't want to overheat the device by immersion all the way to the body.

Glass-sealed ceramic packages (cerdips, cerpacks, cerquads) are at risk of cracked seals if the leads are immersed into solder all the way to the body, unless they are preheated. This risk is not due to failure to match expansion coefficients but rather to the difference in thermal conductances between the metal lead and the glass. The glass cannot heat as quickly as the lead. Seal glasses vary in their ability to withstand the shock, but failing to preheat any glass-sealed package before immersing the leads in solder is unwise. It is abuse²⁷. Preheating components before solder dipping is not, however, required by soldering standards.

Process: Drainage and oxidation of the through-hole connection

When a knife is pulled out of honey, the amount that comes along with the knife depends on how fast it is pulled out. The explanation is simply that while honey is nominally liquid, it is viscous and it takes time for this liquid to "seek its own level". Solder, though nowhere as viscous, does take some time to flow. If the lead protrusion separates from the solder bath or wave above a limiting speed, then assuming there is good wetting, extra solder will remain on the connection. (With poor wetting, extra solder is not to be expected, because there is a lack of force to pull it away from the bath or wave.)

The shape assumed by this extra solder depends on whether flux is available to prevent forming an oxide skin. If there is, then the fillet may be convex, and it may even bridge to a nearby connection, but it won't be pointed. Solder points ("icicles") extending from the solder side form as the connection to the bath or wave is broken. In the absence of flux, the solder oxidizes, as previously discussed. The resulting oxide skin is strong enough to resist the liquid's tendency to reduce its surface area; this would cause wrinkling of the skin. The oxide skin protects bridges and icicles as they form. As mentioned, shrinkage of the solder during freezing does wrinkle the oxide skin.

Simple experiments can be performed to show the effects of withdrawal speed and flux, using a prewet wire with a small hook at the end. With a fast withdrawal the flux may not get a chance to flow and cover the growing solder surface, and an icicle will be produced. Also, if the wire is not fluxed or it stays in the flowing solder long enough for the flux to wash away, a fast withdrawal is not needed to form an icicle. The reason for the icicle shape is not that the solder freezes before the liquid can change its shape, as can be confirmed by pushing it promptly after it forms. If the experiment is repeated in a nitrogen glove box, one finds that flux is not needed, and that while extra solder can be pulled out, an icicle cannot be produced.

On a wave solder machine with oil intermix, it is difficult to pull out extra solder because the oil reduces the effective viscosity. It also, like the flux, reduces the surface tension of the solder and prevents oxidation. Oil intermixed with solder sometimes results in partial or complete dropping of solder from large plated-through holes that have no lead or a small diameter lead. If too much oil is mixed with solder, it gets trapped in the solder plug or leaves a visible hole in the fillet. Oil inclusions do not reduce the reliability of the connection²⁸.

SUMMARY OF PART II

Solder wetting depends on heat transfer and the surface or interface properties of the basis metal being soldered. Wetting is judged by the surface contour: small contact angle and concave shape. Surface texture and luster are not useful guides to the reliability of the connection, but can be used to identify causes. Wetting is determined by just two basic factors: heat transfer and solderability. Heat transfer for modern CCA's is more difficult because of the much higher heat capacity. This makes preheat more important. Preheat supplements the heat provided by the soldering process itself to ensure that the coolest surface to be wetted rises above the solder melting temperature. Solderability is a material property that must be ascertained before assembly. Improvements in the tests used for this are needed. Solderability problems are due to deficiencies in the finish that is applied to the surface of basis metals for the purpose of preserving solderability. Boards and components also need to be characterized for their resistance to soldering heat. Available evidence suggests that most failures of solder connections are due to design, materials, or assembly problems, not soldering process deficiencies. Many of the failed connections did not even appear defective, and would not be detected even by a skilled inspector.

REFERENCES

1. Ralph W. Woodgate, "Charts, Taguchi, and the Wheel", Printed Circuit Assembly, 3 (1), 11-12 (January 1989).
2. J. Gordon Davy, "How Should CCA Solder Defect Inspection be Performed?", Proc. 1988 Nepcon-East pp. 451-165. Also in Printed Circuit Assembly 2, No. 9 pp. 20-24; No. 10 pp. 36-41; No. 11 pp 26-27 (Sept - Nov 1988).
3. S. J. Lorber, W. J. Willoughby, Jr., and E. J. Westcott, letter to heads of major DOD electronic manufacturing contractors, September 1987. Letter is summarized and discussed in Ref. 2.
4. Ralph W. Woodgate, Handbook of Machine Soldering, p. 4. New York: John Wiley and Sons, 1983.
5. R. Gangemi and P. Cipoletti, "The Dynamic Measurement and Functional Inspection of Solder Joints", Picatinny Arsenal Technical Report No. 5055, (December 1976). Available as AD-A034852 from National Technical Information Service, Springfield, Virginia.
6. Philip B. Crosby, Quality is Free, 1979. McGraw-Hill Book Company and Mentor-New American Library.
7. C. Lea and F. H. Howie, "Blowholing in PTH Solder Fillets - Part 1, Assessment of the Problem", Circuit World 12 (4), 14-19 (1986).
8. See for example Howard G. Manko, Solders and Soldering, Second Edition, p. 6. New York: McGraw-Hill Book Co., 1979.
9. Vern Smallwood, Westinghouse, private communication (1980).
10. Ben J. Cunningham, "The Return of Drag Soldering", Circuits Manufacturing 28 (12), M18-M22 (Dec. 1988).
11. MIL-STD-275E (31 Dec. 1984), Printed Wiring for Electronic Equipment, para. 5.2.5.
12. H. Steen, "Dendritic Patterns on Solder Joints on Printed Circuit Boards", Proc. Conf. on Soft Soldering and Welding in Electronics and Precision Mechanics, Munich, 1981, Deutscher Verband fur Schweisstechnik, pp 5-10.
13. John A. DeVore, "Solderability and Surface Mounting", Proc. 1988 Electronics Manufacturing Seminar, Naval Weapons Center, China Lake, CA, pp. 301-313.
14. Buford G. Slay, "Lessons Learned in Testing Solderability of Integrated Circuits Using Method 2003 of MIL-STD-883", Proc. 1987 Electronics Manufacturing Seminar, Naval Weapons Center, China Lake, CA (NWCTP 6789).
15. John A. DeVore, "Effect of Co-Deposited Organics in Plated Coatings on Electronic Hardware Reliability", Proc. 1981 Soldering Technology Seminar, Naval Weapons Center, China Lake, CA; Roger Wild, "Plating Effect on Component Solderability and Solder Joint Strengths", Proc. 1983 Soldering Technlogy Seminar, Naval Weapons Center, China Lake, CA.

16. R. J. Klein Wassink, Soldering in Electronics, pp. 36-44, 257-258. Ayr, Scotland: Electrochemical Publications, 1984.
17. See for example H.A.H. Steen and G. Becker, "The Effect of Impurity Elements on the Soldering Properties of Eutectic and Near-Eutectic Tin-Lead Solder", Brazing and Soldering No. 11, Autumn 1986, pp. 4-11 (18 Refs.).
18. G. Becker, "A Workshop Method to Detect Impurities in a Solder Bath", Proceedings, Conf. on Soft Soldering and Welding in Electronics and Precision Mechanics, Munich, Deutscher Verband fur Schweisstechnik, 71, 87-90 (1981). (In English).
19. See for example John H. Lau and Donald W. Rice, "Solder Joint Fatigue in Surface Mount Technology: State of the Art", Solid State Technology, Oct. 1988, pp. 91-104 (205 refs); W. Engelmaier, "Functional Cycles and Surface Mounting Attachment Reliability", Circuit World 11 (3), 61-67, 72 (1985) (47 refs).
20. NASA Requirements for Soldered Electrical Connections (NHB 5300.4 (3A-1), revalidated June 1986), Appendix C, "Solder Interconnect Problems on Printed Wiring Boards".
21. "Solder Joint Failure (Creep Failure)", General Document Summary Sheet F1-F-89-01, July 1989; available from Government-Industry Data Exchange Program, Naval Weapons Center, Corona, CA 91720.
22. Ref. 20, p. 15.
23. Howie, F. H. and Lea, C., "Blowholing in PTH Solder Fillets, Part 2: The Nature, Origin and Evolution of the Gas", Circuit World, 12 (4), 20-25 (1986).
24. ANSI/IPC-A-610 (Aug. 1983), Acceptability of Printed Board Assemblies, para. 8.1.
25. Aaron der Marderosian, "The Electrochemical Migration of Metals", Proc. 1977 Reliability Physics Symposium, pp 134-141.
26. Lori Clifton, "SMT Ceramic Capacitor Thermal Cracking Considerations in Rework", IPC Technical Review, 29, 19-22 (April-May 1988).
27. Kurt Kirsten, Motorola; Buf Slay, Texas Instruments, private communications.
28. Ref. 4, p. 101.

APPENDIX IA

CCA SOLDERING PROCESS DEVELOPMENT BY "CONTROLLED EXPERIMENT"

1. Select one soldering machine.
2. Identify machine variables (solder temperature, conveyor speed, etc.)
3. Collect a sample (of an adequate number of units) of a particular assembly design.
4. Solder one or more CCA's with a particular combination of machine variables (high temperature-low speed, low temperature-low speed, etc.)
5. Inspect the CCA's to find and count solder defects.
6. Use statistical methods to find that combination of machine variables correlated with the smallest number of defects.
7. Divide the smallest number of defects by the number of connections. This represents the "soldering process capability" for this design on this machine.
8. Record the results and solder CCA's of this design with the machine variables identified in Step 6.

APPENDIX IB

CCA SOLDERING PROCESS DEVELOPMENT BY DEFECT CAUSE DETERMINATION

1. Create reference standard solder defects on CCA's by deliberately causing them, (examples: poor lead wetting, insufficient time in solder) using methods suggested by the Probable Causes list of the Defect Standards table, Reference 5
2. Select a CCA soldered by a candidate "best" process (all known process variables specified).
3. Inspect the CCA for damage and for those solder connections that differ significantly from the rest.
4. For each connection found in Step 3, assign a defect category by comparing its appearance to the reference standard defects. Also assign a category to any damage found.
5. Count and record the number of each defect category found on the CCA, and record any damage categories.
6. For each category of damage and solder defect found for which the cause (from the Probable Causes list) is uncertain, determine the cause:
 - a) For a potential material cause, evaluate the material for compliance with its specification. (Example: test problem component for lead solderability, perform solder float test for PWB.)
 - b) For a potential process cause, identify a process change that will reduce or eliminate that cause. (Example: increase time in solder.)
7. Verify cause assignments by soldering a comparable CCA, inspecting by Steps 3-5, and comparing with previous results:
 - a) The CCA has any material deficiencies found in Step 6a eliminated.
 - b) The process is changed as indicated from Step 6b.
8. Repeat Steps 6 and 7 for any remaining defects until defects disappear.
9. Prevent solder defects on CCA's:
 - a) Prevent components and CCB's with material deficiencies from being released to the factory.
 - b) Solder comparable CCA's using the verified process.

APPENDIX II

INSPECTION PROCESS DEVELOPMENT BY "CONTROLLED EXPERIMENT"

1. Select a group of inspectors (based on availability or reputation).
2. Identify inspection process variables (magnification, defect list, instructions, performance feedback, etc.).
3. Collect a sample (of an adequate number of pieces) of a particular assembly design.
4. All inspectors count and record defects (by category and location) on all assemblies, using one set of inspection process variables.
5. Find:
 - a) The number of connections reported as defects by any inspector $[n(\text{any})]$, and
 - b) the number of connections reported as defects by all inspectors $[n(\text{all})]$. To qualify for $n(\text{all})$, the defect category assigned by the inspectors must agree.
6. Repeat Steps 4 and 5 using a different set of inspection process variables. If you do not think you will be able to interpret the results, pre-select each set of inspection process variables. If you think you are able to interpret the results, then use them to suggest appropriate improvements for the inspection process.
7. The inspection disagreement rate is defined as $[n(\text{any}) - n(\text{all})] / n(\text{any})$. Identify the inspection process variables that give the smallest disagreement rate. This rate represents the "inspection process capability".
8. If the inspection process capability is better than a 10 percent disagreement rate, it is reliable enough for use in experiments on the soldering process.

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OPTIMIZATION OF THE WAVE SOLDERING PROCESS FOR AN ADVANCED AVIONICS PROCESSOR MOTHERBOARD USING DESIGN OF EXPERIMENT (DOE) METHODS

by

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ABSTRACT

Hughes RSG Process Engineers performed a Design of Experiment study to optimize wave solder parameters for an advanced avionics processor PWB motherboard. Due to the difficult nature of the PWB (22 layers, 19" x 16", over 18,000 solder joints) and the scarcity of hardware, advanced experimental techniques were necessary to maximize results and to validate results statistically. The experimenters used a randomized block full factorial test design to identify critical parameters and interactions. This test was followed by a randomized full factorial with center point to refine the critical wave solder parameters. The *first* board soldered using the final test results achieved 99.8% acceptable solder joints to WS-6536 and MIL-STD-2000.

INTRODUCTION

The motherboard assembly is a 22 layer board having dimensions of 16.5 x 19.5 x 0.167 inches. Sixty electrical connectors, each with 300 pins, plus test connectors must be soldered to the motherboard PWB, creating a total of over 18,000 solder joint connections. This assembly is larger, denser, and thicker than any previously built at RSG and as such the most advanced equipment was chosen to achieve successful assembly. The wave solder machine selected is configured with an 18 foot conveyor, wave fluxer, four preheaters, one topside preheater, turbulent solder wave, and a laminar solder wave. Closed loop controls are used by the machine to ensure that parameter settings are being maintained.

To define and execute the requirements of this experiment, a team approach was used. Team members included the design engineer, manufacturing engineers, quality assurance, production, and statisticians. Team members met periodically to assess the progress of the experiment and to guide the future steps.

IDENTIFICATION OF WAVE SOLDERING PARAMETERS

To develop a viable wave solder schedule for the motherboard assembly, a statistical evaluation of the pertinent wave solder parameters would be performed. The first task which had to be accomplished before any statistical procedures were considered was to identify all the various parameters present in the wave soldering operation. The following is a list of those parameters as assembled by the team.

TABLE 1. Wave Soldering Machine Independent Parameters

Flux Type	Flux Wave Height
Air knife pressure	Solder Temperature
Flux specific gravity	Conveyor angle
Conveyor speed	Solder purity
Solder wave #1 height	Preheater temp. #1
Solder wave #2 height	Preheater temp. #2
Solder wave #2 form	Preheater temp #3
	Preheater temp #4

Based on previous experience, the team members selected the following five parameters which were the most significant to the operation of the wave soldering machine: Flux specific gravity, solder wave #1 height (turbulent wave), solder wave height #2 (laminar wave), conveyor speed, and preheater temperature settings.

DETERMINING SIZE OF EXPERIMENT

Initially, both Fractional Factorial and Full Factorial Methods were considered for the Design of Experiment. The Fractional Factorial method was dropped from further consideration since it could not be assumed that no interactions existed between various parameters of the wave soldering machine. Two variable levels (high and low) were chosen to be used with the full factorial testing method. The resultant 32 treatments (runs) which were required of the full factorial method could not be accommodated due to the scarcity of motherboard PWBs and the necessary connectors. In order to set up an economical full factorial design of experiment, the number of treatments (runs) had to be reduced. To accomplish this task, flux specific gravity was dropped from consideration, thus reducing the size of the test from 32 runs to 16 runs. To provide additional replications, the 32 available connectors would be cut in half, thereby providing a total of 64 connector samples for a randomized block full factorial test. As indicated previously, motherboard PWBs were scarce and no more than four could be obtained. To comply with the requirements of the full factorial test, suggestions were made to either run each full size board four times, or cut each board into four quarter size test boards which could be run individually.

COMPARISON OF FULL SIZE MOTHERBOARDS AND QUARTER SIZE MOTHERBOARDS

This evaluation was undertaken to study the effects of substituting quarter size motherboards for full size motherboards.

A full size motherboard and two quarter size motherboards were utilized to develop thermal profiles of the PWBs (temperature vs. time).

The primary concern was whether or not the topside temperature of the quarter size panels was equivalent to the topside temperature of the full size PWB. This equivalence of top side temperature throughout the pre-heat region, if present, would demonstrate equivalent thermal properties of the quarter and full size panels.

PROCEDURE TO TEST FOR COMPARISON OF THERMAL PROFILES OF PWBs

Two quarter panel size PWBs and a full size PWB were each run four times in the wave solder machine, using the following wave solder schedule:

TABLE 2. Wave Solder Schedule For Evaluation of Thermal Profiles

Preheater #1	160°F
Preheater #2	200°F
Preheater #3	250°F
Preheater #4	385°F
Wave #1 (turbulent)	OFF
Wave #2 (laminar)	0.45
Conveyor speed	1 ft/min

For each run, a thermocouple was attached to the surface of the PWB (Figure 1 thermocouple positions 1, 2, 3, and 4 correspond to runs 1, 2, 3, 4). Temperature readings were recorded at 15 second intervals. Analysis of the temperature readings was accomplished by computing means and variances for each 15 second interval. Figure 2 is a display of mean recorded temperatures of the three PWBs. The differences observed in the heating up and cool-down patterns of the three PWBs are not significant. The small phase shift in the temperature readings is due to the size difference between the large and small PWBs and the resultant position of the panels on the conveyor. Figure 3 is a display of the mean recorded temperatures of the two quarter size panels.

Figure 4 shows the results of the two tailed "t" tests performed for the recorded mean temperature readings of the full size and quarter size PWBs. For the purpose of this test, the mean and variance for the quarter size panel were computed using the readings from both quarter size panels. The test hypothesis was:

"Are mean temperatures at 15 second intervals different between full size and quarter size PWBs?"

$$H_0: \bar{X}_F = \bar{X}_Q \quad \text{Null Hypothesis}$$

$$H_a: \bar{X}_F \neq \bar{X}_Q \quad \text{Alternative Hypothesis}$$

With $\alpha=0.10$ and 10 degrees of freedom, the test level t_0 equals 1.812. As it can be observed from Figure 4, all test points fall below the test level t_0 .

Based on the results obtained, H_0 could not be rejected and therefore, with 90% confidence we interpreted that both quarter size and full size motherboards respond in the same fashion to a typical preheat environment. Sixteen quarter panel size PWBs were subsequently prepared (by cutting four full size PWBs) to perform the full factorial test.

SCREENING EXPERIMENT

Randomized Block Full Factorial Test Design. A randomized block full factorial method was selected to test the following hypotheses:

"Does any parameter or interaction have an effect on wave soldering the connectors to the motherboard, regardless of position?"

$H_0: \tau_i = 0$ Null Hypothesis

$H_a: \tau_i \neq 0$ Alternative Hypothesis

$\alpha = 0.10$ Test Level

Where τ_i is the effect of every parameter and every interaction.

Having chosen two levels (high and low) for each of the four significant wave soldering machine parameters, Table 3 was constructed to specify the respective values of these parameters. Sixteen runs (24 combinations) were required to test each combination of the parameters at high and low levels. These levels were set at what was believed to be extreme values to maximize any differences in results. Table 4 is a matrix of the full factorial set of test runs.

Thirty two full size connectors were cut in half, thereby providing 64 half connectors. These half connectors, containing 150 pins each, were consistently located on all PWB test samples in each of four locations. The experiment as designed, would "block" the effect of connector location, and would accurately test the hypotheses.

TABLE 3. Values for Wave Soldering Parameters

Level	Conveyor Speed	Preheat	Wave #1	Wave #2
Low (-)	1.00 ft/min	#1 160°F #2 200°F #3 250°F #4 385°F	0%	0.35 in.
High (+)	1.50 ft/min	#1 260°F #2 300°F #3 350°F #4 390°F	50%	0.40 in.

TABLE 4. Full Factorial Matrix

Run	Conveyor Speed	Preheat	Tubulent Wave	Laminar Wave
10	+	+	+	+
1	+	+	+	-
15	+	+	-	+
11	+	+	-	-
3	+	-	+	+
16	+	-	+	-
14	+	-	-	+
7	+	-	-	-
13	-	+	+	+
12	-	+	+	-
5	-	+	-	+
6	-	+	-	-
2	-	-	+	+
8	-	-	+	-
4	-	-	-	+
9	-	-	-	-

PROCEDURE

Test PWBs were initial vendor prototypes. Solderability of these PWBs was known to be marginal. However the assumption was made that parameters improving solder joint yield on these PWBs would act similarly on PWBs meeting the solderability requirements.

The PWB test samples were pre-baked in a nitrogen filled oven for 16 hours at 190°F. Each board was stuffed with four half connectors which had been pretinned and cleaned. Connector positions were identical on all 16 PWBs, with all unused sites masked off. All of the test boards were subsequently run in the wave solder machine per the requirements of the Full Factorial Matrix (Table 4). After each run, the test boards were demasked and cleaned using standard cleaning procedures.

INSPECTION OF SOLDERED JOINTS

All soldered joints were inspected per the requirements of WS- 6536 and MIL-STD-2000 at 12X magnification (total of 9600 joints). The defects were partitioned into the following categories: unfilled holes, insufficient solder joints, excessive solder joints, and over heated solder joints.

The inspections were kept as objective as possible by randomizing the inspection sequence and by not informing the inspector which run was being inspected. The results of visual inspection were utilized to determine the yield data, which takes into consideration the effects of total recognized defects relative to the total number of solder joints, i.e.

$$\% \text{ Yield} = 1 - \frac{\text{total number of defects}}{\text{total number of solder joints}}$$

Analysis of variance (ANOVA) was undertaken to determine if any of the four main effects of the eleven interactions were significant. Figure 5 represents the significance of the main effects and interactions using the F statistic at a 90% confidence level. Strong interactions seem to exist between preheat profile and the turbulent wave (BC). A strong main effect can also be attributed to the preheat profile (B). Less significant interactions exist between conveyor speed and the turbulent wave (AC), and conveyor speed, turbulent and laminar waves (ACD).

By referring to Figures 6 and 7, it can be concluded that the low preheat profile when the turbulent wave is off contributes to the highest number of good solder joints (higher yield). Figures 8 and 9 indicate that a combination of high conveyor speed and low laminar and turbulent waves also contributes to obtaining higher yields.

OPTIMIZATION EXPERIMENT

Randomized Full Factorial With Center Point. The results obtained, low preheat, turbulent wave off, low laminar wave, high conveyor speed, from the first ANOVA are preliminary, but point toward the direction of higher yield. To develop a more viable wave solder schedule, further refinement of the significant parameters are required in the region having the highest yield. Since laminar wave height is already at the minimum height allowed by the military specifications, the only remaining parameters to be optimized are conveyor speed and preheat settings.

Using the results of the first ANOVA, a new set of test values for conveyor speed and preheat settings was established. Included in this set of test values was a center value that was replicated three times to determine experimental error. Center points were added to give a better prediction of experimental error and to provide a basis for evaluating the fit of a linear model. If the results showed significant nonlinearity, then only four additional points would be required to complete a Central Composite Design (CCD) experiment and could be used to fit a complete second order model. Table 5 is a list of those values and Table 6 is a matrix of the full factorial optimization test.

TABLE 5. Values for Wave Solder Optimization

Level	Conveyor Speed	Preheat
Low (-)	1.50 ft/min	#1 110°F #2 150°F #3 200°F #4 335°F
High (+)	1.75 ft/min	#1 260°F #2 300°F #3 350°F #4 390°F
Center pt. (o)	1.63 ft/min	#1 135°F #2 175°F #3 225°F #4 360°F

TABLE 6. Full Factorial Optimization Matrix

Run	Conveyor Speed	Preheat
6	+	+
5	+	-
1	-	+
2	-	-
3	0	0
7	0	0
4	0	0

RSG manufactured PWBs were used for the full factorial optimization test. These boards meet solderability requirements and gave consistently higher yields than those boards used for the first ANOVA.

Seven quarter size panels were prepared with two half connectors apiece. The connectors were consistently located on the test panels. All of the test boards were run per the requirements of the Full Factorial Optimization matrix (Table 6), demasked, cleaned and inspected to the requirements of WS-6536 and MIL-STD-2000. Visual inspection data was used to determine yield (percent acceptable) for each test run.

To check for linearity in the design region, a test was used to determine if a significant difference exists between the mean of the center points yields and the mean of the remaining optimization test yields. The test hypothesis was:

"Is there a significant difference in the mean of the center point yields and the remaining test yields?"

$$H_0: \bar{X}_{cp} = \bar{X}_r \quad \text{Null Hypothesis}$$

$$H_a: \bar{X}_{cp} \neq \bar{X}_r \quad \text{Alternative Hypothesis}$$

With $\alpha=0.10$ and 12 degrees of freedom, the test level t_0 equals 2.179. The computed value of t was 0.100, therefore H_0 could not be rejected and it was assumed with 90% confidence that the model was linear in the test region.

Analysis of variance was used to determine if the effect of conveyor speed, preheat temperature, or their interaction were significant. Figure 10 is a representation of those effects using the F statistic at a 90% confidence level. Interaction exists between conveyor speed and preheat temperature (AB) with conveyor speed exhibiting a strong main effect (A). Figures 11 and 12 indicate that higher solder joint yields were obtained with a low conveyor speed and a high preheat in the optimization test region. This result is in the direction opposite that obtained with the first ANOVA. Using the results of the full factorial optimization test and the results of the randomized block full factorial test, a wave solder schedule for the motherboard assembly was formalized.

SUMMARY

DOE techniques provided economical and significant results in developing a wave solder schedule for the motherboard assembly. These techniques should be applied to optimize other processes during the developmental phases. Continued success of the initial solder runs will be aggressively pursued by controlling incoming solderability of boards and parts, and by analyses of wave solder parameters not studied in this task, such as flux specific gravity.

RESUMES

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B.S. Chemical Engineering, University of California Los Angeles

Chris Schutzenberger is a Senior Project Engineer at Hughes Radar Systems Group in El Segundo, CA. During his time as a Process Engineer he has supported the F/A-18 Radar product line and implemented WS-6536 on the F-14A Radar product line. In addition he was a key contributor in developing the LCC and Ceramic Daughterboard processes for the F-15 MSIP Radar upgrade. He has been part of the Assembly Process Engineering section of the Product Operations Division since he joined Hughes in 1983.

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Mehrdad Khademi is a member of the technical staff at Hughes Radar Systems Group in El Segundo, CA. He has been part of the Assembly Process Engineering section of the Product Operations Division since his arrival at Hughes in 1986. He has been responsible for process support of F-15 and F-14 Radar product assembly lines as well as various solvent cleaning and solder joint reliability studies. Prior to joining Hughes, Mr. Khademi worked for C.F. Braun and Co. where he was involved in engineering and construction efforts of chemical plants.

S.V. SCHULTZ

B.S. Mathematics, Idaho State University

Samuel Schultz is a member of the technical staff at Hughes Radar Systems Group in El Segundo, CA. He has been part of the Assembly Process Engineering section of the Product Operations Division since his arrival at Hughes in 1987. He has been responsible for process support of the F-14 Radar product assembly line and automated wave soldering. Mr. Schultz, prior to joining Hughes, worked for American Microsystems Inc. where he was involved in developing statistical process controls.

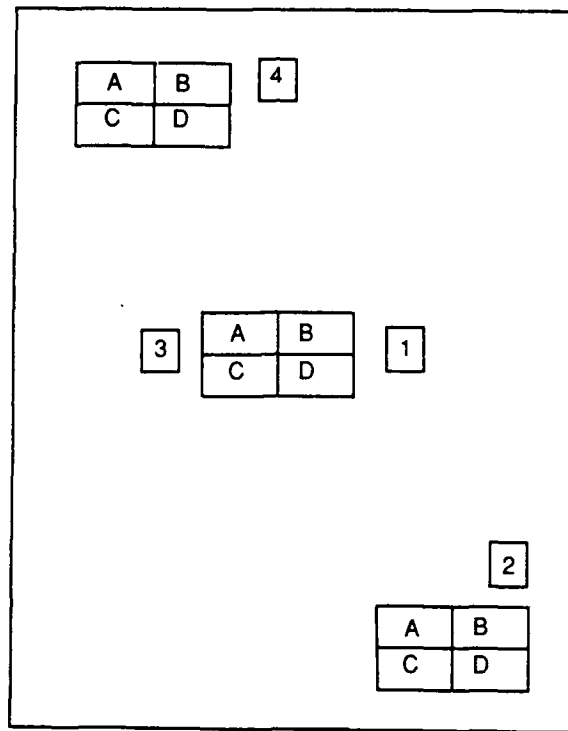


FIGURE 1. Thermal Profile Measurement Sites On PWB Surface.

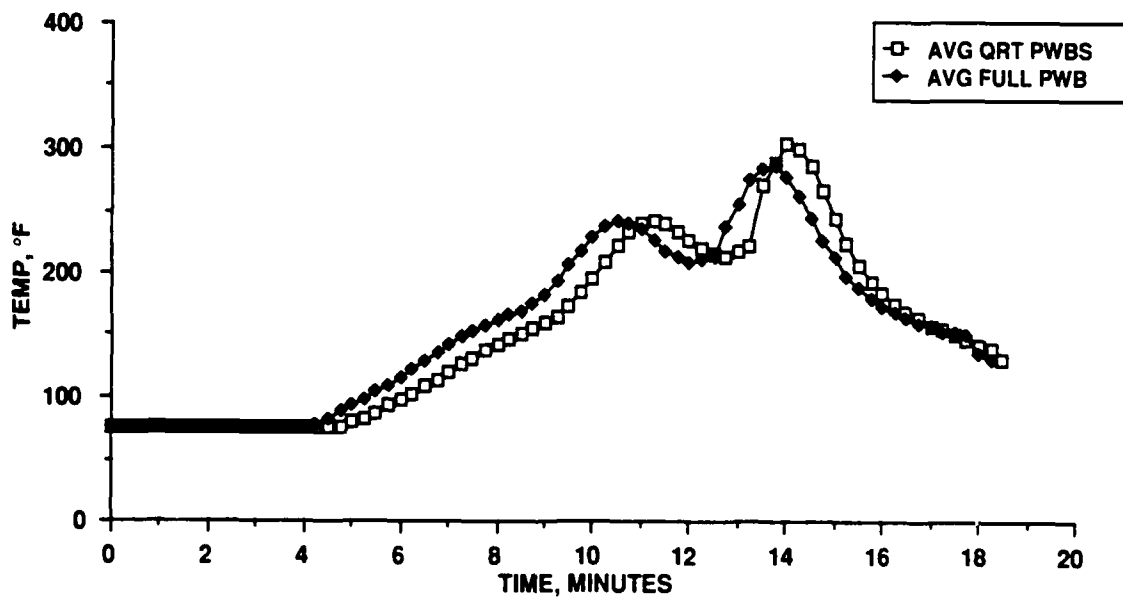


FIGURE 2. Mean Recorded Temperatures of Full Size and Quarter Size ATF Backplanes.

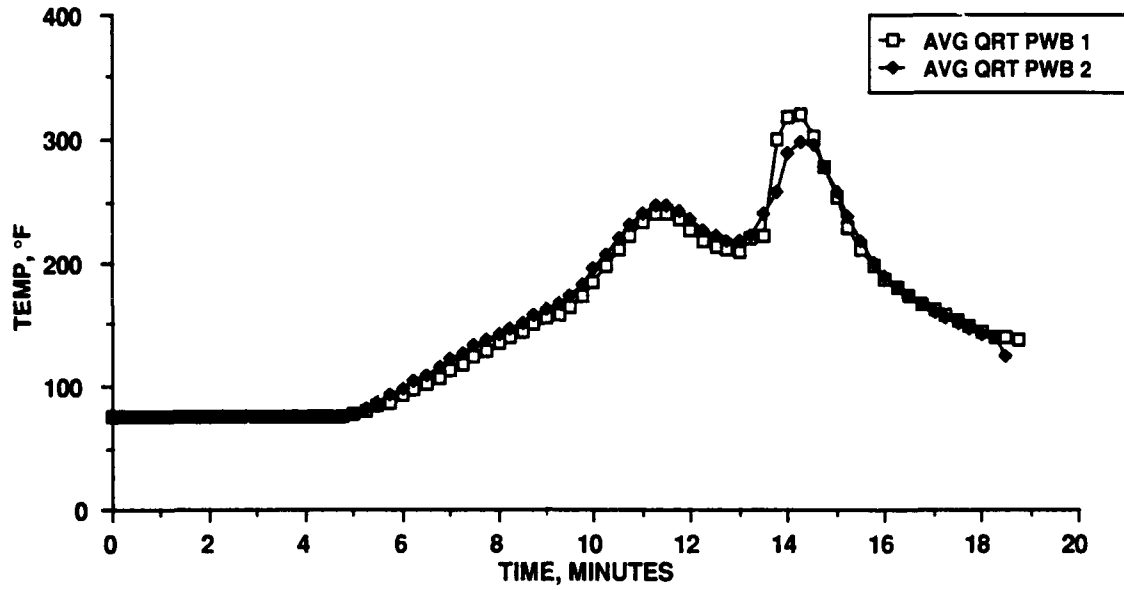


FIGURE 3. Mean Recorded Temperatures of Quarter Panel Size ATF Backplanes.

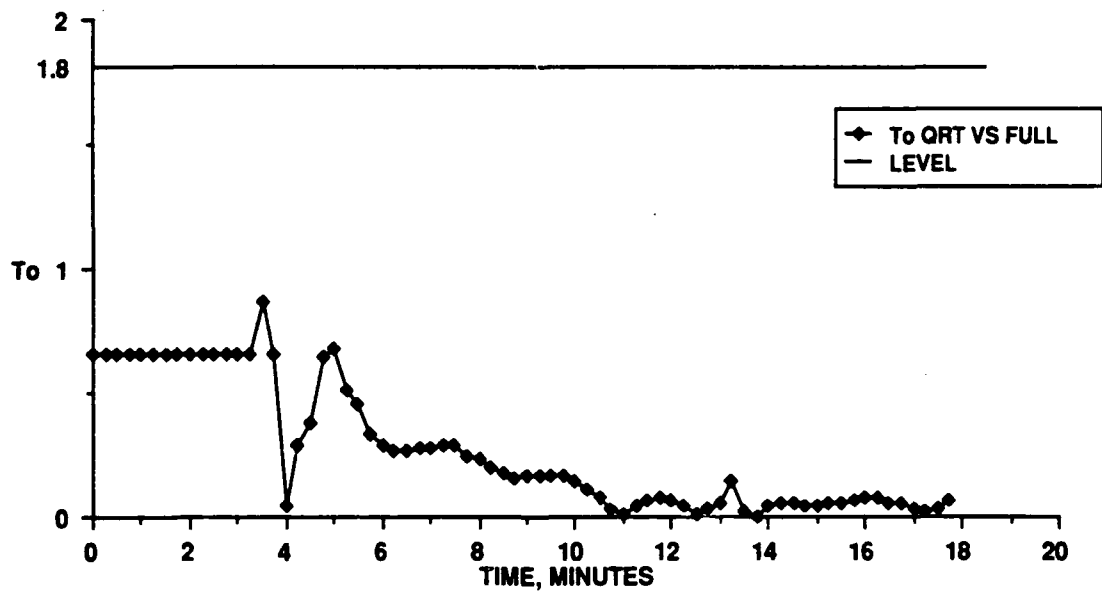


FIGURE 4. To For Mean Recorded Temperatures of Full Size and Quarter Panel Size ATF Backplanes.

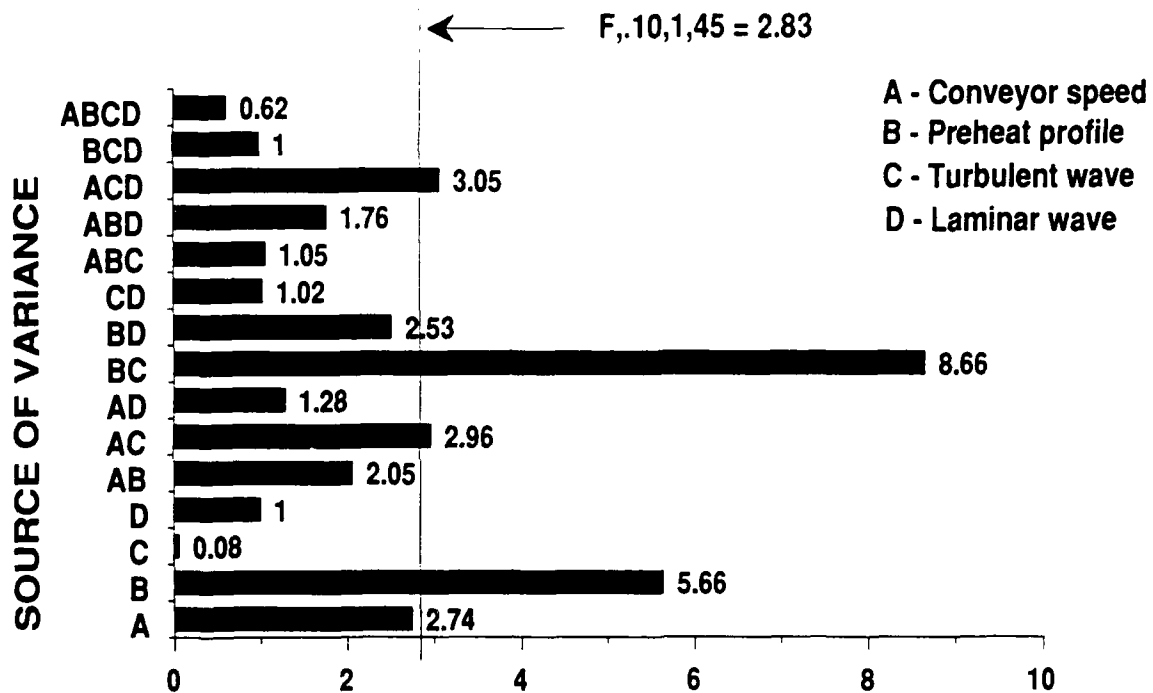


FIGURE 5. Analysis of Variance-Total Visual Defects.

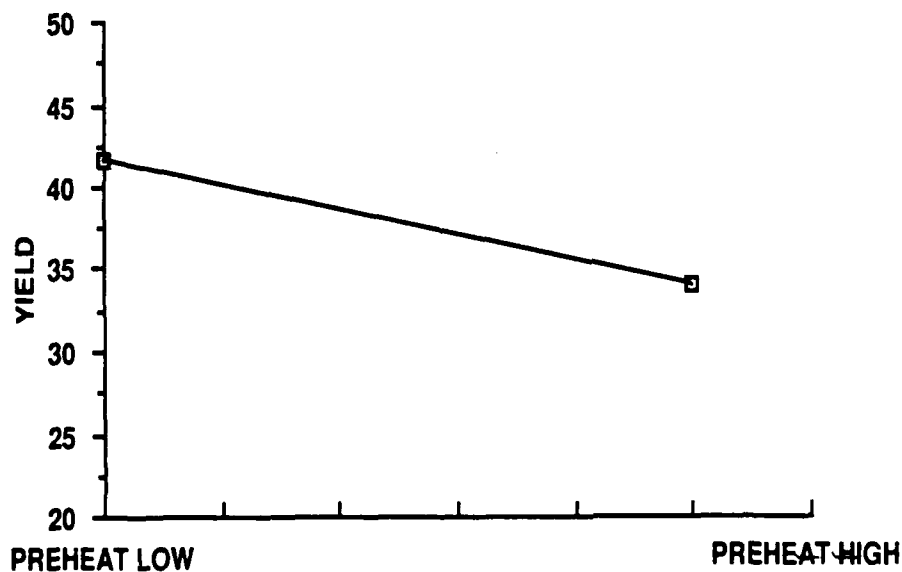


FIGURE 6. Preheat Profile (B Main Effect) - Total Visual Defects.

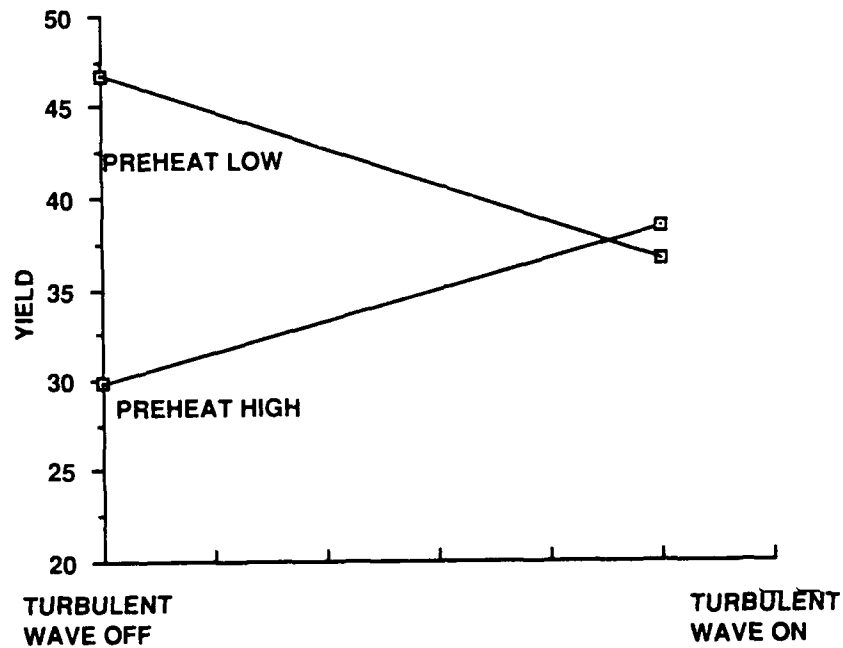


FIGURE 7. Preheat Profile and Turbulent Wave Interaction (BC Effect) – Total Visual Defects.

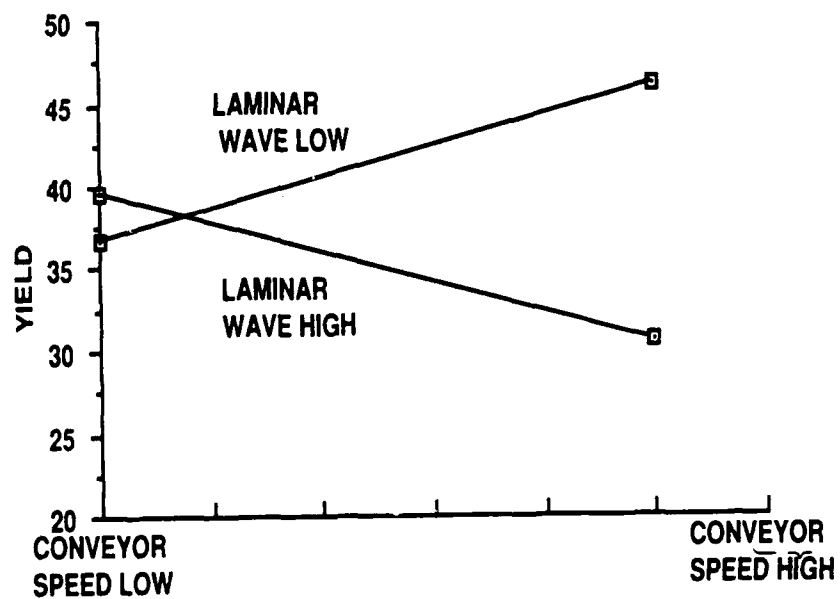


FIGURE 8. Conveyor Speed and Laminar Wave Interaction (ACD Effect) - Total Visual Defects

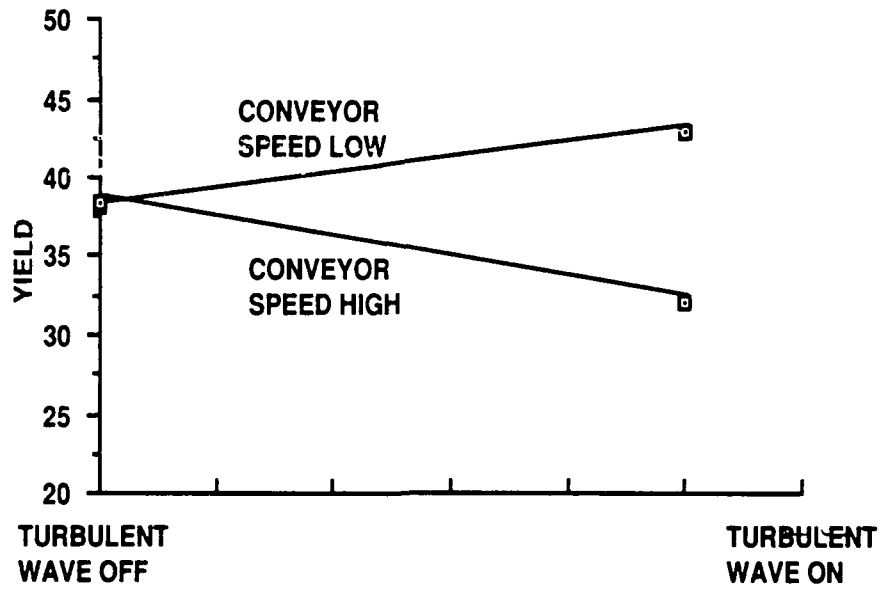


FIGURE 9. Conveyor Speed and Laminar Wave Interaction (AC Effect) - Total Visual Defects

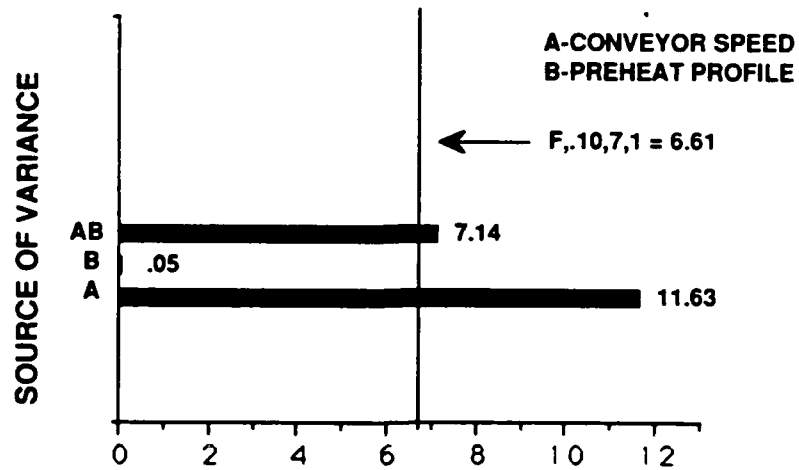


FIGURE 10. Analysis of Variance Total Visual Defects - Wave Solder Optimization

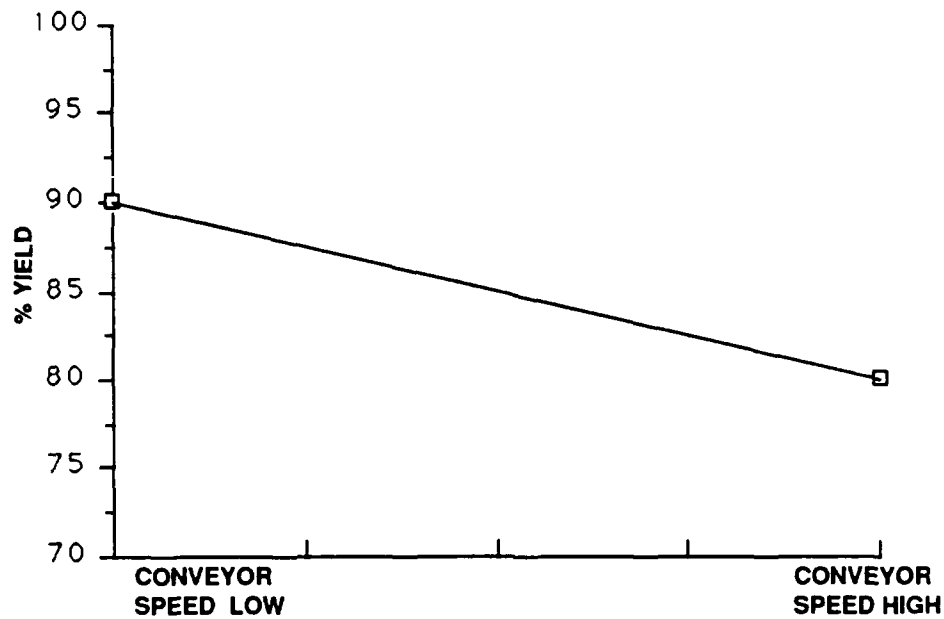


FIGURE 11. Conveyor Speed (A Main Effect) - Total Visual Defects

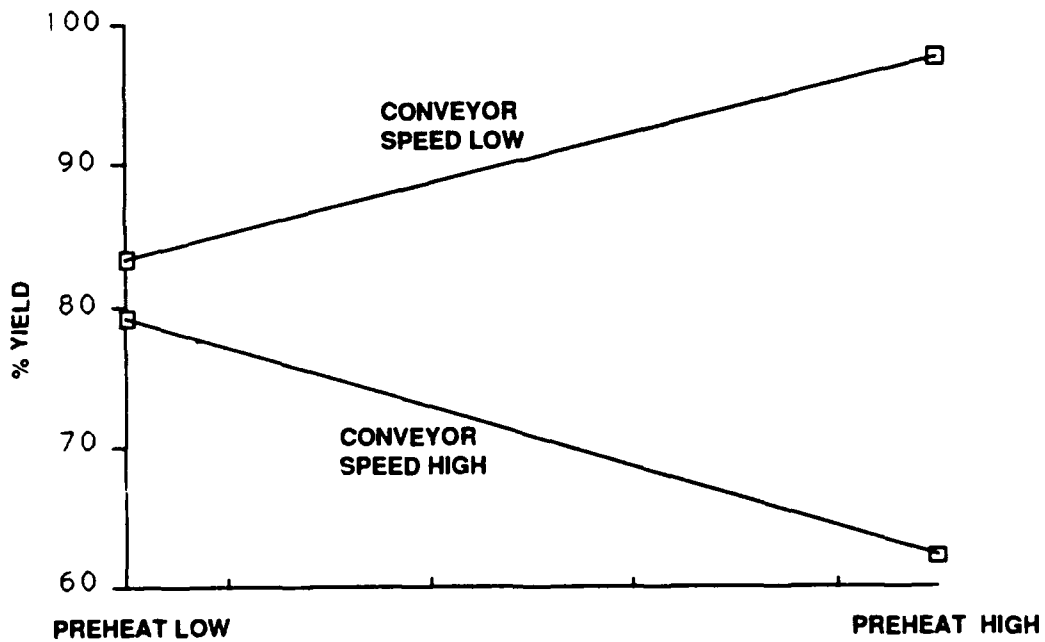


FIGURE 12. Preheat Profile and Conveyor Speed (AB effect) - Total Visual Defects

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Chris received a BS degree in Chemical Engineering from UCLA and is a member of Tau Beta Pi.

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**A COMPARISON OF ROSIN RESIDUE DETERMINATION
BY THE IPA EXTRACTION TECHNIQUE WITH THE
SUPPLEMENTAL ULTRASONIC EXTRACTION TECHNIQUE**

by

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ABSTRACT

This paper examines the residual rosin residue test as defined in the IPC document Cleaning and Cleanliness Testing Program: A Joint Industry/Military/EPA Program to Evaluate Alternatives to Chlorofluorocarbons (CFCs) for Printed Board Assembly Cleaning. In particular, it examines three issues regarding the technique as outlined in this test procedure. These three issues are:

- (1) shaking the bag with the IPA/assembly
- (2) using an extractive medium based on IPA/water/phosphoric acid as opposed to straight IPA
- (3) using ultrasonics as an extractive aid in the technique.

Data are presented addressing these three issues.

PWA/SMA CONTAMINATION TESTING

Testing printed wiring assemblies (PWAs) and surface mount assemblies (SMAs) is becoming more critical as the assembly functions become more complex and the feature sizes grow smaller. The ionic contamination test (solvent extract resistivity test) has been known in the industry for fifteen years. Although this test has proven very useful for contamination testing, considerable interest exists for determining the amount of organic contamination being left on the surface after cleaning. Because the majority of fluxes and pastes being used today are still based on rosin chemistry, a test for detecting and quantifying the amount of rosin residue would prove quite useful as a supplementary test to ionic contamination testing.

BENCHMARK/PHASE 2 TESTING

In 1988 a concerted move was made among the EPA, the military, and the industry to eliminate chlorofluorocarbons (CFCs) in industrial uses. In particular, a group was constituted which became known as the EPA/DoD/Industry Ad Hoc Solvents Working Group. This group focused specifically on the usage of CFC-113-based solvents used for electronics cleaning. In order to accomplish this goal, the Ad Hoc Solvents Working Group, after careful deliberation that extended almost over a entire year, hammered out a standard test procedure and standard test assembly. The chief purpose of this standard test procedure and test assembly was to define a benchmark cleanliness reference standard using the stabilized CFC-113/methanol azeotrope and batch cleaning as the cleaning process.

This benchmark test (Phase 1 test) using the cleaning process involving batch cleaning and the stabilized azeotrope of CFC-113 and methanol was performed by two government laboratories, EMPF in Ridgecrest, CA and NAC in Indianapolis, IN. For each producer of an alternative technology who wishes to receive DoD support for his technology, it is incumbent for him to perform the benchmark test using his particular cleaning technology in place of the benchmark (Phase 1) cleaning process.

RESIDUAL ROSIN TEST

The test procedures used in the Benchmark/Phase 1 to determine the benchmark cleanliness reference level were four: (1) ionic contamination testing, (2) residual rosin testing, (3) surface insulation resistance (SIR) and (4) organic residue testing via high performance liquid chromatography (HPLC). The residual rosin test as defined by the Ad Hoc Solvents Working Group test procedure (Cleaning and Cleanliness Testing Program: A Joint Industry/Military/EPA Program to Evaluate Alternatives to Chlorofluorocarbons (CFCs) for Printed Board Assembly Cleaning) involved making an extract of the test assembly using isopropyl alcohol (IPA) as the extractive medium and shaking a bag containing the IPA/assembly for ten minutes. A sample is then taken from the bag, placed in a cuvette, and a spectrophotometric reading made at an absorbance of 242 nanometers (nm). Previous to this, standards were run of the flux and paste used. Based on the absorbance values of the standards, the amount of micrograms (μg) of rosin residue extracted off the SMA by the IPA can be easily determined.

TEST TECHNIQUE

Although the residual rosin test is undoubtedly very useful, the particular technique used in making the extraction came into question. Three points, in particular, were raised as issues regarding the technique in the standard test procedure. These issues were:

- (1) shaking the bag introduced an unmistakable operator effect,
- (2) evidence suggests that an extractive medium based on IPA/water/phosphoric acid might be superior to straight IPA in an extractive medium,
- (3) ultrasonics might prove a very useful supplement to aid the residual rosin to quickly go into solution.

EXPERIMENTAL PROCEDURE

Data from five different techniques are presented here. The purpose of the investigation was to determine the effectiveness of those five extraction techniques for removing rosin residues from surface mount assemblies (SMAs). The particular SMAs was used in the experiment were 4.25" X 4.37" and have fourteen (14) leadless ceramic chip carriers (LCCCs) on the assembly: three 84 termination LCCCs, one 68 termination LCCC, two 52 termination LCCCs, four 28 termination LCCCs, and four 20 termination LCCCs. Two different solder pastes were employed: an RA paste and an RMA paste. Each paste had a built-in standoff of 5 mils. The soldering technique was vapor phase reflow. The assemblies had the paste screened on the board, the components were mounted manually, and the assembly reflowed. After solder reflow the assemblies were cleaned. Two different solvent cleaning agents were used: (1) a stabilized azeotrope of HCFC-141b/HCFC-123/methanol which will be called in this paper the HCFC-based solvent and (2) a stabilized azeotrope of CFC-113/methanol/isohexane/acetone (commercially available as Genesolv®DFX) which will be called in this paper the CFC-based solvent. After cleaning, the extractive techniques for removing rosin residues were then employed. The five techniques are as follows:

1. manual shaking in zip loc bag - 100ml solution
in IPA time: 10 min.
2. unagitated soaking in IPA in a s/s vessel - 60
ml solution time: 15 min.
3. s/s vessel containing IPA using ultrasonics -
60ml solution time: 15 min.
4. unagitated soaking in a solution consisting of
98.9% IPA, 1.0% DI water, .1% Phos. acid - 60ml
solution time: 15 min.
5. number 4 solution using ultrasonics - 60ml
solution time: 15 min.

TEST DATA

Each datum point is the average of the UV spectrophotometric readings made from four assemblies.

<u>Paste</u>	<u>Solvent</u>	Extraction Techniques (in $\mu\text{g}/\text{in}^2$)				
		(1)	(2)	(3)	(4)	(5)
RA	HCFC-based	58	47	76	51	90
	CFC-based	88	30	195	46	291
RMA	HCFC-based	50	38	59	33	112
	CFC-based	40	23	52	26	138

CONCLUSION

The conclusion to be drawn is that the most effective extractive technique for removing residual rosin is the use of an IPA/water/phosphoric acid solution in a stainless steel tank using ultrasonics as a supplemental aid to make the extraction. The next best technique is the use of straight IPA in a stainless steel tank using ultrasonics as a supplemental aid in making the extraction.

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Kirk is a member of SME, the Electronics Group of SME, IPC, SMTA, and the International Electronics Packaging Society. He holds a Ph.D. degree from The Johns Hopkins University and an MBA degree from the Florida Institute of Technology.

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CLEANING MILITARY ELECTRONICS IN THE FUTURE

by

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ABSTRACT

Military specifications place strict guidelines on which fluxes can be used when assembling printed circuit assemblies (PCAs). These fluxes, along with additional military specifications, limit the choices for how PCAs can be cleaned. The Montreal Protocol has now taken its first step in removing one of the few, and perhaps most popular options available, chlorofluorocarbons (CFCs).

The Montreal Protocol, calling for a gradual reduction of all CFC based products, was signed by 24 nations in September, 1987. The pact, although aimed at producers, directly affects all users of CFCs, especially those associated with military contracts.

This brief describes the EMPF's present research on finding alternative materials to CFCs and other research on furthering the possibility of using water soluble fluxes, low solids fluxes and ultrasonics in the future.

INTRODUCTION

The Electronics Manufacturing Productivity Facility (EMPF), located in Ridgecrest, California, is a U.S. Naval activity tasked to do research and development in electronics manufacturing. The 30,000 square foot facility, located near the China Lake Naval Weapons Center, allows equipment to be brought in on loan from manufacturers to aid various research projects. In 1988, the EMPF, along with other Department of Defense and commercial institutions, combined efforts to find alternatives for CFCs. The group, known as the EPA/DOD/IPC Ad Hoc Solvents Working Group, developed a test plan that included three phases. Phase 1, referred to as the Benchmark, used a common CFC solvent to set standards for future solvents. Phase 2 of the study will evaluate new solvents and compare cleanliness test results of those solvents to the

Benchmark results. Phase 3 will examine the possibility of using water soluble fluxes, low solids fluxes, and inert atmosphere soldering processes to replace CFCs.

TESTING

Phase 1

The Benchmark was designed to measure how well a CFC solvent cleans PCAs, and set standards for alternative solvents. In the past, the ways of evaluating one solvent against another were limited. One example is the resistivity of solvent extract test, or ROSE test. The ROSE test is probably the most popular way of measuring how well a cleaning process is working, but it reveals only part of a solvent's cleaning ability. Benchmark testing incorporated other tests that more clearly identified how well a CFC solvent cleans a PCA. In addition to ROSE, test methods included measuring residual rosin using an ultraviolet spectrophotometer, residue analysis using High Performance Liquid Chromatography (HPLC), and measuring leakage current across specific test points using Surface Insulation Resistance (SIR).

The test board was designed primarily around the SIR portion of the test. The SIR tests would reveal if the board was contaminated, and also where the contamination was being left. The test board was made of FR-4 laminate material and measured 4- by 4- by 0.060-inches. The board was designed with four quadrants labeled A, B, C, and D (See Figure 1). Quadrants A and B, representing surface mount technology, each contained an interdigitated comb pattern with 0.006-inch lines and spaces, a pair of parallel traces running inside the component pads, and a pair of parallel traces running outside the component pads. Quadrants C and D representing mixed technology, each contained a comb pattern and the component pads were linked together with via holes in a daisy-chain pattern. The via holes allowed the flux to get under the components. Each of the four quadrants contained four copper pads, each capped with a solder mask dot, yielding a fixed 0.005-inch clearance under each component. Quadrants A and D were populated with a 68-pin, 0.050-inch pitch, leadless chip carrier.

The boards were assembled in five different sequences, which are shown in Table 1. Group A received no

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by Timothy J. Crawford

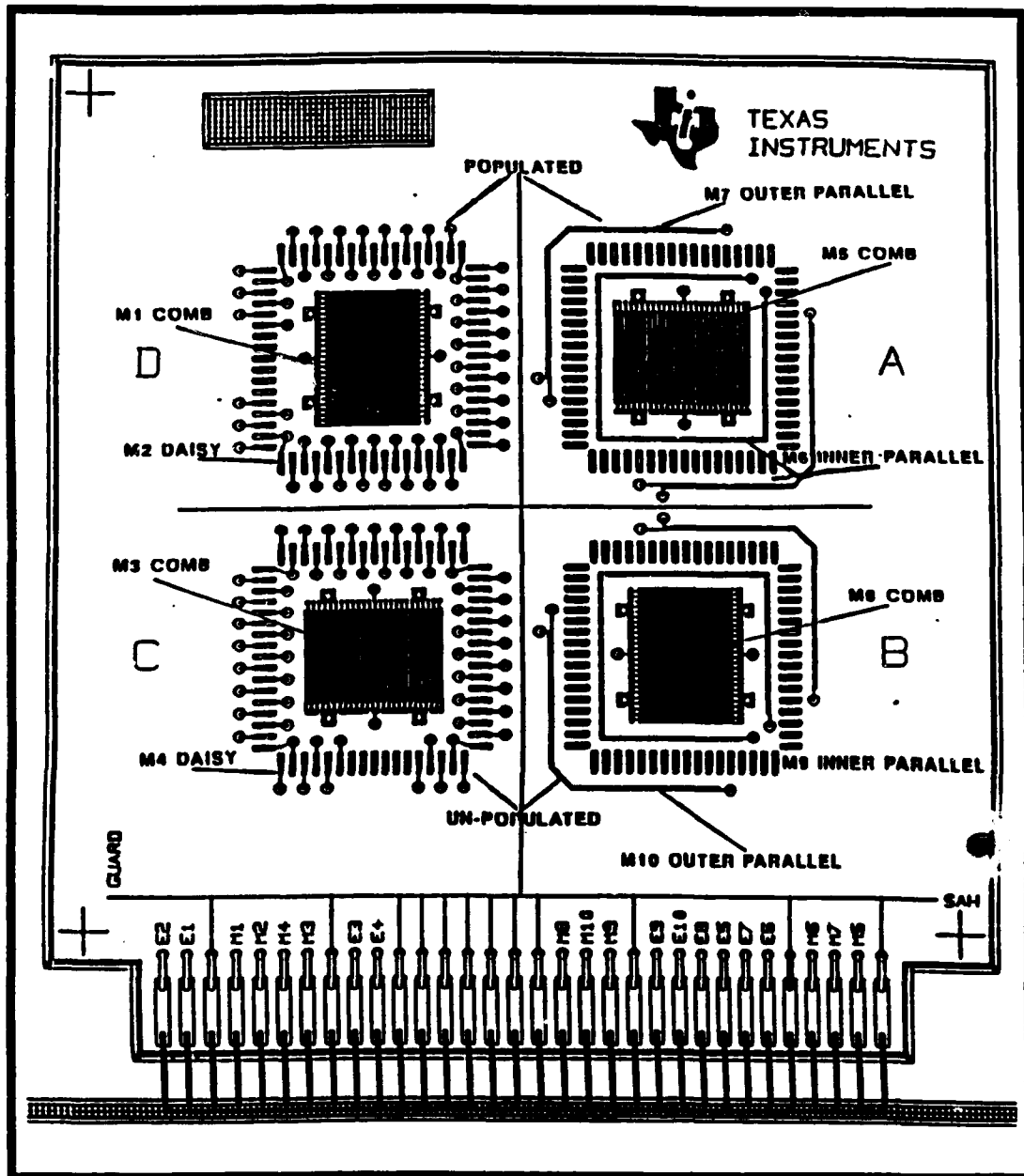


FIGURE 1. CFC BENCHMARK TEST BOARD.

contamination and was used as a control group. Group B was divided into two groups, B1 and B2, and represented worst case situations having contamination and no cleaning. Groups B1 and B2 were both exposed to simulated surface mount technology using solder paste as a source of contamination, but Group B2 underwent an additional step, having the boards fluxed and passed through a wave solder machine. In this instance, Group B2 represented mixed technology. Group C boards were assembled identical to B1 boards, but cleaning was included after reflow. Group D duplicated the B2 process, and added a cleaning step after reflow and after wave soldering. This particular assembly sequence would reveal the amount of contamination added to the board and how much contamination was being removed by the CFC solvent.

TABLE 1. BOARD ASSEMBLY SEQUENCES.

<u>Group</u>	<u>Assembly Sequence</u>
A	No Solder Paste, Clean, Test
B1	Solder Paste, Reflow, No Clean, Test
B2	Solder Paste, Reflow, Wave Solder, No Clean, Test
C	Solder Paste, Reflow, Clean, Test
D	Solder Paste, Reflow, Clean, Wave Solder, Clean, Test

Testing of Phase 1 was performed at the Electronics Manufacturing Productivity Facility (EMPF) in Ridgecrest, California and at the Naval Avionics Center (NAC) in Indianapolis, Indiana. As each facility ran the tests twice, four sets of data were obtained and the results presented in this paper are illustrated in boxplot form. The boxplot represents a set of data which shows the median, the upper quartile (the point containing 25% of the data points above the median), the lower quartile (the point containing 25% of the data points below the median), and the range of the data (See Figure 2).

Ionic Cleanliness Testing. Ionic cleanliness testing was done using an Alpha Metals Omegameter 600 SMD. Results from these tests can be seen in Figures 3 and 4.

The correlation between the two EMPF test runs and the second NAC test run was good. NAC encountered problems during testing that may have contributed to the higher amounts of contamination being deposited on the

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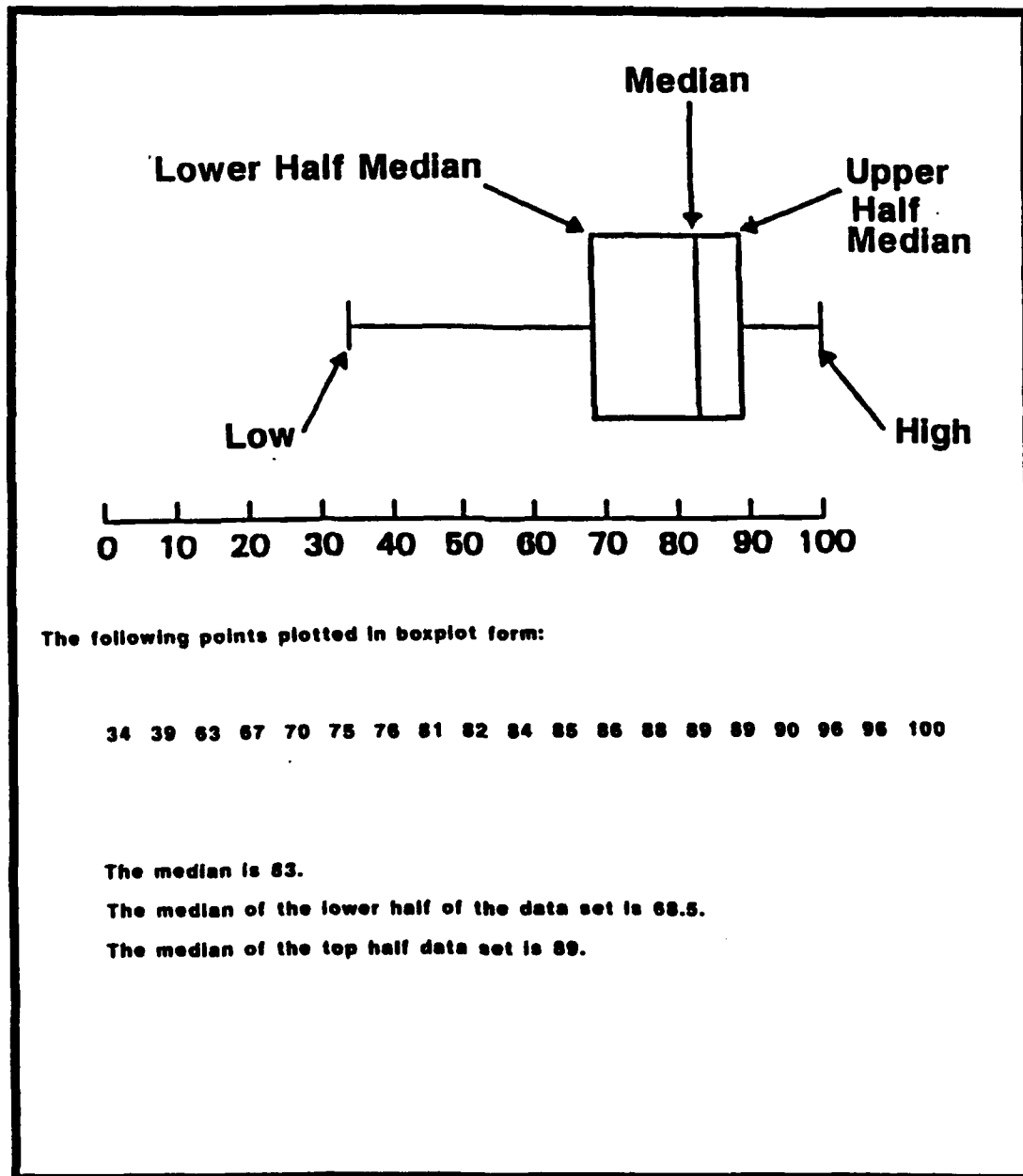


FIGURE 2. SAMPLE BOXPLOT.

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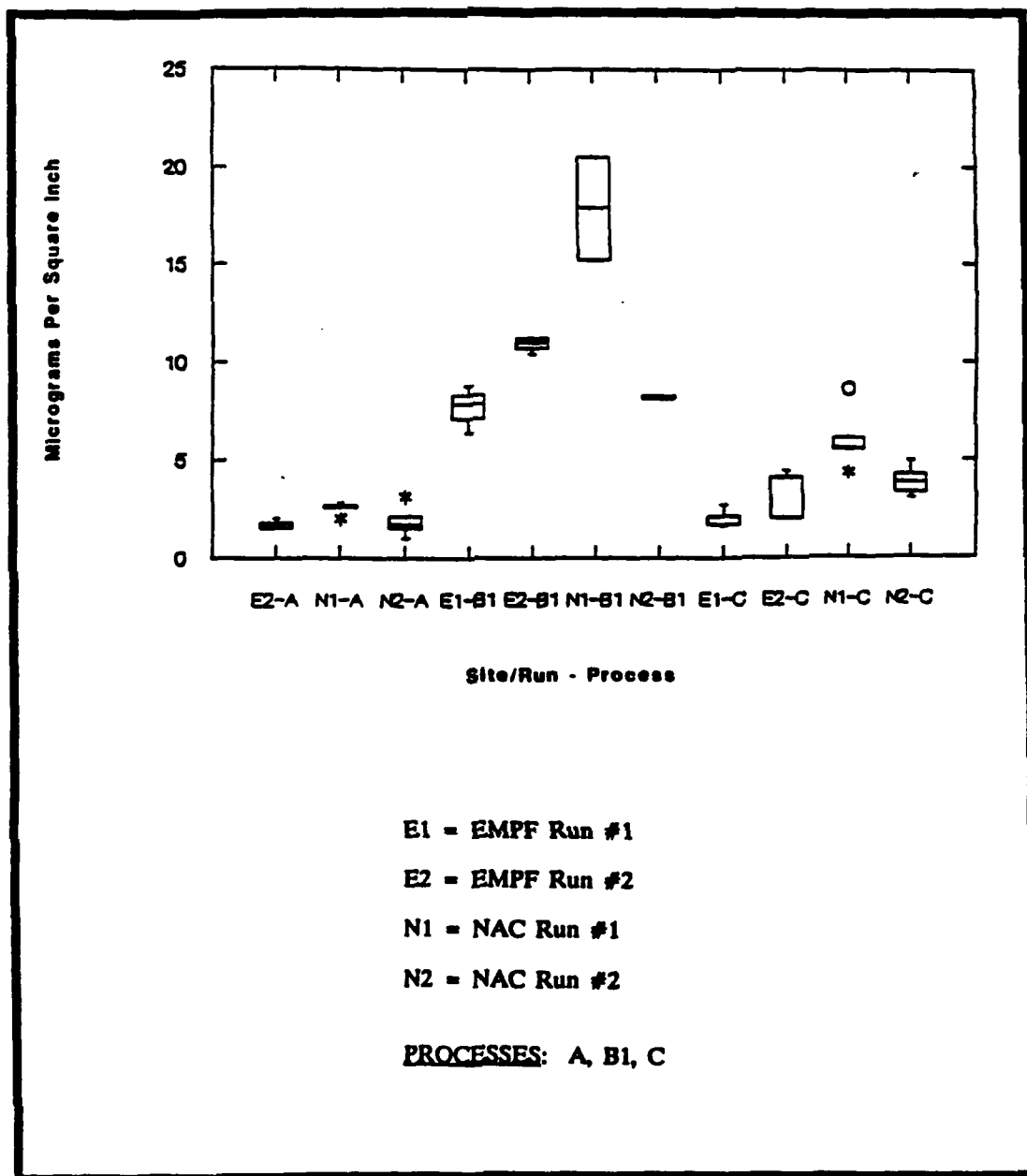


**FIGURE 3. BENCHMARK IONIC CLEANLINESS TEST COMPARISON
OF PROCESSES, A - B1 - C.**

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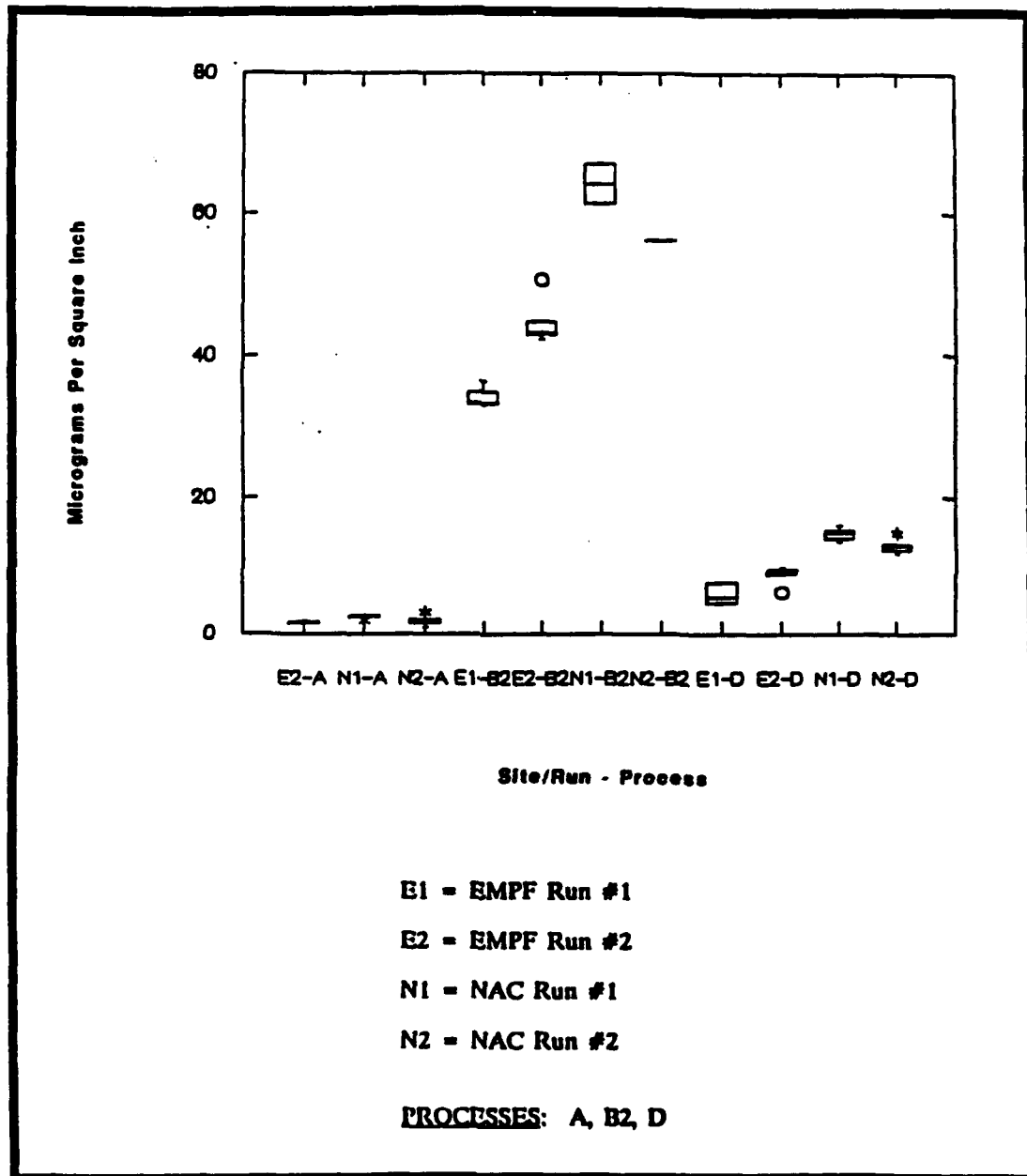


**FIGURE 4. BENCHMARK IONIC CLEANLINESS TEST COMPARISON
OF PROCESSES, A - B2 - D.**

boards during the first test run of B1.

The higher readings noted in the B2 Group were attributed to the EMPF using a foam flux system which deposits less flux on the board than a wave flux system such as the one used at NAC.

Residual Rosin Testing. Residual Rosin Testing was performed using an ultraviolet spectrophotometer. The procedure included mixing a set of standards made from the same type of flux (Kester 1585 MIL RA type), and measuring the absorbance readings at 242 nanometers (nm). Rosin contamination from the test boards was then dissolved in isopropyl alcohol and absorbance readings were compared to these standards. The extraction procedure for removing the rosin residue from the test sample consisted of placing the board into a sealed plastic bag with 100 milliliters (ml) of isopropyl alcohol and manually shaking the bag for 10 minutes. The results of the Benchmark are shown in Figures 5 and 6.

Once again, NAC's first test run results from the residual rosin test showed that higher amounts of contamination were being deposited on the boards. Although Group A was not exposed to any rosin contamination, samples taken from this group gave low absorbance readings. These readings were attributed to other materials extracted from the bag and/or the bare board that absorbed at the same wavelength as rosin.

During testing not all of the contamination was being removed in ten minutes. To gain insight into how much contamination was actually on the board, NAC added an extended contamination testing to their second test run. This testing consisted of submersing the bag in an ultrasonic tank for an additional 20 minutes. The results of the additional soaking time are shown in Figures 5 and 6, and are labeled N2-EX- B1 and N2-EX-B2. The additional NAC testing, and the difference in data obtained from the EMPF and NAC, provided evidence that made the extraction procedure questionable.

Results from Groups B2 and D testing showed the EMPF runs as comparable to each other and the NAC runs as comparable to each other. The difference between the NAC runs and the EMPF runs can be attributed to the difference in flux systems as described earlier or the extraction procedure.

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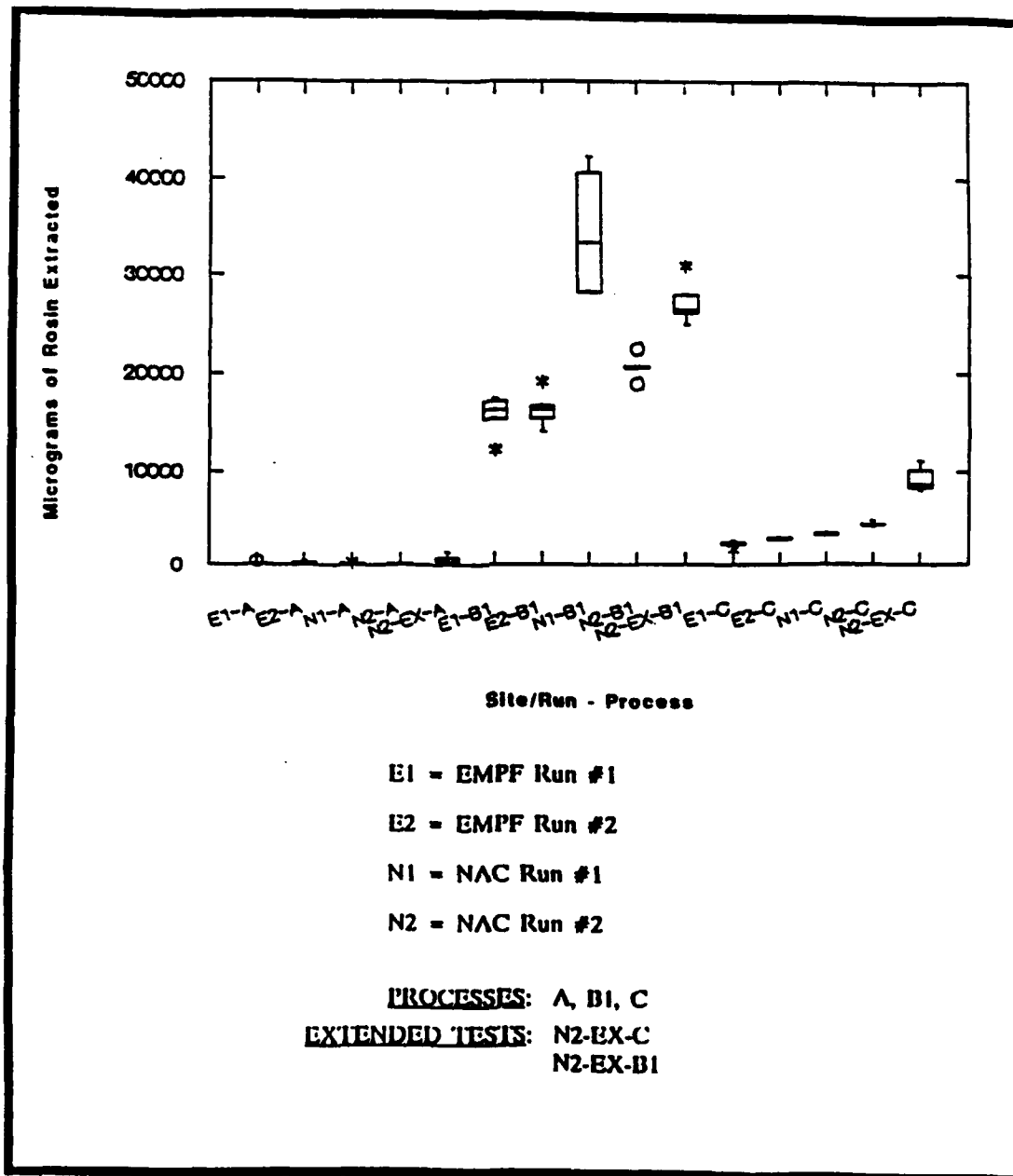


**FIGURE 5. BENCHMARK RESIDUAL ROSIN TEST COMPARISON
 OF PROCESSES, A - B1 - C.**

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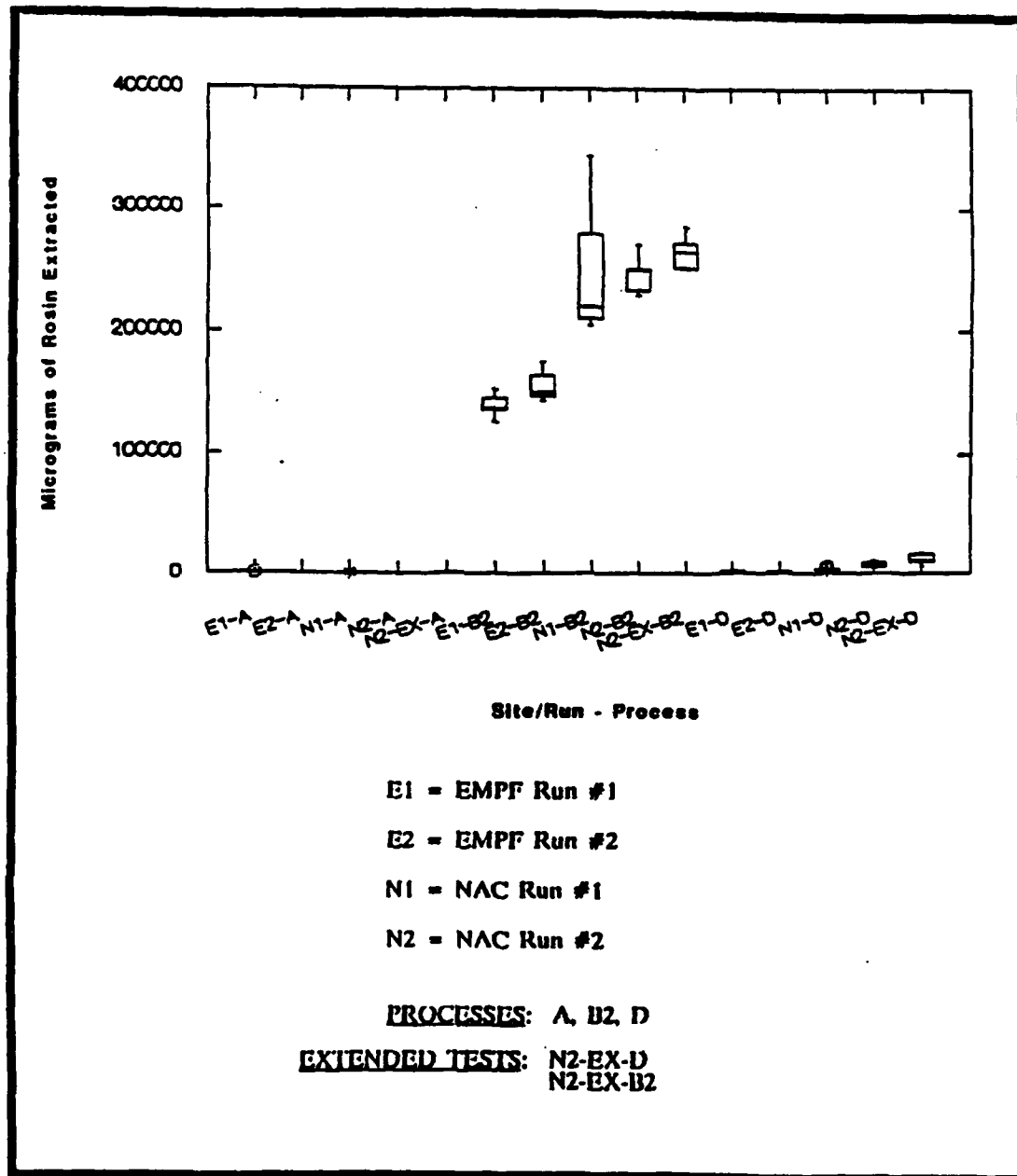


**FIGURE 6. BENCHMARK RESIDUAL ROSIN TEST COMPARISON
OF PROCESSES, A - B2 - D.**

To ensure accuracy of the test, a separate test was conducted at the EMPF after the Benchmark testing was complete. The test changed various steps in the procedure used in Phase 1 to determine if it could be made more reproducible and accurate. A 1- by 1-inch brass plate with a 0.008 inch channel machined into one side was used in place of a component. The plate was bolted to a 2- by 3-inch piece of FR-4 laminate material and was easily removed to measure any residue. The amount of rosin was calculated based on a weighed amount of flux placed in the channel of the plate (See Figure 7). The brass plate with the flux was then placed into an oven and baked for ten minutes at 100°C. After cooling to room temperature, the brass plate was bolted upside down to the laminate material (See Figure 8) and tested for the efficiency of each technique at removing rosin from tight spaces.

The first test coupons were set up and tested using the same technique as in the Benchmark test. The results of this test proved that approximately 70% of the total flux was being removed from under the plate.

Because only 70% of the contamination was removed, the intensity of the manual shake was changed. A more vigorous shake increased the removal of flux to approximately 80%, but the bags began to leak. The bags that developed leaks imparted high readings which were caused by the same amount of rosin being dissolved in a smaller volume of isopropanol. Since the problem with the bags was also experienced during the Benchmark testing, the procedure was changed to no shaking and extended dissolving time. This procedure also proved inadequate as only approximately 50% of the residue was removed even after one hour of soaking.

Testing thus far proved that a manual type of agitation had introduced too much of a variable. An alternative variable to manual agitation was to dip the plastic bag containing the board and the isopropanol into a tank of water and use ultrasonics as a form of agitation. However, as isopropanol is lighter than water, it floated to the top of the plastic bag in a bubble and very little isopropanol remained around the board to dissolve the rosin. The next variable was to change the ultrasonic median from water to mineral spirits, a material with a specific gravity similar to isopropanol. The mineral spirits, combined with the ultrasonic cavitation, weakened the bag to the point that the mineral spirits contaminated

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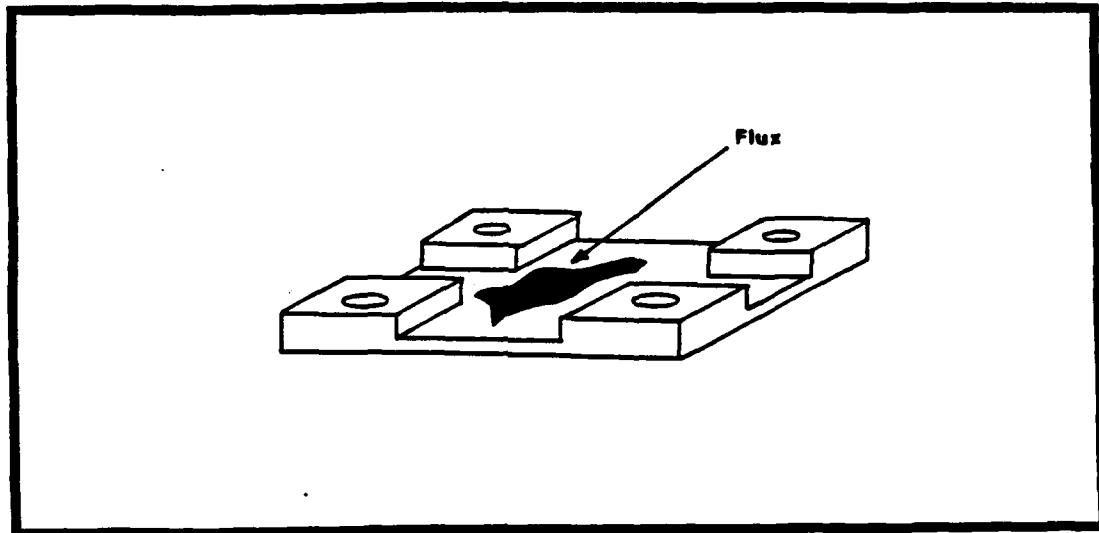


FIGURE 7. BRASS PLATE.

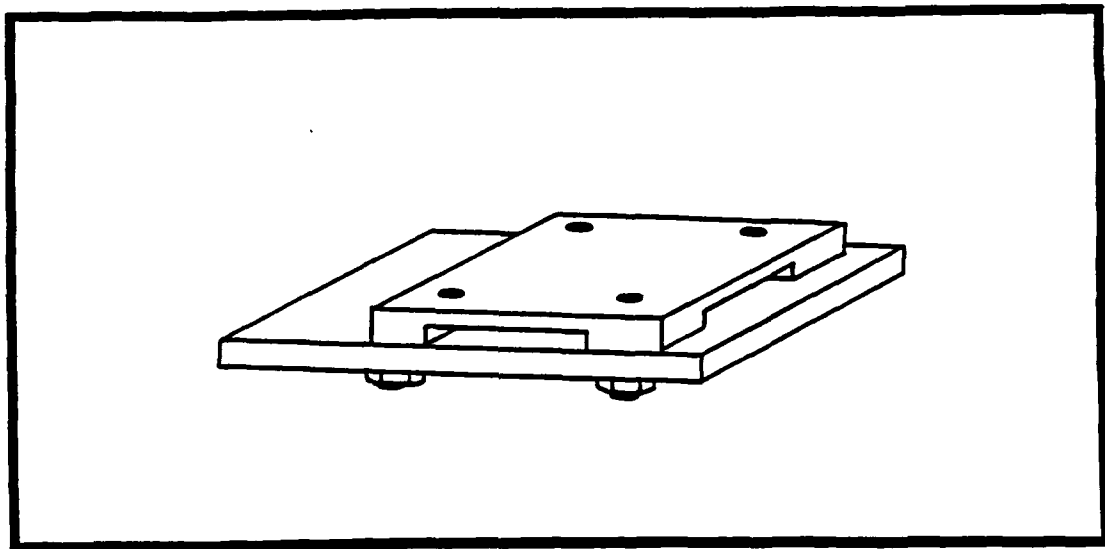


FIGURE 8. BRASS PLATE ASSEMBLED ONTO LAMINATE.

the sample.

Many of the problems encountered during testing were attributed to the plastic bag, so a stainless steel tank was manufactured to replace the bag during the ultrasonic process. With the tank, testing yielded the best results with a mean of 97.3% removal and a standard deviation of 1.13.

White residue was another problem encountered during the residual rosin portion of Phase 1 testing. To remedy this problem, a solution of 1.0% phosphoric acid, 0.1% water, and 98.9% isopropanol was substituted for straight isopropanol. The results of this test showed that the white residue problem was eliminated; however, the removal of baked on rosin was slowed considerably.

Surface Insulation Resistance Testing. Surface Insulation Resistance (SIR) testing measured how much ionic contamination remained on the boards by measuring the electrical current resistance between circuit traces. An RA type flux was being used, and any trace of an activator should have been easily measured. However, when Benchmark testing was completed test results showed high resistivity on most of the boards.

Two hypotheses were submitted. The first hypothesis was the possibility that no flux was reaching the topside of the boards; therefore, no flux was present on any of the test points. The second hypothesis was that the rosin, being an insulator, encapsulated the activator and test points, which resulted in high resistance readings.

The EMPF performed a test that decided which hypothesis was correct. The SIR test equipment was set up and 20 CFC boards were cleaned and tested for cleanliness in the Omegameter. Ten of the boards were dipped into a beaker of Kester RA flux and allowed to drip dry for approximately 20 minutes. All 20 boards were then plugged into the test equipment and placed into the humidity chamber. Testing was conducted the same as during the Benchmark.

Results from the SIR test did not distinguish which boards had the flux and which did not. These results affirmed that the rosin was encapsulating the activator and the test points.

SIR testing is presently incorporated in the Phase 2

test plan, but only for reference and not as pass/fail criteria. There are two reasons for retaining SIR as part of the test plan. One reason being that an alternative solvent may selectively remove the nonionic rosin, but leave the ionic activator. Secondly, that an alternative solvent may degrade a board's surface, and lower its SIR values.

Phase 2

In Phase 2 testing, an alternative solvent, which is less harmful to the ozone will be evaluated. The test procedure used in Phase 1 is repeated in Phase 2, but substituting the CFC solvent with the alternative candidate. Cleanliness results from the new solvent will be compared to results obtained during Benchmark testing to determine if the alternative candidate cleans as well as the CFC solvent.

The alternate solvent scheduled for testing at the EMPF in mid January is Petroferm Bioact EC-7. Bioact EC-7 is a terpene based solvent which is classed as semi-aqueous. Semi-aqueous indicates that a two-stage cleaning process is required using water as the second stage. Since terpenes require special cleaning equipment, the EMPF could get the equipment on loan and not have to invest large amounts of money.

Terpenes have great potential to replace CFCs because they have good rosin dissolving characteristics, are non-toxic, biodegradable and have a zero ozone depletion potential (ODP). Waste water treatment facilities are set up for handling terpenes as many are already being used in commercial cleaners.

The terpenes' capability to clean has long been recognized. However, terpenes have not been used in the past because of flammability problems such as a low flash point, a low Lower Explosive Limit (LEL), and the stability and availability of CFCs.

The Montreal Protocol has forced the electronics industry to overlook CFCs and solve the flammability problems. The flash point is the level at which a solvent gives off a vapor significant enough that a spark could ignite a fire. As terpenes do not have to be heated to work, the problem could be avoided by chilling the terpene

and maintaining its temperature below the flash point. In contrast, the LEL is the amount, that if present in the air as a mist or splash, a spark could ignite a fire or an explosion. To develop a cleaning process that does not splash or create a mist is difficult. New equipment has been developed to handle terpene solvents and are presently being marketed.

Phase 2 is designed so other facilities can test materials. A Test Method Validation Team (TMVT) can be scheduled through the Institute for Interconnecting and Packaging Electronic Circuits (IPC) to monitor any testing with alternative solvents. Firms such as Allied Signal and Martin Marietta are already working on potential replacements for CFCs. Such research promises alternatives by the end of 1990.

Phase 3

Phase 3 testing is still in the planning process. This phase will evaluate water soluble fluxes, low solids fluxes, and inert atmosphere soldering processes. New types of problems need to be addressed, such as how to categorize fluxes, setting up a standard cleaning process, how to measure cleanliness, how clean is clean, and how the results can be compared to the original Benchmark results. In addition to these problems, a reliability issue from using these materials needs to be addressed. SIR testing will be helpful in this phase more than in the first phase, but there is a need to determine a pass/fail limit. Residual rosin testing will be useless in Phase 3, so a need exists to develop a test to replace it.

Ultrasonics

The EMPF is researching the use of ultrasonics for cleaning military hardware. Phases 1 and 2 of a three phase project have been completed and a copy of the report is available through the EMPF. Testing of Phase 3 has begun and it will compare cleanliness results of boards cleaned in ultrasonics to those cleaned using conventional methods. In addition, the functional boards will be tested for degradation of components and visual deficiencies. The boards will then be subjected to environmental testing (thermal shock, cycling, humidity), power cycling and vibration. When the stress tests are completed, the

boards will be tested again for functional degradation of the components. Finally, wire bonds will be pull tested and compared to military specifications to determine if they meet the standards.

SUMMARY

CFCs are slowly being phased out and a need exists to find alternative cleaning solvents. The persons involved in the initiation and signing of the Montreal Protocol were aware that a reduction in CFC based products would not be an expedient process. Companies are experimenting with alternative cleaners and the Department of Defense also recognizes the need to reexamine the use of alternate fluxes, soldering processes and cleaning processes. However, care must be taken to avoid accepting a solvent that jeopardizes other environmental factors as a trade-off.

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AQUEOUS CLEANING AND IONIC RESIDUE TEST SYSTEM A TECHNICAL BRIEF

BY

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ABSTRACT

Aqueous removal of rosin fluxes from PWBs through saponification has been used for a number of years. Batch systems which use this process have been perfected to the point where they not only clean but measure and record wash parameters such as rinse water resistivity and temperature. Heretofore a direct correlation between final rinse resistivity and Mil-P-28809 method cleanliness test results was difficult to achieve due to differences in ion behavior in water vs. water/alcohol mixtures. To overcome this short-coming, the Model 7300 system incorporates a water/alcohol test cycle following cleaning. Operator safety is assured through the use of a nitrogen inerting system and cleaning process test results are documented on a built-in printer. This system 100% tests all boards while maintaining throughput in excess of 500-1000 assemblies per shift.

Cleaning and Testing in One System

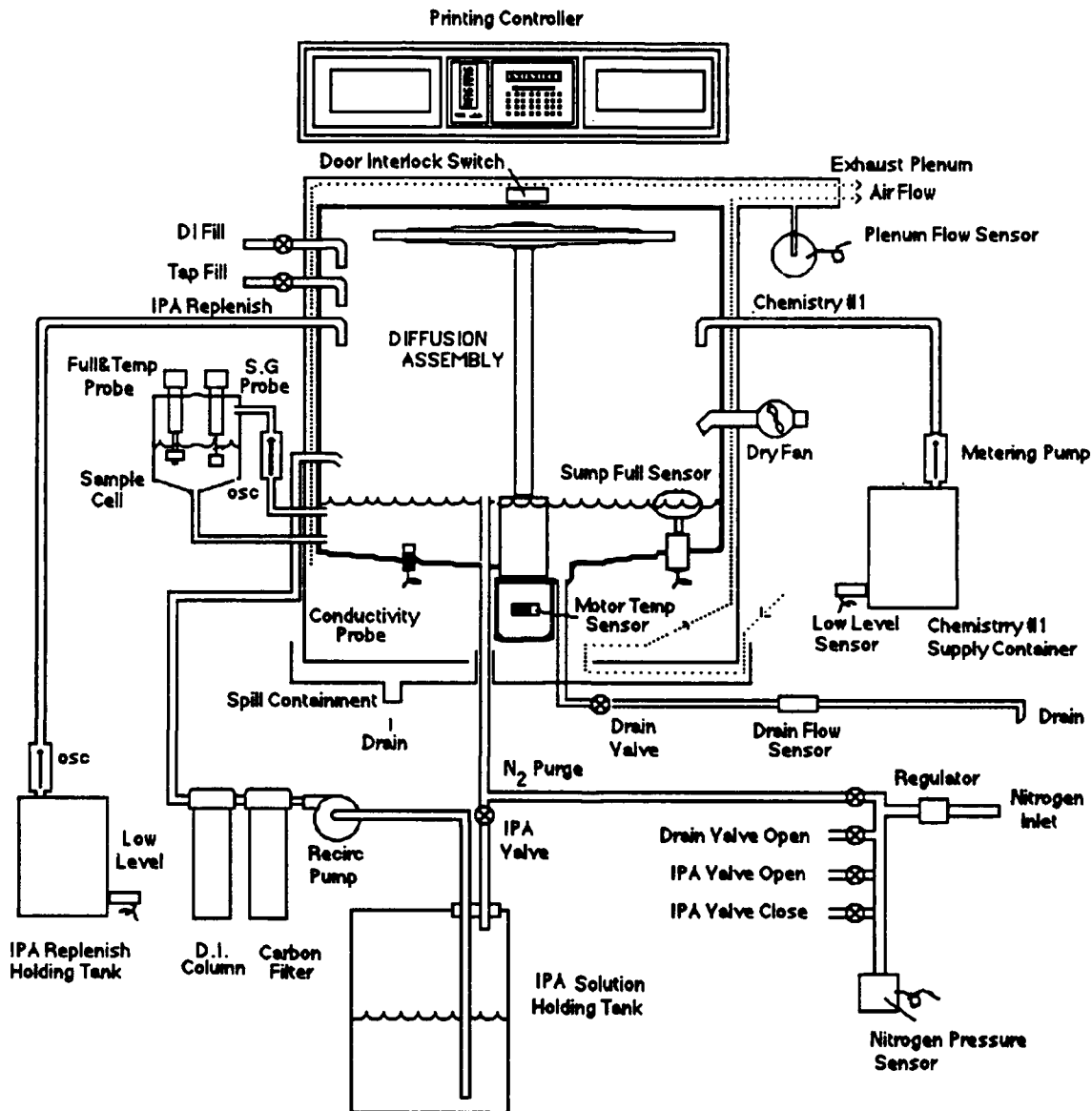
The Alcohol Clean and Test System provides fast, economical removal of rosin or water-soluble fluxes and associated contaminants from SMD assemblies. In addition, the Alcohol Clean and Test System performs a batch cleanliness test that ensures conformity with the MIL-P-28809 resistivity test method without separate costly and time-consuming single-board testing.

Total Programmability

The Alcohol Clean and Test System's control unit monitors and controls all cycle functions, including pre-rinse times, wash times, and rinse and dry cycles, chemistry concentration, and the testing cycles. All programming is done by the operator, who enters the lot number and the cycle parameters on the controller's front panel.

While operating, the controller indicates the current cycle status on the easy-to-read LED display. During the cycle, the Alcohol Clean and Test System prints the wash time, the number of rinses, the temperature of the water used, the percentage of chemistry added, the length of the cycle, resistivity readings, and the lot number with the current day and time.

Another feature of the system is the Smart Sensor Package, standard with the Alcohol Clean and Test System. The Smart Sensor Package features a water level sensor for quick and accurate filling and a drain-flow sensor that reduces cycle times to allow for greater throughput. The Smart Sensor cuts process time by as much as 25% compared to ordinary fixed-time controllers.



Batch Mil-Spec Testing -- How It Works

Once the rosin saponification and water rinsing cycles are complete, the system controller empties the wash chamber and pumps in the standard test solution (75% alcohol, 25% water). The assemblies are rinsed in the test solution for 15 minutes. Final resistivity must exceed 2 megohms-cm or the batch is rejected. After testing the test solution is returned to its container, the assemblies are air dried and the system is ready for the next load.

The test solution is continuously monitored for specific gravity to determine the need for automatic alcohol addition. The alcohol/water test solution is contained in a holding tank under the washer, and the solution is

continuously circulated through a deionizing column to remove ionic contaminants.

Designing for Safety

Because the test solution contains alcohol, safety has been an important design criterion in the development of the Alcohol Clean and Test system. In case of power loss, the solution flows back into the container. Nitrogen is used to purge the wash chamber, thus reducing the oxygen content and the flammability of the contents. The pressure of the nitrogen supply is constantly monitored to provide additional protection.

To keep the air in and around the system free of flammable fumes, air is pulled in from the bottom periphery of the machine, moved up around the wash chamber and exhausted out the top. Air vacuum sensors monitor the air flow and automatically shut the system down in case the air flow is interrupted. Accurate temperature monitoring has been designed in to make sure that the temperature of the contents of the wash chamber and sump is maintained well below critical. The temperature of the main drive motor is also monitored continuously, and the motor automatically shuts down if the maximum temperature is exceeded.

Batch Versus In-Line Cleaning Systems

One of the main advantages of a batch cleaning system like the Alcohol Clean and Test System, is process control. Another is the flexibility in setting and adjusting process time for optimum results. While the cleaning time in an in-line system, for example, is governed by the rate of the overall process, the batch cleaner can be independently controlled. The cost of acquiring and operating a batch system versus an in-line system has been well-explored and documented. Aside from exceptionally long runs, the costs of the batch system are always significantly lower. Unit costs per year are usually lower, especially if two or more batch systems are used, since they can normally be handled by a single operator. Capital outlay is, of course, much less, and energy use for providing hot DI water is in the range of half or less of in-line.

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Rex attended Oregon State University School of Electrical Engineering and has 25 years' experience in the design and manufacture of electronic instrumentation for the medical and industrial processes. His early work involved development of electronics for kidney patient hemodialysis machines. Recent work has focused on the areas of batch aqueous and cleaning solder process temperature profiling of electronic assemblies.

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RESIDUE FREE, CLEAN REFLOW SOLDERING FOR SURFACE MOUNT TECHNOLOGY

by

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ABSTRACT

In surface mount assembly, (RMA) flux residue has been cited as a cause of decreased circuit life and poor surface insulating resistance. Conventional chloro-fluorocarbon (CFC) cleaning solvents used to remove RMA flux residue, create severe environmental problems and hence there is an industry commitment to eliminate CFC materials.

The BOC Group Technical Center has developed a process whereby electronic components are reflow solder attached to printed circuit boards using a reactive fluxing atmosphere and a non-rosin based solder paste. Any trace residue is invisible to the naked eye, is noncorrosive, and is benign to the circuit's metallurgy. Post solder cleaning is not required.

This paper describes the development of the process and its successful implementation at a major electronics manufacturing site, by a collaborative effort between Airco Gases, Multicore Solders, BTU Engineering, with the BOC Group Technical Center.

INTRODUCTION

Typically, mildly activated rosin (RMA) based solder paste is used for surface mount productions. When the boards exit the reflow oven or the vapor phase reflow machine, a significant amount of residue is observed at the older joints. Because this residue contains ionic constituents which can cause shorting and product failures over time, it must be removed after the reflow operation. Chlorofluorocarbon (CFC) solvents are commonly used, most notably, CFC-113.

CFCs do an excellent job of cleaning surface mount assemblies because of their ability to penetrate into small openings underneath the devices. Because of environmental consequences attributed to the release of CFCs into the atmosphere, however, many nations have restricted the use of these solvents, with eventual phase out by 1992.

PROCESS DEVELOPMENT

The development of the no-residue surface mount assembly process derived from a technical assistance request from the Airco Gases company of the BOC Group. An Airco customer who manufactured a complicated microwave frequency assembly, employed a solder alloy preform but could not use a liquid flux in securing a final component to the circuit. Consequently, in order to promote surface wetting above the preform's liquidus temperature, the point of attachment had to be manually scraped to remove the surface oxide from the base metal before depositing the preform. The Group Technical Center was asked to recommend a fluxing atmosphere which would eliminate the need for manually scouring the attachment site before I-R reflowing the preform.

An investigation into reducing the metal oxides associated with this situation was undertaken, and the results published in Reference 1. During this work, it was proposed that we develop a process which would eliminate liquid solder fluxes from all SMT operations, including those which utilized on solder pastes. In doing so, it was reasoned that post solder cleaning could be eliminated.

For a process suitable for high-yield, high-volume soldering, four major criteria were designated for success: delivery, solderability, appearance, and reliability.

Already there were several no-clean solder pastes targeted for SMT, being promoted to the marketplace. As a start, these were evaluated in our laboratory and were all found to be deficient in one or more of the requirements. Rheological properties varied, from a paste which could not be stenciled, to one which slumped very badly and had virtually no tack. Solderability was generally quite poor, but improved if a nitrogen atmosphere was used in place of air. The residue, however, was considerable, unsightly, and tacky, which in the opinion of the BOC researchers was unacceptable for a commercial SMT operation. Reliability testing was not considered at this time since no viably acceptable assemblies were produced with any of these pastes.

Solder Paste Development

Liquid fluxes in paste formulations do more than merely scour oxides from the metal surfaces to be joined. The fluxing agents also function as a vehicle for delivering the powdered solder alloy to the attachment site, hold the solder powder in place, and maintain the components in proper alignment with the pads on the board during the thermal cycle.

Rosin acts as both a flux and vehicle in conventional RMA pastes. If the rosin is removed from the formulation, and it is assumed that an active atmosphere will provide the necessary fluxing action, a vehicle will still be needed that provides the necessary rheological features for deposition and holding the components in place.

Our first task was to identify a liquid vehicle which would perform all the conventional duties except fluxing. A reactive gas atmosphere would do this instead. The chosen vehicle successfully passes such characterization tests as the copper mirror and surface insulation resistance tests, described in Reference 2. No evidence of corrosion was observed in the copper mirror tests after 10 days at 35 °C and 90% RH. In the surface insulation resistance measurements, the vehicle was painted on interdigitated comb conductor patterns and processed in the controlled atmosphere at the solder reflow temperature. All uncleaned samples had SIR values in excess of 10×10^{11} ohms, closely approaching the values measured on the unprocessed control patterns.

Even though this vehicle system is benign to the circuit's materials, it is desirable to eliminate residues for aesthetics and testability. Visible residues are objectionable to many users, and flux residues can hinder bed of nails testing. Therefore, another requirement of our vehicle was the ability to depolymerize at the reflow temperature by reaction with a second gaseous component in the fluxing atmosphere. If such a vehicle-depolymerizer couple could be found, the reaction products would be fugitive, thereby eliminating the traditional vehicle residue. In short, the cleaning of SMT paste residues could be eliminated.

Formulation of a no-residue solder paste that would reflow in the presence of a gaseous fluxing agent, required a solder alloy powder having low surface oxide and carbon contamination. Most metal powders have their bulk oxide content specified, i.e. < 0.5%. If however all of this oxide resides on the particles' surfaces, then the surface concentration can be considerable. Another requirement was that the powder be spherical with a narrow particle size distribution.

For the initial paste formulation work, a solder composition of 63Sn/37Pb and mesh -200/+325 was chosen. The powder was argon spray atomized and packaged under argon in order to minimize surface oxide formation. As an additional precaution, powder weighing and mixing with the vehicle were conducted under a protective nitrogen atmosphere.

Reflow Atmosphere Development

Formulations of candidate pastes were made using the oxide free solder powder with various vehicle systems that were reasonably expected to depolymerize within the established atmosphere in the proximity of the reflow temperature. The reflow characteristics and depolymerization reactions of these pastes were screened on copper

test coupons for different atmosphere compositions, in a Cahn 131 thermogravimetric microbalance, or TGA.

Copper test coupons (10 x 30 mm) were prepared by dipping coupons into 0.5 N HCl, then immediately washing with distilled water to remove acid. Coupons were then exposed to ambient air in the laboratory for five days to allow the surfaces to mildly oxidize. The prepared test coupons were then stored under nitrogen until needed.

A net 0.05 g of the solder paste was placed in the microbalance on a mildly oxidized copper coupon. After purging the muffle with nitrogen for 15 minutes, the controlled atmosphere was established, comprising the fluxing and depolymerizing components in nitrogen. The samples were heated at the rate of 100 °C/minute, up to a peak temperature of 250 °C, then cooled to room temperature at the same rate.

After the initial screening, selected pastes and atmosphere combinations were studied in a Five Star bench top I-R oven. The oven was fitted with a specially designed quartz muffle, 254 mm x 279 mm x 25.4 mm, in order to perform the reflow tests under a controlled atmosphere condition. The temperature ramp was maintained to approximate a heating profile in a continuous mesh belt I-R oven, and monitored using a thermo-couple placed in contact with the sample. For these reflow tests, 2.54 mm diameter solder pads were stencil printed on the mildly oxidized copper coupons, which were used to simulate the base metal of a PWB.

LABORATORY RESULTS

In all the TGA weight loss measurements, the initial weight loss was observed at 70 °C which is in the boiling range of the organic solvent. Secondly, the slopes of all the curves in the temperature range, 70-200 °C, is very steep and correspond primarily to the rapid loss of the solvent.

In the case of the nitrogen atmosphere, the entire weight loss is attributed to the solvent alone. By comparison, the mixed atmosphere indicates a greater weight loss, due to the reaction of the polymer thickener with the atmosphere. The reaction by-products are lower in molecular weight and thus fugitive at the reflow temperature. Visual inspection of the copper coupons confirms this. For the nitrogen processed coupon, a thick, non-tacky, amber colored residue was evident in the form of globules on the solder surface, but not on the copper. The surface wetting was judged marginally acceptable. But for the coupon processed in the mixed atmosphere, the solder surface was clean, as well as that of the copper. In this case the surface wetting was judged excellent.

It should be noted that the weight loss of these pastes when heated in air, is essentially the same as the weight loss measured for heating in nitrogen. The solder, however, does not flow and wet the copper surface when air is present.

Solder joints were evaluated for mechanical strength by pulling a 20 gauge copper wire soldered to 2 mm x 2 mm copper thick film pads on alumina substrates. An ETP vertical pull tester was used. The joint integrity was further investigated through metallographic examination of cross-sections for the presence of void spaces. For control purpose, a conventional RMA paste was processed in the same manner except that air, rather than the mixed atmosphere was used as the process environment.

The results showed that the joints produced by the no-residue process were consistently comparable or better than the joints obtained by standard reflow practice.

FIRST COMMERCIAL DEMONSTRATION

During the final stage of the laboratory work, Airco Gases organized a full scale demonstration with a major manufacturer of electronic communications equipment. In order to implement the new process, this manufacturer purchased an 18 inch mesh belt I-R soldering oven from BTU Engineering, specially modified to accommodate the reactive atmosphere used in this process.

Meanwhile, evaluation of the solder paste's rheological properties by established methods (Reference 3.) revealed several severe deficiencies important to high-volume stencil printing operations, and tackiness was unsuitably low (Reference 4.) too. Reformulation efforts by our laboratory could not correct this situation within the time constraints imposed by the commitment to commercialize the process. It was now evident that we needed some real expertise in solder paste technology on the team.

Collaboration with Multicore Solders

After the need for collaboration was acknowledged, the laboratory results were presented to Multicore Solders with an offer to form a cooperative effort for commercializing and further developing the process. This proved to be a timely move, for after the commercial trial was begun, several iterations of reformulation were necessary to meet all the customer's criteria for success.

Electronic packages were constructed with Sn62/Pb36/Ag2 no-residue solder paste supplied by Multicore, pretinned circuit boards (polyimide and FR-4), and various surface mount components provided by the electronics manufacturer.

Circuit boards were printed with the solder paste on an AIM/Presco vision printer system. Components were then placed into position with a Panasert pick and place machine. The assembled boards were next conveyed to the 18 inch BTU soldering oven for reflow in the reactive atmosphere. The oven's atmosphere was produced from bulk gasses supplied by Airco Gases. Three individual components were mixed, then partially reacted in a catalytic converter to produce a fourth, reactive species.

The overall flow rate for the BTU unit was 39 000 liters per hour. Through three injection tubes, 20 400 liters per hour of blended atmosphere were introduced into the heated zones. The balance of the unit's flow was nitrogen for inlet and outlet curtains and eductors (Figure 1). The oxygen level inside the oven was maintained below 20 ppm, as determined by a Teledyne Model 311 oxygen analyzer. Other gas constituents of the proprietary gas blend were monitored and controlled to within $\pm 2.5\%$ of their target values.

The minimum flow to the oven was determined by monitoring oxygen at two points along the length of the heated section. One atmosphere monitoring point was located in the soak zone and the other was located in the peak temperature zone. In addition, detectors were located at the oven's inlet and outlet to indicate if any of the mixed atmosphere should diffuse through the nitrogen curtains. The balance between oxygen incursion into the oven and mixed atmosphere outward diffusion, was struck at the minimum possible flow by adjusting the venturi nitrogen supply for each eductor, the nitrogen flow to the curtains, and the mixed atmosphere flow. A number of iterative adjustments were made until the lowest overall flow was achieved for maintaining the desired atmosphere composition inside the oven.

Oven heating was provided by two I-R lamps per zone, top and bottom, while six thermocouples per zone (left, center, right, for both top and bottom) were used to monitor temperature. Temperature control was $\pm 2^\circ\text{C}$.

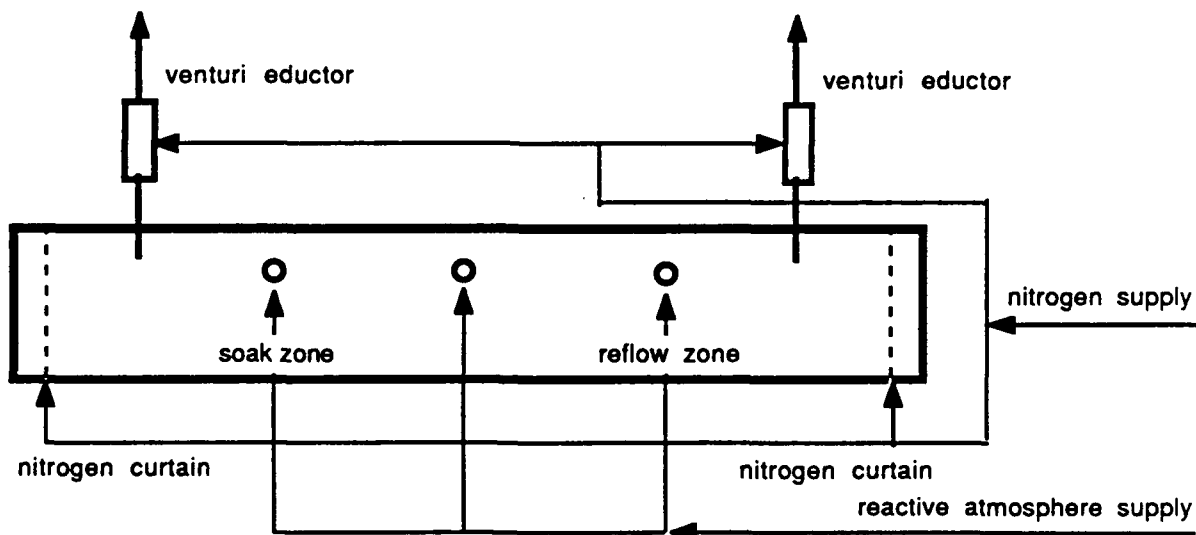


FIGURE 1. Gas Supply Schematic Diagram for the BTU I-R Reflow Oven

It was found that the temperature could be affected by certain flow and atmosphere conditions. For instance, high flow rates through the injection tubes could create hot spots, particularly on the bottom. The atmosphere entering from injectors located along the top of the oven would act as a heat sink, creating an undesirable thermal gradient in the unit. Once the proper flow conditions were established, the I-R oven performed flawlessly. A typical temperature profile is shown in Figure 2.

The processed board assemblies were inspected for cleanliness, solder joint wetting, and functionality. They were then introduced into the accelerated life test cycle, which included time at elevated temperature and humidity, drop tests, and more of the functional tests. This cycle was repeated a specific number of times.

During the production trial, a number of material changes were made in order to accommodate particular needs of the manufacturer. New formulations of the solder paste were batched by Multicore's laboratory in Hemel Hempstead, England, shipped to BOC's laboratory in Murray Hill, New Jersey, for I-R reflow characterization, then selected pastes were shipped to the manufacturing site where the Airco engineers used them to solder the trial boards. Parameters such as wetting, printability, viscosity, slump, solids concentration, tack time, stencil life, solder ball formation, and residue were determined during each material change.

Wetting behavior was evaluated by reflowing selected components onto trial boards in the Five Star reflow oven. The presence of solder balls was determined by visual inspection of the reflowed boards. Room temperature slump was measured with an ETP linear gauge and viscosity with a Brookfield viscometer. Tack time was determined by placing components onto boards with stenciled paste. The boards would then be inverted after standing for one hour under ambient conditions. If components did not stay in place, the paste failed. Stencil life was measured by allowing the paste to stand on the stencil over a period of time. At 1 hour intervals, a print would be made. If the pattern was able to be printed, the paste was considered acceptable. Residue characteristics were determined with a Cahn 131 TGA. Paste samples were heated in the reflow atmosphere mix, and the weight of organic residue remaining with the solder alloy was obtained.

The first boards were manufactured with PASTE A1. The printing technique used was print-return. This required the paste to be cohesive enough to be dragged back by the squeegee and adhesive enough to stay on large area pads. The paste would print 25 mil pitch pads but performed marginally in this printing technique. The paste was also rated unacceptable by the manufacturer for slump, tack, and wetting. These characteristics are summarized in Table 1.

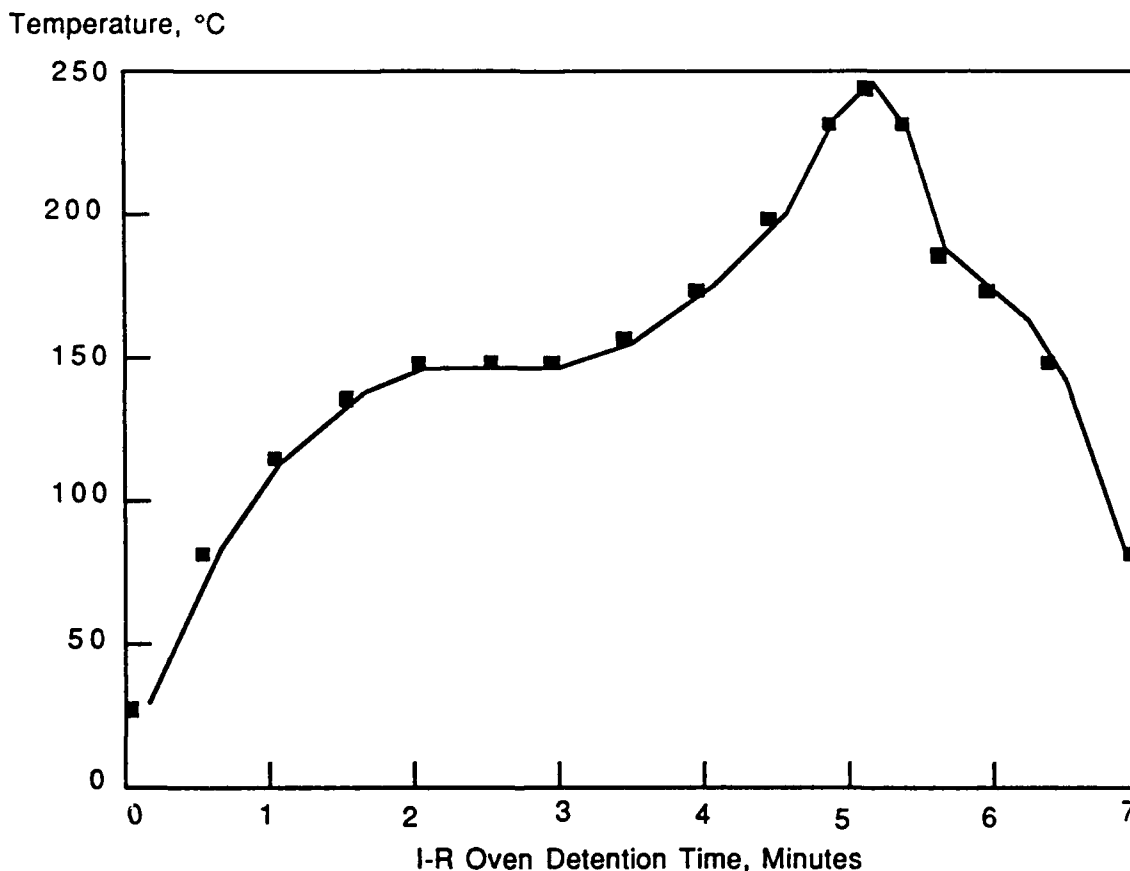


FIGURE 2. Reflow Oven Temperature Profile.

Immediately after printing, slumping could be observed visually. During placement of components by the pick and place machine, certain components shifted slightly. In addition, one type of component in the assembly, an SOT, could not be adequately wetted. Laboratory analyses of these SOTs revealed their leads to be inadequately pretinned and somewhat oxidized. Nevertheless, these components were being successfully soldered in a parallel operation, employing an RMA paste, and the manufacturer expected the new process to perform equally.

In an effort to improve PASTE A1's wetting behavior, changes in the temperature profile and atmosphere composition were attempted. These process changes only gave marginal improvements. In all cases, however, there was no visible residue on the solder joints.

TABLE 1. Solder Paste Performance Results

<u>Paste</u>	<u>Slump</u>	<u>Tack</u>	<u>Print</u>	<u>Wetting</u>	<u>Balls</u>	<u>Residue</u>
A1	U	U	B	U	A	A
B1	B	U	A	U	A	A
B2	B	U	B	A	A	B
C1	A	A	A	A	A	A
C2	A	B	A	A	A	B
D1	A	A	A	A	A	A
D2	A	A	A	A	A	A

A = Acceptable, B = Borderline, U = Unacceptable

The next trial was performed with a series of PASTE B formulations. As shown in Table 1, PASTE B1 gave improved wetting, plus enhancements in printing and slumping behavior. On the negative side, this paste had poor tack and tended to loose solvent during extended production runs. But as before, no visible signs of residue remained on the solder joints.

PASTE B2 was formulated to promote wetting on nickel based surfaces. This indeed did wet all the components satisfactorily, and provided a long stencil life too. There was, however, a small amount of visible residue which remained on the solder joints. The BOC laboratory prequalification of this paste indicated that the joints should be residue free. This problem was eventually resolved on site by slightly increasing the preheat time and temperature.

But still, all was not right with PASTE B2. Previously, there was no indication of slumping with the basic vehicle composition. Printing on fine pitch, 25 mil pads, was acceptable. Larger pads presented problems. The paste did not adhere well to the larger pads and was removed upon the squeegee's return stroke. Because pad adhesion was poor, tackiness was also found to be inadequate, as would be expected.

Analyzing the B series trials, it was evident that PASTE B1 provided all the necessary printing properties and PASTE B2 contained all the wetting properties. A combination of the properties given by these two individual pastes would be required in

one single paste which would be user acceptable. Thus, a C series of pastes were formulated, based on the previous results.

Both PASTE C1 and PASTE C2 exhibited the desired characteristics and could be used in the production of surface mount assemblies which do not require post solder cleaning, as shown in Table 1. Even though all criteria were met for a high yield, high production rate paste, a fourth and final series of pastes was constructed to further optimize the process.

The TGA analyses of the different paste formulations (Table 2) reveal the maximum weight loss of organic vehicle was achieved with PASTE D1 and the reactive atmosphere. This paste also exhibited excellent wetting and rheological properties. Functionally, PASTE D2 was similar to PASTE D1.

TABLE 2. TGA Analyses of Solder Pastes
Reactive Atmosphere vs Nitrogen

<u>Paste</u>	<u>Sample Vehicle Weight*</u>	<u>Weight* Loss Nitrogen</u>	<u>Weight* Loss Rctv. Atm.</u>	<u>% Weight Loss Nitrogen</u>	<u>% Weight Loss Rctv. Atm.</u>
A1	5.00	3.81	4.54	76.2	90.8
B1	4.90	4.06	4.26	82.9	86.9
B2	4.80	4.12	4.22	85.8	87.9
C1	4.55	3.58	4.04	76.7	88.8
C2	4.55	3.84	4.09	84.4	89.9
D1	4.75	3.99	4.46	84.0	93.9
D2	4.85	3.88	4.30	80.0	86.7

* g x 10⁻³

CONCLUSION

A novel solder reflow process was conceived and functionally demonstrated at the BOC Group Technical Center. This was subsequently commercialized in a major electronics manufacturing facility in the United States, by Airco Gases, with assistance from BTU Engineering. During the trial, refinements in the solder paste composition were made by Multicore Solders.

The solder joints made by this proprietary process showed excellent joint strengths and met all the criteria for ionic cleanliness (MIL-P-28809) and surface insulation resistance (IPC-A-600) without cleaning. Circuit boards manufactured by this process are comparable to circuit boards manufactured with standard RMA pastes and subsequently cleaned by CFC solvent.

REFERENCES

1. Bandyopadhyay N., Kirschner M., and Marczl M., "Development of a Fluxless Soldering Process for Surface Mount Technology," Journal of Surface Mount Technology, Vol. 2, No. 4, October (1989), pp. 10-19.
2. "General Requirements for Electronic Grade Soldering Fluxes," IPC Standard IPC-SF-818, Institute for Interconnecting and Packaging Electronic Circuits, Lincolnwood, IL, 1987.
3. Morris J.R., Wojcik, T., "Stencil Printing of Solder-Paste for Fine-Pitch Surface Mount Assembly," Ninth IEPS Proceedings, September 1989.
4. Morris J.R., "Solder Paste Tackiness Measurement," Brazing and Soldering, No. 14, Spring 1988, pp 34-37.

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**ESCA ANALYSIS OF AGEING OF METALLIC SURFACES:
SOLDERABILITY OF NICKEL SILVER**

by

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ABSTRACT

Nickel silver (copper-zinc-nickel alloy) was chosen for an ageing-solderability study, because of recent interest in this metal in electronics assembly. An Auger/ESCA study was performed on the surface of samples of nickel silver to determine the chemical nanostructure at various levels of ageing (0-2 years). During this time a redistribution of the three constituent metals occurred, with migration of copper to the surface. All three metal constituents oxidized at different rates. Additionally, the thickness of the surface carbon layer increased with time.

The effect of physical abrading (cleaning by erasing) on the samples on solderability, ageing, and chemical surface was also studied. After erasure, all samples appeared similar to each other and close to the original composition, and the copper oxide layer was completely removed. All the cleaned surfaces, when returned to the atmosphere, experienced air oxidation of copper to copper oxide in less than two days.

Angle-resolved ESCA studies were performed to determine the concentration gradient close to the surface. Nickel was not evenly distributed with depth, but was more concentrated on the surface.

INTRODUCTION

Nickel silver, an alloy of copper-zinc-nickel, can be utilized in applications involving soldering, although its solderability is lower than that of copper or even brass.[1] The advantage of nickel silver is that it need not be plated (tinned) to protect its solderability. Hence, if the solderability of nickel silver can be maintained, material costs can be reduced in the manufacture of electronic devices. Because of its potential in the electronic industry, we chose nickel silver as a model system in ageing. It had been observed that the solderability of nickel silver components deteriorated over a period of a few years' storage, and a study was initiated to study the nanostructure of the surface of the nickel silver as a function of this ageing process. Accordingly, samples were carefully selected whose history and respective ages were known. These samples were analyzed by ESCA (electron spectroscopy for chemical analysis, sometimes known as XPS, or X-ray photoelectron spectroscopy), a method that chemically analyzes the uppermost few atomic diameters of surface.[2]

The nickel silver chosen for this study was C77000 with a composition of 55-27-18 copper-zinc-nickel (the common name is "nickel silver 55-18").[3] The published limits of the composition is $\pm 1.5\%$ [3]. The samples were carefully selected, with ages of 0, 1, and 2 years. Accelerated ageing was not performed, because of the unknown correlation between real-time and accelerated ageing phenomena.[4]

ESCA ANALYSIS OF SAMPLES

ESCA determines the composition (and sometimes the oxidation state) of the upper ca. 50 Angstroms of a metal surface.[2] ESCA analysis of these three samples showed two trends: (1) an increase of oxide and carbon concentration (see Figures 1-3) and (2) a change in composition of the ternary metal composition (see Figures 4-6). (Sample ESCA data resides in the APPENDIX). Figure 7 summarizes the ternary metal composition vs the ageing process. Chlorine was always low in concentration (less than 2%) and did not increase with time.

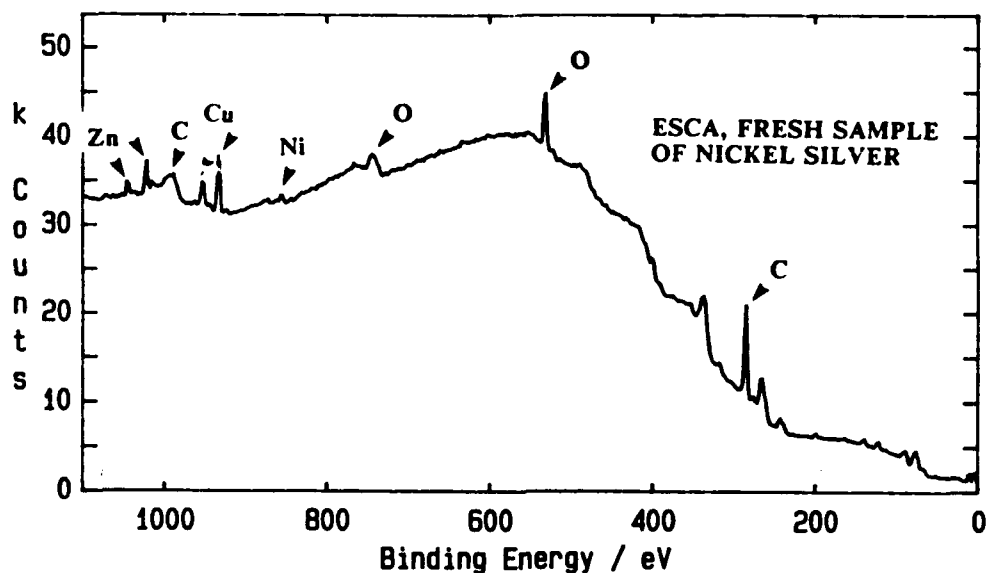


FIGURE 1. ESCA spectrum of fresh sample of C77000 nickel silver (55-27-18 Cu-Zn-Ni). Oxidation is minimum, some carbon impurities are present. (Only the more important diagnostic peaks are identified.)

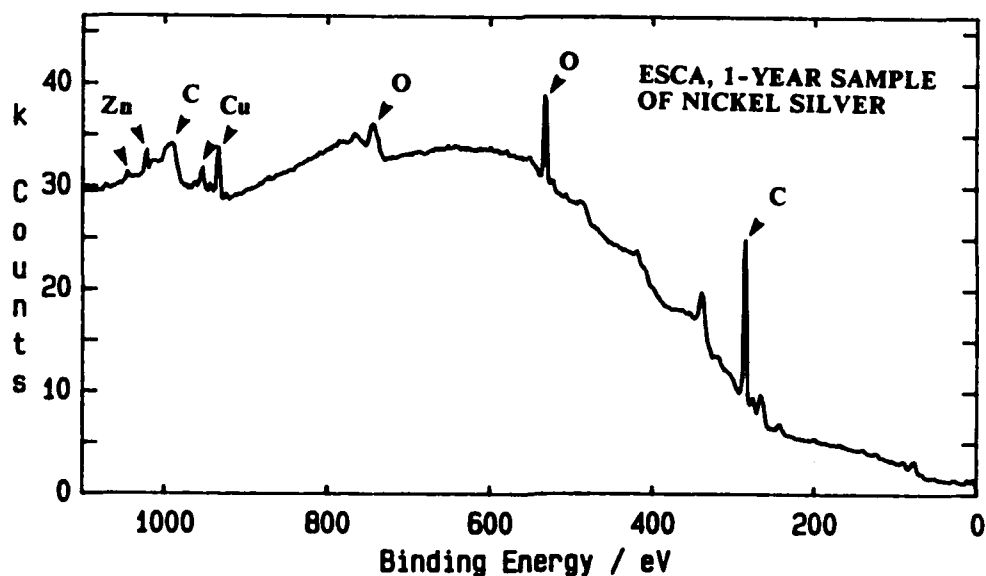


FIGURE 2. ESCA spectrum of 1-year sample of C77000 nickel silver. Oxidation and carbon are increasing.

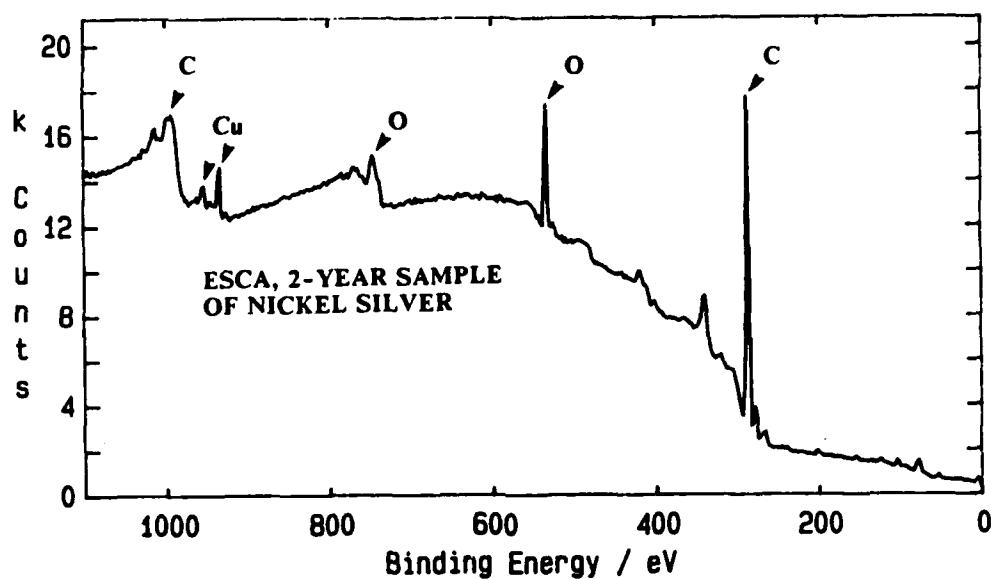


FIGURE 3. ESCA spectrum of 2-year sample of C77000 nickel silver. The trends of more oxidation and carbon continue.

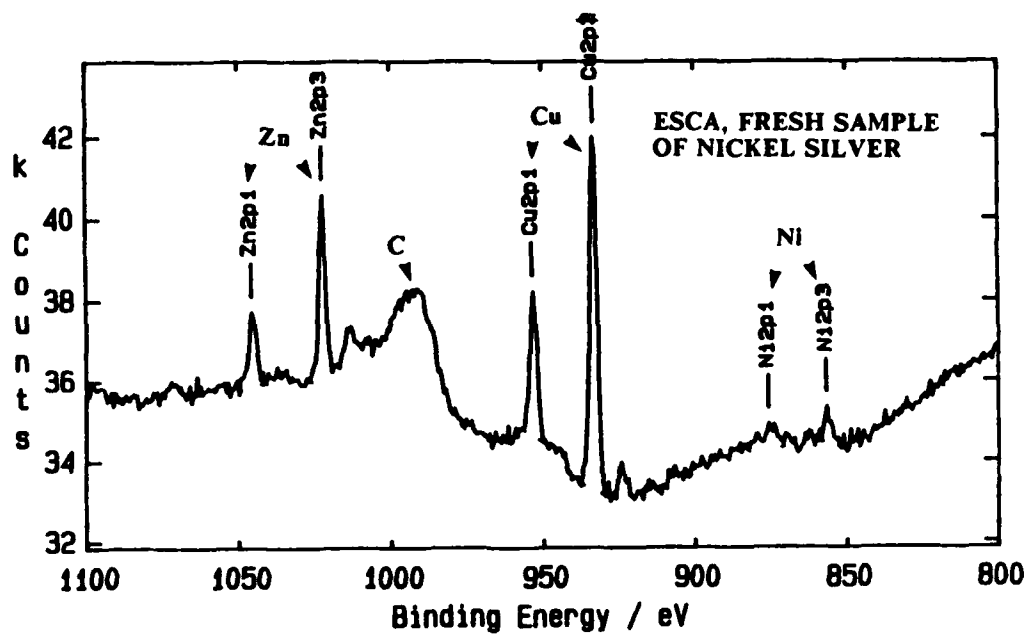


FIGURE 4. Expanded view of Figure 1, exhibiting the metal region.

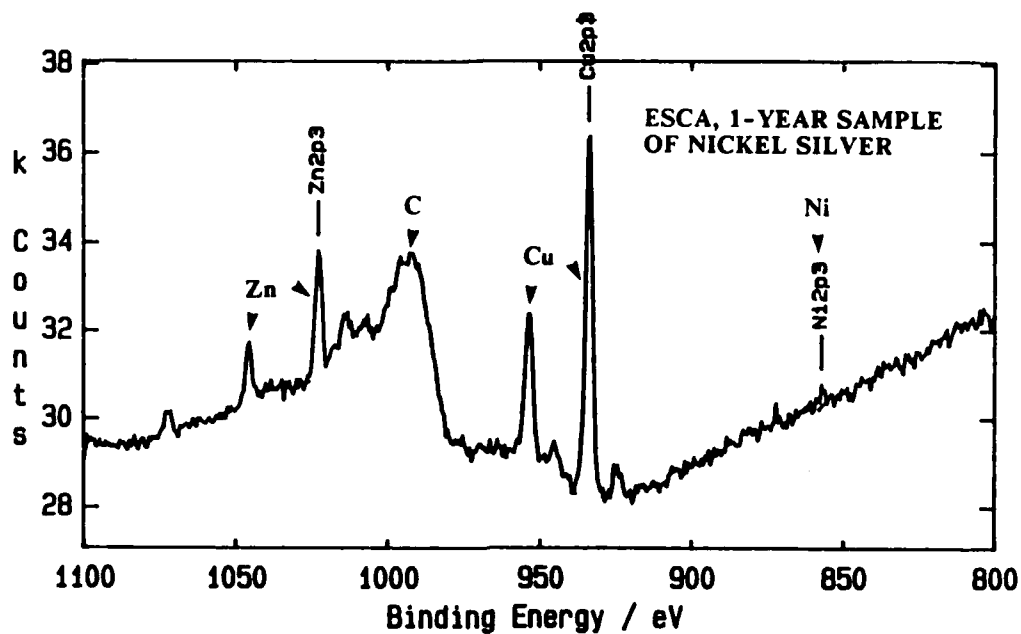


FIGURE 5. Expanded view of Figure 2.

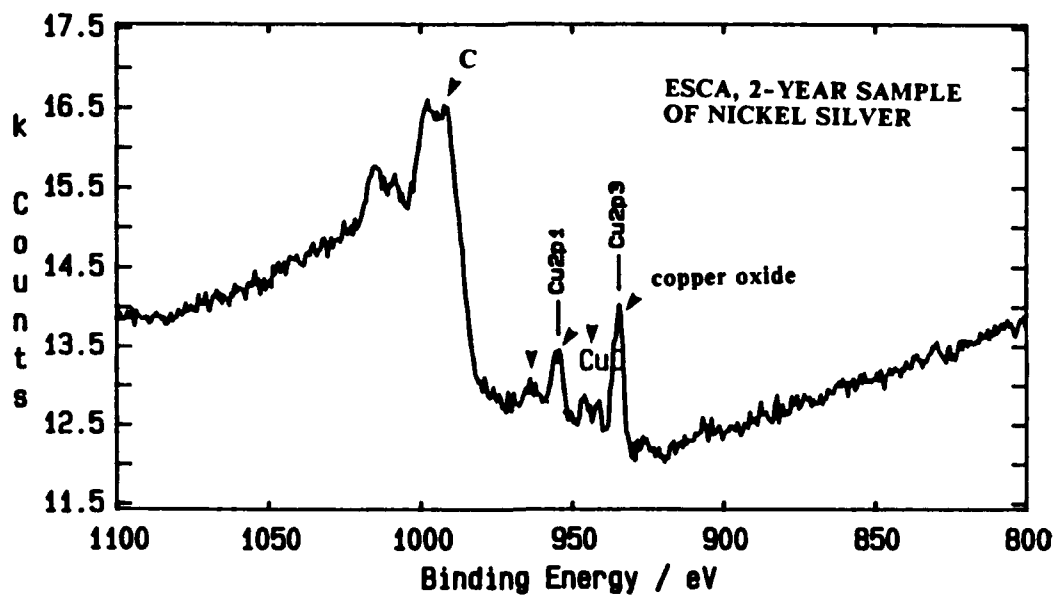


FIGURE 6. Expanded view of Figure 3. The copper is now predominant, and the copper oxide peaks are enhanced.

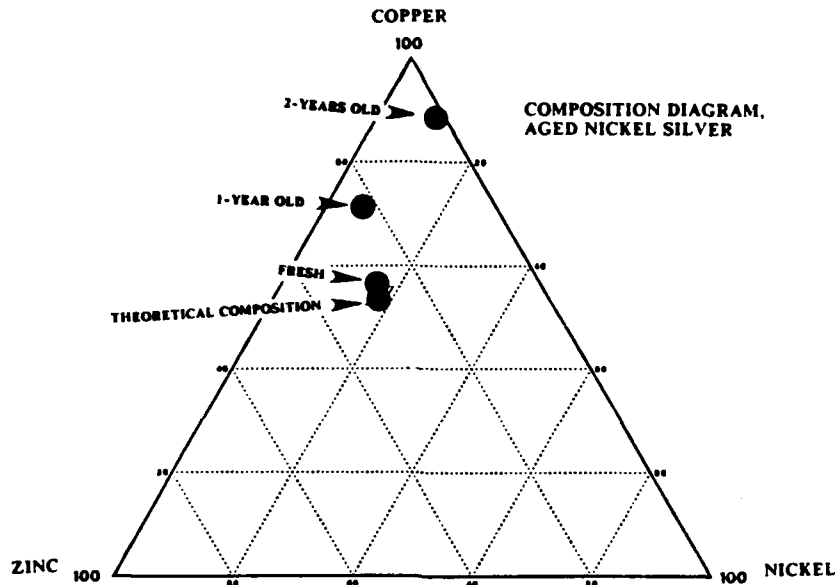


FIGURE 7. Composition diagram for the ESCA data of Figures 4-6. The fresh sample has a composition very close to that of the theoretical value.

The increase of carbon is not unexpected, because of organic contamination from the air. The redistribution of the metallic elements, however, is more unusual, with copper migrating to the surface. At the end of the 2-year period, copper is virtually the only metal at the surface. Nickel is generally in the oxidized state.[5] (It is not possible to ascertain the oxidation state of zinc, since the oxidized peak lies underneath the elemental peak.[5])

ESCA ANALYSIS OF ERASED SAMPLES

Because of the chemical evolution of the surface described above, and because erasing improved the solderability of nickel silver, it was thought that perhaps the experiment should be repeated with a mechanically cleaned surface. Samples were erased using a high quality pink eraser and analyzed by ESCA. The results showed that all samples appeared similar to one another and close to the original composition (see Figure 8), with the amount of oxide reduced (see Figure 9). The nickel was generally in the oxidized form (see Figure 10).

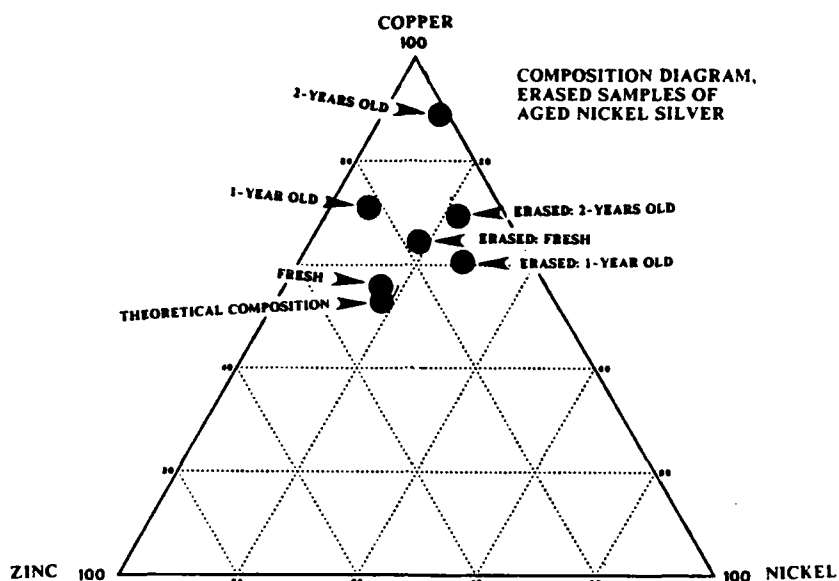


FIGURE 8. Composition diagram for the ESCA data of cleaned 0-, 1-, and 2-year samples. All samples appear similar to one another and close to the original composition.

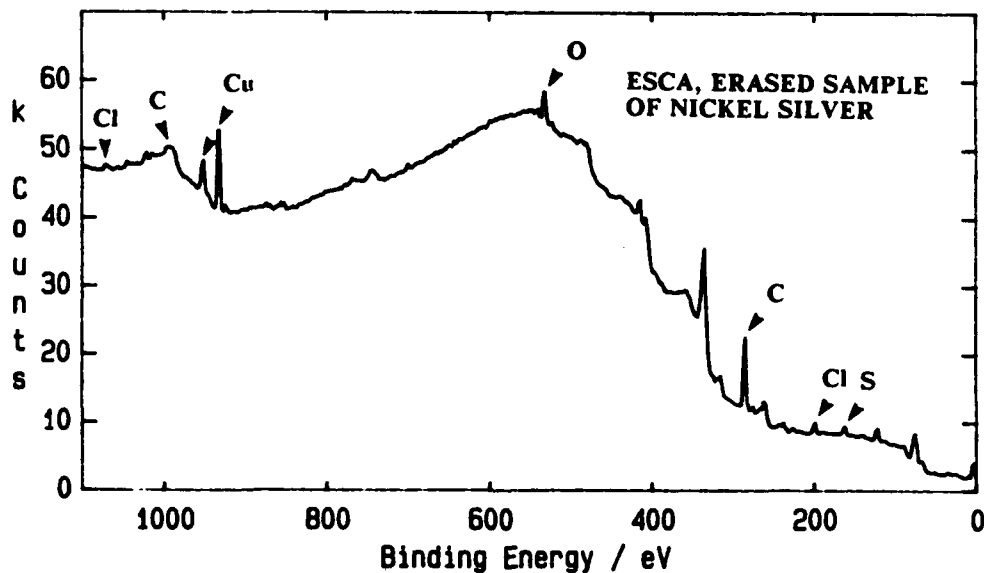


FIGURE 9. ESCA spectrum of erased nickel silver. Although oxide and carbon are reduced, chlorine and sulfur are now present.

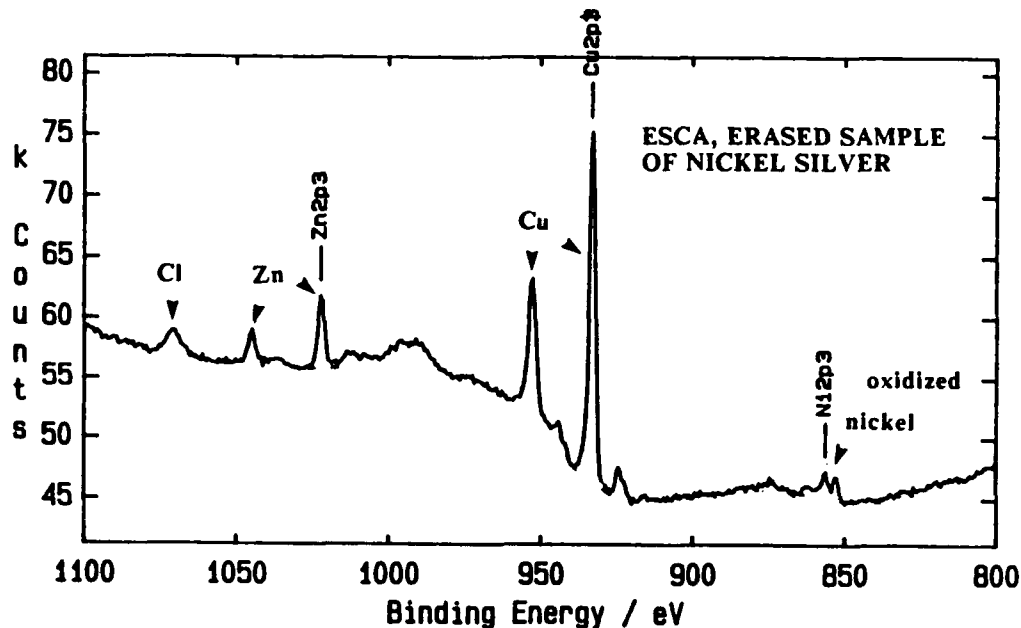


FIGURE 10. Expanded view of Figure 9. Chlorine is present and the nickel is in the oxidized form.

The erased samples experienced an increase of chlorine and sulfur (see Figures 9,10). Whereas unerased samples had much lower chlorine contents (below 2%), erased samples had chlorine contents approaching 10%. The reason for this became clear when an EDX (energy dispersive X-ray spectrum) of the eraser was taken (see Figure 11). Several samples of erasers were chosen for analysis (pink and green), all of which showed this characteristic composition of elements.

An angle-resolved spectrum of the erased sample showed a concentration gradient, with copper generally depleted on the surface (see Figures 12,13). A layer of nickel chloride may be on the surface.

A sample that had been erased was allowed to stand at atmospheric pressure for two days. The ESCA spectrum showed that during this 2-day period, the copper on the surface had virtually completely oxidized (see Figure 14). Obviously, the action of the eraser was to catalyze the oxidation of the surface.

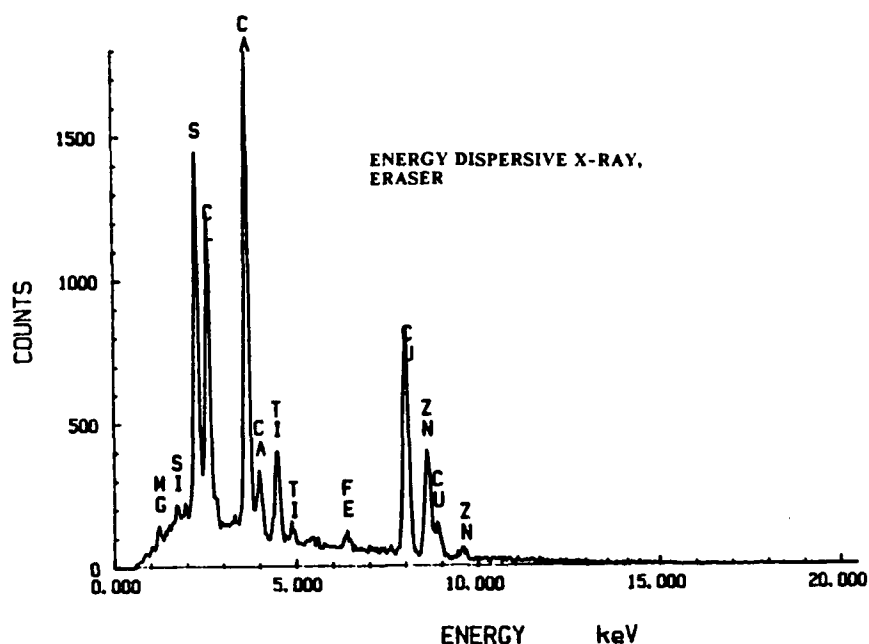


FIGURE 11. EDX (energy dispersive X-ray) spectrum of eraser. The source of the chlorine and sulfur in the erased nickel silver is apparent.

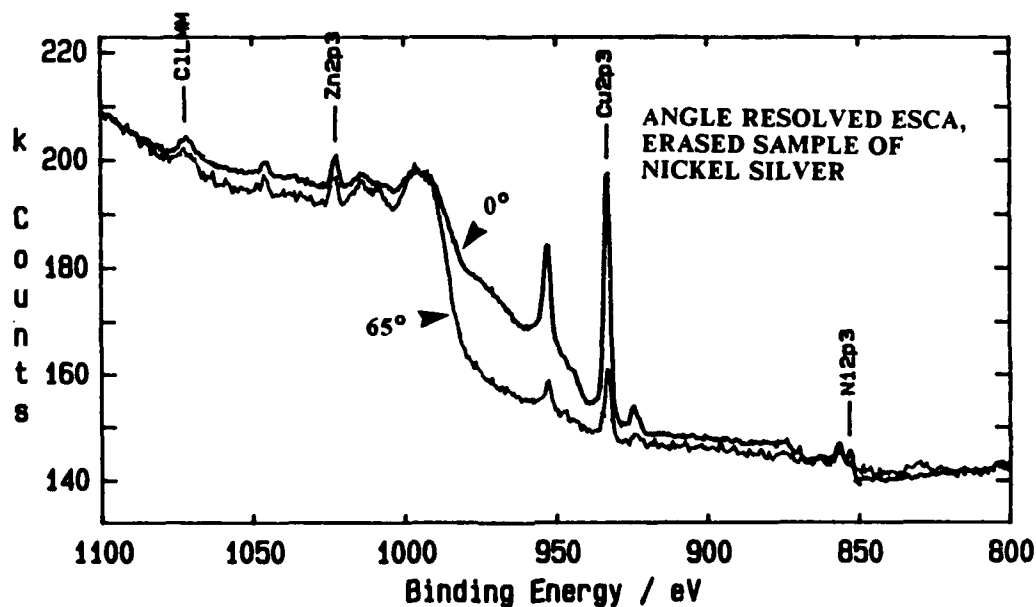


FIGURE 12. Angle resolved ESCA spectrum of erased nickel silver, showing a concentration gradient (less copper on surface).

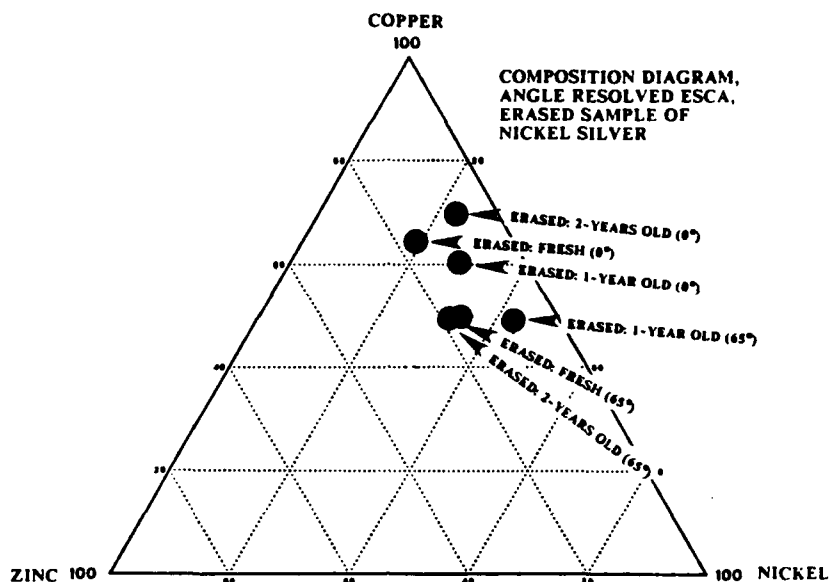


FIGURE 13. Composition diagram for angle-resolved ESCA of erased sample. Copper is depleted on the surface of the sample.

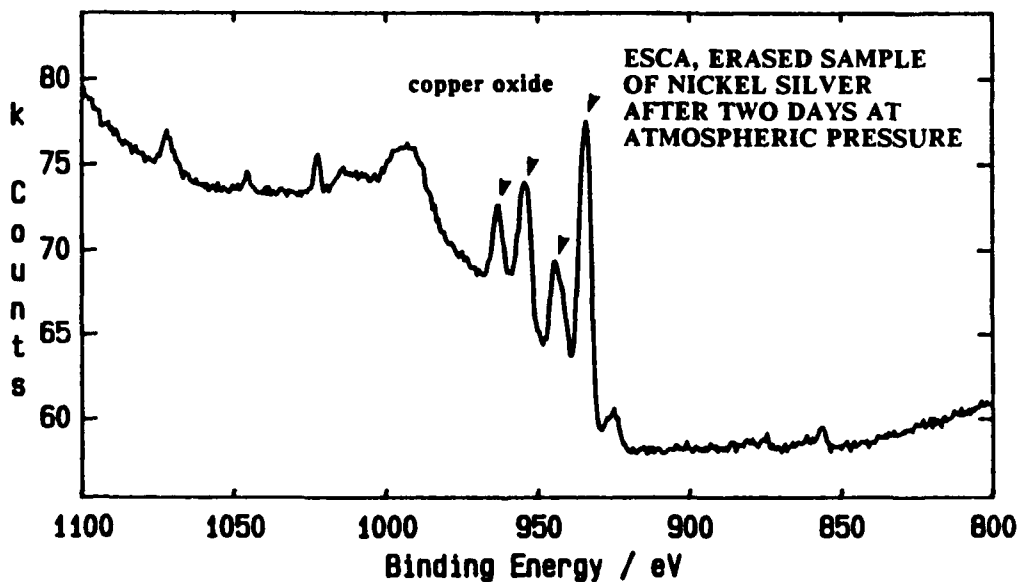


FIGURE 14. ESCA spectrum of erased sample after being exposed 2 days to atmospheric pressure. The copper has completely oxidized.

SUMMARY

Here is the summary of observations of this study:

(1) As a nickel silver sample ages, its surface oxide and carbon contents increase.

(2) As a nickel silver samples ages, the metal gradient evolves so as to include almost exclusively copper on the immediate surface (top few atom diameters).

(3) Erasing a nickel silver sample immediately "improves" the surface by removing oxygen and carbon, but reoxidation occurs extraordinarily rapidly. Furthermore, the erasing leaves chlorine and sulfur on the surface, and the nickel is oxidized. Angle resolved ESCA suggests a layer of oxidized nickel may lay on the surface.

Acknowledgments

Acknowledgment is extended to Motorola Inc., Ft. Worth, Texas 76137, for furnishing samples of nickel silver, and for the use of their EDX instrumentation.

Experimental

Samples (1-cm² specimens of half-hard C77000 alloy) were ultrasonicated in isopropyl alcohol, rinsed in isopropyl alcohol, and air dried. ESCA analyses were performed using a VG ESCALAB MkII Auger/ESCA spectrometer. EDX analyses were performed using a JEOL JSM-35-CF scanning electron microscope with a Tracor Northern 2000 energy dispersive X-ray system.

References

1. R. J. Klein Wassink, Soldering in Electronics, 2nd ed., Electrochemical Publications Limited, 8 Barns Street, Ayr, Scotland, 1989, p 265.
2. A. Joshi, "Auger Electron Spectroscopy," Metals Handbook, Ninth Edition, Vol. 10 Materials Characterization, American Society for Metals, Metals Park, Ohio 44073, 1986, p 550; J. B. Lumsdem, "X-Ray Photoelectron Spectroscopy," ibid, p 568.
ESCA
3. Metals Handbook, Ninth Edition. Vol. 2 Properties and Selection: Nonferrous Alloys and Pure Metals, American

Society for Metals, Metals Park, Ohio 44073, 1979, p 381.

4. M. L. Ackroyd, "A Survey of Accelerated Techniques for Solderable Substrates," Publ. 531, Int. Tin Res. Inst.

5. C. D. Wagner, W. M. Riggs, L. E. Davis, J. F. Moulder, and G. E. Muilenberg, Handbook of X-ray Photoelectron Spectroscopy, Perkin-Elmer Corporation, Eden Prairie, MN 55344.

APPENDIX -- SAMPLE ESCA DATA -- ELEMENTAL COMPOSITIONS

<u>SAMPLE</u>	<u>Cl</u>	<u>C</u>	<u>O</u>	<u>Ni</u>	<u>Cu</u>	<u>Zn</u>	
Fresh				16.2	56.5	27.2	(Wt. %)
	2.2	71.7	19.6	1.2	3.7	1.5	(Atomic %)
1-year old				5.6	72.2	22.3	(Wt. %)
	0.4	83.1	13.3	0.2	2.3	0.6	(Atomic %)
2-years old				11.8	86.3	1.9	(Wt. %)
	0.8	86.4	11.6	0.1	1.0	0.02	(Atomic %)
Fresh, Erased				20.4	64.2	15.4	(Wt. %)
	8.9	49.6	24.9	2.12	12.3	2.2	(Atomic %)
1-year, Erased				29.9	59.4	10.7	(Wt. %)
	9.1	53.9	27.0	2.2	6.2	1.6	(Atomic %)
2-year, Erased				26.9	63.7	9.4	(Wt. %)
	8.4	52.5	21.2	1.2	6.1	0.5	(Atomic %)

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SOLDERABILITY TESTING AND STATISTICS

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ABSTRACT

Values are given for the amount of soldering faults in consumer products. The reliability can only be increased by using statistical methods in solderability testing. Therefore everything which shall be soldered should be tested on solderability. The statistical methods used and some of the results obtained with them are presented.

INTRODUCTION

Solderability testing has become a necessity in electronic manufacturing both for high reliable products and in massproduction. Massproduction can not be carried out any longer today without statistics. So it is evident that solderability testing and statistics belong together. It is known that the mass of bad solder joints existing today is caused by bad solderability.

NUMBER OF SOLDERING FAULTS

It is often talked about the consequences of bad solder joints, but it is difficult to find in literature exact relations between bad solder joints and solderability and what type of faults bad solderability causes. We know today that bad solderability causes high contact resistance in the solder joint when the joint is subjected to ageing, Figure 1. This leads to electrical malfunctions. Manko (Reference 1) writes that bad solderability can cause cracks in solder joints.

It is difficult too to find what trouble bad solder joints cause in daily life. During a conference recently held in Germany it was mentioned that of all cars which break down on the ways in Germany 5% stop due to malfunction in electronics. In 30 % of the cases the reason was a bad solder joint. Remember that not all cars today are equipped with electronics yet.

In 80 % of the cases when TV - sets have to be repaired the cause is a faulty solder joint, usually due to thermal fatigue but even bad solderability. When colour TV's came on the market the introduction was retarded some months due to bad solderability. The explanation is given by a simple statistical reasoning. The more components and thus solder joints that are used in a unit the better the quality of the joints has to be in order to achieve the same quality level in the units, Figure 2. As surface mount devices enable us to pack tighter we face the same problem. We get more components and solder joints on the board, thus the quality level has to be risen if we do not want to reduce the yield.

When investigating the cause of bad solder joints it is often found that a bad design or manufacturing process counts for the largest proportion of faults. This proportion is in the range of 1 000 to 10 000 ppm. The terminations of the SOT's and certain chip capacitors are not designed for wave soldering and thus cause a lot of faults when soldered with this method, Figure 3. The solder simply can not come into contact with the termination. Components can be packed too tight so that a bridging between the terminals with solder can not be avoided. The soldering machine may have too low a soldering temperature or more common a too short a soldering time.

When all these different kinds of faults are eliminated the number of faulty solder joints usually have been reduced to the range of 100 to 1000 ppm. There are however examples that bad solderability can give a failure rate of some 10 000 ppm (Reference 2). However, having come down to a failure rate of 100 to 1 000 ppm the cause of the failure is found in solderability (80 %), fluxes (7 %), solder (3 %) and other reasons (10 %).

SOLDERABILITY TESTING METHODS

There are a number of solderability testing methods, the subjective qualitative and the objective quantitative ones (Figure 4). Today the most often used objective one is the wetting balance method. However to ease the explanation of statistical methods it is referred to the solder globule method as this method is less complex in using only one figure for establishing the solderability : the time which is needed for the solder globule to elapse over the round wire.

The result of the wetting balance test is the variation of the wetting force with time (Figure 5). The wetting time is important for the production, the wetting force gives an indication on the quality of the formed solder joint. Therefore both values are important. But the evaluation is more complex. Consequences from the statistics for the solder globule method to the wetting balance test must be drawn.

MODERN WETTING BALANCE TESTERS

It took many years before we knew how a wetting balance curve should be evaluated and which points in the wetting balance curve were relevant and which values were acceptable. The practical evaluation of the curve and the statistical treatment was extremely time consuming without a computer.

Thus modern wetting balance testers are designed in such a way that a computer controls the functions of the balance (Figure 6) due to the testing method chosen from a menu. The measured force values are collected by the computer and presented online on the monitor in form of a wetting balance curve. The computer evaluates the wetting balance curves according to the requirements given by the testing method or other requirements given in a menu. Thus the operation is very simple. Directly after the test a report can be printed out which includes all necessary testing data as well as the statistically treated results.

It is possible with modern wetting balance testers to carry out quite different solderability tests (Figure 7) taking care of different specifications or very different kind of components, for hole mounting, for surface mounting, wire, leads or printed circuit leads. With this type of wetting balance tester most of the material soldered to day can be tested under the necessary conditions as e.g. soldering or dipping speed or solder bath temperature. Our knowledge of solderability is so large today that we are able to test correctly even if no standards are available for the particular detail to be tested. We are even able to give a correct statement whether the detail is solderable or not.

STATISTICAL METHODS

Solder globule method

Statistical methods have been used for decades. When using them for solderability testing we have found difficulties. One difficulty is that statistical knowledge is not sufficiently spread. People like statistics in the form of the Gaussian curve (Figure 8). It is difficult to them to get the distribution presented in another form as e.g. a straight line in a logarithmical normal distribution diagram where the x - axis presents the wetting or soldering time in a logarithmical scale and the y - axis is a normal distribution for the measured values. This presentation has a number of advantages. It is very easy to see if the measured values form a straight line or if there are deviations (Figure 9). If they form a straight line the assumption is right that the measured values follow a normal distribution. But the deviations give the real important information : something is wrong with the solderability, continue the analysis. Such deviations are not necessarily easy to detect in the conservative form of the Gaussian distribution.

The straight line gives an indication that the samples are taken of a uniform lot. If this is true you never really will know before you have tested the whole lot. In the technical world it is quite common to extrapolate from the known to the unknown in order to see what happens (Figure 9). If the test result is acceptable you go on and see what happens in reality. In our case we go with the material into production and solder it. We get the help from the mathematics which tells us with which confidence we can rely on the extrapolation and which spread we can expect in the values we are interested in. In other words which risk we take in the production. If in our case the estimated soldering times are acceptable we use this material for soldering in production. Here we will find out if our assumptions were right or not. Many years of experience have shown that this method works, that it is possible with this method to reduce the number of soldering faults to values which in practice no longer are detectable by visual inspection : below 10 or even 0,1 ppm (Reference 3).

Wetting Balance Method

The wetting balance gives two measures for the solderability, the wetting time and the wetting force which are connected to each other. Both for the wetting time and wetting force acceptance values have been discussed. One is e.g. a normalized wetting force of 300 mN/m shall be achieved within 2 s (Figure 10). This makes statistics more complex. May be this is the reason why quality inspectors accept the solderability of a material when

- one test sample passes the requirement
- a specified number of samples passes the requirement
- the mean value of a specified number of samples passes the requirement.

This is wholly insufficient. As we experienced from the solder globule method it is possible to get a fully acceptable mean value for the wetting time and still get a number of unsolderable component terminations (figure 11 and Figure 9). If you want to know if all the material is solderable or let us say that not more than one faulty solder joint in 10 000 solder joints can be expected (which correlates to 100 ppm) you need to carry out more than 5 tests and to use statistics.

As only a number of samples are taken of the lot (a number of 10 or fifty is recommended) you have to regard the possible spread for your measured values. In the case of the wetting balance both for the wetting time and wetting force. This makes the evaluation by hand tricky but is easy for a computer.

ZERO DEFECT SOLDERING

Zero defect soldering is a term indicating a program which both theoretically and practically is impossible.

When coming down below 100 ppm difficulties arise in finding soldering faults. Only systematically faults can be detected which in turn may press the failure rate much below 0.1 ppm, impossible to detect visually. Automatical methods can take the strain from the quality inspector. But every automatical method can only detect certain types of faults. Even if many more faults can be detected than by visual inspection, some are left.

Statistics show that you never can predict the exact number of faults (Figure 9). In the case of solderability testing an example can be shown that within a confidence range of 90 % the failure rate can be expected to vary between 10 to 1 000 ppm. Nevertheless the material has an excellent solderability. 99.99 % of the material solders within 1 s.

SOME RESULTS

The use of statistics can reduce the number of soldering faults drastically.

In one case all the components on one board were investigated (Figure 12). By analysing the result it was found that an increase of the soldering time from 0.8 to 2 s reduced the number of faults from 48 810 to 26 220 at a total number of 550 000 solder joints. The remaining 26 220 faults were due to bad materials processing in one case and to a wrong choice of solderable material in the other case : brass. Both failure causes were eliminated which reduced the number of faulty solder joints to nearly zero. This work was carried out with the solder globule method, but could easily have been done with the wetting balance method.

More interesting and more general results could be obtained with statistical methods applied to the wetting balance.

In one investigation where 1755 wetting balance tests were carried out and 14 040 points on the wetting balance curves were analyzed and compared by the analysis of variance we found that three classes of soldering properties exist :

1. Fast soldering - good wetting
2. Fast soldering - insufficient wetting
3. Slow soldering - insufficient wetting

In other words : Fast wetting does not mean that your solder joint automatically is a qualitative acceptable joint. Even for the wetting force a value could be derived from the mass of results :

For a good quality solder joint the wetting force should be larger than 300 mN/m.

REFERENCES

- 1 Howard H. Manko
SOLDERING HANDBOOK FOR PRINTED CIRCUITS AND SURFACE
MOUNTING
Van Nostrand Reinhold Company, New York, 1986
- 2 Gert Becker
Ein Auswerteverfahren für Versuche zum Bestimmen der
Löteignung
Schweissen und Schneiden 20 (1968) Heft 7 pp 318 -
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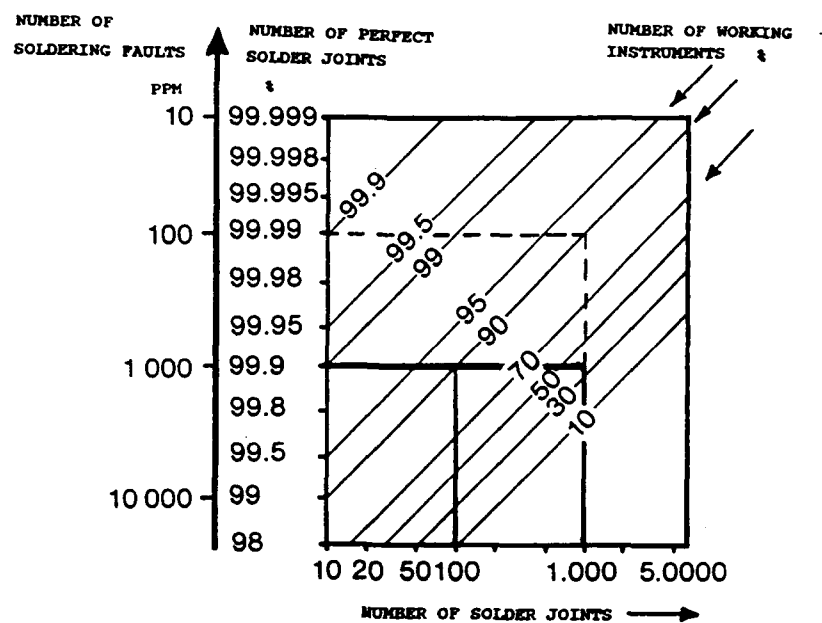


FIGURE 1 THE IMPORTANCE OF GOOD SOLDERABILITY

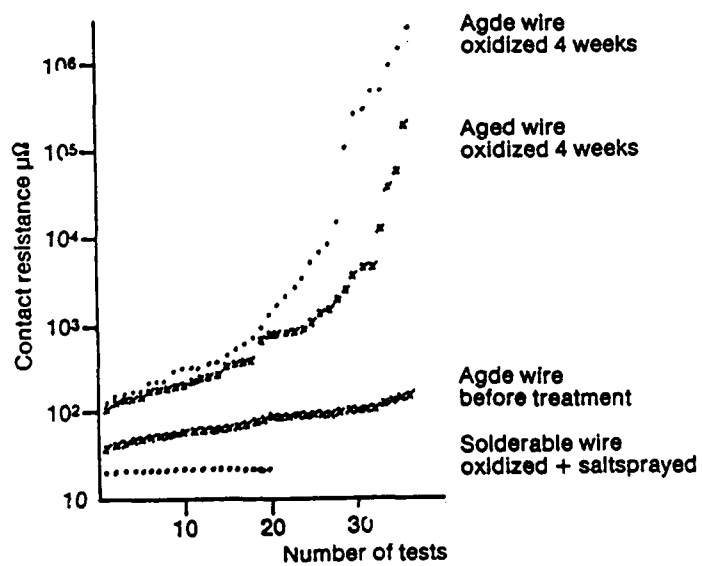


FIGURE 2 RESULTS OF ELECTRICAL CONTACT RESISTANCE MEASUREMENTS VERSUS SOLDERABILITY

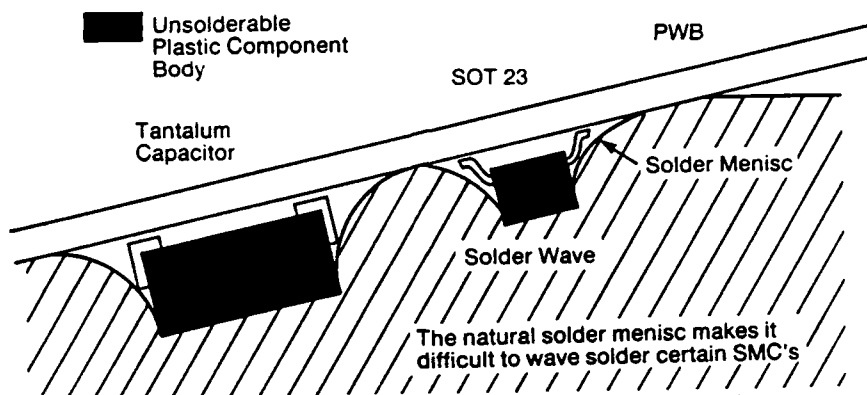


FIGURE 3 POSSIBILITY TO FEED SOLDER TO THE JOINT

**Qualitative
Subjective**

- Dipping Method
- Dewetting Test
- Solder Spread Test

**Quantitative
Objective**

- Solder Globule Method
- Wetting Balance Method
- Meniscometer Method
- Siemens Method

FIGURE 4 SOLDERABILITY TESTING METHODS

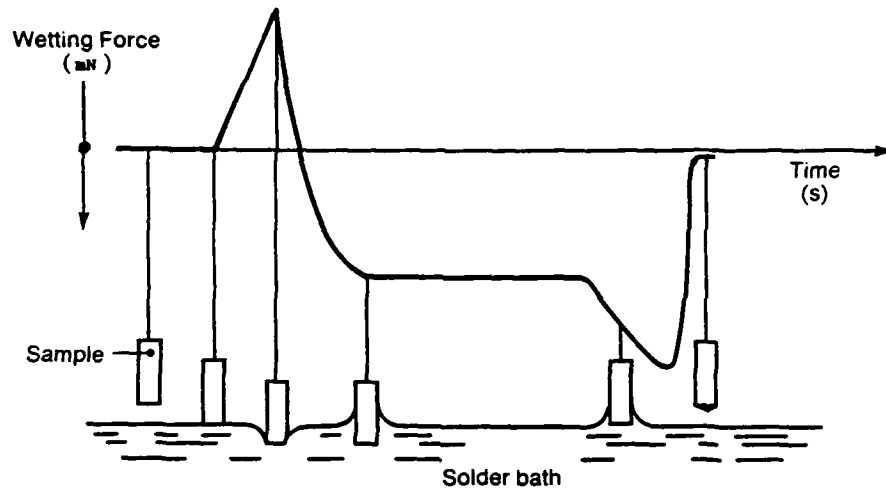


FIGURE 5 THE WETTING BALANCE CURVE

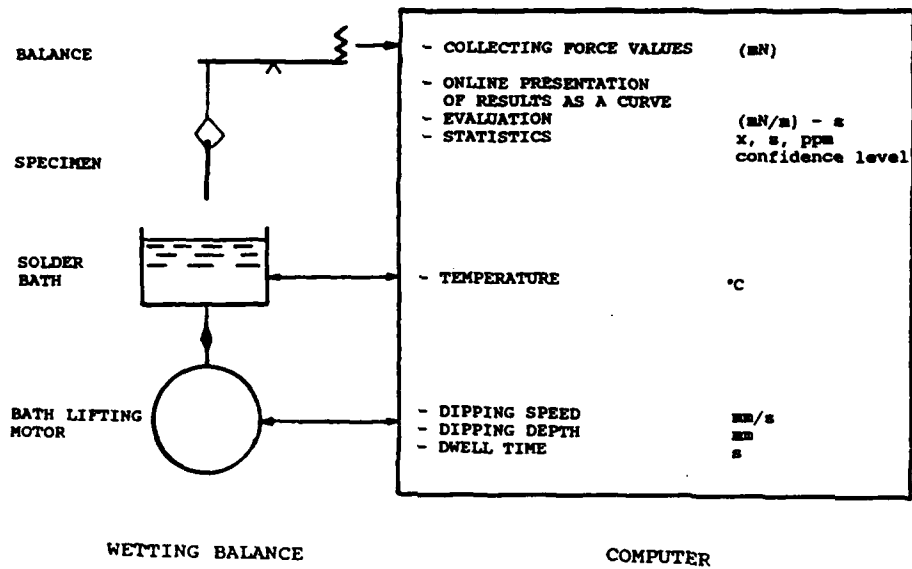


FIGURE 6 A MODERN WETTING BALANCE TESTER

IEC 68-2-54	WETTING BALANCE
IEC 189-1	PVC WIRE
IEC 251-1	ENAMELED WIRE
IPC - S 805 A	COMPONENTS
MIL - STD 883-C	COMPONENTS
NORDIC STD	SMD
SCANNING METHOD	
SIEMENS METHOD	SHEET METAL
COMPANY STD	e.g. PWB - LEADS
RESEARCH	

FIGURE 7 MENUE OF TESTING METHODS

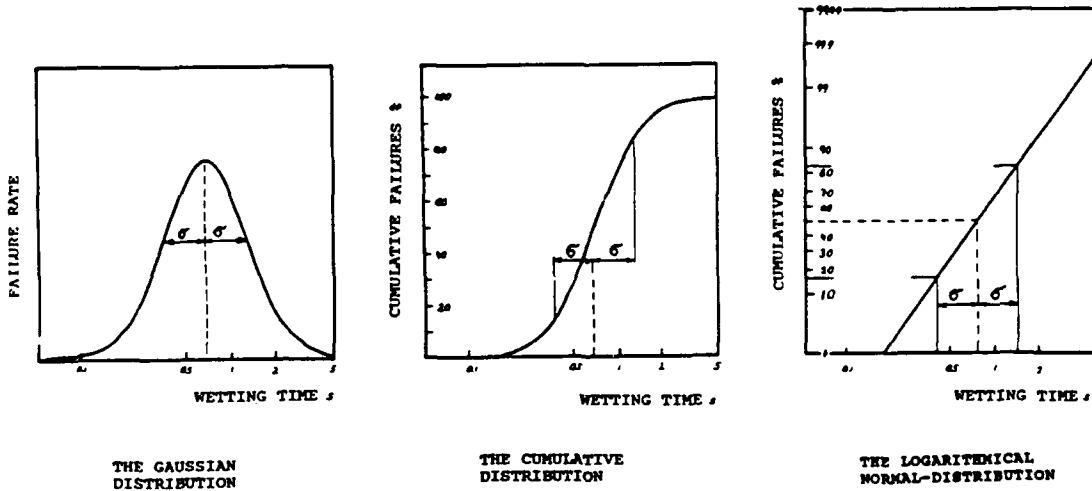


FIGURE 8 STATISTICAL DISTRIBUTIONS

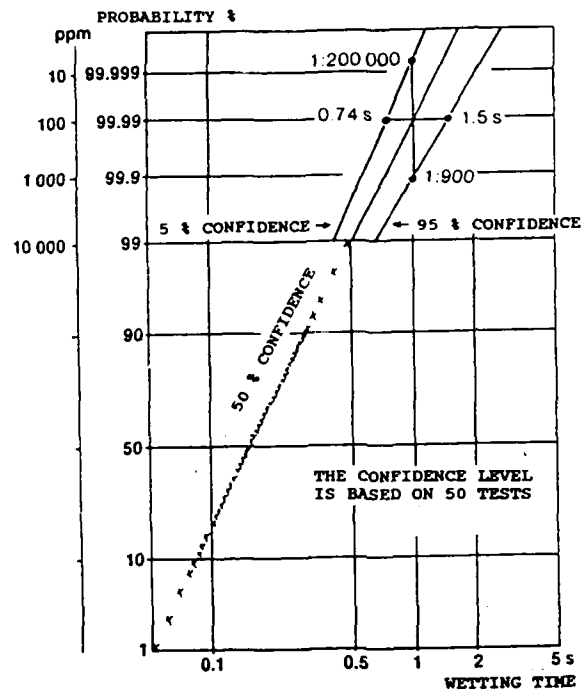


FIGURE 9 EXTRAPOLATION AND SPREAD OF TESTING RESULTS

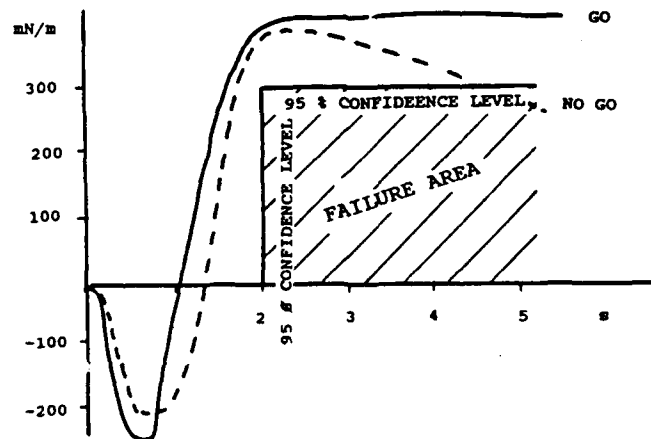


FIGURE 10 A PROPOSED ACCEPTANCE VALUE FOR THE WETTING BALANCE TEST

Component	Comp. mark	Number of components on one PC board	Number of component leads on 10,000 boards	Expected number of soldering defects when soldering 10,000 boards at a soldering time of	
				0.8 sec	2.0 sec
Capacitors	A	1	20,000	0	0
	B	1	20,000	18,800	8,400
	C	3	60,000	9,600	1,800
Resistors	D	1	20,000	20	0
	E	2	40,000	20	0
	F	1	20,000	10	0
	G	1	20,000	600	0
Diodes	H	2	40,000	0	0
	I	1	20,000	160	10
	K	1	20,000	400	10
	L	1	20,000	0	0
Relay (tabs)	M	2	130,000	0	0
Transformers (tabs)	N	1	60,000	0	0
	O	1	60,000	19,200	16,000
Expected number of soldering defects				48,810	26,220
Number of soldered connections				550,000	

FIGURE 11 MEAN VALUE VERSUS 99.99% VALUE

Component		Number of tests		50% of all connections are soldered at x sec or less		99.99% of all connections are soldered at x sec or less	
		1	2	1	2	1	2
Capacitors	A	25	24	0.19	0.19	0.68	0.75
	B	44	42	1.85	3.5	>2	>2
	C	46	43	0.41	0.68	>2	>2
Resistors	D	48	47	0.50	0.46	0.96	>2
	E	60	49	0.44	0.47	0.82	>2
	F	50	46	0.26	0.32	1.0	>2
	G	47	48	0.40	0.35	1.74	>2
Diodes	H	53	48	0.14	0.16	0.56	1.5
	I	47	46	0.19	0.05	2.0	0.8
	K	43	49	0.32	0.05	1.86	0.30
	L	50	47	0.07	0.07	0.43	0.29
Relay (tabs)	M	60		0.13		0.28	
Transformers (tabs)	N	29	28	0.15	0.21	0.43	0.96
	O	30	28	0.20	0.20	7 did not solder	>2

1 as received
2 aged

FIGURE 12 APPLICATION OF STATISTICS ON A PRACTICAL PROBLEM

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Using Wetting Balance Parameters with Discriminant Analysis
to Classify Visual Coverage and Defect Categories

by

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Abstract

Visual inspection remains the dominant method of assessing component lead solderability as per MIL-883/2003, MIL-202/208, MIL-750, IPC-805 and EIA IS-49. However, the wetting balance has received much attention as an attractive alternative to visual inspection. By using parameters or points directly from a wetting balance curve, discriminant functions are developed which classify units by visual coverage and defect categories. The results of the discriminant function is compared with a discriminant function technique involving indices from wetting balance curves, previously published by the authors (reference 1). The present technique offers the advantages of increased sensitivity and simplicity over using a function built from indices. A comparison with individual solderability tests and indices also shows this new technique to be superior in predicting solder coverage on a component lead and solder coverage defect category.

Section 1. Introduction

A recurring theme of the present semiconductor industry is to control processes--not product. It is no longer sufficient to simply inspect product attributes, instead the causes or processes which produce the product attributes must be understood and controlled. It is in this context that the wetting balance has received much attention. By understanding the information provided in the trace of a wetting balance curve, it is hoped that both solder coverage and defect category (or no defect) may be predicted. This has the potential to simultaneously save time and reduce costs. Difficulties in obtaining real-time prediction of solderability on the basis of wetting balance data is discussed in reference 2.

The most widely used method to assess electronic component termination solderability, or the ability of a lead surface to metallurgically accept molten solder during the soldering operation, is by means of visual inspection or the so called dip-and-look test. While it is generally very easy to determine very good or catastrophically bad component termination solderability using optical methods, the subjectivity in these inspector dependent methods often make it difficult to assess marginal solderability.

By contrast, the wetting balance can give an objective assessment of the component termination solderability because it generates a set of (time, force) variables data in the form of a wetting curve. The merits of the wetting balance as an objective and sensitive measure of solderability have been argued by many authors (see, for example, references 1-7). In fact, DeVore, has given a detailed description of the three recognized mechanisms of solderability, wetting, non-wetting and dewetting, in terms of objective wetting balance measurements (reference 2).

Previous attempts to use information from the wetting balance curve have focused on either using criteria developed for specific points on the curve as in MIL-STD-883/2022, or on obtaining indices from points on the wetting balance curve such as DeVore's solderability index or several other indices developed by the authors (reference 1).

The difficulty in the attempts to use indices to assess solderability seems to be in their relation to the visual tests. Clearly, the use of the wetting balance must be able to ascertain when a unit will be visually "good" and when a problem such as surface roughness (asperity), pin holes, dewetting or non-wetting occurs. To compound the difficulty in attempting to use an objective method to agree with a subjective visual inspection is the fact that subtle differences in wetting balance parameters may not have any correspondence to visual results. Nevertheless, the correlation of wetting balance data and visual data has yet to be definitively or statistically determined although numerous attempts have been made (see references 1-7).

As semiconductor manufacturing moves from a data poor environment to a data rich one, more and more information may be extracted from the wetting balance curve. The technology now exists to essentially digitize the wetting balance curve so that one need not be constrained to only consider two or three points taken manually from the curve.

In this regard, let

$$(t, F_{(t)})$$

be the time and gram-force ordered pair for the point taken from the wetting balance curve at time t . Figure 1 displays a typical wetting balance curve along with notation for curve measurements used in this paper. Note in Figure 1 that t denotes a time recorded at $\frac{1}{2}$ seconds while t_e denotes a time taken at a particular event, (i.e. t_{max} is the time at which the wetting force reaches a maximum value before extraction from the solder pot). A similar notation holds for force measurements with $F_{(t)}$ denoting forces recorded at time t and F_e denoting forces recorded at the event e .

In this paper all gram-force measurements are given in force per unit distance by adjusting for buoyancy and perimeter with the formula

$$F_{(corrected)} = (\text{observed gram-force measurement} + F_b)/p$$

in which p is the perimeter of the unit's cross section coplanar with the solder surface, and

$$F_b = \rho g V$$

is the buoyancy force with ρ = density of molten solder (8.155 g/cm³ for Sn63 solder), g = acceleration due to gravity (980 cm/sec²) and V = volume of solder displaced by the component termination during immersion. When different specimens with various heat demands and geometries (such as PWB's and LCC's) undergo the transformation above, the general shape of wetting balance curves appear similar.

Part of the appeal of current solderability indices and solderability tests is that they may be computed simply from only a few points taken from the wetting balance curve. Obviously, this neglects the information contained in the remaining points.

Although the technology to select a large number of points ($t, f_{(t)}$) directly from a wetting balance curve is not yet in widespread use, this paper seeks to examine the feasibility of predicting solderability coverage and defect category on the basis of a relatively large number of points. This will point the way to a productive use of the ability to extract large numbers of points from a wetting balance curve to accurately predict solderability performance.

The method employed here is to apply the statistical technique of discriminant analysis to construct functions (linear combinations of discriminating variables) based on parametric data from the wetting balance which will reliably classify units according to solder coverage and defect category. Discriminant analysis may be used for two purposes: interpretation and classification.

In the interpretive use, an understanding of which variables affect coverage or defect type may be obtained through the construction of linear combinations of the discriminating variables called discriminant functions. These functions may then be used in the classification activity to classify units into either coverage categories or defect categories on the basis of scores obtained from the discriminant functions.

The essential idea is that units with scores most closely resembling the scores of actual units in a particular category are classified accordingly. The use of discriminant functions for linear combinations of solderability indices has already been described by the present authors in reference 1. Here we extend the application of the discriminant function technique to many individual points taken from the wetting balance curve. This technique is then compared with current solderability indices and tests on visual inspection data taken on 18 lead ceramic dual in-line package (CERDIP) test samples.

Section 2. Current Solderability Indices and Tests

In order to assess the possible benefits of a solderability classification using discriminant analysis over other methods, we will briefly outline some of the current solderability indices and solderability tests. A few brief comments on several of the indices and tests will be made. We will also include descriptions of four indices proposed by the present authors (reference 1) as competitors to the more standard approaches. The notation used to define these indices is consistent with that in Figure 1.

DeVore's Solderability Index

John DeVore (reference 2) proposed a solderability index, here called SI, which may be defined as

$$SI = \frac{F_{(2)}}{t_0(F_{\text{spike}} - F_{\text{end}})}$$

It is worth noting that SI is invariant with respect to the perimeter soldered and is unique in that it incorporates values relating to wetting speed (t_0), wetting force ($F_{(2)}$) and dewetting ($F_{\text{spike}} - F_{\text{end}}$).

In addition, DeVore has recommended that "good" solderability is achieved when SI exceeds 5. Thus an informal solderability test could consider a unit passing whenever it achieves a value of SI exceeding 5.

DeVore's Coefficient of Wetting

DeVore (reference 3) has also discussed a measure called the coefficient of wetting which is given by

$$CW = \frac{F_{eq}}{t_{eq}}$$

The sample must reach equilibrium in order for this index to be calculated. In practice, this is may be overly restrictive for many units which do not attain equilibrium with the usual 5 second wetting balance test. Moreover, experience with computing this index demonstrates that there may be some difficulty deciding exactly when the equilibrium point has been reached, in fact, on only 12 of 102 (11.7%) curves could an equilibrium be identified.

Stability of Wetting Index

Becker (reference 4) describes a stability of wetting measure which we call SW and is defined as

$$SW = F_{max} - F_{end}.$$

Note that this index is primarily concerned with dewetting.

Industry Standard Solderability Test

Becker (reference 4) also gives an informal industry standard solderability test which defines a pass if

$$F_{(2)} \geq 300 \text{ mN/mm.}$$

MIL-STD-883/TM2022 Solderability Test

This method considers a unit to pass if

$$t_0 \leq 0.59 \text{ sec and} \\ F_{(1)} \geq 2/3 F_{(5)}.$$

Woolridge's Modified MIL-STD-883/TM2022

Woolridge (reference 5) describes a modification to the MIL-STD-883/TM2022 test whereby a unit is considered to pass the test if the following three conditions are satisfied,

$$t_0 \leq 1 \text{ sec} \\ F_{(2.5)} \geq 200 \text{ } \mu\text{N/mm and} \\ F_{(5)} \geq 200 \text{ } \mu\text{N/mm}.$$

Percent of Theoretical Maximum Force

The theoretical maximum wetting force, F_{th} , can be defined as the surface energy or surface tension of the solder at the temperature of interest. Manko (reference 8) has published 490 dyne/cm @ 280 C for 63/37 solder. Some of the industry experts have informally agreed at the recent EIA and IPC meetings that the value should be closer to 420 dyne/cm = 420 $\mu\text{N/mm}$. We have chosen to use 490 $\mu\text{N/mm}$ in this paper.

We may now define the percent of the theoretical maximum wetting force as,

$$PCTF_{th} = \frac{100\%F_{max}}{F_{th}}$$

This index, like DeVore's SI, is invariant with respect to perimeter.

The following four indices were proposed by Mullenix, Gerke and Kwoka (reference 1) and were used as discriminating variables to develop discriminant functions for predicting solder coverage and defect category.

Angle to Maximum

The angle formed between the time axis and the line connecting the point of maximum wetting force with the origin (start of test) may be written,

$$\text{MAXANG} = \tan^{-1} \left(\frac{F_{\max}}{t_{\max}} \right).$$

Note that MAXANG is similar to DeVore's coefficient of wetting, CW, except that the time and force at maximum (before extraction from solder) is used instead of at equilibrium. This makes the index capable of being computed in cases where equilibrium is not achieved. The correlation of MAXANG to CW is 0.93 (see Table 1).

Adjusted $F_{\max}$

Point B on figure 2 displays the idealized "best case" wetting balance curve for a given maximum attained wetting force. Such a curve would rise nearly straight up to a given maximum point B then remain at that level for the entire test. In practice a curve cannot exactly follow this idealized curve, but it can approach it by rising steeply, attaining its maximum at point M and leveling off at that maximum value. The adjusted $F_{\max}$ seeks to take the shape of the curve into account and weight $F_{\max}$ by how close the shape of the curve resembles the idealized "best case" curve.

To accomplish this, the closest point on the graph to B is found by rotating a ray laying on the force axis with tail at the origin, O, toward the time axis. The first point on the curve which this ray meets will be the tangent, T, formed by the ray and the wetting balance curve. The line segment joining B and T will intersect the line segment OM at the point S (see Figure 2).

Observe that the steeper the curve rises, the larger the segment ST becomes. The ratio ST/SB gives the proportion of the distance to the "best case" point B accounted for by the location of the point S. The adjusted $F_{\max}$ may now be defined as

$$F_{\max} = \frac{ST}{SB} F_{\max}.$$

where

$$ST = \left[(t_{\max} - x_s)^2 + (F_{\max} - y_s)^2 \right]^{1/2}.$$

$$SB = \left[x_s^2 + (F_{\max} - y_s)^2 \right]^{1/2}.$$

and (x_s, y_s) are the coordinates of the point S with

$$x_s = \frac{t_{\max}}{1 + \frac{t_{\max}}{t_{\min}} - \frac{F_{\max}}{F_{\min}}}$$

$$y_s = \frac{F_{\max}}{t_{\max}} x_s$$

Curves with identical maximum points M and common ratio ST/SB have tangents laying along a line parallel to OM. This defines a class of curves each making trade-offs of steepness of rise with sharpness of the turn to reach M.

Adjusted $F_{\min}$

Similar to the construction of $ADJF_{\max}$, we define

$$ADJF_{\min} = \frac{S'T}{S'B} F_{\min}.$$

Figure 2 shows the line segments in the above formula and in particular displays the point B' on the force axis which is equal to F_{1n} . With the substitution of F_{1n} for F_{max} in the formula for x_s given above for $ADJF_{max}$, the same formulas may be used to compute $ADJF_{1n}$.

Force Range

The force range is simply

$$F_{range} = F_{spike} - F_{min}.$$

As with the stability of wetting index, SW, the force range is mainly intended to assess dewetting.

Section 3. Previous Results

In a previous work by the authors (reference 1), 102 CERDIP's (18 lead) were subjected to both the wetting balance and a visual inspection. The solderability tests from the previous section were then compared according to their agreement with visual inspection results. In addition, discriminant functions composed of linear combinations of both existing indices and those proposed by the authors were developed and also compared with the same visual inspection data. The solderability indices are compared for linear correlations in Table 1. Only the pairs CW with MAXANG and CW with F_{range} seem to share a strong linear correlation.

Table 2 summarizes the solderability test results pertaining to solder coverage among the five tests: SI (Devore's $SI > 5$), IS (industry standard test mentioned by Becker), MIL883 (MIL-STD-883/TM2022 test), MOD883 (Woolridge's modified MIL-STD-883/TM2022 test) and DISCFN (discriminant function classification method). A correct decision concerning coverage classification is stipulated to mean that the unit passed the solderability test and was visually judged to have 95-100% coverage.

It is clear from Table 2 that in this study the discriminant function is superior in making correct classifications concerning visual coverage with 85% correct classification of the cases. The nearest competitor was MOD883, Woolridge's modified MIL-STD-883/TM2022, which achieved 75% correct classifications on coverage followed by SI (49%), IS (46%) and MIL883 (31%).

All of the tests indicate the desirable property that if a unit passes the test, then there is a high probability that the unit will have at least 95% coverage. On the other hand, only the MOD883 and DISCFN tests were able to correctly identify a large proportion of the units with at least 95% coverage--74% and 84% respectively. The MIL883 test seems overly restrictive in this regard, only passing about 8% of the units visually rating 95-100% coverage.

An added benefit of the DISCFN approach is that it directly classifies units into coverage categories--it is not a pass/fail test. The classification results were 96% correctly classified in the 95-100% group (67 units), 38% correctly classified in the 75-94% group (13 units), 91% correctly classified in the 50-74% group (11 units) and 100% correctly classified in the 25-49% group (2 units).

None of the solderability tests performed well with respect to passing units being correctly grouped in the "no defect" category. The SI test did the best with 33% of the passing units actually having no visual defects, followed by MOD883 (28%), IS (19%) and MIL883 (0%). However, the MOD883 test performed the best with respect to passing 77% of the units with no visual defects. The results for the other tests were 36% for SI, 18% for IS and 0% for MIL883.

As with coverage classification, the DISCFN operates on a slightly different principle. It does not score a pass or fail, rather it proceeds to classify the unit directly into one of five defect categories: no defect, asperous (or rough surface), dewet, nonwet and pinholes. The percentages of correct classification into the various groups was 45% for the no defect group (20 units), 74% for the asperous group (42 units), 50% for the dewet group (4 units) and 75% for the nonwet group (8 units). The discriminant functions were not able to be computed for the units with pinholes due to missing information for one or more of the indices making up the functions.

Section 4. Extension of the Discriminant Analysis Method

In this section we describe an extension of the discriminant analysis method to incorporate many points taken directly from the wetting balance curve as discriminating variables, rather than indices compiled from a relatively few number of points as in reference 1. For an introduction to discriminant analysis, consult, for instance, Klecka (reference 8).

Since the technology is now available to sample almost any number of points from the wetting balance curve by computer, this extension is important for indicating the feasibility of using these large numbers of points in a discriminant function to predict solderability with respect to coverage and defect category. The results are compared against visual inspection and seem to be a slight improvement in the method reported by the authors in reference 1.

The points initially chosen as candidates for the discriminating variable were

F_{min} , F_{max} , F_{1an} , F_{end} , F_{spike} , F_1 , F_2 , $F_{2.5}$, F_4 , $F_{4.5}$ and F_5 .

However, not unexpectedly, $F_{4.5}$ and F_5 are highly correlated at 0.996 and F_2 and $F_{2.5}$ are highly correlated at 0.983. Because of certain mathematical requirements, terms which are linear combinations of other terms should not appear in the same group of discriminating variables. Hence, $F_{2.5}$ and $F_{4.5}$ were excluded from the list.

Four different attempts were made to predict solderability. First, classification into the individual defect categories of "no defect," "asperous," "dewetting," "pin holes," or "non-wetting" was attempted. Second, a discriminant function was developed to classify units according to "no defect" or "some defect" categories. Third, a function was developed to classify units according to 95-100% coverage. Fourth, classification into the individual coverage categories or 0-24%, 25-49%, 50-74%, 75-94%, and 95-100%.

The basic idea of discriminant analysis for each of the above four cases is to compute functions which will help characterize the differences between the categories being considered and provide a means to classify a unit into the class it most closely resembles on the basis of the discriminant functions scores. For each of these four cases we use SAS, Statistical Analysis System, to report the standardized canonical coefficients, the total canonical structure coefficients, and the raw canonical coefficients. To calibrate the functions, half of the data was used, and it was then applied to the remaining half for classification purposes.

Briefly, the standardized coefficients enable the assessment of the discriminant variable's contribution to calculating the discriminant score. The standardized coefficients take into account the joint contributions of all of the discriminant variables. The total structure coefficients are simple bivariate correlations and hence are not affected by the relationships with the other variables. The total structure coefficients give information about the linear relationship (or correlation) between a discriminating variable and the discriminating function. When the correlation is near 1.0 or -1.0 the variable and function are providing similar information. The raw coefficients may be used for computing the discriminant function score but are not used for interpretation of contributions of the variables.

Results of classification into specific defect categories is given in Table 3 along with the standardized, total structure, and raw canonical coefficients. The technique seems to excel with regard to classifying asperous defects as it correctly classified 85% of this group. The overall correct classification percentage for all five defect groups is 62%. This is a 10% improvement over the method using indices reported by the authors in reference 1. A two function plot of the classification procedure is given in Figure 3.

By only considering two categories, "no defect" and "some defect," an overall 82% correct classification was found. Within the "no defect" units only 26% were correctly classified, but among the "some defect" units, 97% were correctly classified. These results are presented in Table 4 and represent a major improvement over current defect type classification methods.

The ability of the method to predict solder coverage seems to be better than for defect category prediction. Table 5 summarizes the results of predicting solder coverage into five categories. The method does extremely well at either low coverage levels or high levels--over 90% correct classifications in these cases. However, the middle category, 75-94% is more difficult to classify. Nevertheless, the overall percent of correct classifications is 87%. This is equivalent to the rate found for the method using indices from reference 1.

The current method performs even better if we are just interested in classifying units into two groups, "95% coverage or better" and "less than 95% coverage." Table 6 lists the results. For this case a total of 90% correct classifications were achieved.

Section 5. Conclusion and Discussion

We have shown the feasibility of predicting solder coverage using a discriminant analysis based on many points taken directly from a wetting balance curve. The correct classification percentage for solder coverage is around 90%. The results for defect type are encouraging, and about a 10% improvement over the previous method reported in reference 1.

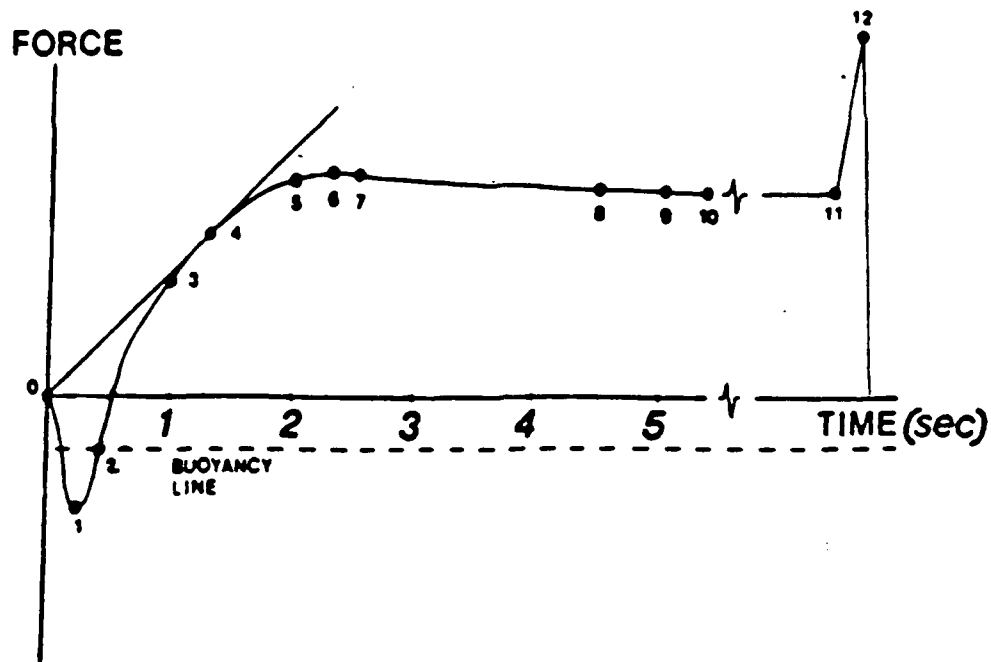
With the coming of the ability to essentially digitize the wetting balance curve, discriminant analysis provides an attractive method of predicting solder coverage and perhaps gains in defect type may also be obtained. In addition, it should be noted that, in contrast to pass/fail tests, only discriminant analysis to this date offers the means to classify units into several categories of either coverage or defect type.

The final goal of any useful solderability test must be to predict the ability of an electronic component termination to "wet" with solder and form an "acceptable" solder joint/fillet when exposed to board level assembly soldering processes. It has been shown that the use of discriminant analysis based techniques for assessing electronic component termination solderability via wetting balance measurements can correlate with visual inspection for 95% coverage for about 90% of units tested.

Although it is necessary that the wetting balance methods agree with visual inspection, it would be even more compelling when it can be shown that the wetting balance measurements are in good agreement with actual board level assembly soldering performance. This will be the topic of future work.

References

1. Mullenix, Paul D., Gerke, R. D. and Kwoka, Mark A., "Assessing Solderability Performance with Wetting Balance Indices and Discriminant Analysis," 13th Annual Soldering Technology Seminar Proceedings, China Lake Naval Weapons Center (March 1989): 301-313, NWC TP 6986 EMPF TR 007.
2. DeVore, J. A., "Solderability and Surface Mounting," 12th Annual Soldering Technology Seminar Proceedings, China Lake Naval Weapons Center, (Feb. 1988): 301-313, NWC TP 6896, EMPF TP003.
3. DeVore, J. A., "The Mechanisms of Solderability and Solderability Related Failures," Printed Circuit World Convention III, (May 1985), IPC Technical Review, (Feb. 1985): 17-20.
4. Becker, G., "Solderability Testing of Surface-Mount Devices," Electronic Packaging and Production, (Oct. 1987): 32-35.
5. Woolridge, J. R., "Lessons Learned During a Year of Production Solderability Testing with a Wetting Balance," 12th Annual Soldering Technology Seminar Proceeding, China Lake Naval Weapons Center, (Feb. 1988): 485-496, NWC TP 6896, EMPF TP000.
6. Allen, B. M., "Testing SMDS for Solderability," Surface Mount Technology, (Oct. 1988): 17-18.
7. Wild, R. N., "Some Component Lead and Solderability Issues," Brazing & Soldering No. 9, (1985): 5-10.
8. Manko, Howard H., Solders and Soldering, 2nd Ed., McGraw-Hill Book Company: New York, 1979.
9. Klecka, W. R., Quantitative Applications in the Social Sciences, Sage University Paper Series, (1980): Series No. 07-019.



0 - ORIGIN	= (0,0)	7 - $t=2.5$ sec	= (2.5, $F_{2.5}$)
1 - MIN	= (t_{min} , F_{min})	8 - $t=4.5$ sec	= (4.5, $F_{4.5}$)
2 - t_b	= (t_b , 0)	9 - $t=5$ sec	= (5, F_5)
3 - $t=1$ sec	= (1, F_1)	10 - EQUILIBRIUM	= (t_{eq} , F_{eq})
4 - TANGENT	= (t_{tan} , F_{tan})	11 - END	= (t_{end} , F_{end})
5 - $t=2$ sec	= (2, F_2)	12 - SPIKE	= (t_{spike} , F_{spike})
6 - MAX	= (t_{max} , F_{max})		

FIGURE 1. WETTING BALANCE PARAMETERS

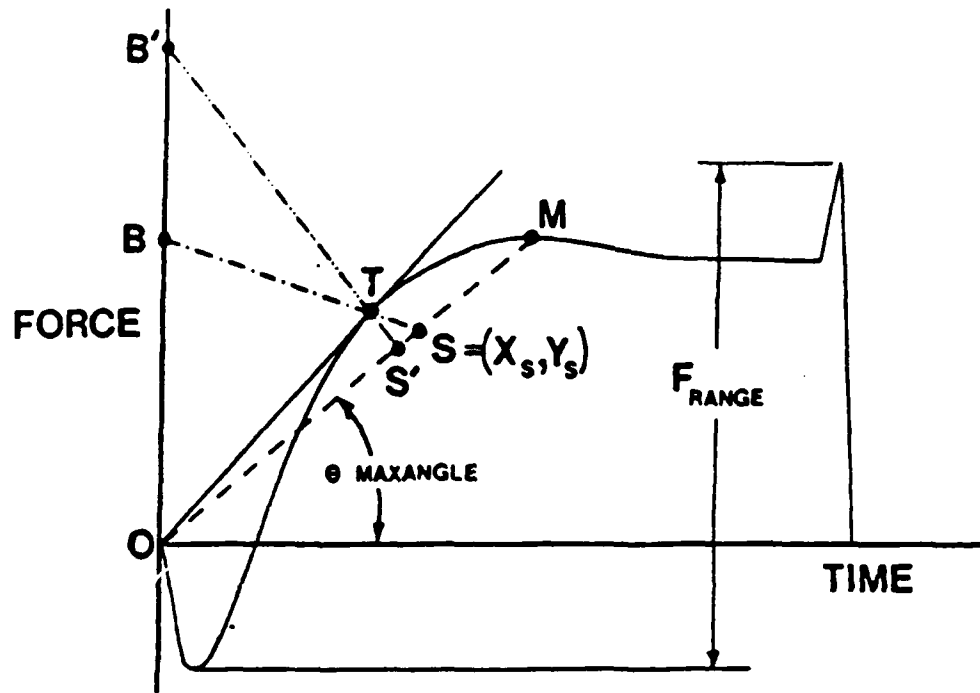


FIGURE 2. POINTS USED TO CALCULATE NEW SOLDERABILITY INDICES

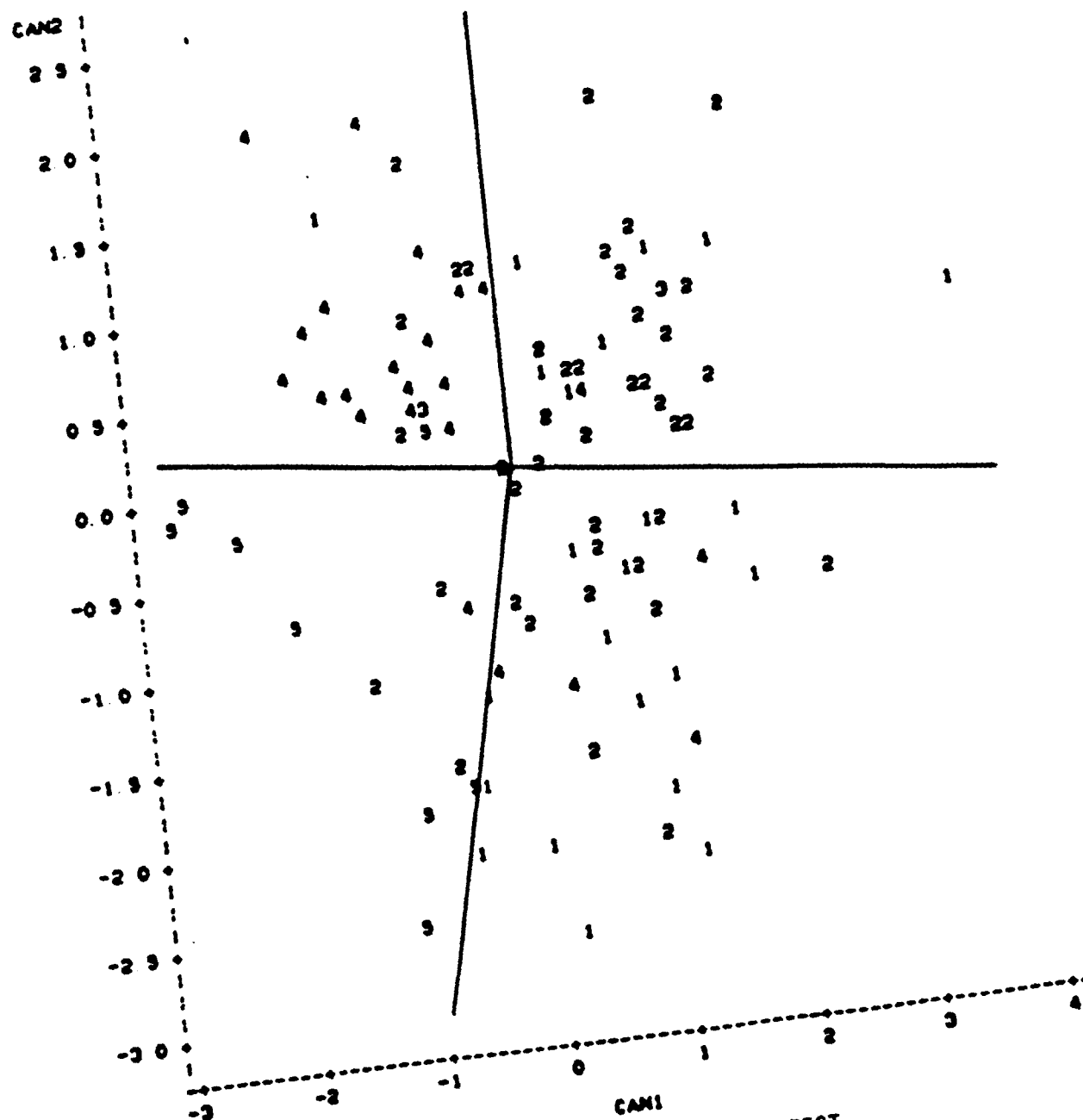


FIGURE 3. TWO FUNCTION PLOT FOR DEFECT
CATEGORY CLASSIFICATION

1 = NO DEFECT
2 = ASPEROUS

3 = DEWET
4 = PINHOLES

5 = NONWET
CAN1=CANONICAL FUNCTION 1
CAN2=CANON. FUNCT. 2

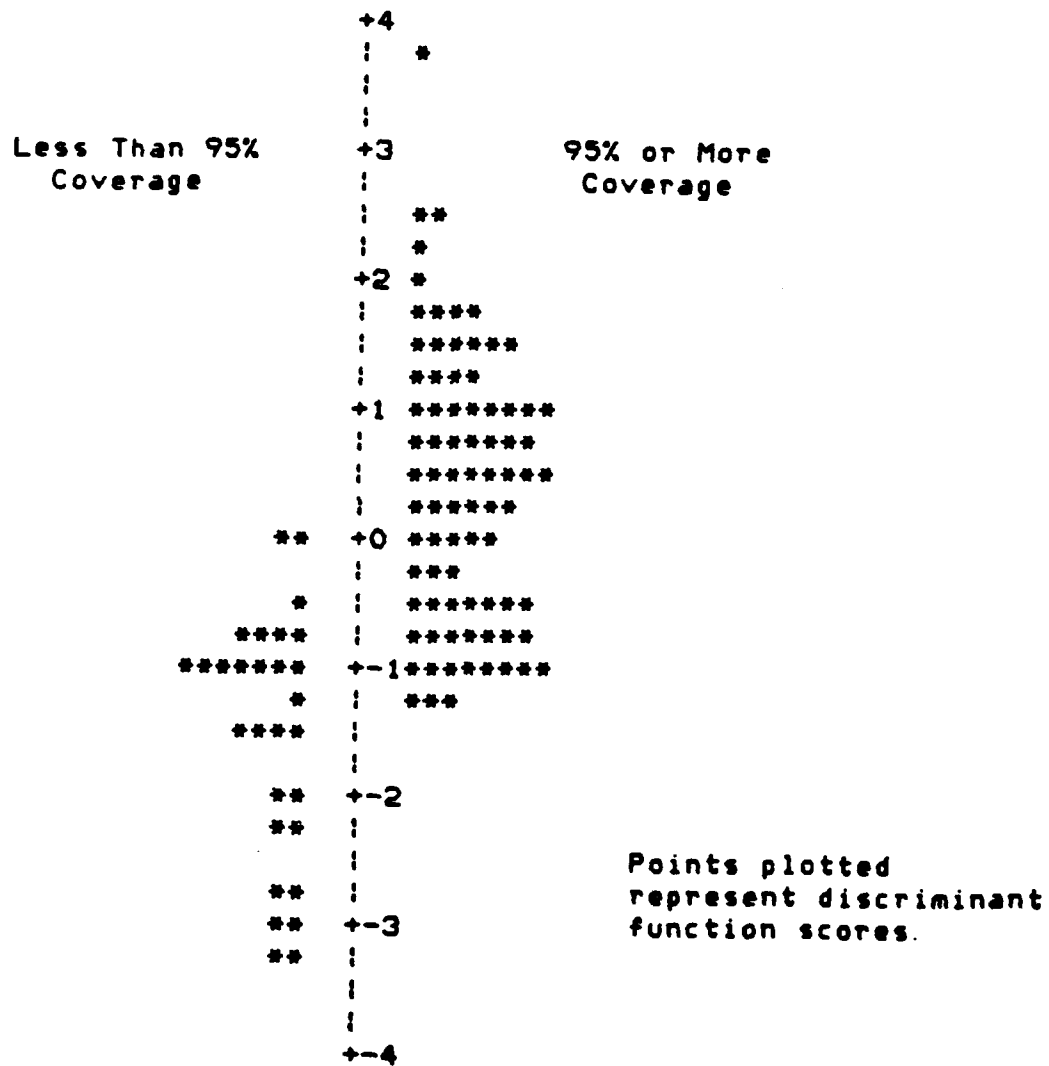


FIGURE 4. ONE FUNCTION PLOT OF CLASSIFICATION INTO OVER 95% OR UNDER 95% COVERAGE

	SI	CW	SW	PCTFth	MAXANG	ADJFmax	ADJFth	Frang
SI	1.00	0.38	0.06	0.57	0.56	0.40	-0.36	0.21
CW	0.38	1.00	0.38	0.95	0.93	0.62	0.56	0.91
SW	0.06	0.38	1.00	0.30	0.24	-0.04	-0.32	-0.09
PCTFth	0.57	0.95	0.30	1.00	0.63	0.80	-0.54	0.76
MAXANG	0.56	0.93	0.24	0.63	1.00	0.14	-0.49	0.49
ADJFmax	0.40	0.62	-0.04	0.80	0.14	1.00	-0.04	0.62
ADJFth	-0.36	0.56	-0.32	-0.54	-0.49	-0.04	1.00	-0.33
Frang	0.21	0.91	-0.09	0.76	0.49	0.62	-0.33	1.00

Table 1. Linear Correlation Among Solderability Indices

METHOD	UNITS WITH 95-100% COVERAGE		UNITS WITH 0-94% COVERAGE		PERCENT CORRECT CLASSIFI- CATIONS
	NUMBER MISCLASSIFIED	NUMBER CORRECTLY CLASSIFIED	NUMBER MISCLASSIFIED	NUMBER CORRECTLY CLASSIFIED	
SI	52	24	0	26	49%
IS	55	21	0	26	46%
MIL883	70	6	0	26	31%
MOD883	20	56	3	21	75%
DISCFN	12	64	3	23	85%

Table 2. Comparison of Solderability Test
 for Over 95% or Under 95% Coverage Classifications

	STANDARDIZED CANONICAL COEFFICIENTS		TOTAL STRUCTURE CANONICAL COEFFICIENTS		RAW CANONICAL COEFFICIENTS		DEFECT CATEGORY	PERCENT CORRECTLY CLASSIFIED	No. of UNITS
	FN1	FN2	FN1	FN2	FN1	FN2			
min	.57	.18	.50	.69	.019	.006	No Defect	43%	23
max	.54	-1.42	.80	-.17	.006	-.015	Asperous	85%	52
tan	.12	.62	.67	-.03	.002	.009	Dewetting	25%	4
end	-.30	-.18	.76	-.23	-.003	-.002	Pin Holes	40%	30
spike	.21	.70	.79	.13	.003	.011	Nonwetting	63%	8
1	.94	-.82	.67	.47	.011	-.009			
2	-1.44	1.89	.73	.43	-.015	.019	Overall	62%	117
5	1.05	-.74	.83	-.19	.011	-.008			

Table 3. Discriminant Analysis Coefficients
and Percent Correctly Classified into Defect
Categories

	STANDARDIZED CANONICAL COEFFICIENTS		TOTAL STRUCTURE CANONICAL COEFFICIENTS		RAW CANONICAL COEFFICIENTS		DEFECT CATEGORY	PERCENT CORRECTLY CLASSIFIED	No. of UNITS
	FN1		FN1		FN1				
min	.18		-.15		.006		No Defect	26%	23
max	1.05		.75		.011				
tan	-.34		.56		-.005				
end	.13		.79		.001		Some Defect	97%	94
spike	-.25		.56		-.003				
1	.94		.13		.011				
2	-1.93		.25		-.020		Overall	82%	117
5	1.15		.79		.012				

Table 4. Discriminant Analysis Coefficients
and Percent Correctly Classified into Defect
or No Defect Categories

	STANDARDIZED CANONICAL COEFFICIENTS		TOTAL STRUCTURE CANONICAL COEFFICIENTS		RAW CANONICAL COEFFICIENTS		PERCENT COVERAGE CATEGORY	PERCENT CORRECTLY CLASSIFIED	No. of UNITS
	FN1	FN2	FN1	FN2	FN1	FN2			
min	.94	-1.45	.60	-.43	.032	-.049	0-24%		0
max	1.30	-.29	.67	.57	.014	-.003	25-49%	100%	2
tan	.07	.23	.53	.59	.001	.003	50-74%	91%	11
end	-.33	.16	.65	.55	-.003	.002	75-94%	25%	16
spike	.67	.51	.82	.43	.010	.008	95-100%	98%	88
1	.98	-.11	.61	.13	.011	-.001			
2	-1.88	1.68	.62	.39	-.019	.017	Overall	87%	117
5	.22	-.86	.65	.53	.002	-.009			

Table 5. Discriminant Analysis Coefficients
and Percent Correctly Classified into Coverage
Categories

	STANDARDIZED CANONICAL COEFFICIENTS		TOTAL STRUCTURE CANONICAL COEFFICIENTS		RAW CANONICAL COEFFICIENTS		PERCENT COVERAGE CATEGORY	PERCENT CORRECTLY CLASSIFIED	No. of UNITS
	FN1	FN2	FN1	FN2	FN1	FN2			
min	.53		.42		.018		95% or Over	97%	88
max	1.45		.74		.019				
tan	-.11		.55		-.002				
end	-.48		.72		-.005		Under 95%	52%	29
spike	.66		.85		.010				
1	1.27		.57		.014				
2	-2.04		.59		-.021		Overall	90%	117
5	.45		.73		.005				

Table 6. Discriminant Analysis Coefficients
and Percent Correctly Classified into Over 95% Coverage
or Under 95% Coverage Categories

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ULTRASONIC SOLDERING

A NEW AND USEFUL TECHNOLOGY FOR THE ELECTRONICS INDUSTRY

by

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ABSTRACT

Pretinning of electronic component and connector leads to enhance and maintain solderability has become a major industry requirement with the implementation of DOD-STD-2000. A hot solder dipped surface is known to be one of the most solderable surfaces.

Ultrasonic soldering technology is being used to produce a hot solder dipped surface on leads without the use of flux thereby eliminating the need for solvent cleaning. In addition, certain leads that do not pass solderability testing when tinned using conventional means consistently pass solderability testing when tinned using ultrasonic means.

Ultrasonic tinning parameters including ultrasonic power level, dwell time, the number of dips, and rate of withdrawal are discussed as they relate to the success of the ultrasonic process. Nitrogen inerting to eliminate solder icicles and produce a better surface finish is also discussed.

GROWTH OF ULTRASONIC SOLDERING TECHNOLOGY

The phenomenon of ultrasonic soldering was first recognized in the early 1930's when it was discovered that ultrasonic agitation in molten solder could remove oxides from non-ferrous metals and promote metallurgical bonding. The process remained a laboratory curiosity until the mid 1960's primarily because of equipment limitations. Ultrasonic equipment of the time was not compatible with the hot working environment required for soldering.

The first practical ultrasonic soldering device was built by Mullard in England and was used by Clairex Corporation to apply solder to the edge of a photocell on ceramic as an electrical connection.

In 1976, NASA named ultrasonic soldering as the "preferred" method of pretinning conductors in NHB 5300.4(3A-1) December 1976. The primary benefit recognized was the unique ability of the ultrasonic soldering process to quickly and thoroughly remove gold plating from surfaces that were to be part of a soldered connection.

Although it was known that ultrasonic soldering had application in the electronics industry, increased use of the process was limited by equipment cost and the lack of a driving industry need for the technology. In the intervening years, the use of ultrasonic soldering for electronics applications has grown slowly. Numerous applications have been explored and a number of ultrasonic soldering devices have been put into operation. For the most part, however, the industry is, even today, either misunderstanding or unaware of ultrasonic soldering and its capabilities.

NEW OPPORTUNITIES FOR ULTRASONIC SOLDERING

Recent changes affecting the electronics industry call (among other things) for an increase in the solderability of leads and reduced use of CFC solvents. Ultrasonic soldering can play a major roll in the attainment of these and other goals. I welcome the opportunity to explore these opportunities with you today.

MECHANICS OF SOLDERING

No matter how it is accomplished, soldering or tinning require that molten solder alloy come into contact with an oxide free base metal at an elevated temperature in the absence of oxygen so that metallurgical bonding can occur. These requirements can be met using either a flux or an ultrasonic process.

FLUX SOLDERING

In conventional soldering, a flux is applied to the area where solder is to be applied prior to the start of the soldering operation. The flux is an acid which chemically removes oxides. Fluxes used range in strength from relatively mild non-activated rosin to the extremely active zinc chloride fluxes depending on the thickness and nature of the oxide to be removed from the base metal. Although fluxes are sometimes thought to also clean, their primary purpose is to remove oxides. They are notably poor "cleaners" for anything other than oxides.

With the temperature at or above the melting point of the solder alloy and the oxides chemically removed, a metallurgical bond is formed between the solder alloy and the base metal when they contact each other.

Fluxes also act as wetting agents, reducing the contact angle between the solder and the base metal. This property leads to wicking and capillary flow which is essential for solder to penetrate into typical solder joints such as those found on both SMT or through-hole printed circuit boards.

ULTRASONIC SOLDERING

In ultrasonic soldering, ultrasonic energy is introduced into molten solder using one of several means. The totally activated pot has emerged as the technology of choice due to the relatively large working area it can offer and the simplicity and reliability of this type of equipment.

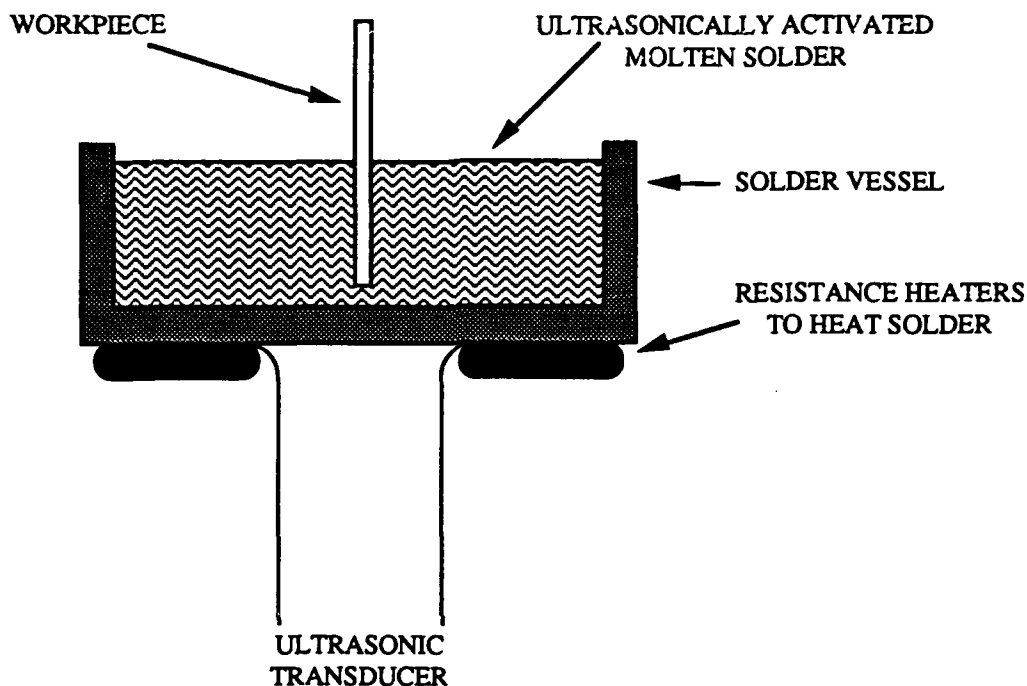


FIGURE 1. Schematic diagram of ultrasonically activated solder pot.

Vibrations generated by a transducer attached to the outside surface of the solder pot are transmitted to molten solder in the pot. The result is cavitation of the molten solder. Oxides are mechanically removed from submerged work pieces by the forces of imploding cavitation bubbles. While the workpiece is still submerged, a metallurgical bond is formed between the solder alloy and the base metal.

BENEFITS OF ULTRASONIC SOLDERING

Recent changes in regulations and specifications aimed at reducing the use of CFC solvents and establishing higher standards for the solderability of leads are of primary concern in the electronics industry today. Ultrasonic soldering technology offers immediate solutions in both areas.

ELIMINATION OF FLUX

The ultrasonic soldering process does not use flux. The immediate benefits are the elimination of fluxing operations and the procedures and equipment associated with them. Flux storage, mixing, handling, venting and cleanup are all eliminated.

REDUCTION IN USE OF CFC SOLVENTS

Surfaces and parts soldered using the ultrasonic process require no cleaning after soldering as there is no flux residue. This is especially beneficial if the flux used would require removal using CFC solvents.

IMPROVED SOLDERABILITY AND AGING RESISTANCE

Tests conducted by users of the ultrasonic process have shown ultrasonically tinned leads to have consistently higher solderability and resistance to aging than those tinned using flux. This is especially evident on gold plated connector leads where the presence of organics is desirable to reduce insertion forces. The mechanical abrasion due to ultrasonic cavitation is apparently able to effectively tin these surfaces when even the most active allowable fluxes can not.

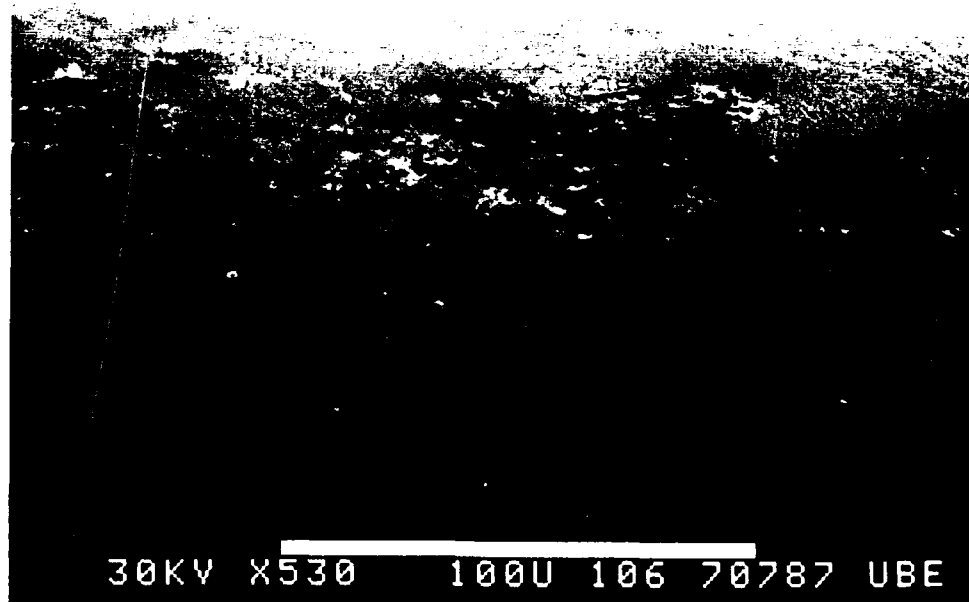


FIGURE 2. SEM Photograph of gold plated connector lead soldered using flux with evidence of unsoldered areas.

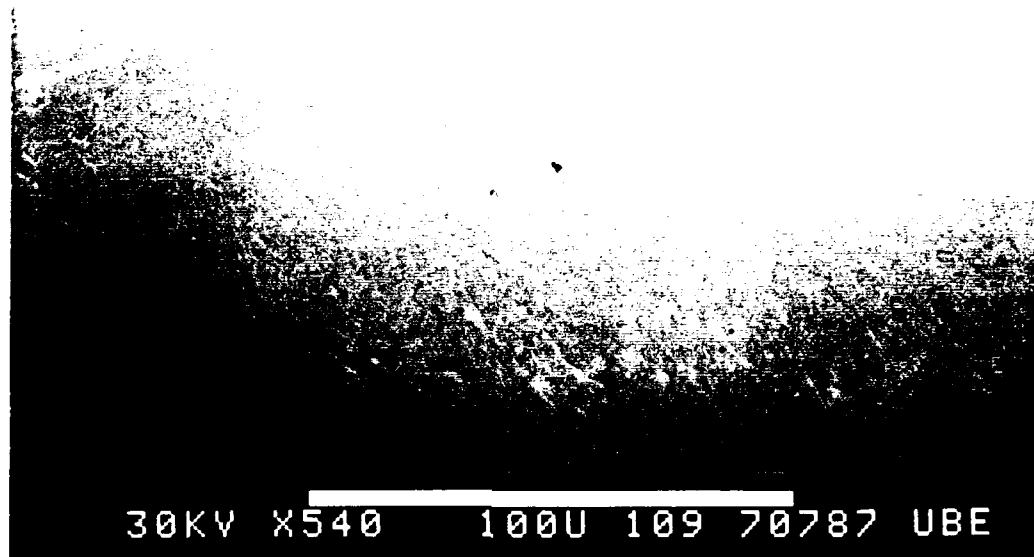


FIGURE 3. SEM Photograph of gold plated connector lead from the same lot as Figure 2 soldered using ultrasonic soldering techniques.

The increased resistance to aging can be attributed to the elimination of flux and its residues encapsulated in the solder coating.

It is interesting to note that one of the methods recently touted to enhance solder coverage and age resistance is relative motion between the solder and the base metal during soldering through the motion of a solder wave. The mechanical action of ultrasonic cavitation is an even more effective extension of this enhancement.

LESS ACTIVE FLUXES REQUIRED FOR BOARD SOLDERING

The improved solderability afforded by the use of ultrasonic techniques may allow assembly operations to be accomplished with fluxes having lower solids content than otherwise required. In many applications, this may mean that the flux residues from the assembly operation need not be removed. If this is the case, the consumption of CFC solvents will be further reduced.

ELIMINATION OF WICKING

As the ultrasonic soldering process does not use flux, the surface tension reducing properties of flux are also missing. There is no wicking using the ultrasonic soldering process. Although this was at first thought to be a shortcoming as it eliminated many assembly soldering operations from consideration, it has proven to be a benefit in other areas. For example, in the case of plated stranded wire, heat sinking is not required to prevent wicking of solder under the insulation.

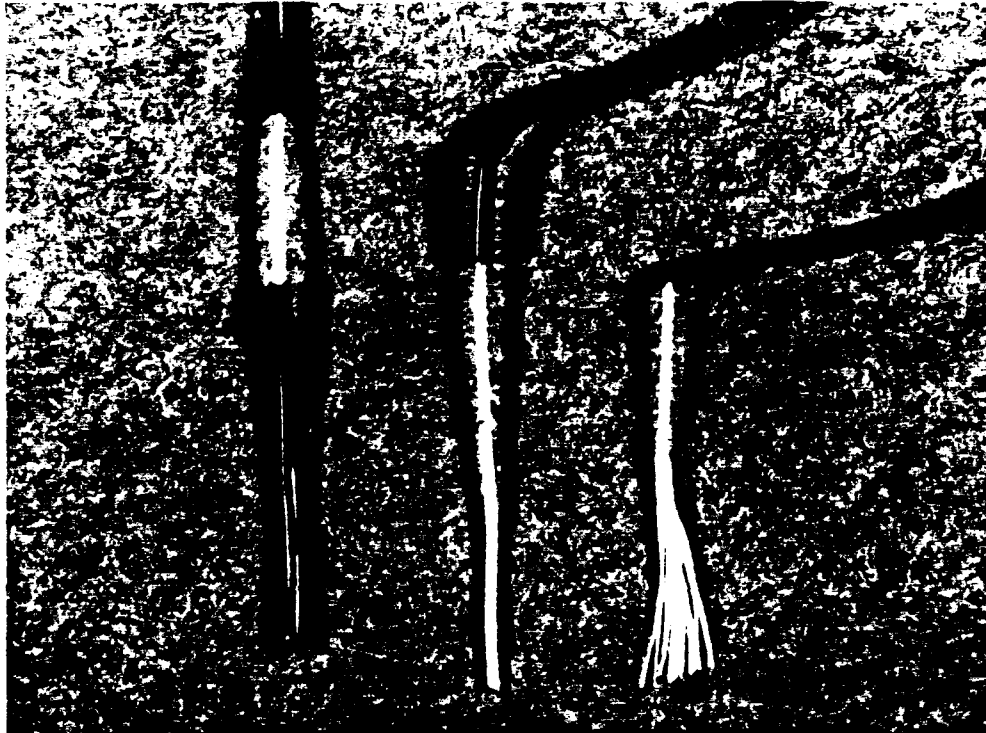


FIGURE 4. Plated, stranded wire dipped in solder with the insulation parted as shown at the left. The center wire was tinned using flux and the wire on the right was tinned ultrasonically. The insertion depth in both cases was to a point slightly above the terminus of the bare portion of the wire. The wire strands which were covered by the insulation during dipping are bonded together in the flux soldered sample while they remain separate in the ultrasonically soldered sample. The bend point above the soldered portion of the wire indicates solder penetration.

There is also no danger of solder wicking up into contacts in connectors.

THE NEW TECHNOLOGY OF ULTRASONIC SOLDERING

Effective use of ultrasonic soldering as any other technology requires an understanding of the process and its parameters. Implementation is not as simple as replacing a

conventional solder pot with one having ultrasonic transducers. Procedures and conceptions of the soldering process also need revision to accommodate ultrasonics. Indeed, ultrasonic soldering has no application in many common soldering operations.

Although many parameters from conventional soldering apply to the ultrasonic process, there is at least one new one to consider and some rethinking required on others.

MULTIPLE DIPPING

In conventional soldering, parts are normally dipped once to tin. Although a second dip may be used to smooth the solder or in an attempt to improve solder coverage in a marginal case, multiple dipping is not a required part of the process.

In ultrasonic soldering, multiple dipping is required to achieve total solder coverage. On the first dip, adsorbed gasses on the surface of the base metal expand and are trapped between the molten solder and the surface to be tinned. These "balloons" of gas effectively cushion the ultrasonic energy in their immediate area preventing both their displacement and oxide removal. On withdrawal, these "balloons" are released at the solder surface. When the now gas-free part is re-inserted, ultrasonic energy can reach and remove the oxides to allow bonding to take place.

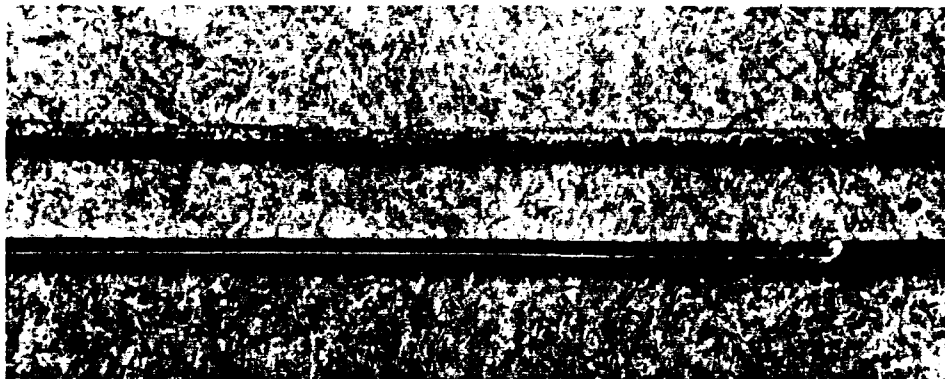


FIGURE 5. Two bare copper wires tinned to illustrate the effect of multiple dipping on solder coverage. The top wire was dipped into the ultrasonic solder pot for a single dip of one second duration. Untinned areas are evident. The lower wire was dipped twice for a total exposure of 2 seconds and is completely solder covered.

In the case of a particularly heavily oxidized part, an additional dip may be required to "rinse off" removed oxides. Additional dips in the ultrasonic process are appropriate in the same circumstances normally requiring additional dwell time using the conventional flux soldering process.

DWELL TIME

In the above paragraph, the number of dips parameter in ultrasonic soldering was likened to the time parameter in conventional soldering. Our experience has shown that the duration of each dip is relatively unimportant as long as the part reaches the soldering temperature. For example, two dips with a total immersion time of 2 seconds is much

more effective than a single dip of 10 seconds duration using the ultrasonic process. Increasing the total duration of the two dips to 20 seconds or more does not improve soldering.

CLEANING

Just as in flux soldering, the parts to be ultrasonically soldered must be suitably clean prior to introduction into the ultrasonic solder pot. Finger prints and other light contamination are no problem and will be removed by the heat of soldering and mechanical agitation due to ultrasonic energy. Epoxy, tape residue and other heavy contamination will prevent soldering just as they do when flux is used.

SOLDER TEMPERATURE

The solder temperature used for ultrasonic soldering can often be lower than that required for flux soldering. Higher temperatures in conventional soldering play a major roll in flux activation which is not an issue in the ultrasonic process. Higher temperatures in the ultrasonic process can speed heat transfer to the part which can save time with some configurations but also tend to speed dross buildup.

APPLICATIONS CONSIDERATIONS

The usefulness of a technology is in its application. Many good, immediate applications have been found for the ultrasonic soldering process. Others have been identified which although they require process changes are practical alternatives in certain cases. Finally (and perhaps most importantly), areas where there is no application have been identified and are understood.

WORKING APPLICATIONS

There are several working applications of ultrasonic soldering in the electronics industry. The current focus is on the the preparation of leads to enhance solderability prior to a subsequent assembly operation. Ultrasonic soldering, due to its mechanical nature is especially effective in fast and thorough removal of gold platings.

Connectors

The tinning of connector leads was among the first uses of ultrasonic soldering in the electronics industry. Ultrasonic soldering gives a reliable solder bond without the problems of flux and solder wicking up into the body of the connector and the contacts. Elimination of cleaning after soldering is of special significance in the case of connectors because of the number of capillary spaces in their construction which tend to hold solvent.

Gold Plated Leads

The removal of gold plating is an important part of the process in tinning a wide variety of leads to prevent gold embrittlement. The mechanical action of the ultrasonic process is able to remove gold from a lead by erosion and mechanical agitation on a micro scale at the

solder - work surface interface. Because the removed gold is dispersed, multiple pots are not required.

Plated Stranded Wire

Ultrasonics can tin plated, stranded wire without risk of solder wicking under the insulation. This is due to the fact that there is no capillary flow in the ultrasonic process. Using conventional means, a heat sink must be used to prevent wicking.

Recovery

In many cases, surfaces unsuccessfully tinned using other means can be recovered using the ultrasonic soldering process. The mechanical action of ultrasonic energy can remove oxides and other contaminants that are not removed by the chemical action of fluxes.

Thick Film

Some circuit paths on thick film substrates can be tinned ultrasonically.

APPLICATIONS REQUIRING NEW PROCEDURES

In some applications, ultrasonic soldering can be used to replace conventional soldering if the joining procedure is changed.

"Wrap" Joints

Without capillary flow, it is not possible to join wires wrapped together or around terminals in a simple dip operation. Although a superficial coating of solder may be applied, there will be no penetration between the wires and/or terminal. Pretinning of the individual components to be joined prior to assembly and re-dipping after assembly can provide a reliable joint.

UNSUITABLE APPLICATIONS

There are several applications where the ultrasonic process is not suitable. In most cases, this is due to the lack of capillary flow.

Unplated Stranded Wire

Solder will not penetrate between the strands of unplated stranded wire due to the lack of capillary flow. Plated strand wire or wire made up of tinned strands will solder successfully using the ultrasonic process. The solder follows the prepared surface to penetrate the strands.

Printed Circuit Boards

Capillary flow is the primary mechanism in both through hole and SMT circuit board soldering. These are not applications for the ultrasonic soldering process.

Insulated Magnet Wire

The so-called heat strippable magnet wires are actually stripped by a combination of heat breaking down the insulation and the action of flux lifting off the charred insulation residue. Heat stripping can not be accomplished without flux.

PROCESS ENHANCEMENTS

Full industry implementation will bring a number of enhancements to the ultrasonic soldering process. Among them are nitrogen inerting and automation.

NITROGEN INERTING

The technology for blanketing the surface of a solder pot with nitrogen to alter the surface tension behavior of the solder is applicable with ultrasonic soldering. The presence of nitrogen over the pot reduces bridging, eliminates icicles on the ends of leads and minimizes dross buildup on the surface of the solder. Many fine pitch components have been successfully soldered using an ultrasonic solder pot with a nitrogen blanket.

AUTOMATION

Automation of the ultrasonic soldering process will be required for high volume connector and lead tinning operations. Some work has already been done in this area with good results. It appears that the process is easily automated.

ULTRASONIC SOLDERING EQUIPMENT

Ultrasonic soldering equipment is readily available with standard pot volumes ranging from 3" in diameter to over 15" in length. The system consists of the heated, ultrasonically activated solder pot and a control cabinet containing the ultrasonic generator and controls.

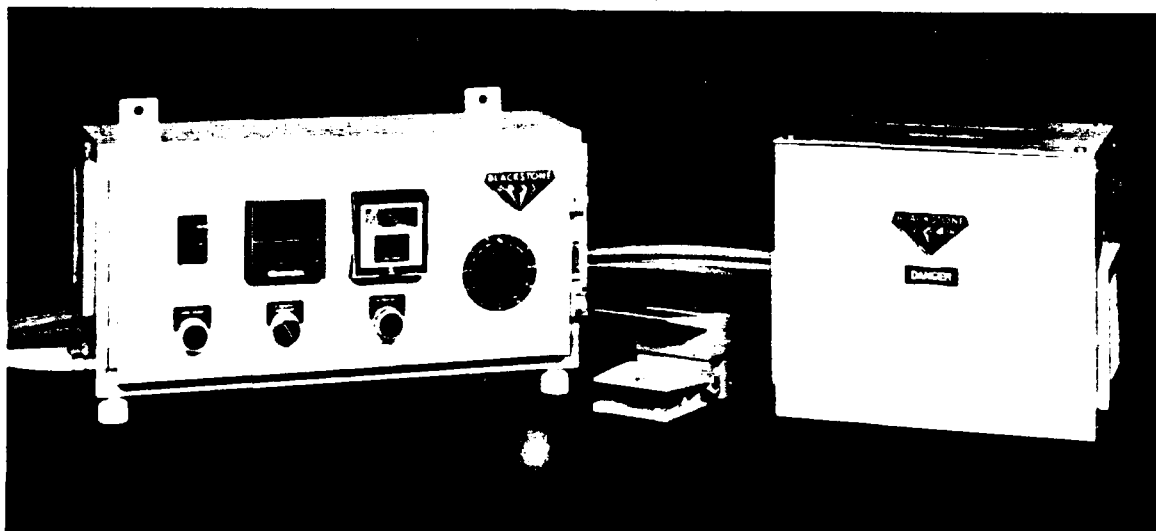


FIGURE 6. Ultrasonic soldering system. The working pot dimensions of this system are 4 inches by 9 inches by 3 inches deep.

SUMMARY

Ultrasonic soldering despite its age is still young. There are obviously still many opportunities for proprietary processes to be developed along with several new applications. There is an industry need for the technology. Once the process details are understood, the electronics industry can utilize ultrasonic soldering to achieve a number of important goals. We hope that this effort today is a start toward industry awareness of a process which has a great deal to offer.

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AN IMPROVED PRINTED CIRCUIT BOARD SOLDERABILITY EVALUATION

by

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ABSTRACT

Modern electronics equipment assembly is increasingly becoming a solder application process. When this process is flawed by solderability problems with component leads, printed circuit boards, or soldering machine processes, solder joint repair can become a significant part of the assembly operation cost.

A process was described in the Autumn 1985 Schloetter International publication which provided increased solder coating thickness at the "knee" of printed circuit board plated through holes after fusing. Increased solder coating at the knee of the plated through holes enabled solder to rise through and onto the topside pads to more reliably/consistently form topside fillets.

The process involves use of a thin layer of pure lead electrodeposited immediately prior to electroplating tin-lead in the printed circuit board fabrication process. Process chemicals and technical support are available in this country from LeaRonald Inc. (LRI) of Freeport, New York.

This paper reports on effort to evaluate the process and its capability to improve long-term solderability of printed wiring boards through changes to the tin-lead plating process.

Committee discussions at IPC and other industry conferences have in the past year or two started to focus on artificial aging of component leads and printed wiring board coupons as a measurement criterion of improved solderability.

Artificially aged coupons and production circuit board evaluations were both used in this effort.

INTRODUCTION

Printed wiring board (PWB) solderability, component solderability and the mass soldering process are the three major items in electronics assembly operations. When assembly volume is high, boards and components are more likely to be fresh, and the soldering process is in a steady, controllable state. Short assembly runs of many different assembly part numbers, a large number of component types with individually low usage, and start/stop operation of the wave solder machine, are at the more difficult end of the assembly operation spectrum. The latter description is characteristic of our assembly area at Rockwell-Collins Defense Communications division. Each of the three soldering assembly factors must be right, or soldering defects are likely to be an unacceptable assembly cost, not to mention any quality issues.

This paper is concerned with the PWB solderability and, in particular, wave soldered boards, with plated through holes (PTH's). The solderability defect most obvious either after assembly, or after coupon solderability testing, is whether solder has risen up a PTH and flowed out onto the surface pad, or whether it has stopped at the knee of the PTH (Figure 1). The background for the paper started several years ago, when the production area had well over a dozen touch-up operators behind the wave soldering machine, repairing imperfect solder joint fillets. A collective effort to reduce the touch-up effort was mounted, and the situation improved.

In the PWB area, the activity started with a solderability specification based on IPC-S-804, but including an artificial aging requirement: a) 16 hours of dry heat at 125 °C; or b) 8 hours of steam aging. A special coupon was prepared to provide more consistent test (Figure 2). Test samples were initially "dip" tested until a growing correlation between problem boards and "capped" holes convinced us to move to "float" testing of coupons or samples.

Our division is a user of PWB's, not a fabricator. Consequently, there were a lot of discussions with suppliers about orders rejected for poor solderability, but there was improvement. Just not enough of it.

There continued to be too many orders where we had to back down from aged solderability to unaged test results for acceptance which predictably showed up as a higher rate

of wave soldered defects. Improved PWB solderability was still an up and down ride with fabricator process variables.

LEAD BARRIER PWB PLATING

Schloetter Ltd. of England reported in a 1985 company paper a new PWB plating process being used on circuit boards supplied to Siemens, the German electronics firm.

The report contained cross-section photographs of "weak knee" plated through holes described as solderability problems which matched very closely our own experiences. The cross-sections showed essentially no plating at the knee, and solder from a "float" test rising to the knee and stopping without flowing onto the PTH pad surface. These were examples of standard PWB reflowed tin-lead electroplating. Along with them were photomicrographs of reflowed tin-lead with thick coverage at the knee of the hole, plus a description of the process.

This paper relates some of the lead-barrier process experiences to date from working with two PWB suppliers to implement the process and observe the results on both test coupons and PWB's for production use.

This paper consists of two parts, early process evaluation work performed by V. L. Carlson, J. W. Evans, J. P. Besong, et al., (Reference 1) followed by an interval of production results monitoring, and then a second look at the process with another PWB supplier.

PROCESS EVALUATION, PART 1

SOLDERING AND SOLDERABILITY

Prior to discussing the Pb barrier, a review of soldering and degradation of solderability is in order.

WETTING

The objective of soldering is to mechanically or electrically attach components to form an assembly. Wetting of the surfaces to be joined by molten solder is necessary to allow the metallurgical interaction, which produces a suitable joint to take place. Simply stated, wetting occurs when the surface energy of the component surfaces is greater than that of the solder (Reference 2). Flux is used to break down substrate oxides and remove contamination to allow this condition to occur. Upon

intimate contact of the molten solder with the substrate, the chemical reactions and dissolution of substrate atoms occur, which results in an intimate metallic joint. In the case of the tin-lead (SnPb) solder/copper (Cu) system, a CuSn intermetallic compound (IMC) forms as Cu_6Sn_5 or Cu_3Sn .

If the flux used is not effective in modifying the surfaces of the substrates to be joined, nonwetting will occur. Nonwetting is a condition in which the solder does not achieve any intimate contact with the base material as a result of a physical barrier such as heavy oxide or oils (Reference 3). De-wetting, another soldering defect, occurs when the solder retracts into mounds in much the same way water beads up on a freshly waxed car (Reference 3). Severe de-wetting will result in very poor joint quality and will occur on a surface or subsurface which has severely degraded with time and temperature.

DEGRADATION OF THE SnPb/Cu SYSTEM

Solderability degrades with time and temperature eventually leading to de-wetting or nonwetting conditions. In the case of reflowed SnPb solder on Cu, this degradation process generally occurs by two phenomena: IMC growth and oxidation. However, IMC growth often plays the "key role" in the degradation process (Reference 4).

As previously mentioned, two IMC's will form as a natural part of the soldering process. During PWB fabrication, Cu_6Sn_5 will form in the electroplated SnPb coating and fusing process. Shortly thereafter, depending upon the temperature exposure history, and lack of Sn, the second IMC in the SnCu system will form: Cu_3Sn . The IMC layer grows as a duplex layer by an Arrhenius relationship. Accelerated growth of the IMC layer occurs at each process bake or high temperature process step (soldermask cure, moisture removal, etc.) in the manufacture of the PWB.

IMC growth is fueled by diffusion of Sn and Cu. As the layer grows, the solder is depleted of Sn (Reference 4). A Pb rich layer will eventually form adjacent to the IMC, encouraging the growth of Cu_6Sn_5 (Reference 4) between the Cu_6Sn_5 layer, and the copper. The Cu_6Sn_5 is highly unsolderable and domination of IMC layer (surface exposure) by this species will lead to de-wetting during assembly (References 2, 4). The effect of this

degradation mechanism on solderability is greatly pronounced by thin solder coatings or a Pb rich solder (lack of Sn) coating.

THE "WEAK KNEE"

The rims or "knees" of the plated through holes (PTH's) are often the first areas to display poor solderability on a PWB. See Figure 1. This is due primarily to a thin coating of SnPb which occurs at the knee during reflow. Surface tension will tend to pull the molten solder from this area. Typical reflowed fluoborate SnPb coatings on PWB plated through hole knees are about 1 micron thick, and frequently less. See Figure 3. (One micron equals approximately 40 millionths of an inch.) In extreme cases, Cu_6Sn_5 will be exposed and eventually oxidize to become unsolderable. In addition, the IMC in the knee area will rapidly convert to Cu_6Sn_5 , an unsolderable IMC due to the activity of Cu diffusion and the relatively low volume of Sn. Consequently, the knee is a prime candidate to show poor solderability in the form of nonwetting or de-wetting during assembly.

THE Pb BARRIER

Until recently, little progress has been made toward solving the problem of the weak knee. However, in Europe, Dr. G. Strube of Schloetter Co., Ltd., has described a solution (References 5, 6). The process, according to Dr. Strube, involves putting down a layer of Pb, 1 to 5 microns thick, from a nonfluoborate bath, prior to depositing a nonfluoborate SnPb finish. The Pb layer reportedly serves to strengthen the knee by leaving a thick solderable coating after reflow and by eliminating IMC formation during reflow (References 5, 6).

The major thrust of the early investigation was to examine the metallurgical characteristics of this system and functionally test circuit boards fabricated with the lead barrier.

EXPERIMENTAL METHODOLOGY

Characterization studies were performed in conjunction with a cooperative supplier on actual PWB samples. The samples consisted of PWB's with no Pb barrier, and 1, 3 and 5 minutes of Pb barrier plated at 15 amps/ft². All samples were then overplated with eutectic SnPb. All the samples were plated in nonfluoborate baths. Fluoborate baths of

lead and tin-lead were tried initially, but resulted in numerous unreflowable slivers after etching and reflow of the test PWB's. Slivering does not occur with the nonfluoborate bath electroplated coatings, as the lead seems to dissolve into the tin-lead. As the lead barrier thickness increases, the reflowed tin-lead does become rough and grainy. A lead barrier thickness of 5 microns yields an unacceptably rough finish. Initially, thickness measurements were made on nonreflowed samples. The rest of the studies were performed on reflowed SnPb samples. Samples were examined in the unaged and aged conditions.

Functional testing was also done on the lead plated circuit boards (after earlier encouraging results on coupon samples) to determine solderability, soldermask and Sn/Pb adhesion, thermal cycle fatigue resistance, and insulation resistance. The board testing program is illustrated in a flow diagram, Figure 4.

The solderability testing was done for "as received," dry aged, and steam aged boards. The dry aged boards were tested by float testing for ten seconds on a solder pot at 474°F.

The moisture and insulation resistance testing was done per MIL-P-55110C, Amendment 5 and MIL-STD-202, Method 106. Each board was given ten humidity cycles of 16 hours each and cycles from 25°C to 65°C, with up to 98% humidity. The boards were also tested for soldermask adhesion and Sn/Pb adhesion.

Boards were populated in production with both surface mount parts and through hole components. After a double solder cycle of vapor phase reflow soldering, lead trimming, wave soldering and cleaning cycles, the boards were inspected by production inspectors. After inspection, the boards were divided into two groups. One group of boards was tested for Sn/Pb and S/M adhesion, while the other group was thermal cycle fatigue tested between the temperature limits of -55°C to +125°C at a rate of 1 cycle per hour.

RESULTS

The Pb thickness measurements are summarized in Figure 5. The measurements shown were made on unreflowed specimens at points located on surface circuitry. The surface measurements fell reasonably close to thicknesses predicted by Faraday's law. Observation of Pb thickness

near the PTH knees indicated a generally thicker range with greater variation. This was most likely due to current concentrations near the knee due to geometric effects on the electric field during plating. However, these observations were not quantified.

Several interesting observations were noted upon inspection of the metallurgical sections. As Figures 6a through 6d indicate, the knee area is covered by a thick layer of SnPb in all cases, including the sample without Pb. Second, the reflow process dissolved all the Pb into solution on the 1-minute Pb barrier samples. At thicker Pb levels, a discrete layer was maintained around the knee region. In many cases, however, much of the Pb was dissolved in the PTH and on top of circuitry and pads. However, the remaining thickness is on the order 2 to 3 microns--several times the thickness of reflowed fluoborate SnPb, or hot air reflowed PWB's.

The largest visual difference between boards with and without the lead plating is the increased surface roughness of lead plated boards. As the lead plating thickness increases, the surface roughness become greater, and overall tin-lead composition ratio may shift significantly from eutectic.

DISCUSSION

The surface thickness of the electroplated Pb is predictable; however, the Pb thickness around the knee areas will be somewhat thicker due to increased current densities. When reflowed, much of the Pb is dissolved into overplated SnPb. A thin Pb layer of about one micron will be completely dissolved, while thicker barriers of Pb will maintain some areas of discrete Pb, particularly around the knee. Reflow process time does have an effect on dissolution rate. The Pb barrier appears to be very effective in "strengthening" the PTH knee by providing a thick solderable coating around it. This is most likely due to reduction in surface tension effects due to dissolution of Pb during reflow, and possibly assisted by a higher (lead rich) melting point. Also, the nonfluoborate SnPb alone left an appreciable thickness around the knee in comparison to a standard reflowed fluoborate SnPb deposit.

The surface composition of Pb barrier boards is affected by the Pb barrier thickness. A very thin layer of Pb will completely dissolve and appreciable IMC will form. The dissolved Pb will enrich the SnPb and lower the Sn

content. Sn depletion will also occur with IMC formation. Consequently, a board with a very thin Pb barrier layer will be richer in Pb at the surface than a board without a barrier layer. As Pb thickness increases, less IMC will form at reflow. Sn depletion is retarded as diffusion and dissolution of Sn are slowed by a thicker Pb layer. As a result, boards with thicker lead tend to have an increase in Sn content at the surface. A rough grainy surface appearance with thicker Pb layer suggests lead-rich nodules within the coating.

SOLDERABILITY TESTS

Solderability of the circuit boards was checked by float testing boards for ten seconds in a 474°F solder pot using type R flux. Boards with one and three minutes of nonfluoborate Pb barrier plus boards with fluoborate and nonfluoborate Sn/Pb only were tested. Boards were tested both unaged and artificially aged. Table 1 illustrates the results of the dry aged solderability testing:

TABLE 1. Percent of Acceptable Plated Through Holes.

DRY AGED	FLUOBORATE	NON- FLUOBORATE	NON- FLUOBORATE	NON- FLUOBORATE
	Sn/Pb	Sn/Pb	(1 min.) Pb	(3 min.) Pb
UNAGED	10	100	100	100
16 HR @ 125°C	0	90	100	100
8 HR @ 155°C	0	70	100	100
32 HR @ 155°C	0	25	100	100

As illustrated in Table 1, the solderability of both the 1-minute and 3-minute Pb barrier-plated boards exhibited excellent solderability. Although showing good solderability, the 3-minute Pb boards had a rougher surface texture than the 1-minute Pb. Also, the 3-minute Pb has nodular growth on the edge of pads and lines. The 1-minute Pb boards are slightly rougher than either the fluoborate or nonfluoborate Sn/Pb (only) plated boards.

Circuit boards were also steam aged and solderability tested (float test). Table 2 illustrates the results for the steam-aged solderability testing:

TABLE 2. Percent Solderability of PTH's After Steam Aging.

	FLUOBORATE Sn/Pb	NON- FLUOBORATE Sn/Pb	NON- FLUOBORATE (1 min.) Pb	NON- FLUOBORATE (3 min.) Pb
UNAGED	16	85	90	100
8 HRS	0	67	89	96
16 HRS	0	16	3	91
32 HRS	0	9	0	91

The results from steam aging were not as good as the results for dry aging. However, a great improvement is noted when comparing the Pb underplated boards to currently used fluoborate acid Sn/Pb plating. Steam aging produces oxides on the surface of the Sn/Pb, while dry aging promotes IMC growth between the Sn and circuit board copper.

INSULATION RESISTANCE RESULTS

Moisture and IR tests, per MIL-P-55110C, Amendment 5, were performed on two coupons from each panel of fluoborate, nonfluoborate, 1- and 3-minute Pb underplated boards. The initial resistance of all samples between layers was $>1 \text{ T}\Omega$. The post-moisture IR between layers was $>1 \text{ T}\Omega$; thus, all samples passed the IR tests.

SOLDERMASK AND Sn/Pb PLATING ADHESION TEST

Nonfluoborate and 1-minute Pb plated boards were tested for plating adhesion and S/M adhesion tested per IPC-SM-840 A. All boards passed the plating adhesion test in the "as received", 16-hour bake at 125°C and 16-hour bake at 155°C with no plating lift.

PART 1 CONCLUSIONS

- (1) Thin Pb barriers, in the range of 1 to 2 microns, will completely dissolve in the reflow process. Thicker barriers, greater than approximately 2 microns, will tend to have regions of undissolved Pb, particularly around the knees. However, the actual amount of Pb dissolution is influenced by reflow time and temperature.

- (2) The Pb barrier retards the degradation of solderability by at least two methods:
 - (A) The knee area is reinforced with a thick solderable coating of SnPb.
 - (B) IMC formation and Sn depletion are retarded during reflow by the presence of the Pb barrier.
- (3) The nonfluoborate SnPb appears to be superior to conventional fluoborate SnPb, as it does not severely thin down at the knee during reflow.
- (4) One minute of Pb underplating, approximately one micron thick, produced good appearance and maintains good solderability. Thicker Pb plating has good solderability; however, it produces boards with rough, nodular growth areas on the pads and lines. In general, the appearance of the lead barrier-plated (and reflowed) PWB's is duller and flatter than fluoborate plated/reflowed boards.
- (5) The Pb underplated boards passed all qualification testing for S/M and Sn/Pb adhesion, thermal fatigue cycling, and insulation resistance.

PROCESS EVALUATION, PART 2

A SECOND LOOK EVALUATION

Following the initial investigation, the process was used first on limited production quantities of PWB's, followed by larger quantities. During a period of about 18 months, over 10,000 PWB's fabricated with the process were used. Solder defect rates from assembly inspection were collected on a group of 12 part numbers in this period. These part numbers were selected because there was wave solder defect data rates available on them from the six months prior to implementing the lead barrier process.

Initial results after implementation showed a nearly 2:1 reduction in wave solder defect rates. Later results tended to drop with time for various reasons.

Then, a second circuit board supplier started using the process, but was unable to maintain consistent and successful solderability results. This was an opportunity to reevaluate the process.

Part 2 of this paper describes the second lead barrier plating process evaluation.

LEAD BARRIER PLATING EVALUATION PLAN

The purpose of the evaluation was limited in scope to collect data which would do two things:

1. Review for repeatability in a short period of time the findings of the work done previously.
2. Provide a starting point for plating parameters for a facility desiring to upgrade circuit board solderability.

It is recognized that much additional process characterization could be done to evaluate more completely the process and establish process control limits.

The approach for this second lead barrier evaluation consisted of:

1. Review the plating bath installation and operating parameters at the chemical supplier's (LeaRonald's) facility.
2. Define a consistent set of lead barrier bath operating parameters, using an "aged" solder float test as the measuring stick of coupon solderability.
3. Set up the test parameters to be evaluated for statistical significance of variables by statistical process control methods.
4. Prepare a 4-layer multilayer board with multiple solderability test coupons (Figure 7).
5. Evaluate the overall surface thickness measurement consistency/correlation of X-Ray Fluorescence (XRF) and Scanning Electron Microscope (SEM) equipment on the combined coating of lead barrier underplate followed by tin-lead overplate prior to reflow.
6. Perform reflow of individual coupons from a given plated sample at three different temperatures (hot oil reflow) to look for resultant variations of remaining coating thickness on the knee of the plated through holes.

7. Prepare cross sections and photographs to document the various plating and reflow combinations prior to solderability testing.
8. The test conditions used and data collected on the samples are shown in a matrix format (Figure 8).

TEST PROCEDURE AND DESCRIPTION

The test boards were prepared by a circuit board supplier through the standard copper pattern plating process step. Pattern photo resist was used on all sample boards.

Twelve sample boards were lead barrier plated, followed by tin-lead plating.

An additional four sample boards were also identified, and plated with tin-lead plating only at LRI. Also, four sample boards were plated with tin-lead only by the PWB supplier. Two of those samples, numbers 17 and 18, are also included in the test data and evaluation as control samples.

The 12 samples plated with a lead barrier underplate were all electroplated in a 1-gallon glass tank with filtration, since LRI has not had sufficient industry demand for the process to set up a pure lead bath in their prototype circuit board plating line. All samples were overplated with tin-lead in the prototype plating lines of approximately 50-gallon tanks. Continuous 10-micron filter filtration of the pure lead tank is recommended (similar to the tin-lead bath).

The plating current density levels selected for the test were consistent with the desire to keep the lead barrier deposit from displacing the total plating composition of tin-lead too far from the nominal 60-percent tin, 40-percent lead condition.

The plating times of 60, 120, and 180 seconds were selected with circuit board shop practice in mind, and were expected to produce a lead thickness range sufficiently broad to provide a functional process with reasonable control limits.

After completion of the test sample plating, the 12 lead barrier boards and 4 control boards plated with

tin-lead only were sheared in two, with half going to the board supplier, and half to Rockwell for evaluation.

TEST AND DATA DISCUSSION

The results and conclusions of this evaluation are drawn from five sources: a) cross-section measurements on nonreflowed samples, b) cross-section measurements on reflowed samples, c) SEM and XRF surface plating thickness and composition measurements on nonreflowed samples, d) unaged float test solderability on samples reflowed at 410°F, and e) aged (16 hours at 125°C) float test solderability on samples reflowed at both 390°F and 430°F.

The data from the tests are presented in Figure 8.

Combined reflowed solder coating thickness at the knee of the plated through hole shows:

- a) Low plating time, low current density lead barrier plating yielded solder coating (total) of less than 100 millionths of an inch thick as a group, and had marginal or unacceptable solderability.
- b) Non-lead barrier plating yielded solder coating (total) of less than 100 millionths of an inch thick as a group and had marginal or unacceptable solderability.
- c) Coating thickness (total) at the knee of the hole on the high current density samples with acceptable solderability ranged from 100 to 500 millionths of an inch thick, depending on time.

Solderability is the key response variable in the test, and there are several observations to be made. The first is illustrated by Figure 9 which relates the aged float solderability test results to plating time and current density. Trends in this figure show scattered data with no trend for the 6 ASF current density, regardless of the plating time. At 12 ASF current density, the 120-second time (there were no 180-second times at this current density) samples showed a grouping with good solderability, but unacceptable solderability at 6 ASF. All combinations of 18 ASF with 60, 120, and 180 seconds of time, either aged or unaged, gave 100 percent acceptable solderability.

PART 2 CONCLUSIONS AND OBSERVATIONS

Much of the following is based on cross-section measurements which are subject to processing technique. Overplating of the tin-lead with copper to prevent distorted tin-lead thickness was not done; however, all measurements were made consistently on the "thin" plating side of the hole such that any smearing would be toward the copper where it would be easier to detect. All cross sections were etched to improve measurement accuracy, and the results are an average of three measurements.

1. Unaged samples had generally better solderability than aged samples.
2. High current density (18 ASF) and any time duration, reflow temperature, or aged condition produced acceptable solderability results.
3. Reflow temperature does not seem to have a strong influence on results, but could be an area for further work on a larger test basis.
4. Composition of the tin-lead (after reflow) measured by XRF ranged from a low of 33 percent tin at high current density/time to 64.8 percent tin with no lead barrier plating.
5. Plating parameters for a production operation need further evaluation to define limits and tolerances accurately. A nominal starting point for defining the limits is suggested by the data to be:
 - a) Current density -- 18 ASF $\pm$ 3 ASF (upper limit to be defined).
 - b) Plating -- 2 minutes $\pm$ 0.5 minute.

OVERALL SUMMARY

Solder coating thickness at the knee of the hole after reflow is consistently 100- to 200-millionths thick with the lead barrier process compared to less than 100-millionths thick without the lead barrier.

Solder composition can drop below 50 percent tin depending on plating parameters.

The evaluation demonstrated superior solderability of samples underplated with a controlled process of lead barrier compared to control samples with only a reflowed tin-lead coating when subjected to artificial aging prior to a solderability test.

REFERENCES

1. Carlson, V. L., Evans, J. W., and Besong, J. P., "Lead Barrier Circuit Board Plating Characteristics," Cedar Rapids, Iowa, September 1987, Rockwell International Working Paper WP87-2027.
2. Hagge, J. K., "Technical Support Information for Circuit Board Solderability Specification 489-0012-001B," Cedar Rapids, Iowa, July 1983, Rockwell International Working Paper WP83-2020.
3. DeVore, John A., "To Solder Easily," Circuits Manufacturing, June 1984.
4. Hagge, J. K. and Davis, G. J., "Aging, Solder Thickness and Solder Alloy Effects on Circuit Board Solderability," Printed Circuit World Convention III, May 1984.
5. Strube, G., "A New Process to Improve Solderability 'SLOTOLON'," Schloetter Co., Ltd. Technical Data Sheet.
6. "The New Process for Improved Solderability of Plated Through Hole Circuits," Schloetter International, Autumn '85.

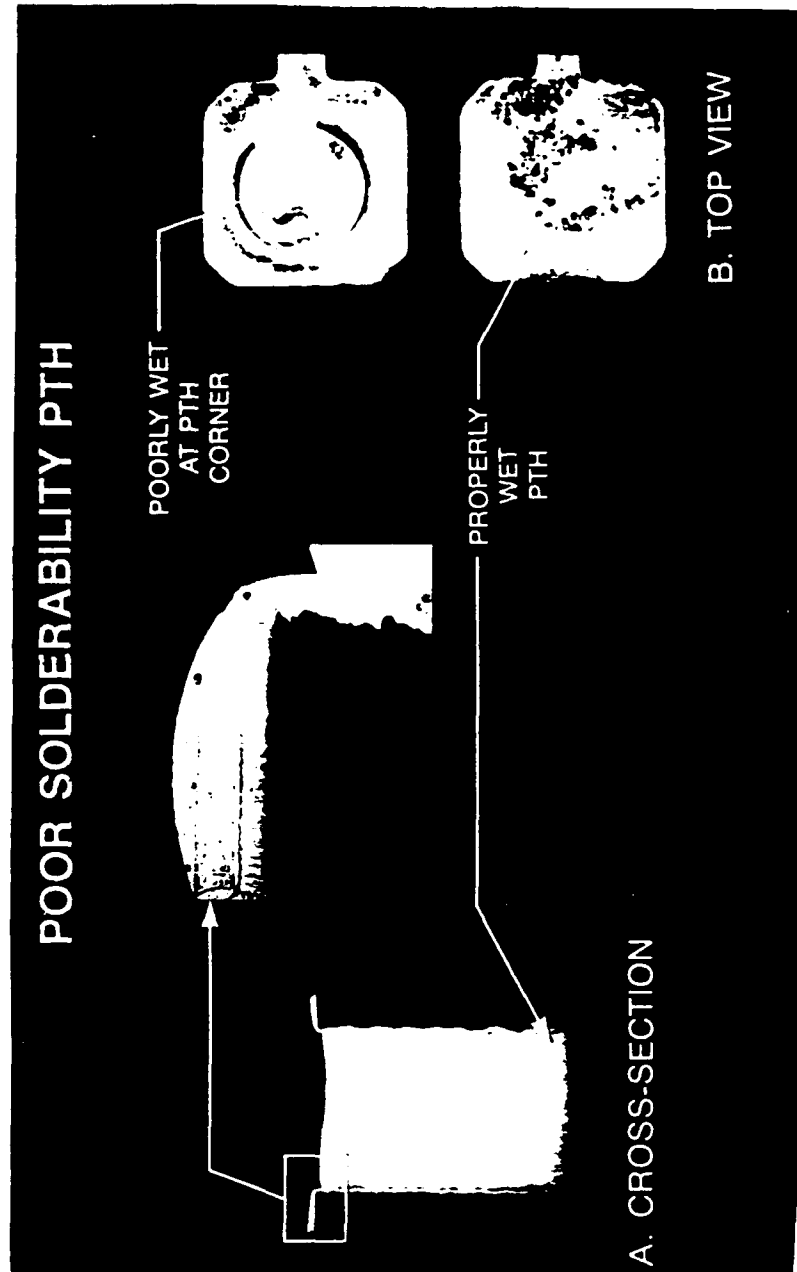


FIGURE 1. Poor Solderability - Weak Knee PTH Example.

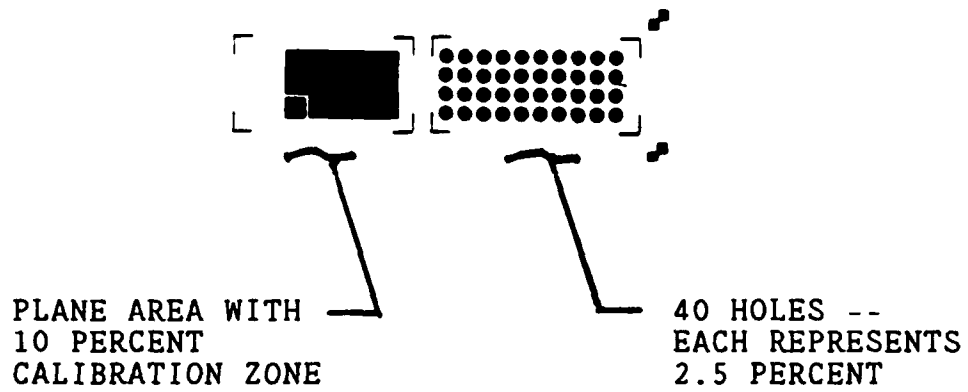


FIGURE 2. Special Solderability Test Coupon.



AS PLATED SECTION
- NO SOLDER TEST
- .0005" KNEE COVERAGE

KNEE COVERAGE ESSENTIALLY
ALL INTERMETALLIC

UNAGED SOLDER DIP SAMPLE
- .0005" KNEE COVERAGE,
ALL INTERMETALLIC



AGED (16 HOURS @ 125°C) SOLDER DIP SAMPLE
- .0003"-.0004" KNEE COVERAGE,
ALL INTERMETALLIC

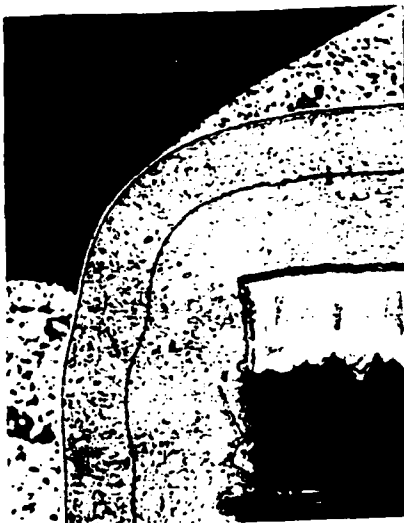


FIGURE 3. Knee Cross Sections.

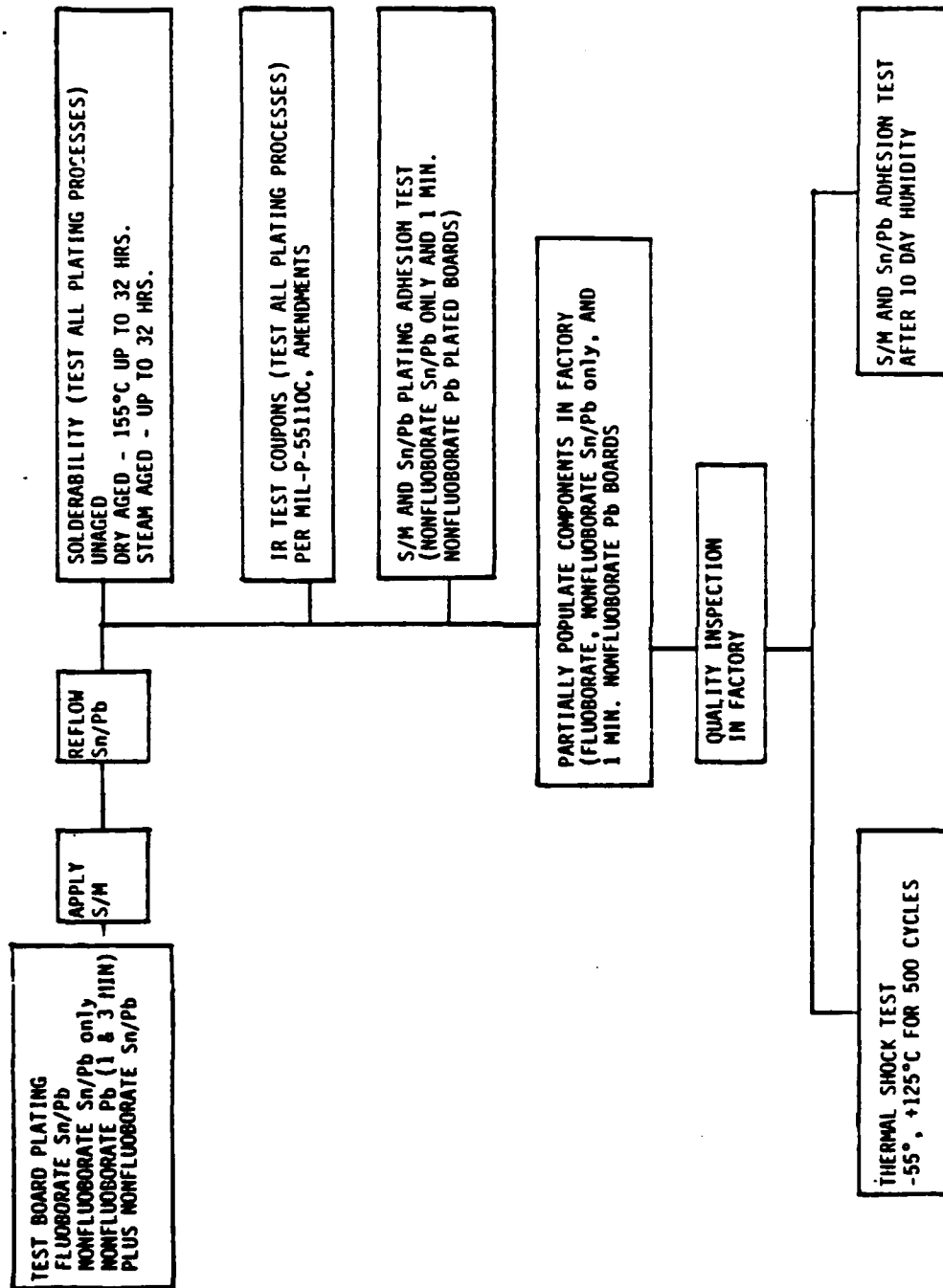


FIGURE 4. Functional Test Flow Diagram.

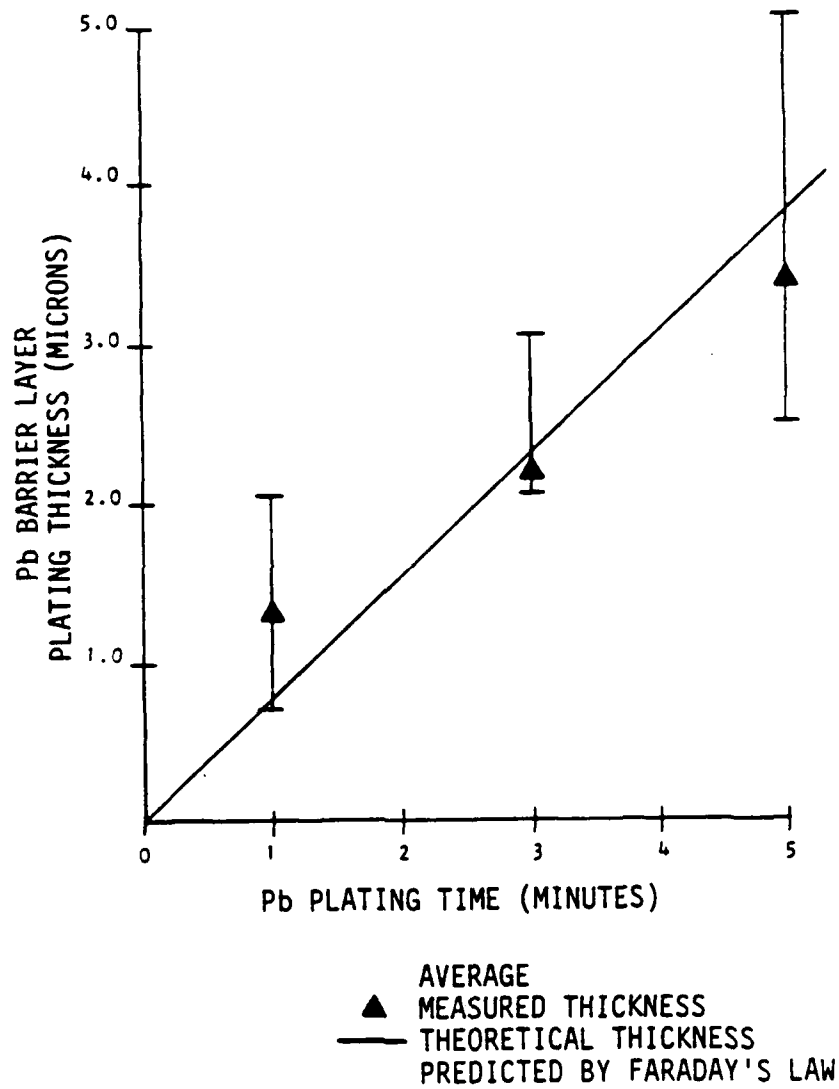


FIGURE 5. Pb Plating Time at 15 amps/ft² vs. Pb Plating Thickness.

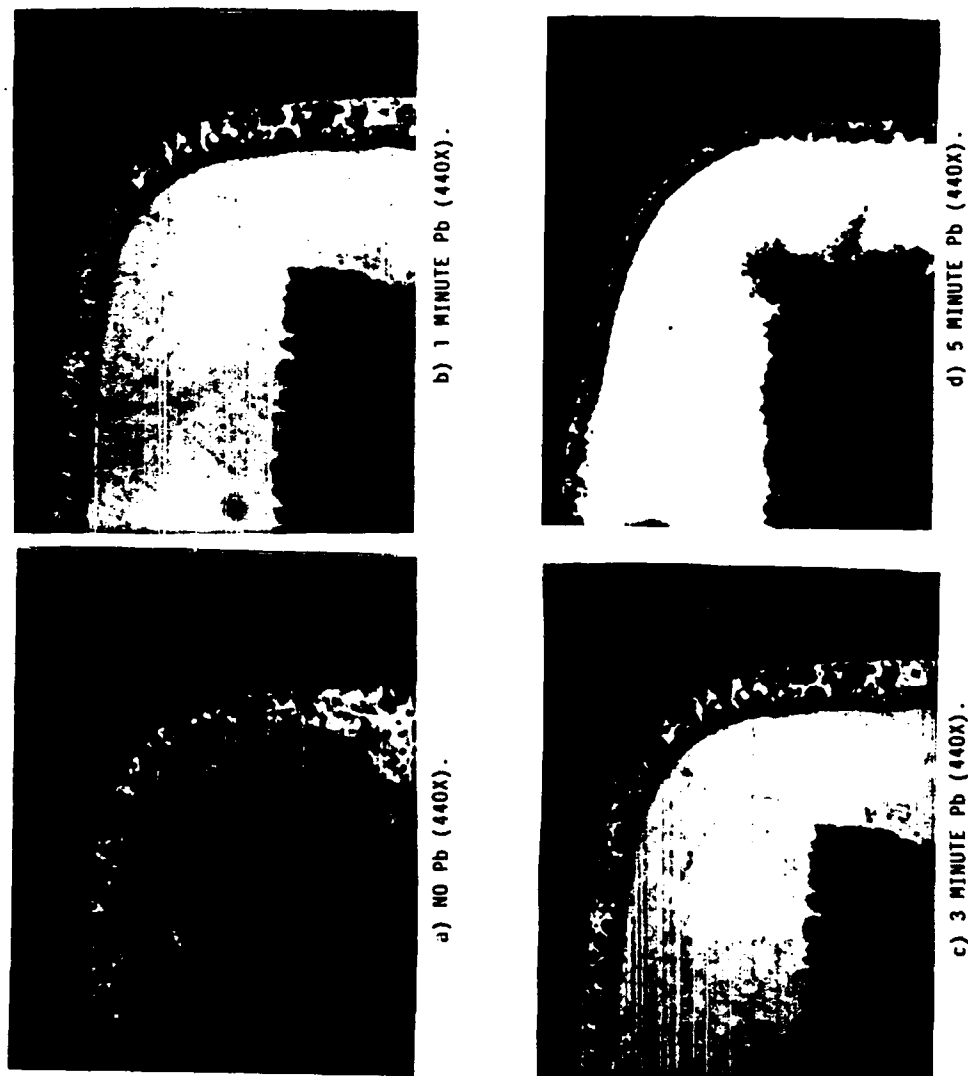


FIGURE 6. Reflowed Nonfluoroborate Cross Sections with Varied Pb Barrier Thickness.

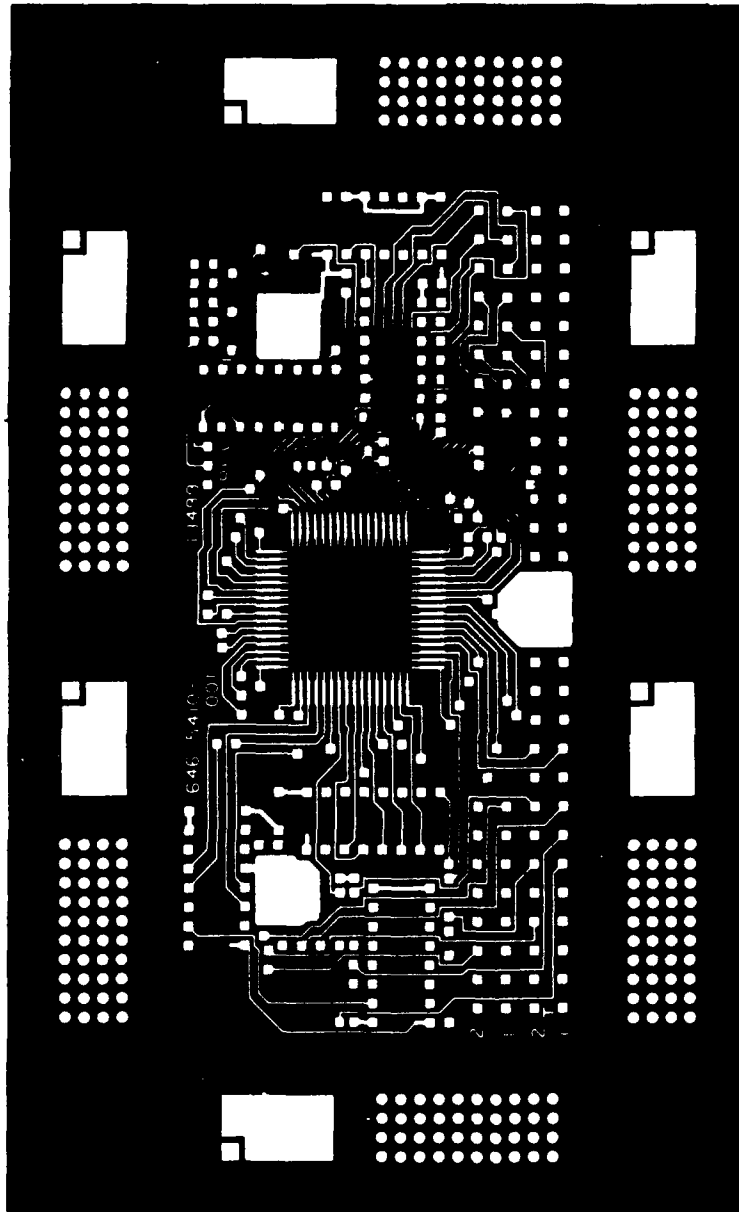


FIGURE 7. Lead Barrier Test Board. Scale ~1:1.

RESULTS OF TESTS PERFORMED ON LEAD BARRIER SAMPLES

SAMPLE NUMBER	AVG. PLATE THICKNESS (INCHES)	AVG. TOTAL PLATE THICKNESS (INCHES)	PLATE CURRENT DENSITY (AMPERES/DM ²)	PLATE TIME (HOURS)	PERCENT LOSS OF PLATE FROM ALL NETWORKS	REPLACEMENT TEMP. (°F)	AVG. TOTAL PLATE THICKNESS (INCHES)	BY TEST AND 1	PERCENT SOLIDITY
1	0.333	0.675	10.00	300 SEC	45.11	370	0.402	AMBER/12X	94.92
1-A					45.11	410	0.378	AMBER/12X	94.92
1-C					54.82	430	0.372	AMBER/12X	94.92
2	0.490	0.982	6.00	300 SEC	45.42	370	0.110	AMBER/12X	3.32
2-A					45.42	410	0.080	AMBER/12X	44.75
2-C					54.82	430	0.067	AMBER/12X	10.88
3	0.152	0.458	12.00	120 SEC	44.11	370	0.241	AMBER/12X	98.92
3-A					44.11	410	0.275	AMBER/12X	98.92
3-C					52.71	430	0.117	AMBER/12X	100.00
4	0.126	0.438	12.00	60 SEC	51.02	370	0.101	AMBER/12X	1.28
4-A					51.02	410	0.051	AMBER/12X	24.40
4-C					63.01	430	0.148	AMBER/12X	20.01
5	0.269	0.539	10.00	300 SEC	33.01	370	0.320	AMBER/12X	100.00
5-A					33.01	410	0.270	AMBER/12X	100.00
5-C					45.11	430	0.408	AMBER/12X	94.92
6	0.123	0.369	6.00	60 SEC	44.42	370	0.067	AMBER/12X	64.92
6-A					44.42	410	0.063	AMBER/12X	100.00
6-C					50.71	430	0.060	AMBER/12X	12.01
7	0.253	0.506	10.00	300 SEC	41.02	370	0.300	AMBER/12X	98.92
7-A					41.02	410	0.372	AMBER/12X	100.00
7-C					54.82	430	0.307	AMBER/12X	100.00
8	0.126	0.378	10.00	60 SEC	32.01	370	0.241	AMBER/12X	98.92
8-A					32.01	410	0.222	AMBER/12X	100.00
8-C					38.11	430	0.104	AMBER/12X	100.00
9	0.113	0.403	6.00	300 SEC	45.01	370	0.400	AMBER/12X	0.01
9-A					45.01	410	0.041	AMBER/12X	70.12
9-C					54.82	430	0.041	AMBER/12X	0.01
10	0.144	0.432	12.00	120 SEC	45.71	370	0.240	AMBER/12X	94.92
10-A					45.71	410	0.227	AMBER/12X	70.12
10-C					54.82	430	0.172	AMBER/12X	100.00
11	0.126	0.378	10.00	60 SEC	45.11	370	0.340	AMBER/12X	98.92
11-A					45.11	410	0.222	AMBER/12X	100.00
11-C					50.11	430	0.120	AMBER/12X	100.00
12	0.070	0.210	6.00	60 SEC	34.01	370	0.004	AMBER/12X	4.01
12-A					34.01	410	0.004	AMBER/12X	100.00
12-C					42.01	430	0.004	AMBER/12X	3.01
13	0.00	0.00	L.S.L.	SEC	45.71	370	0.00	AMBER/12X	74.41
13-A					45.71	410	0.00	AMBER/12X	100.00
13-C					71.41	430	0.00	AMBER/12X	100.00
14	0.00	0.00	L.S.L.	SEC	45.01	370	0.120	AMBER/12X	92.01
14-A					45.01	410	0.00	AMBER/12X	100.00
14-C					70.01	430	0.00	AMBER/12X	21.01
15	0.00	0.00	L.S.L.	SEC	44.11	370	0.00	AMBER/12X	94.92
15-A					44.11	410	0.00	AMBER/12X	100.00
15-C					64.11	430	0.00	AMBER/12X	21.01
16	0.00	0.00	L.S.L.	SEC	45.01	370	0.120	AMBER/12X	12.01
16-A					45.01	410	0.00	AMBER/12X	100.00
16-C					65.01	430	0.00	AMBER/12X	0.01
17	0.00	0.114	12.00	90 SEC	44.01	370	0.00	AMBER/12X	0.01
17-A					44.01	410	0.00	AMBER/12X	44.92
17-C					54.01	430	0.00	AMBER/12X	0.01
18	0.00	0.114	12.00	SEC	44.71	370	0.00	AMBER/12X	97.92
18-A					44.71	410	0.00	AMBER/12X	71.91
18-C					54.71	430	0.00	AMBER/12X	0.01

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FIGURE 8. Lead Barrier Plating Test Data Summary.

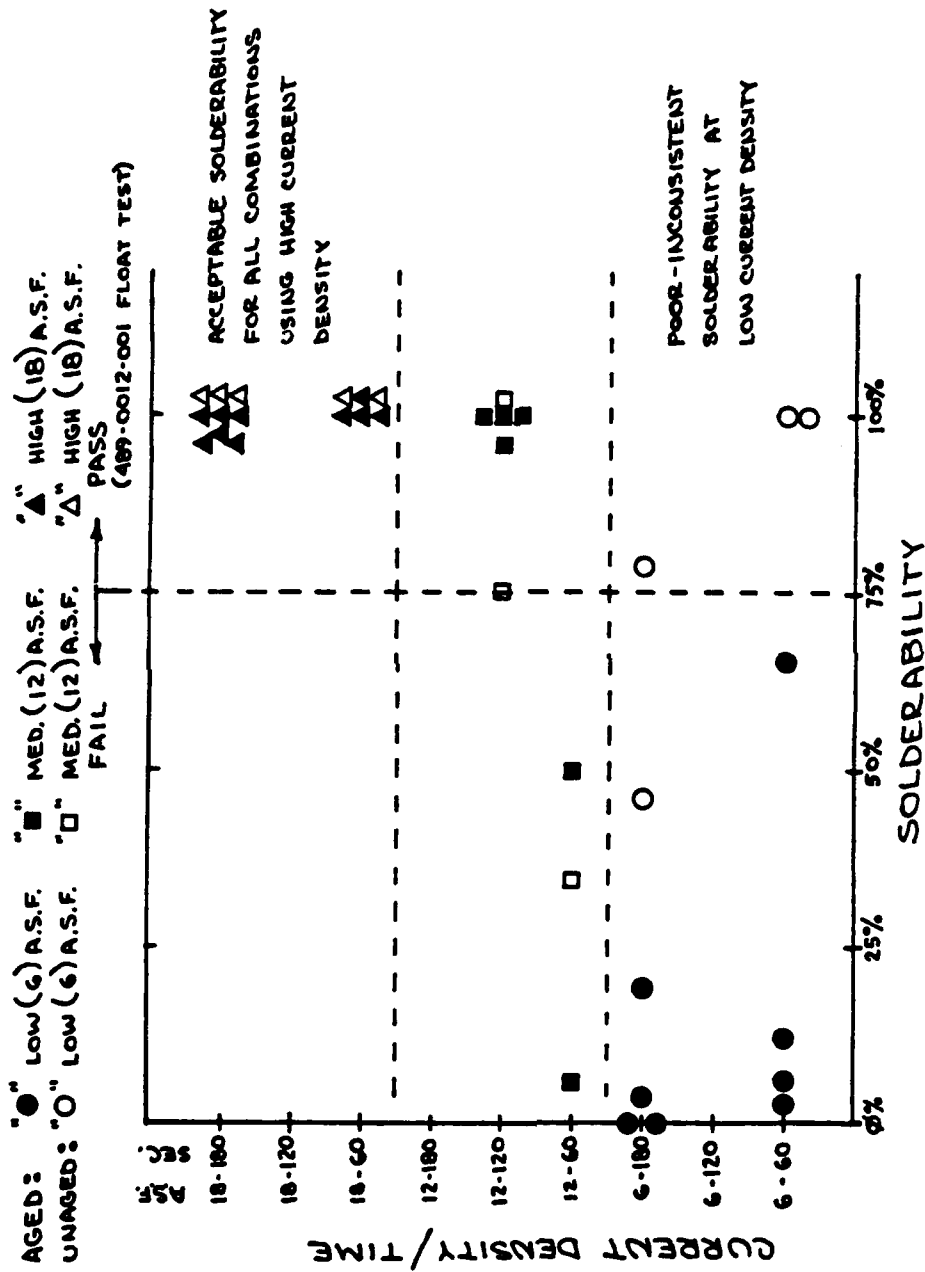


FIGURE 9. Solderability Test Results as a Function of Plating Current Density and Time.

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SUMMARY OF THE ELECTRONIC FIELD HARDWARE REPORT

By

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ABSTRACT:

This paper contains excerpts as well as a summarization of key issues from the DOD-STD-2000 Acceptance Criteria Field Electronic Hardware Examination Report.

The team visited repair depots to try to evaluate what affect anomalies not in compliance with military standards posed to reliability. Also, if reliability problems were occurring from electronics manufacturing practices, recommendations discussing design guidelines and defect criteria would be documented. In addition to recommendations on specific solder joint criteria for standards, the Field Survey Team made a number of general recommendations.

The primary report considered the survey observations; other research reports and interviews; and engineering rationale when drawing conclusions and recommendations for DOD-STD-2000. For ease of understanding, this paper will only discuss the observations. The author recommends review of the primary report for more information and explanation as to the Hardware Examination Team's conclusions.

INTRODUCTION

This study was an outgrowth of a meeting held on 31 March 1988 in Crystal City, Virginia, to coordinate industry's participation with government agencies relating to the implementation of the DOD-STD-2000 series of documents. This initiative resulted in the establishment of three joint government and industry committees: Top Technical Issues, Acceptance Criteria, and Statistical Process Control. The Acceptance Criteria

Committee tasked one subcommittee (Field Survey Team) to examine electronic equipment at repair depots. The subcommittee charter included the following tasks:

- a. Determine the condition of solder joints on functional hardware based on types of defects, severity of defects, and field history usage.
- b. Identify any attributes relating to design, assembly, and handling that may degrade equipment reliability.
- c. Draft recommendations based on the committee's findings and submit them to the DOD-STD-2000 Working Committee for consideration as input to the specifications.

This paper will only discuss the observations made during the review. Although the observations, technical information, interviews, and engineering rationale were used in the primary report to make recommendations to the Working Committee, these will not be discussed here. It is recommended to the reader that they refer to the initial report for this information.

TASK/PROCEDURES:

The team examined a variety of Air Force, Army, and Navy military systems over a six-month period. The team's goal was to document the general appearance of each printed circuit assembly (PCA) examined, document attributes, and assess the reliability impact of anomalies in accordance with present military solder specifications.

Hardware was requested from the depots with the following preferences:

- a) Field experience and history
- b) Currently functional PCAs
- c) Failure documentation or information
- d) Reliability documentation or information
- e) Manufacturing history information

All solder joints on the boards were examined with respect to WS6536E and DOD-STD-2000 (NOTE: much of the hardware was built to other soldering standards). Examinations were normally conducted using stereo binocular microscopes set at 4x to 30x magnification. Hardware examiners did not document all of the defects found on the hardware. Anomalies which were considered more critical to product reliability were thoroughly documented. Non-critical anomalies were not documented as thoroughly. In some cases, only 10-40% of the anomalies were documented; for example, grainy solder. This discretionary practice was necessary to cover all of the hardware available for review.

Two factors kept the team from performing extensive progressive destructive analysis and/or functional electrical test; primarily, hardware ownership and secondarily, availability of resources. In a few instances, further evaluation was conducted. This included:

- a) Electrical testing on boards with cracked solder joints.
- b) Auger and microsection analysis of a solder-circuitry adhesion problem.
- c) EDS of a corroded transistor case.
- d) Microsectioning of cracked solder joints.
- e) Tweezer pull test on surface mounted flat packs.

RELIABILITY ASSESSMENT APPROACH

Since extensive failure analysis of solder joint anomalies was not practicable, it is important to understand the examination team's method of assessing potential reliability problems. NOTE: For ease of explanation, the team defined a solder joint fracture as a total metallurgical separation of the connection. A crack was defined as a partial separation with some of the connection intact.

Fractured and/or cracked solder joints were used as the basis of determining if a solder joint anomaly could have an affect on solder joint reliability. Basically, if an anomaly frequently possessed solder joint cracks, the anomaly was considered a potential reliability

problem. For example, nonwetting on untinned gold finished connectors posed a potential reliability hazard as they frequently were associated with cracks. This does not necessarily mean that the cracks caused an electrical failure, nor will they in the future.

Since the primary mechanism of solder joints causing electrical failures is a fractured connection, only a fractured solder joint was used as the examination team's primary means of identifying a potential electrical failure due to a solder joint. When a crack occurred, both sides of the PCA were examined for a total metallurgical fracture of the solder joint. If this was not the case, the cracked solder joint was discarded as being a current electrical integrity problem. (cracked solder joints may cause electrical failures under unique conditions; for example, current density changes; corona effects from sharp edges; and, insertion losses due to discontinuities in the surface of the conductor at microwave frequencies (skin effect)).

SUMMARY OF HARDWARE CHARACTERISTICS:

A wide variety of hardware configurations as well as hardware vintages and missions were examined in this study. A total of 290 boards were examined at 13 depots (6 military and 7 contractors). A total of 7778 defects were "documented". The documented defects represented 10 to 40 percent of the total defect count on a PCA. Eighty percent of the circuit cards examined were functional; had a history of field usage; and, were expected to be returned to the field. Hardware at one facility had not been placed into field operation but had passed qualification testing.

The boards were manufactured using hand soldering, wave soldering, hot bar reflow, vapor phase soldering, and infrared soldering processes. Some of the specifications used to assemble the hardware included: MIL-STD-454, WS-6536, MIL-S-45743, MIL-S-46844, and NHB-5300.43A-1.

For information summarizing characteristics of the hardware examined, see Table 1.

APPLICATION. Hardware classified under avionics included navigation; communication; flight control; landing gear sensors, radar, signal conditioner, antisubmarine warfare; and altimeter modules. Ground support electronics deployed on tanks and personnel carriers included computers; test equipment; security; communications; and armor gunfire control. Missile hardware included strategic; tactical; and conventional weapons that were air; ground; ship; or submarine launched. The team also examined a satellite which was returned to earth by the space shuttle. This satellite served as a remote interface unit for a multimission spacecraft.

AGE. The hardware examined was manufactured in a period from 1958 to 1989. Nearly 60 percent of the hardware examined was manufactured within the last 10 years, while another 40 percent was older than 10 years. History documentation for the hardware was very difficult to obtain. The age of most hardware was estimated by using component/PCA lot date codes, unit warranty/ID tags, and elapsed time meters (ETM).

TECHNOLOGY, SUBSTRATE, AND NUMBER OF LAYERS. Most of the hardware examined was of plated thru-hole technology. Some surface mount hardware as well as mixed technology was available for examination. Also, epoxy-based laminates were, by far, the most prevalent laminate configuration used by manufacturers. Most hardware was multi-layered, ranging from 2 to 14 layers. Thirty-five percent of the hardware was double sided.

OBSERVATIONS:

These observations are general and do not apply to all depots and personnel.

a) Some boards returned from the field to repair depots were poorly packaged for handling and ESD considerations.

TABLE 1

SUMMARY OF HARDWARE EXAMINED

<u>APPLICATIONS:</u>	AVIONICS:	53 %
	MISSILE:	22
	GROUND SUPPORT:	23
	SPACE:	1
	UNKNOWN:	1
<u>AGE OF HARDWARE:</u>	1960-1969	6 %
	1970-1974	8
	1975-1979	20
	1980-1984	21
	1985-PRESENT	35
	UNKNOWN	10
<u>TECHNOLOGIES:</u>	PTH	75 %
	MIXED	17
	SMT LEADED	6
	TERMINAL CHASSIS	2
<u>SUBSTRATES:</u>	EPOXY	80 %
	POLYIMIDE	9
	METAL CHASSIS	7
	PHENOLIC	3
	CERAMIC	1
<u>LAYERS:</u>	1	2 %
	2	36
	3	4
	4	3
	6-8	20
	10	2
	12	0.5
	14	0.5
	MULTI(No. unknown)	32

b) At the depot level, historical data on military hardware was extremely difficult to obtain if available at all. Also, documentation that identified the source of electrical failures was difficult or impossible to acquire. Symptoms of the failure were identified on the repair orders at the depot level. However, not all depots kept records of corrective actions. If records were filed, they were difficult to access and required a great amount of effort.

c) When repair technicians pursued obvious failure trends, the failures appeared to be related to specific assemblies made by specific contractors and suppliers.

d) One case of older hardware appeared to have produced more failures, yet this hardware was not removed from the inventory and demanded more repair than recently manufactured hardware.

e) Repair personnel encountered obvious design related problems that were not corrected.

f) Generally, field repair practices were of poor quality compared to the originally delivered product. A significant amount of the solder anomalies found by the review team was the result of repair. Inadequate training and lack of proper equipment (soldering iron too large, wrong temperature, and inadequate ESD protection) appear to be the main contributors. Poor repair practices frequently caused the following problems:

- 1) Measling and crazing
- 2) Overheated connections
- 3) Scrapped circuitry and leads
- 4) Lifted leads and traces
- 5) Severe probe marks; sometimes greater than 50 percent of the solder connection - capable of holding the probe completely upright by itself
- 6) Cold solder connections
- 7) Butt splice soldering of two leads together with minimal solder
- 8) Rosin connections

g) It appeared that repair technicians lack the background or training to determine if a solder joint caused a failure. ESD training was also poor and awareness varied significantly at each depot. Generally, due to the variety of hardware, no standard repair procedures nor standard training certification were evident.

h) Based on the broad variety and the age of hardware examined, solder appearance has improved as a result of material science and technology advancements in the last twenty years. However, the solder appearance could not be directly related to improved reliability.

i) Depot repair technicians interviewed by the team stated that 95 to 98 percent of all field failures were attributable to components.

j) Most hardware examined had numerous examples of solder anomalies as defined by specifications currently used to build and inspect hardware. An average of 27 defects per board was documented. Surface mount boards appeared to have less anomalies than through-hole boards.

k) Many of the observed anomalies would not be considered defects based on the specifications to which they were originally built (eg. MIL-STD-454). With the exception of a few examples, (e.g. non-soldered connection), the anomalies observed on this study were cosmetic and did not render boards mechanically or electrically unreliable.

l) Plastic deformation and stress cracks were observed on some solder joints. These attributes were determined to be the result of design, process related factors, and/or normal aging from field usage.

m) Several non-printed circuit assembly failures were confirmed during this review. One involved a single component soldered to a wire in an aircraft application. The resulting problem was due to a poor application of design and materials. A resistor was soldered with Sn63 in a high temperature jet engine environment. The high thermal environment reflowed the solder.

Another situation involved a wire harness failure, where insulation had aged and cracked, exposing bare wire. This caused an electrical short. It should be noted that the failure was caused by an aging condition; the wire insulation was in excess of 15 years old and was also a poor choice of material.

n) There were four printed circuit board related failures that were observed during the survey. One problem encountered was random peeling of solder from the copper circuitry. The solder foil could be easily removed by tweezers, leaving a copper surface present with no sign of solder on the surface. Adjacent to the solder trace were flatpack leads, surface-mounted to the circuit. Once the peeling was initiated at any site near the flat pack leads, the peeling would progress to cause a lifted pad on a flatpack. This failure would, in turn, cause an electrical failure. A sample of the solder foil removed from this circuit board was analyzed by both Auger and SEM/EDAX methodologies. The sample was evaluated on the side that was in immediate contact with the copper foil. The analysis revealed that a copper/tin intermetallic compound of Cu_3Sn was present at the interface. This problem occurred specifically on one supplier's hardware and is considered to be a process problem.

Additionally, connectors (two cases) were reported to have caused intermittent system failures. Recessed pins, deformed contacts, and oxidation were root causes of the failure. Generally, the failures were corrected by reseating the connectors. In some cases, 50 percent of the failures were corrected by simply reseating the boards in the connectors.

The final case observed involved crystal oven pins made of a ferrous alloy that were not properly coated nor hot solder dipped, directly resulting in electrical opens. The solution to this problem was to manually resolder joints on the boards that experienced this failure mode. The circuits did become electrically functional, but the cause of the initial problem was not resolved.

o) The team observed some severe solder anomalies that may have caused previous functional failures. However, these did not surface (cause a failure) during the time of investigation; for example, non-soldered connections.

p) Electrical testing of boards with cracked solder joints demonstrated that the boards were still operating properly. A few boards were twisted and thermally shocked in an attempt to induce failures; however, boards continued to operate.

q) Conformal coating visually appeared to have withstood aging and environmental effects very well.

r) No metallurgical solder joint fractures were observed. However, in the case of one disturbed solder joint, a minute force on the component lead with the examination tweezers caused a separation from the solder. This specific incident included insufficient solder and a severely lifted lead on the gull wing mounted package.

OBSERVATIONS BASED ON SPECIFIC DEFECTS:

A Pareto analysis was established for the quantity of specific defects documented in this study. Table 2 displays the Pareto analysis for the top defects.

TABLE 2

**PARTIAL PARETO DISTRIBUTION OF MOST FREQUENTLY
DOCUMENTED DEFECT QUANTITIES**

DEFECT CODE	DEFECT DESCRIPTION	NUMBER
A108	POOR WETTING	1970
A155	LEADS CUT AFTER FINAL SOLDERING	1772
A121	ALL OTHER SOLDER DEFECTS EXCEPT THOSE LISTED AS LEVEL B PROCESS INDICATORS	990
A107	EXCESSIVE SOLDER, LEAD NOT DISCERNIBLE	320
B217	PITS, PINHOLES, HOLES, OR VOIDS (BOTTOM OF VOID VISIBLE AND FREE OF RESIDUES)	296
A147	COMPONENT HAS IMPROPER CLEARANCE ABOVE THE PWB	261
A106	INSUFFICIENT SOLDER	244
A112	DEWETTING OF SOLDER CONNECTION AREAS	240
B219	SOLDER NOT SMOOTH AND SHINY	232
A105	FRACTURED OR DISTURBED	183
A160	ALL OTHER ASSEMBLY DEFECTS EXCEPT THOSE LISTED AS LEVEL B PROCESS INDICATORS	118
B221	MEASLING OR CRAZING	114

TABLE 2 (Continued)

PARTIAL PARETO DISTRIBUTION OF MOST FREQUENTLY
DOCUMENTED DEFECT QUANTITIES

DEFECT CODE	DEFECT DESCRIPTION	NUMBER
A120	EXCESS SOLDER IN THE BEND RADIUS	108
A115	FLUX RESIDUE, OILS, GREASES ON ASSEMBLY	107
A130	IMPROPER TRANSMISSION OF STRESS OF LEADS AND WIRES (IMPROPER STRESS RELIEF)	106
A117	OVERHEATED SOLDER	77
A110	PITS, PINHOLES, HOLES, OR VOIDS (BOTTOM CANNOT BE SEEN)	70
A109	SOLDER SPLATTERING	69
A137	LEAD CLINCHED BEYOND ALLOWABLE LIMITS (ELECTRICAL CLEARANCE INSUFFICIENT)	51
A139	INSUFFICIENT LEAD LENGTH	48
A136	LEADS OR WIRES SCRAPPED, EXPOSING METAL OR STRETCHED	38
A198	ALL OTHER PRINTED WIRING AND PRINTED WIRING BOARDS DEFECTS EXCEPT THOSE LISTED AS LEVEL B PROCESS INDICATORS	37
A114	SOLDER POINTS, PEAKS, OR ICICLES	31
A138	EXCESSIVE LEAD LENGTH (ELECTRICAL CLEARANCE INSUFFICIENT)	30
B215	COMPONENT NOT CENTERED	23
A180	PATTERN LAMINATED (AFTER SOLDERING)	21

Figure 1 shows that the 15 defect codes occurring most frequently represented nearly 90 percent of the total defects that were documented in this effort. Figure 2 shows how many times a specific defect code was documented on individual PCAs. For example, poor wetting (A108) occurred on 114 PCAs out of total 290 (39%). The accumulative percentage of the total defect count associated with the specific defect codes is also graphed. Looking at the accumulative distribution of the defects, 75 percent of the defects occur with the 15 most frequently called defect codes per individual PCA (if a specific defect code is called out more than once on a PCA, it is only counted once).

TOP 15 DEFECT QUANTITY BY DEFECT CODES

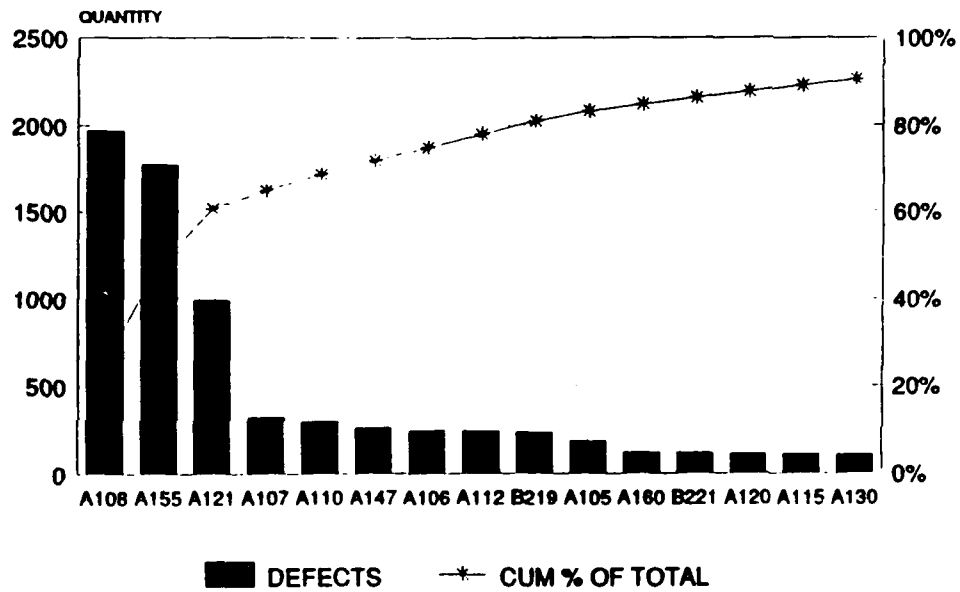


FIGURE 1

TOP 15 DEFECT CODES DETECTED ON PCB'S

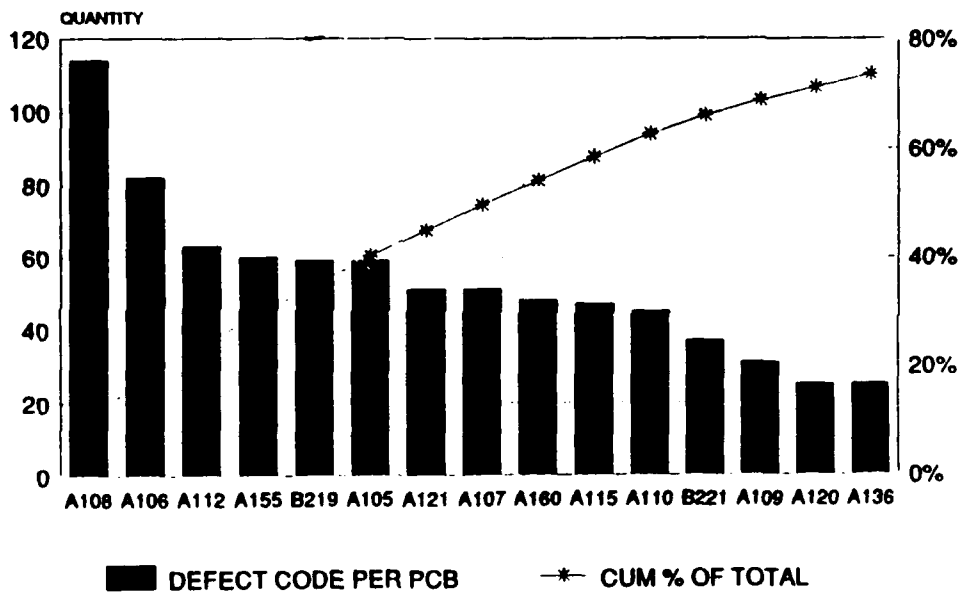


FIGURE 2

Figure 3 shows how the top 15 drivers for both the quantity of specific defects and specific defect code occurrence on PCBs correlate. This figure endorses the hypothesis that the defects documented generally occur on most hardware regardless of the PCA manufacturer and hardware configuration.

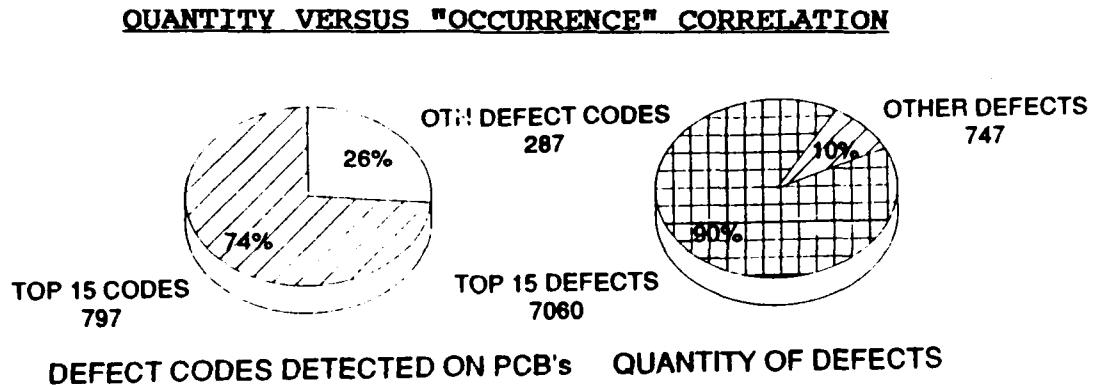


FIGURE 3

a) **Poor Wetting.** Thirty percent (605 joints) of poor wetting occurrences were due to weak knees. Weak knees are defined as the exposed corner of the plated-through-hole barrel. The remaining 70 percent of defects in this category were apportioned over component leads or the PCB pad in general. Wetting varied from minimal poor wetting to severe non-wetting on connector pins and pads. Solder joint cracking frequently occurred on gold connectors with non-wetted connection.

Observations did not reveal any failures related to weak knees. Gross nonwetting (re-defined as a 90° wetting angle) should be considered a reliability issue.

b) **Leads Cut After Final Soldering.** In terms of exposed copper on lead ends, the final cut after soldering did not produce any failures or indication of any corrosion. In some situations, leads had separated (crack) from the solder due to the trimming of the lead.

Solder joint cracks resulting from lead trim after solder would fall under the A105 Fractured or Disturbed Solder classification. Components with cracked solder joints from lead trimming should be examined for damage and not simply touched up.

c) **Gold Finish on Component Leads.** Gold finishes appear to be more critical for surface mounted devices than for feed-through technology. Gold on SMDs frequently contributed to a very grainy, dull finish to the solder. Non-tinned gold leads on plated-through hole connections generally did not produce evidence of cracking in the solder joints, except gold plated connector pins that exhibited wetting problems. When able to be further tested, these cracks did not affect the operation of the board.

Observations did not reveal any failures related to gold finish on through-hole components. It is recommended that nonwetted, gold-finished connectors be reworked and, preferably, pretinned. Tinning of gold finished SMD's should be mandatory, regardless of the gold plate thickness, until further study proves otherwise.

d) **Excessive Solder, Lead Not Discernible.** Observations did not reveal any failures related to excess solder.

e) **Pits, Pinholes, Holes, or Voids (Bottom of Void Visible and Free of Residues).** Observations did not reveal any failures related to pinholes, pits, and holes. One observed blowhole cavity was easily 50% of the solder connection. Rework practices caused frequent probe marks in solder connections; many probe marks were as deep as 50% of the board thickness.

f) **Component has Improper Clearance above the PWB.** The anomalies documented in this category were predominantly flush mounted radial leaded capacitors (CKROX). Solder joint reliability on flush mounted CKROX type capacitors did not appear to be a reliability concern as long as there is a bottom fillet.

Several large capacitors were not properly secured and were mounted too high above the board. The parts subsequently developed cracked solder joints. These parts were designed to be supported by a rubber pad. Somehow, this pad was dislodged.

Some kidney bean tombstone capacitors were flush mounted such that their coating (Durez; TM) was embedded in solder joints. Most of these defects occurred on very few boards. Observations did not reveal any failures related to this situation.

g) Insufficient Solder. In most cases, insufficient solder anomalies exceeded 75% plated through hole fill. Fifteen percent of the cases of insufficient solder were attributed to weak knees. Observations did not reveal any failures related to insufficient solder. It appears that 75% solder fill of the PTH is sufficient for reliability.

h) Dewetting of Solder Connection Areas. Generally, only minor dewetting conditions were observed during this review, and did not appear to cause any reliability problems. Eleven percent of the dewetts were due to weak knees. Component lead dewetting was commonly 25 percent of the lead periphery and sometimes as high as 75 percent. Worst case dewetting on solder connection areas was 80 percent dewett of the top side pad area. This condition occurred with a 99 percent solder fill of the barrel and complete bottom side fillet. Observations did not reveal any failures related to dewetting. Allowable peripheral dewetting on the bottom side should be 25 percent of the component lead or pad.

i) Solder not Smooth and Shiny. Grainy solder was one of the most frequently observed conditions of solder joints. When graininess was observed, it was generally present throughout the board and the exact number of occurrences was not documented. Observations did not reveal any failures related to grainy solder.

j) Fractured or Disturbed. The 179 total anomalies documented for this defect code can be broken down into 161 cracked solder joints and 18 disturbed solder joints. There were no solder joint fractures.

Table 3 is a summary of the data base on fractured, cracked, and/or disturbed solder joints. Table 4 displays how the cracked solder connections were distributed on the hardware reviewed.

TABLE 3

	Number
-----	-----
Side brazed CERDIPS	73
Gold (nonwett-connectors)	MANY
Nonwett	6
Poor wetting	6
Dewett	4
Component pushed over	4
Excessive solder	4
Insufficient solder	3
Birdcaged Wire	3
Grainy, frosty	2
Excess standoff height	2
Lifted Pad	1
Damaged wire insulation	1
Solder stacking	1
Conformal coating on leads	1

In one case, a gull wing surface mounted component exhibited a disturbed solder connection in which a lead was easily separated from the solder when a small force was applied to the lead.

Solder joint cracking generally did not correlate with soldering anomalies, except for severe nonwetting on gold connectors, side-brazed CERDIPS, unsupported component, and improper handling practices. Many cracked solder joints occurred on otherwise good solder joints with no other defect anomalies.

k) **Measling or Crazing.** Most crazing observed occurred due to the repair process; often occurring on every solder joint of the replaced component. The worst case of crazing covered an entire 60-pin connector. Another documented case of crazing stretched over 11 pins on a 60-pin connector on one side and over 13-pins on the other side. Many times conductors were connected by crazing; especially PTH barrels during the rework process. Observations did not reveal any failures related to crazing.

TABLE 4

FRACTURED OR DISTURBED SOLDER CONNECTIONS

TOTAL: 179

APPLICATION:

AVIONICS:	45
MISSILE:	101
GROUND SUPPORT:	18
SPACE:	2
UNKNOWN:	17

AGE:

1960-1969:	6
1970-1974:	27
1975-1979:	22
1980-1984:	88
1985-Present:	32
UNKNOWN:	8

TECHNOLOGY:

PTH:	164
SMTL:	3
MIXED:	16

COMPONENTS:

CAPACITORS:	22
RESISTORS:	13
TRANSISTORS:	1
IC's:	86
DIODES:	3
CONNECTORS:	14
TERMINALS:	1
FLATPACKS:	3
OTHER:	32
UNKNOWN:	7

LAMINATE:

POLYIMIDE:	6
EPOXY:	166
PHENOLIC:	4
UNKNOWN:	6

LAYERS:

1:	4
2:	43
3:	6
4:	6
6-8:	16
MULTI:	108

l) **Excess Solder in the Bend Radius.** Solder in the bend radius occurred frequently, many times beyond the current allowable specification requirements, and did not appear to affect reliability. On some resistors, solder actually touched the component body. Solder in the bend radius occurred on 42 resistors, 38 flat packs, and 17 diodes. Observations did not reveal any failures related to solder in the bend radius.

m) **Flux Residue, Oils, Greases on Assembly.** Flux occurred frequently on the hardware. Most cases exhibited a localized flux residue or small amounts of burnt flux. A few PCAs appeared as though they had never been cleaned prior to conformal coating. In this case, flux was throughout the entire assembly. One PCA, which exhibited a great deal of flux residues, had a history of frequent intermittent type failures. Flux residues occurred frequently from the repair process. The small amounts of discolored flux observed during this examination did not appear to affect reliability.

n) **Improper Transmission of Stress of Leads and Wires (Improper Stress Relief).** A number of gull winged and axial lead components with improper lead dress were noted, some of which were quite severe. Most of this defect occurred on resistors. Observations did not reveal any failures related to improper transmission of stress.

o) **Solder Splattering.** The range of solder splatter observed during the examination varied from tightly adhering webbing/splatter to loosely adhering solder balls. Some of the solder splatter was embedded in the board and could not be removed.

CONCLUSIONS:

Many nonconformities existed on much of the military hardware. In this study, the prevalent belief that solder joints are a frequent cause of field failures could not be substantiated on pth technology. From interviews with repair personnel, it was learned that solder joint failures were believed to represent only 2 to 5 percent of problems encountered at the depot level. Also, the repair technicians believe that 95 to 98% of the failures were related to component failures. Design

and/or manufacturing practices that were associated with solder joint cracks were: side-brazed CERDIPS, gross non-wetts on gold finished connectors, leads bent over from handling, and unsupported components (due to lost spacer).

The team did observe severe cases that would have been expected to cause functional failures but had not at the time of investigation; for example, non-soldered connections. In these instances, it would have been reasonable to believe that an electrical failure could have resulted from the anomaly at an earlier time. If they did cause such a failure, the anomaly was not discovered nor corrected by either field or depot repair technicians.

The few electronic failures encountered were attributed to the design, manufacturing, and/or rework of printed circuit assemblies (PCA's). The failures encountered include: reflow of a solder joint in a high-temperature jet-turbine environment, electrical shorting from exposed bare wire due to cracked wire insulation, intermittents caused by corroded connectors, electrical opens due to improper coating on ferrous/nickel-ferrous leads, and a solder-circuitry adhesion problem.

Although field repair technicians were very knowledgeable in electrical trouble shooting, training and proper PCA repair procedures were lacking; especially electrostatic discharge (ESD) procedures.

At repair depots, it appears that there is no effective data base used to track and reduce assembly failures. This perpetuates the same mistakes in both design and assembly processing by not providing feedback to the Original Equipment Manufacturer (OEM). At one depot, interviewed personnel revealed that the older hardware tended to exhibit a higher component failure rate. Nevertheless, this hardware was not removed from the inventory and repeated repair cycles occurred.

RECOMMENDATIONS

Recommendations about specific defect codes are made in the primary report. The following are the general recommendations:

a) The emphasis in hardware reliability and quality assurance should be based on design and process control. End-item inspection criteria should be categorized between reliability concerns and process indicators. It is recommended that a Design Handbook be created which discusses general, good design practices. Please refer to the primary report for recommendations and modifications on specific defects.

b) To properly analyze solder joint related failures at repair depots, an analysis group trained in solder related issues is required. This group would be responsible for maintaining a depot level failure database which would incorporate all of the features of a closed-loop Failure Reporting and Correction Action System (FRACAS). Since this may not be financially and logistically feasible at each depot, it is recommended that further effort be made to address this issue.

c) The data base from this hardware examination is sufficient for PTH technology. It is recommended that another hardware examination team be created to look at only surface mount technology.

d) Generally, field repair practices appeared to be of poor quality. A training program should be implemented to train field and depot personnel in the proper methods for performing solder and printed wiring repairs. The examination team did not pursue this area in great detail. It is recommended that a future effort be established for determining the reasons of poor workmanship practices and the means to correct this problem.

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