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TNO-report

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Design of an X-band PIN Diode Phase Shifter by Computer Optimization

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ABSTRACT

This report describes the design and experimental results of a four bit microstrip diode phase shifter in the frequency band of 9.0 to 10.0 GHz The phase shifter has been built on an alumina substrate and the desired differential phase shift is reached by switching transmission lines by PIN diodes.
The lay-out of the circuits was designed for minimum physical dimensions.
Three circuits have been realized with good results.
The circuit containing the 22.5 and 45 degree bits, gives an insertion loss of 0.75 dB and a maximum phase deviation of less than 3.5 degrees.
The circuit containing the 90 and 180 degree bits, gives an insertion loss of 1.3 dB. The average phase shift of the 90 degree bit is not optimal (98 degrees) but the phase deviation in regard to the average phase shift is less than 1.7 degrees. The 180 degree bit gives a phase deviation of less than 4.5 degree.
The four bit phase shifter good results for both insertion loss and differential phase shift, but still has serious problems with the input impedance match.

rapport no. : FEL-89-B286
titel : Ontwerp van een x-band PIN-diode fasedraaier m.b.v. computeroptimalisatie

auteur(s) : Ing. F.J. Klumpers
instituut : Fysisch en Elektronisch Laboratorium TNO

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SAMENVATTING

Dit verslag handelt over het ontwerp en de realisatie van een vier bit microstrip fasedraaier voor de frequentieband van 9 tot 10 GHz.
De fasedraaier is uitgevoerd op een substraat van aluminiumoxide en de fase-bepalende lijnstukken worden geschakeld door PIN diodes.
Bij het aanmaken van de lay-out is getracht de fysische afmetingen van de fasedraaier zo klein mogelijk te houden.
Er zijn uiteindelijk 3 substraten aangemaakt met bevredigende resultaten.
Het circuit met het 22,5 en 45 graden bit heeft over de frequentieband 0,75 dB transmissieverliezen en heeft een maximale fasefout van minder dan 3,5 graden.
Het circuit met het 90 en 180 graden bit heeft 1,3 dB transmissieverliezen. Alhoewel de gemiddelde fasedraaiing van het 90 graden bit incorrect is (98 graden), is de fasefout ten opzichte van dit gemiddelde minder dan 1,7 graden. Het 180 graden bit heeft een maximale fasefout van minder dan 4,5 graden.
Het circuit met de vier bit fasedraaier geeft goede resultaten wat betreft zowel de transmissieverliezen als de fase, maar heeft echter nog problemen met de VSWR.

APPENDIX A: ANALYSIS AND OPTIMIZATION OF THE SEPERATE FOUR PHASE SHIFTER BITS.

APPENDIX B: NETWORK AND TOPOLOGY SECTIONS

1 INTRODUCTION

In this report the development of a PIN diode phase shifter to operate at X-band (9.5 to 10.5 GHz) is described.
After the development of a C-band (5.4 to 6.0 GHz) [2] and an S-band phase shifter (2.8 to 3.2 GHz) [1] an X-band phase shifter was designed, using the same components which are used for the C-band phase shifter.
The phase shifter has a four bit configuration.
As the phase shifters at lower frequencies, it consists of a 22.5 and 45 degree loaded line and a 90 and 180 degree hybrid coupled sections.
All bits make use of two series mounted Hewlett-Packard type HP5082-0047 PIN diode chips.
The designed phase shifter has been built on 0.635 mm thick alumina.
The four bit configuration is made on a 25.4 to 25.4 mm alumina substrate.
Because it was at that time not possible to produce X-band microstrip circuits at the former Physics Laboratory TNO, the circuits have been fabricated at Hollandse Signaal Apparaten B.V. (Hengelo, Netherlands) and at the former LEOK (Oegstgeest, Netherlands).
This implies that it was impossible to produce many different circuits and the development time was not optimal.
The next sections in this report describe the theoretical performance characteristics and the experimental results of three circuits with two or more phase shifter bits on an alumina substrate.

2 CIRCUIT SELECTION

The configuration of the microstrip diode phase shifters at 3 and 6 GHz [1,2] gave good results, so this configuration has been chosen for the X-band diode phase shifter.
The X-band phase shifter was designed with series mounted PIN diode chips switching open-circuited transmission lines.
At 3 and 6 GHz this configuration was selected by considerations of low loss, simplicity and small geometrical dimensions.

2.1 Loaded-line configuration for the 22.5 and 45 degree bits

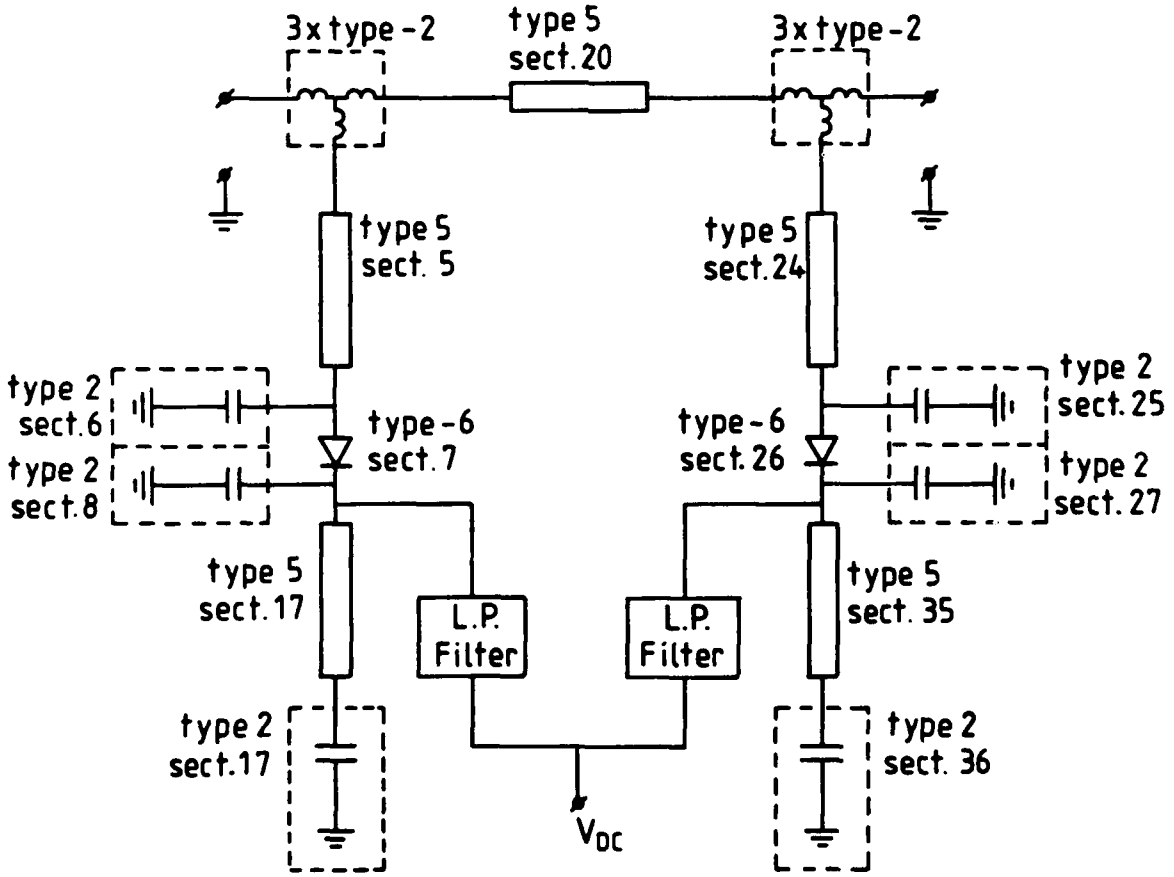


Figure 2.1 Schematic circuit of the loaded-line phase shifter

Figure 2.1 shows the schematic circuit diagram of the loaded-line phase shifter.
The numbering of the transmission lines is equal to the line numbers of the data-input for the optimization program PHASER (appendix A).
The loaded-line configuration consists of two identical open-circuited stubs, each provided with a PIN diode chip, spaced approximately a quarter-wavelength apart on the main transmission line.
Switching the two PIN diodes from one state to the other results in a differential phase shift.

The bias voltages and currents are supplied via a two-stage low pass filter, consisting of four transmission lines each approximately a quarter wavelength long (line number 10-14 and 29-33).
The discontinuities near the end of the open circuited lines and near the gaps are shown as capacitances.
The microstrip T-junction discontinuities present in the main transmission line near the two shunts are accounted as negative inductions

The loaded line phase shifter has very low insertion loss and is small in size.
Drawbacks of this configuration are the narrow bandwidth and a maximum phase shift of approximately 45 degrees.

2.2 Hybrid coupled configuration for the 90 and 180 degree bits

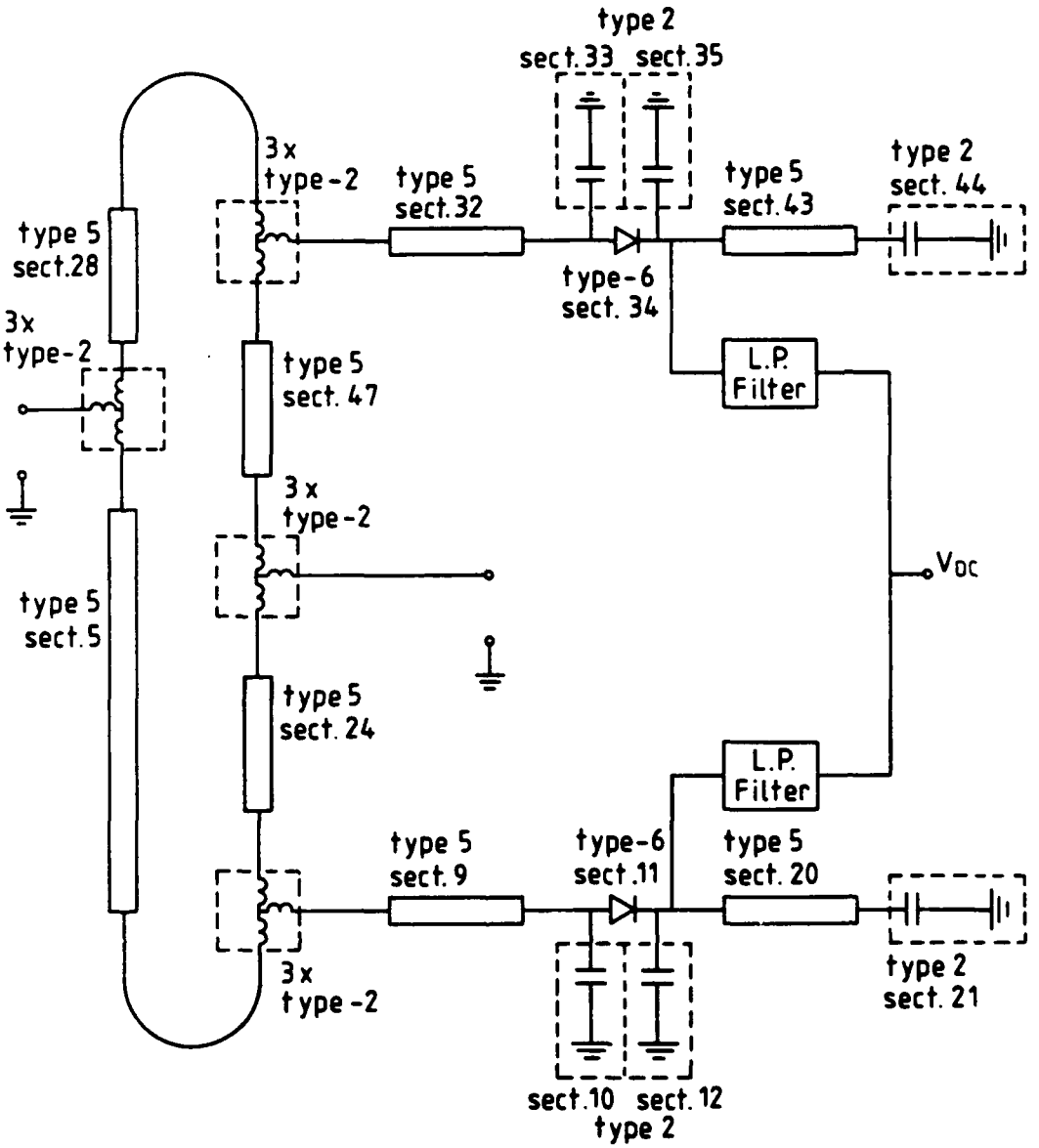


Figure 2.2 Schematic circuit diagram of the hybrid coupled configuration

As described before, the best solution for a 45 degree phase shifter is the loaded line configuration, due to its low loss and small size.
To achieve 90 degree phase shift two 45 degree phase shifter are needed, but with two phase shifters both advantages of the loaded line configuration are not valid anymore.
Both the 90 and the 180 degree phase shifters employ the hybrid coupled configuration.
This type of phase shifter is easy to develop and can produce a large phase shifts.
Its insertion loss is higher than the loaded line phase shifter.
Figure 2.2 shows the schematic circuit diagram of the hybrid coupled configuration.
At the input of the hybrid coupled phase shifter the signal splits equally into the two arms terminated with the reactive loads.
The reactive loads consist of an open-circuited transmission line with a series mounted PIN diode at some distance from the open end.
The power reflected at the end of these loads is recombined in the rat-race ring and leaves at the output of the phase shifter.
Switching the PIN diodes in and out, a differential phase shift will be achieved.
The bias voltages and currents for switching the PIN diodes are supplied via a two stage low pass filter, each approximately a quarter wavelength long (line number 13-18 and 37-41).
The line numbers in the schematic diagram correspond with the line numbers of the data input of the optimization program PHASER (appendix A).

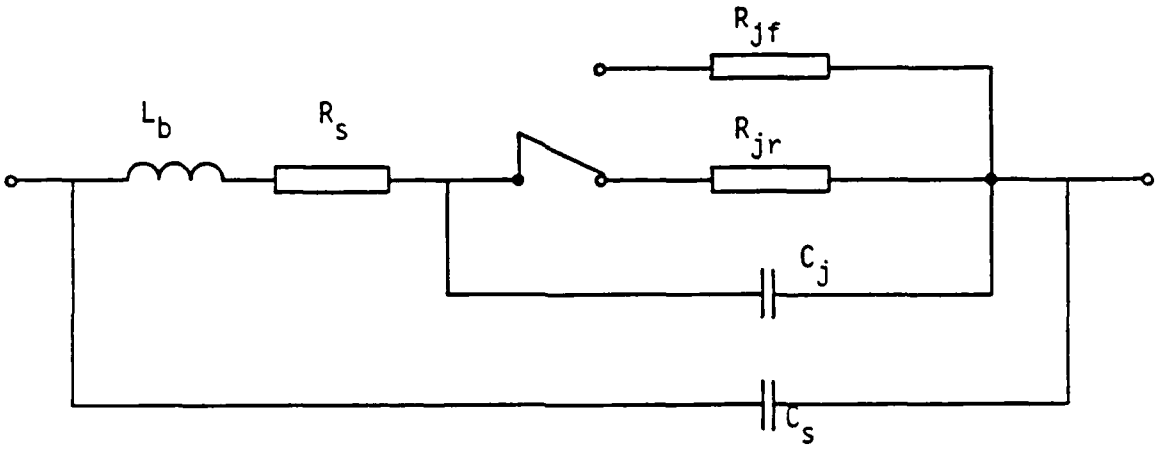
3 EQUIVALENT CIRCUIT OF THE SERIES MOUNTED PIN DIODE CHIPS

The X-band phase shifter uses PIN diodes for switching additional transmission lines.
This type of diode consist of three layers of semiconductor material as shown in Figure 3.1

Figure 3.1 construction of a PIN diode

The I-layer of the PIN diode is a pure intrinsic material and has a relative high specific resistance.
In reverse state the I-layer absorbes the total reverse voltage and the capacity will be constant due to a reverse voltage.
In forward state the I-layer will be saturated with electrons and will have a low resistance.
The PIN diode used for this phase shifter is the HP5082-0047 produced by Hewlett and Packard.
This diode has been chosen because it is a chip model and has less parasitic losses due to the lack of package.
The chip is direct mounted on the circuit with silver compound and the tranmission line to switch in and out is connected to the top of the chip diode via a golden bonding wire.
The amplitude of the reverse voltage and the forward current is approximately 50 volts and 100 mA for each PIN diode.
This current and voltage is sufficient to garanty a good performance for low RF power.

To describe the PIN diode in terms for the optimization program PHASER the following electrical schematic diagram was used for the PIN diode (Figure 3.2).



Where : L_b - inductance of the bonding wire
C_s - capacity of the gap
R_s - series resistance of the diode and bonding wire
R_{jf} - junction resistance of the diode forward
R_{jr} - junction resistance of the diode reverse
C_j - junction capacity of the diode reverse

Figure 3.2 Electrical schematic diagram of the PIN diode including the bonding wire.

For optimization there are now two situations of the PIN diode;

- forward state : The diode has a low ohmic resistance and has no capacity
- reverse state : The diode has a high resistance and some junction capacity

In both cases the diode plus bonding wire has a inductance and a certain resistance.

The HP 5082-0047 diode is used because of the good performances for the C-band and S- band phase shifters.
A problem with the HP diode for the X-band phase shifter is the actual size of the diode.
In the theoretical model of the diode the size of the diode is very small in comparison with the length of the transmission lines.
For the X-band phase shifter the diode size is no longer small in comparison to the wavelength.
Developing a new theoretical model was impossible and the design of the phase shifter was done with the old model. Futher improvement of the circuit behaviour was done experimentally.

4 CIRCUIT DESIGN BY COMPUTER OPTIMIZATION

To optimize the single bits the computer program PHASER is used [1].
In this program the parameters of the PIN diode model, the circuit topology and the electrical dimensions of the transmission lines are given.
Selected parameters of the transmission lines are optimized in order to achieve a constant phase shift, a good input and output match and a low insertion loss over the required frequency band.
All capacitances of the transmission lines, the diode and the gap as well as the microstrip T-junction discontinuity effects are taken into account.
The calculation of the optimized transmission lines is based on a 0.635 mm thick alumina substrate with a dielectric constant of 9.9 and assumes a TEM transmission line mode for microstrip.
The attenuation constant of a 50 Ohm transmission line is assumed to be 0.08 dB/Lambda and for other transmission lines the attenuation constant is proportional with the line impedance normalized to 50 Ohms.

4.1 Theoretical results for the 22.5 and 45 degree loaded line bits

In order to achieve the best results for both the 22.5 and the 45 degree bits, the lengths of all transmission lines are optimized, the low pass filter for the d.c. bias included.
Besides the optimization of the length of the transmission lines the width of the transmission line connecting the two stubs is also optimized.
Experimental results show that the phase shift for the 22.5 degree bit was to low, due to a lack of a good theoretical model for the PIN diode. In order to get the required 22.5 degree phase shift the design was done for a higher phase shift value.
The first experimental results of the 45 degree bit showed the desired phase shift at a wrong frequency, so a new optimization was made in an other frequency band.

The results of the theoretical results are given in Table 4.1 and 4.2 and are plotted in Figures 4.1 and 4.2.

FREQUENCY RESPONSE

	Forward biased			Reverse biased			
Freq GHz	VSWRI	VSWRO	Loss dB	VSWRI	VSWRO	Loss dB	Phase Degrees
8.70	1.576	1.589	.41	1.110	1.122	.19	34.61
8.80	1.443	1.455	.31	1.129	1.137	.19	33.61
8.90	1.334	1.347	.25	1.142	1.147	.19	32.62
9.00	1.246	1.260	.20	1.151	1.152	.19	31.84
9.10	1.175	1.191	.17	1.153	1.152	.19	31.22
9.20	1.121	1.139	.15	1.151	1.147	.20	30.74
9.30	1.085	1.106	.13	1.144	1.137	.20	30.42
9.40	1.072	1.093	.13	1.134	1.122	.20	30.23
9.50	1.082	1.098	.12	1.122	1.105	.20	30.19
9.60	1.102	1.114	.12	1.111	1.088	.20	30.29
9.70	1.123	1.132	.12	1.107	1.075	.21	30.53
9.80	1.143	1.149	.12	1.113	1.077	.22	30.91
9.90	1.159	1.163	.13	1.135	1.099	.23	31.42
10.00	1.172	1.175	.13	1.172	1.139	.25	32.08
10.10	1.182	1.183	.13	1.222	1.192	.28	32.87
10.20	1.187	1.187	.13	1.286	1.258	.32	33.80
10.30	1.189	1.188	.13	1.364	1.336	.37	34.88

Table 4.1.1 : Theoretical results of the 22.5 degree loaded-line bit

Design objectives:

Phase = 32 degr, VSWRI = 1.03, VSWRO = 1.03, Loss = .2 dB

Dimensions of microstrip lines

Substrate height = .635 mm

Dielectric constant = 9.90

Sect	Type	Zo (Ohms)	Width (mm)	Length (mm)
5	5	60.0	.410	4.332
10	5	110.0	.058	3.596
12	3	25.0	1.974	2.216
13	5	110.0	.058	3.491
14	3	50.0	.614	3.273
16	5	60.0	.410	1.216
20	5	46.9	.698	3.460

Table 4.1.2 Design objectives of the 22.5 degree bit

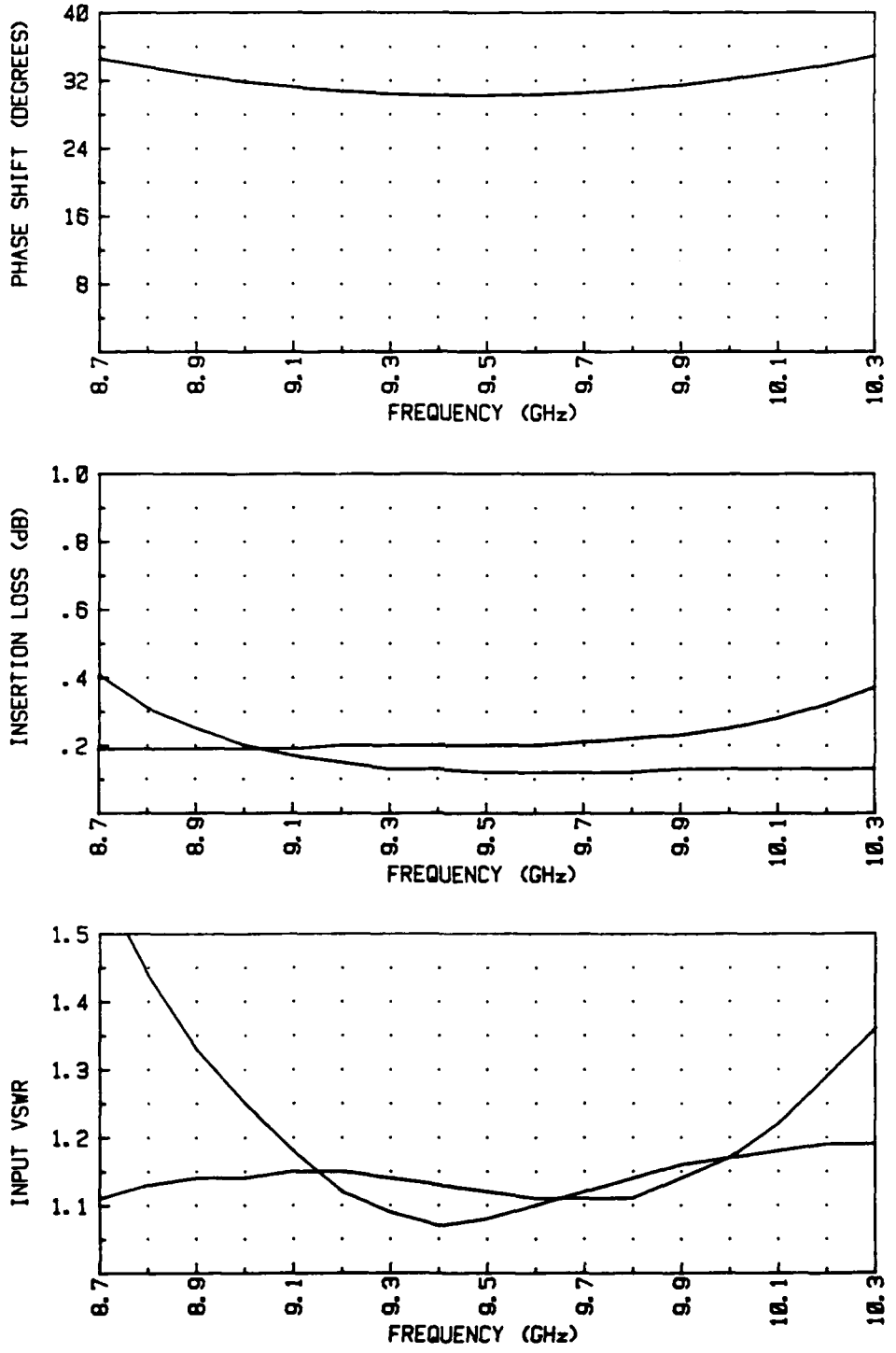


Figure 4.1 Theoretical results of the 22.5 degree loaded-line bit

FREQUENCY RESPONSE

	Forward biased			Reverse biased			
Freq GHz	VSWRI	VSWRO	Loss dB	VSWRI	VSWRO	Loss dB	Phase Degrees
8.40	1.918	1.918	.78	1.336	1.336	.27	63.56
8.50	1.699	1.699	.59	1.317	1.317	.27	61.12
8.60	1.523	1.523	.46	1.293	1.293	.26	59.00
8.70	1.382	1.382	.36	1.264	1.264	.25	57.22
8.80	1.266	1.266	.29	1.230	1.230	.25	55.77
8.90	1.172	1.172	.24	1.192	1.192	.24	54.65
9.00	1.095	1.095	.21	1.149	1.149	.24	53.84
9.10	1.034	1.034	.19	1.103	1.103	.24	53.36
9.20	1.033	1.033	.18	1.055	1.055	.24	53.18
9.30	1.078	1.078	.17	1.029	1.029	.26	53.31
9.40	1.122	1.122	.17	1.078	1.078	.28	53.75
9.50	1.162	1.162	.18	1.152	1.152	.31	54.50
9.60	1.197	1.197	.18	1.243	1.243	.37	55.57
9.70	1.228	1.228	.19	1.354	1.354	.44	56.97
9.80	1.254	1.254	.19	1.490	1.490	.55	58.70
9.90	1.274	1.274	.20	1.657	1.657	.69	60.78
10.00	1.290	1.290	.20	1.864	1.864	.88	63.19

Table 4.2.1 Theoretical results of the 45 degree loaded-line bit

Design objectives:

Phase = 58.0 degr, VSWRI = 1.03, VSWRO = 1.03, Loss = .2 dB

Dimensions of microstrip lines

Substrate height = .635 mm

Dielectric constant = 9.90

Sect	Type	Zo (Ohms)	Width (mm)	Length (mm)
5	5	70.0	.276	3.847
10	5	110.0	.058	3.437
12	3	25.0	1.974	2.519
13	5	110.0	.058	4.575
14	3	50.0	.614	4.076
16	5	70.0	.276	2.888
20	5	43.8	.796	3.262

Table 4.2.2 Design objectives of the 45 degree bit

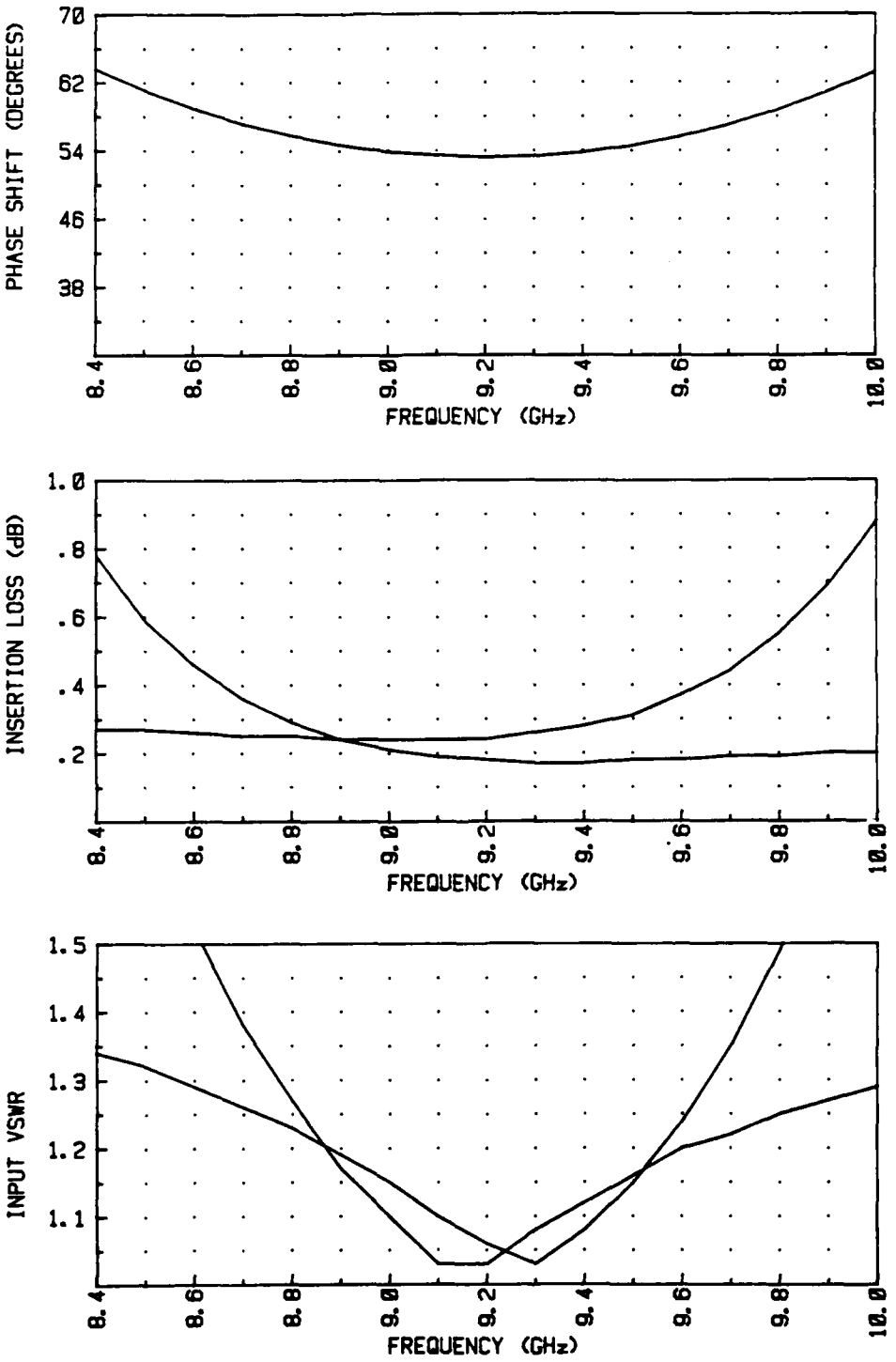


Figure 4.2 Theoretical results of the 45 degree loaded-line bit

4.2 Theoretical results for the 90 and 180 degree rat-race hybrid coupled bits.

For both the 90 and 180 degree bits the best performance is obtained by optimising the length of all transmission lines including all bias low pass filter transmission lines
After optimization of the 90 degree phase bit, the length of line number 5 was reduced to zero and the bonding wire of the PIN diode had to be placed on the rat-race ring.
Placing this bonding wire on the rat-race appeared to be very critical for the differential phase shift as well for the input and output impedance match.
Reproducing this 90 degree bit will be very critical.
Due to a lack of a optimal diode model, the inductance of the bonding wire and the junction capacity is determined experimentally for each separate bit.
Table 4.3 and 4.4 show the results of the optimization and Figure 4.3 and 4.4 show this data plotted.

FREQUENCY RESPONSE

	Forward biased			Reverse biased			
Freq GHz	VSWRI	VSWRO	Loss dB	VSWRI	VSWRO	Loss dB	Phase degrees
8.7	1.148	1.157	.33	1.250	1.245	.64	89.99
8.8	1.134	1.141	.32	1.193	1.187	.61	90.14
8.9	1.118	1.124	.31	1.144	1.137	.59	90.17
9.0	1.100	1.105	.30	1.104	1.096	.57	90.11
9.1	1.080	1.085	.30	1.074	1.064	.56	89.98
9.2	1.060	1.065	.29	1.056	1.044	.56	89.81
9.3	1.041	1.048	.29	1.054	1.041	.55	89.63
9.4	1.029	1.038	.28	1.064	1.050	.56	89.46
9.5	1.033	1.040	.28	1.077	1.064	.56	89.34
9.6	1.049	1.054	.27	1.091	1.077	.56	89.27
9.7	1.069	1.072	.27	1.104	1.089	.57	89.29
9.8	1.091	1.092	.27	1.115	1.097	.58	89.41
9.9	1.112	1.112	.27	1.124	1.104	.59	89.65
10.0	1.133	1.131	.27	1.130	1.107	.60	90.02
10.1	1.152	1.150	.28	1.135	1.109	.61	90.55
10.2	1.171	1.167	.28	1.138	1.108	.63	91.24
10.3	1.188	1.184	.28	1.139	1.105	.64	92.13

Table 4.3.1 Theoretical results of the 90 degree rat-race hybrid coupled bit

Design objectives:

Phase = 90 degr., VSWRI = 1.03, VSWRO = 1.03, Loss = .3 dB

Dimensions of microstrip lines

Substrate heigth = 0.635 mm

Dielectric constant = 9.900

Sect	Type	Zo Ohms	Width mm	Length mm
5	5	70.71	.268	9.309
11	5	110.00	.058	3.831
13	3	25.00	1.974	2.885
14	5	110.00	.058	3.156
15	3	25.00	1.974	3.167
17	5	50.00	.614	1.316
20	5	70.71	.268	2.968
24	5	70.71	.268	2.417
28	5	50.00	.614	3.110
39	5	50.00	.614	1.722
43	5	70.71	.268	2.478

Table 4.3.2 Design objectives of the 90 degree bit

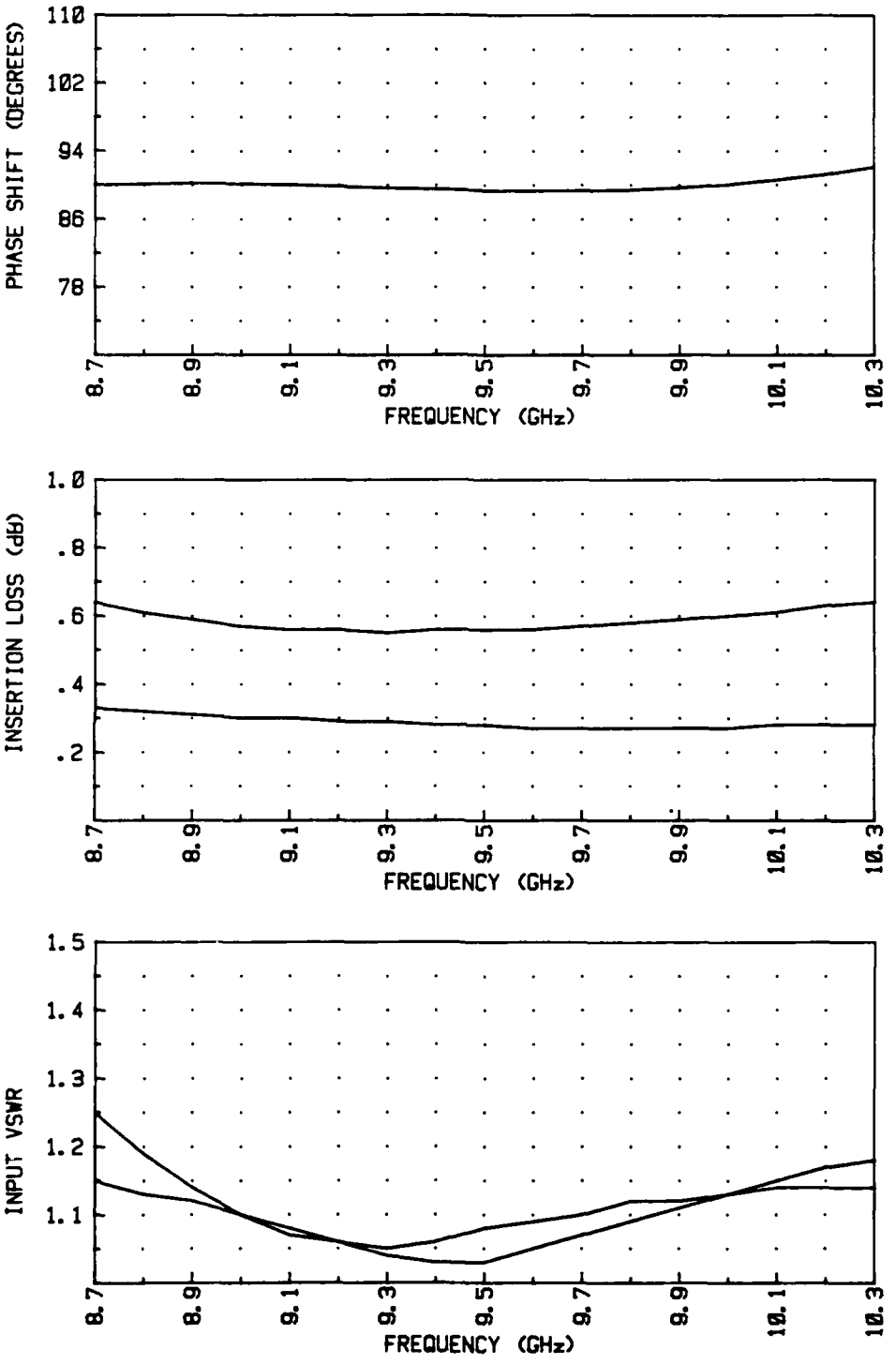


Figure 4.3 Theoretical results of the 90 degree rat-race hybrid coupled bit

FREQUENCY RESPONSE

	Forward biased			Reverse biased			
Freq GHz	VSWRI	VSWRO	Loss dB	VSWRI	VSWRO	Loss dB	Phase degrees
8.7	1.140	1.147	.41	1.147	1.141	.54	182.82
8.8	1.082	1.090	.40	1.128	1.122	.54	181.32
8.9	1.034	1.044	.39	1.107	1.103	.54	180.07
9.0	1.006	1.018	.38	1.085	1.082	.53	179.08
9.1	1.036	1.034	.38	1.062	1.060	.53	178.35
9.2	1.061	1.057	.38	1.040	1.038	.53	177.88
9.3	1.080	1.074	.38	1.024	1.020	.54	177.66
9.4	1.091	1.085	.38	1.026	1.017	.54	177.67
9.5	1.095	1.089	.38	1.043	1.032	.54	177.89
9.6	1.092	1.086	.38	1.062	1.050	.55	178.31
9.7	1.082	1.077	.38	1.081	1.065	.55	178.90
9.8	1.064	1.060	.38	1.096	1.077	.56	179.64
9.9	1.041	1.038	.38	1.107	1.084	.56	180.50
10.0	1.014	1.014	.38	1.114	1.086	.56	181.46
10.1	1.032	1.033	.39	1.117	1.083	.56	182.49
10.2	1.078	1.078	.40	1.118	1.078	.56	183.55
10.3	1.137	1.136	.42	1.120	1.075	.56	184.62

Table 4.4.1 Theoretical results of the 180 degree rat-race hybrid coupled bit

Design objectives:

Phase = 180 degr., VSWRI = 1.03, VSWRO = 1.03, Loss = .3 dB

Dimensions of microstrip lines

Substrate heigth = 0.635 mm

Dielectric constant = 9.900

Sect	Type	Zo Ohms	Width mm	Length mm
5	5	70.71	.268	9.642
9	5	50.00	.614	1.392
14	5	110.00	.058	3.856
16	3	25.00	1.974	2.344
17	5	110.00	.058	3.684
18	3	25.00	1.974	2.844
20	5	50.00	.614	2.893
24	5	70.71	.268	3.075
28	5	70.71	.268	3.711
32	5	50.00	.614	4.119
43	5	50.00	.614	2.804
47	5	70.71	.268	3.724

Table 4.4.2 Design objectives of the 180 degree bit

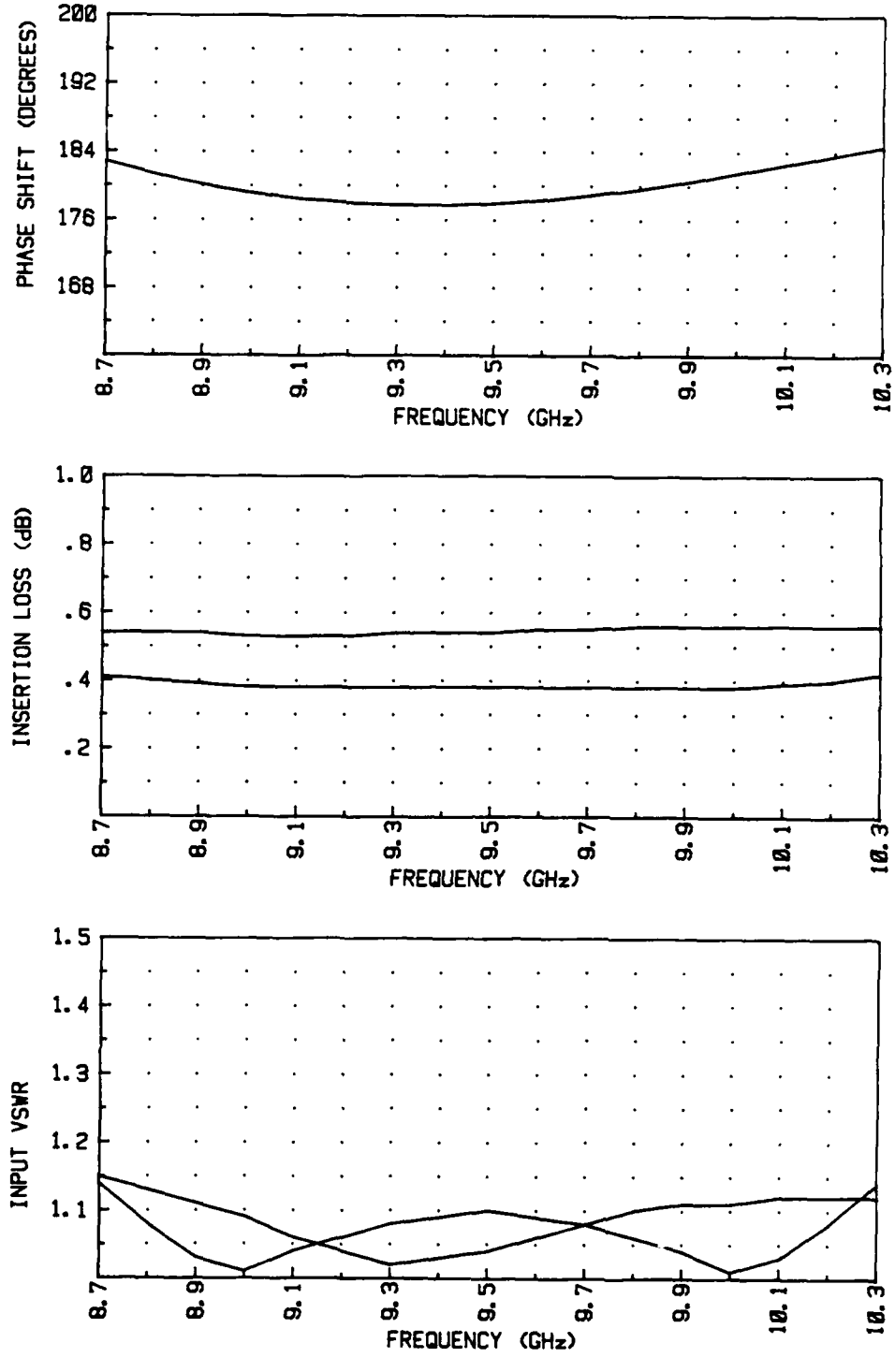


Figure 4.4 Theoretical results of the 180 degree rat-race hybrid coupled bit

5 EXPERIMENTAL RESULTS

To minimize experimental effort, the four bits are split into 2 sections; a substrate with the 22.5 and 45 degree bits and a substrate with the 90 and 180 degree bits.
With this set-up a good impression is obtained of the 4 separate bits.
Both, the 22.5 and 45 and the 90 and 180 have been built on a 0.635 thick alumina substrate of 25.4 mm by 50.8 mm.
Part 5.1 and 5.2 describes this two phase shifters respectively.
Finally the four bits have been built on one substrate as small as possible. Due to the reduction of size of the substrate, the physical lay-out is not exactly the same.
This 4 bit phase shifter was fabricated on a 0.635 mm thick alumina substrate of 25.4 by 25.4 mm.
Part 5.3 handles about the four bits built together.

5.1 Experimental results of the 22.5 and 45 degree bits

Figure 5.1 shows the lay-out of the 22.5 and 45 degree phase shifter.
The insertion loss, return loss and differential phase shift was measured over the frequency band of 9 GHz to 10 GHz.

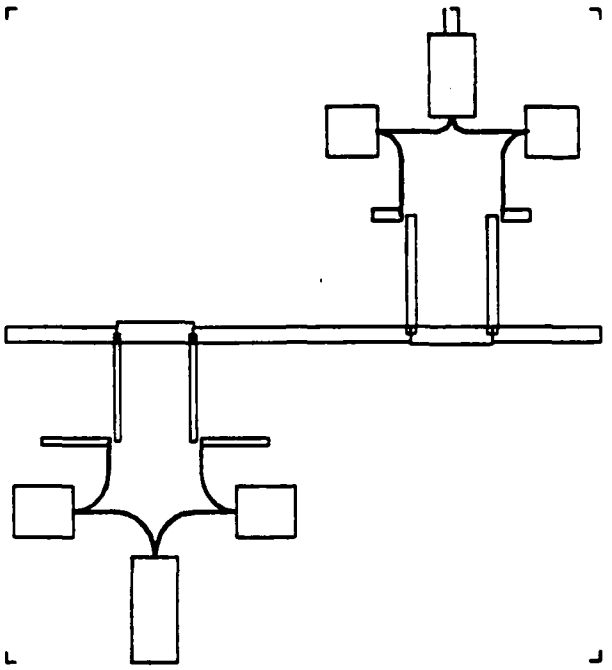


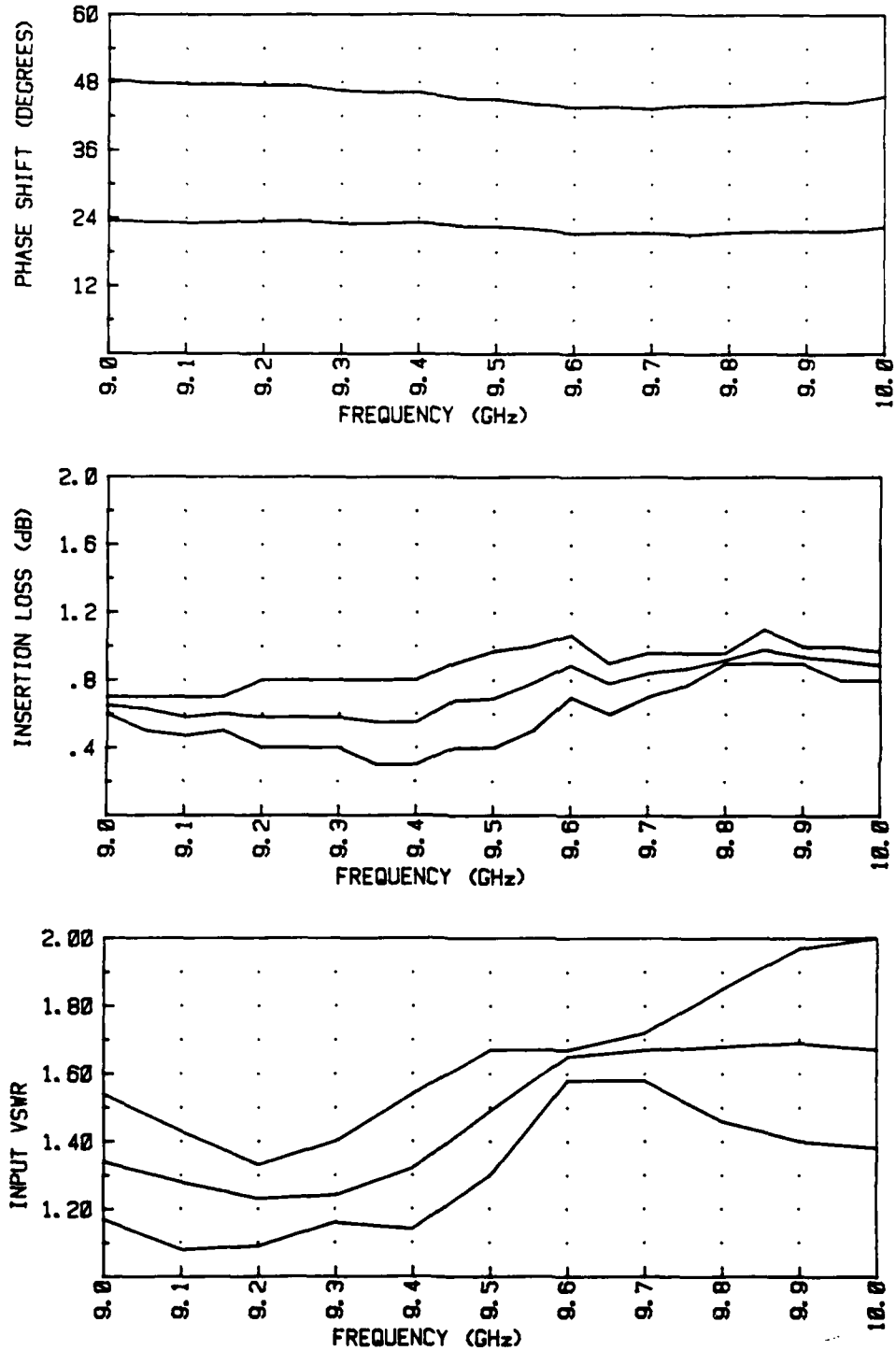
Figure 5.1 Lay-out of the 22.5 and 45 degree bits

The results of the phase shift of the 22.5 degree bit show an error of less than 1.3 degrees over the frequency band, while the error of the 45 degree bit is less than 3.5 degrees.
The average insertion loss of this two bit phase shifter in all bias states from 9.0 to 10.0 GHz is less than 0.75 dB.
Measured maximum insertion loss was less than 1.1 dB.
This insertion loss includes also the loss of the two microstrip SMA connectors.
The VSWR of the two bit phase shifter is less than 2.0.
Table 5.1 shows the results of the smallest bits and Figure 5.2 shows the plotted data.

Frequency (GHz)	Input VSWR (*) min.	aver.	max.	Insertion loss (*) min. (dB)	aver. (dB)	max. (dB)	Phase shift 22.5 degr. bit (degrees)	45 degr. bit (degrees)
9.0	1.17	1.34	1.54	0.6	0.65	0.7	23.5	48.4
9.1	1.08	1.28	1.43	0.47	0.58	0.7	23.1	47.7
9.2	1.09	1.23	1.33	0.4	0.58	0.8	23.4	47.5
9.3	1.16	1.24	1.40	0.4	0.58	0.8	23.0	46.5
9.4	1.14	1.32	1.54	0.3	0.55	0.8	23.2	46.2
9.5	1.30	1.49	1.67	0.4	0.69	0.97	22.5	45.0
9.6	1.58	1.65	1.67	0.7	0.89	1.07	21.3	43.6
9.7	1.58	1.67	1.72	0.7	0.84	0.96	21.3	43.3
9.8	1.46	1.68	1.85	0.9	0.92	0.96	21.3	43.9
9.9	1.40	1.69	1.97	0.9	0.94	1.0	21.7	44.6
10.0	1.38	1.67	2.00	0.8	0.89	0.97	22.4	45.5

(*) = Any bias state

Table 5.1 Experimental results of the 22.5 and 45 degree bits



(*) = any bias state

Figure 5.2 Experimental results of the 22.5 and 45 degree bits

5.2 Experimental results of the 90 and 180 degree bits

Figure 5.3 shows the lay-out of the 90 and 180 degree phase shifter.
The two bit phase shifter was measured over the frequency band of 9.0 to 10.0 GHz.

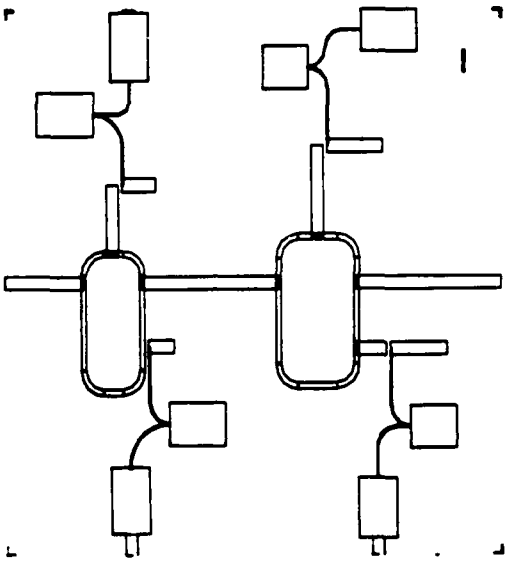


Figure 5.3 Lay-out of the 90 and 180 degree bits

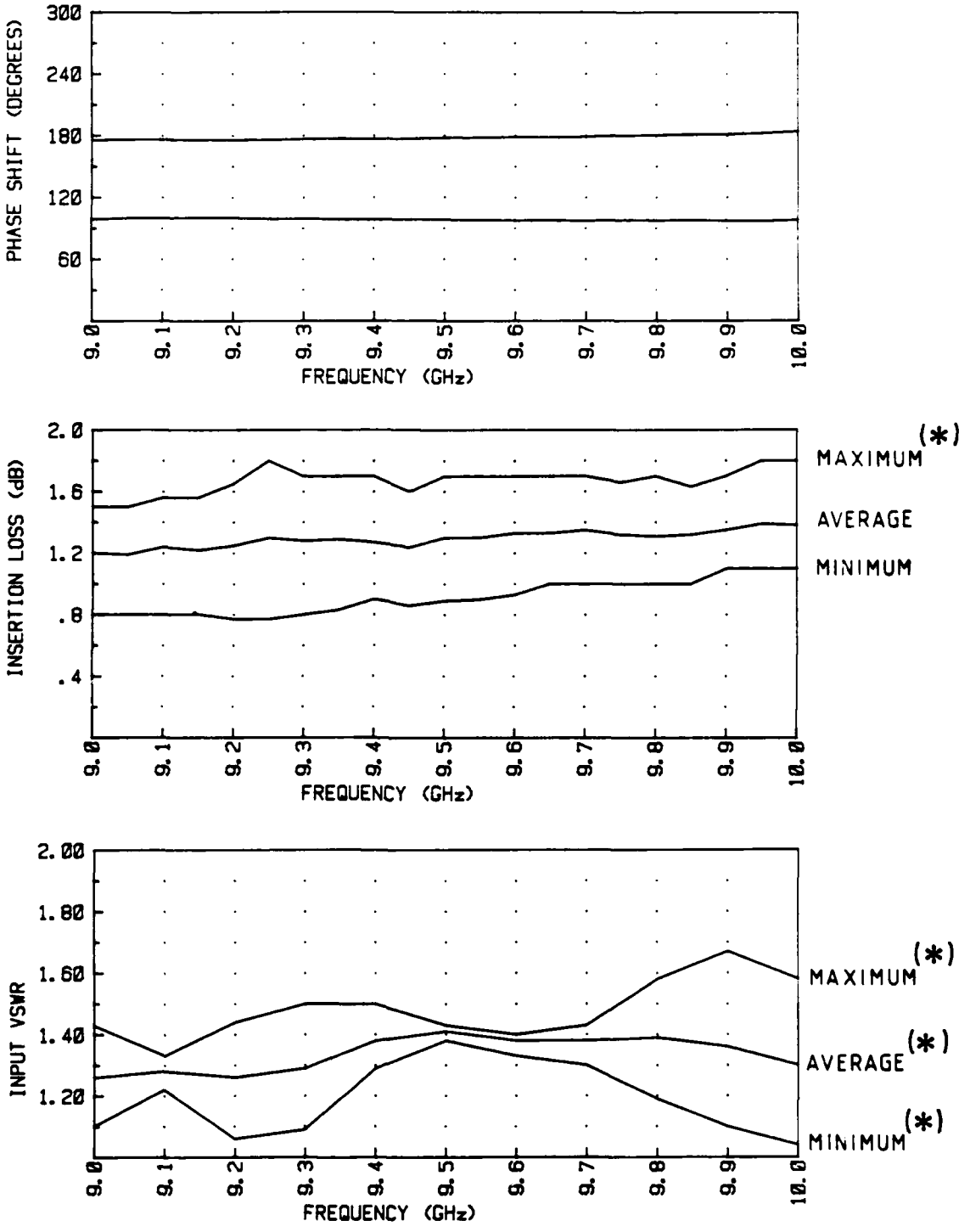
The 90 degree phase shifter has an average phase shift of 98.2 degrees.
The maximum deviation from this average phase shift is less than 1.9 degrees over the frequency band 9 - 10 GHz.
Although the average phase shift of this bit is not the desired 90 degrees, the phase deviation error is excellent.
The 180 degree phase bit gives very good results.
The average phase shift of the 180 degree bit is 178.5 degrees which is nearly the desired phase shift.
The phase deviation in regard to a phase shift of 180 degrees is less than 4.5 degrees.
The average insertion loss of the subtrate with the two bits is 1.3 dB (all bias states included) with a maximum of less than 1.8 dB.

This insertion losses include also the losses of the SMA connectors. Over the measured frequency band the VSWR of this two bit phase shifter is less than 1.7.

Frequency (GHz)	Input VSWR (*) min.	aver.	max.	Insertion loss (*) min. (dB)	aver. (dB)	max. (dB)	Phase shift 90 degr. bit (degrees)	180 degr. bit (degrees)
9.0	1.10	1.26	1.43	0.8	1.20	1.5	98.6	175.6
9.1	1.22	1.28	1.33	0.8	1.24	1.56	99.8	176.3
9.2	1.06	1.26	1.44	0.77	1.25	1.65	99.8	176.1
9.3	1.09	1.29	1.50	0.8	1.28	1.7	99.1	176.9
9.4	1.29	1.38	1.50	0.9	1.27	1.7	98.2	176.7
9.5	1.38	1.41	1.43	0.89	1.30	1.7	98.2	177.7
9.6	1.33	1.38	1.40	0.93	1.33	1.7	97.6	178.7
9.7	1.30	1.38	1.43	1.0	1.35	1.7	97.0	179.0
9.8	1.19	1.39	1.58	1.0	1.31	1.7	97.4	180.6
9.9	1.10	1.36	1.67	1.1	1.35	1.7	96.9	181.4
10.0	1.04	1.30	1.58	1.1	1.38	1.8	97.9	184.1

(*) = Any bias state

Table 5.2 Experimental results of the 90 and 180 degree bits



(*) = any bias state

Figure 5.4 Experimental results of the 90 and 180 degree bits

5.3 Experimental results of the four bit phase shifter

This phase shifter was also measured over the frequency band of 9.0 to 10.0 GHz.

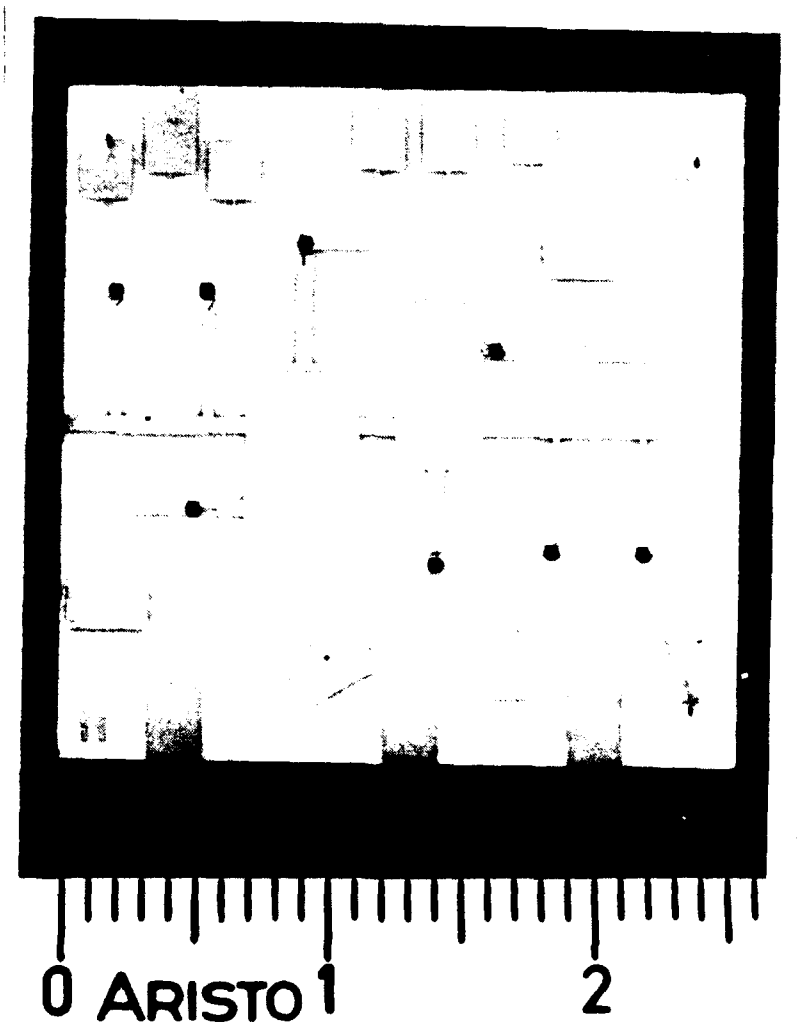


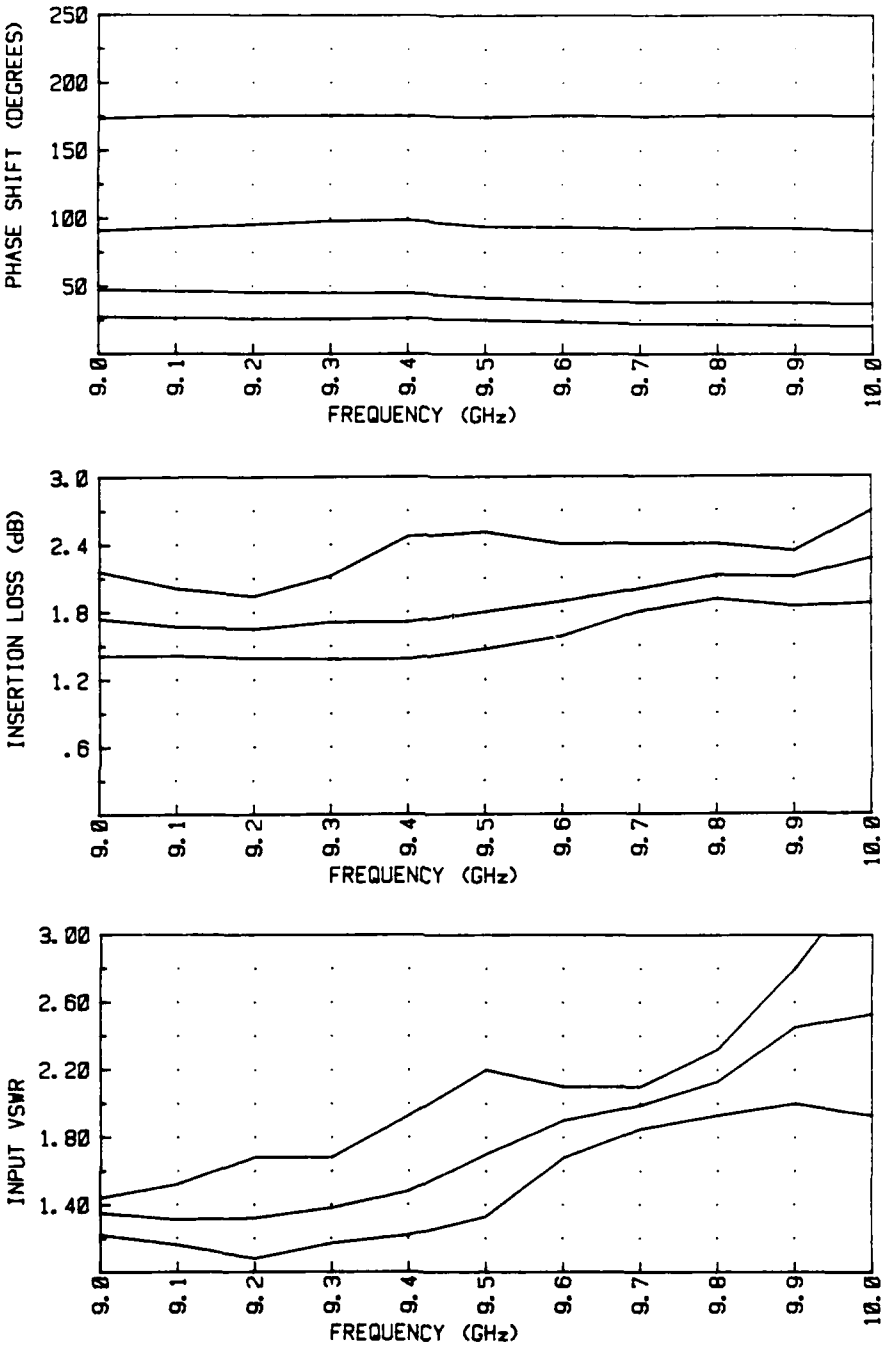
Figure 5.5 Lay-out of the X-band 4 bit phase shifter

Because the physical dimensions of the X-band phase shifter had to be minimized, the lay out of the separate phase shifters had to be modified.
The average phase shift of the 22.5 degree bit is 24.0 degrees with a maximum phase error of 3.5 degrees.
The average phase shift of the 45 degree bit is 41.85 degrees, with a maximum error of 5.65 degrees.
The 90 degree bit shows a average phase shift of 93.8 degrees, with a maximum error of 4.9 degrees.
The last bit, 180 degree bit has a average phase shift of 175.4 degrees, with a maximum error of 1.8 degrees.
The average insertion loss of the four bit phase shifter is less than 1.9 dB (all bias states included).
The maximum measured insertion loss is less than 2.5 dB.
This loss Figure includes the SMA connector losses.
The measured VSWR shows that the impedance match is not correct, since the measured maximum VSWR is about 3.4
Table 5.3 lists the tabulated experimental results of the four bit phase shifter. A graphical representation of these results is given in Figure 5.6.

Frequency (GHz)	Input VSWR (*) min.	aver.	max.	Insertion loss (*) min. (dB)	aver. (dB)	max. (dB)	Phase shift (bias state) 0001 (degrees)	0010	0100	1000
9.0	1.22	1.35	1.44	1.41	1.74	2.16	27.1	47.5	90.9	173.6
9.1	1.16	1.31	1.52	1.41	1.67	2.01	26.2	46.1	93.0	175.2
9.2	1.08	1.32	1.68	1.39	1.65	1.94	25.6	45.3	95.4	175.7
9.3	1.17	1.38	1.68	1.38	1.71	2.12	25.6	44.8	97.9	176.0
9.4	1.22	1.48	1.93	1.38	1.71	2.47	26.3	45.0	98.7	175.8
9.5	1.33	1.70	2.20	1.47	1.80	2.51	24.4	41.4	94.0	174.6
9.6	1.68	1.90	2.10	1.58	1.89	2.40	23.5	39.3	93.5	176.0
9.7	1.85	1.99	2.10	1.80	2.00	2.40	22.2	38.1	92.2	175.0
9.8	1.93	2.13	2.32	1.91	2.12	2.40	21.6	38.1	93.1	176.0
9.9	2.00	2.45	2.80	1.84	2.10	2.33	20.8	37.7	92.3	175.6
10.0	1.93	2.53	3.40	1.87	2.27	2.69	20.5	37.0	91.0	175.7

(*) = 5 bias states : 0000 = 0.0 degree
0001 = 22.5 degrees
0010 = 45.0 degrees
0100 = 90.0 degrees
1000 = 180.0 degrees

Table 5.3 Experimental results of the four bit X-band phase shifter



(*) - bias states : 0000 - 0.0 degree
0001 - 22.5 degree
0010 - 45.0 degrees
0100 - 90.0 degrees
1000 - 180.0 degrees

Figure 5.6 Experimental results of the four bit X-band phase shifter

6 CONCLUSIONS

This report describes the development of an X-band 4 bit phase shifter (22.5, 45, 90 and 180 degrees) for the frequency band of 9.0 to 10.0 GHz.

The two bit phase shifter with the 22.5 and the 45 degree bits, as well as the other two bit phase shifter, with the 90 and 180 degree bit, gives relative good results.

Although the average phase shift of the bits does not meet the exact design value, the maximum phase deviation is small.

The maximum phase deviation of the 22.5 degree bit is less than 1.3 degrees and the maximum phase deviation of the 45 degree bit is less than 3.5 degrees.

The average phase shift of the 90 degree bit is not optimal (98 degrees), but phase deviation over the band is excellent (less than 1.7 degrees). The 180 degree bit gives a phase deviation of less than 2.1 degrees.

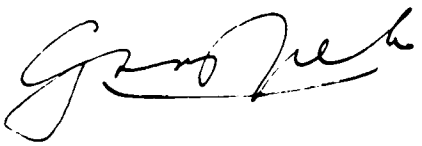
The average insertion loss of the lowest bits is .75 dB and the average insertion loss of the 90 + 180 degree bits is 1.3 dB.

These insertion losses include the losses of the two SMA connectors.

Building all bits on one small alumina substrate results in deterioration of the input match and insertion loss, due to the lack of optimization of the transmission lines between the bits and due to the RF coupling between the bits.

The final optimization of the bits was done experimentally, because of the lack of a good theoretical model of the PIN diode.

With the computer program PHASER good performances are possible for frequencies up to 6 GHz, but for higher frequencies a more accurate PIN diode model has to be developed.



Ir. G.A. v.d. Spek (Groupleader)

Ing. F.J. Klumpers (Author)

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8 ACKNOWLEDGMENT

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Appendix A

ANALYSES AND OPTIMIZATION OF THE FOUR INDIVIDUAL PHASE SHIFTER BITS

22.5 DEGREE LOADED-LINE BIT

Microwave network analyses/optimization

Input description of network configuration

Sect	Type	Parameters						
1	11	50.000						
2	-2	0.000	-.075	10000.000				
3	7							
4	-2	0.000	-.008	10000.000				
5	5	50.000	.350 V	.096				
6	2	0.000	.000	.010				
7	-6	.300	.025	.110	1.400	10000.000	0.000	
8	2	0.000	.000	.010				
9	7							
10	5	110.000	.250 V	.176				
11	2	0.000	.000	.080				
12	3	25.000	.200 V	.040				
13	5	110.000	.250 V	.176				
14	3	50.000	.250 V	.080				
15	8							
16	5	60.000	.100 V	.096				
17	2	0.000	.000	.026				
18	8							
19	-2	0.000	-.075	10000.000				
20	5	47.000 V	.250 V	.080				
21	15	2.000						
22	15	3.000						
23	15	4.000						
24	15	5.000						
25	15	6.000						
26	15	7.000						
27	15	8.000						
29	15	9.000						
30	15	10.000						
31	15	11.000						
32	15	12.000						
33	15	13.000						
34	15	14.000						
35	15	15.000						
36	15	17.000						
37	15	18.000						
38	12	50.000						

VARIABLE PARAMETERS WITH LIMITS BEFORE AND RESULTS AFTER OPTIMIZATION

Sect	Type	Param. before	Lower limit	Upper limit	Param after
5	5	.350	.300	.400	.354
10	5	.250	.200	.300	.281
12	3	.200	.150	.250	.198
13	5	.250	.200	.300	.273
14	3	.250	.200	.300	.272
16	5	.100	.050	.150	.099
20	5	47.000	45.000	50.000	46.900
20	5	.250	.200	.300	.290

Fractional wavelength reference frequency = 9.50 GHz

FREQUENCY RESPONSE

	Forward biased			Reverse biased			
Freq GHz	VSWRI	VSWRO	Loss dB	VSWRI	VSWRO	Loss dB	Phase Degrees
8.70	1.576	1.589	.41	1.110	1.122	.19	34.61
8.80	1.443	1.455	.31	1.129	1.137	.19	33.61
8.90	1.334	1.347	.25	1.142	1.147	.19	32.62
9.00	1.246	1.260	.20	1.151	1.152	.19	31.84
9.10	1.175	1.191	.17	1.153	1.152	.19	31.22
9.2	1.121	1.139	.15	1.151	1.147	.20	30.74
9.30	1.085	1.106	.13	1.144	1.137	.20	30.42
9.40	1.072	1.093	.13	1.134	1.122	.20	30.23
9.5	1.082	1.098	.12	1.122	1.105	.20	30.19
9.60	1.102	1.114	.12	1.111	1.088	.20	30.29
9.70	1.123	1.132	.12	1.107	1.075	.21	30.53
9.80	1.143	1.149	.12	1.113	1.077	.22	30.91
9.9	1.159	1.163	.13	1.135	1.099	.23	31.42
10.00	1.172	1.175	.13	1.172	1.139	.25	32.08
10.10	1.182	1.183	.13	1.222	1.192	.28	32.87
10.20	1.187	1.187	.13	1.286	1.258	.32	33.80
10.30	1.189	1.188	.13	1.364	1.336	.37	34.88

Design objectives

Phase = 32.0 degrees

VSWRI = 1.030

VSWRO = 1.030

Loss = .20 dB

Dimensions of microstrip lines

Substrate height = .635 mm
Dielectric constant = 9.90

Sect	Type	Zo (Ohms)	Width (mm)	Length (mm)
5	5	60.0	.410	4.332
10	5	110.0	.058	3.596
12	3	25.0	1.974	2.216
13	5	110.0	.058	3.491
14	3	50.0	.614	3.273
16	5	60.0	.410	1.216
20	5	46.9	.698	3.460

45 DEGREE LOADED-LINE BIT

Microwave network analyses/optimization

Input description of network configuration

Sect	Type	Parameters					
1	11	50.000					
2	-2	0.000	-.061	10000.000			
3	7						
4	-2	0.000	-.007	10000.000			
5	5	70.000	.300 V	.112			
6	2	0.000	.000	.007			
7	-6	.300	.025	.110	1.400	10000.000	0.000
8	2	0.000	.000	.010			
9	7						
10	5	110.000	.300 V	.176			
11	2	0.000	.000	.080			
12	3	25.000	.200 V	.040			
13	5	110.000	.350 V	.176			
14	3	50.000	.300 V	.080			
15	8						
16	5	70.000	.250 V	.112			
17	2	0.000	.000	.026			
18	8						
19	-2	0.000	-.061	10000.000			
20	5	45.000 V	.250 V	.080			
21	15	2.000					
22	15	3.000					
23	15	4.000					
24	15	5.000					
25	15	6.000					
26	15	7.000					
27	15	8.000					
29	15	9.000					
30	15	10.000					
31	15	11.000					
32	15	12.000					
33	15	13.000					
34	15	14.000					
35	15	15.000					
36	15	17.000					
37	15	18.000					
38	12	50.000					

VARIABLE PARAMETERS WITH LIMITS BEFORE AND RESULTS AFTER OPTIMIZATION

Sect	Type	Param before	Lower limit	Upper limit	Param after
5	5	.300	.250	.350	.300
10	5	.300	.250	.350	.260
12	3	.200	.150	.250	.217
13	5	.350	.300	.400	.346
14	3	.300	.250	.350	.328
16	5	.250	.200	.300	.225
20	5	45.000	43.000	47.000	43.793
20	5	.250	.200	.300	.256

Fractional wavelength reference frequency = 9.20 GHz

FREQUENCY RESPONSE

	Forward biased			Reverse biased			
Freq GHz	VSWRI	VSWRO	Loss dB	VSWRI	VSWRO	Loss dB	Phase Degrees
8.40	1.918	1.918	.78	1.336	1.336	.27	63.56
8.50	1.699	1.699	.59	1.317	1.317	.27	61.12
8.60	1.523	1.523	.46	1.293	1.293	.26	59.00
8.70	1.382	1.382	.36	1.264	1.264	.25	57.22
8.80	1.266	1.266	.29	1.230	1.230	.25	55.77
8.90	1.172	1.172	.24	1.192	1.192	.24	54.65
9.00	1.095	1.095	.21	1.149	1.149	.24	53.84
9.10	1.034	1.034	.19	1.103	1.103	.24	53.36
9.20	1.033	1.033	.18	1.055	1.055	.24	53.18
9.30	1.078	1.078	.17	1.029	1.029	.26	53.31
9.40	1.122	1.122	.17	1.078	1.078	.28	53.75
9.50	1.162	1.162	.18	1.152	1.152	.31	54.50
9.60	1.197	1.197	.18	1.243	1.243	.37	55.57
9.70	1.228	1.228	.19	1.354	1.354	.44	56.97
9.80	1.254	1.254	.19	1.490	1.490	.55	58.70
9.90	1.274	1.274	.20	1.657	1.657	.69	60.78
10.00	1.290	1.290	.20	1.864	1.864	.88	63.19

Design objectives

Phase = 58.0 degrees

VSWRI = 1.030

VSWRO = 1.030

Loss = .70 dB

Dimensions of microstrip lines

Substrate height = .635 mm

Dielectric constant = 9.90

Sect	Type	Zo (Ohms)	Width (mm)	Length (mm)
5	5	70.0	.276	3.847
10	5	110.0	.058	3.437
12	3	25.0	1.974	2.519
13	5	110.0	.058	4.575
14	3	50.0	.614	4.076
16	5	70.0	.276	2.888
20	5	43.8	.796	3.262

90 DEGREE RAT-RACE COUPLER BIT

Microwave network analyses/optimization

Input description of network configuration

Sect	Type	Parameters					
1	11	50.000					
2	-2	0.000	-.042	10000.000			
3	9						
4	-2	0.000	-.166	10000.000			
5	5	70.710	.750 V	.112			
6	7						
7	2	0.000	.000	.012			
8	-6	0.450	.025	.170	1.40	10000.000	0.00
9	2	0.000	.000	.012			
10	7						
11	5	110.000	.250 V	.176			
12	2	0.000	.000	.080			
13	3	25.000	.250 V	.040			
14	5	110.000	.250 V	.176			
15	3	25.000	.250 V	.040			
16	8						
17	5	50.000	.100 V	.080			
18	2	0.000	.000	.036			
19	8						
20	5	70.710	.250 V	.112			
21	-2	0.000	-.166	10000.000			
22	9						
23	-2	0.000	-.166	10000.000			
24	5	70.710	.200 V	.112			
25	-2	0.000	-.166	10000.000			
26	7						
27	-2	0.000	-.042	10000.000			
28	5	50.000	.250 V	.080			
29	2	0.000	.000	.012			
30	-6	0.450	.025	.170	1.4	10000.000	0.00
				10000.000	0.000		
31	2	0.000	.012				
32	7						
33	15	11.000					
34	2	0.000	.000	.080			
35	15	13.000					
36	15	14.000					
37	15	15.000					
38	8						

39	5	50.000	.150 V	.080
40	2	0.000	.000	.036
41	8			
42	-2	0.000	-.166	10000.000
43	5	70.710	.200 V	.112
44	-2	0.000	-.166	10000.000
45	10			
46	-2	0.000	-.042	10000.000
47	12	50.000		

VARIABLE PARAMETERS WITH LIMITS BEFORE AND RESULTS AFTER OPTIMIZATION

Sect	Type	Param before	Lower limit	Upper limit	Param after
5	5	.750	.700	.800	.749
11	5	.250	.200	.300	.299
13	3	.250	.200	.300	.257
14	5	.250	.200	.300	.247
15	3	.250	.200	.300	.283
17	5	.100	.050	.150	.109
20	5	.250	.200	.300	.239
24	5	.200	.150	.250	.195
28	5	.250	.200	.300	.259
39	5	.150	.100	.200	.143
43	5	.200	.150	.250	.199

Fractional wavelength reference frequency = 9.500 GHz

FREQUENCY RESPONSE

	Forward biased			Reverse biased			
Freq GHz	VSWRI	VSWRO	Loss dB	VSWRI	VSWRO	Loss dB	Phase degrees
8.7	1.148	1.157	.33	1.250	1.245	.64	89.99
8.8	1.134	1.141	.32	1.193	1.187	.61	90.14
8.9	1.118	1.124	.31	1.144	1.137	.59	90.17
9.0	1.100	1.105	.30	1.104	1.096	.57	90.11
9.1	1.080	1.085	.30	1.074	1.064	.56	89.98
9.2	1.060	1.065	.29	1.056	1.044	.56	89.81
9.3	1.041	1.048	.29	1.054	1.041	.55	89.63
9.4	1.029	1.038	.28	1.064	1.050	.56	89.46
9.5	1.033	1.040	.28	1.077	1.064	.56	89.34
9.6	1.049	1.054	.27	1.091	1.077	.56	89.27
9.7	1.069	1.072	.27	1.104	1.089	.57	89.29
9.8	1.091	1.092	.27	1.115	1.097	.58	89.41
9.9	1.112	1.112	.27	1.124	1.104	.59	89.65
10.0	1.133	1.131	.27	1.130	1.107	.60	90.02
10.1	1.152	1.150	.28	1.135	1.109	.61	90.55
10.2	1.171	1.167	.28	1.138	1.108	.63	91.24
10.3	1.188	1.184	.28	1.139	1.105	.64	92.13

Design objectives

Phase = 90.000 degrees
VSWRI = 1.030
VSWRO = 1.030
Loss = .300 dB

Dimensions of microstrip lines

Substrate heigth = 0.635 mm
Dielectric constant = 9.900

Sect	Type	Zo Ohms	Width mm	Length mm
5	5	70.71	.268	9.309
11	5	110.00	.058	3.831
13	3	25.00	1.974	2.885
14	5	110.00	.058	3.156
15	3	25.00	1.974	3.167
17	5	50.00	.614	1.316
20	5	70.71	.268	2.968
24	5	70.71	.268	2.417
28	5	50.00	.614	3.110
39	5	50.00	.614	1.722
43	5	70.71	.268	2.478

180 DEGREE RAT-RACE COUPLER BIT

Microwave network analyses/optimization

Input description of network configuration

Sect	Type	Parameters						
1	11	50.000						
2	-2	0.000	-.042	10000.000				
3	9							
4	-2	0.000	-.166	10000.000				
5	5	70.710	.750 V	.112				
6	-2	0.000	-.166	10000.000				
7	7							
8	-2	0.000	-.042	10000.000				
9	5	50.000	.100 V	.080				
10	2	0.000	.000	.012				
11	-6	0.450	.025	.110	1.40	10000.000	0.00	
12	2	0.000	.000	.012				
13	7							
14	5	110.000	.250 V	.176				
15	2	0.000	.000	.080				
16	3	25.000	.250 V	.040				
17	5	110.000	.250 V	.176				
18	3	25.000	.250 V	.040				
19	8							
20	5	50.000	.250 V	.080				
21	2	0.000	.000	.036				
22	8							
23	-2	0.000	-.166	10000.000				
24	5	70.710	.200 V	.112				
25	-2	0.000	-.166	10000.000				
26	9							
27	-2	0.000	-.166	10000.000				
28	5	70.710	.250 V	.112				
29	-2	0.000	-.166	10000.000				
30	7							
31	-2	0.000	-.042	10000.000				
32	5	50.000	.300 V	.080				
33	2	0.000	.000	.012				
34	-6	0.450	.025	.110	1.40	10000.000	0.00	
35	2	0.000	.012					
36	7							

37	15	14.000		
38	2	0.000	.000	.080
39	15	16.000		
40	15	17.000		
41	15	18.000		
42	8			
43	5	50.000	.250 V	.080
44	2	0.000	.000	.036
45	8			
46	-2	0.000	-.166	10000.000
47	5	70.710	.250 V	.112
48	-2	0.000	-.166	10000.000
49	10			
50	-2	0.000	-.042	10000.000
51	12	50.000		

VARIABLE PARAMETERS WITH LIMITS BEFORE AND RESULTS AFTER OPTIMIZATION

Sect	Type	Param before	Lower limit	Upper limit	Param after
5	5	.750	.700	.800	.776
9	5	.100	.080	.150	.116
14	5	.300	.300	.350	.301
16	3	.250	.200	.300	.209
17	5	.250	.200	.300	.288
18	3	.250	.200	.300	.254
20	5	.250	.200	.300	.241
24	5	.200	.150	.250	.248
28	5	.250	.200	.300	.299
32	5	.300	.280	.350	.342
43	5	.250	.200	.300	.233
47	5	.250	.200	.300	.300

Fractional wavelength reference frequency = 9.500 GHz

FREQUENCY RESPONSE

	Forward biased			Reverse biased			
Freq GHz	VSWRI	VSWRO	Loss dB	VSWRI	VSWRO	Loss dB	Phase degrees
8.7	1.140	1.147	.41	1.147	1.141	.54	182.82
8.8	1.082	1.090	.40	1.128	1.122	.54	181.32
8.9	1.034	1.044	.39	1.107	1.103	.54	180.07
9.0	1.006	1.018	.38	1.085	1.082	.53	179.08
9.1	1.036	1.034	.38	1.062	1.060	.53	178.35
9.2	1.061	1.057	.38	1.040	1.038	.53	177.88
9.3	1.080	1.074	.38	1.024	1.020	.54	177.66
9.4	1.091	1.085	.38	1.026	1.017	.54	177.67
9.5	1.095	1.089	.38	1.043	1.032	.54	177.89
9.6	1.092	1.086	.38	1.062	1.050	.55	178.31
9.7	1.082	1.077	.38	1.081	1.065	.55	178.90
9.8	1.064	1.060	.38	1.096	1.077	.56	179.64
9.9	1.041	1.038	.38	1.107	1.084	.56	180.50
10.0	1.014	1.014	.38	1.114	1.086	.56	181.46
10.1	1.032	1.033	.39	1.117	1.083	.56	182.49
10.2	1.078	1.078	.40	1.118	1.078	.56	183.55
10.3	1.137	1.136	.42	1.120	1.075	.56	184.62

Design objectives

Phase - 180.000 degrees
VSWRI - 1.030
VSWRO - 1.030
Loss - .300 dB

Dimensions of microstrip lines

Substrate heigth - 0.635 mm
Dielectric constant - 9.900

Sect	Type	Zo Ohms	Width mm	Length mm
5	5	70.71	.268	9.642
9	5	50.00	.614	1.392
14	5	110.00	.058	3.856
16	3	25.00	1.974	2.344
17	5	110.00	.058	3.684
18	3	25.00	1.974	2.844
20	5	50.00	.614	2.893
24	5	70.71	.268	3.075
28	5	70.71	.268	3.711
32	5	50.00	.614	4.119
43	5	50.00	.614	2.804
47	5	70.71	.268	3.724

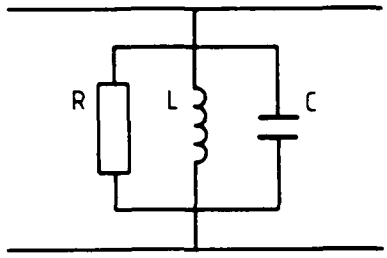
Appendix B

NETWORK AND TOPOLOGY SECTIONS

Parallel Parallel

Type : 1

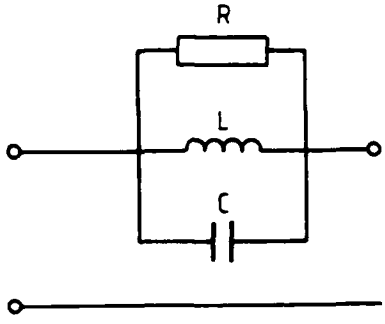
Data : R, L, C



Series Parallel

Type : -1

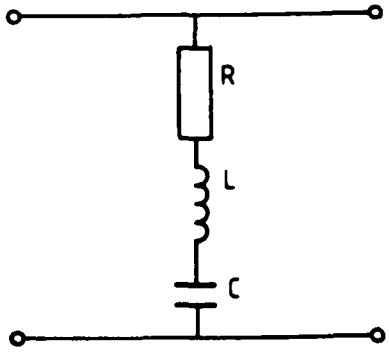
Data : R, L, C



Parallel Series

Type : 2

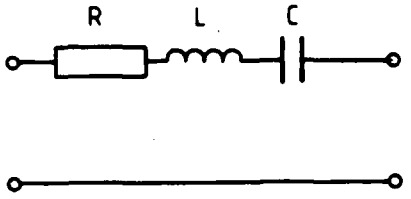
Data : R, L, C



Series Series

Type : -2

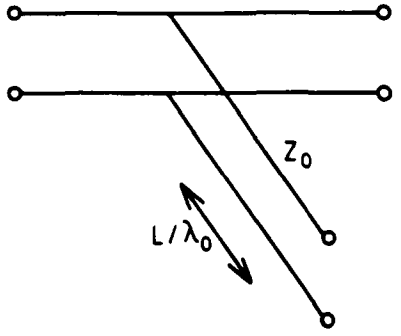
Data : R, L, C



Parallel Open

Type : 3

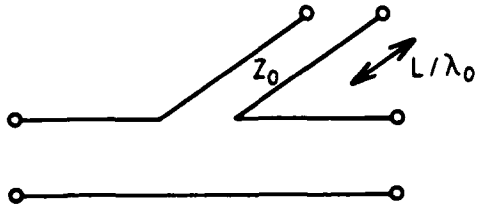
Data : Z_o, L/λ_o, α/λ_o



Series Open

Type : -3

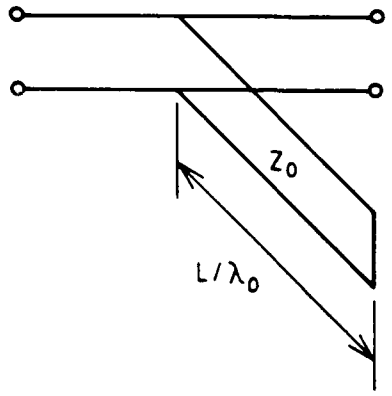
Data : Z_o, L/λ_o, α/λ_o



Parallel Short

Type : 4

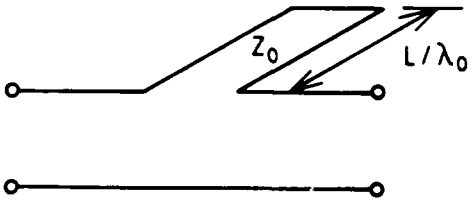
Data : Z_o, $L/\lambda o$, $\alpha/\lambda o$



Series Short

Type : $-4R_{jf}$

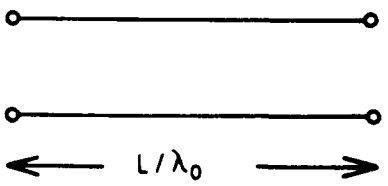
Data : Z_o, $L/\lambda o$, $\alpha/\lambda o$



Series Lined

Type : 5

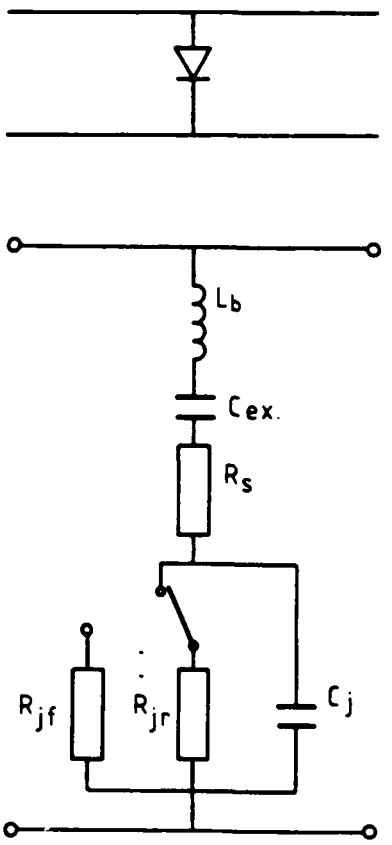
Data : Z_o, $L/\lambda o$, $\alpha/\lambda o$



Parallel PIN diode

Type : 6

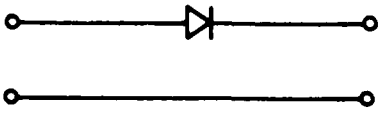
Data : L_b, C_{ex}, C_j, R_s, R_{jf}, R_{jr}



Series PIN diode

Type : -6

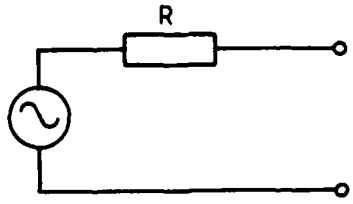
Data : L_b, C_{ex}, C_j, R_s, R_{jf}, R_{jr}



Branch Start
Type : 7
Data : none

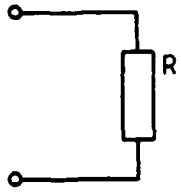
Generator
Type : 11
Data : R

Branch Termination
Type : 8
Data : none
Branch is in parallel with
main path



Branch Termination
Type : -8
Data : none
Branch is in series with
main path

Load
Type : 12
Data : R



Parallel Path Start
Type : 9
Data : none

Combination Parallel Paths
Type : 10
Data : none

Copy Sect
Type : 15
Data : Line number
to be copied

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10. TITLE AND SUBTITLE

DESIGN OF AN X-BAND PIN DIODE PHASE SHIFTER BY COMPUTER OPTIMIZATION

11. AUTHOR(S)

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12. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

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13. SPONSORING/MONITORING AGENCY NAME(S)

14. SUPPLEMENTARY NOTES

15. ABSTRACT (MAXIMUM 200 WORDS, 1044 POSITIONS)

THIS REPORT DESCRIBES THE DESIGN AND EXPERIMENTAL RESULTS OF A FOUR BIT MICROSTRIP DIODE PHASE SHIFTER IN THE FREQUENCY BAND OF 9.0 TO 10.0 GHZ

THE PHASE SHIFTER HAS BEEN BUILT ON AN ALUMINA SUBSTRATE AND THE DESIRED DIFFERENTIAL PHASE SHIFT IS REACHED BY SWITCHING TRANSMISSION LINES BY PIN DIODES.

THE LAY-OUT OF THE CIRCUITS WAS DESIGNED FOR MINIMUM PHYSICAL DIMEN-SIONS.

THREE CIRCUITS HAVE BEEN REALIZED WITH GOOD RESULTS.

THE CIRCUIT CONTAINING THE 22.5 AND 45 DEGREE BITS, GIVES AN INSERTION LOSS OF 0.75 DB AND A MAXIMUM PHASE DEVIATION OF LESS THAN 3.5 DEGREES. THE CIRCUIT CONTAINING THE 90 AND 180 DEGREE BITS, GIVES AN INSERTION LOSS OF 1.3 DB. THE AVERAGE PHASE SHIFT OF THE 90 DEGREE BIT IS NOT OPTIMAL (98 DEGREES) BUT THE PHASE DEVIATION IN REGARD TO THE AVERAGE PHASE SHIFT IS LESS THAN 1.7 DEGREES. THE 180 DEGREE BIT GIVES A PHASE DEVIATION OF LESS THAN 4.5 DEGREE.

THE FOUR BIT PHASE SHIFTER GOOD RESULTS FOR BOTH INSERTION LOSS AND DIFFERENTIAL PHASE SHIFT, BUT STILL HAS SERIOUS PROBLEMS WITH THE INPUT IMPEDANCE MATCH.

16. DESCRIPTORS	IDENTIFIERS
PHASE SHIFTER	MICROSTRIP PHASE SHIFTER
DESIGN	PIN DIODES
X-BAND	

17a. SECURITY CLASSIFICATION (OF REPORT)	17b. SECURITY CLASSIFICATION (OF PAGE)	17c. SECURITY CLASSIFICATION (OF ABSTRACT)
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