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INVESTIGATION OF InP PROCESSING TECHNIQUES FOR DEVICE APPLICATIONS

University of California

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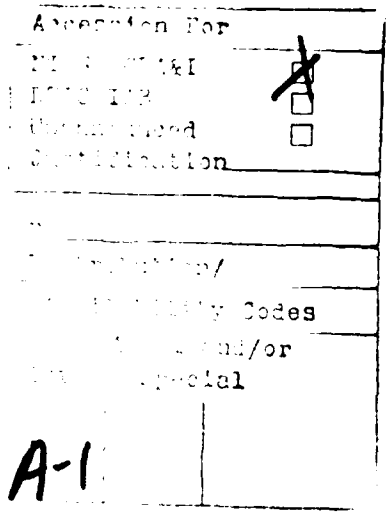
ABSTRACT

This report summarizes the results obtained from an investigation entitled "Investigation of InP Processing Techniques for Device Applications" carried out for the Rome Air Development Center during the period February 20, 1985, to September 30, 1987.

The emphasis of this research program was strongly oriented towards the overall technology of InP for photonic and other device applications. These investigations reported here include such important and diverse subjects as (1) the use of Rutherford backscattering (RBS) to study the solid phase epitaxial growth of InP after amorphization by heavy implant doses, (2) the formation of a novel insulator on InP for passivation, (3) the metallurgy of the "traditional" AuGe/Ni/Au contact for n-type InP, and an analysis of the annealing of such contacts during the short times involved in RTA, (4) the use of electrochemical profiling techniques to determine non-uniform implant distributions into InP, and (5) the diffusion of the deep Fe trap in semi-insulating InP substrates as a result of standard thermal treatments. Significant progress has been made in all of these areas.



I. INTRODUCTION

This report summarizes the results obtained from an investigation entitled "Investigation of InP Processing Techniques for Device Applications" carried out for the Rome Air Development Center during the period February 20, 1985, to September 30, 1987.

Research on InP at the University of California, Santa Barbara, began with an investigation of the use of scanned CW lasers to anneal the damage resulting from implantation into InP, GaAs, and Si. This work was supported by an earlier investigation entitled "Minority Carrier Investigations of Beam-Annealed and Thermally-Annealed Semiconductors" carried out for the Rome Air Development Center during the period October 15, 1981, to October 14, 1984. The emphasis of the early work was on optical characterization (for example, low temperature photoluminescence), since this and related techniques used minority rather than majority-carrier effects and where therefore more sensitive to low levels of residual damage. The large thermal gradients inherent in this annealing technique produced their own defects, however, and the emphasis of this research shifted to the exploitation of short bursts of incoherent light for periods of one to several seconds to anneal implant damage (so-called rapid thermal annealing, or RTA). Electrical characterization of the resulting material was employed in addition to optical techniques such as photoluminescence and Raman scattering.

More recently, however, during the period covered by the investigation which is the subject of this report, the emphasis of this research program has become much more strongly oriented towards the overall technology of InP itself for photonic and other device applications. These investigations include such important and diverse subjects as (1) the use of Rutherford backscattering (RBS) to study the solid phase epitaxial growth of InP after amorphization by heavy implant doses, (2) the formation of a novel insulator on InP for passivation, (3) the metallurgy of the "traditional" AuGe/Ni/Au contact for n-type InP, and an analysis of the annealing of such contacts during the short times involved in RTA, (4) the use of electrochemical profiling techniques to determine non-uniform implant distributions into InP, and (5) the diffusion of the deep Fe trap in semi-insulating InP substrates as a result of standard thermal treatments. Significant progress has been made in all of these areas, as will be described in detail in Section III below.

II. MOTIVATION

The III-V compound semiconductor InP has emerged as an important material for sophisticated device applications, especially those which employ the use photons instead of, or in addition to, electrons for the various control or information-carrying functions needed for modern high-speed microelectronic circuitry. In general the III-V compounds are being seriously considered as alternatives to Si for memory, logic, and transmission-line media for two important reasons: (1) compared with Si, electrons have superior transport properties in these materials because of the smaller effective mass (due to the greater conduction-band curvature), and (2) the efficient generation of visible or near infrared light is possible because the bandgap of most of these compounds is direct rather than indirect (as is the case for Si), so that photonic devices can be made from these materials that are analagous to or compatible with the more conventional electronic devices. In addition to these important intrinsic properties of such binary compounds as GaAs and InP, the existence of a large family of ternary and quaternary III-V compounds that are lattice matched to one of the above binaries makes possible the fabrication of arrays of epitaxial layers that differ in terms of bandgap, refractive index, and electronic properties. As a result, totally new configurations of these materials can be constructed which provide electron and/or photon confinement, and the separation of the carriers from the impurity dopants that provide them in the material, leading to semiconductor lasers and other guided-wave photonic devices, and electronic devices which have enhanced carrier mobility because of this separation of carriers, as, for example, in the so-called HEMT (High Electron Mobility Transistor) or SDHT (Separately Doped Heterostructure Transistor). With the discovery of quantum-size effects in the extremely thin epitaxial layers that can now be fabricated by modern growth techniques, the basic physical properties of the bulk material can be altered almost at will by changing the composition and thickness of these epitaxial layers, and the concepts of "bandgap engineering" and "wave-function engineering" promise almost unlimited flexibility for the device engineer of the future.

Of all of the III-V compounds, GaAs has received by far the most attention. For example, GaAs HEMT devices are currently under development at a number of research laboratories in the United States, Europe and Japan (including the Center for Compound Semiconductors at UCSB), and GaAs lasers are used for many applications. In fact, GaAs and its lattice-matched ternary compound, AlGaAs, are considered to be so important for both electronic and optical devices, that the Japanese have conducted a large-scale cooperative research project on the subject of optoelectronic devices, sponsored by the Ministry for International Trade and Industry (MITI) and involving fourteen of the major electronics companies in Japan. A major feature of this cooperative joint research project was the establishment of the Optoelectronics Joint Research Laboratory (OJL), to which a

subset of nine member companies contributed funds and a research staff of approximately 50 scientists. The focus of OJL was to investigate new materials and processing technologies that would lead to the true integration of optical and electronic devices, so-called optoelectronic integrated circuits (OEICs). This emphasis was chosen for two reasons: (1) The technology of GaAs and its related compounds is considerably more difficult than that of Si, and less effort has been employed to solve the many materials problems involved, so that a sharp focus on this technology was felt to be essential, and (2) by studying generic materials problems rather than specific devices, the participating companies need not disclose sensitive information concerning device fabrication.

The Japanese Optoelectronic Joint Project has been considered to be extremely successful by observers both in the United States and Japan.[1] The Japanese currently dominate the commercial world market in optoelectronic devices, with approximately $0.5 billion in sales, including billions of light-emitting diodes (LEDs), and millions of laser diodes (LDs), Hall elements, and other optical and electronic devices. In addition, significant research progress has been made by OJL in collaboration with its member companies on important GaAs materials problems such as bulk and epitaxial crystal growth, focussed ion beam implantation (FIBI), reactive ion etching (RIE), the physics of the surfaces and interfaces of the relevant compound semiconductors, and the characterization of defects and impurities in these materials that effect their electronic and optical properties. These research accomplishments are most impressive; it is the opinion of this observer, after spending a three-month sabbatical as a Visiting Research Scientist at OJL during the Fall of 1985, that Japanese domination of the optoelectronics market will continue at an even greater level as a result of the major commitment of resources by government and industry to this important field. Even more ominous for the United States is the decision by the Japanese government to continue their commitment to optoelectronics with a second, follow-on cooperative project beginning in 1987, when the current project lifetime expires. Although little definite information is currently available, the present thinking is that the project will have a longer lifetime (probably 10 years), will involve more companies (perhaps 12), and will include an emphasis on InP (and the appropriate ternary and quaternary compounds that are related to InP) as well as GaAs. Because of its larger electronic mobility and lattice-match to compounds (such as InGaAsP) having smaller bandgaps, InP has the potential for even faster electronic devices, and optical sources and detectors that are better matched to state-of-the-art optical fibers. However, the technology for the InP-based materials is much less well-developed than that of GaAs, and considerable effort is needed to make devices based on these materials competitive in performance with GaAs devices. It appears that the Japanese are intent on making the necessary commitment; this report summarizes one aspect of the U.S. effort.

II. SUMMARY OF RECENT RESULTS

A. Rapid Thermal Annealing and Solid Phase Epitaxy of Ion Implanted InP

In a number of papers dealing with ion implantation into InP, there appears to be some disagreement on the necessity of heating the InP substrate when performing high dose implants, i.e. those that would produce amorphous layers if carried out on samples at room temperature or below. Some of the earliest papers suggest that heated implants should be used to achieve maximum electrical activation and mobilities,[2-5] while others report that high activation can be obtained with room temperature implants even when amorphous layers are produced.[5-8]

The motivation for an amorphous ion implant followed by solid phase epitaxy is as follows: It has been known for some time that in silicon this technique results in activation of the implanted dopant at significantly lower temperature (<600°C) than those required to remove implant defects when the target is not amorphized.[9] The lower temperature required for the anneal and activation of an amorphizing implant would be attractive for compound semiconductor devices from the stand point of minimizing material decomposition as well as reducing impurity redistribution.

We have evaluated the annealing behavior of amorphous and disordered layers using ion channeling. The samples have various amorphized thicknesses as a result of implantation temperatures of 77K, room temperature, and 200°C followed by different annealing processes (both furnace annealing and rapid thermal annealing). In addition, we have made electrical measurements on samples implanted at room temperature and 180°C to provide some insight into the effect of residual damage on electrical activation.

The channeling results for samples implanted at room temperature and 77K followed by furnace annealing at 750°C for 15 min. are summarized in Fig. 1 where the thickness of the residual disorder following annealing is plotted against the thickness of the amorphous layer in the as-implanted samples. We show that the post-anneal residual disorder of amorphous layers thicker than 2000Å is linearly dependent on the initial amorphous layer thickness. The data for both room temperature and 77K implants are in agreement with results reported before by Woodhouse for Se[10] and Auvray for Cr and Se.[11]

The behavior of the disordered layer with an amorphous thickness less than 2000Å is different, as we can see from Fig. 2 and Fig. 3. In Fig. 2 we show the annealing behavior of 10^{14} and $5x10^{13}$ Si ions/cm^2 implanted at room temperature following 15 min. at 750°C. The samples do not completely reorder but remain relatively free of damage.

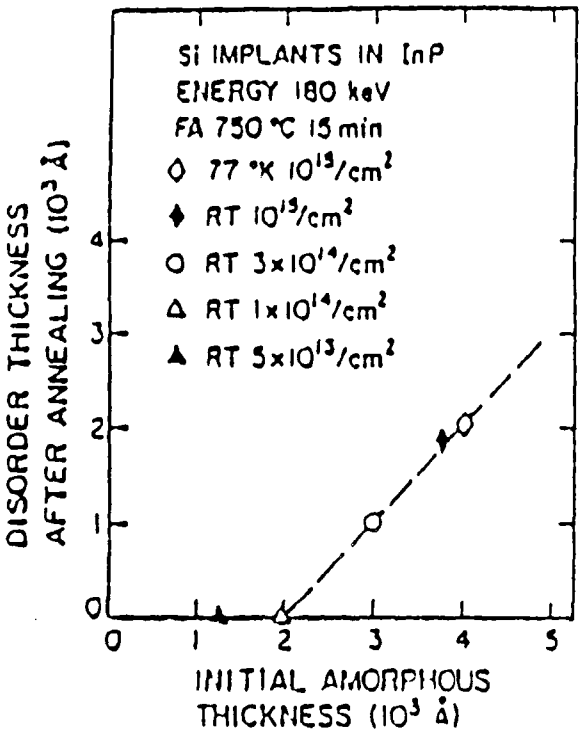


Fig. 1. Residual damage thickness following FA annealing at 750°C vs. initial amorphous thickness for room temperature and 77K Si implanted InP.

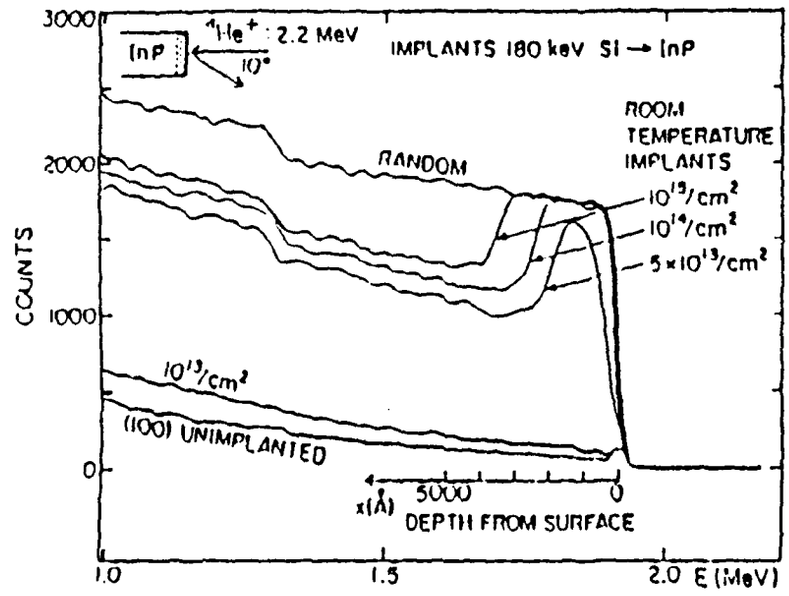


Fig. 2. Aligned and random backscattering spectra for unannealed InP implanted at room temperature with 180 keV, 10^{14} and 5×10^{13} Si/cm^2, following FA at 750°C 15 min.

In Fig. 3 we show the annealing results of $5x10^{13}$ Si ions implanted at room temperature at 170 keV followed by 60 min. furnace annealing at 250°C. There is epitaxial regrowth from crystalline InP both underlying and overlying the amorphous layer and leaving a small residual disorder peak. This residual peak is totally removed by higher temperature annealing. The regrowth nearly stopped following 60 min. annealing at 250°C. The mechanism which prevents complete epitaxial regrowth for layers over 2000Å thick is not understood.

To circumvent the formation of an amorphous layer and thus the residual disorder on subsequent annealing, elevated temperature (>150°C) implants offer a possible alternative.[12] Because of the increased mobility of point defects at such temperatures, the dynamic annealing of an individual cascade region and amorphous or damage zone is greatly enhanced, inhibiting the formation of an amorphous layer. Fig. 4 shows that there is only a small difference in crystalline quality between unimplanted and implanted samples with doses of $3.3x10^{14}$ and 10^{15} Si ions/cm^2 implanted at 200°C. Fig. 5 also shows the effect of the rapid thermal annealing at 850°C for 20 seconds on the implanted layer. The disorder is reduced to a level comparable to that of an unimplanted wafer. Furnace annealing, on the other hand, is unable to anneal the small amount of residual damage that is left after hot implant.

Thus, we have shown that ion implanted amorphous InP can be regrown at temperatures below 300°C, provided that the maximum epitaxial regrowth thickness is under 2000Å. For thicker amorphous layers, near-surface residual disorder remains after furnace annealing, whose thickness is linearly dependent on the initial thickness of the amorphous layer. For implantation at 175°-200°C self annealing reduces crystalline disorder to a low level even at high doses. Rapid thermal annealing following hot implants further reduces the damage level to that of an unimplanted wafer.

Electrical measurments were performed over a wide range of implantation conditions. For the electrical parameters used in this investigation implantation at elevated temperature appears to offer an advantage for both furnace and rapid thermal annealing techniques. The results of rapid thermal annealing are comparable to the best value obtained with the conventional thermal technique. Implantation at elevated temperature offers the possibility of using low temperature furnace annealing, about 600°C, to obtain high electrical activation; this can not be obtained following room temperature implants, even in the case of complete regrowth of the damage layer.

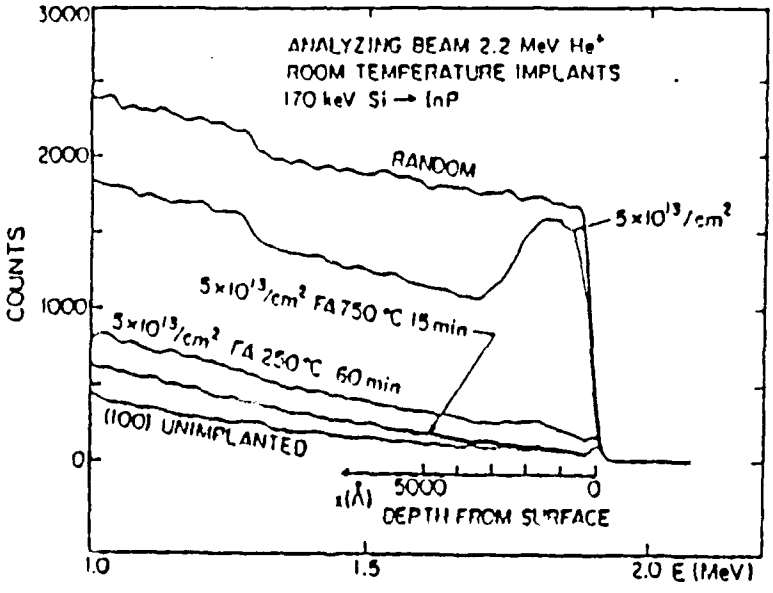


Fig. 3. Aligned (100) and random backscattering spectra of unannealed InP implanted at room temperature with 170 keV, 5x10^{13} Si/cm^2, following FA at 250°C 1 hr. and 750°C 15 min.

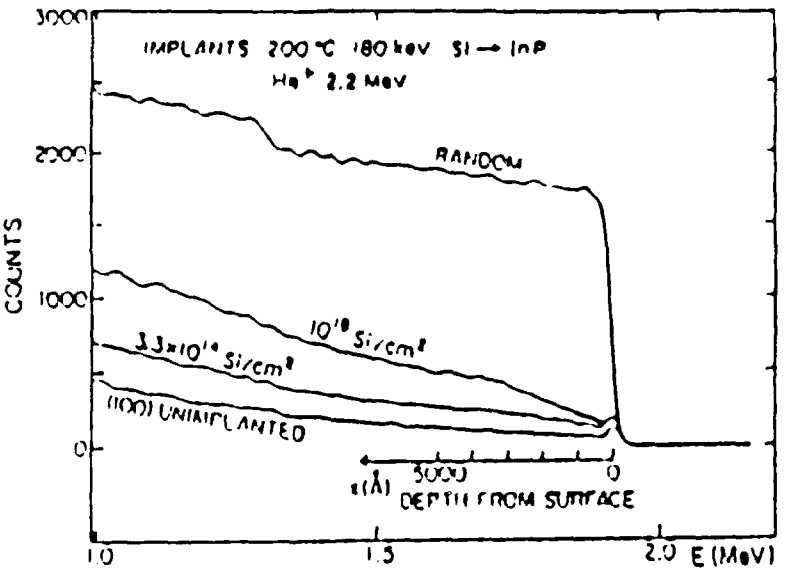


Fig. 4. Aligned (100) and random backscattering spectra for InP implanted at 200°C with 3.3×10^{14} and 10^{15} Si/cm^2.

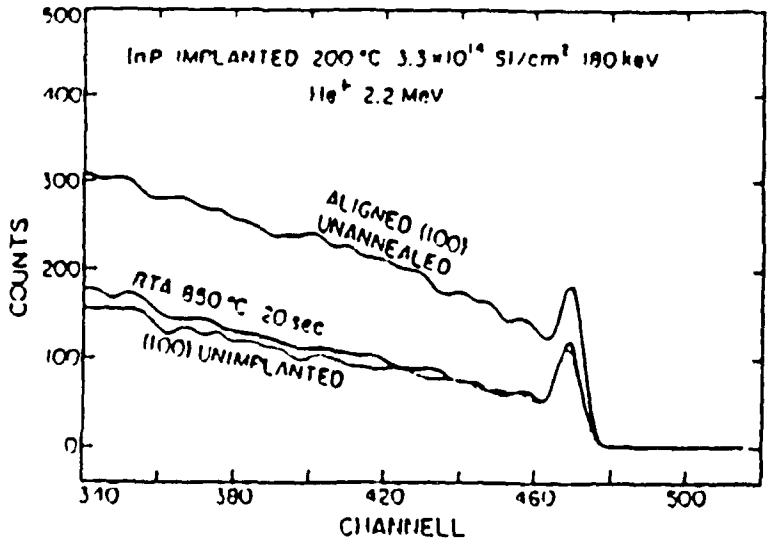


Fig. 5. Aligned (100) backscattering spectra for InP implanted at 200°C with 180 keV, 3.3×10^{14} Si/cm^2, before and following RTA at 850°C 20 sec.

B . Electrochemical Profiling of Ion-Implanted InP

The determination of the carrier concentration profile obtained after ion implantation into compound semiconductors followed by annealing is often done by a series of differential Hall measurements, an extremely tedious and difficult process. Another difficulty encountered with InP and related compounds is the formation of high-quality Schottky barriers. This problem can be avoided, however, by employing an electrolytic liquid barrier, thus allowing conventional C-V analysis to be performed. A useful extension of this approach is to take advantage of the electrolyte as a means of controlled dissolution of the specimen in situ. This allows continuous profiling to virtually any depth, as the electrolytic solvent continuously removes material at a well-defined rate. Thus, the usual doping-dependent limitations due to reverse breakdown are avoided.

Electrochemical C-V profiling has been widely used for the measurement of doping properties in GaAs for a number of years. The principal use of this technique has been to profile the doping of multilayer epitaxial structures. However, the use of electrochemical C-V techniques to profile ion implanted distributions is still very limited.[13,14] In this work we report the successful application of automatic electrochemical profiling to the measurement of ion-implanted InP. The factors which influence the accuracy and reproducibility of carrier profiling in implanted material by means of electrolyte Schottky barrier C-V measurements are critically examined. Before attempting to measure carrier profiles, the basic characteristics of the InP/HCl barrier were explored for uniformly-doped material.

The criteria governing the choice of electrolyte for an electro- chemical profiling system are as follows: the C-V characteristics of the semiconductor-electrolyte interface must approximate a Schottky barrier; i.e effects due to the electrolyte, or surface states on the capacitance should be negligible. We found that this condition could be satisfied for more than three orders of magnitude in carrier concentration. The carrier concentration obtained from the slope of the $1/C^2$ data was found to be slightly higher (20-50%) than that obtained by both van der Pauw Hall measurements or the two-frequency C-V analysis.

An example of the special features of the electrochemical profiling technique applied to an ion-implanted and annealed InP sample is shown in Fig. 6 and 7. Fig. 6 shows the electrically active carrier distribution for undoped material, for material doped to, $1.2*10^{16}$ cm^{-3}, and for undoped InP implanted with $3.3*10^{14}$ Si/cm^2 followed by rapid thermal annealing at 850°C for various times. Fig. 7 shows the profiles of the carrier concentration vs. depth obtained by electrochemical profiling for samples implanted with 10^{13} and $3*10^{14}$ Si ions/cm^2 at room temperature and 200°C, followed by furnace annealing for 15 minutes at 750°C.

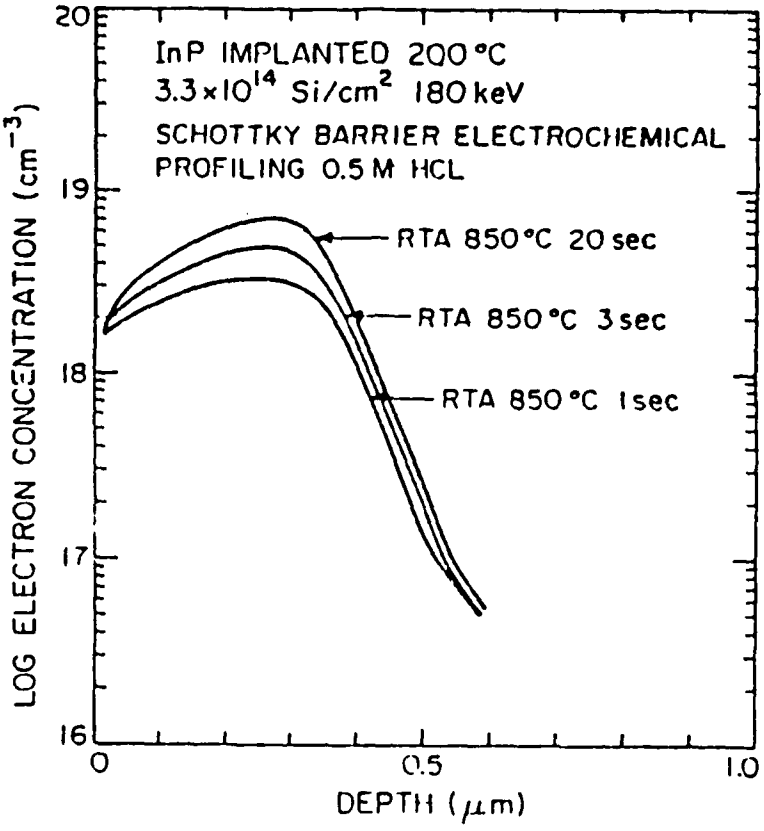


Fig. 6. Electron carrier concentration profiles for InP implanted at 200°C with 180 keV Si ions to a dose of 3.3*10[14] cm[2] followed by RTA at 850°C for 1, 3, and 20 seconds.

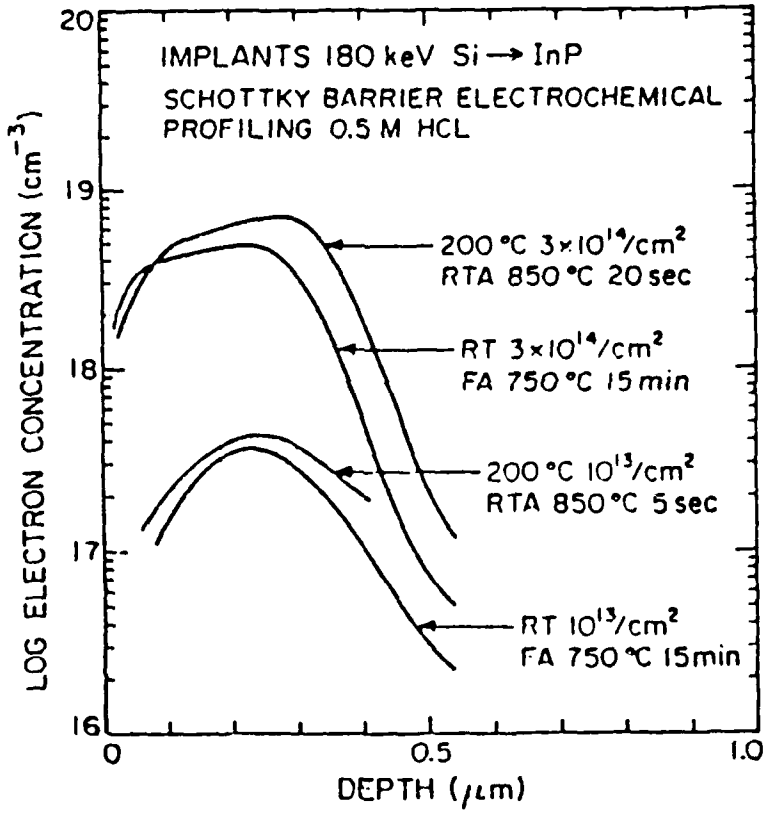


Fig. 7. Electron concentration profiles for InP implanted at RT with 180 keV Si ions to a dose of 10^{13} and $3*10^{14}$ cm^2 followed by FA at 750 °C for 15 minutes, and for implantation at 200°C with the same doses followed by RTA at 850°C for 5 seconds . room temperature implants and rapid thermal annealing for hot implants.

The accuracies of these carrier concentration profiles obtained from measurements of Mott-Schottky capacitances are criticaly dependent on the area of the semiconductor contact and its edge definition. The effective barrier area must be known with extremely good accuracy. The area is defined by a plastic sealing ring, mounted on the electrochemical cell of the Profiler Plotter.

As n-type material etches only under illumination, there are two different areas that we have to include in our calculation. A_c is the central area which was illuminated, and is thus the only region within which InP dissolved. A_e is the excess wetted area which arises from simple shadowing of the illumination, due to slight rounding of the edge profile of the sealing ring. The effect of the excess wetted area on carrier concentration measurements was analyzed by Ambridge *at el.*[15] for the case of n-type GaAs; the commercial Polaron software is based on this work. The areas A_c and A_e must be measured accurately and be included in the input data before profiling.

By first measuring the capacitance per unit area on the sample surface before etching, the program calculates the carrier concentration point-by-point as the sample is etched. This is done by subtracting the excess capacitance contributed by A_e (which is constant) from each capacitance measurement made during the etching and profiling process, and then applying the normal technique for extracting the carrier concentration. The result of this procedure, in the case of a small error in determining A_e, is that the relative error is a function of depth, because the ion-implanted profile is not a constant. Since the capacitance per unit area is high at the sample surface following implantation and activation of the dopant, the relative error in carrier concentration could be very large at the end of the implanted profile, where the concentration is 2 to 3 orders of magnitude lower than the surface carrier concentration. We investigated the effect of errors in A_e on carrier concentration profiles by using an undoped sample with a background concentration of $1.2*10^{16}$ cm^{-3} implanted at 200°C with a dose of $3.3*10^{14}$ Si ions/cm^2 at 180 keV, followed by rapid thermal annealing at 850°C for 5 seconds. Fig. 8 shows the results of three different profile measurements on the same sample, using a fixed value for the measured etched area ($A_c = 0.086$ cm^2) and three different values for A_e, the excess wetted area. (The actual area is about 0.005 cm^2). From these results it is clear that errors within the limit of determination of A_e (0.001 to 0.002 cm^2) could contribute very large errors for the lower concentration side of the implanted layer. Thus, in order to have reproducible results, it was necessary to measure the etched area very accurately, and to use several standard samples for a better determination of A_e. Also, in each profile measurement, we required that the concentration at the end of the implanted layer profile (1 μm) be at least equal to the background concentration.

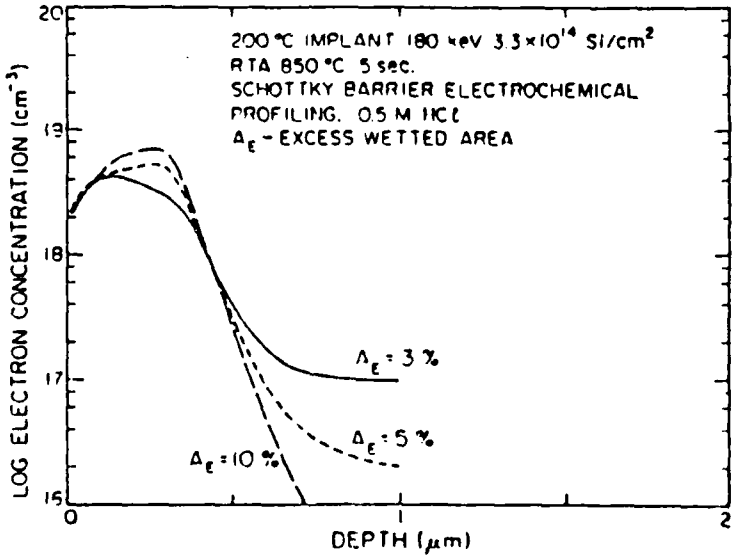


Fig. 8. Electron concentration profiles for InP implanted at 200°C with 180 keV Si ions to a dose of $3.3*10^{14}$ cm^2 followed by RTA at 850°C for 5 seconds. Calculation uses constant value of A_c and assumed values of A_e (calculated as a pecentage of the total wetted area). Bulk background concentration is n=10^{16} cm^{-3}.

Another source of error is the fact that the reverse anodic current is a very sensitive parameter to the residual damage remaining following ion implantation and a low level of electrical activation. In this case there is no difference between the anodic I-V characteristic of a damaged implanted layer and an undamaged sample having a high carrier concentration, such as 10^{19} cm^{-3}. Illumination does not affect the reverse current, and there is no current saturation. The main difference between samples with a high carrier concentration and those with residual damage is the measured conductance per unit area, which, in the case of the damaged sample, has a higher minimum and a narrower low-conductance voltage "window". Thus, dark leakage current affects the determination of the carrier concentration.

The exact mechanism by which an anodic current is induced by unannealed damage following ion implantation is not clear. It is known that for Si and the wider bandgap III-V semiconductors, generation current tends to dominate the n-type anodic behavior, and defects are principle sites for carrier generation. The increasing amount of anodic current following implantation can be attributed to a better overlap of filled electrolyte states with unfilled semiconductor hole states. It appears, therefore, that in the case of ion-implantation profiling, the advantage of using an electrolyte that is suitable for both dissolution and barrier formation is offset by the disadvantage that a small amount of residual damage has a large effect on the transport properties of the barrier. This effect has been used by Huller *et al.*[14] to qualitatively profile the damage in ion-implanted Si.

Finally, we have found that deep levels induced by the damage at a depth greater than the range of the implanted ions can cause extraneous peaks on the G-V and C-V curves, and by using the electrochemical profiling technique we can therefore qualitatively profile the concentration of deep levels.

C. Rapid Thermal Alloyed Ohmic Contact on InP

Ohmic contacts are Schottky barriers through which majority carriers can tunnel, provided the free carrier concentration at the metal-semiconductor interface can be made sufficiently high to reduce the barrier width to a few tenths of angstroms. The conventional technique of forming a high surface concentration of free carriers on n type material is to deposit a donor type metal plus Au, after which the InP-metal combination is heated above the Au-metal eutectic temperature in order to melt the films. Upon cooling the donor metal is incorporated into the InP, forming the ohmic contact. The usual ohmic contact to n-type InP with low specific contact resistance is an alloyed Au:Sn[16-19] or Au:Ge[19-21] contact.

Au:Ge was originally chosen for its low eutectic melting temperature (360°C). It is believed that Indium out-diffuses into the Au, and that the Ge, which acts as an amphoteric dopant in InP, settles onto In vacancies, thus becoming a donor. The alloyed contact so formed has the disadvantage of having a bad surface morphology, bad edge definition, and uneven penetration depth. As device dimensions decrease the inhomogeneity of the alloyed contact will become unacceptable.

Specific contact resistance in the low 10^{-6} Ω cm^2 has been reported on n-type InP.[19-21] However, the detailed alloying behavior of this contact is still not well understood, because the alloying reactions that occur at the metal-InP interface are very complicated. There are several investigations dealing with electrical results (e.g., contact resistivity measurements) and morphology, but few dealing with the structural and metallurgical aspects.[18,20] A high rate of heating and cooling is felt to be important for the production of a contact of low resistivity. The reduction of the heating time could diminish (a) the loss of the volatile component of InP, (b) The intermixing of metal and semiconductor, and (c) phase segregation and grain size. Moreover, short, controlled heating times allow the evaluation of the different reactions that occur on the surface.

In this study we report the results of a systematic study of ohmic contact formation to InP by metal deposition and halogen lamp annealing. Alloying temperatures between 300 and 500° C and time cycles between 2 and 10 seconds were investigated. Rutherford backscattering (RBS) was used to trace the distribution of metal layers through different stages of alloying. By monitoring the interface reactions, it was possible to establish a correlation between interface structure and contact resistance.

Fig. 9 shows random RBS energy spectra of 2.7 MeV He ions from the as-deposited sample. The Ge and Ni peaks are superimposed on the In bulk spectra in reverse order because of the difference in mass between the elements. After heat treatment at 405° C for 2 sec, RBS shows that the Ge diffuses toward the surface into the Ni layer, and part of the Ni diffuses in the opposite direction, through the AuGe layer to the InP interface. Out-diffusion of mostly In and some of the P also occurs. Some of the Au also begins to diffuse into the InP. The Ge out-diffusion and Ni in-diffusion begin at a temperature of about 350° C. After annealing at 415° C for 5 sec, the Ge does not change its position, (although the peak tends to broaden somehwhat), but the majority of the Ni diffuses to the InP interface . The In diffuses through the AuGe and Ni barrier into the surface Au layer, and the P edge disappears entirely. At higher alloying temperature, 440°C for 5 sec, the Ge diffuses back into the InP interface, more Au diffuses into the InP, and the In peak is now well-defined, at an energy that corresponds to In on the surface of the outer Au layer. Similar behaviour of metal intermixing can be seen following treatment in the graphite strip heater.

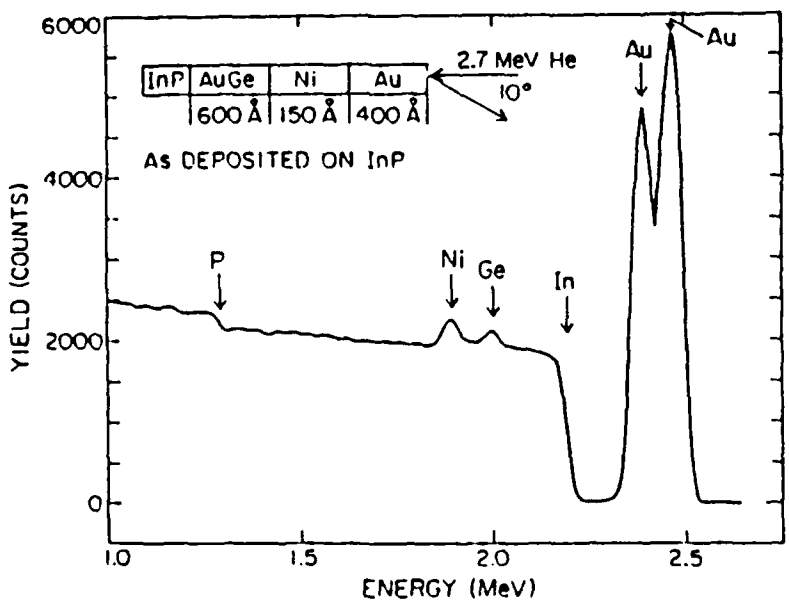


Fig. 9. 2.7 MeV ^{4}He random backscattering spectra of AuGe/Ni/Au layers deposited on InP.

Similar results for GaAs have been described by Kuan *et al.* [22] Still higher alloying temperature or longer time caused further diffusion of Au into the interface, and out-diffusion of In and P.

The specific contact resistivity measured from the average of different Kelvin structures following rapid thermal alloy at different temperatures for 2 seconds is shown in Fig. 10. The resistivity of AuGe/Ni/Au contacts is very sensitive to temperature. For samples heat treated at 330° C the contact is nonohmic. The contact becomes ohmic but the resistance is still high for samples alloyed at temperatures at and above the eutectic temperature, 360°C. However, as is clear from Fig. 10, higher temperatures in the range of 430 to 450°C produce the lowest contact resistivity , about $2*10^{-7}$ Ω-cm^2. The contact resistivity increases for still higher alloying temperature. For comparison, Fig. 11 shows resistivity measurements using the TLM structure, for a sample alloyed at the optimum conditions of 430°C for 2 seconds. The pad-to-pad resistance was measured using a four-probe technique, and the distance between pads was measured for each sample. The specific contact resistance was calculated using the Transmission Line Model (TLM) model. From this model we can also extract the sheet resistance of the Si implanted channel, determined to be 104 $\Omega/^{\cdot}$ in the case shown, and the specific contact resistance was $3.7*10^{-7}$ W cm^2. The optimized specific contact resistance using a graphite strip heater was also $4*10^{-7}\Omega$-cm^2 for heat treatment at 420° C for 10 seconds.

In summary, the major reactions at the AuGe/Ni/Au contact interface observed in this work are as follows: At low temperature, 320 - 405°C, Ge out diffuses into the Ni layer, possibly creating NiGe, as described in ref.[20,22] Ni in-diffuses to the semiconductor interface. Also, out-diffusion of In and P toward the surface is observed, with In being the faster diffusing species. Au penetration into the InP bulk is observed as well. At higher temperature, 430-440°C, the diffusion of Ge from the NiGe phase back to the semiconductor interface is found to be the major change that brings the contact resistance from values higher then $5*10^{-6}$ Ω-cm^2 down to a minimum of $2*10^{-7}\Omega$-cm^2. The optimized amount of In that out-diffused from the semiconductor interface could also influence these results. At still higher temperature, 450-500°C, and/or longer anneal time, the contact resistance again increases. This increase is correlated with Au diffusion into the semiconductor crystal, and In out-diffusion.

It is generally believed that a low resistance ohmic contact to n-type InP is achieved by the presence of a heavily-doped n$^+$ layer at the metal/ InP interface, where carrier transport occurs mainly through tunneling. Following this model, the relatively high resistivity exhibited after low temperature treatment, 340-400°C, is probably due to the lack of this layer, since most of the doping element Ge is trapped in the Ni layer to which it has

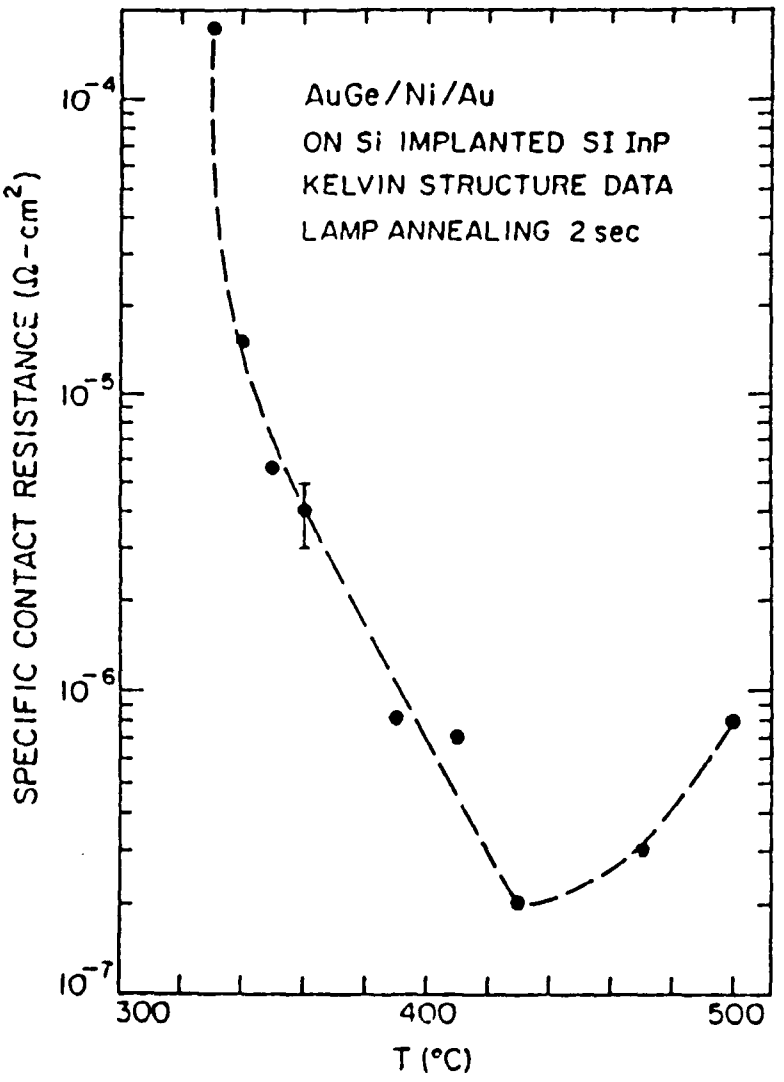


Fig. 10. Variation of measured specific contact resistance with peak lamp-annealing temperature.

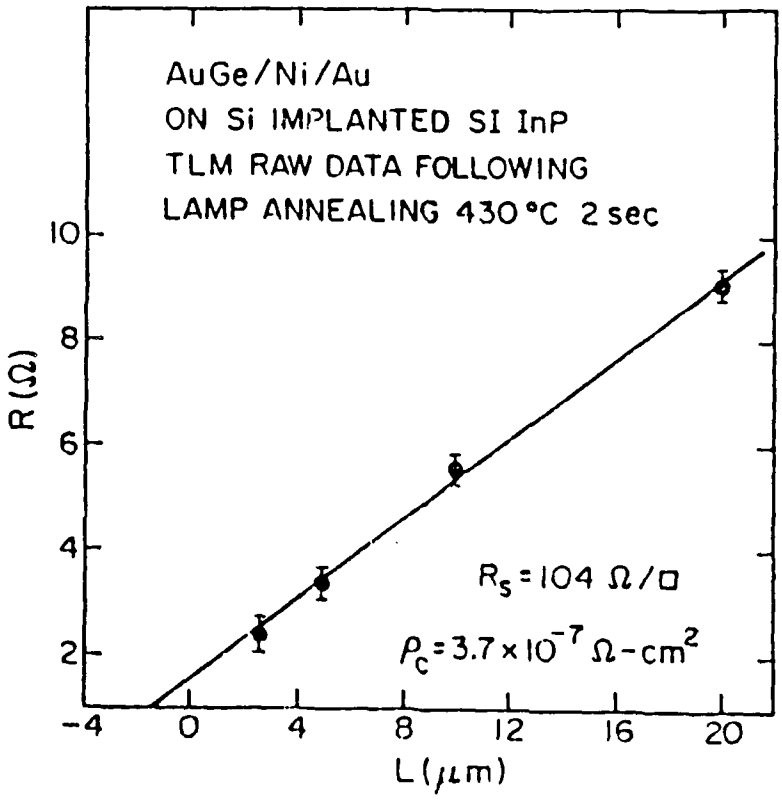


Fig. 11. TLM data showing resistance between pads vs. distance between pads, for RTA at 430°C for 2 sec.

diffused, and which is separated from the InP substrate by ≈1000 Å thick layer of gold which no longer contains appreciable Ge.

If contacts are alloyed above 450° C, or for a time longer than about 20 seconds, continuous island growth is found to occur on the outer surface, as can be seen by electron or optical microscopy. The RBS spectra give ambiguous results for the analysis of intermixing between the metals and the InP interface. The decreasing contact resistivity could result from the dominance of Au/InP areas over the InP interface. The various reactions of Au with InP have been described in detail.[21] It appears that for InP, just as in the case of GaAs[22] the alloyed ohmic contacts consist of "good" contact areas where the Ge doped the InP and "poor" contact areas with Au at the InP interface. The measured contact resistance is therefore sensitive to the size, distribution and ratio of these two areas.

As has been shown in this work, the interactions that take place on the surface are very fast and are sensitive to temperature. Thermal processing for a very short time enables us to optimize the process by correlating electrical measurements with the structure, and to probe, at least partially, the different reactions that occur during the alloying process.

D. The use of Hg-Sensitized PHOTOX SiO_2 as a Dielectric on InP

This work investigates the use of a new dielectric on InP; PHOTOX is a low temperature (100°C) chemical-vapor-deposited film produced by reacting silane with oxygen. The PHOTOX process uses Hg vapor excited by exposure to UV radiation which catalyzes decomposition of N_2O to produce oxygen. The interface has been characterized using MIS capacitors. Good results have been obtained in terms of high and low frequency capacitance, density of surface states, and flat band condition.

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IV. PUBLICATIONS RESULTING FROM THIS CONTRACT

1. Correlation of RBS and Electrical Measurements on Si Implanted InP Following Rapid Thermal and Furnace Annealing.
   G. Bahir, J.L. Merz, J.R. Abelson, and T.W., Sigmon, Ion Beam Processes in Advanced Electronic Materials and Device Technology, edited by B.R. Appleton, F.H. Eisen, and T.W. Sigmon, Materials Research Society Symposium Proceedings, San Francisco, CA, April 1985, (Materials Research Society, Pittsburgh, PA, 1985), 297-302.

2. Rapid Thermal Annealing and Solid State Epitaxy of Ion Implanted InP.
   G. Bahir, J.L. Merz, J.R. Abelson and T.W. Sigmon, Proc. of SPIE - The International Society for Optical Engineering, Vol. 623, "Advanced Processing and Characterization of Semiconductors III" (ed by D.K. Sadana and M.I. Current), Los Angeles, CA, January 22-24, 1986; pp.149-156.

3. Regrowth of Amorphized InP.
   G. Bahir, J.L. Merz, J.R. Abelson and T.W. Sigmon, Gallium Arsenide and Related Compounds 1986, edited by W.T. Lindley, Institute of Physics Conference Series Number 83, Las Vegas, Nevada, September 28 to October 1, 1986 (Institute of Physics, Bristol, England, 1987); pages 283-288.

4. Effect of Si Implantation and Rapid Thermal Annealing on GaAs/AlGaAs Superlattice Disordering.
   J.D. Flood, G. Bahir, J.L. Merz, J. Kobayashi, T. Fukunaga, K. Ishida, and H. Nakashima, Interfaces, Superlattices, and Thin Films, edited by J.D. Dow and I.K. Schuller, Materials Research Society Symposium Proceedings, Vol. 77, Boston, Mass., December 1-5, 1986 (Materials Research Society, Pittsburgh, PA, 1987).

5. The Effect of Implantation and Annealing Conditions on the Fe Profile in Semi-insulating InP.
   G. Bahir, J.L. Merz, J.R. Abelson, T.W. Sigmon, Beam-Solid Interactions and Transient Processes, edited by S.T. Picraux, M.O. Thompson, and J.S. Williams, Materials Research Society Symposium Proceedings, Vol 74, Boston, Mass., December 1-5, 1986, (Materials Research Society, Pittsburgh, PA, 1987).

6. The Effect of Rapid Thermal Annealing for the Compositional Disordering of Si-Implanted AlGaAs/GaAs Superlattices.
   J. Kobayashi, T. Fukunaga, K. Ishida, H. Nakashima, J.D. Flood, G. Bahir, and J.L. Merz, Appl.Phys. Lett. 50, 519-521 (2 March 1987).

7. Electrochemical Profiling of Ion-Implanted InP.
G. Bahir, J.L. Merz, J.R. Abelson, and T.W. Sigmon, J. Electrochem. Soc. 134, 2187-2193 (September 1987).

8. Rapid Thermal Alloyed Contact On InP.
G. Bahir, J.L. Merz, J.R. Abelson, and T.W. Sigmon, J. Electronic Mat. 16-4 (1987).

9. Correlation Between Carrier and Atomic Distribution in Si-Implanted Semi-Insulating InP.
G. Bahir and J.L. Merz, Gallium Arsenide and Related Compounds 1987, Institute of Physics Conference Series, No. 91, Edited by A. Christou and H.S. Rupprecht, Proceedings of the 14th Int. Symp. on GaAs and Related Compounds, Heraklion, Crete, Greece; September 28 to October 1, 1987 (Institute of Physics, Bristol, England, 1988); pages 467-470.

10. Iron Redistribution and Compensation Mechanisms in Si-implanted InP
G. Bahir, J.L. Merz, J.R. Abelson and T.W. Sigmon, J. Appl. Phys., (to be published).

V. TALKS AND PRESENTATIONS RESULTING FROM THIS CONTRACT

1. "Correlation of Rutherford Backscattering and Electrical Measurements on Si-Implanted InP Following Rapid Thermal and Furnace Annealing"; G. Bahir, J.L. Merz, J.R. Abelson, and T.W. Sigmon, Materials Research Society Spring Meeting, San Francisco, CA, April 15-18, 1985.

2. "Electrochemical Carrier Concentration of Ion-Implanted InP"; G. Bahir, J.L. Merz, J. Abelson, and T.W. Sigmon, Meeting of the Electrochemical Society, Toronto, Canada, May 12-17, 1985.

3. "The Electrical Properties of Hg Sensitized PHOTOX SiO_2: Interface," G. Bahir and J.L. Merz, Meeting of the Electrochemical Society, Las Vegas, NV, Oct. 13-18, 1985.

4. "Rapid Thermal Annealing and Solid Phase Epitaxy of Ion Implanted InP", G. Bahir, J.L. Merz, J.R. Abelson and T.W. Sigmon, O-E/LASE symposium on Opto-Electronics and Laser Applications, Los Angeles, CA, January 23, 1986 (Invited).

5. "Rapid Thermal Alloyed Ohmic Contact on InP", G. Bahir, J.L. Merz, J.R. Abelson, and T.W. Sigmon, Electronic Materials Conference, University of Massachusetts, Amherst, MA, June 25-27, 1986.

6. "Regrowth of Amorphized InP"; G. Bahir, J.L. Merz, J.R. Ablelson, and T.W. Sigmon, 13th International Symposium on GaAs and Related Compounds, Las Vegas, Nevada, September 28-October 1, 1986.

7. "The Effect of Implantation and Annealing Conditions on the Fe Profile in Semi-Insulating InP"; G. Bahir, J.L. Merz, J.R. Abelson, and T.W. Sigmon, Annual Meeting of the Electrochemical Society, San Diego, CA, October 21-23, 1986.

8. "Effect of Si Implantation and Rapid Thermal Annealing on GaAs/AlGaAs Superlattice Disordering"; J.D. Flood, G. Bahir, J.L. Merz, J. Kobayashi, T. Fukunaga, K. Ishida, and H. Nakashima, Fall Meeting of the Materials Research Society, Boston, MA, December 1-4, 1986.

9. "The Effect of Implantation and Annealing Conditions on the Fe Profile in Semi-Insulating InP"; G. Bahir, J.L. Merz, J.R. Abelson, and T.W. Sigmon, Fall Meeting of the Materials Research Society, Boston, MA, December 1-4, 1986.

10. "Low Temperature Passivation of InP"; G. Bahir, M.H. Jin, and J.L. Merz, Electronic Materials Conference, Santa Barbara, CA, June 24-26, 1987.

11. "Correlation between Carrier Distribution and Atomic Distribution in Si-Implanted Semi-Insulating InP"; Gad Bahir and J.L. Merz, 14th International Symposium on GaAs and Related Compounds, Crete, Greece, September 28 to October 1, 1987.

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