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RADC-TR-90-181
In-House Report
July 1990



AD-A226 746

SYSTOLIC EMULATOR EXPERIMENTATION

Richard N. Smith and Michael W. Fenton

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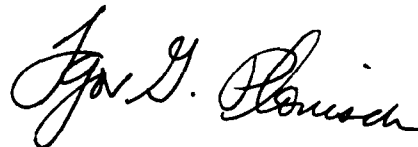
LAURENCE W. DOUBLEDAY, Chief
Communications Transmission Division
Directorate of Communications

APPROVED:



JOHN A. GRANIERO
Technical Director
Directorate of Communications

FOR THE COMMANDER:



IGOR C. PLONISCH
Directorate of Plans & Programs

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REPORT DOCUMENTATION PAGE			Form Approved OPM No. 0704-0188	
Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources gathering and maintaining the data needed, and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing the burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Information and Regulatory Affairs, Office of Management and Budget, Washington, DC 20503.				
1. AGENCY USE ONLY (Leave blank)		2. REPORT DATE July 1990		3. REPORT TYPE AND DATES COVERED In-House Apr 87 - Apr 90
4. TITLE AND SUBTITLE SYSTOLIC EMULATOR EXPERIMENTATION			5. FUNDING NUMBERS PE - 62702F PR - 4519 TA - 42 WU - 63	
6. AUTHOR(S) Richard N. Smith and Michael W. Fenton				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Rome Air Development Center (DCCD) Griffiss AFB NY 13441-5700			8. PERFORMING ORGANIZATION REPORT NUMBER RADC-TR-90-181	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) Rome Air Development Center (DCCD) Griffiss AFB NY 13441-5700			10. SPONSORING/MONITORING AGENCY REPORT NUMBER	
11. SUPPLEMENTARY NOTES RADC Project Engineer: Richard N. Smith/DCCD/(315) 330-3224				
12a. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution unlimited.			12b. DISTRIBUTION CODE	
13. ABSTRACT (Maximum 200 words) Adaptive spatial filtering or adaptive antenna nulling techniques have been used to remove or eliminate directional electromagnetic interferences or unwanted signals from getting into radio receivers. This signal processing technique has been studied for many years. Many systems have been proposed, some have been built and a few have been fielded. High speed parallel processors are beginning to show promise in providing real-time solutions for meeting the processing requirements needed for space applications. One type of high speed parallel processor architecture is called systolic. The name arises from the way the data pulses through the cell-like structure of the processor in a prescribed pipelined manner. Effective implementation of adaptive signal processing techniques using systolic array processors, especially, required careful matching between the algorithm to be performed and the processor architecture. This				
14. SUBJECT TERMS Systolic, Processor, Parallel Emulation, Simulation			15. NUMBER OF PAGES 134	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT UNCLASSIFIED	18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	20. LIMITATION OF ABSTRACT UL	

Block 13 (Cont'd)

process of matching algorithm and architecture can be facilitated by computer emulation.

This report will describe the process of designing, emulating, and testing two adaptive antenna nulling processors. The processors were designed to be part of a three-element adaptive antenna sidelobe canceller system. Using this system, the signals to two elements are appropriately weighted, and their sum is then subtracted from the reference signal to remove interference. After the processors were designed and emulated, they were tested using artificial data and simulated data obtained from an emulated three-element antenna array system. The performance of each processor was then evaluated using residue and antenna gain pattern plots.

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I. Introduction

This work was done under Task 2 of the "Communications Adaptive Array Processor Evaluation" In-House project #45194263. The objective of this task was to employ two computer software tools to explore the interrelationships between adaptive antenna algorithms and systolic processors. The two software tools, EMUL and GADAR[1], were delivered by the Hazeltine Corp. under the "Systolic Array Processor Brassboard" project #45194248. The EMUL software tool is designed for the emulation of various systolic array processor architectures. Each processor architecture is designed to specifically implement a single algorithm such that the algorithm may be processed efficiently. The GADAR software tool allows the generation of simulated signals for the purpose of testing processor performance. Due to the lack of comprehensive documentation of these tools, this report may also serve as a guide to the use of EMUL and GADAR.

Adaptive spatial filtering or adaptive antenna nulling techniques have been used to remove or eliminate directional electromagnetic interferences or unwanted signals from getting into radio receivers. This signal processing technique has been studied for many years. Many systems have been proposed, some have been built and a few have been fielded.

High speed parallel processors are beginning to show promise in providing real time solutions for meeting the

processing requirements needed for space applications. One type of high speed parallel processor architecture is called systolic. The name arises from the way the data pulses through the cell-like structure of the processor in a prescribed pipelined manner. Effective implementation of adaptive signal processing techniques using systolic array processors, especially, requires careful matching between the algorithm to be performed and the processor architecture. This process of matching algorithm and architecture can be facilitated by computer emulation.

This report will describe the process of designing, emulating and testing two adaptive antenna nulling processors. The processors were designed to be part of a three-element adaptive antenna sidelobe canceller system [2] (see Figure 1). Using this system, the signals to two elements are appropriately weighted, and their sum is then subtracted from the reference signal to remove interference. After the processors were designed and emulated, they were tested using artificial data and simulated data obtained from an emulated three element antenna array system. The performance of each processor was then evaluated using residue and antenna gain pattern plots.

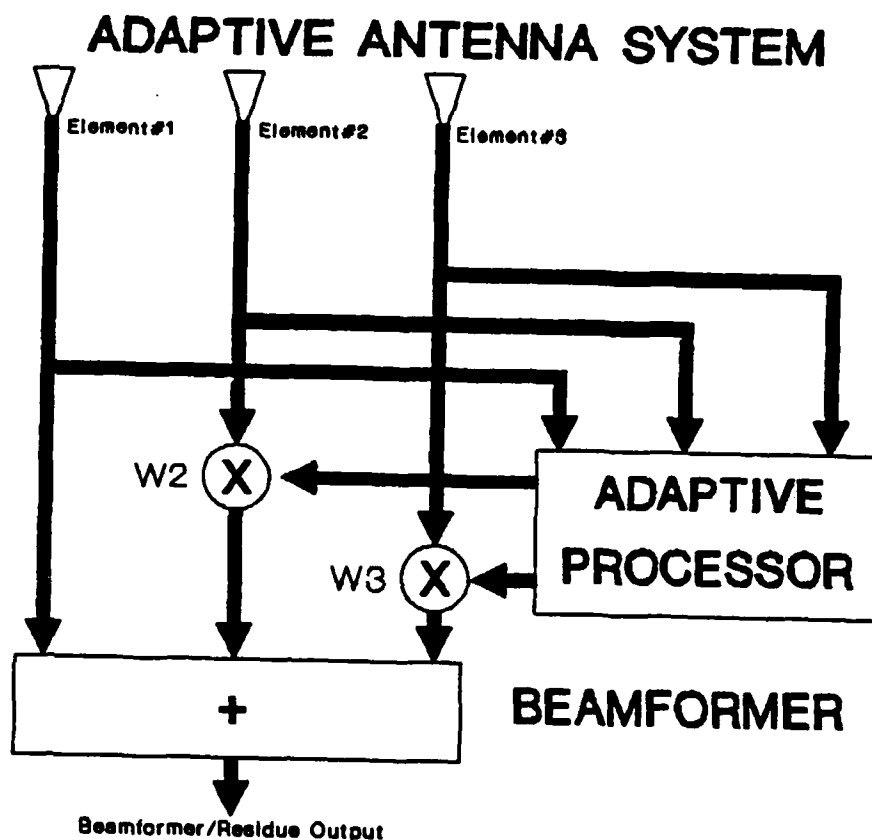


Figure 1

II Algorithms

2.1 Adaptive Spatial Filtering

A three element adaptive antenna system is shown in Figure 1. This system is configured as a side lobe canceller[2]. Antenna elements #2 and #3 are weighted and combined with element #1 in the beamformer. The beamformed/residue output is

used as an input for a conventional receiver. Based on the signals received from the three antenna elements the adaptive processor computes the weights that are to be applied to antenna elements #2 and #3. The weights adjust the amplitude and phase of elements #2 and #3, so that when all the signals are combined in the beamformer, the output power of the interference signal will be minimized. This interference suppression technique is sometimes referred to as spatial filtering because it suppresses interference based on a spatial discriminate.

2.2 Sample Matrix Inversion (SMI)

The SMI algorithm is primarily a block data algorithm. This means that M array snapshots are collected and then processed to compute a weight set. A snapshot is defined to be a sample from each antenna element at one specific time. This process is repeated to compute subsequent weight sets. The number of required snapshots, M , is at least $2N$ where N is the number of adaptive elements. The choice of $2N$ samples insures that, providing that there is no desired signal present, the weights computed will provide a solution that is within 3db of an optimum solution [2].

The SMI algorithm solves the system of equations (matrix equation) shown in Equation 1.

$$Ax=b \quad (1)$$

In this equation, A is referred to as the data matrix and contains 2N snapshots from each of the weighted antenna elements. The vector x is referred to as the weight vector and will contain N weights. The vector b is called the reference vector and contains 2N snapshots of the reference element. To solve this system of equations we proceed by multiplying both sides of Equation 1 by the Hermitian transpose of the data matrix A as shown in Equation 2.

$$A^H Ax = A^H b \quad (2)$$

Now the system is a square system of equations and the solution can be obtained by multiplying both sides by the inverse of the matrix $(A^H A)$ as shown in Equation 3.

$$(A^H A)^{-1} (A^H A) x = (A^H A)^{-1} A^H b \quad (3)$$

Equation 3 can be rewritten as shown in Equation 4.

$$x = (A^H A)^{-1} A^H b \quad (4)$$

The vector x contains the weight/solution vector that will satisfy the original system of equations.

2.3 Unitary Transformations (Givin's Method)

The following discussion is based on an RADC final report written by ESL entitled "High Speed Adaptive Signal Processing"[3]. The algorithm, called Givin's Method, is a method of solving a system of linear equations that is formed from sampled signals taken from an adaptive array. The adaptive array takes samples of the same signal that are spatially or time separated, causing them to differ slightly in amplitude and phase. One of these samples is used as a reference, and an estimate of the reference is made by taking a linear combination of the rest of the samples. This estimate is subtracted from the reference to cancel out any high power interference. A system of equations must be solved to determine the weights that each of the samples must be multiplied by. The system of equations is of the form, $Aw=b$, where A is an $m \times n$ matrix comprised of the m snapshots of the signal sampled at each of the n antenna elements, w is an n element weight column vector, and b is the m element reference column vector.

An example using three antenna elements and four snapshots is used to demonstrate Givin's Method. The system of equations to be solved looks like this:

$$\begin{bmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \\ A_{31} & A_{32} \\ A_{41} & A_{42} \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \\ b_3 \\ b_4 \end{bmatrix}$$

The columns of A represent the two nonreference antennae, and the rows represent the four snapshots taken at each. The w values are the unknown weights and the b values are the values of the four snapshots of the signal at the reference antenna.

The goal of Givin's method is to multiply the system of equations by some unitary transformation matrix that will result in a system of equations that is easy to solve. Factoring the A matrix into some matrix Q and an upper triangular matrix U gives the equation:

$$QUw=b$$

Q is defined to be a unitary matrix so that

$$Q^H=Q^{-1}$$

where Q^H is the Hermitian transpose of Q. Multiplying both sides of the equation by this gives

$$Q^HQUw=Q^Hb$$

$$\text{and } Uw=Q^Hb$$

With the weight vector being multiplied by an upper triangular matrix, this equation is very simple to solve. Q^Hb must be solved first, and then a simple backsolve will give the weight vector. Q is the unitary transformation matrix that is

needed. Givin's method does not calculate this matrix specifically, but it applies a series of two by two matrices to the A matrix, which has the same effect of producing the upper triangular matrix. Since the Q^H vector must be applied to b as well as to A, it is convenient to form a new matrix having $n + 1$ columns that combines the two. The new matrix will be in the form

$$\bar{A} = \begin{bmatrix} A_{11} & A_{12} & b_1 \\ A_{21} & A_{22} & b_2 \\ A_{31} & A_{32} & b_3 \\ A_{41} & A_{42} & b_4 \end{bmatrix}$$

The algorithm applies what are called Givin's rotations. It calculates a two by two matrix defined to be

$$M = \begin{bmatrix} c & s \\ -s & c \end{bmatrix}$$

where

$$c = x^*/r$$

$$s = n/r$$

$$r = (n^2 + |x|^2)^{1/2}$$

where n is a real number, x is complex, and x^* is the complex conjugate of x . It assigns entries from the same column and in adjacent rows of the $\bar{A}$ matrix to x and n starting with the lower left corner. This would be in the form

$$\bar{A} = \begin{bmatrix} A_{11} & A_{12} & b_1 \\ A_{21} & A_{22} & b_2 \\ x & A_{32} & b_3 \\ n & A_{42} & b_4 \end{bmatrix}$$

Since n has to be a real number, a row of zeroes is added to form

$$\bar{A} = \begin{bmatrix} A_{11} & A_{12} & b_1 \\ A_{21} & A_{22} & b_2 \\ A_{31} & A_{32} & b_3 \\ x & A_{42} & b_4 \\ n & 0 & 0 \end{bmatrix}$$

The M matrix is then formed and multiplies the bottom two rows resulting in

$$\bar{A} = \begin{bmatrix} A_{11} & A_{12} & b_1 \\ A_{21} & A_{22} & b_2 \\ A_{31} & A_{32} & b_3 \\ r & A_{42} & b_4 \\ 0 & 0 & 0 \end{bmatrix}$$

The next step is to give x the value of A₃₁ and n the value of r and form a new M matrix. Note that the old value of r is now called n. Now multiply the third and fourth rows by this matrix and the new matrix will be

$$\bar{A} = \begin{bmatrix} A_{11} & A_{12} & b_1 \\ A_{21} & A_{22} & b_2 \\ r & A_{32} & b_3 \\ 0 & A_{42} & b_4 \\ 0 & 0 & 0 \end{bmatrix}$$

This procedure is continued up to the diagonal element which is A₁₁, then it is done in each of the remaining columns. After this is complete, the final matrix will look like

$$\bar{A} = \begin{bmatrix} A_{11} & A_{12} & b_1 \\ 0 & A_{22} & b_2 \\ 0 & 0 & b_3 \\ 0 & 0 & 0 \\ 0 & 0 & 0 \end{bmatrix}$$

Keep in mind that these nonzero values are not the same as the values in the original matrix. Now the matrix is in the desired upper triangular form. In matrix form the equation looks like

$$\begin{bmatrix} A_{11} & A_{12} \\ 0 & A_{22} \\ 0 & 0 \end{bmatrix} \begin{bmatrix} w_1 \\ w_2 \end{bmatrix} = \begin{bmatrix} b_1 \\ b_2 \\ b_3 \end{bmatrix}$$

The values of the weights can be solved using the equations

$$A_{11}w_1 + A_{12}w_2 = b_1$$

$$A_{22}w_2 = b_2$$

Using back substitution

$$w_2 = b_2/A_{22}$$

$$w_1 = (b_1 - A_{12}w_2)/A_{11}$$

In summary Givins's method forms the matrix $\bar{A} = [A \ b]$, applies the algorithm to form $Q^H \bar{A} = [U \ Q^H b]$, and then solves $Uw = Q^H b$ for w using back substitution.

III Processor Design and Emulation

3.1 EMUL

EMUL is a software tool which can be used to emulate a parallel processor design. The process starts by designing a processor architecture optimized for a specific algorithm. Basic building blocks such as delays, multipliers, adders etc... are connected together to form the processor. To design

an optimum processor for a specific algorithm the inherent parallelism of the algorithm must be identified and exploited. Parallelism is characterized by simple calculations which are similar and can be computed independently of other calculations. These simple calculations can be implemented using a few sub-processors sometimes referred to as cells. EMUL can be used to design and link cells together to build complete processors.

The simple algorithm shown in Equation 5 will be used to describe the process of designing, emulating and testing using EMUL.

$$(a^2+b^2)/(c^2+d^2)^{-1/2} \quad (5)$$

Inspecting this algorithm for parallelism indicates that a, b, c, and d should be squared then the results used to form the numerator and denominator sums. This suggests two identical sub-processors/cells to compute the numerator and denominator sums. One possible design for the subject processor is shown in Figure 2. In Figure 2 "D1" means a delay of one, "Mult" means multiply, "Sum" means summation and "Inverse Square Root" means one over the square root of the input. The nodes and processor elements should be numbered as shown in Figure 2. The level of design in Figure 2 is required before using EMUL to emulate a processor. With Figure 2 in hand the example processor structure can be interactively input to EMUL. The

Example Processor

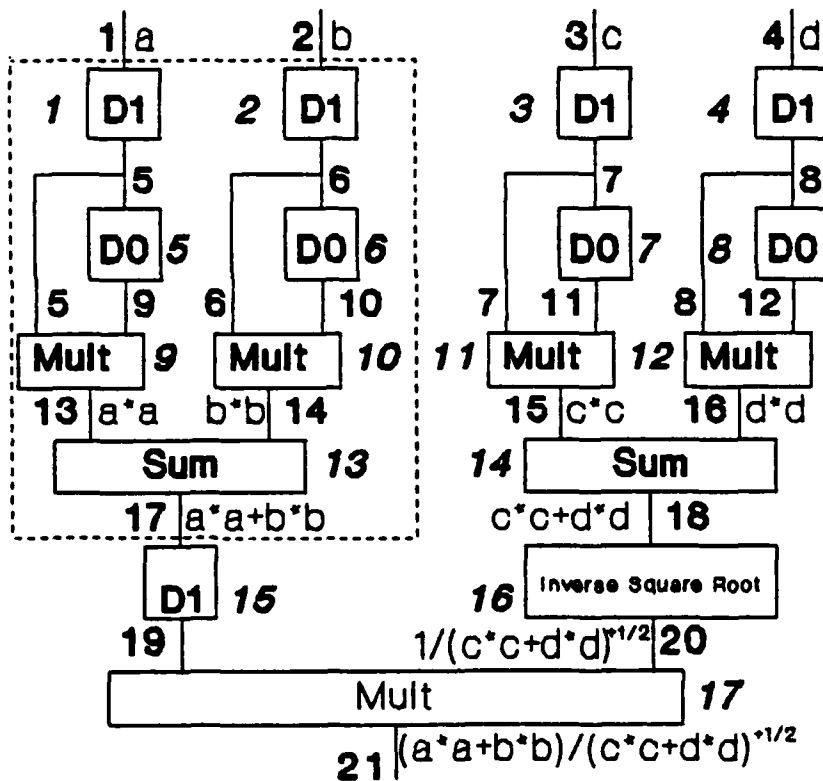


Figure 2

processor shown in Figure 2 can be simplified by combining the elements within the dotted line to form a cell. This cell is shown in Figure 3. At this point we are ready to use EMUL to emulate the cell and test its operation. A computer print out of an interactive session with EMUL to emulate and test the subject cell is contained in Appendix A. Using EMUL interactively a system specification file will be created. For the cell shown in Figure 3 the file is called EXPCEL.SSF and is contained in Appendix A. This file for each element in the

Example Cell

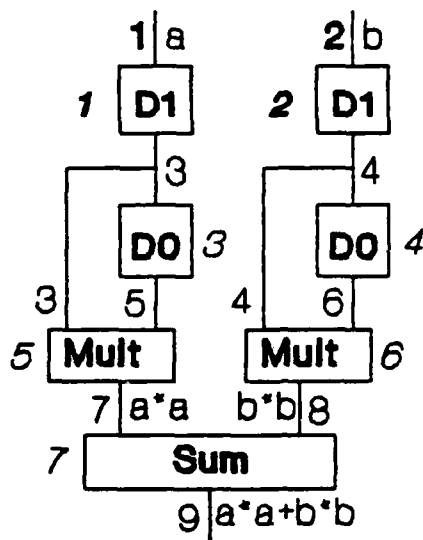


Figure 3

cell contains the input and output node numbers, fixed or floating point specification, type of element, number of bits of precision and the delay through the element. Once a .SSF file is complete, a test run specification file must be developed. For the subject cell this file is called EXPCEL.TSF and is also contained in Appendix A. The .TSF file contains the number of input data snapshots, number of elements in the processor/cell, the number of cells within the processor and the input node, input data value and the input element number for each input to the processor/cell. Once these two files are complete the simulation/emulation can be run. The emulation produces an output file called EXPCEL.OUT which is

contained in Appendix A. The .OUT file contains the inputs and outputs of all elements processing data for each clock cycle and for each data snapshot.

In Figure 4 the complete example system is shown. This system incorporates the cell previously developed. The interactive session listing, .SSF, .TSF, and .OUT files, are contained in Appendix B. One important item to note is that cells can contain no more than 99 elements. Appendix B can be studied for correct operation of EMUL.

All algorithms exhibit some degree of parallelism and

Example System

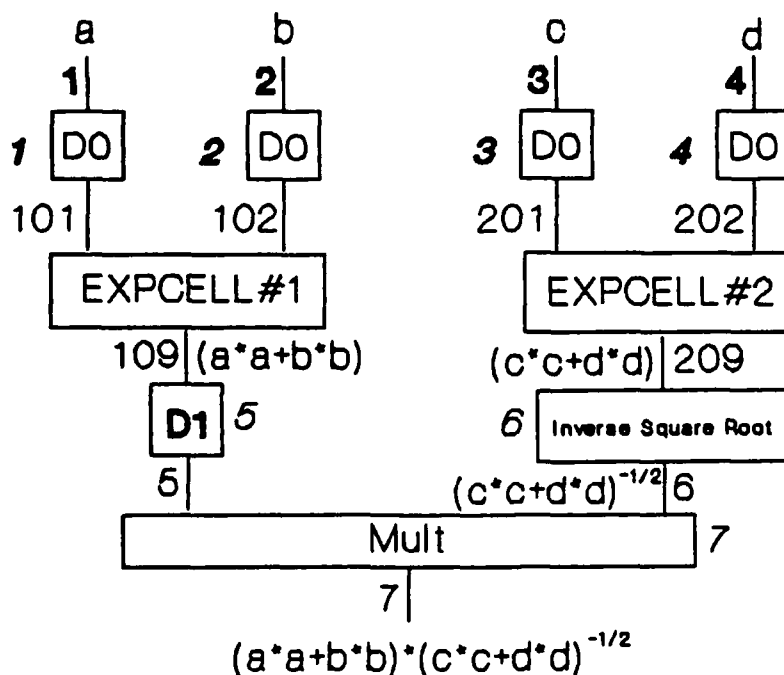


Figure 4

nonparallelism. When parallelism exists it can be exploited as shown in the example above. When nonparallelism exists, such as a processor performing vector dot products, a sum of products is necessary. This requires that the output of a summing element be fed back to its input. Such a feed back element configuration is shown in Figure 5. Note the dotted line connected to input node number two. This node can be initialized on the first snapshot to any convenient constant. The interactive emulation file for this example is contained in Appendix C. Note that node two is initialized to zero and the element adds all the numbers presented at node one for subsequent clock cycles.

Element Feedback Example

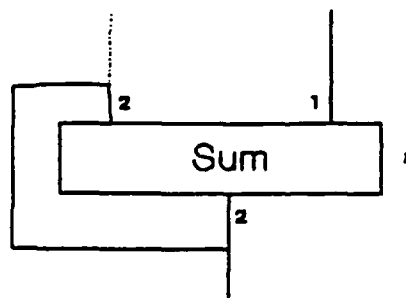


Figure 5

3.2 Emulation of the Sample Matrix Inversion Processor

The SMI algorithm consists basically of two major steps. The first step is to form a correlation matrix from the received antenna array data and the second step is to invert that matrix to obtain the weight vector. The SMI processor consists of two subprocessors which implement these two steps. In Figure 6 one subprocessor is referred to as the "COMPLEX

SAMPLE MATRIX INVERSION PROCESSOR (SMI)

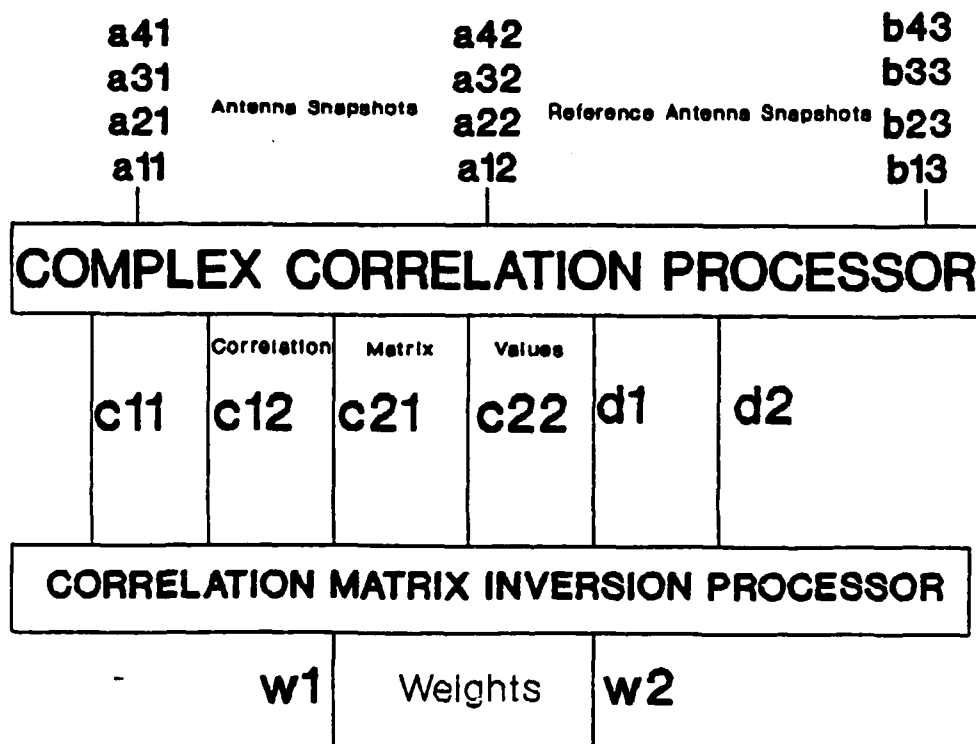


Figure 6

CORRELATION PROCESSOR" and the second subprocessor is referred to as the "CORRELATION MATRIX INVERSION PROCESSOR". As shown in Figure 6 these two processors together form the SMI processor.

The "COMPLEX CORRELATION PROCESSOR" is shown in Figure 7. Only two cells were needed to implement this processor. The Complex Vector Magnitude Cell (CVMcell) is shown in Figure 8. This cell performs a complex vector dot product of a vector

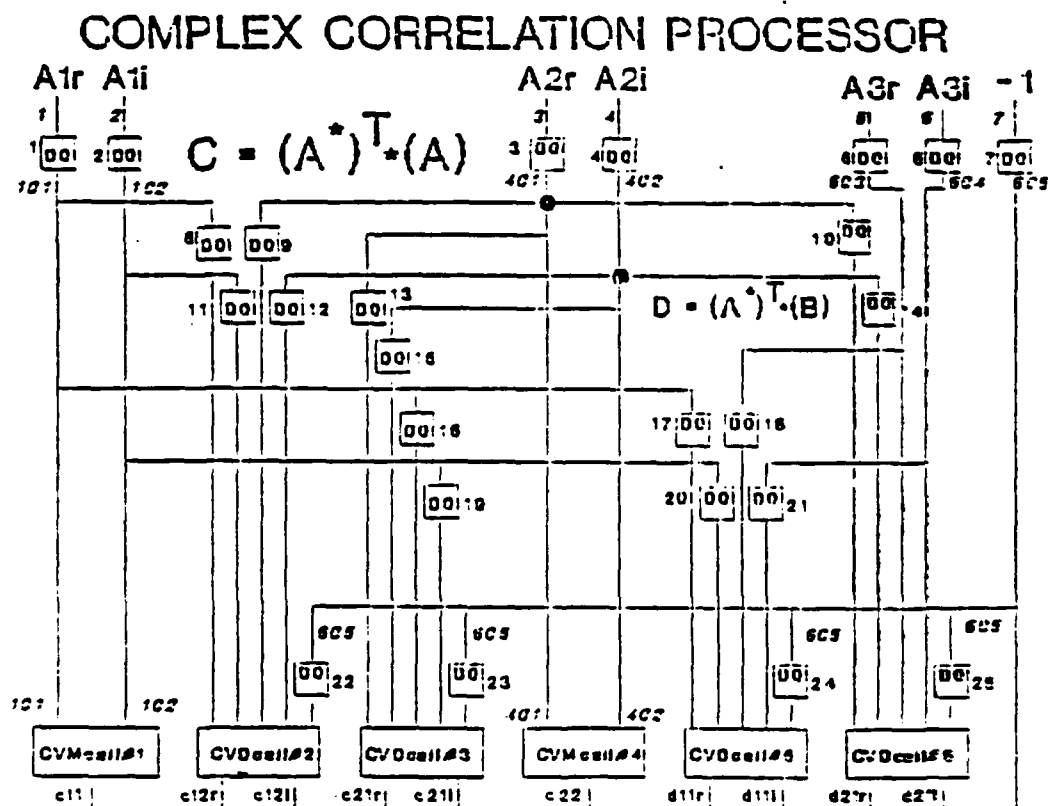


Figure 7

COMPLEX VECTOR MAGNITUDE CELL (CVMcell)

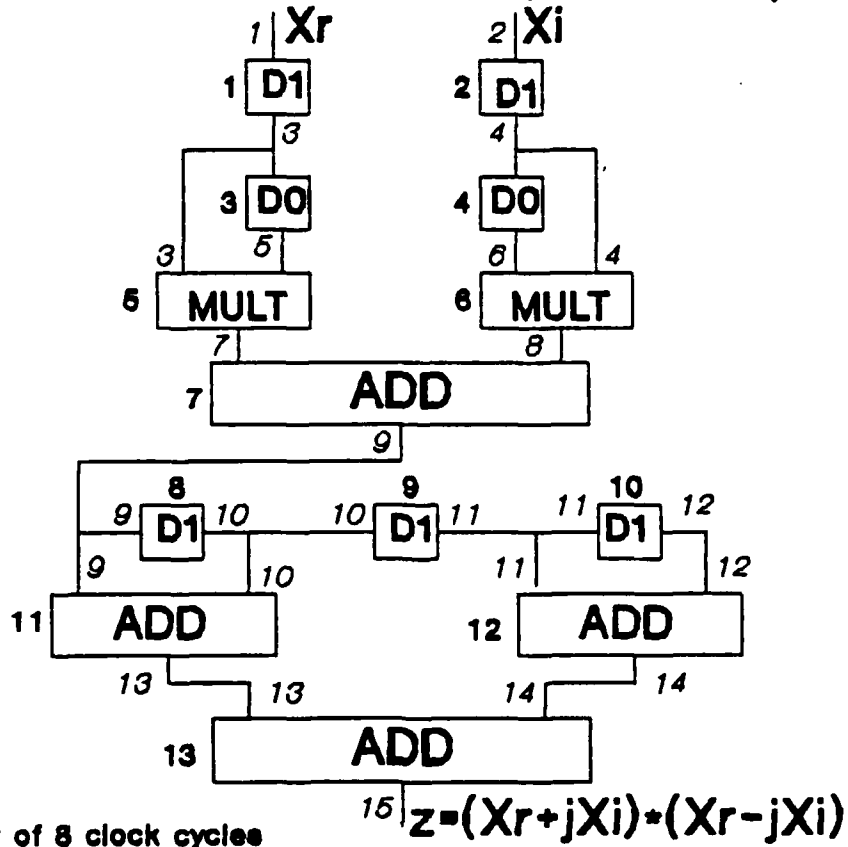


Figure 8

with itself. The Complex Vector Dot Product Cell (CVDcell) is shown in Figure 9. This cell performs a complex vector dot product for any two complex vector inputs. Note that a -1 input must be applied to Element 13 to form the conjugate. Both of these cells operate on vectors of size four and output valid results every eight clock cycles.

The "CORRELATION MATRIX INVERSION PROCESSOR" is shown in Figure 10. Two cells were used to implement this subprocessor.

COMPLEX VECTOR DOT PRODUCT CELL (CVDcell)

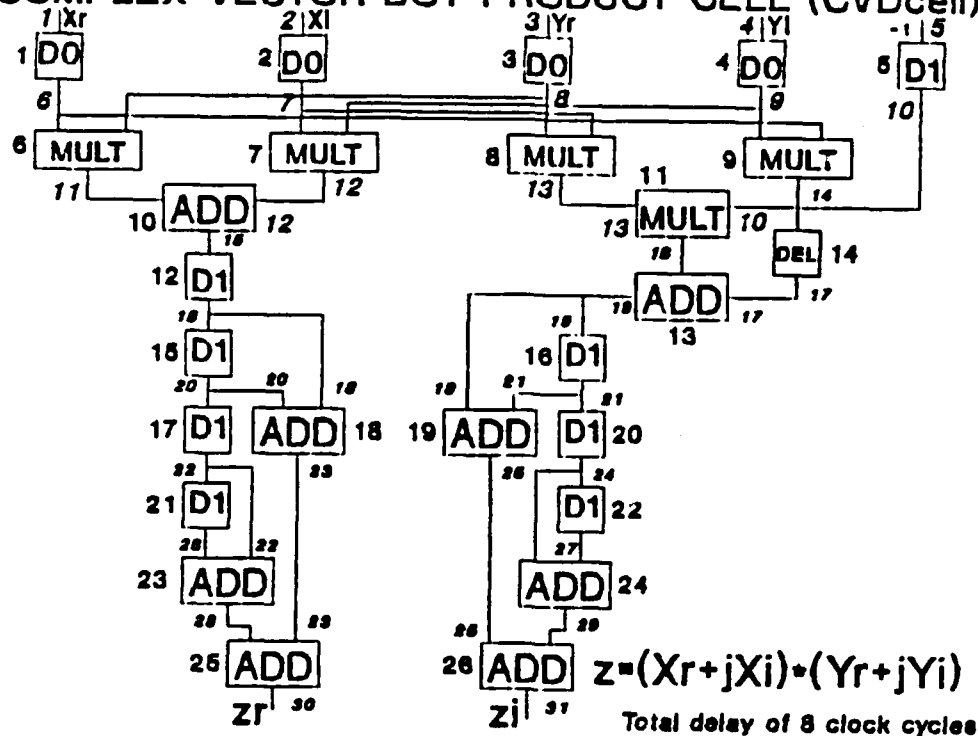


Figure 9

The Inverse determinate cell (IDTcell) is shown in Figure 11. This cell computes the determinate of the correlation matrix and divides this quantity into one using a one over the square root element. Note that -1 is used to perform subtraction. The Weight Cell (WTcell) is shown in Figure 12. This cell also uses multiplication by -1 to do later subtractions. The associated emulation files are in Appendix D.

3.3 Emulation of the Unitary Transformations Processor

When designing the hardware needed for implementing

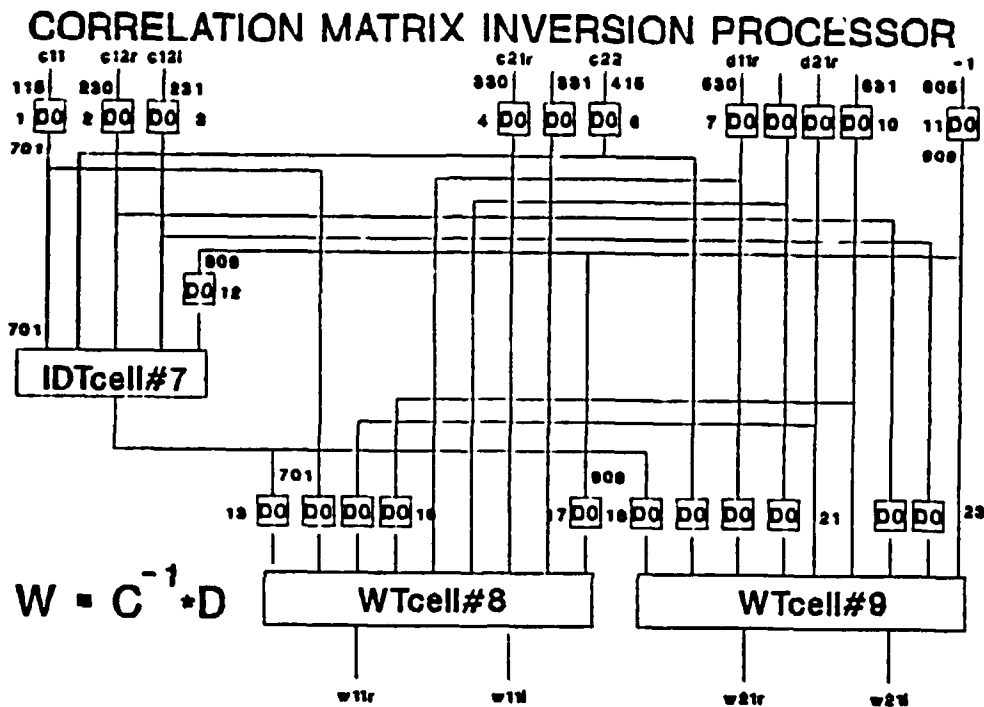


Figure 10

Givin's method, two types of arrays are needed: the QU array and the backsolve array. The QU array forms the $[U Q^H b]$ matrix and is composed of two types of cells. The boundary cell calculates the values of c and s for the M matrix, and the internal cell applies the M matrix to the $\bar{A}$ matrix. Since the three element adaptive array that was used in the previous example will also be the one used on the systolic array processor emulator, the backsolve array will be very simple and can be designed as a single cell. Therefore, three types of cells are required.

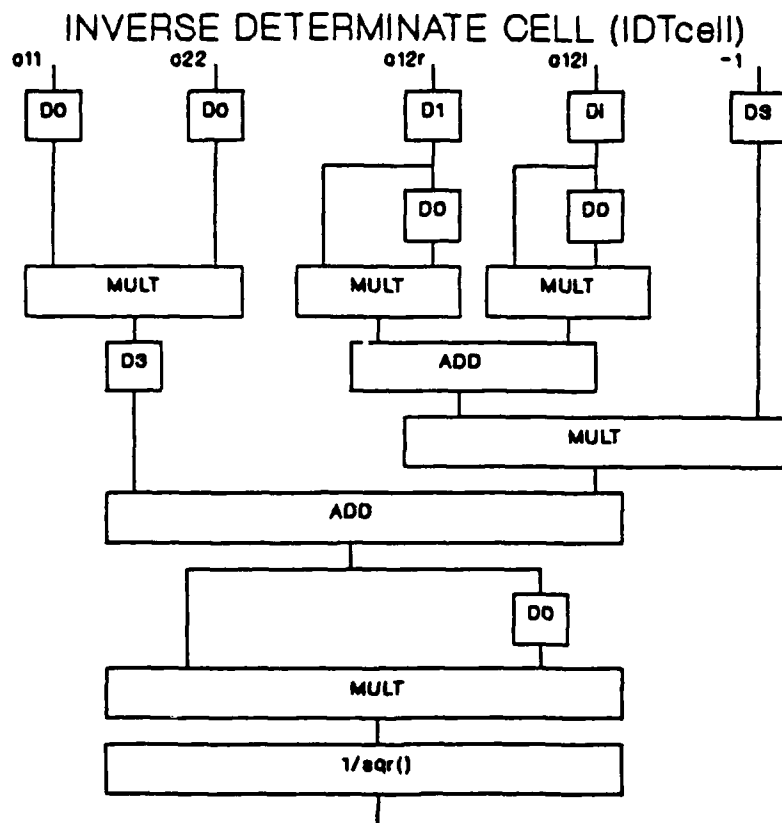


Figure 11

The "BOUNDARY CELL", shown in Figure 13, creates the Givin's rotation matrices. The outputs of this cell are the values of c and s . The elements of a column of the $\bar{A}$ matrix are input to the cell starting with the bottom row at the inputs X_r and X_i which are the real and imaginary components. There will be one of these cells for every column of the matrix (for every antenna element). On the right hand side of the cell the components of the input (r) are squared and summed producing the square of the magnitude (r^2). This value is summed with n^2 (which is the previous value of r^2 , and in the first case is zero), and the inverse of the square root of this

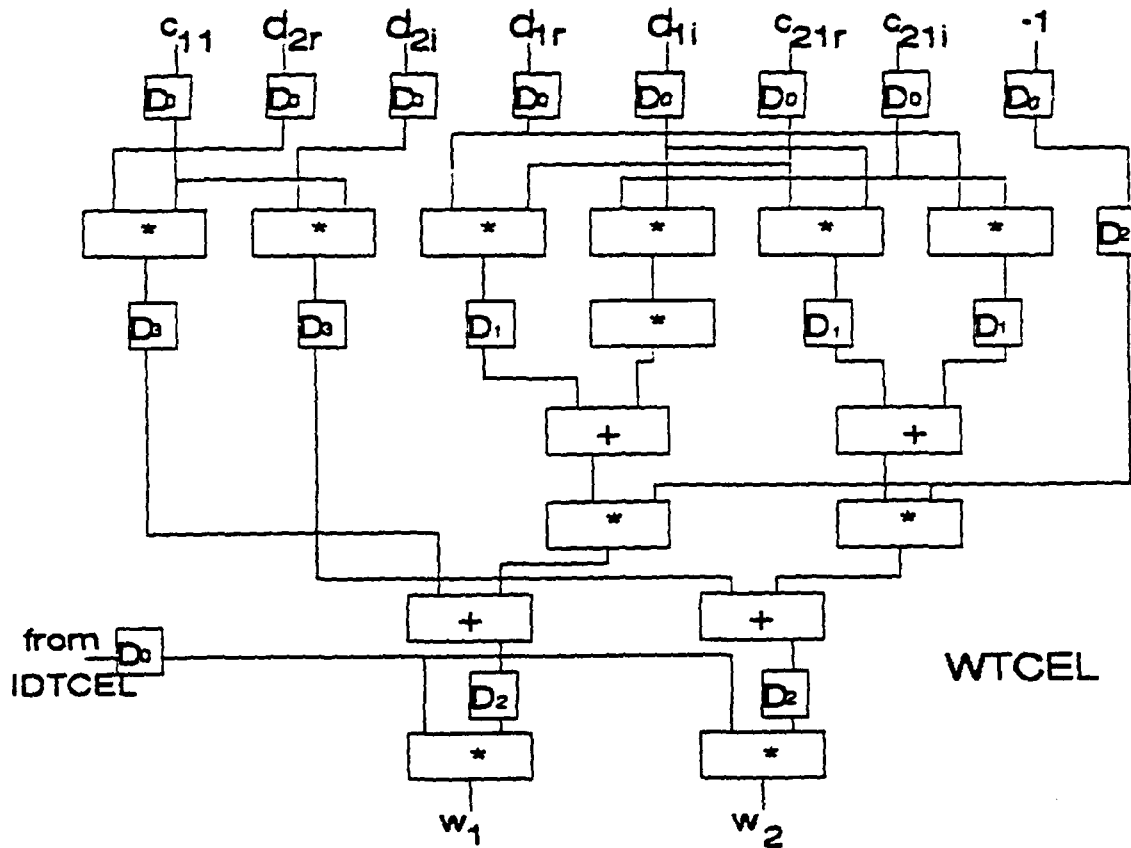


Figure 12

value is taken to give the new value of $1/r$. Multipliers 17, 18, and 19 produce the value of c and multiplier 21 produces s . Note that s is output one cycle later than c . Multiplier 20 recovers the value of n by recovering the previous value of r by multiplying together the previous values of r^2 and $1/r$.

The "INTERNAL CELL", shown in Figure 14, applies Givin's rotations to a single column of $\bar{A}$. The bottom most element of the column falls through to become the first value of y . This is done by having the first values of c and s to be equal

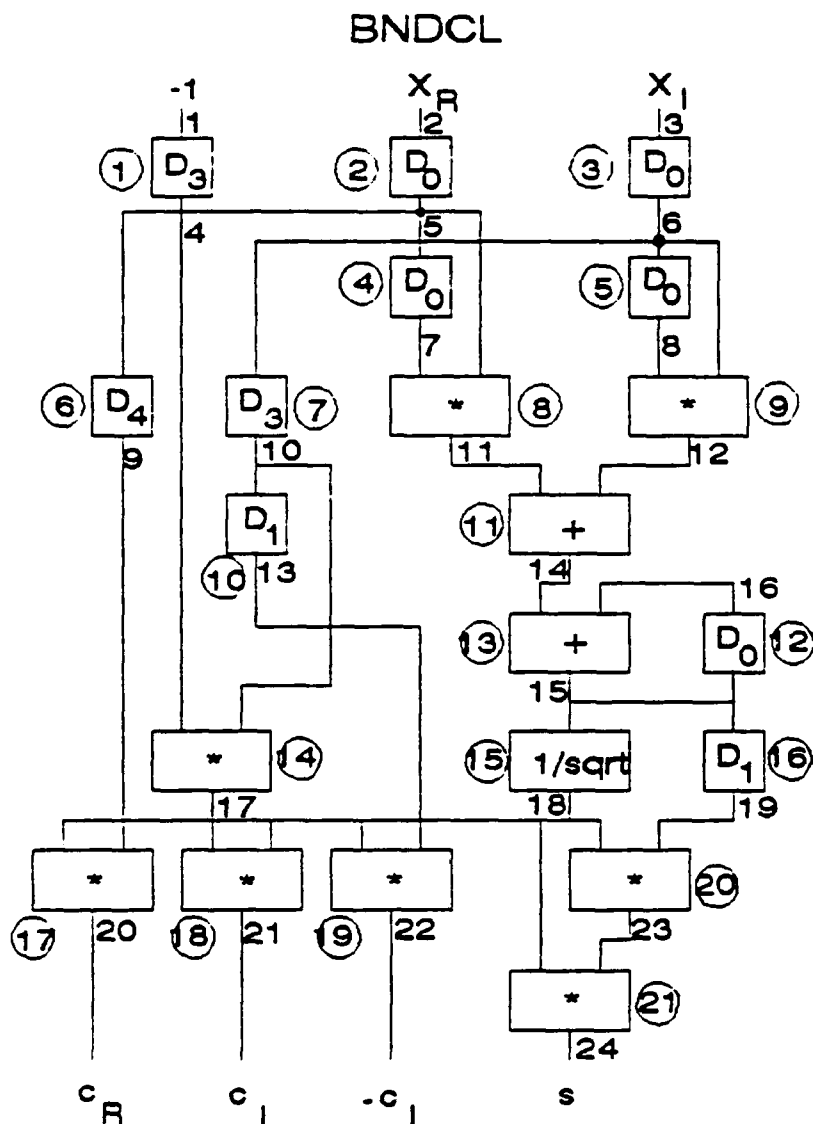


Figure 13

to 1 and 0 respectively. The delays of multipliers 8 through 13, adders 20, 21, 28 and 29, and delays 22 and 23 are set to be 0 so that the value of y will be ready on the next clock cycle. This seemed to be the only sensible way to emulate the processor, because there is no way to have a delay equal to a

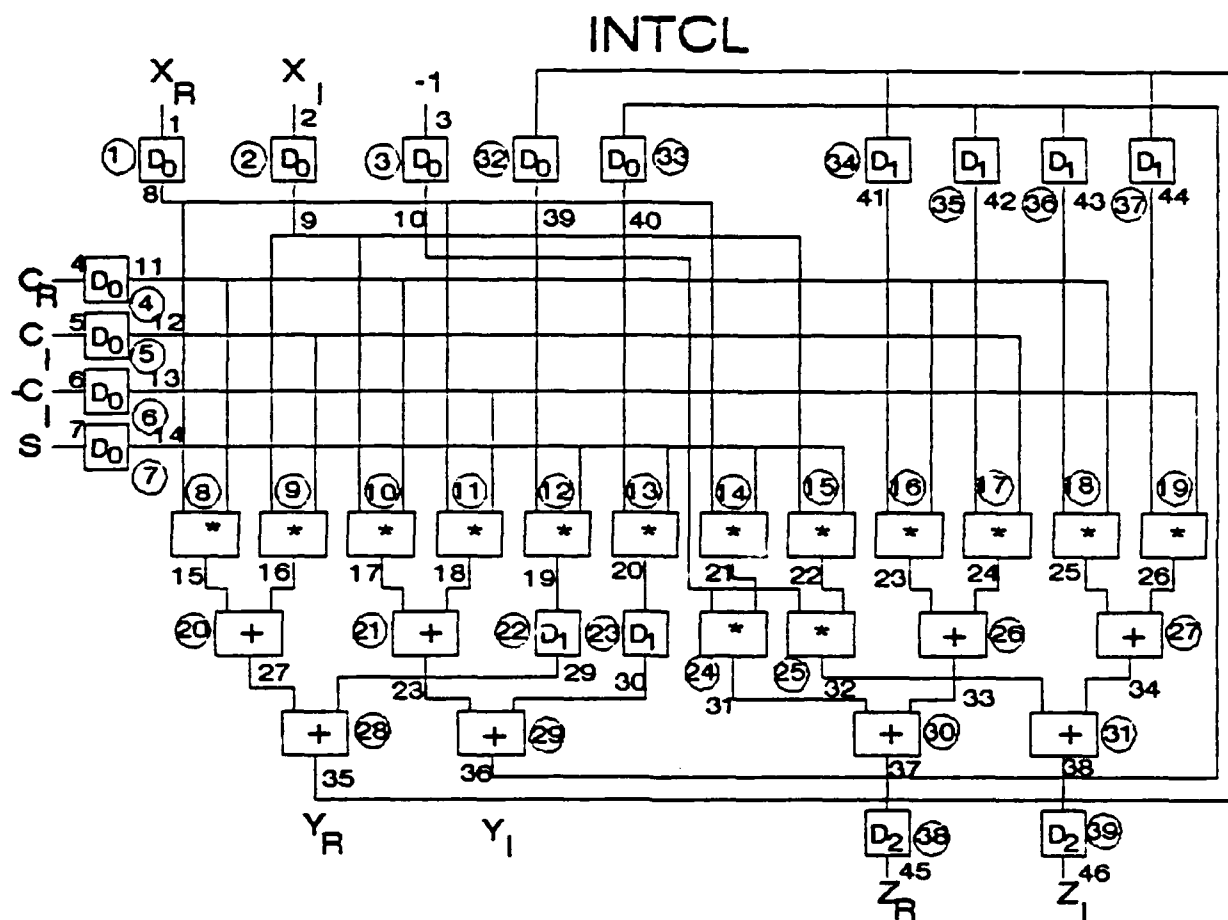


Figure 14

fraction of the time of a snapshot. After the rotations are applied to x and y , these values are called y and z . The value of z is output, and y is fed back to be used in the next rotation. This is done up to the diagonal element in the $\bar{A}$ matrix. The equations for calculating these values are

$$\begin{aligned} Y_r &= C_r X_r - C_i X_i + S Y_r \\ Y_i &= C_r X_i + C_i X_r + S Y_i \\ Z_r &= C_r Y_r + C_i Y_i - S X_r \\ Z_i &= C_r Y_i - C_i Y_r - S X_i \end{aligned}$$

The "BACKSUBSTITUTION CELL" is shown in Figure 15. This

BACSUB

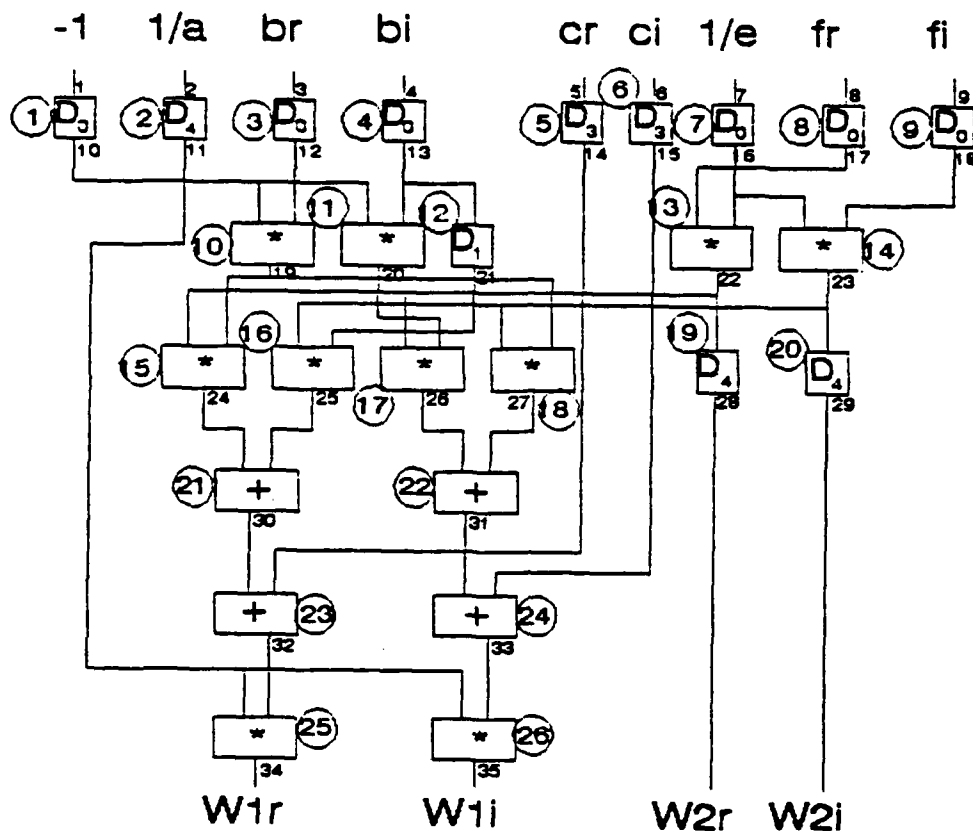


Figure 15

cell is straight forward and computes the weights through the equations

$$w2 = b2/A22 \text{ and}$$

$$w1 = (b1 - A12*w2)/A11$$

In the figure the equations are

$$w2 = f/e \text{ and}$$

$$w1 = (c - b*w2)/a$$

The full form of the "GIVIN'S METHOD WEIGHT COMPUTER" is in the same formation as the final A matrix, and is shown in Figure 16. The three columns are input into the top three cells. Final values of $1/A_{11}$, A_{12} , A_{13} , $1/A_{22}$, and A_{23} are produced from boundary cell 1, internal cell 2 and 3, boundary

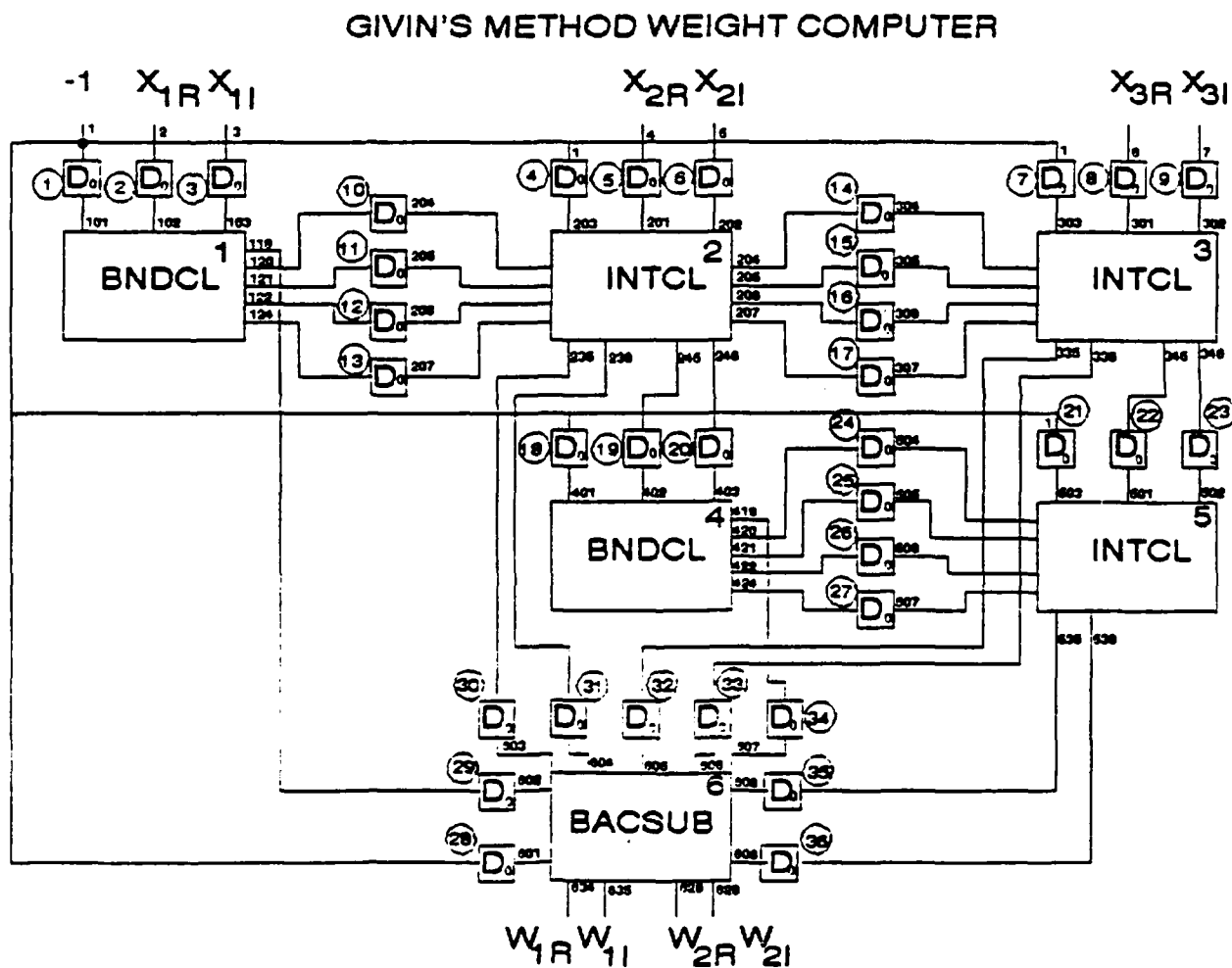


Figure 16

cell 4, and internal cell 5 respectively. These values are then fed into the back substitution cell. The column 2 inputs must be delayed until the values of c and s are ready from the column 1 boundary cell. The column three inputs must also be delayed because internal cell 5 must wait for the boundary cell in column two. These delays are added to the cells internally as well as delays used so that the outputs of one cell will arrive at the inputs of other cells at the right time. These delays are the factors that limit the speed of the processor. The emulation files for these cells are in Appendix E.

IV Processor Test and Evaluation

4.1 GADAR

GADAR is a software tool which allows a user to emulate a design of a single or multiple antenna receiver system. A simplified single antenna element receiver system is shown in Figure 17. The system is emulated by connecting together elements, numbering elements, defining and numbering nodes where elements are connected and choosing the performance parameters of each element. Receive antennas and emitting sources can be positioned in a three dimensional coordinate system to allow emulation of various communications system scenarios. The output of the system shown in Figure 17 is in-phase and quadrature digital base band data from the analog

SINGLE ELEMENT RECEIVER

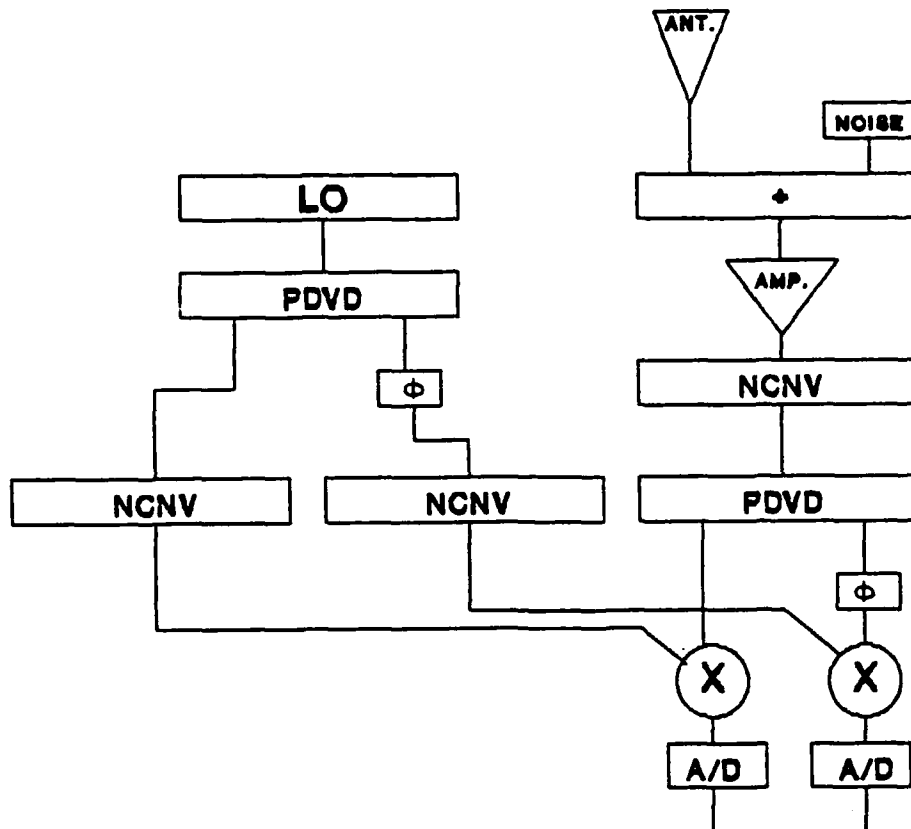


Figure 17

to digital converters 14 and 15. An interactive emulation file for this single element receiver system is contained in Appendix F.

4.2 Testing of the SMI Processor

Using GADAR a three element receiver system was designed and emulated. The three element receiver system is shown in Figure 18. The output of the three element receiver is

THREE ELEMENT RECEIVER

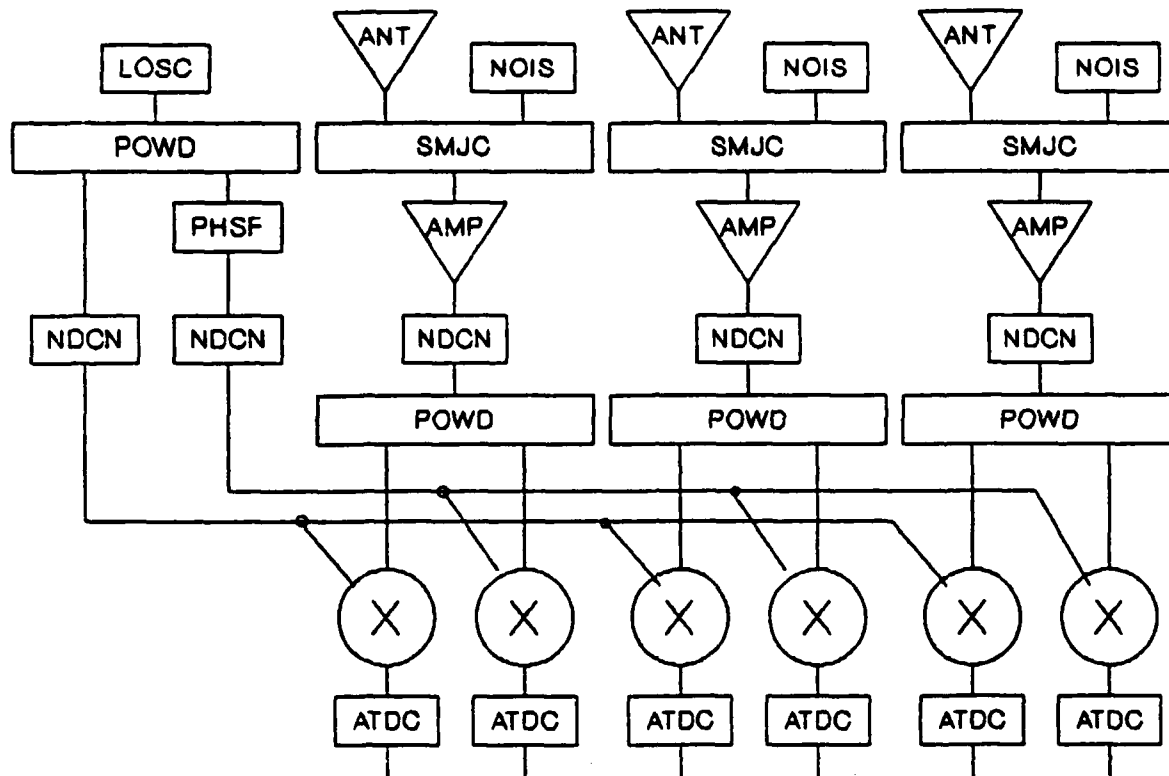


Figure 18

in-phase and quadrature baseband digital samples from the three antenna elements of the emulated array receiver system. An interactive file showing the emulation process of the three element system and the output data file is included in Appendix G. The data represents a single sinusoidal interference source broad side to the three element array. The output file of GADAR is used as an input file to EMUL for the emulation of the SMI processor described in Section 3.2. In Figure 18 the symbols are Local Oscillator (LOSC), Power Divider (POWD), Phase

Shifter (PHSF), Node Conversion (NDCN), Antenna (ANT), NoiseSource (NOIS), Summing Junction (SMJC), Amplifier (AMP), Analog To Digital Converter (ATDC) and a circle with an x inside is a Mixer/Multiplier. Using the data from the three element receive array the SMI processor computed two weights for application to the two adapted elements. The complex weights computed by the SMI processor are (0.367,0.338), (0.367,0.337). Using the equations described in Section 2.2 the weights were computed to be (0.385,0.354), (0.385,0.354). Four samples were averaged to obtain the SMI processor result. Using "An Adaptive Satellite Communication Analysis Computer Program (SATCOM)" [4] an adaptive antenna patterns plot was generated. The adaptive antenna pattern is shown in Figure 19 where the dotted line is the broadside steered conventional three element pattern and the solid line is the adaptive gain pattern with the SMI computed weights applied to the GADAR generated data. The pattern shows about a 18db null in the direction of the interference source. Other patterns were run with similar results verifying the proper operation of the SMI processor. Using the element feedback technique described in Section 3.1 the SMI processor could be designed to average large numbers of samples to provide improved performance.

Amplitude Scale =
-18 dB/division

THREE ELEMENT PATTERN

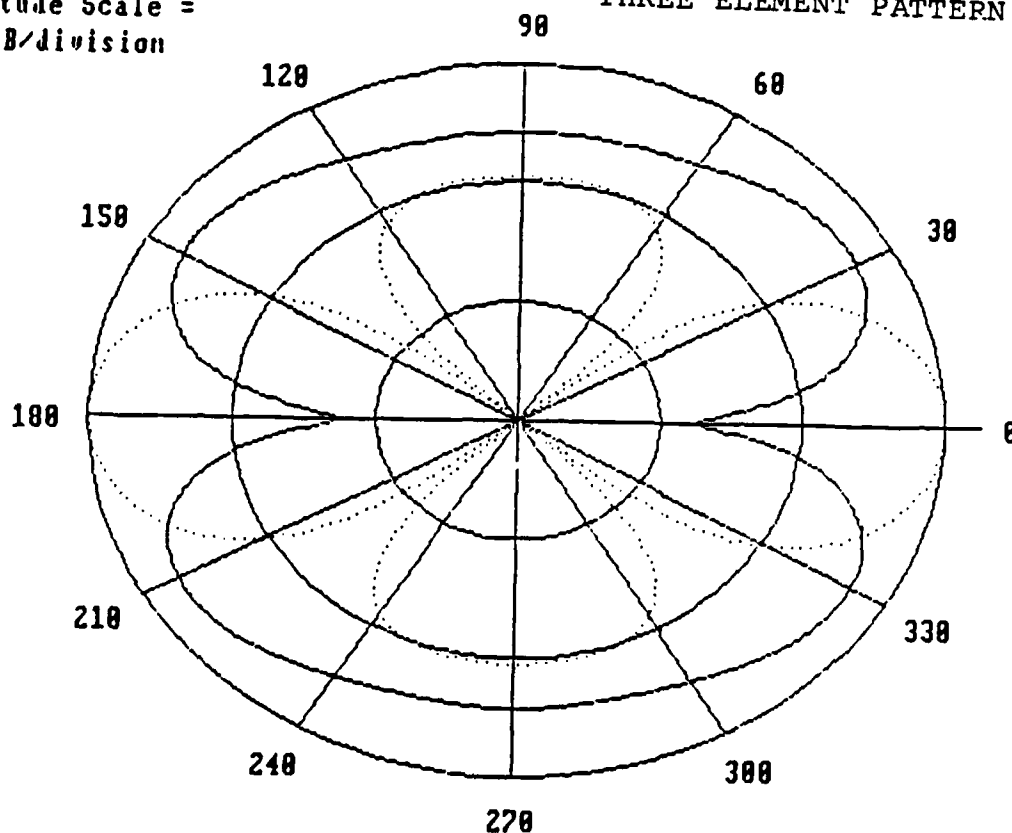


Figure 19

4.3 Testing of the Unitary Transformations Processor

The data generated using GADAR was also used for testing the Givin's method weight computer. The results were identical to the results using the equations. These were (.385, .354) and (.385, .354). These results were output on the 24th cycle of snapshot 1 and the 22nd cycle of snapshot 3. They are shown in the output file in Appendix E.

V Conclusions

This report covers the process of designing and emulating an adaptive antenna processor, designing and emulating an adaptive antenna receive system and using the output of the antenna receive system to test the emulated adaptive antenna processor. The work done has shown that EMUL and GADAR can be effectively used to design and emulate adaptive signal processing systems. The design, emulation and testing of a system in this fashion can provide a high degree of confidence that a hardware implementation will be functionally correct. Intermediate numerical results obtained from the emulation can provide a means of checking hardware design operation. The use of element feedback techniques can increase processor performance and reduce processor latency. The main limitation of the emulation is that the size of the processor design is limited by 99 available cells.

VI Recommendations

This work shows that many adaptive signal processing systems, specifically adaptive antenna processing systems, could benefit from the application of highly pipelined parallel digital systolic processors. Highly specialized parallel digital processors can greatly enhance the speed and dynamic range with which specific signal processing algorithms can be

implemented. This approach can provide the power necessary to solve computationally intensive signal processing problems in real time. GADAR and EMUL should be enhanced to handle larger problems. The addition of nonlinear elements to EMUL would also allow the emulation of certain types of neural net signal processing systems suitable for real time adaptive communication signal processing needs.

References

- [1] Hazeltine Corporation, "Systolic Array Processor Brassboard", RADC-TR-89-62, June 1989. (B136 000L)
- [2] Widrow, "Adaptive Signal Processing", Prentice-Hall, 1985.
- [3] ESL-A Subsidiary of TRW, "High Speed Adaptive Signal Processing Final Report", RADC-TR-85-53, March 1985 (B095 367)
- [4] Syracuse Research Corporation, "An Adaptive Satellite Communications Analysis Computer Program User's Manual (SATCOM)", SRC TR 89-1528, November 1989.

Appendix A

Interactive Example Cell Emulation File

```
Username: SMITHR
Password:
```

Send your MISVAX files to a LONEX printer, use the LP command.

Directory DC\$DISK2:[SMITHR]

Directory DC\$DISK2:[SMITHR.EMUL]

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

B

WHAT IS THE NAME OF THE CONFIGURATIN SPECIFICATION FILE
TO BE OPENED FOR WRITING?

EXPCEL.SSF

Select a component type for component 1.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

D

Component number 1 is of type: DELY. What is the one input
node number for this component?

1

What is the output node number for this component?

3

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 1 of
type DELY. Do you wish to change anything? (yes or no)

First input node: 1
Output node: 3
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock cycle(s): 1

NO

Select a component type for component 2.

- A Cell (this is a heading for chips to then be specified)
- E Add Chip

- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

D

Component number 2 is of type: DELY. What is the one input node number for this component?

2

What is the output node number for this component?

4

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 2 of type DELY. Do you wish to change anything? (yes or no)

First input node: 2
 Output node: 4
 Numerical format: FLOT
 16 bit or 32 bit size: 32
 Clock cycle(s): 1

NO

Select a component type for component 3.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

D

Component number 3 is of type: DELY. What is the one input node number for this component?

3

What is the output node number for this component?

5

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

0

The following parameters have been specified for component 3 of type DELY. Do you wish to change anything? (yes or no)

First input node: 3
Output node: 5
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock cycle(s): 0

NO

Select a component type for component 4.

A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Look Up Chip
F quit (terminate structure entry)

D

Component number 4 is of type: DELY. What is the one input node number for this component?

4

What is the output node number for this component?

6

What numerical format is desired for this format?

A floating point
B fixed point

A

Should the component be 16 bit or 32 bit?

A 16
B 32

B

How many clock cycles is this chip?

0

The following parameters have been specified for component 4 of type DELY. Do you wish to change anything? (yes or no)

First input node: 4
Output node: 6
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock cycle(s): 0

NO

Select a component type for component 5.

A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Look Up Chip
F quit (terminate structure entry)

C

3 Component number 5 is of type: MULT. What is input node
number 1 for this component?

5 Component number 5 is of type: MULT. What is input node
number 2 for this component?

7 What is the output node number for this component?

What numerical format is desired for this format?
A floating point
B fixed point
A

Should the component be 16 bit or 32 bit?
A 16
B 32
B

1 How many clock cycles is this chip?

The following parameters have been specified for component 5 of
type MULT. Do you wish to change anything? (yes or no)
First input node: 3
Second input node: 5
Output node: 7
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock Cycle(s): 1
NO

Select a component type for component 6.
A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Look Up Chip
F quit (terminate structure entry)
C

4 Component number 6 is of type: MULT. What is input node
number 1 for this component?

6 Component number 6 is of type: MULT. What is input node
number 2 for this component?

8 What is the output node number for this component?

What numerical format is desired for this format?
A floating point
B fixed point
A

Should the component be 16 bit or 32 bit?

A 16
B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 6 of
type MJLT. Do you wish to change anything? (yes or no)

First input node: 4
Second input node: 6
Output node: 8
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock Cycle(s): 1

NO

Select a component type for component 7.

A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Look Up Chip
F quit (terminate structure entry)

B

Component number 7 is of type: ADDR. What is input node
number 1 for this component?

7

Component number 7 is of type: ADDR. What is input node
number 2 for this component?

8

What is the output node number for this component?

9

What numerical format is desired for this format?

A floating point
B fixed point

A

Should the component be 16 bit or 32 bit?

A 16
B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 7 of
type ADDR. Do you wish to change anything? (yes or no)

First input node: 7
Second input node: 8
Output node: 9
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock Cycle(s): 1

NO

Select a component type for component 8.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

F

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

D

\$ TYPE EXPCEL.SSF
ONFIGURATIN

1	0	3	FLOT	DELY	32	1
2	0	4	FLOT	DELY	32	1
3	0	5	FLOT	DELY	32	0
4	0	6	FLOT	DELY	32	0
3	5	7	FLOT	MULT	32	1
4	6	8	FLOT	MULT	32	1
7	8	9	FLOT	ADDR	32	1

\$ RUN EMUL

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM EMUL. EMUL IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

- HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
- EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
- BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

C

WHAT IS THE NAME OF THE EXPERIMENT SPECIFICATION FILE
TO BE OPENED FOR WRITING?
EXPCEL.TSF

At this time EMUL requires a general knowledge of the system that

will now be tested. How many input snapshots of the input data do you want to process?

1

What are the total number of chips in the system you are specifying, that are not located within a cell?

7

What are the total number of cells in the array processor?

0

The following parameters have been specified for this system. Do you wish to change anything?(yes or no)

Number of snapshots: 1
Number of chips: 7
Number of cells: 0

NO

For each input node of snap no. enter a line of input containing input node number, input data value and chip to which this data enters.

How many input nodes will you enter at this time?

2

ENTER 2 LINES OF INPUT DATA AT THIS TIME
(input node no., data value, input chip no.)

1 -1 1
2 2 2

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

D

\$ TYPE EXPCEL.TSF
XPERIMENT

1

7

0

1	-1	1
2	2	2
1	0	0

\$ RUN EMUL

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM EMUL. EMUL IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

A

WHAT IS THE NAME OF THE INPUT EMU FILE?

EXPCEL.TSF

WHAT IS THE NAME OF THE OUTPUT FILE?

EXPCEL.OUT

WHAT IS THE NAME OF THE INPUT CHIP FILE?

EXPCEL.SSF

WHAT IS THE SPECIAL VISIBLE CHIP INPUT FILE

(ENTER 'NONE' IF THERE IS NONE)

(THE SPECIAL VISIBLE OUTPUT IS ALWAYS WRITTEN TO FILE 'SPVIS.OUT') ?

NONE

PULSING THE DATA...

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

D

\$ TYPE EXPCEL.OUT

*****THE SYSTOLIC EMULATOR HAS BEEN ACTIVATED*****

THE FOLLOWING INFORMATION REGARDING EACH ELEMENT HAS BEEN GIVEN TO THE EMULATOR

CHIP NUMBER	INPUT NODES NUMBERS	OUTPUT NODE NUMBER	CHIP OPERATION	CHIP CLOCK CYCLES
1	1 0	3	Delay (Time Shift)	1
2	2 0	4	Delay (Time Shift)	1
3	3 0	5	Delay (Time Shift)	0
4	4 0	6	Delay (Time Shift)	0
5	3 5	7	Multiplication	1
6	4 6	8	Multiplication	1
7	7 8	9	Addition	1

SNAPSHOT NUMBER 1 HAS BEGUN

The following data has been accepted by the emulator for input as follows:

Input Node Number	Actual Data Value
1	-1.00
2	2.00

ELEMENTS HAVE BEEN GROUPED ACCORDING TO INPUT READINESS.
PROCESSING ACCORDING TO SPECIFIED OPERATION CAN NOW BEGIN!

SNAPSHOT 1SHALL NOW BEGIN
////////////////////////////////////

Cycle 1 of snapshot 1 is ready to process
2 elements will output data.

These Chips are:

1. Chip Number 1
OUTPUT OF DELAY CHIP 1 IS -1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 1 IS -1.00
2. Chip Number 2
OUTPUT OF DELAY CHIP 2 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 2 IS 2.00

////////////////////////////////////
////////////////////////////////////
////////////////////////////////////

Cycle 2 of snapshot 1 is ready to process
4 elements will output data.

These Chips are:

1. Chip Number 3
OUTPUT OF DELAY CHIP 3 IS -1.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 3 IS -1.00
2. Chip Number 4
OUTPUT OF DELAY CHIP 4 IS 2.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 4 IS 2.00
3. Chip Number 5
 $-1.00 * -1.00 = 1.00$
OUTPUT OF CHIP 5 IS 1.00
4. Chip Number 6
 $2.00 * 2.00 = 4.00$
OUTPUT OF CHIP 6 IS 4.00

////////////////////////////////////
////////////////////////////////////
////////////////////////////////////

Cycle 3 of snapshot 1 is ready to process
1 elements will output data.

These Chips are:

1. Chip Number 7
 $1.00 + 4.00 = 5.00$
OUTPUT OF CHIP 7 IS 5.00

////////////////////////////////////
////////////////////////////////////

ALL AVAILABLE INPUT DATA HAS BEEN READ.
THE EMULATOR WILL NOW BE DEACTIVATED
\$ LOG
SMITHR logged out at 15-DEC-1989 10:24:03.95Connection closed by remote host

Appendix B

Interactive Example System Emulation File

```
Username: SMITHR
Password:
```

Last interactive login on Tuesday, 12-DEC-1989 15:34

Send your MISVAX files to a LONEX printer, use the LP command.

```

$ RUN EMUL          SET DEF [SMITH?          DIR

```

BOTH.DIR;1	EMUL.DIR;1	GADAR.DIR;1	INFO.DIR;1
LOGIN.COM;4	LOGIN.COM;3	LOGIN.COM;2	LOGIN.JOU;1
SYSTEM.DIR;1			

\$ DIR

```

ALGOR1.TSF;1      BACSUB.SSF;1      BACSUB.TSF;1      BNDCEL.SSF;1
BNDCEL.TSF;1      CACEL.SSF;1      CBACSB.SSF;1      CBNDCL.SSF;1
CBNDCL.SSF;1      CBNDCL.TSF;1      CCMCEL.SSF;1      CCOREL.SSF;1
CCOREL.TSF;1      CINTC2.SSF;1      CINTCL.SSF;1      CMCEL.SSF;1
CMULCL.SSF;1      CMULCL.TSF;1      CMXSOL.SSF;1      CMXSOL.TSF;1
COM.DIR;1         CORREL.SSF;1      CSMCEL.SSF;1      CSMI.OUT;1
CSMI.SSF;1        CSMI.TSF;1      CVDCEL.SSF;1      CVMCEL.SSF;1
EMUL.EXE;1        EXPCEL.OUT;1      EXPCEL.SSF;1      EXPCEL.TSF;1
FOR000.DAT;1      GIV2.SSF;1      GIV2.TSF;1      GIV3.SSF;1
GIV3.TSF;1        GIV4.SSF;1      IDTCEL.SSF;1      IDTCEL.TSF;1
INTCEL.SSF;1      INTCEL.TSF;1      MATSOL.SSF;1      SMI.SSF;1
SOURCE.DIR;1      SPVIS.OUT;1     TEST.DIR;1       WTCEL.SSF;1
WTCEL.TSF;1

```

\$ RUN EMUL

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM EMUL. EMUL IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

B-2

INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

B

WHAT IS THE NAME OF THE CONFIGURATIN SPECIFICATION FILE
TO BE OPENED FOR WRITING?
EXPSYS.SSF

Select a component type for component 1.
A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Look Up Chip
F quit (terminate structure entry)

D

Component number 1 is of type: DELY. What is the one input
node number for this component?

1

What is the output node number for this component?

101

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

0

The following parameters have been specified for component 1 of
type DELY. Do you wish to change anything? (yes or no)

First input node: 1
Output node: 101
Numerical format: FLOT

16 bit or 32 bit size: 32
Clock cycle(s): 0

NO

Select a component type for component 2.
A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Look Up Chip
F quit (terminate structure entry)

D

Component number 2 is of type: DELY. What is the one input node number for this component?

2

What is the output node number for this component?

101 2

What numerical format is desired for this format?

A floating point
B fixed point

A

Should the component be 16 bit or 32 bit?

A 16
B 32

B

How many clock cycles is this chip?

0

The following parameters have been specified for component 2 of type DELY. Do you wish to change anything? (yes or no)

First input node: 2
Output node: 102
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock cycle(s): 0

NO

Select a component type for component 3.
A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Look Up Chip
F quit (terminate structure entry)

D

Component number 3 is of type: DELY. What is the one input node number for this component?

3

What is the output node number for this component?

201

What numerical format is desired for this format?

A floating point

A B fixed point
 A
 Should the component be 16 bit or 32 bit?
 A 16
 B 32
 B
 How many clock cycles is this chip?
 0
 The following parameters have been specified for component 3 of
 type DELY. Do you wish to change anything? (yes or no)
 First input node: 3
 Output node: 201
 Numerical format: FLOT
 16 bit or 32 bit size: 32
 Clock cycle(s): 0
 NO
 Select a component type for component 4.
 A Cell (this is a heading for chips to then be specified)
 B Add Chip
 C Multiply Chip
 D Delay Chip
 E Look Up Chip
 F quit (terminate structure entry)
 D
 Component number 4 is of type: DELY. What is the one input
 node number for this component?
 4
 What is the output node number for this component?
 202
 What numerical format is desired for this format?
 A floating point
 B fixed point
 A
 Should the component be 16 bit or 32 bit?
 A 16
 B 32
 B
 How many clock cycles is this chip?
 0
 The following parameters have been specified for component 4 of
 type DELY. Do you wish to change anything? (yes or no)
 First input node: 4
 Output node: 202
 Numerical format: FLOT
 16 bit or 32 bit size: 32
 Clock cycle(s): 0
 NO
 Select a component type for component 5.
 A Cell (this is a heading for chips to then be specified)

- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

D

Component number 5 is of type: DELY. What is the one input node number for this component?

109

What is the output node number for this component?

5

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 5 of type DELY. Do you wish to change anything? (yes or no)

First input node: 109
 Output node: 5
 Numerical format: FLOT
 16 bit or 32 bit size: 32
 Clock cycle(s): 1

NO

Select a component type for component 6.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

E

Component number 6 is of type: LOOK. What is the one input node number for this component?

209

What is the output node number for this component?

6

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 6 of type LOOK. Do you wish to change anything? (yes or no)

First input node: 209
Output node: 6
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock Cycle(s): 1

NO

Select a component type for component 7.

A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Look Up Chip
F quit (terminate structure entry)

C

Component number 7 is of type: MULT. What is input node number 1 for this component?

5

Component number 7 is of type: MULT. What is input node number 2 for this component?

6

What is the output node number for this component?

7

What numerical format is desired for this format?

A floating point
B fixed point

A

Should the component be 16 bit or 32 bit?

A 16
B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 7 of type MULT. Do you wish to change anything? (yes or no)

First input node: 5
Second input node: 6
Output node: 7
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock Cycle(s): 1

NO

Select a component type for component 8.

A Cell (this is a heading for chips to then be specified)
B Add Chip

C Multiply Chip
 D Delay Chip
 E Look Up Chip
 F quit (terminate structure entry)

A

Enter the number of input nodes of this cell.

2

Enter the number of output nodes of the cell.

1

Enter the number of chips in cell.

7

Do you wish to change anything for this cell?(y or n)

Number of input nodes: 2

Number of output nodes: 1

Number of chips in cell: 7

NO

Select a component type for component 9.

A Cell (this is a heading for chips to then be specified)
 B Add Chip
 C Multiply Chip
 D Delay Chip
 E Look Up Chip
 F quit (terminate structure entry)

D

Component number 9 is of type: DELY. What is the one input node number for this component?

1

What is the output node number for this component?

3

What numerical format is desired for this format?

A floating point
 B fixed point

A

Should the component be 16 bit or 32 bit?

A 16
 B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 9 of type DELY. Do you wish to change anything? (yes or no)

First input node: 1

Output node: 3

Numerical format: FLOT

16 bit or 32 bit size: 32

Clock cycle(s): 1

NO

Select a component type for component 10.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

D

Component number 10 is of type: DELY. What is the one input node number for this component?

2

What is the output node number for this component?

4

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 10 of type DELY. Do you wish to change anything? (yes or no)

First input node: 2
 Output node: 4
 Numerical format: FLOT
 16 bit or 32 bit size: 32
 Clock cycle(s): 1

NO

Select a component type for component 11.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

D

Component number 11 is of type: DELY. What is the one input node number for this component?

3

What is the output node number for this component?

5

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16

B 32

B

How many clock cycles is this chip?

0

The following parameters have been specified for component 11 of type DELY. Do you wish to change anything? (yes or no)

First input node: 3
Output node: 5
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock cycle(s): 0

NO

Select a component type for component 12.

A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Lock Up Chip
F quit (terminate structure entry)

D

Component number 12 is of type: DELY. What is the one input node number for this component?

4

What is the output node number for this component?

6

What numerical format is desired for this format?

A floating point
B fixed point

A

Should the component be 16 bit or 32 bit?

A 16
B 32

B

How many clock cycles is this chip?

0

The following parameters have been specified for component 12 of type DELY. Do you wish to change anything? (yes or no)

First input node: 4
Output node: 6
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock cycle(s): 0

NO

Select a component type for component 13.

A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Lock Up Chip
F quit (terminate structure entry)

C

Component number 13 is of type: MULT. What is input node
number 1 for this component?

3

Component number 13 is of type: MULT. What is input node
number 2 for this component?

5

What is the output node number for this component?

7

What numerical format is desired for this format?

A floating point

B fixed point

A

Should the component be 16 bit or 32 bit?

A 16

B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 13 of
type MULT. Do you wish to change anything? (yes or no)

First input node: 3

Second input node: 5

Output node: 7

Numerical format: FLOT

16 bit or 32 bit size: 32

Clock Cycle(s): 1

NO

Select a component type for component 14.

A Cell (this is a heading for chips to then be specified)

B Add Chip

C Multiply Chip

D Delay Chip

E Look Up Chip

F quit (terminate structure entry)

C

Component number 14 is of type: MULT. What is input node
number 1 for this component?

4

Component number 14 is of type: MULT. What is input node
number 2 for this component?

6

What is the output node number for this component?

8

What numerical format is desired for this format?

A floating point

B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 14 of type MULT. Do you wish to change anything? (yes or no)

First input node: 4
Second input node: 6
Output node: 8
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock Cycle(s): 1

NO

Select a component type for component 15.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

B

Component number 15 is of type: ADDR. What is input node number 1 for this component?

7

Component number 15 is of type: ADDR. What is input node number 2 for this component?

8

What is the output node number for this component?

9

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 15 of type ADDR. Do you wish to change anything? (yes or no)

First input node: 7
Second input node: 8
Output node: 9
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock Cycle(s): 1

NO

Select a component type for component 16.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

A

Enter the number of input nodes of this cell.

2

Enter the number of output nodes of the cell.

1

Enter the number of chips in cell.

7

Do you wish to change anything for this cell?(y or n)

Number of input nodes: 2

Number of output nodes: 1

Number of chips in cell: 7

NO

Select a component type for component 17.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

D

Component number 17 is of type: DELY. What is the one input node number for this component?

1

What is the output node number for this component?

3

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 17 of type DELY. Do you wish to change anything? (yes or no)

First input node: 1

Output node: 3

Numerical format: FLOT

16 bit or 32 bit size: 32
Clock cycle(s): 1

NO

Select a component type for component 18.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

D

Component number 18 is of type: DELY. What is the one input node number for this component?

2

What is the output node number for this component?

4

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 18 of type DELY. Do you wish to change anything? (yes or no)

First input node: 2
Output node: 4
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock cycle(s): 1

NO

Select a component type for component 19.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

D

Component number 19 is of type: DELY. What is the one input node number for this component?

3

What is the output node number for this component?

5

What numerical format is desired for this format?

- A floating point

A B fixed point
 Should the component be 16 bit or 32 bit?
 A 16
 B 32
 B
 How many clock cycles is this chip?
 0
 The following parameters have been specified for component 19 of
 type DELY. Do you wish to change anything? (yes or no)
 First input node: 3
 Output node: 5
 Numerical format: FLOT
 16 bit or 32 bit size: ?2
 Clock cycle(s): 0
 NO
 Select a component type for component 20.
 A Cell (this is a heading for chips to then be specified)
 B Add Chip
 C Multiply Chip
 D Delay Chip
 E Look Up Chip
 F quit (terminate structure entry)
 D
 Component number 20 is of type: DELY. What is the one input
 node number for this component?
 4
 What is the output node number for this component?
 6
 What numerical format is desired for this format?
 A floating point
 B fixed point
 A
 Should the component be 16 bit or 32 bit?
 A 16
 B 32
 B
 How many clock cycles is this chip?
 0
 The following parameters have been specified for component 20 of
 type DELY. Do you wish to change anything? (yes or no)
 First input node: 4
 Output node: 6
 Numerical format: FLOT
 16 bit or 32 bit size: 32
 Clock cycle(s): 0
 NO
 Select a component type for component 21.
 A Cell (this is a heading for chips to then be specified)

- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

C

Component number 21 is of type: MULT. What is input node number 1 for this component?

3

Component number 21 is of type: MULT. What is input node number 2 for this component?

5

What is the output node number for this component?

7

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 21 of type MULT. Do you wish to change anything? (yes or no)

First input node: 3
 Second input node: 5
 Output node: 7
 Numerical format: FLOT
 16 bit or 32 bit size: 32
 Clock Cycle(s): 1

NO

Select a component type for component 22.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

C

Component number 22 is of type: MULT. What is input node number 1 for this component?

4

Component number 22 is of type: MULT. What is input node number 2 for this component?

6

What is the output node number for this component?

8

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 22 of type MULT. Do you wish to change anything? (yes or no)

First input node: 4
Second input node: 6
Output node: 8
Numerical format: FLOT
16 bit or 32 bit size: 32
Clock Cycle(s): 1

NO

Select a component type for component 23.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

B

Component number 23 is of type: ADDR. What is input node number 1 for this component?

7

Component number 23 is of type: ADDR. What is input node number 2 for this component?

8

What is the output node number for this component?

9

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 23 of type ADDR. Do you wish to change anything? (yes or no)

First input node: 7

Second input node: 8
 Output node: 9
 Numerical format: FLOT
 16 bit or 32 bit size: 32
 Clock Cycle(s): 1

NO

Select a component type for component 24.
 A Cell (this is a heading for chips to then be specified)
 B Add Chip
 C Multiply Chip
 D Delay Chip
 E Look Up Chip
 F quit (terminate structure entry)

F

AT THIS TIME, DO YOU WANT TO:
 A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
 B GENERATE A NEW SYSTEM SPECIFICATION FILE.
 C GENERATE A NEW TEST RUN SPECIFICATION FILE.
 D EXIT FROM EMUL

D

\$ TYPE EXPSYS.SSF

ONFIGURATIN

1	0	101	FLOT	DELY	32	0
2	0	102	FLOT	DELY	32	0
3	0	201	FLOT	DELY	32	0
4	0	202	FLOT	DELY	32	0
109	0	5	FLOT	DELY	32	1
209	0	6	FLOT	LOOK	32	1
5	6	7	FLOT	MULT	32	1
2	1	7				
1	0	3	FLOT	DELY	32	1
2	0	4	FLOT	DELY	32	1
3	0	5	FLOT	DELY	32	0
4	0	6	FLOT	DELY	32	0
3	5	7	FLOT	MULT	32	1
4	6	8	FLOT	MULT	32	1
7	8	9	FLOT	ADDR	32	1
2	1	7				
1	0	3	FLOT	DELY	32	1
2	0	4	FLOT	DELY	32	1
3	0	5	FLOT	DELY	32	0
4	0	6	FLOT	DELY	32	0
3	5	7	FLOT	MULT	32	1
4	6	8	FLOT	MULT	32	1
7	8	9	FLOT	ADDR	32	1

\$ RUN EMUL

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM EMUL. EMUL IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USER IN THE

INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND
PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A
CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A
RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST
OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

C

WHAT IS THE NAME OF THE EXPERIMENT SPECIFICATION FILE
TO BE OPENED FOR WRITING?

EXPSYS.TSF

At this time EMUL requires a general knowledge of the system that
will now be tested. How many input snapshots of the input data do
you want to process?

1

What are the total number of chips in the system you are
specifying, that are not located within a cell?

7

What are the total number of cells in the array processor?

2

The following parameters have been specified for this system. Do you wish to
change anything?(yes or no)

Number of snapshots: 1
Number of chips: 7
Number of cells: 2

NO

For each input node of snap no. enter a line
of input containing input node number, input data
value and chip to which this data enters.

How many input nodes will you enter at this time?

4

ENTER 4 LINES OF INPUT DATA AT THIS TIME
(input node no., data value, input chip no.)

1 1 1
2 2 2
3 3 3
4 4 4

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

```

D
$ TYPE EXPSYS.TSF
XPERIMENT
1
7
2
1      1      1
2      2      2
3      3      3
4      4      4
1      0      0
$ RUN EMUL

```

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM EMUL. EMUL IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

- HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
- EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
- BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

A

WHAT IS THE NAME OF THE INPUT EMU FILE?

EXPSYS.TSF

WHAT IS THE NAME OF THE OUTPUT FILE?

EXPSYS.OUT

WHAT IS THE NAME OF THE INPUT CHIP FILE?

EXPSYS.SSF

WHAT IS THE SPECIAL VISIBLE CHIP INPUT FILE

(ENTER 'NONE' IF THERE IS NONE)

(THE SPECIAL VISIBLE OUTPUT IS ALWAYS WRITTEN TO FILE 'SPVIS.OUT') ?

NONE

PULSING THE DATA...

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

D

\$ TYPE EXPSYS.OUT

*****THE SYSTOLIC EMULATOR HAS BEEN ACTIVATED*****

THE FOLLOWING INFORMATION REGARDING EACH ELEMENT HAS BEEN GIVEN TO THE EMULATOR

CHIP NUMBER	INPUT NODES NUMBERS	OUTPUT NODE NUMBER	CHIP OPERATION	CHIP CLOCK CYCLES
1	1 0	101	Delay (Time Shift)	0
2	2 0	102	Delay (Time Shift)	0
3	3 0	201	Delay (Time Shift)	0
4	4 0	202	Delay (Time Shift)	0
5	109 0	5	Delay (Time Shift)	1
6	209 0	6	Look Up: Sq Root Recip.	1
7	5 6	7	Multiplication	1

SNAPSHOT NUMBER 1 HAS BEGUN

The following data has been accepted by the emulator for input as follows:

Input Node Number Actual Data Value

1			1.00		
2			2.00		
3			3.00		
4			4.00		
101	1 0	3		Delay (Time Shift)	1
102	2 0	4		Delay (Time Shift)	1
103	3 0	5		Delay (Time Shift)	0
104	4 0	6		Delay (Time Shift)	0
105	3 5	7		Multiplication	1
106	4 6	8		Multiplication	1
107	7 8	9		Addition	1
201	1 0	3		Delay (Time Shift)	1
202	2 0	4		Delay (Time Shift)	1
203	3 0	5		Delay (Time Shift)	0
204	4 0	6		Delay (Time Shift)	0
205	3 5	7		Multiplication	1
206	4 6	8		Multiplication	1
207	7 8	9		Addition	1

ELEMENTS HAVE BEEN GROUPED ACCORDING TO INPUT READINESS.
PROCESSING ACCORDING TO SPECIFIED OPERATION CAN NOW BEGIN!

SNAPSHOT 1 SHALL NOW BEGIN

////////////////////////////////////

Cycle 1 of snapshot 1 is ready to process

8 elements will output data.

These Chips are:

1. Chip Number 1
 OUTPUT OF DELAY CHIP 1 IS 1.00
 IT HAS A DELAY OF 0 CLOCK CYCLES
 OUTPUT OF CHIP 1 IS 1.00
2. Chip Number 2
 OUTPUT OF DELAY CHIP 2 IS 2.00

IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 2 IS 2.00

3. Chip Number 3
OUTPUT OF DELAY CHIP 3 IS 3.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 3 IS 3.00

4. Chip Number 4
OUTPUT OF DELAY CHIP 4 IS 4.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 4 IS 4.00

5. Chip Number 101
OUTPUT OF DELAY CHIP 101 IS 1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 101 IS 1.00

6. Chip Number 102
OUTPUT OF DELAY CHIP 102 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 102 IS 2.00

7. Chip Number 201
OUTPUT OF DELAY CHIP 201 IS 3.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 201 IS 3.00

8. Chip Number 202
OUTPUT OF DELAY CHIP 202 IS 4.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 202 IS 4.00

////////////////////////////////////
////////////////////////////////////
////////////////////////////////////

Cycle 2 of snapshot 1 is ready to process
8 elements will output data.

These Chips are:

1. Chip Number 103
OUTPUT OF DELAY CHIP 103 IS 1.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 103 IS 1.00

2. Chip Number 104
OUTPUT OF DELAY CHIP 104 IS 2.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 104 IS 2.00

3. Chip Number 203
OUTPUT OF DELAY CHIP 203 IS 3.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 203 IS 3.00

4. Chip Number 204
OUTPUT OF DELAY CHIP 204 IS 4.00
IT HAS A DELAYOF 0 CLOCK CYCLES

OUTPUT OF CHIP 204 IS 4.00

5. Chip Number 105
1.00 * 1.00 = 1.00
OUTPUT OF CHIP 105 IS 1.00

6. Chip Number 106
2.00 * 2.00 = 4.00
OUTPUT OF CHIP 106 IS 4.00

7. Chip Number 205
3.00 * 3.00 = 9.00
OUTPUT OF CHIP 205 IS 9.00

8. Chip Number 206
4.00 * 4.00 = 16.0
OUTPUT OF CHIP 206 IS 16.0

////////////////////////////////////
////////////////////////////////////
////////////////////////////////////

Cycle 3 of snapshot 1 is ready to process
2 elements will output data.

These Chips are:

1. Chip Number 107
1.00 + 4.00 = 5.00
OUTPUT OF CHIP 107 IS 5.00

2. Chip Number 207
9.00 + 16.0 = 25.0
OUTPUT OF CHIP 207 IS 25.0

////////////////////////////////////
////////////////////////////////////
////////////////////////////////////

Cycle 4 of snapshot 1 is ready to process
2 elements will output data.

These Chips are:

1. Chip Number 5
OUTPUT OF DELAY CHIP 5 IS 5.00
IT HAS A DELAY OF 1 CLOCK CYCLES
OUTPUT OF CHIP 5 IS 5.00

2. Chip Number 6
OUTPUT OF CHIP 6 IS 0.200

////////////////////////////////////
////////////////////////////////////
////////////////////////////////////

Cycle 5 of snapshot 1 is ready to process
1 elements will output data.

These Chips are:

1. Chip Number 7
5.00 * 0.200 = 1.00
OUTPUT OF CHIP 7 IS 1.00

////////////////////////////////////
////////////////////////////////////

ALL AVAILABLE INPUT DATA HAS BEEN READ.

THE EMULATOR WILL NOW BE DEACTIVATED

\$ LP EXPSYS.SSF

\$ LP EXPSYS.TSF

\$ LP EXPSYS.OUT

\$ LOG

SMITHR logged out at 13-DEC-1989 08:28:52.95Connection closed by remote

Appendix C

Interactive Element Feedback Example Emulation File

```
Username: SMITHR
Password:
```

Last interactive login on Friday, 15-DEC-1989 10:14Z>

Lookup the phone number and office symbol of RADC personel, use the
 FIND command.

Send your MISVAX files to a LONEX printer, use the LP command.

To get information on special utilities installed on the 8650 cluster, type 'help @RADC' at the \$ prompt.

```

$ cd /usr/share/doc/ncurses5.9.20160214-1/examples/ncurses
$ DIR

```

BOTH.DIR;1	EMUL.DIR;1	GADAR.DIR;1	INFO.DIR;1
LOGIN.COM;4	LOGIN.COM;3	LOGIN.COM;2	LOGIN.JOU;1
SYSTEM.DIR;1			

```
$ SET DEF DM [SMITHR.EMUL]
$ DIR
```

ALGOR1.TSF;1	BACSUB.SSF;1	BACSUB.TSF;1	BNDCEL.SSF;1
BNDCEL.TSF;1	CACEL.SSF;1	CBACSB.SSF;1	CBNDC2.SSF;1
CBNDCL.SSF;1	CBNDCL.TSF;1	CCMCEL.SSF;1	CCOREL.SSF;1
CCOREL.TSF;1	CINTC2.SSF;1	CINTCL.SSF;1	CMCEL.SSF;1
CMJLCL.SSF;1	CMJLCL.TSF;1	CMXSOL.SSF;1	CMXSOL.TSF;1
COM.DIR;1	CORREL.SSF;1	CSMCEL.SSF;1	CSMI.SSF;1
CSMI.TSF;1	CVDCEL.SSF;1	CVMCEL.SSF;1	EMUL.EXE;1
EXPCEL.OUT;1	EXPCEL.SSF;1	EXPCEL.TSF;1	FOR000.DAT;1
GIV2.SSF;1	GIV2.TSF;1	GIV3.SSF;1	GIV3.TSF;1
GIV4.SSF;1	IDTCEL.SSF;1	IDTCEL.TSF;1	INTCEL.SSF;1
INTCEL.TSF;1	MATSOL.SSF;1	SMI.SSF;1	SOURCE.DIR;1
SPVIS.OUT;1	TEST.DIR;1	WTCEL.SSF;1	WTCEL.TSF;1

\$ RUN EMUL

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM EMUL. EMUL IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A

CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

B

WHAT IS THE NAME OF THE CONFIGURATIN SPECIFICATION FILE
TO BE OPENED FOR WRITING?
FEDBAK.SSF

Select a component type for component 1.

- A Cell (this is a heading for chips to then be specified)
- B Add Chip
- C Multiply Chip
- D Delay Chip
- E Look Up Chip
- F quit (terminate structure entry)

B

Component number 1 is of type: ADDR. What is input node
number 1for this component?

1

Component number 1 is of type: ADDR. What is input node
number 2for this component?

2

What is the output node number for this component?

2

What numerical format is desired for this format?

- A floating point
- B fixed point

A

Should the component be 16 bit or 32 bit?

- A 16
- B 32

B

How many clock cycles is this chip?

1

The following parameters have been specified for component 1 of
type ADDR. Do you wish to change anything? (yes or no)

First input node: 1
Second input node: 2
Output node: 2
Numerical format: FLOT
16 bit or 32 bit size: 32

Clock Cycle(s): 1
NO

Select a component type for component 2.
A Cell (this is a heading for chips to then be specified)
B Add Chip
C Multiply Chip
D Delay Chip
E Look Up Chip
F quit (terminate structure entry)

F

AT THIS TIME, DO YOU WANT TO:
A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
B GENERATE A NEW SYSTEM SPECIFICATION FILE.
C GENERATE A NEW TEST RUN SPECIFICATION FILE.
D EXIT FROM EMUL

D

\$ TYPE FEDBAK.SSF

ONFIGURATIN

1 2 2 FLOT ADDR 32 1

\$ RUN EMUL

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM EMUL. EMUL IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
B GENERATE A NEW SYSTEM SPECIFICATION FILE.
C GENERATE A NEW TEST RUN SPECIFICATION FILE.
D EXIT FROM EMUL

C

WHAT IS THE NAME OF THE EXPERIMENT SPECIFICATION FILE
TO BE OPENED FOR WRITING?
FEDBAK.TSF

At this time EMUL requires a general knowledge of the system that will now be tested. How many input snapshots of the input data do you want to process?

3


```

What are the total number of chips in the system you are
specifying, that are not located within a cell?
1

What are the total number of cells in the array processor?
0

The following parameters have been specified for this system. Do you wish to
change anything? (yes or no)
Number of snapshots:      3
Number of chips:          1
Number of cells:          0
NO

For each input node of snap no. 1 enter a line
of input containing input node number, input data
value and chip to which this data enters.

How many input nodes will you enter at this time?
2

ENTER 2 LINES OF INPUT DATA AT THIS TIME
(input node no., data value, input chip no.)
1 1 1
2 0 1

For each input node of snap no. 2 enter a line
of input containing input node number, input data
value and chip to which this data enters.

How many input nodes will you enter at this time?
1

ENTER 1 LINES OF INPUT DATA AT THIS TIME
(input node no., data value, input chip no.)
1 2 1

For each input node of snap no. 3 enter a line
of input containing input node number, input data
value and chip to which this data enters.

How many input nodes will you enter at this time?
1

ENTER 1 LINES OF INPUT DATA AT THIS TIME
(input node no., data value, input chip no.)
1 3 1

AT THIS TIME, DO YOU WANT TO:
A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
B GENERATE A NEW SYSTEM SPECIFICATION FILE.
C GENERATE A NEW TEST RUN SPECIFICATION FILE.
D EXIT FROM EMUL
D
$ TYPE FEDBAK.TSF
XPERIMENT
3
1
0

```

1	1	1
2	0	1
1	2	1
1	3	1
1	0	0

\$ RUN EMUL

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM EMUL. EMUL IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
 EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
 BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
 B GENERATE A NEW SYSTEM SPECIFICATION FILE.
 C GENERATE A NEW TEST RUN SPECIFICATION FILE.
 D EXIT FROM EMUL

A

WHAT IS THE NAME OF THE INPUT EMU FILE?

FEDBAK.TSF

WHAT IS THE NAME OF THE OUTPUT FILE?

FEDBAK.OUT

WHAT IS THE NAME OF THE INPUT CHIP FILE?

FEDBAK.SSF

WHAT IS THE SPECIAL VISIBLE CHIP INPUT FILE

(ENTER 'NONE' IF THERE IS NONE)

(THE SPECIAL VISIBLE OUTPUT IS ALWAYS WRITTEN TO FILE 'SPVIS.OUT') ?

NONE

PULSING THE DATA...

AT THIS TIME, DO YOU WANT TO:

A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
 B GENERATE A NEW SYSTEM SPECIFICATION FILE.
 C GENERATE A NEW TEST RUN SPECIFICATION FILE.
 D EXIT FROM EMUL

D

\$ TYPE FEDBAK.OUT

*****THE SYSTOLIC EMULATOR HAS BEEN ACTIVATED*****

THE FOLLOWING INFORMATION REGARDING EACH ELEMENT HAS BEEN GIVEN TO THE EMULATOR

CHIP NUMBER	INPUT NODES NUMBERS	OUTPUT NODE NUMBER	CHIP OPERATION	CHIP CLOCK CYCLES
-------------	------------------------	-----------------------	----------------	-------------------

1	1	2	2	Addition	1
---	---	---	---	----------	---

SNAPSHOT NUMBER 1 HAS BEGUN

The following data has been accepted by the emulator for input as follows:

Input Node Number	Actual Data Value
1	1.00
2	0.00

ELEMENTS HAVE BEEN GROUPED ACCORDING TO INPUT READINESS.
PROCESSING ACCORDING TO SPECIFIED OPERATION CAN NOW BEGIN!

SNAPSHOT 1 SHALL NOW BEGIN

////////////////////////////////////

Cycle 1 of snapshot 1 is ready to process
1 elements will output data.

These Chips are:

1. Chip Number	1			
	1.00	+	0.000E+00=	1.00
OUTPUT OF CHIP	1	IS		1.00

////////////////////////////////////
////////////////////////////////////

SNAPSHOT NUMBER 2 HAS BEGUN

The following data has been accepted by the emulator for input as follows:

Input Node Number	Actual Data Value
1	2.00

SNAPSHOT 2 SHALL NOW BEGIN

////////////////////////////////////

Cycle 1 of snapshot 2 is ready to process
1 elements will output data.

These Chips are:

1. Chip Number	1			
	2.00	+	1.00	= 3.00
OUTPUT OF CHIP	1	IS		3.00

////////////////////////////////////
////////////////////////////////////

SNAPSHOT NUMBER 3 HAS BEGUN

The following data has been accepted by the emulator for input as follows:

Input Node Number	Actual Data Value
-------------------	-------------------

1

3.00

SNAPSHOT 3 SHALL NOW BEGIN
////////////////////////////////////

Cycle 1 of snapshot 3 is ready to process
1 elements will output data.

These Chips are:

1. Chip Number 1
3.00 + 3.00 = 6.00
OUTPUT OF CHIP 1 IS 6.00

////////////////////////////////////
////////////////////////////////////

ALL AVAILABLE INPUT DATA HAS BEEN READ.
THE EMULATOR WILL NOW BE DEACTIVATED

\$ LOG
SMITHR logged out at 15-DEC-1989 11:03:41.29 Connection closed by remote

Appendix D

Associated SMI Processor Emulation Files

2	0	2
3	1	3
4	0	4
5	3	5
6	1	6
7	-1	7
1	0	1
2	-1	2
3	2	3
4	0	4
5	3	5
6	-3	6
7	-1	7
1	1	1
2	-1	2
3	1	3
4	2	4
5	5	5
6	1	6
7	-1	7
1	2	1
2	3	2
3	-1	3
4	-1	4
5	-3	5
6	5	6
7	-1	7
1	0	0

\$ dir

Directory DCSDISK2:[SMITHR]

ALGOR1.SSF;1
GADAR.DIR;1
LOGIN.COM;2

ALGOR1.TSF;1
INFO.DIR;1
LOGIN.JOU;1

BOTH.DIR;1
LOGIN.COM;4
SYSTEM.DIR;1

EMUL.DIR;1
LOGIN.COM;3

Total of 11 files.

\$ type algor1.ssf

CONFIGURATIN

1	0	101	FLOT	DELY	32	0
2	0	102	FLOT	DELY	32	0
3	0	401	FLOT	DELY	32	0
4	0	402	FLOT	DELY	32	0
5	0	603	FLOT	DELY	32	0
6	0	604	FLOT	DELY	32	0
7	0	605	FLOT	DELY	32	0
101	0	201	FLOT	DELY	32	0
401	0	301	FLOT	DELY	32	0
102	0	202	FLOT	DELY	32	0
402	0	204	FLOT	DELY	32	0
402	0	302	FLOT	DELY	32	0
401	0	203	FLOT	DELY	32	0
603	0	503	FLOT	DELY	32	0
401	0	601	FLOT	DELY	32	0
101	0	303	FLOT	DELY	32	0
101	0	501	FLOT	DELY	32	0
604	0	504	FLOT	DELY	32	0
102	0	304	FLOT	DELY	32	0
102	0	502	FLOT	DELY	32	0
402	0	602	FLOT	DELY	32	0

605	0	205	FLOT	DELY	32	0
605	0	305	FLOT	DELY	32	0
605	0	505	FLOT	DELY	32	0
115	0	701	FLOT	DELY	32	0
230	0	703	FLOT	DELY	32	0
231	0	704	FLOT	DELY	32	0
330	0	807	FLOT	DELY	32	0
331	0	808	FLOT	DELY	32	0
415	0	702	FLOT	DELY	32	0
530	0	805	FLOT	DELY	32	0
531	0	806	FLOT	DELY	32	0
630	0	905	FLOT	DELY	32	0
631	0	906	FLOT	DELY	32	0
605	0	909	FLOT	DELY	32	8
909	0	705	FLOT	DELY	32	0
701	0	802	FLOT	DELY	32	0
702	0	902	FLOT	DELY	32	0
805	0	903	FLOT	DELY	32	0
806	0	904	FLOT	DELY	32	0
703	0	907	FLOT	DELY	32	0
704	0	908	FLOT	DELY	32	0
905	0	803	FLOT	DELY	32	0
906	0	804	FLOT	DELY	32	0
909	0	809	FLOT	DELY	32	0
722	0	801	FLOT	DELY	32	0
722	0	901	FLOT	DELY	32	0
2	1	13				
1	0	3	FLOT	DELY	32	1
2	0	4	FLOT	DELY	32	1
3	0	5	FLOT	DELY	32	0
4	0	6	FLOT	DELY	32	0
3	5	7	FLOT	MULT	32	1
6	4	8	FLOT	MULT	32	1
7	8	9	FLOT	ADDR	32	1
9	0	10	FLOT	DELY	32	1
10	0	11	FLOT	DELY	32	1
10	9	12	FLOT	ADDR	32	1
11	0	13	FLOT	DELY	32	1
13	11	14	FLOT	ADDR	32	1
14	12	15	FLOT	ADDR	32	1
5	2	26				
1	0	6	FLOT	DELY	32	0
2	0	7	FLOT	DELY	32	0
3	0	8	FLOT	DELY	32	0
4	0	9	FLOT	DELY	32	0
5	0	10	FLOT	DELY	32	1
6	8	11	FLOT	MULT	32	1
7	9	12	FLOT	MULT	32	1
8	7	13	FLOT	MULT	32	1
9	6	14	FLOT	MULT	32	1
11	12	15	FLOT	ADDR	32	1
13	10	16	FLOT	MULT	32	1
14	0	17	FLOT	DELY	32	1
15	0	18	FLOT	DELY	32	1
16	17	19	FLOT	ADDR	32	1
18	0	20	FLOT	DELY	32	1
19	0	21	FLOT	DELY	32	1
20	0	22	FLOT	DELY	32	1
20	18	23	FLOT	ADDR	32	1
19	21	24	FLOT	ADDR	32	1

21	0	25	FLOT	DELY	32	1
22	0	26	FLOT	DELY	32	1
25	0	27	FLOT	DELY	32	1
26	22	28	FLOT	ADDR	32	1
25	27	29	FLOT	ADDR	32	1
28	23	30	FLOT	ADDR	32	1
24	29	31	FLOT	ADDR	32	1
5	2	26				
1	0	6	FLOT	DELY	32	0
2	0	7	FLOT	DELY	32	0
3	0	8	FLOT	DELY	32	0
4	0	9	FLOT	DELY	32	0
5	0	10	FLOT	DELY	32	1
6	8	11	FLOT	MULT	32	1
7	9	12	FLOT	MULT	32	1
8	7	13	FLOT	MULT	32	1
9	6	14	FLOT	MULT	32	1
11	12	15	FLOT	ADDR	32	1
13	10	16	FLOT	MULT	32	1
14	0	17	FLOT	DELY	32	1
15	0	18	FLOT	DELY	32	1
16	17	19	FLOT	ADDR	32	1
18	0	20	FLOT	DELY	32	1
19	0	21	FLOT	DELY	32	1
20	0	22	FLOT	DELY	32	1
20	18	23	FLOT	ADDR	32	1
19	21	24	FLOT	ADDR	32	1
21	0	25	FLOT	DELY	32	1
22	0	26	FLOT	DELY	32	1
25	0	27	FLOT	DELY	32	1
26	22	28	FLOT	ADDR	32	1
25	27	29	FLOT	ADDR	32	1
28	23	30	FLOT	ADDR	32	1
24	29	31	FLOT	ADDR	32	1
2	1	13				
1	0	3	FLOT	DELY	32	1
2	0	4	FLOT	DELY	32	1
3	0	5	FLOT	DELY	32	0
4	0	6	FLOT	DELY	32	0
3	5	7	FLOT	MULT	32	1
6	4	8	FLOT	MULT	32	1
7	8	9	FLOT	ADDR	32	1
9	0	10	FLOT	DELY	32	1
10	0	11	FLOT	DELY	32	1
10	9	12	FLOT	ADDR	32	1
11	0	13	FLOT	DELY	32	1
13	11	14	FLOT	ADDR	32	1
14	12	15	FLOT	ADDR	32	1
5	2	26				
1	0	6	FLOT	DELY	32	0
2	0	7	FLOT	DELY	32	0
3	0	8	FLOT	DELY	32	0
4	0	9	FLOT	DELY	32	0
5	0	10	FLOT	DELY	32	1
6	8	11	FLOT	MULT	32	1
7	9	12	FLOT	MULT	32	1
8	7	13	FLOT	MULT	32	1
9	6	14	FLOT	MULT	32	1
11	12	15	FLOT	ADDR	32	1
13	10	16	FLOT	MULT	32	1

14	0	17	FLOT	DELY	32	1
15	0	18	FLOT	DELY	32	1
16	17	19	FLOT	ADDR	32	1
18	0	20	FLOT	DELY	32	1
19	0	21	FLOT	DELY	32	1
20	0	22	FLOT	DELY	32	1
20	18	23	FLOT	ADDR	32	1
19	21	24	FLOT	ADDR	32	1
21	0	25	FLOT	DELY	32	1
22	0	26	FLOT	DELY	32	1
25	0	27	FLOT	DELY	32	1
26	22	28	FLOT	ADDR	32	1
25	27	29	FLOT	ADDR	32	1
28	23	30	FLOT	ADDR	32	1
24	29	31	FLOT	ADDR	32	1
5	2	26				
1	0	6	FLOT	DELY	32	0
2	0	7	FLOT	DELY	32	0
3	0	8	FLOT	DELY	32	0
4	0	9	FLOT	DELY	32	0
5	0	10	FLOT	DELY	32	1
6	8	11	FLOT	MULT	32	1
7	9	12	FLOT	MULT	32	1
8	7	13	FLOT	MULT	32	1
9	6	14	FLOT	MULT	32	1
11	12	15	FLOT	ADDR	32	1
13	10	16	FLOT	MULT	32	1
14	0	17	FLOT	DELY	32	1
15	0	18	FLOT	DELY	32	1
16	17	19	FLOT	ADDR	32	1
18	0	20	FLOT	DELY	32	1
19	0	21	FLOT	DELY	32	1
20	0	22	FLOT	DELY	32	1
20	18	23	FLOT	ADDR	32	1
19	21	24	FLOT	ADDR	32	1
21	0	25	FLOT	DELY	32	1
22	0	26	FLOT	DELY	32	1
25	0	27	FLOT	DELY	32	1
26	22	28	FLOT	ADDR	32	1
25	27	29	FLOT	ADDR	32	1
28	23	30	FLOT	ADDR	32	1
24	29	31	FLOT	ADDR	32	1
5	1	17				
1	0	6	FLOT	DELY	32	0
2	0	7	FLOT	DELY	32	0
3	0	8	FLOT	DELY	32	1
4	0	9	FLOT	DELY	32	1
5	0	10	FLOT	DELY	32	3
6	7	11	FLOT	MULT	32	1
11	0	12	FLOT	DELY	32	3
8	0	13	FLOT	DELY	32	0
9	0	14	FLOT	DELY	32	0
8	13	15	FLOT	MULT	32	1
9	14	16	FLOT	MULT	32	1
15	16	17	FLOT	ADDR	32	1
17	10	18	FLOT	MULT	32	1
12	18	19	FLOT	ADDR	32	1
19	0	20	FLOT	DELY	32	0
19	20	21	FLOT	MULT	32	1
21	0	22	FLOT	LOOK	32	1

9	2	32				
1	0	10	FLOT	DELY	32	0
2	0	11	FLOT	DELY	32	0
3	0	12	FLOT	DELY	32	0
4	0	13	FLOT	DELY	32	0
5	0	14	FLOT	DELY	32	0
6	0	15	FLOT	DELY	32	0
7	0	16	FLOT	DELY	32	0
8	0	17	FLOT	DELY	32	0
9	0	18	FLOT	DELY	32	1
12	11	19	FLOT	MULT	32	1
13	11	20	FLOT	MULT	32	1
14	16	21	FLOT	MULT	32	1
15	17	22	FLOT	MULT	32	1
16	15	23	FLOT	MULT	32	1
17	14	24	FLOT	MULT	32	1
18	0	25	FLOT	DELY	32	2
19	0	26	FLOT	DELY	32	3
20	0	27	FLOT	DELY	32	3
21	0	28	FLOT	DELY	32	1
22	18	29	FLOT	MULT	32	1
23	0	30	FLOT	DELY	32	1
24	0	31	FLOT	DELY	32	1
28	29	32	FLOT	ADDR	32	1
30	31	33	FLOT	ADDR	32	1
32	25	34	FLOT	MULT	32	1
25	33	35	FLOT	MULT	32	1
26	34	36	FLOT	ADDR	32	1
27	35	37	FLOT	ADDR	32	1
36	0	38	FLOT	DELY	32	2
37	0	39	FLOT	DELY	32	2
10	38	40	FLOT	MULT	32	1
10	39	41	FLOT	MULT	32	1
9	2	32				
1	0	10	FLOT	DELY	32	0
2	0	11	FLOT	DELY	32	0
3	0	12	FLOT	DELY	32	0
4	0	13	FLOT	DELY	32	0
5	0	14	FLOT	DELY	32	0
6	0	15	FLOT	DELY	32	0
7	0	16	FLOT	DELY	32	0
8	0	17	FLOT	DELY	32	0
9	0	18	FLOT	DELY	32	1
12	11	19	FLOT	MULT	32	1
13	11	20	FLOT	MULT	32	1
14	16	21	FLOT	MULT	32	1
15	17	22	FLOT	MULT	32	1
16	15	23	FLOT	MULT	32	1
17	14	24	FLOT	MULT	32	1
18	0	25	FLOT	DELY	32	2
19	0	26	FLOT	DELY	32	3
20	0	27	FLOT	DELY	32	3
21	0	28	FLOT	DELY	32	1
22	18	29	FLOT	MULT	32	1
23	0	30	FLOT	DELY	32	1
24	0	31	FLOT	DELY	32	1
28	29	32	FLOT	ADDR	32	1
30	31	33	FLOT	ADDR	32	1
32	25	34	FLOT	MULT	32	1
25	33	35	FLOT	MULT	32	1

26	34	36	FLOT	ADDR	32	1
27	35	37	FLOT	ADDR	32	1
36	0	38	FLOT	DELY	32	2
37	0	39	FLOT	DELY	32	2
10	38	40	FLOT	MULT	32	1
10	39	41	FLOT	MULT	32	1

\$ log
SMITHR logged out at 21-DEC-1989 14:10:57.49Connection closed by remote ho

Welcome to VAX/VMS V5.2

Username: SMITHR

Password:

Welcome to VAX/VMS version V5.2 on node MISVX1

Last interactive login on Friday, 22-DEC-1989 07:51Z>

.....
Lookup the phone number and office symbol of RADC personel, use the
FIND command.

Send your MISVAX files to a LONEX printer, use the LP command.

To get information on special utilities installed on the 8650 cluster,
type 'help @RADC' at the \$ prompt.

.....
\$ SET DEF [SMITHR.EMUL]
\$ DIR

Directory DC\$DISK2:[SMITHR.EMUL]

ALGOR1.OUT;1	ALGOR1.SSF;1	ALGOR1.TSF;1	BACSUB.SSF;1
BACSUB.TSF;1	BNDCEL.SSF;1	BNDCEL.TSF;1	BNDCL2.SSF;1
BNDCL2.TSF;1	CACEL.SSF;1	CBACSB.SSF;1	CBNDCL2.SSF;1
CBNDCL.SSF;1	CBNDCL.TSF;1	CCMCEL.SSF;1	CCOREL.SSF;1
CCOREL.TSF;1	CINTC2.SSF;1	CINTCL.SSF;1	CMCEL.SSF;1
CMULCL.SSF;1	CMULCL.TSF;1	CMXSOL.SSF;1	CMXSOL.TSF;1
COM.DIR;1	CORREL.SSF;1	CSMCEL.SSF;1	CSMI.SSF;1
CSMI.TSF;1	CVDCEL.SSF;1	CVMCEL.SSF;1	EMUL.EXE;1
EXPCEL.SSF;1	EXPCEL.TSF;1	FEDBAK.SSF;1	FEDBAK.TSF;1
GIV2.SSF;1	GIV2.TSF;1	GIV3.SSF;1	GIV3.TSF;1
GIV4.SSF;1	IDTCEL.SSF;1	IDTCEL.TSF;1	INTCEL.SSF;1
INTCEL.TSF;1	MATSOL.SSF;1	MUX.SSF;3	MUX.SSF;2
MUX.SSF;1	MUX.TSF;8	MUX.TSF;7	MUX.TSF;6
MUX.TSF;5	MUX.TSF;4	MUX.TSF;3	MUX.TSF;2
MUX.TSF;1	SMI.SSF;1	SOURCE.DIR;1	TEST.DIR;1
TYPE.;1	WTCEL.SSF;1	WTCEL.TSF;1	

Total of 63 files.

\$ RUN EMUL

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM EMUL. EMUL IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
 EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
 BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

A

WHAT IS THE NAME OF THE INPUT EMU FILE?

ALGOR1.TSF

WHAT IS THE NAME OF THE OUTPUT FILE?

ALGOR1.OUT

WHAT IS THE NAME OF THE INPUT CHIP FILE?

ALGOR1.SSF

WHAT IS THE SPECIAL VISIBLE CHIP INPUT FILE

(ENTER 'NONE' IF THERE IS NONE)

(THE SPECIAL VISIBLE OUTPUT IS ALWAYS WRITTEN TO FILE 'SPVIS.OUT') ?

NONE

PULSING THE DATA...

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW TEST RUN SPECIFICATION FILE.
- D EXIT FROM EMUL

D

\$ TYPE ALGOR1.OUT

*****THE SYSTOLIC EMULATOR HAS BEEN ACTIVATED*****

THE FOLLOWING INFORMATION REGARDING EACH ELEMENT HAS BEEN GIVEN TO THE EMULATOR

CHIP NUMBER	INPUT NODES NUMBERS	OUTPUT NODE NUMBER	CHIP OPERATION	CHIP CLOCK CYCLES
1	1 0	101	Delay (Time Shift)	0
2	2 0	102	Delay (Time Shift)	0
3	3 0	401	Delay (Time Shift)	0
4	4 0	402	Delay (Time Shift)	0
5	5 0	603	Delay (Time Shift)	0
6	6 0	604	Delay (Time Shift)	0
7	7 0	605	Delay (Time Shift)	0
8	101 0	201	Delay (Time Shift)	0
9	401 0	301	Delay (Time Shift)	0
10	102 0	202	Delay (Time Shift)	0
11	402 0	204	Delay (Time Shift)	0
12	402 0	302	Delay (Time Shift)	0
13	401 0	203	Delay (Time Shift)	0
14	603 0	503	Delay (Time Shift)	0
15	401 0	601	Delay (Time Shift)	0
16	101 0	303	Delay (Time Shift)	0
17	101 0	501	Delay (Time Shift)	0
18	604 0	504	Delay (Time Shift)	0
19	102 0	304	Delay (Time Shift)	0
20	102 0	502	Delay (Time Shift)	0
21	402 0	602	Delay (Time Shift)	0
22	605 0	205	Delay (Time Shift)	0
23	605 0	305	Delay (Time Shift)	0
24	605 0	505	Delay (Time Shift)	0

25	115	0	701	Delay (Time Shift)	0
26	230	0	703	Delay (Time Shift)	0
27	231	0	704	Delay (Time Shift)	0
28	330	0	807	Delay (Time Shift)	0
29	331	0	808	Delay (Time Shift)	0
30	415	0	702	Delay (Time Shift)	0
31	530	0	805	Delay (Time Shift)	0
32	531	0	806	Delay (Time Shift)	0
33	630	0	905	Delay (Time Shift)	0
34	631	0	906	Delay (Time Shift)	0
35	605	0	909	Delay (Time Shift)	8
36	909	0	705	Delay (Time Shift)	0
37	701	0	802	Delay (Time Shift)	0
38	702	0	902	Delay (Time Shift)	0
39	805	0	903	Delay (Time Shift)	0
40	806	0	904	Delay (Time Shift)	0
41	703	0	907	Delay (Time Shift)	0
42	704	0	908	Delay (Time Shift)	0
43	905	0	803	Delay (Time Shift)	0
44	906	0	804	Delay (Time Shift)	0
45	909	0	809	Delay (Time Shift)	0
46	722	0	801	Delay (Time Shift)	0
47	722	0	901	Delay (Time Shift)	0

SNAPSHOT NUMBER 1 HAS BEGUN

The following data has been accepted by the emulator for input as follows:

Input Node Number	Actual Data Value				
1	2.00				
2	0.00				
3	1.00				
4	0.00				
5	2.00				
6	-1.00				
7	-1.00				
101	1	0	3	Delay (Time Shift)	1
102	2	0	4	Delay (Time Shift)	1
103	3	0	5	Delay (Time Shift)	0
104	4	0	6	Delay (Time Shift)	0
105	3	5	7	Delay (Time Shift)	1
106	6	4	8	Delay (Time Shift)	1
107	7	8	9	Delay (Time Shift)	1
108	9	0	10	Delay (Time Shift)	1
109	10	0	11	Delay (Time Shift)	1
110	10	9	12	Delay (Time Shift)	1
111	11	0	13	Delay (Time Shift)	1
112	13	11	14	Delay (Time Shift)	1
113	14	12	15	Delay (Time Shift)	1
201	1	0	6	Delay (Time Shift)	0
202	2	0	7	Delay (Time Shift)	0
203	3	0	8	Delay (Time Shift)	0
204	4	0	9	Delay (Time Shift)	0
205	5	0	10	Delay (Time Shift)	1
206	6	8	11	Delay (Time Shift)	1
207	7	9	12	Delay (Time Shift)	1
208	8	7	13	Delay (Time Shift)	1
209	9	6	14	Delay (Time Shift)	1
210	11	12	15	Delay (Time Shift)	1
211	13	10	16	Delay (Time Shift)	1

212	14	0	17	Delay (Time Shift)	1
213	15	0	18	Delay (Time Shift)	1
214	16	17	19	Delay (Time Shift)	1
215	18	0	20	Delay (Time Shift)	1
216	19	0	21	Delay (Time Shift)	1
217	20	0	22	Delay (Time Shift)	1
218	20	18	23	Delay (Time Shift)	1
219	19	21	24	Delay (Time Shift)	1
220	21	0	25	Delay (Time Shift)	1
221	22	0	26	Delay (Time Shift)	1
222	25	0	27	Delay (Time Shift)	1
223	26	22	28	Delay (Time Shift)	1
224	25	27	29	Delay (Time Shift)	1
225	28	23	30	Delay (Time Shift)	1
226	24	29	31	Delay (Time Shift)	1
301	1	0	6	Delay (Time Shift)	0
302	2	0	7	Delay (Time Shift)	0
303	3	0	8	Delay (Time Shift)	0
304	4	0	9	Delay (Time Shift)	0
305	5	0	10	Delay (Time Shift)	1
306	6	8	11	Delay (Time Shift)	1
307	7	9	12	Delay (Time Shift)	1
308	8	7	13	Delay (Time Shift)	1
309	9	6	14	Delay (Time Shift)	1
310	11	12	15	Delay (Time Shift)	1
311	13	10	16	Delay (Time Shift)	1
312	14	0	17	Delay (Time Shift)	1
313	15	0	18	Delay (Time Shift)	1
314	16	17	19	Delay (Time Shift)	1
315	18	0	20	Delay (Time Shift)	1
316	19	0	21	Delay (Time Shift)	1
317	20	0	22	Delay (Time Shift)	1
318	20	18	23	Delay (Time Shift)	1
319	19	21	24	Delay (Time Shift)	1
320	21	0	25	Delay (Time Shift)	1
321	22	0	26	Delay (Time Shift)	1
322	25	0	27	Delay (Time Shift)	1
323	26	22	28	Delay (Time Shift)	1
324	25	27	29	Delay (Time Shift)	1
325	28	23	30	Delay (Time Shift)	1
326	24	29	31	Delay (Time Shift)	1
401	1	0	3	Delay (Time Shift)	1
402	2	0	4	Delay (Time Shift)	1
403	3	0	5	Delay (Time Shift)	0
404	4	0	6	Delay (Time Shift)	0
405	3	5	7	Delay (Time Shift)	1
406	6	4	8	Delay (Time Shift)	1
407	7	8	9	Delay (Time Shift)	1
408	9	0	10	Delay (Time Shift)	1
409	10	0	11	Delay (Time Shift)	1
410	10	9	12	Delay (Time Shift)	1
411	11	0	13	Delay (Time Shift)	1
412	13	11	14	Delay (Time Shift)	1
413	14	12	15	Delay (Time Shift)	1
501	1	0	6	Delay (Time Shift)	0
502	2	0	7	Delay (Time Shift)	0
503	3	0	8	Delay (Time Shift)	0
504	4	0	9	Delay (Time Shift)	0
505	5	0	10	Delay (Time Shift)	1
506	6	8	11	Delay (Time Shift)	1

507	7	9	12	Delay (Time Shift)	1
508	8	7	13	Delay (Time Shift)	1
509	9	6	14	Delay (Time Shift)	1
510	11	12	15	Delay (Time Shift)	1
511	13	10	16	Delay (Time Shift)	1
512	14	0	17	Delay (Time Shift)	1
513	15	0	18	Delay (Time Shift)	1
514	16	17	19	Delay (Time Shift)	1
515	18	0	20	Delay (Time Shift)	1
516	19	0	21	Delay (Time Shift)	1
517	20	0	22	Delay (Time Shift)	1
518	20	18	23	Delay (Time Shift)	1
519	19	21	24	Delay (Time Shift)	1
520	21	0	25	Delay (Time Shift)	1
521	22	0	26	Delay (Time Shift)	1
522	25	0	27	Delay (Time Shift)	1
523	26	22	28	Delay (Time Shift)	1
524	25	27	29	Delay (Time Shift)	1
525	28	23	30	Delay (Time Shift)	1
526	24	29	31	Delay (Time Shift)	1
601	1	0	6	Delay (Time Shift)	0
602	2	0	7	Delay (Time Shift)	0
603	3	0	8	Delay (Time Shift)	0
604	4	0	9	Delay (Time Shift)	0
605	5	0	10	Delay (Time Shift)	1
606	6	8	11	Delay (Time Shift)	1
607	7	9	12	Delay (Time Shift)	1
608	8	7	13	Delay (Time Shift)	1
609	9	6	14	Delay (Time Shift)	1
610	11	12	15	Delay (Time Shift)	1
611	13	10	16	Delay (Time Shift)	1
612	14	0	17	Delay (Time Shift)	1
613	15	0	18	Delay (Time Shift)	1
614	16	17	19	Delay (Time Shift)	1
615	18	0	20	Delay (Time Shift)	1
616	19	0	21	Delay (Time Shift)	1
617	20	0	22	Delay (Time Shift)	1
618	20	18	23	Delay (Time Shift)	1
619	19	21	24	Delay (Time Shift)	1
620	21	0	25	Delay (Time Shift)	1
621	22	0	26	Delay (Time Shift)	1
622	25	0	27	Delay (Time Shift)	1
623	26	22	28	Delay (Time Shift)	1
624	25	27	29	Delay (Time Shift)	1
625	28	23	30	Delay (Time Shift)	1
626	24	29	31	Delay (Time Shift)	1
701	1	0	6	Delay (Time Shift)	0
702	2	0	7	Delay (Time Shift)	0
703	3	0	8	Delay (Time Shift)	1
704	4	0	9	Delay (Time Shift)	1
705	5	0	10	Delay (Time Shift)	3
706	6	7	11	Delay (Time Shift)	1
707	11	0	12	Delay (Time Shift)	3
708	8	0	13	Delay (Time Shift)	0
709	9	0	14	Delay (Time Shift)	0
710	8	13	15	Delay (Time Shift)	1
711	9	14	16	Delay (Time Shift)	1
712	15	16	17	Delay (Time Shift)	1
713	17	10	18	Delay (Time Shift)	1
714	12	18	19	Delay (Time Shift)	1

715	19	0	20	Delay (Time Shift)	0
716	19	20	21	Delay (Time Shift)	1
717	21	0	22	Delay (Time Shift)	1
801	1	0	10	Delay (Time Shift)	0
802	2	0	11	Delay (Time Shift)	0
803	3	0	12	Delay (Time Shift)	0
804	4	0	13	Delay (Time Shift)	0
805	5	0	14	Delay (Time Shift)	0
806	6	0	15	Delay (Time Shift)	0
807	7	0	16	Delay (Time Shift)	0
808	8	0	17	Delay (Time Shift)	0
809	9	0	18	Delay (Time Shift)	1
810	12	11	19	Delay (Time Shift)	1
811	13	11	20	Delay (Time Shift)	1
812	14	16	21	Delay (Time Shift)	1
813	15	17	22	Delay (Time Shift)	1
814	16	15	23	Delay (Time Shift)	1
815	17	14	24	Delay (Time Shift)	1
816	18	0	25	Delay (Time Shift)	2
817	19	0	26	Delay (Time Shift)	3
818	20	0	27	Delay (Time Shift)	3
819	21	0	28	Delay (Time Shift)	1
820	22	18	29	Delay (Time Shift)	1
821	23	0	30	Delay (Time Shift)	1
822	24	0	31	Delay (Time Shift)	1
823	28	29	32	Delay (Time Shift)	1
824	30	31	33	Delay (Time Shift)	1
825	32	25	34	Delay (Time Shift)	1
826	25	33	35	Delay (Time Shift)	1
827	26	34	36	Delay (Time Shift)	1
828	27	35	37	Delay (Time Shift)	1
829	36	0	38	Delay (Time Shift)	2
830	37	0	39	Delay (Time Shift)	2
831	10	38	40	Delay (Time Shift)	1
832	10	39	41	Delay (Time Shift)	1
901	1	0	10	Delay (Time Shift)	0
902	2	0	11	Delay (Time Shift)	0
903	3	0	12	Delay (Time Shift)	0
904	4	0	13	Delay (Time Shift)	0
905	5	0	14	Delay (Time Shift)	0
906	6	0	15	Delay (Time Shift)	0
907	7	0	16	Delay (Time Shift)	0
908	8	0	17	Delay (Time Shift)	0
909	9	0	18	Delay (Time Shift)	1
910	12	11	19	Delay (Time Shift)	1
911	13	11	20	Delay (Time Shift)	1
912	14	16	21	Delay (Time Shift)	1
913	15	17	22	Delay (Time Shift)	1
914	16	15	23	Delay (Time Shift)	1
915	17	14	24	Delay (Time Shift)	1
916	18	0	25	Delay (Time Shift)	2
917	19	0	26	Delay (Time Shift)	3
918	20	0	27	Delay (Time Shift)	3
919	21	0	28	Delay (Time Shift)	1
920	22	18	29	Delay (Time Shift)	1
921	23	0	30	Delay (Time Shift)	1
922	24	0	31	Delay (Time Shift)	1
923	28	29	32	Delay (Time Shift)	1
924	30	31	33	Delay (Time Shift)	1
925	32	25	34	Delay (Time Shift)	1

926	25	33	35	Delay (Time Shift)	1
927	26	34	36	Delay (Time Shift)	1
928	27	35	37	Delay (Time Shift)	1
929	36	0	38	Delay (Time Shift)	2
930	37	0	39	Delay (Time Shift)	2
931	10	38	40	Delay (Time Shift)	1
932	10	39	41	Delay (Time Shift)	1

ELEMENTS HAVE BEEN GROUPED ACCORDING TO INPUT READINESS.
PROCESSING ACCORDING TO SPECIFIED OPERATION CAN NOW BEGIN!

SNAPSHOT NUMBER 8 HAS BEGUN

The following data has been accepted by the emulator for input as follows:

Input Node Number	Actual Data Value
1	2.00
2	3.00
3	-1.00
4	-1.00
5	-3.00
6	5.00
7	-1.00

SNAPSHOT 8SHALL NOW BEGIN

////////////////////////////////////

Cycle 8 of snapshot 1 is ready to process
11 elements will output data.

These Chips are:

- Chip Number 35
OUTPUT OF DELAY CHIP 35 IS -1.00
IT HAS A DELAYOF 8 CLOCK CYCLES
OUTPUT OF CHIP 35 IS -1.00
- Chip Number 113
OUTPUT OF DELAY CHIP 113 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 113 IS 2.00
- Chip Number 413
OUTPUT OF DELAY CHIP 413 IS 1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 413 IS 1.00
- Chip Number 225
OUTPUT OF DELAY CHIP 225 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 225 IS 2.00
- Chip Number 226
OUTPUT OF DELAY CHIP 226 IS -1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 226 IS -1.00
- Chip Number 325

OUTPUT OF DELAY CHIP 325 IS 1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 325 IS 1.00

7. Chip Number 326
OUTPUT OF DELAY CHIP 326 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 326 IS 2.00

8. Chip Number 525
OUTPUT OF DELAY CHIP 525 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 525 IS 2.00

9. Chip Number 526
OUTPUT OF DELAY CHIP 526 IS 1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 526 IS 1.00

10. Chip Number 625
OUTPUT OF DELAY CHIP 625 IS 1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 625 IS 1.00

11. Chip Number 626
OUTPUT OF DELAY CHIP 626 IS 1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 626 IS 1.00

////////////////////////////////////

Cycle 16 of snapshot 1 is ready to process
8 elements will output data.

These Chips are:

1. Chip Number 46
OUTPUT OF DELAY CHIP 46 IS 2.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 46 IS 2.00

2. Chip Number 47
OUTPUT OF DELAY CHIP 47 IS 2.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 47 IS 2.00

3. Chip Number 801
OUTPUT OF DELAY CHIP 801 IS 2.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 801 IS 2.00

4. Chip Number 901
OUTPUT OF DELAY CHIP 901 IS 2.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 901 IS 2.00

5. Chip Number 831
OUTPUT OF DELAY CHIP 831 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES

OUTPUT OF CHIP 831 IS 2.00

6. Chip Number 832
OUTPUT OF DELAY CHIP 832 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 832 IS 2.00
7. Chip Number 931
OUTPUT OF DELAY CHIP 931 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 931 IS 2.00
8. Chip Number 932
OUTPUT OF DELAY CHIP 932 IS 2.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 932 IS 2.00

////////////////////////////////////

Cycle 16 of snapshot 2 is ready to process
8 elements will output data.

These Chips are:

1. Chip Number 46
OUTPUT OF DELAY CHIP 46 IS 1.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 46 IS 1.00
2. Chip Number 47
OUTPUT OF DELAY CHIP 47 IS 1.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 47 IS 1.00
3. Chip Number 801
OUTPUT OF DELAY CHIP 801 IS 1.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 801 IS 1.00
4. Chip Number 901
OUTPUT OF DELAY CHIP 901 IS 1.00
IT HAS A DELAYOF 0 CLOCK CYCLES
OUTPUT OF CHIP 901 IS 1.00
5. Chip Number 831
OUTPUT OF DELAY CHIP 831 IS 1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 831 IS 1.00
6. Chip Number 832
OUTPUT OF DELAY CHIP 832 IS 1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 832 IS 1.00
7. Chip Number 931
OUTPUT OF DELAY CHIP 931 IS 1.00
IT HAS A DELAYOF 1 CLOCK CYCLES
OUTPUT OF CHIP 931 IS 1.00
8. Chip Number 932
OUTPUT OF DELAY CHIP 932 IS 1.00

Appendix E

Associated Unitary Transformation Processor Emulation Files

CONFIGURATIN

1	0	101	FLOT	DELY	32	0
2	0	102	FLOT	DELY	32	0
3	0	103	FLOT	DELY	32	0
1	0	203	FLOT	DELY	32	0
4	0	201	FLOT	DELY	32	0
5	0	202	FLOT	DELY	32	0
1	0	303	FLOT	DELY	32	0
6	0	301	FLOT	DELY	32	0
7	0	302	FLOT	DELY	32	0
120	0	204	FLOT	DELY	32	0
121	0	205	FLOT	DELY	32	0
122	0	206	FLOT	DELY	32	0
124	0	207	FLOT	DELY	32	0
211	0	304	FLOT	DELY	32	0
212	0	305	FLOT	DELY	32	0
213	0	306	FLOT	DELY	32	0
214	0	307	FLOT	DELY	32	0
1	0	401	FLOT	DELY	32	0
245	0	402	FLOT	DELY	32	0
246	0	403	FLOT	DELY	32	0
1	0	503	FLOT	DELY	32	0
345	0	501	FLOT	DELY	32	0
346	0	502	FLOT	DELY	32	0
420	0	504	FLOT	DELY	32	0
421	0	505	FLOT	DELY	32	0
422	0	506	FLOT	DELY	32	0
424	0	507	FLOT	DELY	32	0
1	0	601	FLOT	DELY	32	0
118	0	602	FLOT	DELY	32	0
235	0	603	FLOT	DELY	32	0
236	0	604	FLOT	DELY	32	0
335	0	605	FLOT	DELY	32	0
336	0	606	FLOT	DELY	32	0
418	0	607	FLOT	DELY	32	0
535	0	608	FLOT	DELY	32	0
536	0	609	FLOT	DELY	32	0
3	5	21				
1	0	4	FLOT	DELY	32	3
2	0	5	FLOT	DELY	32	0
3	0	6	FLOT	DELY	32	0
5	0	7	FLOT	DELY	32	0
6	0	8	FLOT	DELY	32	0
5	0	9	FLOT	DELY	32	4
6	0	10	FLOT	DELY	32	3
5	7	11	FLOT	MULT	32	1
6	8	12	FLOT	MULT	32	1
10	0	13	FLOT	DELY	32	1
11	12	14	FLOT	ADDR	32	1
15	0	16	FLOT	DELY	32	0
14	16	15	FLOT	ADDR	32	1
4	10	17	FLOT	MULT	32	1
15	0	18	FLOT	LOOK	32	1
15	0	19	FLOT	DELY	32	1
9	18	20	FLOT	MULT	32	1
17	18	21	FLOT	MULT	32	1
13	18	22	FLOT	MULT	32	1
18	19	23	FLOT	MULT	32	1
18	23	24	FLOT	MULT	32	1
7	6	39				

GIVS.SS

1	0	8	FLOT	DELY	32	5
2	0	9	FLOT	DELY	32	5
3	0	10	FLOT	DELY	32	5
4	0	11	FLOT	DELY	32	0
5	0	12	FLOT	DELY	32	0
6	0	13	FLOT	DELY	32	0
7	0	14	FLOT	DELY	32	0
11	8	15	FLOT	MULT	32	0
13	9	16	FLOT	MULT	32	0
11	9	17	FLOT	MULT	32	0
12	8	18	FLOT	MULT	32	0
14	39	19	FLOT	MULT	32	0
14	40	20	FLOT	MULT	32	0
14	8	21	FLOT	MULT	32	1
14	9	22	FLOT	MULT	32	1
11	41	23	FLOT	MULT	32	1
12	42	24	FLOT	MULT	32	1
11	43	25	FLOT	MULT	32	1
13	44	26	FLOT	MULT	32	1
15	16	27	FLOT	ADDR	32	0
17	18	28	FLOT	ADDR	32	0
19	0	29	FLOT	DELY	32	0
20	0	30	FLOT	DELY	32	0
10	21	31	FLOT	MULT	32	1
22	10	32	FLOT	MULT	32	1
23	24	33	FLOT	ADDR	32	1
25	26	34	FLOT	ADDR	32	1
27	29	35	FLOT	ADDR	32	0
28	30	36	FLOT	ADDR	32	0
31	33	37	FLOT	ADDR	32	1
32	34	38	FLOT	ADDR	32	1
35	0	39	FLOT	DELY	32	0
36	0	40	FLOT	DELY	32	0
35	0	41	FLOT	DELY	32	1
36	0	42	FLOT	DELY	32	1
36	0	43	FLOT	DELY	32	1
35	0	44	FLOT	DELY	32	1
37	0	45	FLOT	DELY	32	2
38	0	46	FLOT	DELY	32	2
7	2	39				
1	0	8	FLOT	DELY	32	9
2	0	9	FLOT	DELY	32	9
3	0	10	FLOT	DELY	32	9
4	0	11	FLOT	DELY	32	4
5	0	12	FLOT	DELY	32	4
6	0	13	FLOT	DELY	32	4
7	0	14	FLOT	DELY	32	4
11	8	15	FLOT	MULT	32	0
13	9	16	FLOT	MULT	32	0
11	9	17	FLOT	MULT	32	0
12	8	18	FLOT	MULT	32	0
14	39	19	FLOT	MULT	32	0
14	40	20	FLOT	MULT	32	0
14	8	21	FLOT	MULT	32	1
14	9	22	FLOT	MULT	32	1
11	41	23	FLOT	MULT	32	1
12	42	24	FLOT	MULT	32	1
11	43	25	FLOT	MULT	32	1
13	44	26	FLOT	MULT	32	1
15	16	27	FLOT	ADDR	32	0

17	18	28	FLOT	ADDR	32	0
19	0	29	FLOT	DELY	32	0
20	0	30	FLOT	DELY	32	0
10	21	31	FLOT	MULT	32	1
22	10	32	FLOT	MULT	32	1
23	24	33	FLOT	ADDR	32	1
25	26	34	FLOT	ADDR	32	1
27	29	35	FLOT	ADDR	32	0
28	30	36	FLOT	ADDR	32	0
31	33	37	FLOT	ADDR	32	1
32	34	38	FLOT	ADDR	32	1
35	0	39	FLOT	DELY	32	0
36	0	40	FLOT	DELY	32	0
35	0	41	FLOT	DELY	32	1
36	0	42	FLOT	DELY	32	1
36	0	43	FLOT	DELY	32	1
35	0	44	FLOT	DELY	32	1
37	0	45	FLOT	DELY	32	2
38	0	46	FLOT	DELY	32	2
3	5	21				
1	0	4	FLOT	DELY	32	14
2	0	5	FLOT	DELY	32	0
3	0	6	FLOT	DELY	32	0
5	0	7	FLOT	DELY	32	0
6	0	8	FLOT	DELY	32	0
5	0	9	FLOT	DELY	32	4
6	0	10	FLOT	DELY	32	3
5	7	11	FLOT	MULT	32	1
6	8	12	FLOT	MULT	32	1
10	0	13	FLOT	DELY	32	1
11	12	14	FLOT	ADDR	32	1
15	0	16	FLOT	DELY	32	0
14	16	15	FLOT	ADDR	32	1
4	10	17	FLOT	MULT	32	1
15	0	18	FLOT	LOOK	32	1
15	0	19	FLOT	DELY	32	1
9	18	20	FLOT	MULT	32	1
17	18	21	FLOT	MULT	32	1
13	18	22	FLOT	MULT	32	1
18	19	23	FLOT	MULT	32	1
18	23	24	FLOT	MULT	32	1
7	2	39				
1	0	8	FLOT	DELY	32	1
2	0	9	FLOT	DELY	32	1
3	0	10	FLOT	DELY	32	16
4	0	11	FLOT	DELY	32	0
5	0	12	FLOT	DELY	32	0
6	0	13	FLOT	DELY	32	0
7	0	14	FLOT	DELY	32	0
11	8	15	FLOT	MULT	32	0
13	9	16	FLOT	MULT	32	0
11	9	17	FLOT	MULT	32	0
12	8	18	FLOT	MULT	32	0
14	39	19	FLOT	MULT	32	0
14	40	20	FLOT	MULT	32	0
14	8	21	FLOT	MULT	32	1
14	9	22	FLOT	MULT	32	1
11	41	23	FLOT	MULT	32	1
12	42	24	FLOT	MULT	32	1
11	43	25	FLOT	MULT	32	1

13	44	26	FLOT	MULT	32	1
15	16	27	FLOT	ADDR	32	0
17	18	28	FLOT	ADDR	32	0
19	0	29	FLOT	DELY	32	0
20	0	30	FLOT	DELY	32	0
10	21	31	FLOT	MULT	32	1
22	10	32	FLOT	MULT	32	1
23	24	33	FLOT	ADDR	32	1
25	26	34	FLOT	ADDR	32	1
27	29	35	FLOT	ADDR	32	0
28	30	36	FLOT	ADDR	32	0
31	33	37	FLOT	ADDR	32	1
32	34	38	FLOT	ADDR	32	1
35	0	39	FLOT	DELY	32	0
36	0	40	FLOT	DELY	32	0
35	0	41	FLOT	DELY	32	1
36	0	42	FLOT	DELY	32	1
36	0	43	FLOT	DELY	32	1
35	0	44	FLOT	DELY	32	1
37	0	45	FLOT	DELY	32	2
38	0	46	FLOT	DELY	32	2
9	4	26				
1	0	10	FLOT	DELY	32	19
2	0	11	FLOT	DELY	32	16
3	0	12	FLOT	DELY	32	11
4	0	13	FLOT	DELY	32	11
5	0	14	FLOT	DELY	32	10
6	0	15	FLOT	DELY	32	10
7	0	16	FLOT	DELY	32	2
8	0	17	FLOT	DELY	32	1
9	0	18	FLOT	DELY	32	1
10	12	19	FLOT	MULT	32	1
10	13	20	FLOT	MULT	32	1
13	0	21	FLOT	DELY	32	1
16	17	22	FLOT	MULT	32	1
16	18	23	FLOT	MULT	32	1
19	22	24	FLOT	MULT	32	1
21	23	25	FLOT	MULT	32	1
22	20	26	FLOT	MULT	32	1
19	23	27	FLOT	MULT	32	1
22	0	28	FLOT	DELY	32	4
23	0	29	FLOT	DELY	32	4
24	25	30	FLOT	ADDR	32	1
26	27	31	FLOT	ADDR	32	1
30	14	32	FLOT	ADDR	32	1
31	15	33	FLOT	ADDR	32	1
11	32	34	FLOT	MULT	32	1
11	33	35	FLOT	MULT	32	1

EXPERIMENT

GIV5.TSF

4		
36		
6		
1	-1	1
2	253	2
3	-235	3
4	-252	5
5	234	6
6	1	8
7	-1	9
116	0	113
229	0	228
230	0	229
239	0	212
240	0	213
241	0	216
242	0	217
243	0	218
244	0	219
329	0	328
330	0	329
339	0	312
340	0	313
341	0	316
342	0	317
343	0	318
344	0	319
416	0	413
529	0	528
530	0	529
539	0	512
540	0	513
541	0	516
542	0	517
543	0	518
544	0	519
1	-1	1
2	-1106	2
3	1035	3
4	1107	5
5	-1036	6
6	0	8
7	1	9
1	-1	1
2	-568	2
3	534	3
4	567	5
5	-534	6
6	0	8
7	-1	9
1	-1	1
2	940	2
3	-885	3
4	-939	5
5	884	6
6	1	8
7	-1	9
1	0	0

GIVS.OUT

//

Cycle 24 of snapshot 1 is ready to process
2 elements will output data.

These Chips are:

1. Chip Number 625
4.618E-04* 834. = 0.385
OUTPUT OF CHIP 625 IS 0.385
2. Chip Number 626
4.618E-04* 766. = 0.354
OUTPUT OF CHIP 626 IS 0.354

//

Cycle 23 of snapshot 2 is ready to process
2 elements will output data.

These Chips are:

1. Chip Number 623
-9.11 + 1.30 = -7.81

Cycle 22 of snapshot 3 is ready to process
6 elements will output data.

These Chips are:

1. Chip Number 619
OUTPUT OF DELAY CHIP 619 IS 0.385
IT HAS A DELAYOF 4 CLOCK CYCLES
OUTPUT OF CHIP 619 IS 0.385
2. Chip Number 620
OUTPUT OF DELAY CHIP 620 IS 0.354
IT HAS A DELAYOF 4 CLOCK CYCLES
OUTPUT OF CHIP 620 IS 0.354
3. Chip Number 538
OUTPUT OF DELAY CHIP 538 IS 1.37
IT HAS A DELAYOF 2 CLOCK CYCLES
OUTPUT OF CHIP 538 IS 1.37
4. Chip Number 539
OUTPUT OF DELAY CHIP 539 IS -2.071E-02

Appendix F

Interactive GADAR Single Element Receiver Emulation File

```
Username: SMITHR
Password:
```

Send your MISVAX files to a LONEX printer, use the LP command.

Directory DC\$DISK2:[SMITHR]

Directory DC\$DISK2:[SMITHR.GADAR]

Total of 18 files.
3 RUN GADAR

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

F-2

BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW SCENARIO SPECIFICATION FILE.
- D GENERATE A NEW TEST RUN SPECIFICATION FILE.
- E EXIT FROM GADAR

B

WHAT IS THE NAME OF THE CONFIGURATIN SPECIFICATION FILE
TO BE OPENED FOR WRITING?

SINREC.SSF

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 1?

- A ANTENNA ELEMENT
- B NOISE GENERATOR
- C POWER DIVIDER
- D TIME DELAY
- E AMPLIFIER
- F NODE CONVERSION FUNCTION
- G ANALOG TO DIGITAL CONVERTER
- H LOCAL OSCILLATOR
- I PHASE SHIFTER (FIXED)
- J MIXER
- K SUMMING JUNCTION
- L NONE (TERMINATE ENTRY)

H

Component number 1 is of type: LO SC
What is the output node number for this component?

1

What is the output level in dBm for the local oscillator of
component number 1?

0.0

What is the center frequency in kHz for the local oscillator of
component number 1?

300000

The following parameters have been specified for component 1
of type LO SC. Do you wish to change anything?(YES or NO)

output node number: 1
center frequency in kHz: 300000.000
output level in dBm: 0.000

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 2?

- A ANTENNA ELEMENT
- B NOISE GENERATOR
- C POWER DIVIDER
- D TIME DELAY
- E AMPLIFIER
- F NODE CONVERSION FUNCTION
- G ANALOG TO DIGITAL CONVERTER
- H LOCAL OSCILLATOR
- I PHASE SHIFTER (FIXED)
- J MIXER
- K SUMMING JUNCTION

C L NONE (TERMINATE ENTRY)

Component number 2 is of type: POWD
 What is the input node number for this component?
 1

Component number 2 is of type: POWD
 How many output nodes are there on this component?
 2

What are the output node numbers for this component?
 2,3

The following parameters have been specified for component 2
 of type POWD. Do you wish to change anything?(YES or NO)
 number of output nodes: 2
 input node number: 1
 output node number: 2
 output node number: 3

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 3?

- A ANTENNA ELEMENT
- B NOISE GENERATOR
- C POWER DIVIDER
- D TIME DELAY
- E AMPLIFIER
- F NODE CONVERSION FUNCTION
- G ANALOG TO DIGITAL CONVERTER
- H LOCAL OSCILLATOR
- I PHASE SHIFTER (FIXED)
- J MIXER
- K SUMMING JUNCTION
- L NONE (TERMINATE ENTRY)

I

Component number 3 is of type: PHSF
 What is the input node number for this component?
 3

What is the output node number for this component?
 4

What is the phase shift in degrees for the phase shifter of
 component number 3?
 90.0

The following parameters have been specified for component 3
 of type PHSF. Do you wish to change anything?(YES or NO)
 input node number: 3
 output node number: 4
 phase shift in degrees: 90.000

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 4?

- A ANTENNA ELEMENT
- B NOISE GENERATOR
- C POWER DIVIDER
- D TIME DELAY

E AMPLIFIER
 F NODE CONVERSION FUNCTION
 G ANALOG TO DIGITAL CONVERTER
 H LOCAL OSCILLATOR
 I PHASE SHIFTER (FIXED)
 J MIXER
 K SUMMING JUNCTION
 L NONE (TERMINATE ENTRY)

F

Component number 4 is of type: NDCN
 What is the input node number for this component?

2

What is the output node number for this component?

5

The following parameters have been specified for component 4
 of type NDCN. Do you wish to change anything?(YES or NO)
 input node number: 2
 output node number: 5

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 5?

A ANTENNA ELEMENT
 B NOISE GENERATOR
 C POWER DIVIDER
 D TIME DELAY
 E AMPLIFIER
 F NODE CONVERSION FUNCTION
 G ANALOG TO DIGITAL CONVERTER
 H LOCAL OSCILLATOR
 I PHASE SHIFTER (FIXED)
 J MIXER
 K SUMMING JUNCTION
 L NONE (TERMINATE ENTRY)

F

Component number 5 is of type: NDCN
 What is the input node number for this component?

4

What is the output node number for this component?

6

The following parameters have been specified for component 5
 of type NDCN. Do you wish to change anything?(YES or NO)
 input node number: 4
 output node number: 6

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 6?

A ANTENNA ELEMENT
 B NOISE GENERATOR
 C POWER DIVIDER
 D TIME DELAY
 E AMPLIFIER
 F NODE CONVERSION FUNCTION
 G ANALOG TO DIGITAL CONVERTER
 H LOCAL OSCILLATOR

I PHASE SHIFTER (FIXED)
 J MIXER
 K SUMMING JUNCTION
 L NONE (TERMINATE ENTRY)

A

Component number 6 is of type ELMN.
 What is the output node number for this component?

7

What is the element type for this component?

A) omni

A

What are the X,Y,Z coordinates in meters specifying the location of this element?

0.0,0.0,0.0

What are the roll, pitch, and yaw angles in degrees of the element bearing relative to normal orientation as defined for the element?

0.0,0.0,0.0

What is the gain of this element in dB?

0.0

The following parameters have been specified for component 6 of type ELMN. Do you wish to change anything?(YES or NO)

output node number: 7

element type name:OMNI

X,Y, and Z in meters: 0.000 0.000 0.000

roll, pitch, and yaw in degrees: 0.000 0.000 0.000

gain in dB: 0.000

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 7?

A ANTENNA ELEMENT
 B NOISE GENERATOR
 C POWER DIVIDER
 D TIME DELAY
 E AMPLIFIER
 F NODE CONVERSION FUNCTION
 G ANALOG TO DIGITAL CONVERTER
 H LOCAL OSCILLATOR
 I PHASE SHIFTER (FIXED)
 J MIXER
 K SUMMING JUNCTION
 L NONE (TERMINATE ENTRY)

B

Component number 7 is of type NOIS.
 What is the output node number for this component?

8

What is the system noise figure in dB at the output of the noise generator of component number 7?

10.0

The following parameters have been specified for component 7 of type NOIS. Do you wish to change anything?(YES or NO)

output node number: 8
noise figure at output in dB: 10.000

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 8?

- A ANTENNA ELEMENT
- B NOISE GENERATOR
- C POWER DIVIDER
- D TIME DELAY
- E AMPLIFIER
- F NODE CONVERSION FUNCTION
- G ANALOG TO DIGITAL CONVERTER
- H LOCAL OSCILLATOR
- I PHASE SHIFTER (FIXED)
- J MIXER
- K SUMMING JUNCTION
- L NONE (TERMINATE ENTRY)

K

Component number 8 is of type: SMJC
How many input nodes in this component?

2

Component number 8 is of type: SMJC
What are the input node numbers for this component?

7,8

What is the output node number for this component?

9

The following parameters have been specified for component 8
of type SMJC. Do you wish to change anything?(YES or NO)

number of input nodes: 2
output node number: 9
input node number: 7
input node number: 8

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 9?

- A ANTENNA ELEMENT
- B NOISE GENERATOR
- C POWER DIVIDER
- D TIME DELAY
- E AMPLIFIER
- F NODE CONVERSION FUNCTION
- G ANALOG TO DIGITAL CONVERTER
- H LOCAL OSCILLATOR
- I PHASE SHIFTER (FIXED)
- J MIXER
- K SUMMING JUNCTION
- L NONE (TERMINATE ENTRY)

E

Component number 9 is of type: AMPL
What is the input node number for this component?

9

What is the output node number for this component?

10

What is the gain in dB for the amplifier of component number 9?
40.0

The following parameters have been specified for component 9
of type AMPL. Do you wish to change anything?(YES or NO)

input node number: 9
output node number: 10
gain in dB: 40.000

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 10?

A ANTENNA ELEMENT
B NOISE GENERATOR
C POWER DIVIDER
D TIME DELAY
E AMPLIFIER
F NODE CONVERSION FUNCTION
G ANALOG TO DIGITAL CONVERTER
H LOCAL OSCILLATOR
I PHASE SHIFTER (FIXED)
J MIXER
K SUMMING JUNCTION
L NONE (TERMINATE ENTRY)

F

Component number 10 is of type: NDCN
What is the input node number for this component?

10

What is the output node number for this component?

11

The following parameters have been specified for component 10
of type NDCN. Do you wish to change anything?(YES or NO)

input node number: 10
output node number: 11

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 11?

A ANTENNA ELEMENT
B NOISE GENERATOR
C POWER DIVIDER
D TIME DELAY
E AMPLIFIER
F NODE CONVERSION FUNCTION
G ANALOG TO DIGITAL CONVERTER
H LOCAL OSCILLATOR
I PHASE SHIFTER (FIXED)
J MIXER
K SUMMING JUNCTION
L NONE (TERMINATE ENTRY)

C

Component number 11 is of type: POWD
What is the input node number for this component?

11

Component number 11 is of type: POWD
How many output nodes are there on this component?

2

What are the output node numbers for this component?
12,13

The following parameters have been specified for component 11
of type POWD. Do you wish to change anything?(YES or NO)

number of output nodes: 2
input node number: 11
output node number: 12
output node number: 13

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 12?

A ANTENNA ELEMENT
B NOISE GENERATOR
C POWER DIVIDER
D TIME DELAY
E AMPLIFIER
F NODE CONVERSION FUNCTION
G ANALOG TO DIGITAL CONVERTER
H LOCAL OSCILLATOR
I PHASE SHIFTER (FIXED)
J MIXER
K SUMMING JUNCTION
L NONE (TERMINATE ENTRY)

12 J

Component number 12 is of type: MIXE

What is the input node number for port R of this component?

12

Component number 12 is of type: MIXE

What is the input node number for port L of this component?

5

What is the output node number for port I of this component?

14

The following parameters have been specified for component 12
of type MIXE. Do you wish to change anything?(YES or NO)

input node number port R: 12
input node number port L: 5
output node number port I: 14

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 13?

A ANTENNA ELEMENT
B NOISE GENERATOR
C POWER DIVIDER
D TIME DELAY
E AMPLIFIER
F NODE CONVERSION FUNCTION
G ANALOG TO DIGITAL CONVERTER
H LOCAL OSCILLATOR
I PHASE SHIFTER (FIXED)
J MIXER
K SUMMING JUNCTION
L NONE (TERMINATE ENTRY)

J

Component number 13 is of type: MIXE
 13 What is the input node number for port R of this component?

Component number 13 is of type: MIXE
 6 What is the input node number for port L of this component?

What is the output node number for port I of this component?
 15

The following parameters have been specified for component 13
 of type MIXE. Do you wish to change anything? (YES or NO)
 input node number port R: 13
 input node number port L: 6
 output node number port I: 15
 NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 14?
 A ANTENNA ELEMENT
 B NOISE GENERATOR
 C POWER DIVIDER
 D TIME DELAY
 E AMPLIFIER
 F NODE CONVERSION FUNCTION
 G ANALOG TO DIGITAL CONVERTER
 H LOCAL OSCILLATOR
 I PHASE SHIFTER (FIXED)
 J MIXER
 K SUMMING JUNCTION
 L NONE (TERMINATE ENTRY)
 G

Component number 14 is of type: ATDC
 14 What is the input node number for this component?

What is the output node number for this component?
 16

How many bits precision does the analog to digital converter
 of component number 14 have available?
 12

What is the maximum voltage level input to the
 analog to digital converter of component number 14?
 1.0

What is the minimum voltage level input to the
 analog to digital converter of component number 14?
 -1.0

The following parameters have been specified for component 14
 of type ATDC. Do you wish to change anything? (YES or NO)
 input node number: 14
 output node number: 16
 bits of precision: 12
 maximum input level (voltage): 1.000
 minimum input level (voltage): -1.000
 NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 15?

- A ANTENNA ELEMENT
- B NOISE GENERATOR
- C POWER DIVIDER
- D TIME DELAY
- E AMPLIFIER
- F NODE CONVERSION FUNCTION
- G ANALOG TO DIGITAL CONVERTER
- H LOCAL OSCILLATOR
- I PHASE SHIFTER (FIXED)
- J MIXER
- K SUMMING JUNCTION
- L NONE (TERMINATE ENTRY)

G

Component number 15 is of type: ATDC

What is the input node number for this component?

15

What is the output node number for this component?

17

How many bits precision does the analog to digital converter of component number 15 have available?

12

What is the maximum voltage level input to the analog to digital converter of component number 15?

1.0

What is the minimum voltage level input to the analog to digital converter of component number 15?

-1.0

The following parameters have been specified for component 15 of type ATDC. Do you wish to change anything?(YES or NO)

input node number: 15
output node number: 17
bits of precision: 12
maximum input level (voltage): 1.000
minimum input level (voltage): -1.000

NO

WHAT COMPONENT TYPE WOULD YOU LIKE TO SELECT FOR COMPONENT 16?

- A ANTENNA ELEMENT
- B NOISE GENERATOR
- C POWER DIVIDER
- D TIME DELAY
- E AMPLIFIER
- F NODE CONVERSION FUNCTION
- G ANALOG TO DIGITAL CONVERTER
- H LOCAL OSCILLATOR
- I PHASE SHIFTER (FIXED)
- J MIXER
- K SUMMING JUNCTION
- L NONE (TERMINATE ENTRY)

L

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW SCENARIO SPECIFICATION FILE.
- D GENERATE A NEW TEST RUN SPECIFICATION FILE.
- E EXIT FROM GADAR

E

\$ TYPE SINREC.SSF

ONFIGURATIN

```

1      LO SC
1 0.30000000E+06 0.00000000E+00
2      POWD
2      1
2      3
3      PHSF
3      4 0.90000000E+02
4      NDCN
2      5
5      NDCN
4      6
6      ELMN
7      OMNI 0.00000000E+00 0.00000000E+00 0.00000000E+00 0.00000000E+00 0.0000
000E+00 0.00000000E+00 0.00000000E+00
7      NOIS
8 0.10000000E+02 0.00000000E+00
8      SMJC
2      9
7      8
9      AMPL
9 10 0.40000000E+02
10     NDCN
10     11
11     POWD
2     11
12     13
12     MIXE
12     5 14
13     MIXE
13     6 15
14     ATDC
14 16 12 0.10000000E+01-0.10000000E+01
15     ATDC
15 17 12 0.10000000E+01-0.10000000E+01
$ RUN GADAR

```

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM GADAR. GADAR IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A

RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW SCENARIO SPECIFICATION FILE.
- D GENERATE A NEW TEST RUN SPECIFICATION FILE.
- E EXIT FROM GADAR

C

WHAT IS THE NAME OF THE SCENARIO SPECIFICATION FILE
TO BE OPENED FOR WRITING?
SINREC.SCF

What type would you like to specify for source number 1?

- A Signal in space
- B None (terminate entry)

A

What type of modulation does signal number 1 have?

- A Noise (flat across band)

A

What are the azimuth (degrees), elevation (degrees) and range (kilometers) describing the location of this signal relative to array center?

90.0,0.0,1.0

What is the effective radiated power (dBm) of this signal in the direction of array center?

-45.0

What is the center frequency of the signal in kHz?

300000

What is the bandwidth of the signal in kHz?

50

The following parameters have been given for source number 1 of type SGNL. Do you want to change anything (YES or NO)?

Modulation type: NOIS.

Azimuth: 90.000 degrees

Elevation: 0.000 degrees

Range: 1.000 kilometers

Effective radiated power: -45.000 dBm

Center frequency: 300000.000 kHz

Bandwidth: 50.000 kHz

NO

What type would you like to specify for source number 2?

- A Signal in space
- B None (terminate entry)

B

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.

B GENERATE A NEW SYSTEM SPECIFICATION FILE.
 C GENERATE A NEW SCENARIO SPECIFICATION FILE.
 D GENERATE A NEW TEST RUN SPECIFICATION FILE.
 E EXIT FROM GADAR
 E
 \$ TYPE SINREC.SCF
 CENARIO
 1 SGNL
 OIS 0.90000000E+02 0.00000000E+00 0.10000000E+01-0.45000000E+02
 0.30000000E+06 0.50000000E+02
 \$ RUN GADAR

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM GADAR. GADAR IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
 EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
 BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
 B GENERATE A NEW SYSTEM SPECIFICATION FILE.
 C GENERATE A NEW SCENARIO SPECIFICATION FILE.
 D GENERATE A NEW TEST RUN SPECIFICATION FILE.
 E EXIT FROM GADAR

D

WHAT IS THE NAME OF THE EXPERIMENT SPECIFICATION FILE
 TO BE OPENED FOR WRITING?
 SINREC.TSF

How many spectral lines should be used to model the broadband sources?

1

What are the system center frequency and bandwidth in kHz?
 300000,50

What is the total number of iterations that you desire to be
 processed during this run?
 16

How often (in sampling intervals) should outputs be written to
 file?
 1

How many system nodes are to be tracked and written to the output file?

2

What are the node numbers to be output to file?

16,17

These parameters have been given for the specification of this experiment. Do you want to change anything? (YES or NO)

Center frequency: 300000.000 kHz
System bandwidth: 50.000 kHz
Number of spectral lines: 1 .
Total number of time samples processed: 16 .
Frequency of output: every 1 samples
The number of output nodes: 2 nodes
output node: 16
output node: 17

NO

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW SCENARIO SPECIFICATION FILE.
- D GENERATE A NEW TEST RUN SPECIFICATION FILE.
- E EXIT FROM GADAR

E

\$ TYPE SINREC.TSF

XPHERIMENT

0.30000000E+06 0.50000000E+02

1

16

1

2

16

17

\$ RUN GADAR

THIS IS THE GENERAL PURPOSE ADAPTIVE ARRAY PROGRAM GADAR. GADAR IS CAPABLE OF SIMULATING A COMMUNICATION SYSTEM HAVING RECEIVING ELEMENTS IN SPACE EXCITED BY A SIMULATED SCENARIO. THE SYSTEM IS SPECIFIED BY THE INTERCONNECTION OF STANDARD COMPONENT BUILDING BLOCKS INTERCONNECTED AT NODES.

SYSTEM AND TEST RUN PARAMETERS ARE SPECIFIED BY THE USER IN AN INTERACTIVE DIALOG AND WRITTEN TO FILES. THESE FILES ARE THEN USED TO SPECIFY SYSTEM CONFIGURATION AND TESTING MODE AT RUN TIME.

THERE ARE THREE TYPES OF ANSWERS TO QUESTIONS USED IN THE INTERACTIVE PROGRAM CONSISTING OF YES AND NO, MENU SELECT, AND PARAMETER SPECIFICATION. ALL USER COMMANDS MUST BE TERMINATED BY A CARRIAGE RETURN ('<CR>').

THERE ARE SEVERAL COMMANDS THAT WILL BE VALID AT ANY TIME THAT A RESPONSE FROM YOU, THE USER, IS REQUIRED. THESE COMMANDS CONSIST OF THE FOLLOWING:

- HELP-ADDITIONAL DETAILS ARE REQUESTED FOR QUESTION.
- EXIT-EXIT AFTER CLOSING FILES PRESENTLY BEING WRITTEN.
- BREAK-CLOSE FILES AND RETURN TO OPERATION SELECTION.

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW SCENARIO SPECIFICATION FILE.
- D GENERATE A NEW TEST RUN SPECIFICATION FILE.

E EXIT FROM GADAR

A

WHAT IS THE NAME OF THE EXPERIMENT SPECIFICATION FILE
TO BE OPENED FOR READING?
SINREC.TSF

WHAT IS THE NAME OF THE SCENARIO SPECIFICATION FILE
TO BE OPENED FOR READING?
SINREC.SCF

WHAT IS THE NAME OF THE CONFIGURATIN SPECIFICATION FILE
TO BE OPENED FOR READING?
SINREC.SSF

WHAT IS THE NAME OF THE GADAR OUT SPECIFICATION FILE
TO BE OPENED FOR WRITING?
SINREC.OUT

AT THIS TIME, DO YOU WANT TO:

- A MAKE A SIMULATION RUN USING PREVIOUSLY GENERATED FILES.
- B GENERATE A NEW SYSTEM SPECIFICATION FILE.
- C GENERATE A NEW SCENARIO SPECIFICATION FILE.
- D GENERATE A NEW TEST RUN SPECIFICATION FILE.
- E EXIT FROM GADAR

E

\$ TYPE SINREC.OUT

ADAR OUT

2	
-44	41
197	-184
101	-95
-167	157
-148	141
123	-117
183	-175
-71	66
-201	197
17	-16
204	-200
41	-40
-191	187
-104	97
166	-154
153	-142
-115	119

\$ LOG

SMITHR

logged out at 22-DEC-1989 13:04:00.64Connection closed by remote

Appendix G

Interactive GADAR Three Element Receiver File

Welcome to VAX/VMS V5.2

Username: SMITHR

Password:

Welcome to VAX/VMS version V5.2 on node MISVX1

Last interactive login on Thursday, 21-DEC-1989 14:19Z>

../

Lookup the phone number and office symbol of RADC personel, use the
FIND command.

Send your MISVAX files to a LONEX printer, use the LP command.

To get information on special utilities installed on the 8650 cluster,
type 'help @RADC' at the \$ prompt.

/../>

\$ set def [smithr.gadar]

\$ dir

Directory DC\$DISK2:[SMITHR.GADAR]

COM.DIR;1	GADAR.EXE;1	GADTST.OUT;1	GADTST.SCF;1
GADTST.SSF;1	GADTST.TSF;1	SINGLE.SCF;1	SINGLE.SSF;1
SINGLE.TSF;1	SOURCE.DIR;1	SYSTEM.SCF;1	SYSTEM.SSF;1
SYSTEM.TSF;1	TER.OUT;1	TER.SCF;1	TER.SSF;1
TER.TSF;1	TEST.DIR;1		

Total of 18 files.

\$ type ter.*;*

DC\$DISK2:[SMITHR.GADAR]TER.OUT;1

ADAR OUT

6					
253	-235	-252	234	252	-234
-1106	1035	1107	-1036	-1106	1034
-568	534	567	-534	-568	535
940	-885	-939	884	939	-884
833	-795	-833	796	832	-795
-694	663	693	-662	-693	662
-1034	987	1033	-987	-1032	985
401	-372	-402	374	402	-373
1131	-1110	-1131	1110	1131	-1110
-98	96	96	-94	-97	96
-1151	1130	1151	-1129	-1150	1129
-234	230	235	-231	-234	229
1074	-1054	-1075	1055	1075	-1054
590	-548	-589	547	589	-547
-932	866	932	-866	-934	867
-857	796	858	-797	-858	797
651	-675	-649	673	650	-674

DC\$DISK2:[SMITHR.GADAR]TER.SCF;1

CENARIO

1 SGNL

OIS 0.00000000E+00 0.00000000E+00 0.10000000E+01-0.40000000E+02
0.30000000E+06 0.50000000E+02

DC\$DISK2:[SMITHR.GADAR]TER.SSF;1

ONFIGURATIN

```
1      LOSC
1 0.30000000E+06 0.00000000E+00
2      ELMN
2      OMNI-0.50000000E+00 0.00000000E+00 0.00000000E+00 0.00000000E+00 0.0000
0000E+00 0.00000000E+00 0.00000000E+00
3      NOIS
3 0.10000000E+02 0.00000000E+00
4      ELMN
4      OMNI 0.00000000E+00 0.00000000E+00 0.00000000E+00 0.00000000E+00 0.0000
0000E+00 0.00000000E+00 0.00000000E+00
5      NOIS
5 0.10000000E+02 0.00000000E+00
6      ELMN
6      OMNI 0.50000000E+00 0.00000000E+00 0.00000000E+00 0.00000000E+00 0.0000
0000E+00 0.00000000E+00 0.00000000E+00
7      NOIS
7 0.10000000E+02 0.00000000E+00
8      POWD
2      1
8      9
9      SMJC
2      10
2      3
10     SMJC
2      11
4      5
11     SMJC
2      12
6      7
12     PHSF
9      13 0.90000000E+02
13     AMPL
10     14 0.50000000E+02
14     AMPL
11     15 0.50000000E+02
15     AMPL
12     16 0.50000000E+02
16     NDCN
8      17
17     NDCN
13     18
18     NDCN
14     19
19     NDCN
15     20
20     NDCN
16     21
21     POWD
2      19
22     23
22     POWD
2      20
24     25
23     POWD
2      21
26     27
24     MIXE
```

```

22 17 28
25 MIKE
23 18 29
26 MIKE
24 17 30
27 MIKE
25 18 31
28 MIKE
26 17 32
29 MIKE
27 18 33
30 ATDC
28 34 12 0.10000000E+01-0.10000000E+01
31 ATDC
29 35 12 0.10000000E+01-0.10000000E+01
32 ATDC
30 36 12 0.10000000E+01-0.10000000E+01
33 ATDC
31 37 12 0.10000000E+01-0.10000000E+01
34 ATDC
32 38 12 0.10000000E+01-0.10000000E+01
35 ATDC
33 39 12 0.10000000E+01-0.10000000E+01

```

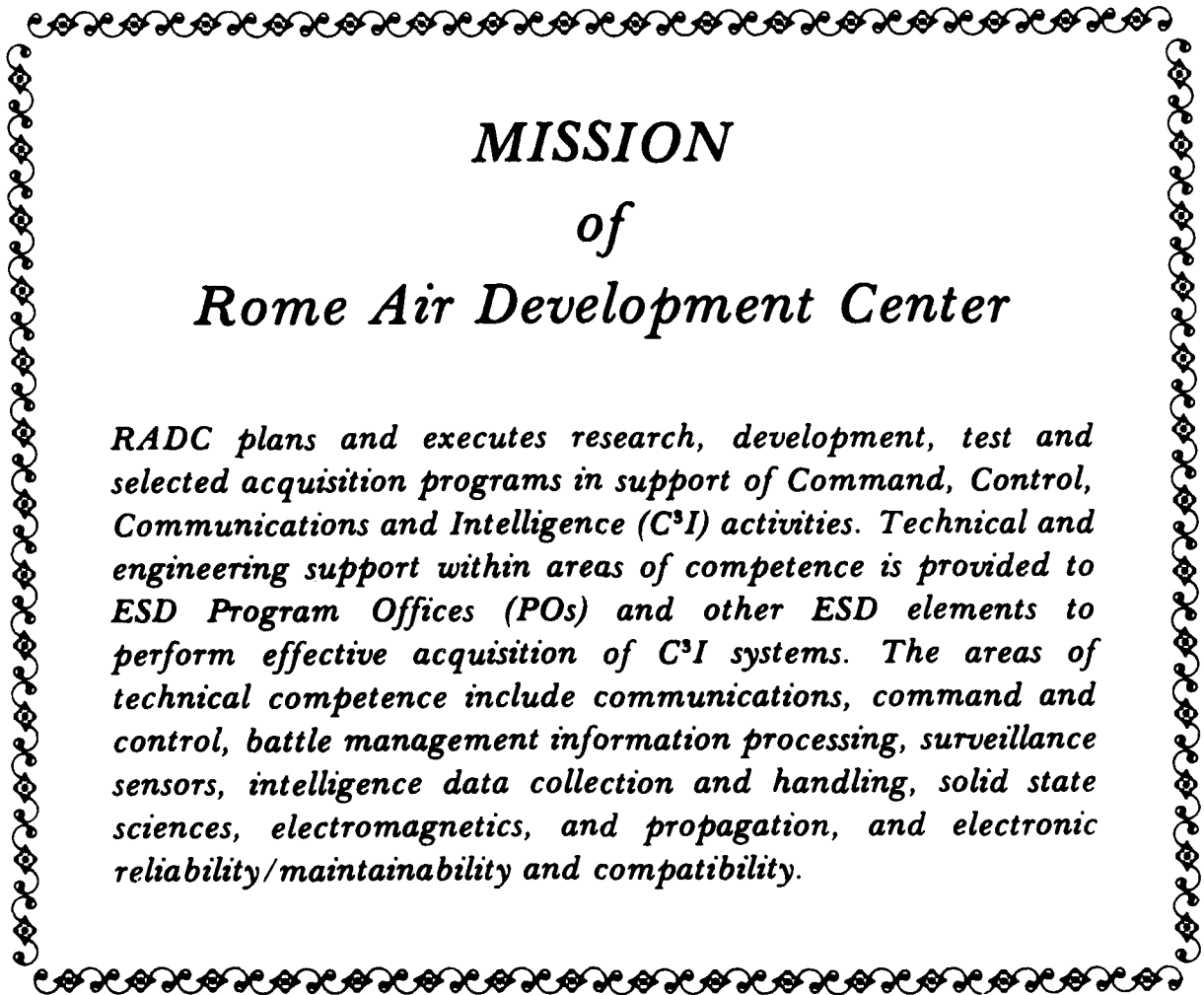
DCSDISK2:[SMITHR.GADAR]TER.TSF;1

XPERIMENT

0.30000000E+06	0.50000000E+02	1	16	1	6	34
35	36	37	38	39		

\$ log

SMITHR logged out at 21-DEC-1989 14:25:51.90Connection closed by remote ho



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