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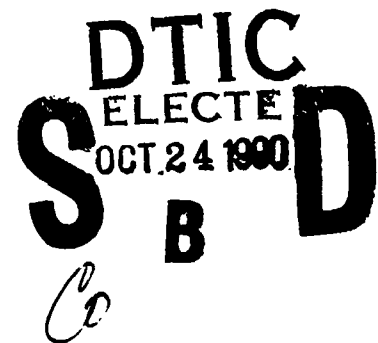# HIGH SPEED SIGNAL PROCESSING CONCEPTS

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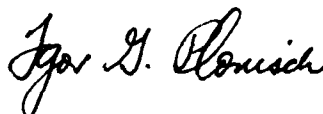
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13. ABSTRACT (Maximum 200 words)
The effort is characterized by introducing novel concepts and algorithms for high throughput, arithmetic intensive applications in signal processing and communications. In addition, efficient implementations of these algorithms in a variety of modalities, including VLSI, and consideration of reliability and fault-tolerance issues are included. The highlights of the achievements of this effort are:

1. Linear phase FIR filters with computational efficiency of IIR filters;
2. VLSI implementation of FIR filters with binary coefficients based on redundancy removal techniques;
3. Optimal distribution of redundancy in hierarchical architectures, with faulty interconnects;
4. Commutative non-linearities and discrete filters;

(Continued)

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    5. Prime power moduli to optimize the dynamic range of RNS-based computation;

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High Speed Signal Processing Concepts

1.0 Abstract

This effort is characterized by introducing novel concepts and algorithms for high throughput, arithmetic intensive applications in signal processing and communications. In addition, efficient implementations of these algorithms in a variety of modalities, including VLSI, and consideration of reliability and fault-tolerance issues are included. In the sequel, the main achievement in each topic is summarized, and cited publications and presentations which resulted from this effort attached.

The highlights of the achievements of this effort and their implications are:

1. Linear phase FIR filters with computational efficiency of IIR filters. This is a breakthrough that removes a fundamental impediment in using linear phase FIR filters in application with sharp transition bands, where very long filters result, as in designing multiband filters in communications applications.

2. VLSI implementation of FIR filters with binary coefficients based on optimal partitioning and redundancy removal which preserves the $O(N/\log N)$ performance based on the number of additions per output in the more involved VLSI environment with interconnections and area-time product taken into account.

3. Optimal distribution of redundancy in hierarchical architectures, with faulty interconnections taken into consideration. This work on fault-tolerance applies also to yield improvement in VLSI and WSI. It is also applicable to real-time fault-tolerance combined with testability, but such extensions require further research for specific applications.

4. The class of all discrete-time systems which commute with every monotone increasing nonlinearity is completely characterized. This class is found to be of the selection filter type, in which each output is selected from the input window according to some decision criteria. Clearly this could be of impact in communications applications, as further investigation could indicate. Also, an efficient implementation of one-dimensional recursive median filters is discussed.

5. Prime power moduli are found to optimize the dynamic range of RNS-based computation and signal processing. Identical modules that are firmware programmable are a possible basis for such a system, and could be produced for a wide range of

applications. Further research is required to continue the preliminary investigation of the arithmetic for prime power moduli of this effort.

6. The volume of the coefficient space domain of polynomials with roots in a given circle is evaluated. This could be the basis of global sensitivity analysis, resolution of spectral estimation and identification algorithms by actually counting the number of polynomials with finite wordlength in a given class. This study could also has information theoretic interpretation as the entropy of classes of polynomials in their coefficient space.

7. It is shown that if a polynomial has its roots in a convex domain which contains the origin, then the roots of any linear convex combination of the polynomial and its normalized derivative are in the same convex domain. This result and its generalization could have implications in robustness analysis of systems, and in some signal processing and communications applications connected to the Hilbert transform.

2.0 FIR Filters Based on Switching and Resetting of IIR Filters

Linear phase FIR filters with computational efficiency of IIR filters. This is a breakthrough that removes a fundamental impediment in using linear phase FIR filters in application with sharp transition bands, where very long filters result, as in designing multiband filters in communications applications.

2.1 Properties and Structure of Linear Phase FIR Filters Based on Switching and Resetting of IIR Filters

New recursive structures are introduced for implementing long linear phase FIR filters using a very small number of multipliers. The implementation of these filters uses the principle of switching and resetting between two identical copies of the same IIR filter, introduced in Ref.1. The impulse response of these filters is a truncated and shifted version of the response of a filter $G(z)G(z^{-1})$ where $G(z)$ is a stable IIR filter and $G(z^{-1})$ is the corresponding unstable one. The filters are implemented as a parallel combination of several branches, each generating a truncated response corresponding to a complex conjugate pole pair and its reciprocal pair. The truncation is performed using a feedforward term, which provides a pole-zero cancellation. To stabilize the pole-zero cancellation and to avoid the quantization error from growing excessively, the branch filters are then implemented by applying the principle of switching and resetting. It is shown, via an example in Pub.1, that using the above approach we can design a nearly optimum FIR filter of order larger than 500 using just 17 adjustable parameters.

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2.2 Efficient Linear Phase Filters Based on Switching and Time Reversal

Although implementation of $G(z^{-1})$ via switching and resetting stabilizes pole-zero cancellation, coefficient sensitivity and roundoff noise requires extra bits. To avoid these effects, reversal of the data blocks before and after filtering, combined with replacing $G(z^{-1})$ by $G(z)$ results in an implementation of $G(z^{-1})$ using a stable filter. As shown in Pub.2, this results however in increased group delay compared to the above approach.

3.0 VLSI FIR Filters Based on Optimal Reduction

VLSI implementation of FIR filters with binary coefficients based on optimal partitioning and redundancy removal which preserves the $O(N/log\ N)$ performance based on the number of additions per output in the more involved VLSI environment with interconnections and area-time product taken into account.

In Ref.2 an efficient realization of FIR filters based on space-time duality is presented. In this approach, all the fixed-point multiplications are reduced to additions, and then a new type of redundancy is identified and removed to reduce the number of equivalent additions per output. To avoid the relative cost of multiplications and additions in fixed-point arithmetic, which is highly implementation dependent, this approach is applied to FIR filters with coefficients in $\{0,1\}$ in Ref.3. With addition as the only arithmetic operations involved, the effectiveness of the approach was made clear in Ref.3, where in comparison to up to N-1 additions per output, only $O(N/log\ N)$ are required. However, in a VLSI implementation, the additions per output is not an adequately representative cost function. The cost of interconnections, memory, area-time trade-offs, and other house keeping functions should also be incorporated. As indicated in Ref.3, a highly parallel VLSI implementation results in poor performance for the new algorithm with only a small advantage over the regular direct design. In Pres.2 it is shown that a carefully defined highly sequential design results in an area-time product which preserves most of the performance of the algorithm. Bill Klavoon is continuing with this effort, examining the details of actual VLSI designs of parts of which an FIR filter, filter bank, with single or multibit coefficients are composed. This effort is a prime candidate for continuation beyond the current funding if the encouraging results obtained are to be developed into actual chip or chip set layouts. Also, VLSI implementation of the most general form of the optimal partitioning and redundancy removal applied to partial sums in Ref.4 is another candidate for further research. This would result in a chip or chip set layout for vector matrix multiplication, and applications that could be mapped into the form of vector matrix multiplication.

4.0 A Hierarchical Approach for the Design of Two-Dimensional Fault-Tolerant Systolic Arrays

Optimal distribution of redundancy in hierarchical architectures, with faulty interconnects taken into consideration. This work on fault-tolerance applies also to yield improvement in VLSI and WSI. It is also applicable to real-time fault-tolerance combined with testability, but such extensions require further research for specific applications.

The reliability evaluation of fault-tolerant systolic arrays is often considered in the current literature with the assumption of no faulty interconnections. This leads to incorrect conclusions about the effect of increasing the redundancy. It would then appear that more redundancy results in higher reliability. In Pub.3, a reliability model for fault-tolerant systolic arrays that incorporates the effect of faulty processing units, as well as faulty switches and interconnections is developed and applied in evaluating different redundancy schemes. In particular, a simple local redundancy scheme is compared with a two-level redundancy one which introduces redundancy hierarchically in two levels It is found that for high redundancy, the two-level scheme can achieve much higher reliability than the local one, given an identical number of spare units. However, for low redundancy, the local scheme is less costly to implement, yet performs slightly better than the two-level one as shown in Pub.3.

5.0 Selection Filters

The class of all discrete-time systems which commute with every monotone increasing nonlinearity is completely characterized. This class is found to be of the selection filter type, in which each output is selected from the input window according to some decision criteria. Clearly this could be of impact in communications applications, as further investigation could indicate. Also, an efficient implementation of one-dimensional recursive median filters is discussed.

5.1 Selection Filters and Commutativity with Memoryless Nonlinearities

The class of nonrecursive filters that commute with every monotone increasing, zero-memory nonlinearity (ZNL) is characterized in Pub.4. Specifically, it is shown that a nonrecursive filter commutes with every monotone increasing ZNL if and only if it is a rank-based selection (RBS) filter that replaces each input value with one of its neighboring input data which is selected depending on the relative amplitudes of the data. It is also shown that RBS filters commuting with every nondecreasing ZNL are stack filters that can be represented as finite maximum-minimum operations.

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5.2 Efficient Implementation of One-Dimensional Recursive Median Filters

It is shown in Pub.5 that one-dimensional (1-D) recursive median (RM) filtering, the present output is fully determined by the input data in the window and by the most recent output. All other past outputs are shown to be redundant. Based on this result, efficient algorithms and VLSI implementation for 1-D RM filters are presented, and shown to compare favorably with those of standard median filtering.

6.0 Residue Number Systems with Prime Power Moduli

In computation based on residue arithmetic via identical modules which admit firmware programmability, it is shown in Pres.4 that the maximum system dynamic range is attained when the moduli of the individual modules are prime powers. Evaluating the required number of modules and their wordlength, to implement a required overall dynamic range is presented Discussion of primitive roots, and ways to implement arithmetic in prime power system is also presented, but requires further research.

7.0 Coefficient Space Properties of Polynomials

The volume of the coefficient space domain of polynomials with roots in a given circle is evaluated. This could be the basis of global sensitivity analysis, resolution of spectral estimation and identification algorithms by actually counting the number of polynomials with finite wordlength in a given class. This study could also has information theoretic interpretation as the entropy of classes of polynomials in their coefficient space.

Also, It is shown that if a polynomial has its roots in a convex domain which contains the origin, then the roots of any linear convex combination of the polynomial and its normalized derivative are in the same convex domain. This result and its generalization could have implications in robustness analysis of systems, and in some signal processing and communications applications connected to the Hilbert transform.

7.1 The Volume of the Coefficient Space Stability Domain of Monic Polynomials

The volume of the coefficient space domain of polynomials with zeros in the unit circle is evaluated in Pub.6. This volume is an upper bound on that of any domain of coefficient variations of any shape under which stability is invariant. Volumes of related domains are computed and the results extended to polynomials with zeros in a circle of arbitrary radius.

This approach of studying polynomials as a class from a global geometry point of view is particularly interesting in studying the entropy of polynomials in their coefficient

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space, and in developing global measures of the ability of models with finite wordlength to achieve a given resolution in applications such as spectral estimation, identification, and target recognition.

7.2 Generating Edges of *D*-Stable Polynomials

It is shown in Pub.7 that if a polynomial P of degree n is D-stable, where D is convex and contains the origin, then all convex combinations of P and its normalized derivative, zP'/n, are also D-stable. It is also shown that convex linear combinations of the logarithmic derivatives of D-stable polynomials with a convex D, have both their poles and zeros in D. Both theorems are motivated by a theorem of Lucas, and provide an example of how to generate edges and polytopes of D-stable polynomials and rational functions from a given set of D-stable polynomials. This result and its generalization could have implications in robustness analysis of systems, and in some signal processing and communications applications connected to the Hilbert transform.

8.0 References, Publications, and Presentations

The Following references are cited in this report. This is followed by the publications resulting from this effort, and presentations and discussions that took place in a final report visit to RADC on Feb. 9, 1990.

8.1 References

1. A. T. Fam, "FIR Filters that Approach IIR Filters in their Computational Efficiency," *Twenty-First Asilomar Conference on Signals, Systems, and Computers*, Pacific Grove, California, pp. 28-30, Nov. 2-4, 1987.

2. A. T. Fam, "Space-Time Duality in Digital Filter Structures," *IEEE Trans. Acoust., Speech, Signal Processing*, vol. 31, no. 3, pp. 550-556, June 1983.

3. A. T. Fam, "A Multi-Signal Bus Architecture for FIR Filters with Single Bit Coefficients," *ICASSP-84*, San Diego, pp. 11.11.1-11.11.3, March 19-21, 1984.

4. A. T. Fam, "Optimal Partitioning and Redundancy Removal in Computing Partial Sums," *IEEE Trans. Comput.*, vol. 36, no. 10, pp. 1137-1143, October 1987.

8.2 Publications Resulting from Effort

1. Tapio Saramäki and Adly T. Fam, "Properties and Structure of Linear-Phase FIR Filters Based on Switching and Resetting of IIR Filters," To be presented at *ISCAS'90*, New Orleans, Louisiana, May 1-3, 1990.

2. Chimin Tsai and Adly T. Fam, "Efficient Linear-Phase Filters Based on Switching and Time Reversal," *ISCAS'90*, New Orleans, Louisiana, May 1-3, 1990.

3. Tein-Hsiang Lin and Adly T. Fam, "A Hierarchical Approach for the Design of Two-Dimensional Fault-Tolerant Systolic Arrays," Submitted to the *1990 International Conference on Parallel Processing*, St. Charles, Illinois, Aug. 13-17, 1990.

4. Adly T. Fam and Yong H. Lee, "Selection Filters and Commutativity with Memoryless Nonlinearities," *ISCAS'90*, New Orleans, Louisiana, May 1-3, 1990.

5. Sung-Jea Ko, Yong Hoon Lee, and Adly T. Fam, "Efficient Implementation of One-Dimensional Recursive Median Filters," Submitted to *IEEE Trans. Circuits Syst.*

6. Adly T. Fam, "The Volume of the Coefficient Space Stability Domain of Monic Polynomials," *ISCAS'89*, Portland, Oregon, pp. 1780-1783, May 8-11, 1989.

7. Adly T. Fam, "Generating Edges of *D*-Stable Polynomials," *28th CDC*, Tampa, Florida, pp. 2271-2272, Dec. 13-15, 1989.

8.3 Presentations at RADC

The following presentations and discussions were part of a final report visit to RADC on Friday, Feb. 9, 1990.

1. Tsai, "Efficient Linear Phase Filters Based on Switching and Time Reversal"

2. Klavoon, "VLSI FIR Filter Design Based on Optimal Reduction"

3. Lin, "A Hierarchical Approach for the Design of Two-Dimensional Fault-Tolerant Systolic Arrays"

4. Fam, "RNS with Prime Power Moduli"

5. Fam, Discussion of:

-The Coefficient Space Geometry of Polynomials

-Work on Selection Filters with Yong Lee

-Work on Switching and Resetting with Tapio Saramäki

-Further Research, including extension of above topics and the Fast Chirp Filter and Transform. A white paper in the form of a preliminary proposal entitled "Fast Chirp Filtering and Arithmetic Intensive Signal Processing" submitted to John Patti.

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