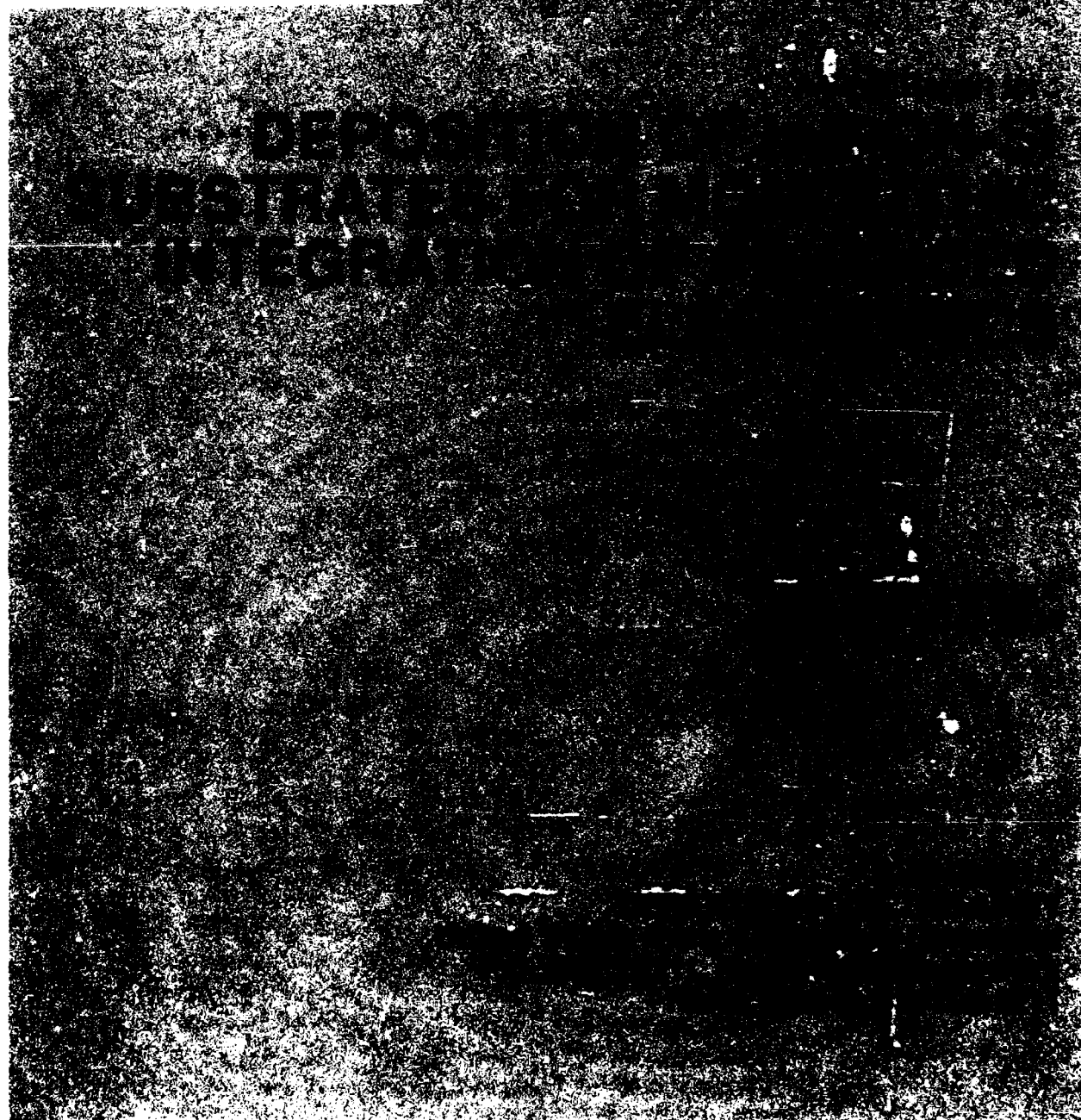


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4. TITLE AND SUBTITLE Deposition of InP-on-Si Substrates for Monolithic Integration of Advanced Electronics			5. FUNDING NUMBERS DAAL03-88-C-0034	
6. AUTHOR(S) Stanley M. Vernon				
7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES) Spire Corporation One Patriots Park Bedford, MA 01730-2396			8. PERFORMING ORGANIZATION REPORT NUMBER	
9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES) U. S. Army Research Office P. O. Box 12211 Research Triangle Park, NC 27709-2211			10. SPONSORING/MONITORING AGENCY REPORT NUMBER ARO 26573.1-EL-SBI	
11. SUPPLEMENTARY NOTES The view, opinions and/or findings contained in this report are those of the author(s) and should not be construed as an official Department of the Army position, policy, or decision, unless so designated by other documentation.				
12a. DISTRIBUTION/AVAILABILITY STATEMENT Approved for public release; distribution unlimited.			12b. DISTRIBUTION CODE	
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14. SUBJECT TERMS InP, InGaAs, heteroepitaxy, MOCVD			15. NUMBER OF PAGES 46	
			16. PRICE CODE	
17. SECURITY CLASSIFICATION OF REPORT UNCLASSIFIED	18. SECURITY CLASSIFICATION OF THIS PAGE UNCLASSIFIED	19. SECURITY CLASSIFICATION OF ABSTRACT UNCLASSIFIED	20. LIMITATION OF ABSTRACT UL	

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A Final Report for:
DEPOSITION OF InP-ON-Si SUBSTRATES FOR
MONOLITHIC INTEGRATION OF ADVANCED ELECTRONICS

S. M. Vernon

19 April 1991

U.S. ARMY RESEARCH OFFICE

Under Contract:
DAAL03-88-C-0034 10/88 - 12/90

Submitted to:
DEPARTMENT OF THE ARMY
United States Army Laboratory Command
P.O. Box 12211, Research Triangle Park
North Carolina 27709-2211

Submitted by:
SPIRE CORPORATION
One Patriots Park
Bedford, MA 01730-2396

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SECTION 1

INTRODUCTION

The on-chip integration of photonic and electronic devices would facilitate improvements in high-speed signal processing and lead to rapid progress in the state of the art of electronic systems. Figure 1-1 shows the concept of such an optoelectronic integrated circuit (OEIC) used for high-speed signal processing. These objectives necessitate advances in the field of semiconductor materials; one promising one that has seen much recent growth is the heteroepitaxy of III-V semiconductors on Si substrates. A variety of GaAs-on-Si devices are now being realized in many research and development laboratories worldwide. Less work has been devoted to the growth of InP on Si despite the importance of InP as an excellent choice for many applications in the realm of IR lasers and high-speed/high-power transistors. Our program to develop InP-on-Si structures is based on the extensive foundation of technology developed by us and others in the fields of heteroepitaxy on Si and growth of InP.

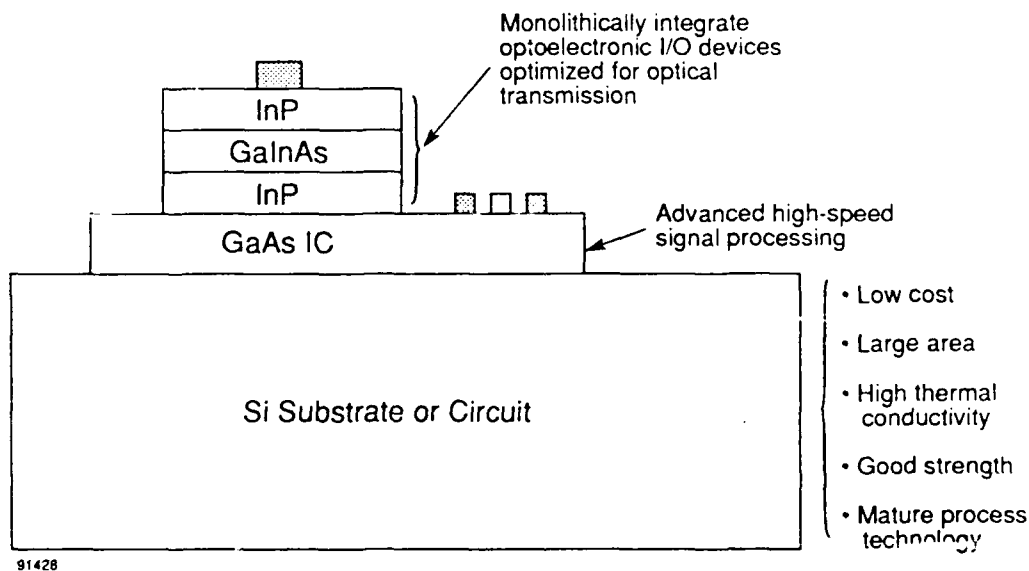


FIGURE 1-1. SCHEMATIC REPRESENTATION OF AN OPTOELECTRONIC INTEGRATED CIRCUIT ENVISIONED AS AN APPLICATION OF THIS RESEARCH.

The technical approach of this program is the deposition of thin-film InP and InP-In_xGa_{1-x}As device structures heteroepitaxially onto Si substrates by the metalorganic chemical vapor deposition technique. The use of a GaAs intermediate buffer layer has been found in Phase I to be of great utility in achieving high-quality InP layers, and also allows for the integration of InP and GaAs devices on a large-area, low-cost, mechanically superior Si wafer. In Phase II we have seen dramatic improvements in the quality of InP layers on GaAs/Si substrates by the use of a thermal-cycle growth (TCG) method, in which layer thickness is built up by a repetitive deposition-anneal-cooldown procedure. The approach of studying the InP-GaAs-Si structure makes use of our well-developed GaAs-on-Si growth process, and provides an intermediate step to help accommodate the 8% lattice mismatch between Si and InP.

The Phase II R&D program described here has shown encouraging progress, which may lead to a technology which has several important benefits. One is to replace the InP bulk substrates, which are fragile, of low thermal conductivity, available only in small diameters, and quite expensive, with Si substrates which have advantages in all the aforementioned categories. Another is to enable integrated circuits (of Si or GaAs) to communicate optically with other chips, using silica fiber optics, instead of electrically, via wire data busses. This important new capability would "harden" the system and aid in its survivability by eliminating interference pickup on the data bus from hostile jamming and/or electromagnetic pulse effects from nuclear explosions. Lasers and LED sources and photodetectors, sensitive at the 1.5 μ m attenuation minimum will allow large interconnect lengths and high data rates, while the monolithic integration of these detectors and sources, made possible by the use of heteroepitaxial structures, will simultaneously utilize the advanced expertise available in processing and designing logic circuitry.

SECTION 2

BASIC GOALS OF THE PHASE II PROGRAM

The basic tasks of the Phase II effort were as follows:

- Improvement of the material quality of InP on Si.
- Characterization of heteroepitaxial InP films.
- Development of a growth process for high-quality, lattice-matched $\text{In}_x\text{Ga}_{1-x}\text{As}$ on InP.
- Characterization of lattice-matched $\text{In}_x\text{Ga}_{1-x}\text{As}$ layers.
- Fabrication and testing of PIN and JFET devices, using the $\text{In}_x\text{Ga}_{1-x}\text{As}$ -InP-GaAs-Si structures here.

All tasks were successfully completed.

SECTION 3

OVERALL PROGRAM SUMMARY

The accomplishments of this program are summarized briefly below:

3.1 SUMMARY OF PHASE I

Listed below is a brief summary of the results achieved during our Phase I program:

- High-quality single-crystal InP films were deposited on Si substrates by the use of a GaAs intermediate layer.
- InP films were deposited directly onto Si substrates under a variety of nucleation conditions, but all films were polycrystalline.
- Surface morphologies of the best InP-on GaAs-on Si films were spectacular and comparable to GaAs-on-Si films.
- Double-crystal X-ray rocking curve analysis showed that the InP quality improves with increasing InP thickness, but is fairly insensitive to GaAs thickness.
- InP homoepitaxial films grown in this program show state-of-the-art crystal quality.
- Analysis by planview TEM shows that InP layers on GaAs-on-Si substrates have $\approx 10^8$ defects/cm², while InP-on-Si samples are polycrystalline.
- The InP-GaAs interface appears to generate as many dislocations as does the GaAs-Si interface.
- InP-GaAs-Si samples showed reasonably good photoluminescence at room temperature and 4 K, and that the PL full width half maximum at 300 K is fairly insensitive to the GaAs buffer thickness.

3.2 SUMMARY OF PHASE II ACCOMPLISHMENTS

- Developed annealing techniques for InP on Si (up to 875°, no surface degradation, no PH₃)
- Improved InP on Si by TCG

- Characterized InP on Si (and on GaAs and GaAs on Si) samples: by TEM, X-ray, PL, Surface, I-V-T, DLTS, minority-carrier lifetime measurements, Hall, and Polaron. Xray FWHM=179 sec, $\mu(77\text{ K})=23000\text{cm}^2/\text{V-sec}$
- Developed growth of lattice-matched $\text{In}_x\text{Ga}_{1-x}\text{As}$ on InP
- Designed JFETs and PINs device structures for $\text{In}_x\text{Ga}_{1-x}\text{As-InP}$ (on InP, GaAs, and GaAs-on-Si substrates)
- Developed fabrication process for PINs and JFETs on InP, GaAs, and GaAs-on-Si substrates.
- Calibrated growth of PINs and JFETs on InP, GaAs, and GaAs-on-Si substrates.
- Grew, fabricated, and tested PINs and JFETs on InP, GaAs, and GaAs-on-Si substrates.

SECTION 4

PROGRAM ORGANIZATION

The program was directed by Stanley M. Vernon of Spire Corporation, which performed all MOCVD growths and annealing, all device fabrication and testing, and much of the material characterization. Several outside collaborations were utilized to help characterize the structures. Profs. W.A. Anderson and C.R. Wie of SUNY at Buffalo performed double-crystal X-ray rocking curve analysis, DLTS, and diode measurements during the first year of the Phase II. Low-temperature photoluminescence was carried out at UCLA by Dr. N.M. Haegel and Mr. V.P. Mazzi, and transmission electron microscopy was provided by Dr. M.M. Al-Jassim of the Solar Energy Research Institute, Golden CO.

SECTION 5

TECHNICAL APPROACH

5.1 FILM GROWTH

All films were grown by atmospheric-pressure MOCVD in a Spire built SPI-MO CVD 450™. InP films were deposited onto InP, GaAs, and GaAs-on-Si substrates in a side-by-side fashion using the "450" reactor, which has a capacity of five two-inch-diameter wafers per run. The GaAs-on-Si substrates were formed previously in a separate growth run using the "two-step" method.⁽¹⁾ This procedure basically consists of a high-temperature bakeout (at $\approx 1000^\circ\text{C}$), a low-temperature nucleation step (at $\approx 400^\circ\text{C}$), and film growth at $\approx 700^\circ\text{C}$. Some of the GaAs-on-Si substrates were also treated with a thermal-cycle growth (TCG) process,⁽²⁾ which consists of deposition at 700°C of about $2000\text{\AA}$ of GaAs, annealing at $\approx 900^\circ\text{C}$, cooldown to room temperature, and repetition of these steps about five times. For the growth of some InP samples, TCG of InP was performed in a manner analogous to that used for GaAs.

5.2 MATERIAL CHARACTERIZATION

The films grown in this program, including InP layers on InP, GaAs, and GaAs-on-Si substrates, have been characterized by numerous techniques, as shown below.

5.2.1 Physical Properties

The three techniques used to study the physical structure of the samples are:

- Nomarski interference-contrast microscopy. This is performed at Spire and used on a run-by-run basis to examine the surface morphology of the films, at magnifications up to 1000X.
- Double-crystal X-ray rocking curve analysis. This technique is used to assess the structural perfection of the various layers, as well as to determine the alloy composition of ternary ($\text{In}_x\text{Ga}_{1-x}\text{As}$) layers, with a high degree of precision. During the first year of the program, the X-ray measurements were performed at SUNY at Buffalo; at the start of the second year, Spire set up its own high-resolution diffractometer, and the measurements have been carried out in house since then.
- Transmission electron microscopy. This powerful technique is used to image the defect structure of the samples, at magnifications up to several hundred thousand times. Structures can be examined in cross-section, to reveal the details of the propagation of the defects, or in plan-view, to accurately determine the defect density over a large area.

5.2.2 Electrical Properties

The samples have been studied in terms of electronic transport properties, by these methods:

- Hall effect. Performed at Spire, at both 300 and 77 K, to measure majority-carrier mobility and net carrier concentration.
- Deep-level transient spectroscopy. Performed at SUNY at Buffalo, this analysis is used to identify and quantify the deep-level traps present in the various structures.
- Electrochemical C-V profiling. This technique, commonly called the "Polaron," measures carrier-concentration versus depth, by combining etch and a C-V analysis techniques in an automated fashion.

5.2.3 Optical Properties

- Photoluminescence. This method of studying the optical properties of the film reveals details about the stress present in the layer, as well as the impurities, and optically active defects present. Analysis was carried out at 4 K at UCLA.
- Photoluminescence decay, with time-resolved photon counting.⁽³⁾ This method, which looks at the transient response of the carriers in a crystal to a pulse of light, is used to accurately determine the minority-carrier lifetime of the semiconductor, as well as the surface recombination velocity.

SECTION 6

THERMAL-CYCLE GROWTH OF InP ON GaAs AND Si

The first experiments performed in Phase II were to learn how to grow the best quality InP on Si possible (i.e., to minimize dislocation density).

The first step was to determine experimentally the minimum PH_3 overpressure to prevent the InP from dissociating in the reactor at the anneal temperature (time held at anneal temperature was 30 min.). Temperatures up to 850°C were studied. The results of this trial were determined by careful Nomarski interference-contrast microscopy examination of the surface of InP on InP, GaAs, and GaAs-on-Si substrates (to check for surface degradation (loss of P)), Hall measurements, and room temperature photoluminescence (PL). The PH_3 partial pressures were varied between 7.5 torr and 56 torr. It was found that a maximum temperature of 800°C could be used with a PH_3 flow of 80 sccm, and a main H_2 flow of 1.0 sLPM, resulting in a PH_3 partial pressure of 56 torr.

Next, experiments with the TCG of InP were done using GaAs substrates. After a process was worked out, it was then easily transferred to GaAs-on-Si substrates. The optimum number of cycles (three), and thickness per cycle ($1\text{ }\mu\text{m}$) were set from past experience with the thermal-cycle growth (TCG) of GaAs on Si.⁽²⁾ The test structure studied is shown in Figure 6-1.

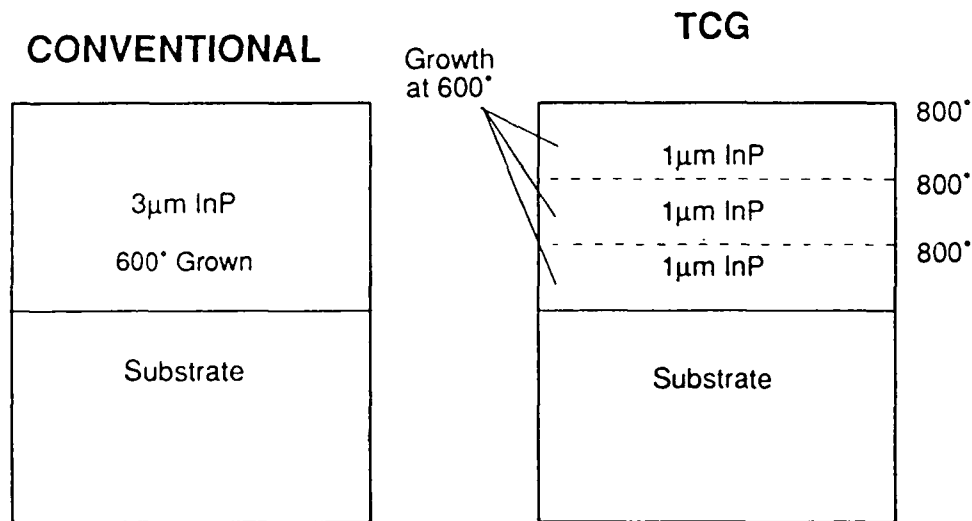


FIGURE 6-1. InP HETEROEPITAXIAL STRUCTURES STUDIED DURING THESE EXPERIMENTS.

Further trials revealed that actually we could go to an annealing temperature as high as 875°C for the TCG process without InP-surface degradation, and using the same partial pressure of PH₃. A number of samples were grown by this new TCG process and characterized. Much to our disappointment, these samples did not show any improvement over the films grown with the 800°C TCG process. It seems as if the nature of InP is such that the defects cannot be annealed out as easily as in GaAs, where the TCG process has been much more successful. Recently, it has been shown that a graded layer of In_xGa_{1-x}As (x graded from 0 to 0.53) is effective at reducing the dislocation density in InP on GaAs/Si films,⁽⁴⁾ and this is the avenue which we will be pursuing in the future.

SECTION 7
THERMAL-CYCLE ANNEALING (TCA)
OF $\text{In}_x\text{Ga}_{1-x}\text{As}$ -InP STRUCTURES ON InP,
GaAs, AND GaAs-on-Si SUBSTRATES

Another alternative process was developed in order to minimize the use of pyrophoric PH_3 in large quantities during the TCG process. This new process involved the use of a lattice-matched capping layer of $\text{In}_x\text{Ga}_{1-x}\text{As}$, and annealing under an AsH_3 overpressure. Annealing temperatures as high as 900°C were achieved, but most samples studied used an anneal temperature of 875°C . Two alternative processes were developed: One method consisted of annealing the $\text{In}_x\text{Ga}_{1-x}\text{As}$ -capped InP, with the wafer in the normal "face-up" position. The wafer surface would severely degrade, due to the loss of In from the $\text{In}_x\text{Ga}_{1-x}\text{As}$; but the underlying InP would not be harmed. A selective etch would be used to remove the top layer ($\text{In}_x\text{Ga}_{1-x}\text{As}$), and thus revealing the annealed InP film. Another recipe would involve a similar annealing of an $\text{In}_x\text{Ga}_{1-x}\text{As}$ -capped InP film, with the wafer placed "face-down" on the susceptor. This served to "seal" the $\text{In}_x\text{Ga}_{1-x}\text{As}$ and prevent In loss from the surface, thus eliminating the need for the selective-etch step. Both variations of the TCA method gave similar defect density results; however, neither was superior to the best results achieved with our TCG process, even though the maximum annealing temperature was 75°C higher. This is due to the fact that TCA is not as effective at reducing the dislocation density as is the TCG process. This has been seen previously for the case of GaAs on Si; unfortunately, it is also true for InP on Si. The TCA experiments and results are described in more detail in Appendix B.

SECTION 8

RESULTS OF InP THERMAL-CYCLE GROWTH (TCG) EXPERIMENTS ON InP, GaAs, AND GaAs-on-Si SUBSTRATES.

A number of samples of InP, deposited by thermal-cycle growth (TCG), were analyzed by numerous characterization techniques and compared to others deposited by conventional growth; the data are presented and discussed in the following sections:

Figure 8-1 is schematic representation of the thermal-cycle growth process used throughout these experiments. Figure 8-2 shows the details of time-temperature schedule used for the TCG process. For InP, the anneal temperature is 800°C, the growth temperature is 600°, and the ambient contains 56 torr of PH₃; for GaAs TCG, the anneal temperature is 950°C, the growth is done at 700°, and the ambient contains 36 torr of AsH₃.

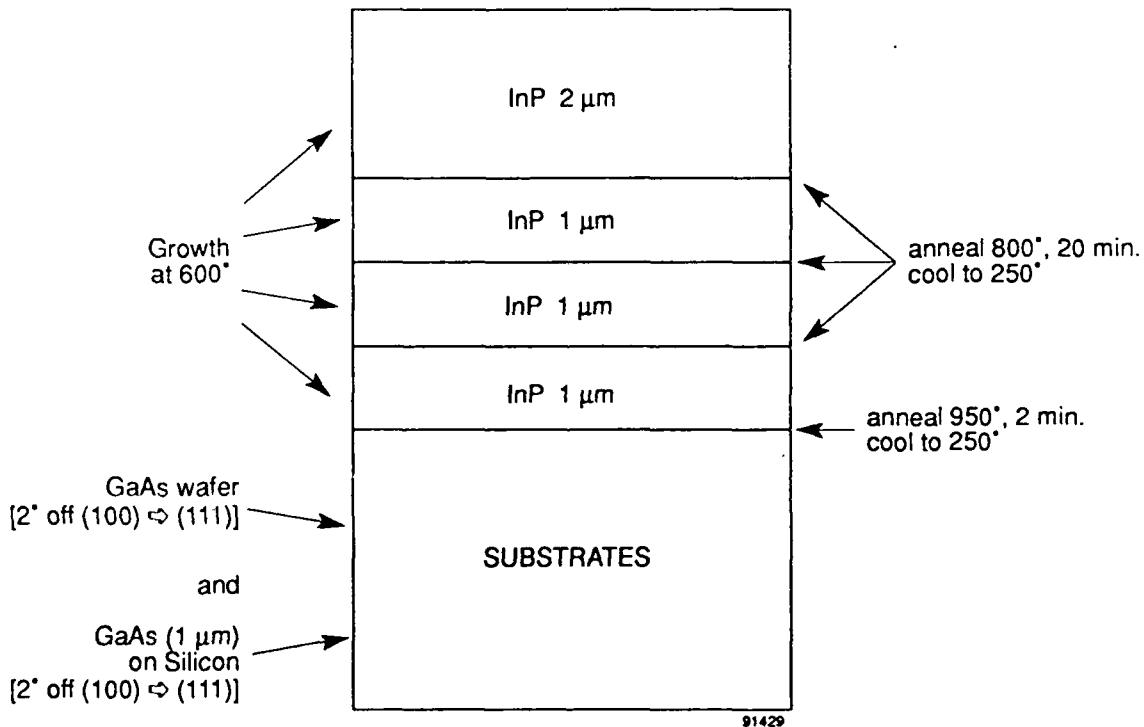


FIGURE 8-1. SCHEMATIC REPRESENTATION OF THE InP THERMAL-CYCLE GROWTH (TCG) PROCESS.

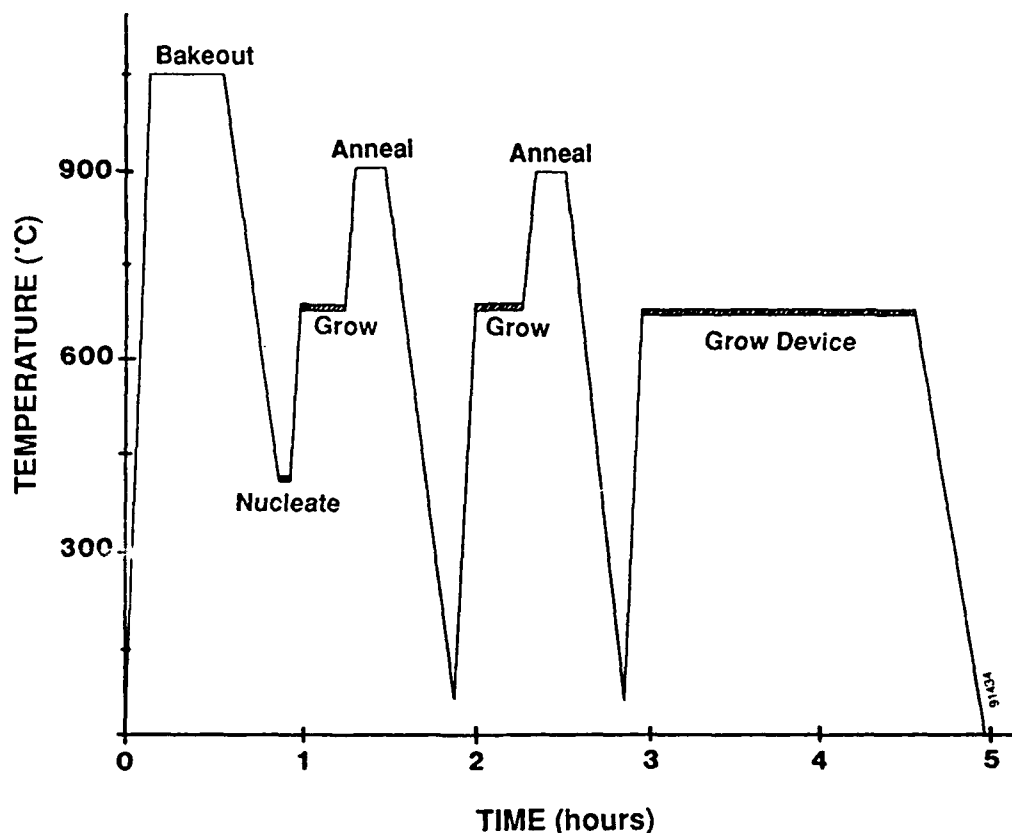


FIGURE 8-2. TIME-TEMPERATURE CYCLE USED FOR THE THERMAL-CYCLE GROWTH (TCG) PROCESS.

8.1 PHYSICAL PROPERTIES

The surface morphologies of InP deposited on GaAs by the two different processes are shown in Figure 8-3. The TCG sample has a much smoother morphology. This correlates to the lower density of stacking faults present in the layer; stacking faults, which are fairly easy to remove by annealing,⁽⁵⁾ often cause fairly rough surface features to appear. The morphology of InP-on-GaAs-on-Si samples are quite similar to those of InP on GaAs.

A double-crystal X-ray rocking curve of InP-on-GaAs-on-Si is shown in Figure 8-4, with a more detailed scan of the InP layer shown in Figure 8-5. The sample studied here was not annealed. The best values obtained for the full width half maximum values are listed in Table 8-1.

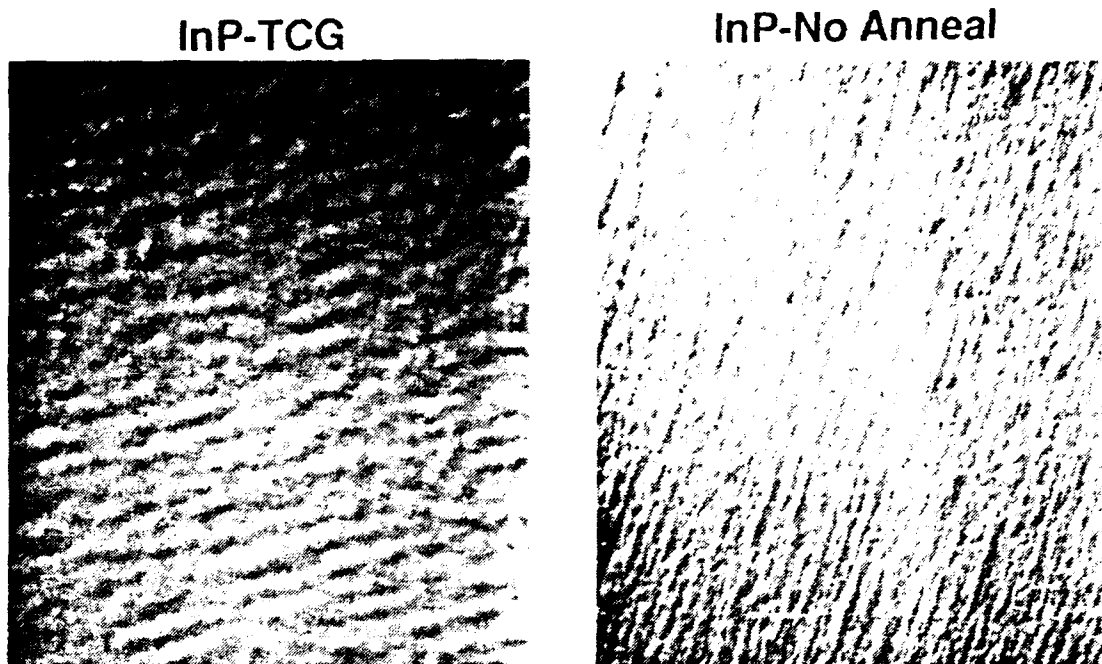


FIGURE 8-3. NOMARSKY MICROGRAPHS OF InP ON GaAs GROWN WITH AND WITHOUT THE THERMAL-CYCLE GROWTH (TCG) PROCESS.

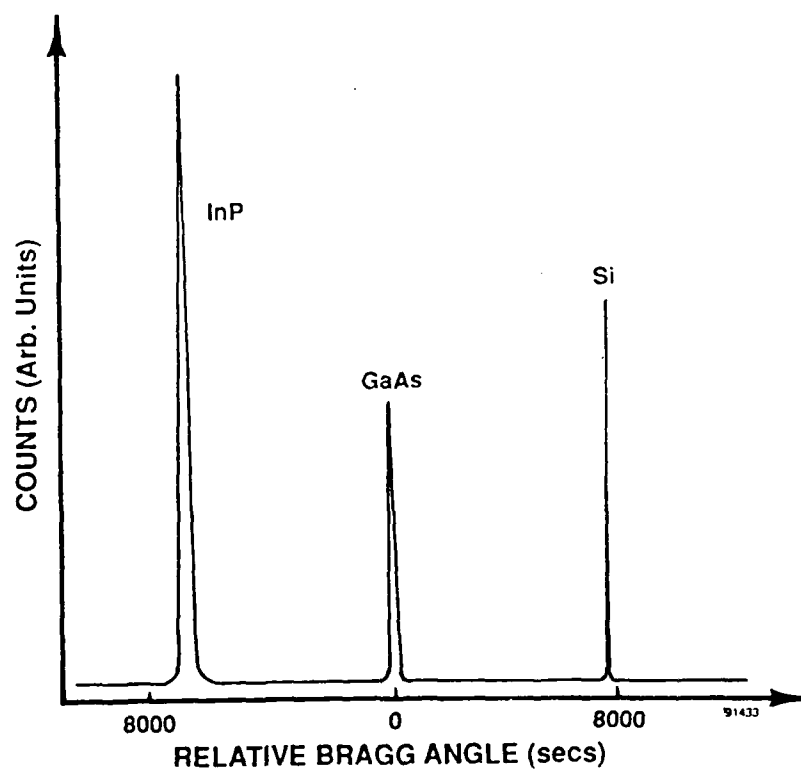


FIGURE 8-4. TYPICAL DOUBLE-CRYSTAL X-RAY ROCKING CURVE FOR AN InP-GaAs-Si SAMPLE.

FWHM = 301 arc-seconds

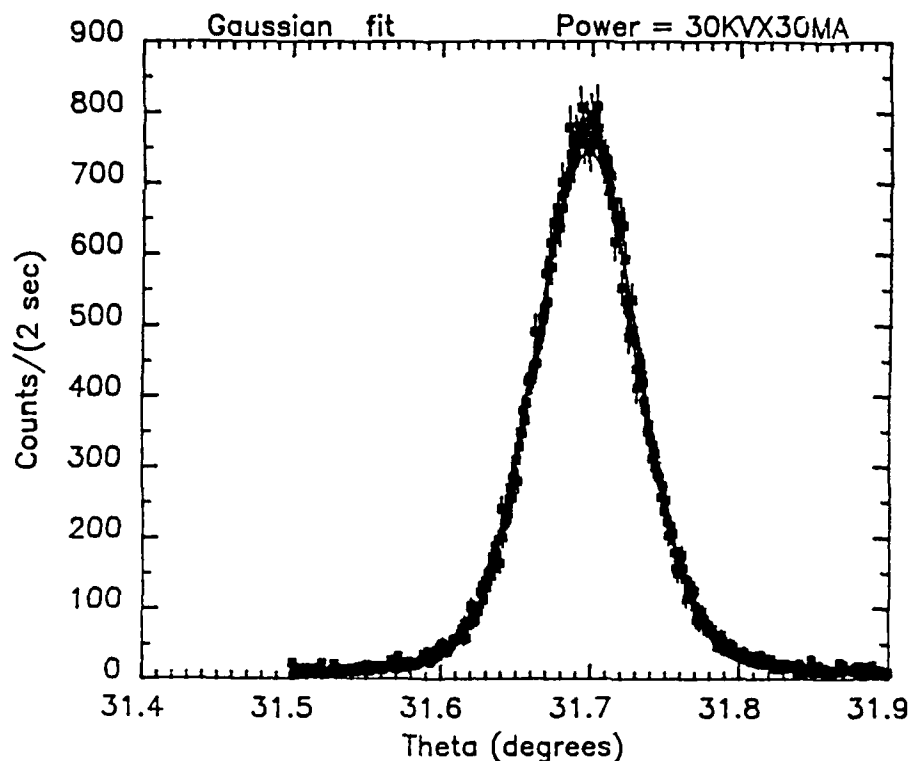


FIGURE 8-5. DETAIL OF THE ROCKING-CURVE PEAK FOR THE InP LAYER OF AN InP-GaAs-Si SAMPLE.

TABLE 8-1. DOUBLE-CRYSTAL X-RAY ROCKING CURVE DATA FOR InP GROWN WITH AND WITHOUT THERMAL-CYCLE GROWTH (TCG) ON FOUR DIFFERENT SUBSTRATES, SIDE BY SIDE.

SUBSTRATES	FWHM (arc-sec)	
	InP	TCG InP
InP	15	15
GaAs	236	179
GaAs/Si	340	273
TCG GaAs/Si	286	194

Note: In all samples, InP layer = 3 μm thick, and GaAs layer = 2 μm thick; the TCG process for the GaAs-on-Si growth involved 3 cycles at 950°C.

The trends evident here are that TCG InP is better than unannealed InP, and that TCG GaAs/Si substrates are better (for the growth of InP) than standard GaAs/Si, and are almost comparable in quality to bulk GaAs wafers.

Figure 8-6 shows a planview TEM comparison of regular InP and TCG InP, each grown on TCG GaAs/Si substrates. The TCG InP process resulted in a reduction in dislocation density of only approximately a factor of three. Similar comparisons in the GaAs-on-Si studies show that TCG is much more effective; Figure 8-7 shows a typical comparison of GaAs on Si versus TCG GaAs on Si, where the dislocation density has been reduced by a factor of twenty.

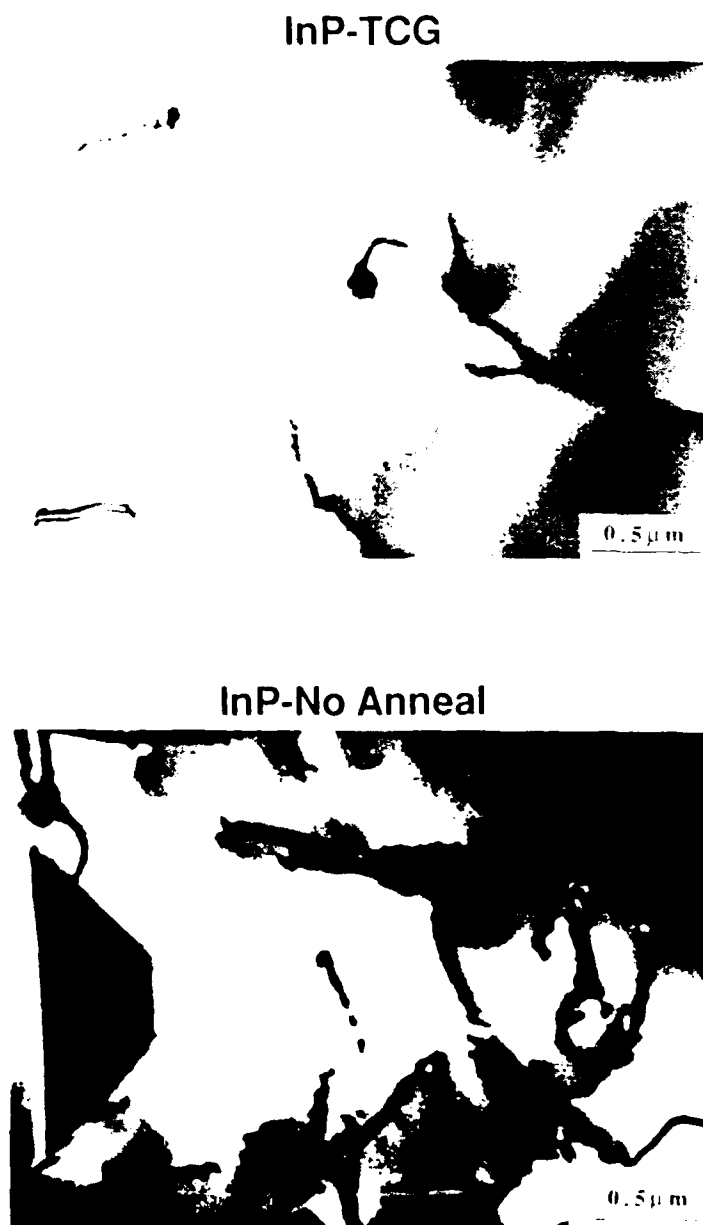


FIGURE 8-6. PLANVIEW TEM MICROGRAPHS OF InP-GaAs-Si SAMPLES, GROWN WITH AND WITHOUT THE InP TCG PROCESS.

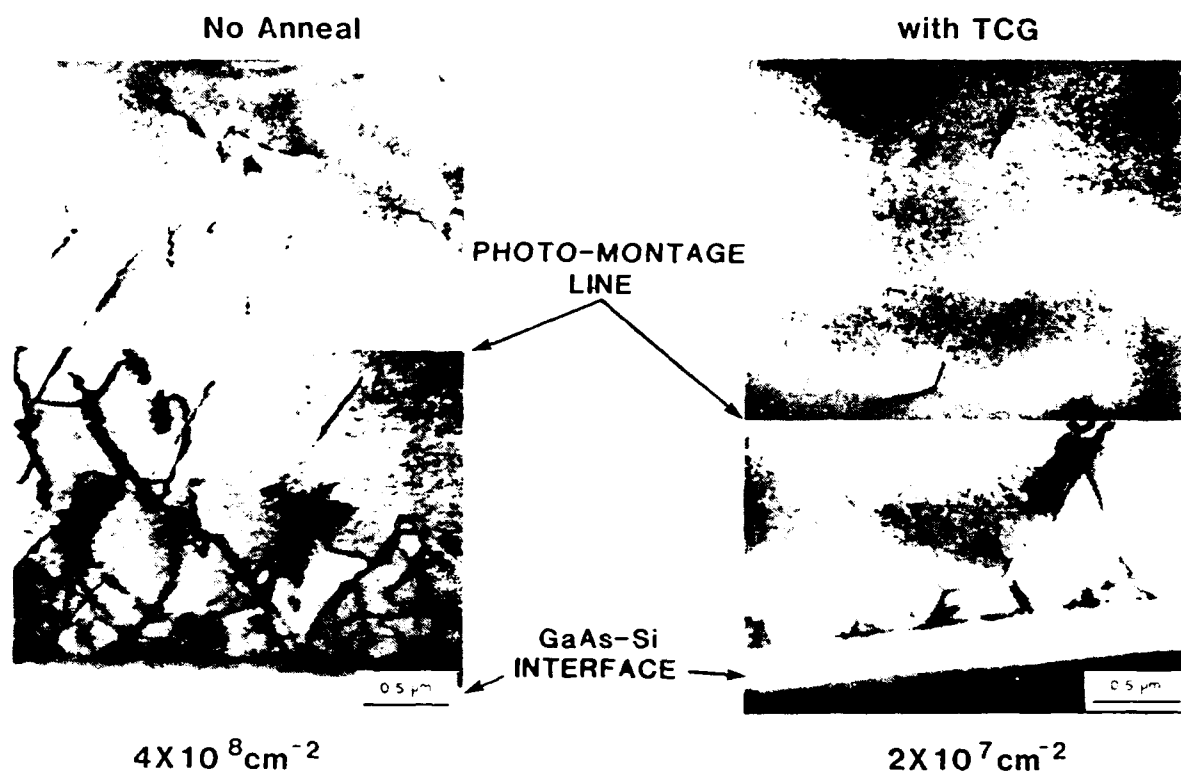


FIGURE 8-7. CROSS-SECTIONAL TRANSMISSION ELECTRON MICROGRAPHS OF GaAs on Si GROWN WITH AND WITHOUT TCG OF GaAs.

Figure 8-8 shows cross-sectional transmission electron micrograph of an InP/GaAs/Si sample; the defects in the InP are seen to originate mostly at the GaAs-InP interface, due to the 4% lattice mismatch present, with only a few of the InP defects coming from those in the GaAs which propagate through. This explains why the quality of the InP layer is only weakly dependent on the quality of the GaAs layer on Si.

A high-resolution lattice-imaging micrograph of an InP-on-GaAs sample is shown in Figure 8-9. A uniformly-spaced array of misfit dislocations is seen at the interface, with an average spacing of $\approx 100\text{\AA}$, as expected from the mismatch between GaAs and InP.

The best results obtained for InP on GaAs, and on TCG GaAs/Si are shown in Table 8-2. Also included are the results for the TCA process discussed in Section 7.

We also tried to reduce the dislocation density in the InP by the use of a strained layer of $1000\text{\AA}$ of $\text{In}_x\text{Ga}_{1-x}\text{As}$, with $x \approx 0.65$, corresponding to a strain of $\approx 1.0\%$. A cross-sectional transmission electron micrograph of this structure is displayed in Figure 8-10. Unfortunately, this sample had a dislocation density as high as similar samples without the $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer. Closer TEM study of this sample revealed many defects originating at the InP- $\text{In}_x\text{Ga}_{1-x}\text{As}$ boundary, due to a growth problem which led to a poor interface.

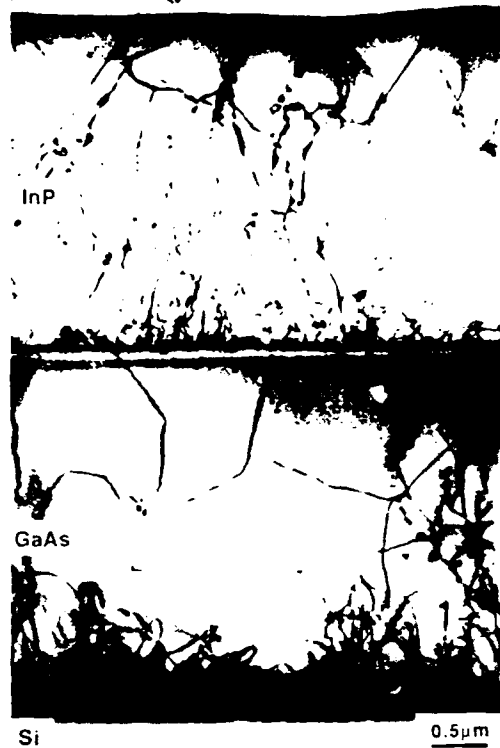


FIGURE 8-8. CROSS-SECTIONAL TRANSMISSION ELECTRON MICROGRAPH OF InP-GaAs-Si GROWN WITHOUT TCG.



FIGURE 8-9. HIGH-RESOLUTION LATTICE-IMAGING TEM MICROGRAPH (CROSS SECTION) OF THE InP-GaAs INTERFACE, SHOWING AN ARRAY OF MISFIT DISLOCATIONS.

TABLE 8-2.

DISLOCATION DENSITY IN InP HETEROEPITAXIAL FILMS,
MEASURED BY PLANVIEW TEM.

STRUCTURE	DEFECTS PER CM ²	
	On GaAs	On GaAs/Si
InP	3.9×10^8	3.0×10^8
TCA - InP	1.9×10^8	2.0×10^8
TCG - InP	6.0×10^7	9.0×10^7

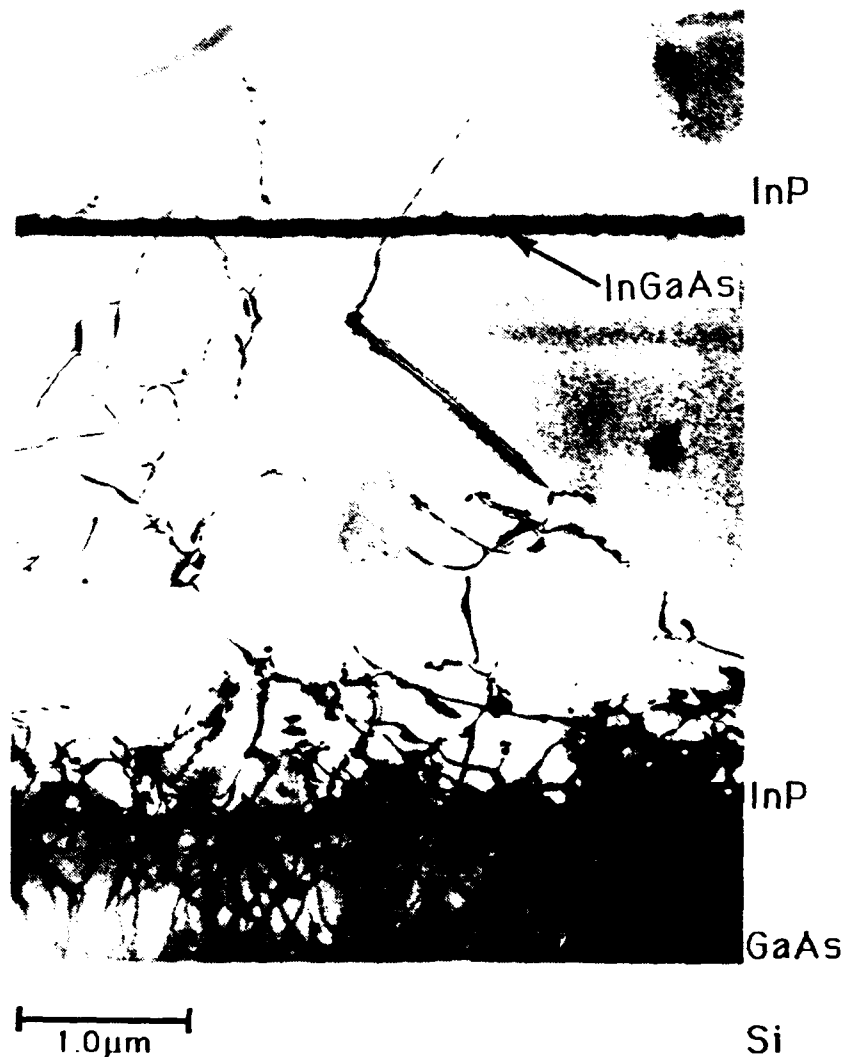


FIGURE 8-10.

CROSS-SECTION TEM OF InP-GaAs-Si USING TCG AND $\text{In}_x\text{Ga}_{1-x}\text{As}$
STRAINED LAYER.

8.2 OPTICAL PROPERTIES

Figure 8-11 shows the low-temperature photoluminescence (PL) data for InP grown on GaAs, and on TCG GaAs/Si substrates; Figure 8-12 shows similar data for InP grown by the TCG process. A comparison of the two reveals a number of features indicating that the TCG InP is superior material. The ratio of the exciton peak to the band-to-acceptor peak indicates a higher minority-carrier lifetime (τ) in the annealed samples. The fact that the exciton peaks on the TCG InP sample are higher and narrower are also indicative of the material quality. The wavelength shift of the exciton peak of InP on InP compared to InP on GaAs (shift toward higher energy) is due to the fact that InP on GaAs is in compression; for InP on GaAs on Si the shift is toward lower energy (InP is in tension), since this structure is dominated by the thermal coefficient of expansion of the Si substrate. In Figure 8-11 we note that the PL from InP on bulk GaAs and on TCG GaAs/Si are similar in shape, again showing that these two substrates usually yield similar results for InP growth.

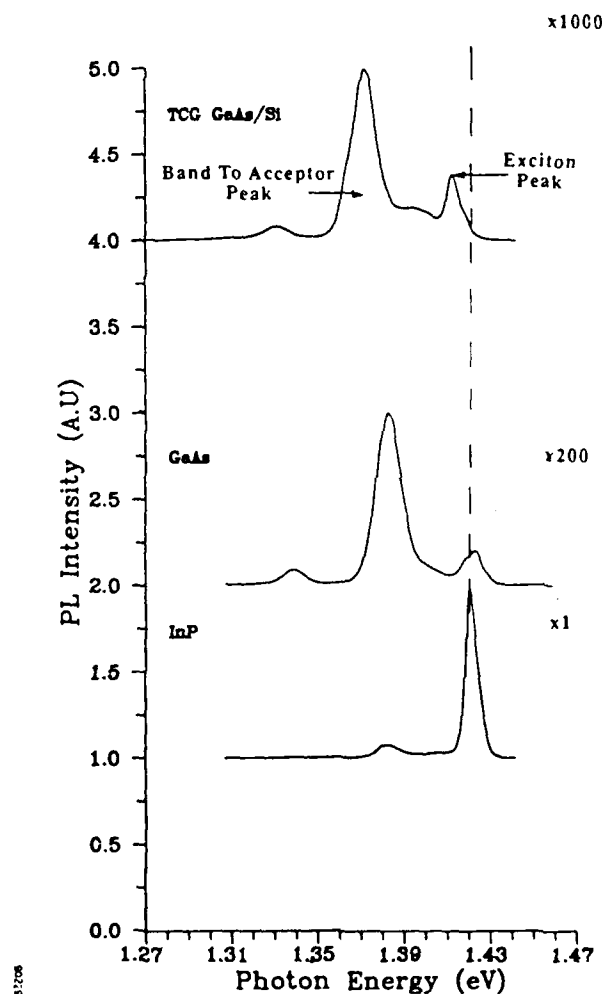


FIGURE 8-11. 4.2 K PHOTOLUMINESCENCE OF InP ON VARIOUS SUBSTRATES-CONVENTION GROWTH.

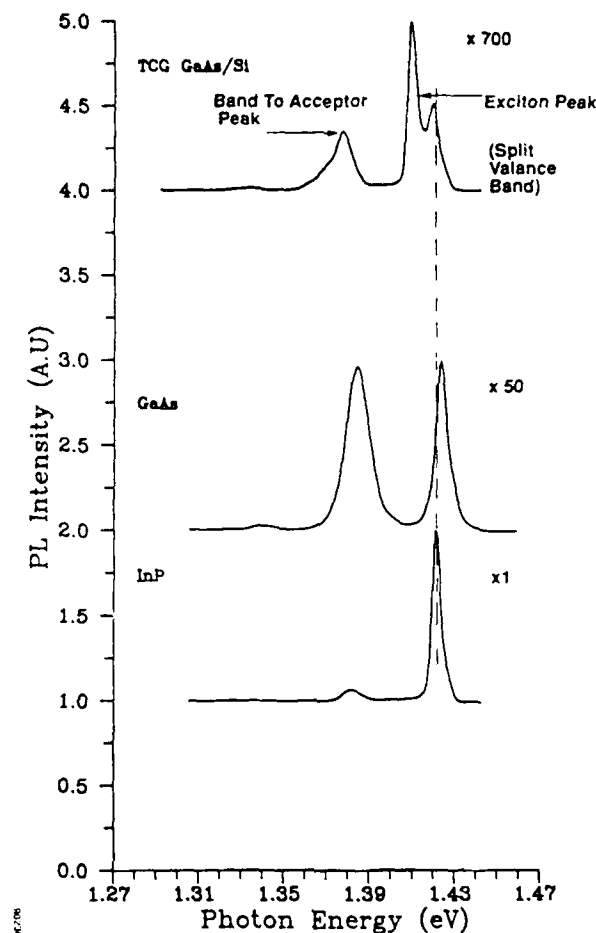


FIGURE 8-12. 4.2 K PHOTOLUMINESCENCE OF InP ON VARIOUS SUBSTRATES-TCG PROCESS.

The minority-carrier lifetimes of the various structures have been studied by the PL-decay technique;⁽³⁾ typical raw data for these measurements are shown in Figure 8-13. The results are summarized in Table 8-3.

These data show that the TCG InP on GaAs or Si has a longer minority-carrier lifetime than that of unannealed InP on similar substrates. We also note that the exact substrate structure makes little difference in the lifetime values, while the Inp on InP is an order of magnitude better. The absolute lifetime values listed here are all lower that what they would be if the measurement were not dominated by the surface recombination velocity (SRV) of the InP surface; the comparisons among the relative values are still meaningful, however. To overcome the effect of the surface recombination velocity, we would need an InP layer which is passivated by a low SRV material, or is very thick (greater than 10 μm). Neither one of these structures was practical for our studies.

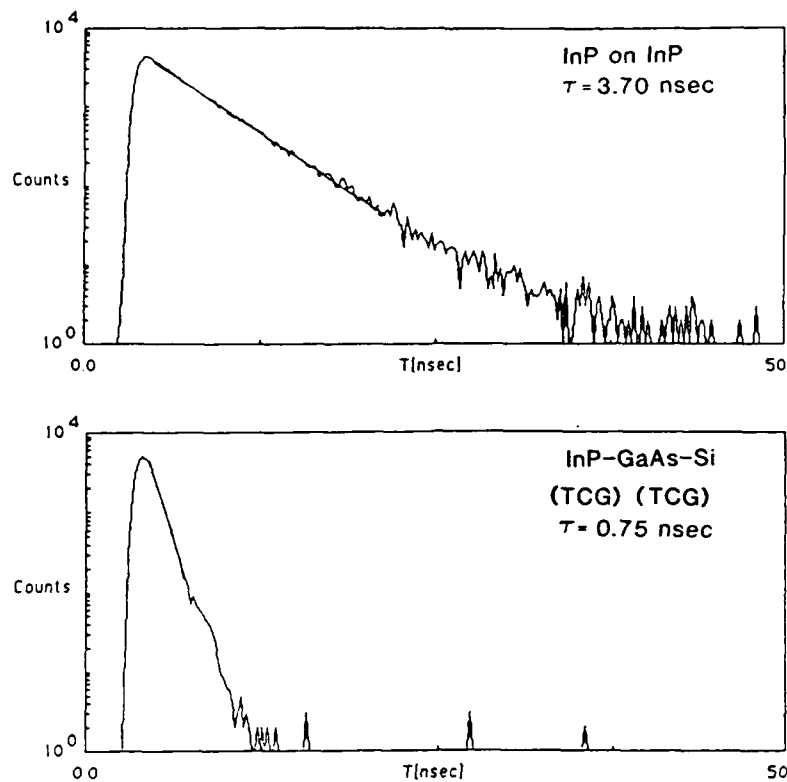


FIGURE 8-13. PHOTOLUMINESCENCE-DECAY MEASUREMENT OF InP LIFETIMES ON InP AND GaAs-on-Si SUBSTRATES.

TABLE 8-3. MINORITY-CARRIER LIFETIME IN InP LAYERS MEASURED BY PL DECAY.

SUBSTRATES	LIFETIME (nanosec)	
	InP	TCG InP
InP	3.7	2.9
GaAs	0.415	0.593
GaAs/Si	0.475	0.55
TCG GaAs/Si	0.464	0.75

Note: All InP layers are 3 μm thick, and undoped, with $n = 0.4 - 2.0 \times 10^{15} \text{ cm}^{-3}$.

8.3 ELECTRICAL PROPERTIES

Hall-effect measurements were performed, at 300 and at 77 K, on undoped InP layers, 3 μm thick, grown side by side, on semi-insulating GaAs and InP wafers. Hall measurements could not be done on samples deposited on Si substrates, due to their high conductivity. The data are presented in Tables 8-4 and 8-5.

TABLE 8-4. 300 K HALL-EFFECT DATA FOR 3- μm -THICK InP LAYERS.

EPI	SUBSTRATE	MOBILITY ($\text{cm}^2/\text{V}\cdot\text{sec}$)	CARRIERS (cm^{-3})
TCG InP	GaAs	1,920	9×10^{14}
TCG InP	InP	3,180	1.5×10^{15}
InP	GaAs	1,440	6×10^{14}
InP	InP	4,150	6×10^{14}

TABLE 8-5. 77 K HALL-EFFECT DATA FOR 3- μm -THICK InP LAYERS.

EPI	SUBSTRATE	MOBILITY ($\text{cm}^2/\text{V}\cdot\text{sec}$)	CARRIERS (cm^{-3})
TCG InP	GaAs	23,000	4×10^{14}
TCG InP	InP	47,200	9×10^{14}
InP	GaAs	8,700	2×10^{14}
InP	InP	72,200	5×10^{14}

These data clearly show the beneficial effect that TCG has on the majority transport properties of InP on GaAs. At 77 K, for unannealed InP, the ratio of the mobilities on GaAs and on InP is only 0.12; for TCG InP, this ratio increases to 0.49.

A Polaron (electrochemical capacitance versus voltage) profile is displayed in Figure 8-14 for a typical InP-on-GaAs-on-Si sample. The high background in the GaAs layer is due to diffusion of Si, which is greatly enhanced by the high dislocation density.⁽⁶⁾ The peak at the InP-GaAs interface reveals how the Si atoms tend to "pile up" at the point of high dislocation density. Thus, this interface acts as a gettering region.

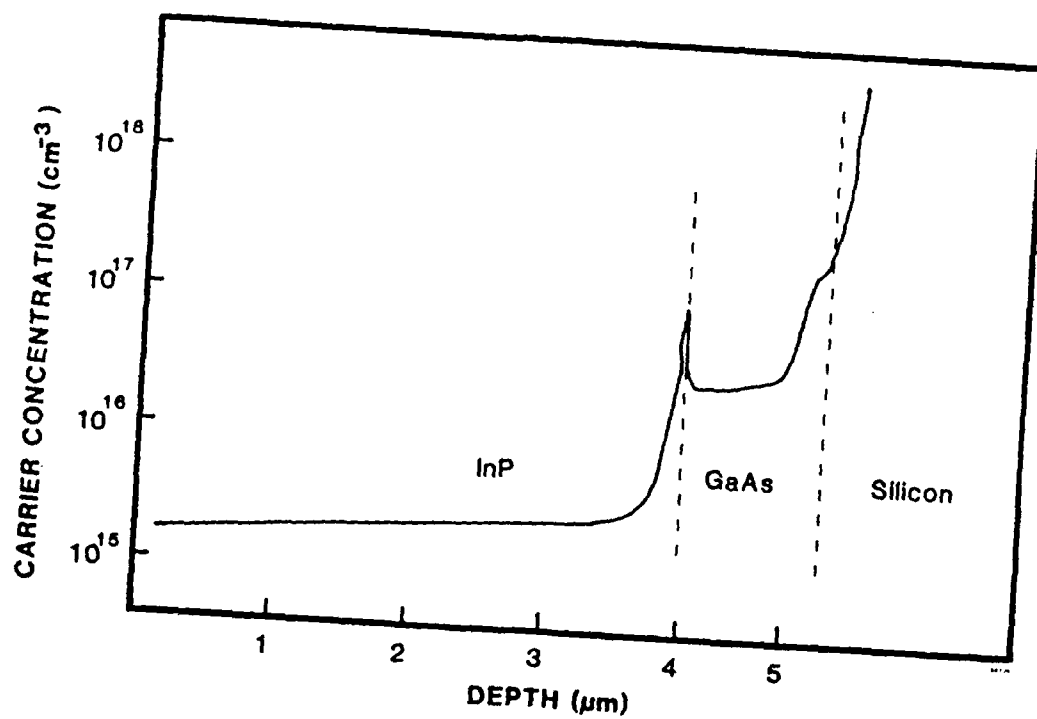


FIGURE 8-14. TYPICAL CARRIER-CONCENTRATION PROFILE (POLARON) OF AN InP-GaAs-Si STRUCTURE.

SECTION 9

GROWTH OF LATTICED-MATCHED $\text{In}_x\text{Ga}_{1-x}\text{As}$ ON InP

The MOCVD growth of $\text{In}_x\text{Ga}_{1-x}\text{As}$ latticed matched to InP was developed during the Phase II program so that the demonstration devices, PIN photodiodes and JFETs, could be fabricated in this material at the end of the program. Another use of lattice-matched $\text{In}_x\text{Ga}_{1-x}\text{As}$ was as a caplayer for the TCA process (see Section 7 above); also, lattice-mismatched $\text{In}_x\text{Ga}_{1-x}\text{As}$ layers were used to introduce strain into the structure in an attempt to reduce the dislocation density. (See Section 8.1).

The first experiments on $\text{In}_x\text{Ga}_{1-x}\text{As}$ growth were carried out at atmospheric pressure, using trimethylindium (TMI) and trimethylgallium (TMG) as the Group III source reagents. The compositional uniformity was a problem at 760 torr; this had also been noted in past experiences with the growth of GaAsP, so we quickly adopted a reactor pressure of 76 torr instead. Another problem noted was that the composition was not very reproducible; this phenomenon has plagued the growth of $\text{In}_x\text{Ga}_{1-x}\text{As}$ in many other labs, and is often due to the problem in obtaining a reproducible pick-up rate of In vapors from the solid TMI source. Therefore, we began using a liquid source, ethyldimethylindium (EDMIN) instead. This greatly improved the control over our process, although efforts to improve our composition reproducibility are still continuing, since for most critical applications, the specifications on the permissible lattice mismatched are very strict: i.e., ≈ 400 ppm ($= \Delta a/a$).

The low-pressure growth process quickly yielded excellent results in terms of compositional uniformity over a full two-inch-diameter wafer. Figure 9-1 shows the typical uniformity measured by double-crystal X-ray rocking curve analysis over the full wafer surface. The best value achieved for uniformity of lattice mismatch over a two-inch wafer is $\Delta a/a = 2.1 \times 10^{-4}$. A state-of-the-art FWHM of the double-crystal X-ray rocking curve peak of the $\text{In}_x\text{Ga}_{1-x}\text{As}$ layer of only 18 arcsec has been achieved, with a lattice mismatch of only 27 ppm ($= \Delta a/a$) (see Figure 9-2). These excellent results have been reproduced on several occasions.

Several other combinations of Group III source reagents were used, but with out success. They include trimethylindium and triethylgallium (TEG), and EDMIn and TEG. The vapor pressure of TEG is lower than that of TMG, so larger carrier flows of H_2 can be used to achieve the same delivery rate of In; this would improve our chances at reproducibility, since part of the problem may be due to the inaccuracy of the mass flow controller when forced to operate at the low end of its range. Although many other laboratories use TEG for the growth of $\text{In}_x\text{Ga}_{1-x}\text{As}$, we were unable to achieve high-quality films. Our problem seems to have been due to a contaminated TEG source. The decision was made to abandon this line of attack, so all further work was carried out with TMG and EDMIn.

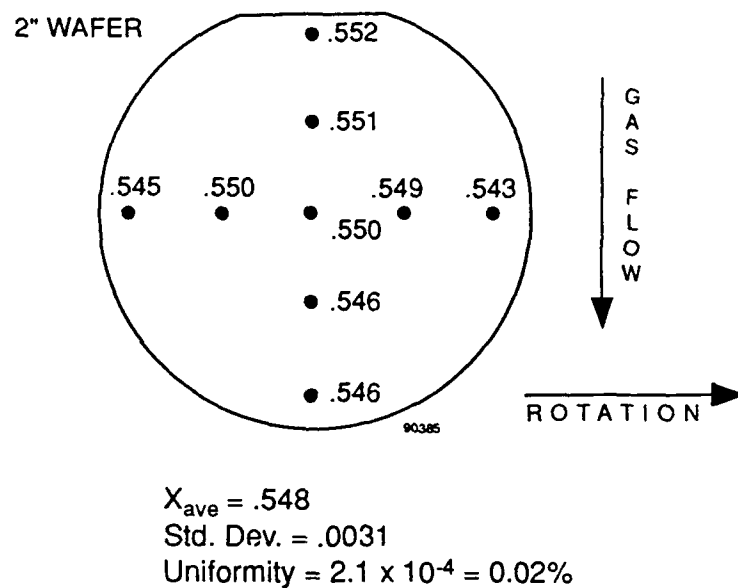


FIGURE 9-1. COMPOSITIONAL UNIFORMITY MAP OF LATTICE-MATCHED $\text{In}_x\text{Ga}_{1-x}\text{As}$ ON InP OVER A TWO-INCH WAFER.

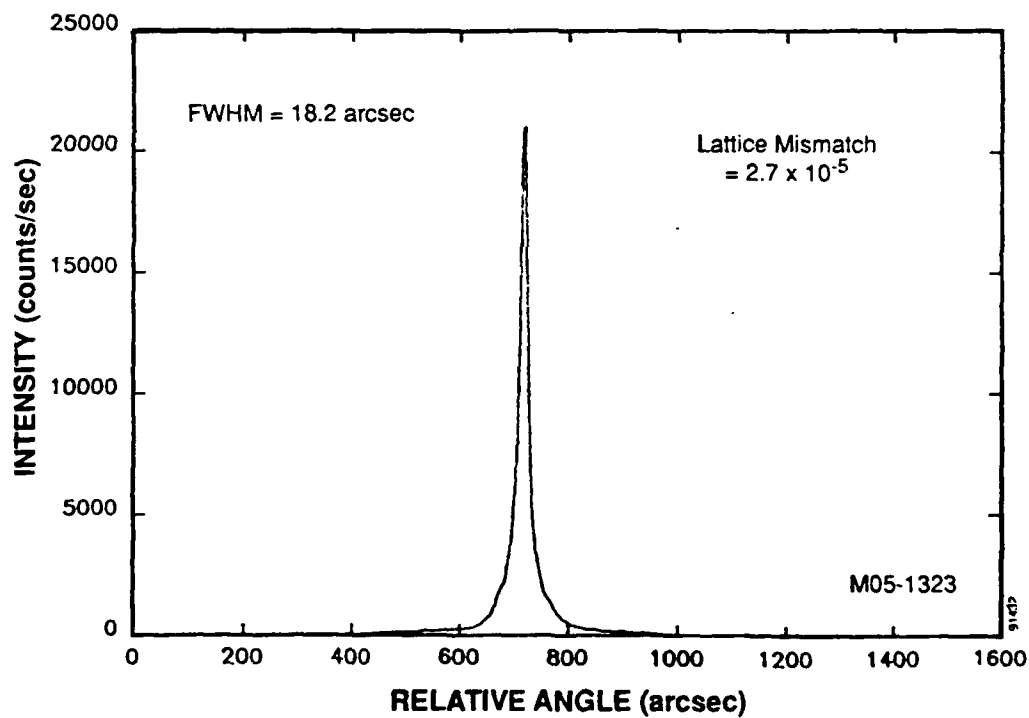


FIGURE 9-2. X-RAY ROCKING CURVE OF LATTICE-MATCHED $\text{In}_x\text{Ga}_{1-x}\text{As}$ ON InP , GROWN BY LOW-PRESSURE MOCVD.

SECTION 10

InGaAs FIELD EFFECT TRANSISTORS AND PHOTODIODES

10.1 INTRODUCTION

Junction field effect transistors (JFETs) were fabricated in InP/InGaAs epilayers on InP, GaAs, and Si substrates to test the suitability of the heteroepitaxial layers for analog and digital circuits. An FET is a good demonstration device since it is a basic building block in both linear and digital ICs. A junction FET was used, instead of the Schottky-gate MESFET typical of GaAs ICs, since gate metals form poor Schottky barriers to the low-bandgap $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ (0.75 eV vs. 1.42 eV for GaAs).

In FETs majority carriers dominate the source-to-drain current, unlike minority-carrier controlled BJTs and HBTs. Majority carrier devices are relatively undisturbed by dislocations and other material defects. At low bias, the net carrier (drift) velocity, which influences speed, may decrease as the mobility decreases due to carriers scattering off dislocations and other material defects. However, most FETs operate with a large bias such that carriers transit the FET channel at their mobility-independent saturation velocity.

The minority carrier lifetime, on the other hand, is extremely sensitive to dislocation density, and concentration and capture cross-section of material defects acting as recombination sites. PIN photodiodes were made to demonstrate minority carrier device operation in the material. PINs are key components in integrated photoreceivers, and are ideal test vehicles for Spire, since characterization facilities for quantum efficiency already exist.

10.2 MOCVD EPITAXIAL DEVICE LAYER DESIGN AND GROWTH

10.2.1 Junction Field-Effect Transistor (JFET)

Although it is possible to grow a single InP/InGaAs epilayer structure for the monolithic integration of both a JFET and a photodiode, for this effort we decided to grow separate structures for each. This enabled us to use optimum dopings and thicknesses for each device, including etch-stop layers so that wet chemical etches would stop at precise depths in the devices, eliminating the need to depend on pre-determined, doping-dependent etch rates during device processing.

Figure 10-1 shows the InGaAs/InP JFET layer structure. The top gate layer of P^+InP forms a P-N heterojunction with the $\text{n-In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel. The reverse-biased depletion region of this junction extends mainly into the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ channel and controls the electron flow between source and drain in the JFET.

A $\text{P}^+\text{InP}/\text{N-InGaAs}$ heterojunction was used as the gate junction instead of a $\text{P}^+\text{InGaAs}/\text{N-InGaAs}$ homojunction, since any viable manufacturing process will need an etch stop such as an InGaAs/InP interface between the gate and FET channel layer. The etch stop allows the InP gate to be defined and the source and drain regions cleared of InP by a selective etch in a

Gate Layer	InP	0.2 μm	$P = 1\text{E}18$
Channel	InGaAs	0.3 μm	$N = 1\text{E}17$
Buffer	InP	1.5 μm	$P = 5\text{E}16$
Buffer	InP	0.5 μm	$P \sim 1\text{E}19$
InP S.I. Substrate	InP-TCG Buffer 3 μm $P \sim 1\text{E}19$		InP-TCG Buffer 3 μm $P \sim 1\text{E}19$
	GaAs S.I. Substrate		GaAs 1 μm
			Silicon Substrate

91430

FIGURE 10-1. DESIGN OF THE EPITAXIAL LAYERS FOR THE JFET STRUCTURE.

reproducible manner, without the worry of etching through the thin FET InGaAs channel. Because the top P⁺InP gate layer has a much different chemistry than the In_{0.53}Ga_{0.47}As n⁺channel, it should be possible to find a selective etch for the InP that will automatically stop at the In_{0.53}Ga_{0.47}As FET channel. This is a very important feature, since if a timed etch is used with a P⁺InGaAs/N⁺InGaAs homojunction instead of a selective etch utilizing the InGaAs/InP heterojunction, it would be easy (and disastrous) to accidentally etch through the relatively thin In_{0.53}Ga_{0.47}As channel region, since there is nothing to automatically stop the etch at the right point.

The "zero-bias" depletion region between the P⁺ InP buffer and the heavier doped n⁺ In_{0.53}Ga_{0.47}As channel extends mainly into the P⁺ InP and helps to isolate the JFET channel from the conducting TCG-InP layers used in the growths on GaAs and Si substrates.

The doping N_D ($10^{17}/\text{cm}^3$) and thickness "a" (0.3 μm) of the In_{0.53}Ga_{0.47}As JFET channel in Figure 10-1 were selected to obtain good FET performance at a reasonable pinch-off voltage V_P , $qN_D a^2/2$, about 6 volts. The top P⁺InP needs a high doping for a good ohmic contact, as well as to insure that most of the depletion region extends into the N⁺ InGaAs FET channel. This layer should be thick enough so that the gate ohmic contact to the top InP does not alloy through and short out the junction. The bottom P⁺ InP layer should be lightly doped compared to the channel region, so that its uncontrolled depletion region does not extend into the FET channel. The exact thicknesses and dopings of the InP regions, unlike that of the InGaAs channel, are not critical.

10.2.2 PIN Photodiodes

Figure 10-2 shows the structure of the PIN photodiode. The top N^+ InP layer (1.34 eV) acts as a window which allows light above 930 nm to transit through with little absorption, while preventing, through favorable alignment of the energy bands, minority carriers generated in the 0.75 eV $In_{0.53}Ga_{0.47}As$ "intrinsic" region from recombining at the front surface of the wafer. The window allows light from 930 nm to the $In_{0.53}Ga_{0.47}As$ absorption edge of 1650 nm to pass through relatively unimpeded. The exact window thickness is unimportant, except it should be thick enough so that the top CrAu contact, when annealed, does not alloy through this layer and short out the diode. It should be heavily doped in order to make a good ohmic contact.

Cap	InGaAs	0.13 μm	$N = 1E19$
Window	InP	0.75 μm	$N = 1E18$
I Layer	InGaAs	4 μm	$N = 3E15$
Buffer	InP	0.5 μm	$P \sim 1E19$
InP S.I. Substrate	InP-TCG Buffer 3 μm $P \sim 1E19$	InP-TCG Buffer 3 μm $P \sim 1E19$	
	GaAs S.I. Substrate	GaAs 1 μm	
		Silicon Substrate	

91431

FIGURE 10-2. DESIGN OF THE EPITAXIAL LAYERS FOR THE PIN STRUCTURE.

The intrinsic region should be doped as lightly as possible for maximum depletion width. The length of the intrinsic region "i" is a tradeoff between several factors. Concerning quantum efficiency, "i" should be at least several absorption lengths, and yet thin enough for the junction to deplete through, to insure efficient carrier collection. Concerning speed, "i" should be thick to minimize the device capacitance, yet thin enough so that the carrier transit times do not slow the photodiode. Concerning noise, "i" should be thin to minimize the space-charge generation-recombination currents, which is proportional to the depletion region volume.

One absorption length for the $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$ is about $1\text{ }\mu\text{m}$, so $3\text{ }\mu\text{m}$ allows for about 95% of the light to be absorbed. Assuming an undoped "intrinsic" background of $10^{15}/\text{cm}^3$, the zero-bias depletion width should be $0.9\text{ }\mu\text{m}$. At 5 volts of reverse bias, the entire $3\text{ }\mu\text{m}$ intrinsic region should be depleted. The capacitance of the diode at -5 volts reverse bias should be $3.8\text{ nF}/\text{cm}^2$. Assuming a 50 ohm load, the RC time constant for a 1 cm^2 device is 190 ns. The carrier transit time is roughly the saturation velocity over the length of the depleted intrinsic region ($3\text{ }\mu\text{m}$), or about 30 ps. Therefore, the speed of this very large area detector is capacitance limited, and we would like to make the depletion region as large as possible. However, with the current background doping of $10^{15}/\text{cm}^3$, $3\text{ }\mu\text{m}$ is about all that can be depleted at modest reverse bias voltages. Therefore, $3\text{ }\mu\text{m}$ was chosen as a good target thickness for the intrinsic region, along with whatever minimum background doping that could be achieved, which was assumed in the above calculations as $10^{15}/\text{cm}^3$.

10.3 DEVICE PROCESSING

10.3.1 Etch Characterization

In order to make contact to the various buried epilayers of InGaAs and InP in the device structures, it was necessary to find selective etches which would etch InGaAs but not InP, and vice versa. Table 10-1 gives some wet chemical etch rates for some common etchants on InP and InGaAs.

TABLE 10-1. ETCHING OF LATTICE-MATCHED InGaAs AND InP (25°C, NO AGITATION).

ETCH	MATERIAL	RATE ($\mu\text{m}/\text{min}$)	COMMENTS
HCL	N InP	9.5	Smooth; rate linear w/time
	Si InP	10.5	Smooth surface
	P InP	8.9	Rough surface
	N InGaAs	0.04	Smooth surface
1HCL:1DI	Si InP	0.15	Smooth surface
	P InP	0.53	Rough surface; not linear w/time
	N InGaAs	0.00	Smooth; no etching after 5 min.
1HCL:3DI	Si InP	0.00	No etching
$1\text{H}_3\text{PO}_4:1\text{H}_2\text{O}_2:8\text{DI}$	InP	0.00	No etching

Conclusions:

- * HCL etches all InP at $10\text{ }\mu\text{m}/\text{min}$. and slows at InGaAs to $400\text{ \AA}/\text{min}$.
- * 1:1:8 selectively etches InGaAs but not InP. We know it etches InGaAs from previous work at Cornell and Spire.
- * 1DI:1HCL selectively etches InP (doping depend.) but not InGaAs.

The above data in Table 10-1 were taken on bulk InP or a thick InGaAs epilayer. Since selective etching is critical to the program's success, and because we wished to confirm that the target MOCVD epilayer thicknesses were accurate, a second experiment on an actual PIN diode wafer piece from lot 1274 (Figure 10-2) was performed. The selective etches determined from Table 10-1 were used to alternately selectively etch away InGaAs and InP layers. Each etch step was measured by DEKTAK surface profiling to gauge that particular layers thickness. This method of confirming the thicknesses of the MOCVD epilayers is destructive. In addition, before the etching and DEKTAK measurements, the optical reflectance of the PIN layer on InP was measured. This reflectance data was fit using a Spire-developed optical reflectance modeling program known as REFIT (REflectance FITting). This optical method, which is non-destructive and quicker, is preferred when accurate optical data files for the material is available.

Thicknesses of a nominally lattice-matched InGaAs/InP NIP photodiode layer on an InP substrate measured by selective etching/Dektak, and by optical reflectance, are compared to the MOCVD target structure in Table 10-2. Figure 10-3 shows the measured optical reflectance of the PIN structure (heavy dots) and the theoretical fit (solid line).

TABLE 10-2. COMPARISON OF MOCVD TARGET, DEKTAK/ETCH, AND OPTICAL REFLECTANCE. Thickness of InGaAs and InP layers in PIN structure of Figure 10-2.

Target Layer		Selective Etch and Dektak	Optical Reflectance (REFIT)
1300Å	InGaAs	1000Å	930Å
7500Å	InP	3300Å	3700Å
4 µm	InGaAs	3 µm	3.2 µm
5000Å	InP	-	-
S.I.	InP	-	-

Comments:

1. The InGaAs reflectance data used is from Reference 7.
2. The reflectance fit from 800 to 1800 nm between the measured data and the theoretical data was not as good a fit as is common for GaAs-based or Si/SiO₂ structures. The optical data files need improvement. However, the agreement with the etch/dektak data indicates that even with the current data files, the thickness determined by reflectance is accurate to within about 15%.
3. The selective etch used for InGaAs was 1H₃PO₄:1H₂O₂:8DI (0.24 µm/min). It stopped at the InP.

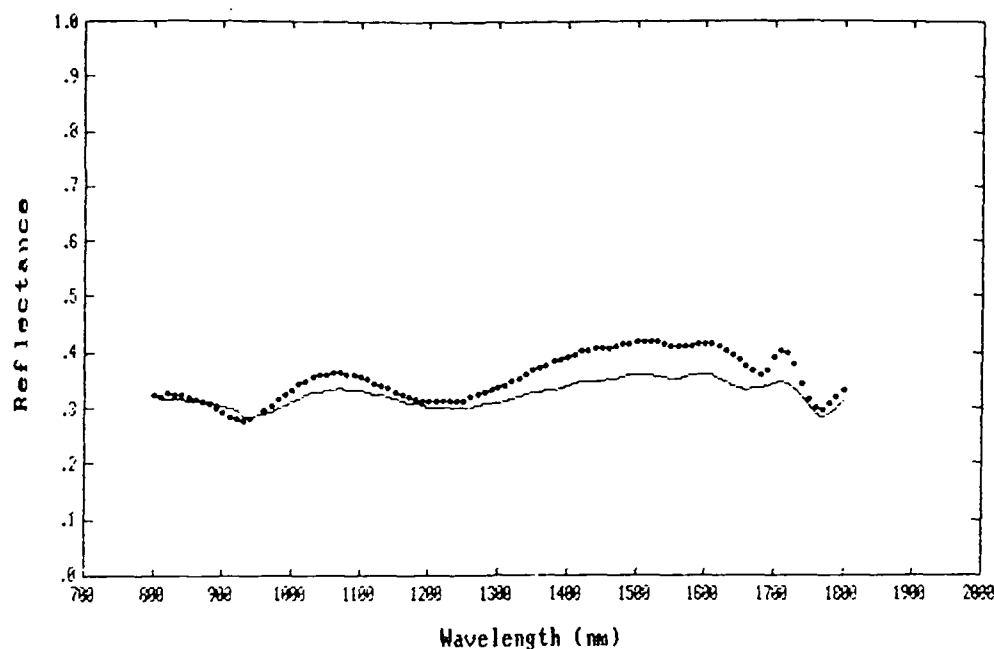


FIGURE 10-3. COMPARISON OF MEASURED OPTICAL REFLECTANCE OF PIN STRUCTURE OF FIGURE 10-2 WITH THEORETICAL REFLECTANCE FIT USING DATA FROM NEE AND GREEN.⁽⁷⁾

4. The selective etch used for InP is 1HCL:1DI (0.4-1 $\mu\text{m}/\text{min}$). It stopped at the InGaAs.
5. A definite visual color change can be seen on the wafer as the InP or InGaAs material is cleared by the etch. This is convenient in determining that all material (either InP or InGaAs) is etched away. This color change is due to the large index of refraction difference between InGaAs and InP. However, for very thin layers, it is more difficult to observe.
6. The InGaAs growth rate seems to be consistently about 30% lower and the InP growth rate also seems to be about 50% less than what was expected for this run (MO5-1274).

10.3.2 Process Sequence for Devices

Below is an abbreviated description of the process sequence used to fabricate both the JFETs and PINs. The devices are quite amenable to monolithic integration, since similar metallization and isolation processes are used for both devices. The final devices fabricated for this program were done in two different epilayer structures, however, to optimize the results.

1. ID wafer backs with MOCVD run #1274-1(PINs) & 1275-1 (FETs)
2. Cleave off a small piece of 1274-1 and 1275-1 and save in labeled envelopes for etch calibration

3. Clean wafer fronts well with de-ionized water (DI)
4. Spin AZ1375 photoresist at 4000RPM on wafer fronts for mesa isolation
5. Bake photoresist 90°C for 30 min.
6. Expose through positive photomask INGAS1-MESA
7. Develop
8. Postbake resist to harden for 90°C 30 min.
9. Wafers 1274 ONLY! Use 1H₃PO₄:1H₂O₂:8DI to etch InGaAs cap- about 25s Is color change seen?
Use 1DI:1HCL to etch N InP - about 20s
Is color change seen?
Use 1:1:8 to etch intrinsic InGaAs - about 6 min.
This etch stops at bottom InP surface (for back PIN contact)
10. Wafers 1275 ONLY! Use 1:1 to etch P+ InP for about 1 min. Should see color change at InGaAs etch stop due to difference in refractive index of InGaAs and InP Use 1:1:8 to etch N InGaAs - about 1 min
Color change?
Use 1:1 to etch P InP - about 4 min
No etch stop, should be no color change.
This etches deep into substrate, isolates the FETs.
11. Photosteps for metal to P+InP (FET gate, PIN back contact) Reverse Image Both 1274 and 1275 Spin AZ1375 4000RPM
12. Bake 90°C for 30 min.
13. Expose through positive photomask INGAS1-GATES
14. Ammonia Bake for image reversal
15. Flood expose to UV source for image reversal
16. Develop
17. Evaporate fronts of all wafers with 2000Å AuZn
18. Liftoff metal covered photoresist in 30 minute acetone soak and spray, leaving metal for top gate FET contacts and top PIN contacts
19. Sinter 1274 wafer only 6 min. 400°C in forming gas (FG) Purge=cool=10 min. in FG

20. Sinter 1275s Only 4 min. 275°C in FG
Purge=cool=10 min. FG
(shorter cooler sinter out to avoid damage to gate junction)
21. Check contacts
22. Photosteps for metal to etched surface (source/drain contacts to InGaAs for FETs, top contact to InP for PINs)
Reverse Image on Both 1274 and 1275
Spin AZ1375 4000RPM
23. Bake 90°C for 30 min.
24. Expose through positive photomask INGAS1-OHMICS
25. Ammonia Bake for image reversal
26. Flood expose to UV for image reversal
27. Develop
28. Wafers 1275 only! Etch away top P+InP in 1:1 to InGaAs etch stop Use Calibration sample first to get etch time to color change, then all 1275 wafers for same time
(This etches InP from source/drain FET areas, revealing InGaAs)
29. Microscope inspection
30. Evaporate all wafers with 400Å Cr, then 3000Å Au
31. Wafers 1274 ONLY! Etch calibration in 1:1:8 to color change
Then all 1274 wafers to color change in about same time
This step etches InGaAs contact cap off window area of PINs.

For this work, one substrate (InP, GaAs and Si) of each layer type (JFET, Figure 10-1 and PIN, Figure 10-2) was available for process development and final devices (six wafers in total). A typical processed wafer piece is shown in Figure 10-4.

10.4 ANALYSIS AND DISCUSSION OF DEVICE RESULTS

10.4.1 InP/InGaAs/InP Junction Field-Effect Transistors (JFETs)

The JFETs fabricated are seen in Figure 10-5. Successful JFETs were made in lattice-matched InGaAs on InP and lattice-mismatched InGaAs-on-GaAs substrates. JFETs on Si operated poorly. We believe this is due to a larger leakage current in the FET gate (P)InP/(N)InGaAs junctions on the Si substrate.

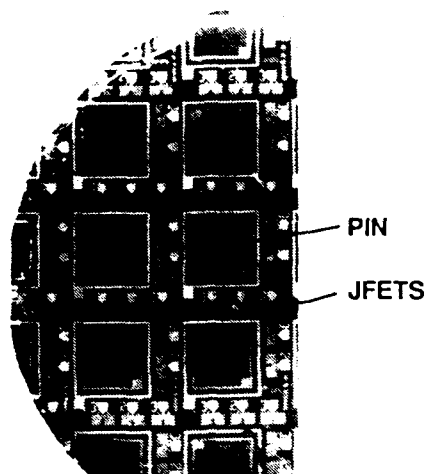
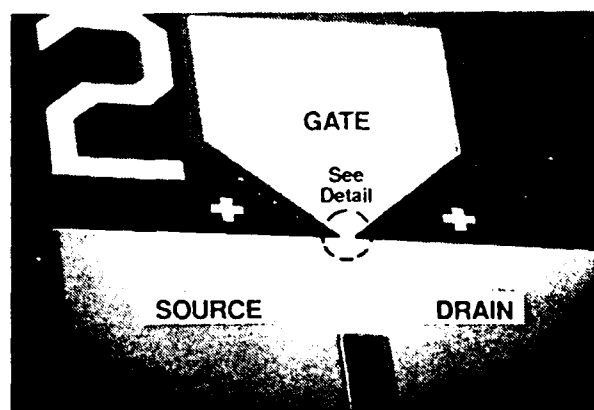
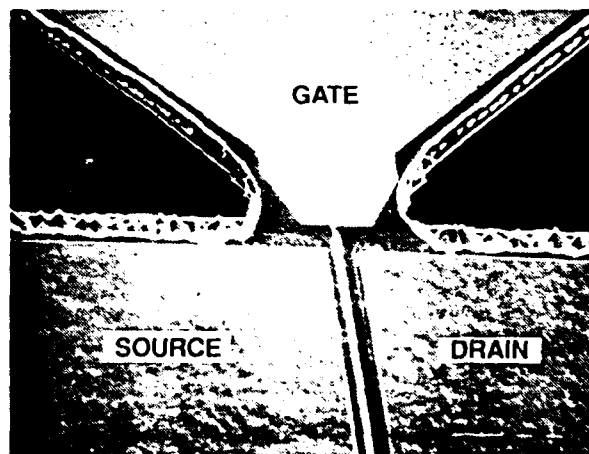


FIGURE 10-4. WAFER (InP substrate) WITH SQUARE PIN PHOTODIODES AND FETs (1:1 SCALE)



a)



b)

FIGURE 10-5. a) SEM PHOTO OF A 500 μm WIDE InGaAs JFET. b) DETAIL OF (a) SHOWING A 2 μm METAL GATE CONTACT (ACTUAL GATE IS LARGER SEE FIGURE 10-8), AND JFET DRAIN AND SOURCE REGIONS. Roughness on mesa sides due to differing etch rates of HCL and phosphoric-based selective etches for the InP and InGaAs layers, respectively.

Figure 10-6 shows IV curves of relatively large area $P^+InP/N^+InGaAs$ heterojunction diodes on the three material substrates. Because of the simple diode structure used, all three exhibit large resistance in the forward direction (i.e. the IV is more linear than exponential). Even if this forward resistance existed in the FET gate diodes themselves, it would not be troublesome since the JFET gates are operated in reverse bias, not forward bias. All three diodes on the three different substrate types are extremely leaky. Test diodes results are summarized in Table 10-3.

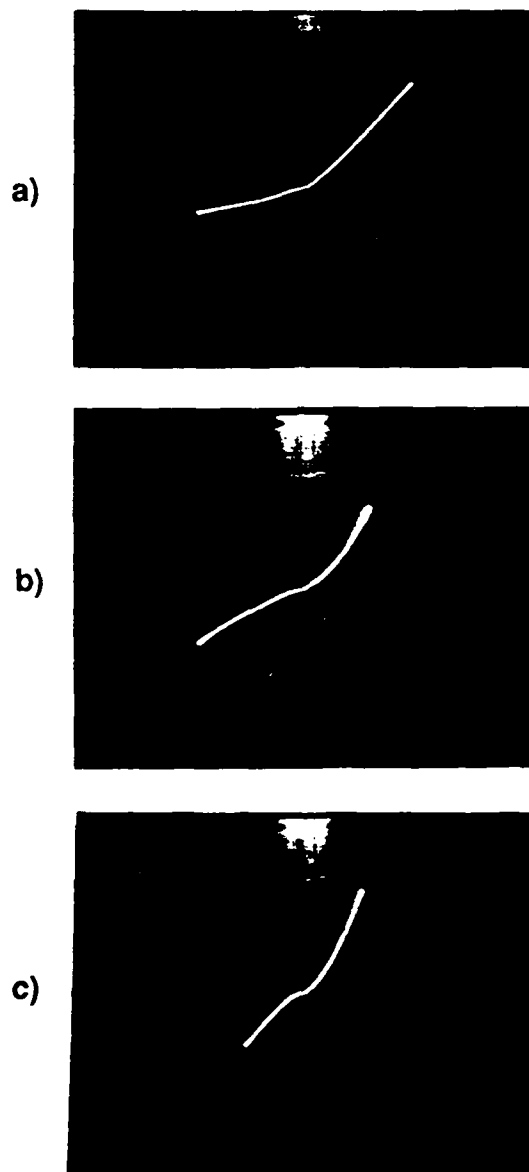


FIGURE 10-6. IV CHARACTERISTICS OF $P^+InP/N^+InGaAs$ GATE HETEROJUNCTION DIODES ON a) InP, b) GaAs, and c) Si SUBSTRATES. Area of these test diodes is 0.095 cm^2 , over 3000X greater than the actual gate area of 0.00003 cm^2 .

TABLE 10-3. IV DATA OF P⁺InP/N⁺InGaAs HETEROJUNCTIONS ON InP, GaAs AND Si.

Test Diode Area 1 mm ²	Currents at a reverse bias of 4V		
Substrate Type	Current (mA)	Current Density (A/cm ²)	Forward Resisistance (ohms)
InP	10	1×10^{-1}	111
GaAs	20	2×10^{-1}	40
Si	40	4×10^{-1}	40

The JFET gates should have similar performance to Table 10-3. The gates need to withstand appreciable reverse bias, and are very sensitive to any material defects. The leakage observed may be due to dislocations threading through the FET gate p-n junction if the InGaAs/InP material is slightly lattice-mismatched, or perhaps due to a high interface recombination velocity at the InP/InGaAs heterojunction interface used as the FET gate pn junction. If additional time and funds were available, we would have liked to characterize simple InGaAs homojunctions to see if the junction leakage currents would have improved. If there was improvement with InGaAs homojunctions, InGaAs/InP heterojunction interface states would be the chief suspect for the leaky performance. If no improvement was seen, lattice mismatch would be the probable cause. Again, heterojunction gates were used since a natural etch stop exists at the InGaAs/InP interface which is important for reproducible device processing.

In the JFET, a large current flows between the source and drain of Figure 10-5. A very small voltage "wiggle" applied to the gate of the JFET pushes electrons away from the region just under the gate p-n junction, shrinking the effective FET channel width there, thereby "wiggling" the larger source-to-drain current. This feature, by which a large output drain current is controlled by a small input gate voltage, is what makes the JFET useful as an amplifier. The magnitude of the output drain current change with respect to the input gate voltage change is the transconductance (g_m), and is the FET's most important figure-of-merit. The g_m is calculated directly from the set of JFET IV curves in Figure 10-7. The results are summarized in Table 10-4.

The best JFETS performed equally well on GaAs and InP substrates (InP was slightly better) and have a g_m of 80 mS/mm at 300 K. This performance is excellent for such a large (6 μ m) gate length. The JFETs on Si showed no observable transconductance. Apparently, the problem is not a shunt current path through the buffer underneath the FET channel, as is often a problem with MESFETs, since the current level seems to be about the same or lower than in the JFETs on InP and GaAs substrates, and seems to be due to an inability of the JFET gate to modulate the current flows. Although the IV data of test diodes show that the InGaAs/InP heterojunctions on Si are the worse of the group, it is not, say an order of magnitude more leaky than the other types. In summary, the degradation mechanism of the JFETs on Si is unknown. Too little time was left in the program when the device work started to make much headway in this puzzle.

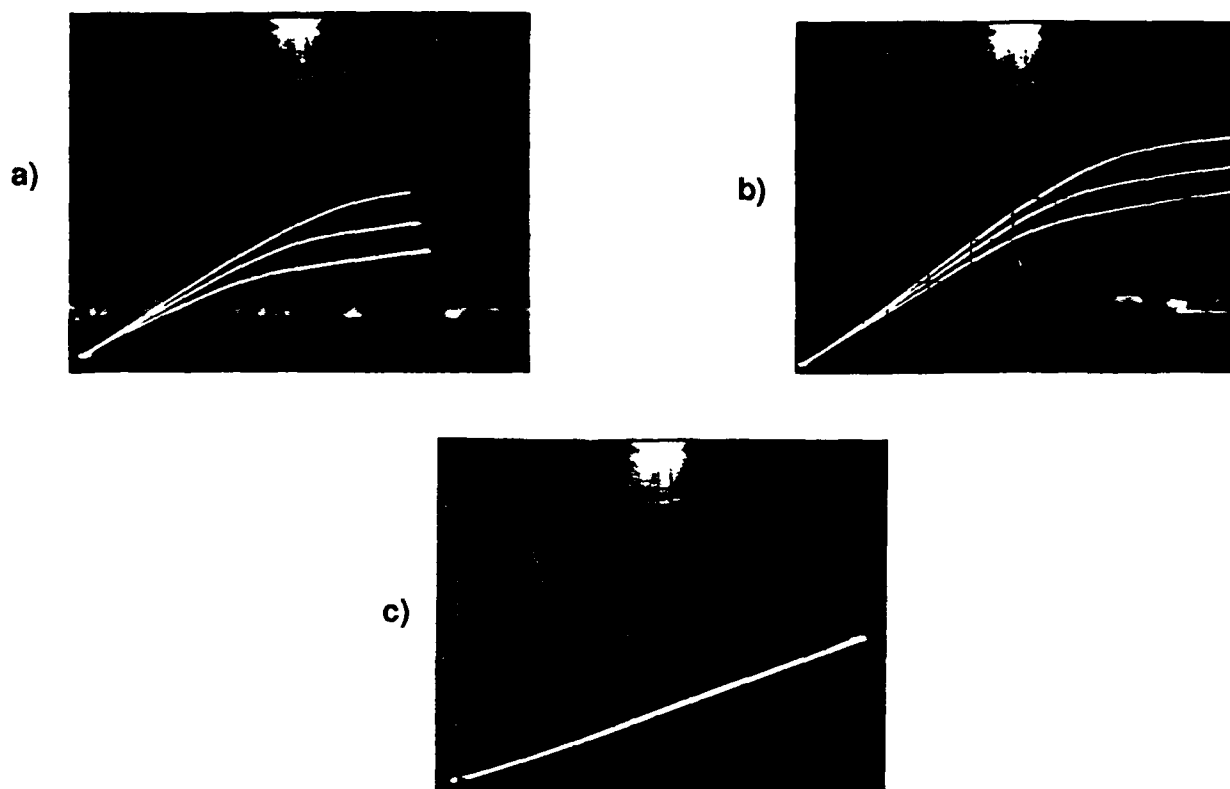


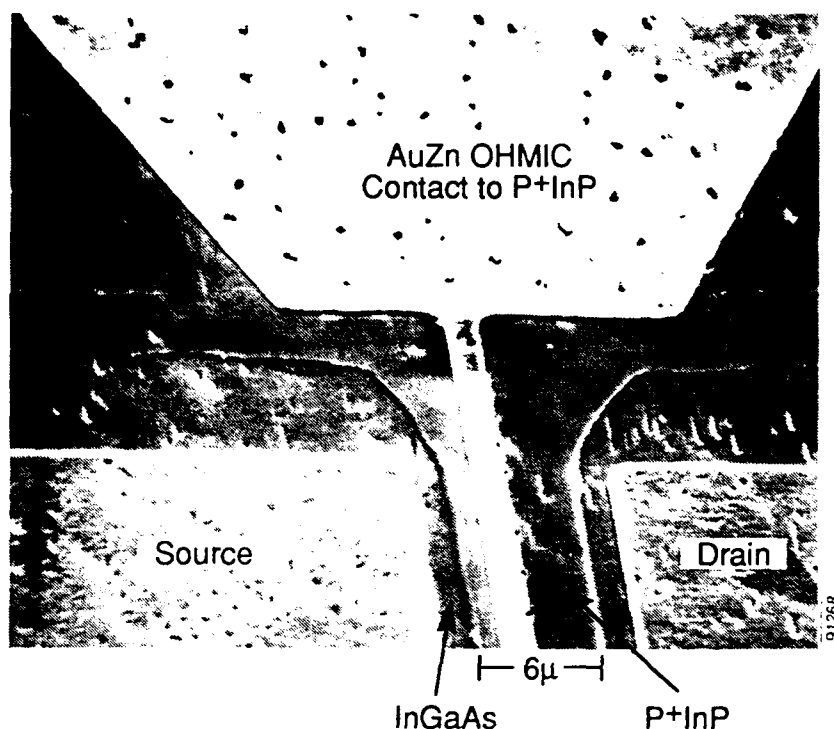
FIGURE 10-7. I-V CURVES OF InGaAs JFETs WITH A (P)InP/(N)InGaAs HETEROJUNCTION GATE AND AN (N)InGaAs CHANNEL ON AN (a) InP, (b) GaAs, AND c) Si SUBSTRATE. Vertical:50mA/div Horizontal:0.5V/div Gate step:1V/step.

TABLE 10-4. MEASURED InGaAs JFET TRANSCONDUCTANCE AND SOURCE-DRAIN RESISTANCE.

Substrate Type	Transconductance g_m (mS/mm)	Source-Drain Resistance r_{ds} (ohms-mm)
InP	80	67
GaAs	80	50
Si	0	-

The effective gate length of these JFETs is about $6\text{ }\mu\text{m}$ as described in Figure 10-8, and not the $2\text{ }\mu\text{m}$ length of the gate metal. It may be informative to compare these devices with the more common GaAs MESFETs. In a MESFET, the gate metal forms a junction directly with the GaAs, and the effective gate length is the same as the metal. The best GaAs MESFETs with gate lengths of $1\text{ }\mu\text{m}$ have a g_m of about 150 mS/mm , and MESFETs with $0.2\text{ }\mu\text{m}$ gates have been reported to have g_m 's over 500 mS/mm . The g_m increases in proportion as the gate length decreases. Schottky gate metals such as Au, Ag, Al, Ti, W, etc. do not make good rectifying junctions with InGaAs, so that a p-n junction must be used, which is normally larger than the

a)



b)

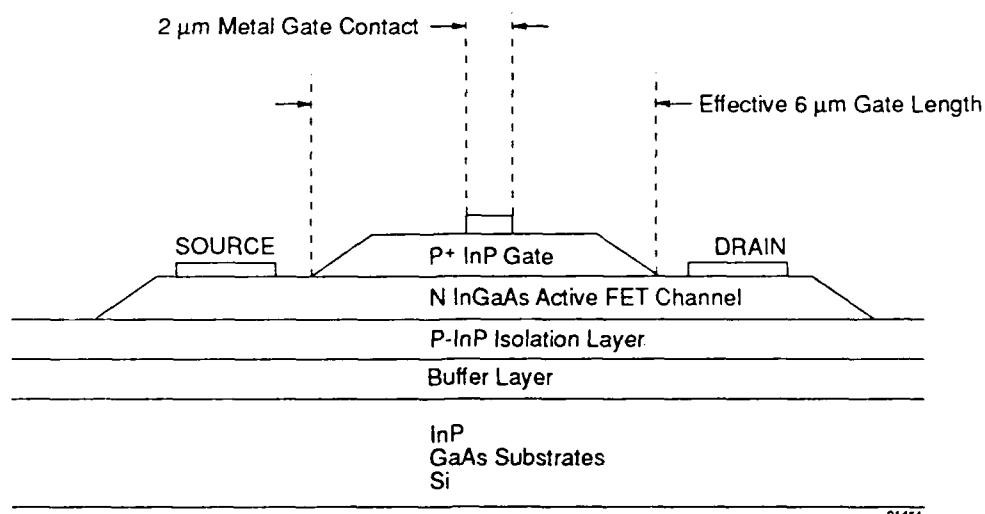


FIGURE 10-8.

a) SEM PHOTO OF AN InGaAs/InP JFET ON A Si SUBSTRATE SHOWING A 2 μm METAL GATE OHMIC CONTACT TO A 6 μm P⁺InP THIN EPILAYER. The p-n heterojunction between the P⁺InP and the underlying N-InGaAs FET channel layer is the gate junction with an effective length of about 6 μm. Some "pit" defects in this InGaAs/InP material on Si can be seen; they possibly contribute to the leaky p-n InP/InGaAs heterojunction IVs of Figure 10-6 and Table 10-3. b) Cross-section of JFET shows a 6 μm effective gate length, defined by the p-n InP/InGaAs heterojunction under the gate.

gate metal. Our JFETs are roughly half the MESFET g_m value even though handicapped with a 6-times larger gate. If some time was spent developing a process to make shorter gate p-n junction lengths, possibly one micron p-n junction lengths could be achieved. If the scaling laws hold true, shrinking the gate length from 6 μm to 1 μm would then mean a six-fold increase in g_m to about 480mS/mm, even if no other improvements were made to these JFETs.

In summary, the JFETs on GaAs and InP substrates are roughly equivalent in performance, both have very good transconductance, and both have the same problem. The FET channel cannot be pinched-off under the gate completely due to the leaky InGaAs/InP heterojunction gate. That is, the source-to-drain current cannot be turned completely off. Therefore, they are suitable for some analog/linear applications, but not digital and logic circuits. This can be improved with further work. The failure of the JFETs on Si is puzzling, since there is apparently no shunt path responsible for the low transconductance, and likewise the test diode IV results, while showing that the junctions on Si substrates were 2-4 times leakier, were similar to the other diodes on InP and GaAs which worked.

10.4.2 InP/InGaAs/InP Heterojunction PIN Photodiodes

The PIN photodiodes were processed without any troubles up to step 31 in the process description given previously. At this point the PIN diodes were essentially finished. Step 31 was the last process, in which the InGaAs contact cap was etched off the InP window. The InGaAs is a small bandgap material, and it is easier to make better ohmic contacts to InGaAs than the higher bandgap InP. However, if left on the InP window, the InGaAs also absorbs light without any chance that the photogenerated carriers in the InGaAs cap would be collected.

Therefore, the normal procedure for these structures is that after the top contact metal is deposited and sintered on the InGaAs, the excess InGaAs not immediately underneath the contacts areas is etched away, revealing the InP window layer. The InP has a bigger bandgap (1.34 eV) than the InGaAs intrinsic region (0.75 eV) deeper in the layers. The InP therefore allows the photons of interest (above 925 nm in wavelength) to pass through unimpeded and be absorbed in the InGaAs intrinsic region, while preventing the carriers photogenerated in the InGaAs intrinsic region from recombining at the front surface through a built-in electric field gradient which pushes them back to the collecting junction.

However, a problem during the cap etch destroyed the metallization on all the photodiode wafers. Because most of the device work was done at the very end of the program, it was not possible to reprocess the wafers. However, some data was measured before the cap etch step 31. This data is presented below. The photocurrents are all decreased somewhat due to the presence of the InGaAs cap on the photoactive area.

Figure 10-9 shows illuminated and unilluminated IVs for PIN diodes on InP, GaAs, and Si substrates. The results are summarized in Table 10-5. The leakage currents for these PIN diodes are roughly equal to the leakage currents for the FET gate diodes of Table 10-3, if the difference in bias voltage that the two measurements were performed at is taken into account. The diodes of Tables 10-3 and 10-5 were grown in two different MOCVD runs, and yet exhibit similar leakage currents. This seems to support the theory that the leakage is due to an inherently high recombination velocity at the InGaAs/InP interface under our current MOCVD growth conditions.

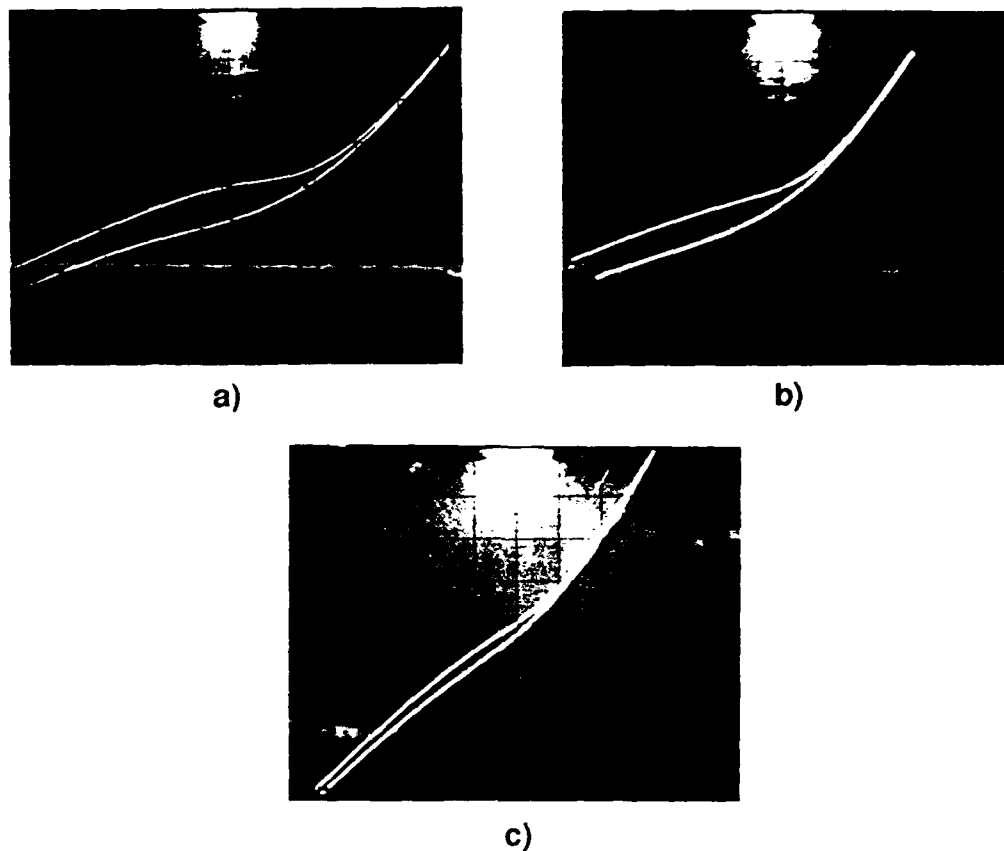


FIGURE 10-9. DARK (TOP) AND ILLUMINATED (BOTTOM) IVs OF InP/InGaAs/InP PIN DIODES ON a) InP, b) GaAs, AND c) Si SUBSTRATES, WITH InGaAs CONTACT CAP LEFT ON. Light from microscope illuminator is uncalibrated but same in all three cases. Same IV scales on all three IVs - Horizontal: 0.1V/div Vertical: 1mA/div Center: 0V, 0mA

TABLE 10-5. IV DATA ON InP/InGaAs/InP PINs ON InP, GaAs AND Si SUBSTRATES.

Substrate Type	Leakage current at 0.5V reverse bias InGaAs cap over photoactive area.		
	Leakage Current Density at 0.5V (A/cm ²)	Photocurrent at 0V (mA)	Forward Resistance (ohms)
InP	1.8×10^{-3}	0.80	100
GaAs	1.6×10^{-3}	0.20	71
Si	4.2×10^{-3}	0.15	63

Since the illumination profiles were the same for the PINs on all three different substrates, and since the quantum efficiency is to first order unaffected by leakage current, it may be inferred that the PIN on the InP substrate is about 4 times more efficient than the GaAs and Si substrates at minority-carrier collection. It may not be correct to assume that the minority-carrier lifetime is directly proportional to the photocurrent and is therefore 4 times greater in the material grown on InP, however. This is especially true in a PIN structure, where most of the carriers should be generated in a depletion region instead of having to diffuse (several diffusion lengths) to the depletion region from bulk regions of the device. However, it can probably be safely said that the minority-carrier lifetime is greater in the InGaAs/InP material on InP than on GaAs or Si.

The internal quantum efficiency of the PIN $P^+InP/nInGaAs/N^+InP$ photodiode on an InP substrate (Figure 10-10) was the only one taken before the disastrous cap etch. The good news is that the quantum efficiency is quite respectable, considering the thin InGaAs contact cap left on the photoactive area. The absorption edge for lattice-matched InGaAs should be at 1.65 microns. The quantum efficiency data shows a slight response beyond this, perhaps an indication that the material is not exactly lattice matched. Although we have been referring to "PIN" diodes throughout this report, since this is the convention, as can be seen in Figure 10-2, the structures are actually "NIP" diodes. The intrinsic region is undoped InGaAs, which typically turns out to be n-type with a doping of about $10^{15}/cm^3$. The actual $P^+InP/N^+InGaAs$ surface is then buried towards the back of the structure. The depletion region is about $1\ \mu m$ at zero bias given the "undoped" background (the quantum efficiency was measured at zero bias). The peak in the quantum efficiency at 1600 nm is probable due to the fact these longer wavelength photons are generated towards the back of the photodiode in or very near the depletion region, so collection is extremely efficient. The wavelengths closer to 1000 nm are generated more towards the front of the intrinsic InGaAs region. They have to diffuse through about $2\ \mu m$ of InGaAs to be collected at the back junction. The quantum efficiency is lower either because the diffusion length for these carriers in the InGaAs is less than $2\ \mu m$, or, as may be indicated by the high leakage currents in the diodes, the front InGaAs/InP heterojunctions of the PIN may be acting as a recombination site instead of a minority carrier mirror. The quantum efficiency drops again below 900 nm since this is where the InP window becomes absorbing.

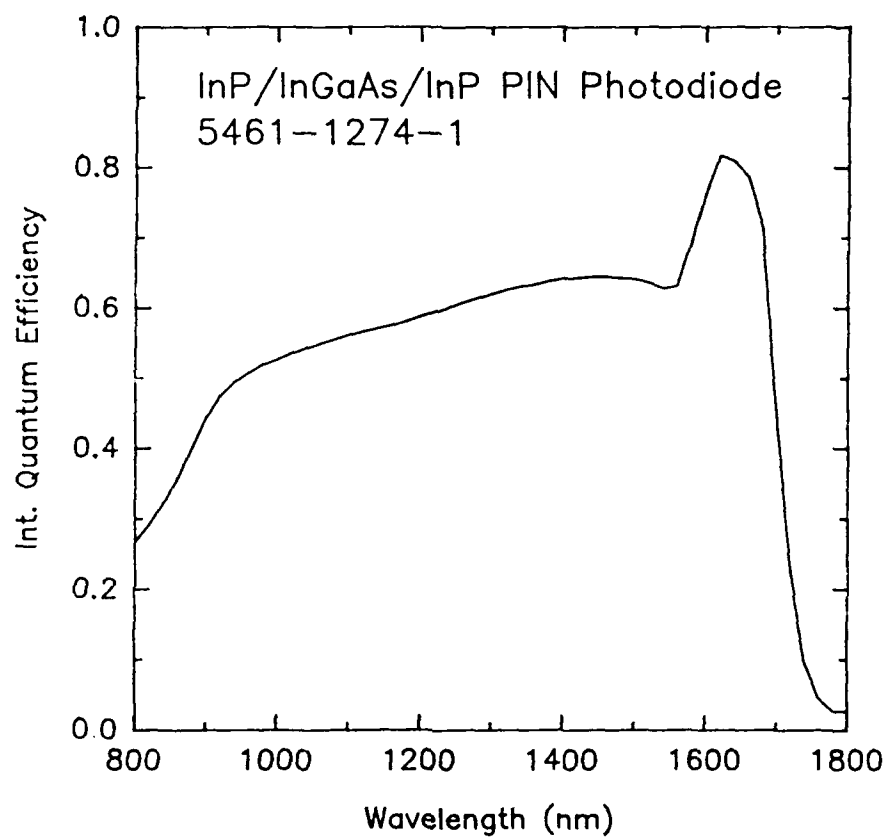


FIGURE 10-10. INTERNAL QUANTUM EFFICIENCY CURVE OF AN InP/InGaAs/InP PIN PHOTODIODE, WITH InGaAs CONTACT CAP LEFT ON. For $\text{In}_{0.53}\text{Ga}_{0.47}\text{As}$, cutoff wavelength is $1.65\text{ }\mu\text{m}$.

SECTION 11

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SECTION 12
ADVANCED DEGREES EARNED

Mr. V.P. Mazzi, a student in the laboratory of Dr. N.M. Haegel, earned his Master of Science in June, 1989, from the Material Science Department, University of California at Los Angeles. His thesis title is "Photoluminescence of InP Heterostructures". His thesis work was supported in part under this contract.

SECTION 13

PUBLICATIONS RESULTING FROM THIS RESEARCH

13.1 INVITED TALKS

"Growth of InP-GaAs-Si Structures by MOCVD," at Seminar Series, Boston University College of Engineering, October, 1989.

13.2 PUBLISHED PAPERS

"Improvement of InP-GaAs-Si Quality by Thermal-Cycle Growth," S.M. Vernon, C.J. Keavney, E.D. Gagnon, N.H. Karam, M.M. Al-Jassim, N.M. Haegel, V.P. Mazzi, and C.R. Wie, Mater. Res. Soc. Symp. Proc. 198, 163 (1990).

"Growth and Characterization of InP/GaAs on SOI by MOCVD," N.H. Karam, V.E. Haven, S.M. Vernon, F. Namavar, J. Randani, N. El-Masry, and N.M. Haegel, Mater. Res. Soc. Symp. Proc. 198, 247 (1990).

"InP on GaAs/Si Substrates for Monolithic Integration of Advanced High-Speed Optoelectronics," S.M. Vernon, Proc. of NOSC/NRL Workshop on Inp Microwave/Millimeter Wave Technology, La Jolla, CA, January, 1989.

"Photoluminescence Characterization of InP on GaAs, Si, and GaAs/Si Substrates," V.P. Mazzi, N.M. Haegel, S.M. Vernon, and V.E. Haven, Mater. Res. Soc. Sump. Proc. 144, 267 (1988).

"Growth and Characterization of MOCVD-grown InP on Si," S.M. Vernon, V.E. Haven, C.R. Abernathy, S.J. Pearton, A.T. Macrander, N.M. Haegel, V.P. Mazzi, K.T. Short, and M.M. Al-Jassim, Inst. Phys. Conf. Ser. 96, 211 (1989).

"Characterization of InP-GaAs-Si Structures Grown by Atmospheric Pressure Metalorganic Chemical Vapor Deposition," S.J. Pearton, K.T. Short, A.T. Macrander, C.R. Abernathy, V.P. Mazzi, N.M. Haegel, M.M. Al-Jassim, S.M. Vernon, and V.E. Haven, J. Appl. Phys. 65, 1083 (1989).

APPENDIX A

"Electrical Studies of InP and GaAs Epitaxial Layers," Report from subcontractor Prof. W.A. Anderson, Center For Electronic and Electro-optic Materials, State University of New York, Buffalo, NY 14260.



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May 23, 1989

Mr. Stan Vernon
Spire Corp.
Patriots Park
Bedford, MA 01730

Dear Stan:

I enclose an added note to be attached to the report previously transmitted. This basically compares our data with that of a reference involving epitaxially grown GaAs/Si.

Sincerely,

A handwritten signature in cursive script that reads "Wayne".

Wayne A. Anderson
Professor & Director

Enc.
WAA/mh

I - Previous Studies of GaAs/Si.

The growth procedure for obtaining high-quality GaAs on an Si substrate has recently been investigated aiming at new devices such as high-efficiency, low-cost solar cells, optoelectronic IC's and GaAs IC's on large-area Si substrates. Although much work has been done, the performance of the GaAs on Si devices is still inferior to those on GaAs substrates, probably due to the difference in the lattice constant and/or the thermal expansion coefficient between Si and GaAs producing defects, dislocations, deep levels and stress. So far, only some (Soga's work is the only one to be found)^[1] work has been done on the deep levels in GaAs on Si in spite of its important role in device performance.

The nature of the deep level in GaAs on Si must be different from that on a GaAs substrate owing to the auto-doped Si into the epi-layer, stress in the layer and induced defects. Soga's sample was MOCVD grown undoped n-GaAs on (100) 2° off Si with an intermediate superlattice (SL) layer structure which consisted of the first lattice-matched 50 μm thick GaP layer on Si and GaP/GaAs_{0.5}P_{0.5} SLS (10 layers) and GaAs_{0.5}P_{0.5}/GaAs SLS (10 layers). In DLTS measurements, the rate windows were changed from 51 to 512 s^{-1} , the reverse-bias voltage was 1.0V and the bias pulse height and width were 1.0V and about 5 μ - 1 ms, respectively.

Figure 1 shows a typical DLTS spectrum for GaAs on Si as well as GaAs on GaAs. The result is convincing in that only one trap ($E_A = 0.73$ eV) was observed in the GaAs/GaAs sample while two traps (0.73 eV and 0.44 eV) were observed for GaAs on Si samples. The details are listed in Table 1. The 0.73 eV trap is thought to be EL2, very popular in MOCVD-grown GaAs.

The nature of the 0.44-eV trap was investigated in greater detail. Fig. 2 shows the carrier and trap concentration as a function of the GaAs thickness. The carrier concentration decreased and saturated at 2 μm (about $2.0 \times 10^{16} \text{cm}^{-3}$).

On the other hand, both trap concentrations decreased with increasing GaAs thickness. Fig. 3 shows the capture cross section of the 0.44-eV trap being decreased with increasing thickness while that of the 0.73-eV trap remained almost unchanged.

These observations suggest that the 0.44-eV level could be attributed to a Si-defects complex. The decrease in the trap concentration with increasing GaAs thickness must be due to the reduced Si-auto-doped in GaAs. The 0.73-eV level must be related to an inherent defect, probably EL2, in the MOCVD grown GaAs. In addition, the calculated DLTS spectra using experimentally obtained deep level energy and capture cross section are also shown in Fig. 1 by broken lines. The spectra of EL2 coincide with the calculated curve for both samples, but the experimental spectrum is broader than the calculated 0.44 eV level. This indicates that such a trap contains several levels centered at 0.44 eV.

II. Our Experiment -- GaAs Homojunction on GaAs and Si

In our lab, a number of MOCVD-grown (at Spire Corp.) GaAs multilayer diodes have been studied using DLTS and other measurements. The substrates are either GaAs or Si, similar to the Japanese group. There is no SL involved. The most distinguishing point might be that a homogeneous GaAs junction ($1\text{ }\mu\text{m}$ p⁺-type emitter, $N_D=2\times 10^{18}\text{cm}^{-3}$ / $3\text{ }\mu\text{m}$ n-type base, $N_A = 2\times 10^{17}\text{cm}^{-3}$) plays the key role and that DLTS probes the base region where the material properties should be different between GaAs and Si substrates.

Probably because the high doping concentration ($2\times 10^{17}\text{cm}^{-3}$) limited the detectable trap density to be about the order of 10^{14}cm^{-3} (10^{-3} of the doping concentration) our DLTS peaks were not quite sharp and were disturbed by background noise so that the deduced deep level parameters were of poor accuracy. However, the same kind of phenomena as the Japanese group has been found. For GaAs on GaAs, only one deep level has observable peaks when high rate windows were

used. The ionization energy and trap density are 0.65-0.71 eV and $1.5-2.0 \times 10^{14} \text{ cm}^{-3}$, respectively. This level may be ascribed to EL2. For GaAs on Si, this level was still noticeable with a little higher density, and in addition a continuous distribution of trap levels appeared with $2-5 \times 10^{14} \text{ cm}^{-3}$ density. The best estimation of the ionization energy where the levels centered is 0.415 eV, comparable to what the Japanese group obtained (0.44 eV). Misfit dislocations or some other Si-related defects are thought to be responsible for this.

III. Reference

- [1] T. Soga, S. Sakai, M. Umeno and S. Hattori. "Deep Levels in GaAs Grown Using Superlattice Intermediate Layers on Si Substrates by MOCVD". Jpn. J.A.P. Part 1. Vol. 25 No. 10. 1510-1513 (1986)

TABLE 1

Summary of deep levels observed in 2 μm -thick GaAs grown on GaAs and (100)2° off Si.

Sample	E_n (eV)	N_t (cm^{-3})	σ_n (cm^2)
GaAs/GaAs	0.73	8.0×10^{13}	1.7×10^{-14}
GaAs/Si	0.73	3.4×10^{14}	3.1×10^{-14}
	0.44	2.7×10^{14}	6.1×10^{-14}

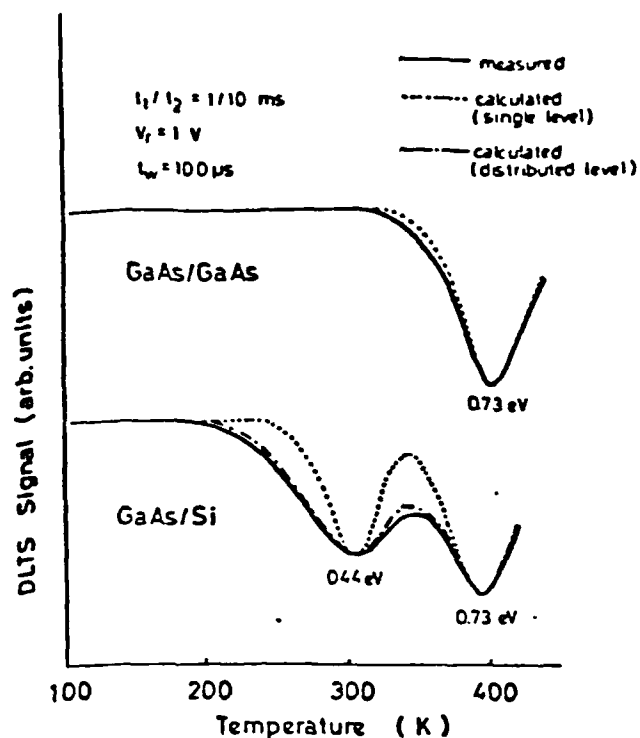


FIGURE 1. Typical DLTS spectra for GaAs layers grown on GaAs and (100)2° off Si. The thickness of GaAs is 2 μm .

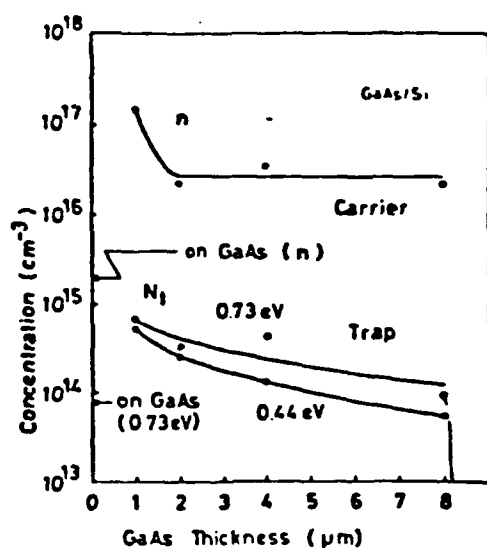


FIGURE 2. Carrier concentration and trap concentration in GaAs on Si as a function of the GaAs thickness.

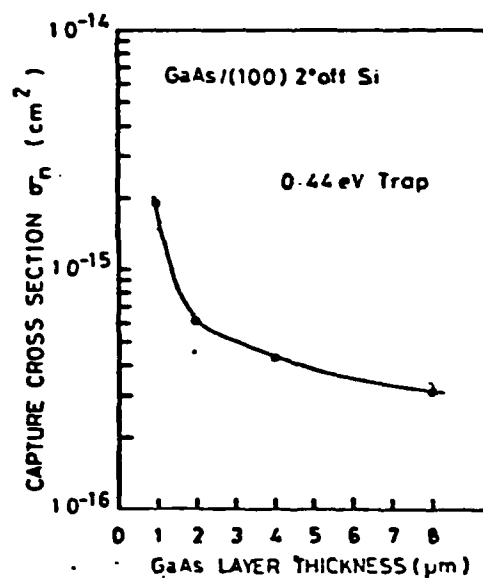


FIGURE 3. Capture cross section of a 0.44 eV trap as a function of the GaAs thickness.



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Progress Report

**"Electrical Studies of
InP and GaAs Epitaxial Layers"**

**Submitted to: Mr. Stan Vernon
Spire Corp.
Patriots Park
Bedford, MA 01730**

May 17, 1989

Wayne Hollister

REPORT FOR SPIRE PROJECT

PART A: EPITAXIAL GaAs ON GaAs OR GaAs ON Si

1. Sample Processing

The wafers were cut into $3 \times 3 \text{ mm}^2$ pieces and then cleaned with TCE, acetone, methanol, DI water rinse and N_2 dry. In and Ni were deposited on the front surface and 1 mm circular dots patterned by a Mo mask. The back contact was Au:Ge alloy covered by Ni. Annealing was carried out at 400°C for 7 min in forming gas. After the ohmic contacts were protected by photoresist, the samples were etched by $\text{H}_2\text{SO}_4:\text{H}_2\text{O}_2:\text{H}_2\text{O}$ (8:1:1).

2. C-V (C-V-T, C-T) Measurements

Fig. 1 and Fig. 2 are C-V-T curves for GaAs/GaAs and GaAs/Si samples, respectively. All the curves are linear hence the p-n junctions are of good quality and the doping concentrations uniform. Fig. 3 and Fig. 4 show that the doping concentration is $2 \times 10^{17} \text{ cm}^{-3}$ for GaAs/GaAs and $1.6 \times 10^{17} \text{ cm}^{-3}$ for GaAs/Si, in good agreement with the given value. Also, one can see from Fig. 1 and Fig. 2 that when temperature decreases to a low range (below 150°K), the temperature dependence of GaAs/GaAs and GaAs/Si become drastically different. The C-T curves in Fig. 5 and Fig. 6 more clearly show this phenomenon. This might be explained that the GaAs/Si structure contains more defects so that a defect-induced band-tail might reduce the effective bandgap and carrier "freeze-out" would happen at an even lower temperature.

3. Photoreflectance Spectroscopy Measurement

The photoreflectance spectrum of GaAs/GaAs and GaAs/Si are shown in Fig. 7 and Fig. 8. The results of 1.4 eV for the bandgap of GaAs/GaAs but 1.3 eV for GaAs/Si structure seem to be in favor of the argument mentioned above. E_g is inferred from the point of oscillation and can be more accurately determined if a standard is utilized.

4. DLTS Measurements

Fig. 9-12 are DLTS spectra for GaAs/GaAs and GaAs/Si. The high doping

concentration (2×10^{17}) limited the detectable trap density to the order of 10^{14} cm^{-3} (10^{-3} of the doping concentration) and the trap density happened to be in the same order so that the DLTS peaks were not as sharp as usual but contained noise. For GaAs on GaAs (Fig. 10) only one deep level had noticeable peaks with the high rate windows. The activation energy and trap density are deduced to be 0.65-0.71 eV and $1.5\text{-}2.0 \times 10^{14} \text{ cm}^{-3}$, respectively. This level may be ascribed as EL2 which is very common in MOCVD-grown GaAs.

For GaAs on Si, this level was still observable, indicating that this level is an inherent defect related to the GaAs epitaxy layer. In addition, a continuous distribution of trap levels appeared. It is very difficult to analyze these traps since they cross over a large temperature range and are different from sample to sample. An estimation for the peaks in Fig. 12 gave 0.42 eV as the activation energy. Misfit dislocations or some other Si-related defects are thought to be responsible for these traps. The random arrangement of these defects cause the different traps in different samples.

5. I-V-T Measurements and Data Analysis

I-V-T data revealed the saturation current density of GaAs/Si to be four orders in amplitude higher than for GaAs/GaAs. Also, the saturation current density of GaAs/Si was less temperature dependent than for GaAs/GaAs. Typical data are shown in Fig. 13 and Fig. 14. Similar temperature dependence was also found for n-T relations, seen in Fig. 15, where n=diode factor.

$\ln J_0$ vs $1000/T$ curves shown in Fig. 16 for GaAs/GaAs and in Fig. 17 for GaAs/Si seem to agree with the DLTS measurements in that at high temperature range the activation energy given by the slope is about 0.71 eV for most of the samples. At lower temperatures, the curves of GaAs/Si samples are much flatter than for GaAs/GaAs, indicating the current mechanisms to be more trap related.

FIGURE CAPTIONS

- Figure 1 C-V-T for GaAs/GaAs
- Figure 2 C-V-T for GaAs/Si
- Figure 3 Doping (N) vs space charge layer width (W) for GaAs/GaAs
- Figure 4 N-W for GaAs/Si
- Figure 5 C-T for GaAs/GaAs
- Figure 6 C-T for GaAs/Si
- Figure 7 Photoreflectance (PR) for GaAs/GaAs
- Figure 8 PR for GaAs/Si
- Figure 9 DLTS for GaAs/GaAs
- Figure 10 DLTS for GaAs/Si #01
- Figure 11 DLTS for GaAs/Si #02
- Figure 12 DLTS for GaAs/Si #03
- Figure 13 IVT for GaAs/GaAs
- Figure 14 IVT for GaAs/Si
- Figure 15 Ideality factor (n) for GaAs/GaAs and GaAs/Si
- Figure 16 Reverse saturation current density ($\ln J_0$ vs $1000/T$) for GaAs/GaAs.
- Figure 17 $\ln(J_0)$ vs $1000/T$ for GaAs/Si.

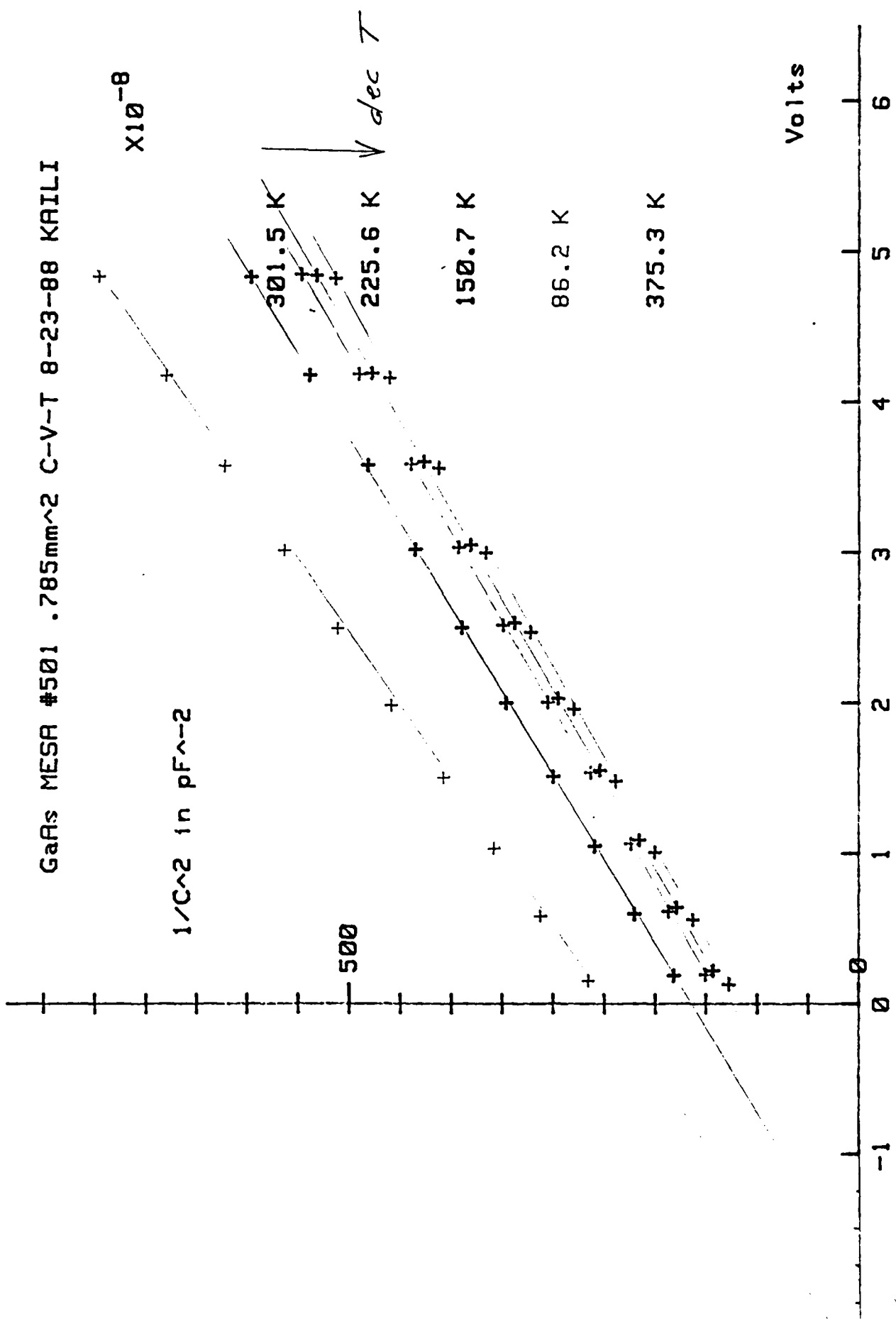


Figure 1 C-V-T for GaAs/GaAs

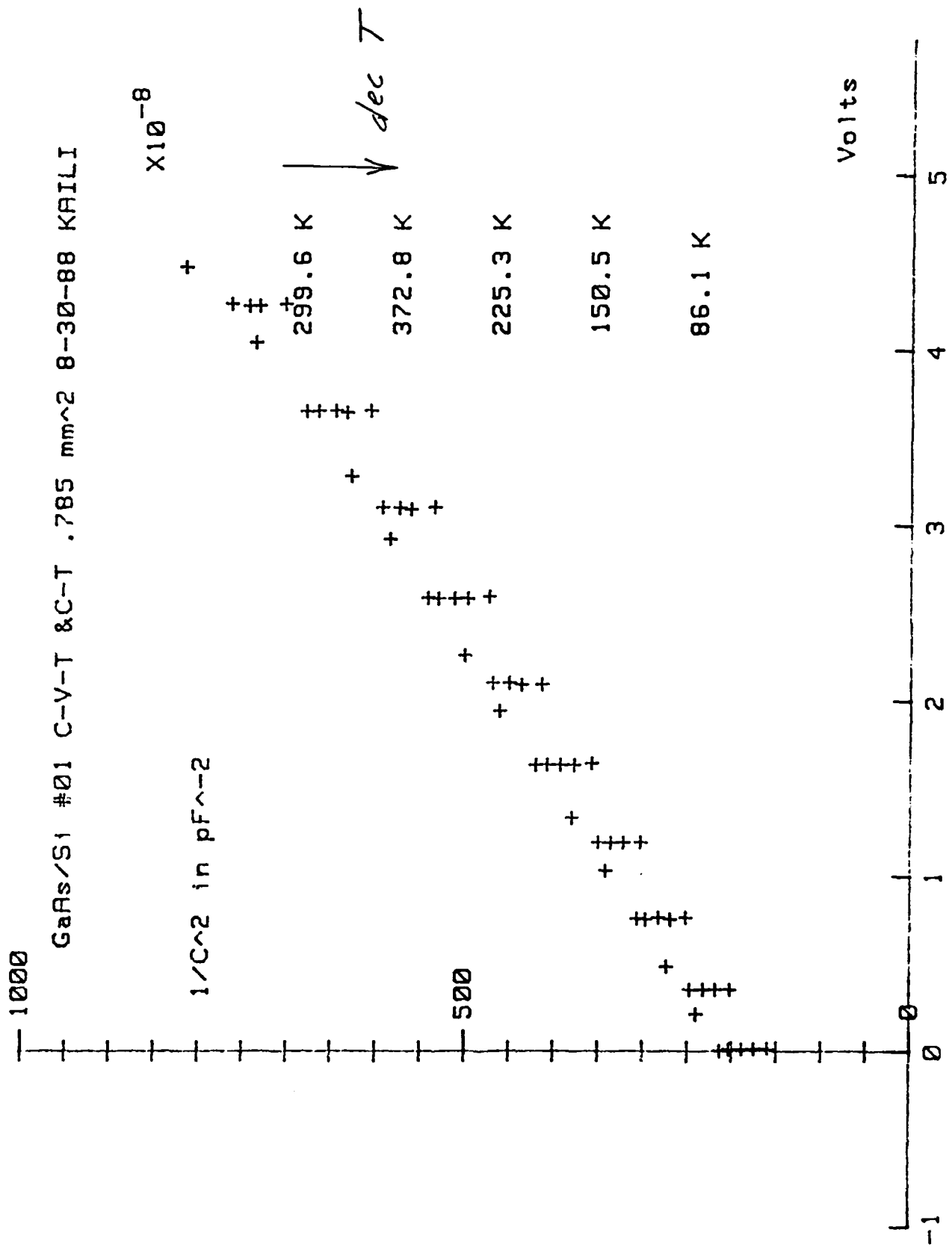


Figure 2 C-V-T for GaAs/Si

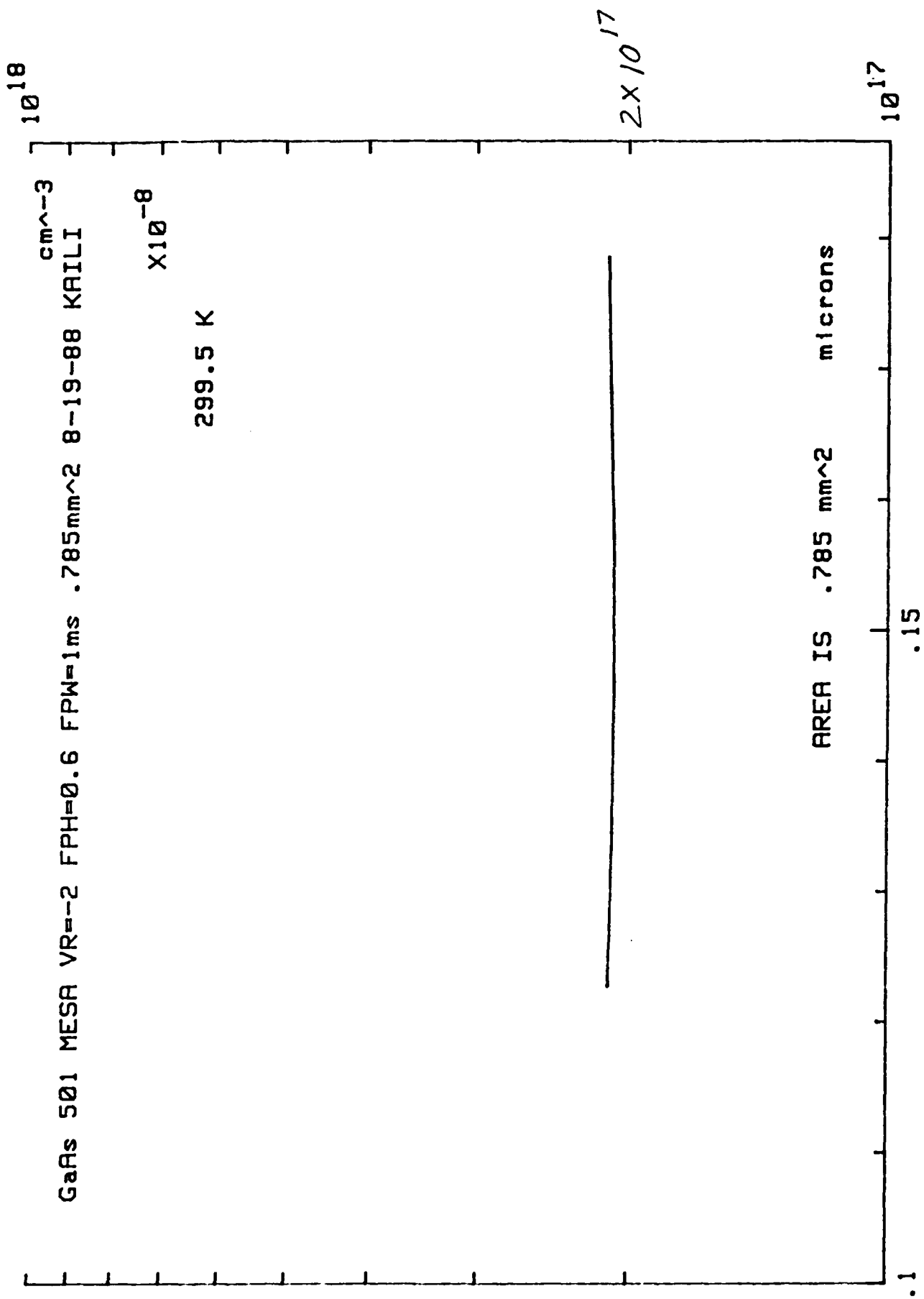


Figure 3 Doping (N) vs space charge layer width (W) for GaAs/GaAs

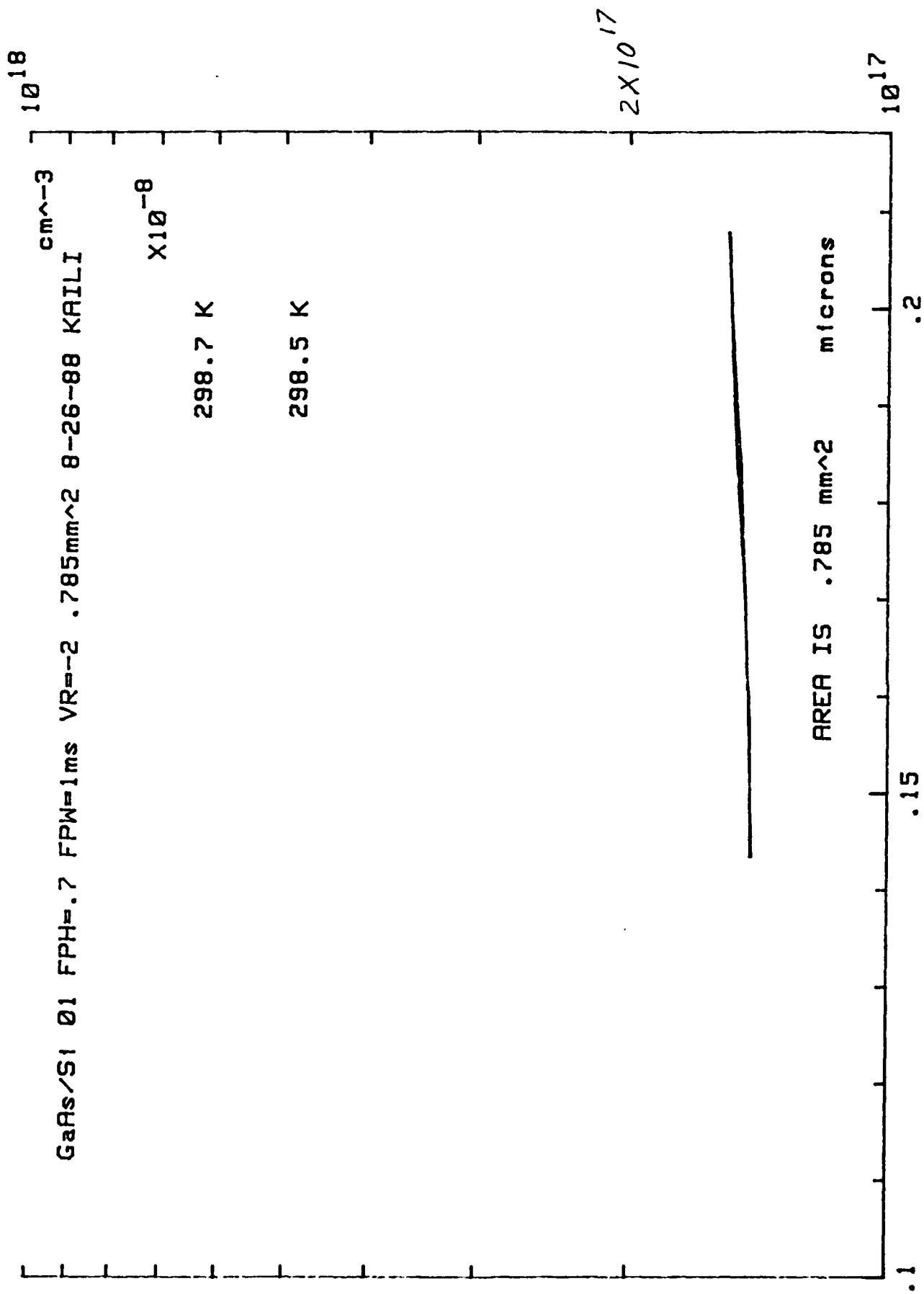


Figure 4 N-W for GaAs/SI

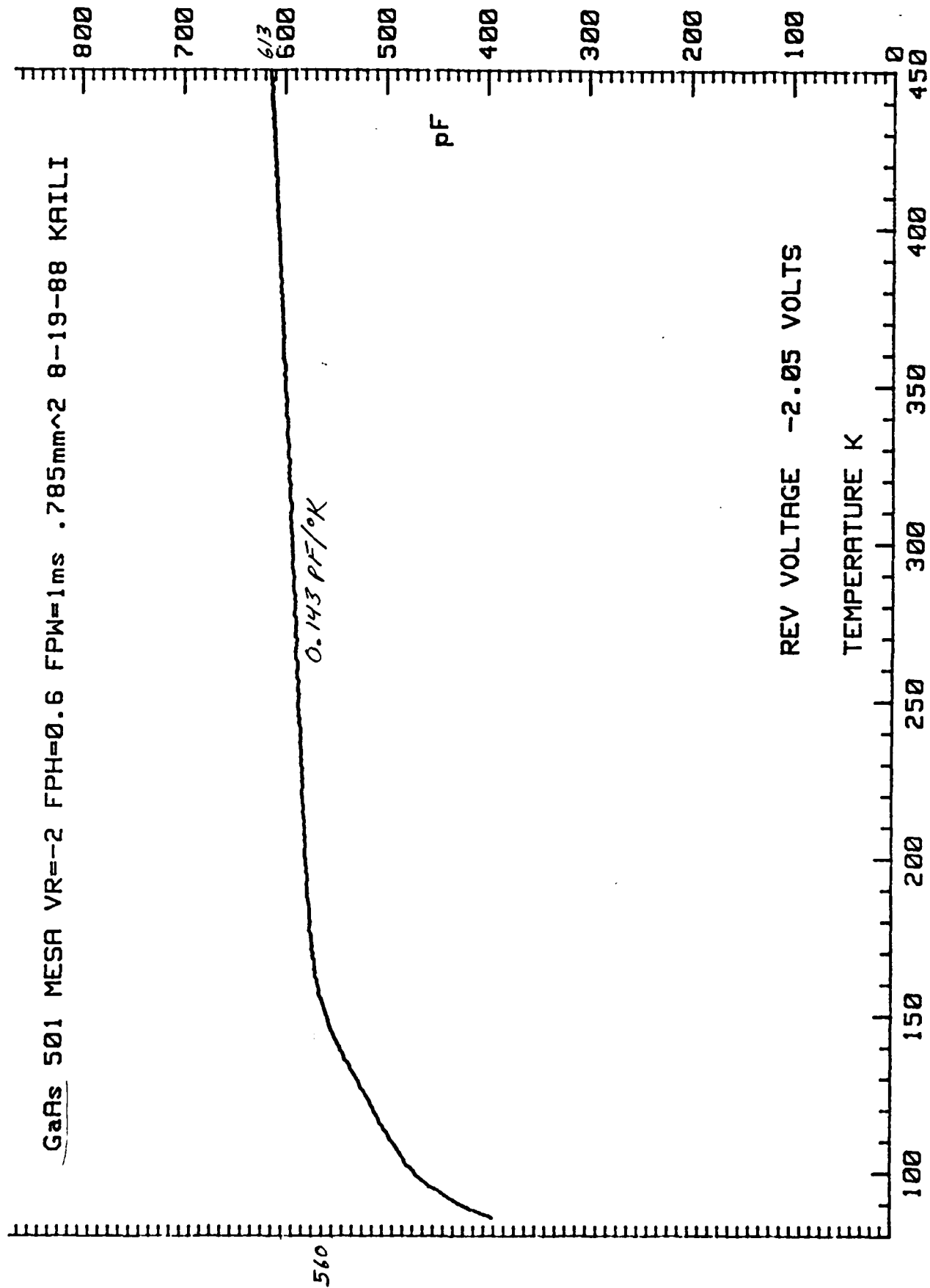


Figure 5 C-T for GaAs/GaAs

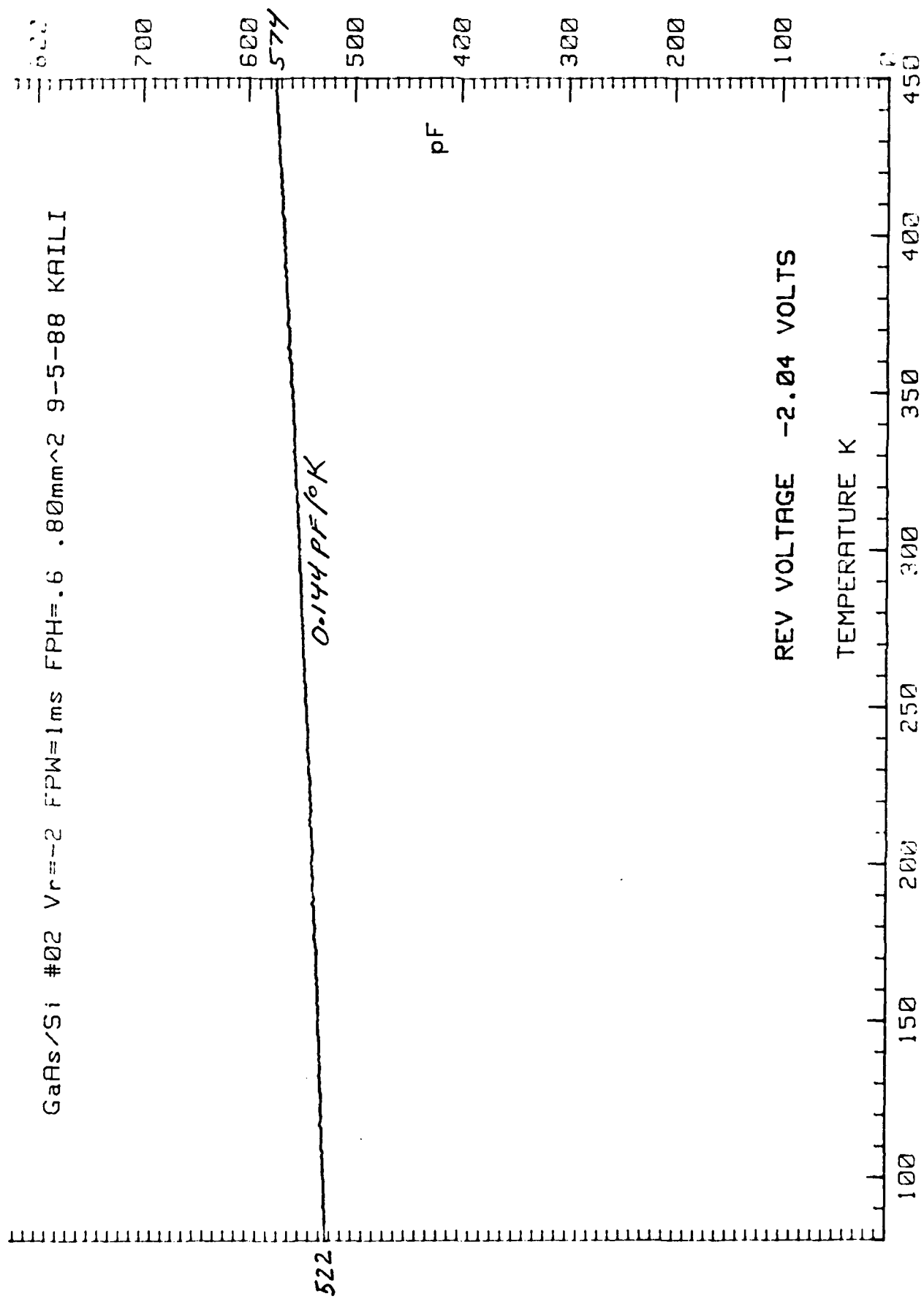


Figure 6 C-T for GaAs/Si

PR (MD2-024-5)

17 (1960-98.04)

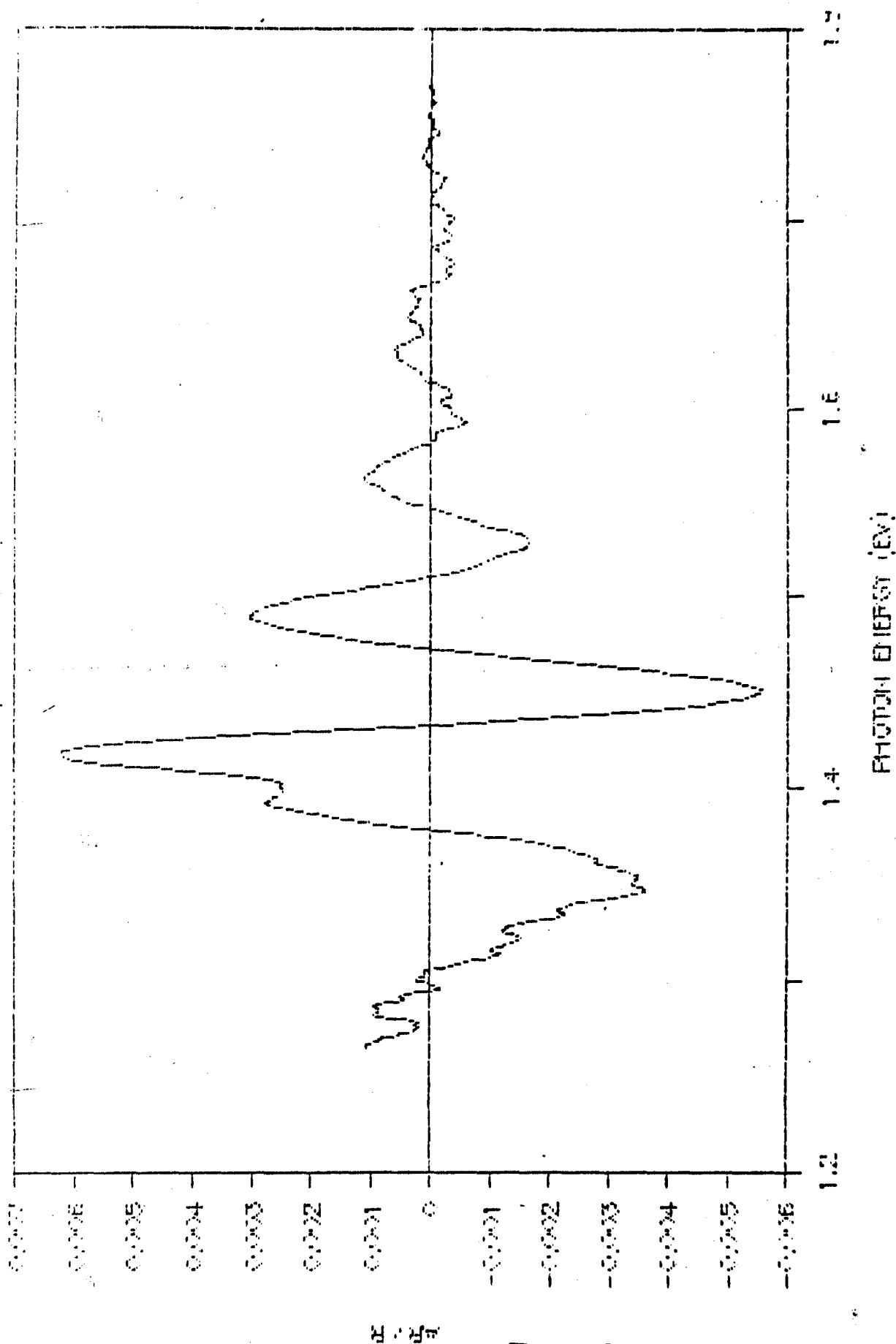


Figure 7 Photoreflectance (PR) for GaAs/GaAs

Best Available Copy

PR (MO2-1042-5)

USE (MO2-1042-5)

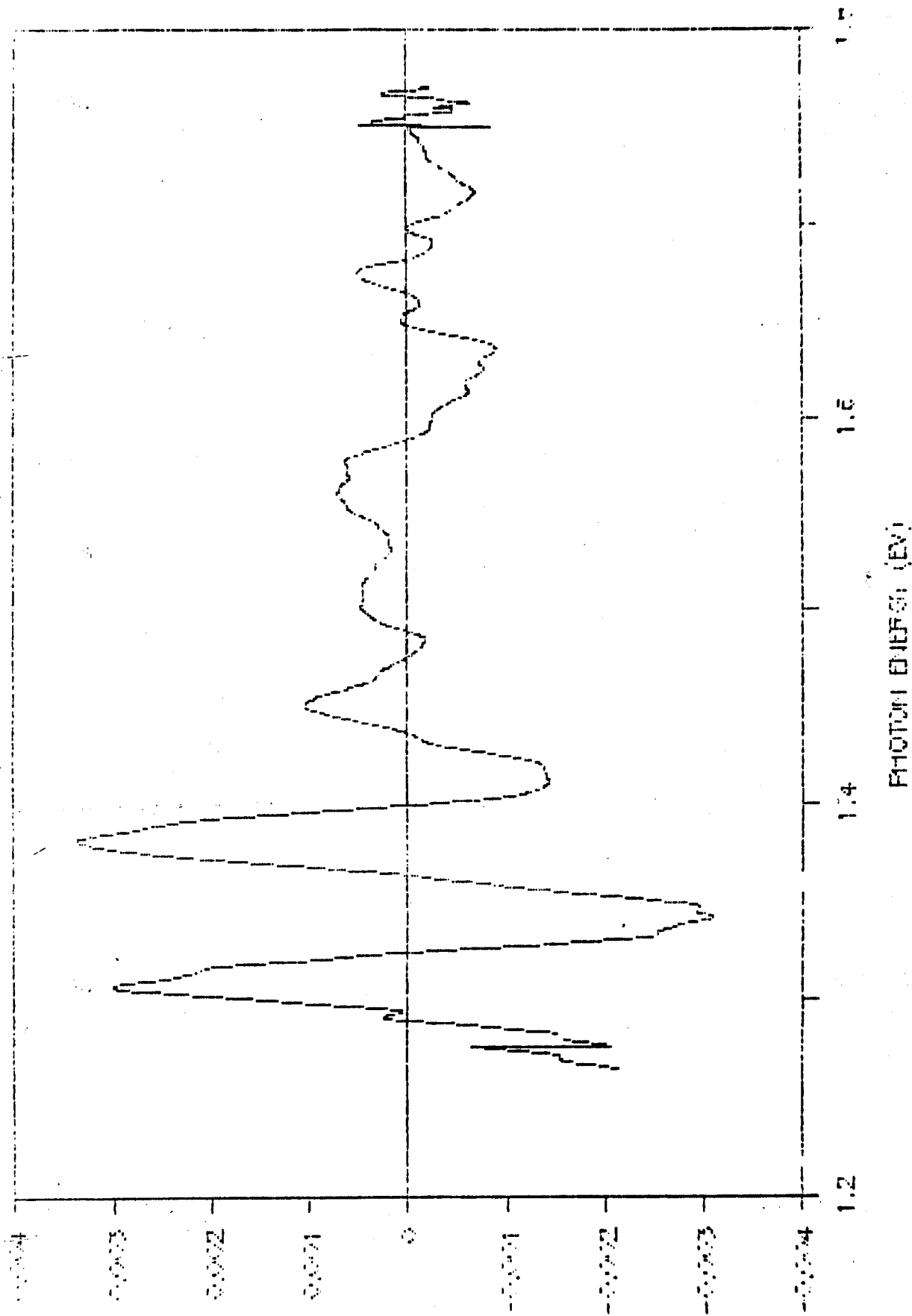


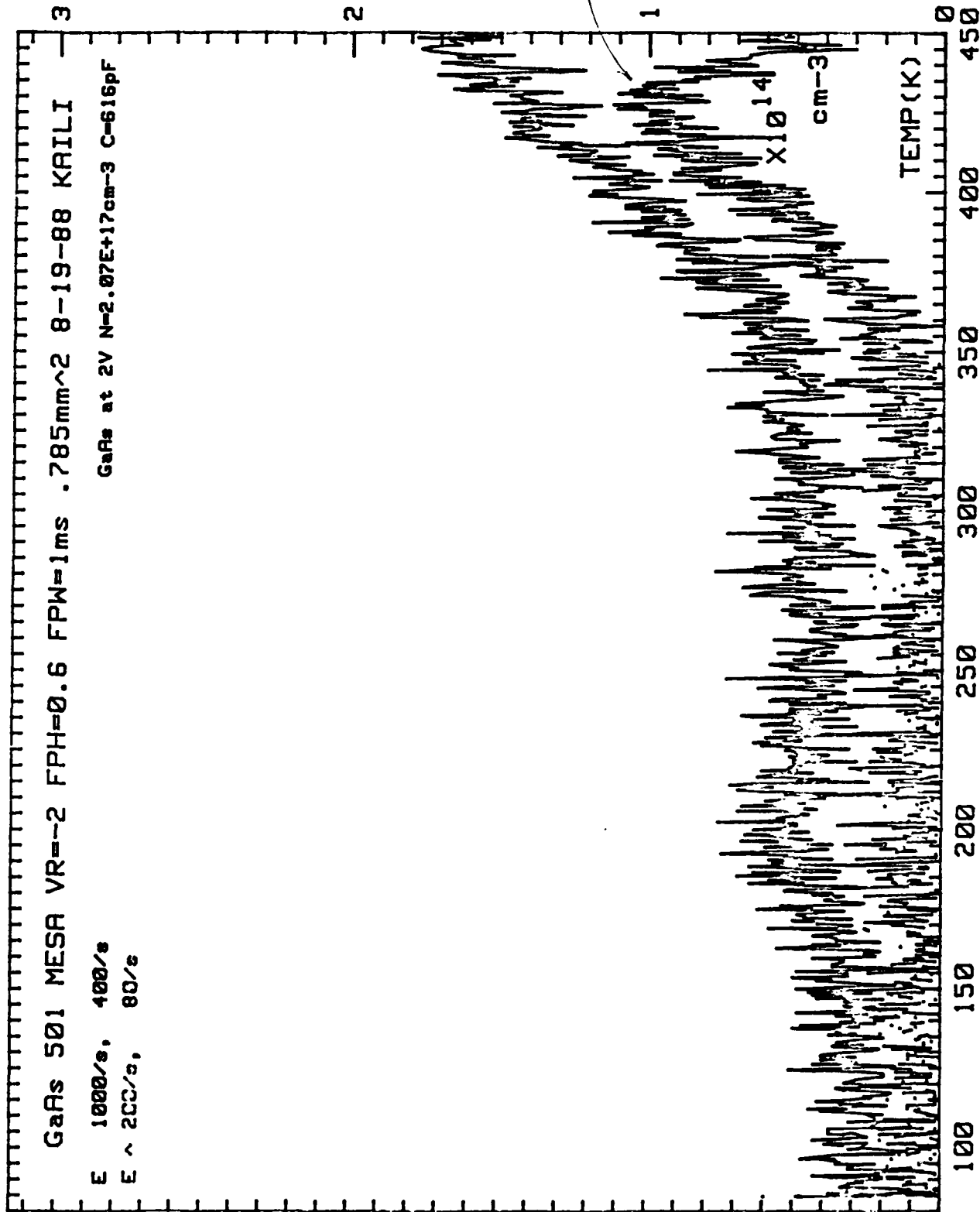
Figure 8 PR for GaAs/Si

3
GaAs 501 MESA VR=-2 FPH=0.6 FPW=1ms .785mm^2 8-19-88 KRILI

E 1000/s, 400/s

E ~ 200/s, 80/s

GaAs at 2V N=2.07E+17cm-3 C=616pF



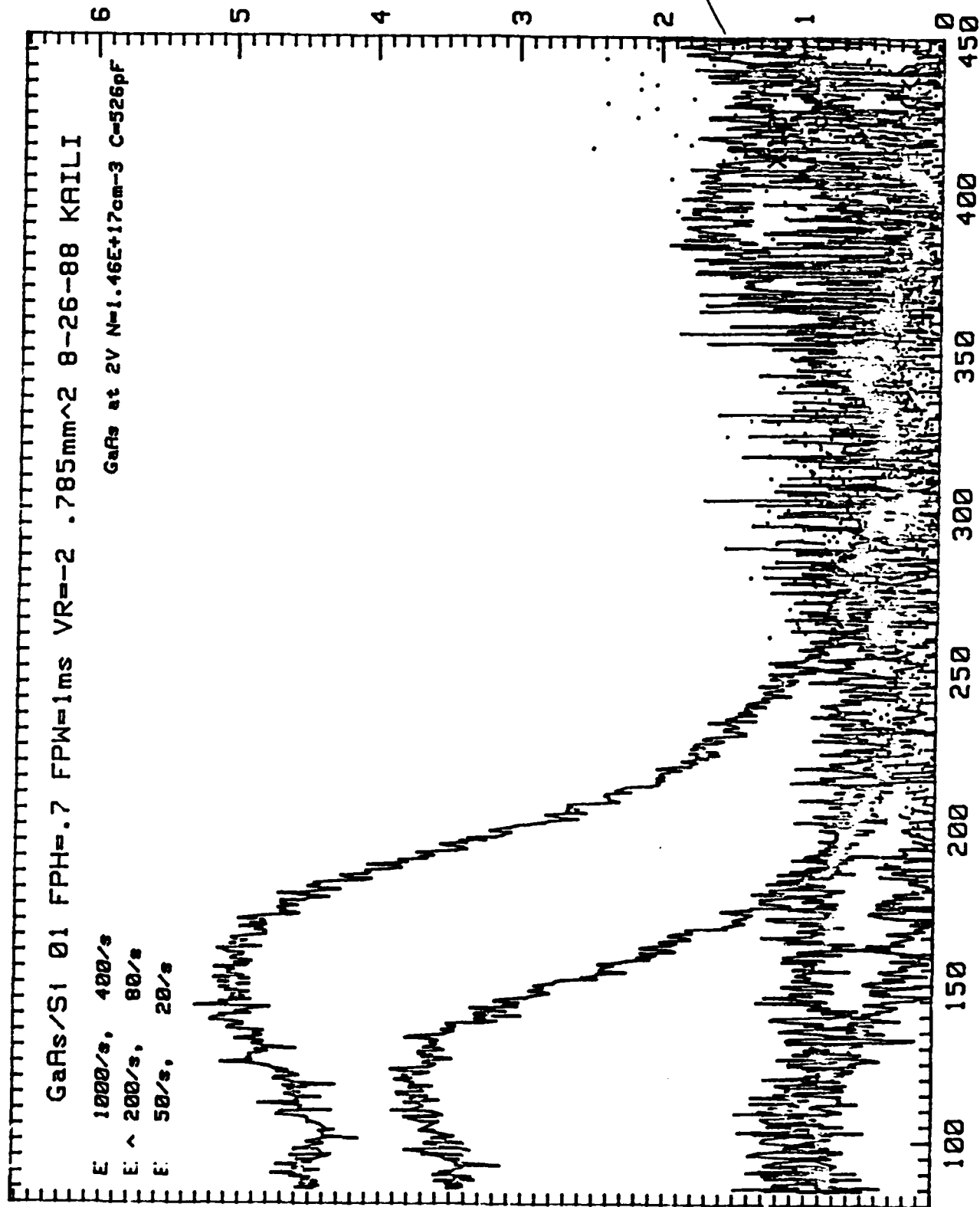


Figure 10 DLTS for GaAs/Si #01

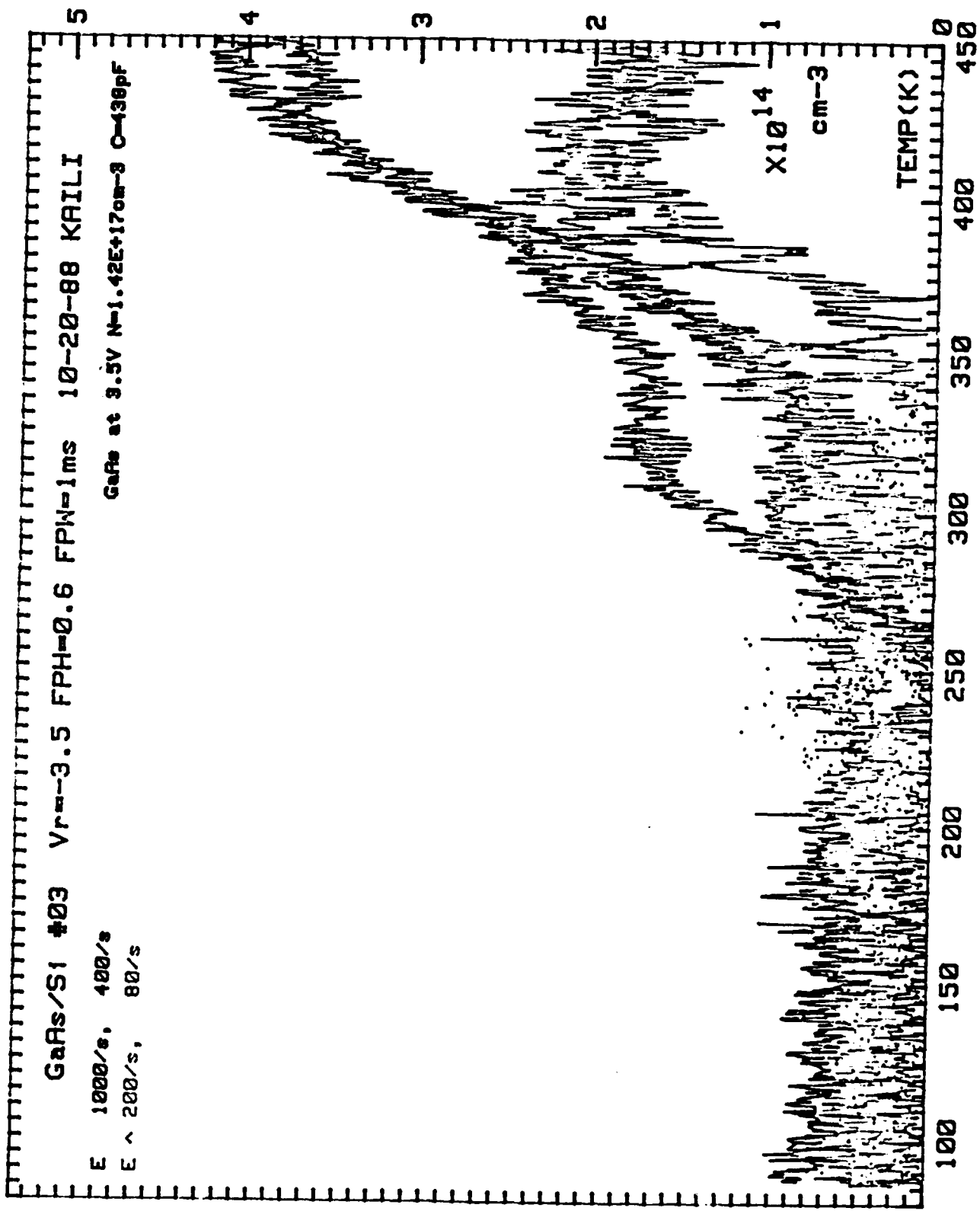


Figure 12 DLTS for GaAs/Si #03

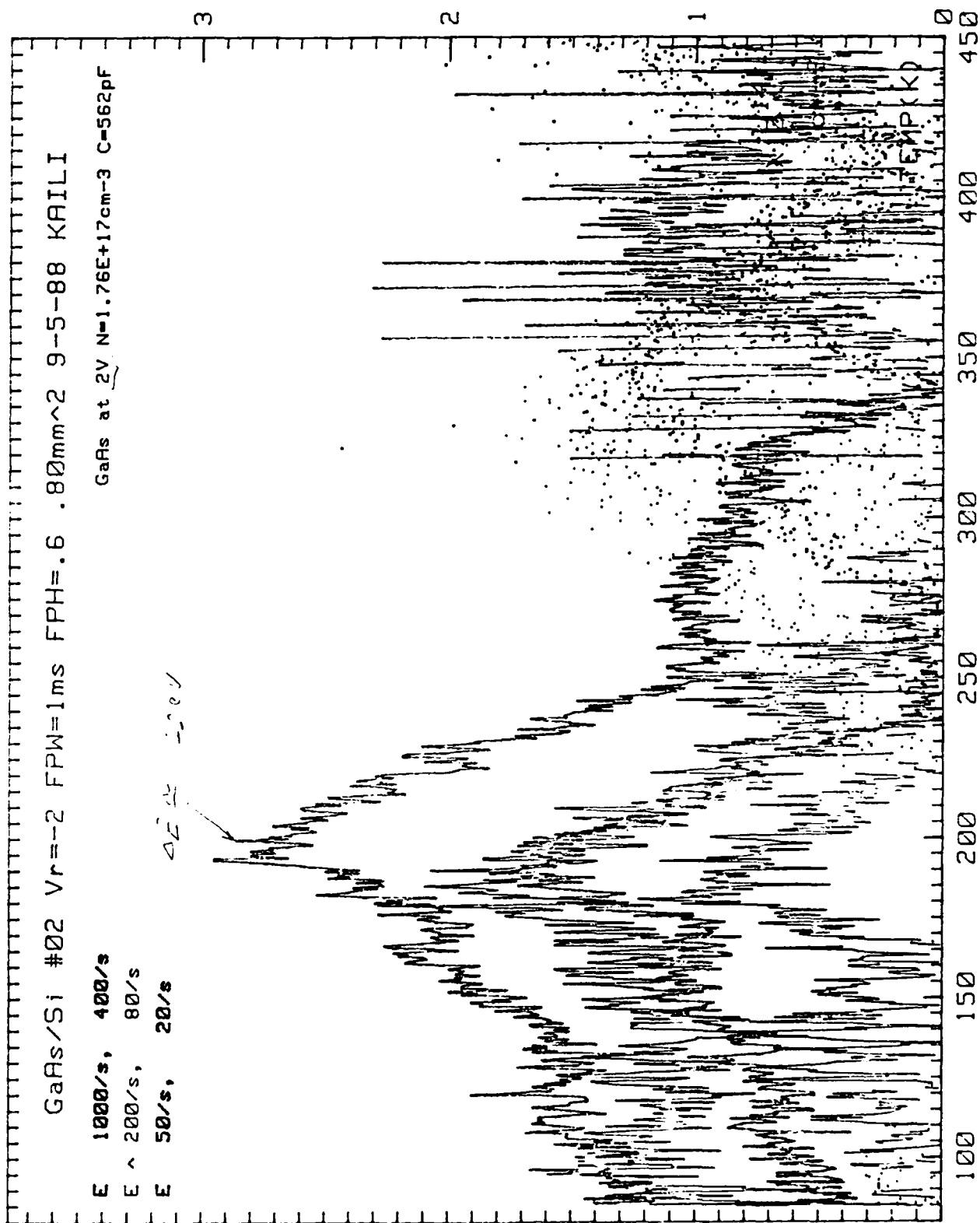


Figure 11 DLTS for GaAs/Si #02

TYPICAL I-V-T CHARACTERISTICS FOR GaAs LIMITATION
 DIODE GROWN ON GaAs SUBSTRATE

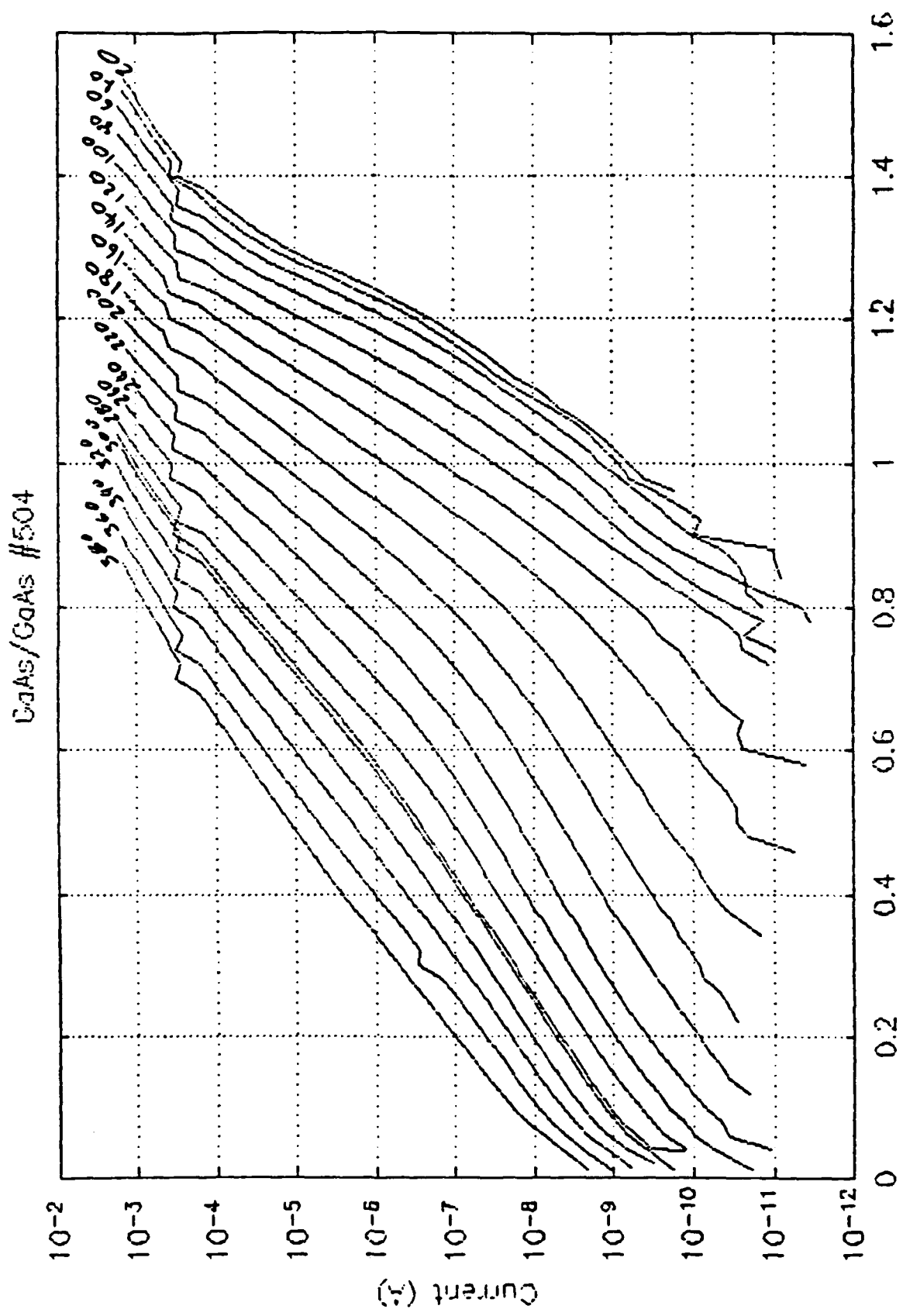


Figure 13

TYPICAL I-V-T CHARACTERISTICS FOR GaAs HOMOJUNCTION
DIODE GROWN ON Si SUBSTRATE

192

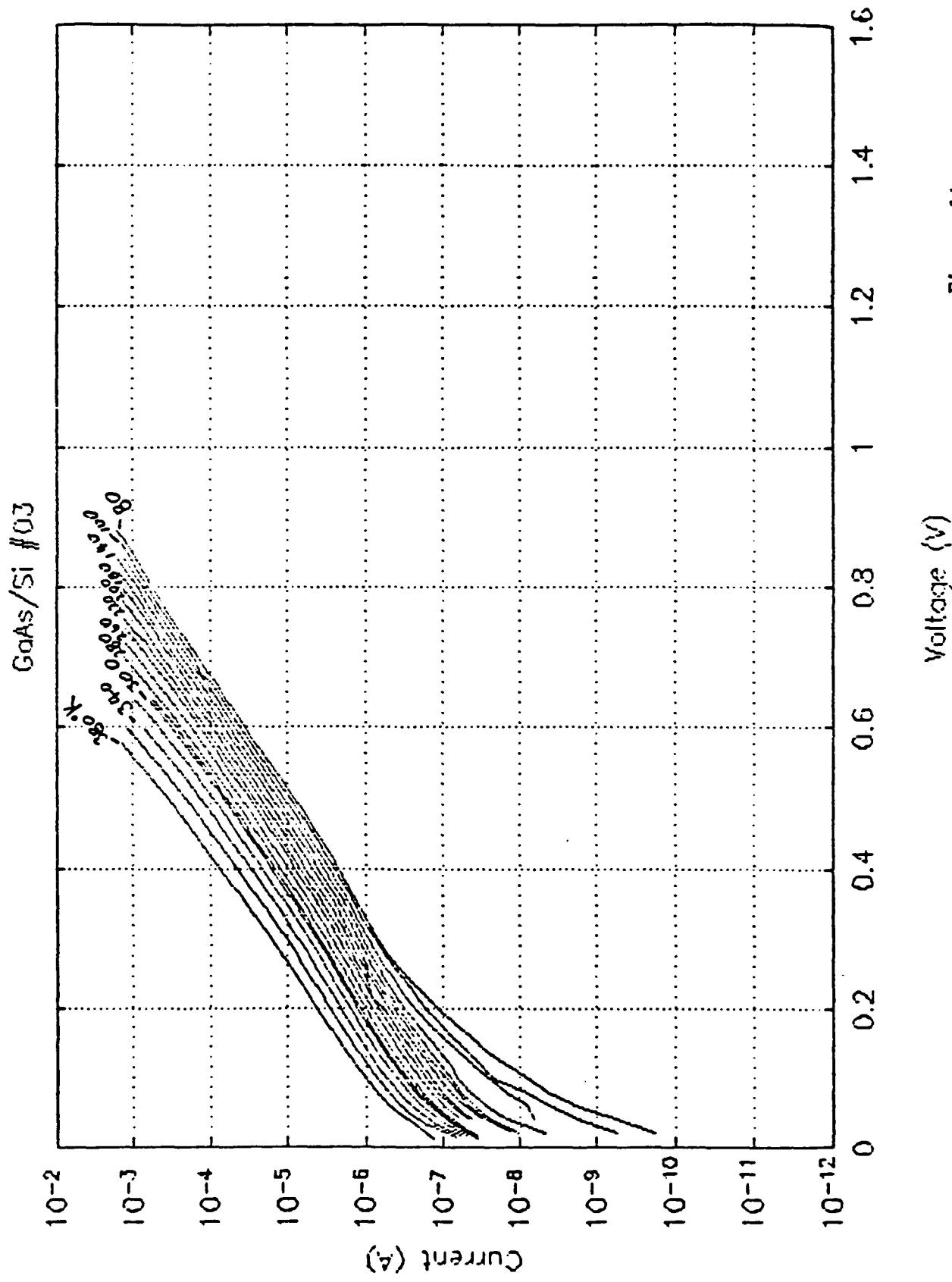
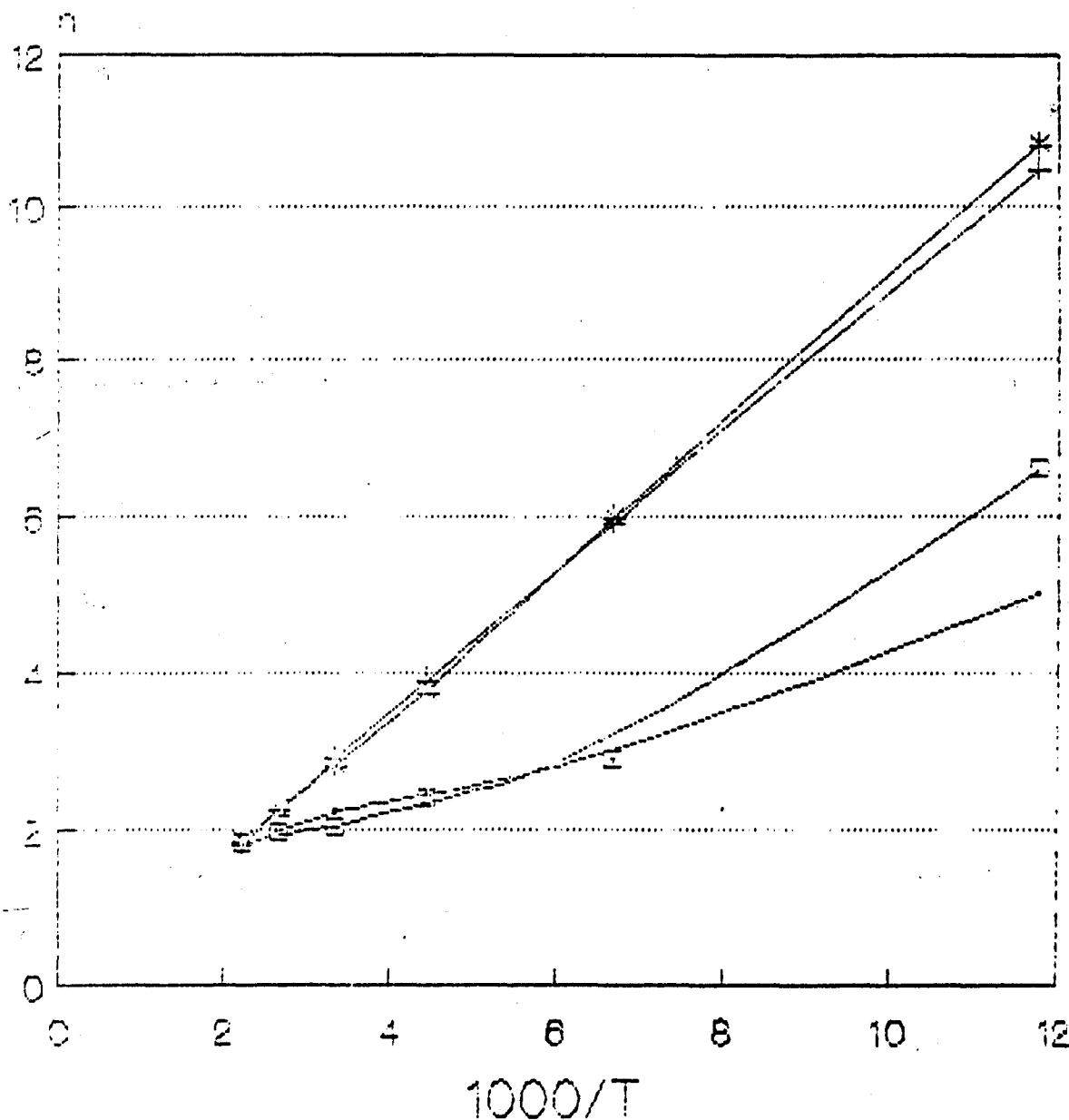


Figure 14 IVT for GaAs/Si

n VS 1000/T

22/10/80



—○— #04
GaAs/GaAs
—+— #03
GaAs/Si
—*— #01
GaAs/Si
—□— 501
Si/GaAs

Figure 15

Ideality factor (n) for GaAs/GaAs and GaAs/Si

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GaAs-GaAs Diodes

$\ln J_0$ vs $1000/T$

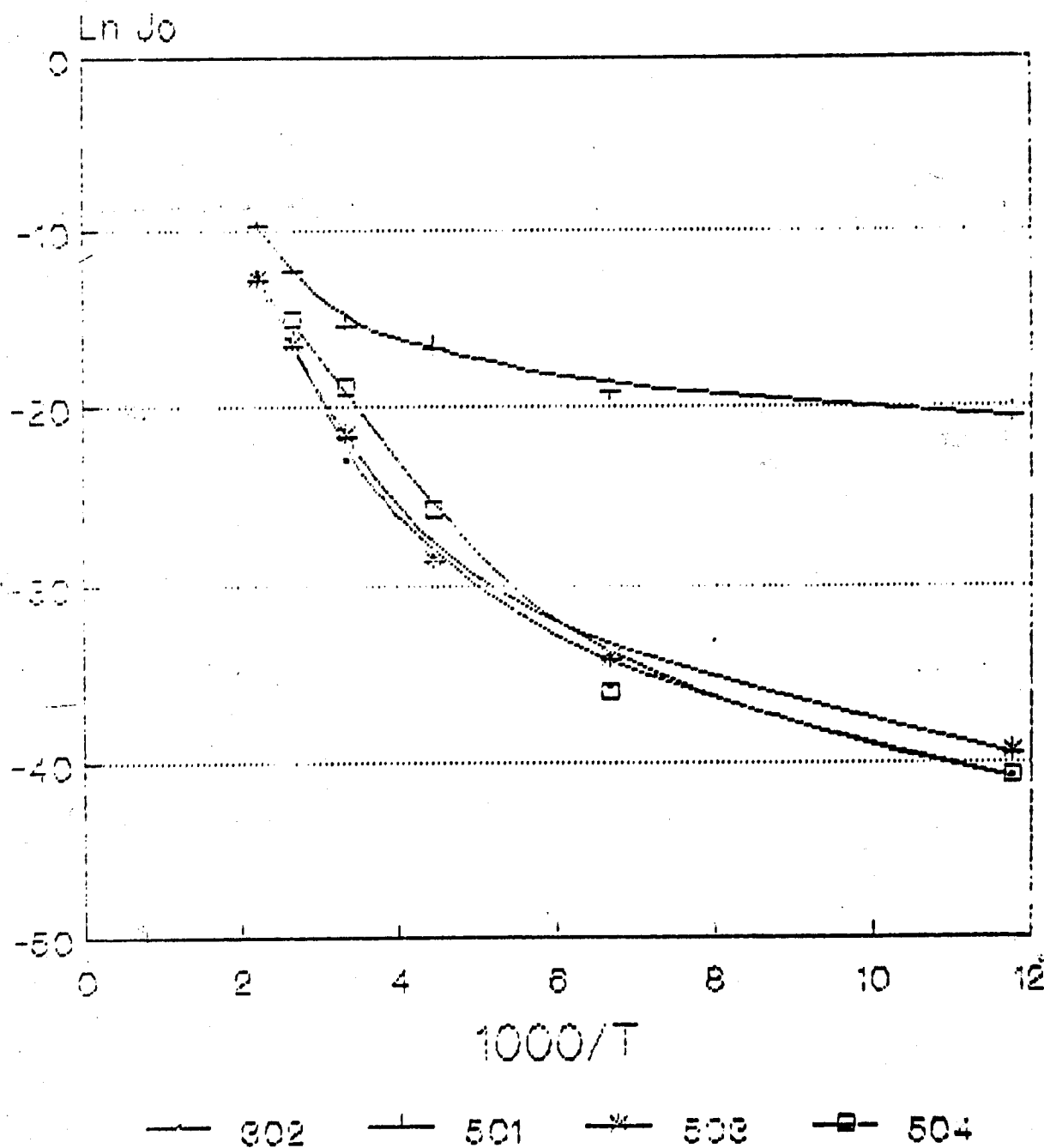
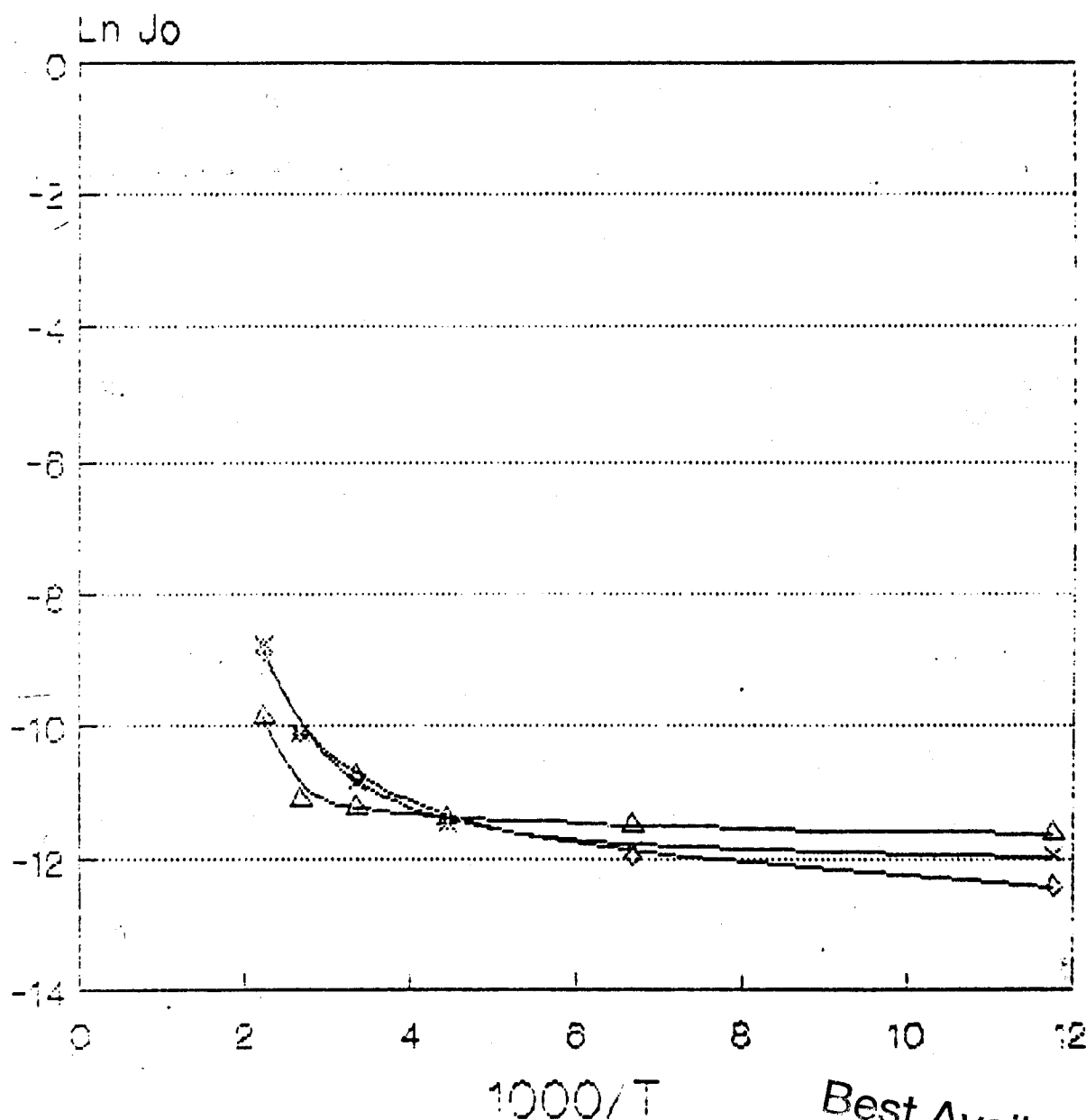


Figure 16 Reverse saturation current density ($\ln J_0$ vs $1000/T$) for GaAs/GaAs.
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GaAs-Si Diodes

$\ln J_0$ vs $1000/T$



—x— #C1 —+— #C2 —Δ— #C3

Best Available Copy

Figure 17

$\ln(J_0)$ vs $1000/T$ for GaAs/Si.

PART B: InP ON InP (n^+-p)

1. Mesa Diode Fabrication

A small piece was cut from the edge of the InP/InP solar cell wafer (#12-1). The back contact was protected by photoresist. On the front surface, a small dot was coated with black wax. Aqua regia was used to remove the front metal and then 1% Bromine methanol used for mesa etching, leading to a diode with area of about 0.95 mm^2 .

2. I-V Measurement

Fig. 1 shows the I-V curve taken at room temperature. The diode characteristics were derived to be: $J_0 = 7.37 \times 10^{-8} \text{ A/cm}^2$, $n = 1.38$.

3. C-V Measurements

Figs. 2-4 are the diagrams of $1/C^2$ -V, N_A -V and N_A -W. The fact that $1/C^2$ -V is a straight line indicates that the p-n junction is of good quality and the doping of the substrate is uniform. The doping concentration is about 10^{17} cm^{-3} . When bias varies from 0.71 to 4.24 volts, the width of the space charge region expands from 0.19 to 0.29 μm in distance from the junction. This is the region probed by DLTS.

4. DLTS Measurements

Fig. 5 is a typical DLTS spectrum which clearly shows three traps: one majority (H_1) and two minority (E_1 and E_2). The main characteristics of the traps are listed in Table 1.

Table 1* DLTS DATA

	Peak Location			
	(°K)	$E_A(\text{eV})$	$\sigma(\text{cm}^2)$	$N_T(\text{cm}^{-3})$
H_1	401.4 at 100/s	$E_v + 0.93$	1.39×10^{-13}	5.65×10^{14}
E_1	~320	?	?	5.5×10^{14}
E_2	210.3 at 100/s	$E_c - 0.40$	3.76×10^{-14}	2.3×10^{14}

*Data were taken with $V_1 = -3\text{V}$, fill pulse height (FPH) = 0.5V and fill pulse width (FPW) = 1ms.

E_1 is a strange trap in that the peaks from different rate windows are condensed so that the Arrhenious plot ($e_n/T^2 \sim 1000/T$) gives an activation energy larger than the bandgap of InP. Data may not be easily interpreted due to closeness in energy of the traps which leads to an interaction. The Arrhenious plots of H_1 and E_2 are shown in Fig. 6 and Fig. 7 respectively. Because the peak positions of E_2 are not very clear, the plot might not be accurate.

For a more detailed study, the value of bias (V_r), FPH and FPW were varied separately. When $|V_r|$ increased (Figs. 9-11) from 1V to 5V, the peak heights of H_1 increased whereas those for E_1 decreased, as shown in Fig. 8. Also, at $V_r = -5V$, the peaks of H_1 became much wider and some small hole trap peaks emerged around 260 and 150°K. This might imply that the H_1 trap is more related to the deeper part of the epi layer, while E_1 is more surface related. In addition, the peak positions of E_1 shifted a little toward low temperature. The variation of E_2 is not as remarkable as H_1 and E_1 .

A more interesting phenomena was observed when FPH changed (Figs. 12-16) from positive to negative: the peaks of E_1 were disappearing but the peaks of H_1 were broadening. These again seem to be in favor of the argument mentioned above. The variation of FPW showed (Figs. 17-24) that 1 ms was long enough to fill up the traps. The analysis of these data also indicated that nonexponential transients might be responsible for the distortion of the trap peaks.

Fig. 25 is a DLTS simulation with the parameters of H_1 obtained from the experiments. This reveals the fact that the existence of the real traps could be very complicated. They could be a complex of several levels causing the capture and emission processes to be nonexponential.

FIGURE CAPTIONS

- | | |
|-----------|---|
| Figure 1 | I-V Data for InP/InP |
| Figure 2 | $1/C^2$ -V Data |
| Figure 3 | Doping Concentration (N) vs applied voltage (V) |
| Figure 4 | N vs space charge layer width (W) |
| Figure 5 | DLTS spectra |
| Figure 6 | Activation plot of H_1 |
| Figure 7 | Activation plot of E_2 |
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| Figure 11 | DLTS @ $V_R = -5V$ |
| Figure 12 | DLTS @ FPH = -0.5V |
| Figure 13 | DLTS @ FPH = 0.0V |
| Figure 14 | DLTS @ FPH = +0.25V |
| Figure 15 | DLTS @ FPH = +0.75V |
| Figure 16 | DLTS @ FPH = +1.0V |
| Figure 17 | DLTS @ FPW = 5 ms |
| Figure 18 | DLTS @ FPW = 1 ms |
| Figure 19 | DLTS @ FWP = 0.5 ms |
| Figure 20 | DLTS @ FWP = 0.1 ms |
| Figure 21 | DLTS @ FPW = 50 μs |
| Figure 22 | DLTS @ FPW = 10 μs |
| Figure 23 | DLTS @ FPW = 5 μs |
| Figure 24 | DLTS @ FPW = 1 μs |
| Figure 25 | Computer Simulation of H_1 |

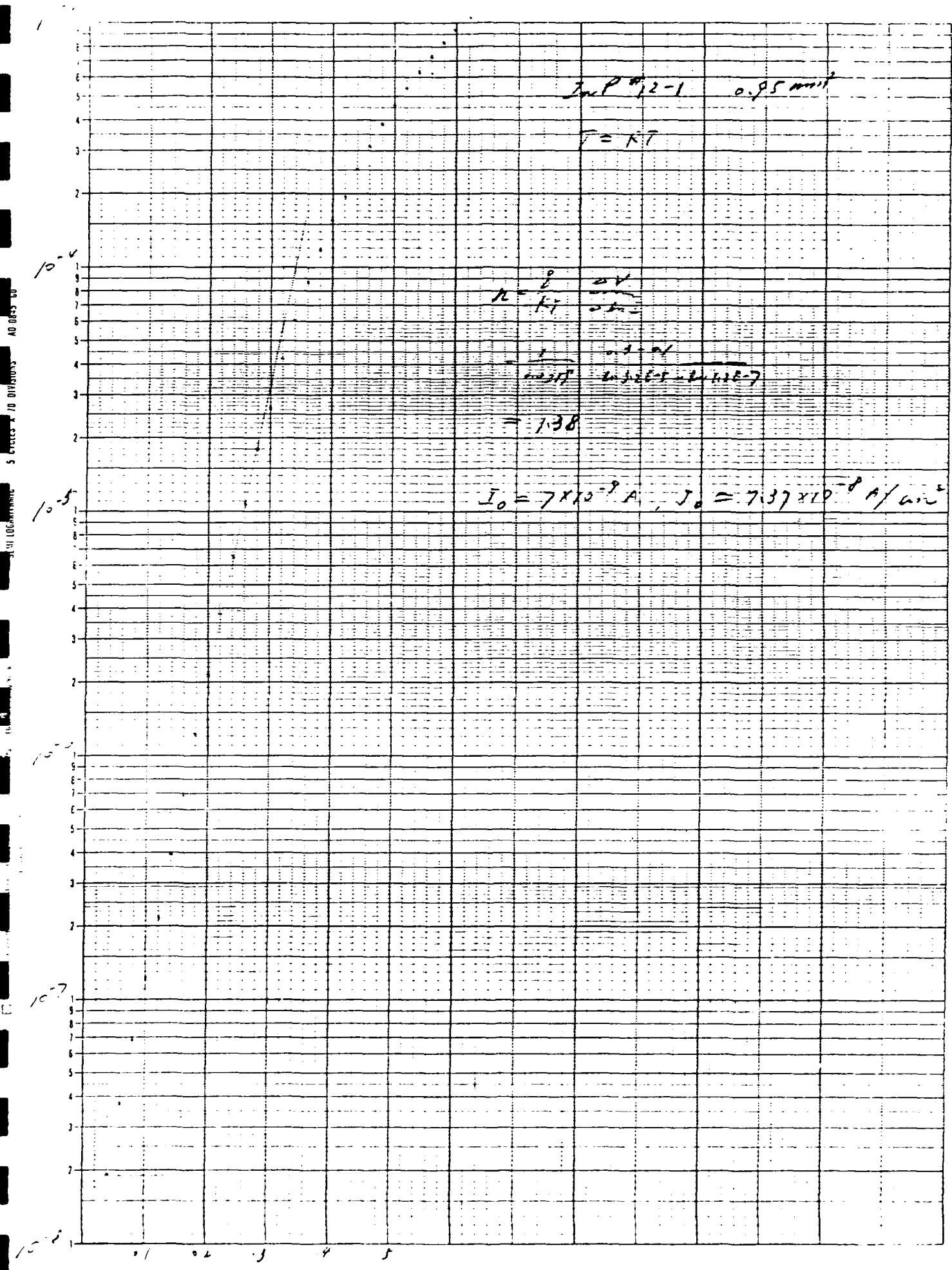


Figure 1

I-V Data for InP/InP

InP SC #12-1 .95mm² V_r=-3 FPH=.5 FFW=1ms KAILI 3-2 -83

X10⁻⁸

1/C² in pF⁻²

304.8 K

500

Volts

-1

0

1

2

3

4

5

6

$\phi \approx 1.55 \text{ eV}$

Figure 2 1/C²-V Data

Fig 2

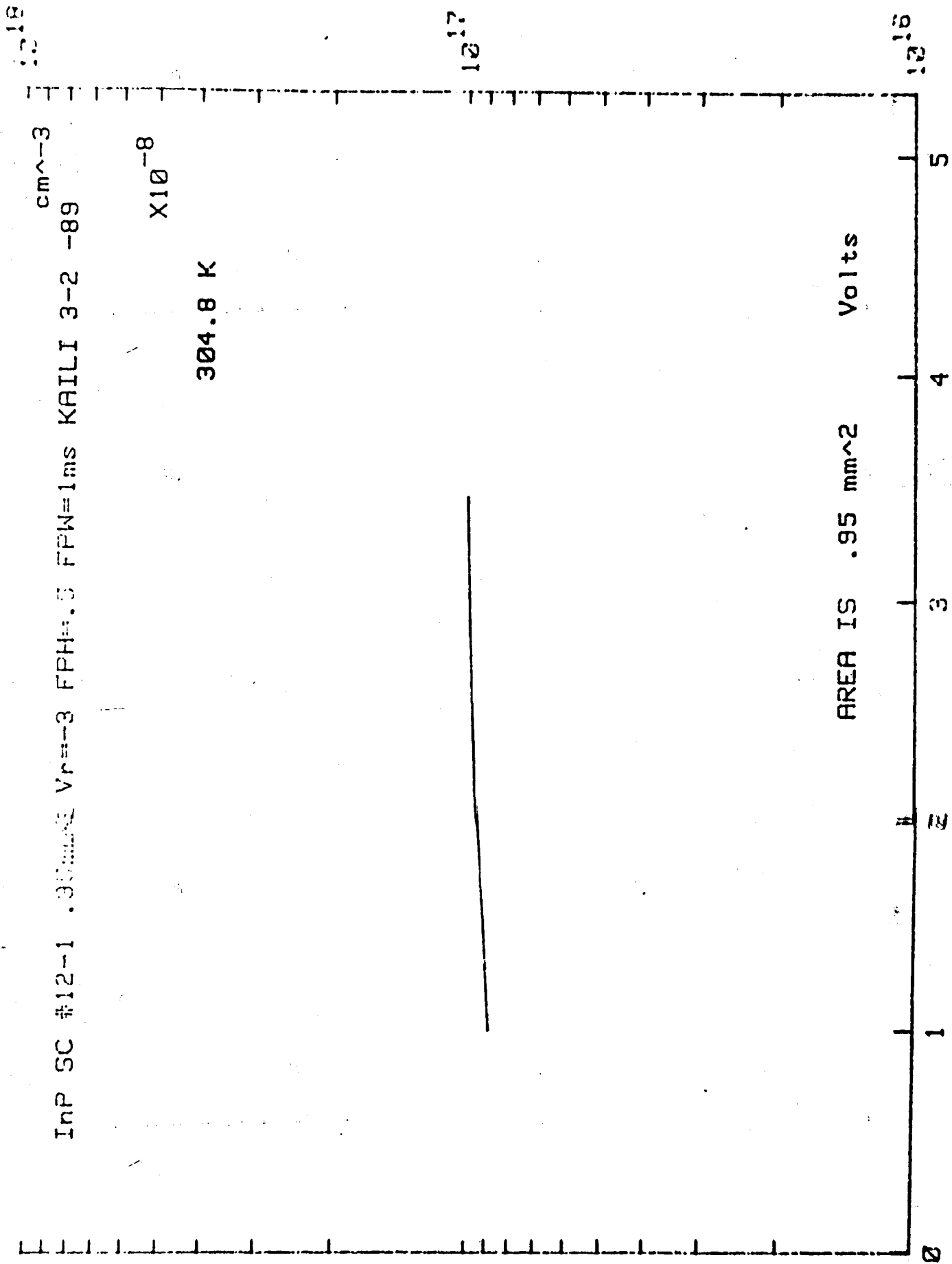
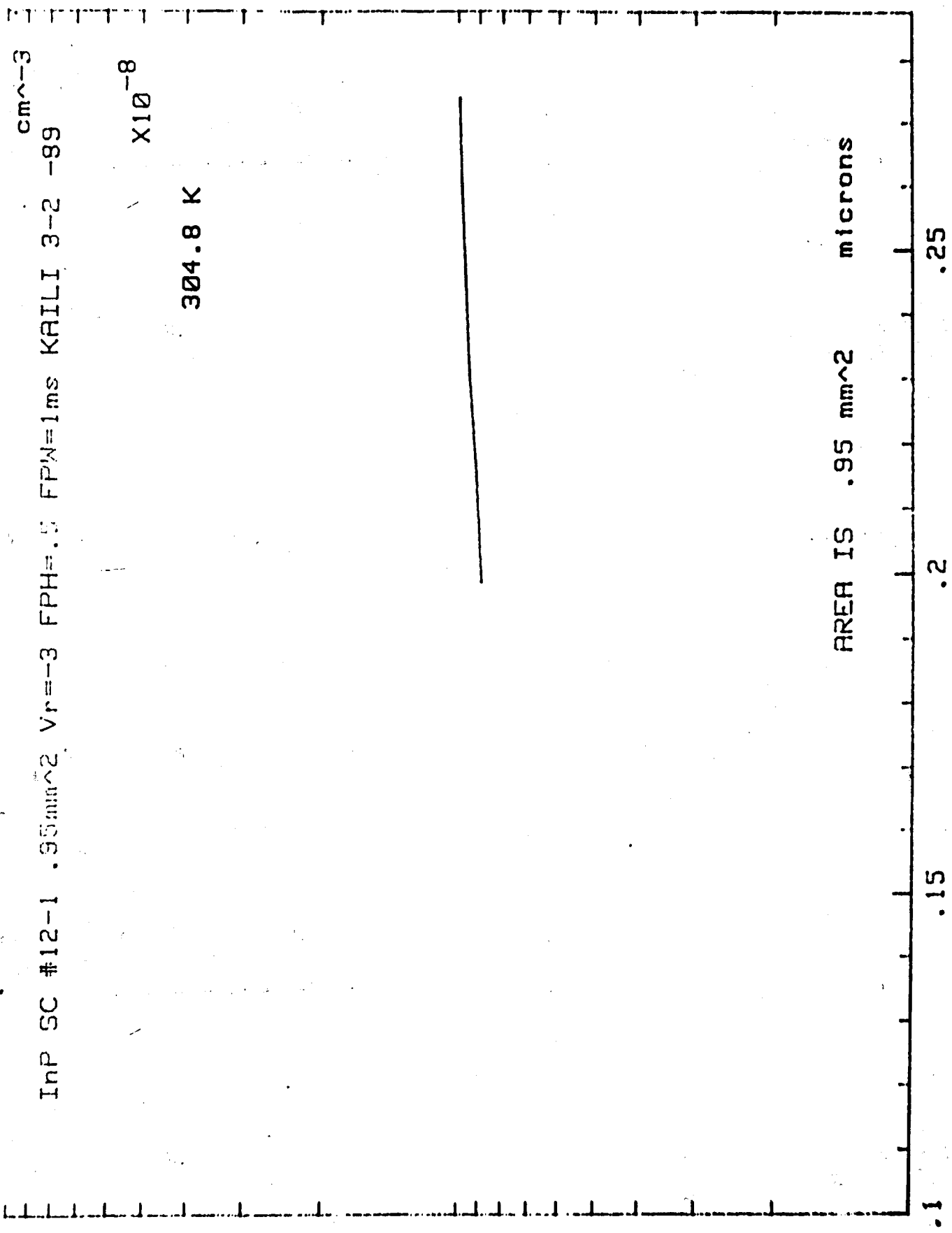


Figure 3 Doping Concentration (N) vs applied voltage (V)

1018

1017

1019



InP SC #12-1 .95mm² Vr=-3 FPH=.5 FFW=1ms KAILI 3-2 -99

Figure 4 N vs space charge layer width (W)

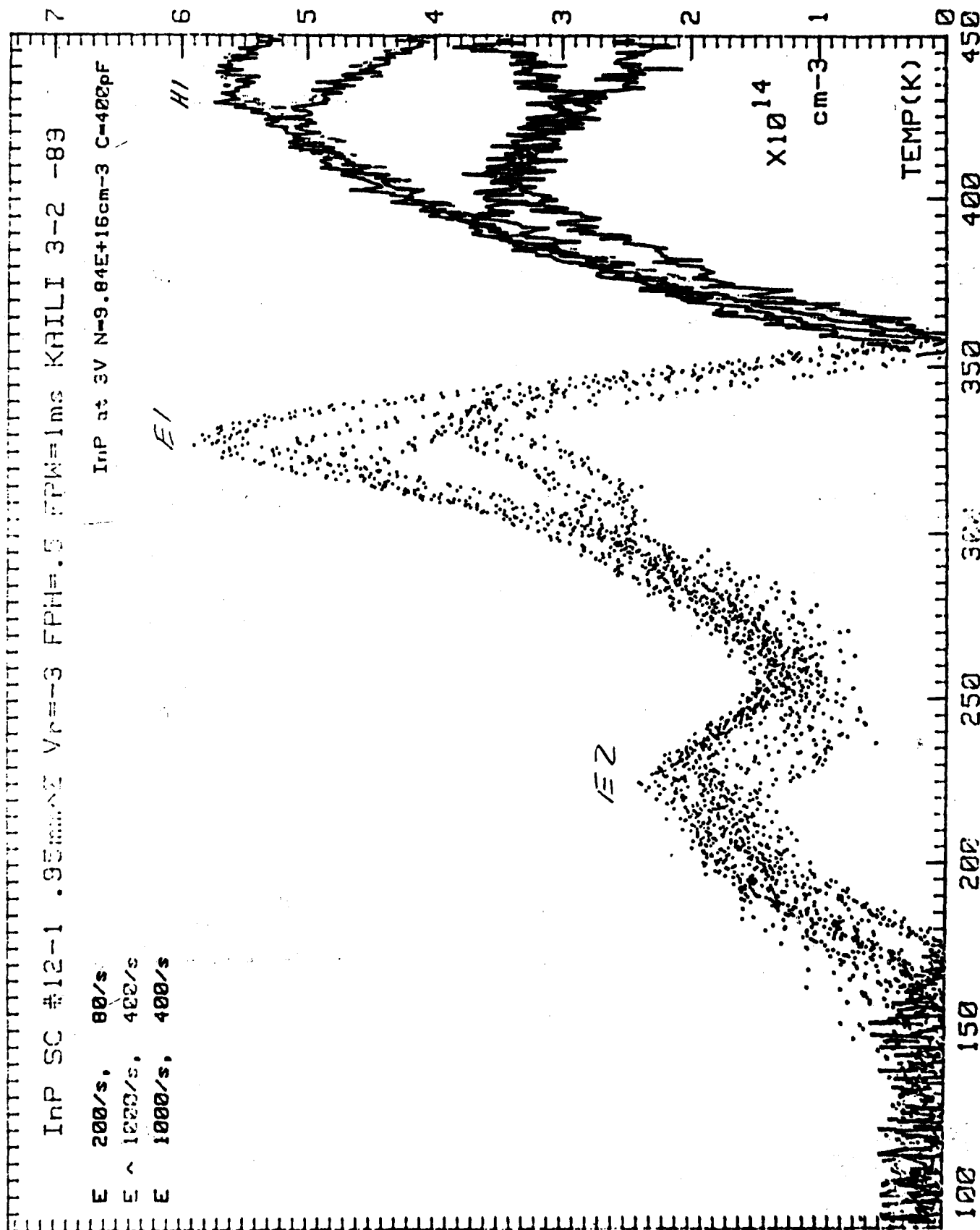


Figure 5 DLTS spectra

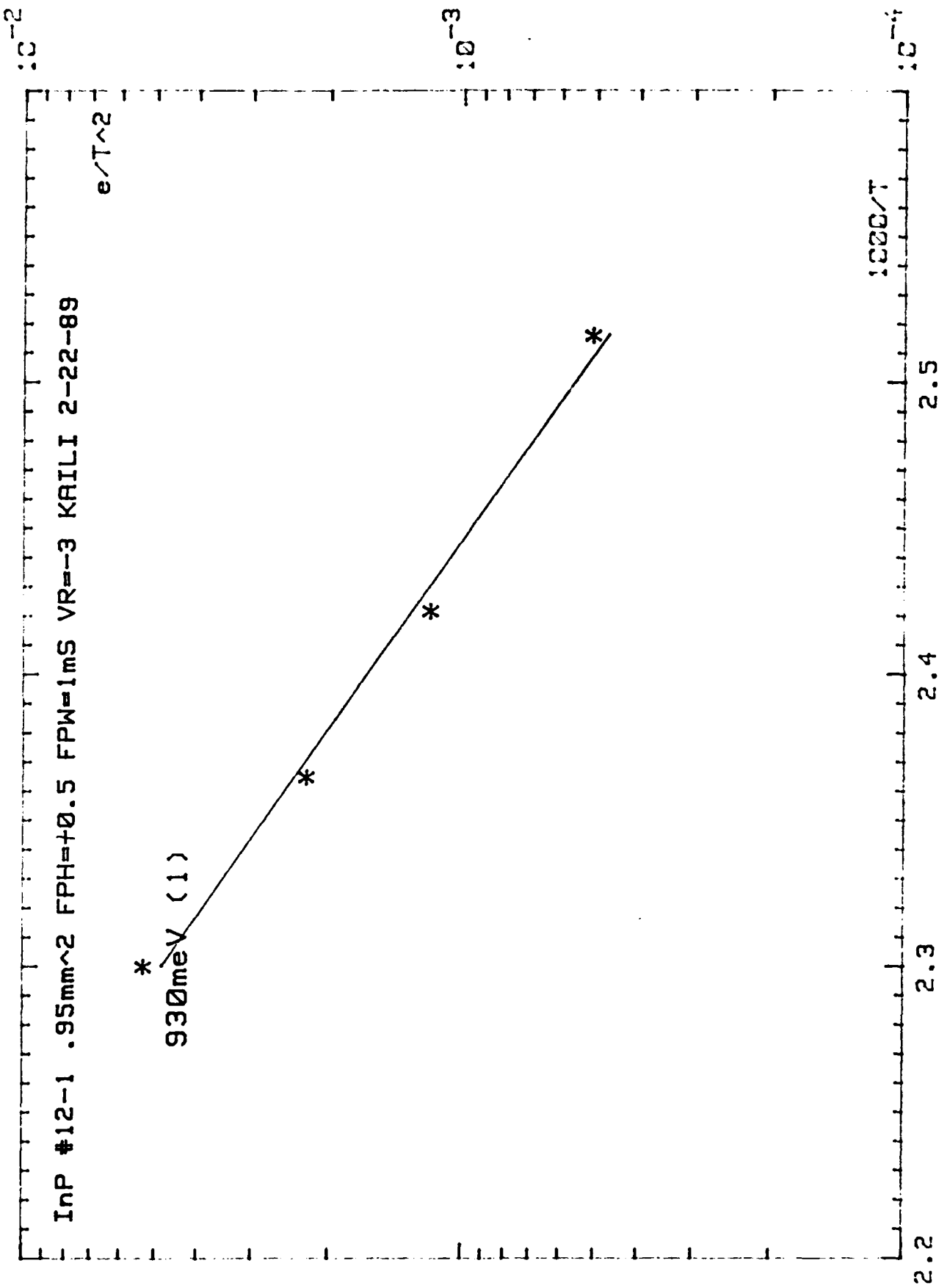


Figure 6 Activation plot of H_1

$E_g = 402 \text{ meV}$ 7 (@100%) = 2/0.3K Indep't = 8.44EeV/K, $\sigma = 3.76 \text{ E-14 cm}^2$

INP SOLAR CELL #12-1 .95mm² FPW=1ms FPH=.5V KAILI 2-16-89

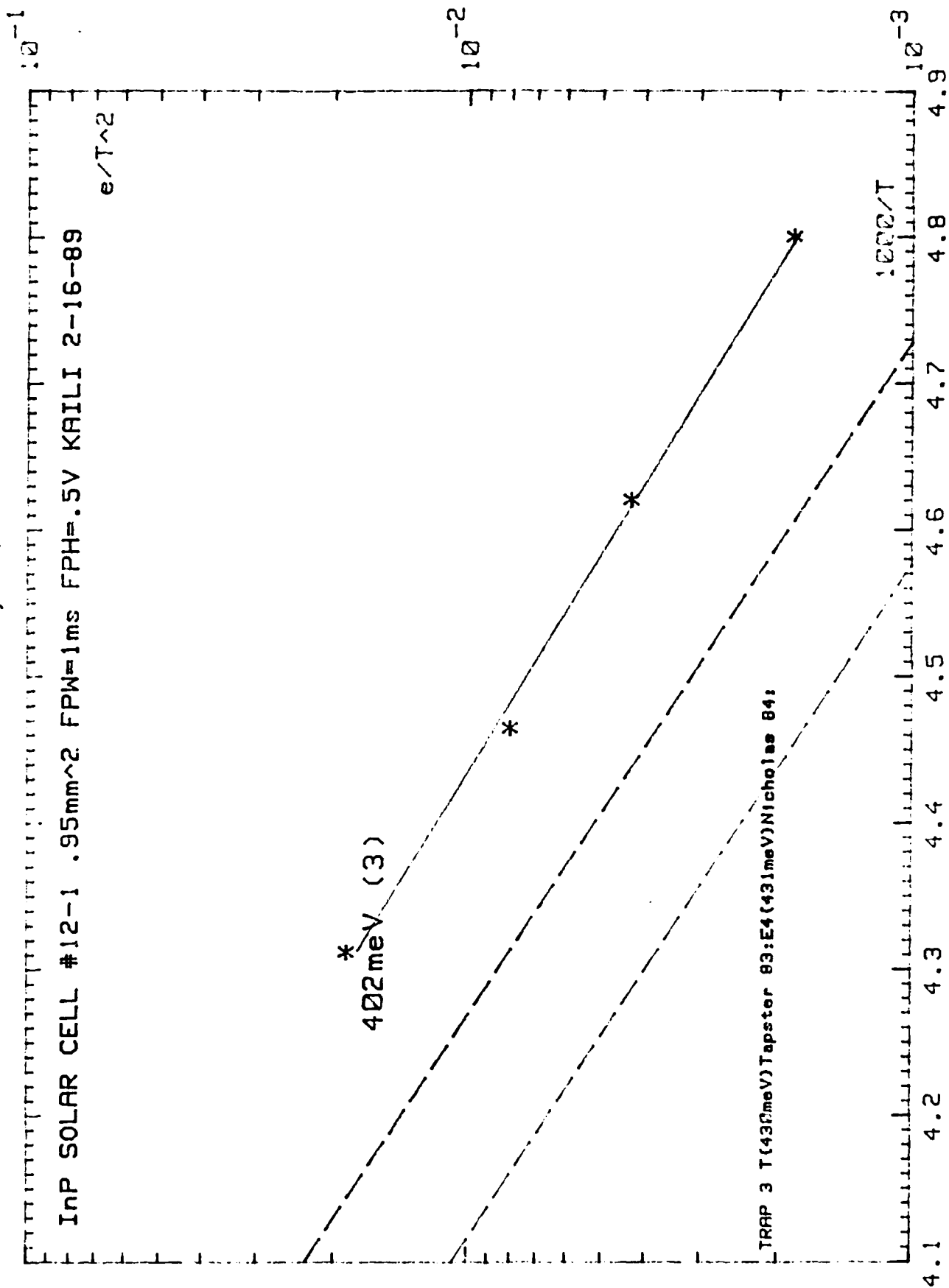


Figure 7 Activation plot of E_2

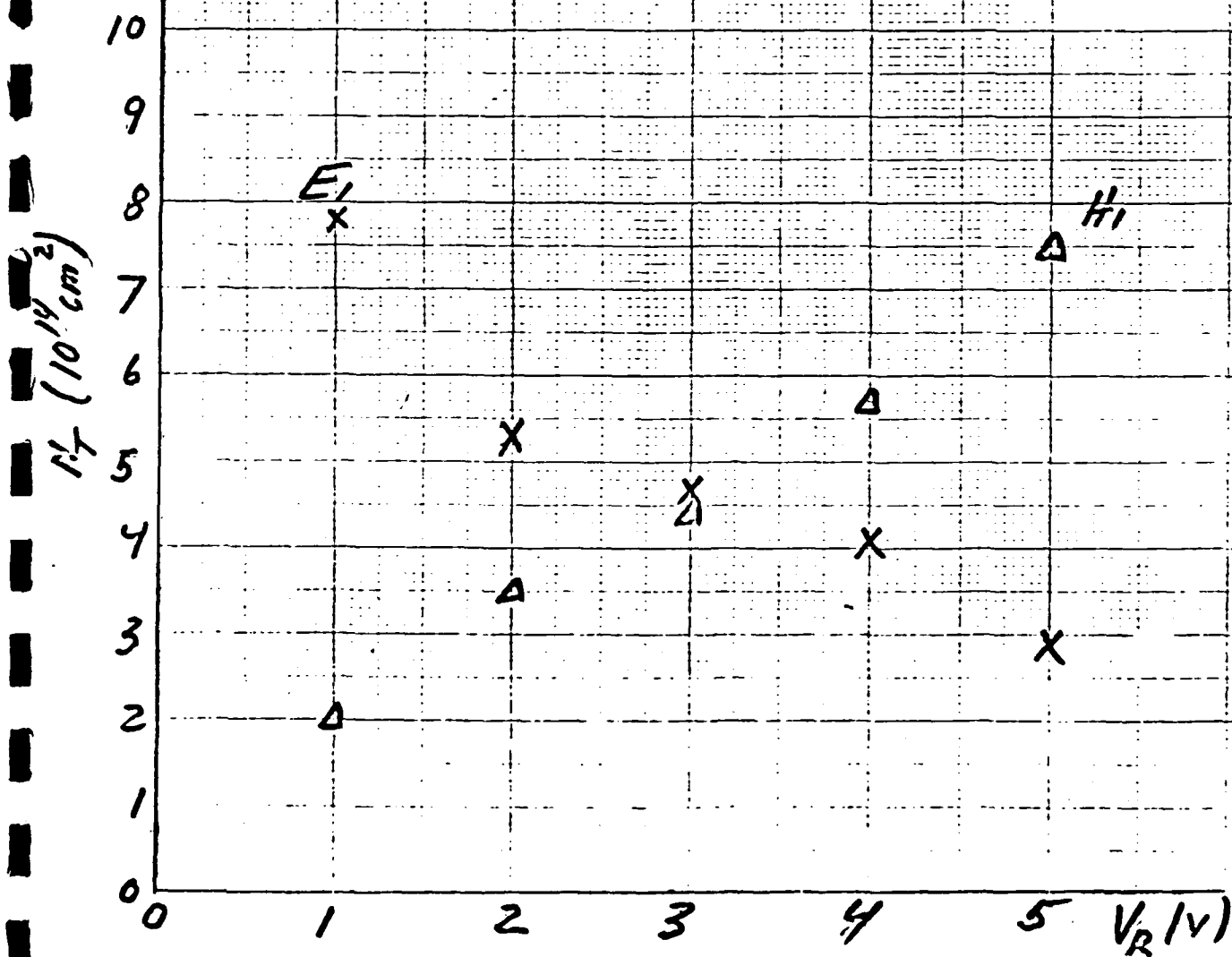


Figure 8

Bias dependence of trap density for H_1 and E_1

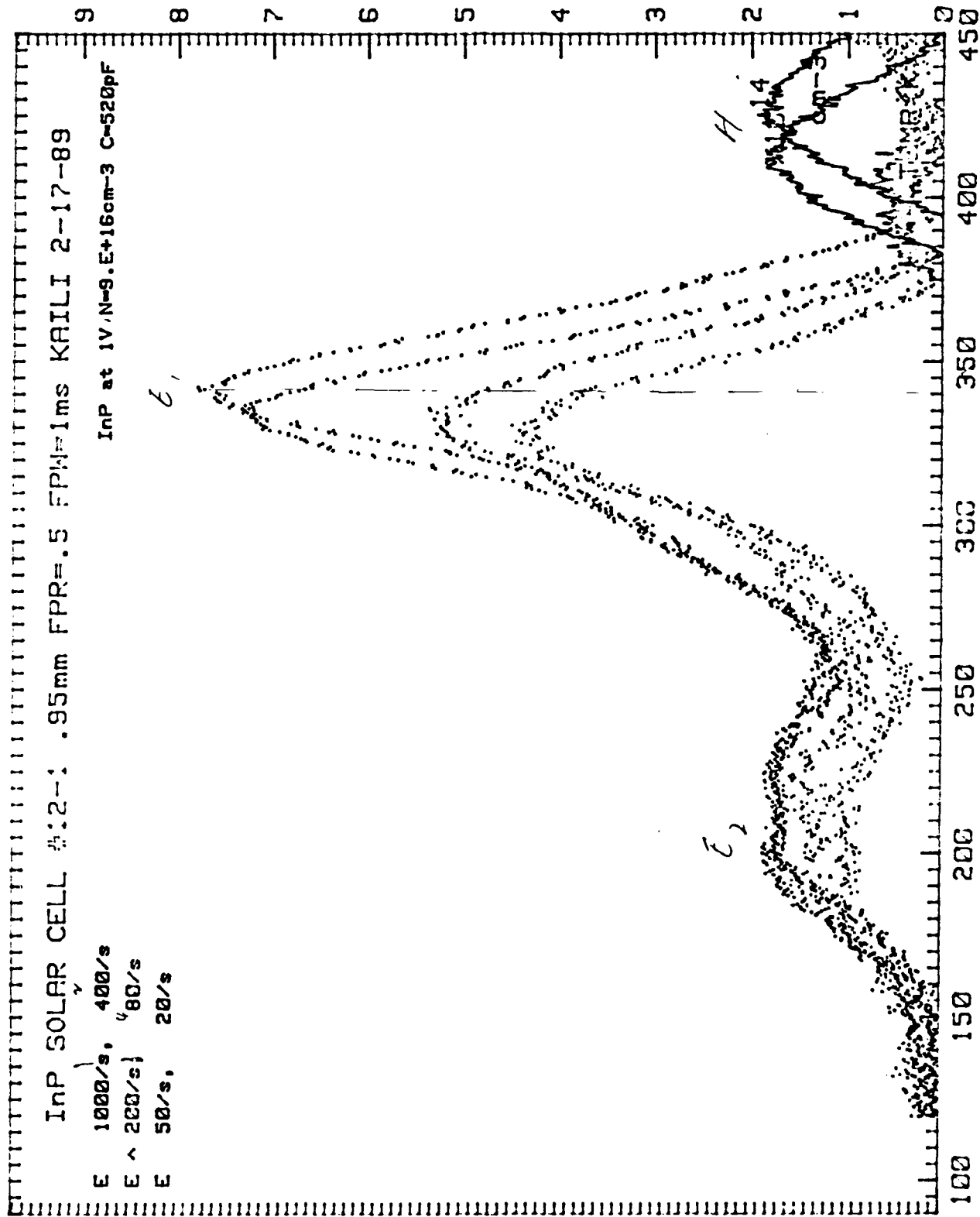


Figure 9 DLTS @ $V_R = -1V$

4.7.8.8.1
 H
 2004

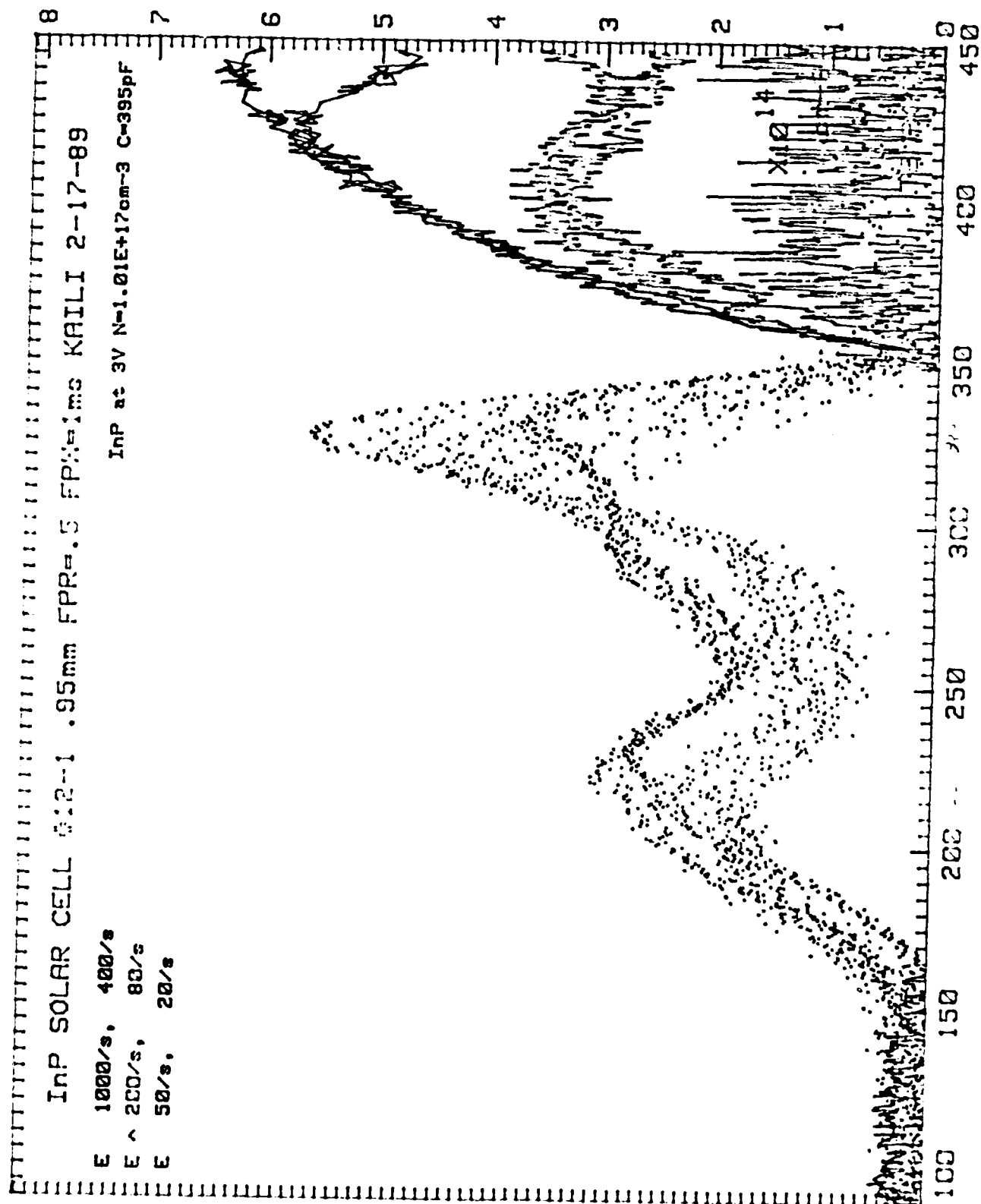
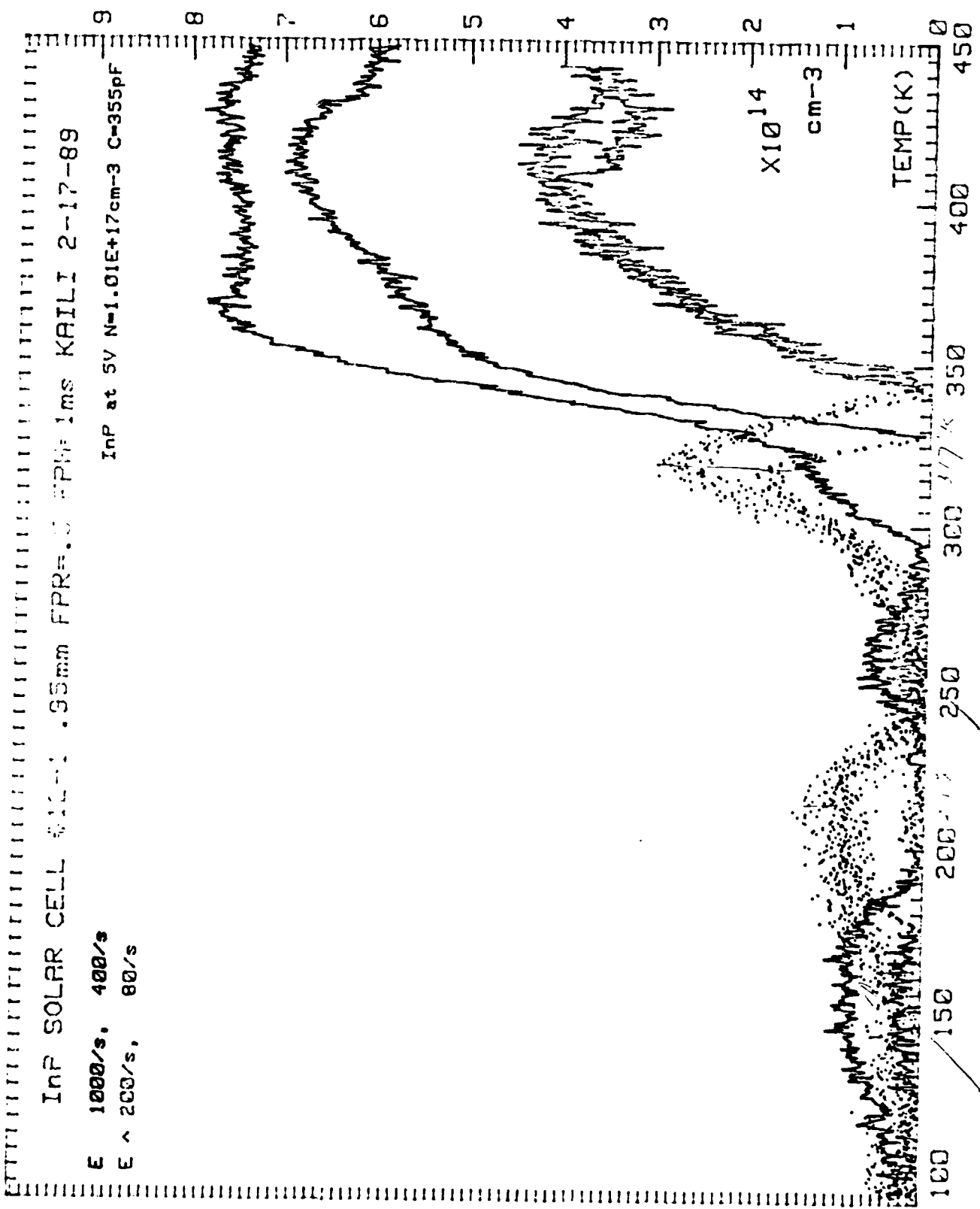


Figure 10 DLTS @ $V_R = -3V$



InP SOLAR CELL 612-1 .95mm FPR=.0 FPR=1ms KAILI 2-17-89

E 1000/s, 400/s
E ~ 200/s, 80/s

Figure 11 DLIS @ V_R = -5V

21
14-20-89
71 514

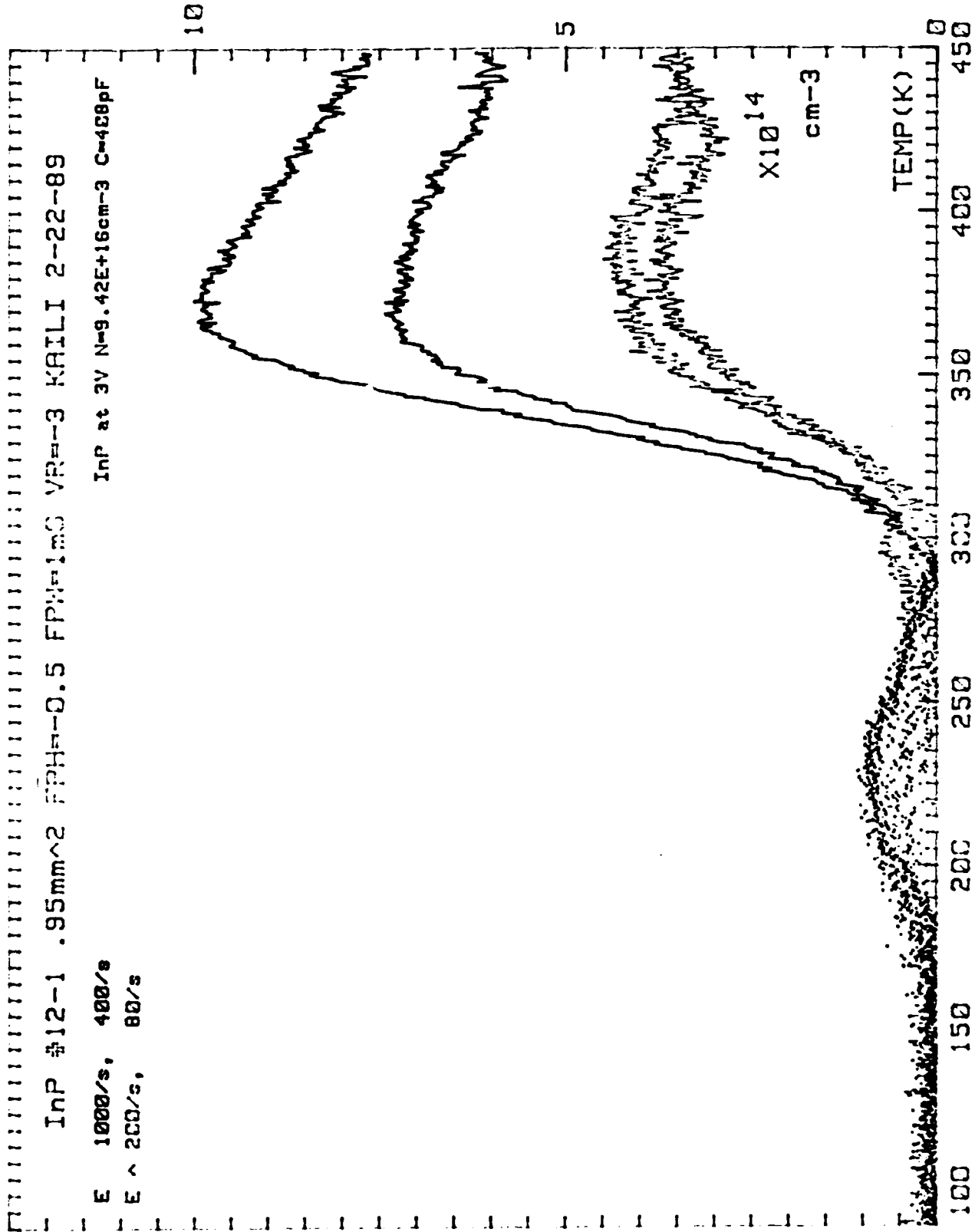


Figure 12 DLTS @ FPH - -0.5v

END

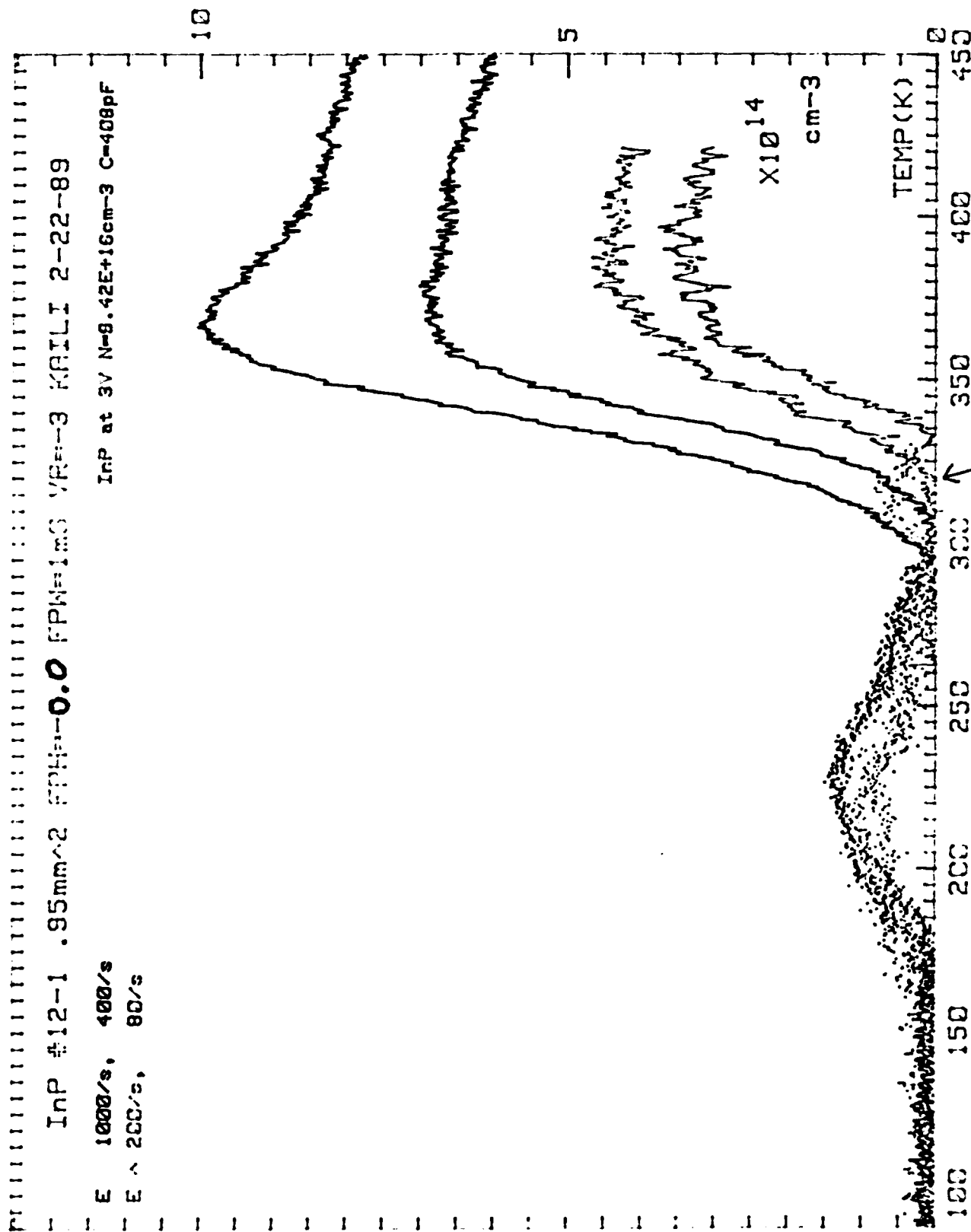


Figure 13 DLTS @ FPH = 0.0V P.W. = 80/s

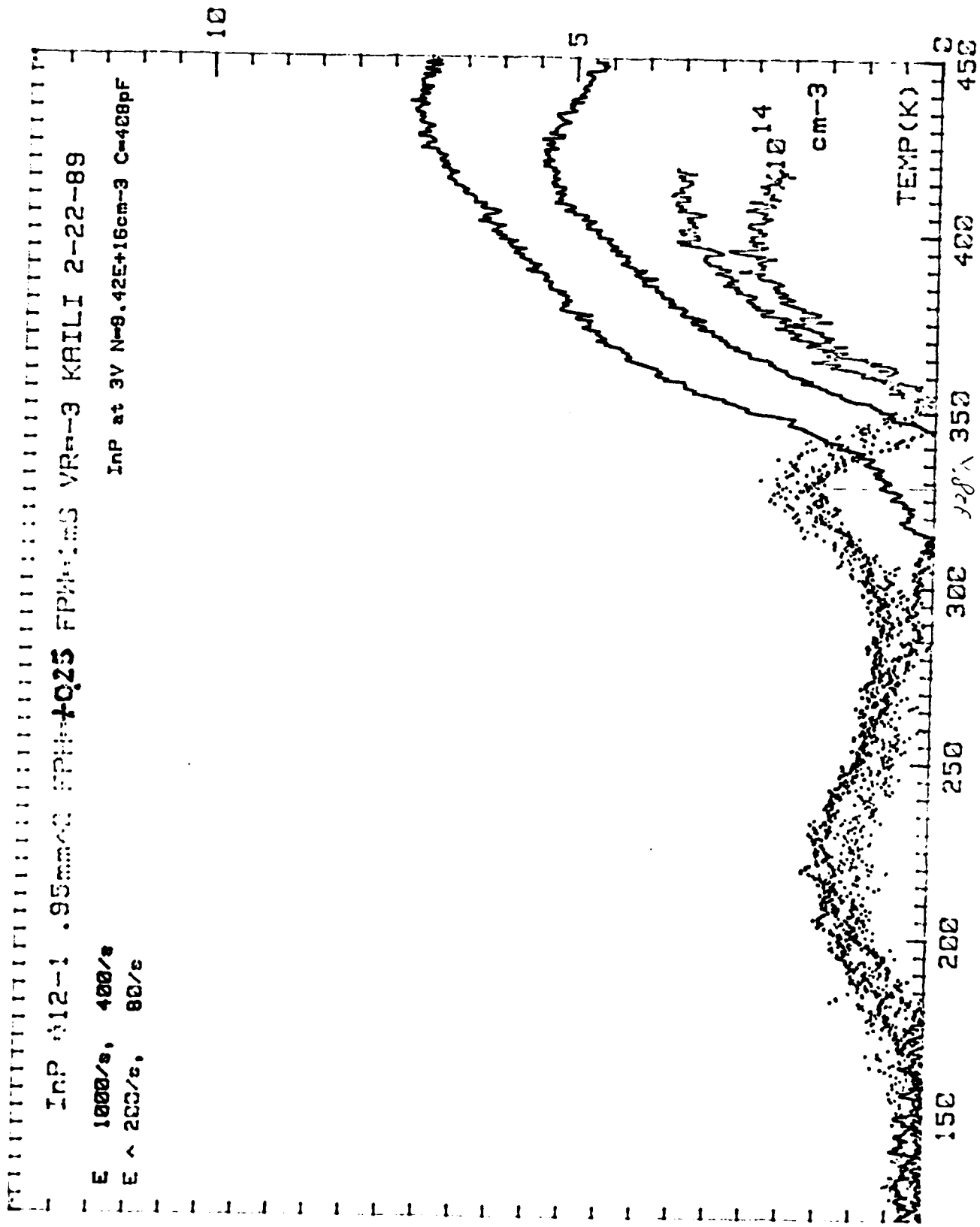


Figure 14 DLTS @ FPH - +0.25V

FPH = +0.25V

INP #12-1 .95mm^2 FPH=+0.75 FPH=1ms VR=3 KAILI 2-22-89

E 1000/s, 400/s

E ~ 200/s, 80/s

InP at 3V N=9.42E+16cm^-3 C=408pF

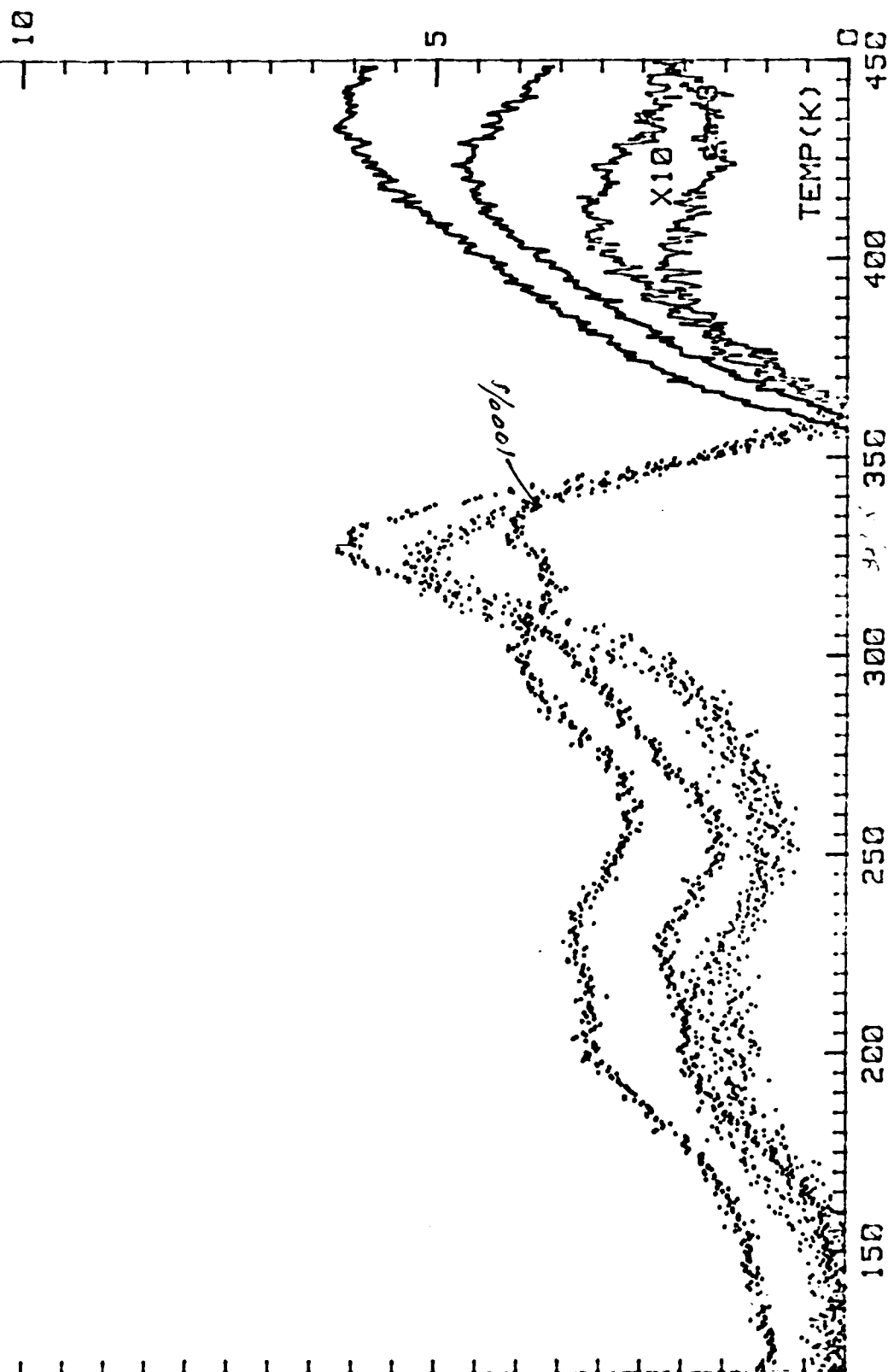


Figure 15

DLTS @ FPH = +0.75V

FPH=+0.75

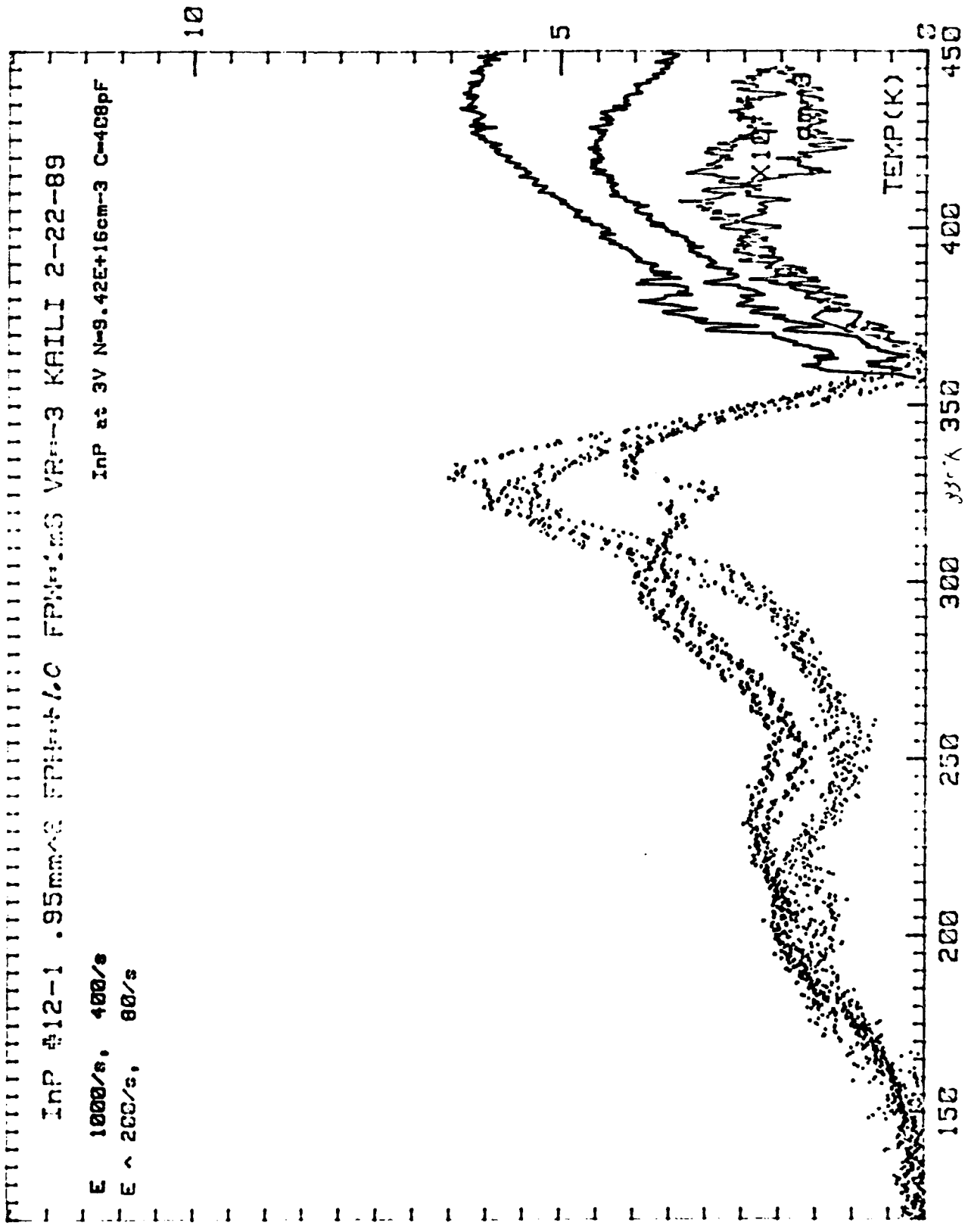


Figure 16 DLTS @ FPH = +1.0V

FPH = +1.0

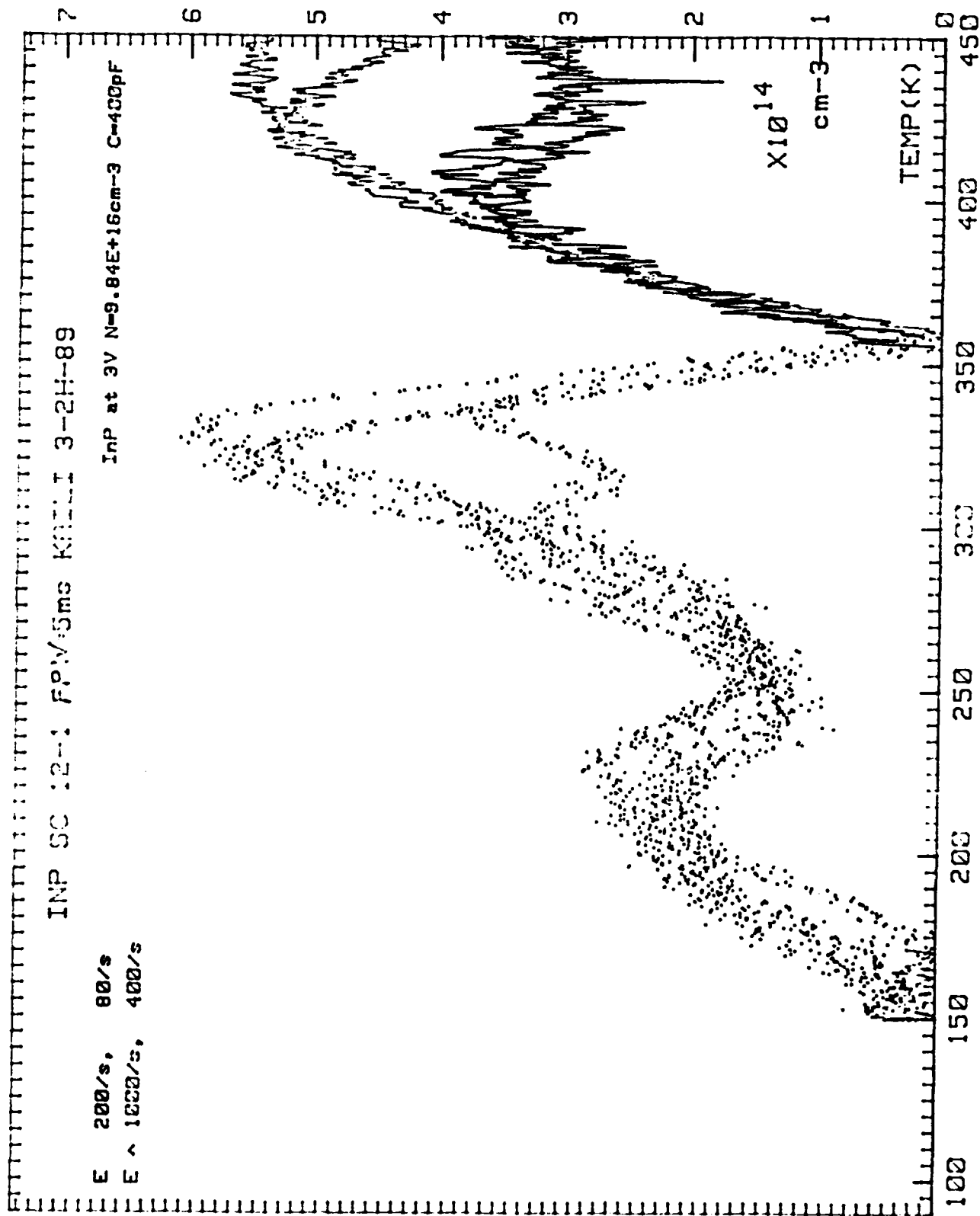


Figure 17 DLTS @ FPW - 5 ms

INP SOLAR CELL #12-1 .95mm FPR=.5 FPA=1ms KAILI 2-17-89

E 1000/s, 400/s
E ^ 200/s, 80/s
E 50/s, 20/s

InP at 3V N=1.01E+17cm-3 C=395pF

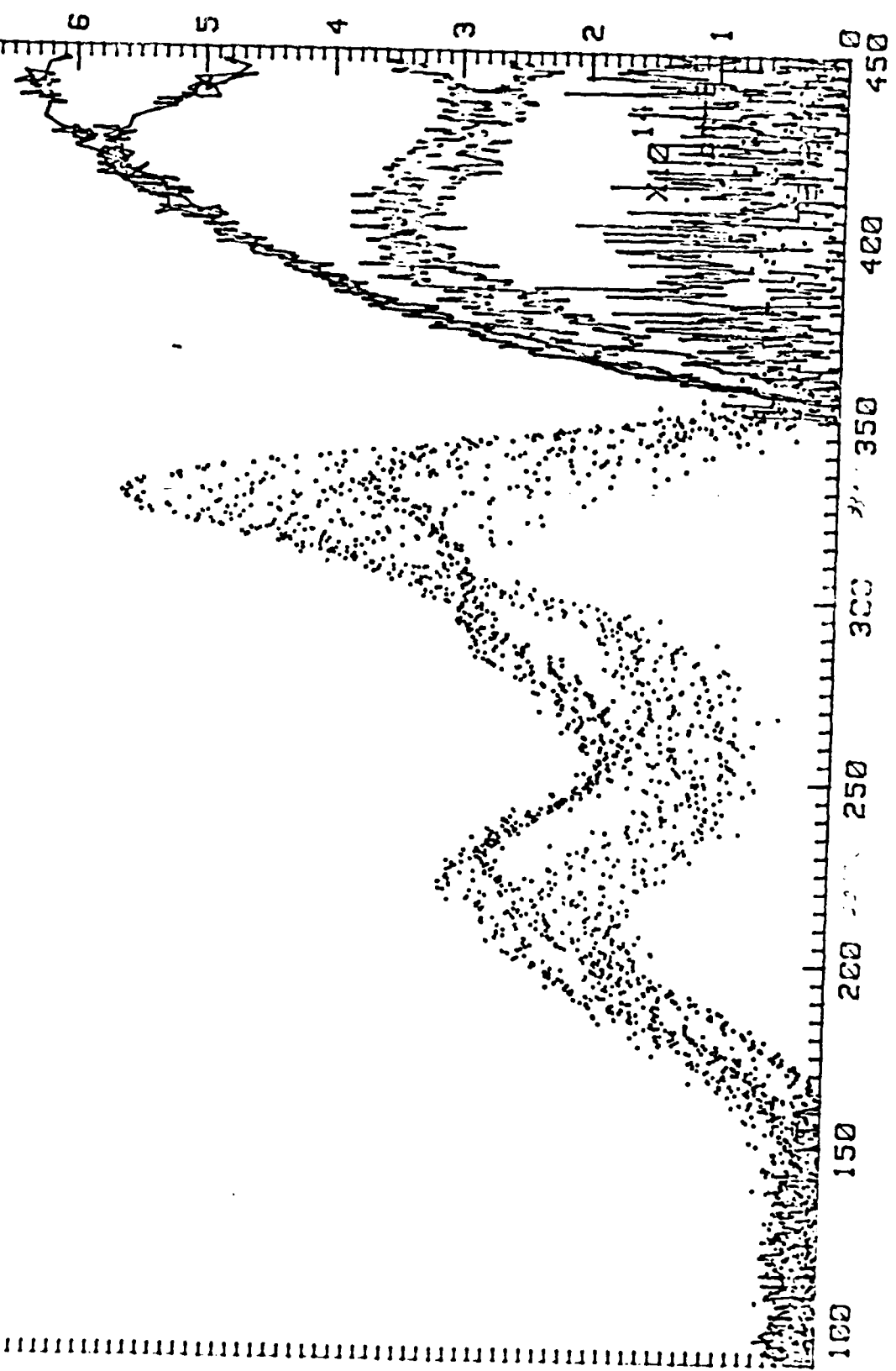


Figure 18 DLTS @ FPW - 1 ms

FP4=0.5V 500ms -30

INP 12-1 FPW=.5mS 3-2G-89

E 200/s, 80/s
E ~ 1000/s, 400/s

INP at 3V N=9.84E+16cm-3 C=483pF

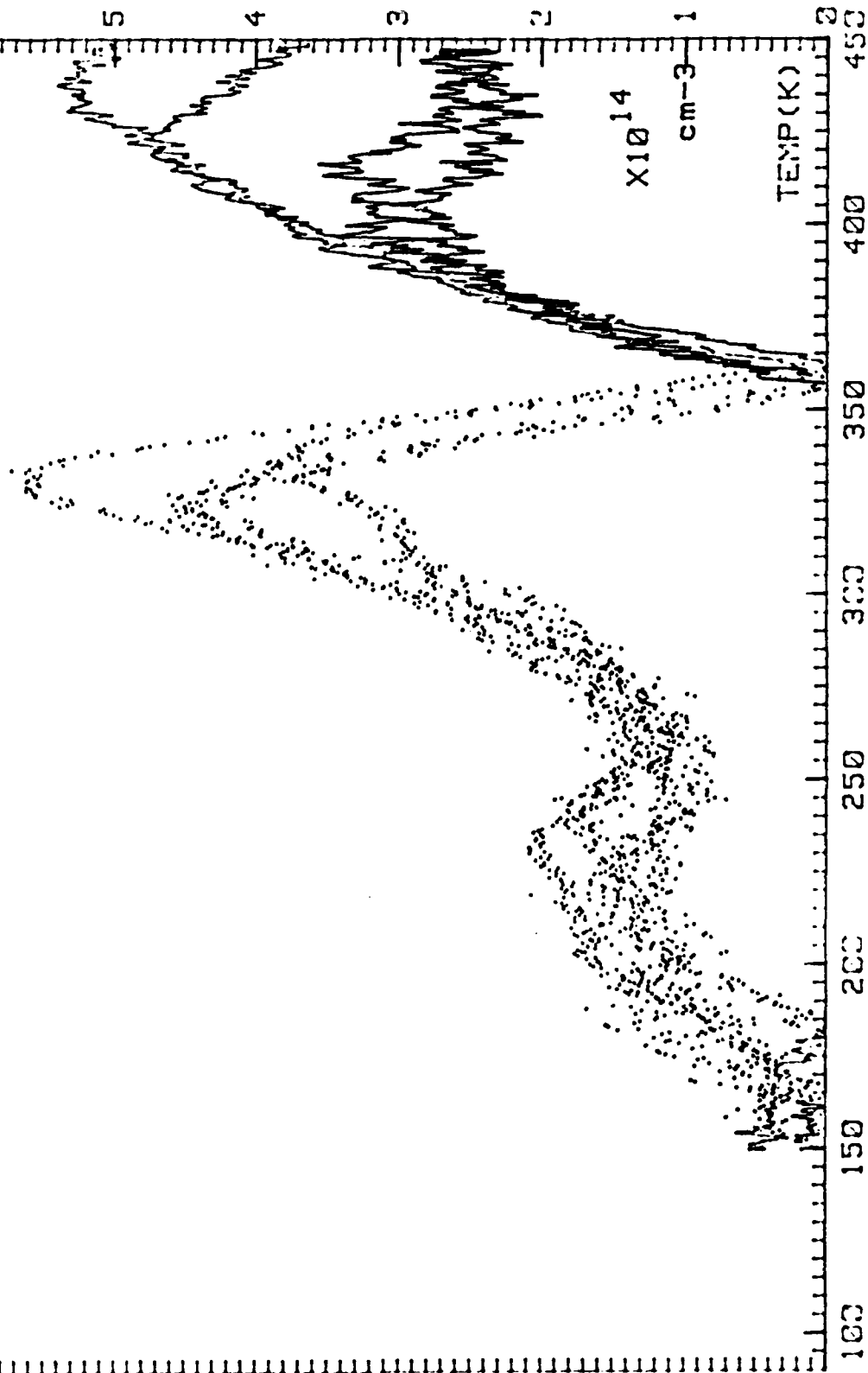


Figure 19 DLTS @ FWP - 0.5 ms

FPH = 0.5V, 0.1 ms

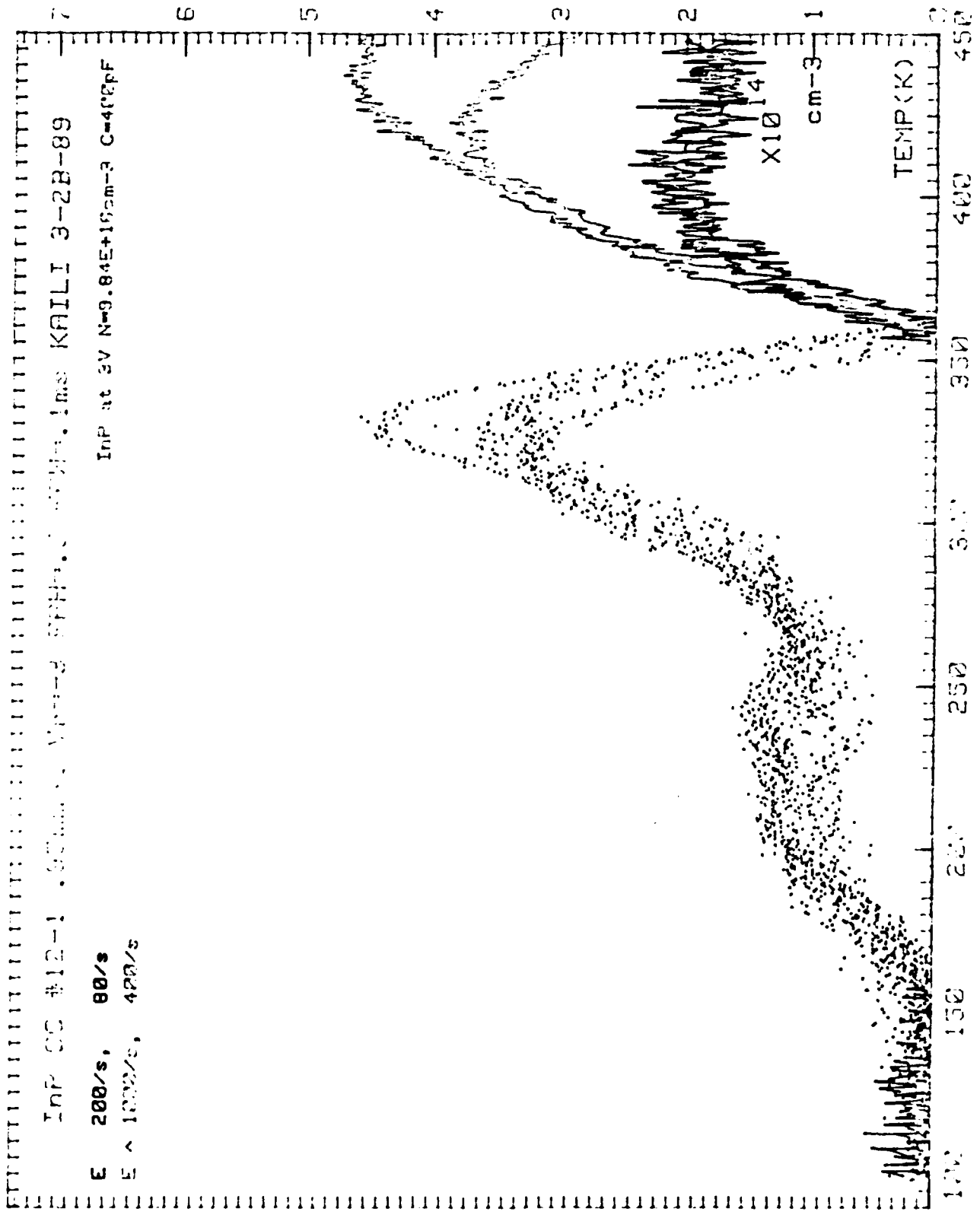


Figure 20 DLTS @ FWP - 0.1 ms

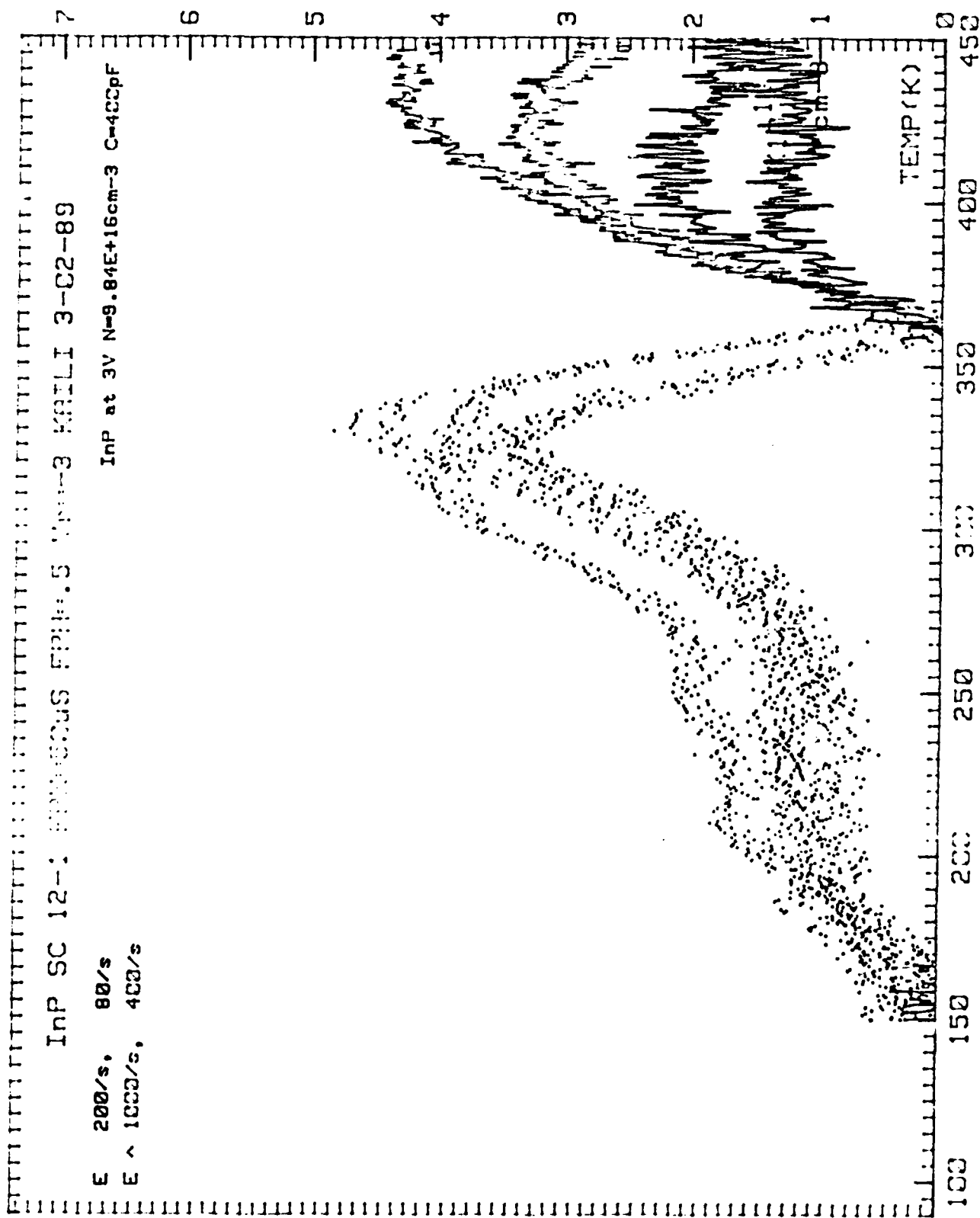


Figure 21 DLTS @ FPW - 50 μ s

FPH-005

10/5

InP SC 12-1 FPN=10us OTHERS SAME KAILIS-02F-89

E 200/s, 80/s
E ^ 1000/s, 400/s

InP at 3V N=9.84E+16cm-3 C=400pF

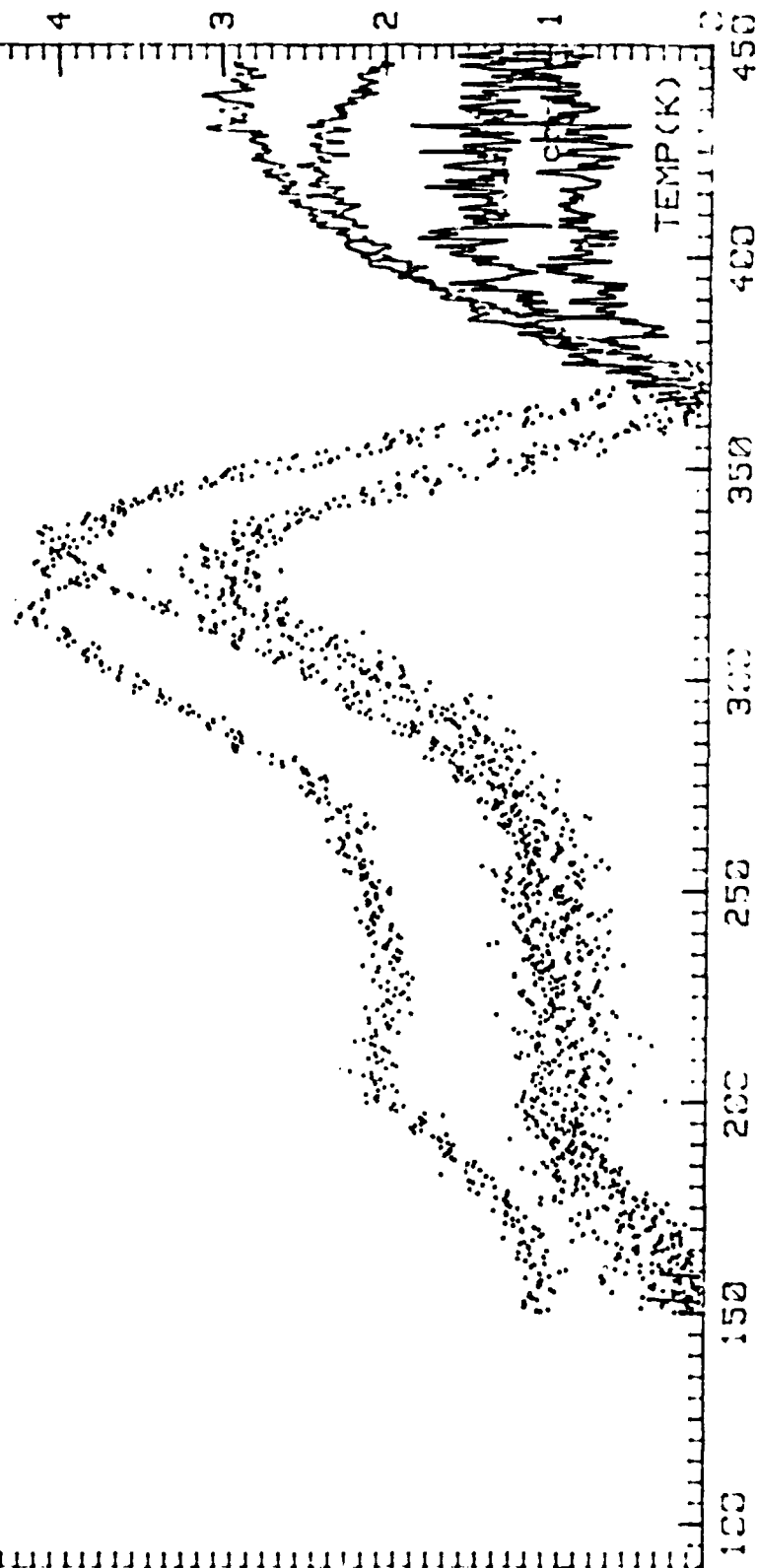


Figure 22 DLTS @ FPN = 10 μ s

InP SC 12-1 .95umx2 FFW=5us FFW=3 KAILI 3-C2-89

E 200/s, 80/s
E ^ 1000/s, 400/s

InP at 3V N=9.84E+16cm-3 C=402pF

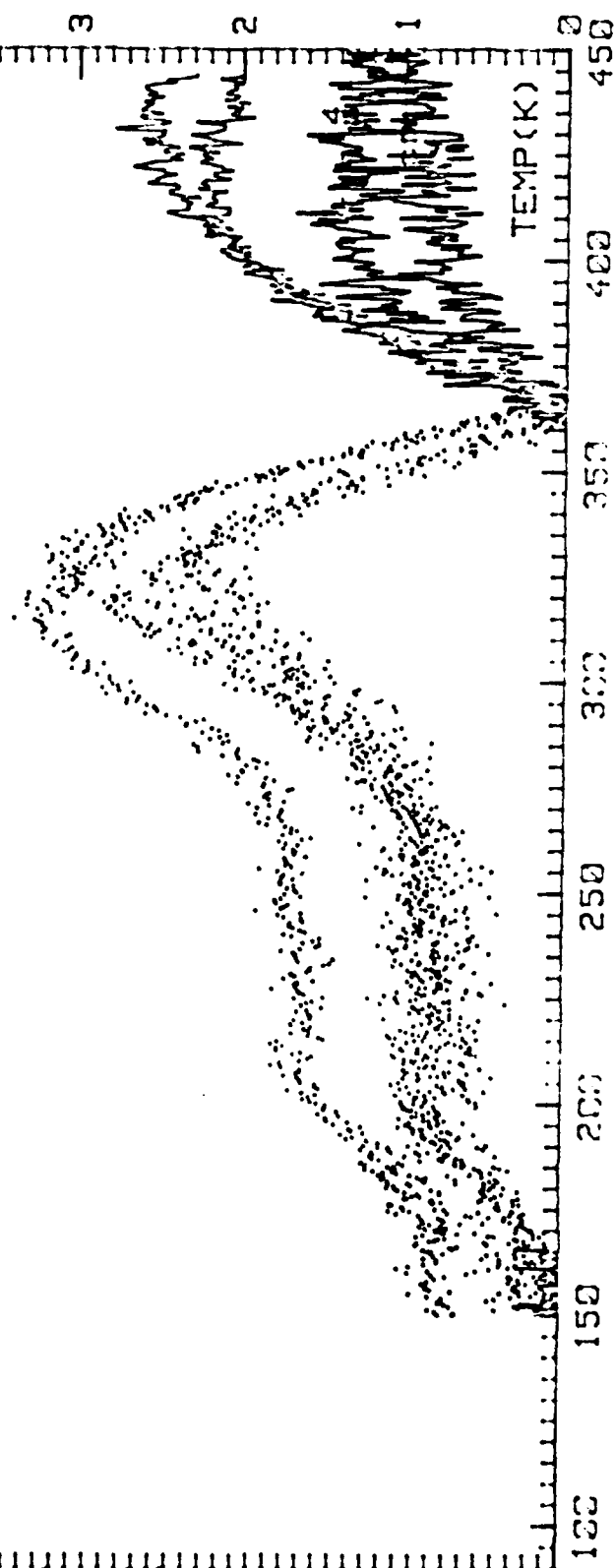


Figure 23 DLTS @ FFW - 5 μ s

InP SC 12-1 RRR=10.5 V_{pp}=3 KRLI 3-C2E-89

E 200/s, 80/s
E ~ 1000/s, 400/s

InP at 3V N=9.84E+16cm⁻³ C=433pF

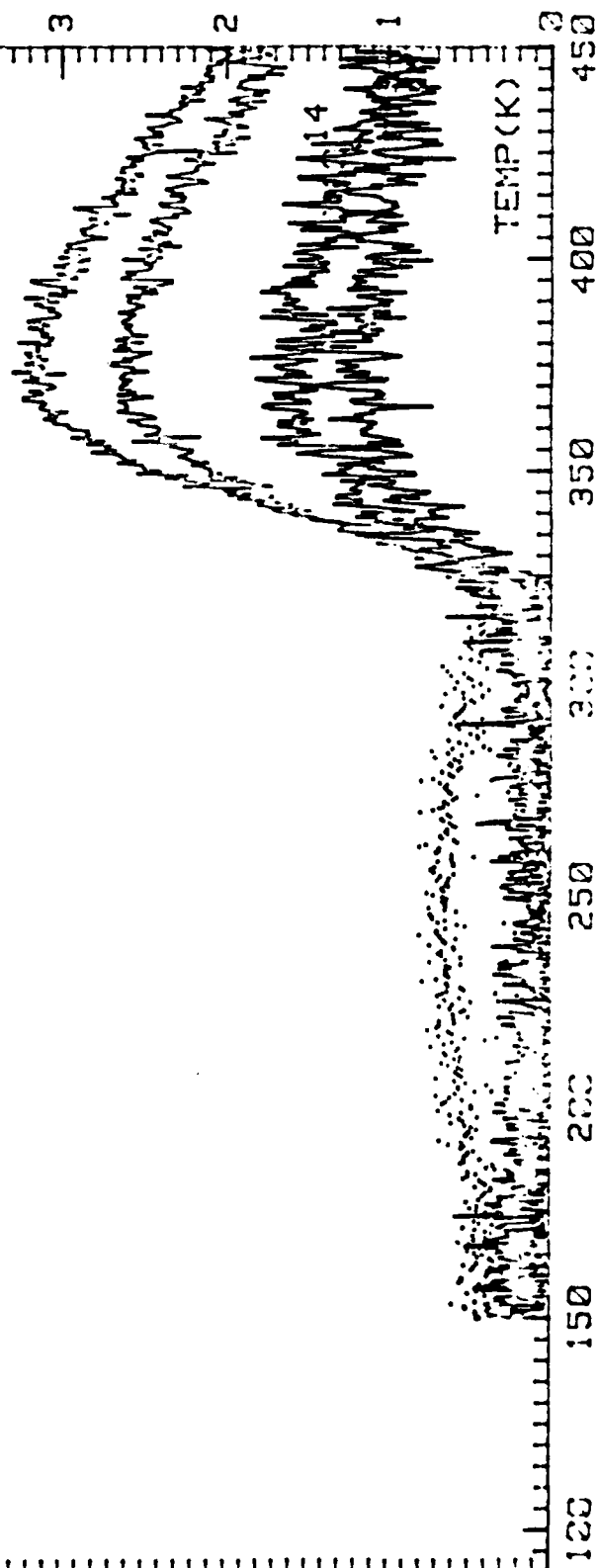


Figure 24 DLTS @ FPW - 1 μ s

Simulation $E_g = 0.35 \text{ eV}$, $C = 1, 9 \times 10^{-13} \text{ cm}^2$

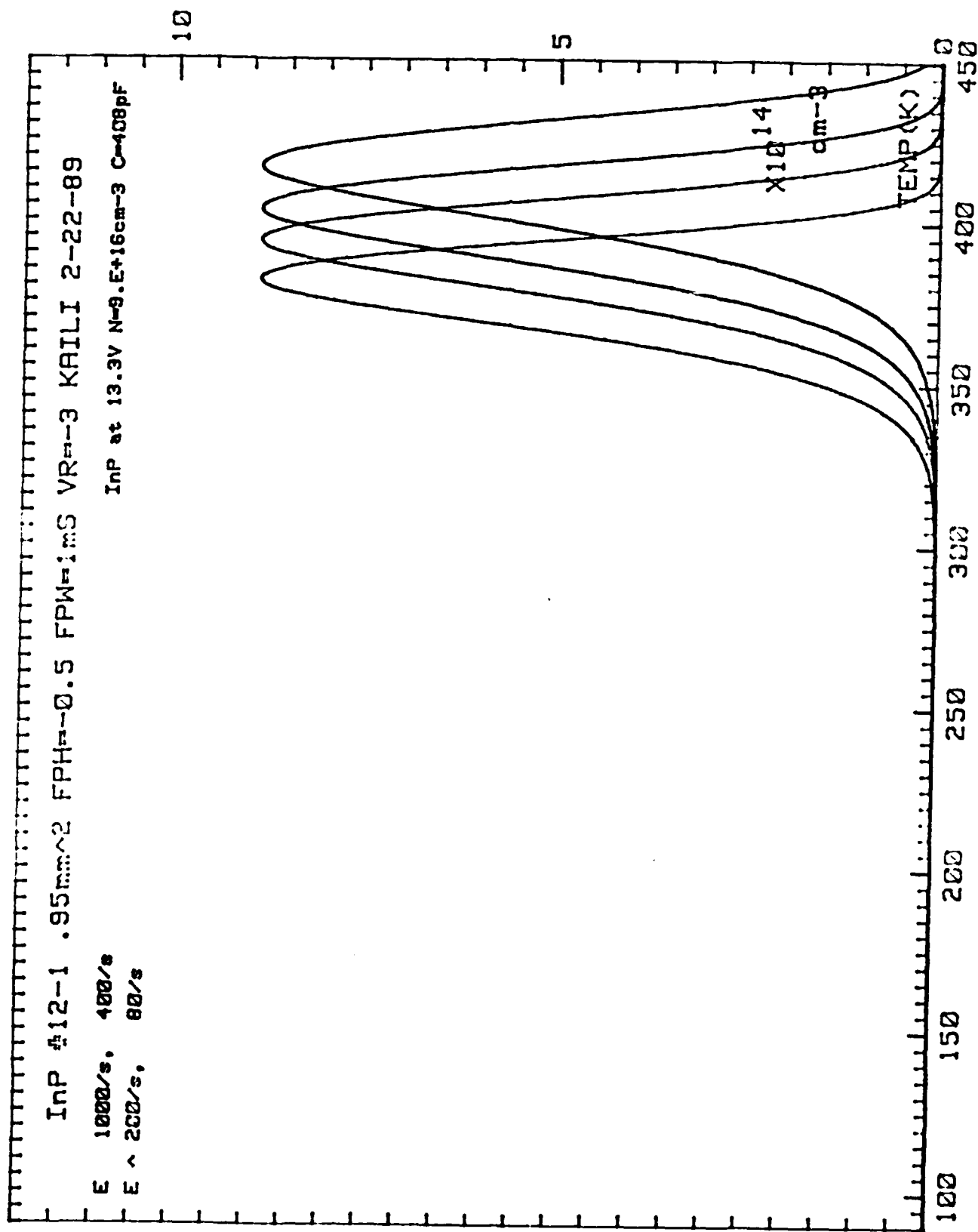


Figure 25 Computer Simulation of H₁

APPENDIX B

"Improvement of InP-GaAs-Si Quality by Thermal-Cycle Growth," S.M. Vernon, C.J. Keavney, E.D. Gagnon, N.H. Karam, M.M. Al-Jassim, N.M. Haegel, V.P. Mazzi, and C.R. Wie, Mater. Res. Soc. Symp. Proc. 198, 163 (1990).

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ABSTRACT

Single-crystal films of InP have been deposited on GaAs, GaAs-coated Si, and InP substrates by metalorganic chemical vapor deposition (MOCVD). Defect-reduction schemes involving various thermal annealing recipes have been developed and characterized. Material quality has been assessed by a variety of methods including transmission electron microscopy, X-ray rocking curve analysis, low-temperature photoluminescence, lifetime measurements, Hall-effect measurements, electrochemical profiling, and Nomarski microscopy. The use of either a thermal-cycle-growth or a thermal-cycle-annealing process leads to heteroepitaxial InP film quality which is significantly improved over that of its as-grown state, with the thermal-cycle growth appearing to be the more effective technique.

INTRODUCTION

InP-on-Si and InP-on-GaAs structures have potentially significant applications in the field of high-speed communications because such heteroepitaxial composites may enable the fabrication of monolithic optoelectronic integrated circuits. Wafers of InP-on-Si may be more well suited to optical-fiber communications than are GaAs-on-Si, since InP-based optical components [utilizing GaInAs(P)] can be designed to match the optimum wavelength regions of 1.3 and 1.55 μm . In order for these minority-carrier devices to function effectively, high-quality, low-defect, long-carrier-lifetime InP must be grown in this lattice-mismatched configuration.

In the GaAs-on-Si field, one technique that has shown a strong ability to reduce defects is the thermal-cycle growth (TCG) process, in which a repetitive growth, anneal, cooldown procedure is carried out, typically inside an MOCVD reactor [1]. The TCG of InP is more difficult than that of GaAs because the dissociation pressure of P over InP is much higher (by three orders of magnitude) than that of As over GaAs.

EXPERIMENTAL PROCEDURES

The structures studied consist of undoped InP films, 3-4 μm in thickness, deposited side-by-side onto GaAs, InP, and GaAs-coated Si substrates; the GaAs layer thickness on the Si substrates is 1-2 μm , an optimum range determined in previous experiments. All layers were grown by atmospheric-pressure MOCVD in a SPI-MO CVD 450 system; this reactor has a batch capacity of five two-inch-diameter wafers arranged in a vertical, rotating, barrel-geometry configuration. The details of the GaAs-on-Si growth have been described previously [2] and involve a three-step (bake out, nucleation, deposition) growth process. The InP growth is carried out at 600°C using PH_3 , either trimethylindium or ethyldimethylindium, and a palladium-purified hydrogen carrier gas.

The growth of the InP in some samples utilizes a TCG process which involves several repetitions of a deposition-anneal-cooldown procedure in which the temperature is brought from 600°C to 800°C in seven minutes, held at 800°C for two minutes, cooled to 250°C over 20 minutes, and then brought

back to the growth temperature (600°C) in 10 minutes for the cycle to be repeated. In other samples, a thermal-cycle annealing (TCA) procedure is employed, in which several anneal-cooldown cycles are all performed at the same point within the InP layer. For the TCA process, the temperature schedule is similar to the TCG-process values listed above, except that the anneal temperature is 875°C, and there is no deposition step between anneal-cooldown cycles. For all samples studied here (both TCA and TCG) a three-cycle process is used. Some GaAs-on-Si samples also utilize a TCG process for growth of the GaAs buffer layer [1]; here a maximum anneal temperature of approximately 900°C is used.

The defect structure and density of the samples is studied by transmission electron microscopy (TEM), using both planview and cross-sectional analyses. Crystalline quality is also assessed by double-crystal X-ray rocking curve analysis, while Nomarski microscopy is used to characterize the surface morphology. The optical properties of samples have been studied by low-temperature photoluminescence (PL) and minority-carrier lifetimes are measured by room-temperature PL decay. Electrical characterization results are obtained by Hall-effect and electrochemical C-V measurements using a Polaron semiconductor profile plotter.

RESULTS

Transmission Electron Microscopy

Analysis by TEM has been a major characterization tool used in comparing the quality of various samples. Figure 1 shows representative cross-sectional TEM micrographs of InP on GaAs for three different film-growth methods. It can be seen that the TCG process significantly reduces the dislocation density from that of the as-grown layer by causing many of the dislocations to form closed loops near the heterointerface. Similar effects have been seen in GaAs-on-Si studies [1]. Figure 1 also shows that the effectiveness of the TCA process is intermediate between that of the TCG and the as-grown films.

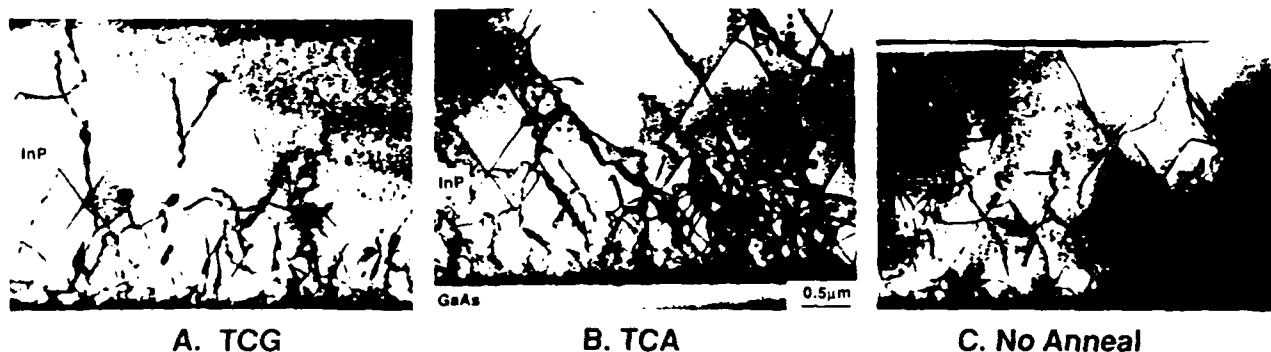


FIGURE 1. CROSS-SECTIONAL TEMs OF InP ON GaAs.

For InP on GaAs on Si films, similar trends have been observed. Table 1 is a summary of the TEM results; these data indicate that (1) both TCG and TCA processes lead to defect reduction in the InP layer, (2) TCG appears to be more effective than TCA, (3) the use of the TCG process in the GaAs buffer layer on Si substrates also helps to reduce the dislocation density, and (4) that InP on TCG GaAs/Si has less defects than InP grown on bulk GaAs wafers.

TABLE 1. DISLOCATION DENSITY IN HETEROEPITAXIAL InP FILMS
VERSUS GROWTH METHOD AND SUBSTRATE TYPE.

InP Layer	Substrate Type		
	GaAs	GaAs/Si	TCG GaAs/Si
As Grown	3.9×10^8	3.5×10^8	2.5×10^8
TCA	3.0×10^8	--	2.0×10^8
TCG	1.4×10^8	2.5×10^8	9.0×10^7

Note: Values are dislocation density in defects per cm^2 , determined by TEM.

Figure 2 shows a representative planview TEM comparison of InP and TCG InP, both grown on TCG GaAs/Si substrates. It has been found, and is evident in this figure, that the TCG InP process greatly reduces the density of stacking faults, usually to a level below that measurable by TEM.



FIGURE 2. PLANVIEW TEMs OF InP-GaAs-Si SAMPLES.

The dislocation values in Table 1 are deduced by examining many TEM micrographs and the differences shown are believed to be significant. Although the factor of two to four reduction in dislocation density achieved is promising and points to a direction for further study, a reduction factor of $10^2 - 10^4$ is really needed in order to obtain very-high-quality material.

Double-Crystal X-Ray Rocking Curve Analysis

Table 2 summarizes the results of X-ray rocking curve analyses of the InP-GaAs-Si structures, and an X-ray rocking curve showing peaks for all three materials is shown in Figure 3. From the full-width half-maximum (FWHM) data of Table 2, the following trends may be noted: (1) the TCG process significantly improves the InP crystallinity, while the TCA process has no major effect, (2) for each InP growth type, the GaAs and TCG GaAs/Si produce similar InP material quality, while the regular GaAs/Si leads to inferior layers.

It has also been found in this study that the GaAs buffer layers sandwiched between the InP and Si have lower FWHM than our normal GaAs/Si samples. This is believed to be due to the reduced strain in the GaAs buffer layers "capped" by the InP material, since the coefficient of thermal expansion of InP is less than that of GaAs and more than that of Si. The InP-capped GaAs-on-Si layers analyzed here have FWHM values as low as 97 arc-seconds as compared to 125 arc-seconds for our typical TCG GaAs on Si.

TABLE 2. DOUBLE CRYSTAL X-RAY ROCKING CURVE RESULTS FOR HETEROEPI-TAXIAL InP FILMS VERSUS GROWTH METHOD AND SUBSTRATE TYPE.

InP Layer	Substrate Type		
	GaAs	GaAs/Si	TCG GaAs/Si
As Grown	270	410	286
TCA	279	--	266
TCG	179	273	194

Note: Values in table are full-width half-maximum (FWHM) data in arc-seconds

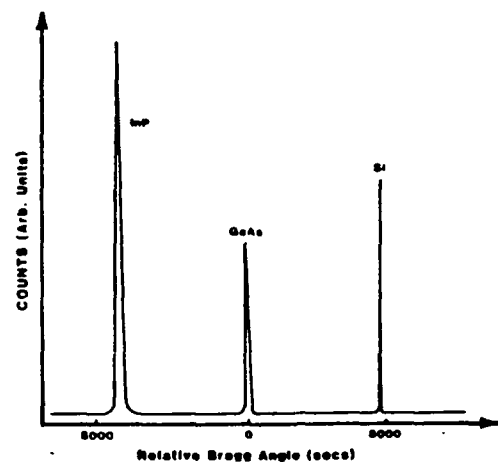


FIGURE 3. TYPICAL DOUBLE-CRYSTAL X-RAY ROCKING CURVE DATA FOR AN InP-GaAs-Si SAMPLE.

Surface Morphology

Figure 4 shows Nomarski micrographs of InP-GaAs-Si structures using the InP TCG and TCA processes. The InP heteroepitaxial films grown without annealing look quite similar to those with the TCA treatment. The TCG samples appear to have a smoother, more "rounded"-type surface, which is very shiny and specular to the eye.

Hall-Effect Measurements

Semi-insulating substrates of GaAs and InP were used to compare the Hall mobilities of InP layers, 3-4 μm thick, grown by our three processes. The results are summarized in Table 3. It is seen here that for the TCG samples, and to a lesser extent the TCA samples, have mobility values on GaAs that are only about a factor of two lower than those obtained on the homoepitaxial structures.

Dopant Profile Analysis

The InP on GaAs on Si samples were studied by electrochemical profiling using a Polaron instrument. The background doping level in the InP layer appears to be approximately $N = 2 \times 10^{15} \text{ cm}^{-3}$, regardless of growth-anneal process. In most samples a dopant spike is seen at the GaAs-InP interface, apparently indicating that Si atoms are being getterred at this heavily

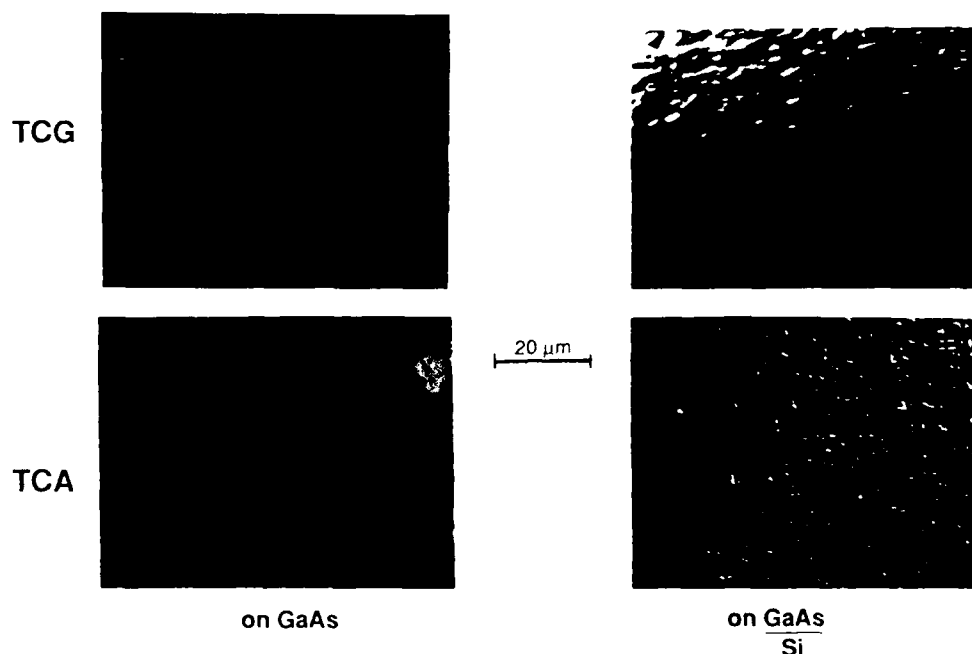


FIGURE 4. SURFACE MORPHOLOGY OF HETEROEPITAXIAL InP FILMS BY NOMARSKI MICROSCOPY.

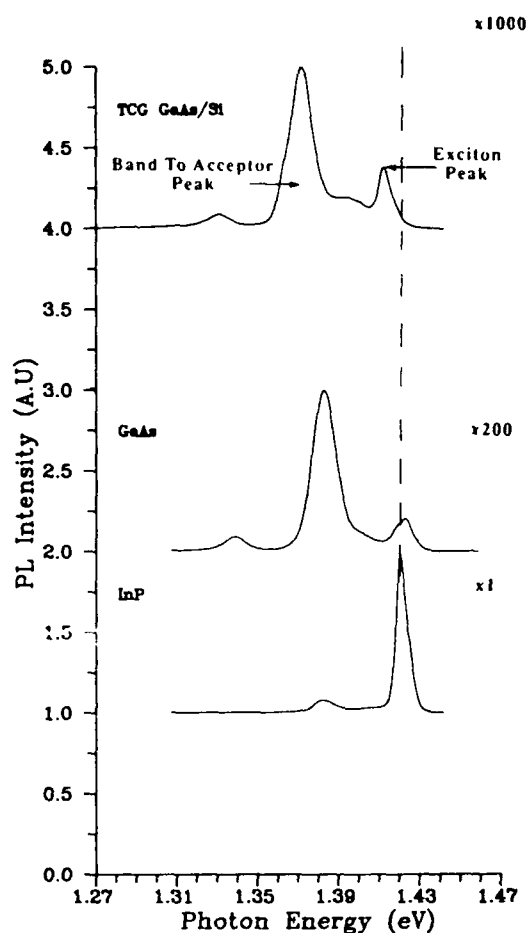
TABLE 3. HALL MOBILITY IN InP LAYERS AT 300K.

InP Anneal	300K Mobility ($\text{cm}^2/\text{V-sec}$)		Mobility on GaAs		$N(\text{cm}^{-2})$
	GaAs	Substrate InP	Mobility on GaAs	Mobility on InP	
TCG	1920	3180	0.60		1×10^{15}
TCA	1750	2890	0.61		2×10^{15}
None	1440	4150	0.35		6×10^{14}
77K Mobility ($\text{cm}^2/\text{V-sec}$)					
TCG	23000	47200	0.49		6×10^{14}
TCA	8800	25300	0.35		1×10^{15}
None	8700	72000	0.12		5×10^{14}

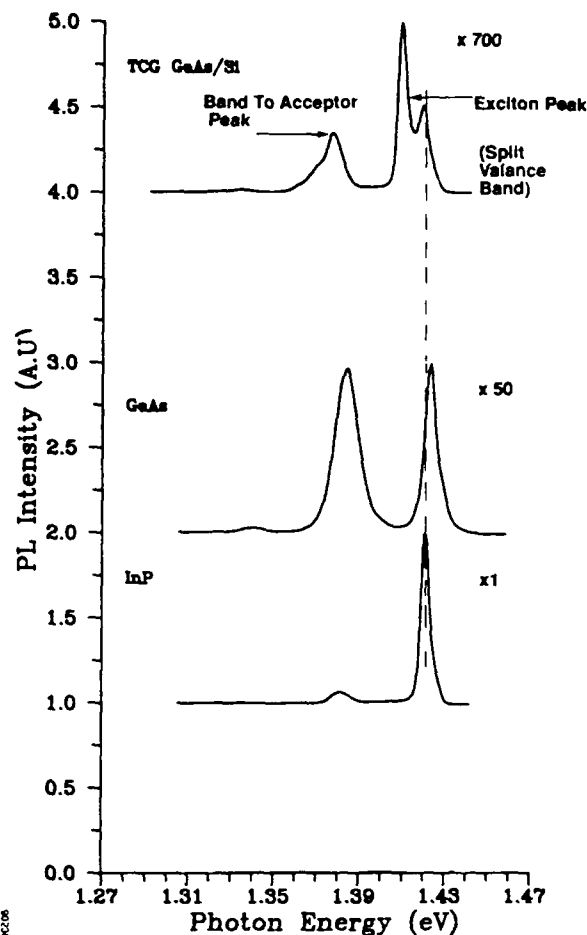
defected region. It is possible, however, that this spike is a Polaron artifact, such as charge accumulation at the interface; more study is needed to answer this question conclusively.

Optical Characterization

Low-temperature photoluminescence (PL) has been used to analyze our InP layers. Figure 5 shows a comparison of the as-grown and TCG InP data; the TCA samples have PL spectra quite similar to the TCG data, although the exciton splitting is not as pronounced. A number of trends are evident in the spectra of Figure 5: (1) TCG leads to an increased height of the near-bandedge exciton peak as compared to the unannealed InP, (2) the stress from the thermal-expansion mismatch between InP and Si ($2.2 \times 10^{-6} \text{ K}^{-1}$) causes



(a)



(b)

FIGURE 5. PHOTOLUMINESCENCE OF InP FILMS AT 4.2 K. (a) No anneal, (b) With TCG.

the exciton peak to split and to shift to lower energy, while the opposite-sign stress from the thermal-expansion mismatch between InP and GaAs ($-2.3 \times 10^{-6} \text{K}^{-1}$) causes the peak to move to higher energy, (3) for the TCG material, the sharpness of the exciton peaks of the heteroepitaxial material is similar to that of the InP homoepitaxial layers, both having a FWHM of approximately 5 meV. The ratio of the exciton peak height to the band-to-acceptor peak height is an indication of the minority-carrier lifetime of the material, with higher ratios implying higher lifetimes. Here again it is obvious that the annealed samples are significantly improved over the as-grown material.

Minority-carrier lifetimes were also measured at room temperature by a PL decay technique using pulsed dye-laser excitation and time-correlated photon counting; the system has been described in detail elsewhere [3]. The data are summarized in Table 4 and confirm the trends of the PL data discussed above. The lack of a surface passivation on the InP causes the absolute values of these data to be highly questionable, but comparisons between samples should still be valid.

TABLE 4. MINORITY-CARRIER LIFETIMES IN InP LAYERS BY PL DECAY.

InP Anneal	GaAs	GaAs/Si	Substrate Type	
			TCG GaAs/Si	InP
TCG	0.59	0.55	0.75	2.9
TCA	0.73	--	0.69	1.9
None	0.42	0.48	0.46	3.7

Values in table are lifetime in nanoseconds. All InP layers are undoped at $N = 0.4-2.0 \times 10^{15} \text{ cm}^{-3}$.

SUMMARY

Heteroepitaxial structures of InP-GaAs-Si may be useful for monolithic integration of optical and electronic function. High-quality InP films have been grown by a large-area MOCVD process on both GaAs and Si substrates. The development of InP in-situ annealing processes has led to superior material properties as determined by structural, electrical, and optical analyses, with InP quality being similar on both GaAs and GaAs-coated Si substrates. By most criteria, the TCG process gives the best results, although the TCA material is in some respects comparable and eliminates the need to use large flows of PH_3 .

The support of this work by SDIO/IST through the Army Research Office and by the NASA Lewis Research Center is gratefully acknowledged.

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