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Development of a Shadow Mask for Sputtering Platinum onto Ferroelectric-Coated Substrates

by Judith T. McCullen
Bernard J. Rod
Robert Reams

U.S. Army Laboratory Command
Harry Diamond Laboratories
Adelphi, MD 20783-1197

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Judith T. McCullen, Bernard J. Rod, and Robert Reams

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13. ABSTRACT (Maximum 200 words)

The Army has a continuing requirement for nonvolatile memories in which critical information placed in system memory is available after the system is reactivated following storage or power down. To meet the needs of future increases in memory size and a requirement for nonvolatile random access memory devices, ferroelectric thin film material research and development has become a priority. Ferroelectric nonvolatile memories combine the advantages of CMOS circuitry, small size, and low power with the ability to retain information in a power-off condition over long periods of time (years). In support of the ferroelectric memory program, a project was undertaken to make a shadow mask for sputter-depositing platinum electrodes with microfabrication techniques to create very small shaped openings through a silicon wafer. The mask is designed so that electrode material such as platinum sputtered through the mask onto a ferroelectric thin film substrate creates small well-defined capacitors that can then be used for extensive ferroelectric material research.

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1. Introduction

Ferroelectric thin films are being investigated as a nonvolatile storage material for fabricating high-density random access memory devices that are able to retain information over long periods without applied power. Memory cell size reduction is an essential part of achieving the substantial increase in the number of memory cells that is projected to be needed for the future designs required by sophisticated Army electronic systems. This reduction in size requires a ferroelectric material that possesses a significantly higher dielectric constant and dielectric reliability [1] than is presently available with the standard silicon dioxide dielectric layers, which in turn has resulted in an increased interest in ferroelectric materials research. Although there are over 1400 known (bulk) ferroelectric materials, most of these exhibit characteristics that are not conducive to use in fabricating integrated circuits [2].

Research into ferroelectric materials is made easier by the evaluation of capacitors fabricated with sol gel spin on PZT (lead zirconate titanate) thin film ferroelectric material. Ferroelectric materials by definition are polar structural phase materials that change phase at a characteristic transition temperature, accounting for spontaneous polarization reversal capabilities and therefore large storage-charge densities [1]. Detailed time-dependent measurements help clarify the causes of degradation of PZT properties due to fatigue and aging to determine the efficacy of using sol gel spin on PZT material for producing a ferroelectric device chip. The ferroelectric device chip will then be fabricated for radiation and reliability testing, and the results will be used to further aid in developing nonvolatile random access memory devices for Army systems.

Ferroelectric capacitors are fabricated with platinum as the top electrode, PZT as the dielectric, and platinum under the PZT to form the bottom plate (fig. 1). To thoroughly evaluate the various PZT materials available, the top platinum has been defined through two different techniques. The first technique involves chemically etching platinum dots after the whole substrate is covered with a platinum film using a selected deposition process (sputtering). The second method requires making a shadow mask whereby the solid mask with patterned windows rests on the substrate and the platinum is then sputtered onto the PZT material through the patterned windows. The second approach is a simple method to create test samples on a quick turnaround (QTA) basis. For our research, the mask was fabricated from a silicon wafer. The process used to develop this shadow mask is the topic of discussion in this report.

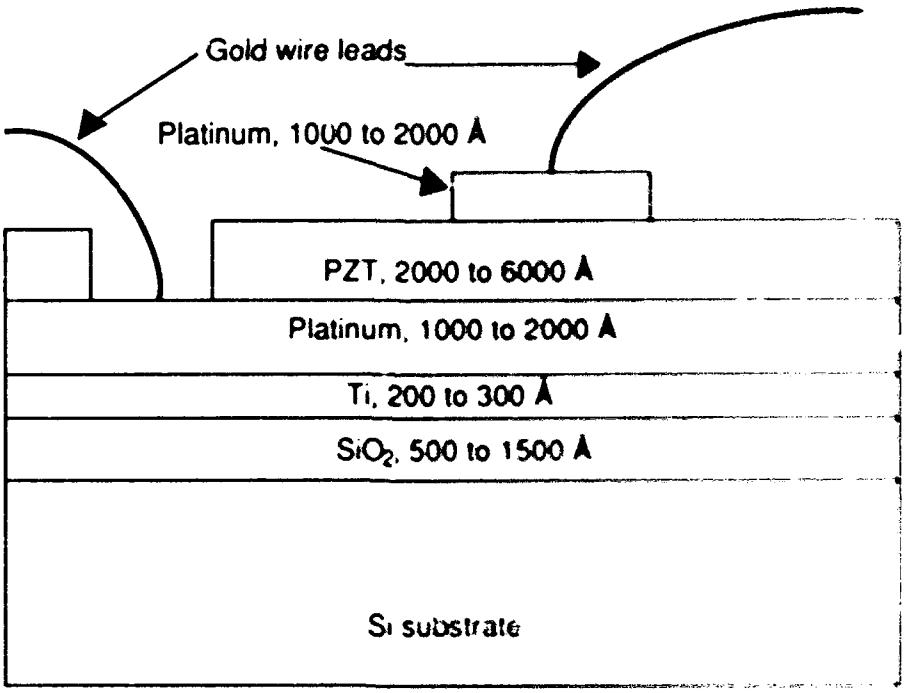

Figure 1. Cross-section of PZT capacitor.

2. Factors Considered in Fabricating Shadow Mask

The goal of this work was to etch patterned holes through a silicon wafer to create a shadow mask through which platinum would be sputtered onto a PZT-coated substrate. In silicon wafers, <100> crystal orientation will etch at a much higher rate than <111>, a differential of almost 100 to 1 with the potassium hydroxide etch mixture considered here [3]. Thus we see that silicon etches along the crystal plane, depending upon the etch used and the crystal orientation of a particular wafer, and not necessarily perpendicularly through the depth of the wafer (fig. 2 and 3 and fig. 4 (sect. 3)). Therefore the etch and the crystal orientation angle must be used to calculate the surface pattern hole size needed to achieve the desired 127-μm-diam holes in the wafer required by this experiment. The approach here was to etch through <100> crystal orientation wafers, both 51-μm thick, with a diameter of 3.175 cm. Also used were wafers with a thickness of 279 μm and a diameter of 5.08 cm (since these were on hand) to determine which would make a better mask.

Three silicon etches were considered for etching through the silicon: a fast-etch mixture of nitric acid, acetic acid, and hydrofluoric acid; a potassium hydroxide etch mixture of potassium hydroxide, normal propanol, and water; and an EDP (ethylenediamine-pyrocatechol) etch mixture. Another consideration, which depended on the etch used, was what material would be suitable to mask the silicon while etching the shadow mask. Photoresist, silicon dioxide, and silicon nitride were all possibilities that were evaluated.

Figure 2. Side view of etch angle: potassium hydroxide etch; <100> crystal orientation.

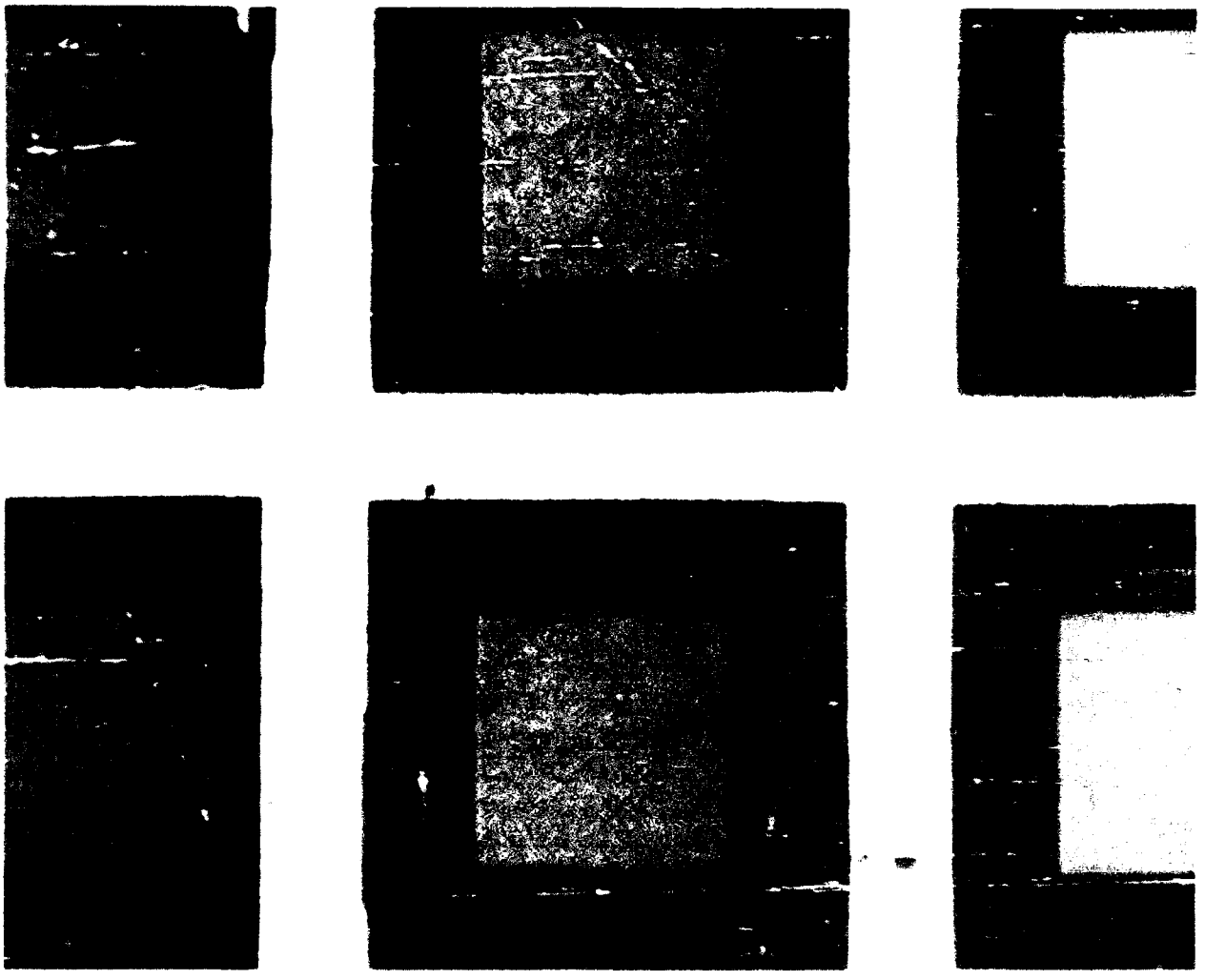

Figure 3. Top view of etch angle: potassium hydroxide etch; <100> crystal orientation.

3. Testing and Evaluation

The first etch test sample, 279 μm thick, was coated with photoresist both on the polished surface and on the back to mask the silicon from the etch. The polished side was patterned with 533- × 533-μm squares. The etch used was an isotropic fast etch of 3 parts nitric acid, 2 parts acetic acid, and 1 part hydrofluoric acid, estimated to etch silicon at 12 to 13 μm (120,000 to 130,000 Å) per minute. The photoresist did not hold up in the etch; it lifted in less than one minute and the area of silicon to be protected was etched along with the holes.

A decision was then made to use an anisotropic potassium hydroxide etch mixture of 80-g normal propanol, 100-g potassium hydroxide, and 320-g deionized water. For several reasons, this is more desirable than the previous fast-acid-based etch, which is isotropic and harder to control when etching thick materials (i.e., μm vs Å). Acid etches tend to etch less uniformly and are more hazardous to work with than caustic etches such as the potassium hydroxide mixture [4].

The surface pattern hole size was calculated for <100> crystal orientation wafers using the potassium hydroxide etch mixture, with the following formula, where d is the etch-through depth and w is the width of the surface pattern [5]:

$d = w/2 \tan (54.7°)$;

therefore, $d = 0.706\, w$.

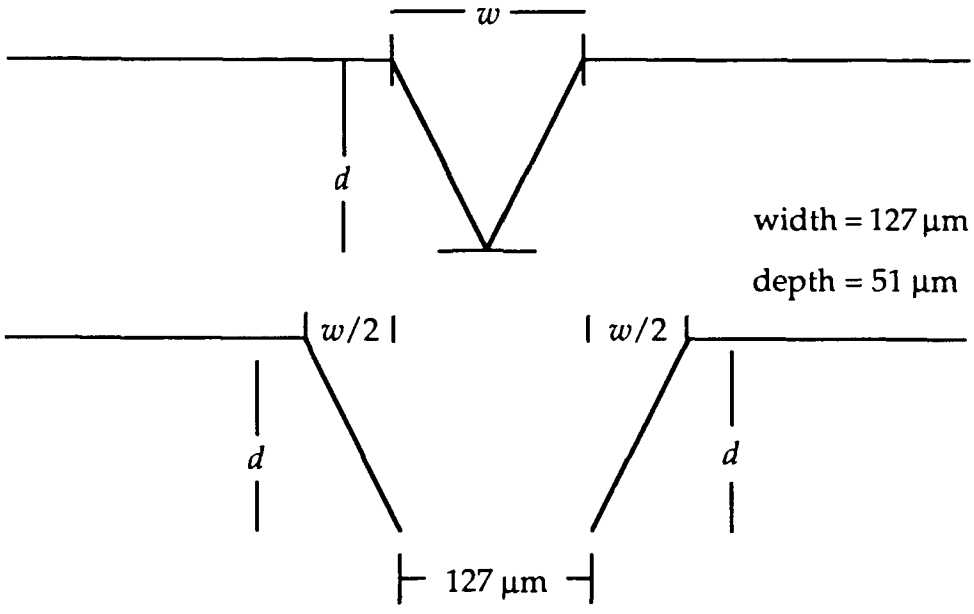

Figure 4. Profile for etch calculation.

If the thickness (i.e., depth) of the wafer to be etched through is known the width of the surface pattern can be calculated. The desired hole size must be added to this calculated figure to determine the actual surface pattern width. Using rounded figures, 533- × 533-μm squares were needed to be patterned for 279-μm-thick etch-through depths and 203 × 203-μm squares for 51-μm depths.

Having used this potassium hydroxide etch mixture in previous work we knew that photoresist does not maintain integrity over time. Thus it was decided to mask the etch with pyrogenically grown silicon dioxide on the samples that measured 51 μm thick. The polished and back surfaces were coated with photoresist, 203- × 203-μm squares were patterned, the silicon dioxide was etched in the patterned areas leaving a mask everywhere else including the wafer back. The resist was removed, and the silicon was etched through in the squares where the silicon dioxide was etched away. Then the silicon dioxide mask was removed. After trying to control the etch rate on several etch-through tests on both 279-μm-thick and 51-μm-thick wafers, we could obtain a fast and yet uniform etch rate of 20,000 Å min (2 μm min) with a potassium hydroxide etch mixture temperature of 95 °C (± 5

The silicon dioxide mask was attacked and eventually etched away before penetrating through the 279-μm-thick silicon samples. We next tested silicon nitride as an etch mask for these thicker samples by first growing a bonding layer of 800-Å silicon dioxide and then depositing 1000-Å silicon nitride. The polished surfaces of each wafer were patterned with 533- × 533-μm squares, the silicon nitride was etched in the patterned areas, the resist was removed, the silicon dioxide was then etched in the patterned area, and then the silicon was etched through the patterned opening. Finally the silicon nitride mask was removed.

4. Results and Conclusions

Because of the selectivity of the etch along the crystal planes and the limitations of aligning the pattern exactly parallel to the crystal plane of the wafer, the patterned squares etched unevenly along the edges, i.e., each area that overlapped a plane was attacked by the etch, producing misshapen etched squares (fig. 5).

Holes of 203-μm diameter were patterned to eliminate having more than one point contact the crystal plane and the resulting etch-through pattern—in spite of slightly shifted rows (due to previously mentioned problem of aligning pattern exactly parallel to crystal plane)—producing more uniformly sized and straight edged squares that measured 127 × 127 μm (fig. 6). Undercutting the circular pattern at four arcs of the circle (fig. 7) resulted in the final square pattern, satisfying the

greater potassium hydroxide etch rate at the <100> crystallographic plane compared to that of the <111> plane. Defective rectangular patterns were used for all acceptable etch through shadow masks. The squares etched in the 51 μm thick wafer proved to be acceptably uniform in shape and size and were also closer together, providing many more capacitors on a small sample chip. Those squares etched in the 279-μm-thick wafers were not uniformly sized and shaped (fig. 8), possibly because the silicon nitride mask started to delaminate at the end of the long period of time necessary to etch through the thicker silicon. The squares were also farther apart because of the distance apart they needed to be patterned to accommodate the etch angle, resulting in much wasted area on the small test sample chip. Platinum was sputtered through the 51 μm thick masks and the resulting platinum squares were quite well defined (fig. 9). Before using the shadow mask, we attempted to sputter platinum through a metal screen on hand, but not designed as a metal mask. In this case, the platinum undershadowed the screen mask, which was too thick (fig. 10), and the resulting dots were therefore unacceptable.

In conclusion, we have shown that with an appropriate processing sequence based on potassium hydroxide, very acceptable shadow masks can be fabricated from silicon wafers. Thin silicon wafers of about 51 to perhaps 127 μm are more desirable than thicker ones for producing uniform structures. Previous microfabricating work done with EDP produced results that were less acceptable than those obtained with the potassium hydroxide and, because EDP is a much more hazardous chemical to use, further EDP process experimentation will not be considered.

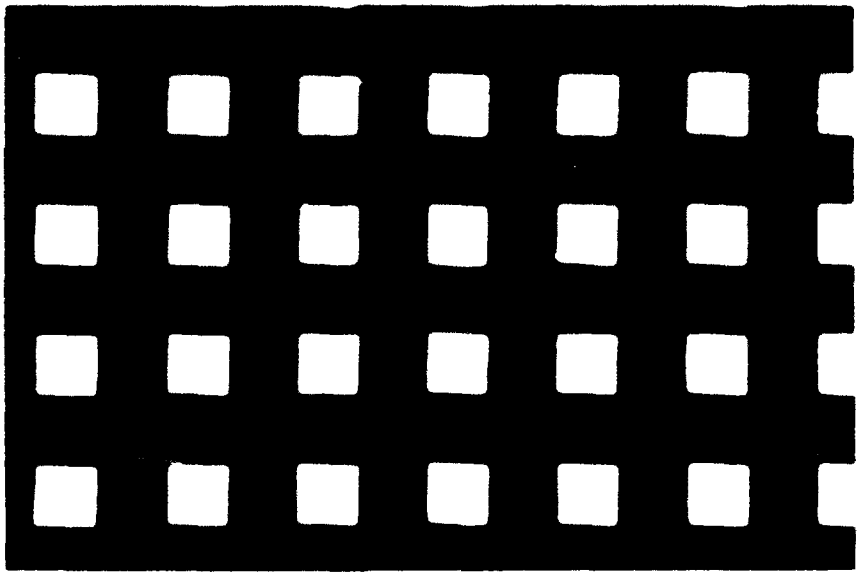

Figure 5. Holes etched in 51-μm-thick wafer using patterned squares.

Figure 8. Squares etched through 279-μm-thick wafer using patterned circles.

Figure 9. Platinum squares sputtered through etch-through shadow mask.

Figure 10. Platinum dots sputtered through metal screen.

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