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1991, 226 pages

Integration of an Anti-parallel Pair of Planar Schottky Barrier Diodes for Millimeter and Submillimeter Wavelengths

A monolithic gallium arsenide chip containing an anti-parallel pair of planar Schottky barrier diodes was developed for integration into subharmonically pumped heterodyne receivers used to detect millimeter and submillimeter wavelength radiation. Such receivers use a local oscillator source at half the frequency required for fundamentally pumped receivers. They are therefore useful in environments that preclude the use of high frequency oscillators, such as lasers, that are bulky and have significant power requirements. Also, the planar technology eliminates the fragile whisker contact, allowing the fabrication of multi-diode circuits. The combination of planar diodes and subharmonically pumped receivers is ideally suited for long lived studies of Earth's upper atmosphere from space.

The diode pair has exhibited excellent electrical characteristics with anodes as small as 1.2 μm. This is the first use of anodes smaller than 2.5 μm on a planar diode. Also, excellent mixing results were obtained in a G-band (183 GHz) subharmonically pumped receiver. This is the first successful application of a planar diode technology at a frequency significantly above 100 GHz. In this receiver, the planar diode pair performed as well as, or better than the best whisker contacted diodes while requiring 3dB less local oscillator power. The diode pair is currently undergoing space certification for U.S. Air Force DMSP weather satellites, and a Space Shuttle study of aero-braking techniques for spacecraft returning from Mars.

Additional studies have made possible the fabrication of a diode pair suitable for use at 600 GHz on NASA's EOS satellites. A prototype 600 GHz design has been generated, and all the fabrication processes necessary for this design have been demonstrated in this research.

Integration of an Anti-parallel Pair of Planar Schottky Barrier Diodes for Millimeter and Submillimeter Wavelengths

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A Dissertation Presented to

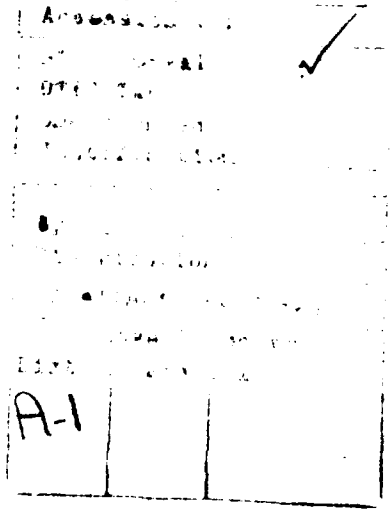
The Faculty of the School of Engineering and Applied Science

University of Virginia

In Partial Fulfillment

of the Requirements for the Degree

Doctor of Philosophy (Electrical Engineering)



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Paul H. Ostdiek

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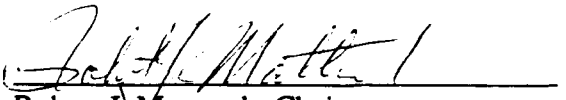

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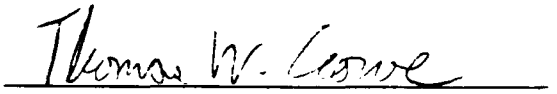

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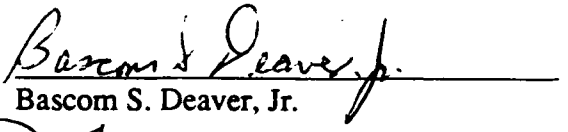

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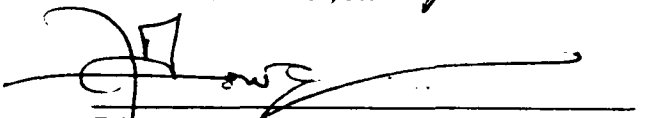

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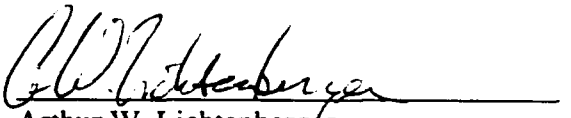

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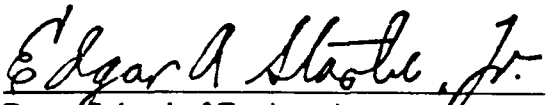

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ABSTRACT

The focus of this work is the development of an anti-parallel pair of planar gallium arsenide Schottky barrier diodes, integrated on a monolithic chip. This chip was designed for integration into subharmonically pumped heterodyne receivers which are used to detect radiation at millimeter and submillimeter wavelengths. The advantage of such a receiver is that it uses a local oscillator source at half the frequency required by a fundamentally pumped receiver. They are therefore useful in environments that preclude the use of high frequency oscillators, such as lasers, that are bulky and have significant power requirements. Also, the use of a planar diode technology eliminates the fragile whisker contact, thus allowing the fabrication of multi-diode circuits. The combination of planar diodes and subharmonically pumped receivers is ideally suited for space applications, such as the Microwave Limb Sounder of NASA's Earth Observing System satellites which will conduct long term studies of Earth's upper atmosphere.

The diode pair, which was designed and fabricated in this research, has exhibited excellent electrical characteristics. These diodes contained anodes as small as 1.2 μm. This is the first use of anodes smaller than 2.5 μm on a planar diode. Also, excellent mixing results were observed with Aerojet-General Corporation's G-band (183 GHz) subharmonically pumped receiver. This is the first successful application of a planar diode technology at a frequency significantly above 100 GHz. In this receiver, the planar diode pair performed as well as, or better than the best whisker contacted diodes. Also, these excellent results were obtained with 3dB less local oscillator power than required for the whisker contacted diodes. Aerojet is currently certifying the diode pair for use in

space on the Air Force's DMSP weather satellites.

The alternative fabrication technologies that are required to scale this successful design to submillimeter frequencies were also investigated. These included reactive ion etching of 0.9 μm anodes, and replacement of the gallium arsenide substrate with quartz. Significantly, this work also demonstrated that excessive heating effects, previously seen in quartz substrate diodes, can be avoided if the ratio of the anode diameter to the thickness of the resulting gallium arsenide membrane is small. A fabrication process suitable for non-alloyed ohmic contacts was also developed.

Also, two scale model studies investigated the parasitic reactances that might limit the chip's performance at submillimeter frequencies. An 800× scale model of a generic planar diode demonstrated that the pad-to-pad capacitance can be controlled by the surface channel depth. Then a set of 61× scale models were used to investigate the inductance of the anode contact fingers.

These studies have made possible the fabrication of an anti-parallel pair of planar Schottky diodes suitable for use at 600 GHz on the Eos satellites. A prototype 600 GHz design has been generated and all of the fabrication processes necessary for this design have been demonstrated in this research.

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Although only one name is on this document, its publication would not have been possible without the help and encouragement provided by others who deserve acknowledgement. First, I wish to thank my academic advisor, Dr. T. W. Crowe, and my graduate committee chairman, Dr. R. J. Mattauch, for their support, and guidance. Their combined efforts have created a special atmosphere within the Semiconductor Device Laboratory that nourishes both research and education. Contributing to this environment is W. L. Bishop, who is one of the most creative individuals I have met, and who has selflessly devoted much time to the work of others, including mine.

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The students at the SDL possess unique skills, and are always willing to assist others. I appreciate the time that many have taken to help me, and want to especially thank W. Peatman, R. Bradley, T. Newman, L. Seidel, J. Hesler, H. Dossal, E. Wingler, and Y. Li for their contributions to my research.

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This work would not have been possible without support of the United States Air Force. I am proud to serve my country through this organization, and honored to work with all those in the Air Force Family.

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DEDICATION

To my wife Karen.

Her love, encouragement, and support has been selfless. I will always remember the sacrifices and hardships she endured, all so I could finish this work. Thankfully, the debt I owe her will take a lifetime to repay.

LIST OF FIGURES

LIST OF TABLES

LIST OF SYMBOLS

A_f	-	cross sectional area of anode contact finger
A_{oc}	-	ohmic contact area
Å	-	Angstroms
C_G	-	capacitance of microstrip gap
C_j	-	junction capacitance
C_{jo}	-	zero bias junction capacitance
C_{pp}	-	pad-to-pad capacitance
C_{SH}	-	shunt capacitance
d	-	depletion depth
DC	-	direct current
E_c	-	conduction band energy
E_F	-	Fermi level energy
E_v	-	valence band energy
f	-	frequency
f_c	-	cut-off frequency
fF	-	femtofarads
F	-	noise figure
F_s	-	ohmic contact geometry scaling factor
G_{avg}	-	average value of conductance waveform
G_{max}	-	maximum value of conductance waveform
G_{min}	-	minimum value of conductance waveform
h	-	Planck's constant
I	-	current
IF	-	intermediate frequency
IM	-	image frequency
$I_{SAT,T}$	-	thermionic emission saturation current

$I_{SAT,TUN}$ - tunneling saturation current

I_T - thermionic emission forward bias current

I_{TF} - thermionic-field forward bias current

k - Boltzmann's constant

K - electron heating factor

L - conversion loss

l_f - anode contact finger length

L_c - inductance of APC-7 connector

L_{eq} - equivalent inductance of two fingers

L_G - inductance of single finger model

L_f - anode contact finger inductance

L_s - inductance of anode contact finger

L_x - anode cone inductance

LO - local oscillator

M - number of diodes used in a mixer

m* - electron effective mass in gallium arsenide

n - active epitaxial layer

n^+ - buffer epitaxial layer

N_d - donor impurity concentration

N_{epi} - impurity concentration of active epitaxial layer

N_{buffer} - impurity concentration of buffer epitaxial layer

pH - pico-Henry

q - electron charge

r - anode radius

r_o - bottom anode radius

r_2 - distance from anode center to ohmic contact

r_t - top anode radius

R_{buffer} - resistance in buffer layer

R_{epi} - resistance of undepleted active epitaxy

R_f - RF anode contact finger resistance

RF - radio frequency - the received signal

R_j - junction resistance

R_{OC} - ohmic contact resistance

$R_{OC,DC}$ - DC ohmic contact resistance

R_s - series resistance

R_{sc} - specific contact resistance

R_{spr} - current spreading resistance

R_x - anode cone resistance

t_{ox} - oxide thickness

T - temperature

T_{cold} - cold load physical temperature

T_{hot} - hot load physical temperature

T_m - mixer equivalent noise temperature

T_n - diode equivalent noise temperature

T_o - ambient temperature

T_{obs} - observed noise temperature

T_{rec} - receiver equivalent noise temperature

V - potential (voltage)

V_o - inverse slope parameter

V_{BB} - semiconductor bulk breakdown voltage

V_{PT} - "punch through" breakdown voltage

v/c - relative phase velocity in microstrip

w - physical width of microstrip line

w_o - effective width of microstrip line at DC

W - thickness of active epitaxial layer

W_m - depletion depth at bulk breakdown

W_{eff} - effective width of microstrip line at DC

y	-	correction factor for zero bias junction capacitance
Y	-	ratio of observed noise powers (hot load/cold load)
Z	-	impedance of the microstrip
Z_o	-	impedance of the microstrip at DC
Z_c	-	impedance of the APC-7 connector
αA	-	loss per unit length of microstrip
αc	-	loss per unit length of APC-7 connector
δ	-	skin depth
ΔV	-	change in forward voltage from 10 to 100 μA
ε_o	-	permittivity of free space
ε_c	-	relative permittivity of the APC-7 connector
ε_{eff}	-	effective dielectric constant of microstrip at DC
ε_r	-	relative permittivity
ε_s	-	semiconductor permittivity
η	-	ideality factor
η_o	-	impedance of free space
μ	-	electron mobility
μA	-	microamps
μm	-	micrometers
ρ_n	-	resistivity of active epitaxial layer
ρ_{n^+}	-	resistivity of buffer epitaxial layer
σ	-	conductivity
ϕ_{bi}	-	built in potential
ϕ_B	-	barrier potential
ϕ_m	-	metal work function
ϕ_s	-	semiconductor work function
χ_s	-	semiconductor electron affinity
ω_{IF}	-	intermediate angular frequency
ω_{IM}	-	image angular frequency

ω_{LO} - local oscillator angular frequency

ω_{RF} - received signal angular frequency

Ω - ohms

CHAPTER 1

INTRODUCTION

1.1 Development of the Schottky Barrier Diode

A Schottky barrier may be formed when a metal and semiconductor are brought into contact. Under certain circumstances, this barrier allows electrons, or holes, to flow more easily from the semiconductor to the metal than from the metal to the semiconductor. Unlike that in p-n junctions, this transport of charge does not depend on the diffusion of minority carriers. Therefore, Schottky diodes are fast devices that can operate at high frequencies. The speed of the device is enhanced by using materials with high electron mobilities, such as gallium arsenide (GaAs).

The physics of metal/semiconductor interfaces has been investigated since 1874 [1] and devices based upon their use have been patented since 1904 [2]. However, it was not until 1938 that Schottky explained this rectifying behavior in terms of a potential barrier, and a redistribution of charge within the semiconductor [3]. Both the height and thickness of this barrier influence the ability of charge to migrate across it. If the crystal is lightly doped with impurity atoms the barrier is thick and inhibits the flow of charge. If the crystal is heavily doped, however, the barrier is thin and electrons easily tunnel through the barrier.

Near ideal junction characteristics were not realized until 1963 when Archer and Atalla used a high vacuum technology to deposit thin metal films on silicon at Bell Telephone Laboratories (BTL) [4]. This allowed the formation of Schottky contacts with consistent characteristics. GaAs was probably first used above 100 GHz in 1963 by

Cohn, Wentworth, and Wiltse [5]. Their diode consisted of a pointed wire whisker that was first pressure contacted to the crystal, and then welded in place by discharging a capacitor through the contact. In 1955 Young and Irvin [6], also of BTL, produced the first "honeycomb" diode, a technology that is still used today. They used photolithography to place an array of three micron diameter, circular holes in a thin oxide layer on a gallium arsenide surface as shown in Figure 1.1. The anodes were formed by electroplating gold onto the semiconductor at the bottom of these holes. Although they also used a whisker to connect the anode to the external circuit, the critical metal-semiconductor interface was formed by electroplated gold, rather than an even more

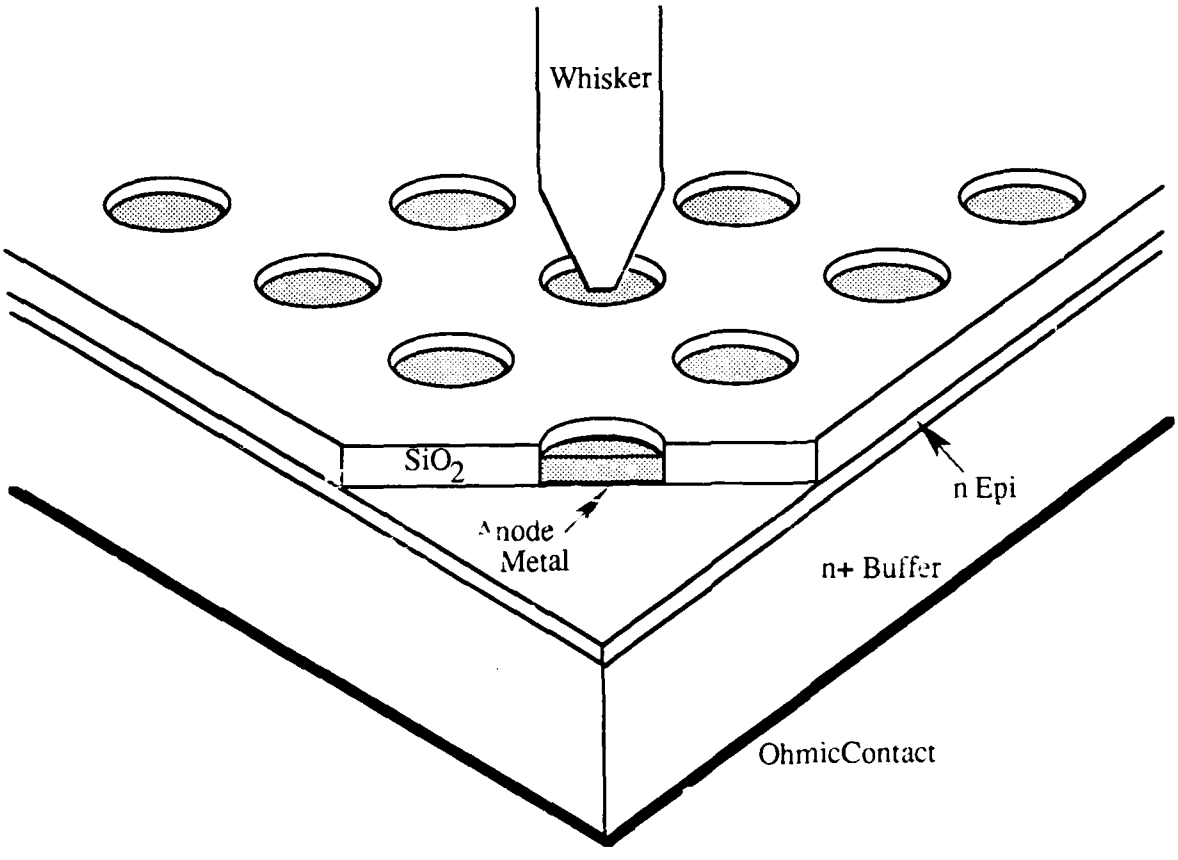


Figure 1.1 The Honeycomb Diode

fragile whisker contact directly to GaAs.

Researchers at the University of Virginia have fabricated honeycomb diodes similar to these since 1969 when R.J. Mattauch improved upon the technology and junction quality, and fabricated diodes for the National Radio Astronomy Observatory (NRAO). It was at this time that Schottky diode mixers began achieving predicted low noise temperatures [7]. Since then, the Semiconductor Device Laboratory (SDL) at the University of Virginia has contributed significantly to radio astronomy by consistently fabricating the highest quality diodes. Over the years these diodes have been optimized so that receivers have been developed for the entire submillimeter wavelength range (300 GHz - 3 THz) [8], [9], [10].

Performance at such short wavelengths is significantly limited by the parasitic capacitance associated with connecting the diode to a circuit. Mixer designers have therefore endured the cost and technical difficulties associated with whisker contacted diodes since this configuration minimizes this parasitic. However, the need to position a fine pointed wire with a precise amount of pressure in the center of an anode one micron in diameter is extremely challenging. The difficulty of building reliable millimeter wave mixers with whisker contacted diodes has been sufficient to deter most from developing more complicated multi-diode mixer structures, which are used widely at lower frequencies [11].

The desire to put heterodyne receivers on space borne platforms exacts even more stringent demands on the design of the receiver and particularly the mixer diode. Some of these requirements are best met by replacing whisker contacted diodes, whose space certification may require three to six months, with planar (whiskerless) diodes [12], [13].

The anode contact of a planar diode is essentially space certified when delivered to the user. Several laboratories have recently developed millimeter wave planar diode technologies with parasitic capacitances approaching those of whisker diodes [14],[15]. These devices replace the fragile whisker with an integrated anode finger which connects the anode to an anode bonding pad. This makes the chip easy to mount and virtually eliminates the possibility of losing contact with the anode.

The availability of planar devices makes feasible the fabrication of more complicated mixer structures. For example, an anti-parallel pair of Schottky barrier diodes will exhibit a symmetric *I-V* curve that can be used in a subharmonically pumped mixer. In such a mixer the received signal (RF) is mixed with a local oscillator (LO) signal that is approximately half the frequency of the RF, yielding an intermediate frequency output given by $\omega_{IF} = \omega_{RF} - 2\omega_{LO}$ [16], [17], [18]. This low frequency signal can then be amplified and analyzed by standard microwave techniques. Since the subharmonically pumped mixer requires an LO source that is only one-half the frequency of the signal, it is ideally suited for applications where stable local oscillator power near the RF is too expensive or impossible to generate; specifically, for satellite based receivers operating at millimeter and submillimeter wavelengths.

Planar diodes also offer the advantage of compatibility with integrated microwave circuit technologies. This allows the realization of better and more complex receivers that are well suited for space applications. Furthermore, planar diodes allow commercial manufacture of the inexpensive, fully integrated receiver required for large scale exploitation of millimeter waves.

1.2 Applications of the Schottky Barrier Diode

A natural application of the rectifying property of a Schottky barrier is the fabrication of diodes that can follow high frequency signals. Such diodes have proven useful in direct [19], [20], [21] and heterodyne detection schemes. Heterodyne receivers have used Schottky diodes to detect signals at frequencies near 3000 GHz, and have achieved noise equivalent powers (heterodyne, NEP_H) near 10^{-19} W/Hz [22], [23], [24].

The heterodyne receiver has been used most extensively in radio telescopes. Astronomers have used these telescopes to study the composition of interstellar matter for several decades. The maturity of their techniques, and the availability of the Schottky diode has generated many new applications. These include the temperature measurement of ions in Tokamak plasmas [24], the measurement of subnanosecond pulse profiles of lasers [22], [25], and remote sensing of the atmosphere [26], [27].

It is recognized today that the earth's atmosphere is a single, closely interacting mass; and that regional atmospheric perturbations can ultimately have global consequences [28]. The study of these perturbations is motivated in part by the current concerns regarding pollution, acid rain, global warming, and depletion of upper atmospheric ozone. Also a world-wide observation network is required to forecast severe weather storms. The use of unmanned earth satellites best provides this long term, global monitoring capability.

Creating a global, surface based observation network is difficult for several reasons. First, trained personnel must be found who are willing to serve in the remotest regions of the earth. Also, the logistical support and communications effort associated with the network become overwhelming. This network must include aircraft, balloons, and

rockets to sample the upper atmosphere. Additionally, an armada of weather ships must be supported to cover the oceans, which are important in meteorological models. In 1966 Widger reported an estimated cost of 160 million dollars to support weather ships in the North Pacific and oceans of the southern hemisphere to provide only a minimal coverage. The total cost of a surface network would be far in excess of the 100 million dollar cost (1966) associated with the early Nimbus series satellites [29], which provided global data four times a day concerning areas as small as 860 square kilometers [30]. Additionally, satellites offer a stable view of the atmospheric limb which maximizes instrument sensitivity and resolution of vertical profiles.

A satellite system is not without its disadvantages however. The limited performance of launch vehicles place restrictions on sensor size, weight, and power consumption. Also, because their orbit is so remote, mistakes become very expensive. Additionally, the space environment is harsh. The system must survive the mechanical stresses of the launch, and thermal cycling and radiation exposures of orbit. These factors exacerbate reliability concerns, making space certification of an instrument difficult.

Microwave remote sensing of earth's atmosphere began in 1944 when Dicke's heterodyne receiver observed thermal radiation emitted by water vapor at 20, 24, and 30 GHz [31]. These experiments showed that space provides a cooler background at centimeter wavelengths than Jansky found at meter wavelengths in the 1930's. Microwave remote sensors moved to space based platforms in 1962 when Mariner 2 used 15.8 and 22.2 GHz receivers to confirm the high surface temperature of Venus [32]. Microwaves were first used to study the earth from space by the Soviet Union in 1968 on

Cosmos 243 [33]. This system monitored 3.5, 8.8, 22.2, and 37.5 GHz emissions to measure atmospheric water (both vapor and liquid), sea surface temperatures, and ice cover. Subsequent flights incorporating microwave receivers include Cosmos 384 (1970), Nimbus-5 (1972), the S-193 radiometer of Skylab's Earth Resource Experiment Package (May 73 - Feb 74), Seasat (1978), Nimbus-7 (1978), Tiros-N (1978 and later), and the Block 5D satellites (1978 and later) of the Defense Meteorological Satellite Program (DMSP) [30].

The last twenty years has witnessed significant increases in the frequencies planned for long lived space instruments. In 1970 plans existed for a 60 GHz receiver for Nimbus-5. In 1980 the maximum frequency increased to 200 GHz as plans were made for the Microwave Limb Sounder of the Upper Atmosphere Research Satellite (UARS) and the Microwave Atmospheric Sounder of the Space Shuttle. Current plans call for a 640 GHz receiver to fly on Eos (Earth Observing System), and future Eos flights to implement receivers at frequencies approaching 3000 GHz [26].

Microwave receiver capability has now matured to the point that many well characterized upper atmospheric molecules are accessible. This capability meshes nicely with desires to conduct long term observations of man's influence on the earth's atmosphere. This combination marks the beginning of a new era in the science of atmospheric remote sensing [34]. Later this year the UARS will be launched. It will use the 63, 183, and 205 GHz receivers of its Microwave Limb Sounder to conduct long term studies of upper atmospheric ClO, H_20, O_3, H_2O_2, HNO_3, temperature, pressure, and wind patterns [26].

The UARS mission will be followed by the Eos satellites. The Microwave Limb Sounder (MLS) flown on the Eos B series satellites will initially carry 117, 205, 268, 560, and 637 GHz receivers, allowing observation of all major molecules in the ozone cycle, for at least fifteen years [35]. It is planned that the 560 and 637 GHz receivers will use planar, anti-parallel diode pairs in subharmonically pumped mixers, provided the planar technology is proven in the near future [36].

Two significant problems must be solved before planar diodes are widely used in space. First, the diodes must be optimized to give competitive performance at the required frequencies. This means that the parasitic capacitances within the device must be reduced [37]. Secondly, a method must be found to supply the mixers with the required LO power. Current submillimeter receivers use lasers as LO sources which are too bulky, and consume too much power for a satellite platform. A solid-state LO source which is small, light, and modest in power requirements is ideal for this application; but such devices (typically Gunn diodes) are limited to about 100 GHz. There is however, an approach that allows the use of a millimeter wave oscillator to pump a submillimeter receiver. Efficient frequency multipliers which double or triple the output frequency of the fundamental source, combined with a subharmonic mixer and an anti-parallel pair of planar diodes form a viable submillimeter receiver. A key element of this approach is that a subharmonically pumped mixer requires an LO source that is only half the signal frequency. Therefore, a 600 GHz receiver could by driven by a 300 GHz source. Although subharmonic mixing does not have a theoretical noise performance as good as that of fundamental mixing [38], it does allow the use of reliable systems suited for the isolation of space.

1.3 Research Objective

The objective of this research is to develop a planar technology that makes possible the use of reliable submillimeter receivers in environments where access to LO power is limited. This is not a problem of fine tuning an existing technology. Rather its focus is the creation of a new device that allows the flight of submillimeter receivers in space. Currently no space compatible LO source exists that is capable of delivering enough LO power for fundamental operation of receivers at these frequencies. There are two ways to solve this problem. The most direct is the ongoing research to create solid-state LO sources with increased output frequencies. A second is to design subharmonically pumped receivers, which allow operation at a frequency twice that at which adequate LO power exists. These are complementary efforts, the improvement of LO sources raises the maximum frequency, while the use of subharmonic pumping increases the maximum frequency by an additional factor of two. The use of submillimeter subharmonically pumped receivers in space requires the development of a planar anti-parallel diode pair, the subject of this research.

This research was begun with two specific goals. First, a single chip containing a pair of planar Schottky barrier diodes, configured anti-parallel to one another, was to be designed, fabricated, and tested. This diode pair was to operate in a 183 GHz[1] subharmonically pumped heterodyne receiver on Air Force Defense Meteorological Satellite Program (DMSP) weather satellites. When begun, the use of planar diodes was limited to frequencies below 100 GHz. The use of a subharmonically pumped receiver appeared to be an ideal way to extend the 100 GHz technology to 200 GHz. The second goal was to investigate the further extension of this millimeter wave technology to

[1] This sensor monitors the 183.310 GHz line of atmospheric water vapor [39].

submillimeter waves with frequencies above 600 GHz. The application in mind here is NASA's Earth Observing System (Eos) satellite scheduled for launch in the year 2001 [36].

1.4 Approach

The cornerstone of this project is the design and fabrication of a diode pair for use in the millimeter wave spectrum. This design is based on past experiences at the Semiconductor Device Laboratory with the planar Surface Channel diode, which was developed after a variety of other planar technologies were explored. Although plans included testing the diode pair in a specific receiver, no one mixer design drove the diode's design process. This first section of research included:

(1) A search for electroplating parameters capable of forming high quality anodes for the SDL's Surface Channel diode. This was required because the Surface Channel technology did not consistently yield quality anodes at the beginning of this research.

(2) Design of a photolithographic mask set and fabrication sequence for the millimeter wave diode pair. Since the chip was designed for general use in the millimeter spectrum this mask set allows for 36 variations in the diode characteristics.

(3) Electrical characterization of the device, including forward current-voltage, capacitance, and DC noise characteristics.

(4) Supplying chips to the Electrosystems Division of Aerojet-General Corporation for evaluation in their 183 GHz subharmonically pumped mixer. This mixer was designed for whisker contacted diodes. Therefore, the choice of this mixer allows a comparison of whisker contacted and planar technologies.

The second portion of this research addresses optimization of the millimeter design for use in the submillimeter spectrum. It includes:

(1) Design and fabrication variations for reduced anode diameter, parasitics, and power requirements.

(2) A scale model study of a parasitic "pad-to-pad" capacitance.

(3) A scale model study of the inductance of the anode contact "fingers."

1.5 Dissertation Outline

The main body of this dissertation is presented in the following seven chapters. These chapters can be summarized as follows:

Chapter 2 presents the theory associated with the physics of both the diode and heterodyne reception. The diode theory discusses the formation of the Schottky barrier, and the transport of charge across the barrier. Also, the parasitics which limit the performance of planar diodes are outlined. Then, noise mechanisms within the diode are discussed. Chapter 2 finishes by discussing both fundamentally and subharmonically pumped mixers (heterodyne receivers).

Chapter 3 begins by comparing the whisker contacted diode with a generic planar "whiskerless" diode. This comparison discusses the strengths and weaknesses of both technologies. Then a variety of planar technologies are reviewed. This is followed by both the present design of the Surface Channel diode and its development.

Chapter 4 presents the design of the anti-parallel diode pair. This includes the design goals, device geometry, and materials used. The design of the photolithography mask is also presented.

Chapter 5 reviews the fabrication techniques used to make the diode pair: photolithography (pattern transfer), additive processes (thin film deposition), and subtractive processes (etching). Then the fabrication sequence of the diode pair is presented.

Chapter 6 presents fabrication results and recounts the problems encountered while developing the fabrication sequence. These included an oxide attack during formation of the ohmic contacts, poor anode quality, and thin anode contact fingers. Also encountered were an attack of the anode area by the surface channel etch, and damage to the substrate due to wafer curling after lapping.

Chapter 7 discusses the performance of the diode pair. This includes electrical characterization of forward current-voltage (*I-V*) characteristics, capacitance, DC noise, and behavior in a 183 GHz mixer.

Chapter 8 addresses the second research objective: optimization of the diode pair for submillimeter waves. This chapter begins by presenting the variations from the standard technology that were investigated. This includes quartz substrate devices, dry etching anode holes, selectively thinning the crystal through the anode holes, non-alloyed ohmic contacts, and dicing/lapping variations. Then a design allowing individual biasing of the diodes is discussed. Also, results of scale modeling of parasitic capacitance and inductance are presented. Finally, an anti-parallel design is presented for use at 600 GHz.

This dissertation concludes in Chapter 9, which presents a summary of this work and recommendations for future work.

CHAPTER 2

THEORY

2.1 Introduction

This chapter presents the theory that is applicable to this project in two sections. First, the theory related to Schottky barrier diodes is examined. This includes the formation of the barrier, and the transport of carriers over, or through this barrier. Also included is the complete circuit model of the junction and the associated packaging parasitics. This section concludes with a discussion of the noise mechanisms within the diode. The second section examines the heterodyne reception of signals, the primary application for our diode. The discussion begins with an introduction to fundamentally pumped mixing, and finishes with an analysis of the subharmonically pumped receiver.

2.2 Schottky Barrier Diode

The theory related to the physics and design of Schottky barrier diodes is presented in five parts. The formation of the barrier that controls current is discussed first. Then the mechanisms responsible for the transport of charge across the barrier are reviewed. The circuit model used to design the diode is presented in the third section. This is followed by a discussion of the packaging parasitics. Finally, the important noise mechanisms within the diode are outlined.

2.2.1 Schottky Barrier

The concept of energy states, allowed and forbidden to electrons, is often used to describe phenomena observed in semiconductors, and will also be used here. Figure 2.1 depicts an energy band diagrams for a semiconductor and a metal. The semiconductor is characterized by the highest energy allowed to a bound electron in the valence band, E_V,

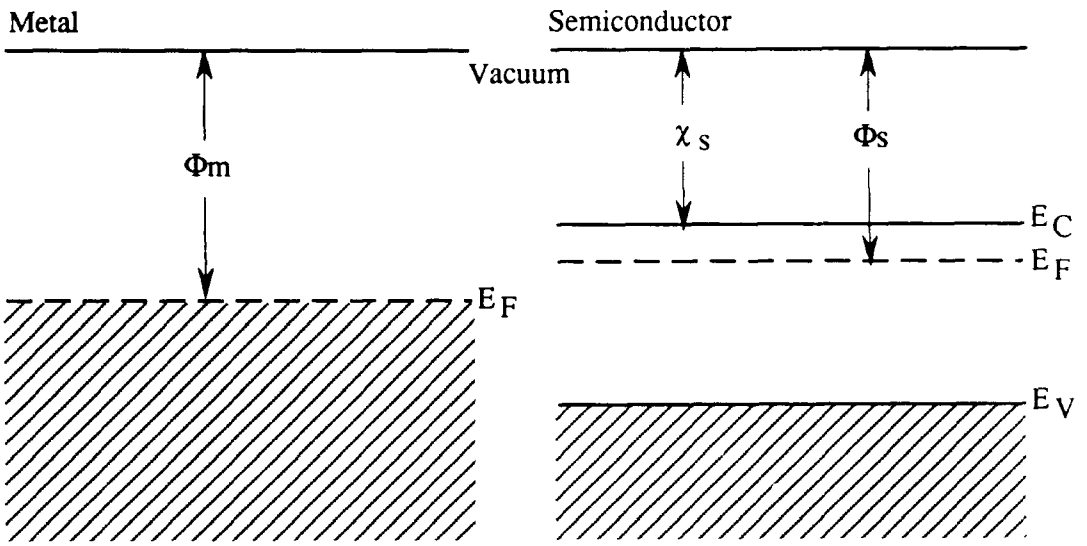


Figure 2.1 Energy Band Diagrams for a Metal and a Semiconductor

the lowest energy allowed to a free electron in the conduction band, E_C, and a Fermi energy level E_F. The Fermi level is a reference that characterizes the energy distribution of electrons at a given temperature, and is used to calculate the concentration of free electrons in the conduction band. A typical metal has a large number of electrons in its conduction band, with its Fermi level located between the mostly occupied and mostly empty portions of the conduction band.

The semiconductor and metal work functions ϕ_s and ϕ_m indicate the energy required to raise an electron from the Fermi level to the vacuum state, where it is free of that material. The electron affinity χ_s is the energy required to raise an electron from the lowest conduction state to the vacuum.

A metal and semiconductor must come into thermodynamic equilibrium with each other when they are close enough to exchange carriers. Therefore, the materials

exchange electrons until the average carrier energy is the same in both materials. The Fermi levels then align with each other. Since the work function of the metal and the electron affinity of the semiconductor do not change, the conduction and valence bands bend. If ϕ_m is greater than ϕ_s, a rectifying contact is formed as depicted in Figure 2.2. Physically, the higher energy electrons within the semiconductor move into the metal leaving immobile positive charge behind, which attracts the electrons in the metal near the junction. A consequence of this charge separation is an electric field, or potential barrier, that discourages the further exchange of carriers. This barrier defines a region depleted of mobile carriers in the semiconductor.

Electrons in the metal must overcome the "barrier" potential ϕ_B to enter the semiconductor, and electrons in the semiconductor need only overcome the "built in"

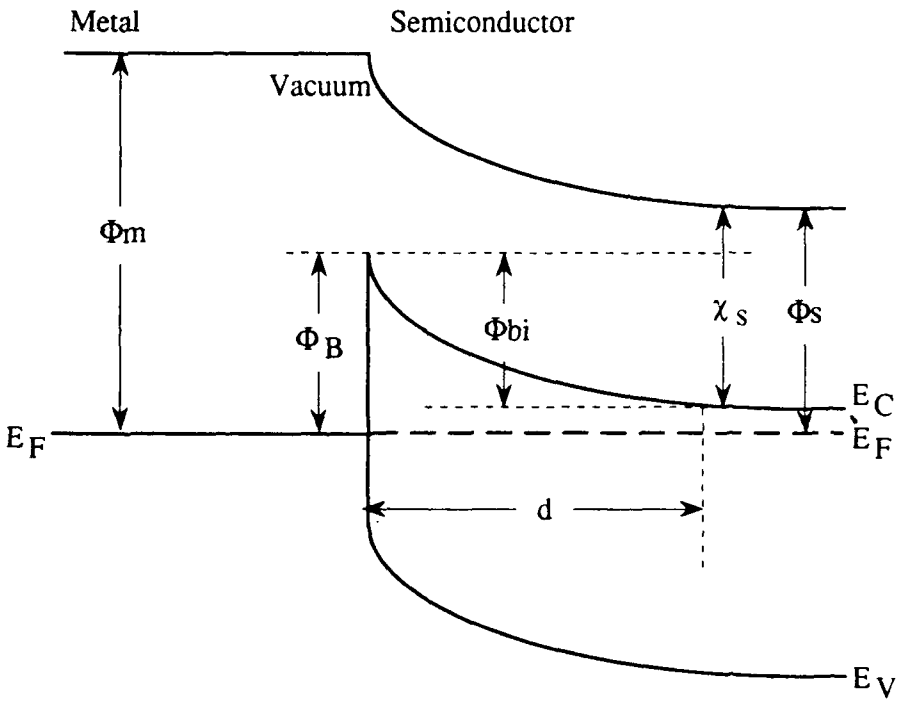


Figure 2.2 Band Diagram of the Schottky Barrier

potential ϕ_{bi} to enter the metal. However, the built-in potential changes when an external voltage is impressed across the junction. As shown in Figure 2.3, a "forward" voltage will reduce both the built-in potential and the width of the depleted region, making it easier for electrons to enter the metal. Both increase, however, when the applied voltage is reversed. The Fermi levels do not line up in either case since the external voltage upsets the internal thermodynamic equilibrium. Notice that the applied voltage does not change the barrier potential seen by electrons in the metal. Effectively then, charge can be made to flow only one way. This is the cause of the rectifying nature of the Schottky diode.

As presented, the barrier potential ϕ_B should vary depending on the particular metal. However, it is observed that for GaAs the barrier height is generally independent of the metal used, and approximately equal to $\frac{2}{3}(E_c - E_v)$. This phenomena is attributed to the pinning the Fermi level by a high density of surface states within the forbidden gap [40]. Physically, the abrupt termination of the crystal lattice creates a large number of incomplete atomic bonds at the surface, which trap charge. A barrier ϕ_B of

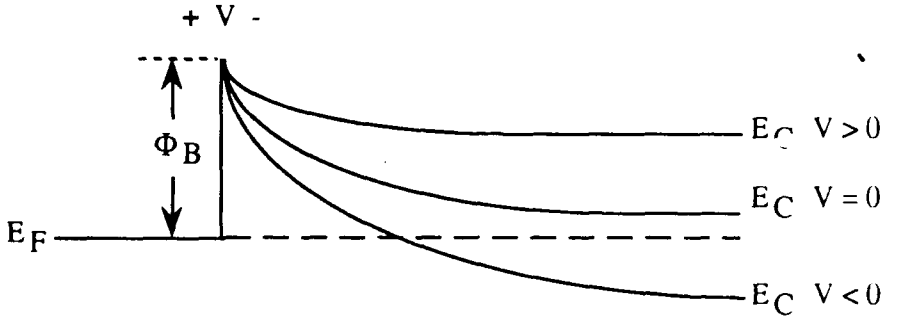


Figure 2.3 External Voltage Effects on the Schottky Barrier

approximately 0.9 eV is observed for GaAs. The choice of the metal used to form the barrier then depends on other aspects of the technology used.

2.2.2 Carrier Transport Mechanisms

Two mechanisms have been found to describe the transport of carriers across the barrier. These are thermionic emission and tunneling. Other processes, such as recombination in the depleted region and hole injection from the metal, are negligible for GaAs and therefore not discussed.

As applied to the Schottky barrier, thermionic emission assumes that the barrier height is much greater than kT, and that tunneling current is negligible. The resulting current-voltage characteristic is then:

$$I_T = I_{SAT,T}\left(\exp\left\{\frac{V}{V_o}\right\} - 1\right) \tag{2.1}$$

where V is the applied voltage, and the inverse slope parameter is:

$$V_o = \frac{\eta kT}{q} \tag{2.2}$$

A diode experiencing ideal thermionic emission has an ideality factor η of one.

The thermionic emission model serves well for lower doped ($< 5\times10^{17}$ cm^{-3}) crystals near room temperatures. However, it does not include the effects of the quantum mechanical tunneling of electrons through the barrier that are important for heavily doped crystals or at low temperatures. To correct this, Padovani and Stratton [41] added

a tunneling mechanism to the model. Their Thermionic-Field emission theory predicts that:

$$I_{TF} = I_{SAT,TUN} \exp\left\{\frac{V}{V_o}\right\} \tag{2.3}$$

where

$$V_o = V_{oo} \coth\left[\frac{V_{oo}}{kT}\right] \tag{2.4}$$

$$V_{oo} = \frac{h}{4\pi}\sqrt{\frac{N_d}{\varepsilon_s m^*}} \tag{2.5}$$

and m* is the effective mass of the carrier and h is Planck's constant.

Figure 2.4 illustrates the dependence of V_o on temperature and doping concentration in the Thermionic-Field emission model. Notice that tunneling limits the value of V_o at low temperatures or for high concentrations of impurities.

2.2.3 Diode Circuit Model

Design of a Schottky diode begins with the circuit model of a crystal rectifier shown in Figure 2.5. In this model, R_j is the variable resistance of the junction. It is the important term for a resistive mixer. The terms C_j and R_s are parasitics which limit the diode's high frequency performance.

The capacitance C_j represents the effect of charge separation by the barrier. It limits the response of the diode at high frequencies by shorting R_j, thereby reducing the

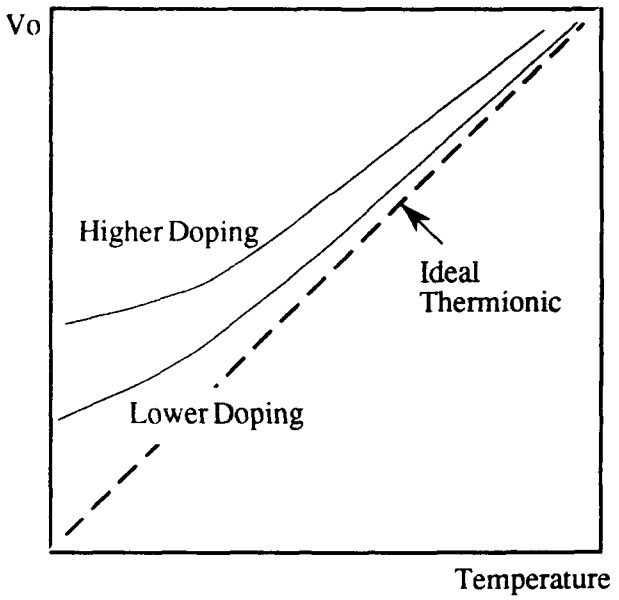


Figure 2.4 V_o vs. Temperature Dependence on Doping Concentration

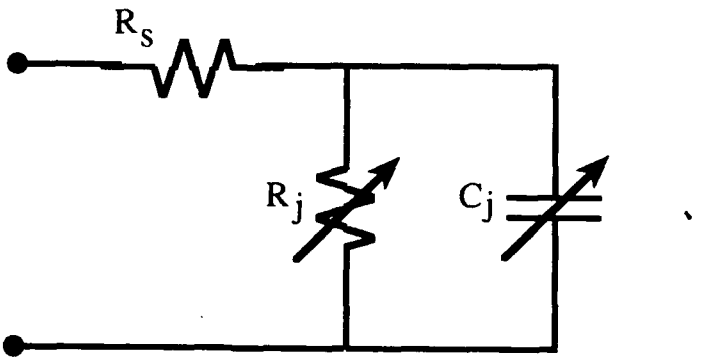


Figure 2.5 Simple Circuit Model of the Schottky Diode.

non-linearity of R_j seen by the external circuit. The junction capacitance is given by Copeland as [42]:

$$C_j = \frac{\varepsilon_s A}{d}\left[1 + \frac{yd}{r}\right] \tag{2.6}$$

where the factor y is [43]:

$$y = 4\left[+\frac{0.43}{\varepsilon_r}\right] \approx 1.5 \text{ for GaAs} \tag{2.7}$$

The first term in (2.6) is the ideal parallel plate capacitance of the anode. The second term is the contribution of the fringing field. The width of the depletion region d is:

$$d = \left[\frac{2\varepsilon_s}{qN_{epi}}(\phi_{bi} - V - \frac{kT}{q})\right]^{1/2} \tag{2.8}$$

For GaAs, the built-in potential is of order one volt, and $\frac{kT}{q}$ is neglected. The anode radius r is chosen to provide a capacitance that matches the diode to the mixer's embedding circuit.

The remaining parasitic term in Figure 2.5 is the series resistance R_S. It is the sum of the undepleted epitaxial layer, the buffer layer, and the ohmic contacts:

$$R_S = R_{epi} + R_{buffer} + R_{oc} \tag{2.9}$$

as illustrated in Figure 2.6. The resistance R_{epi}, due to the undepleted epitaxy, depends on the applied bias voltage, and is calculated as:

$$R_{epi} = \frac{\rho_n(t_{epi} - d)}{\pi r^2} \tag{2.9}$$

The depleted region width is given by (2.8) and is typically set to zero in RF calculations. This provides an upper limit estimate of this resistance for the forward biased diode.

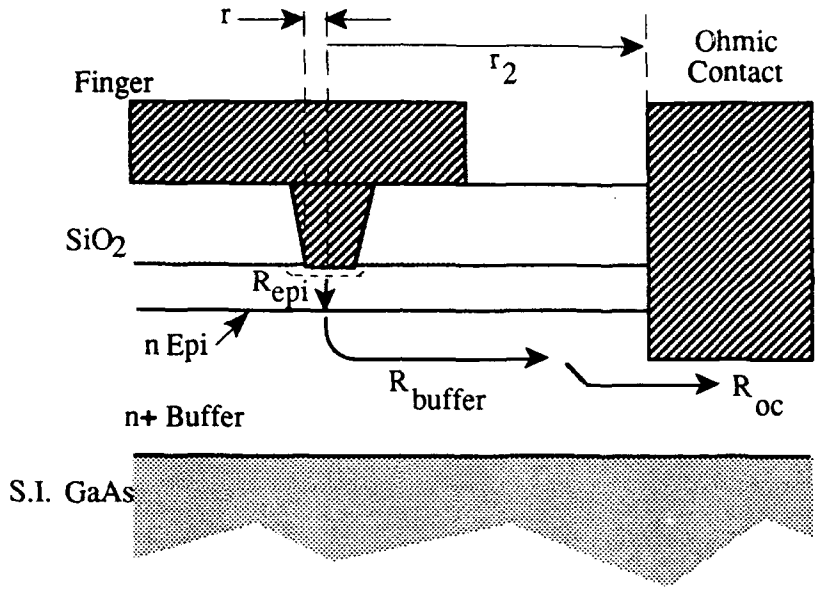


Figure 2.6 Resistances Contributing to the Diode's Series Resistance

After leaving the epitaxial layer, the current spreads in the buffer layer and turns towards the ohmic contact. This is represented by R_{buffer}. At DC this resistance is [44]:

$$R_{buffer,DC} = \frac{\rho_{n^+}}{4r} \tag{2.10}$$

The contribution of the ohmic contact to the DC series resistance is:

$$R_{oc,DC} = \frac{R_{sc}}{A_{oc}} \tag{2.12}$$

The specific contact resistance R_{sc} is typically $10^{-5}\Omega cm^2$ or greater. This value sets a lower limit on the ohmic contact pad area A_{oc}.

At high frequencies the current interacts with its own magnetic field. This interaction constricts the current to the surface of the material, forcing the charge to flow through small cross sectional areas, thereby increasing resistance. These areas are

usually characterized by the conductor's "skin depth" δ:

$$\delta = [\pi f \mu \sigma]^{-1/2} \tag{2.13}$$

The high frequency series resistance is best calculated using numerical techniques to solve Maxwell's equations in a manner similar to Bhapkar's work [45]. The resistance can be estimated; however, by splitting R_{buffer} into two parts: $R_{buffer} = R_{spr} + R_{buf,RF}$. The term R_{spr} represents the resistance encountered as the current spreads after leaving the anode. The resistance of the buffer layer itself is $R_{buf,RF}$. Blanton [46] modified the expression of Carlson et al. [47] for R_{spr} at high frequencies as:

$$R_{spr} = \frac{\rho_{n^+}}{2\pi r} \tan^{-1}\left[\frac{\delta}{r}\right] + F_S \frac{\rho_{n^+}}{4\pi\delta} \tag{2.14}$$

The geometric scaling factor F_S accounts for the ohmic contact geometry depicted in Figure 2.7, and calculated as

$$F_S = \frac{360°}{2\theta + 180°} \tag{2.15}$$

In this work $\theta = 0°$ so SF = 2. Then the buffer layer resistance at RF is:

$$R_{buf,RF} = \frac{F_S \rho_{n^+}}{2\pi\delta} ln\left[\frac{r_2}{r}\right] \tag{2.16}$$

The ohmic contact resistance at RF is given for the planar diode by Sętzer [48] and Blanton [46] as:

$$R_{OC,RF} = \frac{1}{F_S \pi r_2}\left[\frac{\rho R_{sc}}{\delta}\right]^{1/2} \tag{2.17}$$

where r_2 is the distance from the anode center to the ohmic contact.

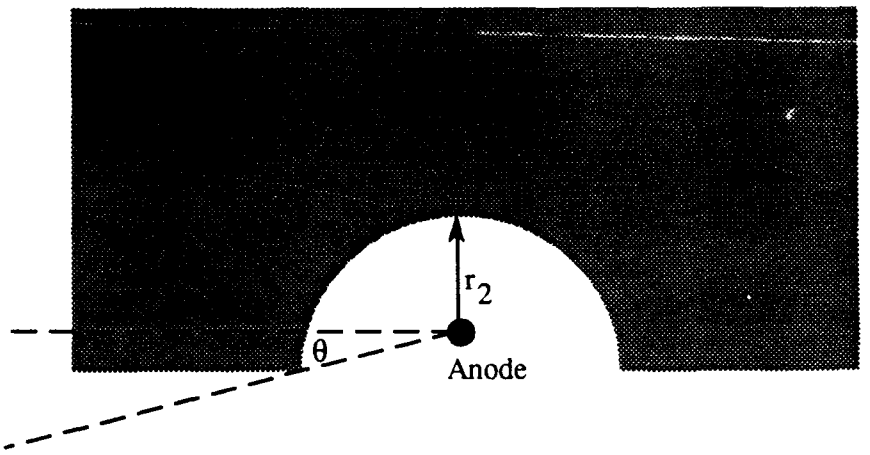


Figure 2.7 Geometry of Ohmic Contact Scaling Factor F_s

The cutoff frequency is a figure of merit used to compare the high frequency performance of diodes. It is calculated from R_s and the zero bias (V=0) junction capacitance as:

$$f_c = \frac{1}{2\pi R_s C_{jo}} \tag{2.18}$$

In practice, a design goal is to make f_c at least a factor of ten greater than the operating frequency.

Study of the $R_s C_{jo}$ product, or cut off frequency yields different results depending on whether $R_{S,DC}$ or $R_{s,RF}$ is used. If the $R_{s,DC}$ is used, it appears that an optimum anode diameter exists for a given doping as shown in Figure 2.8. However, Setzer demonstrated that if the $R_{s,RF}$ is used instead, the smallest anode will always yield the largest cutoff frequency. From a practical point of view though, it can become difficult to couple adequate LO power into a very small anode if the diode's impedance is not matched to that of the embedding circuit.

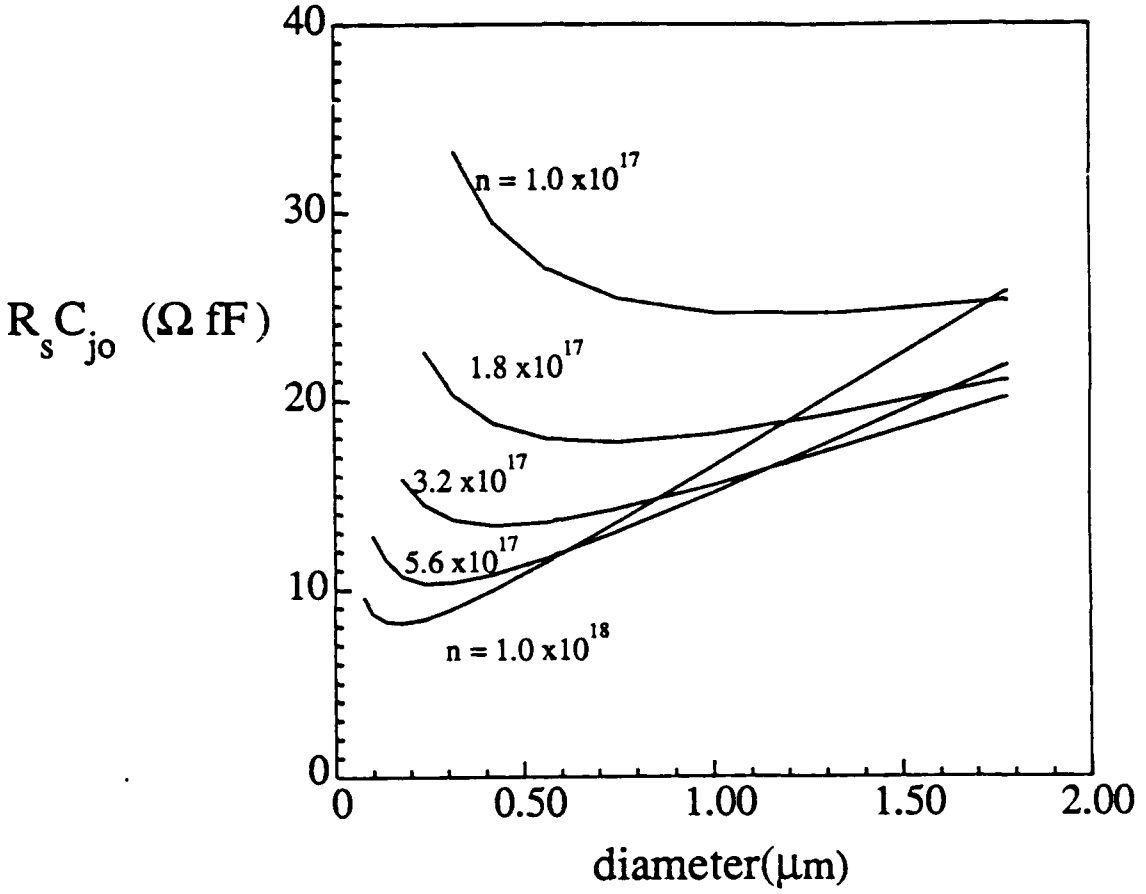


Figure 2.8 $R_{S,DC}C_{jo}$ Product vs. Anode Diameter for Several Active Layer Dopings.

If the epi is thinned to reduce R_S, the depleted region may extend, or "punch-through" into the n^+ buffer causing a higher electric field and reduced breakdown voltage. For an abrupt transition n-n^+, the punch through voltage is calculated as:

$$V_{PT} = \left[\frac{W}{W_m}\right]\left[2 - \frac{W}{W_m}\right]V_{BB} \qquad (2.19)$$

where V_{BB} is the bulk breakdown voltage for an epi thicker than the maximum depletion width W_m. A rule of thumb is to make $t_{epi} = W_o + 100\text{Å}$, but not to let V_{PT} be less than 4 volts. A V_{PT} too low may allow the diode to breakdown during the pump cycle,

adding noise and possibly damaging the diode.

Reviewing the relationship for C_{jo} and R_S we see that as N_{epi} increases C_{jo} increases but R_S decreases. A tradeoff exists. To resolve this issue Crowe [50] studied the importance of various parameters in mixer performance and concluded that for frequencies less than 600 GHz it was most important to reduce noise. This means that the mixers should be cooled and a low N_{epi} (10^{16} cm^{-3}) used to reduce shot noise. Above 600 GHz the product R_SC_{jo} becomes most critical as the cutoff frequency was approached. Therefore, these are room temperature mixers using small anodes and higher N_{epi} (10^{17}). At these high frequencies LO pump power is scarce, so it is crucial that the impedance of the diode match the embedding circuit to make best use of the available power.

2.2.4 Packaging Parasitics

The diode circuit, as presented in Figure 2.5, neglects "packaging" parasitics. The planar diode realistically contains additional parasitic terms as shown in Figure 2.9. These terms are thoroughly discussed by Setzer [48] and will, therefore, only be outlined.

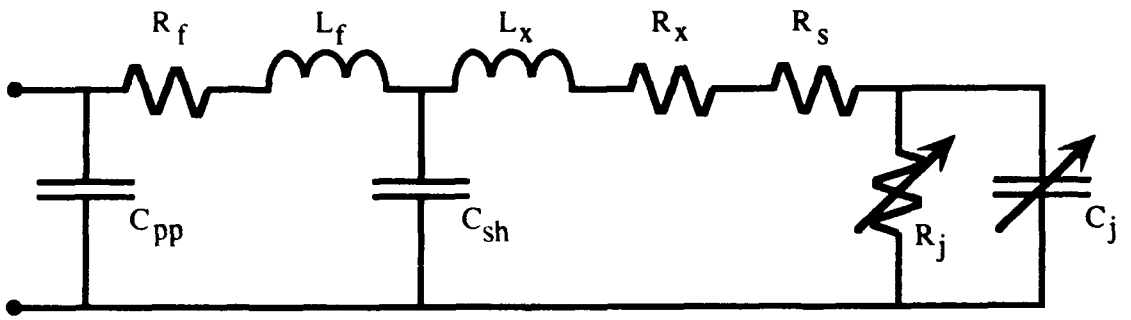


Figure 2.9 Packaging Parasitics of the Planar Diode Chip

The dominant inductance L_f is due to the anode contact finger. Unfortunately, no one formula exists that accurately predicts the values observed in scale model studies. This is discussed further in Chapter 7. The second inductance term L_x is due to the anode. Setzer calculates this inductance as being less than 2.5 pH at 100 GHz [48]. This is small compared to L_f and is neglected in this work.

The capacitance C_{pp} is contributed by the two large bonding pads. It is a function of the pad areas, spacing, and substrate thickness. C_{pp} is best determined from a scale model of the actual waveguide used. Measurements of actual diodes in open space at 1 MHz show C_{pp} to be about 10 fF for 4 mil square pads separated by 2 mils on thick GaAs. Scale model studies indicate that C_{pp} is less than 5 fF for the same geometry in a waveguide. This is discussed further in Chapter 7.

The shunt capacitance C_{SH} is due to the tip of the contact finger and anode. C_{SH} is composed of the four parallel terms shown in Figure 2.10, and is, therefore, equal to the

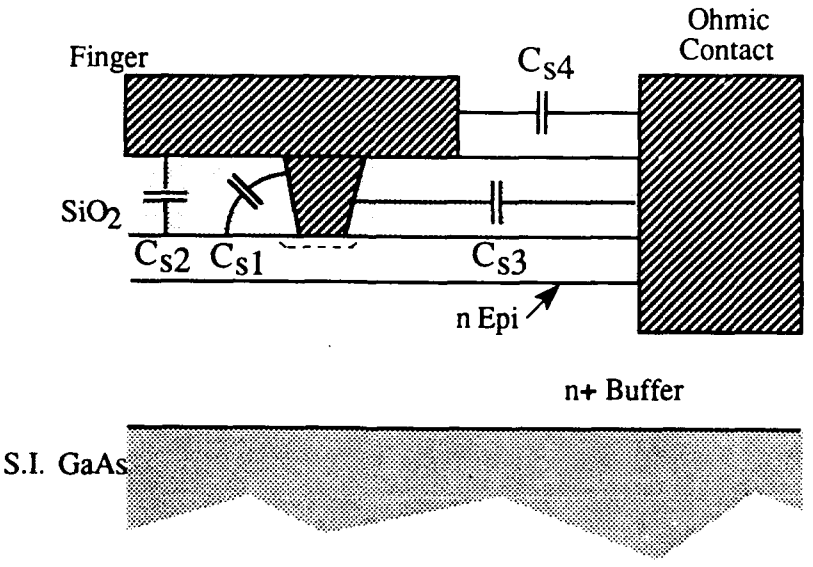


Figure 2.10 Shunt Capacitances of the Anode Contact Finger

sum $C_{SH} = C_{s1}+C_{s2}+C_{s3}+C_{s4}$. The capacitance due to the conical shape of the anode is C_{s1}. It is calculated by Kerr's [52] formula as:

$$C_{s1} = \frac{\pi\varepsilon_0(a_0^2 - b_0^2)^{1/2}}{\arctan\left[\frac{(a_0^2-b_0^2)^{1/2}\tan(\theta_0/2)}{(a_0+b_0)}\right]} \tag{2.20}$$

where:

$$a_0 = r_0 \ln\left(\frac{V_2-r_0}{r_1-r_0}\right)$$

$b_0 = (r_2-r_1)$

r_0 = radius at bottom of anode

r_1 = radius of depletion region

$r_2 = r_o + t_{ox}/\sin\theta$

θ_o = angle between anode cone and GaAs.

Setzer found C_{s2} by field mapping to be [48]:

$$C_{s2} = 2.5\varepsilon_r\varepsilon_o l_e \tag{2.21}$$

where l_e is the length of the finger overlying the active material. Capacitance C_{s3} and C_{s4} are approximated as cylindrical capacitances [48]:

$$C_{cyl} = \frac{2\pi\varepsilon_r\varepsilon_o}{\ln\left[\frac{r_o}{r_i}\right]} \tag{2.22}$$

where r_0 is the radius of the outer cylinder and r_i is the radius of the inner cylinder.

The resistance term R_F is due to the contact finger and given as:

$$R_F = \frac{\rho_{Au} l_f}{A_f} \tag{2.23}$$

where the cross sectional area A_f is the area through which current actually flows. At RF A_f is equal to the product of the cross sectional circumference and the skin depth, δ. R_X is the resistance of the conical anode at RF frequency and is given as:

$$R_X = \frac{\rho_{Au}}{2\pi\delta} \cos(\theta_o) \ln\frac{r_t}{r_o} \tag{2.24}$$

where r_t is the radius of the top of the anode.

2.2.5 Noise Mechanisms

Heterodyne receivers are used to detect extremely weak signals in a significantly noisy background. This is accomplished by observing the signal for a time long enough for the steady signal to stand out from the random background noise. Since the minimum observing time required to detect the signal is proportional to the square of the receiver's noise temperature, it is important to reduce noise within the receiver. Therefore, it is beneficial to reduce the diode's equivalent noise temperature.

Two types of noise are important in Schottky diodes: shot and thermal (Johnson). Shot noise is caused by the random fluctuation in the flow of electrons across the barrier. Thermal noise is associated with the random motion of electrons through the diode's series resistance. Their combined effect is summarized in the equivalent noise temperature, T_n, of the diode. This parameter is defined as the physical temperature a thermal load, of the same small-signal impedance as the diode, must be at to deliver the

same noise power to the circuit. This can be expressed as [49], [51]:

$$T_n = \frac{qV_o}{2k}\,\frac{R_j}{R_j+R_s} + T_e\frac{R_{epi}}{R_j+R_s} + T_o\frac{R_{buffer}+R_{oc}}{R_j+R_s} \tag{2.25}$$

where $T_e = T + KI^2$.

At low biases the first term dominates since R_j is much greater than R_s. This term represents shot noise and is dependent on the inverse slope parameter V_o. The other terms dominate at biases when R_s is much greater than R_j. The effective temperature T_e contains an empirical correction factor K to account for the excess noise in the epitaxial layer at high currents. K is observed to depend on anode diameter and active layer doping density. Hegazi attributes this excess noise to hot electrons. Zirath [51] describes K as:

$$K = \frac{2\tau_e}{3kq\mu N_d^2 A^2} \tag{2.26}$$

where τ_e is the average energy relaxation time of the electrons and μ is their mobility. A is the anode area. Typical noise curves for a Schottky diode at room temperature and 25K are shown in Figure 2.11.

2.3 Heterodyne Receiver

Heterodyne receivers are used to convert the information contained in high frequency signals to lower frequencies where it is easily analyzed. They typically consist of an antenna, a mixer, a set of filters, and an amplifier. One possible configuration of these elements is shown in Figure 2.12. The antenna collects the signal radiation ω_{RF}, which is then coupled into the mixer and mixed with the local oscillator signal ω_{LO}. The mixing process translates the information contained in the RF signal to a much lower

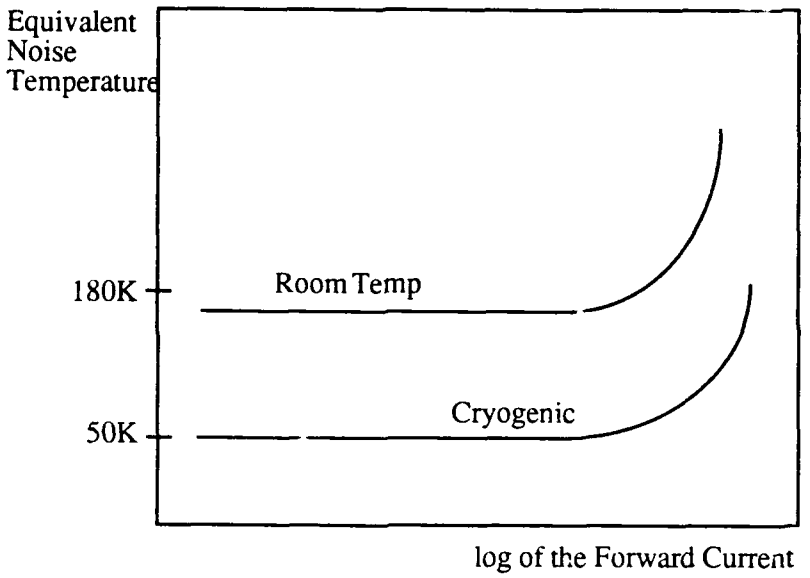


Figure 2.11 Equivalent Diode Noise Temperature of a DC Biased Diode

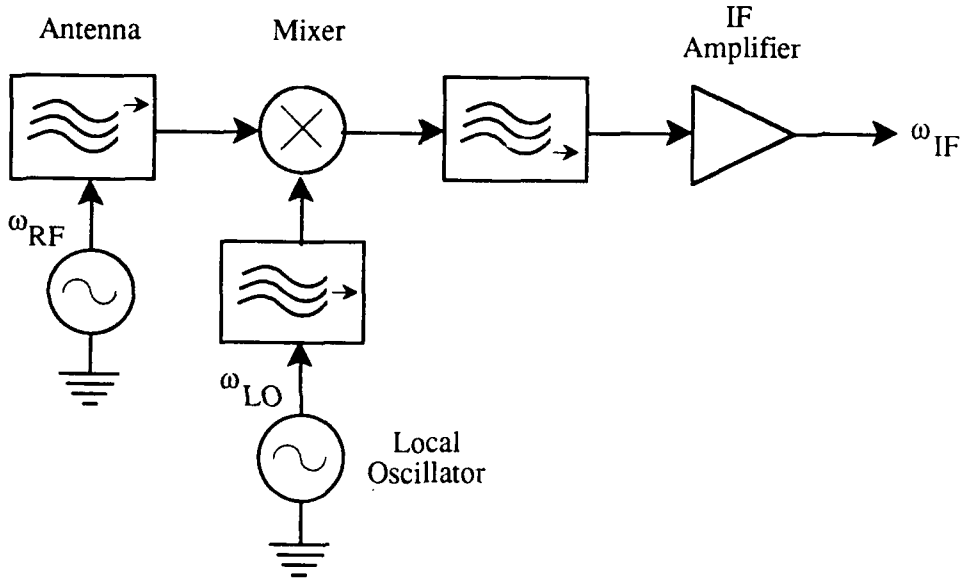


Figure 2.12 Block Diagram of a Heterodyne Receiver

frequency signal referred to as the intermediate frequency ω_{IF}. This mixing process, which is illustrated in Figure 2.13, requires a non-linear element such as a diode. The

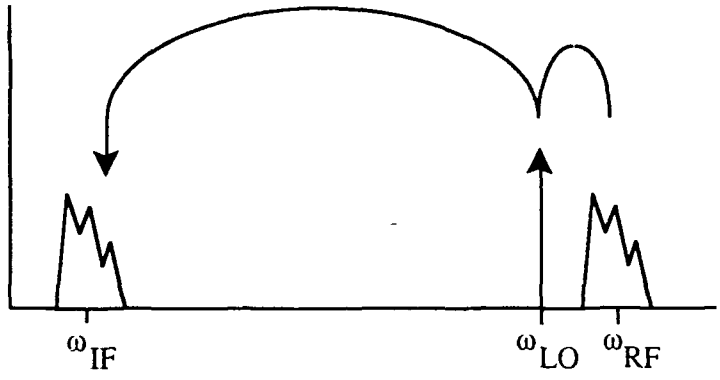


Figure 2.13 Down Conversion of an RF Signal

filters isolate the IF signal for amplification and subsequent processing, and confine the RF and LO power to the vicinity of the diode. Usually, the RF and LO are so close to each other in frequency that they are coupled to the mixer by the same path. Thus, a diplexer is required to combine these signals spatially before they enter the mixer.

The principle of heterodyne reception was first patented in 1902, when Fessenden used a transformer to combine the RF and LO signals, and a diaphragm as the non-linear element. The IF was an audible signal. Armstrong is generally credited with the first super-heterodyne receiver in 1921 which converts the RF to an IF above the audio band. Armstrong used a vacuum triode tube as his mixing element. Super-heterodyne reception was actually patented twice before Armstrong's results were published: by Levy in 1917 (U.S.) and Schottky in 1918 (Germany).

Mixers actually generate copies of the RF signal at a large number of different frequencies. The choice of which copy to use as the IF offers one way to classify mixers. Two types of heterodyne receivers will be examined. The first is the fundamentally pumped mixer, which isolates the difference frequency as the IF: $\omega_{IF} = |\omega_{RF} - \omega_{LO}|$.

This choice typically yields the best overall receiver performance. The subharmonically pumped mixer, on the other hand, is designed to suppress the fundamental response so that the strongest signal containing a copy of the RF is: $\omega_{IF} = |\omega_{RF} - 2\omega_{LO}|$. The diodes fabricated in this research are designed for this type of mixer which, although not the most sensitive, has many important benefits.

2.3.1 Fundamentally Pumped Mixers

Fundamental mixers are used in state-of-the-art, submillimeter wave receivers. They are capable of efficiently converting more RF power into the IF band than any other type of mixer, and have been used at RF frequencies as high as 3000 GHz. The fundamental mixer is discussed below to introduce the mixing phenomena and related terminology before analyzing the subharmonically pumped mixer in the next section.

The process of mixing can be illustrated by expanding the *I-V* characteristic of the non-linear mixing element in a power series [53]. Consider the circuit shown in Figure 2.14 which consists of one nonlinear element A, and a zero impedance source. Suppose

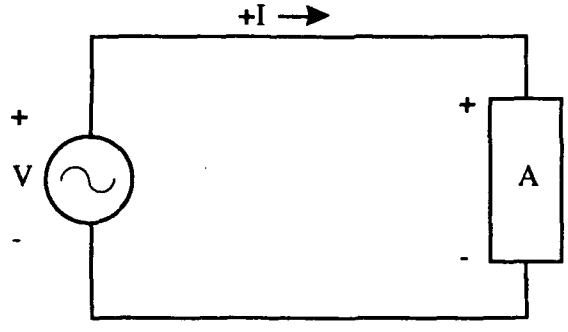


Figure 2.14 A Single Non-Linear Element Circuit

the *I-V* characteristic of element A can be described by the three term power series:

$$I = aV + bV^2 + cV^3 \tag{2.26}$$

where V is the voltage impressed across the element's terminals by the source V_S. If V_S is the sum of two waves at frequencies, ω_1 and ω_2 (eg. $\omega_{RF} = \omega_1$ and $\omega_{LO} = \omega_2$):

$$V_S = V_1\cos\omega_1 t + V_2\cos\omega_2 t \tag{2.27}$$

then (2.26) can be expressed as:

$$I = I_1(t) + I_2(t) + I_3(t) \tag{2.28}$$

Where the use of standard trigonometric identities yields:

$$I_1(t) = a(V_1\cos\omega_1 t + V_2\cos\omega_2 t) \tag{2.29}$$

$$I_2(t) = \frac{b}{2}\{V_1^2 + V_2^2 + V_1^2\cos 2\omega_1 t + V_2^2\cos 2\omega_2 t + 2V_1V_2[\cos(\omega_1 - \omega_2)t + \cos(\omega_1 + \omega_2)t]\} \tag{2.30}$$

$$I_3(t) = \frac{c}{4}\{3(V_1^3 + 2V_1V_2^2)\cos\omega_1 t + 3(V_2^3 + 2V_1^2V_2)\cos\omega_2 + V_1^3\cos 3\omega_1 t + V_2^3\cos 3\omega_2 t + 3V_1^2V_2[\cos(2\omega_1 + \omega_2)t + \cos(2\omega_1 - \omega_2)t] + 3V_1V_2^2[\cos(2\omega_2 + \omega_1)t + \cos(2\omega_2 - \omega_1)t]\} \tag{2.31}$$

Careful examination of each contribution reveals several important points. First, the non-linear element has produced a DC current and signals at ten new frequencies, each is a linear combination of ω_1 and ω_2 as:

$$\omega_{m,n} = m\omega_1 + n\omega_2 \tag{2.32}$$

where m,n = ...-3,-2,-1,0,1,2,3,... These mixing products will be referred to as being of

order (|m| + |n|). The important point in this analysis is that the even and odd mixing products are produced by specific terms of the power series expansion of the *I-V* response. The fundamental mixing response ($\omega_1 - \omega_2$) can only be produced by the even power terms (ie. bV^2) of this expansion. The off power terms (aV, cV^3) produce only the odd order mixing products. This will be important for the subharmonically pumped mixer discussed later.

Important parameters that describe the performance of mixers are the conversion loss, L, and the mixer equivalent noise temperature, T_m. Conversion loss is the ratio of the average power available from the RF source to the average signal power converted to the IF band and delivered to the IF load. Conversion loss is always greater than unity for classical resistive mixers using Schottky diodes. The SSB equivalent mixer noise temperature is the temperature required of a matched impedance at the signal ($\omega_{LO} + \omega_{IF}$) port of an equivalent, but noiseless, mixer to deliver the same noise power to the IF load as the actual mixer does. T_m is sometimes presented as a noise figure F (in dB):

$$F = 10 \log \left[\frac{T_m}{290} + 1 \right] \tag{2.33}$$

2.3.2 Subharmonically Pumped Mixers

Harmonic mixers are designed to allow only the sidebands of a harmonic of the LO, $n \cdot \omega_{LO}$ (n=2,3,4,...) to respond at ω_{IF} so that $\omega_{IF} = \omega_{RF} - n\omega_{LO}$. The n=2 harmonic mixer, shown in Figure 2.15, is often referred to as being "subharmonically pumped."

The concept of subharmonic pumping was mentioned by Büchs in 1971, when he built a 10 GHz RF mixer pumped by a 5 GHz LO using planar beam lead diodes [16]. In

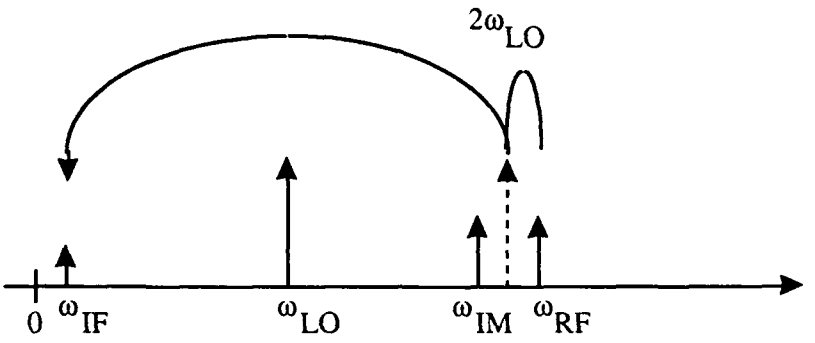


Figure 2.15 Mixing with the Second Harmonic of the LO

1974, Schneider and Snell built a 3.5 GHz RF mixer and Cohn et al. built a 12 GHz RF and a 55 GHz RF mixer [18]. McMaster, Schneider, and Snell produced a 95 GHz RF subharmonically pumped mixer in 1976 [54]. Then in 1978, Carlson et al. used notch front diodes to achieve a SSB mixer temperature of 400K at 98 GHz, comparable to the best fundamentally pumped mixers [47]. Planar beam lead diodes were attempted in this mixer yielding a SSB T_m of 1600K while requiring 10 dBm more LO power than the whiskered notch-front diodes. This degraded performance was attributed to the 60 to 75 fF of parasitic capacitance in the diodes.

Single diode mixers have often been used in harmonic mixers. However, since their fundamental mixing response is great, a significant amount of RF power is converted to a sideband of the LO and is then lost in the LO circuitry. This unwanted response can be eliminated by using a mixing element containing only odd terms in its *I-V* characteristic. An anti-parallel pair of diodes has an antisymmetric *I-V* characteristic (shown in Figure 2.16) containing only odd order terms in its power series expansion. Thus mixing with the fundamental is suppressed, and more RF power can be converted to the IF band.

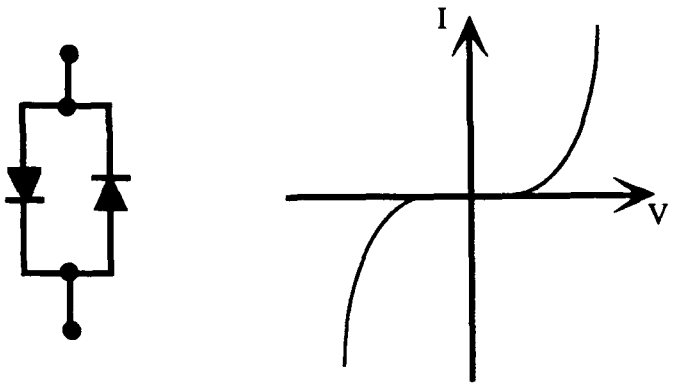


Figure 2.16 *I-V* Characteristic of Anti-parallel Diodes

Consider the circuit shown in Figure 2.17 which contains an anti-parallel pair of identical non-linear elements. The non-linear currents of elements 1 and 2 are expanded as:

$$I_1 = f(V) = aV + bV^2 + cV^3 + dV^4 + eV^5 + \cdots \tag{2.37}$$

$$I_2 = -f(-V) = aV - bV^2 + cV^3 - dV^4 + eV^5 + \cdots \tag{2.38}$$

Notice that the polarity of the second element is reversed, but the sign convention of the

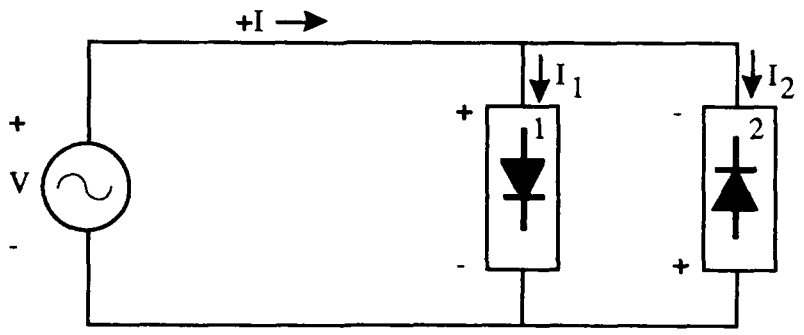


Figure 2.17 A Circuit Containing an Anti-parallel Pair of Non-Linear Elements

current and voltage is the same as for the first element. The total current external to the diode loop is then:

$$I = I_1 + I_2 = 2aV + 2cV^3 + 2eV^5 + \cdots \tag{2.39}$$

We can see then that the *I-V* response of a perfectly matched anti-parallel pair of non-linear elements contains only odd powers of the voltage. Therefore, only odd degree components are present in the external current so only odd order mixing products are generated.

The even degree components are only important internal to the diode loop, where the loop current is:

$$I_{loop} = -I_1 = I_2 = bV^2 + dV^4 + \cdots \tag{2.40}$$

The even order terms survive now since their coefficients have opposite signs in I_1 and I_2. The coefficients of the odd degree components have the same sign in I_1 and I_2, and therefore must be zero since $a \neq -a$, $c \neq -c$, $\cdots$. So the even order currents and mixing products circulate within the loop, while the odd order currents circulate outside. Therefore, there can be no even order voltages across the diode pair. This means that each diode effectively shorts the other at all even order mixing frequencies [53].

In many situations the fundamentally pumped mixer will not have enough LO power to achieve good performance. In such cases the subharmonically pumped mixer will yield vastly improved performance if adequate LO power is available at $\frac{\omega_{RF}}{2}$. However, the minimum possible conversion loss of a subharmonically pumped mixer is always greater than that of an equivalent fundamentally pumped mixer with adequate LO power. Their poorer performance is explained by examining the conductance waveforms

of each diode in the mixer.

The conductance of each diode can be approximated as a rectangular pulse of length t_g ($t_g = 0.22G_{max}$) [55], as shown in Figure 2.18. This is equivalent to replacing the diode with an ideal switch. Barber [55] has shown that the conversion loss of such a mixer is proportional to the square of the average value of conductance G_{avg}, and that both conversion loss and noise are reduced by minimizing the pulse duty ratio. Büchs and Begemann [56] have extended Barber's approach to multi-diode mixers. They treated a mixer with M diodes as a parallel combination of M single diode mixers, each fundamentally pumped at a frequency $\frac{\omega_{LO}}{M}$ and appropriately phased. Figure 2.19 shows the pulsed conductance waveforms of a two diode, subharmonically pumped mixer. The conductance of each diode is separated from the other by 180° in phase, and add together to create conductance waveform of the subharmonically pumped mixer. Notice that the conductance waveform of each diode has a minimum value G_{min}. This value depends upon the *I-V* characteristics of the diode, and is independent of the pump

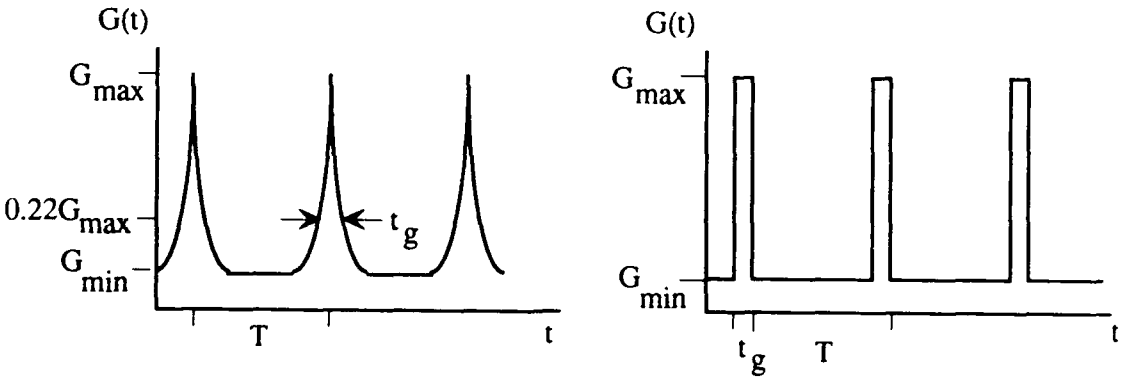


Figure 2.18 A Rectangular Pulse Model of the Diode's Conductance

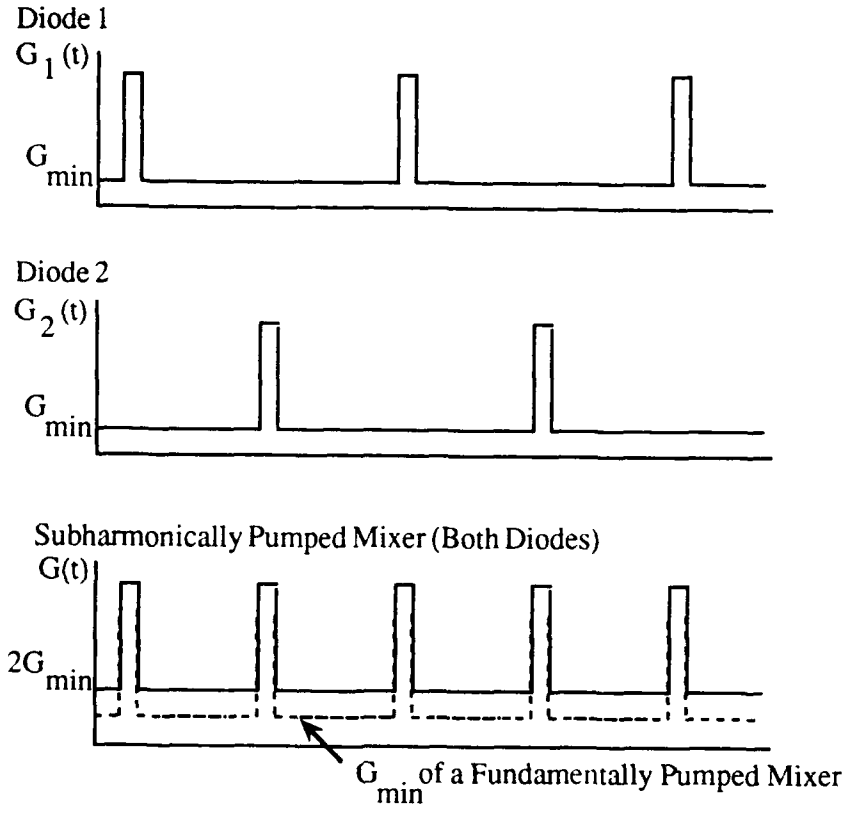


Figure 2.19 The Conductance Model for a Circuit with 2 Diodes

frequency. Since it is assumed that all diodes in this discussion are identical, each has the same value for G_{min}. The G_{min}'s of the two diodes add, making the minimum conductance value of the subharmonically pumped mixer equal to $2G_{min}$. The conductance waveforms of both the fundamentally pumped and subharmonically pumped mixers, both operating at the same RF frequency, have the same number of conductance pulses in any given time interval. This means that the conductance waveform of the subharmonically pumped mixer is identical to that of the fundamentally pumped mixer, except for the larger minimum conductance. The dashed line in Figure 2.19 indicates the lower G_{min} of the fundamentally pumped mixer. This means that the subharmonically

pumped mixer has a greater G_{avg}, and therefore experiences greater conversion loss than a fundamentally pumped mixer.

However, a subharmonically pumped mixer allows less LO noise to contribute to the mixer's total noise than a single diode mixer. Figure 2.20 shows a noisy LO and the sidebands that can be down converted for fundamental and subharmonic mixing. The width of the LO's spectral noise density curve is exaggerated. If the diodes are perfectly matched, the fundamental mixing response is eliminated and only the noise in the sidebands near $2\omega_{LO}$ is down converted. In reality, the diodes are not perfectly matched, so the antisymmetry of the mixer is degraded. Therefore, some LO noise near ω_{LO} will end up in the IF. However, this contribution is significantly less than the noise down-converted by a fundamentally pumped mixer. Henry et al. have shown that if a diode mismatch allows a DC current, then the ratio of LO noise contributions P_{LO} in the

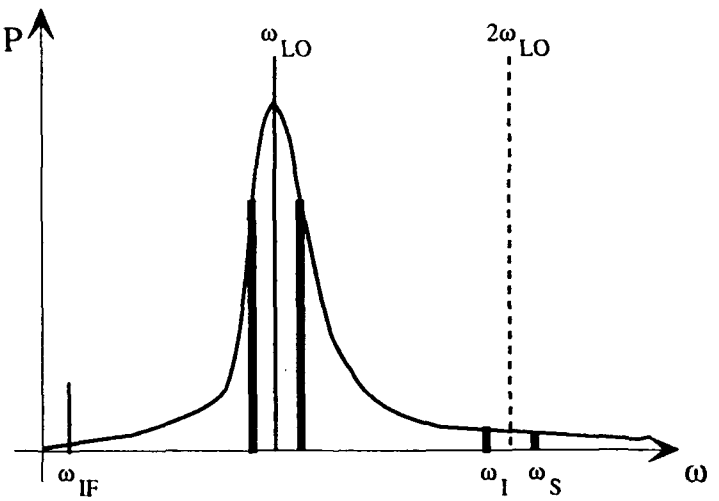


Figure 2.20 LO Noise Contribution to the IF

sidebands near ω_{LO}, to the LO noise contributions P_{2LO} near $2\omega_{LO}$ is [57]:

$$\frac{P_{LO}}{P_{2LO}} = \left[2\frac{I_{DC}}{I_{LO}} \cdot \frac{\omega_{LO}}{\omega_{IF}}\right]^2 \tag{2.49}$$

This suggests that mismatches have an enhanced effect at high frequencies.

Other advantages of the subharmonically pumped mixer include the self protection against large reverse currents offered by the anti-parallel diode configuration. Also, subharmonically pumped mixers require no external diplexer to combine the RF and LO signals. This results in simpler circuits that can be operated over wider IF bandwidths.

Subharmonically pumped mixers also have other disadvantages besides their poorer conversion loss. For example, the simple circuit is difficult to realize with whisker contacted diodes, particularly since the diode characteristics and parasitic impedances must be well matched. Also, the diodes are usually operated with no DC bias. Therefore, they require larger amounts of LO power than single diode mixers, although at much lower frequency. To gain the full benefit of subharmonic pumping, it would be useful to have diodes that are DC biased or have a reduced barrier height. Both of these disadvantages can be overcome with the use of integrated planar diodes.

2.4 Summary

This chapter presented the theory applicable to both the Schottky barrier diode and its use in subharmonically pumped mixers. This presentation began with a discussion of the Schotty barrier, and the transport of charge across this rectifying barrier. Circuit models were then presented to illustrate the junction parameters and parasitics that affect mixing. Next, the noise mechanisms within the diode were discussed. Then, theory relevant to fundamentally and subharmonically pumped mixers was presented.

CHAPTER 3

PLANAR TECHNOLOGY

3.1 Introduction

This chapter introduces planar diode technology by first comparing the strengths and weaknesses of planar and whiskered diodes. Then, a variety of planar diode structures are overviewed, with particular emphasis on the technological problems inherent in each. Finally, the development of the Surface Channel diode at the University of Virginia is reviewed.

3.2 A Comparison of Planar and Whiskered Diodes

The structure of a whisker contacted diode chip is shown in Figure 3.1. It consists of a "honeycomb" array of anodes on its top surface and an ohmic contact on the bottom surface. Between are a thick, highly doped (n-type) substrate and a thin, moderately doped epitaxial layer. The anodes are defined photolithographically in a thin insulating film of silicon dioxide.

To use this device, the user bonds the ohmic contact to the circuit and uses a thin, pointed wire "whisker" to contact one of the anodes, as shown in Figure 3.2. The large number of closely spaced anodes ensures that a randomly placed whisker will have a high probability of contacting one of the anodes. The anode array also adds redundancy, which is important should the anode become damaged.

The electrical circuit used to model the whiskered diode is presented in Figure 3.3. The variable junction resistance (R_j) is the important parameter for mixing, while the junction capacitance (C_j) and the series resistance (R_s) are parasitics that degrade

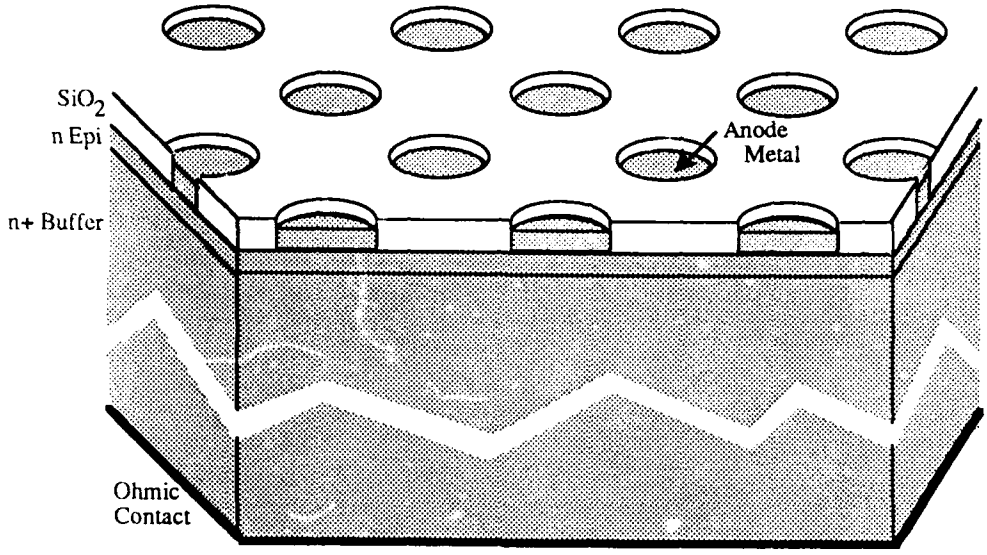


Figure 3.1 The Whisker Contacted Diode Chip

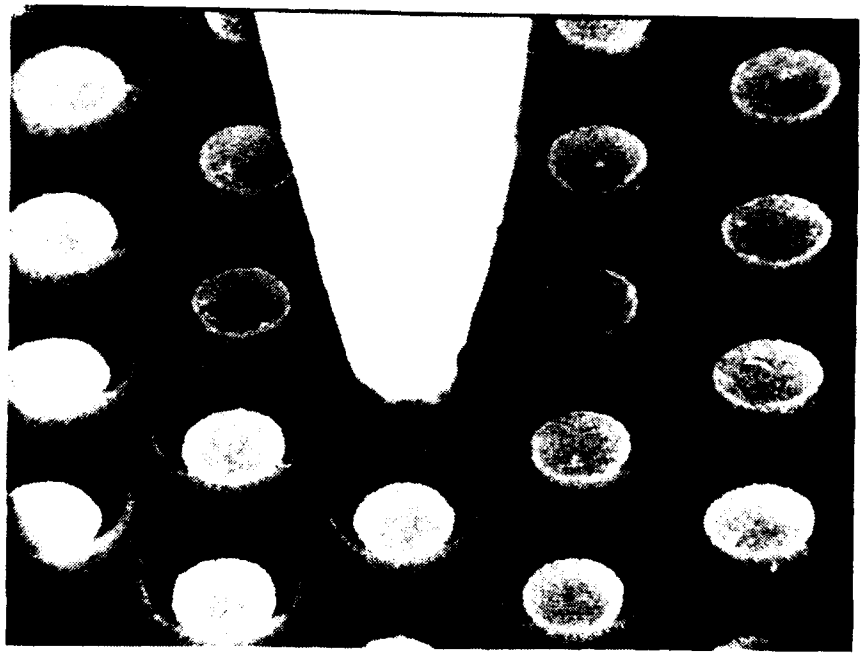


Figure 3.2 A Whisker Contacted to a Single Anode

performance. Additional parasitics associated with this technology includes the series inductance L_S and shunt capacitance C_{SH}. The geometry of a thin wire whisker perpendicular to a conducting plane of GaAs offers the lowest shunt capacitance possible. A 2.5 μm anode may typically have a C_{SH} of 3 fF or less [48]. The self inductance of the whisker can be large (>300 pH) for long whiskers, but is controlled by the microwave engineer who designs the diode mount.

There are several advantages associated with the whisker contacted diode. Its simple fabrication technology requires only one photolithography step on a planar

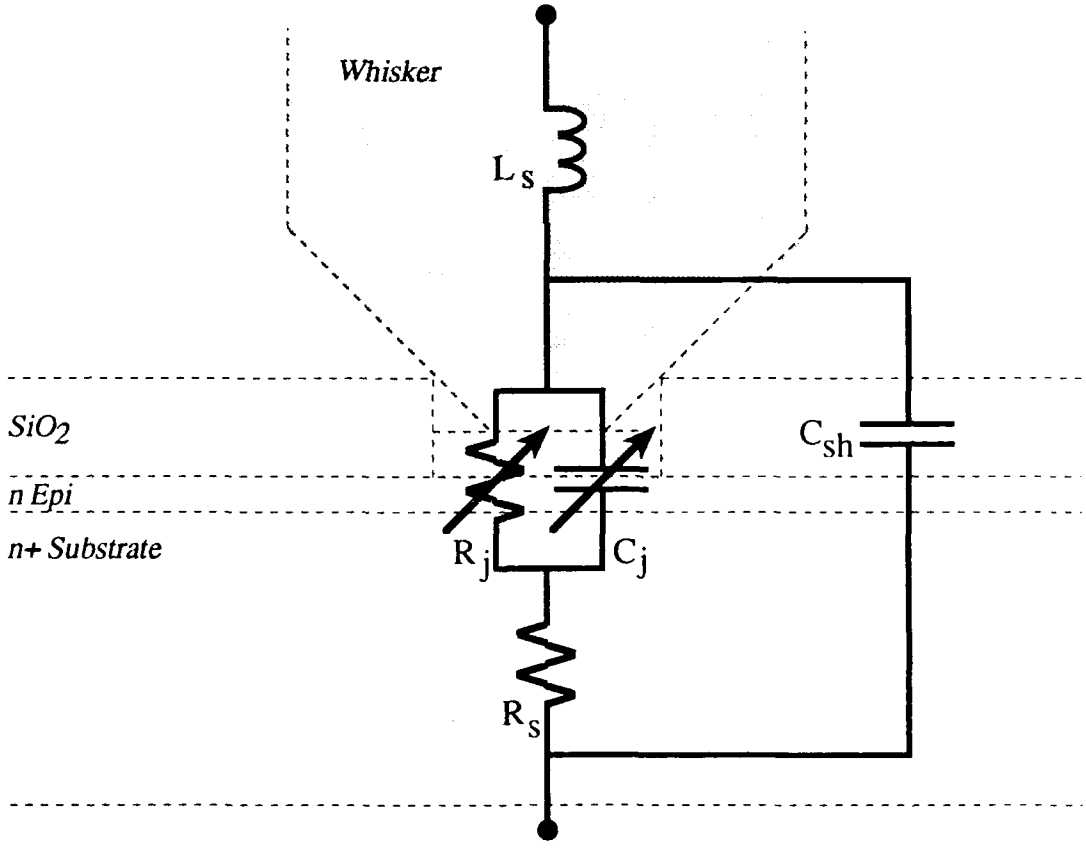


Figure 3.3 A Circuit Model for a Whisker Contacted Diode

surface. Therefore, small anodes can be created. Also, the large number of anodes on a chip supply great redundancy. Furthermore, the use of a whisker offers a low shunt capacitance and control of series inductance. These factors work to make the whisker contacted diode the best available for submillimeter wavelength frequencies, allowing their use at frequencies as high as 3 THz.

The whiskered diode does have its disadvantages however. Considerable time and expense are required to contact the anode. Also, the nature of the contact raises reliability concerns, particularly for space applications. Finally, it is difficult to assemble multi-diode mixers with matched anode characteristics.

Planar technologies are attractive since they eliminate the fragile whisker, making the diode rugged and easy to use. Furthermore they allow assembly of multi-diode mixers with matched diode characteristics. On the other hand, the fabrication of planar diodes is a complicated process. Also, no redundancy is offered since the diode has only one anode. However, the main disadvantage of planar diodes is the large shunt capacitance which has limited their usefulness at high frequencies.

In its simplest form, the planar diode consists of the Schottky anode, an anode contact finger leading to a bonding pad, and an ohmic contact pad as shown in Figure 3.4. Both pads are on the top surface of the chip and therefore must be electrically isolated from each other. The circuit used to model the planar diode is shown in Figure 3.5. Again, the Schottky junction is modeled by a variable conductance, and a variable capacitance. A series resistance caused by the undepleted epitaxial layer, the spreading of current in and resistance of the buffer layer, and the ohmic contact. The series inductance associated with the finger can be less than 50 pH since the finger is short. The

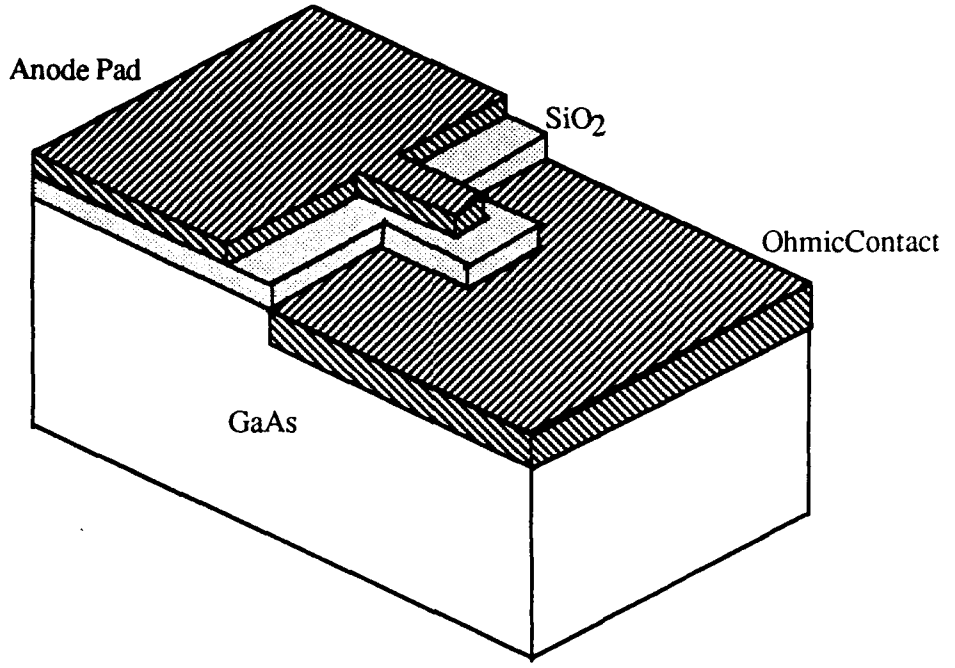


Figure 3.4 A Generic Planar Diode

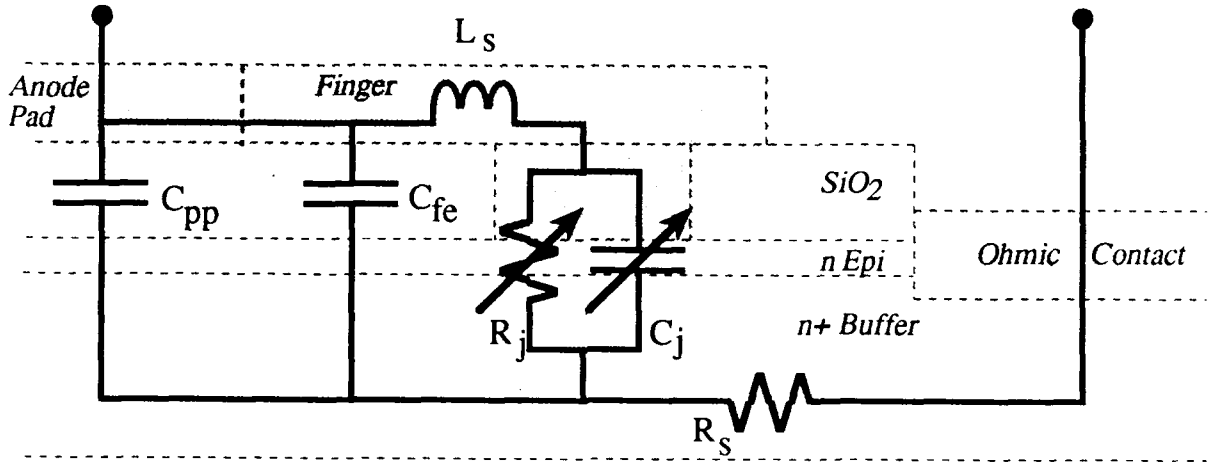


Figure 3.5 A Circuit Model for the Generic Planar Diode

major shunt capacitances due to the pads C_{pp} and the finger overlying active material C_{fe} were discussed in section 2.2.3. Typical values are 10-20 pF for C_{pp} and 1 fF for

C_{fe}. The variety of planar diodes discussed below involve different ways to electrically isolate the two pads, while reducing the pad-to-pad capacitance.

3.3 Planar Technologies

The primary design goal of a planar technology is to eliminate the conduction between the pads and to minimize shunt capacitances, while keeping the diode fabrication simple. A great variety of planar technologies have been proposed. Each succeeds in insulating the pads, but the shunt capacitance achievable, and processing complexity make some designs undesirable. Six basic technologies, including the Surface Channel, are outlined below.

Dielectric Isolation

The simplest technique is to separate the pads by an insulating film as depicted in Figure 3.4. Although this technique will isolate the pads at DC, the large anode pad forms a parallel plate capacitor with the active GaAs underneath. This capacitance, which can be of order 1000 fF, will shunt the diode junction at millimeter wavelengths, making the diode useless for RF applications.

Selective Crystal Growth

Selective crystal growth techniques can be used to isolate the bonding pads by growing conductive GaAs only in the region where the anode and ohmic contact will reside. This technique was used by Allen and Antell in 1973 to create the first planar GaAs diodes for use at millimeter wave frequencies (60-80 GHz) [58]. In 1973 Ballamy and Cho also fabricated planar diodes used at 103 GHz in selectively grown material [59]. First, a thin SiO_2 film is deposited on a semi-insulating substrate. Then

photolithography and etching are used to mask the substrate regions where the anode pad is to be formed as shown in Figure 3.6.

Then the substrate is etched, removing several microns from the region where the anode and ohmic contact are to be formed. Next, molecular beam epitaxy (MBE) is applied over the nonplanar surface to grow the n^+ buffer and n epilayer in the etched regions. The polycrystalline GaAs grown over the SiO_2 is removed by etching the SiO_2 out from under it. The diode is then fabricated in a conventional fashion yielding a cross section as shown in Figure 3.7.

This provides a planar surface for the photolithographic formation of small anodes. Also, the fabrication technology is fairly simple after the conductive GaAs has been grown. However, the selective growth of high quality GaAs is difficult, and requires access to a MBE machine.

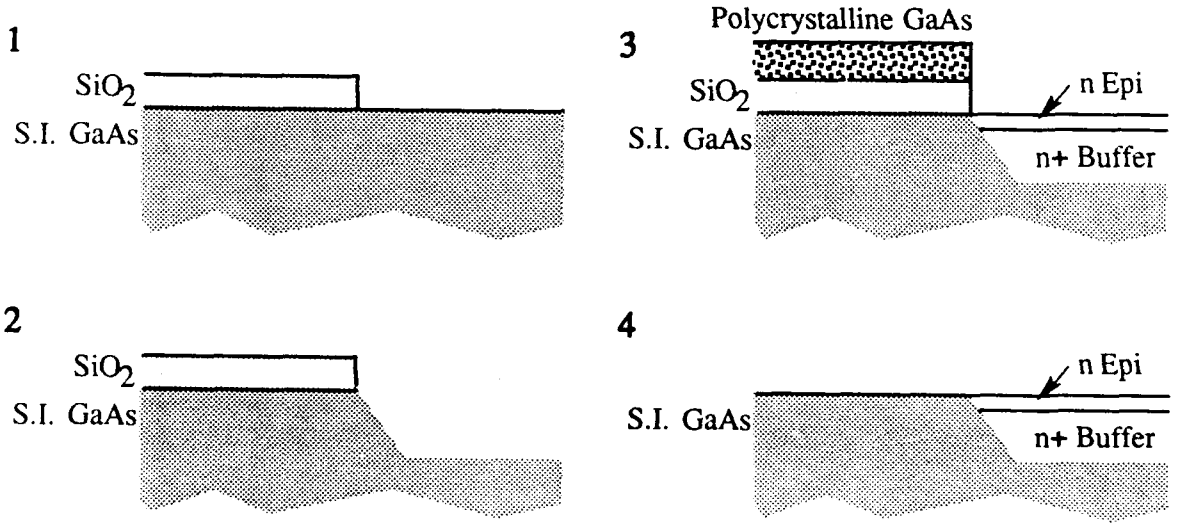


Figure 3.6 Wafer Fabrication using Selective Crystal Growth

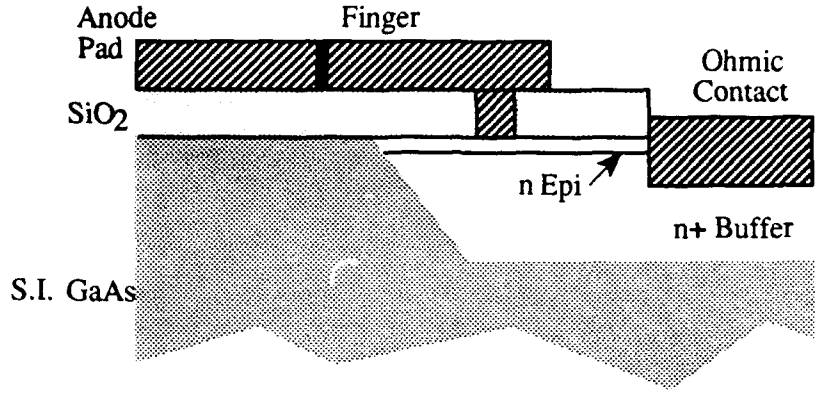


Figure 3.7 The Selective Crystal Growth Technology

Proton Bombardment

This technique involves the use of a high energy beam of protons to render portions of the GaAs epitaxial layer semi-insulating. The diode shown in Figure 3.8 is first fabricated on conductive GaAs on a semi-insulating substrate. Then a thick layer of gold is used to protect the anode and ohmic contact from the proton beam. The areas exposed to the beam become heavily damaged, greatly reducing the conductivity. The parasitic capacitance C_{pp} is a fringing field capacitance, typically less than 20 fF. In 1977 Murphy et al. used this technique to demonstrate the beating of two submillimeter waves (668 GHz) in a planar diode [60]. Anderson et al. also used proton bombardment in 1981 to fabricate an anti-parallel pair of diodes for use at 60 GHz [61]. Then in 1985 Cronin and Law used proton bombarded diodes in a 90-110 GHz mixer [62].

The main problem with proton bombardment is the need for a very high proton energy in order to damage the entire epitaxial layer. This equipment is not available in most research labs, and the cost and delay of sending samples to an external lab is prohibitive.

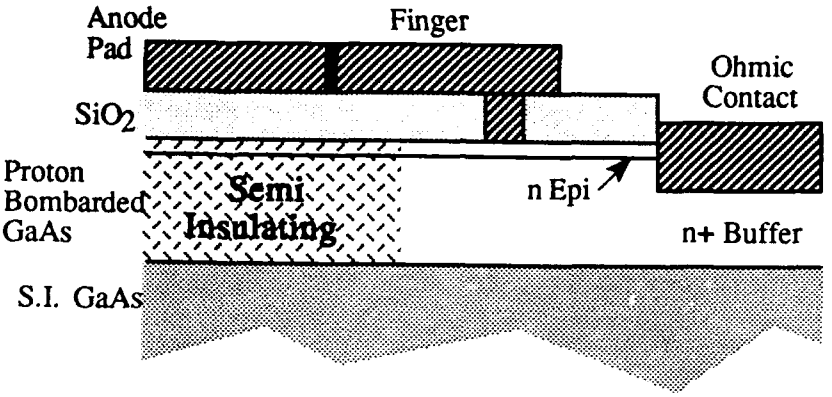


Figure 3.8 The Proton Bombardment Technology

Mesa

The mesa technology uses a simple etch step to remove the conducting GaAs from below the anode contact pad area. This leaves a mesa whose height is several microns. A thick dielectric film is then deposited over the GaAs to separate the anode contact metallization from the conductive GaAs exposed in the mesa wall. Next, the anode pad is placed over the dielectric and semi-insulating GaAs at the bottom of the mesa. The anode and ohmic contact are placed at the top, as shown in Figure 3.9.

A mesa technique is used today by Archer et al. [15] to fabricate excellent diodes that have been incorporated in hybrid integrated circuit mixers at 33-50 GHz and monolithic MIC subharmonic mixers for 75-110 GHz. However, coverage of the large step height of the mesa requires the use of thick photoresist, which makes it very difficult to fabricate submicron anodes. This difficulty makes the mesa technology incompatible with submillimeter wavelength applications.

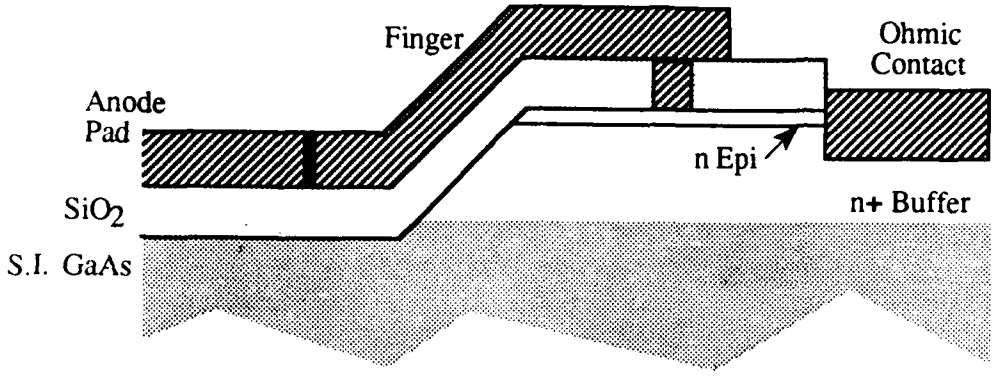


Figure 3.9 The Mesa Technology

Dielectric Fill

The fifth technology isolates the anode pad by using a liquid dielectric to fill regions where the conductive GaAs have been removed. This technique makes the nonplanar mesa technology planar, allowing submicron photolithograhpy. It was used by Mills et al. to fabricate diodes used at 94 GHz [63]. Their device is shown in Figure 3.10. First, photolithography is used to pattern an SiO_2 mask that allows the conductive GaAs to be etched away, forming 25 μm high steps. Then a liquid glass-powder solution is spun onto the wafer filling the etched areas. The wafer is then sequentially heated to remove the solvent and binder, and then to glassify the film. The anode is then formed conventionally. When finished, the wafer is thinned chemically until the glass regions are visible from the back.

The fabrication of planar diodes is complicated by the different thermal properties of SiO_2 and GaAs. The use of liquid glass, which requires a three stage bake, is not compatible with the alloyed ohmic contact technology used at SDL. Also, concerns exists regarding the physical integrity of the device at cryogenic temperatures.

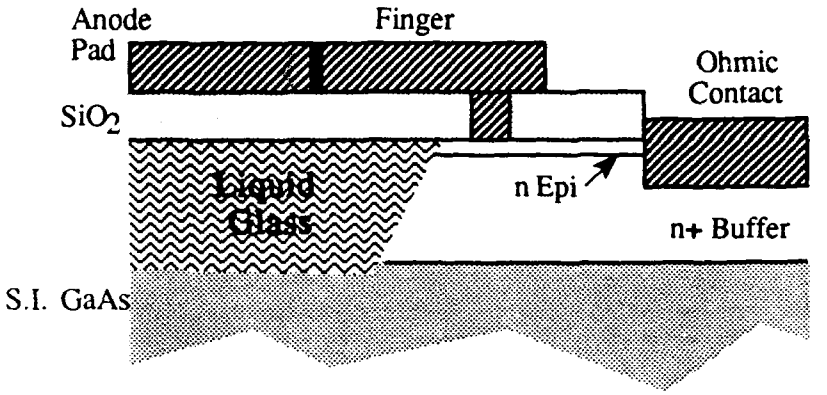


Figure 3.10 The Dielectric Fill Technology

Surface Channel

Our planar diode technology uses a trench or a "surface channel" to remove the conducting material between the anode and the anode pad. The channel breaks the conduction path between the anode and ohmic contact pads. Notice that the Surface Channel diode, shown in Figure 3.11, has the anode pad over a conductive layer of GaAs and, therefore, a large C_{pp1}. However, this capacitance is in series with a small fringing field capacitance C_{pp2} between the pads, resulting in a low total C_{pp}, typically between 10 and 20 fF. This technique was used by Calviello in 1981 to form an anti-parallel pair of diodes for use in a subharmonically pumped mixer at 95 GHz [64]. The SDL independently developed a "Surface Channel" technology in 1986 that produces diodes used in fundamental mixers at 100 GHz. These diodes have performed as well as whisker contacted diodes.

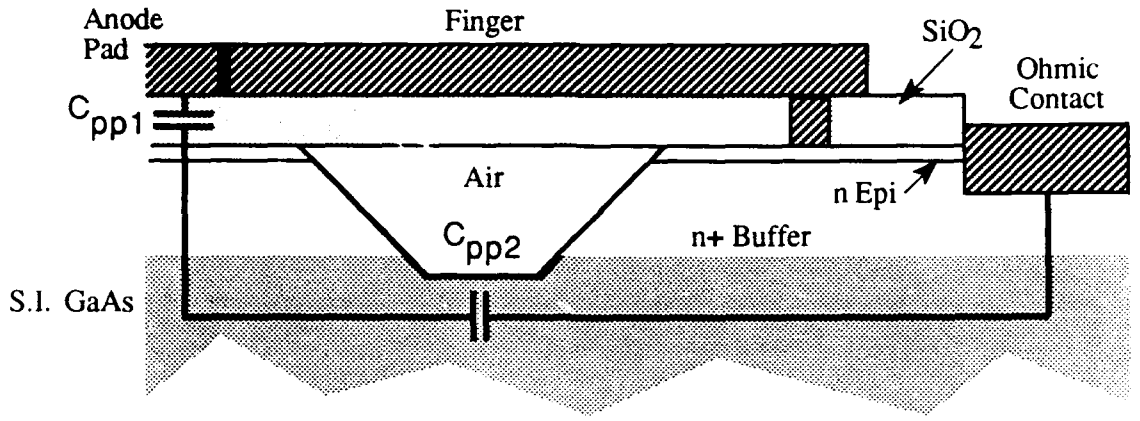


Figure 3.11 The Surface Channel Technology

3.4 Development of Planar Diodes at U.Va.

The Initial Flip-Chip Technology

The first attempts at fabricating planar diodes at the University of Virginia's Semiconductor Device Laboratory were begun in 1977 and are discussed by Setzer [48]. This device was based on a design proposed by Schneider of Bell Labs. In reality, it was a whiskered diode, with an ohmic contact on half of the top surface. The device had no anode contact or anode contact soldering pad. The chip is presented in Figure 3.12, and consisted of one bonding pad and a linear array of anodes. Used as a "flip chip", the diode was inverted and soldered onto a stripline circuit gap as shown in Figure 3.13. The cathode pad was soldered to the broad side of the gap, while the anode was soldered to a narrow extension of the stripline on the other side of the gap. This mounting technique required a special jig for alignment. The soldering was possible because the cathode pad, anode, and both sides of the stripline gap were plated with pure indium over gold.

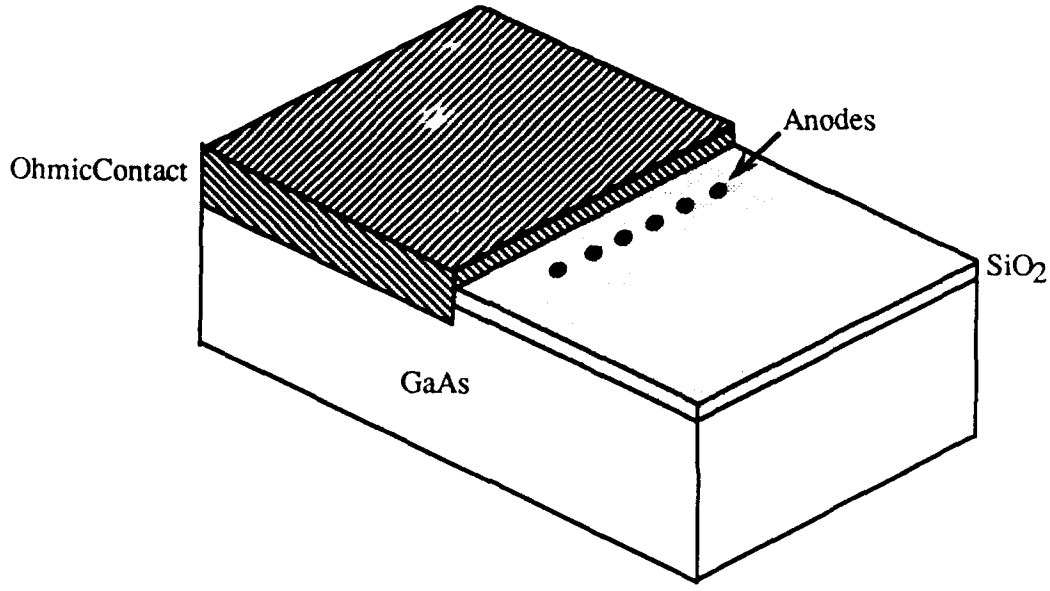


Figure 3.12 The Setzer Flip Chip

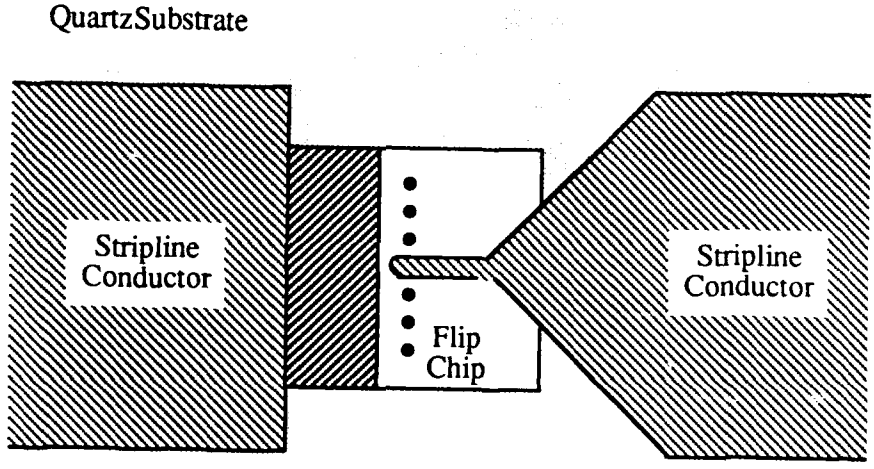


Figure 3.13 The Setzer Flip Chip Mounted on a Stripline

Setzer's anodes exhibited good electrical characteristics when tested with a whisker, and after mounting to the stripline. However, the ΔV changed from 67 to 72 mV during

bonding. The anodes were two microns in diameter, plated on an epitaxial layer doped to 9×10^{16} cm^{-3}, and had a cutoff frequency of 3.2 THz. They were formed by etching with a 92% CF_4, 8% O_2 plasma completely to the underlying GaAs. The ohmic contact pads were covered with photoresist during pulse plating. Having demonstrated the planar concept, this approach was not pursued in later efforts.

Selective Crystal Growth, Dielectric Fill, and a Mesa Technology

The SDL's next effort in planar technology is described in Blanton's 1984 thesis [46]. Both a selective crystal growth and liquid glass technologies were considered. The selective crystal growth approach was dropped after receiving samples grown by Molecular Beam Epitaxy (MBE) with poor crystal morphology. The liquid glass approach seemed feasible but concerns existed regarding the mechanical properties of the glass. It was felt that extensive mechanical characterization of the glass was first required. Blanton next tried the mesa approach discussed above, but experienced problems with photoresist coverage over the mesa. Finally, work on a proton bombarded technology was begun. No complete diodes were fabricated in this study of possible planar diode technologies.

Proton Bombardment

The results of the SDL proton bombardment technology are published in McKinney's 1986 thesis [65]. Bishop [66] and McKinney used the photolithography mask set design for Blanton's mesa structures until September 1985. Anodes were again plasma etched to bare GaAs. Photolithography was used to mask the ohmic contact pads, requiring a 180°C, 90 minute oven bake to harden the resist before plating. This

technology yielded poor quality anodes. After forming the anode contacts and anode pads, a gold mask was deposited and the samples were proton bombarded at MIT Lincoln Laboratories. Lincoln Labs annealed the first set of samples after bombardment as part of their usual procedure. Unfortunately, this destroyed the anodes under the gold mask. Although the next set of samples sent to Lincoln Labs were bombarded successfully, this technology was abandoned due to lack of in-house process control.

Mesa Technology II

Blanton's mesa technology was then revisited. This time a more viscous photoresist (AZ-4330) successfully covered the mesa. Also, the anode formation process was altered in an attempt to achieve better electrical characteristics. A thin undoped oxide was first grown over the GaAs. Then a thick boron doped oxide. The faster plasma etch rate of the boron doped oxide allowed it to be removed, leaving the thin undoped oxide at the bottom of the hole to protect the GaAs until the anodes were ready for plating. This thin layer was removed immediately before the anodes were electroplated by wet etching in BHF. Bishop fabricated a batch of good devices using this technique. Another mask set was then designed for a new mesa device. At this time, Bishop proposed forming an airbridge by rotating the crystal 90 degrees. This causes the GaAs mesa to be undercut, allowing a photoresist fillet to electrically isolate the anode contact finger from the active epi as illustrated in Figure 3.14. Also, the boron doped oxide was not used. Instead, a thick undoped oxide was grown. The anode holes were then wet etched at a known rate to leave a thin oxide at the bottom of the holes. Bishop successfully fabricated a batch of devices [66]. However, this technology was abandoned for two reasons. First, the anode pad was formed directly on semi-insulating GaAs, and acted as a large Schottky contact.

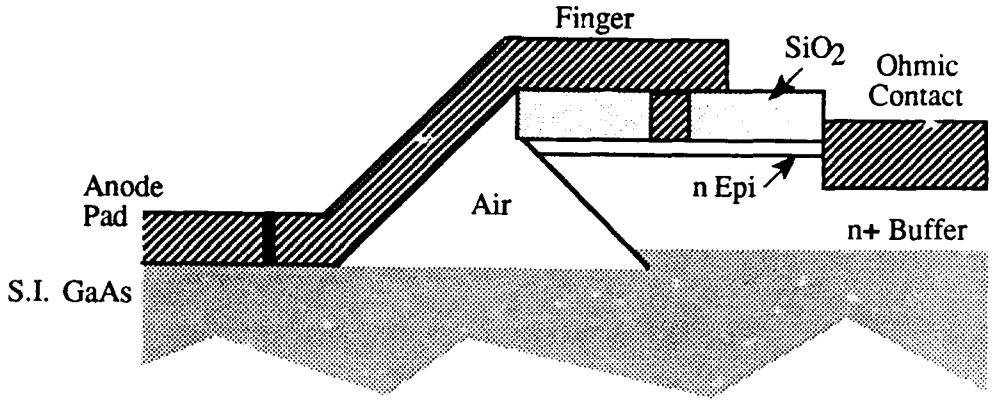


Figure 3.14 The Air Bridge Mesa Structure

This should not have caused excessive leakage, but it was decided that an oxide film was needed between the semi-insulating GaAs and the anode pad as on the first mesa device, still using the air bridge. However, there was no desire to return to the earlier mesa work, and a more promising technology was conceived.

The Surface Channel

In February 1986 Mattauch proposed placing a trench, or "surface channel', across the entire chip to form an air bridge that electrically isolates the anode and cathode. Bishop quickly validated this concept in the laboratory [66]. This is a novel approach since the air bridge is etched after the anode contact finger is formed and thus requires no photoresist fillet. This technology is similar to the proton bombardment technology in that all critical processing steps are carried out on a planar surface, nowever, a simple GaAs etch step replaces the proton bombardment.

The surface channel technology yields an anode contact finger with excellent mechanical properties. Bishop and McKinney demonstrated that the diode required no

special mounting to compensate for thermal stress since electrical characteristics did not degrade when cooled to 77 K [14]. Garfield also calculated that the maximum bending deflection of a 50 μm anode finger at an acceleration of ten times that of gravity was only 0.005 Å, and its resonant frequency was 80 MHz [67].

The early Surface Channel technology used photoresist to cover the ohmic contacts while electroplating the anodes. This technique proved unreliable since most diodes were electrically unstable. It was suspected that the photoresist was dissolving into the plating solution and interfering with the plating process. Therefore, McKinney grew a second oxide over the ohmic contacts at 300°C, below the alloy temperature of the metals.

Garfield and Bishop have also made many other important contributions to the Surface Channel technology [68]. First, anodes sometimes appeared to be damaged in the sputter etch step used to form the anode finger. This was solved by reducing the sample etch time and changing the anode plating parameters to better fill the anodes with gold. Secondly, the oxide would occasionally separate from the GaAs near the ohmic contacts. This problem was solved by plating the ohmic contact metals on the buffer layer instead of the epitaxial layer. Garfield's addition of an oxide etch back step to separate the SiO_2 and ohmic metals also improved the oxide integrity. Finally, the adhesion of gold plated over the ohmic contact metals was improved by removing surface oxides with NaOH instead of HCl acid. Garfield also made a major contribution by demonstrating that the Surface Channel diode performed as well as similar whisker contacted diodes in 100 GHz mixers [69].

Bishop designed a new mask set in 1988. Two major problems remained to be solved at this time. First the tin/nickel electroplating solution used to form the ohmic contacts often attacked the interface between the photoresist and oxide. More importantly however, the electrical quality of the anodes was often poor. Bishop solved the tin/nickel problem in 1989 by switching to a commercially available solution (NiStan). Bishop and Ostdiek demonstrated that ohmic contacts formed with NiStan performed as well as the old Sn/Ni technology.

In 1989 Ostdiek attempted to improve anode quality by investigating different pulse plating parameters (capacitance, resistance, voltage) [1] and observed that good anodes were plated when poor oxide coverage of the ohmic contacts allowed the etch back area near the anode to plate as well. These anodes were thought to be protected from a large plating-current spike by the nearby areas. It was also observed that better anodes were formed using lower capacitances if there was no nearby area to protect the anode. The smaller capacitances were believed to limit the peak value of the current pulse by reducing the amount of charge in the pulse. These observations led to the conclusion that some area near the anode should be exposed during plating; and that a new plating-current profile, containing no sharp current spikes, warranted investigation. This study confirmed observations made by Bishop when fabricating earlier batches of planar diodes. Therefore, Bishop tried plating anodes with the ohmic contacts exposed using a constant DC plating-current. He found that this technique consistently produced high quality anodes.

The anodes plate at a very slow rate when the ohmic pads are exposed, while the large ohmic pads plate very quickly. Therefore, Bishop and Ostdiek developed a new

[1] This effort is discussed in section 6.3.2.

photolithography step to fill only the anode holes by covering the ohmic pads. Bradley included this anode fill pattern in the 1989 planar varactor mask set, which was then under design.

The last major addition to this technology was made in 1990 when Bishop developed a technique for replacing the GaAs substrate with a removable quartz substrate. This is significant for two reasons. First, it lowers the parasitic capacitance of the pads since quartz has a lower dielectric constant. More importantly though, the substrate can be removed after the chip is bonded to a stripline. The capacitance of the pads is then associated with the stripline, as for MMIC devices. Since the remaining shunt capacitances are equivalent to those of whiskered diodes, submillimeter wavelengths may soon be accessible to planar diodes.

3.5 Summary

The planar diode contains an integrated anode contact that eliminates the use of a whisker. The result is a rugged, reliable contact that is ideally suited for space applications However, planar diodes are complicated to fabricate, and contain a large packaging capacitance due to their bonding pads. The search for a simple fabrication sequence that minimizes the pad to pad capacitance has generated a number of planar technologies. The surface channel technology evolved out of these efforts. This technology provides a planar surface for all optical processing steps since the channel is etched last. It has been successfully used to produce millimeter wave diodes of highest quality.

CHAPTER 4

DESIGN

4.1 Introduction

In this chapter the design of the anti-parallel pair of planar diodes is discussed. The goals that defined the design are presented first. Then the geometry of the diode pair and the photolithography mask set are presented. Finally, the fabrication of the mask set and the choice of semiconductor materials are discussed.

4.2 Design Goals

The development of a planar, anti-parallel pair of Schottky barrier diodes on a monolithic chip is a goal of this research. This diode pair is expected to operate at 183 GHz; however, the design must allow scaling for operation at submillimeter wavelengths. Several specific goals have guided the design of this device.

First, the new device incorporates as much of the Surface Channel technology as possible. This technology yields excellent diodes that have performed as well as whisker contacted diodes in fundamentally pumped mixers at 100 GHz. Also, since it is compatible with the use of photolithographic fabrication of submicron anodes, it can be scaled for use at submillimeter frequencies. Furthermore, this technology allows all processing to be done in-house at the SDL.

Since our chip is an integrated diode pair, there are two anodes, and two ohmic contact pads per chip. This means that traditional testing of devices is not possible on the wafer after the anode contact fingers are formed, since the ohmic pads are interconnected. Also, the finger pads are plated on top of the ohmic pads not oxide. This

causes concerns regarding the adhesion of the fingers to the pads since blistering has occurred between metal films during development of the surface channel diode. Also, this means that the edge bead formed on the ohmic contact pad during the overplate step must be eliminated.

The diode pair fabricated for this research is designed for general use in the millimeter wavelength spectrum. It is not designed for one specific receiver. Therefore, the mask set includes a variety of geometries. This allows the junction characteristics and packaging parasitics to be tailored to meet future requirements. Also, alternative geometries were available if the performance of the original design was unacceptable in the 183 GHz mixer. Normally, different geometries generally require different sets of fabrication parameters. However, this mask set is designed so that only one fabrication sequence need be developed. This is accomplished by keeping all plating areas constant throughout each geometry. The ohmic contact pads are the same size for all variations.

The chip was designed to be as small as possible, and is actually significantly smaller than the original Surface Channel diode. This has two distinct benefits. First, it improves the yield since there are more diodes in a batch. Also, it minimizes the amount of the gallium arsenide in the waveguide. Waveguides become smaller as the operating frequency increases. Eventually, the waveguide may become too small to accommodate a chip as large as the 15×5×5 mils required for the Surface Channel diode. Our goal was to put two diodes on a 10×5×1 mil chip.

The final design goal was to fabricate device anodes with similar electric characteristics. Matched anodes allow full realization of the benefits of subharmonic pumping, most importantly, the reduction of LO noise by suppressing the fundamental

response. This was accomplished by supplying each anode with similar electroplating current densities. This required moving the alignment markers and arrays of test anodes from the center of the wafer to the edges. Although mismatches between anodes cannot be totally eliminated because of local variations in the epitaxial GaAs, our anodes proved to be very well matched.

4.3 Chip Design

The final chip design is presented in Figure 4.1. The ohmic contact pads are 6x6 mils on the mask and will be somewhat smaller after dicing. This is the minimum size to ensure a DC resistance below 0.1 Ω using the SDL's SnNi/Ni/Au ohmic contact technology which has a specific contact resistance as low as 10^{-5} Ω cm^2 [70].

The anode contact fingers are two microns wide in the mask, but become 3.5 μm wide on the wafer by overexposing the photoresist. This is consistent with the Surface Channel technology, and eases alignment to the anodes. Four variations of finger length

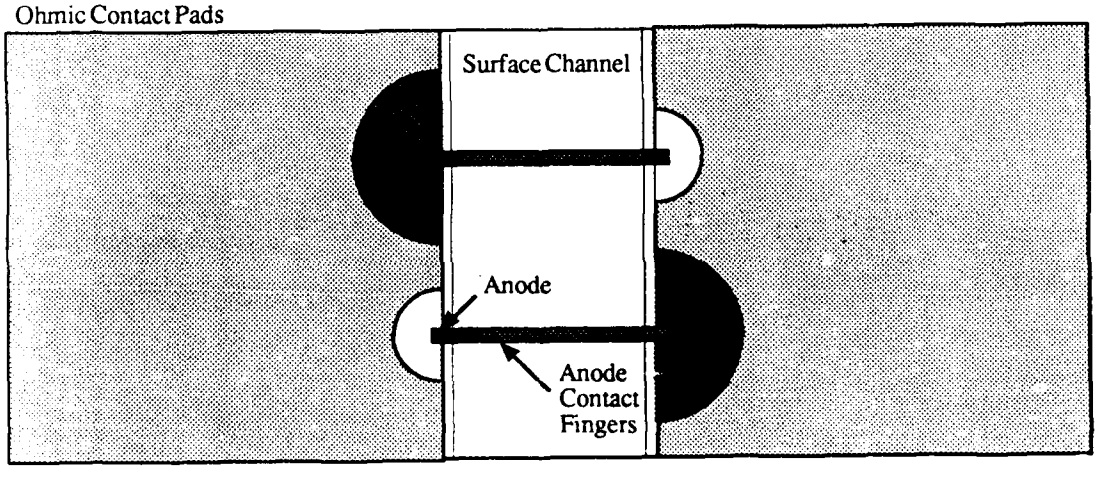


Figure 4.1 Anti-parallel Diode Pair Design

(15, 25, 50, 75 μm) and three spacings (20, 40, 60 μm) are in the mask set, yielding twelve different finger geometries. The lengths were chosen to match those in the mask set of the Surface Channel diode, with the exception of the 75 μm finger. This was added to offset the effect of the mutual inductance of the two fingers. The equivalent inductance of two identical parallel inductances can be half the self inductance of one finger. Therefore the 75 μm fingers were added for a high inductance device, should one be needed. The widest finger spacing of 60 μm was chosen to keep the fingers one mil from the expected dicing curf. This allows room for misalignment during dicing, and reduces the possibility of damaging a finger when handling the chip with tweezers. The 15 μm finger length was added as a possible high frequency device. This is close to the smallest finger allowed with the surface channel etchant used since the channel edge must be five microns from the ohmic contacts. Therefore, the finger must be significantly longer than ten microns.

The mask set contains anode diameters of 1, 1.5, and 2 μm. Controlling the anode hole size through photolithographic exposure time and etching process allows anode diameters from 1 to 2.5 microns.

4.4 Mask Fabrication

The seven level mask set was designed at the SDL using AutoCAD and manufactured by the Electron Beam Technology/ALO Division of Perkin-Elmer (now a part of DuPont Photomasks Inc.). Details of the mask set and its fabrication are discussed in Appendix A. The mask was made using a thin "see through" layer of chromium. This layer is opaque at the UV wavelengths used to expose the resist, and is transparent to white light. This choice made alignment of the masks to existing features

on the wafer much easier.

4.5 Diode Material

The cutoff frequency of a Schottky barrier diode is calculated from the series resistance and junction capacitance of the diode. It is therefore related to that material's carrier mobility μ and its permittivity ϵ as:

$$f_{co} \propto \frac{\mu}{\sqrt{\epsilon}} \tag{4.1}$$

This means that fast, high frequency diodes must be made of a material of high mobility and low dielectric constant, such as gallium arsenide with its high intrinsic mobility and low permittivity ($\epsilon_r \approx 13$). Other materials, such as InGaAs have even higher mobilities, but they have smaller band gaps and therefore can not support large reverse voltages. Furthermore, their technology base has yet to reach the maturity of GaAs.

The crystal structure used in this design is shown in Figure 4.2. It consists of a semi-insulating substrate, a highly doped buffer layer, and a moderately doped epitaxial layer. The substrate must have a high resistivity to isolate the two ohmic contact pads electrically. This substrate was grown at Hitachi using the Liquid Encapsulated Czochralski technique and was 2° off <100> towards <110>. Its mobility is between 6100 and 7400 $cm^2/V \cdot s$ and has a resistivity between 1.5 and 4.4 x 10^7 Ω cm.

The choice of the doping density and thickness of the epitaxial layers is critical to the diode performance. Since the Schottky contact is formed on the n-type active layer, this layer is designed to optimize the characteristics of the junction. A low active layer doping density yields improved sharpness of the IV characteristic due to reduced tunneling current [50]. However, this also increases the $R_S C_{jo}$ product, degrading high

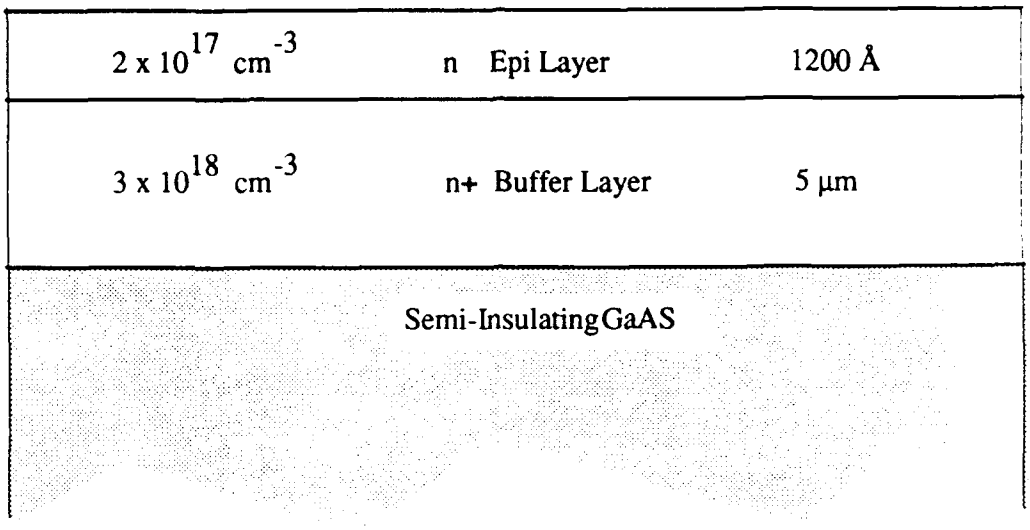


Figure 4.2 Standard Diode Crystal Structure

frequency performance. The chosen doping density of $2\times10^{17}cm^{-3}$ represents an appropriate trade-off between these effects for a room temperature millimeter wavelength receiver. The thickness of the active layer is chosen to be slightly greater than a zero-bias depletion depth. This is a standard design used in the SDL.

The buffer layer serves as the current path between the active layer and the ohmic contact. Thus, it does not directly affect the characteristics of the metal-semiconductor junction, but is a significant source of series resistance. For this reason it is doped as highly as possible. The buffer layer thickness is chosen to minimize resistance while not being so thick as to make the surface channel etch difficult.

4.6 Summary

The Surface Channel technology was chosen as the basis of the anti-parallel diode pair design. The diode pair was designed specifically for use at millimeter wavelengths, but can be scaled to submillimter wavelengths. The photolithography mask set allows the use of one set of fabrication parameters to be used to create 12 different ohmic contact pad and anode contact finger geometries. Also, anode diameters from 1 to 2.5 microns are possible. The most important design criteria was that the anodes be as well matched as possible. This was achieved by ensuring that the anodes were embedded in virtually identical environments during all plating and etching steps.

CHAPTER 5

FABRICATION

5.1 Introduction

This chapter presents the fabrication sequence of the anti-parallel chip, which contains alloyed ohmic contacts, GaAs substrate and anodes defined by wet etching. This process requires a man-month of labor to produce one batch of diodes. Some of the techniques used in fabrication are first discussed. Then the sequence is outlined. The details of this technology are presented in Appendix B. Problems encountered during process development and their solutions are discussed in the final section.

5.2 Techniques

The fabrication of semiconductor devices involves three general processes. First, photolithography is used to protect specific regions of the wafer from subsequent substractive and additive processes. Subtractive processes are used to remove unwanted material by etching, and additive processes are used to deposit material, building up device features.

5.2.1 Photolithography

Photolithography is a pattern transfer technique that uses light, a thin light sensitive film called photoresist, and an opaque mask containing a transparent image. The patterned photoresist film itself serves as a mask to protect portions of the underlying substrate from subsequent additive or subtractive processing. The variety of photolithographic technologies can be categorized as either positive or negative, as illustrated in Figure 5.1. A positive process removes the photoresist from the exposed

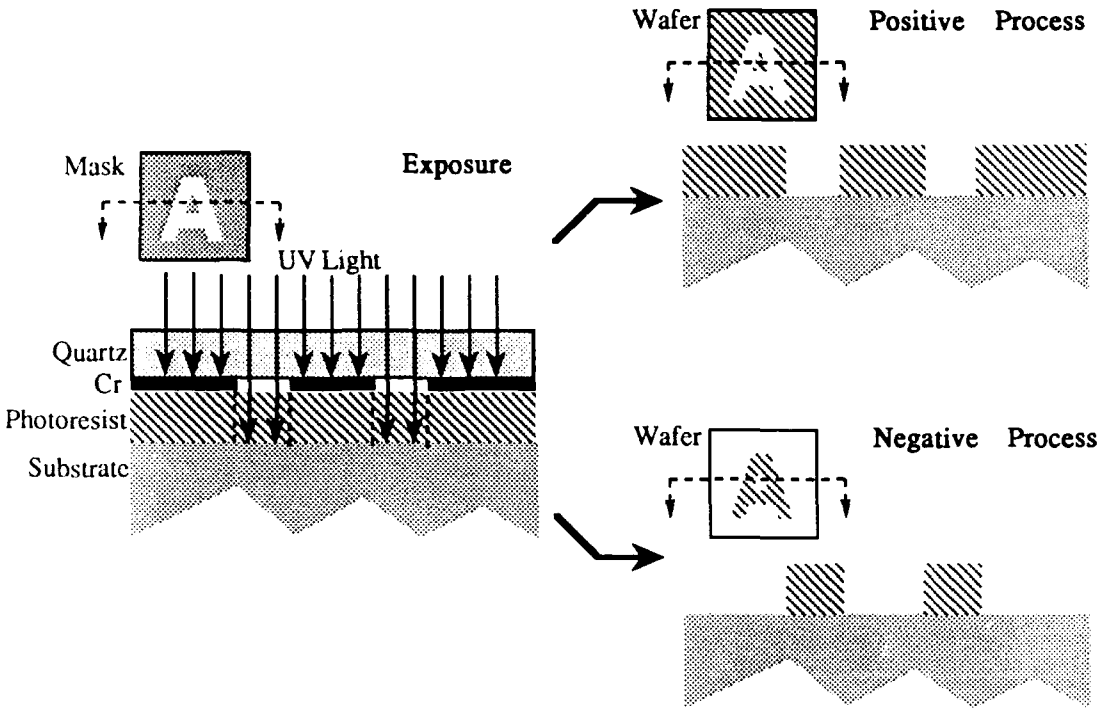


Figure 5.1 Positive and Negative Photolithographic Processes

areas under the transparent regions of the mask. A negative process removes the unexposed photoresist under the opaque mask regions.

A typical photolithographic process uses a positive photoresist that is composed of a diazonaphtoquinone ester (DQ) dispersed in a phenolic-formaldehyde or novalak resin, and a casting solvent [71]. The novalak resin is soluble in aqueous alkaline solutions. The DQ inhibits the dissolution of the novalak until it is destroyed. It is sometimes referred to more generally as the Photoactive Compound or PAC. The DQ is destroyed photochemically when it absorbs radiation at the wavelength of 365, 405, or 435 nm. Upon absorption, the DQ undergoes a multistep change to form an indene acid which allows the novalak to be removed by the developer.

Some positive resists may be used in negative processes by a technique known as image reversal. A post exposure bake is first used to render the exposed regions permanently insoluble to the developer. Then, a flood exposure of the entire resist makes the previously unexposed regions soluble.

Some photoresists are also designed specifically for negative processes. They usually require one or more photochemical events to form crosslinks between polymers. These crosslinked regions have an increased molecular weight, and, therefore, a lower solubility.

Photolithography is typically composed of seven steps. They are:

- Surface Preparation
- Resist Application
- Soft Bake
- Exposure
- Post Exposure Bake
- Development
- Hard Bake

Surface Preparation

Surface preparation includes cleaning, baking and priming the wafer. This is done to ensure good adhesion between the photoresist and the substrate. The wafer is first cleaned to remove surface contamination that can interfere with pattern transfer, or damage the mask. In this research, this was achieved by spraying ethanol and scrubbing the wafer lightly with a cotton swab while it spun on a vacuum chuck. The wafer was then immersed in boiling ethanol and blown dry with a filtered N_2 stream immediately upon removal. The ethanol dip is repeated, with the position of the tweezers changed between dips. Next, the wafer is dipped into the boiling solvent and the wet surface is gently scrubbed with a cotton swab upon removal. This step is also repeated. The

dip/blow-dry step is then repeated two more times. This whole process is repeated for both boiling trichloroethane and boiling methanol. Finally, the wafer is immersed in a fresh beaker of boiling methanol for 30 seconds. These solvents are rated for Class-10 use, and are flammable.

The wafer is then baked to remove moisture from its surface. This can be done in an oven (180°C for 30 minutes) or on a hotplate (120°C for 5 minutes). Both methods were used in this research and found to be adequate for all subsequent processing.

The surface of the wafer is often sealed with an adhesion promoter. Hexamethyldisilzane (HMDS) is a complex molecule that bonds to both the SiO_2 substrate and the photoresist. It also improves adhesion by bonding with any water molecules that might be present on the surface. The HMDS is applied in vapor phase for ten minutes. HMDS is not too effective, however, on metal or gallium arsenide surfaces [71].

Resist Application

The photoresist is a liquid that is applied to the wafer surface. The wafer can be spun (0-10000 rpm) to remove excess resist leaving behind a thin uniform film. The spinning also evaporates the casting solvent, leaving the resin and PAC as solids. The final thickness of the film depends upon both the spin speed and the resist viscosity. The wafer must be centered on the spinner chuck for the best uniformity. Also, the resist should be pooled over the wafer edges to break the surface tension there. High spin speeds (>6000 rpm) result in thin films (0.2-1.5 μm) and minimal edge beads. However, thin films are likely to contain more pinhole defects, do not cover non-planar features as well, and do not survive as long during dry etch processing.

Resist Softbake

The softbake removes the casting solvent that did not evaporate during spinning. It also provides for the proper photospeed needed to record the mask's pattern. If overbaked, there is not enough water for the PAC to react with, and thus photospeed is reduced, resulting in poor contrast. Also, the film becomes brittle. If the resist is underbaked, too much solvent remains which also reduces photospeed, and reduces adhesion. Temperature is more important than time as long as the resist achieves a steady-state temperature. Softbaking can be achieved in convection ovens; however, hotplates are generally preferred because the resist is heated from the substrate up. This prevents a skin from forming that interferes with the diffusion of the solvents. It is also quick, often achieving excellent results in less than one minute.

Exposure

A variety of optical exposure systems exist. A Karl Suss MJB3 mask aligner capable of proximity, contact, and vacuum (hard) contact exposure modes is used at the SDL. Vacuum contact provides the high resolution pattern transfer required of sub-micron photolithography. Unfortunately, it also provides for an increased number of defects in the resist and more mask damage. This is tolerated since one wafer die contains 300 device patterns, and the SDL is involved in research, not mass production.

The intensity and exposure time together determine the energy delivered to the photoresist. All processes at the SDL use an intensity of 10 mW/cm^2 and the time is adjusted for best results.

Parameters limiting the resolution of contact printing are the wavelength of the radiation and the proximity of the mask to the resist. Short wavelength ultraviolet

radiation (405 nm) is used to reduce diffraction effects. The combination of bevelled wafer edges and vacuum contact printing provide for intimate mask/resist contact by reducing the photoresist edge bead. This is accomplished by drawing a vacuum between the mask and the chuck holding the wafer. Then, atmospheric pressure on the back side of the chuck pushes the wafer into the mask.

Post Exposure Bake

The post exposure bake is used for three purposes. It is used most often to improve resist adhesion to the substrate, and to eliminate standing wave patterns in the vertical resist profile which result when reflected light interferes with incident light. The adhesion of the resist to the substrate is improved after the post exposure bake, but this improvement gradually disappears in a few hours. Therefore, the wafer should be processed soon after photolithography. Coherent, monochromatic optical systems will provide resist profiles that contain ripples. These are caused by the interference of the reflected and incident light. The post exposure bake eliminates this problem by causing unexposed PAC to diffuse from high to low concentrated regions. This bake must be related to the soft bake so the final photospeed is not significantly degraded. Lastly, as discussed above, this bake can be used to reverse the mask image.

Development

The soluble regions of the resist film are now removed by an aqueous alkaline developer. The time required to develop the pattern depends upon the parameters used to form the film and its image. As exposure energy increases the concentration of PAC's decrease. This increases solubility. Also, development times change when bake temperatures are increased. The concentration of the developer is also important. As the

concentration is increased the development time decreases and contrast increases. However, linewidth control decreases as the short development times are hard to control [71]. The temperature of the developer should be controlled (21-23°C) for repeatable results, and consistent agitation is required for uniform development.

Hard Bake

The hard bake improves adhesion and the chemical resistance of the resist. The high temperature drives out the no longer needed solvents and water, and causes polymerzation. However, the resist will flow slightly during this bake making sharp edges rounded. To prevent this the resist can be cured before the bake by exposure to ultraviolet light. This causes a skin to form that helps preserve the pattern during the bake, and maintain vertical resist edge profiles.

5.2.2 Subtractive Processes

Several etching techniques are used to remove material from the wafer. The techniques used in the Surface Channel technology can be categorized as either wet or dry. Wet etching is used to remove films of silicon dioxide, chromium, and gallium arsenide; while dry etching is used for general wafer cleaning, removal of thin gold films and silicon dioxide. Important concerns to all etching processes are the thickness of the film to be removed, time required to reach the endpoint, mask adhesion/erosion, and undercutting of the mask.

Wet Etching

Silicon dioxide is etched in buffered hydrofluoric acid. A standardized solution of buffered hydrofluoric acid (BOE 10:1 or BOE 10:1 Superwet [72]) is maintained at 22°C to etch undoped SiO_2 (grown at 350°C) at a rate of 35 Å/sec. The etch is isotropic, with

a lateral etch rate equal to the vertical etch rate. Agitation is required for uniform results.

Etching small features requires the use of BOE 10:1 Superwet. This solution contains a surfactant that reduces surface tension, allowing small features to be wetted. It is important to prewet the wafer in deionized water with mild ultrasonic agitation for several minutes before etching.

The etch mechanism involves the attack of bifluoride ions [71], and the replacement of oxygen with fluorine. The etch is characterized by:

$$6HF + SiO_2 \rightarrow H_2SiF_6 + 2H_2O$$

Buffered hydrofluoric acid is used because its hydrogen ion concentration is controlled, and an unbuffered solution readily penetrates the photoresist forming pinhole defects.

An IBM French patented solution of AZ Developer, potassium permaganate, and deionized water is used to remove chromium films. If fresh, this solution will not attack SiO_2. It does attack GaAs, photoresist, and alloyed ohmic contact metals if they are not overplated with gold. It has a low etch rate of approximately ≈100 Å/minute. The chromium film is overetched purposely to ensure its removal is complete. A rule of thumb is to use an etch time that is identical to the length of time the film was deposited at ≈60 Å/minute.

At the SDL a variety of etchants are used to remove gallium arsenide. All are mixtures of an agent that oxidizes the GaAs, and an acid or base to remove the oxide. The typical base etchant is a "Fizz" etchant composed of sodium hydroxide, hydrogen peroxide and water. The concentrations used vary depending upon the processing step. They are listed in Appendix 3 and discussed by Aydinli [73]. A citric acid, hydrogen peroxide solution (citric acid 50% by weight: H_2O_2 30% (10:1)) is also used to remove

large amounts of GaAs while forming ohmic contacts. This solution etches at a rate of approximately 33 Å/sec at 22°C, and is isotropic.

Small amounts of conductive GaAs are removed by anodic etching in an alkaline solution of ethylene glycol [74]. This technique allows the precise removal of GaAs in layers as thin as 50 Å. The GaAs serves as the anode in this electrochemical technique, and is oxidized by the holes supplied by the current. The current is controlled by a voltage limited controlled current source that stops the current when the voltage drop across the oxide reaches a value characteristic of the desired thickness. The oxide is later removed by an acid.

Dry Etching

Dry etching provides greater control of the process through a variety of process parameters. It is very important in GaAs device fabrication because the vertical etch rate is much greater than the lateral etch rate. It is, therefore, well suited for defining small features. However, it is a complex process with an etch rate dependent upon almost every process parameter.

Sputter etching and reactive ion etching (RIE) systems were used in this research. Both techniques use a plasma created by coupling RF power through an impedance matching circuit to a working gas. This generates a strong electric field that accelerates free electrons until they collide with, and ionize the neutral atoms or molecules of the gas to form a plasma.

The sputter etching system at SDL creates an argon plasma. The argon ions are accelerated by the electric field towards the sample where they transfer their momentum to the sample. This causes material to be physically dislodged, or "sputtered", from the

surface.

The RIE system at SDL uses CF_4 as the working gas. The primary plasma reaction used for oxide etching is:

$$CF_4 + e \rightarrow CF_3^+ + F^* + 2e$$

Similar to sputter etching, the CF_3^+ ion is accelerated towards the sample. Unlike argon in the sputtering system, however, this ion is chemically active, and enhances both the vertical and horizontal etch rates.

5.2.3 Additive Processes

Two processes are used to deposit metals onto the sample: sputter deposition and electroplating. The sputter etch system can be used to etch a target placed above the sample. Then the dislodged material drops onto the sample, to which it adheres. This technique is used to place chromium and gold films onto SiO_2. Chromium is deposited first because sputtered gold will not adhere to SiO_2. The sputter system at the SDL is a single target system. Therefore, the vacuum must be broken, the target changed, and vacuum re-established before depositing gold. Venting the chamber exposes the chromium to the atmosphere when the target is changed. The samples must therefore be allowed to outgas in a vacuum for several hours before the gold film is deposited. This insures that the gold film will adhere to the chromium.

Electroplating is used throughout fabrication because it is inexpensive and sometimes superior to vacuum deposition. Anodes are electroplated at the SDL because the GaAs surface can be properly prepared chemically for low noise diodes [73]. The factors important to electroplating are sample and anode geometry, conductivity of the underlying substrate, surface preparation, the ratio of anode to cathode areas, and the

circuit used to supply the ions for plating. This research uses capacitive pulse, square wave, and DC plating. Plating areas and current densities are controlled by mounting the samples on an electroplating fixture. This fixture consists of an insulated probe that is lowered to contact the wafer, which is waxed onto a glass slide. In spite of its age, the electroplating technique is still very much an art.

Thin oxide films are used in diode designs to passivate the crystal, protect it from damage during processing, and serve as an insulator between the conductive GaAs and the overlying metal. GaAs is a troublesome material in this regard because it does not possess a suitable native oxide the way silicon does. Therefore, the oxide must be deposited by an additive process.

This is done with an atmospheric pressure chemical vapor deposition system developed at SDL [48]. The device wafer and a scrap wafer are placed on a rotating substrate at 350°C, and ultra pure silane and oxygen gases are used to form the oxide as:

$$SiH_4 + O_2 \xrightarrow{350°C} SiO_2 + 2H_2$$

The thickness of the film is adequately controlled by watching the film change color during deposition. The scrap wafer is used later to determine the oxide thickness. Typically, it is about 100 Å thicker in the middle than at the edge of the wafer.

5.3 Standard Sequence

Before fabrication begins, the 3-inch GaAs wafer supplied by the crystal grower must be diced into 0.260×0.220 inch wafers. It is important, however, to confirm the orientation of the devices with respect to the crystal before dicing since a critical step in device fabrication, the surface channel etch, relies on an orientation dependent etch. As

supplied, the 3-inch wafer usually has a major flat indicating the <011> direction for a crystal grown 2 degrees off of <100> towards <110>. This flat must run parallel to the surface channel and ohmic contact stripes, and perpendicular to the anode contact fingers.

The crystal direction is confirmed by slicing a 0.050 inch strip of the 3-inch wafer parallel to the major flat. Then a series of circular masks (≈0.010 inch diameter) formed with a mixture of trichloroethylene and black wax (Apiezon-W wax) are placed on the epitaxial surface. Once dry, the slice is dipped into a buffered hydrofluoric (BHF) acid solution (BOE 10:1) for ten seconds to remove any surface oxides. The GaAs is then etched for three minutes in a 1:1:10 solution of $NaOH:H_2O_2$:deionized water. This causes a mesa to be formed in the epitaxial layer whose edge profiles will vary with crystal direction. The sample is examined with a microscope after the black wax has been removed with trichloroethane. Two opposite edges of the mesa will appear dark and thick as shown in Figure 5.2. These thick edges indicate where the mesa gently slopes down. The thin edges offset 90 degrees from the thick edges are where the black wax mask was undercut. These edges are parallel to the $<01\bar{1}>$ direction and should run

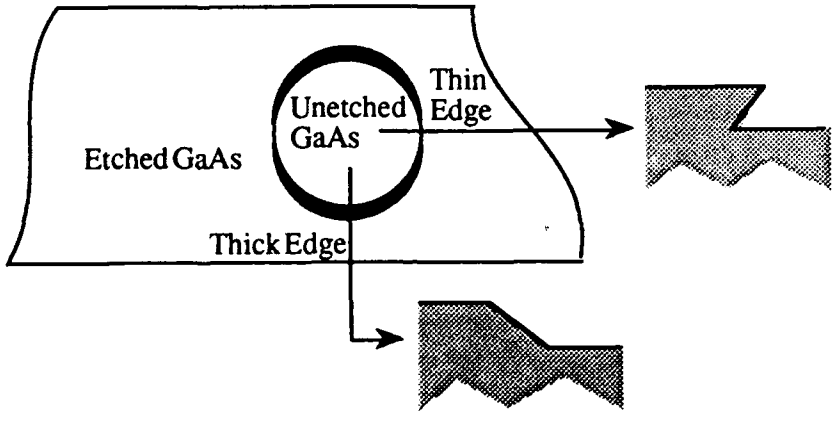


Figure 5.2 Mesa Etch Confirmation of Crystal Direction

parallel to the anode contact fingers so that they are undercut by the surface channel etchant. It is also a good idea to inspect the wafer by scanning electron microscopy. Then, the 3-inch wafer should be diced into approximately 42 0.260×0.220 inch wafers as shown in Figure 5.3. Notice that the 0.260 inch edge is parallel to the thick edge of the etched mesa.

After the wafer is removed from the main slice, its edges are bevelled. Bishop added this step for two important reasons. First, it reduces the amount of damage caused to the wafer by tweezers during future handling. More importantly though, it reduces the effect of the edge bead formed when photoresist is applied. The edge bead forms on the bevelled surface below the plane of the mask. This allows the mask to contact the resist for a more faithful pattern reproduction. Reduction of the edge bead also keeps the GaAs wafer from cracking when it is pushed into the mask during vacuum contact.

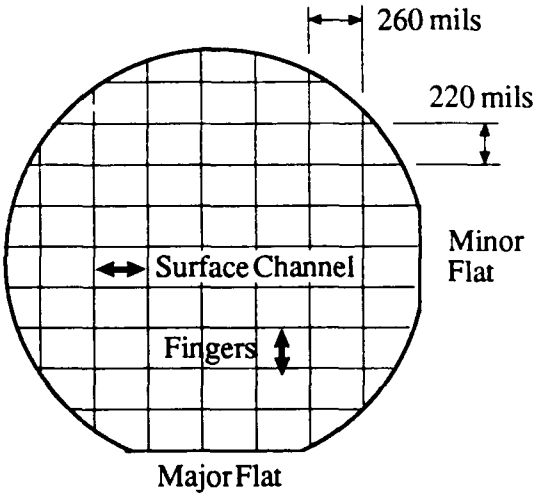


Figure 5.3 Diced 3-inch Wafer

Elimination of edge bead interference also allows lower spin speeds to be used during application. Therefore, thicker resist films can be deposited with fewer pinhole defects [75].

The doping profile of the crystal is characterized next, and the active epitaxial layer is thinned to a desired thickness. A mercury probe, CV profile station is used to determine the doping profile of the epi and buffer layer. For consistency's sake, the epi/buffer interface was assumed to exist when the doping rose from 2×10^{17} cm^{-3} to 5×10^{17} cm^{-3}.

The epi layer is then anodically thinned to a desired thickness for good electrical characteristics. The doping profile is again characterized to confirm the thinning process. Then, an additional 50 Å is removed anodically so no anodes will be formed on a surface previously exposed to mercury.

Once bevelled and thinned, the wafer is ready for the variety of additive, subtractive, and photolithographic processes. First, 5000 Å of SiO_2 is deposited on the GaAs as shown in Figure 5.4.

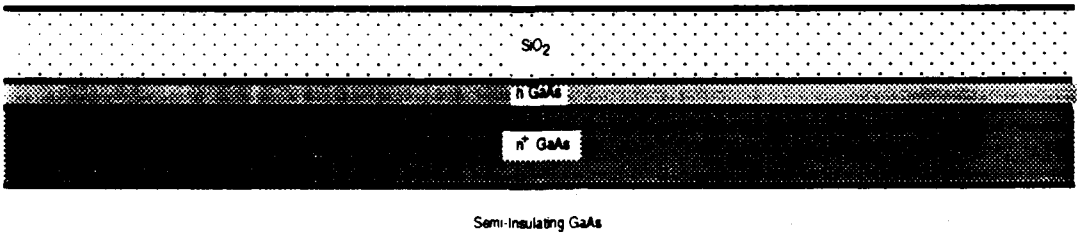


Figure 5.4 Oxide Deposition

The wafer is then ready for the first of six photolithography steps. It is crucial that all six patterns are aligned with less that one micron of error. To accomplish this the first photolithography step transfers a series of alignment, or registration markers into the oxide. The alignment markers used are discussed in section 4.3. After photolithography, the pattern is transferred into the oxide by etching in BOE 10:1 Superwet until 900-1000 Å of oxide is left at the bottom of the alignment markers.

The ohmic contact step is next. A minimum of five hours is required for photolithography, etching, and electroplating of the ohmic contact metals, making this the longest step in the process. Photolithography is first used to transfer the ohmic contact pad pattern into both the oxide and the GaAs as shown in Figure 5.5. BOE 10:1

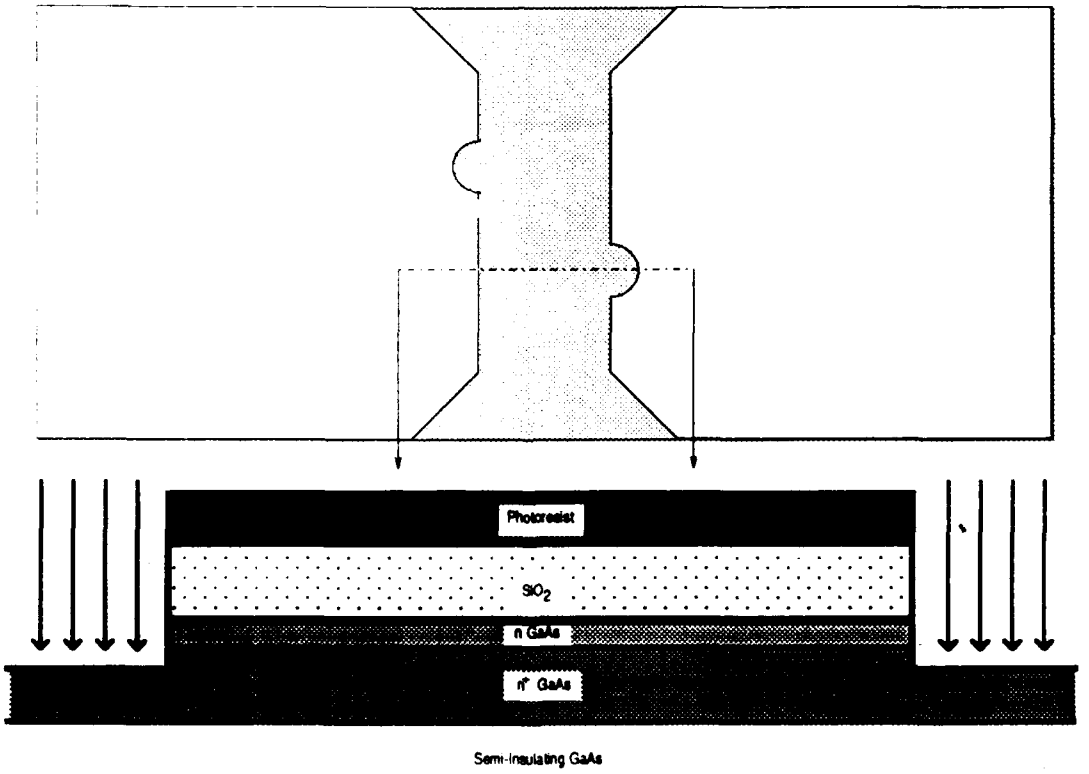


Figure 5.5 Ohmic Contact Photolithography

[72] is used to remove the oxide from the pad areas. BOE Superwet should not be used since it contains surfactants that are suspected of causing poor adhesion of metals to the ohmic contact. A citric acid solution is then used to etch half a micron into the highly doped buffer layer. It is important to rinse the wafer thoroughly under a running deionized water stream after the citric etch. This helps prevent bubbling of the ohmic metals during the alloy step by removing organics left by the etchant.

The wafer is then mounted on a glass slide which is attached to the electroplating fixture. The ohmic metals are electroplated in four steps. First, a commercial tin/nickel mixture (NiStan) is used to pulse plate Sn/Ni onto the GaAs. This same solution is used to DC plate Sn/Ni in the second step. Then Ni is DC plated and followed by a DC plating of Au as shown in Figure 5.6. Next the SiO_2 is etched back away from the metals, undercutting the photoresist as shown in Figure 5.7. This prevents Au from diffusing into the oxide, and reduces thermal stresses during alloy. At this point the resist adhesion to the oxide may begin to fail. Therefore, this etch should be done in three one minute intervals, and inspected between each interval.

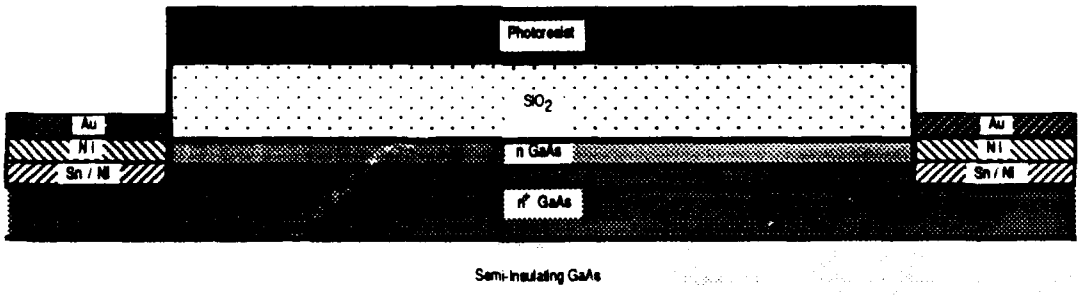


Figure 5.6 Ohmic Metals Electroplated

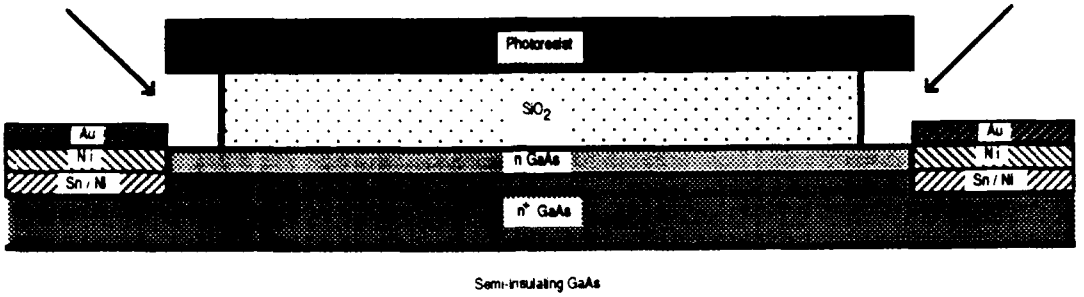


Figure 5.7 Ohmic Etch Back

Next, the photoresist is removed, and the wafer cleaned. Then the ohmic metals are alloyed with the GaAs in a forming gas environment. (See Figure 5.8) The wafer is heated in this step by a tantalum ribbon heater to a temperature of about 350°C [68] for 50 seconds.

Finally, the ohmic contact pads are overplated with a thick layer of Au as depicted in Figure 5.9. To do this, the wafer is first cleaned and surface oxides of the metals are removed by pickling in a NaOH solution for 5 minutes. The Au is capacitively pulse plated to eliminate the Au edge bead that is formed by DC plating. This edge bead

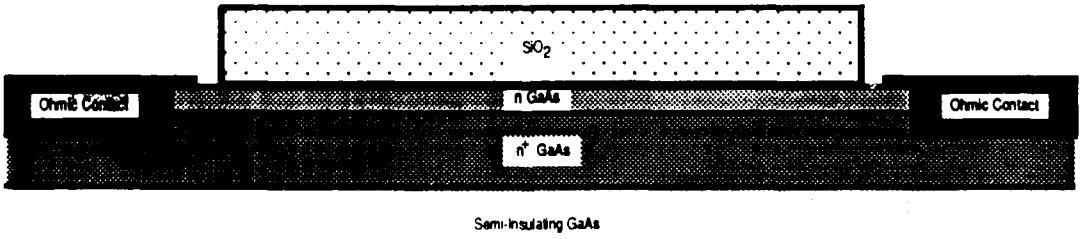


Figure 5.8 Ohmic Metals Alloyed

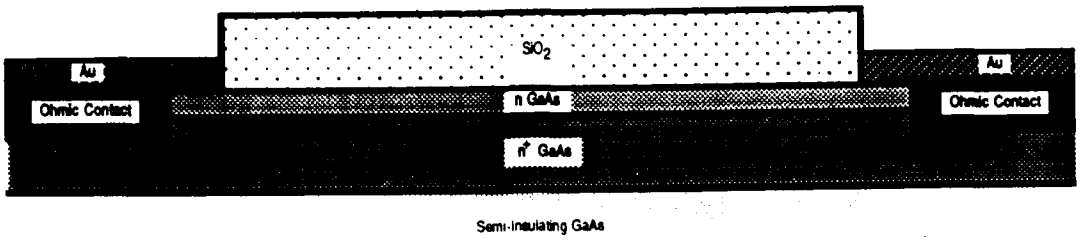


Figure 5.9 Ohmic Contact Overplate

interferes with transferring the anode pattern and metallization of the anode contact finger.

After photolithography, BOE Superwet [72] is used to etch the anode holes as shown in Figure 5.10. However, 800 Å of oxide is left at the bottom to protect the GaAs surface until the anode plating step.

To plate the anodes, the holes are prewet in deionized water. Then the remaining oxide in the anode holes is removed with BOE Superwet etchant [72] and rinsed in deionized water. The GaAs crystal is then etched in a $NaOH:H_2O_2$ "Fizz" etch. Then platinum is electroplated with a direct current, followed by gold as shown in Figure 5.11. The wafer is held by a pair of tweezers and dipped to a specified depth into the plating solution during plating in order to maintain a consistent deposition rate.

Notice that the ohmic contact pads were left unprotected during the anode plating step. This has two effects. First, the ohmic contacts are plated with a thin film of platinum and gold. This is not believed to have any measurable affect. Second, the large ohmic contact pad tends to consume most of the plating ions, making it difficult to plate within the anode holes. Therefore, after thin layers of platinum and gold are plated to

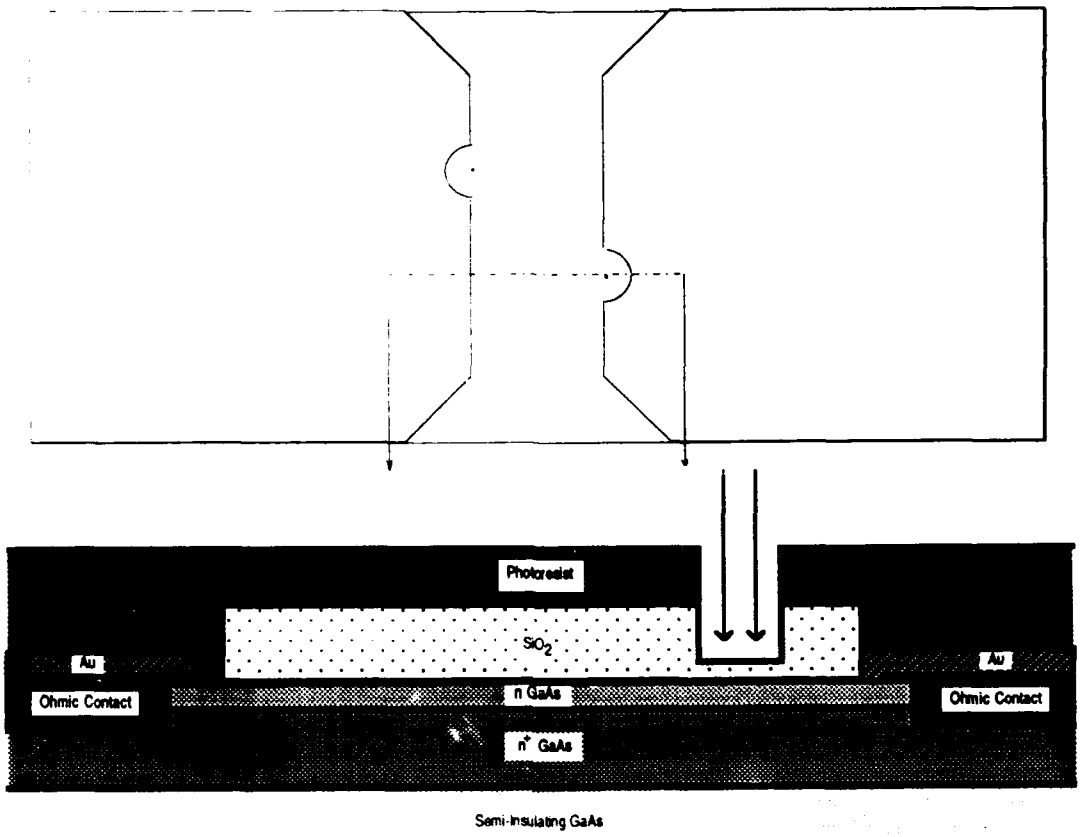


Figure 5.10 Anode Hole Definition

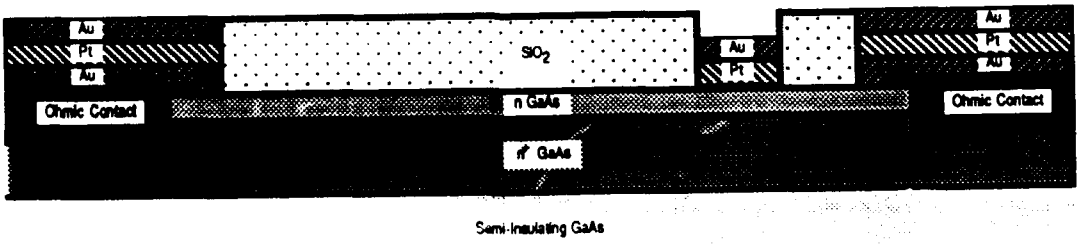


Figure 5.11 Anode Plating

form the critical metal-semiconductor junction, an additional lithography step is used to cover the ohmic contacts with photoresist as shown in Figure 5.12. This allows the anode

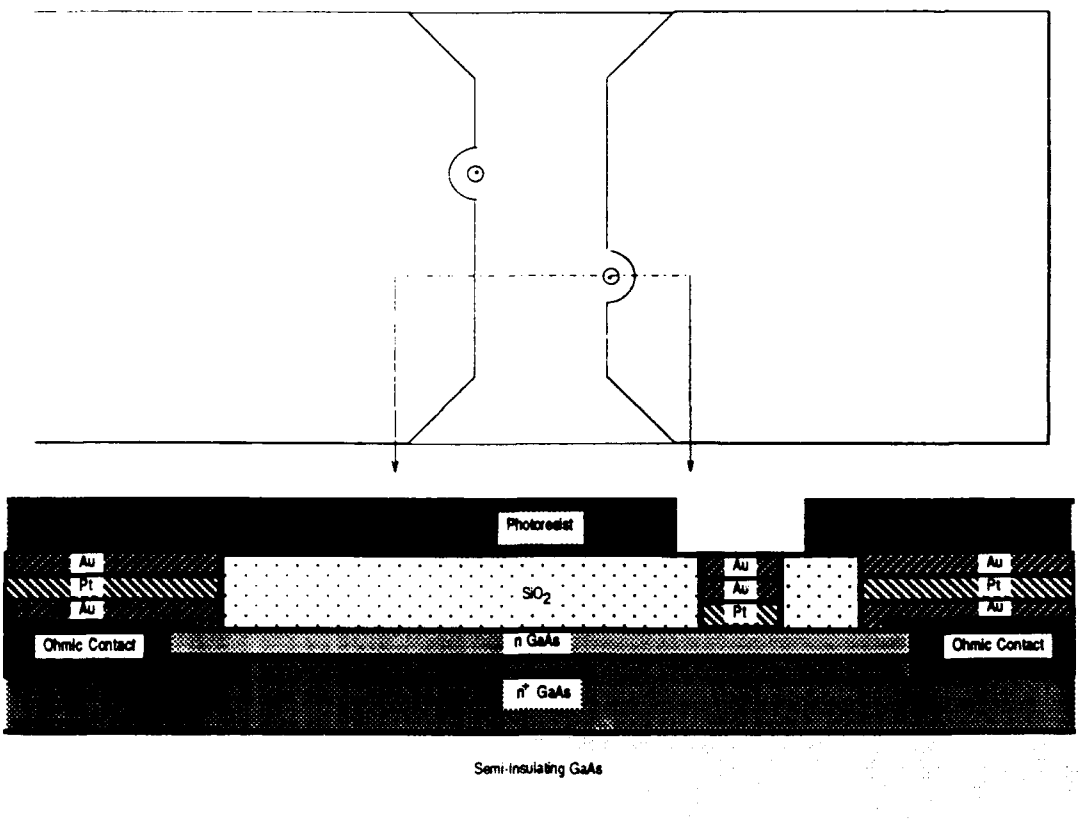


Figure 5.12 Anode Fill Step

holes to fill with gold at an acceptable rate in the subsequent plating step.

Now the wafer is ready for the anode contact fingers. These fingers are to be electroplated over an insulating SiO_2 film. Therefore, a conductive film of chromium and gold are first deposited over the entire wafer in the sputter etch system (Figure 5.13). Then, after photolithography, the fingers are electroplated as shown in Figure 5.14. First with a thin layer of Autronex-N [76] gold plating solution, then with a thick layer of Sel-Rex BDT-200 [76] gold solution. The BDT-200 solution provides uniform plating throughout the narrow finger region.

Both dry and wet etching are used to remove the thin chromium/gold film covering the wafer. First the gold film is removed by sputter etching (Figure 5.15). No

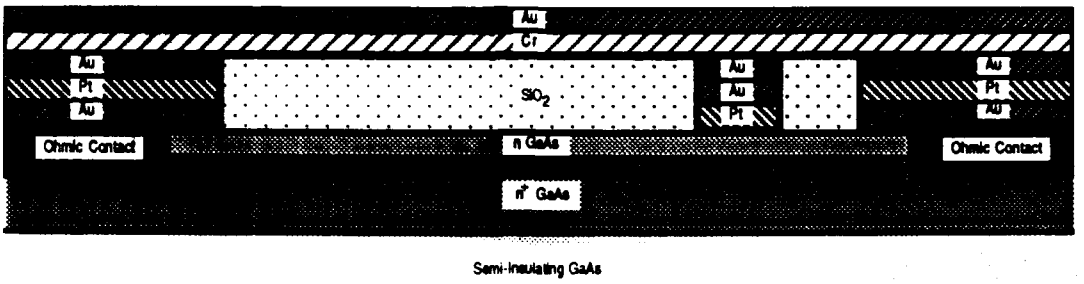


Figure 5.13 Sputter Deposition of Cr and Au Films

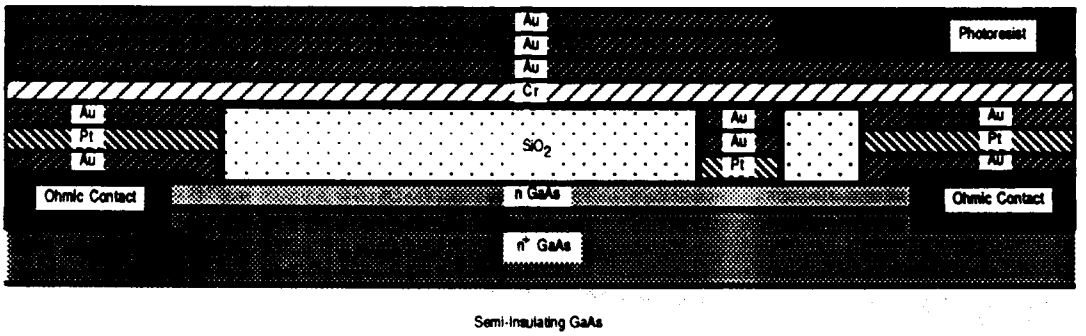


Figure 5.14 Anode Contact Finger Plating

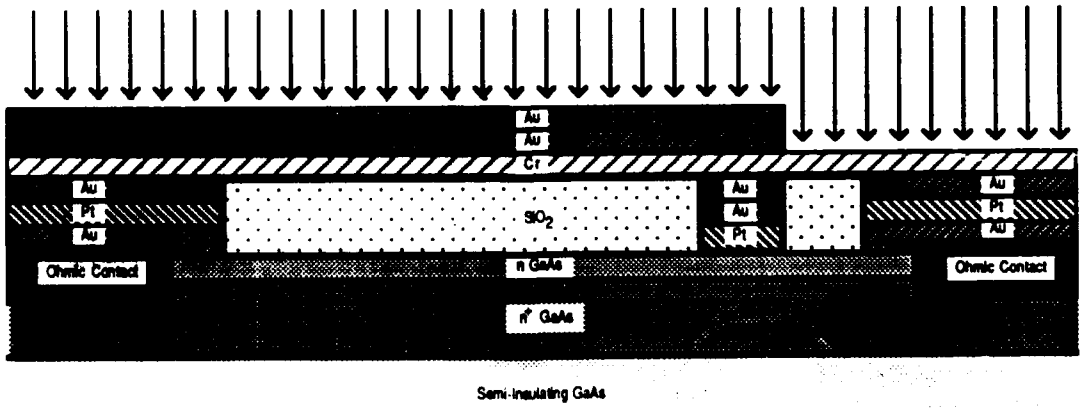


Figure 5.15 Sputter Etch Removal of Gold

photolithography is required since the fingers are thick enough to form their own mask. Then the chromium is removed by a wet etchant as discussed previously (Figure 5.16). Sputter etching is not used since it damages the anodes, and does not completely remove the chromium.

The final photolithography step defines the surface channel. Buffered hydrofluoric acid is first used to remove the oxide. Then, as shown in Figure 5.17, the conducting GaAs between the pads is removed a $NaOH:H_2O_2$ etchant. This etchant provides different etch profiles for different crystal directions, allowing the finger to be undercut completely.

The wafer is then lapped to the desired thickness and diced.

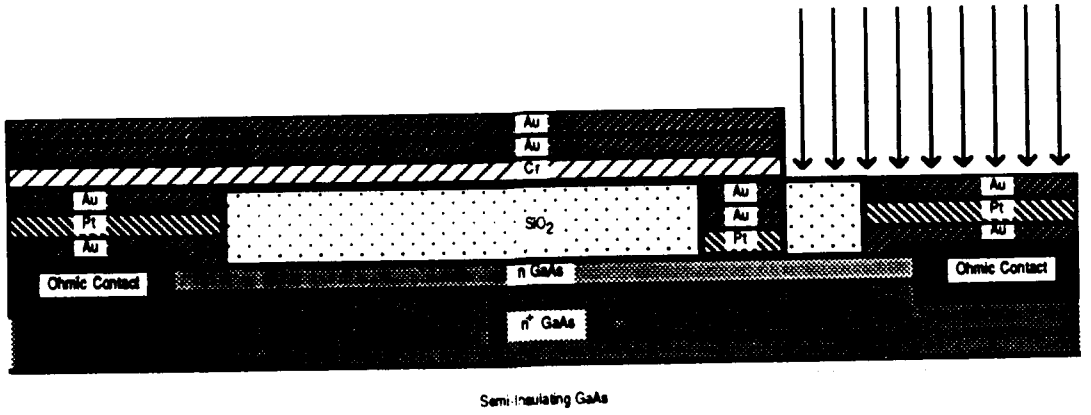


Figure 5.16 Wet Etch Removal of Chromium

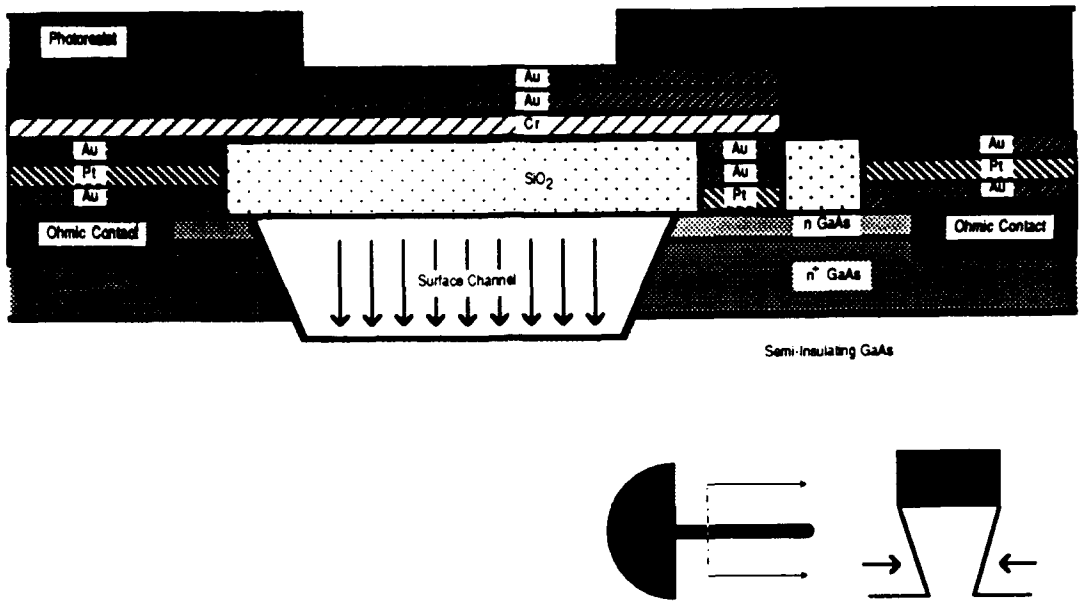


Figure 5.17 Surface Channel Etch

5.4 Summary

This chapter presented the technology used to fabricate the anti-parallel diode pair. A scanning electron micrograph of the finished device is shown in Figure 5.18. The general processes used to fabricate semiconductor devices was first discussed. This included photolithography, subtractive, and additive processes. Then an overview of the actual sequence used to fabricate the diode was given. This sequence is detailed in checklist format in Appendix B.

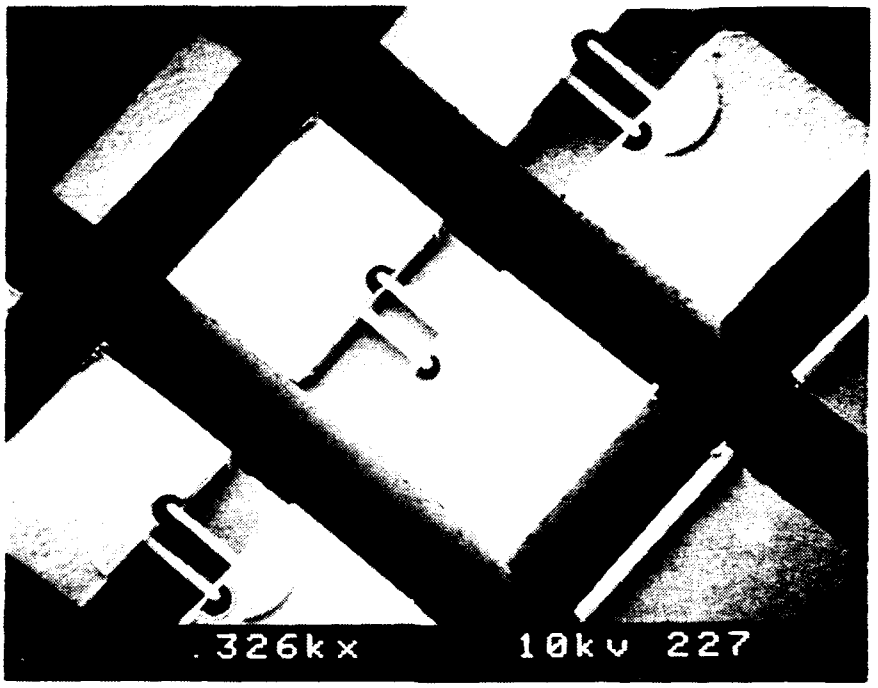


Figure 5.18 SEM Photograph of the Finished Diode Pair

CHAPTER 6

FABRICATION RESULTS, PROBLEMS, AND SOLUTIONS

6.1 Introduction

This chapter presents the results obtained with the fabrication technology discussed in Chapter 5, and problems encountered during its development. The physical results are presented in the first section below. The following section then discusses the solution of the five major problems encountered in this research. These problems were: an oxide attack during ohmic contact formation, poor anode quality, unpredictable anode contact finger thickness, an undesired surface channel etch of the GaAs near the anode, and wafer curling after lapping.

6.2 Fabrication Results

Three batches of diode pairs were made using the fabrication sequence discussed in the previous chapter. The typical diode pair is shown in the scanning electron micrograph presented as Figure 6.1. This particular device comes from the third batch (SD2T3). The chip is five mils wide, ten mils long and was mechanically lapped to a thickness of one mil. The surface channel is six microns deep. The anode contact fingers, which span the channel, are 50 μm long, and contact anodes 1.5 μm in diameter. These fingers are mechanically robust and maintain contact with the anode at cryogenic temperatures (20K).

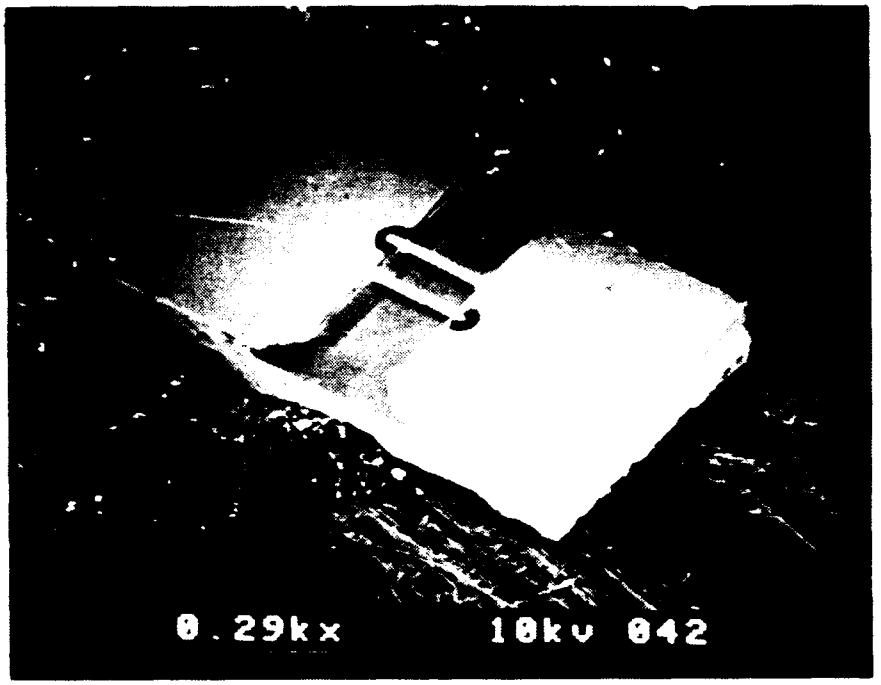


Figure 6.1 An SEM Photograph of the Monolithic Diode Pair

6.3 Problems and Solutions

Two major problems existed with the Surface Channel technology at the beginning of this research, and three new problems were encountered during process development. These problems and their solutions are discussed below.

6.3.1 Oxide Attack During Ohmic Contact Formation

The tin/nickel plating solution used at the beginning of this research attacked the oxide at the photoresist interface as shown in Figure 6.2. This problem was studied by Bishop and Ostdiek. Bishop decided that the attack was related to the uncontrolled pH of the SnNi solution, and therefore ordered a commercial, pH controlled solution (Nistan).

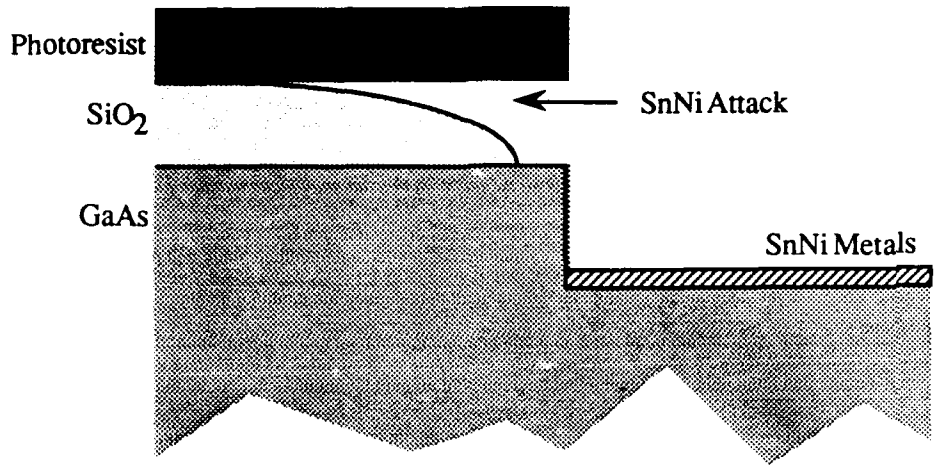


Figure 6.2 SnNi Plating Solution Oxide Attack

In the meantime, a process requiring two photolithography steps was investigated. First, the normal photolithography was performed. Then two of the six sets of alignment markers were covered with photoresist to preserve them for the second lithography. The photoresist was applied by hand with a thin wire. Then the oxide etch was performed as shown in Figure 6.3. The oxide etch back is also performed at this time, and the photoresist removed when finished. Next, the second photolithography opens areas for the GaAs etch and electroplating, while shrouding the oxide in photoresist as also shown in Figure 6.3.

This technique protected only half of the devices, and the attack was localized to specific points of failure. Although no regular pattern was observed for the attack, it is believed that misalignment of the second lithography contributed to this attack. This process was repeated changing only the plating solution. A 50°C Nistan solution was used instead of the SDL SnNi solution, and no oxide attack was observed. The misalignment of the Nistan sample was the same as that of the SDL SnNi sample.

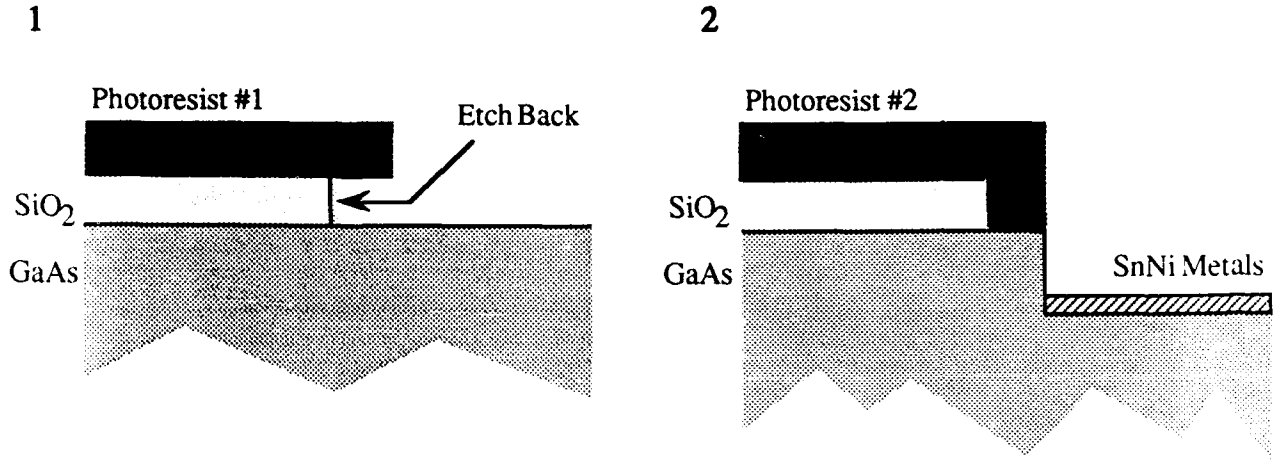


Figure 6.3 A Two Step Test of Photoresist Coverage

The two samples were then tested electrically. The resistance of the Nistan sample was ten times that of the SDL Sn/Ni sample before alloy. Fortunately however, the samples had identical resistances after alloying. Bishop also found that the Nistan solution was compatible with the standard, single lithography process.

At this time it was noticed that a fibrous debris, or "scum", was left on the wafer after developing the photoresist as shown in Figure 6.4. This photoresist scum was then removed with an oxygen plasma etch before the oxide etch. This etch was limited to ten minutes to avoid erosion of the photoresist mask.

The Nistan based technology was used with excellent results on over 15 batches of planar diodes until the SDL moved into its new clean room facilities. Then, in the new facility, the oxide was found to be regularly attacked, but not always. The two wafers shown in Figures 6.5 and 6.6

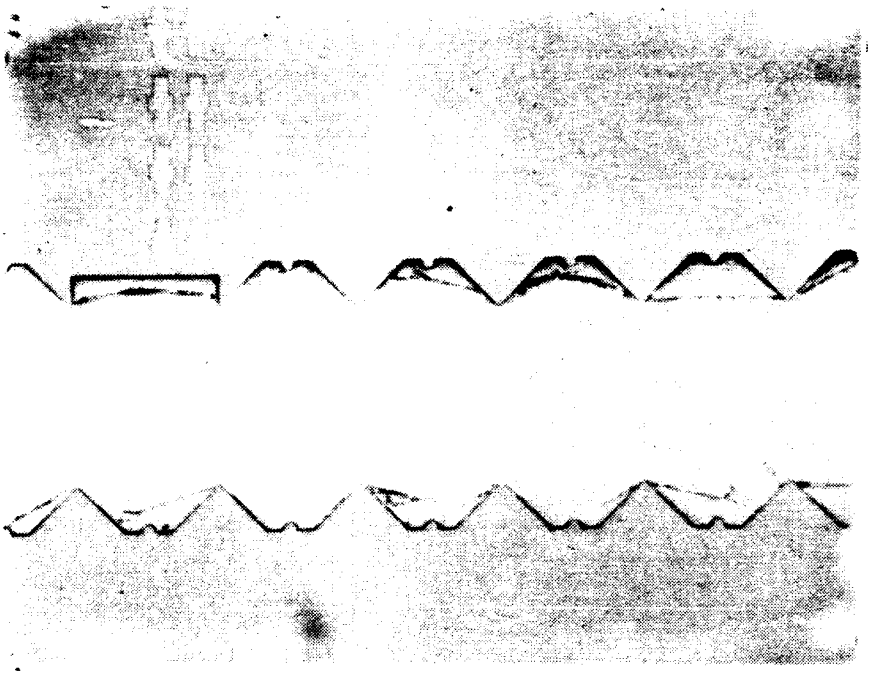


Figure 6.4 Photoresist Debris Left After Development

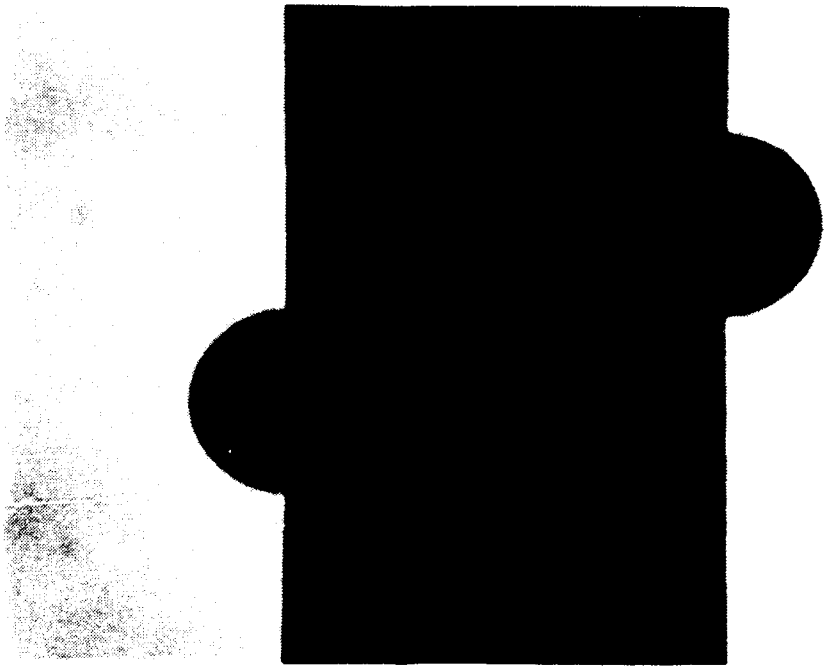


Figure 6.5 Desired Etch Back Results

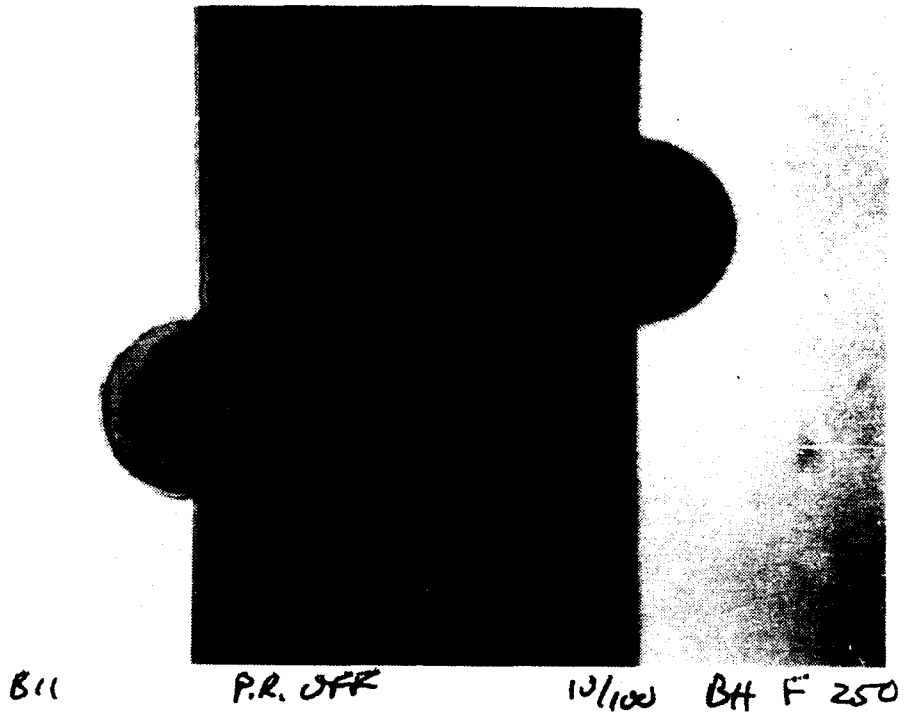


Figure 6.6 Oxide Attack During the Etch Back Step

underwent identical photolithography, and were processed together in an identical fashion. These wafers appeared identical until the final etch back step. This oxide attack was eliminated by adding a second hard bake at 150°C to improve photoresist adhesion to the oxide. Both oven and plate baked resists performed well; however, the oven baked resists were difficult to remove later.

Past experiences with the SnNi/Ni/Au ohmic contact technology used at the SDL have taught us to expect new problems to develop at any point in the future. The process is very hard on the photoresist since it is expected to withstand two different chemical etchants and four electroplating solutions. It is surprising that the photoresist usually adheres well throughout all this processing. While simple fabrication technologies are used to fabricate them, the contacts are metallurgically complex. The alloy temperatures,

times, and methods leave little room for error. Also, the fabrication requires over five continuous man-hours, and is at times tedious. Today however, the SnNi/Ni/Au ohmic contact technology used at SDL reliably produces good ohmic contacts.

6.3.2 Anode Burn Out

The original Surface Channel technology used pulsed electroplating to form anodes. In this process a capacitor was charged to a given voltage, and then discharged through the plating solution and sample. Experience gained over years fabricating whisker contacted diodes indicated that this was required to overcome a space charge region that forms in the solution near the GaAs, and plate a monolayer of atoms. This technique produced excellent whisker contacted anodes; however, it consistently failed to produce high quality anodes for the planar technology. Bishop noticed that the anodes had very low turn on and reverse breakdown voltages, and a high ΔV between 10 and 100 microamps of forward current. In effect, the anodes appeared to have been burned out, having been damaged by a large current. The diode is formed when the first layer of metal atoms is plated on the crystal. So most of the pulses are used to fill the anode well with metal, not form the diode. Each of these subsequent current spikes may damage the diode.

This research began with an effort to find an electroplating environment that would not damage the anodes. Factors influencing this environment are voltage, capacitance, and resistance of the plating circuit; as well as pulse rate, shape, and plating geometry which includes the anode to cathode area ratio. The plan was to vary one electrical parameter and note its effect on anode quality.

Capacitance was chosen to be studied first. After studying six batches of anodes it became apparent that two factors were important. First, the batch plated with the smallest capacitor (0.15 μF, 28 V) yielded the only set of good anodes. This capacitance can only supply a small amount of charge. Although it does so in a short time, this current is divided among hundreds of anodes resulting in a low peak and average current. It was concluded that a rectangular pulsed plating current might be used to successfully plate anodes. This pulse could supply enough charge to plate a monoatomic layer of platinum atoms, while avoiding the large current spikes that can damage the anode during capacitive discharge plating.

Secondly, it became obvious that geometry was important. The mask set contains arrays of test anodes similar to whiskered diodes, and isolated device anodes. The ohmic contact pads were covered by either an oxide or photoresist to isolate these anodes to force larger currents through them. It was observed that the test array anodes were consistently better than the isolated anodes. Also, each wafer contained some device anodes that were near cracks or pinholes that allowed the nearby ohmic contact to plate. These anodes were as good as those of the test array, and better than the isolated anodes. This suggested that the currents used were too great for a single isolated anode, and that a nearby plating area was required to protect the anode. To test this idea one batch of anodes was plated using a large (100 μF) capacitance with exposed ohmic contacts pads. These anodes had good turn on and breakdown voltages. However, the *I-V* curve was electrically unstable, exhibiting what is referred to as creep.

It seemed then that a combination of low capacitance, or square wave plating with exposed ohmic contacts was worth investigating. It was not pursued however, because

Bishop discovered that DC plating with exposed ohmic contact pads consistently yielded excellent device anodes. The anode study was abandoned because Bishop's technology worked so well, and there were other problems to solve.

6.3.3 Thin Anode Contact Fingers

A problem was encountered finding the correct electroplating currents for the anode contact fingers. The first attempt at plating the anode contact fingers was on a scrap wafer using a current of 250 μA for 20 minutes. These fingers plated too thick, and actually overflowed the confines of the photoresist mask and spread horizontally. The current was reduced to 20 μA for the first batch of diodes (SD2T1). These fingers plated to less than 0.25 μm thick. They were thin enough to bow, yet they were strong enough to be soldered into a mixer current.

The plating area was then compared with that of the Surface Channel diode. This showed that a current of 111 μA was required for the $3A/ft^2$ current density recommended for the Selrex BDT-200 gold solution by manufacturer. Therefore a current of 111 μA was used as the observed DC value of the square current waveform (AC current = 163 μA) for the second batch of diodes (SD2T2). These fingers were even thinner than those of the first batch. They are shown in Figure 6.7. The following gold sputter etch step actually removed some fingers altogether. These fingers were originally less than 0.15 μm.

At this point it was suspected that plating current was being shunted around the chip through some leakage path, possibly at the black wax seal on the electroplating probe. Gold was present on the probe tip. However, no conclusion could be drawn from this fact since other researchers had been plating gold at this time with no seal.

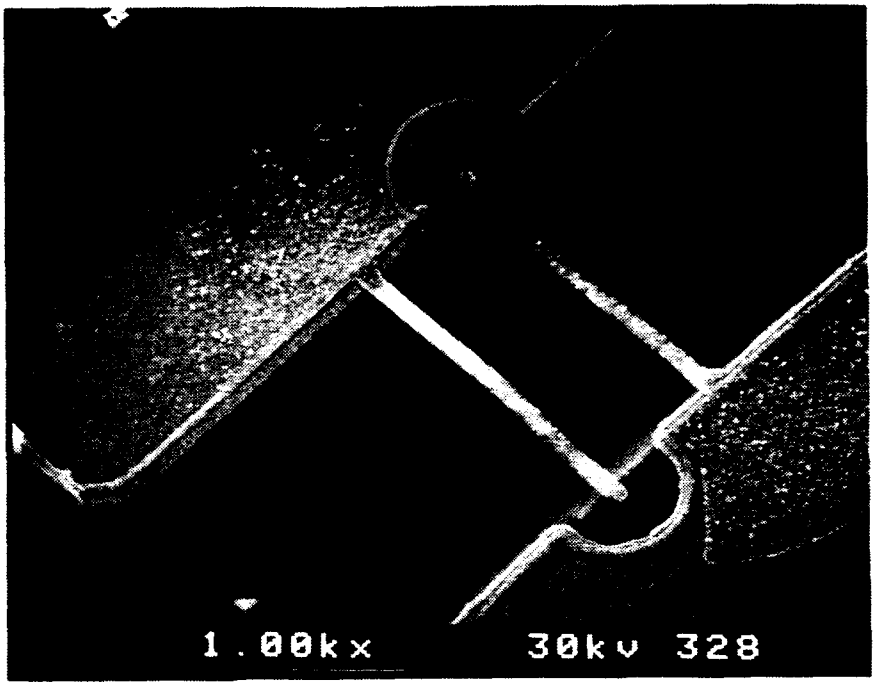


Figure 6.7 Thin Anode Contact Fingers

Plating fingers on the third batch (SD2T3) was approached very carefully. The black wax seal was inspected, and a current of 150 μA was used. A surface step profile measurement (Tencor) indicates that these finger metals were less than 0.9 μm thick. Therefore, the finger photolithography, and plating were repeated using a current of 175 μA. Little plating occurred though, because a large hole opened in the black wax seal. This 175 μA plating was attempted again, successfully plating the fingers to a thickness of 2.7 μm. These fingers, shown in Figure 6.8, appear to be misaligned with respect to the anode. Actually, the first plating was properly aligned and covers the anode. The third plating attempt was misaligned because the plating tab, which the probe contacted in the second attempt, was covered by a thick layer of gold. This nonplanar feature caused the wafer to shift when vacuum contact was attempted with the mask aligner.

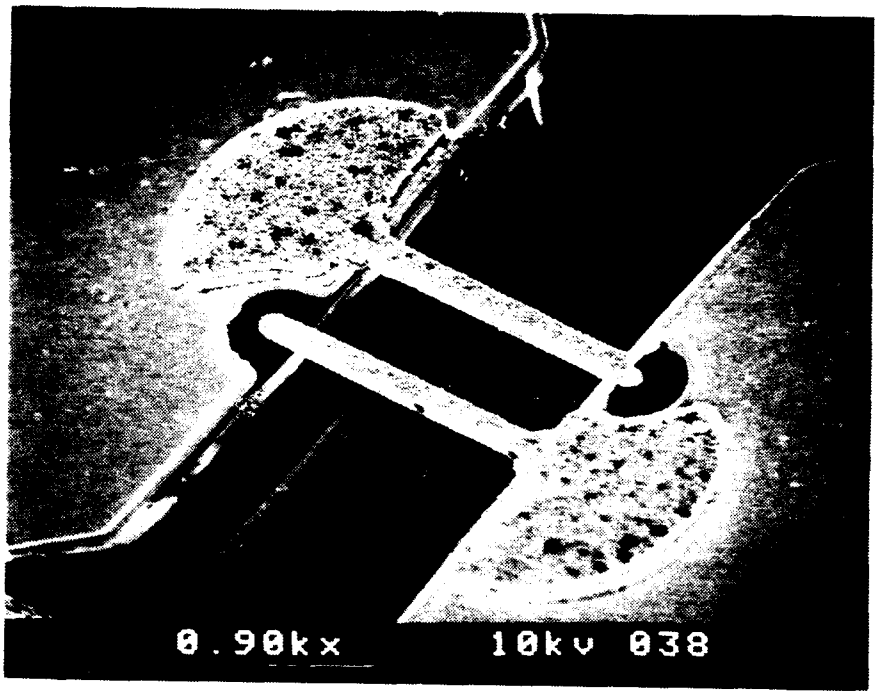


Figure 6.8 Thick Anode Contact Fingers Formed in Multiple Plating Steps

A fourth batch (SR2T1) was then plated with 200 μA resulting in 2.5 μm thick fingers. It therefore seemed that the correct current was found. However, this current is nearly twice that scaled from the Surface Channel technology. It was decided that pinholes must exist in the black wax seal, which short the wafer and account for the unpredictable results.

The probe was therefore sealed in three layers of black wax in the next batch. First, black wax was forced between the probe and its insulation, and the tip sealed. After drying with a heat lamp, the exterior of the probe insulation and tip were again sealed and dried. Finally, the seal was carefully removed from only the apex of the tip. Contact with the wafer was made in a third black wax seal. Careful inspection showed that each layer did contain pinholes, which have since been attributed to the use of trichloroethane

instead of trichloroethylene to liquify the wax. In spite of these pinholes, the three layer seal consistently yielded plating thicknesses of 3 μm with 111 μA of current in the next six batches plated. Figure 6.9 shows the results obtained for the SD1T2 batch.

It was also discovered that vigorous random mechanical agitation during the entire 20 minutes is critical for smooth, uniform results. Both stir bead and N_2 bubbler agitation were tried, but failed to provide uniform coverage in ten test batches of Surface Channel diodes. The only method that yielded good results was to attach the electroplating fixture to a ring-stand with the wafer in the plating solution. Then to randomly tap the fixture for the full 20 minutes at 120 taps/minute.

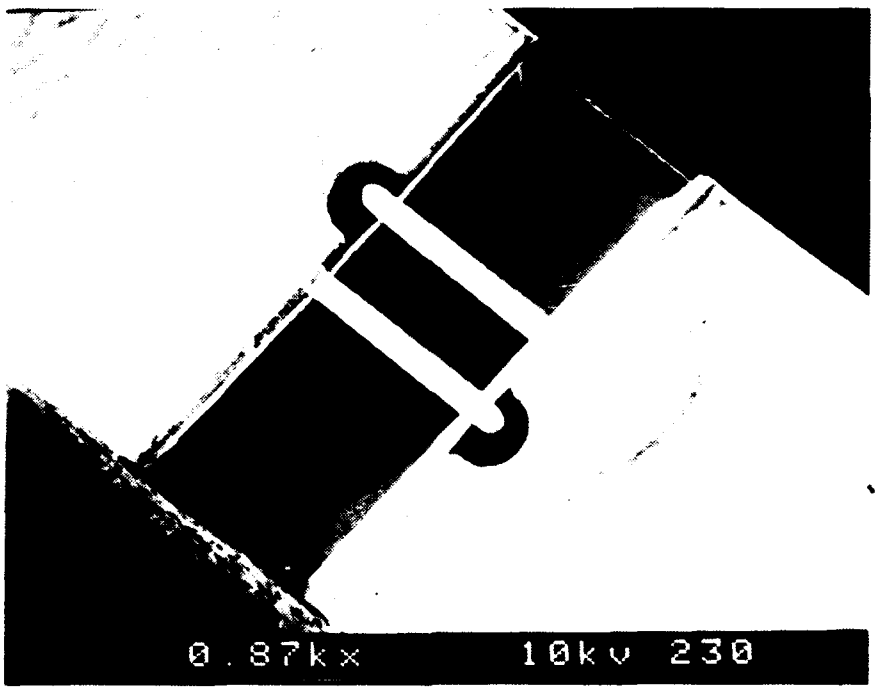


Figure 6.9 Successful Plating of 3 μm Thick Fingers

6.3.4 Surface Channel Attack of Anode Region

Another problem encountered while developing the diode pair technology is an attack of the GaAs near the anodes. A typical example of this attack is shown in Figure 6.10. For comparison, Figure 6.11 shows the anode region on the other side of the channel which was not attacked. These micrographs come from the first batch of diodes for which the surface channel mask was misaligned towards the right anode of the pair. Every right anode on the wafer was attacked as shown. This attack can be avoided by carefully aligning the channel mask and minimizing the duration of the Surface Channel etch.

The attack is believed to be caused by a separation, or lifting, of the oxide from the GaAs surface near the ohmic contact during the 350°C alloy step. It usually occurs whenever the surface channel reaches the ohmic contact pad. Then the etchant appears to wick into the anode region along the edge of the ohmic contact.

A sequence of photographs taken of wafers used to develop the anode technology show this lifting. First, Figure 6.12 shows an oxide that has been partially chipped away, with gold in both the chipped region, and under the nearby oxide. This is illustrated in Figure 6.13. The gold is electroplated along with the anode and does not adhere to the insulating SiO_2. The chipping is caused by the use of ultrasonic agitation during plating. Figure 6.14 shows a complete oxide with no chipping and some plating under the oxide. Also, Figure 6.15 shows an oxide with the attacked region completely chipped away and plated.

This anode region attack is not observed in the single diode Surface Channel technology because the channel does not come within a micron of the ohmic contact.

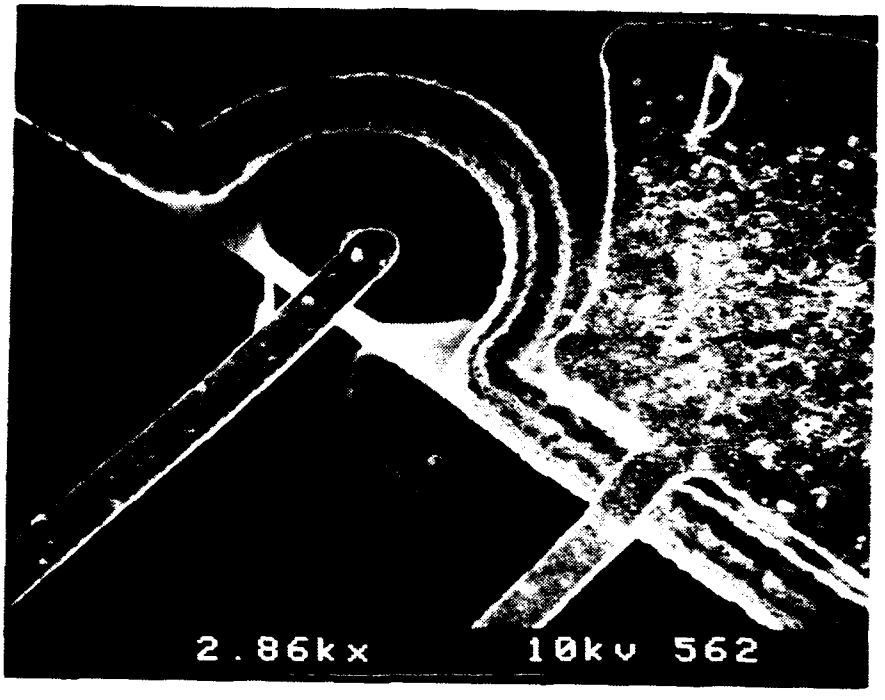


Figure 6.10 Surface Channel Attack of GaAs Near the Anode

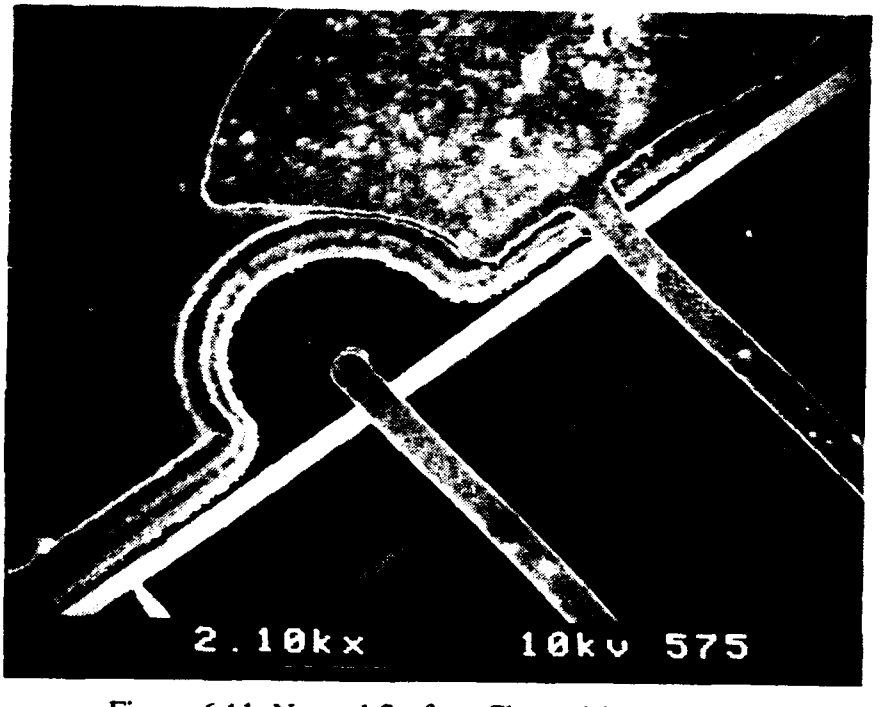


Figure 6.11 Normal Surface Channel Etch Results

Figure 6.12 Damaged Oxide Near the Ohmic Contact

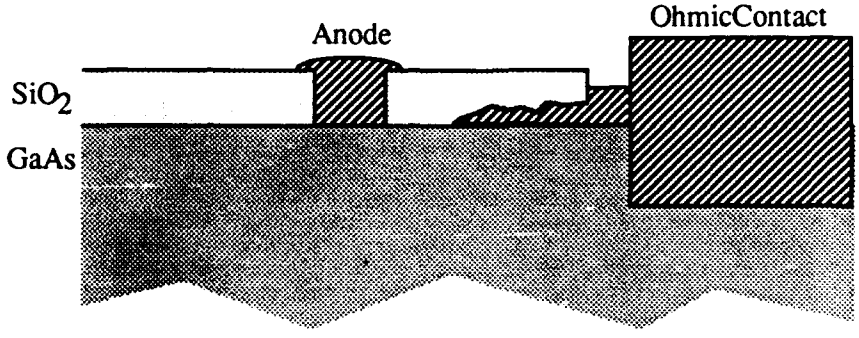


Figure 6.13 Sketch of Oxide Damage Near the Ohmic Contact

Figure 6.14 Oxide Lifting Near the Ohmic Contact

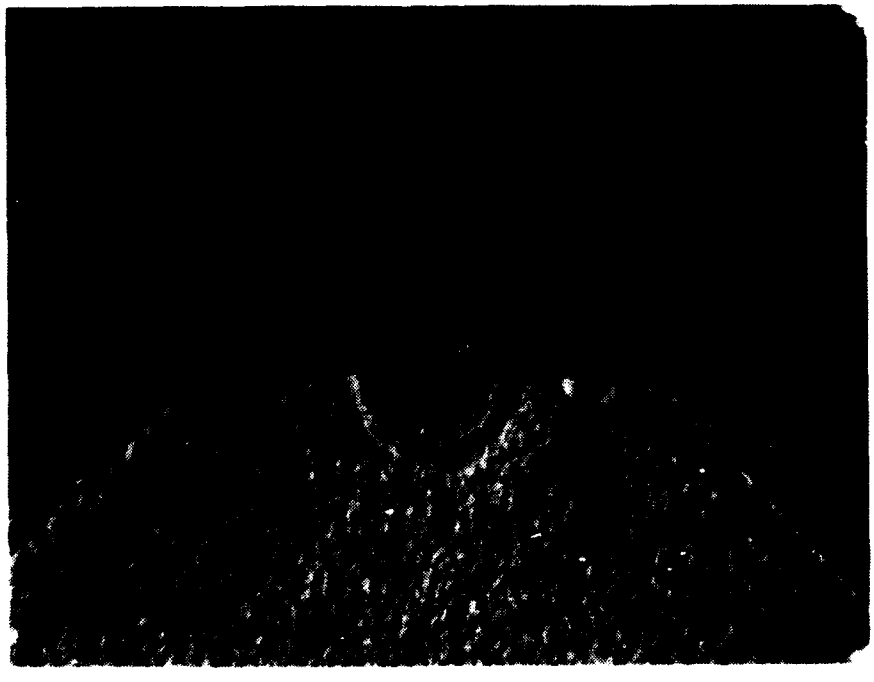


Figure 6.15 Oxide Chipping Near the Ohmic Contact

The Surface Channel pattern is 8 microns from the anode and ohmic contact. However, there is little room for misalignment in the diode pair mask set because the channel is five microns from the anode. On the wafer though, the ohmic pads expand a couple of microns into the etch back area. This means that a perfectly aligned channel edge is three microns or less from the separated SiO_2.

It should be noted that no correlation was found between the *I-V* characteristics of the anode and this attack. However, this attack may have an effect at RF, perhaps causing a mismatch in series resistance.

6.3.5 Wafer Curling

The second and third batches of diode pairs were mechanically lapped to a thickness of 1.5 mils and 1 mil respectively. Both wafers curled when removed from the lapping block. The third batch of diodes curled so much that it had to be cleaved into two pieces to be diced. This curling did not degrade the electrical performance of the diodes, however the substrate appeared brittle and cracked after dicing as seen in Figure 6.1. These cracks are undesirable since they may make space certification of the device more difficult.

This problem is solved by dicing the wafer before lapping. First, a five mil deep cut is made along the chip edges. (This has an added advantage of allowing on wafer testing of the diodes since the devices are no longer connected.) Then one mil deep reference cuts are made to be used as an endpoint indicator. Next, the wafer is mounted face down on the lapping block, and is carefully lapped until the reference cuts are visible. This technique, developed by Bishop and Ostdiek, yields excellent results. The dicing of batch SD1T2 is shown in Figure 6.16. Notice the chips have smooth sides with little or

no tearing of the ohmic contact.

6.4 Summary

This chapter discussed the fabrication of the anti-parallel diode pair. Three prototype batches were fabricated before the correct set of fabrication parameters were discovered. The problems encountered and their solutions are also discussed. Two problems affecting the Surface Channel technology had to be solved before the prototype batches were attempted. These were an attack of the oxide while electroplating the ohmic contact metals, and anode damage suffered during their formation by pulse plating. Problems encountered while fabricating the prototype batches included anode contact fingers that were too thin, attack of GaAs near the anodes by the surface channel

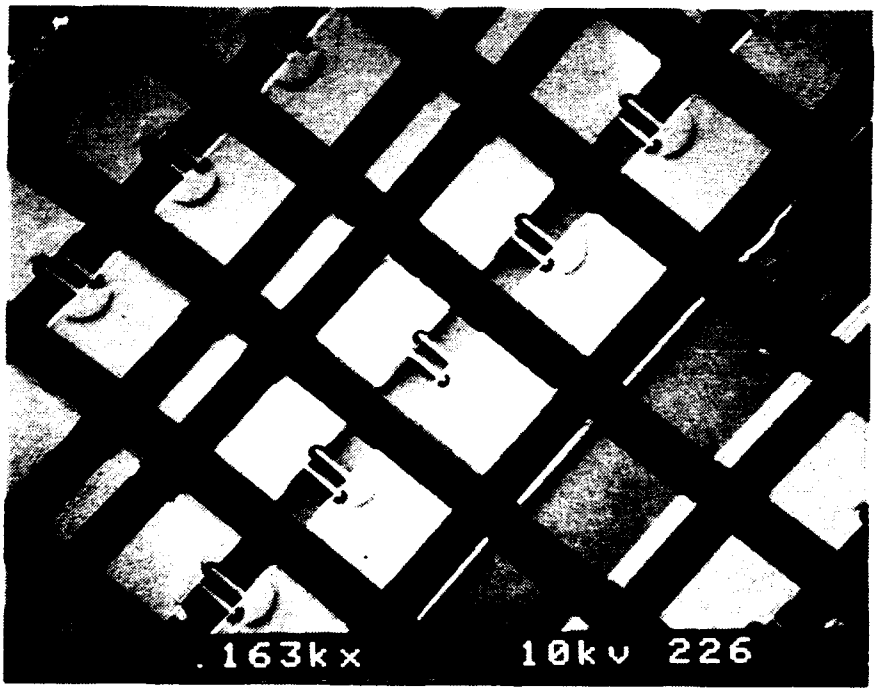


Figure 6.16 Isolation of Diode Pairs by 5 mil Dicing Cuts

etchant, and wafer curling after lapping.

At this point four of the five major problems encountered have been solved. Future efforts should focus on solving the surface channel etch attack of the GaAs near the anode. The best solution to this problem appears to require development of an ohmic contact technology that requires no alloying at high temperatures. Such a development would make the ohmic contacts easier to fabricate, and allow anodes to be plated before the ohmic contact is deposited. This solution was investigated, and is discussed in Chapter 8.

CHAPTER 7

PERFORMANCE

7.1 Introduction

This chapter discusses the electrical performance of three batches of diode pairs fabricated using the technology outlined in chapter 5. The current/voltage characteristic and capacitance of the diodes are presented first. Then the observed noise properties of the diodes are discussed. The RF evaluation of the diodes in a 183 GHz subharmonically pumped receiver composes the final section.

7.2 Electrical

Three batches of diode pairs were fabricated with the standard sequence; each with 50 micron long anode contact fingers separated by 20 microns, and anodes 1.8 microns or less in diameter. The electrical characteristics of these diodes are summarized in Table 7.1.

Table 7.1
Characteristics of Standard Diode Pairs with GaAs Substrates

Batch	SD2T1	SD2T2	SD2T3	
Anode Diameter	1.8 ± 0.2	1.6 ± 0.2	1.5	μm
V_{knee} (1μA)	---	711	715	mV
10(μA)	794 (3)	789 (4)	785 (5)	mV
ΔV	72.3 (0.5)	72.0 (0.6)	71.8 (0.2)	mV
η	1.21 (0.008)	1.21 (0.010)	1.21 (0.003)	
R_S	8.6 (0.7)	9.0 (1.4)	7.4 (0.8)	Ω
V_{br}	-5.8	-5.5	-6.2	V
C_{TOTAL}	19	15	18	fF
C_{pp}	10	7.5	10	fF
C_{jo}	4.8	3.8	4.0	fF

The ±0.2 indicated for the anode diameters of first two batches indicates the uncertainty in this value. It is not a standard deviation indicating variance from a mean value. The data in parentheses indicates the average difference in that parameter between the two diodes of a single chip. For example, the average 10 μA knee voltage of batch SD2T1 is 794 mV, and the average difference in this voltage between the two anodes of one chip was 3 mV. These data indicate that the anodes are very well matched. This means that there is little asymmetry in the *I-V* response shown in Figure 7.1 for the diode pair.

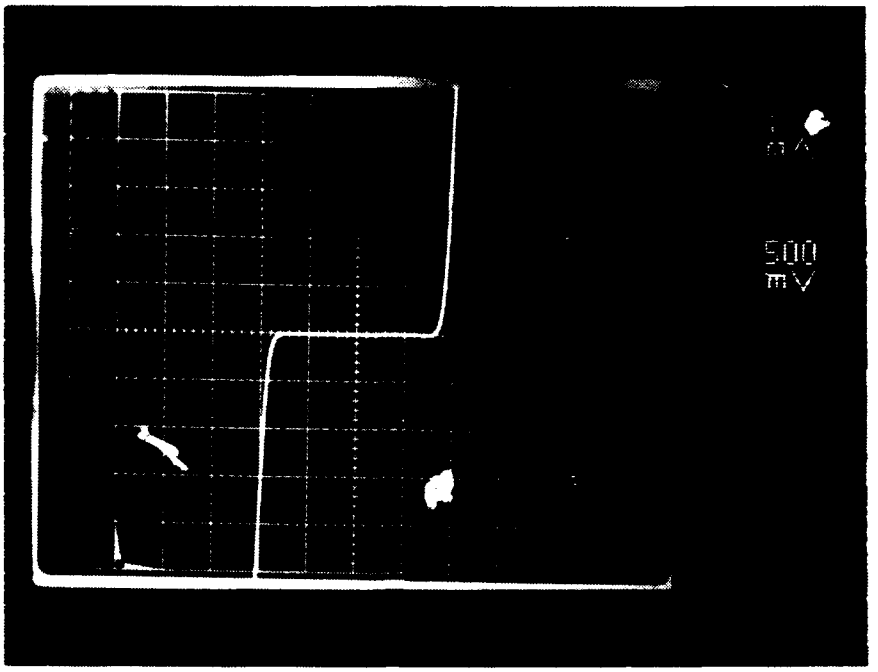


Figure 7.1 Observed *I-V* Characteristics of the Diode Pair

The parameter ΔV is the voltage difference observed for forward currents of 100 μA and 10 μA. The ideality factor η is calculated from a voltage difference for low currents as:

$$\eta = \frac{V_2 - V_1}{\frac{kT}{q} \ln \frac{I_2}{I_1}} \tag{7.1}$$

and is related to ΔV (in mV) at room temperature for $I_2 = 10I_1$ as:

$$\eta = 16.8 \cdot \Delta V \tag{7.2}$$

The observed ideality factor of 1.21 is excellent for anodes of this size and epitaxial layer doping density.

The series resistance R_S of diodes from the first two batches is higher than expected because of their very thin fingers. The series resistance is conveniently measured from the change in the slope of the log I vs V curve as:

$$R_S = \frac{(V_4 - V_3) - (V_2 - V_1)}{(I_4 - I_3)} \tag{7.3}$$

where I_1, I_2, I_3, and I_4 are 10 μA, 100 μA, 1mA, and 10 mA, and $V_2 - V_1$ is ΔV. This method ignores the temperature variation of the anode with current. It has been estimated to be too low by R_b [77]:

$$R_b = \frac{\eta k}{q} \rho_T V_{knee} \tag{7.4}$$

where ρ_T is the thermal resistance of the diode (≈3°K/mW for a 2.5 μm anode). This error is approximately 0.3 Ω for a 2.5 μm anode and is expected to be greater for smaller anodes.

The reverse breakdown was measured at a reverse current of 1 μA after one finger was intentionally broken. These anodes had very stable *I-V* characteristics, and did not exhibit creep. Creep is defined as the difference in voltage observed at a forward current of 10 μA after a momentary 100 μA reverse current was forced through the anode.

The total capacitance of the diode pair was measured with an HP4275A LCR meter at a probe station. The pad-to-pad capacitance C_{pp}, was measured after both fingers were removed. Then the zero bias junction capacitance of the two parallel diodes is estimated as:

$$C_{jo} = \frac{C_{total} - C_{pp}}{2} \tag{7.5}$$

The effect of a deep surface channel was investigated by fabricating the second batch of diodes with a 10 μm deep channel instead of the standard 6 μm. This lowered C_{pp} by 25%. A scale model was built to further study this effect and is discussed in chapter 8.

7.3 DC Noise

The room temperature noise properties of the diodes were measured as a function of forward bias current. These observed diode equivalent noise temperatures provide another indication of diode quality. Good diodes will exhibit minimal noise characteristics throughout the range of useful currents.

The noise measurement system at the SDL [78], [79] uses a noise meter to measure directly the noise power coupled into the noise system by the diode, and a network analyzer to measure the reflection coefficient. The diode's equivalent noise temperature is graphed as a function of forward current with error bars indicating the total uncertainty of the measurement.

The observed equivalent noise temperature of one anode of the typical diode pair with a GaAs substrate is given in Figure 7.2. This measurement was taken at room temperature. The solid line is the noise predicted from the measured *I-V* response using the theory discussed in section 2.2.6. The actual data points are the ×'s. The error bars indicate a large uncertainty at low currents, where the system is most sensitive to errors in diode reflection coefficient. The room temperature noise characteristics of the diode pair on a quartz substrate (discussed in Chapter 8) is presented in Figure 7.3. Notice that the noise properties of the diode pair do not appear to change by replacing the GaAs substrate with quartz. The observed equivalent noise temperature of the GaAs substrate

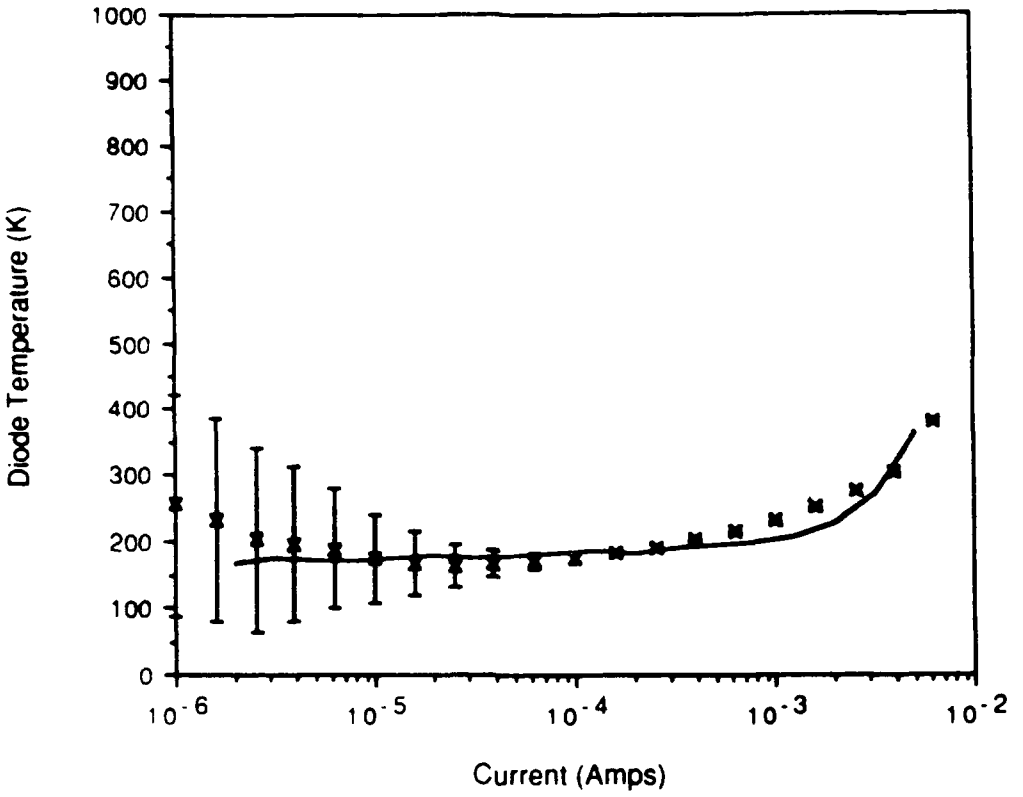


Figure 7.2 Noise Characteristics of the GaAs Substrate Diode at Room Temperature

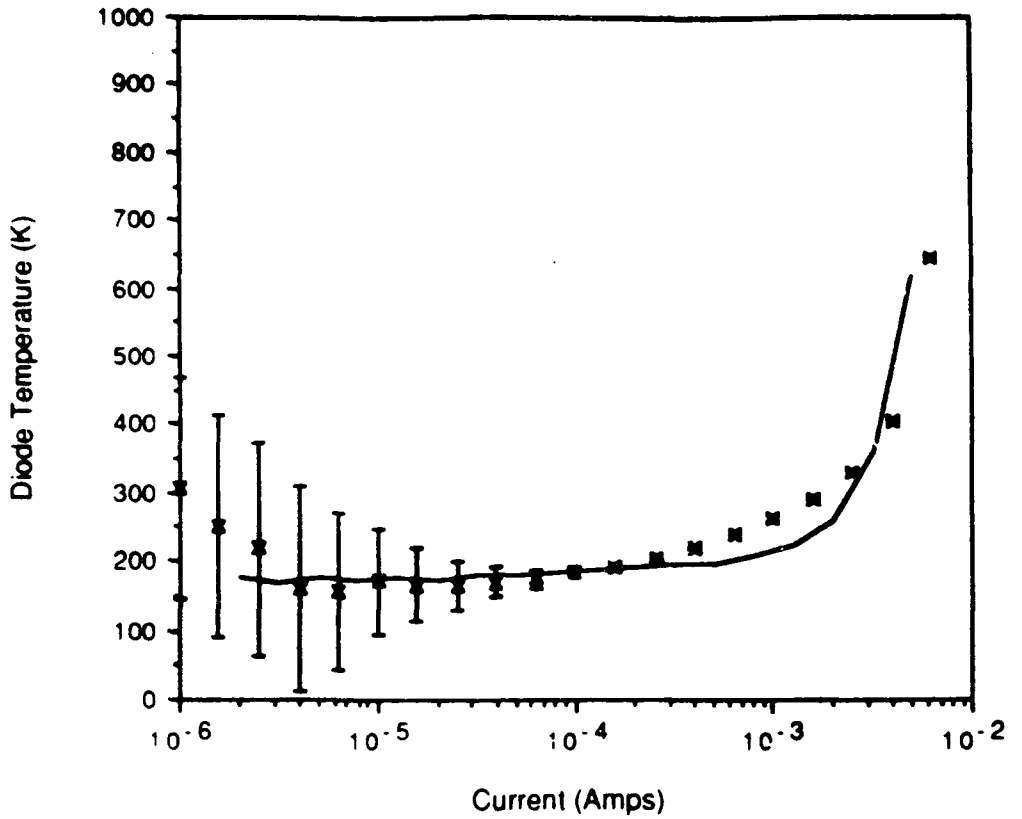


Figure 7.3 Noise Characteristics of the Quartz Substrate Diode at Room Temperature

diode at 25K is shown in Figure 7.4. These data indicate that the diodes are excessively noisy at cryogenic temperatures, indicating that the anode quality can be improved. This problem appears with whisker contacted diodes as well, and is thought to be associated with damaged GaAs caused by relief of stresses in the SiO_2 when the anode hole is being etched [80]. It is corrected by carefully timing the oxide etch so that the anode hole opens just enough to allow plating, but not enough to remove the the oxide covering the damaged GaAs at the hole's periphery. This is possible for the whisker contacted diode, since each chip is plated separately. Therefore, several whisker contacted diode chips may be sacrificed to find the correct etch time. This procedure is not possible with the

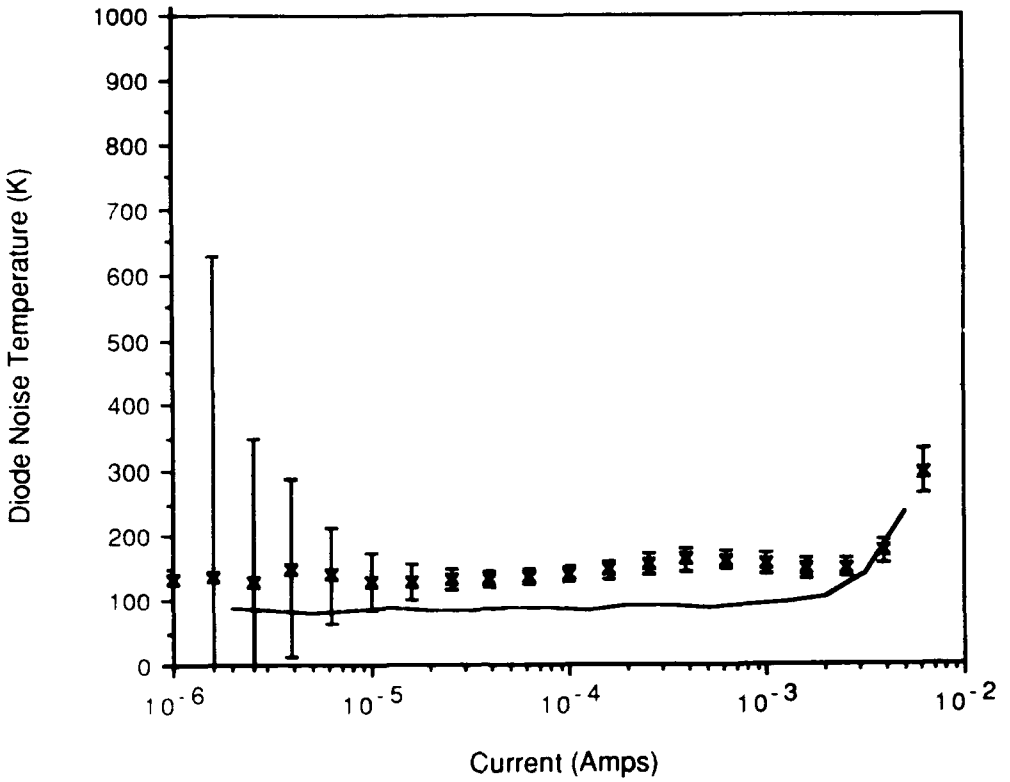


Figure 7.4 Cryogenic Noise Test Results for a GaAs Substrate Diode

planar diode chip because all chips in the batch are plated at the same time. Furthermore, the oxide thickness varies across the wafer, so a given etch time would be correct for only some of the devices in the batch. Further research is needed to find a solution to this problem; however, the diodes developed in this thesis are designed specifically for room temperatures, where they exhibit excellent noise characteristics. The next section will show that the diode pair also exhibits excellent noise characteristics at RF frequencies.

7.4 183 GHz Subharmonically Pumped Mixer at Aerojet

The planar diode pairs were evaluated in a 183 GHz subharmonically pumped mixer at the Electrosystems Division of Aerojet-General Corporation in Azusa, CA.. This mixer, described by Galin [81], was originally designed for whisker contacted diodes that were soldered to a stripline circuit on a fused quartz substrate. The monolithic diode pair was used in their place with no modification to the circuit. These mixers yielded performance equal to, or better than the performance of mixers with whisker contacted diodes operating at the same frequencies.

Four diode pairs were soldered onto four identical mixer circuit striplines. All four assemblies were then tested in the same waveguide housing. These mixers operated with an LO of 91.65 GHz and an IF bandwidth from 0.75 to 7.75 GHz. The IF band was multiplexed into three IF channels centered at 1, 3, and 7 GHz. This allows all three channels to be observed simultaneously. The channel bandwidths were 0.5, 1.0, and 1.5 GHz respectively [83].

The receivers were evaluated using a "hot-load/cold-load," or Y-factor technique to calculate their equivalent noise temperatures [82]. Each load consisted of a microwave absorbing material at a fixed temperature (300K and 77K) and observed alternatively as shown in Figure 7.5. The observed powers are then linearly related to the load temperatures as shown in Figure 7.6 and the equivalent receiver temperature is calculated

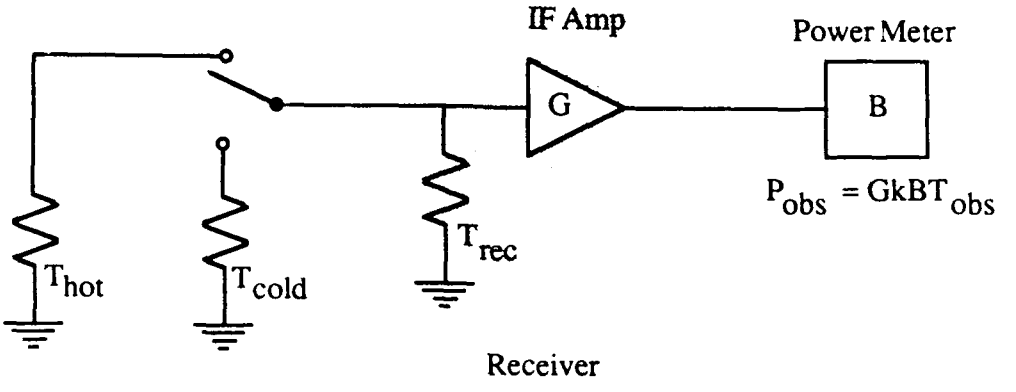


Figure 7.5 Block Diagram of a Receiver Noise Measurement System

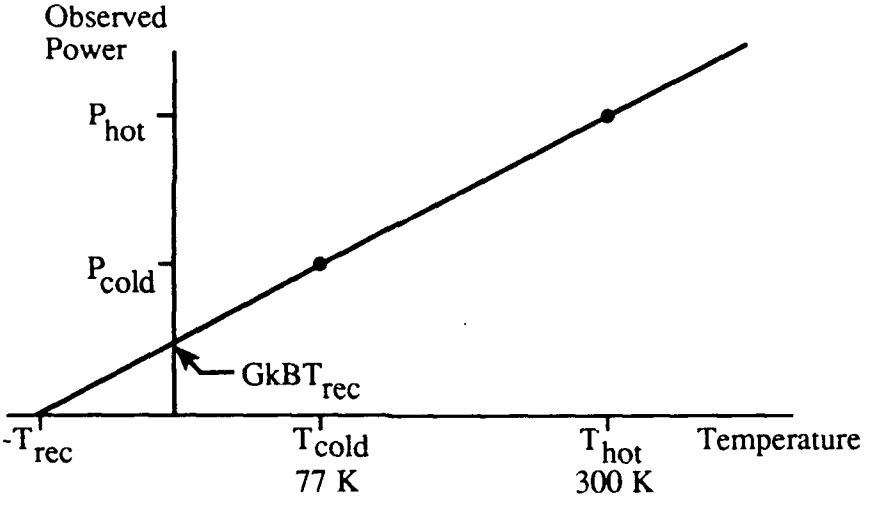


Figure 7.6 Y-Factor Calculation of Equivalent Receiver Noise

from the observed power ratios as:

$$T_{rec} = \frac{T_{hot} - Y \cdot T_{cold}}{(Y - 1)} \tag{7.6}$$

$$Y = \frac{P_{hot}}{P_{cold}} \tag{7.7}$$

This temperature can be expressed as a noise figure through (2.33).

The observed receiver noise figure of each mixer assembly is shown in Figure 7.7. The horizontal bars indicate the bandwidth of each channel. These noise figures include an IF loss/noise figure of 1.5, 1.7, and 2.0 dB respectively in each channel. For comparison, data is also presented to indicate the performance of the "best" whisker contacted diodes in a similar mixer. The stripline circuit containing diode four was tested in a separate waveguide housing of the same design, but manufactured differently. This assembly yielded the best performance observed, in large part due to the improved quality of the new waveguide. It should be kept in mind that the performance of the whiskered diode was optimized by design, and that no optimization was attempted for the planar diodes. It is significant that the assemblies containing planar diodes required 10 mW or less LO power. This is 3 dB less than the LO requirements of the similar whisker contacted diode assemblies which were much more difficult to make [83]. This is

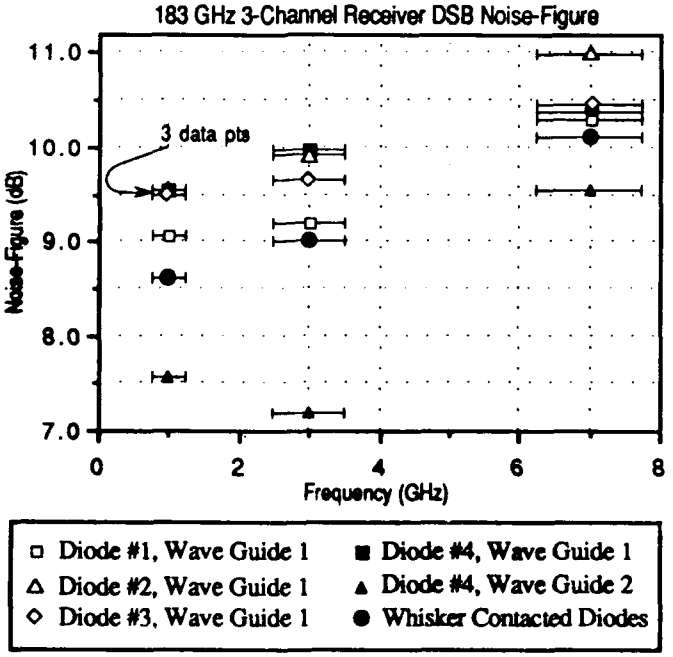


Figure 7.7 Comparison of Planar and Whiskered Diode Mixer Results

important because the main goal of using a subharmonically pumped mixer is to make the LO power easier to generate. Therefore, a diode technology that reduces the amount of LO power required is advantageous. Aerojet-General Corp. is currently space qualifying the planar diode pairs for use in the water vapor sensor on the Air Force Defense Meteorological Satellites (DMSP).

7.5 Additional Mixer Results

The diode pair has been tested in four other subharmonically pumped mixers. A summary of the preliminary results obtained in these mixers are summarized in Table 7.2. These data are presented in tabular format to enhance their legibility. This table is a compilation of data, and not a comparison since each mixer reflects different design goals, and each mixer is at a different point in its development phase.

Table 7.2
Preliminary Results of Additional Mixing Experiments

Research Group	RF Frequency (GHz)	SSB Conversion Loss (dB)	Typical LO Power (mW)
Univ. of Michigan	140	11.2	4.5
	180	12.8	<10
Univ. of Bath	130-210	8.5-13 (DSB)	---
Jet Propulsion Lab	200-230	6.5-11.5	<10
Millitech/NASA	140	10.5-16	6-16

The University of Michigan's mixer is a quasi-optical system that uses a wideband (30-240 GHz) log-periodic antenna, and a hyperhemispherical substrate lens to collect

both the RF and LO radiation [84]. The diode pair used in this mixer contained a quartz substrate. Notice that the performance of this mixer is comparable to those using GaAs substrate chips. The impedance of this diode pair was not matched to the antenna, and the LO power specified is that estimated to have been delivered to the antenna's terminals. Kerr's multiple reflection algorithm [38] has been used to analyze this receiver by dividing the system into two single diode problems, each with LO embedding impedances of zero for even harmonics and DC.

The University of Bath's mixer data is preliminary and applies to a double side band configuration. This data was taken with two separate stripline assemblies with diode pairs that were soldered at the SDL. Unfortunately both assemblies contained defects which degraded the mixer's performance. Better results are expected when better circuits are assembled [85].

The single side band noise figure of the JPL receiver was measured to be in the range of 9 to 12 dB, while the single side band conversion loss of 6.5 dB is excellent [86].

The Millitech/NASA mixer will be space certified to fly on the Space Shuttle to investigate the plasma that shrouds the spacecraft during re-entry. This is a part of a research program to develop an aero-braking technique for spacecraft returning from Mars [87].

7.6 Summary

This chapter summarized the electrical performance of the anti-parallel diode pair. The diodes exhibited excellent *I-V* and room temperature noise properties. The diodes appear to generate excess noise at cryogenic temperatures (25K). However, these diodes were designed for room temperature operation. Experiments conducted at Aerojet Electrosystems Division show that the monolithic diode pair performs as well as, or better than whisker contacted diodes in the same mixer. Also, excellent preliminary results are being obtained in four other subharmonically pumped receivers. The diode pair used in one mixer consists of a GaAs membrane that resides on a quartz substrate. The performance of this mixer is comparable to those of mixers using the standard diode pair with a thick GaAs substrate.

CHAPTER 8

OPTIMIZATION

8.1 Introduction

Use of the planar anti-parallel diode pair at submillimeter wavelengths will require two major design improvements. The anode diameter must be reduced to increase the diode's cut off frequency, and the parasitic circuit elements of the diode chip must be reduced. Additional concerns may include the need to bias the anodes individually to reduce LO power requirements, and reduction of the size of the GaAs chip. These issues are addressed in Section 8.2 below. Also two scale model studies were undertaken to gain information regarding the diode's parasitic reactances. These studies are discussed in Section 8.3. Finally, the design parameters for a 600 GHz diode pair are discussed in Section 8.4.

8.2 Design Variations

Variations on the fabrication technology mentioned in Chapter 5 are discussed in this section. Five variations were investigated experimentally. These are:

- the use of dry etching to reduce anode diameter,
- anodic thinning of the GaAs surface before anode plating to reduce noise,
- use of an etch-stop layer to remove or replace the high dielectric GaAs substrate,
- plating a metal heat-sink on the back of a membrane chip to reduce heating, and
- the use of a non-alloyed ohmic contact to simplify fabrication.

These five variations, plus the possible design of a chip that allows individual biasing of the diodes, are discussed.

8.2.1 Dry Etched Anodes

At submillimeter wavelengths it is important to decrease the $R_S C_{jo}$ product, which is directly related to the diode's cut off frequency. This means that anode diameters must be reduced to submicron dimensions. Unfortunately, the wet oxide etchants used during the surface channel diode development are isotropic, and this limits the diameters attainable to about one micron. The smallest anode formed on a surface channel diode prior to this research was 2.5 μm. Dry etching techniques, however, exhibit little undercutting and are therefore capable of producing anodes limited in size only by the mask set.

A reactive ion etching sequence was developed for the anti-parallel diodes that consistently produces anodes that are only about 0.1 μm larger than the mask. The sequence consists of transferring a one micron anode pattern to a film of AZ4110 photoresist. Then the underlying SiO_2 is etched in a reactive ion etching system, with a plasma formed from 94% CF_4 at 50 mTorr and 18% power, to leave 600 Å of oxide in the holes to protect the GaAs. This oxide is removed by means of a 17 second wet etch in BOE just prior to anode plating. This short wet etch expands the hole diameter to 1.1 or 1.2 μm.

This technique was used to fabricate the anodes of batches SD1T1 and SD1T2 whose average electrical characteristics are listed in Table 8.1. Two batches of diodes whose anodes are 0.9 μm in diameter were also produced. This was accomplished by underexposing the photoresist, and using a minimal BOE etch time to open the anodes. Although these diodes have not been characterized fully at the date of this writing, they have clearly demonstrated that 0.9 μm diameter anodes can be fabricated with this

technology.

Table 8.1
Electrical Characteristics of Dry Etched Anodes

	SD1T1	SD1T2
$V_{knee}(1\mu m)$	729 mV	747
ΔV	71.9 mV	71.8
R_S	8.7 Ω	11.0
V_{br}	-6.5 V	-6.9 V

8.2.2 Anodically Thinned Anodes

The quality of the GaAs/metal interface is critical to the performance of the diode. Several effects, such as crystal damage caused by SiO_2 deposition or chemical contamination, can degrade the quality of this interface seriously; causing unstable *I-V* characteristics and excess diode noise. In particular, Sherrill [80] has shown that an over-etch of the anode window prior to plating causes a large amount of damage along the anode periphery. This damage causes excess noise which is particularly noticeable at cryogenic temperatures. Fortunately, it is possible to anodically etch the GaAs surface, just prior to anode plating, to remove the damaged material and eliminate the excess noise [80], [88]. This is now a standard processing step in the fabrication of low-noise whisker contacted devices.

The use of anodic thinning of GaAs is important to the planar technology because all anodes in the batch are plated at the same time, and a slight overetch is required to ensure that all anodes are open. Unfortunately, anodic thinning cannot be used in the

standard planar diode fabrication sequence because the ohmic contact will short the anodic solution, preventing the GaAs from etching. Although we have attempted to seal the ohmic contact with photoresist, thereby allowing the etch, this was not successful because the photoresist would not seal the rough ohmic contact surface completely.

To circumvent this problem, it was attempted to etch the anode holes and perform anodic oxidation before the ohmic contact was formed. Two additional benefits are realized by inverting this order. The wafer surface is truly planar for the most critical photolithographic step, and better alignment is possible from mask level to mask level since the anodes themselves can be used as alignment markers.

The main problem with this process is that during the ohmic contact formation only the soft anodic oxide is used to protect the portion of the GaAs surface where the anode will be plated. Unfortunately, the batch of diodes created this way was rinsed in Microposit 1112A photoresist stripper, which contains buffered hydrofluoric acid, that may have removed this oxide before the ohmic contact step. The typical characteristics of the anodes are listed in Table 8.2. This batch exhibits an *I-V* instability referred to as creep. V_{creep} is the change in voltage observed for a 10 μA bias current after 100 μA of reverse current was forced through the anode.

Table 8.2 Electrical Characteristics of Anodically Thinned Anodes	
V_{knee} (1 μA)	661 mV
ΔV	73.7 mV
R_S	7.5 Ω
V_{br}	-3.8 V
V_{creep}	6.6 mV

Although this first attempt to thin the anodes anodically was not successful, anodic thinning will remain important to the fabrication of planar diodes since it is a proven method to remove the damaged GaAs before the Schottky metal is plated. A better method to achieve this will be to use a non-alloyed ohmic contact technology. This will allow the anodes to be etched and plated before the ohmic contacts are formed. Unfortunately a reliable non-alloyed ohmic contact technology was not available for this research. Since our main goal was to fabricate devices for room temperature evaluation, and excess noise is only an important problem at cryogenic temperatures, this technology was not pursued further.

8.2.3 Quartz Substrate

The principal advantage of whiskered diodes is their low shunt capacitances. The planar diode is significantly handicapped by the presence of two large pads overlying a thick GaAs substrate with a dielectric constant of 13. However, this parasitic pad-to-pad capacitance can be reduced if the substrate is either replaced by a material with a lower

dielectric constant, or removed altogether. A technique has been developed by Bishop [89] to achieve this, and this technique has been successfully demonstrated with the diode pair technology.

The GaAs wafer used in this process requires a thin layer of AlGaAs between the substrate and the buffer layer. The AlGaAs is used as an etch stop, since the chemical etchant used to remove the substrate removes GaAs much faster than AlGaAs. The fabrication process is identical to the standard fabrication until the wafer is ready for dicing. Then, the wafer containing the finished diodes is waxed face down on a glass slide and the substrate is etched away, leaving behind a membrane only a few microns thick. Because the surface channel was etched through the AlGaAs, no material exists between the pads except for the fingers and wax. Then a quartz wafer is bonded to the membrane by a thin adhesive film. The GaAs/quartz wafer is then diced, and the individual quartz substrate chips are released by dissolving the wax. The SEM photograph of this device is presented in Figure 8.1 shows the 5 μm thick device on a thick layer of adhesive and a 2 mil thick quartz substrate. The closer view shown in Figure 8.2 shows that the surface channel is preserved in the process. The adhesive forms the channel bottom.

Other researchers have used Van der Waal forces to bond a GaAs membrane directly to the quartz [90]. However, Bishop's technique is preferred for this application because the adhesive is soluble in a solvent, allowing it to be removed after the chip is soldered to a circuit. Then the device has no substrate as shown in the SEM photograph in Figure 8.3. The ohmic contact pads are now part of the stripline to which they are bonded, and their capacitance is associated with that of the stripline. The limiting

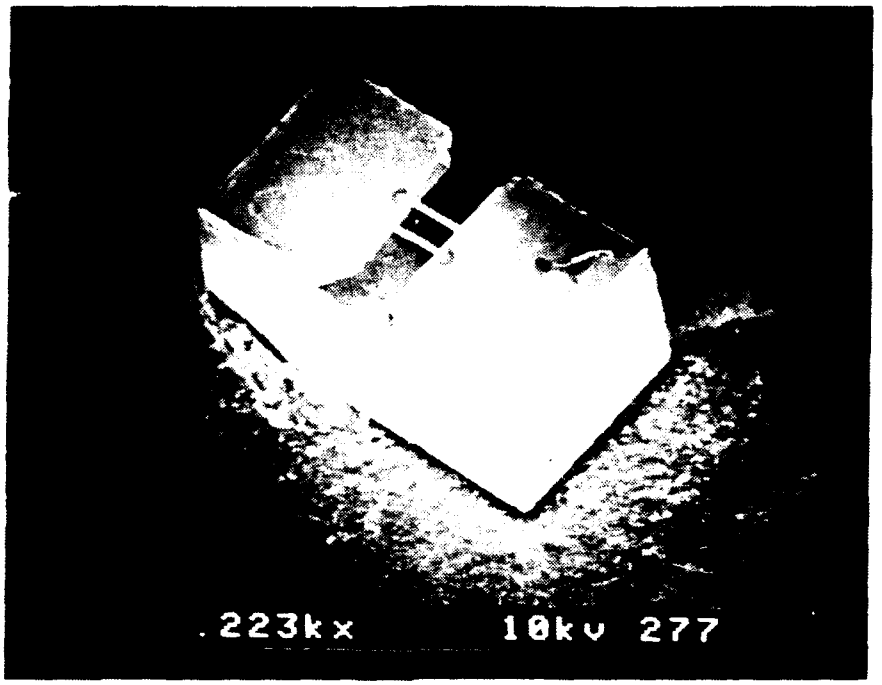


Figure 8.1 SEM Photograph of a Diode Pair with a Quartz Substrate

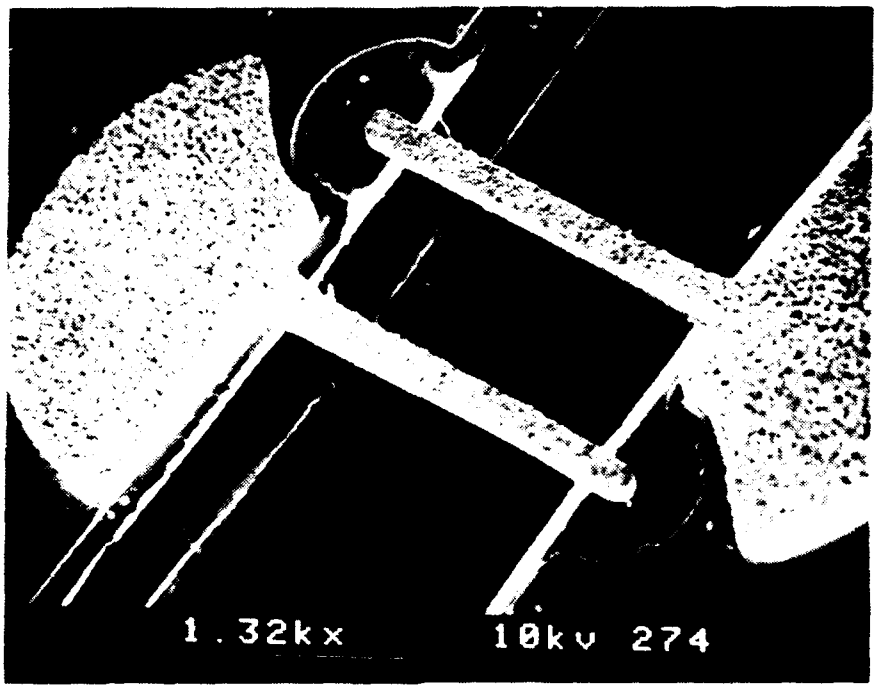


Figure 8.2 The Surface Channel of the Quartz Substrate Diode

capacitance C_{pp} has been eliminated effectively, and the planar diode now has parasitic reactances similar to those of a whiskered diode.

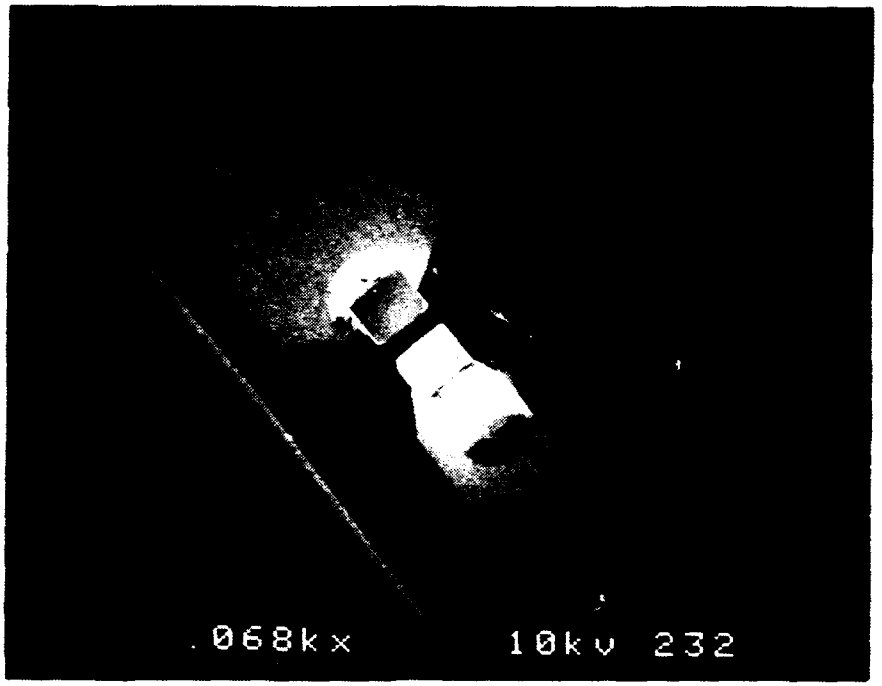


Figure 8.3 SEM Photograph of a Substrateless Diode Pair Soldered to a Stripline

The electrical characteristics of the diode pair with quartz substrate (batch SR2T1) are presented in Table 8.3. These anodes were 1.2 μm in diameter.

Table 8.3 Electrical Characteristics of Quartz Substrate Diode Pairs	
V_{knee} (1 μA)	711 mV
ΔV	72.0 mV
R_S	6.3 Ω
V_{br}	-4.1 V
C_{TOTAL}	9-9.5 fF
C_{pads}	3.5 fF
C_{jo}	2.8-3 fF

Notice that the pad-to-pad capacitance is significantly less than the 10 fF observed for chips with GaAs substrates and the same pad geometries. The performance of these diodes in the University of Michigan's quasi-optical millimeter wave mixer was discussed in the previous chapter.

Bishop observed unusually low series resistance in his first set of quartz diodes. This low resistance was only observed after the GaAs substrate was removed, and is believed to be caused by excess heat in the diode, which yields an anomalously low R_S measurement [77]. Essentially, the removal of the GaAs substrate has eliminated an important heat sink. This change in measured series resistance was not observed in the batch of diode pairs. Thus, the results given in Table 8.3 demonstrate that not all quartz substrate diode chips will have this increased heating effect. A possible explanation for this lies in the comparison of the anode diameter to buffer layer thickness ratio. In

Bishop's chips the ratio was 2.5:3, so that removal of the substrate clearly changes the thermal conductivity in the vicinity of the anode. Whereas in the dual diode chip presented here, the ratio was 1.2:5. In this case the heat generated in the junction area has a much better chance to spread before encountering the GaAs/adhesive/quartz interface. Thus, the chip behaves much more like a standard chip, without any noticeable excess heating. Although further study is required, it is evident that maintaining a small anode diameter to buffer layer thickness ratio should minimize the excess heating effect. Further efforts, such as the placement of a metal heat sink below the buffer layer may yield additional benefits.

8.2.4 Quartz Substrate Chips with Integrated Heat Sink

The quartz substrate technology allows processing of the backside of the membrane before attaching the substrate. One application suggested by Bishop was to plate a metal heat sink under the anodes. A technique has been developed to electroplate platinum and gold onto the membrane to serve as this heat sink.

The GaAs membrane was found to be strong enough to allow direct, but gentle contact by the plating fixture probe. Then the black wax sealing the probe tip is allowed to dry. The wafer was immersed in a Sel-Rex platinum solution and electroplated with a direct current of 20 mA for two minutes. Then Autronex-N [76] gold was electroplated at 20 mA for four minutes. (Initially, ohmic metals (SnNi/Ni/Au) were tried, but they did not adhere well to the GaAs.)

This work indicated that a metallic layer can be electroplated onto the back side of a membrane device, demonstrating that simple backside processing is possible. However, the usefulness of such a heat sink remains to be demonstrated.

8.2.5 Non-Alloyed Ohmic Contacts

There are many benefits to the use of non-alloyed ohmic contacts. They are easier to fabricate, and the elimination of a heating step from the process is easier on the GaAs. Also the use of a non-alloyed technology would allow the anodes to be anodically thinned and plated before the ohmic contacts are formed. Furthermore, the specific contact resistance of the non-alloyed contacts can be much lower than that of the SnNi/Ni/Au technology currently used [91]. This would allow smaller ohmic contact pads to be used, reducing pad-to-pad capacitance and chip size.

Two batches of diodes with non-alloyed ohmic contacts were attempted. Both used a delta-doped ohmic contact technology. The wafer was grown on SDL's organo-metallic chemical vapor deposition system, and its structure is shown in Figure 8.4. It is similar to the standard wafer except for the addition of a 500 Å transition layer and 500 Å of alternatively low/high Si doped GaAs on top. Although the wafer contained a number of crystal defects, it was believed to be good enough to demonstrate the fabrication process, and determine if the delta-doped layers could yield a low resistance ohmic contact.

The diode fabrication process must be altered because the ohmic contacts are now placed on the top layer of GaAs and the anodes on a buried layer. Therefore, the delta doped and transition layers must be removed from the anode regions in a controlled manner before the SiO_2 is deposited, as shown in Figure 8.5. Anodic etching was used for this task since it is our best controlled GaAs etching technique. To do this the ohmic contact mask was used in a negative, image reversed photolithography step to protect the ohmic contact regions from the etch. AZ 5214E photoresist was applied at 4000 rpm and

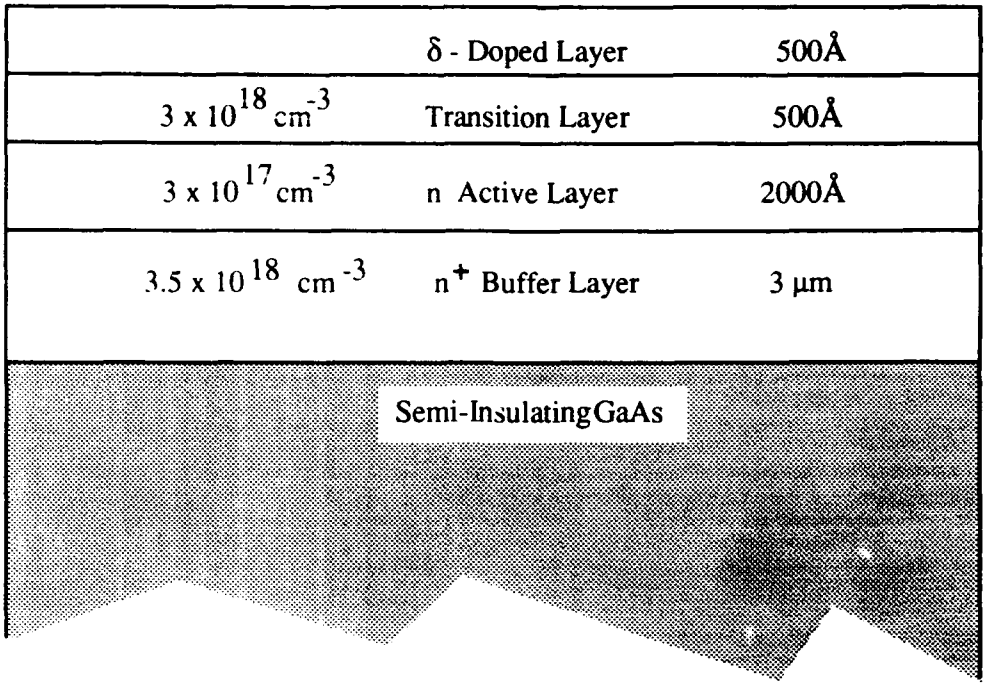


Figure 8.4 The Delta Doped Crystal Structure

exposed for 10 seconds at 10 mW/cm^2. Then, after a two minute pause, it was post baked on a hotplate at 120°C for 45 seconds. A five minute pause came next, and then a 1.5 second flood exposure. Finally, the resist was developed in AZ440 MIF for 65 seconds. Then a total of 1400 Å of GaAs was removed from the unprotected regions in two anodic thinnings.

After the SiO_2 film was deposited, the ohmic mask was used in a positive process to allow the ohmic metal to be plated. First the overlying SiO_2 was removed to expose the GaAs as shown in Figure 8.6. Then Autronex-N gold was electroplated in three steps. The wafer was etched in BOE for 10 seconds, immersed in deionized water and immediately placed into the gold plating solution. First, capacitive pulse plating (0.5 μF)

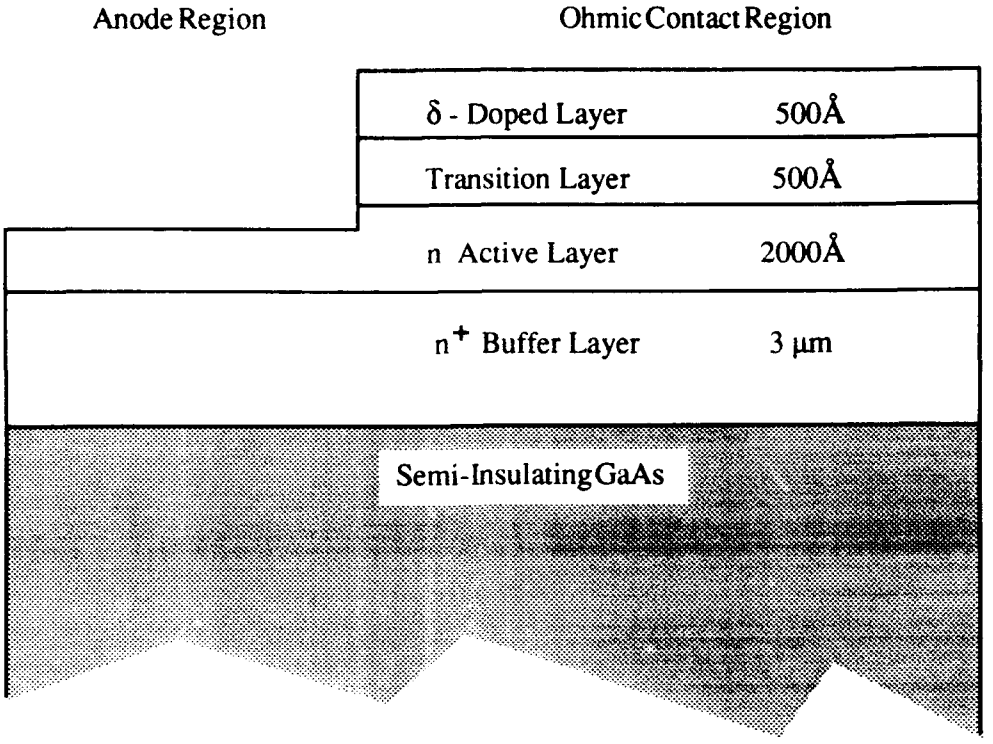


Figure 8.5 Opening the Epi Layer for Anode Formation in Later Steps

was used for 200 pulses. Next, the gold was DC plated at 0.5 mA for 2 minutes. Finally, 3000 pulses at 10 μF were used to avoid forming an edge bead.

Unfortunately, the contacts were non-ohmic, behaving like soft diodes. Bhaumik studied this technology independently [92] and concluded that the delta doped contacts were sensitive to pre-plating processing and are unreliable. He did find however, that the InGaAs technology could yield specific contact resistances as low as 2×10^{-6} Ωcm^2. The fabrication sequence developed in this dissertation should also work for InGaAs wafers as well. InGaAs technology was not explored because no suitable material was readily available, and development of an InGaAs material system to yield a reliable ohmic contact was beyond the scope of this project. However, the goal of demonstrating the

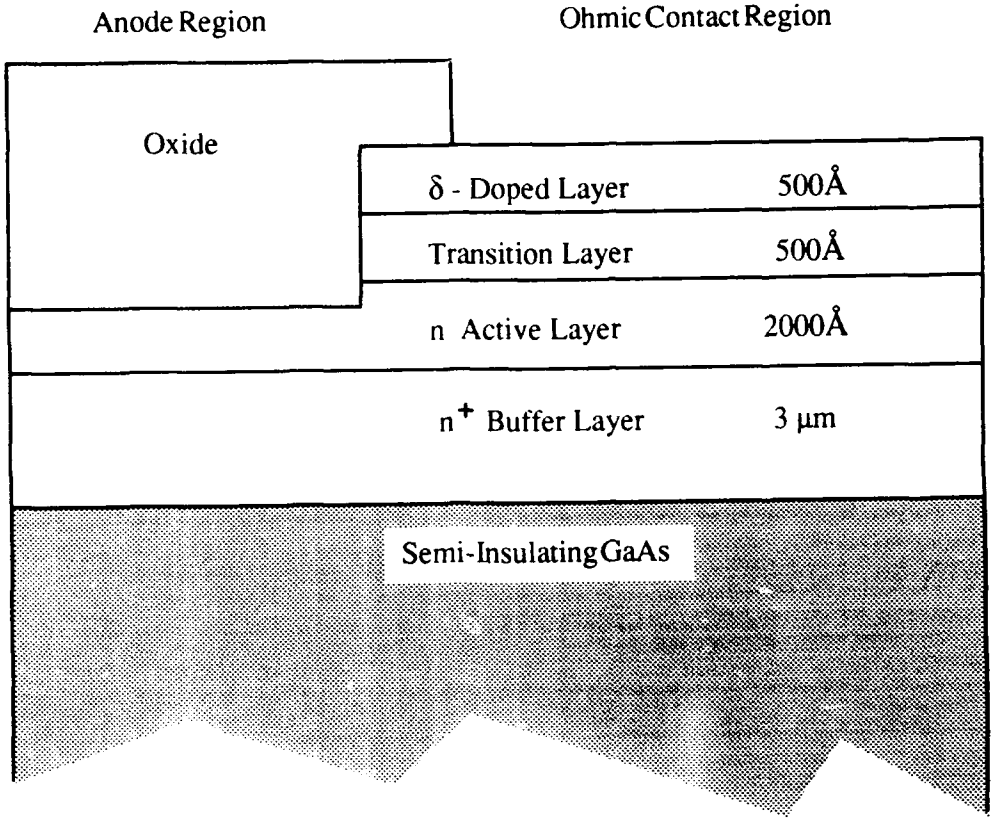


Figure 8.6 Opening the Oxide for Deposition of Ohmic Contact Metals

fabrication process has been met, and only the availability of suitable materials is required for further investigations.

8.2.6 A Monolithic Chip with Individually Biased Diodes

In the standard diode configuration, shown in Figure 8.7, it is not possible to DC bias the diodes. Because of this the LO voltage must be large to ensure that both diodes are turned-on, as shown in Figure 8.8a. The required LO power can be significantly reduced however, if each diode is individually biased. Then, as shown in Figure 8.8b only a small LO voltage is required. Individual biasing also allows partial correction of

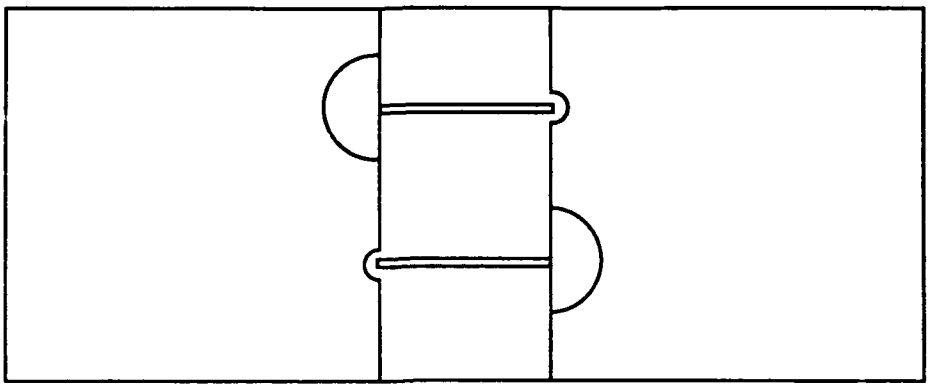


Figure 8.7 The Two Pad, Unbiasable Diode Pair

diode mismatches, a useful characteristic at submillimeter wavelengths. One possible configuration consists of splitting one ohmic pad into two as shown in Figure 8.9.

A three pad design was considered but not included in the mask set since the immediate fabrication goal was to develop diodes for Aerojet's 183 GHz mixer. This design was incompatible with their mixer, and other existing stripline designs.

8.3 Scale Model Studies

Maxwell's field equations can be written in a dimensionless form allowing the electrical characteristics of a model to be scaled to other dimensions and frequencies. This is useful because it allows the characterization of submillimeter wavelength devices using scale models and centimeter wavelength equipment.

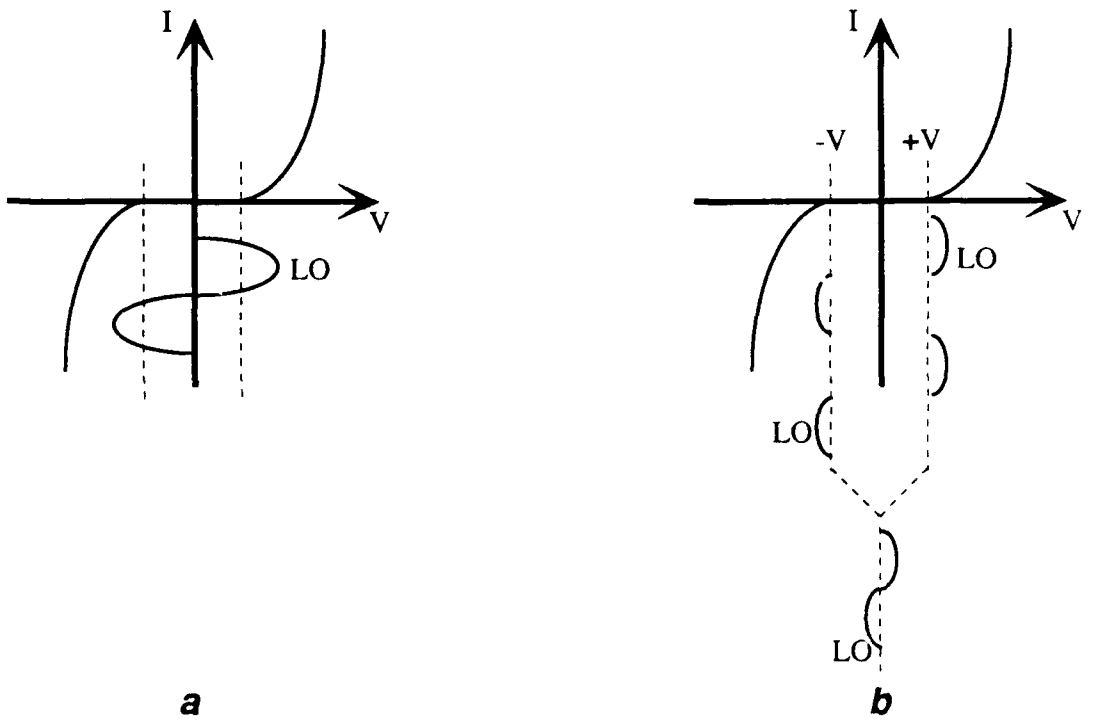


Figure 8.8 A Comparison of LO Requirements for Unbiased (a) and Biased (b) Diodes

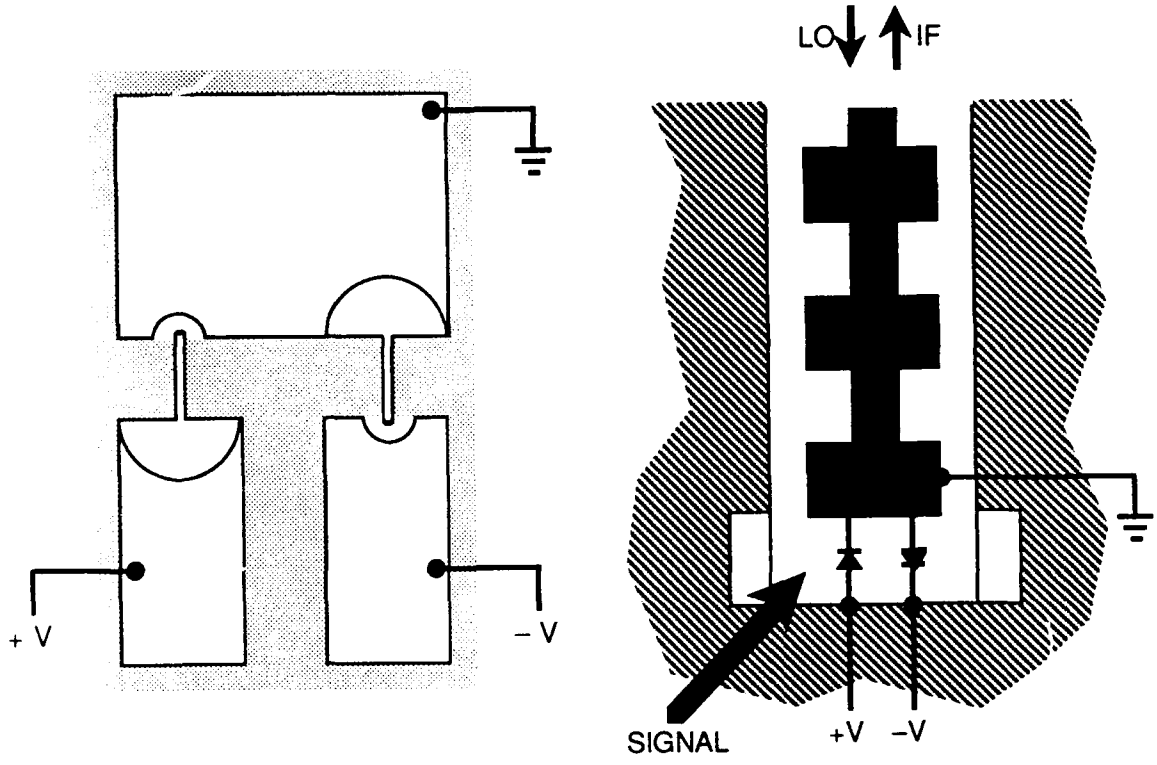


Figure 8.9 A Three Pad Design that Allows Individually Biasing

Two devices are electrodynamically similar if the following conditions are met [93]:

$$\mu_1 \varepsilon_1 \left[\frac{l_1}{t_1}\right]^2 = \mu_2 \varepsilon_2 \left[\frac{l_2}{t_2}\right]^2 \tag{8.1}$$

$$\mu_1 \sigma_1 \frac{l_1^2}{t_1} = \mu_2 \sigma_2 \frac{l_2^2}{t_2} \tag{8.2}$$

The parameters l_1 and l_2 are lengths that characterize the objects' geometry. The period of the fields are represented by t_1 and t_2. The first condition (8.1) implies that if $\mu_1 = \mu_2$ and $\varepsilon_1 = \varepsilon_2$, then the device geometry, and therefore reactances, can be scaled inversely with frequency. This means that if the lengths are scaled by a factor of fifty, then

frequency is scaled by a factor of one fiftieth. Subsequently, the second condition (8.2) demands that the conductivities scale by one fiftieth as well. This presents a problem since it is difficult to find materials with suitable conductivities. However, this is only a problem if lossy materials are considered. In our case, the second condition is ignored because the models are used only to study the lossless elements of the diode.

Two model studies were conducted to examine the parasitic reactances associated with device geometry. The first study examined the effect of the surface channel depth on the pad-to-pad capacitance C_{pp}. It showed that C_{pp} is significantly smaller for deeper channels. A second model study was undertaken to gain insight into the self and mutual inductances of the anode contact finger. This model also measured the pad-to-pad capacitance observed within a waveguide. Furthermore, it measured the inductance associated with the anode contact finger. Unfortunately, the chip inductances were more complicated than anticipated. Thus, although this study greatly increased our understanding of the inductance of the chip, we were unable to make an accurate measurement of the mutual inductance of the anode contact fingers.

8.3.1 Capacitance Model of the Surface Channel

The effect of surface channel depth on C_{pp} was investigated by fabricating one batch of diodes (SD2T2) with a ten micron deep channel instead of the usual six microns. This lowered C_{pp} from 10 fF to 7.5 fF. To study this effect further, a simple model of a generic planar diode was constructed using four inch square by 3/8 inch thick blocks of $\varepsilon_r \approx 13$ material (barium titanate). The capacitance was measured by an HP-4275 LCR meter using a one volt, 10 kHz signal. The results shown in Figure 8.10 support the observed reduction of pad-to-pad capacitance with increased surface channel depth. This

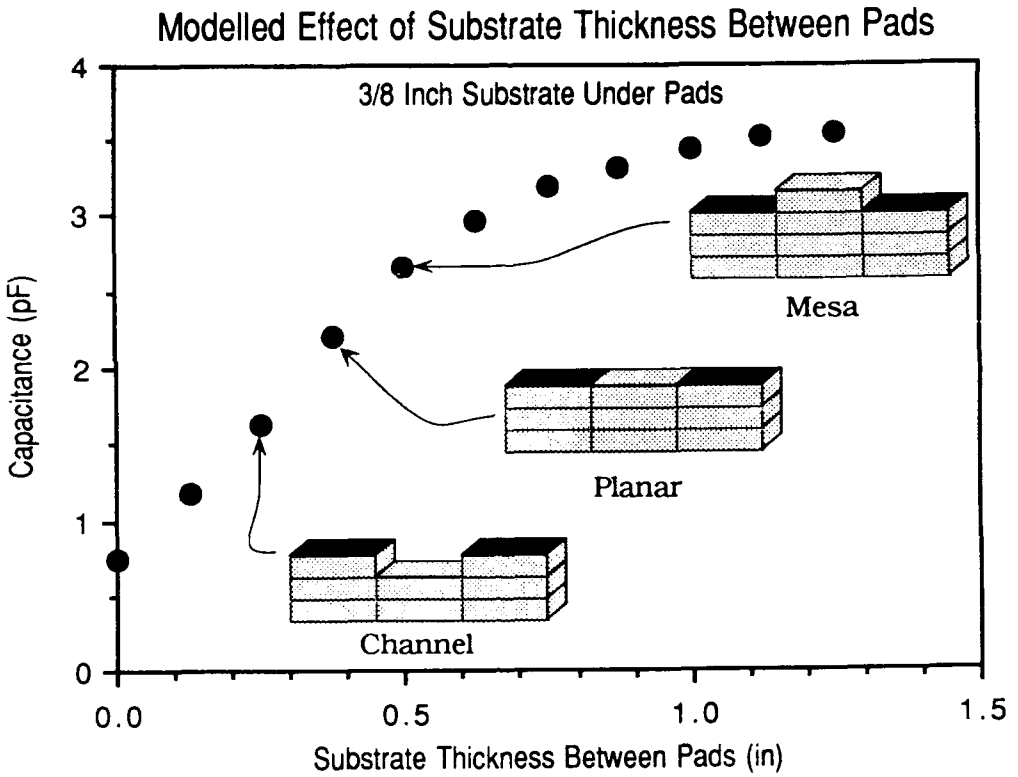


Figure 8.10 Surface Channel Modeling Results

model also implies that a surface channel configuration yields lower parasitic capacitances than the mesa structure shown.

The surface channel cuts the conductive path between the pads, creating a fringing capacitance that lowers the total pad-to-pad capacitance. Past designs used the surface channel to control the magnitude of this capacitance by the channel width alone, but this capacitance can also be controlled by the depth of the surface channel. A deeper channel may allow the use of shorter, lower inductance fingers without increasing the pad-to-pad capacitance significantly. Future designs should therefore allow for deeper surface channels by placing the channel edge several microns farther away from the anode than

in the current mask set.

8.3.2 Inductance Model of the Anode Contact Fingers

The performance of a multi-diode mixer is degraded at signal frequencies near the resonance between the diode finger's inductance and its junction capacitance. Kerr [38] showed that at these frequencies each diode of an anti-parallel pair conducts twice in one LO cycle. Then the signal power is converted to an IF current that circulates within the diode loop, and not in the external circuit. Hicks and Khan [94] repeated this analysis for non-symmetrical diodes and found that performance is degraded when one of the two diodes conducts twice per LO cycle. Neither of these investigations considered the mutual inductive coupling of the diodes. However, they do emphasize that a mixer designer must know the values of the inductances present in the diode in order to avoid certain circumstances where resonances can lead to poor mixer performance.

A 61× scale model was built to gain some knowledge of these inductances. It should be emphasized that these results are only directly valid for the waveguide modeled since the inductances depend on the dimensions of the stripline and its enclosure, although general conclusions may also be accurate for other structures.

Thirty models were constructed to de-embed the desired reactances from the measurement circuit for the twelve finger geometries in the mask set. The full two port S parameter response of each model was measured (1 to 3 GHz) with an HP8753A network analyzer, and recorded in a computer file. Then the software package TOUCHSTONE was used to match a circuit model to these data through an optimization routine.

The physical model consisted of a suspended microstrip line and scale models of the diode chip. It is sketched in Figure 8.11. The stycast substrate had a dielectric constant

of 3.75, similar to that of quartz. The microstrip was suspended in an enclosure with a narrow air channel underneath. A finite difference program [95] was used to calculate an effective impedance of 66.6 Ω and an effective dielectric constant of 1.85 for this model at DC. The width of the stripline was chosen to match the width of the chip to eliminate unnecessary inductances.

The suspended stripline and coaxial to stripline connectors were characterized by the circuit shown in Figure 8.12. The electrical model used the microstrip dispersion relation of Pramanick and Bhartia [96]:

$$\varepsilon_{e(f)} = \varepsilon_r - \frac{\varepsilon_r - \varepsilon_{eff}}{1 + (f/f_T)^2} . \tag{8.3}$$

Then the impedance of the line was calculated as:

$$Z_{(f)} = \frac{\eta_0 h}{W_e(f)\sqrt{\varepsilon_e(f)}} \tag{8.4}$$

where

$$W_e(f) = W + \frac{W_{eff} - W}{1 + (f/f_T)^2} \tag{8.5}$$

and

$$\eta_0 = 120\pi$$

h = substrate thickness.

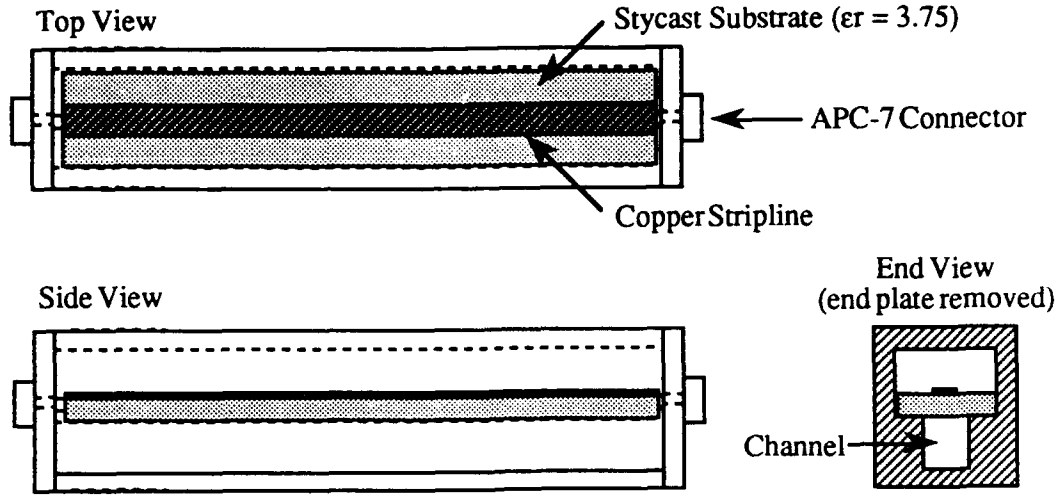


Figure 8.11 Sketch of the Suspended Stripline Model

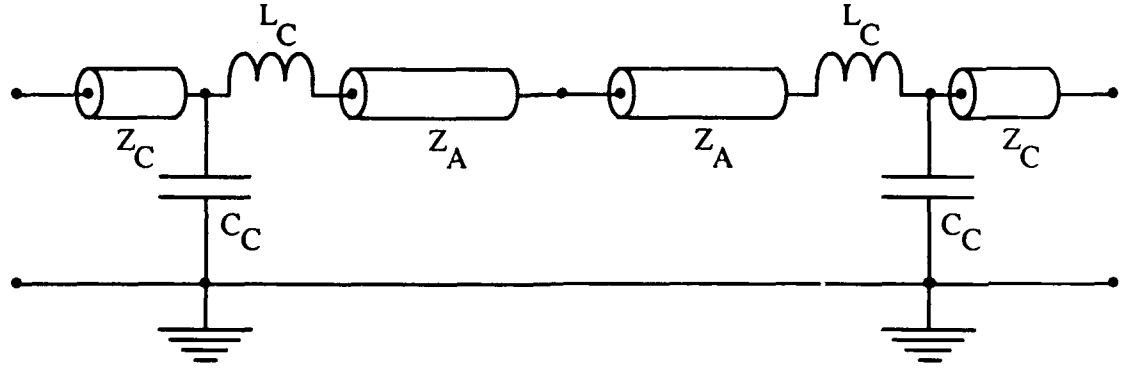


Figure 8.12 Electrical Model of the Stripline and Connectors

The physical width of the line is W and W_{eff} is the equivalent width at DC. This equivalent width accounts for fringing field effects at the edge of the strip, and is therefore a function of frequency. This relationship was found to provide a better fit to

the measured response while providing sensible values for other known parameters (Schneider's dispersion relation [97] was used first and found to fit the data nicely, but at the expense of nonsensible values for some known parameters). Atwater surveyed several known dispersion relations and concluded that (8.3) differs from a variety of measured data by less than 2.5% [98]. All parameters were constrained to vary to within known uncertainties. The values of the parameters yielding the best fit, and their known values are listed in Table 8.4. The match between the electrical and physical models is shown in Figures 8.13 and 8.14.

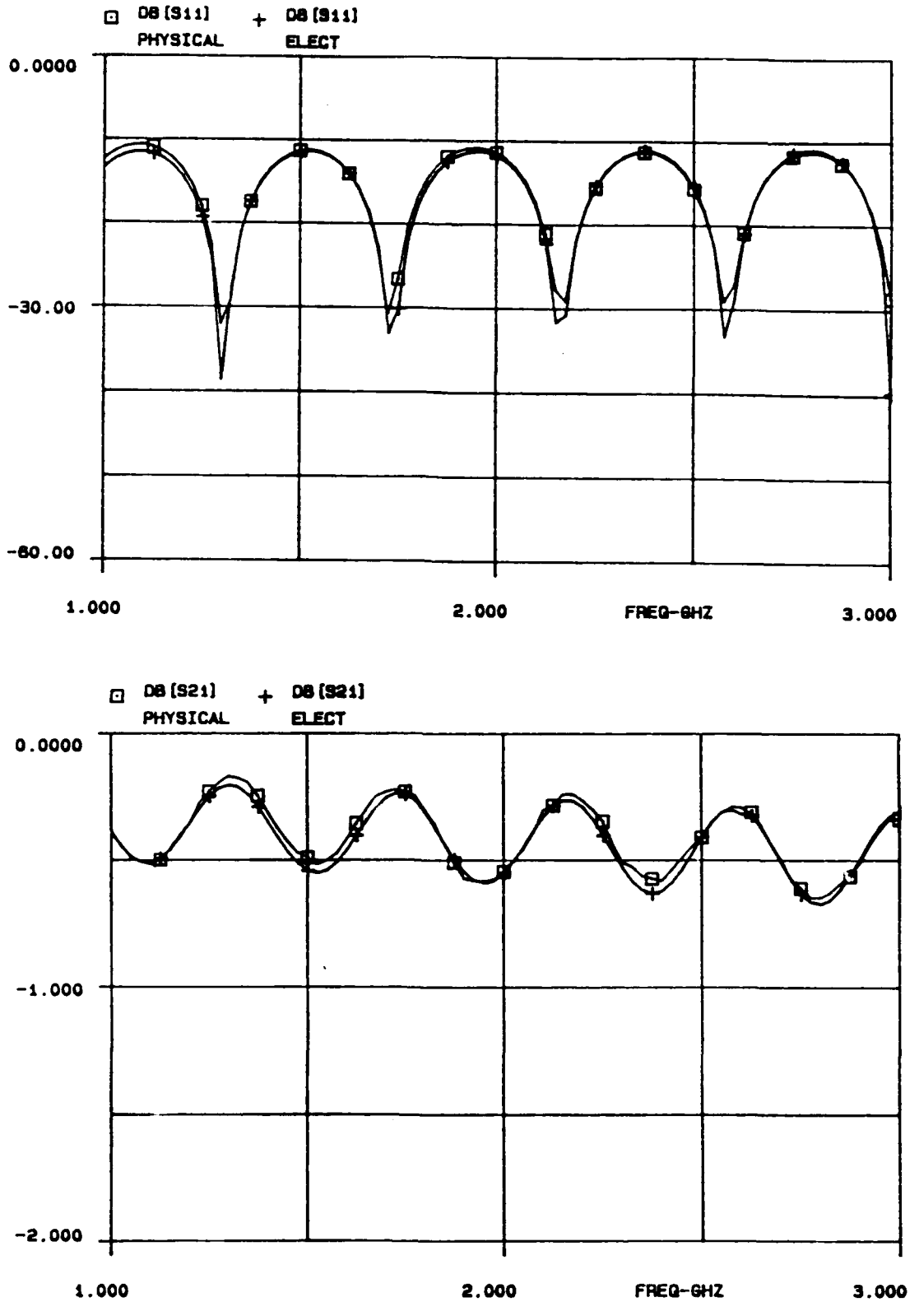


Figure 8.13 Magnitude S_{11} and S_{21} of the Stripline Model

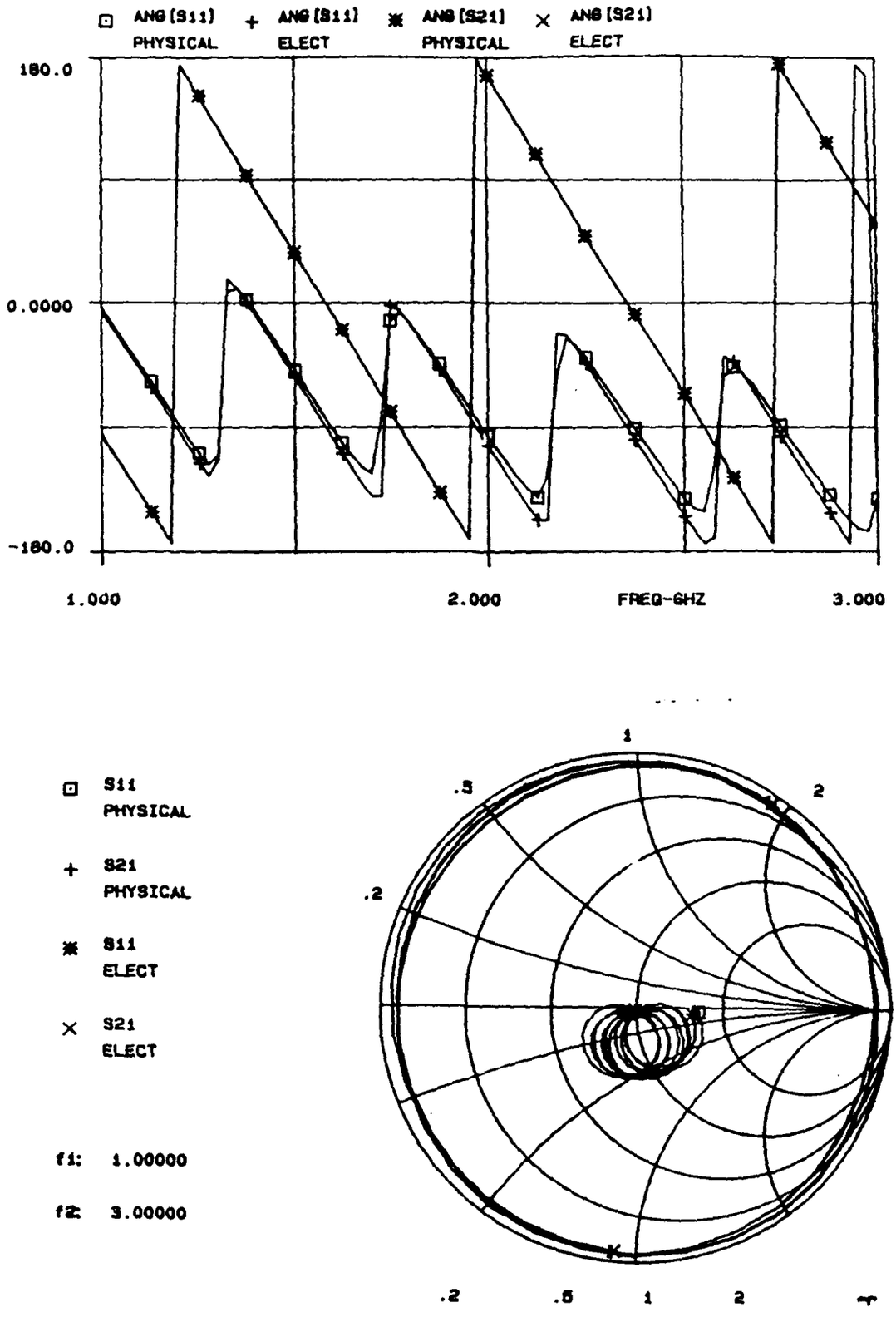


Figure 8.14 Angle S_{11} and S_{21} and Smith Chart for the Stripline Model

Table 8.4
Stripline and Connector Parameters of the Circuit Model

Parameter	Observed Value	Known Value
ε_r	3.71	3.75
Z_c	50.9Ω	---
$length_c$	1.6 cm	1.6 ± 0.1 cm
ε_c	1.03	---
α_c	0.012 dB/cm	---
C_c	121.5 fF	---
L_c	347.8 pH	---
h	0.408 cm	0.406 ± 0.002 cm
w	0.637 cm	0.635 ± 0.002 cm
Z_o	67.0 Ω	66.6 Ω
v/c	0.735	0.735
$length_A$	12.6 cm	12.5 ± 0.1 cm
α_A	0.008 dB/cm	---
f_T	16.1 GHz	---
w_o	1.68 cm	---

The capacitance of the gap between the two pads was investigated next. A large gap was first cut in the microstrip conductor. Then a scale model of the GaAs chip was bonded across the gap. This model consists of two copper pads on an $\varepsilon_r \approx 12$ block of stycast scaled to represent a chip 9.5×4.1×1.8 mils with no fingers connecting the pads.

The diode model was mounted in a "flip chip" configuration using conductive silver paint. The gap discontinuity was represented as a capacitive Π network as shown in Figure 8.15. Results are shown in Figure 8.16. The lower data points are gap capacitances of a substrateless model.

The solid line represents the theory for a microstrip gap modified for the flip chip configuration. This capacitance relation is applicable to a stripline with a material such as quartz $\varepsilon_{r1} = 3.75$ under the line, and air ($\varepsilon_{r2} = 1$) above [99]. However, in our model the GaAs replaces the air above the gap. Only the substrate's dielectric constant ε_{r1} is used in this calculation. Therefore, its value was changed to $\varepsilon_{r1} = 14.75$ to calculate the data presented as a solid line in Figure 8.16. This value was chosen because it yields the same average ε_r that is present in the actual model. The good agreement with the observed

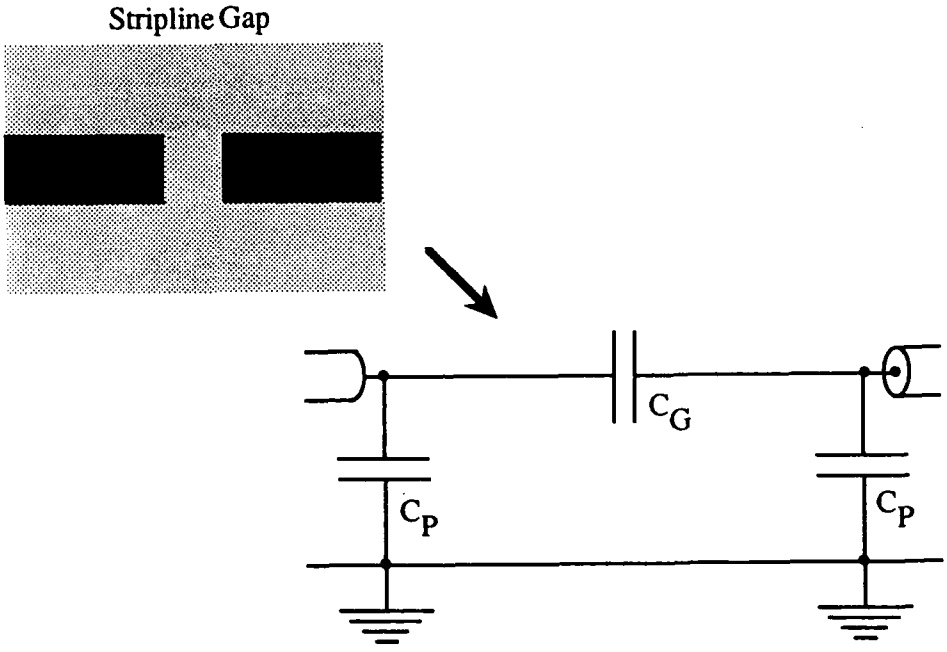


Figure 8.15 Equivalent Circuit of the Stripline Gap Model

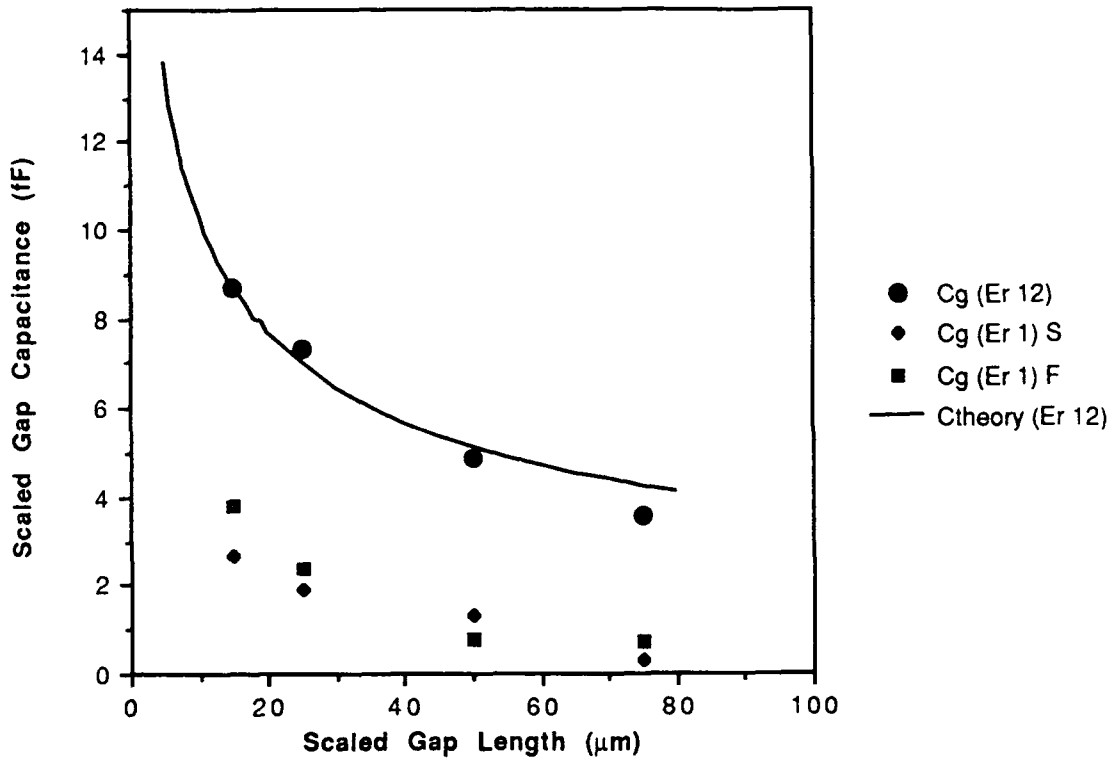


Figure 8.16 C_{pp}: With (Er 12) and Without (Er 1) an $\varepsilon_r = 12$ Substrate

capacitances indicates that this modification is appropriate.

The inductance of a single finger was modeled by using a chip model containing one finger 7.8 mils wide and 1.5 mils thick after each capacitance measurement. This model, which was cut out of a solid strip of copper tape on the $\varepsilon_r = 12$ block, scales to a finger 3.3 μm wide and 0.6 μm thick. Since the finger length was less than 0.05 λ_g it was modeled as a single inductor, L_g and two shunt capacitances, C_L forming a Π as shown in Figure 8.17 [99]. The values of C_p and C_g, which were previously determined, were not allowed to vary.

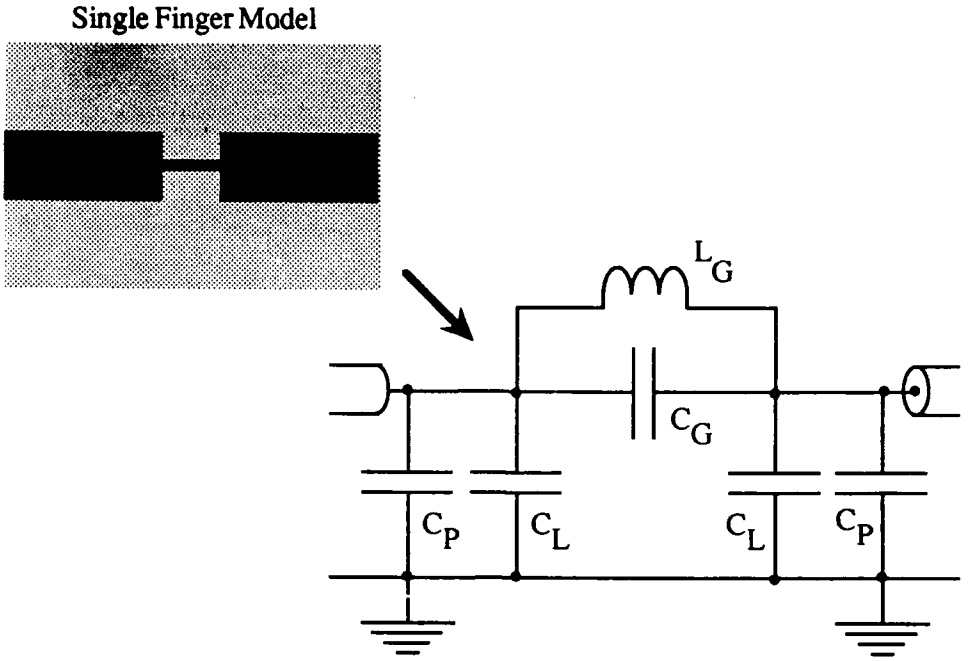


Figure 8.17 Equivalent Circuit: Single Finger Model

Figure 8.18 presents the observed single finger inductances. The scaled data fit a line of slope 0.63 ± 0.01 pH/μm with an intercept of 15.1 ± 0.6 pH. The slope is attributed to the self inductance per length of the finger and fits an equation of the form:

$$\frac{L}{l} = \frac{\mu_o}{2\pi} \ln\left[\frac{R}{w}\right] \tag{8.6}$$

which describes the inductance of a coaxial line when w is the radius of the center conductor, and R is the radius of the outer conductor. However, for our case R is the distance from the finger to closest wall of the enclosure and w is the finger width.

The intercept corresponds to the inductance of a zero-length finger. The fact that this intercept is non-zero means that another inductance is present. This inductance can be understood by considering the path of the electrons in the circuit. The largest currents

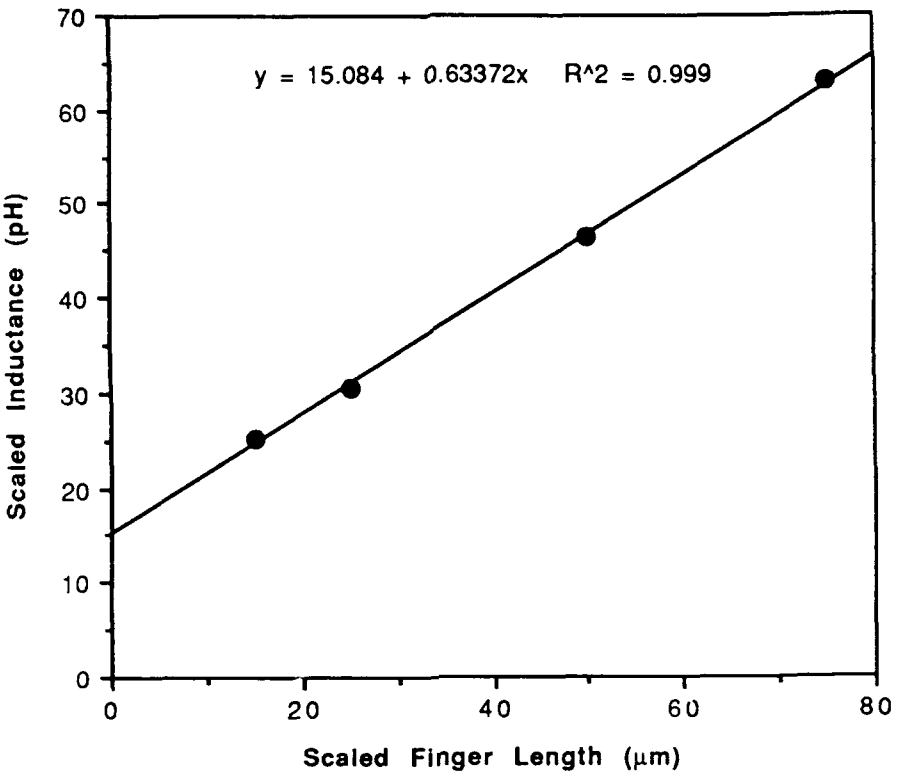


Figure 8.18 Observed Inductances of the Single Finger Models

flow along the edge of the line [100] until they approach the abrupt linewidth change associated with the finger. Then the current must change direction to flow through the finger as illustrated in Figure 8.19. This "fringing" inductance is associated with magnetic eddy currents caused by the abrupt the transition.

The dual finger chips were also modeled by the Π of L_g and C_L shown in Figure 8.17. The observed equivalent inductances L_g of the two finger models are presented in Figure 8.20. As expected, the inductances increased with decreasing finger spacing. This is expected for positive coupling through a positive value of the mutual inductance.

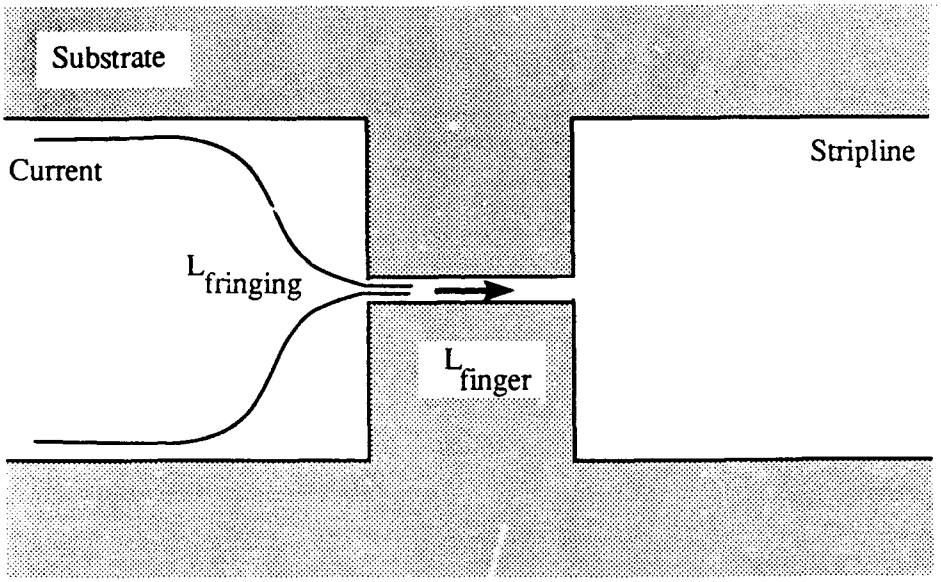


Figure 8.19 Fringing Inductance of Abrupt Change in Stripline Width

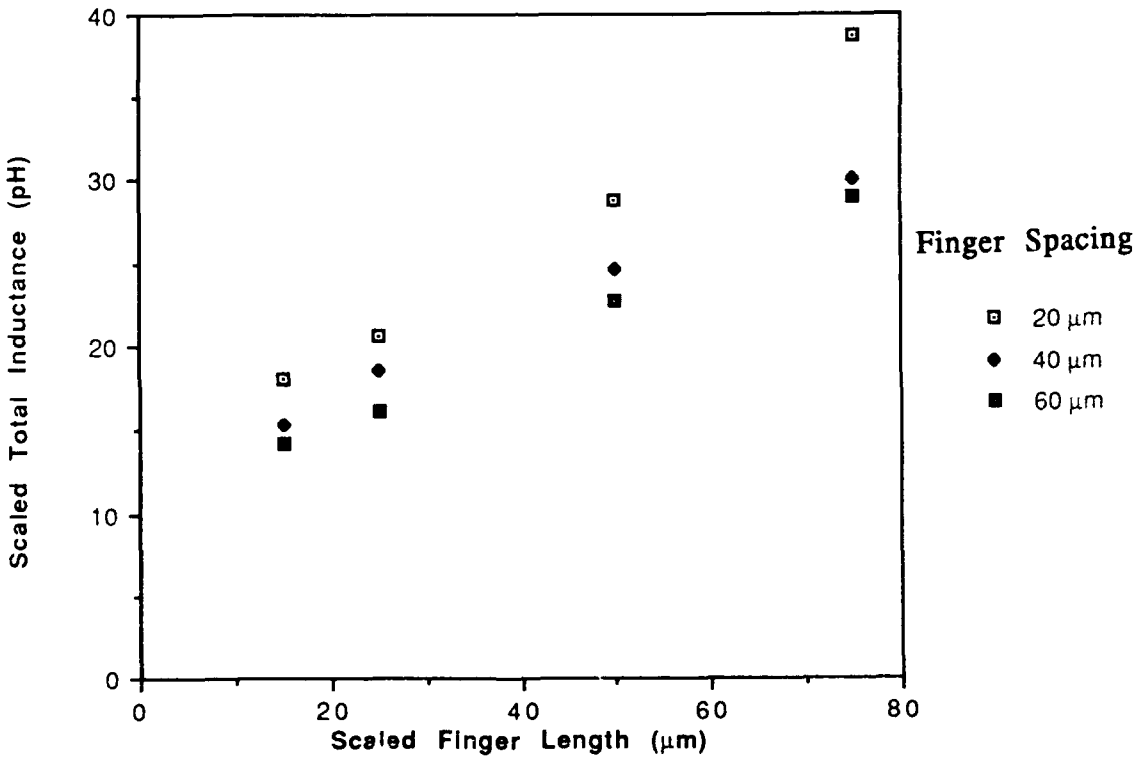


Figure 8.20 Observed Inductances of the 2-Finger Models

If the fringing inductance can be subtracted from the total inductance, then the mutual inductance of the parallel fingers can be calculated by solving:

$$L_{eq} = \frac{L_s^2 - M^2}{2(L-M)} \tag{8.7}$$

This was initially attempted without correcting for the fringing inductance, but the solution was not valid. Specifically, the observed data yielded some values for L_{eq} that were less than $\frac{L_s}{2}$, which is not possible. We later concluded that the fringing inductance was significant, and more importantly, changes significantly as the finger spacing is changed. This greatly complicates the study of the mutual inductance of the two fingers.

In reality equation (8.7) should be written as:

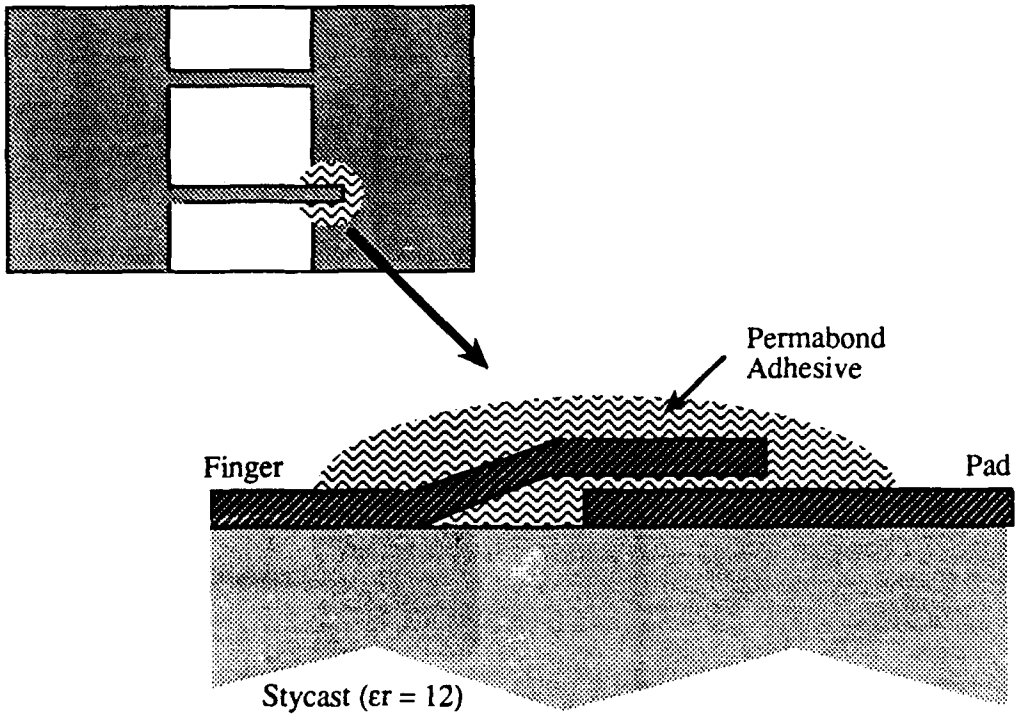
$$L_{eq} = \frac{L_s^2 - M^2}{2(L-M)} + L_{fringing} \tag{8.8}$$

where the fringing inductance is a strong function of finger geometry. For example, when two fingers are present the current has an easier time passing through the circuit. Therefore, the fringing inductance L_f is smaller than that observed for the single finger models. To further complicate the situation, the fringing inductance also depends on how close the fingers are to the strip edges, due to the non-uniform current distribution in the stripline.

Two additional model sets were studied in an attempt to understand this problem. First a new set of two finger models was made with fingers 75 μm long. In this set, one finger tip overlapped the stripline but was separated from it by a thin film (<1/2 mil) of Permabond 910 adhesive ($\varepsilon_r \approx 3$). This physical model and its electrical model are shown

in Figure 8.21 and 8.22. The two inductors in the electrical model were positively coupled by a mutual inductance that was allowed to vary as a fit parameter. This model is a good representation of an actual anti-parallel diode pair where one path is opened by the junction capacitance (reverse biased anode), and the other is shorted by the junction conductance (forward biased anode).

After the response of these capacitive models was recorded, the opened finger was removed and the model retested. This second model was fit to the Π circuit shown previously in Figure 8.17. The results shown in Figure 8.23 show that the single finger inductance does increase as the finger is displaced from the center. Since neither the finger's length nor its separation from the ground plane have changed, this increase must be due to changes in the fringing inductance. The capacitance C_F that best fit the data



Finger 8.21 A Better Anti-parallel Diode Pair Model

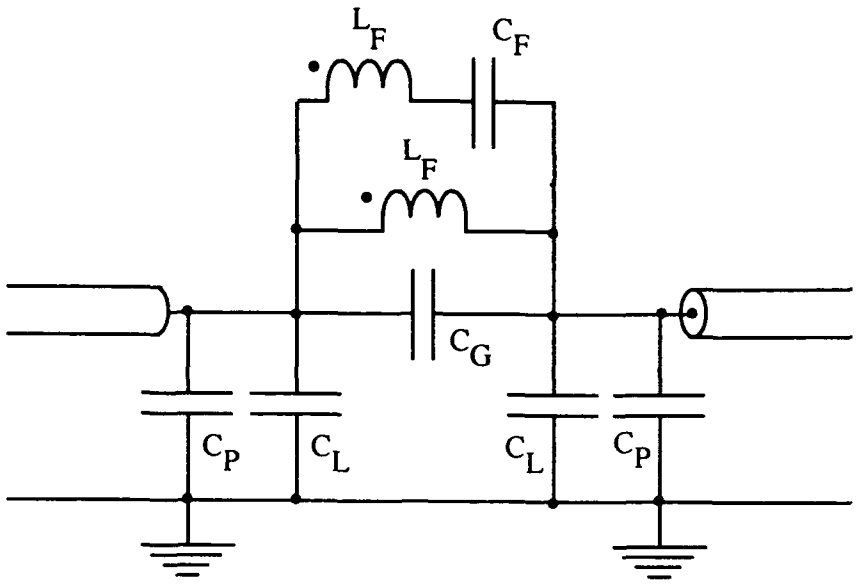


Figure 8.22 Equivalent Circuit: Diode Pair Model

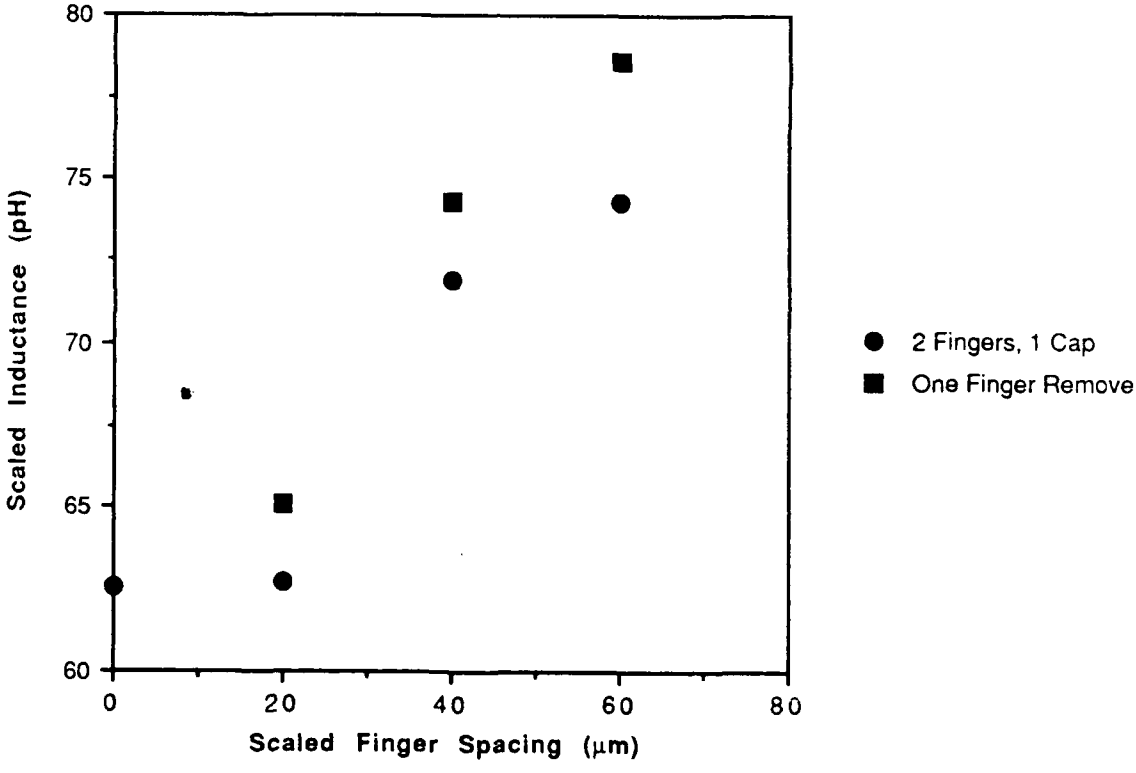


Figure 8.23 Single Finger Inductance: Offset from Stripline Center

agrees with the capacitance calculated for a parallel plate capacitor using the physical dimensions of the model. The mutual inductances observed were 28.3, 12.7 and 0.7 pH for the 20, 40 and 60 μm spacings of the 75 μm long fingers.

The goal of this waveguide model study was to measure the magnitude of the self and mutual inductances associated with the two contact fingers. The approach was to measure the inductance of a single finger model, and the equivalent inductance of a parallel combination of two such fingers; then to use these values to calculate the mutual inductance using equation 8.8. However, this approach was too simple for this problem, because it was found that the fringing inductance, which is associated with the constriction of the stripline currents by the finger(s), changes significantly when two fingers are present. It also varies significantly when the distance between the fingers is changed. This model did not allow these effects to be determined separately.

In spite of this we were still able to draw several conclusions. We found that the theory used to describe the capacitance of a microstrip gap can be modified to yield a useful approximation of the pad-to-pad capacitance associated with the flip chip configuration. Also, the inductance per unit length of the anode contact finger, in a waveguide, can be reasonably calculated using equation 8.6. Additionally, the fringing inductance causes the total inductance of the finger to increase if the finger is not centered on the gap. However, the fringing inductance will decrease when two fingers are present, and this inductance is reduced significantly as each finger approaches the edge of the stripline.

Further work is required to analyze the inductances associated with the two contact fingers. Perhaps a good starting point is to repeat the last modeling effort, which placed a

capacitance at the end of one finger, for different finger lengths. This effort would be easier if a larger scale (eg. > 100×) were used. Also, chip capacitors should be used instead of the capacitance obtained by above approach. Furthermore, the scope of the effort should be expanded to investigate the effects of strip width, substrate thickness, and the proximity of the enclosure walls on the single finger inductance on both microstrip and suspended striplines. The results of this effort would also be more precise if photolithographic techniques were used to fabricate the models. Since the models will be fairly large, the required masks could be manufactured cheaply.

8.4 Comments on a 600 GHz Design

Although the inductance scale model work was not sufficiently complete to optimize the chip's design for 200 GHz, the actual performance of the diode pair shows that we have a good design. Therefore, without complete knowledge of the parasitic inductances, a good starting point is to scale our successful 200 GHz design to 600 GHz. As is discussed below, the fabrication processes required to realize this 600 GHz design have largely been developed in the course of this dissertation.

The 600 GHz chip will require 0.9 μm diameter anodes. This is certainly achievable with dry etching techniques, and fabrication of submicron anode holes has already been demonstrated with two batches of anti-parallel diodes. Further reduction of anode diameters, which may yield improved performance, will require the fabrication of a new mask set.

The scaled ohmic contact pads are 1.3×1.3 mils in size. These pads will contribute two to four ohms to the series resistance if fabricated with the SnNi/Ni/Au technology. This additional resistance is tolerable, but not desired. Therefore, a new ohmic contact

technology, with a specific contact resistance of 10^{-6} Ωcm^2, should be investigated to minimize this resistance. It is anticipated that an InGaAs technology capable of meeting this requirement will soon be available in the SDL.

For 600 GHz, our design scales the anode contact fingers to a 15 μm length, spaced 7 μm apart. This finger length is compatible with the surface channel etch. However, the finger spacing is not. The anode resides at the center of a 10 μm arc that defines the edge of the ohmic contact. The radius of this arc can be reduced to no less than 8 μm, because smaller radii would not leave sufficient room for misalignment of the different photolithographic mask levels. Therefore it is suggested that this ohmic contact arc around the anode be placed 8 μm from the anode center, and that the fingers be separated by 10 μm (center to center).

A crystal structure similar to that used in this research is appropriate for 600 GHz; however, the doping of the active epitaxial layer should be increased to $4\times10^{17}cm^{-3}$ and be only 700 Å thick. This doping level ensures that the operating frequency is a factor of 10 from the plasma resonance frequency of 6 THz [45]. Also, a $4.5\times10^{18}cm^{-3}$ buffer layer can be 3 μm thick since the skin depth is 2 μm at 600 GHz. This will make the shorter anode contact fingers easier to achieve since the surface channel depth can be decreased.

The GaAs substrate thickness must be reduced from 25 μm to 8 μm. A chip this thin cannot be fabricated reliably without the use of an etch stop layer. Furthermore, it would be impossible to handle these chips because the surface channel must be at least 3 μm deep. This makes the substrate only 5 μm thick under the channel. Therefore, the quartz substrate technology of Bishop should be used at 600 GHz. Fortunately, the

anode diameter to buffer layer thickness ratio will be 0.5:3, so excess heating effects related to the quartz substrate are not anticipated. However, this remains to be demonstrated and the use of backside processing may be required to attach a metallic heat sink.

The feasibility of fabricating diodes using the above design has been demonstrated in this research. All required processes now exist, with the exception of an ohmic contact technology with a lower specific contact resistance. Further investigation of this design now awaits the development of this technology.

8.5 Summary

The chapter began with an investigation of alternative fabrication technologies that may be required to develop submillimeter wavelength devices. The use of dry etching to form anodes smaller than one micron was successfully demonstrated. A batch of diode pairs was made using Bishop's technique [89] to replace the high dielectric GaAs substrate with quartz. This batch demonstrated that the excess heating effects seen in the first batch of quartz substrate diodes can be avoided if the ratio of the anode diameter to buffer layer thickness is large. Backside processing of the buffer layer was also demonstrated, and a process to use non-alloyed ohmic contacts was developed.

Two modeling studies were discussed. An 800× scale model of a generic planar diode demonstrated that the pad-to-pad capacitance can be reduced significantly by etching the surface channel deeper. Then, a 61× scale waveguide model investigated the inductances associated with the two anode contact fingers. This model study measured the inductance of a single finger, but could not be used to determine the mutual inductance of two fingers. This was due to the unanticipated affect of the fringing

inductance associated with the constriction of current as it passes through the fingers. Specifically, this inductance was found to be significant and to vary as the chip geometry was changed. Thus, we were experimentally unable to isolate changes in finger inductance from changes in fringing inductance. However, much was learned, and a future study was proposed to investigate this effect.

This chapter concluded by presenting a design for an anti-parallel pair of planar diodes suitable for use at 600 GHz. All the fabrication processes required to use this design have been demonstrated, and fabrication of this device requires only the development of an improved ohmic contact technology.

CHAPTER 9

CONCLUSIONS AND FUTURE WORK

9.1 Overview

The University of Virginia's Semiconductor Device Laboratory has developed gallium arsenide Schottky barrier diodes that have exhibited record-low noise temperatures at millimeter and submillimeter wavelengths. Heterodyne receivers using these whisker contacted diodes have been flown successfully on aircraft; however, the use of the whisker is difficult to incorporate into receivers that will fly on satellites. The necessary step of contacting a whisker to the diode's anode is arduous, and time consuming. Furthermore, the contact may not withstand the high vibration environment of a space launch. For these reasons the development of a planar Surface Channel technology ideally suited for space systems was begun in the SDL. These planar diodes contain an integral anode contact finger that eliminates the use of the whisker. This finger maintains contact to the anode throughout severe thermal cycling, and in high vibrational environments. Additionally, these Surface Channel diodes have performed as well as the whisker contacted diodes at 100 GHz. The research presented in this dissertation is a natural extension of the Surface Channel technology, and will yield space qualified diodes for use at submillimeter wavelengths.

The performance of a space based heterodyne receiver is restrained by the limited local oscillator powers available. The high frequency LO sources used in ground and aircraft based receivers are unsuitable for space applications since they are bulky and demand too much power. Current research is striving to develop an LO source that is

small, light, and modest in power requirements. An alternative solution is to build receivers that can operate with the lower frequency LO sources that are available. One such receiver is the subharmonically pumped mixer. It requires an LO source that is at only half the signal frequency. Thus, a 600 GHz receiver can be driven by a 300 GHz source. This approach will be used in the proposed Microwave Limb Sounder on the Earth Observing System and the study of suitable diode technologies for this system is the subject of this research. A specific goal of this dissertation was to demonstrate this technology through the design, fabrication, and evaluation of a planar, anti-parallel pair of Schottky diodes for use in subharmonically pumped receivers of millimeter wavelength radiation.

The theory relevant to both the Schottky barrier diode and the subharmonically pumped mixer were presented in Chapter 2. A survey of planar diode technologies and the development of the SDL's Surface Channel diode were presented in Chapter 3. Chapter 4 discussed the design goals, and design of the diode pair which used the Surface Channel technology as its basis. Next, the general techniques used to fabricate semiconductor devices, and the fabrication sequence of the diode pair were presented in Chapter 5. The problems encountered during development of the diode pair technology and their solutions were discussed in Chapter 6. The electrical performance of the diode pair was presented in Chapter 7. This included the performance of the diode pair in a 183 GHz mixer at Aerojet-General Corporation, where the planar diode performance was found to be as good as that of whisker contacted diodes. The performance of the diode pair in four other receivers was also discussed.

Finally, Chapter 8 addressed several optimization issues important in making the diode pair useful at submillimeter wavelengths. These consisted of techniques to increase cutoff frequency by using dry etching to produce small anodes to reduce junction capacitance. Also, the pad-to-pad parasitic capacitance was significantly reduced by replacing the GaAs substrate with quartz. The quartz substrate can be removed after bonding to further reduce this capacitance. Additionally, the substrate replacement technique allows for the deposition of a metal heat sink under the anode. Also developed was a fabrication technology suitable for using non-alloyed ohmic contacts.

Chapter 8 also presented the results of two scale model studies which were conducted to study the parasitic reactances of the diode. A preliminary design of a 600 GHz diode pair and the required fabrication technology were reviewed.

9.2 Summary of Significant Achievements

The achievements realized in this research are presented in two parts below. These include contributions important to the Surface Channel diode technology, and achievements related to a submillimeter design which merit special attention.

The important contributions made to the Surface Channel technology include:

- Study of anode pulse plating parameters with W.L. Bishop which contributed to the development of a reliable anode technology for the Surface Channel diode.
- Participation in development of an improved Ohmic Contact technology, including verification of the suitability of Nistan plating solution and an additional hotplate hard bake to improve photoresist adhesion.
- Development of a post-photolithography O_2 plasma etch to remove photoresist debris left during development.

- Development of a technique to overplate ohmic contact pads with gold while avoiding creation of an edge bead.
- Modification of all photolithography bakes to use hotplates instead of ovens, reducing fabrication time and improving resist removal without degrading the performance of the photoresist.
- First demonstration of anodic thinning of planar diode anodes through the anode holes.
- Development of a fabrication technology suitable for use with non-alloyed ohmic contacts, when the required material becomes available.
- Discovery and experimental verification of significantly reduced parasitic pad-to-pad capacitance with deeper surface channels.

The achievements of special note, which are related to the development of a submillimeter design are:

- Design and development of a planar, anti-parallel diode pair fabrication technology which produced diodes with excellent, and very well matched electrical characteristics.
- Demonstration of mixing results comparable to, or better than those achieved with whisker contacted diodes in a 183 GHz subharmonically pumped mixer. This is the first use of planar diodes in a heterodyne receiver at frequencies significantly above 100 GHz with performance equal to that of whisker contacted devices. These diodes are currently being spaced qualified to fly on the Air Force's DMSP weather satellites, and on the Space Shuttle as part of a project to develop aero-braking techniques for manned spacecraft returning from Mars.
- Fabrication of diodes with quartz substrates [89], and demonstration of good

mixing results using these diodes in a quasi-optical subharmonically pumped receiver. It was also demonstrated that excess heating effects can be avoided by keeping the anode diameter small compared to the thickness of the buffer layer. This work included development of a technique for adding a heat sink to these quartz substrate devices, an important demonstration of back-side wafer processing.

- Scale model study of anode contact finger self inductance and pad-to-pad capacitance. This study demonstrated that the spacing of the fingers changes the fringing inductance associated with the abrupt transition from ohmic contact pad to finger. This fringing inductance has been shown to complicate the study of chip parasitics, and show the need for a much more detailed study.
- Development of anode hole etching techniques capable of producing anodes close to a micron in diameter with excellent electrical characteristics. This included the first fabrication of planar diodes with anodes less than one micron in diameter.
- Proposed a preliminary design for a 600 GHz subharmonically pumped diode chip, and demonstrated all of the required fabrication processes.

9.3 Future Work

The two significant goals of this research were to fabricate a diode pair for use at millimeter wavelengths, and investigate issues related to the future fabrication of submillimeter diode pairs. This work, and that of many other SDL researchers has laid much of the groundwork required to fabricate these devices, yet there is more to accomplish. Operation at submillimeter wavelengths requires a reduced junction capacitance, and better understanding of the parasitic reactances.

The junction capacitance can be reduced by using dry etching techniques to form submicron diameter anodes. Although a 0.9 μm anode has been demonstrated, this is perhaps too large for an optimized design at 600 GHz. Thus a new photolithography mask set mask should be fabricated so that the smaller anode diameters can be achieved

The parasitic reactances can be minimized by reducing the physical dimensions of the diode pair. Smaller pads will certainly reduce the large pad-to-pad capacitance that currently limits the performance of planar diodes. However, these small pads will increase the series resistance of the diode unless a new ohmic contact technology is developed. The use of InGaAs non-alloyed ohmic contacts should be added to the SDL's planar diode technology because they have the lower specific contact resistances required for small pads. The additional photolithography and subtractive processes that would be required are easier, and more reliable than the metallurgically complex SnNi/Ni/Au technology currently used. Furthermore, this technology eliminates the high temperatures associated with the alloy step which are suspected of forcing the SiO_2 to separate from the GaAs near the ohmic contact. This separation can allow the surface channel etchant to attack the GaAs near the anode. Non-alloyed Ohmic Contacts will also allow the anodes to be thinned anodically and plated before the ohmic contacts are formed. An acceptance criterion for a non-alloyed ohmic contact technology must be that the ohmic contact metals adhere well to the semiconductor. Small, low resistance pads are of little use if they separate from the InGaAs after the chip is bonded to a circuit. This adhesion criterion should therefore include thermal cycling and vibrational tests of chips soldered to striplines.

The performance of the diode pair can be improved further by developing a three terminal technology that allows each of the two diodes to be biased individually. This design has two benefits. Since each diode is biased near its turn-on voltage, the amount of LO power required to drive a subharmonically pumped mixer is reduced significantly. Also, individual biasing reduces the effects of anode mismatches by eliminating any existing DC currents.

Finally, a new set of waveguide models must be studied to learn more about the inductive effects associated with two anode contact fingers. This includes the fringing inductance associated with the abrupt change in width associated with the ohmic contact pad and the fingers, and the mutual inductance of the fingers themselves. Knowledge of these inductances will allow the designer to avoid resonances that degrade performance when the diodes begin to conduct twice in one LO cycle. This study should attempt to find an empirical relationship between the geometry of the fingers, the pad width, and the geometry of the waveguide. Associated with this study must be an extension of Kerr's analysis of subharmonically pumped mixers using his multiple reflection algorithm to include the effects of mutual inductance. Without the knowledge gained from these models, future designers are forced to rely upon a trial-and-error technique. Such an approach would require a mask set that yielded several geometries within one batch. Each of these different devices would then have to be tested in a mixer until an acceptable design was found.

In spite of the amount of proposed work, this anti-parallel technology can be extended immediately to submillimeter wavelengths. The performance of these prototype devices will certainly be improved through the proposed work; however, the

demonstration of excellent results at submillimeter wavelengths is in the near future.

APPENDIX A

PHOTOLITHOGRAPHY MASK SET

The photolithography mask set was designed using AutoCAD (Autodesk, Inc.) and a SUN 386i computer work station. The drawing files were converted to the CALMA GDSII format using Step Electronics ASM3500 AutoCAD to GDSII Translator before being sent to Perkin-Elmer (their Electron Beam Technology/ALO Division which is now part of Dupont Photomasks, Inc.) on 9 track tape. There they were converted to the MEBES format for use on their electron beam machines.

The mask set consists of seven separate 3×3 inch quartz plates. This plate size was chosen over the standard 4×4 inch plate size to save money. Fewer plates are needed since the smaller sized plate actually has a larger accessible area because it can be mounted on the mask holder in different positions. This is important since the mask aligner's wafer chuck moves only about one inch horizontally or vertically, to place the 0.26×0.22 inch wafer under the desired pattern.

Each plate was first divided into an 8×6 array of 48 wafer patterns, or dies. A total of 81 unique dies exist in this set, with four copies of each for redundancy. Twelve dies were included in one top level file for each plate, with the lower left corner of each pattern positioned at the origin of AutoCAD's "world coordinate system." This allowed each die to be written as a complete pattern by the electron beam, avoiding the necessity of aligning incomplete patterns between runs. This eliminated one concern regarding the acceptability of the set.

One top level file contained only nine dies: 4 surface channel, 4 solder plate, and one fiducial die. The corresponding plate contains four copies of the surface channel and solder plate die, and 16 copies of the fiducial.

The wafer die is itself divided into a 6x25 array of device unit cells and six alignment unit cells. These arrays are bounded by two electroplating tabs. The four corners of the wafer are used as fiducials where each die transfers its version number, providing an "on-wafer" record of the processing.

The University of Virginia logo in the upper right corner marks the top of the wafer, and is used to orient the wafer during processing. Each unit cell contains two devices, providing a total of 300 identical diode pairs on each wafer. The unit cell pattern was drawn and stored in a separate file. A copy of this pattern is then written into one unit cell location in the wafer drawing. It is then "**array**ed" into the remaining locations. This saves file space since the drawing is stored only once, and copied to the remaining 149 locations when the pattern is generated. Also, each unit cell was drawn with a minimum of pattern overlap to reduce the electron beam write time required. Only one layer is used in each unit cell file. Each wafer die is given a 2 part number, such as 02.07. The digits left of the decimal indicate the mask level, and the digits to the right indicate the version of that level. The decimal is dropped in file names, so the unit cell drawing for version 07 (50 μm long fingers, spaced 20 μm apart) of the ohmic contact (level 02) is in file "UC0207.DWG." This unit cell is used to create the wafer die (file "W0207.DWG") for this version of the ohmic contact pads. The mask levels, which correspond to the first two digits, are listed in Table A.1. The version of each mask level (the second two digits) is indicated in Table A.2. There is only one version of the

Fiducial Level, it is referred to as 01.00.

Table A.1
Mask Level Numbers

Process	Level Name	Level Number	Resides On Mask No.
Alignment Markers	Fiducial	01	1
Ohmic Contact Pads	Pads	02	2
Anodes	Anodes	03	3,4,5
Anodes Fill	Anode Fill	04	6
Anode Contact Fingers	Fingers	05	7
Surface Channel	Channel	06	1
Solder plate	Solder plate	07	1

Table A.2
Mask Level Version Numbers

Finger Length μm	Finger Spacing μm	Mask Levels 02, 04, 05, 06, 07	Mask Level 03 Anode Diameter 1 μm	1.5 μm	2 μm
15	20	01	01	02	03
	40	02	04	05	06
	60	03	07	08	09
25	20	04	10	11	12
	40	05	13	14	15
	60	06	16	17	18
50	20	07	19	20	21
	40	08	22	23	24
	60	09	25	26	27
75	20	10	28	29	30
	40	11	31	32	33
	60	12	34	35	36

Only a limited subset of the AutoCAD commands were known to be compatible with the GDSII translator when this mask set was drawn. Therefore, the commands used to create the drawings were limited to:

text	block
circle	insert
donut	explode
solid	array
pline	mirror

The **text** command does translate to GDSII, but in a block form that is adequate for a copyright statement. The **circle** and **donut** commands can be used to draw anodes; however, the **circle** command uses less disk space. Use of the **pline** should be limited to lines of constant (non-zero) width and arcs. The combination of **block**, **insert**, and **array** is useful for saving time and disk space by copying existing drawings upon pattern regeneration. Do not use the scale option when inserting. Scaling is compatible after the

block references have been destroyed by the **explode** command. The AutoLISP command programming feature proved to be very useful when inserting unit cell drawings into wafer die drawings. Finally, layer zero was not used since it was believed to be incompatible with the GDSII translator.

The mask set was made on 60 mil quartz plates with a "see through" film of chromium to the following tolerances. The electron beam was calibrated to the one micron specification of the National Bureau of Standards. The patterns were drawn with one unit of length in AutoCAD representing one micron. The maximum defect size tolerated was 1 micron, with no more than 2 defects in each square inch. The registration of each wafer die was within 0.25 microns of its correct position on the mask. The minimum feature tolerance and writing address are listed in Table A.3.

Table A3
Mask Set Tolerances

Level	Name	Tolerance	Writing Address
1	Fiducials	2 μm dia. ± 0.2 μm	0.125
2	Pads	10 μm rad. ± 0.2 μm	0.25 μm
3	Anodes	1 μm dia. ± 0.1 μm	0.125 μm
4	Anode Fill	6 μm dia. ± 0.2 μm	0.25 μm
5	Fingers	2 μm hor. ± 0.2 μm	0.25 μm
6	Channel	5 μm ver. ± 0.3 μm	0.25 μm
7	Solder Plate	50 μm ver. ± 1 μm	0.25 μm

APPENDIX B

ANTI-PARALLEL DIODE FABRICATION SEQUENCE

The specific details of the fabrication sequence used to create the standard, GaAs diode pairs is presented in this Appendix.

UNIVERSITY OF VIRGINIA
SEMICONDUCTOR DEVICE LABOATORY
THORNTON HALL
CHARLOTTESVILLE, VA 22903

ANTIPARALLEL DIODE FABRICATION SEQUENCE
(P.H.Ostdiek: REV 6/27/91 of W.L.Bishop: Surface Channel Technology)

WAFER/THICKNESS_____ ANODE DIAMETER_____

TECHNICIAN_____ EPI THICKNESS_____

START DATE_____ FINGER LENGTH/SPACING_____

COMMENTS_____

_____

Codes:
- BD - Blow dry w/ N_2
- ALC - Alconox
- ETH - Ethanol
- T - Temperature
- P - Power
- BW - Apiezon-W wax
- t - Time
- DI - Deionized water
- IR - Infrared
- TCA - Trichloroethane
- TCE - Trichloroethylene
- d - thickness
- RT - Room Temperature
- ACE - Acetone
- V - Voltage
- METH - Methanol
- US - Ultrasound
- ↓ - Continuous process
- ↔ - End of process

STEP NO.	PROCESS	PARAMETERS	COMMENTS
1	**WAFER BEVELING**	**DATE(S)**_____	
1.1	Remove wafer from main slice	Hotplate, T = 125 °C	
1.2 ↓	Clean wafer to remove G-wax	ACE spray ACE boil and BD, 3x ETH spin	
1.3 ↓	Inspect	Surface quality	
1.4 ↓	Mount wafer to beveling rod	Heat rod 2 min, w/hotplate on 2 Remove and apply G-wax	
1.5 ↓	Spray coat wafer	BW/TCE solution, spray on w/airbrush	
1.6 ↓	Dry wax	IR lamp, 100 W, 10 inches, t = 45 min	
1.7 ↓	Bevel wafer edges	4/0 paper, 17 degrees, 15 strokes	

1.8 ↔	Etch wafer on rod	1:1:5::H_2O_2:NH_4OH:DI. 3 min Running DI	
1.9 ↓	Remove black wax	Spray w/TCA, BD	
1.10 ↓	Remove wafer	Heat rod 2 min. w/ hotplate on 2 Remove and push wafer off	
1.11 ↓	Remove G-wax	ACE spray	
1.12 ↓	Clean wafer	TCA; TCA; ACE; ACE: boil and BD in each solvent	
1.13 ↔	*Inspect*	*Surface quality*	
2	**WAFER ANODIZE AND PROFILE**	**DATE(S)**_____	
2.1 ↓	Clean wafer	ETH spin and scrub ETH; TCA; METH: 2X boil and BD in each	
2.2 ↓	Etch wafer to remove native oxide	BOE 10:1 (no Superwet), 10 sec DI, 10 sec, 2X; BD	
2.3 ↔	CV on Hg probe	1 MHz, 0.01 volts	V_{bias} = _____ Attach n_x plots d_{epi} = _____ n_{epi} = _____
2.4 ↓	Clean μscope slide	Scrub w/ ALC ALC in 100% US Running DI rinse; BD METH boil; BD	
2.5 ↓	Clean wafer	ETH spin ETH; TCA; METH: 2X boil and BD in each	
2.6 ↓	Mount wafer to slide	Molten Apiezon-W at T = 125 °C	
2.7 ↓	Clean plating fixture probe tip	TCA spray; BD; repeat as req'd	
2.8 ↓	Mount slide w/ wafer to plating fixture	Apply droplet of TCE/Black-wax to probe tip Immediately contact wafer end	
2.9 ↓	Dry wafer/plating fixture assembly	IR lamp, 100 W, 10 inches, t = 45 min	
2.10 ↓	Etch native oxide	BOE 10:1, 5 sec; DI 2x, keep wet	
2.11 ↓	Anodize wafer to desired voltage	Ethylene glycol:DI:tartaric acid::100:50:1.5 pH adjusted to 6.5 w/ NH_4OH 14.5 A/volt, 370 μA, illumination on	V = _____ epi removed = _____

2.12 ↔	Rinse	Running DI, 60 sec minimum; BD	
2.13	Inspect	Oxide color, appearance	Oxide color = _____ Appearance = _____
2.14 ↓	Remove slide from plating fixture and remove wafer from slide	Hotplate at T = 125 °C	
2.15 ↔	Clean wafer	TCA spray TCA boil and BD, 3X	
2.16	Remove anodic oxide	1:1::HCl:DI, 10 sec Running DI wash, 60 sec; BD	
2.17 ↓	Etch wafer to remove native oxide	BOE 10:1 (no Superwet), 10 sec DI, 10 sec, 2X; BD	
2.18 ↓	Clean wafer	Meth boil; BD	
2.19 ↔	CV on Hg probe	1 MHz, 0.01 volts	V_{bias} = _____ Attach n_x plots d_{epi} = _____ n_{epi} = _____
2.20	Repeat anodize and profile (exclude 2.1-2.3)	To desired epi thickness	d_{epi} = _____
2.21	Repeat anodize (2.4-2.16) to remove 50 Å	3.4 V, 370 μA	Remove any epi that contacted Hg in past steps
3	**OXIDE DEPOSITION**	**DATE(S)**_____	
3.1	Clean all system glassware and susceptor	BOE 725:DI::1:1, 5 min CW 4X fill/dump DI 4X fill/dump 120 C, 20 min bake	
3.2	Assemble system, purge and preheat	FGLP 0.2 μm filter Fill/dump purge 15X Preheat to 350 C, flow purge 20 min	
3.3 ↓	Clean wafer (Note: run scrap wafer for thickness measurement)	BOE 10:1(no Superwet) 10 sec DI 10 sec; BD ETH spin METH, TCA, ETH: boil and BD ETH boil 30 sec just before oxide growth	

3.4 ↓	Deposit oxide	350 C; silane = 65; oxygen = 71; nitrogen = 14 5000 Å	t_{oxide} = _____ (estimated)
3.5 ↔	Remove wafer and shutdown CVD system	Heater off Silane tank off, pressure to 0 N_2 purge on, O_2 off Fill/dump purge 15X Flow purge, 20 min	
3.6	Inspect wafer	Oxide color, pinholes, defects	d_{oxide} = _____
3.7	Oxide uniformity	Tencor wafer edge to edge symmetrically	$d_{oxide(center)}$ - $d_{oxide(edge)}$ = _____
3.8	Measure oxide thickness	Mask 1/2 scrap wafer with molten Black wax BOE 10:1, 4 min TCA spray, BD Tencor	$d_{oxide,scrap}$ = _____
4	**BASE ALIGNMENT PHOTOLITH AND ETCH**	T_{room} = 72 °F, %RH = 45	T_{room} = _____, %RH = _____ Mask level = _____
4.1 ↓	Clean wafer	ETH spin scrub ETH; TCA; METH: boil and BD METH boil, 30 sec	
4.2 ↓	Drybake wafer	T = 120 °C, t = 5 min, hotplate	
4.3 ↓	Apply HMDS	Vapor phase, fresh HMDS, 10 min	
4.4 ↓	Apply resist	AZ 1370SF, 6000 RPM, 30 sec, HVLP filter, flood resist over wafer edges	Resist Dropper _____ Dates: Stock _____
4.5 ↓	Softbake	T = 90 °C, t = 45 sec, hotplate	
4 6 ↓	Condition	10 min, room conditions	
4.7 ↓	Expose	MJB3 UV 400, 10 mW/cm^2, 10 sec, vacuum contact	
4.8 ↓	Develop	AZ DEV:DI::1:1, 60 sec, T = 22 °C DI 2x, BD	
4.9 ↓	Inspect and rework as req'd	Resist removal	
4.10 ↓	Hardbake	T = 120 °C, 45 sec, hotplate	
4.11 ↔	Etch	BOE 10:1 Superwet, T = 22 °C, 35 Å/sec to leave 900-1000 Å; DI 2x; BD	

4.12	Inspect pattern	Violet to gray violet color (900-1000 Å)	Color = _____ d_{oxide} = _____
4.13	Remove resist	1112A:DI::1:1, as req'd at T=60 - 90 °C, Running DI wash 60 sec; hot DI 2X; BD	
5	**OHMIC CONTACT PHOTOLITH**	**DATE(S)**_____ T_{room} = 72 °F, %RH = 45	T_{room} = _____, %RH = _____ Mask level = _____
5.1 ↓	Clean wafer	ETH spin no scrub ETH; TCA; METH: boil and BD METH boil, 30 sec	
5.2 ↓	Drybake wafer	T = 120 °C, t = 5 min, hotplate	
5.3 ↓	Apply HMDS	Vapor phase, fresh HMDS, 10 min	
5.4 ↓	Apply resist	AZ 1350J, 5000 RPM, HVLP filter, flood resist over edge of wafer	
5.5 ↓	Softbake	T = 90 °C, t = 45 sec, hotplate	
5.6 ↓	Condition	10 min, room conditions	
5.7 ↓	Expose	MJB3 UV 400, 10 mW/cm^2, 7 sec, vacuum contact	
5.8 ↓	Develop	AZ DEV:DI::1:1, 60 sec, DI 2x, BD	
5.9 ↓	Inspect and rework as req'd	Resist removal	
5.10 ↓	Hardbake	T = 120 °C, 45 sec, hotplate T = 150 °C, 45 sec, hotplate	
6	**OHMIC CONTACT ETCH AND PLATE**	**DATE(S)**_____	
6.1 ↓	O_2 plasma descum	500-700 mT, 50 W (forward), 5 min	
6.2 ↓	Etch	BOE 10:1 (No Superwet), 35 Å/sec to remove oxide + 20 sec; DI 2x; BD	t_{etch} = _____
6.3 ↓	Inspect pattern and etch	As above until all oxide removed	
6.4 ↓	Oxide and resist thickness	Tencor near UVa logo	$d_{oxide,resist}$ = _____

6.5 ↓	Etch GaAs	BOE 10:1 (no Superwet), 10 sec Running DI, keep wet Citric acid(50%):H_2O_2(30%)::10:1, T = 22 °C 2 min 30 sec (≈33 Å/sec) to remove 5000 Å DI, Running DI rinse 2 min	t_{etch} = _____
6.6 ↓	Depth GaAs etched	Tencor near UVa logo	$d_{GaAs,oxide,resist}$ = _____ — $d_{etched\ GaAs}$ = _____ Etch rate = _____
6.7 ↓	Repeat 6.5 until 5000Å GaAs removed	Use above data to compute new etch time	t_{etch} = _____
6.8 ↓	Clean μscope slide	Wipe w/ clean wiper; TCA, ACE, METH: spray & BD	
6.9 ↓	Mount wafer to slide	Molten Apiezon-W at T = 125 °C	
6.10 ↓	Clean plating fixture probe tip	TCA spray; BD; repeat as req'd	
6.11 ↓	Mount slide w/ wafer to plating fixture	Apply droplet of TCE/Black-wax to probe tip Immediately contact wafer end	
6.12 ↔	Dry wafer/plating fixture assembly	IR lamp, 100 W, 10 inches, t = 45 min	
6.13 ↓	Plasma descum	O_2, 50 W, 5 min	
6.14 ↓	Etch wafer on fixture	BOE 10:1 (not Superwet), 10 sec DI, 2X, 3 sec each, keep wet	
6.15 ↓	Plate tin-nickel	Immerse in Ni-Stan, 50 C (bath 55 C), 10 sec (no plate), Capacitor pulse plate, ½ μF, 200 pulses, 40V; DI, keep wet, change to DC mode	NiStan Date: _____
6.16 ↓	Plate tin-nickel	Immerse in Ni-Stan, 50 C (bath 55 C), 10 sec (no plate), DC plate 0.5 mA, 70 sec DI, running DI, keep wet	
6.17 ↓	Plate nickel	Immerse in nickel, RT, 10 sec (no plate) DC plate 0.5 mA, 2 min DI, running DI, keep wet	
6.18 ↓	Plate gold	Immerse in Autronex-N, RT, 10 sec (no plate), DC plate 0.5 mA, 2 min, DI, running DI, 60 sec; BD	
6.19 ↔	Etch back oxide	BOE 10:1, 22 °C, 1 min, Running DI, 60 sec; BD inspect at μscope repeat 3x, stop if oxide is attacked	

6.20	Remove slide from plating fixture and remove wafer from slide	Hotplate at T = 125 °C	
6.21	Clean wafer	Spray w/ TCA TCA boil and BD, 3X; ACE boil 3X	
6.22	Remove resist	O_2 plasma, 500-700 mT, 50 W, 10-20 min; If necessary:1112A:DI::1:1, as req'd at T≈60 -90 °C; Running DI wash 60 sec, Hot DI 2X	
6.22	Inspect	Plating quality (smoothness, uniformity)	
6.23	Photograph	1 photo 1.5X objective 1 photo 100X objective	Attach photos
7	**OHMIC CONTACT ALLOY AND OVERPLATE**	**DATE(S)**_____	
7.1 ↓	Clean wafer (omit if plated recently)	METH boil, 30 sec	
7.2 ↓	Insert wafer into alloy chamber	Purge w/ 95:5::N_2:H_2, 5 min	
7.3 ↓	Alloy wafer	Raise strip heater current quickly to 1.7 A Dwell 20 sec Raise current to 2.1 A, wait for complete alloy plus 5 sec Current quickly to 0 A	Total Alloy t = _____ (sec) Bubbled? Yes/No Peeled? Yes/No Describe appearance:
7.4 ↓	Cool wafer and remove from alloy chamber	Purge w/ 95:5::N_2:H_2, 5 min	
7.5	Photograph	1 photo 1.5X objective 1 photo 100X objective	Attach photos
7.6	Measure step height	Tencor near UVa logo	d_{step} = _____
7.7 ↓	Clean μscope slide	Wipe w/ clean wiper; TCA, ACE, METH spray & BD	
7.8 ↓	Clean wafer	ETH, TCA, METH, boil and BD in each METH boil, 30 sec, BD	
7.9 ↓	Mount wafer to slide	Molten Apiezon-W at T = 125 °C	
7.10 ↓	Clean plating fixture probe tip	TCA spray; BD; repeat as req'd	

7.11 ↓	Mount slide w/ wafer to plating fixture		
7.12 ↓	Plasma Descum	O_2, 50 W fwd, 5 min	
7.13 ↓	NaOH etch	NaOH (23.3 g/l), 5 min. Running DI, 60 sec; keep wet	
7.14 ↓	Plate gold	Autronex-N, RT, immerse 10 sec (*no plate*) Pulse plate, 10 μF, 40 V, ≈1.5Å/pulse, fill to bottom of oxide DI; running DI; BD	$\#_{pulses}$ = _____
7.15 ↓	Measure step height	Tencor near UVa logo	d_{step} = _____ $d_{plated\ Au}$ = _____
7.16 ↔	Repeat 7.14-7.15 as req'd	*Fill Au to bottom of oxide*	
7.17	Remove slide from plating fixture and remove wafer from slide	Hotplate at T = 125 °C	
7.18	Clean wafer	Spray w/ TCA TCA boil and BD, 3X	
7.19	Inspect	Plating quality (smoothness, uniformity, adhesion scrape test)	Adhesion = _____
8	**ANODE PHOTOLITH AND FIRST ETCH**	T_{room} = 72 °F, %RH = 45	T_{room} = _____, %RH = _____ Mask Level = _____
8.1 ↓	Clean wafer	ETH spin ETH; TCA; METH: boil and BD in each METH boil, 30 sec	
8.2 ↓	Drybake	T = 120 °C, t = 5 min, hotplate	
8.3 ↓	Apply HMDS	Vapor phase, fresh HMDS, 10 min	
8.4 ↓	Apply resist	AZ 1370SF, 6000 RPM, HVLP filter, flood resist over wafer edges	
8.5 ↓	Softbake	T = 90 °C, t = 45 sec, hotplate	
8.6 ↓	Condition	10 min, room conditions	
8.7 ↓	Expose	MJB3 UV 400, 10 mW/cm^2, 6 sec, vacuum contact	
8.8 ↓	Develop	AZ DEV:DI::1:1, T = 22 °C, 60 sec DI 2x, BD	

8.9 ↓	Inspect pattern and rework as req'd	Resist removal; anode diameter	
8.10 ↓	Hardbake	45 sec, 120 C, hotplate	
8.11 ↓	Inspect pattern	Anode diameter	Anode diameter = _____
8.12 ↔	Etch pattern	Prewet DI w/30% US, 2 min, keep wet BOE 10:1 Superwet, T = 22 °C, 35 Å/sec, to leave 800 Å in windows DI 2x; BD	t_{etch} = _____
8.13	Remove resist, DI wash, BD	1112A:DI::1:1, as req'd, T = 90 °C Running DI wash 60 sec; hot DI, 2X	
8.14	Inspect		Anode diameter = _____
8.15	Photograph	1 photo, large test array, 100X objective 1 photo, small test array, 100X objective 1 photo, device anode, 100X objective	Attach photos
9	**ANODE FINAL ETCH AND PLATE**	**DATE(S)**_____	
9.1 ↓	O_2 plasma descum	500-700 mT, 50 W(forward), 10 min	
9.2 ↓	Prewet	DI, 30% US, 5 min, vigorous agitation	
9.3 ↓	Etch oxide	BOE 10:1 Superwet, remove oxide plus 20% DI, keep wet	t_{etch} = _____
9.4 ↓	Fizz etch	23 g/l NaOH:30% H_2O_2::30 ml:3 drops, 30% US, 10 sec; Vigorous BD, 5 sec	
9.5 ↓	Platinum plate	Platinex III, T = 90 C, 30% US immerse to tweezer mark, 20 sec (no plate), 20 mA DC, 2 min DI, 10 sec, keep wet	t_{plate} = _____
9.6 ↔	Gold plate	Autronex-N, T = 35 C, 30% US, immerse to tweezer mark, 10 sec (no plate), 20 mA, 2 min DI, running DI; BD	t_{plate} = _____
9.7	Inspect	Add DI to Pt and Au solutions to replace water lost during heating	Anode diameter = _____

10	**ANODE FILL**	T_{room} = 72 °F, %RH = 45	T_{room} = _____, %RH = _____ Mask Level = _____
10.1 ↓	Clean wafer	ETH spin ETH; TCA; METH: boil and BD METH boil, 30 sec	
10.2 ↓	Drybake wafer	T = 120 °C, t = 45 sec, hotplate	
10.3 ↓	Apply HMDS	Vapor phase, fresh HMDS, 10 min	
10.4 ↓	Apply resist	AZ 1370SF, 6000 RPM, HVLP filter, flood resist over edges	
10.5 ↓	Softbake	T = 90 °C, t = 45 sec, hotplate	
10.6 ↓	Condition	10 min, room conditions	
10.7 ↓	Expose	MJB3 UV 400, 10 mW/cm^2, 20 sec, vacuum contact	
10.8 ↓	Develop	AZ DEV:DI::1:1, 60 sec, T = 22 °C DI 2x; BD	
10.9 ↓	Inspect and rework as req'd	Alignment accuracy **Important: remove resist w/ ACE and O_2 plasma, do not use 1112A!**	
10.10 ↓	Hardbake	T = 120 °C, 45 sec, hotplate	
10.11 ↓	Prewet wafer	DI in 30% US, 2 min, keep wet	
10.12 ↓	HCl pickle	HCl:DI::1:1, RT, 15 sec DI; running DI, keep wet	OPTIONAL
10.13 ↔	Gold plate	Autronex-N, RT, 30 % US, immerse to tweezer mark 10 sec (no plate) 2 μF, 3000 pulses, 28 V DI; running DI, BD	
10.14	Inspect	Anodes full?	
10.15	Replate	If necessary, replate from 10.12, excluding 10.13	Total pulses to fill = _____
10.16	Remove resist	1112A:DI::1:1, 30 sec, T=60 °C Running DI wash 60 sec; hot DI, 2X; BD	
10.17	Inspect	Fill level; plating quality	

10.17	Photograph	1 photo, large test array, 100X objective 1 photo, small test array, 100X objective 1 photo, device anode, 100X objective	Attach photos
10.18	IV probe	Whisker contact 12 anodes, 2 per column: centered near upper and lower half of each Attach forward and reverse IV and creep data	Currents: 100nA,1μA,10μA,100μA,_____,_____ Averages: dV = _____(100μA,10μA) V_{knee} = _____(1μA) V_{rev} = _____(1μA) R_s = _____ V_{creep} = _____(10μA)
11	**SPUTTER DEPOSITION: CHROMIUM & GOLD**	**DATE(S)**_____	
11.1 ↓	Clean wafer	ETH spin ETH; TCA; METH: boil and BD METH boil, 30 sec; BD	
11.2 ↓	Clean μscope slide (1/2 slide)	Scrub w/ ALC ALC in 100% US Running DI rinse; BD METH boil; BD	
11.3 ↓	Mount wafer to slide	Adhere with small amount of Apiezon L-grease in wafer center	
11.4 ↓	Clean chromium target	Spray with Freon and BD	
11.5 ↓	Clean substrate holder	Wipe w/ Freon soaked wiper; BD	
11.6 ↓	Load wafer and target into turbo sputter system	Set bias capacitor to 40% vane overlap	
11.7 ↔	Pump system down	4 hours minimum, turbo cooling water on	P_{base} = _____
11.8 ↓	Admit argon	Stabilize at 20 mTorr	P_{work} = _____
11.9 ↓	Etch target	Shutter closed C_{tune}:178½ Sputter mode C_{load}:035 V_T = 600 V t = 5 min, target and sample cooling on	$P_{forward}$ = _____ $P_{reverse}$ = _____ C_{tune} = _____ C_{load} = _____

11.10 ↓	Etch sample	Shutter open C_{tune}:185 Etch modeb C_{load}:045 V_S = 360 V t = 3 min, target and sample cooling on	$P_{forward}$ = _____ $P_{reverse}$ = _____ C_{tune} = _____ C_{load} = _____
11.11 ↓	Etch target	Shutter closed C_{tune}:178½ Sputter mode C_{load}:035 V_T = 600V t = 5 min, target and sample cooling on	$P_{forward}$ = _____ $P_{reverse}$ = _____ C_{tune} = _____ C_{load} = _____
11.12 ↓	Sputter chromium	Shutter open C_{tune}:182 Sputter mode C_{load}:032 V_T = 600 V V_S = 80 V t = 10 min, target and sample cooling on	$P_{forward}$ = _____ $P_{reverse}$ = _____ C_{tune} = _____ C_{load} = _____
11.13 ↓	RF power off and vent chamber	Nitrogen vent	
11.14 ↓	Clean gold target	Spray with Freon and BD	
11.15 ↓	Load gold target into turbo sputtering system		
11.16 ↔	Pump system down	4 hrs minimum	P_{base} = _____
11.17 ↓	Admit argon	Stabilize at 20 mTorr	
11.18 ↓	Etch target	Shutter closed C_{tune}:177½ Sputter mode C_{load}:035 V_T = 600 V t = 5 min, target and sample cooling on	$P_{forward}$ = _____ $P_{reverse}$ = _____ C_{tune} = _____ C_{load} = _____
11.19 ↓	Etch wafer	Shutter open C_{tune}:185 Etch mode C_{load}:045 V_S = 360 V t = 5 min, target and sample cooling on	$P_{forward}$ = _____ $P_{reverse}$ = _____ C_{tune} = _____ C_{load} = _____
11.20 ↓	Etch target	Shutter closed C_{tune}:177½ Sputter mode C_{load}:035 V_T = 600 V t = 5 min, target and sample cooling on	$P_{forward}$ = _____ $P_{reverse}$ = _____ C_{tune} = _____ C_{load} = _____
11.21 ↔	Sputter gold	Shutter open C_{tune}:181½ Sputers mode C_{load}:032 V_T = 600 V V_S = 80 V t = 10 min, target and sample cooling on	$P_{forward}$ = _____ $P_{reverse}$ = _____ C_{tune} = _____ C_{load} = _____
11.22	RF power off; vent chamber	N_2 vent	

11.23	Remove slide w/ wafer and inspect	Appearance	
11.24	Clean substrate holder and pump down	Wipe w/ Freon soaked wiper; BD	
11.25	Clean wafer	Spray front and back of wafer w/ TCA TCA boil and BD, 3X	
11.26	Clean slide	TCA spray	
11.27	Adhesion test	Apply Scotch tape across slide width and burnish Pull tape off quickly	Adhesion = _____
11.28	Cr and Au thickness	Mask 3-5 lines on slide w/ Apiezon-W Etch in gold etch and Tencore Etch in chrome etch and Tencore	T_{total} = _____ T_{chrome} = _____ T_{gold} = _____
12	**ANODE CONTACT PHOTOLITH AND PLATING**	**DATE(S)** T_{room} = 72 °F, %RH = 45	T_{room} = _____, %RH = _____ Mask Level = _____
12.1 ↓	Clean wafer	ETH spin ETH; TCA; METH: boil and BD METH boil, 30 sec	
12.2 ↓	Drybake wafer	T = 120 C, t = 45 sec, hotplate	
12.3 ↓	Apply HMDS	Vapor phase, fresh HMDS, 10 min	
12.4 ↓	Apply resist	AZ 4330, 6000 RPM, HVLP filter, flood over wafer edges	
12.5 ↓	Softbake	T = 90 C, t = 45 sec, hotplate	
12.6 ↓	Condition	10 min, room conditions	
12.7 ↓	Expose	MJB3 UV 400, 10 mW/cm^2, 30 sec, vacuum contact	
12.8 ↓	Develop	AZ 400K:DI::1:4, 60 sec, T = 22 °C DI 2x; BD	
12.9 ↓	Inspect and rework as req'd	Complete resist removal	
12.10 ↓	Deep UV cure	30 min	
12.11 ↓	Hardbake	T = 120 °C, 20 min, oven	

12.12	O_2 Clean	O_2, 50 W, 5 min	
12.13 ↓	Inspect	Absence of resist flow	
12.14 ↓	Measure resist thickness	Tencor center anode contact pattern	d_{resist} = _____
12.15 ↓	Clean μscope slide	Scrub w/ ALC ALC in 100% US Running DI rinse; BD METH boil; BD	
12.16 ↓	Mount wafer to slide	Molten Apiezon-W at T = 125 °C	
12.17 ↓	Clean plating fixture probe tip	TCA spray; BD; repeat as req'd	
12.18 ↓	Mount slide w/ wafer to plating fixture	Apply droplet of TCE/Black-wax to probe tip Immediately contact wafer end	
12.19 ↓	Dry wafer/plating fixture assembly	IR lamp, 100 W, 10 inches, t = 45 min	
12.20 ↓	Plate gold	HCl:DI::1:1, 2 min DI; running DI, 30 sec, keep wet Autronex-N, RT, dwell 10 sec, 300 pulses, 1 μF, 28 V, DI; running DI, keep wet BDT-200, T = 50 C, dwell 10 sec, no stir bar, 250 μA, 1kHz, vigorous mechanical agitation, no N_2 or air bubbler, 20 min (ring stand); DI; running DI wash, 60 sec; BD	
12.21 ↓	Measure Au thickness	Tencor center anode contact pattern	$d_{Au,plated}$ = _____
12.22 ↔	Inspect and plate as req'd to fill resist	Plate quality Plate thickness	
12.23	Remove slide from plating fixture and remove wafer from slide	Hotplate at T = 125 °C	
12.24	Clean wafer	TCA spray TCA boil and BD, 3x	
12.25	Remove resist	1112A:DI::1:1, 30 sec, T=60 °C Running DI wash 60 sec; hot DI, 2X; BD	
12.26	Inspect and profile	Tencore profile wafer length	t_{finger} = _____
12.27	Photograph	1 photo 50X objective	Attach photo

13	**GOLD AND CHROMIUM ETCH**	**DATE(S)_ _____**	
13.1 ↓	Clean wafer	ETH spin ETH; TCA; METH: boil and BD METH boil, 30 sec; BD	
13.2 ↓	Clean μscope slide (1/2 slide used for deposition)	ETH; TCA; METH: boil and BD METH boil, 30 sec; BD	
13.3 ↓	Mount wafer to slide	Adhere with small amount of Apiezon L-grease in wafer center	
13.4 ↓	Clean dummy target	Spray with Freon and BD	
13.5 ↓	Clean substrate holder	Wipe w/ Freon soaked wipe and BD	
13.6 ↓	Load wafer and target		
13.7 ↔	Pump system down	1 hour minimum	P_{base} = _____
13.8 ↓	Admit argon	Stabilize at 20 mTorr	
13.9 ↓	Etch wafer	Shutter open C_{tune}:185 Etch mode C_{load}:048 V_S = 80 V t = 20 min, sample cooling on	$P_{forward}$ = _____ $P_{reverse}$ = _____ C_{tune} = _____ C_{load} = _____
13.10 ↓	RF power off; vent chamber	N_2 vent	
13.11 ↔	Remove slide/wafer and clean wafer	Spray front and back of wafer w/ TCA TCA boil 2X; BD	
13.12	Inspect wafer and re-etch as req'd	All sputtered gold removed?	
13.13 ↓	Clean wafer	ETH spin ETH; TCA; METH: boil and BD	
13.14	Photograph	1 photo 50 objective	Attach photo
13.15 ↓	Etch chromium	AZ Developer:DI:$KMnO_4$::325:175:5, wait 30 min calibrate on glass slide t_{etch}≈10 min (1 min for each min deposited) Running DI wash, 60 sec	t_{etch} = _____ (Slide should be perfectly clear when held to light)
13.16 ↔	Inspect	Cr removal Appearance	

13.17	Etch chromium	Repeat from 13.13 as req'd	
13.18	Photograph	1 photo 50X objective	Attach photo
13.19	Finger Thickness	Tencor center pair	$d_{fingers}$ = _____
14	**SURFACE CHANNEL PHOTOLITH AND ETCH**	**DATE(S)** _____ T_{room} = 72 °F, %RH = 45	T_{room} = _____, %RH = _____ Mask *Level* = _____
14.1 ↓	Clean wafer	ETH spin ETH; TCA; METH: boil and BD METH boil, 30 sec	
14.2 ↓	Drybake wafer	T = 120 C, t = 5 min, hotplate	
14.3 ↓	Apply HMDS	Vapor phase, fresh HMDS, 10 min	
14.4 ↓	Apply resist	AZ 1350J, 6000 RPM, HVLP filter, flood resist over wafer edges	
14.5 ↓	Softbake	T = 90 °C, t = 45 sec, hotplate	
14.6 ↓	Condition	10 min, room conditions	
14.7 ↓	Expose	MJB3 UV 400, 10 mW/cm^2, 7 sec, vacuum contact	
14.8 ↓	Develop	AZ DEV:DI::1:1, 60 sec. T = 22 °C DI 2x, BD	
14.9 ↓	Inspect and rework as req'd	Alignment	
14.10 ↓	Hardbake	T = 120 °C, 45 sec, hotplate	
14.11 ↓	Etch oxide	BOE 10:1 (no Superwet), as req'd to remove all oxide plus 20 % DI 2x; BD	t_{etch} = _____ (same t_{etch} used in step 6.2)
14.12 ↓	Inspect wafer		
14.13 ↓	Etch GaAs	1:1:10::23 g/l NaOH:H_2O_2:DI, RT Calibrate on scrap GaAs (≈0.6μm/min) Etch as req'd into semi-insulating GaAs Running DI wash, 60 sec; BD	t_{etch} = _____ $d_{channel}$ = _____ (calculated)
14.14 ↓	Inspect and re-etch as req'd	Optical channel depth Surface quality	$d_{channel}$ = _____ (optical) Surface quality = _____

14.15 ↓	Channel Discolored?	HCl:DI::1:1, t=30 sec	This removes colored stains at bottom of channel. Be certain the channel is etched into S-I GaAs!
14.16 ↔	Probe surface channel	Lab to reverse breakdown	V_b = _____
14.17	Remove resist	1112A:DI::1:1, 30 sec, T=60 °C Running DI wash 60 sec; hot DI, 2X; BD	
14.18	Measure channel depth	Tencore and attach data	
14.19	Photograph	1 photo, channel floor, 50X objective 1 photo, device anodes, 50X objective	Attach photos
15	**LAP DICE**	**DATE(S)**_____	
15.1 ↓	Apply protective coating	AZ PC, 1000 RPM, 5 sec, HVLP filter, flood over wafer edges	
15.2 ↓	Bake	T=120 C, 1 min, hotplate	
15.3 ↔	Mount wafer to lapping block	G-wax a. 125 C Push wafer flat w/ swab	
15.4	Set dial indicator	Set to original wafer thickness	
15.5	Lap	600 grit paper, wet	
15.6	Measure thickness	Dial indicator	
15.7	Repeat as req'd to desired thickness		Final dial indicator thickness_____
15.8	Clean wafer back	ACE spray and scrub to remove all G-wax	
15.9 ↓	Remove wafer from lapping block	Hotplate on low Soak block in ACE until wafer falls off	
15.10 ↔	Clean wafer	ACE boil and BD, 3x	
15.11 ↓	Mount wafer to silicon slice	Molten Apiezon-W at T= 125 C Push lightly at wafer ends to seat in wax	
15.12 ↓	Apply protective coating	AZ PC: Apply small droplet or spin on two coats at 4000 RPM w/ 120 C plate bake for each	
15.13 ↔	Dry protective coating	IR lamp, 100 W, 45 min, 10 inches	

15.14 ↓	Dice chips	Test blade and dress as req'd	Blade type = _____ RPM = _____ Feed Rate = _____
15.15 ↔	Remove resist	1112A:DI::1:1, 30 sec, T≈60 C Running DI wash 60 sec; hot DI, 2X; BD	
16	**IV TEST, SORT AND CLEAN**		
16.1	IV testing	All chips, attach data	
16.2 ↓	Remove chips	Remove chips soaking in a beaker of TCA	
16.3 ↔	Clean and store	Fill and decant above TCA beaker 5x to remove all Apiezon-W Spray/rinse chips out of beaker onto filter paper, Wipe work area with anti-static wipe, Store chips in Petri dishes or Gel Pak	

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