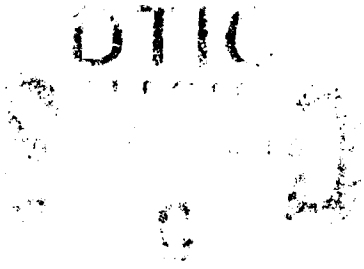


HDL-CR-91-043-1

November 1991

Radiation Effects Test Chip Guidelines

by David R. Alexander

Prepared by

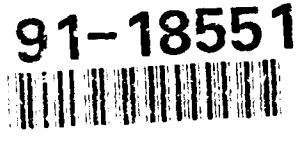
Mission Research Corporation
1720 Randolph Road, SE
Albuquerque, NM 87106-4245

Under contract

DAAL02-86-D-0043

(COTR: Harvey A. Eisen)

This work was sponsored by the Defense Nuclear Agency under subtask RVRA, work unit 190, entitled TREE Program Support.



U.S. Army Laboratory Command
Harry Diamond Laboratories
Adelphi, MD 20783-1197

The findings in this report are not to be construed as an official Department of the Army position unless so designated by other authorized documents.

Citation of manufacturer's or trade names does not constitute an official endorsement or approval of the use thereof.

Destroy this report when it is no longer needed. Do not return it to the originator.

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	November 1991	Final (Contractor), 28 Feb 87 to 8 Feb 91

4. TITLE AND SUBTITLE
Radiation Effects Test Chip Guidelines

5. FUNDING NUMBERS
C: DAAL02-86-D-0043
PE: 62120

6. AUTHOR(S)
David R. Alexander
(COTR: Harvey A. Eisen, SLCHD-NW-TS)

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Mission Research Corporation
1720 Randolph Road, SE
Albuquerque, NM 87106-4245

8. PERFORMING ORGANIZATION REPORT NUMBER
HDL-CR-91-043-1

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Harry Diamond Laboratories
2800 Powder Mill Road
Adelphi, MD 20783-1197

10. SPONSORING/MONITORING AGENCY REPORT NUMBER
MRC/ABQ-R-1288

11. SUPPLEMENTARY NOTES
AMS code: 612120.H2500
HDL PR: 266728

This work was sponsored by the Defense Nuclear Agency under subtask RVRA, work unit 190, entitled TREE Program Support.

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

Test chips and special test structures are assuming a role of ever increasing importance in the development of radiation-hardened microcircuits. The reason for this expanding role lies in the expense and complexity of VHSIC (very high speed integrated circuits) and VLSIC (very large scale integrated circuits) class microcircuits. Special devices are required to

1. investigate failure mechanisms,
2. evaluate process hardness,
3. develop design rules, and
4. provide for hardness assurance monitoring.

The purpose of this document is to provide information on a variety of devices which have been found useful in developing radiation-hardened microcircuits for metal oxide semiconductor (epi/bulk, SOS, and SOI) and bipolar technologies.

14. SUBJECT TERMS
Test structures, radiation testing, semiconductor hardening

15. NUMBER OF PAGES
194

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	17. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	UL

Contents

FIGURES

1. INTRODUCTION

1.1 Overview

Test chips and special test structures are assuming a role of ever increasing importance in the development of radiation-hardened microcircuits. The reason for this expanding role lies in the expense and complexity of VHSIC (very high speed integrated circuits) and VLSIC (very large scale integrated circuits) class microcircuits. Special devices are required to:

1. investigate failure mechanisms;
2. evaluate process hardness;
3. develop design rules; and
4. provide for hardness assurance monitoring.

The purpose of the following document is to provide information on a variety of devices which have been found useful in developing radiation-hardened microcircuits for MOS (epi/bulk, SOS, and SOI) and bipolar technologies.

1.2 Background

Test chips incorporating specialized test structures are widely used throughout the semiconductor industry for process development and control. The need for such devices was recognized early by several manufacturers, and there is an extensive literature base documenting their design and application. In the early 1970's, the National Institute of Standards and Technology (NIST), formerly National Bureau of Standards (NBS), became especially active in the development of standard test structure designs [1]. The 400 series of NBS Special Publications is an excellent source of historical design and application information. Much of the work in radiation effects test structures grew out of the NIST efforts.

Achieving a radiation-hardened microcircuit in any technology is a complex function of processing, electrical design, and layout. Test structures provide valuable information for optimization of each of these activities. Process variables (e.g., starting material characteristics, epitaxial layer characteristics, implant depths, drive-in times and temperatures, oxide growth procedures, and photolithographic dimension control) often have first-order effects on radiation hardness. Process control structures (e.g., van der Pauw devices, Kelvin contact devices, etc), in conjunction with devices designed to identify failure mechanisms, can provide valuable insight to process modifications for hardening [2].

The electrical design activity must consider the post-irradiation performance of circuit elements such as transistors, diodes, and resistors. The performance information is typically gathered from test devices which are representative of the elements used in the microcircuit design [3].

The layout activity translates the electrical design into a mask topography which will implement the circuit function in the process technology. The layout is constrained by the design rules defined for the technology from special test structures with variations in critical dimensions. These design rules often take the form of spacings between different layers in the fabrication process (e.g., buried layers, implants, and oxide boundaries). Design rules which may be adequate for commercial devices may require significant modification for a hardened microcircuit.

In selecting test structures for a particular application, the engineer must have a clear understanding of his objectives. The test structures selected must be appropriate for those objectives. In the development of a new process, the emphasis may initially be on identifying failure mechanisms. Simple structures for

process control and radiation effects characterization will be needed.

As the process becomes better defined, the emphasis may be on hardness evaluation to identify fabrication modifications which are most beneficial for performance and hardness. Both simple radiation characterization structures and small-scale macrocells will be required at this stage.

Once the process is well defined, the emphasis will probably shift to identifying design rules. Structures will be required with variations in their critical dimensions. Test results from such devices permit the engineer to establish design rules which will ensure hardened designs.

As the effort moves from development to production, the emphasis will shift from discovering rules to monitoring compliance with design rules, improving yield [4], and ensuring that performance will remain satisfactory under worst-case conditions. Test structures often form the basis for hardness assurance decisions.

When the emphasis is on identifying the importance of various failure mechanisms in determining process hardness, test structures should be selected to enhance the contribution of a particular mechanism to the observed radiation response. For example, in many metal-oxide semiconductor (MOS) technologies, post-irradiation source-to-drain leakage may be an important failure mechanism. The exact location of the leakage path must be determined in order to apply the appropriate hardening procedures. If the leakage is occurring around the ends (edges) of the transistor, a parallel connection of many transistors of minimum width will emphasize edge leakage. If a closed geometry transistor (i.e., an edgeless layout, where the source, gate, and drain are arranged in an annular pattern as in sect. 4.10) of equivalent width is included, comparison of the post-irradiation performance of the two structures will provide a indication of the importance of edge leakage.

This example points out the importance of having a particular failure mechanism in mind when designing a test structure. It also indicates the need to consider the application of the structure in radiation testing and data reduction. By including two devices whose only difference is the number of edges, we can draw an unambiguous conclusion directly from the test results.

When the emphasis is on hardness evaluation, special consideration should be given to the location of the test structure on the test chip layout. Structures intended for testing in the same radiation environment should be placed together. Placement of bonding pads should be made to facilitate packaging all devices to be tested in one environment in the same package with a single set of pin assignments. This greatly simplifies the test effort at remote facilities and eliminates many sources of error. If possible, the radiation test engineers should be included in decisions related to device selection and location. Test plan development should be done in parallel with test chip design to ensure that test requirements are considered.

For those environments (e.g., total ionizing dose) in which the radiation effect is a strong function of the bias, several identical structures should be included on the test chip. This permits multiple bias conditions to be examined simultaneously during a single irradiation. The availability of several identical structures can result in significant savings in packaging costs, test facility time, and data analysis effort.

In many cases, simple test structures, macrocells, and more complex circuits may be included in the same section of the test chip. This permits a complete characterization from the transistor through the subcircuit level to be

made at the radiation facility without a change of test fixture. For example, ionizing dose rate tests typically are made on packaged parts at either a linear accelerator (LINAC) or flash x-ray (FXR) machine. If all photoresponse structures are grouped together, photocurrent measurements on diodes and upset measurements on macrocells and subcircuits can be made using the same package.

When emphasis is placed on determining design rules, consideration should be given to including test structures which are identical except for a critical dimension. Structures should contain dimensions which are nominal, incrementally larger, and incrementally smaller. In very new technologies or where failure mechanisms are incompletely understood, additional spacings may be required. Once design rules are determined, they should be made part of the automated design rule checking procedure employed by the manufacturer. Design rules which are not checked are not design rules at all.

Hardness assurance test structures are often derived from those found to be most sensitive to the failure mechanisms and process variations identified earlier in the development cycle. Emphasis should be placed on worst-case structures. Also, test structures with parameters which are directly related to circuit performance are particularly important. Hardness assurance devices may be placed directly on the die, on process monitors which are typically placed in each wafer quadrant, or in the saw kerf adjacent to the die. Their location depends on the degree of process uniformity over the wafer. With the increasing availability of x-ray sources for wafer irradiation, hardness assurance structures may be evaluated for post-irradiation performance at wafer probe [5–8]. Sufficient space must be allocated for these devices to ensure that adjacent microcircuits are not irradiated and that the test structures are not shadowed by the contact probes.

1.3 Summary

To assist the designer in locating descriptions of specific structures for a technology and radiation environment, all the devices discussed in this document are listed in Table 1, with an indication of their purpose, appropriate technologies, radiation environment, and location within the text. A review of the table will show that several structures address similar effects and environments. However, closer examination of the detailed description will reveal nuances in the application of each structure, which will help designers differentiate among radiation failure mechanisms.

Table 1. Summary of test chip structures.

	Name	Technology	Radiation environment	Reference section	Structure application
	(Chapter 3. Process Characterization Structures)				
1.	Crossbridges all inter-connects	MOS, Bipolar	Ionizing Dose, dose rate, neutrons	3.2	Resistivity and linewidth
2.	Van der Pauw all implants	MOS, Bipolar	Ionizing Dose, dose rate, neutrons	3.3	Resistivity
3.	Spreading resistance target	MOS, Bipolar	Ionizing Dose, dose rate, neutrons	3.4	Doping profiles
4.	Kelvin contacts	MOS, Bipolar	Dose rate, survivability	3.5	Parasitic resistance, burnout, and rail span collapse
5.	Via chains for all interconnect layers	MOS, Bipolar	Dose rate, survivability	3.6	Parasitic resistance, burnout, and rail span collapse
6.	Contact chains for all implants	MOS, Bipolar	Survivability	3.7	Parasitic resistance and burnout
7.	Electrothermal migration device	MOS, bipolar	Survivability	3.8	Rail span collapse and burnout
8.	Four-layer continuity device	MOS/SOS, MOS/SOI	Dose rate	3.9	Epi-thickness

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
			(Chapter 4. Gate Oxide Devices)		
9.	Transistors–variable length	MOS	Ionizing dose	4.2	Effective channel length
10.	Transistors–variable width	MOS	Ionizing dose	4.3	Effective channel width
11.	Transistors–charge pump (four terminal)	MOS	Ionizing dose	4.4	Measurement of interface states
12.	Transistor–nominal length/extra width	MOS	Ionizing dose	4.5	Radiation effects on transistor I/V characteristics with reduced edge and narrow channel effects
13.	Transistor–W/L = 10μm/10μm	MOS	Ionizing dose	4.6	Radiation effects on mobility with reduced short channel effects
14.	Transistor–nominal (multiple devices)	MOS	Ionizing dose	4.7	Radiation effects on typical I/V characteristics as a function of layout and bias conditions
15.	Transistors–orthogonal	MOS	Ionizing dose	4.8	Radiation effects on bilateral operation

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
			(Chapter 4. Gate Oxide Devices (cont'd))		
16.	Transistors–multi-edge	MOS	Ionizing dose	4.9 (see 4.5)	Enhanced radiation-induced edge leakage
17.	Transistors–edgeless	MOS/BLK MOS/SOS MOS/SOI	Ionizing dose	4.10	Separate subthreshold and back channel leakage from edge leakage
18.	Transistors–source/body ties	MOS/SOS MOS/SOI	Ionizing dose and dose rate	4.11	Eliminate kink effects and parasitic bipolar transistor photocurrent multiplication
19.	Capacitor–minimum aspect rati	MOS	Ionizing dose	4.12	Check oxide thickness and separate oxide trapped charge and interface states
20.	Capacitor–large aspect ratio	MOS	Ionizing dose	4.13	Minimize series resistance effects on measurements
			(Chapter 5. Field Oxide Devices)		
21.	Transistors–edgeless–poly gate	MOS	Ionizing dose	5.2	Check field inversion and leakage
22.	Transistors-edgeless–metal-1 gate	MOS	Ionizing dose	5.3	Check field inversion and leakage

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
	(Chapter 5. Field Oxide Devices (cont'd))				
23.	Transistors–2 edge-poly gate	MOS	Ionizing dose	5.4	Check field inversion, leakage, and design rules
24.	Capacitor–poly/silicon, minimum aspect ratio	MOS	Ionizing dose	5.5	Check field inversion and parasitic capacitance value
25.	Capacitor–poly/silicon, large aspect ratio	MOS	Ionizing dose	5.6	Check field inversion and parasitic capacitance value with minimum resistance effects on measurement
26.	Capacitor–metal-1/ silicon, minimum aspect ratio	MOS	Ionizing dose	5.7	Check field inversion and parasitic capacitance value
27.	Capacitor–metal-1/silicon, large aspect ratio	MOS	Ionizing dose	5.8	Check field inversion and parasitic capacitance with minimum resistance effects on measurement

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
			(Chapter 6. Interlevel Dielectric Devices)		
28.	Capacitors for interconnect levels minimum aspect ratio	MOS bipolar	Ionizing dose	6.2	Parameterize interlevel dielectric capacitance
29.	Fringing field capacitor, metal-1/ poly serpentine	MOS	Ionizing dose	6.3	Parameterize fringing field capacitance
			(Chapter 7. Trench Structures)		
30.	Trench FET w/double trench with and without gate	MOS Bipolar	Ionizing dose	7.2	Leakage current under trench
31.	Trench FET w/single trench with and without gate	MOS Bipolar	Ionizing dose	7.3	Leakage current under trench
32.	Trench array with and without gate	MOS Bipolar	Ionizing dose	7.4	Leakage current under trench

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
			(Chapter 8. SOI Structures)		
33.	Epi/oxide/ substrate capacitor	MOS Bipolar	Ionizing dose	8.2	Back channel threshold voltage shift
34.	SIM target	MOS Bipolar	Ionizing dose	8.3	Impurity content of oxide
			(Chapter 9. Radiation Sensitive Parasitic Devices)		
35.	Photodiode drain/substrate, unguarded, minimum aspect ratio	MOS	Dose rate	9.2	Primary photocurrent as a function of dose rate
36.	Photodiode drain/substrate, guarded, minimum aspect ratio	MOS	Dose rate	9.3	Primary photocurrent as a function of dose rate with restricted collection volume
37.	Photodiode drain/substrate, unguarded, large aspect ratio	MOS	Dose rate	9.4	Lateral collection volume for primary photocurrent
38.	Phototransistor drain/substrate/ well	MOS	Dose rate	9.5	Maximum secondary photocurrent

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
	(Chapter 9. Radiation Sensitive Parasitic Devices (cont'd))				
39.	Photodiode well/substrate, Unguarded, minimum aspect ratio	MOS	Dose rate	9.6	Primary photocurrent as a function of dose rate with unrestricted collection volume and secondary photocurrent from vertical parasitic transistor
40.	Photodiode well/substrate, Guarded, minimum aspect ratio	MOS	Dose rate	9.7	Primary photocurrent from vertical collection volume
41.	Photodiode well/substrate, Unguarded, large aspect ratio	MOS	Dose rate	9.8	Lateral collection volume for primary photocurrent
42.	Photoconductivity interdigitated, epi-to-epi	MOS/SOS MOS/SOI	Dose rate	9.9	Photoconductivity between epi islands through the substrate
43.	Photoconductivity interdigitated, poly-to-poly	MOS/SOS MOS/SOI	Dose rate	9.10	Photoconductivity between poly lines through the substrate
44.	Photoconductivity interdigitated, poly-to-epi	MOS/SOS MOS/SOI	Dose rate	9.11	Photoconductivity between poly lines and epi islands through the substrate

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
	(Chapter 9. Radiation Sensitive Parasitic Devices (cont'd))				
45.	MOS phototransistor	MOS	Dose rate	9.12	Secondary photocurrent in a parasitic bipolar transistor
46.	SCR path source/well/ substrate/ source maximum collection efficiency	MOS	Latchup	9.13	Holding voltage and current as a function of source-to-well and well-to-source spacing
47.	SCR path source/well/ substrate/ source maximum anode and cathode gate resistance	MOS	Latchup	9.14	Holding voltage and current as a function of well (contact) to latch path and substrate (contact) to latch path spacing
48.	Snapback structure	MOS	Snapback	9.15	Snapback holding voltage as a function of contact spacing
49.	Substrate spreading resistance	MOS	Latchup	9.17	Lateral spreading resistance as a function of contact dimensions and spacing
50.	Well spreading resistance	MOS Bipolar	Latchup	9.18	Spreading resistance as a function of contact dimensions and spacing

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
	(Chapter 9. Radiation Sensitive Parasitic Devices (cont'd))				
51.	Charge collection diode array	MOS Bipolar	SEU	9.19	Waveshape and amplitude for heavy ion strike and charge sharing among layers
	(Chapter 10. Bipolar transistors)				
52.	Transistor library samples	Bipolar	Ionizing dose, neutrons	10.2	Degraded transistor characteristics as a function of polarity and layout
53.	Transistor with nested emitter	Bipolar	Ionizing dose	10.3	Collector to emitter leakage
54.	Transistor with walled emitter	Bipolar	Ionizing dose	10.4	Collector to emitter leakage
55.	Transistors with base/ emitter contact swap	Bipolar	Ionizing dose	10.5	Degraded transistor characteristics as a function of polarity and layout
56.	Differential pair transistors with individual E/B/C terminals	Bipolar	Ionizing dose, Neutrons	10.6	Post-irradiation characteristic matching

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
			(Chapter 10. Bipolar transistors (cont'd))		
57.	Differential amplifier	Bipolar	Ionizing dose, neutrons	10.7	Post-irradiation offset
			(Chapter 11. Bipolar Diodes)		
58.	Diode connected transistors	Bipolar	Ionizing dose, neutrons	11.2	Post-irradiation characteristics
59.	Buried Zener	Bipolar	Ionizing dose, neutrons	11.3	Change in zener voltage
60.	Schottky without guard ring	Bipolar	Ionizing dose, dose rate	11.4	Post-irradiation characteristics
61.	Schottky with guard ring	Bipolar	Ionizing dose, dose rate	11.5	Post-irradiation characteristics
62.	Photodiode, buried layer/ substrate, no guard band, minimum aspect ratio	Bipolar	Dose rate	11.6	Primary photocurrent with unrestricted collection volume
63.	Photodiode, buried layer/ substrate, no guard band, large aspect ratio	Bipolar	Dose rate	11.7	Lateral photocurrent collection volume

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
	(Chapter 11. Bipolar diodes (cont'd))				
64.	Photodiode buried layer/ substrate with guard band of minimum width and spacing	Bipolar	Dose rate	11.8	Restricted lateral collection volume and secondary photocurrent
65.	Photodiode collector/ substrate with large width and and minimum spacing	Bipolar	Dose rate	11.9	Restricted lateral collection volume and secondary photocurrent
66.	Photodiode buried layer/ substrate with surrounding substrate contact	Bipolar	Dose rate	11.10	Restricted lateral collection volume
67.	Photodiode base/collector with minimum aspect ratio	Bipolar	Dose rate	11.11	Collector/base primary photocurrent
68.	Phototransistor with typical aspect ratio	Bipolar	Dose rate	11.12	Secondary photocurrent

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
	(Chapter 12. Multi-Device Structures)				
69.	Four-layer path in shared isolation tub	Bipolar	Latchup	12.2	Latch path within a shared isolation tub
70.	Schottky diode sharing buried layer with transistor	Bipolar	Latchup	12.3	Latch path within a shared buried layer
71.	Adjacent transistors in separate buried layer tubs	Bipolar	Latchup	12.4	Substrate latch path
72.	Adjacent transistor and resistor in separate buried layer tubs	Bipolar	Latchup	12.5	Substrate latch path
73.	Field oxide FET with adjacent buried layers for source and drain	Bipolar	Ionizing dose	12.6	Leakage current
74.	Annular field oxide FET with metal-1 gate	Bipolar	Ionizing dose	12.7	Leakage current
75.	Gated diode	Bipolar	Ionizing dose	12.8	Surface leakage

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
			(Chapter 13. Resistors)		
76.	Maximum resistivity resistor with field plate	Bipolar	Ionizing dose	13.2	Resistivity change
77.	Resistor without tub resistor tie	Bipolar	Dose rate	13.3	Effective resistance change
78.	Resistor with tub resistor tie	Bipolar	Dose rate	13.4	Effective resistance change
79.	Pinched resistor	Bipolar	Neutrons	13.5	Base width and doping monitor
			(Chapter 14. Macrocells)		
80.	Inverter NAND/NOR delay chains and ring oscillators	MOS Bipolar	Ionizing dose, neutrons	14.2	Propagation delay degradation
81.	Key subcircuit functions	MOS bipolar	Ionizing dose, neutrons	14.3	Performance degradation
82.	Standard gate design for technology	MOS Bipolar	Ionizing dose, neutrons	14.4	Performance degradation

Table 1. (cont'd)

	Name	Technology	Radiation environment	Reference section	Structure application
			(Chapter 14. Macrocells (cont'd))		
83.	*Shift* registers	MOS Bipolar	SEU, ionizing dose, dose rate, neutrons	14.5	Upset threshold and clocking frequency reduction
84.	RAM section	MOS Bipolar	SEU, ionizing dose, dose rate, neutrons	14.6	Upset threshold, leakage access time degradation
85.	NAND/NOR gate	MOS Bipolar	Ionizing dose, dose rate neutrons	14.7	Noise margin and transient upset
86.	Input protection circuits	MOS Bipolar	Electrical overstress, dose rate, survivability, ionizing dose	14.8	Photoresponse and burnout characteristics
87.	Minimum gate into a latch	MOS Bipolar	Dose rate, SEU	14.9	Transient upset and SEU propagation in combinational logic
88.	Large combinational macro	MOS Bipolar	Ionizing Dose, dose rate survivability, neutrons	14.10	Transient upset, speed degradation, burnout

Although the list of test structures is extensive, it is not exhaustive. Designers should use the structures discussed here as a starting point and modify them to be appropriate to their specific technology. Emphasis should be placed on the purpose of each test structure in identifying potential failure mechanisms. Modifications to the structure design for a particular technology are always appropriate so long as the final device achieves its purpose.

As a result of two conferences, the availability of reference information on test structures and test chip designs has improved greatly over the last five years. The IEEE International Conference on Microelectronic Test Structures publishes proceedings, which are an extremely valuable source of information on structures, measurement procedures, and application of results [9–12]. The papers are primarily oriented toward commercial technologies. Since 1986, the Defense Nuclear Agency and the U. S. Army Harry Diamond Laboratories (HDL) have been sponsoring a Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance. The summaries of these workshops are available as special reports [13–15]. The reader is encouraged to refer to these publications for detailed design and application information.

2. FLOOR PLAN DESIGN

2.1 Introduction

The planning and design of the floor plan of the test chip are critical steps in achieving a tool which can be used successfully for developing radiation-hardened processes and circuits. The arrangement of the test structures on the die, the location and dimensions of probe/bonding pads, and the grouping of related test structures into sections will have a major impact on the test chip's success. As in all designs, the test chip will represent a compromise between competing motivations. It will also be constrained by limitations in available resources and schedule requirements. However, resources spent in the planning stage will result in reduced testing effort, better test results, clearer understanding of radiation failure mechanisms, and fewer redesigns.

Perhaps the two most strongly competing motivations are

1. the desire to include every conceivable test structure; and
2. the desire to include only those structures which are most likely to be tested.

Placing too many structures on a chip wastes design and layout time and expands the die size. They may also make the test effort too ambitious if the test team attempts to make measurements on every structure. However, most test chips include contingency structures which are not intended for routine testing. They are included to yield valuable insight into the cause of an unexpected radiation response. The contingency structures are typically simple devices for determining process characteristics and basic radiation parameters. They include crossbridge and van der Pauw structures, individual transistors and diodes, and simple macrocells (gates and delay chains). Often these structures are placed on the interior of the test chip section and are accessible only by probing or special bonding patterns. Each design team will have to determine the tradeoff between excessive numbers of structures and an adequate number to cover contingencies. In making that decision, the design team should carefully consider the purpose of the test chip and should involve the test engineer and other interested parties.

2.2 Packaging Considerations

Test chips for radiation effects investigations are most often designed in sections. With packaging, these devices to be tested in the same radiation environment are grouped together. Most radiation effects testing requires that the device be packaged for mechanical support, for protection in transport to the test facility, and for electrical connection to the part during and after the test. Therefore, sections of the test chip are typically arranged so that they can be scribed and bonded separately.

Packages used for radiation testing should be as simple as possible. Many test fixtures available at the test facilities or from government laboratories are based on 40-pin dual-in-line packages (DIP's). These packages are readily available in ceramic and can accommodate die up to 250 mils square. Ceramic packages are important because they contribute very little dose enhancement, and their lids can be easily removed. Often lids of packaged test chips are taped on rather than being soldered down. This permits easy removal for environments in which testing is done on unlidded devices. This feature also facilitates visual inspection and probing if necessary for post-irradiation diagnostics.

The pin constraints and the well size of the package selected may provide good guidelines for choosing the dimensions of the test chip sections. Consideration should be given to the bonding diagram for the packaged test samples

when the floor plan is designed. Devices which will be tested simultaneously must be placed together and have appropriate bond pad arrangements. Although a 40-pin DIP is mentioned above, other package types may be chosen. However, selection of overly complex or expensive packages should be avoided if at all possible.

2.3 *Floor Plans*

Figure 1 is a diagram of a test chip floor plan divided into quadrants. Each quadrant may be scribed and packaged independently. Moreover, each quadrant contains structures which are primarily intended for a particular type of test or radiation environment. Quadrant 1 has devices intended for process control, model parameterization, and total dose characterization at probe using an x-ray source. Quadrant 2 contains simple devices and macrocells intended for Co-60 total dose testing and neutron irradiation. Quadrant 3 contains simple devices and macrocells intended for dose rate and latchup testing. Quadrant 4 contains simple structures and a large macrocell for single event upset (SEU) testing or more complete characterization in the other environments.

Each quadrant will probably be bond pad limited. There are several schemes which have been devised for increasing the number of pads. For several years, NIST has advocated a 2×N array of pads, as shown in figure 2 [16]. Values of N typically range from 8 to 16. This type of arrangement is most useful for contacting process characterization structures during probe. A simple probe card can be fabricated to contact these pads, and electrical testing can proceed quite rapidly. NIST test chips typically use 80 μm probe pads on 160 μm centers for the array. Buehler et. al. [17] have identified two additional placements (i.e., 94 μm pads on 144 μm centers within a row with 184 μm spacings between rows and 75 μm pads on 100 μm centers within a row with 154 μm centers between rows) that are relatively common throughout the semiconductor industry. If the pads will only be probed, 50 to 75 μm (2 to 3 mil) square pads are usually adequate. If there is a chance that devices will be bonded out, 75 to 100 μm (3 to 4 mil) pads should be used.

Care should be exercised in assigning terminals to bond pads in 2×N layouts. For commercial technologies the tendency in test chips is to tie all sources to a common bond pad and all gates to a single bond pad for a given polarity of transistor (e.g., NMOS). Individual pads are then assigned for the drains. While this arrangement gives an efficient allocation of the pads for normal electrical characterization, it precludes providing a variety of bias conditions for irradiation. Therefore, in a radiation effects test chip, the preferred design assigns each transistor terminal to its own pad.

For radiation effects test chips, there are two additional considerations for the use of a 2×N scheme. First, many manufacturers and government laboratories use a low-energy x-ray tester to perform total dose testing on devices during probing. Since the x-ray beam can be blocked or scattered by the probes, the test structures should be placed in the center between the two columns of pads. Second, there may be instances when devices from the process control section are selected for packaging. Bonding to a 2×N array can be quite difficult because the pads are so close together, and there is a tendency for a test structure to use pads from both columns. The layout designer can make packaging easier by identifying these structures that are most likely to be of interest. Then the arrays containing those structures can be placed around the periphery of the section. The pads used for the high-interest structures can be restricted to the outside column so that bond wires will not have to cross over to the inside column.

Another scheme for increasing the number of available bond pads is to use concentric rings. Structures which will be tested at

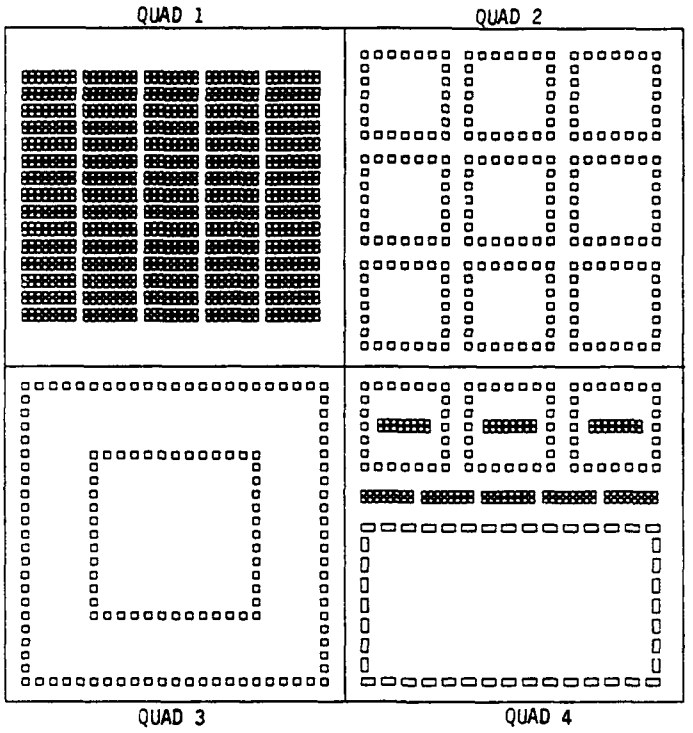


Figure 1. Floor plan of a test chip organized into four quadrants.

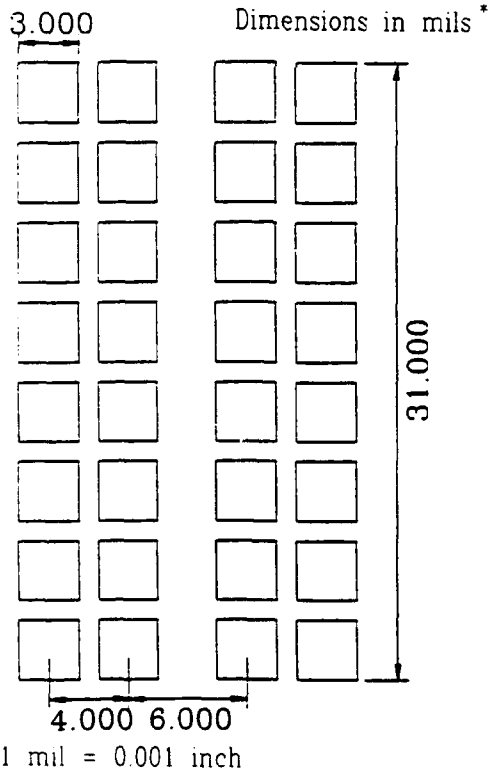


Figure 2. Probe pad placement for test structures organized in a 2×N pattern.

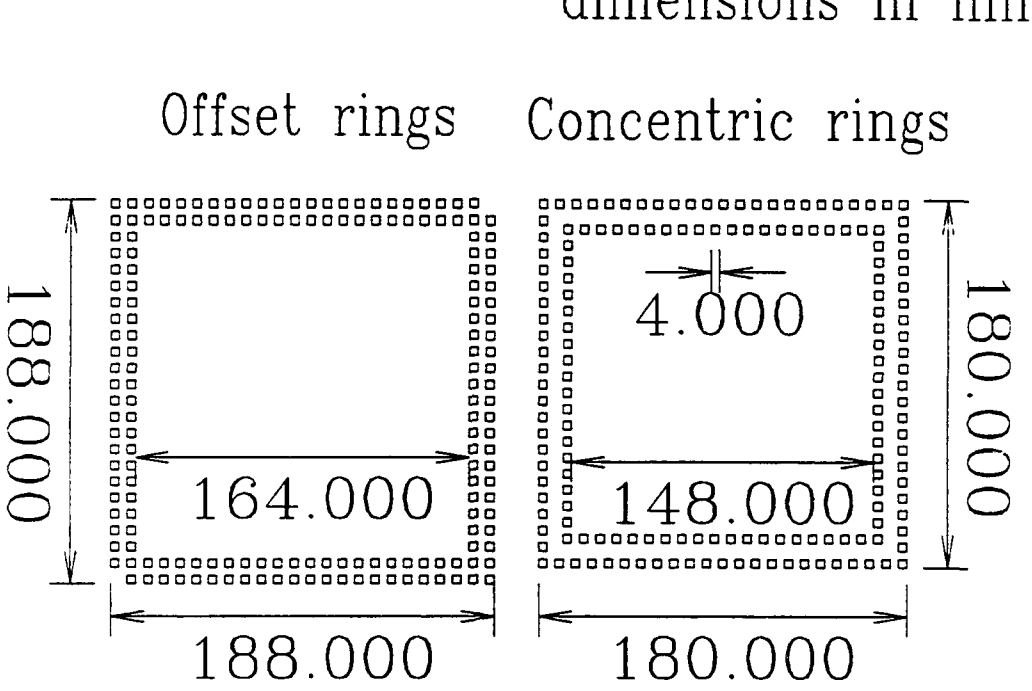


Figure 3. Test chip layout illustrating use of concentric rings of bond pads.

the same time should all be tied to pads from the same ring. A few of the variations on this approach are shown in figure 3. In these two approaches, the concentric rings are quite close together, and long metallization runs may be required to connect structures with their bonding pads. This is particularly true if the structure is placed in the center of the die. If the technology or structure is particularly sensitive to capacitive loading, the designer should be careful in the placement of individual structures.

The inner ring of bond pads can be made smaller, as shown in figure 4. This will reduce the metallization run between the device and its bonding pad. However, the number of pads in the inner ring is substantially reduced. In some cases, contingency structures may be placed in the center of the die and connected to probe pads. These structures would not be bonded out to package leads, but they would be available for probe testing if necessary. This approach is most appropriate for process monitor structures such as cross bridges and van der Pauw devices. Active devices, such as transistors, would be of limited use because they could not be biased during irradiation.

Finally, bonding pads can be arranged around the periphery of individual circuits on the die as shown in figure 5. This is most effective on sections containing large macrocells. Pads are placed as they would be if the macro were being laid out for production. The macros are then combined in a mosaic on a single section of the test chip. In some cases, the designer may wish to leave additional space between the macros so that they can be scribed and packaged individually. This may be desirable if the performance of the macro is particularly sensitive to package parasitics.

Even with the pad placement alternatives discussed above, the test chip designer may still find that he is pad limited. Recently, several authors have discussed multiplexing schemes to

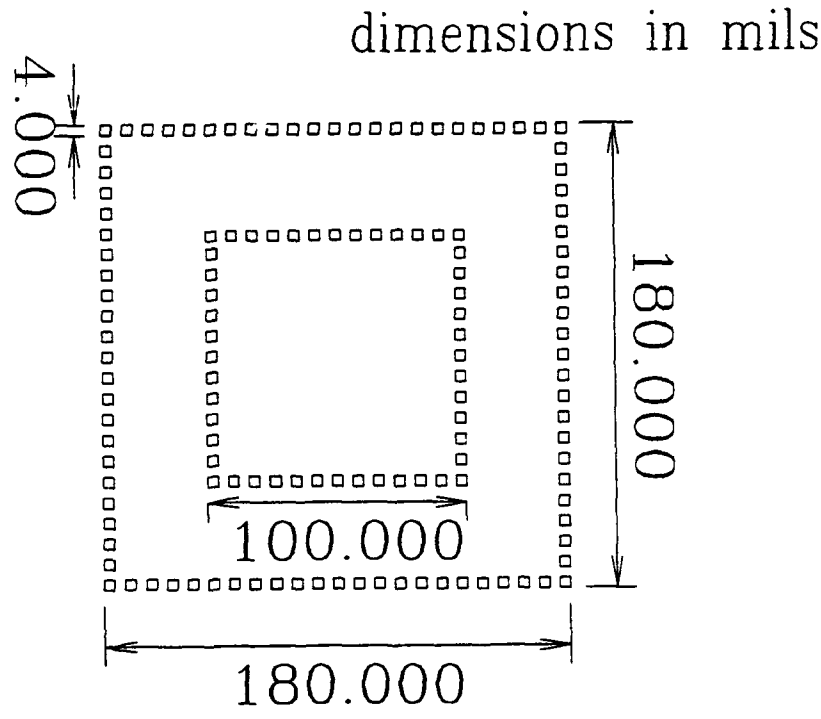


Figure 4. Test chip layout illustrating interior probe pads for process monitor structures associated with macrocell test structures.

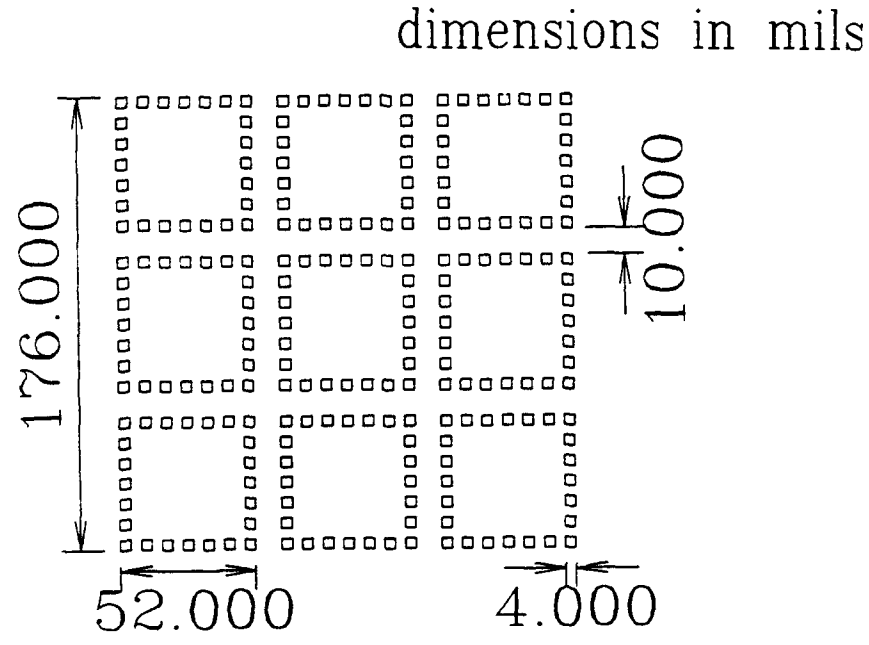


Figure 5. Bond pad arrangement for individually packageable macrocell on a test chip.

expand the number of devices accessible [18–(21]. Caution must be used in applying multiplexing approaches to radiation effects test chips, because the characteristics of the active elements in the multiplexer will change as a function of radiation. In x-ray irradiations at the wafer level, the beam can be collimated, and the multiplexer can be laid out so that it is shielded from the beam. In such cases, a multiplexing scheme can be an effective way to access several test structures through a few pads. Test chips containing a large number of macrocells are good candidates for multiplexing.

Designers who are developing their first test chip may find a review of previous test chips to be beneficial in providing ideas for floor planning and general design approach. Several test chips have been documented and can serve as examples of designs for both process monitors and radiation-sensitive test structures [22–28].

2.4 Metallization

The designer should pay close attention to the metallization pattern used to connect the test structures to their bonding pads. If the runs are too long, the extra capacitance may affect the results of measurements. If the metal is too narrow or there are too few vias and contacts, the yield may be impaired. In general, large numbers of vias and contacts should be employed, and metal widths significantly greater than minimum design rules should be employed, if there are no contrary considerations.

Consideration should also be given to using second-level metal for interconnects between the pad and the test structure. In some technologies, there is a possibility of inverting the silicon surface as a result of trapped charge in field oxides. This charge trapping may be enhanced by bias on metallization runs. In some structures, such as field oxide transistors, the effect of the parasitics under the interconnect metal may invalidate the measurement on the intended structure. The effect can be reduced or eliminated by making the interconnect on second-level metal. The addition of the interlevel dielectric decreases the field in the oxide.

In technologies built in silicon substrates, attention must be given substrate contacts. Control of the substrate bias is often crucial in making accurate measurements on both MOS and bipolar devices. Although provisions should be made for backside contact to the substrate in packaged devices, topside contacts are also important for probe measurements. The designer should not rely on a single contact to a well, tub, or isolation region. Instead substrate contacts should be made as close as possible to the test structure. Metallization runs should be made directly to the substrate contact.

3. PROCESS CHARACTERIZATION STRUCTURES

3.1 Introduction

There are many excellent characterization structures which are useful in developing and monitoring an advanced microcircuit process. Several are documented in publications by the NIST and are described in the Proceedings of the IEEE Conference on Test Structures. The reader is referred to those documents for a complete treatment of process characterization and photolithographic control devices. This chapter discusses the subset of process characterization structures which are particularly useful in the development of radiation hardened technologies.

3.2 Crossbridge Structures

3.2.1 Purpose

The crossbridge structure shown in figure 6 is used to determine both sheet resistance and line width.

3.2.2 Description

The crossbridge structure is a six-terminal device which incorporates a van der Pauw device (for sheet resistance determination) and a minimum line-width resistor. By knowing the design dimensions for length, the designer may determine the line width of the device. The crossbridge is used extensively in process characterization and control for commercial as well as radiation-hardened technologies. There is an extensive list of references which the designer should consult for information on design, measurement, and data analysis [39–45].

3.2.3 Special Design Considerations

In large test chips, crossbridge structures should be included for all interconnect levels and for all implants with critical dimensions. For smaller test chips or hardness assurance kerf structures, only levels which are particularly important for radiation hardness may be used.

3.2.4 Application

The crossbridge is particularly useful for evaluating polysilicon material used for gates or high-resistivity polysilicon used for cross-coupled resistor in SEU hardening schemes. Both the resistivity and the line width of polysilicon can be important contributors to device hardness even though they are not directly affected by radiation. The resistivity of the polysilicon is an important contributor to the RC time constants associated with propagation of a signal through the circuit. This is particularly the case in technologies in which polysilicon is used for a partial interconnect layer. The line width of the polysilicon directly determines the gate channel length in self-aligned MOS technologies. If the polysilicon is underetched (i.e., wider than targeted) the width-to-length ratio, and consequently the drive of the transistor, will be reduced. Additional drive reduction from total dose irradiation may result in excessive propagation delays and failure due to race conditions. If the polysilicon is overetched (i.e., narrower than targeted), hot electron effects may become more important, and the reliability of the device may be reduced.

The resistivity and dimensions of other interconnect and implant layers may be similarly important in a radiation environment. The resistivity of metallization layers will directly impact rail span collapse problems (i.e., excessive voltage drops in the bus metallization due to photocurrents experienced in a dose rate environment). It is also a direct factor in determining heating of the metallization and potential burnout in extremely high dose rate, survivability environments.

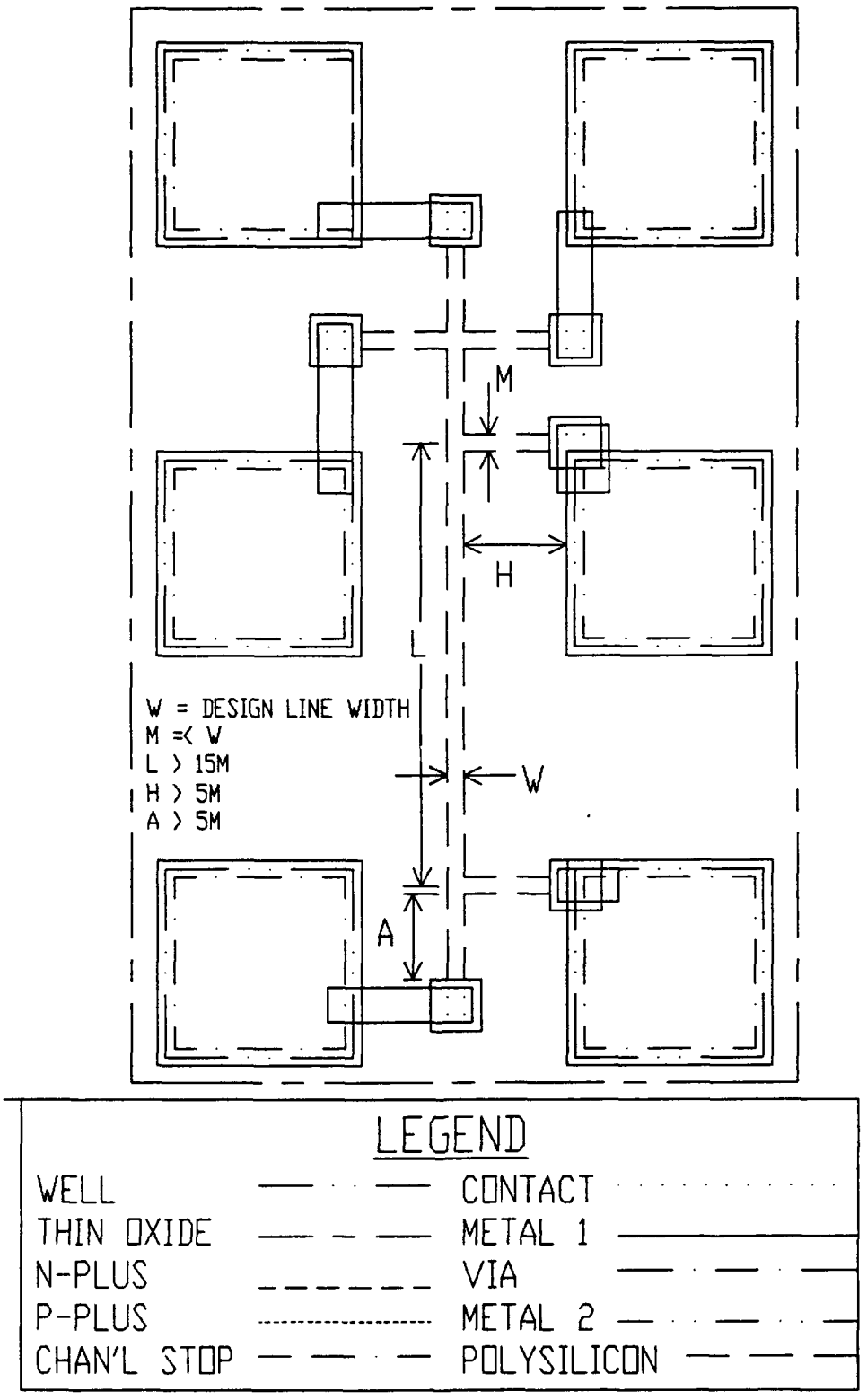


Figure 6. Crossbridge test structure.

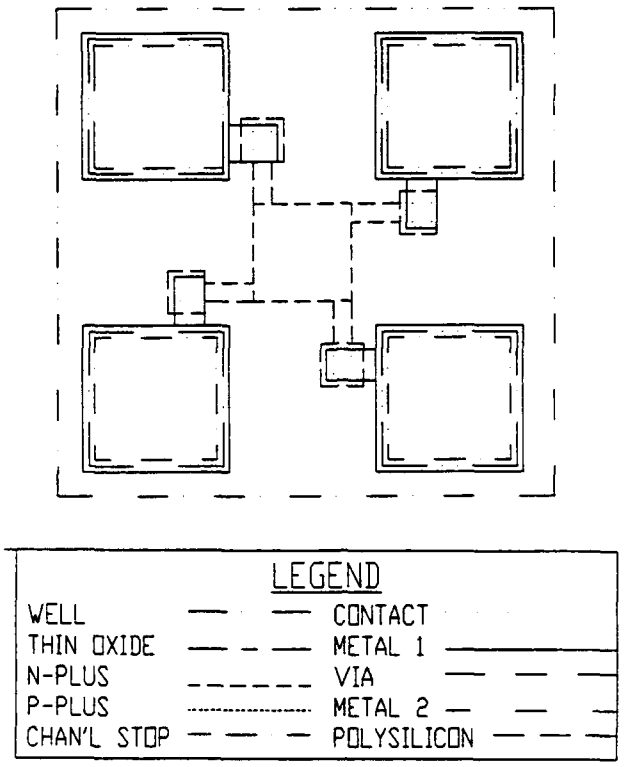


Figure 7. van der Pauw test structure.

3.3 van der Pauw Structures

3.3.1 Purpose

The van der Pauw structure (shown in figure 7) which is used to determine sheet resistance, is one of the most widely used process monitoring structures in the semiconductor industry. Applications of the data from van der Pauw devices are well documented by NIST [46–47].

3.3.2 Description

The van der Pauw structure most commonly used is a four terminal device with two terminals used to force current through the measured area and two terminals used to sense the voltage. The measured area is typically square.

3.3.3 Special Design Considerations

van der Pauw structures should be included for each diffusion or implant used in the process.

3.3.4 Application

Doping concentrations as reflected in the sheet resistances have a direct impact on device performance and radiation hardness. The doping determines:

1. The surface potential required for inversion at silicon/silicon-dioxide interfaces;
2. The dimensions of depletion layer widths and hence prompt photocurrent values;
3. The gain of parasitic bipolar transistors which participate in latchup paths, and many other critical radiation effects parameters.

The van der Pauw structure provides a simple measurement of a parameter directly related to doping concentration. It is useful in both process monitoring portions of large test chips and as a contingency structure on sections containing devices for radiation testing.

3.4 Spreading Resistance Target

3.4.1 Purpose

The spreading resistance target, as shown in figure 8, is used to provide a large area which can be angle lapped and used for spreading resistance measurements to determine doping profiles. Considerable care must be taken in the interpretation of data from spreading resistance measurements. Review of the literature associated with this profiling procedure is highly advised [49–51].

3.4.2 Description

The spreading resistance target is typically a square structure at least 50 μm on a side which contains all the implants used to construct devices in the technology. The vertical structure of the device should be consistent with the device being fabricated. For example, in an n-well CMOS technology, a target should be included for the drain/well/epi/substrate structure required to make a p-channel transistor, as well as a drain/epi/substrate structure required to make an n-channel transistor. The structures should include all threshold adjust, guard band, and channel stop implants.

3.4.3 Special Design Considerations

Since it must be angle lapped for a spreading resistance measurement to be made, the structure should be placed close to the edge of the die. Usually a minimum of 20 μm is required to make a good spreading resistance measurement, and it is most economical if passes through different layers can be made on the same bevel. Therefore, the dimensions of the structure should be adjusted to make room for each set of measurements required. Designers should consult their process characterization department to determine the dimensions required for ensuring good measurement values.

3.4.4 Applications

As noted in the discussion on van der Pauw devices, doping concentration plays a major role in determining device performance and radiation hardness. Spreading resistance measurements provide one of the most commonly used methods for determining the actual doping profiles produced by the process. These profiles are also required for device physics simulation of photoresponse, latchup, SEU waveforms, and other radiation effects.

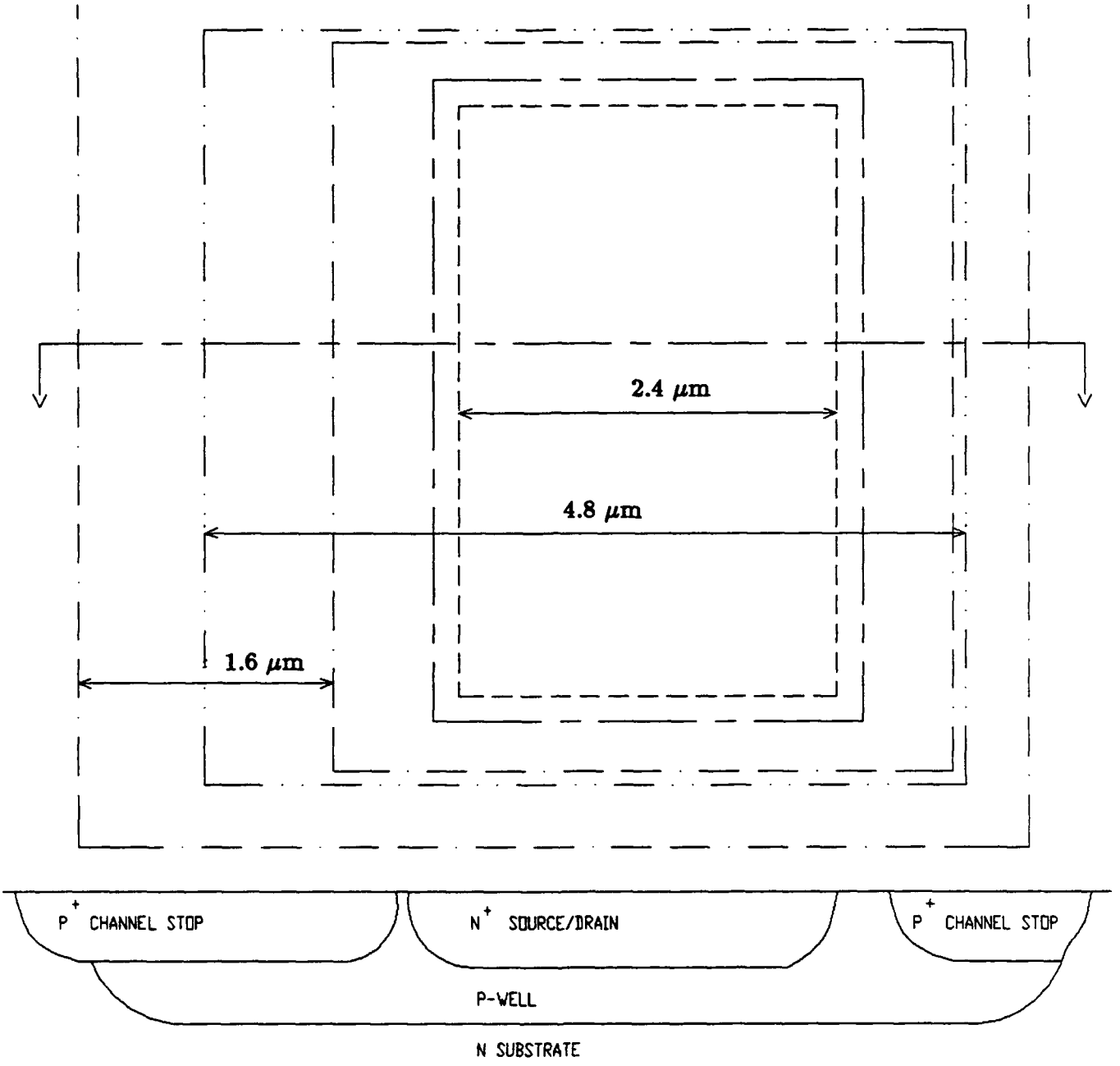
3.5 Kelvin Contacts

3.5.1 Purpose

Kelvin contact structures (as shown in fig. 9) are used to determine the resistance of vias and contacts. Contact and via resistance problems are often major yield limiters in modern microcircuit technologies. Therefore, Kelvin contact structures, together with via and contact chains (sect. 3.7 and 3.8) are universally included in process development and yield analysis test chips [52–58].

3.5.2 Description

The Kelvin contact structure is a four-terminal device in which two terminals are used to force current from one layer to another through a via or contact opening. The other two terminals are used to monitor the voltage across the via or contact.



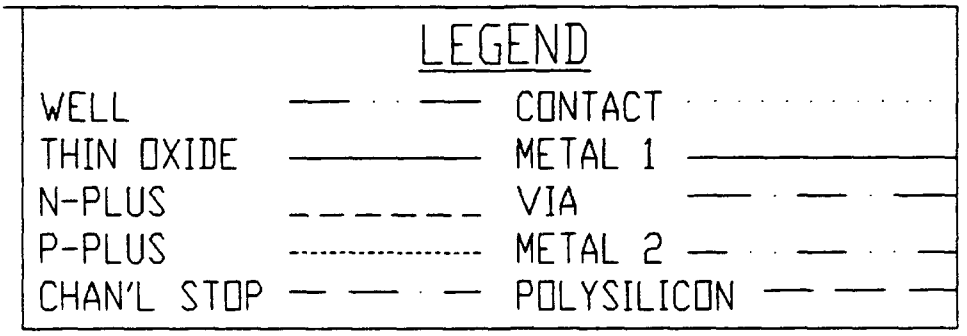


Figure 8. Spreading resistance target.

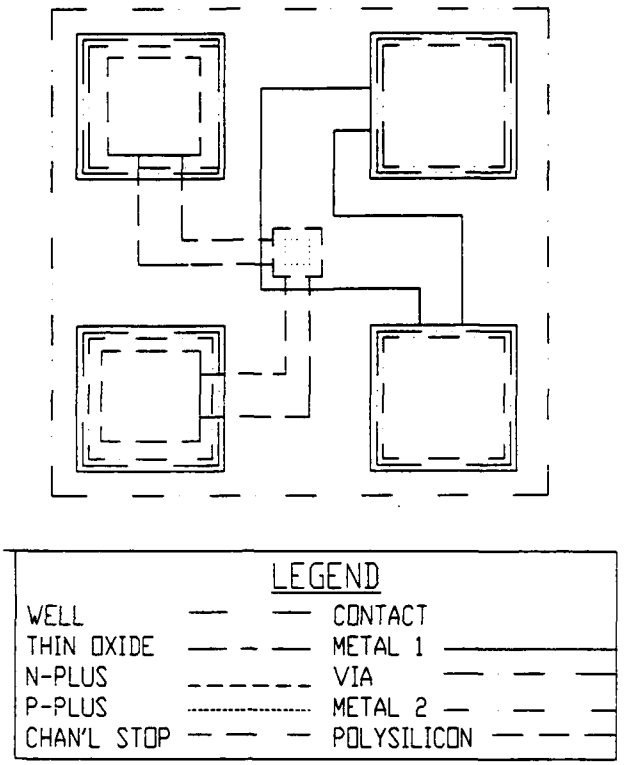


Figure 9. Kelvin contact test structure.

3.5.3 Special Design Considerations

The via and contact resistance are a function of the dimensions of the via or contact. If different dimensions for the via/contact opening are allowed in the design rules, structures for each dimension should be included.

3.5.4 Applications

Via/contact resistance can add significantly to the RC time constants in some propagation paths. Also, poor metal coverage in vias/contacts may result in reduced burnout thresholds in high-dose-rate survivability environments. Kelvin contacts offer a convenient method for monitoring via/contact resistance in both hardened process development and hardness assurance for established processes.

3.6 Via Chains for Interconnects

3.6.1 Purpose

Via chains as shown in figure 10 are used to monitor the integrity of metallization/interconnect systems.

3.6.2 Description

The via chain is a daisy chain interconnect of two different levels of metallization or metal and polysilicon. The levels are connected by vias. The distance between vias is typically determined by minimum design rules.

3.6.3 Special Design Considerations

Contacts to the via chains should be brought out to bond pads at intervals of 200 to 500 contacts. Typical chain dimensions are at

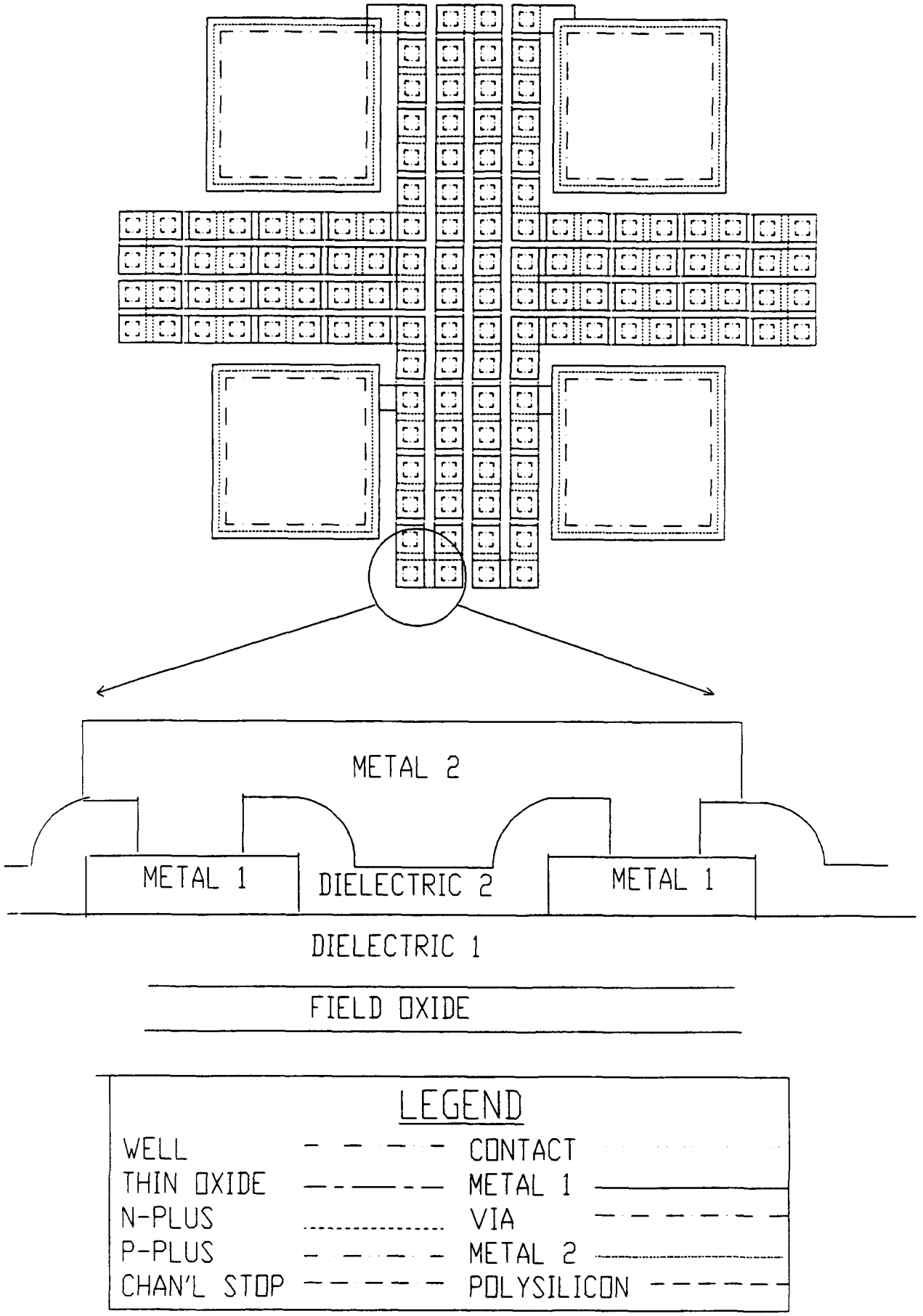


Figure 10. Via chain test structure.

least 1000 contacts. Bringing out intermediate pad contacts permits the chain to be used even if the entire structure does not yield.

3.6.4 Applications

Metallization system integrity is of primary importance for survivability in very high dose rate environments. The resistance of the via/metal system is important for treating rail span collapse. The via chain is a convenient structure for determining the current density required for burnout for the metallization system in hardened process development. It is also useful for monitoring metallization system resistance variations for hardness assurance.

3.7 Contact Chains

3.7.1 Purpose

Contact chains as shown in figure 11 are used to monitor the integrity and resistance of contacts between interconnect layers and silicon implant regions.

3.7.2 Description

The contact chain is a daisy chain interconnect of a conductor level (metal or polysilicon) and an implant layer (e.g., source/drain region). The levels are connected by contacts. The distance between contacts is typically determined by minimum design rules.

3.7.3 Special Design Considerations

Contacts to the contact chains should be brought out to bond pads at intervals of 200 to 500 contacts. Typical chain dimensions are at least 1000 contacts. Bringing out intermediate pad contacts permits the chain to be used even if the entire structure does not yield.

3.7.4 Applications

Metallization/contact system integrity is of primary importance for survivability in very high dose rate environments. The resistance of the contact/metal system can also be important for determining propagation delay. The contact chain is a convenient structure for determining the current density required for burnout for the metallization/contact system in hardened process development. It is also useful for monitoring metallization/contact system resistance variations for hardness assurance.

3.8 Electrothermal Migration Device

3.8.1 Purpose

The electrothermal migration device, as shown in figure 12, is typically used to investigate reliability issues related to electrothermal migration in the metallization system. For radiation effects, the structure is useful in determining the short pulse burnout characteristics of the metallization. Care must be taken in performing testing on these devices for metallization quality studies. The designer should carefully review the literature on the application of these devices [59–61].

3.8.2 Description

The electrothermal migration device is a minimum line-width metallization run in a serpentine pattern. It is typically run over an orthogonal pattern of other structures to yield a topography of maximum roughness. Each metallization layer is brought out to pads so that current can be driven through the pattern.

3.8.3 Special Design Considerations

The electrothermal migration structure should be used in conjunction with

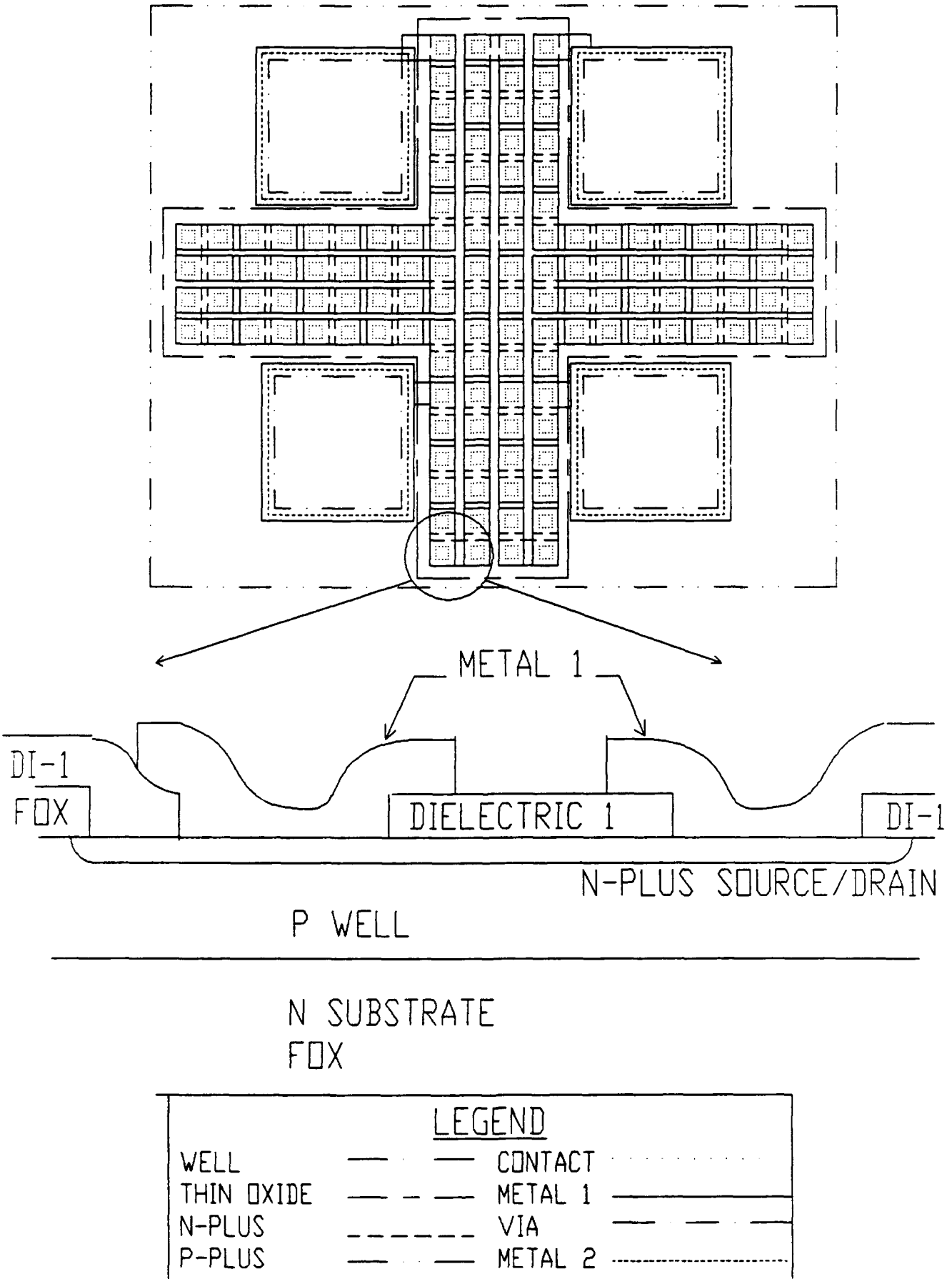


Figure 11. Contact chain test structure.

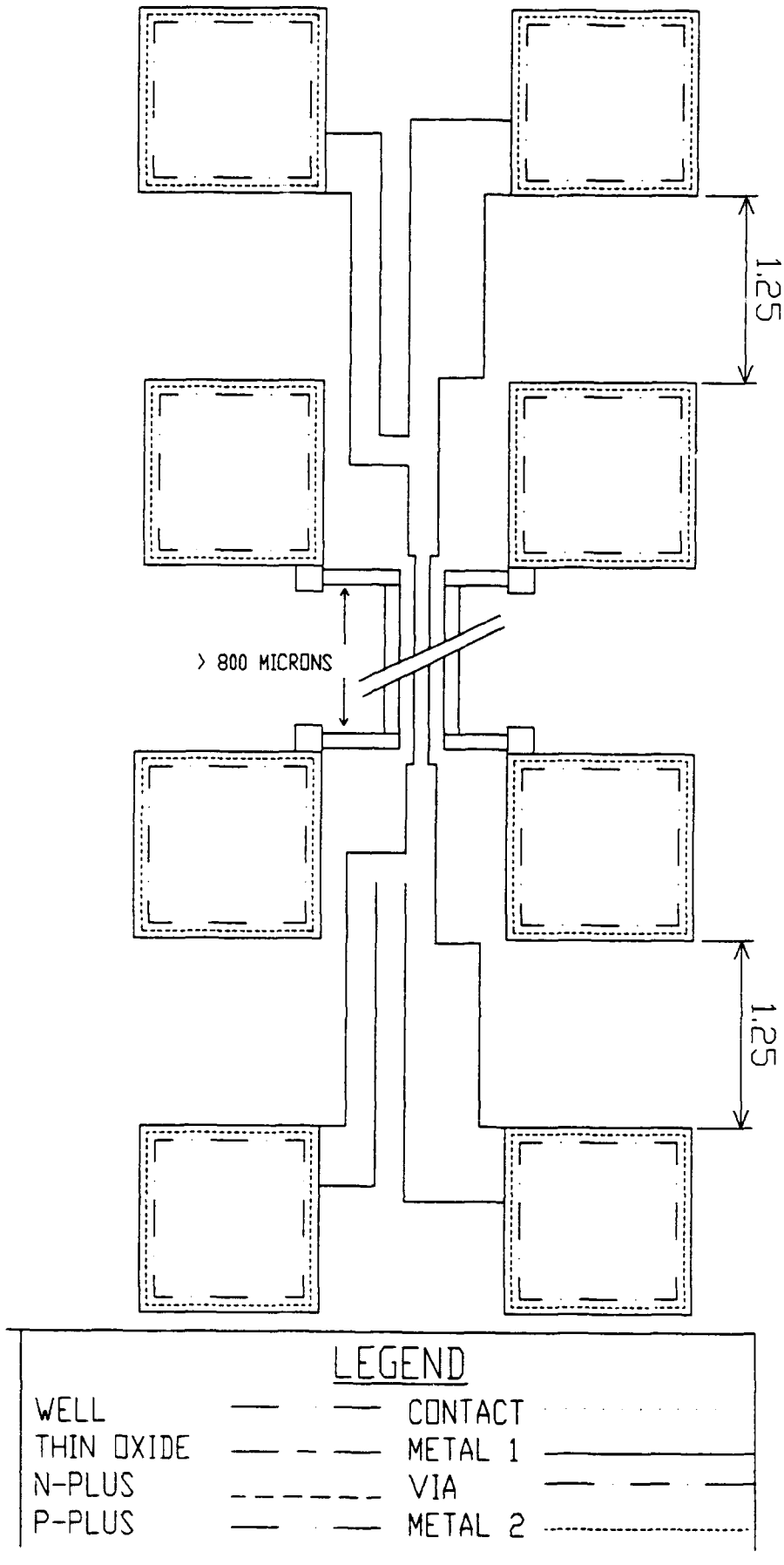


Figure 12. Electrothermal migration test structure.

via/contact chains. By comparing the failure location and failure current density in both structures, the engineer can determine if burnout is determined by the basic metallization or the vias. If the line width design rule for metallization containing vias is larger than minimum line width metal, the electrothermal migration structure should have the same width as the via/contact chain.

3.8.4 *Applications*

For pulsed burnout testing, the electrothermal migration structures are typically driven with a constant impedance pulser (e.g., 50 ohms). The voltage across the device is monitored with a high-impedance voltage probe. The current can be monitored with a current probe or a current viewing resistor. Pulse rise time should be in the range from 1 to 10 ns with durations of 50 to 100 ns.

3.9 *Four-Layer Continuity Device*

3.9.1 *Purpose*

The four-layer continuity device, as shown in figure 13 is used in silicon-on-sapphire (SOS) and silicon-on-insulator (SOI) technologies to determine if the source drain implants have been driven all the way to the silicon/insulator interface [62].

3.9.2 *Description*

The four-layer continuity device is an epi island with alternating n-plus and p-plus source/drain implant sections. If continuity can be detected between the source drain regions with the same polarity as the epi, the source/drain implants have not been driven all the way to the silicon/insulator interface.

3.9.3 *Special Design Considerations*

A structure must be included for each polarity of the epi island.

3.9.4 *Applications*

If continuity can be established in the structure, then either the epi island is too thick or the implant energies have not been set correctly. If the epi island is too thick, then retrograde doping in the island to control back channel leakage may be ineffective. If the source/drain implants are too shallow, additional photocurrent will be collected from under the source/drain region. Also, the drain capacitance will be larger and result in slower propagation delay times.

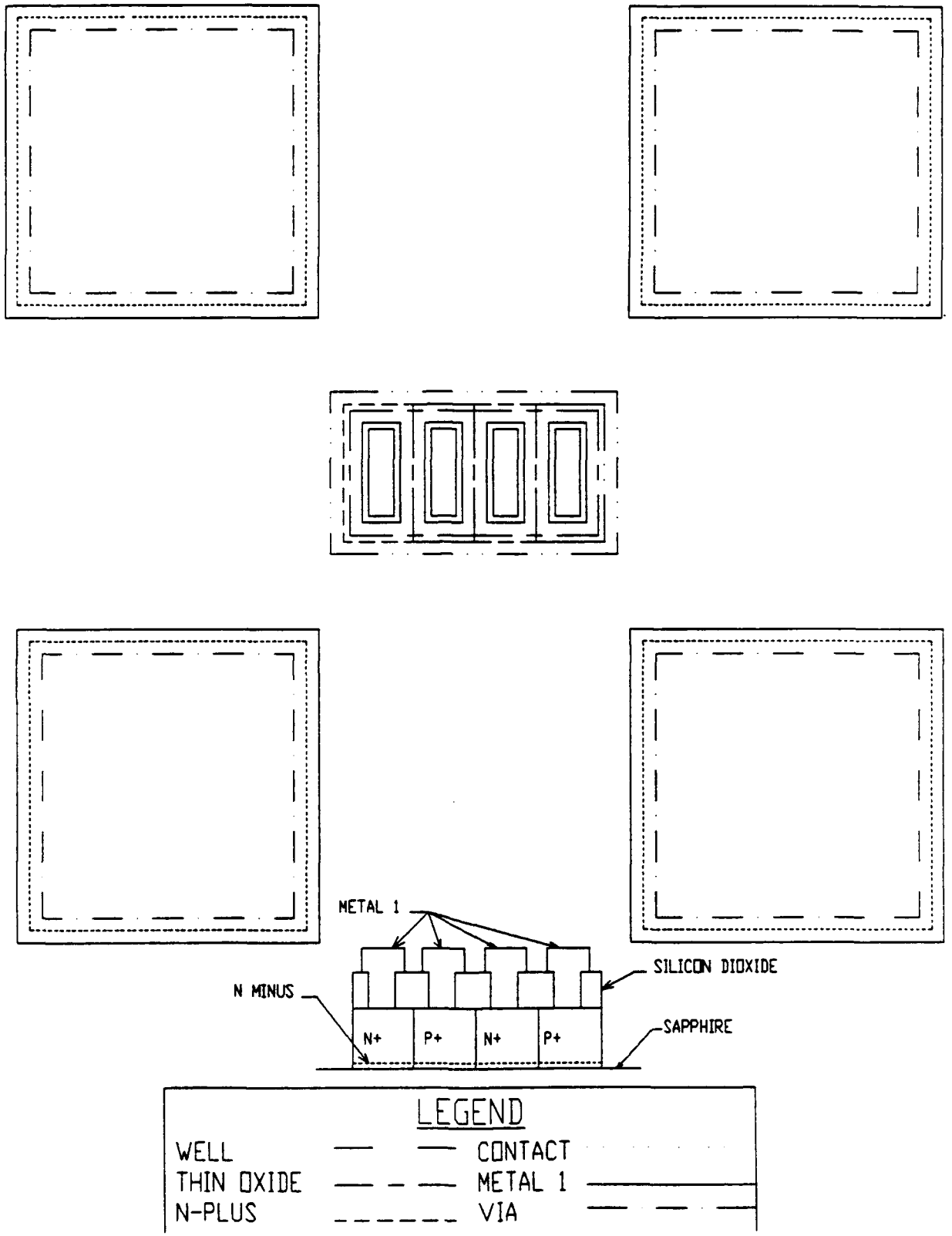


Figure 13. Four-layer continuity test structure.

4. GATE OXIDE DEVICES

4.1 Introduction

The test structures described in this section are directed toward gate oxide hardness in MOS technologies. In several cases, variations in width or length have been indicated. For the examples, a 2 μm CMOS technology has been assumed. The nominal device has been assumed to be 10 μm wide for the N-channel and 15 μm for the P-channel. The designer should substitute the width and length values appropriate for his technology.

The gate oxide test structures have been selected to permit determination of threshold voltage shift, mobility degradation, and leakage current as a function of total ionizing dose. In most cases, threshold voltage shift should be separated into components due to oxide trapped charge and interface state density as a function of total dose. There are several techniques for extracting the two components for test structure data. These include:

1. Analysis of changes in subthreshold I/V characteristics [63];
2. Analysis of the transconductance characteristic [64];
3. Charge pumping [69]; and
4. Capacitance measurements as a function of bias and frequency.

Devices have been included to support each of these techniques. Designers should select the device(s) appropriate for the measurement techniques used by their laboratory. They may wish to include devices appropriate for more than one method of separating trapped charge and interface-state effects. This will provide an independent means of verification of results.

4.2 Variable-Length Transistors

4.2.1 Purpose

The variable-length MOS transistors shown in figure 14 are used to determine effective channel length [65–67].

4.2.2 Description

The variable-length transistor structure consists of a set of four transistors of each polarity with common gates, common sources, and individual drain pads. If a bulk technology is being used, a common substrate or well contact is made close to each transistor. All transistors have the same channel width. The width is selected to be large enough to be unaffected by narrow channel effects or expected channel width variations. Within those constraints, the width should be reasonably close to the nominal value used by circuit designers. Channel lengths should range from slightly below the process target to significantly longer than the target. If only one set of transistors is to be made available, then separate contacts should be provided for gate, source, and drain of each transistor.

4.2.3 Special Design Considerations

The transistors of each polarity should be placed close together to eliminate the effects of any statistical variations in channel length on the die. To evaluate variations across a die, multiple devices should be included at different locations on the die. The transistor with the channel length less than the technology target should be placed last in the chain, or its gate should branch from the common gate bus. Otherwise, an open in the gate poly could disconnect all other gates from the pad.

4.2.4 Applications

The channel length directly affects the drive capability of the transistor through the

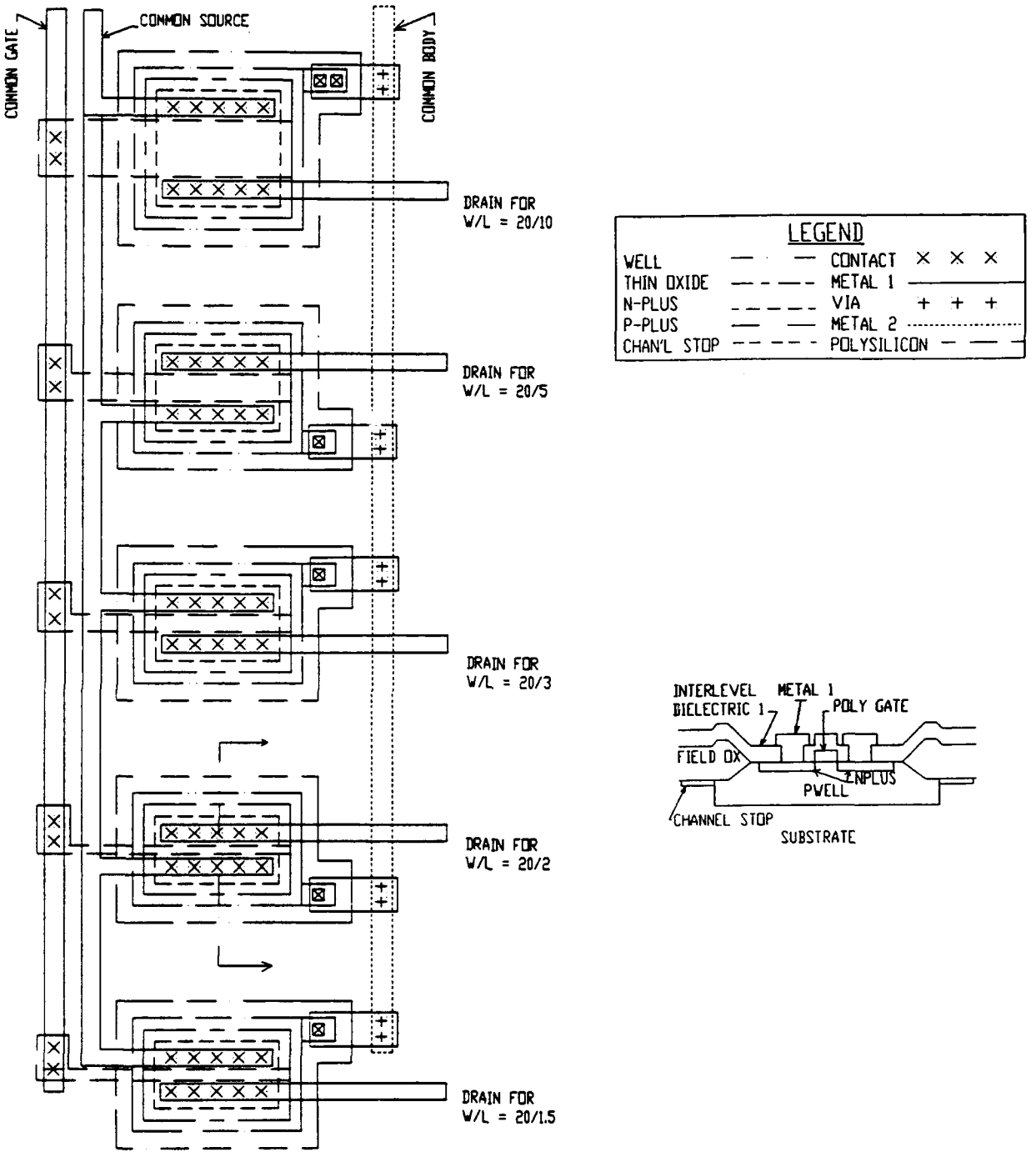


Figure 14. Variable-length transistor test structures.

width-to-length ratio. It has an indirect effect through short channel effects on threshold voltage and saturation current. Thus, the sensitivity of transistor performance to radiation-induced mobility and threshold voltage shifts will be affected by effective channel length. The channel length must be known accurately to correlate transistor characteristics to macrocell performance during development. In production, effective channel length should be monitored along with radiation-induced parameter shift to ensure that drive capability remains within the design window.

4.3 Variable-Width Transistors

4.3.1 Purpose

The variable-width MOS transistors shown in figure 15 are used to determine effective channel width [68].

4.3.2 Description

This structure consists of a set of four transistors of each polarity with common gates, common sources, and individual drain pads. If a bulk technology is being used, a common substrate or well contact is made close to each transistor. All transistors have the same channel length. The length is selected to be large enough to be unaffected by short channel effects or expected channel length variations. Within those constraints, the length should be reasonably close to the nominal value used by circuit designers. Channel widths should range from the design minimum to a value typical of input/output (I/O) stages.

4.3.3 Special Design Considerations

The transistors of each polarity should be placed close together to eliminate the effects of any statistical variations in channel length on the die. To evaluate variations across a die, multiple devices should be included at different locations on the die.

4.3.4 Applications

The channel width has a direct effect on the drive capability of the transistor through the width-to-length ratio. It has an indirect effect through narrow channel effects on threshold voltage. Thus, the sensitivity of transistor performance to radiation-induced mobility and threshold voltage shifts will be affected by effective channel width. This is especially the case for designs (e.g., memories) which use minimum-width devices. In such designs the effective width must be known accurately to correlate transistor characteristics to macrocell performance during development. In production, effective channel length should be monitored along with radiation-induced parameter shift to ensure that drive capability remains within the design window. In technologies which do not use narrow width devices, the effective width might not be of interest, and this structure could be eliminated.

4.4 Charge Pump Transistors

4.4.1 Purpose

The charge pump transistor shown in figure 16 is used to determine interface-state density as a function of total ionizing dose [69–72].

4.4.2 Description

Charge pump measurements require independent connections to gate, source, drain, and substrate. These connections should not be shared with any other device. Best results are typically achieved with devices that have relatively long, wide channels to ensure that the mask defined gate area is a good estimate of the effective gate area. If minimum gate lengths are used, short channel effects may cause some ambiguity in the data analysis.

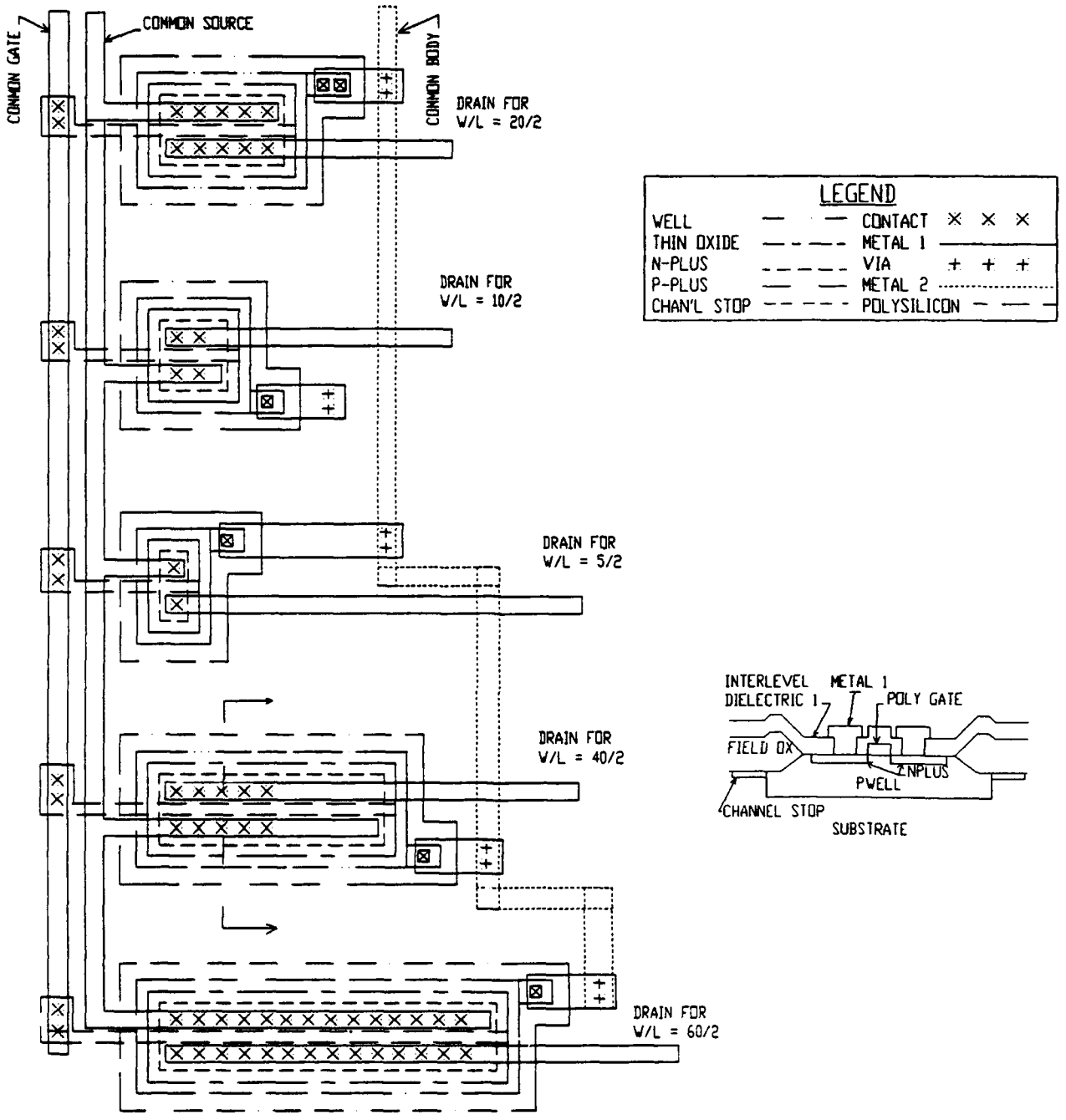


Figure 15. Variable-width transistor test structure.

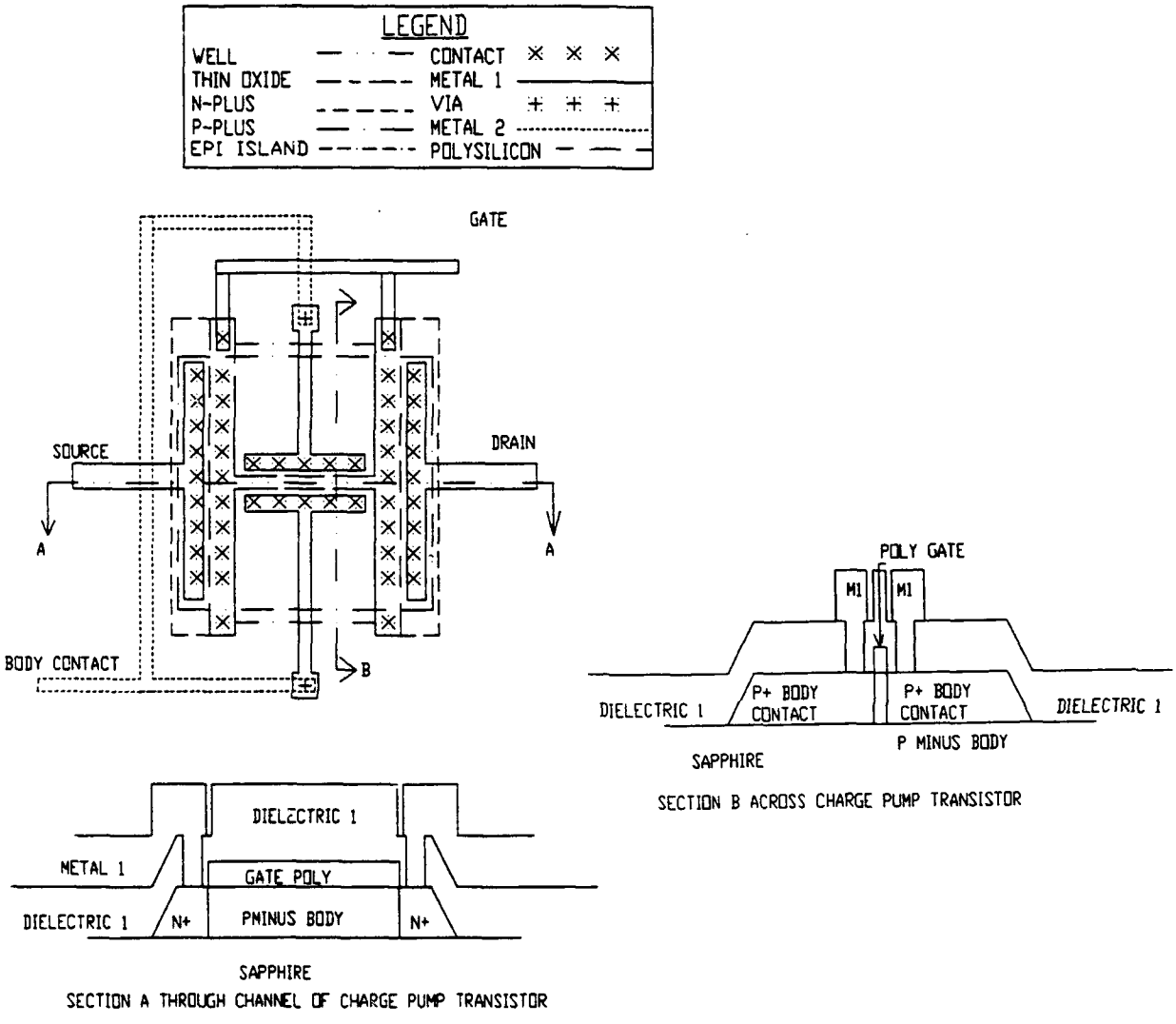


Figure 16. Four-terminal transistor test structure for charge pump.

4.4.3 *Special Design Considerations*

In insulated substrate technologies, special care must be taken in forming contact to the channel body. The epi island must be extended beyond the normal source drain region and the gate poly must be widened to protect the extension from the source/drain implant. The source/drain implant from the opposite polarity device must be placed in the extended island material to form an ohmic contact for the body. The designer should work closely with the processing engineer to ensure that a producible design has been achieved.

4.4.4 *Applications*

Charge pumping is one of several methods which can be used to separate oxide trapped charge from interface-state buildup. It is especially effective for insulated substrate technologies where back channel and edge leakage might make subthreshold techniques difficult to apply.

4.5 *Transistor—Short/Wide (Two-Edge)*

4.5.1 *Purpose*

The short, wide. two-edge transistor as shown in figure 17, is used to minimize edge leakage on transistor characteristics [73].

4.5.2 *Description*

This device is a standard transistor layout with an extended width (typically at least 10× the nominal width). This device may share a common gate and source with other transistors of the same polarity (e.g., variable length and width transistors in 4.2 and 4.3).

4.5.3 *Special Design Considerations*

Because of its large width the short/wide two-edge transistor may not fit well within a 2×N pad array. However, the designer is cautioned not to place it between two arrays because it will be shadowed by the probes and cannot be irradiated by the ARACOR x-ray tester. The designer may wish to place this transistor in an array with the multi-edge transistor.

4.5.4 *Application*

Source-to-drain edge leakage can be an important failure mechanism in both bulk CMOS and CMOS/SOS or CMOS/SOI. The edge leakage effect is less observable in very wide devices because it is responsible for a smaller percentage of the total device current. Thus, comparison of the I/V characteristics of a very wide two-edge transistor with a multi-edge device of equivalent width can be helpful in determining the exact magnitude of the edge leakage under different bias conditions.

4.6 *Transistor (W=L)*

4.6.1 *Purpose*

The transistors with equal width and length (as shown in fig. 18, are used to evaluate surface mobility and threshold voltage without complications from short- or narrow-channel effects.

4.6.2 *Description*

A standard two-edge layout is used with the width equal to the length. Typically, channel lengths of 20 μm are sufficient to eliminate short channel effects.

4.6.3 *Special Design Considerations*

This device may share common gate and source connections with other transistors.

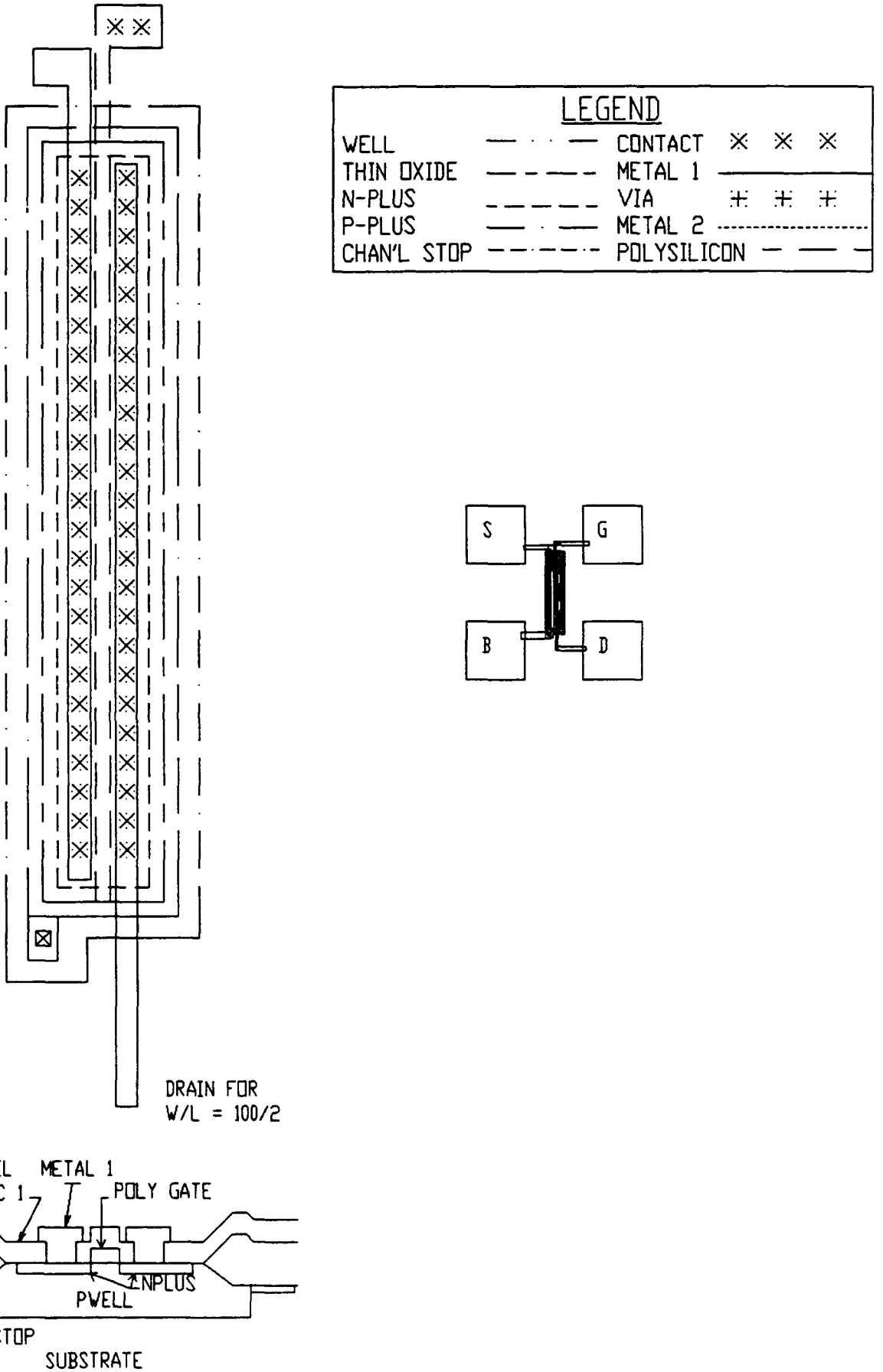


Figure 17. Extra-wide-transistor test structure.

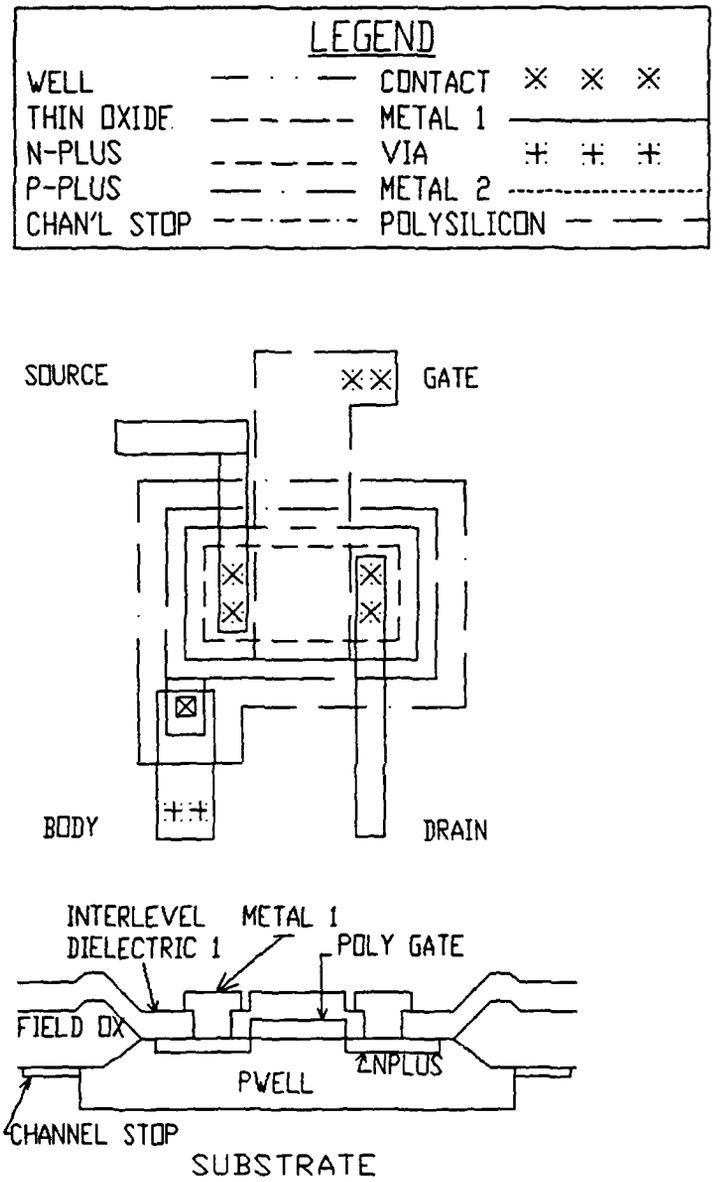


Figure 18. Unity-aspect-ratio transistor test structure.

4.6.4 *Applications*

The long channel length of this device makes it useful in separating surface mobility and threshold voltage changes with total dose from short- and narrow-channel effects including avalanche multiplication at the drain. The threshold voltage and mobility extracted from measurements on these devices may be less ambiguous than on devices with smaller dimensions.

4.7 *Nominal Transistor Array*

4.7.1 *Purpose*

The nominal transistor array, as shown in figure 19, is used to evaluate total dose effects as a function of bias and overlaying metallization layers.

4.7.2 *Description*

This device is an array of transistors with identical widths and lengths and individual pads for gate, source, and drain. Dimensions should be determined by the nominal length and width used in circuit design.

4.7.3 *Special Design Considerations*

Enough transistors should be included in the array to permit bias conditions to simulate transistor operation in:

1. an inverter,
2. a NAND/NOR gate, and
3. A transmission gate.

Total dose effects are a strong function of bias, and bias conditions for worst-case leakage might not be the same as for worst-case threshold voltage shift. Identical devices make comparison much easier for different bias conditions. In some cases, the stress created by metal overlays might affect the radiation performance of the transistor. Therefore, devices with first- and second-layer metal overlays are also included in the array. Note that individual pads have been used for the source, drain, and gate of each transistor.

4.7.4 *Applications*

The results of tests on these devices are important for correlation of measured transistor performance with observed circuit operation. Models based on these results should be made available to circuit designers for use in their simulations with computer-aided design programs such as SPICE.

4.8 *Transistors—Orthogonal Orientations*

4.8.1 *Purpose*

The orthogonally oriented transistors, as shown in figure 20, are used to check for symmetrical source-to-drain versus drain-to-source I/V characteristics.

4.8.2 *Description*

This structure consists of two transistors of each type (n-channel and p-channel) oriented at 90 degrees to one another.

4.8.3 *Special Design Considerations*

These transistors could be part of the array discussed in section 4.7. Although each transistor must have individual source and drain pads, they could share a common gate.

4.8.4 *Applications*

Technologies with short channel lengths may not exhibit bilateral operation as a result of the angle used for the source/drain implant or etch problems. This can be checked by comparing the I/V characteristics of orthogonally oriented transistors.

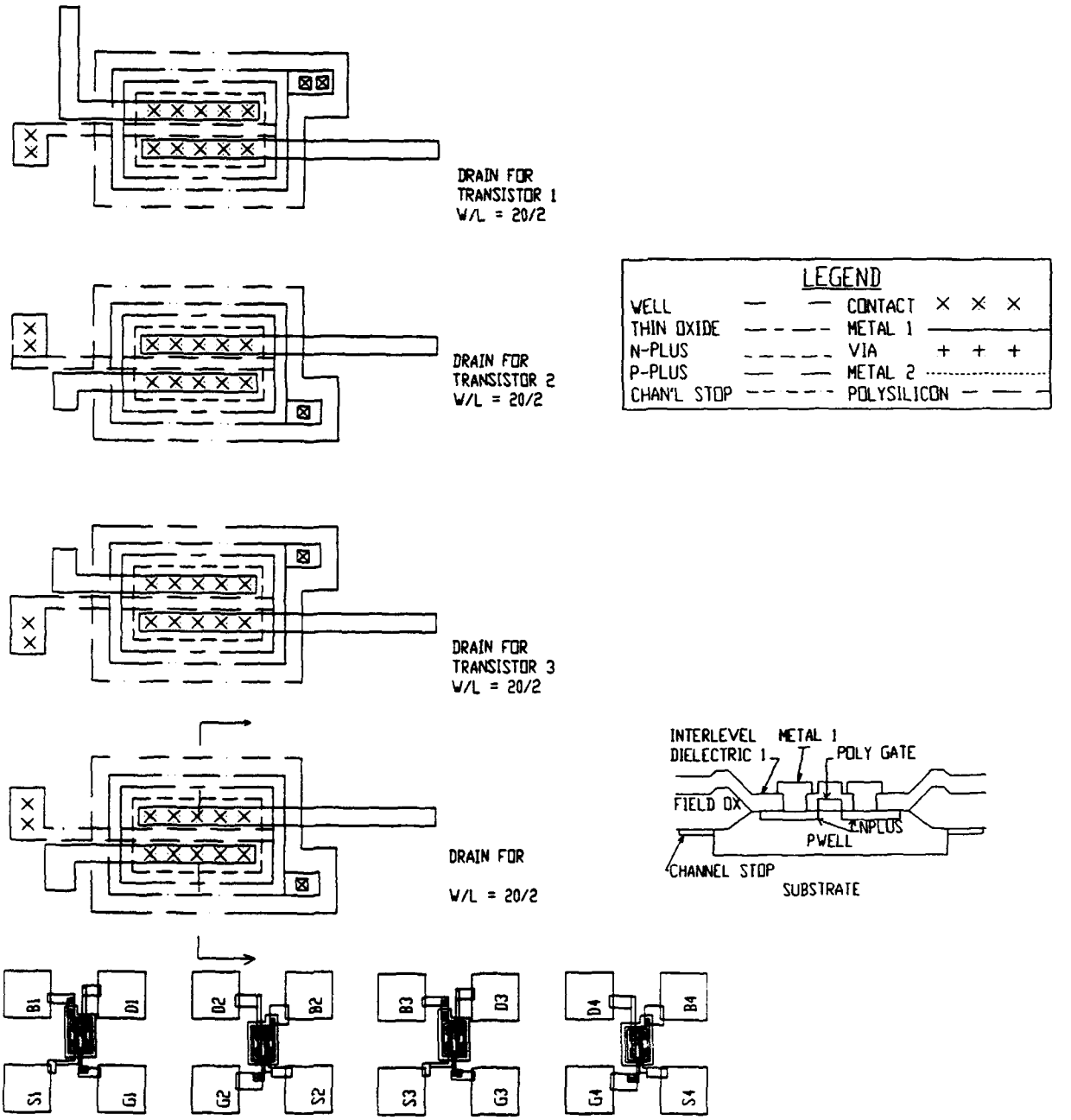


Figure 19. Multiple nominal dimension transistor test structures.

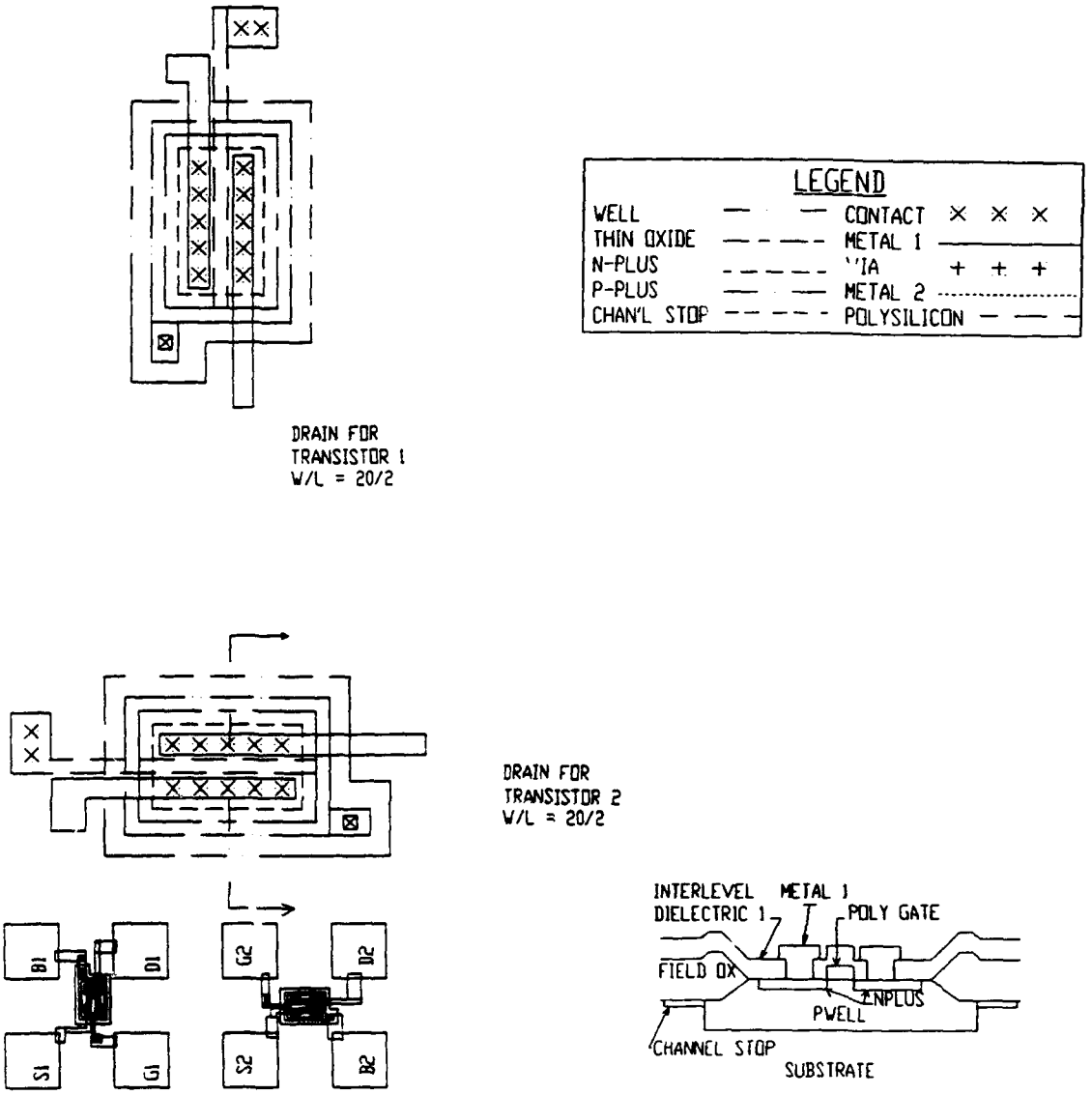


Figure 20. Orthogonal transistor test structure.

4.9 *Multi-Edge Transistors*

4.9.1 *Purpose*

The multi-edge transistors, shown in figure 21 are used to emphasize edge leakage in comparison to normal source/drain current or back-channel leakage.

4.9.2 *Description*

The multi-edge transistor is a parallel connection of several narrow two-edge transistors. Typically, at least 20 transistor sections (i.e., 40 edges) are used in the structure.

4.9.3 *Special Design Considerations*

The multi-edge transistor should be used in conjunction with a two-edge device of equivalent width, as discussed in paragraph 4.5.

4.9.4 *Applications*

Source-to-drain edge leakage can be an important failure mechanism in both bulk CMOS and CMOS/SOS or CMOS/SOI. The edge leakage effect is less observable in very wide two-edge devices because it is responsible for a smaller percentage of the total device current. Thus, comparison of the I/V characteristics of a very wide two-edge transistor with a multi-edge device of equivalent width can be helpful in determining the exact magnitude of the edge leakage under different bias conditions.

4.10 *Edgeless Transistors*

4.10.1 *Purpose*

The edgeless transistor, as shown in figure 22, is used to eliminate edge leakage from the transistor I/V characteristics.

4.10.2 *Description*

The edgeless transistor uses a concentric design with the drain in the center and the source on the outside. Thus, there is no edge path for source/drain leakage.

4.10.3 *Special Design Considerations*

The width of the device is ambiguous since the source and drain perimeters are different. A working estimate of the width is the perimeter of a line which bisects the channel. The device usually has relatively long sides (25 μm) so that corner effects are not significant. A wide, edgeless device is useful for comparison to the wide two-edge and the multi-edge devices.

4.10.4 *Applications*

Since the edgeless device has no edge leakage component, it can be used to separate back channel leakage effects from edge leakage. Therefore, it should be used in conjunction with two-edge and multi-edge devices of equivalent width.

4.11 *Transistors with Source/Body Ties*

4.11.1 *Purpose*

The source/body ties in insulated substrate transistors (see fig. 23) are used to eliminate kink effects (reduction in threshold voltage and increase in drain current) resulting from floating body material in insulated substrate technologies (i.e., SOS and SOI). The source/body ties are also used to eliminate secondary photocurrents arising from primary photocurrent multiplication by the parasitic bipolar transistor. This is especially the case in SOI technologies where the minority carrier lifetime can be quite high.

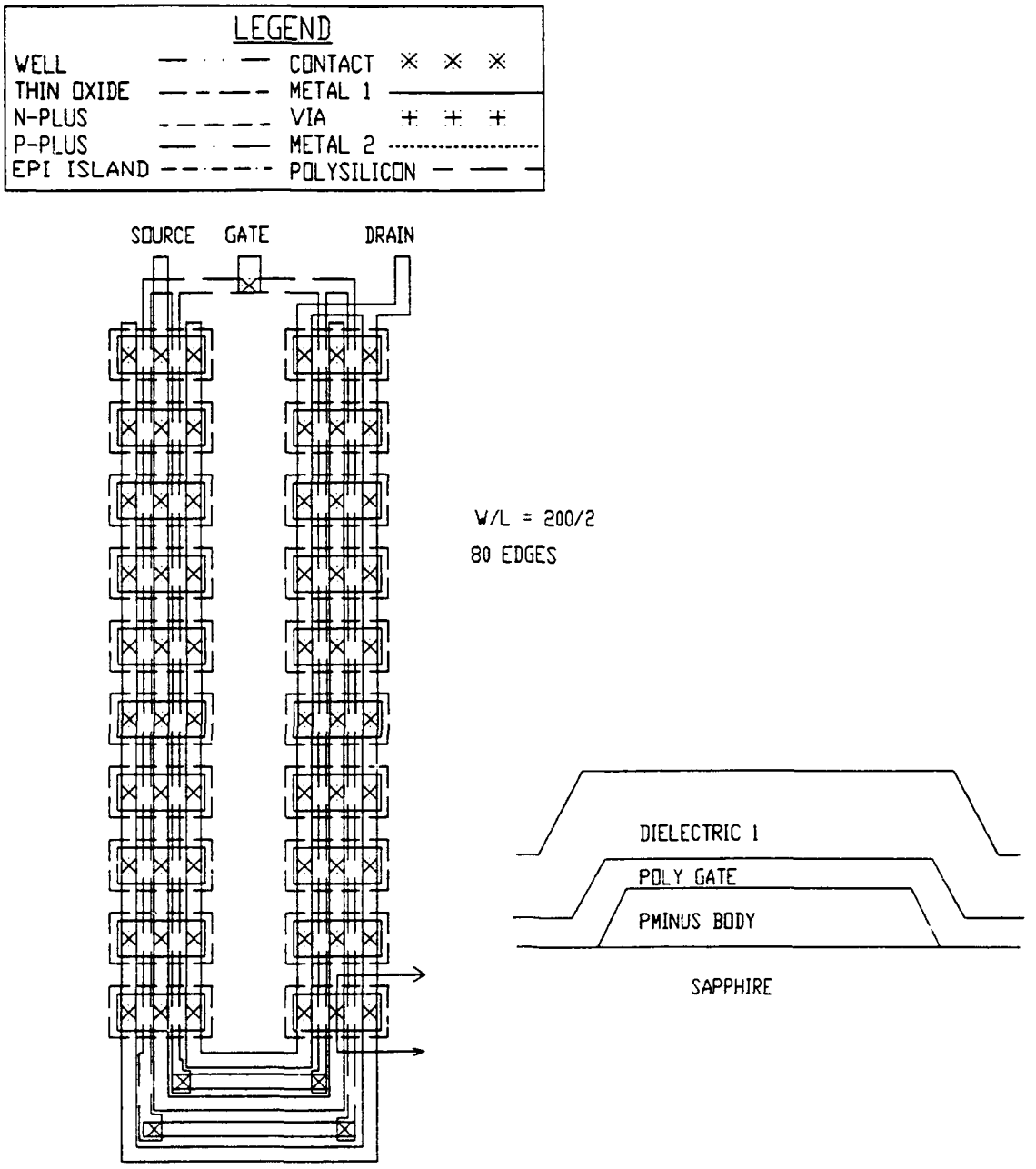


Figure 21. Multi-edge transistor test structure.

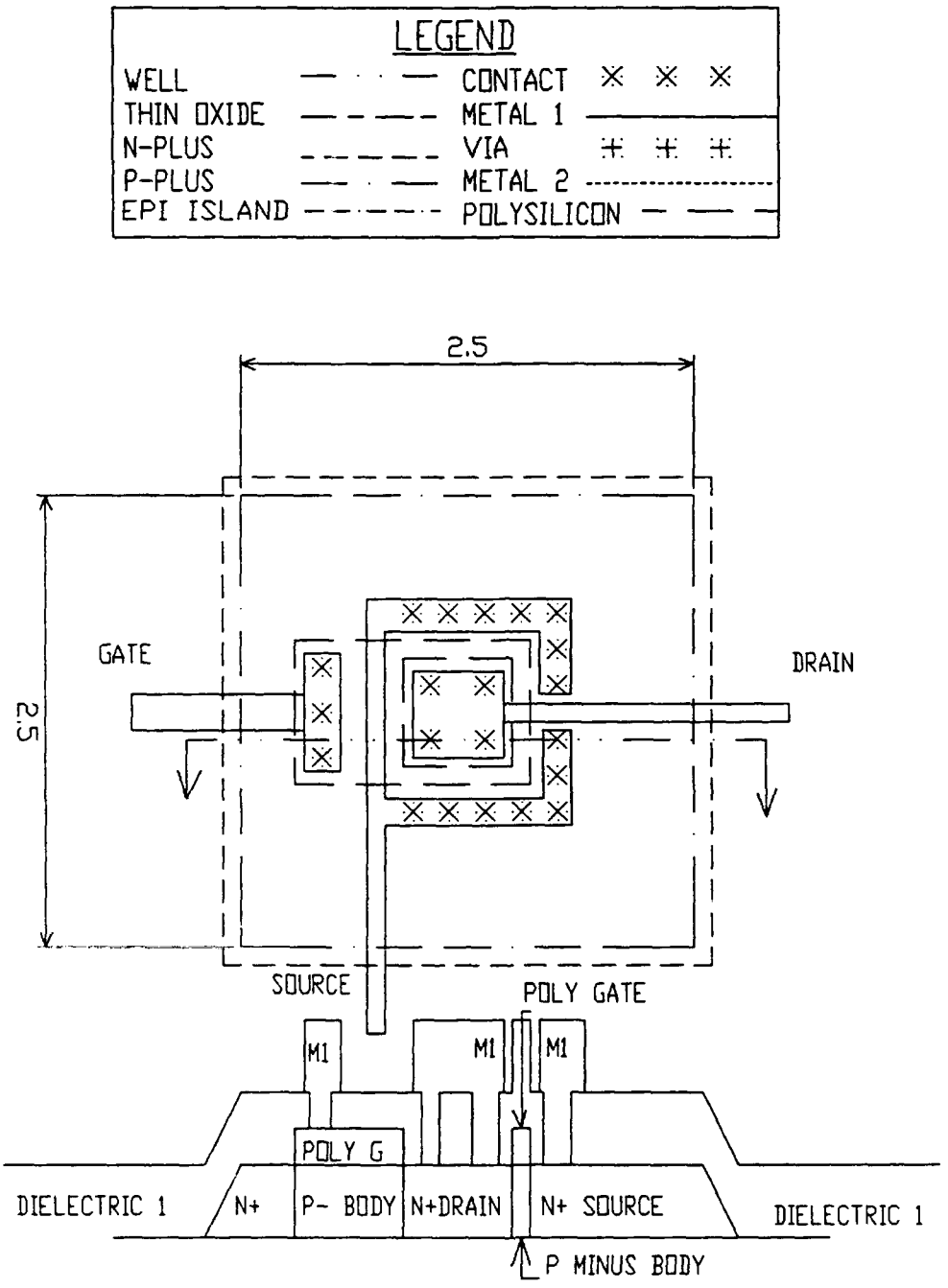


Figure 22. Edgeless transistor test structure.

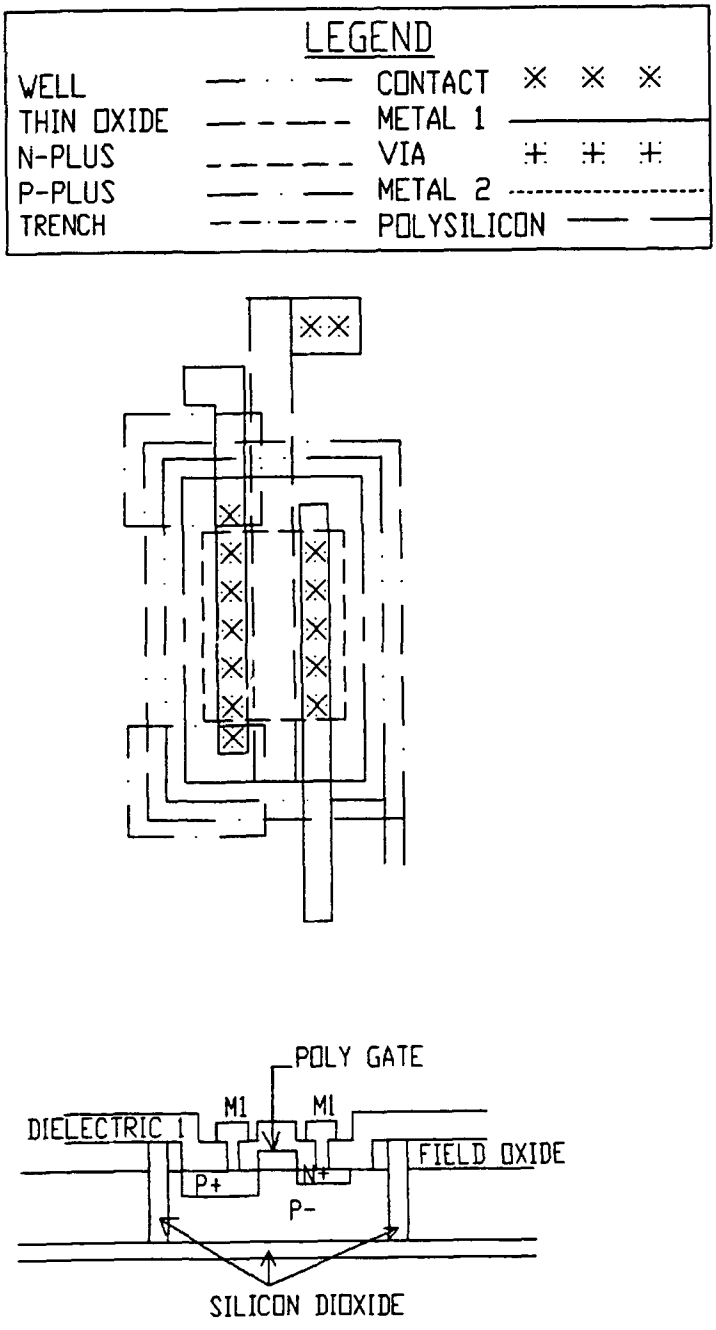


Figure 23. Source/body-tie transistor test structure.

4.11.2 Description

There are several ways for implementing source/body ties in the different insulated substrate technologies. The designer should select a method consistent with the processing technology.

4.11.3 Special Design Considerations

The body of the transistor is a high-resistivity material. Consequently, it is difficult to form an ohmic contact while still preserving minimum transistor geometries. If the source/body tie is made only at one end of the transistor, there will probably be enough body resistance to debias the other end of the transistor.

4.11.4 Applications

The transistor with body tied to source is usually included to perform I/V characterization for model parameter extraction. The benefit for increasing dose-rate-upset thresholds has to be determined from macrocell characterization.

4.12 Gate Oxide Capacitor—Minimum Aspect Ratio

4.12.1 Purpose

The gate oxide capacitor, as shown in figure 24, is used to

1. determine gate oxide thickness;
2. determine threshold voltage shifts with total dose, and
3. Separate interface-state and trapped-oxide charge components of the threshold voltage [74–76].

4.12.2 Description

The minimum-aspect-ratio gate-oxide capacitor is a simple square structure with a polysilicon gate electrode and peripheral contacts to the substrate or well material. Devices should be made over both substrate and well.

4.12.3 Special Design Considerations

The capacitance value will scale directly with the area and inversely with the oxide thickness. The designer should consult with the test engineer to determine the value of capacitance required for best test results. Typically, a value of 5 pF is sufficient. Because of the small aspect ratio and the large size, there will be significant parasitic resistance between the center of the capacitor and the contact ring for the lower plate. The resulting RC time constant may be significant for high-frequency measurements.

4.12.4 Applications

There are several methods for using capacitors as diagnostic tools for radiation effects. The designer may wish to consult the references noted in section 4.12.1 for background material. Capacitors are especially good tools for quick turnaround process development runs. They can be made with simple masks and do not require all the process steps to yield usable devices. However, capacitors cannot simulate all the bias conditions encountered by transistors. Final evaluation of the radiation hardness of a process should be done with transistors.

4.13 Gate Oxide Capacitor—Large Aspect Ratio

4.13.1 Purpose

The large-aspect-ratio gate-oxide capacitor, as shown in figure 25, is used to eliminate parasitic series resistance from the connection to the bottom plate of the capacitor. The

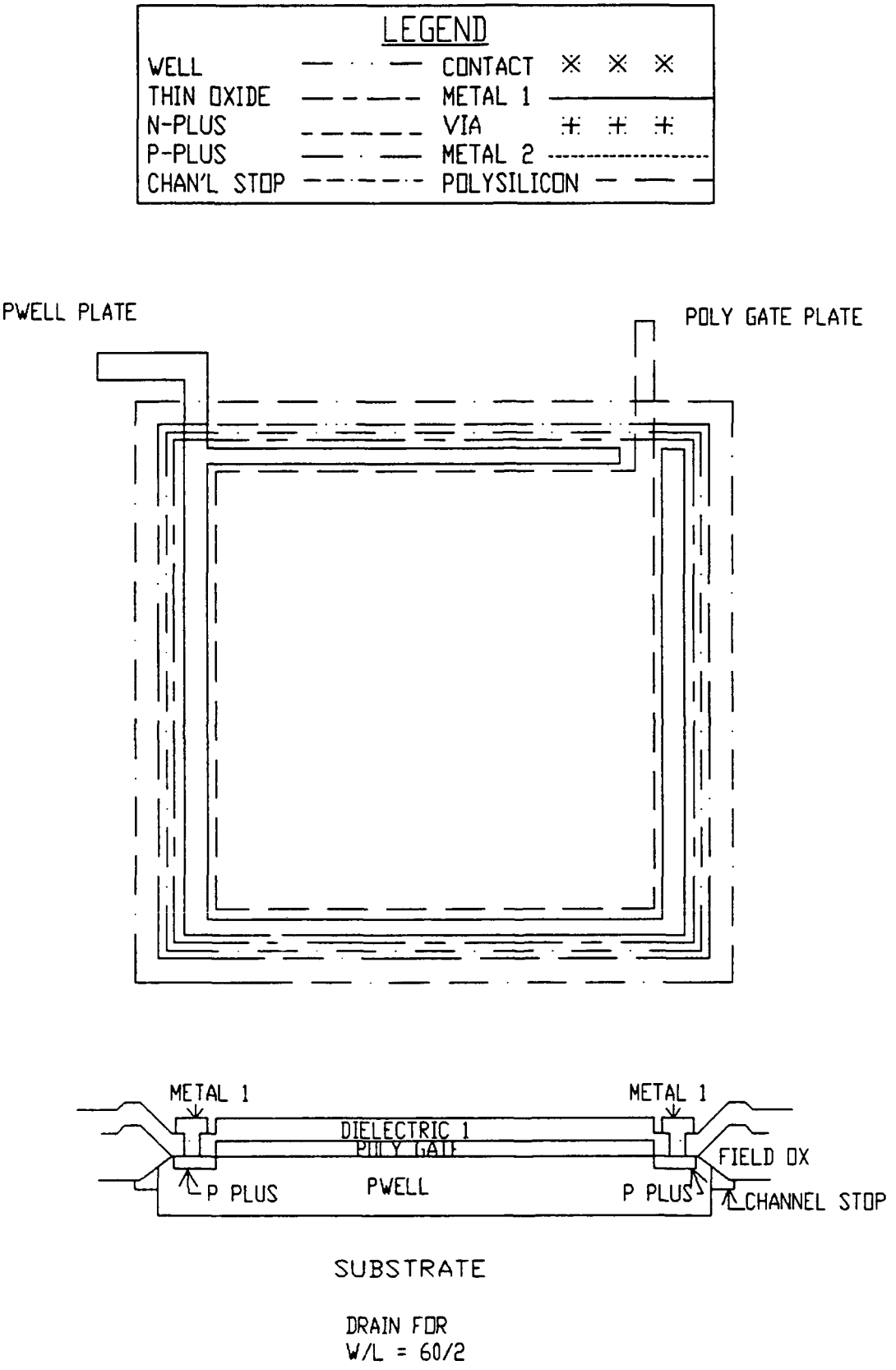


Figure 24. Gate oxide capacitor with minimum aspect ratio.

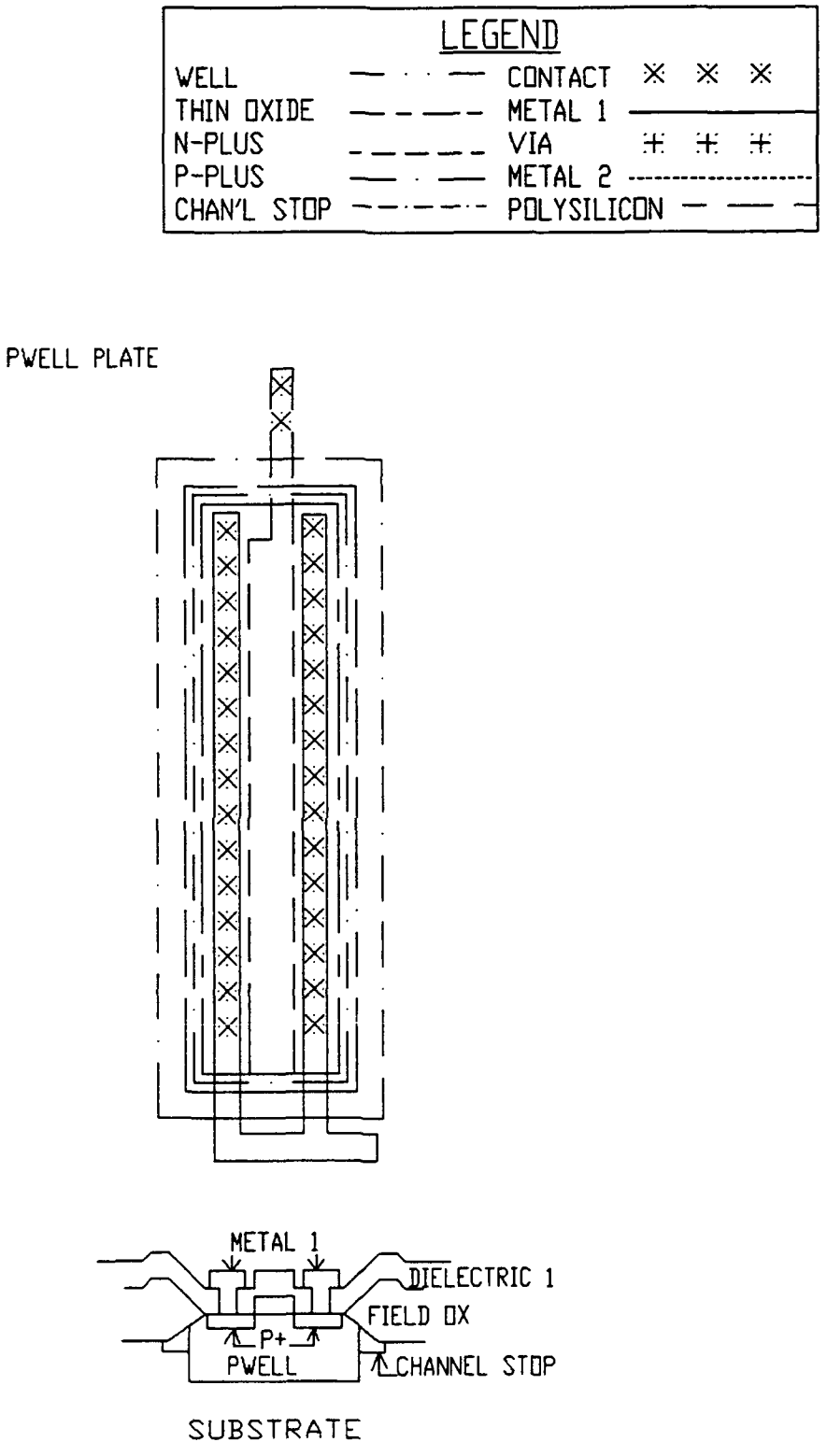


Figure 25. Large-aspect-ratio capacitor test structure.

device may also act as a depletion mode transistor for profiling the doping concentration in the body.

4.13.2 Description

The large-aspect-ratio gate-oxide capacitor may be a serpentine or interdigitated structure with substrate or well contacts on either side of the body. The two contacts are brought out to separate pads so that the device can be used as a depletion mode transistor.

4.13.3 Special Design Considerations

The device should have a body length between the contacts to the lower plate of 3 to 5 μm. The width of the device should be chosen to give good test results. Typically, 5 pF is a good target value.

4.13.4 Applications

The large aspect ratio capacitor has similar applications to the minimum aspect ratio capacitor. The reduced series resistance in the lower plate improves the accuracy of high-frequency measurements.

5. FIELD OXIDE DEVICES

5.1 Introduction

The test structures described in this section are directed toward field oxide hardness in MOS technologies. They are also useful to parameterizing values for parasitic capacitance between polysilicon or metal 1 and the silicon substrate or well. These values are needed for simulation of propagation delay paths for correlating transistor characteristics to actual circuit performance.

Potential leakage paths associated with field oxides include

1. leakage between devices within the well or substrate, and
2. leakage between a device in a well and the substrate.

Devices should be included to check both types of paths if they are appropriate to the technology.

5.2 Edgeless Field-Oxide Transistors with Poly Gates

5.2.1 Purpose

Edgeless field transistors with polysilicon gates, as shown in figure 26, are used to check for leakage between devices within a well or substrate.

5.2.2 Description

This structure is a typical edgeless transistor as described in section 4.10, with the exception that the channel is under field oxide, rather than thin, gate oxide. The source and drain are the source/drain implants for thin oxide transistors. The structure simulates leakage between source and drain of adjacent transistors.

5.2.3 Special Design Considerations

The channel length should be the minimum source/drain spacing for adjacent transistors. The device should be relatively wide to maximize the drain current amplitude. There may be a design rule for spacing between source/drain contact openings and polysilicon interconnect. This rule may be violated for the test structure to ensure that the gate extends completely over the field oxide field-effect transistor (FET) channel. The designer may include both a device made with the design rule and one which violates the design rule. Additional devices may be included with variations in source/drain spacing of adjacent transistors to investigate design rule modification.

5.2.4 Applications

These devices are primarily used to develop design rules for spacing between adjacent transistors. Split lots may be required to investigate the effects of channel-stop implant-concentration as well as spacing on leakage characteristics.

5.3 Edgeless Transistors with Metal-1 Gate

5.3.1 Purpose

The edgeless field transistors with metal-1 gates, as shown in figure 27, are used to check for leakage between devices within a well or substrate.

5.3.2 Description

This structure is a typical edgeless transistor as described in section 4.10, with the exception that the channel is under field oxide, rather than thin, gate oxide. The source and drain are the source/drain implants for thin oxide transistors. The structure simulates leakage between source and drain of adjacent transistors.

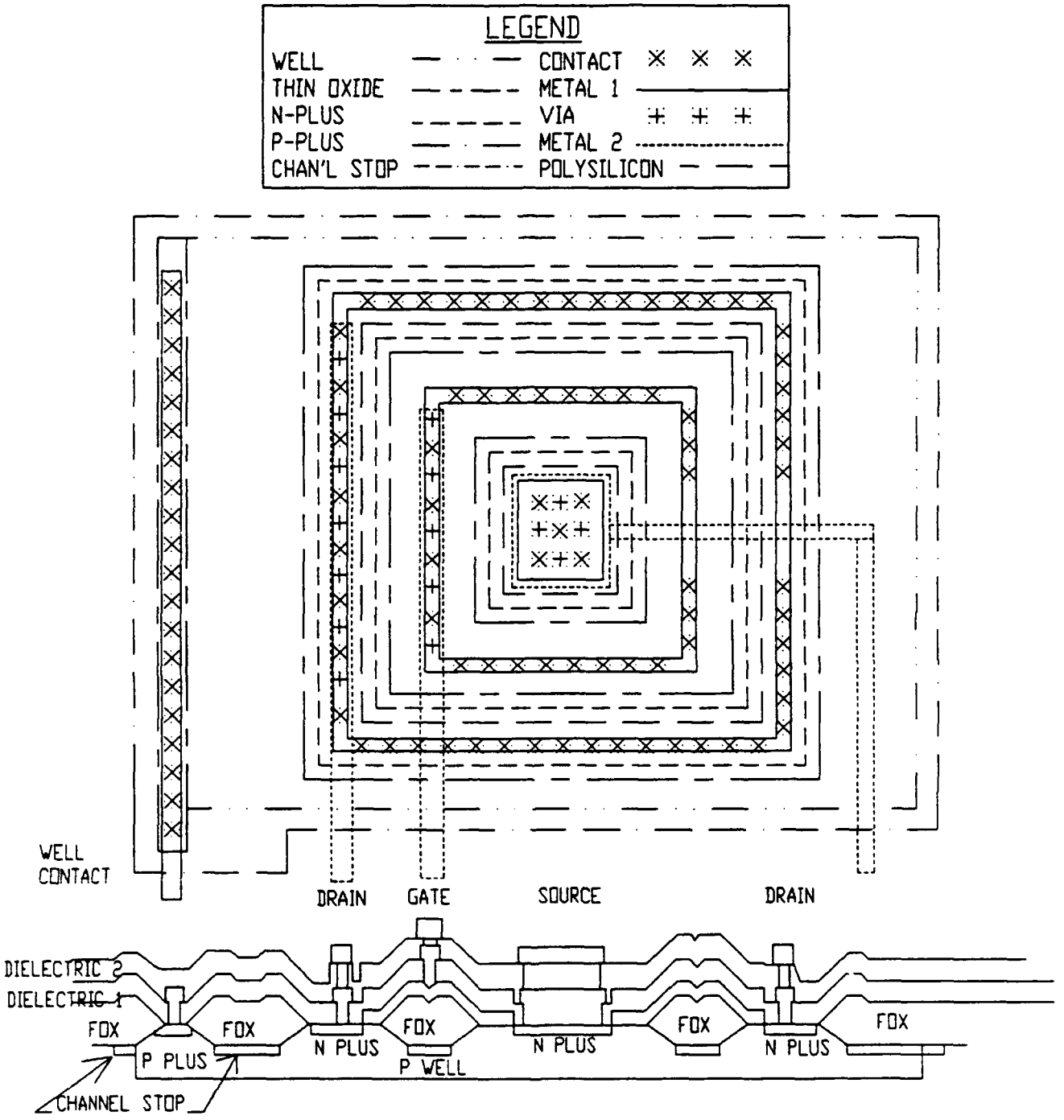


Figure 26. Edgeless poly-gate field-oxide transistor test structure.

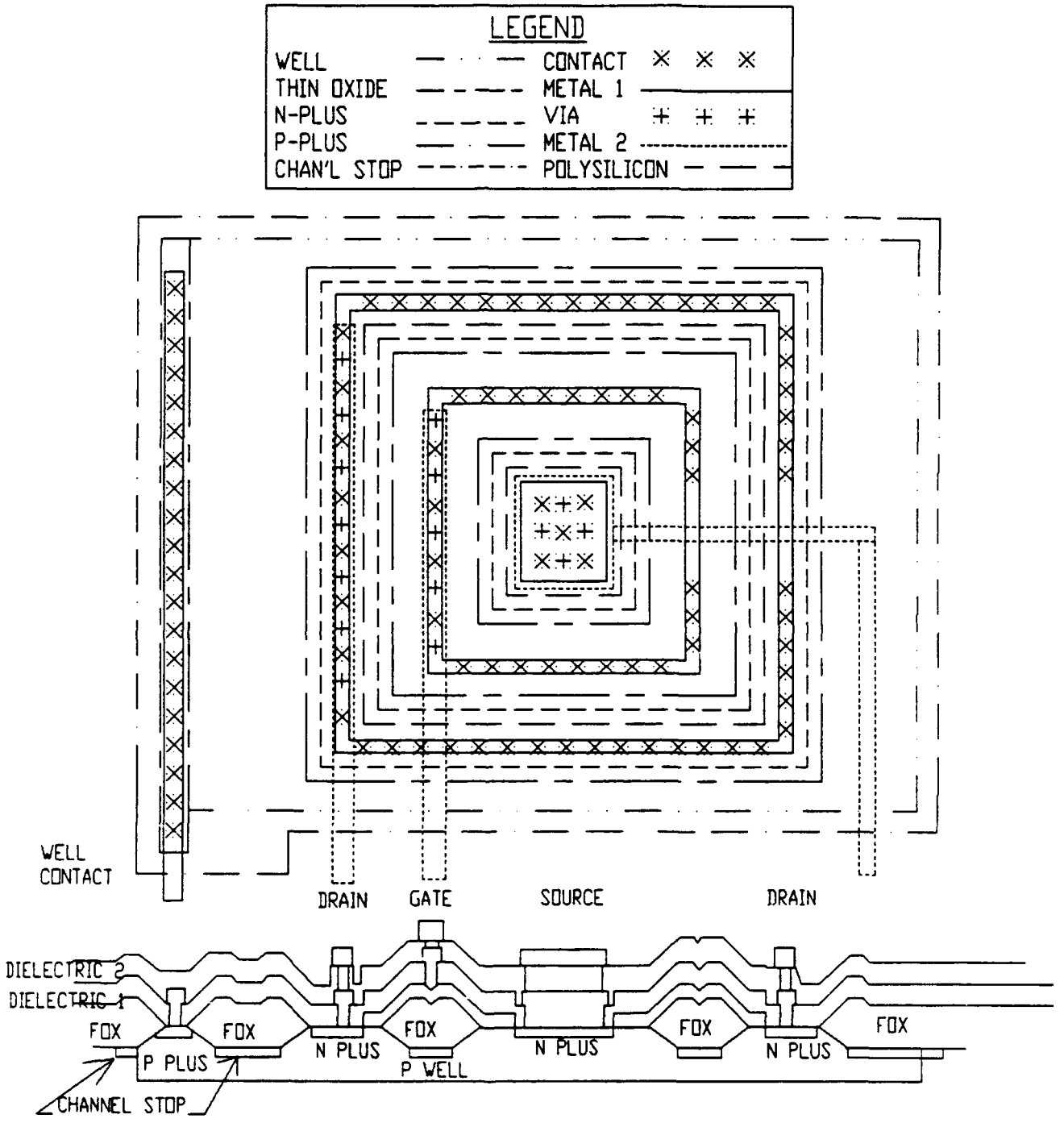


Figure 27. Edgeless metal-gate field-oxide transistor test structure.

5.3.3 *Special Design Considerations*

The channel length should be the minimum source/drain spacing for adjacent transistors. The device should be relatively wide to maximize the drain current amplitude. There may be a design rule for spacing between source/drain contact openings and metal-1 interconnect. This rule may be violated for the test structure to ensure that the gate extends completely over the field oxide FET channel. The designer may include both a device made with the design rule and one which violates the design rule. Additional devices may be included with variations in source/drain spacing of adjacent transistors to investigate design rule modification.

5.3.4 *Applications*

Some technologies do not allow polysilicon to be used as an interconnect level between adjacent transistors. In such cases, any field inversion will take place under metal-1 runs. These devices are primarily used to develop design rules for spacing between adjacent transistors. Split lots may be required to investigate the effects of channel-stop implant-concentration as well as spacing on leakage characteristics.

5.4 *Two-Edge Transistors with Poly or Metal-1 Gate*

5.4.1 *Purpose*

The two-edge transistor shown in figure 28 with poly or metal-1 gate is used to investigate leakage between the well and the source of the transistor fabricated in the substrate.

5.4.2 *Description*

For a P-well technology, this parasitic field-oxide MOSFET is formed between the substrate and the source of an N-channel transistor fabricated in the well. The gate material must overlay the channel region between the N-channel source and the P-well edge. The leakage path connects the V_{ss} and V_{dd} supplies. The length of the device should be the design rule for N-channel source to P-well spacing. The width should be the dimension of a typical P-well. The overlaying gate may be either polysilicon, or metal-1, or a separate structure may be included for each interconnect.

5.4.3 *Special Design Considerations*

Several of these structures may be included to select with a variety of spacings between well and source to establish design rules.

5.4.4 *Applications*

Well-to-source leakage paths should be checked carefully in all technologies, especially those employing a hardened field oxide rather than channel stops. These potential leakage paths are connected directly between V_{dd} and V_{ss} and can have large areas involved in the path.

5.5 *Polysilicon/Silicon Capacitor with Minimum Aspect Ratio*

5.5.1 *Purpose*

The polysilicon/silicon capacitor with minimum aspect ratio, as shown in figure 29, is used to check field inversion and determine parasitic poly-to-silicon capacitance values.

5.5.2 *Description*

The capacitor is formed between interconnect polysilicon and the well or substrate material. Top side contacts should be made to the silicon around the periphery of the capacitor.

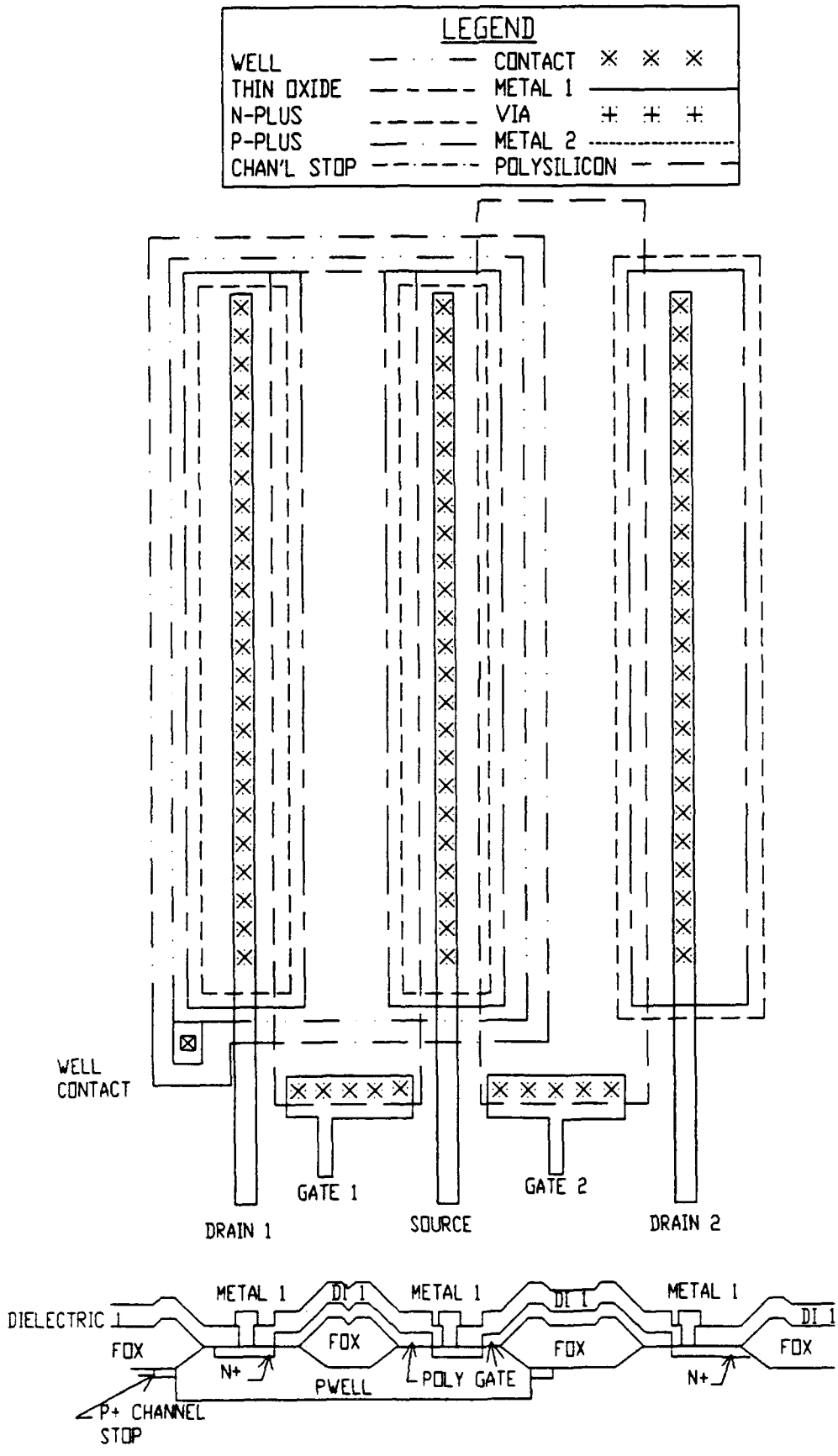


Figure 28. Field oxide transistor with polysilicon gate.

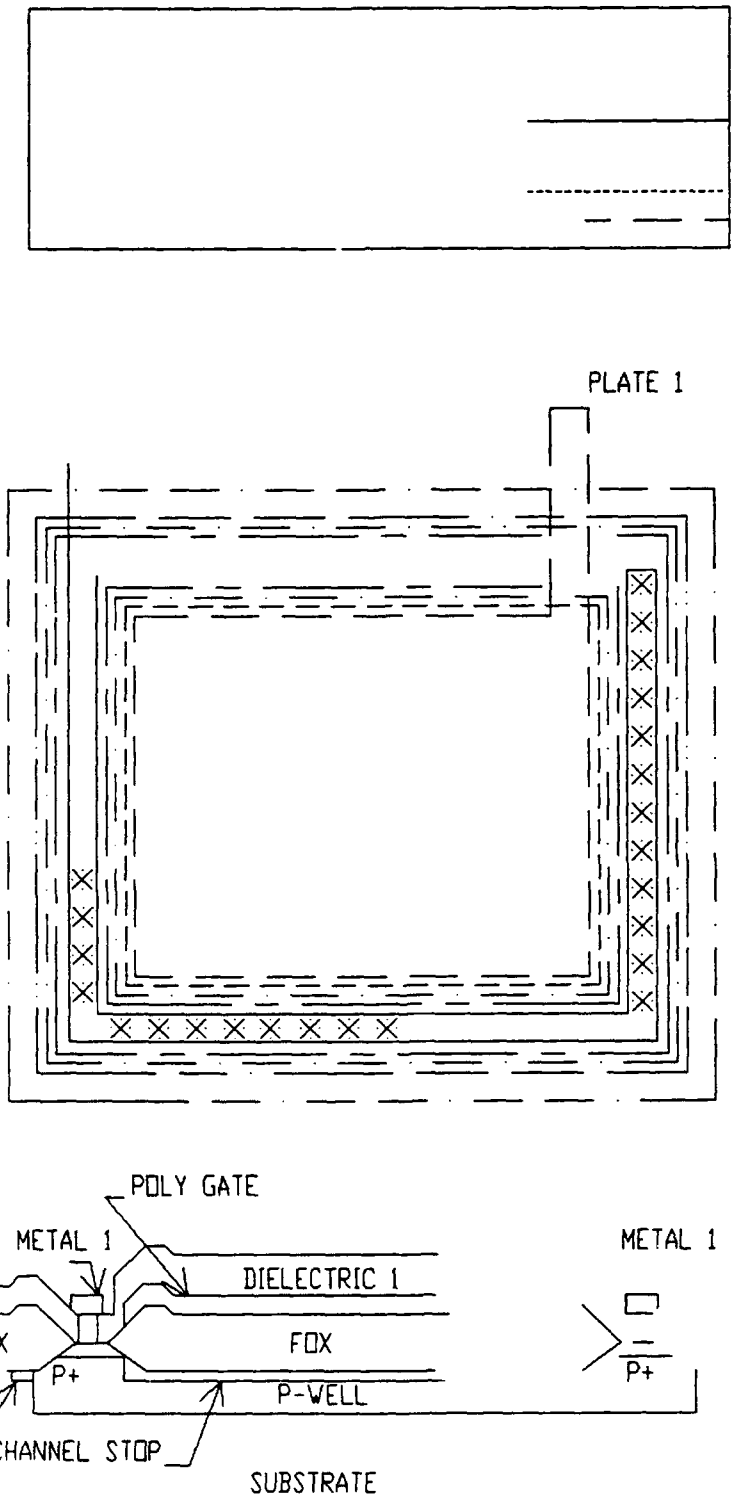


Figure 29. Polysilicon field-oxide capacitor with minimum aspect ratio.

5.5.3 *Special Design Considerations*

The capacitor should be sized to give a value of capacitance which can be measured accurately. Typically, values in the range of 5 pF are adequate.

5.5.4 *Applications*

Although capacitance techniques can be used to determine threshold voltage shifts in the field oxide, extremely careful measurements must be made. Usually, field oxide transistors are better vehicles for radiation effects investigations.

5.6 *Polysilicon/Silicon Capacitor with Large Aspect Ratio*

5.6.1 *Purpose*

The polysilicon/silicon capacitor with large aspect ratio, as shown in figure 30, is used to check field inversion and determine parasitic poly-to-silicon capacitance values.

5.6.2 *Description*

The capacitor may be a serpentine or interdigitated structure formed between interconnect polysilicon and the well or substrate material. Top side contacts should be made to the silicon around both edges of the capacitor. The contacts on each side can be brought out to independent pads so that the device can be used as a depletion mode FET.

5.6.3 *Special Design Considerations*

The capacitor should be sized to give a value of capacitance which can be measured accurately. Typically, values in the range of 5 pF are adequate.

5.6.4 *Applications*

Although capacitance techniques can be used to determine threshold voltage shifts in the field oxide, extremely careful measurements must be made. Usually, field oxide transistors are better vehicles for radiation effects investigations. The large aspect ratio capacitor can also be act as a depletion mode FET and be used to characterize the doping profile of any surface implant under the field.

5.7 *Metal-1/Silicon Capacitor with Minimum Aspect Ratio*

5.7.1 *Purpose*

The metal-1/silicon capacitor with minimum aspect ratio, as shown in figure 31, is used to check field inversion and determine parasitic metal-1-to-silicon capacitance values.

5.7.2 *Description*

The capacitor is a large-area metal-1 plate over thick field oxide and well or substrate area. Topside substrate contacts should be placed around the periphery of the capacitor.

5.7.3 *Special Design Considerations*

The capacitor should be sized to give a value of capacitance which can be measured accurately. The capacitance per unit area of these devices is quite low because it includes both the thick field oxide and the interlevel dielectric between the polysilicon and metal-1.

5.7.4 *Applications*

Although the capacitance technique can be used to determine threshold voltage shifts in the field oxide, extremely careful measurements must be made. Usually, field oxide transistors are better vehicles for radiation effects investigations.

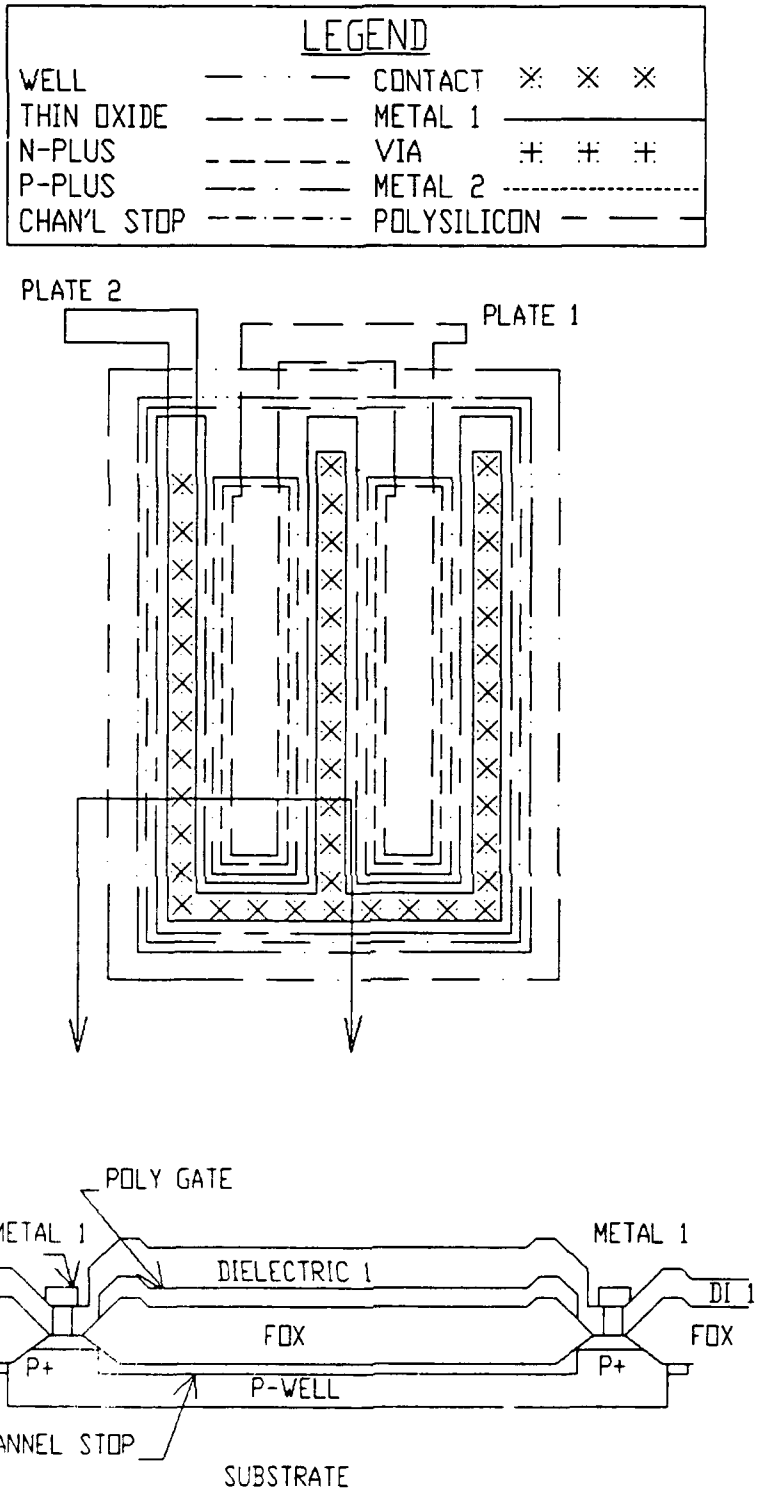


Figure 30. Polysilicon field-oxide capacitor for large aspect ratio.

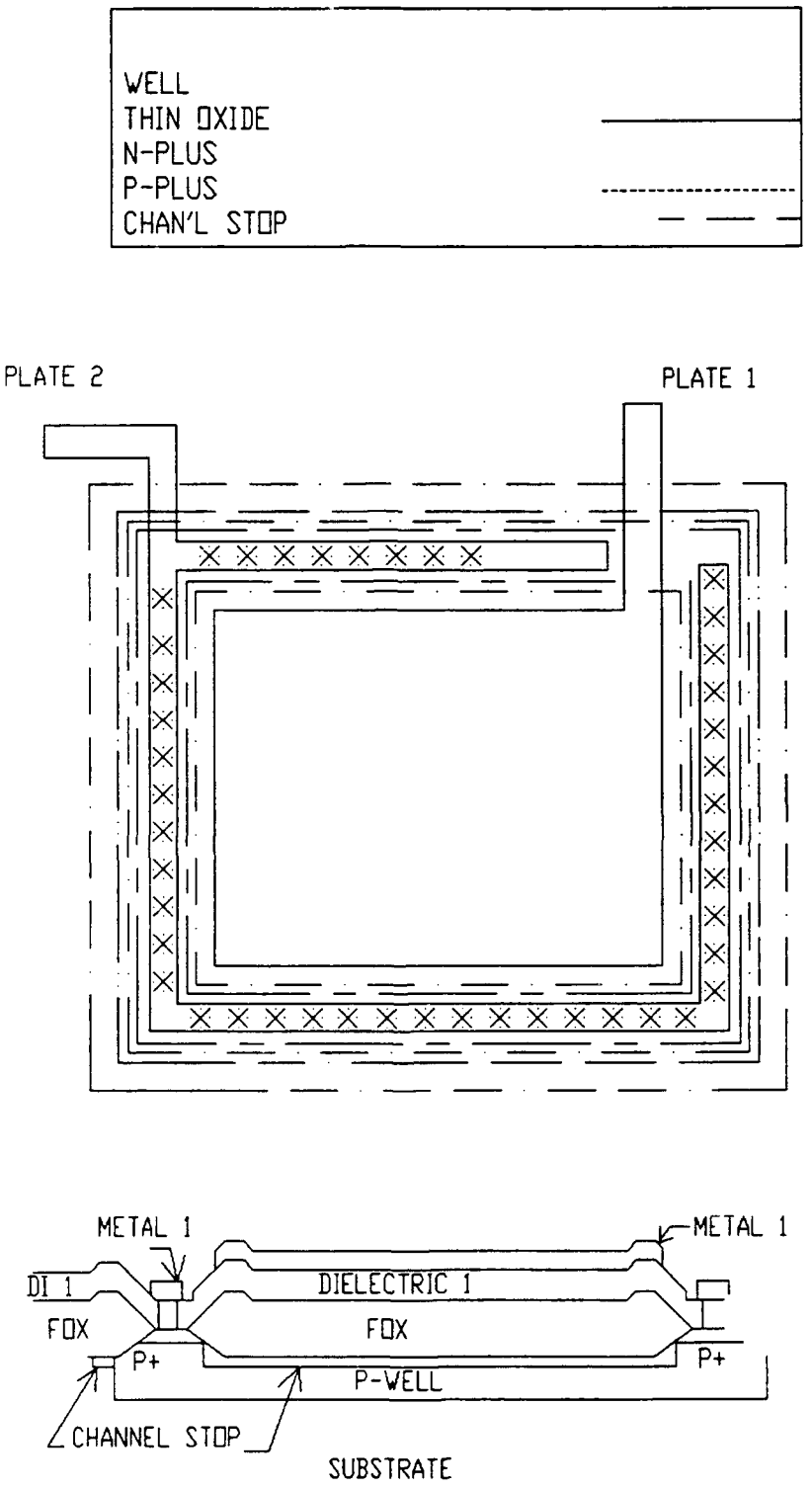


Figure 31. Metal-1 silicon capacitor with minimum aspect ratio.

5.8 Metal-1/Silicon Capacitor with Large Aspect Ratio

5.8.1 Purpose

The metal-1/silicon capacitor with large aspect ratio, as shown in figure 32, is used to check field inversion and determine parasitic poly-to-silicon capacitance values.

5.8.2 Description

The capacitor may be a serpentine or interdigitated structure formed between metal-1, the field oxide, and the well or substrate material. Top side contacts should be made to the silicon around both edges of the capacitor. The contacts on each side can be brought out to independent pads so that the device can be used as a depletion mode FET.

5.8.3 Special Design Considerations

The capacitor should be sized to give a value of capacitance which can be measured accurately. Typically, values in the range of 5 pF are adequate.

5.8.4 Applications

Although capacitance technique can be used to determine threshold voltage shifts in the field oxide, extremely careful measurements must be made. Usually, field oxide transistors are better vehicles for radiation effects investigations. The large aspect ratio capacitor can also be act as a depletion mode FET and be used to characterize the doping profile of any surface implant under the field.

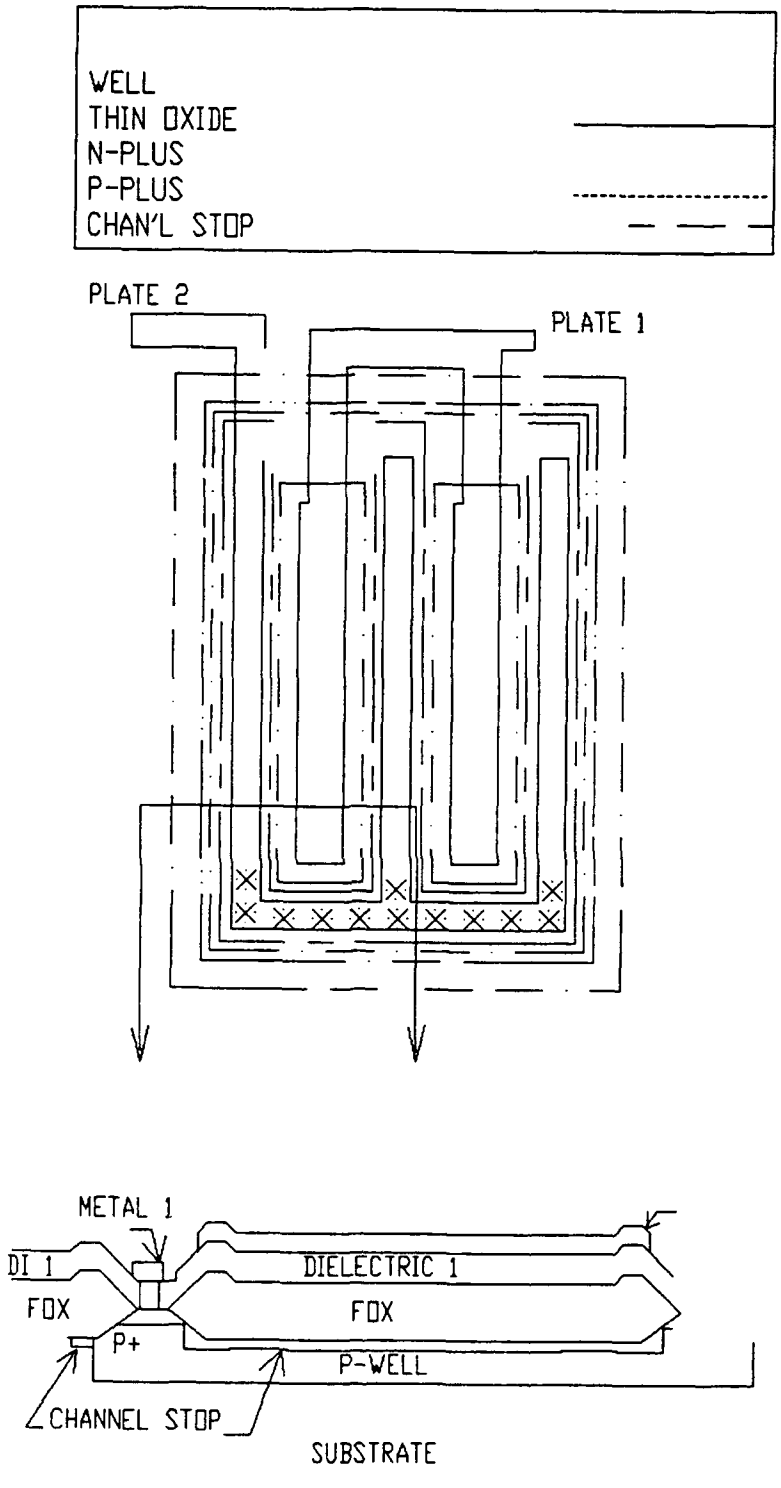


Figure 32. Metal-1 silicon capacitor with large aspect ratio.

6. INTERLEVEL DIELECTRIC DEVICES

6.1 Introduction

Capacitance between interconnect layers can be important in determining the load driven by individual gates. Although the values of these capacitors do not change with radiation, they are important in modeling specific propagation delay paths.

6.2 Capacitors with Interconnect Level Plates

6.2.1 Purpose

Capacitors formed between interconnect levels, as shown in figure 33, are used to measure interlevel capacitance [77].

6.2.2 Description

These devices are large parallel plate capacitors with each layer brought out to a separate pad.

6.2.3 Special Design Considerations

These very large structures may be eliminated on small test chips.

6.2.4 Applications

Interlevel capacitance may be especially significant on technologies such as gate arrays which use long metallization runs for routing between macrocells.

6.3 Fringing Field Capacitor—Metal-1/Polysilicon

6.3.1 Purpose

The fringing field capacitor, as shown in figure 34, is used to determine interlevel capacitance for layers which are not overlapping but are in close proximity.

6.3.2 Description

This capacitor may be a serpentine or interdigitated structure. The two interconnect layers are spaced at the minimum design rule for gate to metal-1-to-source/drain contact.

6.3.3 Special Design Considerations

The fringing field capacitance between the gate poly and the metal-1 contact to source drain may not be important if parallel runs are not permitted along the length of the transistor. If that is the case, this structure may be omitted.

6.3.4 Applications

If the gate poly runs parallel to the metal-1 contact to the source/drain over the length of the transistor, the fringing field capacitance between the two interconnects acts as a Miller capacitance. It is multiplied by the gain of the gate, and can have a significant impact on the stage propagation delay.

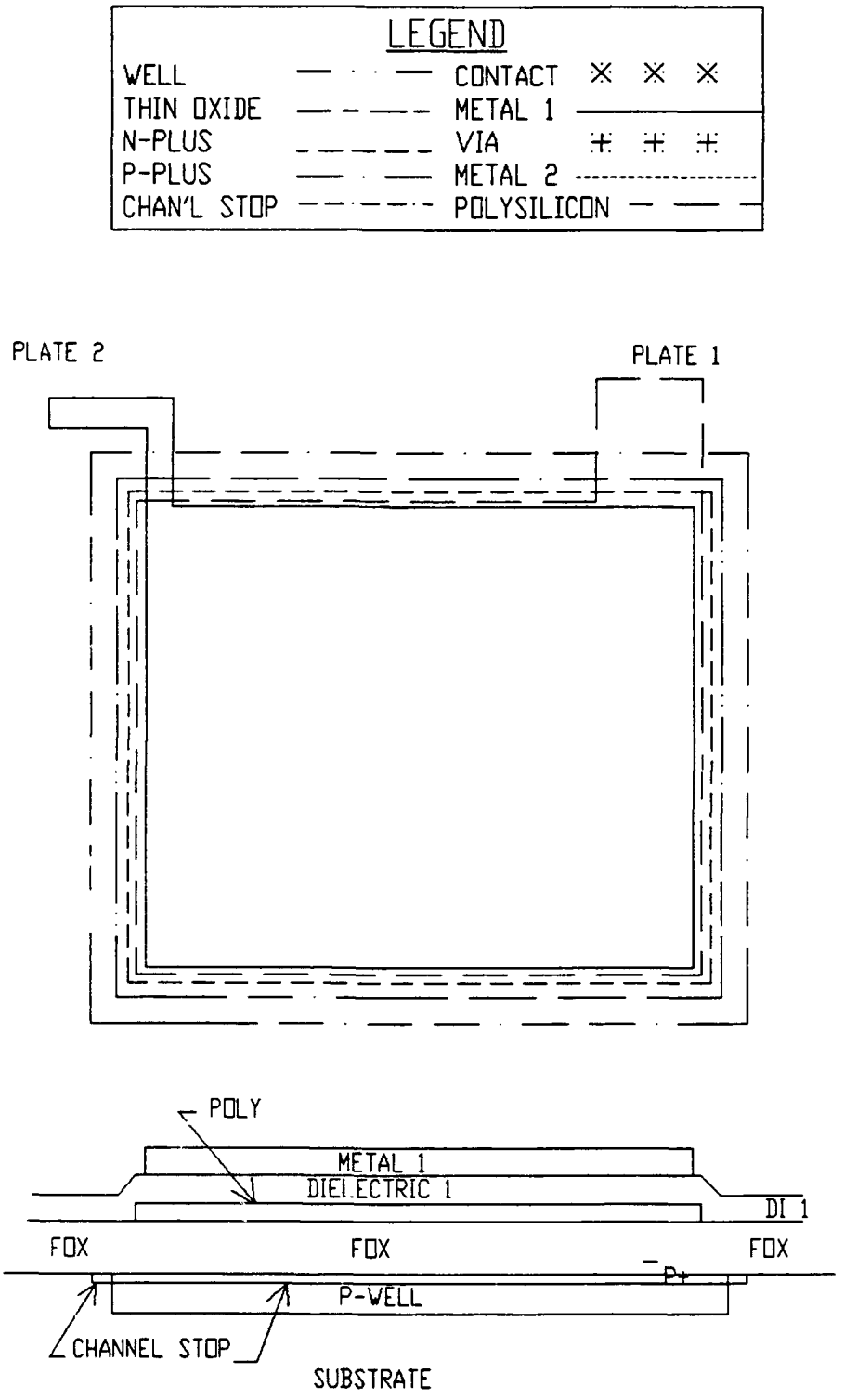
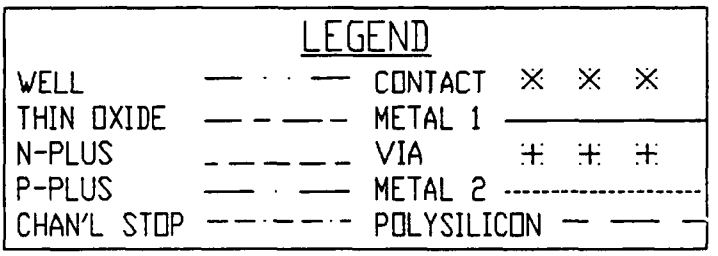


Figure 33. Interlevel dielectric capacitor with minimum aspect ratio.



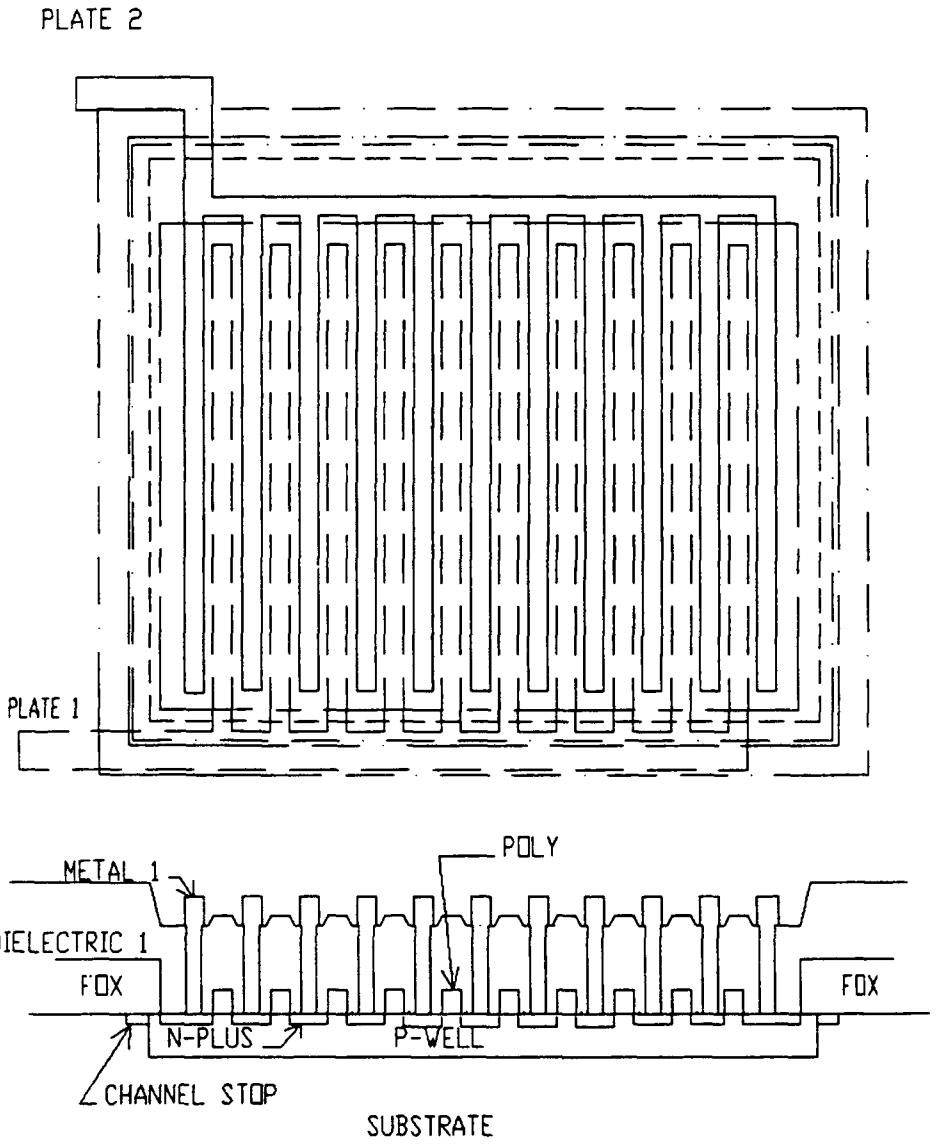


Figure 34. Fringing field capacitor test structure for metal-1/poly.

7. TRENCH STRUCTURES

7.1 Introduction

The use of trench isolation is becoming an increasingly popular method for lateral isolation of devices. The trench is formed by reactive ion etching into the silicon substrate. A thermal oxide is grown around the bottom and sidewalls of the trench. Then it is backfilled with polysilicon or a deposited glass. The polysilicon may or may not be doped. If it is doped, the polysilicon is often connected to a bonding pad and biased. Ionizing radiation causes positive charge to be trapped in the oxide. This may be sufficient to invert the interface along the trench sidewalls and bottom and cause a leakage path from one isolation area to the next [78–80].

7.2 Double-Trench FET Array

7.2.1 Purpose

The double trench FET, as shown in figure 35, is used to investigate leakage between isolation regions for technologies which use a trench to isolate each active device. This results in two trenches between each pair of devices.

7.2.2 Description

This device consists of two separately trenched isolation regions running side by side. Implants have been made into the isolation regions so that ohmic contacts can be made. The array consists of

1. variations in trench spacing,
2. structures with and without a gate over the trench region, and
3. the location of the substrate contact with respect to the trench.

Width of the structures is determined by typical design dimensions for the isolation regions. If the process permits a trench contact, a pad is provided for trench bias.

7.2.3 Special Design Considerations

The trench FET's should have separate pads for source, drain, and gate. Total dose effects in these structures are a strong function of bias. Several bias conditions may be evaluated simultaneously during an irradiation if enough independent pads are provided.

7.2.4 Applications

Investigations on some trench technologies have shown worst-case bias to be achieved when the isolation region on each side of the trench is biased. This appears to be of more importance than bias on the top gate. Some investigations have shown that worst-case leakage has occurred when there is no top gate included in the structure. Trench isolation is a relatively new technology. The designer may wish to include a number of variations to help in determining design rules.

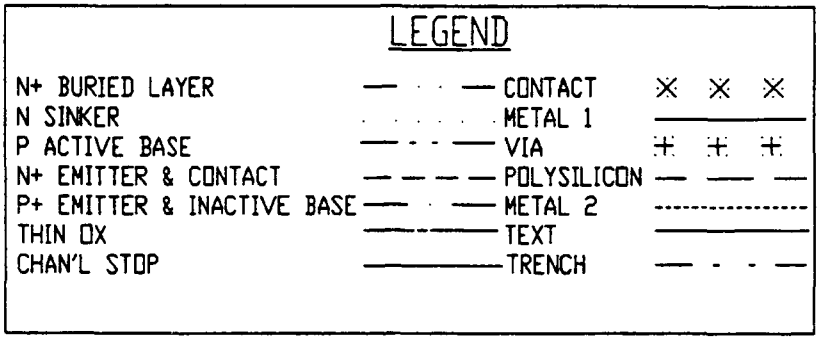
7.3 Single-Trench FET Array

7.3.1 Purpose

The single-trench FET, as shown in figure 36, is used to investigate leakage between isolation regions for technologies which use a single trench for isolation between active devices.

7.3.2 Description

This device consists of two isolation regions separated by a single trench. Implants have been made into the isolation regions so that ohmic contacts can be made. The array consists of structures with and without a gate over the



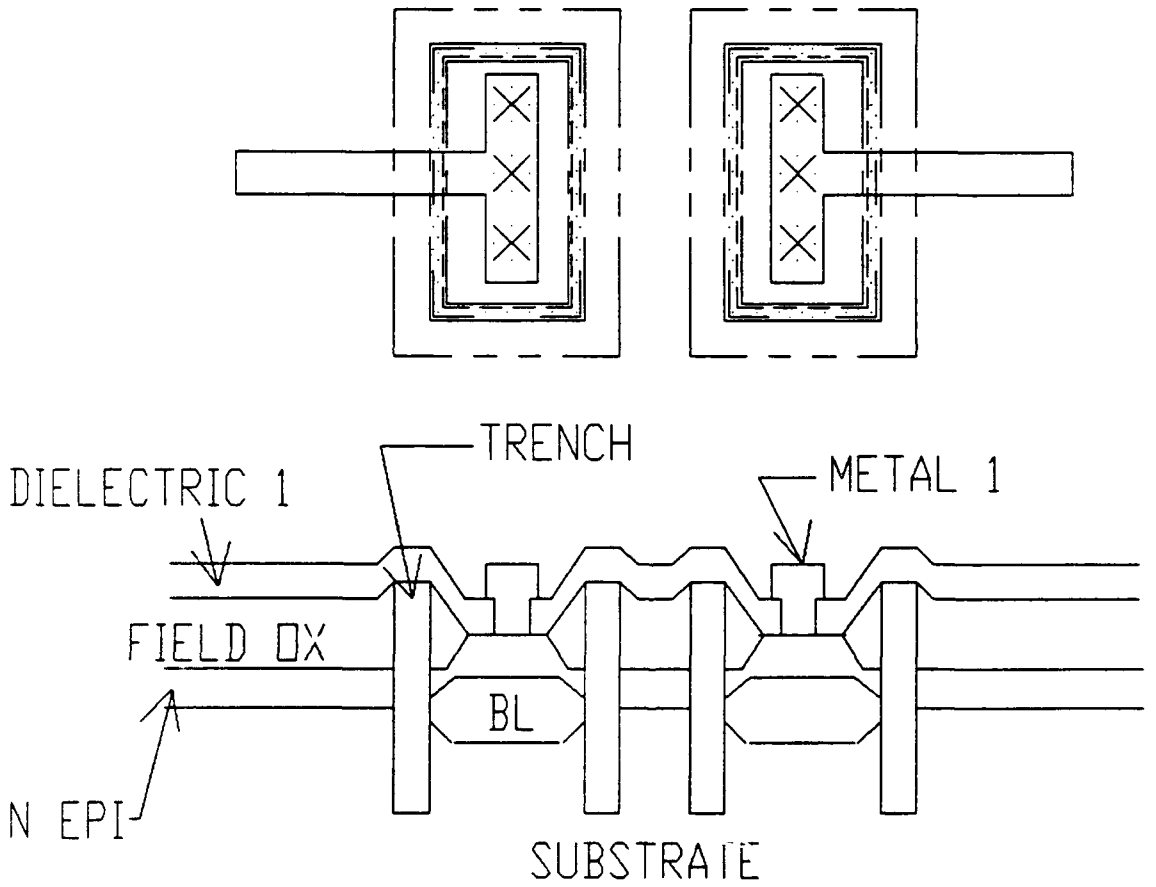


Figure 35. Double-trench FET test structure.

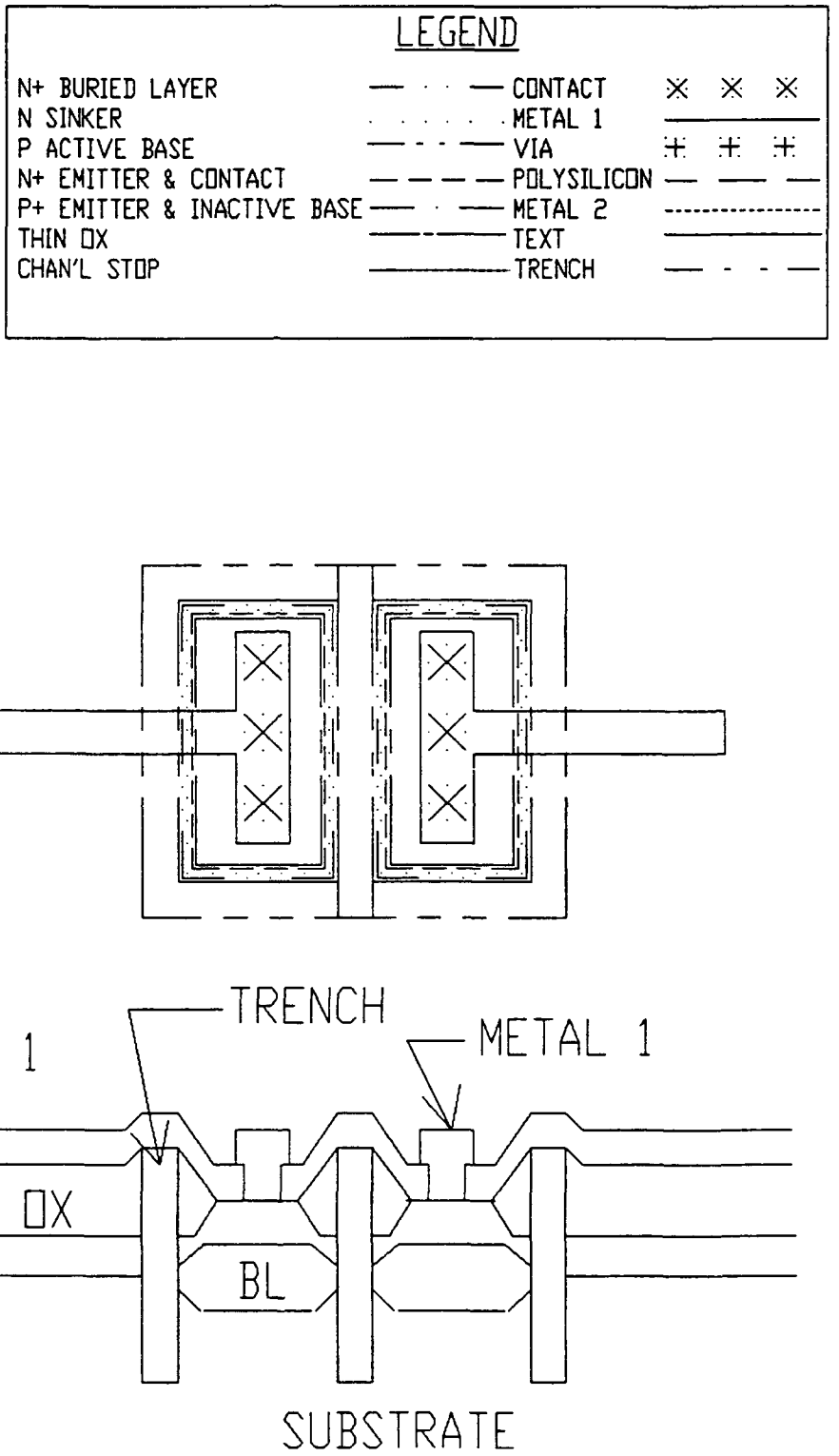


Figure 36. Single-trench FET test structure with and without gate.

trench region. Width of the structures is determined by typical design dimensions for the isolation regions. If the process permits a trench contact, a pad is provided for trench bias.

7.3.3 Special Design Considerations

The trench FET's should have separate pads for source, drain, and gate. Total dose effects in these structures are a strong function of bias. Several bias conditions may be evaluated simultaneously during an irradiation if enough independent pads are provided.

7.3.4 Applications

Investigations on some trench technologies have shown worst-case bias to be achieved when the isolation region on each side of the trench is biased. This appears to be of more importance than bias on the top gate. Some investigations have shown that worst-case leakage has occurred when there is no top gate included in the structure. Trench isolation is a relatively new technology. The designer may wish to include a number of variations to help in determining design rules.

7.4 Trench Array

7.4.1 Purpose

The trench array as shown in figure 37 is used to investigate leakage between isolation regions located at a variety of angles and with various amounts of top gate material extending over the trench region [81].

7.4.2 Description

Depending on the technology, this device may use either double or single trenching. The intent is to position isolation regions in an array similar to that expected in a real design. Implants are placed into each isolation region so that ohmic contacts can be made. The array consists of structures with and without a gate over the trench region. Width of the structures is determined by typical design dimensions for the isolation regions. If the process permits a trench contact, a pad is provided for trench bias.

7.4.3 Special Design Considerations

In this array only one gate pad is provided, but separate pads are provided for each isolation region being used as a drain.

7.4.4 Applications

The use of this array permits evaluation of end-to-end leakage and diagonal leakage as well as the long edge leakage evaluated in previous structures.

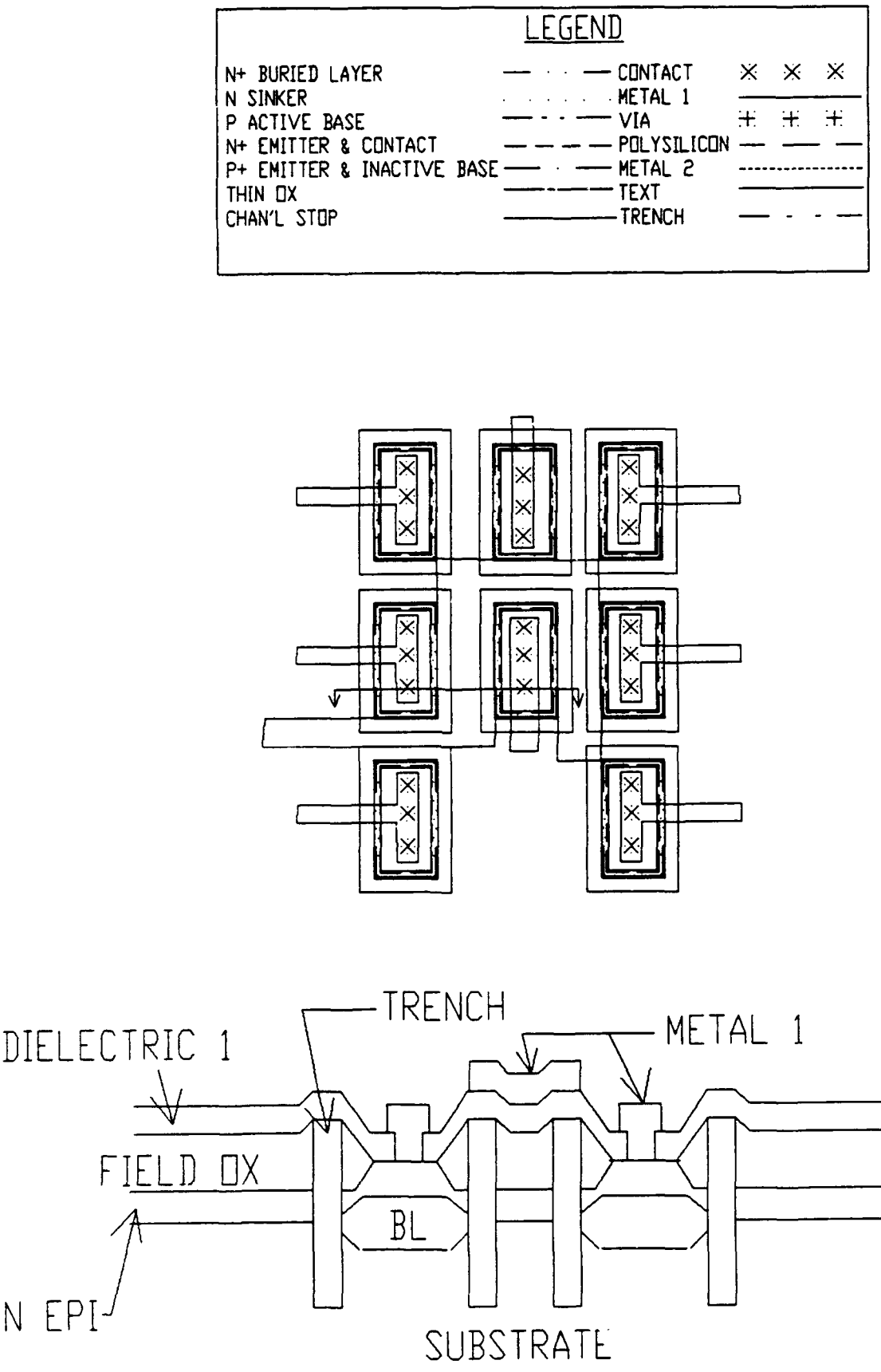


Figure 37. Trench array test structure.

8. SOI STRUCTURES

8.1 Introduction

Silicon-on-insulator (SOI) technology employs a thin layer of single crystalline silicon on top of a buried insulator of silicon dioxide. Although a relatively new technology, SOI offers great promise for high performance microcircuits with greatly improved dose rate and single event upset rates. If appropriate design rules are followed, this technology should also eliminate latchup. However, several questions remain to be answered with respect to total-dose-induced sidewall and back channel leakage [82], [83], [85], [86].

8.2 Epi/Oxide/Substrate Capacitor

8.2.1 Purpose

The epi/oxide/substrate capacitor, as shown in figure 38, is used to evaluate total dose effects on the back channel insulating oxide [84].

8.2.2 Description

The device consists of an isolation region with implants to ensure an ohmic contact to metal-1. The die substrate forms the other plate of the capacitor.

8.2.3 Special Design Considerations

The isolation region must be sized large enough to yield a capacitance value large enough to measure. Typically, values of approximately 5 pF are sufficient. The area scaling can be determined once the target thickness of the insulating oxide has been selected by the processing engineer.

8.2.4 Applications

Standard capacitance/voltage measurement techniques can be used to evaluate threshold voltage changes as a function of total dose.

8.3 SIM Target

8.3.1 Purpose

The SIM (scanning ion microprobe) target, as shown in figure 39, is used to characterize the quality of the backside silicon dioxide insulating layer.

8.3.2 Description

The SIM target is a large rectangle of unimplanted field material. The target should be at least 100 mil square.

8.3.3 Special Design Considerations

A region in the saw kerf may be used if the kerf is not taken up with process control structures.

8.3.4 Applications

At present, the SIMOX (silicon implanted with oxygen) is the most widely used method for fabricating SOI material. This process has historically included a large percentage of heavy metal contaminants in the insulating silicon dioxide matrix. These contaminants have an adverse effect on leakage performance both pre- and post-irradiation. Therefore, SIM targets have been included on many SOI test wafers for diagnostics. The SIM procedure is destructive.

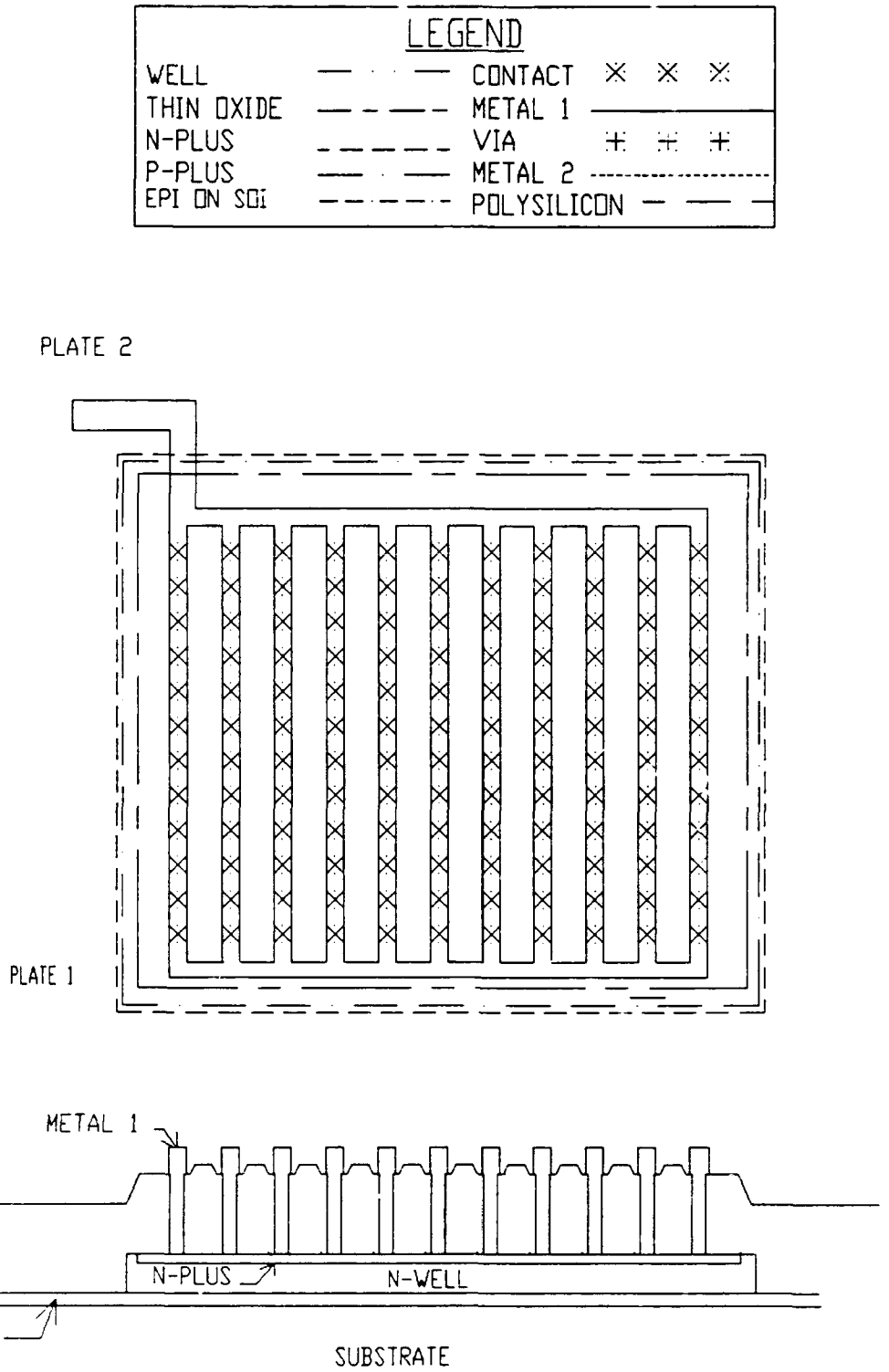


Figure 38. Buried oxide capacitor test structure.

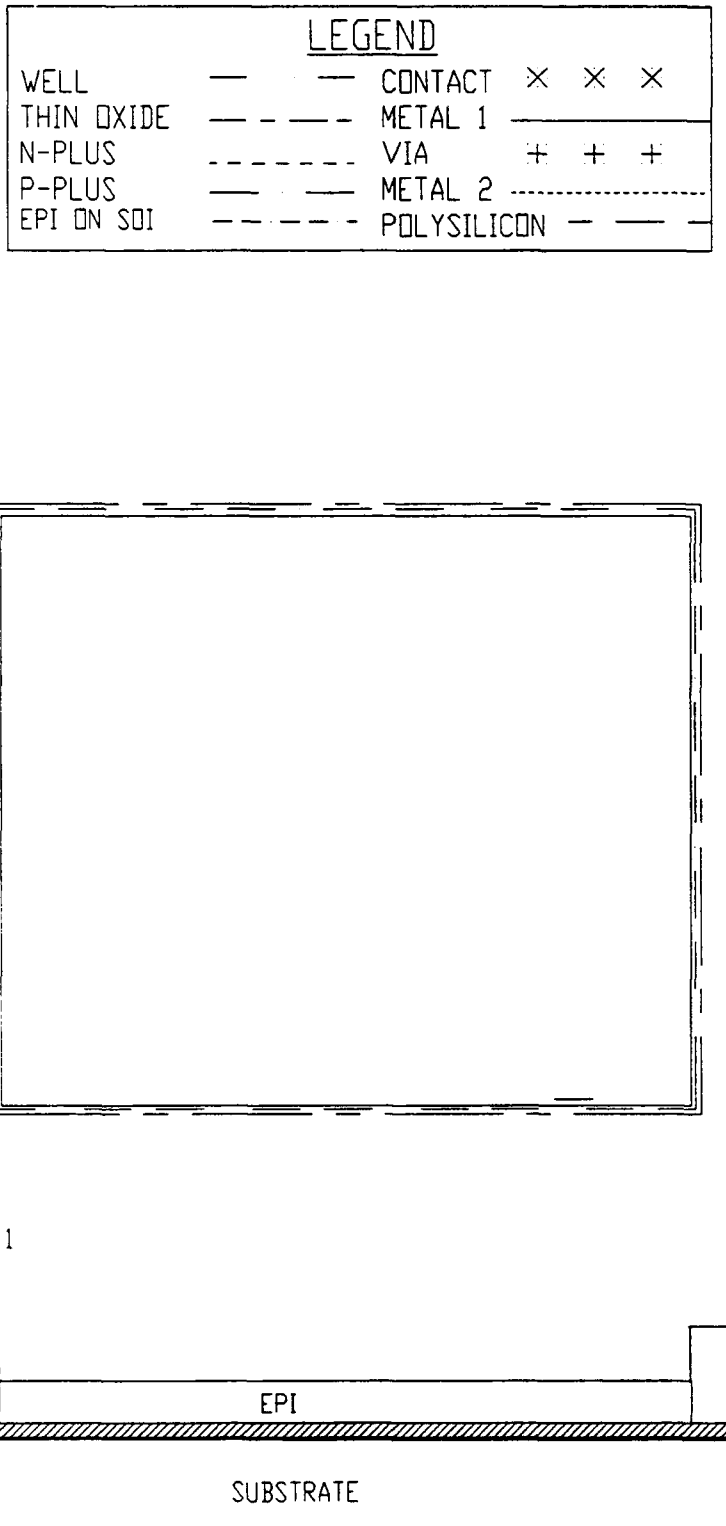


Figure 39. Scanning ion microprobe (SIM) test structure.

9. RADIATION-SENSITIVE PARASITIC DEVICES

9.1 Introduction

In bulk and epitaxial substrate CMOS technologies, the response of parasitic substrate devices is the primary determining factor for upset and latchup in dose rate and SEU environments. The devices discussed in this section may be used to determine photocurrent amplitudes as a function of dose rate and to identify design rules and hardening procedures. The designer should estimate the photocurrent expected from the test structure [87] and confer with the test engineer to assure that the signal will be large enough to measure.

9.2 Photodiode—Unguarded Drain/Substrate with Minimum Aspect Ratio

9.2.1 Purpose

The drain/substrate photodiode, as shown in figure 40, is used to determine maximum primary photocurrent collection as a function of dose rate.

9.2.2 Description

This photodiode is typically a square or circular device with dimensions selected to yield a measurable photocurrent an order of magnitude below the expected upset threshold. For design purposes, assume that the photocurrent is 6.4 $\mu A/cm^3/rad(Si)/s$ per cubic centimeter per rad(Si)/s. The collection volume is the area of the diode times the vertical collection distance under it. The vertical collection depth is the depletion layer width plus a diffusion length into the bulk material. For epi processes, the vertical depth is limited to approximately the thickness of the epi material. A photocurrent of 10 mA can usually be measured accurately at most simulators if reasonable care is taken in the test fixture design.

9.2.3 Special Design Considerations

The diode should be separated from any adjacent device or substrate contact by two diffusion lengths. Since photocurrent is also collected laterally, the measurement should not be complicated by having two structures compete for the same collection volume. Care should be taken to ensure enough contacts to the drain diffusion portion of the diode. The packaged devices must have backside contacts to the substrate. That contact should yield a low contact resistance.

9.2.4 Applications

This structure will be used to determine the maximum photocurrent that can be collected at a drain node. Photocurrent measurements should be made as a function of radiation pulse width in order to determine maximum collection volume and to identify the pulse width scaling factors appropriate for the technology.

9.3 Photodiode—Guarded Drain/Substrate with Minimum Aspect Ratio

9.3.1 Purpose

The drain/substrate photodiode, as shown in figure 41, is used to determine primary photocurrent collection as a function of dose rate for a device with a laterally restricted collection volume.

9.3.2 Description

This photodiode is typically a square or circular device with dimensions selected to yield a measurable photocurrent an order of magnitude below the expected upset threshold. The large area center diode is surrounded by a drain diode ring which is also brought out to a contact pad. Spacing between the two diodes is

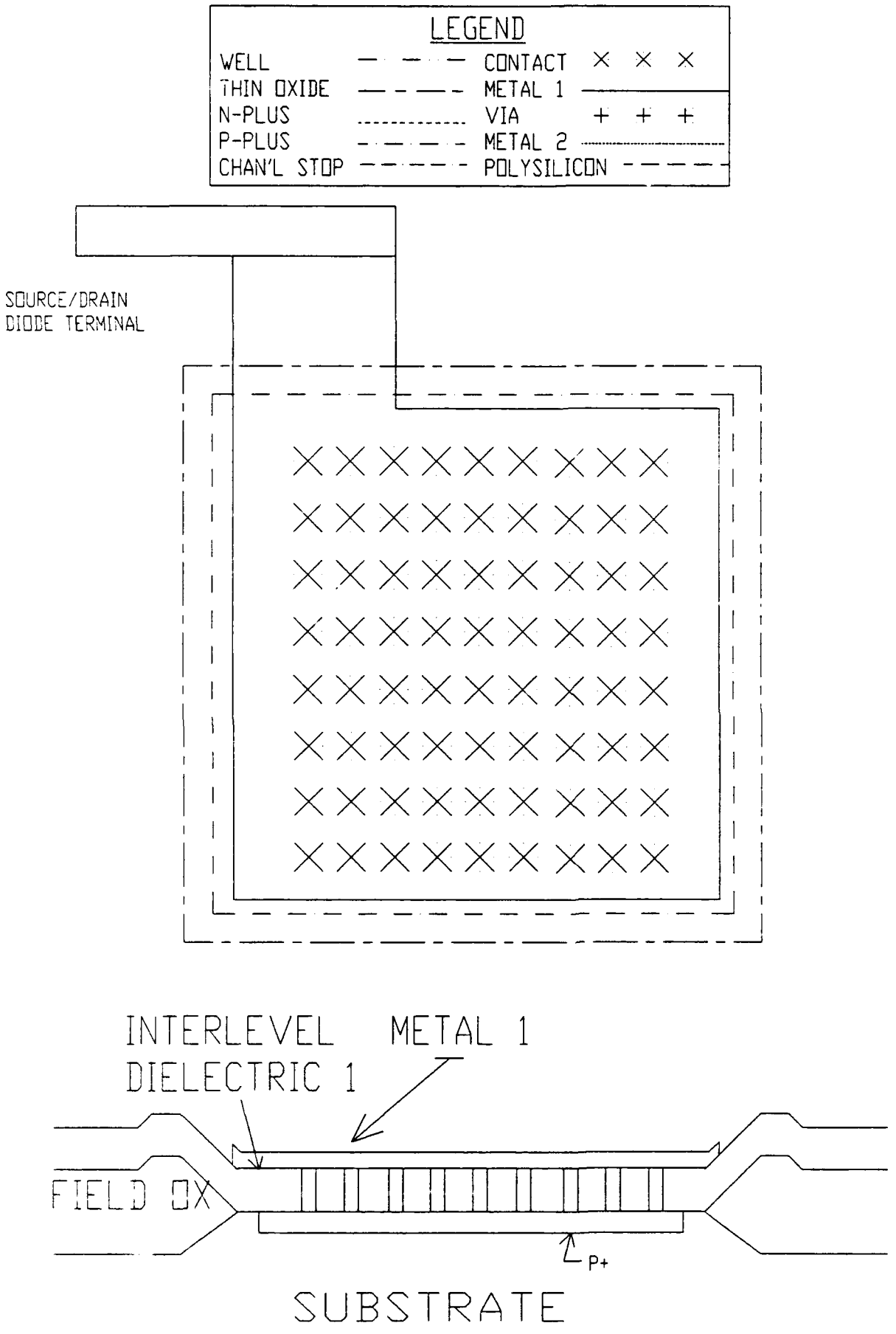


Figure 40. Minimum-aspect-ratio drain/substrate photodiode with no guardband.

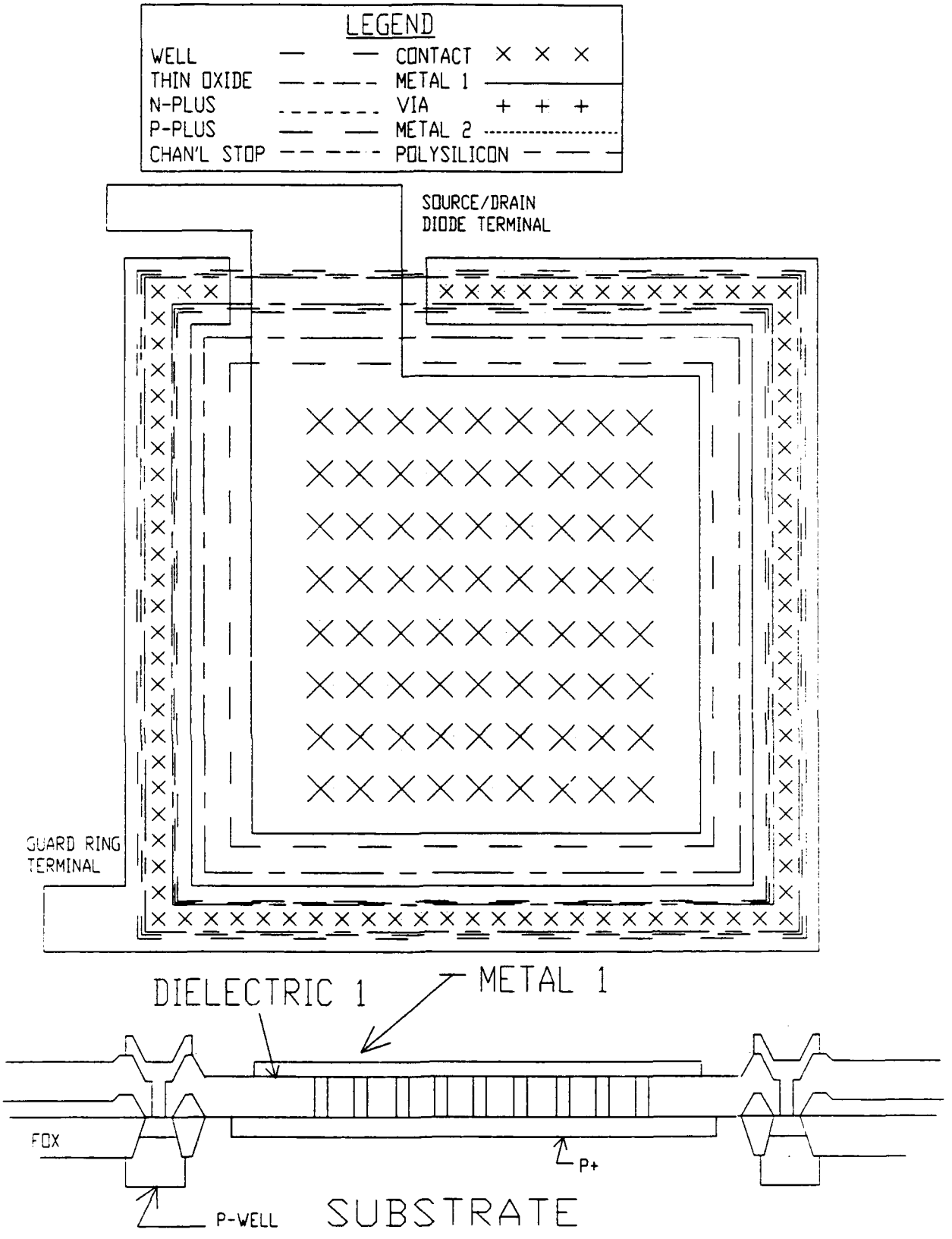


Figure 41. Minimum-aspect-ratio drain/substrate photodiode with guardband.

the minimum separation between adjacent drain implants. Other spacings may be included for design rule investigations. Width of the ring should be at least the minimum width of a drain implant. Wider rings may also be investigated. The dimensions of the inner diode should be identical to structure 9.2.

9.3.3 *Special Design Considerations*

The structure should be separated from any adjacent device or substrate contact by two diffusion lengths. Since photocurrent is also collected laterally, the measurement should not be complicated by having two structures compete for the same collection volume. Care should be taken to ensure enough contacts to both drain diffusion portions of the diode. The packaged devices must have backside contacts to the substrate. That contact should yield a low contact resistance.

9.3.4 *Applications*

This structure will be used to separate the lateral component of photocurrent from the vertical component. The surrounding ring will intercept lateral photocurrents and prevent them from reaching the inner diode ring. There is a possibility of parasitic transistor action between the inner diode and the surrounding diode ring. By biasing the two at different voltage (V_{ss} for one and V_{dd} for the other), the dose rate threshold for parasitic transistor action can be determined.

9.4 *Photodiode—Unguarded Drain/Substrate with Large Aspect Ratio*

9.4.1 *Purpose*

The drain/substrate photodiode, as shown in figure 42, is used to emphasize the lateral collection component of primary photocurrent as a function of dose rate.

9.4.2 *Description*

This photodiode is typically a rectangular device with the same area as structures 9.2 and 9.3 but with a much larger aspect ratio. This results in a greatly increased periphery and emphasizes the lateral photocurrent component. A factor of 10 increase in periphery in comparison to structures 9.2 and 9.3 is a reasonable design goal.

9.4.3 *Special Design Considerations*

The diode should be separated from any adjacent device or substrate contact by two diffusion lengths. Since it will be quite long, the structure may be located near the edge of the die. Care should be taken to ensure enough contacts to the drain diffusion portion of the diode. The packaged devices must have backside contacts to the substrate.

9.4.4 *Applications*

This structure will be used to determine the value of the lateral photocurrent collected by the diode. The measurements made on this structure should be compared with data from devices 9.2 and 9.3 to yield a definitive value for lateral collection.

9.5 *Phototransistor (Drain/Substrate/Well)*

9.5.1 *Purpose*

The drain/substrate/well phototransistor as shown in figure 43 is used to determine the effect of lateral parasitic-transistor action on photocurrent multiplication as a function of dose rate.

9.5.2 *Description*

This phototransistor is an annular lateral bipolar transistor with dimensions se-

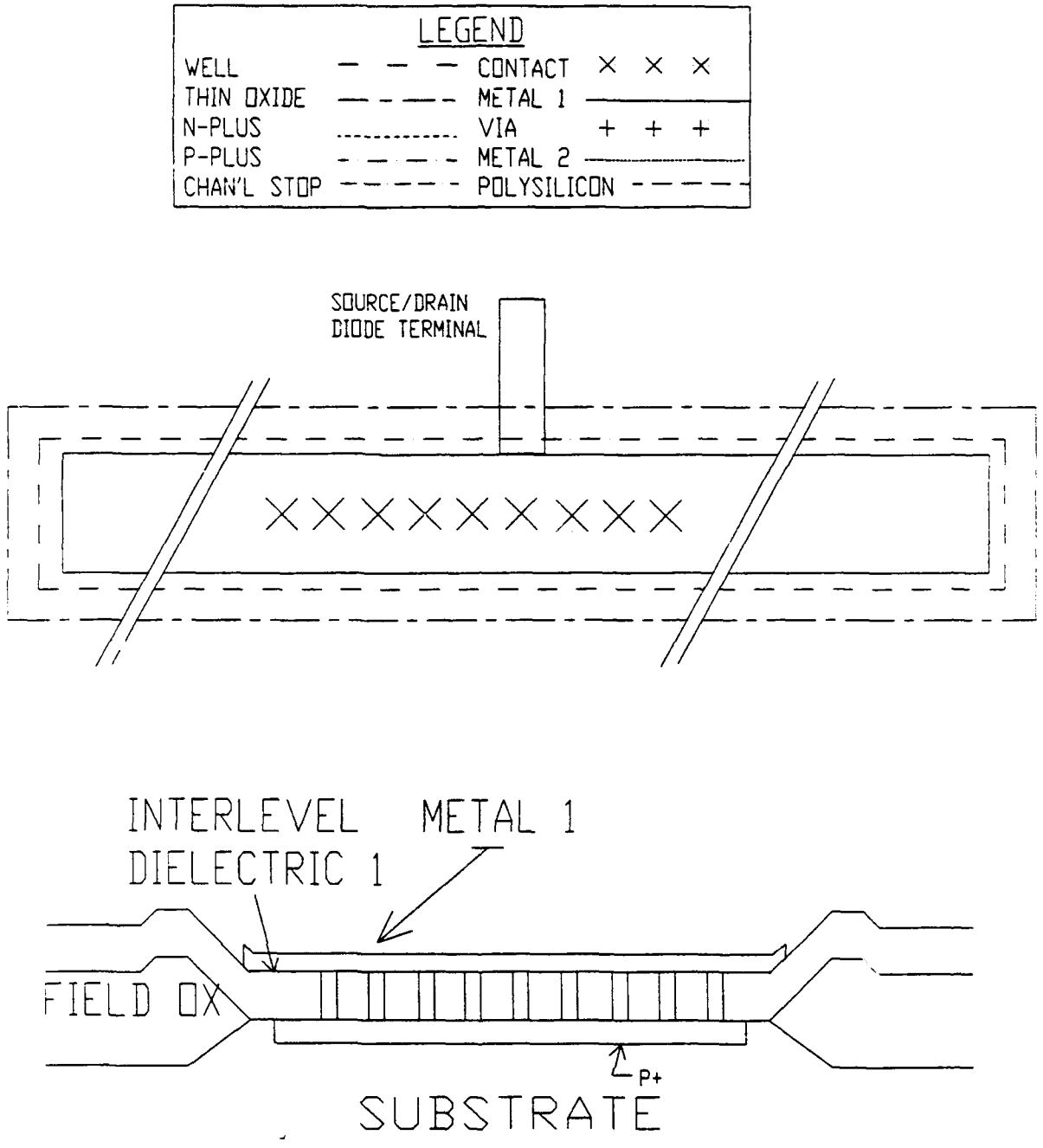


Figure 42. Large-aspect-ratio drain/substrate photodiode with no guardband.

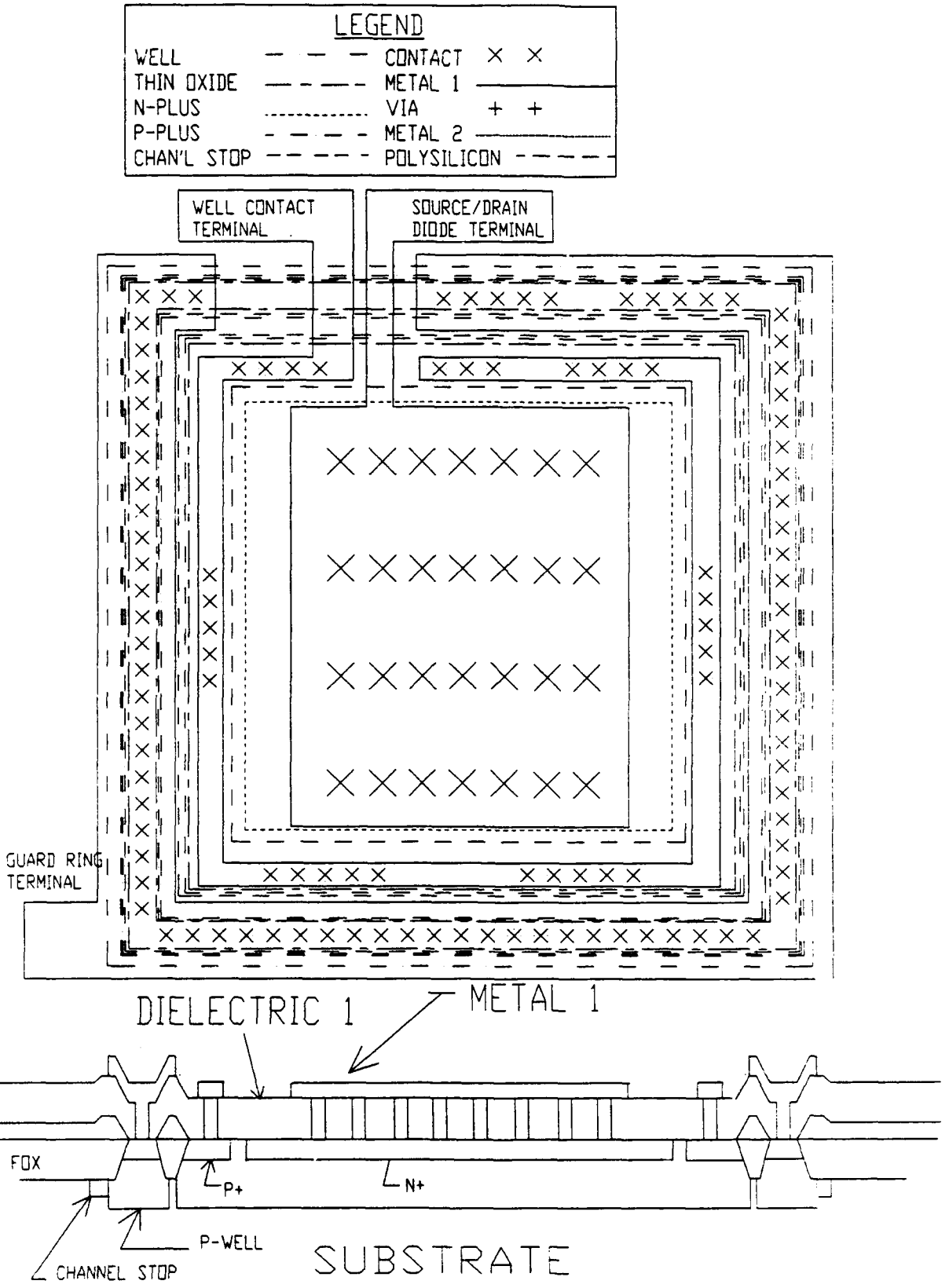


Figure 43. Drain/substrate/well phototransistor.

lected to yield a measurable primary photocurrent an order of magnitude below the expected upset threshold for the technology. The large area center diode is surrounded by a well diode ring which is also brought out to a contact pad. Spacing between the two diodes is the minimum separation between adjacent drain implant and well. Other spacings may be included for design rule investigations. Width of the ring should be enough to accommodate a well contact and a minimum geometry transistor. Wider rings may also be investigated. The dimensions of the inner diode should be identical to structure 9.2.

9.5.3 *Special Design Considerations*

This structure need not be separated from adjacent devices by two diffusion lengths. The photocurrent of interest is that collected directly under the structure, which results in a voltage drop across the parasitic base resistance. Multiple phototransistor structures may be included with variations in spacing and the use of intervening substrate contacts in the region between the drain and well. Care should be taken to ensure enough contacts to both the drain diffusion (emitter) and the well (collector). The packaged devices must have backside contacts to the substrate. That contact should yield a low contact resistance.

9.5.4 *Applications*

This structure will be used to evaluate the photoresponse of the lateral parasitic transistor formed by the drain, substrate, and well. This is one component of the latchup path in bulk CMOS. Evaluation of the photoresponse may yield insight into techniques for prevention of latchup.

9.6 *Photodiode—Unguarded Well/Substrate with Minimum Aspect Ratio*

9.6.1 *Purpose*

The well/substrate photodiode as shown in figure 44 is used to determine maximum primary photocurrent collection as a function of dose rate.

9.6.2 *Description*

This photodiode is typically a square or circular device with dimensions selected to yield a measurable photocurrent an order of magnitude below the expected upset threshold. For design purposes, assume that photocurrent is 6.4 $\mu A/cm^3/rad(Si)/s$ per cubic centimeter per rad(Si)/s. The collection volume is the area of the diode times the vertical collection distance under it. The vertical collection depth is the depletion layer width plus a diffusion length into the bulk material. For epi processes, the vertical depth is limited to approximately the thickness of the epi material below the well. A photocurrent of 10 mA can usually be measured accurately at most simulators if reasonable care is taken in the test fixture design.

9.6.3 *Special Design Considerations*

The diode should be separated from any adjacent device or substrate contact by two diffusion lengths. Since photocurrent is also collected laterally, the measurement should not be complicated by having two structures compete for the same collection volume. Care should be taken to ensure enough contacts to the well diffusion portion of the diode. The packaged devices must have backside contacts to the substrate. That contact should yield a low contact resistance.

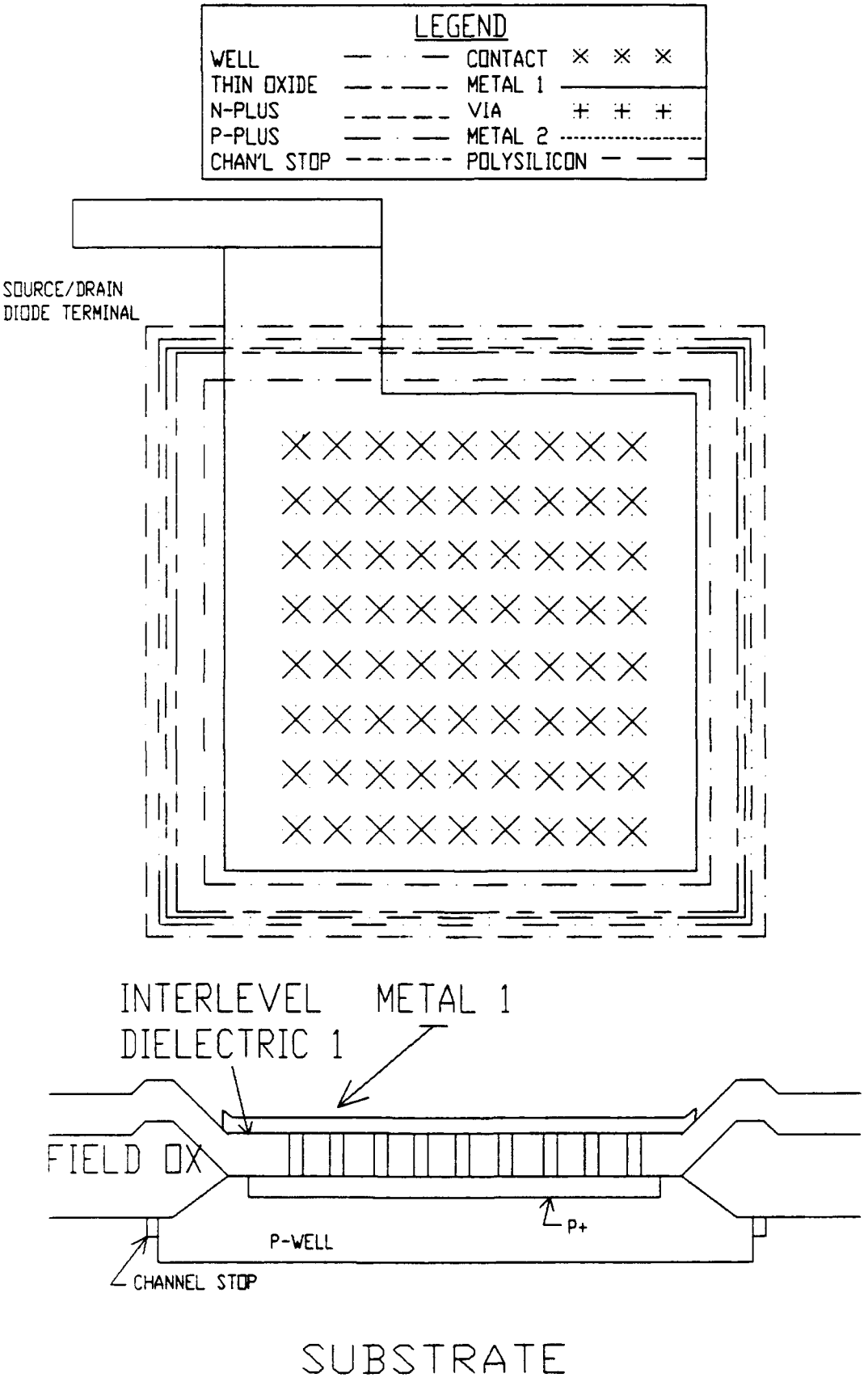


Figure 44. Minimum-aspect-ratio well/substrate photodiode with no guardband.

9.6.4 Applications

This structure will be used to determine the maximum photocurrent that can be collected by a well junction. Photocurrent measurements should be made as a function of radiation pulse width in order to determine maximum collection volume and to identify the pulse width scaling factors appropriate for the technology.

9.7 Photodiode—Guarded Well/Substrate with Minimum Aspect Ratio

9.7.1 Purpose

The well/substrate photodiode as shown in figure 45 is used to determine primary photocurrent collection as a function of dose rate for a device with a laterally restricted collection volume.

9.7.2 Description

This photodiode is typically a square or circular device with dimensions selected to yield a measurable photocurrent an order of magnitude below the expected upset threshold. The large area center diode is surrounded by a well diode ring which is also brought out to a contact pad. Spacing between the two diodes is the minimum separation between adjacent wells. Other spacings may be included for design rule investigations. Width of the ring should be at least the minimum width of a well with a contact and a minimum geometry transistor. Wider rings may also be investigated. The dimensions of the inner diode should be identical to structure 9.6.

9.7.3 Special Design Considerations

The structure should be separated from any adjacent device or substrate contact by two diffusion lengths. Since photocurrent is also collected laterally, the measurement should not be complicated by having two structures compete for the same collection volume. Care should be taken to ensure enough contacts to both well diffusion portions of the diode. The packaged devices must have backside contacts to the substrate. That contact should yield a low contact resistance. A similar structure with a drain ring replacing the well ring may also be included on the test chip to investigate the effectiveness of drain implants in intercepting lateral photocurrents.

9.7.4 Applications

This structure will be used to separate the lateral component of photocurrent from the vertical component. The surrounding ring will intercept lateral photocurrents and prevent them from reaching the inner diode ring. For structures with surrounding drain rings, there is a possibility of parasitic transistor action between the inner diode and the surrounding diode ring. By biasing the two at different voltage (V_{ss} for one and V_{dd} for the other), the dose rate threshold for parasitic transistor action can be determined. Parasitic transistor action is not of so much interest for the well ring structures since wells are always held to the same voltage.

9.8 Photodiode—Unguarded Well/Substrate with Large Aspect Ratio

9.8.1 Purpose

The well/substrate photodiode as shown in figure 46 is used to emphasize the lateral collection component of primary photocurrent as a function of dose rate.

9.8.2 Description

This photodiode is typically a rectangular device with the same area as structures

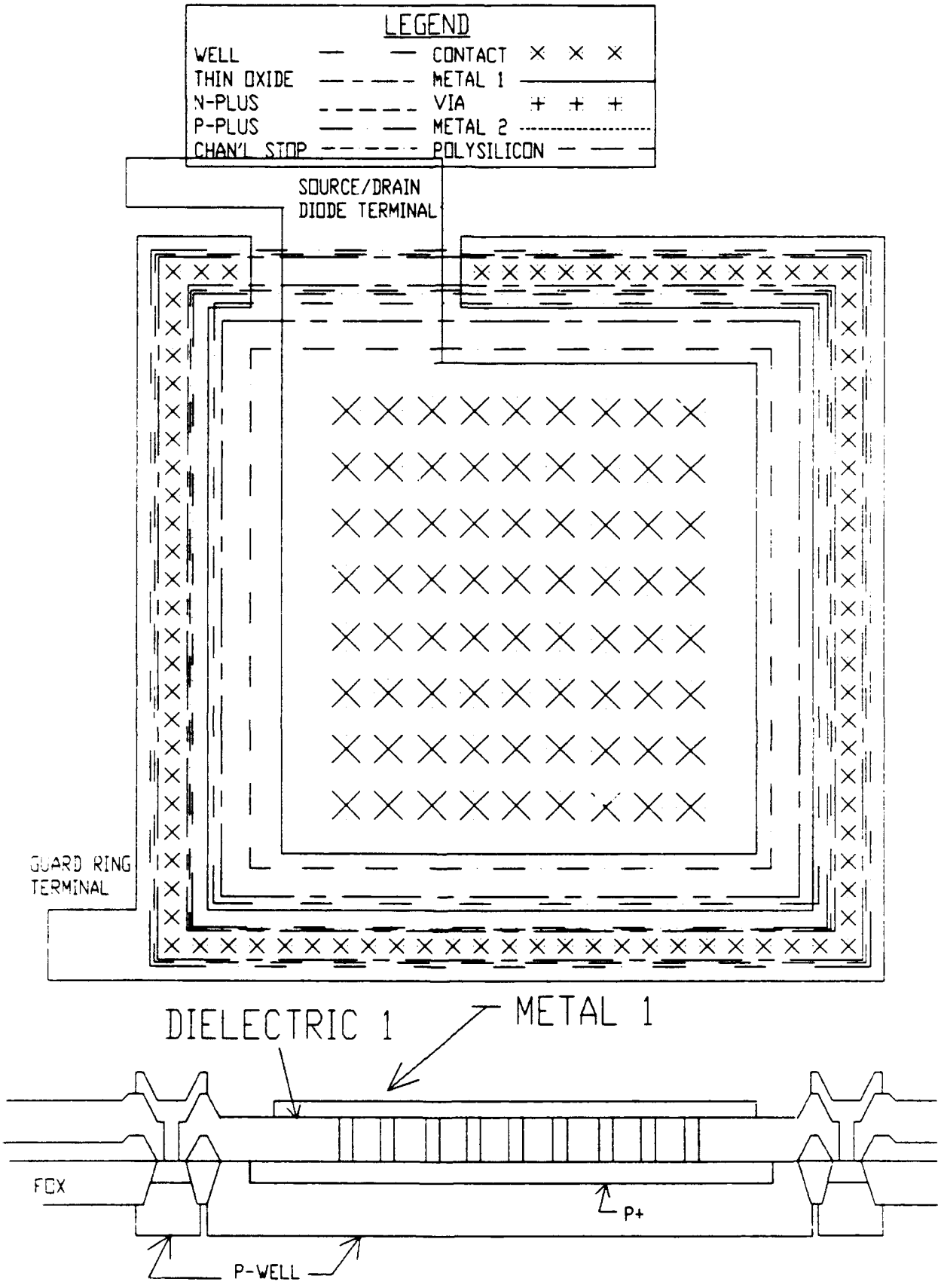
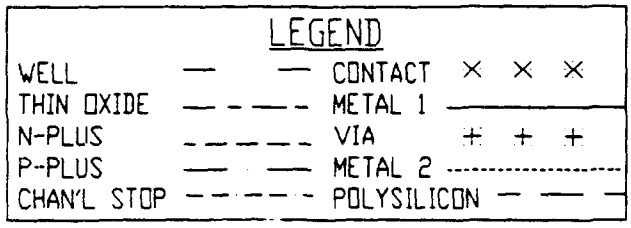
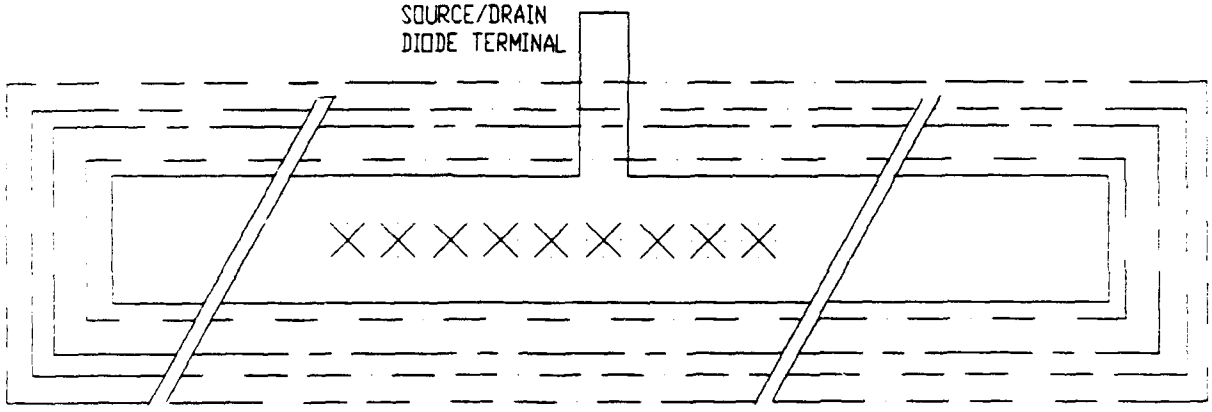


Figure 45. Minimum-aspect-ratio well/substrate photodiode with guardband.





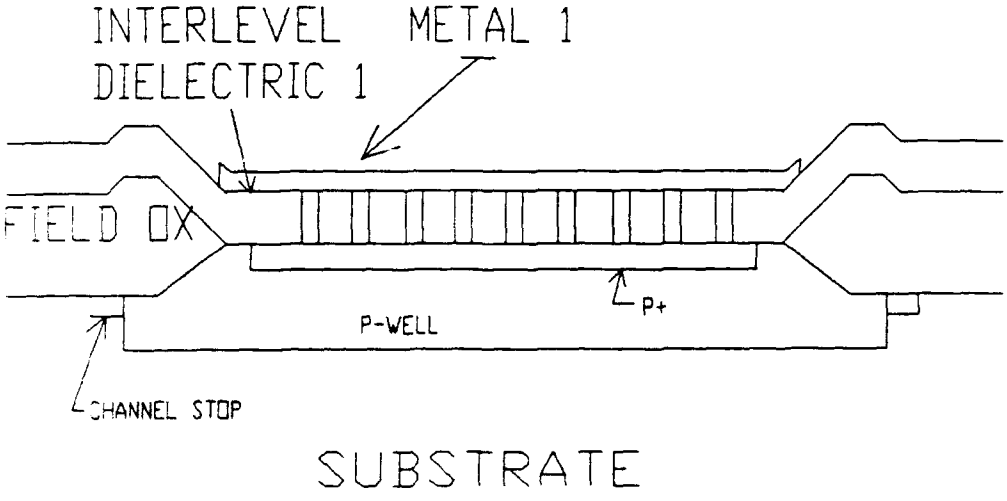


Figure 46. Large-aspect-ratio well/substrate photodiode with no guardband.

9.6 and 9.7 but with a much larger aspect ratio. This results in a greatly increased periphery and emphasizes the lateral photocurrent component. A factor of 10 increase in periphery in comparison to structures 9.6 and 9.7 is a reasonable design goal.

9.8.3 Special Design Considerations

The diode should be separated from any adjacent device or substrate contact by two diffusion lengths. Since it will be quite long, the structure it may be located near the edge of the die. Care should be taken to ensure enough contacts to the well diffusion portion of the diode. The packaged devices must have backside contacts to the substrate.

9.8.4 Applications

This structure will be used to determine the value of the lateral photocurrent collected by the well diode. The measurements made on this structure should be compared with data from devices 9.6 and 9.7 to yield a definitive value for lateral collection.

9.9 Photoconductivity Structure—Epi Island to Epi Island

9.9.1 Purpose

The photoconductivity structure as shown in figure 47 is used to determine the radiation-induced conductivity between adjacent epi islands in an SOS technology [88–89].

9.9.2 Description

This structure consists of interdigitated epi islands with minimum epi to epi spacing. The epi fingers of each side are connected in parallel and brought out to a bonding pad.

9.9.3 Special Design Considerations

Under normal conditions the two sides of the interdigitated structure are electrically isolated. During a pulse of ionizing radiation, the normally insulating substrate becomes conductive, and current flows from one side to the other. Typically, these structures have approximately 10,000 microns of facing surface area. Additional structures may be included with variations in epi island spacing for design rule evaluation.

9.9.4 Applications

During dose rate testing, one side of the epi structure is connected to V_{dd}, the other, to V_{ss}. Current between the two structures is monitored with a current viewing resistor or current probe. The radiation-induced currents are quite small, and care must be taken to account for noise from air ionization and the package.

9.10 Photoconductivity Structure—Poly-to-Poly Interconnect

9.10.1 Purpose

The photoconductivity structure as shown in figure 48 is used to determine the radiation-induced conductivity between adjacent polysilicon interconnect runs in an SOS technology [88].

9.10.2 Description

This structure consists of interdigitated polysilicon interconnect with minimum poly-to-poly spacing. The poly fingers of each side are connected in parallel and brought out to a bonding pad.

9.10.3 Special Design Considerations

Under normal conditions the two sides of the interdigitated structure are electri-

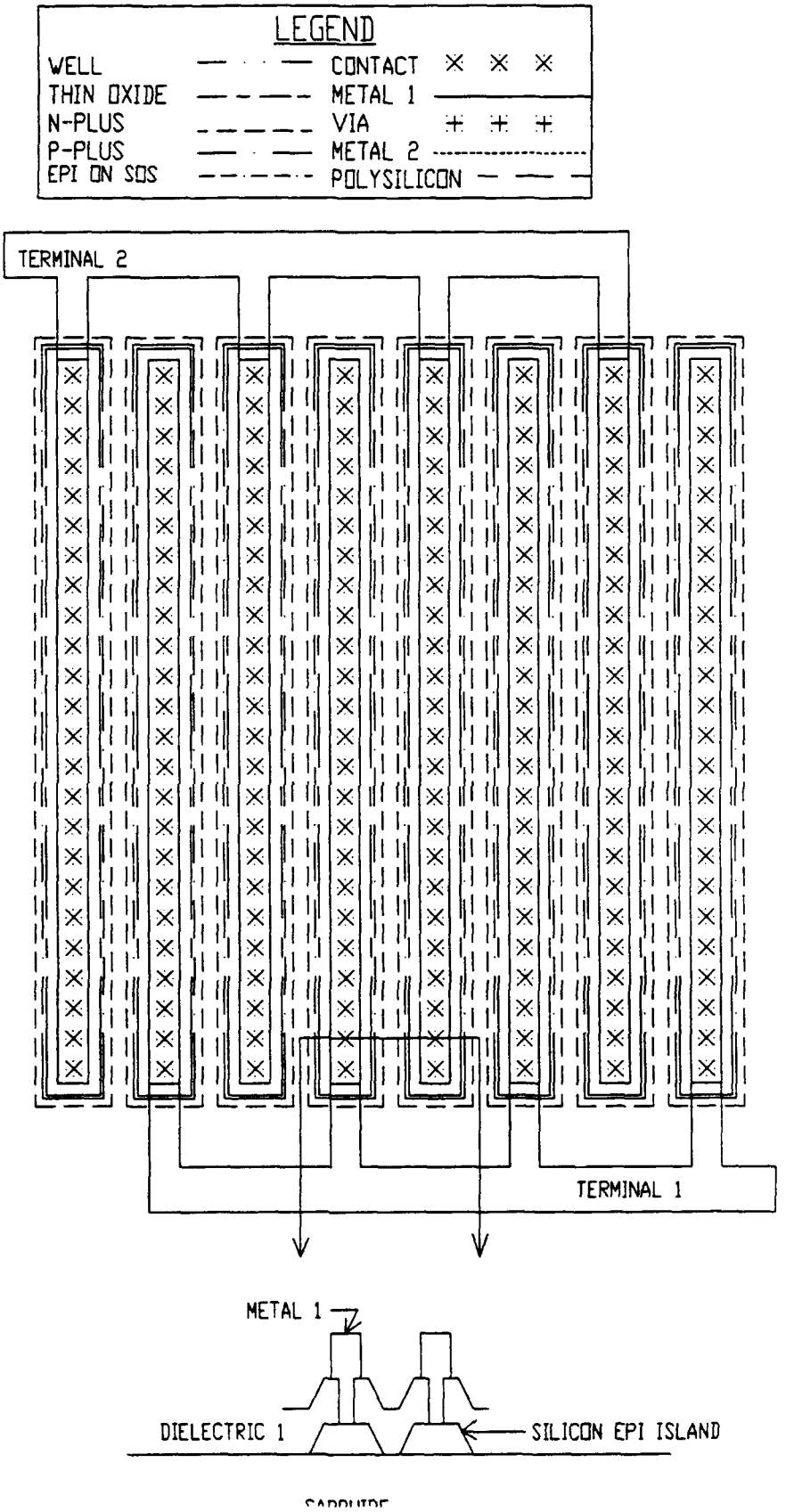


Figure 47. Photoconductivity structure for inter-island conduction in SOS.

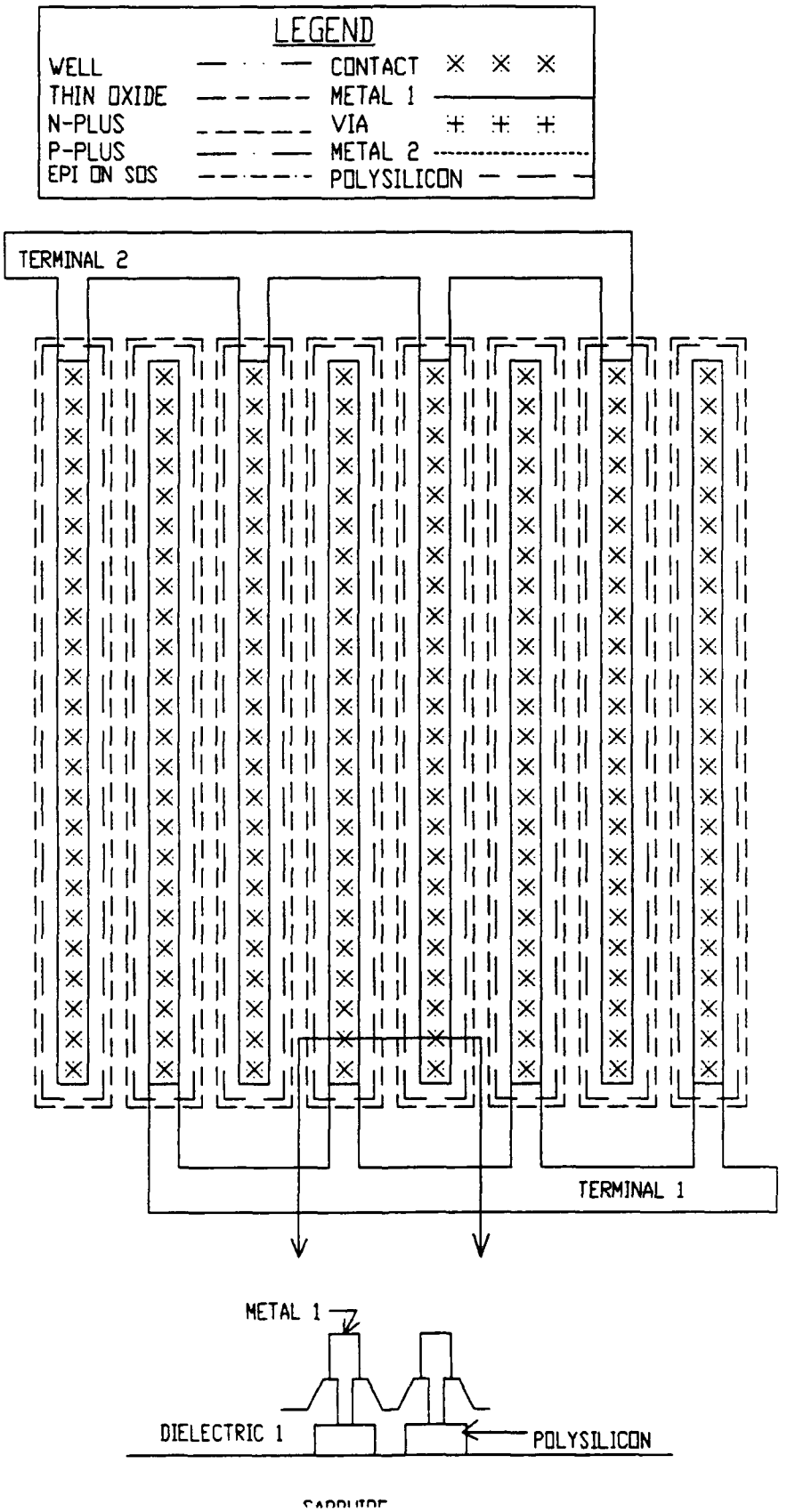


Figure 48. Photoconductivity structure for poly-to-poly interconnect conduction.

cally isolated. During a pulse of ionizing radiation, the normally insulating substrate becomes conductive, and current flows from one side to the other. Typically, these structures have approximately 10,000 microns of facing surface area. Additional structures may be included with variations in polysilicon line spacing for design rule evaluation.

9.10.4 Applications

During dose rate testing, one side of the epi structure is connected to V_{dd}, the other, to V_{ss}. Current between the two structures is monitored with a current viewing resistor or current probe. The radiation-induced currents are quite small, and care must be taken to account for noise from air ionization and the package.

9.11 Photoconductivity Structure—Poly Interconnect to Epi Island

9.11.1 Purpose

The photoconductivity structure as shown in figure 49 is used to determine the radiation-induced conductivity between adjacent polysilicon interconnects and epi islands in an SOS technology.

9.11.2 Description

This structure consists of interdigitated polysilicon interconnect and epi islands with minimum poly to epi spacing. The poly fingers of one side are connected in parallel and brought out to a bonding pad. The epi fingers on the other side are connected in parallel and brought out to a separate pad.

9.11.3 Special Design Considerations

Under normal conditions the two sides of the interdigitated structure are electrically isolated. During a pulse of ionizing radiation, the normally insulating substrate becomes conductive, and current flows from one side to the other. Typically, these structures have approximately 10,000 microns of facing surface area. Additional structures may be included with variations in poly-to-epi spacing for design rule evaluation.

9.11.4 Applications

During dose rate testing, the epi structure is connected to one supply voltage (e.g., V_{dd}). The poly structure is connected to the other (e.g., V_{ss}). Current between the two structures is monitored with a current viewing resistor or current probe. The radiation-induced currents are quite small, and care must be taken to account for noise from air ionization and the package.

9.12 MOS Phototransistor

9.12.1 Purpose

The MOS phototransistor as shown in figure 50 is used to determine to drain photocurrent in SOI and SOS technologies [88].

9.12.2 Description

This device is an extremely wide, multi-edge transistor. Minimum channel length should be used.

9.12.3 Special Design Considerations

SOS and SOI technologies are attractive for radiation-hardened applications because their insulating substrates preclude latchup, and their small charge collection volumes result in high upset thresholds for dose rate and SEU environments [90]. However, they do exhibit some photoresponse, and this structure is designed to determine the values to be used for analyses. It must be used in conjunction with other structures to separate the different components of the photoresponse. These

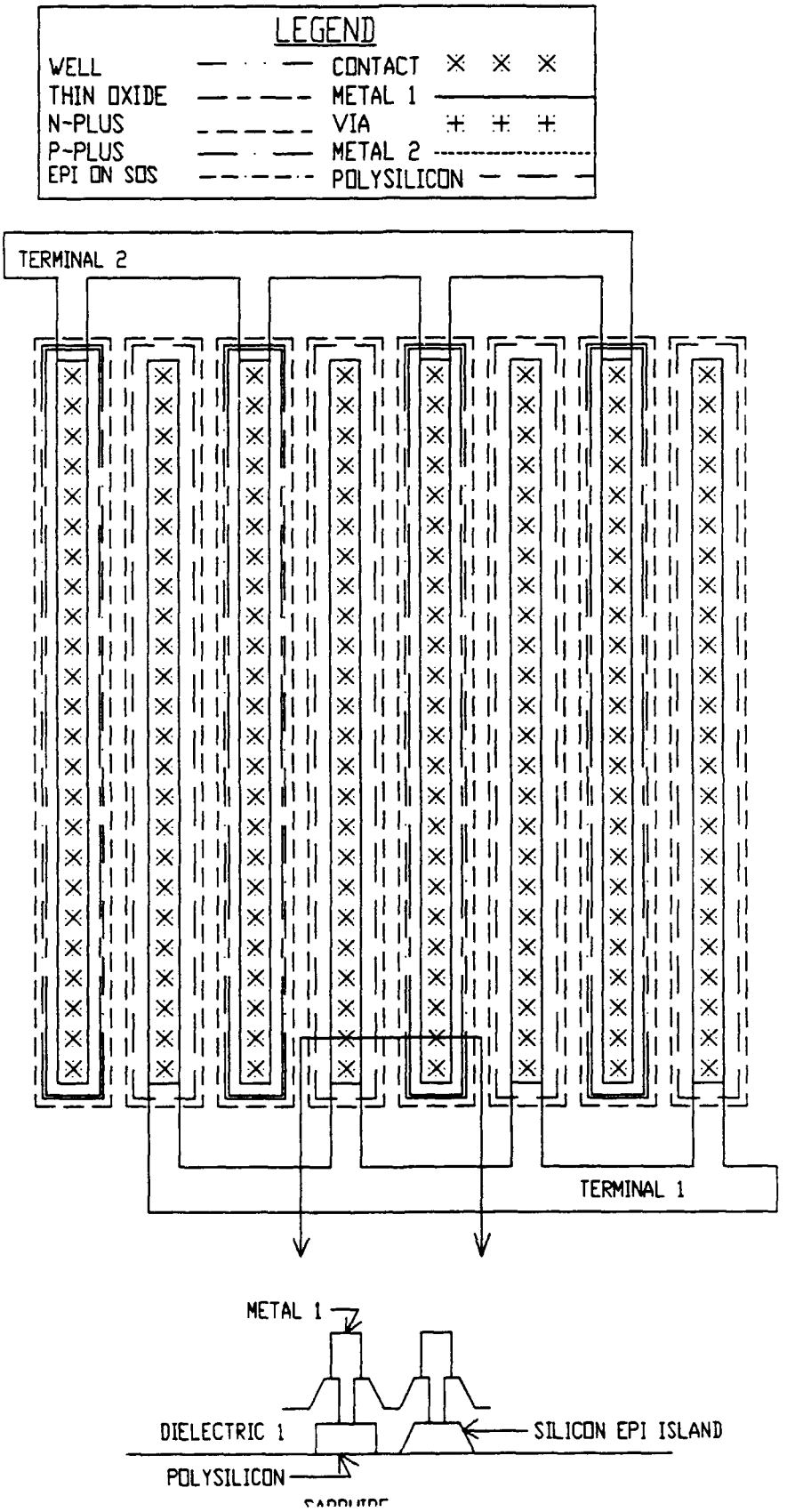


Figure 49. Photoconductivity for poly-interconnect-to-epi island conduction.

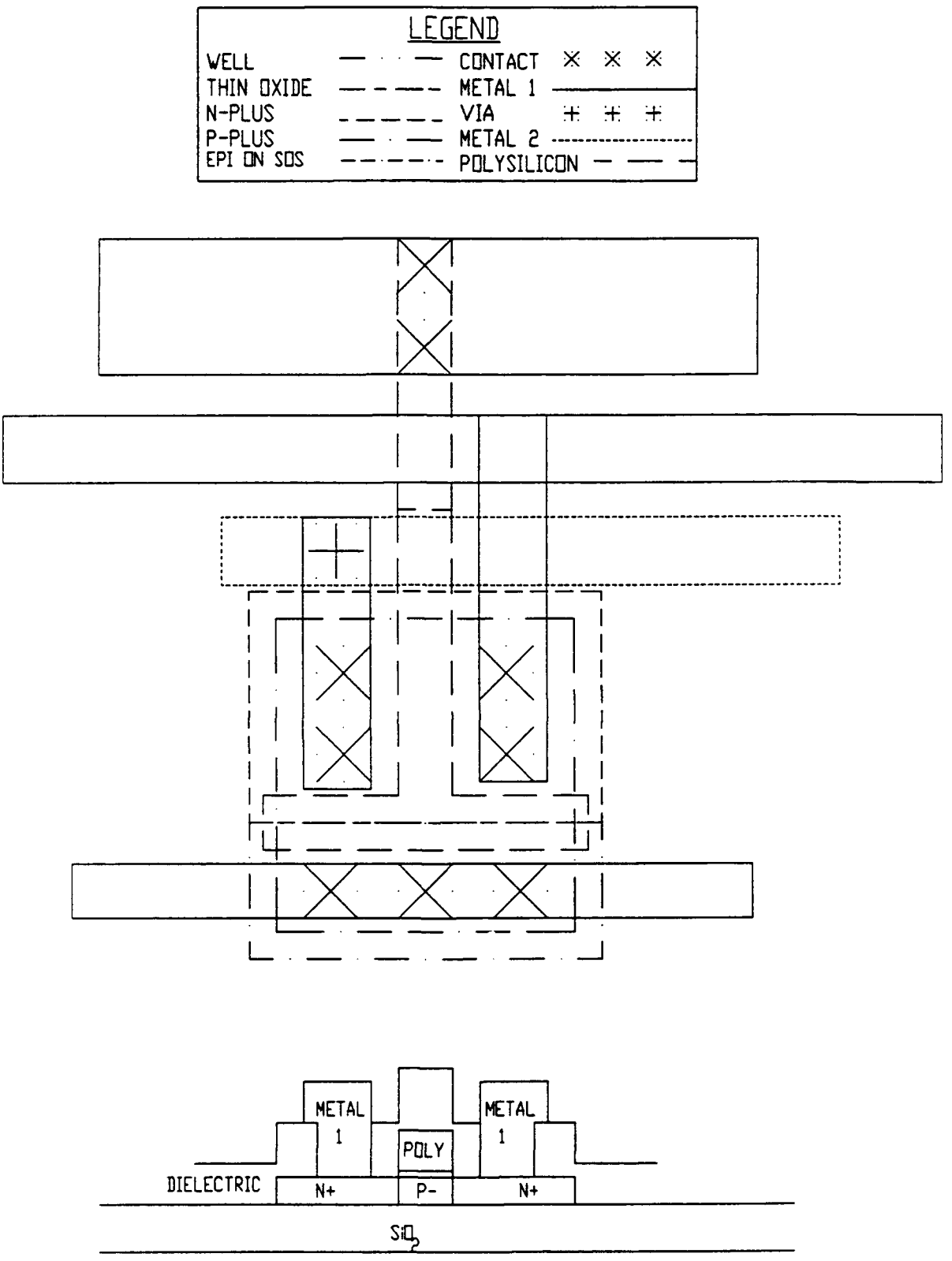


Figure 50. CMOS/SOI parasitic phototransistor.

components include substrate currents, gate currents, and junction photocurrents. In sapphire, the substrate becomes photoconductive during irradiation. Structures in section 9.9 through 9.11 were designed to measure the photoconductivity as a function of dose rate. In technologies which use silicon dioxide as the substrate dielectric (e.g., SIMOX), the electron current through the insulator can contribute a significant fraction of the total photoresponse. This current can be estimated from the following equation [88]:

$$I = qG_{ox}t_{ox}A_{ox}R \qquad (1)$$

where

q	=	electronic charge$(1 \times 10^{-19}$ coulombs/electron$)$
G_{ox}	=	electron generation rate in silicon dioxide $= 1 \times 10^{13}$ e/rad(Si)/s/cm^{-3}
t_{ox}	=	oxide thickness
A_{ox}	=	area of the oxide
R	=	dose rate(rad(Si)/s)

The experimental value of the silicon dioxide substrate insulator is typically determined with a capacitor structure such as the one described in Section 8.2.

Electron current through the gate dielectric can also contribute to the photoresponse. It can also be estimated from the above equation. Measured values are determined from gate oxide capacitor structures such as those in Section 4.12.

The phototransistor structure in this section is subject to ionizing radiation induced currents in both the substrate and gate oxides as well as junction photocurrents. The gate and substrate currents must be subtracted from the total response in order to determine the junction currents. The structure illustrated in the figure is from a SIMOX technology. Consequently, it is shown with a connection between the source and the body of the transistor. In SIMOX, the lifetime of minority carriers in the body can be quite high. This gives rise to a parasitic bipolar transistor with the drain acting as the collector, the body acting as the base, and the source acting as the emitter. The primary photocurrent from the drain to the body can raise the body voltage with respect to the source (emitter) enough to forward bias it and produce secondary photocurrent [90]. The body tie to the source is provided to prevent the body-to-source voltage from exceeding the V_{beon} of the parasitic transistor. The number of body ties required is typically determined by including a number of these devices with different widths between the body-to-source contacts.

In SOS technologies, the minority carrier lifetime in the body is usually very short (unless solid phase epitaxy or a similar process has been used to improve silicon quality). Therefore, body ties are usually not required to prevent secondary photocurrents. (Body ties in SOS may be desirable in some instances to prevent self biasing of the body from modulating the threshold voltage.)

9.12.4 Applications

The photoresponse of this structure will typically be measured at very high dose rates. Precautions will be required to reduce noise to the lowest possible levels.

9.13 SCR Path with Maximum Collection Efficiency

9.13.1 Purpose

The SCR path structure as shown in figure 51 is used to determine the latchup holding voltage and holding current in CMOS technologies. Latchup is an important issue in both commercial and radiation hardened microcircuit technologies. Therefore, designers should review several references before completing the test structures for their process [91–102].

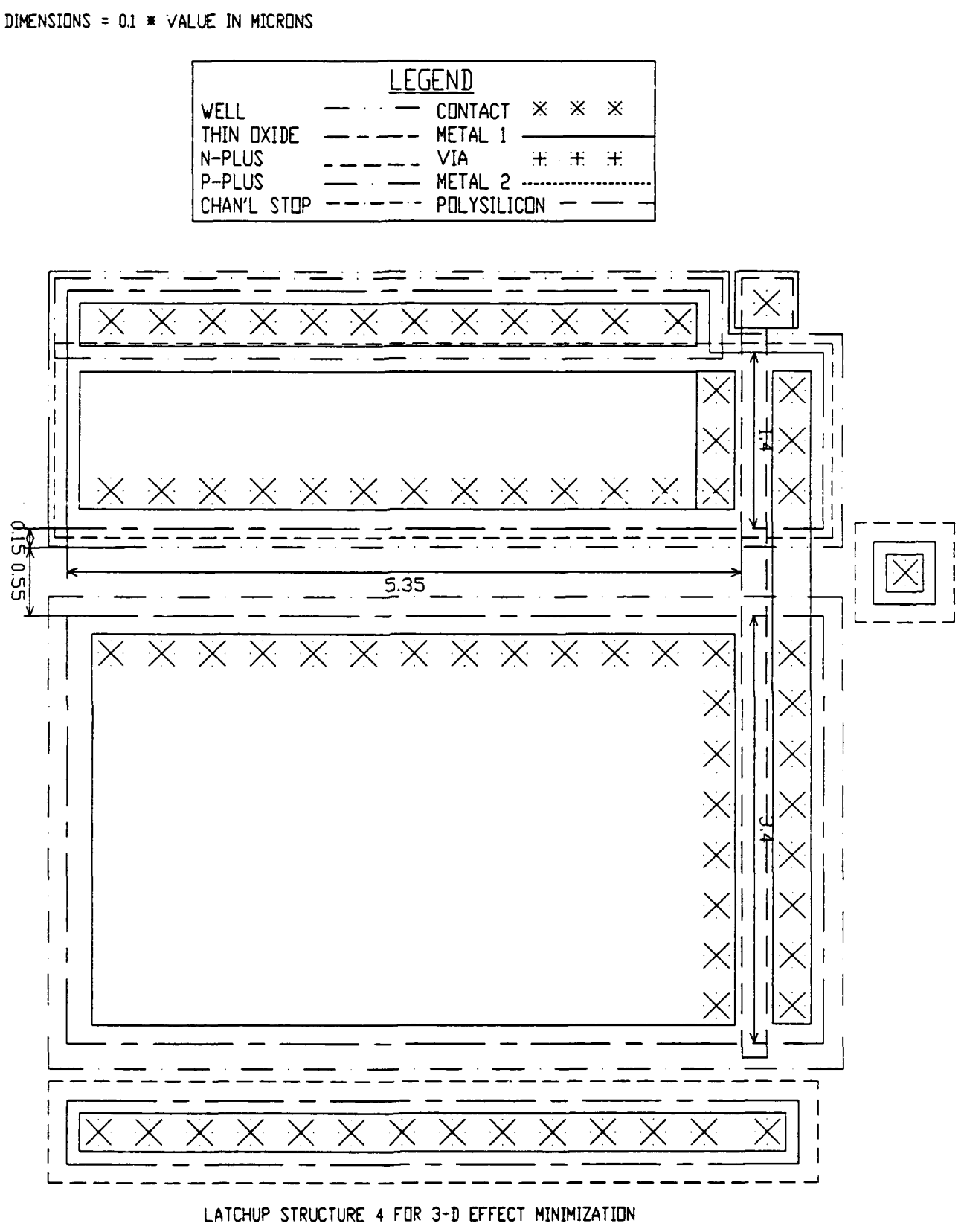


Figure 51. Latchup path configured for maximum collection efficiency.

9.13.2 Description

The latch path simulated involves a source (in well), well, substrate, and source (in substrate). The structure is designed to maximize the amount of junction area involved in the latch path. Typically, the junction regions involved in the latch are at least 25 μm wide. The device should be wide enough to establish essentially two-dimensional current flow. Contacts are provided to the well and substrate. The minimum design rule should be used to determine all spacings. A poly field plate has been included over the latch path to evaluate the effects of vertical field on latchup initiation or holding characteristics. If guardbands are used in the technology, they should be included in the structure. An array of structures may be required to investigate the impact of spacing variations for drain-to-well, contact-to-latch path, guard ring-to-well, and guard ring contact-to-latch path.

9.13.3 Special Design Considerations

Two substrate contacts have been included on either side of the structure so that an aiding electric field can be established across the latch region [101].

9.13.4 Application

For latchup to occur and be sustained in a device the gain product of the parasitic transistors involved in the latch path must be greater than unity. Also, the parasitic resistances associated with the anode and cathode gates must be sufficiently large to permit a V_{beon} drop across them at the currents associated with the holding point. This device is designed to maximize the gain of the parasitic transistors, but it will minimize the shunt resistances. Thus, the failure of this structure to latch (or to have a holding voltage greater than the supply voltage) is a necessary but not sufficient condition for latchup-free operation in a microcircuit. Results of tests on this structure should be considered along with those from device 9.14 in a careful analysis of latchup potential. The design of the microcircuit will have to employ the same design rules for junction spacing and location of substrate and well contacts if the test structures are to truly reflect its latchup susceptibility.

9.14 Path with Maximum Anode and Cathode Gate Resistance

9.14.1 Purpose

The SCR path structure as shown in figure 52 is used to determine the latchup holding voltage and holding current in CMOS technologies.

9.14.2 Description

The latch path simulated involves a source (in well), well, substrate, and source (in substrate). The structure is designed to maximize the resistance between the well and substrate contacts (i.e., anode and cathode gate resistance) and the latch path. The structure shown in the figure was taken for an inverter design. It uses minimum length N-channel and P-channel transistors placed end-to-end. The substrate and well contacts are placed at the extreme ends of the structure. An additional substrate contact has been placed to one side near the location of the latch path. It is used in gain measurements for the parasitic transistors in the latch path, but it is left floating in the holding voltage and current measurements. This device is narrow enough so that three-dimensional current flow is important. If there are other device orientations in either the internal design or the I/O of the microcircuit that would provide a more likely latch path, they should be used as the basis for designing this structure. The minimum design rule should be used to determine all spacings. A poly field plate has been included over the latch path to evaluate the effects of vertical field on latchup initiation or holding

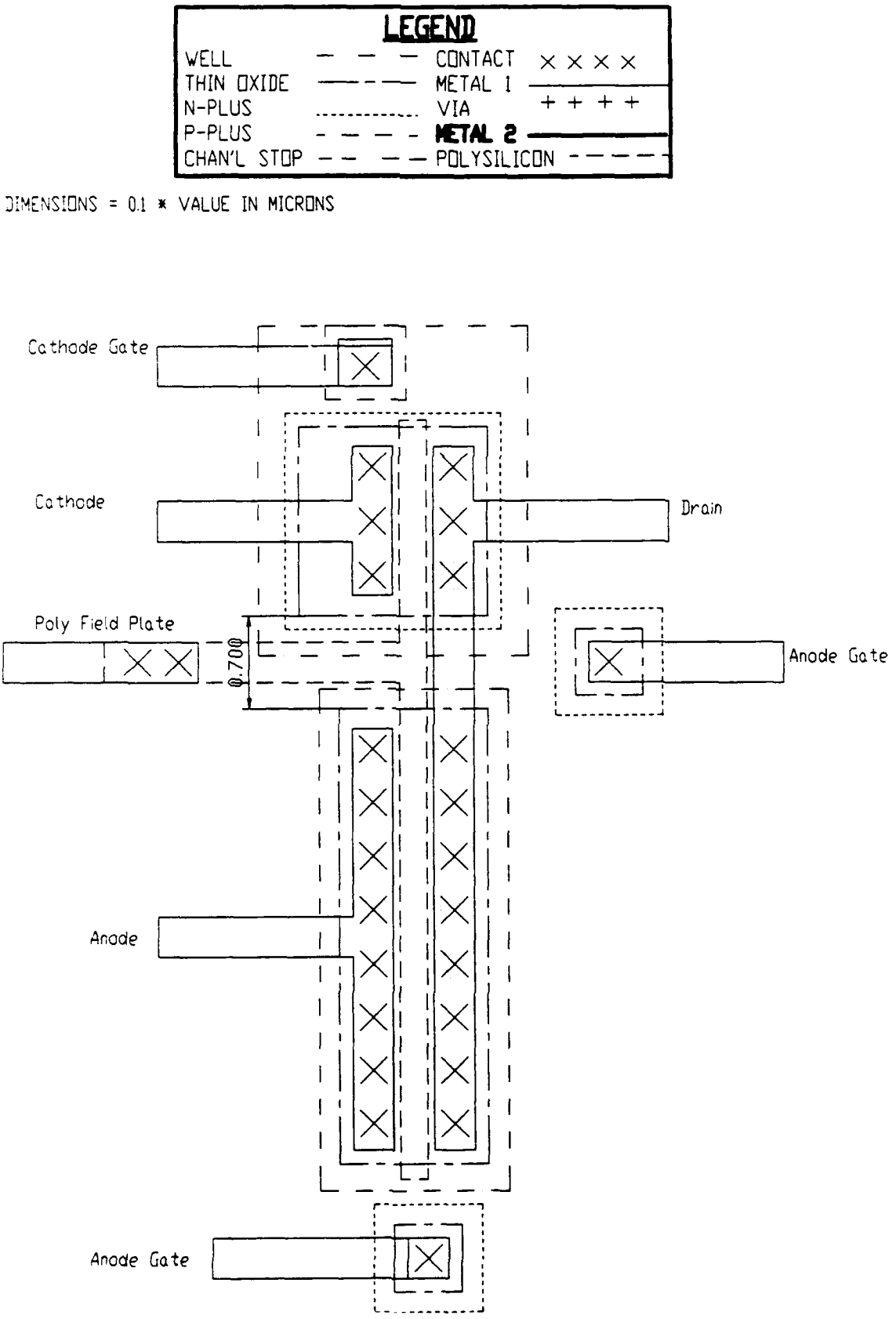


Figure 52. Latchup path configured for maximum gate resistance.

characteristics. If guardbands are used in the technology, they should be included in the structure. An array of structures may be required to investigate the impact of spacing variations for drain-to-well, contact-to-latch path, guard ring-to-well, and guard ring contact-to-latch path.

9.14.3 Special Design Considerations

Two substrate contacts have been included on either side of the structure so that an aiding electric field can be established across the latch region.

9.14.4 Application

In order for latchup to occur and be sustained in a device, the gain product of the parasitic transistors involved in the latch path must be greater than unity. Also, the parasitic resistances associated with the anode and cathode gates must be sufficiently large to permit a V_{beon} drop across them at the currents associated with the holding point. This device is designed to maximize the resistance in the anode and cathode gates, but it may minimize the gain of the parasitic transistors. Thus, the failure of this structure to latch (or to have a holding voltage greater than the supply voltage) is a necessary but not sufficient condition for latchup-free operation in a microcircuit. Results of tests on this structure should be considered along with those from device 9.13 in a careful analysis of latchup potential. The design of the microcircuit will have to employ the same design rules for junction spacing and location of substrate and well contacts if the test structures are to truly reflect its latchup susceptibility.

9.15 N-Channel Snapback Test Structure

9.15.1 Purpose

The snapback test structure as shown in figure 53 is used to determine the sustaining voltage for the snapback conduction mechanism. Snapback is a three-layer, regenerative breakdown mode in MOS devices [103]. Output drivers are especially susceptible to snapback breakdown.

9.15.2 Description

This test structure is a large N-channel transistor similar to those found in output drivers of the microcircuit. The transistor is oriented so that if avalanche breakdown occurs at the drain, the maximum amount of avalanche current will flow under the source and out of the topside substrate contact. Spacings are based on minimum N-channel transistor gate lengths and a variety of distances to the topside substrate contact.

9.15.3 Special Design Considerations

Initiating and sustaining the snapback conduction mechanism require a combination of both MOS and bipolar transistor action. The MOS transistor must be oriented so that the avalanching drain current flows under the source. This permits the source to be turned on and act as the emitter of a parasitic bipolar transistor. Any design which tends to enhance parasitic bipolar transistor performance or increase the parasitic base resistance will increase the likelihood of snapback. Location and sizing of substrate contact structures should be consistent with design rules which are checked for the technology.

9.15.4 Applications

The snapback structure is typically tested by avalanching the drain and recording the drain current versus drain voltage I/V characteristic. If the snapback characteristic is cut by the load line represented by the P-channel device, the transistor is likely to experience snapback.

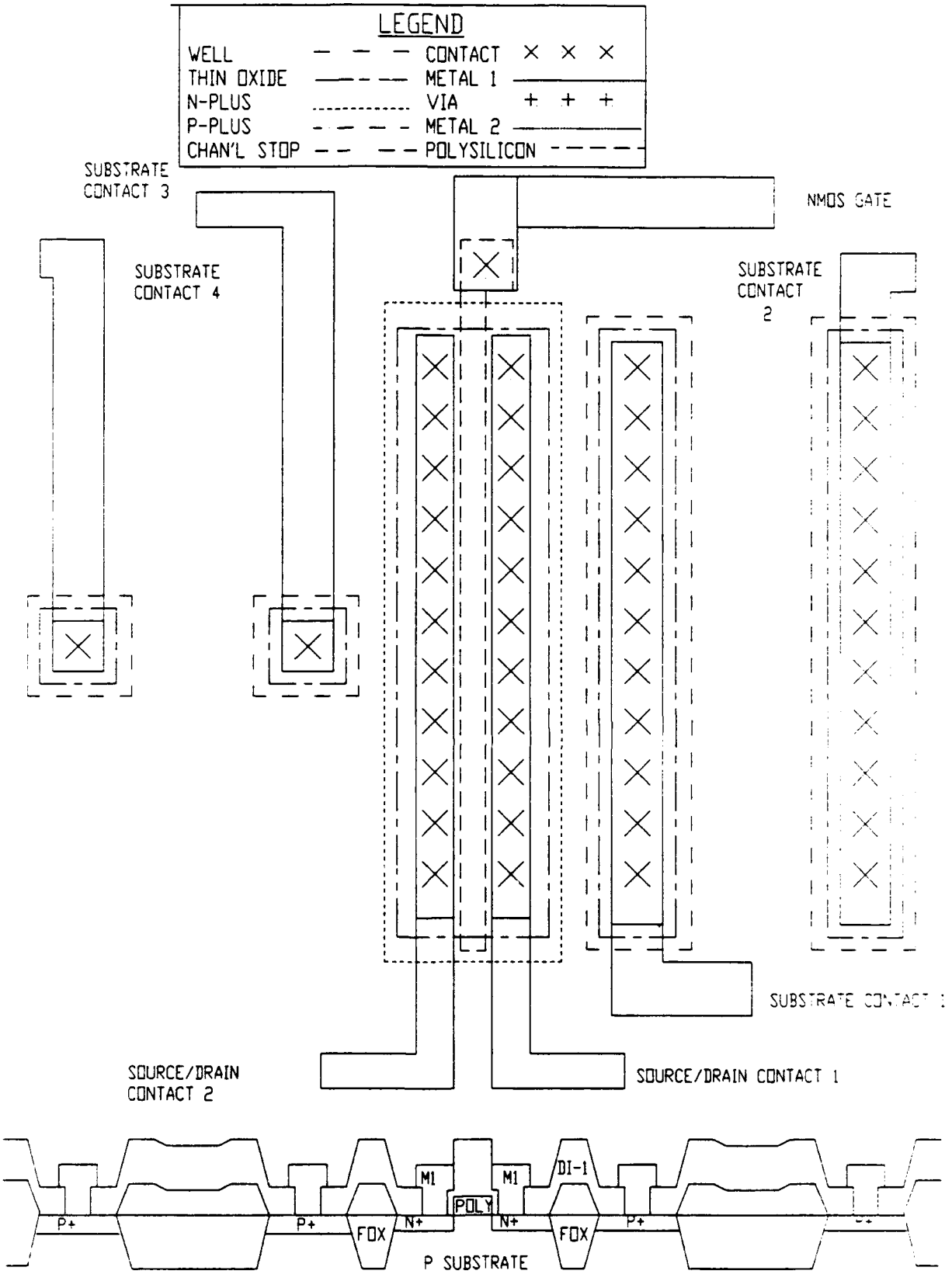


Figure 53. Snapback test structure.

9.16 Substrate Spreading Resistance Structure

9.16.1 Purpose

The substrate spreading resistance structure as shown in figure 54 is used to determine the value of vertical and lateral spreading resistance for devices fabricated in the substrate material.

9.16.2 Description

The structure consists of a series of substrate contact structures and diodes of various dimensions. There are two long substrate contact structures (typically 100 μm) located in the center, with minimum spacing between them. A third long substrate contact structure is located 200 μm away. Midway between the structures, there is a minimum geometry substrate contact. On one end of the structure there is a 4$\times$ substrate contact. On the other end, there is a minimum-geometry buried layer-to-substrate diode.

9.16.3 Special Design Considerations

Any buried layers, wells, or implants which might intervene between substrate contacts should be included in one section of this device between the minimum substrate contact and the long narrow contact.

9.16.4 Applications

By making measurements between the contact structures and diodes, the test engineer can determine the lateral and vertical spreading resistance as a function of geometry (i.e., point contact or line contact), carrier type (majority or minority), and spacing between contacts. The substrate spreading resistance is important both for latchup and photoresponse analyses.

9.17 Well Spreading-Resistance Structure

9.17.1 Purpose

The well spreading resistance structure as shown in figure 55 is used to determine the value of lateral spreading resistance for devices fabricated in the well.

9.17.2 Description

The structure consists of a series of well contact structures and diodes of various dimensions. There are two long well contact structures (typically 100 μm) located in the center, with minimum spacing between them. A third long well contact structure is 200 μm away. Midway between the structures, there is a minimum geometry well contact. On one end of the structure is a 4$\times$ well contact. On the other end there is a minimum geometry drain-to-well diode.

9.17.3 Special Design Considerations

Any channel stops or other implants which may intervene between well contacts should be included in one section of this device between the minimum well contact and the long narrow-well contact.

9.17.4 Applications

By making measurements among the contact structures and diodes, the test engineer can determine the lateral spreading resistance as a function of geometry (i.e., point contact or line contact), carrier type (majority or minority), and spacing between contacts. The well spreading resistance is important both for latchup and photoresponse analyses.

9.18 SEU Charge Collection Array

9.18.1 Purpose

The SEU charge collection array as shown in figure 56 is used for measuring waveshape and amplitude of heavy ion strikes [104].

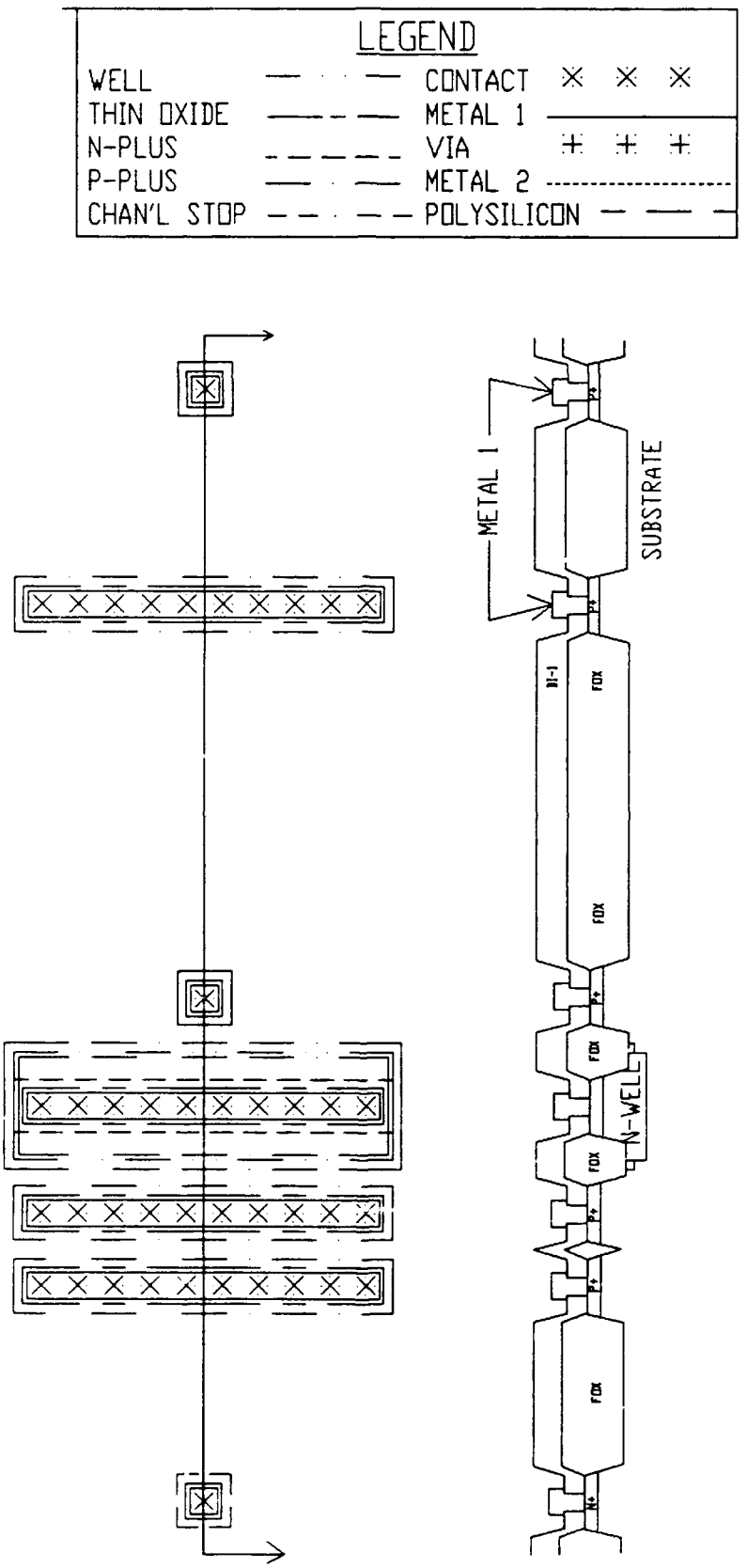


Figure 54. Substrate spreading resistance test structure.

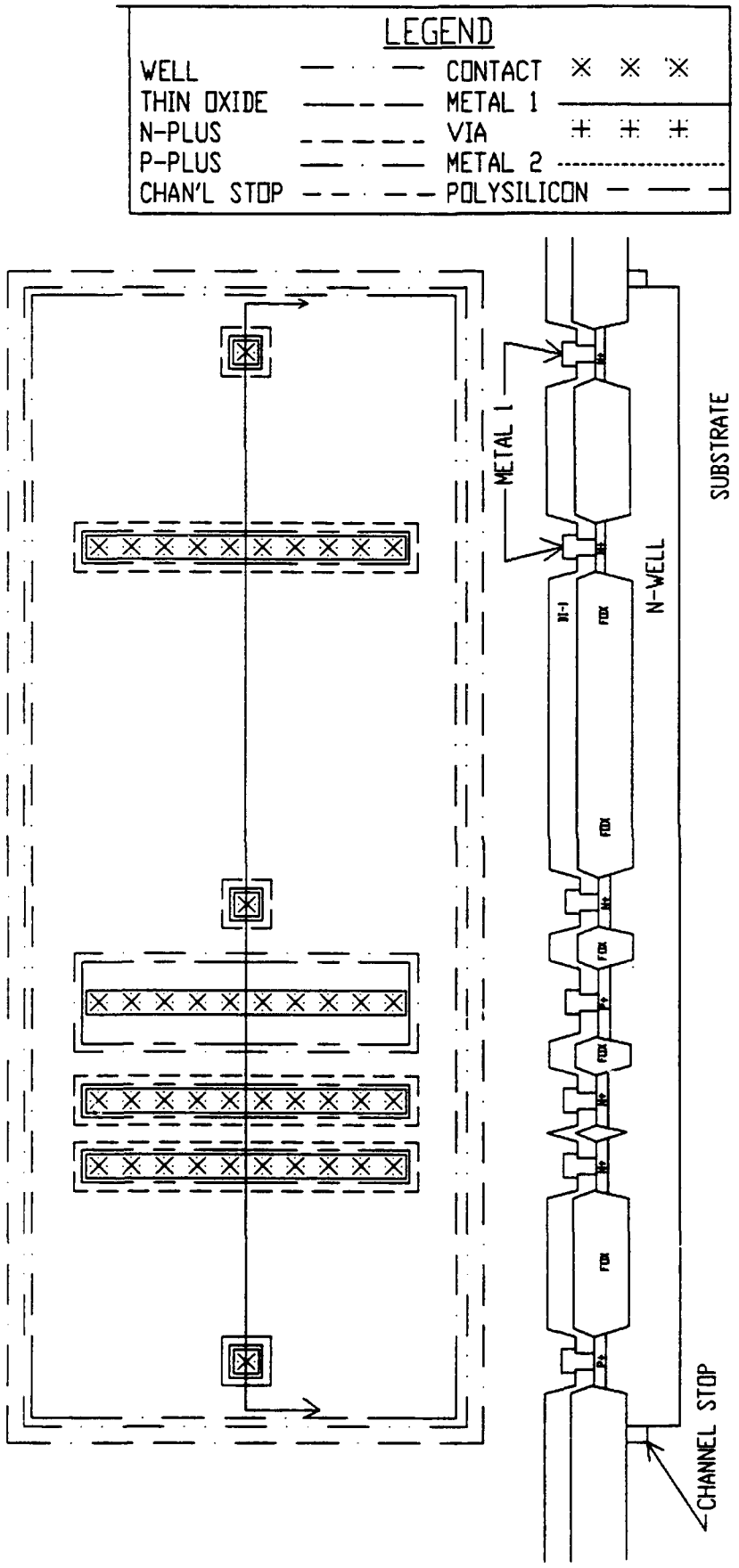


Figure 55. Well spreading-resistance test structure.

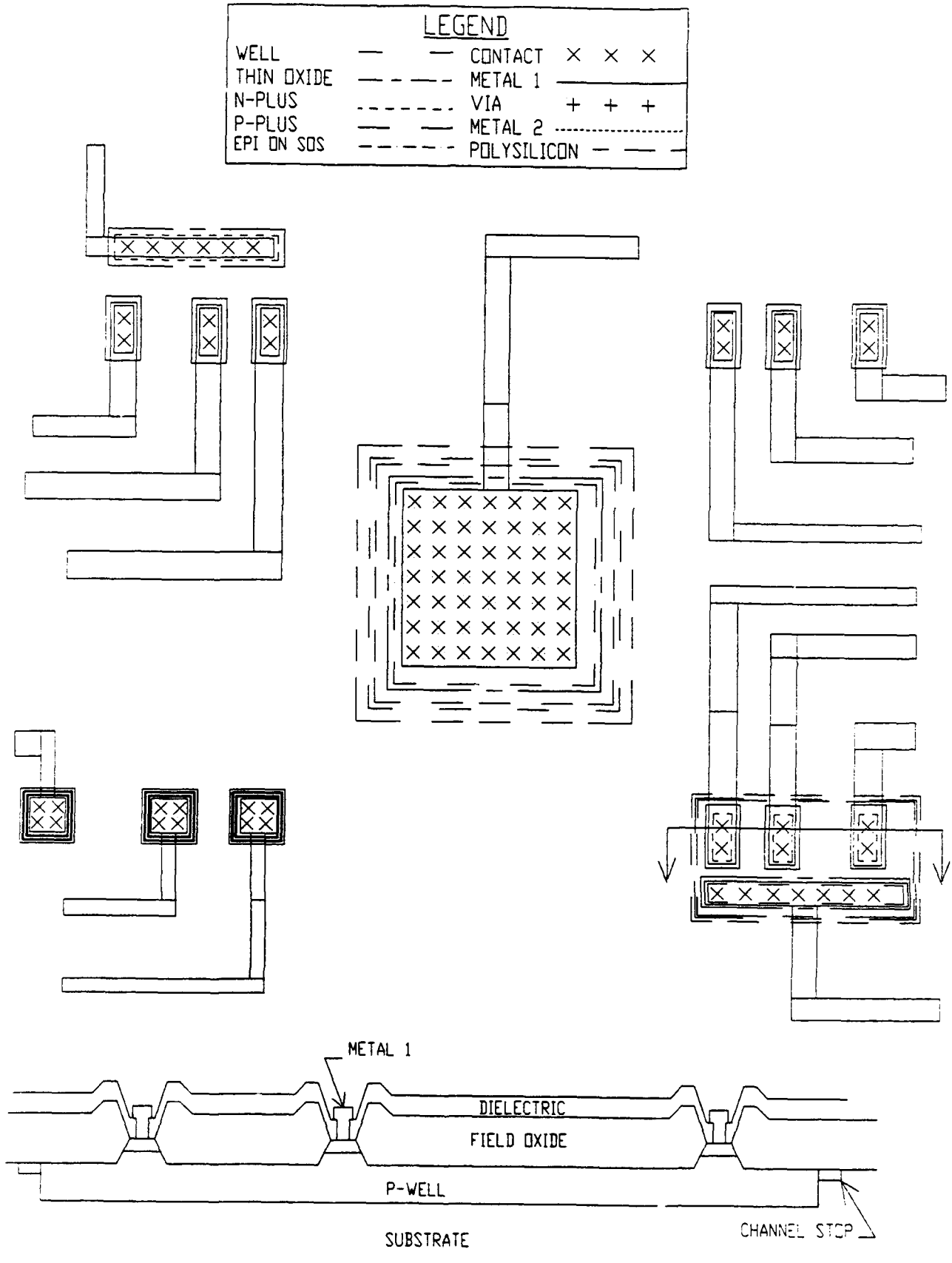


Figure 56. SEU charge collection array.

9.18.2 Description

This is an array of devices located around the periphery of a large reference diode. The large diode is included as a reference point for a collimated ion beam. The diode can be easily located by moving the ion beam across the center of the die. Once the large diode is found, all other structures can be located from it. The remaining structures represent either complete devices or combinations of device layers found in the technology. For example, the structure for a bipolar technology used as an example in the figure includes a buried layer substrate diode, a base/epi/buried layer/substrate structure, a complete transistor, etc. In some sections of the array, a series of identical structures with minimum spacing has been included to investigate charge sharing between adjacent structures in the case of an oblique strike.

9.18.3 Special Design Considerations

Device dimensions on this test structure should be representative of the size of devices used in microcircuit designs. Bonding pads should be provided for all device terminals.

9.18.4 Applications

Waveshape and amplitude measurements for individual heavy ion strikes require careful experimental techniques. If chip amplifiers can be fabricated in the technology, the structures may be combined with amplifier circuits to drive the instrumentation. These amplifiers require careful design [104].

10. BIPOLAR TRANSISTORS

10.1 Introduction

This section is directed toward bipolar technologies and transistor structures used in microcircuit design. Bipolar transistor characteristics are strongly affected by their layout. The test chip should contain representatives of all the layout orientations expected to be used by designers. In general, the base and collector of the test transistor should be brought out to separate pads. Several emitters may be tied together and brought out to a single pad. A good topside contact to the substrate should be included near each transistor.

10.2 Transistor Library Samples

10.2.1 Purpose

The representatives from the transistor cell library are used to evaluate radiation effects on the different transistor geometries used by designers in developing a microcircuit function [105]. Figure 57 illustrates the layout of a few transistors from such a library.

10.2.2 Description

Most bipolar designs are developed from a library of transistors with different layouts to provide different DC and AC performance characteristics. Layout variations include different types of collector structures (single contact, horseshoe contact, etc), varieties of emitter geometries (single stripe, multiple stripe, interdigitated, rectangular, round, walled, nested, etc), different base designs (Schottky clamped, unclamped, etc), different sequences of contacts (collector/base/emitter versus collector/emitter/base), and several similar layouts with different scale factors (2×, 3×, 4×, etc). As many of these types of structures as possible should be included on the test chip.

10.2.3 Special Design Considerations

Since a large number of transistors are likely to be in the library, a 2×N pad array is probably the most efficient way to include all of them on the test chip. A representative of each type of layout should be located on the periphery of the test chip so they can be bonded out in a package for radiation testing.

10.2.4 Applications

Representatives of each layout type should be included in neutron and total ionizing dose tests. Complete pretest and posttest I/V characteristics should be measured and used to develop circuit simulation models for use by the designers. Careful consideration should be given to the bias conditions during radiation for each type of device. Emitter current density and collector voltage have a strong impact on the radiation performance of bipolar transistors. Bias conditions should be selected which are similar to those used in the application of each device type. For best neutron hardness, transistors should typically operate at current densities near the peak in their gain versus collector current characteristic (i. e., peak beta).

10.3 Transistor with Nested Emitter

10.3.1 Purpose

The transistor with a nested emitter as shown in figure 58 is used to reduce collector-to-emitter leakage effects from total dose testing.

10.3.2 Description

Designers should use transistor layouts typical of those to be used in the circuit. The emitter is laid out so that the emitter diffusion does not intercept the sidewall of the transistor. The emitter is completely surrounded (nested) by the base implant.

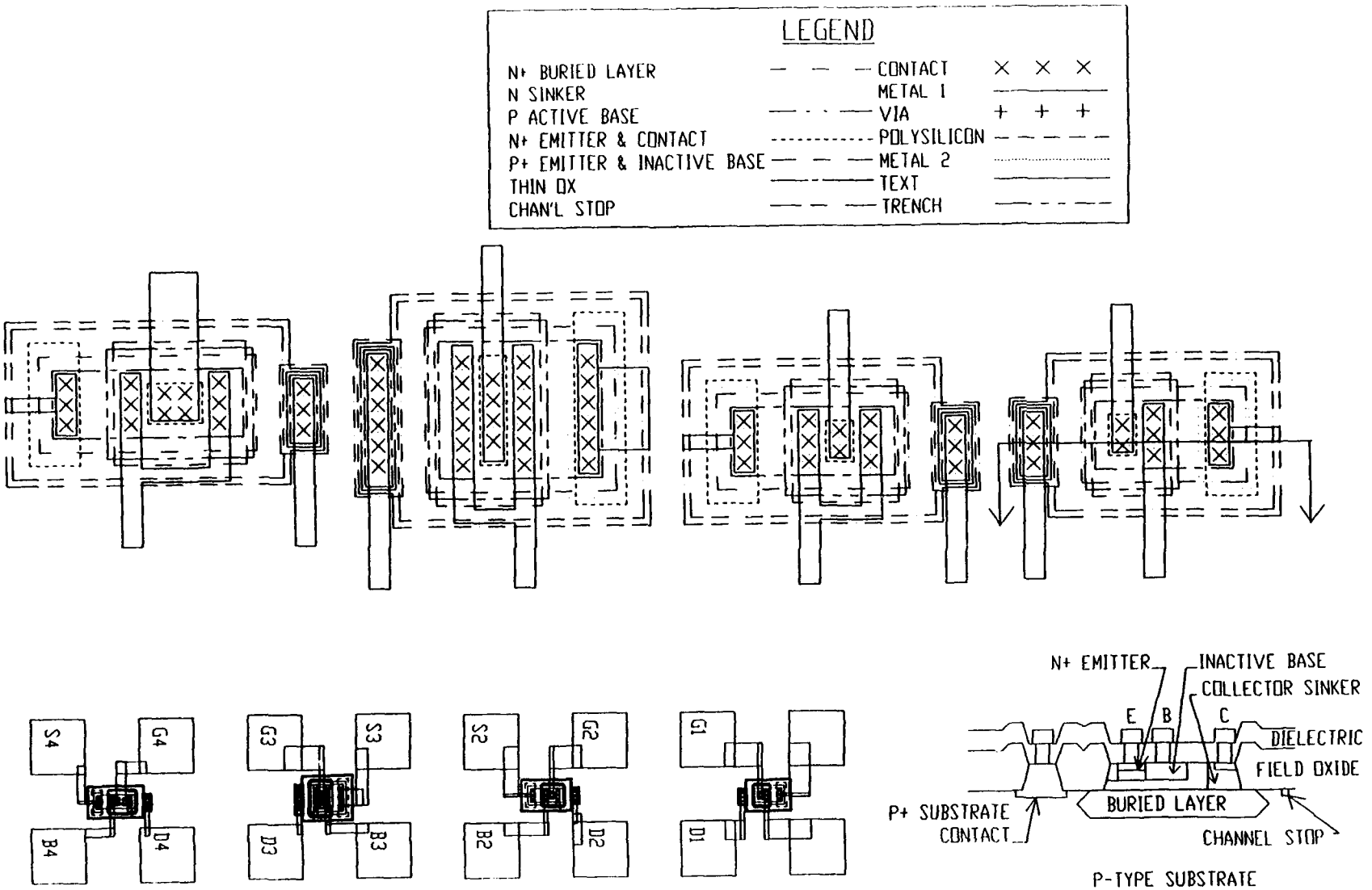


Figure 57. Test transistor selection from a library.

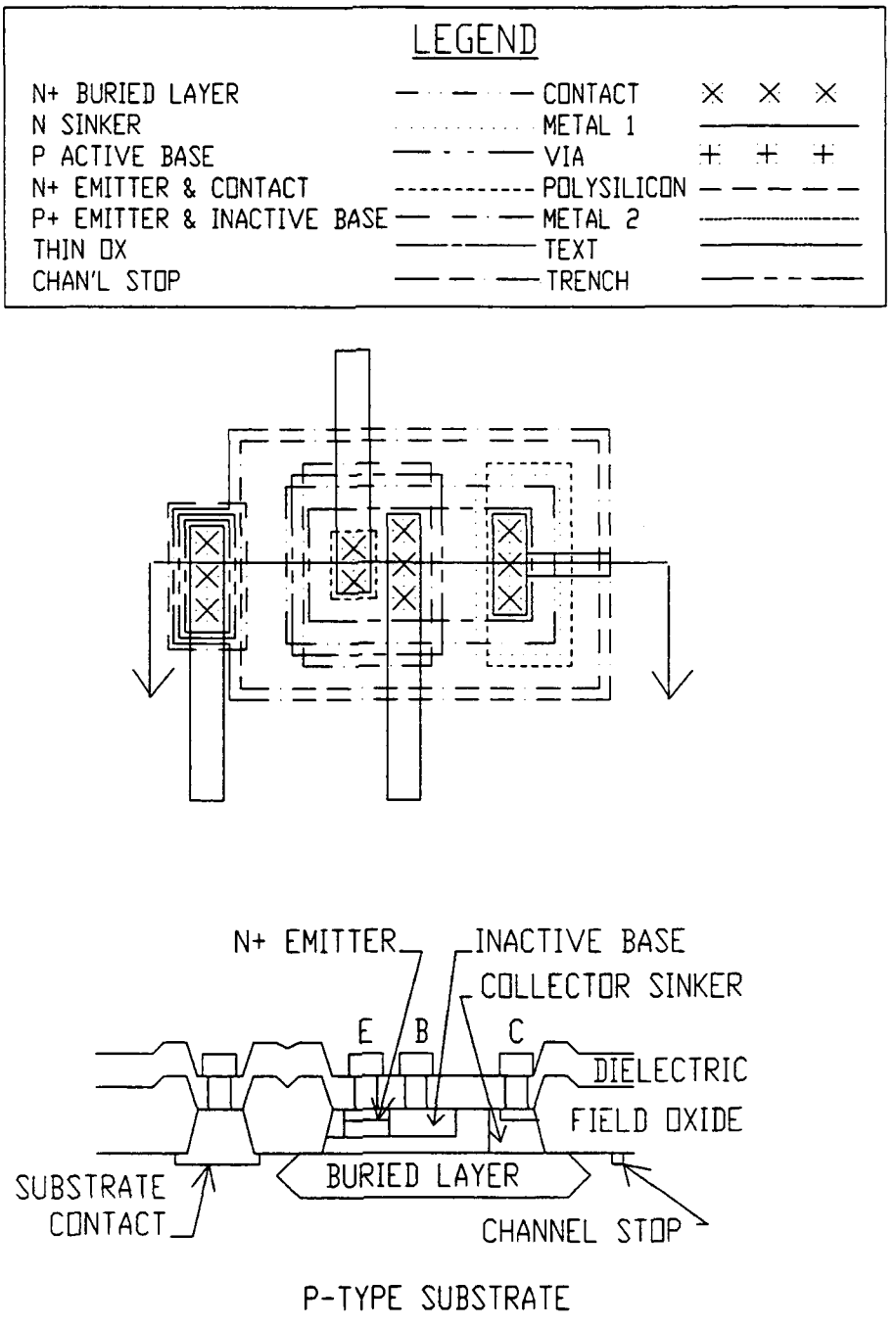


Figure 58. Nested emitter transistor.

10.3.3 Special Design Considerations

Even if the process typically uses walled emitters, a nested emitter structure should be included so that total-dose-induced collector-to-emitter leakage can be separated from increases in base recombination current. This will also indicate the benefits to be gained from modifying the designs to use only nested emitters. An array of these devices may be desirable to determine the required emitter-to-sidewall design rule.

10.3.4 Applications

In technologies using recessed field oxides or trenches for lateral isolation, charge can be trapped in the oxide along the side of the base. The base may then become inverted along the sidewall. If the emitter is walled against the sidewall, a channel will be formed between the emitter and collector, and there will be a large increase in leakage current. Since the emitter tends to diffuse out toward the sidewall even in nested emitters, these structures will be required to determine the spacing between the emitter cut and the sidewall.

10.4 Transistor with Walled Emitter

10.4.1 Purpose

The transistor with a walled emitter as shown in figure 59 is used to evaluate collector-to-emitter leakage arising from total dose testing.

10.4.2 Description

Designers should use transistor layouts typical of those to be used in the circuit. The emitter is laid out so that the emitter diffusion overlaps the sidewall of the transistor. The dimension of the resistor is determined by the wall of the isolation region.

10.4.3 Special Design Considerations

Even if the process typically uses nested emitters, a walled emitter structure should be included so that the magnitude of total-dose-induced collector-to-emitter leakage can be identified if walled emitters are contemplated in future designs.

10.4.4 Applications

In technologies using recessed field oxides or trenches for lateral isolation, charge can be trapped in the oxide along the side of the base. The base may then become inverted along the sidewall. If the emitter is walled against the sidewall, a channel will be formed between the emitter and collector, and there will be a large increase in leakage current.

10.5 Transistors with Base/Emitter Contact Swap

10.5.1 Purpose

The transistors with different sequences of collector, base, and emitter contacts as shown in figure 60 are used to determine if the positioning of the base contact has a significant effect on the post-irradiation I/V characteristics.

10.5.2 Description

This structure consists of these transistors from the library which may have the order of their collector, base, and emitter contacts interchanged by the designer in order to facilitate interconnect routing. The devices are identical except for the order of their contacts.

10.5.3 Special Design Considerations

There are no special design considerations.

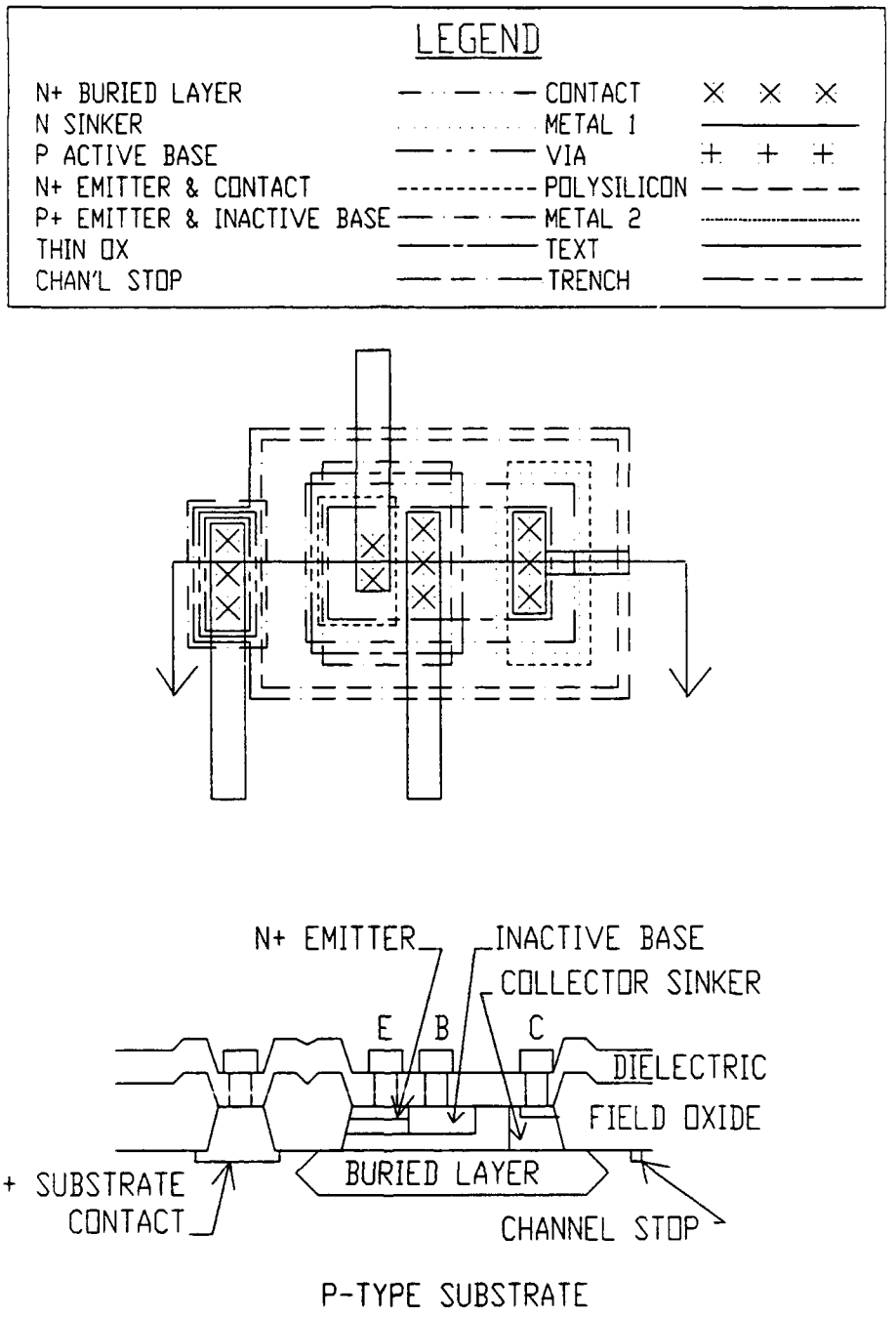


Figure 59. Transistor with walled emitter.

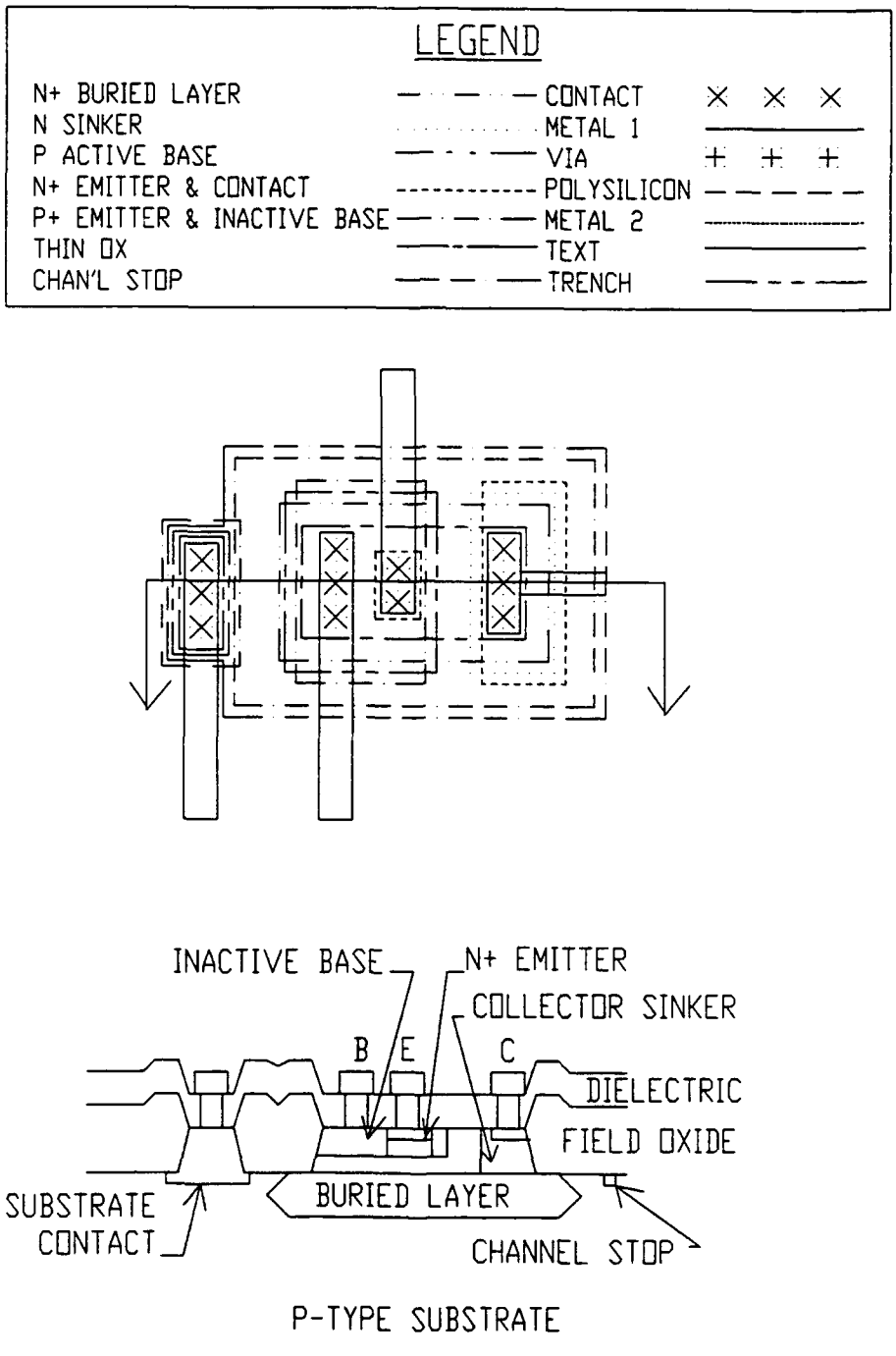


Figure 60. Transistors with variations in contact sequence.

10.5.4 Applications

Changing the order of the terminal contacts affects the current density in different portions of the transistor. In general, the emitter current tends to crowd toward the edge closest to the base contact. The local change in current density may cause differences in the total dose response of otherwise identical transistors. This may be particularly important in designs which require transistor characteristics to be closely matched.

10.6 Differential Pair Transistors with Individual Terminals

10.6.1 Purpose

The differential pair transistors with individual terminals, as shown in figure 61, are used to monitor parameter matching in differential pairs after neutron or total dose irradiation.

10.6.2 Description

The structure consists of transistors from the library which are available for use as differential pairs. They are spaced at the minimum design rule for adjacent transistors. Individual pads are provided for emitter, base, and collector terminals.

10.6.3 Special Design Considerations

Multiple sets of differential pairs may be placed at different locations on the test chip die to determine how parameter matching varies with die position.

Some of the pairs should be placed orthogonally to check for any misalignment effects on parameter matching.

10.6.4 Applications

In many bipolar designs for analog applications, transistor parameter matching after irradiation is extremely important for maintaining circuit performance. This matching must be checked on adjacent transistors. Bias during irradiation should reflect the expected differences in current density for the two sides of a differential pair for circuit applications. Typically both gain matching and V_{beon} matching as a function of collector current are especially important parameters to be monitored.

10.7 Simple Differential Amplifier

10.7.1 Purpose

The simple differential amplifier, as shown in figure 62, is used to monitor offset current and voltage and common mode rejection ratio as a function of total dose and neutron fluence.

10.7.2 Description

This structure consists of three transistors configured as a differential pair with their emitters connected to a constant current source.

10.7.3 Special Design Considerations

Transistors for the differential pair should be the same size as those used in device 10.6. The constant current source should be the library device typically used by the designers for that application.

10.7.4 Applications

The simple differential amplifier is included so that offsets and rejection ratio can be measured simultaneously with transistor parameters. Comparison of computer predictions

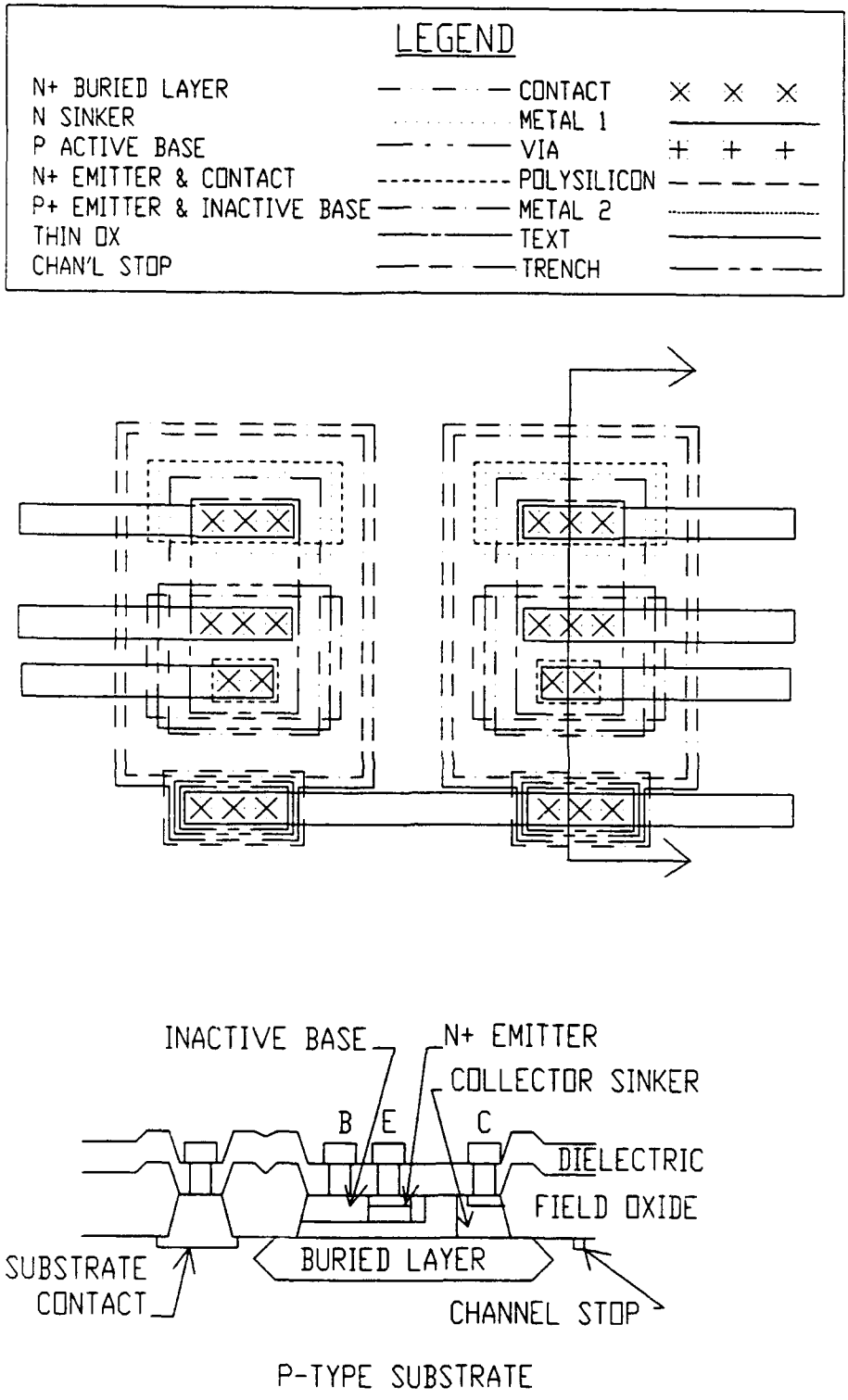


Figure 61. Bipolar transistor differential pair.

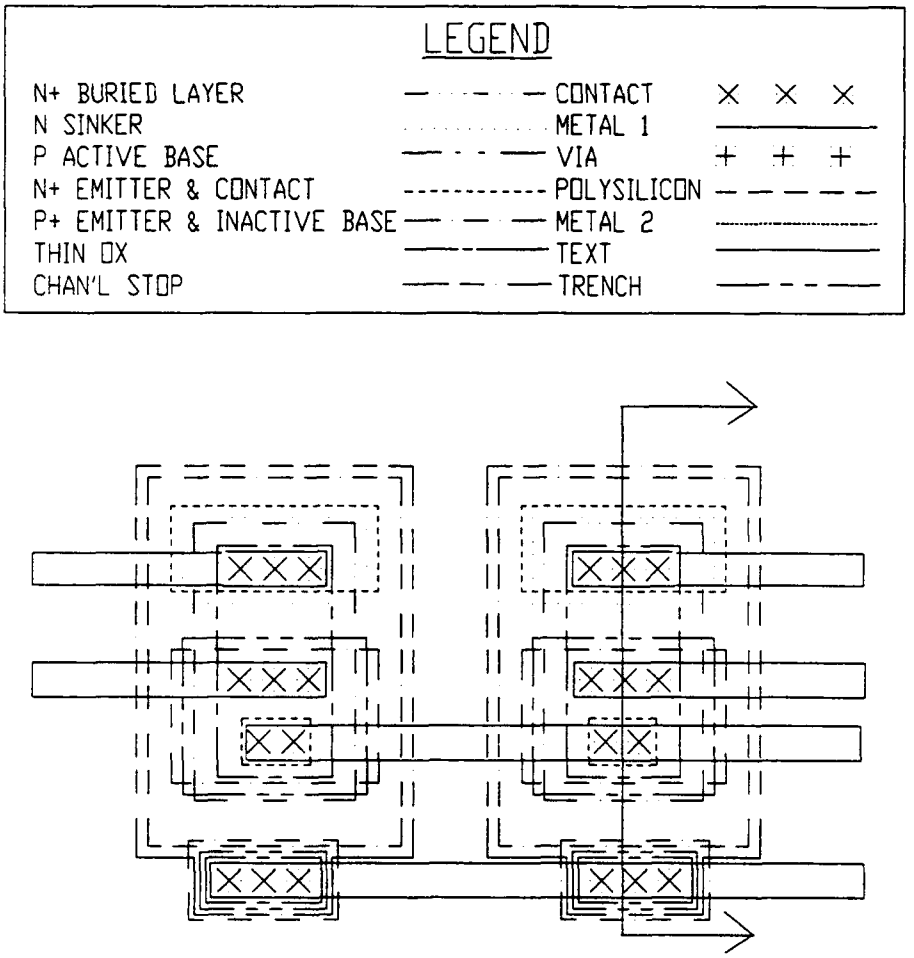


Figure 62. Bipolar transistor differential amplifier.

of offsets and rejection ratios with measured values can indicate the accuracy of the computer models.

11. BIPOLAR DIODES

11.1 Introduction

The test structures described in this section include both intentional diodes included as part of the design library and parasitic diodes which are important in determining the photoresponse of the microcircuit. The effects of total ionizing dose and neutrons on the I/V characteristics of the intentional diodes should be included in the computer-aided design models available to designers. The parasitic diodes will be used primarily to determine photocurrent as a function of dose rate and device geometry [106]. Structures have been included to emphasize both the vertical and lateral components of the photocurrent. The vertical component is collected directly under the device. The lateral component is collected from adjacent areas.

11.2 Diode-Connected Transistors

11.2.1 Purpose

The diode-connected transistors, as shown in figure 63, are included to determine the post-irradiation I/V characteristics of transistors from the device library connected as diodes.

11.2.2 Description

These structures are transistors from the design library which have been connected as diodes. Their I/V characteristics vary depending on the terminals connected or the implants which may have been eliminated.

11.2.3 Special Design Considerations

There are no special design considerations.

11.2.4 Applications

The emitter-base junction diode is often used as a Zener reference in analog bipolar designs. Variations in the reference voltage with radiation should be measured and included in the design models. The forward bias characteristics of other diode types are of greater interest.

11.3 Buried Zener

11.3.1 Purpose

The buried Zener structure as shown in figure 64 is used to monitor the change in its reference voltage as a function of neutron fluence and total ionizing dose.

11.3.2 Description

This structure is the buried Zener reference diode available to the designer from the library. Dimensions should be selected to reflect those typically used in designs.

11.3.3 Special Design Considerations

Multiple buried Zeners with different areas may be included to permit evaluation of both current and current density effects on post-irradiation performance.

11.3.4 Applications

The buried Zener is used as the primary reference voltage in many bipolar analog designs. A thorough characterization of the change in reference voltage with radiation is an important part of the information required for a hardened design. Care must be taken to ensure that temperature is precisely controlled to be the same for both pre-irradiation and post-irradiation characterization. Otherwise, temperature effects may be confused with the effects of radiation damage.

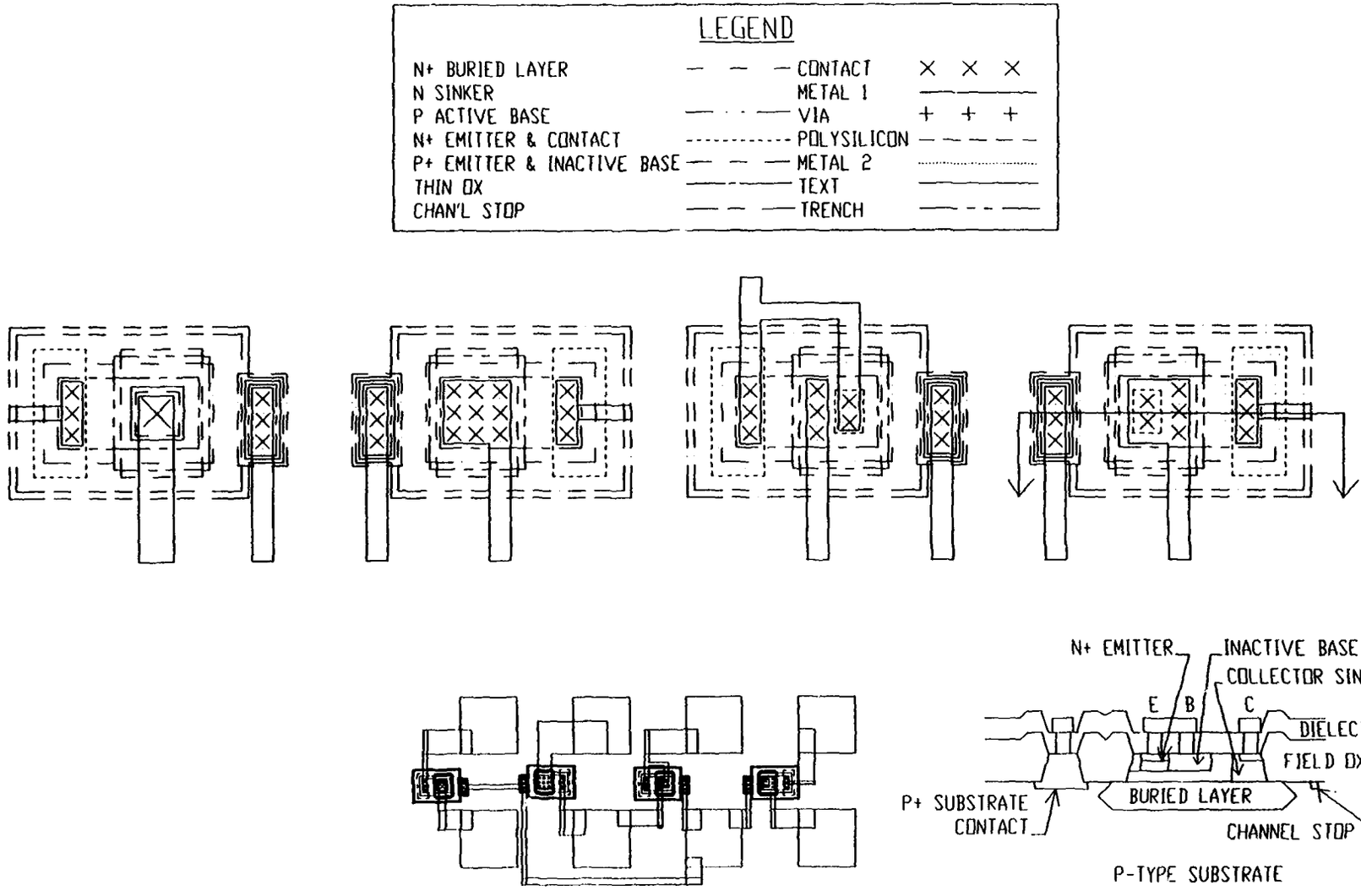
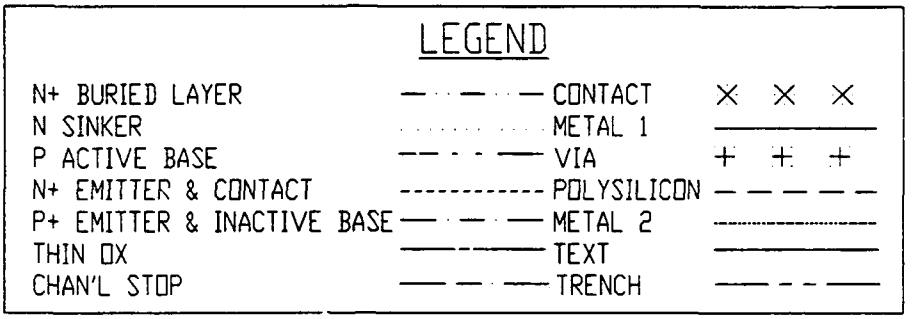
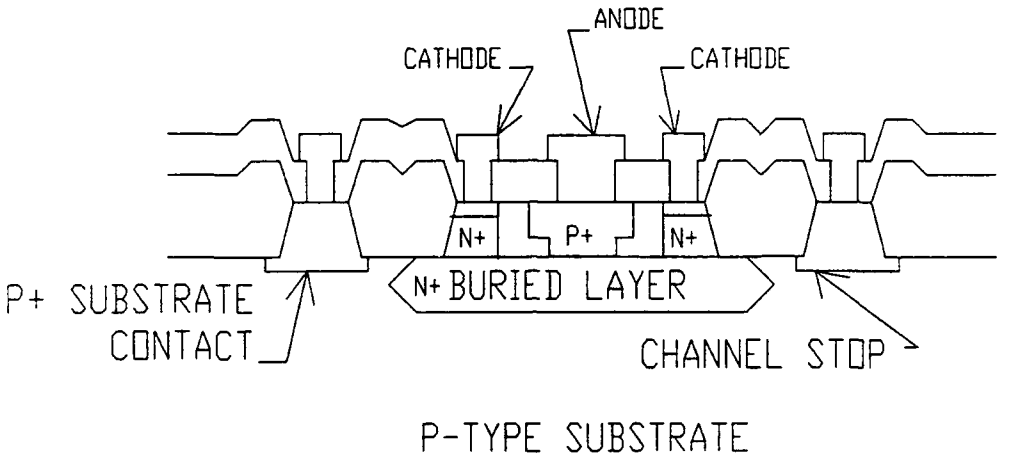


Figure 63. Diode connected transistor test structures.





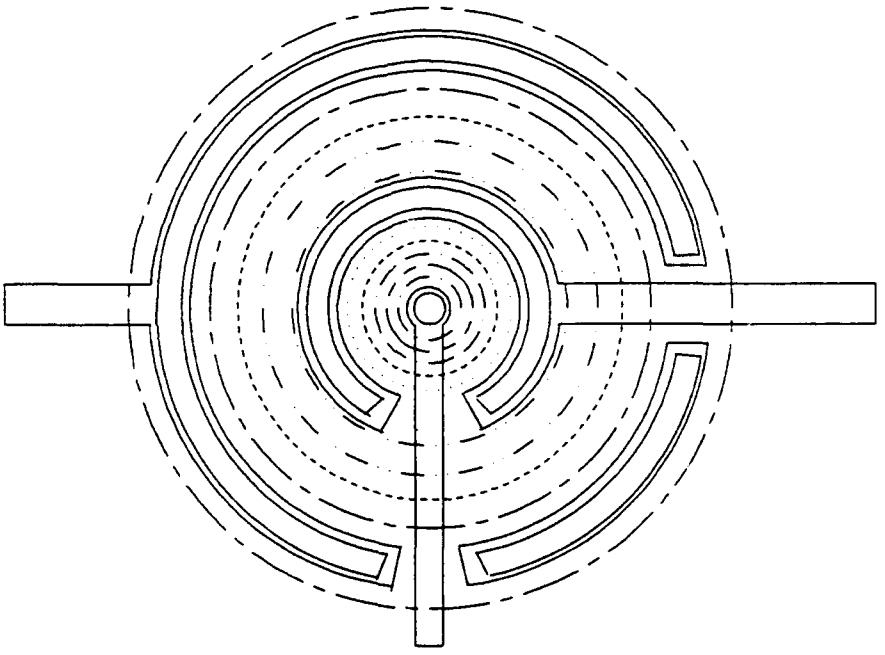


Figure 64. Buried Zener diode test structure.

11.4 Schottky Without Guard Ring

11.4.1 Purpose

The Schottky diode without a guard ring, as shown in figure 65, is used to evaluate post-irradiation leakage current increase.

11.4.2 Description

This is a large-area Schottky barrier diode with an aspect ratio similar to that used in design applications. The area is selected to produce a measurable photocurrent at the expected upset threshold.

11.4.3 Special Design Considerations

The overlap of the metallization over the contact cut should be the minimum allowed by the design rule.

11.4.4 Applications

Schottky-barrier diodes, which are used as collector/base clamps in Schottky transistor transistor logic (TTL) technologies and as collector coupling devices in Schottky integrated injection logic, have a tendency toward large reverse leakages and reduced reverse breakdown voltages. These arise from the high electric fields at the device edges due to the curvature of the depletion layer. These regions of sharp curvature can be eliminated by a guard ring implant or by use of a field plate. However, both techniques require additional area. Total dose irradiation may result in even more sharply curved depletion regions by contributing to accumulation at the N-region surface and making it appear more heavily doped. Therefore, the post-irradiation leakage current should be evaluated for this technology and provided as a parameter to designers. Likewise, the primary photocurrent scaling factor for the Schottky diodes is a necessary design parameter. Usually, the collection volume of the Schottky diode is limited by the dimensions of the epi tub which contains it.

11.5 Schottky with Guard Ring

11.5.1 Purpose

The Schottky diode with a guard ring, as shown in figure 66, is used to evaluate post-irradiation leakage current increase.

11.5.2 Description

This is a large-area Schottky-barrier diode employing a guard ring with an aspect ratio similar to that used in design applications. The area is selected to produce a measurable photocurrent at the expected upset threshold.

11.5.3 Special Design Considerations

This structure should be used in conjunction with device 11.4 to determine the improvement in post-irradiation leakage current afforded by using a guard ring for the Schottky diode.

11.5.4 Applications

Schottky-barrier diodes, which are used as collector/base clamps in Schottky TTL technologies and as collector coupling devices in Schottky integrated injection logic, have a tendency toward large reverse leakages and reduced reverse breakdown voltages. These arise from the high electric fields at the device edges due to the curvature of the depletion layer. These regions of sharp curvature can be eliminated by a guard ring implant or by use of a field plate. However, both techniques require additional area. Total dose irradiation may result in even more sharply curved depletion regions by contributing to accumulation at the N-region surface and making it appear more heavily doped. Therefore, the post-irradiation leakage current should be evaluated for this technology and provided as a parameter to the designers. Likewise, the primary photocurrent scaling

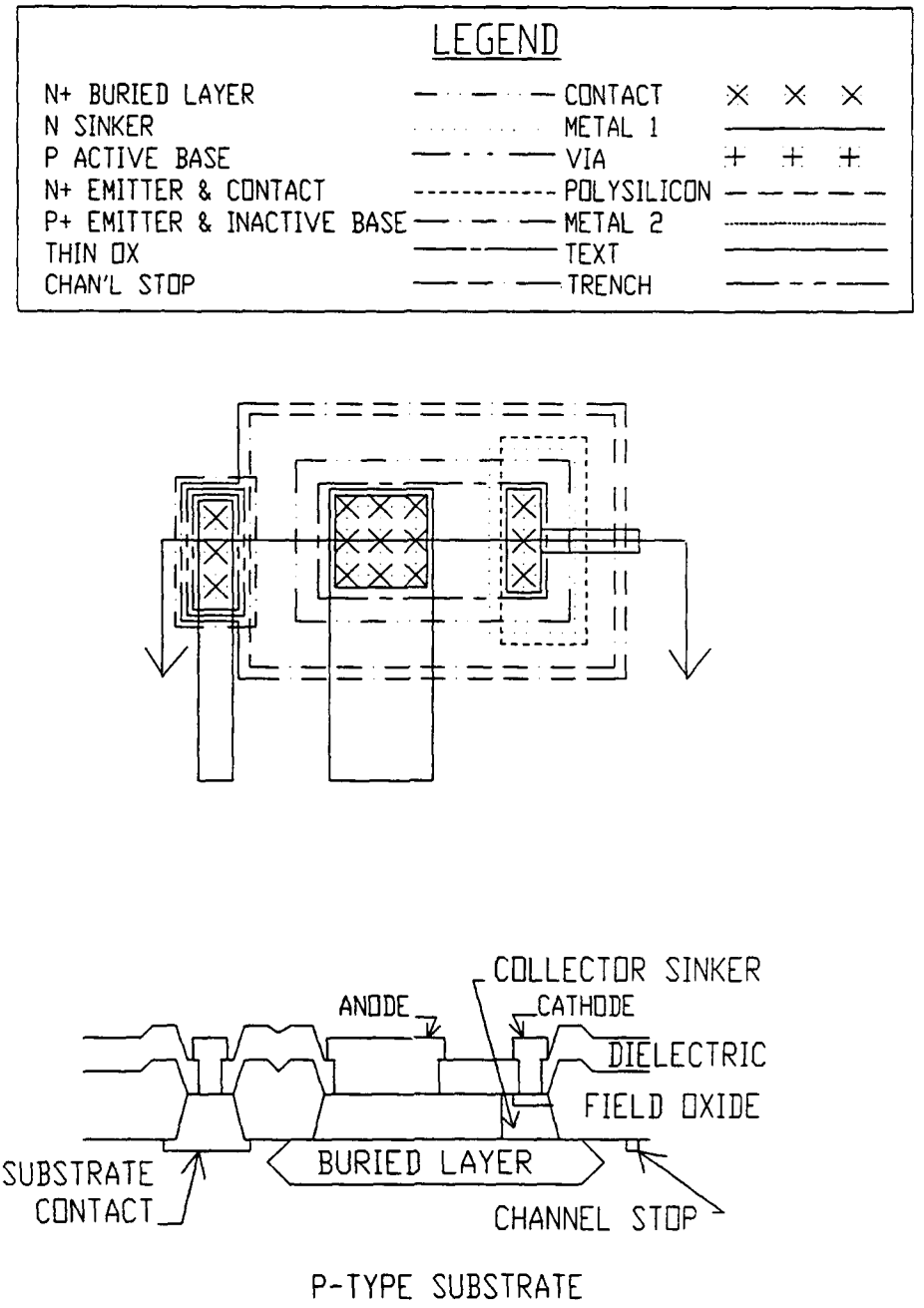


Figure 65. Schottky diode without guard ring.

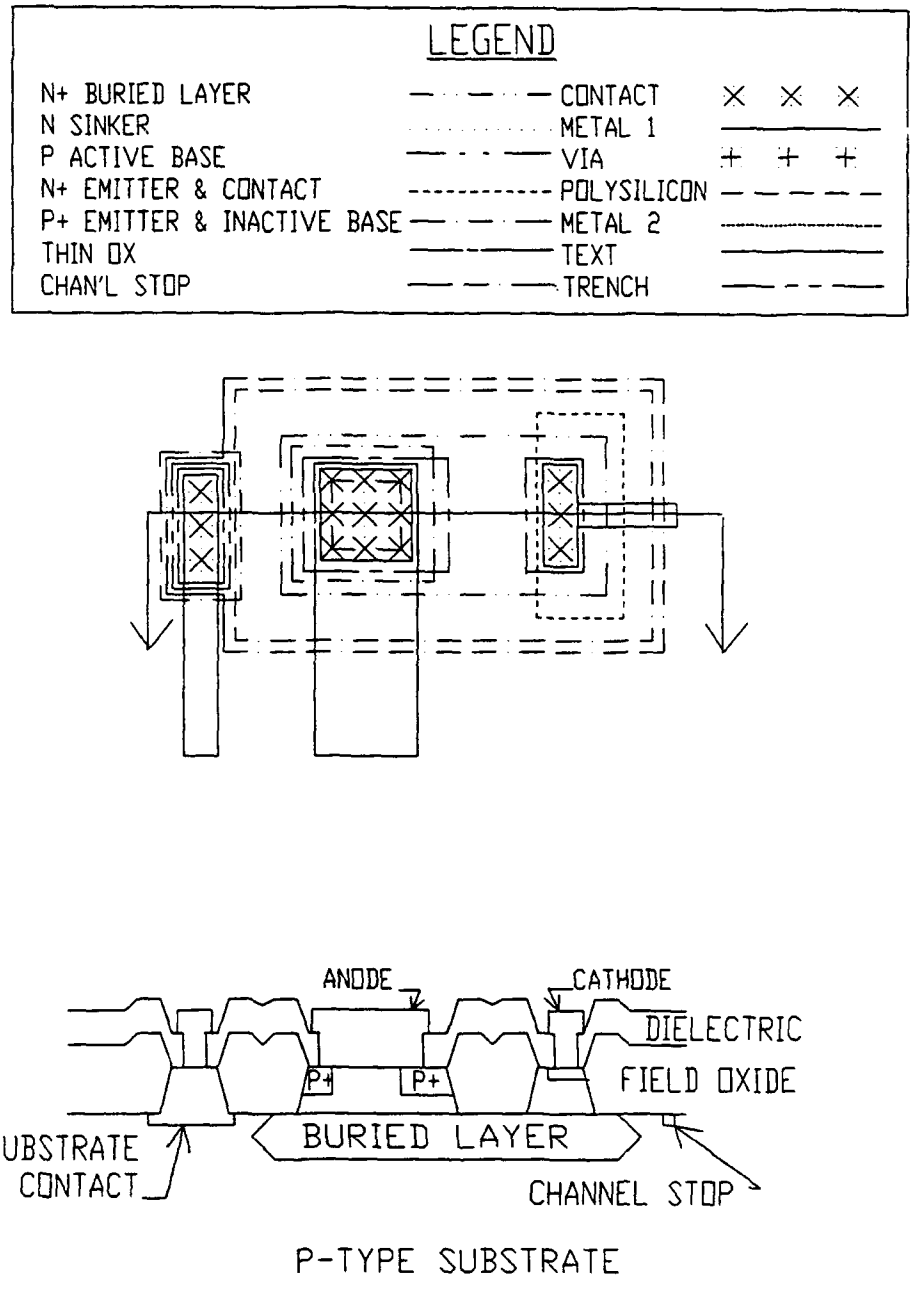


Figure 66. Schottky diode with guard ring.

factor for the Schottky diodes is a necessary design parameter. Usually, the collection volume of the Schottky diode is limited by the dimensions of the epi tub which contains it. The collection volume may be increased by including the guard ring implants since they extend the depth of the device and will probably be more efficient collectors of lateral photocurrents.

11.6 Photodiode—Buried Layer/Substrate, No Guardband, and Minimum Aspect Ratio

11.6.1 Purpose

The buried layer/substrate diode as shown in figure 67 is used to determine the maximum primary photocurrent as a function of dose rate [87].

11.6.2 Description

This photodiode is typically a square or circular device with dimensions selected to yield a measurable photocurrent an order of magnitude below the expected upset threshold. For design purposes, assume that the photocurrent is 6.4 microamps per cubic centimeter per rad(Si)/s. The collection volume includes both the material directly under the diode (vertical collection volume) and a portion of the material surrounding the diode (lateral collection volume). The vertical collection volume is the area of the diode times the vertical collection distance under it. The vertical collection depth is the depletion layer width plus a diffusion length into the bulk material. Many bipolar processes use a low-resistivity buried layer under the collector to reduce collector resistance. This buried layer is often contained in a high-resistivity substrate (e.g., 1×10^{15} cm^{-3}) which may have a long minority carrier lifetime (1 to 2 μs). Thus, the vertical collection volume can be quite large, extending 60 to 80 μm into the substrate. The lateral collection volume for each diode edge will consist of a quarter cylinder with its axis coincident with the transistor edge and its radius equal to the diffusion length.

In other technologies, the substrate structure may employ a low-resistivity, short-lifetime substrate with a high-resistivity, long-lifetime epi. In these cases, the vertical collection volume will be mostly confined to the epi region under the buried layer. The lateral collection volume will be a parallelopiped with a width equal to the device edge dimension, length equal to a diffusion length in the epi material, and thickness equal to the epi layer thickness.

Thus, the test chip designer must consider the vertical structure of the technology when sizing the photodiode. A conservative design approach is to consider only the vertical collection volume and size the diode so that a measurable photocurrent is available from the vertical component only. A photocurrent of 10 mA can usually be measured accurately in most simulators if reasonable care is taken in the test fixture design.

11.6.3 Special Design Considerations

The diode should be separated from any adjacent device or substrate contact by two diffusion lengths. Since photocurrent is also collected laterally, the measurement should not be complicated by having two structures compete for the same collection volume. In epi technologies, the diffusion length in the high-resistivity epi region is longer than the low-resistivity substrate. The epi diffusion length (typically 50 to 100 μm) should be used in determining separation between adjacent devices. Care should be taken in providing a good contact to the buried layer. If a collector sinker implant (i.e., a low resistivity, deep implant providing contact to an N-plus buried layer) is available in the technology, the diode area should be filled with sinker. A large number of contacts should also be provided for the cathode contact. The packaged devices must have a backside contact

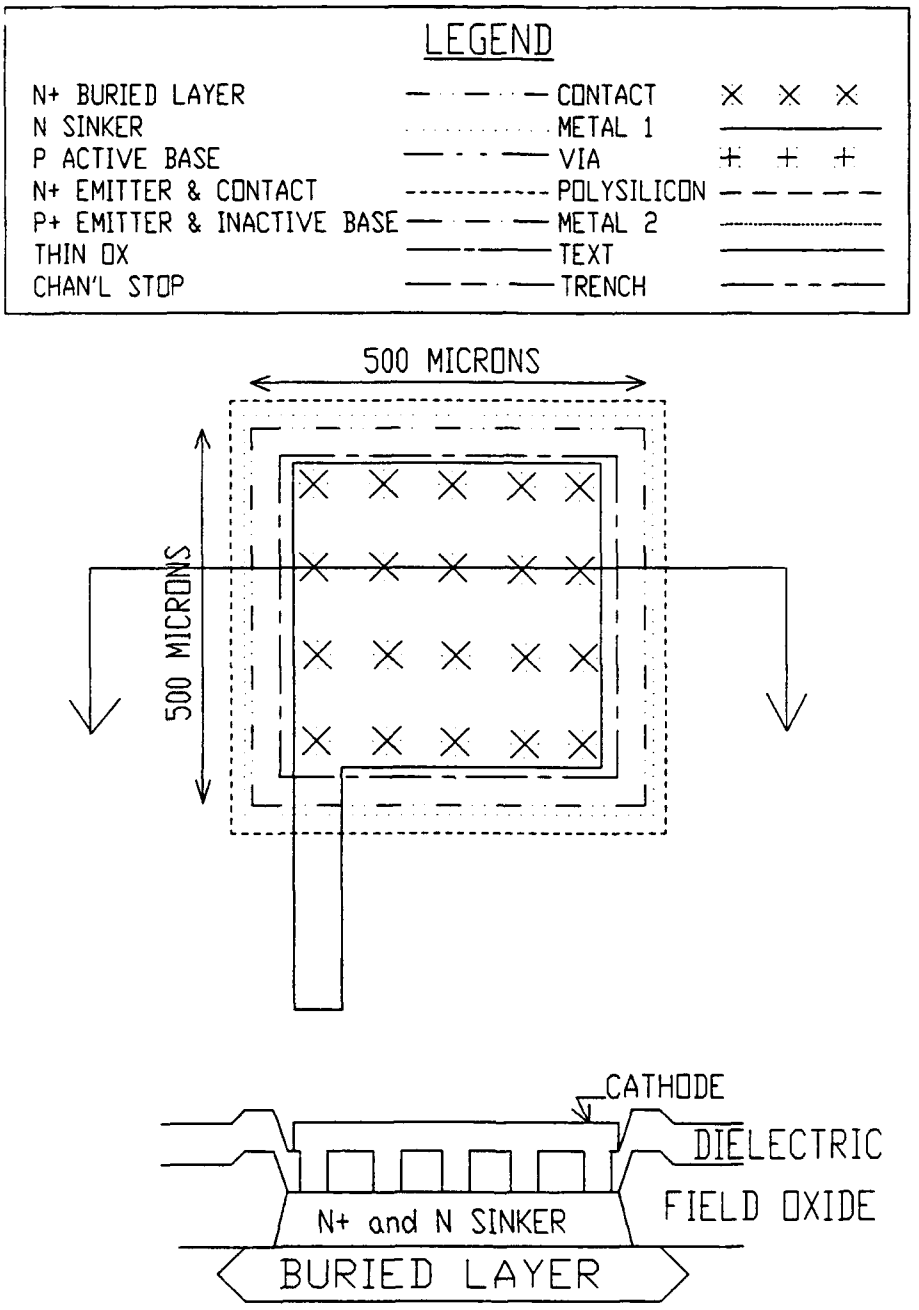


Figure 67. Buried layer/substrate photodiode with minimum aspect ratio and no guardband.

to the substrate. That contact should yield a low contact resistance.

11.6.4 Applications

This structure will be used to determine the maximum photocurrent that can be collected at a node. In bipolar technologies, the collector node photocurrents often dominate the photoresponse of the circuits because of the large collector/substrate area and the long lifetime in the substrate. Therefore, the amplitude and waveshape of this photocurrent must be measured carefully. The interactions with adjacent devices and with surrounding guardbands can also be quite important. These are addressed in the following structures.

11.7 Photodiode—Buried-Layer/Substrate, No Guardband, and Large Aspect Ratio

11.7.1 Purpose

The buried-layer/substrate, large-aspect-ratio diode, as shown in figure 68, is used to emphasize the lateral collection component of primary photocurrent as a function of dose rate.

11.7.2 Description

This diode is typically a rectangular device with the same area as device 11.6 but with a much larger aspect ratio. As with device 11.6, a collector sinker implant should be included to make good contact to the buried layer along its entire length. Several contacts should be made to the cathode along the entire length.

11.7.3 Special Design Considerations

Since the device will be quite long, it might be located near the edge of the die. It should be separated by one diffusion length from the edge and by two diffusion lengths from the nearest device or substrate contact.

11.7.4 Applications

This device will be used to determine the value of the lateral photocurrent collected by the buried layer. The data taken with this device should be compared with that taken with device 11.6 to determine the amount of photocurrent due to lateral collection.

11.8 Photodiode—Buried-Layer/Substrate with Guardband of Minimum Width and Spacing

11.8.1 Purpose

The buried layer/substrate diode with minimum dimension guardband as shown in figure 69 is used to evaluate the effectiveness of the guardband for intercepting the lateral component of the primary photocurrent.

11.8.2 Description

This structure consists of an interior diode with the same dimensions as device 11.6. It is enclosed by a buried layer ring. It is conceptually similar to an input clamp diode with a surrounding guardband which is used to suppress ringing in many bipolar technologies. Attention should be given to providing enough contacts to both the interior diode and the surrounding guardband. The guardband should be strapped with metal. Only the backside substrate contact is used. Connections to the interior diode and the guardband should be brought out to separate pads.

11.8.3 Special Design Considerations

The structure should be separated from the nearest device by two diffusion lengths.

11.8.4 Applications

This device can be used to help separate the lateral photocurrent collection from

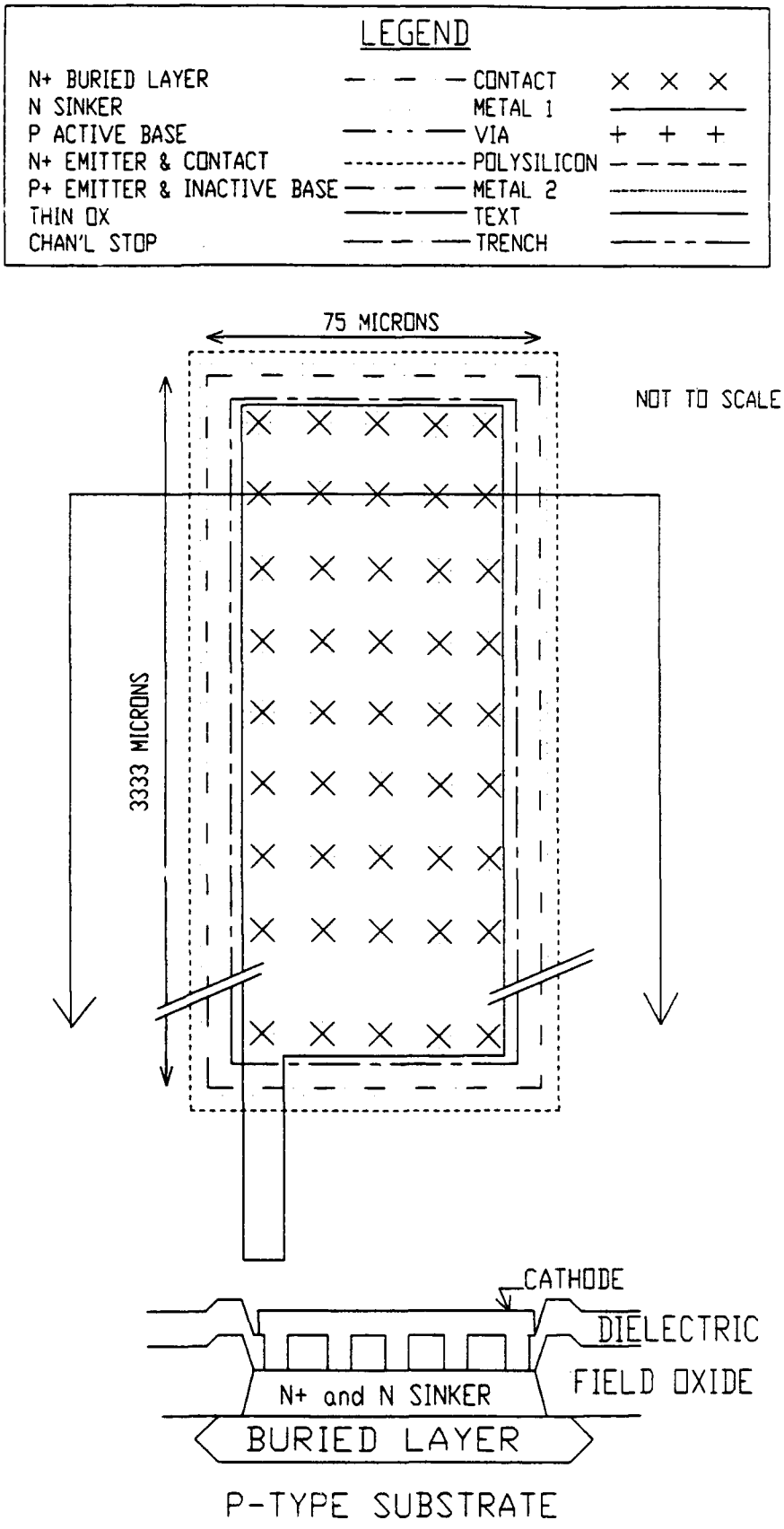


Figure 68. Buried-layer/substrate photodiode with large aspect ratio and no guardband.

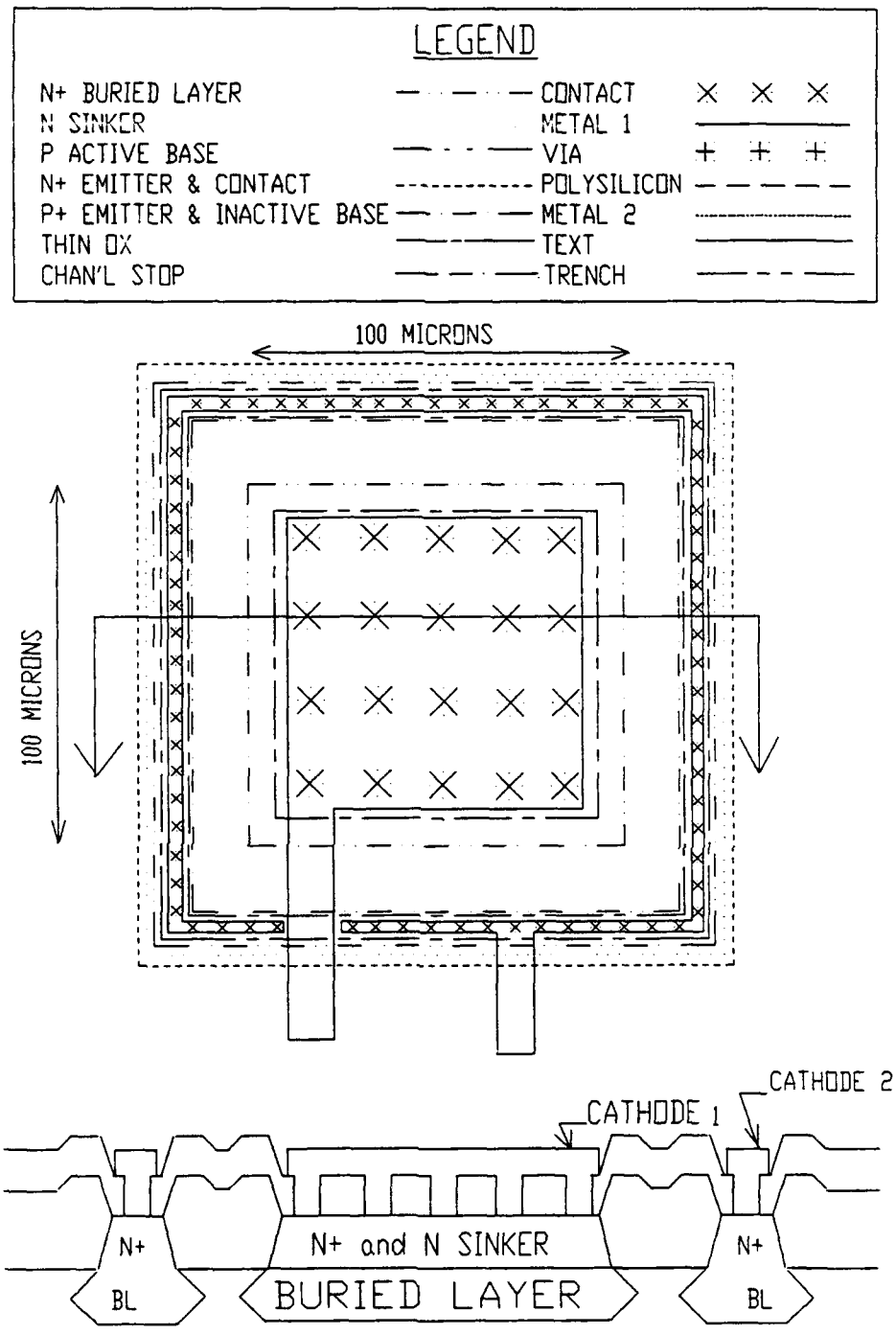


Figure 69. Buried-layer/substrate photodiode with guardband of minimum width and spacing.

the vertical collection. The surrounding buried layer ring is usually effective in collecting the lateral component of the photocurrent, and thus preventing it from reaching the interior diode. Comparison of the response of this structure to the devices described in 11.6 and 11.7 can be particularly helpful in separating the vertical and lateral photocurrent components. Note that this structure may also exhibit secondary photocurrent effects. The primary photocurrent flowing through the parasitic substrate resistance produces a large enough voltage drop to forward bias one or both junctions. The primary photocurrents will then be multiplied by the gain of the lateral parasitic transistor. This effect will be evidenced by the relationship of photocurrent to dose rate becoming super-linear at high dose rates. It may also be affected by biasing the guardband at either ground or V_{cc}.

11.9 Photodiode—Buried-Layer/Substrate with Guardband of Large Width and Minimum Spacing

11.9.1 Purpose

The buried layer/substrate diode surrounded by a large guardband as shown in figure 70 is used to evaluate photocurrent collection of devices in a high-density layout.

11.9.2 Description

This structure consists of an interior, buried-layer diode surrounded with buried-layer guard ring. The interior diode is typically sized to yield a measurable photocurrent at the anticipated upset dose rate for the technology. The guard ring is spaced at a minimum distance from the interior diode and is at least one diffusion length wide. Separate contacts are provided for the interior diode and the guard ring.

11.9.3 Special Design Considerations

This device can be placed adjacent to other test structures. It does not require separation of two diffusion lengths from its nearest neighbor.

11.9.4 Applications

When devices are located in a high-density array (e.g., memories or gate arrays) with minimum separation, photocurrent collection may be more closely described by a one-dimensional model. Lateral collection may be much less important since many devices are competing for the same collection volume. Comparison of the response of this structure to the devices in sections 11.6 through 11.8 can provide insight into differences in photocurrent collection in densely packed arrays as opposed to collection in I/O circuits located on the periphery of the die.

11.10 Photodiode—Buried Layer/Substrate with Surrounding Substrate Contact

11.10.1 Purpose

The buried-layer/substrate diode with a surrounding substrate contact as shown in figure 71 is used to evaluate the effectiveness of a topside contact to the substrate in interrupting lateral photocurrent collection.

11.10.2 Description

This structure consists of a buried-layer diode which is sized to provide a measurable photocurrent at the expected upset threshold based solely on the vertical collection volume. It is surrounded by a topside contact to the substrate with minimum design rule dimensions and spacing between diode and substrate contact. Independent pads are provided for the diode and the substrate contact.

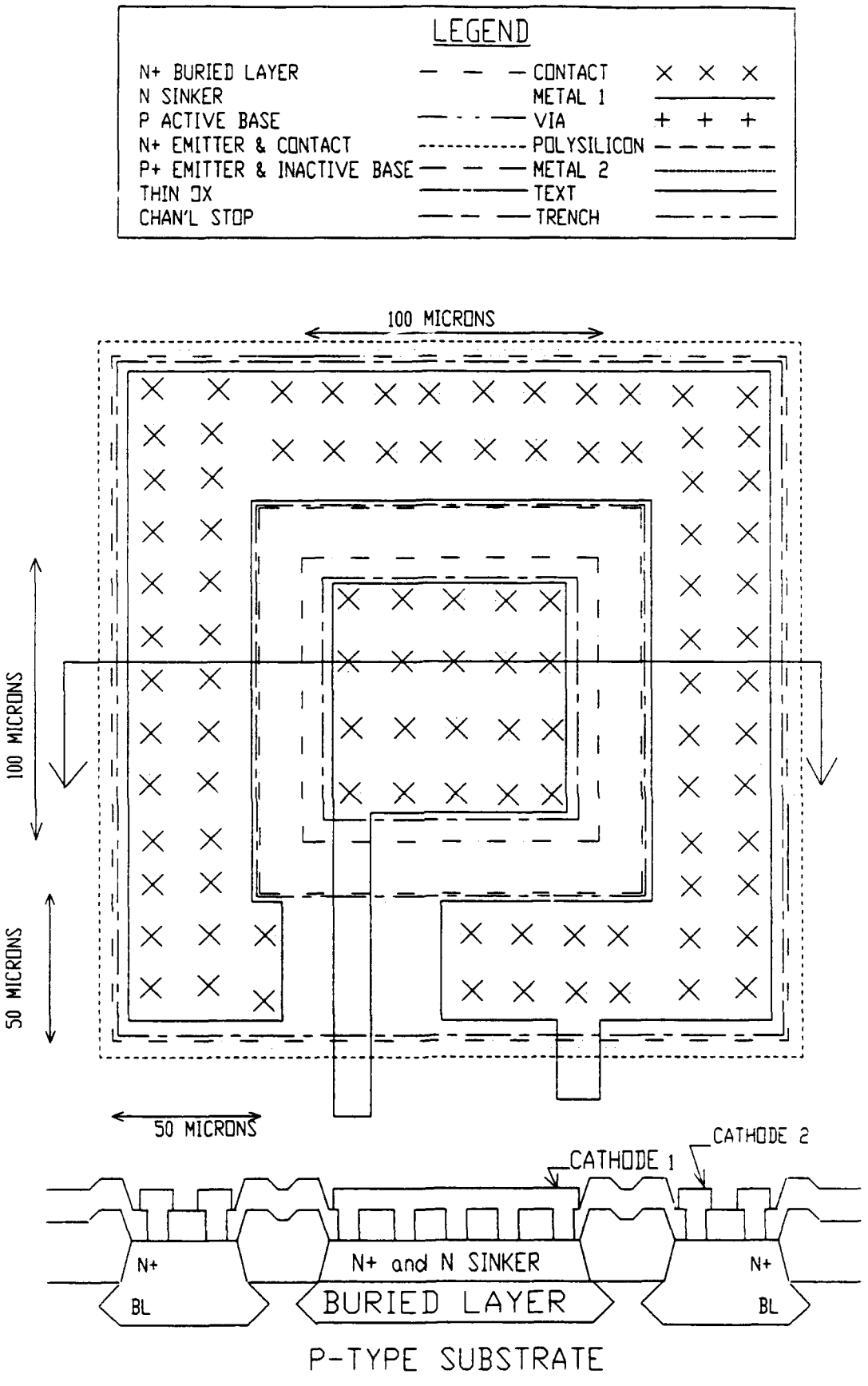


Figure 70. Buried-layer/substrate diode with guardband of large width and minimum spacing.

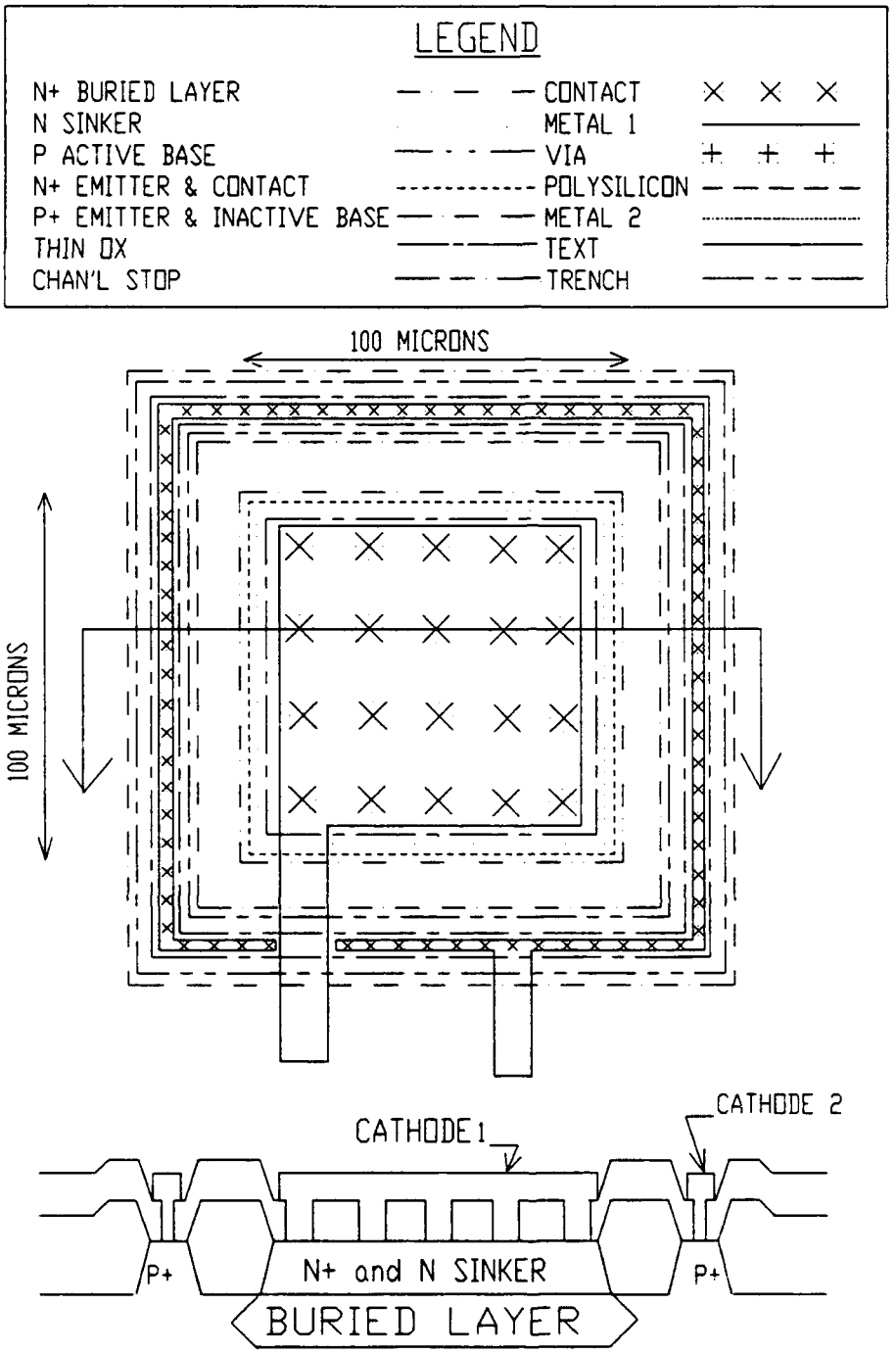


Figure 71. Buried-layer/substrate photodiode with surrounding substrate contact.

11.10.3 *Special Design Considerations*

This structure should be separated from the nearest device by two diffusion lengths. The metallization contact to the substrate contact structures should extend all the way around the device. The substrate contact may have a relatively high resistance and require a metallization strap to ensure a low impedance path for the photocurrent. The substrate contact should be brought out to a pad that is separate from all other substrate contacts.

11.10.4 *Applications*

A topside contact to the substrate can provide a region of high recombination velocity which is effective in reducing lateral photocurrent collection. In comparison to a buried-layer guard ring, the substrate contact has the advantage of no secondary photocurrent. In some technologies, the minimum design rule spacing may be less for substrate contacts than for guard ring diode. If this is the case, tighter packing densities may be achieved.

11.11 *Photodiode—Base/Collector with Minimum Aspect Ratio*

11.11.1 *Purpose*

The base/collector diode, as shown in figure 72, is used to determine the primary photocurrent for the base/collector junction.

11.11.2 *Description*

The device is a diode with contacts to the base region and the collector. It is surrounded by a substrate contact ring. If possible the device should be sized to provide a measurable photocurrent at the expected upset threshold. However, the collection volume for the base/collector region is quite small. The design may have to be compromised to limit the size to a reasonable area. This may require photocurrents to be measured at a higher dose rate and extrapolated to the lower values.

11.11.3 *Special Design Considerations*

In bulk substrate technologies, the collector/substrate diode is an unavoidable parasitic associated with the transistor. Both the base/collector photocurrent and the collector/substrate photocurrent will be flowing through the collector contact. The device should be laid out to minimize any secondary photocurrent effects resulting from the parasitic PNP transistor formed by the intentional base, collector, and substrate. This can be done by providing two collector contacts, a large area base contact, and a surrounding substrate contact. The base and collector contacts should be brought out to separate pads.

11.11.4 *Applications*

The base/collector photocurrent should be measured with the current probe in the base lead to prevent corrupting the data with the collector/substrate photocurrent. The resulting photocurrent data should be reduced to provide photocurrent per unit area so that it can be scaled to areas associated with actual transistor dimensions.

11.12 *Phototransistor with Typical Aspect Ratio*

11.12.1 *Purpose*

The phototransistor as shown in figure 73 is used to determine the photoresponse of a typical transistor as a function of dose rate. It may also be used to verify predictions of transistor response based on transistor models and scaled values of base/collector and collector/substrate primary photocurrents.

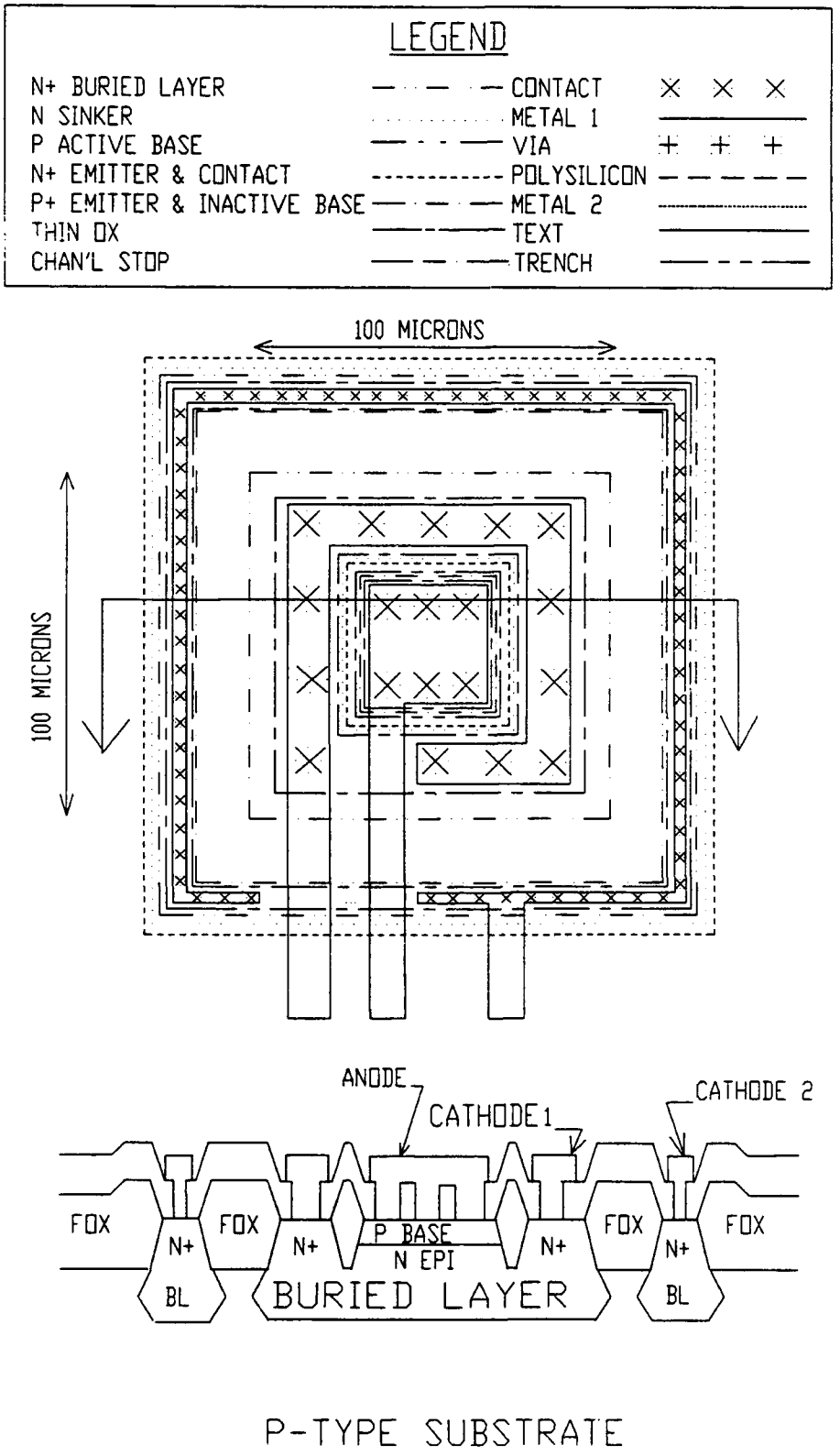


Figure 72. Base/collector photodiode with minimum aspect ratio.

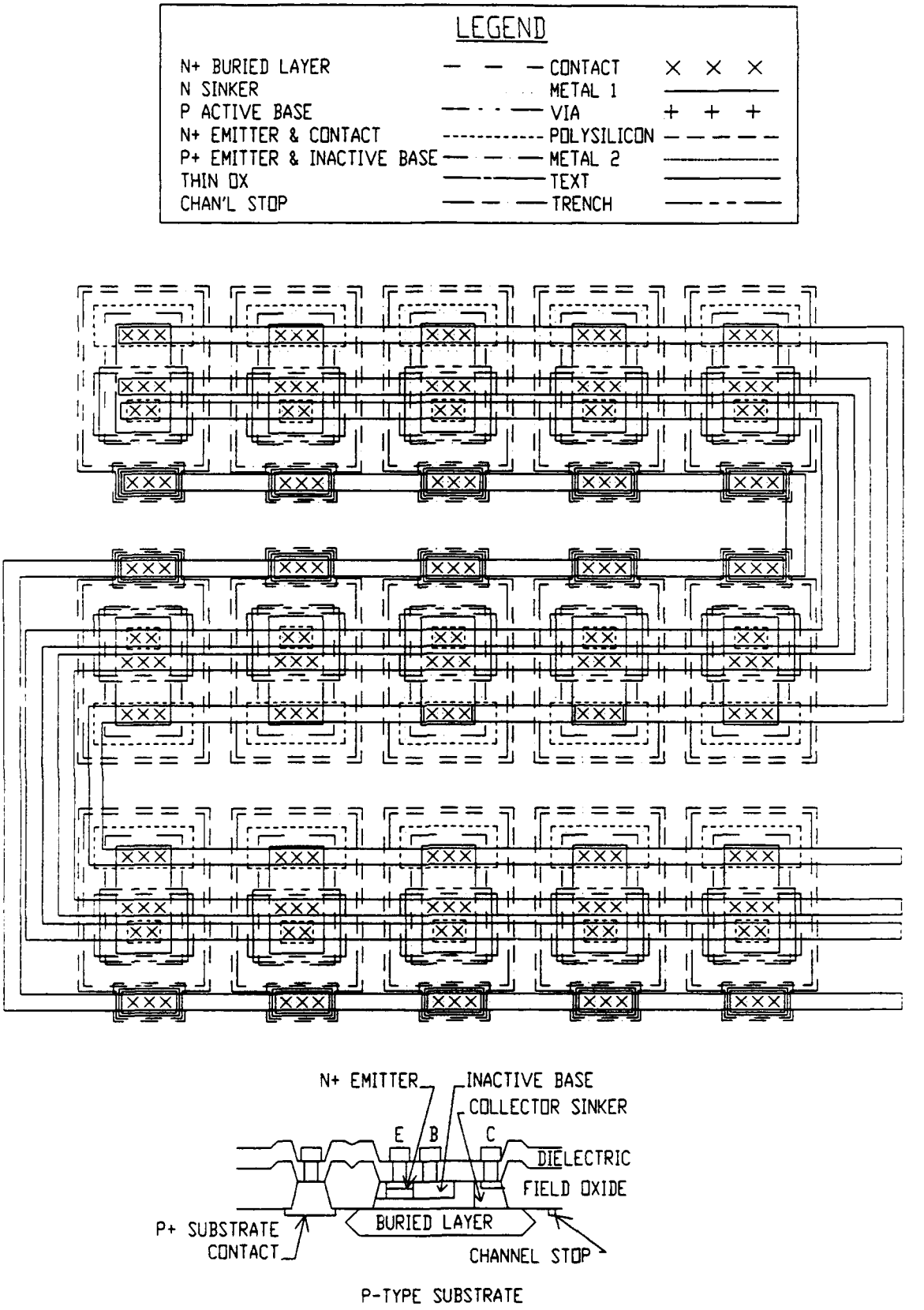


Figure 73. Phototransistor with typical aspect ratio.

11.12.2 Description

The phototransistor structure maintains the same aspect ratio as a typical transistor from the device library. However, it may be scaled up to provide a larger photoresponse signal. Individual pads should be provided for the emitter, base, and collector. The substrate contact may share a pad with other substrate contacts on other structures.

11.12.3 Special Design Considerations

Particular attention should be given to keeping the base resistance of this test device similar to that found in a typical transistor from the device library. The voltage dropped across the base resistance is responsible for the turn-on of the emitter base junction and consequently secondary photocurrent. If there are many transistor types in the library, several phototransistor test structures may be required to evaluate the dose rate response of each type.

11.12.4 Applications

Accurate modeling of base resistance is one of the most difficult aspects of bipolar transistor simulation. Therefore, it is advisable to include a means for experimentally verifying photocurrent inclusive models whose parameters have been extrapolated from diode measurements.

12. MULTIDEVICE STRUCTURES

12.1 Introduction

The test structures described in this section involve multiple devices which may or may not share a common isolation region or common buried layer. These structures represent parasitic paths associated with intentional devices which may be activated by ionizing dose or dose rate environments. The result may be a leakage path or a latchup condition between adjacent devices.

12.2 Four-Layer Path in a Shared Isolation Tub

12.2.1 Purpose

The four-layer path (PNPN) in a shared isolation tub, as shown in figure 74, is used to determine the latchup characteristics (i.e., switching voltage, triggering dose rate, holding voltage, and holding current) of a latch path between devices within a shared isolation tub.

12.2.2 Description

The structure shown in the figure simulates a resistor in the same isolation region as a transistor. However, similar structures could be developed to simulate:

1. diode and transistor,
2. two transistors, or
3. diode and resistor sharing an isolation area.

The figure contains similar devices shown in both a junction-isolation technology and a bipolar, recessed-field-oxide technology. The recessed field oxide structure is shown with the transistor and resistor in separate epi tubs but sharing a common buried layer. The recessed field oxide is represented as not extending all the way to the buried layer and consequently leaving a section of material with long lifetime which may participate in a latch path. The gap between the recessed field oxide and the buried layer may be intentional or may be the result of a processing error. Separate pads should be provided for each region in the PNPN path.

12.2.3 Special Design Considerations

Minimum design rule spacings should be used for adjacent elements (i.e., the transistor and resistor). Devices should be oriented to maximize the gain of transistor in the parasitic PNPN path.

12.2.4 Application

The best practice for latchup prevention is to permit only one element per isolation region. Unfortunately, the designer may inadvertently include multiple devices in a region. Design rule checkers should be programmed to ensure that such a design error is detected. If design rules permit multiple devices in an isolation region (generally a bad practice), an empirical evaluation of the latchup parameters should be made to ensure that latchup indeed does not occur or that the holding conditions (current and voltage) cannot be maintained after the radiation event. Plans for hardness assurance monitoring must also be made.

Latchup can be eliminated as a problem if:

1. Potential latch paths can be shown to be latch-free under worst-case conditions;
2. The holding voltage and/or holding current at all temperatures cannot be maintained due to specific limitations of supply voltage or current;

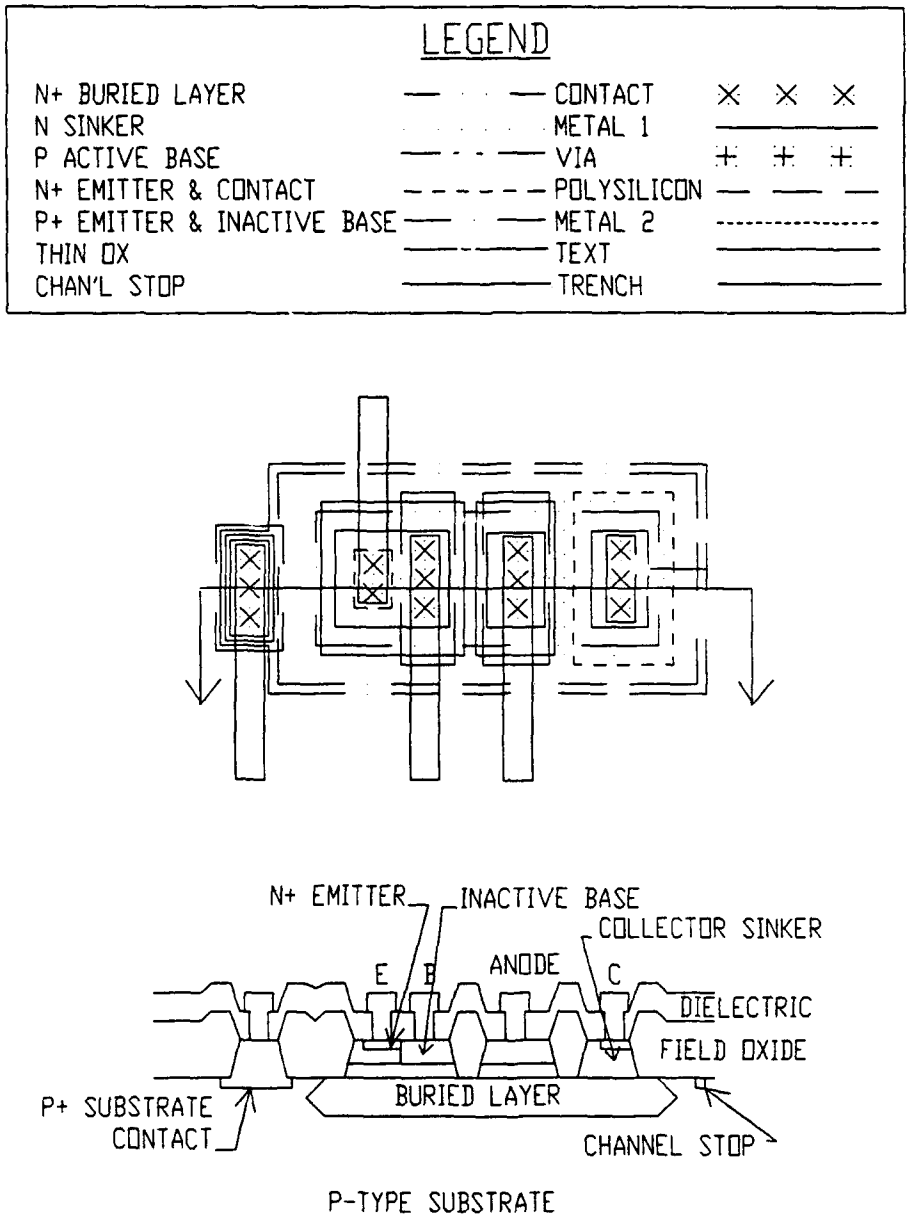


Figure 74. Four-layer latchup path in a shared isolation tub.

3. Circuit connections prevent latchup from occurring (e.g., Darlington connection of transistors in the same isolation region).

12.3 Schottky Diode Sharing a Buried Layer with a Transistor

12.3.1 Purpose

The transistor with a Schottky diode in the collector as shown in figure 75 is used to evaluate possible latchup conditions in those technologies which use Schottky diodes for signal coupling between logic gates.

12.3.2 Description

This structure is a simple inverter stage which incorporates the Schottky diode as an integral part of the collector. Although several diodes are typically included in the collector, only the closest diode-to-transistor spacing is of interest in this structure. Individual pads are provided for the Schottky anode, collector, base, and emitter of the transistor.

12.3.3 Special Design Considerations

Minimum design rule spacing should be used between the Schottky diode and the transistor.

12.3.4 Applications

The latch path simulated with this structure includes the Schottky diode as the emitter of the PNP transistor. Schottky diodes are typically poor minority carrier emitters. However, depending on the Schottky barrier metal, the type of processing performed, and the proximity and gain of the NPN transistor, this structure could conceivably latch. Testing on a worst-case path of this type can be used to ensure that no latch is possible for the particular processing used or that the holding voltage and/or holding current conditions cannot be sustained after the radiation event.

12.4 Adjacent Transistors in Separate Buried Layer Regions

12.4.1 Purpose

Adjacent transistors in separate buried layer regions as shown in figure 76 are used to determine the latchup characteristics (i.e., switching voltage, triggering dose rate, holding voltage, and holding current) of a latch path involving the substrate.

12.4.2 Description

This structure is composed of two typical dimension transistors placed side by side at minimum spacing. Substrate contacts are placed on either side of the latch path to facilitate measurement of gain characteristics for the parasitic transistors (lateral NPN and vertical PNP). Additional substrate contacts should be placed at spacing and orientation designated by the design rules. Individual pads should be provided for the base and collector of one transistor, the collector of the second transistor, the near substrate contacts, and the distant substrate contacts.

12.4.3 Special Design Considerations

If the test chip is to be used in process development, the designer may wish to include several of these structures. Additional structures could include variations in transistor spacing and location of substrate contacts. If three transistors are used, two buried-layer-to buried-layer spacings could be investigated.

12.4.4 Applications

The latch path for this structure includes:

1. The base (anode) and collector (anode gate) of one transistor and

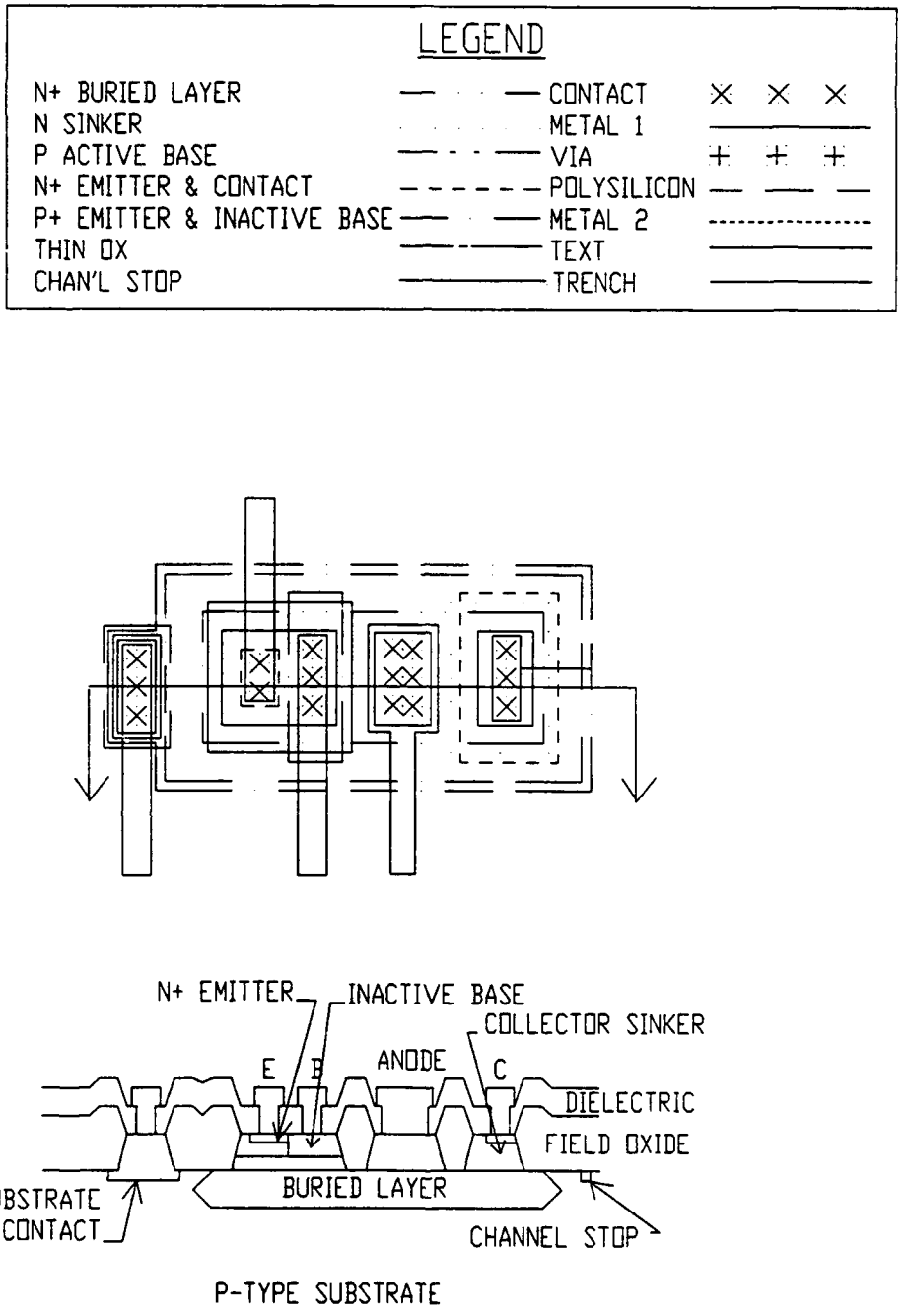


Figure 75. Latchup path involving a Schottky diode in a shared buried layer.

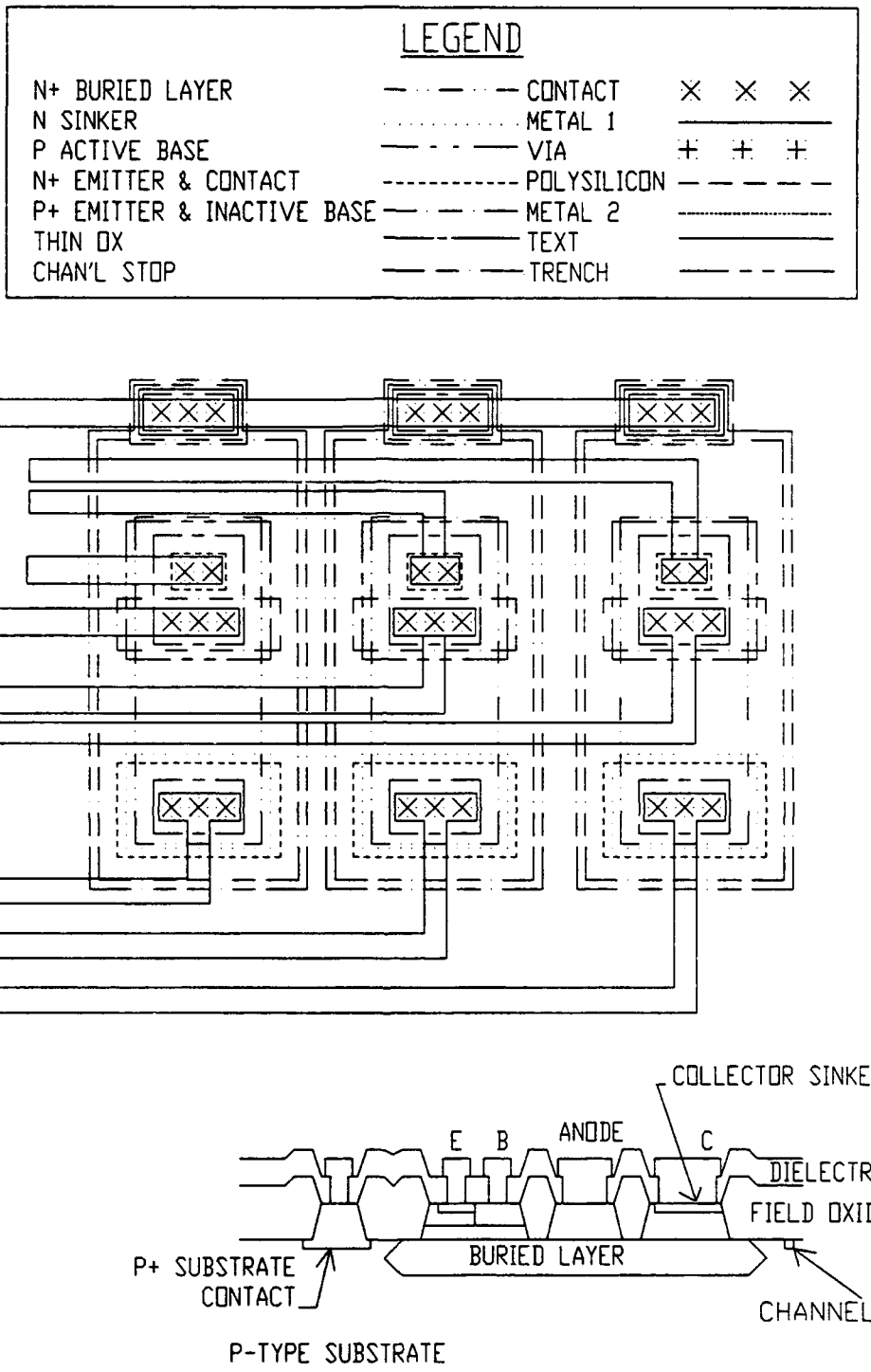


Figure 76. Latchup path involving separate transistors in separate buried layer regions.

2. The substrate (cathode gate) and the collector (cathode) of the second transistor.

In some technologies, mask misalignments may cause a space between the recessed field oxide and the buried layer. This can greatly increase the gain of the vertical PNP transistor. The designer may wish to use multiple, orthogonal layouts of this structure to detect such misalignments. Alternatively, intentional misalignments can be included in the layout.

12.5 Adjacent Transistor and Resistor in Separate Buried Layer Regions

12.5.1 Purpose

The adjacent transistor and resistor in separate buried layer regions as shown in figure 77 are used to determine the latchup characteristics (i.e., switching voltage, triggering dose rate, holding voltage, and holding current) of a latch path involving the substrate.

12.5.2 Description

This structure is composed of a typical transistor and resistor with adjacent buried layers separated by minimum spacing. Substrate contacts are placed on either side of the latch path to facilitate measurement of gain characteristics for the parasitic transistors (lateral NPN and vertical PNP). Additional substrate contacts should be placed at spacing and orientation designated by the design rules. If the design rules do not require resistors to be plugged (i.e., shorted to the epi tub on the high-voltage side of the resistor), separate connections should be made to the resistor and epi tub. If the technology permits multiple resistors in an epi tub, the designer may wish to provide other tub contacts at a variety of distances from the latch path. All tub contacts should be brought out to individual pads. Also, individual pads should be provide for the base and collector of the transistor, the near substrate contacts, and the distant substrate contacts.

12.5.3 Special Design Considerations

If the test chip is to be used in process development, the designer may wish to include several of these structures. Additional structures could include variations in spacing between transistor and resistor and location of substrate contacts. An additional transistor could be placed on the other side of the resistor at another spacing.

12.5.4 Applications

The latch path for this structure includes:

1. The resistor material (anode) and epi tub (anode gate) of the resistor and
2. The substrate (cathode gate) and the collector (cathode) of the transistor.

In some technologies, mask misalignments may cause a space between the recessed field oxide and the buried layer. This can greatly increase the gain of the vertical PNP transistor. The designer may wish to use multiple, orthogonal layouts of this structure to detect such misalignments. Alternatively, intentional misalignments can be included in the layout.

12.6 Field Oxide FET with Adjacent Buried Layers for Drain and Source

12.6.1 Purpose

The adjacent buried layers as shown in figure 78 form at thick field oxide MOSFET which is used to evaluate total-dose-induced leakage [107].

12.6.2 Description

This structure consists of two buried layers with dimensions defined by typical transistors. Collector contact diffusions have

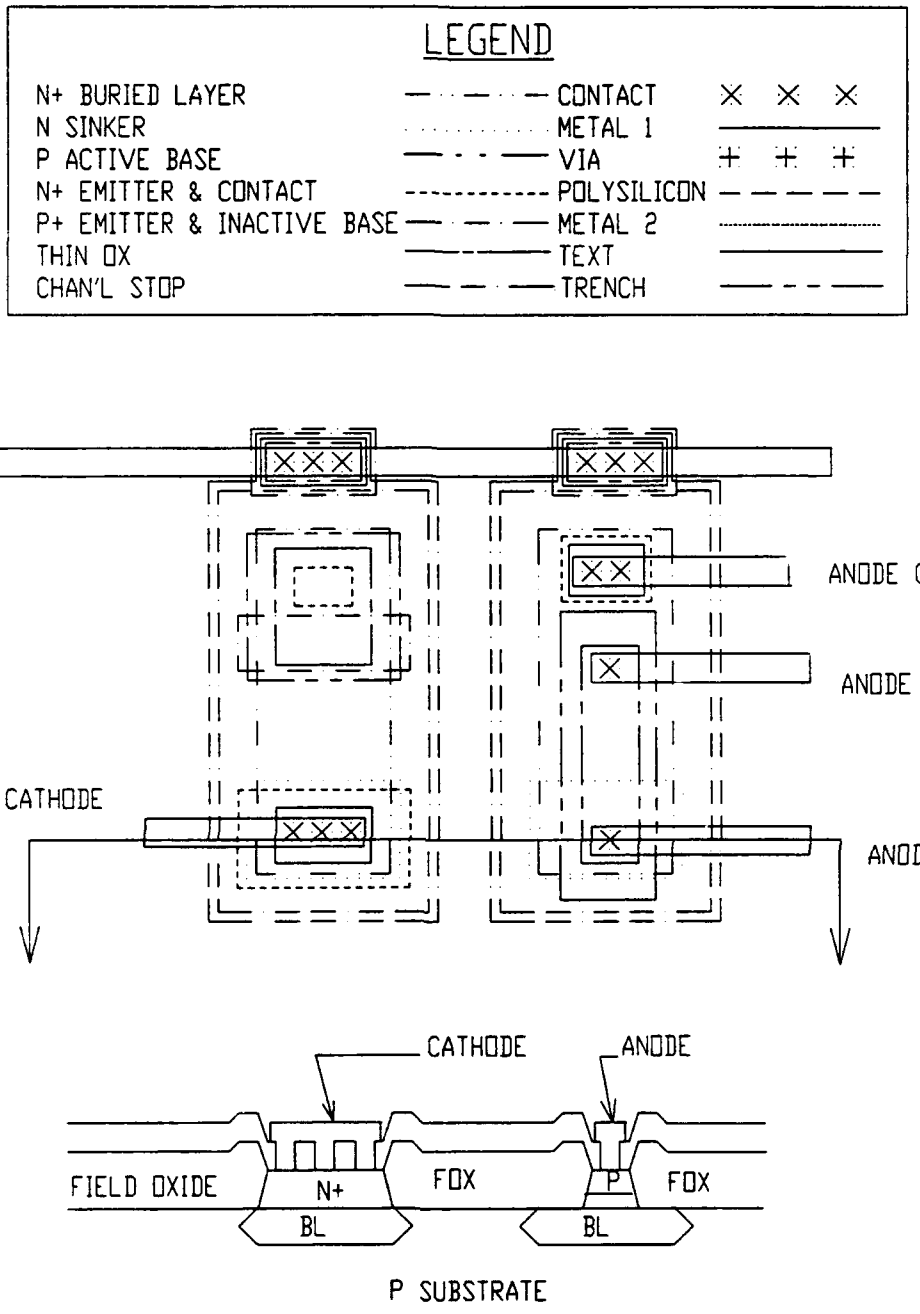


Figure 77. Latchup path involving a transistor and resistor in adjacent buried layers.

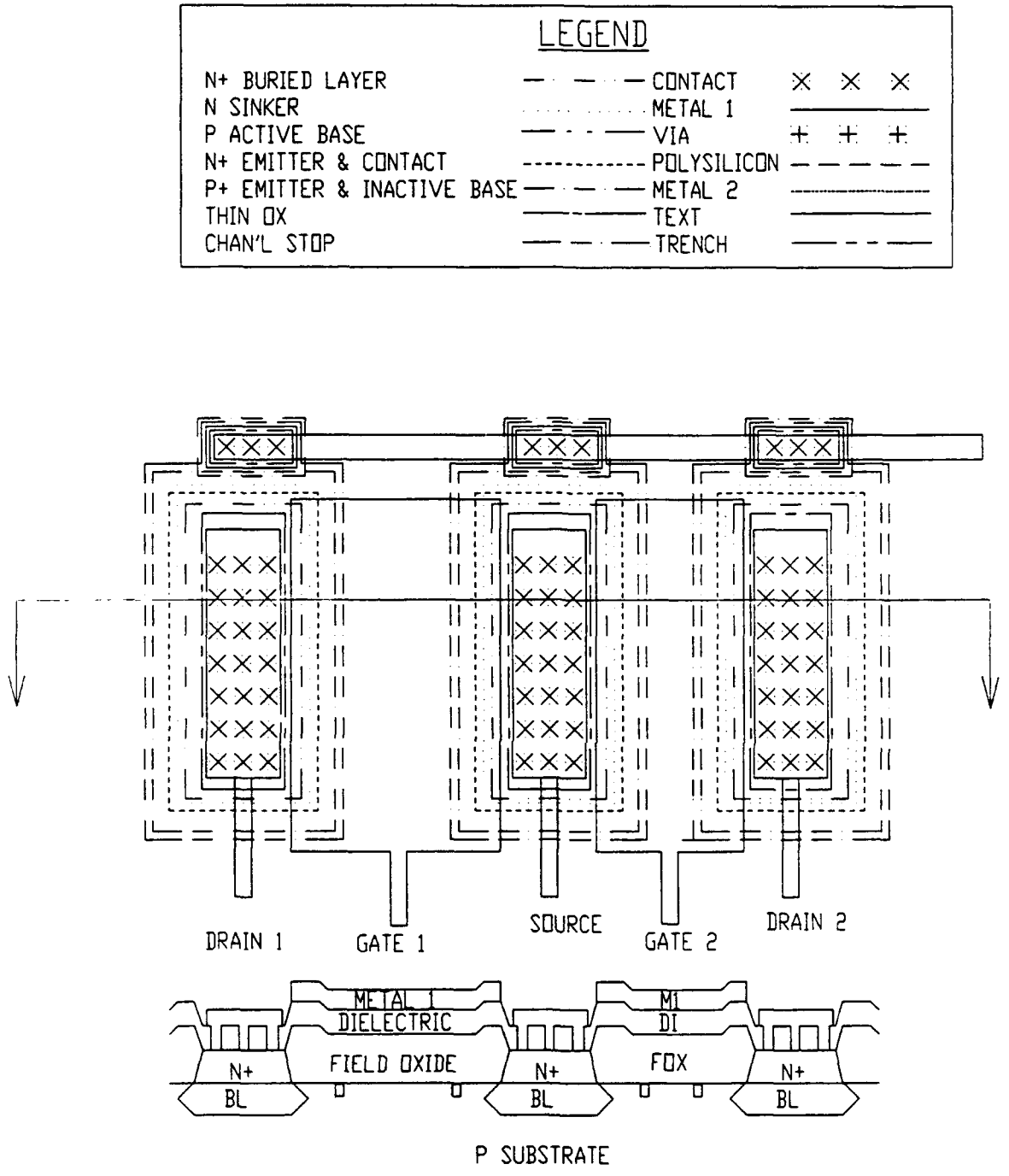


Figure 78. Field oxide parasitic FET for bipolar technology.

been included in the epi tubs to ensure good contacts to the buried layer regions. The buried layers constitute the drain and source of a thick field oxide MOSFET. Typically several variations of the structure are included to investigate the sensitivity of the total ionizing dose-induced leakage to:

1. Buried layer to buried layer spacing,
2. Dimensions of channel stop implants located between the buried layers, and
3. Dimensions of metal gates over the parasitic MOSFET channel.

Individual pads are required for the gates and drains. Sources may share a common pad.

12.6.3 Special Design Considerations

Each of these devices should be surrounded by a channel stop with a substrate contact. The connection for the first level metal gate should be brought in on metal 2. This restricts the leakage current to just the region between the buried layers in the device.

12.6.4 Applications

Buried-layer-to-buried layer leakage is a dominant failure mechanism in bipolar technologies employing a recessed field oxide. The leakage is affected by the spacing between buried layers and the existence and bias condition of metallization overlaying the parasitic channel. The threshold dose for the onset of leakage can be increased by placing a channel stop implant between the buried layers. This structure and its variations can be beneficial in determining the design rules required to minimize the radiation-induced leakage problem.

12.7 Annular Field Oxide FET with Metal-1 Gate

12.7.1 Purpose

The annular field oxide MOSFET as shown in figure 79 is used to evaluate buried-layer-to-buried-layer leakage associated with transient suppression diodes on input terminals.

12.7.2 Description

This structure is a typical input transient suppression diode surrounded by a buried layer ring. Two variations are shown. In the first, the first level metal connection to the cathode bridges the region between the buried layer ring and the diode buried layer. In the second, a section has been removed from the buried layer ring, and the connection to the diode cathode runs through the gap. Thus, there is no gate bridging directly between the parasitic source and drain. A channel stop implant has been located midway between the two buried layer regions. Independent pads are provided for the diode cathode and the buried layer ring. The substrate contact may be shared with other devices.

12.7.3 Special Design Considerations

Each of these devices should be surrounded by a channel stop with a substrate contact. The connection for the first level metal gate should be brought in on metal 2. This restricts the leakage current to just the region between the buried layers in the device.

12.7.4 Applications

Input leakage current is often the first parameter to exceed specifications as a result of irradiation of recessed field oxide, bipolar microcircuits. The increased leakage is typically

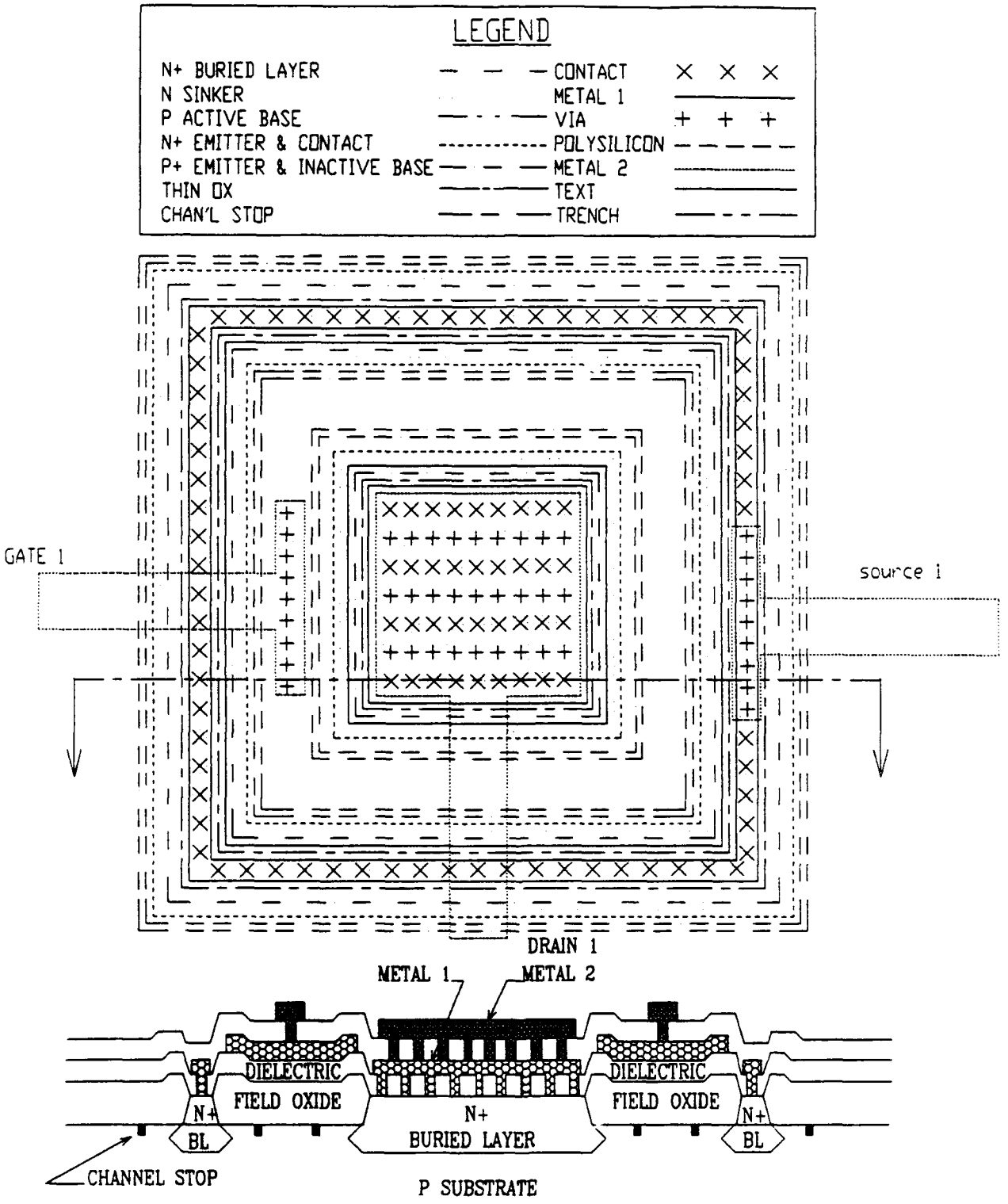


Figure 79. Annular field oxide FET with metal-1 gate.

caused by a radiation-induced channel between the input transient suppression diode and its surrounding buried layer. Structures such as this are useful in evaluating hardness improvements due to changes in spacing, width of channel stop, and other design modifications.

12.8 Gated Diode

12.8.1 Purpose

The gated diode structures similar to the device shown in figure 80 are used to determine surface recombination velocity in the base region of bipolar, NPN transistors, in the collector region of a bipolar, PNP transistor, and at the silicon/silicon-dioxide surface of buried layer/substrate diodes [1].

12.8.2 Description

The particular gated diode shown in the illustration is for base region investigations in an NPN transistor. Similar structures would be used for the other regions of interest for the technology. In each structure the field plate should overlap the PN junction and extend well into the P-type material.

12.8.3 Special Design Considerations

The area of the P-type material overlapped by the metal field plate in the gated diode should be approximately as large as the PN junction of the diode. This permits the signal from the gate controlled portion of the device to be as large as the background signal from the diode. Connection to the gate should be brought in on second-level metal with a via down to the first-level metal gate as close as possible to the device.

12.8.4 Applications

In bipolar devices, oxide trapped charge resulting from total dose irradiation tends to invert the surface of P-type regions associated with NPN and PNP transistors. This increases the volume of the junction depletion region and can greatly increase the recombination/generation leakage current. The gate is used to provide a compensating electric field to force the surface back into accumulation. This permits the surface contribution of the leakage current to be separated from the regular depletion region contribution.

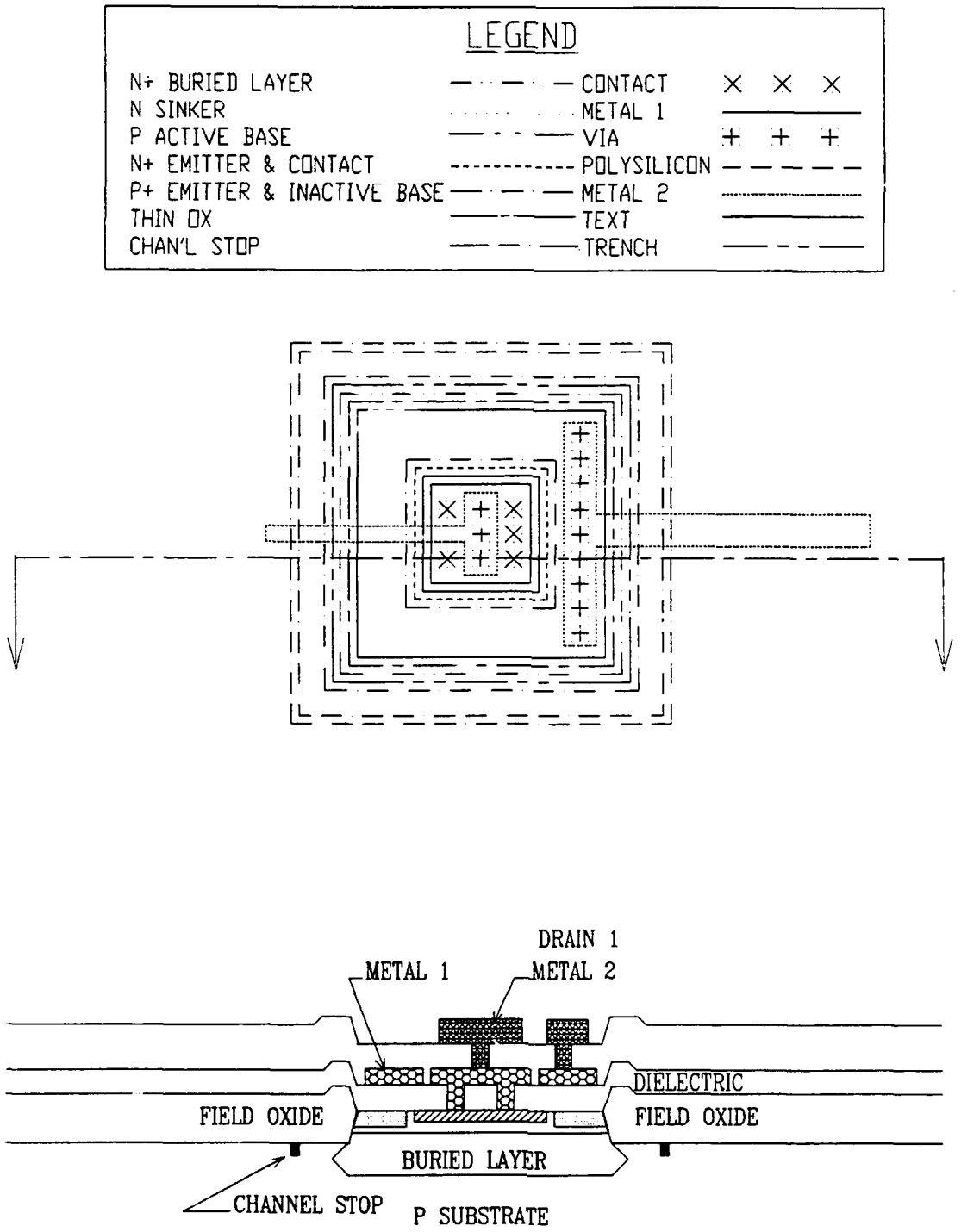


Figure 80. Gated diode test structure.

13. RESISTORS

13.1 Introduction

The test structures described in this section are used to evaluate radiation effects on diffused resistors which are typically used in bipolar technologies. Post-irradiation changes in resistor values may by especially important in analog microcircuits. Therefore, these devices should be carefully considered for test chips used with analog processes.

13.2 Maximum Resistivity Resistor with Field Plate

13.2.1 Purpose

The resistor with field plate as shown in figure 81 is used to determine the change in resistance caused by trapped oxide charge resulting from total ionizing dose.

13.2.2 Description

This structure consists of a ten square resistor with typical dimensions for the technology. It should contain no bends. It is overlaid by a level-1-metal field plate which completely overlaps the edges and is within minimum spacing of the resistor contacts. The resistor tub should be plugged (i.e., shorted to one end of the resistor). Terminals are provided for each end of the resistor and the field plate.

13.2.3 Special Design Considerations

These structures should be included for all P-type resistors using implants with sheet resistivity greater than 1000 ohms/square. If space permits, the designer may wish to include resistors with and without field plates. This simplifies testing and data interpretation.

High-resistivity polysilicon resistors may also be affected by oxide trapped charge. Similar test structures should be used for technologies which employ polysilicon resistors.

13.2.4 Applications

Charge trapped in the oxide as a result of total ionizing dose irradiations can result in the depletion or inversion of the surface of P-type resistors. This changes the resistivity and cross-section of the resistors and consequently their value. The effect is more pronounced in resistors made from higher resistivity layers. Since the amount of charge trapped in the oxide is a function of the electric field, a field plate has been placed over the resistor structure. Total dose measurements should be made as a function of applied bias up to the maximum power supply voltage used in the technology.

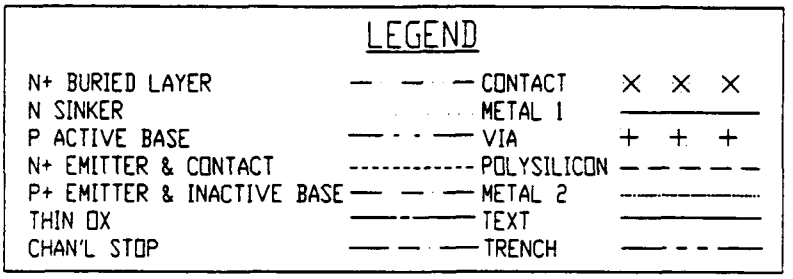
13.3 Resistor With and Without Tub/Resistor Tie

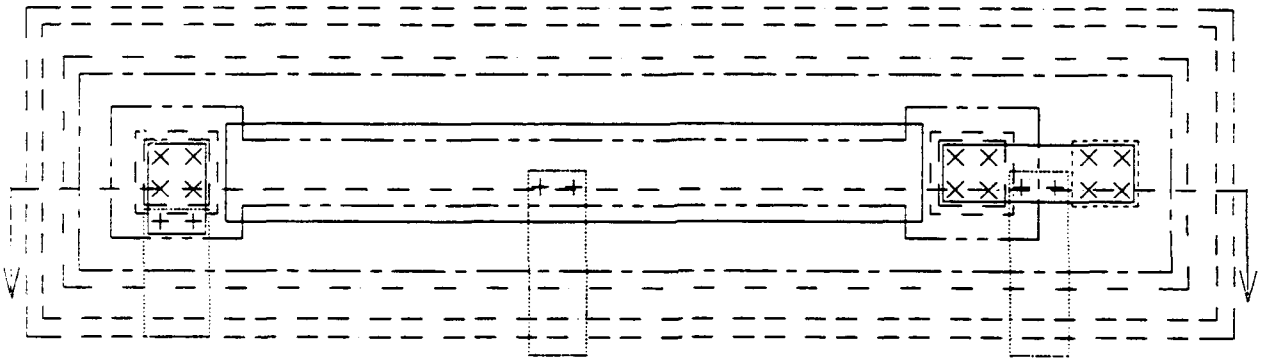
13.3.1 Purpose

The resistor structures shown in figure 82 are used to investigate effective resistance changes in an ionizing dose rate environment. Such structures are important in dielectrically isolated technologies in which diffused resistors are used for current limiting at high dose rate [108].

13.3.2 Description

Two types of dielectrically isolated resistors are shown in the figure. The first has a plugged tub (i.e., the resistor and tub regions are shorted by a metallization strip). The second has the tub region floating. The two resistors share a common pad for one terminal and have separate pads for the other. The resistors are at least ten squares long.





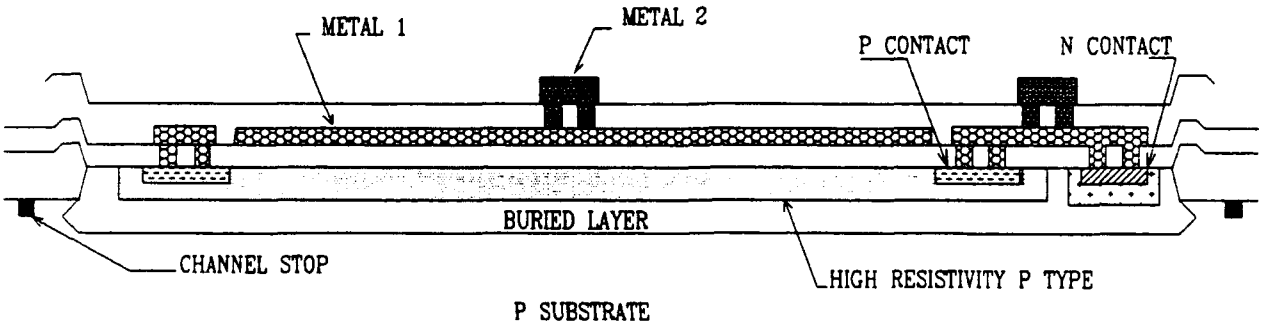


Figure 81. Diffused resistor with field plate.

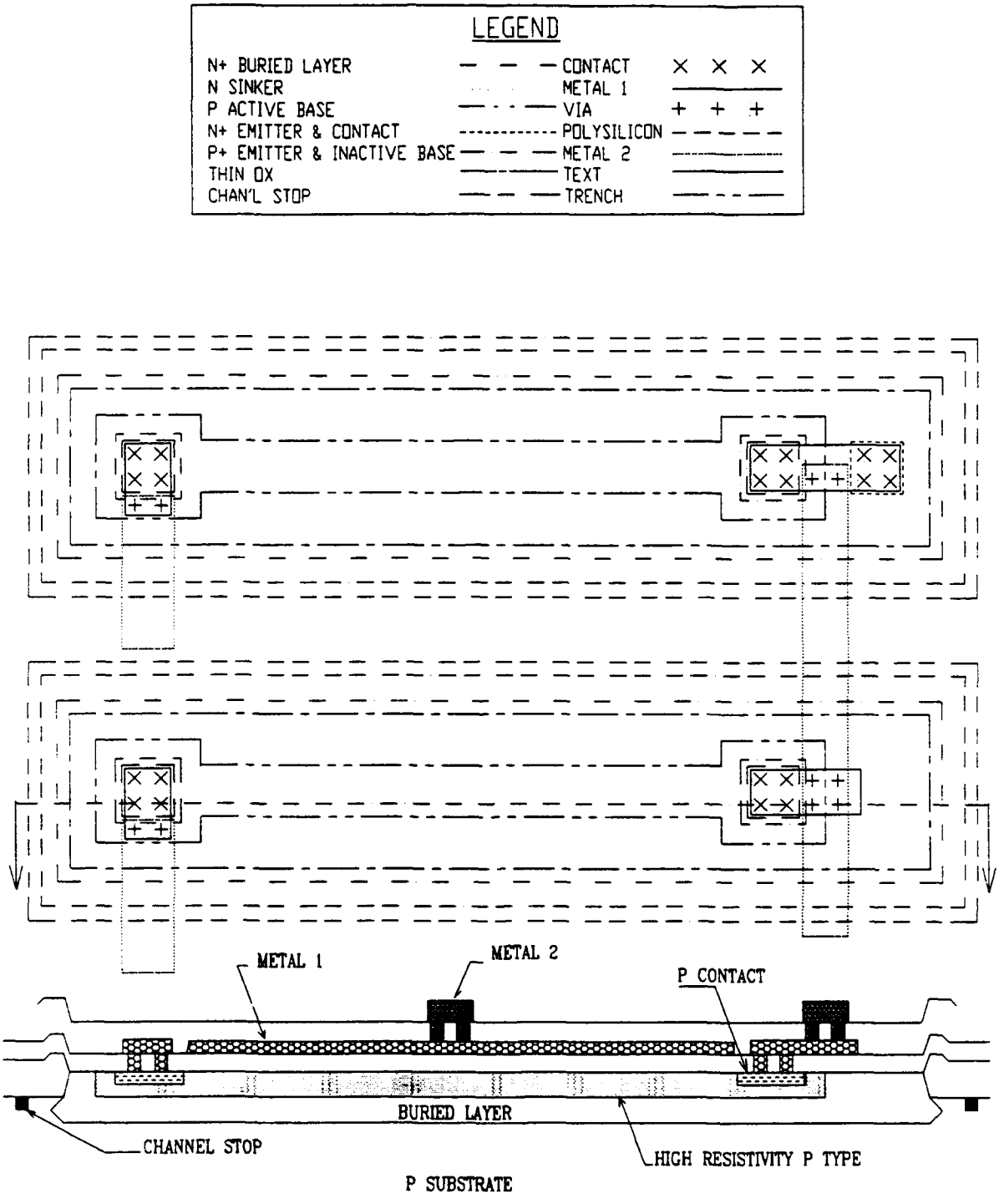


Figure 82. Diffused resistors with and without body ties.

13.3.3 *Special Design Considerations*

Changes in effective resistance during exposure to high-dose-rate ionizing radiation are most important for those resistors used for current limiting. Therefore, limiting resistors made from high-resistivity layers are typically given primary attention. However, resistors made from lower resistivity layers may also be important if a critical value of resistance must be maintained during exposure.

13.3.4 *Applications*

These devices are used to characterize resistance as a function of dose rate. The effective resistance during irradiation will depend on the initial resistivity, the depth of the tub material, and whether or not the tub is plugged. The change in effective resistance is the result of both conductivity modulation and photocurrent flowing between the resistor and tub material. Usually, the relationship between the dose rate and effective resistance is expressed in terms of the critical dose rate where the resistance is half its original value.

13.4 *Pinched Resistor*

13.4.1 *Purpose*

The pinched resistor structure shown in figure 83 is typically used as a hardness assurance monitor for neutron hardness as determined by base width and doping profile. It is included in process characterization and evaluation test chips in order to establish a correlation between pinched resistance values and post-neutron irradiation gain values [109].

13.4.2 *Description*

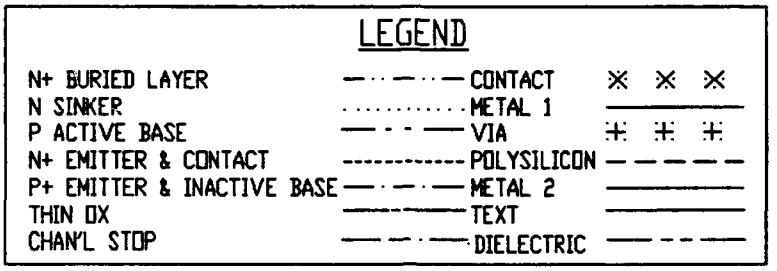
This device has the same cross-section structure as a bipolar transistor. However, its topological layout is similar to a JFET with the base acting as the channel and the emitter as the top side gate. The base contact which acts as the source is connected to the emitter (gate) contact so that a zero gate to source voltage is maintained. Correlations are typically made between the measured conductance (at Vgs = 0) and the neutron damage coefficient measured from data on an adjacent transistor.

13.4.3 *Special Design Considerations*

In process characterization test chips the pinched resistor structure should be placed near the transistor geometry, which is expected to limit the neutron hardness of the technology. The designer may wish to include the pinched resistor in his transistor library array.

13.4.4 *Applications*

The pinched resistor has the advantage of requiring only a simple dc measurement which is relatively temperature insensitive and can have a good correlation to the neutron damage coefficient. It is particularly useful for 100% electrical screening at the wafer level.



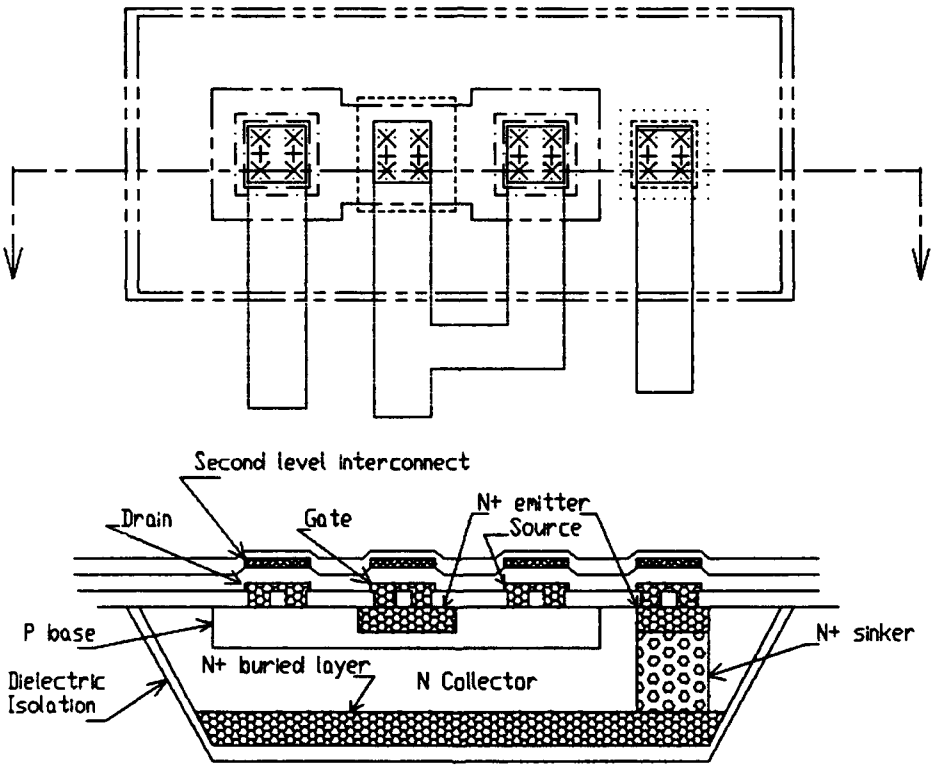


Figure 83. Pinched resistor test structure.

14. MACROCELLS

14.1 Introduction

The test structures described up to this point were designed to isolate specific radiation effects mechanisms as they relate to simple devices such as transistors, diodes, resistors, and capacitors. In some cases, the designs were selected to enhance the effects so that measurements were simpler or the signal-to-noise ratio was improved. The resultant test structures can be very much different from the devices used in the actual microcircuit layout. The test chip designer must remember that the goal of his effort is to develop techniques for radiation hardening of practical microcircuits [110]. Thus, the results of measurements on test chips must be relatable to microcircuit performance in a straightforward manner.

By including macrocells on the test chip, the designer can ensure that both test structures and macrocell circuits were processed from the same material under the same conditions and were exposed to the same radiation environment. This can greatly reduce the number of variables that must be considered in relating test structure results to circuit performance. Modeling procedures which extrapolate test structure results to circuit performance can be validated by comparing predictions and measurements for the macrocells contained on the test chip. The macrocell results also provide a check on the possibility that there is an unforeseen interaction among devices which may be important to post-irradiation circuit performance.

In selecting macrocells to include on a test chip, the designer must consider:

1. the amount of area available,
2. the number of output pads,
3. loading effects,
4. requirements for output buffers, and
5. the importance of a particular macrocell to microcircuit design.

In comparison to test structures, macrocells take up much more area and usually are designed to follow the layout rules defined for the technology. The design should be subjected to design rule checking to ensure that the layout rules have been followed. The input, output, and power supply pads should be arranged so that the device can be bonded out in a package. The output drive capacity of macrocells used for internal logic may be quite limited, especially after irradiation. The designer may wish to simulate worst-case design rules by increasing the output load with additional capacitance or active loads equivalent to the inputs of other cells. Care must be taken to prevent inadvertently overloading a macrocell output by requiring cells intended for internal logic to drive directly off-chip. Usually, properly sized buffers are required for the examining the output of macrocells used in internal logic.

In the following subsections, a few typical types of macrocells are identified and suggestions are made for their use on a test chip. The list is a very small subset of all the macrocells which could be examined. The test chip designer may use this as a starting point for the types of circuits which may be included on the chip and for the kinds of precautions which must be considered in their implementation.

14.2 Inverter/NAND/NOR Delay Chains and Ring Oscillators

14.3 Purpose

The delay chain/ring oscillator is used to determine the effect of radiation on propagation delay for typical inverters or logic gates for the technology. There is a great deal of literature on the design of delay chain circuits and the

interpretation of data from them [111–122]. The designer and test engineer should review this material carefully to ensure that the delay chain circuits are used appropriately.

14.4 Description

The delay chain or ring oscillator is one of the most widely used macrocell configurations for test chips. It consists of the series connection of a number of simple inverters or gates. For a ring oscillator, the output is fed back to the input, and an odd number of gates is required to provide an unstable state. A prime number of stages should be selected for a ring oscillator to suppress generation of harmonics. If frequency of oscillation measurements are made with a counter, care must be taken to ensure than the counter does not select a harmonic. For a delay chain, enough stages are required to ensure an easily measurable delay between the input and output. Since the chain is composed of internal logic devices, the output should be buffered to ensure that the results are not dominated by the output load. If the delay chain is split into a long chain and a short chain, the effects of the output buffer can be normalized out by subtracting the short chain measurement from the long chain measurement.

14.5 Special Design Considerations

In general, delay chains are more appropriate for radiation effects measurements than ring oscillators. Whereas the bias on the transistors in a ring oscillator is continually changing, the bias condition of each device in a delay chain can be set during irradiation. Since total ionizing dose effects are very sensitive to bias condition, the ability to set up a known bias condition is very desirable. It also makes the comparison of predicted and measured propagation delays much simpler since the predictions can be based on data taken from transistors irradiated under static bias conditions. If ring oscillators are used, they should include a gate to interrupt oscillation during irradiation so that a static bias condition can be obtained.

Delay chains are also preferable because they can be used to determine both low-to-high and high-to-low propagation delays. The values of the delays are often more representative of actual circuit operation because they swing between full output high and low levels. Ring oscillators tend to oscillate about the high gain portion of the inverter voltage transfer characteristic.

If sufficient area is available, the output buffers should be separated from the delay chain or ring oscillator if the device is going to be tested at wafer probe with an x-ray source. Sufficient separation should be maintained such that the output buffers can be shielded from the radiation. Typically, 4 mils is sufficient spacing. This makes interpretation of the post-irradiation data easier since the degradation of the output buffers does not have to be considered. The output buffers should also be provided with separate power pins. This helps prevent switching noise from being coupled into the output.

14.5.1 Application

Delay chains can be used to determine changes in propagation delay as a function of total ionizing dose or neutron fluence. Values of both low-to-high and high-to-low delay should be determined as a function of bias condition during irradiation. If the delay chain is composed of multiple input gates rather than inverters, the bias condition on all inputs should be carefully considered to achieve worst-case performance. For example, in a CMOS NOR gate, the unused inputs should probably be biased to a high state during irradiation to ensure maximum hole trapping in the N-channel device.

Frequency-dependent propagation delays have been observed in some insulated substrate technologies with floating bodies. The

increase in propagation delay with frequency becomes more pronounced after irradiation. Measurements on delay chains for such technologies should cover the frequency range between 10 kHz and 10 MHz.

14.6 Key Subcircuit Functions

14.6.1 Purpose

Designs of complex microcircuits are typically partitioned into a number of key circuit functions. An understanding of the radiation performance of these functions may be crucial to the evaluation of their design and their interaction with other subcircuits.

14.6.2 Description

Naturally, the specific function to be included on a test chip will be determined by the types of microcircuit designs which the test chip results will support. For example, a test chip intended to support an analog process might include subcircuits for comparators, sample and hold units, voltage references, etc. A test chip to support memory designs might include I/O buffers, decode circuits, a variety of random access memory (RAM) cells, different sense amplifier designs, etc.

14.6.3 Special Design Considerations

The test chip designer should give special consideration to subcircuit loading, provisions for power, and pad placement. If the output of the subcircuit cannot directly drive an off-chip load, provisions must be made for output buffers. If area limitations are severe, the outputs of several subcircuits may be multiplexed to a single set of output buffers. However, the post-irradiation performance of the multiplexer should be carefully considered to ensure that the subcircuit performance is not compromised by the monitoring scheme [18–21].

Usually, subcircuits can share a common power bus. However, if the circuits are sensitive to switching noise, individual power busses should be provided. Special attention should be given to the number and placement of topside contacts to the substrate. They should be characteristic of those incorporated in actual microcircuit designs.

Subcircuits are usually packaged for testing in radiation environments. Therefore, pads should be arranged to facilitate bonding. During the test chip design, consideration should be given to the type of package that will be used for radiation testing. Subcircuits should be placed to make efficient use of the number of pins available in the package. If there is a desire to correlate subcircuit performance to process variables or transistor characteristics, suitable test structures should be included on the subcircuit section. The test structures may not require output pads since they can be measured through probe pads. However, provisions for biasing from a bondable pad may be required.

14.6.4 Applications

Special subcircuits are often used to evaluate alternative designs or design rules when analytical tools are inadequate for making a selection. They are also useful in verifying the predicted performance of a selected design.

14.7 Standard Internal Gate Design

14.7.1 Purpose

Standard internal gate designs are used to evaluate changes in transfer characteristics and noise margins as a function of radiation and bias condition.

14.7.2 Description

The standard internal gate design is particularly useful in test chips used for

radiation-hardened technologies for gate arrays or standard cells. Multiple input gates up to the limit permitted by the electrical design rules of the technology should be included. If these devices have unbuffered outputs, they should be used only for monitoring leakage, changes in the output level, noise margin, and transfer function.

14.7.3 Special Design Considerations

The design should provide for variations in bias on multiple input gates. This usually means a separate output pad for at least two inputs. If a worst-case bias condition can be identified, some inputs may be tied to the power supply or ground.

14.7.4 Applications

In standard cell or gate array technologies, the results of measurements on internal gate may become part of the design specifications and used to set electrical design rules for maximum fanout.

14.8 Shift Registers or Counters

14.8.1 Purpose

Shift registers or counters are used to determine maximum post-irradiation clock frequencies, radiation-induced-state change thresholds, and single-event-upset characteristics of sequential devices other than memories.

14.8.2 Description

Shift registers and counters are series connections of flip flops with appropriate feedback in the case of counters. Counters are particularly easy to test in a radiation environment since they require only one signal input, and their correct output is known from the number of clock pulses.

14.8.3 Special Design Considerations

Outputs of the shift register or counter should be buffered.

14.8.4 Applications

Shift registers should be tested to determine both maximum clock frequencies and the setup and hold times required between data and clock. Counters and shift registers should be tested for post-irradiation minimum pulse widths on clock, reset, and set terminals.

14.9 RAM Section

14.9.1 Purpose

Sections of a RAM which may be much smaller (e.g., 512 bits) than a full semiconductor memory can be very useful in evaluating dose rate upset, single event upset, and post-irradiation performance. Different designs for RAM cells can be used in memory sections which share I/O, decode, sense amplifiers, and output multiplexers with other sections. Design concepts and performance can be evaluated without building a full-scale memory.

14.9.2 Description

Due to the high degree of interaction among the subcircuits in a RAM design, it is difficult to evaluate the radiation performance of the entire microcircuit from measurements on individual subcircuits. A RAM section contains all the elements of a full-sized memory but with a smaller array of memory cells. The RAM section size should be consistent with the partitioning expected in the full RAM design. Naturally, portions of the decode, output multiplexing, and other peripheral circuits should be sized to the address requirements of the RAM section. Dummy loads may be required on some nodes to simulate the effects of additional elements in a full RAM design.

14.9.3 Special Design Considerations

The response of a RAM section can be used to evaluate the intrinsic dose rate and SEU hardness of the designed RAM cell. However, the dose rate upset threshold of the full RAM may be affected by rail span collapse which is caused by voltage drops along the power supply bus in the full design. The result is that the voltage across a memory cell at the end of a power bus may be much lower than the voltage supplied at the power pins. In order to simulate this effect in a memory section, independent power pads can be supplied for the memory array. Thus, it can be tested at a reduced voltage to determine the relationship between upset and voltage across the cell.

For SEU testing, the dimensions of the memory array must be large enough so that there is a high probability of a strike through the critical node during a reasonable exposure time. Typically, memory arrays of at least 6.4 bits have been sufficient to make efficient use of beam time at a heavy ion source.

14.9.4 Applications

In addition to their use in evaluating dose rate and SEU thresholds, RAM sections are valuable for determining changes in access time as a function of temperature and radiation dose.

14.10 Input/Output Buffers

14.10.1 Purpose

Input/output buffers are useful for evaluating changes in output drive, output leakage, input leakage, and noise margin to be expected post-irradiation. They can also be used to determine the upset threshold output.

14.10.2 Description

Most microcircuit designs use standard I/O buffers to receive incoming signals and to drive off-chip loads. These macrocells may have characteristics which are much different from those of internal logic cells. For example, CMOS buffers designed to receive TTL inputs or drive TTL loads are designed differently from simple CMOS inverters. These macrocells may be responsible for a large portion of the post-irradiation leakage current.

14.10.3 Special Design Considerations

I/O buffer macrocells are typically designed with individual power pads so that their power consumption can be monitored.

14.10.4 Applications

If chip area is a problem, I/O buffers may have multiplexed inputs to provide chip buffering for internal logic cells.

14.11 Input Protection Circuits

14.11.1 Purpose

Input protection networks are used to suppress electrostatic discharge spikes and other electrical overstress waveforms arising from electromagnetic pulse (EMP), internal electromagnetic pulse (IEMP), and system-generated electromagnetic pulse (SGEMP). Circuits are typically designed to shunt the overstress energy to either the power supply or ground.

14.11.2 Description

The design of the input protection network depends on the devices available in the technology. In general, the devices require a fast switching response to clamp the

overstress voltage before it exceeds the dielectric strength of gate insulators. The protection network must be capable of handling the overstress energy without catastrophic failure.

14.11.3 Special Design Considerations

Input protection networks should be included on all input buffers for macrocells. This permits the packaged devices to be handled without electrostatic discharge damage if normal precautions are taken. Individual test structures such as MOS transistors should not have input protection networks on their terminals. The leakage from the input protection network may mask the subthreshold performance of the transistor. Test chip transistors must be handled with extraordinary caution because of their susceptibility to electrostatic discharge damage.

14.11.4 Applications

Input protection networks used in radiation-hardened microcircuits may have more stringent requirements than those used in c mercially equivalent functions. The energy content in EMP, SGEMP, and IEMP waveforms may be considerably higher than typical electrostatic discharge (ESD) transients. Therefore, design precautions should be taken to ensure uniform current flow during operation of the protection network. Routing of metallization and dimensions of metallization runs should be adequate to handle anticipated currents without current crowding or excessive power dissipation in the conductors.

14.12 Minimum Gate into A Latch

14.12.1 Purpose

The dose rate response of an internal logic gate is difficult to measure directly because the monitoring circuitry excessively loads the gate and affects its radiation performance. By driving a latch with the gate, the upset threshold can be determined as the dose rate at which the transient response of the gate is sufficient to change the state of the latch.

14.12.2 Description

Usually this test structure consists of two latches. Each has provisions for external reset. One latch has its input tied to a reference voltage; another is driven by an internal logic gate. Both latches are monitored during dose rate testing to determine if the upset threshold of the latch driven with the gate output is degraded. An upset at a lower dose rate indicates that the transient response of the gate is sufficient to cause a state change in the latch.

14.12.3 Special Design Considerations

If the transient response of the internal logic gate must be known with greater precision, a comparator with an external voltage reference may be included between the gate and latch. This assumes that the technology will support the design of a comparator. If the dose-rate-induced state change threshold for the latch is close to the transient upset threshold of the gate, a hardened latch may have to be designed in order to differentiate between the two effects.

14.12.4 Applications

If output pads are limited, the latch outputs can be applied to a gate and only the gate output must be monitored externally. The output gate could be an I/O buffer as described previously.

14.13 Large Combinational Macrocell

14.13.1 Purpose

Large combinational macrocells such as arithmetic logic units, multipliers, etc, can be used to monitor transient upset, post-irradiation propagation delay degradation, and high-dose-rate burnout effects [123–124].

14.13.2 Description

Combinational macrocells such as arithmetic logic units are often building blocks for large microcircuit functions. If they are available from a design library, they can be useful additions to a test chip as examples of complex metallization runs and realistic propagation delay paths. If latches are added to their outputs, they can be useful for monitoring transient upsets propagating through the logic as a result of dose rate or single event effects.

14.13.3 Special Design Considerations

The large cell should have full design rule checks performed.

14.13.4 Applications

Combinational macrocells can be useful in evaluating predictions made for propagation delay changes post-irradiation. Care should be taken to ensure bias conditions during irradiation are consistent with those used in the analysis.

LITERATURE CITED

1. Martin G. Buehler, "Microelectronic Test Patterns: An Overview," NBS Special Publication 400-6 (August 1974).

2. M. A. Mitchell, et al., "Electrical Test Structures for Characterization and Control of Microelectronics Processing," *Proc. Microelectronics Measurement Technology Seminar* (March 1981), p VI-1-VI-29.

3. M. G. Buehler and L. W. Linholm, "Role of Test Chips in Coordinating Logic and Circuit Design and Layout Aids for VLSI," ***Solid State Technol.***, Vol. 24 (September 1981), p 68-74.

4. W. Lukaszek et al., "Test Chip Design for Automated Diagnosis of CMOS Yield Problems," SRC Report (May 1989).

5. Ross A. Kohler, "QML Philosophy and SEU Hardness Assurance: A Test Case," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

6. Tom Adamski, "Honeywell's Approach to QML Using Test Structures," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

7. Hollis Pence, "Hardness Assurance Using Offline Statistical Process Control," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

8. F. W. Sexton, et al., "Test Structures for a QML Approach to Radiation Hardness Assurance," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

9. M. G. Buehler, IEEE VLSI Workshop on Test Structures, (February 17-18, 1986).

10. *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988).

11. *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 2 (March 1989).

12. *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 3 (March 1990).

13. Harvey A. Eisen, Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance, HDL-SR-90-7 (26 April 1990).

14. Harvey A. Eisen, Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance, HDL-SR-88-4 (7 April 1988).

15. Harvey A. Eisen, Workshop on Test Structures for Radiation Hardening and Hardness Assurance, DNA/Aerospace Corporation (19 February 1986).

16. M. G. Buehler, "Comprehensive Test Patterns with Modular Test Structures: The 2 by N Probe Pad Array Approach," *Solid State Technol.*, Col. 22, no. 10 (October 1979), pp. 89-94.

17. M. G. Buehler, et al., "Proposed End-of-Fabrication Parametric Test Structures for the CMOS Process Monitor," JPL D-4520 (June 1987).

18. A. Nishimura, "Multiplexed Test Structures: A Novel VLSI Technology Development Tool," IEEE VLSI Workshop on Test Structures (February 17-18, 1986), p. 336.

19. A. J. Walton, et al., "A Novel Approach for Reducing the Area Occupied by Contact Pads on Process Control Chips," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 3 (March 1990), p. 75.

20. K. L. M. van der Klauw, et al., "Self Multiplexing Force-Sense Test Structures for MOS IC Application," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 3, (March 1990), p. 81.

21. H. Sayah, and M. G. Buehler, "Linewidth and Step Resistance Distribution Measurements Using an Addressable Array," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 3 (March 1990), p. 87.

22. R. Allen and M. Buehler, "Design Considerations for Spaceborne CMOS Test Chip," Workshop on Test Structures for Radiation Hardening and Hardness Assurance, DNA/Aerospace Corp. (19 February 1986).

23. D. Alexander, J. Salzman, et al., "Radiation Effects Test Structures on the TI R2D3 Test Bar," DNA/Aerospace Corp. Workshop on Test Structures for Radiation Hardening and Hardness Assurance (19 February 1986).

24. K. Wilson, "Evaluating IC Technologies for Space Applications–The G[illegible] Test Chip," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (7 April 1988).

25. M. G. Buehler, et al., "Test Structures for the Space Electronics Monitor (SEMAC)," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (7 April 1988).

26. M. A. Mitchell, "Radiation Hard 1.25 micron CMOS Technology Assurance Using the YCRAT Test Chip," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance, (7 April 1988).

27. J. Silver, et al., "Features of the UTMC HX17 SOI Parametric Test Chip," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

28. Y. Sacham-Diamand, et al., "The Advanced-Berkeley CMOS (AB-MOS) Test Chip," IEEE VLSI Workshop on Test Structures (February 17-18, 1986), p. 356.

29. M. Steger, et al., "VLSI Process and Device Control by Modular Systems of Combined Test Structures," IEEE VLSI Workshop on Test Structures (February 17-18, 1986), p. 400.

30. M. G. Buehler, et al., "CMOS Process Monitor," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988), p. 164.

31. C. Alcorn, et al., "Kerf Structures Designed for Process and Device Characterization," *Solid State Technol.*, Vol. 28 (May 1985), pp. 229-235.

32. W. E. Ham, "Semiconductor Measurement Technology: A Comprehensive Test Pattern and Approach for Characterizing SOS Technology," NBS Special Publication 400-56 (1979).

33. D. S. Gerber, et al., "TA682 Test Chip Layout Documentation", Sandia Report SAND85-2282 (March 1986).

34. T. J. Russell, "Description of a CMOS Test Chip, NBS-39," NBSIR 83-2683 (April 1983).

35. J. S. Suehle, et al., "Evaluation of a CMOS/SOS Process Using Process Validation Wafers," NBSIR 82-2514 (June 1982).

36. K. P. Roenker, and L. W. Linholm, "An NMOS Test Chip for a Course in Semiconductor Parameter Measurements," NBSIR 84-2822 (April 1984).

37. M. G. Buehler, and L. W. Linholm, "Toward a Standard Test Chip Methodology for Reliable, Custom Integrated Circuits," *Proceedings of the Custom Integrated Circuits Conference* (May 1981), p. 142.

38. C. M. Cork, "Off-line Photolithographic Parameter Extraction Using Electrical Test Structures," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 2 (March 1989), p. 7.

39. M. A. Mitchel, et al., "A Crossbridge for Measurement of Gate-Limited Source/Drain Diffusion," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 3 (March 1990), p. 95.

40. M. G. Buehler and W. R. Thurber, "Bridge and van der Pauw Sheet Resistors for Characterizing the Linewidth of Conducting Layers," *J. Electrochem. Soc.*, Vol 125, No. 4 (April 1978), pp. 650-654.

41. M. G. Buehler and W. R. Thurber, "An Experimental Study of Various Cross Sheet Resistor Test Structures," *J. Electrochem. Soc.*, Vol. 125., No. 4 (April 1978), pp. 645-650.

42. M. G. Buehler and C. W. Hershey, "The Split-Crossbridge Resistor for Measuring the Sheet Resistance, Linewidth, and Line Spacing of Conducting Layers," *IEEE Trans. Electron Devices*, Vol. ED-33, No. 10 (October 1986), pp. 1572-1579.

43. G. P. Carver, et al., "Design Considerations for the Crossbridge Sheet Resistor," NBSIR 82-2548 (July 1982).

44. H. R. Sayah and M. G. Buehler, "Comb/Serpentine/Cross-Bridge Test Structure for Fabrication Process Evaluation," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988).

45. D. Yen, et al., "A Cross-bridge Test Structure for Evaluating the Linewidth Uniformity of an Integrated Circuit Lithography System," *J. Electrochem. Soc.*, Vol. 129, No. 10 (October 1982), pp. 2313-2318.

46. W. Muray Bullis, "Semiconductor Measurement Technology–Quarterly Report," October 1, 1973, to March 31, 1974. NBS Special Publication 400-4 (November 1974), pp. 46-48.

47. L. S. van der Pauw, "A method of Measuring the Resistivity and Hall Coefficient on Lamella of Arbitrary Shape," Phillips Research Reports, No. 13 (1958), pp. 1-9.

48. Martin G. Buehler, "Microelectronic Test Patterns NBS-3 for Evaluating the Resistivity-Dopant Density Relationship of Silicon," NBS Special Publication 400-22 (June 1976).

49. W. Muray Bullis, "Semiconductor Measurement Technology–Quarterly Report," April 1 to June 30, 1974. NBS Special Publication 400-8 (February 1975), pp. 7-18.

50. A. Mayer and S. Schwartzman, "Preparation of Bevelled Surfaces for Spreading Resistance Probing by Diamond Grinding and Laser Measurement of Bevel Angles," Semiconductor Measurement Technology: Spreading Resistance Symposium, J. R. Ehrstein, ed., NBS Special Publication 400-10 (December 1974), pp. 123-137.

51. B. L. Morris, "Some Device Applications of Spreading Resistance Measurements on Epitaxial Silicon," *J. Electrochem. Soc.*, 121 (1974), pp. 422-426.

52. Harry A. Shaafft, "Semiconductor Measurement Technology–ARPA/NBS Workshop III–Test Patterns for Integrated Circuits," NBS Special Publication 400-15 (January 1976), p. 38.

53. T. Schreyer, et al., "Comparison of Test Structures Used for the Measurement of Low Resistive Metal-Semiconductor Contacts," IEEE VLSI Workshop on Test Structures (February 17-18, 1986), p. 7.

54. W. J. C. Alexander, and A. J. Walton, "Sources of Error in Extracting the Specific Contact Resistance from Kelvin Device Measurements," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988), p. 17.

55. K. W. J. Findlay, et al., "The Effect of Contact Geometry on the Value of Contact Resistivity Extracted from Kelvin Structures," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 2 (March 1989), p. 133.

56. S. J. Proctor and L. W. Linholm, "A Direct Measurement of Interfacial Contact Resistance," *IEEE Elec. Dev. Let.*, Vol. EDL-3, No. 10 (October 1982).

57. S. J. Proctor, et al., "Direct Measurements of Interfacial Contact Resistance," End Contact Resistance, and Interfacial Contact Layer Uniformity," *IEEE Trans. Electron Devices*, Vol. ED-30, No. 11 (November 1983), pp. 1535-1542.

58. G. K. Reeves, et al., "Physical and Electrical Characteristics of Contact Interfaces Using Multilayer Interconnect Test Structures," IEEE VLSI Workshop on Test Structures (February 17-18, 1986), p. 24.

59. H. A. Schafft, and J. Albers, "Thermal Interactions between Electromigration Test Structures," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988), p. 132.

60. C. Caprile, "Contact Electromigration: A Method to Characterize Test Structures for Reliability Parameter Extraction," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 2 (March 1989), p. 115.

61. N. Zamani and Y. S. Lin, "Temperature Control in Wafer Level Testing of Large Multisegment Electromigration Test Structures," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988), p. 138.

62. L. W. Linholm, "The Design, Testing, and Analysis of a Comprehensive Test Pattern for Measuring CMOS/SOS Process Performance," NBS Spec. Publ. 400-66 (August 1981).

63. P. S. Winokur, et al., "Correlating the Radiation Response of MOS Capacitors and Transistors," *IEEE Trans. Nucl. Sci.*, NS-31 (December 1984).

64. K. F. Galloway, et al., "A Simple Model for Separating Interface and Oxide Charge Effects in MOS Device Characteristics," *IEEE Trans. Nucl. Sci.*, Vol. NS-31, No. 6 (December 1984), pp. 1497-1501.

65. J. Teplik, "Experiment Comparison of Leff Measurement Techniques," IEEE VLSI Workshop on Test Structures (February 17-18, 1986), p. 152.

66. D. Wilson, "Delta L Extraction Using Parasitic Bipolar Transistors," IEEE Proceedings on Microelectronic Test Structures, Vol. 1 (February 1988), p. 85.

67. G. Freeman and W. Lukaszek, "Gate Dimension Characterization Using the Inversion Layer," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 2 (March 1989), p. 3.

68. H. P. Tuinhout, "MOSFET Effective Dimensions Determination for VLSI Process Evaluation," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 2 (March 1989), p. 61.

69. E. W. Enlow, et al. "Subthreshold Technique for Fixed and Interface Trapped Charge Separation in Irradiated MOSFETS," DNA-TR-89-157, Defense Nuclear Agency (April 1990).

70. E. W. Enlow, "Standard Test Method for Determining the Mean Interface Trap Density of MOSFETs by Charge Pump," ASTM F-996 (October 1990).

71. M. Gaitan, et al., "Accuracy of the Charge Pumping Technique for Small Geometry MOSFETs," *IEEE Trans. Nucl. Sci.*, Vol. 36, No. 6 (December 1989), p. 1990.

72. T. J. Russell, "Production Compatible Microelectronic Test Structures for the Measurement of Interface State Density and Neutral Trap Density," NBSIR 81-2413 (January 1982).

73. R. A. Allen, et al., "A Direct Method for Measuring the Gate Oxide Capacitances of MOSFETs," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988), p. 45.

74. M. Kuhn, "A Quasi-Static Technique for MOS C-V and Surface State Measurements", *Solid State Electronics*, 13 (1970), pp. 873-885.

75. T. C. Zietlow, et al., "Correlation of Total Dose Damage in Capacitors and Transistors to 1.25 micron Integrated Circuits," *IEEE Trans. Nucl. Sci.*, Vol. NS-34, No. 6 (December 1987), p. 1635.

76. T. S. Russell, et al., "Correlation Between CMOS Transistor and Capacitor Measurements of Interface Trap Spectra," *IEEE Trans. Nucl. Sci.*, Vol. NS-33, No. 6 (December 1986), pp. 1228-1233.

77. C. Kortekaas, "Interconnect Capacitance Characterization for MOS-IC Process and Circuit Design," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988), p. 39.

78. J. Faue, et al., "Gated GrooveFET Structure for Analyzing Total Dose Effects in a Trench Isolation Process," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (7 April 1988).

79. K. Kishi, "Novel Test Structure to Study Location of Breakdown for Trench Capacitor," Proceedings of the International Conference on Microelectronic Test Structures, Vol. 2 (March 1989), p. 245.

80. E. W. Enlow, et al., "Total Dose Induced Hole Trapping in Trench Oxides," *IEEE Trans. Nucl. Sci.*, Vol. 36, No. 6 (December 1989), p. 2415.

81. D. Platteter, Private Communications (September 1985).

82. D. M. Fleetwood and S. S. Tsao, "Test Structures for Total Dose Radiation Testing of SOI MOSFETs," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (7 April 1988).

83. T. W. Houston, et al., "Radiation Hardening Test Structures for CMOS/SOI," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (7 April 1988).

84. W. A. Krull, et al., "The Buried Oxide Capacitor: A Test Structure for the Radiation Characterization of Silicon-On-Insulator," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

85. J. Marshall, et al., "Two CMOS on SIMOX Test Chips, NIST3 and NIST4," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

86. Jay Shrankler and Todd Randazzo, "An SOI Rad Bar for Quick Production Level Hardness Assurance," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

87. E. W. Enlow and D. Alexander, "Photocurrent Modeling of Modern Microcircuit PN Junctions," *IEEE Trans. Nucl. Sci.*, Vol. 35, No. 6 (December 1988), p. 1467.

88. J. Herbert and G. Brucker, "SOS Test Structures for Measurement of Photocurrent Sources and Upset Dose Rates in Memories," DNA/Aerospace Corp. Workshop on Test Structures for Radiation Hardening and Hardness Assurance (19 February 1986).

89. D. G. Mavis, D. R. Alexander and G. L. Dinger, "A Chip-Level Modeling Approach for Rail Span Collapse and Survivability Analysis," *IEEE Trans. Nucl. Sci.*, Vol. 36, No. 6 (December 1989), p. 2239.

90. S. E. Kerns, et al., "Model for CMOS/SOI Single Event Vulnerability," *IEEE Trans. Nucl. Sci.*, Vol. 36, No. 6 (December 1989), p. 2305.

91. Rauchfuss, "Latchup Test Structures: A Hardening Tool and Hardness Assurance Safeguard," DNA/Aerospace Corp. Workshop on Test Structures for Radiation Hardening and Hardness Assurance (19 February 1986).

92. A. H. Johnson, "Test Structures for Radiation-Induced Latchup," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

93. B. L. Hiken and J. Cable, "Test Chip Methodology for Latchup Evaluation in Advanced Semiconductor Technologies," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (7 April 1988).

94. Andre Stolmeijer, "Measuring Latchup," IEEE VLSI Workshop on Test Structures (February 17-18, 1986), p. 326.

95. W. Reczek, et al., "Guidelines for Latchup Characterization Techniques," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988), p. 120.

96. J. Quincke, "Novel Test Structures for the Investigation of the Efficiency of Guard Rings Used for I/O Latchup Prevention," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 3 (March 1990), p. 35.

97. C. Cane, et al., "A New Test Structure to Characterize the Latchup Effect," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 3 (March 1990), p. 47.

98. W. Reczek, et al., "Reliability of Latchup Characterization Procedures," Proceedings of the International Conference on Microelectronic Test Structures, Vol. 3 (March 1990), p. 51.

99. R. R. Troutman, "Latchup in CMOS Technology: The Problem and Its Cure," Kluwer Academic Publishers, Boston (1986).

100. Y. Song, et al., "The Dependence of Latchup Sensitivity on the Layout Features in CMOS Integrated Circuits," *IEEE Trans. Nucl. Sci.*, Vol. NS-33, No. 6 (December 1986), pp. 1493-1498.

101. D. B. Estreich, "Latchup and Radiation Integrated Circuit – LURIC: A Test Chip for CMOS Latchup Investigation," Sandia National Laboratories, SAND78-1540 (November 1978).

102. T. Cavioni, et al., "Latchup Characterization in Standard and Twin Tub Test Structures by Electrical Measurements, 2-D Simulations, and IR Microscopy," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 3 (March 1990), p. 41.

103. A. Ochoa, et al., "Snap-back: A Stable Regenerative Breakdown Mode of MOS Devices," *IEEE Trans. Nucl. Sci.*, Vol. NS-30, No. 6 (December 1983), p. 4127.

104. D. Berndt and R. Belt, "Honeywell Single-Event Upset Test Chip–'Advanced Digital Bipolar II (ADB-111/SOI) VHSIC1 Technology," 87SRC15 (30 June 1987).

105. J. Fertsch, et al., "Area-Periphery Partitioning for Currents in Self-Aligned Bipolar Transistors," Proceedings of the International Conference on Microelectronic Test Structures, Vol. 2 (March 1989), p. 79.

106. Gary Lum, "Test Structures to Understand Dose Rate Upset," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

107. R. L. Pease and R. M. Turfler, "Total Dose Effects in Recessed Oxide Digital Bipolar Microcircuits," *IEEE Trans. Nucl. Sci.*, Vol. NS-30, No. 6 (December 1983), p. 4216.

108. J. G. Bossun, et al., "The Effects of Ionizing Radiation on Diffused Resistors," *IEEE Trans. Nucl. Sci.*, Nol. NS-21, No. 6 (December 1974), p. 315.

109. B. Ahlport, et al., "Use of a Pinch Resistor for Neutron Hardness Assurance Screening of Bipolar Integrated Circuits," *IEEE Trans. Nucl. Sci.*, Vol. NS-28, No. 6 (December 1981), p. 4318.

110. R. M. Greene, "The Role of Test Structures and Modeling in Circuit Radiation Hardening: A Chip Designer's Perspective," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (7 April 1988).

111. Y. S. Lin, et al., "Modeling Radiation-Induced Timing Delays Measured from the Timing Sampler Test Structure," Workshop on Test Structures for Semiconductor Device Radiation Hardening and Hardness Assurance (26 April 1990).

112. D. J. Radack and L. W. Linholm, "The Application of Microelectronic Test Structures for Propagation Delay Measurements," IEEE VLSI Workshop on Test Structures (February 17-18, 1986), p. 190.

113. B. R. Blaes, "CMOS Timing Sampler Array for Measuring Circuit Delays," IEEE VLSI Workshop on Test Structures (February 17-18, 1986), p. 208.

114. J. Winerl, et al., "Ring Oscillator Structure for Realistic Dynamic Stress of MOSFETs and Interconnects," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988), p. 56.

115. K. Lippe, et al., "A Programmable-Load CMOS Ring Oscillator/Inverter Chain for Propagation Delay Measurements," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 2 (March 1989), p. 225.

116. B. R. Blaes and Buehler, M. G., "Inverter Propagation Delay Measurements Using a Timing Sampler Circuit," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 2 (March 1989), p. 227.

117. S. G. dos Santos, et al., "An Experimental Measurement Technique of Interconnection RC Delay for Integrated Circuits Using the Step Voltage Response," *Proceedings of the International Conference on Microelectronic Test Structures*, Vol. 2 (March 1989), p. 233.

118. N. Nasaki, "Higher Harmonic Generation in CMOS/SOS Ring Oscillators," *IEEE Trans. Electron Devices*, Vol. ED-29 (February 1982), p. 280-283.

119. D. J. Radack and L. W. Linholm, "The Application of Microelectronic Test Structures for Propagation Delay Measurements," IEEE Workshop on Test Structures (February 1986), pp. 190-209.

120. B. R. Blaes, M. G. Buehler, and Y. S. Lin, "Propagation Delay Measurements from a Timing Sampler Intended for Use in Space," *IEEE Trans. Nucl. Sci.*, NS-34, No. 6 (December 1987), pp. 1470-1473.

121. S. Long, "Test Structures for Propagation Delay Measurements on High Speed Integrated Circuits," *IEEE Trans. Electron Devices*, ED-31 (August 1984), pp. 76-79.

122. J. M. Cassard, "A Sensitivity Analysis of SPICE Parameters Using an Eleven-Stage Ring Oscillator," *IEEE Trans. Electron Devices*, Vol ED-31, No. 2 (February 1984), pp. 264-269.

123. D. M. Ne berry and B. E. Peters, "Total Dose Radiation Response of Test Structures and VLSI Logic Devices: An Analytical and Experimental Correlation," *IEEE Proceedings on Microelectronic Test Structures*, Vol. 1 (February 1988), p. 61.

124. F. W. Sexton and J. R. Schwank, "Correlation of Radiation Effects in Transistors and Integrated Circuits," *IEEE Trans. Nucl. Sci.*, Vol. NS-33, No. 6 (December 1986), pp. 3975-3981.

Distribution

Administrator
Defense Technical Information Center
Attn DTIC-FDAB (2 copies)
Cameron Station, Building 5
Alexandria, VA 22304-6156

Commander
Defense Electronic Supply Center
Attn DESC-E
1507 Wilmington Pile
Dayton, OH 45444-5270

Director
Defense Nuclear Agency
Attn RAEE (TREE)
Attn TITL (2 copies)
6801 Telegraph Road
Alexandria, VA 22310-3398

Commander
Information Systems Command
Attn STEWS-NE, J. Meason
White Sands Missile Range, NM 88002-5180

Commander
US Army Nuclear & Chemical Agency
Attn MONA-NU, Adam Renner
7500 Backlick Road, Bldg 2073
Springfield, VA 22150-3198

Chief
US Army Research Office
Attn R. Griffith
PO Box 12211
Triangle Park, NC 27709-2211

Deputy Commander
US Army Strategic Defense Cmd
Attn CSSD-SD-A
PO Box 1500
Huntsville, AL 35807

Superintendent
Naval Postgraduate School
Attn Code 1424, Library
Monterey, CA 93943-5000

Commanding Officer
Naval Research Laboratory
Attn Code 4613, B. Campbell
Attn Code 4682, D. B. Brown
Attn Code 6816, H. Hughes
Attn Code 6816, R. Hevey
Attn Code 6816, W. Jenkins
Washington, DC 20375-5000

Commander
Naval Surface Warfare Center
Attn Code H23, R. Smith
10901 New Hampshire Ave
Silver Spring, MD 20903-5000

Commanding Officer
Naval Weapons Support Center
Attn Code 6054, D. Platteter
Crane, IN 47522

Air University Library
Attn AUL-LSE
Bldg 1405, Room 160
Maxwell AFB, AL 36112-5564

Phillips Laboratory
Attn STEE, CAPT J. Lyke
Attn STEE, CAPT M. MacDonald
Attn STEE, S. Simpson
Kirtland AFB, NM 87117-6008

Rome Air Development Center, AFSC
Attn RBR, C. Messenger
Griffiss AFB, NY 13441-5700

Distribution (cont'd)

Commander
Rome Laboratories
Attn STER
Hanscom AFB, MA 01731-5000

Commander
Wright Research & Development Center
Attn AFWAL/ELE
Attn WRDC/MTE
Wright-Patterson AFB, OH 45433-6543

University of California
Lawrence Livermore National Lab
Attn L-156, J. Yee
Attn L-84. G. Pomykal
Attn W. Orvis
PO Box 808
Livermore, CA 94550-0622

Los Alamos National Laboratory
Attn MS B230, E. Leonard
PO Box 1663
Los Alamos, NM 87545

Sandia National Laboratories
Attn Div 1332, P. Winokur
Attn Div 2160, D. C. Gwyn
Attn Div 2146, T. A. Dellin
Attn Div 9342, T. F. Wrobel
PO Box 5800
Albuquerque, NM 87185

NASA, Goddard Space Flight Center
Attn Code 311, J. Adolphson
Attn Code 313, V. Danchenko
Attn Code 724, O. M. Jhabvala
Greenbelt, MD 20771

National Institute of Standards &
Technology
Attn P. Roitman
Gaithersburg, MD 20899

Clemson University,
Physics & Astronomy Dept
Attn P. J. McNaulty
Clemson, SC 29634-1911

Johns Hopkins University
Applied Physics Lab
Attn R. Maurer
Johns Hopkins Road
Laurel, MD 20723-6099

Maryland University
Department of Electrical Engineering
Attn H. C. Lin
College Park, MD 20742

University of Arizona
Electrical & Computer Engr Dept
Attn K. Galloway
Tucson, AZ 85721

Vanderbilt University
Electrical Engr Dept
Attn S. Kerns
PO Box 1824, Sta. B
Nashville, TN 37235

Yale University
Dept of Elec Engr
Attn T. P. Ma
319 Becton Center, 15 Prospect St
New Haven, CT 06520-2157

Advanced Research & Applications Corp
Attn E. King
Attn R. Armistead
425 Lakeside Drive
Sunnyvale, CA 94086

Aerospace Corp
Attn A. Amram
Attn I. Garfunkel

Distribution (cont'd)

Aerospace Corp (cont'd)
Attn K. G. Holden
Attn M2-259, W. A. Kolasinski
Attn M4/949, L. Mendoza
Attn MS M4/934, N. Sramek
Attn P. Buchman
PO Box 92957
Los Angeles, CA 90009-2957

Aerospace Design Concepts
Attn R. Greene
10 Stevens Lane
Vincentown, NJ 08088

BDM International Inc
Attn D. Wunsch
PO Box 9274
Albuquerque, NM 87119

Boeing Co
Attn 7J56, A. Johnston
PO Box 3707
Seattle, WA 98124-2207

Booz-Allen & Hamilton
Attn L. Albright
4330 East West Highway
Bethesda, MD 20814

California Institute of Technology
Jet Propulsion Lab
Attn 300/329, M. Buehler
Attn MS-303/220, C. Barnes
4800 Oak Grove Drive
Pasadena, CA 91109

Calspan Corp, Advanced Technology
Division, Franklin Research Division
Attn R. Thompson
2600 Monroe Boulevard
Morristown, PA 19403

Carlan Associates
Attn A. Carlan
4951 Rock Valley Rd
Rancho Palos Verdes, CA 90274

Charles Stark Draper Lab, Inc
Attn MS 11, N. Tibbetts
555 Technology Square
Cambridge, MA 02139

Computer Sciences Corp
Attn A. Schiff
2100 Air Park Road, SE, Suite 200
Albuquerque, NM 87106

David Sarnoff Research Center, Inc
Attn CN 5300, G. Cullen
Attn CN 5300, R. Smeltzer
Attn CN 5300, Security
Princeton, NJ 08543-5300

Electronic Industries Association
Attn J. Kinn
2000 Pennsylvania Avenue, NW
10th Floor
Washington, DC 20006

Full Circle Research
Attn J. Spratt
PO Box 4010
San Marcos, CA 92069

General Electric, Astro-Space Division
Attn G. Brucker
PO Box 800
Princeton, NJ 08543-0800

Distribution (cont'd)

General Electric Co, Aerospace
Electronic Systems Department
Attn MD 289, D. Nerad
French Road
Utica, NY 13503

General Electric Co
Defense Systems Department
Attn B. Flaherty, Rm 2282
100 Plastics Avenue
Pittsfield, MA 01201-3698

General Electric Co, Space Division
Valley Forge Space Center
Attn M 1211, J. Andrews
PO Box 8555
Philadelphia, PA 19101

General Electric, Solid State Div
Attn C. F. Wheatley, Jr.
125 Crestwood Rd
Mountaintop, PAS 18707-2189

General Research Corp
Attn A. Hunt
PO Box 6770
Santa Barbara, CA 93160-6770

H. M. Weil Consultant, Inc
Attn H. Weil
9 East Sunrise Drive
Santa Fe, NM 87501

Harris Corp
Harris Semiconductor Sector
Attn M/S 54-102, J. C. Lee
Attn MS 54-102, B. R. Doyle
Attn MS 62B-916, R. S. Brandt
Attn N. Van Vonno
Attn MS 101/4825, W. Abare
PO Box 37
Melbourne, FL 32392

Honeywell, Inc
Solid State Electronics Center
Attn D. Fett
Attn M/S 4C25, R. Julkowski
Attn QA, G. Kirchner
Attn R. Maciolek
12001 State Highway 55
Plymouth, MN 55441

Honeywell, Inc, Space Systems Group
Space & Strategic Systems OPR
Attn MS 725-5
13350 U.S. Highway 19 North
Clearwater, FL 34624-7290

Hughes Aircraft Co
Ground Systems Group
Attn Systems Tech Dept, W. Schenet
PO Box 3310
Fullerton, CA 92534-3310

Hughes Aircraft Company
Space & Communication Group
Attn S4/X301, E. Kubo
Attn S4/S304, L. Darda
PO Box 92919
Los Angeles, CA 90009

Hughes Microelectronics
Attn MS 116, K. Aubuchon
6155 El Camino Real
Carlsbad, CA 92008

IBM Corp, Federal Systems Division
Attn C. Alcorn
Attn N. Haddad
9500 Godwin Drive
Manassas, VA 22110-41988

Distribution (cont'd)

IBM Corp, Thomas J. Watson Rsch Ctr
Attn J. Ziegler
PO Box 218
Yorktown Heights, NY 10598-0218

IIT Research Institute
Attn I. Mindel
10 W. 35th Street
Chicago, IL 60616

Integrated Devices Technology
Attn QA, C. Crane
3236 Scott Blvd
Santa Clara, CA 95051

Intel Corp
Attn SP1-57, M. Orr
5000 W. Chandler Blvd
Chandler, AZ 85224

JAYCOR
Attn S. C. Rogers
2951 28th St, #3075
Santa Monica, CA 90405-2976

Kaman Sciences Corporation
Attn Library, B. Kinslow
PO Box 7463
Colorado Springs, CO 80933-7463

Kaman Sciences Corporation
Washington Operations Division
Attn DASIAC
2560 Hungtington Ave, Suite 200
Alexandria, VA 22303

Kaman Sciences Corporation
Santa Barbara Operations
Attn DASIAC
PO Box 1479
Santa Barbara, CA 93102-1479

Kearfott Guidance & Navigation Corp
Attn MC 12B74, J. Brinkman
1150 McBride Avenue
Little Falls, NJ 07424

Litton Systems, Inc
Guidance & Control Systems Division
Attn F. Motter
5500 Canoga Avenue
Woodland Hills, CA 91367

Lockheed Missiles & Space Co., Inc
Attn 610-02, P. Bene, Bldg 579
Attn Dept 5960, D. Meshel
Attn Dept 81-63, J. Cayot
PO Box 3504
Sunnyvale, CA 94088-3504

Lockheed Missiles & Space Co., Inc
Attn Technical Information Center
3251 Hanover Street
Palo Alto, CA 94304-1187

Lockheed Sanders, Inc
Attn MS NCA1-6263, B. G. Carrigg
PO Box 2057
Nashua, NJ 03061

Logicon R & D Associates
Attn D. Carlson
2100 Washington Blvd
Arlington, VA 22204-5706

Loral Aeronutronic
Attn Technical Information Services
Attn Technical Library
Ford Road & Jamboree
Newport Beach, CA 92658-9983

Distribution (cont'd)

LSI Logic
Attn Mil/Aero, W. Schneider
48660 Kato Rd
Fremont, CA 94538

LTV Aerospace & Defense Company
Aircraft Division
Attn EM-08, Library
PO Box 655907
Dallas, TX 75265-5907

Martin Marietta Corp, Missile Systems
Attn J. Tanke
TIC/MP-30
PO Box 555837-MP11
Orlando, FL 32885-5837

Martin Marietta Corporation
Attn Research Laboratory
PO Box 179
Denver, CO 80201

Martin Marietta Laboratories
Attn S. Buchner
1450 S Rolling Road
Baltimore, MD 21227-3898

McDonnell Douglas Corporation
HOF Region
Attn Dept 4100 MC 2871240, R. L. Kloster
PO Box 516
St Louis, MD 63166

McDonnell Douglas Corporation
Attn P. Albrecht
5301 Bolsa Avenue
Huntington Beach, CA 92647-2048

G. M. Messenger, Consulting Engineer
Attn G. Messenger
3111 Bel Air Drive, 7-F
Las Vegas, NV 89109-1558

Mission Research Corporation
Attn D. Alexander
Attn E. Enlow
Attn R. Pease
1720 Randolph Rd SE
Albuquerque, NM 87106

Mission Research Corporation
Attn J. Raymond
5434 Ruffin Road
San Diego, CA 92123

Mitre Corporation
Attn M. Fitzgerald
Burlington Road
Bedford, MA 01730

Myers & Associates
Attn D. Myers
1508 Arena Pl., SE
Albuquerque, NM 87123

National Semiconductor
Attn MS 10-50, M. Maher
333 Western Ave
Portland, ME 04106

National Semiconductor Corp
Attn F. C. Jones
PO Box 58090
Santa Clara, CA 95052-8090

Nichols Research Corporation
Attn H. Hardt
4040 South Memorial Parkway
Huntsville, AL 35802

Norden Systems, Inc
Attn Technical Library
PO Box 5300
Norwalk, CT 06856

Distribution (cont'd)

Northrop Research & Technology Ctr
Attn A. Bahraman
One Research Park
Palos Verdes Peninsula, CA 90274

Pacific-Sierra Research Corp
Attn H. Brode
12340 Santa Monica Blvd
Los Angeles, Ca 90025-2587

Physitron, Inc
Attn M. Christopher
3325 Triana Blvd, Suite A
Huntsville, AL 35805

Physitron, Inc
Attn M. Rose
16885 Via Del Campo Court, Suite 200
San Diego, CA 92127

Rand Corp
Attn B. Bennett
2100 M Street, NW
Washington, DC 20037-1270

Rand Corp
Attn C. Crain
PO Box 2138
Santa Monica, CA 90406-2138

Raytheon Co
Attn 1J8, S. Bernacki
Attn MS 1-2-1735, H. Flescher
528 Boston Post Road
Sudbury, MA 01776

Research Triangle Institute
Attn M. Simons
PO Box 12194
Research Triangle Park, NC 27709

Rockwell International Corp
Attn V. De Martino
PO Box 3105
Anaheim, CA 92803-3105

Rockwell Microelectronics
Attn R. Kjar
4311 Jamboree Rd
Newport Beach, CA 92658-8902

S-Cubed, A Division of Maxwell Labs, Inc
Attn J. M. Wilkenfeld
PO Box 1620
La Jolla, CA 92038-1620

Science Applications Intl Corp
Attn P. Zielie
6 Fortune Drive-Third Floor
Billerica, MA 01821

Science Applications Intl Corp
Attn W. Chadsey
PO Box 1303
McLean, VA 22102-1303

Science Applications Intl Corp
Attn D. Millward
Attn MS-43, D. Long
10260 Campus Point Drive
San Diego, CA 92121

Science Applications Intl Corp
Space & Command Systems Group
Attn J. Retzler
26679 W Agoura Road, Suite 200
Calabasas, CA 91302

Distribution (cont'd)

Sundstrand Corp
Attn C. White
PO Box 7003, 4751 Harrison Ave
Rockford, IL 61125-7003

System Planning Corp
Attn B. Stupski
1500 Wilson Blvd
Arlington, VA 22209

Safety Systems Division
Systron-Donner, A Thorn EMI Company
Attn Security Officer,
Mail Code PER/970-1388
2731 Systron Drive
Concord, CA 94518

Technology Development Associates
Attn R. V. Benedict
992 Old Eagle School Road, Suite 910
Wayne, PA 19087

Teledyne Brown Engineering
Attn MS 19, G. R. Ezell
Attn MS-50, L. T. Smith
PO Box 070007
Huntsville, AL 35807-7007

Texas Instruments, Inc
Attn G. Pollack
Attn L. Hite
Attn MS 3143, T. Cheek
Attn MS 3145, J. Salzman
Attn MS 961, E. Jeffrey
Attn T. Houston
PO Box 655474
Dallas, Tx 75265

TRW Space & Defense
Attn MS 84/1002, P. Guilfoyle
One Space Park
Redondo Beach, CA 90278-1071

TRW Space & Defense Sector
Ballistic Missiles Division
Attn D. B. Gibson
PO Box 1310
San Bernardino, CA 92402

TRW Space & Defense Sector
Space & Te Group Ogden Eng Operations
Attn HL Dept/Library
PO Box 804
Clearfield, UT 84015-0804

Unisys Corporation-Defense Systems
Shipboard & Ground Systems
Attn P. Marroffino
Marcus Avenue
Great Neck, NY 11020

UTMC Microelectronics Center
Attn G. Reinsma
Attn S. Tyson
1575 Garden of the Gods Rd
Colorado Springs, CO 80907-3486

Visidyne Inc
10 Corporate place
Attn C. H. Humphrey
South Bedford Street
Burlington, MA 01803

Westinghouse Elec Sys Gp
Attn M. Fitzpatrick
Attn MS 3AT2, D. Adams
PO Box 1521
Baltimore, MD 21203

Harry Diamond Laboratories
Attn SLCHD-NW-RP, Chief
Attn SLCHD-NW-TS, Chief (10 copies)