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Superconducting

Analog to Digital Converters: Final Report

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Edited by Joel M. Schoen

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MITRE

PREFACE

The Final Report for Project 91080 is presented as a collection of technical reports by participants on the project. The first report is a summary of the project results and an introduction to the reports that follow.

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REPORT

Technical Report 1

SUPERCONDUCTING ANALOG-TO-DIGITAL CONVERTER WORK AT MITRE

by

J. M. Schoen

ABSTRACT

MITRE's involvement in superconducting electronics is described. The stimulus for this work was the discovery of superconductivity at temperatures above that of liquid nitrogen suggesting that more economic superconducting electronic systems were feasible. The phenomena associated with superconductivity, Josephson junctions, and superconducting quantum interference devices (SQUIDs) are briefly described. Various techniques to perform analog-to-digital conversion using these phenomena are then reviewed with emphasis on fundamental limitations. Finally, MITRE's work in FY90 and FY91 is introduced.

SECTION 1

INTRODUCTION

During the past three years, MITRE sponsored a research project to investigate the feasibility of using superconducting electronics to improve the performance of analog-to-digital (A/D) converters. This report summarizes the work performed on that project during FY90 and FY91.

SECTION 2

SUPERCONDUCTING ELECTRONICS WORK AT MITRE

This section reviews the activities that led to the development of the project, other work in superconducting, A/D converters, and the overall organization of the report.

The exciting developments in superconducting materials research, which began in 1986, was the initial stimulus for MITRE to begin to investigate potential applications of superconductivity to the Air Force command, control, communications, and intelligence (C^3I) applications. The prospect of superconducting electronics that could operate near room temperature while providing increased speed, lower power consumption, and novel modes of performance, led to a renewed worldwide interest in a field that had become stagnant (at least in the U.S.) for approximately four years. The period of stagnation began in the U.S. in 1983, when IBM abandoned its efforts to build a superconducting computer. Work in other countries, most notably Japan, continued, eventually leading to the perfection of reproducible tunnel junctions made of niobium-aluminum oxide-niobium sandwiches [1,2].

In 1987, MITRE began to assess the applicability of high-temperature superconductors to C^3I applications. MITRE had not been involved in superconducting electronics previously, although some staff members had worked with superconductors prior to joining MITRE. There were several misconceptions as to the general properties of superconductors and the specific characteristics of the newly discovered high-temperature ceramics. A one-day tutorial was held in November 1987 to acquaint MITRE staff members with superconductor properties as applied to both the older, conventional superconductors and the newer, high-temperature superconductors. The tutorial was conducted by Professors T. Orlando and D. Rudman of the Massachusetts Institute of Technology.

Two working groups began to evaluate the impact of superconducting electronics on sensor (especially radar) and communications systems; each group issued a working paper (designated references [3] and [4] , respectively). Several interesting potential applications of

superconducting electronics were identified by the working groups. These include, but are not limited to, high-stability oscillators and clocks, high-gain antennas, low-loss radio-frequency and microwave circuit elements, and increased-capability A/D converters.

The latter application is particularly valuable because the A/D conversion process, which is necessary to exploit fully the digital techniques developed over the past forty years, is a bottleneck to improved system performance. State-of-the-art C^3I electronic systems that employ digital signal and data processing must first convert analog input signals from a sensor or communications system to appropriately sampled digital signals. The Very High Speed Integrated Circuit (VHSIC) program provides circuitry for implementing signal and data processing with clock rates of 100 MHz. The Monolithic Microwave Integrated Circuit (MMIC) program provides analog circuits with operating frequencies of up to 100 GHz. C^3I systems contemplated for deployment in the 1990s may require a dynamic range in excess of 90 dB (15-bit precision) [3]. However, at the present time, A/D conversion with 16-bit precision is limited to 500 Ksamples/sec. Clearly, the speed and quality of present A/D converters limit the performance and capabilities of many C^3I systems.

The limitations imposed on system performance by A/D conversion have been recognized for some time. Efforts to overcome these limitations have concentrated on new architectures (to increase conversion speed) and compensation techniques (to overcome deficiencies in the conversion process caused by higher conversion speeds). MITRE is playing a leading role in developing adaptive compensation methods to improve A/D converter performance [5], and in evaluating state-of-the-art A/D converters [6]. Generally, progress in improving converter performance by new architectures in semiconducting technology and by adaptive compensation has been achieved in an incremental fashion. Fundamental limitations of semiconductor performance will result in a leveling off of this progress.

A small, continuing effort has been exploring A/D conversion using alternative techniques, including superconducting electronics [7] and electro-optics [8]. In 1988, the best projected performance of superconducting A/D converters was 16-bit precision with conversion rates of 10 Megasamples/sec [7] or 6-bit precision with 4 Gigasamples/sec [9]. Electro-optical converters have a projected performance of 4-bits at 2 Gigasamples/sec [8]. This project investigated several

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novel A/D converter architectures that promised improved performance; these architectures are based upon quantum mechanical phenomena associated with superconductivity.

A description of the pertinent properties of superconductors and Josephson junction (JJ) devices will facilitate a discussion of the A/D converter architectures investigated at MITRE.

SECTION 3

SUPERCONDUCTOR AND JOSEPHSON JUNCTION PROPERTIES

THE ORIGIN OF SUPERCONDUCTIVITY

The phenomenon of superconductivity is characterized by two distinct effects: (1) the absence of DC resistivity (Onnes, 1911), and (2) the expulsion of magnetic fields (Meissner and Ochsenfeld, 1933). Both effects must be present for a material to be classified as a superconductor.

An explanation of the theoretical foundations of superconductivity took a number of years to develop. The difficulty was in identifying an attractive force between electrons that can overcome the Coulombic repulsion, which normally accounts for the properties of matter in the solid, liquid, gaseous, and plasma states. Until 1957, the most successful explanation of superconductive properties had a phenomenological basis and modeled a superconductor as consisting of two interpenetrating fluids: a superconducting fluid and a normal, resistivefluid [11].

The Two-Fluid Model could successfully account for the AC resistance of a superconductor. When an applied electric field varies with time, the superconducting fluid acts as an inductor, while the normal fluid acts as a resistor in parallel with the inductor. In the limit of the DC case, the inductive impedance drops to zero, and the normal fluid resistance is shorted out. The Two-Fluid Model did not provide any insight into the factors that accounted for the formation of the superconducting fluid.

In 1957, Bardeen, Cooper, and Schrieffer published their theory (now known as the BCS theory), for which they were awarded the Nobel Prize in physics [12]. They explained the origin of the attractive force between electrons, and developed the mathematical formalism to demonstrate that such a force results in the formation of what had been characterized as two fluids by the phenomenological theory. Recent discoveries of high-temperature superconductors may

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not have the same attractive force as that proposed by BCS; nevertheless, the mathematical underpinnings of the BCS theory appear to be valid when the attractive force has been identified [13].

The superconducting A/D converters that are under study at MITRE employ the more conventional, low-temperature superconductors; therefore, the BCS theory is relevant to this discussion. Attraction between electrons in a BCS superconductor takes place through an indirect interaction with lattice vibrations. A conduction electron (one not tightly bound to an atomic nucleus) is free to move around in a metallic solid. Electrons have the same charge and normally repel each other; electrons can, in fact, attract the ionic cores of the metal (the atomic nuclei and tightly bond core electrons), which exhibit a positive charge. The distortion of the solid lattice near a conducting electron appears to another electron which is about ~ 1 μm a way to give the first electron a slightly positive charge. The reciprocal attraction also takes place, so the two electrons can thereby form a loosely coupled bound pair (called a Cooper pair).

Electrons are spin one-half particles. Like all fermions, they must satisfy the Pauli Exclusion Principle: only one electron can exist in a particular state of the system. The Cooper pair electrons form spin zero or spin one particles (spin zero is expected). They are bosons, and do not have to satisfy the Pauli Exclusion Principle. The Cooper pair electrons, therefore, all condense into the lowest energy state; in this state, long-range correlation of the phase of the Cooper pair wave-functions is apparent. The correlation of electronic wave-function phase, over macroscopic distances, results in some very useful characteristics, which are discussed shortly.

At this point, a brief review of the implications of condensation of Cooper pairs is in order. The Cooper pair wave functions have already built into their formulation, the interaction between the electrons and the lattice vibrations. The Schroedinger wave equation does not have any other interactive terms. As such, there is no scattering of Cooper pair electrons (this is called second quantization in quantum mechanics). Since the scattering of charge carriers is at the source of resistance, the Cooper pair electrons do not exhibit DC resistance.

The preceding picture of condensation neglects the effect of temperature. As the temperature increases from absolute zero, lattice vibrations begin to increase in magnitude. Some

vibrations become strong enough to break up the Cooper pairs, and the two electrons become normal electrons (that is, they exhibit resistance). The higher the temperature, the more Cooper pairs are broken up; at a critical temperature, which depends on the mechanical and electrical properties of the lattice, all Cooper pairs are destroyed and the solid reverts to its normal state.

A correlation between the BCS theory and the Two-Fluid Model can be made with ease. Cooper pair electrons comprise the superconducting electron fluid, while broken pair electrons comprise the normal fluid. The BCS theory can correctly explain the appearance of the zero resistance state and its persistence at low but finite temperatures. The BCS theory also supplies an explanation of the Meissner effect (the expulsion of magnetic fields from a superconductor), but the details of the explanation are complicated by electrodynamic and many-body physics formalism and is omitted from the present discussion. Instead, a heuristic explanation of certain aspects of the Meissner effect is given during the discussion of flux quantization in Superconducting Quantum Interference Devices (SQUIDs).

JOSEPHSON EFFECTS AND JUNCTIONS

Consider a very thin, non-superconducting region separating two superconductors. In 1962, Josephson [14] postulated that Cooper pair electrons can tunnel, as a pair, through the non-superconducting region, if it were sufficiently thin. A JJ so formed behaves as a superconductor up to a specific current density, beyond which it reverts to a normal tunnel junction. Thus, the junction would pass current up to a critical value without a voltage appearing across the junction; this phenomenon is called the DC Josephson effect. When a DC voltage is applied across the non-superconducting region, the energy states on each side of the region are shifted with respect to each other. The energy shift is

$$\delta E = 2eV \tag{1}$$

where V is applied voltage and e is the electronic charge. The factor of 2 is present because two electrons are tunneling as a Cooper pair. In order for the Cooper pair to tunnel across the non-superconducting region, it must now radiate a photon, with a suitable frequency to balance the energy difference

$$hf = \delta E = 2eV \qquad (2)$$

or

$$f = \frac{2e}{h}V \qquad (3)$$

In these equations, h is Planck's constant. The ratio (2e/h) is equal to 483.6THz/V. The generation of high frequency radiation in a JJ in response to an applied DC voltage across the junction is the AC Josephson effect. Brian Josephson received the Nobel Prize in physics for his work in the tunneling of Cooper pairs.

The rich behavior of the JJ, including high-speed switching from the zero-voltage conduction state to the finite-voltage conduction state, generation of high frequency radiation in response to a DC voltage bias, and low power dissipation, has led to many investigations of the use of JJ in electronics. Unfortunately, the JJ device is a two-terminal element that exhibits many non-intuitive characteristics; in fact, its complexity has seriously slowed progress in the application of JJs. In addition, the junction properties depend strongly on the characteristics of the non-superconducting region. Reproducibility of junction characteristics in a highly integrated monolithic structure has been an issue.

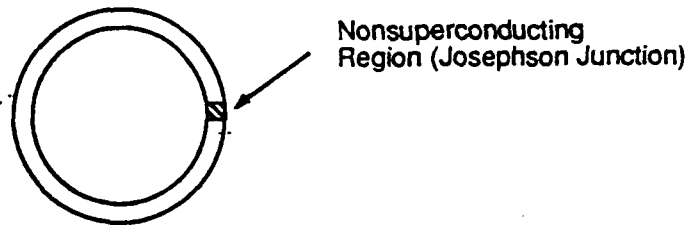## SUPERCONDUCTING QUANTUM INTERFERENCE DEVICES (SQUIDS)

A very interesting device can be formed by including a JJ in a ring of superconducting material. Consider first the situation in which there is no magnetic field present. The ability of Cooper pairs to tunnel through the non-superconducting region implies that the Cooper pair wave function is correlated around the ring. Moreover, the phase of the wave function must pass through an integral multiple of 2π radians in going around the ring. It can be demonstrated [15] that the number of nodes in the Cooper pair wave function is proportional to the magnetic flux, Φ, passing through the ring

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$$\Phi = \iint_S B \cdot dS \qquad (4)$$

In equation (4), B represents the magnetic field and S is the enclosed, open surface of the SQUID. The implication to a solid superconductor is that ring currents would have to be induced to maintain the relationship between flux and wave function nodes. It is energetically more favorable in the solid superconductor to generate currents at the surface to expel the magnetic flux. This is a heuristic explanation of the Meissner effect.

Consider now a SQUID to which a static magnetic field is applied. A Cooper pair current is induced in the superconducting loop to counteract the applied magnetic flux. This induced current is a consequence of Lenz's law; as the magnetic field increases, the induced current increases. When the critical current of the JJ is exceeded, the junction goes normal, a voltage pulse appears across the junction, an additional flux quantum ($\Phi o = h/2e$) is admitted to the SQUID, and the Cooper pair wave function gains another node. The current flowing in the SQUID is now in the opposite direction with a magnitude just below the JJ critical current. As the flux increases, the current decreases in magnitude, passes through zero, and then begins to approach the junction's critical current again for the admittance of yet another flux quantum. When the magnetic flux decreases, the process occurs in reverse, with negative voltage pulse appearing across the junction and flux quanta being expelled. Figure 1-1 illustrates the response of a SQUID to an applied magnetic flux.

The situation described above consists of a single JJ SQUID. SQUIDs with two or more junctions in the superconducting loop are common. The response of SQUID current versus applied magnetic flux for a two-junction SQUID resembles the interference pattern of a two-slit diffractometer. This is why the SQUID is a Quantum Interference Device [16].

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Nonsuperconducting
Region (Josephson Junction)

a) SQUID Configuration
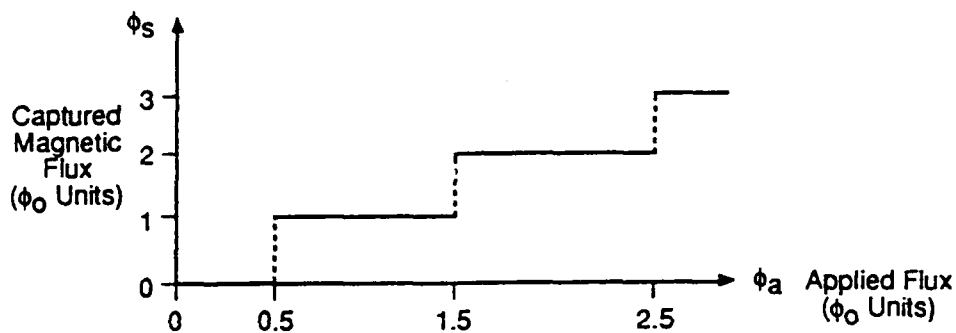
b) Magnetic flux in SQUID as a function of applied magnetic flux (ϕ_O)
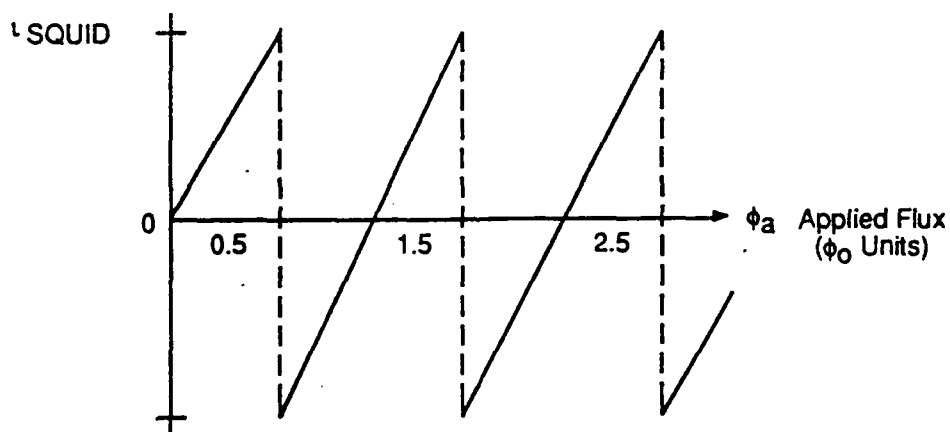
c) Current induced in SQUID as a function of applied magnetic flux (ϕ_a)

Figure 1-1. Response of Superconducting Quantum Interference Device (SQUID)

SECTION 4

SUPERCONDUCTING A/D CONVERTER ARCHITECTURES

This section reviews superconducting A/D converters, and also describes state-of-the-art counting and parallel JJ architectures (more details in reference 7). The MITRE architecture is then reviewed in the context of current designs.

STATE-OF-THE-ART SUPERCONDUCTING A/D CONVERTERS

Superconducting A/D converters can be broadly characterized as counting types and parallel JJ architectures. Within each broad type are several subcategories. Generally, the counter-type architecture is suited for applications where more than 8 bits of precision are required and the input bandwidth is less than 1 GHz. Parallel type A/D converters are superior in applications requiring 6 or fewer bits and signal bandwidths exceeding 1 GHz.

Counting Type A/D Converters

The tracking A/D converter employs the flux quantization phenomena in SQUIDs to track an analog signal. The analog input signal is magnetically coupled to a SQUID; each time the signal rises or falls to inject or expel a magnetic flux quantum from the SQUID, a voltage pulse is produced across the JJ. The pulses are typically 1-10 psec in duration and of millivolt amplitude; therefore, circuits employing JJs are necessary to detect and count them. During the interval that the counter is being read, it is possible for pulses to be lost. Lee [17] has developed a biasing scheme for the SQUID device in which it is made hysteretic during the counter read cycle, and then biased non-hysteretic during counting intervals. In this fashion, no pulses are lost, and counting rates of 100 GHz are possible. For a 16-bit resolution, this corresponds to a sample rate of 1.5 Msamples/sec. Recently J. Przybysz of Westinghouse has described the construction of a 14-bit, 1 Msample/sec converter based upon this architecture [18].

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A second counting-type superconducting A/D converter is based upon the AC Josephson effect. The input signal is applied to a JJ, and the junction oscillates with a frequency proportional to the applied voltage (483.6 MHz/μV); the oscillations from the junction drive a counter. The counter output is proportional to a time-averaged (over the counting interval) Josephson frequency, and consequently time-averaged voltage. A sample rate of 1.5 Msamples/sec for 16-bit resolution seems feasible.

Parallel-Type Superconducting A/D Converters

Two types of parallel superconducting A/D converters have been reported in the literature. The first type exploits the periodic response of SQUIDs, while the second is based on conventional semiconductor architectures, but capitalizes on the high speed of JJs as compared to semiconductor devices. Because of limitations on component precision, parallel-type superconducting A/D converters are generally limited to 6-8 bits of precision.

Consider the two-junction SQUID illustrated in figure 1-2A. The SQUID measuring current Ic can be used to evaluate the magnetic flux Φ passing through the SQUID, and consequently, the magnetic field (B = Φ/S) normal to the plane of SQUID. Here S is the free area enclosed by the SQUID.

Figure 1-2B displays the response of the SQUID by showing the relationship between the critical value of I_c, which causes a junction to switch from the superconducting (zero voltage) state to the normal (voltage) state. The critical value varies between twice the junction critical current i_c and zero [16].

If the analog signal is magnetically coupled to the SQUID, and I_c chosen such that half the distance along the x-axis $\tilde{I}_c$ is below I_c, and the other half of the distance $\tilde{I}_c$ is above I_c, then a periodic comparator has been formed with an output voltage as a function of input current (as shown in figure 1-2C). The scale on the x-axis of figure 1-2C can be altered by changing the size of the SQUID, (that is, by altering A) or by changing the magnetic coupling strength of the input signal to the SQUID.

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a) SQUID Circuit Configuration

Note: ι is current induced in SQUID by magnetic induction $\vec{B}$

ι_c = Junction critical current when B = 0

b) Critical value of $\tilde{I}_c$ required to cause a junction to switch from superconducting to voltage conducting state as a function of B

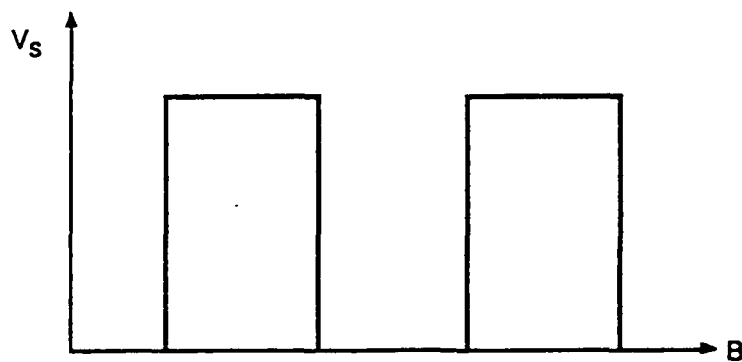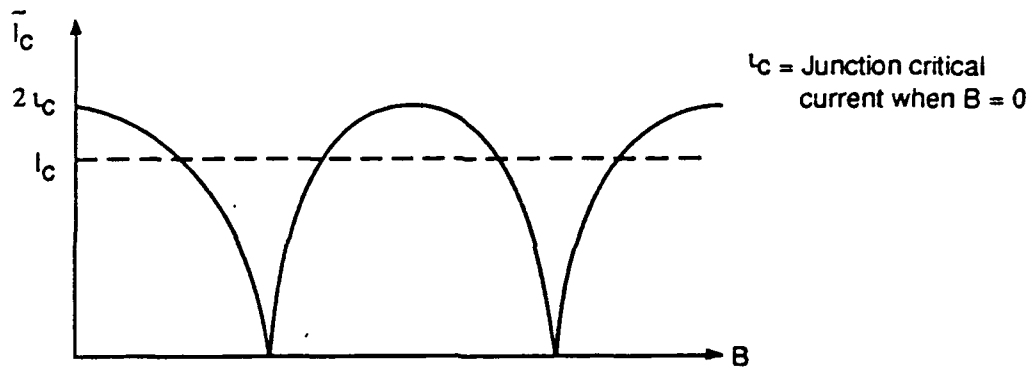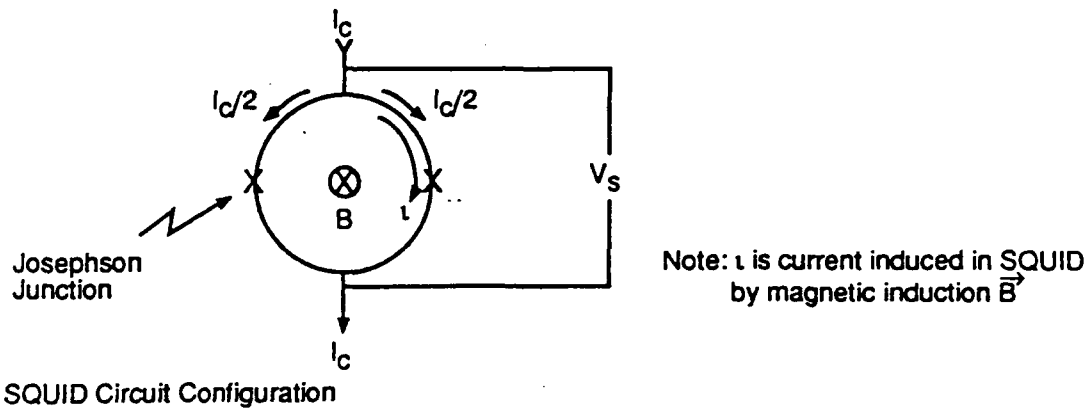c) Voltage output of SQUID (V_s) when I_c is chosen as in (b) above

Figure 1-2. Two-Junction SQUID Used as Comparator with Periodic Response

A suitable selection of N such SQUIDs with area or coupling strength decreasing by factors of two can form an N-bit analog-to-Gray code digital converter. In practice, I_c is pulsed to read the comparator. Recently, a 4-bit 5 Gigasample/sec converter employing this architecture was reported [19]. The key feature of the periodic comparator A/D converter architecture is that a single comparator is required for each bit of precision. Unfortunately, the high-speed performance of the converter is limited to slowly varying input signals -- the settling time of each comparator limits the input signal slew rate. This limit occurs when the I_c pulse occurs during the time when the SQUID is still adjusting to the rapidly varying input signal.

The flash Josephson A/D converter architecture requires 2N-1 comparators for N bits of precision. It basically utilizes each JJ comparator as a non-periodic comparator with a single decision threshold. Projections of performance of a converter constructed utilizing the flash Josephson architecture suggest that 2.7 bits effective precision at 98 Gigasamples/sec is an upper limit [7].

MITRE SUPERCONDUCTING A/D CONVERTER ARCHITECTURES

Quantum Effect A/D Converters

During the first 18 months of our investigation of the use of superconducting electronics to enhance A/D conversion, we concentrated our efforts on the use of residue number system (RNS) representations in the A/D conversion process. An RNS representation of a number is a unique description of the number as a series of remainders with respect to division by a set of mutually prime base integers. The exploitation of RNS representations in the conversion process was suggested by several phenomena associated with Josephson junctions and SQUIDs, which made feasible the direct analog computation of the residue of an input signal with respect to a predefined base. High-speed analog-to-residue conversion is attractive even if RNS-based signal processing is not used. Digital computations to covert from an RNS-based signal representation to conventional, binary representation can be performed simply and rapidly. The RNS-based conversion technique replaces the A/D conversion process by a series of parallel conversions of lower precision and higher sampling rates. It was also conjectured that the use of parallel channels of lower

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precision could also relax component precision requirements. Error analysis and simulations during FY91 proved that this conjecture is indeed true; however, the expected advantage in using the RNS-based approach (relaxation of the component precision requirements from 1 part in 2^{16} to 1 part in 2^5) could not be met by using five residue bases each having 5-bit precision. A paper describing the limited precision enhancement achievable by using RNS-based conversion techniques has been prepared.

Three different approaches to analog-to-residue conversion using superconducting electronics were evaluated. One approach of particular interest was based upon a proposal by F. N. Eddy of MITRE. It is described in detail in reference [20]. A superconducting implementation of this A/D converter architecture was evaluated in detail and a key component, the superconducting VCO, was fabricated and measured. A patent application has been filed for this A/D conversion scheme.

The superconducting implementation of the A/D converter developed at MITRE is based upon the alternating current (ac) Josephson effect. A single Josephson junction could conceivably be used to perform the voltage-to-frequency conversion required for the MITRE A/D converter; however, the output power from a single junction is insufficient for use in the rest of the circuit. An array of Josephson junctions can be constrained to oscillate at a common frequency when subjected to an input signal. Phase-locked oscillation of the array is accomplished by means of a suitable feedback arrangement. The array of Josephson junctions acts as a voltage-to-frequency converter that generates a signal whose frequency is proportional to the magnitude of the input voltage.

The output of the Josephson junction VCO is fed in parallel to instantaneous frequency discriminators consisting of delay lines and phase detectors. The phase difference between the delayed and original signals are compared. The delay line lengths are selected to be inversely proportional to a set of mutually prime numbers so that this circuit effectively performs analog-to-residue number conversion. If the delay line lengths are selected to be proportional to powers of two, then this circuit performs A/D conversion using the conventional binary number representation of the analog input.

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We identified two key components in the MITRE A/D converter. These are the voltage-to-frequency converter and the delay line. The former affects the converter precision and speed, while the latter influences precision alone. During FY90 we undertook a joint development effort with Prof. James Lukens of the State University of New York at Stony Brook for the design and fabrication of a phase-locked array of Josephson junctions to serve as a VCO that would be tunable in the frequency range from 9 to 18 GHz with as sufficiently narrow spectral line width -- 137 kilohertz (kHz) -- to provide 16-bit voltage resolution. VCO output power of approximately 3 nanowatts delivered to a 50 Ohm load was required. The superconducting VCO was fabricated during FY90 and characterized at Stony Brook and at MITRE during FY91. Technical Report 2 is a report by the Stony Brook group of the design and measurement of the VCO. Technical Report 3 describes the MITRE measurement of the VCO. Correlation of the measurements made at the two locations using different instrumentation was achieved except in terms of output power where measurement differences were attributed to differences in instrumentation bandwidth. The resultant VCO consisted of a linear array of 65 Josephson junctions. Output power delivered to a 50 Ohm load was found to be 4 nanowatts. The oscillator spectral line width was under 300 kHz and could be modulated with frequencies as high as 500 MHz. Prof. Lukens is confident that with additional adjustments to the feedback network, the spectral line width could be assured to be under the requisite 137 kHz. The superconducting VCO may prove useful as a frequency-agile signal source for communications applications. Further development work is required to perfect such a signal source.

The second key component associated with the MITRE A/D converter architecture is the delay line. To achieve 16-bit precision, the delay line lengths must be held to one part in 2^{16} with a minimum delay of approximately 500 nanoseconds. For a 500 nanosecond delay line length, the delay tolerance must be kept to 7.5 picoseconds over the 9-18 GHz frequency band! Based upon precision enhancements that may be possible by means of the use of RNS-based representations (see Technical Report 4), a relaxation of this requirement to one part in 2^{13} may be feasible. Analysis of current technology suggested that a tolerance of one part in 2^{8} is the best achievable tolerance [20]. The minimum delay line length limits the speed of this converter circuit to 2 million samples per second. The factors governing

delay line requirements suggest that converters using the MITRE architecture in excess of 8-bit precision are not feasible with current technology.

While the analysis of the limits of precision of the architecture were in progress, we undertook an investigation of techniques to achieve the required long delays in superconducting technology. Stripline was chosen to minimize dispersion across the frequency range of operation. Time delays on the order of 500 nanoseconds are difficult to achieve because of the long lengths of the lines required to implement them. One promising approach to develop compact delay lines is to exploit the phenomenon of *kinetic inductance* in superconducting stripline. As the width of the dielectric under the stripline becomes very thin, a slow wave mode of propagation in the line becomes feasible. The propagation characteristics of this slow wave depend strongly upon the complex conductivity of the stripline. For superconducting striplines, the complex conductivity is the parallel combination of the inductive impedance of the superconducting electrons in parallel with the inductance and resistance of the nonsuperconducting electrons in the film. Current stripline design techniques and automated design tools do not take account of the complex conductivity of the superconducting films. MITRE has developed a technique to use a complex conductivity model in the design of stripline structures, so that the slow wave propagation mode can be used effectively. The contribution is described in Technical Report 5. It is of value beyond its application to the MITRE superconducting A/D converter architecture that spurred its development.

During the course of this project, we also investigated the limitations of other A/D converter architectures that employ the unique quantum phenomena found in Josephson junctions and SQUIDs. A SQUID consists of one or more Josephson junctions connected with a ring of superconducting material. Magnetic flux through a SQUID is quantized in units of 2×10^{-15} Webers. A SQUID consisting of two Josephson junctions can pass a direct current below the SQUID's critical current without a voltage drop. If a magnetic field is applied to a SQUID, the induced current around the ring alters the apparent critical current of the SQUID. The induced current adds to the applied current in one junction and subtracts from the applied current in the other junction. The change of the SQUID's critical current is periodic with the period related to the admission or expulsion of magnetic flux quanta from

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the SQUID. A single-bit A/D converter can be constructed from such a periodic threshold SQUID by applying current to the SQUID which will exceed the critical current over half the input dynamic range. Multiple-bit converters can be implemented by adjusting the magnetic coupling of the input signal in powers of two to an array of SQUIDs. An analog-to-residue converter can be constructed by scaling the coupling in parallel channels to the base numbers of the residue number system. Magnetic coupling can be scaled by either changing the size of the SQUID area, or by using a resistor ladder to scale the current driving each SQUID. The concept of using period threshold devices to perform analog-to-residue conversion is discussed in Technical Report 6. Six-bit A/D converters based upon the periodic threshold response of SQUIDs have been reported by the National Institute of Standards and Technology with sampling rates as high as 2 billion samples per second. Performance of the periodic threshold converter can be enhanced by sharpening the input signal transitions. The use of superconducting circuitry to sharpen the input signal is reviewed in Technical Report 7. Increasing the precision of the period threshold converter is difficult because of component precision issues. Typically, integrated microelectronic components cannot be controlled to tolerances tighter than 0.1 percent. This corresponds to a precision of approximately 8 bits.

Signal Processing Enhancements

One of the objectives of this project was to investigate the feasibility of increasing A/D converter performance through the use of superconducting electronics. The performance goals were 16-bit precision at 125 million samples per second. The architectures that we have investigated can be employed to perform analog-to-residue or analog-to-digital conversion depending upon the choice of circuit parameters. They are all based upon direct exploitation of a quantum mechanical effect, and, except for the architecture that relies upon pulse counting as magnetic flux quanta enter and leave a SQUID, all have difficulty realizing precision in excess of 8 bits. The counting converter cannot achieve the desired sampling rate. High performance, semiconducting A/D converters overcome these same limitations in precision due to circuit tolerance issues by trading precision for speed.

The fundamental concept underlying the use of successive approximation techniques is that a faster than necessary, lower-precision converter can perform several conversions in sequence to achieve a higher level of precision. The subranging A/D converter initially quantizes and codes the signal against a coarse grid of values. The output code is converted to an analog signal and subtracted from the input signal. The resultant signal is then quantized and coded. Several such cycles using this approach are feasible with increasing precision available at the expense of overall conversion time. Superconducting A/D converters with precision of 6-bits and conversion rates in excess of 2 billion samples per second as described above were considered as the starting point for a subranging A/D converter (see Technical Report 8). A superconducting implementation of this converter architecture should prove to be faster that its semiconductor counterpart because of the inherent speed of the basic 6-bit superconducting A/D converter. To achieve the desired performance, a track and hold circuit for the input signal is required to reduce aperture jitter to under 70 femtoseconds rms. No superconductor structures can implement a track and hold circuit with such tight constraints. Semiconductor circuits are too slow. Vacuum microelectronics may provide satisfactory speed, but the technology is not sufficiently mature. Moreover, a sampling pulses for the system must have rise times on the order of ten femtoseconds. A laser system could produce such pulses. Our conclusion is that subranging superconducting A/D converters are not practical for short-term implementation.

Another technique to enhance the performance of semiconducting A/D converters is the sigma-delta modulator architecture. In a sigma-delta modulator, one or more single-bit A/D converters track the change of the input signal over previous time intervals. Sampling at the one-bit converters is performed at rates of 100 - 1000 times the required sampling rate. The output of the single-bit converters is a single bit pulse stream which is then converted by a digital signal processing technique called decimation into a sequence of multi-bit samples at the desired sampling rate. Semiconductor-based, sigma-delta modulator converters have been built by Westinghouse with a sampling rate of 5 million samples per second and 14-bit precision.

During FY91 we completed an investigation of the feasibility of developing a superconducting sigma-delta modulator A/D converter. This is described in Technical

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Report 9. Our approach was to replace semiconducting components with their superconducting counterparts. An alternative approach currently under active investigation in industry is to utilize a novel architecture that is dependent on quantum mechanical effects.

Our analyses of the performance of a superconducting, sigma-delta modulator A/D converter suggested that the delay line in the feedback path to each single-bit converter (to allow it to compute the difference of the input from its previous value) was a critical component. Simulation of the performance of the converter using the VHSIC Hardware Description Language (VHDL) and post processing with MATLAB software* is described in Technical Report 10. It suggests that performance degradation is likely to occur with delay line tolerances typical of current microelectronics technology. The sigma-delta modulator implementation based upon quantum mechanical effects does not suffer from this limitation. Performance in excess of our objectives of 16-bit precision with a sample rate of 125 million samples per second seems feasible in the near future. Details about this approach cannot be provided here because the information is proprietary. We plan to closely follow the development of this converter and evaluate its potential for use in C^3I systems.

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* MATLAB is a general purpose mathematics tool kit available from The MathWorks, Natick, MA.

SECTION 5

SUMMARY AND CONCLUSIONS

During the course of this project, we investigated a number of novel techniques to perform analog-to-digital conversion in superconducting electronics. Thorough investigations of the anticipated performance limitations of these techniques, as well as the limitations of conventional A/D conversion architectures, always revealed that some circuit parameter or timing must be held to the required precision of the converter. This is a general limitation of the achievable precision and/or speed of the converter. It is not at all unexpected. Since we are trying to quantize a signal to a specific precision, we must maintain at least that precision in the circuit.

In the course of our investigations, we did identify an A/D conversion technique which may promise to achieve performance of 16-bit precision with sample rates in excess of 125 Msamples/sec. This promised performance is made possible by the use of superconducting electronics and sigma-delta modulation. It is currently being developed in a proprietary fashion by a U.S. company. MITRE plans to follow this work in anticipation of inserting this technology in advanced C^3I systems.

By-products of this project include the design, construction, and measurement of a frequency-agile voltage controlled oscillator constructed from a phase-locked array of Josephson junctions, the development of techniques to design and build compact microwave delay that exploits kinetic inductance effects to achieve long delays in small areas, and an analysis of the improvement to signal precision that can be expected by the use of an extension of the residue number representation to continuous, real signals.

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Technical Report 2

DEVELOPMENT OF A RAPIDLY TUNABLE MICROWAVE SOURCE

by

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Kelin Wan
Linus Fetter
Aloke Jain

ABSTRACT

An array of Josephson effect oscillators has been developed as a rapidly tunable microwave source covering 9 to 18 GHz. Arrays of 65 junctions have been designed, fabricated in niobium tri-layer technology, and subjected to preliminary testing. Our initial goal for these arrays, which have a number of novel design features, was a tuning rate of one megahertz. The majority of the power generated, several tenths of a microwatt, was delivered to a 1Ω on-chip load and detector. A small fraction of the power was coupled through a 50 Ω coaxial line to a spectrum analyzer to study the signal properties of the array. All major design concepts in the source have been demonstrated. Initial tests show that the source can be modulated at frequencies up to 500 MHz.

I. Design Parameters and Projected Performance.

The design objectives were as follows:

- Frequency should be continuously tunable from 9 to 18 GHz by varying the bias current.

- The oscillator frequency should track the bias current modulation to at least 1 MHz.

- The power delivered to a 1 Ω load resistor on-chip should be about $\frac{1}{4}$ μW.

- The linewidth should be less than 100 kHz.

- Broadband 50 Ω coupling out of the cryostat should be available for analysis of the power spectrum.

The following design criteria were developed to meet these objectives. The junctions were to be placed along a 1 Ω superconducting microstrip terminated with a 1 Ω thin film resistor, which constituted the load. The rf current induced in the microstrip by the Josephson oscillations would serve to couple the oscillations of the junctions in-phase so that the rf currents from the various junctions would sum coherently and in-phase in the load. The general theory of such coupling, along with design criteria, have been presented previously.[2-4] Design criteria particular to the present array are discussed below.

- The array length l_{array} must be less than about 1/8 λ_{18}, where λ_{18} is the electromagnetic wave length in the array microstrip at 18 GHz, to ensure continuous tunability.

- The I_cR_J product of the junctions should be less than the operating voltage (18 μV) at the lowest frequency to ensure low harmonic content. Here I_c is the junction critical current and R_J its shunt resistance.

- I_c should be as large as possible ($\simeq 2$ mA) to deliver the highest power to the load. This implies a shunt resistance of $R_J \simeq 0.01$ Ω for each junction.

- The junctions' length (along the direction of rf current flow) should be as short as possible to permit the large number of junctions needed for impedance matching to be placed within $1/8\ \lambda_{ls}$ of each other. The junction length of 2 μm and the junction spacing of 10 μm are set by the practical limits of lithography.

- The junction width is set by the need for low resistances — i.e., wide shunt resistors and low impedance microstrip — and is in the range of 40 to 100 μm. This, coupled with the desired I_c , means that the junctions must be wider than the Josephson penetration depth, λ_J, thus stable operation is not assured. So, one aspect of this project will be a test for stable operation in such wide junctions.

- The array should be biased in "parallel" (that is, the polarity of the dc voltage alternates between successive junctions along the array) to compensate for less than optimal parameter scatter among the junctions and ensure coherent phase-locking.

- The bias leads must present a uniform low inductance to the ac bias modulation to provide rapid tunability. At the same time, a high rf impedance must be presented across the array to avoid shorting out the Josephson oscillations. The bias "tree" discussed below was developed for this purpose.

II.   Layout and Fabrication of the Array Source.

A.   Microwave circuits.

The overall layout of the array is shown in Fig. 1a. Here the 65 junctions are distributed along a 1 Ω microstrip, fabricated on top of a silicon chip. First the ground plane (niobium) is deposited followed by the SiO dielecric. The junctions, along with the remaining microstrip and bias lead, are then fabricated. The microstrip is shorted to the ground plane at the left end and terminated in nominal 1 Ω load resistor on the right. Figure 1b shows an expanded view of the right end of the array. Following the load resistor is the detector junction, which is an independently biased Josephson junction used to monitor the rf current through the load.

A 50 Ω microstrip taps off of the array just before the load. This microstrip is connected, at the upper left, to a 50 Ω coplanar wave guide (CPW) directly on the silicon. The CPW in turn is connected to an SMA connector, which is used to couple the array to a 50 Ω coaxial line out of the cryostat. A more detailed view of the various masking levels for several of the single junction cells adjacent to the load resistor is shown in Fig. 1c.

B.   Bias structure.

The bias leads are seen in the upper right of Fig. 1b. These leads connect to a bias tree as shown in Fig. 1d and ultimately to external bias leads (using, e.g., a silver paint connection) at the base of the tree. The bias tree is superconducting and connects to the array between each pair of junctions. The tree is designed to provide a low inductance, equal impedance path for the bias current between the base of the tree and any point on the array. This is important if the desired high tuning rates are to be achieved. Another important feature of this tree is the high impedance it presents to the rf currents flowing through the array. In order to maximize this impedance, no ground plane has been put under the bias tree. While this leads to a structure which is poorly characterized at microwave frequencies, we shall see below that this does not appear to cause problems.
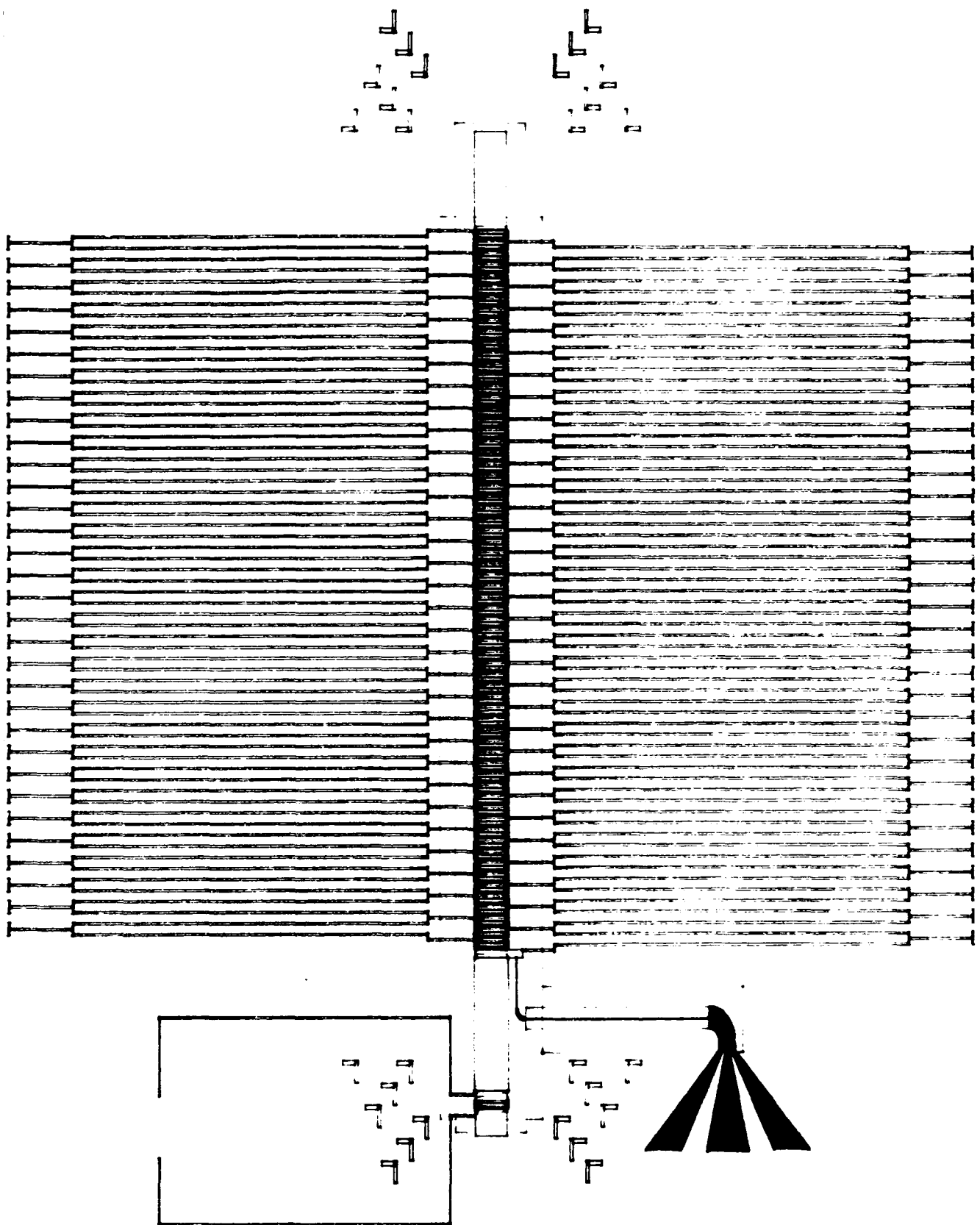
Figure 1a

Outline of EBL generated masks for layers of 65 junction array. Vertical extent of the pattern is approximately 1.4 mm.
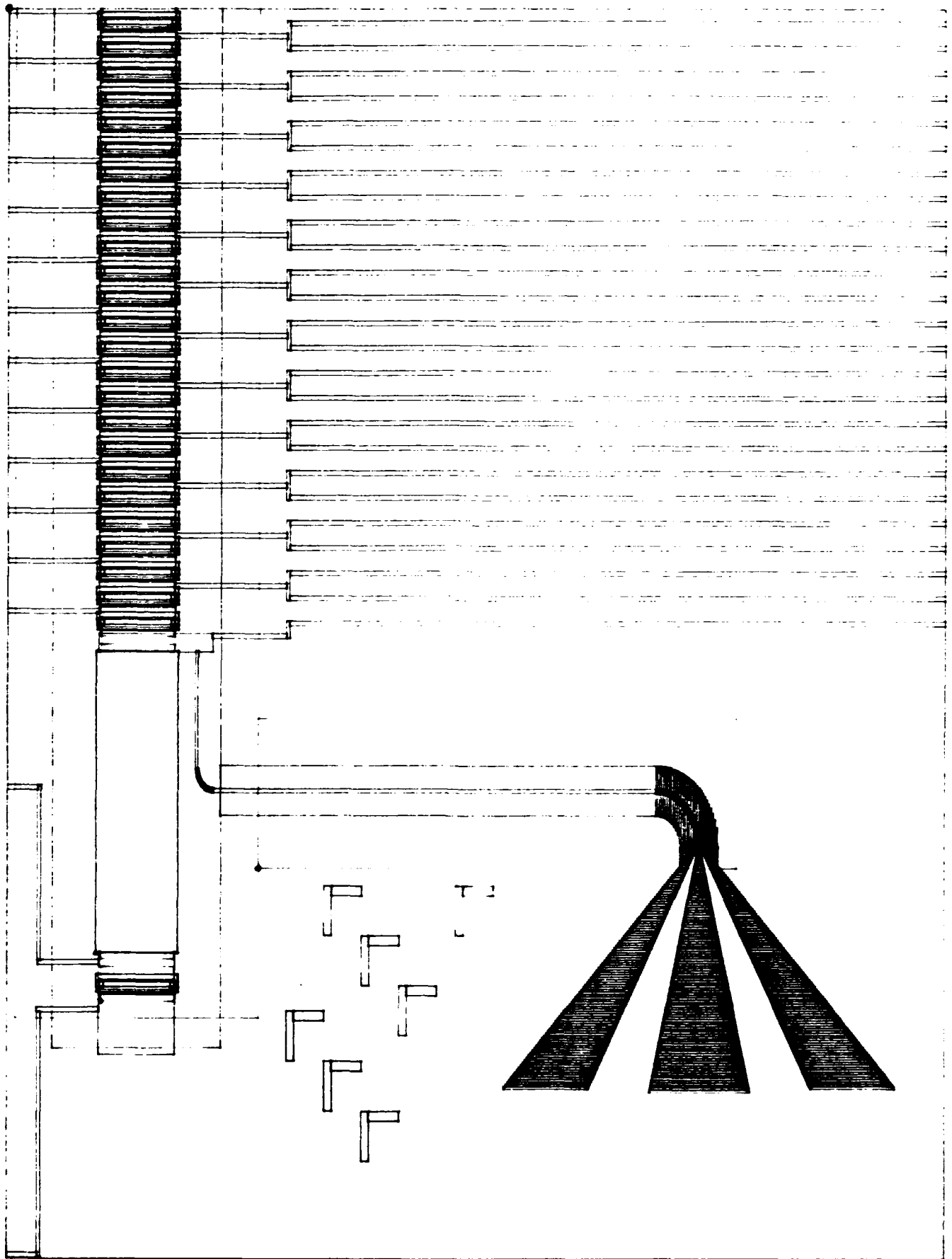
Figure 1b

Enlarged view of upper right quadrant of Fig. 1a. CPW to microstrip transition is shown

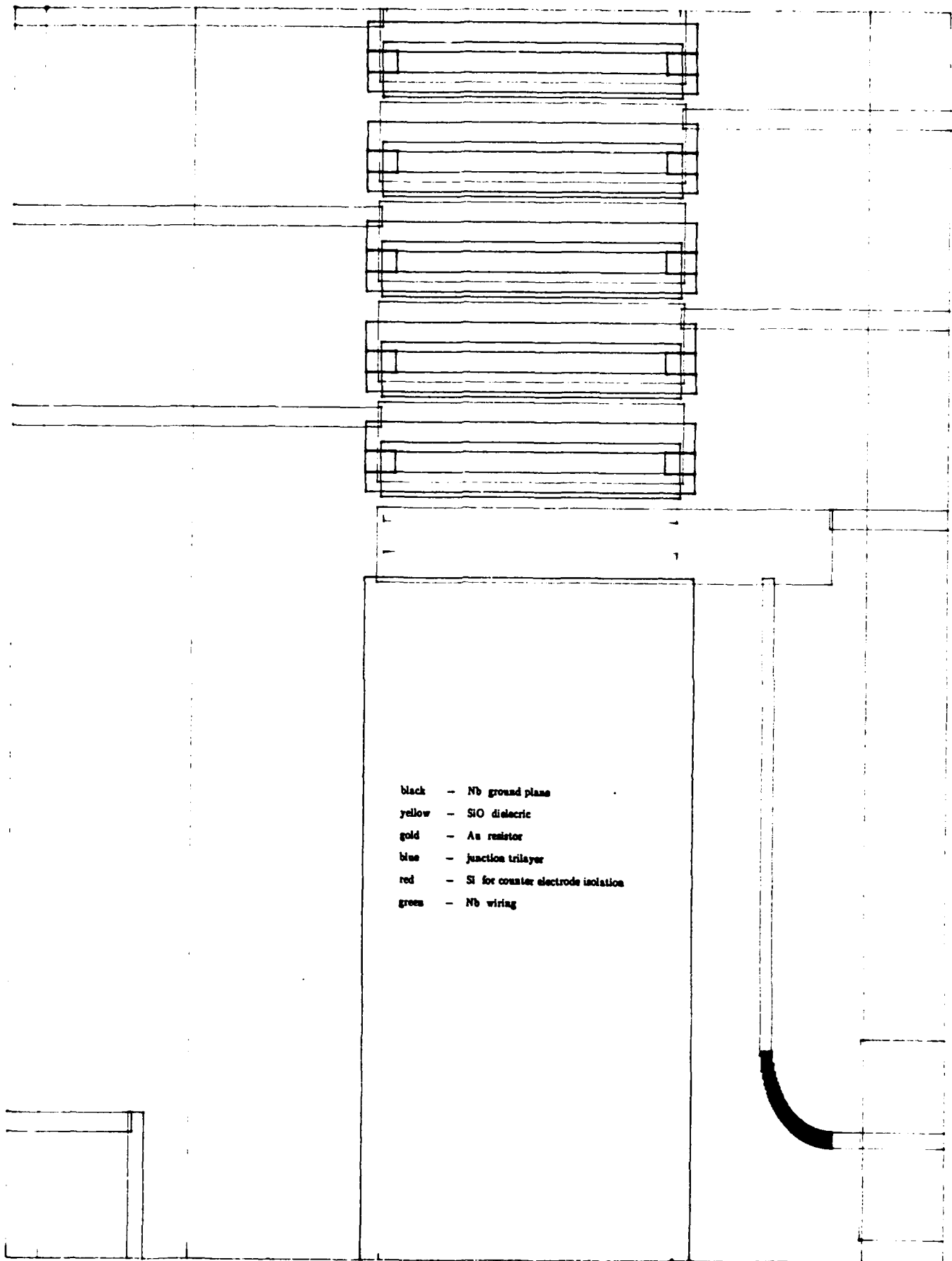in upper right. The load resistor and detector junction are shown in lower right.

black — Nb ground plane

yellow — SiO dielecric

gold — Au resistor

blue — junction trilayer

red — Si for counter electrode isolation

green — Nb wiring

Figure 1c

Further enlargment of 1a   near the left end of the load resistor. Tap for   50 Ω
...crostrip is shown in upper right. The masking patterns for various layers can be clearly
distinguished
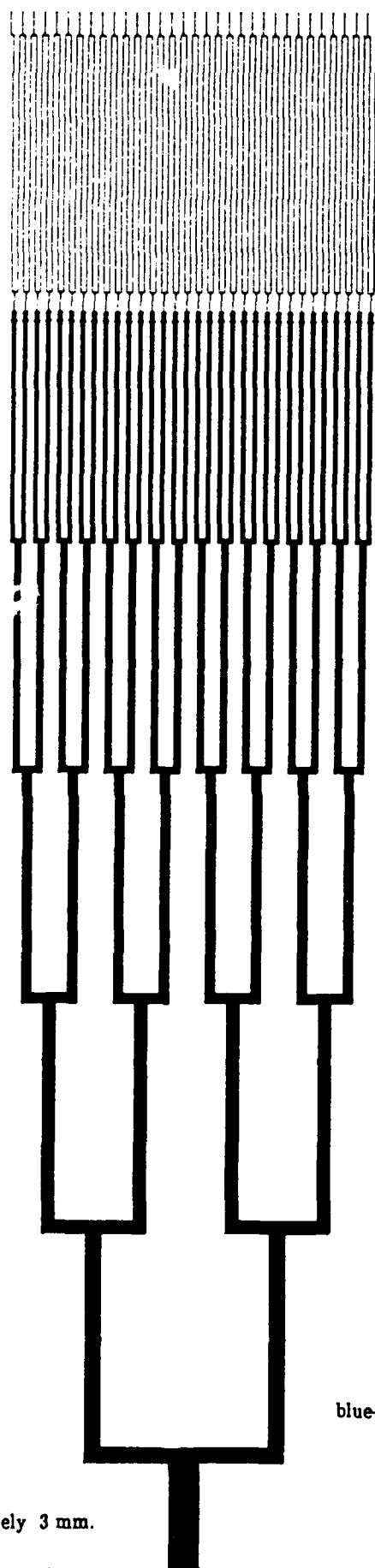
light green — EBL pattern

blue-green — photo-lithographic pattern

Total length of the tree is approximately 3 mm.

Figure 1d

Array bias tree for uniform distribution of the bias current to the junction.
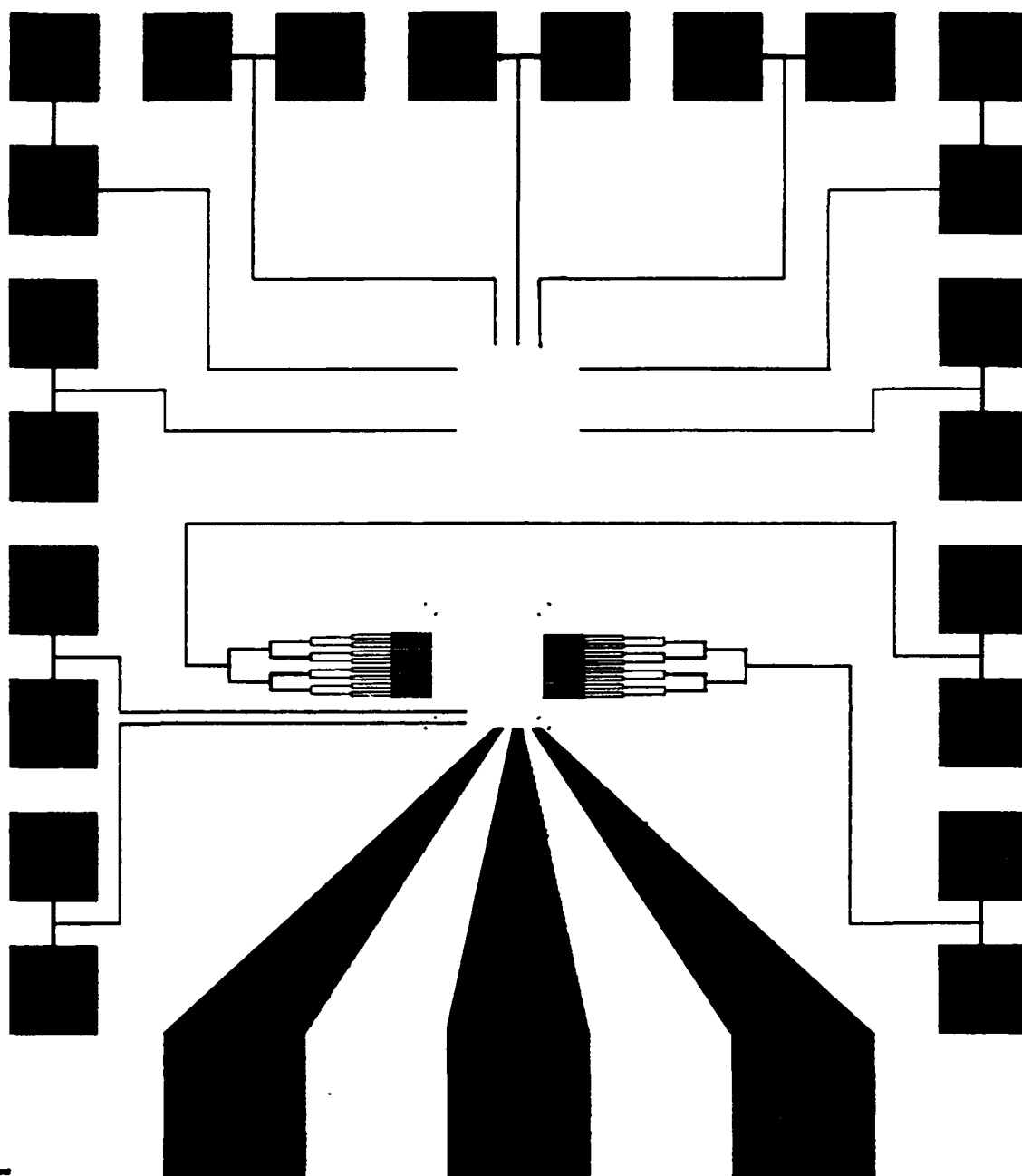
Figure 1e

Photo-lithographic mask for chip. Contact pads, bias tree and CPW structure are shown.

Corner brackets are 0.500 in. apart.

Below the microstrip a second tree, connected between alternate pairs of junctions, completes the bias circuit to the external bias leads. Each junction is, thus, part of two interlocking superconducting loops, so all junctions must have the same average dc voltage and average frequency of oscillation. This parallel bias scheme compensates, to first order, for the nonuniformity in both the junction critical currents and resistances. Although this causes the polarity of the junction's dc voltage to alternate along the array, the rf oscillations are all in phase, so that the rf amplitude across the entire N junction array is just N times that across a single junction.

C.   Josephson junctions.

Figure 2 shows a vertical section through the array illustrating the structure of the niobium trilayer junctions. The key feature here, which differs from the standard process, is the presence of a very low inductance shunt resistor (the gold layer) directly under the junctions. This resistor layer contacts the base electrode and is connected to the counter electrode by the final niobium wiring layer. The details of the fabrication process are presented in subsequent sections. The junctions in the final version of the array are $2\ \mu m$ long by $40\ \mu m$ wide. The design critical current of $2\ mA$ implies a critical current density $J_c = 2.5 \times 10^3 A/cm^2$. The corresponding $\lambda_J = 6\ \mu m$, thus the resulting junctions are about 7 Josephson penetration depths wide. The gold shunt resistors are also about $40\ \mu m$ wide and about 1 to $2\ \mu m$ long.

D.   Test area.

An area has been included on the chip for test circuits as a check on the processing. The masking layout of this area is shown in Fig. 3. The lower right contains a resistor fabricated in the same way as the junction shunt resistors and is designed to provide an independent measure of this resistance. Next to this is a duplicate of the array load resistor which can be used to measure the value of the load resistance in the array. The lower left corner contains a coupled two junction cell with junctions having the same parameters as those in the array. Here one junction essentially acts as the detector of

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Au-Shunted Nb\AlOx\Nb Junction Array

Nb

Nb

Nb

Nb

SiO

Nb

SiO

Nb

SUBSTRATE
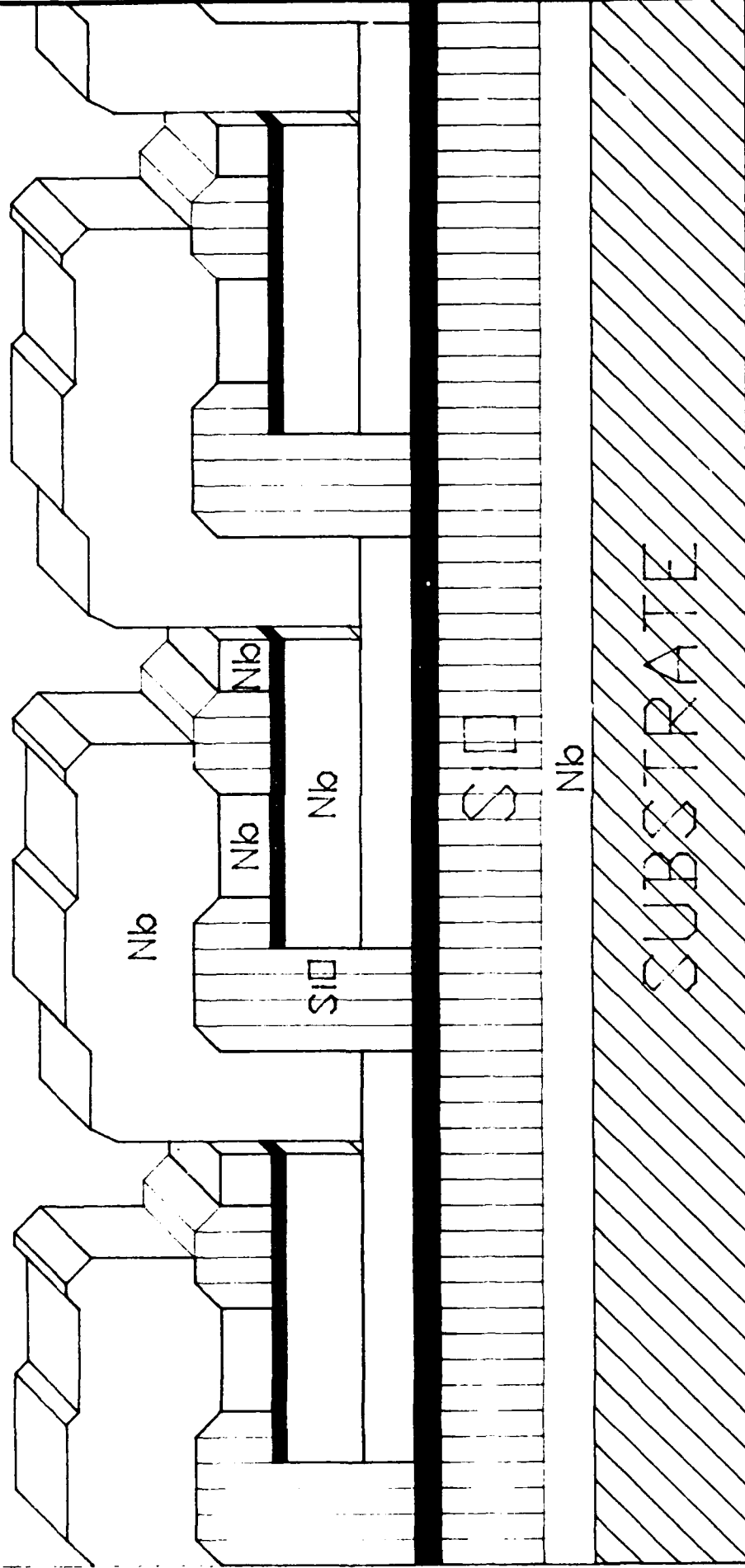
Legend:
- ▬ Au
- ▬ AlOx

Figure 2

Vertical section through the array showing the various layers. Not to scale.
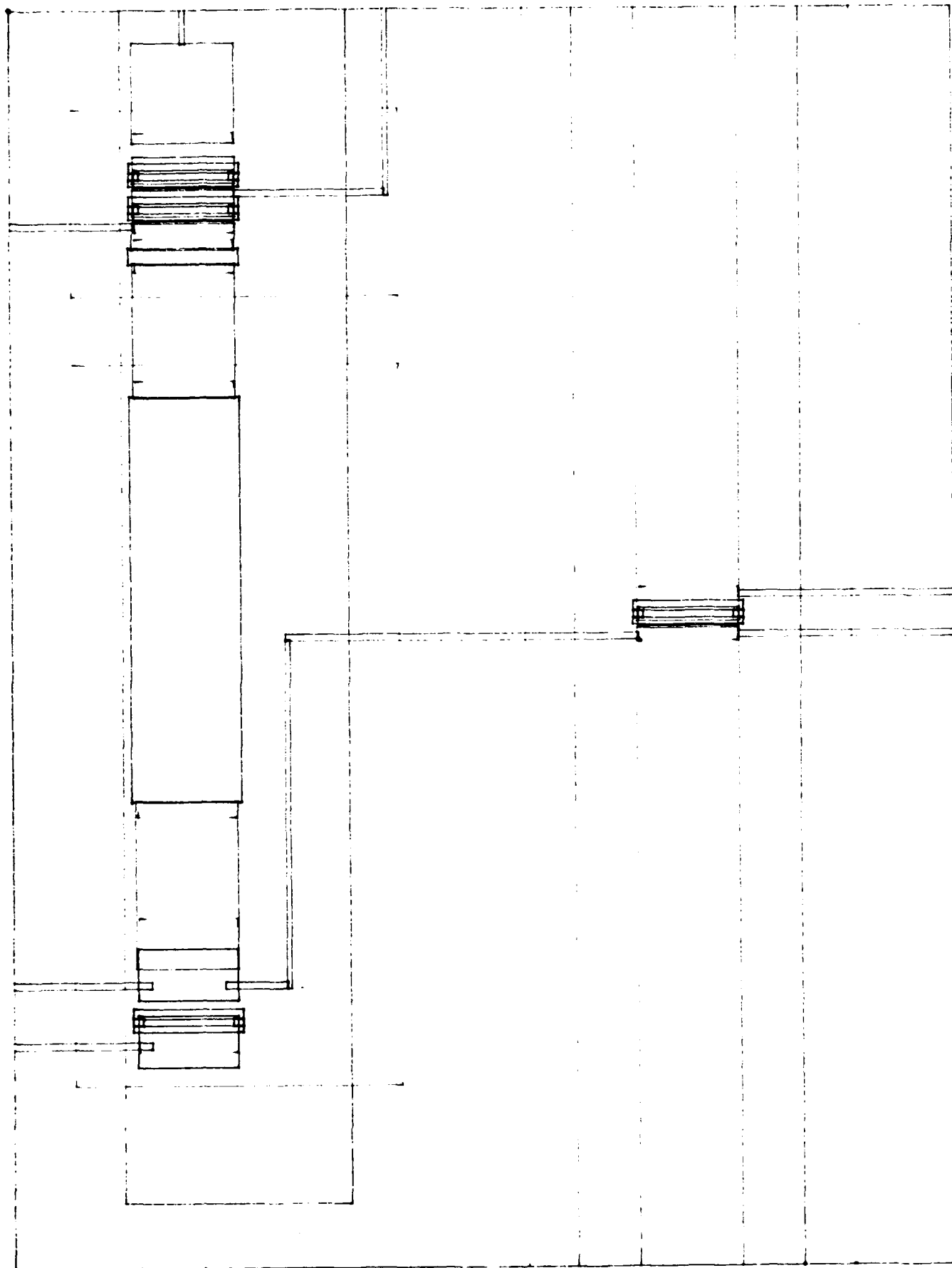
Figure 3

Layout of EBL pattern for the test area of the chip. Top: single junction in a microstrip
resonator. Bottom left: two junction coupled cell for locking strength measurements.
Center: load resistor. Right: junction shunt resistor.

radiation emitted by the other. This has been included as an aid in detecting any instabilities in the wide junctions we are using. The upper half of the test area contains a resonator driven by a Josephson oscillator in its center. This allows us to measure the surface resistance of the microstrip used in the array. The various structures also permit the measurement of contact resistances and critical current of the various bias leads. This test area is located on the left side in Fig. 1e, which shows the overall chip layout with the CPW transition between the microstrip and the SMA connector on the right. The corner brackets in this figure are separated by 0.5 in..

III.   Processing Details.

A.   Substrate cleaning.

The substrates used are 16-mil thick, <100> oriented Si, received in 3 in. diameter slices. The wafers are sliced and cleaved into 0.5 in. × 0.5 in. chips prior to cleaning. The chips are given two acetone/ultrasound treatments, then rinsed in isopropyl alcohol (IPA) followed by distilled water. Two chemical treatments in 1:1 Hydrogen Peroxide : Sulfuric Acid follow, with rinses in distilled water and IPA between and after each. The chips are stored in IPA, and blown dry with nitrogen gas immediately prior to use.

B.   Ground plane fabrication.

Clean, unpatterned substrates are mounted on a water-cooled copper stage in the niobium deposition system. The system is evacuated to a base pressure of 1×10^{-7} Torr, and 200 nm of Nb is sputter deposited in 1 mTorr of Ar. Patterning of this layer is accomplished using AZ1350J positive photo resist as a mask for etching the Nb in a 1:3:8 mixture of $HF:HNO_3:H_2O$. The resulting pattern consists of the array's ground plane, partial bias leads, and contact pads.

C.   Dielectric layer fabrication.

The dielectric layer for the microstrip is patterned with a multi-layer resist system, which is used to assure a tapered edge profile in the deposited material. The resist system consists of a fully exposed 600 nm layer of poly-methyl-methacrolate (PMMA) coated with 6 nm of Al (as a diffusion barrier) and another 600 nm of PMMA. The dielectric plane is patterned in this upper layer of PMMA using electron beam lithography; the pattern is developed in 1:3 methyl-isobutyl-ketone : IPA. The diffusion barrier is etched (in NaOH) through this mask, and the lower pre-exposed layer of PMMA finally developed, yielding a deposition mask with a well-undercut surface-normal profile.

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The masked substrates are mounted on a rotatable and tilted stage in the deposition system, which is evacuated to 3×10^{-7} Torr. A 5 mTorr oxygen plasma is used to remove any residue; then 700 nm of material from a silicon monoxide source is deposited on the tilted, rapidly-rotating substrates. The PMMA masking material is removed in an acetone/ultra-sound bath. The resulting dielectric layer has the well-tapered edge profile needed to assure continuity of subsequent layers across the ground-plane edge.

D.   Resistor/base electrode fabrication.

In our current process, the Au resistor material and a niobium contact layer to the junction's base electrode are deposited through the same deposition mask. This mask is patterned by e-beam lithography in a single layer of PMMA, registered to the previously defined ground plane. In the array region, this mask consists of a single 650-micron long bar through which we first deposit 80 nm of Au (using an e-gun source) and then 40 nm of Nb (using the sputter deposition source). Lift-off is accomplished in acetone, and the multilayer resist system described above is again applied in preparation for the next lithographic step.

The layers discussed above, together with the details of the junction and wiring layer fabrication, are shown in Fig. 4.

E.   Junction "tri-layer" material fabrication.

The multilayer resist is patterned using e-beam lithography. In the array region, this pattern consists of 6 nm × 42 nm windows repeated with a 10 nm period as shown in Fig. 4-1 and closely registered to the resistor layer. The patterned substrates are mounted on a water-cooled copper block and placed in the deposition system, which is evacuated to a base pressure of 10^{-7} Torr. The substrates are briefly sputtered in a 5 mTorr plasma to remove any native oxide from the previously deposited Nb base electrode contact layer. We then dc-sputter deposit 40 nm of Nb in 1 mTorr Ar, followed immediately by the rf-sputter deposition of 2-3 nm of Al in 5 mTorr Ar. High purity O_2 is then admitted to a pressure of 5 mTorr, and the Al oxidized to form

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Au–Shunted Nb\AlO\Nb Junction

Sub.

Nb

SiO

Au

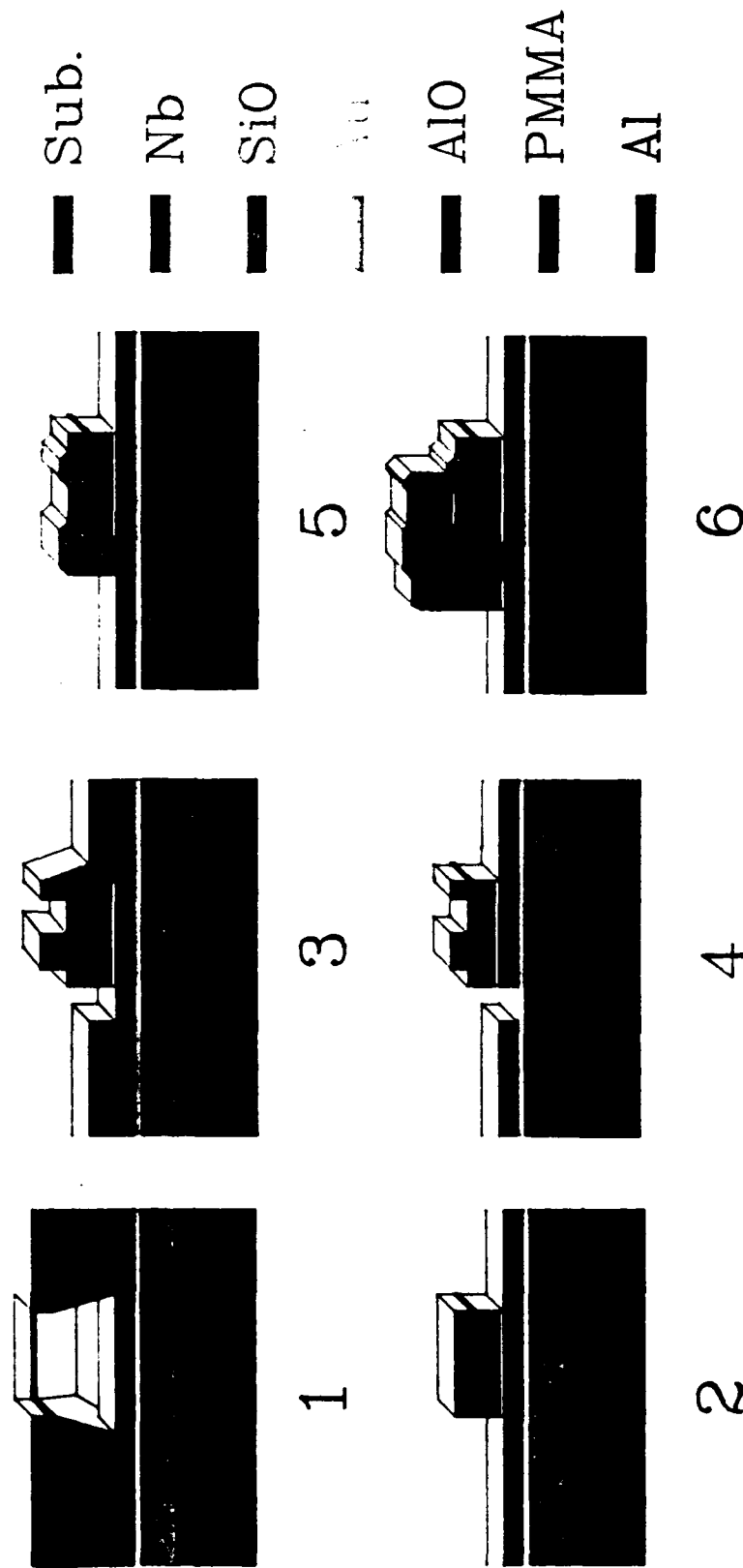AlO

PMMA

Al

1

2

3

4

5

6

Figure 4

Masking and deposition steps for junction and wiring layer formation. See text.

the junction tunnel barrier. The trilayer preparation is completed by dc-sputter deposition of a 40 nm thick Nb counter electrode, again in 1 mTorr Ar. This trilayer, following liftoff, is shown in Fig. 4-2.

F.   Device definition/isolation.

Next, a single 600 nm layer of PMMA is applied and used for the e-beam patterning of the active device area. This pattern is tightly aligned to the previously deposited trilayer islands (see Fig. 4-3) and is first used as an etch mask to define the junction area and the length of the shunt resistors. The reactive ion etch (RIE) is performed using a CF_4/O_2 plasma which attacks only the exposed Nb surfaces, stopping at the Nb/Al interface of the trilayer material and at the Nb/Au interface of the resistor layer. Immediately following this etch, 120 nm of material from a silicon monoxide source is deposited as an isolation layer as shown in Figs. 4-4 and 4-5.

G.   Wiring.

The "wiring" mask is exposed using EBL in a single layer of PMMA, and defines the appropriate interconnections between devices, resistors, the ground plane, and bias leads. The patterned chip is again placed in the Nb deposition system, and briefly sputtered in 5 mTorr of Ar to remove any native Nb oxide from the counter electrode. Nb is dc-sputter deposited to 300 nm, and the mask is removed in acetone/ultrasound. The resulting completed device is shown in Fig. 4-6.
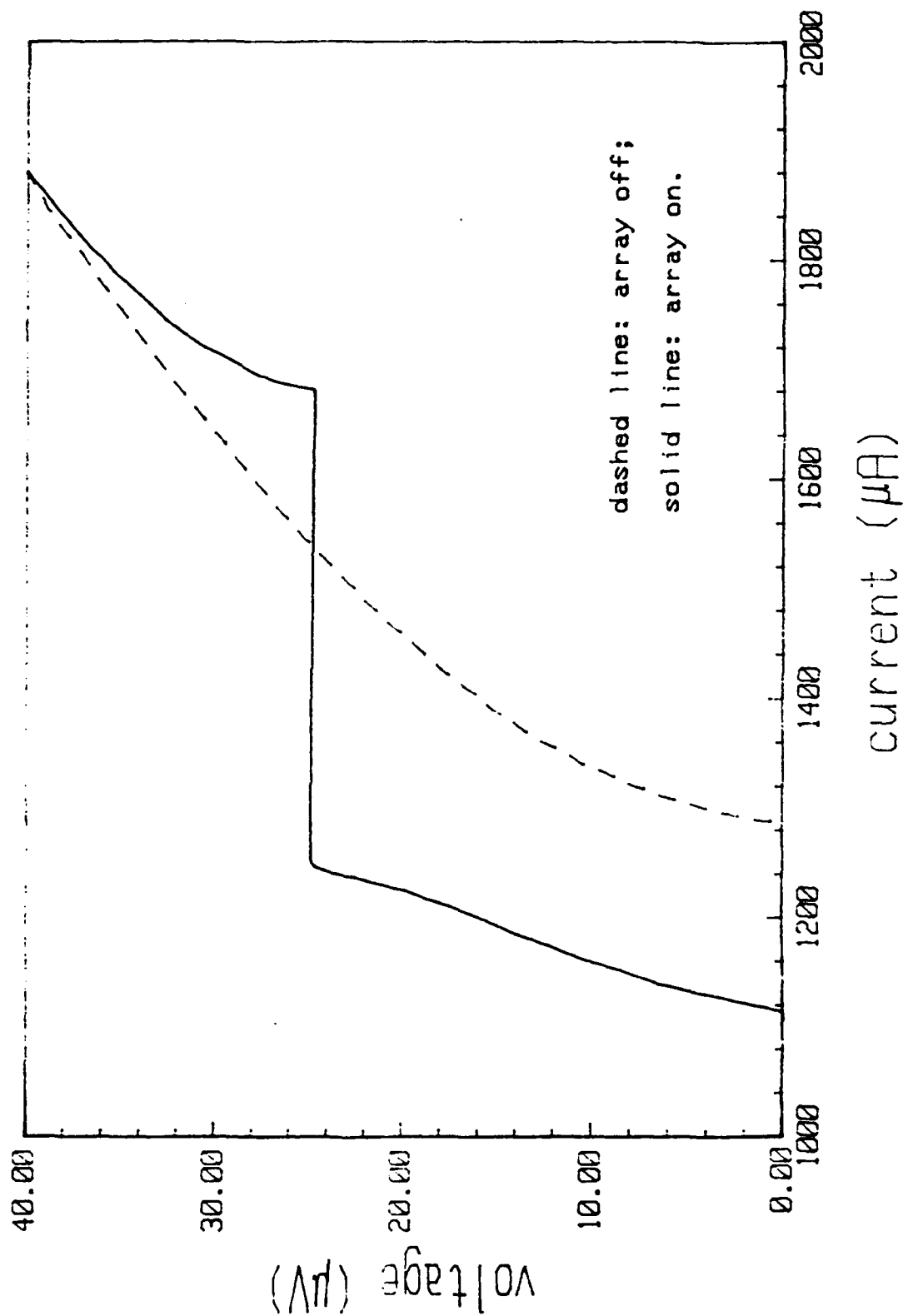
Figure 5

Current-voltage characteristic of detector junction with array operating at 12 GHz (solid line) and array bias current equal zero (dashed line). Step amplitude provides a measure of n load current (see text).
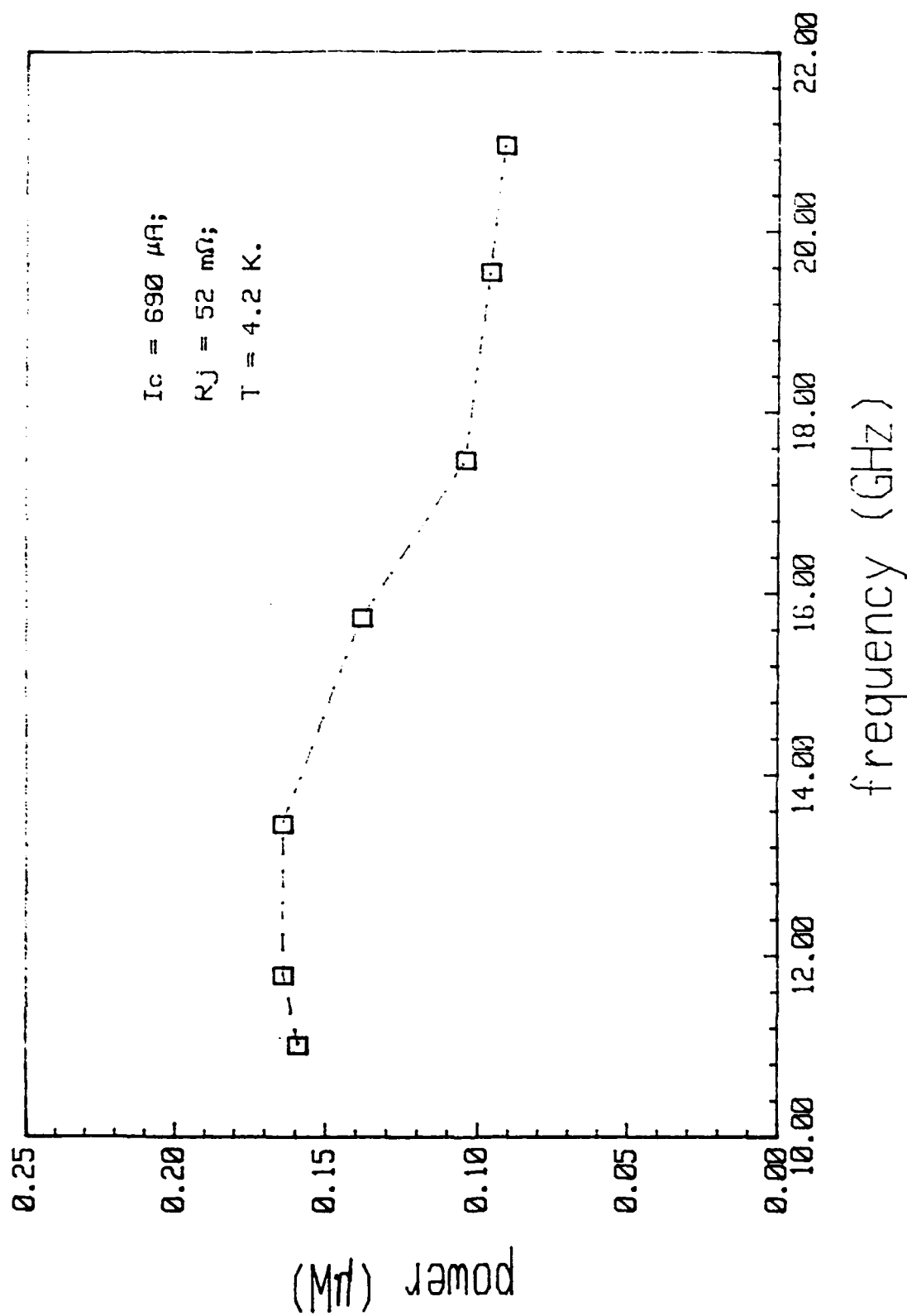
Figure 6

Total power in the fundamental delivered to the on-chip load at various array operating

frequencies from 11 GHz to 21 GHz.

IV. Test Results.

A large number of samples were fabricated during the program in the course of the processing development required by these specialized circuits. While none of the chips so far has worked perfectly, we have — as outlined below — been able to demonstrate all of the essential features of the circuit design. The data discussed below were obtained primarily from chips numbered 20 GHz-8XA, -8XB, and -8XC.

As mentioned above, power can be detected in two ways, either by using the on-chip Josephson detector to monitor the load current or by coupling a fraction of the power through the 50 Ω line to the spectrum analyzer. The first method does not permit a determination of the linewidth. The on-chip detector response is shown in Fig. 5. The amplitude of the Shapiro step, seen when the array is on, is proportional to the rf current through the detector and load.

The step amplitude I_s is related to the peak amplitude of the rf current I_{rf} in the linear response regime by

$$I_s = 2 \alpha I_{rf}$$

with α being given (in the RSJ model) by

$$\alpha = \frac{1}{2(1+v^2)^{\frac{1}{2}}}$$

where $v \equiv V_{dc}/I_c R_J$ is the reduced bias voltage of the junction. See, e.g., Ref. 2, Sec. 3.3. For the data shown in Fig. 5 with $R_J = 23$ mΩ and $v = .94$, the step amplitude of 440μA implies $I_{rf} = 605\mu$A. Thus the power delivered to the load ($R_L = 1 \Omega$) is 0.18 μW. The voltage of the step gives the operating frequency of the array.

By repeating this measurement for a range of array bias currents a plot of array power vs. operating frequency can be obtained, as shown in Fig. 6. Several important pieces of information are contained in this figure. First, the array operates continuously over more than an octave as expected. Second, the power is reasonably constant as the frequency is changed, indicating that the bias trees have not introduced resonances in the

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microwave response. Finally the total power delivered to the load is that expected for in-phase, coherent operation of all junctions. The power level and operating range are somewhat different than our original projections, since the junction parameters of somewhat off from the design values. The major problem here is that the resistance is about five times that desired. Further work on the processing is needed to achieve lower values. This gives a higher than desired $I_c R_J$ product which in turn gives a higher than predicted operating frequency. It also forces the use of a smaller than desired I_c, resulting in a lower than desired power.

This particular sample also had a defective SiO dielectric layer which peeled off on thermal cycling. This problem was caused by incorrect SiO deposition rates and has been corrected. Unfortunately, because of this defect, when 8XA was cycled it failed, so no information on linewidth or tuning rates was obtained. In a second sample (8XB) from this batch, the array also failed for the same reason. One interesting bit of data was obtained from this sample, however; we were able to measure the linewidth of the radiation from the detector junction as a function of bias current. These data are shown in Fig. 7 along with the predictions from the RSJ model assuming a small junction. As can be seen, the measured linewidth is as predicted. This is a strong indication that, even though this junction is $7 \lambda_J$ wide, there are no flux flow instabilities. Note that one would expect radiation from the array itself to have a linewidth factor of 65 (to number of junctions) less than this. A further factor of 5 reduction should be achieved when the resistance is reduced to the design value.

Most of our data have been taken on sample 8XC. Here, the array — though not the detector — functioned and has survived many thermal cycles. Radiation from this sample has been studied extensively with the spectrum analyzer. A minimum linewidth of about 300 kHz was obtained, in line with the single junction spectrum above. A further problem was detected here, however. The contact resistance at the bias pads was 10 - 25 Ω giving a power dissipation there of nearly a quarter of a watt. This led to
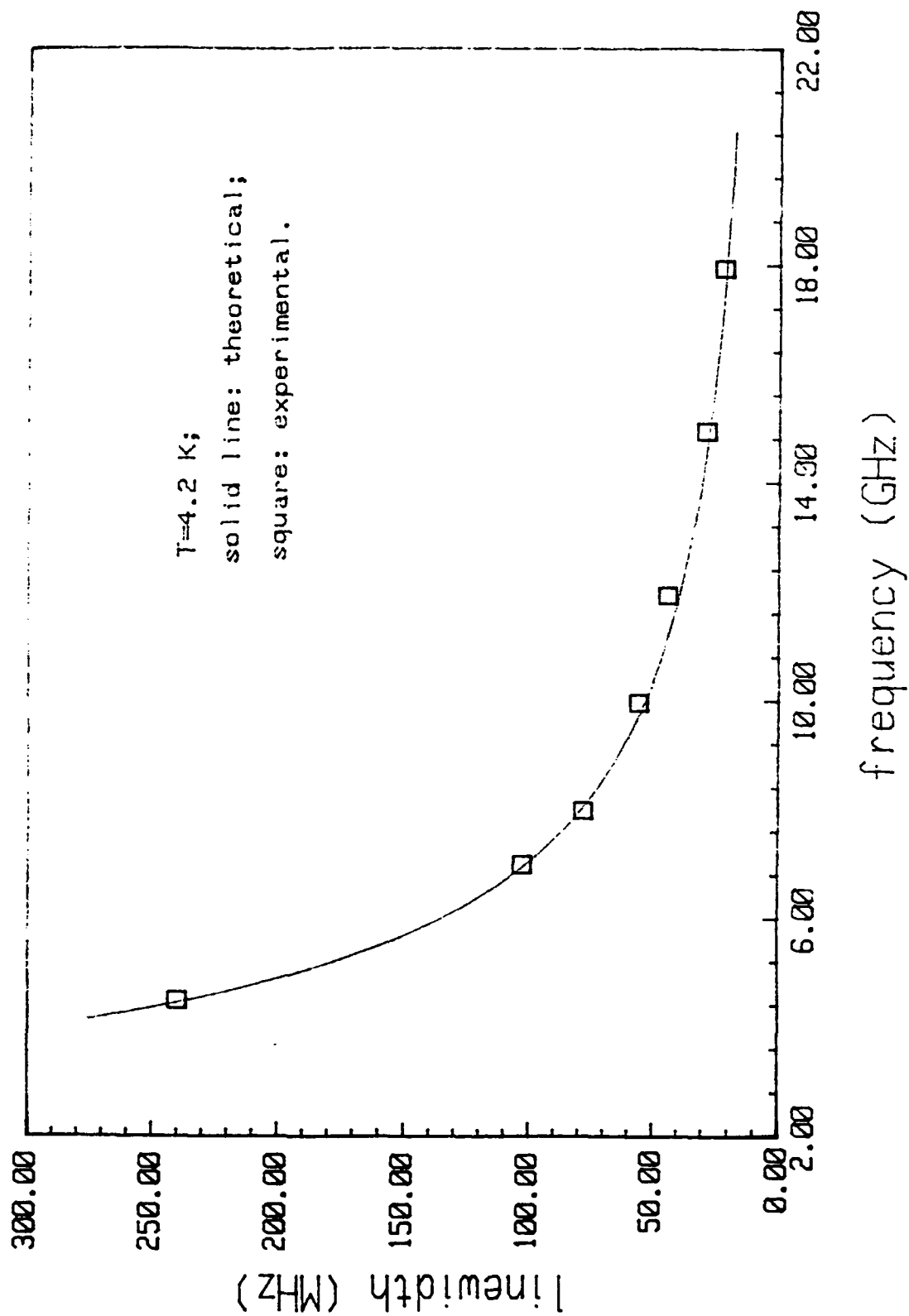
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Figure 7

The linewidth of the radiation from the detector junction (array off) — squares vs. frequency as measured by the spectrum analyzer. Predicted linewidth from RSJ model is shown as the solid curve.

thermal instabilities which caused frequency jumping in the array. This problem could be fixed by cooling the array below the lambda point where the thermal conductivity of helium is much greater. A more satisfactory fix for the future will likely be either to series bias the array (with much lower current) or to bond superconducting leads to the pads.

The most interesting results from this sample were the measurements of tuning speed. Data could be obtained in the 15 - 18 GHz frequency range. The lower limit was set by the minimum operating frequency of the array (again the I_cR_J product was higher than the design value) and the upper limit by our spectrum analyzer. Although these measurements are preliminary, they set very encouraging lower limits on the tuning speed of the arrays. Two basic types of measurements were made: First, the bias current through the array was abruptly switched from the zero voltage to the finite voltage state and the rise time for the power output was measured. Second, a sinusoidal current modulation was added to the array bias to modulate the operating frequency between 15 and 18 GHz. The maximum modulation frequency for which the array output would track the bias was determined.

Figure 8 shows, schematically, the setup for measuring the turn on time of the array. A square wave bias modulation is applied through the coaxial cable and the output power detected after amplification by a 6 - 18 GHz amplifier. Figure 8 also shows the detected power vs. time during this modulation. As can be seen, the rise time is a fraction of a microsecond. It is quite possible that this is due to the electronics, so further testing is required to determine the intrinsic turn on time of the array.

The second test consisted of applying a sinusoidal bias modulation to the array in its on state. The bias was alternately applied through the coaxial cable and the bias tree. For low frequencies, in the kilohertz range, we observe (for averaging times long compared to the modulation frequency) a broad spectrum of radiation from the modulated array. Typical results are shown in Fig. 9. The bandwidth of this radiation is
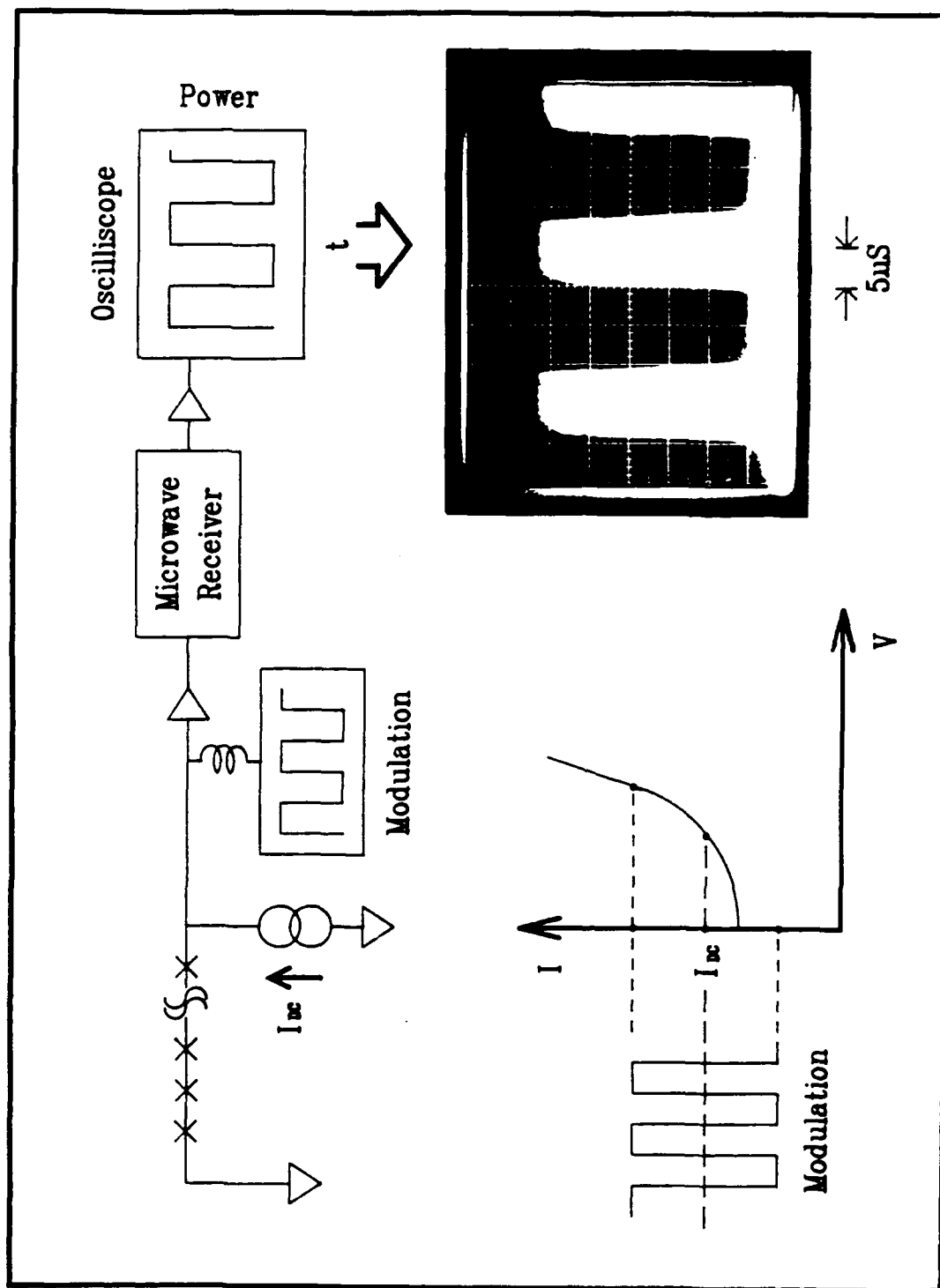
31

Figure 8

Rise time of power when the array is switched from off to operating state showing the schematic of measurement circuit and bias current modulation and the detected power vs. time as bias current is switched at 50 kHz.

modulation frquency: 1000 Hz;
solid line: measured;
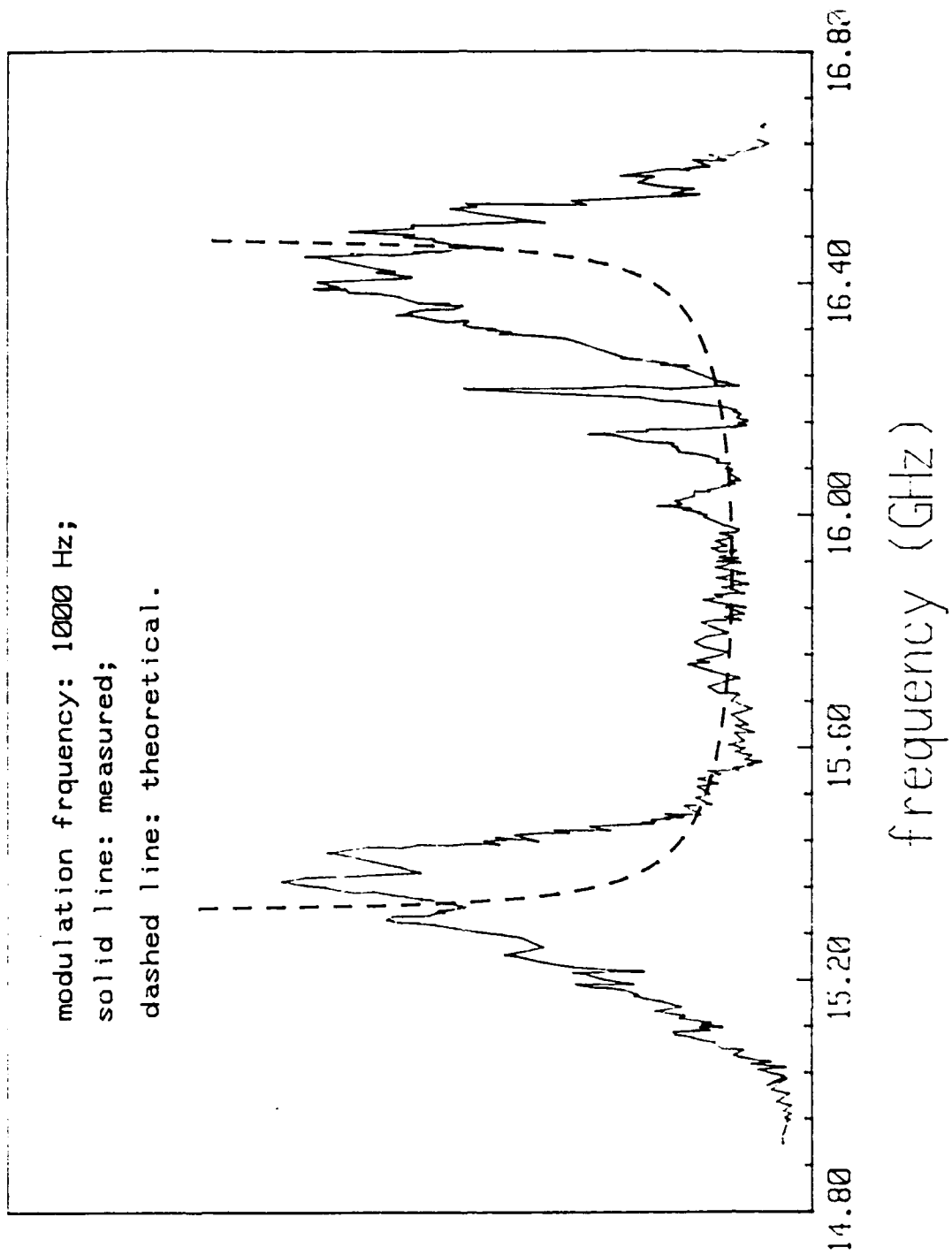dashed line: theoretical.

frequency (GHz)

power spectrum density (arb.)

Figure 9

Power spectral density from array modulated by a lower frequency sine wave.

proportional to the modulation amplitude, and its spectral density is proportional to the inverse time derivative of the sine wave. For higher frequencies, in the megahertz range, a series of side bands separated by the modulation frequency are observed. Typical high frequency modulation results are shown in Fig. 10 for a modulation frequency of 500 MHz. While these data were obtained coupling the bias current through the bias tree, similar results have been obtained coupling the modulation current through the coaxial cable. The success of this later modulation scheme is somewhat surprising, and more study is needed to understand just how it is working.

These results clearly represent lower limits to the tuning speeds attainable in Josephson effect sources. Even with these imperfect arrays, the measured rates may well be limited by the measurement techniques used. One would expect even faster rates for series biased array using more uniform junctions, since no redistribution of bias current among the junction would take place during tuning. The theoretical (or experimental) upper limit for the tuning rate in the presence of attainable parameter scatter is not known. This is certainly an area that deserves much more study. It seems likely that the tuning rate for Josephson effect sources can far exceed that attainable with semiconductor sources.
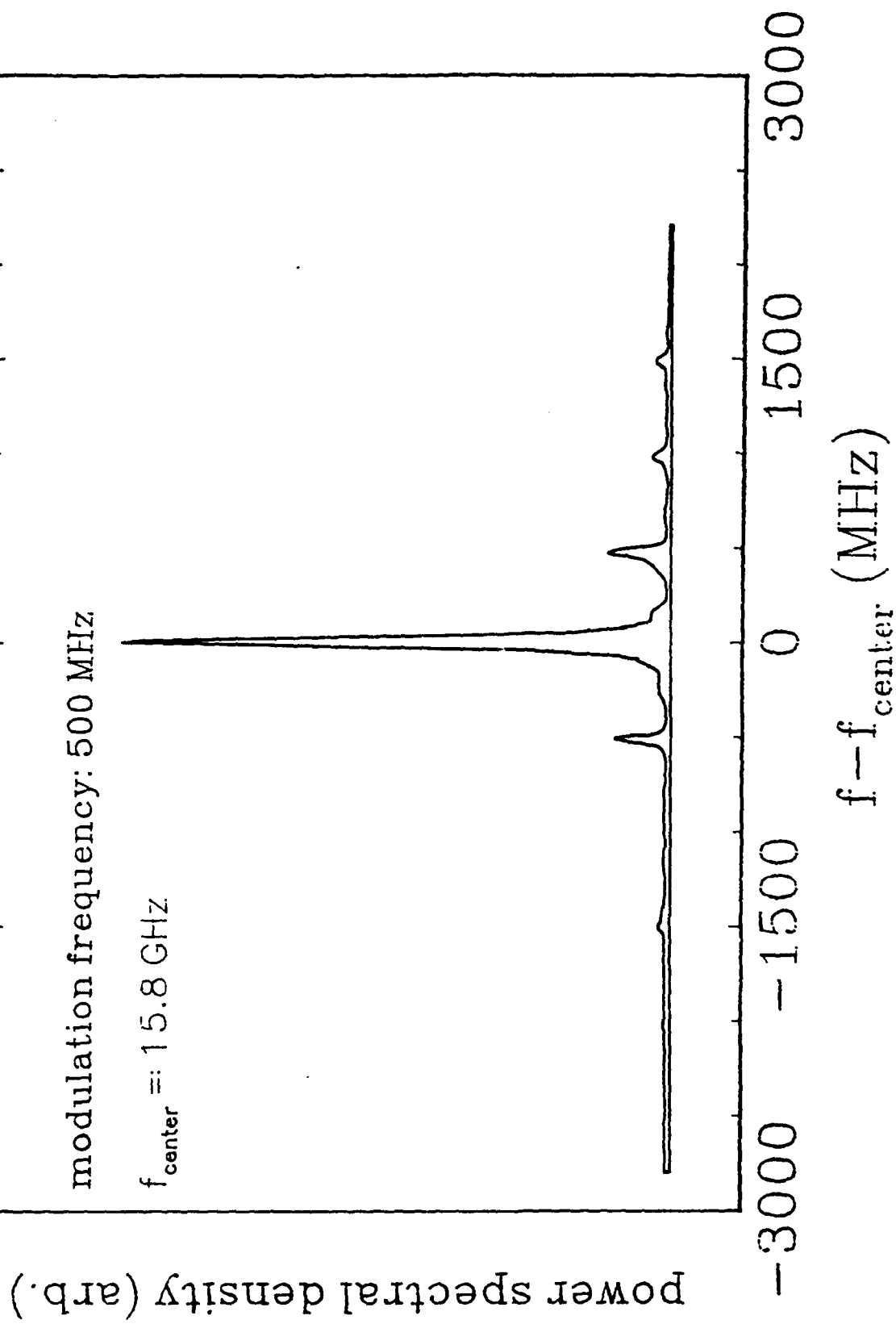
Figure 10

Power spectral density from array with bias modulated at 500 MHz. Side bands separated by 500 MHz are seen.

The plot is labeled: modulation frequency: 500 MHz, $f_{center} = 15.8$ GHz, with axes $f - f_{center}$ (MHz) and power spectral density (arb.)

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Technical Report 3

DESIGN AND EVALUATION OF A JOSEPHSON ARRAY OSCILLATOR

by

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ABSTRACT

The report describes the design and measured performance of a superconducting Josephson array oscillator. An array of Josephson junctions was fabricated to function as a 12 to 18-GHz frequency agile voltage controlled oscillator for application in analog-to-digital conversion. At a temperature of 4.2 K, measured peak RF power was approximately -84 dBm in a 300 kHz bandwidth. This work was performed in support of MITRE Sponsored Research project 91080, Superconducting Analog-to-Digital Converters.

EXECUTIVE SUMMARY

BACKGROUND

The MITRE sponsored research (MSR) initiative to investigate applications of superconductivity in technically challenging areas of application -- especially, analog-to-digital signal converters -- quickly focused on several subcomponent devices. Because of the generally recognized precise relationship of the Josephson junction oscillating frequency to the voltage across the junction, the group investigating the application elected to focus some of its attention on these devices as a converter component. We sought to understand how to effectively use these junctions with their inherent quantum precision in analog-to-digital converters. Initial analysis showed that individual junctions were impractical; their individual power and impedance levels tended to be too low (fractions of picowatts and ohms, respectively); and their output bandwidth too large.

INVESTIGATION STRATEGY

MITRE chose to investigate arrays of Josephson junctions, teaming with a physics department research group at the State University of New York at Stony Brook (SUNY). MITRE investigators explained our system problem to physicists there, who for several years had worked on stabilizing arrays of junctions. Meanwhile, we developed a cryogenic laboratory capability to be able to make performance measurements on superconductor devices.

ANALYSIS

When our preliminary models suggested promising application possibilities for the superconducting A/D converter (SADC) application, we asked SUNY for design and fabrication support. They created improved designs and fabricated custom lithographic array patterns. They made working oscillator devices, measured performance of them first, and then supplied several working oscillators to MITRE.

EVALUATION RESULTS

The concept of the array as a controlled and coherent oscillator has been demonstrated, with output in the desired frequency range. MITRE's measurement of power output indicated less than ideal power output and the report covers possible reasons for this. Nevertheless, the oscillators work. In addition, SUNY has recently measured the agility of their devices to shift output frequencies (by rapidly modulating the driving bias) while operating at a frequency in the 12 to 18-GHz range and believes the device's frequency agility is better than that of any other known device type in this regard.

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SECTION 1

DIGITAL CONVERTERS AND SUPERCONDUCTOR DRIVERS

The MITRE research project to investigate ways of converting analog voltage signals into digital format -- analog-to-digital conversion -- included a program to investigate superconductor components of a converter design. This paper reports on the design and evaluation of a superconductive voltage-controlled oscillator (VCO) as an essential component of a superconducting analog-to-digital converter.

1.1 SUPERCONDUCTING ANALOG-TO-DIGITAL CONVERTERS

The overall architecture of a concept for a superconducting analog-to-digital converter (SADC) as devised by The MITRE Corporation has been described by Schoen [1]. The operational goal of the design is 16-bit precision with a sampling rate of 5 megahertz. The preliminary account of this work includes mathematical models of performance and implementation studies. The MITRE SADC architecture is built upon use of residue number principles: it postulates rapid conversion of analog voltage data into precise frequency data, with multi-channel decomposition of these data through signal phase resolution. As such, frequency and phase precision requirements are equivalent to a system precision of 1 part in 2^{16} and, thus, demand frequency precision $\Delta\omega/\omega \sim 2 \times 10^{-5}$.

1.2 VOLTAGE CONTROLLED OSCILLATORS

Precise conversion of signal information to frequency and the phase information can be accomplished using superconducting Josephson junctions. In following sections, we report design considerations for arrays of Josephson junctions configured as a drive source for a SADC. The design discussion shows some of the options to both increase the output power and reduce the output bandwidth of a VCO array. The report continues with our evaluation measurement results and conclusions. A preliminary account [2] of MITRE design considerations for an SADC VCO has appeared as part of reference 1; and Section 2 is based upon it.

The Josephson-junction array VCO source is the key component of the SADC. There are additional superconducting components in the frequency discriminator unit which electrically follows the VCO, and this frequency discriminator is introduced in the design section. Details of the MITRE frequency discriminator and its subcomponents have been described previously [3] and are outside the scope of this report on the design and evaluation of a superconducting VCO for a specific SADC architecture. The evaluation section describes the test of a typical superconducting VCO. In addition to the present investigation of VCO use, phase-locked arrays of Josephson junctions may offer new superconducting electronics design capabilities outside the present focus on SADC applications. If Josephson junctions

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arrays can be controllably engineered and then fabricated, they may offer new possibilities in communication systems design as frequency-agile, precise submillimeter wavelength radiation sources.

SECTION 2

DESIGN CONSIDERATIONS

The main disadvantage of a single Josephson junction as a source in an SADC is low-power output. Adequate power is needed to pass through a delay line(s) and drive one or more phase-detecting mixers. In the absence of firm requirements for the mixers and delay lines, a goal of 10 nW of oscillator output power is desirable. This power level is far in excess of single junction output levels in the picowatt range. In addition, there are impedance mismatch concerns associated with matching the intrinsically low impedance single junction oscillator with transmission lines used for delay. For example, if the mean converter output frequency is 15 GHz, a single shunted junction circuit will tend to have an impedance on the order of only 0.01 to 0.1 ohm. A series array of N junctions can exhibit the phase locked constructive interference of N oscillators with array output power increasing as N^2. Such array characteristics have been verified. Jain, *et al.* [4] show the result of a study of arrays with various numbers of junctions in series and operating at 10 GHz. Their array with 99 junctions achieved an output power of about 5 nW into 50 ohms. For comparison, the single junction output was measured to be about 0.5 pW, which is about two percent of the theoretical matched output of the individual junctions given by $I_c^2 R_n/8 \sim 20$ pW, where I_c is the junction critical current and R_n is the normal-state resistance of a junction.

Another SADC requirement is the need for spectral purity in the VCO. For the MITRE SADC discussed in this report, phase precision requirements equivalent to one part in 2^{16} imply output frequencies must be within the range $\Delta\omega$ given by $\Delta\omega/\omega < 2 \times 10^{-5}$. This is a severe requirement. An analysis by Likharev [5] of thermal noise fluctuations yields a bandwidth that is proportional to both the temperature and the resistance of a single junction. This is a minimum which is increased by other possible noise sources, including $1/f$ noise, for example. According to Likharev, the width at 4 K is 160 MHz per ohm of source resistance. At a frequency of 10^{10} Hz and assuming $R_n \sim 0.01$ ohm, the linewidth associated with a single junction would be $\sim 2 \times 10^8$ Hz. If an array configuration is used, then theoretically this linewidth should be reduced by $1/N$, so that, for $N = 200$, $\Delta\omega/\omega \sim 1 \times 10^{-4}$. Although the linewidth of this particular example is higher than the requirement by nearly one order of magnitude, Jain, *et al.* [4] show that additional shunt resistance will narrow the linewidth.

The critical issue for the desired coherent operation of an array is phase locking. A Josephson junction array will comprise an ensemble of similar but not identical junctions, each hosted in a similar but not identical local environment. A tendency toward incoherent radiation with a distribution of frequencies may be countered by the presence of a judicious locking current. Conditions for phase locking have been investigated theoretically and performance of phase locked arrays has been the subject of significant activity. Empirical information is still used, however, and some investigators [4] report anomalous behavior

with, for example, only 15 percent of the junctions in an array exhibiting mutually locked behavior.

During this investigation, MITRE made progress in analyzing coherent oscillation of Josephson junctions. We have worked on useful designs [3] that generally fit the project requirements. We have selected component layouts that seem realizable and consistent with physical limitations. For example, although we would prefer a large number of junctions ($N \sim 10^3$) to increase output power and improve VCO linewidth, we are restricted by foundry design rules and coherent phase requirements. The need to have all the junctions driven in phase even at the highest frequency (about 20 GHz for the converter) requires all the N junctions to be within approximately one-tenth of a wavelength at this highest frequency after taking into account the somewhat retarded speed of propagation on the junction substrate. Sets of practical values of inductance, capacitance, and resistance have been generated and analyzed by various computer routines. Although earlier accounts of MITRE analysis work on practical designs suited for SADC applications have appeared [1, 2], the MITRE analysis of candidate VCO array designs is reviewed in this section. Because part of the MITRE investigation plan included cooperating with Prof. J. E. Lukens of SUNY to fabricate and evaluate basic VCO designs, the SUNY design practices and parameter expectations were significant. In the remainder of this section, we review some of our basic VCO designs, some improvements suggested by SUNY to improve output stability and some limitations of VCOs with regard to SADC use. After we had made some initial studies based on 20 GHz as an upper frequency and reviewed in section 2.2 below, we made a decision to shift the planned operating range to 9 to 18 GHz. The reduction of the upper frequency allowed use of lower cost evaluation fixtures with no expected loss of generality in evaluation outcomes.

2.1 BASIC DESIGN

To provide a focus of analytical capability, we initiated a design of a suitable test article for the SADC project to test one critical component, the VCO. As an initial design of a VCO test device, we analyzed the design outlined in figures 1 through 3 and the text below. Based on relations given by Jain, *et al.* [4], the estimate of the output power at 10 GHz is 0.16 µW (-38 dBm).

The overview of the basic design is shown in figure 1. It shows a sample array of 200 junctions configured with 50-ohm input and output impedances. The important controlling parameters of the array are listed in table 1. Table 2 shows the predicted performance parameters of the array. The design focus is on measurability first and optimal operation second. The concept of the design is to provide a testable component having projected operating characteristics that appear to support the SADC architecture applications. Thus, the derived array operating characteristics shown in table 2 seem to be generally compatible with SADC use. Integration of the VCO component, however, with a sample-and-hold amplifier input and a superconducting delay line output would require modification of the design [1].
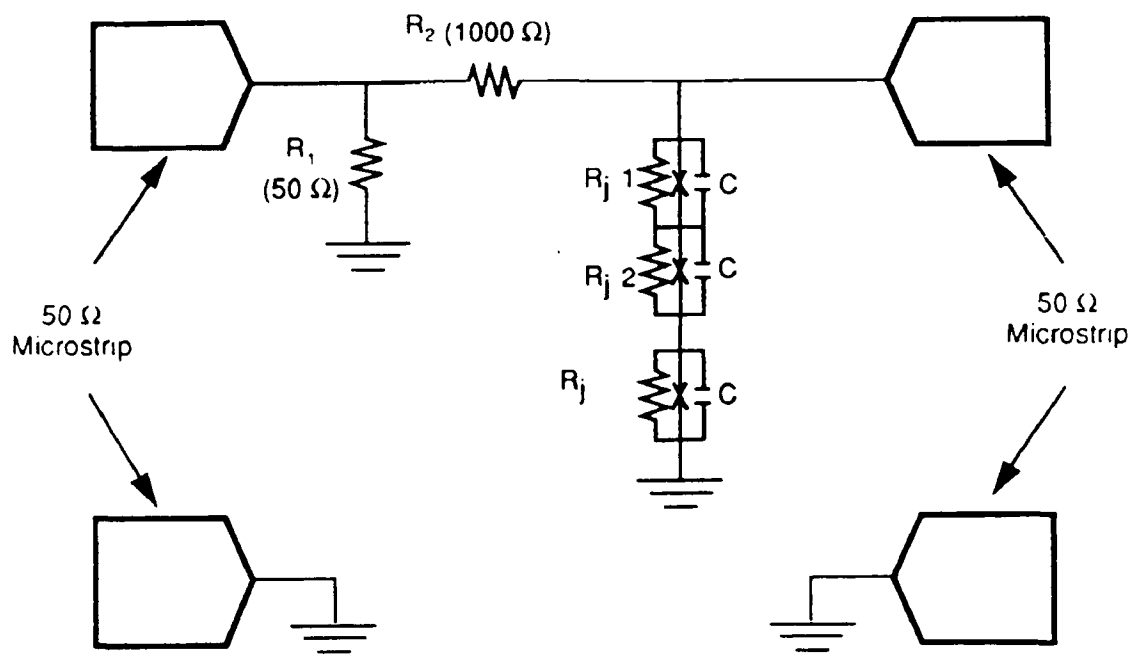
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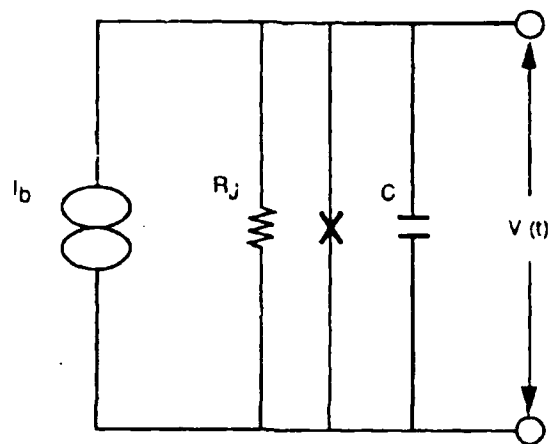Figure 1. Schematic Diagram of the Josephson VCO Array

Figure 2. Equivalent Circuit of a Single Junction Unit

Figure 1 shows the array input and output; as well as, the overall circuit schematic of a 200-junction array. Figure 2 shows the single junction unit cell that is replicated through the array. The bias current I_b flows through this unit and the voltage $V(t)$ develops across it. The time average of this voltage $\overline{V}$ determines the frequency f of junction oscillation: $f = (2e/h)\overline{V}$. The over-bar symbol indicates an average over time that is long with respect to the oscillation period.

The array may be treated as a lumped element providing that the phase difference across its external points is small. This condition limits the array size. The usual criterion [4-6] for
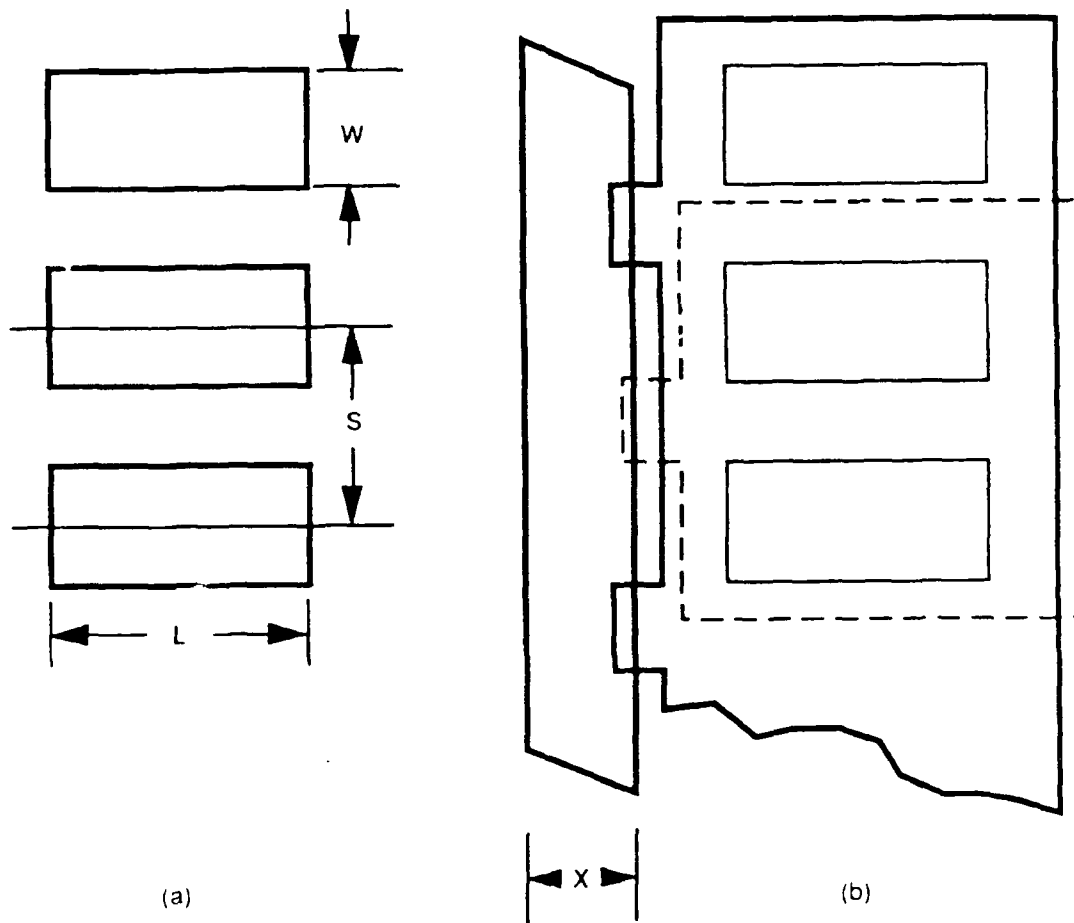

Figure 3. Concept of the Array Pattern. (a) Junction layout with $W = 3$ μm, $L = 6$ μm, $S = 6$ μm, (b) Normal metal shunt of 1 μm thickness with width $x \sim 3$ μm and path length(s) ~ 6 μm based on a resistivity of 0.5 μΩ-cm

Table 1. Array Configuration Specification of a 200-Junction Array

Parameter	Value
Junction width FF [a]	3 μm
Junction length L	6 μm
Junction spacing S [a]	6 μm
Junction critical current I_c [b]	1.8 mA
Junction shunt resistance R_j [c]	0.010 ohm
Number of Junctions N [d]	200
Junction capacitance C [e]	0.81 pF

[a] minimum width and spacing (pitch) according to Hypres [7].

[b] $(10^4 \text{ A/cm}^2)\ W\,L$.

[c] Approximate value so that $1.7\ I_c R_j/\Phi_o \sim 15$ GHz.

[d] $N = \dfrac{10^8 \text{ m/s}}{4S(20\,\text{GHz})}$.

[e] $C = \left[45\ \text{fF}(\mu\text{m})^{-2}\right]WL$

Table 2. Array Operating Parameters of a 200-Junction Array

Parameter	Value
Reduced current i [a]	[1.52, 2.50]
Operating range of junction current I_b [b] (mA) @ $10 \leq f$ (GHz) ≤ 20	[2.74, 4.5]
Operating range of array input current I_o [c] (mA) @ $10 \leq f$ (GHz) ≤ 20	[55,90]
Bias power to 200 junctions, P_{bias} [d] (μW)	[15,41]
β_c [e]	0.0004
Output frequency f_o [f] (GHz)	[10,20][h]
Linewidth $\Delta\omega/\omega$ [g]	[4.2 x 10^{-7}, 4.9 x 10^{-7}]
Output power P_A [h] (μW)	0.16

[a] i is the reduced current such that $I_c R_j \sqrt{i^2 - 1}/\Phi_o = 10$ or 20 GHz,

[b] $I_b = i\, I_c$,

[c] $I_o = I_b\, (10^3$ ohm/50 ohm),

[d] $P_{bias} = N I_b{}^2 R_j$;

[e] $\beta_c = 2e I_c R_j{}^2 C/h$,

[f] f_o to be determined from JSPICE for single junction shunted by R_j, C;

[g] $\Delta\omega/\omega = 2k_B T\omega/P_{bias}$ in accord with eq. 8.17 of Jain, *et al.* Physics Reports, Vol. 106, 1984,

[h] $P_A = [I_c{}^2\ (50$ ohm$)\ /2]\gamma^N$, where the γ $_N$-value of 0.002 is obtained from Figure 5-3 of Jain *et al.* (Ibid., pp. 405-6) with $N/N_{opt} = (200/5000) = 0.04$.

spatial limitations related to phase coherence limits the longest linear dimension S such that $S \leq \lambda/10$ where $\lambda \sim (c/4) \, (f_{max})^{-1}$ with c being the speed of light in vacuum and f_{max}, the highest frequency of operation. Phase velocities as low as $c/10$ may be possible according to the literature [4].

Minimum spacing of junctions depends on lithographic production limits. The minimum spacing S recommended by the Hypres Corporation for their niobium films is 6 μm [7]. This limit is consistent with SUNY practices [4,6], and this minimum is used in the pattern shown in figure 3. Figure 3(a) shows junctions as rectangles L by W. The dimensions used, 6 μm by 3 μm, yield a junction area of 1.8×10^{-11} m^2. The product of this area and the typically achievable [6] Josephson critical current density J_c of 10^4 A/cm^2 yields an expected tunneling critical current I_c of 1.8 mA. The junction capacitance value of 0.84 pF per junction is consistent with the same junction area and an assumed specific capacitance of 45 fF (μm)$^{-2}$. These values are summarized in table 2.

Figure 3(b) shows a concept for replication of resistively shunted junctions. The pattern shown could be produced by a stepped offset of the upper superconductor film on the lower, both having lateral tabs. The tabs are shown shunted by a normal metal film deposited onto the plane of junctions and over the superconductive tabs to form a line of shunt resistors somewhat displaced from the line of Josephson junction centers.

Although the above pattern (figure 3(b)) concept is achievable, the self-inductance of the shunts is non-optimal. The estimated self inductance of each junction shunt is about 1 pH. The effect is to introduce systematic error into the predictions of array performance (table 2), especially at the higher operating frequencies. Instead of this pattern, investigators at SUNY use an underlying shunt resistance film. Sauvageau [6] shows one example of the SUNY-type of low inductance shunted junction having an effective inductance of 0.1 pH or less.

As referenced in [2] in the section on error analysis, the voltage-to-frequency conversion in the subject superconducting VCOs deviates somewhat from an ideal linear proportion. The overall conversion of signal voltage at the 50-ohm input of the array to a frequency at its output is not a quantum ratio of 16-bit precision, but depends on resistance ratios, voltage fluctuations, etc. This conversion deviation is the result of using a current bias of the array, not a voltage bias. For example, based on the tabulated performance parameters in table 2, input voltages of 2.75 and 4.50 volts correspond to output frequencies of about 10 and 20 GHz, respectively. Equations[1] of Lukens, et al. [8] yield

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[1]   We use both the equation $f = (2e/h) \overline{V}$ and the relations $\overline{v} \equiv \overline{V}/V_c = (i^2 - 1)^{1/2}$, $i \equiv I_b/I_c$.

and $V_c \equiv I_c R_j$ associated with equation 2 in reference 7. Since the flux quantum Φ_o is

$$f_1 \approx I_b R_j \Phi_o \left[1 - \left(I_c / I_b \right)^2 \right]^{1/2}$$

(1)

where I_b is the bias current and R_j is the (shunted) junction resistance. Using the junction values of table 5-1 and letting $I_b \sim V_{in}/(1000 \text{ ohms})$, this conversion becomes

$$f_1 = K V_{in} \left[1 - \left(V^* / V_{in} \right)^2 \right]^{1/2}$$

(2)

where $K = R_j \Phi_o^{-1} (1000 \, \Omega)^{-1} = 4.84 \text{ GHz-V}^{-1}$ and $V^* = (1000 \text{ ohm}) I_c = 1.8\text{V}$. Also, I_b is the bias current, Φ_o is the flux quantum and V_{in} is the input voltage. In what follows in section 2, the current through the array is denoted I, and the bias notation is dropped.

2.2 JSPICE SIMULATIONS

MITRE performed JSPICE simulations to investigate single Josephson junction VCOs. JSPICE is a version of the popular SPICE 2G circuit simulation program which features an embedded Josephson junction model. JSPICE represents an important tool for the design of subsystems of the superconducting analog-to-digital converter. This section describes initial conditions in JSPICE, typical JSPICE simulation results and a discussion of these results.

The Josephson junction model implemented in JSPICE is known in the literature as the resistively shunted junction (RSJ) model [4,5]. The RSJ model includes an ideal Josephson junction in parallel with the junction capacitance and a voltage dependent shunt resistance, as depicted by the equivalent circuit shown in figure 4 (The Josephson RSJ model is between node 1 and ground, and is treated by JSPICE as a single device.) The ideal Josephson junction obeys the Josephson relations and accounts for Cooper pairs (the superconducting electrons) tunneling through the junction, while the voltage-dependent resistance represents the quasiparticle (single "normal" electron) tunneling current. JSPICE requires that the initial conditions of a Josephson junction be declared, which include the junction phase, ϕ and the junction voltage, V_j. It is appropriate to uniquely specify only one of these parameters, with the other set to zero. Which parameter is specified depends on the initial voltage state (zero or finite) of the Josephson junction.

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equal to $h/2e$, we can write $f = \Phi_o^{-1} \overline{V}$ and recognize $\overline{V} = I_c R_j \left[\left(I_b / I_c \right)^2 - 1 \right]^{1/2}$, so that

$$f = R_j I_b \Phi_o \left[1 - \left(I_c / I_b \right)^2 \right]^{1/2}.$$
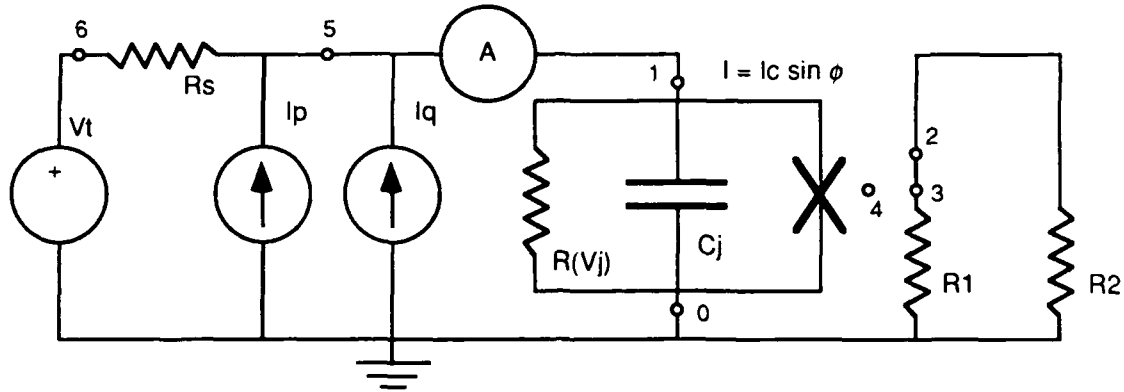
Figure 4. Josephson Junction Voltage Controlled Oscillator

The zero voltage state of the Josephson junction implies that the current through the junction does not exceed the junction's critical current. In this case the junction phase should be specified, which is given by the Josephson current-phase relation [9] shown here in the alternate form

$$\phi = \arcsin\left(\frac{I_c}{I}\right)$$

(3)

where I is the current through the junction.

A finite junction voltage specified as an initial condition implies that the junction phase difference is increasing with time as given by the Josephson voltage-phase relation [10]

$$\frac{\partial \phi}{\partial t} = \left(\frac{2e}{\hbar}\right) V_j$$

(4)

In other words, if a constant voltage is applied to the junction, integration of equation (4) shows that

$$\phi = \phi_o + \left(\frac{2e}{\hbar}\right) V_j\, t$$

(5)

where ϕ_o is an initial phase. Substitution of this result into equation (5-3) yields

$$I = I_c \sin(\omega jt + \phi_o)$$

(6)

where

$$\omega_j = \left(\frac{2e}{\hbar}\right)V_j$$

(7)

Thus, an applied voltage on a Josephson junction causes an AC current oscillation through the junction, a phenomenon known as the AC-Josephson effect. The Josephson AC current oscillations will be partially shunted by the junction capacitance and (more importantly) the junction resistance thereby causing the junction voltage to oscillate at a frequency of

$$f = \left(\frac{1}{2\pi}\right)\left(\frac{2e}{\hbar}\right)\bar{V}_j \cong (483 \text{ MHz/mV})\bar{V}_j$$

(8)

which is the fundamental voltage-to-frequency relationship which we are exploiting in our analog-to-digital converter architecture. Therefore, an initial condition specification of finite junction voltage causes Josephson AC current/voltage oscillations from time $t = 0$. This condition does not necessarily imply that the junction current exceeds I_c, although if $I < I_c$ the junction voltage oscillations may die out if the junction and its external circuit provide sufficient damping.

If the initial state of a junction is not obvious from the circuit topology, a preliminary simulation with both ϕ and V_j set to zero and all sources set to their quiescent values can provide the initial state of the junction(s). The Josephson junction will rapidly (within 200 ps) converge to its quiescent state, which can be determined by monitoring the node voltages of the circuit. The junction phase is brought out to a dummy node labeled *NPHI* within JSPICE

A Josephson VCO circuit was investigated to establish a correlation between the JSPICE simulation program and ACSL simulation programs separately run at MITRE and described elsewhere [1], additionally, this investigation illustrated an important use of initial conditions in JSPICE. Figure 4 shows the Josephson junction VCO circuit model simulated using the JSPICE program. JSPICE incorporates a quasiparticle resistance model containing a Fermi-like function for the resistance transition between the minimum resistance and the normal state resistance of the junction as the the junction voltage approaches and then exceeds the gap voltage; accordingly, in our modeling, we set the JSPICE variable *RTYPE*=2 as discussed by Jewett [11]. The current which flows in the short between nodes 2 and 3 can be used to modulate the critical current; thereby, modeling the effect of magnetic field on the Josephson junction. This modulation option was not used in the simulations presented here, and therefore nodes 2 and 3 were simply connected to ground via 1-kilohm resistors while the JSPICE control current type parameter *CCT* was set to zero. Node 4 is the dummy phase node *NPHI* referenced above, which cannot be connected to any actual circuit element. The current sources I_q and I_p are the DC bias current and preconditioning current pulse sources, respectively. In the following simulations I_q was set to 99 μA. The test input voltage was represented by the voltage source V_t with source resistance R_s, where R_s had a value of 10 kΩ. All of the following simulations were performed using the JSPICE program running

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on a VAX 2000 workstation under the VMS operating system. Additionally, identical results were obtained using JSPICE on the MITRE UNIX VAX machines.

Figure 5 depicts the junction voltage as a function of time where the junction was initially biased with the DC current I_q, $\phi = 1.4293$ rad, and $V_j = 0$. At time $t = 10$ ps the junction was pulsed with a 1 ps duration current pulse of 23.5 μA magnitude, and 1 ps rise and fall times. Beyond approximately 60 ps the peak value of the junction voltage was ~1.022 mV. A Fourier analysis performed on the waveform showed the junction voltage to be oscillating at a fundamental frequency of 476.0 GHz with a total harmonic distortion of 0.52 percent. Thus, the frequency spectrum of this Josephson VCO circuit is relatively monochromatic.

The simulations presented in figures 5 and 6 depict the response of the Josephson junction VCO to a step input current waveform. The input current waveform is the sum of the DC bias current and the current from the test voltage source V_t with its associated series resistance R_s. In the simulation, the junction was DC biased at 99 μA with initial conditions of $\phi = 0$ and $V_j = 1.022$ mV. Note in figure 6 at time $t = 0$ that the junction voltage is oscillating in the same manner as it was in figure 5 at time $t = 200$ ps, a manifestation of the junction initial conditions. The use of initial conditions provides the Josephson oscillations at the beginning of the simulation, allowing us to eliminate the preconditioning current pulse and its transient response. This allows the simulations to focus on the desired VCO behavior, where the voltage oscillations are sensitive to perturbation by the external voltage V_t.

2.3 OSCILLATOR PHASE LOCKING

The essence of the VCO multi-junction array is the coherent oscillation of all or almost all of its individual oscillators. The principal fault of the 200-junction array of table 1 is that its output may fail to lock coherently. The conditions for coherent output of multiple-junction arrays depends on several parameters. Hadley et al. [12] have examined the intrinsic stability of an array of junctions with respect to both the bias current and the junction beta parameter β_c. The β_c-value (where $\beta_c = 2eI_cR_j^2C/h$) of our test design is only 0.0004 and, thus, barely in the range where [12] predicts some measure of coherence. And thus, the (β_c, I_b)-values are far from their optimal range. Reference 12 recommends a β_c of between 0.5 and 1.0 as well as a reduced current bias, the ratio of applied bias current I_b to critical current I_c, in the range of 2 to 2.5. But values of I_c, R_j and C are, however, not independent of (a) each other, (b) operating frequency constraints, and (c) chip and physical dimensional constraints. The main risk is that production variation in values of I_c (and C) and R_j from junction to junction will not support coherent oscillation of the junctions of the array.

With the greater insight gained by study of the array of table 1, we have considered some modifications to enhance its stability. According to Jain et al. [4], the physical effect that is central to phase locking is the constructive interference of the array current components with the high frequency (hf) circuit currents as if the latter were independent perturbing currents. We assume the array to be phase locked and focus on a single junction. We consider the
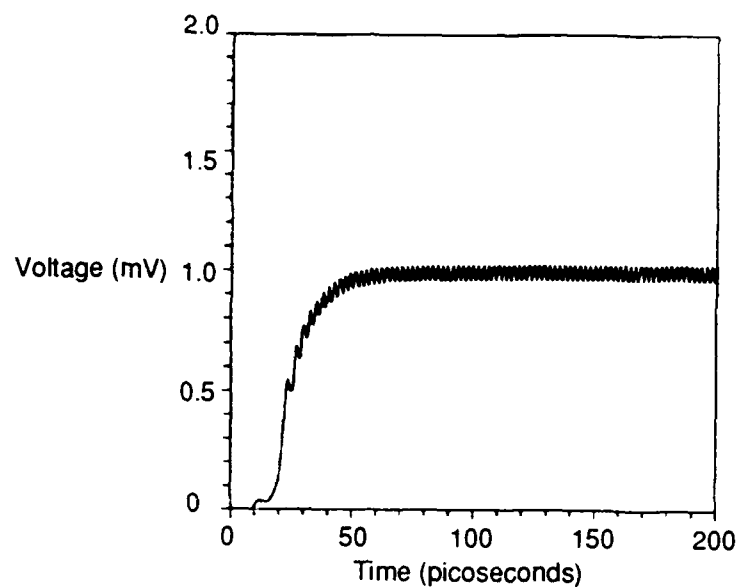
Figure 5. Voltage Response as a Function of Time for a Josephson Junction to a Static Bias and a Conditioning Pulse ($V_t = 0$)
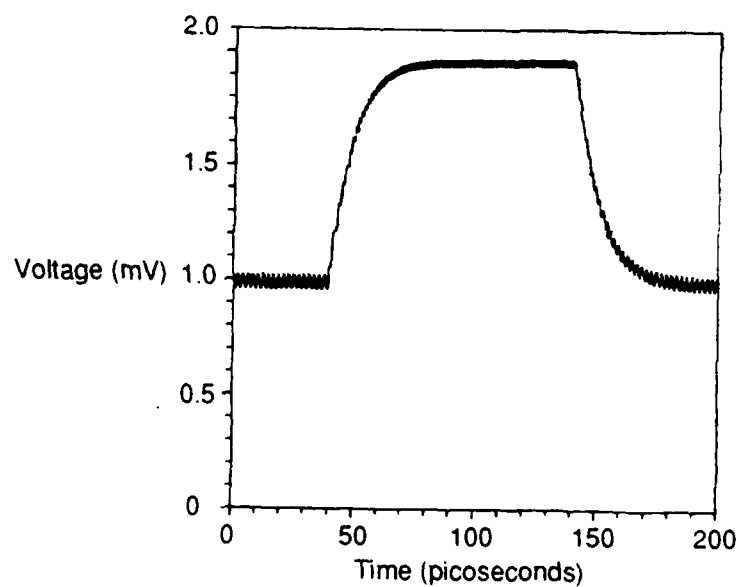

Figure 6. Voltage Response as a Function of Time for a Josephson Junction to a Positive Current Step (Current Bias $< I_c$)

possible small phase variation between that junction current in phase with its source emf but with both (1) current leading voltage in accord with the resistively shunted junction that includes junction capacitance, and (2) perturbed by the locking current flowing through the array and the rest of the hf circuit in its entirety. Inductive feedback shunting the array can complement the effect of junction capacitances within the array which, by the figure of merit of [12], are vanishingly small. While some inductance benefits phase locking by producing a negative phase locking angle p_l, too much hf circuit reactance is undesirable. Notably, increased hf inductance reduces both the magnitude of the locking current in the single junction and the available output power in the load. Reference 4 normalizes the comparison of a single junction reactance to that of the entire hf circuit by introducing a normalized (hf circuit) impedance z_c. It consists of the ratio of the impedance of the hf circuit to the resistance of the array. In a sense, this formulation amounts to a mean apportionment of the finite output impedance. This approach is expanded below to the case of the simple array (table 1) studied in [5] but with the addition of an inductive load. Following reference 4, we observe that variations in local parameters -- for example, currents controlled by shunting resistance and critical current -- can be inversely viewed as the ideal with the rest of the array currents as the amount of variation that can be tolerated while maintaining phase locking of all N quasi-independent sources in the array.

Our preliminary analysis showed the effect of including a finite inductance and then optimized inductance as part of the output impedance, an inclusion which should improve the phase-locking stability of the driving oscillator of the superconducting digital converter proposed by MITRE [1, 2]. Additionally, we analyzed a change of the output stripline/ microstrip from 50 to 2 ohms. This preliminary optimization study concluded that the 200-junction array may require an impedance-matching stripline if the output signal is to provide detectable input levels to room temperature instruments with 50-ohm inputs such as a spectrum analyzer or oscilloscope. Our preliminary study considered three perturbations to the circuit shown in figure 1. All three had to do with changing the output impedance seen by the array. These include (1) adding a feasible and, possibly minimal, series inductance L_s; (2) optimizing L_s for maximum phase locking; and (3) changing the resistive component R_l of the output impedance to better match the intrinsic impedance of the array, that array impedance being 2 ohms in table 2. Lukens et al. [8] point out the effects of inductance in the high frequency circuit is to phase delay currents with, possibly, beneficial results. We somewhat arbitrarily choose L_s =100 pH as a realistic minimum inductance in series with the output and calculate the phase locking stability factor $\delta I/I_L$. The inductance value of 100 pH is realizable in small-dimension circuits appropriate to coupling the array to a microstrip output. For reference, a loop consisting of a 3-μm conductor far from a ground plane and comprising a 1200-μm by 6-μm rectangle has an inductance on the order of 1 nH. This value would be reduced if the inductive loop is near to a conducting ground plane.

Estimates below on the effects of finite inductance in the output circuit are based on the frequency of 15 GHz, the center frequency of the VCO band. Figure 7 shows the high-frequency (output) portion of the array of table 1 and figure 1 as discussed above but
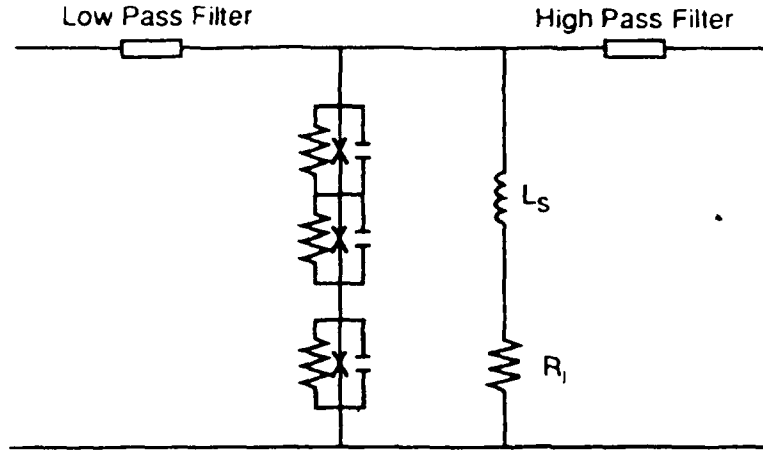
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Figure 7. Schematic Diagram of an Inductively Shunted Josephson Array VCO

modified by an added inductance L_s. Computing the array's normalized impedance z_c [Eq. 16b, ref. 8] by

$$z_c = \left(1/NR_j \right) \left(NR_j + R_l + i\omega L_s \right),$$

(9)

yields $z_c = 26 \, (1 + 0.181 \, i)$, and the locking phase angle p_l from [eq. 17, ref. 8]

$$p_l = \tan^{-1} \left[-\text{Im}(z_c) / \text{Re}(z_c) \right],$$

(10)

obtaining $p_l = -0.18$ rad. Now the value of the (presumed) locked current I_L in the array is determined from the complex current $\bar{I}_l$ given by the ratio of the harmonic amplitude to the effective impedance as (eq. 16a of reference 8)

$$\bar{I}_l = \bar{V} / \left(R_j z_c \right).$$

(11)

The bias conditions determine the magnitude of the fundamental frequency amplitude $\bar{V}$. Using values of table 1, it can be shown that $\bar{V} = 13 \, \mu V$ at 15 GHz, and with $|z_c| = 26$ ohms and $R_j = 0.01$ ohm, $I_L = |I_e| = 0.049$ mA. The assumed distribution of locking current has a maximum deviation δI_k given by the largest deviation that will not perturb the locked oscillation, namely (eq.19 of reference 8)

$$\delta I_k \approx I_L \min\left\{[1 + \cos(p_l)], [1 - \cos(p_l)]\right\}$$

(12)

so that for the (L_s = 100 pH) case studied, δI_k = 0.79 μA.

Other cases were studied for other load conditions. The cases with predicted maximum allowed variation in locking current, and translated to maximum allowed critical current $\delta I_c/I_c$ by assuming the locking or biasing current is a factor of two greater than the critical current. These three cases are tabulated in table 3. The feature we observe is that maximum variations can be small, even thought the third case was optimized under certain conditions (based on the optimal inductance predicted by eq. 20 of reference 8) and is comparable to achievable variability limits in critical currents.

Table 3. Maximum Allowed $\delta I_c/I_c$ of the 200-Junction Array of Figure 1

R_l (ohm)	L_s (pH)	δI_k (μA)	$\delta I_c/I_c$ (%)
50	100	0.79	0.022
50	552	12.5	0.35
2	74	160	4.5

The above sensitivity analysis of phase locking of prototype VCO sources for driving converter circuits shows the sensitivity to critical current variation within an array. SUNY investigators are able to control critical currents across a given array to within about 3-percent of the mean critical current of that array. Individual junctions which fall outside the allowed range will not only fail to contribute to coherent output, but also will contribute to the noise in the output. Preliminary studies of phase locking of our prototype designs based on 50-junction arrays with strong inductive feedback suggested by SUNY [6] show that all junctions would lock at the center of output frequency range but as many as three junctions would become decoupled at the ends of the range. In our design, we had intended to couple the array output directly from (or in place of) the pure resistance element R_l in figure 7. However, SUNY observed that there is an advantage in extracting only a fraction (about 1/10 th) of the oscillator power through the high pass limiting filter (figure 7) and then into a high impedance microstrip transmission line leading to a detector or analyzer. Such a coupling allows the oscillator to be more independent of both frequency of the output and following stage loading effects. This coupling can be conveniently obtained by mismatching a 50-Ω output transmission line to a low characteristic impedance array with load resistor. For example, with respect to table 3, for an R_l of 2 Ω the maximum allowable $\delta I_c/I_c$ of 4.5%

provides a manufacturable array (recall that a 3% mean is achievable) for which a 50-Ω coupled line provides the desired loose coupling. The SUNY fabricated and MITRE characterized VCO array described later in section 3 was built using this principle.

2.4 VCO LIMITATIONS

In completing the latest version of a VCO design, we have made some preliminary observations about limitations of the design. We have mentioned the linewidth which, although acceptable in some applications, may be unacceptable in the MITRE converter. Second, we have shown that the VCO design is really a current bias design and the ratio of frequency output to voltage input is not a constant proportion but increases slightly with voltage over the conversion range. Third, the candidate design features a 50-ohm input more suited for experimental evaluation than practical application. Its use in a VCO to quantify a low level signal would necessitate a precision linear wideband preamplifier. Fourth, the candidate design features a high-impedance (50-ohm) output which may not be optimal for driving low-impedance delay line components of a converter, but this drawback is not significant. The above limitations and others related to the sensitivity of the design to parasitic reactances and unavoidable variations in both prescribed reactances and Josephson junction parameters is being investigated. MITRE analysts investigated the internal dynamics of VCOs related to conversion with the goal of mitigating the limitations cited or consequences of them [1]. In particular, Sauvageau [6] and other SUNY investigators have observed that the use of a stabilizing inductive feedback circuit as shown in Figure 7 both enhances oscillator stability and tends to decouple the oscillator from its following load.

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2.5 ASSOCIATED COMPONENTS

The purpose of designing an agile VCO of narrow band output is to serve as a source for the frequency discriminator of the A/D converter. The architecture of the analog-to-digital converter proposed by MITRE [1] requires a multiple channel frequency discriminator. Its precision depends on accurate resolution of signals whose frequency vary over an octave. In the MITRE SADC architecture [1], each channel resolves the frequency of the input signal with respect to a given basis consistent with residue number mathematics.

A schematic view of a frequency discriminator is shown as a block outline in figure 8. According to the design concept, the necessary high resolution may be obtained by using different phase delay followed by phase detection. The discriminator incorporates at least one differential superconducting delay line, a superconductor-insulator-superconductor (SIS) phase detector and a low-pass filter of the phase detector output. A more complete review is found in [3].
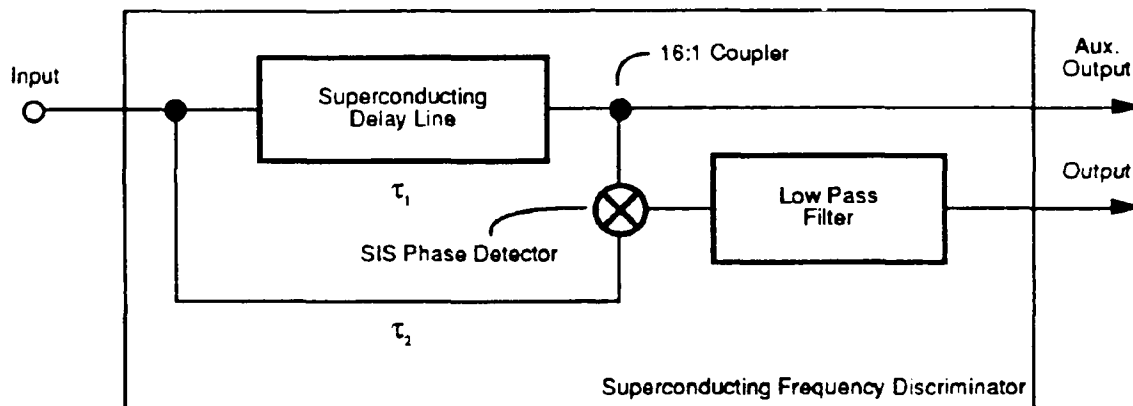
Figure 8. Block Diagram of the Superconducting Delay Line Frequency Discriminator

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SECTION 3

VCO EVALUATION

We have concluded a series of measurements on a superconducting voltage controlled oscillator fabricated by investigators at the State University of New York. The sample evaluated was typical of those produced for the investigation of the MITRE SADC architecture. This section describes the sample, measurement conditions and test results. MITRE and SUNY measurement correlation is discussed. The tests included characterizing the VCO output frequency and RF power level as a function of bias current, and a direct measurement of the junction shunt resistance (R_s). The insertion loss of the MITRE cryogenic probe and connecting cable was also measured. This section describes the sample, measurement conditions and test results.

3.1 SAMPLE DESCRIPTION

The VCO design, as fabricated by SUNY investigators, is an iteration of the MITRE design. Our preliminary work in the array design and its principle of operation, are described in sections 1 and 2; and in a prior account [2]. However, the fabricated arrays are different from the arrays MITRE analyzed. In particular, the fabricated arrays use only 65 junctions and an array microstrip terminated with a load and junction detector as described below. MITRE evaluated the typical superconducting VCO sample 20GHz-11G.

The following series of figures show the physical structure of the superconducting VCO array. Figure 9 depicts the overall VCO chip layout. Details of the area labeled "VCO Array" are shown in figure 10. Finally, figure 11 illustrates the "Array of Junctions" of figure 10. Included in figure 11 is a cross-sectional view of the Josephson junction array. Refering now to figure 10, drive current for the VCO array is applied through a parallel bias network as shown. Output oscillations from the VCO array are coupled from the 1-Ω array microstrip into a mismatched 50-Ω microstrip tapped on the incident power side of a terminating 1-Ω resistor. This mismatch is intended to limit the amount of coupled RF power, so as to not disturb the coherent oscillations of the array. The 50-Ω microstrip is transitioned to a 50-Ω coplanar waveguide, which can be connected to an SMA launcher in a cryogenic probe assembly. RF output power may be detected and measured on-chip by an integrated Josephson junction detector through observations of Shapiro steps in the detector junction's DC current-voltage relationship [13,14]. These steps are finite current offsets in the detector current whose magnitudes are proportional to applied RF power -- offsets which SUNY has observed but which we have not observed for reasons given later.

The characteristics which SUNY measured for the VCO sample 20GHz-11G are listed below in table 4. The RF power available from the 50-Ω coplanar waveguide was found to be a maximum of ~4 nW (-54 dBm) at a temperature of 4.2 K. This was measured with a
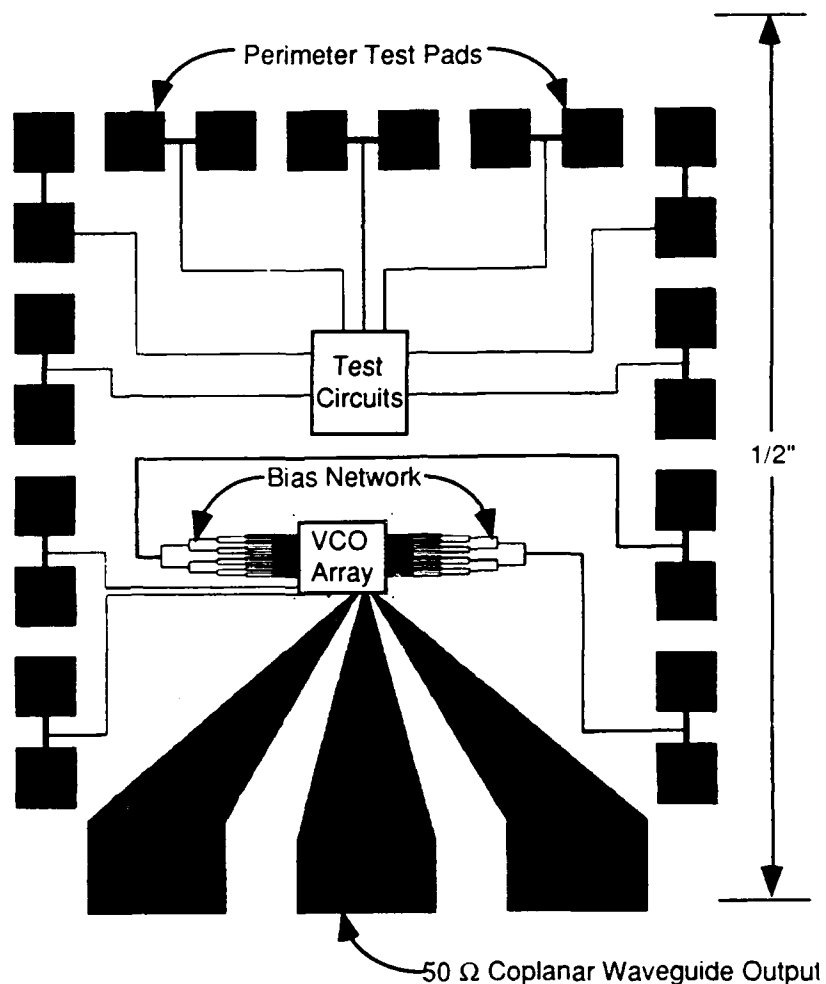
Figure 9. SUNY Superconducting VCO Chip Layout

bolometric power meter, which is broadband and has an advantage over a spectrum analyzer in that the technique is completely passive (i.e., well matched into 50 Ω without any spurious signals emanating from it). There is some concern that spurious power emission from a given spectrum analyzer's first local oscillator (LO) could be present at its input when it is used and thereby affect phase locking in the VCO array. SUNY reported that the output power variation with temperature (from 1.4 K to 4.2 K) was less than ten percent. However, the operation temperature strongly affects the output radiation bandwidth, which was determined by SUNY to be approximately 20 MHz at 4.2 K.
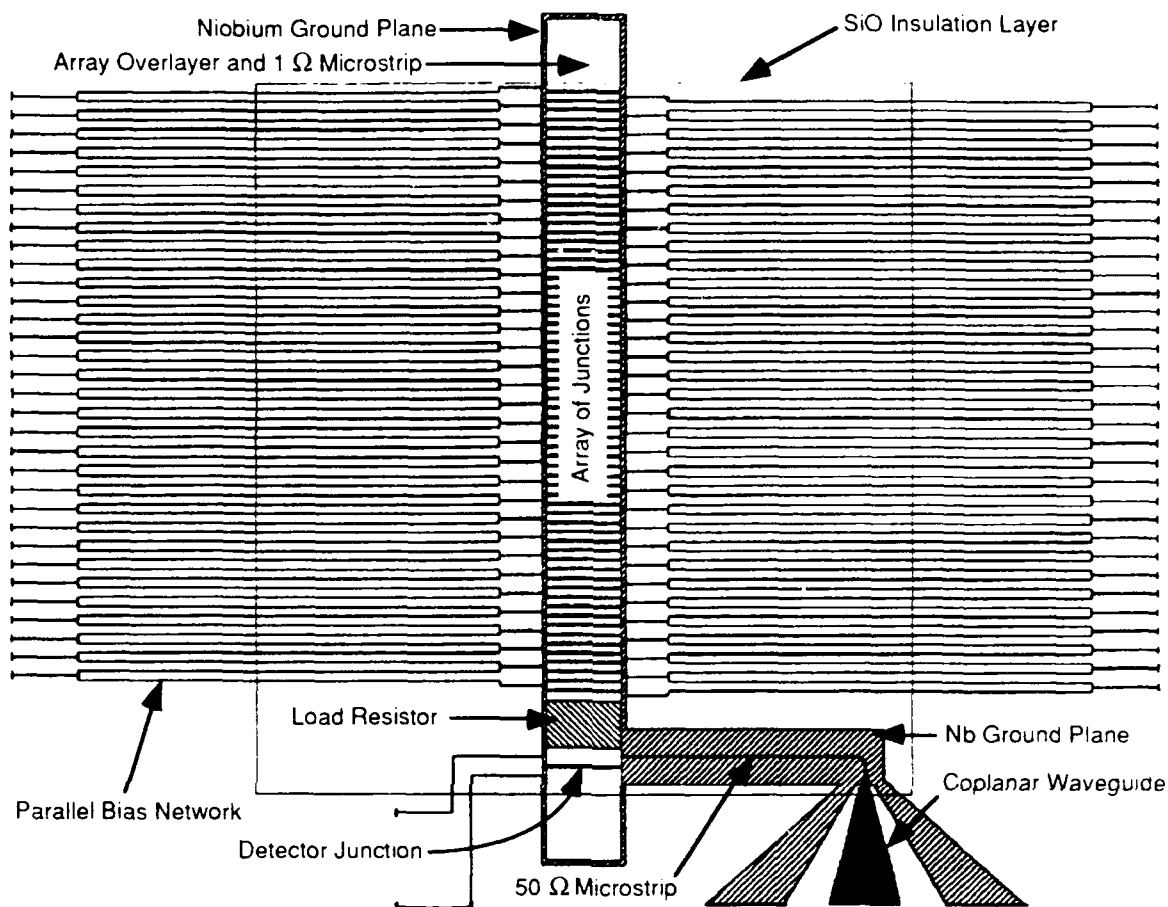
Figure 10. Detail of the VCO Array

Table 4. Performance Characteristics for the Superconducting VCO Sample 20GHz-11G

- Critical current: $I_c \sim 1\text{mA}$
- Shunt resistance: $60 \text{ m}\Omega < R_s < 100 \text{ m}\Omega$
- Maximum bias current: $I_{max} < 150 \text{ mA}$
- Typical operating current: $I_{operating} \sim 100 \text{ mA}$
- Typical operating voltage: $V_{operating} \sim 30 \text{ mV}$
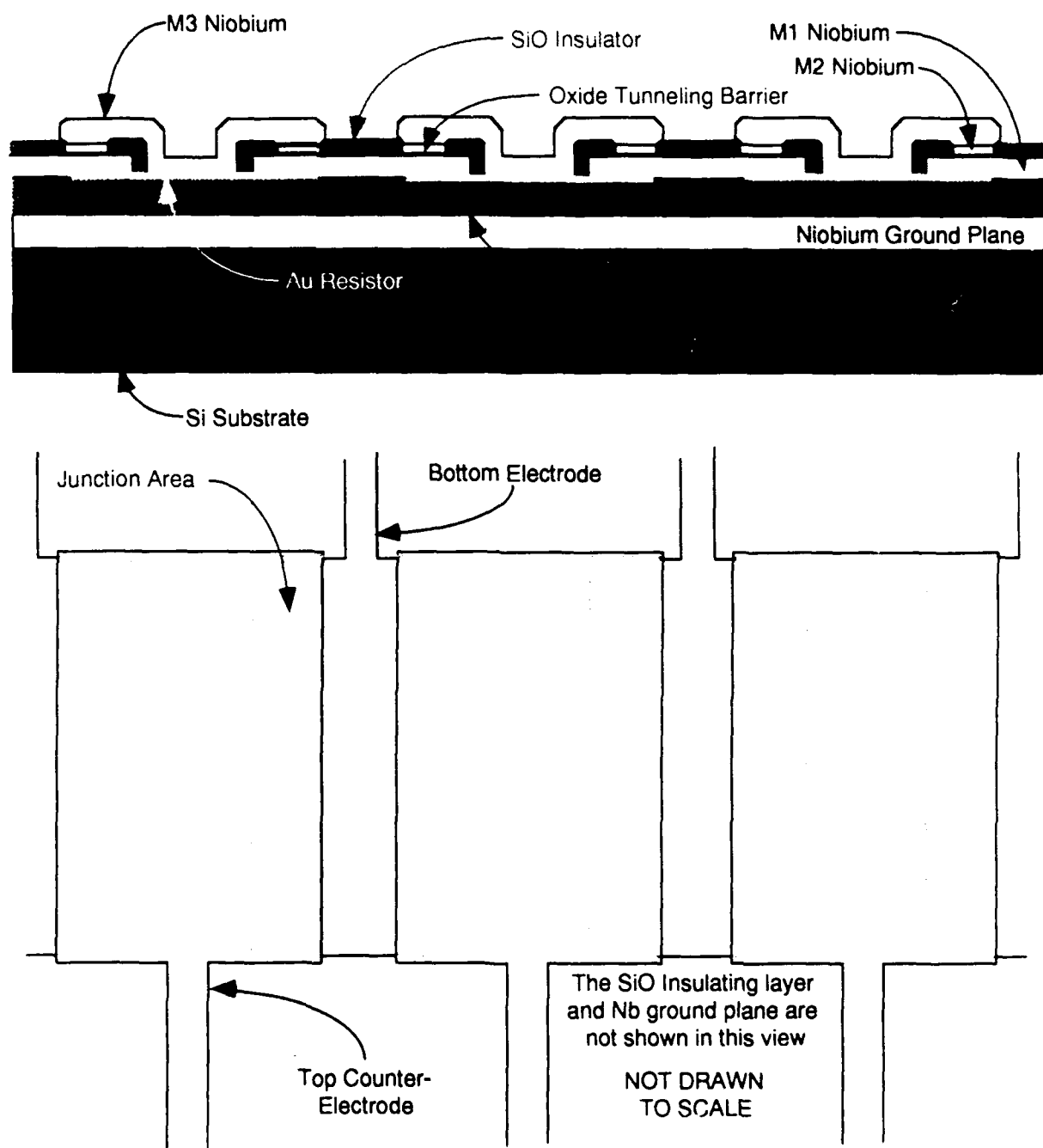- Expected output power: $P_{50\Omega} \sim 4 \text{ nW} (-54 \text{ dBm})$

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M3 Niobium

SiO Insulator

M1 Niobium

M2 Niobium

Oxide Tunneling Barrier

Niobium Ground Plane

Au Resistor

Si Substrate

Junction Area

Bottom Electrode

The SiO Insulating layer
and Nb ground plane are
not shown in this view

NOT DRAWN
TO SCALE

Top Counter-
Electrode

Figure 11. Cross-Sectional and Top-Down Views of the Array Josephson Junctions

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3.2 MEASUREMENT RESULTS

In our initial characterization of the superconducting VCO we used a MITRE-built current source to drive the array and an HP71201A spectrum analyzer to measure the output radiation. The MITRE current source is nearly identical to a sweeping, battery-powered supply described in [15], except that we substituted a higher power output transistor (IRF520) for the specified JFET, and laboratory power supplies in place of four 6-V dry cells. These are sufficiently noise free so that battery operation, which we also tested, is indistinguishable. As mentioned above it is important for the spectrum analyzer not to influence the coherent oscillations of the VCO array through leakage of the first LO. SUNY provided us with a conservative specification that any spurious radiation should be less than -120 dBm. We did measure the first LO emission of the HP71201A to be -90 dBm without the spectrum analyzer's HP70620A preamplifier. The integral preamplifier provides an additional 30 dB of reverse isolation, and we were able to verify that the first LO emission was less than -115 dBm with the preamplifier. We also had available broadband isolators which provided an additional 18 dB of reverse isolation each. The VCO sample was attached to the SMA launcher of the MITRE cryogenic probe using silver epoxy. The VCO array is operated in a reservoir of liquid helium at a temperature of 4.2 K or lower. The following paragraphs present various measured data for the superconducting VCO.

3.2.1 Output Power Spectrum

During this initial test we measured the VCO output frequency and power as a function of drive current. Figure 12 shows a typical output spectrum as recorded by the HP71201A, at a bias current of 87.0 mA. It shows a peak response of approximately -84 dBm at a frequency of 18.4 GHz. The peak RF power we observed was 30 dB less than the -54 dBm reported by SUNY [16].
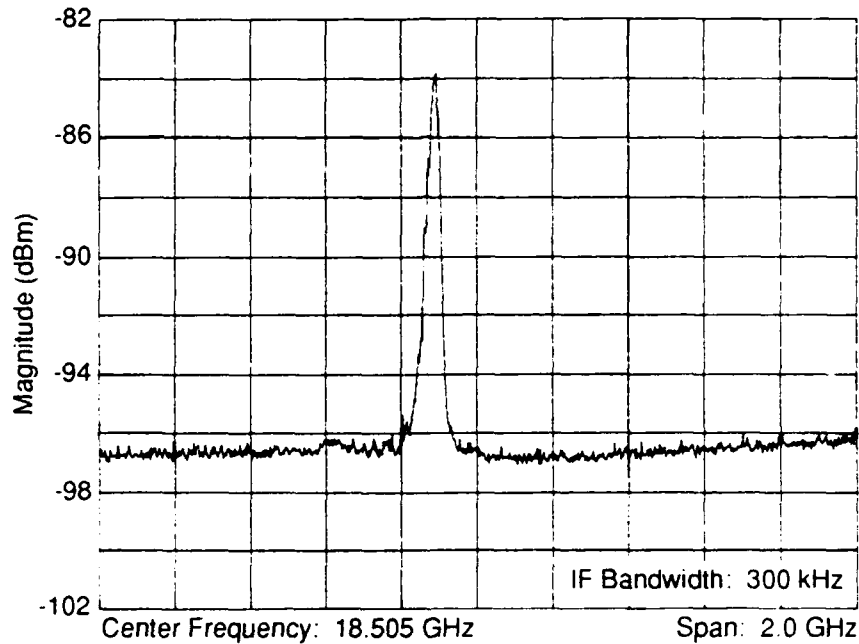

Figure 12. Typical VCO Output Power Spectrum

3.2.2 Frequency Dependence on Bias

In figure 13 our measured data is compared with the theoretical prediction of equation (1), which shows the fundamental frequency observed or predicted as a function of bias current. The three theoretical curves are defined by assignment of various choices of shunt resistance (R_s) and Josephson critical current (I_c) values. Curve 1 is based on values of both R_s and Ic reported in table 1 and curve 3 is based on the previously reported design value of R_s, 20 mΩ. Curve 2 is the result of an empirical fit using R_s and I_c values of 30 mΩ and 0.5 mA, respectively. It is evident from figure 13 that the fit of curve 2 is clearly superior. This

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fact, coupled with the 30 dB discrepancy between MITRE and SUNY RF power measurements, led us to pursue additional experiments to reconcile these differences and independently estimate array parameters.
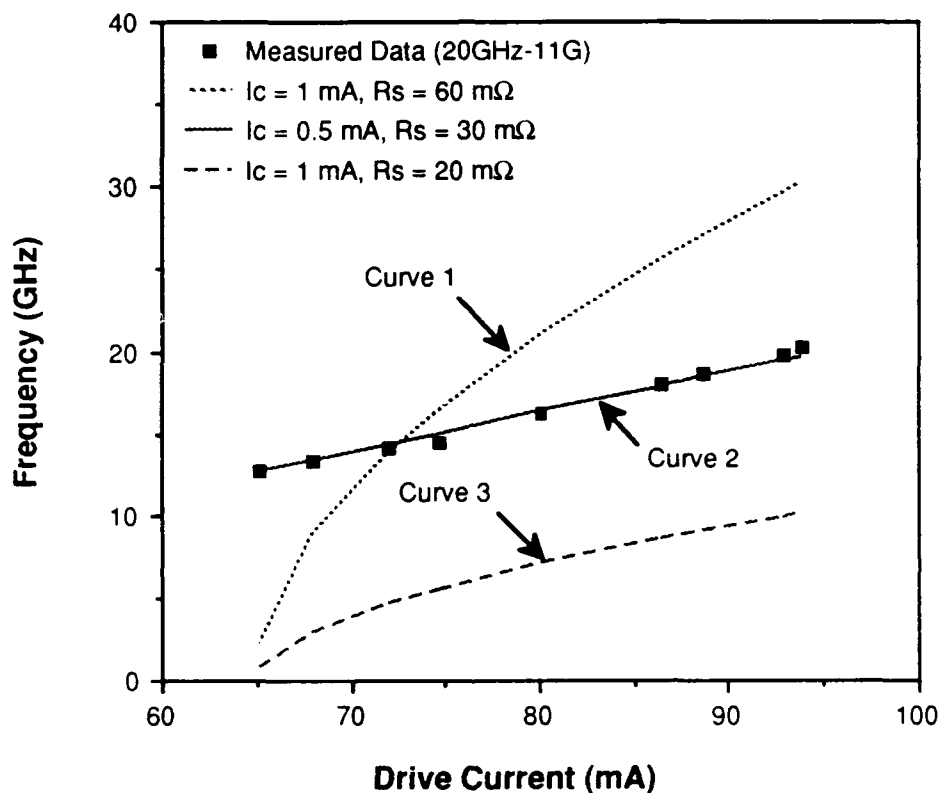

Figure 13. Oscillator Frequency versus Bias Current

According to the design, the integrated detector junction of the VCO array has identical dimensions to, and is fabricated concurrently with the drive junctions of the array. Therefore the detector junction should be representative of each of the 65 array junctions. The detector junction is separately testable, which allowed us to directly measure its shunt resistance R_s. We accomplished this using a four-wire resistance measurement technique, where a Keithley 238 precision current source drove current through the junction and the voltage developed across it was measured with an HP3478A voltmeter. Thus, an accurate measurement of Rs was made by varying the detector junction bias current and recording the resulting junction voltage as shown in figure 14. Below about 0.5 mA the junction voltage drop was

immeasurably small (i.e. superconducting state). This observation indicates that I_c at 0.5 mA for the detector junction, and the slope (37.2 mΩ) of the straight line fit to the data is the measured shunt resistance of the detector junction and hence our best estimate of R_s for the array junctions. SUNY [17] believes, however, that this detector junction is not representative of the array junctions because their measurements show array junction critical currents of approximately 1 mA. We were unable to directly measure array junction critical currents, and hence were unable to confirm their measurements. The slope of the curve indicates the junction shunt resistance R_s. These measurements were made on the detector junction (representative of the individual array junctions) as discussed in the text.
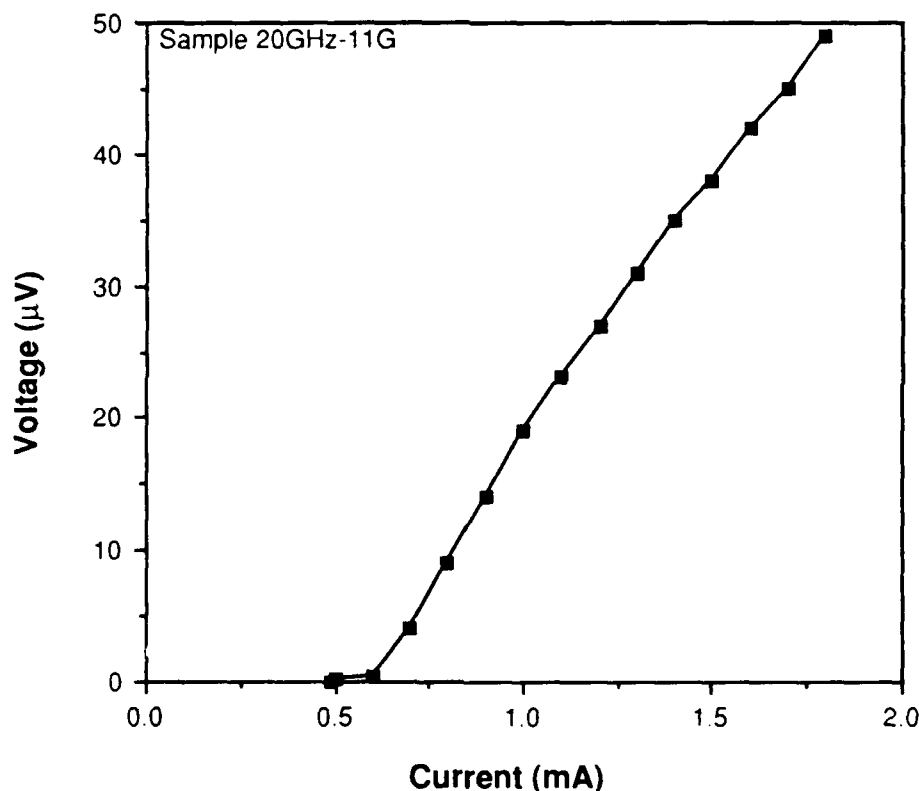

Figure 14. Voltage as a Function of Current for a Single Shunted Josephson Junction.

3.2.3 Comparison to Other Measurements

In an effort to resolve the conflicting output power observations, we measured RF power as a function of VCO drive current using both the HP71201A spectrum analyzer and an HP438A bolometric power meter. Prior to this measurement, we recontacted the VCO chip using indium foil, replacing the silver epoxy which was suspect at cryogenic temperatures. During this experiment, drive current was provided by the Keithley 238 precision current source. Figure 15 contrasts the power measurements taken with the spectrum analyzer and the power meter, while a typical output spectrum for the recontacted VCO chip is depicted in figure 16. Although the peak power measured using the spectrum analyzer was now 6 dB less than the previous measurement (-90 verses -84 dBm), the measurement difference between figures 12 and 16 is likely a result of losses incurred by the chip recontacting.

Figure 15. Output Power versus Bias Current

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
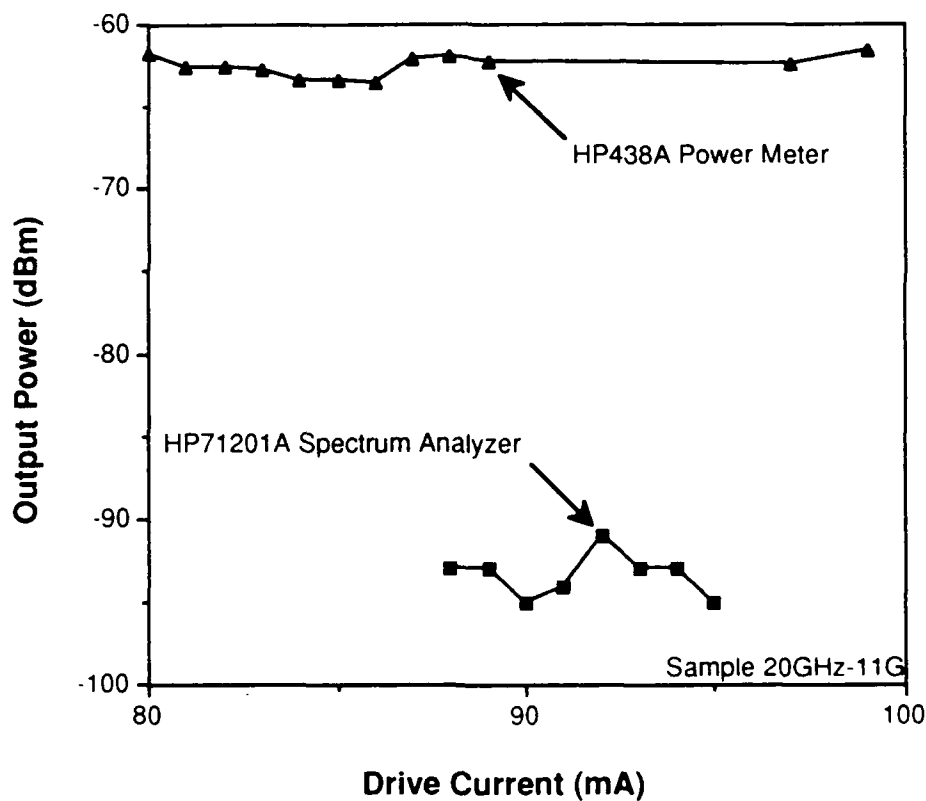
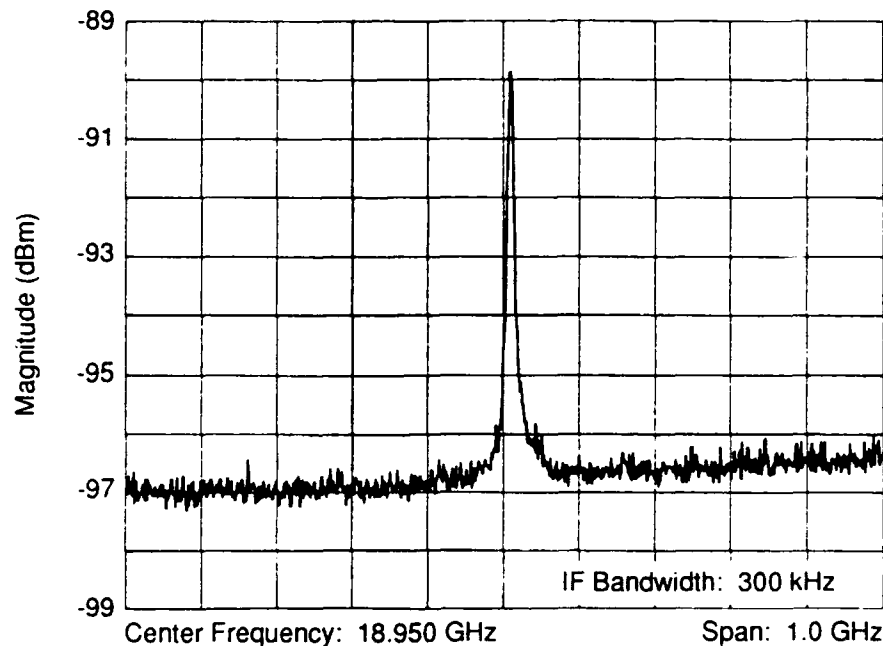Figure 15. Output Power versus Bias Current

Figure 16. Typical VCO Output Power Spectrum

It is important to recognize that the bandwidth of the spectrum analyzer measurement (figure 16) is quite narrow with respect to the array output bandwidth. SUNY measured an output radiation bandwidth of 20 MHz at 4.2 K, whereas it was necessary for MITRE to use a resolution bandwidth of 300 kHz to sufficiently lower the noise floor to allow the spectrum analyzer power measurements. Since the bolometric power meter integrates all incident RF power, this fact alone accounts for a 20 dB measurement difference between the power meter and the spectrum analyzer. We were not able to correlate this measurement with on-chip power measurements, because MITRE does not have a sufficiently sensitive voltmeter to measure Shapiro steps. SUNY has also suggested [17] that the measured frequency peaks as reported here may be the second harmonic response, and that the fundamental response (at the same frequency) would be obtained at about twice this bias current. We do not believe this to be the case, and through an additional spectrum analyzer investigation we have confirmed that we were indeed measuring the fundamental response.

The insertion loss of the cryogenic probe and connecting cable could be another contributor to the observed output power differences. Insertion loss measurements were taken for the cryogenic probe, and the cable that attached the probe to the test equipment. Figure 17 shows a plot of insertion loss versus frequency for the cryogenic probe, and connecting cable. The maximum insertion loss measured was approximately 6.5 dB at a

frequency of 20 GHz. In comparison, the maximum insertion loss of the SUNY probe and connecting cable has been reported to be about 3 dB [17].
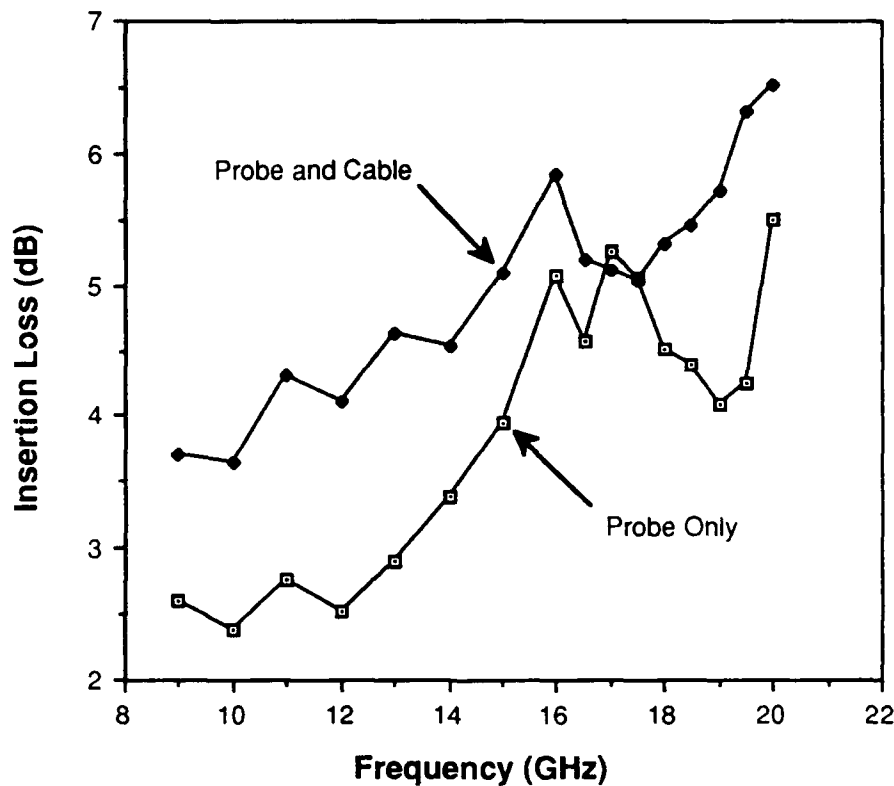

Figure 17. Insertion Loss of the Cryogenic Probe

In concluding our observations on the performance of the sample 20GHz-11G, there are inconsistences between the MITRE data and the baseline data on the array as reported to MITRE by SUNY. The major difference is that the narrowband spectrum analyzer power measurement fails to integrate the available output power. Further measurements should be performed at lower temperature (1.4 K) in order to narrow the bandwidth of the output radiation.

More recently, Wan et al. [18] have reported on the ability of these arrays to track a given frequency and then change rapidly to another frequency in response to various modulating bias inputs. They report the ability to tune and track a modulating input at a center frequency

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in the 12 to 18-GHz range exceeds a rate of 3.6 GHz. They also report a power level of 0.2 μW as detected on the oscillator chip. When we take into account the impedance mismatch (50:1) in transitioning to the output coax and the 6 dB loss in that coax to room temperature, it appears that our power measurement is about 10 dB down from this level. However, we made a narrow band (300 kHz) measurement by necessity, and the actual power spectrum is more likely to be on the order of 20 MHz.

SECTION 4

CONCLUSION

In summary, theoretical modelling and analysis of superconducting voltage controlled oscillators as driving sources for digital converters is inconclusive. This investigation has not demonstrated their utility for that purpose.. MITRE measurements of VCO chip number 20GHz-11G have been completed to the extent possible with existing MITRE equipment. We have confirmed that coherent oscillations with some degree of phase locking of the 65 junctions of the array are observed. Overall system output power as measured at MITRE at 18 GHz was -84 dBm when measured with a resolution bandwidth of 300 kHz. The fit of the data and such measurements as we can perform on the detector junction appear to be self consistent. VCO output power levels of 0.02 to 0.2 microwatts may be usable for a frequency discriminator drive source in a superconducting analog-to-digital converter design. But if the output spectrum is much broader than 300 kHz, then the precision requirements will be compromised. Measurements by investigators at the State University of New York on these multiple-junction oscillators demonstrate the ability of these arrays to change their output frequency rapidly (a rate in excess of 3.6 GHz) in the range of 12 to 18 GHz.

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GLOSSARY

ADC   analog-to-digital converter

SADC   superconducting analog-to-digital converter

VCO   voltage-controlled oscillator

Technical Report 4

OBTAINING HIGH-ACCURACY MEASUREMENTS FROM LOW-ACCURACY MEASUREMENTS

by

D. I. Zwillinger
D. J. Muder

ABSTRACT

This document explores the possibility of using a modification of a residue number system (RNS) to combine low-accuracy measurements in order to obtain high-accuracy measurements. We focus on the application of this technique to analog-to-digital (A/D) conversion and obtain an upper bound on the average number of bits of information that can be obtained from many low-accuracy A/D devices. This upper bound increases as the logarithm of the number of devices.

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FIGURE   **PAGE**

SECTION 1

INTRODUCTION

Frequently we would like to measure an analog quantity to a high degree of accuracy and store or process the result in a digital format. However, high-accuracy analog-to-digital (A/D) converters can be quite expensive and/or difficult to build. This suggests the following question: Is it possible to combine the outputs of many low-accuracy A/D converters in such a way as to obtain a high-accuracy measurement? J. Schoen [2] has suggested a method for doing this by using an analog extension of a residue number system (RNS). This system is called an analog residue number system (ARNS).

While this method certainly does result in increased accuracy (as we demonstrate in section 3), its ultimate value depends on the number of devices needed to obtain a given increase in accuracy. Our result is a best-case upper bound on the average number of bits of information that can be obtained from using N low-accuracy devices. We find that this upper bound increases as $\log N$.

A list of variable names is in appendix A.

SECTION 2

DEFINITION OF ARNS

A residue number system (RNS) is a well-known way of representing integer quantities. It works in the following way: Suppose that $m_1, m_2, \ldots, m_N$ are relatively prime positive integers (called the *moduli* of the system). Any given integer k can then be represented by its residues $(k \mod m_1, \ldots, k \mod m_N)$. The Chinese Remainder Theorem [1] guarantees that this representation is unique for any positive k less than the product of the moduli. The advantage of this system is that the residues are in some sense uncoupled; operations like addition and multiplication can be performed on individual residues without reference to the other residues.

The ideas behind RNS can be generalized to analog systems, producing ARNS. Let us suppose that we have N positive real numbers $m_1, m_2, \ldots, m_N$. Given an analog input d, we compute the analog residues by removing as many integer multiples of the moduli as possible, and still have a non-negative remainder:

$$r_i := d - m_i \left\lfloor \frac{d}{m_i} \right\rfloor, \tag{1}$$

where $\lfloor \rfloor$ indicates the floor function. (This is the same formula that RNS would use to find the residues of an integer d.) The residue r_i lies in the range $0 \le r_i < m_i$. For convenience, we can scale the residues so that they all lie in the interval $[0, 1)$, i.e., let $s_i := r_i/m_i$. Then n-bit A/D conversion can be applied to each scaled residue to obtain an integer q_i in the range $[0, 2^n - 1]$: Let $q_i := f(s_i 2^n)$, where f is a rounding function. We then associate the integer-valued vector $\mathbf{q} = \mathbf{q}(d) = \{q_1, \ldots, q_N\}$ with the input d. We refer to this as the *codeword* associated with the input d.

If $\mathbf{q}$ is the codeword of d, then $\mathbf{q}$ is also the codeword of any input in an interval containing d. As d increases, different codewords occur; but since there are only a finite number of codewords, eventually a codeword will repeat, i.e., it will correspond to two noncontiguous intervals. This is what limits the dynamic range of the system. Hereafter we will assume that d lies in the interval $[0, D]$, where D is small enough that each codeword is associated with only a contiguous range of d values in $[0, D]$.

Our motivation for examining ARNS came from the A/D conversion system of [2]. The components of this system are very fast, low-precision A/D converters based on superconducting quantum interference devices (SQUIDs). The outputs of these converters are periodic, and thus the system is nicely modelled as an ARNS with the moduli corresponding to the periods of the components.

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SECTION 3

SOME SIMPLE EXAMPLES

In this section we illustrate both the forward and inverse methods of conversion. The forward method consists of finding the residues (and hence the codeword) corresponding to a given analog input. The inverse method translates a codeword back to a possible analog input.

3.1 THE FORWARD MAPPING

Consider using ARNS with two moduli ($M = 2$); $m_1 = 1.10$ and $m_2 = 1.20$. We suppose that we have 1 bit A/D converters with which to discretize the residues ($n = 1$). It is then easy to see that:

    (i)   If $0.00 \leq d < 0.55$, then $r_i = d$, and $\mathbf{q} = (0,0)$.

    (ii) If $0.55 \leq d < 0.60$, then $r_i = d$, and $\mathbf{q} = (1,0)$.

    (iii) If $0.60 \leq d < 1.10$, then $r_i = d$, and $\mathbf{q} = (1,1)$.

    (iv) If $1.10 \leq d < 1.20$, then $r_1 = d - 1.1$, $r_2 = d$, and $\mathbf{q} = (0,1)$.

And, hence, $D = 1.20$; observe that $\mathbf{q}(1.20 + \delta d) = (0,0) = \mathbf{q}(0)$, when $0 < \delta d \ll 1$.

In figure 2 we show the values of s_1 and s_2 as a parametric function of the input d. Superimposed on this figure are the grid values given by the $f(x)$ function (indicated by the dashed lines). We refer to this type of figure as an ARNS portrait. From this figure we see the sequence of codewords (quadrants in this case) visited by the input value d are $(0,0)$, $(1,0)$, $(1,1)$, and $(0,1)$.

Assuming that the input value is uniformly distributed on the range $[0.00, 1.20]$, the expected number of bits of the information obtained about the input signal by the two measurements is given by the binary entropy

$$H(\mathbf{p}) = -\sum_i p_i \log_2 p_i,$$

where p_i is the probability of being in region i (see McEliece [3]). In this example, the probability that the output is

    (i) $\mathbf{q} = (0,0)$ is $p_1 = 0.55/1.20 \simeq 0.46$,

    (ii) $\mathbf{q} = (0,1)$ is $p_2 = 0.05/1.20 \simeq 0.04$,

    (iii) $\mathbf{q} = (1,1)$ is $p_3 = 0.50/1.20 \simeq 0.42$,

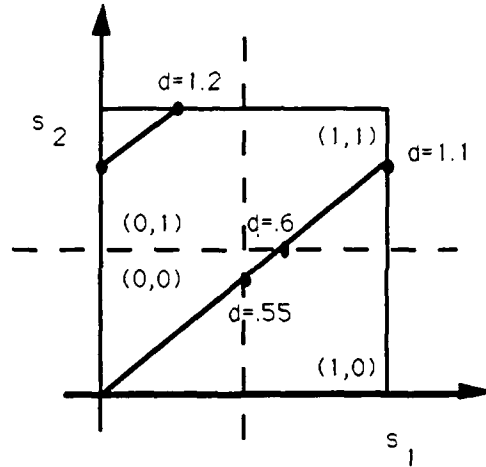   (iv) $\mathbf{q} = (1,0)$ is $p_4 = 0.10/1.20 \simeq 0.08$,

Figure 1. The ARNS Portrait of the Example.

from which we find the entropy to be 1.53 bits. We conclude: two 1 bit measurements can be combined to yield, on average, 1.53 bits of information about the input signal. Hence, we have combined two low-accuracy estimates of an analog quantity to obtain a higher (expected) accuracy estimate of that analog quantity.

Note that the average information obtained about the input signal is *not* the same as the accuracy of the output. In the above example, only 1.1 bits of accuracy are obtained about the input signal when the output codeword is $q = (0,0)$ (since the accuracy, in bits, is given by the logarithm, base 2, of the probability of occurrence, $1.1 = \log_2 0.46$). Alternately, when the output codeword is $q = (0,1)$ we obtain $\log_2 0.05 = 4.3$ bits of information. If we average together the accuracy obtained (the weighting factor is the probability of occurrence), then we obtain the entropy. So the 1.53 bits we obtain finally is only an average; 46% of the time we will obtain only 1.1 bits of accuracy.

In this example, the range of d values resulted in a "path" through four codewords. The most information (i.e., the largest entropy) that can be obtained from a visit to four codewords is $\log_2 4 = 2$ bits (which is obtained by assuming that each codeword has an equal probability of being visited, see McEliece [3]). In general, using N devices that each have an accuracy of n bits, the largest possible entropy obtainable is given by assuming that each of the $(2^n)^N$ codewords has an equal probability of being visited; that is

$$\text{maximal information} \leq \log_2 (2^n)^N = Nn \text{ bits} \tag{2}$$

With $N = 2$ and $n = 1$ this yields the above bound of 2 bits of information on average.

If we had used the same moduli as above, but used 2-bit A/D converters instead of 1-bit A/D converters, then we would have found:

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(i)   If $0 \leq d \leq 0.275$, which occurs with probability 0.229, then $\mathbf{q} = (0,0)$.

(ii)   If $0.275 \leq d \leq 0.3$, which occurs with probability 0.021, then $\mathbf{q} = (1,0)$.

(iii) If $0.3 \leq d \leq 0.55$, which occurs with probability 0.208, then $\mathbf{q} = (1,1)$.

(iv)   If $0.55 \leq d \leq 0.6$, which occurs with probability 0.042, then $\mathbf{q} = (2,1)$.

(v)   If $0.6 \leq d \leq 0.825$, which occurs with probability 0.188, then $\mathbf{q} = (2,2)$.

(vi)   If $0.825 \leq d \leq 0.9$, which occurs with probability 0.063, then $\mathbf{q} = (3,2)$.

(vii) If $0.9 \leq d \leq 1.1$, which occurs with probability 0.167, then $\mathbf{q} = (3,3)$.

(viii) If $1.1 \leq d \leq 1.2$, which occurs with probability 0.083, then $\mathbf{q} = (0,3)$.

And, again, $D = 1.20$. The maximum accuracy is obtained, 5.5 bits, when the output is $\mathbf{q} = (1,0)$; the minimum accuracy is obtained, 2.1 bits, when the output is $\mathbf{q} = (0,0)$. Appropriately averaging the different accuracies, we find the entropy to be 2.70 bits of information.

3.2   THE INVERSE MAPPING

In principle, the codeword vector $\mathbf{q}(d)$ can be inverted to obtain the range of d values $(d_{\min}, d_{\max})$ that yield $\mathbf{q}(d)$ for the first time. However, we have not yet been able to find an efficient way to determine this inverse function.

We will illustrate, however, how the vector of residues can be used to obtain the analog input d giving rise to those residues. Consider, as in section 3.1, using the two moduli $m_1 = 1.10$ and $m_2 = 1.20$. We assume that we have obtained the residues $r_1 = 0.24$ and $r_2 = 0.34$; we would like to find the corresponding value of d. By (1) we have the two relations

$$d = r_1 + k_1 m_1 \qquad \text{and} \qquad d = r_2 + k_2 m_2,$$

for some unknown integers k_1 and k_2. Since there might have been small errors made, we prefer to write this as

$$\widehat{d} \sim r_1 + k_1 m_1 \qquad \text{and} \qquad \widehat{d} \sim r_2 + k_2 m_2, \tag{3}$$

where $\widehat{d}$ is an estimate of d. Equating these two expressions, we find that $r_1 + k_1 m_1 \sim r_2 + k_2 m_2$ or

$$0.24 + k_1(1.10) \sim 0.34 + k_2(1.20)$$

or

$$k_1(1.10) + k_2(-1.20) \sim 0.10$$

or (dividing both sides by 0.10)

$$k_1(11.0) + k_2(-12.0) \sim 1. \tag{4}$$

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If we approximate the real numbers appearing in (4) by rational numbers, then we can determine the values of k_1 and k_2 by the method described in Jaeschke [4]. Alternately, the Euclidean algorithm (see Knuth [5], page 325) can be used to find the k_1 and k_2 values that satisfy (4). (Normally the Euclidean algorithm is applied to integer inputs, but we will formally apply it to the analog input values 11.0 and 12.0.) Applying this algorithm, we obtain $k_1 = k_2 = -1$; which (using (3)) gives us an estimate of d: $\hat{d} = -0.86$. Note, however, that this is only one possible value of d: other values are given by $\hat{d} + L$, where L is any number that satisfies $L = 0 \pmod{m_1}$ and $L = 0 \pmod{m_2}$. For this example, L can be any integer multiple of $10 m_1 m_2 = 13.2$. so we conclude that the analog input d could be any of $\{\hat{d}, \hat{d} \pm L, \hat{d} \pm 2L, \dots\}$. Since we are looking for the smallest positive value of $\hat{d}$, we would choose $\hat{d} = 12.34$.

In this example the inputs to the Euclidean algorithm were really integers, but that need not be the case. Let's analyze another possible set of residues: $r_1 = 0.235$ and $r_2 = 0.345$ (which are perturbations of the above values). In this case we need to solve the equation (this is the equation analogous to (4)):

$$k_1(10.0) + k_2(-10.91) \sim 1.$$

In this case we again obtain $k_1 = k_2 = -1$. Now, however, (3) yields the two different estimates of d: $\hat{d} = -0.865$ and -0.855; clearly indicating that an error has occurred somewhere in the system. However, to the accuracy of the input moduli, we would probably take $\hat{d} = -0.86$.

Inverting an N-element vector of residues to find the analog input that gave rise to those inputs is now straightforward. Any two residues (and their corresponding moduli) can be replaced by a single residue with a larger modulus. In the above example, the remainders with respect to the moduli $m_1 = 1.10$ and $m_2 = 1.20$ were replaced by a remainder relative to the modulus $L = 13.2$. This process can be repeated until only a single set of estimates for d are obtained.

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SECTION 4

FINITE PRECISION IMPLICATIONS

In (2) we saw that an ARNS A/D converter can provide no more than Nn bits of accuracy. However, in most cases limitations on the accuracy of representing the moduli prevent this upper bound from being attained. In this section we examine these limitations and establish an upper bound on accuracy that is logarithmic (rather than linear) in N, the number of devices. In fact, our upper bound is a bound not simply on the accuracy of the converter, but on the average information that such a converter can provide about the input signal. As we saw in the examples of the previous section, average information is a weaker concept than guaranteed accuracy; an A/D converter can provide an average of b bits of information without guaranteeing b bits of accuracy.

In a real implementation of an A/D converter or similar device, the analog moduli m_i cannot be represented with perfect accuracy. Furthermore, since the moduli are analog quantities, their values can drift with usage; that is, each modulus can vary on each use. If, however, the first B bits of m_i always remain the same, we will say that m_i has been represented with B bits of accuracy. More precisely, we will assume that $\lceil 2^{B+1} m_i \rceil$ (mod 2) is equally likely to be zero or one, where $\lceil \ \rceil$ represents the ceiling function. Alternatively, we presume that m_i has a design value v_i, and each time the parameter m_i is used it has some value in the range $(v_i - 2^{-B-1}, v_i + 2^{-B-1})$.

The effects of this limitation in accuracy ripple through the system, placing limits on the accuracy of the output that, in most cases, are far more restrictive than the bound of Nn bits. In this section we will analyze these limitations for the case (typical in RNS applications) where all the moduli are of the same order of magnitude. That is, we assume the moduli can be scaled so that all of them lie in the interval $(1/2, 1)$.

We first need some notation to indicate the nominal accuracy of any of the moduli: let M_i denote the minimal value of m_i. That is, while m_i is a random variable that can change with each use, M_i is the least value that m_i can be; M_i is not a random variable. For example, if m_i is in the range $(v_i - 2^{-B-1}, v_i + 2^{-B-1})$, then $M_i = v_i - 2^{-B-1}$. We always have the relation

$$\frac{M_i}{m_i} = \frac{v_i - 2^{-B-1}}{m_i} \geq \frac{v_i - 2^{-B}}{\max m_i} = \frac{v_i - 2^{-B-1}}{v_i + 2^{-B-1}} = 1 - \frac{2^{-B}}{v_i + 2^{-B-1}}.$$

assuming, as before, that every v_i is between one-half and one we find that

$$1 \geq \frac{M_i}{m_i} \geq 1 - 2^{-B+1} = 1 - \epsilon, \tag{5}$$

where ϵ is defined by the last expression.

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To determine the finite precision implications, we start with the definition of the residue (equation (1)) and try to determine the accuracy of the output q_i; we recall that q_i is given by

$$q_i = f(s_i 2^n) = f\left(\frac{r_i}{m_i} 2^n\right) = f\left(2^n \left\{\frac{d}{m_i} - \left\lfloor \frac{d}{m_i} \right\rfloor\right\}\right). \tag{6}$$

We observe that the expression d/m_i appearing in (6) can be written as $(d/M_i)(M_i/m_i)$ and, because of the uncertainty of m_i, this is a value in the range (see (5))

$$\left[\frac{d}{M_i}(1 - \epsilon), \frac{d}{M_i}\right].$$

First, we assume that d is in the range $[0, 2^{B-n-1} M_i)$. In this case, the value of d/M_i is always less than 2^{B-n-1}, therefore $(d/M_i)\epsilon$ is less than 2^{-n}. That is, the error in d/M_i, due to the variability of m_i, will be smaller than the least significant bit in the n-bit A/D converter. Hence, for this range of d values, the value of q_i will have n significant bits.

Now we consider the value of d to be in the range $[2^{B-n-1} M_i, 2^{B-n} M_i)$. In this case, $(d/M_i)\epsilon$ is in the range $(2^{-n}, 2^{-n+1})$; that is, one bit of the q_i value could be in error. Since we are searching for an upper bound, we will assume the most optimistic case, that q_i has n bits of accuracy.

In the more general case, we now assume the value of d to be in the range $[2^{B-n-1+j} M_i, 2^{B-n+j} M_i)$ (for $j = 0, 1, 2, \ldots$), then $(d/M_i)\epsilon$ is in the range $(2^{-n+j}, 2^{-n+j+1})$; that is, at least j bits of each q_i will be in error, with the error being possibly as large as $j + 1$ bits. In the most optimistic case, q_i has $n - j$ bits of accuracy. Clearly, when $j = n$, there is no accuracy in the resulting value of q_i. This leads to the upper bound $D \leq 2^B M_i$. Since we have assumed that each v_i is less than 1, we also have $M_i \leq 1$. Hence, the maximum value of d is bounded above by $D = 2^B$.

Now let us consider the number of useful values that can be produced by using this upper bound on D. When d is in the range $[0, 2^{B-n-1} M_i)$, every transition of q_i is significant. That is, when the value of q_i changes, every bit in the new value of q_i provides real information about the input (rather than simply reflecting jitter in the moduli). From (6) we see that when d increases by M_i, the output q_i may vary through as many as 2^n values. Hence, as d varies from 0 to $2^{B-n-1} M_i$, the number of transitions is upper-bounded by 2^{B-1}.

Alternately, when d is in the range $[2^{B-n-1+j} M_i, 2^{B-n+j} M_i)$, only the transitions that change the $n - j$ most significant bits of q_i provide information about the input (since the $n - j$ least significant bits are assumed to be in error in this range). The

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width of the interval, times at most 2^{n-j} significant values per M_i width, leads to at most 2^{B-1} significant transitions.

Hence, for all d values in the range $[2^{B-n-1}M_i, 2^B M_i])$, the number of significant changes in q_i is $\sum_{j=0}^{n} 2^{B-1} = (n+1)2^{B-1}$. To this number we add the number of significant changes that occur when d is in the range $[0, 2^{B-n-1}M_i)$; which is 2^{B-1}. The net result is that at most $(n+2)2^{B-1}$ different significant transitions occur when d varies along its maximum range.

Now that we have found the maximum number of significant transitions that can occur for a single modulus as the input is varied, we consider the maximum number of significant transitions that can occur when the ARNS system is used. Using N moduli the maximum number of significant transitions that can occur is simply $N(n+2)2^{B-1}$. Phrased another way, there are only $N(n+2)2^{B-1}$ different codewords that can be reliably reached. Hence, the maximal amount of information that can be obtained about the input signal is bounded above by

$$\text{maximal information} \leq \log_2 N(n+2)2^{B-1} \leq [(B-1) + \log_2(n+2) + \log_2 N] \text{ bits.} \quad (7)$$

If this bound is combined with the obvious bound in (2), then we obtain our final result:

$$\text{maximal information} \leq \min\left(nN, (B-1) + \log_2(n+2) + \log_2 N\right) \text{ bits.} \quad (8)$$

We emphasize that (7), and hence (8), are not tight upper bounds on the accuracy of the A/D converter for several reasons:

- (i) The distribution of input values will not be uniform on the total number of codewords visited.
- (ii) The maximum number of codewords visited is an upper bound.
- (iii) The bound of (8) is an average over the set of all inputs. It is possible that for some inputs the accuracy is much less.

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SECTION 5

NUMERICAL EXAMPLES

Let us reconsider the example in section 3.1 in view of the new upper bound. In the first part of the example we had $N = 2$ measurements and $n = 1$ bits of accuracy for each measurement. No mention of the accuracy of the analog components was made in that section. Assuming a minimal value of $B = 1$ bits of accuracy (since otherwise $n = 1$ bits of measurement accuracy does not seem reasonable), the bound in (7) results in an upper bound of $\min(2, 0 + \log_2 3 + \log_2 2) = 2$ bits of accuracy. We must emphasize, again, that this figure is only an average accuracy; some trials will result in more accuracy, others in less.

In the second part of the example in section 3.1, we used $n = 2$. If we assume that $B = 2$ in this case, the bound in (7) results in an upper bound of $\min(4, 1 + \log_2 4 + \log_2 2) = \min(4, 4) = 4$ bits of accuracy. How would this last result change if we considered using more devices? Using $N = 100$ devices (and keeping $n = 2$ and $B = 2$) we find that we cannot obtain more than 9.6 bits of accuracy.

Consider now a more realistic example. Suppose that low-accuracy measurements are made to an accuracy of 5 bits ($n = 5$). Suppose that the moduli are accurate to 9 bits of accuracy ($B = 9$). If we combine 10 low-accuracy measurements ($N = 10$) then, from (7), the maximum number of bits of measurement information that can be obtained about the input signal is less than $\min(50, 9 + \log_2 7 + \log_2 10) = 15.1$ bits. To have our upper bound be 16 bits of accuracy, we would need to use at least $N = 19$ devices. Of course, since the values presented in this section are upper bounds, the actual performance might be worse. We do not know how many devices would be required to have the minimal accuracy be 16 bits.

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SECTION 6
CONCLUSION

We have shown how low-accuracy measurements can be combined to yield high-accuracy measurements. We have found (see equation (7)) that the maximum number of bits of information that can be derived about the input increases no faster than the logarithm of the number of low-accuracy devices used.

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APPENDIX A

DEFINITION OF VARIABLES

Variables

B	accuracy, in bits, of the moduli
d	analog input value
D	maximal value of d
N	number of moduli in ARNS system
m_i	a sample analog modulus
M_i	minimal value of m_i
n	number of bits in the low-accuracy measurements
$\mathbf{q}$	a codeword
r_i	a residue
s_i	a scaled residue
v_i	design value for m_i

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Technical Report 5

SUPERCONDUCTING MICROWAVE TRANSMISSION LINES

by

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ABSTRACT

Superconducting microwave transmission lines can be designed to have lower loss, lower dispersion, and lower phase velocity than conventional metal lines. These properties make superconducting transmission lines attractive for use in many devices and systems such as filters and analog-to-digital converters. The problem with designing microwave circuits which utilize these lines is that accurate circuit models do not exist. This paper presents models for the microwave transmission line parameters (phase velocity, attenuation, and characteristic impedance) of superconducting lines as a function of temperature and geometry. An experiment to verify these models is also presented.

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SECTION 1

INTRODUCTION

The work described in this report was performed as part of project 91080, "Superconducting Analog-to-Digital Converters." One class of superconducting analog-to-digital converters (SADCs) utilize Josephson junctions, transmission lines, and filters consisting of metal in a superconducting state. In order to design SADCs, good models for superconducting microwave transmission lines must exist. This work focuses on modeling superconducting planar microwave transmission lines and designing experiments to verify these models.

Microwave transmission lines fabricated with superconducting material have several advantages over conventional transmission lines. Superconductors exhibit zero resistance at DC and the resistance increases with the square of the frequency. At microwave frequencies, the surface resistance of superconducting niobium is still three orders of magnitude smaller than that of copper at 4.2 K [1]. Thus, smaller microwave filters with higher Q-factors for Microwave and Millimeterwave Microwave and Millimeterwave Monolithic Integrated Circuits (MMIC) applications can be realized by using superconducting material. In addition to low loss, superconducting metals exhibit kinetic inductance associated with the magnetic fields stored in the superconductor. This kinetic inductance can be utilized to fabricate transmission lines with phase velocities as small as 1/100th of the speed of light [2].

Planar transmission lines compatible with SADC designs include Microstrip (MS), Coplanar Waveguide (CPW), Coplanar Strips (CPS), and slotline. The superconducting transmission line models we have developed are general and apply to any geometry of transmission line. Kinetic inductance effects are easiest to measure in MS geometry. For this reason the experimental portion of this study has focused primarily on MS. Kinetic inductance MS lines have extremely low characteristic impedances and for this reason we have analyzed CPW as a high-impedance to low-impedance transition from our 50-ohm measurement system to MS. The geometry of MS and CPW lines are illustrated in figures 1 and 2.

There are no commercially available computer aided design (CAD) tools for microwave design that accurately model the unique properties of superconductors. We have developed a capability for modeling elementary superconducting transmission lines, including the accurate simulation of complex conductivity as a function of temperature and frequency. In section 2 of this paper, these models are presented. These models produce results which can be incorporated into microwave circuit design programs such as Touchstone or Supercompact. Experiments must be performed to confirm the validity of our models. A general technique for extracting microwave transmission line parameters from measurements made on transmission line resonators is presented in section 2.

We have successfully used the resonant technique from section 2 to measure the properties of normal conducting transmission lines and the results are presented in section 3. We have
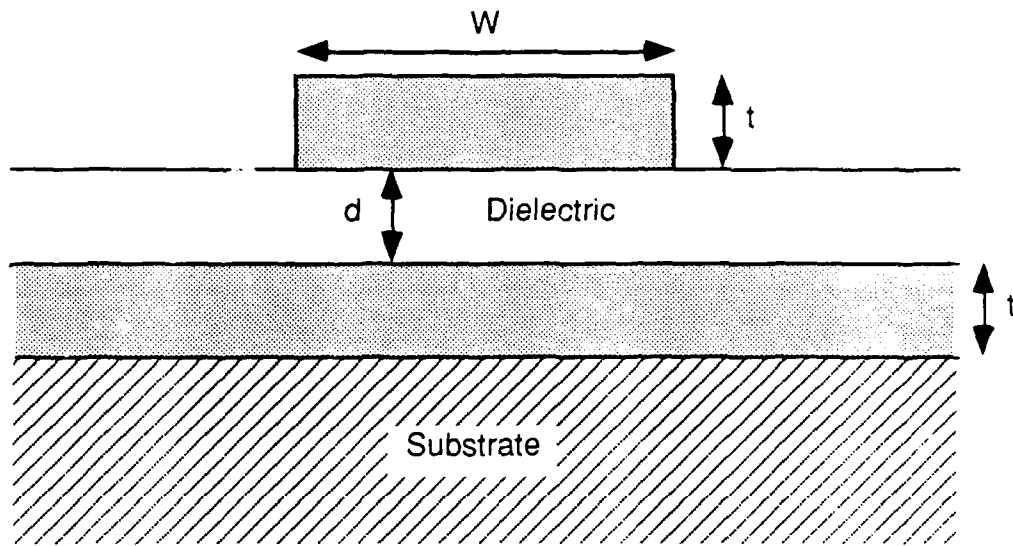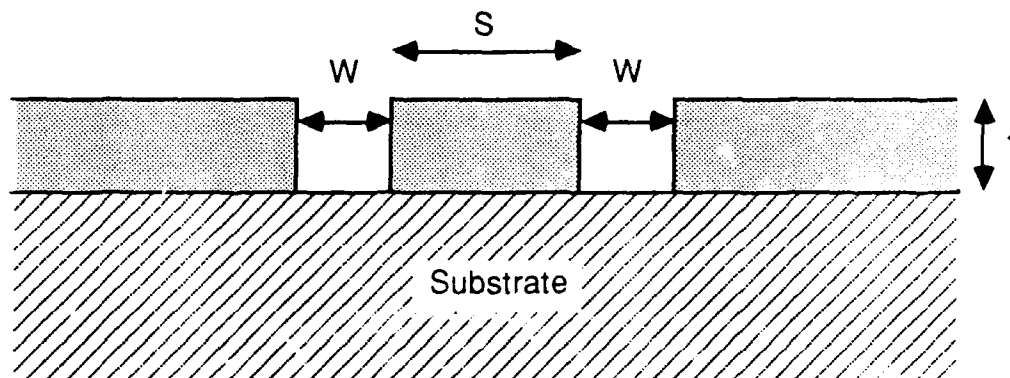
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Figure 1. Microstrip (MS) Geometry

Figure 2. Coplanar Waveguide (CPW) Geometry

designed two independent experiments to verify the superconducting transmission line models developed in section 2. These proposed experiments are an impedance mismatch coupled resonator and a dielectric step coupled resonator and are described in section 3. Designs for test circuits, along with associated matching networks are presented. Section 4 presents our recommendations for future work at MITRE in the area of superconducting microwave transmission lines.

SECTION 2

SUPERCONDUCTING TRANSMISSION LINES

The unique properties of superconducting materials can be exploited in microwave circuits to provide low-loss/dispersionless transmission lines, compact delay lines, and high-Q resonators. These applications result from fundamental differences in conductivity and field penetration between conventional metals and superconductors. For example, the surface impedance of a superconductor is several orders of magnitude more reactive than it is lossy. Also, field penetration into a superconductor is less than the classical skin depth and is essentially independent of frequency, thereby greatly reducing material dispersion in waveguides. In this section we will first examine the surface impedance of superconductors, and then present transmission line models which include this superconducting surface impedance.

2.1 SUPERCONDUCTING SURFACE IMPEDANCE

Superconductivity is the name given to a remarkable state transition of a material which is characterized by the disappearance of electrical resistance and the complete expulsion of magnetic flux. The name superconductivity was coined by Kamerlingh Onnes who, in 1911, discovered that resistance of a mercury filament abruptly dropped to an immeasurably small value at a temperature of approximately 4.2 kelvin (K). The diamagnetic property of superconductivity was discovered in 1933 by Meissner and Ochsenfeld, who showed that the transition to the superconducting state involved the expulsion of magnetic flux in a superconductor. This is in contrast to a perfect conductor, which would be expected to trap magnetic flux lines in place.

The temperature at which the superconducting state transition occurs is known as the critical temperature (T_c). The noun *superconductor* refers to a material which undergoes this state transition. A superconductor exhibits zero DC resistivity and diamagnetism at temperatures below the T_c, and the adjective *superconducting* is used to describe this condition. At temperatures above the T_c, a superconductor behaves as a *normal* metal. Today, approximately half of the metallic elements are known to be superconductors at sufficiently low temperature, as well as many compounds including the "high-T_c" ceramic materials.

Superconductivity was first characterized by phenomenological theories which attempted to account for the unique diamagnetic property of superconductors. The London theory [3] assumed that the superconductor conduction mechanism could be described by a two-fluid model which consists of normal electrons and super (resistanceless) electrons, and that diamagnetism could be explained by restrictions (not violations) of Maxwell's equations. The microscopic theory of superconductivity followed in 1956 when Cooper showed that two electrons could be coupled together into a bound state (Cooper pairs) through phonon scattering of the electrons in the lattice [4]. The hypothesis that electron-phonon interaction was responsible for superconductivity helps explain why good normal conductors (e.g., gold and copper, which do

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not have strong lattice vibrations) do not superconduct, while poor normal conductors are often superconductors. Cooper's result was extended to many pairs of interacting electrons to formulate the Bardeen-Cooper-Schrieffer microscopic theory of superconductivity (usually referred to as the BCS theory) [5].

The key principle of the BCS theory is that the super electrons are actually paired electrons which have condensed into a superconducting ground state, thereby resulting in a reduction of total system energy. An important feature of the superconducting ground state is that the Cooper pairs are all in the same quantum state, have the same energy, and are all described by the same wave function. This is a consequence of the paired electrons obeying Bose-Einstein statistics and; therefore, the Pauli exclusion principle (with respect to Fermions) does not apply. Thus the Cooper pairs overlap in a superconductor, with it being energetically favorable for them to have coherent (locked) phases over macroscopic distances (i.e., much greater than the lattice spacing.)

The condensation of electrons out of a continuum of allowed energy values into Cooper pairs at a single energy level also gives rise to an energy gap (Δ) at the Fermi surface. This energy gap is orders of magnitude less than the Fermi energy, typically about one millielectron volt, compared to Fermi energies of several electron volts. The energy gap, Δ, is the average energy per electron of a Cooper pair, relative to the continuum. The binding energy of a Cooper pair is therefore 2Δ, this being the minimum energy required to break the pair. Thus the situation in a superconductor can be thought of as analogous to a semiconductor, with both having an energy gap at the Fermi surface. When a superconductor is at finite temperatures below the T_c, thermal energy and incident radiation can break Cooper pairs. The electrons from the broken pairs are known as excited *quasiparticles*, which behave as normal electrons with well specified momenta. Since the binding energy between paired electrons is 2Δ, absorption of incident radiation is possible for field frequencies of $\omega > 2\Delta/\hbar$ where $\hbar$ is the reduced Plank's constant. This frequency is refered to as the gap frequency of a superconductor, typically about 1 THz. In the following paragraphs we will describe the surface impedance of superconducting materials by first presenting the complex conductivity of superconductors according to the two-fluid model, and then extend this result to include gap phenomena and temperature effects using the BCS theory.

The London theory predicts that fields (including static fields) cannot penetrate a superconductor beyond a penetration depth λ_L (a material parameter, typically 100 nm.) The penetration depth of a superconductor is defined as [6]

$$\lambda_L = \frac{m}{\mu_o n_s e^2}$$

(1)

where m is the electron mass, μ_o is the free space permeability, n_s is the density of the paired electrons, and e is the elementary charge. The total electron density (n) is the sum of n_s and the normal electron density n_n. Assuming an electric field in a superconductor in the form $Ee^{j\omega t}$ where ω is angular frequency $\omega = 2\pi f$ (vectors are denoted by bold face variables), the London equations are given as:

$$\text{curl } J_s = -\frac{1}{\mu_o \lambda_L^2} E$$

(2)

$$\frac{\partial J_s}{\partial t} = \frac{1}{\mu_o \lambda_L^2} E$$

(3)

where J_s is the current density of the paired electrons. The total current density is the sum of J_s and the normal electron current J_n:

$$J = J_n + J_s = (\sigma_1 - j\sigma_2)E$$

(4)

Equation 4 shows that the superconductor current density is related to the electric field by the *complex* conductivity of the superconductor. An equivalent circuit for the impedance of an incremental section of a superconductor is depicted in figure 3.
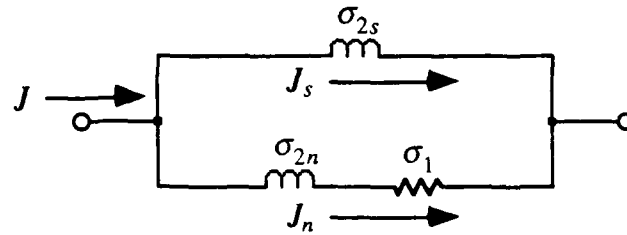
Figure 3. Superconductor Impedance Equivalent Circuit

The real and imaginary components of the complex conductivity are derived from equation 3 and a momentum relaxation equation accounting for the effect of collisions between the normal electrons. The results are given as [7]:

$$\sigma_1 = \frac{n_n e^2 \tau}{m(1 + \omega^2 \tau^2)} \qquad \sigma_2 = \frac{n_s e^2}{m\omega} + \frac{n_n e^2 (\omega\tau)^2}{m\omega(1 + \omega^2 \tau^2)}$$

(5)

where τ is the momentum relaxation time. Note that the real part of the conductivity depends only on the normal electrons. Therefore superconductors are only "lossless" at DC, and losses will result from changing fields due to the normal electrons present. At frequencies low enough

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such that $\omega^2\tau^2 < 1$ (typically less than 100 GHz), σ_1 and σ_2 can be reduced and by substitution of equation 1 we obtain:

$$\sigma = \sigma_1 - j\sigma_2 = \sigma_n(n_n/n) - j\left(1/\omega\mu_o\lambda_L^2\right) \tag{6}$$

$$\text{where} \quad \sigma_n = ne^2\tau/m \tag{7}$$

The normal state conductivity, σ_n, is related to the penetration depth and the energy gap at a temperature of absolute zero by:

$$\sigma_n = \frac{\hbar}{\pi\Delta(0)\lambda_L^2(0)} \tag{8}$$

The real and imaginary components of the conductivity can be calculated using the two-fluid model. However, the two-fluid model does not take into account energy gap effects such as electron pair splitting due to incident radiation. It has been shown that accurate calculations of the superconductor conductivity require the use of the Mattis-Bardeen theory [8] where expressions of the complex conductivity were derived from the BCS theory [9]. In general the Mattis-Bardeen theory is quite complicated, but in the extreme anomalous limit their result reduces to integral equations which can be solved numerically. These equations are given as:

$$\frac{\sigma_1}{\sigma_n} = \frac{1}{\hbar\omega}\int_\Delta^\infty [f(E) - f(E + \hbar\omega)]g(E)dE$$

$$+ \frac{1}{\hbar\omega}\int_{\Delta-\hbar\omega}^{-\Delta}[1 - f(E + \hbar\omega)]g(E)d(E) \tag{9}$$

$$\frac{\sigma_2}{\sigma_n} = \frac{1}{\hbar\omega}\int_{\Delta-\hbar\omega,-\Delta}^{\Delta} \frac{[1 - 2f(E + \hbar\omega)][E^2 + \Delta^2 + \hbar\omega E]}{\left[\Delta^2 - E^2\right]^{1/2}\left[(E + \hbar\omega)^2 - \Delta^2\right]^{1/2}}dE \tag{10}$$

where $f(x)$ is the Fermi function,

$$f(x) = \frac{1}{1 + e^{x/k_sT}} \tag{11}$$

$$\text{and} \quad g(E) = \frac{E^2 + \Delta^2 + \hbar\omega E}{\sqrt{E^2 - \Delta^2}\sqrt{(E + \hbar\omega)^2 - \Delta^2}} \tag{12}$$

6

The first integral of equation 9 represents thermally excited quasiparticles, while the second integral accounts for photon-excited quasiparticles and is zero below the gap frequency. Equation 10 for σ_2 considers the paired electrons and its lower limit is taken as $-\Delta$ at frequencies above the gap frequency ($\hbar\omega > 2\Delta$). In equation 12 the signs of the square roots are such that $g(E)$ is positive in both integrals of equation 9. The energy gap has an implied temperature dependence which can be found by solving for the root of [10, 11]:

$$\frac{\Delta(T)}{\Delta(0)} = \tanh\left[\frac{T_c}{T}\frac{\Delta(T)}{\Delta(0)}\right]$$

(13)

or approximated by [12]:

$$\Delta(T) = \Delta(0)\sqrt{\cos\left[\frac{\pi}{2}(T/T_c)^2\right]}$$

(14)

The assumption of the extreme anomalous limit is typically valid for pure elemental superconductors. The material of interest in this paper (niobium) is a London superconductor (i.e., current density at a point may be described by a constant, local field.) However, the Mattis-Bardeen theory provides the best available means to calculate the complex conductivity of a superconductor [13], and this theory has been shown to exhibit good correlation with experimental results for both niobium [14, 15] and high-T_c ceramic superconductors [16, 17]. Therefore, we will use the above Mattis-Bardeen equations to calculate the complex conductivity of superconducting niobium.

A computer program, written in FORTRAN, was used to numerically integrate the Mattis-Bardeen equations 9 through 13. A typical result showing the complex conductivity as a function of frequency is shown in figure 2. The curves shown are for niobium at a temperature of 4.2 K, where σ_1 and σ_2 are given relative to σ_n. Here σ_1 varies with frequency, which is not predicted by the two-fluid model. The London theory does predict the correct $1/\omega$ dependence of σ_2. At the gap frequency (approximately 720 GHz), note the precipitous decrease of σ_2 and the corresponding rise in σ_1. This is a result of the incident radiation having sufficient energy to split paired electrons.

The superconducting surface impedance Z_s is calculated using Maxwell's equations with the London equations and is given by [18]

$$Z_s = \frac{j\omega\mu_o}{\sqrt{j\omega\mu_o\sigma_1 + \left(1/\lambda_L^2\right)}}\coth\left[t\sqrt{j\omega\mu_o\sigma_1 + \left(1/\lambda_L^2\right)}\right]$$

(15)

We can make use of Mattis-Bardeen complex conductivity by rewriting equation 6 in the form

$$j\omega\mu_o\sigma = j\omega\mu_o\sigma_1 + \left(1/\lambda_L^2\right)$$
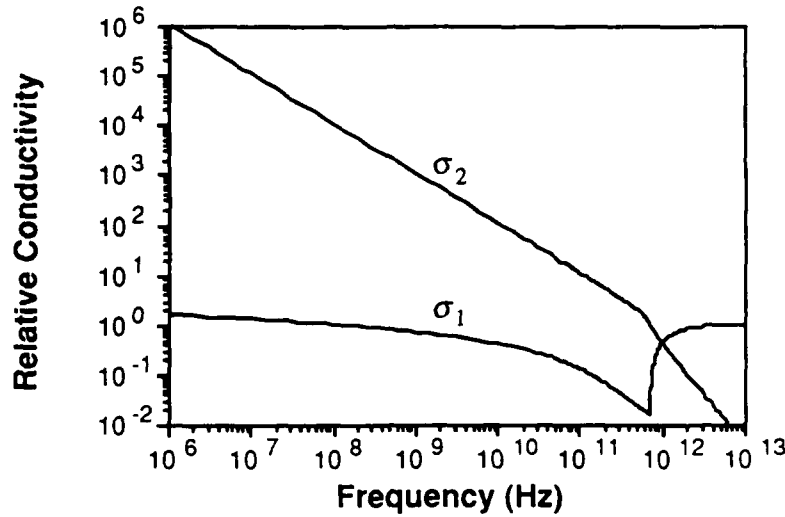
(16)

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Figure 4. Relative Complex Conductivity Versus Frequency (note: the data shown is for niobium at a temperature of 4.2 K, relative to the normal state conductivity σ_n)

and substituting it into equation 15 to yield

$$Z_s = \sqrt{j\omega\mu_o/\sigma} \coth\left(t\sqrt{j\omega\mu_o/\sigma}\right)$$

(17)

where $\sigma = \sigma_1 - j\sigma_2$ and t is the conductor metalization thickness. Figure 5 depicts the surface impedance for superconducting niobium at microwave frequencies. Note that the reactive component of the surface impedance is approximately three orders of magnitude larger than the real part. This reactive impedance is responsible for the low-loss properties of superconducting transmission lines.

Finally, we can verify the assertion that field penetration into a superconductor is less than the classical skin depth. Making use of the usual expression for skin depth

$$\delta = \sqrt{2/(\omega\mu_o\sigma_n)}$$

(18)

we can calculate and compare the skin depth of normal and superconducting metals. Figure 6 depicts the result, where the superconducting skin depth is much less than the normal state skin depth. This does not result in additional losses for the superconductor since the surface impedance is predominantly reactive. More importantly, the superconducting skin depth is independent of frequency, thereby greatly reducing material dispersion in waveguides.
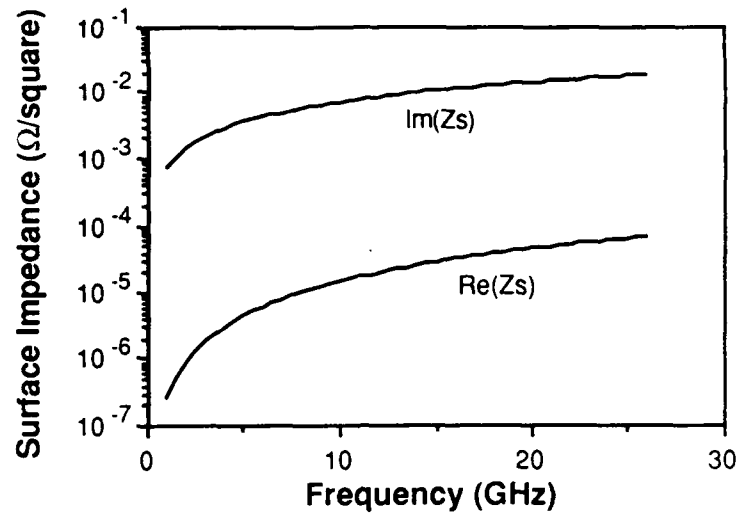
8

Figure 5. Superconducting Surface Impedance Versus Frequency (note: the data shown is for niobium at a temperature of 4.2 K. The normal state conductivity σ_n is 15.7 x 10^6 S/m)
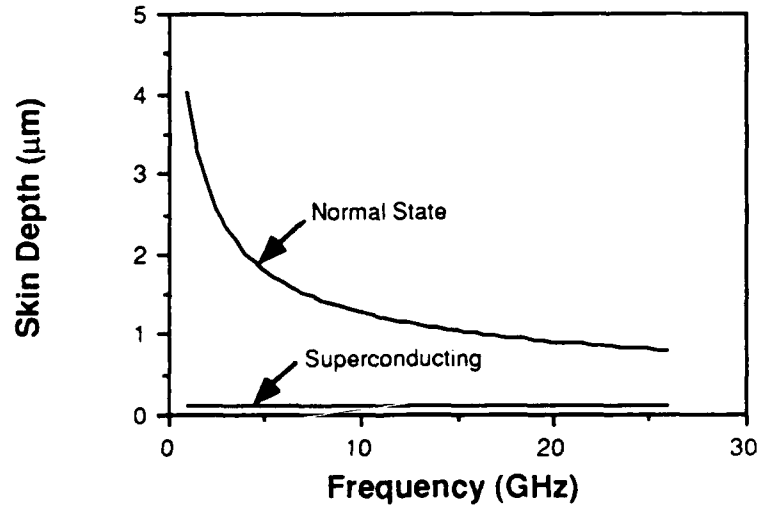

Figure 6. Superconducting and Normal Skin Depth Versus Frequency (note: the data shown is for niobium where σ_n = 15.7 x 10^6 S/m)

2.2 TRANSMISSION LINE MODELS

The physics of wave propagation on a superconducting transmission line are the same as that for normal metal waveguides. However, it was shown in the previous section that a superconductor has a fundamentally different surface impedance at microwave frequencies, where Z_s is orders of magnitude more reactive than it is lossy. This complex Z_s is calculated from the superconducting complex conductivity, which is also related to the field penetration (λ_L) in the superconductor by equation 16 above. Furthermore, losses on a superconducting transmission line are proportional to the square of frequency, in contrast to the conventional surface resistance varying as the square root of frequency. It is necessary to include all of these effects in order to accurately model superconducting transmission lines. Fortunately, this can be conveniently accomplished through the use of the complex surface impedance Z_s, calculated from the superconductor complex conductivity, in the transmission line equations from the literature.

General transmission line theory defines the propagation factor γ which describes the attenuation and phase response of a transmission line. The propagation factor is given by

$$\gamma(f) = \alpha(f) + j\beta(f)$$

(19)

where α and β are the attenuation and phase "constants," respectively. The use of the word "constant" is misleading since α and β typically vary with frequency f. The propagation factor is defined in terms of the transmission line's distributed series impedance (Z) and shunt admittance (Y), which also define the characteristic impedance (Z_o) of the transmission line. These relationships are given in equations 20 and 21.

$$\gamma = \sqrt{ZY}$$

(20)

$$Z_o = \sqrt{Z/Y}$$

(21)

The distributed series impedance and shunt admittance are functions of the transmission line geometry, and are given by

$$Z = j2\pi f \mu_o g_1 + Z_s(f)g_2$$

(22)

$$Y = 2\pi f \varepsilon_o \left(j\varepsilon_{re} + \varepsilon_r \tan \delta \right) / g_1$$

(23)

In these equations ε_o is the free space permittivity, ε_r is the relative permittivity of the dielectric, ε_{re} is a geometry dependent effective permittivity, and $\tan \delta$ is the loss tangent of the transmission line dielectric material. The factors g_1 and g_2 account for transmission line geometry, allowing the above equations to be completely general.

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The analysis of planar transmission lines (e.g., MS and CPW) is difficult because they cannot support a pure transverse electromagnetic (TEM) wave. This is a result of fringing electric field lines experiencing an inhomogeneous dielectric, leading to discontinuities in the field which cause contributions from longitudinal components. However, at low frequencies a quasistatic solution can be obtained by assuming that the lowest-order mode is approximately a TEM wave. This quasi-TEM approach is manifested in equation 23 as the effective permittivity ε_{re}, which is an average of the dielectric material and free space. Closed form expressions for the effective permittivity in MS is given by [19]

$$\varepsilon_{reo} = \tfrac{1}{2}(\varepsilon_r + 1) + \frac{\tfrac{1}{2}(\varepsilon_r - 1)}{\sqrt{1 + 12d/W}} - \frac{(\varepsilon_r - 1)(t/d)}{4.6\sqrt{W/d}} \quad \text{for} \quad W/d \geq 1 \tag{24}$$

$$\varepsilon_{reo} = \tfrac{1}{2}(\varepsilon_r + 1) + \frac{\tfrac{1}{2}(\varepsilon_r - 1)}{\sqrt{1 + 12d/W}} + 0.02(\varepsilon_r - 1)(1 - W/d)^2 - \frac{(\varepsilon_r - 1)(t/d)}{4.6\sqrt{W/d}} \quad \text{for} \quad W/d < 1 \tag{25}$$

In these expressions W is the MS width, t is the metalization thickness, and d is the dielectric thickness. These are pictorially shown in figure 1. Note that these expressions have no frequency dependence, hence the notation ε_{reo}. With increasing frequency, longitudinal field components become significant, causing the fields to become more concentrated in the dielectric and; thereby, increasing the effective permittivity. This results in modal dispersion, which is especially critical for superconducting transmission lines which have increased bandwidth by virtue of their reduced losses [20-22]. This modal dispersion can be expressed by an empirical formula as [23, 24]

$$\frac{\beta}{\beta_o} = \sqrt{\varepsilon_{re}(f)} = \frac{\sqrt{\varepsilon_r} - \sqrt{\varepsilon_{reo}}}{1 + 4F^{-1.5}} + \sqrt{\varepsilon_{reo}} \quad \text{where} \tag{26}$$

$$F = f\sqrt{\mu_o \varepsilon_o} \, 4d\sqrt{\varepsilon_r - 1} \left\{ 0.5 + \left[1 + 2\ln(1 + W/d) \right]^2 \right\} \tag{27}$$

Finally, the MS geometry dependent factors g_1 and g_2 are given in equations 28 through 34 [25].

$$g_1 = \frac{1}{2\pi} \ln\left[\frac{8d}{W_e} + 0.25\frac{W_e}{d} \right] \quad \text{for} \quad W/d \leq 1 \tag{28}$$

$$g_1 = \left\{ \frac{W_e}{d} + 1.393 + 0.667\ln\left[\frac{W_e}{d} + 1.444 \right] \right\}^{-1} \quad \text{for} \quad W/d > 1 \tag{29}$$

$$\frac{W_e}{d} = \frac{W}{d} + \frac{1.25}{\pi} \frac{t}{d} \left[1 + \ln \frac{4\pi W}{t} \right] \quad \text{for} \quad W/d \le \frac{1}{2\pi} \tag{30}$$

$$\frac{W_e}{d} = \frac{W}{d} + \frac{1.25}{\pi} \frac{t}{d} \left[1 + \ln \frac{2d}{t} \right] \quad \text{for} \quad W/d > \frac{1}{2\pi} \tag{31}$$

$$g_2 = \frac{1}{2\pi d} \left\{ 1 - \left[\frac{W_e}{4d} \right]^2 \right\} \left\{ 1 + \frac{d}{W_e} + \frac{d}{\pi W_e} \left[\ln \frac{4\pi W}{t} + \frac{t}{W} \right] \right\} \quad \text{for} \quad \frac{W}{d} \le \frac{1}{2\pi} \tag{32}$$

$$g_2 = \frac{1}{2\pi d} \left\{ 1 - \left[\frac{W_e}{4d} \right]^2 \right\} \left\{ 1 + \frac{d}{W_e} + \frac{d}{\pi W_e} \left[\ln \frac{2d}{t} - \frac{t}{d} \right] \right\} \quad \text{for} \quad \frac{1}{2\pi} < \frac{W}{d} \le 2 \tag{33}$$

$$g_2 = \frac{\left\{ \frac{W_e}{d} + \frac{\frac{W_e}{\pi d}}{\frac{W_e}{2d} + 0.94} \right\} \left\{ 1 + \frac{d}{W_e} + \frac{d}{\pi W_e} \left[\ln \frac{2d}{t} - \frac{t}{d} \right] \right\}}{d \left\{ \frac{W_e}{d} + \frac{2}{\pi} \ln \left[2\pi e \left(\frac{W_e}{2d} + 0.94 \right) \right] \right\}^2} \quad \text{for} \quad 2 < \frac{W}{d} \tag{34}$$

A computer program, written in FORTRAN, was used to calculate the propagation characteristics of superconducting microstrips to illustrate some of the properties of superconducting transmission lines, and more importantly serve as a base line for developing an experiment to verify these properties. Figure 7 shows the attenuation of a 10 µm MS line, a dielectric thickness of $d = 0.1$ µm, and fabricated from superconducting niobium. In the figure, the loss of the superconducting MS is compared with a normal state MS which is representative of either copper or aluminum metalization. Note that the loss for the superconducting MS is approximately four orders of magnitude less than that predicted for the normal state MS, albeit the superconducting losses are increasing as the square of frequency.

Figure 8 depicts the propagation constant (normalized to the free space propagation constant β_o) of a superconducting MS as a function of the dielectric thickness. This simulation illustrates an interesting feature of superconducting transmission lines which can be exploited to build compact delay lines. In the figure, note that the propagation constant is inversely proportional to the dielectric thickness, and actually becomes greater than the relative dielectric constant of the substrate (here $\varepsilon_r = 4$). This effect is due to the kinetic inductance of the paired electrons, as manifested through the superconducting complex conductivity. An essential requirement for this effect to be exhibited is the close physical proximity of two superconductors, in this case the MS conductor and its ground plane.
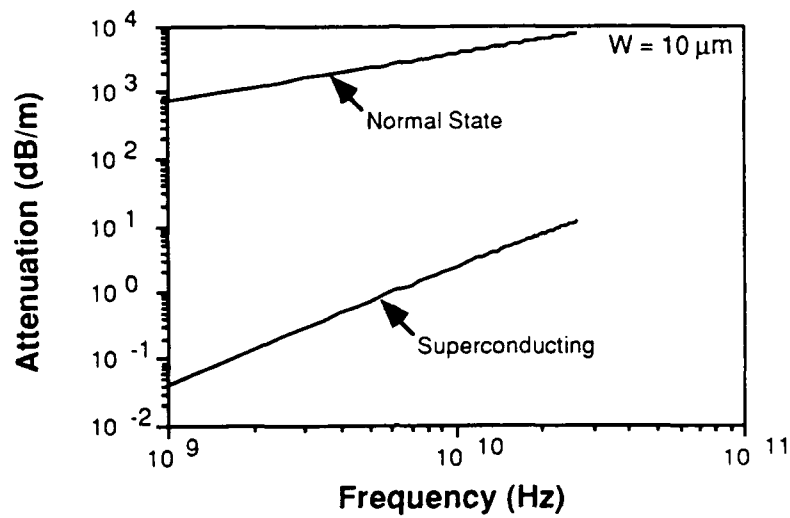
Figure 7. Attenuation as a Function of Frequency for a Microstrip Transmission Line (note: the simulation shown is for $W = 10$ μm, $d = 0.1$ μm, $t = 0.1$ μm, and $\sigma_n = 15.7 \times 10^6$ S/m)
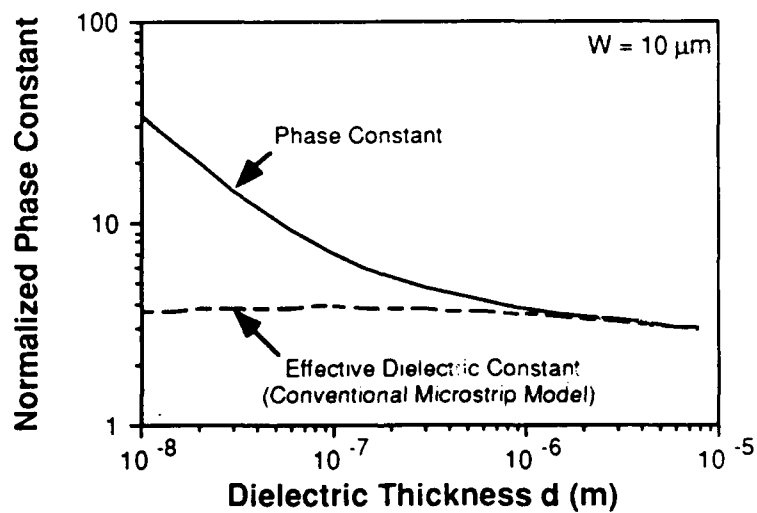

Figure 8. Microstrip Phase Constant Versus Dielectric Thickness

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Figure 9 depicts the characteristic impedance Z_o for a superconducting MS as a function of dielectric thickness. Three MS widths are shown. As described in the next section, the data in figure 9 was used to choose the impedance of a MS resonator for an experimental verification of the theories presented in this section.
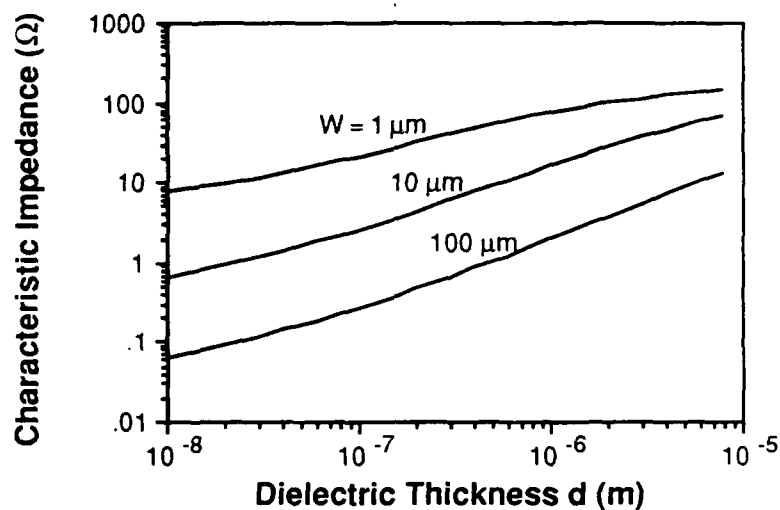
Figure 9. Microstrip Characteristic Impedance Versus Dielectric Thickness

2.3 TRANSMISSION LINE CHARACTERIZATION TECHNIQUES

In order to verify our models, a method for measuring the complex propagation factor, γ, of a microwave transmission line is required. The complex propagation factor consists of two parts. The imaginary part, β is proportional to the phase velocity on the line. The real part, α, is the attenuation constant of the line. A resonant technique should be employed to perform these measurements due to the increased accuracy of this technique as opposed to straight transmission line S parameter measurements [19]. Reflection (S_{11}) measurements or transmission (S_{21}) measurements on transmission line resonators can both be performed to determine the complex propagation constant of a transmission line.

The measurement of β requires two resonators of different lengths in order to account for the effects of reactive discontinuities on the effective resonator length. The measurement of α requires only one resonator. The measurement of α on the second resonator gives us increased measurement accuracy as the two results can be averaged.

In order to perform measurements on a resonator, the resonator must be coupled to the measurement system. This coupling must be loose so that the resonance condition is not disturbed. The coupling to the resonator must not be so loose that the reflected or transmitted signal from the resonator cannot be measured. As a general rule, about 20 dB of coupling is desired, measured away from the resonant frequency. The most widely used coupling scheme for MS and stripline resonators is to end couple through a capacitive gap. This is due to the existence of accurate models for these gaps, and the minimal effects on resonator performance. For CPW resonators, the most widely used coupling method is a feed line normal to the resonator, in the center. End coupling of CPW resonators has also been demonstrated [26].

A resonance condition exists in a transmission line section when a standing wave pattern exists which satisfies the boundary conditions at the end of the line. If the ends of the resonator are open circuited or short circuited, and the resonator is a multiple of 1/2 wavelength long, a resonance condition will exist. MS resonators are almost always implemented as open circuit sections because no via holes are necessary to achieve an open circuit. With CPW, short circuit and open circuit resonators are both easily realizable. Of the many CPW resonators described in the literature, all except one are short circuited sections. However, research by Gopinath [27] claims that open circuited CPW resonators have lower radiation losses.

The procedure for extracting transmission line parameters from resonance measurements is as follows. First, two resonators of different lengths, but identical in all other ways including coupling circuits must be fabricated. Both α and β can then be obtained from automatic network analyzer S_{11} or S_{21} measurements on these resonators.

The measurement of β involves measuring the resonant frequencies of the two resonators f_1 and f_2. For a reflection measurement, a minimum value of S_{11} is obtained at the resonant frequency. For a transmission measurement S_{21} reaches a maximum value at the resonant frequency. All of the discontinuities associated with the resonator and coupling circuits can be

represented as an effective reactance, which in turn can be modeled as a change in the line length of the resonator which is referred to as Δl_d. When the effective line length is a multiple of 1/2 wavelength, a resonance occurs. The resonant frequency, line length and effective dielectric constant are related by the equation:

$$l_1 + \Delta l_d = \frac{n_1 c}{2 f_1 \sqrt{\varepsilon_{re}}} \tag{35}$$

where l_1 is the physical length of the first resonator, n_1 is an integer, c is the speed of light in vacuum, and ε_{re} is the effective dielectric constant of the line. Similarly for the second resonator:

$$l_2 + \Delta l_d = \frac{n_2 c}{2 f_2 \sqrt{\varepsilon_{re}}} \tag{36}$$

These two equations can be solved simultaneously for ε_{re} and Δl_d. β is related to ε_{re} by the simple relation:

$$\beta = \omega \sqrt{\mu_o \varepsilon_o \varepsilon_{re}} \tag{37}$$

where ω is the resonant angular frequency. The measurement assumes that there is no dispersion (i.e., the transmission line parameters, and Δ_{ld} are the same at both resonant frequencies). This will not be a problem if the two different resonators lengths are fairly close to each other (within 1/10th of a wavelength at the resonant frequency) or if the resonator lengths differ by a multiple of 1/2 wavelength at the frequency of interest giving them approximately the same resonant frequency.

The main source of error in the attenuation measurements is radiation losses associated with the open end discontinuities of the resonator. There are two solutions to this problem. The first is to shield the resonator in a hollow metallic waveguide with a cutoff frequency above the desired measurement range. This will cause the resonator radiation to couple to evanescent modes in the waveguide which are reflected back into the resonator and are not lost. The second method for avoiding errors due to radiation is to use existing models for the radiation at open ends and subtract this from the measured loss. Radiation models for MS open ends and coplanar open ends exist in the literature [28]. Although we are concentrating on MS in this paper, it is important to note that this resonant technique can be used to analyze any type of transmission line provided the radiation losses can be accounted for. No closed form approximations exist to model the radiation effects in CPS, however an electromagnetic (EM) simulator could be used to model these effects. The radiation problem is greatly reduced in stripline geometry which does not have higher order radiation modes. The stripline technique is the most widely used to date in the measurement of the very small attenuation constants associated with superconducting transmission lines.

The quality factor (Q) of a resonator is defined as the product of the resonant frequency and the energy stored in the resonator, divided by the average power loss in the resonator. For the α

measurement the unloaded Q of each resonator must be measured. The unloaded Q is the Q associated only with losses in the resonator. The unloaded Q of a resonator consists of three components, Q_c associated with conductor losses, Q_d associated with dielectric losses, and Q_r associated with radiation losses. The total unloaded Q is related to these components by

$$\frac{1}{Q} = \frac{1}{Q_c} + \frac{1}{Q_d} + \frac{1}{Q_r}$$ (38)

The loaded Q factor includes losses associated with the external coupling circuit. Each resonator used in the β measurement will yield an independent measure of Q near its resonant frequency. There are two methods for doing this. Both methods will de-embed the effects of the coupling circuit, but not any radiation effects associated with the resonator itself. The two attenuation measurement techniques were proposed by Kajfez [29] and Ginzton [30]. These methods are described below.

The first method is proposed by Ginzton. This method can be utilized on both reflection or transmission measurements. For a transmission measurement, the frequencies on either side of resonance which have transmission 3 dB below the resonance level are found and labeled F_a and F_b. The loaded Q is then given by the equation

$$Q_l = \frac{F_r}{F_a - F_b}$$ (39)

where F_r is the resonant frequency. The coupling coefficient, k associated with the transmission resonator is given by

$$k = \frac{|S_{21\ max}|}{2(1 - |S_{21\ max}|)}$$ (40)

Once the coupling coefficient is determined, the unloaded Q can be obtained from

$$Q = Q_l(1 + 2k)$$ (41)

The use of Ginzton's method for reflection measurements is slightly more complicated because the return loss at resonance is usually within 3 dB of the return loss away from resonance. Ginzton has chosen to use Voltage Standing Wave Ratio (VSWR) measurements to find the half power points on the resonance curve. The frequencies at the half power points on the VSWR curve are defined as F_a and F_b. The VSWR at these points is given by the expression:

$$VSWR_{a,b} = \frac{2 + y^2(1 + z^2) + \sqrt{4 + y^2(1 + z^4) - 2zy^2(4 - zy^2)}}{2y(1 + z)}$$ (42)

In this procedure three new parameters, x, y, and z are defined using VSWR measurements. y is defined as 1/(VSWR at resonance), x is given by 1/(VSWR away from resonance) and z is x/y. The unloaded Q of the resonator is given by

$$Q = F_r/(F_b - F_a). \tag{43}$$

The second method for finding the unloaded Q of a resonator is a graphical procedure proposed by Kajfez [30] which utilizes reflection measurements. This procedure relies on the fact that the reflection response(S_{11}) of a resonator traces approximately a circle on the Smith Chart as the frequency is swept through resonance. this is illustrated in figure 10. The point on the circle closest to the center of the Smith Chart is the resonant frequency and this is defined as point 3. The diameter of the circle (D) is a function of the coupling efficiency. Points 1 and 2 and their corresponding frequencies f_1 and f_2 are found by picking two points on the circle some arbitrarily small angle ϕ away from resonance. These two points on the Smith Chart are located at the positions:

$$\Gamma_{1,2} = (\frac{|\Gamma_r|+1}{2})e^{i\theta_r} + (\frac{|\Gamma_r|+1}{2})e^{i(\theta_r \pm 2\phi)} \tag{44}$$

The loaded Q can now be found by the expression:

$$Q_l = \frac{f_r}{f_2 - f_1}\tan\phi \tag{45}$$

The coupling coefficient k can be found from:

$$k = \frac{1 - |\Gamma_r|}{1 + |\Gamma_r|} = \frac{D}{2 + D} \tag{46}$$

and the desired unloaded Q is given by

$$Q = Q_l(1+k). \tag{47}$$

The factor of two which is found in equation 41 and not in equation 47 was removed because this is a reflection measurement and only one port is involved.
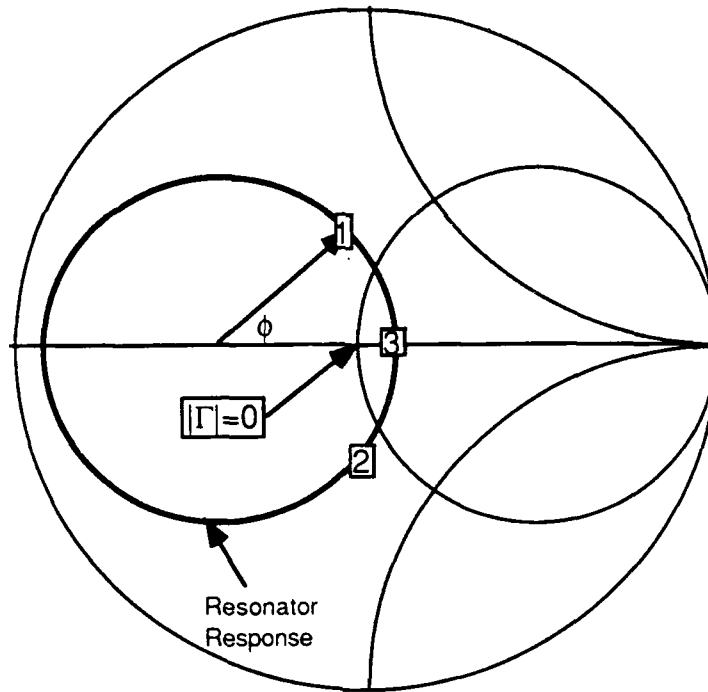
Figure 10. Reflection Coefficient of a Resonator Plotted on the Smith Chart

The attenuation constant can be determined from the phase constant, β, and the unloaded Q of the resonator as

$$\alpha = \frac{\beta}{2Q} \tag{48}$$

It is important to remember that this attenuation constant includes the effects of any radiation from discontinuities in the resonator itself. Due to the resistance free properties of the superconducting transmission lines, the attenuation constant will be extremely small, resulting in very high Q resonators.

SECTION 3

PROPOSED EXPERIMENTS

In this section we describe experiments which have designed in order to measure the transmission line parameters of superconducting transmission lines using the resonant technique described in section 2.3.

3.1 NORMAL CONDUCTOR RESONATOR MEASUREMENTS

In order to use the techniques described in section 2.3, we must be able to accurately measure the resonant frequency and quality factor of a transmission line resonator. In order to determine the accuracy of our measurement system and simulation tools, preliminary simulations and measurements on non-superconducting MS resonators fabricated on duroid substrates were performed. The resonators and feed circuits were modeled using both Supercompact and Sonnet software's EM simulator. In order to minimize fabrication costs, two resonators were fabricated on the same substrate. Reflection type resonators were chosen so that a minimum of connectors would be required.

The circuit used in this experiment is shown in figure 11. The circuit consists of two MS resonators with different lengths and identical feed structures. This structure was chosen because it can be modeled using both Supercompact and Sonnet, and can be packaged in our existing test fixture. Measurements were made using a Wiltron 360 automatic network analyzer. Results from each of the simulations and the experiment are summarized in table 1. Note that the Sonnet simulations are designated "EM." The resonant frequencies predicted by Sonnet agreed very well with the measurement. The Supercompact simulation was considerably less accurate. Neither simulation was accurate in predicting the Q of the resonators.

Sonnet's EM simulator has an option of using corner fill to subsection the rectangles, and they recommend using this feature whenever capacitive coupling is to be analyzed. With corner fill, Sonnet was able to predict the resonant frequency very accurately. Supercompact does provide a close approximation, and is much quicker to calculate data. Sonnet takes about ten minutes per frequency point calculation, while Supercompact takes about two seconds. Neither of the simulators was able to predict the Q of the resonator closely. This is probably due to surface roughness and impurities in the metalization. The difference between the simulated Qs is due to the fact that Supercompact does not model the radiation from open end discontinuities. The difference between the Supercompact and Sonnet result provides an indication of the magnitude of the error caused by radiation effects.

The results of this preliminary study were extremely encouraging. The measurements of duroid MS resonators confirmed the effectiveness of our experimental technique. We have gained confidence in Sonnet software's ability to accurately simulate resonator circuits. This will

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Table 1. Simulated and Measured Data for the Duroid Resonators

Summary of Results				
	Measured	Super Compact	EM, with corner fill	EM, without corner fill
Q of 300 mil resonator	103	263	220	240
Q of 252 mil resonator	103	202	198	281
F_{res} of 300 mil resonator	6.75 Ghz	6.847Ghz	6.79Ghz	7.005Ghz
F_{res} of 252 mil resonator	7.932 Ghz	8.034Ghz	7.935Ghz	8.165Ghz
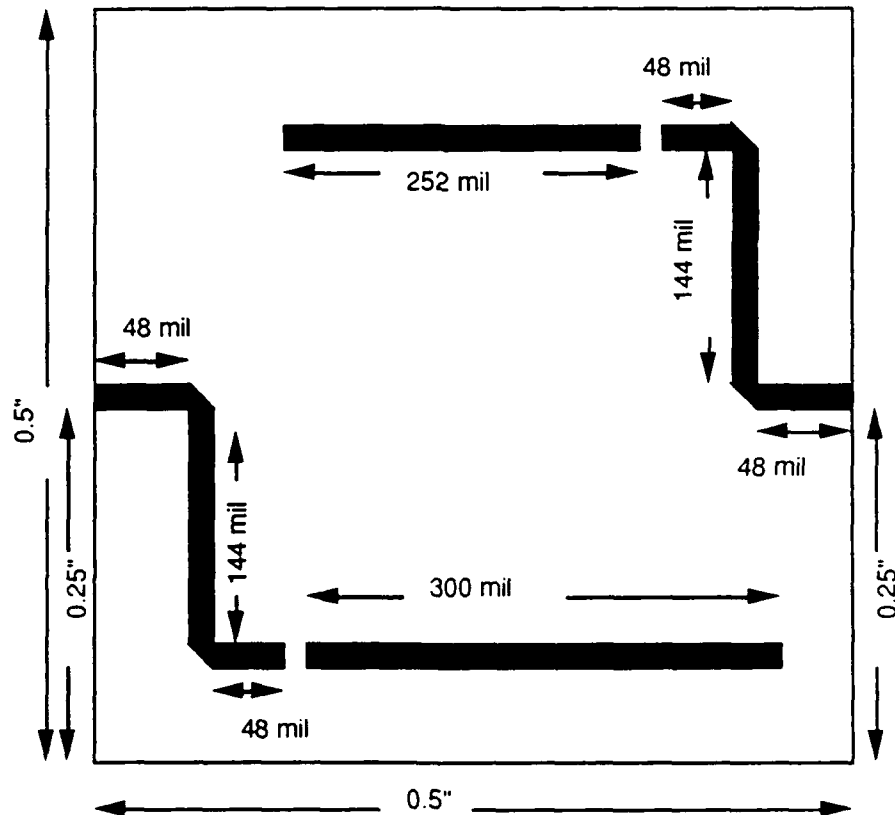
Line widths are 24 mil everywhere; both gaps are 6 mil.

Figure 11. Microstrip Resonator Test Circuit

be important as the design of our superconducting resonator circuits are based on simulations performed with Sonnet.

Measurements of actual superconducting resonators will be considerably more difficult to achieve. This is due to the very low losses of superconductors which will result in large resonator Qs. At DC, a superconductor has zero resistance, however at RF frequencies the resistance increases as the square of the frequency. At microwave frequencies (1 - 20 GHz) the surface resistance of superconducting niobium is about three orders of magnitude smaller than copper. The highest reported Q for a superconducting resonator is 5×10^4 [31], although our niobium resonators should have Q factors much lower than this due to surface roughness and impurities. With the 100-KHz accuracy of our Wiltron network analyzer we can measure Q factors up to 10^5. The HP 8510 network analyzer has an HP8341 synthesizer with 1 Hz accuracy which will resolve a Q factor of 10^{10} at 10 GHz.

A potential problem which became obvious during the normal conductor measurements is the low value of return loss, even at the resonant frequency. The copper/duroid resonators had a return loss of about 5 dB at resonance which was very easy to resolve from other noise associated with the system. If the reflection losses of superconducting resonators are two orders of magnitude lower than the copper resonators, it may be impossible to detect the resonance above the noise floor of the system. This problem could be avoided by using a transmission measurement, optimizing the coupling, providing matching circuits, and by de-embeding inside the test fixture through attachment of the calibration standards within the dewar. We did not test a transmission resonator made from normal conductors because we have shown that we can accurately simulate resonator performance and it was not necessary to fabricate another circuit.

3.2 SUPERCONDUCTING TRANSMISSION LINE GEOMETRY

As shown in section 2, the effective dielectric constant of a superconducting transmission line can be made greater than the dielectric constant of the material used for the transmission line. This will only occur if the kinetic inductance effects of the superconducting material are much greater than the normal inductance effects of the transmission line. To accomplish this, a majority of the magnetic field must be contained within the superconductor. In order to confine the magnetic fields to the superconductor, and not the dielectric, the two conductors of any TEM or quasi-TEM transmission line must be extremely close.

This restriction of conductor spacing limits the types of practical lines that can be fabricated with existing photolithography. In superconducting MS, kinetic inductance does not have a significant effect on the propagation constant unless the dielectric thickness is on the order of 0.1 μm or less. Fabrication of 0.1-μm SiO_2 dielectric layers is routinely accomplished without pinholes which would short a MS line. CPW and CPS transmission lines are not practical for this application due to the extremely small gaps that would have to be photolithographically defined. For this reason we have chosen to concentrate our study exclusively on MS transmission lines.

The use of a very thin dielectric imposes some restrictions on the measurement techniques available for this study. According to our models, MS lines of reasonable width have very low characteristic impedances. A 50-μm wide line with a 0.1μm dielectric has a characteristic impedance of 0.5 ohms . A 5-μm wide line has a characteristic impedance of 4 ohms. Lines smaller than this which extend for a few mm are not practical to fabricate with existing photolithography technology.

Coupling to thin MS lines from a 50-ohm coaxial measurement system is a challenging engineering problem. In the duroid substrate experiment, coupling through a capacitive gap was used. This technique is not possible with thin dielectric MS as shown in figure 12. The field lines extend at most 1 μm away from the edge of a MS with 0.1-μm dielectric thickness [32]. A gap any bigger than 1 μm will provide very little coupling. This was verified with Sonnet software's EM simulator. In the simulation, a 100-μm wide MS line on a 0.1-μm substrate was coupled to another line through a 1-μm gap. The coupling was less than -60 dB. The limits of photolithography prevent us from making a gap small enough to provide any significant coupling to a resonator.
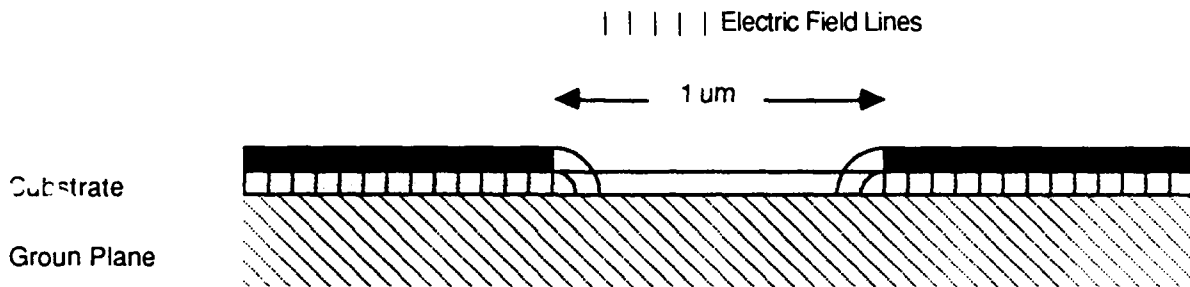
Figure 12. Gap Coupling in Thin Dielectric Microstrip

Any coupling scheme that is used will need to account for a large mismatch in impedance as well as an extreme change in line geometry. At microwave frequencies, our goal will not be a perfect match since this will be extremely difficult to achieve. Instead the goal of the coupling scheme should be to transfer enough power to the MS line to allow us to measure the desired quantities (resonant frequency and Q factor). In the measurement technique outlined above, both reflection and transmission resonator methods are presented. Reflection measurements will not be practical for kinetic inductance MS. Due to line discontinuities most of the incident power will be reflected back to the source before it gets to the resonator. A reflection measurement will have to discriminate a small resonance from a large reflected signal. For this reason transmission measurements such as Ginzton's method should be employed to characterize superconducting transmission lines.

After abandoning the gap coupling technique, we have developed two methods for achieving the desired coupling. The two methods are impedance mismatch coupling and dielectric step coupling. Impedance mismatch coupling is simpler to implement, but produces reduced accuracy. Impedance mismatch coupling is described below and the stepped dielectric coupled resonator is described in section 3.3.

Impedance mismatch coupling utilizes the impedance mismatch between the measurement system and the resonator as a loose coupling mechanism. This technique has been successfully utilized by Pond [2] in a measurement of kinetic inductance MS lines. This method would involve measurements on relatively wide (10 - 100 μm) lines which would be coupled by a precision coax to MS adapter such as a Wiltron beaded K connector as shown in figure 13.
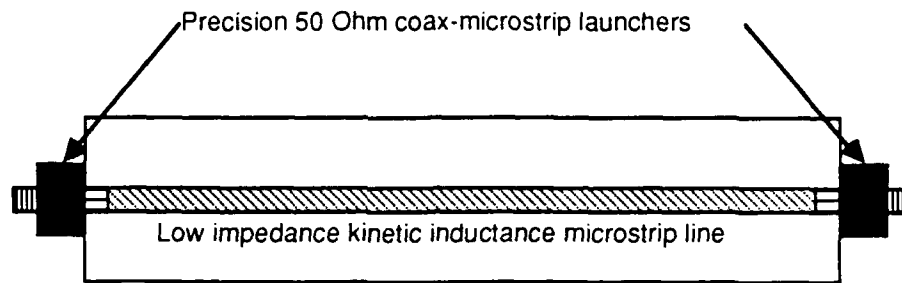
Figure 13. Impedance Mismatch Coupled Resonator

The impedance mismatch technique described above will have sufficient accuracy for our purposes. The length of the resonator is defined by the positioning of the MS launchers. The measurement technique relies on being able to accurately define the length of the resonator. Recall that for the phase velocity (β) measurement, two resonators of different lengths are required. The two simultaneous equations to be solved for the effective dielectric constant are given by 2.35 and 2.36 where l_1 is the physical length of the first resonator, n_1 is an integer, c is the speed of light in vacuum, and e_{re} is the effective dielectric constant of the line. Similarly for the second resonator l_2 is the length and n_2 is its resonant mode number. These two equations can be solved simultaneously for ε_{re} and Δl_d. The equation for ε_{re} is given by:

$$\varepsilon_{re} = \left\{ \frac{c}{2(l_1 - l_2)} \left[\frac{n_1}{f_1} - \frac{n_2}{f_2} \right] \right\}^2 \tag{49}$$

Errors occur due to inaccuracies in the measurement of $l_1 - l_2$. The accuracy of this measurement can be greatly improved by choosing n_1 different from n_2. If $n_1 = 1$ and $n_2 = 2$

(*i.e.*, the first resonator is 1/2 wavelength long and the second resonator is a full wavelength long) then $l_1 - l_2$ is a much larger value and the small error in resonator length due to the launcher is not as significant. Using different resonant modes will improve the accuracy of this measurement significantly. This will be demonstrated later in the next section.

One potential problem with the impedance mismatch technique is that the extremely thin substrate will puncture easily when the connector is attached. If the substrate is punctured, the transmission line could become shorted. Pond has avoided this problem by cutting out a small hole in the ground plane in the area where the connector is to be attached. At 500 MHz this discontinuity lowers the coupling coefficient by about 1 dB. It is our goal to make measurements at frequencies as high as 10 GHz. In order to avoid undesired radiation or reflections, the hole in the ground plane should be kept much smaller than a wavelength. At 10 GHz, a 2-mm hole will be less than 1/7th of a wavelength on a SiO_2 substrate. This should be small enough that any errors can be removed with the measurement techniques described above.

The final design for the impedance mismatch resonator measurement circu: will consist of two MS lines of 100-μm width, deposited on a 0.1 μm thick substrate. The two resonator lengths are 1.1 and 0.55 cm and should resonate at approximately 10 GHz.

3.3   DIELECTRIC STEP COUPLED RESONATOR

Due to the potential risk involved with the impedance mismatch coupled resonator, and its limited accuracy, we have designed a second resonator coupling mechanism. This coupling mechanism is described in section 3.3.1. If an impedance step is not used, it becomes necessary to match a low impedance MS to a high impedance coax through a transformer of some sort. The transformer must have a flat broad band frequency response near the resonant frequency we are trying to measure. A sinusoidal or a Dolph-Chebyshev impedance taper will be suitable for this purpose [33]. Section 3.3.2 describes a method for realizing this transformer. In section 3.3.3 we present the results of simulations which were performed to insure that substrate resonances in our circuits would not interfere with our measurements.

3.3.1   Resonator Design

In this section, the dielectric step coupled resonator is described. Many possible coupling methods were simulated using Sonnet software. It was found that coupling through a step in line width or through an abrupt CPW-MS transition would not produce a measurable level of coupling. It was found that the best results were obtained by a change in dielectric thickness. If we couple a line with a dielectric thickness of 0.2 μm to a line with a common ground plane and a dielectric thickness of 0.1 μm, the desired loose coupling is achieved. This overlap coupling is shown in figure 14.

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Connection to
SMA Launchers

Section C

Section B   Section A

(a) Perspective View

Overlap

Overlap Thickness

Dielectric Thickness

Ground Plane
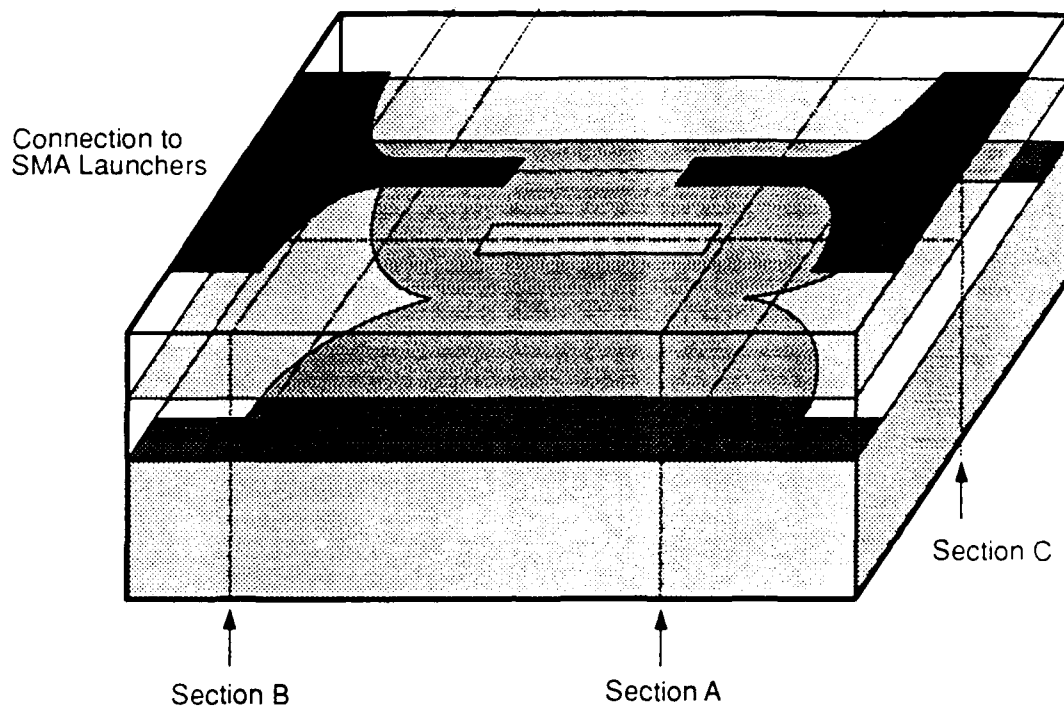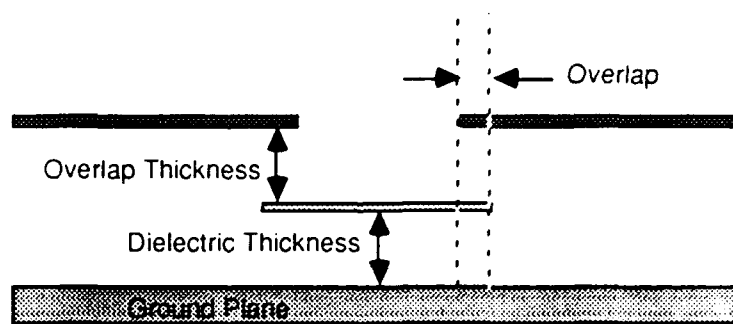
(b) Section C Cross-Sectional View

Figure 14. Geometry of a Dielectric Step Coupled Microstrip Resonator

A simulation of dielectric step coupling was performed using Sonnet software. Two different width resonators were simulated. The resonator widths are 10 and 100 μm, and the dielectric thickness and overlap thickness is 0.1 μm in both cases. The overlap length is 100 μm for both resonators. Using our models, the resonant frequency is designed to be 10 GHz. Figure 15 shows a simulation of the frequency response of two different width, 0.57-cm long resonators coupled to their test ports by dielectric steps. The 100-μm wide resonator has a higher Q factor but is not coupled as well as the 10-μm resonator. These simulations show that dielectric step coupled resonators will produce the desired response. Based on these simulations we determined that the optimum overlap thickness is equal to the dielectric thickness. The dielectric thickness was chosen as 0.1 μm because this is the smallest thickness which can be deposited without pinholes.
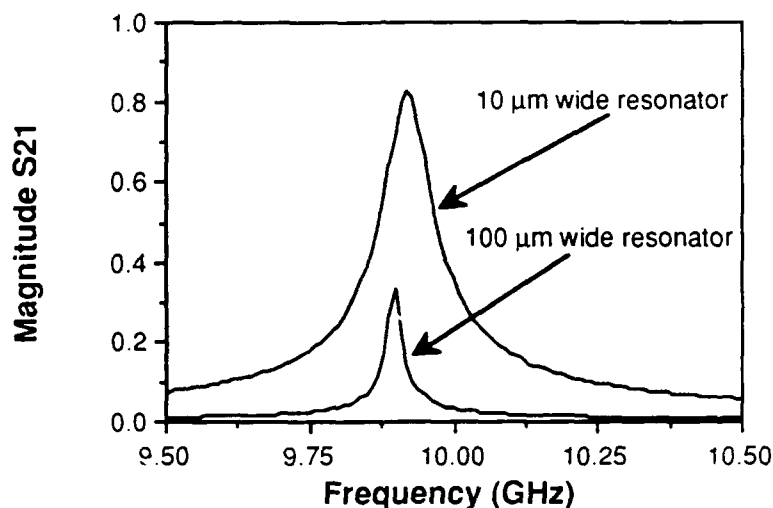
Figure 15. Frequency Response of Dielectric Step Coupled Resonators

The coupling mechanism is not completely understood. Some of the coupling is due to the overlap of the TEM modes in the two substrate regions. However, there is an additional coupling mechanism between the magnetic fields propagating in the superconductors themselves. Pond [32] has done some preliminary work to investigate this effect.

Due to the unknown nature of the coupling, the effective change in resonator length must be assumed to be a function of frequency. As discussed before, this can be corrected by using a full wavelength resonator and a half wavelength resonator. The resonant frequency will be almost the same and the line length difference will be large compared to the change in effective

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line length due to the coupling. Three resonators were designed to resonate near 10 GHz using our model for propagation constant and simulated using Sonnet software. The width of all three were kept constant at 100 μm, and the dielectric thickness was set to 0.1 μm. The lengths were 0.55 cm, 0.57 cm, and 1.1 cm. The simulator predicted resonant frequencies of 10.23 GHz, 9.9 GHz, and 10.26 GHz. Using equation 3.1 with $n_1=n_2=1$, simulations on the 0.55 cm and 0.57 cm resonators compute an effective dielectric constant of 5.97. The 0.55 cm and 1.1 cm resonators with $n_1=1$ and $n_2=2$ yield an effective dielectric constant of 7.11 which is much closer to the value of 7.2 predicted by our model.

3.3.2 Impedance Matching Network

In order to measure the stepped dielectric resonator, a matching circuit is necessary. This matching network will create an interface between the low impedance resonator and a 50-ohm measurement system. The circuit designed is a tapered transmission line with a continuous impedance profile. At the input and output of the transformer are the 50-ohm measurement system and the 4.5-ohm resonator, respectively. In order to couple to the resonator, the low impedance end of the transformer should be MS. Since the thin film networks to be fabricated have no substrate via holes, MS will not be suitable for the high impedance end of the transformer. Instead, the high impedance end of the line will be implemented with CPW. This will allow an interface to 50-ohm SMA launchers. Thus, in addition to transforming from 50 ohms to a few ohms, the matching circuit must also physically change from CPW to MS.

3.3.2.1 Physical Transformation

A method to physically change from a high impedance CPW to a low impedance MS has been demonstrated [33]. This method is compatible with the resonator circuits to be fabricated. Figure 2 shows a cross-sectional view of CPW. Figure 1 shows a cross-sectional view of MS. To make these two sections physically compatible, the center metal of the CPW is placed above the dielectric layer (see figure 16, which corresponds to section B as shown in figure 14(a)). As long as the horizontal dimensions are much larger than the vertical dimensions, the CPW models will still accurately describe this structure. Thus, S, the top plate width, and W, the gap, must be much larger than d, the dielectric thickness, and t, the metal thickness. The characteristic impedance of the CPW can be varied by changing S and W.

To allow more flexibility in the impedance values of the MS, and to smoothly transition to the CPW section of the transformer, a gap is introduced in the ground plane, as depicted in figure 17 (note that is drawing corresponds to section A of figure 14(a)). Comparing figures 16 and 17, it is seen that the top plate, dielectric layer, and ground plane are all consistent throughout the taper.
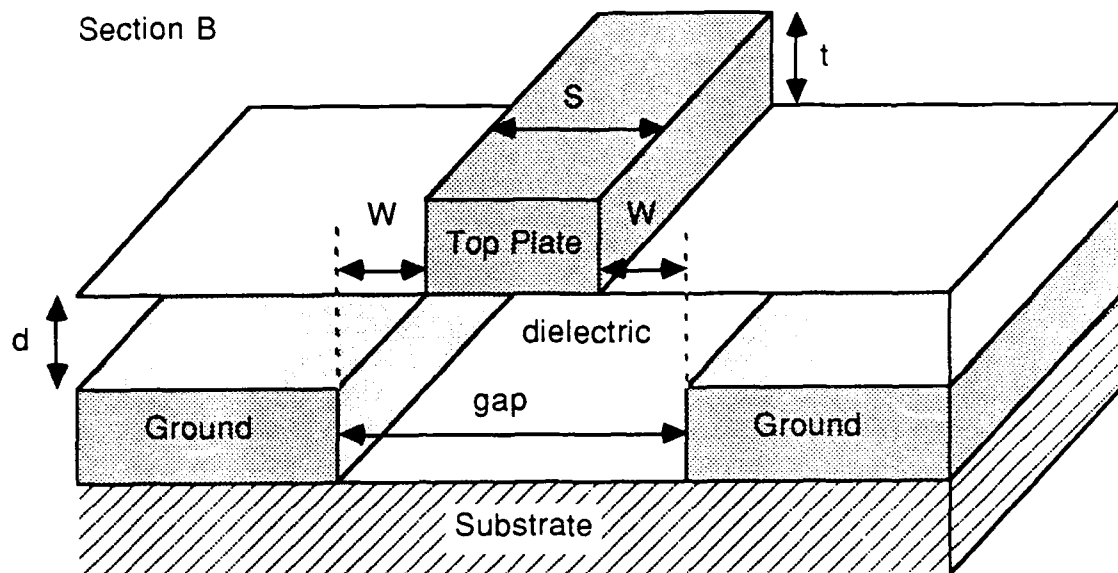
Section B

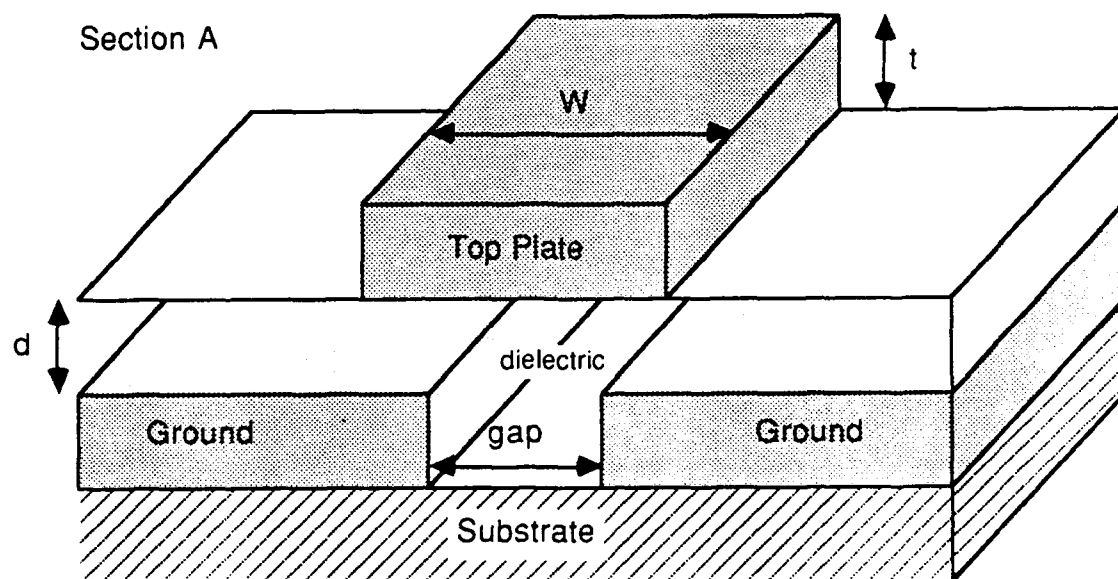Figure 16. Modified Coplanar Waveguide

Section A

Figure 17. Microstrip with Gap in Ground Plane

The transformer will have a CPW high impedance region and a MS low impedance region. The CPW region occurs when the gap is larger than the top plate width. The MS region occurs when the gap is smaller than the plate width. In addition, there will also be a transition region, where the top plate and gap widths are close to the same value, where neither the CPW or MS models are valid.

3.3.2.2   Electrical Transformation

To change the impedance of the CPW and MS, the top plate and gap widths are varied to give a smooth impedance transformer. Four impedance profiles are considered, a linear, an exponential, a Dolph-Chebyshev, and a sinusoidal. These are all characterized by the impedance along the taper as a function of position. For the linear taper,

$$Z(x) = \frac{Z_2 - Z_1}{L} x + Z_1 \tag{50}$$

for the exponential taper, [34]

$$Z(x) = Z_1 \exp\frac{x}{L} \ln\frac{Z_2}{Z_1} \tag{51}$$

for the Chebyshev taper, [33]

$$Z(x) = Z_1 \exp\{\frac{1}{2} \ln\frac{Z_2}{Z_1}[\sin(\pi(\frac{x}{L} - \frac{1}{2})) + 1]\} \tag{52}$$

and for the sinusoidal taper,

$$Z(x) = \frac{Z_1 - Z_2}{2} \cos(\pi\frac{x}{L}) + \frac{Z_1 + Z_2}{2} \tag{53}$$

where L is the length of the taper, x is the position along the taper, Z_1 is the impedance at $x=0$ (the input impedance), Z_2 is the impedance at $x=L$ (the output impedance), and $Z(x)$ is the impedance at the point x.

Figure 18 is a plot of impedance versus position (x) along the taper for all four profiles. The length used is 10,000 μm, Z_1 is fifty ohms, and Z_2 is 4.5 ohms. Note that once either the position or impedance is specified, the other parameter is uniquely determined.

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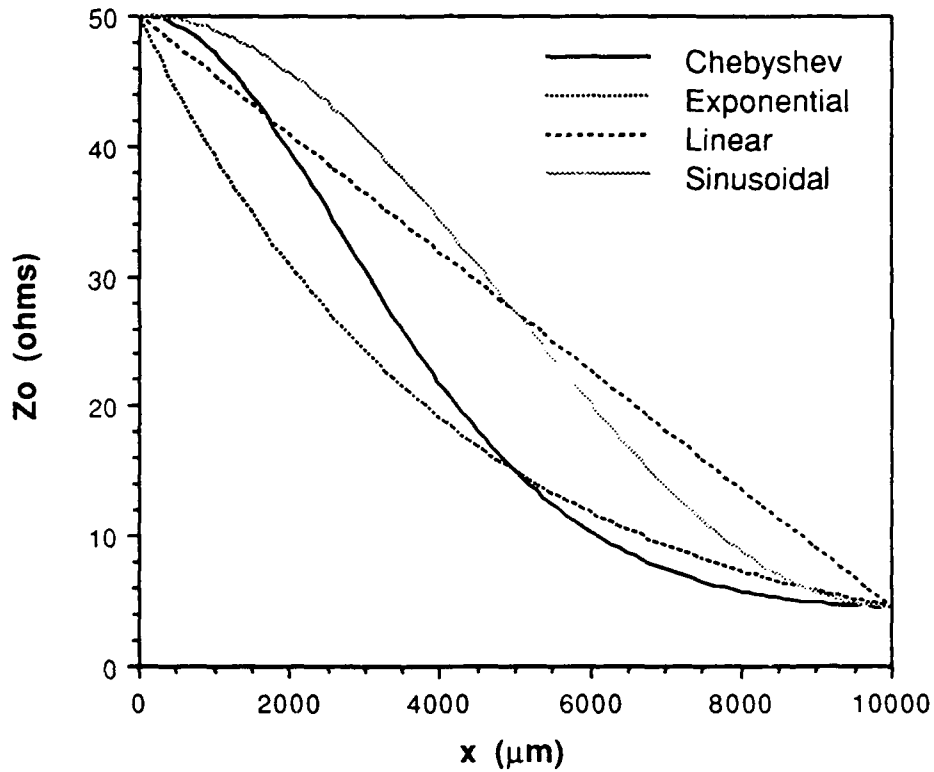
Figure 18. Plots of Impedance Versus Position for the Four Taper Profiles.

3.3.2.3 Initial Analysis

Except at very low frequencies, the transmission line taper acts like a high-pass filter with a cut-off frequency of [33]

$$f_c = \frac{cv_r}{2L} \qquad (54)$$

where c is the speed of light in a vacuum and v_r is the relative velocity in the transmission line. For example, a relative phase velocity of 0.50 and a taper length of 10 mm gives a cut-off frequency of 7.5 GHz. This length of 10 mm is suitable for use with the resonator, which is

designed for 10 GHz and above. Furthermore, a 10-mm taper is a reasonable length for a superconducting test circuit.

To initially compare the four profiles, a microwave CAD program (Super-Compact) was used to simulate the tapers. This was accomplished by splitting each taper into a number of linear tapers, an element available in the simulator. This element has an output impedance, an input impedance, a length, and a phase velocity. If enough linear components are used, the Chebyshev, exponential and sinusoidal transformers can be accurately modeled.

A FORTRAN program was written to automatically create Super-Compact netlists for the four types of transformers. Inputs to this routine are the length of the transformer, the number of linear tapers to use, the input and output impedances of the transformer, and the phase velocity. The output from the program is a circuit file formatted for use with the microwave CAD program. The length of each linear taper is the total length divided by the number of tapers. The input and output impedances are calculated from the corresponding position along the transformer.

As a preliminary demonstration, a transformer circuit for each impedance profile is simulated. The transformers analyzed are ten millimeter tapers, each split into 100 linear tapers, with an input impedance of 50 ohms and an output impedance of 4.5 ohms. A phase velocity of fifty percent is assumed. The circuit simulated consists of the 50- to 4.5-ohm transformer, a delay line, and a 4.5-to-50-ohm transformer. The delay line is a 4.5-ohm, 10-mm transmission line with a phase velocity of 0.50. This circuit is similar to a structure that will actually be fabricated to test the transformer, ie, a taper to transform to a resistance below ten ohms, a low impedance superconducting transmission line, and another taper to transform back to fifty ohms. Figure 19 shows the insertion loss of all four transformers.
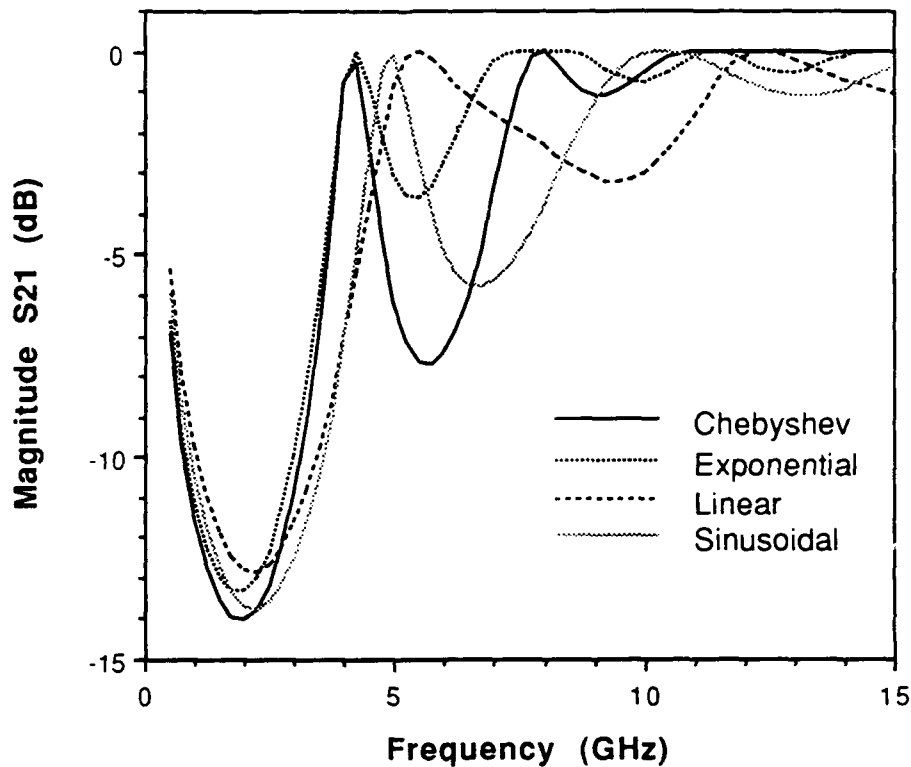
Figure 19. Responses of Four Transformers Using 0.50 Phase Velocity

Figure 19 shows that the linear taper has the greatest insertion loss in the frequency range of interest. In the 10-GHz region, the Chebyshev, exponential and sinusoidal responses are similar. The Chebyshev taper has the flattest passband (*i.e.*, above 10 GHz) response. Another important parameter is the reflection coefficient; the magnitude of S_{11} should be as small as possible. S_{11} is shown in figure 20. The linear taper has the worst performance; it is difficult to distinguish among the other three transformers.
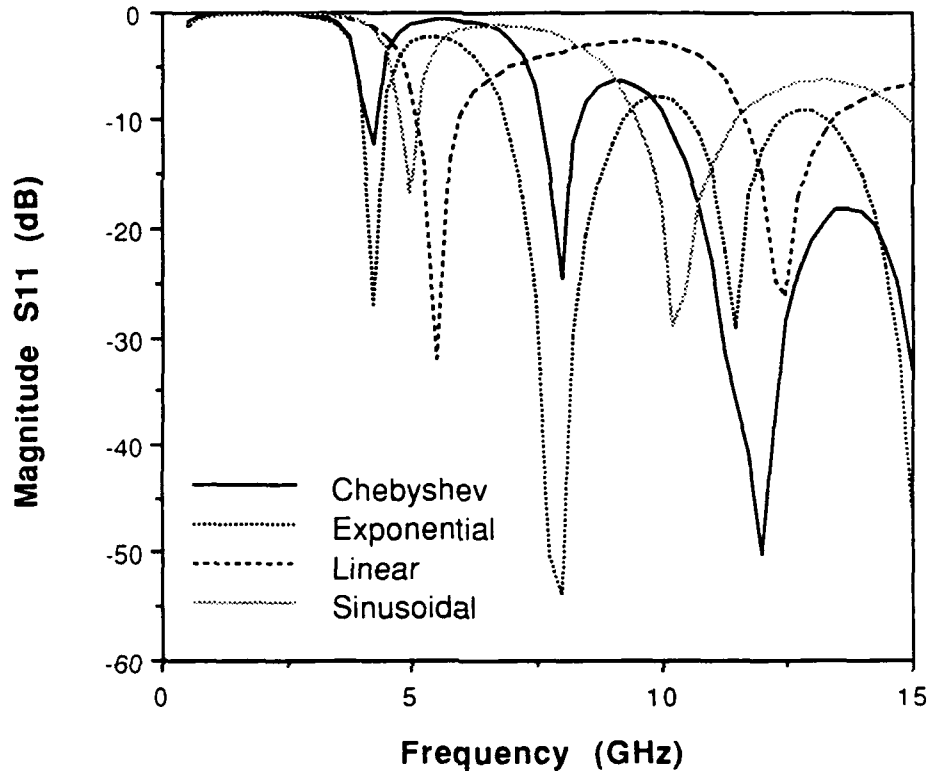
Figure 20. Reflection Coefficient of Four Transformers Using 0.50 Phase Velocity.

3.3.2.4 Transmission Line Parameters

To physically realize the desired impedance profile, the top plate and gap widths are varied. In the CPW region, the characteristic impedance of the line is given by [19]

$$Z_o = \frac{30\pi}{\sqrt{\varepsilon_{re}}} \frac{1}{G_1} \tag{55}$$

ε_{re} is the effective dielectric constant of the line. G_1 is the complete elliptic integral of the first kind, approximated by [19]

$$G_1 = \pi \left\{ \ln\left[2\frac{1+\sqrt{k'}}{1-\sqrt{k'}} \right] \right\}^{-1} \quad \text{for} \quad 0 \leq k < \frac{1}{\sqrt{2}} \tag{56}$$

$$G_1 = \pi^{-1} \ln\left[2\frac{1+\sqrt{k'}}{1-\sqrt{k'}} \right] \quad \text{for} \quad \frac{1}{\sqrt{2}} \leq k \leq 1 \tag{57}$$

where

$$k = \frac{S}{S+2W} \quad \text{and} \quad k' = \sqrt{1-k^2} \tag{58}$$

The quasistatic value of the effective dielectric constant of the line is given by [19]:

$$\varepsilon_{reo} = \frac{\varepsilon_{rs}+1}{2}\left[\tanh\left\{ 1.785\log\frac{h}{W}+1.75 \right\} + \frac{kW}{h}r \right] \tag{59}$$

and

$$r = \{0.04 - 0.7k + 0.01(1.0 - 0.1\varepsilon_{rs})(0.25 + k)\} \tag{60}$$

where ε_{rs} is the relative dielectric constant of the substrate, h is the substrate height and W is the spacing between the lines (see figure 16). The following dispersion correction relates ε_{re} as a function of frequency to ε_{reo} [21]:

$$\sqrt{\varepsilon_{re}(f)} = \sqrt{\varepsilon_{reo}} + \frac{\sqrt{\varepsilon_{rs}}-\sqrt{\varepsilon_{reo}}}{1+aF^{-b}} \tag{61}$$

where

$$F = \frac{f}{f_{TE}} \quad \text{and} \quad f_{TE} = \frac{c}{4h\sqrt{\varepsilon_{rs}-1}} \tag{62}$$

and [35]

$$b = 1.8 \tag{63}$$
$$\log(a) = u \log (S/W) + v \tag{64}$$
$$u = 0.54 - 0.64q + 0.015q^2 \tag{65}$$
$$v = 0.43 - 0.86q + 0.540q^2 \tag{66}$$
$$q = \log(S/h) \tag{67}$$

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S is the center line width (see figure 16).

The relative phase velocity in the line, as a percentage of the speed of light, is given by [21]:

$$v_p = \frac{1}{\sqrt{\varepsilon_{re}}} \tag{68}$$

The horizontal dimensions of the modified CPW must be an order of magnitude greater than the vertical dimensions. Thus,

$$S,W \geq 10d \text{ and } S,W \geq 10t \tag{69}$$

In the MS region the line can be modeled as a parallel-plate transmission line [33]. The characteristic impedance is given by:

$$Z_o = \frac{d}{W - G} \sqrt{\frac{\mu_o}{\varepsilon_o \varepsilon_r}} \sqrt{\frac{2\lambda_L + d}{d}} \tag{70}$$

where d is the dielectric thickness, W is the top plate width, G is the gap width, ε_r is the relative dielectric constant of the dielectric layer, and λ_L is the London penetration depth of the superconducting metals. This equation is valid for

$$W - G \geq 20d \tag{71}$$

The phase velocity is given by:

$$v_p = \sqrt{\frac{1}{\mu_o \varepsilon_o \varepsilon_r}} \sqrt{\frac{d}{2\lambda_L + d}} \tag{72}$$

Equation 33 can be solved to give the effective dielectric constant in the MS region:

$$\varepsilon_{re} = \frac{1}{v_p^2} \tag{73}$$

In the CPW region, propagation occurs largely in the substrate. Thus, the equations for Z_o and ε_r are functions of the metal widths and substrate parameters, but not a function of the thickness or ε_r of the dielectric layer. Conversely, propagation in the MS occurs between the metal plates, in the dielectric layer. Here, Z_o and ε_r are functions of the metal widths and dielectric layer parameters, but not a function of the substrate height or substrate dielectric constant.

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For MS, since the wave is traveling in the dielectric layer, and the dielectric thickness is of the same order as the metal thicknesses, the penetration depth of the wave into the superconducting metals is important. Hence the London penetration term (λ_L) occurs in the MS equations. For CPW however, propagation is in the substrate. Since the substrate height is much larger than the metal thickness, penetration effects are ignored.

3.3.2.5 Determining the Widths of the Top Plate and Gap

With the CPW and MS equations, the top plate and gap widths can be determined to give any desired impedance. The top plate width must be 550 µm at the CPW input to interface to SMA launchers. To be compatible with the resonator to be tested, at the end of the MS region, the top plate width must be ten microns wide and the gap width must narrow down to zero. However, in the transition region, neither the CPW nor MS models are valid. The exact characteristics of this region are cannot be exactly determined. Therefore, the length of the transition region should be minimized. This is done by making the CPW and MS regions as long as possible.

The length of the CPW region is maximized by minimizing the impedance at the start of the transition. The end of the CPW region occurs when W (the spacing between top metal and ground plane) is at its minimum value (equation 69). The CPW equations show that for a fixed W, the characteristic impedance decreases as S (the top plate width) increases. As a result, the top metal width is kept constant through the CPW region. Decreasing the top metal width will increase the transition region length. The top plate width should not increase in the CPW region since this metal must smoothly narrow down to a ten micron wide line. Large changes in metal widths over short distances could add unmodeled and unwanted discontinuities.

In the MS region, the impedance is inversely proportional to the top metal width minus the gap width (equation 70). The length of the MS region is maximized by maximizing the impedance at the transition int. This occurs by making W-G as small as possible. This is limited by the validity of equation 70, shown by equation 72. Once the minimum value of W-G for MS is given, the maximum MS impedance and therefore the position of the end of the transition region is determined. Changing W cannot move this point. For this reason, W is also held constant throughout the MS region. Thus, the top plate width is a constant 550 µm in the CPW region, and a constant 10 µm in the MS region. Note that this also has the advantage of simplifying the layout of the top metal.

Since the impedance at each point along the transformer is known, the gap width can be determined once the top plate width has been specified. For the MS region, equation 70 can be solved for the gap width:

$$G = W - \frac{d}{Z_o} \sqrt{\frac{\mu_o}{\varepsilon_o \varepsilon_r}} \sqrt{\frac{2\lambda_L + d}{d}}$$

(74)

For the CPW region, no simple expression exists for the gap width based on the top plate width and the characteristic impedance. Therefore, an iterative method must be used to calculate the gap width for this region.

In the transition region, the top plate and gap widths should smoothly change from their values at the end of the coplanar region to their values at the beginning of the MS region. This was accomplished by approximating these shapes as cubic polynomials. In addition to the top plate and gap widths, the derivatives of these shapes with respect to x (the position along the taper) at the interfaces will be kept consistent. This gives four equations in four unknowns:

$$A(x_1)^3 + B(x_1)^2 + Cx_1 + D = y_1 \tag{75}$$
$$3A(x_1)^2 + 2Bx_1 + C = y_1' \tag{76}$$
$$A(x_2)^3 + B(x_2)^2 + Cx_2 + D = y_2 \tag{77}$$
$$3A(x_2)^2 + 2Bx_2 + C = y_2' \tag{78}$$

where, using the top plate width as an example:

x_1 is the value of x at the end of the CPW region (the start of the transition);
x_2 is the value of x at the start of the MS region (the end of the transition);
y_1 is the width of the top plate at $x=x_1$;
y_1' is the derivative of the top plate at $x=x_1$;
y_2 is the width of the top plate at $x=x_2$;
y_2' is the derivative of the top plate at $x=x_2$.

This system of equations is established and solved for both the top plate width and the gap width, allowing these structures to be calculated in the transition region.

A FORTRAN program has been written to automatically generate data to draw the masks and files to simulate the taper. This routine is completely general, that is, all of the parameters of the metals, dielectric, substrate, and taper can be entered. The routine accepts the taper length; the desired input and output impedance; the number of tapers to break the transformer into; the height and relative dielectric constant of the substrate; the thickness and relative dielectric constant of the dielectric layer; the penetration depth of the superconducting metal; the frequency (used for dispersion correction); the desired width of the top plate in the CPW region; the desired width of the top plate in the MS region; and the limits on the validity of the characteristic impedance equations.

The routine assumes only that the top plate width is constant in the CPW and MS regions. For all four impedance profiles, the routine calculates the exact locations where the CPW and MS models are no longer valid, that is, the exact location of the transition region is found. The gap width needed to give the necessary impedance is found for the CPW and MS regions. Information on the top plate and gap is used to fit the cubic polynomials in the transition region. A data file showing the width of the top plate and gap is created. This file could be used to digitize the masks.

3.3.2.6 Improved Analysis

The FORTRAN routine also creates Super-Compact netlist files for each transformer. The program calculates the exact phase velocity at the midpoint of each linear taper. This gives a much more accurate prediction of the performance than the preliminary analyses shown in section 3.3.2.3. Since the models cannot be used to predict the phase velocity in the transition region, this parameter is also fit to a cubic.

An example is shown in tables 2 and 3 to demonstrate the use of the routine. For the MS region, a ten micron wide top metal gives a minimum Z_0 of 5.14 ohms. This impedance value is entered as the desired output impedance. This minimum value of Z_0 occurs when the gap width is zero. The output data is summarized in table 3-3. Note that the Chebyshev and sinusoidal tapers have the added advantage of having the shortest transition regions, where the impedance and relative phase velocity cannot be modeled exactly. The circuit simulated consists of the 50-to 5.14-ohm transformer, a delay line, and a 5.14- to 50-ohm transformer. The delay line is a 5.14-ohm, 10-mm transmission line with a phase velocity of 0.367. The responses of the four tapers are shown in figures 21 and 22.

Table 2. Inputs to Taper Routine

Taper length	10 mm
Impedance at input	50 ohms
Impedance at output	5.14 ohms
Number of tapers	100
Substrate height	100 μm
Substrate ε_r	4
Dielectric thickness	0.2 μm
Dielectric ε_r	4
Penetration depth (niobium)	0.086 μm
Frequency	10 GHz
CPW limit	$W \geq 10d$
MS limit	$W - G \geq 20d$

Table 3. Summary of Output from Taper Routine

	Top Metal Width	Gap Width	Phase Velocity
Start of Taper	550.0 μm	622.2 μm	0.705
Start of Transition	550.0 μm	554.0 μm	0.637
End of Transition	10.0 μm	6.0 μm	0.367
End of Taper	10.0 μm	0.0 μm	0.367

	Start of Transition	End of Transition	Length of Transition
Chebyshev Taper	x = 3496.3 μm	x = 5623.4 μm	2127.1 μm
Exponential Taper	x = 2724.8 μm	x = 5973.0 μm	3248.2 μm
Linear Taper	x = 5149.7 μm	x = 8282.1 μm	3132.4 μm
Sinusoidal Taper	x = 5095.3 μm	x = 7279.3 μm	2184.0 μm
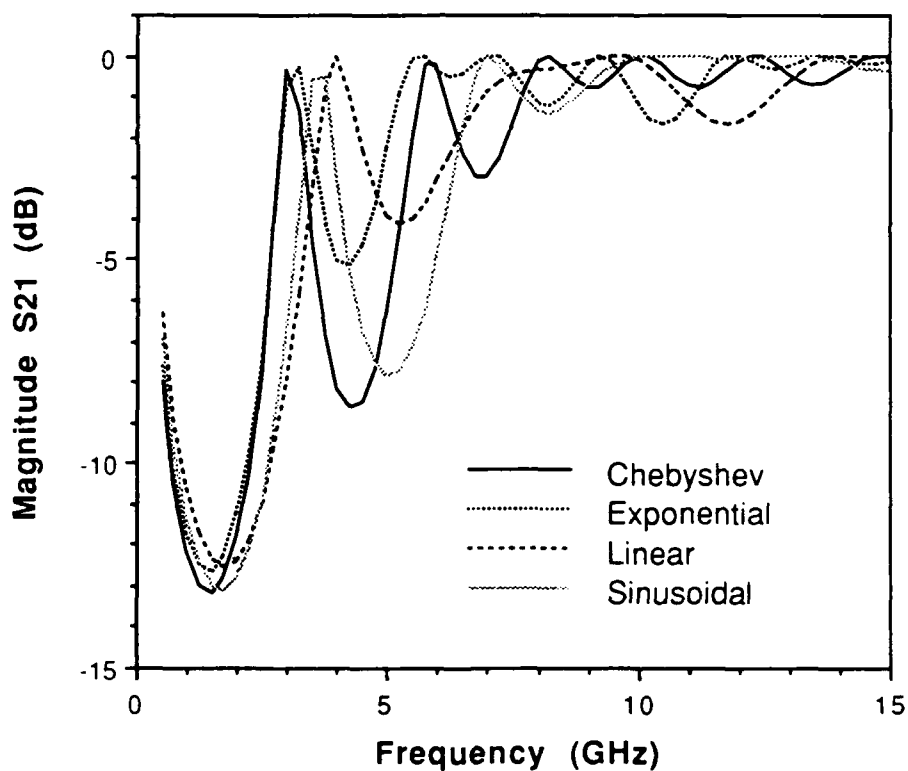
Figure 21. Transformer Responses Using Exact Calculation of Phase Velocity
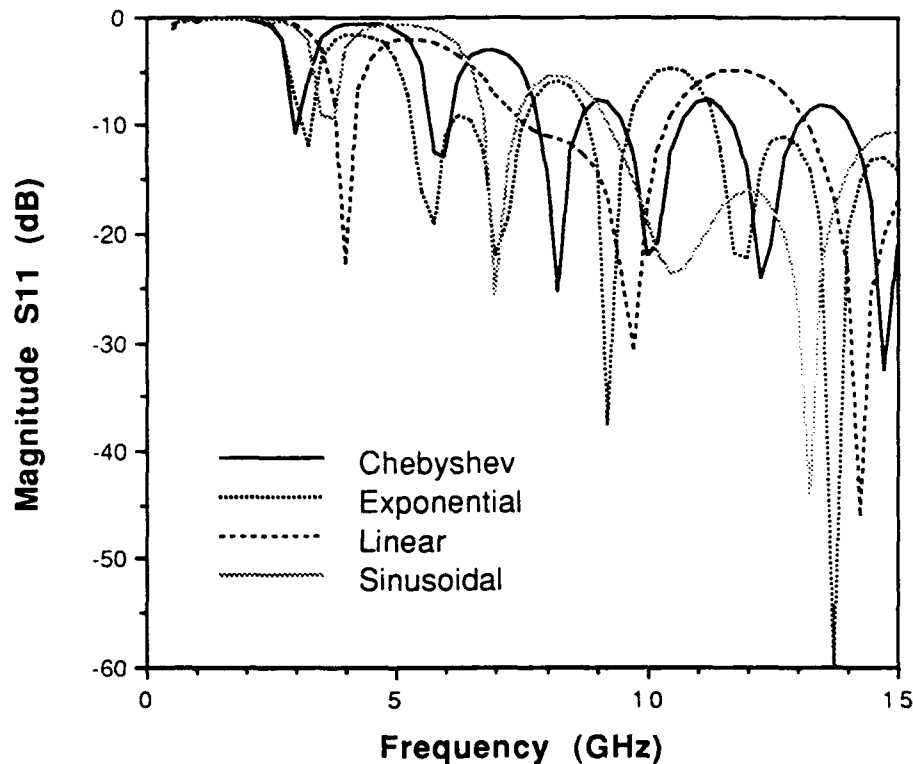
Figure 22. Transformer Responses Using Exact Calculation of Phase Velocity

The sinusoidal transformer is the best for this particular example since it has the flattest passband response (figure 21), although the Chebyshev taper would also be a reasonable choice. The plot of S_{11} (figure 22) is inconclusive since all four tapers exhibit similar performance. The responses have changed significantly from figure 19 due to the inclusion of the exact calculation of the phase velocity. The mask data from the sinusoidal transformer is plotted. Figure 23 shows a plot of the top plate and gap widths along the taper. Note that both structures are continuous and smooth.

3.3.3 Substrate Resonances

The transformer described is based on work done by McGinnis and Beyer [33]. Assuming a fixed phase velocity, they successfully designed and fabricated a 50- to 2-ohm Chebyshev transformer. However, they observed dropouts in the response of the transformer fabricated

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which they attributed to substrate resonances. These dropouts occurred near 4.5 GHz and 8 GHz and caused almost 10 dB more loss in the circuit than predicted. We investigated this phenomenon through research and simulations on dielectric resonators to insure that similar problems would not affect our experiment.
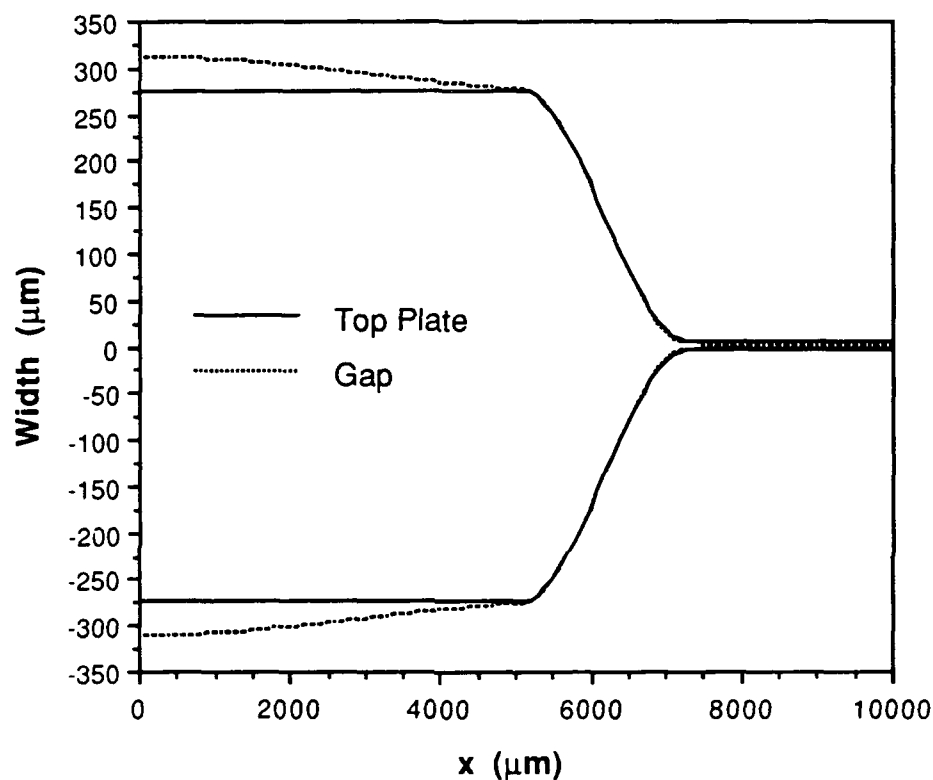
Figure 23. Plot of Top Plate and Gap for the Sinusoidal Transformer

The McGinnis and Beyer circuit is fabricated on a square substrate 25 mm on a side. This is shown in figure 24. The location of the input and output ports are shown. The height of the substrate is 400 μm; the dielectric constant of the substrate is 12.

The resonant frequency of a cylindrical dielectric resonator can be approximated by:[36]

$$f(\text{GHz}) = \frac{1}{\sqrt{\varepsilon_r}} \left(\frac{34}{L(\text{mm})} + \frac{117.3}{r(\text{mm})} \right) \tag{79}$$

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where r is the radius, L is the length, ε_r is the dielectric constant. Instead of a cylindrical resonator, the case here is a dielectric slab with a height 400 μm and a width 25 mm. However, the experiment will be fabricated on a 100-μm substrate with a dielectric constant of 4. Since the resonant frequency is inversely proportional to the square root of ε_r, reducing this by a factor of 3 will increase the frequency by a factor of 1.7. Furthermore, if L is large, the frequency becomes inversely proportional to r, and thus decreasing the substrate thickness by a factor of 4 will also move the resonances to a higher frequency.
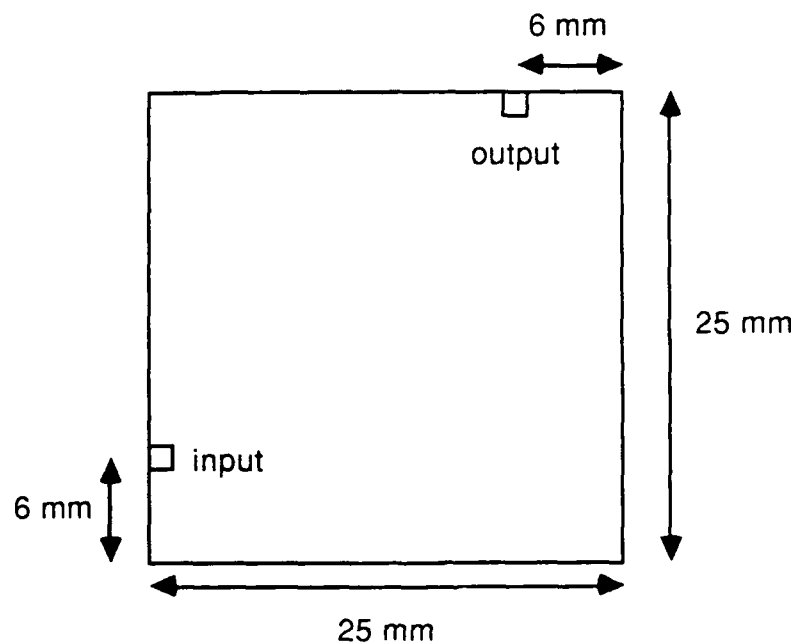
Figure 24. Substrate and Ports Used by McGinnis and Beyer

To show this numerically, Sonnet Software's EM simulator was used to simulate the throughput between isolated ports on dielectric slabs. The slab (except for thickness) and ports are constructed the same as the McGinnis circuit (see figure 3-14). Four simulations are performed:

$h = 400$ μm, $\varepsilon_r = 12$ (the situation in the McGinnis paper)
$h = 400$ μm, $\varepsilon_r = 4$
$h = 100$ μm, $\varepsilon_r = 12$
$h = 100$ μm, $\varepsilon_r = 4$ (the situation of the current experiment)

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Figure 25 is a plot of the predicted responses. The h = 400 μm, ε_r = 12 simulation shows several peaks in S_{21} near 10 GHz. Decreasing either parameter generally reduces S_{21}. Decreasing both parameters effectively reduces the signal between the ports to a minimal level, especially in the frequency range of concern (the 10 GHz region).
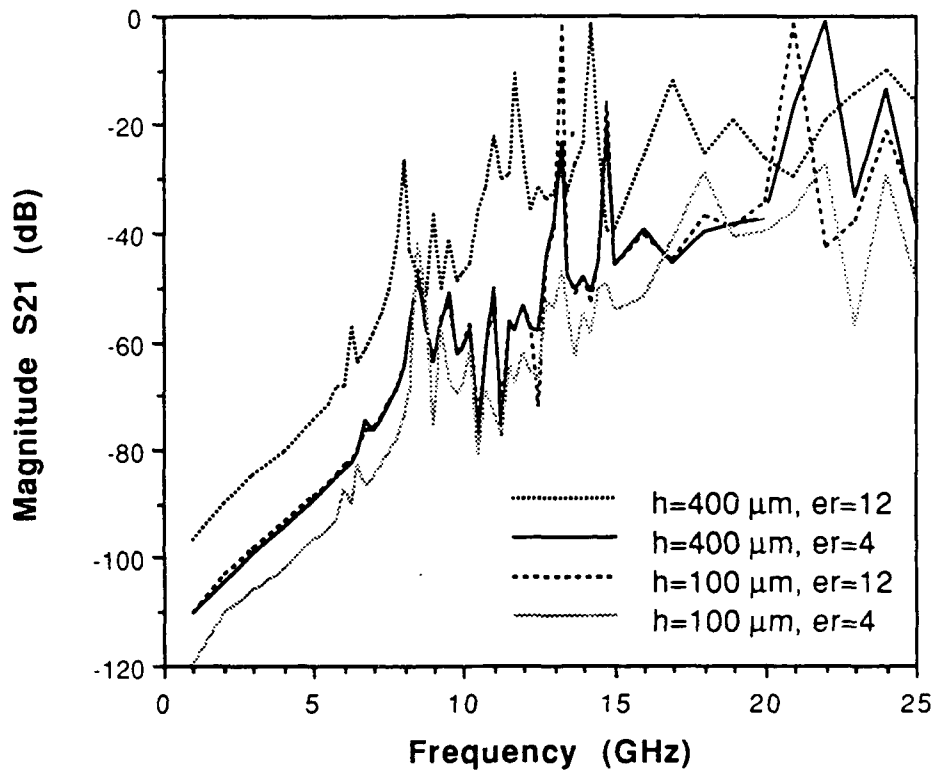
Figure 25. Isolated Ports on a 25-mm by 25-mm Dielectric Slab

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EM simulations were also run on the substrate to be used for the resonator experiment. This substrate is 30 mm by 0.5 mm. To again illustrate the effects of reducing the substrate height and decreasing the dielectric constant, simulations are performed on a substrate with the following parameters:

h = 400 μm, ε_r = 12
h = 400 μm, ε_r = 4
h = 100 μm, ε_r = 12
h = 100 μm, ε_r = 4

Figure 26 shows S_{21} between isolated ports on a 30-mm by 0.5-mm substrate. The simulation shows that for the ε_r = 4, h = 100 μm case, the ports are well isolated.
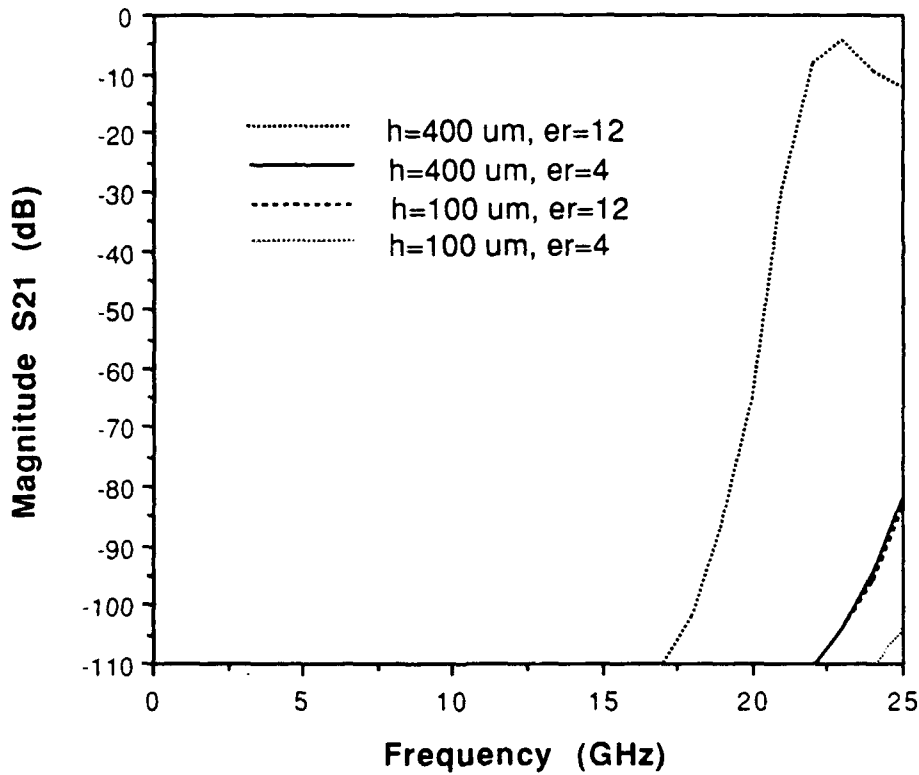
Figure 26. Isolated Ports on a 30-mm by 0.5-mm Dielectric Slab

3.3.4 Summary

The complete dielectric step coupled resonator with impedance matching transformer is illustrated in figure 27. There are three mask layers, the ground plane (red), the center conductor (blue) and the resonator (green). The placement of the three layers relative to each other is illustrated. Figure 28 depicts top and cross-sectional views of this same layout (as shown in figure 27).
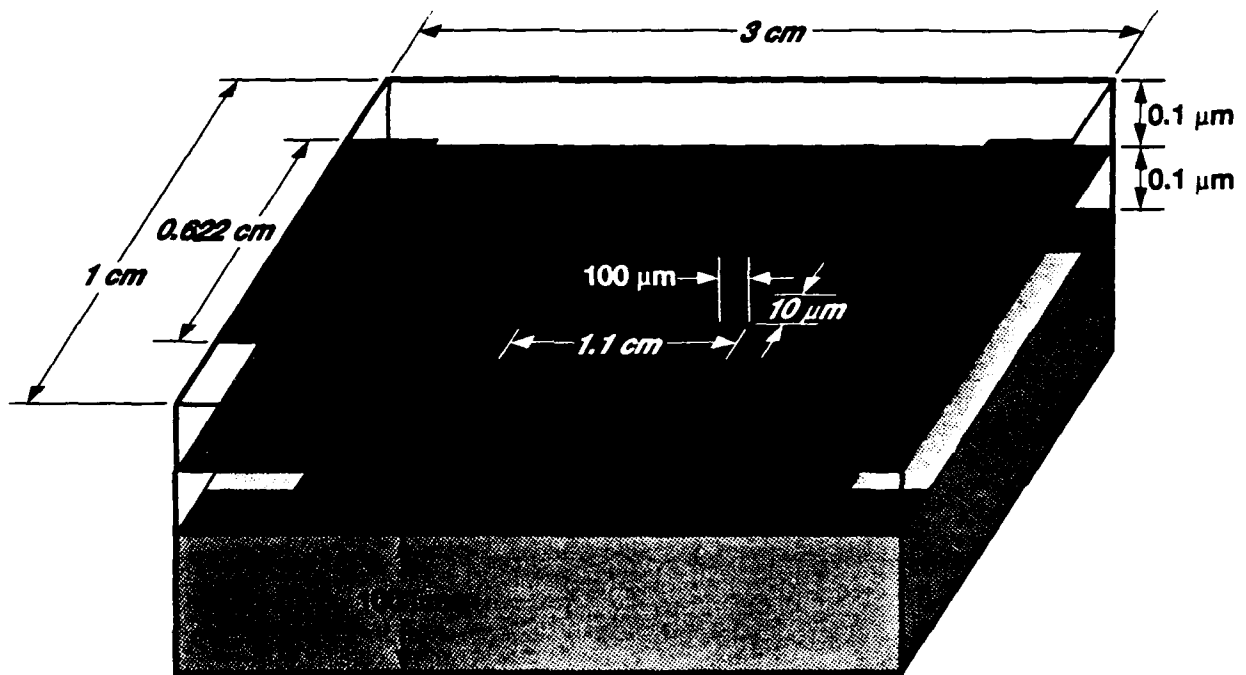
Figure 27. Complete Dielectric Step Coupled Resonator, Perspective View
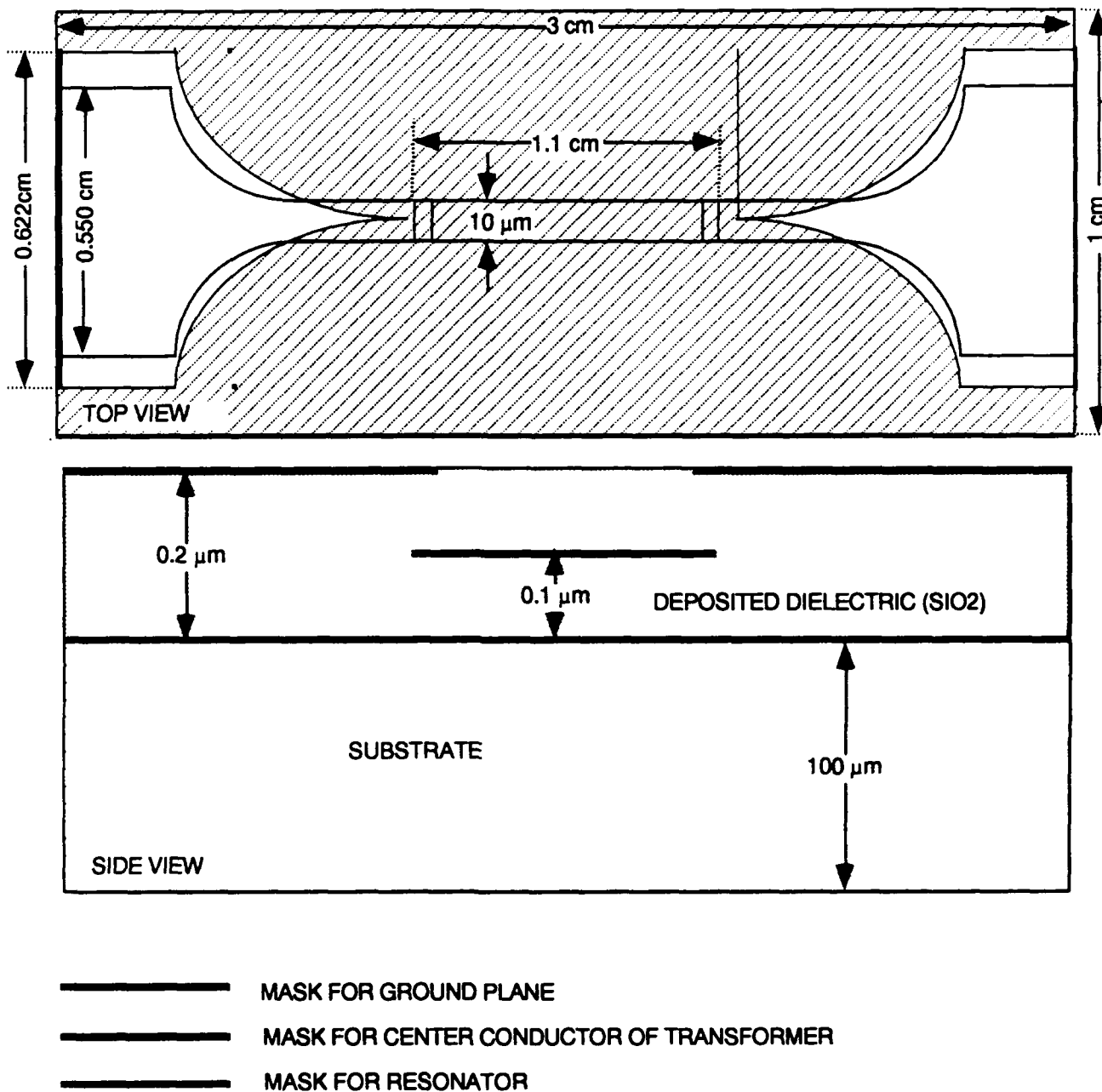
Figure 28. Complete Dielectric Step Coupled Resonator, Top and Cross-Sectional Views

SECTION 4

CONCLUSIONS/RECOMMENDATIONS

The accepted quasistatic planar waveguide models are not at issue when simulating superconducting transmission lines, but rather, the conventional model for conductor surface resistance and losses. Superconducting materials exhibit a strongly inductive surface *impedance* whose losses are proportional to the square of frequency, in contrast to the conventional surface resistance varying as the square root of frequency. For accurate modeling of superconducting transmission lines these effects must be accounted for. This can be conveniently accomplished through the use of a complex surface impedance Z_s, calculated from the superconductor complex conductivity, in the accepted MS and CPW equations. Unfortunately, commercially available CAD tools do not allow the conductivity or surface resistance of a material to be complex quantities.

It is necessary that accurate computer-aided design models be included in existing MMIC design software (for example, *Touchstone*, *SuperCompact* and SPICE) to effectively integrate superconducting materials into the realm of MMIC design. During this investigation we have developed models of superconducting transmission lines which can be interfaced with commercially available MMIC design software, either by embedding the models into the simulation software or by deriving equivalent circuit models. Equivalent circuit models could be substituted for the superconducting MS, allowing simulation of superconducting microwave circuits without requiring the modification of the simulation software code. Alternately, our superconducting transmission line model could be used to calculate scattering parameter data in a form suitable for input into the CAD simulator, treating the superconducting transmission line as a two-port device.

An experiment for verifying the superconducting transmission line models has been proposed. The experiment requires two resonators, 1/2 and 1 wavelength long. We have decided to perform the experiments at 10 GHz which is a compromise between small size circuits, and radiation losses. MS geometry has been chosen due to the ability to fabricate thin dielectric substrates. We have decided to use a 0.1 µm dielectric layer for all measurements.

Two measurement circuits are proposed. The first is a 100 µm wide, 0.5-ohm resonator coupled to its test ports by 50-ohm coaxial to MS launchers. The second circuit is a 10-µm wide, 5-ohm MS coupled to the measurement system by a dielectric step and a 50 to 5-ohm transition section. The transition section ends in a 50-ohm CPW section. The dielectric step coupling has been simulated with Sonnet software's EM simulator. A mask large enough to set up both circuits will be a reasonable size. A foundry which can generate both circuits using niobium metalization and SiO_2 dielectric should be used. These circuits will require 0.01-µm accuracy in dielectric film thickness and 2-µm accuracy in photolithography.

Many existing systems can be improved, and many new systems will become realizable with the use of superconducting microwave transmission lines. We have developed models for these transmission lines which are suitable for inclusion in commercial microwave circuit CAD software. We have also designed experiments which will allow us to verify the accuracy of these models.

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GLOSSARY

CAD	computer-aided design
CPS	coplanar strip
CPW	coplanar waveguide
EM	electromagnetic
MMIC	Monolithic Microwave Integrated Circuits
MS	microstrip
SADC	superconducting analog to digital converters
SMA	
TEM	transverse electromagnetic
T_c	critical temperature
VSWR	voltage standing wave ratio

Technical Report 6

HIGH PERFORMANCE, SUPERCONDUCTING ANALOG-TO-DIGITAL CONVERTER

by

J. M. Schoen

ABSTRACT

The use of residue number arithmetic to extend the precision of a superconducting analog-to-digital converter based upon the periodic threshold response of Superconducting Quantum Interference Devices (SQUIDs) is described. By suitably sizing an array of SQUID devices and magnetically coupling the input signal to the array, a digitized version of the residue representation of the signal can be obtained. Preliminary estimates of the performance of a converter based upon this principle suggests that 16-bit precision at 2 Gigasamples/sec is achievable. Areas of investigation to begin design of such a converter are described.

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SECTION 1

INTRODUCTION

This paper defines the configuration of a high-performance, superconducting analog-to-digital (A/D) converter, which utilizes the periodic characteristics of Superconducting Quantum Interference Devices (SQUIDs). The underlying principle by which the converter operates is not new. It was originally proposed by Zappe [1], and several versions built by Harris, Hamilton and Lloyd [2-5] at the National Bureau of Standards. Recently, a Japanese version of the converter has been reported with a 4-bit precision and a 5 Gigasample/sec conversion rate [6].

The conversion scheme is based upon the periodic threshold response characteristics of SQUIDs. This approach has been demonstrated to yield fast conversion rates for low precision (generally 5 bits or less) [5]. The MITRE contribution to this approach is to employ residue arithmetic to enhance the precision achievable with this conversion scheme. Specifically, we propose to utilize the fact that a 16-bit number can be represented as four, 5-bit numbers, and that the periodic response of a SQUID can be used to compute the residue of a number to achieve high-precision, high-sample rate conversion.

The characteristics of a SQUID device which form the basis of the periodic threshold type superconducting A/D converter are described in the next section. Residue arithmetic representation and its application to this A/D converter architecture is discussed in Section 3. Areas of investigation necessary to begin design of a converter which exhibits the enhanced performance suggested in this paper are covered in Section 4.

SECTION 2

SQUID PERIODIC THRESHOLD A/D CONVERTERS

A SQUID device consists of a ring of superconducting material broken by two Josephson junctions. Strictly speaking, such a device is categorized as a d.c. SQUID. Figure 1 is a schematic representation of a d.c. SQUID as a two-terminal device.

To describe the operation of a SQUID, it is first necessary to discuss the characteristics of a Josephson junction. A Josephson junction consists of an extremely thin non-superconducting gap between two superconducting materials. Typically, the gap consists of an insulating oxide, but it could be made in a number of different ways. Electrons are paired in a superconductor. If the gap is sufficiently thin, the paired electrons can tunnel **as a pair** from one side to the other.

From a simple circuit perspective, the Josephson junction resembles a superconductor. It can pass a current with no voltage drop. The current that the Josephson junction can pass without a voltage is limited. A critical current exists which, if exceeded, will result in a voltage appearing across the junction. This current is significantly lower than the critical current of the superconducting material comprising each side of the junction.

A d.c. SQUID appears to be two Josephson junctions in parallel. In the absence of a magnetic field, the SQUID behaves like a single Josephson junction, except that it exhibits a critical current equal to the sum of the critical currents of each Josephson junction. It is in the presence of a magnetic field that a SQUID exhibits a richer behavior.

When a magnetic flux density B is imposed perpendicular to the plane of the SQUID, a current is induced in the SQUID by Lenz's law to oppose the field. The magnetic flux, Φ (area integral of B perpendicular to the plane of the SQUID) passing through the SQUID cannot assume an arbitrary value. In [7], Φ is shown to be related to the phase of the electron pair wave function around the loop of the SQUID. A requirement that the wave function phase around the loop is single valued results in a requirement on the total magnetic flux passing through the SQUID. The total flux is the applied magnetic flux and the flux resulting from the current induced by Lenz's law in the SQUID. The total flux must equal an integral multiple of the magnetic flux quantum, h/2e, where h is Planck's constant and e is the electronic charge. Note the flux quantum, Φ_0, has an extremely low value of 2.07 x 10^{-15} Webers, which implies that a SQUID is extremely sensitive to magnetic fields.

Figure 2 illustrates the effect of an applied magnetic flux on the currents flowing through a SQUID. The current induced in the SQUID is denoted i in figure 2. The current passing through the SQUID is denoted by I. If we assume both Josephson junctions are identical in the SQUID, then the current in one junction is (I/2) + i and in the other junction it is (I/2) - i.
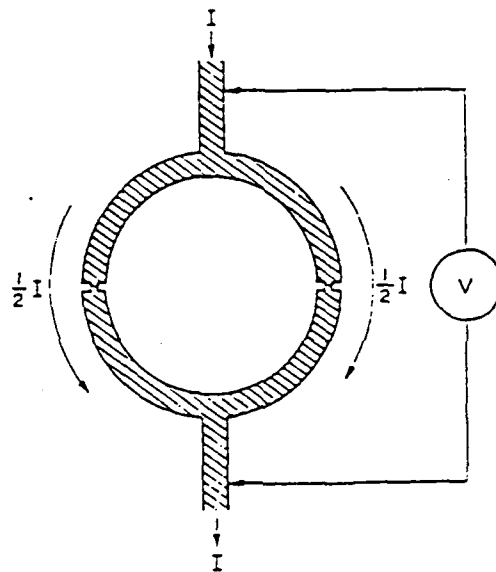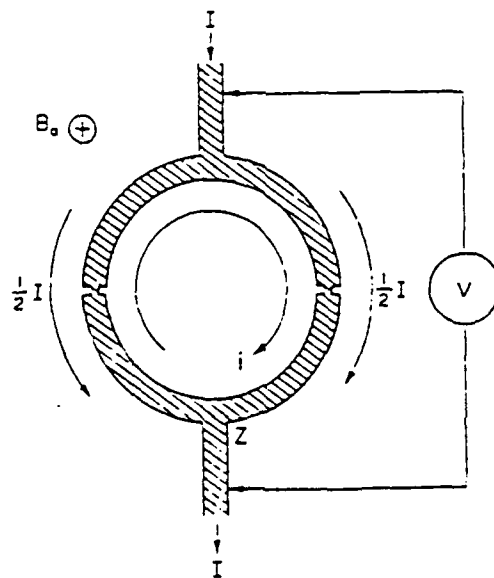
Figure 1. Configuration of a d.c. SQUID

Figure 2. Effect of External Magnetic Flux Density B on SQUID Currents

When there is a magnetic flux-induced current flowing in the SQUID, the apparent critical current of the SQUID will be reduced. A plot of SQUID critical current versus magnetic field, H, is plotted in figure 3 [7]. A requirement for this dependence of critical current on the magnetic field to be true is that the maximum induced flux, LI_c, where L is the SQUID inductance and I_c is the critical current of the SQUID, exceed the flux quantum. This requirement is necessary to insure that all measuring fields can be screened adequately. Note that when the measuring field is sufficiently high to admit or expel another flux quantum, this process is energetically favored over further screening by induced current in the SQUID. The value I_c in figure 3 is given by

$$\Delta I_c = \Phi_0/L.$$

A point to observe about the response of the SQUID's critical current to an applied field is that it is periodic. A one-bit A/D converter can be constructed by applying a current whose value is indicated by the dashed line in figure 3. If the applied field causes the critical current to be below the value of the measuring current, a voltage of approximately 2.5 mV magnitude will appear across the SQUID. If the critical current exceeds the measuring current, no voltage will be observed. To create a two-bit converter, a second SQUID is magnetically coupled to the same field. The area of this second SQUID is twice that of the first. Figure 4 illustrates the response of each SQUID to the applied field and measuring current. Additional bits can be added by scaling each successive SQUID area by a factor of two. The limiting factor to the number of bits of precision that can be obtained from a converter of this type is area consideration [5]. The magnitude of the voltage pulses which must be captured, as well as the potential speed of operation, dictates that Josephson junction latches will be required at the outputs of the converter.

Another interesting feature of the periodic threshold response of a SQUID is that a response can be considered to be a computation of the residue of the applied field with respect to the quantity $\Phi_0/\mu_0 A$. Although this computation is not linear, as an examination of figure 3 clearly reveals, the use of quantization on multiple channels will enable us to compute the digitized residue with respect to a selected number of bases without concern for the non-linearity of the SQUIDs periodic threshold response. The issue of residues as applied to periodic threshold A/D conversion will be covered in the next section.

Before completing the discussion of periodic threshold A/D conversion, some words about response time are in order. A typical response time of a SQUID to an applied signal is less than 10 ps. If we allow 20 ps for the SQUID to settle, and then apply a pulse of current to measure the SQUID response, a maximum sample rate of 25 GHz seems feasible. When one takes into account the inductive loading of all the SQUIDs via the magnetic coupling of the input signal, the sample rate falls to the 2-5 GHz range [8].
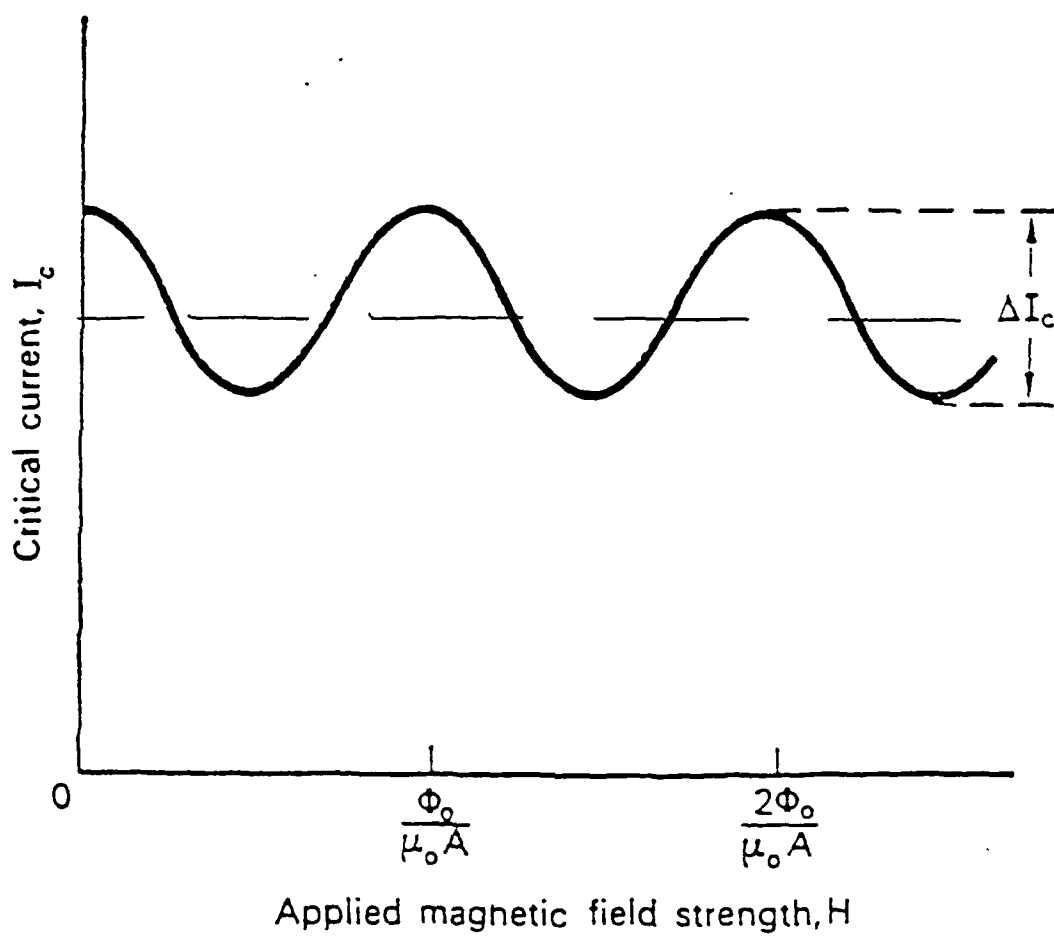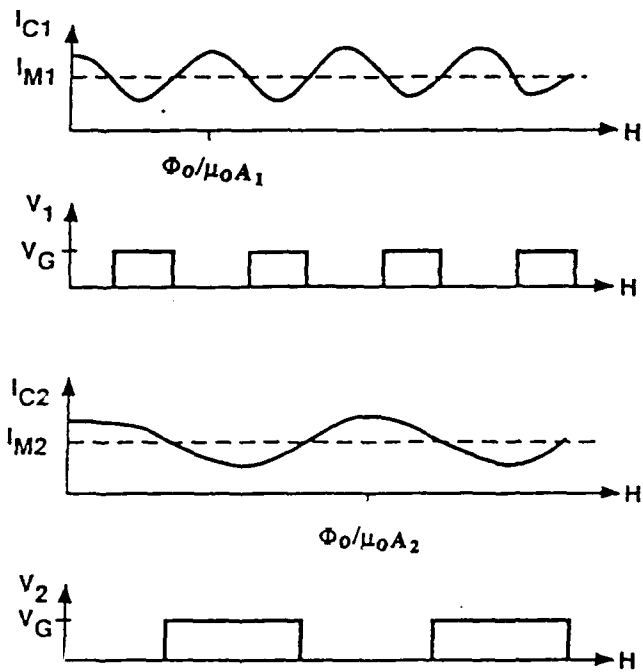
4

Figure 3. SQUID Critical Current as a Function of Applied Magnetic Field H.

Subscripts refer to SQUIDs numbered 1 and 2. I_{ci} is critical current, V_i is voltage output, and I_{mi} is current pulse applied to SQUID to monitor its state.

Figure 4. Response of Two Threshold SQUIDs to an Applied Field H.

SECTION 3

RESIDUE NUMBER REPRESENTATION AND SUPERCONDUCTING A/D CONVERSION

During the past five years, MITRE has been investigating residue number system (RNS) based signal processing, which leads to simple, high-speed integrated circuit designs employing parallel channels and repeatable elements in which "carry" operations can be ignored. Our familiarity with RNS representations led us to consider the possibility of using them to enhance the A/D conversion process, even if subsequent RNS signal processing is not employed. Conversion from RNS digital representation to conventional representation is straightforward.

The key point of RNS representation is that given a set of mutually prime numbers {P1, P2, Pi}, any number between zero and π_i Pi-1 can be uniquely represented by the set of the moduli of the numbers with respect to the mutually prime bases {Pi}. If one chooses the prime numbers representable by 5-bit binary codes (i.e., {17, 19, 23, 29, 31}), it is possible to represent any number with 22-bit precision. Another feature of RNS representation is that by adding additional bases, the codes can be made error correcting [9, 10]. The selection of the set {17, 19, 23, 29, 31} can represent numbers with 16-bit precision. If N primes are required to represent a 16-bit number, N + 2 primes are required to detect two errors or correct one error. Also the product of any N primes must be $>2^{16}$.

Our experience suggested that if we could convert our input signal into a series of residues, and then perform the A/D conversion on the residues at lower precision, then we would have enhanced the conversion process. Let us examine precisely how that can be done with the periodic threshold SQUID A/D converter described in Section 2. An examination of figure 3 suggests that the periodic threshold has a period proportional to 1/A, where A is the SQUID area. To obtain the appropriate residues, it is necessary to select SQUID areas inversely proportional to the desired residue. To provide for a 5-bit representation, it is necessary to have a series of five SQUIDs for each channel with areas in proportion to 1: 2: 4: 8: 16. Table 1 summarizes the area ratios of 25 SQUIDs required to achieve 16-bit precision. Any four of these primes will give 16-bit precision with no error detection or correction. Five primes allows error detection, but not correction.The area ratio of the smallest to the largest is 29.2, which should be achievable using current lithographic techniques.

Table 1. Ratio of SQUID Areas to Achieve 16-bit Precision with Error Detection

Channel	Areas				
17	$\frac{1}{17}$	$\frac{2}{17}$	$\frac{4}{17}$	$\frac{8}{17}$	$\frac{16}{17}$
19	$\frac{1}{19}$	$\frac{2}{19}$	$\frac{4}{19}$	$\frac{8}{19}$	$\frac{16}{19}$
23	$\frac{1}{23}$	$\frac{2}{23}$	$\frac{4}{23}$	$\frac{8}{23}$	$\frac{16}{23}$
29	$\frac{1}{29}$	$\frac{2}{29}$	$\frac{4}{29}$	$\frac{8}{29}$	$\frac{16}{29}$
31	$\frac{1}{31}$	$\frac{2}{31}$	$\frac{4}{31}$	$\frac{8}{31}$	$\frac{16}{31}$

The next section is a discussion of issues which must be evaluated in order to begin an implementation of this approach to A/D conversion.

SECTION 4

IMPLEMENTATION STRATEGY

The approach to superconducting analog-to-digital conversion described in this working paper has a number of distinct advantages compared to the other methods under consideration in Project 91080. The scheme is based upon a circuit design that has been reported to work in several lab_ratories. It is simple and therefore can be built in monolithic form.

Nevertheless, a number of areas must be investigated before a full fledged design effort can begin. An analysis of errors in the converter and sensitivity to circuit variations and noise must be performed. The effects of non-linearity in the threshold curves should be minimized, since transitions from the zero to finite voltage states occur in the linear region of the threshold characteristic. Deviations in the SQUID area will cause the position at which the SQUID moves from the zero to finite voltage state to shift horizontally. Similarly, noise in the SQUID can cause an apparent horizontal shift in the transition from zero to finite voltage state. The nature of these shifts and whether they can be readily corrected for using RNS techniques must be evaluated.

Techniques for magnetically coupling the input current to the SQUID have been discussed in detail [11, 12]. The challenge of effectively and uniformly coupling to 25 SQUIDs must be addressed. It is also possible to directly use equal size SQUIDs to achieve a similar periodic threshold behavior. In this case, however, a resistive ladder must be used to vary the periodicity of the response [2, 5]. The trade offs of varying SQUID size versus a resistive ladder must be assessed.

A suitable back-end latching circuit must be identified for each SQUID output. Because of the magnitude and speed of the voltage outputs, Josephson junction electronics must be employed.

Other areas which must be considered include the mode by which the measuring current pulse is applied to each SQUID. Ideally, a single pulse can be applied to each SQUID in series, but then the output voltage of each SQUID will not be measured with respect to ground. It is not yet clear if the magnitude of each measuring current pulse should be the same. Will it be necessary to tune each pulse to measured SQUID characteristics? The timing of the measuring pulse with respect to the latching of the output will impact aperture error for the converter. The timing can only be ascertained after the SQUID response to both the magnetically coupled input signal and the measuring pulses have been simulated. Simulation of the SQUID system can be most easily performed by using the JSPICE program developed by students of Professor T. Van Duzer at U. California at Berkeley [13]. All required circuit elements are included in this version of the ubiquitous SPICE program which is available on several computers at MITRE.

Once the converter response time and sample rate have been determined by simulation, input signal bandwidth must be addressed. Does the low pass filter characteristic of the input circuit (source impedance and SQUID-coupling inductor) sufficiently reduce the input bandwidth to satisfy the Nyquist criteria? Is any signal preconditioning required? These issues will be considered as the study of this conversion scheme progresses.

SECTION 5

SUMMARY

A novel way to enhance the precision of periodic threshold SQUID-type A/D converters has been described. The approach takes advantage of the use of residue arithmetic to represent 16-bit numbers by their residue with respect to five mutually prime bases expressed in 5-bit form. Double error detection and single error correction can be included in this scheme.

To implement this approach, error and sensitivity analysis must be performed. JSPICE simulation should prove beneficial in determining SQUID coupling and response and its impact on circuit timing and input signal requirements.

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Technical Report 7

EDGE SHARPENING WITH JOSEPHSON JUNCTION

by

J. Schwartz

ABSTRACT

An example is given of the use of Josephson junction to sharpen the rise times of electronic waveforms. Conventional circuit analysis of edge sharpening is compared to the use of JSPICE circuit analysis software. A set of tentative design parameters is obtained by the conventional design methods, using an equivalent circuit for the Josephson elements. A more comprehensive simulation analysis using JSPICE confirms the choices of parameter values. The effectiveness of these parameter values are compared to alternative parameter values for waveform sharpening.

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SECTION 1

INTRODUCTION

For analog-to-digital (A/D) conversion, it is important to minimize the rise time of the waveform samples, since this determines the effective aperture time for the track and hold function of the converter. For this reason, an edge sharpening circuit is sometimes used in conjunction with a superconducting (A/D) converter. An edge sharpening circuit takes a clock pulse with a rise time of the order of 5 ps or greater and outputs pulses with rise times of about 2 ps. The edge sharpener utilizes a pair of Josephson junctions to take advantage of their fast switching properties. The other circuit components are conventional resistors and capacitors.

The circuit description presented here is intended to acquaint a designer with some of the characteristics of such circuits, namely parameter values and speeds, as determined by superconducting components. Some cases are described by using a so-called "static model," which bypasses a full description of the underlying physical laws, and assumes the parameters are accepted as experimentally determined. These cases have been further analyzed with the JSPICE program, [1] [1] to validate the results of the simpler manual analysis. Thus, a correlation is made with analytical methods applicable at various levels of detail. The approach used here can be an effective guide to the initial choice of design parameter values when followed up by more comprehensive analysis. The JSPICE simulation program is, however, somewhat cumbersome to apply for initial design estimates. These estimates take substantial computer time, graphic outputs are not automatic, and interpretation of the results is time consuming. However it was the best method available to verify the appropriateness of parameter choices and circuit operating points. The detailed simulation that JSPICE performs, along with its reliability, make it a useful tool for finding errors and omissions in simpler design estimates. JSIM [2] is a recent extension of JSPICE,

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[1] JSPICE is an extension of the popular program SPICE (Simulation Program with Integrated Circuit Emphasis) which has been developed by students of T. Van Duzer at the University of California at Berkeley for modeling superconducting electronic circuits. This extended program has been designated JSPICE (Josephson junction SPICE) because it contains an equivalent circuit model specifically of the Josephson junction.

[2] JSIM is an experimental extension of JSPICE, producted by T. Van Duzer and his students at the University of California at Berkeley. The numerical analysis methods in JSIM are better suited to the specific differential equations typical of Josephson junctions than the more general solution methods applied in SPICE and JSPICE. In fact, they are several times as fast. However, with these modified numerical methods, JSIM sacrifices the ability to simulate semiconductor circuits. Its use is limited to simpler combinations of the Josephson junction, used in conjunction with resistance, capacitance, and inductance. In addition, JSIM has some new features in its output flexibility that make the tabulation and plotting of its outputs more convenient. Brief experience with this

which can be used to perform the same analyses more efficiently. It is recommended for future efforts of this type. Also on UNIX workstations and similar systems, XGRAPH [3] is available for convenient graphic plotting of the modeled waveforms.

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program indicates that it requires considerably less time to analyze a circuit than does the JSPICE program.

[3] XGRAPH is a graphic plotting facility, available with UNIX operating systems that provide Xwindows and associated graphic user interfaces. In a system having this software, plots of the contents of one or more data files are conveniently produced at the terminal. High quality hard copy plots of the same data may also be initiated that correspond to what is viewed on the terminal, with resolutions as high as the computer system printers can provide. Documentation on the use of XGRAPH is available online in the UNIX systems that carry the software.

SECTION 2

EDGE SHARPENING CIRCUIT

The edge sharpening circuit has been discussed in the literature by Hamilton et al [2] and by Dhong et al [3]. Examples of the superconducting A/D converters, of which it may be a part, have been covered in other works [4,5]. Digital sampling rate and precision are basic to future applications. The 2 ps aperture, shown to be feasible using superconductive circuitry, is at least as fast as the most current semiconductor circuitry and is essential for achieving desirable sampling rates. The performance limitations of A/D converters using threshold comparators have also been studied [2,3].

Figure 1 shows the circuit investigated. J1 and J2 are a pair of Josephson junctions. They have slightly different values of critical current, Icrit, and gap voltage, Vg. Some of the additional circuit values, including the associated capacitance and resistances, are given in table 1. Given these junction parameters and the required output voltage peak amplitude (about 5 mv), the two other circuit elements, resistances R_R and R_{INCL}, can be chosen together based on input voltage peak amplitude. The input pulses, intended to supply the "clock voltage," Vclock, to drive the A/D comparator circuitry, have about a 10 mv peak and a trapezoidal rise and fall time of 5 ps. The pulse duration is several picoseconds. Repetition rates may be as low as 100 MHz (i.e., a pulse separation of 10,000 ps), but the aperture time is important to performance. The A/D converter circuits digitize the input value of clock voltage that was present during the aperture time. In fact, this feature replaces the function of the track and hold subsystem of semiconductor A/D converters. The simplified analysis is based on considering the Josephson junctions J1 and J2 as simply rapid switches. If the value of the current through them is initially less than Icrit (generally the order of several mA), then they act as a short circuit, i.e., the net voltage across each is zero. If Icrit is exceeded, they enter the "voltage state," and the voltage across each rises very rapidly to the order of Vg, generally the order of 2.5 mV. In the voltage state, the junctions exhibit resistance. They are not usually linear devices, and both a minimum value Rn and a maximum value R_O for the resistance across the switch is generally specified. In addition, each junction has a capacitance in the sub-picofarad range. Additional effects occur, such as a tendency to self-oscillation at frequencies above 10 GHz, but these effects are minimized in the current design and will not be treated here. The JSPICE model takes these effects fully into account. We assume the junction changes state instantaneously, but the transient voltage across it is modified by the the associated RC time constants. There is actually hysteresis in that the voltage across the device does not generally become zero when the drive current falls below Icrit, but persists until a fraction of Icrit is determined by the other device parameters. In the present case, this hysteresis in no way affects the leading edge of the clock pulse.
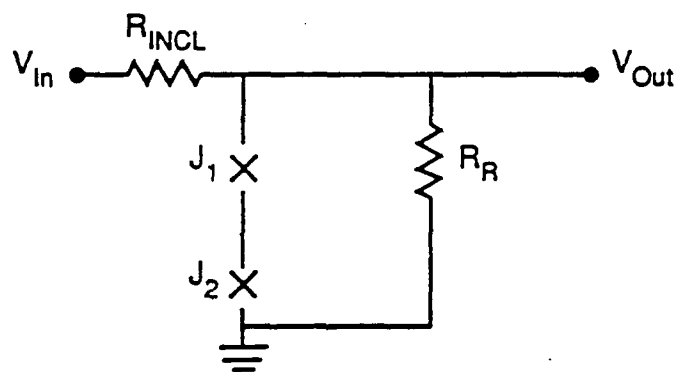
Figure 1. Edge Sharpener Basic Circuit

Each Josephson junction shown in figure 1 can be replaced by the static equivalent circuit shown in figure 2, with appropriate parameter values in parallel. Figure 2 shows a high speed switch (J_{sw}) in parallel with a capacitor (C_J) and (nonlinear) resistance R_J. The parameters of typical junction devices are given for each junction in table 1 along with the combined value of both junctions.

Table 1. Parameter Values of Josephson Junctions
Used in Circuit Analysis

Junction	Area Factor	Icrit (ma)	CJ (pf)	RJ (ohm)	R0 (ohm)	Vg (mv)
J1	23	5.75	2.875	.30	3.0	2.5
J2	25	6.25	3.125	.28	2.8	2.5
Combination (series *)	N/A	6.	1.5	.58	5.8	5.

* This combination assumes the difference between Icrit values of J1 and J2 is insignificant. An average value for Icrit is used for the series combination of J1 and J2. The resulting analysis overestimates the degree of sharpening available, but gains simplicity. This approximation is further refined by subsequent design estimates when the fuller analysis provided by the JSPICE program is used.

2.1 CIRCUIT ANALYSIS BASED ON STATIC MODEL

Given the above circuits and the junction parameters, it is possible to sketch the "static voltage current curve" for the pair of Josephson junctions in series. Figure 3 shows the voltage that appears across the combination as the current approaches the critical values of current for J1 and J2, assuming that the current is applied slowly starting from zero. If the current rose rapidly, the voltage would rise to the same levels, but it also would be accompanied by a delay of a few ps. On the other hand, when the current falls below the lowest critical value the voltage may not drop to zero immediately. Just how low the current may fall before the voltage drops to zero is a function of the junction parameters, particularly of the combination known as β.

β is defined as

$$\beta = Ic*(Rn**2)*C/\Phi_0$$

Substitute for J_1, J_2
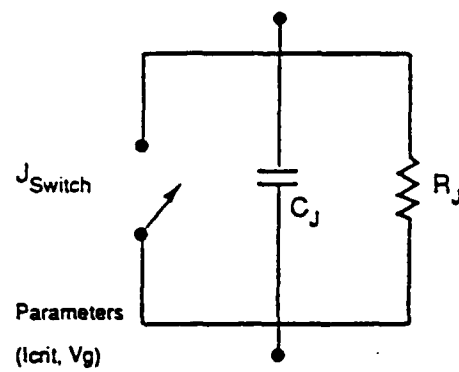
Figure 2. Josephson Junction Switch: Static Equivalent Circuit

Static Voltage-Current Curve for Edge Sharpner

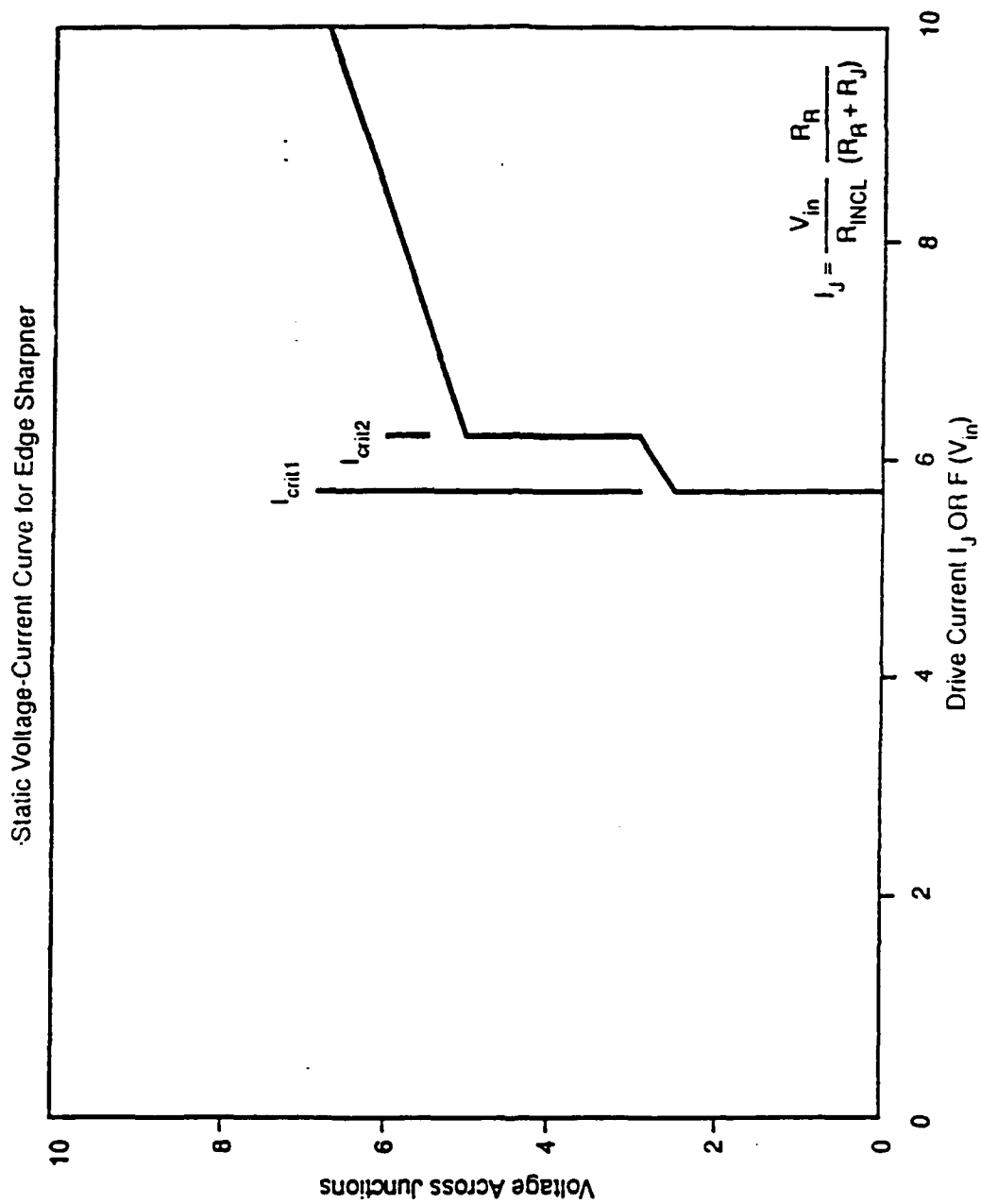$$I_J = \frac{V_{in}}{R_{INCL}} \cdot \frac{R_R}{(R_R + R_J)}$$

Figure 3. Voltage-Current Curve for Static Equivalent Circuit

where

Ic is the critical current of the junction
Rn is the normal resistance of the junction
    i.e. its resistance when it switches to
    the conducting state
C is the junction capacitance
Φ_O is the "quantum of flux" physical constant
    $= 2.07 * 10^{-15}$ Weber

However since the emphasis here is on the rising edge of the current and voltage the fall time need not be examined further.

For use in preliminary design analysis, we assume in figure 3 that the junction closes instantaneously. The time constant of the circuit in which the switch is located accounts for response-time effects. The equivalent circuit of figure 4 is the model used. For example, with R_J=.58 ohms, R_R and R_{INCL} is of significantly larger value, and C_J=1.5 pf, the effective time constant is .87 ps. In a circuit with this time constant, the response to a step function is about 2.5 times this value, i.e., the exponential rise time is 2.2 ps. This is the fastest rise time to be anticipated from the circuit.

2.2 DETAILED DISCUSSION OF EQUIVALENT CIRCUIT

In the circuit in figure 4, the Josephson junction pair is replaced by an equivalent switch, Jsw, which opens whenever the current through the junction pair exceeds the critical current of both junctions (which are at nearly equal values). The combination of the junction critical current parameters and the driving resistance, R_{INCL}, determines the value of input voltage, Vin, at which the switch opening occurs. If this V threshold is a fraction, f, of Vin, it determines the degree of sharpening between the rise rate of the input pulse and the output pulse. A consequence of this method of pulse sharpening is that the output pulse is delayed compared to the input pulse. A brief explanation is given of the other circuit values. The resistance of the Josephson junction, R_J, is supplemented by R_R, a circuit resistance value that allows design freedom toward choosing the circuit turn-on time constant. The capacitance value, C_J, is the capacitance of the junction. The overall time constant is governed by all these parameters, and specific equations are stated in following sections. The actual circuit rise time, TC, is determined by the typical exponential rise waveform, which is the response to a step input. Taking the definition of rise time to be the time it takes for the waveform to rise from 10% to 90% of its final value, this is fulfilled by a time interval about 2.5 times the exponential rise time constant.
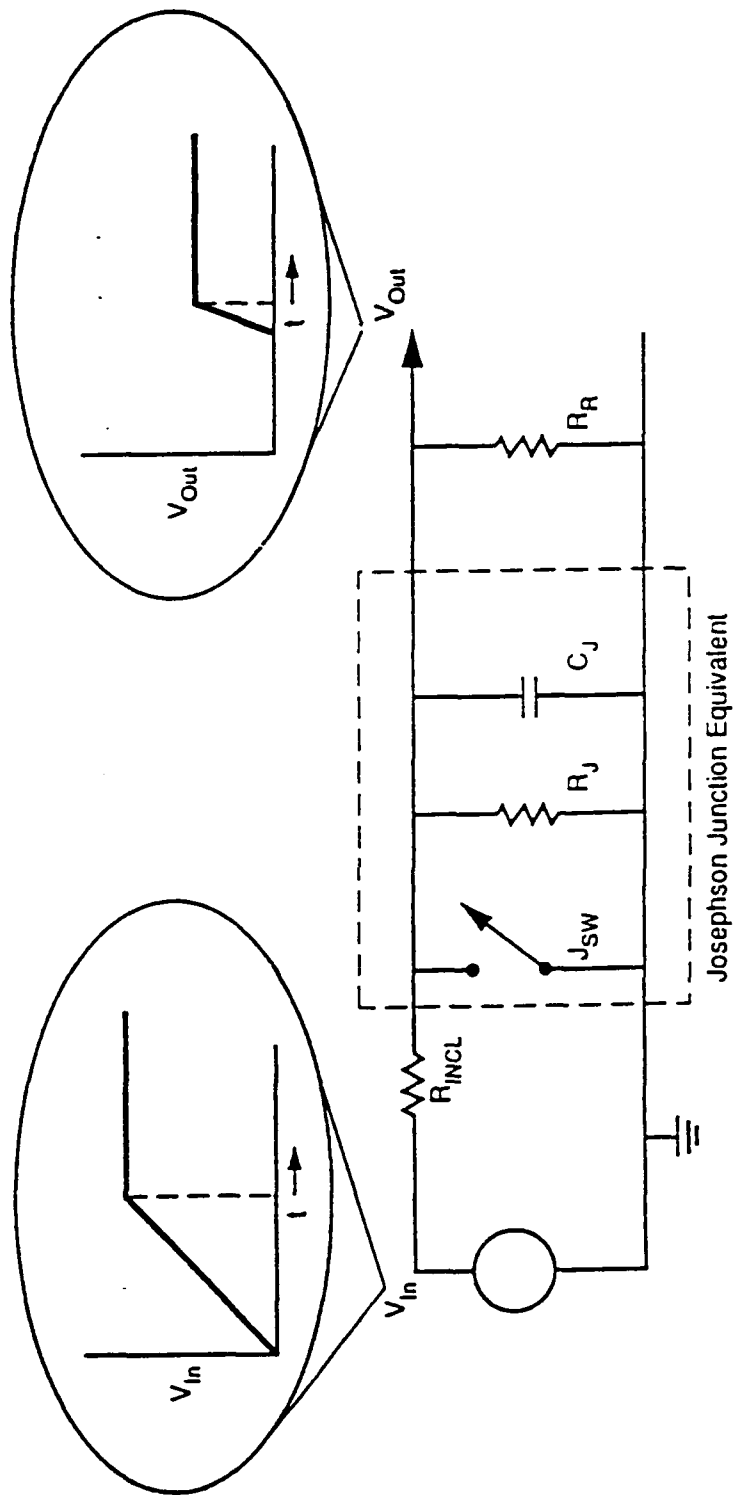
Figure 4. Edge Sharpener Equivalent Circuit

Some alternative descriptions of the edge sharpening process use different descriptive parameters. Using figure 5 as an illustration, various parameters can be defined.

$$f = 1 - \frac{t_{rs}}{t_{ru}}$$

where f is the fraction of maximum value of input waveform above which edge sharpener allows outputs.

$$g = \frac{t_{rs}}{t_{ru}} = 1 - f$$

where g is the sharpened rise time divided by the unsharpened rise time.

$$h = \frac{t_{ru}}{t_{rs}} = \frac{1}{g}$$

where h is the sharpening factor. Different authors may state the relationship in terms of any of these parameters.

It is understood that the sharpened rise times discussed above are for an ideal case that does not include circuit rise time. To take rise time into account, the sharpened rise time of figure 5 should be replaced by 2.5 times the exponential rise time, 2.2 ps in the current example, as determined by the equivalent circuit of figure 4.

Since the output maximum amplitude is generally less than the input amplitude for practical reasons in the operation of such a circuit, this relative amplitude factor is part of the circuit design, as are the relative time factors. Generally Vout is kept at a reasonable fraction of Vin, such as 1/2. This allows R_{INCL} to be large enough (compared to R_J) that it doesn't lower the effective time constant of the circuit. In addition, this resistance affects decoupling of the edge sharpening circuit from possible other A/D converter circuits being driven simultaneously from the same Vin. The value of R_{INCL} should be high enough to decouple the output circuit time constant from both the rise time of the input circuit and from interaction of multiple A/D converter clocks driven by the same output voltage. It should, therefore, be at least twice the normal resistance of the Josephson junctions. This consideration implies a voltage drop between Vin and Vout that is generally 2:1 or greater.

A conclusion of the present study is that, based on analysis of this static circuit, the switch drive current is given by:

$$I_J = (\text{Vin} / R_{INCL}) * R_R / (R_R + R_J) \tag{1}$$
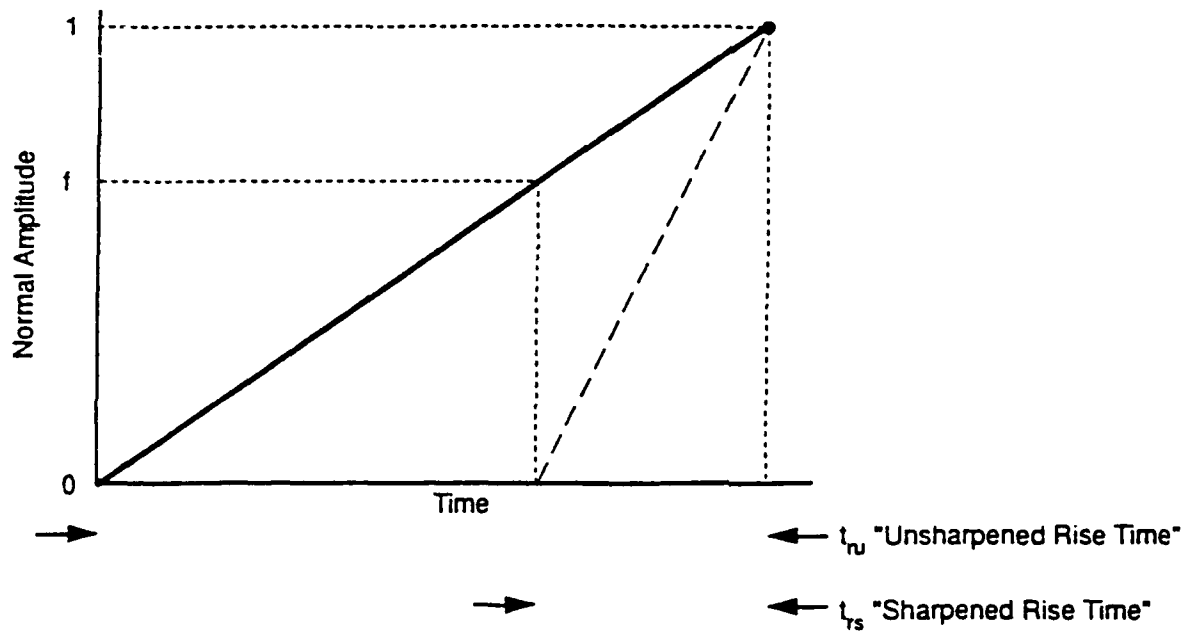
Figure 5. Relation Among Parameters Characterizing Sharpening

This equation relates the current to the input voltage and the circuit parameters. Edge sharpening occurs because the "shorting" of the switch holds Vout at 0 until Vin has risen to a point where Ij crosses Icrit. When Ij exceeds Icrit, the switch opens and is replaced by resistance Rj, which allows Vout to rise according to this circuit analysis.

2.3 CHOICES FOR BEST EDGE SHARPENING

The point at which the edge-sharpened rise begins, as a fraction of Vin, is f. This is the point at which I=Icrit. According to equation 1, however,

$$Icrit = f * Vin_{MAX} / R_{INCL}) * R_R / (R_R + R_J)$$

so that, if $R_R >> R_J$, as is the case for preferred designs,

$$f \approx Icrit * R_{INCL} / Vin_{MAX}$$

The sharpened rise time, Trs, is the time in which Vout rises from 0, which value it has while the switches are effectively closed before Icrit is reached, to the value it has in equilibrium when $Vin = Vin_{MAX}$. This rise time is subject to a minimum defined by the time constant of the output circuit. The relation of Trs to the original rise time, Tr is

$$Trs = MIN((1-f) * Tr , 2.5 * TC) \tag{2}$$

The minimum sharpened response time, as imposed by the output circuit time constant is a significant part of the design procedure. As indicated by equation 2, it is pointless to have higher values of f than strictly necessary. In the present case of a 5 ps rise time for Vin, a value of $f \approx .5$ is appropriate. An unnecessarily high value for f might lead to a less stable value of Vout, therefore it should be avoided.

If the rise time of Vin were 10 ps, then a design value of $f \approx .75$ would be appropriate with the same circuit conditions. Given Vin_{MAX}, f, and Icrit, the choice of R_{INCL} is given by

$$R_{INCL} = f * Vin_{MAX} / Icrit \tag{3}$$

A summary of the present simplified analysis is provided in figure 6, which illustrates input and output waveforms for a case with f=.5 and for a case with f=.75. An exponential time constant of 0.87 ps is accounted for in both illustrations along with the idealized time sharpening. In these figures, Ts indicates the (delayed) start of the output waveform, and Tf the end of the nominal rise time, including the exponential rise effect.
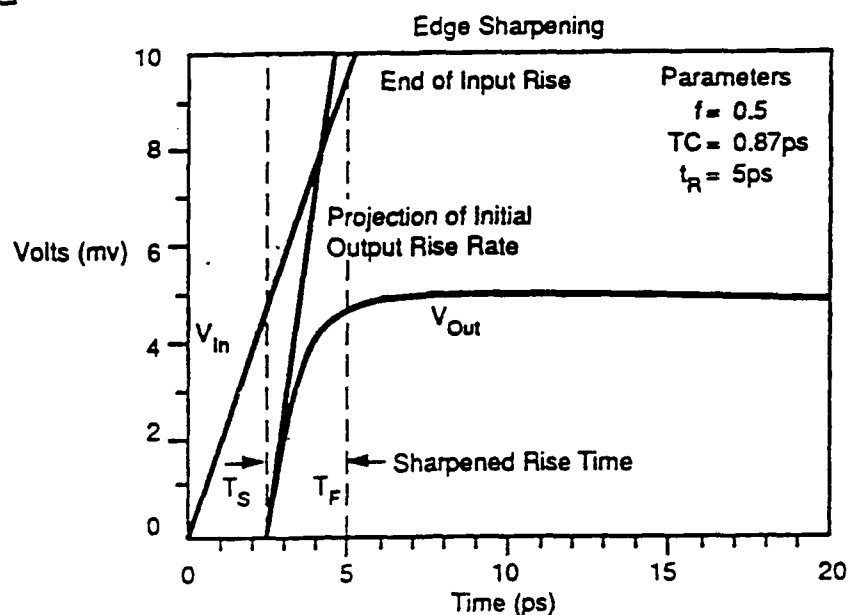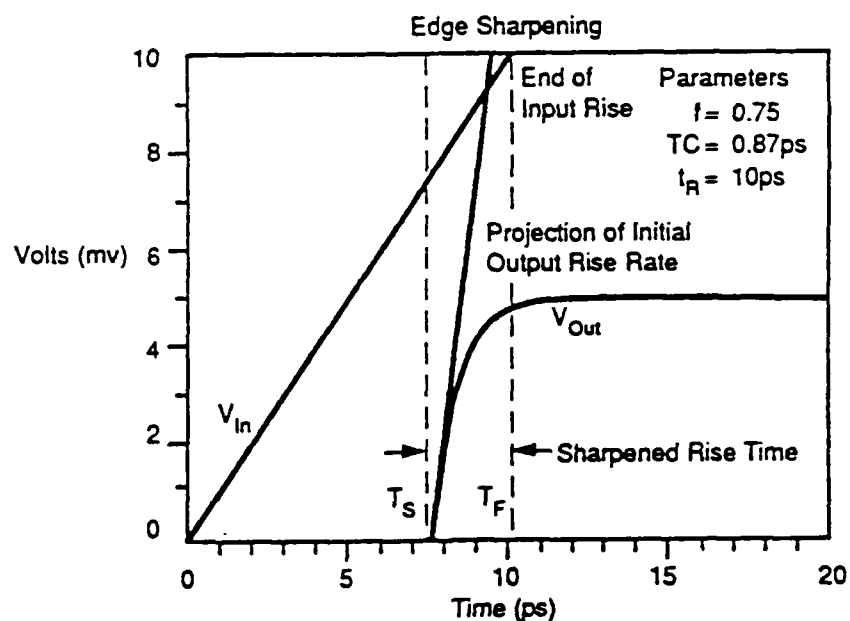
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a. Input and Output Waveforms With f = .5

b. Input and Output Waveforms With f = .75

Figure 6. Summary of Edge Sharpening Theory for Two Sample Cases

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2.4 CIRCUIT ANALYSIS USING JSPICE SIMULATION

The computer program JSPICE presents an analysis that is more thorough and more comprehensive than the previous mentioned analysis using a static model. The JSPICE analysis has been performed for a limited variety of conditions. Table 2 lists the parameters of a series of such runs, as annotated with brief comments about the comparison of input and output waveforms. The junction parameters of the runs, designated 1 and 2, were, not attainable in practice. The run results were included here, though, because they represent good edge sharpening, and otherwise conform to the basic design estimate procedure described above.

Table 2. Summary of Analytical Runs with JSPICE

RUN	Vin Max (mv)	AREA factor	Ic (ma)	C_J (pf)	R_N Ω	R_0 Ω	R_{INC} Ω	R_R Ω	COMMENTS
1	C 50	1	6.9	.15	5.83	58.3	4.	14	Sharpening output
		1	7.5	.15	5.83	58.1	4.	14	not saturated w/ Vin.
2	F 50	1	6.9	.15	5.83	58.3	4.	14	Param values impractical.
		1	7.5	.15	5.83	58.1	4.	14	
1A	C 50	23	5.75	2.9	.304	3.04	5.	0.96	No sharpening.
		25	6.25	3.1	.280	2.80	5.	0.96	Saturated output levels.
2A	F 50	23	5.75	2.9	.304	3.04	5.	0.96	
		25	6.25	3.1	.280	2.80	5.	0.96	
1B	C 70	23	5.75	2.9	.304	3.04	3.72	0.56	No sharpening.
		25	6.25	3.1	.280	2.80	3.72	0.56	Saturated output levels.
2B	F 70	23	5.75	2.9	.304	3.04	3.72	0.56	
		25	6.25	3.1	.280	2.80	3.72	0.56	
1D	C 15	23	5.75	2.9	.304	3.04	0.35	0.56	No sharpening.
		25	6.25	3.1	.280	2.80	0.35	0.56	Saturated output levels.
2D	F 15	23	5.75	2.9	.304	3.04	0.35	0.56	
		25	6.25	3.1	.280	2.80	0.35	0.56	
1F	C 15	23	5.75	2.9	.304	3.04	1.0	5.0	Good sharpening ~10 mv
		25	6.25	3.1	.280	2.80	1.0	5.0	in saturated output levels.
2F	F 15	23	5.75	2.9	.304	3.04	1.0	5.0	
		25	6.25	3.1	.280	2.80	1.0	5.0	

There were two series of runs that differed in the step size of the test clock waveforms. The 1-run series contains pulses that cover a large variation in amplitude in five stepped amplitude levels. The letter C adjacent to the run designation indicates the relatively coarse step size. The 2-run series contains five stepped-amplitude levels within a factor of 2 of the maximum. The letter F adjacent to the run designation indicates the relatively fine amplitude steps.

Because there were two junctions in series, of slightly differing properties, the two parameter sets are shown for each run. For the 1 and 2 runs, all physical parameters are identical: only the input amplitude steps differ. The area factor refers to a specific feature of the JSPICE model input. It allows a JSPICE element to have different parameter values with different invocations and with scalings of all the other parameters. Since the scaling is the same as the situation for different devices fabricated on the same monolithic structure, it represents a factual situation as well as an ease in modeling. In table 2, this factor has been applied: all tabulated parameters are given as the extended values, appropriate for circuit analysis. Comments are stated alongside each set of runs.

Figures 7-9 show the result of JSPICE analysis for Vin and Vout waveforms that correspond to parameter sets shown in the table 2. These analysis runs include progressive steps in the input waveform to illustrate performance for a variety of input voltage step values.

Figures 7 and 9, corresponding to runs 1, 2, 1F and 2F, respectively, illustrate the cases where edge sharpening occurred. In these cases, F is approximately 0.5 or more for some portion of the range of input voltage steps, and the output waveforms clearly are delayed from the input waveforms and have higher initial slopes. Figure 8 illustrates the case of the A runs and is also typical of the B and D runs where no edge sharpening occurred. For these cases the output waveforms for all input step values generally begin with less delay, and have slopes that never exceed the input waveform slopes.

These analyses corroborate the estimates, and add further details typical of actual Josephson junction operation, such as self-oscillation. This effect, which is unavoidable with Josephson junction circuitry, can only be accounted for by a full analysis such as JSPICE provides. This is one of the reasons that verification of any simpler design procedure should be carried out on at least a sampling of a set of design conditions. In the cases shown, the self-oscillation is small enough not to interfere with the essential waveforms needed to drive the clock for the A/D converter circuitry. In general, the magnitude of these oscillations depends on the combination of junction parameter values used, particularly of β.

These analyses support a case derived from 1F and 2F runs, in which Vin_{MAX} is 10 mv, Vout is 5 mv, R_{INC} is 1 ohm, and R_R is 5 ohms. For the indicated Josephson junction parameters, this case appears to be compatible with a set of A/D converter circuits, which are to be studied in the future, given driving waveforms derived from the edge sharpener.
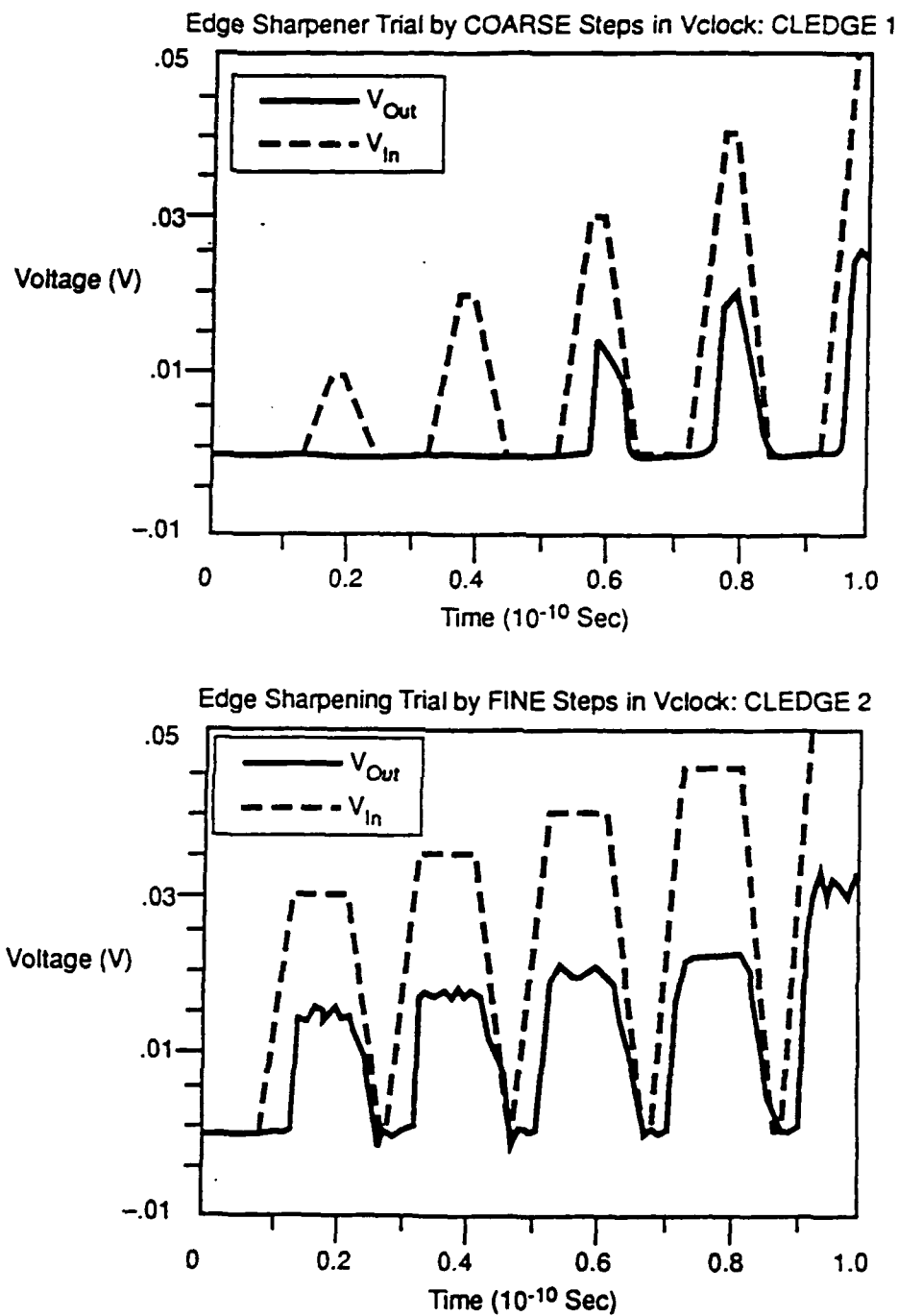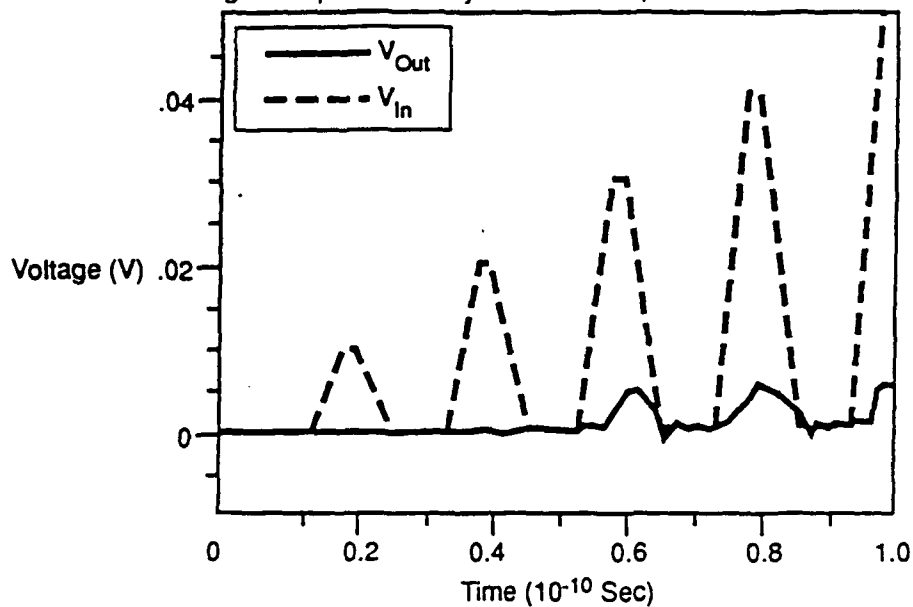
Edge Sharpener Trial by COARSE Steps in Vclock: CLEDGE 1

Figure 7. Input and Output Waveforms of Runs 1 and 2

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Edge Sharpener Trial by COARSE Steps in Vclock: CLEDGE 1A

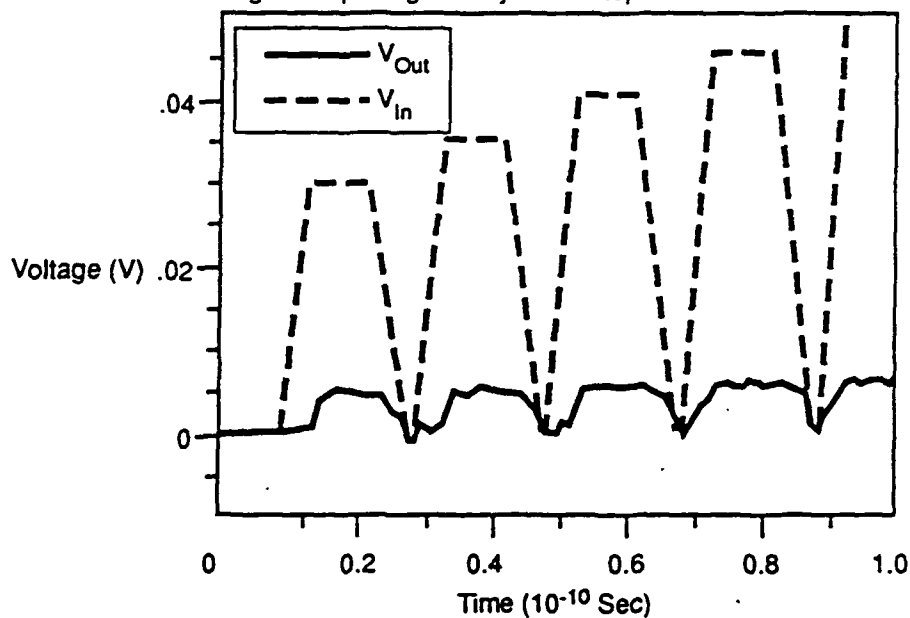

Edge Sharpening Trial by FINE Steps in Vclock: CLEDGE 2A

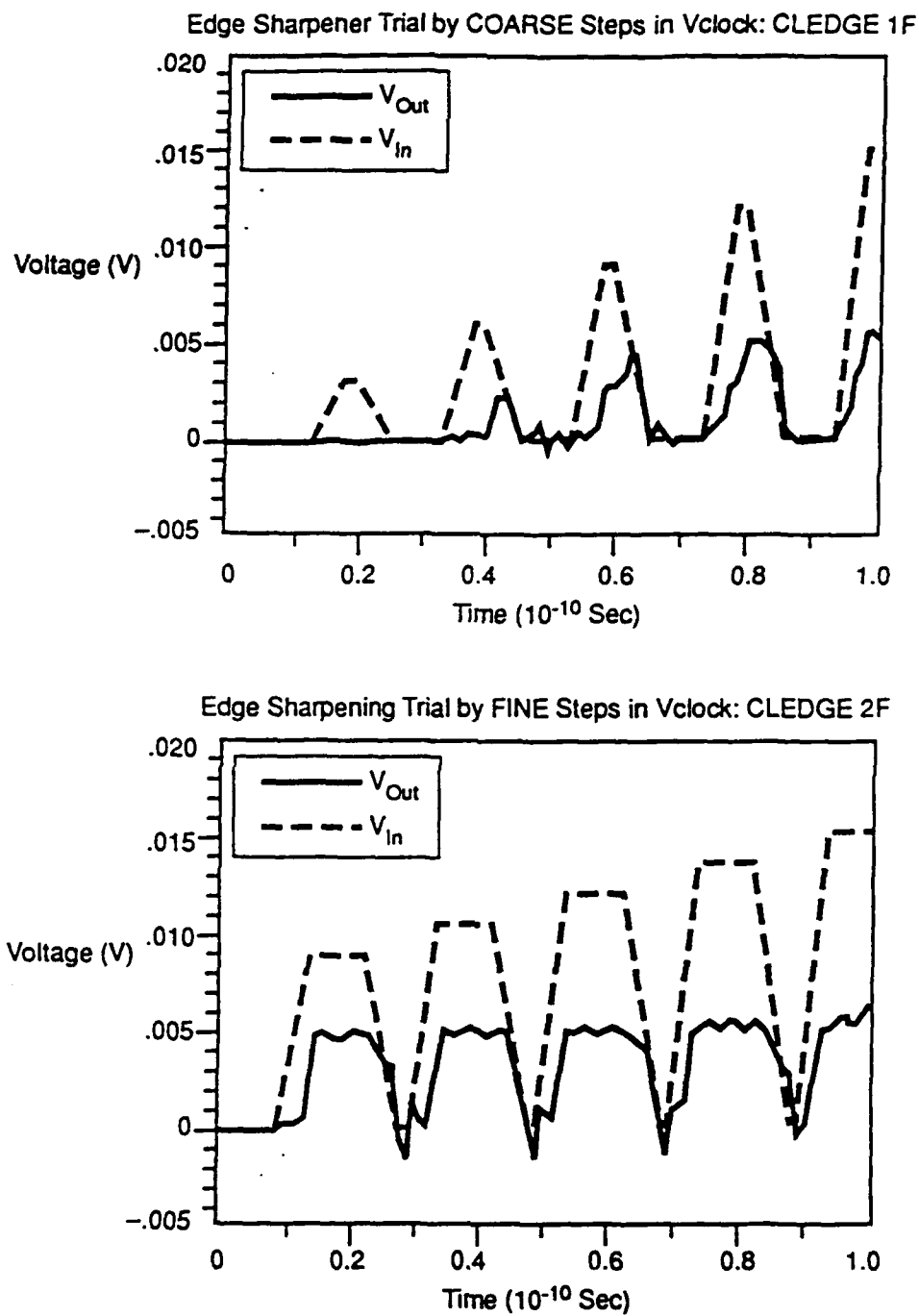

Figure 8. Input and Output Waveforms of Runs 1A and 2A

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Edge Sharpener Trial by COARSE Steps in Vclock: CLEDGE 1F

Edge Sharpening Trial by FINE Steps in Vclock: CLEDGE 2F

Figure 9. Input and Output Waveforms of Runs 1F and 2F

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SECTION 3

CONCLUSIONS

A design estimate procedure, as summarized in equations 1, 2, and 3, provides a working method for selection of the resistance values in Hamilton's edge sharpening circuit, given the driving clock voltage, Vin_{MAX}, the desired clock voltage for the driven A/D converter, Vout, the Josephson junction parameter values, the input rise time, and the required output rise time. For the examples followed up by JSPICE analysis, the equivalent circuit model and associated "rules of thumb" are confirmed. Edge sharpening results when the resistance values follow the formulas given, but not when they are outside the recommended conditions. While the simple design estimation procedure was effective in the particular examples discussed, there are enough parameter values and other complications to justify use of the more comprehensive JSPICE analysis -- at least to verify the appropriateness of initial design choices. The more recent JSIM procedures are expected to be even more efficient for design verifications.

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Technical Report 8

DESIGN EVALUATION OF A SUBRANGING SUPERCONDUCTING ANALOG-TO-DIGITAL CONVERTER

by

Margaret A. Poole

ABSTRACT

The development of high-speed, high-resolution analog-to-digital (A/D) converters is needed for many applications. Experimental superconducting A/D converters are fast, but have limited resolution. This working paper discusses design considerations for a subranging 16-bit, 125 megasamples per second, superconducting A/D converter which is suitable for HF receiver applications.

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SECTION 1

INTRODUCTION

Many applications require analog-to-digital (A/D) converters with higher precision and higher data rates than can be obtained from existing devices. Recent work on superconducting A/D converters has demonstrated their high speed but rather limited resolution. The objective of Project 91080 is to develop a 16-bit A/D converter with a sampling rate of 125 megasamples per second (MS/s). The state-of-the-art for semiconductor A/D converters is shown in figure 1 and table 1. Although a few converters with less than 8 bits and more that 16 bits exist, almost all development efforts are directed toward 8- to 16-bit converters. The trade-off between resolution (in bits) and conversion rate is clearly shown in the figure. Superconducting A/D converter development efforts have produced experimental devices with 6-bit resolution and conversion rates of a few gigahertz [1,2]. The results of development work on an 8-bit superconducting converter were very disappointing [3]. Thus a superconducting 16-bit converter would have a resolution far beyond that of other superconducting converters, and with a 125 MS/s sampling rate such a converter would be considerably beyond the state-of-the-art for semiconductor converters. An important application for such a converter would be in HF receivers with input frequencies from 5 to 30 MHz. A converter with a conversion rate of 125 MS/s could be used to sample the HF signal directly. Thus the input filter bank and the up and down converters typically used in HF receivers could be eliminated.

This is the first of two working papers evaluating alternative architectures for a superconducting A/D converter. A subranging converter is discussed in this paper. A second paper will investigate sigma-delta converter architectures. This report first provides some background on superconductivity in section 2 and then describes the subranging architecture in section 3. Next the effects of the converter specifications on the design are discussed in section 4. Sections 5 and 6 discuss the two major designs required: the track-and-hold circuit and the digital-to-analog converter with its associated analog circuits. The results of the study are summarized in section 7.
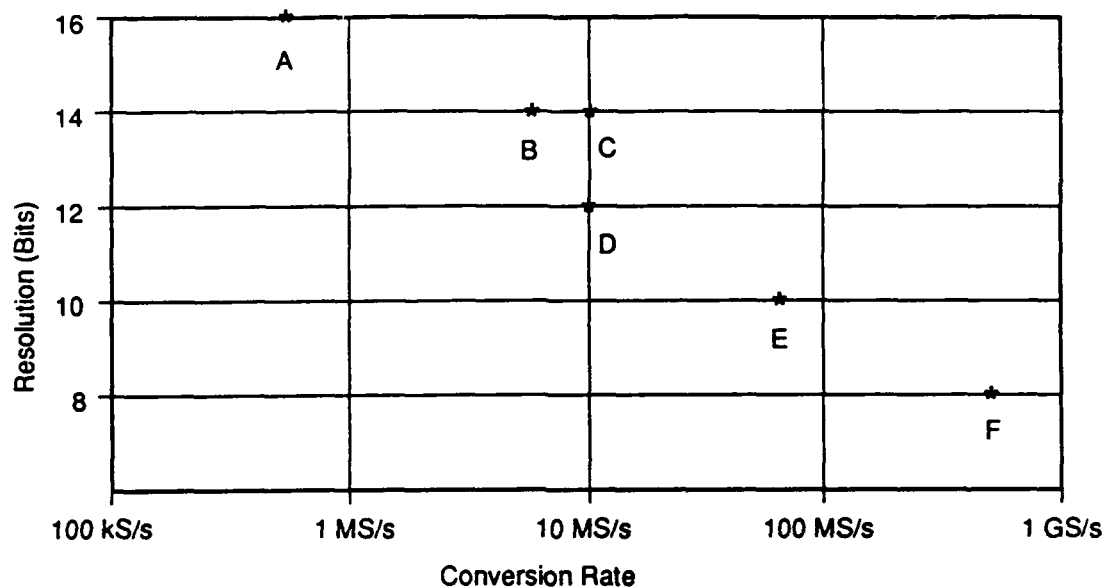
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Figure 1. State-of-the-Art A/D Converters

Table 1. A/D Converters

Letter	Manufacturer	Part No.	No. of Bits	Conversion Rate	Architecture	Status
A	Analogic	AM41216	16	500 kS/s	Subranging	Production
B	Westinghouse	WEC1405B	14	5 MS/s	Subranging	Limited Prod.
C	Analog Devices	AD9014	14	10 MS/s	Subranging	Prototypes
D1	Analog Devices	AD900	12	10 MS/s	Subranging	Production
D2	Burr Brown	ADC60	12	10 MS/s	Subranging	Production
E	Analog Devices	AD9060	10	60 MS/s	Flash	Prototypes
F	Tektronix	TKAD10C	8	500 MS/s	Dual Flash	Production

SECTION 2

SUPERCONDUCTIVITY BACKGROUND

2.1 SUPERCONDUCTING MATERIALS AND CHARACTERISTICS

The ability of materials to conduct current with zero resistance was discovered in 1911. Mercury, tin, and lead were found to suddenly become superconductive as the temperature was lowered to about that of liquid helium (4.2 K). Beginning in the 1950s, several hundred compounds (mainly niobium compounds) with critical temperatures in the 17 K to 23 K range were discovered. The breakthrough in high-temperature superconductivity occurred in 1986 with rare earth copper oxides. These materials fall into two basic types, 40 K, 95 K, and 125 K materials, of which the latter can be cooled with liquid nitrogen at 77 K. These high-temperature mixed-metal oxides have the mechanical and physical properties of ceramics. They are strong but brittle. Fabrication presents problems, and only a few experimental devices have been built. In contrast, fabrication of low-temperature superconductors is quite routine.

In order to remain in the superconducting state, a material must be held within an envelope of temperature, current density, and magnetic field strength. These critical values depend upon the material. DC current can flow in a superconducting material without loss. The resistance of the material to AC current is very low but not zero. Another phenomenon of superconducting materials is the Meissner effect. A low-temperature superconductor will not allow a magnetic field to penetrate its interior.* If a superconductor is approached by a magnetic field, it sets up currents on its surface that create an equal but opposite magnetic field. Thus if a magnet is placed above a superconductor, the opposing magnetic field will keep the magnet suspended above the superconductor.

A comprehensive microscopic theory of superconductivity was put forth by Bardeen, Cooper, and Schrieffer in 1957. According to this BCS theory, at low temperatures pairs of

---

* The action of a high-temperature superconductor is somewhat different.

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electrons (Cooper pairs), which normally repel each other, attract each other and form an electrical superfluid with energy levels a discrete amount below those of normal electron states. This difference in energy levels is the superconducting energy gap. The BCS theory does not completely explain the operation of high-temperature superconductors. As discussed in [4], the mechanism of high-temperature superconductivity is almost certainly different from that of low-temperature superconductivity. It is not possible to say what the parameters of high-temperature superconductors may be.

2.2 SUPERCONDUCTING DEVICES

Early proposed applications for superconducting materials were as current carriers in electric power systems and electromagnets. Our interest is in devices for electronic applications. Two important components are Josephson junctions and superconducting quantum interference devices. These devices have a number of important attributes: fast switching, low power, wide bandwidth, low noise, and high sensitivity.

2.2.1 Josephson Junction (JJ) Devices

In 1962 Josephson analyzed what would happen at the intersection of two superconductors which are separated by a thin insulating barrier. He predicted that a supercurrent would tunnel through the Josephson junction and that there would be no voltage drop across the junction provided that the current did not exceed a critical value. This DC Josephson effect results in the current-voltage characteristic shown in figure 2. As the current is increased, the JJ remains in its zero-voltage state until the current reaches the critical current, I_C. At that point, the JJ quickly switches along the load line to the voltage state at a voltage of about $2\Delta/e$ where Δ is the energy gap and e is the electron charge. The value of $2\Delta/e$ is about 2.9 mV. As the current returns to zero, the transfer curve is retraced back to zero.

Current

I_C
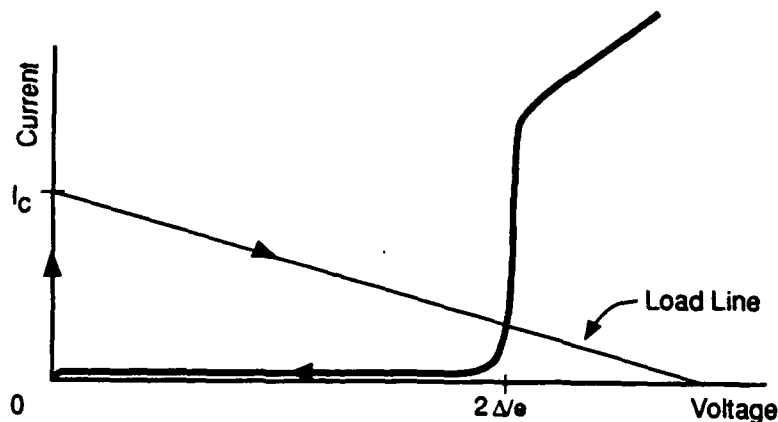
Load Line

0   2 Δ/e   Voltage

Figure 2. Josephson Junction Transfer Function

The theoretical switching speed from the zero-voltage to the voltage state has been predicted to be [5]

$$T_{SW} = \hbar/2\Delta$$

where

$\hbar$ = reduced Planck's constant = $h/2\pi$ = 1.0546×10^{-34} J-s

For Pb-alloy Josephson junctions, $T_{SW} \sim 0.23$ ps. A modeling study of practical single-junction devices has concluded that the narrowest pulse to which the junction can respond is about 2 ps [6]. Experimental tests of a Josephson junction sampler produced a rise time of 2.1 ps, and improved designs were predicted to have rise times of less than 1 ps [7]. Switching speed is limited by the junction capacitance, C, and the charging current, I. (Refer to the equivalent circuit in figure 3.) The smallest practical ratio of C/I is stated in [8] to be 0.5 pF per milliampere which corresponds to the approximate upper limit in junction current density of 10^4 A/cm^2 for Nb - Al$_2$O$_3$ - Nb junctions. Then the junction switching time would equal about 1.5 ps. This fast switching speed of about 1-2 ps is the reason for considering superconducting devices for the high-speed A/D converter.
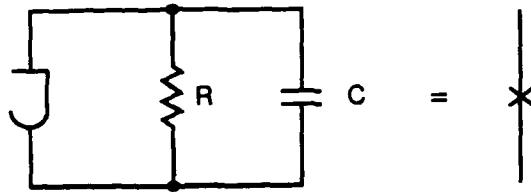
Figure 3. Josephson Junction Equivalent Circuit

Josephson also predicted that a DC voltage across the junction would create a high-frequency AC supercurrent. The frequency of this oscillation is

$$f = \frac{2e}{h} V = 483.6 \times 10^{12} \quad Hz/V$$

where

h = Planck's constant = 6.6262×10^{-34} J-s

V = DC voltage

This relationship between voltage and frequency was the basis of a previous A/D converter design approach. Two other Josephson effects also occur. If the voltage applied across the junction is equal to nhf/2e where n is an integer, and if an RF field is applied across the JJ, a direct supercurrent will flow. In addition, if an unbiased (zero current) JJ is radiated with an RF field, a DC voltage is generated across the junction. This voltage is at steps of nhf/2e. Although these AC effects are interesting phenomena, our interest is in the DC effect and the switching characteristics.

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2.2.2 Superconducting Quantum Interference Devices (SQUIDs)

A SQUID contains one or more Josephson junctions connected in one or more superconducting loops. RF SQUIDs are constructed with one JJ in one loop. DC SQUIDs usually have two JJs in one loop. These SQUID designations refer to the type of biasing used. The basic characteristic of SQUIDs is flux quantization where one flux quantum equals

$$\Phi_0 = \frac{h}{2e} = 2.07 \times 10^{-15} \quad Wb.$$

An important application for both RF and DC SQUIDs is as magnetometers in which magnetic flux passes through the loop. A flux-locked loop circuit is used to convert magnetic flux to voltage.

The flux quantization characteristic of DC SQUIDs can be used in another way. Consider the SQUID circuit shown in figure 4. The signal current I_S, is inductively coupled to the SQUID to produce a flux, Φ, through the SQUID loop. Biasing is provided by the current I. The output is the voltage across the SQUID. The output depends on I and I_S as shown in figure 5. If I_S produces an integral number of flux quanta through the loop, the output voltage for a given bias current is low. Other values of I_S produce higher output voltages. Thus the SQUID can be used as a flux-to-voltage converter with a periodic characteristic. This SQUID can also be used as a comparator with an output voltage of zero when the JJs are in the superconducting state or with an output voltage of the gap voltage of about 2.9 mV when the JJs are in the voltage state. The JJ critical current, I_C, depends upon the flux through the loop and hence upon the signal current, I_S, as shown in figure 6. As the analog input signal current, I_S, is varied, the current I is pulsed to be equal to I_{TH}. If I is less than I_C, the output remains at zero. If I is greater than I_C, the SQUID switches to its voltage state. The result is that the SQUID acts as a comparator. A "1" is produced whenever the SQUID is pulsed with I = I_{TH} greater than I_C, and a "0" is produced when the I = I_{TH} pulse is less that I_C. The value of I_{TH} is adjusted for equal "1" and "0" pulse widths.
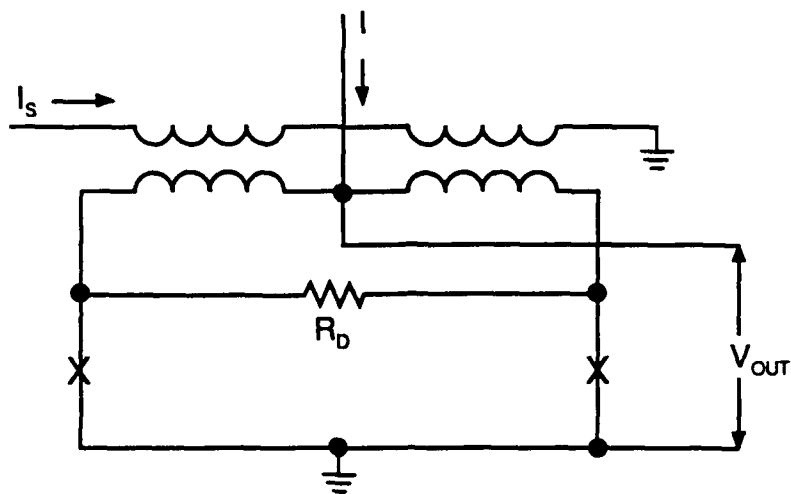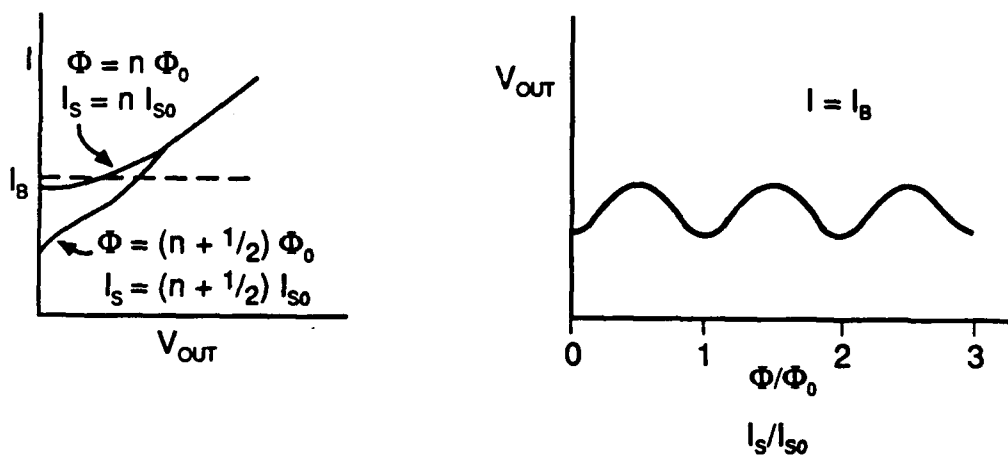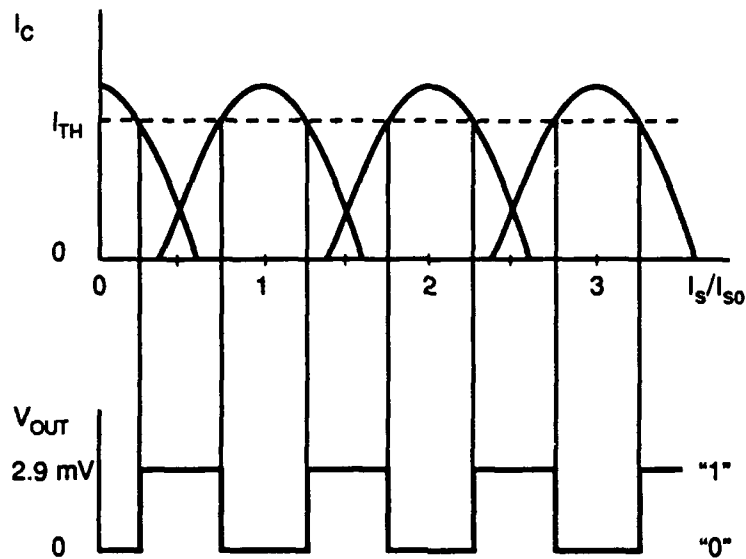
Figure 4. SQUID Circuit

Figure 5. SQUID Characteristics

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Figure 6. SQUID Comparator Operation

2.3 SUPERCONDUCTOR CIRCUITS

2.3.1 Analog-to-Digital Converters

The periodic relation between I_S and I_C is the basis for much of the previous superconducting A/D converter development work. The comparator output in figure 6 represents the output of the least significant bit (LSB) of the binary code as the input signal is increased in a SQUID. If a signal of $I_S/2$ is applied to a second SQUID, the pulse width out of this SQUID is twice as wide corresponding to the binary code of the second LSB. The same technique can be used to generate the other binary bits. With appropriate biasing applied to each of the SQUIDs to adjust the data transition points, the binary data representation shown in figure 7.A can be obtained. Thus N SQUIDs are required for the N-bit binary converter. In this parallel converter, all N SQUIDs sample the input simultaneously. A problem in all parallel converters exists if the sampling pulse occurs when the input signal is at a level corresponding to a data transition in two or more bits (or
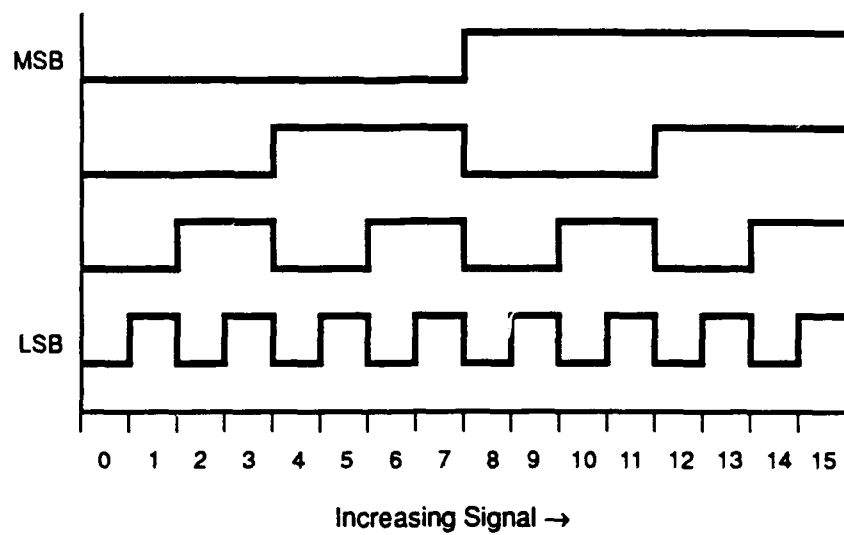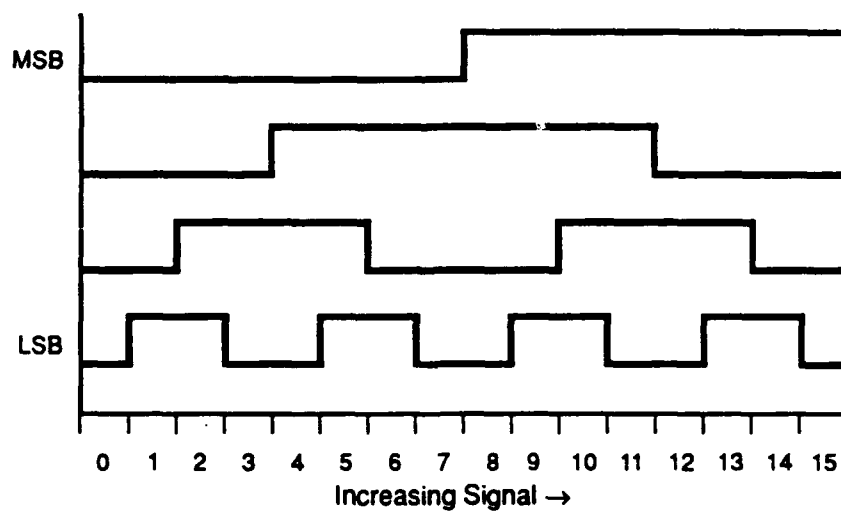
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Figure 7.A. Binary Code

Figure 7.B. Gray Code

Figure 7. Digital Representations

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SQUIDs). For example, in figure 7.A an input changing from an equivalent binary seven to eight produces transitions in all four bits (or SQUIDs). A sampling pulse at that time could produce any of 2^4 binary outputs. The solution to this problem is to use a Gray code in which no more than one bit has a data transition for any specific input. Figure 7.B illustrates a Gray code that can be implemented by suitable attenuation and biasing for each SQUID.

Previous superconducting A/D converter development efforts [1,2,9,10] have produced 4- or 6-bit converters of this type with sampling rates of an few gigasamples per second. An attempt to increase the number of bits to eight resulted in a device with a sampling rate of only a few megasamples per second [3].

2.3.2 Track-and-Hold Circuit

Only one superconducting T/H circuit has been reported in the literature [11]. This experimental device had a bandwidth of 1.2 GHz and a dynamic range of 25 dB (about 4-bit resolution). The actual switching time from track to hold was not measured. However, this transition was accomplished by switching a Josephson junction from its voltage state to its zero-voltage state. This transition is known to be much slower than the very fast transition in the other direction. The authors predict that an optimized circuit could achieve a 4 GHz bandwidth and a 35 dB dynamic range (about 6-bit resolution). Thus the performance of this circuit falls far short of our requirements for 16-bit resolution (about 98 dB dynamic range). The switching time is also too slow as will be discussed in section 4.2.

2.3.3 Digital Logic

Josephson logic circuit technology has been described in [12] as "primitive." Many different configurations for basic AND and OR circuits are still being investigated. The most complex devices reported in the literature are 4-bit counters, 8-bit adders, 4-bit multipliers, a 16-bit ALU, a 4096-bit RAM, and a 4-bit slice microprocessor. Nevertheless, Hitachi and Fujitsu have recently announced Josephson computers [13] consisting of a few chips. Thus designing with superconducting digital logic is possible.

2.3.4 Analog Circuits

Some analog signal processing circuits suitable for radar applications have been developed. These circuits include tapped delay lines, convolvers, correlators, and resonators [14]. A few superconducting video amplifiers have been reported. However, no superconducting transistor with gain exists [15,16]. Josephson junction devices are basically two-state devices and are not generally suitable for analog applications. In addition, JJs are two-terminal devices which lack a third terminal for control.

SECTION 3

SUBRANGING A/D CONVERTER ARCHITECTURE

The most commonly used architecture for high-resolution A/D converters is the subranging architecture. Figure 8 is a simplified block diagram of a two-stage subranging converter. The most significant bits (MSBs) are determined by A/D #1. These MSBs are then converted back to analog and subtracted from the original analog signal. The analog difference is then digitized by A/D #2 to obtain the least significant bits (LSBs). Because analog-to-digital conversion is a two-step process, a track-and-hold (T/H) circuit is needed. The A/D converters are usually implemented as flash converters for high-speed conversion. The accuracy requirements of A/D #1 can be reduced greatly by providing a one-bit overlap with A/D #2. The digital logic performs the arithmetic needed to produce an N-bit output from the total of N + 1 bits from A/D #1 and A/D #2.
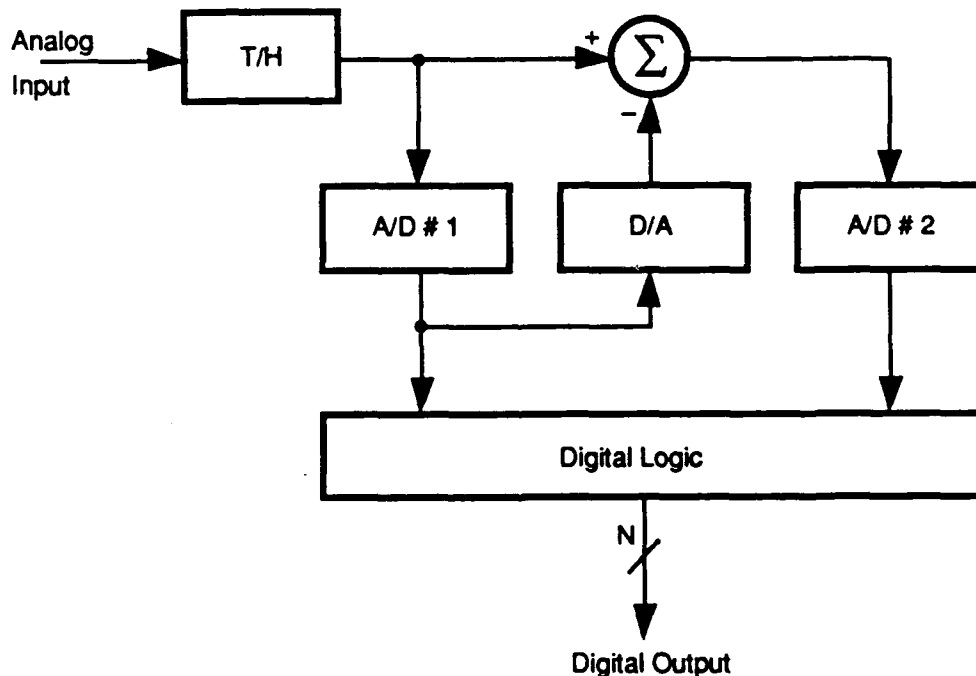

Figure 8. Two-Stage Subranging A/D Converter

The proposed superconducting A/D converter architecture is shown in figure 9. Three stages are necessary to achieve 16-bit resolution using 6-bit superconducting A/D converters of the type developed in [1,2]. There is a one-bit overlap between stages. The Gray-to-binary converters, registers, and correction logic can be implemented with superconducting digital logic. Because MITRE has no previous experience with superconducting circuits, implementation of the shaded blocks in figure 9 will require a considerable effort. However, the major design tasks are the analog circuits. The possibility of implementing these analog circuits with superconducting or other technologies is investigated in later sections of this report.
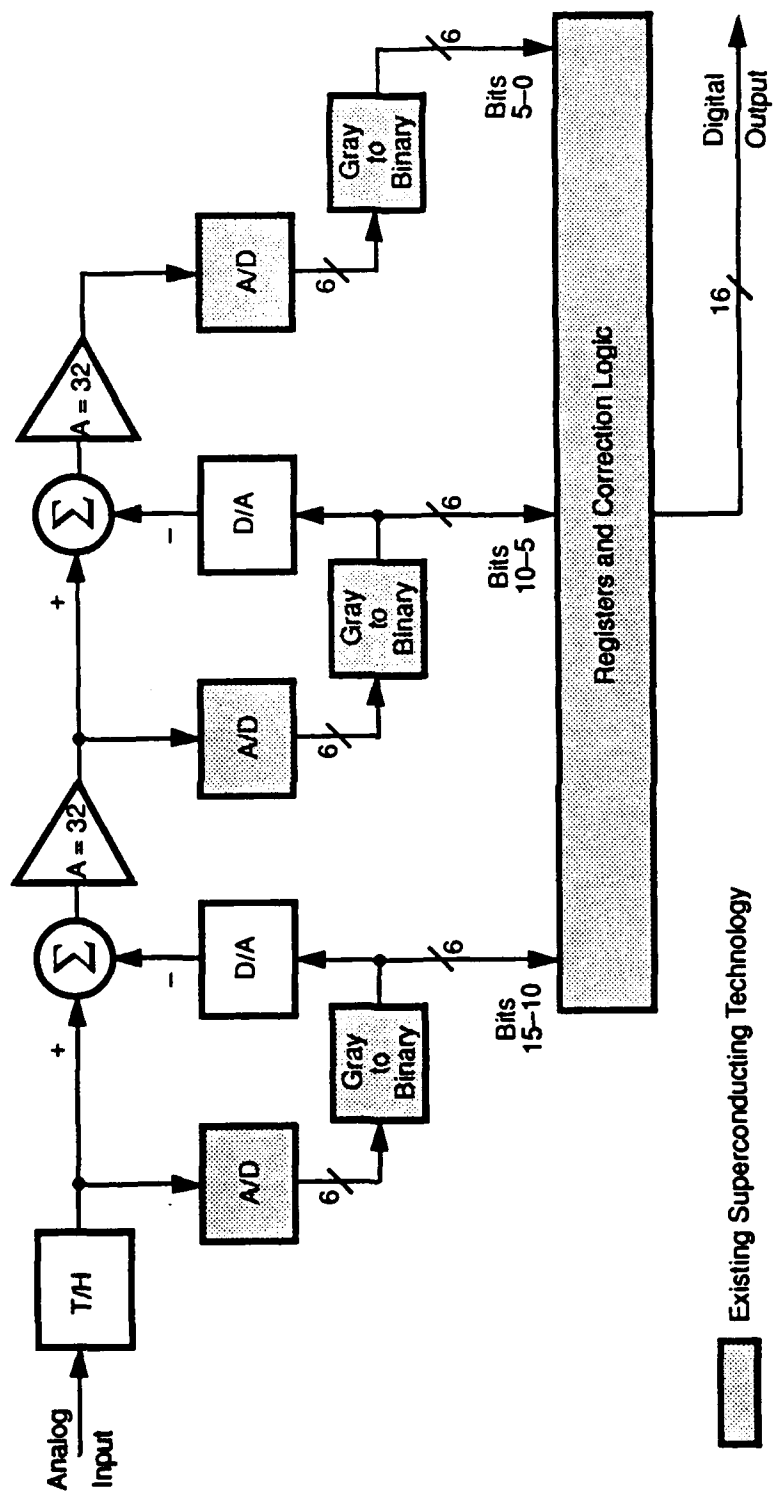
Figure 9. Proposed Superconducting A/D Converter

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SECTION 4

EFFECT OF A/D CONVERTER SPECIFICATIONS ON CIRCUIT DESIGN

4.1 A/D CONVERTER SPECIFICATIONS

The objective of this project is to develop a superconducting A/D converter with 16-bit resolution, a 125 MS/s sampling rate, and a maximum input frequency of 30 MHz. In order to understand the significance of these specifications, a brief discussion of A/D converter terminology and characteristics may be helpful.

The signal-to-noise ratio of an ideal N-bit converter is given by

$$SNR = 6.02\,N + 1.8 \text{ dB}$$

in which the only noise is ideal quantization noise. Other noise sources in actual converters include thermal noise, internal noise, nonideal quantization noise, and aperture jitter. Other sources of noise in the system include power supply noise and sampling clock jitter. Nonideal converters also cause distortion due to nonlinearities. This distortion is in the form of signal harmonics, intermodulation products, and spurious frequencies. A common converter specification is signal-to-noise-and-distortion (SINAD). The effective number of bits of a converter is usually defined as

$$N_{\text{eff}} = \frac{SINAD - 1.8}{6.02}$$

where SINAD is in dB. Thus the effective number of bits takes into account the degradation due to all kinds of noise and distortion in the converter. The effective number of bits is usually almost as large as the actual number of bits when the sampling rate and the input frequency are low. As the sampling rate and the input frequency increase, the effective number of bits decreases.

4.2 APERTURE JITTER

Aperture jitter is defined as the A/D converter variation in sampling time. For a rapidly changing input signal, aperture jitter can result in large errors in the digitized output. Consider a sampling time error of τ as shown in figure 10.
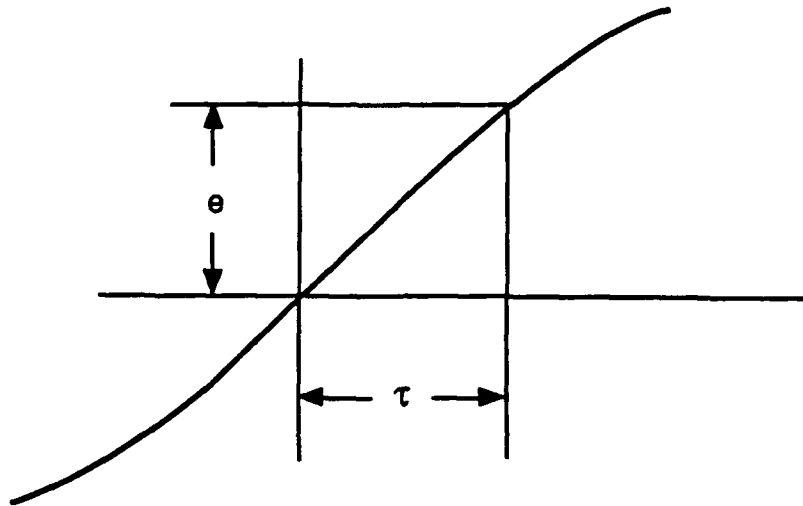

Figure 10. Sampling Time Error

This timing error produces a voltage error, e, in the quantized output. The problem is most severe for samples near the zero-crossing points of high frequency input signals. A sine wave with an amplitude of one volt has a maximum slope of 1 V/rad = $2\pi f$ V/s. For an N-bit converter, an error e $= 1/2^{N-1}$ corresponds to one quantization step. Therefore, an aperture error of $\tau = 1/2^N\pi f$ will produce an error of one quantization step. For N = 16 and f = 30 MHz, $\tau = 160$ fs. Specification sheets for A/D converters usually give an rms value for the aperture jitter. The A/D converter signal-to-noise ratio produced by an rms aperture jitter of σ is equal to [17]

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$$SNR = 20 \log (1/2\pi f\sigma) \quad dB$$

For the aperture jitter noise to be less than the ideal quantization noise, σ must be no greater than 70 fs rms. The ability of a superconducting A/D converter to meet this requirement is a major concern. Note that the allowable aperture jitter depends only on the number of bits and the input frequency and is not related to the sampling rate. The uncertainty in switching instants can be minimized by using a device with a very fast switching time. The aperture jitter can also be minimized by minimizing the rise time of the sampling pulse. For an A/D converter with a track-and-hold circuit at its input, the aperture jitter is the timing jitter of the T/H at the track-to-hold transition.

4.3 ACCURACY

Accuracy has three components: DC offset, gain, and linearity. A DC offset anywhere in the entire circuit will cause a DC component in the digital output of the overall A/D converter. In many cases, this offset is unimportant. In those cases where it is important, subsequent digital signal processing can eliminate it. For the track-and-hold circuit, the gain does not matter just as the gain of the circuits preceding the T/H circuit does not matter. The one T/H parameter that is important is linearity. The required accuracy of the A/D converters in the subranging architecture is only about one part in 2^6. The circuits which must have gain and linearity accuracies of one part in 2^{16} are the D/A converters, summers, and amplifiers. (Refer to section 6.1 for a more detailed explanation.)

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SECTION 5

TRACK-AND-HOLD CIRCUIT DESIGN

5.1 STANDARD TRACK-AND-HOLD ARCHITECTURE

A basic track-and-hold (T/H) circuit is shown in figure 11. Operational amplifier (op amp) A1 is a voltage follower which provides isolation between the analog input and the rest of the circuit. During the track mode, switch S is closed so that the voltage across capacitor C follows the input signal. Op amp A1 must be fast and have a low output impedance for charging C. When switch S is opened, the capacitor holds its charge because the input impedance of op amp A2 is very high. A2 is another voltage follower with sufficiently low output impedance to drive the circuits which follow. Thus the basic building blocks for a T/H circuit are a fast switch, voltage followers with high input impedances and low output impedances, and a capacitor. Nonideal components produce a variety of deviations from ideal performance as discussed in [18-20] and elsewhere. The design of a T/H with 16-bit performance will be very difficult. The problems in implementing a T/H circuit and alternative design approaches are discussed in the following sections.
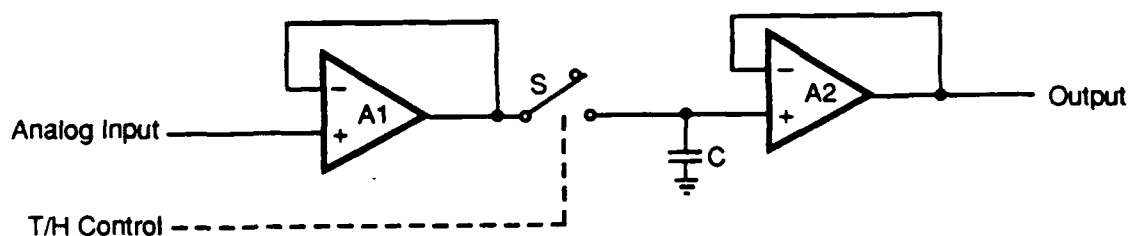
Figure 11. Basic Track-and-Hold Circuit

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5.2 VOLTAGE FOLLOWER DESIGN

The voltage follower parameters which affect the performance of the track-and-hold circuit are linearity, speed, noise, input impedance, and output impedance. Unity gain is not important, and DC offset can probably be compensated for later.

The voltage followers in figure 11 are shown as op amps because this is the type of integrated circuit used in present designs. The use of a simpler circuit, such as an emitter follower or Darlington circuit, should also be investigated. If an op amp is required, its design will be a major undertaking. (Refer to section 6.3 for a discussion of amplifier design.)

5.2.1 Superconductor Devices

No superconducting op amps exist. Neither are there any amplifiers that can cover a frequency range from DC to 100 MHz or more. There is not even a superconducting transistor for use as an emitter follower. Three-terminal transistor-like devices with power gain do not exist.

Only two devices show some potential. One is a superconductive magnetoelectric field-effect device which has high input impedance and low output impedance [21, 22]. This device is best described as a controlled switch with a Josephson junction as the switch. The operation of the circuit can be linearized somewhat by shunting the junction with a resistor to produce more transistor-like characteristics. An operational amplifier could probably be built with these devices. However, the linearity of such an op amp would almost certainly be inadequate to suppress harmonics and intermodulation products by the 98 dB needed to meet our specifications. The second device is a superconductor/superconductor/semiconductor bipolar transistor. According to a modeling study, this device should have gain [23]. However, no actual devices have been built.

5.2.2 Semiconductor Devices at Low Temperatures

One method of obtaining high-speed computer operation is to use CMOS field effect transistor (FET) circuits at low temperatures. At 77 K the switching speed of CMOS circuits is improved by a factor of two or more [24, 25]. The inherent small gate size and low power consumption of CMOS circuits allow very dense packaging. The ETA 10 computer has been developed for operation at 77 K [25]. The specially designed CMOS IC used in this computer is a 20,000-gate, 1-cm square gate array. The complete 3,000,000-gate CPU is packaged on a single printed circuit board, and cooling is not a major problem.

Low temperature CMOS operation has many advantages, but a few potential problems: hot-carrier effects, carrier freezeout, and 1/f noise. Characterization of experimental MOS devices has demonstrated the peculiar subthreshold current behavior caused by freezeout [26]. This kink in the current voltage curves is present at 77 K but becomes more pronounced and hysteretic at 4.2 K. The physics governing this operation is not well understood, but a model has linked it to a transient lasting milliseconds to seconds [27]. A solution to this problem must be found before we can consider using MOS transistors at 4.2 K.

Published information on low temperature operation of gallium FETs (MESFETs, MODFETs, IGFETs, HEMTs, etc.) is very limited. Recently a manufacturing method for eliminating the kink in the current voltage curves of an AlInAs-GaInAs HEMT has been reported [28]. Much more device development is needed to produce an operational FET at 4.2 K. In addition, power dissipation may be a problem at 4.2 K.

Silicon bipolar transistors exhibit a severe reduction in current gain ($\beta= I_c/I_b$) as the temperature is reduced. Some progress has been made in improving low-temperature betas. Reference [29] reports transistors with $\beta > 25$ at 77 K, but $\beta > 3$ at 9 K. This transistor is not useful at 4.2 K. The use of polysilicon emitter contacts can actually produce an increase in beta as the temperature is reduced to 77 K [30], but other parameters of this transistor such as punch-through voltage are degraded [31]. The fabrication of a silicon pseudo-heterojunction bipolar transistor (HBT) with increasing current gain to a beta of 107 as the temperature is

lowered to 77 K has been reported [32]. The beta of this transistor at 4.2 K was not measured, and neither were its other parameters. Power dissipation may also be a problem for bipolar transistors at 4.2 K. At the present time, no bipolar transistor which is suitable for our application exists.

5.2.3 Vacuum Microelectronic Devices at Low Temperatures

Vacuum microelectronics is a new technology which uses semiconductor lithography to build vacuum tubes of micrometer dimensions and submicrometer tolerances. These devices use field emission from cold cathodes rather than thermionic emission. The devices are faster than semiconductors, insensitive to temperature changes, and radiation tolerant. The cross section of a triode is shown in figure 12.
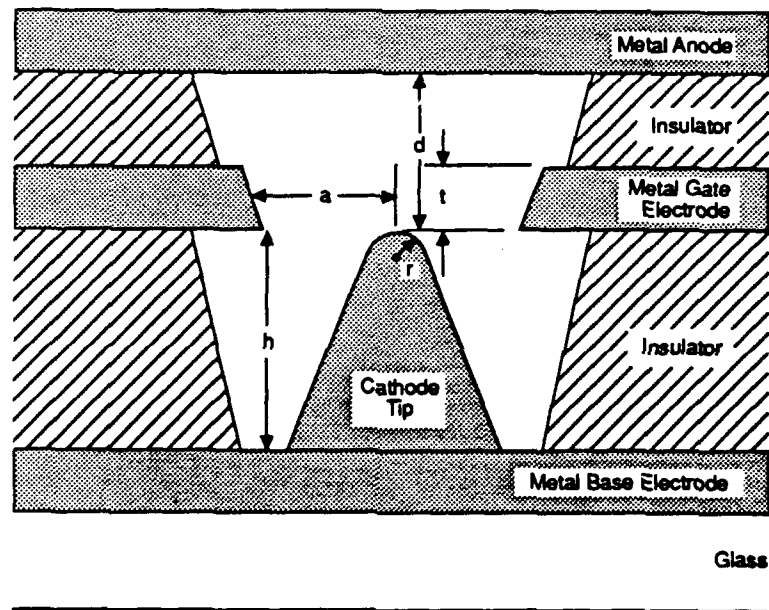

Figure 12. Vacuum Microelectronic Triode

As discussed in [33], the dimensions are determined by the electron mean free path, λ_e, for collision with residual gas molecules. From the kinetic theory of gases

$$\lambda_e = \frac{T}{273\ P\ P_c(v)} \quad mm$$

where

T   = absolute temperature in degrees K

P   = pressure in torr (1 atmosphere = 760 torr)

P_c (v) = probability of collision as function of voltage
(function of type of residual gas)

The distance, d, from cathode tip to metal anode should be about $10^{-2}\ \lambda_e$, and the distance, a, must be less than or equal to d. At T = 300 K and P = 1 torr (~10^{-3} atmosphere), reasonable dimensions are d = a = 0.5 μm. These dimensions are consistent with photolithographic capabilities. An anode voltage of 20 V will produce an electron transit time of 0.38 ps without vacuum breakdown. Thus these devices should be very fast.

The insensitivity of vacuum microelectronic devices to temperature is shown by considering the gas law

$$PV = kT$$

where

P = pressure

V = volume

25

T = absolute temperature

k = constant

The volume of the residual confined gas remains constant as the temperature is lowered so that

$$V = k \frac{T}{P}$$

Then the mean free path becomes

$$\lambda_e = \frac{V}{273 \, k \, P_c(v)} \; mm$$

which is independent of temperature. Thus a device which operates at room temperature should also operate at 4.2 K. Note that the residual gas for the vacuum devices must be helium to prevent condensation at temperatures near 4.2 K. Another consideration is excessive power dissipation which may make operation at 4.2 K impractical, especially if high power supply voltages are needed. Device fabrication is discussed in more detail in [34] and [35]. Some fabrication problems have been experienced. No characterization of experimental devices has been reported.

5.2.4 Synopsis of Voltage Follower Design Alternatives

No superconducting transistors exist. Josephson junctions are bistable devices which are useful in digital logic circuits, but are generally not suitable for analog applications.

CMOS FET transistors have been used in digital circuits at 77 K. At 4.2 K, freezeout produces irregularities in the current-voltage characteristics. Gallium FETs exhibit the same problem. Although the physics of this effect are not well understood, some progress has been made in eliminating the problem in gallium FETs.

The current gain, β, of silicon bipolar transistors drops rapidly as the temperature is lowered. The use of polysilicon emitter contacts has produced transistors with high betas at 77 K, but other parameters are degraded. No transistor with a usable beta at 4.2 K has been reported.

Although semiconductor devices, both FETs and bipolar transistors, that can operate at 77 K presently exist, the field of high-temperature (up to 95 K) superconductivity has not advanced very far. It is uncertain which will be developed first--high-temperature superconductor devices or semiconductors for 4.2 K operation.

Vacuum microelectronic devices have the advantage of being insensitive to temperature. A few experimental diodes and triodes have been built using this new technology, but the devices have not been characterized. If no unexpected effects occur, practical devices may be developed within a few years.

5.3 SWITCH DESIGN

The characteristics of the switch in figure 11 are critical to meeting the A/D converter specifications. The switch must be very fast (<1 ps track-to-hold switching time) as discussed in section 4.2 This switch must also have very low resistance when closed and very high impedance when open. A Josephson junction cannot be used because of its low resistance when open. This is the reason why the superconducting track-and-hold circuit mentioned in section 2.3.2 had such poor dynamic range. Two alternative switch design approaches which make use of extremely fast laser pulses for controlling the switch are discussed in the following sections.

5.3.1 Optoelectronic Switch

A very simple optoelectronic switch can be built by using a photoconductive material to span the gap between two conductors. When a laser illuminates the photoconductor, the

absorption of photons produces electron-hole pairs in the photoconductor, thereby making a connection between the two conductors. When the laser is turned off, the connection is broken.

Optical pulses as narrow as 6 fs [36] and up to a few nanoseconds can be generated. The pulse needed for the T/H switch has a width of about 4 ns and a fall time corresponding to the track-to-hold transition of much less than a picosecond. The rise time is not critical. Laser pulse shapes may be Gaussian or may have extremely fast rise times but approximately exponential fall times. Although several pulse shaping techniques exist [37,38], achievement of such a fast fall time for a wide pulse is probably not possible.

Photoconductors also exhibit a very fast transition to the conducting state because electron-hole pair generation is intrinsically fast. However, recombination during the transition to the nonconducting state is much slower. A standard technique for reducing the recombination time is to deliberately introduce defects into the photoconductor. Nevertheless, the turn-off time corresponding to the track-to-hold transition is much too slow for our application. Thus neither the laser pulses nor the photoconductor response characteristics exhibit the needed shapes.

5.3.2   Optoelectronic Trigger for Vacuum Microelectronic Switch

Although wide pulses with fast fall times cannot be generated using lasers and photoconductors, narrow pulses with ultrafast rise times are routinely produced. These fast pulses, although not jitter-free as usually described, can more than meet our requirement of 70 fs rms jitter. These pulses can be used to trigger a one-shot circuit which in turn produces square pulses to control a switch. Of the technologies discussed in section 5.2, vacuum microelectronics is the only one that has a chance of being fast enough for the one-shot circuit.

With regard to the switch itself. a FET switch would probably be too slow. FETs also have odd behavior at low temperatures. One type of switch which is frequently used is a diode bridge as shown in figure 13. A possible implementation of a switch control circuit is
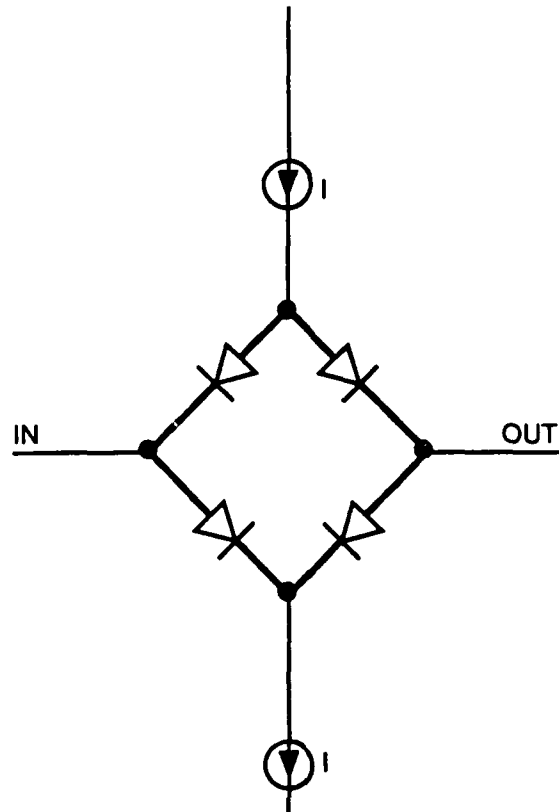
Figure 13. Diode Bridge Switch

shown in figure 14. In figure 13 when both current sources are on, the output voltage is the same as the input. When the current sources are off, the output is isolated from the input by the reverse resistance of the diodes. In this circuit also, speed considerations necessitate the use of vacuum microelectronic technology. Implementation of the NPN-type current source is simple. A possible circuit for the PNP-type current source is shown in figure 14. Because the FET is always on, its speed is unimportant, and its operating point can probably be set to avoid troublesome regions. Vacuum microelectronic technology must be developed further before implementation of this circuit can be seriously considered. Although this type of switch may be fast enough, the circuit may not be accurate enough. There probably is no way to predict what the accuracy will be.
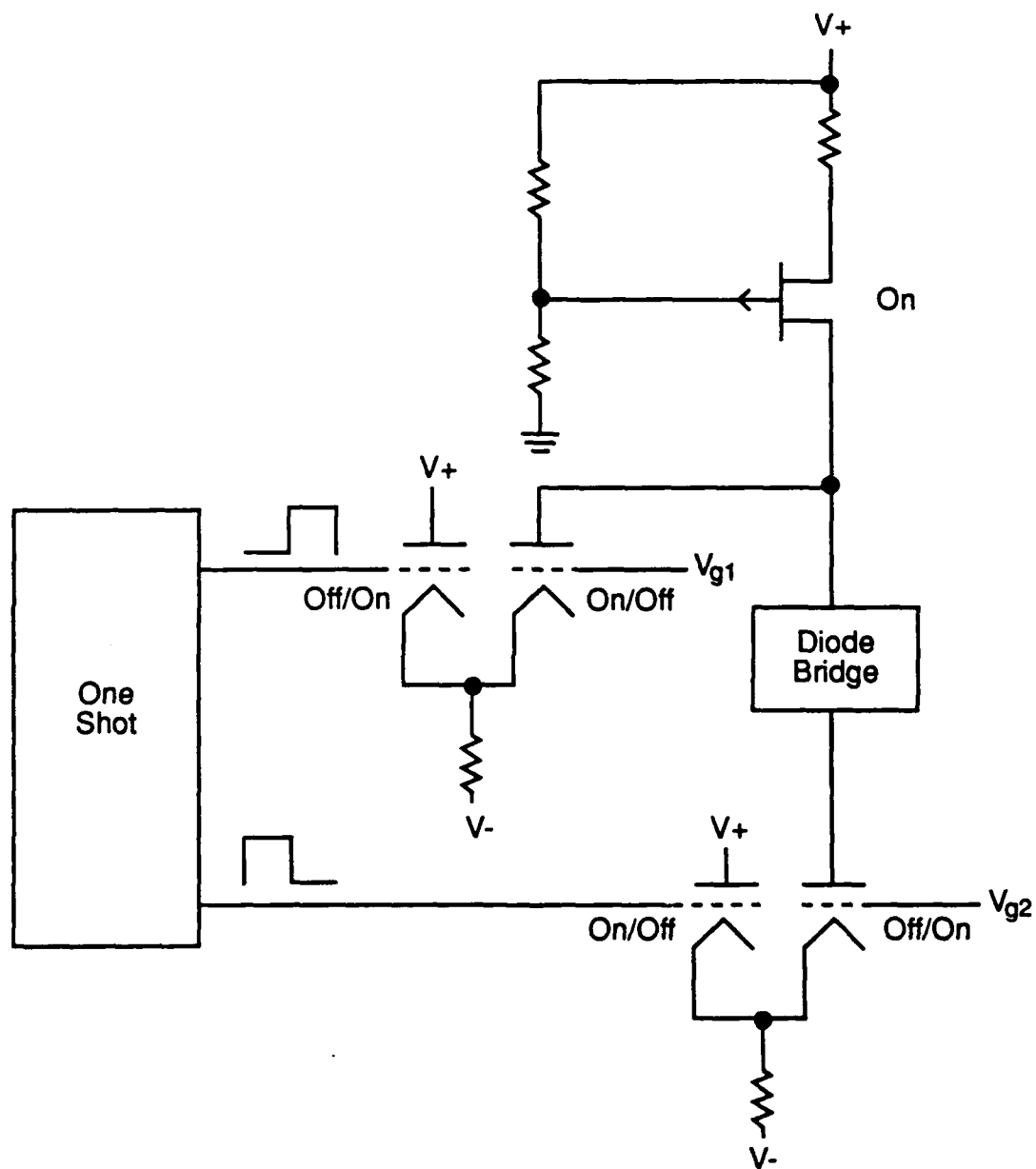
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Figure 14. Switch Control

5.4 CAPACITOR

The characteristics of the track-and-hold capacitor are also critical in achieving an accuracy of one part in 2^{16}. The factors which affect performance are the dissipation factor, dielectric absorption, and lead resistance and inductance. Figure 15 is the equivalent circuit of a capacitor.
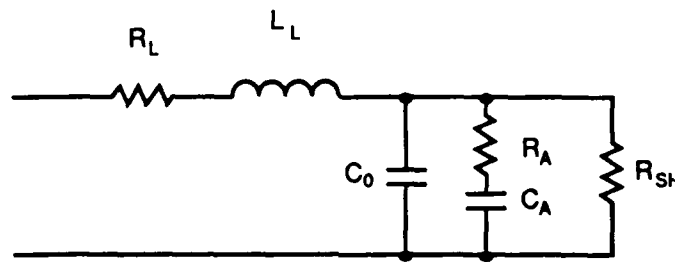

Figure 15. Equivalent Circuit of Capacitor

In this figure, R_L and L_L are the lead resistance and inductance, C_0 is the capacitance due to fast polarization of the dielectric, C_A is the "absorption" capacitance due to slow polarization of the dielectric, R_A is a fictitious resistance that slows down the charging and discharging of C_A, and R_{SH} is the shunting insulation resistance of the capacitor.

The dissipation factor of a capacitor is defined as

$$D = \frac{1}{\omega C_0 R_{SH}}$$

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For a T/H circuit, the dissipation factor is related to the droop in the held voltage. In order to achieve an accuracy of one part in 2^{16}, the voltage across the capacitor must not decrease to less than 99.9985% of its original value during the hold period of about 4 ns. In the T/H circuit the insulation resistance, R_{SH}, is connected in parallel with the input impedance, R_{IN}, of the second voltage follower. R_{SH} of the capacitor should be much larger than R_{IN} so that the droop is determined by C_0 and R_{IN}. The dissipation factor of a capacitor is lowest when the insulator is a vacuum or air or helium, and it is quite low for polystyrene and Teflon capacitors.

The effect of dielectric absorption is to produce a delayed response. If a capacitor is charged by a source for a sufficient length of time, both C_0 and C_A will charge to the source voltage. Likewise, if a capacitor is discharged for a long enough time, both C_0 and C_A will discharge completely. However, if the discharge time is short, C_0 will discharge completely but C_A will not. When the short circuit across the capacitor is removed, the charge remaining on C_A will be redistributed between C_A and C_0 so that a voltage will appear across the capacitor. In the T/H circuit, the voltage across C_A will lag the input signal, and the held voltage will differ from the input signal voltage at the time that the switch is opened. This voltage error can be minimized by using a dielectric with low absorption. Dielectrics such as a vacuum, air, or helium are best. Dielectrics of Teflon, polystyrene, ceramic, and polypropylene are good.

Lead resistance and inductance also cause delayed signals and errors in the held voltage. A microelectronic capacitor rather than a leaded component is recommended. However, silicon dioxide, which is the usual dielectric, has rather low insulation resistance. The possibility of using helium as a dielectric needs to be investigated from both an electrical and a mechanical fabrication point of view. The breakdown voltage of the dielectric must also be considered. Multiple-plate construction may be necessary to achieve sufficient capacitance.

Some of the inaccuracies caused by a non-ideal capacitor may be reduced by compensation circuits and a more complicated switching system if the voltage followers are op amps. However, these more complicated circuits may be difficult to implement and may cause problems of their own.

5.5 TRACK-AND-HOLD CIRCUIT DESIGN SUMMARY

The overall performance of the A/D converter is very dependent on the characteristics of the T/H circuit. Both speed and accuracy are important. Superconductor technology is not suitable for either the analog voltage followers or the switch. Three technologies have been considered for implementation of the voltage followers: FET transistors, bipolar transistors, and vacuum microelectronics. Efforts to develop FET and bipolar transistors for low temperature operation have been reasonably successful at temperatures down to 77 K, but problems exist at 4.2 K. Vacuum microelectronics has good potential, but fabrication problems exist. No technology presently exists for implementation of a voltage follower. We must wait for one of the following to occur:

1. Development of bipolar or FET transistors for operation at 4.2 K

2. Development of high-temperature superconductivity technology for operation with transistors at 77 K

3. Development of vacuum microelectronic devices with suitable characteristics

With regard to the switch and its control, only one approach has a chance of being fast enough. A laser is needed to generate trigger pulses with rise times in the tens of femtoseconds. These pulses then trigger a vacuum microelectronic one shot which drives a vacuum microelectronic diode bridge switch. Laser systems for generating fast pulses exist. Vacuum microelectronic technology is essential but has not developed very far. Although this circuit may be fast enough, its accuracy cannot be predicted. The capacitor in the T/H circuit is also critical, and it requires careful design too.

SECTION 6

DIGITAL-TO-ANALOG CONVERTER, SUMMER AND AMPLIFIER

This section discusses the other analog building blocks needed for the 16-bit A/D converter. These analog circuits offer a design challenge just as difficult as that of the T/H circuit. Some of the required components are quite similar to those needed in the T/H circuit.

6.1 ACCURACY

The purpose of the D/A converter in figure 9 is to convert the six-bit digital word representing the A/D converter output into an analog current. This current is subtracted from a current representing the sampled input signal, thereby producing a difference current for digitization of the lower-order bits by the next A/D converter. An error of one LSB in any of the individual A/D converter circuits is corrected in the next stage due to the one-bit overlap between stages. For a more detailed discussion of accuracy, refer to [39] and [40]. In order for the accuracy of the entire A/D converter to be one part in 2^{16}, the accuracy of the difference current must be one part in 2^{16} of the input full-scale signal.

6.2 D/A CONVERTER AND SUMMER

The operation of the D/A converter and summer is represented in figure 16 in which the summer (subtractor) is just a connection. The D/A converter current sources are generated using a common voltage and resistor values whose ratios are powers of two. Thus the accuracy of the D/A converter depends upon the accuracy of these resistor ratios. An important consideration is the resistor ratio accuracy achievable using monolithic fabrication techniques. Many 16-bit D/A converters exist, and there are even a few 18- and 20-bit converters. A number of special techniques are used to achieve these accuracies [41].
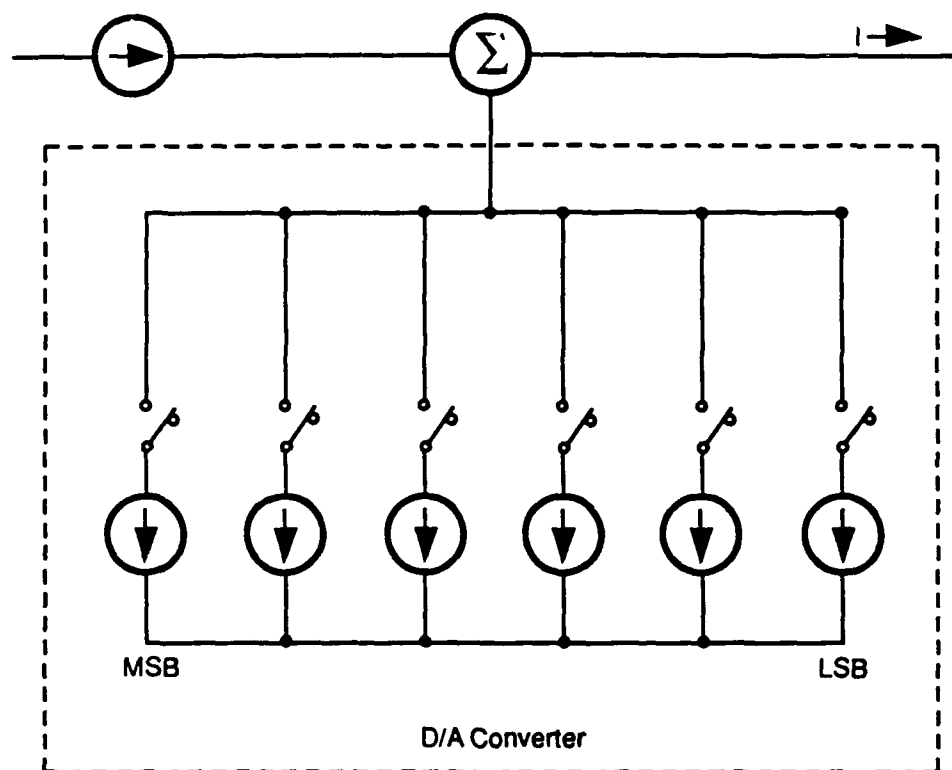
Figure 16. D/A Converter and Summer

FET switches are used in standard D/A converters. For our converter, a switching speed of about 1 ns is required. GaAs FETs may operate that fast assuming that TriQuint is realistic about their proposed 12- to 14-bit 1 GS/s D/A converter [42]. However, operation at 4.2 K is a problem as discussed in section 5.2.2. The other possibility is to use a vacuum microelectronic differential amplifier as a switched current source as in figure 14.

6.3 AMPLIFIER

The A/D converters can handle only a 6-bit range of inputs. Thus amplification of the difference current out of the summer is needed to provide the proper input to the A/D converter in the following stage. An inverting operational amplifier as shown in figure 17 would serve the purpose.
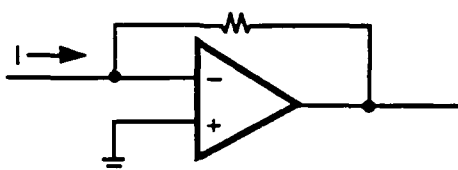

Figure 17. Inverting Operational Amplifier

The feedback resistor must be fabricated to the same tight tolerances required of the D/A converter resistors. This op amp must also be very fast. Like the D/A converter, it must settle within about 1 ns.

Designing this op amp will be very difficult. Neither FET nor bipolar IC technology is suitable because the transistors are too slow and because of the problems discussed in section 5.2.2. The only technology which may be fast enough is vacuum microelectronics. However, semiconductor op amp designs cannot be directly adapted to vacuum tube op amps because semiconductor op amps use both PNP and NPN devices, whereas vacuum tubes can only be NPN devices. The result is biasing problems in a DC-coupled vacuum tube op amp. The original vacuum tube op amps which were designed in the 1950s solved the biasing problem by using floating power supplies or neon bulbs. Obviously these are not suitable components for microelectronic fabrication. Semiconductor zener diodes and high-voltage vacuum microelectronic diodes are other possible devices for handling the bias problem.

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Another problem with these early op amps was DC drift. Balancing circuits or chopper-stabilizing circuits were needed. The latter was a separate chopper and AC amplifier that fed back a signal to compensate for DC drift. The specifications for an early op amp without chopper stabilization are listed in table 2. Note the low unity gain bandwidth. Chopper-stabilized circuits were much slower because the bandwidth was limited by the chopper rate.

Table 2. Specifications for G. A. Philbrick Model K2-W Op Amp

Output	$\pm$ 50 V @ 1 mA
Full Power Response	42 kHz
DC Gain	15,000
Unity Gain Bandwidth	700 kHz
24-Hour Drift	5 mV

In summary, the design of an accurate, high-speed op amp will be a major challenge. The only technology that holds any hope for an op amp response time of about 1 ns is vacuum microelectronics. However, DC biasing and perhaps drift problems will make the design of an op amp for this application very difficult. Because vacuum microelectronics is such a new field, device characteristics have not been measured, and the performance of a vacuum microelectronic op amp cannot be predicted.

SECTION 7

SUMMARY AND CONCLUSIONS

The objective of this project is to develop a 16-bit, 125 MS/s, superconducting A/D converter. An important application is in HF receivers with input signals in the 5 to 30 MHz band. A converter with these specifications is far beyond the state-of-the-art.

Superconductivity in metals at temperatures of about 4.2 K was discovered almost 80 years ago. In the 1950s, niobium compounds were found to be superconducting at critical temperatures of about 20 K. The recent discovery of high-temperature superconducting materials has stimulated renewed interest in superconductivity. However, there are problems in processing these new materials, and all existing superconducting circuits use low-temperature niobium compounds. Superconducting circuits are based upon Josephson junctions which are very fast, low-power devices with a zero-voltage state and a voltage state. A SQUID, containing one or more Josephson junctions in one or more loops, has the capability of flux quantization and flux-to-voltage conversion. SQUIDs have been used in developmental 6-bit A/D converters and in digital logic circuits. Josephson junctions are binary devices and are generally not suitable for analog applications. No superconducting transistors or DC amplifiers exist.

The proposed 16-bit subranging A/D converter (figure 9) uses superconducting circuits for the three 6-bit A/D converters and the digital logic. Other technologies are required for the track-and-hold circuit, the D/A converters, the summers and the amplifiers.

The specifications of 16 bits and a maximum input frequency of 30 MHz necessitate a T/H aperture jitter of less than 70 fs rms. This jitter requirement and the 16-bit accuracy specification make designing the analog circuits extremely difficult. Because no superconducting transistors exist, bipolar and FET transistors operating at low temperatures were investigated as substitutes. The betas of bipolar transistors fall off at low temperatures so that these devices are not useful. FET current-voltage characteristics exhibit hysteresis at low temperatures. In addition, although bipolar and FET transistors are fast enough for use

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as T/H voltage followers at 30 MHz, they are not fast enough for the other analog circuits that must operate at the 125 MS/s sampling rate or higher. Vacuum microelectronic technology with its high speed and temperature insensitivity is a possible solution, but fabrication problems exist. Even if vacuum microelectronic devices with suitable characteristics are developed, designing circuits such as op amps with them will require a major effort, especially when the required accuracy is one part in 2^{16}.

In order to meet the sampling jitter requirement, the sampling pulses must be generated by a laser system producing pulses whose rise times are tens of femtoseconds. Extremely fast pulses like this have been produced. These pulses could then be used to trigger a vacuum microelectronic one-shot circuit which controlled a vacuum microelectronic diode bridge switch in the T/H circuit if suitable vacuum microelectronic devices were developed. The switch control system should be fast enough, but the accuracy of the switch circuit is unpredictable.

In summary, development of a superconducting 16-bit A/D converter with a sampling rate of 125 MS/s and a 30 MHz maximum input frequency requires a multiple-discipline approach. In addition to superconducting 6-bit A/D converters and digital logic, a very fast laser system is needed. The most difficult problem will be developing the analog circuits required. Vacuum microelectronic technology has the potential for implementing these circuits. However, this is a new technology with fabrication problems. If these problems are solved and devices with suitable characteristics are developed, the design of this A/D converter may be possible. Vacuum microelectronic devices also might be used for the digital logic and for the 6-bit A/D converters. Then the superconducting circuits and dewar of liquid helium could be eliminated. The result would be a vacuum microelectronic 16-bit, 125 MS/s A/D converter with a laser timing system.

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Technical Report 9

FEASIBILITY STUDY OF A SUPERCONDUCTING SIGMA-DELTA ANALOG-TO-DIGITAL CONVERTER

by

Margaret A. Poole

ABSTRACT

The development of high-speed, high-resolution analog-to-digital (A/D) converters is needed for many applications. Experimental superconducting A/D converters are fast, but have limited resolution. This working paper discusses design considerations for a superconducting sigma-delta ($\Sigma\Delta$) A/D converter with a 16-bit output at 125 megasamples per second. A converter with these specifications is suitable for high-resolution HF receiver applications.

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SECTION 1

INTRODUCTION

Many applications require analog-to-digital (A/D) converters with higher precision and higher data rates than can be obtained from existing devices. Recent work on superconducting A/D converters has demonstrated their high speed but rather limited resolution. The objective of Project 91080 is to develop a 16-bit A/D converter with a sampling rate of 125 megasamples per second (MS/s). The state of the art for semiconductor A/D converters is shown in figure 1 and table 1. Although a few converters with less than 8 bits and more than 16 bits exist, almost all development efforts are directed toward 8- to 16-bit converters. The trade-off between resolution (in bits) and conversion rate is clearly shown in the figure. Superconducting A/D converter development efforts have produced experimental devices with 6-bit resolution and conversion rates of a few gigahertz [1,2]. Recent development efforts have concentrated on higher resolution converters such as the Westinghouse 12-bit 5 MS/s counting converter [3]. Thus a superconducting 16-bit converter with a 125 MS/s sampling rate would be considerably beyond the state of the art for both semiconductor and superconductor converters. An important application for such a converter would be in HF receivers with input frequencies from 5 to 30 MHz. A converter with a conversion rate of 125 MS/s could be used to sample the HF signal directly. Thus the input filter bank and the up and down converters typically used in HF receivers could be eliminated.

This is the second of two working papers evaluating alternative architectures for a superconducting A/D converter. A subranging converter was discussed in WP-28903. This paper investigates sigma-delta ($\Sigma\Delta$) converter architectures. Because $\Sigma\Delta$ converters are relatively new, no books on the subject have been written, and $\Sigma\Delta$ converters are not well understood. This report provides a comprehensive review of $\Sigma\Delta$ converters including basic principles, architectures, and performance in section 2, thereby satisfying one of the Project 7920 objectives. Section 3 provides some background on superconductivity. Next the implementation of a superconducting $\Sigma\Delta$ converter is discussed in section 4. The results of the study are summarized, and future plans are discussed in section 5.

Figure 1. State-of-the-Art A/D Converters

Table 1. A/D Converters

Letter	Manufacturer	Part No.	No. of Bits	Conversion Rate	Architecture	Status
A	Analogic	AM41216	16	500 kS/s	Subranging	Production
B	Westinghouse	WEC1405B	14	5 MS/s	Subranging	Limited Prod.
C	Analog Devices	AD9014	14	10 MS/s	Subranging	Prototypes
D1	Analog Devices	AD900	12	10 MS/s	Subranging	Production
D2	Burr Brown	ADC60	12	10 MS/s	Subranging	Production
E	Analog Devices	AD9060	10	60 MS/s	Flash	Prototypes
F	Tektronix	TKAD10C	8	500 MS/s	Dual Flash	Production

SECTION 2

SIGMA-DELTA A/D CONVERTERS

A sigma-delta ($\Sigma\Delta$) A/D converter (also sometimes called delta-sigma) consists of a high-speed low-resolution quantizer, commonly referred to as a $\Sigma\Delta$ modulator, followed by a digital filter as shown below.
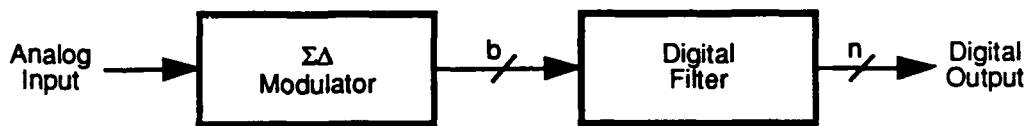
Figure 2. Sigma-Delta A/D Converter

The trade-off between sampling rate and resolution puts $\Sigma\Delta$ modulators far down and to the right of the converters shown in figure 1. The number of bits, b, out of the $\Sigma\Delta$ modulator is small and frequently is only one. The digital filter produces n-bit output digital words at a rate much lower than the modulator sampling rate so that the overall $\Sigma\Delta$ converter characteristics are closer to those shown in figure 1.

An important characteristic of $\Sigma\Delta$ modulators is quantization noise shaping. Because the number of modulator bits is small, the quantization noise power at the modulator output is high. However, most of this noise lies above the signal band provided that the oversampling ratio, the ratio of the modulator sampling frequency to twice the signal bandwidth, is large. Subsequent digital filtering attenuates this out-of-band noise. The resulting signal-to-noise ratio within the signal bandwidth can be high.

Delta modulators and sigma-delta modulators are different variations of the basic linear feedback modulator shown below in which the modulator is modeled as a sampled data system.
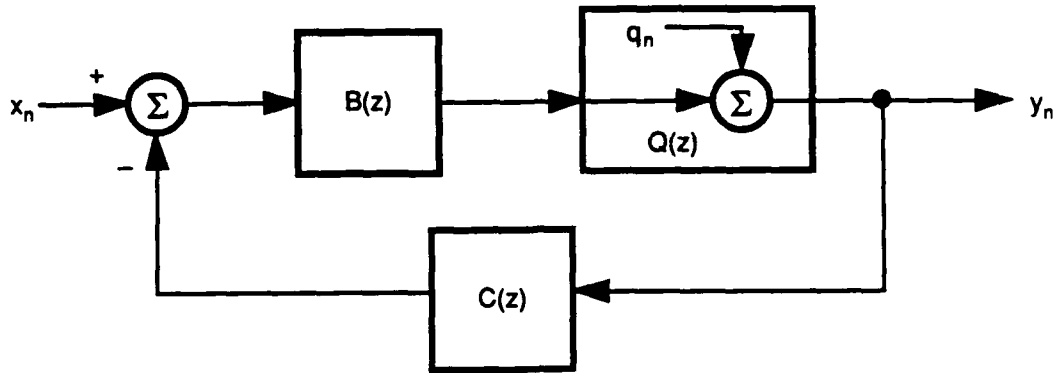
Figure 3. Basic Modulator Circuit

B and C are filters. Quantization noise is added by the quantizer Q. The input and output of the circuit are related by

$$Y(z) = \frac{B(z)X(z) + Q(z)}{1 + B(z)C(z)} \qquad (1)$$

A delta-modulator is a predictive coder in which B(z) equals one and C(z) predicts the next value of x_n based on past values of y_n. Predictive delta-modulators are used for speech coding in differential pulse code modulators (DPCM) and continuously variable slope delta (CVSD) modulators. $\Sigma\Delta$ modulators are used in PCM encoders. In a $\Sigma\Delta$ modulator C(z) equals one, and B(z) is an integrator with a transfer function of

$$B(z) = \frac{z^{-1}}{1 - z^{-1}} \qquad (2)$$

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Substituting (2) in (1) yields

$$Y(z) = z^{-1}X(z) + (1 - z^{-1})Q(z) \qquad (3)$$

Thus the modulator output is the delayed input plus shaped quantization noise. Furthermore, the noise shaping function has a high-pass response so that the noise is pushed out of the baseband. As a consequence, the modulator can have a high signal-to-noise ratio (SNR) within the baseband. Later analysis will show that for a given signal bandwidth, the SNR of this signal loop $\Sigma\Delta$ modulator increases 9 dB for each doubling of the sampling rate and modulators of order M have SNR increases of (6M + 3) dB per octave. In contrast, in conventional types of A/D converters without noise shaping, the SNR increases only 3 dB for each doubling of the sampling frequency.

The advantages of $\Sigma\Delta$ modulators compared to other types of A/D converters are as follows:

1. The complexity of the analog circuitry is greatly reduced by shifting the computational burden to the digital filter.

2. High-precision or matched analog components are not required.

3. The requirements of the anti-aliasing filter preceding the modulator are greatly simplified because of the high sampling rate.

4. No sample-and-hold (or track-and-hold) circuit preceding the modulator is required.

5. If a one-bit quantizer is used, the modulator is inherently linear and theoretically produces no harmonic distortion or intermodulation distortion. Errors in the quantizer levels produce gain or DC offset errors, but not nonlinearities.

The two main disadvantages of ΣΔ modulators are the need for high-speed circuits and the complexity of the digital filters.

The sections which follow discuss several types of ΣΔ modulators and digital filtering. For more information on ΣΔ converters, an extensive bibliography can be found in [4].

2.1 SIGMA-DELTA MODULATORS

The two basic types of ΣΔ modulators are referred to as classical and cascade. Both types of modulators start with the basic single-loop ΣΔ modulator shown in figure 3 and with the input-output relationship in equation (3). This basic ΣΔ modulator is described in more detail in the next section. Then the classical and cascade architectures, their performance, and experimental results are discussed.

2.1.1 Basic ΣΔ Modulator

The basic single-loop ΣΔ modulator is shown in figure 4..

Figure 4. Basic ΣΔ Modulator

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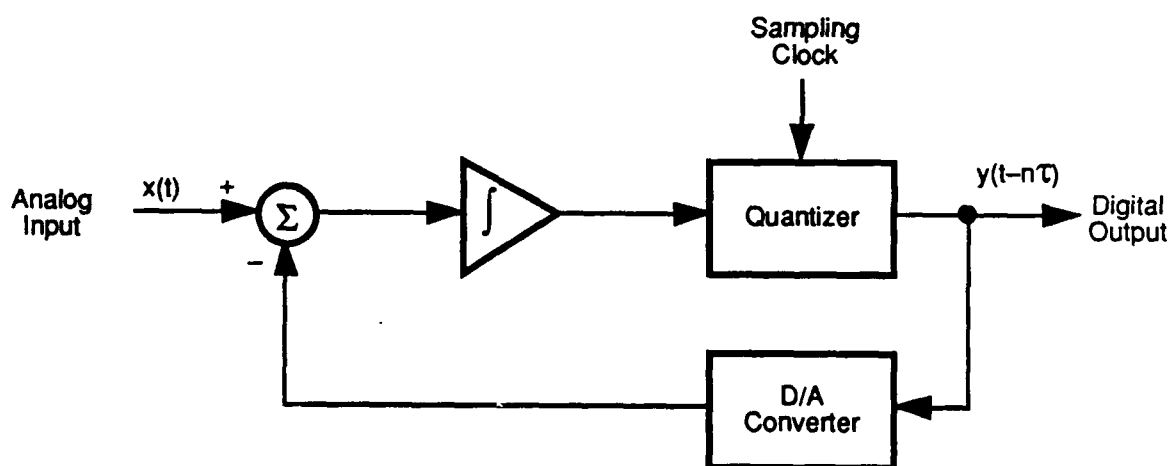
The quantizer produces digital samples at the sampling clock frequency, $f_s = 1/\tau$. Usually a one-bit quantizer is used, but some modulators have multi-bit quantizers. The integrator produces the noise shaping. The only way to accurately determine the operation of this non-linear circuit is by simulation for successive input samples. The simulation must be repeated for each different input signal. Another drawback is that simulation provides only limited insight into basic circuit characteristics. The standard analytical approach is based on a linear model with additive quantization noise. Analysis of this mixed analog and digital circuit first requires that the schematic be redrawn in a sampled data representation in which all signals are sampled signals as shown in figure 5.
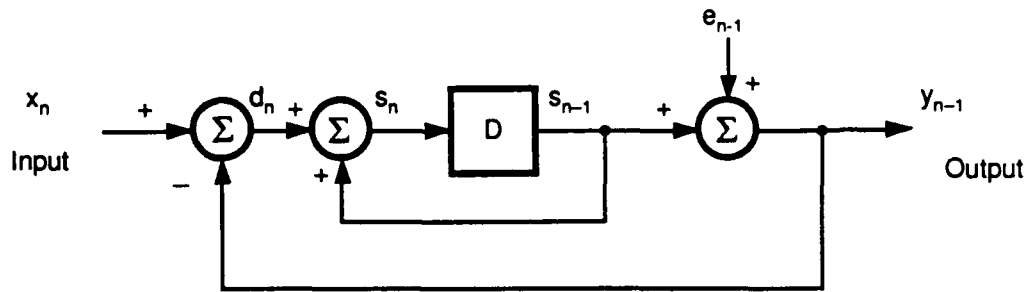
Figure 5. Sampled Data Representation of Basic $\Sigma\Delta$ Modulator

The integrator is represented as a delay of one sampling period and a summer. The quantizer adds a quantization error signal, e. The accuracy of the analysis depends upon assumptions about this quantization error.

2.1.1.1 Performance Analysis

The equations for the basic $\Sigma\Delta$ modulator in figure 5 are as follows:

$$d_n = x_n - y_{n-1} \tag{4}$$

$$s_n = d_n + s_{n-1} \tag{5}$$

$$y_{n-1} = e_{n-1} + s_{n-1} \tag{6}$$

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Combining these equations yields

$$y_n = x_n + e_n - e_{n-1} \tag{7}$$

Taking z transforms

$$Y(z) = X(z) + (1 - z^{-1}) E(z) \tag{8}$$

Hence the modulator output is the sum of the input and filtered quantization noise. Replacing z with $e^{j\omega\tau}$, the power spectral density of the modulator output noise is

$$S_N(\omega) = \left|\left(1 - e^{-j\omega\tau}\right)E(\omega)\right|^2 \tag{9}$$

$$S_N(\omega) = \left|e^{-j\omega\tau/2}\left(e^{j\omega\tau/2} - e^{-j\omega\tau/2}\right)\right|^2 |E(\omega)|^2$$

$$S_N(\omega) = \left|e^{-j\omega\tau/2}\right|^2 \left|2j \sin \frac{\omega\tau}{2}\right|^2 |E(\omega)|^2$$

$$S_N(\omega) = \left(4 \sin^2 \frac{\omega\tau}{2}\right)|E(\omega)|^2$$

$$S_N(\omega) = 2(1 - \cos \omega\tau)|E(\omega)|^2 \tag{10}$$

In order to evaluate the $\Sigma\Delta$ modulator output noise spectral density, the quantizer noise spectral density must be known. In conventional multi-bit A/D converters, the quantization noise is closely approximated as being white and having a power level of $\Delta^2/12$ which is uniformly distributed between $\pm f_s/2$ where Δ is the quantizer step size and f_s is the sampling frequency. In experimental tests of $\Sigma\Delta$ modulators, high-level spurious output frequencies have been observed for DC inputs and sinusoidal inputs [5-8]. A mathematically rigorous evaluation of the quantization noise is extremely difficult. However, progress in analyzing the noise has been made recently [7-10]. As an alternative, dithering the input can smooth

the noise spectrum but does not make it white [11]. Nevertheless, the standard A/D converter noise assumptions are close approximations for many signals, and will be used here. Then

$$|E(\omega)|^2 = \frac{\Delta^2}{12}\frac{1}{f_s} = \frac{\Delta^2\tau}{12} \qquad (11)$$

$$S_N(\omega) = \frac{\Delta^2\tau}{6}(1-\cos\omega\tau) = \frac{\Delta^2}{6f_s}\left[1-\cos\left(\frac{2\pi f}{f_s}\right)\right] \qquad (12)$$

The noise power in the band from $-B \le f \le B$ is equal to

$$\sigma_B^2 = 2\int_0^B S_N(f)df \qquad (13)$$

$$\sigma_B^2 = \frac{\Delta^2\tau}{3}\int_0^B (1-\cos 2\pi f\tau)df$$

$$\sigma_B^2 = \frac{\Delta^2\tau}{3}\left[B - \frac{\sin 2\pi B\tau}{2\pi\tau}\right]$$

$$\sigma_B^2 = \frac{\Delta^2}{6\pi}[2\pi B\tau - \sin 2\pi B\tau] \qquad (14)$$

In a highly oversampled converter, $B/f_s = B\tau <<1$, and the approximation $\sin x \approx x - x^3/3!$ can be used.

$$\sigma_B^2 \approx \frac{\Delta^2}{6\pi}\left[2\pi B\tau - 2\pi B\tau + \frac{(2\pi B\tau)^3}{6}\right]$$

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$$\sigma_B^2 \approx \frac{2}{9}\Delta^2\pi^2(B\tau)^3 = \frac{\Delta^2\pi^2}{36}\left(\frac{2B}{f_s}\right)^3 \tag{15}$$

The one-bit quantizer step size, Δ, must be large enough to allow the $\Sigma\Delta$ modulator output to track the input as indicated in equation (7). Thus the peak value of a sine wave input must not exceed $\Delta/2$. The power of the largest allowable sine wave input is

$$P_s = \left(\frac{\Delta}{2}\frac{\sqrt{2}}{2}\right)^2 = \frac{\Delta^2}{8} \tag{16}$$

The maximum signal-to-noise ratio within the band, B, for a sine wave input is equal to

$$SNR_B = \frac{P_s}{\sigma_B^2} \approx \frac{9}{2\pi^2}\left(\frac{f_s}{2B}\right)^3 \tag{17}$$

The signal-to-noise ratio in dB is

$$SNR_{B(dB)} \approx 10\ log\left(\frac{9}{2\pi^2}\right) + 30\ log\left(\frac{f_s}{2B}\right) \tag{18}$$

Let

$$L = log_2\left(\frac{f_s}{2B}\right) = 3.322\ log_{10}\left(\frac{f_s}{2B}\right) \tag{19}$$

Then

$$SNR_{B(dB)} \approx 9L - 3.41 \tag{20}$$

The ratio $f_s/2B$ is commonly referred to as the oversampling ratio R.* Equation (20) shows that the signal-to-noise ratio increases 9 dB for each doubling of the oversampling ratio for large R. Of this 9 dB, 3 dB is due to doubling the noise bandwidth for each

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* A few authors define oversampling ratio as f_s/B.

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doubling of R and is the same SNR improvement obtained from conventional A/D converters. The other 6 dB SNR improvement is due to noise shaping. The noise power spectral density as derived in equation (12) is plotted in figure 6 for fixed f_s and total quantization noise power. The noise spectrum is flat for conventional A/D converters, but has a high pass response for $\Sigma\Delta$ converters. For the basic $\Sigma\Delta$ modulator, the noise shaping is 6 dB per octave. Higher-order $\Sigma\Delta$ modulators provide greater noise shaping. Because of the quantization noise assumptions, the actual noise spectrum may be slightly different.

The signal-to-noise ratio within the baseband is plotted in figure 7 as a function of R. The slope of the curve for the basic $\Sigma\Delta$ modulator is 9 dB per octave which compares favorably with the 3 dB per octave slope for conventional A/D converters. However, in order for the basic $\Sigma\Delta$ modulator to achieve a signal-to-noise ratio of more than 80 dB, a very high oversampling ratio is needed. High-order $\Sigma\Delta$ modulators provide better performance and will be discussed in sections 2.1.2 and 2.1.3.

The theoretical signal-to-noise ratio was derived for a maximum-amplitude sine wave input using the simplifying assumption made in equation (11). Another way to determine the SNR is to consider the fact that the modular output is always $\pm \Delta/2$ and thus has a power level of $\Delta^2/4$. This modulator output power is equal to the sum of the output signal power plus the quantization noise power.

$$P_o = P_s + P_N = \frac{\Delta^2}{4} \tag{21}$$

For the maximum sine wave input

$$P_N = \frac{\Delta^2}{4} - \frac{\Delta^2}{8} = \frac{\Delta^2}{8} \tag{22}$$

Thus when the total quantization noise across the frequency band from $-f_s/2$ to $f_s/2$ is considered, the signal-to-noise ratio is 0 dB and is independent of the sampling rate. The main difference between this result and the previously derived expression for SNR_B is due to the modulator's effect of moving most of the noise out of the baseband. If $B = f_s/2$, $R = 1$ and
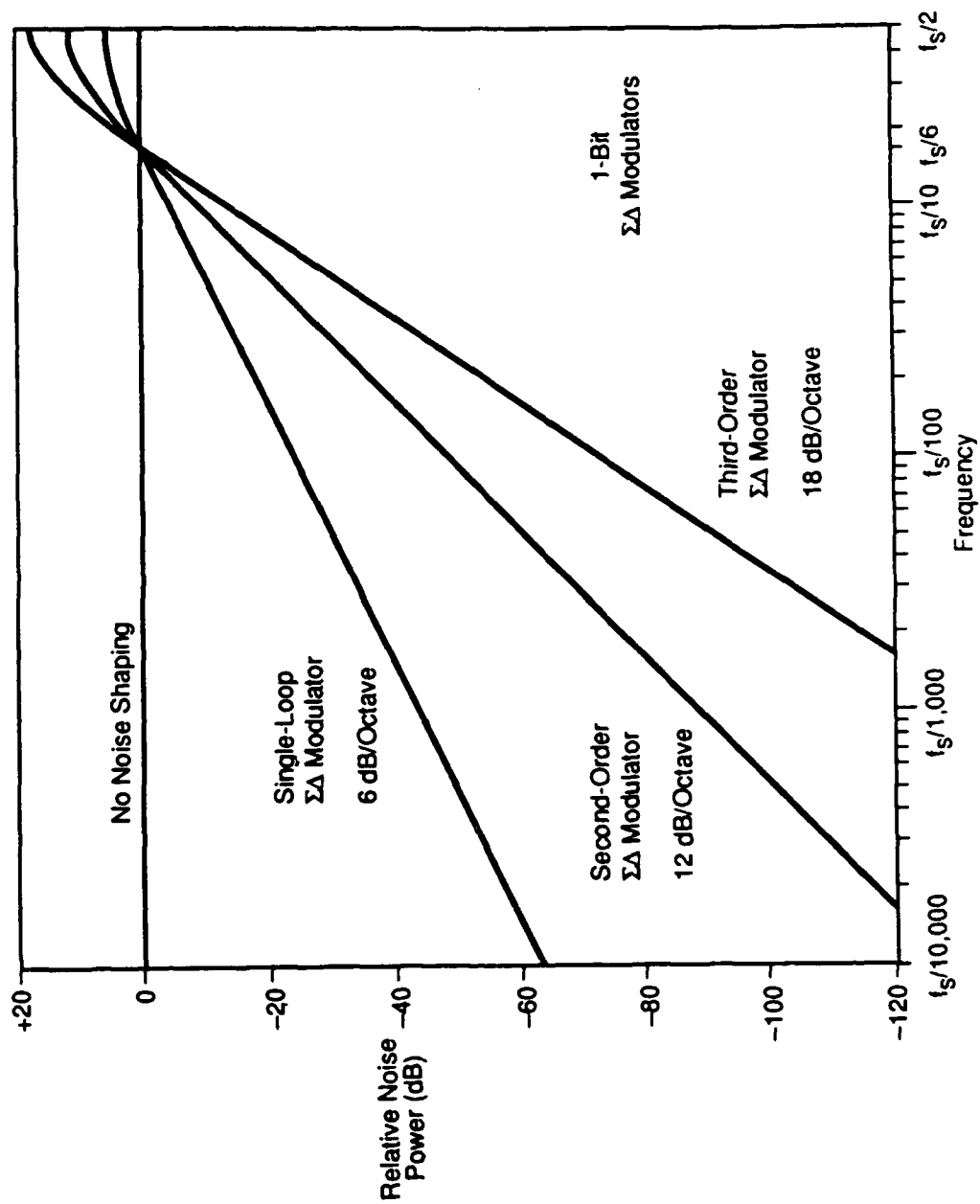
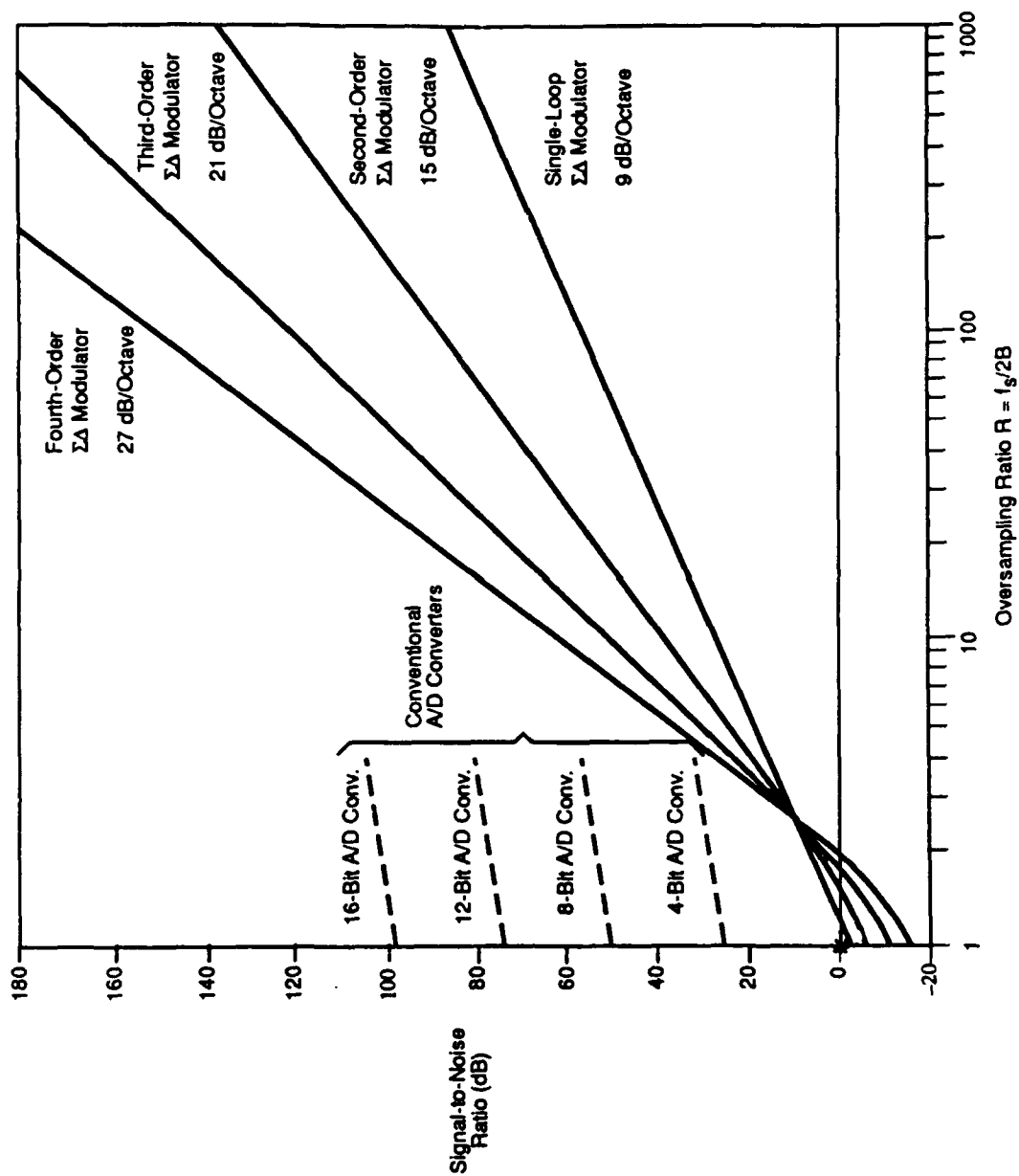Figure 6. $\Sigma\Delta$ Modulator Noise Power Spectral Density

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Figure 7. ΣΔ Modulator Signal-to-Noise Ratio

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SNR_B should equal 0 dB. This point is indicated by an asterisk in figure 7. The fact that the basic $\Sigma\Delta$ modulator curve does not pass through this point indicates that the quantization noise assumptions were not quite right.

Consider next the signal-to-noise ratio for smaller amplitude inputs. The quantization noise power in equation (15) appears to be independent of the signal. If so, the SNR should decrease at the same rate that the signal decreases. However, according to equation (21) when the signal power decreases, the quantization noise power must increase. Hence the signal-to-noise ratio must decrease faster than the signal decreases. This result also points out problems with the quantization noise assumptions.

Because the basic $\Sigma\Delta$ modulator output is always $\pm \Delta/2$, the signal-to-noise ratio for low level input signals is poor. One way to increase the SNR is to use a multi-bit quantizer so that the quantization noise is reduced. For b bits, the number of quantizer output levels is 2^b. In order to prevent modulator overloading (to be discussed later), the input signal must not exceed the quantizer output levels. Therefore, the allowable signal range is $(2^b -1)\Delta$, and the peak signal amplitude is $(2^b - 1) \Delta/2$. If the baseband quantization noise power is assumed to be constant regardless of the signal amplitude and to depend only on Δ as equation (15) implies, the signal-to-noise ratio improvement for a full-scale sine wave as the number of bits increases is shown in table 2. These impressive performance improvements are partially offset by losses due to component inaccuracies as will be discussed in the next subsection.

Table 2. SNR Improvement with Multi-Bit Quantizer

Number of Bits	Number of Quantization Levels	Allowable Signal Range	Peak Signal Level	SNR Improvement
1	2	Δ	$\Delta/2$	0 dB
2	4	3Δ	$3\Delta/2$	9.5 dB
3	8	7Δ	$7\Delta/2$	16.9 dB
4	16	15Δ	$15\Delta/2$	23.5 dB
5	32	31Δ	$31\Delta/2$	29.8 dB
6	64	63Δ	$63\Delta/2$	36.0 dB

2.1.1.2 Causes of Performance Degradation

The major difference between the actual output of a single-loop $\Sigma\Delta$ modulator and the output as predicted in the previous section is the fact that the quantization noise is neither white nor continuous [5-8]. Large discrete spurious signals are produced at the modulator output for DC inputs and for sinusoidal inputs. Some of these spurious signals lie within the baseband and cannot be filtered out by the digital filter. These spurious signals arise from repetitive modulator digital output sequences which can be produced in tracking a DC input or a repetitive input of any form. The common method for handling this problem is to add dither noise to the input. This dither noise smooths the spectrum but does not make the quantization noise white [11]. The dither signal breaks up the repetitive modulator output sequences and reduces the power in the spurious outputs. Several methods are used to eliminate the dither noise on the output. If the dither noise lies in the same frequency band as the input signal, a digitized representation of the dither noise can be subtracted from the modulator output. Alternatively, if the dither noise spectrum lies above the signal band, subsequent digital filtering can attenuate it sufficiently. The frequency of the dither signal can also be selected to lie in a stopband of the digital filter. Because of the severity of the spurious noise problem in signal-loop $\Sigma\Delta$ modulators, dither noise is always added in actual circuit implementations.

Simulations of single-loop $\Sigma\Delta$ modulators have shown that the integrator is the most critical circuit in the modulator. Degradation of the ideal integrator transfer function occurs if there is leakage causing a droop in the voltage held by the integrating capacitor. The effect on modulator performance can be seen by putting an amplifier with a gain of $(1-\delta)$ immediately after the second summer in figure 5. Then the expression for s_n in equation (5) is multiplied by $(1-\delta)$ and equation (7) becomes

$$y_n = (1 - \delta)\, x_n + e_n - e_{n-1} + \delta\, e_{n-1} \tag{23}$$

The term δe_{n-1} represents unshaped noise which appears at the output as though it were added directly to the input. Thus leakage can limit the achievable SNR of the modulator.

The integrator is usually implemented as an operational amplifier (op amp) with a feedback capacitor and a switched-capacitor input circuit which acts as a resistor. Other switches, which are controlled by the quantizer output, provide an additional positive or negative reference input to the integrator. The integrator is usually fabricated using MOS technology. One of the requirements of the op amp is high open-loop gain to minimize leakage. The gain needed is approximately equal to the oversampling ratio [12]. Because of the high sampling rate, the op amp must have a high frequency response, a fast slew rate, and a fast settling time. The op amp must also have sufficient output signal swing and enough output drive capability to charge the capacitor quickly. The accuracy of the capacitor ratios is not critical. However, changes of capacitance with voltage do degrade performance [12]. The time constants of the switches are important, too.

A one-bit quantizer (a comparator) is inherently linear and does not produce harmonics or intermodulation distortion. For a one-bit quantizer, the gain of the integrator does not matter because the comparator response depends only on the signal polarity. If the threshold of the comparator is not exactly zero, the modulator output will have a DC offset. This is not usually a problem, but the DC offset can be eliminated by filtering if necessary. The comparator delay is not critical. However, the digital output rise and fall times either must be equal or must be very fast [13]. A modulator with a multi-bit quantizer can cause distortion. The linearity of the quantizer itself has little effect, but the overall modulator linearity is determined almost solely by the linearity of the D/A converter. For this reason, multi-bit quantizers are not used often.

Noise in the analog circuits can also degrade circuit performance. The sources of noise include power supply noise, digital clock noise, thermal noise, amplifier 1/f noise, and switch noise. The effect of noise on modulator performance depends upon the noise power, the frequency of the noise (in or out of the signal band), and the point in the modulator feedback circuit at which the noise is introduced. The op amp and the switches are the major noise contributors. Noise in the quantizer is not important because it adds very little to the quantization noise. In order to minimize the effect of noise, the integrator is usually implemented as a differential pair of circuits. This configuration also minimizes any even harmonics.

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Another potential contributor to modulator noise is sampling clock jitter. For a given sampling error, Δt, the jitter noise is largest when the input signal is at the upper edge of the frequency band, B, because the slope of the signal is highest at this frequency. The maximum power in the jitter noise has been shown to be [14,15]

$$\sigma_J^2 = \frac{A^2}{2}(2\pi B \Delta t)^2 \qquad (24)$$

where $A = \Delta/2$ is the peak signal amplitude for a one-bit quantizer. Let $k = \Delta t/\tau = \Delta t f_s$.

Then

$$\sigma_J^2 = \frac{\Delta^2 \pi^2 k^2}{8}\left(\frac{2B}{f_s}\right)^2 \qquad (25)$$

In order for the jitter noise to be less than the quantization noise

$$\frac{\Delta^2 \pi^2 k^2}{8}\left(\frac{2B}{f_s}\right)^2 < \frac{\Delta^2}{12}$$

$$k^2 < \frac{2}{3\pi^2}\left(\frac{f_s}{2B}\right)^2$$

$$k < 0.26\left(\frac{f_s}{2B}\right) \qquad (26)$$

Even with no oversampling ($f_s/2B = 1$), the allowable jitter is 0.26τ. With reasonable oversampling ratios, the allowable jitter is much greater than the sampling period. Thus sampling clock jitter is not a problem.

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Another problem that does not exist in a single-loop modulator is overload. If the input signal does not exceed the quantizer output levels of $\pm \Delta/2$, the signals at all points within the modulator are bounded, and no nonlinearities are introduced by overdriving the internal circuits. The maximum signal level at any point is $\pm \Delta$.

2.1.2 Multi-Loop Classical $\Sigma\Delta$ Modulators

In order to achieve high signal-to-noise ratios with the basic single-loop modulator, the oversampling ratio must be very high. As a result, component speed frequently limits performance. One way to obtain more effective noise shaping is to use a multi-loop $\Sigma\Delta$ modulator which provides a signal-to-noise improvement of more than 9 dB for each doubling of the sampling frequency. Double-loop modulators provide a 15 dB per octave increase in SNR. Modulators with more than two loops can become unstable as the input signal level increases. Even double-loop modulators must be designed carefully to assure stability. The following subsections discuss theoretical performance, sources of performance degradation, and experimental results for multi-loop $\Sigma\Delta$ modulators.

2.1.2.1 Performance Analysis of Double-Loop Modulator

Multi-loop $\Sigma\Delta$ modulators are formed by the addition of integrator loops ahead of the basic $\Sigma\Delta$ modulator loop. A double-loop modulator is shown in figure 8. The two integrators make this a second-order circuit. Figure 9 shows the sampled data representation of the circuit which is used for analysis. The equations for the circuit are

$$v_n = x_n - y_{n-1} \tag{27}$$

$$w_n = v_n + w_{n-1} \tag{28}$$

$$d_n = w_n - y_{n-1} \tag{29}$$

$$s_n = d_n + s_{n-1} \tag{30}$$

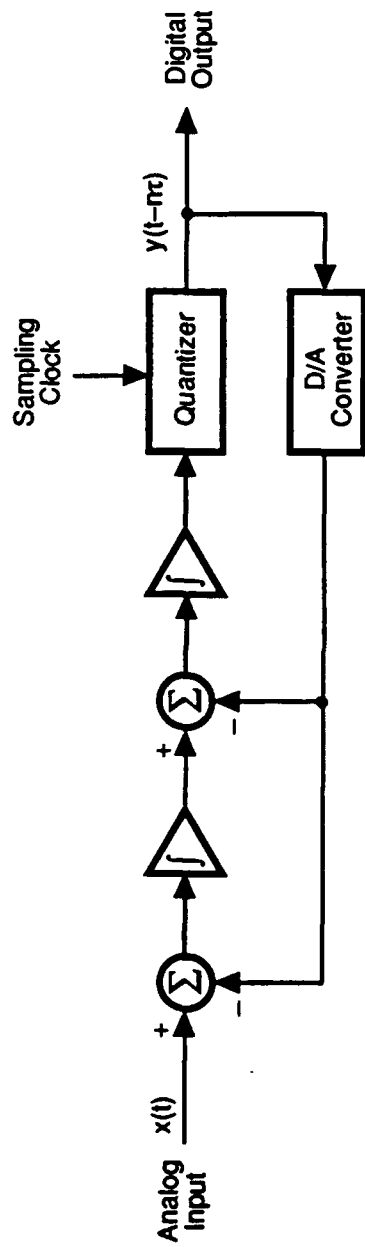$$y_{n-1} = s_{n-1} + e_{n-1} \tag{31}$$

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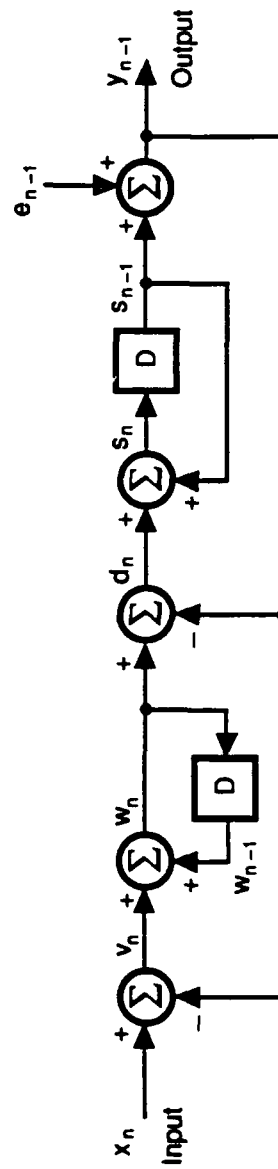Figure 8. Double-Loop Classical $\Sigma\Delta$ Modulator

Figure 9. Sampled Data Representation of Double-Loop $\Sigma\Delta$ Modulator

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Combining equations yields

$$y_n = x_n + e_n - 2e_{n-1} + e_{n-2} \tag{32}$$

Taking z transforms

$$Y(z) = X(z) + (1 - z^{-1})^2 E(z) \tag{33}$$

Comparison of equations (33) and (8) shows the increased noise shaping provided by the double-loop modulator. The power spectral density of the modulator output noise is

$$S_N(\omega) = \left| \left(1 - e^{-j\omega\tau} \right)^2 E(\omega) \right|^2 \tag{34}$$

$$S_N(\omega) = \left| \left[e^{-j\omega\tau/2} \left(e^{j\omega\tau/2} - e^{-j\omega\tau/2} \right) \right]^2 \right|^2 |E(\omega)|^2$$

$$S_N(\omega) = \left| e^{-j\omega\tau} \right|^2 \left| \left(2j\sin\frac{\omega\tau}{2} \right)^2 \right|^2 |E(\omega)|^2$$

$$S_N(\omega) = \left(16\sin^4\frac{\omega\tau}{2} \right) |E(\omega)|^2$$

$$S_N(\omega) = 4(1 - \cos\omega\tau)^2 |E(\omega)|^2 \tag{35}$$

The quantizer noise will be assumed to be white and to have a power level of $\Delta^2/12$ which is uniformly distributed between $\pm f_s/2$. This is the same assumption that was made for the basic single-loop modulator. This assumption comes closer to being true for the double-loop modulator. Then

$$|E(\omega)|^2 = \frac{\Delta^2}{12}\frac{1}{f_s} = \frac{\Delta^2\tau}{12} \tag{36}$$

$$S_N(\omega) = \frac{\Delta^2\tau}{3}(1-\cos\omega\tau)^2 = \frac{\Delta^2}{3f_s}\left[1-\cos\frac{2\pi f}{f_s}\right]^2 \tag{37}$$

The noise power in the band from $-B \le f \le B$ is equal to

$$\sigma_B^2 = 2\int_0^B S_N(f)df \tag{38}$$

$$\sigma_B^2 = \frac{2\Delta^2\tau}{3}\int_0^B\left(1-2\cos 2\pi f\tau + \cos^2 2\pi f\tau\right)df$$

$$\sigma_B^2 = \frac{2\Delta^2\tau}{3}\int_0^B(1-2\cos 2\pi f\tau + 1/2 + 1/2\cos 4\pi f\tau)df$$

$$\sigma_B^2 = \frac{2\Delta^2\tau}{3}\left[\frac{3B}{2}-\frac{\sin 2\pi B\tau}{\pi\tau}+\frac{\sin 4\pi B\tau}{8\pi\tau}\right]$$

$$\sigma_B^2 = \frac{\Delta^2}{12\pi}[12\pi B\tau - 8\sin 2\pi B\tau + \sin 4\pi B\tau] \tag{39}$$

If the oversampling ratio, $R = f_s/2B = 1/2B\tau$, is high, the approximation
$\sin x \approx x - x^3/3! + x^5/5!$ can be used.

$$\sigma_B^2 \approx \frac{\Delta^2}{12\pi}\left[12\pi B\tau - 16\pi B\tau + 8\frac{(2\pi B\tau)^3}{6} - 8\frac{(2\pi B\tau)^5}{120} + 4\pi B\tau - \frac{(4\pi B\tau)^3}{6} + \frac{(4\pi B\tau)^5}{120}\right]$$

$$\sigma_B^2 \approx \frac{8}{15}\Delta^2\pi^4(B\tau)^5 = \frac{\Delta^2\pi^4}{60}\left(\frac{2B}{f_s}\right)^5 \tag{40}$$

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In order for the modulator output to track the input, the peak value of the input is $\Delta/2$ for a one-bit quantizer and the signal power is

$$P_s = \frac{\Delta^2}{8} \tag{41}$$

Then the maximum signal-to-noise ratio within the band for a sine wave input is equal to

$$SNR_B = \frac{P_s}{\sigma_B^2} \approx \frac{15}{2\pi^4}\left(\frac{f_s}{2B}\right)^5 \tag{42}$$

The signal-to-noise ratio in dB is

$$SNR_{B(dB)} \approx 10\log\left(\frac{15}{2\pi^4}\right) + 50\log\left(\frac{f_s}{2B}\right) \tag{43}$$

Let

$$L = \log_2\left(\frac{f_s}{2B}\right) = 3.322\log_{10}\left(\frac{f_s}{2B}\right) \tag{44}$$

Then

$$SNR_{B(dB)} \approx 15L - 11.14 \tag{45}$$

The signal-to-noise ratio of the double-loop modulator is plotted in figure 7. Because of errors in the noise assumptions, this curve does not pass through the asterisk as it should. Theoretically the double-loop modulator SNR increases 15 dB for each doubling of the sampling frequency. Compared to the basic single-loop modulator, the additional 6 dB

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provided by the double-loop circuit is due to the extra $(1-z^{-1})$ noise-shaping factor in equation (33). The noise power spectral density in equation (37) is plotted in figure 6 for fixed f_s and total quantization noise power. The amount of noise shaping is 12 dB per octave.

2.1.2.2 Performance Analysis of Higher-Order Modulators

As mentioned previously, stability is a problem for third- and higher-order modulators because each integrator introduces a 90° phase shift. Nevertheless, modifications to the classical multi-loop architecture can allow stable operation, but stability usually depends upon maintaining tight control over circuit parameters. Performance analysis of an Mth order $\Sigma\Delta$ modulator assumes a transfer function of

$$Y(z) = X(z) + (1 - z^{-1})^M E(z) \qquad (46)$$

regardless of the actual circuit schematic. It can be shown that the theoretical noise power spectral density is

$$S_N(\omega) = \frac{\Delta^2 \tau}{12} \left\{ 2[1 - \cos \omega \tau] \right\}^M \qquad (47)$$

The theoretical noise within the baseband is given as [16]

$$\sigma_B^2 = \binom{2M}{M} \frac{\Delta^2}{12} \left(\frac{2B}{f_s} \right) + (-1)^M \frac{\Delta^2}{3\pi} \sum_{k=0}^{M-1} (-1)^k \binom{2M}{k} \frac{\sin 2(M-k)\pi B / f_s}{2(M-k)} \qquad (48)$$

For high oversampling rates, equation (48) can be approximated as

$$\sigma_B^2 \approx \frac{\Delta^2 \pi^{2M}}{12(2M+1)} \left(\frac{2B}{f_s} \right)^{2M+1} \qquad (49)$$

For one-bit M^{th} order modulators, the signal-to-noise ratio is

$$SNR_B \approx \frac{3(2M+1)}{2\pi^{2M}} \left(\frac{f_s}{2B} \right)^{2M+1} \qquad (50)$$

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$$SNR_{B(dB)} \approx (6M+3)L + 10\log\left[\frac{3(2M+1)}{2\pi^{2M}}\right]$$ (51)

where

$$L = \log_2\left(\frac{f_s}{2B}\right)$$

Figures 6 and 7 show the curves for higher-order modulators.

2.1.2.3 Performance Degradation of Multi-Loop Modulators

A serious problem with multi-loop modulators is overload which is defined as excessively high signal levels within the modulator. For input levels less than $\pm \Delta/2$, simulations have shown that the maximum output of the first integrator in a double-loop modulator is about three times the maximum input level [15,17]. The output of the second integrator is about four times the input level for an input 3 dB below full scale, and the output is more than ten times the input for a full-scale input [17]. The consequence is saturation in the second integrator. Unlike the single-loop modulator in which the signal-to-noise ratio is highest for a full-scale input, the SNR of the double-loop modulator decreases rapidly as the input approaches full scale. Double-loop modulator circuits are normally operated with inputs well below full scale so that the theoretical SNR given by equation (42) for a full-scale input cannot actually be attained. Overloading can be reduced by making some slight changes in the modulator including the addition of some amplifiers [18]. However, in order to obtain the transfer function in equation (33), the relative gains must be very tightly controlled. The overload problem can be eliminated completely by using a 2-bit quantizer in the classical double-loop modulator [19], but then the linearity of the D/A converter limits performance.

The output spectrum of a second-order modulator is much smoother than that of a first-order modulator but still contains some spurious output frequencies [6]. A dither signal is not normally used. If a 2-bit quantizer is used in a double-loop modulator without overload, the quantization noise is white and uniformly distributed [9]. The other sources of performance degradation mentioned in section 2.1.1.2 for the single-loop modulator also apply to multi-loop modulators. In addition, more precise gains are needed in multi-loop modulators.

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The high signal levels in the second integrator are an additional problem. Overdriving the second integrator produces odd harmonics, especially the third harmonic [18].

2.1.2.4 Other Types of Classical Higher-Order Modulators

Many modifications to the classical modulator architecture have been proposed to improve the signal-to-noise ratio, to minimize overloading and nonlinearities, and to improve circuit stability. These are listed in table 3 for reference purposes.

Table 3. Alternative Higher-Order Modulators

No.	Modu-lator Order	Quantizer Bits	Comments	References
1	2	1	1 Loop	[20]
2	4	4	1 Loop	[13,21]
3	4	1	4 Lowpass Filters, 1 Loop	[22]
4	2	1	1 Feedforward & 2 Feedback Loops, 2 Quantizers	[23]
5	4	1	4 Feedback & 4 Feedforward Loops	[24]
6	2	1	Integrator Gain Scaling, 2 Loops	[15]
7	2	1	Integrator Gain Scaling, 2 Loops	[18]
8	2	1	Integrator Gain Scaling, 2 Loops	[25]
9	2	2	No Overload, 2 Loops	[19]
10	2	1	2 Loops	Crystal CS5317
11	4	1	?	Crystal CS5324
12	4	1	2 Feedback & 4 Feedforward Loops	Crystal CS5328[26]
13	2	1	Feedforward Loop, Gain Scaling Extra Nonlinear Feedback Loop	[27]
14	2	N-Bit Quant 1-Bit Fdbk	2 Feedback Loops, Separate Digital Input & Filter	[28]
15	3	1	Multiple Feedforward & Feedback Paths	[29]
16	3	1	Multiple Feedforward & Feedback Paths	[30,31]
17	3	5	1 Loop	[32]

2.1.2.5 Experimental Results

The performance of higher-order classical $\Sigma\Delta$ modulators is listed in table 4. These performance figures are experimental results of actual devices. Simulations have not been

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Table 4. Measured Performance of Classical Higher-Order Modulators

Number	Modulator Order	fs	B	R = fs/2B	Theoretical SNR	Measured SNR	SNR Loss	Reference
	2	15 MHz	60 kHz	125	93 dB	SNR = 77 dB; THD = -71 dB	16 dB	[33,34]
1	2	12 MHz	20 kHz	300	112 dB	SNR = 84 dB; THD = -85 dB	28 dB	[20]
2	4	6.144 MHz	20 kHz	154	192 dB	SNR = 105 dB; THD = -90 dB	87 dB	[13, 21]
3	4	256 kHz	500 Hz	256	187 dB	THD = 112 dB		[22]
4	2	2.048 MHz	4 kHz	256	108 dB	SNR = 83 dB	25 dB	[23]
5	4	2 MHz	20kHz	50	124 dB	SNR - 87 dB; SINAD = 72 dB; DR = 90 dB	37 dB	[24]
6	2	4 MHz	7.8 kHz	256	108 dB	SNR = 78 dB; SINAD = 74 dB; DR = 89 dB	30 dB	[15]
		4 MHz	15.6 kHz	128	93 dB	DR = 84 dB		
		4 MHz	31.2 kHz	64	78 dB	DR = 74 dB		
		4 MHz	62.5 kHz	32	63 dB	DR = 59 dB		
7	2	10.24 MHz	40 kHz	128	94 dB	SNR = 81 dB; DR = 88 dB	13 dB	[18]
8	2	100 kHz	500 Hz	100	88 dB	SNR = 74 dB	14 dB	[25]
10	2	2.56 MHz	9.6 kHz	133	94 dB	SINAD = 81 dB		Crystal, CS5317
11	4	256 kHz	500 Hz	256	187 dB	SNR = 115 dB; SINAD=110 dB	72 dB	Crystal, CS5324
12	4	3.072 MHz	24 kHz	64	134 dB	SNR = 94 dB; DR = 97 dB	40 dB	Crystal, CS5328, [26]
16	3	6.4 MHz	45.5 kHz	70	110 dB	SNR = 90 dB	20 dB	[30, 31]
17	3	3 MHz	23.4 kHz	64	129 dB?	SNR = 97 dB; THD = -75 dB	32 dB?	[32]

included in the table. Besides the signal-to-noise ratio, figures are sometimes given for signal-to-noise-and-distortion (SINAD), total harmonic distortion (THD), and dynamic range (DR).

The first conclusion to be drawn from the results in table 4 is that the actual SNRs are much lower than the theoretical SNRs, especially for very high theoretical SNRs. Non-ideal components, noise, overload, and spurious outputs as discussed in section 2.1.2.3 significantly degrade performance. For modulators with multi-bit quantizers (numbers 2 and 17 in the table), harmonic distortion is a much more important performance limiter than is noise. This result demonstrates why most modulators have been built with one-bit quantizers. The best signal-to-noise ratios achieved were 84 dB for second-order modulators, 97 dB for third-order modulators, and 115 dB for fourth-order modulators.

2.1.3 Cascade $\Sigma\Delta$ Modulators

Another technique for achieving better performance with higher-order modulators is to use a cascade of several basic single-loop $\Sigma\Delta$ modulators. Figure 10 shows a third-order modulator of the type of multi-stage noise shaping modulator proposed in [35-37] and designated as "MASH" by the authors. In this modulator, the input to the ith stage is the quantizer error signal from the $(i - 1)^{th}$ stage. The quantizer outputs are delayed and/or differentiated and then combined to form the output. The main advantages of this cascade architecture are guaranteed stability and no overload. In addition, when there are three or more stages, the modulator output quantization noise is white [38]. One-bit quantizers are used so that the circuit is linear. A slightly different architecture with similar characteristics is described in [39]. The following subsections discuss theoretical and actual performance for the type of modulator in figure 10.

2.1.3.1 Performance Analysis

The following equations apply to the ith stage in figure 10:
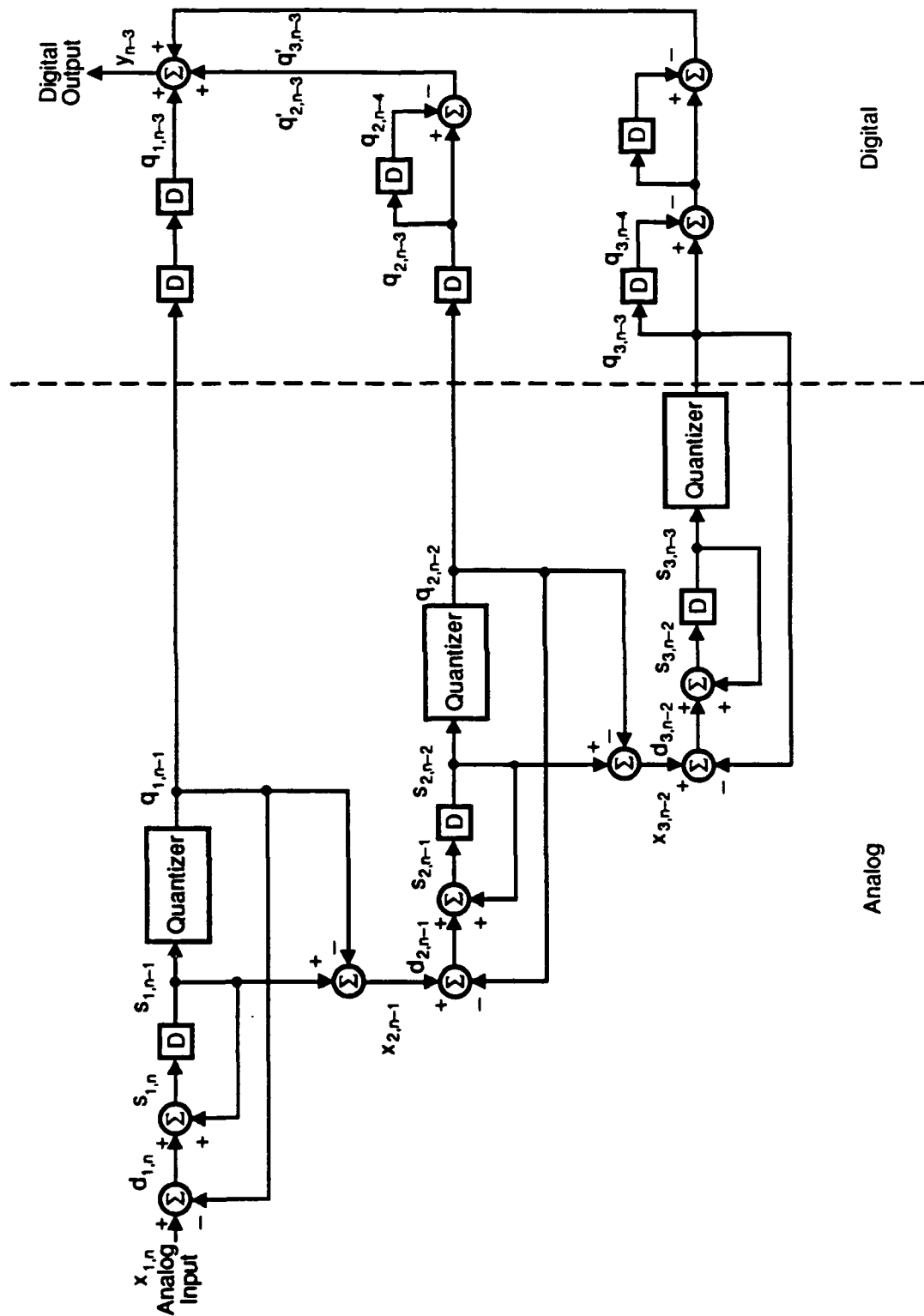
$$d_{i,n} = x_{i,n} - q_{i,n-1} \tag{52}$$

Figure 10. Cascade $\Sigma\Delta$ Modulator (Three-Stage)

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$$s_{i,n} = d_{i,n} + s_{i,n-1} \tag{53}$$

$$q_{i,n-1} = e_{i,n-1} + s_{i,n-1} \tag{54}$$

Combining these equations yields

$$q_{i,n} = x_{i,n} + e_{i,n} - e_{i,n-1} \tag{55}$$

The input to the $(i + 1)^{th}$ stage is

$$x_{i+1,n-1} = s_{i,n-1} - q_{i,n-1} = -e_{i,n-1} \tag{56}$$

The outputs of the three quantizers are

$$q_{1,n-1} = x_{1,n-1} + e_{i,n-1} - e_{1,n-2} \tag{57}$$

$$q_{2,n-2} = -e_{1,n-2} + e_{2,n-2} - e_{2,n-3} \tag{58}$$

$$q_{3,n-3} = -e_{2,n-3} + e_{3,n-3} - e_{3,n-4} \tag{59}$$

For a two-stage modulator

$$y_{n-3} = q_{1,n-3} + q'_{2,n-3} \tag{60}$$

$$y_{n-3} = x_{1,n-3} + e_{2,n-3} - 2e_{2,n-4} + e_{2,n-5} \tag{61}$$

For a three-stage modulator

$$y_{n-3} = q_{1,n-3} + q'_{2,n-3} + q'_{3,n-3} \tag{62}$$

$$y_{n-3} = x_{1,n-3} + e_{3,n-3} - 3e_{3,n-4} + 3e_{3,n-5} - e_{3,n-6} \tag{63}$$

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Examination of equations (57), (61), and (63) shows that the modulator output equals the input plus shaped quantization noise from the last stage only. The quantization noise from each stage (except the last stage) is canceled by its succeeding stage. Taking transforms of equations (57), (61), and (63) produces the general equation

$$Y(z) = X(z) + (1-z^{-1})^M E(z) \tag{64}$$

which is the transfer function of an ideal M^{th} order $\Sigma\Delta$ modulator.

For one-bit quantizers, overload is prevented by setting all three quantizer levels at $\pm \Delta/2$ which is also the maximum excursion of the input signal. Then the maximum possible signal levels within all stages of the modulator are shown in table 5.

Table 5. Cascade Modulator Maximum Signal Levels

Point in Modulator	Maximum Signal Levels
x_i	$\pm \Delta/2$
d_i	$\pm \Delta$
s_i	$\pm \Delta$
q_i	$\pm \Delta/2$
e_i	$\pm \Delta/2$

The digital output of an M-stage modulator has 2^M levels. If the quantizer outputs are normalized to ± 1, the modulator output levels are $\pm 1, \pm 3, \pm 5, ...\pm 2^M - 1$. Unfortunately, $M + 1$ bits are needed to represent the output in twos-complement notation.

2.1.3.2 Causes of Performance Degradation

The integrator is a very critical component in cascade modulators just as it is in classical modulators. Equation (23) shows that leakage in the integrator produces a small additional noise term, δe_{n-1}, at the output of the quantizer in the first stage. This noise term is not canceled in stage #2, but instead appears at the modulator output as if it were added directly to the input. Integrator leakage in later stages is differentiated (shaped) at least once in the

to the input. Integrator leakage in later stages is differentiated (shaped) at least once in the digital logic. Hence the design of the integrator in the first stage is the most critical with regard not only to leakage but also to other non-ideal effects. All of the integrator imperfections discussed in section 2.1.1.2 can cause performance degradation in a multi-stage modulator and are especially important in the first stage.

An additional source of error in multi-stage modulators is gain mismatch between stages. If this occurs, the input to the second stage is not $-e_{1,n-1}$ as given by equation (56) but is

$$x_{2,n-1} = -(1-\varepsilon)\, e_{1,n-1} \tag{65}$$

Then equation (58) becomes

$$q_{2,n-2} = -(1-\varepsilon)\, e_{1,n-2} + e_{2,n-2} - e_{2,n-3} \tag{66}$$

and equation (61) for the output of a two-stage modulator becomes

$$y_{n-3} = x_{1,n-3} + \varepsilon(e_{1,n-3} - e_{1,n-4}) + e_{2,n-3} - 2e_{2,n-4} + e_{2,n-5} \tag{67}$$

Thus the quantization noise from the first stage is not completely canceled, but a small amount of it is shaped by the second stage and appears at the output.

2.1.3.3 Experimental Results

Table 6 lists the performance of the three cascade modulators actually fabricated and reported in the literature. All of these modulators use one-bit quantizers. The signal-to-noise ratios of modulator numbers two and three are comparable to those for classical modulators. A major difference between the results for the two types of modulators is that spurious outputs are more likely to limit performance in classical modulators than in cascade modulators.

Table 6. Measured Performance of Cascade Modulators

No.	Mod. Order	f_s	B	$R=f_s/2B$	Theor. SNR	Measured SNR	SNR Loss	Ref.
1	2	2.048 MHz	3.4 kHz	301	112 dB	SNR = 69 dB	43 dB	[35]
2	3	3.0 MHz	24 kHz	62.5	106 dB	SINAD = 91 dB THD = 93 dB	15 dB	[36]
3	3	10.24 MHz	80 kHz	64	106 dB	SINAD = 91 dB	15 dB	[39]

2.1.4 Summary

A $\Sigma\Delta$ modulator is a relatively simple A/D converter which samples the signal at rates which are many times the baseband frequency to produce a low-resolution digital output. The high-level modulator quantization noise is shaped so that most of the noise lies above the baseband. An Mth order modulator has a transfer function of

$$Y(z) = X(z) + (1 - z^{-1})^M \ Q(z) \tag{68}$$

where $Q(z)$ is the quantization noise. Derivation of the theoretical signal-to-noise ratio is based on the assumption of white quantization noise, an assumption that is not usually valid. This assumption results in a theoretical signal-to-noise ratio within the baseband of

$$SNR_{B(dB)} \approx (6M+3)L+10\log\left[\frac{3(2M+1)}{2\pi^{2M}}\right] \tag{69}$$

where L is the logarithm to the base two of the oversampling ratio $f_s/2B$.

$\Sigma\Delta$ modulators are divided into two basic types, classical or multi-loop and cascade or multi-stage. The single-loop modulator shown in figure 4 is the basis for all $\Sigma\Delta$ modulators. Careful implementation of the integrator is critical to achieving a high signal-to-noise ratio.

If a multi-bit quantizer is used, the linearity of the D/A converter is also very important. Signal-to-noise ratios of as much as 115 dB have been achieved with fourth-order modulators and oversampling ratios of 256. Because of implementation problems at high sampling rates, $\Sigma\Delta$ converter applications have been limited to signals in the audio band. A summary of $\Sigma\Delta$ modulator architectures and characteristics is given in table 7.

2.2 DIGITAL FILTERS

A $\Sigma\Delta$ A/D converter requires a digital filter in addition to the $\Sigma\Delta$ modulator. The function of the digital filter is to attenuate the out-of-band noise and downsample the data. The digital filter input is digital b-bit words (b is one or a small number) at a very high sampling rate, f_s. The output of the digital filter is n-bit words at a sampling rate of f_s/N.

Much has been written about digital filtering of $\Sigma\Delta$ modulator output data because of the special considerations pertinent to this application. First of all is the particular spectral shape of the out-of-band noise. Secondly, the very high input data rate limits the hardware implementation options. Several stages of filtering and decimation are normally used so that trade-offs between the filter frequency responses and the intermediate sampling rates for each stage must be considered. If a cascade $\Sigma\Delta$ modulator is used, a method exists for incorporating the digital section of the modulator into the first filter. The following sections discuss the types of filters used in $\Sigma\Delta$ converters, the basic architecture for the multi-stage filter, filter transfer functions, and implementation issues.

2.2.1 Types of Filter Responses

2.2.1.1 Sinc^k Filters

Before discussing sinc^k digital filters, a review of the sinc function and some digital filtering concepts is useful. The sinc function is defined as

$$\text{sinc } x \equiv \frac{\sin \pi x}{\pi x} \tag{70}$$

Table 7. Sigma-Delta Modulators

ARCHITECTURE	SNR	SPURIOUS OUTPUTS	OVERLOAD	STABILITY	COMMENTS
Basic Single Loop 1 Bit	Low	Many High-Level without Dither	No	Always Stable	
Classical Double Loop 1 Bit	Medium	Some	Yes	Stable if Designed Carefully	
Classical Double Loop 2 Bits	Medium	Some	No	Stable if Designed Carefully	D/A Accuracy Critical.
Classical >2 Loops 1 Bit	High	Few	Depends on Circuit	Stable if Designed Carefully	Component Tolerances Important.
Classical >2 Loops >1 Bit	High	Few	Depends on Circuit	Stable if Designed Carefully	D/A Accuracy Critical. Component Tolerances Important.
Cascade ≥ 2 Stages 1 Bit/Stage	Medium - High	Few - None	No	Always Stable	Gain Matching Between Stages Important.

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For continuous signals with the time-domain waveforms shown in the left-hand column in figure 11, their sinc^k frequency-domain responses as obtained by taking Fourier transforms are shown in the right-hand column. Nulls are produced at multiples of 1/T. The sidelobes extend to $\pm \infty$. As k increases, the sidelobe levels decrease. The frequency responses are also shown in figure 12. The sidelobe peaks are shown to decrease at a rate of 6k dB per octave.

Consider next samples of the rectangular waveform in figure 11 (with the origin shifted to the left-hand edge of the pulse).

$$h_n = \begin{cases} 1, & 0 \le n \le N-1 \\ 0, & \text{elsewhere} \end{cases} \tag{71}$$

The discrete Fourier transform is then

$$H(\omega) = \sum_{n=-\infty}^{\infty} h_n e^{-j\omega n} = \sum_{n=0}^{N-1} e^{-j\omega n} \tag{72}$$

$$H(\omega) = 1 + e^{-j\omega} + e^{-j2\omega} + \cdots e^{-j(N-1)\omega} = \frac{1 - e^{-jN\omega}}{1 - e^{-j\omega}} \tag{73}$$

$$H(\omega) = \frac{e^{-jN\omega/2}\left(e^{jN\omega/2} - e^{-jN\omega/2}\right)}{e^{-j\omega/2}\left(e^{j\omega/2} - e^{-j\omega/2}\right)}$$

$$H(\omega) = e^{-j(N-1)\omega/2}\left[\frac{\sin(N\omega/2)}{\sin(\omega/2)}\right] \tag{74}$$

The magnitude of $H(\omega)$ is plotted in figure 13 for N = 5. The frequency response is seen to be an aliased version of the (sin x)/x response of the continuous signal shown in figure 11. Samples of the other waveforms in figure 11 produce similar aliased frequency responses with lower sidelobes.
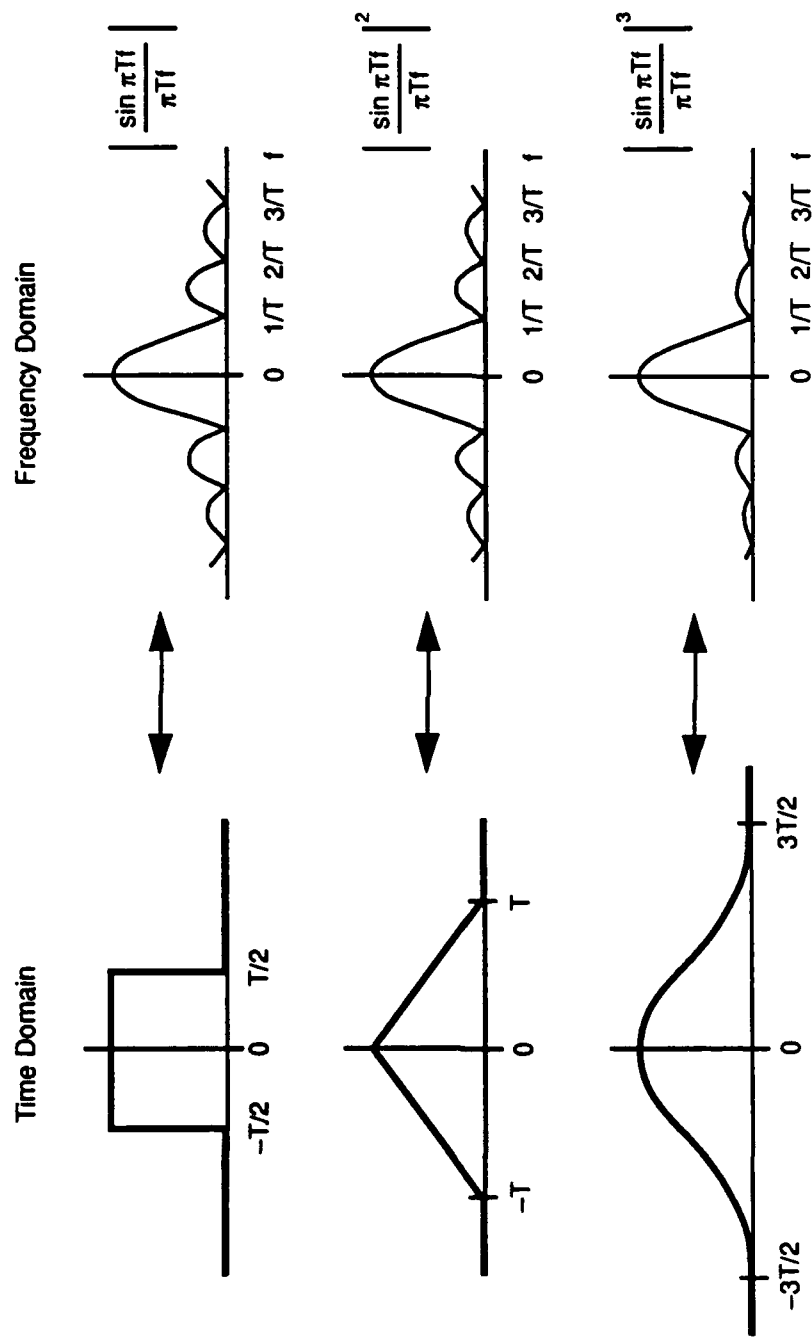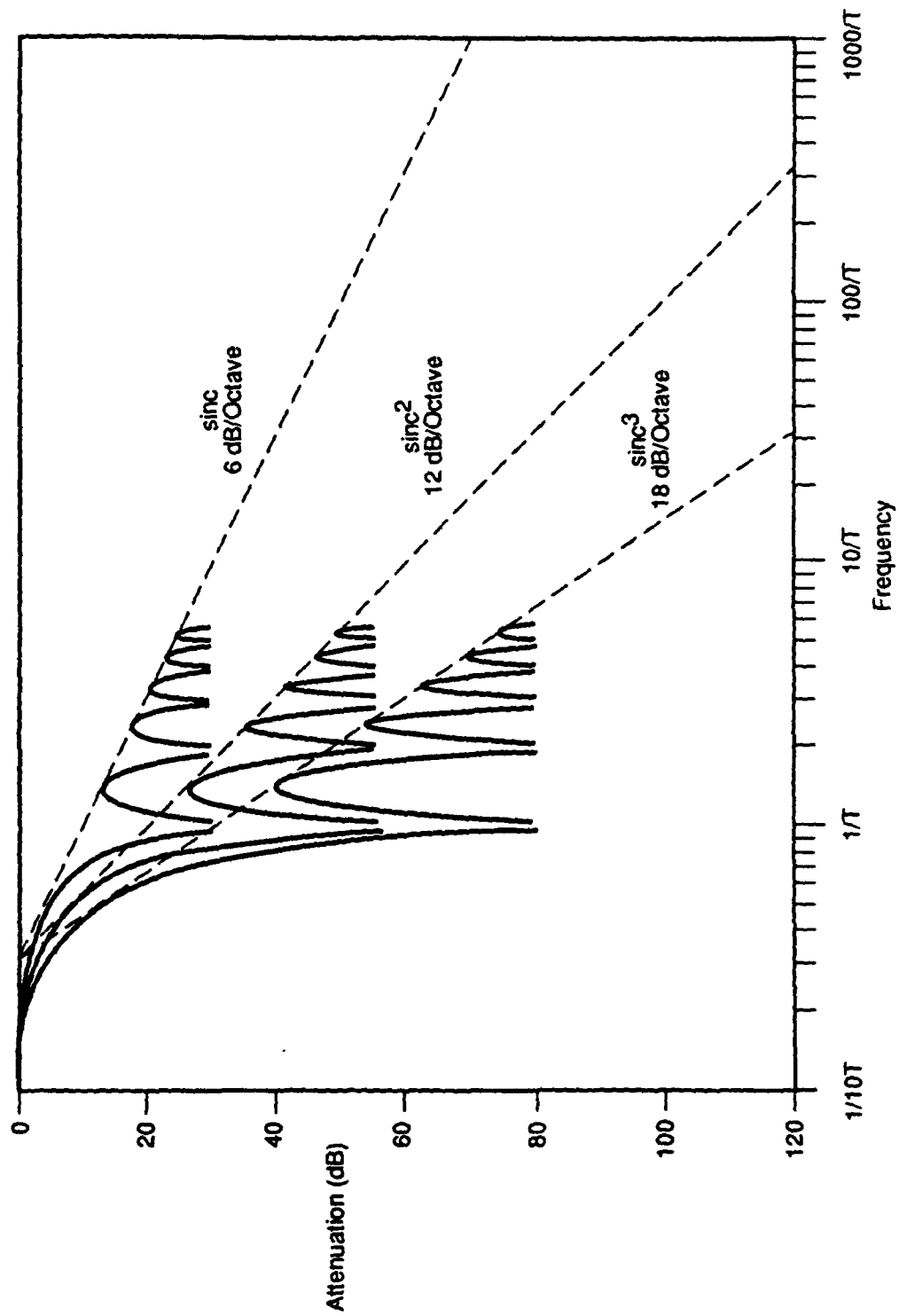
35

Figure 11. Sinc^k Functions

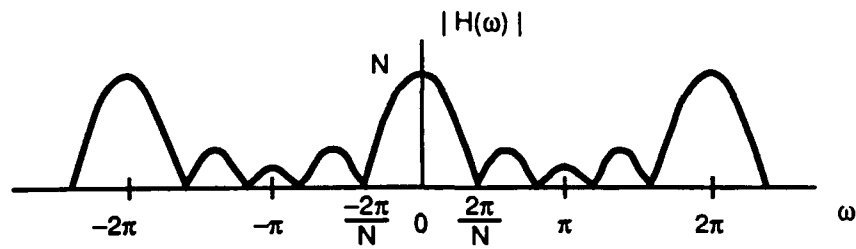Figure 12. Sinc^k Function Frequency Response

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Figure 13. Frequency Response of Sampled Rectangular Pulse

When filtering a digital signal, calculations are usually performed on one block of data samples at a time. In a preliminary step, the digital data stream is windowed by some function such as one of the time-domain functions in figure 11. Windowing consists of multiplying each digital sample in a block of samples by the digitized amplitude of the window function at the corresponding point in time, that is

$$y_n = w_n x_n \tag{75}$$

A $sinc^k$ filter, which is sometimes called a comb filter, is a finite impulse response (FIR) filter with coefficients equal to the amplitudes of the corresponding samples of one of the time-domain waveforms in figure 11. A diagram of an N-stage FIR filter is shown in figure 14.
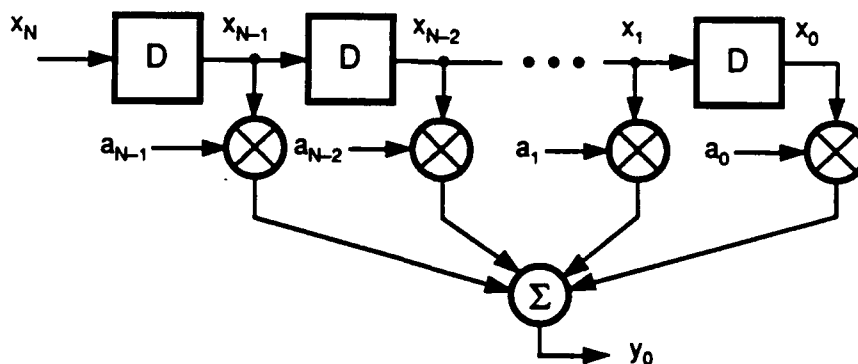

Figure 14. FIR Filter

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The sinc^k filter first windows the data with a sinc^k window and then adds the N weighted samples. The filter output is

$$y_0 = \sum_{n=0}^{N-1} a_n x_n \qquad (76)$$

Because the a_n are symmetrical, a sinc^k filter has linear phase. The sinc^1 filter in which the a_n equal one is sometimes called a moving-average or accumulate-and-dump or integrate-and-dump filter. The sinc^2 filter is also called a triangular filter. Taking z transforms of equation (76) for the sinc^1 filter yields

$$Y(z) = X(z)\left[\sum_{n=0}^{N-1} z^{-n}\right] = \left[\frac{1-z^{-N}}{1-z^{-1}}\right] X(z) \qquad (77)$$

The transfer function of the sinc^1 filter is

$$H(z) = \frac{Y(z)}{X(z)} = \frac{1-z^{-N}}{1-z^{-1}} \qquad (78)$$

which is the frequency response of a sampled sinc^1 signal as given by equation (73) with $z = e^{j\omega}$.

Summarizing, a sinc^k filter multiplies the spectrum of the data by the spectrum of an aliased sinc^k function such as that shown in figure 13. In this figure, f_s corresponds to $\omega = 2\pi$, and the signal baseband lies within the main lobe close to zero. Because the oversampling rate is very high, the sinc^k filter response may be designed to have many sidelobes by making N large. N is the number of samples in time T at a sampling rate of f_s. For a sinc^k filter, the length of the filter (number of stages) is shown in figure 11 to be

$$L = kN = kf_s T \qquad (79)$$

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The peaks of the sidelobes of a sinc^k filter roll off at 6k dB per octave if the aliasing is negligible or slightly less than that with aliasing. This stopband response is the reason that almost all $\Sigma\Delta$ digital filters use a sinc^k filter to counteract the 6M dB per octave rise in the noise spectrum out of the Mth order $\Sigma\Delta$ modulator. If a single sinc^k filter is used to filter the output of an Mth order modulator, and if the filter output is downsampled by R, and if the length of the filter is held constant at R so that N = R/k, it has been shown that a good sinc^k filter choice is k = M + 1 [7, 19, 38, 40].

Any sinc^k filter can be implemented as a tapped delay line FIR filter as shown in figure 14. For k = 1 the a_n equal one, and the filter can also be implemented as an accumulator. For one-bit data the filter can be a counter. A sinc^2 filter uses triangularly weighted coefficients which can be generated by an up-down counter. Higher order sinc^k filters require ROMs to supply the coefficients. An alternative approach to implementing a sinc^k filter is to use k cascaded sinc^1 filter stages.

2.2.1.2 Other Filters

An equiripple filter is an FIR filter which equalizes the ripple in the passband and in the stopband. The filter coefficients are symmetrical so that the filter also has linear phase. This filter is described in [41]. The Remez algorithm is used to determine the filter coefficients.

The desire to minimize filter hardware has led to efforts to design FIR filters whose coefficient bits are mostly zeros with only a few ones. Refer to [42, 43]. A half-band linear phase FIR filter has an impulse response (coefficients) of

$$h(n)=\frac{\sin \pi n / 2}{\pi n} \qquad n = -N, -N+1, \cdots -1, 0, 1, \cdots N-1, N \qquad (80)$$

Of the 2N + 1 coefficients, N of them equal zero so that the hardware required is minimized. The cut-off frequency of the filter is one-fourth of the sampling frequency. A quadratic programming approach can provide higher signal-to-noise ratios with shorter filter lengths [44].

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2.2.2 ΣΔ Filter Architectures

2.2.2.1 Decimating Filter Principles

If one digital filter is used to filter the ΣΔ modulator output at a sampling rate of f_s and to output data at the Nyquist rate, 2B, the length of the filter must be at least as large as the oversampling rate, R. Such a filter requires much hardware. In addition, the multipliers in the FIR filter have to operate at the modulator sampling rate. A much more efficient approach is to use several filter stages with downsampling after each stage. Downsampling or decimation by D consists of taking every D^{th} sample. A multi-stage filter with decimation is shown in figure 15. The first stage should be a simple filter which can be implemented with high-speed circuits. Its response must be sufficient to allow downsampling at f_s/D_1 without aliasing as shown in figure 16. The next stage would typically be a more complicated filter that provides very sharp attenuation just beyond the edge of the baseband. Because this filter operates at a lower speed, more complicated components such as multipliers are usually available for implementation. Figure 16 shows the spectra of the quantization noise at each stage of a two-stage filter. The baseband is shaded.

In order to determine the overall transfer function of the multi-stage decimating filter shown in figure 15, it is necessary first to recognize the equivalence between the two decimating filters shown in figure 17. This equivalence becomes clear by considering that a filter with D delay stages (represented by z^{-D}) ahead of a decimator by D is equivalent to a filter with one delay stage (represented by z^{-1}) after decimation by D. Figure 15 can then be redrawn as figure 18 by using the following procedure:

1. Replace the combination of D_1 and $H_2(z)$ with the combination of $H_2(z^{D_1})$ and D_1.
2. Combine D_1 and D_2 into one decimator $D_1 D_2$.
3. Repeat steps 1 and 2 for succeeding pairs of decimators and filters.
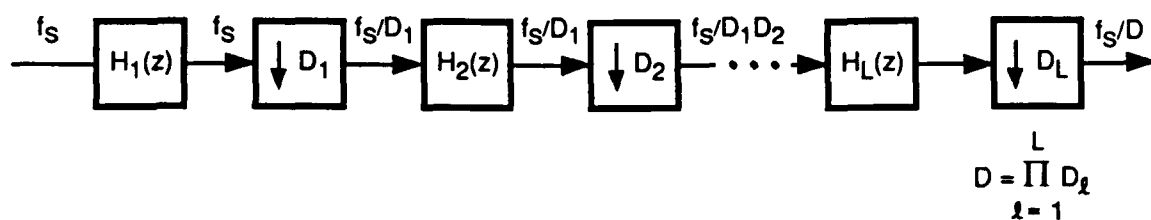
41
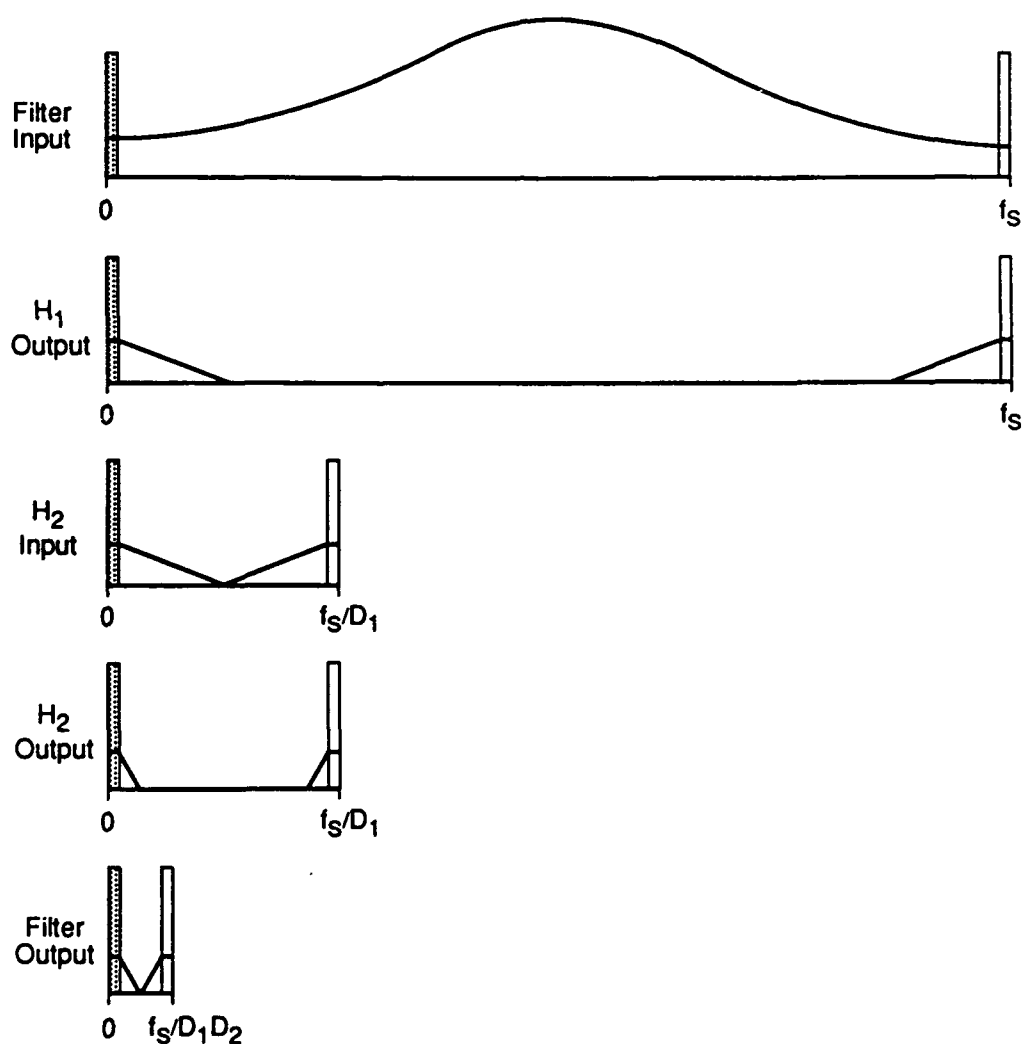
Figure 15. Multi-Stage Digital Filter with Decimation

Figure 16. Spectra in Two-Stage Digital Filter with Decimation
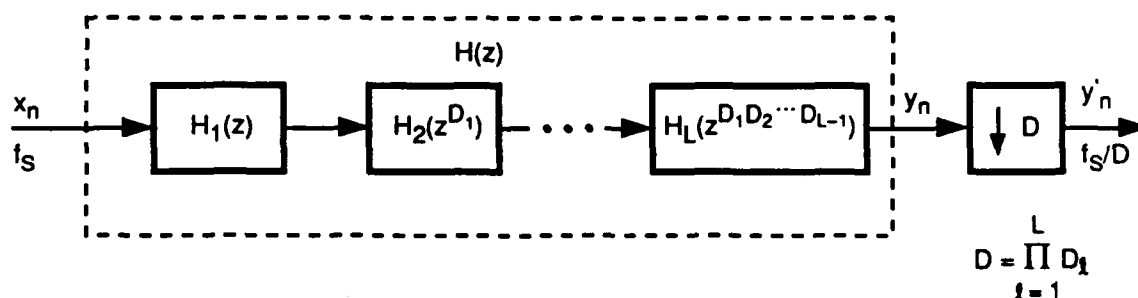
42

Figure 17. Equivalent Decimating Filters

$$D = \prod_{\ell=1}^{L} D_\ell$$

Figure 18. Equivalent Multi-Stage Decimating Filter

The resulting transfer function is

$$H(z) = H_1(z)\, H_2(z^{D_1})\, H_3(z^{D_1 D_2}) \cdots H_L(z^{D_1 D_2 \cdots D_{L-1}}) \tag{81}$$

Thus decimation in stages as shown in figure 15 allows the transfer function of equation (81) to be implemented with a cascade of much shorter filters.

2.2.2.2 Decimating Sinc^k Filters

Consider next methods for implementing sinc^1 filters using decimation. As an example, consider an eight-stage filter with a transfer function of

$$H(z) = \sum_{n=0}^{7} z^{-n} \tag{82}$$

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This filter could be implemented as a canonical FIR filter with eight stages as shown in figure 14. An alternative approach is based on recognizing that equation (82) can also be written as

$$H(z) = \left(\frac{1}{1 - z^{-1}} \right)\left(1 - z^{-8} \right) \tag{83}$$

This transfer function can be implemented as two filters, an IIR filter (integrator) and an FIR filter (differentiator), as shown in figure 19A without decimation and in figure 19B with decimation.
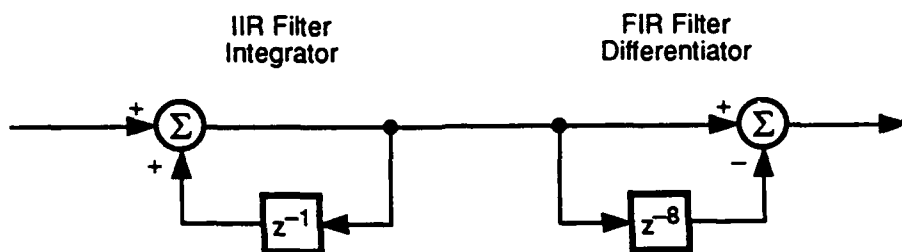
19A. Without Decimation
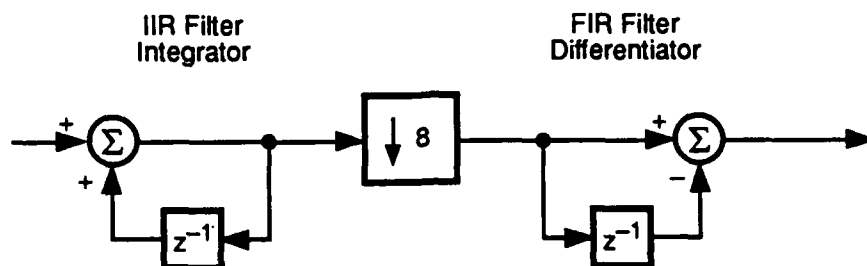
19B. With Decimation

Figure 19. Sinc[1] Filter Implementation with IIR and FIR Filters

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Note the reduction in hardware which is possible with decimation. Of course, decimation can be used only if the integrator (lowpass filter) attenuates the high frequency noise sufficiently so that aliasing is not a problem. For $\Sigma\Delta$ A/D converters, higher order sinc^k filters are required because of the high-level out-of-band noise. For a required transfer function of

$$H(z)=\left(\frac{1}{1-z^{-1}}\right)^k\left(1-z^{-8}\right)^k \tag{84}$$

a cascade of k integrators should precede the decimator. Then the general form of the IIR-FIR decimating sinc^k filter is shown in figure 20.
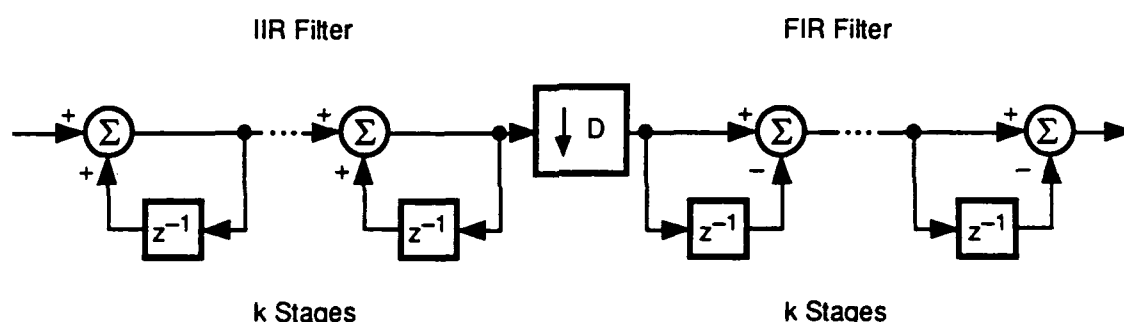

Figure 20. General IIR-FIR Decimating Sinc^k Filter

This type of filter was first proposed in [45] with k stages in each of the IIR and FIR sections and with M delays in each FIR stage. The frequency response of the filter is

$$H(\omega)=\left[\frac{\sin(MD\omega/2)}{\sin(\omega/2)}\right]^k \tag{85}$$

The advantages of this filter are as follows:

o   No multipliers are required.
o   All of the coefficients are one.
o   Storage requirements are less than those for an equivalent FIR filter.
o   The structure is regular.
o   The same architecture can be used for a wide range of decimation factors.

One additional advantage of this filter for a cascade $\Sigma\Delta$ modulator is that some of the modulator digital logic for the alternate modulator architecture in [39] is incorporated into the first few IIR filter stages.

The disadvantages of this type of filter are the following:

o   The transfer function is determined by only three factors (k, D, and M) so that the range of achievable filter characteristics is limited.

o   Register widths may need to be large to prevent overflow and instability. (Refer to [45, 46].)

The sinc[1] filter transfer function in equation (83) can also be implemented as a cascade of FIR filters using the relation

$$H(z) = \sum_{n=0}^{7} z^{-n} = \left(1 + z^{-1}\right)\left(1 + z^{-2}\right)\left(1 + z^{-4}\right) \qquad (86)$$

Decimation reduces the hardware required as shown in figure 21. For higher order sinc[k] filters, each FIR stage is replaced with a cascade of k stages. This type of filter has no overflow or stability problems. However, the achievable filter responses are limited.

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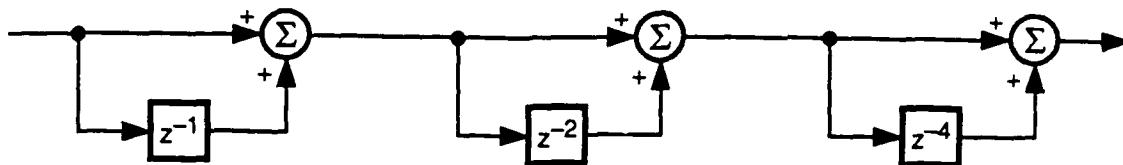
21A. Without Decimation
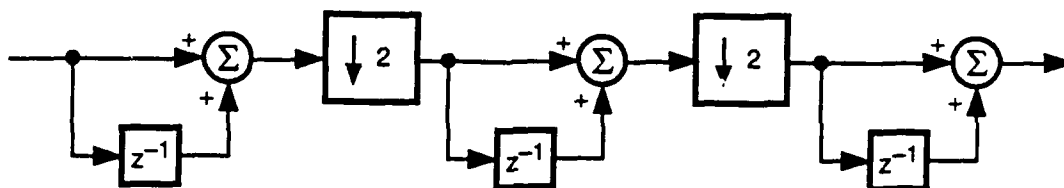
21B. With Decimation

Figure 21. Sinc[1] Filter Implementation with FIR Filters

2.2.2.3 Decimating $\Sigma\Delta$ Filters

After considering the various types of filter responses, methods for implementing these filters with simple digital circuits, and the use of decimation to minimize the hardware requirements, the matter to be considered next is the actual design of a $\Sigma\Delta$ decimating filter. Although each application has its own specific requirements, almost all of the $\Sigma\Delta$ filters reported in the literature have the same basic structure which is shown in figure 22. The first filter is a decimating $sinc^k$ filter with $k = M + 1$ where M is the order of the modulator. Decimation may occur in several steps within the filter, but the output rate is f_s/D which is made equal to slightly more than four times the bandwidth. The first null of the $sinc^k$ filter is also made to occur at f_s/D so that all the aliasing bands are located around the nulls in the $sinc^k$ frequency response as shown in figure 23. The second filter is a lowpass filter (e.g.,

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sinc, equiripple, half-band) which shapes the response in the passband and attenuates the stopband sufficiently to allow decimation by two to a frequency slightly more than the Nyquist frequency of twice the bandwidth. This lowpass filter requires many stages to provide the required spectral shaping. Because its input data rate is only four times the bandwidth, multipliers and special digital filtering ICs can be used.
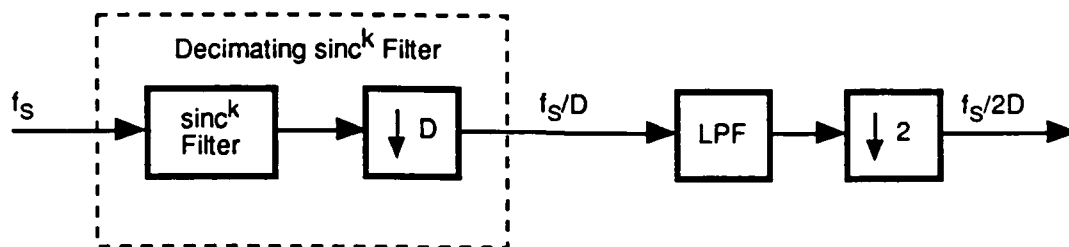

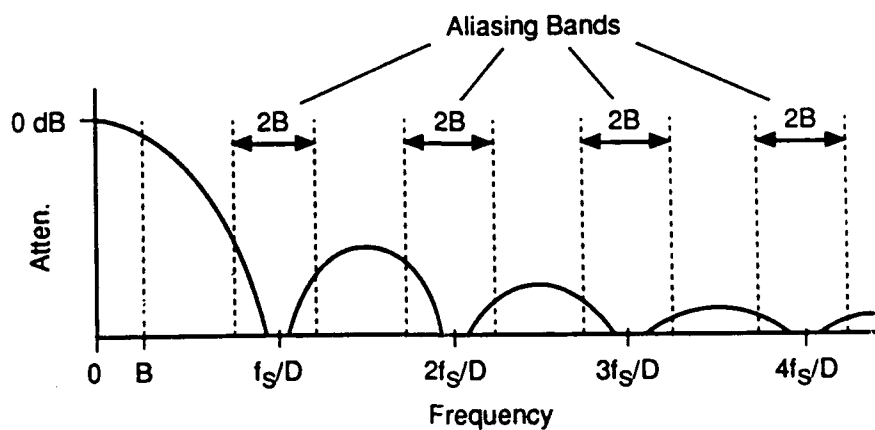Figure 22. $\Sigma\Delta$ Filter Architecture

Figure 23. Decimating Sinc^k Filter Frequency Response

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SECTION 3

SUPERCONDUCTIVITY BACKGROUND

3.1 SUPERCONDUCTING MATERIALS AND CHARACTERISTICS

The ability of materials to conduct current with zero resistance was discovered in 1911. Mercury, tin, and lead were found to suddenly become superconductive as the temperature was lowered to about that of liquid helium (4.2 K). Beginning in the 1950s, several hundred compounds (mainly niobium compounds) with critical temperatures in the 17 K to 23 K range were discovered. The breakthrough in high-temperature superconductivity occurred in 1986 with rare earth copper oxides. These materials fall into three basic types, 40 K, 95 K, and 125 K materials, of which the latter two can be cooled with liquid nitrogen at 77 K. These high-temperature mixed-metal oxides have the mechanical and physical properties of ceramics. They are strong but brittle. Fabrication presents problems, and only a few experimental devices have been built. In contrast, fabrication of low-temperature superconductors is quite routine.

In order to remain in the superconducting state, a material must be held within an envelope of temperature, current density, and magnetic field strength. These critical values depend upon the material. DC current can flow in a superconducting material without loss. The resistance of the material to AC current is very low but not zero. Another phenomenon of superconducting materials is the Meissner effect. A low-temperature superconductor will not allow a magnetic field to penetrate its interior.* If a superconductor is approached by a magnetic field, it sets up currents on its surface that create an equal but opposite magnetic field. Thus if a magnet is placed above a superconductor, the opposing magnetic field will keep the magnet suspended above the superconductor.

A comprehensive microscopic theory of superconductivity was put forth by Bardeen, Cooper, and Schrieffer in 1957. According to this BCS theory, at low temperatures pairs of

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* The action of a high-temperature superconductor is somewhat different.

electrons (Cooper pairs), which normally repel each other, attract each other and form an electrical superfluid with energy levels a discrete amount below those of normal electron states. This difference in energy levels is the superconducting energy gap. The BCS theory does not completely explain the operation of high-temperature superconductors. As discussed in [47], the mechanism of high-temperature superconductivity is almost certainly different from that of low-temperature superconductivity.

3.2 SUPERCONDUCTING DEVICES

Early proposed applications for superconducting materials were as current carriers in electric power systems and electromagnets. Our interest is in devices for electronic applications. Two important components are Josephson junctions and superconducting quantum interference devices. These devices have a number of important attributes: fast switching, low power, wide bandwidth, low noise, and high sensitivity.

3.2.1 Josephson Junction (JJ) Devices

In 1962 Josephson analyzed what would happen at the intersection of two superconductors which are separated by a thin insulating barrier. He predicted that a supercurrent would tunnel through the Josephson junction and that there would be no voltage drop across the junction provided that the current did not exceed a critical value. This DC Josephson effect results in the current-voltage characteristic shown in figure 24. As the current is increased, the JJ remains in its zero-voltage state until the current reaches the critical current, I_C. At that point, the JJ quickly switches along the load line to the voltage state at a voltage of $2\Delta/e$ where Δ is the energy gap and e is the electron charge. The value of $2\Delta/e$ is about 2.9 mV. As the current returns to zero, the transfer curve is retraced back to zero.
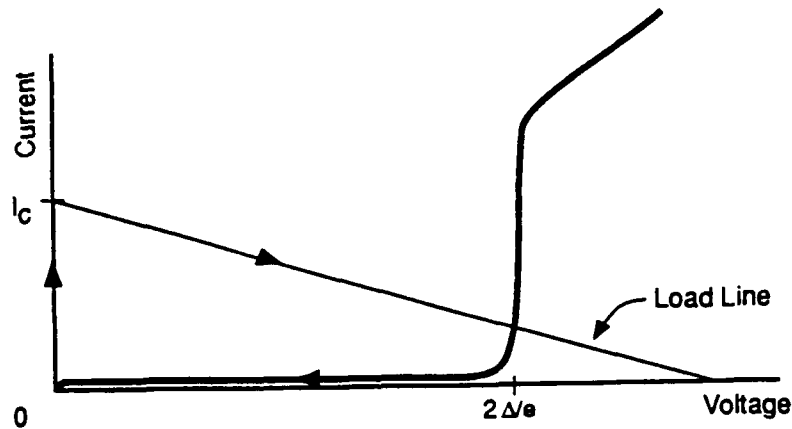
Figure 24. Josephson Junction Transfer Function

The theoretical switching speed from the zero-voltage to the voltage state has been predicted to be [48]

$$T_{sw} = \hbar/2\Delta$$

where

$\hbar$ = reduced Planck's constant = $h/2\pi$ = 1.0546×10^{-34} J-s

For Pb-alloy Josephson junctions, $T_{sw} \sim 0.23$ ps. A modeling study of practical single-junction devices has concluded that the narrowest pulse to which the junction can respond is about 2 ps [49]. Experimental tests of a Josephson junction sampler produced a rise time of 2.1 ps, and improved designs were predicted to have rise times of less than 1 ps [50]. Switching speed is limited by the junction capacitance, C, and the charging current, I. (Refer to the equivalent circuit in figure 25.) The smallest practical ratio of C/I is stated in [51] to be 0.5 pF per milliampere which corresponds to the approximate upper limit in junction current density of 10^4 A/cm² for Nb - Al₂O₃ - Nb junctions. Then the junction switching time would equal about 1.5 ps. This fast switching speed of about 1-2 ps is the reason for considering superconducting devices for the high-speed A/D converter.
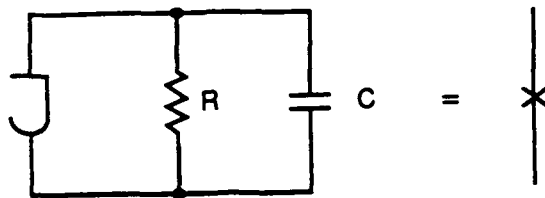
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Figure 25. Josephson Junction Equivalent Circuit

Josephson also predicted that a DC voltage across the junction would create a high-frequency AC supercurrent. The frequency of this oscillation is

$$f = \frac{2e}{h}V = 483.6 \times 10^{12} \quad Hz/V$$

where

h = Planck's constant = 6.6262×10^{-34} J-s

V = DC voltage

This relationship between voltage and frequency was the basis of a previous A/D converter design approach. Two other Josephson effects also occur. If the voltage applied across the junction is equal to nhf/2e where n is an integer, and if an RF field is applied across the JJ, a direct supercurrent will flow. In addition, if an unbiased (zero current) JJ is radiated with an RF field, a DC voltage is generated across the junction. This voltage is at steps of nhf/2e. Although these AC effects are interesting phenomena, our interest is in the DC effect and the switching characteristics.

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3.2.2 Superconducting Quantum Interference Devices (SQUIDs)

A SQUID contains one or more Josephson junctions connected in one or more superconducting loops. RF SQUIDs are constructed with one JJ in one loop. DC SQUIDs usually have two JJs in one loop. These SQUID designations refer to the type of biasing used. The basic characteristic of SQUIDs is flux quantization where one flux quantum equals

$$\Phi_0 = \frac{h}{2e} = 2.07 \times 10^{-15} \quad \text{Wb.}$$

An important application for both RF and DC SQUIDs is as magnetometers in which magnetic flux passes through the loop. A flux-locked loop circuit is used to convert magnetic flux to voltage.

The flux quantization characteristic of the DC SQUID in figure 26 can be used in several other ways. The signal current I_S, is inductively coupled to the SQUID to produce a flux, Φ, through the SQUID loop. Biasing is provided by the current I. The output is the voltage across the SQUID. If the JJs are resistively shunted and if $I_B > 2I_C$, the output depends on I_B and I_S as shown in figure 27. If I_S produces an integral number of flux quanta through the loop, the output voltage for a given bias current is low. Other values of I_S produce higher output voltages. Thus the SQUID can be used as a flux-to-voltage converter with a periodic characteristic. A SQUID can also be used as a comparator with an output voltage of zero when the JJs are in the superconducting state or with an output voltage of the gap voltage of about 2.9 mV when the JJs are in the voltage state. The JJ critical current, I_C, depends upon the flux through the loop and hence upon the signal current, I_S, as shown in figure 28. As the analog input signal current, I_S, is varied, the current I is pulsed to be equal to I_{TH}. If I is less than I_C, the output remains at zero. If I is greater than I_C, the SQUID switches to its voltage state. The result is that the SQUID acts as a comparator. A "1" is produced whenever the SQUID is pulsed with $I = I_{TH}$ greater than I_C, and a "0" is produced when the $I = I_{TH}$ pulse is less than I_C. The value of I_{TH} is adjusted for equal "1" and "0" pulse widths.
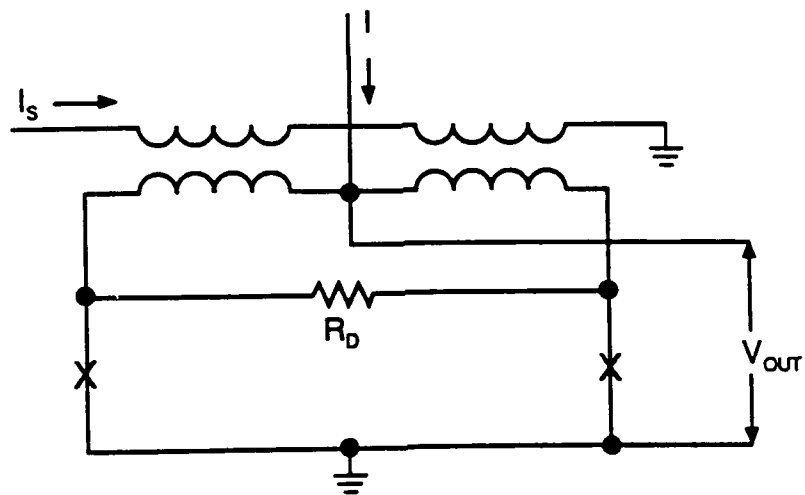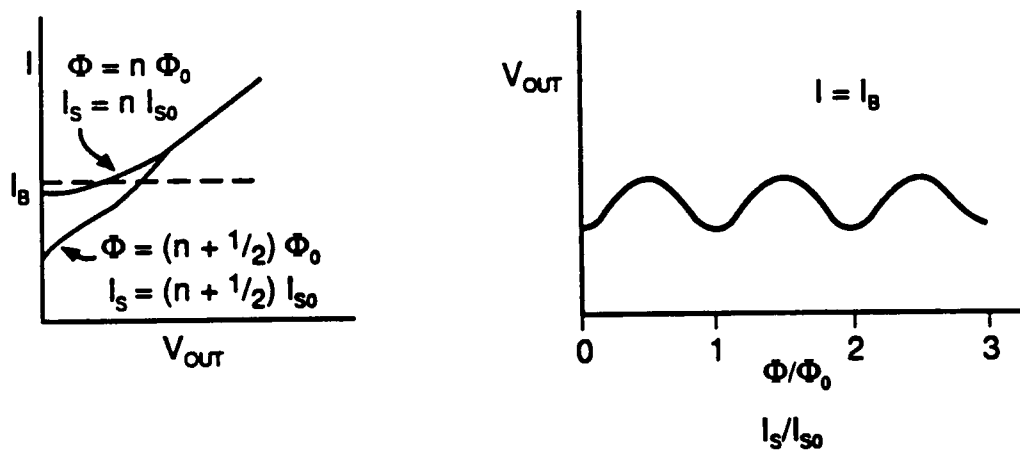
Figure 26. DC SQUID Circuit

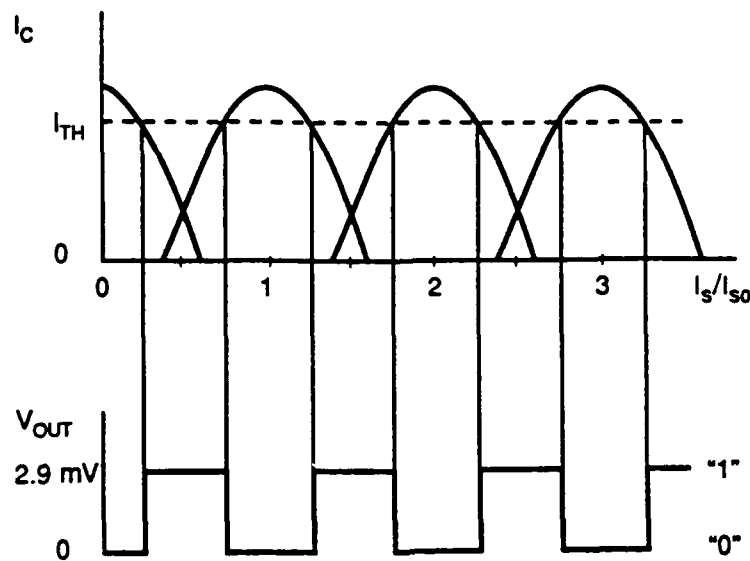Figure 27. DC SQUID Characteristics

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Figure 28. DC SQUID Comparator Operation

3.3 SUPERCONDUCTOR CIRCUITS

3.3.1 Comparators

DC SQUIDs of the type shown in figure 26 are commonly used as comparators in superconducting flash A/D converters and in parallel converters of the type described in [1, 2]. Although the sampling rates of these converters are 1-5 GS/s, the analog bandwidth for an N-bit converter is greatly limited by two factors: distortion of the SQUID characteristics due to the dynamics of the SQUID loop when a flux quantum is added or subtracted, and the change in input signal during the long aperture time in which a comparison is made. One way to minimize the aperture time is to add additional SQUIDs with positive feedback to produce a latching operation when the first SQUID starts to switch. This technique has produced some increase in analog bandwidth [52-55].

A faster comparator can also be built using a one-junction SQUID [56-58] whose circuit and operational characteristics are shown in figure 29. Some additional components are needed to sample the polarity of I_J. Based on simulations, a sampling rate of more than 20 GS/s has been predicted. The analog bandwidth should also be high.
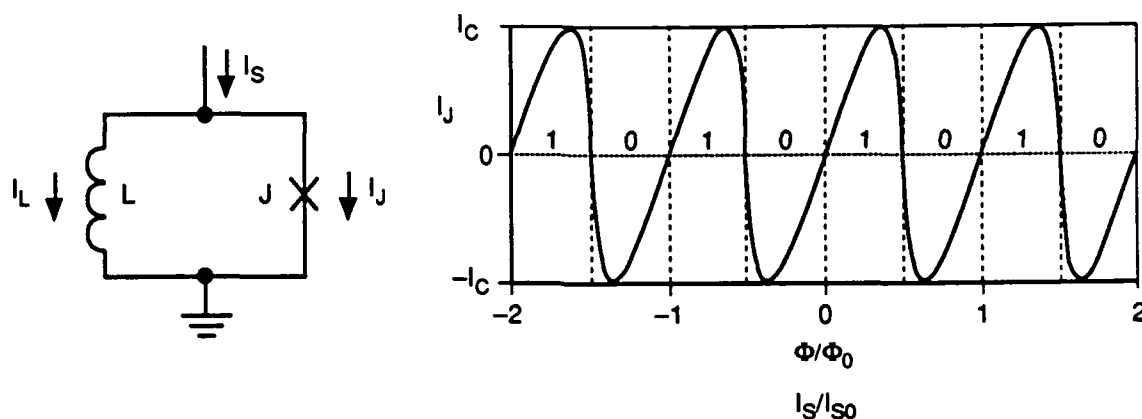

Figure 29. One-Junction SQUID Circuit and Operational Characteristics

3.3.2 Track-and-Hold Circuit

Only one superconducting T/H circuit has been reported in the literature [59]. This experimental device had a bandwidth of 1.2 GHz and a dynamic range of 25 dB. The authors predict that an optimized circuit could achieve a 4 GHz bandwidth and a 35 dB dynamic range. The dynamic range is limited by the small leakage current when the junction is in the open state and by quantization of the flux. The switching time was not measured, but it should be consistent with the bandwidth.

3.3.3 Amplifiers

Josephson Junction devices are basically two-state devices and are generally not suitable for analog applications. No superconducting transistor or operational amplifier with wideband

gain and high input impedance exists [60, 61]. A few narrowband amplifiers have been reported. Recent efforts have concentrated primarily on vortex flow transistors (VFTs) which are also called flux flow transistors (FFTs) [62-64]. These devices are current-controlled voltage sources. Another type of amplifier is a current-controlled current source (called a super-CIT) [64, 65]. Both of these amplifier types can be incorporated in distributed amplifier configurations to produce wideband responses with some gain [64, 65]. Amplifier linearity has not been determined experimentally.

3.3.4 Digital Logic

The pioneering work on developing digital logic circuits has been done by the Japanese, specifically by Fujitsu, Hitachi, Electrotechnical Laboratory, and NEC. Their emphasis has been on developing the circuits needed to build a superconducting computer. Many different configurations for the basic AND and OR circuits have been investigated without any real standard emerging. Memory has been especially difficult to implement. References [66-69] provide overviews of the work in this area. The most advanced superconducting computer chip is the 8-bit Fujitsu processor with the following characteristics [70]:

Clock Rate	1 GHz
ALU	16 Functions, 13 Bits
Multiplier	8-Bit x 8-Bit
RAM	2 16-Word x 8-Bit
Instruction ROM	64-Word x 24-Bit
Coefficient ROM	16-Word x 8-Bit
Chip Size	5mm x 5 mm
Number of Gates	6,300
Power	12 mW

Recent work on digital logic circuits has been concentrated on single flux quantum (SFQ) circuits, especially counters and shift registers, which are faster than other types of logic.

Table 8 lists digital logic circuits that may be useful in implementing the digital functions in a superconducting $\Sigma\Delta$ A/D converter. All circuits use low-temperature niobium junctions. Mixing circuits with different technologies presents some problems.

Table 8. Superconducting Digital Logic Circuits

Circuit	Technology	Speed	Reference
8-Bit Multiplier	MVTL	<1000 ps	[70]
16-Bit Multiplier (Model)	MVTL	1100 ps	[71]
8-Bit SR	MVTL	430 ps	[72]
32-Bit SR (Simulation)	MVTL	33 ps	[73]
4-k Memory	MVTL	590 ps	[70]
Gate (AND, OR, NOT)	SFQ	30 ps	[74]
T FF	SFQ	8 ps	[75]
12-Bit Counter	?	50 ps	[3]
Shift Register	?	250 ps	[76]
4-Bit Mult., 8-Bit Add (Simulation)	?	330 ps	[77]

SECTION 4

SUPERCONDUCTING ΣΔ CONVERTER IMPLEMENTATION

The specifications for the superconducting A/D converter are 16-bit resolution and a corresponding signal-to-noise ratio approaching 98 dB in a 30 MHz band. The tentative output data rate has been set at 125 MHz. The first matters to be settled are the modulator order and the sampling rate. The sampling rate should equal the output data rate multiplied by some power of two for ease of implementation. Considering the fact that the SNRs of actual ΣΔ converters are much lower than their theoretical SNRs, we should design the converter for a theoretical SNR of about 110 dB. Using the curves in figure 7, two possible choices are a second-order modulator with a sampling rate of 16 GHz (R = 267) or a third-order modulator with a sampling rate of 4 GHz (R = 67). The next step is choosing a ΣΔ modulator from those listed in table 7. The problems of overload and stability can be avoided by using a cascade architecture. The potential problem of gain matching between stages must be checked. The final choice between two or three stages depends upon the operating speeds of (1) the analog ΣΔ modulator and (2) the digital logic in the modulator and in the first stage of the digital filter. These digital circuits must operate at the ΣΔ modulator sampling rate. The following subsections discuss possible implementations of the ΣΔ modulator and digital filter using superconducting circuits.

4.1 ANALOG MODULATOR

4.1.1 Integrator

The integrator, especially the integrator in the first stage, has proven to be the most critical circuit in ΣΔ modulators. In semiconductor technology, an operational amplifier with a feedback capacitor is used as an integrator. This type of circuit cannot be built in superconducting materials because op amps do not exist. In addition, the low-impedances of all superconducting devices would result in rapid discharge of the capacitor.

An alternative is to implement the integrator as a summer and a delay using a digital approach as shown in figure 5. The analog delay can be implemented as a track-and-hold

circuit that is clocked at the sampling rate. The superconducting T/H circuit described in section 3.3.2 might be suitable, but the effect of its poor dynamic range needs further evaluation. The effect of T/H leakage current is to produce a dead spot in the transfer curve. This problem can be handled by biasing the circuit in the linear region. The effect of T/H flux quantization is to add quantization noise at the T/H output. For the cascade modulator shown in figure 10, the term $\varepsilon_{i,n-1}$ must be added to $s_{i,n-1}$ in equations (53), (54), and (56). Then equation (55) becomes

$$q_{i,n} = x_{i,n} + e_{i,n} - e_{i,n-1} + \varepsilon_{i,n} \tag{87}$$

Equation (56) remains the same, but the output of a two-stage modulator in equation (61) becomes

$$y_{n-3} = x_{1,n-3} + e_{2,n-3} - 2e_{2,n-4} + e_{2,n-5} + \varepsilon_{1,n-3} + \varepsilon_{2,n-3} - \varepsilon_{2,n-4} \tag{88}$$

Thus the T/H quantization noise in the first stage appears at the modulator output as though it were added directly to the input. The T/H quantization noise in the second stage is given first-order shaping so that its effect is not as important as that for the first stage. The first-stage T/H quantization noise is uniformly distributed between $\pm f_s/2$. Within the baseband, this noise is reduced by the oversampling ratio $R = f_s/2B$. For two stages and $R = 267$, the noise is reduced by 24 dB. For three stages and $R = 67$, the noise is reduced by 18 dB. If the quantization noise of the T/H circuit in section 3.3.2 is 35 dB below the signal, the $\Sigma\Delta$ modulator output SNR would be 59 dB for the two-stage circuit and 53 dB for the three-stage circuit. Therefore, the T/H quantization noise would allow only nine- or ten-bit accuracy. The only way to reduce the T/H flux quantization noise is to increase the inductance. However, the necessary large increase in inductance would make the circuit too slow. Therefore, a T/H circuit cannot be used as a delay in implementing the integrator.

A transmission line can be used to provide an analog delay. Superconducting transmission lines are fabricated routinely. The problem with a transmission line is that its fixed length is suitable for only one sampling rate. In addition, a very important question

exists about the required delay tolerance. This must be determined by simulation. If the delay tolerance is critical, a method for adjusting the delay has been proposed in [78], but experimental devices did not perform as expected.

4.1.2 Amplifier and Analog Loop

The actual analog modulator circuit for each stage in the cascade $\Sigma\Delta$ modulator is shown in figure 30. (This figure is a reconfiguration of one stage in figure 10.) The combiners and splitters can be fabricated using stripline techniques. However, the 3 dB loss in each combiner or splitter necessitates the addition of an amplifier to provide unity gain around the loop. Development of a suitable amplifier is a major concern. The superconducting amplifiers discussed in section 3.3.3 are possibilities when they are incorporated in a distributed amplifier. A major concern is amplifier gain accuracy and stability In section 2.1.1.2, the importance of unity loop gain was demonstrated by inserting an amplifier with a gain ot $(1 - \delta)$ in the loop. The modulator output in equation (23) then contained an extra term δe_{n-1} representing unshaped noise which would also appear at the output of the entire cascade modulator. When the 18 dB or 24 dB reduction in noise due to oversampling is taken into account, the maximum allowable value for δ is -80 dB for a three-stage modulator or -74 dB for a two-stage modulator. There is no hope of fabricating the modulator loop with the gain controlled so closely. A means for finely adjusting the gain is needed. Because the circuit will be operated at 4.2K, a mechanical gain control is not practical. One possibility is to use one or more field-effect transistors as voltage-controlled resistors in a variable attenuator. Experimental tests are needed to verify the operation of such an attenuator. The loop gain must be extremely close to unity at all signal levels. An equivalent requirement is that the amplifier and other components in the loop must be extremely linear. The performance of the superconducting amplifiers discussed in section 3.3.3 will not be known for probably a year or more.

As discussed in section 2.1.3.2, the splitter output to the succeeding stage must be almost the same as the splitter output to the input combiner. For a difference in splitter outputs of ε, the modulator output error signal is shaped quantization noise equal to $\varepsilon(e_{1,n-3} - e_{1,n-4})$. Because the noise is shaped, it is attenuated according to the single-loop curve in figure 7.
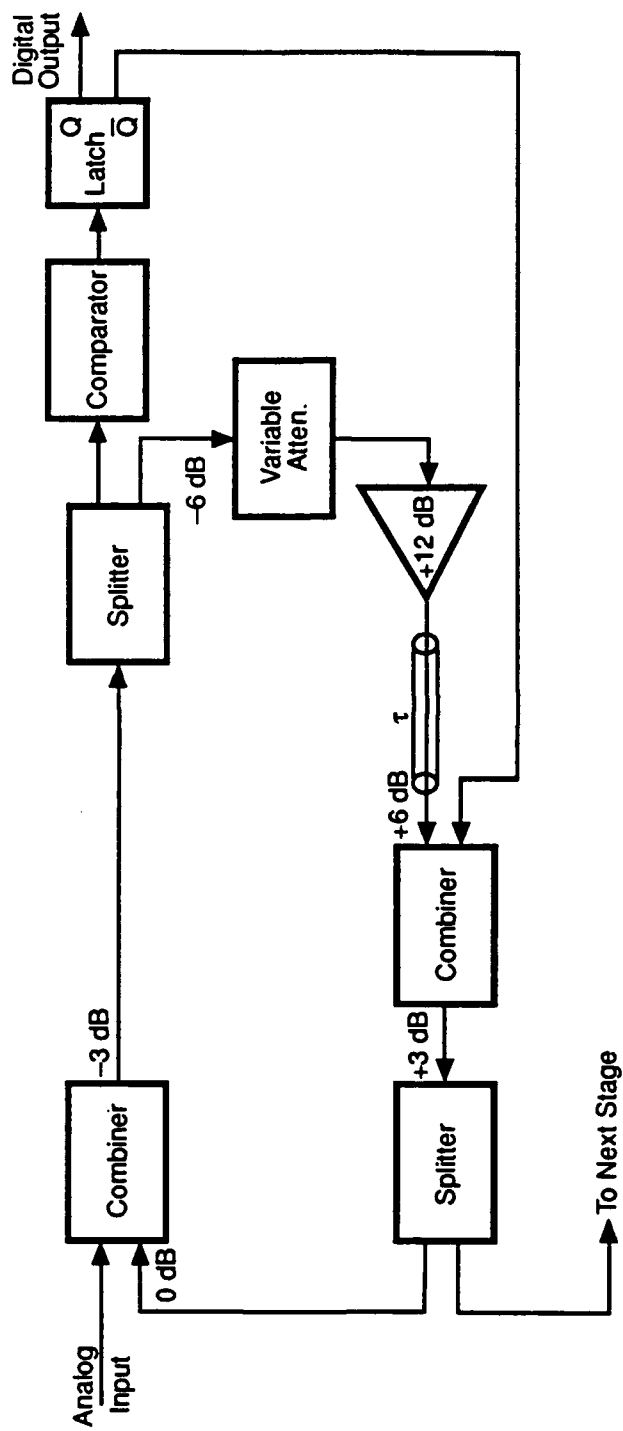
Figure 30. Analog ΣΔ Modulator Stage

The required minimum values of ε are then about -29 dB for a second-order modulator and -47 dB for a third-order modulator in order to achieve an SNR of 98 dB. Thus the splitter must be carefully designed, but its tolerances should not be a major problem. Minor gain adjustments could be made if necessary.

Development of the analog modulator loop depends on each component in the circuit and also on compatible signal and impedance levels around the loop. If the amplifier is a current-controlled current source, the circuit is a current loop and the latch output must also be a current. If the amplifier is a current-controlled voltage source, the latch output should also be a voltage. Then somewhere in the loop voltage must be converted back to current. Thus development of the modulator loop cannot begin until an amplifier with acceptable gain, linearity, impedance levels, and other characteristics is developed.

With regard to the comparator, the one-junction SQUID discussed in section 3.3.1 is recommended because of its speed. The signal current, I_s, should be set so that its maximum values are less than $\pm I_{so}/2$. Then the polarity of I_J must be sampled and latched.

4.2 DIGITAL LOGIC

Recent efforts to develop single flux quantum (SFQ) digital logic circuits should result in many new high-speed circuits within the next few years. The preliminary designs of the modulator digital logic and the first digital filter stage emphasize simple circuits which presently exist or are expected to be developed within the next few years.

As mentioned in section 2.1.3.1 for an M-stage modulator with the quantizer outputs normalized to ± 1, the $\Sigma\Delta$ modulator output levels are $\pm 1, \pm 3, \pm 5 \cdots \pm 2^M - 1$. Thus the number of output levels is 2^M, but $2^M + 1$ bits are needed to represent the output in twos-complement notation. Changing this notation to eliminate the extra bit can reduce the hardware or simplify the logic in the first stage of the digital filter. This may be important because this stage must operate at the sampling rate. Consider a cascade two-stage

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modulator with the output of the first quantizer designated as A_n and the output of the second quantizer as B_n at time n. The $\Sigma\Delta$ modulator output is

$$C_n = A_{n-1} + B_n + B_{n-1} \tag{89}$$

Table 9 shows the required truth table for quantizer outputs of ± 1 and the actual truth table for quantizer outputs of zero and one using the logic shown in figure 31. It is seen that the set $\{-3, -1, +1, +3\}$ is transformed to the set $\{0, 1, 2, 3\}$. Adjustments for the DC offset must be made later.

Table 9. Two-Stage Cascade $\Sigma\Delta$ Modulator Truth Tables

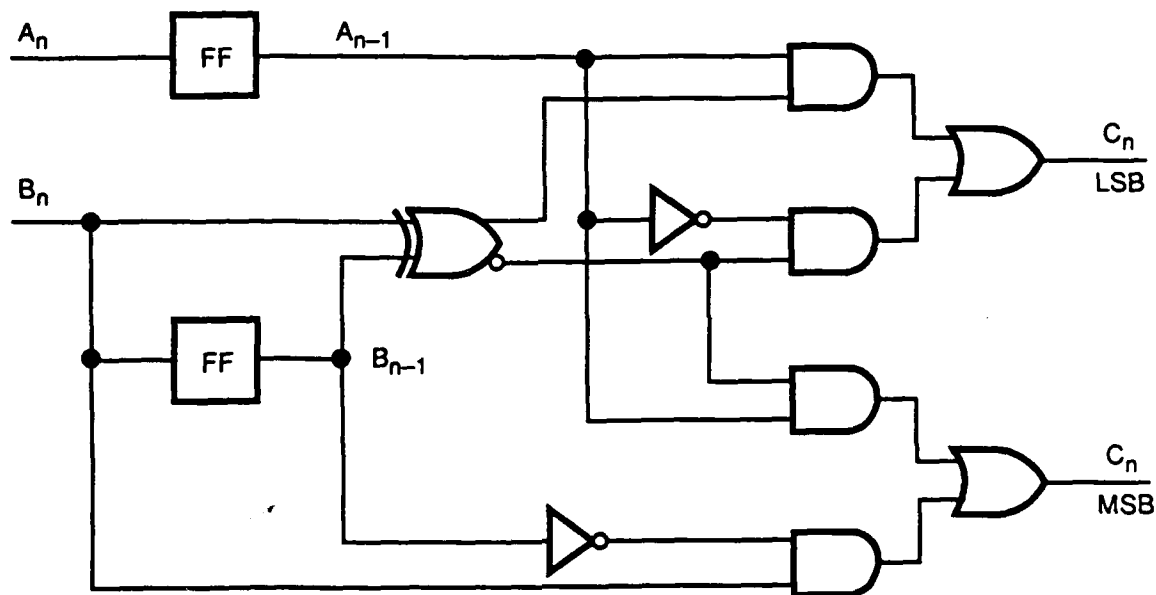| Required Truth Table				Implemented Truth Table					
A_{n-1}	B_n	B_{n-1}	C_n	A_{n-1}	B_n	B_{n-1}	C_n MSB	C_n LSB	C_n
-1	-1	+1	-3	0	0	1	0	0	0
-1	-1	-1	-1	0	0	0	0	1	1
-1	+1	+1	-1	0	1	1	0	1	1
+1	-1	+1	-1	1	0	1	0	1	1
-1	+1	-1	+1	0	1	0	1	0	2
+1	-1	-1	+1	1	0	0	1	0	2
+1	+1	+1	+1	1	1	1	1	0	2
+1	+1	-1	+3	1	1	0	1	1	3

Figure 31. Two-Stage Cascade $\Sigma\Delta$ Modulator Digital Logic

The decision to use a two- or three-stage cascade $\Sigma\Delta$ modulator means that the modulator output will be two- or three-bit words. Another consequence of deciding on two or three modulator stages is the requirement that the first filter stage have a $sinc^3$ or $sinc^4$ response or something similar. Several alternatives for implementing this first filter stage, which operates at f_s, are discussed in the following paragraphs. Subsequent filter stages should be easier to design because of their lower data rates.

If a $sinc^3$ or $sinc^4$ filter is implemented as an FIR filter as shown in figure 14, multipliers with about eight-bit coefficients will probably be needed. Much hardware will be required because the filter must be very long. One way to eliminate the multipliers and greatly reduce the hardware required is to use an IIR-FIR decimating $sinc^k$ filter as shown in figure 20, or an FIR decimating $sinc^k$ filter as shown in figure 21. If fast superconducting memories are available, the filter structure shown in figure 32 should be considered. This is an FIR filter in which each ROM produces a precalculated output equal to
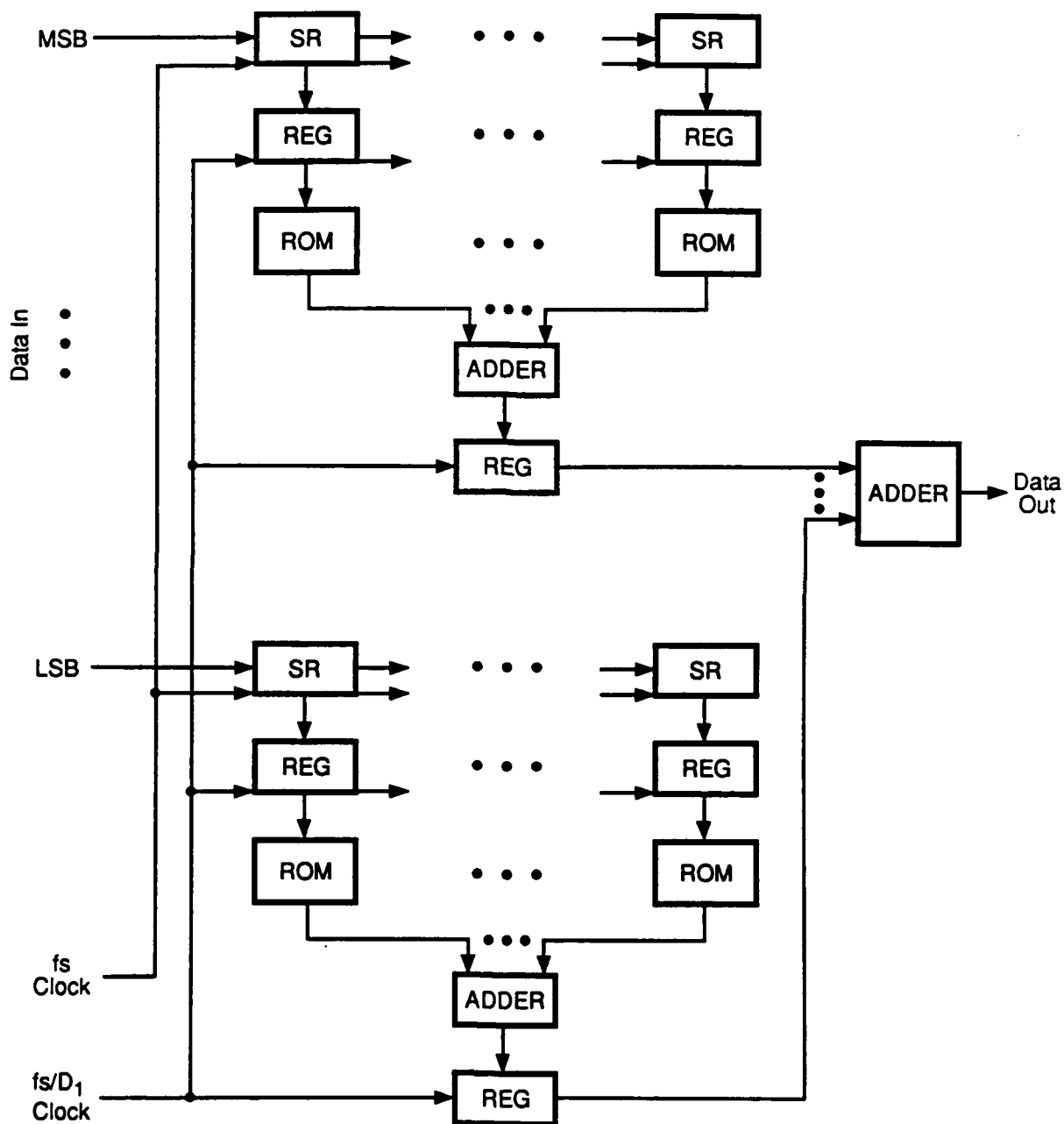
Figure 32. Digital Filter with ROMs

$$y = \sum_{i=n}^{n+N-1} a_i x_i \qquad\qquad (90)$$

for the particular group of N bits which form its input address. Thus this architecture does not require hardware multipliers. Only the shift registers operate at the sampling rate. All of the other circuits operate at the decimated output data rate of f_s/D_1. One advantage of this filter is that its response is not restricted to a sinc^k response. In addition, the use of precalculated outputs conveniently handles the data DC offset problem.

SECTION 5

SUMMARY, CONCLUSIONS, AND FUTURE PLANS

The objective of Project 91080 is to develop a superconducting A/D converter with 16-bit resolution and a sampling rate of 125 MS/s. Previous investigations of superconducting A/D converters have been unsuccessful in identifying a suitable architecture. This report investigates sigma-delta ($\Sigma\Delta$) converters to determine the feasibility of a superconducting $\Sigma\Delta$ converter and to fulfill a requirement of Project 7920.

The principle of $\Sigma\Delta$ converters is to trade sampling rate for resolution. A $\Sigma\Delta$ modulator puts out only a few bits at a very high rate. Subsequent digital filtering increases the resolution and decreases the data rate. One of the characteristics of $\Sigma\Delta$ modulators is noise shaping which moves the noise above the baseband where it can be filtered out. The theoretical performance of an Mth order $\Sigma\Delta$ modulator has been determined. The sources of performance degradation in the two types of modulators, classical and cascade, have been discussed. Performance of actual $\Sigma\Delta$ modulators has been found to be much worse than their theoretical performance. The typical $\Sigma\Delta$ digital filter is a decimating filter with two or more stages. A first-stage filter with a $sinc^k$ response is commonly used to counteract the shaped noise out of the modulator. Other filter stages may have equiripple or similar responses. Because of the high modulator sampling rate, special $sinc^k$ filter structures have been devised to simplify the hardware.

A brief review of superconductivity and superconducting Josephson junction (JJ) circuits has been presented. The main advantage of JJ circuits is their high speed which is the reason for trying to use them in a high-speed, high-resolution A/D converter. The main problem in using JJ circuits in this application is the dearth of analog components and circuits, especially transistors and amplifiers. Nevertheless, a superconducting $\Sigma\Delta$ modulator circuit which may work has been proposed. Because this $\Sigma\Delta$ modulator uses a transmission line to provide a delay equal to the sampling clock period, the sampling frequency cannot be varied. Two matters must be resolved before pursuing circuit development any further. The first is the effect of the transmission line delay tolerance on modulator performance. Simulation of

the $\Sigma\Delta$ modulator consisting of both analog and digital components is needed. The second matter is development of a suitable distributed amplifier by researchers at the University of Wisconsin-Madison. This amplifier must be very linear, and its signal and impedance levels must allow interfacing in the $\Sigma\Delta$ modulator loop. If it is determined in FY91 that both of these matters can be resolved favorably, two other issues require a closer look. First, a means of finely adjusting the gain around the modulator loop must be verified. Secondly, the availability of sufficient digital logic circuits for the modulator and digital filter is critical. Researchers at the University of California-Berkeley have offered to assist us in this area.

In conclusion, the development of a superconducting $\Sigma\Delta$ A/D converter may be possible, but several potential problems require further study. In FY91 we will determine the effect of delay line tolerance on performance, and monitor the amplifier development work being done at the University of Wisconsin-Madison. Depending on the results of these studies, we will decide whether or not to pursue the development of this A/D converter.

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Technical Report 10

VHDL SIMULATION STUDY OF SUPERCONDUCTING ΣΔ MODULATORS

by

L. A. Crook

ABSTRACT

The VHSIC Hardware Description Language (VHDL) was used to model the performance of a superconducting sigma-delta (ΣΔ) modulator. The purpose of the investigation was to determine the sensitivity of the modulator to variations in the delay line length of the integrator component. The output of the VHDL model was subsequently analyzed using the Matlab signal processing capabilities. It was found that the ΣΔ modulator requires a tighter transmission line tolerance than the 0.1 percent available with current technology. A 0.1 percent transmission line tolerance results in unacceptable signal quantization noise for a 16-bit analog-to-digital converter.

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SECTION 1

INTRODUCTION

Sigma-delta ($\Sigma\Delta$) modulators are used to enhance the performance of semiconducting analog-to-digital (A/D) converters. During the past year the feasibility of using the $\Sigma\Delta$ modulator structure with superconducting analog-to-digital converters has been studied. This paper reports on the simulation of the performance of a superconducting $\Sigma\Delta$ modulator using the VHSIC Hardware Description Language (VHDL).

Figure 1 shows the basic components of a $\Sigma\Delta$ A/D converter. The $\Sigma\Delta$ modulator samples the analog input at a very high rate and produces a low-precision digital output, typically one bit. The quantization noise at the output of the modulator is high due to the low precision; however, noise shaping caused by the high oversampling ratio pushes most of the noise power to frequencies above the signal band. Therefore, the $\Sigma\Delta$ modulator can have a high signal-to-noise ratio (SNR) within the signal band [1]. The multi-stage architecture of the $\Sigma\Delta$ digital filter consists of a special decimating filter to convert the oversampled b-bit words to normal sampled n-bit, higher precision words and a lowpass filter to attenuate the out-of-band quantization noise. While b is a small number, frequently 1, n may be as large as 16 and in some cases larger. The result of this structure is a high-speed, high-resolution $\Sigma\Delta$ A/D converter.
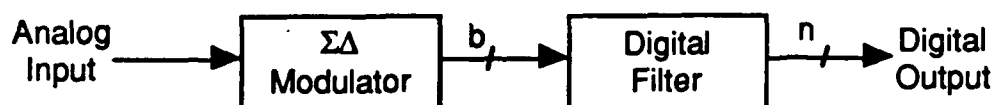
Analog Input → $\Sigma\Delta$ Modulator → b → Digital Filter → n → Digital Output

Figure 1. Sigma-Delta A/D Converter

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There are ΣΔ modulator architectures in use in A/D converters. All are variations of the basic one-loop, ΣΔ modulator shown in figure 2. Prior research has shown that the integrator is a critical component in the modulator and that its implementation in superconducting technology is not straightforward. In semiconductor technology the implementation of the integrator would use an operational amplifier, which cannot be easily implemented in superconducting technology. Therefore, it was decided to create an integrator with a summer and a delay of one sampling period. Furthermore, after ruling out other options, a superconducting transmission line was chosen to implement the integrator delay [1].
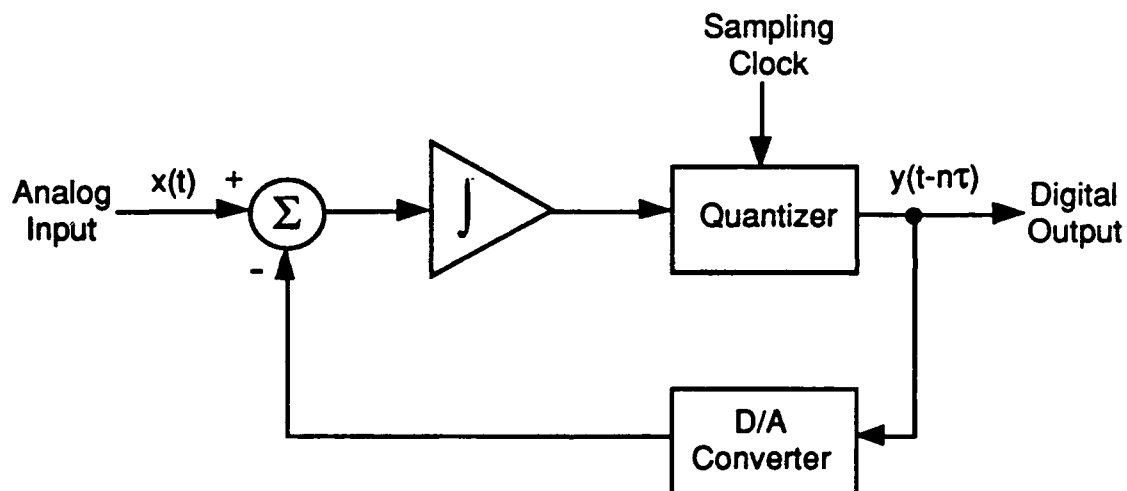

Figure 2. Basic Sigma-Delta Modulator

This paper reports the findings of a study performed to investigate the delay line tolerance, specifically, the effect that a variation in the analog delay would have on the modulator's performance. The modulator was modeled and simulated in VHDL. A sampled data representation of the modulator, such as the one shown in figure 3, was modeled behaviorally in VHDL, simulated, and the data collected and analyzed for its SNR and relative

2

noise power above the baseband. The first simulation performed was that of the nominal case, with all delays equal to one sampling period. The results for SNR and relative noise power for the nominal case were compared to the theoretical findings of the performance analysis in [1].
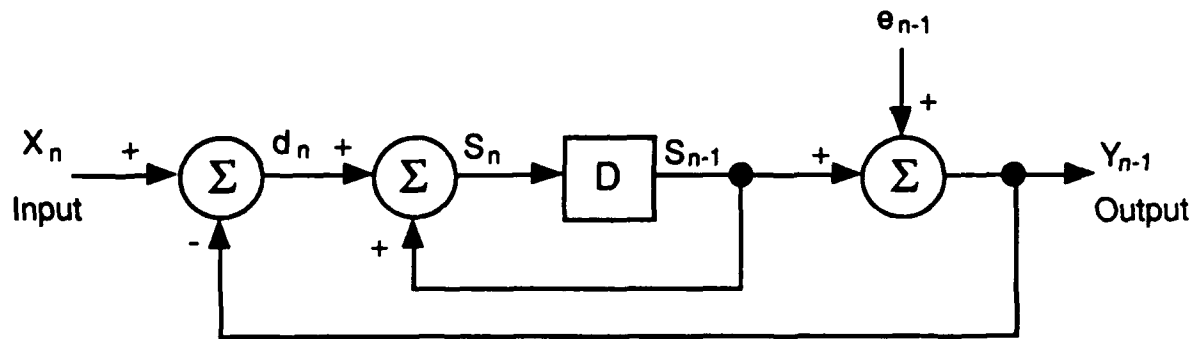

Figure 3. Sampled Data Representation of a Basic Sigma-Delta Modulator

SECTION 2

SIMULATION OF THE SIGMA-DELTA MODULATOR

2.1 VHDL REPRESENTATION OF THE SIGMA-DELTA MODULATOR

The specific modulator investigated in this study was a three-stage, cascade $\Sigma\Delta$ modulator, shown in figure 4, comprised of three of the basic single-loop modulators in figure 2. In a cascade modulator, the input to any stage after the first is the quantization error from the previous stage. So the quantization error is in turn quantized.

The mixed analog and digital circuit in figure 4 is composed of instances of just five basic components, a quantizer, a delay, a two-input summer, a three-input summer, and a subtractor (denoted "differ"). These components were modeled behaviorally in VHDL. The modulator model contained declarations for its five subcomponents, and for every appearance of the delay, for example, created a new delay instance with a unique name and a list of signals to associate with the port signals of the subcomponent. The VHDL code for the components and the modulator appears in the appendix.

The delay time for each delay instance was controlled individually by its generic parameter *delay_time*, which defaulted to 10 nanoseconds (ns), one sampling period for a modulator with a 100 MHz sampling frequency. The six delays in the digital portion of the circuit were always set to the default value. After a simulation of the nominal case with all delays set to 10 ns, subsequent simulations were performed with 1.0 percent and 0.1 percent deviations from the default on each of the delays D1, D2, and D3 individually. For any simulation, at most only one of these delays varied from the default value.
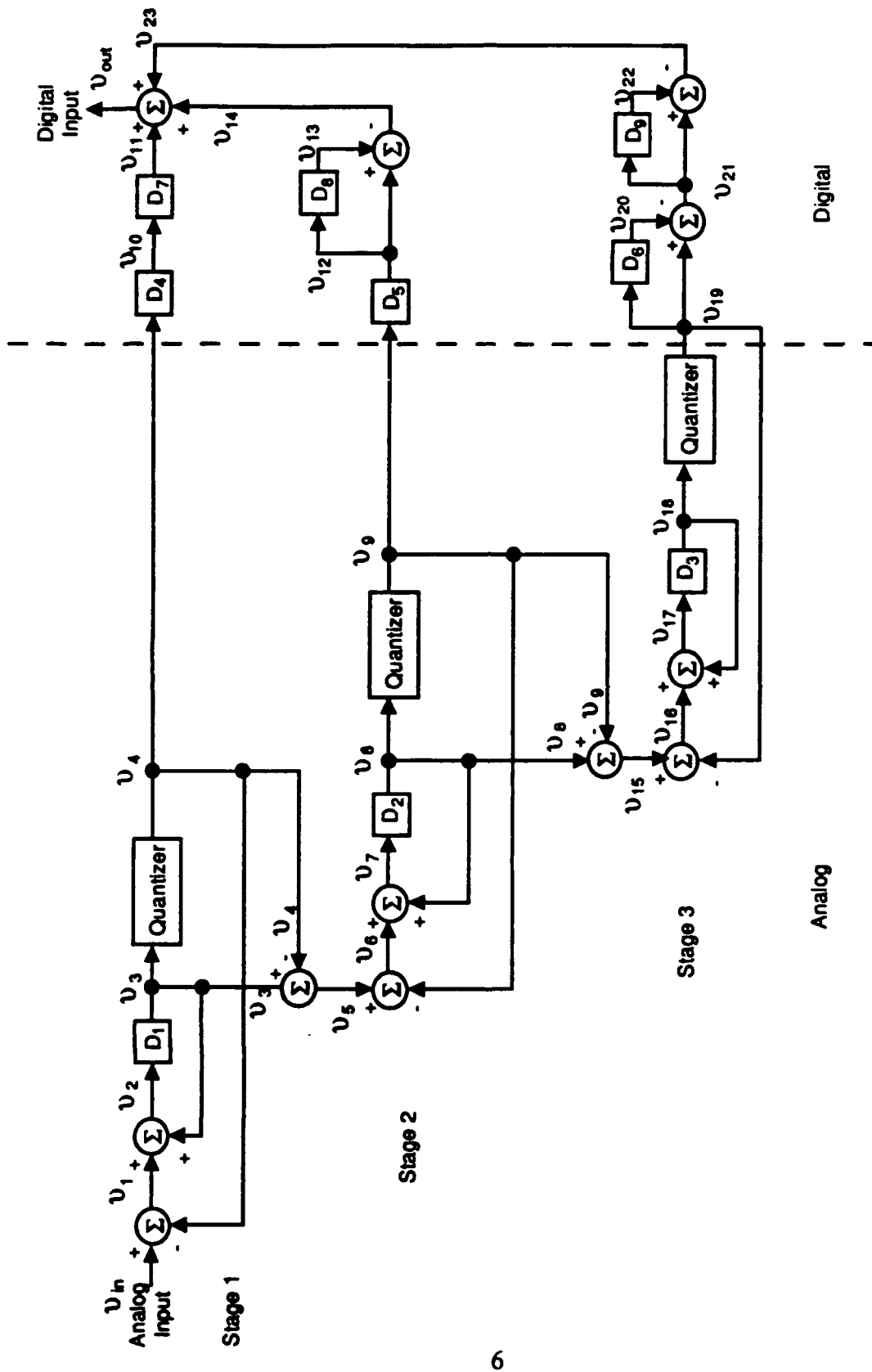
5

Figure 4. Sampled Data Representation of a Three-Stage, Cascade Sigma-Delta Modulator

VHDL does not offer a sine function to be used in analog applications. The analog input for the first stage of the modulator was simulated using Matlab[1] to sample a 5/5.12 MHz sine wave with a sampling frequency of 100 MHz. This data was placed in a file to be read by a file input/output process in the VHDL testbench to provide the input stimulus for the modulator model. The digital output of the simulated modulator was collected in a second file for later analysis.

2.2 MODELING AND SIMULATION ISSUES

A modeling issue that arose during this study concerned the most accurate way to represent the delay of the modulator. VHDL supports two time delay modes, inertial and transport delay. Initially, the modulator delay was modeled as an inertial delay, the default delay mode for a signal assignment statement. However, it was found that the modulator, specifically, the delay model, was not performing as expected. In VHDL a signal assignment statement containing an "after" clause is executed by updating a queue of scheduled transactions for the signal. In an inertial assignment, a new transaction scheduled to take place after a transaction already in the queue, causes the older transaction to be discarded [2]. In simulations of the modulator modeled with inertial delays, transactions that were scheduled to take place on the output signals of the delay components did not occur. They were cancelled each time a new analog input sample stimulated the modulator and the delay component input. An event has to be of a longer duration than the specified inertial delay in order to be propagated. This is analogous to a filter in which a short pulse is absorbed by an RC network with a longer time constant.

An alternate delay mode provided in VHDL is the transport delay. Using this delay mode, any event, regardless of duration, is simply delayed by the specifed transport delay. In contrast to the inertial delay case, a transport signal assignment will cause the new transaction, scheduled to occur after one already waiting in the queue, to be simply added at the end of the

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[1] Matlab is a mathematics analysis package run on SUN computers. It is available from the MathWorks, Natick, MA.

queue [2]. The transmission line delay of the $\Sigma\Delta$ modulator is properly modeled as a transport delay. Once the effect was understood and the delay mode was changed, the component operated as expected.

Another important issue raised concerned the choice of a simulation timebase. The Synopsys toolset, which was used in this study, requires the user to specify the timebase. Permitted values range from a femtosecond to a second. The Synopsys VHDL simulator does not recognize any fractions of the simulator timebase. Therefore, a simulation with a specified timebase of a nanosecond would treat a 9.9 ns delay in a signal assignment statement as a 9 ns delay. For this reason, a simulation timebase of a picosecond was used in this study. An unfortunate result of decreasing the timebase from a nanosecond to a picosecond was the much greater amount of time required to run a simulation of the same length to completion.

The simulations with 1.0 percent delay variations took at most 36 hours to complete. However, the simulation of the case with D1 = 10.01 ns took approximately 12 days to run to completion. Therefore, further simulations with a 0.1 percent variation in the delay were not pursued.

SECTION 3

SIMULATED MODULATOR OUTPUT

The output of each modulator simulation was a sequence of 64K data points. This sequence could not be studied directly. It was necessary to investigate the frequency components comprising the output data. Matlab software was used to calculate and plot the power spectral density of the modulator output. Of particular interest was the signal power at the input frequency and above, as the high oversampling ratio of the $\Sigma\Delta$ modulator is expected to push the quantization noise to frequencies above the signal band.

Figure 5 contains the results of the power spectral density calculations for the simulation of the nominal case and the cases of a 1.0 percent delay increase in each of the three stages. The results of the simulations with a 1.0 percent decrease in the three analog delays are shown in figure 6. The power spectral density of the modulator output with a 0.1 percent increase in the first stage delay is shown in figure 7.
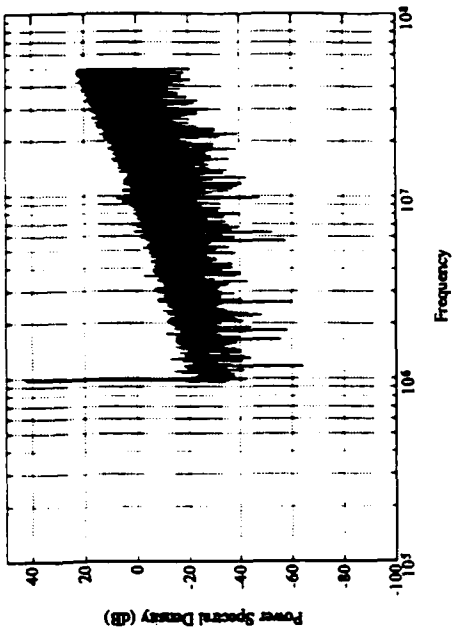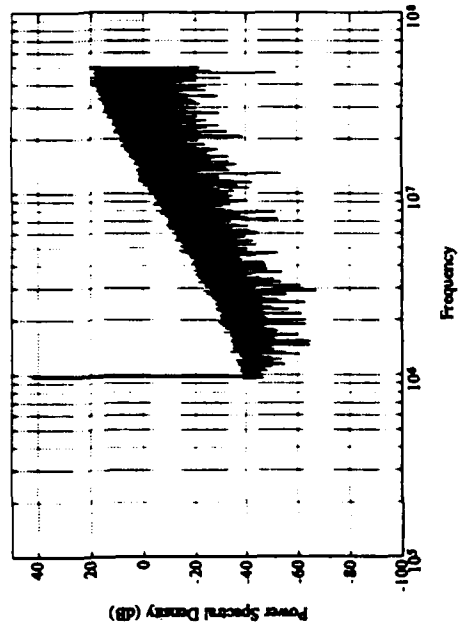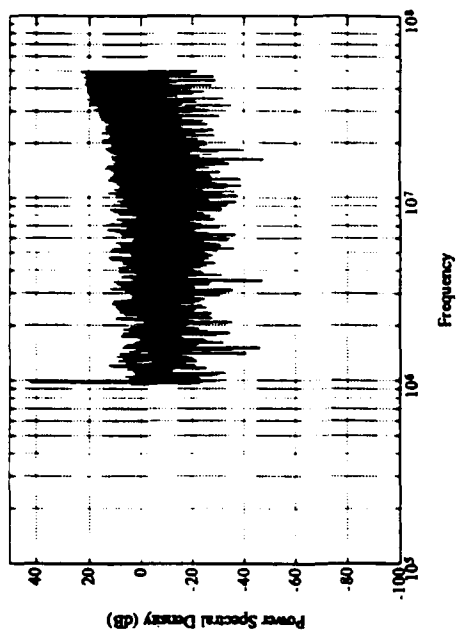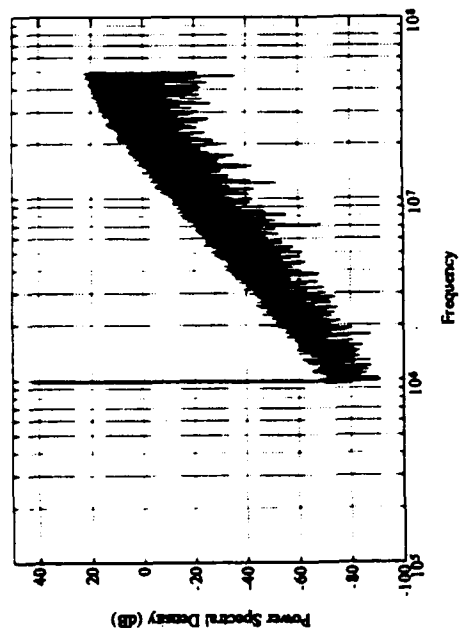
Figure 5. Power Spectral Density of Modulator Output
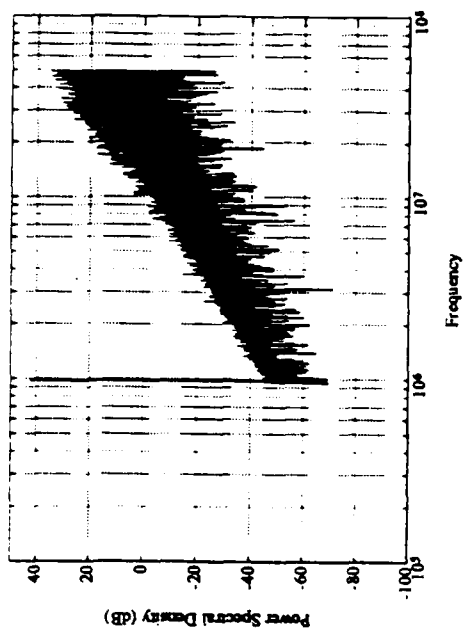a) Nominal Delays b) D1 = 10.1 ns c) D2 = 10.1 ns d) D3 = 10.1 ns

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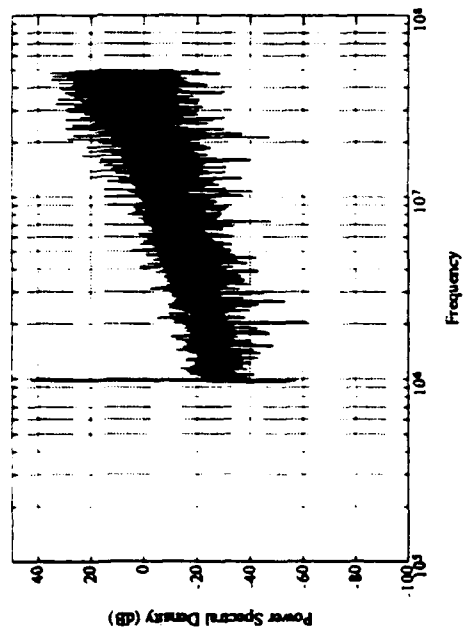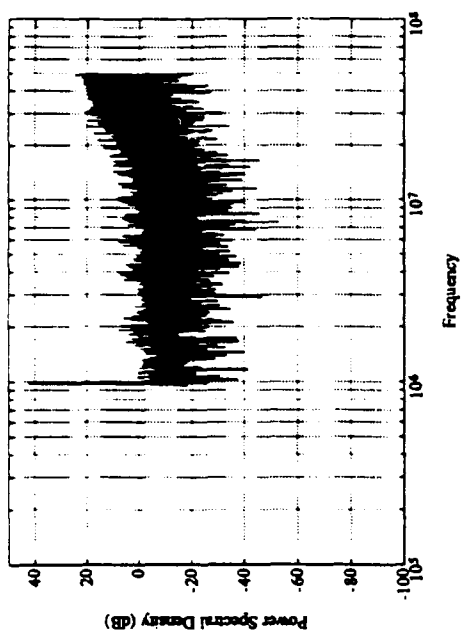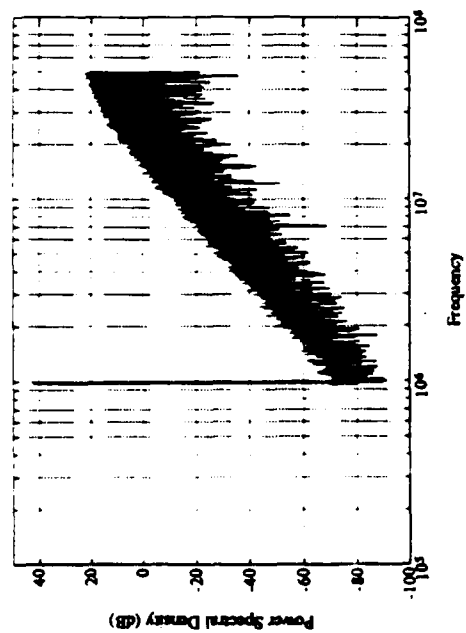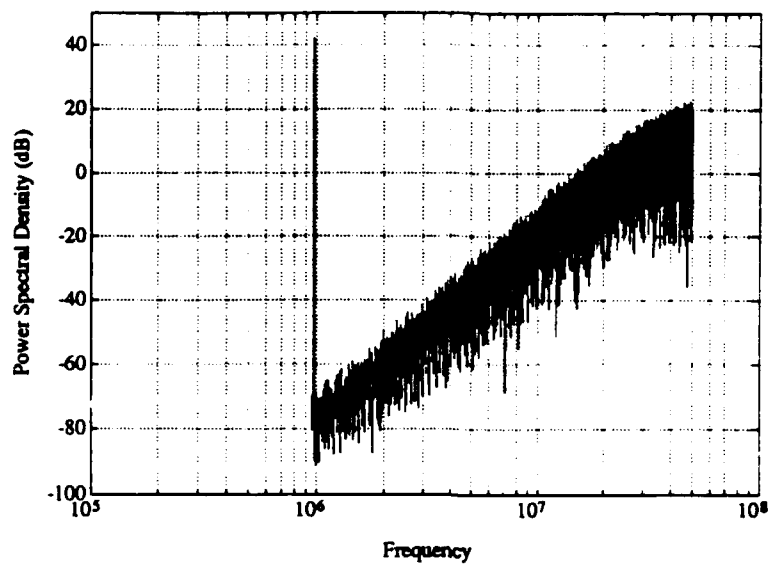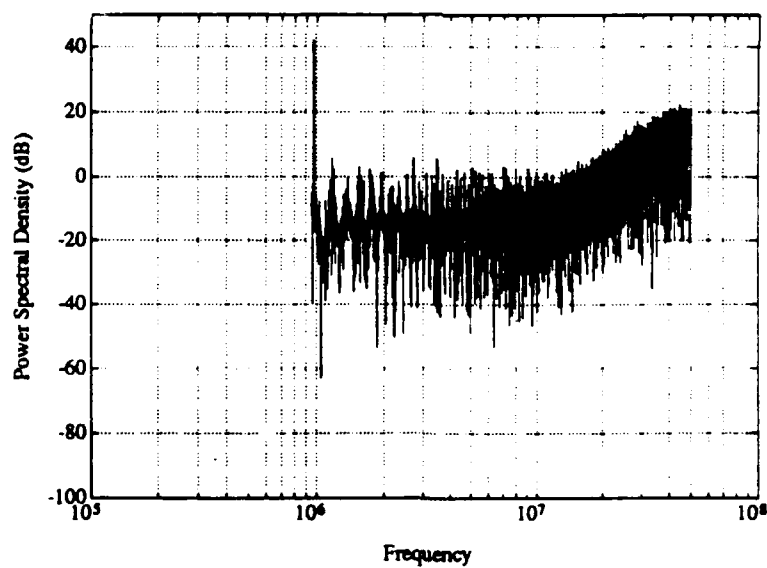Figure 6. Power Spectral Density of Modulator Output
a) Nominal Delays b) D1 = 9.9 ns c) D2 = 9.9 ns d) D3 = 9.9 ns

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(a)

(b)

Figure 7. Power Spectral Density of Modulator Output a) Nominal Delays b) D1 = 10.01 ns

SECTION 4

DISCUSSION OF RESULTS

In the $\Sigma\Delta$ modulator performance analysis of [1], equations were derived for the theoretical SNR and the noise power spectral density. For a third-order cascade modulator with a sampling frequency of 100 MHz and an oversampling ratio of 51.2, the theoretical SNR was calculated to be approximately 100 decibels (dB). The relative noise power of the theoretical modulator was found to increase 18 dB per octave, or 60 dB per decade. Actual results for the simulated modulator are comparable, as seen in figure 5(a). The output has a SNR of approximately 115 dB. In addition, the simulated modulator has achieved the noise shaping as predicted, with a slope of 60 dB per decade and no noise shaping beyond one-sixth the sampling frequency, where the noise power is 0 dB. These findings for the nominal case validate the VHDL simulation of the modulator.

The results of further simulations reveal considerable degradation in the performance of the modulator when the critical transmission delay is shortened or lengthened even slightly. The power spectral density plots of figure 5 illustrate this for a 1.0 percent increase in the delay. When the transmission delay in the first stage was increased to 10.1 ns, the SNR dropped to 47 dB. Noise shaping was nonexistent. A 0.1 ns increase in the stage 2 delay yielded a 67 dB SNR and noise shaping of about 23 dB per octave. The same increase in the third stage delay resulted in a SNR of 84 dB and 40 dB per octave noise shaping.

Results for a 1.0 percent delay decrease were similar. When the transmission delay in stage 1 was decreased to 9.9 ns, the SNR was 52 dB and there was no noise shaping. A 1.0 percent decrease in the second stage delay yielded a SNR of 67 dB and noise shaping of 23 dB per decade. The same variation in the stage 3 delay led to a 92 dB SNR and 42 dB per decade noise shaping.

These findings reveal a relationship between the performance degradation of the modulator and the stage in which a transmission line deviates from its intended value. Clearly,

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the further from the first stage a delay variance is found, the less impaired is the modulator operation. With respect to noise shaping in particular, it appears that a deviation from the nominal delay in any stage negates the advantage of that stage and subsequent stages. Changing the delay in the first stage removed all noise shaping. A variation in the second stage led to the noise shaping predicted for a one-loop $\Sigma\Delta$ modulator, as if the second and third stages had not been present. A deviation in the third stage delay resulted in the noise shaping expected of a two-stage modulator.

It is obvious from these results that the $\Sigma\Delta$ modulator cannot tolerate a 1.0 percent variance in the transmission delay without being rendered useless. Indeed, a 0.1 percent deviation in the delay was also found to deteriorate the performance of the modulator. A 0.01 ns increase in the first stage delay yielded a SNR of 52 dB and little noise shaping. Clearly, the 0.1percent variance in the transmission delay is unacceptable.

SECTION 5

CONCLUSIONS

This effort has shown that it is possible to simulate the $\Sigma\Delta$ modulator with VHDL. In general, it is better to use a VHDL simulator that automatically adjusts its timebase, such as the Intermetrics Simulator.

A 0.1 percent transmission line tolerance, which is the tightest tolerance available with current microelectronics technology, cannot be used to implement a superconducting sigma-delta modulator based upon a direct conversion from semiconducting to superconducting components. The non-ideal time delay negates all advantage of the $\Sigma\Delta$ architecture. Other approaches to achieve the desired feedback are necessary.

LIST OF REFERENCES

1. Poole, M. A., November 1990, *Feasablility Study of a Superconducting Sigma-Delta Analog-to-Digital Converter*, WP-29107, The MITRE Corporation, Bedford, MA.

2. Lipsett, R., C. F. Schaefer, and C. Ussery, 1989, *VHDL: Hardware Description and Design* Norwell, MA: Kluwer Academic Publishers.

APPENDIX

VHDL MODELS OF COMPONENTS AND MODULATOR

```
entity summer2 is                                    -- 2-input summer entity declaration
    port ( v1, v2 : in     real   := 0.0 ;
           vout    : out    real   := 0.0 );
end summer2;

architecture behavior of summer2 is
begin
    process
    begin
        vout <= v1 + v2;
        wait on v1, v2;
    end process;
end behavior;


entity summer3 is                                    -- 3-input summer entity declaration
    port ( v1, v2, v3   : in     real   := 0.0 ;
           vout         : out    real   := 0.0 );
end summer3;

architecture behavior of summer3 is
begin
    process
    begin
        vout <= v1 + v2 + v3;
        wait on v1, v2, v3;
    end process;
end behavior;


entity differ is                                     -- subtractor entity declaration
    port ( v1, v2 : in     real   := 0.0 ;
           vout    : out    real   := 0.0 );
end differ;

architecture behavior of differ is
begin
    process
    begin
        vout <= v1 - v2;
        wait on v1, v2;
    end process;
end behavior;
```

```vhdl
entity time_delay is                                    -- transmission delay entity declaration
    generic ( delay_time : time := 10 ns );
    port ( vin  : in    real := 0.0 ;
           vout : out   real := 0.0 );
end time_delay;

architecture behavior of time_delay is
begin
    vout <= transport vin after delay_time;
end behavior;


entity quantizer is                                     -- 1-bit quantizer entity declaration
    port ( vin  : in    real := 0.0 ;
           vout : out   real := 0.0 );
end quantizer;

architecture behavior of quantizer is
begin
    process
    begin
        if vin >= 0.0 then vout <= 1.0;
          else vout <= -1.0;
        end if;
        wait on vin;
    end process;
end behavior;




use work.all;                                           -- identify library of analyzed components

entity modulator is                                     -- modulator entity declaration
    port ( vin  : in    real ;
           vout : out   real );
end modulator;

architecture structural of modulator is

    signal  v1, v2, v3, v4, v5, v6, v7, v8, v9,         -- modulator signals declaration
        v10, v11, v12, v13, v14, v15, v16,
        v17, v18, v19, v20, v21, v22, v23  : real := 0.0;
```

```vhdl
component summer2                          -- subcomponent declaration - summer2
    port ( v1, v2 : in    real;            --   with binding indication
           vout   : out   real );
end component;

for all : summer2 use entity work.summer2(behavior);

component summer3                          -- subcomponent declaration - summer3
    port ( v1, v2, v3  : in    real;       --   with binding indication
           vout        : out   real );
end component;

for all : summer3 use entity work.summer3(behavior);

component differ                           -- subcomponent declaration - differ
    port ( v1, v2 : in    real;            --   with binding indication
           vout   : out   real );
end component;

for all : differ use entity work.differ(behavior);

component time_delay                       -- subcomponent declaration - time_delay
    generic ( delay_time : time );         --   with binding indication
    port ( vin  : in    real;
           vout : out   real );
end component;

for all : time_delay use entity work.time_delay(behavior);

component quantizer                        -- subcomponent declaration - quantizer
    port ( vin  : in    real;              --   with binding indication
           vout : out   real );
end component;

for all : quantizer use entity work.quantizer(behavior);

begin                                      -- instantiations of subcomponents follow

-- Stage 1 - Analog portion

    DIF11 : differ
        port map ( vin, v4, v1 );

    SUM1 : summer2
        port map ( v1, v3, v2 );
```

```
    D1 : time_delay                          -- length of this delay varied for study
        generic map ( 10 ns );
        port map ( v2, v3 );

    QUAN1 : quantizer
        port map ( v3, v4);

    DIF12 : differ
        port map ( v3, v4, v5 );

-- Stage 1 - Digital portion

    D4 : time_delay
        generic map ( 10 ns );
        port map ( v4, v10 );

    D7 : time_delay
        generic map ( 10 ns );
        port map ( v10, v11 );

-- Stage 2 - Analog portion

    DIF21 : differ
        port map ( v5, v9, v6 );

    SUM2 : summer2
        port map ( v6, v8, v7 );

    D2 : time_delay                          -- length of this delay varied for study
        generic map ( 10 ns );
        port map ( v7, v8 );

    QUAN2 : quantizer
        port map ( v8, v9 );

    DIF22 : differ
        port map ( v12, v13, v14 );

-- Stage 2 - Digital portion

    D5 : time_delay
        generic map ( 10 ns );
        ort map ( v9, v12 );
```

```
      D8 : time_delay
         generic map ( 10 ns );
         port map ( v12, v13 );

      DIF23 : differ
         port map ( v8, v9, v15 );

 -- Stage 3 - Analog portion

      DIF31 : differ
         port map ( v15, v19, v16 );

      SUM3 : summer2
         port map ( v16, v18, v17 );

      D3 : time_delay                              -- length of this delay varied for study
         generic map ( 10 ns );
         port map ( v17, v18 );

      QUAN3 : quantizer
         port map ( v18, v19 );

 -- Stage 3 - Digital portion

      D6 : time_delay
         generic map ( 10 ns );
         port map ( v19, v20 );

      DIF32 : differ
         port map ( v19, v20, v21 );

      D9 : time_delay
         generic map ( 10 ns );
         port map ( v21, v22 );

      DIF33 : differ
         port map ( v21, v22, v23 );

 -- Digital Output

      SUMOUT : summer3
         port map ( v11, v14, v23, vout );

end structure;
```