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Final Report

to

Department of the Navy
Office of Naval Research
800 N. Quincy Street
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Attn: Dr. Alvin Goodman

Under the Strategic Defense Initiative Organization
Program for Reliable Electronic Systems

Title

Reliability of Small Geometry VLSI Devices for Microelectronics

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by

Principal Investigator

Marvin H. White

LEHIGH UNIVERSITY
Sherman Fairchild Professor
of Solid-State Studies
Sherman Fairchild Laboratory #161
and
Department of Electrical Engineering
and Computer Science
Packard Laboratory #19
Bethlehem, PA. 18015

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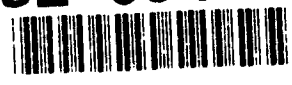

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Dr. Alvin Goodman
ONR/Code 1114
Arlington, VA 22217-5000

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1.0 Introduction

This proposal is a continuation of a project which began in August 1986 under the title. "Reliability of Small Geometry VLSI Devices for Microelectronics" which supported the SDI initiative under Reliable Advanced Electronics. The SDIO agent for the project has been Dr. Clifford Lau and the ONR technical officer has been Dr. Al Goodman. The goal of the project, in a broad sense, is "to perform exploratory research into the physics of carriers in silicon inversion layers with a focus on the issues which affect the reliability of small geometry VLSI devices". This project permits us to study the physical electronics of silicon surfaces and the overlying insulators, thereby providing excellent tools for graduate research and education. We are aware of the specific needs of the SDI mission and the way the above research translates into the project needs. In the proposed project we stress the application of this research to the area of Wafer Scale Integration where reliability and fault tolerance are key issues for the SDI program.

The extensive signal processing and data storage required to implement high-resolution, sensor-based systems demands that strong consideration be given to the area of system and component reliability. At the component level the issues revolve around the reliability of the scaled MOS Transistors with nanometric feature sizes. One important area is the susceptibility of the gate insulator to (1) hot electron trapping, (2) premature dielectric breakdown, and (3) space radiation environment considerations which can limit the MTTF of the SDIO mission. This requires an examination of the basic gate dielectric and there is mounting strong evidence for the replacement of the conventional oxide by an ONO-type dielectric. This dielectric has been employed quite successfully in the storage capacitor of high-density DRAM's and the inter-poly dielectric in floating-gate EEPROM's. More recently, a number of researchers have argued for the use of ONO dielectrics as the basic gate insulator in nanometric MOS devices based upon its immunity to hot carrier trapping and increased dielectric breakdown attributes. In the previous SDI program we were able to make contributions to the understanding of ONO dielectrics [1] as well as grow extremely high quality, 'ultra-clean dry' thermal oxide layers on the silicon surface [2].

A second issue at the component level is the SDI need for low-power, high-density, nonvolatile data storge with nondestructive readout (NDRO), radiation tolerance and immunity to single event upsets (SEU's). In this area we have performed research on a low voltage, electrically reprogrammable, nonvolatile semiconductor memory device called the SONOS transistor. We have demonstrated programmability at 5V levels

and we have initiated a technology transfer effort to the Westinghouse Electric Corporation's Advanced Technology Division in Baltimore, MD. In addition, we have had active discussions with SIMTEK, in Ft. Collins, CO. to provide a technology transfer of low programming voltage SONOS memory cells for high density nonvolatile memories. The research in this area has allowed us to understand the basic operation of charge transport and storage in multi-dielectric nonvolatile memory devices. We have performed charge separation in the erase and write modes for both electrons and holes on the same device structure with a dual channel SONOS structure [3]. The proposed continued research in these areas emphasizes the importance of electrically-reprogrammable, nonvolatile semiconductor memory devices for (1) high-density memory and (2) 'links' for fault-tolerant Wafer Scale Integration. The system reliability aspects in SDI will be enhanced with the development of such electrically-reprogrammable links to provide self reorganization and restructuring of the data path through these control 'links'. The large amount of data taken by the SDI sensors and the need to maintain a continual update on the position of multiple targets puts a high demand on the system reliability and the need for fault tolerant architectures. An electrically-reprogrammable, non-volatile, 'link' would play a major role in insuring system reliability and offering the means to achieve an adaptive and self-restructuring data flow for fault tolerant operation.

The anticipated payoff of this research is both basic and practical. The basic for fundamental portion concerns the understanding of charge trapping in dielectrics and their influence on device reliability (i.e the component level). The practical or applied portion has a direct impact on the formation of a highly reliable gate insulator for the nanometric small geometry MOS Transistors and the realization of nonvolatile semiconductor memory devices. These devices will play a major role in Reliable Wafer Scale Integration because the scaled MOS Transistor are the 'core' elements of the signal processing in the SDI system, while the nonvolatile SONOS semiconductor memory devices can serve as radiation hardened high-density memories and electrically-reprogrammable 'links' to provide ASIC cells for adaptive fault tolerant system architectures. The final payoff in this research is the education of graduate students for the microelectronics industry. During the previous ONR-SDI program we graduated 4 Ph.D. students who are now working at IBM T. J. Watson Jr. Research Laboratory in Yorktown Hts., N.Y., Motorola in Austin, Texas, Wafer Scale Integration in Cupertino, CA., IMEC in Leuven, Belgium. At the present time, we have 2 other Ph.D. students, supported under the ONR-SDI program, completing their Ph.D. dissertations and they expect to graduate in the near future.

2.0 Technical Progress in the Previous ONR-SDI Program

In this section we will detail our experimental and theoretical investigations during the previous ONR program. The basic objective of this program, as stated in the introduction, is to perform exploratory research into the physics of carriers in silicon inversion layers with a focus on the issues which affect the reliability of small-geometry microelectronic devices with nanometric dimensions. Specific goals of the previous program focused on,

- Ultra-clean gate oxidation studies
- Nonvolatile semiconductor memory structures
- MOSFET modeling at cryogenic temperatures
- Irradiation and hot-carrier induced defects
- Multi-dielectric ONO gate insulator

These studies were conducted to address three areas which impacted the following needs of the SDI mission:

(1) High reliability gate insulator to prolong the SDI mission lifetime.
(2) Increased carrier mobility to improve the functional thru-put rate and signal processing speed.
(3) Nonvolatile semiconductor memroy devics with low voltage programming and compatibility with radiation hardened CMOS VLSI technology for high density data storage.

The specific accomplishments, which will be described in detail in the following sections, are

- a new, nonvolatile semiconductor memory device consisting of a dual-channel SONOS device to provide charge separation under erase and write programming voltages.

- a new method to profile the trapped charge in a nonvolatile semiconductor memory device based upon an analysis of the charge retention features.

* a new approach to modeling interface traps in Quantized MOSFET inversion layers with the use of tri-level charge pumping. Quantization effects were observed with the use of substrate bias.

* a new theory for the 2D capture cross section of interface traps. This theory accounts for the discrete energy states in the conduction band caused by the Quantization of electron motion normal to the silicon surface. The energy dependence of the 2D capture cross section was determined for both electron and hole capture processes.

* a new theory of hot electron trapping in gate oxides has been developed which combines Poole-Frenkel and Hot Carrier trapping into the energy-balance equation. Experiments were carried out with a new vertical-field, buried channel, hot carrier injector structure to provide very low electric fields in the gate insulator. Ultra clean/dry oxides were used in the studies.

* an analytical model was developed for the electric field in vicinity of the drain junction of a MOSFET. The results of this model are applicable to the LDD MOSFET device which is employed to minimize hot-carrier trapping in gate dielectrics.

* a new method was developed to extract modeling parameters for MOSFETs with multi-dielectric gate insulators (e.g. the CNO type).

2.1 Nonvolatile Semiconductor Memory Research

In this section we describe the research performed in the area of nonvolatile semiconductor memory devices. *The student researchers in this area were Frank Libsch, Anirban Roy and Umesh Sharma who have received their Ph.D. degrees and are now working for I.B.M.'s T. J. Watson Research Lab., Wafer Scale Integration and Motorola-Austin, respectively.* This section details the work of these researchers and their contributions to the understanding of the scaling of the SONOS nonvolatile semiconductor memory device.

2.11 Characterization of Scaled Low Voltage SONOS Devices

A Model, based on two carrier conduction (electrons and holes) at both injecting boundaries (semiconductor bulk and gate electrode) has been developed to interpret the ERASE/WRITE characteristics of scaled SONOS devices. The amphoteric statistics in this model describe the positive and negative charging of the deep-level traps in the nitride 'memory' layer. S[M]NOS (polysilicon[metal]-oxide-nitride-oxide-semiconductor) transistors and capacitors with the botton ('tunnel') oxide layer thickness around 20A, the final nitride layer thickness below 100A, and the top ('blocking') oxide layer thickness between 35-50 A. have been fabricated and characterized. The model is consistent with the experimental data which provides physical insight into the mechanisms of charge injection, transport and storage during the ERASE/WRITE operation. Lattice imaging electron microscopy (TEM), ellipsometry, electrical capacitance, and chemical etch back techniques have been used to determine scaled S[M]ONOS material parameters. The linear voltage ramp technique [4], which simultaneously measures the flatband voltage shift and separates the charges at the injecting boundary, and the dynamic pulse techniques of flatband tracking [ ] and threshold monitoring [6], which measure ERASE/WRITE, retention and endurance operations, have been employed to electrically characterize the scaled S[M]ONOS devices. Fig. 1 illustrates the saturated flatband memory window for the scaled MONOS device where the crossover time is defined as the start time of pulsed memory window availability. Fig. 2 illustrates the dynamic programming of these devices where the crossover time is 1.5 ms with the flatband memory window centered at -1.4V for a -5V 100ms ERASE and a +5V 10 ms WRITE operation.

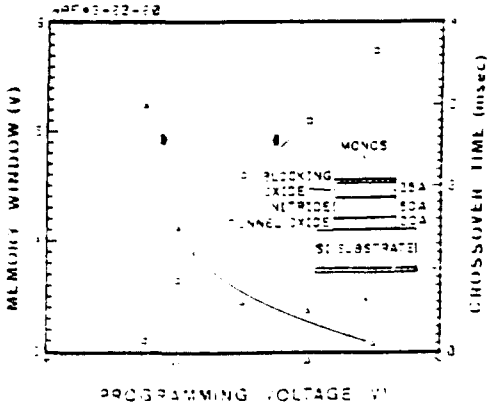


Fig. 1 V_{fb} and memory window center vs V_g for Wafer 3. The device dimensions are X_{OT} = 20 Å, X_N = 50 Å, X_{OB} = 35 Å, and area = 1.269 × 10⁻³ cm².

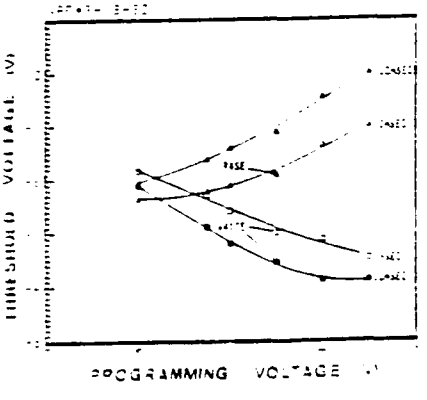


Fig. 2 Saturated memory window and crossover time vs V_g for Wafer 3. The device dimensions are X_{OT} = 20 Å, X_N = 50 Å, X_{OB} = 35 Å, and area = 1.269 × 10⁻³ cm².

We have demonstrated a differential, saturated ERASE/WRITE flatband shift of 3.8V with a differential 5V programming voltage for scaled-down S[M]ONOS devices with dimensions of 20A for the tunnel oxide, 50A for the nitride and 35A for the blocking oxide. With 5V saturated ERASE/WRITE programming voltages and 10^6 ERASE/WRITE cycles, extrapolated retention gives a projected 10 year 0.5V memory window at room temperature [7]. Fig. 3 illustrates the 'zero bias' retention characteristics of a MONOS device and the associated energy band diagram to show the discharge of the stored charge in the 'memory' traps. The *turn-on voltage* of the scaled MONOS device is obtained through the equation,

$$V_t = V_{th} + [2I_{DS}/\beta]^{1/2} \qquad (1)$$

where $\beta = \mu_o(W/L)C_{ox}$ and

$$V_{th} = V_{FB} + 2\emptyset_F + \gamma(2\emptyset_F + V_{SB})^{1/2} \qquad (2)$$

represents the device threshold voltage with $\gamma = (2K_S q N_B)^{1/2} C_{ox}$ as the *body-effect* factor. Thus, the characteristics of Fig. 3 are shifted in the positive direction (at $V_{SB} = 0$) by approximately 2V for the turn-on voltage, V_t, which makes the characteristics appear more symmetrical about $V_{GS} = 0$. These MONOS devices have the best ERASE/WRITE electrical characteristics reported to date for scaled dielectrics and we attribute the results to the optimization of the insulator thicknesses as well as control over the trap density within the nitride film.

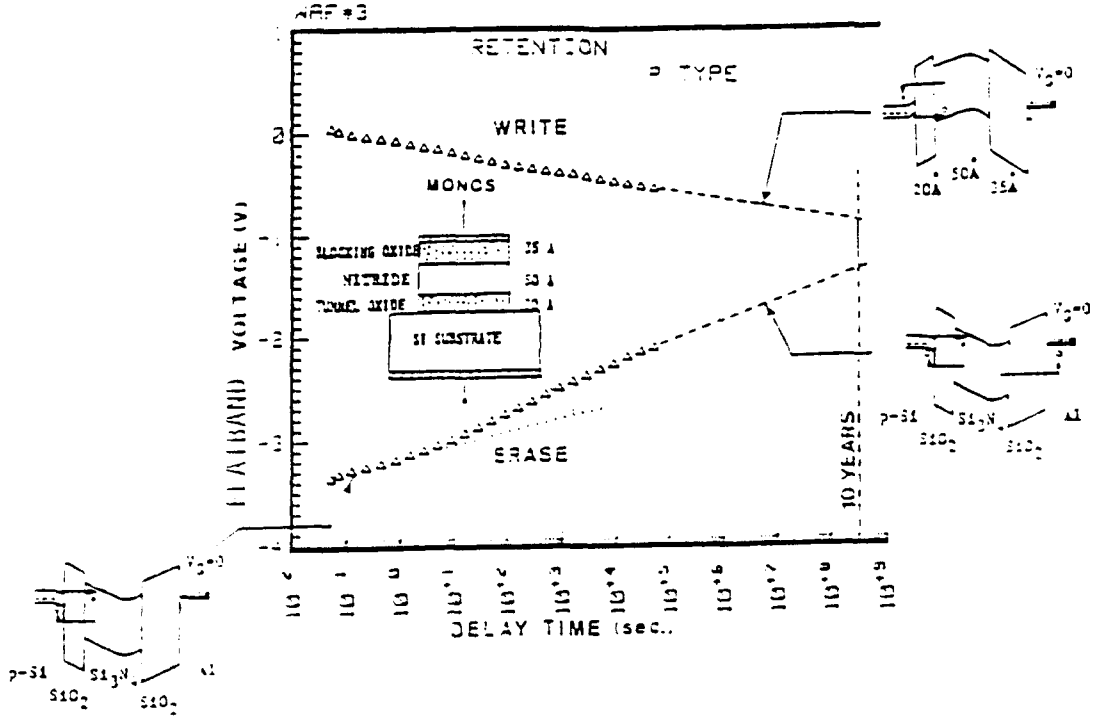


Fig. 3 Zero bias retention characteristics at $V_{FB} = 3$ after 10^6 cycles. The device is initialized with ± 5 V bias, 10 s pulse widths. The device dimensions are $X_{OT} = 20$ Å, $X_N = 50$ Å, $X_{OB} = 35$ Å, and area = 1.269×10^{-3} cm^2.

In addition, these devices have displayed excellent resistance to ionization radiation where fast interface traps are not generated up to 1 Mrad (Si) Co^{60} gamma dose [8]. There is a small build-up in the bulk insulator which saturates with dose and the effective electron mobility is unaffected by the radiation. Fig. 4 illustrates the C-V characteristics of a SONOS device before and after irradiation where a +5V bias has been maintained to maximize the amount of stored charge. Fig. 5 shows the measured mobility before and after irradiation and there is no indication of deterioration. Simulations indicate the charge distribution in the gate insulator [9] must lie within 25A of the Si-SiO_2 for mobility deterioration with maximum deterioration when the charge distribution lies in the plane of the interface. There is very little experimental evidence of interface trap build-up in these SONOS devices and a model has been proposed which relies on the immobility of protons to penetrate the nitride insulator [8].

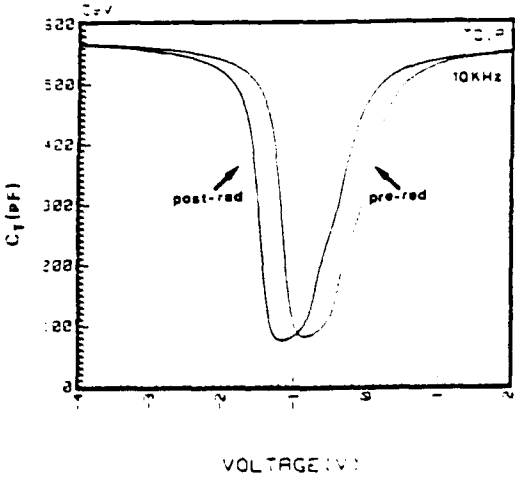


Fig. 4 C–V curves measured at 10 kHz before and after radiation. There is no increased distortion in the curve after radiation (type B device).

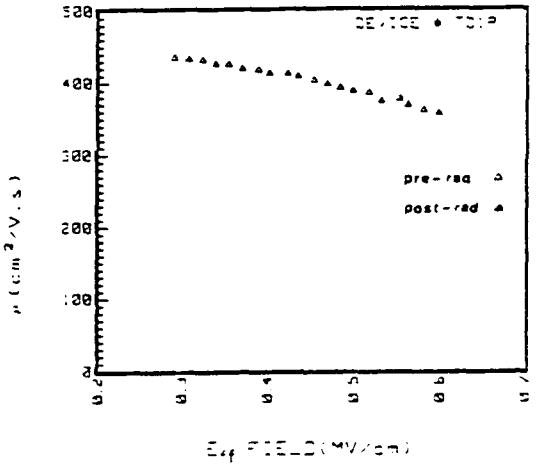


Fig. 5 Inversion layer mobility before and after radiation plotted as function of effective field. Mobility is unchanged after radiation (type B device).

2.12 Dual Channel SONOS Device for Charge Separation

The charge transport and trapping properties of insulating films on semiconductors are related to reliability problems in MOSFET's and memory properties of nonvolatile memory devices. Physically-based device models require delineation of electron and hole processes. Until recently, electron and hole charge separation at the semiconductor-insulator interface has been restricted on gate bias polarity because of minority carrier recombination-generation at the silicon surface [4]. We have, for the first time, demonstated a dual channel transistor accomplishes electron and hole charge separation on the same microstructure for both gate polarities which

obviates the need for complementary transistors and assumptions of identical dielectric and interface properties for the transistor pair. We have applied this new approach to the study of scaled dielectric oxide-nitride-oxide (ONO) memory devices and their charge trapping characteristics [3]. Figs 6 and 7 illustrate the single (surface channel) and dual-channel (surface and buried channel) SONOS nonvolatile memory device structures and their respective linear voltage ramp (LVR) or quasi-static C-V characteristics. We can see charge separation for back-tunneling electron current, I_n, is not possible with the surface channel structure because the electrons recombine with holes which are existent in the surface accumulation layer. These electrons do not have time to move laterally along the channel to be collected by the source and drain junctions. Electron back-tunneling is evident in the dual-channel do the efficient collection of electrons by the buried-channel.

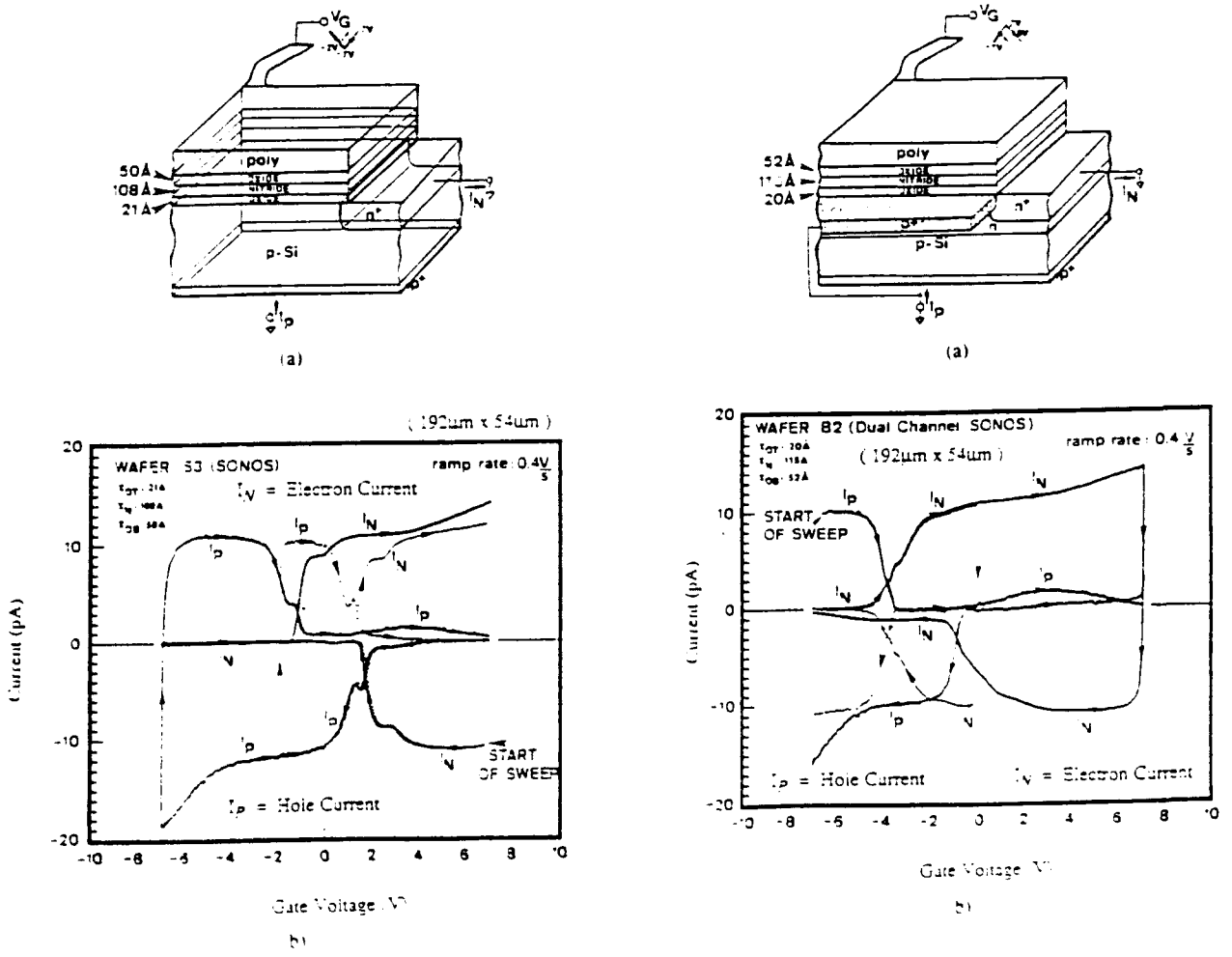


Fig. 6

(a) Isometric view of the n-channel SONOS transistor during LVR measurements. (b) Electron and hole currents corrected for parasitics in a LVR measurement of n-channel transistor from wafer *S3*.

Fig. 7

(a) Isometric view of the dual-channel transistor structure (192 µm x 54 µm) from wafer *B2* during the LVR measurement. (b) Electron and hole currents from the LVR measurement on a dual-channel device from wafer *B2*. Curves are corrected for parasitics.

The operation of the dual channel structure is illustrated in Fig. 8 under positive and negative gate bias conditions. We see under positive gate bias the electrons can be supplied by the buried channel while back-tunneling holes are collected by the substrate. Conversely, under negative gate bias the holes are supplied by the surface channel while back-tunneling electrons are collected by the buried channel. Thus, efficient charge separation is possible under both bias conditions and the charge centroids of both carrier types may be estimated.

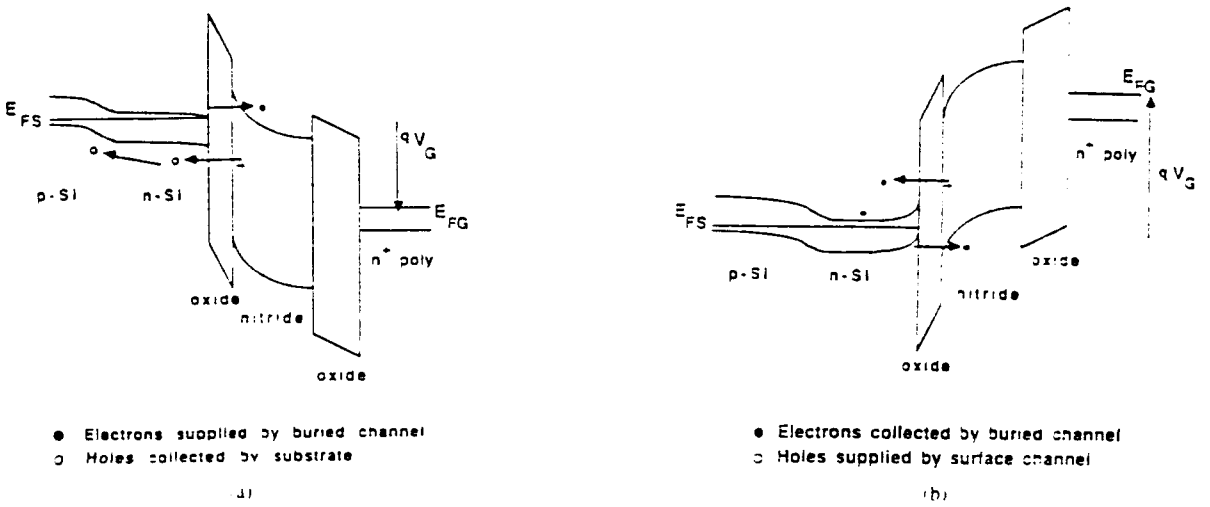


Fig. 8 Energy band diagrams of a dual-channel SONOS transistor under (a) positive gate bias and (b) negative gate bias.

2.13 Tunneling Spectroscopy of SONOS Trapped Charge [10]

An analytical model for the extraction of the spatial trapped charge in silicon nitride has been formulated with amphoteric trap statistics. The model includes the energy distribution of traps in the nitride and the time-dispersive tunneling transitions from these nitride traps. We have examined charge loss from sub-100A nitride films with MONOS memory devices at 110K under different gate bias conditions. If MONOS retention data is taken such that the silicon surface is maintained in a depletion/weak-inversion condition with a suitably selected gate voltage, then the primary charge loss mechanism in the retention mode of operation is back-tunneling of charge from the nitride traps into the silicon bands. The actual charge distribution in the nitride is a function of the charge injection and trapping during the ERASE/WRITE operation as Modified Fowler-Nordheim tunneling of electrons into the nitride generates a non-uniform spatial distribution of trapped charge for an assumed spatially uniform trap density in the nitride.

The charge trapping in silicon nitride is very efficient which leads to the observed nonvolatile memory characteristics in SONOS devices. One memory state corresponds to excess electrons in the nitride while the other memory state describes a condition of excess holes. There are two possibilities to explain the 'charging' behavior of silicon nitride films:

(a) Non-interacting, *close-compensating donor and acceptor traps* which are present in densities of more than 10^{19} /cm^3 and each trap has one transition energy (E_T) and 2 charge states (D^+, D^-).

(b) *Amphoteric traps* which have 3 charge states (D^+, D^-, D^0) and 2 transition energies (E_{TD}, E_{TA}).

There is considerable controversy over which description represents the actual storage of charge in the nitride, however, we have taken the approach which leads to a *single atomistic origin*, namely, the amphoteric trap model. Fig. 9 illustrates the two possibilities for trap models in the silicon nitride and Fig. 10 describes the emission processes for trapped electrons at zero gate bias for an amphoteric trap model. In our model development we considered the back-tunneling from negatively charged traps and we supressed the Poole-Frenkel or thermally assisted detrapping into the nitride by reducing the temperature. Furthermore, we adjusted the experimental conditions (i.e. gate bias during retention) to exclude injection of holes to the neutral traps.

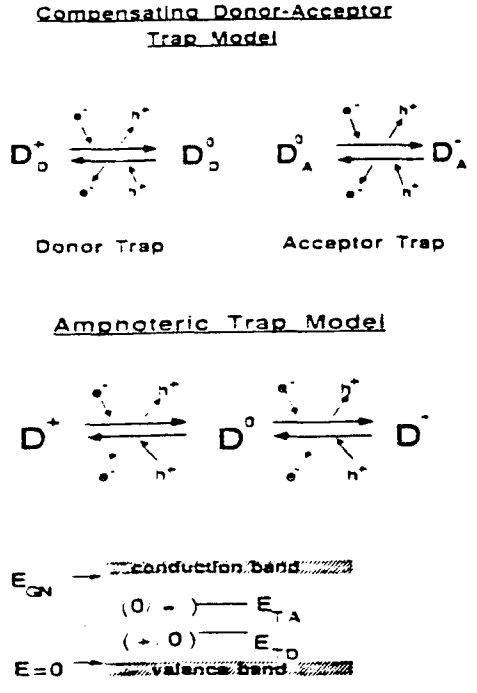


Fig. 9 Charge states and electron and hole processes for: (a) compensating donor acceptor traps; and (b) amphoteric trap; the transitional energies E_{TA} and E_{TD} are also shown.

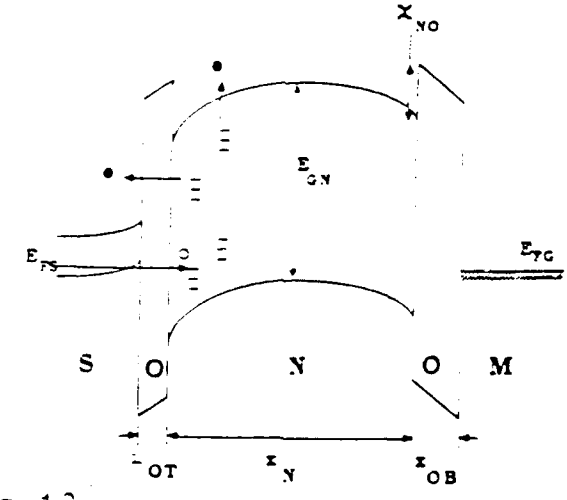


Fig. 10 Energy band diagram for the MONOS structure at zero bias with excess electrons trapped in the nitride; the electron emission processes include thermal excitation from the negative charged state into the nitride conduction band, back-tunneling into the Si conduction band from the negative charged state; there is possibility of hole injection from the Si to the neutral charge state.

Fig. 11 illustrates biased retention data for a p-channel MONOS device operating under depletion/weak-inversion and Fig. 12 shows the spatial distribution of the initial trapped electrons in the nitride. An analytical expression for the threshold decay rate has been derived and with a polynomial fit to the retention data we have extracted the initial electron trap distribution. For a 20A tunnel oxide, 87A nitride and 50A blocking oxide MONOS memory transistor the retention data yielded a spatial distribution of negatively charged traps which linearly increased from the tunnel oxide interface into the nitride bulk saturating about 20-30A into the nitride.

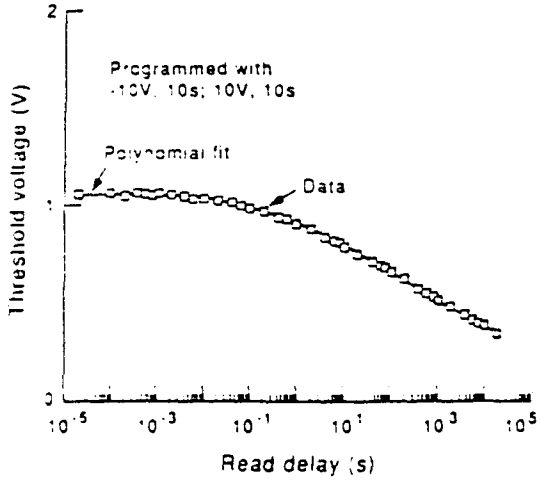


Fig. 11 Biased retention data at 110 K and the polynomial fit for the p-channel transistor from Fig. 5 programmed with initial threshold voltage ~1.5 V higher than in Fig. 5 and bias voltage of 3 V.

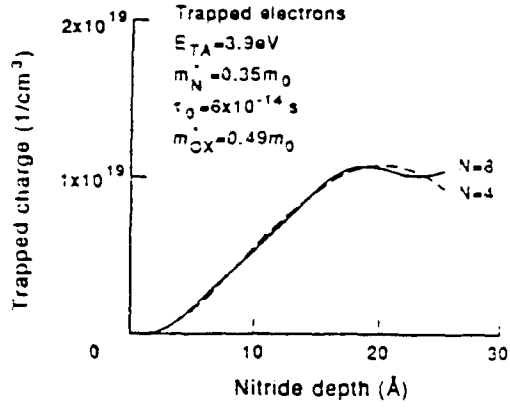


Fig. 12 Spatial distribution of the initial electron trapped charge density in the nitride for the data in Fig. 7 for two different orders of polynomial fit N = 4 and N = 8 and single acceptor level 3.9 eV.

2.2 Interface Trap Modeling in Quantized MOSFET Inversion Layers [11]

The work described in this section was done by Richard Siergiej who is completing the requirements for a Ph.D. at the present time. In highly doped n-channel small geometry device the conduction band is quantized into discrete energy levels when the channel is inverted. In addition, the carriers are localized spatially and the centroid of charge is a finite distance away from the Si-SiO_2 interface. Thus, an electron in a filled interface trap will emit to the first allowed energy level, known as the ground state, which resides 50 meV above the surface conduction band energy level for doping densities of 10^{17} atoms/cm^3. Bulk potential bias will change the degree of quantization and must be included in a modified theory to extract the emission times and capture cross section values for interface traps. We have extended the Shockley-Read-Hall (SRH) theory to

include two-dimensional surface quantization effects and formulate the statistics to account for localization of conduction band charge in both space and energy. The interface trap emission characteristics may be obtained with an electrical measurement called the tri-level charge pumping technique, which offers a convenient method to study emission from interface traps to quantized conduction band states. Measurement techniques of quasi-static C-V, high-frequency C-V, drain current, and charge pumping are used to characterize the interface. Tri-level charge-pumping measurments on large (100μm x 10μm), highly doped MOSFET's provide experimental evidence of two dimensional effects and extracted electron capture cross sections are found to be an order of magnitude larger than values obtained from classical theory.

2.21 Inversion Layer 2-D Quantization

The band diagram for a two-dimensional Si-SiO_2 system is shown in Fig. 13. In the general problem of surface quantization in (100) silicon, two sents of subbands are formed due to the asymmetric properties of the doubly degenerate energy ellispsoids along the k_z axis and the four-fold degenerate ellipsoids along k_x and k_y [1 2]. The lowest subband is formed from the doubly degenerate ellipsoids and is called the ground state. The levels E_0, E_1, and E_2 are due to the doubly degenerate energy ellipsoids in k-space while the E_0^1 level is the ground state for the four-fold degenerate ellipsoids.

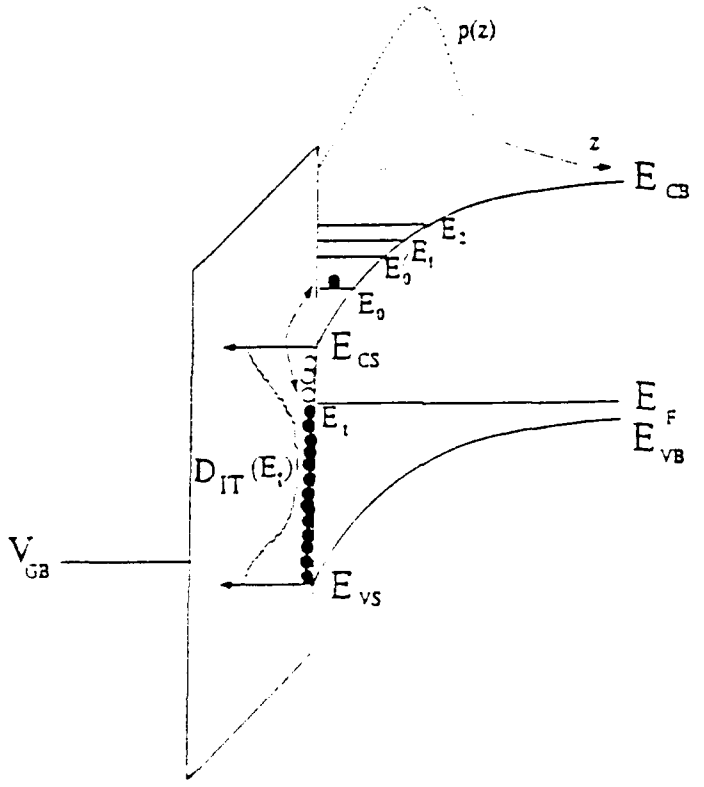


Fig. 13 The Two-Dimensional Si-SiO_2 System

2.22 Tri-Level Charge Pumping Technique

The experimental techniques employed to analyze the 2-D inversion layer effects involve a new measurement method called tri-level charge pumping. The automated measurement setup is shown in Fig. 14 which consists of a menu-driven charge-pumping program on the HP9000 computer. Pulses are supplied from the HP8115A pulse generator to the gate of the device under test. Charge pumping current is measured with a Keithley 616 electrometer and an HP59313A A/D converter. Bulk bias is supplied with the HP4145A. The gate waveform is illustrated in Fig. 15 together with the data obtained from the electrometer measurement of the charge-pumping current. The substrate bias creates a change in the emission times and this is shown in Table I. The experimental results may be explained with the quantization of the inversion layer into subbands and the electron and hole emission times are extracted as shown in Fig. 16. This method offers an excellent means to obtain the emission times and the capture cross sections of both carrier types [1 1].

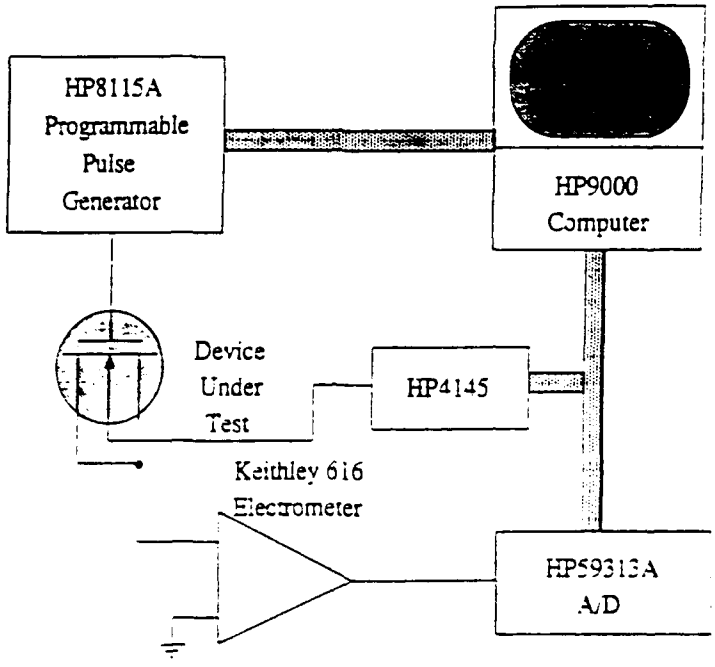


Fig. 14 Automated Charge Pumping Measurement Set-Up

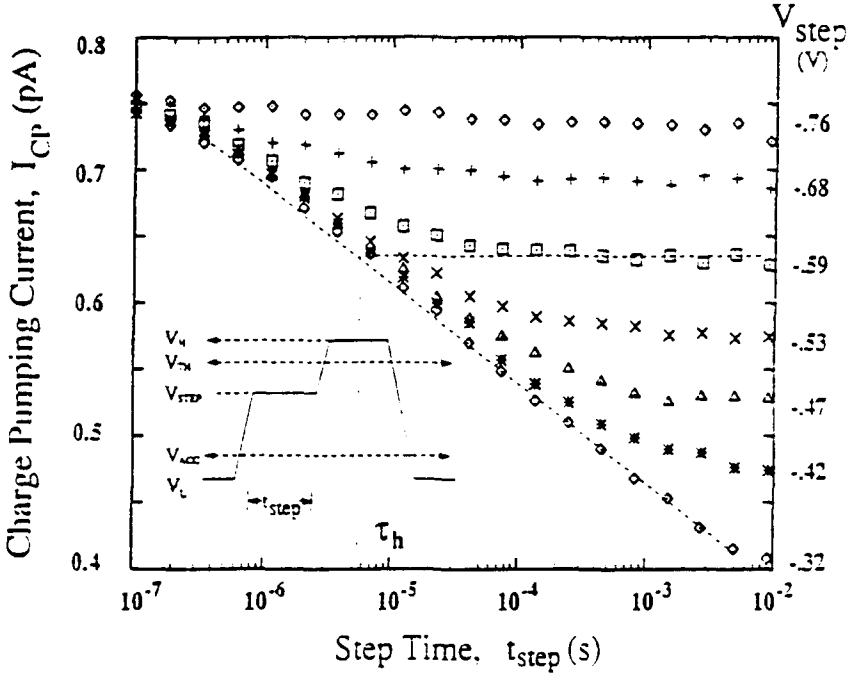


Fig. 15 Charge Pumping Current I_{cp} vs. Step Time t_{step}

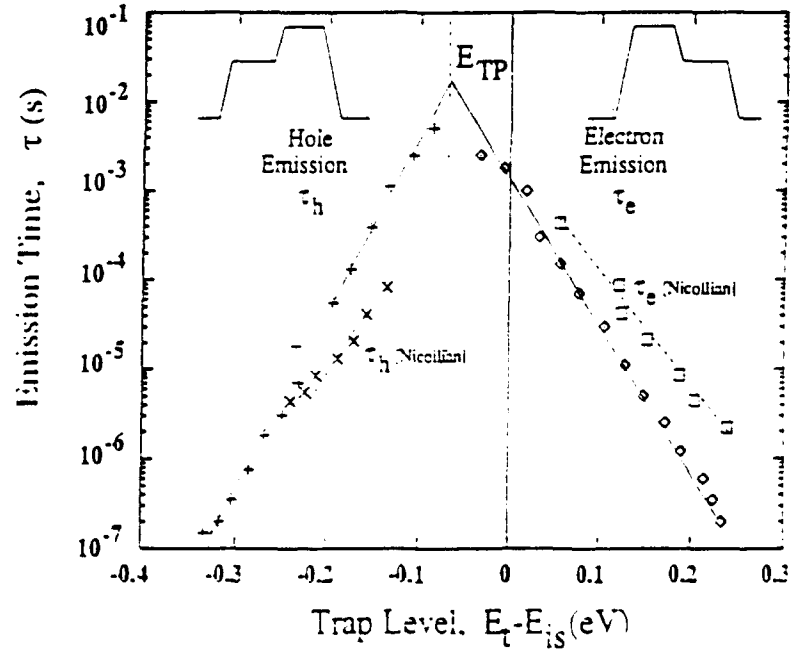


Fig. 16 Electron and Hole Charge Pumping Emission Times

2.23 Two-Dimensional Capture Cross Sections

In the past, researchers had considered emission and capture processes to occur from the conduction band edge to the energy of the interface trap as shown in Fig. 13 [13]. An analysis of the 2-D capture cross section for electrons in the inversion layer yields

$$\overline{\sigma}_n(2D) = \frac{e^{(E_{CS}-E_t+\Delta E_0)/kT}}{\tau_e v_{th} N_C(2D)} \qquad (3)$$

where

$$\Delta E_0 \approx (\frac{\hbar^2}{2m_l})^{\frac{1}{3}}(\frac{9\pi q}{8K_s\epsilon_o})^{\frac{2}{3}}[2K_s\epsilon_o q N_B(2\phi_F + V_{SB})]^{\frac{1}{3}} = \alpha(2\phi_F + V_{SB})^{\frac{1}{3}} \qquad (4)$$

is the ground state splitting from the conduction band edge and the surface electric field is determined by $\mathcal{E}_s = (Q_B + Q_{inv})/K_s\epsilon_o$. The ground state has a substrate bias dependence and this is seen in the ratio of the emission times from an interface trap to the ground state in the conduction band. If we combine equations (3) and (4) we obtain the expression

$$ln(\frac{\tau_{e1}}{\tau_{e2}}) = \frac{\alpha}{kT}[(2\phi_F + V_{SB1})^{\frac{1}{3}} - (2\phi_F + V_{SB2})^{\frac{1}{3}}]. \qquad (5)$$

We can extract the capture cross section dependence on trap energy and measure such cross sections close to the edge of the conduction band at reduced temperatures.

Table I
Experimental and Theoretical
Quantization Results

Substrate Bias, (V)	Emission Time, (s)	$\mathcal{E}_s$ (V/cm)	E_0 (meV)	$ln(\frac{\tau_e}{\tau_e\|_{V_{SB}=0}})$ eqn (26)	
0	$1.1x10^{-5}$	$1.6x10^5$	49	Experiment	Theory
1	$1.9x10^{-4}$	$2.4x10^5$	64	.55	.58
2	$3.0x10^{-4}$	$3.0x10^5$	73	1.0	.97

The emission times of electrons and holes are equal at an energy level called the *pinning level* , E_{TP}, [14] which is given as

$$E_{TP} - E_{is} = -\frac{kT}{2} ln(\frac{\sigma_n}{\sigma_p}) + \frac{\Delta E_0}{2} \qquad (6)$$

We find the capture cross sections for electrons and holes are almost constant with energy over the middle of the energy gap with $\sigma_p(3D) = 10^{-16}$ cm^2 and $\sigma_n(2D) = 10^{-13}$ cm^2. The latter are typical for coulombic trapping centers and appears tri-level charge pumping probes neutral interface traps in the upper half of the bandgap over the range of energy levels studied. The small capture cross sections for holes in the lower part of the gap indicates charge pumping probes donor-like (positively charged) interface traps. Thus, over the limited range of energies studied with this technique at room temperature, a simple donor-like interface trap model can explain the observed behavior of the capture cross section data. Substitution of the data obtained in the experiment for electrons and hole capture cross sections gives $E_{TP} - E_{is}$ = -65 meV, which is in good agreement with Fig. 16.

2.3 Hot Electron Trapping in Gate Oxides

Hot electron trapping in gate insulators is a reliability problem associated with scaled MOSFET's. In other instances, channel hot electron (CHE) injection into a gate oxide is employed to electrically program a *floating gate* nonvolatile semiconductor memory device. In our studies we have addressed several issues, namely, (1) the growth of ultra clean/dry oxides with low latent defects, (2) the development of a consistent theory of hot electron trapping in gate insulators which covers a wide range of oxide electric fields, and (3) the creation of novel test structures to examine and model hot carrier trapping in gate insulators. *The work performed in this section is the research of Sukyoon Yoon who is completing the requirments for a Ph.D. at the present time.*

2.31 Ultra Clean/Dry Triple Wall Oxidation

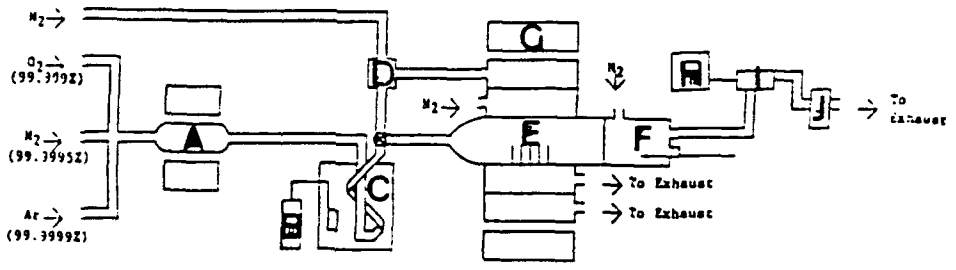
According to the conventional scaling theory for MOS transistors [15], the gate oxide thickness decreases from 200A for 1.25 μm CMOS technology [16], which have a 1.0 μm effective channel lengths, to 70A for 0.25 μm [17] which have 0.25 μm effective channel lengths. Without a concommitant reduction in supply voltage from the present 5V TTL 'glue-chip' levels reliability problems in these thin insulators will be a major issue in scaling MOSFET's. The desirable gate insulator should have good uniformity, small defect

density, high dielectric breakdown strength, high charge-to-breakdown, small interface trap density and should endure hot electron injection and ionizing radiation without the occurrence of high interface trap densities and fixed oxide charges.

To grow reliable thin gate oxides we must as a first condition prepare a $Si-SiO_2$ interface with a low concentration of hydrogenated dangling bonds. A high density of these bonds would not be detected in the initial electrical characteristics of a MOSFET since the 'charge state' of these bonds would be neutral or latent. However, the electrical characteristics of the MOSFET's may be highly unstable since these hydrogen bonds can be broken by hot electrons and/or ionizing irradiation. Thus, active or 'charged' electron traps may be generated due to these dangling bonds. A second condition is to have a low active trap density so even if the traps become activate, then the trapped charge is too small to alter the characteristics of the MOSFET's.

The conventional single-wall oxidation method introduces defects or impurity traps in the oxide by allowing the diffusion of heavy metal ions and mobile alkali ions through the quartz tube wall [18]. Also, a considerable amount of moisture is incorporated into the oxide by the diffusion of water through the single quartz wall. To elimate these adverse conditions a special triple-wall oxidation furnace system has been designed and implemented successfully [2]. This new oxidation system permits the study of the $Si-SiO_2$ interface with a control on the number of electronic defects inherent in the processing of MOS devices. Several authors have reported ultra-dry oxides, but they were grown in double-wall oxidation furnaces [19]. A double-wall furnace can provide a HCl protective atomosphere in an outer gap around the reaction chamber to remove metal contaminants; however, such a technique has been entirely satisfactory since there is a tendency for some contamination to occur due to water or moisture associated with halogen reaction products.

The triple-wall oxidation system consists of 4 major parts: a triple-wall oxidation furnace tube, a precombustion furnace, a cold trap assembly and a hygrometer assembly. Fig. 17 (A) shows the schematic diagram and Fig. 17 (B) is a photograph of the triple-wall oxidation system. The custom-designed, triple-wall oxication furnace tube (E) is made of 3 concentric quartz tubes whose ends are sealed together to leave gaps between each quartz tube. The operation of this system has been described previously [2] and we have seen a tight dielectric breakdown distribution for 9.3 nm gate oxides around a mean value of 15 MV/cm. Furthemore, there is very little evidence of an initial or premature breakdown [20] which has been attributed to 'weak spots' in the oxide and associated large local electric fields. We believe that such 'weak spots' and pinholes are minimized for the oxides grown in the ultra-clean triple-wall oxidation furnace. The mean breakdown electric field is much higher than the previously reported values of 10-12 MV/cm. [21].



(a)

A. Pre-combustion Furnace Assembly

B. Immersion Cooler

C. Dewar and Quartz Cooling Coil

D. TCA Apparatus

E. Triple-wall Furnace Quartz Tube

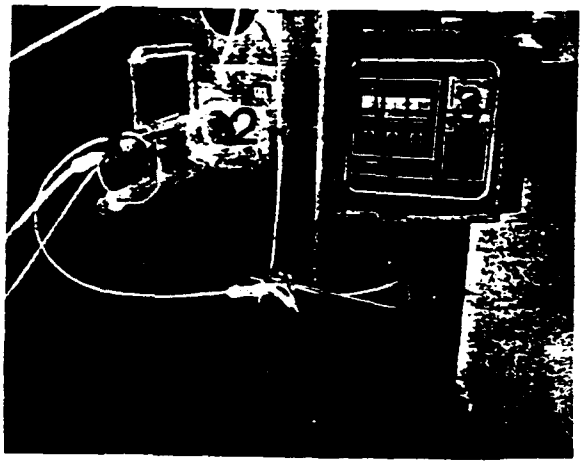
F. White Elephant

G. Oxidation Furnace

H. Dewpoint Meter

I. Humidity Sensor

J. Dessicant Chamber



(b)

Photograph of Triple-wall Oxidation System

1. White Elephant
2. Triple-wall Oxidation Furnace
3. Oxidation Furnace
4. Pre-combustion Furnace Assembly

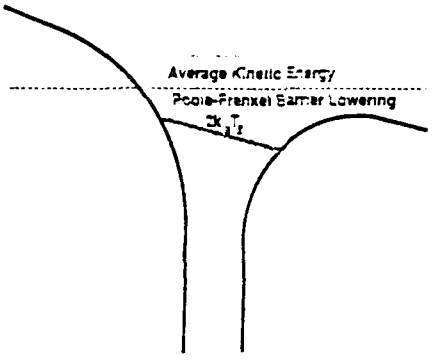
Fig. 17

– A) Schematic diagram of the triple-wall oxidation furnace system. (B) Photograph of the triple-wall oxidation furnace system.

We have also observed a higher charge-to-breakdown, Q_{BD}, with oxides grown in the triple-wall oxidation system. We have seen values of 45 C/cm^2 at low current stress (0.1A/cm^2) approaching 18 C/cm^2 at high current stress conditions (1A/cm^2). There have been reported values of larger Q_{BD}'s for ONO dielectrics [22], but these values for oxides are the highest reported to date. We have also stressed insulators with Q_{BD} values of 20 C/cm^2 under the condition of high oxide electric fields (i.e. Fowler-Nordheim tunneling) and found the interface trap density at midgap saturates at 4 x 10^{12} traps/cm^2 which is considerably smaller than previous results [23] where the trap density continued to increase with stress. Finally, we employed a vertical field injector structure [24] to study the build-up of the interface trap density in a moderate oxide electric field (1 MV/cm). The results shown D_{it}(mg) after stress increased from 8.6 x 10^9 traps/eV cm^2 to 2.8 x 10^{10} traps/eV cm^2 with a stress of 3.4 C/cm^2. This rate of interface trap generation is about 10^{-3} which is 2 orders of magnitude less than reported values in the industry. This result indicates 1B electrons must pass through the triple-wall grown oxide at 1 MV/cm oxide field before 1 interface trap is generated. We believe this is a direct consequence of removing the latent defects in the oxide with the triple-wall oxidation system.

2.32 Theory of the Hot Electron Capture Cross Section

A unified theory of hot carrier trapping has been developed with the concept of an average hot electron energy (q α E), where α is the mean-free path of approximately 3.2 nm [25]. The approach is to start with the energy balance equation and a colombic trap as shown in Fig. 18 , where the 'trap' term is attributed to the Lax theory of cascade capture [26], the Poole-Frenkel effect was included by Dussel and Boer [27] and we have added the average kinetic energy term [28]. The effect of this formulation is to realize a unified theory of hot carrier trapping over a wide range of oxide electric fields. In the very low field regime (< 0.1 MV/cm) the capture cross section is constant with applied electric field and in the moderate electric field regime (<1 MV/cm) the capture cross section varies as the -3/2 power with applied field. Finally, for the high field regime (> 1 MV/cm) the capture cross section varies with the -3 power of electric field. Previous work by Ning offered an explanation for the high field dependence based upon an assumed dependence of capture cross section and energy [29].



$$-\frac{zq^2}{4\pi K_\infty \varepsilon_o r} - qEr\cos(\theta) = -\left(zk_B T_L - \sqrt{\frac{zq^3 E}{\pi K_\infty \varepsilon_o}} - \alpha qE\right)$$

Potential Energy | Electric Field | Trap | Poole-Frenkel Barrier Lowering | Average Kinetic Energy

Fig. 18 Formulation of the Energy Balance Equation for the Hot Electron Capture Cross Section of a Colombic Trap. [28]

The analytical development of the capture cross section provides the equations as shown in Fig. 19. The shaded regions represent the additional contributions of the present theory and the capture cross section is shown qualitatively as a function of oxide electric field. Fig. 20 illustrates an isometric view of the capture cross section under the application of a 1.5 MV/cm oxide electric field. We have applied a graphical 2-D package to illustrate the influence of oxide electric field on the capture cross section of a Coulombic trap.

$$\frac{\bar{\sigma}_n(\mathcal{E})}{\bar{\sigma}_n(0)} = \frac{6}{\eta^3} H(\eta)$$

$$\eta \equiv \frac{\sqrt{\frac{q^3 \mathcal{E}}{\pi \kappa_{ox} \varepsilon_o}} + q\alpha\mathcal{E}}{2kT}$$

$$H(\eta) \equiv \left(1 + \frac{\alpha}{2}\sqrt{\mathcal{E}'}\right)^4 \left[G^+(\eta) - G^-(\eta) - \frac{1}{3}\left(1 + \frac{\alpha}{2}\sqrt{\mathcal{E}'}\right)^2 \left(G^+(\eta)^3 - G^-(\eta)^3\right) \right]$$

$$G^{\pm}(\eta) \equiv \frac{1+\eta}{\eta}\left[1 - \sqrt{1 \mp \frac{1}{\left(1 + \frac{\alpha}{2}\sqrt{\mathcal{E}'}\right)^2}\frac{\eta^2}{(1+\eta)^2}}\right]$$

$$\mathcal{E}' \equiv \frac{4\pi\kappa_{ox}\varepsilon_o}{q}\mathcal{E}$$

Fig. 19 Analytical Formulation of Capture Cross Section

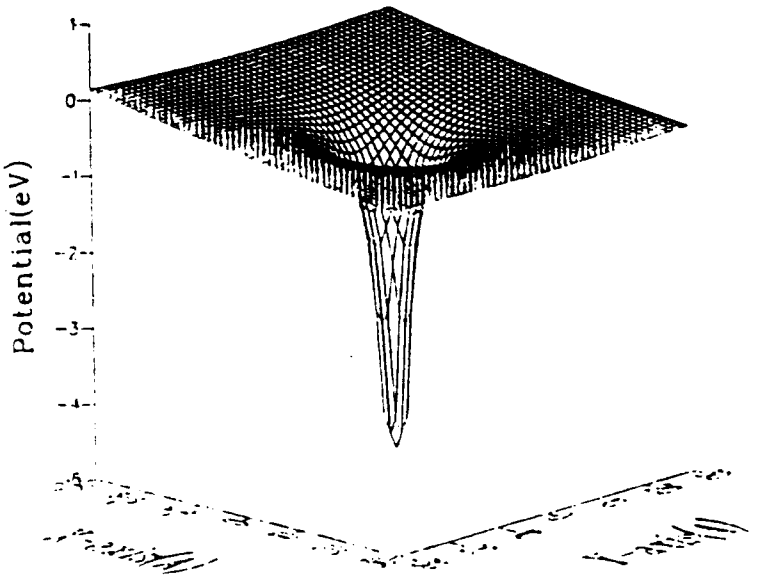


Fig. 20 Hot Electron Trap Cross Section Dependence on Field

2.33 Vertical Field Buried Channel Injector [30]

The study of oxide traps under very low fields has several advantages such as the elimination of electron heating and bulk trap creation with the eventual hope of correlating these traps with technology variations. If we examine the literature on trap capture cross sections, then we observe a seeming mirage of capture cross section data. A primary reason for this diluge of data is, as we have seen from the previous section, the dependence of capture cross section on the oxide electric field. Thus, it is imperative for the researcher to know the electric field conditions under which the oxide trapping occurs and to be able to control these electric fields, particularly in the low field regime. Early experiments with two terminal injectors, such as the avalanche injection technique [31], were unable to control independently the injection level and the oxide electric field. A 4-terminal, surface channel vertical field injector has been used by several investigators [24] to study charge trapping in the gate oxide and to control independently the injection level as well as the electric field in the oxide. A major problem with the surface channel structure is the need to form an inversion layer to control the oxide electric field and, thus, this technique is limited to oxide fields above 0.5 MV/cm. Furthermore, these previous techniques were limited to the electrical injection of one carrier species. In order to circumvent these problems and address the situation of carrier injection at low oxide electric fields, we developed a novel substrate hot electron and hot hole injection structure with a double-implanted buried Channel MOSFET. Fig. 21 illustrates the cross section of the buried channel hot carrier injector structure.

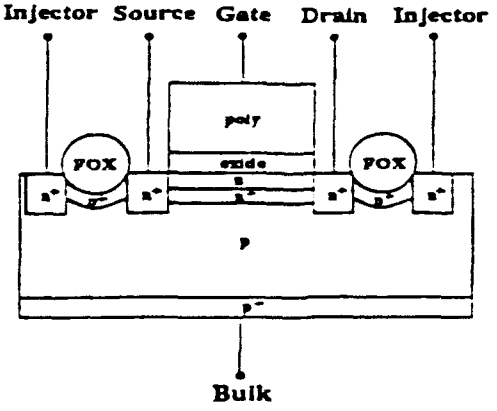
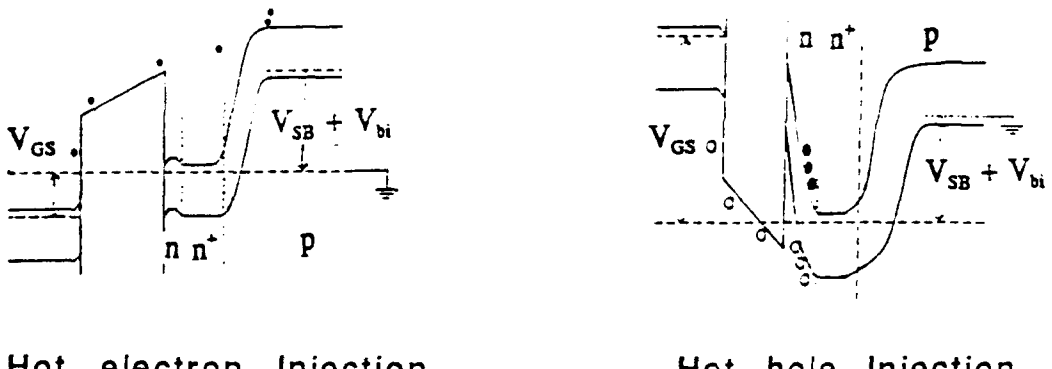


Fig. 21 Double Ion-Implanted Buried Channel Injector

The operation of the buried channel injector is shown in Fig. 22 where hot electron injection occurs by a forward-biased adjacent diode (injector) when the surface is in the accumulation mode. This permits the gate voltage to be lowered to the flatband voltage and electrons may be injected at even zero oxide electric field. In the case of hole injection, the gate is biased to provide a hole inversion layer (supplied laterally by the substrate) and the channel is maintained at a fixed potential. Punchthru is avoided by the use of a double implant. The resulting high surface electric field is conducive for avalanche generation of holes and these holes are accelerated to the oxide by the normal electric field. Fig. 23 illustrates hot electron injection over a range of low electric fields (0 to 0.5MV/cm) at a fixed injection level (A) and for a fixed oxide field (0.04 MV/cm) as the injection level is varied (0 to 9 mA) (B). This is an excellent method to examine the capture cross sections over a wide range of electric fields. The capture cross-sections measured with technique are illustrated in Fig. 24.



Hot electron Injection **Hot hole Injection**

Fig. 22 Operation of the Buried Channel Hot Carrier Injector

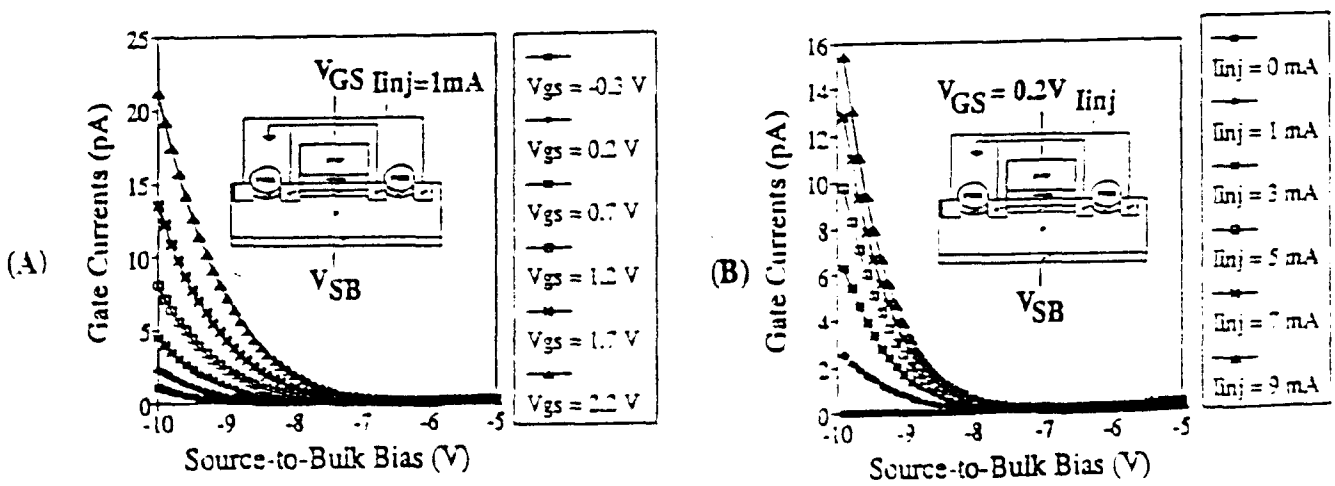


Fig. 23 Experimental Results for Hot Electron Injection

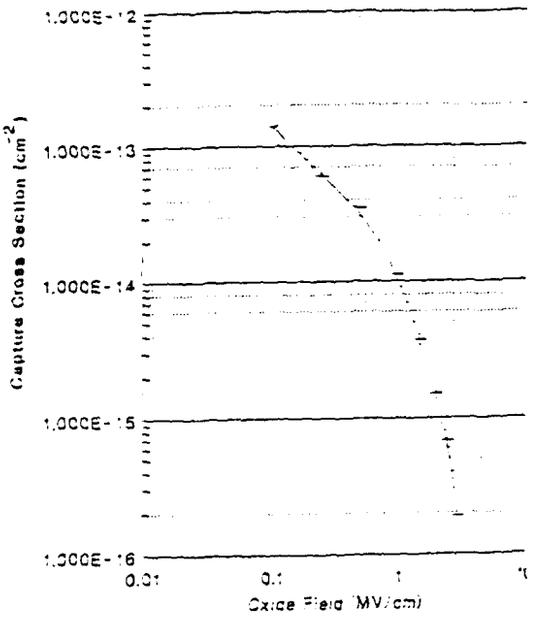


Fig. 24 Experimental Determination of Capture Cross Sections with the Buried Channel Hot Electron Injector

2.4 MOSFET Device Modeling Studies

In this section we will describe work which relates to the study of MOSFET devices, especially devices which are scaled with ONO dielectrics. A novel method will be described which characterizes MOS Transistors with mixed gate dielectric technologies. Current extraction techniques to obtain physically-based model parameters must correct for the presence of the gate capacitance. We present a method to correct I_{DS} vs V_{GS} data for gate capacitance and, thereby, extract accurately low field carrier mobility and surface roughness parameter. Next, we examine the lateral channel electric field for a MOSFET in the vicinity of the drain junction with a pseudo two-dimensional analysis. We derive formulae for the maximum electric field and channel pinch-off distance which are important in the study of device reliability. Finally, we examine nonuniform hot electron injection in vertical injector structures because the extraction of parameters, such as capture cross sections and trap densities, are sensitive to the uniformity of the charge injection.

2.41 Model Parameter Extraction in Multi-Dielectric Devices [1]

The work performed in this section was done by Richard Siergiej as part of his Ph. D. research. In comparing different gate dielectric technologies in MOS transistors, such as oxide-nitride-oxide (ONO) and SiO_2 we must devise a normalizing method to account for the difference in the physical dielectrics. Previous characterization techniques have normalized the data

by dividing the drain current, I_{DS}, or the transconductance, g_m, by the effective gate capacitance, C_{eff}. However, if we apply these methods $\{I_{DS}/C_{eff}, g_m/C_{eff}\}$ to actual devices to determine the advantages and disadvantages of mixed dielectric systems (i.e. the carrier mobility and degree of surface roughness as a function of the particular technology), then we find an ambiguous interpretation of the data because these methods do not remove *completely* the dependence on dielectric capacitance. Our effort has been to develope a method for comparing mixed dielectric systems with the goal of (1) removing the dielectric capacitance dependence in order to unambiguously extract the low field mobilty and the surface roughness parameter, and (2) provide a method which is direct and easy to implement in a computer-based data-acquisition system without the need for extensive numerical techniques.

The basic first order drain current equation, neglecting the influence of interface traps, for small drain biases may be written as,

$$I_{DS} = \frac{\mu_o(\frac{W}{L})C_{eff}(V_{GS} - V_{TH})V_{DS}}{1 + \theta_s[V_{GS} - V_{TH} + 2\lambda\sqrt{2\varphi_F + V_{SB}}]} \qquad (7)$$

where μ_o is the low field mobility, W and L are the MOSFET width and length, respectively, θ_S is the *surface roughness or scattering* parameter and λ is the *body-effect* parameter. The transconductance g_m can be obtained by differentiation of (7) to obtain,

$$g_m = \frac{dI_{DS}}{dV_{GS}} = \mu_{FE}(\frac{W}{L})C_{eff}V_{DS} \qquad (8)$$

where the *field-effect mobility* is,

$$\mu_{FE} = \frac{\mu_o[1 + \lambda\theta_s\sqrt{2\varphi_F + V_{SB}}]}{[1 + \theta_s(V_{GS} - V_{TH} + 2\lambda\sqrt{2\varphi_F + V_{SB}})]^2} \qquad (9)$$

and the surface scattering parameter may be expressed as

$$\theta_s = \frac{K_O}{2K_S t_{eff} E_{cr}} \qquad E_{cr} = \frac{l\hbar\sqrt{\pi}}{\mu_o\Delta^2 m^*} \qquad (10)$$

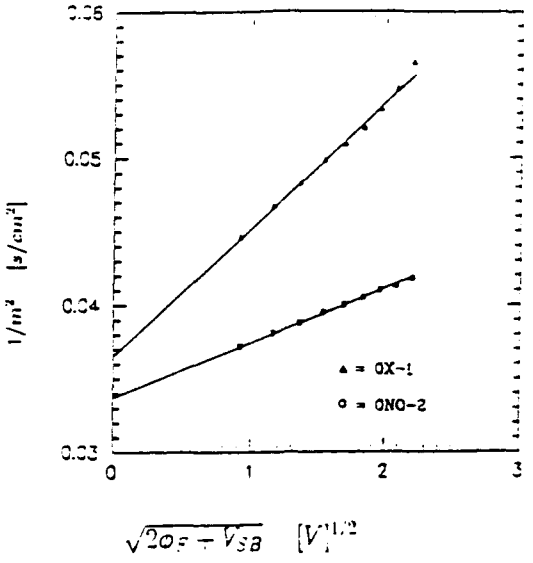
in terms of the critical electric field, E_{cr}, for mobility degradation. The parameters 'Δ' and 'l' describe the mean asperity height and correlation length, respectively, for a Gaussian distribution of surface asperities [9]. A physical picture of the Si-SiO_2 interface may be obtained with such model parameters and related to the particular selection of technology. In fact, on this very point there has been considerable discussion with Japanese firms, such as Hitachi and Toshiba, to understand why one type of ONO technology

provides improved MOSFET electrical characteristics as compared with other technologies. These companies have discovered the oxidized LPCVD nitride films (i.e. these are the films we have been studying on the ONR-SDI program and Hitachi refers to these films as ONO *stacked nitride*) offer superior performance to other approaches, such as the ammonia and nitrogen treated ONO films. One such explanation (offered by Hitachi) is the decrease in nitrogen (4% at.wt.) at the $Si-SiO_2$ interface as compared with the build-up of nitrogen in the other ONO films (8% at.wt.). This is believed to be due to the prolonged time at high temperatures for the ammonia and nitrogen annealed oxides. In addition, the transconductance and extracted mobilities are higher for the *stacked nitride* ONO films. We believe these films may be the approach for deep submicron devices due to their superior dielectric properties and their overall ability to withstand hot carrier injection and irradiation. This opinion is shared by the above-mentioned Japanese companies [**3 2**].

If we simply divide the transconductance by the effective capacitance to compare a particular ONO technology with another or to a so-called *pure oxide* when each technology has dielectrics with different film thicknesses, then erroneous conclusions can be drawn since this formulation does not remove completely the dependence of the transconductance on the dielectric thickness. An examination of the effective mobility in Equation (9) reveals a thickness dependence through the O_S term in the denominator. The O_S term is independent of thickness since $\lambda = \sqrt{2K_S \epsilon q N_B}/C_{eff}$. Our approach [1] is to divide the drain current, I_{DS}, by the square root of $g_m C_{eff}$ to obtain,

$$\frac{I_{DS}}{\sqrt{g_m C_{eff}}} = \sqrt{\frac{\mu_o (\frac{W}{L}) V_{DS}}{[1 + 2\lambda\theta_s \sqrt{2\phi_F + V_{SB}}]}} (V_{GS} - V_{TH}). \qquad (11)$$

where the slope 'm' is independent of dielectric properties. Thus, we may use Equation (8) to compare insulator technologies by plotting $1/m^2$ versus $[2\phi_F + V_{SB}]^{1/2}$ as shown in Fig. 25. The intercept on the ordinate gives the low-field electron mobility, μ_0, and the slope combined with the intercept gives information on the surface roughness. The pure oxide sample (OX-1) is an ultra-dry oxide with oxide thickness of 237A and an extracted low-field mobility of 542 $cm^2/V\text{-}s$ with a critical velocity $v_{cr} = E_{cr}\mu_0 = 4.2 \times 10^8 cm/s$. The *stacked nitride* ONO sample had an effective oxide thickness of 201A with an extracted low-field mobility of 588 $cm^2/V\text{-}s$ and a critical velocity $v_{cr} = 9.9 \times 10^8 cm/s$ which is twice the pure oxide sample. Thus, the ONO *stacked nitride* dielectric has more than twice the resistance to mobility degradation than its pure oxide dielectric counterpart. The critical velocity consists of fundamental constants and surface related modeling parameters as we can see from Equation (10).



A plot of $1/m^2$, where m is the slope of equation 2, versus $\sqrt{2\phi_F - V_{SB}}$. From the intercept the low field mobility may be found, and the slope gives information regarding the surface roughness. The pure oxide sample (▲ = OX-1) has a rougher surface and lower low field mobility than the ONO sample (○ = ONO-2).

Fig. 25 Comparison of Ultra-dry and Stacked Nitride ONO Technologies

2.42 Analytical Model of a LDD MOSFET [33]

The work reported in this section is part of Yin Hu's research for her Ph.D. degree in the area of solid-state devices. A new analytical model for the lateral channel electric field in LDD MOSFET's has been developed from a pseudo-two-dimensional analysis. The model gives a prediction of the channel electric field when the lightly doped drain (LDD) region is both fully depleted and partially depleted. The normal field mobility degradation and variation of the saturation field E_{sat} with gate voltage have been considered in the model. The model also predicts the variation of the pinch-off point, L_{sat}, with gate bias. Fig. 26 illustrates the cross section of a fully-overlapped LDD MOSFET device which is analyzed by contructing a rectangular Gaussian box with infinitesimal thickness at a general position along the channel. The electric fields at the bouncaries of this general slice are specified by selecting the top of the box as the Si-SiO_2 interface and the bottom of the box as a depth x_j', which may be different from the depth of the LDD junction x_j. The former has been determined from a 2-D device simulation [33] which reveals the normal field in the bulk cannot be neglected as by previous researchers [34,35]. In our model we consider the normal field at the bottom of the Gaussian box, the saturation electric field as a function of V_{GS}, iteratively determine the pinch-off point, L_{sat}, and include the series resistance, R_s, associated with an undepleted LDD region. Fig. 27 illustrates lateral channel electric field as a function of distance and a comparison with the numerical simulator MINIMOS [36].

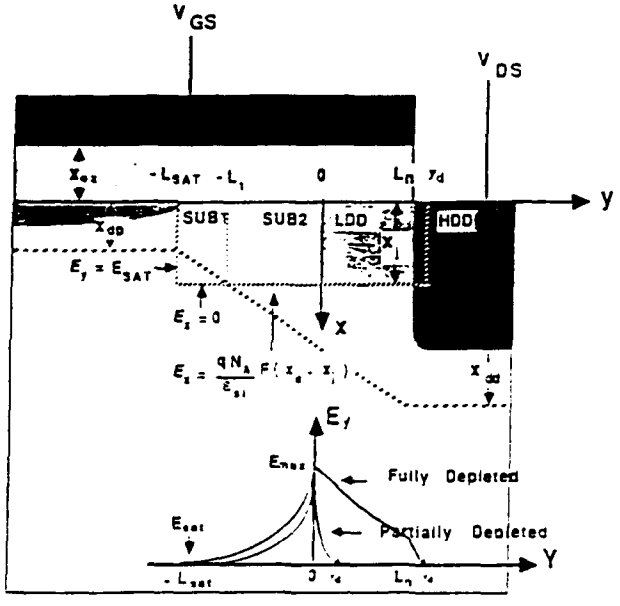


Fig. 26

Cross section of a fully overlapped LDD MOSFET structure near the drain. The region of interest is shown enclosed by the dashed line.

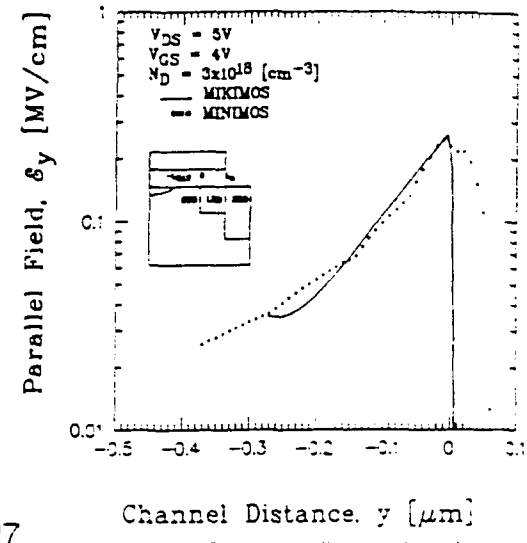


Fig. 27 The lateral electric field versus distance along the channel for a fully overlapped LDD structure. The parameters used in the calculations are $N_A = 5 \times 10^{16}$ cm^{-3}, $N_D = 3 \times 10^{18}$ cm^{-3}, $L = 1$ μm, $L_n = 0.1$ μm, and $x_j = 0.25$ μm.

2.42 Hot Carrier Induced Degradation

The work reported in this section was performed by Richard Booth who has completed his Ph.D. and is currently a postdoctoral researcher at IMEC in Leuven, Belgium. Since we use vertical field injector structures to inject hot carriers into the gate insulator we have investigated the case of symmetrical vs. asymmetrical hot-electron injection into MOS Transistors. The effect of nonuniform injection and trapping on the electrical characteristics of long channel MOS Transistors has been examined. Long channel transistors have been symmetrically injected with carriers introduced from adjacent diode stripes which are parallel to the length of the transistor. Asymmetrical injection is performed by introducing carriers from diodes which are closer to the drain of the device under test. The rate of change in the extrapolated threshold voltage is higher for asymmetrical injection, since the same amount of injected charge is submitted to a smaller portion of the channel region. The maximum transconductance rises over the period of stressing for the asmmetrical injection situation, while the transconductance consistently decreases with stress time for symmetrical injection [37] as illustrated in Fig. 28. We expect the threshold voltage to increase more rapidly for the asymmetrical devices for the same injected electron density because a portion of the channel (i.e. a 'sub-transistor') has a higher injected carrier density per unit area. The

transconductance increase and decrease may be explained with a simple two transistor model [38] which represents the degraded and undegraded portions of the transistor connected in series. The measured transconductance of the device itself is dominated by the transconductance of the sub-transistor with the lowest conductance. Near threshold the higher threshold voltage of the degraded sub-transistor is the important factor and since the effective channel length of this transistor is very small (i.e. a high conductance), we see the transconductance peak shift positive in the asymmetrical injection case. In contrast, for the case of symmetrical injection, we have a continual transconductance degradation or a shift in the negative direction.

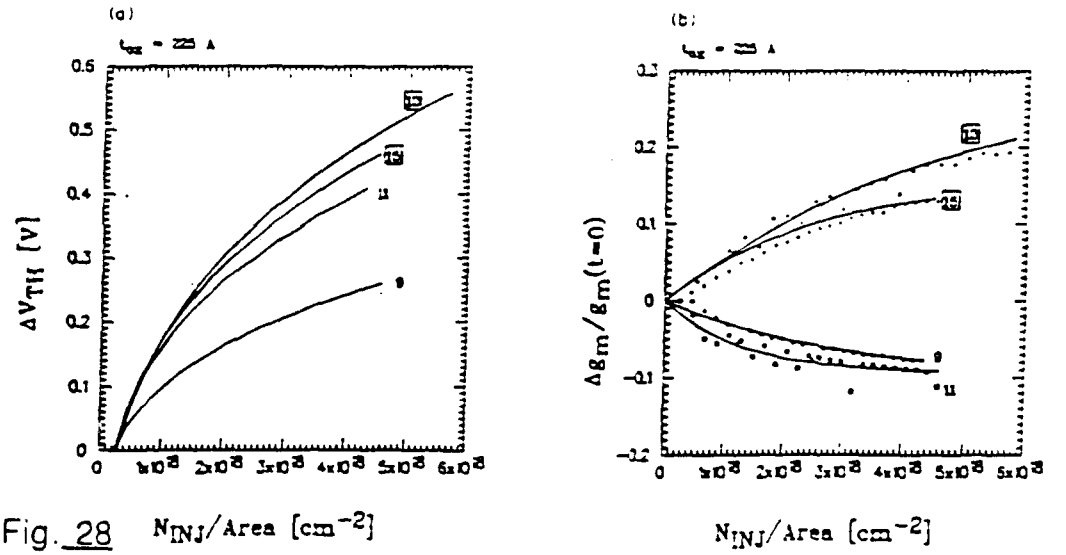


Fig. 28

Change in (a) threshold voltage and (b) transconductance vs normalized injected electron density for devices with initial oxide thickness of 225 Å. Devices 13 and 15 were asymmetrically injected; devices 9 and 11 were symmetrically injected.

3.0 OTHER ACCOMPLISHMENTS

In this section we describe the papers published during the previous ONR-SDI program, the graduated Ph.D. students and the Technology Transfer to Industry.

3.1 PAPERS PUBLISHED - ONR CONTRACT

1. U. Sharma, R. Booth and M. White, "Static and Dynamic Transconductance of MOSFETs", IEEE Trans. Electron Devices, Vol. 36, 5, May 1989.

2. U. Sharma and M. White, "Ionizing Radiation Induced Degradation of MOSFET Channel Frequency Response", IEEE Trans. on Nucl. Sci., Vol 3, June 1989.

3. U. Sharma, R. Booth, and M. White, "A Time-Dependent Parameter Acquisition System for the Characterization of MOS Transistors and SONOS Memory Devices", IEEE Trans. Instr. and Meas., Vol. 38, 1, March 1989.

4. A. Roy, F. R. Libsch and M. H. White, "Electron Tunneling from Polysilicon Asperities into Polyoxides", Solid-State Electronics, Feb. 1989.

5. A. Roy and M. H. White, "Electron and Hole Charge Separation with a Dual Channel Transistor", 47th IEEE Device Research Conference, June 1989.

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3.2 GRADUATED Ph.D STUDENTS

Anirban Roy, "Characterization and Modeling of Charge Trapping and Retention in Novel Multi-Dielectric Nonvolatile Semiconductor Memory Devices", 1989.

Frank Robert Libsch, "Physics, Technology and Electrical Aspects of Scaled MONOS/SONOS Devices for Low Voltage Non Volatile Semiconductor Memories (NVSMs)", 1989.

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Umesh Sharma, "An Investigation of Ionizing Radiation Induced Charge Trapping and Interface Trap Generation", 1989

3.3 Technology Transfer to Industry

In this past program we were able to transfer nonvolatile semiconductor memory to several companies. In particular, Westinghouse Electric Corp. in Baltimore, MD. has received cooperation and information with regards to the scaling of SONOS device structures. The optimum selection of insulator thicknesses combined with techniques of characterization (e.g. the linear voltage ramp and pulsed C-V methods) are typical areas of technology which have been transferred to Westinghouse. There have been joint efforts to understand the effects of scaling nonvolatile memory devices to the extent Westinghouse will often perform special operations (e.g. hydrogen annealing) to work in a collaborative manner. For example, Westinghouse recently provided Lehigh with custom photomasks to permit the fabrication of p+ gridded wafers for C-V evaluation. Another example of technology transfer is with SIMTEK Corp. in Ft. Collins, CO. where we have started a program of technology transfer to enable SIMTEK to scale their SONOS devices to programming voltages below 10V. Westinghouse is primarily a military supplier of custom I.C.'s while SIMTEK is more focused on the commercial I.C. arena.

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8.0 The Sherman Fairchild Microelectronic Research Laboratory

The Sherman Fairchild Center for Solid-State Studies was established in the Fall of 1976 with a $5.2M grant from the Sherman Fairchild Foundation to provide an interdisciplinary staff of faculty and students for research in solid-state. A central theme of the Center is the nature and role of defects in insulators and semiconductors. A description of the grant reads, "..to strengthen and further develop a program of excellence in solid-state education and research for both undergraduate and graduate students..". Today, the Sherman Fairchild Center is characterized by 15 interdisciplinary faculty and 30 graduate students in solid-state studies. There are 3 endowed chairs (physics, materials science and electrical engineering) held by George Watkins, Ralph Jaccodine and Marvin White, respectively. Fig. 1 illustrates the Sherman Fairchild Center of Solid-State Studies.

Fig. 1 Sherman Fairchild Center
for Solid-State Studies

Inside the Sherman Fairchild center there exists a 3,000 sq. ft. Microelectronics Research Laboratory (Class 10,000 open spaces with Class 100 workstations) with a primary emphasis on CMOS I.C. technology. The initiation of a design begins with simulation programs (e.g. SPICE, SUPREM, PISCES..etc.) resident on the Center's SUN Workstation Network. The layout and design is accomplished with 3 SUN SPARC Workstations using Mentor Graphics GDT design tools. Fig. 2 shows the SUN SPARC Workstation/Network Server, a SPARC Station IPC, both equipped w/color monitors, and a SPARC Station SLC.

Fig. 2 SUN SPARC 1 Workstations

Fig. 3 illustrates a CMOS test vehicle with micrometer feature sizes fabricated with ion-implanted, n-well technology and polysilicon gate electrodes. The test vehicle serves as a multi-project chip with students participating in the design and layout of the mask set. The chip is fabricated with a 9 mask photolithograph set including 'scratch-pad' protect. This technology has been employed in the past few years for such projects as CMOS transistor modeling of threshold voltage, transconductance, mobility, output conductance, and propagation delay characterization. In addition, low temperature device studies (1.7K-300K) are performed with this mask set. With the addition of other masks to the basic sequence, we have fabricated CMOS operational amplifier-pH sensor systems and studied nonvolatile semiconductor memory devices. The CAD software of the SUN SPARC Station post-processes for the EBES (Electro-Beam Exposure System) which generates 4" chrome working plates for 3" silicon wafer processing.

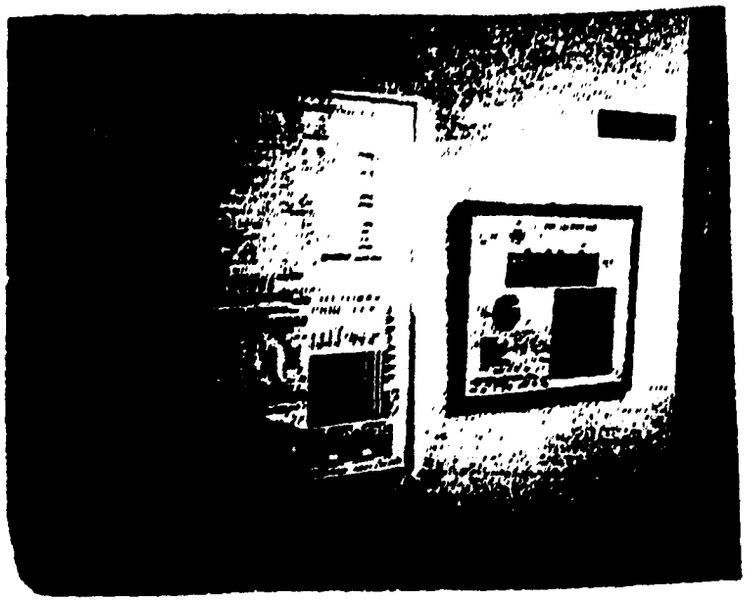

Fig. 3 CMOS Multi-Project Chips n-well.
3 micrometer feature sizes (11.3mm x 11.4mm)
9 mask steps

The photolithography consists of positive resist and the following contact aligners, shown in Fig. 4, 1) two Cobilt 400's, 2) a Karl Suss MJB3 equipped for a resolution of 0.6 micron, and 3) a Research Devices infrared aligner. Fig. 5 illustrates diffusion furnaces for boron and phosphorus and oxidation furnaces. Fig. 6 shows the custom low-pressure chemical vapor deposition system (LPCVD) which is employed for the polysilicon, silicon nitride, and low temperature oxides. The combined LPCVD/plasma etcher and deposition system is computer-controlled with a microprocessor board serving as a smart peripheral to an HP-85. Menu-driven programs in BASIC permit education and research to be carried out on multi-layer films of variable composition and thicknesses. A typical SONOS structure for nonvolatile semiconductor memory research may require a nitride thickness of 50 to 100A with graded composition. Fig. 7 illustrates a RF magnetron metallization system employed in the CMOS fabrication sequence. Fig. 8 illustrates a 3-wall gate oxidation furnace to prepare defect-free oxides by removing ionic contamination. Fig. 9 shows the 205 KeV Extrion ion implantation system for the multiple implants.

Fig. 4 Photolithography

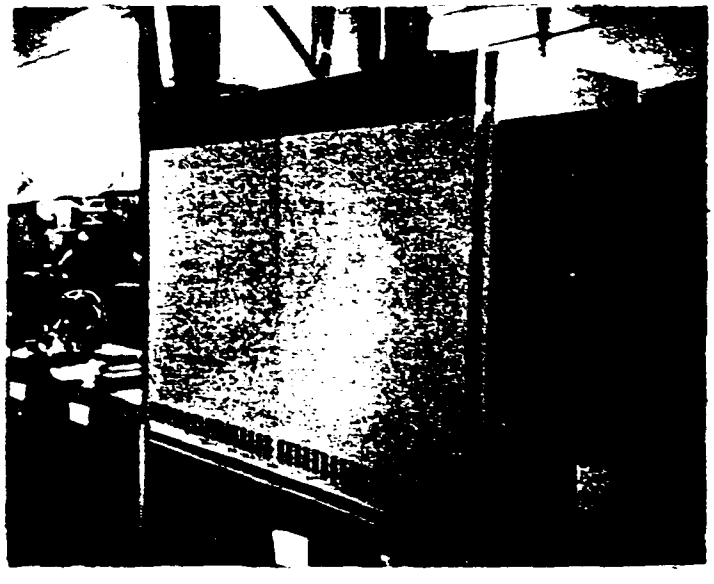

Fig. 5 Diffusion and Oxidation Furnaces
(Boron and Phosphorus)

Fig. 6 Custom LPCVD/Plasma System

Fig. 7 Metallization

Fig. 8 Custom 3-Wall Oxidation Furnace for Defect-Free Gate Insulators

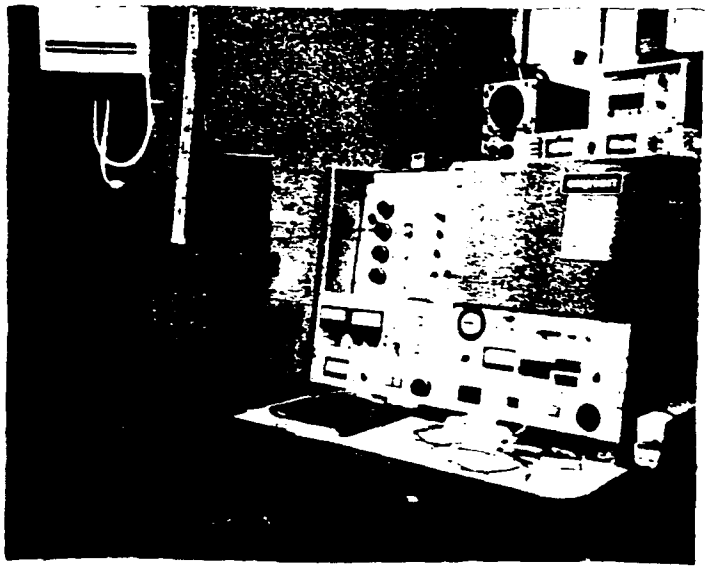

Fig. 9 Ion Implantation System

Analytical characterization of microelectronic devices is performed with a Scanning Electron Microscope (Fig. 10) and a High Resolution 300KV Scanning Transmission Electron Microscope (Fig. 11) to obtain atomic resolution of interfaces.

Fig. 10 JEOL 840F High Resolution SEM

Fig. 11 STEM Philips 430

After the device structures are fabricated they are characterized with a computer-aided date acquisition system. The basic system uses HP-9836 and HP-900 microcomputers with IEEE 488 (HP-IB) peripherals for data acquisition, analysis and display. Fig. 12 illustrates the HP-9836 operation with a probe-stand, and RK-81A semi-automatic prober, and an HP-4145 Semiconductor Parameter Analyzer. The software is a menu-driven TECAP program which has been customized to serve the needs of the laboratory. Fig. 13 illustrates another HP-9836 computer interfacing with an HP-3577A Network Analyzer and Tektronix-7854 digitizing scope for high-speed and high-frequency analysis. The low temperature measurement system (1.7K-300K), seen in Fig. 14 consists of a Janis Helium dewar, an Air Products Cryo Pump, and a 4K Gauss electromagnet. Charge pumping measurements on MOS transistors are made at various temperatures using the HP8115A dual channel pulse generator and a Keithley 616 electrometer under menu driven control from an HP9000 computer.

Fig. 12 Computer Aided Data Acquisition
and Modeling (HP-9836, HP-4145)

Fig. 15 shows the various C-V measurement methods we exercise in examining the quality of dielectrics and interfaces. Quasi-static C-V measurements are made with an HP8116A function generator and a Keithley 616 electrometer. Arbitrary frequency C-V is accomplished with an HP4192A impedance analzer and an HP4280A C-V meter. High temperature C-V capability (300C) is useful to track the quality of contamination control in our processing. Custom built pattern generator and threshold detect circuitry, seen in Fig. 16, is used to monitor developments in our non-volatile memory research.

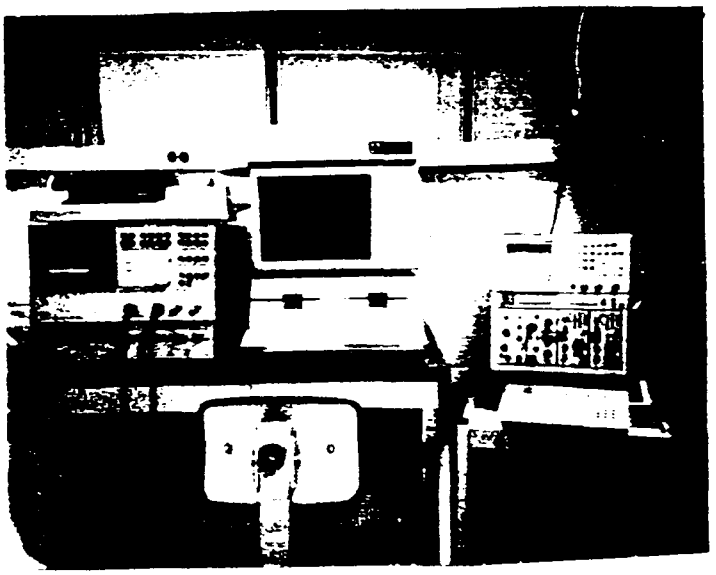

Fig. 13 Computer Aided Data Acquisition (HP-9836, HP-3577A, TEK-7854)

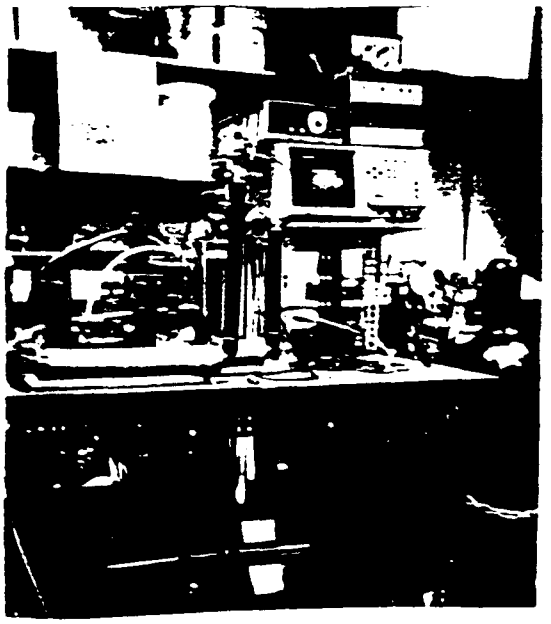

Fig. 14 Shows a cryoelectronics research station for low-temperature device characterization

Graduate student research in microelectronics is an interdisciplinary approach as each student uses and develops simulation programs to characterize the device-technology interface, designs and lays out test device structures (sensors, devices, circuits), fabricates the structures, and performs test and evaluation with computer-aided data acquisition and analysis. The total experience, namely, design-simulation-fabrication-test, is the core aspect of our microelectronics program, and within this framework each student selects a control theme. For example, a student may wish to concentrate on the device-technology interface with studies of hot carrier injection; however, the study may involve unique test structures and circuits on the chip. Another student may wish to examine the device-circuit interface with studies in nonvolatile semiconductor memory devices and erase/write/read operation. A particular thesis will generally involve all of the above aspects, however, the student will concentrate on a particular area.

A 'hands-on' graduate laboratory course (Advanced Microelectronics Fabrication Laboratory) exposes the graduate students to safety procedures, chemical cleaning methods, photolithogrpahy techniques, oxidation and diffusion, plasma etching, LPCVD of polysilicon and silicon nitride, ion-implantation, metallization, and chip separation packaging. In this course, the students perform a complete CMOS fabrication sequence with in-process simulators (SUPREM), and final evaluation of process monitors and devices.