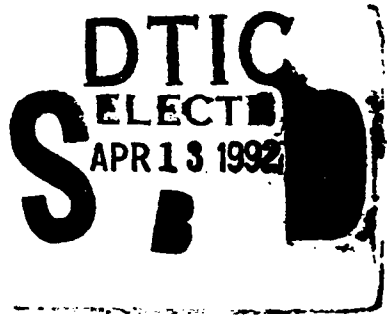
RL-TR-91-359
In-House Report
December 1991

AD-A248 602

VARIABLE HOLD TIME IN DYNAMIC RANDOM ACCESS MEMORIES

Daniel J. Burns. Wilmar Sifre, Mark W. Levi



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92-09309

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REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

Public reporting burden for this collection of information is estimated to average 1 hour per response, including the time for reviewing instructions, searching existing data sources, gathering and maintaining the data needed, and completing and reviewing the collection of information. Send comments regarding this burden estimate or any other aspect of this collection of information, including suggestions for reducing this burden, to Washington Headquarters Services, Directorate for Information Operations and Reports, 1215 Jefferson Davis Highway, Suite 1204, Arlington, VA 22202-4302, and to the Office of Management and Budget, Paperwork Reduction Project (0704-0188), Washington, DC 20503.

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	December 1991	In-House Sep 89 - Jun 91

4. TITLE AND SUBTITLE
VARIABLE HOLD TIME IN DYNAMIC RANDOM ACCESS MEMORIES

5. FUNDING NUMBERS
PE - 62702F
PR - 2338
TA - 01
WU - 23

6. AUTHOR(S)
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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
Rome Laboratory (ERDR)
Griffiss AFB NY 13441-5700

8. PERFORMING ORGANIZATION REPORT NUMBER
RL-TR-91-359

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Rome Laboratory (ERDR)
Griffiss AFB NY 13441-5700

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES
Rome Laboratory Project Engineer: Daniel J. Burns/ERDR/(315) 330-2868

12a. DISTRIBUTION/AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)
Unstable data retention time has been observed in small populations of bits in certain dynamic random access memory (DRAM) products. This effect has been called variable hold time (VHT), and it represents a potential soft error failure mechanism. This is especially true for devices with poorly controlled refresh time distributions in situations where system refresh time requirements may be aggressive (eg. at either high temperature where Tref is low, or in a low temperature application which assumes high Tref values). Commonly specified device testing procedures do not determine the distribution of bit refresh times or VHT characteristics, and therefore there is no assurance that VHT soft errors will not occur in use. This report describes testing procedures developed to characterize VHT in DRAMs, and includes test results for a limited number of samples of a few device types. Our test results indicate that generally refresh times are specified conservatively enough, and that VHT instabilities are low enough that no soft errors would be expected in these particular devices. However, at least one device type tested was marginal in this respect, and further study is needed to understand lot-to-lot VHT variations with different manufacturers' materials and processing.

14. SUBJECT TERMS	15. NUMBER OF PAGES
Dynamic Random Access Memory, DRAM, Variable Hold Time, VHT, Refresh Time, Instability, Reliability, Screen	138
	16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	U/L

NSN 7540-01-280-5500
Standard Form 298 (Rev. 2-89)
Prescribed by ANSI Std. 239-18
298-102

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1.0 Introduction

Variable Hold Time (VHT) [1] is a relatively obscure potential soft error failure mechanism in Dynamic Random Access Memory (DRAM) microcircuits. The objective of this report is to describe new device characterization techniques and to provide data needed to assess the significance of the VHT problem for at least a few real world devices. Such data is needed in order to decide whether VHT is a widespread reliability concern in fielded commercial DRAMs, and whether special screening tests for VHT should or should not be required in military specifications for DRAM devices. This work was carried out in-house in the Reliability Physics Branch, Microelectronics Reliability Division, at the Air Force Systems Command's Rome Laboratory, Griffiss AFB NY.

The remainder of this section discusses the Variable Hold Time (VHT) phenomenon, and the only other reference to VHT work we know of, that of Yaney, et. al. [1]. We also review references on refresh time measurement, and Random Telegraph Noise (RTN) in small area devices, a phenomenon probably closely related to VHT. A significant amount of effort went into developing the hardware and software to enable practical, efficient, bit-by-bit refresh time measurements, and into analyzing the massive amount of data which resulted. Sections 2 and 3 of this report discuss this hardware and software, hopefully in enough detail to make it possible for anyone interested in duplicating or extending this work to save considerable time. Typical measurements are also shown in Section 3, and the data analysis procedures we used to extract various parameters are explained. Additional measurement results are shown in Section 4, and Section 5 discusses physical models proposed to explain VHT behavior. Section 6 concerns physical analysis of bit locations which were found to have unstable refresh times. Finally, Appendix A discusses device logical to physical bit mapping, and an optical technique we have developed and used for the first time in our lab for physical bit map verification, an important aspect of producing bit mapped images of refresh time and other parameters considered in this study, and for locating bits on the device for physical analysis.

1.1 Background

DRAM refresh time is generally thought of as a fixed, stable number, however, there is actually a fairly wide distribution of individual bit refresh times in any given part. Further, most bits exhibit continual, discrete 'hops' up or down in refresh time. These hops occur randomly, separated by seconds or hours, and can be a significant fraction (typically on the order of 15%) of the mean bit refresh time. Refresh time specifications must take into account the magnitude of this hopping, especially at high temperatures (where refresh time is lowest), or soft errors may result. At this writing, we believe that there are no electrical tests or screens specified in the MIL-STD slash sheets or on commercial device data sheets which would reliably identify devices with severe VHT bits.

Although static memories find more use in military systems, dynamic memories are being used in important systems. At this writing, little (if anything) has been published regarding VHT in commercially available devices, and discussions with manufacturers have so far indicated a lack of available data. This work was undertaken because we thought that it would be of benefit to not only military, but industrial and commercial DRAM users, and DRAM manufacturers to determine whether VHT is a real threat to reliable performance in critical systems.

A significant difficulty exists in generating VHT data. Measurements to characterize this potential soft error failure mechanism are troublesome, requiring that high temperature refresh time measurements for large numbers of individual bits be repeated and analyzed continually in tests spanning many hours or even days. Commercial memory testers do not appear to provide workable solutions to the problem of tracking the refresh time of very large numbers of individual bits over long periods of time. Conventional ATE could not be used because of the huge amount of continuous test time required. We have found that a generic personal computer (PC) provides a practical, low cost approach to VHT characterization testing. This report describes a unique DRAM VHT testing system we developed to make the required refresh time measurements. A simple hardware modification and appropriate software enables a PC to test individual bit refresh times in DRAMs residing in its own memory space.

We then tested samples of several DRAM types, monitoring bit refresh times and characterizing hopping activity over long periods of time. We found significant VHT activity in all of the samples we tested. Our tests showed that the magnitude of VHT instability was significant compared to the mean of refresh times for all of the devices tested, however, minimum bit refresh times were still large compared to specified limits. At higher temperature one device tested would be marginal, in the sense that the actual refresh time distribution was disturbingly close to the device specification.

We conclude that VHT does not pose a significant threat to data integrity for the devices tested, but we also emphasize that a very limited number of device types, samples, and date codes were tested. Since VHT is present in all devices, we recommend some form of device characterization and monitoring to assure that production devices are free from VHT problems. If it is determined that VHT is unpredictable from lot to lot or wafer to wafer, steps should be taken to identify the processing steps which effect VHT, to understand its causes, and to reduce its incidence. We expect that VHT will continue to be a concern in DRAMs, and in dynamic circuitry in general, especially if cell critical charge decreases in future devices; if low temperature systems are built which attempt to use relaxed DRAM refreshing requirements; and if the current surging interest in semiconductor artificial neural networks spawns high precision analog DRAM storage cells.

Further analysis of data from our testing also leads us to conclude that VHT is caused by a mechanism similar to that proposed to explain small drain current fluctuations (or random telegraph noise - RTN) observed in small area MOS transistors [3,4,5,11].

1.2 Review of References

This Section reviews papers in the literature which seemed relevant to VHT. Although the first reference is the only one we are aware of which treats VHT in DRAMs directly, the waveforms of Tref we measure are strikingly similar to waveforms of fluctuating drain current in small area MOSFETs thought to be caused by trapping at one or a few localized sites.

1.2.1 AT&T VHT Paper (IEDM 87)

Yaney, et al [1] first described VHT in DRAMs, and proposed that it was the spatially-resolved manifestation of burst noise commonly observed in larger junctions. They observed cell leakage current changes up to 10 pa. They monitored VHT in 64K, 256K and 1M DRAMs with planar, Hi-C cells, using a DRAM tester modified to continually retest the refresh time of a single bit, and found that VHT bit refresh times exhibited

activation energies of about 0.2ev compared to 0.6ev or higher for normal bits. They also measured transition, or hop rates at different temperatures, and found their activation energies to be about 1ev. They observed that a thermal "bump" of 150C for 30 minutes made VHT easier to detect, and that VHT was worse for more negative substrate biases. They reported physical analysis which correlated VHT to oxidation induced stacking faults, edge dislocation, epi stacking faults (on epi) and very small defects observable only by TEM. They observed that many bit locations had these types of defects but did not exhibit VHT. They proposed a physical model which involved modulation of (junction) leakage current through a major defect or multiplication center by the change in occupancy of a minor flaw located nearby. Finally, they called VHT a serious problem, requiring monitoring of process induced silicon microdefects, and they called for use of error correction in systems.

1.2.2 DRAM Cell Leakage Current Mechanisms

DRAM cell leakage current mechanisms have been studied [7], and can be distinguished to some degree by determining their activation energies (Ea). They include bulk thermal generation (Ea≈1.12ev), generation in the depletion region (avg Ea=0.56ev), interface state induced leakage (Ea depends on surface state Ea's, but may be about 0.36ev), defect and impurity induced states (Ea=?) and band to band tunneling mechanisms in the Si (very high Ea, temperature independent). Different leakage mechanisms may be dominant in the storage cell area, at the cell periphery and edge of the thin storage cell gate, and in the access transistor gate area and edges. Finally, sub-threshold leakage through the access transistor may contribute. It would seem that tunneling at defects in the overlaying storage gate dielectric would also be a possible contributor.

Reference [2] indicates that when one mechanism predominates,

$$Tref = A(T,V)e^{(Ea/kT)} \qquad \text{(Eq. 1-1)}$$

where
- V = capacitor voltage
- T = temperature (K)
- k = Boltzman's constant
- Tref = refresh time (inverse of leakage current)
- A(V,T) = a slightly temperature and voltage dependent factor
- Ea = activation energy

They observed Ea values 0.56 ev for thermally generated carriers in the bulk Si near the storage cell depletion region, 0.36 ev for surface state induced leakage current, and much higher values of Ea at very low temperature, where tunneling mechanisms predominate. In the case of thermal generation in the bulk Si they used A(V,T)=T^2.0 [2], and 1.5 in another reference. Reference [8] points out that bulk and surface state related leakage currents exhibit different dependencies on substrate doping as well.

1.2.3 Alpha Particle Irradiation

It would seem that alpha strikes which produce less than the critical amount of charge required to cause a bit error would mimic VHT. However, the most significant VHT behavior is confined to a subset of bits which exhibit temporarily lower or higher refresh times repeatedly. This is not consistent with single event, random location alpha hits. The devices we tested had alpha protection die overcoats.

It is interesting to note that reference [9] points out that DRAM refresh time may be degraded by alpha particle hits [10], however, the rate of degradation is extremely low. They indicate that for a cell with a pre-irradiation leakage current of 4.2E-5 pa/um^2 the average value of increase in leakage current is 8.89E-5 pa/alpha. The cell leakage current for the devices tested at 85C in our study can be estimated from

$$q = CV$$
$$\text{or} \quad i*t = CV$$
$$i = CV/t$$

where q = charge
i = current
C = capacitance (e.g., 50e-15f)
V = voltage(e.g., 5 v)
t = time(e.g., 1 sec)

$$\text{or} \quad i = 50e\text{-}15f*(5v)/1s$$
$$= 2.5E\text{-}1 \text{ pa}$$
$$= 250 \text{ fa}$$

A typical hop may decrease the refresh time from 1 sec to 0.8 sec, corresponding to a leakage current change from 250 fa to 312 fa. The change is 62 fa, several orders of magnitude larger than that expected from an alpha induced degradation.

1.2.4 Random Telegraph Noise (RTN)

Several recent references [3,4,5,11] have concerned "random telegraph noise" (RTN) which we believe is related to VHT. Very small variations or fluctuations in small area MOSFET drain current are thought to be caused by single traps or groups of traps populating and depopulating. They indicate that for a small area channel (< about 1 sq um) it is possible to have only a single oxide trap in the vicinity of the surface Fermi potential over the entire channel area, and that capture and emission of a channel carrier by the trap results in a modulation of drain current. This represents a noise source for very small transistors or for any size transistor which relies on very small off state leakage currents (as does a DRAM storage cell). These references are generally trying to sort out the place and nature of the traps, whether they are in the silicon, at the interface or in the oxide, and whether they act together in groups. The characteristics of RTN drain current waveforms are similar to VHT Tref waveforms.

We see statistics of high and low refresh time which are similar to those reported for low and high drain current in RTN. We also realized that our measurements are not always fast enough to resolve every hop. At times we had a minimum hop duration resolution of as long as 700s (operating with floppy drives only). This was due to about 1 second of data analysis overhead at each of the 100 steps in refresh time, plus drive accessing to store and retrieve three 64K files. Operating with a hard drive holding the large files decreased the overhead time somewhat, but we undoubtedly were not recording good data on frequently hopping bits. Running the test program with only one step, or a just few steps, lowered the time resolution to only a few seconds. A limited amount of testing was done under those conditions (see Section 4). In those cases one can observe only bits which happen to hop back and forth across one of the few step boundaries. In principle, it should be possible to reduce the test time further by storing the data in memory most of the time rather than on disk. This would eliminate disk accesses and speed up testing greatly. Our system has only 128K of RAM.

1.2.5 Berkeley RTN Paper (IEEE Trans on ED June 1989)

Hung, et. al. [6] described an automated system for making direct measurements of low level leakage current in small channel area transistors. Drain current fluctuations of up to 1% were observed. They showed that the probability distribution of the high and low level drain current level durations is fit by an exponential distribution indicating random trap capture and emission processes. The distribution was of the form

$$P(ton,toff) = 1/(<ton,toff>)e^{(-ton,toff/<ton,toff>)} \quad \text{(Eq.1-2)}$$

where ton and toff are high and low drain current state durations

P(ton,toff) is the probability of high or low state durations

<ton> is the average on state duration

<toff> is the average off state duration.

They observe that RTN can be completely described by <ton>, <toff>, and the magnitude of the transitions (at a given temperature). The first two parameters are extracted from the above plots, and the last is determined from a plot of probability of drain current levels. They also showed that there was Gaussian noise overlaid on the latter plot.

1.2.6 Physical Model Paper

Reference [11] presents a comprehensive model for the generation of RTS waveforms in semiconductor devices. They point to previous work which suggests that RTS currents in MOSFETs are attributed to charge state transitions at traps in the oxide very close to the silicon surface. They report measuring RTS current magnitudes at room temperature of 0.5fa to 100pa in reverse biased diodes and gates of JFETs. They observe that in MOSFETs at low drain voltages, RTS amplitudes are a fixed fraction of mean current as bias and temperature are varied. They have measured characteristic times from 0.1 seconds to 20 hours, and say that these times depend strongly on both temperature and bias, and that the distribution of times is thought to extend down to microseconds. Their measurements showed about 10-25% standard deviations of average transition times, under well controlled experimental conditions. They find that in MOSFETs operating in subthreshold conduction with fixed drain voltages, changes in gate voltage cause characteristic high and low level durations to change in opposite directions, while changes in temperature with fixed voltages cause them to change in the same direction. They say that charge capture by a trap is dominated by a tunneling mechanism, and its characteristic time depends inversely on carrier concentration. Also, they say that charge emission from a trap is temperature dependent. For the case of a conducting channel, traps nearer to the Si/SiO2 interface and in higher field and mobility areas (e.g., . at the drain) have the largest effects. Also, traps in areas of low carrier density (10E7/cm3 to 10E11/cm3) are more likely to have capture and emission times large enough to detect (1s to 100us). In subthreshold conduction, areas close to the metallurgical source-substrate junction, the drain junction, and near the Si/SiO2 interface will have the largest effects.

The authors observe that in MOSFETs in weak inversion, characteristic times do NOT change in the same direction for changes in gate and source-drain bias. This they say

points to capture processes, at traps accessible by tunneling, as the dominant events. We will return to this discussion in Section 5, and try to understand how it applies in the context of a DRAM cell.

1.3 Plan for Experimental Work

As a result of Yaney's paper [1], we decided to do testing on several commercial DRAMs to assess the need for VHT screens in typical devices. We had already been measuring refresh times of large populations of bits in DRAMS for another purpose (to evaluate refresh time as a screen for thin oxide defects).

We obtained samples of typical 64K DRAMs by changing out devices from the motherboards of several PCs, and from contract residue devices being tested for another purpose. We decided to make measurements of VHT behavior at two temperatures for several devices, and see if VHT really did or did not represent a soft error risk, especially at higher temperature. We also planned to do physical analysis (eg., delayering and visual/SEM inspection of hopper bits).

2.0 Alternatives for Making Tref Measurements for DRAM Bits

In this section we briefly discuss hardware alternatives we considered for making refresh time measurements for large numbers of DRAM bits. We also discuss development of the approach we chose, which was based on a generic personal computer. Finally, we discuss temperature control of the DUT, since it was necessary to maintain the DUTs at elevated temperature in order to decrease Trefs and shorten overall test times.

2.1 Hardware Alternatives and PC System Development.

We did not have a dedicated memory tester, and we could not afford the required test time on our automatic microcircuit test equipment. We developed a unique system for making the measurements which uses a personal computer (PC). We thought that it would be particularly attractive to be able to do these measurements in a PC system, with the DUT residing in system memory space, with easy access by software. A quite different DRAM Tref measurement approach using a PC has since been reported in reference [2]. It uses port bits to supply control signals to the DRAM device, which significantly limits the speed of testing (and difficulty of test programming) because several output instructions are required to read or write a bit, rather single MOV instructions.

We found that with very simple hardware modifications, and appropriate software, it was indeed possible to make Tref measurements on DRAMs in a PC's main memory space. We plugged the DUT into a modified, piggybacked socket which was in turn plugged into a DRAM socket on the memory area on the PC's motherboard. Our initial attempt at implementing the Tref measurement involved gating off the active low ROW ADDRESS STROBE (RAS') to the DUT, but only when the system presented a specific row address to the device. This required sequential testing of each row at several Trefs to establish the Trefs of all bits in the device. The gating signal and the row address to be tested were supplied by output port bits to a word comparator and gating circuit. Actually, rows would be tested in pairs, since refreshing a bit on row 0 really also refreshes all bits on rows 0 and 128, etc. in the DRAMs we tested. The software for controlling this

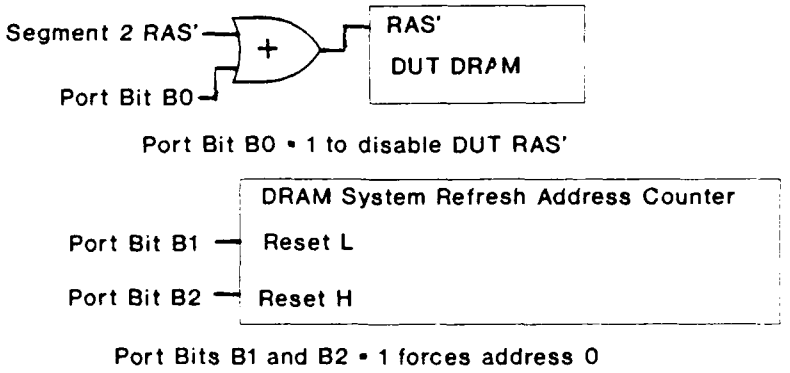
testing, and for analyzing the measurement data included an assembly language test routine linked to a compiled basic program.

The main complication with this first approach was that our PC system had very limited memory (128K). The Tref testing would render the memory segment containing the DUT unusable during testing times. Although the assembler, linker, and loader could be controlled to produce a code which did not load into the segment of memory where the DUT resided, we could not find adequate ways to control the basic language's use of memory for variable and string space well enough to keep the system from using the DUT. We did not need the DUT space for performing the measurements or keeping data (since only two rows of bits were being tested at once, but the system unpredictably used the DUT, and when it happened, the system crashed. A workable solution was found, which involved pre-storing and restoring the two rows of bits which were to be tested. Since the addresses of the 512 bits which were going to be lost during testing were known, they were read and stored temporarily in a safe buffer away from the DUT. After testing was complete, the lost bits were restored from the buffer to the DUT, before returning to the BASIC portion which needed this data. The core of the test algorithm and the temporary buffer was located at specific absolute memory locations out of the DUT.

Our first DRAM bit Tref measurements were actually done in this way. However, the test time for testing hundreds of rows at several Tref trial values to obtain reasonable precision was impossibly long. To be practical, all rows in the DUT had to be tested at the same time. Some evaluation of time saving row-by-row algorithms was done. The most obvious and easiest to program algorithm is a simple series of evenly spaced Tref trial tests over a fixed range of Trefs, during which those bits which fail first at each step are noted. We did simulations of other binary search algorithms that would isolate several unknown Trefs in multiple variable ranges. None of these gave drastic improvements over the stepped trial method. Some of these problems actually could have been solved by using a machine with much more memory installed. But a much more straight-forward solution in any case would be to adopt a software implementation running totally in assembly language.

In our second approach we coded all the test control and preliminary data analysis and data storage in assembly language rather than linked assembly and BASIC. A new approach was also incorporated which allowed testing all bits at once. This did away with the address port and comparator. The hardware for this approach is shown in Figure 2-1. The RAS' gating used only one two-input OR gate. We also lifted two pins on ICs in the PC's DRAM Controller Refresh Address Counter and connected them to I/O port bits. The operation of this circuit is as follows.

Figure 2-1. Hardware for Tref Measurement System Using PC



The DUT DRAM RAS' signal is OR'ed with a port bit. When the port bit is at logic 0 the DUT can be written and read by MOV commands in software running on the PC system. When the port bit is at logic 1, RAS' is held from the DUT. This allows pausing for controlled periods of time without refreshing the data in the DUT in order to test refresh time. We found that the Tref measurements obtained with only this RAS' gating control sometimes contained partial rows of higher values. We might not have realized this, except that we were also looking at physically bit mapped displays of the data. We were seeing several rows with groups of closely spaced high Tref values, and they were not always in the same rows. Possibly when the device was read out after a long pause with no refresh, the data readout circuits or address input buffers and decoders would not begin functioning correctly until a few bits had been read out. The addresses of the first few rows refreshed when coming out of the pause varied because the system refresh address counter was always running and could be anywhere.

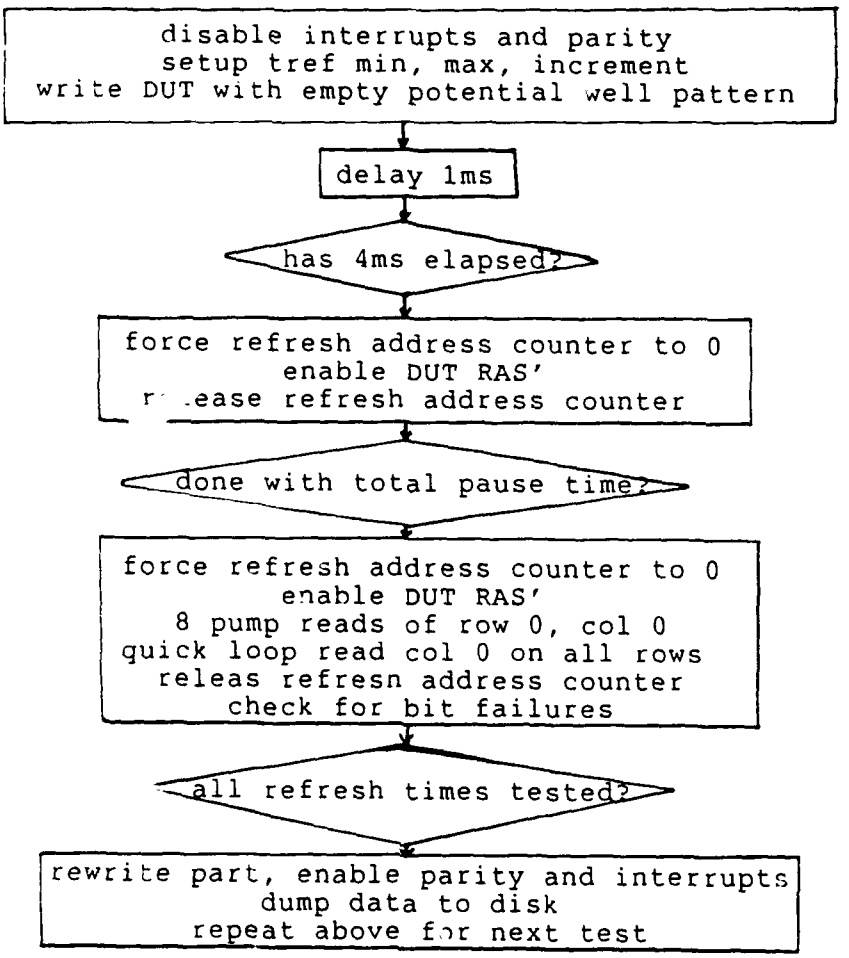
To cure this problem, we added control of the refresh address counter by connecting programmable port bits to its reset pins. As an added precaution, we tried to keep the DRAMs internal circuitry 'alive' during testing, by doing a 'sneak read' of one bit (row 0, col 0) every 4 milliseconds during the refresh pause. This actually refreshed all the bits on rows 0 and 128, so all data on those rows would be lost. Actually, it is possible to do the sneak read on any bit, and lose data on some other two rows. We chose to just ignore the data for the two refreshed rows, rather than doubling the test time to pick up measurements for bits on the refreshed rows.

To do the sneak read, RAS' to the DUT must be enabled for just a few microseconds. We suspected that occasionally the DRAM system refresh controller might do a row pair refresh event during this time. This could not be prevented, but the potential problem (refresh of rows other that 0 and 128 in the DUT) was avoided by resetting the refresh controller address counter to address 0 and holding it during the sneak read. This was accomplished by connecting two port bits to the DRAM system refresh address counter reset pins. When they are high, the system refresh address counter is forced to address 0, and held, even if there is a clock pulse to the counter. We also added 8 pump reads of bit 0 before testing the memory after the pause.

In addition, the software must also disable system interrupts during the entire testing process, since interrupts could conceivably lead to unpredictable attempts to use the DUT, or portions of memory we were using to store and process data. A flow chart of the final test procedure is shown in Figure 2-2.

The sneak read of one bit with the system refresh address counter forced to address 0 alters the PC's normal DRAM refresh action sequence for the entire PC memory, including the memory segment where the test program is stored and where the measurement data is stored. Effectively, every 4 ms the normal refresh sequence is stopped with the address counter at some unknown address, held up for a few microseconds, and then restarted at address 0. Thus, some rows skip one normal refresh event, and must survive until the next one occurs, never longer than an additional 2ms. Therefore, some portion of the memory experiences at worse a 4ms refresh interval. We found that this had no ill effects in our PC.

Figure 2.2 Tref Testing Procedure Flow Chart.



Once this hardware was working, and we were taking data, we quickly found that the average bit refresh times of almost all the devices we tested were on the order of 1 to 1000 seconds at room temperature. Making several sequential Tref tests, and then repeating it several times would lead to impossibly long test times, even using the second approach described above, which tests all bits at once at each trail Tref. For example, if the range minimum is zero, we can calculate the time required to take 100 sets of measurements, with 100 Tref trail steps, at two temperatures, across a trial range, assuming 2 seconds of test and analysis overhead at each trial, to be approximately (2 temps)*(100 sets/temp)*(100 steps/set)*(2sec+range/2). Table 2-1 shows total test times for various ranges. The times increase if range minimum is raised from 0.

Table 2-1 Estimated Total Test Times

Tref Range	Test Time
1000 sec	116 days
100 sec	12 days
10 sec	1.6 days
1 sec	13 hours

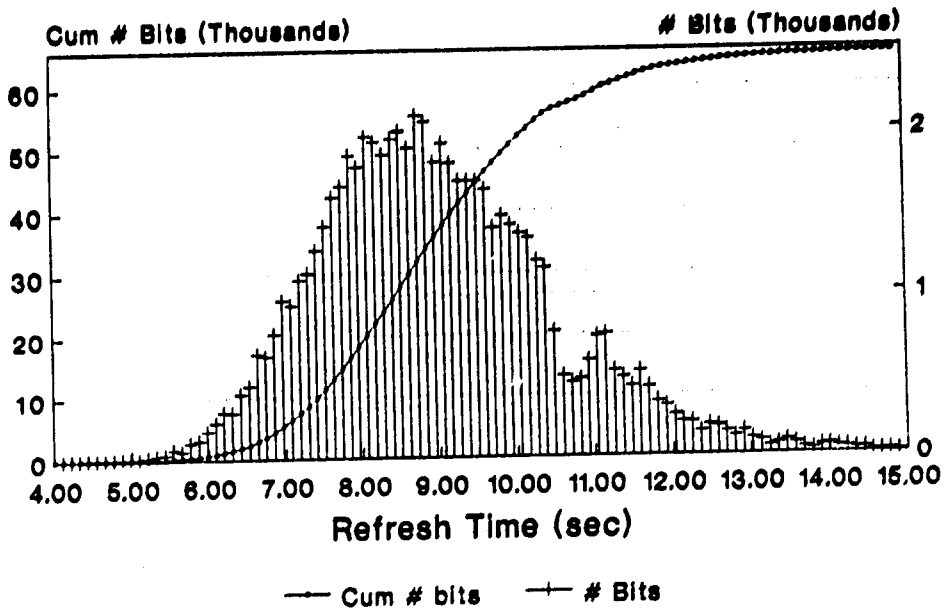
We decided to heat the parts during the measurements to reduce the refresh times to between 1 to 10 sec. This really is undesirable, because we don't have any assurance that the activation energy of the stable and unstable components of leakage current are similar. Therefore, increasing temperature could result in swamping a relatively small unstable component of leakage current with a large stable component. This could force the use of higher resolution steps, which in turn would mean more test time. Another problem is that some of the memories we tested were 70C parts, and actually do not work much above that temperature. Fortunately, it was always possible to find a range of temperatures between about 65C and 90C where refresh times were generally in the range of 0.1 to 10 seconds and where the device still worked.

2.2 Device Temperature Control

To control the device temperature, the socket was enclosed on the top and sides with cardboard backed foam. This shielded it from room air currents and the draft of the cooling fan in the PC cabinet. A heater resistor was placed beneath the socket, between the pins, and a thermocouple wire was placed in a slot in the top of the DUT socket, with thermal grease, in contact with the bottom of the DUT package. The resistor current was controlled by a closed loop temperature controller using the thermocouple sensor. Based on readings of the temperature controller, we believe that our temperature control was much better than 1C, and based on the following discussion, we think that was adequate to study VHT in these memory devices.

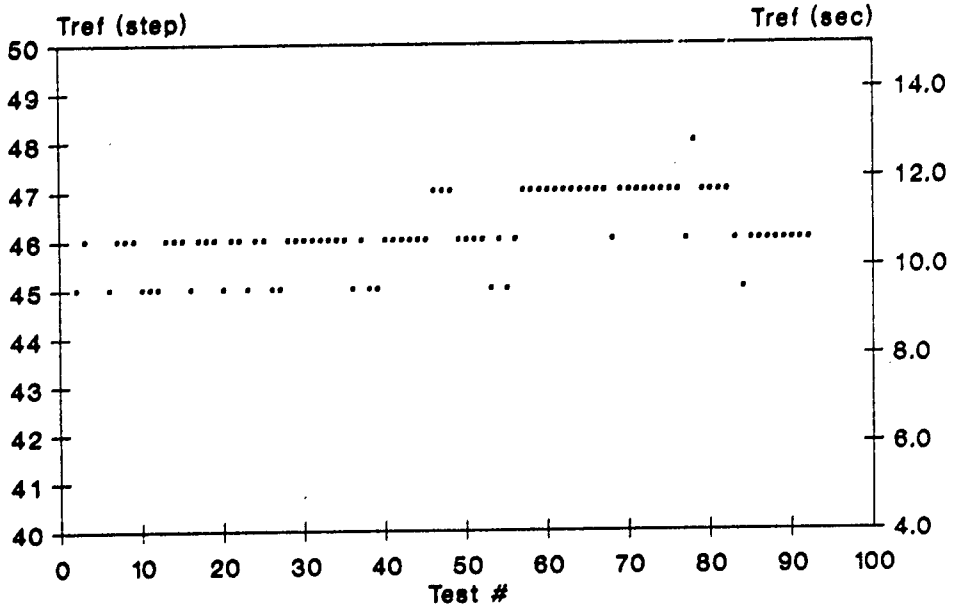
Temperature control is very important in Tref measurements. Activation energies of the leakage current components which determine Tref are expected to be in the range of 0.3-1.12 ev. We needed to choose a step size which was small enough to resolve significant Tref hops, but large enough to avoid measuring too much temperature noise. We had no idea what magnitude of VHT instability to expect, or how much temperature noise there was in the DUTs, so we did some testing. We chose a step size to give us 100 steps, or 1% Tref resolution across the range tested. For example, one test used Tmin=4000 ms and Tmax=15000 ms, and 100 steps of 110 ms each. This resulted in a well centered and covered Tref distribution, and about 2-3% absolute Tref measurement accuracy. An example of the results is shown in the histogram in Figure 2-3.

Figure 2-3. Histogram of Bit Trefs
All Bits, File 1 of Test 94



Bin width is 0.110 sec

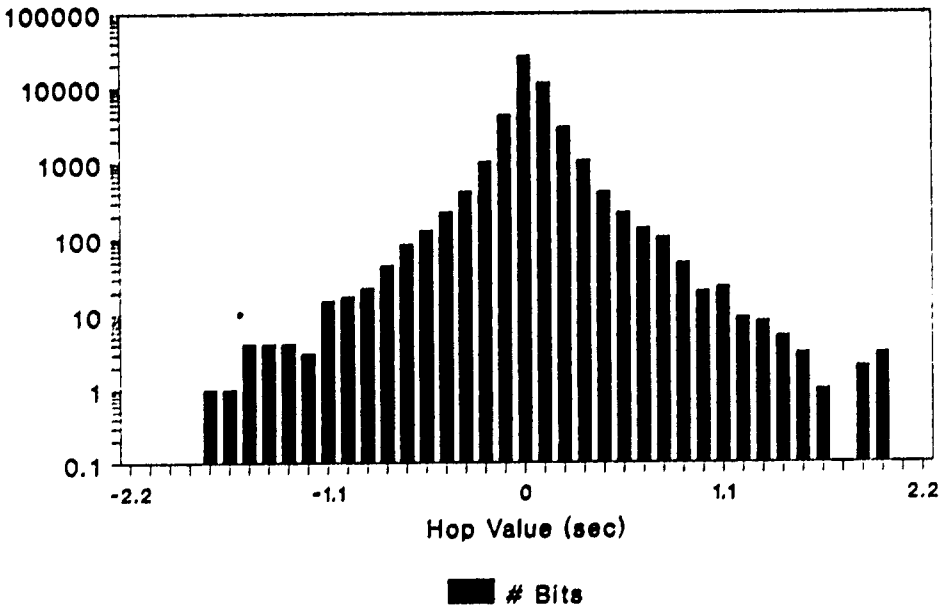
Figure 2-4. Tref Avg vs Test #
Test 94, #327, All Bits



This data resulted from a series of 100 Tref test trials, beginning at 4000 ms and stepping in 100 steps of 110 ms to 15000 ms. This test was repeated 92 times, and the mean of the distribution was calculated each time, assuming a normal distribution. Figure 2-4 shows that the mean was stable to within about +/-1 step stability, except for one point at +2 steps.

If we pick two sequential sets of the 92 tests, and calculate the bit-by-bit differences in Tref between the two sets of measurements, we see that there is quite a bit of instability, or what we call 'hopping'. Figure 2-5 shows a histogram of the bit-by-bit differences between two such tests. Each count in the bins represents a bit which exhibited a Tref hop of the X axis magnitude from one test to the next test.

Figure 2-5. Distribution of Hop Values
All Bits, File 12 of Test 94

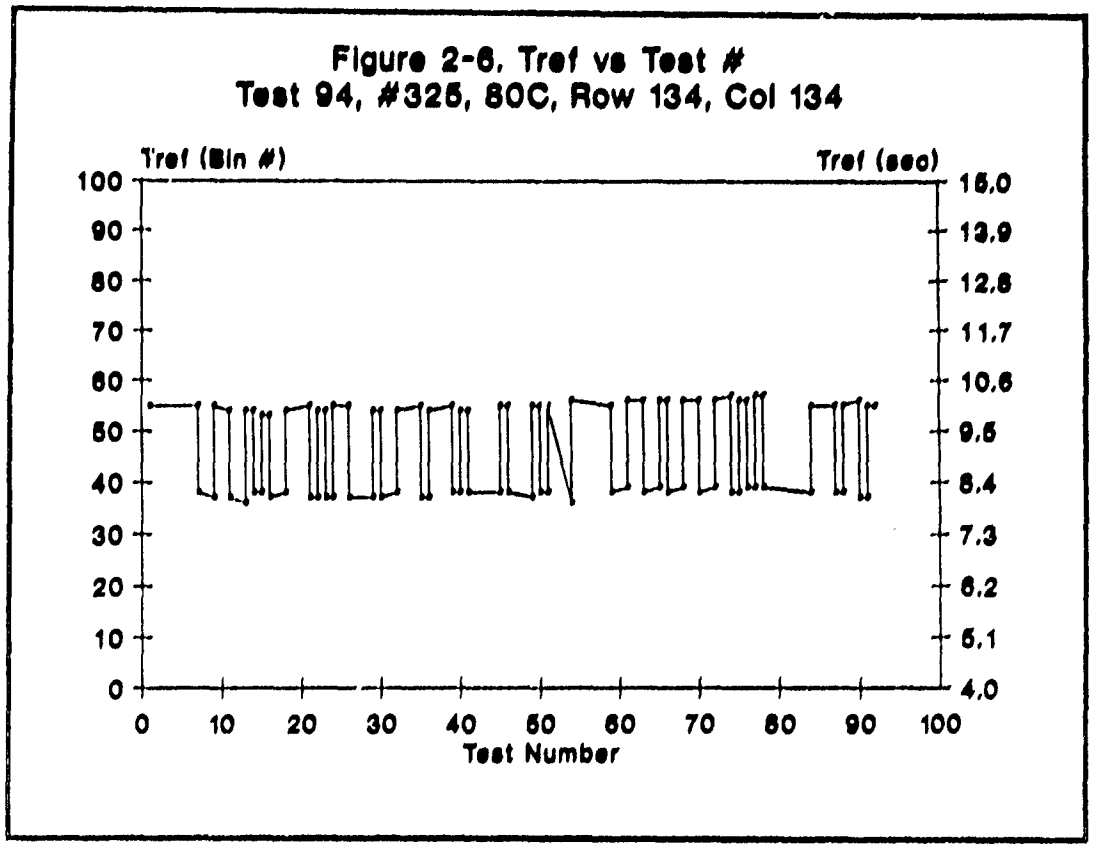


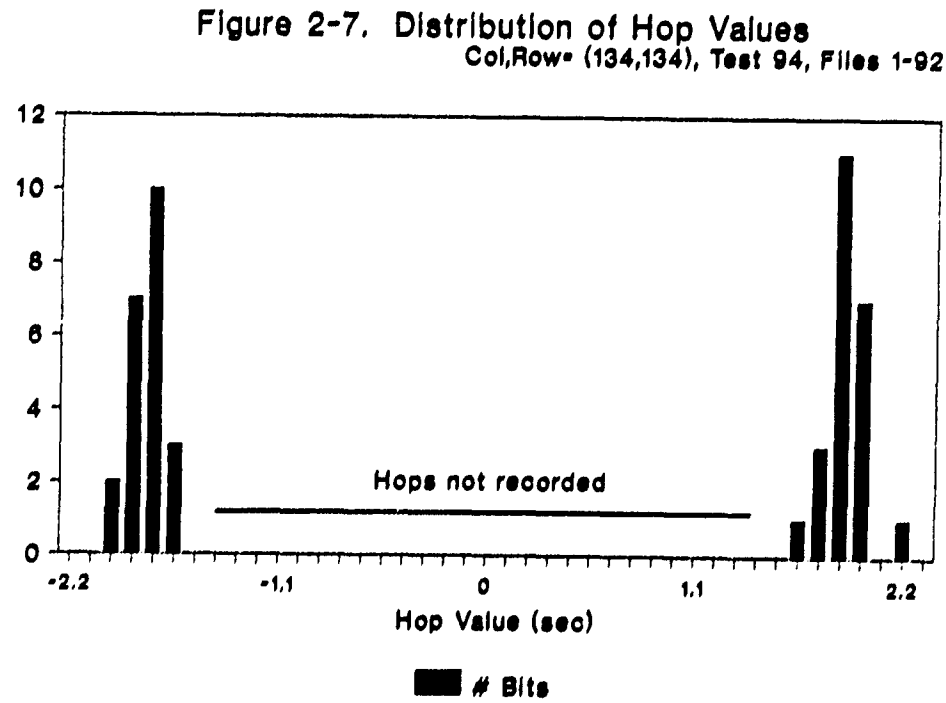
Bin width is 0.110 sec

The distribution of 'hop' magnitudes for sequential tests is continuous, at least for smaller hop magnitudes, and decreasing. Most of the bits are not 'rock stable'. We would like to know how much of the hopping is due to temperature fluctuations, and how much is due to the VHT phenomena. We can make some observations, however.

The first is that it was typical for several thousands of bits to exhibit no Tref step change at all between tests (the middle bin in Figure 2-5). However, we can't prove that these same rock stable bits remained so test after test, because even though we binned and saved this distribution for every set of tests, we only saved the bit addresses of the largest hops (typically those greater than about 10-15 steps). We had chosen to ignore any hops below 13 steps because there were so many that recording them would result in too much data.

A second observation is that the bits which did exhibit large hops, and were recorded, hopped between Tref levels which were themselves quite stable. An example of this behavior is shown in Figure 2-6.





Bin width is 0.110 sec

Figure 2-8. Tref VS Test #
Test 95, #325, 85C, Row 134, Col 134

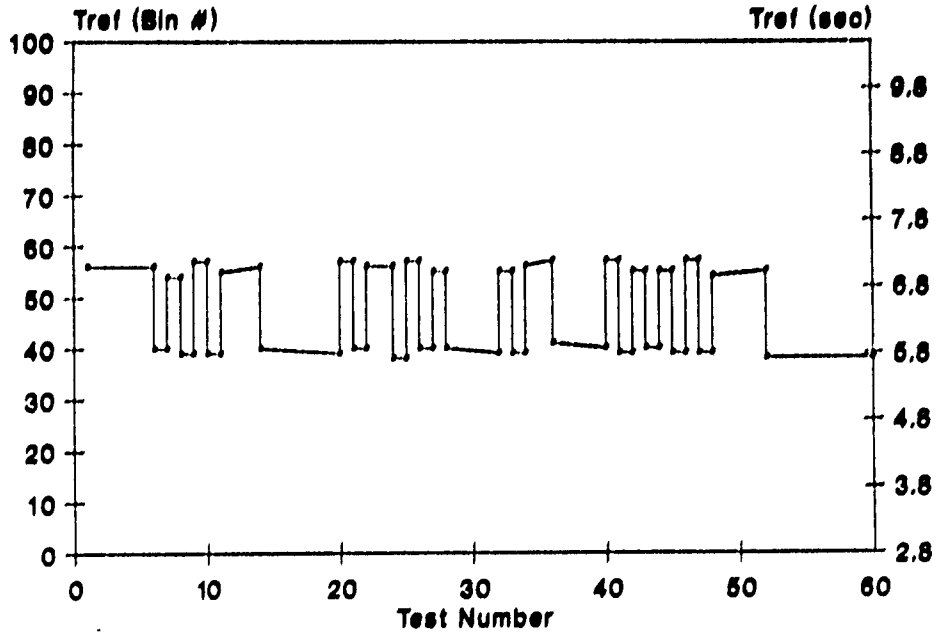
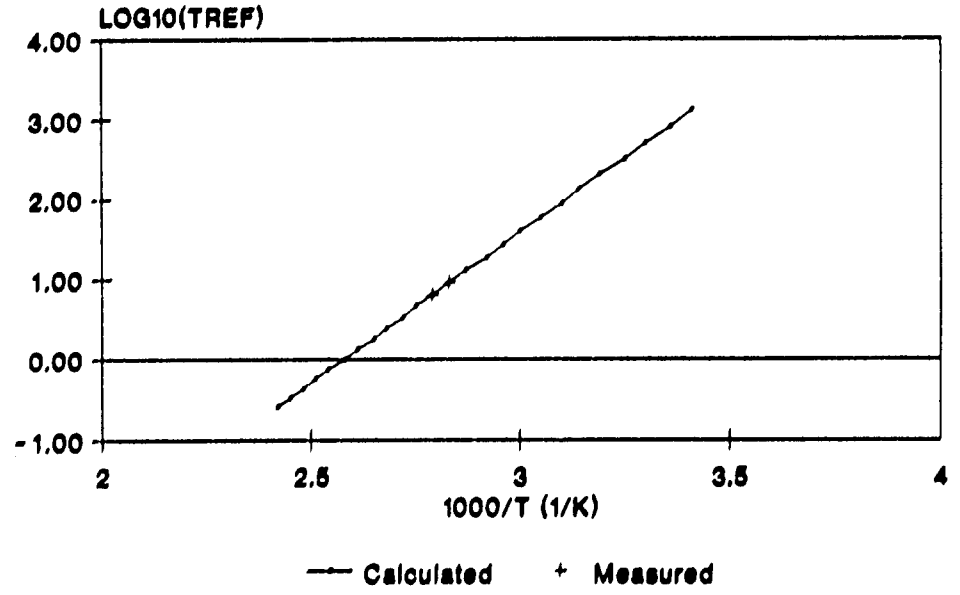


Figure 2-9. LOG10(Tref) VS 1000/TEMP
Tests 94/95, #325, Row 134, Col 134



Ea=0.68 ev

The Tref level measurements shown there track one bit throughout 92 sets of tests done at 80C. This hopping could not possibly be temperature induced, since we find that such active bits are not concentrated together, and their physically adjacent bits are often quite stable.

Another observation about the overall temperature stability of the DUT is based on Figure 2-7, which shows a histogram of high and low Tref levels in Figure 2-6. The middle part of the distribution (X=-12 to +12) is truncated out because hops of magnitude less than 13 were not recorded. Even so, it is clear that the distributions are decreasing toward the middle. This behavior is expected, and has been observed in some of the RTN studies referenced, for example, as shown in Figure 4 of reference [6]. Here it suggests that the variation of Tref measurement accuracy due to all causes is on the order of +/- 2 steps.

It is interesting to consider what magnitude of local temperature variation would be needed to cause Tref changes equal to what we are calling significant hops, in this case 13 steps of .11 sec. Figure 2-8 is the Tref waveform for the same bit as Figure 2-6, but measured at 85C. The arithmetic mean of the waveform in Figure 2-6 (9.07 sec) averages out instability due to both temperature and hopping. The arithmetic mean of the waveform at 85C, in Figure 2-8 is 6.45 sec, and Figure 2-9 shows the log of the arithmetic means plotted against reciprocal temperature. Using Equation 1, we can calculate that the dominant temperature dependent leakage current component has an activation energy of about 0.68 ev, and this was typical for bits in this device. Looking at the data for this plot, we determine that for a Trefavg to decrease from 9.07 sec by our minimum hop value, 13 steps of 110 ms, to 7.6 sec., the temperature would have to increase from 80C to 82.5C, or by 2.5C. Further, the largest hops observed were roughly twice as large, and these could only be explained by a temperature increase to 85.5C, or by 5.5C. We think that local temperature differences of this magnitude between adjacent bits are not probable.

To this point, we have discussed temperature noise with respect to two tests done relatively closely spaced in time (about 10 minutes). We took an added precaution against long term minor temperature drift during long sequences of many tests by calculating the hop magnitude as the difference between the current and the last Tref measurements, rather than the current and the first Tref measurements. We thought this would desensitize the measurements to any large gradual changes in ambient temperature which might effect the DUT temperature, such as weekend building air conditioning cycles.

We strongly suspect that the bits in middle bins of Figure 2-5 are actually exhibiting small hops, and that there is only one or two steps of temperature noise in the measurements between two consecutive sets of tests. We believe that the continuous and decreasing probability of hops of increasing magnitudes is real, and due to a continuous and decreasing probability of defects of increasing severity or location in the device.

We note here that using a 64K memory chip as a test vehicle is a very efficient way to study noise effects of traps in the manner of the RTN references. It is possible to quickly generate a relatively huge amount of data on the distribution of hop magnitudes, duration parameters, and activation energies of Tref and the duration parameters for thousands of trap sites. RTN studies up to this point have been carried out as long tests of individual test samples using sensitive, low-bandwidth current amplifiers. The DRAM approach would probably be most useful in studying very long time constant trapping behavior.

3.0 Tref Testing and Data Analysis Software

This section reviews the software required to run the hardware Tref tests which were described in Section 2. This section also gives a general overview of data analysis, using examples of measurements. Copies of the testing and analysis software can be obtained from RL by completing and mailing in the software request form found on Page 22 of this report. The 8086/8088 assembly language testing programs were run on a Zenith Z-100 computer. The first step of data analysis was done on any MSDOS PC in BASIC. Data archiving and further data analysis was done in FORTRAN on a VAX mainframe.

3.1 General Refresh Time Measurement Sequence

In order to determine all individual bit refresh times, a set of tests is run. The DUT is written with a pattern which results in all empty potential wells. This pattern is computed from data sheet information, and was verified by test. RAS' to the DUT memory is then gated off for a timed interval, and is then restored. The DUT is read out, and failing bits are noted. This test is then repeated, with a slightly longer timed interval. The length of the timed interval is varied over a specified range, using a fixed step size.

The refresh time measurement of each bit in the DUT is represented by a byte in memory. They are initialized to a certain value, and then during testing they are written with the value of the first step number at which each bit fails to hold data. Once tests at all steps across the refresh time test range are completed, the data set is stored, and compared with the previous set. The addresses of only those bits which have changed by a threshold amount from the previous to the current measurement set are noted in a 'hopper' file, and another set is started.

An example of a histogram of a raw Tref data set is shown in Figure 3.1-1. An example of part of a hopper file listing is shown in Table 3.1-1. An example of the histogram of hop magnitudes is shown in Figure 3.1-2a. Figure 3.1-2b. shows the same data on a log Y scale. After some large number of sets has been completed, the temperature is changed and another run is made.

Figure 3.1-1. Bit Refresh Times
#127, 80C, TEST 90, 99 FILES

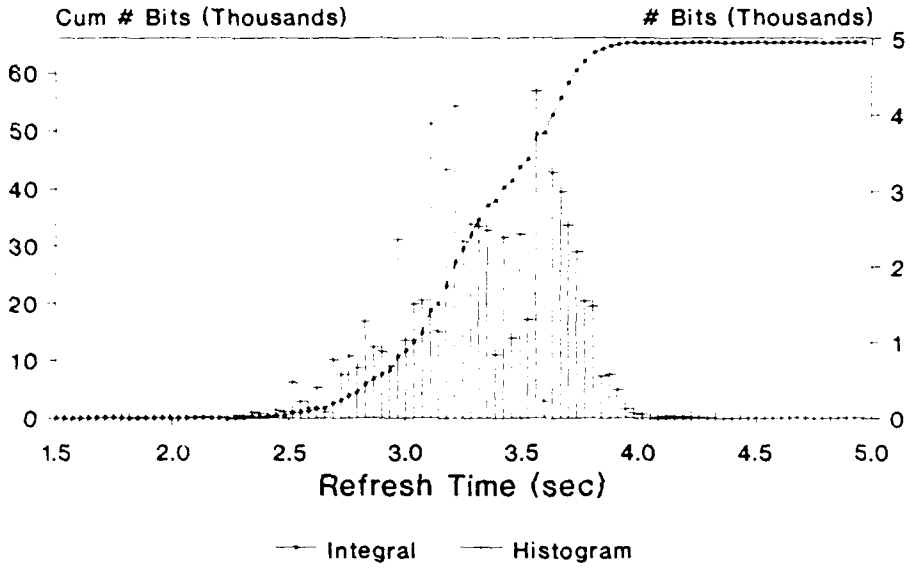
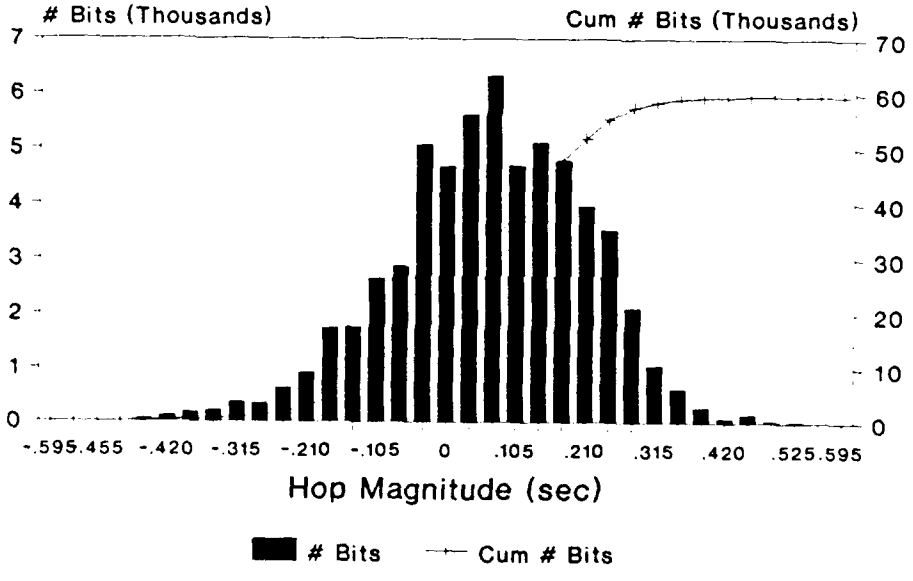


Figure 3.1-2.a. Hop Magnitude Histogram
#127, 80C, Test 90, File 2.



0.110 sec/bin

Figure 3.1-2.b. Hop Magnitude Histogram
#127, 80C, Test 90, File 2.

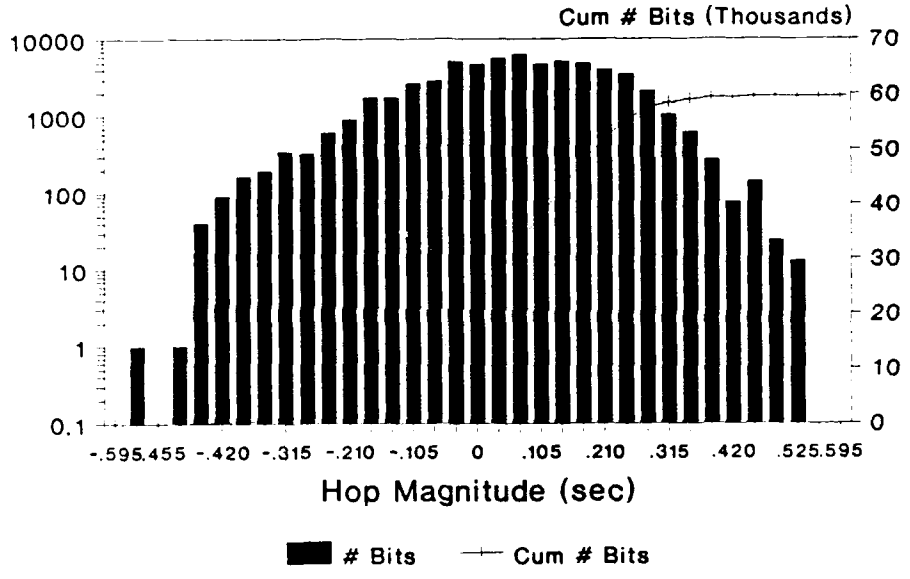


Table 3.1-1. Example Hopper File Listing.
(Translated version of binary file).

```
FILE NAME:H00002.DAT
VHTTHR: 13      TEST NUMBER: 2      # BITS OVER THRESHOLD: 312
  TMIN: 1500          TMAX: 5000                # STEPS: 100
  MEAN: 51         STD DEV: 10
  DATE: 9- 25-90      TIME: 13: 28: 8

(partial listing of recorded hops...)
 COL ROW PRE CUR DIF     COL ROW PRE CUR DIF     COL ROW PRE CUR DIF
   0 135  65  52 -13       0 137  51  64  13       2 152  69  56 -13
   2 198  54  67  13       3 135  65  52 -13       5 183  68  55 -13
   6 152  69  56 -13       6 183  68  55 -13       7 229  61  47 -14
   8 204  52  65  13       8 229  61  47 -14       9 141  42  55  13
   9 229  61  47 -14      10  60  51  64  13      11 133  42  55  13
  11 141  42  56  14      12 135  65  52 -13      12 142  69  56 -13
  13 141  42  57  15      13 229  61  47 -14      14 165  69  56 -13
  15 133  42  55  13      16 137  51  64  13      17 204  52  65  13

+ BINNED DIFFERENCE MAGNITUDES (EXCLUDING ROWS 0 AND 128)
  0:   4666  5611  6317  4683  5103  4764  3943  3509  2104  1041
 10:    617   273    75   143    24    13     0     0     0     0
 20:      0     0     0     0     0     0     0     0     0     0
 30:      0     0     0     0     0     0     0     0     0     0
 40:      0     0     0     0     0     0     0     0     0     0
 50:      0     0     0     0     0     0     0     0     0     0
 60:      0     0     0     0     0     0     0     0     0     0
 70:      0     0     0     0     0     0     0     0     0     0
 80:      0     0     0     0     0     0     0     0     0     0
 90:      0     0     0     0     0     0     0     0     0     0
100:      0     0

- BINNED DIFFERENCE MAGNITUDES (EXCLUDING R0 AND R128)
  0:   4666  5065  2848  2629  1746  1721   904   609   330   347
 10:    194   165    90    40     1     0     1     0     0     0
 20:      0     0     0     0     0     0     0     0     0     0
 30:      0     0     0     0     0     0     0     0     0     0
 40:      0     0     0     0     0     0     0     0     0     0
 50:      0     0     0     0     0     0     0     0     0     0
 60:      0     0     0     0     0     0     0     0     0     0
 70:      0     0     0     0     0     0     0     0     0     0
 80:      0     0     0     0     0     0     0     0     0     0
 90:      0     0     0     0     0     0     0     0     0     0
100:      0     0
```

Table 3.1-2 lists the software used for testing. The main testing task is controlled by setup information edited into a disk file. This file specifies the min and max of the Tref range to be tested, the number of steps across the range, the threshold to define a 'hopper' (in number of steps), a flag to request a file dump of the current set of Tref measurements, and a flag to indicate the device type.

Initially, we estimate the min and max refresh times and run a few sets of tests. We stop the tests and inspect the Tref histogram to check whether the Tref distribution is bracketed by the range minimum and maximum. If needed, the min and max times are adjusted so that the main part of the Tref distribution is spread across steps 20 through 80 of the histogram.

At this time we also inspect the number of hopper bits recorded, and adjust the hopper threshold so that a reasonably small number of bits qualify (typically less than 500 bits, or about half of the maximum size buffer size of 1000 bits). The data from a series of 100 tests at one temperature typically fits on one 5 1/4 inch floppy. We note that the first set of measurements is saved to a permanent disk file, but for subsequent tests, the set of current measurements is stored to another temporary file, which is over-written after each test. This file serves as the baseline for calculating hops when the next test is completed. This reduces the storage space requirements typically by two orders of magnitude or more, but throws most of the raw data away.

Once a run of many tests at one temperature has been completed, the resulting hopper files are collected into one large file. That file is then sorted by col, row, and test number, and transferred to a VAX for analysis. If the large file is too big to be sorted by MSDOS on the PC, it is transferred to the vax, and sorted there. A small portion of such a collected and sorted file is shown in Table 3.1-3. Note there that the bit at col 0, row 135 hopped by at least the threshold amount at test numbers 2, 3, 6, etc. This file is then further analyzed to extract overall population characteristics and to identify individual bits for further analysis.

Table 3.1-2 Tref Test Software

Bracketing the tref ranges:	
PARAMS.DAT	- specifies testing parameters
VHT.EXE	- makes measurements
VHT1.EXE	- translate Tref distribution
DI2.EXE	- inspect Tref distribution
Main testing:	
PARAMS.DAT	- specifies testing parameters
VHT	- makes measurements
Preparing test results for analysis:	
VHT1.EXE	- collects results for several tests
SORT.EXE	- sorts hops by row,col,test for analysis

TABLE 3.1-3 FORMAT OF COLLECTED AND SORTED HOP FILE

COL	ROW	CURRENT TEST #	PREVIOUS TREF MEASUREMENT (IN STEPS)	CURRENT TREF MEASURMENT (IN STEPS)	CHANGE IN TREF (IN STEPS)
0	7	26	69	56	-13
0	10	58	61	48	-13
0	11	19	46	60	14
0	22	48	56	41	-15
0	22	69	43	56	13
0	25	58	45	59	14
0	33	79	60	47	-13
0	43	68	54	69	15
0	46	45	48	61	13
0	52	58	45	58	13
0	129	36	63	50	-13
0	135	2	65	52	-13
0	135	3	52	66	14
0	135	6	65	52	-13
0	135	7	52	66	14
0	135	14	50	65	15
0	135	54	63	50	-13
0	135	74	69	54	-15
0	135	83	50	63	13
0	135	92	51	64	13
0	135	93	64	51	-13
0	135	94	51	65	14
0	136	9	59	43	-16
0	136	10	43	57	14
0	137	2	51	64	13
0	147	3	56	69	13
0	147	9	67	53	-14
0	147	84	69	55	-14

MAILED TO: RL/ERDR (D. Burns)
Griffiss AFB NY 13441-5700

STATEMENT OF TERMS AND CONDITIONS RELEASE OF AIR FORCE-OWNED OR DEVELOPED COMPUTER SOFTWARE PACKAGES

Date_____

1. Release of the following US Air Force software package (computer programs, systems descriptions, and documentation) is requested: VHT Software

2. The requested software package will be used for the following purpose:

Such use is projected to accrue benefit to the government as follows:

3. I/We will be responsible for assuring that the software package received will not be used for any purpose other than shown in paragraph 2 above; also, it will not be released to anyone without prior approval of the Air Force. Further, the release of the requested software package will not result in competition with other software packages offered by commercial firms.

4. I/We guarantee that the provided software package, or any modified version thereof, will not be published for profit or in any manner offered for sale to the government; it will not be sold or given to any other activity or firm, without the prior written approval of the Air Force. If this software is modified or enhanced using government funds, the government owns the results, whether the software is the basis of, or incidental to a contract. The government may not pay a second time for this software or the enhanced or modified version thereof. The package may be used in contract with the government but no charge may be made for its use.

5. The US Air Force is neither liable nor responsible for maintenance, updating or correcting any errors in the software provided.

6. I/We understand that no material subject to national defense security classification or proprietary rights was intended to be released to us. I/We will report promptly the discovery of any material with such restrictions to the Air Force approving authority. I/We will follow all instructions concerning the use or return of such material in accordance with regulations applying to classified material, and will make no further study, use, or copy such material subject to security or proprietary rights marking.

7. I/We understand that the software package received is intended for domestic use only. It will not be made available to foreign governments nor used in any contract with a foreign government.

Signature of Requestor

Name of Requestor

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Name/Title of Air Force Approving Authority

Organization/Location

3.2 Data Analysis During and After Testing

The mean and standard deviation of the current Tref measurements is calculated and stored at the end of each individual test set. Also, the bit-by-bit Tref measurements are binned in histogram style and this data is saved. Finally, bit-by-bit hop magnitudes are calculated and histogrammed for all hops which exceed the specified threshold. This data analysis is very quickly done in assembly language, and is used to generate a quick summary report of hopping activity as a first step in post-test data analysis.

Table 3.2-1 shows the main post-test data analysis and display software elements, and will be used along with examples of their outputs as an outline to explain the data analysis that is done.

Table 3.2-1 Post-Test data analysis and display software

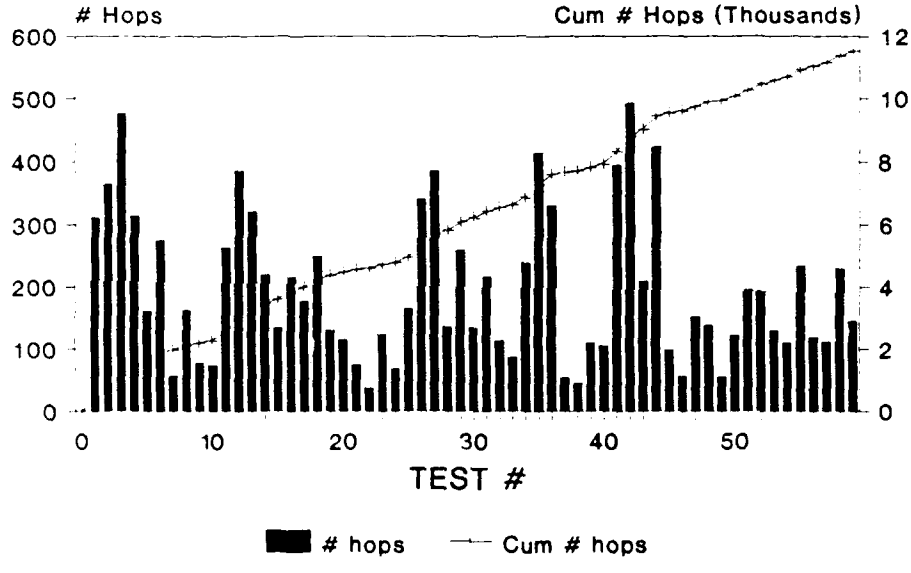
```
Analyzing the data
   analall.com              - control of several sets of cold,hot
     script1.com            - control of one set of cold,hot
       script2.com          - control of one temp
         anal.com           - do analysis of one temp
            file.for        - make tnh,min, bmnh,bmin ,anal.dat files
            anal_bdat.for   - select bits for individual analysis
         transbp.for        - get selected bit tavg, physical x,y
         physloc.for        - make physical map of selected bits
     tea.com                - Ea of average bit refresh time
     bit_tea.com            - Ea's of delected bit avg refresh time
     minmax_tea.com         - Ea's of min and max trefs of selected bits
     join_tea.for           - join Ea plots into 1
     tutds2.com             - fit all tutd plots
     tutds1.com             - select bits for tutd parameter Ea anal.
     join_tutd.for          - join 3 tutd par. Ea plots for sel. bits
     poke.com               - put data in subdirectory
     script3.com            - find and bin Ea's of all hopper bit Trefs

Displaying Data
   DI2.bas                  DUR tref histograms, summaries
   CN.bas                   Images,Tavg

   shohis.for               show various histograms
   cn.for                   physical images of bit parameters
   graph.for                waveforms
   mapper.for               logical to physical bit mapping

   Harvard graphics         used for various charts
```

Once the collected and sorted data file is available, a series of batch files which form and execute these analysis programs is run.

The analysis software was written to analyze data archived for several devices in one run. Therefore there are layers of control 'scripts', which specify a device and temperature for analysis, built around the actual programs which do the analysis.

For each device, at each temperature, a set of histograms and plots can be produced which characterize the Tref times and hopping activity of all the bits in the DUT taken as a population, or of single bits. Figure 3.2-1 through Figure 3.2-9 show examples of these histograms for all the bits in the DUT taken as a population. The remaining figures in this section will show examples of the information extracted from the raw data, including individual bit hop magnitude distributions, average Trefs, Trefavg activation energies, high and low Tref level duration distributions and the activation energies of parameters which characterize them.

Figure 3.2-1. # HOPS VS TEST #
TEST 90, #127, 80C, Files 1-59



ALL HOPS, ALL BITS

Figure 3.2-1 shows the number of bits which exceeded the hop threshold during the first 60 of 99 sets of measurements in what we called test sequence 90 (DUT #127, test temperature 80C). In this plot, one test set took 1221 sec, and 60 tests took about 20 hours. It appears that there may be a slight 3-4 hour periodicity in this data. We could find no apparent reason for this, although we considered that building air conditioning or power line noise might conceivably have been a factor. The DUT was enclosed, well shielded from air currents, and thought to be controlled to better than 1C with a thermocouple and temperature controller. The PC had its own regulated power supply, which supplied the DUT. Noise in that supply coming through from the building power or ground might account for some part of the Tref measurement noise, but we would expect it to be random, not periodic.

Figure 3.2-2 shows a histogram of hop durations for a sequence of tests, taking all hops and all hopper bits as a population. There are many hops which lasted only one test duration. These were initially thought to be more likely to be caused by system noise than hops which persisted for more than one test, so we made provisions and generally did exclude these from data analysis, even though they were recorded in the data files.

The shape of the plot of Figure 3.2-3 was typical, always showing an indirect relation between the number of bits and the number of hops. Many bits had few hops, and few bits had many hops. Note that there are four outlier bits which exhibited significantly more hops than would be predicted by fitting the distribution.

Figure 3.2-4 plots the frequency of occurrence of hops of various magnitudes, for only those hops above the threshold amount, which was 13 bins in this case. There is some question about whether the distribution really is peaked in the middle, or is coming down toward the middle, because we did not record the data on small hops because of our disk size limitation. We suspect that it really is coming down, and this is consistent with the observations of fluctuating drain currents by others. Figure 3.1-2a earlier showed that there is a peak in the middle of the distribution of hop sizes measured between a pair of tests, looking at all bits, not just the active hoppers. We saw many cases where the distribution for one bit was clearly double peaked and not peaked in the middle, and other cases where there were peaks around two positive and negative values. This has also been observed in drain current fluctuation studies, and is thought to indicate the presence of two trapping sites or configurations. Figure 3.2-4 also shows that the high and low values are not really unique metastable values, but form what may be a normal distribution.

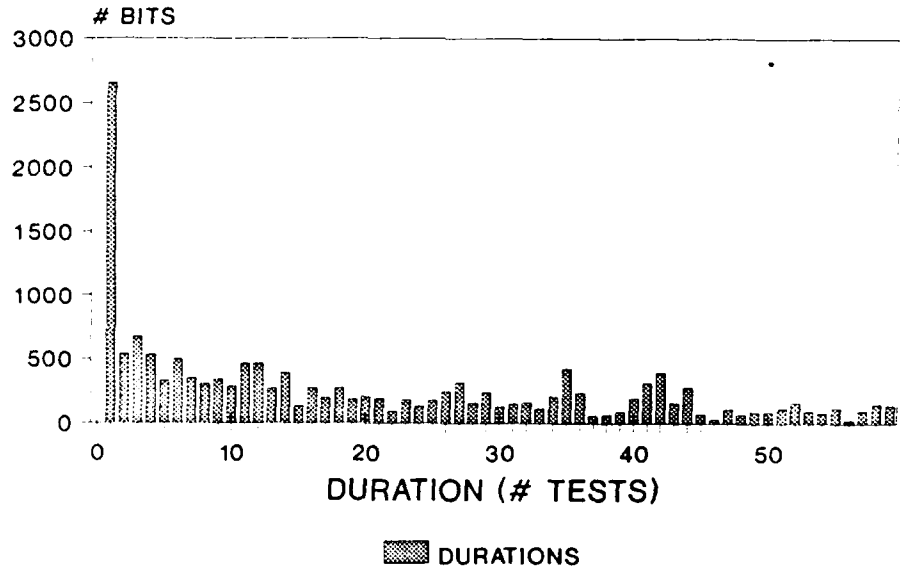
To identify bits which assumed the lowest and highest absolute Tref values during test sequences, we extracted the plots shown in Figures 3.2-5, -6. Figure 3.2-7 is taken from Figure 3.1-1, the initial distribution of all Trefs for this part, but plotted with the same Y scale as in Figures 3.2-5 and 3.2-6 for comparison. Comparing Figure 3.2-5 with Figure 3.2-7, we can see that the initial distribution has more bits at low values than the active hopper low value distribution. This leads to the conclusion that the lowest Tref bits in the initial distribution are not due to severe hopping activity, i.e., they are bits with low values which are relatively stable, rather than active hoppers in their low value state. However, comparing Figure 3.2-6 with Figure 3.2-7, we can see that the initial distribution has fewer bits with high values. This leads to the opposite conclusion that the highest values of Tref in the initial distribution are due to hopping activity, i.e.,. they are active hoppers in their high value state, rather than bits with high values which are relatively stable. Taken together, the data seems to suggest that some factor which decreases Tref value may also decrease the likelihood of hopping. Or, stated another way, some factor which increases Tref may also increase the likelihood of hopping.

Factors which increase Tref, and therefore which could be causing hopping activity, include those which cause higher cell capacitance or charge storage, such as thinner oxide, larger cell area, higher substrate doping density, larger surface state density, wider or shorter transfer gate, and possibly increased surface roughness. On the other hand, there may be no real cause and effect relationship. For example, it could be that regardless of what causes higher cell capacitance or charge storage, the increased density of carriers in a cell with high Tref increases the hopping activity due to some uniformly distributed feature.

Figure 3.2-8 shows a histogram of the ranges of the Tref values of hopper bits for the same bits shown in the previous figures.

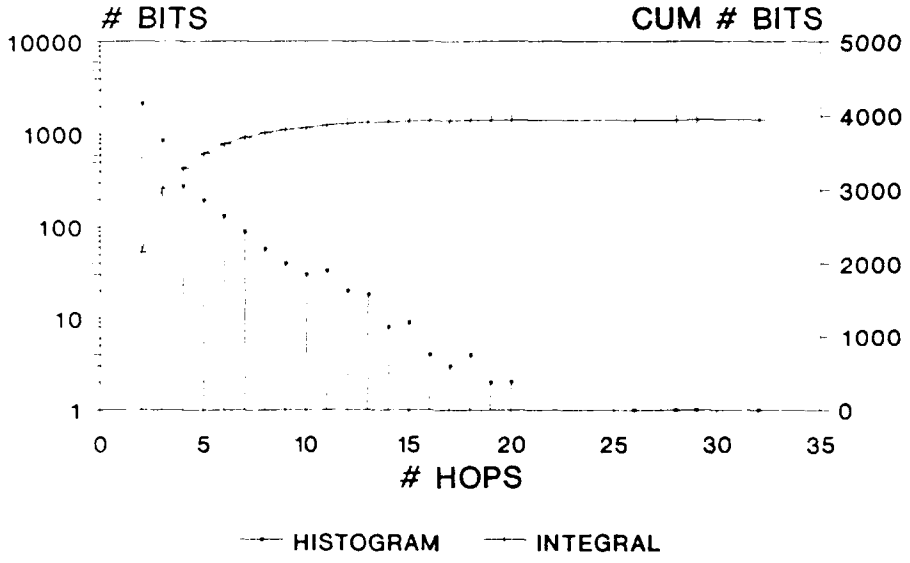
We chose certain bits for further analysis, including some which had many hops, large hops, lowest and highest Trefs, and large Tref ranges. Typically, about 20 individual bits were identified which were the high and low outliers of each those five distributions. Figure 3.2-9 shows a physical location plot which shows where the selected outlier bits were located on the chip. There is some tendency for the active hoppers (TNH-total number of hops) to cluster in the middle of the chip, where the maximum hop values (MHM) also cluster. Maximum hop values, minimum values and high range values are further away from the center, and are more scattered.

Figure 3.2-2. Histogram of Hop Durations
TEST 90, #127, 80C, Files 1-59



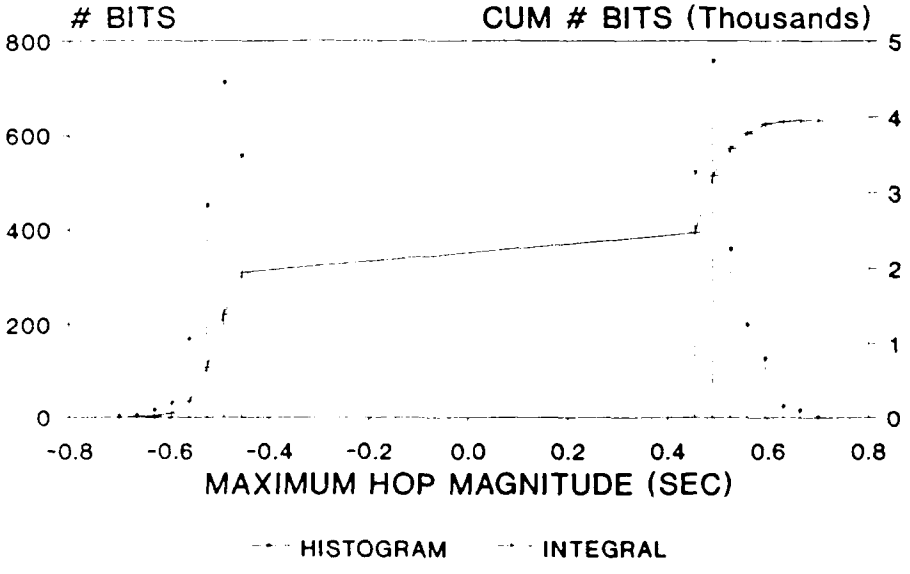
All Bits, All Hops

Figure 3.2-3. TOTAL NUMBER OF HOPS
TEST 90, #127, 80C, Files 2-99



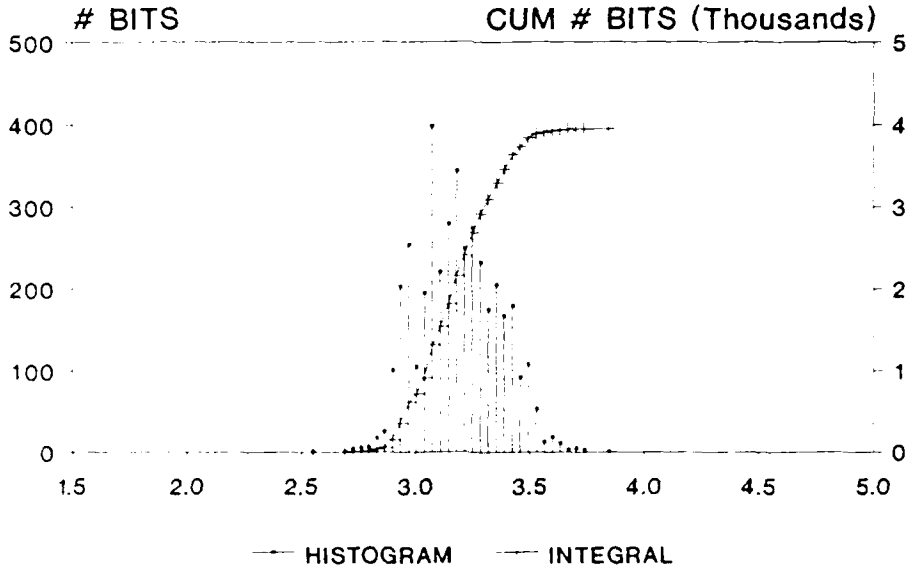
BITS WITH >=2 HOPS

Figure 3.2-4. MAXIMUM HOP MAGNITUDES
TEST 90, #127, 80C, 99 TESTS



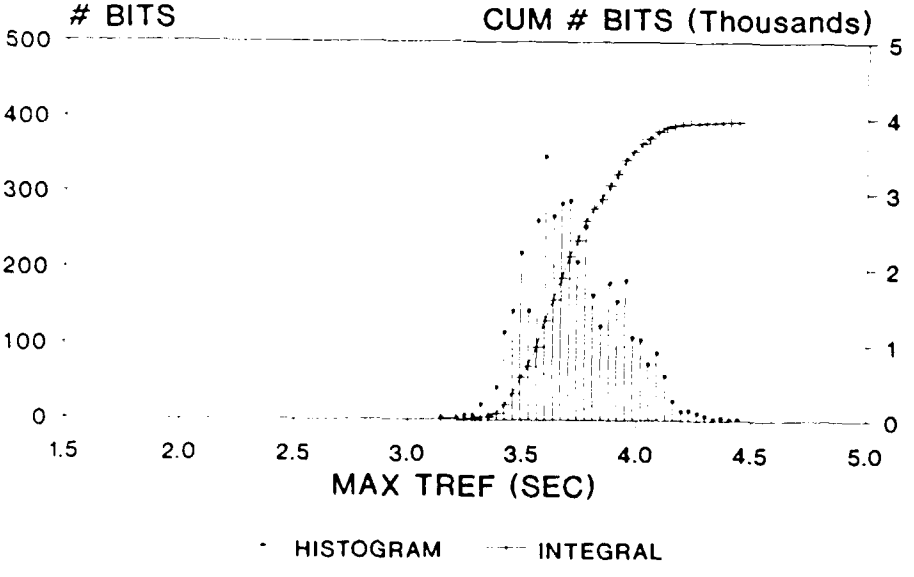
BITS WITH >=2 HOPS

Figure 3.2-5. MINIMUM BIT REFRESH TIMES
TEST 90, #127, 80C, 99 TESTS



BITS WITH >=2 HOPS

Figure 3.2-6. MAXIMUM BIT REFRESH TIMES
TEST 90, #127, 80C, 99 TESTS



BITS WITH >=2 HOPS

Figure 3.2-7. Bit Refresh Times
#127, 80C, TEST 90, 99 FILES

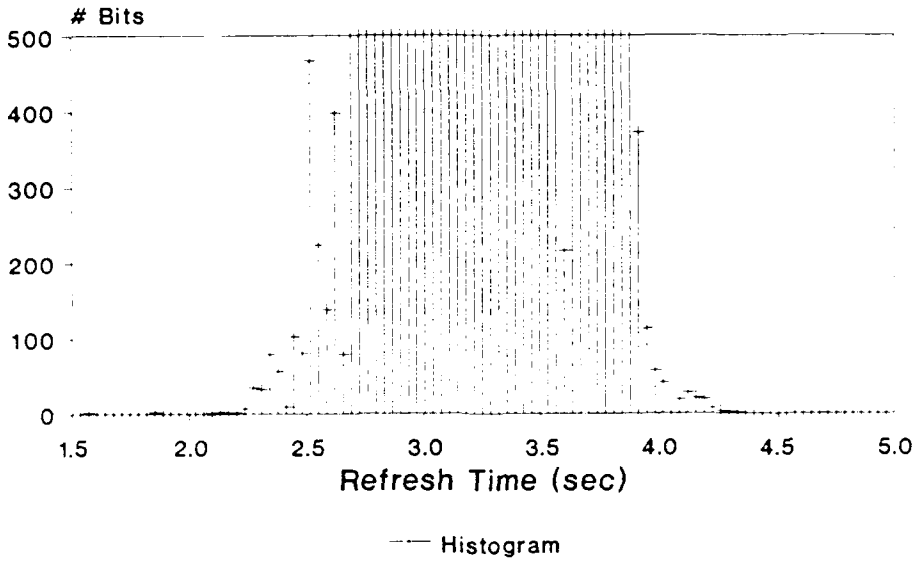
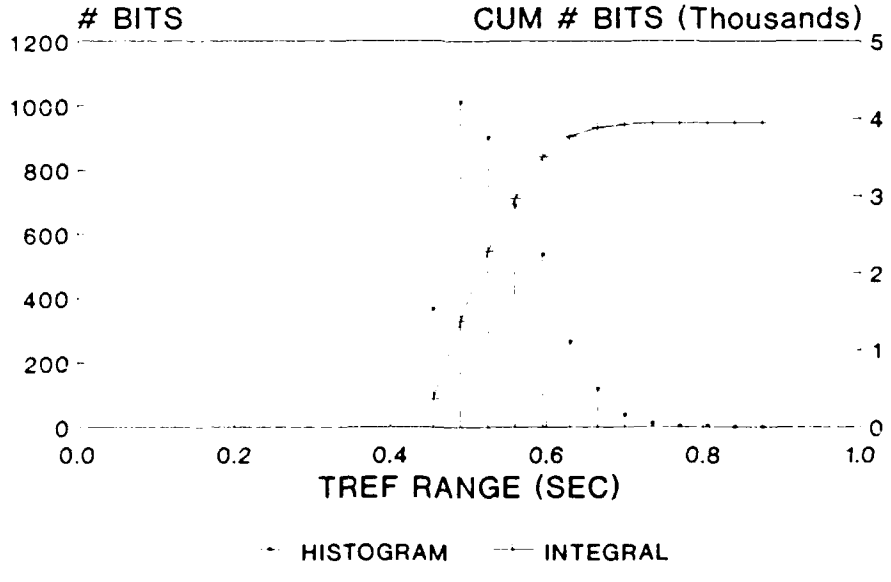
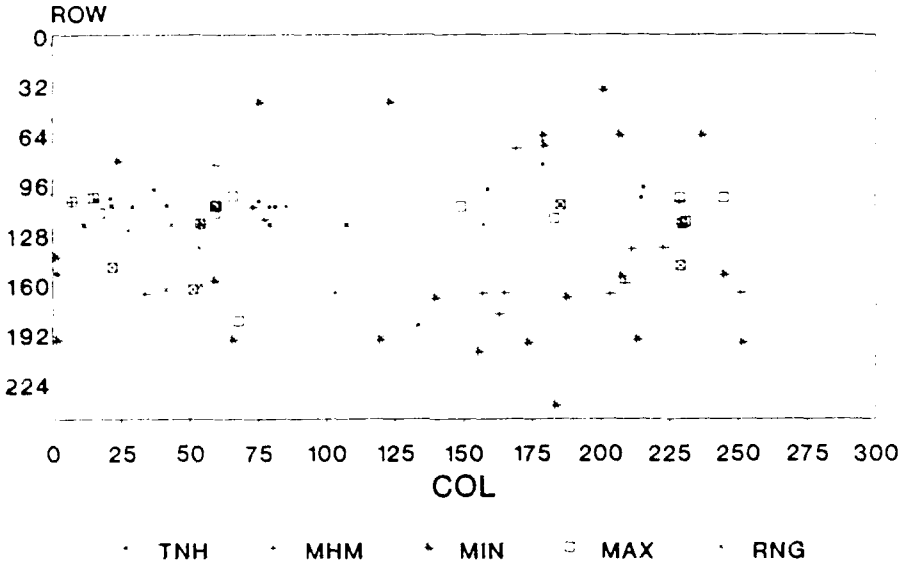


Figure 3.2-8. RANGE OF BIT REFRESH TIMES
TEST 90, #127, 80C, 99 TESTS



BITS WITH >2 HOPS

Figure 3.2-9. LOCATIONS OF OUTLIER BITS
TEST 90, #127, 80C, 99 TESTS



20 EACH CATAGORY

From our raw data. waveforms of Tref can be extracted for a single bit, as shown in Figure 3.2-10a. The diagonal line segments indicate that there were two or more hops below the set threshold which must have occurred to transition between the Tref levels. They were not recorded, so we don't know the Tref values vs time there. If a particular bit was recorded as a hopper at both test temperatures, the activation energy (Ea) of the dominant leakage current component can be determined. Figure 3.2-10b shows such a case. The average value of the waveform was calculated at both temperatures, and fit with Equation 1-1. The Ea was 1.16 electron volts (ev), and the plot is shown in Figure 3.2-10c. It is interesting to note that if an Ea is calculated for this bit using the low level at 80C and the high level at 85C, the result is 0.82 ev. Also, if an Ea is calculated for this bit using the high level at 80C and the low level at 85C, the result is 1.4 ev. Also, if both the high levels, or both the low levels are used, the results are 1.13 and 1.12, respectively. With larger hopping, the error in activation energy is larger, and this effect may account for the discrepant Ea's for hopper bits reported in [1].

Figure 3.2-10a. Bit Trefavg Waveform
Test 90 #127 80C Col 226 Row 136

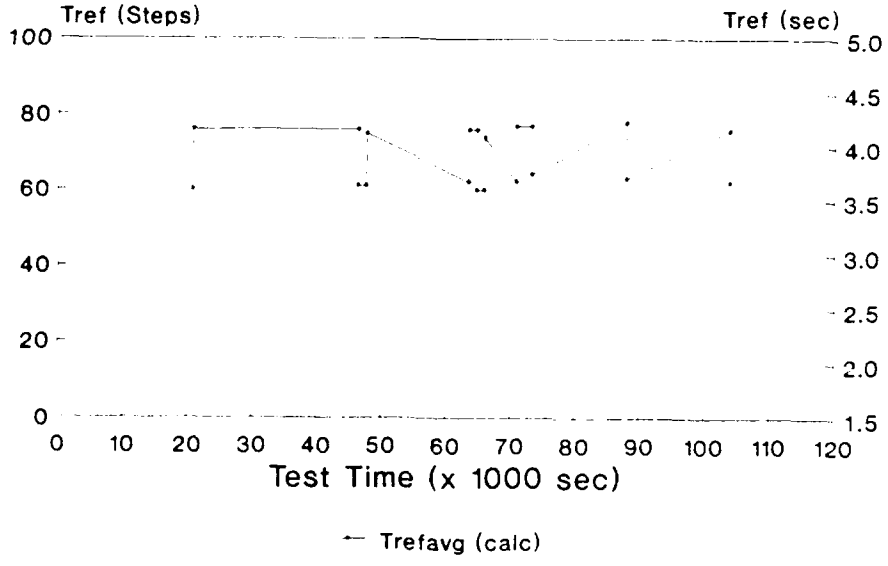


Figure 3.2-10b. Bit Trefavg Waveform
Test 91 #127 85C Col 226 Row 136

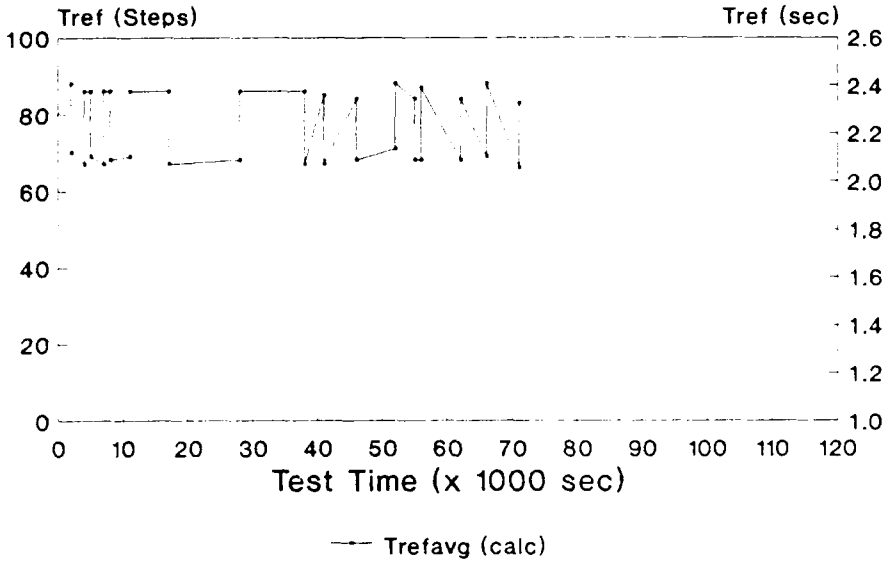
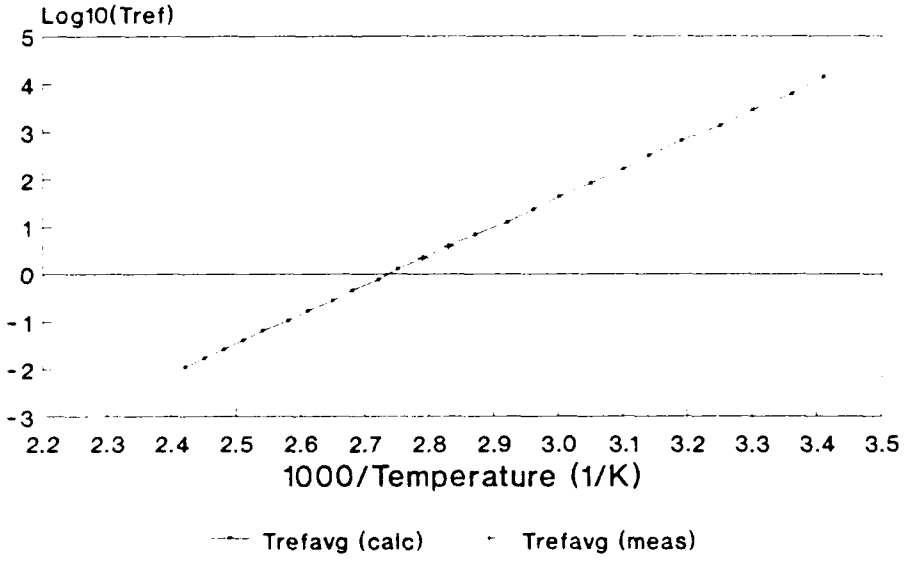


Figure 3.2-10c. Ea of Trefavg
Tests 90&91 #127 80&85C Col 223 Row 136



Ea=1.16 ev

Another observation we can make at this point is that the difference between the high and low levels at 80C is 0.560 sec., and at 85C it is 0.288 sec.

The ratios of these deltas to the Trefavg's are 560/3.901=0.143 and 288/2226=0.129. The simple Ea of these ratios is 0.22ev (the simple Ea is calculated in a manner similar to Equations 1-1, but without the pre-exponential A temperature correction factor).

This means that a Tref Ea screen test based on one Tref measurement at two temperatures would not be effective. A proper screen must identify both hop levels at both temperatures. This would probably require much more test time than a simple one shot Tref test. If this were not done, however, it is quite likely that active and severe hopper bits could be missed entirely because they were measured at their high levels or at their low levels at both temperatures.

We found it quite typical for different hopper bits to have similar Trefavg Ea's, which were in turn very similar to the Ea of the average of all bit Trefs in the device (including hoppers and non-hoppers). Figure 3.2-11a. shows Ea plots of 5 hopper bits and the device average Tref. For this manufacturer's device, they are all about 1.1-1.2 ev, which suggests that the dominant leakage current mechanism is thermal generation in the bulk silicon, which should have an Ea of 1.12 ev.

We could also calculate the average Tref of all hopper bits at both temperatures, as shown in Figures 3.2-11b (80C) and 3.2-11c (85C) and the Ea of all unique bits which occur in each set, as shown in Figure 3.2-11d. This figure shows that the Ea of average Tref for the hopper bits forms a normal distribution peaked right in the neighborhood of 1.12 ev. Previous workers reported that hopper bits exhibited grossly lower Ea [1], and could be screened on that basis, but we do not see that in our data on this manufacturer's device.

Figure 3.2-11a. Trefavg Ea Plots
TESTS 90&91 #127 80C&85C 5 Hopper Bits

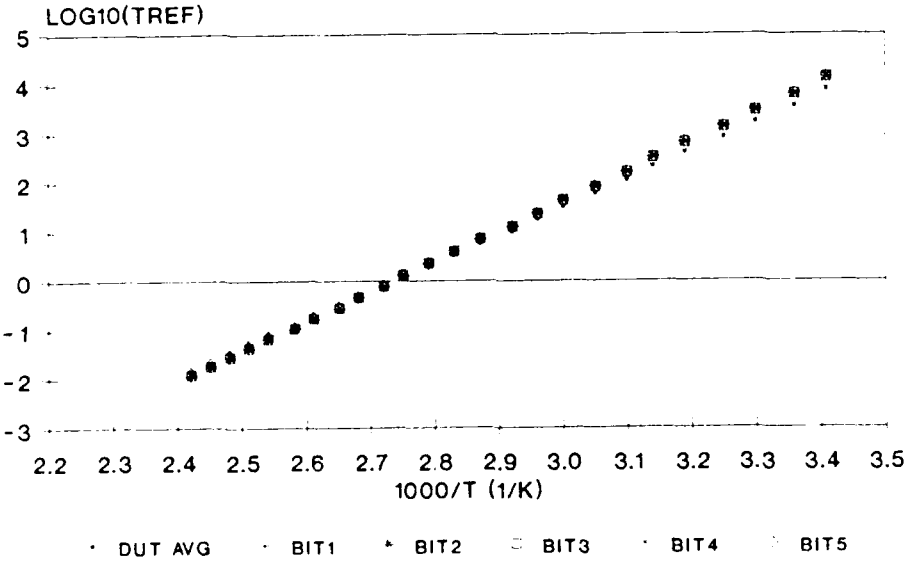


Figure 3.2-11b. Trefavg of Hopper Bits
Test 90 #127 80C

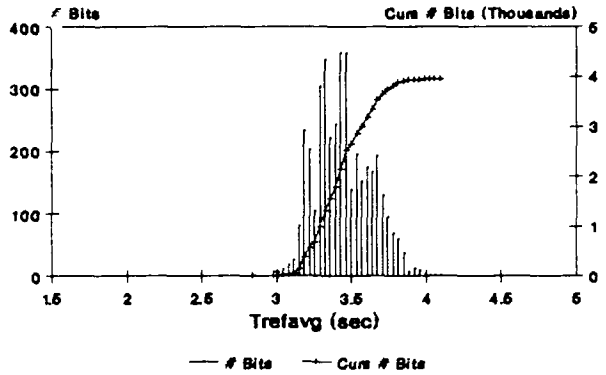


Figure 3.2-11c. Trefavg of Hopper Bits
Test 91 #127 85C File 1

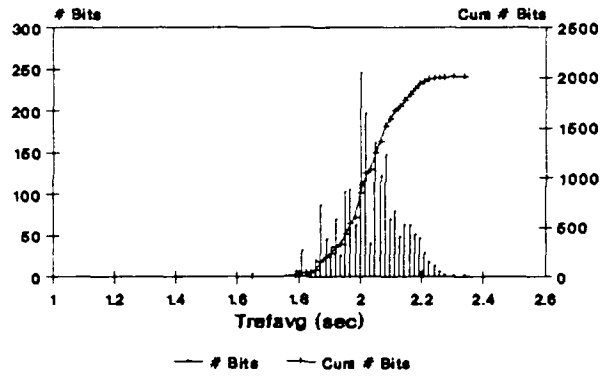
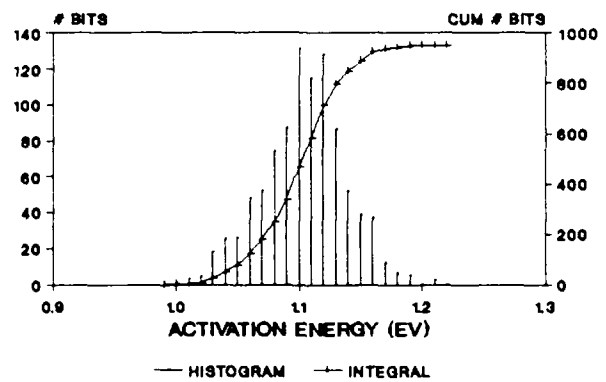
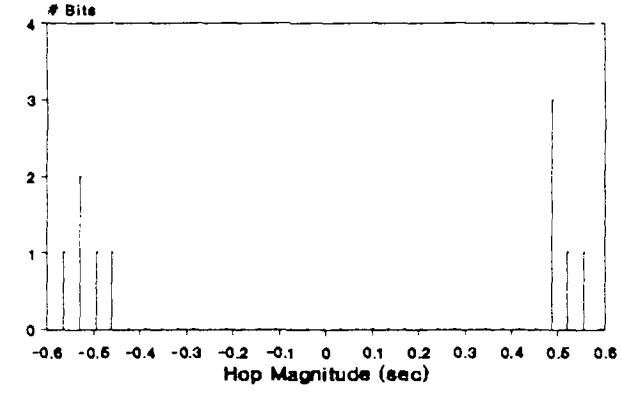


Figure 3.2-11d. Eas of Hopper Bits
Tests 90&91 #127 80C&85C



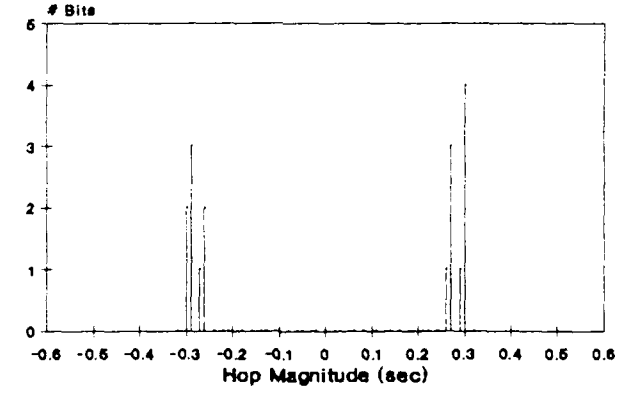
In a manner similar to [6] and others, we produced histogram plots showing the probability of Tref levels occurring (Figures 3.2-12a and 3.2-12b). While these usually contained distributions about one high level and one low level, is was not uncommon to find distributions at two high levels and low levels. That behavior suggests the presence of two trapping sites in a bit. We also saw various cases of Tref waveforms with three distinct levels, which can be explained by trapping at one site modulating trapping activity at second site.

Figure 3.2-12a. Hop Magnitudes
Test 90 #127 80C Col 226 Row 136



(35 ns bin size)

Figure 3.2-12b. Hop Magnitudes
Test 91 #127 85C Col 226 Row 136



(16 ns bin size)

Figure 3.2-13a. Hop Duration Magnitudes
Test 94 #325 80C Col 27 Row 16

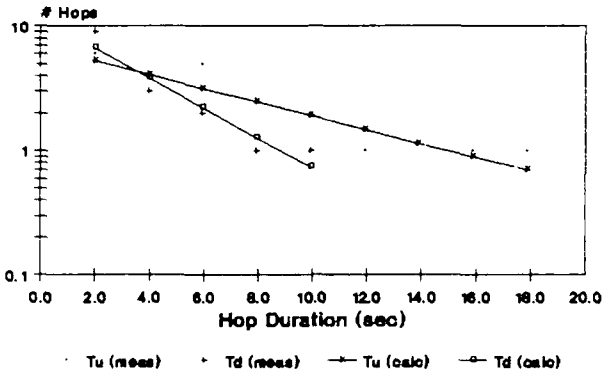


Figure 3.2-13b. Hop Duration Magnitudes
Test 95 #325 85C Col 27 Row 16

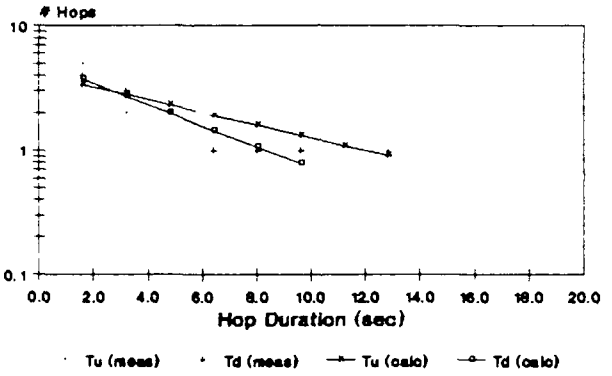
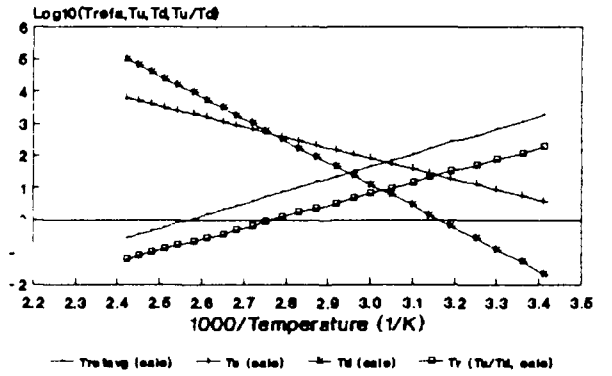


Figure 3.2-13c. Tref, Tu, Td, Tu/Td Ea
Tests 94&95 #325 80C&85C Col 27 Row 16



EaTu=1.08ev EaTd=1.77ev EaTu/Td=0.68ev

Finally, we extracted histograms of high and low Tref level durations, as in [6]. We had some difficulty finding bits with well behaved Tu and Td plots at two temperatures, probably because strong temperature dependence could cause a trap which fluctuates at one temperature to be filled or empty all the time at another temperature. Figure 3.2-13a and 3.2-13b show examples of Tu and Td plots for what we think is the same trap in the same bit at two temperatures. These figures contain measured Tup and Tdown durations, as well as data calculated after fitting with Equation 1-2. Note that these plots are for a bit in device #325, made by a different manufacturer than device #127, the source of data for the previous figures in this section. In both of these cases the high Tref durations are longer than the low Tref durations, indicating that the low leakage current level predominates over the high leakage current level.

From the Tu and Td parameters derived from the curve fitting at two temperatures, the Ea of Tu, Td, and the ratio Tu/Td can be calculated, as shown in Figure 3.2-13c. For this particular bit, the Tu and Td distributions are fairly believable, that is, there are several points for each. The Ea of the ratio of Tu/Td is 1.9 ev, which happens to be about the same as the Ea of Trefavg for this bit, which is also shown in this figure. This was not always the case, however. It was more often the case that the Ea's of Tu/Td were not similar to the Ea of Trefavg, as shown for the 10 bits in Table 3.2-2. However, inspection of the data showed that several of these bits had few hops, or many at the shorter durations, which indicates that the Tu and Td parameter fitting was questionable. This point should be studied further, with longer tests which would accumulate more hops and support more accurate parameter extractions.

Table 3.2-2. Tu, Td, Tu/Td and Tref avg Ea's (in ev) for 10 bits. (tests 94&95)

col	row	#hc	#hh	EaTu	EaTd	EaTu/Td	EaTrefavg
5	103	11	18	5.4	3.1	2.2	0.72
6	248	26	25	-3.5	1.6	-5.1	0.72
27	16	36	21	0.2	-0.7	0.9	0.71
62	30	45	27	-1.1	-2.6	1.5	0.71
80	246	24	17	-3.2	-0.3	-2.9	0.79
128	201	48	28	-1.0	-1.0	0.0	0.75
142	132	27	19	0.4	-0.9	1.3	0.72
149	255	40	19	-0.6	-4.4	3.8	0.67
195	107	38	19	-2.6	-2.2	-0.4	0.68
197	212	26	21	0.1	2.0	-1.9	0.71

Finally, Figures 3.2-14a through c show photographs of Tref images produced on a PC for devices # 127, 325, and 7. Each pixel represents the initial measured Tref, with values of 0-100 mapped onto an 8 level intensity grey scale. The images are corrected for true physical layout, with columns running horizontally and rows vertically, oriented with pin 1 in the upper right hand corner. For Figure 3.2-14a (DUT #127, Test 90) and Figure 3.2-14b (DUT #325, Test 94) the Tref distribution was centered in the range tested, but the parts are manufactured by different companies. For Figure 3.2-14c (DUT #7, Test 40), the range was intentionally adjusted so that only the highest Tref bits were measured. The manufacturer is the same as for Figure 3.2-14a, but effectively, the 8 level greyscale is spread across the very highest Tref bits, and all others appear as dark. This Figure was included to illustrate that using this software display tool, it was quite easy to locate the physical locations of bits which had high or low Trefs by modifying the Tref value to grey scale mapping. We could also produce images directly from hopper data files, and plot these to locate hopper bits.

Figure 3.2-14a. Tref Image of DUT #127, Test 90

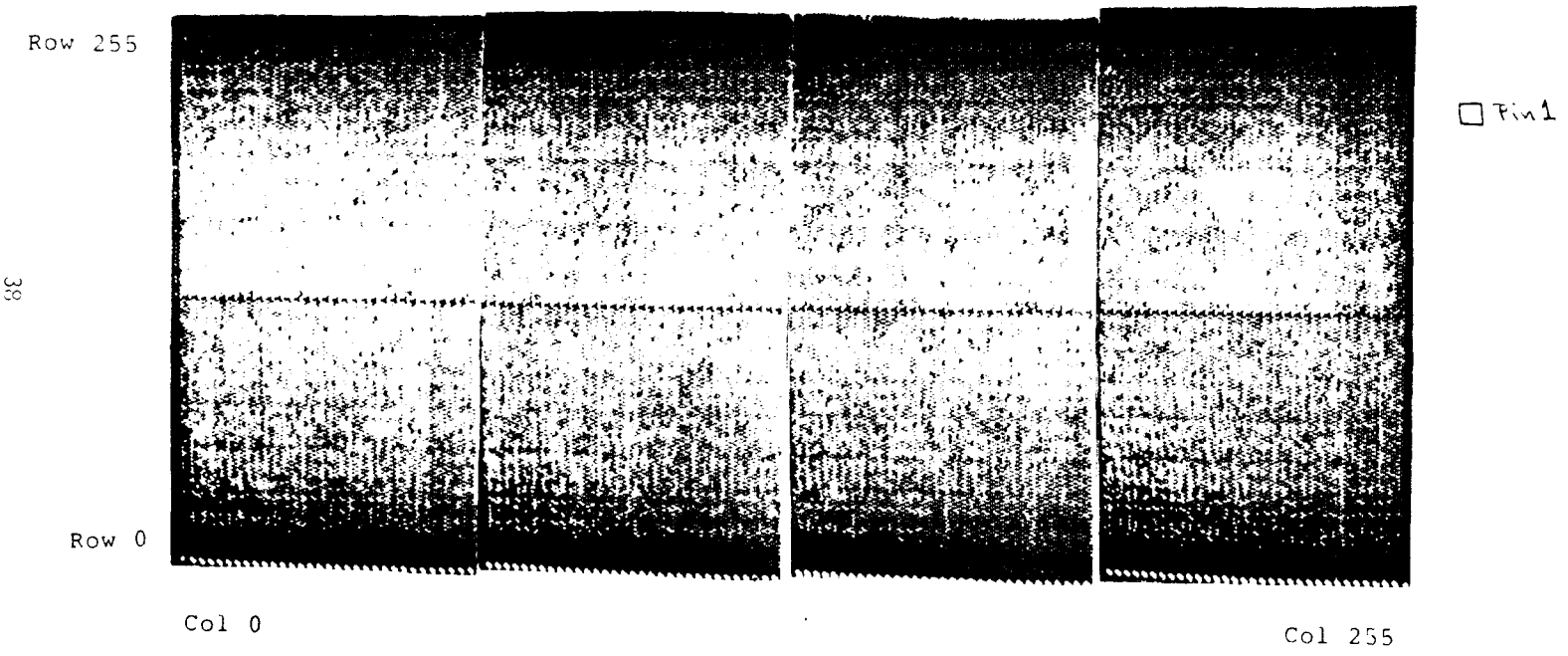


Figure 3.2-14b. Tref Image of DUT #325, Test 94

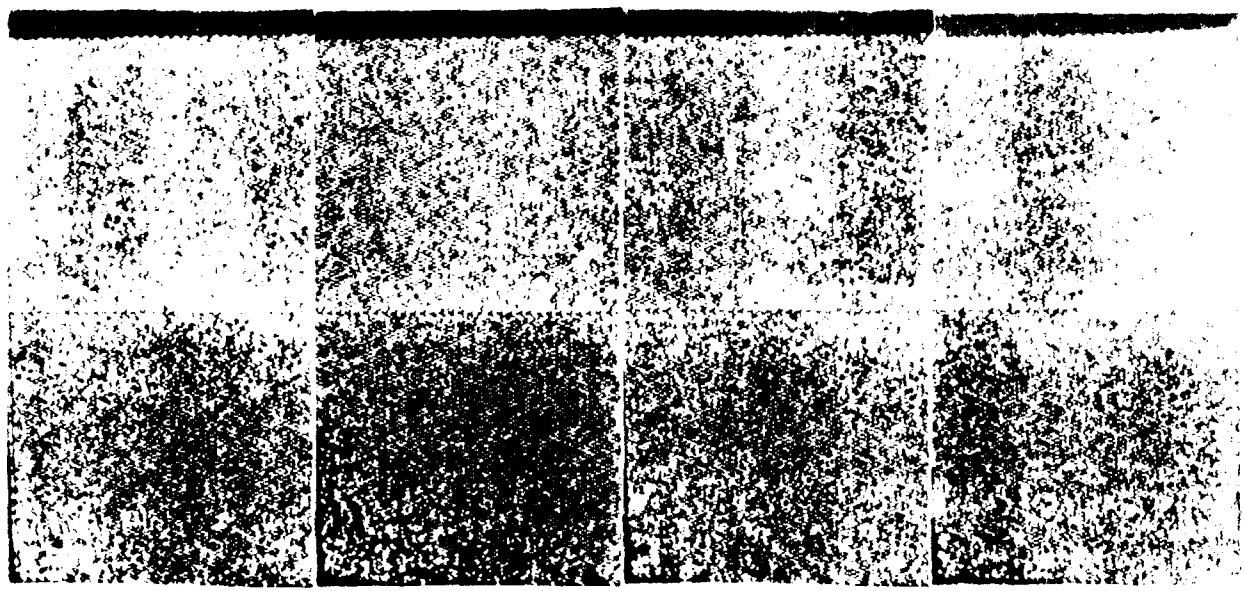
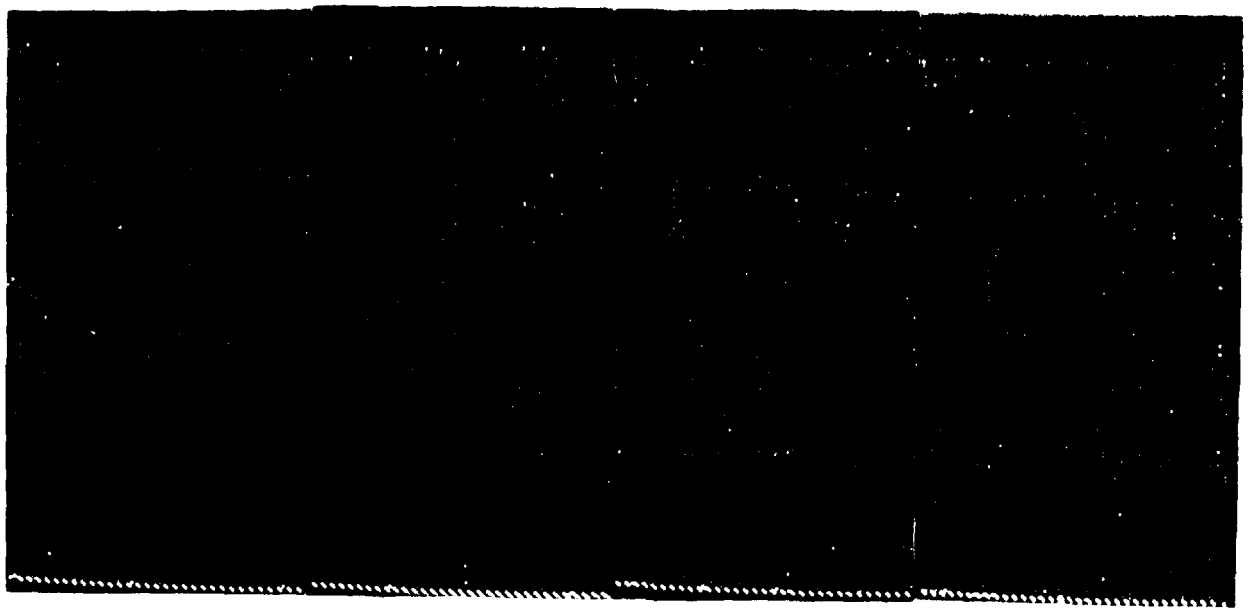


Figure 3.2-14c. Tref Image of DUT #7, Test 40
(Only highest Trefs)



4.0 Test Results and Discussion

This section will show and discuss test results. Table 4.0-1 shows test conditions used to study five 64K DRAM devices. Devices #7, #325 and #457 were from one vendor, and devices #127 and #129 were from another vendor. Device #7 was from a different lot than #325 and #457. Each device was tested at two temperatures, and each series of tests was assigned a test number for reference. For all tests except 40 and 41 the Tref trails were chosen to span the Tref range indicated in the table by the TMIN and TMAX columns, in the number of evenly spaced intervals shown in the STEPS column. In tests 40 and 41 the Tref trials spanned just the top tail of the Tref distribution in just 8 steps, in an attempt to minimize test time and resolve faster hopping bits. A smaller difference in test temperature was also used to try to insure measuring the same trapping centers.

Table 4.0-1 Test conditions used for several tests.

Test	Part	TEMP	TMIN	TMAX	# STEPS	Tref Avg	Hop Thr	# TESTS	BFA VTH,#	VAX FILE	TEST DATE ('90)
40	Device #7	80C	7950	9600	8	1.0	1	1-350	1,2	BFA40	DONTKNOW
41	"	82C	6700	7800	8	1.0	1	1-350	1,2	BFA41	DONTKNOW
90	Device #127	80C	1500	5000	100	49.7	13	2-99	13,1	BFA90	Sept 26
91	"	85C	1000	2600	100	57.0	16	1-74	16,1	BFA91	Sept 27
92	Device #129	80C	1700	4600	100	53.4	14	1-109	14,1	BFA92	Nov 09
93	"	85C	1000	2800	100	57.3	14	1-70	14,2	BFA93	Nov 13
94	Device #325	80C	4000	15000	100	46.4	13	2-92	13,1	BFA94	Nov 14-20
95	"	85C	2800	10500	100	46.2	12	1-52	12,1	BFA95	Nov 20-21
96	Device #457	80C	4000	15000	100	47.9	12	1-107	13,1	BFA96	Nov 23-26
97	"	85C	2800	10500	100	53.1	12	1-59	12,1	BFA97	Nov 21-23

	HOP THR/ TREF AVG RATIO(%)	# HOP BITS	TREF AVG CN,7	TREF AVG Ea	MTEST TIME S	HOP THR (MS)	STEP SIZE (MS)	LARGEST HOP VAL (MS)	LARGEST HOP RNG (MS)	MIN HOP TREF (MS)
40	-	57	n/a	n/a	180	206	206	-825	1031	8156
41	-	953	n/a	0.86	180	137	137	687	962	6837
90	14.1	3948	3229	n/a	1221	455	35	700	875	2550
91	13.3	2010	1912	1.09	1000	256	16	-400	416	1512
92	12.5	4758	3248	n/a	1199	406	29	-638	754	2483
93	12.4	8688	2031	0.96	(1000)	252	18	-450	468	1234
94	15.7	460	9099	n/a	1981	1430	110	-3630	3630	5430
95	14.8	314	6356	0.73	1601	924	77	-2156	2310	3801
96	14.2	390	9269	n/a	1979	1320	110	3080	3300	6200
97	13.7	675	6889	0.59	1585	924	77	2310	2695	4802

The Tref Avg column in Table 4.0-1 lists the bin number of the average of all bit Tref bins, measured at time zero. Bin 1 corresponds to TMIN and bin 100 corresponds to TMAX. The VTH column shows the number of bins chosen as the threshold amount a bit would have to hop by in sequential tests to be recorded. This threshold was chosen to result in a managable number of hops per test. The next column shows the number of tests done in the sequence, that is the number of times all bits were measured. The column labeled BFA THR MIN# has two numbers. The first is the threshold number of bins to define a hopper which was re-applied in post-test data analysis (this could be bigger than the treshold used during testing), and the second is the minimum number of hops required to cause a bit to be included in the files used for data analysis. This allowed disregarding bits which hopped infrequently in parameter extractions.

The lower portion of Table 4.0-1 shows various numbers extracted from the results, including; the number of bits which hopped, the value of the Tref distribution avg in millisconds, the Tref Ea, measured test time for one set of Tref measurements (based on data file time stamp), the magnitude of the minimum Tref change called a hop and recorded, the magnitude of Tref corresponding to one bin of Tref (Tref measurement precision), the largest hop observed, largest hop range observed, and minimum Tref value assumed by a hopper bit during testing. By dividing Trefavg by the HOP THR , we see that the percentage change which defined a hopper varied between about 12 and 15 percent. This tends to explain why many more hops were recorded in tests 92&93 than in tests 90&91 (same manufacturer), but does not explain why there were so many more hops recorded in tests 90-93 than in 94-97 (different manufacturers).

Sections 4.1 through 4.10 discuss characteristics of overall hopper bit populations for the ten tests. Nine figures are shown to characterize the hopping behavior of the overall bit population for the COLD or lower temperature tests. These same nine, as well as two additional figures are shown for the HOT or higher temperature tests. These plots will be explained here, and highlights for each device and bit will be pointed out in the following sections.

The nine plots shown for both the COLD and HOT tests including histograms of

1. all Trefs taken at time zero
2. all hop durations recorded during the test
3. # bits vs total # of hops
4. # bits vs maximum hop magnitude which occurred during testing
5. # bits vs minimum Tref which occurred during testing
6. # bits vs maximum Tref which occurred during testing
7. # bits vs range of Tref which occurred during testing
8. # bits vs average Tref value only for hopper bits, and
9. a physical location plot of the 20 furthest outliers of histograms 3-7.

The additional two figures shown for the HOT tests are

10. a histogram of the activation energies of those bits which hopped by at least the threshold amount at least five times during testing
11. a plot of log10(Tref) vs inverse test temperature of the mean of the initial Tref distribution (plot 1. above) and five typical hopper bits.

Sections 4.11 through 4.13 discuss characteristics of individual hopper bits selected from tests 40&41, 90&91, and 96&97. The information includes a table showing all bits which hopped more than 5 times at both temperatures, their Tref, Tu and Td

parameters and their activation energies. Also, this data is shown in the following histograms,

1. Tref avg activation energies (Ea's)
2. Tu " "
3. Td " "
4. Tu/Td " "
5. Tu*Td " "

and the following scatter plots,

6. Tu Ea's vs Tref Ea's
7. Td Ea's vs Tref Ea's
8. Tu/Td Ea's vs Tref Ea's
9. Tu*Td Ea's vs Tref Ea's.

Finally, six individual bits were picked from each DUT which had high numbers of hops at each temperature (to support parameter extraction), and plots were produced of

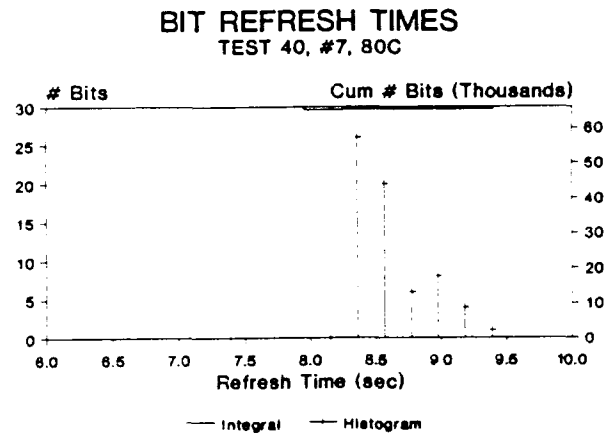
10. Tref vs test time (COLD)
11. Tref vs test time (HOT)
12. a histogram of hop values (COLD)
13. a histogram of hop values (HOT)
14. probability plot of Up and Down hop level durations (COLD)
15. probability plot of Up and Down hop level durations (HOT).

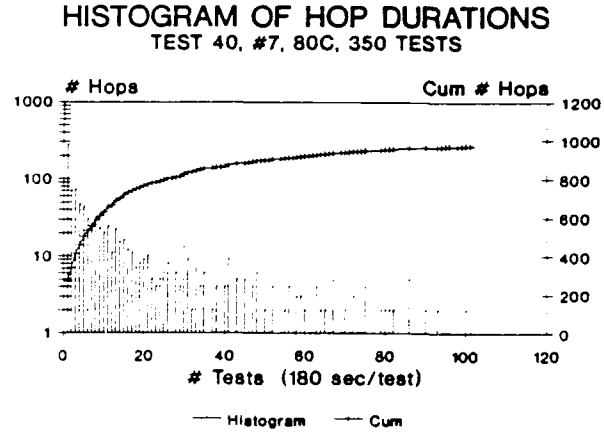
The following sections include comments about the test results for each DUT. It might be useful for the reader to review the results of one of the DUTs other than #7 first, to get a better idea of what typical results looked like, since special test conditions were used for #7.

4.1 Test 40: Device #7, 80C

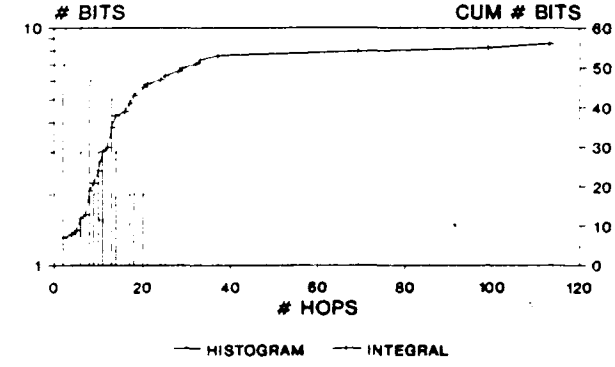
This DUT was tested with a restricted Tref range, with few steps, in order to reduce test time and measure hopping behavior with better time resolution. Note in Figure 4.1-2 (top right) that several hops occurred after very long stable periods, for instance five hours. Note in Figure 4.1-3 (middle left) that there were bits which hopped about 70 and about 110 times during the 350 tests, but most of the bits hopped less than about 20 times. This suggests that the Tref waveforms measured are real. By comparing Figures 4.1-1 and 4.1-6 (lower right), it can be seen that bits hop up after time zero testing to become the highest outliers. The worst hoppers covered a Tref range of just over one second. The minimum Tref of all hopper bit measurements was about 8.1 seconds. Many of the outlier bits were on the perimeter of the chip.

Figures 4.1-1 to 4.1-6 Test 40 #7 80C

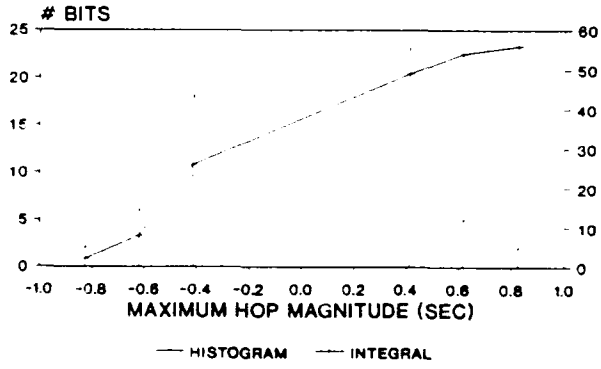




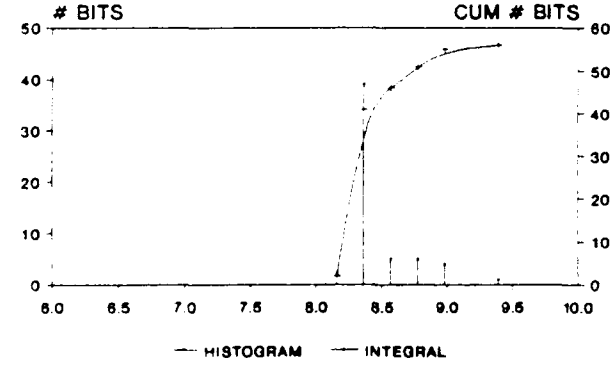
Bits with >= 2 hops



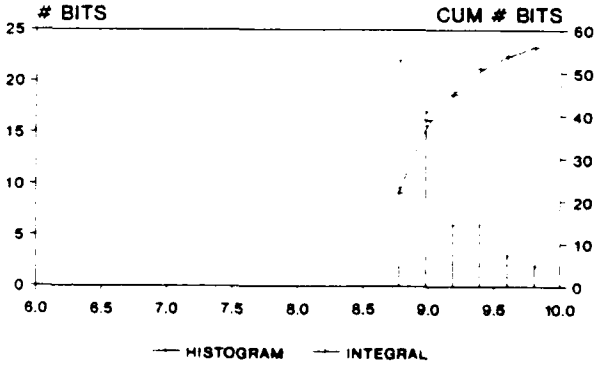
BITS WITH >=2 HOPS



BITS WITH >=2 HOPS

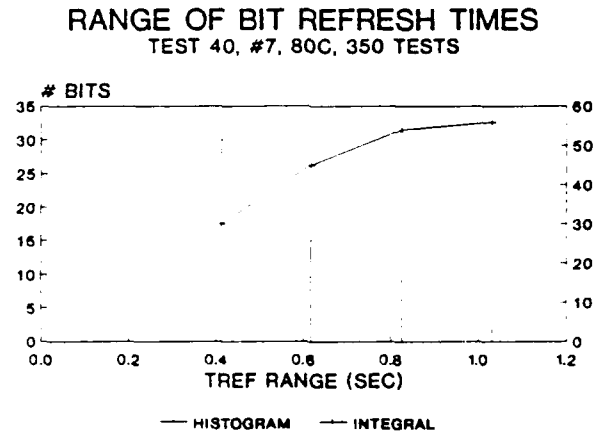


BITS WITH >=2 HOPS

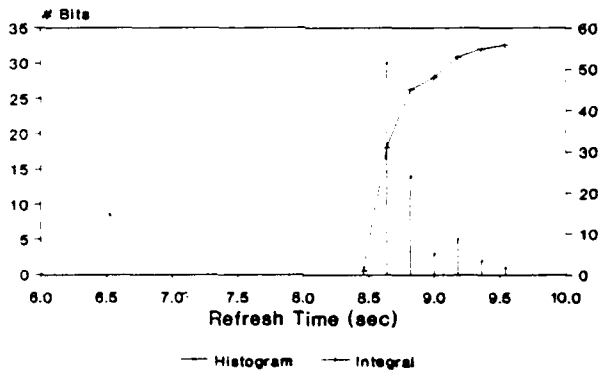


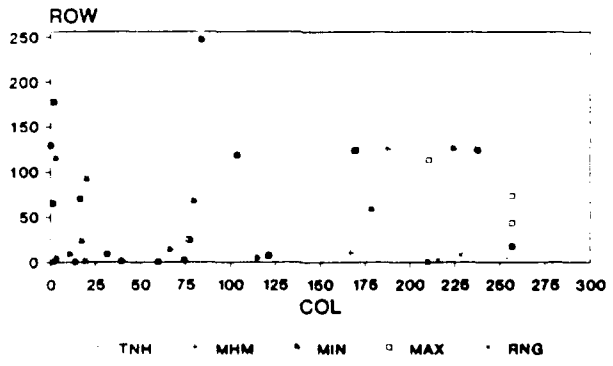
BITS WITH >=2 HOPS

Figures 4.1-7 to 4.1-9 Test 40 #7 80C



BITS WITH >=2 HOPS



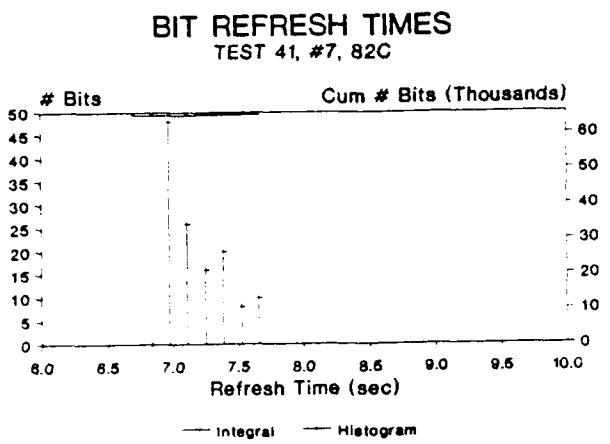


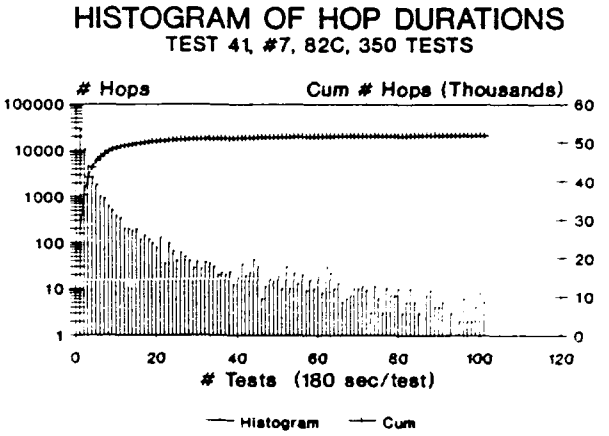
20 EACH

4.2 Test 41: Device #7, 82C

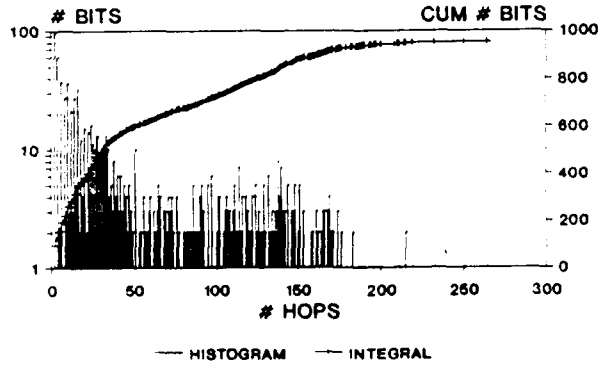
The largest range of Tref hopping was about 0.96 seconds. The minimum Tref for a hopper bit was about 6.8 seconds. Figure 4.2-11 shows that the activation energy (Ea) of the mean of the Tref distribution measured at the beginning of the test was 0.89ev. The distribution of hopper bit avearge Tref Ea's is shown in Figure 4.2-10, and was spread between 0.76ev and about 1.05ev. It is interesting to note that in the distribution of total number of hops, the cumulative line shows three areas with different slopes. This was much more apparent in this test, possibly because the number of tests is higher.

Figures 4.2-1 to 4.2-6 Test 41 #7 82C

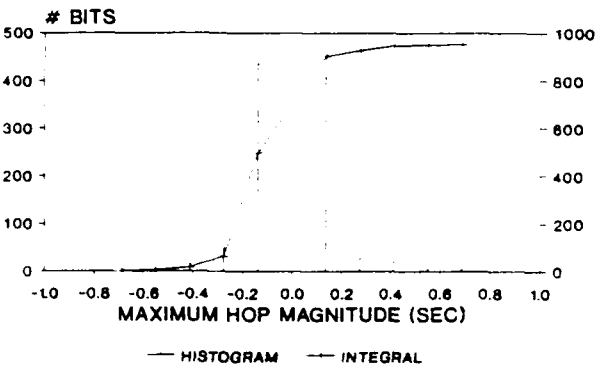




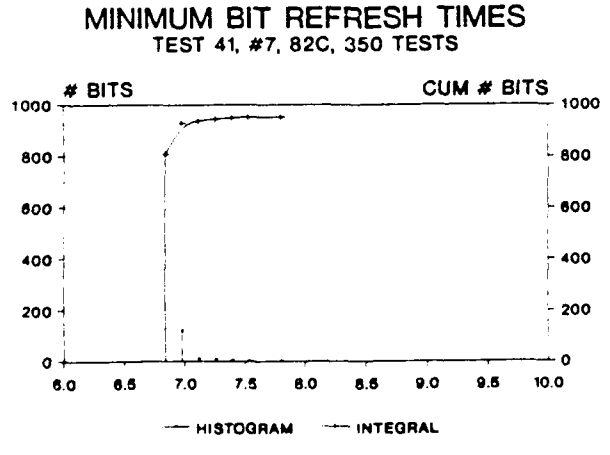
Bits with ≥ 2 hops



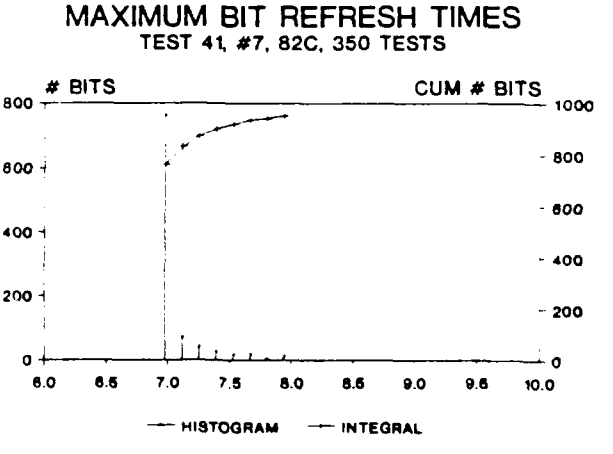
BITS WITH ≥2 HOPS



BITS WITH ≥2 HOPS

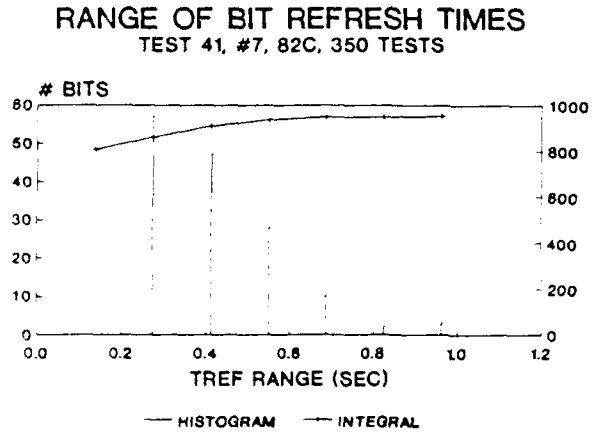


BITS WITH ≥2 HOPS

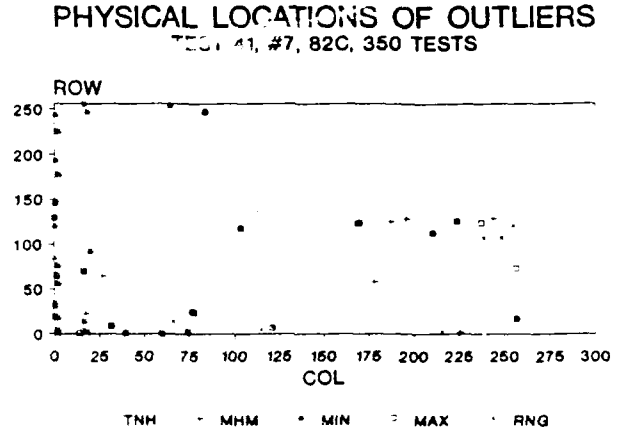


BITS WITH ≥2 HOPS

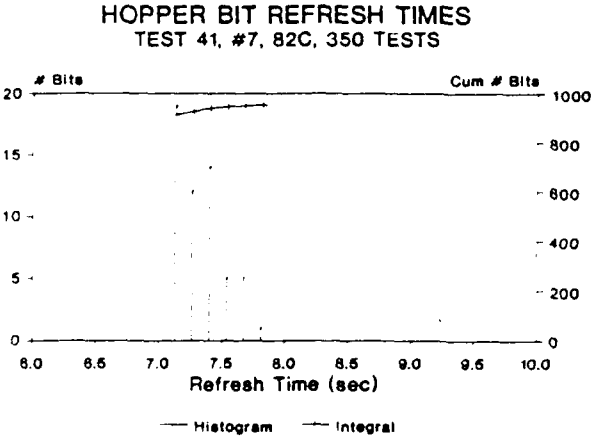
Figures 4.2-7 to 4.2-11 Test 41 #7 82C

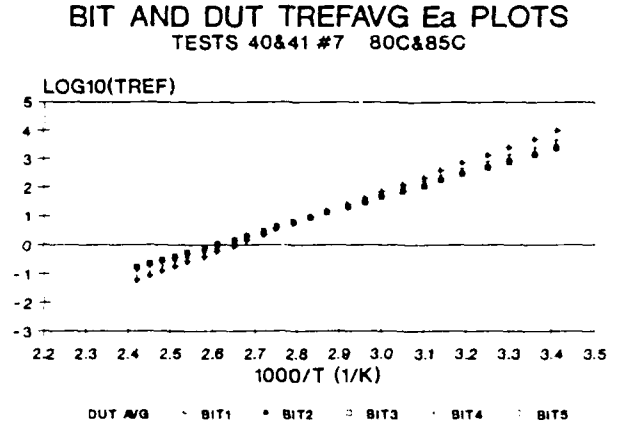


BITS WITH >=2 HOPS

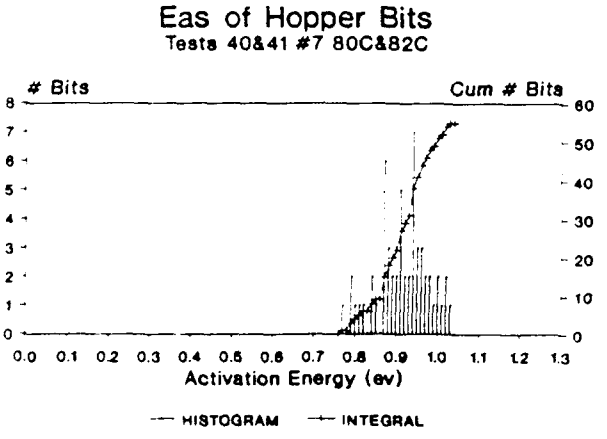


20 EACH





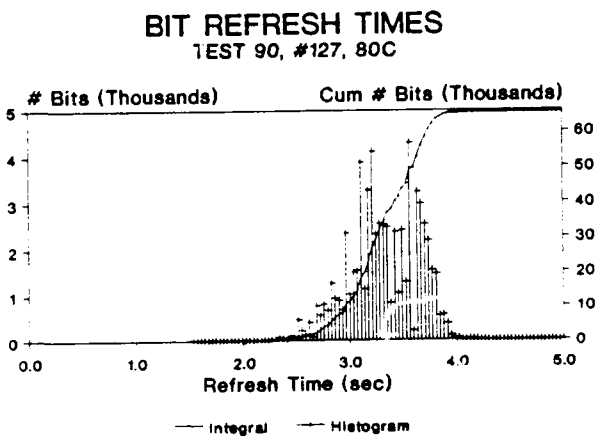
Ea's: .89 .98 .79 .77 .84 .99 (ev)

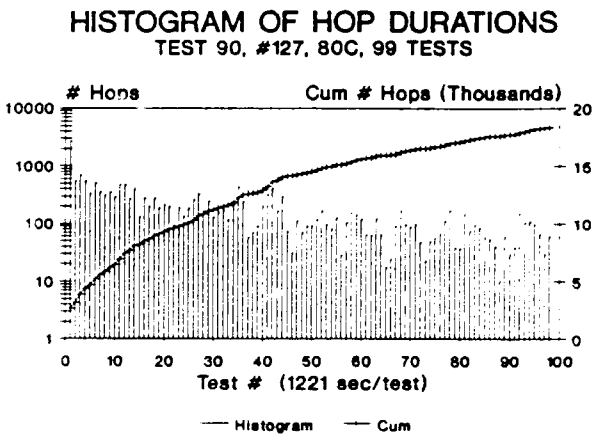


4.3 Test 90: Device #127, 80C

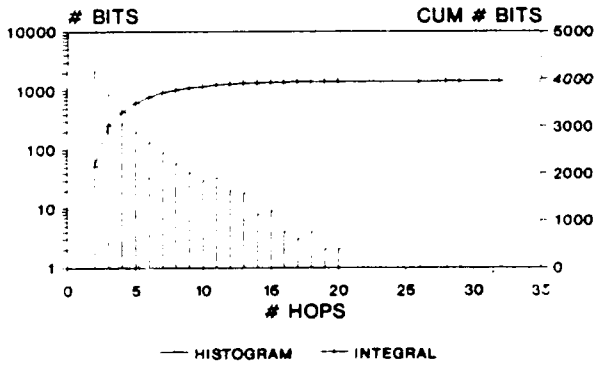
This test covered about 34 hours, during which 99 sets of tests were done. The initial Tref distribution was multi-modal, and the distribution of hop durations is fairly flat out to long times. Again by comparing the bit refresh time distribution (Figure 4.3-1) and the minimum and maximum Tref distributions (Figures 4.3-5 and -6), it can be seen that the highest outliers are hoppers, whereas the lowest outliers are apparently relatively stable. Figure 4.3-8 shows that the hopper bits are restricted to the upper part of the Tref distribution. The largest Tref hopping range was about 0.875 ms. The minimum Tref for a hopper bit was about 2.5 seconds. Outliers of the distributions were scattered rather than confined to the chip edges.

Figures 4.3-1 to 4.3-6 Test 90 #127 80C

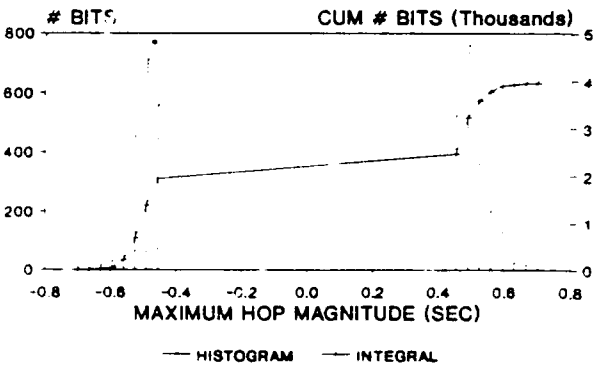




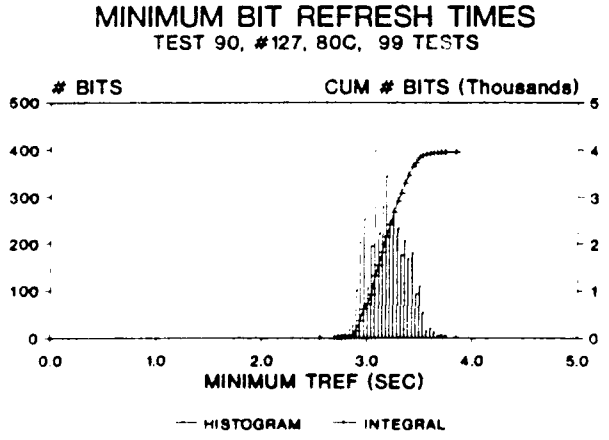
Bits with >= 2 hops



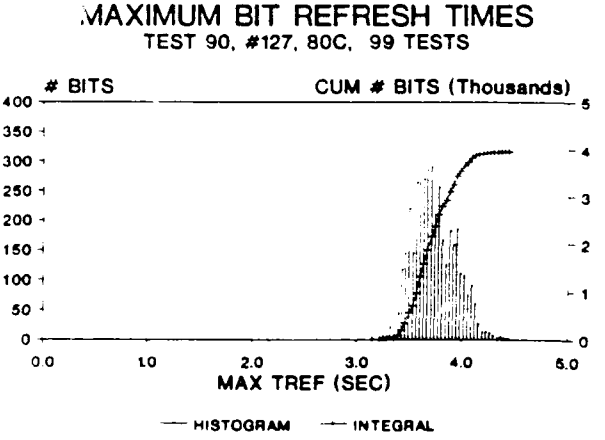
BITS WITH >=2 HOPS



BITS WITH >=2 HOPS

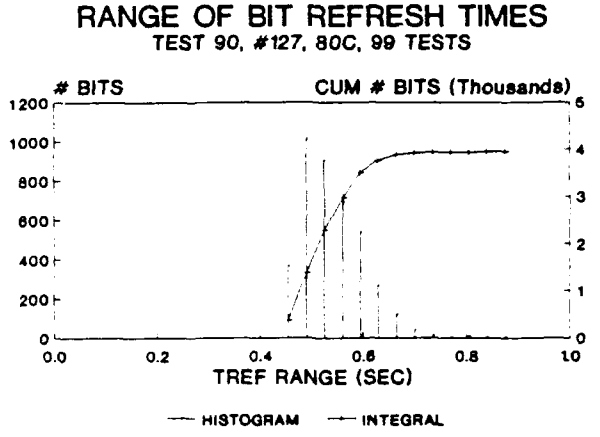


BITS WITH >=2 HOPS

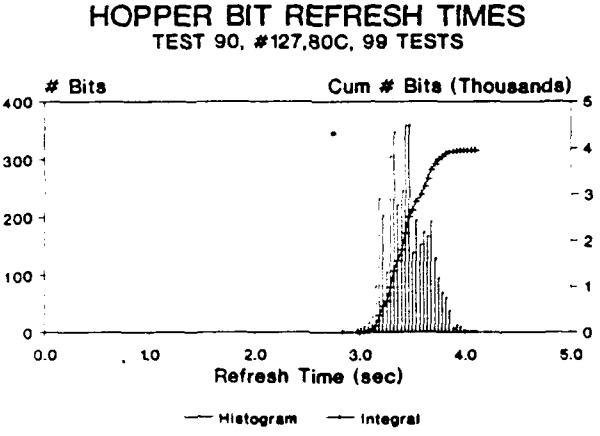


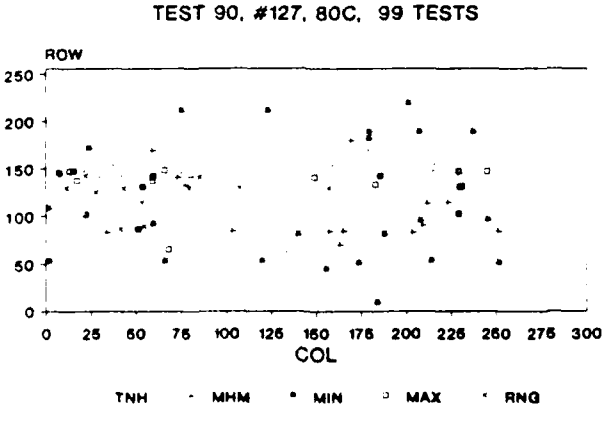
BITS WITH >=2 HOPS

Figures 4.3-7 to 4.3-9 Test 90 #127 80C



BITS WITH >=2 HOPS





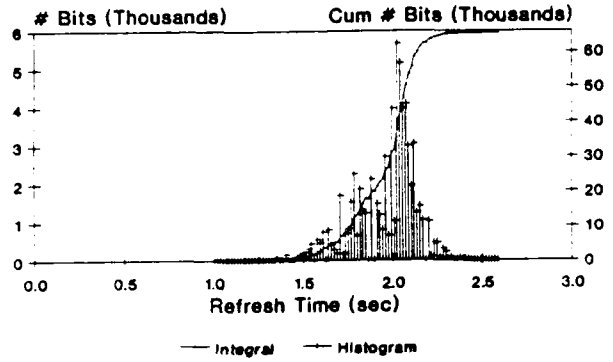
20 EACH

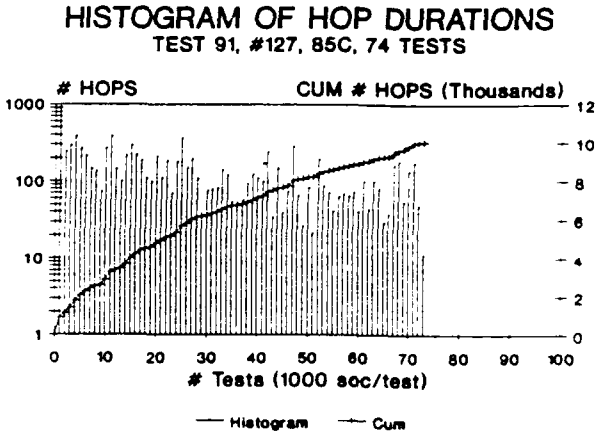
4.4 Test 91: Device #127, 85C

The results were similar to the colder temperature, with low Tref bits not due to hopping. The largest range of Tref hopping was about 0.41 seconds. It is interesting to note in the range plot that the number of hopper bits exhibiting smaller and smaller ranges does not increase. Even though no ranges would have been recorded which were less than 256ms (the HOP THR for this test), it is apparent that the distribution peaks at about 300ms and decreases. This value represents about .3s/2.0s*100% or 15% of the average Tref value. This was also observed for other tests.

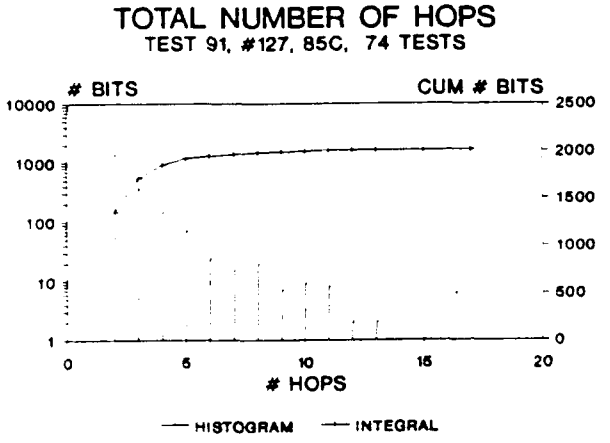
The minimum Tref for a hopper bit was about 1.5 seconds. Hopper bit average Tref Ea's ranged between about 1.0ev and 1.2ev, and the Ea of the mean of the initial Tref distribution was about 1.09ev.

Figures 4.4-1 to 4.4-6 Test 91 #127 85C

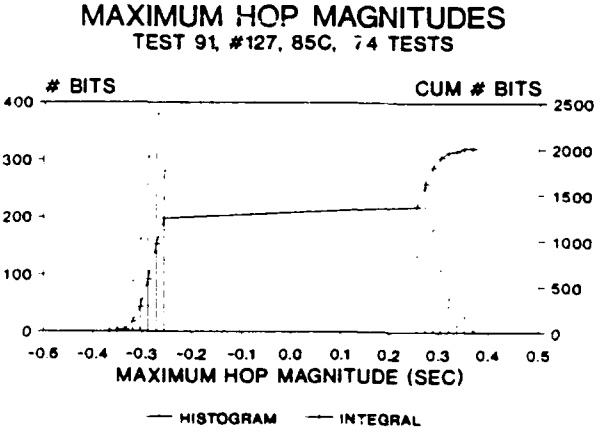




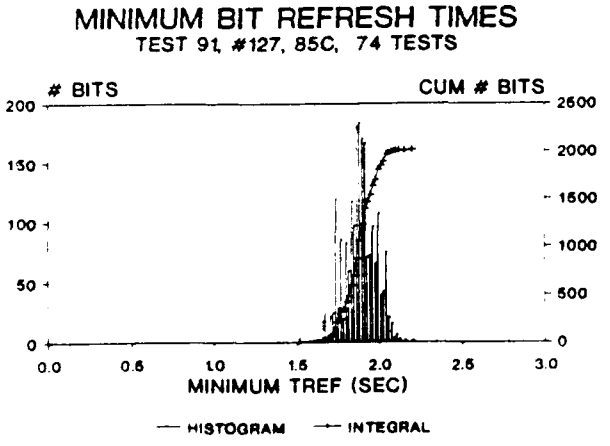
Bits with >= 2 hops



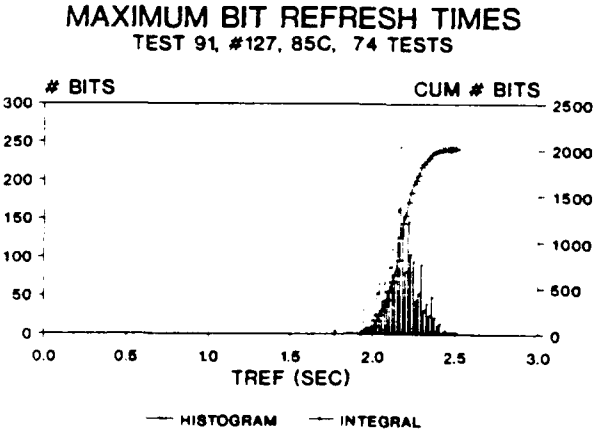
BITS WITH >=2 HOPS



BITS WITH >=2 HOPS

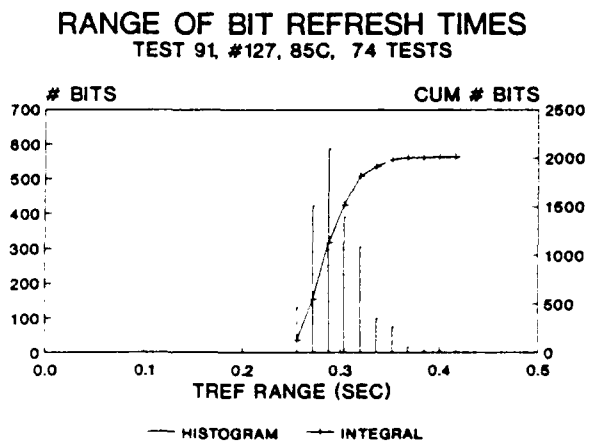


BITS WITH >=2 HOPS

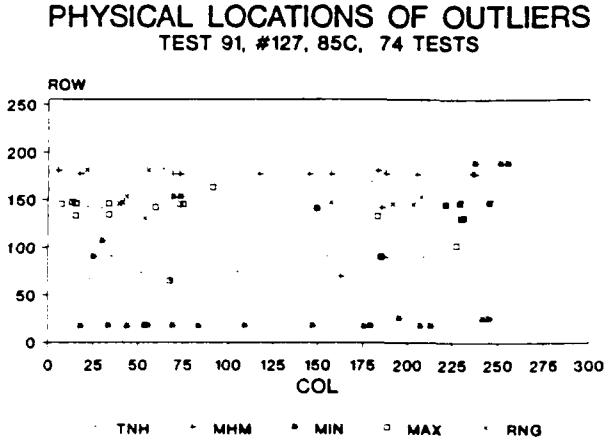


BITS WITH >=2 HOPS

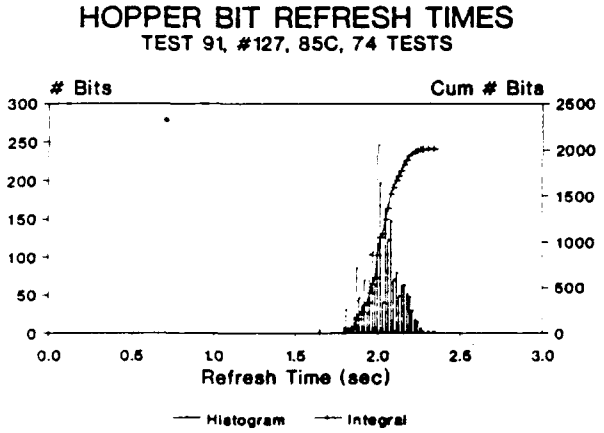
Figures 4.4-7 to 4.4-11 Test 91 #127 85C

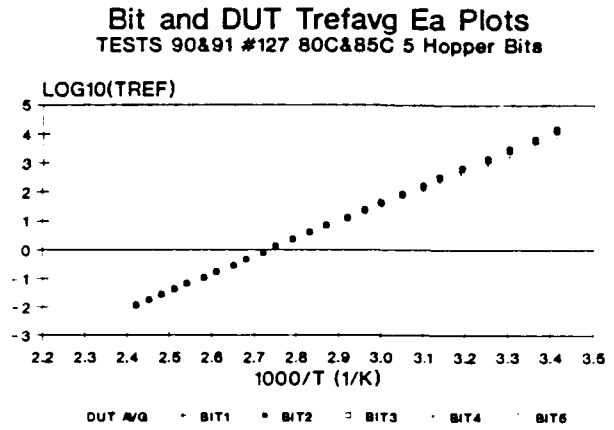


BITS WITH >2 HOPS

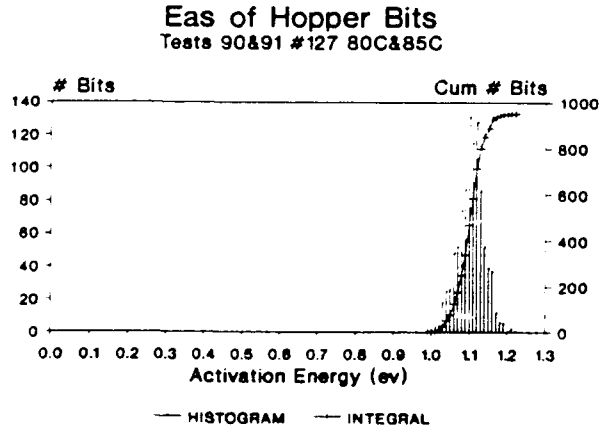


20 EACH





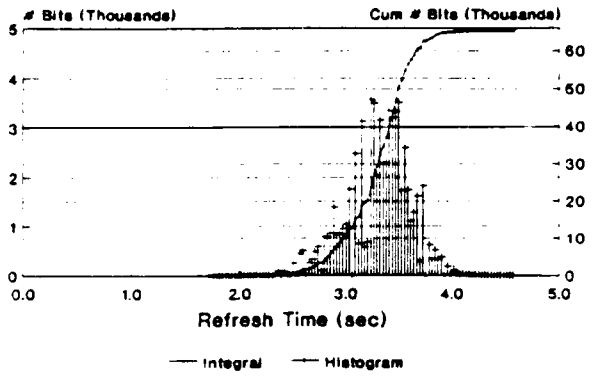
Ea's: 1.09 1.17 1.13 1.16 1.15 1.15 (ev

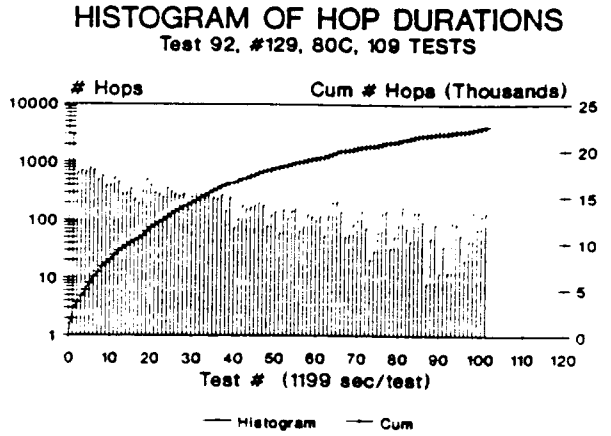


4.5 Test 92: Device #129, 80C

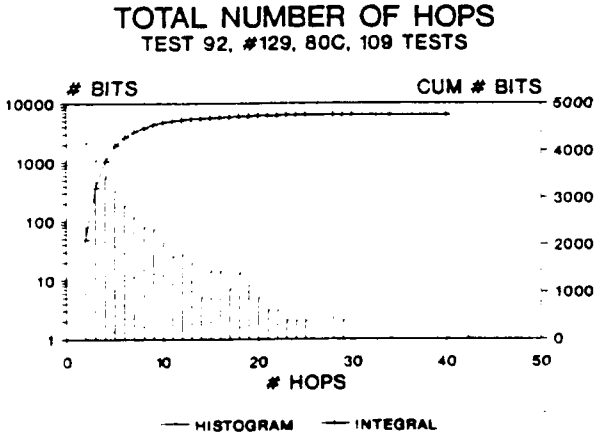
Again the Tref distribution was somewhat multi-modal, with bits below about 2.5 seconds stable rather than hopping. The largest range of Tref hopping was about 0.75 seconds. The *minimum* Tref for a hopper bit was about 2.5 seconds. The overall Tref distribution and other graphs are very similar to that of DUT #127 at 80C.

Figures 4.5-1 to 4.5-6 Test 92 #127 80C

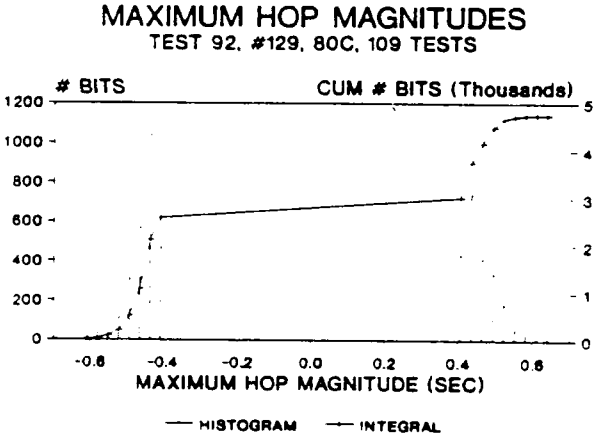




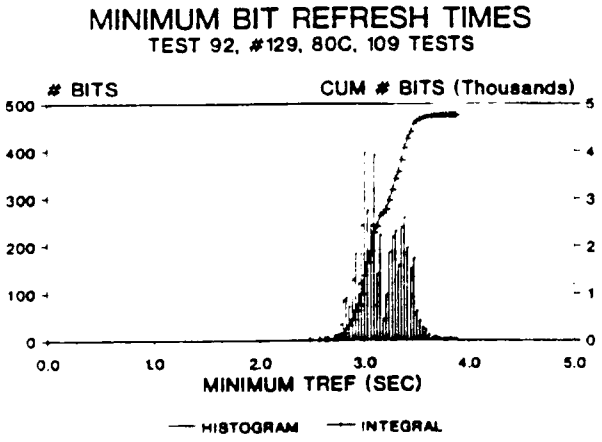
Bits with >= 2 hops



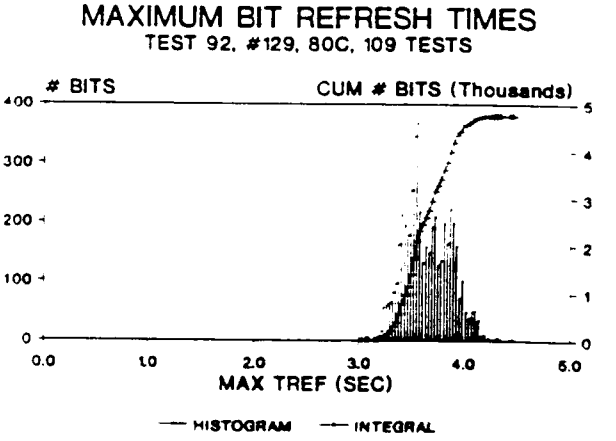
BITS WITH >=2 HOPS



BITS WITH >=2 HOPS

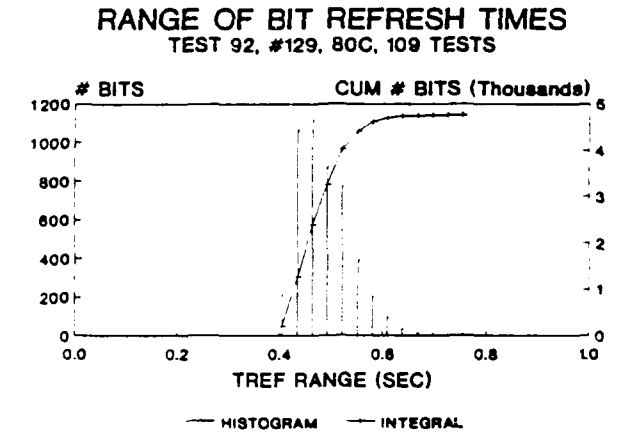


BITS WITH >=2 HOPS

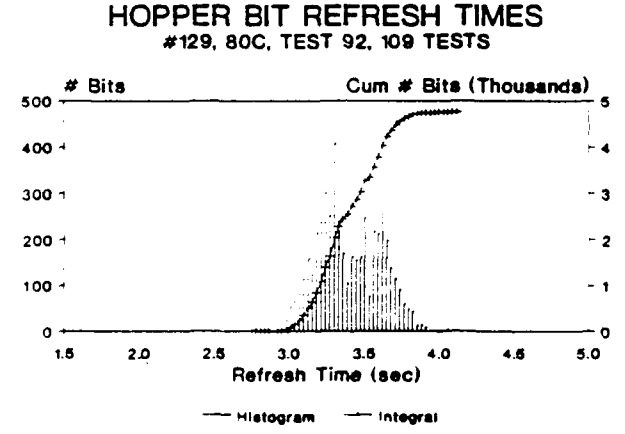


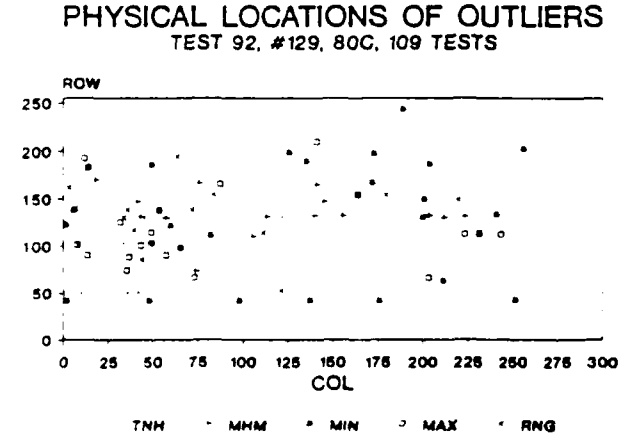
BITS WITH >=2 HOPS

Figures 4.5-7 to 4.5-9 Test 92 #129 80C



BITS WITH >=2 HOPS





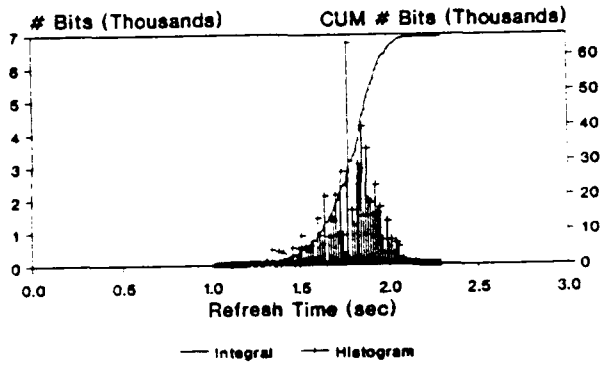
20 EACH

4.6 Test 93: Device #129, 85C

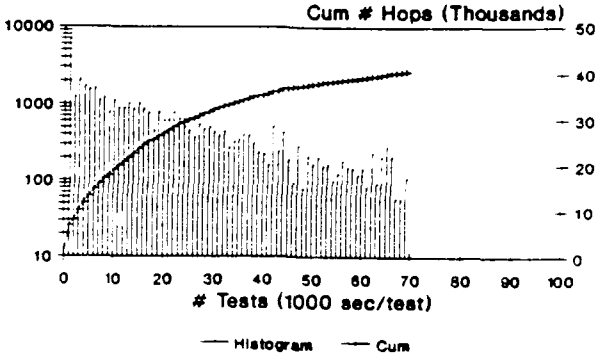
Here there were a couple of hopper bits which were in the low end of the Tref distribution. The largest range of Tref hopping was about 0.47 seconds. The minimum Tref for a hopper bit was about 1.2 seconds. The Ea of the mean of the initial Tref distribution was about 0.96ev, and the range of hopper bit average Tref Ea's was from about 0.8ev to 1.12ev. These Ea's are a little lower than DUT #127. This might be explained by a difference in the thermal characteristics of the socketing and thermocoupling of the two parts.

Figures 4.6-1 to 4.6-6 Test 93 #129 85C

BIT REFRESH TIMES
TEST 93, #129, 85C, 70 TESTS

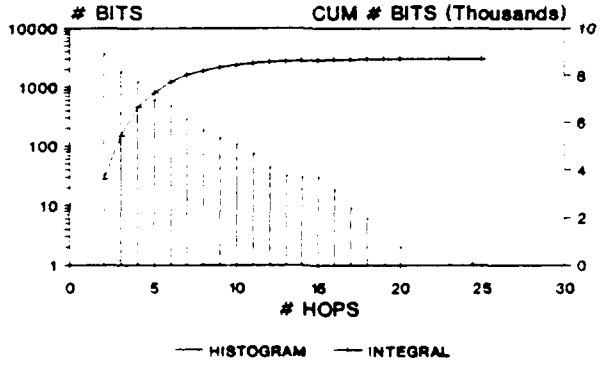


HISTOGRAM OF HOP DURATIONS
TEST 93, #129, 85C, 70 TESTS



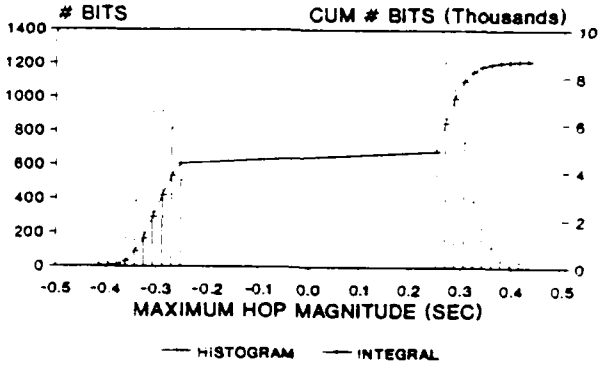
Bits with >= 2 hops

TOTAL NUMBER OF HOPS
TEST 93, #129, 85C, 70 TESTS



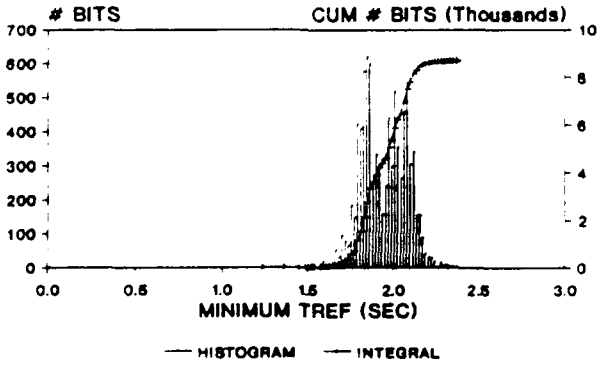
BITS WITH >=2 HOPS

MAXIMUM HOP MAGNITUDES
TEST 93, #129, 85C, 70 TESTS



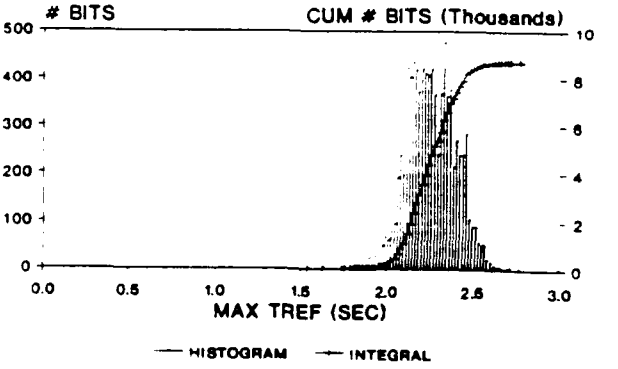
BITS WITH >=2 HOPS

MINIMUM BIT REFRESH TIMES
TEST 93, #129, 85C, 70 TESTS



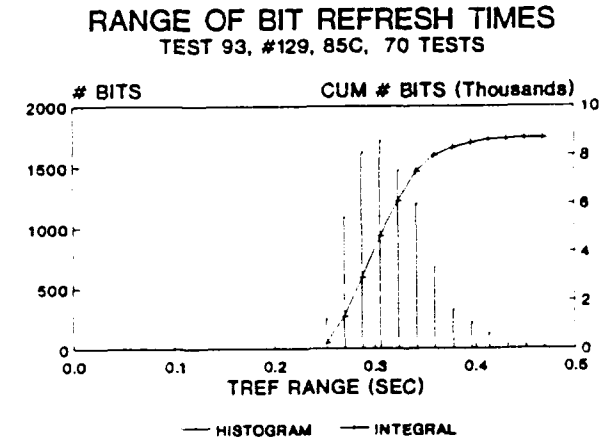
BITS WITH >=2 HOPS

MAXIMUM BIT REFRESH TIMES
TEST 93, #129, 85C, 70 TESTS

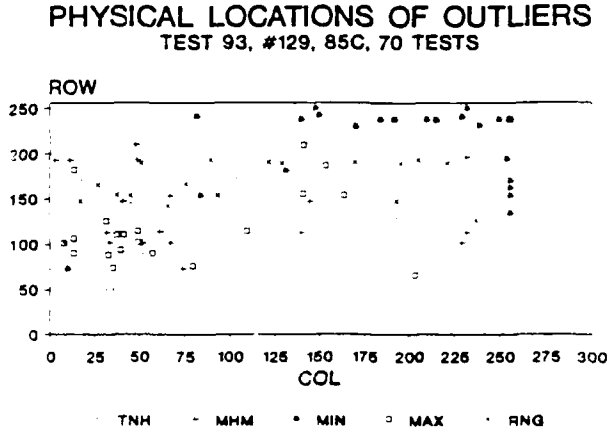


BITS WITH >=2 HOPS

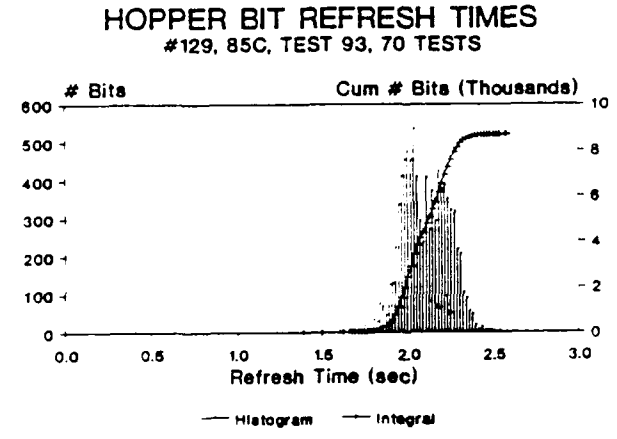
Figures 4.6-7 to 4.6-11 Test 93 #129 85C

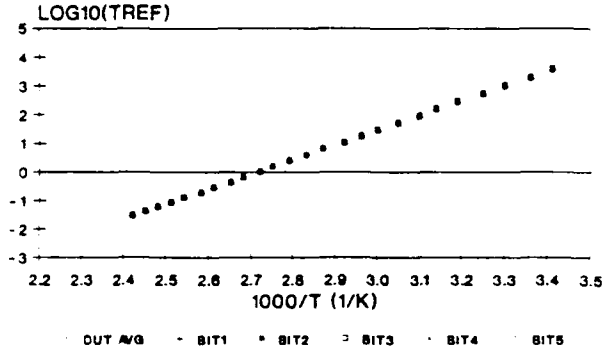


BITS WITH >2 HOPS

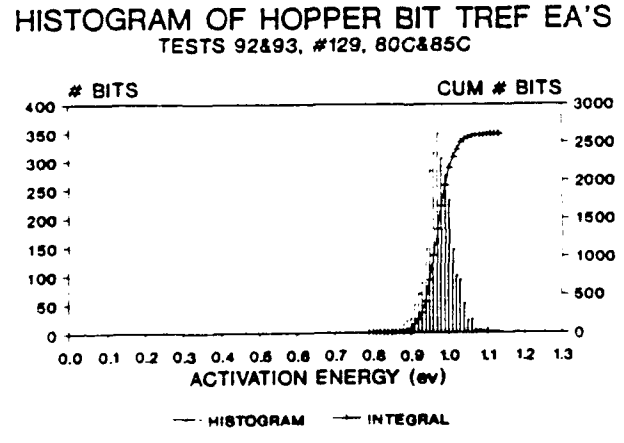


20 EACH





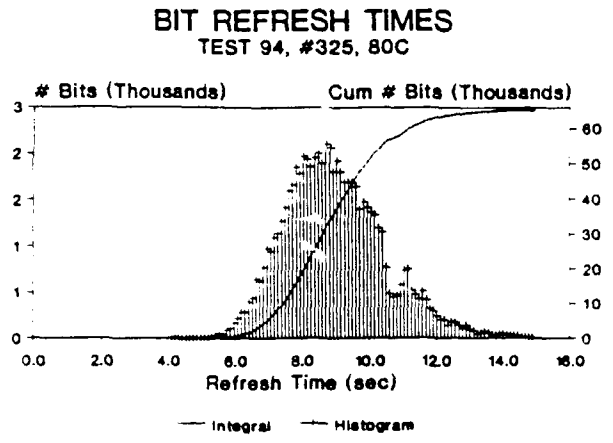
Ea's: .96 .97 .96 .96 .98 .97 (ev)

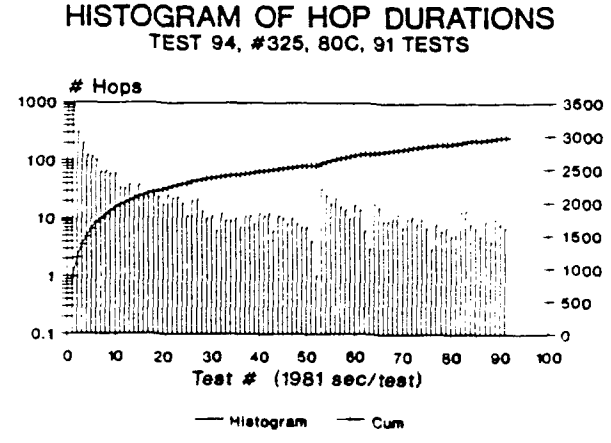


4.7 Test 94: Device #325, 80C

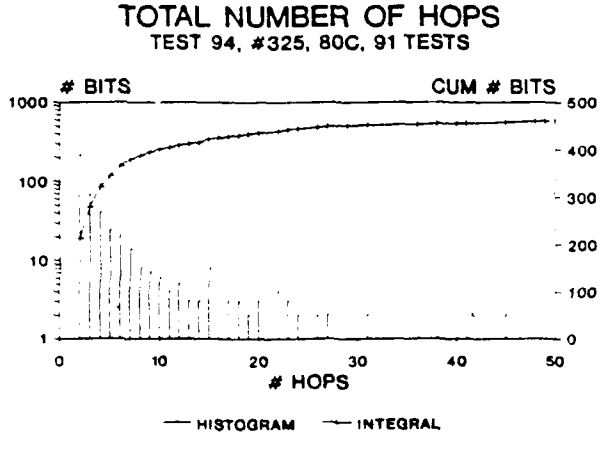
This DUT was from a different manufacturer than #'s 127 and 129. The Tref's were significantly higher, the Ea's are significantly lower and the Tref distribution is somewhat smoother. Again it appears that the low Tref bits are not hoppers. The largest range of Tref hopping was about 3.6 seconds. The minimum Tref for a hopper bit was about 5.4 seconds.

Figures 4.7-1 to 4.7-6 Test 94 #325 80C

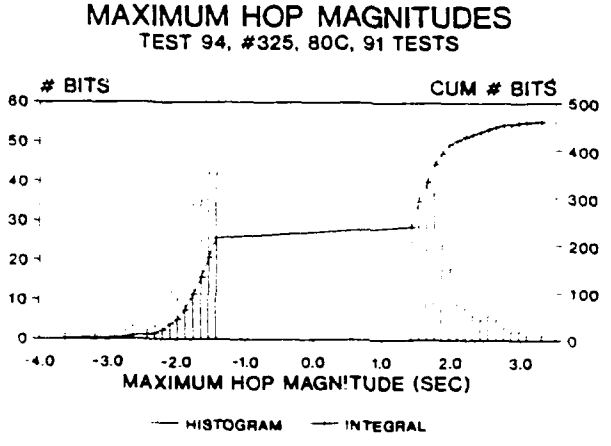




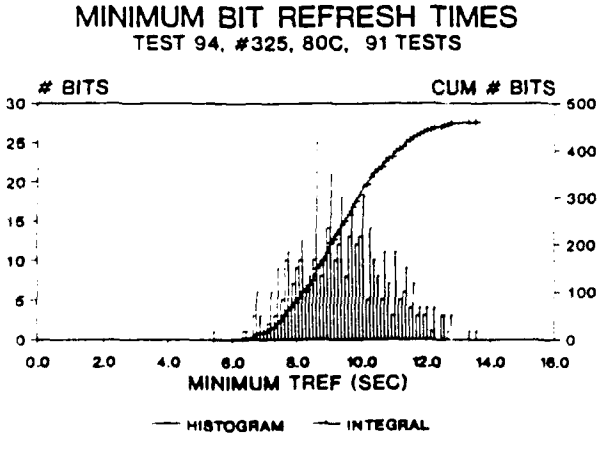
Bits with >= 2 hops



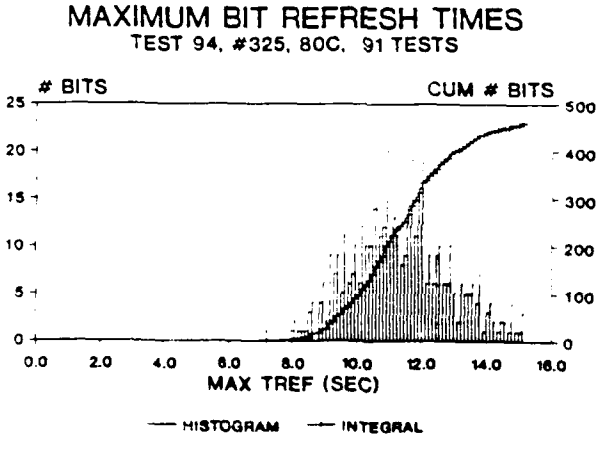
BITS WITH >=2 HOPS



BITS WITH >=2 HOPS

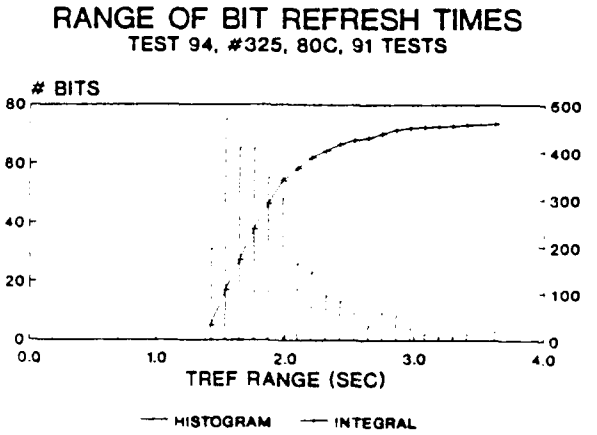


BITS WITH >=2 HOPS

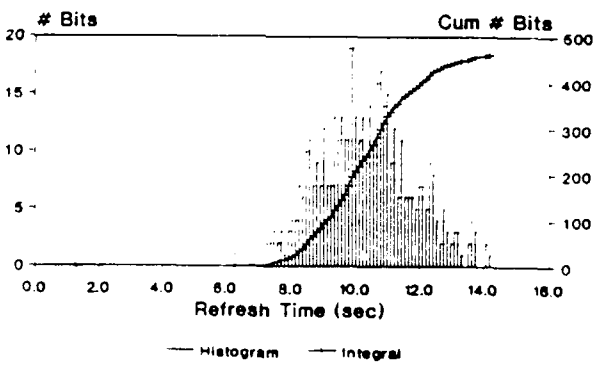


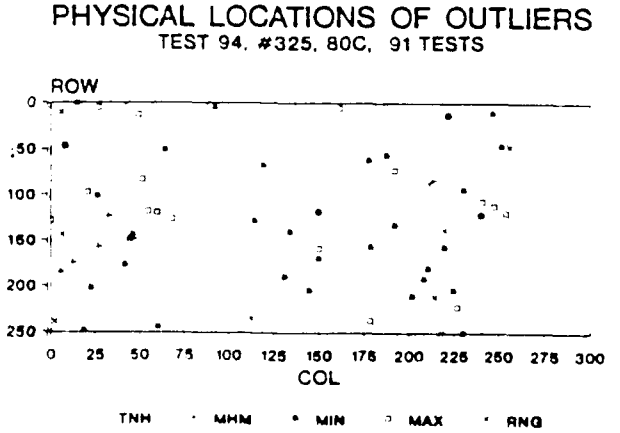
BITS WITH >=2 HOPS

Figures 4.7-7 to 4.7-9 Test 94 #325 80C



BITS WITH >=2 HOPS





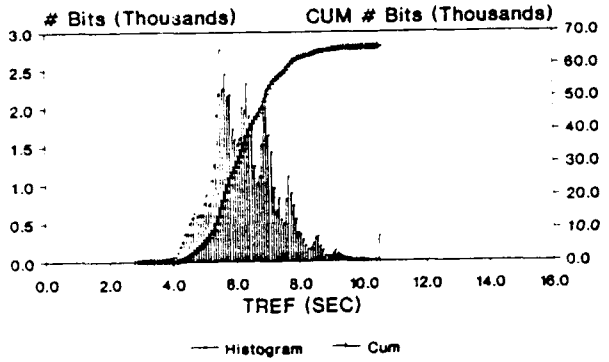
20 EACH

4.8 Test 95: Device #325, 85C

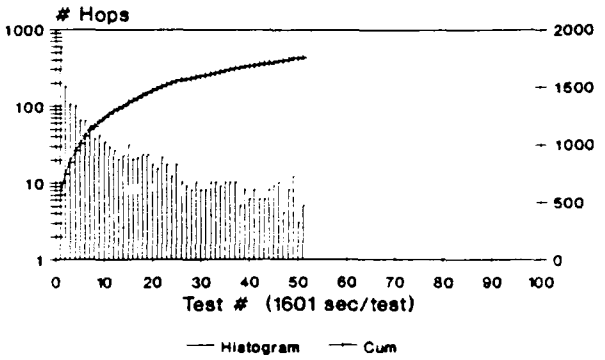
At this slightly higher temperature the Tref distribution was somewhat multi-modal. The largest range of Tref hopping was about 2.3 seconds. The minimum Tref for a hopper bit was about 3.8 seconds. Again the lowest Tref bits were not hoppers. The Ea of the mean of the initial Tref distribution was about 0.73ev, and the range of the hopper bit average Tref's was from about 0.5ev to 0.9ev. The physical locations of the outliers were scattered.

Figures 4.8-1 to 4.8-6 Test 95 #325 85C

BIT REFRESH TIMES
TEST 95, #325, 85C

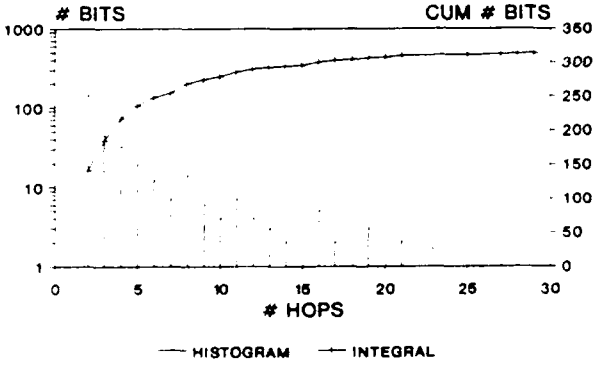


HISTOGRAM OF HOP DURATIONS
TEST 95, #325, 85C, 52 TESTS



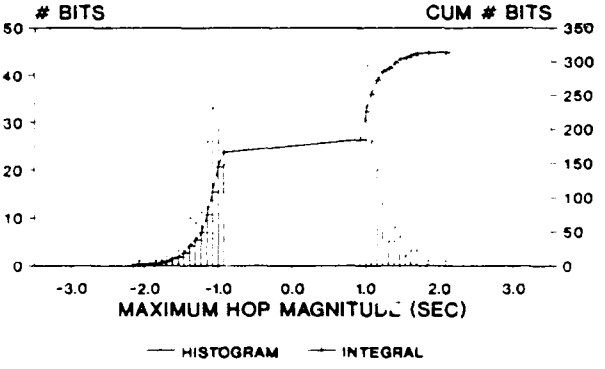
Bits with >= 2 hops

TOTAL NUMBER OF HOPS
TEST 95, #325, 85C, 52 TESTS



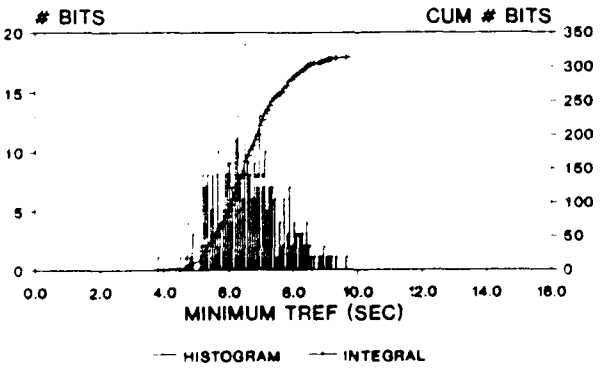
BITS WITH >=2 HOPS

MAXIMUM HOP MAGNITUDES
TEST 95, #325, 85C, 52 TESTS



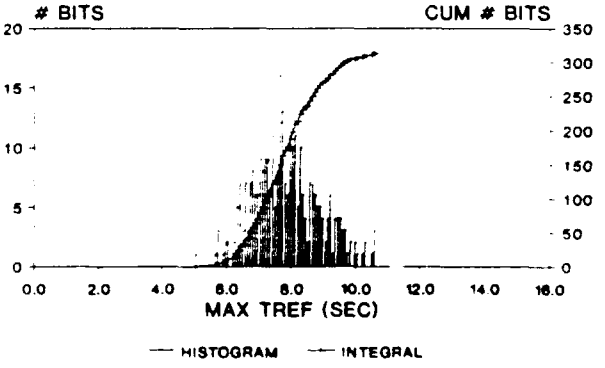
BITS WITH >=2 HOPS

MINIMUM BIT REFRESH TIMES
TEST 95, #325, 85C, 52 TESTS



BITS WITH >=2 HOPS

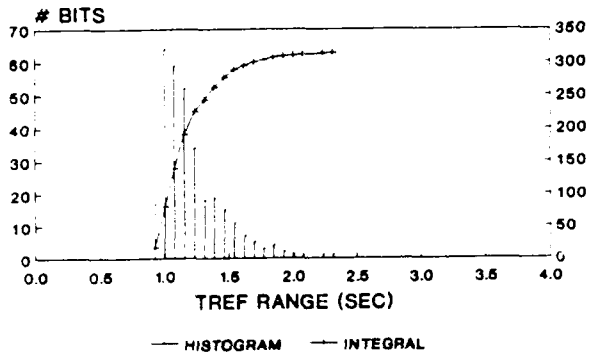
MAXIMUM BIT REFRESH TIMES
TEST 95, #325, 85C, 52 TESTS



BITS WITH >=2 HOPS

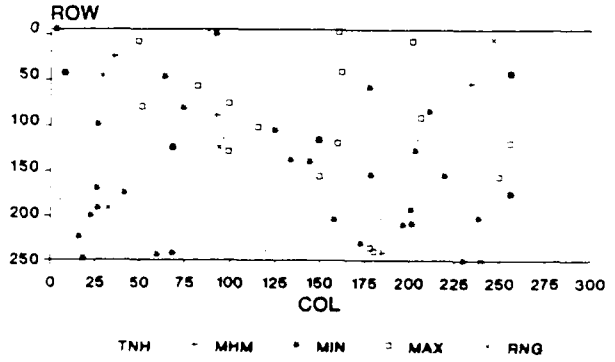
Figures 4.8-7 to 4.8-11 Test 95 #325 85C

RANGE OF BIT REFRESH TIMES
TEST 95, #325, 85C, 52 TESTS



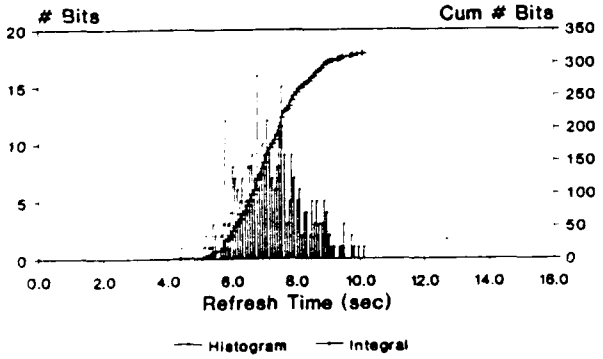
BITS WITH >=2 HOPS

PHYSICAL LOCATIONS OF OUTLIERS
TEST 95, #325, 85C, 52 TESTS

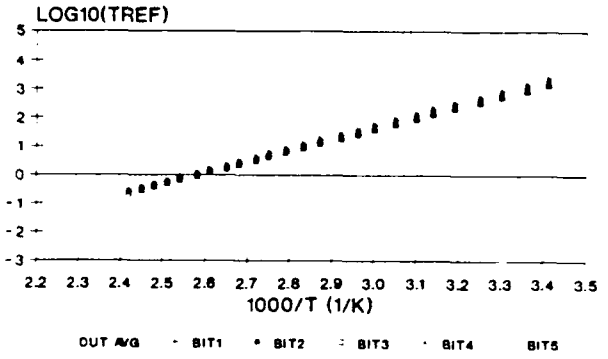


20 EACH

HOPPER BIT REFRESH TIMES
TEST 95, #325, 85C, 52 FILES

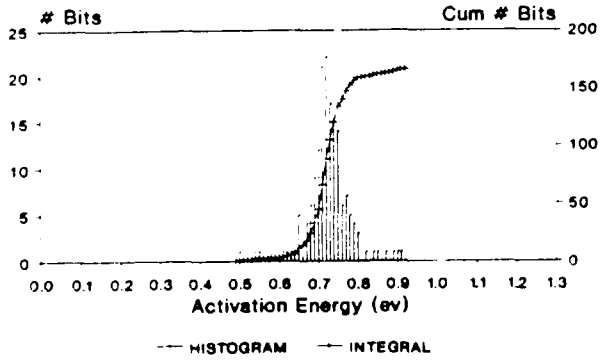


BIT AND DUT TREFAVG Ea PLOTS
TESTS 94&95 #325 80C&85C 5 HOPPER BITS



Ea's: .73 .69 .75 .71 .72 .71 (ev)

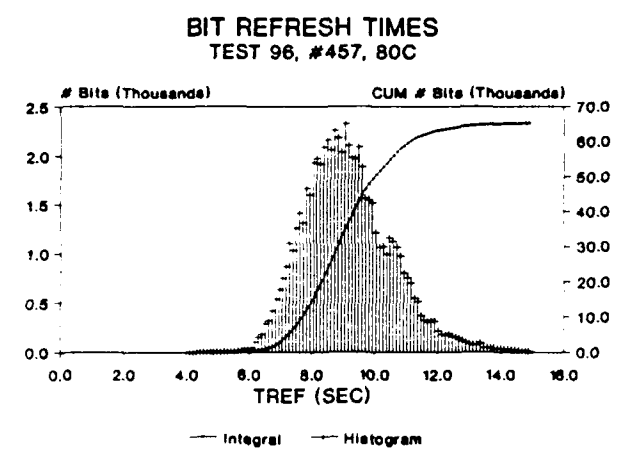
Eas of Hopper Bits
Tests 94&95 #325 80C&85C



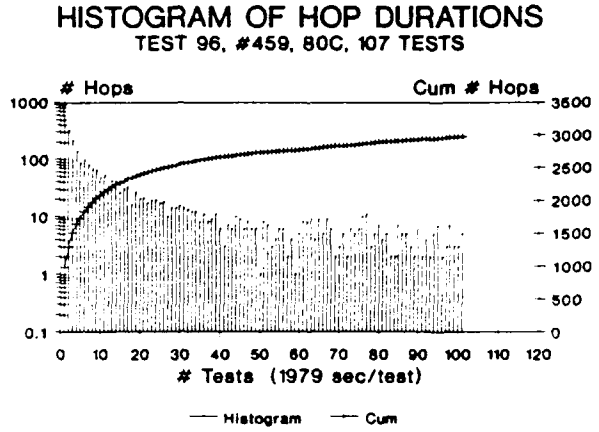
4.9 Test 96: Device #457, 80C

Again the lowest bits were not hoppers. The initial Tref was smooth and not multi-modal, although the tail is more extended to the higher values. The largest range of Tref hopping was about 3.3 seconds. The minimum Tref for a hopper bit was about 6.2 seconds.

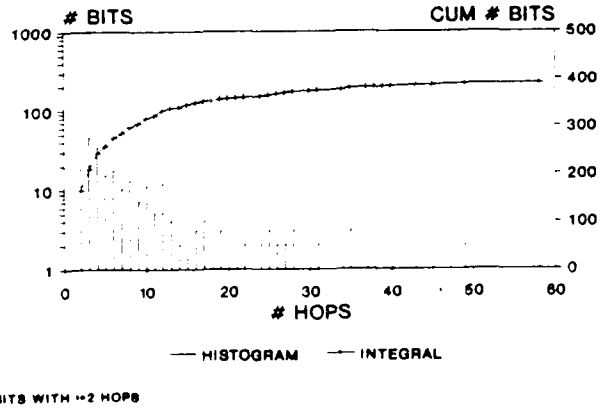
Figures 4.9-1 to 4.9-6 Test 96 #457 80C



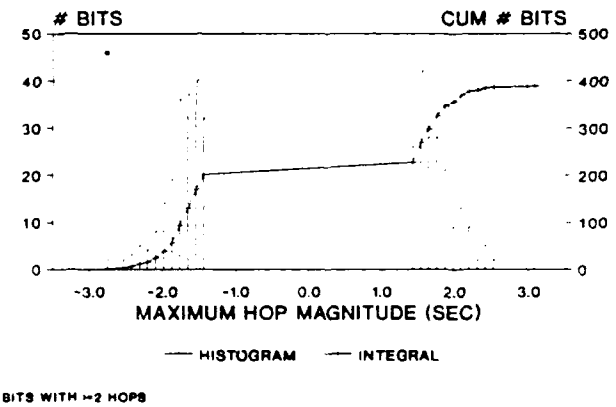
First Test



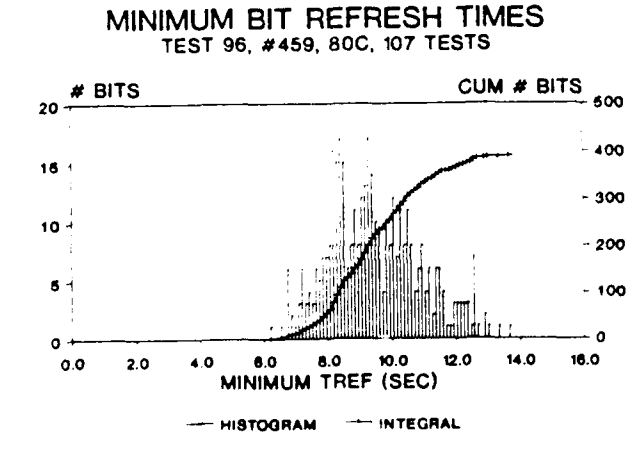
Bits with >= 2 hops



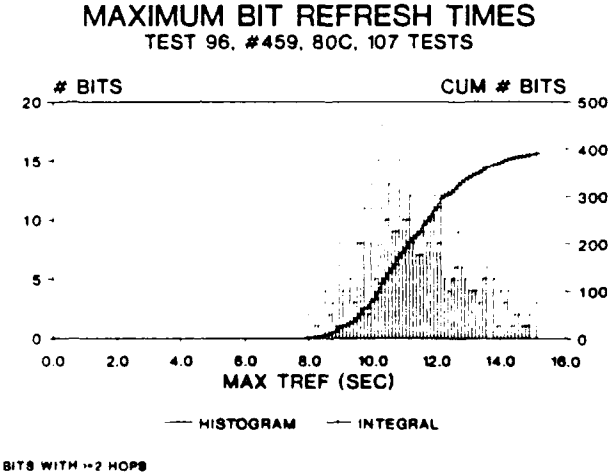
BITS WITH >=2 HOPS



BITS WITH >=2 HOPS

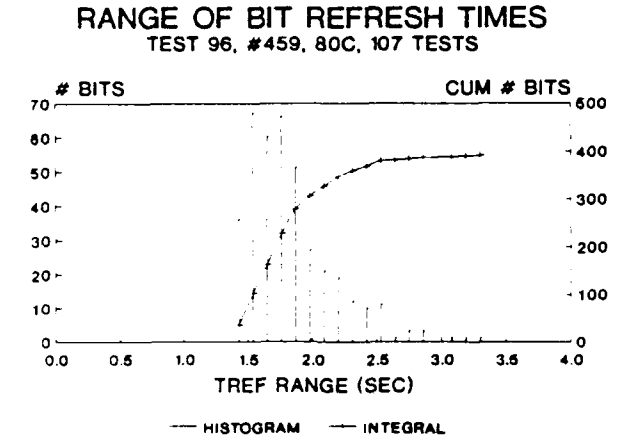


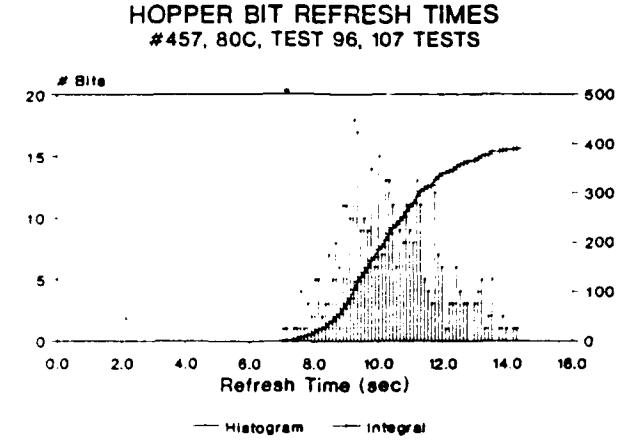
BITS WITH >=2 HOPS

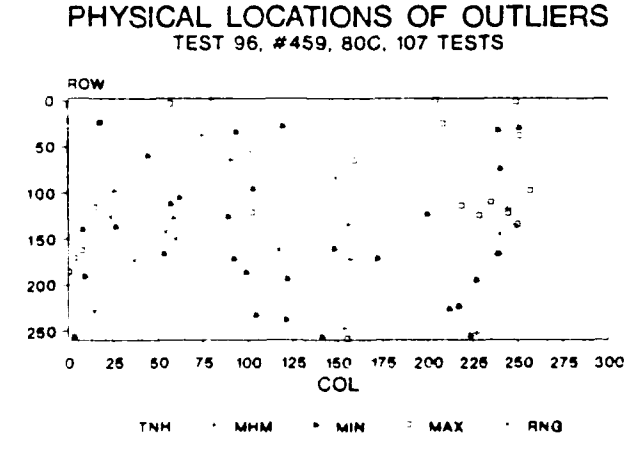


BITS WITH >=2 HOPS

Figures 4.9-7 to 4.9-9 Test 96 #457 80C





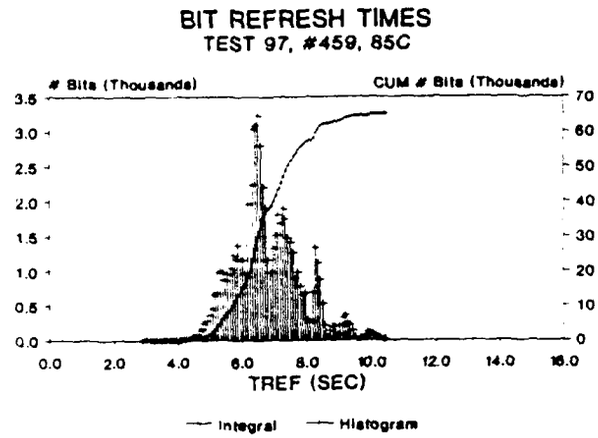


4.10 Test 97: Device #457, 85C

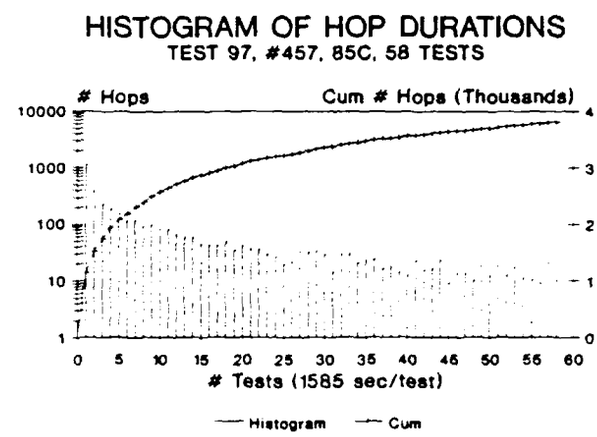
The Tref distribution was multi-modal at this temperature, and in this case the lowest Tref bits were hoppers. The largest range of Tref hopping was about 2.7 seconds. The minimum Tref for a hopper bit was about 4.8 seconds. The Ea of the mean of the initial Tref distribution was about 0.59ev, and the Ea's of hopper bit average Trefs was comparable, ranging between 0.4ev and 0.8ev.

The following sections concern the Tref, Tu and Td parameter activation energy analysis of hopper bits and the overall populations of hopper bits. These parameters were extracted as explained in Section 3.2.

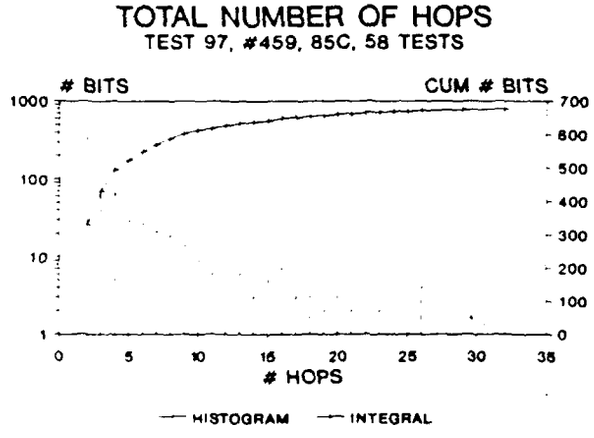
Figures 4.10-1 to 4.10-6 Test 97 #457 85C



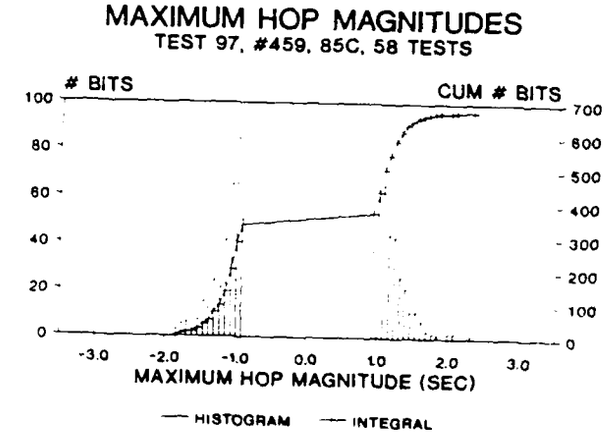
First Test



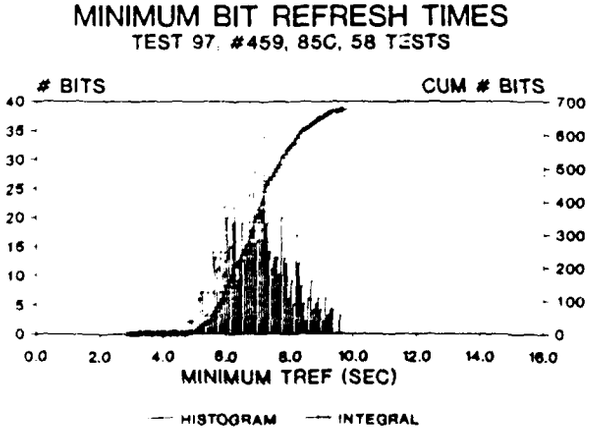
Bits with >= 2 hops



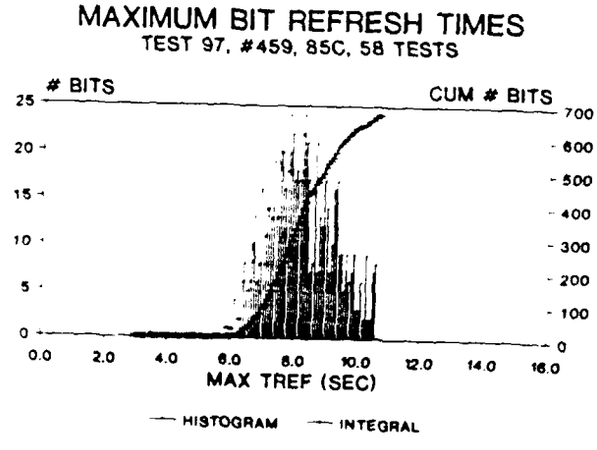
BITS WITH >=2 HOPS



BITS WITH >=2 HOPS

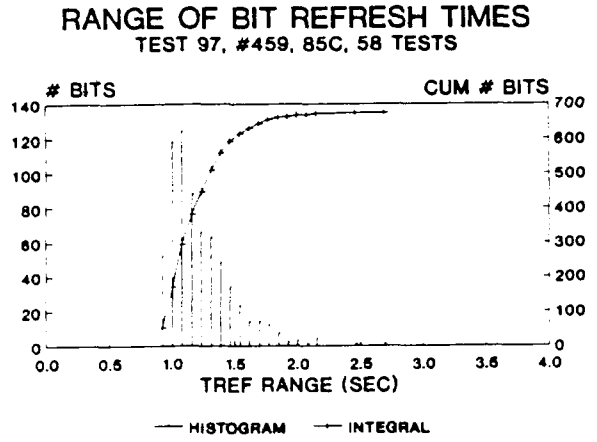


BITS WITH >=2 HOPS

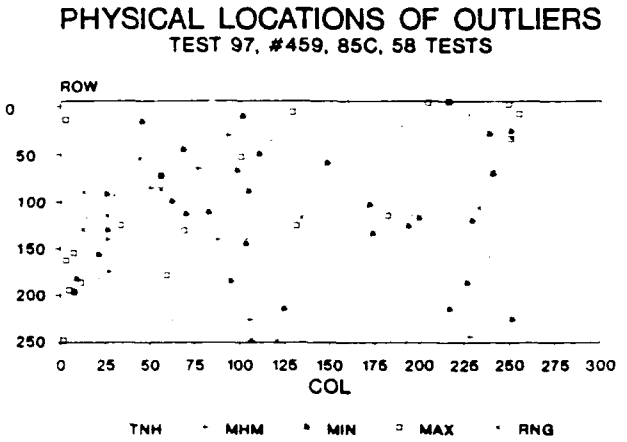


BITS WITH >=2 HOPS

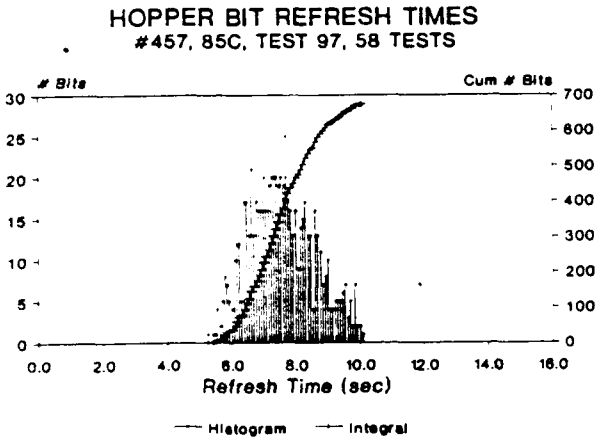
Figures 4.10-7 to 4.10-11 Test 97 #457 85C

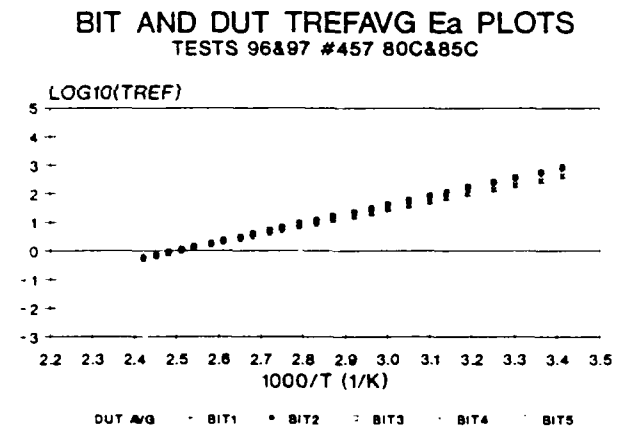


BITS WITH >2 HOPS

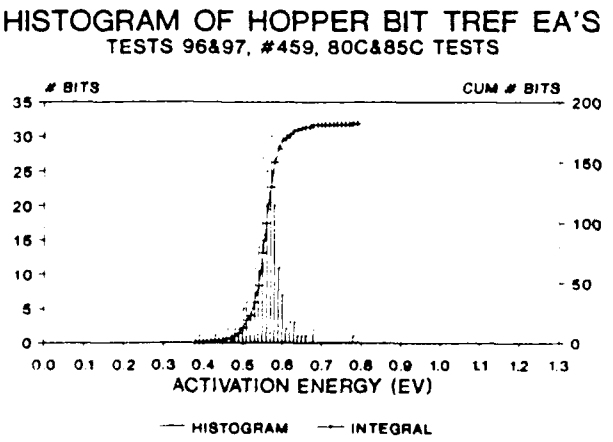


20 EACH





Ea's: .59 .50 .57 .59 .53 .53 (ev)



4.11 Individual Bit Characteristics - Test 40 and Test 41: DUT #7

Table 4.11-1 shows a summary of the average Tref values, Tu and Td parameter values and their activation energies for all the individual bits which hopped by at least the minimum threshold amount, at least 5 times, at both temperatures (for Tests 40&41). The two test temperatures were chosen to be very close together in an attempt to measure the activity of the same trap(s). The column labels mean logical column, logical row, # of hops (cold), # hops (hot), Tref average (cold), Tref average (hot), Ea of Tref average, extracted Tu parameter value (cold), extracted Tu parameter value (hot), Ea of Tu parameter, extracted Td parameter value (cold), extracted Td parameter value (hot), Ea of Td parameter, Ea of Tu/Td, and Ea of Tu*Td. The Trefavg Ea's were calculated as before, with the pre-exponential A(V,T) term, and the Tu and Td Ea's are simple activation energies, without a temperature dependent pre-exponential factor.

Figures 4.11-1 through 4.11-5 are a histograms of the Ea's listed in Table 4.11-1 (Tref average, Tu, Td, Tu/Td, and Tu*Td). Note that the Ea's were binned to bins 2ev wide, so those lower than 2ev are shown as 2ev. The Ea of Tu and Td, are very large. Figures 4.11-6 through 4.11-9 are scatter plots of the Ea's of Tu, Td, Tu/Td and Tu*td vs Ea of Tref, respectively. There is no clear pattern of correlation.

Six individual bits were selected which had a fair number of hops at each temperature. For these bits, we made a plot of Tref vs test time, a histogram of hop magnitudes, and a histogram of Tu and Td durations (from which the Tu and Td parameters were extracted). This gives insight into how reliable the parameter extractions probably were. Figure 4.11-10 shows the Tref vs time waveforms for the first three selected bits at two temperatures. Figure 4.11-11 shows the plots for the other three. The diagonal lines represent times during which the Tref must have changed between the two levels in multiple hops which were smaller than the threshold chosen to trigger recording as a hop.

Most of the bits (1-4) apparently had more than one trapping center actively populating and unpopulating, especially at the higher temperature. The Tu and Td parameter extractions are valid only if there is one trapping center active. Bits 5 and 6 (col,row=142,153 and 181,200, respectively) are probably the closest to being dominated by one trap. Bit 5 was mostly low, with short hops up, and its Ea of Tu was 0.8ev. Bit 6 was mostly high, with short hops down, and its Ea of Td was 1.3ev.

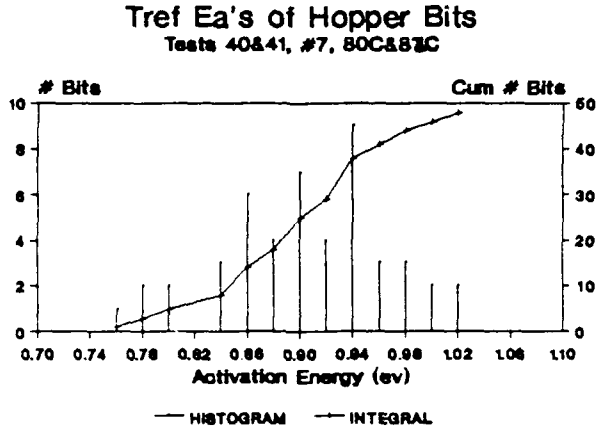
Figures 4.11-12 and 4.11-13 show histograms of the hop magnitudes extracted from the Tref waveforms. The fact that there are two centers hopping is not always apparent in these histograms, although it is quite clear in some of them.

Finally, Figures 4.11-14 and 4.11-15 show the histograms of Tu and Td durations. The least squares fits from which the Tu and Td parameters were extracted are also shown. Very flat and low curves have few hops at each temperature, and the parameter extractions are less meaningful. Multiple trapping centers cannot always be easily recognized in these plots either, unless they happen to have different duration parameters. In that case there would be two regions in the curves with different slopes. From these curves, it would appear that the data is best for bits 3 and 5.

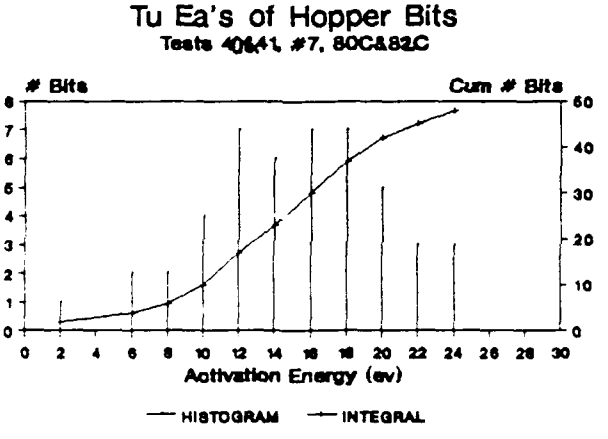
Table 4.11-1
Test 40/41 Hopper Bit Tref, Tu, Td Values and Activation Energies

Selected bit #															
↓ col	row	#hc	#hh	Trc	Trh	EaTr	Tu c	Td c	Ea Tu	Td c	Td h	Ea Td	Ea Tu*Td	Ea Tu/Td
0	3	29	166	8.6	7.2	0.91	180.0	9.7	15.5	13.3	3.8	6.7	8.8	22.2
0	127	13	187	9.1	7.6	0.94	180.0	4.3	19.9	59.0	5.0	13.1	6.8	33.0
2	174	25	169	9.4	7.7	0.96	129.8	1.2	25.0	135.6	10.1	13.8	11.2	38.9
9	143	14	176	8.6	7.2	0.87	140.3	6.4	16.5	105.7	6.3	15.0	1.4	31.5
11	40	18	174	8.7	7.3	0.92	80.3	2.3	19.0	106.7	5.8	15.5	3.6	34.5
① 29	224	32	194	8.5	7.2	0.79	48.5	5.6	11.5	171.6	4.9	19.0	-7.5	30.5
41	191	24	200	9.1	7.6	0.89	123.8	2.3	21.3	98.5	9.6	12.4	8.9	33.7
46	255	18	197	8.9	7.4	0.95	120.6	3.2	19.3	105.9	2.6	19.7	-0.4	38.9
48	255	14	147	9.2	7.7	0.91	180.0	12.9	14.0	103.9	1.1	24.3	-10.2	38.3
49	221	8	176	8.7	7.4	0.81	180.0	6.4	17.8	180.0	2.2	23.5	-5.8	41.3
④ 64	254	33	156	9.0	7.6	0.87	100.9	2.9	19.0	91.9	10.2	11.7	7.3	30.7
66	229	13	208	8.6	7.1	0.99	180.0	3.8	20.5	196.3	0.9	28.6	-8.0	49.1
71	175	11	169	8.6	7.2	0.91	119.6	11.9	12.3	180.0	6.5	17.7	-5.4	30.0
72	239	7	185	8.6	7.1	0.97	180.0	5.8	18.3	125.9	4.5	17.8	0.6	36.1
74	255	21	163	8.6	7.1	0.92	102.2	6.5	14.7	69.2	8.8	11.0	3.7	25.7
② 92	255	28	211	8.8	7.6	0.77	96.2	1.3	22.8	158.4	2.6	21.9	1.0	44.7
96	159	11	122	8.6	7.2	0.90	180.0	30.3	9.5	63.6	21.7	5.7	3.7	15.2
103	231	20	215	9.1	7.5	0.98	146.9	2.8	21.1	118.6	1.6	23.0	-1.9	44.2
105	157	10	170	9.2	7.6	0.94	180.0	21.9	11.2	117.3	3.8	18.3	-7.1	29.5
121	246	6	151	8.6	7.0	1.00	180.0	16.4	12.8	125.9	0.4	30.3	-17.6	43.1
122	223	37	210	8.8	7.4	0.84	9.3	2.9	6.3	139.6	3.9	19.1	-12.8	25.4
131	255	5	196	8.6	7.1	0.93	180.0	7.2	17.1	125.9	5.5	16.7	0.4	33.9
133	136	17	165	8.8	7.4	0.87	72.8	5.0	14.2	180.0	3.9	20.4	-6.1	34.6
133	247	8	215	8.6	7.1	0.95	180.0	2.2	23.3	180.0	1.3	26.2	-2.8	49.5
⑤ 142	153	99	136	8.6	7.0	1.02	24.4	21.0	0.8	25.9	0.4	21.7	-20.9	22.5
145	127	17	186	8.6	7.2	0.85	88.0	3.7	16.9	180.0	4.2	20.0	-3.1	36.9
147	26	6	88	8.6	7.0	1.01	180.0	2.8	22.1	125.9	13.6	11.9	10.2	34.0
149	167	11	168	8.7	7.4	0.87	180.0	7.6	16.9	180.0	9.9	15.4	1.4	32.3
161	136	10	165	8.8	7.3	0.96	180.0	5.8	18.3	180.0	18.5	12.1	6.2	30.4
167	181	11	170	8.8	7.4	0.87	125.9	13.6	11.8	180.0	5.5	18.6	-6.7	30.4
③ 172	144	69	214	8.8	7.5	0.79	22.9	4.5	8.7	55.4	0.6	23.7	-15.0	32.5
172	176	13	138	8.8	7.3	0.89	56.0	17.2	6.3	180.0	24.0	10.7	-4.4	17.0
174	192	10	29	8.6	7.0	1.02	180.0	91.6	3.6	113.4	14.4	11.0	-7.4	14.6
181	160	8	166	8.8	7.4	0.87	91.6	7.1	13.6	14.4	2.2	10.0	3.6	23.6
⑥ 181	200	20	46	9.3	7.8	0.90	122.9	1.3	24.0	153.2	118.9	1.3	22.7	25.4
183	239	16	189	8.7	7.2	0.93	84.9	8.7	12.1	103.9	2.3	20.2	-8.1	32.4
191	229	13	169	8.6	7.2	0.88	63.6	7.8	11.2	180.0	11.9	14.5	-3.3	25.7
191	234	6	173	8.6	7.2	0.91	180.0	10.3	15.3	180.0	9.2	15.8	-0.6	31.1
195	184	13	154	9.0	7.4	0.98	180.0	1.6	25.2	88.0	8.6	12.4	12.8	37.6
217	191	14	162	8.6	7.1	0.94	118.7	9.6	13.4	71.3	2.3	18.3	-4.9	31.7
218	63	8	179	8.6	7.1	0.94	180.0	7.1	17.2	103.9	1.8	21.6	-4.4	38.8
220	215	11	168	8.7	7.3	0.84	125.9	2.4	21.1	180.0	11.5	14.6	6.4	35.7
228	208	9	153	8.8	7.3	0.91	125.9	3.7	18.8	180.0	7.8	16.8	2.0	35.5
237	164	12	157	8.7	7.3	0.94	180.0	11.2	14.8	96.3	5.9	14.9	0.0	29.7
245	146	8	188	8.6	7.1	0.94	180.0	3.2	21.4	180.0	1.8	24.6	-3.1	46.0
255	158	8	144	9.2	7.6	0.94	180.0	13.5	13.8	125.9	7.3	15.2	-1.4	28.9
255	159	9	161	8.8	7.4	0.88	180.0	13.2	13.9	180.0	7.0	17.3	-3.3	31.2
255	189	113	250	8.7	7.4	0.80	6.9	0.3	17.1	8.5	1.7	8.7	8.4	25.9

Figures 4.11-1 to 4.11-5 Tref, Tu, and Td Parameter Activation Energies (DUT #7, All Hopper Bits with >=5 hops)



>=6 HOPS



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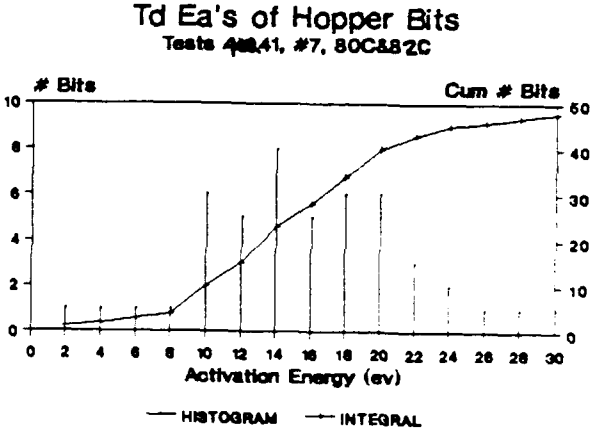

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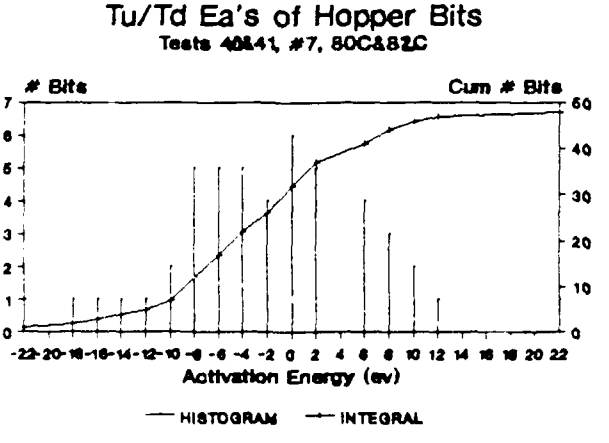

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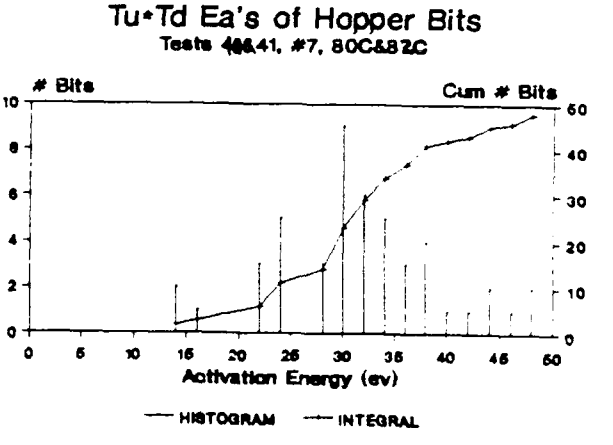
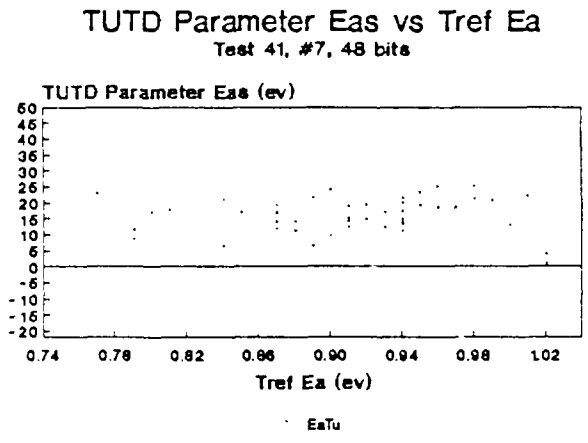
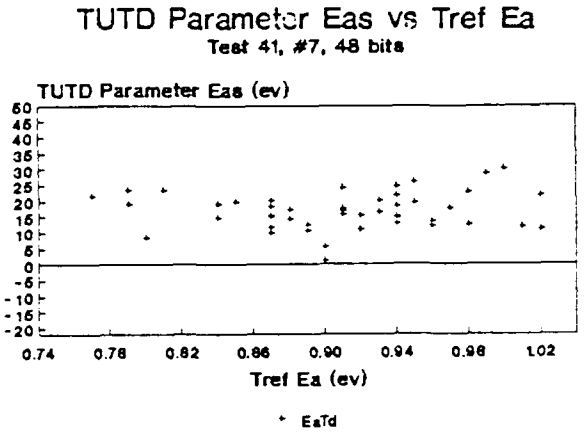
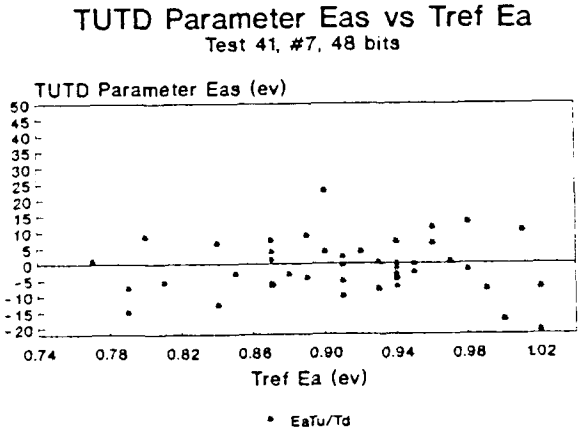


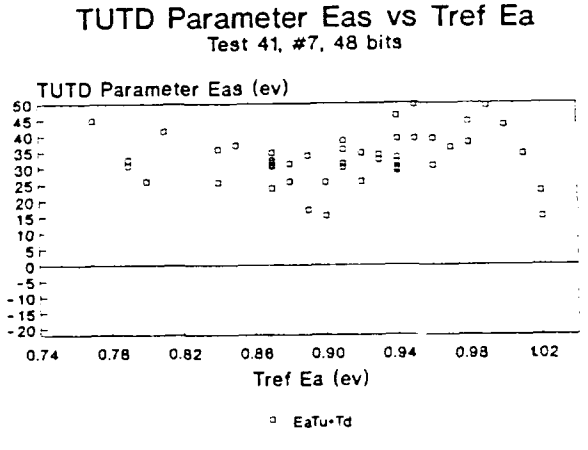
>=6 HOPS (Bits at 7.1&17.8ev not shown)

Figures 4.11-6 to 4.11-9 Tu, Td, Tu/Td and Tu*Td Ea's vs Tref Ea's
(DUT #7, All Hopper Bits with >=5 hops)

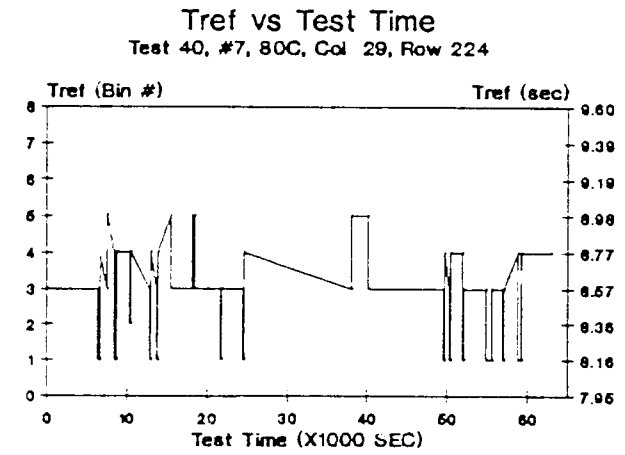




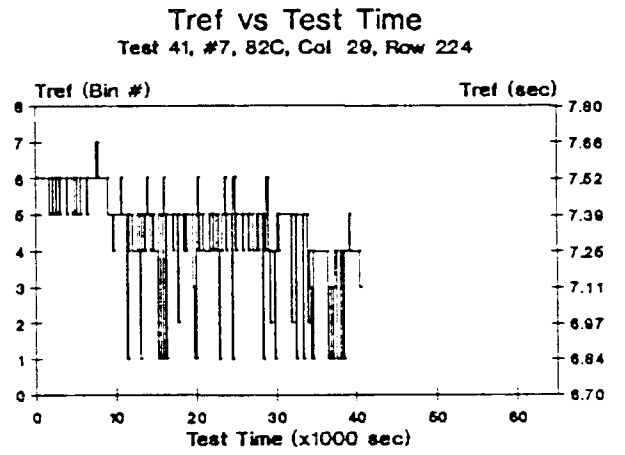




Figures 4.11-10a to 4.11-10f Tref vs Test Time Waveforms
(DUT #7, selected bits 1-3, each at two temperatures)



350 tests



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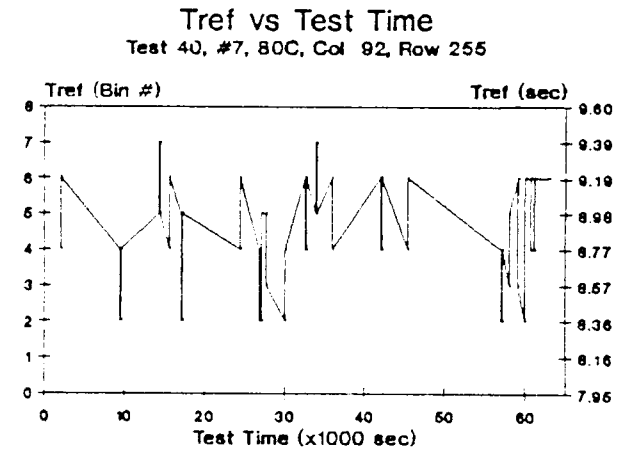

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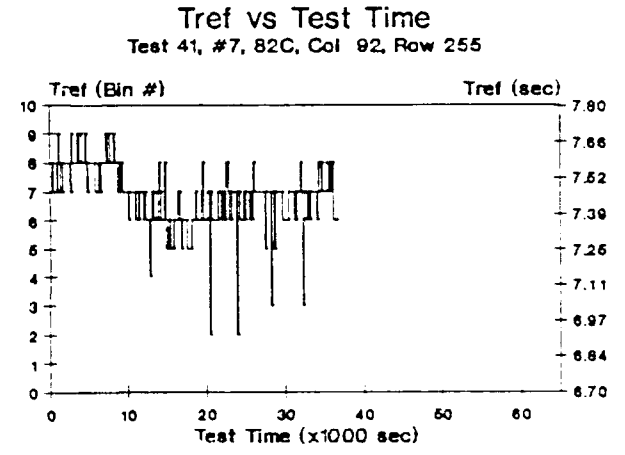

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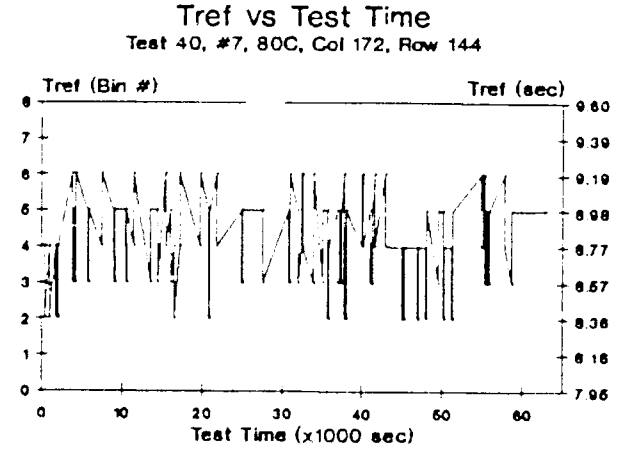

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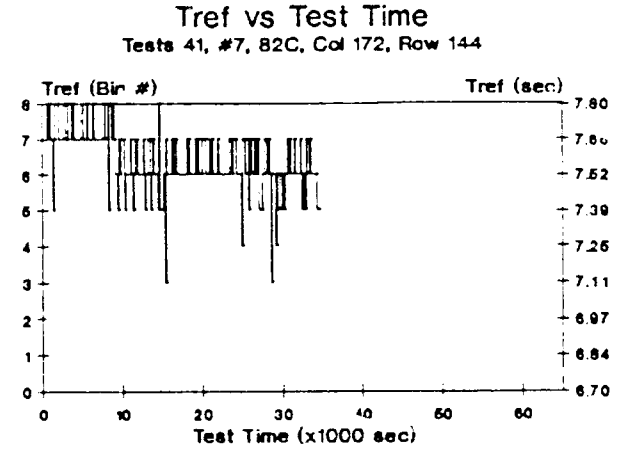
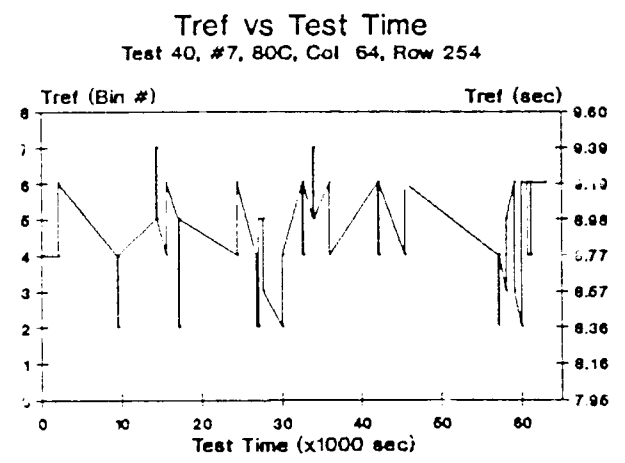


350 tests

Figures 4.11-11a to 4.11-11f Tref vs Test Time Waveforms
(DUT #7, selected bits 4-6, each at two temperatures)



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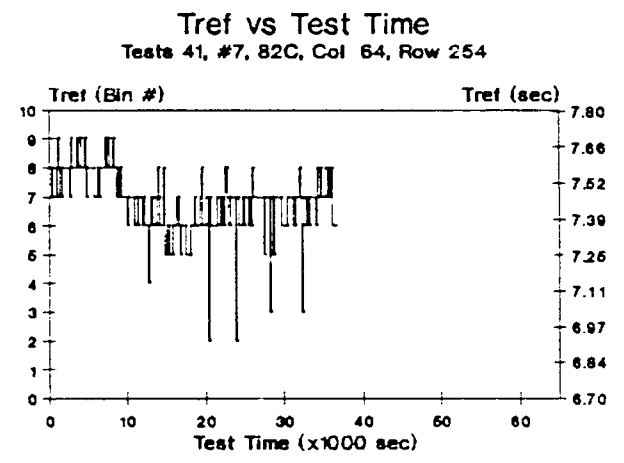

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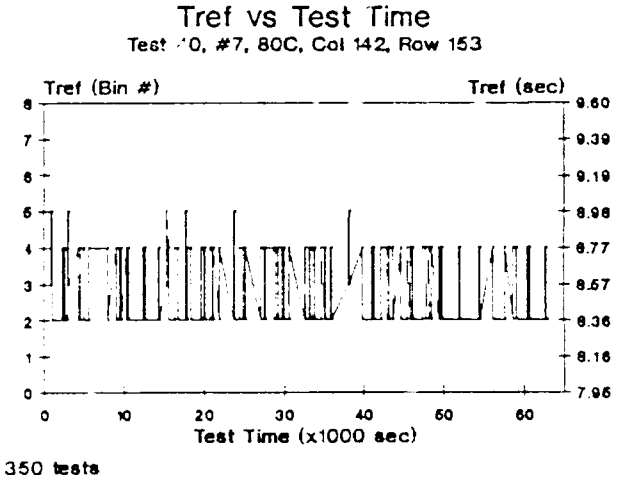

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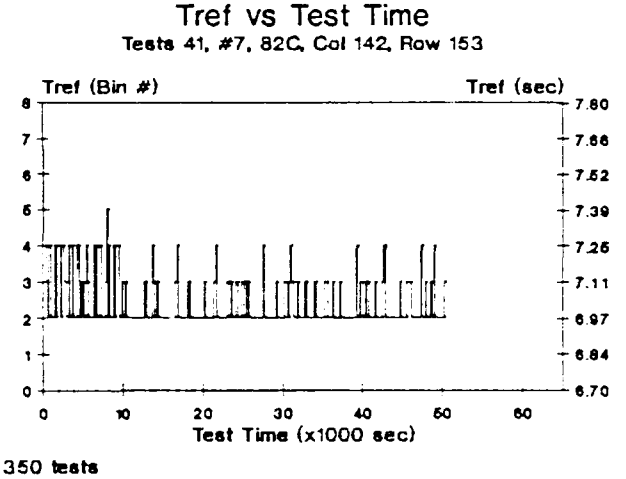

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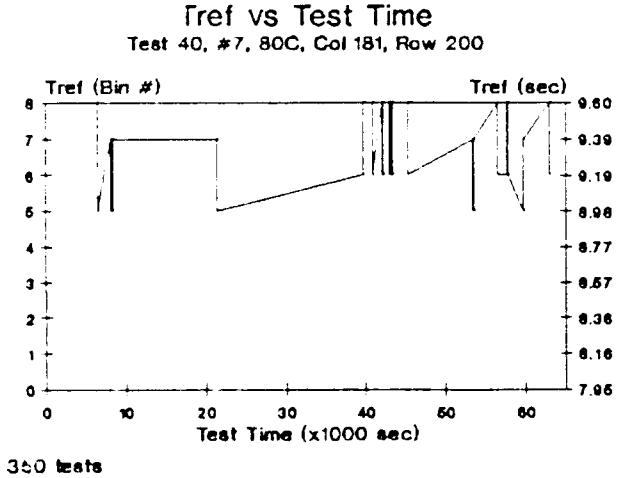

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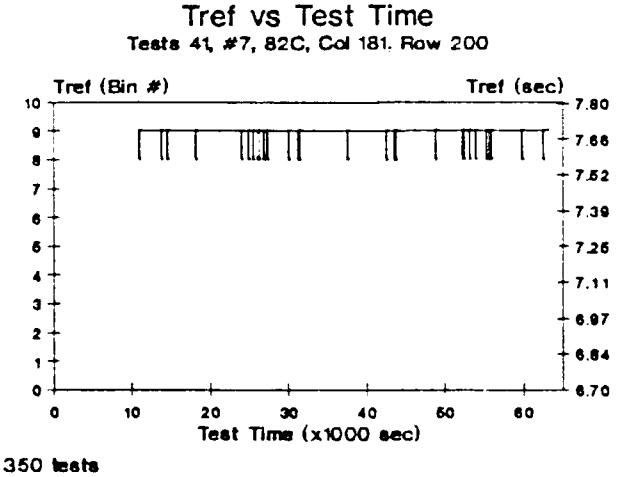
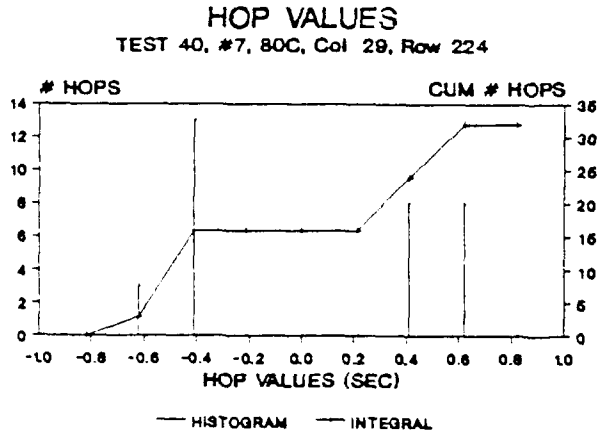
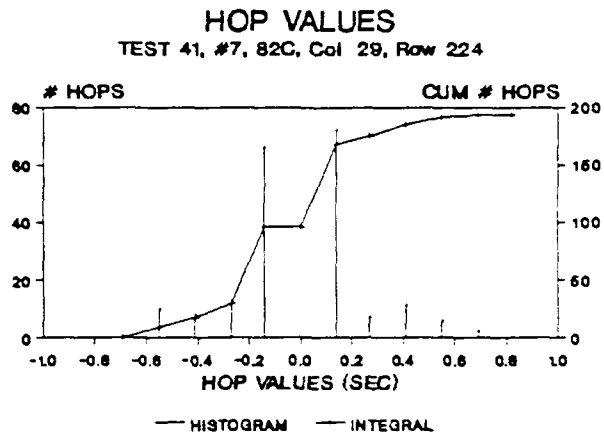
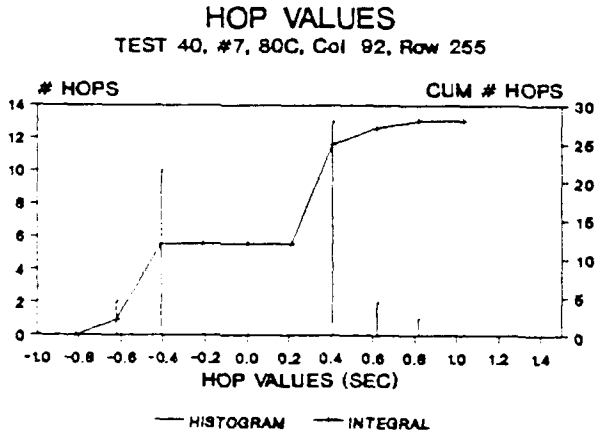


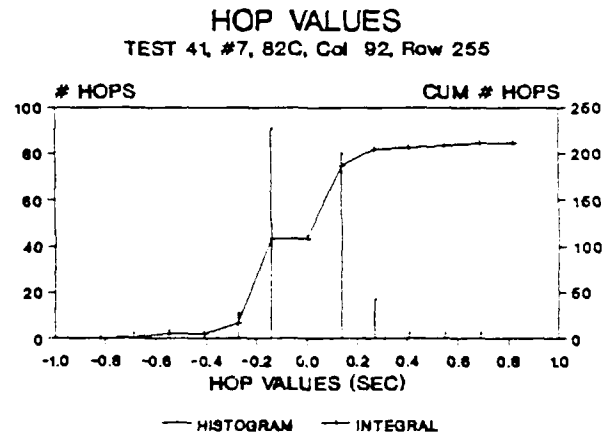
350 tests

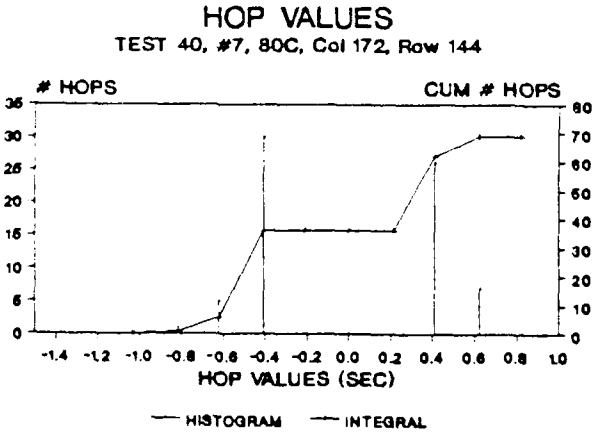
Figures 4.11-12a to 4.11-12f Hop Value Histograms
(DUT #7, selected bits 1-3, each at two temperatures)

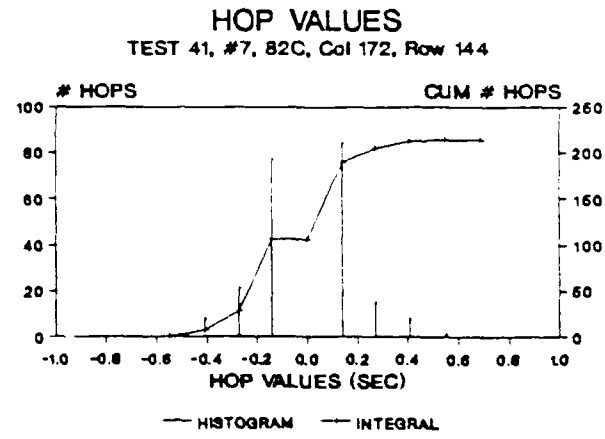




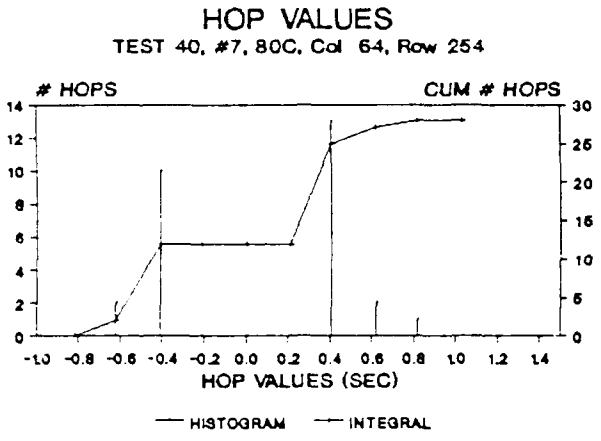


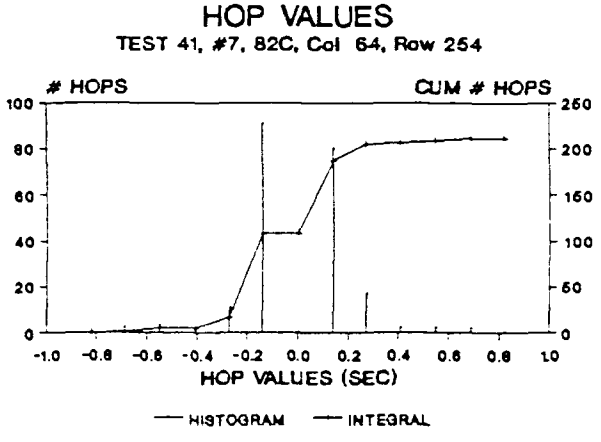


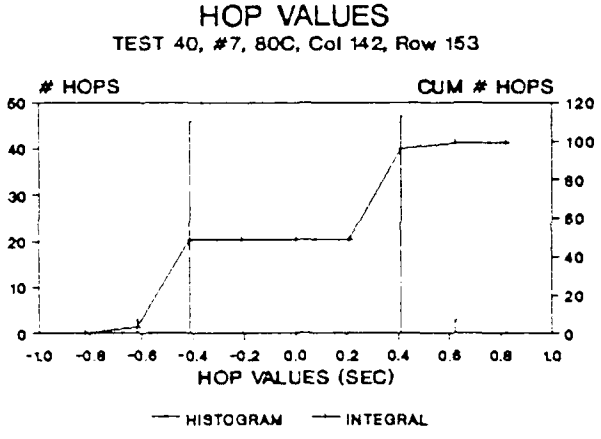


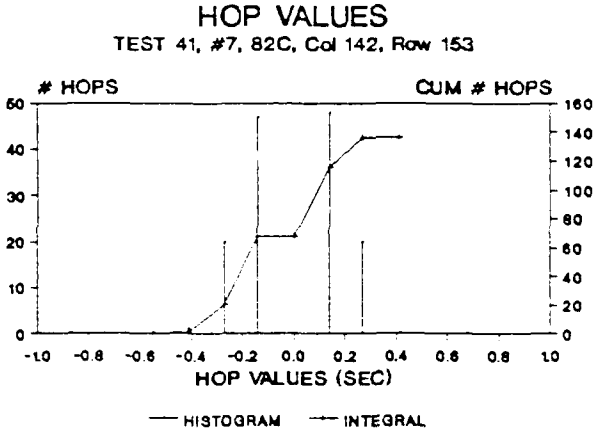


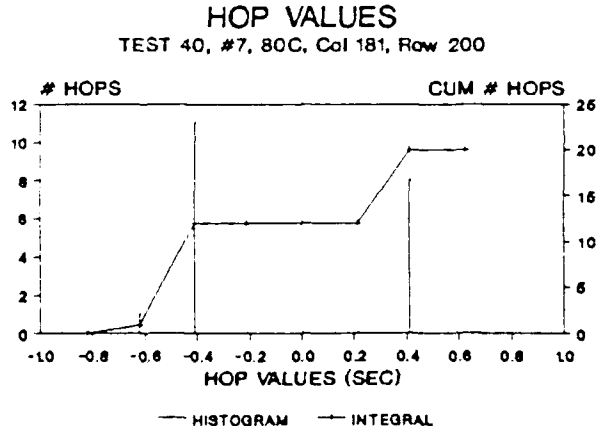
Figures 4.11-13a to 4.11-13f Hop Value Histograms
(DUT #7, selected bits 4-6, each at two temperatures)

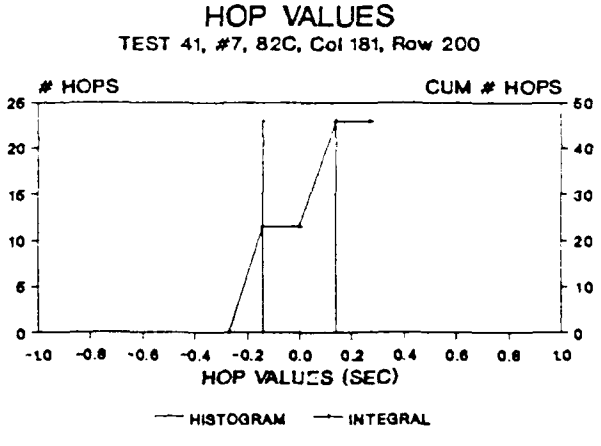




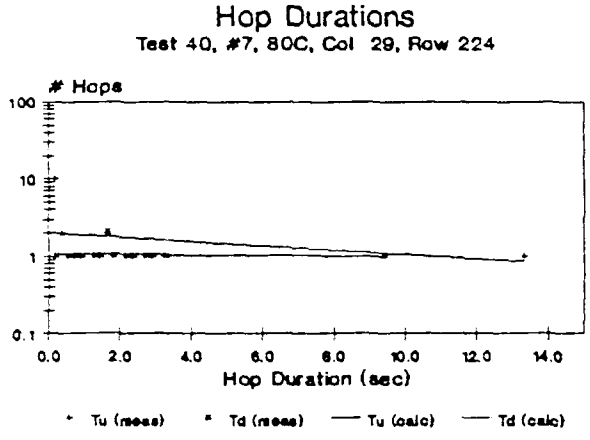


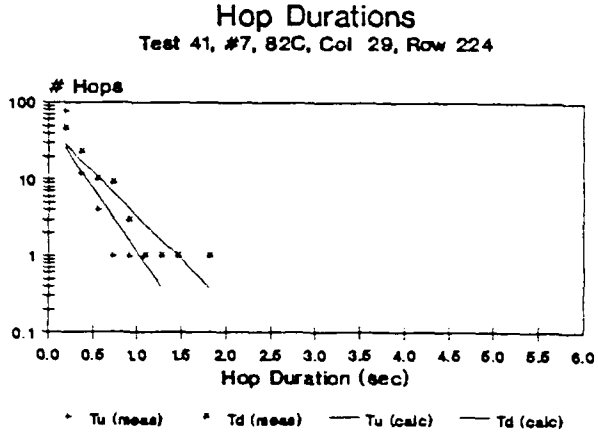


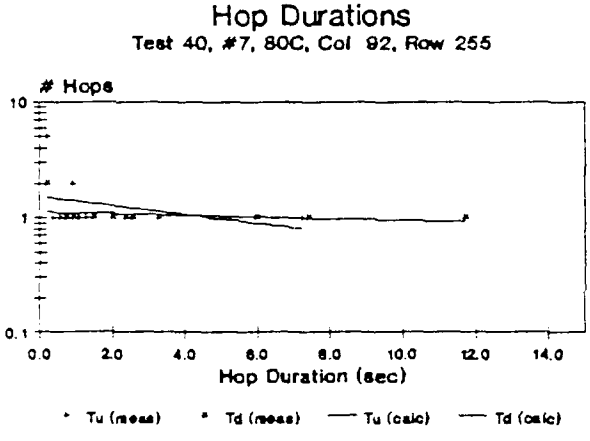


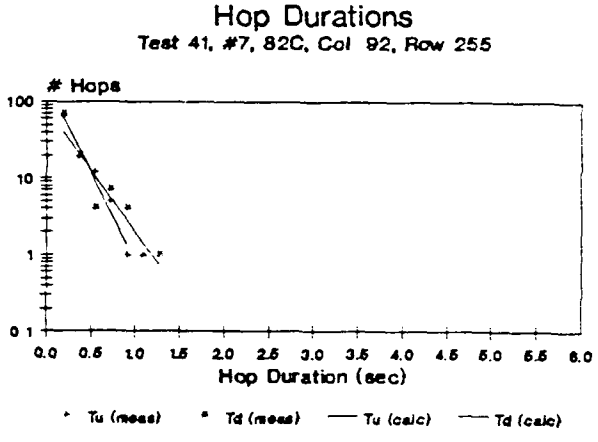


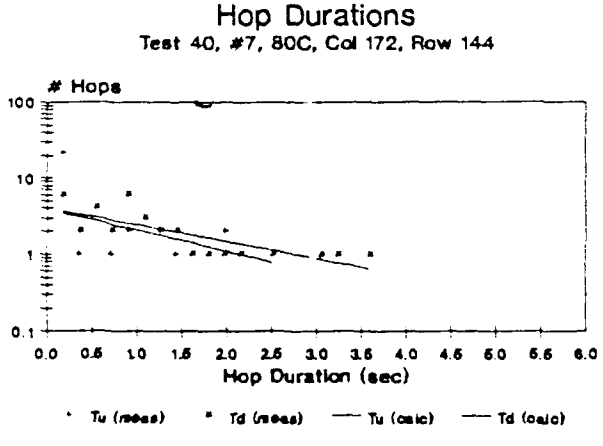
Figures 4.11-14a to 4.11-14f Tu and Td Duration Histograms
(DUT #7, selected bits 1-3, each at two temperatures)

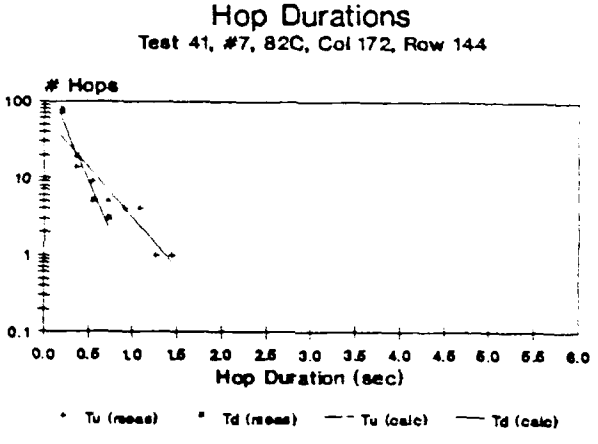




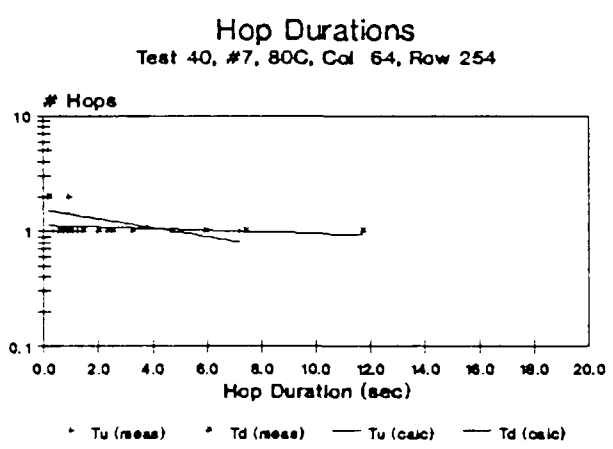


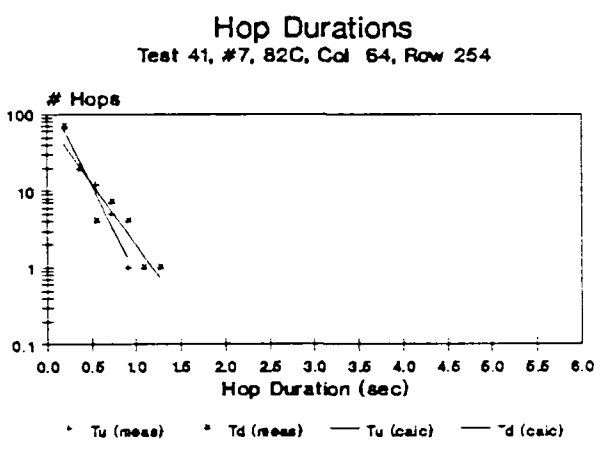


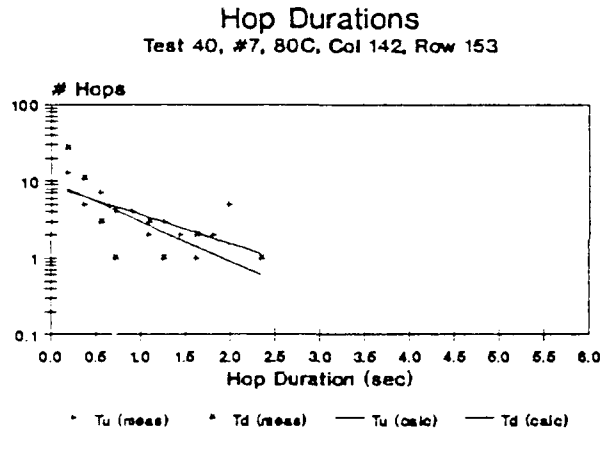


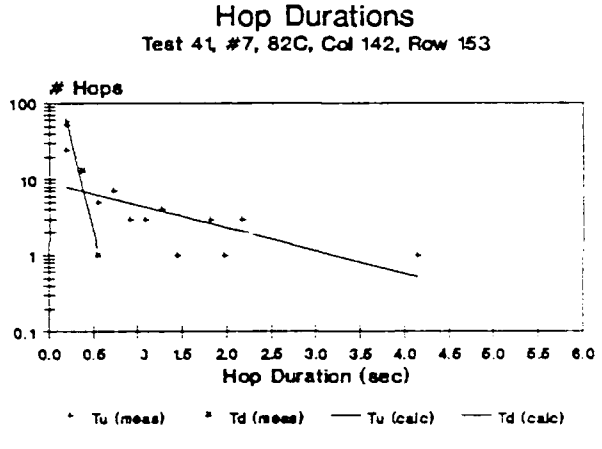


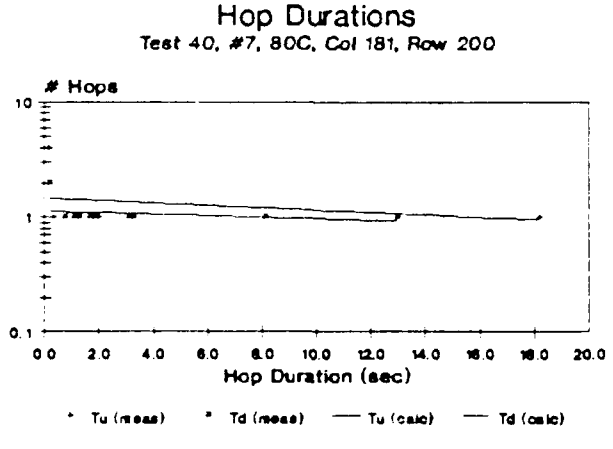
Figures 4.11-15a to 4.11-15f Tu and Td Duration Histograms
(DUT #7, selected bits 4-6, each at two temperatures)

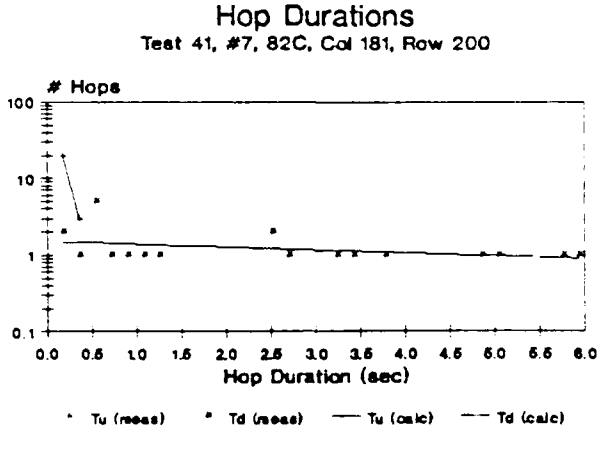












4.12 Test 90 and Test 91: DUT #127

The Tref, Tu and Td parameter extraction and activation energy calculations for DUT #127 are shown in this section, is the same format as the previous section. Table 4.12-1 shows a list of the Tref, Tu and Td parameter values and activation energies. Figure 4.12-1 shows that the distribution of hopper bit Tref averages is well behaved. Because there were few hops for several bits, some values of the Tu and Td became 180, and their Ea's became 0. There was a mixture of positive and negative Ea's for Tu and Td. It is possible that different traps were active in the cold and hot tests, and this could explain the negative activation energies. Scatter plots are shown in Figures 4.12-6 to 4.12-9 of these Ea's vs Tref Ea for the hopper bits.

Tref waveforms for the six selected individual bits at both temperatures are show in Figures 4.12-10 and 4.12-11. The hot test ended just after 74000 sec. The second bit shown actually did not hop before more than 60000 sec. In this device, the Tu and Td plots (Figures 4.14 and 4.15) show inadequate data to reliably extract the parameters and their activation energies in almost all cases. Of those shown, bit 3 is probably the best.

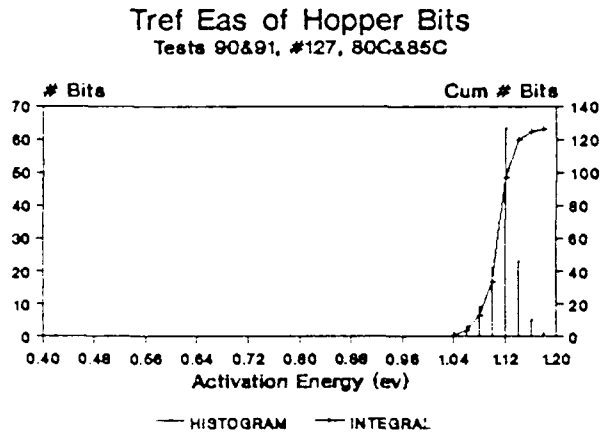
Table 4.12-1
Test 90/91 Hopper Bit Tref, Tu, Td Values and Activation Energies

Selected bit # col	row	#hc	#hh	Trc	Trh	EaTr	Tu c	Td c	Ea Tu	Td c	Td h	Ea Td	Ea Tu*Td	Ea Tu/Td
2	152	8	8	3.7	2.1	1.15	180.0	125.9	0.8	180.0	125.9	0.8	0.0	1.5
4	135	6	5	3.5	2.0	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
⑤ 6	152	7	10	3.7	2.1	1.14	180.0	180.0	0.0	180.0	125.9	0.8	-0.8	0.8
7	152	6	5	3.6	2.1	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
② 8	136	7	15	3.9	2.2	1.17	103.9	55.4	1.4	180.0	111.7	1.0	0.3	2.4
12	137	7	5	3.6	2.1	1.13	125.9	125.9	0.0	180.0	180.0	0.0	0.0	0.0
14	135	8	8	3.5	2.0	1.13	180.0	125.9	0.8	180.0	180.0	0.0	0.8	0.8
26	177	11	5	3.7	2.2	1.09	86.9	180.0	-1.6	180.0	180.0	0.0	-1.6	-1.6
28	135	6	7	3.5	2.0	1.13	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
28	195	12	6	3.8	2.2	1.12	180.0	180.0	0.0	128.4	128.4	0.0	0.0	0.0
38	135	9	8	3.5	2.0	1.13	180.0	125.9	0.8	180.0	180.0	0.0	0.8	0.8
39	135	6	7	3.5	2.0	1.13	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
40	152	8	6	3.6	2.1	1.11	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
41	135	8	5	3.5	2.0	1.12	82.5	180.0	-1.7	180.0	180.0	0.0	-1.7	-1.7
42	177	16	7	3.7	2.2	1.11	103.8	180.0	-1.2	68.9	180.0	-2.1	0.9	-3.2
③ 43	154	14	13	3.8	2.2	1.13	116.3	41.6	2.2	120.4	75.8	1.0	1.2	3.2
44	136	7	5	3.7	2.2	1.11	41.6	180.0	-3.1	75.8	180.0	-1.9	-1.3	-5.0
48	135	9	8	3.5	2.0	1.12	180.0	125.9	0.8	180.0	180.0	0.0	0.8	0.8
50	154	8	11	3.8	2.2	1.15	125.9	71.4	1.2	180.0	124.5	0.8	0.4	2.0
52	137	7	5	3.6	2.1	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
54	135	8	5	3.5	2.0	1.12	82.5	180.0	-1.7	180.0	180.0	0.0	-1.7	-1.7
55	154	8	10	3.8	2.2	1.14	103.9	103.9	0.0	180.0	103.9	1.2	-1.2	1.2
56	177	28	9	3.8	2.2	1.13	27.9	180.0	-4.0	38.6	180.0	-3.3	-0.7	-7.3
60	152	9	11	3.7	2.1	1.14	180.0	80.2	1.7	180.0	125.9	0.8	1.0	2.5
61	149	13	9	3.8	2.2	1.13	45.6	180.0	-3.0	180.0	180.0	0.0	-3.0	-3.0
62	152	9	8	3.7	2.1	1.13	180.0	180.0	0.0	180.0	125.9	0.8	-0.8	0.8
63	135	8	7	3.5	2.0	1.12	82.5	180.0	-1.7	180.0	180.0	0.0	-1.7	-1.7
64	167	10	9	3.8	2.2	1.13	103.9	103.9	0.0	180.0	180.0	0.0	0.0	0.0
65	182	20	9	3.8	2.2	1.14	50.1	180.0	-2.7	57.7	78.3	-0.7	-2.1	-3.4
66	167	5	13	3.7	2.2	1.11	180.0	34.6	3.5	180.0	71.4	2.0	1.6	5.5
66	177	5	5	3.7	2.2	1.09	125.9	180.0	-0.8	180.0	180.0	0.0	-0.8	-0.8
68	147	18	6	3.8	2.2	1.15	45.0	180.0	-3.0	86.3	129.8	-0.9	-2.1	-3.9
72	195	9	5	3.7	2.2	1.10	180.0	180.0	0.0	125.9	125.9	0.0	0.0	0.0
74	177	11	6	3.7	2.2	1.12	75.7	180.0	-1.9	142.9	180.0	-0.5	-1.4	-2.4
76	135	7	5	3.5	2.0	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
77	131	15	5	3.8	2.2	1.15	87.5	87.5	0.0	99.4	99.4	0.0	0.0	0.0
77	135	10	5	3.6	2.1	1.11	88.0	88.0	0.0	68.7	68.7	0.0	0.0	0.0
77	172	11	6	3.8	2.2	1.12	45.0	45.0	0.0	180.0	180.0	0.0	0.0	0.0
77	195	9	12	4.0	2.3	1.16	50.0	45.6	0.2	180.0	180.0	0.0	0.2	0.2
79	195	5	7	4.0	2.3	1.17	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
80	131	15	5	3.8	2.2	1.13	74.9	74.9	0.0	99.4	99.4	0.0	0.0	0.0
80	195	8	11	3.9	2.2	1.15	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
81	135	10	5	3.5	2.0	1.12	57.7	57.7	0.0	180.0	180.0	0.0	0.0	0.0
⑥ 82	177	17	10	3.8	2.2	1.12	91.0	53.1	1.2	113.0	180.0	-1.0	2.2	0.2
83	129	15	6	3.8	2.2	1.15	81.8	125.9	-0.9	180.0	180.0	0.0	-0.9	-0.9
85	149	11	7	3.8	2.2	1.13	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
86	135	11	6	3.5	2.0	1.12	82.5	82.5	0.0	180.0	180.0	0.0	0.0	0.0
87	177	7	5	3.7	2.2	1.08	125.9	180.0	-0.8	180.0	180.0	0.0	-0.8	-0.8
89	154	7	8	3.8	2.2	1.11	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
91	131	15	11	3.9	2.2	1.14	42.0	180.0	-3.1	90.0	180.0	-1.5	-1.6	-4.6
91	169	9	5	3.9	2.2	1.18	85.3	85.3	0.0	180.0	180.0	0.0	0.0	0.0
92	137	6	5	3.6	2.1	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
92	152	7	8	3.6	2.1	1.11	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
93	195	13	5	3.8	2.2	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
94	135	7	5	3.5	2.0	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
96	195	6	6	3.8	2.2	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
98	135	12	6	3.5	2.1	1.10	42.8	180.0	-3.1	180.0	180.0	0.0	-3.1	-3.1
99	152	5	6	3.6	2.1	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
102	149	13	7	3.8	2.2	1.11	86.2	180.0	-1.6	180.0	180.0	0.0	-1.6	-1.6
104	149	13	8	3.8	2.2	1.14	110.7	180.0	-1.0	180.0	180.0	0.0	-1.0	-1.0

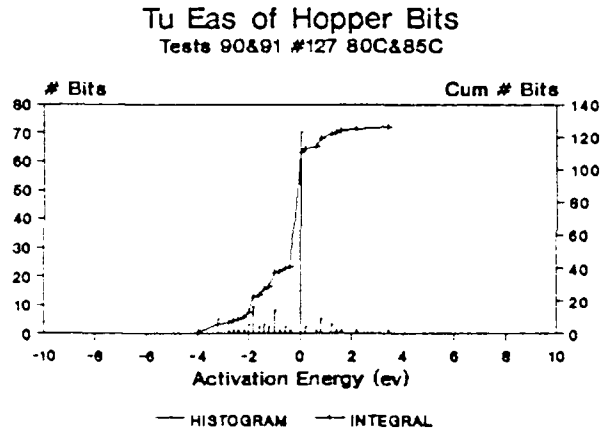
Table 4.12-1 (Continued)
Test 90/91 Hopper Bit Tref, Tu, Td Values and Activation Energies

105	137	5	5	3.6	2.1	1.11	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
107	177	9	7	3.7	2.2	1.08	88.7	180.0	-1.5	180.0	180.0	0.0	-1.5	-1.5
(9) 118	167	10	11	3.8	2.2	1.13	103.9	125.9	-0.4	180.0	180.0	0.0	-0.4	-0.4
119	131	11	6	3.8	2.2	1.14	91.0	91.0	0.0	180.0	180.0	0.0	0.0	0.0
119	135	12	5	3.5	2.0	1.12	52.3	52.3	0.0	180.0	180.0	0.0	0.0	0.0
124	129	13	5	3.7	2.2	1.14	88.0	125.9	-0.8	75.2	180.0	-1.9	1.1	-2.6
126	177	15	6	3.7	2.2	1.14	103.8	180.0	-1.2	123.9	180.0	-0.8	-0.4	-2.0
130	177	6	5	3.7	2.2	1.11	125.9	125.9	0.0	180.0	180.0	0.0	0.0	0.0
131	135	6	5	3.5	2.0	1.12	125.9	180.0	-0.8	180.0	180.0	0.0	-0.8	-0.8
132	154	7	12	3.8	2.2	1.13	180.0	180.0	0.0	180.0	80.2	1.7	-1.7	1.7
135	149	16	10	3.8	2.2	1.13	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
139	152	8	7	3.6	2.1	1.10	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
141	135	6	6	3.5	2.0	1.13	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
141	195	12	8	3.8	2.2	1.11	180.0	180.0	0.0	75.7	180.0	-1.9	1.9	-1.9
144	149	7	5	3.7	2.2	1.09	125.9	125.9	0.0	180.0	180.0	0.0	0.0	0.0
145	137	8	5	3.6	2.1	1.11	125.9	125.9	0.0	180.0	180.0	0.0	0.0	0.0
148	147	6	8	3.8	2.2	1.12	180.0	180.0	0.0	180.0	125.9	0.8	-0.8	0.8
148	195	6	6	3.7	2.2	1.08	180.0	180.0	0.0	125.9	180.0	-0.8	0.8	-0.8
150	149	8	9	3.8	2.2	1.13	75.7	180.0	-1.9	180.0	180.0	0.0	-1.9	-1.9
(1) 150	177	32	8	3.8	2.2	1.13	65.8	180.0	-2.2	45.4	180.0	-3.0	0.8	-5.1
151	135	11	7	3.5	2.0	1.12	82.5	125.9	-0.9	180.0	180.0	0.0	-0.9	-0.9
151	154	9	10	3.8	2.2	1.15	125.9	71.4	1.2	180.0	124.5	0.8	0.4	2.0
(8) 152	131	18	10	3.9	2.2	1.14	57.1	180.0	-2.5	60.0	180.0	-2.4	-0.1	-4.8
152	135	8	5	3.5	2.0	1.12	82.5	180.0	-1.7	180.0	180.0	0.0	-1.7	-1.7
153	131	15	5	3.8	2.2	1.14	74.9	74.9	0.0	103.9	103.9	0.0	0.0	0.0
153	137	9	6	3.6	2.1	1.11	125.9	180.0	-0.8	180.0	180.0	0.0	-0.8	-0.8
154	135	5	5	3.5	2.0	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
161	135	6	5	3.5	2.0	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
162	135	11	5	3.5	2.1	1.10	57.7	57.7	0.0	180.0	180.0	0.0	0.0	0.0
166	135	9	5	3.5	2.0	1.13	82.5	82.5	0.0	180.0	180.0	0.0	0.0	0.0
168	195	5	5	3.9	2.2	1.15	82.5	180.0	-1.7	180.0	180.0	0.0	-1.7	-1.7
175	135	6	5	3.5	2.0	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
175	177	10	6	3.7	2.2	1.09	88.4	180.0	-1.5	180.0	180.0	0.0	-1.5	-1.5
177	228	6	5	3.3	2.0	1.08	125.9	125.9	0.0	180.0	180.0	0.0	0.0	0.0
180	135	8	5	3.5	2.0	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
180	177	18	7	3.8	2.2	1.12	76.2	180.0	-1.8	121.2	180.0	-0.9	-1.0	-2.7
182	228	6	5	3.3	2.0	1.08	125.9	125.9	0.0	180.0	180.0	0.0	0.0	0.0
183	177	26	8	3.8	2.2	1.15	86.3	78.3	0.2	43.1	180.0	-3.1	3.3	-2.9
186	228	5	5	3.3	2.0	1.07	78.3	78.3	0.0	180.0	180.0	0.0	0.0	0.0
194	135	6	5	3.5	2.0	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
194	137	7	5	3.6	2.1	1.13	125.9	125.9	0.0	180.0	180.0	0.0	0.0	0.0
194	177	29	11	3.8	2.2	1.15	67.2	83.0	-0.6	30.3	180.0	-3.8	3.2	-4.4
195	177	13	8	3.7	2.2	1.11	85.7	180.0	-1.6	73.8	180.0	-1.9	0.3	-3.5
195	248	10	6	3.2	1.9	1.06	88.0	88.0	0.0	180.0	180.0	0.0	0.0	0.0
208	195	8	5	3.7	2.2	1.12	180.0	180.0	0.0	125.9	125.9	0.0	0.0	0.0
212	152	7	6	3.6	2.1	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
215	248	8	7	3.2	1.9	1.11	180.0	180.0	0.0	180.0	86.4	1.6	-1.6	1.6
216	195	8	7	3.8	2.2	1.12	125.9	180.0	-0.8	180.0	180.0	0.0	-0.8	-0.8
217	137	8	5	3.6	2.1	1.11	125.9	125.9	0.0	180.0	180.0	0.0	0.0	0.0
217	248	8	5	3.2	1.9	1.05	103.9	103.9	0.0	180.0	180.0	0.0	0.0	0.0
221	167	10	9	3.8	2.2	1.13	103.9	180.0	-1.2	180.0	180.0	0.0	-1.2	-1.2
222	154	11	9	3.8	2.2	1.16	180.0	180.0	0.0	96.6	180.0	-1.3	1.3	-1.3
(4) 226	136	10	17	3.9	2.2	1.16	125.9	138.0	-0.2	180.0	112.0	1.0	-1.2	0.8
226	152	5	7	3.6	2.1	1.13	180.0	180.0	0.0	180.0	125.9	0.8	-0.8	0.8
228	172	7	5	3.7	2.2	1.10	83.3	180.0	-1.7	180.0	180.0	0.0	-1.7	-1.7
229	135	6	8	3.5	2.0	1.12	180.0	125.9	0.8	180.0	180.0	0.0	0.8	0.8
230	167	8	8	3.6	2.2	1.14	85.3	63.6	0.6	180.0	180.0	0.0	0.6	0.6
231	167	8	8	3.8	2.2	1.13	103.9	125.9	-0.4	180.0	180.0	0.0	-0.4	-0.4
232	135	7	6	3.5	2.0	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
235	195	19	7	3.8	2.2	1.12	110.7	180.0	-1.0	93.5	180.0	-1.4	0.4	-2.5
236	149	7	8	3.8	2.2	1.12	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
239	149	8	5	3.7	2.1	1.15	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
240	195	7	10	3.9	2.2	1.15	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
248	177	20	8	3.8	2.2	1.12	66.3	180.0	-2.1	92.2	180.0	-1.4	-0.7	-3.6
249	147	8	10	3.8	2.2	1.13	180.0	180.0	0.0	180.0	71.4	2.0	-2.0	2.0
251	228	6	5	3.3	2.0	1.07	125.9	125.9	0.0	180.0	180.0	0.0	0.0	0.0

Figures 4.12-1 to 4.12-5 Tref, Tu, and Td Parameter Activation Energies (DUT #127, All Hopper Bits with >=5 hops)



>=5 HOPS



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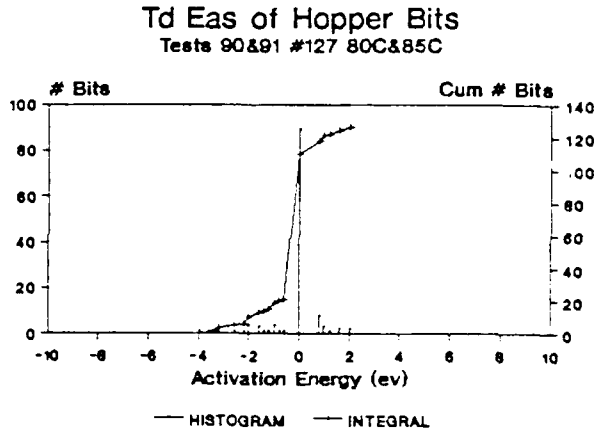

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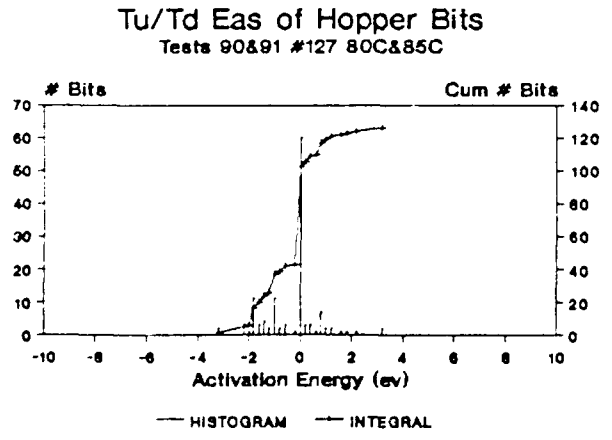
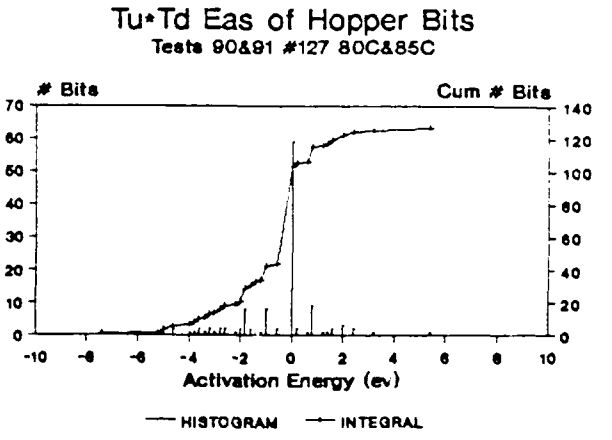
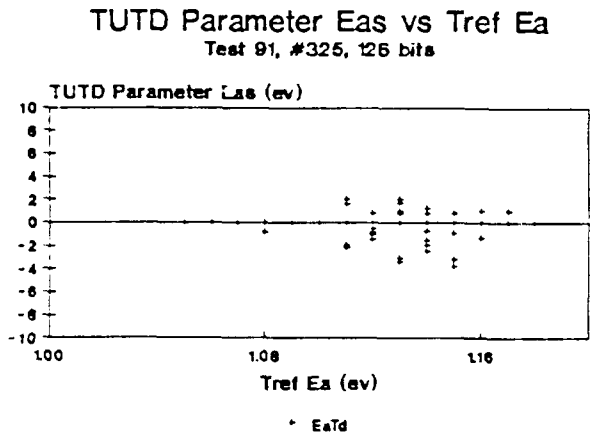


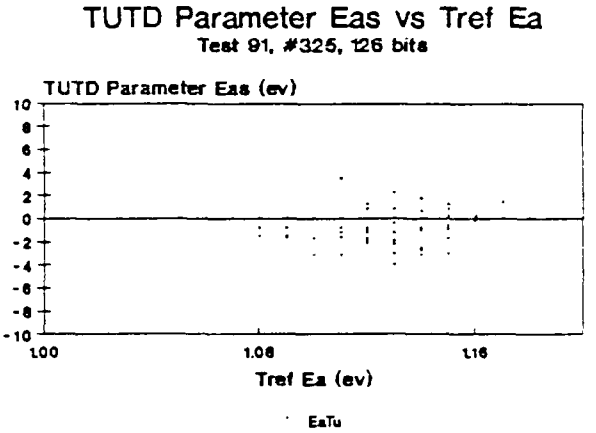
>=5 HOPS

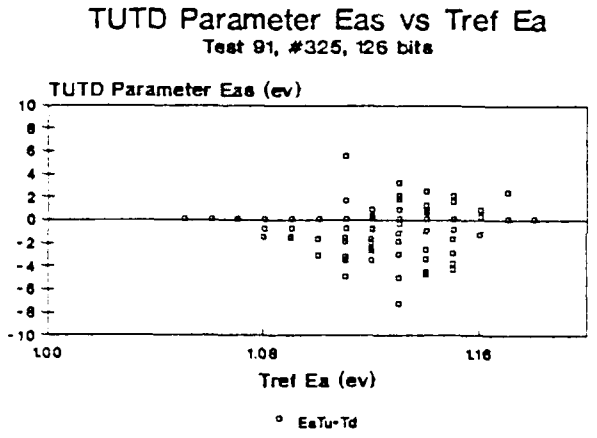


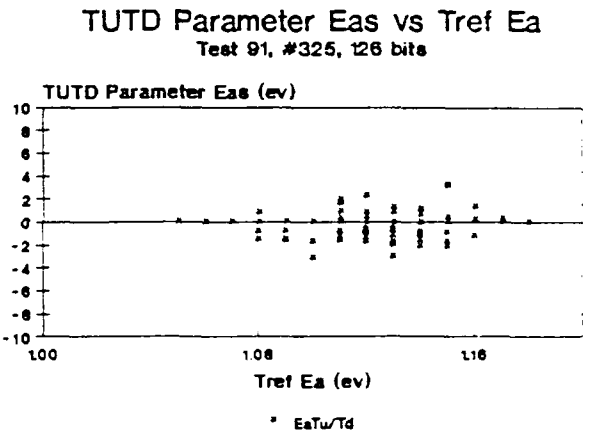
>=5 HOPS

Figures 4.12-6 to 4.12-9 Tu, Td, Tu/Td and Tu*Td Ea's vs Tref Ea's
(DUT #127, All Hopper Bits with >=5 hops)

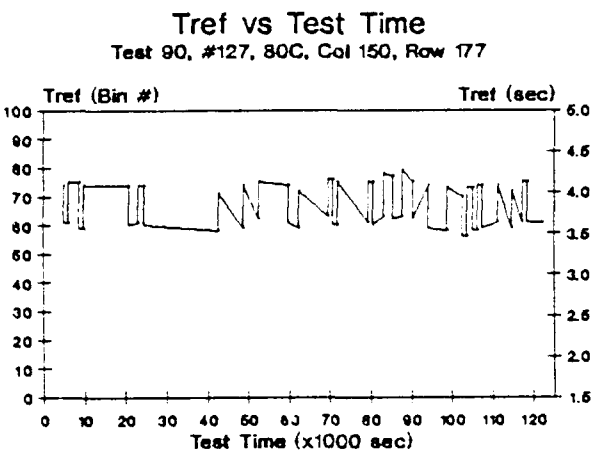


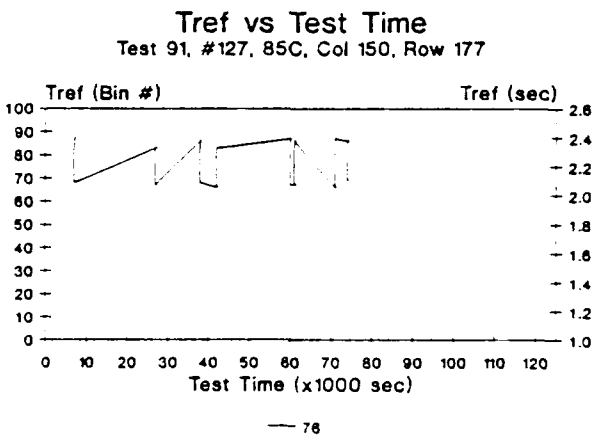


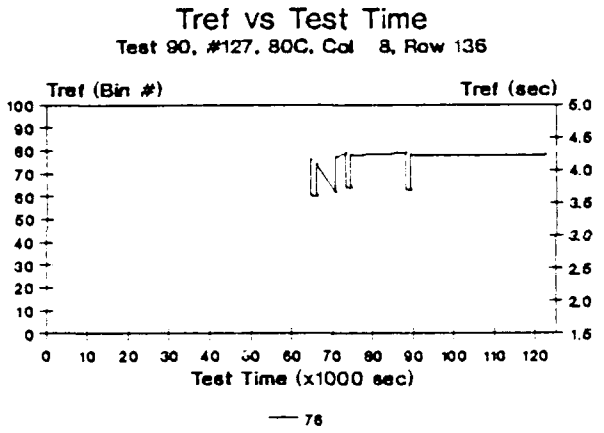


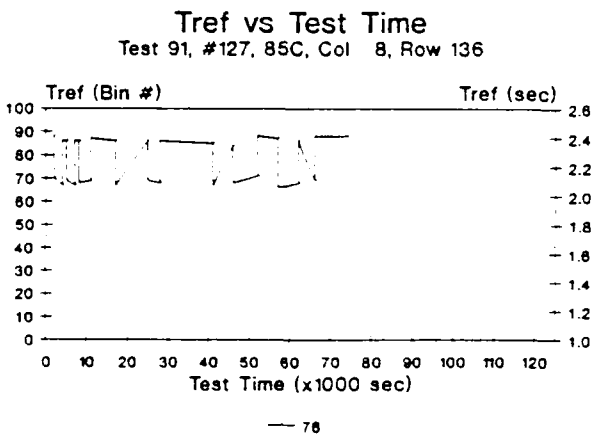


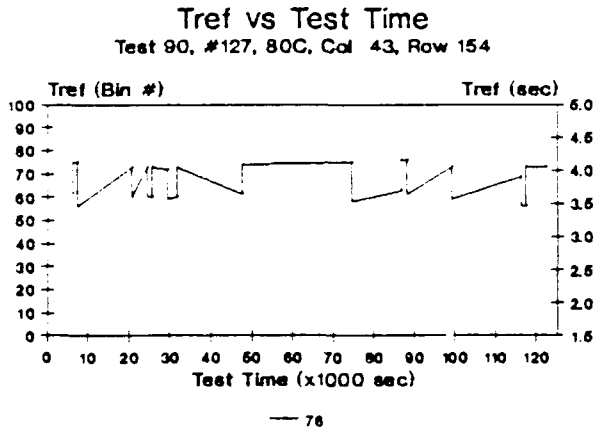
Figures 4.12-10a to 4.12-10f Tref vs Test Time Waveforms
(DUT #127, selected bits 1-3, each at two temperatures)

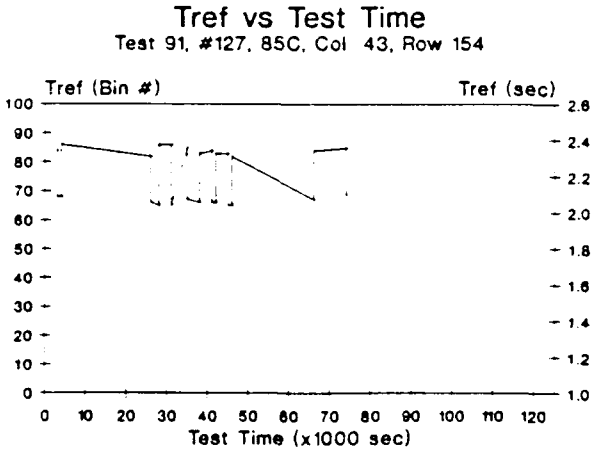




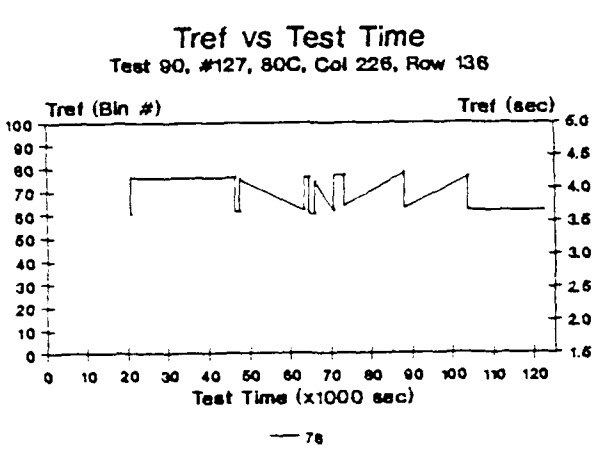


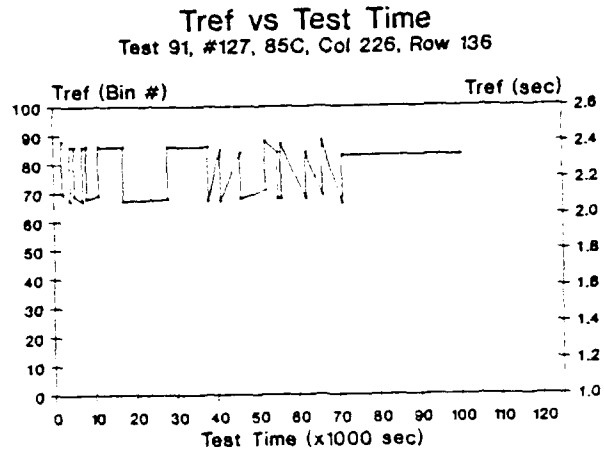


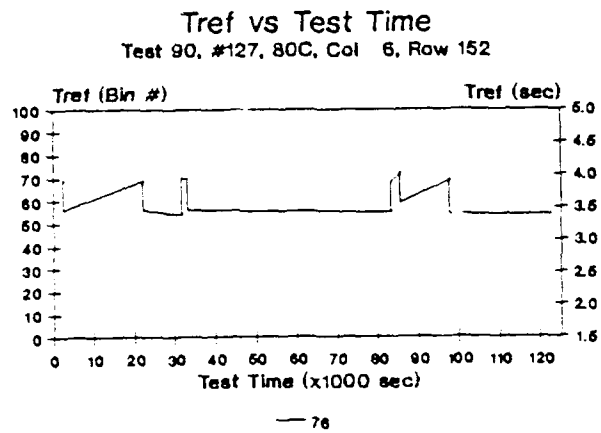


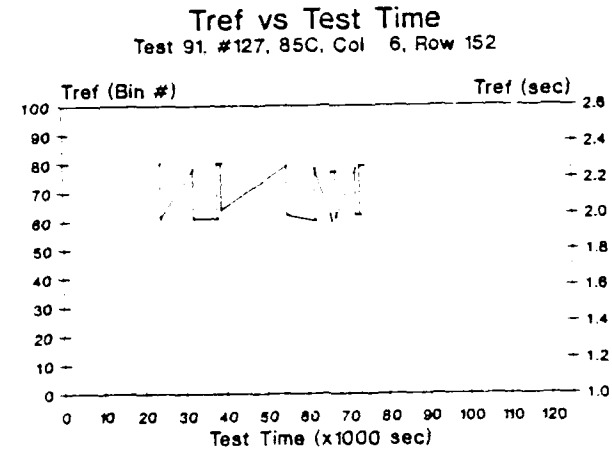


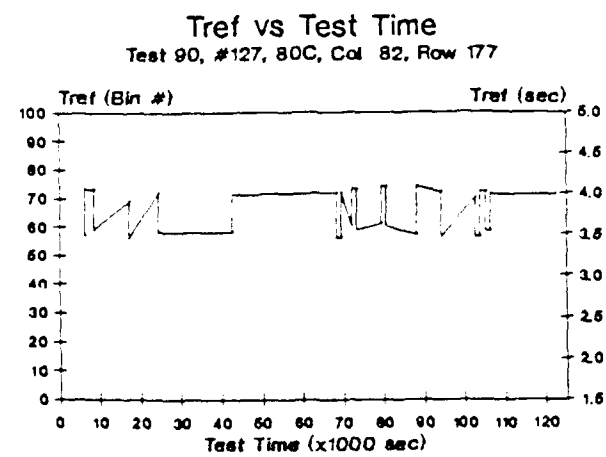
Figures 4.12-11a to 4.12-11f Tref vs Test Time Waveforms
(DUT #127, selected bits 4-6, each at two temperatures)

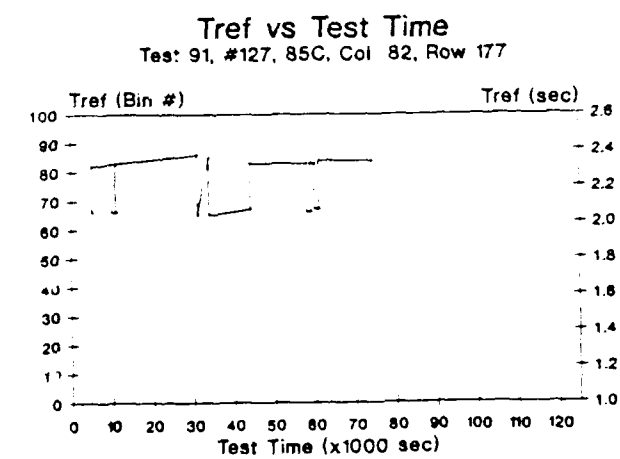




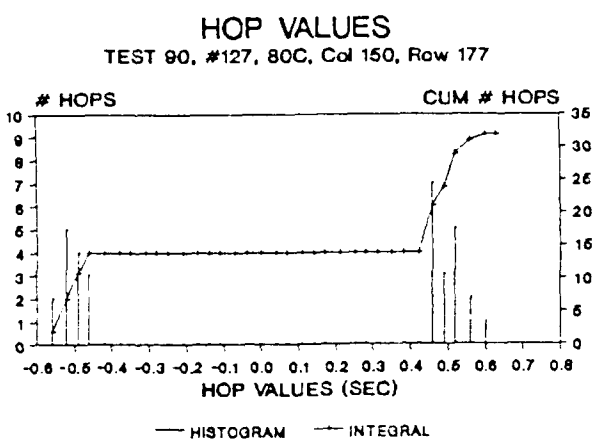


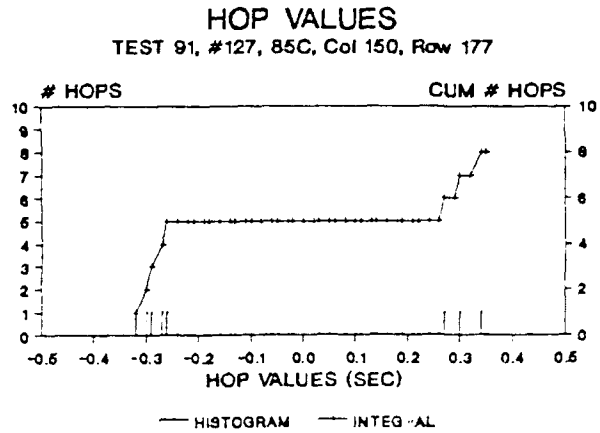


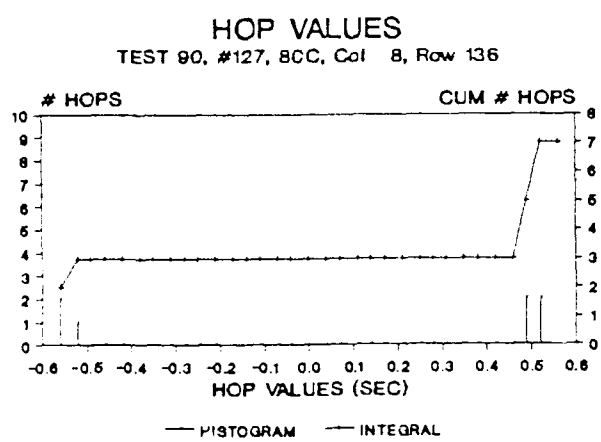


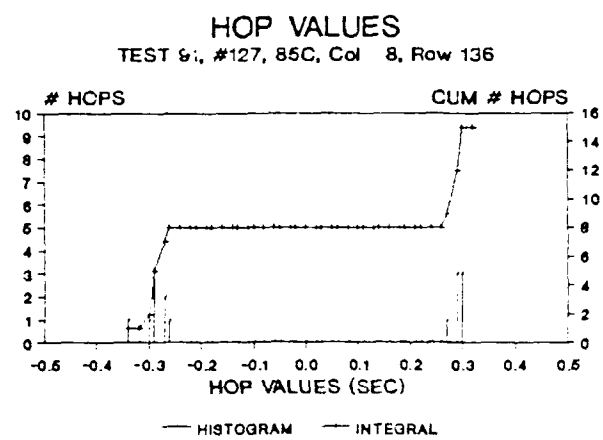


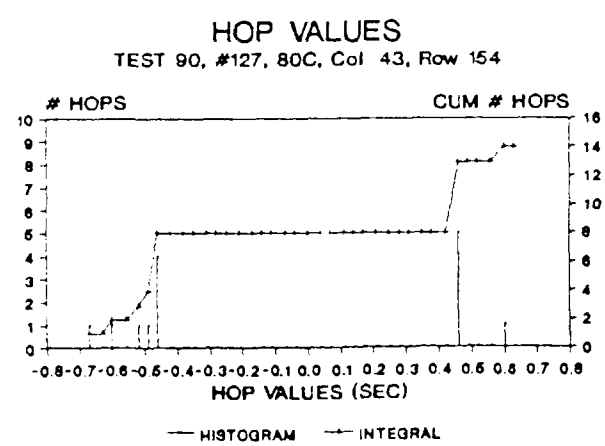
Figures 4.12-12a to 4.12-12f Hop Value Histograms
(DUT #127, selected bits 1-3, each at two temperatures)

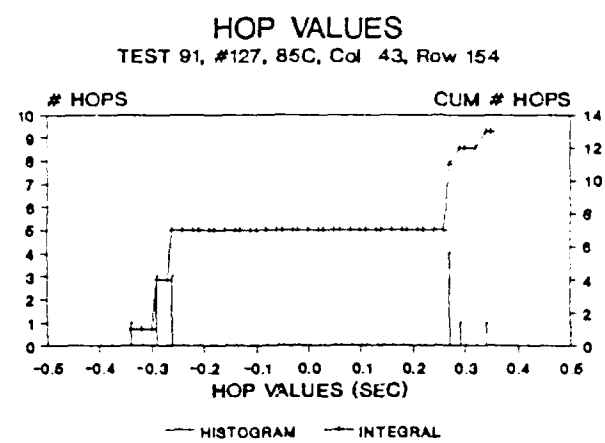




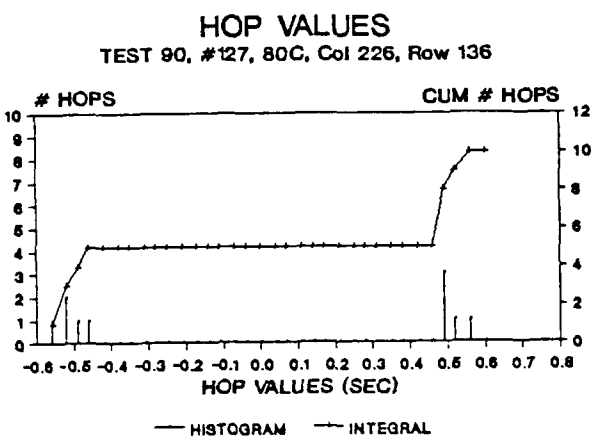


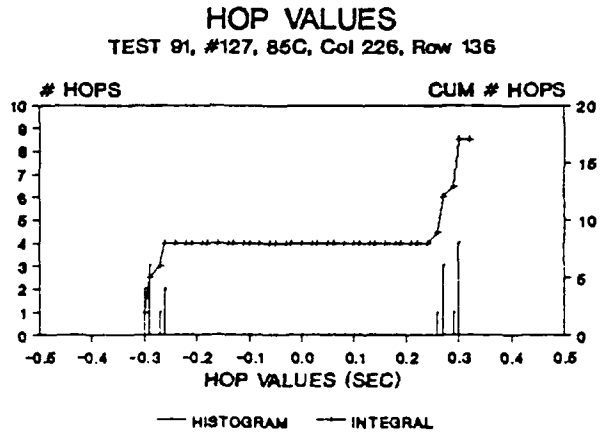


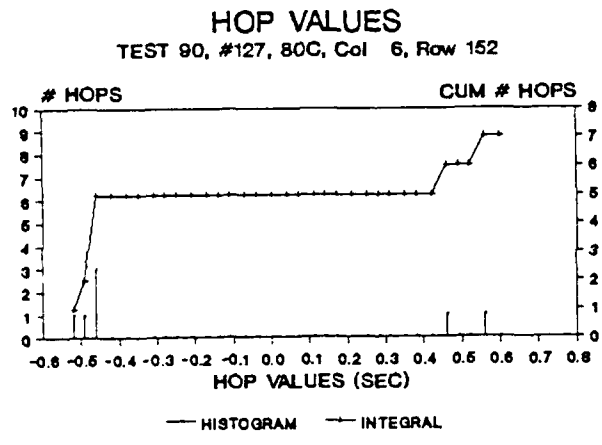


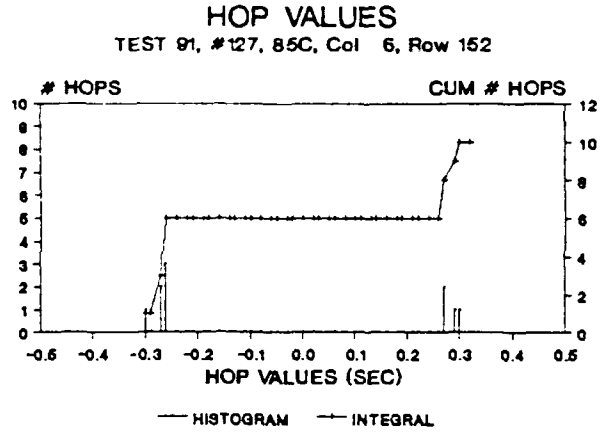


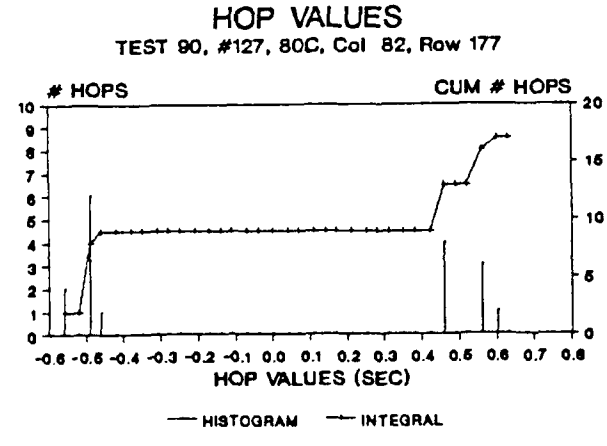
Figures 4.12-13a to 4.12-13f Hop Value Histograms
(DUT #127, selected bits 4-6, each at two temperatures)

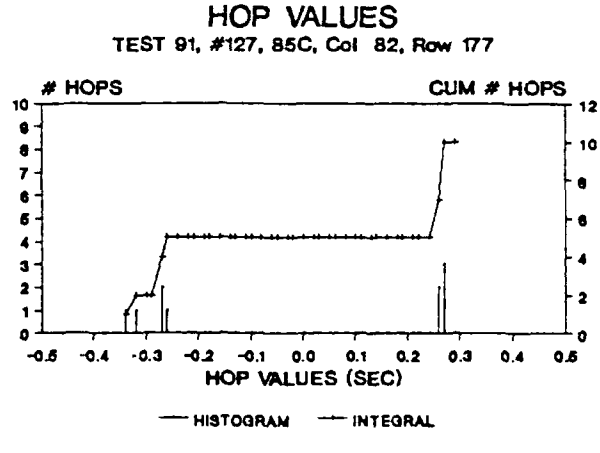




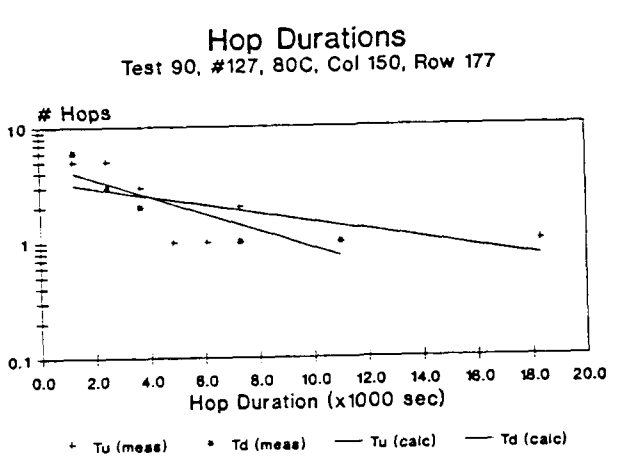


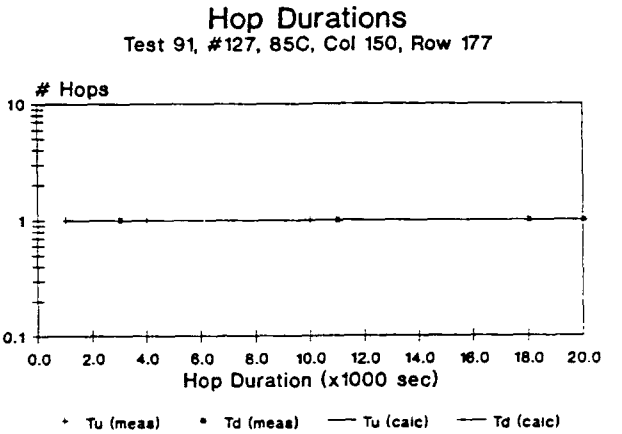


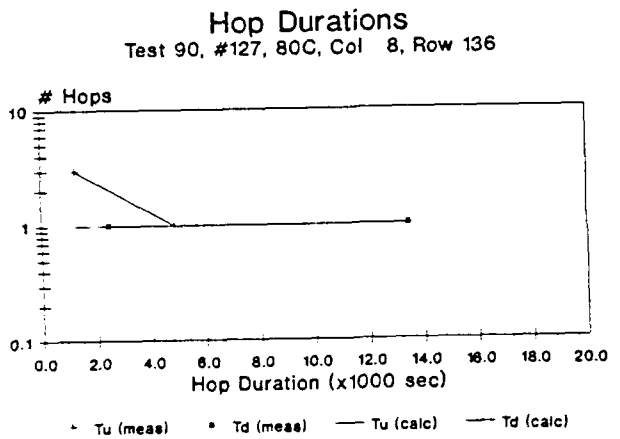


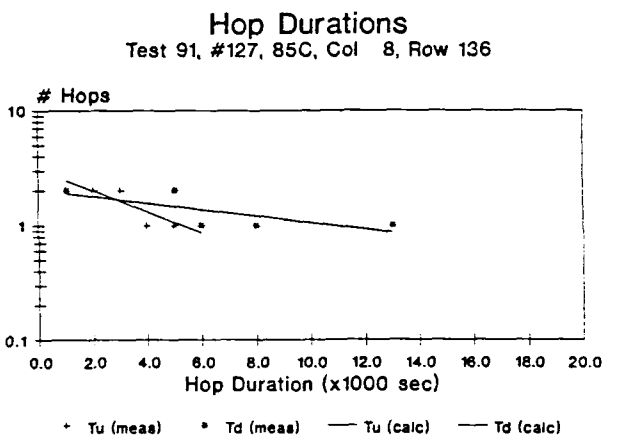


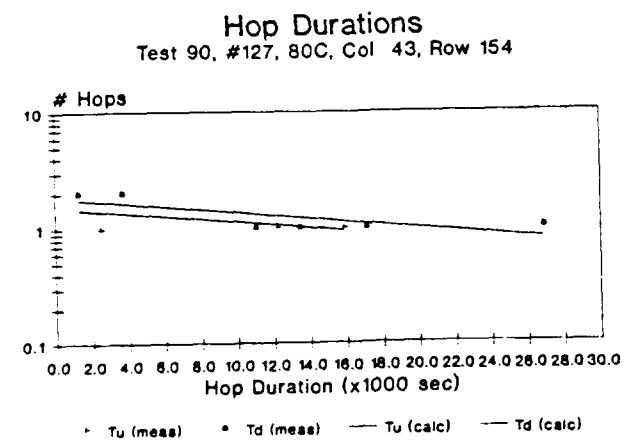
Figures 4.12-14a to 4.12-14f Tu and Td Duration Histograms
(DUT #127, selected bits 1-3, each at two temperatures)

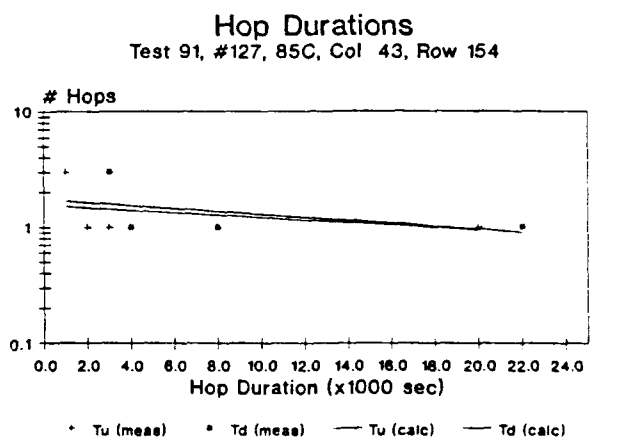




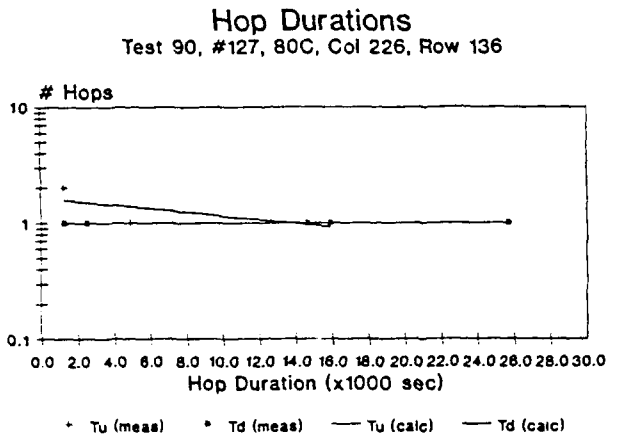


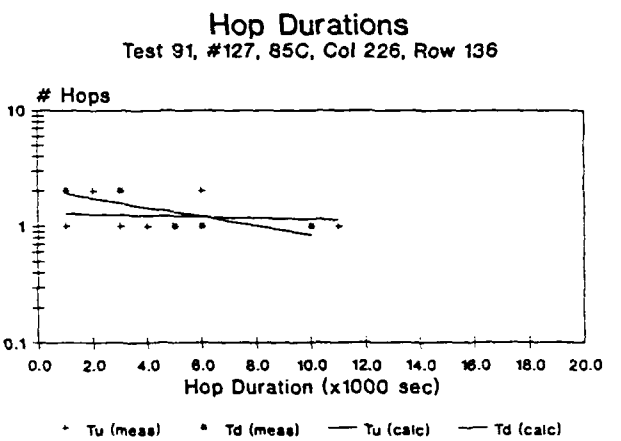


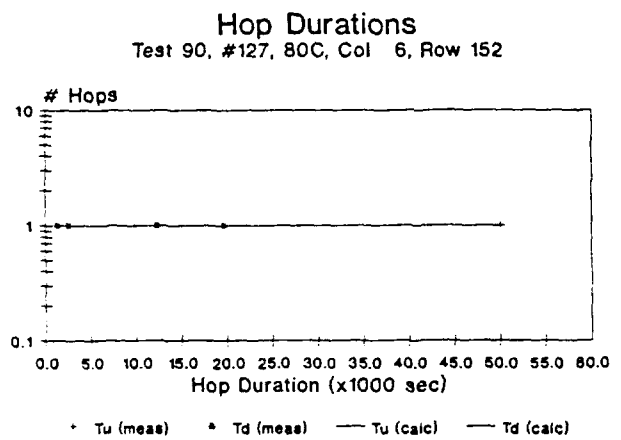


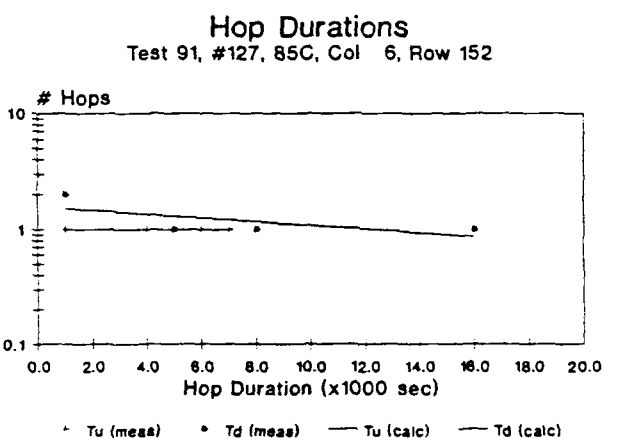


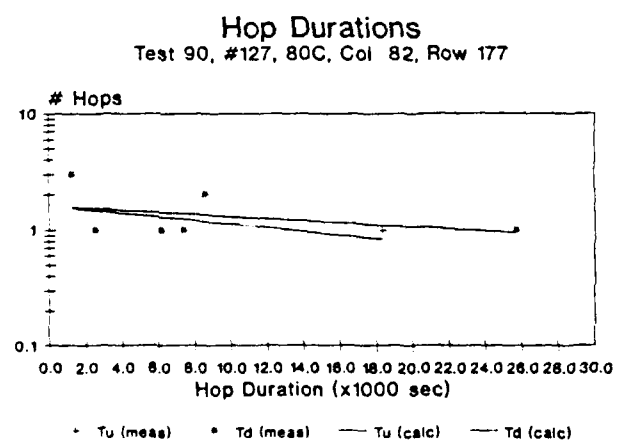
Figures 4.12-15a to 4.12-15f Tu and Td Duration Histograms
(DUT #127, selected bits 4-6, each at two temperatures)

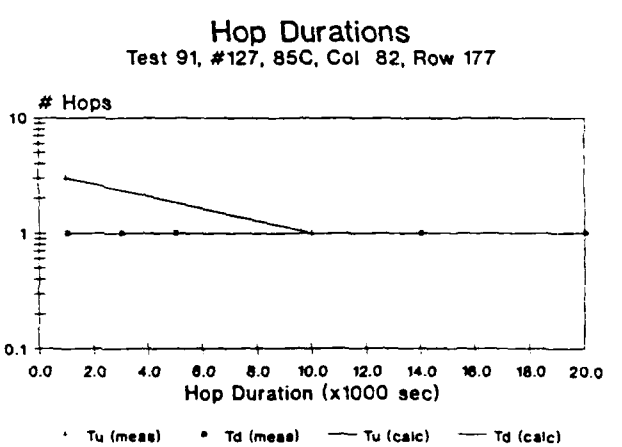












4.13 Test 96 and Test 97: DUT #457

The results for this device are shown in Table 4.13-1 and Figures 4.13-1 to 4.13-15. This device also had a mix of positive and negative Ea's for the Tu and Td parameters. Again, this may be due to different traps being active at the two temperatures.

Most of the six bits selected and shown in Figure 4.13 appear to only have one trap active, and exhibited several hops at each duration. Therefore, the Tu and Td parameters and the Ea's are probably more reliable.

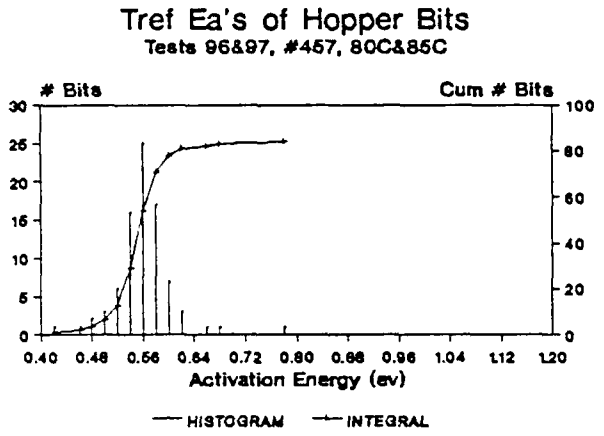
Table 4.13-1
Test 96/97 Hopper Bit Tref, Tu, Td Values and Activation Energies

Selected ↓col	row	bit #hc	# #hh	Trc	Trh	EaTr	Tu c	Td c	Ea Tu	Td c	Td h	Ea Td	Ea Tu*Td	Ea Tu/Td
6	45	12	15	10.3	7.7	0.57	132.9	90.0	0.8	136.8	183.6	-0.6	1.5	0.2
6	78	10	18	9.1	6.9	0.55	78.7	3.7	6.6	180.0	94.7	1.4	5.2	8.0
12	16	17	15	11.6	8.6	0.59	131.0	187.3	-0.8	59.7	14.4	3.1	-3.8	2.3
16	173	6	14	10.9	8.3	0.56	180.0	55.4	2.5	180.0	55.7	2.5	0.0	5.1
17	198	10	8	10.3	7.8	0.57	180.0	180.0	0.0	79.6	90.0	-0.3	0.3	-0.3
20	180	8	5	11.8	9.0	0.55	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
21	110	21	12	13.5	9.9	0.63	85.1	129.9	-0.9	109.2	112.7	-0.1	-0.8	-1.0
25	116	6	10	11.6	8.6	0.59	180.0	180.0	0.0	103.9	79.6	0.6	-0.6	0.6
(3) 29	194	30	32	8.6	6.6	0.50	90.0	32.1	2.2	19.4	9.5	1.5	0.7	3.8
34	47	6	11	12.3	9.0	0.62	180.0	180.0	0.0	180.0	103.9	1.2	-1.2	1.2
34	216	19	16	9.3	7.5	0.43	60.0	59.7	0.0	120.8	122.1	0.0	0.0	0.0
35	232	8	7	11.2	8.4	0.56	88.0	103.9	-0.4	180.0	180.0	0.0	-0.4	-0.4
36	237	13	16	9.1	7.0	0.53	86.9	171.7	-1.5	27.5	25.5	0.2	-1.6	-1.3
37	184	5	5	9.2	6.8	0.59	180.0	125.9	0.8	125.9	180.0	-0.8	1.5	0.0
38	57	5	6	10.4	7.8	0.57	180.0	45.0	3.0	180.0	180.0	0.0	3.0	3.0
44	62	12	6	8.7	6.6	0.56	70.5	103.9	-0.8	38.8	180.0	-3.3	2.5	-4.1
(5) 46	127	35	22	10.6	7.9	0.58	4.3	9.6	-1.7	60.3	71.1	-0.4	-1.4	-2.1
48	160	13	6	11.2	8.6	0.52	180.0	45.0	3.0	98.5	180.0	-1.3	4.3	1.7
53	92	5	9	10.1	7.6	0.55	45.0	180.0	-3.0	180.0	20.0	4.7	-7.7	1.7
55	55	34	11	10.2	7.6	0.60	28.3	180.0	-4.0	29.8	103.9	-2.7	-1.3	-6.7
56	79	13	6	13.5	9.2	0.78	26.1	125.9	-3.4	180.0	180.0	0.0	-3.4	-3.4
56	111	10	21	12.7	9.5	0.57	20.0	39.5	-1.5	180.0	82.9	1.7	-3.1	0.2
56	141	15	17	8.7	6.6	0.54	134.3	165.1	-0.4	14.4	59.7	-3.1	2.6	-3.5
63	195	8	7	9.6	7.2	0.57	72.5	180.0	-2.0	180.0	180.0	0.0	-2.0	-2.0
67	38	12	12	9.2	7.0	0.55	180.0	180.0	0.0	180.0	70.5	2.0	-2.0	2.0
68	56	10	9	12.4	9.2	0.60	208.4	83.4	2.0	180.0	180.0	0.0	2.0	2.0
69	218	9	5	9.7	7.3	0.57	88.0	125.9	-0.8	605.4	180.0	2.6	-3.4	1.8
72	67	37	9	11.1	8.0	0.66	5.9	45.6	-4.4	60.6	73.8	-0.4	-4.0	-4.8
72	247	9	6	7.8	6.1	0.48	103.9	103.9	0.0	180.0	180.0	0.0	0.0	0.0
73	160	28	12	12.8	9.5	0.58	66.2	11.2	3.8	13.3	111.7	-4.6	8.4	-0.8
73	227	10	10	8.7	6.7	0.51	57.4	103.9	-1.3	180.0	180.0	0.0	-1.3	-1.3
74	154	31	12	11.0	8.1	0.62	74.0	180.0	-1.9	5.3	22.5	-3.1	1.2	-5.0
76	106	12	7	10.8	8.0	0.60	180.0	180.0	0.0	88.0	103.9	-0.4	0.4	-0.4
(7) 79	132	58	26	11.2	8.5	0.56	15.2	6.7	1.8	1.9	78.4	-8.0	9.7	-6.2
(4) 82	246	45	20	10.3	7.8	0.55	27.9	17.9	1.0	16.3	116.3	-4.2	5.2	-3.3
86	253	15	5	10.3	7.8	0.56	180.0	125.9	0.8	180.0	180.0	0.0	0.8	0.8
87	44	6	26	10.2	7.7	0.55	125.9	1.2	9.9	180.0	71.7	2.0	7.9	11.9
88	78	7	11	9.8	7.4	0.56	180.0	126.5	0.8	28.3	180.0	-4.0	4.7	-3.2
88	178	6	8	9.4	7.0	0.57	180.0	103.9	1.2	180.0	180.0	0.0	1.2	1.2
88	232	6	9	7.7	5.9	0.54	103.9	88.0	0.4	180.0	180.0	0.0	0.4	0.4
94	71	12	7	9.3	7.2	0.50	41.8	103.9	-2.0	180.0	125.9	0.8	-2.7	-1.2
95	9	24	10	10.5	7.9	0.57	1.5	79.6	-8.5	125.5	180.0	-0.8	-7.8	-9.3
95	191	8	6	12.0	8.6	0.68	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
98	13	31	16	10.7	8.1	0.56	44.2	21.6	1.5	74.5	155.5	-1.6	3.1	0.0
110	210	19	10	11.1	8.8	0.46	134.8	180.0	-0.6	110.0	142.9	-0.6	-0.1	-1.2
113	63	19	14	9.6	7.2	0.57	10.0	14.4	-0.8	106.3	184.7	-1.2	0.4	-2.0
(6) 114	21	43	26	12.5	9.4	0.57	18.4	29.2	-1.0	43.6	25.8	1.1	-2.1	0.1
115	20	10	6	10.2	7.8	0.54	41.6	103.9	-2.0	180.0	180.0	0.0	-2.0	-2.0
(8) 118	165	38	23	8.4	6.4	0.53	16.8	31.2	-1.3	23.7	39.9	-1.1	-0.2	-2.5
120	192	12	9	9.2	6.9	0.58	85.9	180.0	-1.6	45.6	103.9	-1.8	0.3	-3.4
120	228	27	16	10.4	7.9	0.55	12.9	9.7	0.6	52.1	101.7	-1.4	2.0	-0.8
122	4	5	7	10.4	7.9	0.55	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
129	45	10	5	8.9	6.7	0.57	71.4	180.0	-2.0	180.0	180.0	0.0	-2.0	-2.0
133	95	27	20	9.4	7.0	0.58	40.8	20.8	1.4	119.1	84.9	0.7	0.7	2.2
(2) 135	105	49	24	11.9	8.9	0.59	21.6	25.7	-0.4	43.9	35.9	0.4	-0.8	0.1
137	47	39	19	11.0	8.3	0.58	32.9	77.1	-1.8	19.5	68.3	-2.7	0.9	-4.5
137	235	16	7	9.3	7.1	0.54	56.7	360.0	-4.0	119.9	180.0	-0.9	-3.1	-4.8
140	27	12	18	9.8	7.3	0.60	180.0	57.3	2.5	180.0	141.9	0.5	1.9	3.0
143	221	28	23	9.8	7.5	0.53	116.3	82.8	0.7	50.8	25.2	1.5	-0.8	2.2
145	172	7	5	10.4	7.8	0.58	82.8	180.0	-1.7	25.2	180.0	-4.2	2.6	-5.9

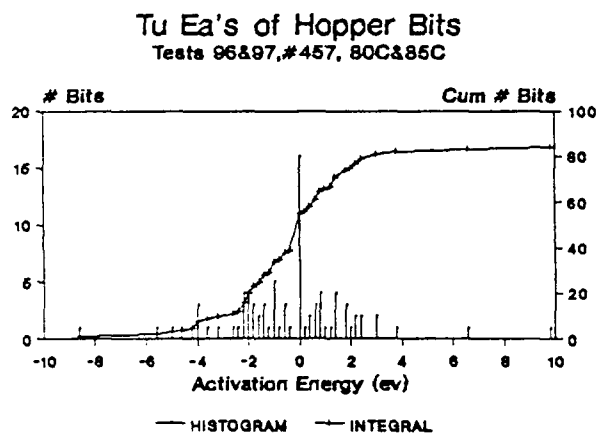
Table 4.13-1 (Continued)
Test 96/97 Hopper Bit Tref, Tu, Td Values and Activation Energies

153	55	35	18	9.6	7.1	0.61	45.0	142.9	-2.5	12.2	25.5	-1.6	-0.9	-4.1
153	184	22	13	9.5	7.2	0.55	54.0	22.5	1.9	110.5	147.2	-0.6	2.5	1.3
153	236	14	8	10.0	7.6	0.54	12.2	88.0	-4.2	180.0	180.0	0.0	-4.2	-4.2
154	158	5	5	9.3	7.1	0.52	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
167	160	12	10	10.1	7.5	0.59	7.2	90.0	-5.4	180.0	180.0	0.0	-5.4	-5.4
167	199	9	9	11.5	8.6	0.57	71.4	63.6	0.2	180.0	180.0	0.0	0.2	0.2
169	48	8	14	12.7	9.5	0.57	63.6	68.9	-0.2	180.0	153.9	0.3	-0.5	0.2
181	55	8	8	9.3	6.9	0.59	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
182	50	40	22	9.0	6.8	0.54	30.8	56.7	-1.3	20.9	55.4	-2.1	0.8	-3.4
207	165	13	13	9.1	6.9	0.55	53.3	41.6	0.5	130.7	54.8	1.9	-1.3	2.4
229	7	7	5	11.4	8.5	0.58	180.0	180.0	0.0	180.0	180.0	0.0	0.0	0.0
229	152	10	6	8.5	6.4	0.57	184.5	180.0	0.1	215.3	180.0	0.4	-0.3	0.4
230	237	17	12	9.1	6.7	0.60	28.3	79.6	-2.2	180.0	180.0	0.0	-2.2	-2.2
231	16	7	8	13.1	9.8	0.57	180.0	90.0	1.5	180.0	180.0	0.0	1.5	1.5
231	22	25	26	9.6	7.3	0.56	77.6	26.2	2.3	43.4	18.0	1.9	0.4	4.2
231	68	49	13	11.3	8.4	0.58	11.6	70.5	-3.9	11.5	180.0	-5.9	2.0	-9.8
231	100	17	22	13.2	9.7	0.61	128.5	91.4	0.7	59.7	11.0	3.6	-2.9	4.4
233	72	12	9	13.2	9.8	0.59	180.0	180.0	0.0	79.6	20.0	3.0	-3.0	3.0
236	47	5	6	12.0	9.0	0.58	180.0	180.0	0.0	129.8	103.9	0.5	-0.5	0.5
240	4	35	15	11.3	8.5	0.58	58.7	133.8	-1.8	4.1	5.0	-0.4	-1.4	-2.2
240	247	43	19	9.5	7.4	0.49	17.6	42.4	-1.9	16.7	107.3	-4.0	2.1	-5.9
245	214	12	12	10.3	7.8	0.56	180.0	90.0	1.5	71.4	239.0	-2.6	4.1	-1.1
253	212	15	21	8.0	6.1	0.53	137.3	60.8	1.8	30.1	6.7	3.2	-1.5	5.0
255	133	26	8	11.8	8.9	0.56	37.6	360.0	-4.9	89.2	180.0	-1.5	-3.3	-6.4

Figures 4.13-1 to 4.13-5 Tref, Tu, and Td Parameter Activation Energies (DUT #457, All Hopper Bits with >=5 hops)



>=5 HOPS



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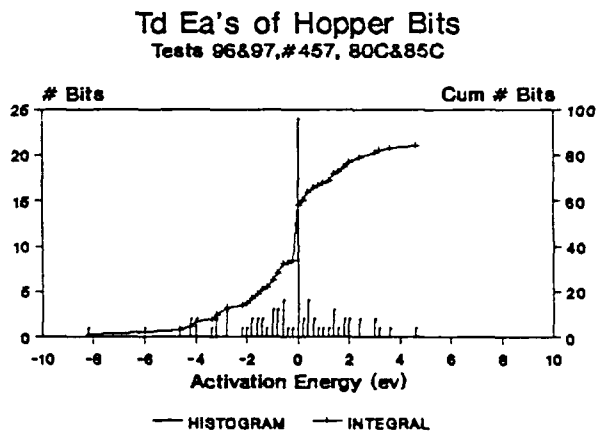

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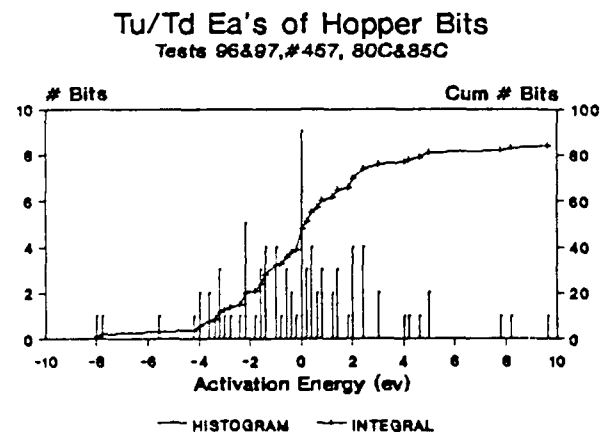

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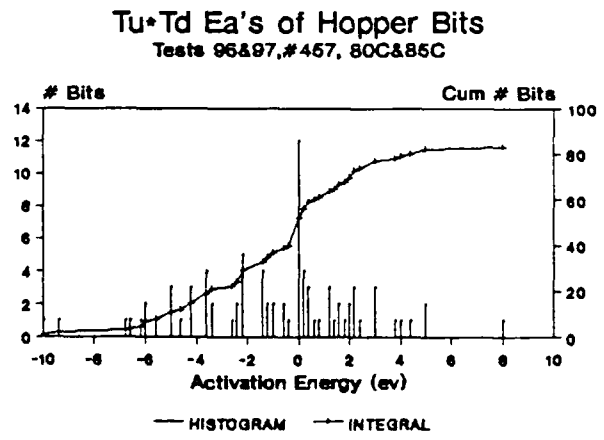
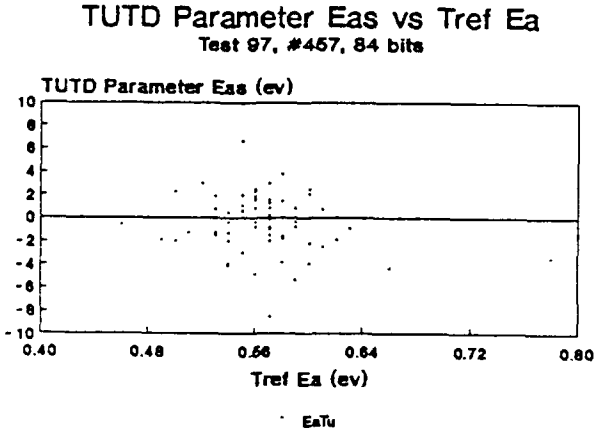
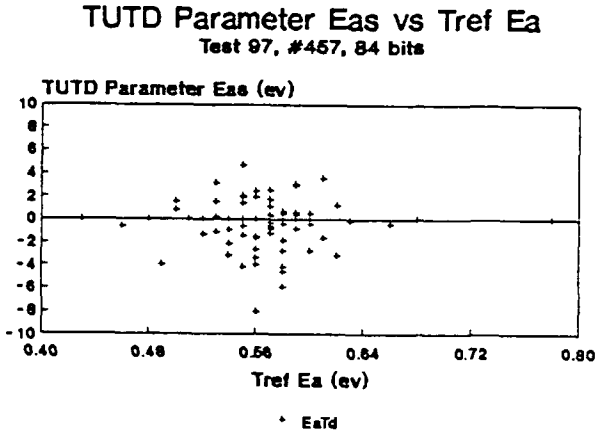
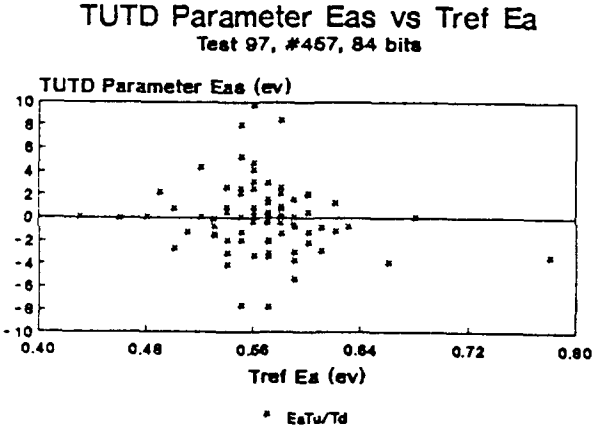


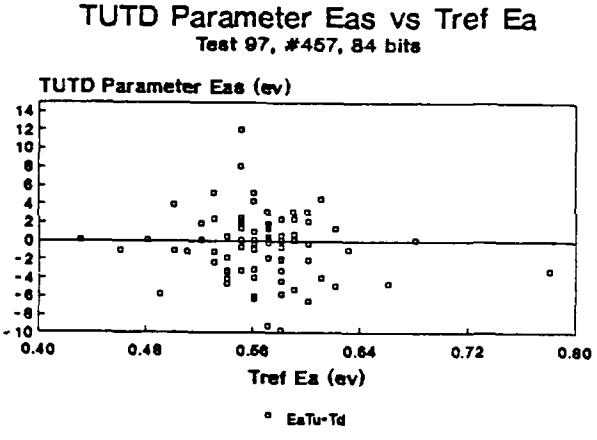
>=5 HOPS

Figures 4.13-6 to 4.13-9 Tu, Td, Tu/Td and Tu*Td Ea's vs Tref Ea's
(DUT #457, All Hopper Bits with >=5 hops)

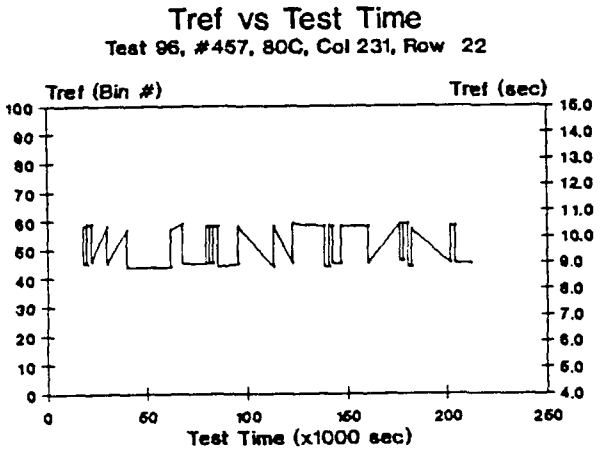


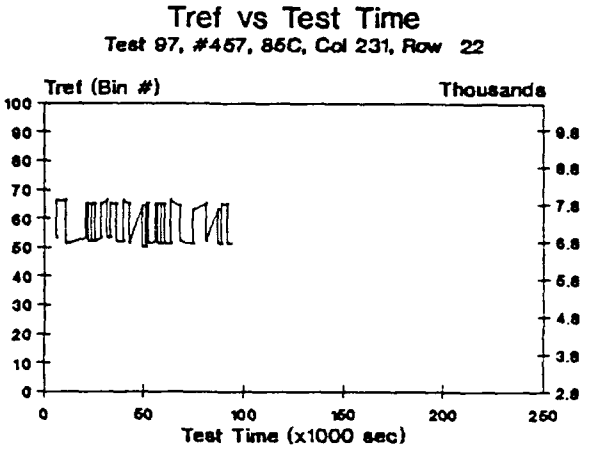


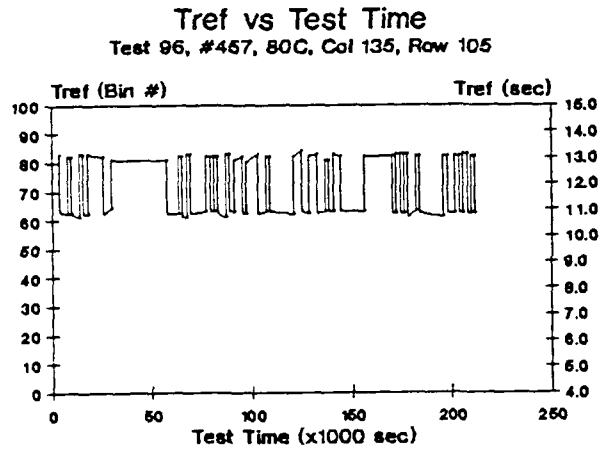


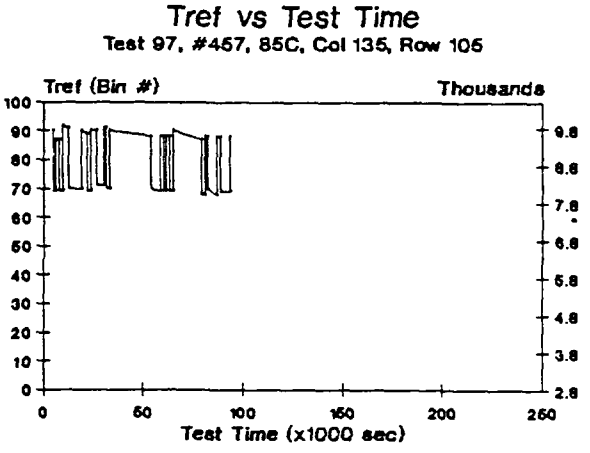


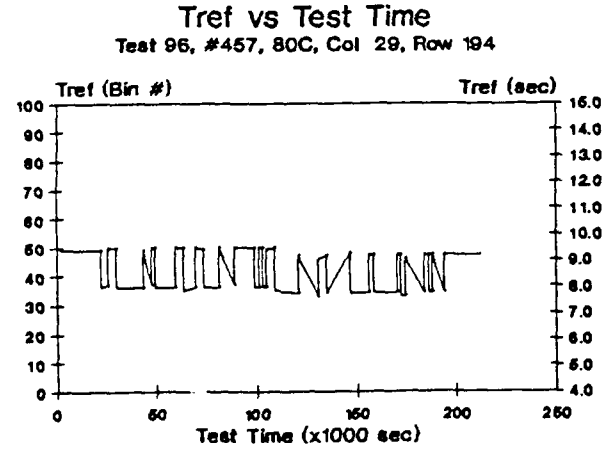
Figures 4.13-10a to 4.13-10f Tref vs Test Time Waveforms
(DUT #457, selected bits 1-3, each at two temperatures)

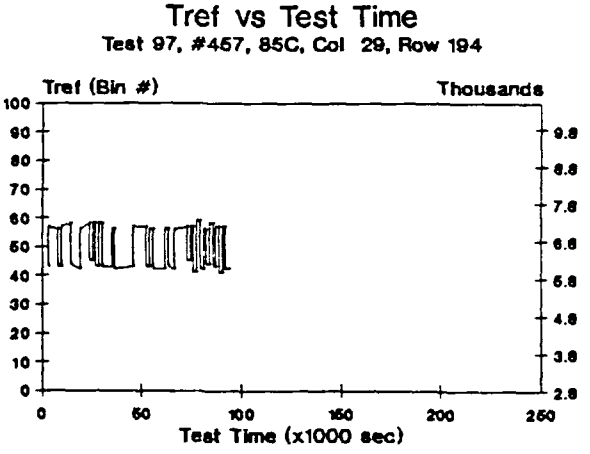




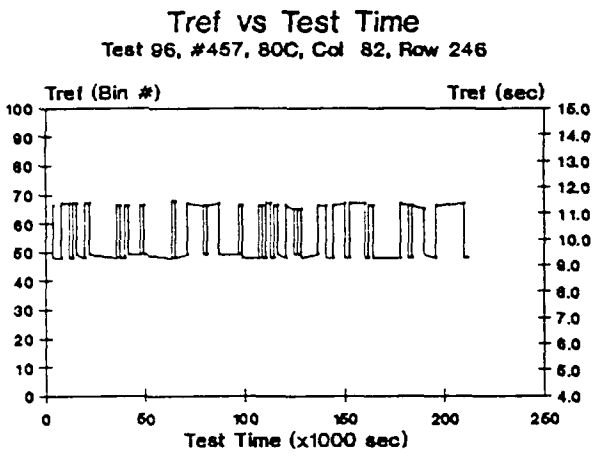


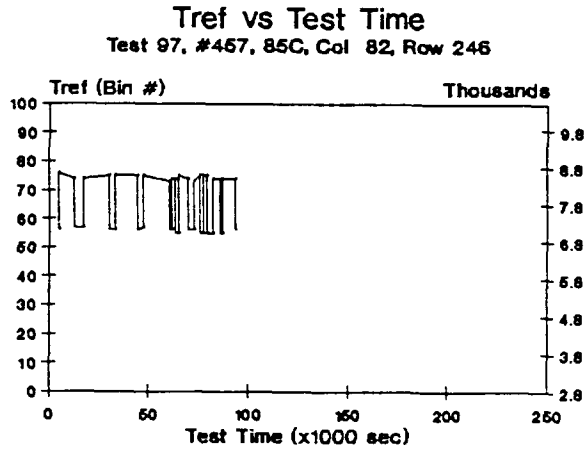


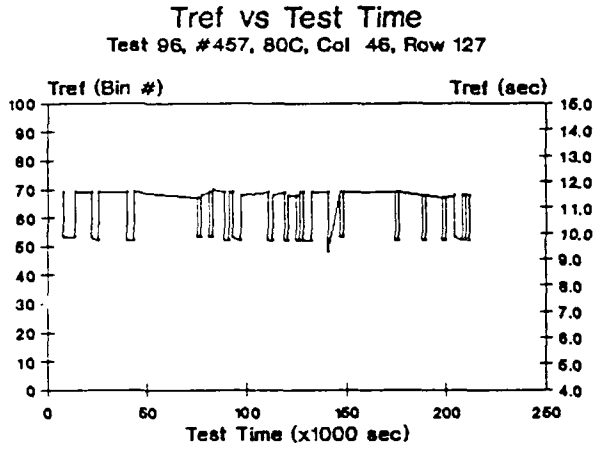


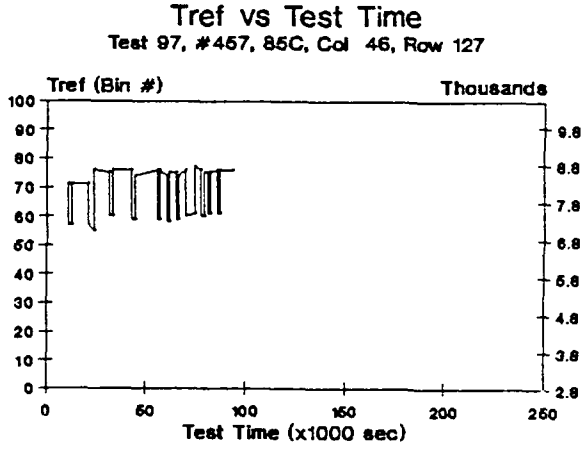


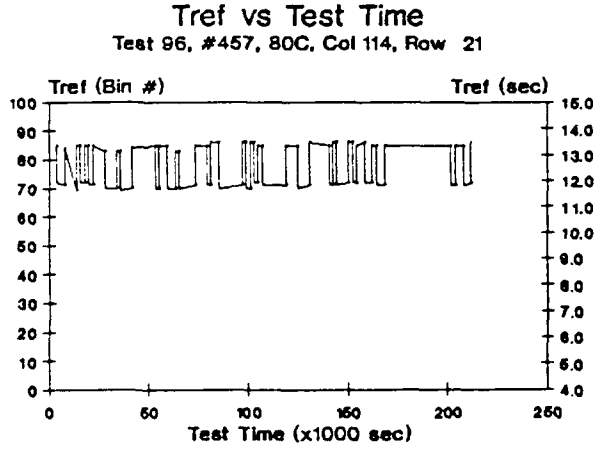
Figures 4.13-11a to 4.13-11f Tref vs Test Time Waveforms
(DUT #457, selected bits 4-6, each at two temperatures)

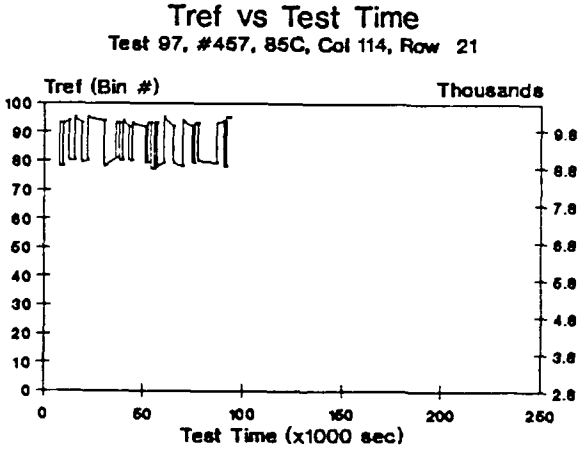




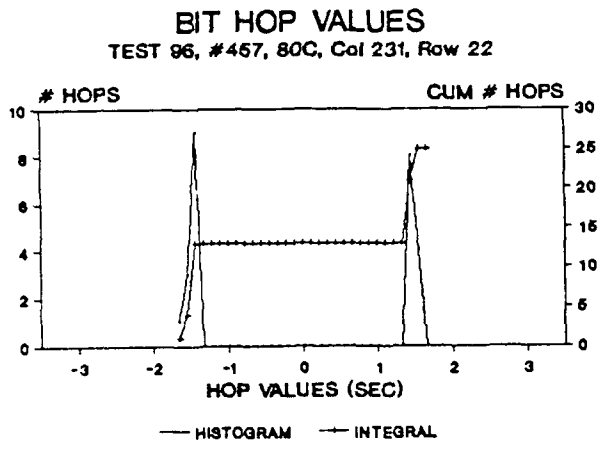


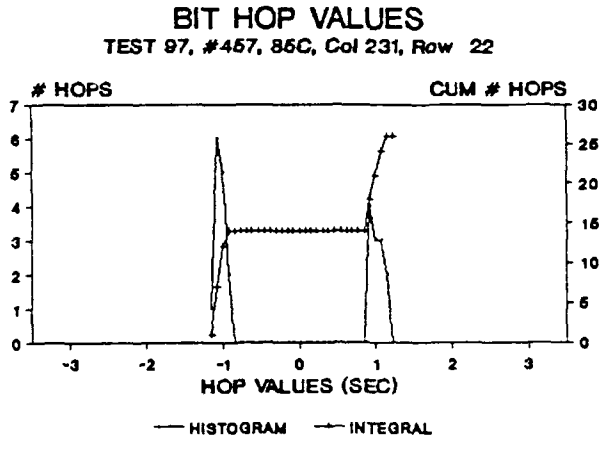


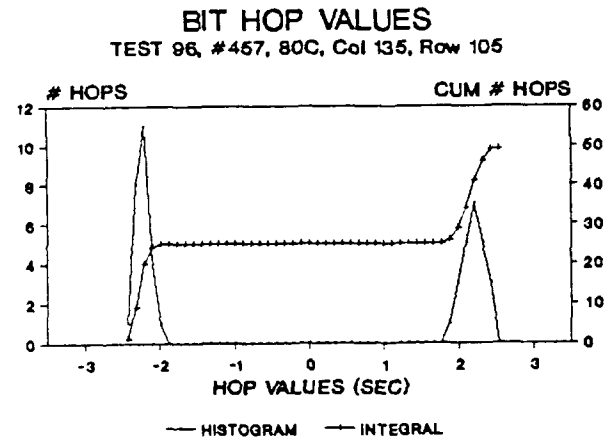


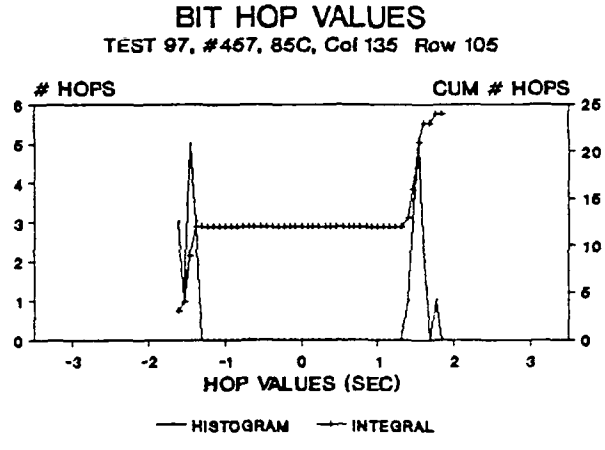


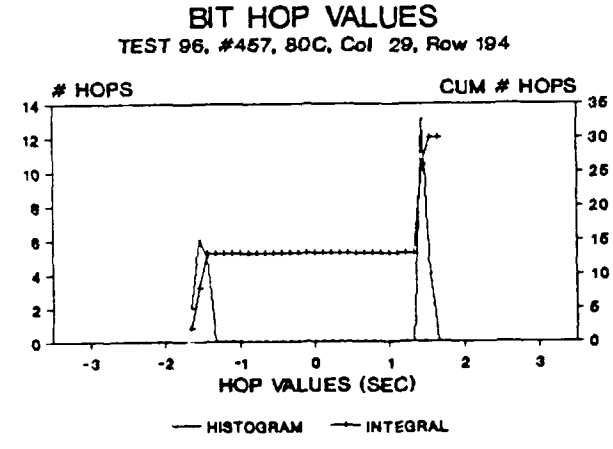
Figures 4.13-12a to 4.13-12f Hop Value Histograms
(DUT #457, selected bits 1-3, each at two temperatures)

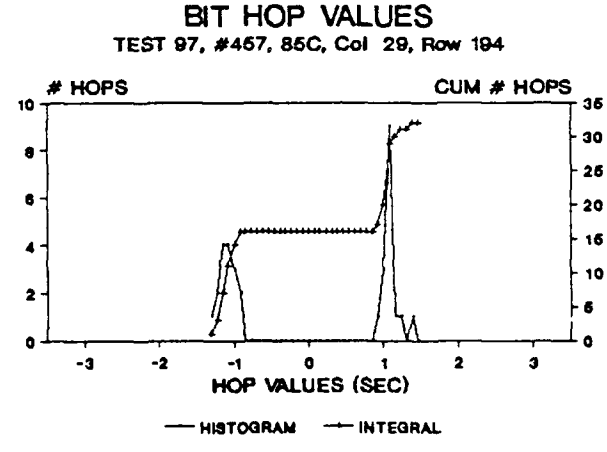




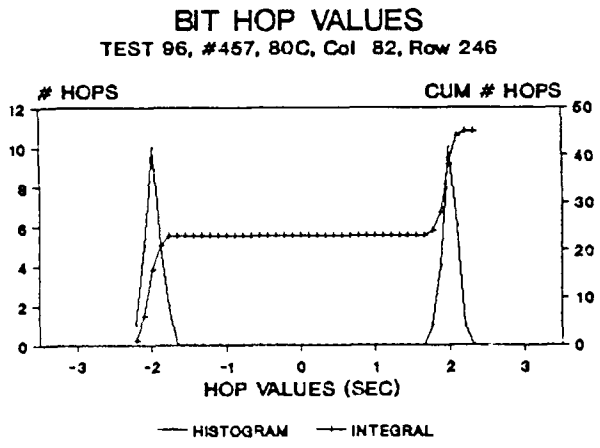


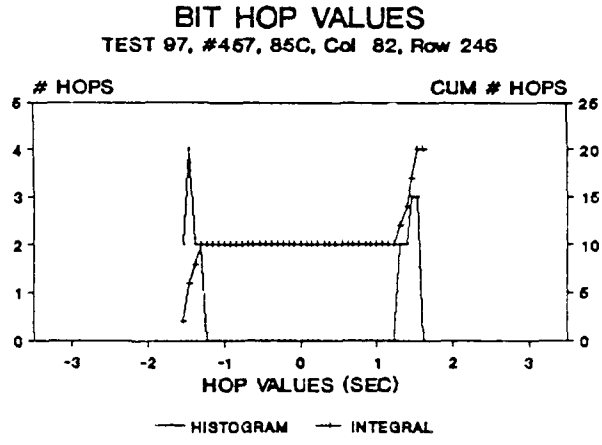


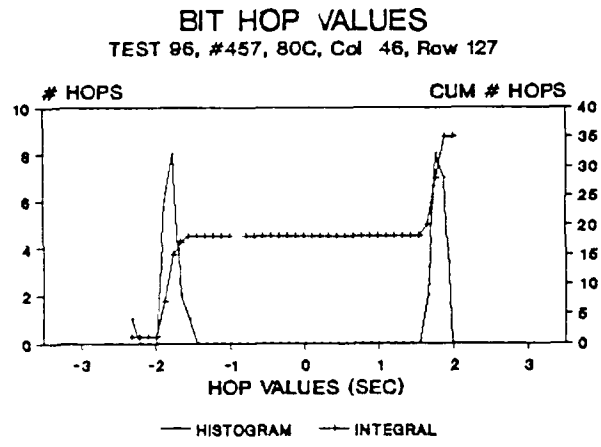


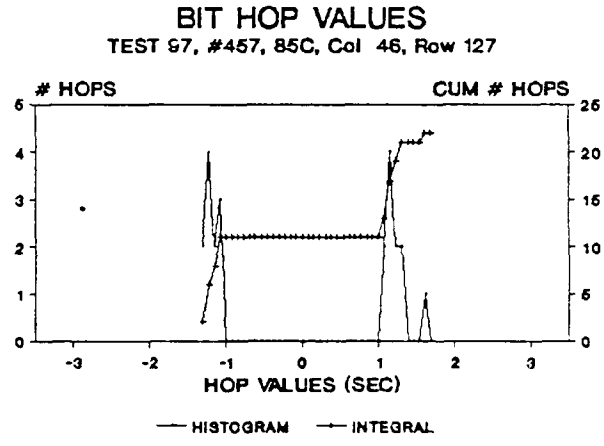


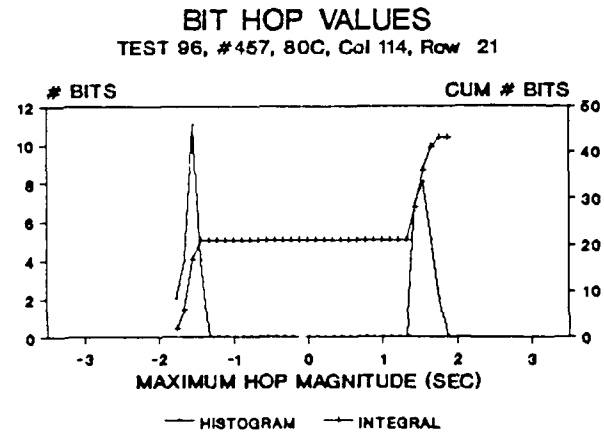
Figures 4.13-13a to 4.13-13f Hop Value Histograms
(DUT #457, selected bits 4-6, each at two temperatures)

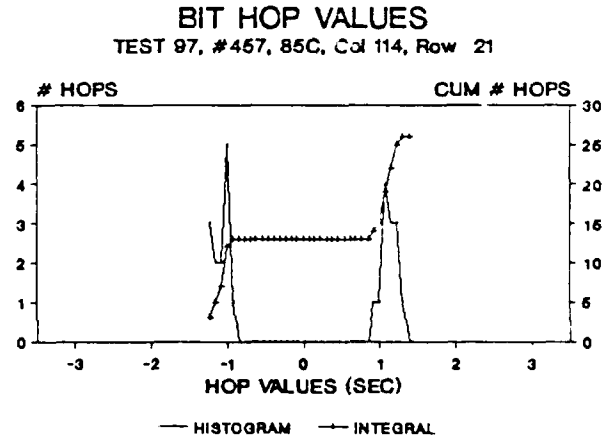




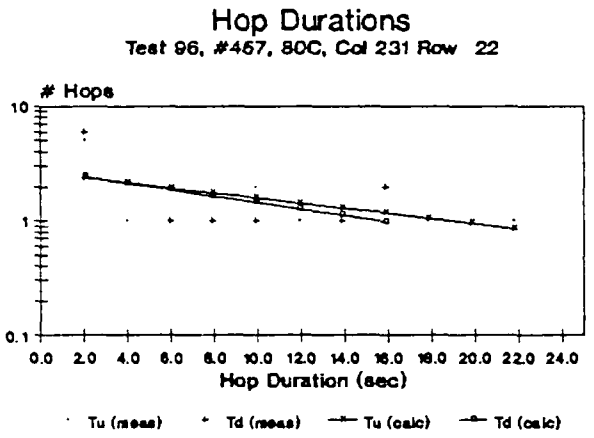


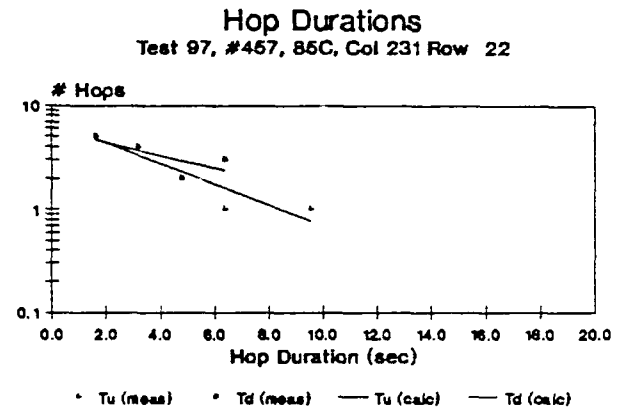




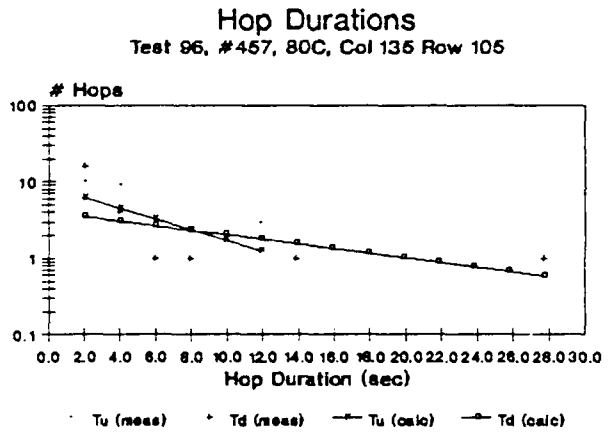


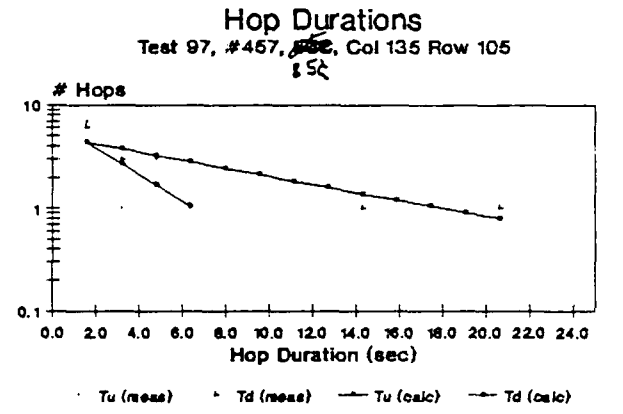
Figures 4.13-14a to 4.13-14f Tu and Td Duration Histograms
(DUT #457, selected bits 1-3, each at two temperatures)



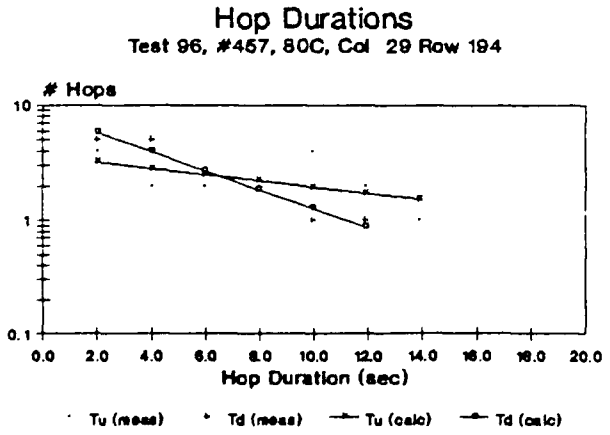


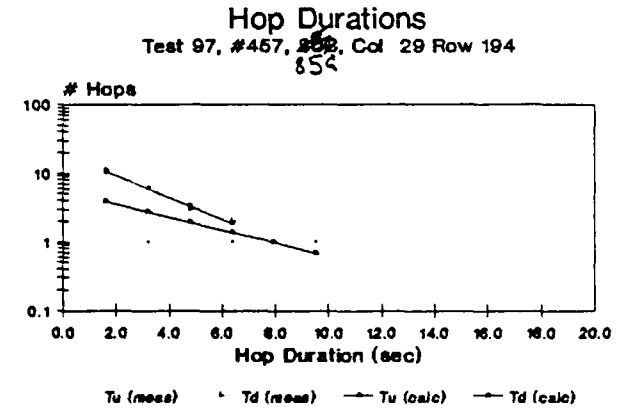
EaTr=0.56ev EaTu=2.3ev EaTd=1.9ev
EaTu/Td=0.4ev EaTu-Td=4.2





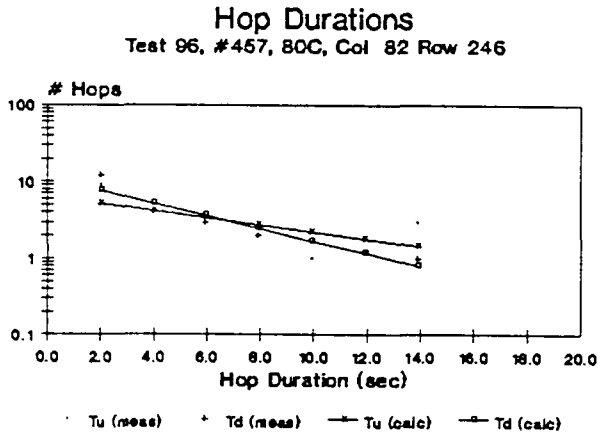
EaTr=0.59ev EaTu=-0.4ev EaTd=0.4ev
EaTu/Td=-0.8ev EaTu-Td=0.1ev

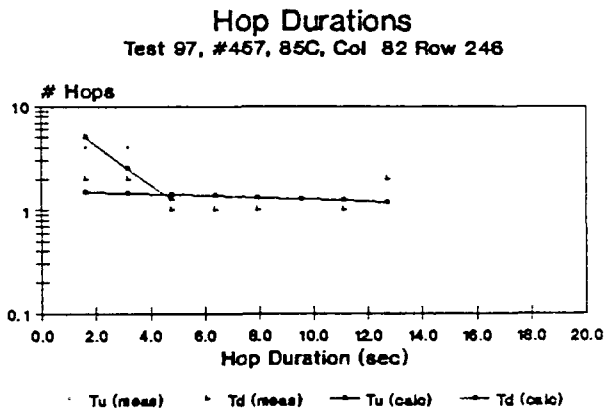




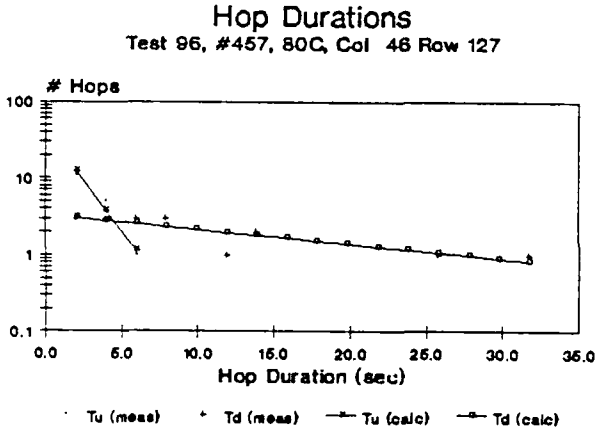
EaTr=0.50ev EaTu=2.2ev EaTd=1.5ev
EaTu/Td=0.7ev EaTu-Td=3.8ev

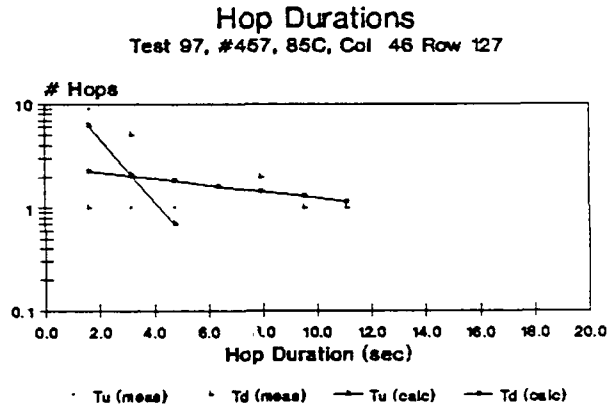
Figures 4.13-15a to 4.13-15f Tu and Td Duration Histograms
(DUT #457, selected bits 4-6, each at two temperatures)



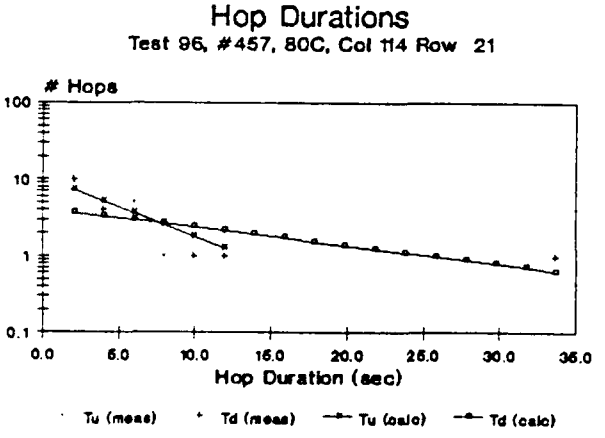


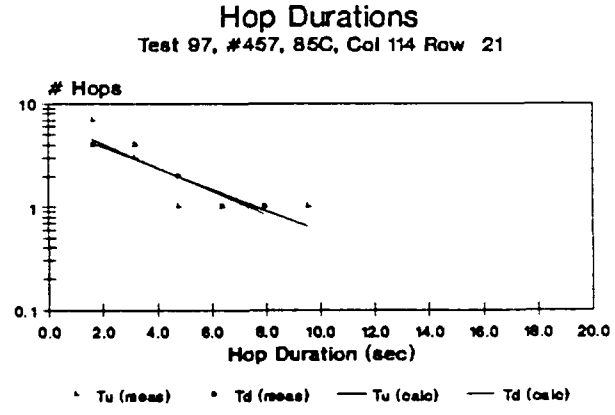
EaTr=0.56ev EaTu=1.0ev EaTd=4.2ev
EaTu/Td=5.2ev EaTu-Td=-3.3ev





EaTr=0.58ev EaTu=-1.7ev EaTd=-0.4ev
EaTu/Td=-1.4ev EaTu-Td=-2.1ev





EaTr=0.57ev EaTu=-1.0ev EaTd=1.1ev
EaTu/Td=-2.1ev EaTu-Td=0.1ev

5.0 Discussion:

Section 5.1 will review the operation of the basic DRAM cell, and relate observations in the references on Random Telegraph Noise to that operation. In Section 5.2 we will compare our results to those of AT&T's in [1]. In Section 5.3 we will make further comments about our results, and in Section 5.4 we will discuss possible new physical models.

5.1 Operation of a DRAM Cell and Relation To Random Telegraph Noise (RTN).

In a typical DRAM storage cell, the storage gate is connected to a positive voltage (eg. 2.5v or 5v) , and the substrate to some small negative voltage (eg. -2v). A potential well is created in the silicon surface below the storage gate. When the cell is written, the bitline supplies a positive voltage through the access transistor, removing minority carrier electrons from the potential well. Carrier generation mechanisms in the bulk Si, at the surface, and at nearby junctions supplies free carriers to the vicinity of the potential well. Electrons tend to be swept into the potential well, and holes away from it. The maximum refresh time is a measure of how long it takes for the well to fill to the critical amount of charge which the sense amp regards as opposite the written logic level. A higher rate of electron generation and collection tends to decrease refresh time. Electrons would also tend to tunnel from the silicon surface to the positively biased storage gate electrode. This would tend to increase Tref as electrons are lost from the potential well. Before the cell is read out, the bitline to the cell and the bitline to a dummy cell (written with an empty potential well) are precharged to some positive voltage. Then the cells are simuitaneously connected to the bitlines, and to a differential amplifier. The bitlines dip (lower for a full potential well than for an empty potential well), and the sens amp responds to the difference in the dips of the two cells to determine the stored data.

In the devices tested, all rows on a column share a sense amp and dummy cell. Therefore, if the dummy cell was written with an empty potential well, unstable leakage current in the dummy cell would affect Tref for multiple rows. This was not observed in these devices, indicating that the instabilities were in the memory cells, not in the dummy cells and sense amplifiers.

We now return to the discussion of Section 1.2.6, and the relation to RTN. It would be of interest to know the location and origin of the traps which cause VHT in the DRAM cell.

In [11] experiments with varying temperature and bias led to the conclusion that the traps responsible for RTN components of drain currents in most Si devices were in the Si or near the Si-SiO2 interface. Various types of traps may hold a positive or negative charge, though one type may dominate. For traps in the Si, capture time depends inversely on carrier concentration. Emission time depends inversely on trap energy, and exponentially on temperature. For traps in the SiO2 near the Si surface, capture time depends on tunneling of carriers from the silicon, and is inversely dependent on carrier concentration there.

Traps in areas of high carrier concentration will have very high occupance rates, short unpopulated times, and may be undetectible (eg. an electron trap in the inverted silicon channel area of an n-channel MOSFET). Traps in areas of low carrier concentration will experience infrequent captures, but alternating emissions of different types can result in high and low drain current level duration times that are similar, and therefore these

traps may be detectable. Also, for a MOSFET in weak inversion, the most important traps are those at the source end of the channel. For example, a populated hole trap in the oxide near the source end of an access transistor which is biased off is mirrored by some portion of a negative charge in the channel, increasing subthreshold drain leakage current. A populated electron trap in the substrate facing the source junction would behave similarly. The fractional change depends on the location and extent of the influence of the charge in relation to the channel width.

Considering depletion regions at the edges of the inversion layer associated with the potential well in a DRAM storage cell, when a trap in the oxide near a generation-recombination center is in the negative state, the field in the depleted p-type silicon below it is locally lower, and field dependent leakage current should be less. The field in the silicon above it is locally higher, and field dependent leakage current there should be more. When such a trap is in the positive state, the field in the silicon below it is locally higher, and field dependent leakage current should be higher. The field in the silicon above it is locally lower, and field dependent leakage current there should be less.

It was observed in [11] that for MOSFETs in weak inversion (low drain voltage and currents), RTS amplitude was a fixed fraction of mean current, on the order of 1-2% for their samples (a 1NJ5 with a gate width of nominally 1.5um). It was found to be independent of bias and temperature over wide ranges. However, the fraction varied from .01% to 100% for other anomalous JFET samples.
We see similar behavior for VHT. For example, on page 33 of this report we noted ratios of hop magnitude to Trefavg of 14.3% and 12.9% at 80C and 85C for DUT #127, col 266, row 136. The ratios for DUT #457, col 231, row 22 (see Figure 4.13-10) were 15.4% and 13.6%. The fractions are much higher than those for the INJ5, which suggests that subthreshold conductance modulation by traps at the source end of the access transistor is not the primary leakage mechanism. They also observed a 0.6ev activation energy for the square root of the product Tu*Td, deriving from the temperature dependence of the square of ni (the intrinsic carrier concentration). We did calculate the Ea of Tu*Td, but we saw a wide variation, probably due to few data points in some of the curves.

Now consider the effects of changes in trap occupancy on tunneling current from the Si into the SiO2. In the oxide close to the Si/SiO2 interface anywhere beneath the storage gate, capture of a hole, or emission of an electron from a trap would increase the field below. This would cause higher electron tunneling current into the oxide. Loss of electrons by tunneling into the oxide would increase the time required to fill the well with electrons, which would increase refresh time. Emission of a hole or capture of an electron would decrease the field below, and the tunneling electron current, and decrease refresh time.

It would be interesting to observe hopping behavior as a function of the amount of charge in the well during filling. If the hop magnitudes were small, and the time constant much smaller than Tref, it might be possible to see a difference in hop rate as the well fills. If the silicon surface potential could be measured, it would slope down in a staircase due to VHT, rather than in a smooth ramp. The free carrier concentration is low everywhere below the cell plate and in the channel of the access transistor during early filling, when the potential well is empty. Considering an electron trap in the silicon near the surface, as the potential well fills with electrons the probability of the trap being filled increases and the hopping rate should decrease. Considering an electron trap in the oxide near the surface, as the well fills the potential at the silicon surface rises, and the field across the oxide increases. The probablity of an electron tunneling into the SiO2

increases, and with it the probability of an electron trap in the oxide being populated. This should also decrease the hopping rate. Considering a hole trap in the silicon, since the concentration of holes is very low everywhere below the storage gate early in the filling process (and even lower later), there should be little change in the hopping rate due to a hole trap filling. Again, as the well fills and the surface potential drops, the field in the oxide increases, and the probability of electrons tunneling into the oxide increases. A hole trap in the oxide would be unaffected by this, and hopping rate should remain the same.

It would also be interesting to characterize hopping as the potential on the storage gate was increased, as in [12] where leakage current was studied. If hopping rates increased, it might mean that the traps were associated with the cell periphery rather than beneath the storage gate.

5.2 Comments with regard to RL vs AT&T Results

In [1] the Ea of Tref of hoppers was observed to be anomalously low. We did not observe that in our tests. This may be because we calculated the Ea using the average of the high and low levels at each temperature, or because of a difference in the devices. As noted previously, anomalously low Ea's do result if the low level is used at the low temperature and the high level is used at the high temperature. A Tref Ea screen test based on one Tref measurement at two temperatures would not be effective. In cases where hopper bits are distinguished by low Ea of Tref, a proper screen must identify both hop levels at both temperatures. This would require much more test time than a simple one shot Tref test. We note that in our tests time constants as long as tens of hours were observed. If this were not done, however, it is quite likely that active and severe hopper bits could be missed entirely. We must agree with the observation in [1] that present DRAM screens may not catch severe VHT. It would seem that Tref tests during burn-in could be done, in a manner similar to our testing. They did observe an increase in hopping activity at higher Vdd, and attributed it to increased field effects in the well. However, it would seem that perphery affects could also explain this behavior. At higher voltages, the periphery of the cell becomes larger, and encompasses more of the bird's beak where the thin storage cell oxide transitions to the thicker field oxide. If it were richer in unstable traps, the hopping behavior would worsen.

5.3 Other Comments

High temperature Tref specs should be large enough to accommodate VHT. Since a Tref distribution measured at any given time includes some bits in the low Tref range in the low state, it could serve as a guide in setting Tref specs. It should be measured at the highest temperature, since Tref is lowest there. Even so, there is risk of missing severe, infrequent hopper bits, unless the Tref distribution is monitored continually over tens of hours. Also, there is some risk of there being large, infrequent, short duration hops, which would be difficult to catch.

At very low temperatures, there is the possibility of drastically increasing the refresh interval due to much lower leakage currents [2]. However, VHT characteristics at low temperature have not been studied.

Analog DRAM cells have been considered for storage of synapse weights in artificial neural network chips. VHT at the 15% level we observed here would appear to limit the precision of weight storage to about 1/.15 or about 6 bits. Although there have been

studies of the effect of small amounts of noise injected on some weights during training, (to increase fault tolerance), the effect of 15% noise on a random set of many weights during training and subsequent performance has not been investigated.

As long as Tref specs are conservative with respect to VHT, it is not likely that these devices will exhibit soft errors due to VHT, however, we did not develop enough data in this effort to predict the frequency of occurrence of very large hops. We did test devices in addition to those reported here, and there was one case where the Tref spec was quite close to the Trefavg of all bits at high temperature.

Another observation we made is that hopper bits are more likely to have higher Trefs. This may suggest that some factor which increases Tref also increases the likelihood of VHT. Factors which would increase cell capacitance and Tref include thinner oxide, larger cell area, higher substrate doping, larger surface state density, wider or shorter transfer gate, and increased storage plate roughness. There also could be some relation to a factor which decreases leakage current into the cell, such as better local gettering or fewer generation centers.

5.4 Possible New Physical Model

In RTN of small MOS transistors the evidence points to trapping and detrapping of charge at a location within the gate oxide, close enough to the oxide-silicon interface for a single charge to produce an observable effect on the charge flowing in the channel, but far enough to trap and detrap only rarely. That is, the field from the trapped charge must be significant at the channel, but there must be only a small overlap of the trap structure with the wave function of the carriers in the channel. In that model a single charge slightly modulates an existing current. That is possible because the current is restricted to a very small region in close proximity to the trapped charge.

In contrast, the current involved in causing loss of information from a DRAM capacitor is mostly produced by thermal generation of carriers within a relatively large volume. It is clear that in cases where the hold time assumes only two values that the phenomenon must be caused by effects from the charging and discharging of a single trap, but the relatively large modulation is not consistent with the direct modulation of the thermally generated current since a single charge affects only a small region in its immediate vicinity. Two possibilities present themselves.

The first is the presence of a trap near a bounding surface of and within the depletion region where a tunneling barrier can be modulated--both in height and width-- by a charged state of the trap. For this case one would expect the frequency of hopping from one hold time to another to be temperature dependent, but the size of the leakage current to be independent of temperature. An important part of this model is the difference in dimensionality between the trap and the surface nearby which is affected by the field of the trapped charge. The latter might be linear in an interface surface or two dimensional otherwise. In either case the excess tunneling current will have a relatively small cross section for further interaction directly with the trapped charge, permitting thermal effects to play the major role in trapping and detrapping.

The second possibility is the presence of an oxide inclusion left over from the surface denuding process. If this is large enough to trap a charge then the generation process at the surface of the inclusion might be substantial, enough to account for ten or twenty percent of the thermally generated current. When charged it would have a substantially reduced probability of emitting a hole-electron pair as a consequence of the interaction with one member of the pair, and its interaction with the other member. The emissions

would tend to be virtual rather than real. In this case it might be expected that the amplitude of the modulation would track the temperature dependence of the average hold time (phonon population). It would be expected that such an inclusion would be of the order of two nanometers in radius, comparable to the trapping depth observed near MOS channels.

Although the measurement of the "excess" current observed in the case of a stable two-level "hopper" is not very precise, it appears that the second case best describes our data. Absolute comparisons from one temperature to another are subject to variations of hold time both from actual variations in the leakage current and from variations in the triggering level of the sense amplifiers. We did not characterize this effect in the devices we tested.

6.0 Physical Analysis

This section discusses physical analysis done in an attempt to identify anomalies which correlate with unstable Tref measurements. After testing, we delayered the devices and inspected several bit locations with optical and scanning electron microscopes. We looked at both 'hopper' bits which exhibited unstable Trefs, and surrounding 'good' bits which had stable Trefs. This section shows typical results selected after analyzing about five hopper bits in each of two devices from two manufacturers (four devices total). Not much could be seen with the optical microscope at 500X, but it was useful to judge when oxide or polysilicon layers were removed. A frame store was used to grab the SEM images. We found it useful to integrate several images and sometimes use the sharpening filters, and the contrast and brightness stretching capabilities of the "Crystal" image processor to highlight otherwise very subtle features. We were bothered by rather poor initial image quality, which we think was due to a combination of sample charging and floor vibration.

The bits chosen for inspection were picked from lists of the outliers of the distributions mentioned in Section 3, i.e. those which exhibited the largest numbers of hops, the largest ranges of Tref values, etc. Generally, five to ten bits which were easy to physically locate were chosen from a list of the 'worst' one hundred. Finding these bit locations on the devices required familiarity with the DUT layouts. We computed physical address maps from data sheet information, and verified them using the optical analysis techniques described in Appendix A. We learned to identify the rows, columns, transfer gates, and storage cell structures in each device. We located a bit location by counting to specific row and column locations while moving the device under a fixed marker on the SEM screen, while scanning at high magnification with a fast frame rate.

Memory cell physical layouts for the two device types we analyzed are shown in Figure 6.1a, for reference to the SEM micrographs later in this section. Bit lines run vertically and word lines run horizontally, as they do in all of the figures which follow. Figure 6.1b shows a drawing of a cell cross section (produced by tracing a photo of a mechanically lapped cross section (which was stopped just outside of the transfer gate area). Figure 6.1c. shows an electrical schematic diagram of a cell. We would look in particular for physical anomalies in the polysilicon, oxide, and silicon associated with the transfer gate of the access transistor, the storage gate area of the memory cell, and along the perimeter of those areas. As noted in Section 1, others have observed disturbances in the bulk silicon which correlated to hopping activity [1].

6.1 Delayering

We obtained delayering procedures written by the device manufacturers. Our results were probably somewhat different, however, because we used different plasma etching equipment, we substituted some etches which we were more familiar with, and because we had a limited number of samples to practice on. The most bothersome problem was lack of etch selectivity, e.g., the plasma etch step intended to remove the nitride passivation would attack any poly2 which was exposed. Similarly, plasma etching or chemical etching aimed at poly2 would also etch exposed poly1, and also any part of the exposed silicon surface. This sometimes occurred if there was over-etching during an previous step. When the delayering recipe is right, and one is practiced, these should not be problems. However, we did notice that it was typical to have quite different total etching results in two corners of a chip, even though we covered the entire device

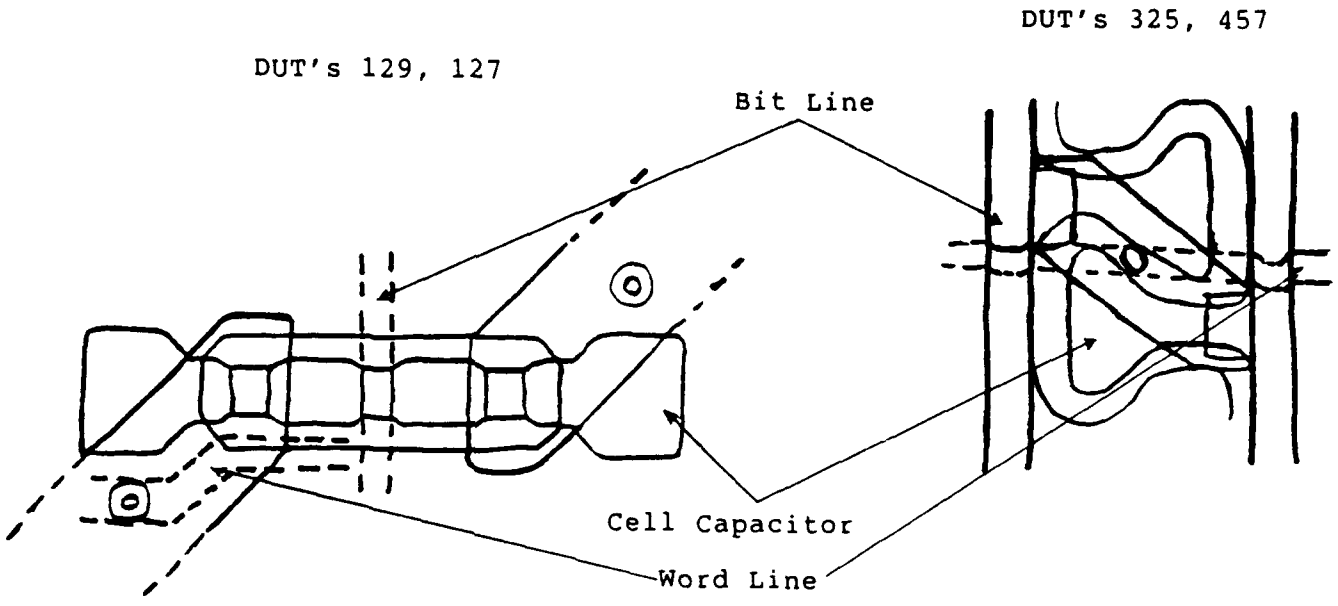


Figure 6.1a. Memory cell physical layouts.

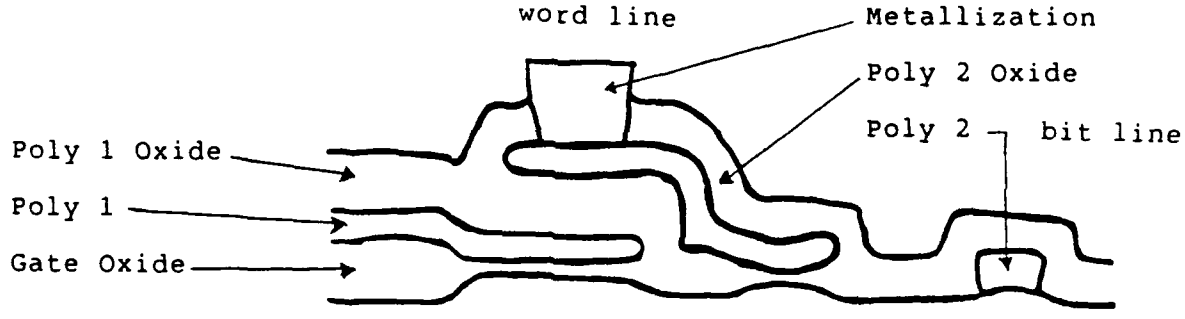


Figure 6.1b. Memory cell physical crossection (not to scale).

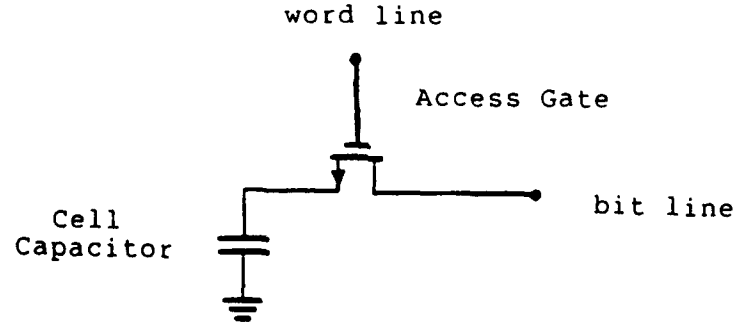


Figure 6.1c. Memory cell electrical schematic.

surface with etchant. We do not know if the etching techniques or the devices caused this effect.

The first step in the delayering sequence was removal of the organic alpha-protection overcoat with fuming red nitric acid at 70C. We used a 10-1 ratio CF4-O2 plasma etch, in a small 75 watt barrel reactor, to remove nitride passivation. We used Siloxide (a commercial buffered HF etch) to remove any remaining oxide overcoat, and interlevel passivations. An aluminum etch consisting of a 1-nitric,1-acetic, 2-water, and 16-phosphoric acid was used to remove the Al metal conductors. The polysilicon etch we used contained 1 part 49% hydrofluoric acid, 40 parts 70% nitric acid, 20 parts distilled water, and 2 parts glacial acetic acid. A 10-1 stain (nitric-hydroflouric) was used as a substrate etch. The results of this etching and inspection is given below.

6.2 Device #129

Figures 6.2a-d and 6.3a-d show SEM micrographs of active hopper bits at logical col,row addresses 127,189 and 242,134 at four steps in the delayering process. First, the alpha coating was removed by seven minutes in fuming red nitric at 70C. Passivated metal row lines were seen at this point, but no storage cell layout detail could be seen. To remove the nitride overcoat passivation, the part was plasma etched in intervals of less than about 5 minutes, for a total time of about 17 minutes. The metal bit lines were removed with a 3 minute B-etch, and the interlevel oxide was removed by a 5 second HF etch. This was supposed to expose the transfer gate and storage gate polysilicon (Figure 6.2a and 6.3a).

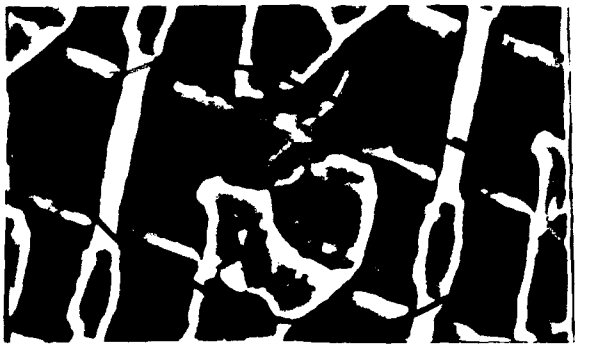
Then the polysilicon storage gate was removed with a 45 sec chemical poly to reveal the storage gate dielectric, as shown in Figures 6.2b and 6.3b. It is apparent that some of the N+ S/D areas which were not under poly 1 had also been opened by the HF etch before the poly etch. Therefore, the poly etch had also etched the access transistor source/drain areas quite deeply. After this poly etch, the gate dielectric in the storage gate was bare, although thicker oxide islands remain in areas which had been under poly2. The gate dielectric was then removed by a short HF etch. Figure 6.2c and 6.3c show that there were some anomalies (indicated by the arrows). At this point we found it difficult to distinguish between extraneous particles introduced by the etches and washing, and features really associated with the device. It is entirely possible that the anomalies noted here were extraneous. However, the next step was a light substrate etch, and this often highlighted suspicious features, e.g., those indicated by arrows in Figure 6.2d, which may very well be crystal faults in the silicon substrate.

We did not always see such anomalies associated with hopper bits, however. There were several hopper bits which had very clear and uniform storage gate areas after the substrate etch. We generally did not continue with further substrate etching. We also saw artifacts in other bits which we had not selected to inspect. We did not expend time counting out those locations to see if they were also bits which hopped.

We do not know what the small white particulates are in the final photos in Figures 6.2d and 6.3d. We were relatively unfamiliar with these devices, and we are not sure whether they are real device features. If they are simply "sticky" particulate contamination, they must have been introduced by the poly etch, since we used the same washing procedures after the etch. If they are real features in the device, we do not know what could cause such a high and variable density. They are submicron in size, and they are found in all areas of the device. It is conceivable that they were related to implant damage of some sort, although they do not seem to be confined to S/D areas.

Figure 6.2. #129, LC 127 LR 189

Figure 6.3 #129, LC 242, LR 134



a. After alpha coat, passivation, metal, and interlevel dielectric removal.

b. After 1st poly storage gate removal. N+ S/D areas have etched deeply.

c. After storage cell gate removal. Arrows indicate possible anomalies.

d. Silicon surface etched. Arrows indicate anomaly sites.

6.3 Device #325

The manufacturer of this device was different from that of device #129. This device was etched to remove the alpha coat, nitride passivation, and metal runs, as discussed above. Figures 6.4a and 6.5a show that poly2 is almost bare, although the thickness of the remaining oxide appears to be different for the two bits. There is also thicker oxide in areas which had been under Al metal runs. Further oxide etching with HF cleared the poly surfaces, as shown in Figures 6.4b and 6.5b. Then the poly was removed with poly etch. We expected that Figures 6.4c and 6.5c would show the remaining gate dielectric, but apparently, there was not complete removal of the oxide over poly1. The poly etch went through holes in the oxide to only partially etch poly1. A relatively long poly etch was then done to remove the rest of the poly1, but this also attacked the Si surface, as shown in Figures 6.4d and 6.5d. About the only features of interest at this point are pits in the cell plate areas which indicate uneven etching, but they were not unique to the hopper bit. This device also had some submicron features which appear as small white spots similar to those seen on the other manufacturer's devices, but at a very much lower densities by comparison.

6.4 Conclusions Based on Physical Analysis

Only one of the four bit locations shown here had a clearly observable substrate anomaly. It was our impression by looking at several hopper bits and the good bits that surrounded them that all hopper bits do not have clearly observable substrate anomalies. We do not know how likely it is that we might have missed defects because of lack of etching experience, but that is possible. However, similar substrate anomalies were observed in nearby bits presumed to be stable. No other obvious flaws in the oxides, poly, dielectric, or metal layers were found which correlated to hopping behavior. Finally, variable densities of submicron features were found which we could not identify. These, too, were not confined to hopper bits. This evidence really is inconclusive, but it leads us to suspect that hopping may not be totally explained by the presence of gross substrate defects alone. Indeed, the references we have reviewed suggest that in theory, single trapping sites may give rise to the observed fluctuations, and we would not expect to be able to observe single isolated trapping sites by SEM inspection. We think that it would be interesting to observe the gate dielectric and silicon surfaces of hopping and stable bit locations at higher resolution, e.g., with a scanning atomic force microscope.

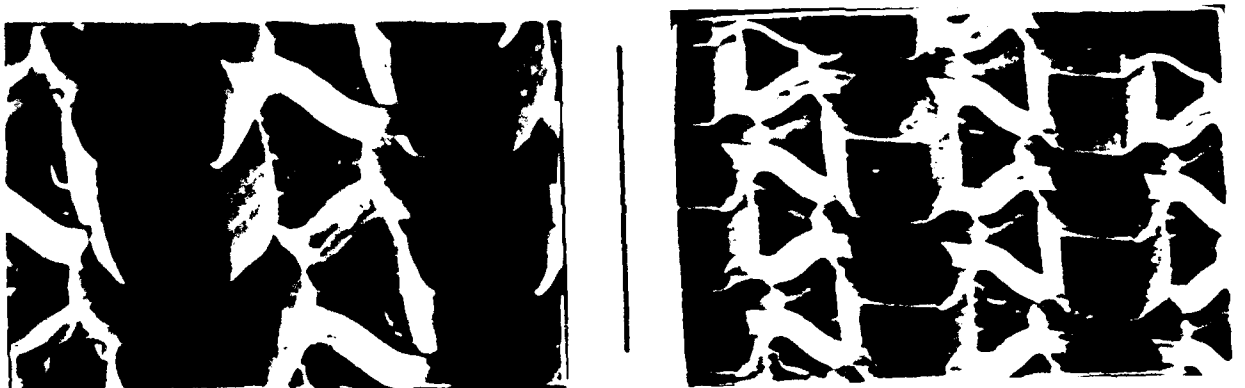
Figure 6.4. #325, LC 80 LR 246

Figure 6.5 #325, LC 64, LR 64

a. After alpha coat, passivation, metal, partial interlevel oxide removal.

b. After further interlevel oxide removal. Some poly1 is bare.

c. After transfer gate ploy1 removal. Some poly2 etched through oxide holes.



d. Silicon surface etched. Irregular etch probably due to delayering.

7.0 Conclusions and Recommendations

This study has shown that for the devices tested, VHT is a real phenomena, and that it accounts for about a 15% instability in Tref. Few devices were tested, however, and we can say little about the variability of VHT across production lots.

We also show that a proper screen for VHT based on Tref activation energy must identify the high and low Tref states of a bit at two temperatures in order to avoid mistakes in calculating the activation energy of Tref. Using this method, we see no trend in the Ea of Tref for hopper bits when compared to the overall population, and therefore no motivation for a screen based on Tref Ea. What is needed is a long (tens of hours) monitored test in which Tref is continually monitored for all bits in a device. Such tests can be implemented using techniques described in this report.

The mechanism causing VHT is uncertain, and is characterized by inconsistent behavior from bit to bit with temperature. This is probably partially due to insufficient data, and uncertainty about whether the same trapping center was being observed at two temperatures in some of our tests. It may also be due to the wide variety of effects which a change in trap occupancy will cause, depending on the trap's polarity and location.

This work has suggested experiments with test structures which might give more information about the traps.

We recommend that vendors characterize their parts for the VHT instability, and investigate the variability of this mechanism over production lots. If warranted, experiments involving variations in production process steps should be done to determine correlations with VHT behavior, and possible fixes.

8.0 References

[1] "A Meta-Stable Leakage Phenomenon in DRAM Charge Storage - Variable Hold Time", D.S. Yaney, C.Y. Lu, R.A. Kohler, M.J. Kelly, and J.T. Nelson, IEDM 1987, paper 14.4.

[2] "Low Temperature Operation of Silicon Dynamic Random Access Memories", P. Wyns, W. DesJardin, and R.L. Anderson, IEEE Transaction on Electron Devices, Vol 36, No. 8, August 1989, pg. 1423-28.

[3] "1/f and Random Telegraph Noise in Silicon Metal Oxide Semiconductor Field Effect Transistors", M.J. Uren, D.J. Day, and M.J. Kirton, Appl. Phys. Lett. 1 December 1985, pg. 1195-97.

[4] "Anomalous Telegraph Noise in Small-Area Silicon Metal Oxide Semiconductor Field Effect Transistors", M.J. Uren, M.J. Kirton, and S. Collins, Physical Review, 12 May 1988, pg. 8346-50.

[5] "Flicker Noise Characteristics of Advanced MOS Technologies", K.K. Hung, P.K. Ko, C. Hu, and Y.C. Cheng, IEDM 1988, pg. 34-37.

[6] "An Automated System for Measurement of Random Telegraph Noise in Meal-Oxide-Semiconductor Field-Effect Transistors", K.K. Hung, P.K. Ko, C. Hu, and Y.C. Cheng, IEEE Trans. on ED, Vol. 36, No.6, June 1989.

[7] "Leakage Studies in High Density Dynamic MOS Memory Devices", P.K. Chatterjee, et. al., IEEE Trans. on ED, ED-26, 1979, pp. 564-575.

[8] "Parasitic Leakage in DRAM Trench Storage Capacitor Vertical Gated Diodes", W.P. Noble, A. Bryant, and S.H. Voldman, IEEE IEDM 1987, paper 14.5, pg. 340-343.

[9] "Degradation of Refresh Time in Dynamic MOS RAM by Irradiation of Alpha Particles", Tsutomu Yoshihara, et. al., IEEE Trans on ED, Vol. ED-28, No. 10, Oct. 1981, pg. 1198-1199.

[10] "Alpha-Particle-Induced Soft Errors in Dynamic Memories", T.C. May and M.H. Woods,Proc. of the 1978 IEEE International Reliability Physics Symposium, pg. 33-40.

[11] "A Physical Model for Random Telegraph Signal Currents in Semiconductor Devices", K. Kandiah, F.B. Deighton, and F.B. Whiting, J. Appl. Phys. 66 (2), 15 July 1989, pg. 937-948

[12] "Leakage Studies in High-Density Dynamic MOS Memory Devices", P. Chatterjee et. al., IEEE Trans on ED, Vol. ED-26, No. 4, Apr., 1979.

Appendix A.

Logical to Physical Address Map Verification Using Die Illumination

This appendix describes how we implemented and verified software for producing bit mapped displays of refresh time (or other parameters). The only practical way to produce these images on a PC is by assembly language programs using table look-up software. These must be supplied with a table for translating logical row and column addresses to screen coordinates.

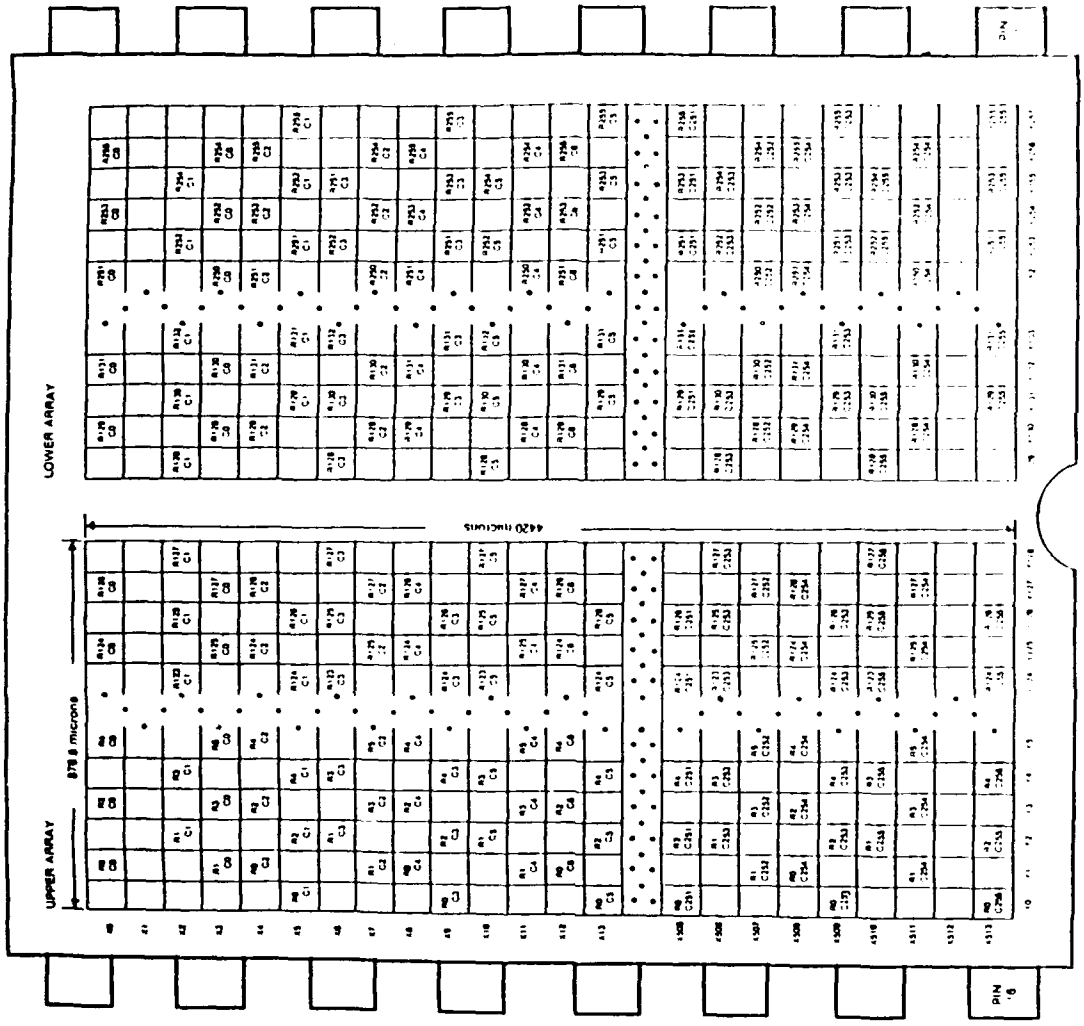
Memory device data sheets generally give information which enables users to calculate the logical addresses of specific physical bit locations, so that topologically correct data patterns can be used in testing. This information is usually in the form of a table and a circuit diagram which show the logical weight of physical address bits, and a map of the physical address layout. Also, the data polarity dependence of physical address is shown, that is, whether a 0 is stored as a full potential well or an empty well. Figure A-1 and A-2 show the data sheet information for the two main devices tested in this study.

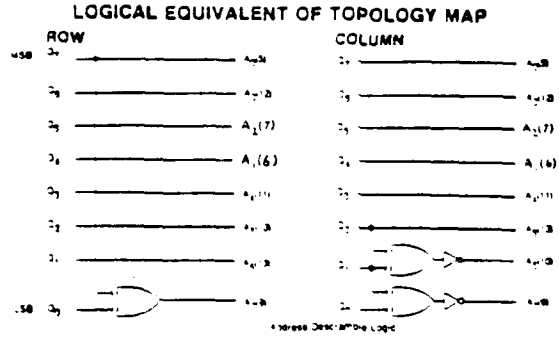
In these variable hold time studies, we were only interested in failure mechanisms causing an empty potential well to fill. Therefore, the testing programs had to determine which data polarity to write for an empty potential well. This detail is explained on the device data sheet, and amounted to writing one data value in the upper physical array (rows 128-255) and the other data value in the lower physical array (rows 0-127), as shown in Figures A-1 and A-2.

We used the data sheet information to write a program which generates a map file which specifies the logical to physical address mapping, as well as the reverse physical to logical address mapping. The map file generation program flow chart is shown in Figure A-3. This file also contains a list of display screen X and Y coordinates, which is corrected for physical address layout, for each logical row (for both even and odd columns), and for each logical column (for both even and odd rows). Actually, the lists apply to the lower half of the array (rows 0-127), and the programs using the table make a simple correction for rows in the upper half array (rows 128-255). Tables TA-1 and TA-2 show the map files generated for the two devices corresponding to Figures A-1 and A-2. These tables can be used in several ways:

for logical row I, look up physical row PR
for logical col I, look up physical col PC
for physical row I, look up logical row LR
for physical col I, look up logical col LC
for logical row I, for even PC, look up screen Y SRE
for logical row I, for odd PC, look up screen Y SRO
for logical col I, for even PR, for PR<128, look up screen X SCE
for logical col I, for odd PR, for PR<128, look up screen X SCO
for logical col I, for even PR, for PR>127, look up screen X SCO
for logical col I, for odd PR, for PR>127, look up screen X SCE

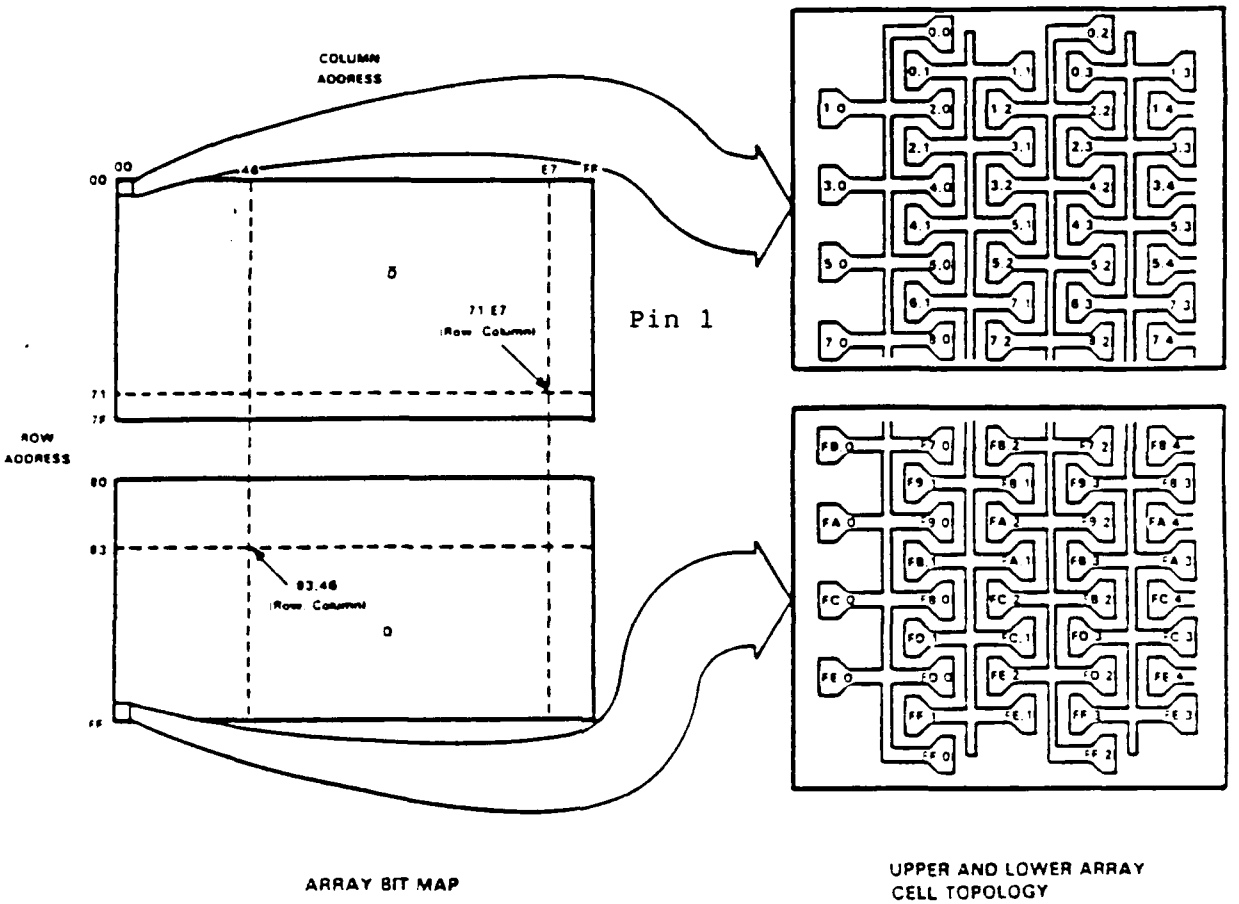
Figure A-1. Vendor 1 Data Sheet Information
for Address Mapping and Data Polarity





Data to write for Empty Well:
Data = 0 if logical row bit 0 = 1 (physical rows 128-255)
Data = 1 if logical row bit 0 = 0 (physical rows 0-127)

Figure A-2. Vendor 2 Data Sheet Information
for Address Mapping and Data Polarity



DESIRED ROW OR COLUMN ADDRESS		WEIGHT	PIN NAME	PIN #
(MSB)	A7	2^7	A7	9
	A6	2^6	A0	5
	A5	2^5	A2	6
	A4	2^4	A1	7
	A3	2^3	A5	10
	A2	2^2	A4	11
	A1	2^1	A3	12
(LSB)	A0	2^0	A6	13

ADDRESS DESCRAMBLING

Data to write for Empty Well:
Data = 1 if logical row bit 7 = 1 (physical rows 128-255)
Data = 0 if logical row bit 0 = 0 (physical rows 0-127)

Figure A-3. Flow Chart of Logical to Physical Address Map File Generation Program

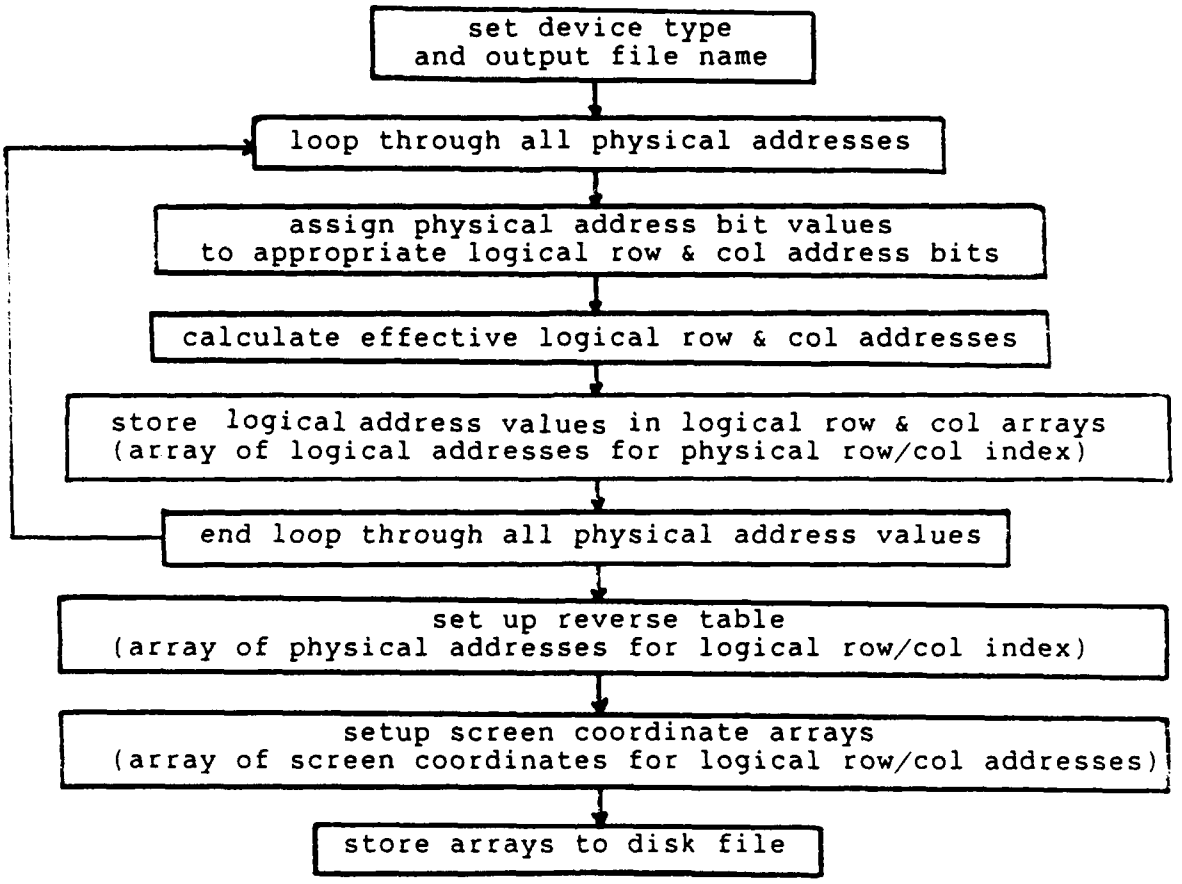


Table TA-1. Vendor 1 Address Translation Map Table

I	PR	PC	LR	LC	SRE	SRO	SCE	SCO
0	0	2	0	160	1	0	0	3
1	129	130	128	32	1	2	5	2
2	16	18	64	0	3	2	4	7
3	145	146	192	128	3	4	9	6
4	32	34	32	192	5	4	8	11
5	161	162	160	64	5	6	13	10
6	48	50	96	96	7	6	12	15
7	177	178	224	224	7	8	17	14
8	64	66	16	176	9	8	16	19
9	193	194	144	48	9	10	21	18
10	80	82	80	16	11	10	20	23
11	209	210	208	144	11	12	25	22
12	96	98	48	208	13	12	24	27
13	225	226	176	80	13	14	29	26
14	112	114	112	112	15	14	28	31
15	241	242	240	240	15	16	33	30
16	8	10	2	162	17	16	32	35
17	137	138	130	34	17	18	37	34
18	24	26	66	2	19	18	36	39
19	153	154	194	130	19	20	41	38
20	40	42	34	194	21	20	40	43
21	169	170	162	66	21	22	45	42
22	56	58	98	98	23	22	44	47
23	185	186	226	226	23	24	49	46
24	72	74	18	178	25	24	48	51
25	201	202	146	50	25	26	53	50
26	88	90	82	18	27	26	52	55
27	217	218	210	146	27	28	57	54
28	104	106	50	210	29	28	56	59
29	233	234	178	82	29	30	61	58
30	120	122	114	114	31	30	60	63
31	249	250	242	242	31	32	65	62
32	4	1	4	164	33	32	64	67
33	133	129	132	36	33	34	69	66
34	20	17	68	4	35	34	68	71
35	149	145	196	132	35	36	73	70
36	36	33	36	196	37	36	72	75
37	165	161	164	68	37	38	77	74
38	52	49	100	100	39	38	76	79
39	181	177	228	228	39	40	81	78
40	68	65	20	180	41	40	80	83
41	197	193	148	52	41	42	85	82
42	84	81	84	20	43	42	84	87
43	213	209	212	148	43	44	89	86
44	100	97	52	212	45	44	88	91
45	229	225	180	84	45	46	93	90
46	116	113	116	116	47	46	92	95
47	245	241	244	244	47	48	97	94
48	12	9	6	166	49	48	96	99
49	141	137	134	38	49	50	101	98
50	28	25	70	6	51	50	100	103
51	157	153	198	134	51	52	105	102
52	44	41	38	198	53	52	104	107
53	173	169	166	70	53	54	109	106
54	60	57	102	102	55	54	108	111
55	189	185	230	230	55	56	113	110
56	76	73	22	182	57	56	112	115
57	205	201	150	54	57	58	117	114
58	92	89	86	22	59	58	116	119
59	221	217	214	150	59	60	121	118
60	108	105	54	214	61	60	120	123
61	237	233	182	86	61	62	125	122
62	124	121	118	118	63	62	124	127
63	253	249	246	246	63	64	129	126
64	2	5	8	168	65	64	128	131
65	131	133	136	40	65	66	133	130
66	18	21	72	8	67	66	132	135
67	147	149	200	136	67	68	137	134
68	34	37	40	200	69	68	136	139
69	163	165	168	72	69	70	141	138
70	50	53	104	104	71	70	140	143
71	179	181	232	232	71	72	145	142
72	66	69	24	184	73	72	144	147
73	195	197	152	56	73	74	149	146
74	82	85	88	24	75	74	148	151
75	211	213	216	152	75	76	153	150
76	98	101	56	216	77	76	152	155
77	227	229	184	88	77	78	157	154
78	114	117	120	120	79	78	156	159
79	243	245	248	248	79	80	161	158
80	10	13	10	170	81	80	160	163
81	139	141	138	42	81	82	165	162
82	26	29	74	10	83	82	164	167
83	155	157	202	138	83	84	169	166
84	42	45	42	202	85	84	168	171
85	171	173	170	74	85	86	173	170
86	58	61	106	106	87	86	172	175
87	187	189	234	234	87	88	177	174
88	74	77	26	186	89	88	176	179
89	203	205	154	58	89	90	181	178
90	90	93	90	26	91	90	180	183
91	219	221	218	154	91	92	185	182
92	106	109	58	218	93	92	184	187
93	235	237	186	90	93	94	189	186
94	122	125	122	122	95	94	188	191
95	251	253	250	250	95	96	193	190
96	6	6	12	172	97	96	192	195
97	135	134	140	44	97	98	197	194
98	22	22	76	12	99	98	196	199
99	151	150	204	140	99	100	201	198
100	38	38	44	204	101	100	200	203
101	167	166	172	76	101	102	205	202
102	54	54	108	108	103	102	204	207
103	183	182	236	236	103	104	209	206
104	70	70	28	188	105	104	208	211
105	199	198	156	60	105	106	213	210
106	86	86	92	28	107	106	212	215
107	215	214	220	156	107	108	217	214
108	102	102	60	220	109	108	216	219
109	231	230	188	92	109	110	221	218
110	118	118	124	124	111	110	220	223
111	247	246	252	252	111	112	225	222
112	14	14	14	174	113	112	224	227
113	143	142	142	46	113	114	229	226
114	30	30	78	14	115	114	228	231
115	159	158	206	142	115	116	233	230
116	46	46	46	206	117	116	232	235
117	175	174	174	78	117	118	237	234
118	62	62	110	110	119	118	236	239
119	191	190	238	238	119	120	241	238
120	78	78	30	190	121	120	240	243
121	207	206	158	62	121	122	245	242
122	94	94	94	30	123	122	244	247
123	223	222	222	158	123	124	249	246
124	110	110	62	222	125	124	248	251
125	239	238	190	94	125	126	253	250
126	126	126	126	126	127	126	252	255
127	255	254	254	254	127	128	257	254
128	1	3	129	161	130	129	256	259
129	128	131	1	33	130	131	261	258
130	17	19	193	1	132	131	260	263
131	144	147	65	129	132	133	265	262
132	33	35	161	193	134	133	264	267
133	160	163	33	65	134	135	269	266
134	49	51	225	97	136	135	268	271
135	176	179	97	225	136	137	273	270
136	65	67	145	177	138	137	272	275
137	192	195	17	49	138	139	277	274
138	81	83	209	17	140	139	276	279
139	208	211	81	145	140	141	281	278
140	97	99	177	209	142	141	280	283
141	224	227	49	81	142	143	285	282
142	113	115	241	113	144	143	284	287
143	240	243	113	241	144	145	289	286
144	9	11	131	163	146	145	288	291
145	136	139	3	35	146	147	293	290
146	25	27	195	3	148	147	292	295
147	152	155	67	131	148	149	297	294
148	41	43	163	195	150	149	296	299
149	168	171	35	67	150	151	301	298
150	57	59	227	99	152	151	300	303
151	184	187	99	227	152	153	305	302
152	73	75	147	179	154	153	304	307
153	200	203	19	51	154	155	309	306
154	89	91	211	19	156	155	308	311
155	216	219	83	147	156	157	313	310
156	105	107	179	211	158	157	312	315
157	232	235	51	83	158	159	317	314
158	121	123	243	115	160	159	316	319
159	248	251	115	243	160	161	321	318
160	5	0	133	165	162	161	320	323
161	132	128	5	37	162	163	325	322
162	21	16	197	5	164	163	324	327
163	148	144	69	133	164	165	329	326
164	37	32	165	197	166	165	328	331
165	164	160	37	69	166	167	333	330
166	53	48	229	101	168	167	332	335
167	180	176	101	229	168	169	337	334
168	69	64	149	181	170	169	336	339
169	196	192	21	53	170	171	341	338
170	85	80	213	21	172	171	340	343
171	212	208	85	149	172	173	345	342
172	101	96	181	213	174	173	344	347
173	228	224	53	85	174	175	349	346
174	117	112	245	117	176	175	348	351
175	244	240	117	245	176	177	353	350
176	13	8	135	167	178	177	352	355
177	140	136	7	39	178	179	357	354
178	29	24	199	7	180	179	356	359
179	156	152	71	135	180	181	361	358
180	45	40	167	199	182	181	360	363
181	172	168	39	71	182	183	365	362
182	61	56	231	103	184	183	364	367
183	188	184	103	231	184	185	369	366
184	77	72	151	183	186	185	368	371
185	204	200	23	55	186	187	373	370
186	93	88	215	23	188	187	372	375
187	220	216	87	151	188	189	377	374
188	109	104	183	215	190	189	376	379
189	236	232	55	87	190	191	381	378
190	125	120	247	119	192	191	380	383
191	252	248	119	247	192	193	385	382
192	3	4	137	169	194	193	384	387
193	130	132	9	41	194	195	389	386
194	19	20	201	9	196	195	388	391
195	146	148	73	137	196	197	393	390
196	35	36	169	201	198	197	392	395
197	162	164	41	73	198	199	397	394
198	51	52	233	105	200	199	396	399
199	178	180	105	233	200	201	401	398
200	67	68	153	185	202	201	400	403
201	194	196	25	57	202	203	405	402
202	83	84	217	25	204	203	404	407
203	210	212	89	153	204	205	409	406
204	99	100	185	217	206	205	408	411
205	4.6	228	57	89	206	207	413	410
206	115	116	249	121	208	207	412	415
207	242	244	121	249	208	209	417	414
208	11	12	139	171	210	209	416	419
209	138	140	11	43	210	211	421	418
210	27	28	203	11	212	211	420	423
211	154	156	75	139	212	213	425	422
212	43	44	171	203	214	213	424	427
213	170	172	43	75	214	215	429	426
214	59	60	235	107	216	215	428	431
215	186	188	107	235	216	217	433	430
216	75	76	155	187	218	217	432	435
217	202	204	27	59	218	219	437	434
218	91	92	219	27	220	219	436	439
219	218	220	91	155	220	221	441	438
220	107	108	187	219	222	221	440	443
221	234	236	59	91	222	223	445	442
222	123	124	251	123	224	223	444	447
223	250	252	123	251	224	225	449	446
224	7	7	141	173	226	225	448	451
225	134	135	13	45	226	227	453	450
226	23	23	205	13	228	227	452	455
227	150	151	77	141	228	229	457	454
228	39	39	173	205	230	229	456	459
229	166	167	45	77	230	231	461	458
230	55	55	237	109	232	231	460	463
231	182	183	109	237	232	233	465	462
232	71	71	157	189	234	233	464	467
233	198	199	29	61	234	235	469	466
234	87	87	221	29	236	235	468	471
235	214	215	93	157	236	237	473	470
236	103	103	189	221	238	237	472	475
237	230	231	61	93	238	239	477	474
238	119	119	253	125	240	239	476	479
239	246	247	125	253	240	241	481	478
240	15	15	143	175	242	241	480	483
241	142	143	15	47	242	243	485	482
242	31	31	207	15	244	243	484	487
243	158	159	79	143	244	245	489	486
244	47	47	175	207	246	245	488	491
245	174	175	47	79	246	247	493	490
246	63	63	239	111	248	247	492	495
247	190	191	111	239	248	249	497	494
248	79	79	159	191	250	249	496	499
249	206	207	31	63	250	251	501	498
250	95	95	223	31	252	251	500	503
251	222	223	95	159	252	253	505	502
252	111	111	191	223	254	253	504	507
253	238	239	63	95	254	255	509	506
254	127	127	255	127	256	255	508	511
255	254	255	127	255	256	257	513	510

Table TA-2. Vendor 2 Address Translation Map Table

I	PR	PC	LR	LC	SRE	SRO	SCE	SCO
0	0	0	0	0	257	256	3	0
1	64	64	64	64	255	256	2	5
2	16	16	8	8	255	254	7	4
3	80	80	72	72	253	254	6	9
4	32	32	16	16	253	252	11	8
5	96	96	80	80	251	252	10	13
6	48	48	24	24	251	250	15	12
7	112	112	88	88	249	250	14	17
8	2	2	32	32	249	248	19	16
9	66	66	96	96	247	248	18	21
10	18	18	40	40	247	246	23	20
11	82	82	104	104	245	246	22	25
12	34	34	48	48	245	244	27	24
13	98	98	112	112	243	244	26	29
14	50	50	56	56	243	242	31	28
15	114	114	120	120	241	242	30	33
16	4	4	2	2	241	240	35	32
17	68	68	66	66	239	240	34	37
18	20	20	10	10	239	238	39	36
19	84	84	74	74	237	238	38	41
20	36	36	18	18	237	236	43	40
21	100	100	82	82	235	236	42	45
22	52	52	26	26	235	234	47	44
23	116	116	90	90	233	234	46	49
24	6	6	34	34	233	232	51	48
25	70	70	98	98	231	232	50	53
26	22	22	42	42	231	230	55	52
27	86	86	106	106	229	230	54	57
28	38	38	50	50	229	228	59	56
29	102	102	114	114	227	228	58	61
30	54	54	58	58	227	226	63	60
31	118	118	122	122	225	226	62	65
32	8	8	4	4	225	224	67	64
33	72	72	68	68	223	224	66	69
34	24	24	12	12	223	222	71	68
35	88	88	76	76	221	222	70	73
36	40	40	20	20	221	220	75	72
37	104	104	84	84	219	220	74	77
38	56	56	28	28	219	218	79	76
39	120	120	92	92	217	218	78	81
40	10	10	36	36	217	216	83	80
41	74	74	100	100	215	216	82	85
42	26	26	44	44	215	214	87	84
43	90	90	108	108	213	214	86	89
44	42	42	52	52	213	212	91	88
45	106	106	116	116	211	212	90	93
46	58	58	60	60	211	210	95	92
47	122	122	124	124	209	210	94	97
48	12	12	6	6	209	208	99	96
49	76	76	70	70	207	208	98	101
50	28	28	14	14	207	206	103	100
51	92	92	78	78	205	206	102	105
52	44	44	22	22	205	204	107	104
53	108	108	86	86	203	204	106	109
54	60	60	30	30	203	202	111	108
55	124	124	94	94	201	202	110	113
56	14	14	38	38	201	200	115	112
57	78	78	102	102	199	200	114	117
58	30	30	46	46	199	198	119	116
59	94	94	110	110	197	198	118	121
60	46	46	54	54	197	196	123	120
61	110	110	118	118	195	196	122	125
62	62	62	62	62	195	194	127	124
63	126	126	126	126	193	194	126	129
64	1	1	1	1	193	192	131	128
65	65	65	65	65	191	192	130	133
66	17	17	9	9	191	190	135	132
67	81	81	73	73	189	190	134	137
68	33	33	17	17	189	188	139	136
69	97	97	81	81	187	188	138	141
70	49	49	25	25	187	186	143	140
71	113	113	89	89	185	186	142	145
72	3	3	33	33	185	184	147	144
73	67	67	97	97	183	184	146	149
74	19	19	41	41	183	182	151	148
75	83	83	105	105	181	182	150	153
76	35	35	49	49	181	180	155	152
77	99	99	113	113	179	180	154	157
78	51	51	57	57	179	178	159	156
79	115	115	121	121	177	178	158	161
80	5	5	3	3	177	176	163	160
81	69	69	67	67	175	176	162	165
82	21	21	11	11	175	174	167	164
83	85	85	75	75	173	174	166	169
84	37	37	19	19	173	172	171	168
85	101	101	83	83	171	172	170	173
86	53	53	27	27	171	170	175	172
87	117	117	91	91	169	170	174	177
88	7	7	35	35	169	168	179	176
89	71	71	99	99	167	168	178	181
90	23	23	43	43	167	166	183	180
91	87	87	107	107	165	166	182	185
92	39	39	51	51	165	164	187	184
93	103	103	115	115	163	164	186	189
94	55	55	59	59	163	162	191	188
95	119	119	123	123	161	162	190	193
96	9	9	5	5	161	160	195	192
97	73	73	69	69	159	160	194	197
98	25	25	13	13	159	158	199	196
99	89	89	77	77	157	158	198	201
100	41	41	21	21	157	156	203	200
101	105	105	85	85	155	156	202	205
102	57	57	29	29	155	154	207	204
103	121	121	93	93	153	154	206	209
104	11	11	37	37	153	152	211	208
105	75	75	101	101	151	152	210	213
106	27	27	45	45	151	150	215	212
107	91	91	109	109	149	150	214	217
108	43	43	53	53	149	148	219	216
109	107	107	117	117	147	148	218	221
110	59	59	61	61	147	146	223	220
111	123	123	125	125	145	146	222	225
112	13	13	7	7	145	144	227	224
113	77	77	71	71	143	144	226	229
114	29	29	15	15	143	142	231	228
115	93	93	79	79	141	142	230	233
116	45	45	23	23	141	140	235	232
117	109	109	87	87	139	140	234	237
118	61	61	31	31	139	138	239	236
119	125	125	95	95	137	138	238	241
120	15	15	39	39	137	136	243	240
121	79	79	103	103	135	136	242	245
122	31	31	47	47	135	134	247	244
123	95	95	111	111	133	134	246	249
124	47	47	55	55	133	132	251	248
125	111	111	119	119	131	132	250	253
126	63	63	63	63	131	130	255	252
127	127	127	127	127	129	130	254	257
128	128	128	128	128	128	127	259	256
129	192	192	192	192	126	127	258	261
130	144	144	136	136	126	125	263	260
131	208	208	200	200	124	125	262	265
132	160	160	144	144	124	123	267	264
133	224	224	208	208	122	123	266	269
134	176	176	152	152	122	121	271	268
135	240	240	216	216	120	121	270	273
136	130	130	160	160	120	119	275	272
137	194	194	224	224	118	119	274	277
138	146	146	168	168	118	117	279	276
139	210	210	232	232	116	117	278	281
140	162	162	176	176	116	115	283	280
141	226	226	240	240	114	115	282	285
142	178	178	184	184	114	113	287	284
143	242	242	248	248	112	113	286	289
144	132	132	130	130	112	111	291	288
145	196	196	194	194	110	111	290	293
146	148	148	138	138	110	109	295	292
147	212	212	202	202	108	109	294	297
148	164	164	146	146	108	107	299	296
149	228	228	210	210	106	107	298	301
150	180	180	154	154	106	105	303	300
151	244	244	218	218	104	105	302	305
152	134	134	162	162	104	103	307	304
153	198	198	226	226	102	103	306	309
154	150	150	170	170	102	101	311	308
155	214	214	234	234	100	101	310	313
156	166	166	178	178	100	99	315	312
157	230	230	242	242	98	99	314	317
158	182	182	186	186	98	97	319	316
159	246	246	250	250	96	97	318	321
160	136	136	132	132	96	95	323	320
161	200	200	196	196	94	95	322	325
162	152	152	140	140	94	93	327	324
163	216	216	204	204	92	93	326	329
164	168	168	148	148	92	91	331	328
165	232	232	212	212	90	91	330	333
166	184	184	156	156	90	89	335	332
167	248	248	220	220	88	89	334	337
168	138	138	164	164	88	87	339	336
169	202	202	228	228	86	87	338	341
170	154	154	172	172	86	85	343	340
171	218	218	236	236	84	85	342	345
172	170	170	180	180	84	83	347	344
173	234	234	244	244	82	83	346	349
174	186	186	188	188	82	81	351	348
175	250	250	252	252	80	81	350	353
176	140	140	134	134	80	79	355	352
177	204	204	198	198	78	79	354	357
178	156	156	142	142	78	77	359	356
179	220	220	206	206	76	77	358	361
180	172	172	150	150	76	75	363	360
181	236	236	214	214	74	75	362	365
182	188	188	158	158	74	73	367	364
183	252	252	222	222	72	73	366	369
184	142	142	166	166	72	71	371	368
185	206	206	230	230	70	71	370	373
186	158	158	174	174	70	69	375	372
187	222	222	238	238	68	69	374	377
188	174	174	182	182	68	67	379	376
189	238	238	246	246	66	67	378	381
190	190	190	190	190	66	65	383	380
191	254	254	254	254	64	65	382	385
192	129	129	129	129	64	63	387	384
193	193	193	193	193	62	63	386	389
194	145	145	137	137	62	61	391	388
195	209	209	201	201	60	61	390	393
196	161	161	145	145	60	59	395	392
197	225	225	209	209	58	59	394	397
198	177	177	153	153	58	57	399	396
199	241	241	217	217	56	57	398	401
200	131	131	161	161	56	55	403	400
201	195	195	225	225	54	55	402	405
202	147	147	169	169	54	53	407	404
203	211	211	233	233	52	53	406	409
204	163	163	177	177	52	51	411	408
205	227	227	241	241	50	51	410	413
206	179	179	185	185	50	49	415	412
207	243	243	249	249	48	49	414	417
208	133	133	131	131	48	47	419	416
209	197	197	195	195	46	47	418	421
210	149	149	139	139	46	45	423	420
211	213	213	203	203	44	45	422	425
212	165	165	147	147	44	43	427	424
213	229	229	211	211	42	43	426	429
214	181	181	155	155	42	41	431	428
215	245	245	219	219	40	41	430	433
216	135	135	163	163	40	39	435	432
217	199	199	227	227	38	39	434	437
218	151	151	171	171	38	37	439	436
219	215	215	235	235	36	37	438	441
220	167	167	179	179	36	35	443	440
221	231	231	243	243	34	35	442	445
222	183	183	187	187	34	33	447	444
223	247	247	251	251	32	33	446	449
224	137	137	133	133	32	31	451	448
225	201	201	197	197	30	31	450	453
226	153	153	141	141	30	29	455	452
227	217	217	205	205	28	29	454	457
228	169	169	149	149	28	27	459	456
229	233	233	213	213	26	27	458	461
230	185	185	157	157	26	25	463	460
231	249	249	221	221	24	25	462	465
232	139	139	165	165	24	23	467	464
233	203	203	229	229	22	23	466	469
234	155	155	173	173	22	21	471	468
235	219	219	237	237	20	21	470	473
236	171	171	181	181	20	19	475	472
237	235	235	245	245	18	19	474	477
238	187	187	189	189	18	17	479	476
239	251	251	253	253	16	17	478	481
240	141	141	135	135	16	15	483	480
241	205	205	199	199	14	15	482	485
242	157	157	143	143	14	13	487	484
243	221	221	207	207	12	13	486	489
244	173	173	151	151	12	11	491	488
245	237	237	215	215	10	11	490	493
246	189	189	159	159	10	9	495	492
247	253	253	223	223	8	9	494	497
248	143	143	167	167	8	7	499	496
249	207	207	231	231	6	7	498	501
250	159	159	175	175	6	5	503	500
251	223	223	239	239	4	5	502	505
252	175	175	183	183	4	3	507	504
253	239	239	247	247	2	3	506	509
254	191	191	191	191	2	1	511	508
255	255	255	255	255	0	1	510	513

The programs which use the map file to create bit mapped images accommodate screen offset and scaling. The using program must only decide whether the logical column is even or odd, whether the row is even or odd, and and whether the row address is greater than or less than 128, and then look up the screen coordinates.

A2. Address Map Verification

Bit mapping software should be verified. The first step was to verify that the software actually bit mapped the logical addresses to the physical locations according to the information supplied on the device data sheets. It also served to verify that the computer hardware we ran it on did not scramble addresses and interfere with writing all empty potential wells. The technical manual schematics indicated that it did not, but we wanted to verify it, as well. The second step was to verify that the decoding actually implemented on the device matched that shown on the data sheet.

To accomplish the first step, we used the software to display 16 simulated refresh time data files. The first eight files had all zeroes except for high values in all bits on columns 1,2,4,8,16,32,64, and 128, respectively. The next eight files had all zeroes except for high values in all bits on rows 1,2,4,8,16,32,64, and 128, respectively. These were displayed, and were all correct. This verified the weighting of the physical addresses, and the correction of physical layout of the physical addresses.

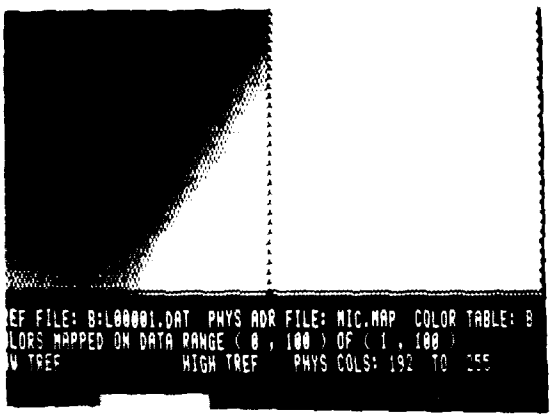
To accomplish the second step, to verify that the decoding actually implemented on the device matched that shown on the data sheet, one approach is to reverse engineer the address decoder circuits. Instead, we first tried Scanning Electron Microscope Voltage Contrast. We were able to verify word line decoding because the metal word line potentials could be read easily. We were not able to verify bit line decoding because we could not resolve potentials on the diffused bit lines.

Then we developed a simple optical technique. Light projected on the chip while it is tested will cause refresh time to be very low in illuminated areas. We projected a diagonal line of light made by a shaped aperture onto a de-lidded device, and ran a single set of refresh time tests. Then we displayed the bit mapped image of refresh time. The image should show very low refresh time in illuminated areas, gradually transitioning to high refresh time in dark areas. This pattern makes it possible to spot both row and column decoding errors as poor definition of the edge. Figures A-4a and A-5a show these patterns for two of the device types studied. They appeared to be correct, but we checked further to determine whether incorrect mappings could actually be detected.

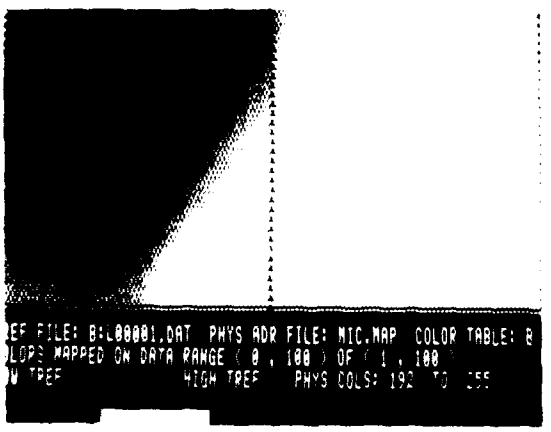
We did this by displaying the patterns with intentionally incorrect map files. Figures A-4b and A-5b show the patterns with least significant two physical row address bit weights swapped. This is the most subtle row mapping error, swapping the middle two rows in each group of four, and is not very recognizable. Figures A-4c and A-5c show the patterns with least significant two physical column address bit weights swapped. This is the most subtle column mapping error, swapping the middle two columns in each group of four, and is somewhat recognizable for one device. Finally, Figures A-6a and A-7a show the patterns with the physical row and column address bits weighted 2 and 4 swapped, and Figures A-6b and A-7b show the patterns with the physical row and column address bits weighted 4 and 8 swapped. These errors are recognizable, as are all mapping errors involving higher weighted bits. We concluded that the mapping software was working correctly.

Figure A-8 shows the first of four screens of a typical bit mapped display of refresh time produced by the PC system. The orientation of the physical rows and column names on the devices are also shown in this figure.

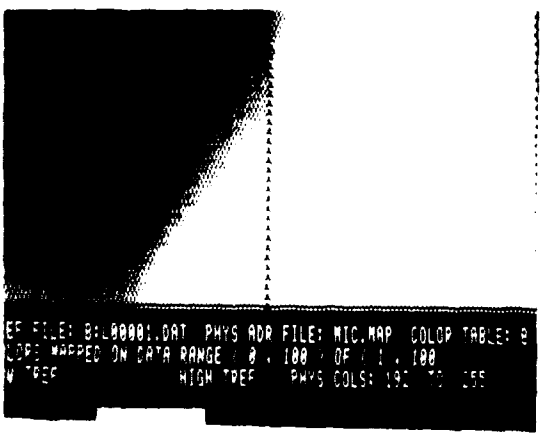
Figure A-4. Optical Map Verification Technique Displays - Vendor 1



a. Correct physical bit weights.

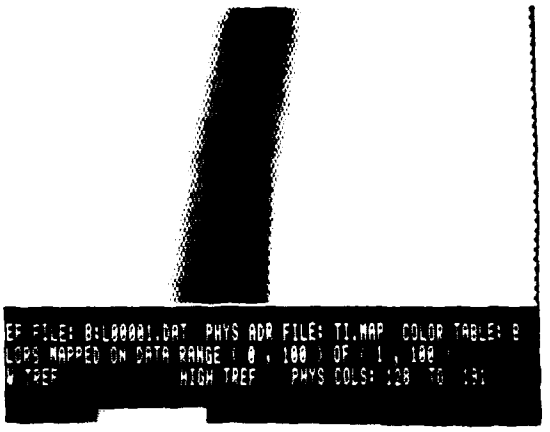


b. Weights of physical row bits B0 and B1 swapped.

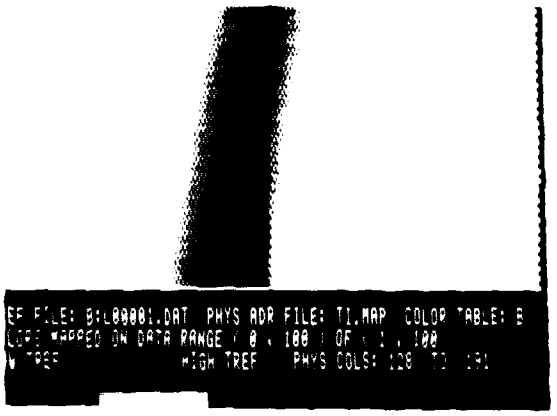


c. Weights of physical col bits B0 and B1 swapped.

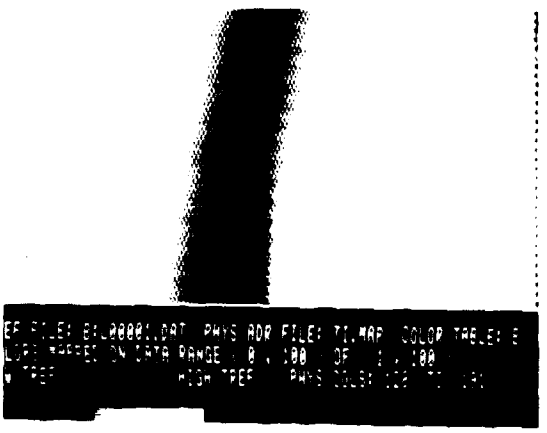
Figure A-5. Optical Map Verification Technique Displays - Vendor 2



a. Correct physical bit weights.

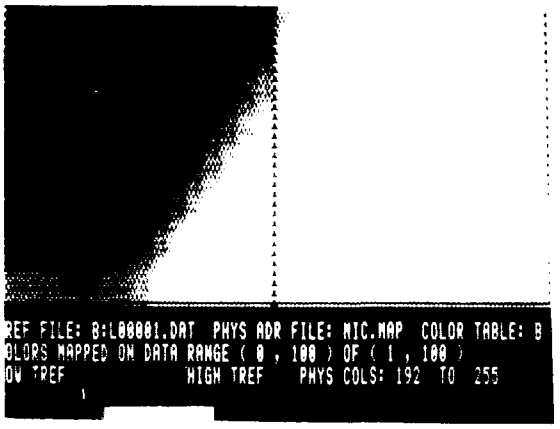


b. Weights of physical row bits B0 and B1 swapped.

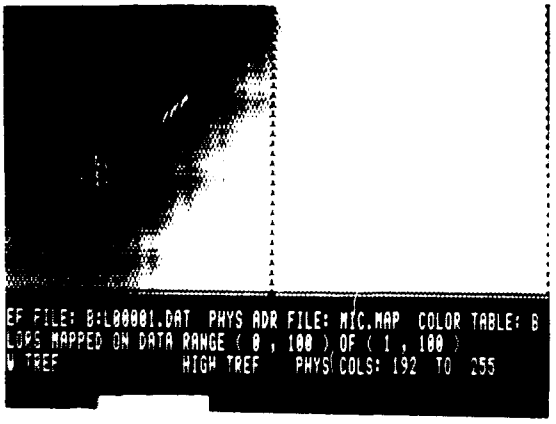


c. Weights of physical col bits B0 and B1 swapped.

Figure A-6. Optical Map Verification Technique Displays - Vendor 1

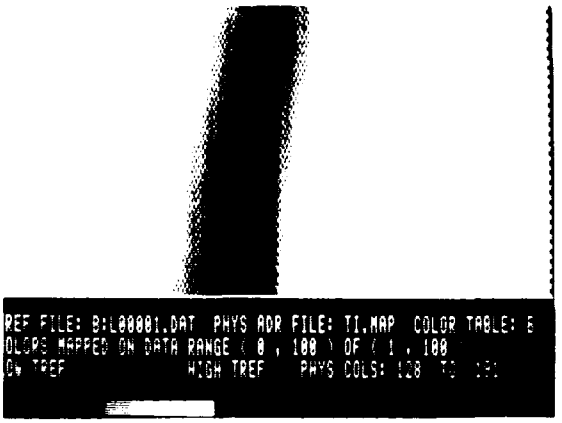


a. Weights of physical row bits B1 and B2 swapped.

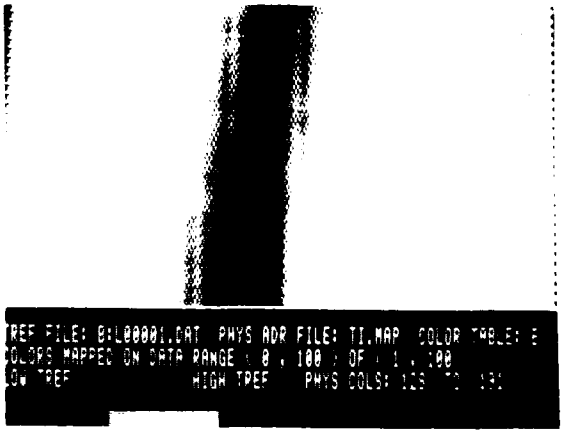


b. Weights of physical col bits B2 and B3 swapped.

Figure A-7. Optical Map Verification Technique Displays - Vendor 2

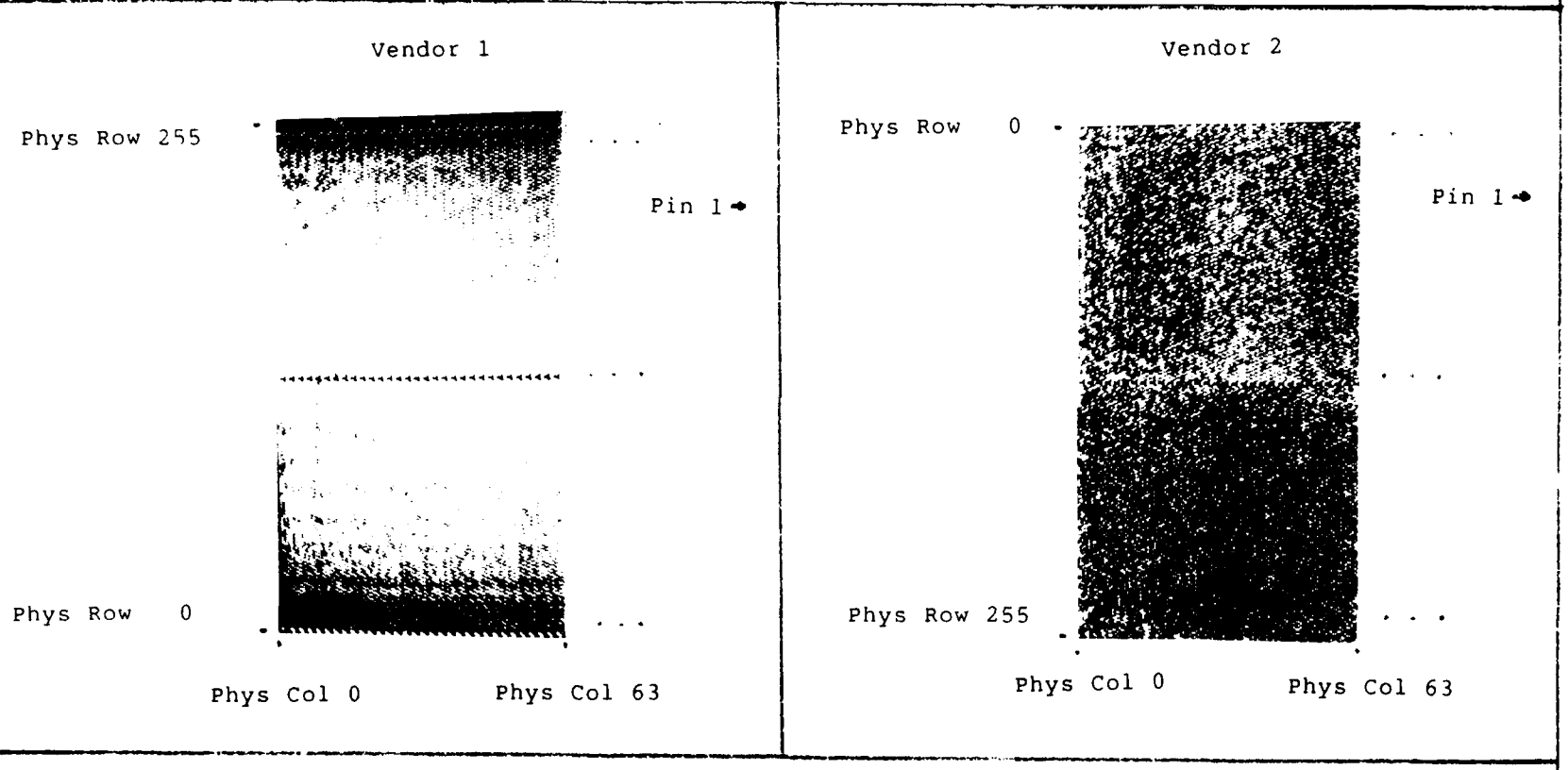


a. Weights of physical row bits B1 and B2 swapped.



b. Weights of physical col bits B2 and B3 swapped.

Figure A-8. Orientation of Physical Rows and Cols on Devices
and Typical Bit Mapped Refresh Time Images (See Notes 1,2,3)



Note 1: Refresh time is intensity mapped onto each pixel using a 3 bit linear gray scale.
Note 2: Histograms of refresh times show here are found in Figures 3-1 and 4-1 of this report.
Note 3: The locations of Rows 0 and 255 really are different for the two devices!

ACKNOWLEDGEMENTS

This work was done in-house in the Microelectronics Reliability Division at Rome Laboratory (RL/ERDR). Dan Burns contributed to background research, measurement hardware and software development, device testing, data analysis, SEM inspection, reporting, and illustrations. Wilmar Sifre contributed greatly to device testing, data analysis, device delayering, and SEM inspection. Fred Robenski provided valuable contributions to device delayering and SEM inspection. Dr. Mark Levi provided background research, the physical model discussion in Section 5.4, and continuous streams of ideas and encouragement throughout the project. Ed Doyle technically reviewed this report, and Marie St.Thomas and Lee Lazicki produced the manuscript. The samples were provided by the device manufacturers, via Doug Younkin, McDonnell Douglas Corp., St. Louis MO, who also provided independent verification of the Tref measurement technique as a sub-task to a follow-on DRAM screening contract. The authors also wish to thank Al Tamburrino, Joe Brauer, and Jack Bart for patiently supporting this internally funded in-house project, and at least two unnamed and unlucky summer engineering aide and cooperative education students involved in the early measurement work.

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