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Abstract

A type IIa natural diamond was implanted with boron to form a p-type channel layer. This layer was then used to fabricate an insulated gate field effect transistor. This is the first reported use of ion implantation to successfully fabricate a field effect device in diamond. Testing was carried out from room temperature to 550 K. Both saturation and pinch-off were observed at room temperature, with a measured transconductance of 6.9 μS/mm. Device failures at elevated temperatures were attributed to gate current leakage through the SiO_2 insulator layer.

INTRODUCTION

Semiconducting diamond is a promising material for high temperature electronic device applications due to its high electron and hole mobilities, high saturation velocity, wide energy band gap, high breakdown voltage, and the highest known thermal conductivity near room temperature. Significant progress has recently been reported in several key areas for the practical realization of diamond as an electronic material. Two examples of this progress are the demonstration of large area homoepitaxial films doped with boron, a major step toward the ultimate goal of single crystal films on substrates other than diamond, and the regrowth of radiation damaged layers in diamond created by ion implantation.

Several workers have previously fabricated transistor structures on diamond. Geis et al. (1991) has investigated the capacitance-voltage properties of metal-insulator-semiconductor structures on bulk type IIb natural diamonds. Gildenblat et al. (1989) and Shiomi et al. (1989) have independently demonstrated MEtal Semiconductor Field Effect Transistor (MESFET) devices. These were the first reports of planar type transistors using a diamond film. Gildenblat et al. (1991) have also demonstrated an Insulated Gate Field Effect Transistor (IGFET) structure in an effort to avoid the gate leakage problems common to MESFET devices. These devices all have in common the use of boron doped homoepitaxial diamond films. More recently, Tsai et al. (1991) have demonstrated a MESFET using a natural type IIa diamond with a p-doped channel created by solid state diffusion of boron in conjunction with rapid thermal processing. In this paper we discuss the use of ion implantation to create a p-doped channel region in naturally insulating (type IIa) diamond. We then discuss the fabrication and testing of an IGFET utilizing the ion implanted channel.

Prins (1988) proposed an implantation scheme consisting of a carbon implant at liquid nitrogen temperature followed immediately by boron implantation, also at liquid nitrogen temperature. The ion energies are chosen such that the projected range of the boron ions matches the depth of maximum damage created by the carbon implantation. Such an overlap, in conjunction with the low temperature, should place the boron ions in close proximity to lattice vacancies. The diamond is then removed from the implanter and annealed at 1273 K, thereby allowing some fraction of the boron atoms to occupy lattice sites. Measurement of the change in resistance in the diamond as a function of temperature (Prins 1988, and Sandhu et al. 1989) indicated an activation energy on the order of 0.3 eV, consistent with the activation energy determined for boron in naturally semiconducting (type IIb) diamond. De la Houssaye et al. (1990) also showed that boron alone implanted at liquid nitrogen temperature and subsequently annealed at 1273 K could also be activated. The efficiency of this approach relative to that of Prins (1988) is being studied further.

EXPERIMENTAL PROCEDURE

The starting material consisted of a natural semi-insulating (type IIa) diamond 5 mm x 5 mm x 0.25 mm in size. Boron ions were implanted at 77 K using a multiple implant scheme (25 keV, 1.5 x 10^{14} B^+/cm^2; 50 keV, 2.1 x 10^{14} B^+/cm^2; and 100 keV, 3.0 x 10^{14} B^+/cm^2) intended to provide an approximately uniformly doped p-type layer of about 210 nm in thickness. After implantation, the diamond was annealed at 1263 K in nitrogen to remove the implantation damage and activate the implanted boron. Following the activation anneal, the carrier concentration and mobility were determined by making a series of van der Pauw resistivity and Hall effect measurements as a function of temperature. The room temperature free carrier concentration was measured to be about 5 x $10^{15}/cm^3$, with a mobility of about 30 cm^2/V-s. The details of this measurement have previously been published by de la Houssaye et al. (1990).

The diamond was then cleaned by etching in a boiling saturated solution of chromic oxide (Cr_2O_3) in sulfuric acid. The purpose of the etch was to remove the electrical contacts (molybdenum/gold) used in the van der Pauw resistivity and Hall effect measurements, and to remove any damaged layer on the diamond surface. The device geometry (shown in Figure 1) was chosen to provide data without requiring a mesa etch. It consisted of a central drain contact 400 μm in diameter, with concentric 200 μm wide gate and source contacts 1000 μm and 1600 μm in outer diameter, respectively. All metallizations were deposited in an ultra-high vacuum system with a pressure during deposition of less than 7×10^{-8} Torr. The source and drain ohmic contacts were fabricated using a bilayer structure consisting of a 10 nm molybdenum film deposited on the diamond, with a 160 nm gold cap. The source and drain contacts were defined with a lift-off process. Following lift-off, the sample was baked at 393 K for 20 minutes in air and then annealed at 1223 K in a hydrogen ambient to form a carbide phase. The gate insulator, consisting of an SiO_2 film approximately 100 nm thick, was deposited by indirect plasma enhanced chemical vapor deposition at a temperature of 573 K. The gate metal was a 10 nm titanium/160 nm gold bilayer structure, also defined by a lift-off process. Titanium was chosen to improve the adhesion of the gate metallization to the gate insulator. The devices were tested at temperatures ranging from room temperature up to 550 K.

DISCUSSION AND CONCLUSIONS

In a previous study (de la Houssaye et al. 1990) we demonstrated that boron ions implanted at 77 K could be electrically activated to form a conducting layer in naturally insulating diamond. Further verification of this may be observed in the source to drain current-voltage characteristics shown in Figure 2. These characteristics were taken prior to deposition of the gate insulator and gate metallization.

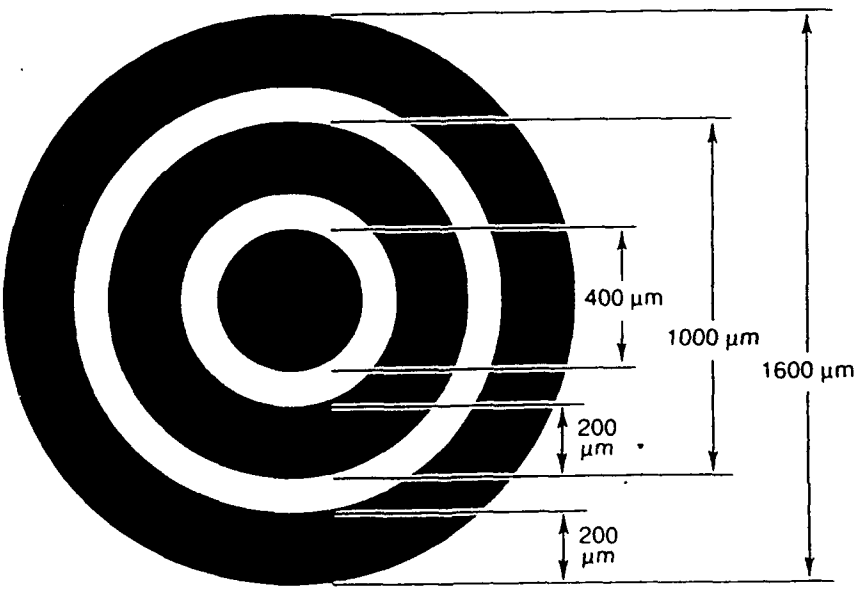

FIGURE 1. Schematic Outline of the IGFET Source (Outer Ring), Gate (Central Ring), and Drain (Center Dot) Contacts.

The transistor characteristics are shown in Figure 3. Current saturation is clearly observed, as is pinch-off at a gate bias of approximately 12 volts. We believe this to be the first observation of pinch-off in a diamond IGFET structure. The transconductance was measured to be 6.9 μS/mm. This is the highest reported value of any diamond device reported to date.

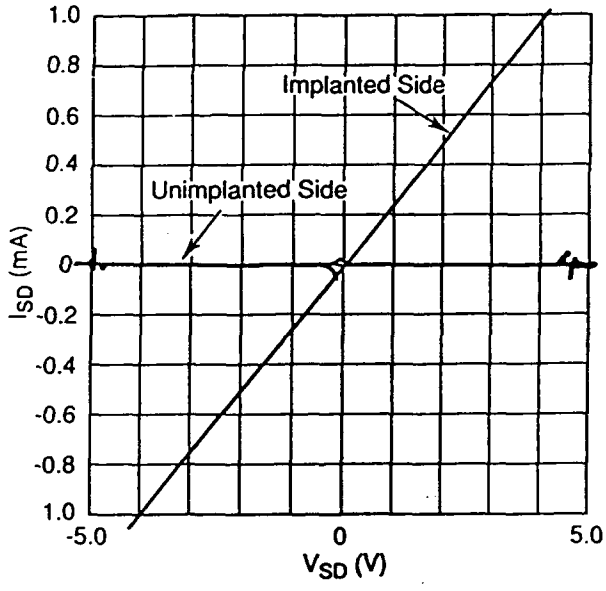

FIGURE 2. Room temperature Source to Drain Current-Voltage Characteristics at Zero Gate Bias on the Implanted and Unimplanted Sides of the Diamond.

The motivation behind the incorporation of an insulated gate structure is to eliminate the gate leakage problem observed in diamond MESFET fabrication. No detectable source to gate leakage current was observed at room temperature using a curve tracer. As the temperature increases, however, there is a significant increase in leakage current. This can also be observed in the 400 K transistor characteristics (Figure 4). We believe that this is the main cause for device failure as the temperature is increased beyond 400 K. We are currently attempting to improve the quality of the SiO_2 film used as the gate insulator.

The characteristics of this device may be improved by increasing the doping, both in the channel region and in the source and drain regions,or by reducing any residual radiation damage in the active layer. Increasing the channel doping should improve the transconductance and help to reduce the series resistance inherent in devices with this geometry. In addition, heavily doping the source and drain regions would help to reduce the source and drain contact resistance. We have shown previously (Hewett et al. 1990) that a significant improvement in specific contact resistance can be obtained by using a highly doped layer for contact formation. This may be carried out rather easily by using a separate ion implantation step for the source and drain contact areas. We are currently investigating device fabrication using such a process.

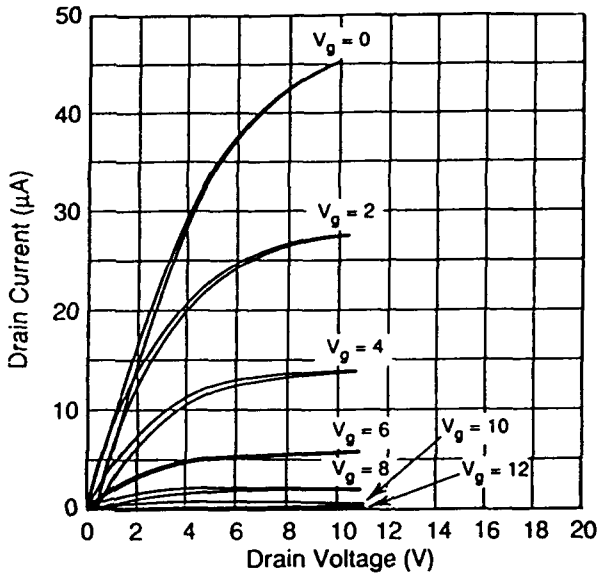

FIGURE 3. Drain Current versus Drain Voltage as a function of Gate Bias at Room Temperature.

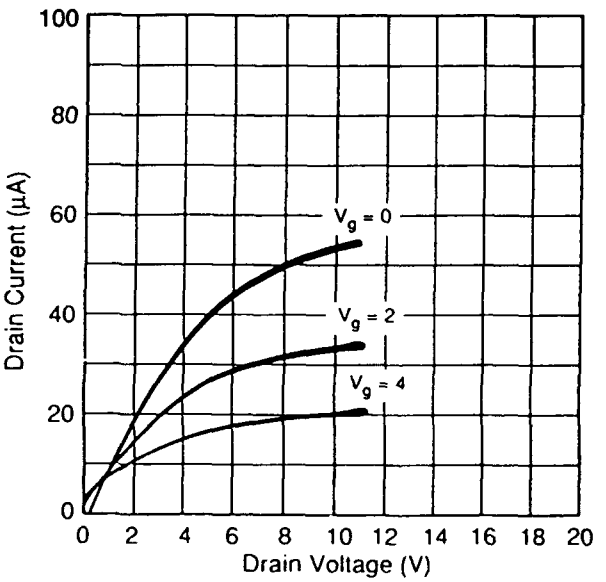

FIGURE 4. Drain Current versus Drain Voltage as a function of Gate Bias at 400 K.

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