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13. ABSTRACT (Maximum 200 words) This Rapid Acquisition of Manufactured Parts (RAMP) Product Data Translation System (RPTS) Printed Wiring Assembly (PWA) Product Data Definition Document (PDDD) establishes the digital standards and formats used in Technical Data Package (TDP) information for a PWA manufacturing facility.					
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LIST OF ACRONYMS

ANSI	American National Standards Institute
AP_SPEC	Component Applicable Specification
ASCII	American Standard Code for Information Interchange
BNF	Backus-Naur Format
BOM	Bill of Material
CAD	Computer Aided Design
CAE	Computer Aided Engineering
CCITT	Consultative Committee International Telegraph & Telephone
CHTYP_LT	Component Logic Type
CHTYP_NTL	Component Negative Tolerance
CHTYP_PTL	Component Positive Tolerance
CHTYP_VAL	Component Value
CLASS	Component Classification
COMP_PWR	Component Power
COTS	Commercial-Off-The-Shelf-Software
EDIF	Electronic Data Interchange Format
EIA	Electrical Institute Associate
FSCM	Federal Supply Code for Manufacturers
FSD	Formal Syntax Definition
GPN	Component Generic Part Name
IGES	Initial Graphics Exchange Specification
IPC	Institute for Interconnecting and Packaging Electronic Circuits
IPO	IGES/PDES Organization
ISF	Industry Standard File
ITEM	Component Item Number
LEAD_MAT	Component Lead Material
LEAD_PLT	Component Lead Plating
MAX_WRK_VOLT	Component Maximum Working Voltage
ME	Manufacturing Engineering
MIL	Military
PCB	Printed Circuit Board
PDDD	Printed Data Definition Document
PDES	Product Data Exchange Using STEP
PKG	Component Package
PN	Component Part Number
PTYPE	Component Part Type
PWA	Printed Wiring Assembly
PWB	Printed Wiring Board
QNTY	Component Quantity
RAMP	Rapid Acquisition of Manufactured Parts
RDES	Reference Designator
REV	Component Revision Level
RPTS	RAMP Product Data Translation System
SCRA	South Carolina Research Authority

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LIST OF ACRONYMS (CONT'D)

SI	System International
SOLDERABILITY	Component Lead Solderability
STD	Standard
SUB	Component SubClassification
TDP	Technical Data Package
3D	Three Dimensional
2D	Two Dimensional

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SECTION 1.0

1.1 SCOPE

This Rapid Acquisition of Manufactured Parts (RAMP) Product Data Translation System (RPTS) Printed Wiring Assembly (PWA) Product Data Definition Document (PDDD) establishes the digital standards and formats used in Technical Data Package (TDP) information for a PWA manufacturing facility.

1.2 Purpose

The purpose of the RPTS PWA PDDD is to provide a complete description of the RAMP Product Data File Set which uses industry standards to carry PWA product data.

1.3 Introduction

The information required to manufacture a PWA can be grouped into the following major areas and are referenced in the adjoining sections:

<u>MAJOR AREA</u>	<u>REFERENCE SECTION</u>
Schematic	3.1 Schematic Electrical Functional Product Data
Assembly	3.3 3D Assembly Product Data
Bill-of-Material	3.1.8 EDIF RAMP Test Entities
Test Requirements	3.1.8 EDIF RAMP Test Entities
	3.4 Raster Data
Artwork	3.2 PWB Product Data
Component Source	3.4 Raster Data
Control	
Component Spec-	3.4 Raster Data
ification control	
MIL standards	3.4 Raster Data

1.4 Application

The files produced using this specification will provide sufficient PWA product data to support the RAMP PWA factory. Electronic Data Interchange Format (EDIF), Institute for Interconnecting & Packaging of Electronic Circuits (IPC),

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Initial Graphics Exchange Specification (IGES), and Consultative Committee of International Telegraph & Telephone (CCITT) are used by RPTS PWA to deliver data to support the RAMP PWA factory (see Table 1-1). EDIF is used to deliver the PWA schematic and component property data; IPC is used to deliver Printed Wiring Board (PWB) artwork and other Two Dimensional (2D) PWB data; and IGES is used to deliver PWA Three Dimensional (3D) assembly and component data.

TABLE 1-1

PRODUCT DATA AND RELATED STANDARDS

<u>PRODUCT DATA TYPE</u>	<u>EDIF</u>	<u>IGES</u>	<u>IPC</u>	<u>CCITT GP 4</u>
SCHEMATIC	X			X
BARE PWB		X	X	X
AS RECEIVED COMPONENT		X		X
ASSEMBLY		X		X
TEST REQUIREMENTS	X			X
COMPONENT SOURCE CONTROL				X
COMPONENT DETAIL SPEC.				X

1.5 Terms and Abbreviations

Schematic. An electrical or logical schematic contains graphical component symbols representing the components within a PWA, connection point symbols representing component electrical connection ports, interconnecting lines representing electrical interconnects or nets between the components and other system assemblies, and American Standard Code for Information Interchange (ASCII) text representing component properties attribute names and values.

Orientation Vector. The orientation vector is a line segment placed in the body of a 3D component model can be used to determine the orientation of the component when the component is placed in the 3D assembly model.

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SECTION 2.0 APPLICABLE DOCUMENTS

Government Documents

Unless otherwise specified, the following specifications and standards of the issue listed shall form a part of this specification to the extent specified herein.

SPECIFICATIONS:

MIL-D-28000 Digital Representation for Communication of Product Data
MIL-R-28002 Rasters Graphics Representations in Binary Format, Requirements
for

STANDARDS:

MIL-STD-1840 Automated Interchange of Technical Information
MIL-STD-275 Printed Wiring for Electronic Equipment

HANDBOOKS:

MIL-HDBK-59 CALS Program Implementation Guide

INDUSTRY STANDARDS DOCUMENTS:

ANSI/EIA RS548 EDIF 2 0 0 Electronic Data Interchange Format
ANSI/IPC-D-350 IPC Printed Board Description in Digital Form
ANSI/IPC-D-353 IPC Test Standard
ANSI/IGES IGES 4.0/5.0 Initial Graphics Exchange Specification
ANSI/EIA 538 CCITT GROUP 4 Consultative Committee of International
Telegraph & Telephone on Raster Data Communication and
Compression

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SECTION 3.0

RAMP PWA PRODUCT DATA DEFINITION

3.1 Schematic Electrical Functional Product Data

EDIF 2 0 0, which is American National Standards Institute (ANSI)/Electrical Institute Associate (EIA) RS548, is used to supply the electrical schematic and component information to the RAMP PWA factory. This is made possible by the RPTS data capture system and RAMP PWA Manufacturing Engineering (ME) Computer Aided Design (CAD) and Computer Aided Engineering (CAE) system support EDIF 2 0 0 Schematic View. The schematic, electrical attributes, and component values are used by the factory to facilitate automation of test generation and fixturing as shown in Figure 3-1. The attribute list for electrical properties shall be transferred to the factory in EDIF format and uses keyword attributes from IGES 5.0, IPC-D-353, and RAMP.

3.1.1 EDIF Cells

The EDIF standard uses a cellular structure which represents the PWA schematic as one cell and its constituent subassembly components as cells within the main PWA cell. There are three EDIF cell type attributes used in RAMP which define the use of a cell: generic, tie, and ripper as follows:

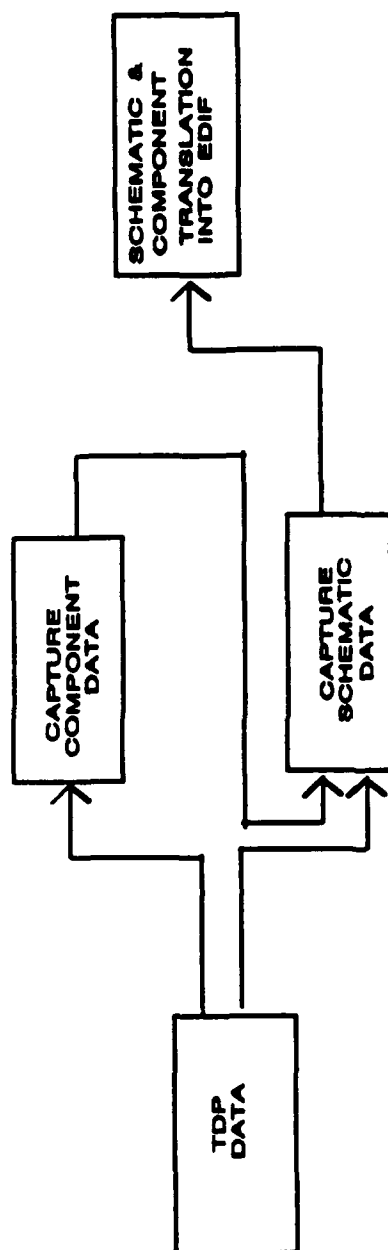
The generic cell type is used for defining a component or whole assembly.

The tie cell type is used in explicitly joining subnets with nets.

The ripper cell type is used to explicitly merge nets with different names, and make changes to nets which may occur in the contents or page constructs.

3.1.2 EDIF Views

Each CELL whether referencing the whole assembly or an individual component on the assembly could have ten different VIEWS of the CELL as modeled in EDIF but only the "Schematic" and "Netlist" views are used by RAMP.



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FIGURE 3-1 EDIF SCHEMATIC & COMPONENT DATA

3.1.2.1 View Interface

Within the EDIF views, there is an interface entity to define the cell interaction within its external environment. The following constructs are legal and defined in EDIF for interface.

- interface
- a. port
- b. portbundle
 - (1) symbol
 - (2) protectionFrame
 - (3) arrayRelatedInfo
- c. parameter
- d. joined
- e. mustJoin
- f. weakJoined
- g. permutable
- h. timing
- i. simulate
 - designator
- j. property
- k. comment
- l. userData

3.1.2.2 View Contents

The optional contents entity defines internal details of a view. The entity is used as required for each cell to provide comment, property and user data statements to describe the components for the applications supported. The contents section of EDIF details the implementation of a view and uses the following constructs as defined in EDIF 2 0 0:

- a. instance
- b. offpageconnector
- c. figure
- d. section
- e. net
- f. netbundle
- g. page
- h. commentGraphics
- i. portImplementation
- j. timing
- k. simulate
- l. when
- m. follow
- n. logicPort

boundingBox
o. userData

3.1.2.3 ViewMap

ViewMap is used in EDIF to express relationships between objects of the same type in different views, but is not supported in RAMP PWA.

3.1.3 EDIF Level

EDIF has three levels 0, 1, and 2 which allow passing data, with progressively more complex numeric representations possible with the higher level. Level 0 is used in RAMP PWA.

3.1.4 EDIF Technology

The technology of the components used in the PWA is defined in EDIF by the Technology entity. The Technology entity contains data on scaling, basic figure groups, and display formats. The EDIF graphic units are in System International (SI) which is a metric convention.

3.1.5 EDIF Libraries

The cells used in EDIF are grouped into libraries based on common characteristics. Besides the three basic cells found in the library there are also edif level and technology data.

3.1.6 EDIF Object Relationships

In EDIF, relationships between objects are expressed by name reference and containment.

3.1.6.1 Name Relationships

SUPPORTED EDIF NAME

<u>CLASS</u>	<u>SCOPING CONSTRUCT</u>
cellName	external, library
designName	edif
edifFileName	no scope
figureGroupName	library
instanceName	net, page, view
libraryName	edif
netName	net, netbundle, page, view
portName	portbundle, simulate, view
propertyName	containing form
ruleName	library
simulateName	view
valueName	block, external, library, page, view
viewName	cell

3.1.6.2 Containment Relationships

Parentheses are used to group data concerning a particular object. For example:

```
(property PTYPE
  (string "SSI")
  (owner "Intergraph"))
```

3.1.7 EDIF FigureGroups

FigureGroups are the basic entity used for describing sets of geometry such as schematic symbols or text.

3.1.8 EDIF RAMP Test Entities3.1.8.1 Component Part Type (PTYPE)

The PTYPE attribute indicates the part type assigned to a part or component of a PWA. PTYPE is also referenced in IPC-D-353, a draft test standard for data communication. The PTYPE attribute is used in incircuit test systems to select the type of test to generate for discrete analog components. The value of PTYPE is a alpha numeric string not to exceed 15 characters in length with the formal syntax shown in Appendix I. The following part types are reserved for PTYPE use:

<u>Name</u>	<u>Meaning</u>
ANA	ANALOG INTEGRATED CIRCUIT
BIZ	BIZENER
CAP	CAPACITOR
CSW	CLOSED SWITCH
CUST	CUSTOM INTEGRATED CIRCUIT
DAR	DARLINGTON TRANSISTOR
DIO	DIODE
DIPCAP	DIP CAPACITOR
EDG	EDGE CONNECTOR
FET	FIELD EFFECT TRANSISTOR
FUS	FUSE
HYB	HYBRID
IND	INDUCTOR
JUM	JUMPER
LED	LIGHT EMITTING DIODE
LSI	LARGE SCALE INTEGRATION
MSI	MEDIUM SCALE INTEGRATION
OPJ	OPEN JUMPER
OSW	OPEN SWITCH
PCA	POLARIZED CAPACITOR
PIS	PACKAGING/INTERCONNECTING STRUCTURE

POT	POTENTIOMETER
PWB	PRINTED WIRING BOARD
RCL	RELAY COIL
RCNO	RELAY CONTACT NORMALLY OPEN
RCNC	RELAY CONTACT NORMALLY CLOSED
RES	RESISTOR
RHE	RHEOSTAT
RP_DB	RESISTOR PACK DIP BUSSED
RP_DH	RESISTOR PACK DIP HYBRID
RP_DI	RESISTOR PACK DIP ISOLATED
RP_DT	RESISTOR PACK DIP TERMINATED
RP_SB	RESISTOR PACK SIP BUSSED
RP_SH	RESISTOR PACK SIP HYBRID
RP_SI	RESISTOR PACK SIP ISOLATED
RP_ST	RESISTOR PACK SIP TERMINATED
SCR	SILICON CONTROLLED RECTIFIER
SSI	SMALL SCALE INTEGRATION
TCA	TANTALUM CAPACITOR
TPCP	TWO PART CONNECTOR PIN
TPCS	TWO PART CONNECTOR SOCKET
TRAS	TRANSFORMER SIGNAL
TRAP	TRANSFORMER POWER
TRNN	TRANSISTOR NPN
TRNP	TRANSISTOR PNP
UNI	UNIUNCTION TRANSISTOR
VHSIC	VERY HIGH SPEED INTEGRATED CIRCUIT
VLSI	VERY LARGE SCALE INTEGRATION
XTL	CRYSTAL
ZDI	ZENER DIODE

Example of usage in the EDIF file after translation:

```
(property PTYPE  
(string "SSI")  
(owner "Intergraph"))
```

3.1.8.2 Reference Designator (RDES)

The RDES attribute indicates the specific reference designator assigned to a part or component of a PWA. RDES is also referenced in IPC-D-353. The RDES attribute is used in incircuit test systems to identify faulty components. The formal syntax is given in Appendix I.

<RDES> (U5)

Example of usage in the EDIF file after translation:

```
(property RDES  
(string "U5")  
(owner "Intergraph"))
```

3.1.8.3 Component Value (CHTYP_VAL)

The CHTYP_VAL attribute indicates a general value characteristic assigned to a part or component such as a resistor, capacitor, or inductor. CHTYP and VAL are also referenced in IPC-D-353. The CHTYP_VAL attribute is used in incircuit test systems to set up the analog measurement range. The formal syntax is given in Appendix I.

The percent sign "%" and units of the value are not allowed in the value field.

Example of usage in the EDIF file after translation:

```
(property CHTYP_VAL
  (string (stringdisplay "2.2K"
    (display
      (figuregroupoverride TEXT1_GROUP
        (visible (false))
        (justify UPPERLEFT)
        (orientation R0)
        (origin (pt 128600 61850))))))
  (owner "Intergraph"))
```

3.1.8.4 Component Positive Tolerance (CHTYP_PTL)

The CHTYP_PTL attribute indicates the positive tolerance characteristic of the nominal value assigned to a part or component of a PWA. The tolerance is given as percentage of the general value. CHTYP and PTL are also used in IPC-D-353, a draft standard for data communication. The CHTYP_PTL attribute is used in incircuit test systems to convey the positive tolerance used to determine if an analog part passes or fails the test. The percent sign "%" is not allowed in the value field. The formal syntax is given in Appendix I.

Example of usage in the EDIF file after translation:

```
(property CHTYP_PTL
  (string (stringdisplay "5"
    (display
      (figuregroupoverride TEXT1_GROUP
        (visible (false))
        (justify UPPERLEFT)
        (orientation R0)
        (origin (pt 128600 63050))))))
  (owner "Intergraph"))
```

3.1.8.5 Component Type Negative Tolerance (CHTYP_NTL)

The CHTYP_NTL attribute indicates the negative tolerance characteristic of the nominal value assigned to a part or component of a PWA. The tolerance is given as a percentage of the general value. CHTYP and NTL are also used IPC-D-353, a test standard for data communication. The CHTYP_NTL attribute is used in incircuit test systems to convey the negative tolerance used to determine if an analog part passes or fails the test. The percent sign "%" and minus sign are not allowed in the value field. The formal syntax is given in Appendix I.

Example of usage in the EDIF file after translation:

```
(property CHTYP_NTL
  (string (stringdisplay "5"
    (display
      (figuregroupoverride TEXT1_GROUP
        (visible (false)))
        (justify UPPERLEFT)
        (orientation R0)
        (origin (pt 128600 62450))))))
  (owner "Intergraph"))
```

3.1.8.6 Component Generic Part Name (GPN)

The GPN attribute indicates a generic part name attribute assigned to a part or component of a PWA. The GPN is located in the schematic near or on the component symbol. The GPN is used in Incircuit test to select the generic library test model of a component. The formal syntax is shown in Appendix I.

Example of usage in the EDIF file after translation:

```
(property GPN
  (string "5476")
  (owner "Intergraph"))
```

3.1.8.7 Component Logic Type (CHTYP_LT)

The CHTYP_LT attribute indicates a logic type characteristic assigned to a part or component of a PWA. IPC-D-353 is a supporting reference for this definition. The CHTYP_LT is used in Incircuit test to select the analog or digital generic test model library. The formal syntax is given in Appendix I.

The following part types are reserved for CHTYP_LT use:

<u>Name</u>	<u>Meaning</u>
ALU	Arithmetic logic Unit
ANA	Analog
CLK	Clock Generator
CNT	Counter
COM	Combinatorial Logic
DMUX	Demultiplexer
DRAM	Used for Dynamic RAMs
HYB	Hybrid
MUX	Multiplexer
PIO	Programmable I/O
PLD	Programmable Logic Device
RAM	Memory Devices
ROM	Read Only Memory
SEQ	Sequential Logic
SRAM	Used for Static RAMs (Random Access Memory)

Example of usage in the EDIF file after translation:

```
(property CHTYP_LT
(string "SEQ")
(owner "Intergraph"))
```

3.1.8.8 Component Applicable Specification (AP_SPEC)

The Applicable Specification Number attribute indicates the specification document number that describes the component. The AP_SPEC is located in the TDP Bill of Material (BOM)/Parts List in column 13 as defined by DOD-STD-100C. The formal syntax is given in Appendix I.

Example of usage in the EDIF file after translation:

```
(property AP_SPEC
(string "MIL-R 39008/1")
(owner "Intergraph"))
```

3.1.8.9 Component Part Number (PN)

The Part Number attribute indicates the part number which identifies the component. The PN is located in the TDP BOM/Parts List in column 14 as defined by DOD-STD-100C. The formal syntax is given in Appendix I.

Example of usage in the EDIF file after translation:

```
(property PN
(string "RCR07G222JM")
(owner "Intergraph"))
```

3.1.8.10 Component Item Number (ITEM)

The Item Number attribute indicates the item number which is uniquely assigned to a component part number in a design as an internal identification number.

The Item number is located in the TDP BOM/Parts List in column 9 as defined by DOD-STD-100C. The formal syntax is given in Appendix I.

Example of usage in the EDIF file after translation:

```
(property ITEM  
  (string "38")  
  (owner "Intergraph"))
```

3.1.8.11 Commercial And Government Entity Code (CAGE)

The CAGE Identification Code attribute indicates the Identification Code assigned to the design activity who made the component. The CAGE is located in the TDP BOM/Parts List in column 12 as defined by DOD-STD-100C. The formal syntax is given in Appendix I.

Example of usage in the EDIF file after translation:

```
(property CAGE  
  (string "10001")  
  (owner "Intergraph"))
```

3.1.8.12 Component Classification (CLASS)

The Component Classification is a component attribute which divides different components into one of 12 basic classes used in manufacturing. The formal syntax is given in Appendix I. CLASS is a South Carolina Research Authority (SCRA) developed classification system. The component classes are listed below in Table 3-1:

TABLE 3-1
COMPONENT CLASSIFICATION

<u>CLASS</u>	<u>MEANING</u>
BATTE	BATTERY
CAP	CAPACITOR
CHEM	CHEMICAL
CON	CONDUCTOR
CORE	CORE
HDWR	HARDWARE
IND	INDUCTOR
LAMP	ILLUMINATORS
PWB	PRINTED WIRING BOARD
RES	RESISTOR
ROTMA	ROTATING MACHINERY
SEMI	SEMICONDUCTOR
SWTCH	SWITCH_RELAY

TABLE 3-1 (CONT'D)
COMPONENT CLASSIFICATION

<u>CLASS</u>	<u>MEANING</u>
TRADU	TRANSDUCER
UCT	MICROCIRCUIT
XFMR	TRANSFORMER

Example of usage in the EDIF file after translation:

```
(property CLASS
 (string "PWB")
 (owner "Intergraph"))
```

3.1.8.13 Component SubClassification (SUB)

The Component SubClassification is a component attribute which divides different components classifications into subclassifications. Each of the 12 basic classes has its own group of subclasses. The formal syntax is given in Appendix I. SUB is a SCRA developed subclassification system. The component subclasses are listed in Table 3-2.

TABLE 3-2
COMPONENT SUB-CLASSIFICATION

<u>CLASS</u>	<u>SUB</u>	<u>MEANING</u>
BATTE	NONR	Nonrechargeable
	RECH	Rechargeable
CAP	FIXED	Fixed Value Capacitor
	VAR	Variable Value Capacitor
CHEM	BAGT	Bonding Agent
	CAGT	Compound Agent
	CLAGT	Cleaning Agent
	IAGT	Insulating Agent
	MAGT	Marketing Agent
	TAGT	Thermal Agent
	ANTEN	Antenna
CON	BUSBR	Busbar
	EDGE	Edge Connector
	FUSE	Fuse
	JUM	Jumper
	OPJ	Open Jumper
	COAX	Coaxial Cable
	WAVG	Waveguide
	PLUG	Connector Plug
	RECPT	Connector Receptacle
	EDGE	Edge Connector
	TERM	Terminal Connector
	TP	Test Point
	KEY	Keyed Connector
CORE	ADAPT	Adaptor Connector
	FEBED	Ferrite Bead Core
HDWR	BOLT	Bolt

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TABLE 3-2 (CONT'D)
COMPONENT SUB-CLASSIFICATION

<u>CLASS</u>	<u>SUB</u>	<u>MEANING</u>
	BRACK	Bracket
	BRVT	Blind Rivet
	CLAMP	Clamp
	CRVT	Countersink Rivet
	CLIP	Clip
	EJECT	Ejector
	EYELE	Eyelet
	FRAME	Frame
	FWSHR	Flat Washer
	LWSHR	Lock Washer
	HANDL	Handle
	LOBAR	Locking Bar
	PUBAR	Pull Bar
	INSUL	Disk Insulator
	PAD	Pad Insulator
	PLATE	Plate Insulator
	WASHR	Washer Insulator
	NUT	Nut
	PIN	Alignment Pin
	SPRIN	Spring Pin
	RRING	Retaining Ring
	TIES	Ties
	TRVT	Tubular Rivet
	SCREW	Screw
	SHIEL	Shield
	SLEEV	Sleeve
	SPACE	Spacer
	SPREA	Spreader
	SPRIN	Spring
IND	FIXED	Fixed Value Inductor
	VAR	Variable Value Inductor
LAMP	FLOUR	Fluorescent

TABLE 3-2 (CONT'D)
COMPONENT SUBCLASSIFICATION

<u>CLASS</u>	<u>SUB</u>	<u>MEANING</u>
PWB	GLOW	Glow Cold Cathode Lamp
	INCAN	Incandescent
	BALLA	Ballast Lamp
	FLEX	Flexible Printed Wiring Board
	HYB	Hybrid Printed Wiring Board
	MOLD	Molded Printed Wiring Board
RES	RFLEX	Reflex Printed Wiring Board
	RIGID	Rigid Printed Wiring Board
	FIXED	Fixed Resistor
	VAR	Variable Resistor
ROTMA	ACMAC	AC Rotating Machinery
	DCMAC	DC Rotating Machinery
SEMI	SYNCH	Synchronous
	DIODE	Diode
	SCR	Silicon Controlled Rectifier
SWTCH	TRANS	Transistor
	RELAY	Relay Switch
	SWTCH	Switch
TRADU	BELL	Bell Transducer
	HALL	Hall Effect Transducer
	MIC	Microphone Transducer
	SPK	Speaker Transducer
UCTT	XTL	CRYSTAL Transducer
	DIG	Digital Microcircuit
	HYB	Hybrid or Custom Microcircuit
	LIN	Analog Microcircuit
XFMR	MIXED	Mixed Analog/Digital Microcircuit
	POWER	Power Transformer
	SIGNAL	Signal Transformer

Example of usage in the EDIF file after translation:

```
(property SUB
(string "TMSTR")
(owner "Intergraph"))
```

3.1.8.14 Component Package (PKG)

The PKG is a component attribute which divides different component package styles into one of 12 basic classes used in manufacturing. The formal syntax is given in Appendix I. PKG is a SCRA developed package classification system. The component PKG types are listed in Table 3-3.

TABLE 3-3 Component Package	
<u>PKG</u>	<u>MEANING</u>
TYPE1	Single Layer PWB
TYPE2	Double Layer PWB
TYPE3	Multilayer without blind or buried vias
TYPE4	Multilayer with blind or buried vias
TYPE5	Multilayer metal core w/o blind or buried vias
TYPE6	Multilayer metal core with blind or buried vias
AXIAL	Package with Axial Leads
RDL	Package with Radial Leads
FP	Flat Package
SIP	Single In Line Package
DIP	Dual In Line Package
CHIP	Surface Mount Chip
CAN	Metal Encapsulated
LCC	Leadless Chip Carrier
JCC	J Bend Leaded Chip Carrier
GCC	Gull Winged Chip Carrier
PGA	Pin Grid Array
COB	Chip On Board
TAB	Tape Automated Bonding
SOIC	Small Outline Integrated Circuit
BOTTL	Bottle
DRUM	Drum
TUBE	Tube
TOROI	Toroid

Example of usage in the EDIF file after translation:

```
(property PKG
(string "SOIC")
(owner "Intergraph"))
```

3.1.8.15 Component Maximum Working Voltage (MAX_WRK_VOLT)

The MAX_WRK_VOLT property is a component's maximum rated working voltage. Acceptable entries are positive values (for example 100, .5) in volts.

Example of usage in the EDIF file after translation:

```
(property MAX_WRK_VOLT
  (string "25")
  (owner "Intergraph"))
```

3.1.8.16 Component Power (COMP_PWR)

The COMP_PWR property is a component's power rating. COMP_PWR is a SCRA developed classification attribute. Acceptable entries are positive values (for example: ".25", "500") in watts.

Example of usage in the EDIF file after translation:

```
(property COMP_PWR
  (string ".25")
  (owner "Intergraph"))
```

3.1.8.17 Component Lead Solderability (SOLDERABILITY)

The SOLDERABILITY property indicates whether a component can be wave soldered or reflow soldered. SOLDERABILITY is a SCRA developed classification attribute. The component specification defines solderability. The acceptable entries are "NIL", "NRFO", "NOWAV", and "NWRF".

Example of usage in the EDIF file after translation:

```
(property SOLDERABILITY
  (string "NRFO")
  (owner "Intergraph"))
```

3.1.8.18 Component Lead Material (LEAD_MAT)

The component lead material property provides the lead composition. LEAD_MAT is a SCRA developed classification attribute. The acceptable entries are "STL" or "OTH".

Example of usage in the EDIF file after translation:

```
(property LEAD_MAT
  (string "STL")
  (owner "Intergraph"))
```

3.1.8.19 Component Lead Plating (LEAD_PLT)

The component lead plating property indicates whether gold was used to plate the leads of a component. LEAD_PLT is a SCRA developed classification attribute. The acceptable entries are "GLD" or "OTH".

Example of usage in the EDIF file after translation:

```
(property LEAD_PLT
(string "GLD")
(owner "Intergraph"))
```

3.1.8.20 Component Quantity (Qty)

The Qty attribute indicates quantity of a component used per instance. The formal syntax is given in Appendix I. The QNTY is derived from the BOM information on quantity of a piece part, one item (1), Not Specified (NS), As Required (AR). QNTY is a SCRA developed classification attribute.

Example of usage in the EDIF file after translation:

```
(property QNTY
(string "AR")
(owner "Intergraph"))
```

3.1.8.21 Component Revision Level (REV)

The REV attribute indicates alpha numeric phrase entered to describe the component revision level. The formal syntax is given in Appendix I. REV is a SCRA developed classification attribute. The REV is located in the component specifications.

Example of usage in the EDIF file after translation:

```
(property REV
(string "A")
(owner "Intergraph"))
```

3.1.8.22 Quantity Unit (QUNIT)

The Qty Unit (QUNIT) attribute indicates unit of quantity of a component used per instance. The formal syntax is given in Appendix I. The QUNIT is derived from the BOM information on quantity of a piece part, each (EA), inches (IN), feet (FT), ounces (OZ), pound (LB), centimeter (CM), kilometer (KM), millimeter (MM), liter (L), pint (PT), quart (QT), gallon (GAL).

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QUNIT is a SCRA developed classification attribute.

Example of usage in the EDIF file after translation:

```
(property QUNIT  
(string "IN")  
(owner "Intergraph"))
```

3.1.9 EDIF File

The EDIF capture file is job.edf and is found in the 1840 header record:
"dstdocid: ".

3.2 Printed Wiring Board

The 2D layout, commonly referred to as PWB data, is the data required to fabricate the PWB and is supplied to a RAMP PWA factory using IPC-D-350 and IGES files. The data describe the traces and component pad shapes, and their locations for each layer of the board. The X,Y coordinate locations for pads and holes on the board are included. Any fabrication information concerning board dimensions, material, composition, and tolerances is included. The fabrication drawings are also included in Raster form from the original TDP. The PWB information as shown in Figure 3-2 is translated into IPC-D-350.

3.2.1 IPC Entity Usage

The IPC-D-350 operations codes that are used by RAMP Product Data descriptions of the PWB are described in the following paragraphs.

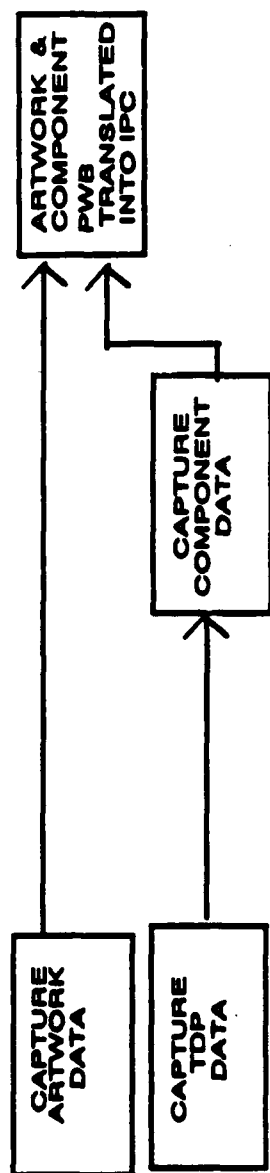
3.2.1.1 General Records

The following IPC-D-350 operations codes are used by RAMP product data:

IPC OPERATIONS CODES	DESCRIPTION
000	Continuation in Present Mode
999	End of Job

3.2.1.2 Line Records

The following IPC-D-350 line records operations codes are used by RAMP product Data:



0140KB

FIGURE 3-2 IPC PWB DATA

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IPC OPERATIONS CODES

DESCRIPTION

111	Begin New Line using Linear Interpolation and Position Data formatted as three adjacent X and Y fields
112	Begin New Line using Linear Interpolation and Position Data formatted as two adjacent X and Y fields
113	Begin New Line using Linear Interpolation and Position Data formatted as two adjacent XYZ fields
114	Begin New Line using Linear Interpolation and Position Data formatted as one set of XYZ fields
121	Begin New Line using Circular interpolation and Position Data formatted as three adjacent X and Y fields
122	Begin New Line using Circular interpolation and Position Data formatted as two adjacent X and Y fields
123	Begin New Line using Circular interpolation and Position Data formatted as two adjacent XYZ fields
124	Begin New Line using Circular interpolation and Position Data formatted as one set of XYZ fields
141	Begin New Line using Linear "paint in" area out line and Position Data formatted as three adjacent X and Y fields
142	Begin New Line using Linear "paint in" area out line and Position Data formatted as two adjacent X and Y fields
143	Begin New Line using Linear "paint in" area out line and Position Data formatted as two adjacent XYZ fields
144	Begin New Line using Linear "paint in" area out line and Position Data formatted as one set of XYZ fields

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- 151 Begin New Line using Circular part outline and
 Position Data formatted as three adjacent X and Y
 fields
- 152 Begin New Line using Circular part outline and
 Position Data formatted as two adjacent X and Y
 fields
- 153 Begin New Line using Circular part outline and
 Position Data formatted as two adjacent XYZ
 fields
- 154 Begin New Line using Circular part outline and
 Position Data formatted as one set of XYZ fields
- 171 Begin New Line using Linear part outline and
 Position Data formatted as three adjacent X and Y
 fields
- 172 Begin New Line using Linear part outline and
 Position Data formatted as two adjacent X and Y
 fields
- 173 Begin New Line using Linear part outline and
 Position Data formatted as two adjacent XYZ
 fields
- 174 Begin New Line using Linear part outline and
 Position Data formatted as one set of XYZ fields
- 181 Begin New Line using Circular part outline and
 Position Data formatted as three adjacent X and Y
 fields
- 182 Begin New Line using Circular part outline and
 Position Data formatted as two adjacent X and Y
 fields
- 183 Begin New Line using Circular part outline and
 Position Data formatted as two adjacent XYZ
 fields
- 184 Begin New Line using Circular part outline and
 Position Data formatted as three XYZ fields

3.2.1.3 Subroutine Definition Records

The following IPC-D-350 subroutine definition operations codes are used by RAMP product Data:

IPC OPERATIONS CODES	DESCRIPTION
211	Begin subroutine definition using a complex feature and Position Data formatted as three adjacent X and Y fields
212	Begin subroutine definition using a complex feature and Position Data formatted as two adjacent X and Y fields
213	Begin subroutine definition using a complex feature and Position Data formatted as two adjacent XYZ fields
214	Begin subroutine definition using a complex feature and Position Data formatted as one set of XYZ fields
221	Begin subroutine definition using Circular interpolation and Position Data formatted as three adjacent X and Y fields
222	Begin subroutine definition using Circular interpolation and Position Data formatted as two adjacent X and Y fields
223	Begin subroutine definition using Point Record special shape (G4) and Position Data formatted as two adjacent XYZ fields
224	Begin subroutine definition using Point Record special shape (G4) and Position Data formatted as one set adjacent XYZ fields
299	End of subroutine

3.2.1.4 Point Records

The following IPC-D-350 point records operations codes are used by RAMP product Data:

IPC OPERATIONS CODES	DESCRIPTION
311	Begin New point record using Feature (land), hole concentric at a point and Position Data formatted as three adjacent X and Y fields
312	Begin New point record using Feature (land), hole concentric at the point, and Position Data formatted as two adjacent X and Y fields
313	Begin New point record using Feature (land), hole concentric at the point, and Position Data formatted as two adjacent XYZ fields
314	Begin New point record using Feature (land), hole concentric at the point, and Position Data formatted as one set of XYZ fields
321	Begin New point record using Feature (land) only at a point and Position Data formatted as three adjacent X and Y fields
322	Begin New point record using Feature (land) only at a point and Position Data formatted as two adjacent X and Y fields
323	Begin New point record using Feature (land) only at a point and Position Data formatted as two adjacent XYZ fields
324	Begin New point record using Feature (land) only at a point and Position Data formatted as one set of XYZ fields
331	Begin New point record using Hole only at a point and Position Data formatted as three adjacent X and Y fields
332	Begin New point record using Hole only at a point and Position Data formatted as two adjacent X and Y fields

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- 333 Begin New point record using Hole only at a point
 and Position Data formatted as two adjacent XYZ
 fields
- 334 Begin New point record using Hole only at a point
 and Position Data formatted as three XYZ fields
- 341 Begin New point record using Tooling feature with
 hole at the point and Position Data formatted as
 three adjacent X and Y fields
- 342 Begin New point record using Tooling feature with
 hole at the point and Position Data formatted as
 two adjacent X and Y fields
- 343 Begin New point record using Tooling feature with
 hole at the point and Position Data formatted as
 two adjacent XYZ fields
- 344 Begin New point record using Tooling feature with
 hole at the point and Position Data formatted as
 one set of XYZ fields
- 351 Begin New point record using Tooling feature only
 at a point and Position Data formatted as three
 adjacent X and Y fields
- 352 Begin New point record using Tooling feature only
 at a point and Position Data formatted as two
 adjacent X and Y fields
- 353 Begin New point record using Tooling feature only
 at a point and Position Data formatted as two
 adjacent XYZ fields
- 354 Begin New point record using Tooling feature only
 at a point and Position Data formatted as one set
 of XYZ fields
- 361 Begin New point record using Tooling hole only at
 the point and Position Data formatted as three
 adjacent X and Y fields
- 362 Begin New point record using Tooling hole only at
 the point and Position Data formatted as two
 adjacent X and Y fields

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- 363 Begin New point record using Tooling hole only at the point and Position Data formatted as two adjacent XYZ fields
- 364 Begin New point record using Tooling hole only at the point and Position Data formatted as one set of XYZ fields

3.2.1.5 Subroutine Call Records

The following IPC-D-350 subroutine call records operations codes are used by RAMP product Data:

IPC OPERATIONS CODES	DESCRIPTION
411	Begin Subroutine call using a Linear repeat or step-and-repeat and Position Data formatted as three adjacent X and Y fields
412	Begin Subroutine call using a Linear repeat or step-and-repeat and Position Data formatted as two adjacent X and Y fields
413	Begin Subroutine call using a Linear repeat or step-and-repeat and Position Data formatted as two adjacent XYZ fields
414	Begin Subroutine call using a Linear repeat or step-and-repeat and Position Data formatted as one set of XYZ fields
421	Begin subroutine call using Rotary repeat or step-and-repeat and Position Data formatted as three adjacent X and Y fields
422	Begin subroutine call using Rotary repeat or step-and-repeat and Position Data formatted as two adjacent X and Y fields
423	Begin subroutine call using Rotary repeat or step-and repeat and Position Data formatted as two adjacent XYZ fields
424	Begin subroutine call using Rotary repeat or step-and repeat and Position Data formatted as one set of adjacent XYZ fields

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3.2.1.6 Annotation Records

The following IPC-D-350 annotation records operations codes are used by RAMP product Data:

IPC OPERATIONS CODES	DESCRIPTION
511	Begin Annotation/dimension record using new annotation record and Position Data formatted as three adjacent X and Y fields
512	Begin Annotation/dimension record using new annotation record and Position Data formatted as two adjacent X and Y fields
513	Begin Annotation/dimension record using new annotation record and Position Data formatted as two adjacent XYZ fields
514	Begin Annotation/dimension record using new annotation record and Position Data formatted as one set of XYZ fields

3.2.2 IPC Parameter Records

The following parameters defined by IPC-D-350 are used in the RAMP Product Data file to describe basic PWB information:

<u>PARAMETER NAME</u>	<u>DESCRIPTION</u>
JOB	Job name from CAD database
DIM	Data Information Module
UNITS	Units of Measurement
LAYER	Relates CAD layers to Data layers in the file
IMAGE	Indicates whether described features are conductive or non-conductive
FAB	Describes PWB Construction materials and thicknesses

The use of these parameters in RAMP Product Data is described in the following paragraphs.

3.2.2.1 Job Parameter

The Job Parameter is the first record in the IPC-D-350 file and indicates the start of the job set. The entry is the PWB fabrication drawing number.

Example of usage in the IPC-D-350 file after translation:

P JOB 74E2N356

3.2.2.2 DIM Parameter

The Data Information Module (DIM) Parameter record indicates the start of a Data Information Module, which declares the type of product described by the data set. It appears just after the JOB Parameter record. The DIM Code Letter is taken from IPC-D-350D table 5-2 Record Interrelationship.

Example of usage in the IPC-D-350 file after translation:

P DIM B

3.2.2.3 Units Parameter

The Units Parameter indicates the Units of Measurement, either CUST (customary) or SI (metric) represented by the numeric values in the file. It follows the DIM Parameter record.

Example of usage in the IPC-D-350 file after translation:

P UNITS CUST

3.2.2.4 Layer Parameter

The PWB is described by the IPC-D-350 file using a series of conductive and nonconductive layers. Each of these layers is made of one or more data layers. The information for each layer is grouped together in the IPC-D-350 file separate from other layers. Just after the UNITS parameter record, a list of LAYER parameters appears which identify the physical PWB layers according to Table 4-1 "Layer Definitions" of IPC-D-350D. For each LAYER parameter, a COMP (compose) parameter exists that specifies which data layers comprise that physical PWB layer. A data layer is a group of geometric patterns that define features such as pad patterns, trace patterns, and power planes. An example of an IPC-D-350 LAYER record is:

P LAYER 03 COMP 11 08 21

In this example record, physical layer 03 which could be a conductive or nonconductive layer is composed of data layers 11, 08, and 21 which could be traces, pads, or other features.

3.2.2.5 Image Parameter

The Image Parameter indicates the type of features being described in the following data records, either COND for conductive features (pads and traces) or NCON for non-conductive features such as silk screens or solder masks.

Example of usage in the IPC-D-350 file after translation:

P IMAGE COND

3.2.2.6 FAB Parameter

Information used to describe the construction of the PWB is contained in the FAB Parameter. This parameter is an IPC-D-350C enhancement not available in IPC-D-350B.

Entity codes included with the FAB parameter are:

00	Nominal PWB Thickness
01	Copper Thickness *
12	PWB Base Material
17	Solder Mask Material
18	Conformal Coat Material

The following is an example of the use of the Fab Parameter:

	<u>ENTITY CODE</u>	<u>LAYER NO.</u>	<u>VALUE</u>
P FAB	00	00	000620

* To convert copper thickness to ounces of copper as per MIL-STD-275E, use:

0.0007 inches	=	0.5 ounces per square foot
0.0014 inches	=	1.0 ounces per square foot
0.0028 inches	=	2.0 ounces per square foot

3.2.3 IPC Feature/Location Records

The data set which follows the opening parameter records is made up of Feature/Location Records organized by Data Layer in accordance with IPC-D-350B.

3.2.4 IPC-D-350 NAMING CONVENTION

The IPC file is named "job.ipc". This file name is found in the IPC MIL-STD-1840 header file in "dstdocid:".

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<u>IPC-D-350 PHYSICAL LAYER NUMBER</u>	<u>DESCRIPTION</u>
Layer 00	BOARD OUTLINE, DRILL HOLES
Layer 01	COMPONENT SIDE - CONDUCTIVE
Layer 02	INNER LAYER 1 - CONDUCTIVE
Layer 03	INNER LAYER 2 - CONDUCTIVE
Layer 04	INNER LAYER 3 - CONDUCTIVE
Layer 05	INNER LAYER 4 - CONDUCTIVE
Layer 06	INNER LAYER 5 - CONDUCTIVE
Layer 07	INNER LAYER 6 - CONDUCTIVE
Layer 08	SECONDARY SIDE - CONDUCTIVE
Layer 09	COMPONENT SIDE SILK SCREEN
Layer 10	COMPONENT SIDE SOLDER MASK
Layer 11	SOLDER SIDE SOLDER MASK
Layer 12	SOLDER SIDE SILK SCREEN

FIGURE 3-3 IPC-D-350 EXAMPLE FOR AN 8-LAYER PWB

3.3 Components

A 3D model of a component is captured for its geometry as it is received from its vendor and for its geometry when assembled onto a PWA. These are known as a component's "as-received" and "as-assembled" models respectively. These data include not only the electrical components but all screws, fasteners, glue and any other hardware items found in the assembly parts list. IGES 4.0 is the data specification used to translate these 3D component data from the RPTS to the RAMP PWA factory.

3.3.1 Supported IGES Entity

RPTS uses the entities listed in Table 3-4.

Table 3-4 RAMP PWA IGES Entities	
<u>IGES ENTITIES</u>	<u>DESCRIPTION</u>
100	Circular Arc
102	Composite Arc
104 FORM	Conic Arcs
0	General Conic
106 FORM	Data Points
12	3D Line Strings
108	Planes
110	Line
116	Point
124	Transformation Matrix
126 FORM	
0	Rational B-Spline Curve
1	Rational B-Spline Curve
2	Rational B-Spline Curve
3	Rational B-Spline Curve
4	Rational B-Spline Curve
5	Rational B-Spline Curve
128 FORM	
0	B-spline Surface (Rational B-Spline Surface)
0	Solid Elliptical Cylinder (Rational B-Spline Surface)
0	Solid Elliptical Cone (Rational B-Spline Surface)
1	B-spline Surface (Rational B-Spline Surface)

Table 3-4 (CONT'D)
RAMP PWA IGES Entities

2	B-spline Surface (Rational B-Spline Surface)
3	B-spline Surface (Rational B-Spline Surface)
4	B-spline Surface (Rational B-Spline Surface)
5	B-spline Surface (Rational B-Spline Surface)
6	B-spline Surface (Rational B-Spline Surface)
7	B-spline Surface (Rational B-Spline Surface)
8	B-spline Surface (Rational B-Spline Surface)
9	B-spline Surface (Rational B-Spline Surface)
142	B-Spline Surface Boundary
144	B-Spline Surface (Trimmed Surface)
150	Solid Block
152	Solid Wedge (Right Angular Wedge)
154	Solid Cylinder (Right Cylinder)
156	Solid Cone (Right Circular Cone)
158	Solid Sphere
160	Solid Torus
162	Solid of Revolution
164	Solid of Projection (Solid of Linear Extrusion)
168	Solid Ellipsoid
180	Solid Boolean Tree
202	Dimension Component (Angular Dimension)
212 FORM	
0	General Note
214 FORM	
1	Leader (arrow)
216	Dimension Component (Linear Dimension)
218	Dimension Component (Ordinate Dimension)
220	Dimension Component (Point Dimension)
222	Dimension Component (Radius Dimension)
230	Sectioned Area
308	Symbol Header (Sub-figure Definition)
314	Color Table (Color Definition)
402 FORM	
7	Unordered Graphic Group with BP
406 FORM	
3	Level Function
15	Name Element
18	Intercharacter Space
408	Singular Sub-figure Instance (symbol)
410	View (Window/View)

3.3.2 As-Received 3D Component Data

The as-received component data consists of stylized representation of the component 3D geometry using maximum tolerance values. The following paragraphs describe the contents of the as-received component data.

3.3.2.1 Form Factor Set

The form factor set is the set of references based on the military specifications and is used to identify a component's shape or type of package. The component geometric data is included with the component's form factor. Form Factor is a group of physical attributes which describe the component shape and package type. The form factor consists of the basic component specification number, component specification slash or dash number if needed, the component package style/type number, and the component package case number. The following is a list of data types that constitutes the RAMP form factor set:

SPEC : {SPECIFICATION}
SNUM : { / (SLASH)NUMBER}
DNUM : { - (DASH)NUMBER}
STYLE/TYPE : {STYLE}
CASE : {CASE}

The form factor information is found in the header file for the component's as-received model. This is formally described in Appendix I.

3.3.2.2 Other Parts List Information

The Other Component Parts List information is defined using the following list of component attributes:

CLASS : {COMPONENT CLASSIFICATION}
SUB : {COMPONENT SUBCLASSIFICATION}
PKG : {COMPONENT PACKAGE}
EIA_JDC : {EIA/JEDEC FORM FACTOR}
CAGE : {CAGE/FSCM NUMBER}
ITEM : {ITEM NUMBER}
RDES : {REFERENCE DESIGNATOR}
PN : {PART NUMBER}
LEAD_MAT : {LEAD MATERIAL COMPOSITION}
LEAD_PLT : {LEAD PLATING MATERIAL COMPOSITION}

SOLDERABILITY: {COMPONENT SOLDERABILITY}

QNTY: : {QUANTITY OF EACH ITEM PER INSTANCE}

The other part list information is found in the header file for the component's as-received model. This is formally described in Appendix I.

3.3.2.3 Component Dimensional Attributes

The component dimensional data from the component specification documents provide the required data to determine actual component size. The following data types and their definitions are the geometric attributes for a component:

MAX_BODY_DIA : {BODY MAXIMUM DIAMETER}

NOM_BODY_DIA : {BODY NOMINAL DIAMETER}

MIN_BODY_DIA : {BODY MINIMUM DIAMETER}

MAX_BODY_LEN : {BODY MAXIMUM LENGTH}

NOM_BODY_LEN : {BODY NOMINAL LENGTH}

MIN_BODY_LEN : {BODY MINIMUM LENGTH}

MAX_BODY_WDT : {BODY MAXIMUM WIDTH}

NOM_BODY_WDT : {BODY NOMINAL WIDTH}

MIN_BODY_WDT : {BODY MINIMUM WIDTH}

MAX_BODY_HGT : {BODY MAXIMUM HEIGHT}

NOM_BODY_HGT : {BODY NOMINAL HEIGHT}

MIN_BODY_HGT : {BODY MINIMUM HEIGHT}

MAX_LEAD_DIA : {LEAD MAXIMUM DIAMETER}

NOM_LEAD_DIA : {LEAD NOMINAL DIAMETER}

MIN_LEAD_DIA : {LEAD MINIMUM DIAMETER}

MAX_LEAD_LEN : {LEAD MAXIMUM LENGTH}

NOM_LEAD_LEN : {LEAD NOMINAL LENGTH}

MIN_LEAD_LEN : {LEAD MINIMUM LENGTH}

MAX_LEAD_WDT : {LEAD MAXIMUM WIDTH}

NOM_LEAD_WDT : {LEAD NOMINAL WIDTH}

MIN_LEAD_WDT : {LEAD MINIMUM WIDTH}

MAX_LEAD_THK : {LEAD MAXIMUM THICKNESS}

NOM_LEAD_THK : {LEAD NOMINAL THICKNESS}

MIN_LEAD_THK : {LEAD MINIMUM THICKNESS}

The component dimensional attributes information is found in the header file for the component's as-received model. This is formally described in Appendix I.

3.3.2.4 As-Received Components Translated Into IGES

Each component part or item in the PWA is captured mechanically in its as-received geometry. The information captured for each component is translated to IGES making a separate IGES file for each component which allows the factory to review each component in its as-received geometric configuration.

3.3.2.5 As-Received Component IGES File Naming

Three IGES files are required for each As-Received component item on the BOM, one file using solid, one file using surface, and one file using wireframe IGES entities. As-Received component models in separate IGES files are named with "r" for As-Received components, followed by the component item number then "s" for IGES translation using solid entities, "u" for IGES translation using surface entities, "w" for IGES translation using wireframe entities, and with "-igs" extension for IGES. These file names are found in the IGES file 1840 header for each model in: "dstdocid:".

As-Received Component IGES with Solid Entities

r1s-igs = As received component BOM item 1 solid IGES file
r2s-igs = " 2
r3s-igs = " 3
...
rNs-igs with N equal to the last component item number on the
BOM and gaps in numerical sequence are allowed.

As-Received Component IGES with Surface Entities

r1u-igs = As received component BOM item 1 surface IGES file
r2u-igs = " 2
r3u-igs = " 3
...
rNu-igs with N equal to the last component item number on the
BOM and gaps in numerical sequence are allowed.

As-Received Component IGES with Wireframe Entities

rlw-igs = As received component BOM item 1 wireframe IGES file
r2w-igs = " 2
r3w-igs = " 3
...
rNw-igs with N equal to the last component item number on the
BOM and gaps in numerical sequence are allowed.

3.3.3 As-Assembled 3D Component

The as-assembled 3D component is a geometric stylized representation of an item as it appears when inserted in the 3D model of the PWA. The 3D as-assembled component model is sent for each instance of the item on the PWA.

An as-assembled 3D component appears as a sub-figure (entity type 408: IGES-SUBFIGURE-INSTANCE) in the IGES translation of the fully developed 3D model of the PWA. There is an IGES entity type 408 for each instance of a item used.

3.3.3.1 Reference Designator

The Reference Designator is the unique identifier for each instance of an item used in a PWA.

RDES = { REFERENCE DESIGNATOR }

Where RDES is the property nomenclature and {REFERENCE DESIGNATOR } is the value of the property.

For 3D components, the value of the property (RDES) is used as the sub-figure name in the IGES translation of the assembly.

3.3.3.2 Pin Numbers

Pin numbers are unique identifiers for each pin of a component.

The pin numbers for 3D components correspond to the pin numbers of components in the 2D assembly. Pin numbers are inserted in the 3D model of the component as text. The location (origin) of the pin number text is coincident with X,Y hole locations as derived from the 2D assembly.

The pin number text is translated in IGES as part of the 3D sub-figure representing a component and is placed on the layer designated as component lead (see Table 3-5 IGES Layering Convention).

3.3.3.3 Component Bodies

The component body is that part of the component that encapsulates the material that performs the required electrical function. The component's leads attach to the component's body. If the component's body also serves as an electrical lead then it is classified as a body.

The geometry generated for the 3D component body is the geometry necessary to create a stylized model. The dimensions of this model are given at their maximum tolerance limits.

The geometry for the component body is in IGES as part of the component sub-figure. See Table 3-5.

3.3.3.4 Component Leads

The component lead is that part of the component that forms an electrical connection with other components.

The geometry generated for the 3D component lead includes the nominal center to center lead spacing and other geometry that is necessary to create a stylized model of the component lead.

The geometry for the component lead is translated into IGES as part of the component sub-figure. See TABLE 3-5.

3.3.3.5 Orientation Vector

The orientation vector is a line segment placed in the body of a 3D component model with its origin at the component centroid. This vector is used to determine the orientation of the component when the component is placed in the 3D assembly model.

The orientation vector is in IGES as part of the component sub-figure is found on the orientation vector layer. See Table 3.5.

3.3.3.6 Centroid

The centroid is a point in the body of a 3D component model located at the center of mass assuming an uniform mass distribution within the solid model of the component body.

The centroid is found in IGES as part of the component sub-figure and is inserted in the model on the layer specified for Orientation Vector. See Table 3.5.

3.4 3D Assembly

The 3D Assembly is the 3D model of the PWA with all the 3D models of the "As Assembled" components inserted in their correct locations. Figure 3-4, IGES Assembly Data, illustrates the type of assembly data carried in IGES.

3.4.1 Maximum Assembly Envelope

The maximum assembly envelope is the maximum extent of component heights after assembly of the PWA.

The 3D version of the maximum assembly envelope is represented as a surface of zero thickness with planes that are coincident with the maximum outside envelope of the PWA.

The surface representing the maximum assembly envelope is in IGES as part of the 3D assembly model on the layer specified for the maximum assembly envelope. See Table 3-5.

3.4.2 Conformal Coat Mask

The conformal coat mask is a protective coating that conforms to the outside of a PWA except in places where the coating would interfere with the operation of the PWA.

The 3D version of the conformal coat mask is represented as a surface with a thickness defined for conformal coating in the TDP with planes that are coincident with the maximum outside envelope of the PWA as defined by the TDP.

The surface representing the conformal coat mask is found in IGES as part of the 3D assembly model on the layer specified for the conformal coat mask. See Table 3-5.

3.4.3 Ink

Ink is used to indicate special markings that must be applied to the PWA.

The 3D version of the ink is placed as text in the 3D assembly model on the areas that reflect the placement of ink text. The ink text is translated in IGES as part of the 3D assembly model on the layer specified for ink. See Table 3-5.

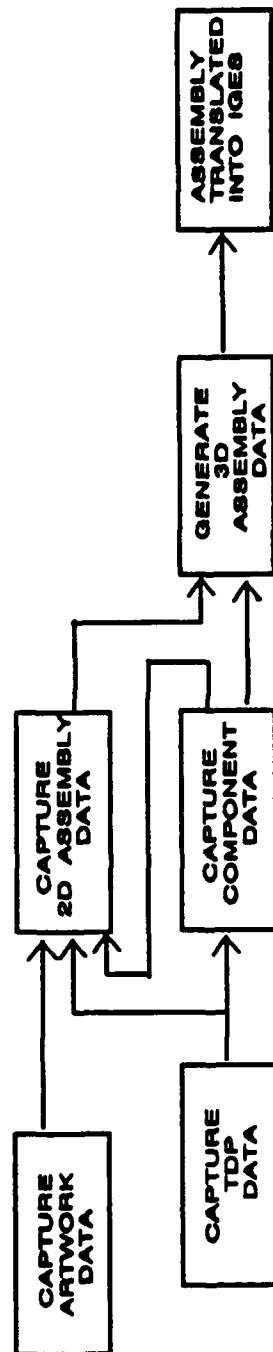


FIGURE 3-4 IGES ASSEMBLY DATA

0180003

3.4.4 Glue

Glue is an adhesive substance used to hold components together. Glue is represented in the 3D assembly as a surface with a thickness that reflects the maximum thickness allowed for glue as specified by the TDP on the areas shown in the TDP where glue is to be applied.

The surface representing the glue is translated as part of the 3D assembly model on the layer specified for glue. See Table 3-5.

3.4.5 Special Assembly

A component that fails any of the following rules is placed on one of the Special Assembly layers (see Table 3-5).

1. The component attaches to the PWB only by soldering its leads.
2. The Orientation Vector is parallel to the PWB orientation vector.
3. The component has no intersecting or overlapping 2D projections with another component as viewed from the component side(s) of the PWA.
4. There are no specific restrictions to the wave/reflow soldering of the component.
5. The component does not have Special TDP Assembly instructions.

Any component failing the above rules has its sub-figure segregated by layer as a special assembly sub-figure. This sub-figure is found in IGES as part of the 3D assembly model on the layer specified for special assemblies. See Table 3-5.

3.4.6 ASSEMBLY DATA LIST

The assembly Data List provides a list of drawing numbers and their type classification of the TDP drawings that comprise the PWA. This Data List is found in the IGES assembly (see Table 3-5). The formal syntax is given in Appendix I. If the specification is not available then the description = "NONE". The following is a list of the document types carried in the Data List:

<u>SPECIFICATION TYPE</u>	<u>SPECIFICATION DESCRIPTION</u>
ASSEM	ASSEMBLY SPECIFICATIONS
PWBSB	PWB SPECIFICATIONS
PROSP	PROCESS SPECIFICATIONS
PROG	COMPUTER SPECIFICATIONS
SCHEM	SCHEMATIC SPECIFICATIONS
TSTSP	TEST SPECIFICATIONS
CMPSP	COMPONENT SPECIFICATIONS
NEXAS	NEXT ASSEMBLY
USEON	USED ON

3.4.7 IGES Layering Convention

The RAMP PWA IGES layering convention is used to identify component and assembly information. This layering convention is given in Table 3-5.

TABLE 3-5 IGES LAYERING CONVENTION
Component Subfigure Layers: LAYER 00 Component Body LAYER 01 Component Leads LAYER 02 Component Orientation Vector/Centroid LAYER 03 Component Pin Text LAYER 04 Future Expansion

TABLE 3-5 (CONT'D)
IGES LAYERING CONVENTION

Assembly Layers:

LAYER 00 BATTE
LAYER 05 CAP
LAYER 10 CHEM
LAYER 15 CON
LAYER 20 CORE
LAYER 25 HDWR
LAYER 30 IND
LAYER 35 LAMP
LAYER 40 RES
LAYER 45 ROTMA
LAYER 50 SEMI
LAYER 55 SWTCH
LAYER 60 TRADU
LAYER 65 UCKT
LAYER 70 XFMR
LAYER 75 SPECIAL ASSEMBLY BATTE
LAYER 79 SPECIAL ASSEMBLY BATTE INSTRUCTIONS
LAYER 80 SPECIAL ASSEMBLY CAP
LAYER 84 SPECIAL ASSEMBLY CAP INSTRUCTIONS
LAYER 85 SPECIAL ASSEMBLY CHEM
LAYER 89 SPECIAL ASSEMBLY CHEM INSTRUCTIONS
LAYER 90 SPECIAL ASSEMBLY CON
LAYER 94 SPECIAL ASSEMBLY CON INSTRUCTIONS
LAYER 95 SPECIAL ASSEMBLY CORE
LAYER 99 SPECIAL ASSEMBLY CORE INSTRUCTIONS
LAYER 100 SPECIAL ASSEMBLY HDWR
LAYER 104 SPECIAL ASSEMBLY HDWR INSTRUCTIONS
LAYER 105 SPECIAL ASSEMBLY IND
LAYER 109 SPECIAL ASSEMBLY IND INSTRUCTIONS
LAYER 110 SPECIAL ASSEMBLY LAMP
LAYER 114 SPECIAL ASSEMBLY LAMP INSTRUCTIONS
LAYER 115 SPECIAL ASSEMBLY RES
LAYER 119 SPECIAL ASSEMBLY RES INSTRUCTIONS
LAYER 120 SPECIAL ASSEMBLY ROTMA
LAYER 124 SPECIAL ASSEMBLY ROTMA INSTRUCTIONS
LAYER 125 SPECIAL ASSEMBLY SEMI
LAYER 129 SPECIAL ASSEMBLY SEMI INSTRUCTIONS
LAYER 130 SPECIAL ASSEMBLY SWTCH
LAYER 134 SPECIAL ASSEMBLY SWTCH INSTRUCTIONS
LAYER 135 SPECIAL ASSEMBLY TRADU

TABLE 3-5 (CONT'D) IGES LAYERING CONVENTION
--

LAYER 139 SPECIAL ASSEMBLY TRADU INSTRUCTIONS LAYER 140 SPECIAL ASSEMBLY UCKT LAYER 144 SPECIAL ASSEMBLY UCKT INSTRUCTIONS LAYER 145 SPECIAL ASSEMBLY XMFR LAYER 149 SPECIAL ASSEMBLY XMFR INSTRUCTIONS LAYER 150 SPECIAL GENERAL INSTRUCTIONS LAYER 155 MAXIMUM ASSEMBLY ENVELOPE LAYER 160 CONFORMAL COAT MASK LAYER 165 ASSEMBLY INKING OR MARKING LAYER 170 ASSEMBLY DATA LIST LAYER 180 PWB

3.4.8 Special Instructions

Special instructions are notes from the TDP that require human interpretation. Special instructions are found in the IGES as part of the 3D assembly model on a special assembly instructions layer for each component class. See TABLE 3-5.

3.4.9 3D Assembly Solid Model

Assembly data are found in an IGES file using solid IGES entities. The file naming convention identifies the IGES file as the solid assembly. The naming convention for 3D solid assembly IGES file is:

jobs-igs

This file name is found in the IGES 1840 header associated with this solid assembly file in "dstdocid:"

3.4.10 3D Assembly Surface Model

Assembly data are found in an IGES file using surface IGES entities. The file naming convention identifies the IGES file as the surface assembly. The naming convention for the 3D surface assembly IGES file is:

jobu-igs

This file name is found in the IGES 1840 header associated with this solid assembly file in "dstdocid:"

3.4.11 3D Assembly Wireframe Model

Assembly data are found in an IGES file using wireframe IGES entities. The file naming convention identifies the IGES file as the wireframe assembly. The naming convention for the 3D wireframe assembly IGES file is:

jobw-igs

This file name is found in the IGES 1840 header associated with this solid assembly file in "dstdocid:"

3.5 TDP Raster

The entire TDP is included in the product data description in raster data format. Raster data are in accordance with MIL-STD-1840 for type I (untiled) as defined in MIL-R-28002 (CCITT G4). Raster image density is 200 Dots Per Inch (DPI) for all drawing sizes. Figure 3-5 "CCITT G4 Raster Data" illustrates the type of raster data carried by CCITT G4.

3.5.1 Raster File Naming

The raster files are named using the drawing type and document number. The document page number is added after a dash. The file name is ended with ".RAS" extension. The document file name is inserted in the 1840 header of the raster file in the destination document ID record "dstdocid:".

For example:

TYPE, DOCUMENT NUMBER-p.RAS

74E2E356-12.RAS

SP82N5200-1.RAS

82N5200-42.RAS

82N5200-3.RAS

The document type is derived from columns 1 and 2 of the aperture card punch code. Document number is derived from columns 3 through 17 and the sheet number is derived from columns 39 through 41. If an * (asterisk)

DRAFT

RTIF PROGRAM DOCUMENT NO.: UMR001002-0
31 JANUARY 1992

appears in column 41, then card number appears in columns 55 through 58.
Unpunched columns are not used.

3.5.2 1840 Header Definition

The 1840 file header records are formatted as specified by MIL-STD-1840 for type I raster binary data.

DRAFT

RTIF PROGRAM DOCUMENT NO.: UMR001002-0
31 JANUARY 1992

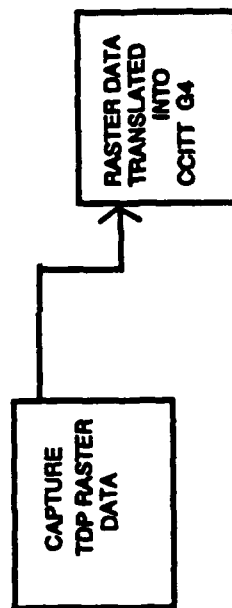


FIGURE 3-5 CCITT G4 TDP RASTER DATA

0151K2

3.6 CALS File Naming Convention

File naming conventions are in accordance with CALS MIL-STD-1840 Automated Interchange of Technical Information and RAMP PWA data conventions. MIL-STD-1840 requires, for file transfer, one declaration file per TDP.

The naming convention requires that the declaration file be named D001, D002, D003, through DNNN with the data files being named D001X001, D001X002, through DNNNXNNN as shown in Figure 3-6. X, the fifth character in the data file, indicates the type of file Q for IGES, E for EDIF, I for IPC-D-350, R for RASTER, and T for TEXTUAL files.

3.6.1 ISF File Naming

The ISF files produced by the RPTS PWA are named to MIL-STD-1840 names as illustrated here:

<u>1840 NAME</u>	<u>DESCRIPTION</u>
------------------	--------------------

D001	= DOCUMENT FILE Declaration
------	-----------------------------

D001R001	= TDP RASTERIZED
----------	------------------

D001T001	= TEXTUAL FILE
----------	----------------

D001Q001	= IGES SOLIDS ASSEMBLY MODEL DATA FILE
----------	--

D001Q002	= IGES SURFACES ASSEMBLY MODEL DATA FILE
----------	--

D001Q003	= IGES WIREFRAME ASSEMBLY MODEL DATA FILE
----------	---

D001Q004	= IGES SOLIDS AS RECEIVED COMPONENT MODEL DATA FILE
----------	---

D001Q00N	= etc. thru to the last solids component model IGES file.
----------	---

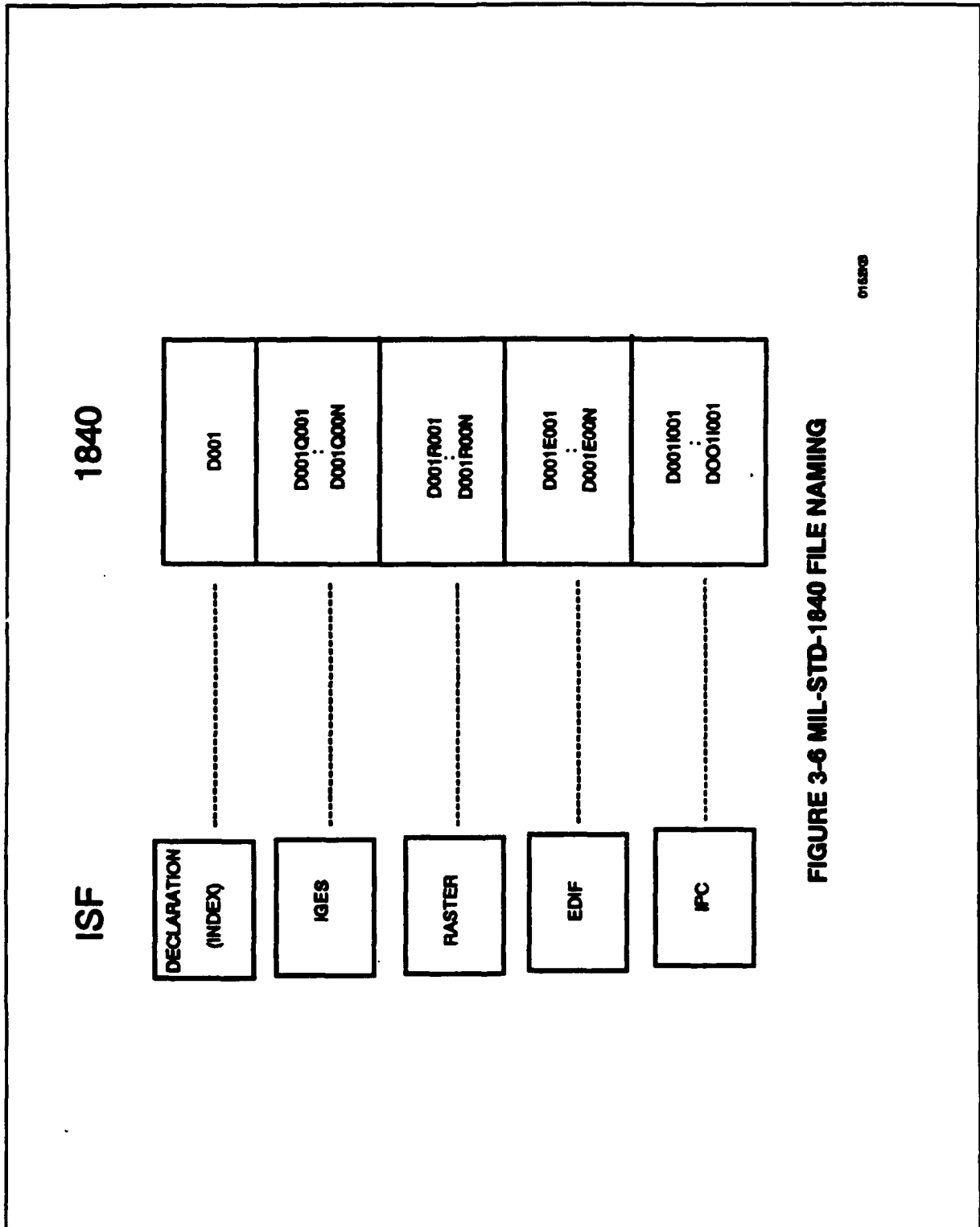
D001Q00(N+1)	= IGES SURFACE AS RECEIVED COMPONENT MODEL DATA FILE.
--------------	---

D001Q00X	= etc. thru to the last surface component model IGES file.
----------	--

D001Q00(X+1)	= IGES WIREFRAME AS RECEIVED COMPONENT MODEL DATA FILE.
--------------	---

D001E001	= EDIF SCHEMATIC DATA FILE = RAMP PWA job.edf
----------	---

D001I001	= IPC LAYOUT DATA FILE = RAMP PWA job.ipc
----------	---



015350

FIGURE 3-6 MIL-STD-1840 FILE NAMING

3.6.2 DPD Release Level

The change level record 4 (chglvl:) in the declaration file of the DPD contains the change level, release status, and release date of the DPD. The change level will have an entry of ORIGINAL for the first release and letters according to DOD-STD-100C for subsequent releases. Letter changes will occur only on VALIDATED DPDs. VERIFIED DPDs will hold the next change letter in the sequence since the last VALIDATED DPD was issued. A DPD undergoing a change may have several VERIFIED releases until it is VALIDATED. Only its release date changes from release to release.

For example suppose the last release level was:

chglvl: B,VALIDATED,19911108

then the next file from the RPTS PWA on the next change request will be:

chglvl: C,VERIFIED,19920225

The next DPD file which reflects a corrected to the change will take a release level:

chglvl: C,VERIFIED,19920312

Then, after the file has been validated by a quality assurance activity its release level changes to:

chglvl: C,VALIDATED,19920305

3.6.3 Declaration File

The declaration file provides information about the identification, source, destination, classification of the document, and gives a count of the files in the set of files that make up the complete document. The required format for the entry of data in 1840 headers is in APPENDIX I.

3.6.4 File Header

Each of the files included in an ISF set has a header. The header is in accordance with MIL-STD-1840. The declaration and header has the following information in sequence (See Table 3-6 and 3-7):

Table 3-6
MIL-STD-1840 Declaration

Declaration FILE D001

srcsys: RPTS, 5300 International Blvd., N. Charleston, SC 29418
 srcdocid: NONE
 srcrelid: NONE
 chglvl: ORIGINAL, VERIFIED, 19920123
 dteisu: 19870721
 dstsys: RPWA, 5300 International Blvd., N. Charleston, SC 29418
 dstdocid: 12051, 74E2N356, E
 dstrelid: NONE
 dtetrn: 19910405
 dlvac: CDRL item 1 of Contract 74529044334 , Due 19920721
 filcnt: Q37, I1, E1
 ttlcls: Unclass
 doccls: Unclass
 doctyp: Printed Wiring Assembly
 docttl: Fault Reset Control

Table 3-7
MIL-STD-1840 Headers

RASTER HEADER

srcdocid	Source System Document Identifier
dstdocid	Destination System Document Identifier
txtfilid	Text File Identifier
figid	Figure Identifier
srcgph	Source System Graphics Filename
doccls	Data File Security Label
rtype	Raster Data MIL-R-28002 Type 1 or 2
rorient	Raster Image Orientation
rpelcnt	Raster Image Picture Element Count
rdensity	Raster Image Density
notes	

Table 3-7 (CONT'D)
MIL-STD-1840 Header

Raster Header file example:

srcdocid: HOLLERITH CODE
dstdocid: SH74E2N356-1.ras
txtfilid: NONE
figid: NONE
srcgph: NONE
doccls: unclass
rtype: 1
rorient: 090,270
rpelcnt: 005120,005120
rdensity: 0400
notes:

IGES, EDIF, AND IPC HEADER

srcdocid	Source System Document Identifier
dstdocid	Destination System Document Identifier
txtfilid	Text File Identifier
figid	Figure Identifier
srcgph	Source System Graphics Filename
doccls	Data File Security Label
notes	

IGES Header file example:

srcdocid: NONE
dstdocid: r10w-igs
txtfilid: NONE
figid: NONE
srcgph: NONE
doccls: unclass
notes:

Table 3-7 (CONT'D)
MIL-STD-1840 Header

EDIF Header file example:

srcdocid: NONE
dstdocid: job.edf
txtfilid: NONE
figid: NONE
srcgph: NONE
doccls: unclass
notes:

IPC Header file example:

srcdocid: NONE
dstdocid: job.ipc
txtfilid: NONE
figid: NONE
srcgph: NONE
doccls: unclass
notes:

3.6.5 File Name Summary

The file name summary provides quick reference of file type, file specification, MIL-STD-1840 name, and a generic CAD name. See Table 3-8.

TABLE 3-8 FILE NAME SUMMARY		
FILE TYPE	SPECIFICATION	1840 NAME
2DECLARATION	= MIL-STD 1840	= D001
RASTER	= MIL-STD 1840	= D001R001 ...
TEXTUAL	= MIL-STD 1840	= D001T001
SCHEMATIC	= EDIF	= D001E001
ASSEMBLY 3D	= IGES	= D001Q001
WIREFRAME		
ASSEMBLY 3D	= IGES	= D001Q002
SURFACE		
ASSEMBLY 3D	= IGES	= D001Q003
SOLID		
COMPONENT	= IGES	= D002Q002 ...
2D LAYOUT	= IPC	= D001I001

3.6.6 Physical Media for File Transfer

The RPTS PWA supports 1/4 cartridge tape as a physical file transfer media.

APPENDIX I10.0 PDD FORMAL SYNTAX10.1 ATTRIBUTE FORMAL SYNTAX

The formal syntax definition (FSD) for adding RAMP required attributes to the component descriptions. The syntax used is derived from Backus-Naur Format (BNF).

Operator definitions.

<u>OPERATOR</u>	<u>MEANING</u>
:	is defined as
	separation between options
[]	optionality brackets
;	end of a rule in the FSD
!	introduction of a comment
{ }	rule grouping
,	separates required operation

10.2 COMPONENT ATTRIBUTES10.2.1 EDIF SCHEMATIC COMPONENT ATTRIBUTES

EDIF component attributes are those component attributes that are defined as properties of a schematic component symbol.

```

comp-model: { comp-spec
               comp-class
               comp-prop
               comp-geom };

comp-class: { "CLASS" class-name };

class-name: { "BATTE"
              batte-sub-name
              pkg-name |
              "CAP"
              cap-sub-name
              pkg-name |
              "CHEM"
              chem-sub-name
              pkg-name |
              "CON"
              con-sub-name
              pkg-name |

```

```

"CORE"
  core-sub-name
  pkg-name |
"IND"
  ind-sub-name
  pkg-name |
"LAMP"
  lamp-sub-name
  pkg-name |
"HDWR"
  hdwr-sub-name
  pkg-name |
"IND"
  ind-sub-name
  pkg-name |
"PWB"
  pwb-sub-name
  pwb-pkg-name
"RES"
  res-sub-name
  pkg-name |
"ROTMA"
  rotmac-sub-name
  pkg-name |
"SEMI"
  semi-sub-name
  pkg-name |
"SWTCH"
  swtch-sub-name
  pkg-name |
"TRADU"
  tradu-sub-name
  pkg-name |
"UCT"
  uckt-sub-name
  pkg-name |
"XFMR"
  xfmr-sub-name
  pkg-name );

```

```
batte-sub-name: { "NONR" | "RECH" };
```

```
cap-sub-name: { "FIXED" | "VAR" };
```

```
chem-sub-name: { "BAGT" | "CAGT" | "CLAGT" | "IAGT" | "MAGT" | "TAGT" };
```

```
con-sub-name: { "ANTEN" | "BUSBR" | "EDGE" | "FUSE" | "JUM" | "PLUG" | "RECPT"
  | "TERM" | "TERMT" | "TERMP" | "TETBK" };
```

```

core-sub-name: { "FEBED" };

ind-sub-name: { "FIXED" | "VAR" };

lamp-sub-name: { "FLUOR" | "GLOW" | "INCAN" | "BALLA" };

hdwr-sub-name: { "BOLT" | "BRACK" | "BRVT" | "CLAMP" | "CRVT" | "CLIP" | "EJECT"
| "EYELE" | "FRAME" | "FWSHR" | "LWSHR" | "HANDL" | "INSUL" |
"NUT" | "PIN" | "RRING" | "TIES" | "TRVT" | "SCREW" | "SHIEL" |
"SLEEV" | "SPACE" | "SPREA" | "SPRIN" };

ind-sub-name: { "FIXED" | "VAR" };

pwb-sub-name: { "FLEX" | "HYB" | "MOLD" | "RFLEX" |
"RIGID" };

res-sub-name: { "FIXED" | "VAR" };

rotma-sub-name: { "ACMAC" | "DCMAC" | "SYNCH" };

semi-sub-name: { "DIODE" | "SCR" | "TRANS" };

swtch-sub-name: { "SWTCH" | "RELAY" };

tradu-sub-name: { "BELL" | "HALL" | "MIC" | "SPK" | "XTL" };

uckt-sub-name: { "DIG" | "HYB" | "LIN" | "MIXED" };

xfmr-sub-name: { "POWER" | "SIGNL" };

pwb-pkg-name: { "TYPE1" | "TYPE2" | "TYPE3" | "TYPE4" | "TYPE5" | "TYPE6" };

pkg-name: { "AXIAL" | "CAN" | "CHIP" | "RDL" | "SM" | "SM" | "PLCLP" |
"MTCLP" | "PCLIP" | "HANDL" | "LOBAR" | "PUBAR" | "DISK" |
"PAD" | "PLATE" | "WASHR" | "ALIGN" | "SPRIN" | "PTIES" |
"STIES" | "TUBE" | "HTSRK" | "COMPS" | "TENSPP" | "THERS" };

attribute_name: "PTYPE" ptype-name
                 "RDES" rdes-name
                 ["CHTYP_VAL" chtyp_val-name]
                 ["CHTYP_PTL" chtyp_ptl-name]
                 ["CHTYP_NTL" chtyp_ntl-name]
                 "GPN" gpn-name
                 ["CHTYP_LT" chtyp_lt-name]
                 "AP SPEC" ap_spec-name
                 "PN" pn-name
                 "ITEM" item-name
                 ["CAGE" cage-name]

```

```
["MAX_WK_VOLT" max_wk_volt-name]
["COMP_PWR" comp_pwr-name]
["SOLDERABILITY" solderability-name]
["LEAD_MAT" lead_mat-name]
["LEAD_PLT" lead_plt-name]
["REV" rev-name]
```

10.2.2 3D COMPONENT ATTRIBUTES IN IGES HEADER

IGES 3D component attributes are those component attributes that are defined as properties of a 3D component.

```
"SPEC" spec-name
["SNUM" snum-name]
["DNUM" dnum-name]
["STYLE" style-name]
["CASE" case-name]
["AP_SPEC" ap_spec-name]
["EIA_JDC" eia_jdc-name]
"CLASS" class-name
"SUB" sub-name
"PKG" pkg-name
["QNTY" qty-name]
["MAX_WK_VOLT" max_wk_volt-name]
["COMP_PWR" comp_pwr-name]
["SOLDERABILITY" solderability-name]
["LEAD_MAT" lead_mat-name]
["LEAD_PLT" lead_plt-name]
"MAX_BODY_DIA" max_body_dia-number
"MIN_BODY_DIA" min_body_dia-number
"MAX_BODY_LEN" max_body_len-number
"MIN_BODY_LEN" min_body_len-number
"MAX_BODY_WDT" max_body_wdt-number
"MIN_BODY_WDT" min_body_wdt-number
"MAX_BODY_HGT" max_body_hgt-number
"MIN_BODY_HGT" min_body_hgt-number
"MAX_LEAD_DIA" max_lead_dia-number
"MIN_LEAD_DIA" min_lead_dia-number
"MAX_LEAD_LEN" max_lead_len-number
"MIN_LEAD_LEN" min_lead_len-number
"MAX_LEAD_WDT" max_lead_wdt-number
"MIN_LEAD_WDT" min_lead_wdt-number
```

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"MAX_LEAD_THK" max_lead_thk-number
"NOM_LEAD_THK" nom_lead_thk-number
"MIN_LEAD_THK" min_lead_thk-number

10.2.3 COMPONENT ATTRIBUTE DATA FORMAT

ptype-name: { "ANA" | "BIZ" | "CAP" | "CSW" | "CUST" | "ZDI" | "DAR"
| "DIO" | "DIPCAP" | "EDG" | "FET" | "FUS" | "HYB"
| "IND" | "JUM" | "LED" | "LSI" | "MSI" | "OPJ" | "OSW"
| "PCA" | "PWB" | "PIS" | "POT" | "PWB" | "RCL" | "RCNO"
| "RCNC" | "RES" | "RHE" | "RP DB" | "RP DH" | "RP DI"
| "RP DT" | "RP SB" | "RP SH" | "RP SI" | "RP ST" | "SCR"
| "SSI" | "TCA" | "TCP" | "TPCS" | "TRA" | "TRNN" |
| "TRNP" | "UNI" | "VHSIC" | "VLSI" | "XTL" | "ZDI"};

rdes-name: { any alpha-numeric name not to exceed 8 characters in
length};

f4-number: { "1" | "1" | "1" | "1"
"2" | "2" | "2" | "2"
"3" | "3" | "3" | "3"
"4" | "4" | "4" | "4"
"5" | "5" | "5" | "5"
"6" | "6" | "6" | "6"
"7" | "7" | "7" | "7"
"8" | "8" | "8" | "8"
"9" | "9" | "9" | "9"
"0" | "0" | "0" | "0" };

chtyp_val-name: { f7.4 [val-multiplier]};

pos-integer: { "1" | "2" | "3" | ...};

val-multiplier: { "T" | "G" | "M" | "K" | "m" | "u" | "n" | "p" |
"f"};

chtyp_ntl-name: percent;

chtyp_ptl-name: percent;

percent: { "1" | "1" | "1" | "." | "1"
"2" | "2" | "2" | "." | "2"
"3" | "3" | "3" | "." | "3"
"4" | "4" | "4" | "." | "4"
"5" | "5" | "5" | "." | "5"
"6" | "6" | "6" | "." | "6"

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"7"	"7"	"7"	"."	"7"
"8"	"8"	"8"	"."	"8"
"9"	"9"	"9"	"."	"9"
"0"	"0"	"0"	"."	"0"

};

gpn-name: { any alpha-numeric ASCII name not to exceed 15
characters in length};

chtyp_lt-name: { "ALU" | "ANA" | "CLK" | "CNT" | "COM" |
"DMUX" | "DRAM" | "HYB" | "MUX" | "PIO" |
"PLD" | "RAM" | "ROM" | "SEQ" | "SRAM" |};

ap_spec-name: { any alpha-numeric name not to exceed 15 characters in
length};

pn-name: { any alpha-numeric name not to exceed 18 characters in
length};

qnty-name: { f3-number "IN" | "NS" | "AR" };

item-name: { f4-number };

cage-name: { f5-number };

f5-number: {

"1"	"1"	"1"	"1"	"1"
"2"	"2"	"2"	"2"	"2"
"3"	"3"	"3"	"3"	"3"
"4"	"4"	"4"	"4"	"4"
"5"	"5"	"5"	"5"	"5"
"6"	"6"	"6"	"6"	"6"
"7"	"7"	"7"	"7"	"7"
"8"	"8"	"8"	"8"	"8"
"9"	"9"	"9"	"9"	"9"
"0"	"0"	"0"	"0"	"0"

};

f15-number:
{

"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"
"2"	"2"	"2"	"2"	"2"	"2"	"2"	"2"
"3"	"3"	"3"	"3"	"3"	"3"	"3"	"3"
"4"	"4"	"4"	"4"	"4"	"4"	"4"	"4"
"5"	"5"	"5"	"5"	"5"	"5"	"5"	"5"
"6"	"6"	"6"	"6"	"6"	"6"	"6"	"6"
"7"	"7"	"7"	"7"	"7"	"7"	"7"	"7"
"8"	"8"	"8"	"8"	"8"	"8"	"8"	"8"
"9"	"9"	"9"	"9"	"9"	"9"	"9"	"9"
"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"

..5);

max_wk_volt-name : { f7.4-number };

f7-number:

"1"	"1"	"1"	"1"	"1"	"1"	"1"	"1"
"2"	"2"	"2"	"2"	"2"	"2"	"2"	"2"
"3"	"3"	"3"	"3"	"3"	"3"	"3"	"3"
"4"	"4"	"4"	"4"	"4"	"4"	"4"	"4"
"5"	"5"	"5"	"5"	"5"	"5"	"5"	"5"
"6"	"6"	"6"	"6"	"6"	"6"	"6"	"6"
"7"	"7"	"7"	"7"	"7"	"7"	"7"	"7"
"8"	"8"	"8"	"8"	"8"	"8"	"8"	"8"
"9"	"9"	"9"	"9"	"9"	"9"	"9"	"9"
"0"	"0"	"0"	"0"	"0"	"0"	"0"	"0"

 ..15);

comp_pwr-name: { f7.4-number);

solderability-name : { "NIL" | "NOWAV" | "NRFLO" | "NWRF");

lead_mtl-name: { "STL" | "OTH");

lead_plt-name: { "GLD" | "OTH");

rev-name: { DOD-STD-100 change letters};

spec-name: { any alpha numeric ASCII name not to exceed 5 characters in length};

snum-name: { any numeric ASCII name not to exceed 3 characters in length};

dnun-name: { any numeric ASCII name not to exceed 4 characters in length};

style-name: { any alpha numeric ASCII name not to exceed 8 characters in length};

case-name: { any alpha numeric ASCII name not to exceed 8 characters in length};

eia_jedec-name: { any alpha numeric ASCII name not to exceed 12 characters in length};

nom_body_dia-number: { f7.4-number);

min_body_dia-number: { f7.4-number);

max_body_len-number: { f7.4-number);

nom_body_len-number: { f7.4-number);

min_body_len-number: { f7.4-number);

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max_body_wdt-number: { f7.4-number };
nom_body_wdt-number: { f7.4-number };
min_body_wdt-number: { f7.4-number };
max_body_hgt-number: { f7.4-number };
nom_body_hgt-number: { f7.4-number };
min_body_hgt-number: { f7.4-number };
max_lead_dia-number: { f7.4-number };
nom_lead_dia-number: { f7.4-number };
min_lead_dia-number: { f7.4-number };
max_lead_len-number: { f7.4-number };
nom_lead_len-number: { f7.4-number };
min_lead_len-number: { f7.4-number };
max_lead_wdt-number: { f7.4-number };
nom_lead_wdt-number: { f7.4-number };
min_lead_wdt-number: { f7.4-number };
max_lead_thk-number: { f7.4-number };
nom_lead_thk-number: { f7.4-number };
min_lead_thk-number: { f7.4-number };

f7.4-number: ("1" | "1" | "1" | "." | "1" | "1" | "1" | "1" |
"2" | "2" | "2" | "." | "2" | "2" | "2" | "2" |
"3" | "3" | "3" | "." | "3" | "3" | "3" | "3" |
"4" | "4" | "4" | "." | "4" | "4" | "4" | "4" |
"5" | "5" | "5" | "." | "5" | "5" | "5" | "5" |
"6" | "6" | "6" | "." | "6" | "6" | "6" | "6" |
"7" | "7" | "7" | "." | "7" | "7" | "7" | "7" |
"8" | "8" | "8" | "." | "8" | "8" | "8" | "8" |
"9" | "9" | "9" | "." | "9" | "9" | "9" | "9" |
"0" | "0" | "0" | "." | "0" | "0" | "0" | "0" |) ;

10.3 ASSEMBLY ATTRIBUTES

"IGES_LAYER" iges_layer-name
 "SNUM" slash-number
 "DNUM" dash-number
 "STYLE" style-name
 "CASE" case-name
 "EIA_JEDEC" eia_jedec-name
 "data_list" data_list-name
 "data_list_drawing" data_list_drawing-name

slash-number: (

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"
"0"

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"
"0"

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"
"0"

);

f3-number: (

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"
"0"

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"
"0"

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"
"0"

);

dash-number: (

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"

"1"
"2"
"3"
"4"
"5"
"6"
"7"
"8"
"9"

);

"0" | "0" | "0" | "0" |);

style-name: { any alpha numeric ASCII name not to exceed 8 characters in length};

case-name: { any alpha numeric ASCII name not to exceed 8 characters in length};

eia_jedec-name: { any alpha numeric ASCII name not to exceed 12 characters in length};

spec_type-name: { "ASSEM", "ARTWK", "SCHEM", "CMPSP", "NEXAS", "USEON" };

data_list_drawing-name: { any alpha numeric ASCII name not to exceed 18 characters in length};

max_body_dia-number: { f7.4-number };

iges_layer-name: { "00"["BATTE COMPONENTS"] |
"05"["CAP COMPONENTS"] |
"10"["CHEM COMPONENTS"] |
"15"["CON COMPONENTS"] |
"20"["CORE COMPONENTS"] |
"25"["HDWR COMPONENTS"] |
"30"["IND COMPONENTS"] |
"35"["LAMP COMPONENTS"] |
"40"["RES COMPONENTS"] |
"45"["ROTMAC COMPONENTS"] |
"50"["SEMI COMPONENTS"] |
"55"["SWTCH COMPONENTS"] |
"60"["TRADUC COMPONENTS"] |
"65"["UCTK COMPONENTS"] |
"70"["XFMR COMPONENTS"] |
"75"["SPECIAL ASSEMBLY BATTE COMPONENT BODIES"] |
"80"["SPECIAL ASSEMBLY CAP COMPONENTS"] |
"85"["SPECIAL ASSEMBLY CHEM COMPONENTS"] |
"90"["SPECIAL ASSEMBLY CON COMPONENTS"] |
"95"["SPECIAL ASSEMBLY CORE COMPONENTS"] |
"100"["SPECIAL ASSEMBLY HDWR COMPONENTS"] |
"105"["SPECIAL ASSEMBLY IND COMPONENTS"] |
"110"["SPECIAL ASSEMBLY LAMP COMPONENTS"] |
"115"["SPECIAL ASSEMBLY RES COMPONENTS"] |
"120"["SPECIAL ASSEMBLY ROTMAC COMPONENTS"] |
"125"["SPECIAL ASSEMBLY SEMI COMPONENTS"] |
"130"["SPECIAL ASSEMBLY SWTCH COMPONENTS"] |
"135"["SPECIAL ASSEMBLY TRADUC COMPONENTS"] |
"140"["SPECIAL ASSEMBLY UCKT COMPONENTS"] |
"145"["SPECIAL ASSEMBLY XMFR COMPONENTS"] |
"150"["SPECIAL INSTRUCTIONS"] |
"155"["MAXIMUM ASSEMBLY ENVELOPE"] |
"160"["CONFORMAL COAT MASK"] |

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```
"165"["ASSEMBLY INKING OR MASKING"] |  
"170"["ASSEMBLY DATA LIST"] |  
"180"["PWB"] );
```

10.4 CALS ATTRIBUTES

DECLARATION FILE

```
srcsys: { srcsys-name }  
srcdocid: { srcdocid-name }  
srcrelid: { srcrelid-name }  
chglvl: { chglvl-name }  
dteisu: { dteisu-date }  
dstsys: { dstsys-name }  
dstdocid: { cage-name }", "{ pn-name }", "{ rev-name }  
dstrelid: { dstrelid-name }  
dtetrn: { dtetrn-date }  
dlvacc: { dlvacc-number }  
filcnt: { filcnt-number }  
ttlcls: { ttlcls-name }  
doccls: { doccls-name }  
doctyp: { doctyp-name }  
doctl: { doctl-name }
```

IGES,EDIF,IPC-D-350 HEADER

```
srcdocid: { srcdocid-name }  
dstdocid: { igesipcedifdstdocid-name }  
txtfilid: { txtfilid-name }  
figid: { figid-name }  
srcgph: { srogph-name }  
doccls: { doccls-name }  
notes: { notes-name }
```

CCITTG4 HEADER

```
srcdocid: { srcdocid-name }  
dstdocid: { ccittg4srcdocid-name }  
txtfilid: { txtfilid-name }  
figid: { figid-name }  
srcgph: { srogph-name }  
doccls: { doccls-name }  
notes: { notes-name }
```

```
srcsys-name: { any alpha numeric ASCII name not to exceed 48 characters  
in length};  
igesipcedifsrcdocid-name: { any alpha/numeric 15 characters};  
ccittg4srcdocid-name: { "HOLLERITH CODE" };  
HOLLERITH CODE: { any ASCII character from the aperture card};  
srcrelid-name: { "NONE" };  
chglvl: { "ORIGINAL" |DOD-STD-100 CHANGE LETTER(S) }", "{ "VALIDATED"  
| "VERIFIED" }", "{(YYYYMMDD)}";
```

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```
dteisu-date : {YYYYMMDD};
dstsys-name: { any alpha numeric ASCII name not to exceed 15
               characters in length};
dstdocid-name: { drawing number comprised any alpha numeric ASCII name
                 not to exceed 15 characters in length };
dstrelid-name: { "NONE" };
dtetrn-date: { "NONE" };
dlvacc-number: { any alpha numeric ASCII name not to exceed 48
                 characters in length};
filcnt-code: { "Q"pos-integer | "I"pos-integer
               "E"pos-integer | "R"pos-integer
               "T"pos-integer };
pos-integer: { "1"
               "2"
               "3"
               "4"
               "5"
               "6"
               "7"
               "8"
               "9"
               "0" };
ttlcls-name: { any alpha numeric ASCII name not to exceed 15
               characters in length};
doccls-name: { any alpha numeric ASCII name not to exceed 15
               characters in length};
doctyp-name: { any alpha numeric ASCII name not to exceed 15
               characters in length};
docttl-name: { any alpha numeric ASCII name not to exceed 15
               characters in length};
txtfilid-name: { "NONE" };
figid-name: { "NONE" };
srogph-name: { "NONE" };
doccls-name: { any alpha numeric ASCII name not to exceed 15
               characters in length};
notes-name: { "any alpha numeric ASCII name representing the
               manufacture of the translator used", "any alpha numeric
               ASCII name representing the Industry Standard Specification
               version", "any alpha numeric ASCII name representing the
               manufacture's translator version" };
```

END FORMAL SYNTAX

APPENDIX II20.0 COMPONENT ORIENTATION VECTOR20.1 ORIENTATION VECTOR

The Component Orientation Vector is provided in the RAMP PWA product data in both the "as-assembled" and "as-received" models of each component of the PWA. This vector can be used to determine the orientation of the component with respect to the PWB as shown in Appendix II, Figure II-1. This vector has its origin as the component's computed center-of-mass and its end point at $.1i + .1j + .1k$ where i, j , and k are unit vectors along the x, y , and z axes respectively. The component "as-received" model is created using the following rules for determining its x, y, z coordinate system:

- 1) A reference orientation of the component is established which conforms to the most mechanically stable or usual mounting position for that component on an imaginary PWB.
- 2) The z axis is then established, for the component, at right angles to the imaginary PWB. Positive z values increase in a direction away from the imaginary PWB.
- 3) The y axis is then established at right angles to the z axis and in the plane of the imaginary PWB and along the longest package dimension (sometimes called the length).
- 4) The x axis is then established at right angles to both the y and z axes and usually is along the shortest body dimension (sometimes called the width).
- 5) The center-of-mass for the component's body is computed as is used as the orientation vector's starting point.
- 6) The vector is then created as follows:

To the center-of-mass point (X_c, Y_c, Z_c) add $.1$ unit in each direction to get the vector's end point $(X_c + .1, Y_c + .1, Z_c + .1)$. The orientation vector is, therefore, described by:

$$V_{cmp} = ((X_c + .1) - X_c)i + ((Y_c + .1) - Y_c)j + ((Z_c + .1) - Z_c)k \text{ or}$$

$$V_{cmp} = .1i + .1j + .1k \text{ with respect to the component's center-of-mass.}$$

The following equations can be used to determine the orientation of the component with respect to the PWB.

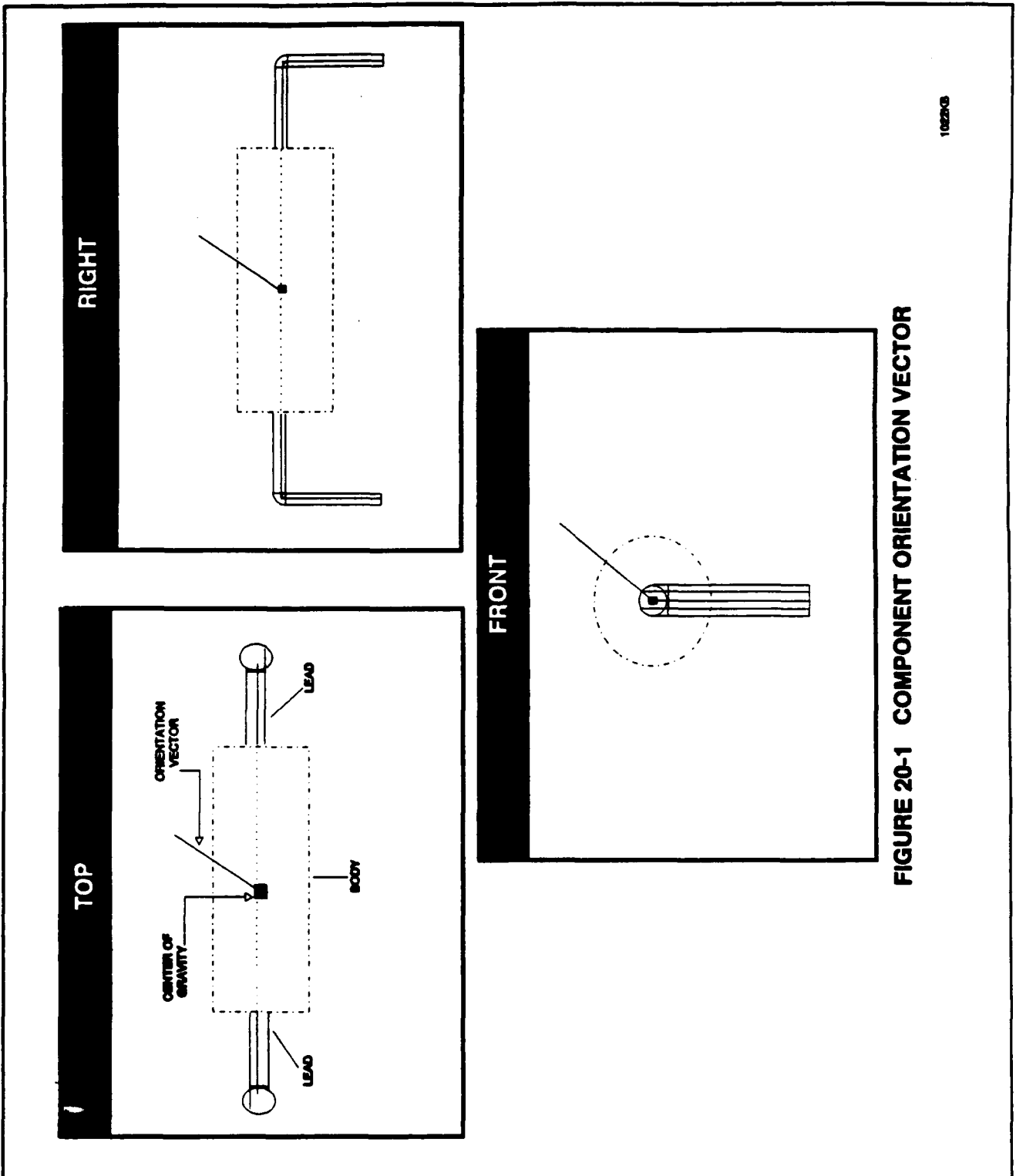


FIGURE 20-1 COMPONENT ORIENTATION VECTOR

When the component is placed on the PWB to form the assembly its center-of-mass takes on a new location (X_p, Y_p, Z_p) with respect to the PWB's coordinate system and the component's orientation vector takes on a new direction given by:

$V_{cmp}' = (X_o - X_p)i + (Y_o - Y_p)j + (Z_o - Z_p)k$ where X_o, Y_o, Z_o is the new vector end point with respect to the PWB's origin.

To compute the component orientation the following relationships need to be computed using the PWB orientation vector V_{pwb} and the component's orientation vector V_{cmp}' :

For rotation about the Z axis in degrees:

for $(X_o - X_p) \geq 0$,

$$\theta_z = \text{Arc sin} [(10 * (Y_o - Y_p)) / \sqrt{2}] - 45^\circ$$

for $(X_o - X_p) < 0$,

$$\theta_z = 180^\circ - \{ \text{Arc sin} [(10 * (Y_o - Y_p)) / \sqrt{2}] \} - 45^\circ$$

For rotation about the X axis in degrees:

for $(Y_o - Y_p) \geq 0$,

$$\theta_x = \text{Arc sin} [(10 * (Z_o - Z_p)) / \sqrt{2}] - 45^\circ$$

for $(Y_o - Y_p) < 0$,

$$\theta_x = 180^\circ - \{ \text{Arc sin} [(10 * (Z_o - Z_p)) / \sqrt{2}] \} - 45^\circ$$

For rotation about the Y axis in degrees:

for $(Z_o - Z_p) \geq 0$,

$$\theta_y = \text{Arc sin} [(10 * (X_o - X_p)) / \sqrt{2}] - 45^\circ$$

for $(Z_o - Z_p) < 0$,

$$\theta_y = 180^\circ - \{ \text{Arc sin} [(10 * (X_o - X_p)) / \sqrt{2}] \} - 45^\circ$$

Where a positive rotation is counter clockwise from the component side of the board. θ_z represents the component's rotation in a plane parallel to the PWB surface. θ_x and θ_y are the component's rotation about axes in the PWB's plane.

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CLASS	SUB	PTYPE	PKG	DESCRIPTION
-----	-----	-----	-----	-----
BATTE	NONR	ALKA	AXIAL	ALKALINE NONRECHARGABLE BATTERY
			CAN	
	NONR	CARB	AXIAL	CARBON NONRECHARGABLE BATTERY
			CAN	
	RECH	LDAC	AXIAL	LEAD ACID RECHARGEABLE BATTERY
			CAN	
	RECH	NICAD	AXIAL	NICKEL CADMIUM RECHARGEABLE BATTERY
			CAN	
CAP	FIXED	CAP	AXIAL	CAPACITOR
			CHIP	
			RDL	
		DIPCAP	DIP	CAPACITOR
		PCA	AXIAL	POLARIZED CAPACITOR
			CHIP	
			RDL	
		TCA	AXIAL	TANTALUM CAPACITOR
			CHIP	
			RDL	
	VAR	CAP	RDL	CAPACITOR
CHEM	BAGT	BAGT		BONDING AGENT
	CAGT	CAGT		COMPOUND AGENT
	CLAGT	CLAGT		CLEANING AGENT
	IAGT	IAGT		INSULATING AGENT
	MAGT	MAGT		MARKING AGENT
	TAGT	TAGT		THERMAL AGENT
CON	ANTEN	DIPOL		ANTENNA

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CLASS	SUB	PTYPE	PKG	DESCRIPTION
		MONPO		
	BUSBR	BUSBR		BUSBAR
	EDGE	EDGE	RDL	EDGE CONNECTOR
			SM	
	FUSE	FUSE	RDL	FUSE
	JUM	JUM		JUMPER
		OPJ		OPEN JUMPER
		COAX		COAXIAL CABLE
		WAVG		WAVEGUIDE
	PLUG	TPCP	RDL	TWO PART CONNECTOR PIN
			SM	
	RECPT	TPCS	RDL	TWO PART CONNECTOR SOCKET
			SM	
	TERM	PIS	RDL	PACKAGING/INTERCONNECTING STRUCTURE
			SM	
	TERMT	TERMT	RDL	TERMINAL BOARD STRIP
			SM	
	TERMP	TERMP	RDL	TERMINAL STRAP
			SM	
	TESTB	TESTB	RDL	TEST BLOCK
			SM	
CORE	FEED	FEED		FERRITE BEAD CORE
IND	FIXED	IND	AXIAL	INDUCTOR
			CHIP	
			RADIAL	
	VAR	IND	RDL	INDUCTOR
LAMP	FLUOR	FLOUR		FLUORESCENT LAMP
	GLOW	GLOW		GLOW COLD CATHODE LAMP

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CLASS	SUB	PTYPE	PKG	DESCRIPTION
	INCAN BALLA	INCAN BALLA		INCANDESCENT BALLAST LAMP
HDWR	BOLT	BOLT		BOLT
	BRACK	BRACK		BRACKET
	BRVT	BRVT		BLIND RIVET
	CLAMP	CLAMP	MTCLP	METAL CLAMP
			PLCLP	PLASTIC CLAMP
	CRVT	CRVT		COUNTERSINK RIVET
	CLIP	CLIP	MCLIP	METAL CLIP
			PCLIP	PLASTIC CLIP
	EJECT	EJECT		EJECTOR
	EYELE	EYELE		EYELET
	FRAME	FRAME		FRAME
	FWSHR	FWSHR		FLATWASHER
	LWSHR	LWSHR		LOCKWASHER
	HANDL	HANDL	HANDL	HANDLE
			LOBAR	LOCKING BAR
			PUBAR	PULL BAR
	INSUL	INSUL	DISK	DISK INSULATOR
			PAD	PAD INSULATOR
			PLATE	PLATE INSULATOR
			WASHR	WASHER INSULATOR
	NUT	NUT		NUT
	PIN	PIN	ALIGN	ALIGNMENT PIN
			SPRIN	SPRING PIN
	RRING	RRING		RETAINING RING
	TIES	TIES	PTIES	PLASTIC TIES
	TIES	TIES	STIES	STRING TIES
	TRVT	TRVT		TUBULAR RIVET
	SCREW	SCREW		SCREW

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CLASS	SUB	PTYPE	PKG	DESCRIPTION
	SHIEL	SHIEL		SHIELD
	SLEEV	SLEEV	TUBE	SLEEVE TUBULAR
			HTSRK	HEAT SHRINK SLEEVING
	SPACE	SPACE		SPACER
	SPREA	SPREA		SPREADER
	SPRIN	SPRIN	COMPSP	COMPRESSION SPRING
			TENSP	TENSION SPRING
			THERMS	THERMAL PRESSURE SPRING
	VAR	IND	RDL	INDUCTOR
PWB	FLEX	FLEX	PWB	PRINTED WIRING BOARD
	HYB	HYB	PWB	PRINTED WIRING BOARD
	MOLD	MOLD	PWB	PRINTED WIRING BOARD
	RFLEX	RFLEX	PWB	PRINTED WIRING BOARD
	RIGID	RIGID	PWB	PRINTED WIRING BOARD
RES	FIXED	RES		RESISTOR
		RP_DH		RESISTOR PACK DIP HYBRID
		RP_DB		RESISTOR PACK DIP BUSSED
		RP_DI		RESISTOR PACK DIP ISOLATED
		RP_SB		RESISTOR PACK SIP BUSSED
		RP_SI		RESISTOR PACK SIP ISOLATED
		RP_ST		RESISTOR PACK SIP TERMINATED
		RP_SH		RESISTOR PACK SIP HYBRID
		RP_DT		RESISTOR PACK DIP TERMINATED
	VAR	RHE		RHEOSTAT
		POT		POTENTIOMETER
		TMSTR		THERMISTOR

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CLASS	SUB	PTYPE	PKG	DESCRIPTION
ROTMA	ACMAC	ACMAC		AC ROTATING MACHINERY
	DCMAC	DCMAC		DC ROTATING MACHINERY
	SYNCH	SYNCH		SYNCHRONOUS
SEMI	DIODE	BIZ		BIZENER
		BDIO		BRIDGE DIODE
		DIO		DIODE
		PSD		PHOTO SENSITIVE DIODE
		PED		PHOTO EMISSIVE DIODE (LED)
		TDI		TUNNEL DIODE
		TYSTR		THYRISTOR DIODE
		TYSTL		LIGHT ACTIVATED THYRISTOR DIODE
		TRANO		TRANSORBE
		ZDI		ZENER DIODE
	SCR	SCR		SILICON CONTROLLED RECTIFIER
	TRANS	DARP		DARLINGTON P JUNCTION TRANSISTORS
		DARN		DARLINGTON N JUNCTION TRANSISTORS
		FETP		FIELD EFFECT P CHANNEL TRANSISTOR
		FETN		FIELD EFFECT N CHANNEL TRANSISTOR
		OCPL		OPTICAL COUPLER TRANSISTORS
		TRNN		NPN JUNCTION TRANSISTOR
		TRNP		PNP JUNCTION TRANSISTOR
		UNIP		UNIUNCTION NP..N JUNCTION TRANSISTOR
		UNIN		UNIUNCTION PN..P JUNCTION TRANSISTOR
SWTCH	RELAY	CKTB		CIRCUIT BREAKER
		RCL		RELAY COIL
		RCNC		RELAY CONTACT NORMALLY OPEN
		RCNC		RELAY CONTACT NORMALLY CLOSED
	SWTCH	CSW		CLOSED SWITCH

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CLASS	SUB	PTYPE	PKG	DESCRIPTION
		OSW		OPEN SWITCH
TRADU	BELL	BELL		BELL TRANSDUCER
	MIC	MIC		MICROPHONE TRANSDUCER
	HALL	HALL		HALL EFFECT TRANSDUCER
	SPK	SPK		SPEAKER TRANSDUCER
	XTL	XTL	RDL	CRYSTAL
UCTT	DIG	LSI	CAN	LARGE SCALE INTEGRATION
			COB	CHIP ON BOARD
			DIP	DUAL INLINE PACKAGE
			FP	FLAT PACK
			GCC	GULL CHIP CARRIER
			JCC	J BEND CHIP CARRIER
			LCC	LEADLESS CHIP CARRIER
			PGA	PIN GRID ARRAY
			SOIC	SMALL OUTLINE INTEGRATED CIRCUIT
			TAB	TAPE AHESION
		MSI	DIP	MEDIUM SCALE INTEGRATION
			COB	CHIP ON BOARD
			DIP	DUAL INLINE PACKAGE
			FP	FLAT PACK
			GCC	GULL CHIP CARRIER
			JCC	J BEND CHIP CARRIER
			LCC	LEADLESS CHIP CARRIER
			PGA	PIN GRID ARRAY
			SOIC	SMALL OUTLINE INTEGRATED CIRCUIT
			TAB	TAPE AUTOMATING BONDING
		VLSI	DIP	VERY LARGE SCALE INTEGRATION
			COB	CHIP ON BOARD
			DIP	DUAL INLINE PACKAGE

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CLASS	SUB	PTYPE	PKG	DESCRIPTION	
			FP	FLAT PACK	
			GCC	GULL CHIP CARRIER	
			JCC	J BEND CHIP CARRIER	
			LCC	LEADLESS CHIP CARRIER	
			PGA	PIN GRID ARRAY	
			SOIC	SMALL OUTLINE INTEGRATED CIRCUIT	
			TAB	TAPE AUTOMATING BONDING	
		VHSIC	DIP	VERY HIGH SPEED INTEGRATED CIRCUIT	COB
			DIP	DUAL INLINE PACKAGE	
			FP	FLAT PACK	
			GCC	GULL CHIP CARRIER	
			JCC	J BEND CHIP CARRIER	
			LCC	LEADLESS CHIP CARRIER	
			PGA	PIN GRID ARRAY	
			SOIC	SMALL OUTLINE INTEGRATED CIRCUIT	
			TAB	TAPE AUTOMATING BONDING	
		SSI	DIP	SMALL SCALE INTEGRATION	
			COB	CHIP ON BOARD	
			DIP	DUAL INLINE PACKAGE	
			FP	FLAT PACK	
			GCC	GULL CHIP CARRIER	
			JCC	J BEND CHIP CARRIER	
			LCC	LEADLESS CHIP CARRIER	
			PGA	PIN GRID ARRAY	
			SOIC	SMALL OUTLINE INTEGRATED CIRCUIT	
			TAB	TAPE AUTOMATING BONDING	
	HYB	CUST	DIP	CUSTOM INTEGRATED CIRCUIT	
			COB	CHIP ON BOARD	

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CLASS	SUB	PTYPE	PKG	DESCRIPTION	-----
-----	-----	-----	-----	-----	-----
			DIP	DUAL INLINE PACKAGE	
			FP	FLAT PACK	
			GCC	GULL CHIP CARRIER	
			JCC	J BEND CHIP CARRIER	
			LCC	LEADLESS CHIP CARRIER	
			PGA	PIN GRID ARRAY	
			SOIC	SMALL OUTLINE INTEGRATED CIRCUIT	
			TAB	TAPE AUTOMATING BONDING	
	LIN	ANA	DIP	ANALOG INTEGRATED CIRCUIT	
			COB	CHIP ON BOARD	
			DIP	DUAL INLINE PACKAGE	
			FP	FLAT PACK	
			GCC	GULL CHIP CARRIER	
			JCC	J BEND CHIP CARRIER	
			LCC	LEADLESS CHIP CARRIER	
			PGA	PIN GRID ARRAY	
			SOIC	SMALL OUTLINE INTEGRATED CIRCUIT	
			TAB	TAPE AUTOMATING BONDING	
	MIXED	ANA	DIP	ANALOG INTEGRATED CIRCUIT	
			COB	CHIP ON BOARD	
			DIP	DUAL INLINE PACKAGE	
			FP	FLAT PACK	
			GCC	GULL CHIP CARRIER	
			JCC	J BEND CHIP CARRIER	
			LCC	LEADLESS CHIP CARRIER	
			PGA	PIN GRID ARRAY	
			SOIC	SMALL OUTLINE INTEGRATED CIRCUIT	
			TAB	TAPE AUTOMATING BONDING	
XFMR	POWER	TRAP	RDL	TRANSFORMER	
	SIGNL	TRAS	RDL	TRANSFORMER	

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APPENDIX IV

40.0 DATA LIST

40.1 DATA LIST

DOCTYP	DOCNUM	DESCRIPTION
-----	-----	-----
ASSEM	DRAWING NUMBER	ASSEMBLY DOCUMENT NUMBER
PWBSP	DRAWING NUMBER	PWB DOCUMENT NUMBER
PROG	DRAWING NUMBER	PROGRAM DOCUMENT NUMBER
PROSP	DRAWING NUMBER	PROCESS DOCUMENT
SCHEM	DRAWING NUMBER	SCHEMATIC DOCUMENT NUMBER
TSTSP	DRAWING NUMBER	TEST DOCUMENT NUMBER
CMPSP	DRAWING NUMBER	COMPONENT SPECIFICATION
NEXAS	DRAWING NUMBER	NEXT ASSEMBLY
USEON	DRAWING NUMBER	USED ON

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APPENDIX V
50.0 TRR COMPONENT ATTRIBUTES

50.1 EDIF SCHEMATIC COMPONENT ATTRIBUTES

EDIF component attributes are those component attributes that are defined as properties of a schematic component symbol. The BNF description of these attributes is as follows:

```
comp-model: { comp-spec  
              comp-class  
              comp-prop  
              comp-geom };
```

```
comp-class: { "CLASS" class-name };
```

```
class-name: { "CAP"  
              cap-sub-name  
              pkg-name |  
              "CONN"  
              conn-sub-name  
              pkg-name |  
              "IND"  
              ind-sub-name  
              pkg-name |  
              "OTHER"  
              other-sub-name  
              pkg-name |  
              "PWB"  
              pwb-sub-name  
              pkg-name |  
              "RES"  
              res-sub-name  
              pkg-name |
```

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"SEMI"
semi-sub-name
pkg-name |
"SWTCH"
swtch-sub-name
pkg-name |
"UCT"
uct-sub-name
pkg-name |
"XFMR"
xfmr-sub-name);
pkg-name ;
"XTL"
xtl-sub-name
pkg-name |

cap-sub-name: { "FIXED" | "VAR" };

res-sub-name: { "FIXED" | "VAR" };

conn-sub-name: { "PLUG" | "RECPT" | "EDGE" | "TERM" |
"TP" | "KEY" | "ADAPT" };

ind-sub-name: { "FIXED" | "VAR" };

other-pkg-name: { "SCREW" | "BOLT" | "NUT" | "RIVET" |
"FWSHR" | "LWSHR" | "BAGT" | "CAGT" | "MAGT" };

pwb-sub-name: { "FLEX" | "HYB" | "MOLD" | "RFLEX" |
"RIGID" };

semi-sub-name: { "LED" | "DIODE" | "TRANS" | "VRSTR" |
"TMSTR" | "TYSTR" | "OCPL" };

swtch-sub-name: { "SWTCH" | "RELAY" };

uckt-sub-name: { "LIN" | "DIG" };

xfmr-sub-name: { "POWER" | "SIGNAL" };

pwb-pkg-name: { "TYPE1" | "TYPE2" | "TYPE3" | "TYPE4" | "TYPE5" | "TYPE6" };

pkg-name: { "AXIAL" | "CAN" | "CHIP" | "RDL" | "SM" | "SM" | "PLCLP" |
"MTCLP" | "PCLIP" | "HANDL" | "LOBAR" | "PUBAR" | "DISK" |
"PAD" | "PLATE" | "WASHR" | "ALIGN" | "SPRIN" | "PTIES" |
"STIES" | "TUBE" | "HTSRK" | "COMPS" | "TENS" | "THERS" };

attribute_name: "PTYPE" ptype-name
"RDES" rdes-name
["CHTYP_VAL" chtyp_val-name]
["CHTYP_PTL" chtyp_ptl-name]
["CHTYP_NTL" chtyp_ntl-name]
"GPN" gpn-name
["CHTYP_LT" chtyp_lt-name]
"AP_SPEC" ap_spec-name
"PN" pn-name
"ITEM" item-name
["CAGE" cage-name]
["MAX_WK_VOLT" max_wk_volt-name]
["COMP_PWR" comp_pwr-name]
["SOLDERABILITY" solderability-name]
["LEAD_MAT" lead_mat-name]
["LEAD_PLT" lead_plt-name]
["REV" rev-name]

50.2 IGES 3D COMPONENT ATTRIBUTES IN IGES HEADER

IGES 3D component attributes are those component attributes that are defined as properties of a 3D component.

"SPEC" spec-name
["SNUM" snum-name]
["DNUM" dnum-name]
["STYLE" style-name]
["CASE" case-name]
["AP_SPEC" ap_spec-name]
["EIA_JEDEC" eia_jedec-name]
"CLASS" class-name
"SUB" sub-name
"PKG" pkg-name
["Qty" qty-name]
["MAX_WK_VOLT" max_wk_volt-name]
["COMP_PWR" comp_pwr-name]
["SOLDERABILITY" solderability-name]
["LEAD_MAT" lead_mat-name]
["LEAD_PLT" lead_plt-name]
"MAX_BODY_DIA" max_body_dia-number
"NOM_BODY_DIA" nom_body_dia-number
"MIN_BODY_DIA" min_body_dia-number
"MAX_BODY_LEN" max_body_len-number
"NOM_BODY_LEN" nom_body_len-number
"MIN_BODY_LEN" min_body_len-number
"MAX_BODY_WDT" max_body_wdt-number
"NOM_BODY_WDT" nom_body_wdt-number
"MIN_BODY_WDT" min_body_wdt-number
"MAX_BODY_HGT" max_body_hgt-number
"NOM_BODY_HGT" nom_body_hgt-number
"MIN_BODY_HGT" min_body_hgt-number
"MAX_LEAD_DIA" max_lead_dia-number

"NOM_LEAD_DIA" nom_lead_dia-number
 "MIN_LEAD_DIA" min_lead_dia-number
 "MAX_LEAD_LEN" max_lead_len-number
 "NOM_LEAD_LEN" nom_lead_len-number
 "MIN_LEAD_LEN" min_lead_len-number
 "MAX_LEAD_WDT" max_lead_wdt-number
 "NOM_LEAD_WDT" nom_lead_wdt-number
 "MIN_LEAD_WDT" min_lead_wdt-number
 "MAX_LEAD_THK" max_lead_thk-number
 "NOM_LEAD_THK" nom_lead_thk-number
 "MIN_LEAD_THK" min_lead_thk-number

50.3 COMPONENT ATTRIBUTE DATA FORMAT

ptype-name: { "ANA" "BIZ" | "CAP" | "CSW" | "CUST" | "ZDI" |
 "DAR" | "DIO" | "DIPCAP" | "EDG" | "FET" | "FUS" | "HYB" |
 "IND" | "JUM" | "LED" | "LSI" | "MSI" | "OPJ" | "OSW" |
 "PCA" | "PWB" | "PIS" | "POT" |
 "PWB" | "RCL" | "RCNO" | "RCNC" | "RES" | "RHE" |
 "RP_DB" | "RP_DH" | "RP_DI" | "RP_DT" | "RP_SB" |
 "RP_SH" | "RP_SI" | "RP_ST" | "SCR" | "SSI" |
 "TCA" | "TCP" | "TPCS" | "TRA" | "TRNN" |
 "TRNP" | "UNI" | "VHSIC" | "VLSI" | "XTL" | "ZDI"};

rdes-name: { any alpha-numeric ASCII character not to exceed 8
 characters in length};

f4-number: { "1" | "1" | "1" | "1" |
 "2" | "2" | "2" | "2" |
 "3" | "3" | "3" | "3" |
 "4" | "4" | "4" | "4" |
 "5" | "5" | "5" | "5" |
 "6" | "6" | "6" | "6" |
 "7" | "7" | "7" | "7" |

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```
"8" | "8" | "8" | "8" |  
"9" | "9" | "9" | "9" |  
"0" | "0" | "0" | "0" | );
```

pos-integer: { "1" | "2" | "3" | ...};

val-multiplier: { "T" | "G" | "M" | "K" | "m" | "u" | "n" | "p" | "P"};

chtyp_ntl-name: percent;

chtyp_ptl-name: percent;

```
percent: { "1" | "1" | "1" | "." | "1" |  
          "2" | "2" | "2" | "." | "2" |  
          "3" | "3" | "3" | "." | "3" |  
          "4" | "4" | "4" | "." | "4" |  
          "5" | "5" | "5" | "." | "5" |  
          "6" | "6" | "6" | "." | "6" |  
          "7" | "7" | "7" | "." | "7" |  
          "8" | "8" | "8" | "." | "8" |  
          "9" | "9" | "9" | "." | "9" |  
          "0" | "0" | "0" | "." | "0" | );
```

gpn-name: { any alpha numeric ASCII name not to exceed 15
characters in length};

```
chtyp_lt-name: { "ALU" | "ANA" | "CLK" | "CNT" | "COM" |  
                "DMUX" | "DRAM" | "HYB" | "MUX" | "PIO" |  
                "PLD" | "RAM" | "ROM" | "SEQ" | "SRAM" | };
```

ap_spec-name: { any alpha-numeric ASCII name not to exceed 15
characters in length};

pn-name: { any alpha-numeric ASCII name not to exceed 18 characters in
length};

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qnty-name: { f3-number | "NS" | "AR" | IN | FT | OZ | LB | EA
| CM | KM | MM | L | ML | PT | QT | GAL };

item-name: { f4-number };

cage-name: { f5-number };

f5-number: { "1" | "1" | "1" | "1" | "1" |
"2" | "2" | "2" | "2" | "2" |
"3" | "3" | "3" | "3" | "3" |
"4" | "4" | "4" | "4" | "4" |
"5" | "5" | "5" | "5" | "5" |
"6" | "6" | "6" | "6" | "6" |
"7" | "7" | "7" | "7" | "7" |
"8" | "8" | "8" | "8" | "8" |
"9" | "9" | "9" | "9" | "9" |
"0" | "0" | "0" | "0" | "0" | };

f15-number:

{ "1" | "1" | "1" | "1" | "1" | "1" | "1" | "1" |
"2" | "2" | "2" | "2" | "2" | "2" | "2" | "2" |
"3" | "3" | "3" | "3" | "3" | "3" | "3" | "3" |
"4" | "4" | "4" | "4" | "4" | "4" | "4" | "4" |
"5" | "5" | "5" | "5" | "5" | "5" | "5" | "5" |
"6" | "6" | "6" | "6" | "6" | "6" | "6" | "6" |
"7" | "7" | "7" | "7" | "7" | "7" | "7" | "7" |
"8" | "8" | "8" | "8" | "8" | "8" | "8" | "8" |
"9" | "9" | "9" | "9" | "9" | "9" | "9" | "9" |
"0" | "0" | "0" | "0" | "0" | "0" | "0" | "0" | ..5);

max_wk_volt-name : { f7.4-number };

f7-number:

```
{ "1" | "1" | "1" | "1" | "1" | "1" | "1" | "1" |  
  "2" | "2" | "2" | "2" | "2" | "2" | "2" | "2" |  
  "3" | "3" | "3" | "3" | "3" | "3" | "3" | "3" |  
  "4" | "4" | "4" | "4" | "4" | "4" | "4" | "4" |  
  "5" | "5" | "5" | "5" | "5" | "5" | "5" | "5" |  
  "6" | "6" | "6" | "6" | "6" | "6" | "6" | "6" |  
  "7" | "7" | "7" | "7" | "7" | "7" | "7" | "7" |  
  "8" | "8" | "8" | "8" | "8" | "8" | "8" | "8" |  
  "9" | "9" | "9" | "9" | "9" | "9" | "9" | "9" |  
  "0" | "0" | "0" | "0" | "0" | "0" | "0" | "0" |..15};
```

comp_pwr-name: { f7-number };

solderability-name : { "NIL" | "NOWAV" | "NRFLO" };

lead_mtl-name: { "STL" | "OTH" };

lead_plt-name: { "GLD" | "OTH" };

rev-name: { DOD-STD-100 change letters length};

spec-name: { any alpha numeric ASCII name not to exceed 15 characters
in length};

snum-name: { any alpha numeric ASCII name not to exceed 4 characters
in length};

dnum-name: { any alpha numeric ASCII name not to exceed 4 characters
in length};

style-name: { any alpha numeric ASCII name not to exceed 8 characters
in length};

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case-name: { any alpha numeric ASCII name not to exceed 8
characters in length};

eia_jedec-name: { any alpha numeric ASCII name not to exceed 4
characters in length};

nom_body_dia-number: { f7.4-number };

min_body_dia-number: { f7.4-number };

max_body_len-number: { f7.4-number };

nom_body_len-number: { f7.4-number };

min_body_len-number: { f7.4-number };

max_body_wdt-number: { f7.4-number };

nom_body_wdt-number: { f7.4-number };

min_body_wdt-number: { f7.4-number };

max_body_hgt-number: { f7.4-number };

nom_body_hgt-number: { f7.4-number };

min_body_hgt-number: { f7.4-number };

max_lead_dia-number: { f7.4-number };

nom_lead_dia-number: { f7.4-number };

min_lead_dia-number: { f7.4-number };

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max_lead_len-number: { f7.4-number };

nom_lead_len-number: { f7.4-number };

min_lead_len-number: { f7.4-number };

max_lead_wdt-number: { f7.4-number };

nom_lead_wdt-number: { f7.4-number };

min_lead_wdt-number: { f7.4-number };

max_lead_thk-number: { f7.4-number };

nom_lead_thk-number: { f7.4-number };

min_lead_thk-number: { f7.4-number };

f7.4-number: { "1" | "1" | "1" | "." | "1" | "1" | "1" | "1" |
"2" | "2" | "2" | "." | "2" | "2" | "2" | "2" |
"3" | "3" | "3" | "." | "3" | "3" | "3" | "3" |
"4" | "4" | "4" | "." | "4" | "4" | "4" | "4" |
"5" | "5" | "5" | "." | "5" | "5" | "5" | "5" |
"6" | "6" | "6" | "." | "6" | "6" | "6" | "6" |
"7" | "7" | "7" | "." | "7" | "7" | "7" | "7" |
"8" | "8" | "8" | "." | "8" | "8" | "8" | "8" |
"9" | "9" | "9" | "." | "9" | "9" | "9" | "9" |
"0" | "0" | "0" | "." | "0" | "0" | "0" | "0" | };
name" | "any alpha numeric ASCII name");

END FORMAL SYNTAX

APPENDIX VI
60.0 TRR IGES LAYERING CONVENTION

TABLE FOR TRR
IGES LAYERING CONVENTION

Assembly Layers:

LAYER 00
LAYER 05 CAP
LAYER 10 GLUE
LAYER 15
LAYER 20
LAYER 25 OTHER
LAYER 30 IND
LAYER 35
LAYER 40 RES
LAYER 45
LAYER 50 SEMI
LAYER 55 SWTCH
LAYER 60 XTL
LAYER 65 UCKT
LAYER 70 XFMR
LAYER 75
LAYER 79
LAYER 80 SPECIAL ASSEMBLY CAP
LAYER 84 SPECIAL ASSEMBLY CAP INSTRUCTIONS
LAYER 85
LAYER 89
LAYER 90 SPECIAL ASSEMBLY CONN
LAYER 94 SPECIAL ASSEMBLY CONN INSTRUCTIONS
LAYER 95
LAYER 99
LAYER 100 SPECIAL ASSEMBLY OTHER
LAYER 104 SPECIAL ASSEMBLY OTHER INSTRUCTIONS
LAYER 105 SPECIAL ASSEMBLY IND
LAYER 109 SPECIAL ASSEMBLY IND INSTRUCTIONS
LAYER 110
LAYER 114
LAYER 115 SPECIAL ASSEMBLY RES
LAYER 119 SPECIAL ASSEMBLY RES INSTRUCTIONS
LAYER 120 SPECIAL ASSEMBLY ROTMA
LAYER 124 SPECIAL ASSEMBLY ROTMA INSTRUCTIONS
LAYER 125 SPECIAL ASSEMBLY SEMI
LAYER 129 SPECIAL ASSEMBLY SEMI INSTRUCTIONS
LAYER 130 SPECIAL ASSEMBLY SWTCH
LAYER 134 SPECIAL ASSEMBLY SWTCH INSTRUCTIONS
LAYER 135 SPECIAL ASSEMBLY XLT

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APPENDIX VII
70.0 TRR RPTS TO RAMP PWA FACTORY MAPPING

<u>CLASS</u>	<u>RPTS</u>	<u>SUB</u>	<u>CLASS</u>	<u>RAMP PWA FACTORY</u> <u>SUB</u>	<u>PKG</u>
BATTE		NONR	OTHER	HDWR	OTHER
BATTE		RECH	OTHER	HDWR	OTHER
CAP		FIXED	CAP	FIXED	
CAP		VAR	CAP	VAR	
CHEM		BAGT	OTHER	BAGT	OTHER
CHEM		CAGT	OTHER	CAGT	OTHER
CHEM		CLAGT	OTHER	OTHER	OTHER
CHEM		IAGT	OTHER	IAGT	OTHER
CHEM		MAGT	OTHER	MAGT	OTHER
CHEM		TAGT	OTHER	TAGT	OTHER
CON		ANTENNA	OTHER	OTHER	OTHER
CON		BUSBAR	CONN	OTHER	OTHER
CON		EDGE	CONN	EDGE	OTHER
CON		FUSE	OTHER	OTHER	
CON		JUM	CONN	OTHER	
CON		PLUG	CONN	PLUG	
CON		RECEPT	CONN	RECEPT	
CON		TERM	CONN	TERM	
CON		TERMST	OTHER	OTHER	OTHER
CON		TERMSP	OTHER	OTHER	OTHER
CON		TESTBK	OTHER	OTHER	OTHER
CORE		FEBED	OTHER	OTHER	OTHER
IND		FIXED	IND	FIXED	
IND		VAR	IND	VAR	
LAMP		FLOUR	OTHER	OTHER	OTHER
LAMP		GLOW	OTHER	OTHER	OTHER
LAMP		INCAN	OTHER	OTHER	OTHER
LAMP		BALLA	OTHER	OTHER	OTHER
HDWR		BOLT	OTHER	HDWR	BOLT
HDWR		BRACK	OTHER	HDWR	BRACK
HDWR		BRVT	OTHER	HDWR	BRVT
HDWR		CRVT	OTHER	HDWR	CRVT
HDWR		CLIP	OTHER	HDWR	CLIP
HDWR		EJECT	OTHER	HDWR	EJECT
HDWR		EYELE	OTHER	HDWR	EYELE
HDWR		FRAME	OTHER	HDWR	FRAME

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TABLE FOR TRR (CONT'D) IGES LAYERING CONVENTION	
LAYER 139	SPECIAL ASSEMBLY XTL INSTRUCTIONS
LAYER 140	SPECIAL ASSEMBLY UCKT
LAYER 144	SPECIAL ASSEMBLY UCKT INSTRUCTIONS
LAYER 145	SPECIAL ASSEMBLY XMFR
LAYER 149	SPECIAL ASSEMBLY XMFR INSTRUCTIONS
LAYER 150	SPECIAL GENERAL INSTRUCTIONS
LAYER 155	MAXIMUM ASSEMBLY ENVELOPE
LAYER 160	CONFORMAL COAT MASK
LAYER 165	ASSEMBLY INKING OR MARKING
LAYER 170	ASSEMBLY DATA LIST
LAYER 180	PWB

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<u>RPTS</u>		<u>RAMP PWA FACTORY</u>		
<u>CLASS</u>	<u>SUB</u>	<u>CLASS</u>	<u>SUB</u>	<u>PKG</u>
HDWR	FWSHR	OTHER	OTHER	FWSHR
HDWR	LWSHR	OTHER	HDWR	LWSHR
HDWR	HANDL	OTHER	HDWR	HANDL
HDWR	NUT	OTHER	HDWR	NUT
HDWR	PIN	OTHER	HDWR	PIN
HDWR	TRVT	OTHER	HDWR	TRVT
HDWR	SCREW	OTHER	HDWR	SCREW
HDWR	SHIEL	OTHER	HDWR	SHIEL
HDWR	SPRIN	OTHER	HDWR	SPRIN
PWB	FLEX	PWB	FLEX	
PWB	HYB	PWB	HYB	
PWB	MOLD	PWB	MOLD	
PWB	RFLEX	PWB	RFLEX	
PWB	RIGID	PWB	RIGID	
RES	FIXED	RES	FIXED	
RES	VAR	RES	VAR	
ROTMA	ACMAC	OTHER	OTHER	OTHER
ROTMA	DCMAC	OTHER	OTHER	OTHER
ROTMA	SYNCH	OTHER	OTHER	OTHER
SEMI	DIODE	SEMI	DIODE	
SEMI	SCR	SEMI	DIODE	
SEMI	TRANS	SEMI	TRANS	
SWTCH	RELAY	SWTCH	RELAY	
SWTCH	SWTCH	SWTCH	SWTCH	
TRADUC	BELL	OTHER	OTHER	OTHER
TRADUC	MIC	OTHER	OTHER	OTHER
TRADUC	HALL	OTHER	OTHER	OTHER
TRADUC	SPK	OTHER	OTHER	OTHER
TRADUC	XTL	XTAL	XTAL	
UCTT	DIG	UCTT	DIG	
UCTT	HYB	UCTT	HYB	
UCTT	HYB (PTYPE)OSC	XTAL	OSC	
UCTT	LIN	UCTT	LIN	
UCTT	MIXED	UCTT	MIXED	
XFMR	POWER	XFMR	POWER	
XFMR	SIGNL	XFMR	SIGNL	

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