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PHOTONIC SWITCHING

Volume 8

Edited by
H. Scott Hinton and Joseph W. Goodman

Proceedings of the International Topical Meeting
March 6–8, 1991
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PREFACE

One of the keys to the future of telecommunications companies will be based on their ability to provide new broadband services to both the business community and the residential customer. These new services include: the transport of NTSC video, Enhanced Quality Television (EQTV), High Definition Television (HDTV), switched video, high data rate file transfers, information retrieval, animated graphics, in addition to being an interconnect for diskless workstations and Local Area Networks/Metropolitan Area Networks (LAN/MAN). With these new services will come the need for the equivalent of a broadband switching office. Such a system could require the capability of supporting in excess of 10,000 users with broadband channel bit-rates exceeding 100 Mb/s. This implies a switching fabric whose aggregate bit-rate could be greater than 1 terabit per second (Tb/s). This fabric, or collection of different fabrics, could have to support both the conventional circuit switching capabilities as they currently exist on the network, in addition to controlling packet services such as ATM cells embedded in SONET streams of data at per port costs similar to existing POTS. The hope of photonic systems is that, through the application of either the temporal or spatial bandwidth available in the photonic domain, the new architectures and fabrics that are conceived, these broadband systems and services be *economically* realized.

Research in photonic switching fabrics can be categorized as systems based on either guided-wave optics or free-space optics. Typically, guided-wave optics have been concerned with the application of optical fiber and the utilization of the large temporal bandwidth available in guided-wave structures such as optical fiber, star couplers, directional couplers, etc. This optical transparency provides large bandwidth analog channels that can be used to transport many channels of digital information. As an example, current single-mode optical fiber supports approximately 25 THz of communications bandwidth around the 1.5 μm wavelength region. This offers the opportunity of multiplexing many users, through either time-division or spectral-division, onto a single-mode fiber thus reducing the cost per user of the required system hardware. Thus, researchers have pursued both time based switching fabrics (photonic time-slot interchangers and multiple access schemes such as time-division multiple access and code-division multiple access), and wavelength based fabrics (wavelength interchangers and both wavelength-division multiple access and spectral code-division multiple access). Arguments for guided-wave optics include:

- Evolves naturally from todays electrical technology since it can integrate directly with electrical transmission lines.
- Builds on the existing fiber base present in the telecommunications network.
- Many guided-wave optically transparent devices have been demonstrated in the laboratory.

- Supports optically transparent switching fabrics.

- The technology is more developed and better understood than the free-space technology.

Free-space optics, on the other hand, has been more concerned with using the available spatial bandwidth to increase the intrasystem connectivity and reduce the limiting effects of buses, low pin-out integrated circuits (IC), low pin-out printed circuit boards, and low pin-out multi-chip modules. This approach is more concerned with extending the life of the electronics technology through the use of optical pin-outs and/or interconnects than replacing it. This new technology could be an important aid to the electronics technology since many of the high performance, high density integrated circuits are pin-out limited. This pin-out limitation forces unnatural system partitioning and limits architectural considerations in both computing and switching systems. Although there has been considerable progress in electronic packaging, such as C4 (flip-chip) and TAB bonding techniques, using "light" as a communications medium may be preferred because "light" has been shown to be energy efficient when the distance between communicating elements is greater than 1 mm. Work in this research area ranges from PCB-to-PCB interconnects to gate-to-gate interconnection of optical logic gates.

Research in free-space optics has been focused on multi-stage space-division switching fabrics, particularly large dimensional fabrics, where the need for a large number of connections is evident. The experimental work done to date has used S-SEED arrays as the switching nodes in the network with bulk optical elements providing the optical interconnects required by the multi-stage networks. Other proposed switching nodes for these fabrics include other optical logic gates, such as optical logic étalons (OLE), double heterostructure optoelectronic switches (DOES), vertical surface transmission electro-photonic (VSTEP) device arrays, or 2-D arrays of "smart pixels" in which the functionality of many nodes are integrated onto a single electronic IC. Due to the potential large scale integration of the switching nodes on each array (up to 10^4 nodes per array) this approach should eventually reduce the hardware cost of such a fabric in addition to providing the capability of implementing a large dimensional switching fabric that could be used as either a packet or time-multiplexed switch. Leading edge research in this area is currently exploring both the performance and cost issues associated with switching fabrics as a function of the granularity of the optical interconnects and the intelligence of the nodes. The potential advantages of this free-space interconnect technology include:

- Provides another dimension of freedom in routing signals.

- Potentially high integration density.

- Low power dissipation per pin-out.

- Parallel structures can reduce latency.

- Through the development of new architectures and fabrics utilizing the parallelism of the available spatial bandwidth, new high performance low cost systems could emerge.

The papers in this book stem from the Third Topical Meeting on Photonic Switching organized by the Optical Society of America and held in Salt Lake City in March of 1991. The meeting was well attended and attracted excellent papers. The papers in this book consist of extended and enhanced submissions from authors who participated at the meeting. The papers have been grouped into eight sections: Space-Division Switching (guided-wave), Space-Division Switching (free-space), Time-Division Switching, Wavelength-Division Switching, Multi-Divisional Switching, Logic and Control, Optical Interconnection, and Novel Devices. Finally, the papers contained within this volume represent the leading edge of research in photonic switching, therefore, the reader should gain a reasonably balanced overview of the current state of photonic switching.

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Space-Division Switching (guided-wave)

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Studies on a 128-Line Photonic Space-Division Switching Network Using $LiNbO_3$ Switch Matrices and Optical Amplifiers

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Abstract

The possibility of a 128 line photonic space division switching network has been demonstrated through experiments using $LiNbO_3$ 8×8 switch matrices and newly developed 1.3μm window facet structure semiconductor optical amplifiers.

Introduction

Photonic space division (SD) switching systems are particularly promising and most practical for providing the necessary broad-band services for future telecommunication needs. A 32 line SD switching system employing polarization independent $LiNbO_3$ 8×8 switch matrices [1] has already been demonstrated for use in a Local-Area-Network [2]. Application expansion of such a switching system requires further increasing the line capacity to greater than 100 lines. Introducing semiconductor Traveling Wave Amplifiers (TWAs) to the switching network would be a very effective method for achieving such an increase [3]-[5].

The proceeding discussion reports design consideration and experimental confirmation of a 128-line photonic SD switching network employing $LiNbO_3$ switch matrices and newly developed 1.3μm window facet structure TWAs.

Switching Network Design

A 128-line non-blocking Clos Network may be realized by using currently available 8×8 and 4×7 photonic switch matrices as outlined in Fig. 1 [5]. The Simplified-Tree-Structure (STS) $LiNbO_3$ switch matrix architecture applied to this network is shown in Fig. 2. In such a network, the worst case signal to interference ratio (SIR) due to optical crosstalk may be expressed as $SIR = |x| - 10\log(m)$ (dB), where x is the optical crosstalk value of the 2×2 switch element and m is the number of switch matrix stages [4],[5]. Since $m = 5$ for a 128-line switching network, a value of less than -18dB for x is necessary, assuming the required SIR to obtain a Bit-Error-Rate (BER) of 10^{-9} is 11dB. A value less than -18.7dB for x has been obtained in polarization independent $LiNbO_3$ switch matrices [1]. Therefore, optical loss budget is the main problem to address in order to successfully achieve a 128-line switching network.

Currently available $LiNbO_3$ switch matrices show 9dB and 12dB maximum losses for the 4×7 and 8×8 devices respectively [1]. If we assume a transmitter output power of 0dBm, a receiver sensitivity of -36dBm (which is typical at bit rates around 1 Gbit/sec), a 2dB transmission line loss (5km), an effective gain of over 22dB (TWA gain minus power penalty) is required in order to achieve a system power margin of at least 5dB. This desired gain can be achieved by using two TWAs. However, in order to maximize the effective gain value of a two stage TWA configuration, the following points must be considered.

(1) TWA location in Switching Network

Placing the TWAs at different locations in the system will result in different input powers and

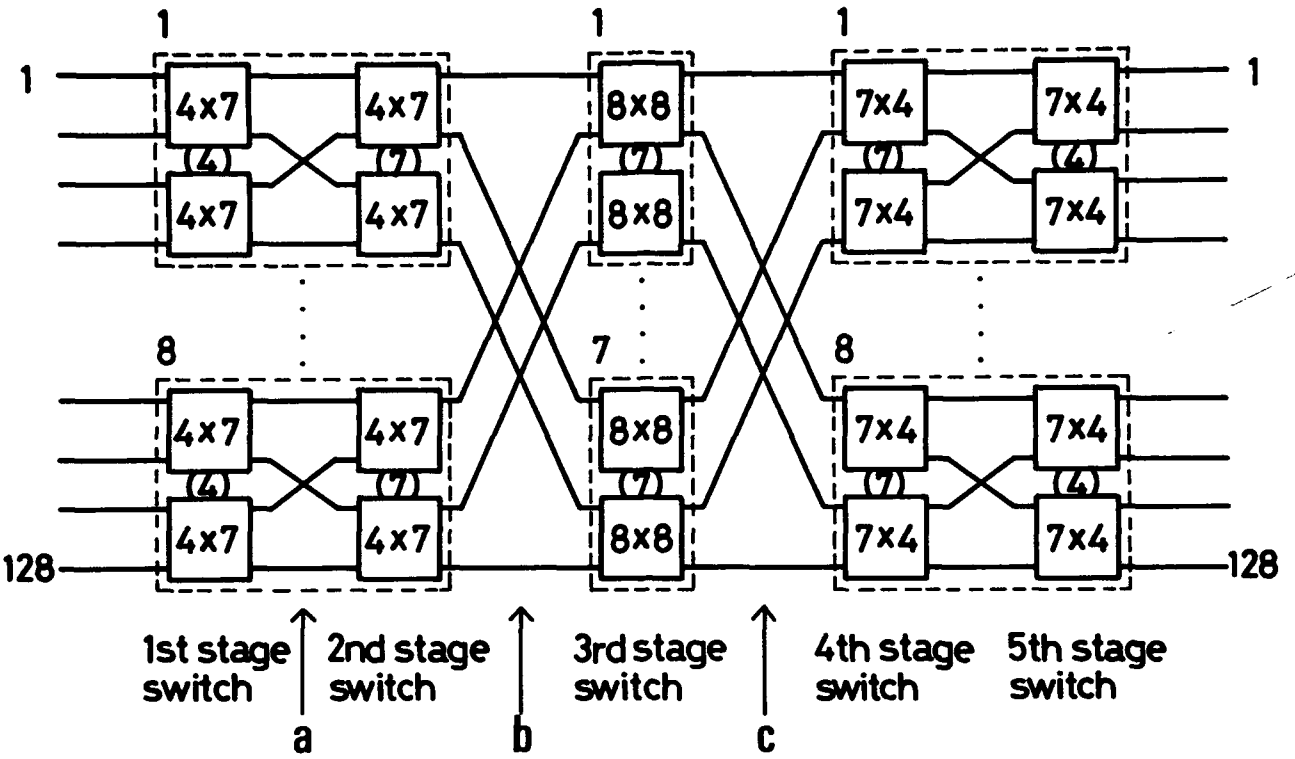


Figure 1. 128-Line photonic Space Division Switching Network indicating TWA insertion positions.

thus different effective gains. Pairs of optical amplifiers may be placed at three possible sites within the switching network, namely [a]+[b], [b]+[c], and [a]+[c] as shown in Fig. 1. Only these three combinations are examined because positioning a TWA before the first switch stage would result in serious gain saturation due to the very large input signal power. Conversely, signal input to TWAs placed after the fourth and fifth stages would be too small. TWA input power will also vary depending upon the switch connection path and the switch input polarization. Such characteristics shall be experimentally examined later.

(2) Optical Reflection

Optical crosstalk due to multiple reflection between cascaded TWAs, can cause power penalty [3],[6]. Optical reflection from switch matrices can also give rise to the same problem. While employing an optical isolator can solve this, such a measure is avoided so as to take advantage of the bi-directional communication possibilities of the switching network. To reduce optical reflection, the analysis in Fig. 3 may be considered. This diagram shows two possible reflection paths in the switching network which may cause power penalty increase. For simplicity, the main components of multiple reflection are considered. We can express the relative reflection crosstalk power between two TWAs, CT_1, and crosstalk power between the switch matrices, CT_2, in the following manner:

$$CT_1 = 2(2G_i + 2\eta - L + R) \quad \text{dB.} \tag{1}$$

$$CT_2 = 2(G_i + 2\eta + r) \quad \text{dB.} \tag{2}$$

where G_i denotes internal gain (dB), η is the optical coupling efficiency between TWA chip and SMF fiber, L is the switch matrix loss, R is the TWA facet reflectivity and r is the reflectivity of the switch-SMF interface. In order to achieve a negligibly small power penalty with direct detection, a crosstalk value of less than -20dB is required. Thus, assuming $G_i = 20$dB, reflection coefficients of less than -30dB and -22dB for R and r, respectively, are required if switch loss is completely compensated by the TWAs ($G_i + 2\eta = L$).

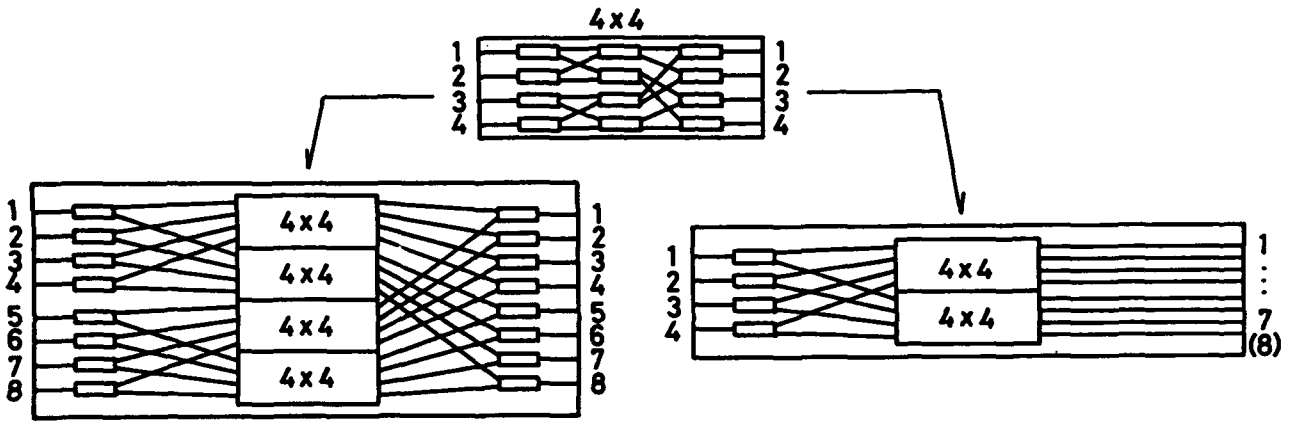


Figure 2. 8×8 and 4×7 switch matrices with Simplified Tree Structure(STS).

Development of Photonic Switching Devices

Based on the above design consideration, window facet structure TWAs and $LiNbO_3$ switch matrix modules have been developed.

(1) TWAs
TWAs with a window facet structure [7] were developed for the 1.3μm wavelength region with facet reflectivities as low as −33dB. TWA chips were SMF-pigtailed at both facets via GRIN lenses using YAG laser welding. Maximum fiber-to-fiber gains of 15dB and 12dB were achieved for the TE and TM modes respectively. Therefore, a total effective gain exceeding 22dB can be achieved with a two stage configuration by keeping the power penalty less than 2dB, even under TM mode operation. TWA module saturation output powers were about −2dBm.

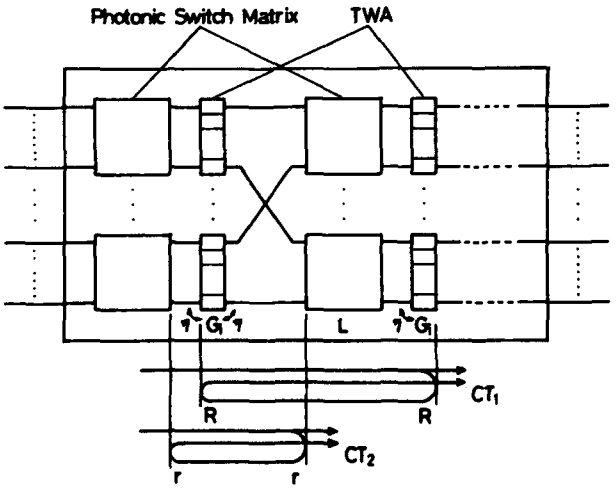


Figure 3. Photonic Switching Network with Switch Matrices and TWAs, indicating Reflection Crosstalk effects.

(2) $LiNbO_3$ Switch Matrix Module
Polarization independent $LiNbO_3$ switch matrix modules were fabricated using chips with anti-reflection (AR) coatings applied to the facets. Resulting reflectivity values at the input and output facets were typically about −27dB.

Experiments

A series of experiments to determine the prospects of using two TWAs to compensate for the loss across a 5-stage switch network employing 128 lines were carried out with particular emphasis upon TWA position, power penalty and resultant system power margin. The transmitter used was a 1.31μm wavelength DFB DC-PBH Laser Diode modulated at 1.12 Gbit/sec with output power of about −1dBm. Sensitivity of the InGaAs APD receiver without TWAs was −36.5dBm (Bit-Error-Rate=10^{-9}). A 3nm bandwidth optical filter with 1dB loss was employed at the optical receiver input to reduce TWA spontaneous emission noise. A 5km subscriber single mode fiber was connected to the switch network. The gain values of the first and second stage TWAs, namely, 'TWA1' and 'TWA2', respectively, were set at 12dB.

Results and Discussion

Bit-error-rate curves for all three possible positions for the two loss compensating TWAs were evaluated for the smallest and largest loss switch-connection paths (Fig. 4). TWA gain,

power penalty, total effective gain, and resultant system margin are detailed in Table 1. When the two TWAs are placed at [a]+[c], the highest switch loss situation revealed a power penalty of 2.4dB. This is a result of firstly the saturated effect of TWA1 which subsequently reduced the gain value, and secondly, the low signal input power to the second stage device. System power margins are reduced to around 1dB in this highest switch loss situation.

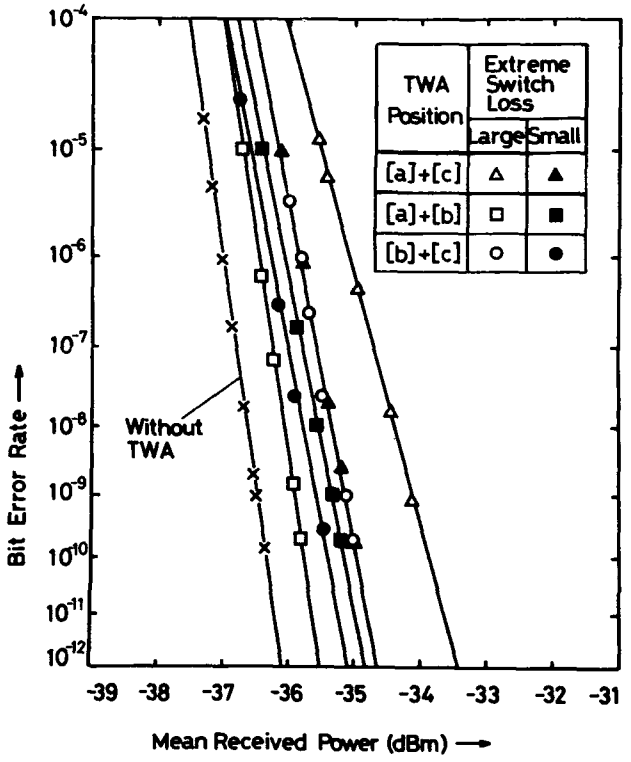


Figure 4. Bit-Errror-Rate Curves for different TWA Positions.

TWAs which were then placed at [a]+[b] showed gain saturation effects in both devices. The further reduction in power margin here however is mainly due to the reduction in the individual gains of the TWAs rather than an increase in power penalty. With the lowest loss paths across the switches, power penalty of only 1.2dB was observed. With this low loss between both devices there is negligible power penalty increase from optical reflection . This reinforces the fact that no optical isolators are needed for this system and therefore paves the way for possible bi-directional transmission.

Finally, the symmetric arrangement of placing the two TWAs at [b]+[c] gave the most practical power margins of over 5dB in the highest switch loss situation. Here maximum gain was utilized, with both TWAs contributing 12dB fiber-to fiber gains and resultant combined effective gains exceeding 22dB. Gain saturation effects have been avoided in this situation and five stages of switches have been loss compensated by the two TWAs.

Conclusion

The design considerations for a 128 line photonic SD switching network with loss compensation from two low reflection window facet traveling wave amplifiers have been investigated. With such a design, 1.3μm window facet structure TWAs and AR coated

TWA SITE	TWA1 GAIN(dB)		TWA2 GAIN(dB)		POWER PENALTY(dB)		EFFECTIVE GAIN(dB)		POWER MARGIN(dB)	
	S	L	S	L	S	L	S	L	S	L
[a]+[c]	8	9	12	12	1.3	2.4	18.7	18.6	13.9	1.1
[a]+[b]	8	9	9	9.5	1.2	0.6	15.8	17.9	10.8	0.4
[b]+[c]	12	12	12	12	1.0	1.3	23	22.7	18.0	5.2

Figure 5. System Characteristics indicating smallest (S) and largest (L) switch loss cases.

$LiNbO_3$ switch matrix modules have been developed. The feasibility of achieving a 128-line photonic SD switching network with a 5 stage Clos architecture has been demonstrated experimentally.

Acknowledgments

The authors are grateful to I. Cha for providing the TWA chips and H. Suzuki for fabricating the TWA modules. Thank you also to S. Suzuki and M. Kondo for very fruitful discussions.

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4 × 4 InP Crossbar Switch Array Using the Electro-optic and Carrier Depletion Effects

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Abstract

An electro-optic 4x4 switch array in indium phosphide has been demonstrated which is suitable for monolithic integration with lasers, detectors, amplifiers and control electronics operating in the 1.3/1.55μm wavelength window.

Introduction

The choice of technology for guided wave optical switches must consider three major issues. Firstly, the transparency of the data path will be determined by the waveguide and switch element optical characteristics. Secondly, the switching speed of the elements, ranging from mS for optomechanical switches to sub-nS for electro-optical and carrier depletion switches, will be determined by the physical mechanism and by the electrical packaging. Switch speed is of especial importance when high data rates are being switched. These issues have been explored for lithium niobate, leading to the demonstration of a 16x16 guided wave electro-optic space switch [1]. The third issue, the monolithic integration of the optoelectronic circuit elements required for routing control and optical signal conditioning, can only be accomplished using a semiconductor technology. Optical detectors and control electronics for routing control and optical amplifiers for optical signal conditioning can be fabricated in compound semiconductor materials.

An electro-optic 4x4 switch has been demonstrated in GaAs [2]. The bandgap structure of GaAs, however, allows only short wavelength optoelectronic devices to be constructed. Optical fibre transmission, by contrast, requires optoelectronic elements operating in the 1.3/1.55μm wavelength region. The switch of [2] was operated at 1.3 microns, so was not compatible with GaAs integrated optoelectronic devices. The InP material system is fully compatible with the optical fibre window. An InP 4x4 guided wave optical switch has been demonstrated where the switching action is obtained by carrier injection [3]. Although this mechanism has significant advantages for data transparency, the switching speed is limited due to extended carrier lifetimes [4]. In this paper we report the first demonstration of an indium phosphide guided wave switch array employing the much faster electro-optic and carrier depletion effects.

Switch Design

The ridge-loaded waveguides, width 3μm, are optimised for operation at 1.55μm using the electro-optic effect enhanced by carrier depletion. Doping the waveguide to obtain an increased refractive index change under reverse bias decreases the control voltage without significantly slowing the switch response. The consequent increase in waveguide loss can be kept modest. 16 directional coupler switch elements are arranged to form a strictly non-blocking 4x4 crossbar switch fabric, so that any required channel rearrangement can be obtained without interruption to other connections (figure 1). The switch elements are 'hard wired' in reverse delta beta mode to minimise the number of electrical control channels. A variation allows uniform delta beta mode operation to be obtained. Switch lengths are 3 and 4mm and the directional coupler gap varies from 2.5 to 3.5μm. Optical interconnection is by 15 or 20mm radius circular bends, yielding a total chip length of 35 to 40mm. Input and output waveguides are spaced by 160μm. Electrical connections employ dual layer metallisation separated by polyimide to bring contacts to separate bond pads at the edge of the substrate. A silica barrier layer beneath the pad metallisation prevents electrical breakthrough to the underlying layers. Test structures incorporated in the design include single waveguides, couplers, switches and diodes.

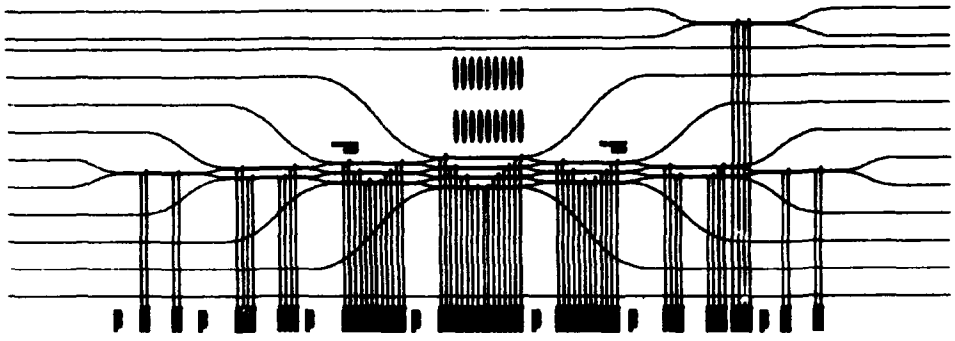


Figure 1. 4x4 switch layout.

Fabrication

The electro-optic switch structure was formed by a single MOCVD growth on an n+ substrate. The $3x10^{16}$ n-doped carrier depletion InGaAsP waveguide had a band gap of 1.3μm and a thickness of 0.5μm. The InP cladding had a thickness of 0.8μm, which was dry-etched to a depth of 0.5μm to form ridge loaded waveguides. Silica was deposited by CVD over the bond pad areas prior to the deposition of the Ti/Zn/Au first layer metallisation. Polyimide was then spun on to perform a passivating, insulating and planarising function (figure 2). Vias were cut by ashing through a silica mask to connect the Ti/Zn/Au second layer metallisation (figure 3). Individual chips were then diced out and assembled on a metal carrier to permit optoelectronic evaluation (figure 4).

Results

The switches were assessed with light at 1.54μm from a semiconductor laser. Satisfactory waveguiding was observed for TE polarisation, with losses of 3dB/cm. Couplers with between one and three coupling lengths were selected for electro-optic characterisation. Switching voltage-length products of 25Vmm were obtained, enabling full switching within the breakdown limit of the material (30 volts).

In conclusion, high speed optical switches with integrated control functions and optical signal conditioning require electro-optic switches in indium phosphide. We have demonstrated the first electro-optic indium phosphide guided wave switch array, comprising sixteen reverse delta beta directional coupler switches in a crossbar fabric. Switching voltage-length products of 25Vmm have been obtained.

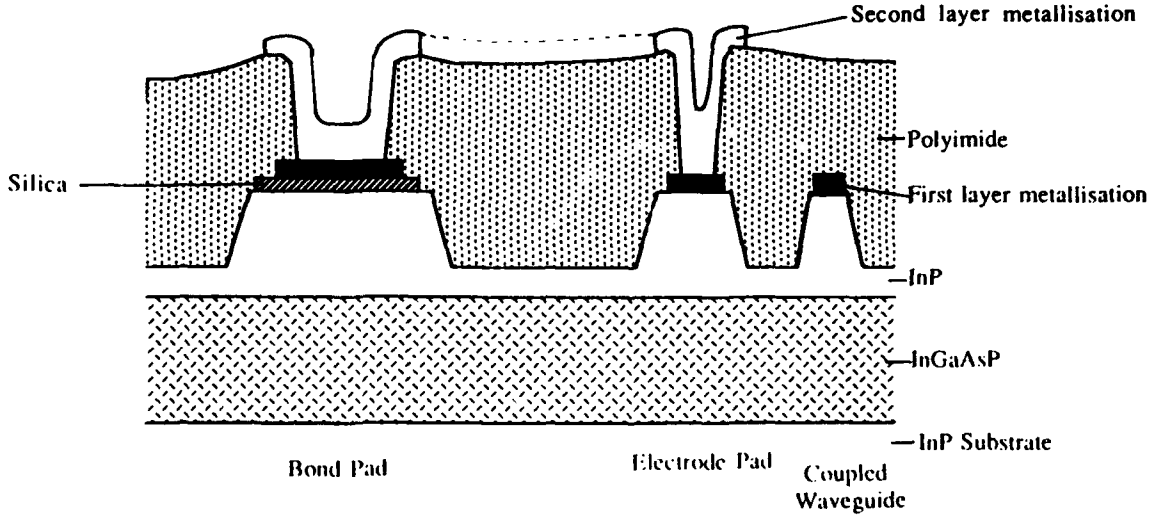


Figure 2. Cross-section through switch.

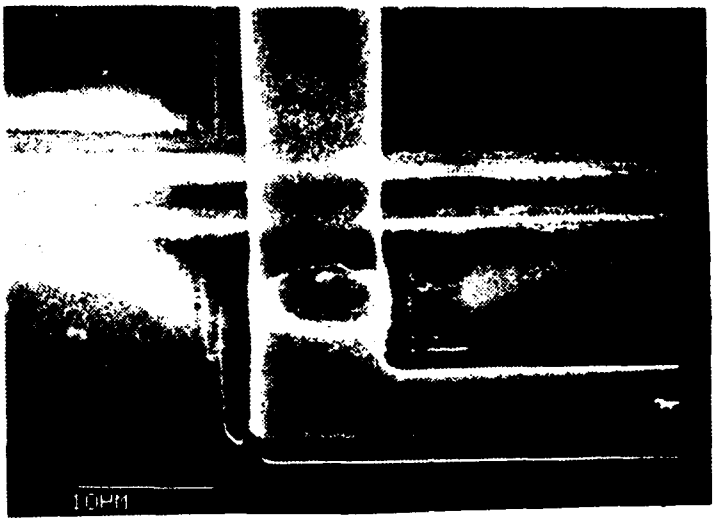


Figure 3. Micrograph of connection between first and second layer metallisations.

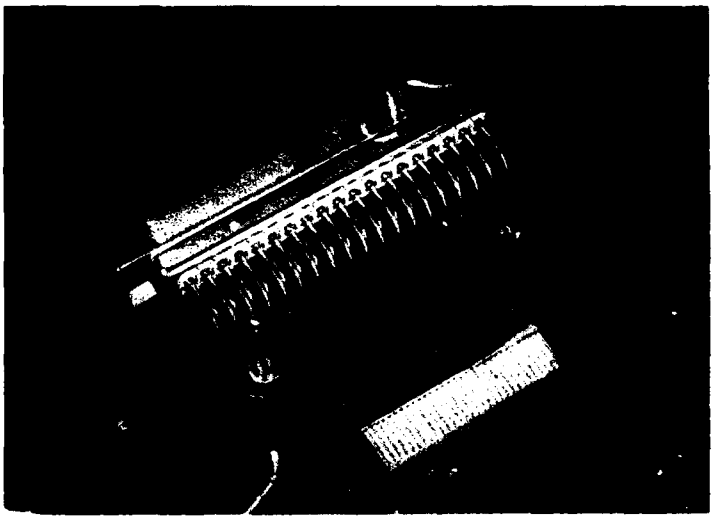


Figure 4. Assembled 4x4 InP electro-optic switch

Acknowledgments

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92-17253

4×4 Nonblocking Acousto-optic Waveguide Space Switch

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Abstract

A 4 x 4 nonblocking integrated acoustooptic space switch has been realized, for the first time, in a Y-cut $LiNbO_3$ channel-planar-channel composite waveguide 0.1 x 1.0 x 3.0 cm^3 in size. The switch consists of four parallel channel waveguides at the input, a large aperture TIPE collimating-focussing lens pair, an array of four tilted SAW transducers, and four parallel channel waveguides at the output. Measured performances for nonblocking switching at the optical wavelength of 0.6328μm include a worst-case crosstalk of -15.6dB, an average throughput of -16.0dB, a frequency resolution (frequency increment required for switching between adjacent output ports) of 18.0 MHz, and a reconfiguration time of 0.145μsec. Capabilities of the switch for performing strictly nonblocking point-to-point, multicast as well as multipoint-to-point were also readily demonstrated.

Introduction

All existing guided-wave optical space switch matrices [1-8] are configured in stages (or tandem), and require a large number of basic cross-point switches as the size of the switch matrix or the number of input and output ports increase. As a result, the real estate of the substrate and the optical propagation losses and crosstalks as well as the complexity in both electrode layouts and electronic driver circuits greatly increase with the size of the switch matrix. Furthermore, both the optical insertion loss and the crosstalks may vary widely with the route the light takes.

Optical space switches that utilize acoustooptic (AO) Bragg diffraction [9] can significantly alleviate the undesirable characteristics referred above. In this paper, a 4 x 4 nonblocking integrated AO space switch that utilizes guided-wave AO Bragg diffractions in a single-mode $LiNbO_3$ channel-planar-channel composite waveguide [10] is reported.

4 x 4 Integrated AO Space Switch Architecture and Working Principle

The switch architecture is shown in Fig. 1. Information-carrying light beams (from an array of four optical fibers, for example) are coupled into the planar waveguide substrate through the input channel waveguides. The light beam from any input channel waveguide expands in the planar waveguide and is collimated by the first TIPE lens [11] because its front focal plane coincides with the output apertures of the input channel waveguides. The collimated light beam tilts at an angle (from the lens axis) which is proportional to the displacement of the input channel waveguide involved from the lens axis. The focussing lens, which may be identical to the collimating lens, follows the tilted transducer array and is followed by the output channel waveguides that serve as coupling elements to the four output ports (to another array of four optical fibers, for example). Note that the input apertures of the output channel waveguides are placed on the back focal plane of the second TIPE lens. A multiplicity of active Bragg diffraction gratings of appropriate periodicity and orientations are then created in the planar waveguide region between the collimating-focusing lens pair by the SAWs generated by the multiple-tilted transducers.

In operation, the light signal from any of the four input ports may be efficiently switched to any of the four output ports by properly varying the propagation direction and the carrier frequency of the SAWs. Thus, by selecting the separation of the input channel waveguide array and its displacement from the lens axis, the tilt angles associated with the input light beams can be adjusted to facilitate programmable and nonblocking routing of the light beams through proper combinations of the transducer element (and thus the direction of propagation of the SAW) and the RF driving frequency.

* This work was supported in part by the NSF.

Design Data

- Substrate: 0.1 x 1.0 x 3.0 cm^3 Y-cut $LiNbO_3$
- Input Channel Waveguide Array
  - Width = 5.0μm
  - Periodicity = 64.0μm
  - Length = 2.0mm
- Output Channel Waveguide Array
  - Width = 5μm
  - Periodicity = 15.0μm
  - Length = 2.0mm
- Collimation-Focusing TIPE lens Pair
  - Focal Length = 10.0mm
- Displacement of #1 Input Channel Waveguide from the Lens Axis: 104μm
- Displacement of #1 Output Channel Waveguide from the Lens Axis: 74μm
- Center Frequencies and Bandwidth of Four-Element Tilted SAW Transducer Array
  - 260, 340, 420 and 500 MHz
  - Bandwidth > 80 MHz for each.

Preparatory Experiment

Measurements were carried out at 0.6328μm He-Ne Laser wavelength.

Fig. 2(a) shows the light path through the lens pair when the light was excited through the #1 input channel waveguide that lies closest to the lens axis, namely, 104μm. The light path is seen to remain nearly a straight line along the lens axis.

Fig. 2(b) shows significant bending of the light path since in this case the guided-light was excited through the #4 input channel waveguide that was

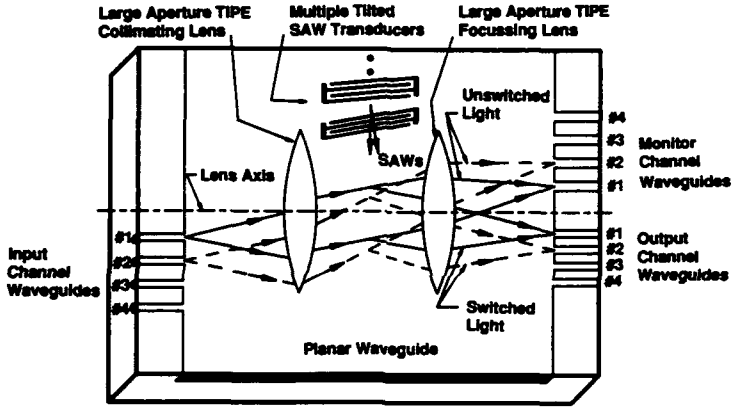


FIG. 1 ARCHITECTURE OF A 4 x 4 INTEGRATED ACOUSTOOPTIC SPACE SWITCH USING BRAGG DIFFRACTIONS IN A $LiNbO_3$ CHANNEL-PLANAR-CHANNEL COMPOSITE WAVEGUIDE (Note : Not To Scale)

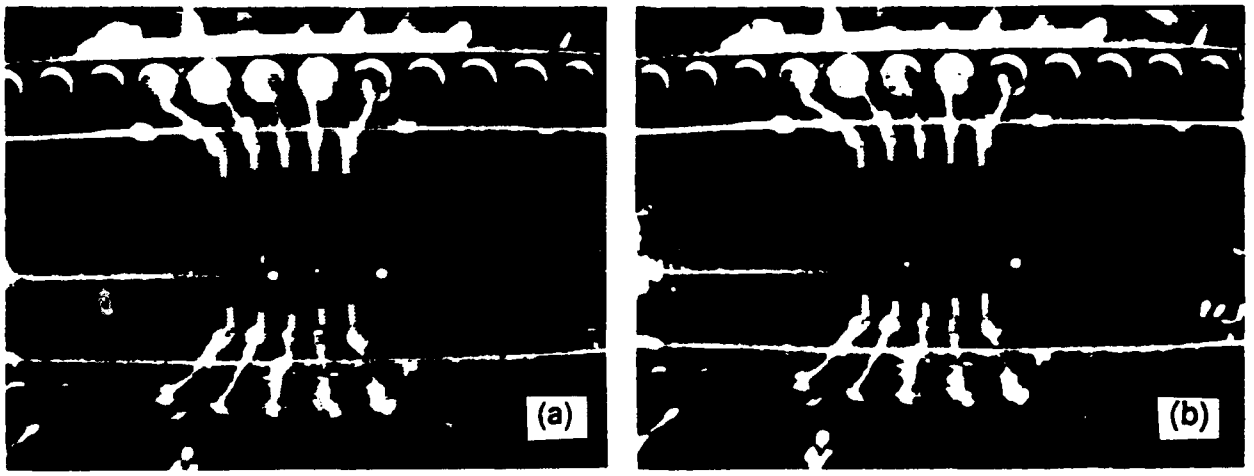


Fig. 2 Photographs Showing The Undeflected (a) And Deflected (b) Optical Paths Of A 0.6328 μm He-Ne Laser Beam Guided Through The TIPE Collimation-Focusing Lens Pair In A $LiNbO_3$ Channel-Planar-Channel Composite Waveguide.

displaced by 296μm from the lens axis. An average throughput of -14.0 dB with variation of ±1.0dB was measured.

Examples of Switching Experiment

By selecting the transducer element to be activated and its driving frequency, a light beam at any of the four input ports was switched to any of the four output ports. For example, Figs.3(a) and 3(b) show the photograph of the light spots and their beam profiles taken at the output ports versus the driving frequency of transducer element #2 when a light beam entered at input port #2. The light spots and beam profiles shown from left to right were obtained, respectively, for the output ports #1, #2, #3, and #4 with the driving frequencies set at 320, 338, 356, and 374 MHz.

Performance Figures:

1. Average Frequency Increment Required Between Adjacent Output Channels = 18MHz.
2. Average Diffraction Efficiency = 70% at RF Drive Power of 150mW.
3. Average Throughput = -16.0 ±1.0dB at RF Drive Power of 150mW.
4. Reconfiguration Time = 0.145μsec.

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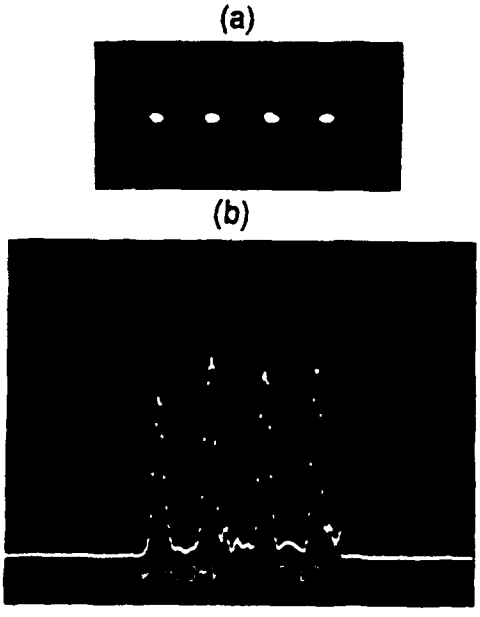


Fig. 3 Photograph (a) And Beam Profile (b) Of The Light Spots At the Output Ports Versus The Driving Frequency Of Transducer #2 For A Light Beam Entered At Input Port #2.

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Semiconductor-Based Switches within the RACE Photonic Switching Program

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Abstract:

Photonic switching options for various applications including ATM switching, high speed LANs, optical cross-connects, etc, are currently investigated within the european project RACE OSCAR (Optical Switching Systems, Components and Application Research). InP based Photonic Integrated Circuits have been identified as key devices. The paper reviews the latest state of the art semiconductor switches designed and fabricated within the project illustrating both the main technological trends as well as the envisaged system applications.

Introduction

The optical fiber has been recognized to be a superior transmission medium. Performing switching in the optical domain might well be the next challenging step. The attractiveness of photonic switching comes from the possibility of performing multidimensional switching by exploiting the wavelength, the time and the space domain /1/. This will enable to significantly increase the capacity of switching fabrics. Although the potential benefits of optical switching are widely acknowledged, the prefered system architecture and the most suitable cost-effective technology are still matter of debate. Partly, this is due to the number of areas where photonic switching can be introduced: these cover applications ranging from simple switches such as slow protection switches, up to highly complex and sophisticated devices where optical processing can be included, such as ATM switches for instance. It is likely that different applications will ask for specific technologies. A variety of applications are currently being studied within the european project RACE 1033 OSCAR (Optical Switching Systems, Components and Application Research) /2/. The system work is supported by an intensive development of key devices some of which will be discussed in the present paper.

Technological options

When considering the merit of both optics and electronics, it is clear that while some functions (interconnection, transmission, switching) are better performed in the optical domain, some others (logic functions, buffering, synchronisation) are easier to implement in the electronic domain. Therefore, in order to exploit the specific advantages of optics and electronics at the best, the future switching fabrics will have to combine optical and electronic devices. With the increase of complexity and switching capacity, the monolithic integration leading to the concept of "electronic islands" located on various places of an optical mother board will become compulsory. Considering both the maturity of different technologies, as well as first system applications, we have focused our work on guided wave devices, although, in a second step, free space options are also serious candidates for solving some specific interconnection problems. Initial work and system demonstrators have been done using $LiNbO_3$ devices /3,4/. However, the largest effort is spent on developing InP optical circuit and integration technology. Indeed, only III-V semiconductors, and when considering the wavelength range of interest for optical communications ($1.3\mu m$ to $1.55\mu m$), particularly InP and related compounds, allow to integrate optic, opto-electronic and electronic functions in a a smart and cost-effective way.

InP based photonic circuit's technology is progressing thanks to the wide use of high per-

formance epitaxial techniques (MOVPE, Chloride-VPE) which have overpassed the old-fashioned liquid phase epitaxy in terms of uniformity (GaInAsP epilayers with compositional fluctuations lower than 0.5 % over 2" wafer can be achieved by both MOVPE and Cl-VPE), interface quality and purity. Dry etching (RIE for instance) has been proven to be much more flexible than chemical etching. Surface damage and edge roughness have been reduced to a level where they do not induce any measurable penalty. Exploiting the flexibility of both the growth and the epitaxial techniques, various waveguide structures have been investigated (Figure 1).

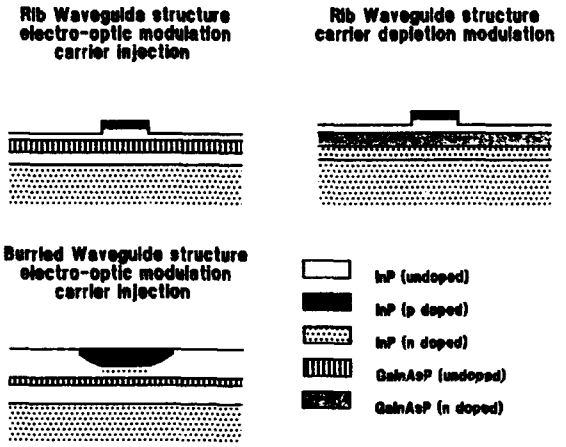


Figure 1: Three basic InP based waveguide structures.

The typical losses for double heterostructure InP/GaInAsP/InP waveguides are now in the 0.2 to 1.0 dB/cm range for both passive and active (i.e. waveguide with top electrode) structures /5,6/. This enables the design and fabrication of large photonic circuits.

A specific area where a lot of work still remains to be done is the waveguide/fibre coupling. By shaping the fiber end it is possible to achieve coupling efficiencies in the order of 3dB/facet; however, a reliable and cost effective solution applicable to multi-fibre/multi-waveguide connection has still to be investigated.

InP switches

The 2x2 space switch forms the basic building block which can be used not only for constructing larger switching matrices, but, considering its dynamic and spectral behaviour, can play also a role in time or/and wavelength multiplexed architectures.

Two families of InP switches have been extensively studied: interferometric devices such as directional couplers, and non-interferometric structures such as the total internal reflection switch and digital optical switch (Figure 2). These structures have been used in combination with various waveguide configuration exploiting the electro-optic or/and carrier induced effects as shown on Figure 3.

The standard directional couplers require 2 to 6 *mm* long interaction length and a driving voltage which ranges from ~ 15 V for an electro-optic device (p-i-n structure where the waveguide core layer is undoped) /7/ down to ~ 5 V for a carrier depletion structure /8/. The speed of these switches is usually limited by the electrode capacitance (typically 1pF/mm). Directional couplers have been also activated using carrier injection: driving current of ~ 5 mA has been measured. Matrices up to 4x4 have been demonstrated /9/. The concept of directional coupler has been extended to vertical structures where extremely short coupling lengths (~ 100 μm) can be obtained. Because of its compactness and the vertical configuration, the device is suitable for 3D like integration /10/. Also, when associated with multiple quantum well structures, non linear, op-

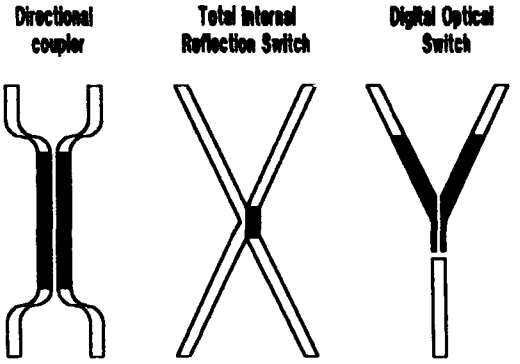


Figure 2: InP based switching structures studied within the project.

Bias Core layer	Reverse Undoped	Reverse Doped	Direct Undoped
Directional Coupler	■	■	■
Digital Optical Switch		■	■
Total Internal Reflection			■

Band-filling
Plasma

Pockels effect
Kerr effect

Figure 3: Summary of the Switch-Waveguide combinations and the associated physical effects.

tically and electrically driven switches have been achieved /11/. The total internal reflection switch is also a very compact device (~ 200 μm). However it requires a strong refractive index change which, for a non quantum well device, can be achieved only through carrier injection. Relatively high driving currents are needed to obtain full switching (200 mA), but the switch is polarisation independent /12/. An attractive device, which might combine the advantages of both the directional coupler and the total internal reflection switch is the Digital Optical Switch, originally demonstrated on $LiNbO_3$ /13/. First InP DOS carrier injection and carrier depletion devices have been fabricated and the digital response as well as the polarisation independence has been demonstrated /14/.

The above discussion shows that the switch and the waveguide structure both determine the overall switch performance. Depending on envisaged system application, different trade-offs have to be considered. Figure 4 and 5 show two examples.

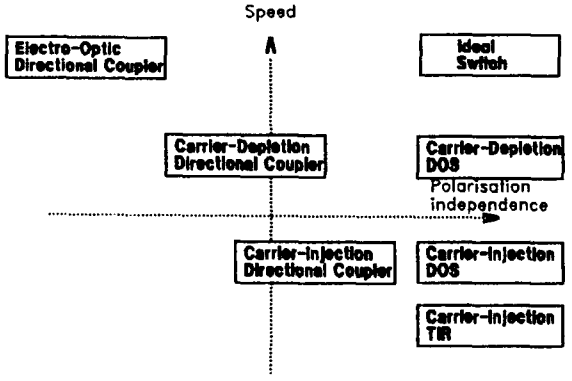


Figure 4: Speed/polarisation independence trade-off for various InP switches

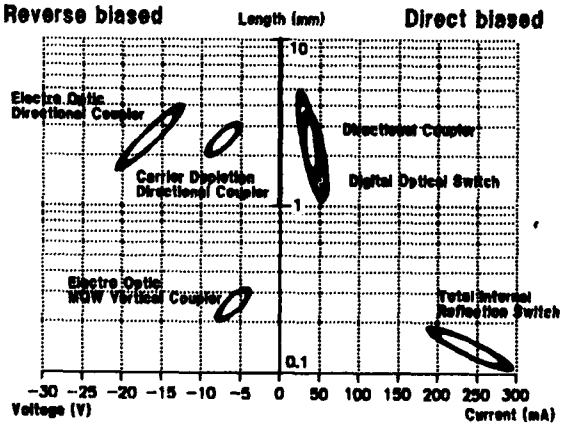


Figure 5: Driving current (resp. voltage) / device length trade-off of direct biased (resp. reverse biased) InP switches.

Monolithic integration

The OSCAR project is also tackling the problem of monolithic integration of optical switches with other optoelectronic and electronic devices. Integration of high speed (5 GHz), low dark current (0.1nA), p-i-n detectors has been successfully achieved /15/. The optical amplifiers are also very attractive since they may compensate for the waveguide and fibre/chip coupling losses. Optical circuits with locally integrated booster amplifiers and exhibiting fibre to fibre gain of several dB have been demonstrated /16/. Furthermore, the optical amplifier can be used also as a multifunctional device, with additional gating and detection properties /17/. This opens the way towards all optical amplifier based matrices with built-in monitoring function /18/.

Electronic integration is another key area which deserves a lot of attention. Three options are presently investigated. The first one uses monolithic integration of InP (HBT) electronics and process validation has been already fulfilled /19/. The two other options uses GaAs based FETs, which have the advantage to be an already well established technology. A monolithic approach is investigated through the use of heteroepitaxy: first InP switches have been integrated with GaAs driver FETs /20/. GaAs FETs can be also integrated on a quasi monolithic fashion using the Epitaxial Lift Off technique /21/; first integration has been also successfully demonstrated with this technique.

Final remarks

The results achieved so far within the european consortium OSCAR have convinced us that InP based technology is viable, and will play an increasingly important role in photonic switching. The variety of optical switches developed can cover a wide range of applications. The progress on monolithic integration also makes possible now to design and fabricate complex devices, with specifications established in view of a given application. One of the first such devices developed is the Passive Access Node switch used in a Very High Speed Optical Loop /22/. Nevertheless, one should not minimize the large effort which still remains to be done before photonic switching is used in real system. In years to come we should see a multiplication of devices developed for and tested in a system environment. This should result in an evolution of system architectures and further progress of device technology.

Acknowledgments

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Low-Loss Acousto-optic Permutation Interconnection Network

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Abstract

An integrated acoustooptic device capable of rapidly permuting an array of optical signals on single mode fibers without suffering fan-in and fan-out losses is presented.

Overview

A new approach to implementing an optical crossbar using a single acoustooptic device in 2D is presented. This is an improvement over previous acoustooptic crossbars which require N channel devices[1,2]. This novel device configuration can permute an array of single mode fiber inputs to outputs without suffering from fan-in and fan-out losses inherent to 3D optical crossbar[3]. Generalized crossbars with broadcast capabilities can also be implemented with the same device by simply changing the driving signals, and this will achieve the minimum possible loss, given by the degree of fanout. The reconfiguration time of the switching network is governed by the acoustic aperture, which is on the order of one microsecond. The device addressing requires only a single driving signal which contains N simultaneous frequencies. This fiber optic switching system avoids optical to electronic conversion permitting the transmission of arbitrary format high bandwidth signals. We present results of the operation of the switch using a bulk phased-array acoustooptic Bragg cell driven with multiple input frequencies that permutes an array of inputs to an array of outputs. A surface acoustic wave integrated optics implementation of the device optimized for permuting the 12 single mode fibers in a fiber ribbon is being built and tested for application as a switch for digital signals in parallel processors and in video and telecommunication switching environments.

Three advantages are realized by this new design that make this an attractive approach to implementing an optical spatial permutation switch. The first is the permutation switch is essentially lossless, except for the small fixed coupling loss into and out of the device, and a slight deviation away from 100% diffraction efficiency. The second is that it requires low power due to effective utilization of the acoustooptic interaction and the efficiency-bandwidth tradeoff. For an $N \times N$ crossbar the efficiency is N^2 times that of a normal wideband acoustooptic device, resulting in milliwatt drive powers for optimum diffraction efficiency. Finally the device is realized on a single integrated optic substrate, rather than requiring 3-dimensional bulk optics, and has such low power dissipation that arrays of the devices can be stacked up, and cascaded into larger networks.

Device Design

The $N_i \times N_o$ low-loss acoustooptic interconnection system is depicted in figure 1. The optical input is a uniformly spaced array of N_i single mode fibers, which are widely spaced so that they are resolvable by a factor of N_o, thus the separation between the fibers, D_i, is N_o times the modal width of each waveguide. The N_o optical outputs are on an array of waveguides which are just resolvable, so that the array of output waveguides are separated by D_o, slightly more than the modal width. The input array is collimated by the first lens, producing a set of collimated beams with large angular separation, which are incident on the SAW acoustooptic Bragg cell. The Bragg cell is fed a superposition of N_i acoustic frequencies, each of which is responsible for directing one of the inputs towards a selected output. The second lens focuses

the acoustically-redirected diffracted optical waves onto the destination fibers, thereby coupling the input optical signals into the appropriately permuted output fibers. The directions of propagation of the optical inputs and outputs and the directions of propagation of the various acoustic frequencies is arranged so that each fiber input is Bragg matched to only one of the acoustic frequencies and does not interact with any of the others. This is fundamentally different than a normal wideband acoustooptic device, in which a single optical input is intended to be diffracted by all of the acoustic frequencies which are present, and requires a special Nth order time delay beam steering transducer design, as shown in Figure 2.

In this acoustooptic crossbar the $O(N^2)$ complexity inherent to a generalized crossbar is folded over into the frequency domain representation The device bandwidth is divided up into N_i nonoverlapping frequency bands, as shown in Figure 3, and one of N_o frequencies is chosen out of each band to direct one of the N_i inputs to the N_o outputs. The number of frequencies which can be independently resolved at any instant in an acoustooptic device is equal to the time-bandwidth (TB) product of the device. Typically TB >400, which means that the crossbar size that is implementable with a single device is about $N < \sqrt{TB} \approx 20$. Alternatively 40 inputs can be steered towards any of 10 outputs, or 10 inputs can be directed to any of 40 outputs, as long as the product of the number of inputs, N_i, with the number of outputs, N_o, is less than the time bandwidth product.

The operation of the acoustooptic interconnect for a 3 input to 3 output crossbar is depicted schematically in Figures 2-4. Figure 2 shows a staircase transducer array operating at three frequencies increasing from the center frequency. The acoustic momentum vector, shown at the right, increases in length with increasing frequency, as well as steering to the left. The Nth order staircase transducer array resets the beam steering angle when an additional acoustic wavelength fits within the stair step as shown at the bottom of Figure 2. As the frequency is varied across the full device bandwidth, the locus of the acoustic momentum vectors traces out a series of three diagonal lines.

The momentum space representation of the optical and acoustic waves, and the birefringent diffraction geometry is illustrated in Figure 3. The widely spaced extraordinary polarized inputs produce wave vectors shown on the inner index surface in a negative uniaxial crystal. The frequency dependent locus of acoustic wave vectors are shown in gray. The lowest frequency band, shown at the top, efficiently couples the first input optic beam to one of the finely spaced, ordinarily polarized, outputs by steering the acoustic wave vector tangentially across the ordinary polarized output surface as the drive frequency varies within the band. Higher acoustic frequencies steer to the loci shown above this output surface, preventing coupling due to the Bragg mismatch. These higher frequencies do fall on the output surface for the other input optical wave vectors as shown in the middle and bottom of Figure 3. The frequency response for each optical input is shown at the right. The nine acoustic frequencies denoted by arrows in the frequency response are used to specify all possible input to output couplings. The coarse frequency bands correspond to the input beams, while the fine frequencies within each band are used to specify the output fiber destination.

Bragg matching is used to eliminate unwanted nonlinear acoustooptic rediffractions as illustrated in Figure 4. The coupling of the first input to the third output, and the second input to the first output is shown on the left. For large diffraction efficiencies we must consider the possibility of second order diffractions. These multiple diffractions, in a normal acoustooptic device, deplete the output beams of power preventing high diffraction efficiencies and also introduce crosstalk. In the lowloss acoustooptic permutation switch we have arranged the design so that the higher order diffractions have a large momentum mismatch, preventing such a light loss. Figure 4 shows, on the right, the coupling on the top left rediffracted through the acoustic wavevector of the bottom left. The polarization wave produced due to the simultaneous presence of multiple acoustic waves, is not Bragg matched since the output optic momentum vector misses the output surface due to the tilt of the output surface compared to the input surface. This prevents power build up in the unwanted multiple diffractions and hence allows the switch to be used at very high diffraction efficiencies without unwanted depletion or crosstalk.

Bulk Acoustooptic Demonstration

A 3×3 optical switch has been experimentally realized by using an off-the-shelf beam-steering AO cell to demonstrate the concept of the anti-beam steering photonic switch. This scheme is a suboptimal realization of the acoustooptic crossbar that can suffer from higher order diffraction effects. The experiment setup is shown in Figure 6. The He-Ne beam was split into three beams and each of which was modulated by an AOM, which were driven by three signal sources. These modulated beams were combined at widely spaced input angles and applied to the Bragg cell which is operated in the antibeam steering condition, so that it has very narrow nonoverlapping acoustic frequency bandwidths for each of the input

beams. This allows each of the optical beams to be independently deflected to the output fiber array by applying the correct combination of RF frequencies, just as in the optimized Nth order beam steering staircase transducer design. The Bragg cell is driven by three RF generators which thereby control the switch matrix. The diffracted output beams are then focused onto three multimode fibers mounted on a 250 μm spacing V groove. Multimode fibers were used to obtain the correct core diameter to separation ratio easily, but a fully integrated system could use single mode output waveguides without suffering additional loss. The output of the fibers were detected by amplified photodiodes. Figure 7a shows the outputs on each fiber when 55.5, 73.3 and 92 MHz tones were applied to the AOD, and the bottom trace is a system clock. Figure 7b shows the permutation switching of the first two input beams, when 59, 69.2, and 92 MHz were applied simultaneously to the AOD. Figure 7c shows the permutation of the last two inputs, when 55.5, 76.6, and 89 MHz were applied to the AOD. Figure 7d shows the broadcasting of the central input beam to all 3 output fibers, when 69.2, 73.3, and 76.6 MHz tones were simultaneously applied to the AOD, but this mode of operation suffers from an unavoidable fan-out loss of 3.

Clos Network

The input and output of the low loss acoustooptic permutation switch are both carried on single mode fibers, thereby allowing the output of one crossbar to be fed into the input of another in order to implement larger switching systems. The Clos network[4], shown in Figure 5a, consisting of R way perfect shuffled interconnects between arrays of crossbars is a natural choice for interconnecting these small crossbars. The R way perfect shuffles grow exceedingly complex in 2D for even small R, and electronic implementation of Clos networks, especially in VLSI, becomes unmanageable. A possible solution to this topological problem is obtained by making use of the 3-dimensional nature of optics, and stacking the planar SAW devices into an array of crossbars. In order to implement a Clos network, the output from an array of R N-input $\times$ M-output crossbars must be R way shuffled and fed into M $R\times R$ crossbars, whose outputs must be M way shuffled and fed into an array of R M-input $\times$ N-output crossbars. This can be implemented easily by rotating a second stack of M optical crossbars by 90 degrees and butt coupling to the first and third stacks, as shown in Figure 5b. A reconfigurable network can be implemented when $M = N$, while a more powerful, fully nonblocking switch is achievable for $M \geq 2N - 1$.

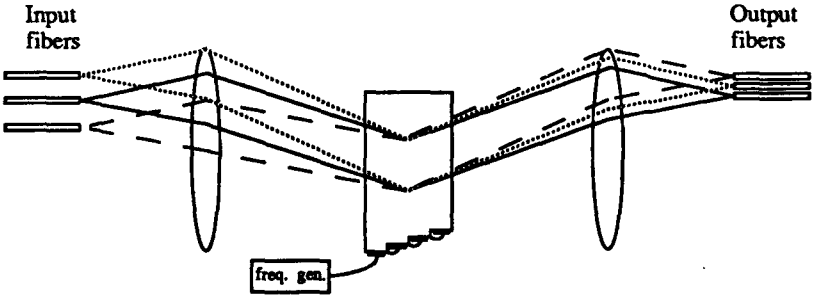


Figure 1 Acoustooptic permutation switch

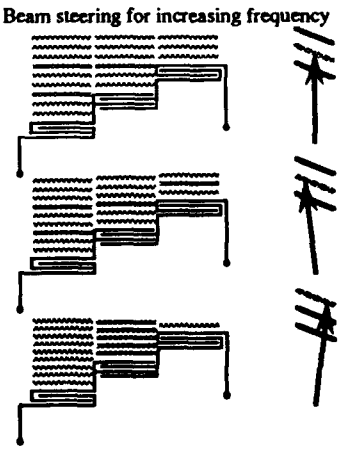


Figure 2 Nthorder acoustic beam steering

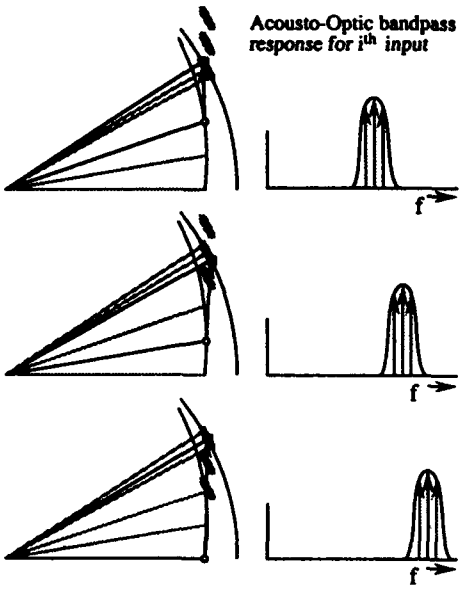


Figure 3 Multi-input frequency response

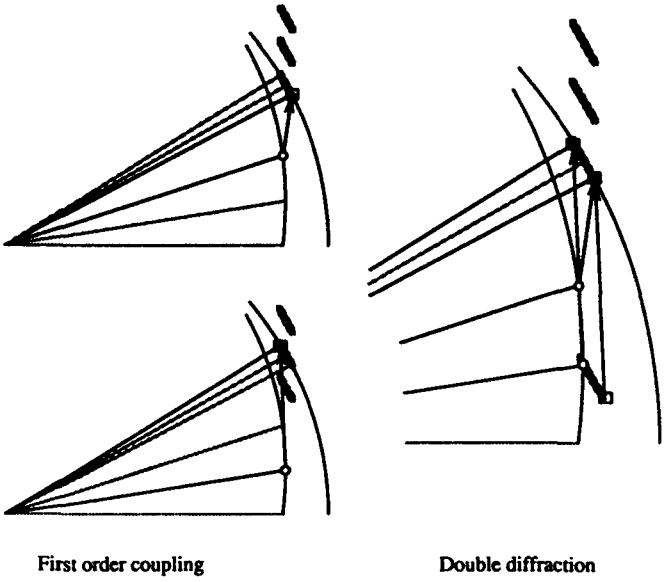


Figure 4 Higher order Bragg Scattering

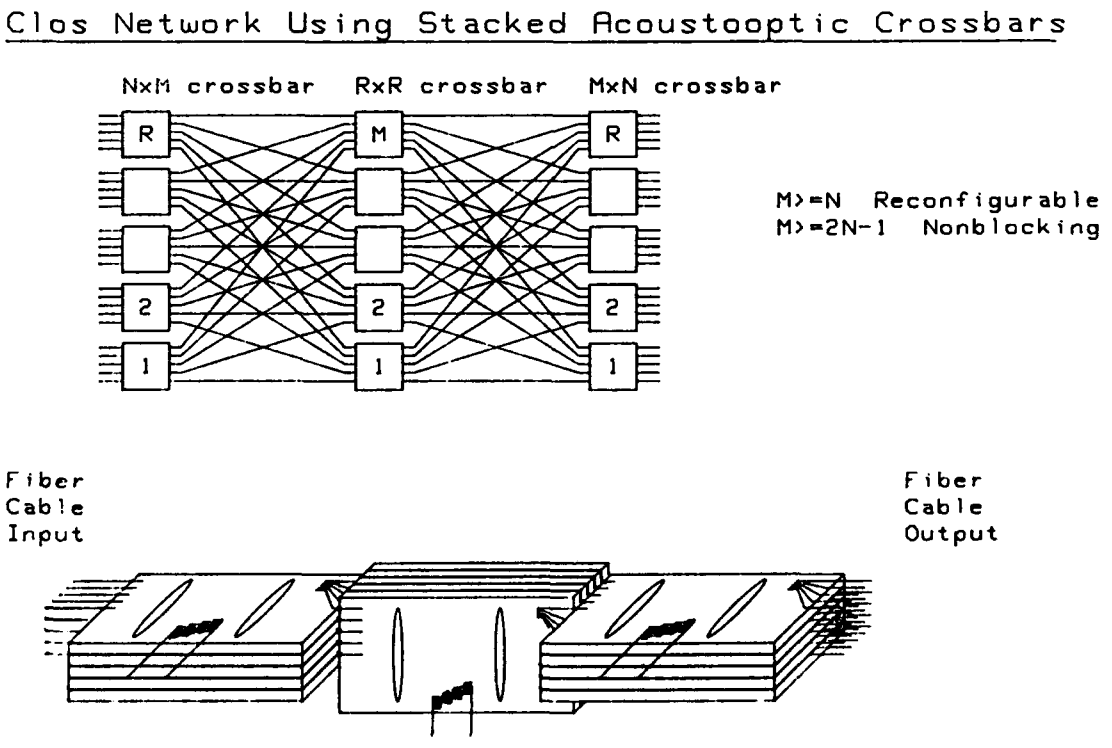


Figure 5 2 dimensional vs. 3 dimensional Clos network

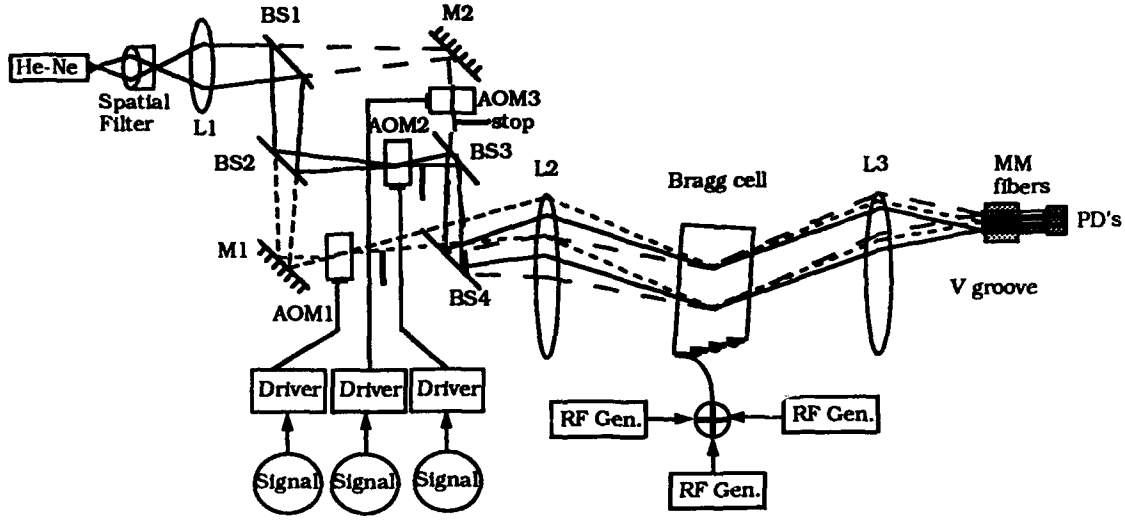


Figure 6 Experimental arrangement

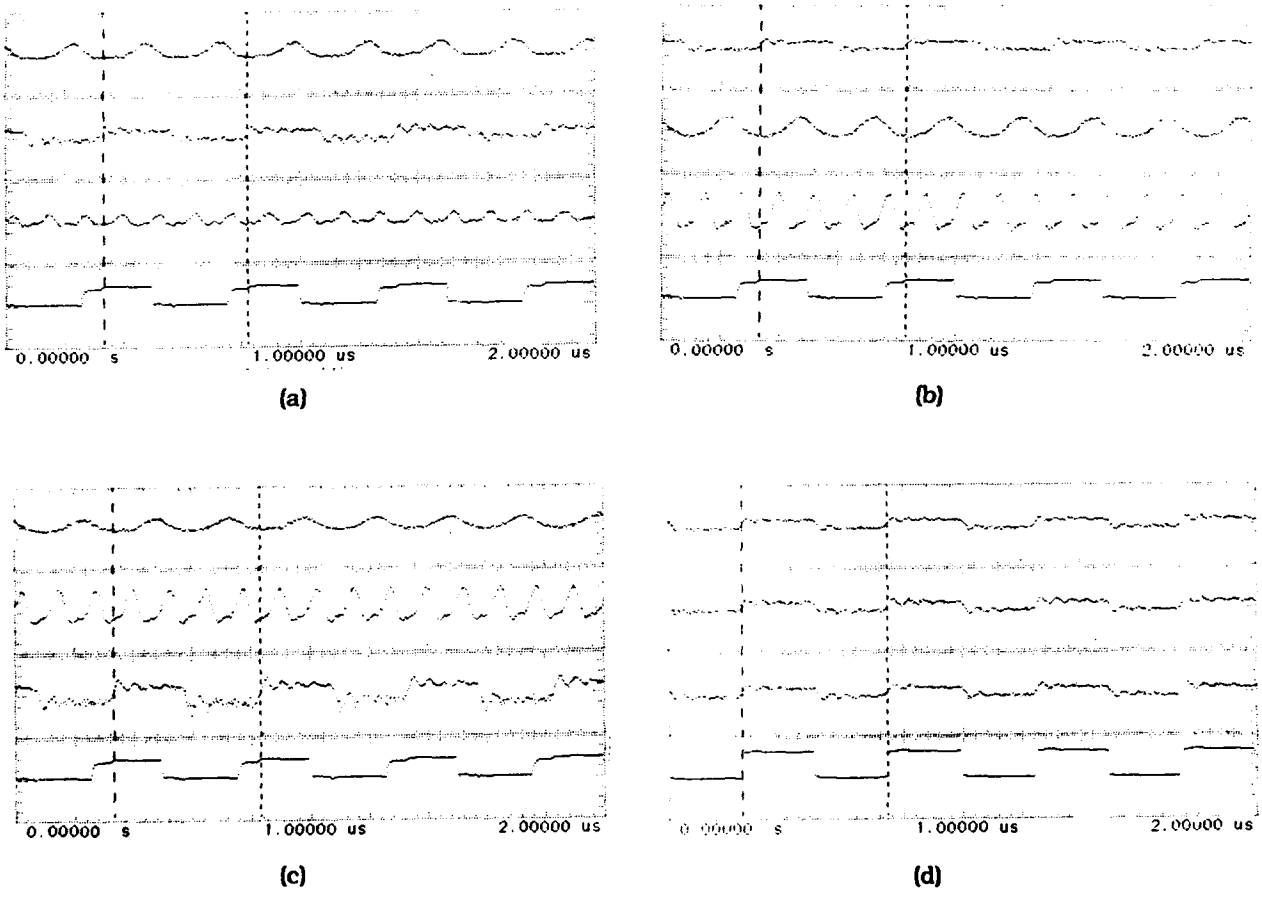


Figure 7 Oscilloscope traces of output signal from fibers (a) unpermuted outputs and system clock, (b) permutation of the first and the second , (c) permutation of the second and the third, (d) broadcast of the second input.

Acknowledgment

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Polarization-Independent GaAs/AlGaAs Electro-optic Guided-Wave Directional Coupler Switch Using (111)-Oriented GaAs Substrate

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Abstract

A polarization independent GaAs/AlGaAs electro-optic directional coupler switch with less than -12dB crosstalk level for any incident polarizations, has been realized for the first time, by using (111)-oriented substrate.

1. Introduction

The interest in guided-wave optical switches made of III-V semiconductor compounds for photonic switching application is growing, because of their large scale integration capability and their ability to be integrated with other semiconductor devices. Therefore, several kinds of optical switch, such as a carrier injection type switch[1], a gain guide type switch[2] and a directional coupler type switch[3], have been investigated. Among them, a GaAs/AlGaAs electro-optic directional coupler (EODC) is attractive, because of its low absorption loss at long wavelength region[4], fast switching speed, low electric power consumption and wavelength independent operation capability. Therefore, a GaAs/AlGaAs EODC is promising as a cross-point element in an integrated matrix switch. Actually, 4x4 GaAs/AlGaAs matrix switches with quite uniform device characteristics have already been realized[5] by the authors. However, all of reported semiconductor directional coupler switches, so far using electro-optic effect, have been polarization sensitive. Polarization independent semiconductor EODCs, compatible with standard single-mode fibers, are desired for practical use. Although some polarization independent $LiNbO_3$ switches have been recently reported[6],[7], no attempt to realize polarization independent semiconductor EODC has been made yet, except theoretical consideration[8].

This paper describes the first polarization independent GaAs/AlGaAs EODC switch. A (111)-oriented crystal, instead of conventional (100) orientation, has been used in order to solve polarization dependency problem. The achieved device has crosstalk as low as -12dB and 19V switching voltage at 1.3μm wavelength, for any incident polarizations.

2. Device Design

In the conventional GaAs EODCs using (100)-oriented substrates, field induced refractive index changes with electric field vertical to the (100) plane are written by

$$\Delta n = \begin{cases} (1/2)n^3 r_{41} E & \text{(TE polarization)} \quad (1) \\ 0 & \text{(TM polarization)} \quad (2) \end{cases}$$

where n, r_{41} and E are refractive index for the medium, electro-optic coefficient and electric field intensity, respectively. Since no refractive index change occurs for TM polarization, conventional GaAs EODC should be polarization sensitive. On the other hand, refractive index changes are written by[9]

$$\Delta n = \begin{cases} (1/2\sqrt{3})n^3 r_{41} E & \text{(TE polarization)} \quad (3) \\ -(1/\sqrt{3})n^3 r_{41} E & \text{(TM polarization)} \quad (4) \end{cases}$$

for EODCs using (111)-oriented substrates with electric field vertical to the (111) plane. Therefore, refractive index changes exist for both TE and TM polarizations. Although the amount of refractive index change differs between TE and TM polarizations, polarization independent operation with the same switching voltage, can still be obtained using the uniform $\Delta\beta$ configuration, with the EODC length to coupling length ratio (L/l_0) being about 1. A switching diagram for the uniform $\Delta\beta$ configuration is shown in Fig.1 to explain the polarization independent operation principle. For

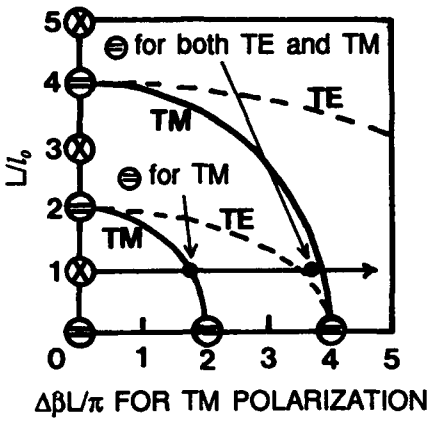


Figure 1. Switching diagram for a (111)-oriented EODC with uniform $\Delta\beta$ configuration.

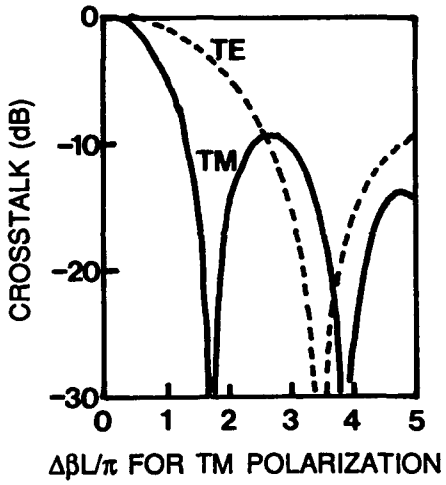


Figure 2. Calculated ⊖ -state crosstalk for a (111)-oriented EODC with uniform $\Delta\beta$ configuration. $\Delta\beta_{TM}=2\Delta\beta_{TE}$ is assumed.

both TE and TM polarizations, ⊖ -state can be achieved at around the TE polarization ⊖ -state voltage, in other words, at around $\Delta\beta L/\pi=3.7$. Calculated ⊖ -state crosstalk, caused by the refractive index change difference between TE and TM polarizations, is shown in Fig.2. Here, $\Delta\beta_{TM}=2\Delta\beta_{TE}$ is assumed, according to Eqs. (3) and (4). Less than -20dB ⊖ -state crosstalk level can be obtained, around $\Delta\beta L/\pi=3.7$, for both TE and TM polarizations, simultaneously .

On the other hand, ⊗ -state crosstalk is determined by the coupling length difference between TE and TM polarizations. In order to obtain less than -15 dB ⊗ -state crosstalk for the uniform $\Delta\beta$ configuration, coupling length should be between 0.9 and 1.1 times EODC length. In general, the coupling length for TM polarization is longer than that for TE polarization. So, Maximum TM polarization coupling length and minimum TE polarization coupling length, allowed to obtain less than -15dB ⊗ -state crosstalk, are 1.1 and 0.9 times EODC length, respectively. Therefore, special care to reduce coupling length mismatch between TE and TM polarizations, was taken when the EODC layer structure was designed. The polarization independent GaAs/AlGaAs EODC structure is shown in Fig.3. A quite small Al composition ratio, 0.1, in AlGaAs cladding layers, was chosen to realize a small refractive index difference between guiding layer and cladding layers, in order to obtain small propagation constant difference between TE and TM polarizations. Since this small refractive index difference might cause higher free carrier absorption loss and higher switching voltage, because of poor optical field confinement, undoped cladding layers between guiding layer and p-cladding layer, and between guiding layer and n-cladding layer, are inserted in order to prevent absorption loss and switching voltage increases.

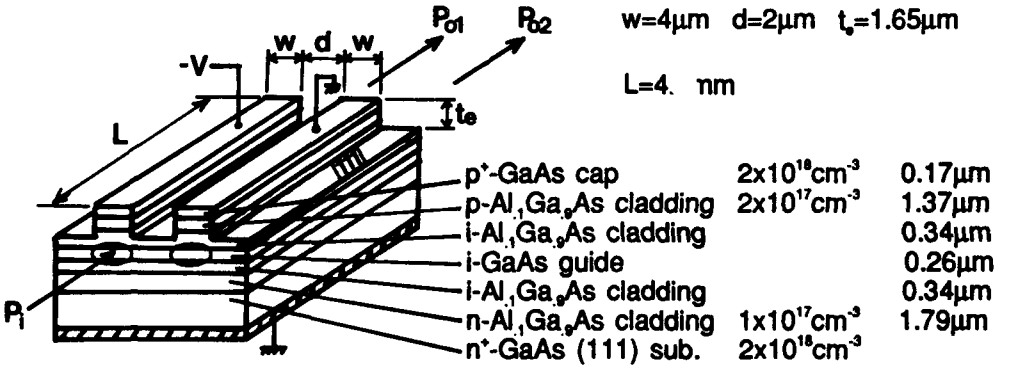


Figure 3. Polarization independent EODC structure.

3. Fabrication and Device Characteristics

The (111)-oriented crystal was grown by MBE (Molecular Beam Epitaxy) with 725° C substrate temperature, which is about 75°C higher than that for (100)-oriented crystals. EODCs with 4μm waveguide width and 2μm waveguide spacing, were fabricated on the MBE grown wafer by using conventional photolithography technique and RIBE (Reactive Ion Beam Etching) with Cl_2 gas.

Fabricated EODCs were characterized by coupling 1.3μm wavelength light into an input waveguide using lens system. Switching characteristics for a 4.2mm long EODC with 4μm wide waveguide and 2μm waveguide spacing are shown in Fig.4. Solid and broken lines represent switching characteristics for TM and TE polarized inputs, respectively, in Fig.4(a), while solid and broken lines indicate those for 45° linear and circular polarized inputs, respectively, in Fig.4(b). Both ⊗-state and ⊖-state were obtained under the uniform $\Delta\beta$ operation at V = 0V and V = 19V, respectively, for any incident polarizations, as shown in Fig.4. The electrode length-switching voltage product ($L \cdot V_\ominus$) is about 80 mm•V, which is 2.6 times larger, mainly due to $\sqrt{3}$ times smaller TE polarization refractive index change, than our conventional polarization dependent EODCs[3], using (100)-oriented substrates. However, the product is still much smaller (4 times smaller) than $LiNbO_3$ polarization independent EODCs[10], which means the switching efficiency of the GaAs EODC

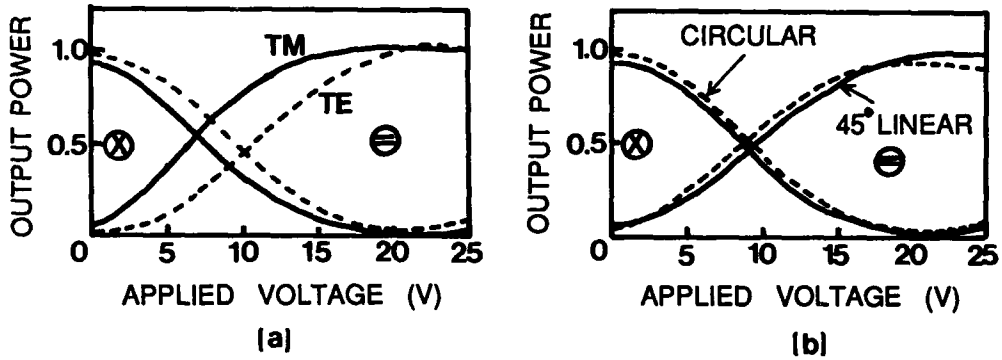


Figure 4. Measured switching characteristics at λ=1.3μm.
(a) For TE and TM polarizations. (b) For 45°linear and circular polarizations.

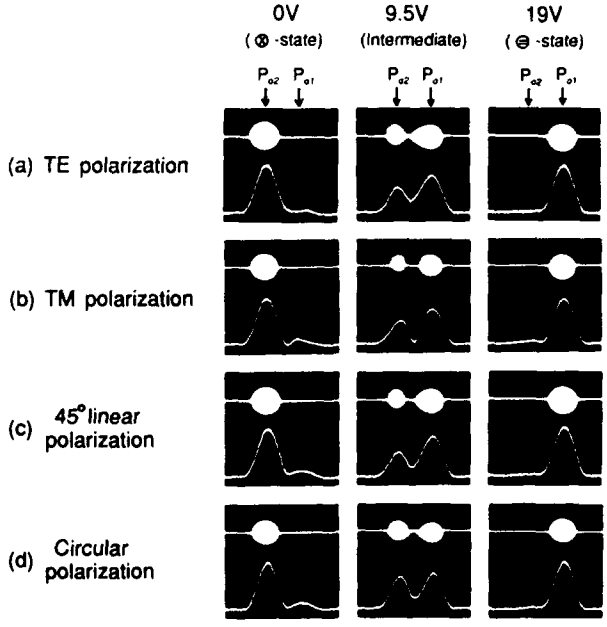


Fig.5 Near field patterns for the EODC's output facet at V=0V, 9.5V and 19V.

Table 1. EODC crosstalk characteristics for various polarizations.

	⊗-state (V=0V)	⊖-state (V=19V)
TE polarization	-15.0dB	-14.6dB
TM polarization	-12.5dB	-13.0dB
45° linear polarization	-12.0dB	-15.5dB
Circular polarization	-12.0dB	-13.7dB

switch is 4 times higher than $LiNbO_3$ EODC switch.

Near field patterns for the EODC's output facet for TE, TM, 45° linear and circular polarization, are shown in Fig.5, at various reverse bias voltages. It is clearly seen that polarization independent switching operation is realized with low crosstalk. Measured crosstalk characteristics for each polarization, are summarized in Table 1. Even worst case crosstalk levels were -12.0dB for ⊗-state and -13.0dB for ⊖-state. The reason why ⊗-state crosstalk for TM polarization is worse than that for TE polarization, is that coupling length for TE polarization is closer to EODC length than that for TM polarization. Estimated coupling lengths are 3.8mm and 4.9mm for TE and TM polarization, respectively.

4. Conclusion

A polarization independent GaAs/AlGaAs EODC switch has been realized for the first time. This result is quite effective to extend application fields of semiconductor EODCs, because standard single-mode fibers can be used as input and output fibers, instead of nonstandard polarization maintaining fibers.

Acknowledgments

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Reduction of the Voltage-Length Product for a Y-Branch Digital Optical Switch

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Abstract

The structure which shows a nearly constant mode coupling peak for a wide range of guide asynchronism is described. The device exhibits low drive voltage and crosstalk.

Introduction

The waveguide type optical switches which operate through modal evolution have attracted much attention by their digital response against applied voltage [1]. The most basic form of this switch is the Y-branch optical switch. Most of the devices reported used straight waveguides to form the Y-branch. Some devices with curved waveguides (shaped branch) were reported recently [2][3]. However, the structure was optimized only for a specific drive voltage and crosstalk. In this report we propose structures which are optimized for a wide range of drive voltages.

Device Structure

The schematic view of the device is shown in Fig. 1. The conventional Y-branch optical switch was composed of straight waveguides (linear branch). In this study, the curved waveguides are used to improve the performance. The length of the electrode measured in the direction of the propagation z is denoted as L and h(z) is the interwaveguide gap.

The first order local normal mode is excited at the branching point (where the coupling coefficient between waveguides is K_0). The power of the first order local normal mode transfers to the waveguide in which the refractive index is enhanced by the electrooptic effect, as it propagates the branch structure. This phenomenon is known as the modal evolution. When the difference of the refractive index between waveguides (dn) is sufficiently large, most of the power of the first order normal mode is in the waveguide in which the refractive index is higher. The drive voltage of the device which operates by this effect shows a threshold characteristic. The precise control of the drive voltage is not needed for this type of device which improves the tolerances.

There are two effects those give rise to crosstalks. Hereafter the crosstalk is defined as a fraction of the output power, i.e., the relative output, in the not intended output port. One effect is the mode coupling and the other is due to the field distribution of the first order local normal mode.

If there is a power transfer (mode coupling)between first order and second order local normal modes, the crosstalk is generated. The most power of the second order normal mode is in the waveguide in which the refractive index is lower than the other, where the interwaveguide gap is large, contrary to the first order mode. The mode coupling effect takes place at two places. The first place is the edge of the electrode near the branching point where the index asymmetry is introduced. The second place is the region in the branch where the geometry of the structure changes along the direction of the propagation. The last effect is reduced by the curved waveguides as will be described later.

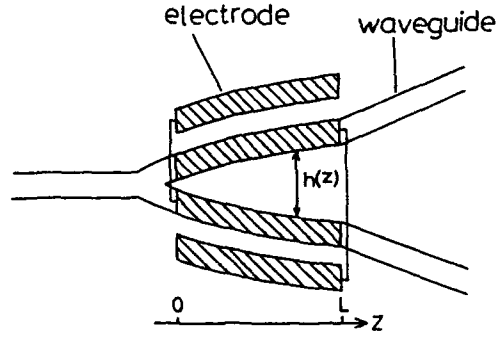


Figure 1. Schematic structure of the Y-branch optical switch.

Optimization of device parameters

The amount of the power transfer between local normal modes at the edge of the electrode is described by guide asynchronism ($\Delta\beta$) to guide coupling coefficient (K_0) ratio X_0. The parameter $\Delta\beta$ is the wave number - index asymmetry product which is proportional to the drive voltage. X_0 should be sufficiently small to reduce the power transfer at the edge of the electrode. Hence, K_0 should be sufficiently large.

At the end of the branch, ideally all the power of the first order local normal mode should be in the waveguide with higher refractive index. However, the actual field distribution of the first order local normal mode is such that some amount of the power remains in the waveguide in which the refractive index is lower than the other. The crosstalk which arises from this effect is expressed by the guide asynchronism ($\Delta\beta$) to guide coupling coefficient (K_L) ratio X_L. The parameter K_L is the coupling coefficient at the end of the branch where the interwaveguide gap is the largest. To reduce the residual power in the not intended waveguide, X_L should be sufficiently large. Thus, K_L should be small to reduce the drive voltage.

We define a parameter R as the minimum to maximum ratio (K_L/K_0) of the coupling coefficient between waveguides. This discussion indicates that R should be sufficiently small. However, a small value of R indicates that the waveguide gap change along the direction of the propagation is large. In this case the mode coupling effect becomes large. Thus from the above discussion, it is known that there is an optimum value for R.

The mode coupling effect tends to be small when K_0 is large. Large K_0 leads to large K_L ($=RK_0$) for fixed R value. Large K_L leads to large $\Delta\beta$ for required crosstalk, which means that the drive voltage will be increased. Thus, there is also an optimum value for K_0.

Mode coupling due to the geometrical change of the structure

The power transfer between local normal modes due to the change of the structure along the direction of propagation can be evaluated using the differential equations. The solution of the differential equation is obtained as the next equation when A_j/A_i is sufficiently small. Here A_i and A_j are the amplitudes of the local normal modes.

$$|A_j/A_i| = |\int C_{ij}\Theta/\Delta\beta_{ij}\exp(ju)\,du| \qquad (1)$$

where $du = \Delta\beta_{ij}\,dz$ and $\Delta\beta_{ij}$ is the propagation constant difference between local normal modes. Θ is the local full branch angle and C_{ij} is the coupling coefficient between local normal modes. This equation shows that the amount of the power transfer depends on the parameter $C_{ij}\Theta/\Delta\beta_{ij}$. The measure of the mode coupling effect [4] is thus defined as

$$\gamma = C_{ij}\Theta/\Delta\beta_{ij}. \qquad (2)$$

The peak value of γ sets the upper bound to the amount of the power transfer between local normal modes. The calculated value of γ is shown in Fig. 3 as a function of the interwaveguide gap h(z) for several values of index asymmetry dn. The calculation was performed using the five layer waveguide structure. The waveguide width was 7 μm, the wavelength was 1.3 μm, the substrate index was 2.14 and the waveguide to substrate index difference was 0.002. The value γ is normalized by k the wave number.

Figure 2 shows that γ peaks at a specific waveguide gap. The peak of γ decreases its level and moves toward a smaller waveguide gap, as the index asymmetry dn is increased.

Another measure of the mode coupling is d, which is the width of the peak measured by the coordinate u. The factor $\Delta\beta_{ij}/\Theta$ appears both in Eq. (1) and expression for d. The value of $\Delta\beta_{ij}/\Theta$ at the γ peak determines the behavior of the γ peak and approximately d.

We can evaluate these parameters using the coupled-mode representation which is a powerful prediction tool. In this representation, the peak of γ denoted as γ_p is given by

$$\gamma_p = (1/4K_0)[X_p/(X_p^2+1)^{3/2}] \times \gamma_3\Theta_p\exp[\gamma_3(h_p-h_0)] \qquad (3)$$

Here, h_p is the interwaveguide gap where γ peaks, h_0 is the interguide gap at the edge of the electrode and γ_3 is the transverse momentum component of the light field in the region between waveguides. The parameter X_p is the guide asynchronism ($\Delta\beta$) to the guide coupling coefficient (K(z)) ratio at the γ peak and Θ_p denotes the value of Θ at the peak.

Change of the characteristics owing to the curved waveguides

As shown in the previous section, the level of the peak γ_p is proportional to the local full branch angle as indicated by Eq. (2), and as the index asymmetry is increased the peak moves toward a smaller waveguide gap and decreases its level. Thus, if the local full branch angle is altered along the direction of the propagation in a specific manner, the characteristics of the Y-branch are expected to change.

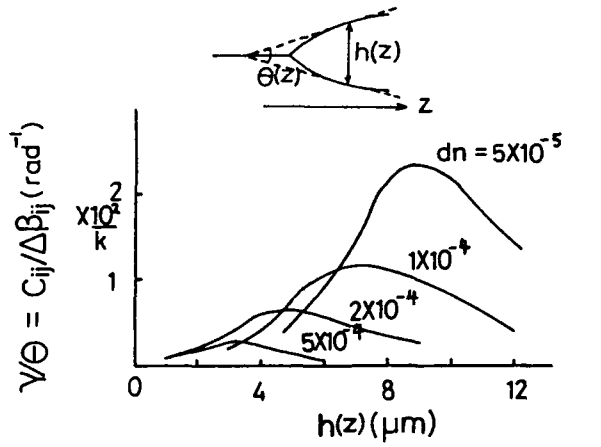


Figure 2. Calculated measure of the mode coupling effect γ as a function of interwaveguide gap h(z) and index asynchronism dn.

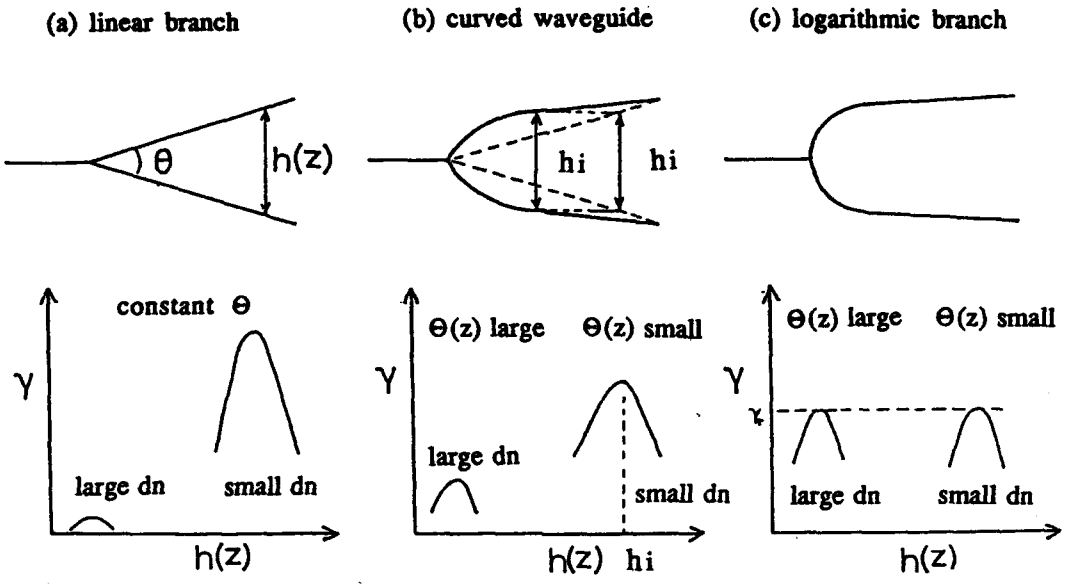


Figure 3. The measure of the mode coupling γ for several branch structures.

In Fig. 3 the schematic description of the measure of the mode coupling effect γ for various branch structures is shown. Figure 3(a) shows the case for the linear branch. This figure is essentially the same as Fig. 2. When the local full branch angle is decreased at a large waveguide gap (denoted as hi in Fig. 3(b) and increased at a small waveguide gap, the level of the peak becomes nearly constant for a wide range of index asymmetry dn. The level of the peak at a small index asymmetry becomes smaller than the linear branch in Fig. 3(b), which indicates that the drive voltage will be reduced.

From the analysis of the mode coupling effect, it is shown that the waveguide gap should be a logarithmic function of the propagation distance to gain the constant peak level (Fig. 3(c)) as we now show.

From Eq. (3) it is known that if the structure is designed in the condition

$$\Theta \exp[\gamma_s(h(z)-h_0)] = \text{constant} \qquad (4)$$

then the peak level γ_p becomes independent of $\Delta\beta$. In this condition h(z) is given as

$$\gamma_s(h(z)-h0) = \ln[(R^{-1}-1)z/L+1]. \qquad (5)$$

These assumptions are verified in Fig. 4. The calculation was performed by the coupled-wave equations. Although the branch with logarithmic curve shows low $\Delta\beta L/\pi$ value to switch the device, the crosstalk is high for experimentally available K_0L value.

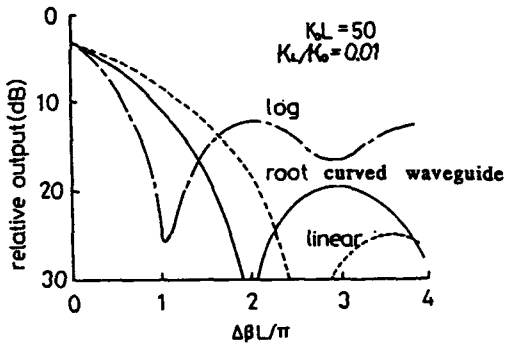


Figure 4. Examples of calculated response curve for various branch structures.

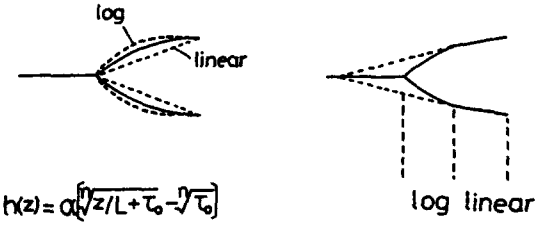


Figure 5. Two preferred structures.

Two preferred structures

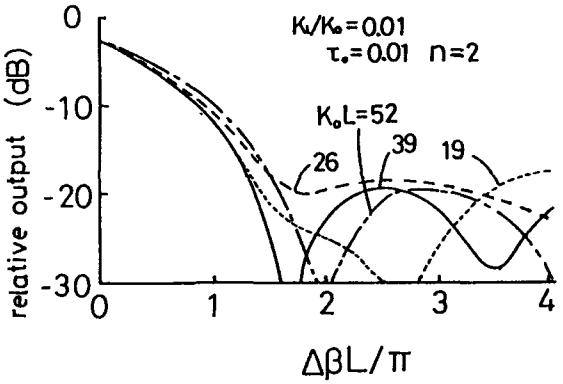
The device composed only of the logarithmic branch exhibits large crosstalk as shown previously. To overcome this problem, we propose two structures. One structure is the intermediate between the linear branch

and the logarithmic branch. We name this structure type I. The other is the structure which is described as a linear branch replaced by the logarithmic branch near the branching point, i.e., the composite structure. We name this structure type II. These are depicted in Fig. 5(a) and (b). We used a waveguide curve expressed by the equation shown in Fig. 5(a) for type I structure. For type II, the linear branch and the logarithmic branch are connected in the condition of yielding the smallest full branch angle for the linear part of the branch.

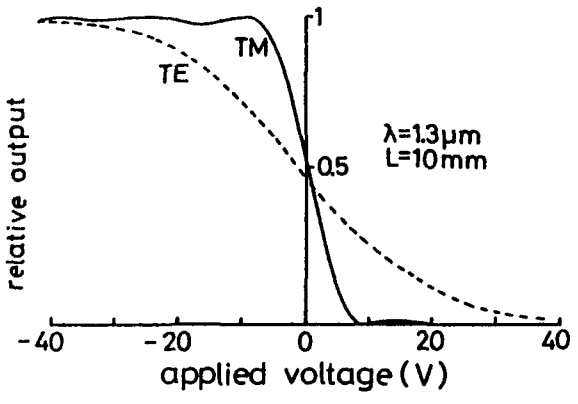
Device Performance

Experimental conditions

The devices were fabricated on z-cut $LiNbO_3$ substrate. The Ti stripe width and thickness were 7μm and 600Å respectively. The diffusion temperature was 1050°C and the diffusion time was 6 hours. The 4000Å thick SiO_2 was used as a buffer layer. The electrode was placed above the buffer layer. The semiconductor layer was used to prevent the pyroelectric effect. The maximum interwaveguide gap was 8.5-9 μm. The interguide gap at the edge of the electrode near the branching point was 1μm. These values were selected to yield R value of 0.01 and K_0L of 30-50. The length of the electrode was 10mm. The voltage-length product of the directional coupler fabricated in similar condition was 9 Vcm.

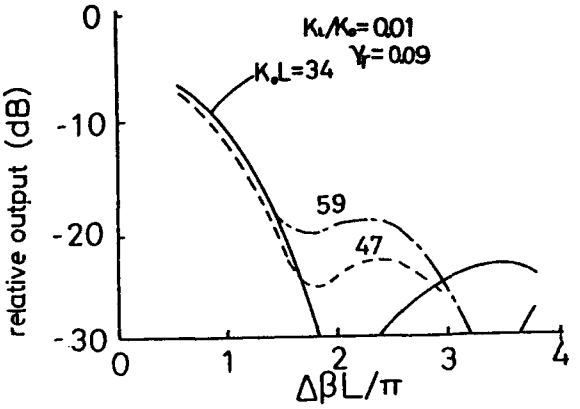


(a) Calculated response curve

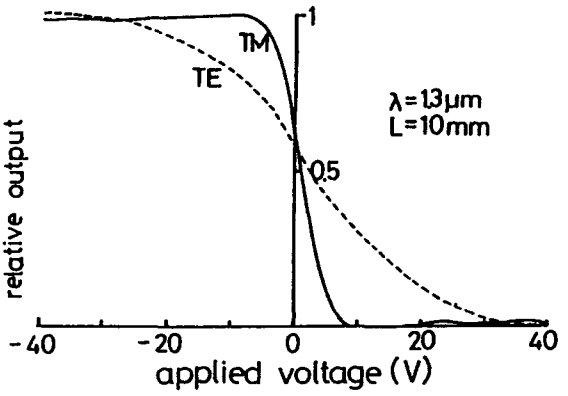


(b) Measured response curve

Figure 6. Calculated and measured response curve for the device with type I structure.



(a) Calculated response curve



(b) Measured response curve

Figure 7. Calculated and measured response curve for the device with type II structure.

Type I

The calculated response curve of the device with type I structure is shown in Fig. 6(a). The calculation was performed using the coupled-wave equations. From the calculated results it is known that crosstalk of less than -20dB is obtainable above $\Delta\beta L/\pi$ value of 1.4-1.7 for various K_0L values. The immunity to the KoL value deviations indicates the large fabrication tolerance of the device.

The measured response curve is shown in Fig. 6(b). The fabricated device was optimized for the TM mode at 1.3μm wavelength. The full swing voltage (= twice of the drive voltage) to achieve 15dB crosstalk was 14V for the TM mode. To achieve 10dB crosstalk the swing

voltage was 10V. For the TE mode, the full swing voltage to achieve 15dB crosstalk was 60V.

Type II

The calculated response curve of the type II structure is shown in Fig. 7(a). From calculated results, it is known that crosstalk of less than -20 dB is obtainable above $\Delta\beta L/\pi$ of 1.5 for various K_0L values.

The measured response curve is shown in Fig. 7(b). The fabricated device is optimized for the TM mode at 1.3μm wavelength. The measured full swing voltage to achieve 15dB crosstalk was 13V for the TM mode. For 10dB crosstalk the full swing voltage was 9V. The parameter γr is the level of the γ peak at the logarithmic part of the branch. For the TE mode, full swing voltage was 56V to achieve 15dB crosstalk.

2x2 switch

The schematic structure of the 2x2 switch using our method is shown in Fig. 8. The measured swing voltage to achieve 15dB crosstalk was 15V for the device with 10mm long electrode at 1.3μm wavelength TM mode. The design of type I was used.

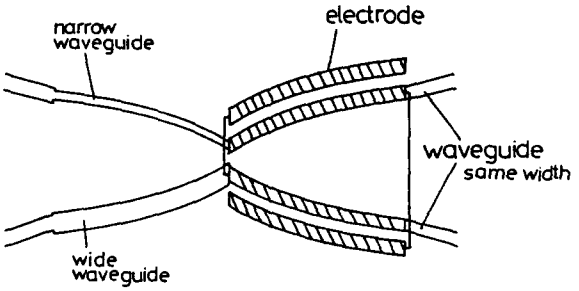


Figure 8. Schematic structure of the 2x2 switch.

Conclusion

Two preferred structures, i.e., the intermediate structure and the logarithmic-linear composite structure, are proposed. These structures show low drive voltages and low crosstalks. The voltage-length product was as low as that of the directional coupler. To achieve the constant mode coupling peak, the interguide gap should be the logarithmic function of the propagation distance. The design was applied to the 2x2 switch and the basic performance of the device was demonstrated.

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Optical Access Switch: First Photonic Switching Demonstrator within the RACE Program

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Abstract

We present the architecture and systems performance measurements for the first photonic switching demonstrator within the European RACE program, an Optical Access Switch. Other applications and evolutionary aspects are discussed.

Introduction

Photonic switching is expected to be important in solving the switching bottleneck in future broadband communications systems, where the requirements on the switches can be increased by as much as three orders of magnitude. The first application of photonic switching is expected to be in the transport network: to increase its capacity, flexibility and reliability.

In this paper, we describe the first photonic switching demonstrator within the European RACE program. The system demonstrated is an Optical Access Switch, in the context of a broadband local exchange. Systems architecture, hardware as well as systems performance are described. Evolutionary aspects in the systems and technology areas will be treated.

Objectives

The objectives of the Optical Access Switch Demonstrator are to demonstrate the application of optical switching in a future broadband local exchange and to evaluate the performance of optical switches in a switching fabric. The realization of the demonstrator is also expected to give important experience valuable for the implementation of new demonstrators using the latest technology in the field of optical switching.

System Environment for an Access Switch

The future broadband local exchange is assumed to comprise an Access Switch which has the function to switch bidirectional Interface Blocks (IB's) at 155.520 Mb/s from the subscriber lines to anyone of the following:

- The trunk network, via a Digital Cross Connect (DCC), in the case the IB is a leased line
- A Distributive Services (DS) STM switch, for example used for TV distribution
- A Communicative Services (CS) STM switch for different kinds of communicative services
- An ATM switch for all types of ATM services

Associated with each subscriber line is a Line Termination / Exchange Termination (LT/ET) which also performs electronic multiplexing and demultiplexing of IB's. The block diagram of the local exchange is shown in Figure 1.

The Optical Access Switch Demonstrator

The demonstrator has all the functions of the above mentioned Access Switch with some exceptions. The implemented functions are distributive switching (demonstrated with selective TV broadcasting), communicative switching (demonstrated with communicative video) and concentration (used for cost reduction).

No LT/ET devices are used at the subscriber termination. Hence the subscriber fibres are carrying only one IB each, nevertheless bidirectional communication is performed on the fibres using Wavelength Division Multiplex (WDM). Furthermore, the actual bit rate in the demonstrator is 140 Mb/s. The reason for this is that com-

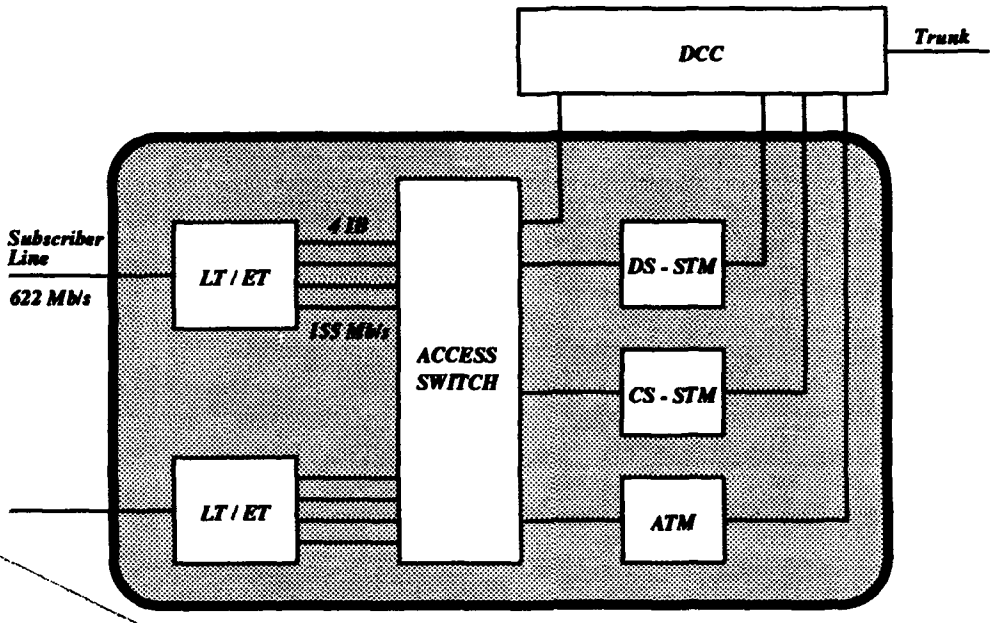


Figure 1. A Broadband Local Exchange. The Access Switch has the function to switch Interface Blocks from the subscriber lines.

mercial equipment such as optical transmitters, optical receivers, coders and decoders are easily available for this bit rate.

The switching components used in the demonstrator are 4 × 4 optical switch matrixes developed by Ericsson (1). The switch matrixes are made in $LiNbO_3$ technology with the following main characteristics:

- Polarization independent
- Cross-talk < -20 dB (optical)
- Insertion loss ≈ 10 dB
- Broadcasting capabilities
- Strictly non-blocking
- Available for either the 1300 nm or the 1550 nm windows
- Switching voltage ± 60 V, 3 dB splitting at 0 V

In Figure 2 the structure of a switch matrix is shown. It is composed of 24 1 × 2 switch elements in a splitter-combiner structure. Each switch element can be set to one of three states: input power transferred to output 1, input power transferred to output 2 or input power equally split between the outputs.

The Optical Access Switch can terminate up to eight subscriber lines. The wavelength 1550 nm is used for the incoming IB's and the wavelength 1300 nm is used for the outgoing IB's. The transmission directions are demultiplexed in WDM's at the subscriber termination in order to make it possible to switch the different wavelengths separately. This is necessary due to the fact that the switch matrixes are designed for a specific wavelength window (1300 nm or 1550 nm). To perform communicative switching between two subscribers, some kind of wavelength conversion is required. In the demonstrator this is performed by a 1550 nm receiver and a 1300 nm transmitter coupled back-to-back. The Optical Access Switch is shown to the upper right in Figure 3.

An incoming signal on one of the subscriber lines first enters a WDM, which separates the incoming signal from the outgoing signal. Then it enters the optical 1550 nm switch matrixes which switches the signal towards the wavelength converters. Then the signal is switched out through the 1300 nm switch matrixes and is multiplexed onto the pertinent subscriber line.

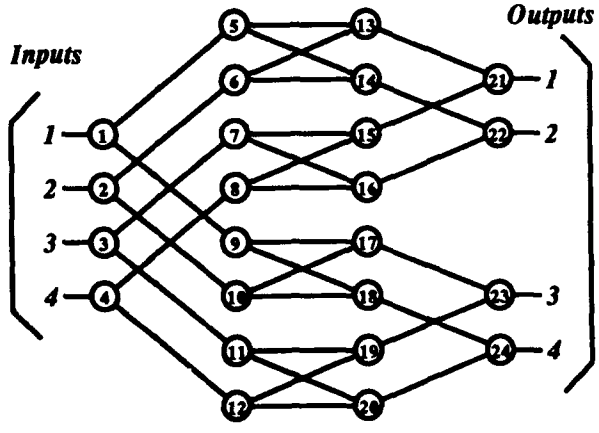


Figure 2. Internal structure of a 4 × 4 optical switch matrix. Every output can be connected to an arbitrary input.

The optical switch matrixes are controlled via a serial interface with logical levels. In the demonstrator no signalling takes place, which means that the routing has to be externally controlled. This is done by a PC via the serial interface. A special software which performs automatic or manual routing through the Optical Access Switch has been developed.

A total of four subscribers with different equipment are connected to the Optical Access Switch. Two of the subscribers are equipped with a TV-monitor and a video telephone. The videotelephone is composed of a TV-monitor and a camera and could thus be used also for watching TV programs (multifunction terminal). These subscribers need two IB's each, and this is arranged by assigning two subscriber lines each to them. The other two subscribers are equipped with a single TV-monitor and no video telephone.

The distributive services are supplied from of a Service Provider which can distribute two TV-channels to an arbitrary number of the connected subscribers. The distributive channels are inserted in two of the switch matrixes in the Optical Access Switch as shown in Figure 3.

All TV signals in the system, including voice, are coded to 70 Mb/s and carried in a 140 Mb/s structure (= 1 IB) in which the excessive capacity is not used. All coders and decoders used in the demonstrator are system components from Ericsson's Fiber Optical CATV System. Similarly, the optical transmitters and receivers are products from Ericssons's 140 Mb/s Fiber Optical Line Transmission System. The WDM components are made by JDS.

Performance Measurements

The optical switch matrixes are the major source for power losses in the optical signal path. The loss through each switch matrix is about 10 dB. However, the span between the transmitter output power level and the receiver sensitivity is 33 dB, which still gives us a good power margin in the system.The power levels and the loss distribution in the Optical Access Switch for a distributive connection are shown at the top in Figure 4.

The cross-talk introduced from the communicative connections and the distributive connections have both been investigated. In the case of communicative connections the signal has passed through two cascaded optical switch matrixes and no switch element is set in broadcasting mode. The cross-talk was found to be < -25 dB in every routing case (in 70% of the cases < -30 dB) with the distributive signal sources turned off. In the case of distributive connections the signal was broadcast to two output terminals and the cross-talk at the other terminals was measured. The cross-talk was found to be < -12 dB in every routing case (in 70% of the cases < -16 dB). The cross-talk from the communicative signal sources was in this case negligible.

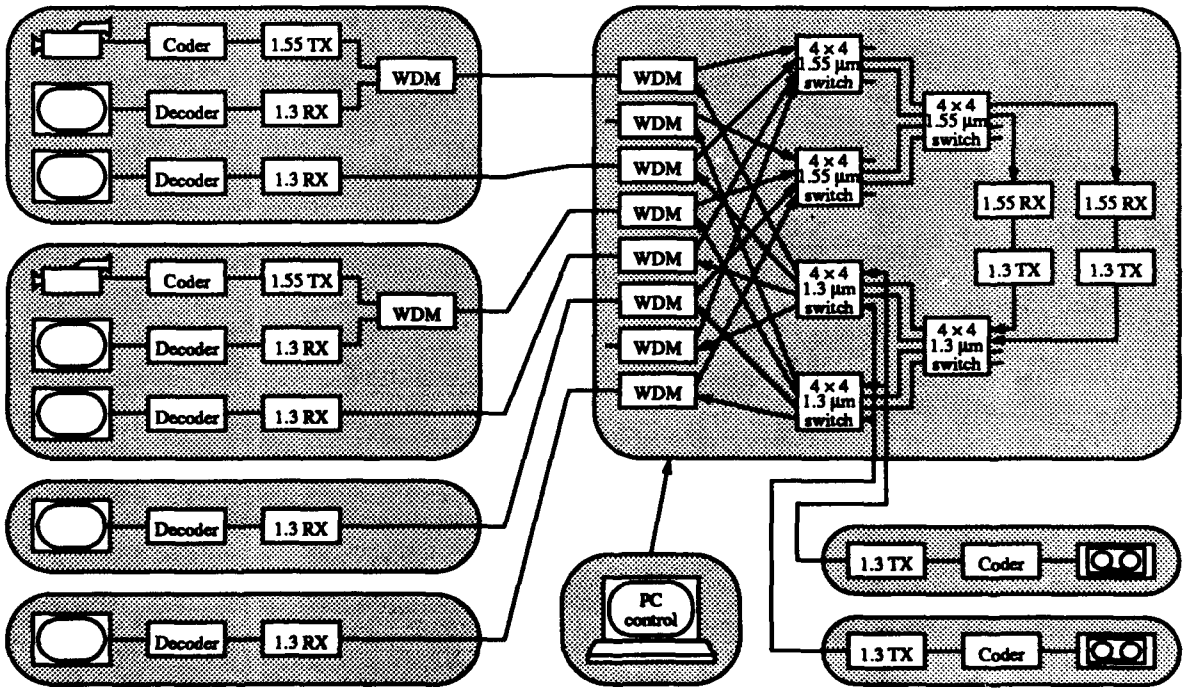


Figure 3. The Optical Access Switch Demonstrator configuration. Four subscribers (left) and two distributive TV sources (bottom right) are connected to the Optical Access Switch (upper right) which can perform communicative and distributive video switching. The Optical Access Switch is controlled from a PC.

The system penalty originated from the degradation of the receiver sensitivity due to the insertion of the Optical Access Switch and the system penalty originated from different cross-talk generating sources are measured. For both halves of the communicative connections (transmitter to wavelength converter and wavelength converter to receiver) the system penalty from the Optical Access Switch is very low, < 0.1 dB. The cross-talk from the other communicative signal source has no significant influence on the BER in this case. In the case of distributive switching, only the 1300 nm switches are of interest in the given architecture. The result of the measurements

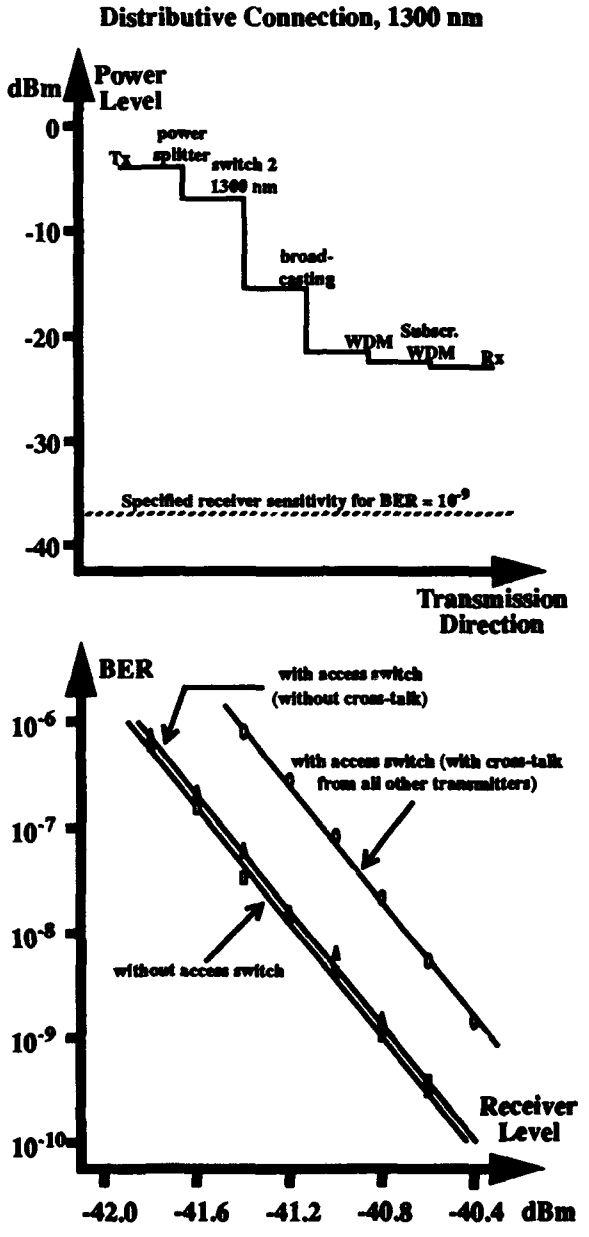


Figure 4. The power loss distribution and the system penalty for a distributive connection.

are shown at the bottom in Figure 4. As for the communicative connection, the penalty originated from the Optical Access Switch is < 0.1 dB. In this case the cross-talk from the other distributive signal source degrades the system, but the total penalty is still < 0.5 dB. The cross-talk from the communicative signal sources is negligible.

Technology Upgrade and Evolutionary Aspects

In order to implement a reasonably full scale system of the kind reported here, upgrades in a number of technology areas are necessary. The size of the Access Switch has to be increased significantly. Here, larger monolithic matrixes can be made in InP, integrating optical amplifiers and switches (2) or using Er fibers as amplifiers. The sizes can further be increased by using optical interconnects, e g involving optics on Si, to cascade switch chips. As far as cross-talk and losses are concerned, required switch sizes are feasible (3),(4). Another important upgrade concerns using multiple wavelengths to increase the capacity of the switch. The way the routing information is transferred to the switch is also important. In the case of using multiple wavelengths, the routing information could be provided to the switch on a specific wavelength, especially assigned for signalling, maintaining the transparency of the system. Photonic switching is of great interest even for other system applications than the Access Switch. One example is the Optical Cross Connect. All these areas are subjects of our current work.

Acknowledgments

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Space-Division Switching (free-space)

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Design Issues in Free-Space Optical Interconnection of Switching Systems

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Abstract

The design of free-space digital optical systems is discussed. Several examples are presented which emphasize the interdependence of each component.

1. Introduction

Two methods exist for communicating high bandwidth information; light and electricity. It is clear that the optimum choice for long distances (~1km) is light hence the adoption of fiber for telephony. It is equally clear that over short distances (<1mm), the optimum choice is electricity hence its use for gate-to-gate interconnection in a chip. It has been shown that as the distance between the transmitter and receiver increases, the energy required by an electrical connection, increases more rapidly than if optics is used[1]. It is difficult to justify the use of optics over short distances and conversely, electrical connection is not ideal except over the shortest distances. The ultimate optimum choice for chip-to-chip and board-to-board interconnection is unclear.

There is interest in 'enhancing' the interconnection of electronic logic using optics (OEICs). There may be some, as yet unidentified, combination of circumstances (number of connections, bandwidth, interconnection distance, fan-out, noise and ground loop immunity, reliability, functionality, cost, weight and size) where optical interconnection is the most appropriate choice. Individual LEDs and lasers coupled into a fiber connected to a detector are already being used in high performance computers to provide some of the connections between frames. One-dimensional arrays (~18) of fiber ribbon connectors are also available for this purpose. There is research on optical backplanes which provide the connections using guided waves in polyimide.

Free-space digital optics is one extreme of the possible alternative roles light may play; massive interconnection density with over 1000 channels operating in parallel. Free-space may ultimately provide larger interconnection density than conventional electronic techniques. At this time, large arrays of emitters or modulators interfaced directly to conventional silicon-based logic are unavailable. The growth of direct gap semiconductors (such as GaAs) on silicon and attaching an array of optical modulators or emitters to an electronic chip using a technique such as flip-chip (bump-bonding) are both addressing this problem. System issues will continue to be investigated using optically bistable devices until these technologies succeed.

The recent development of large two-dimensional arrays of digital, optically bistable devices has facilitated the construction of test-bed, free-space photonic switches[2,3] and optical processor sub-systems[4,5]. The high switching energy (~several picojoules) and low functionality of bistable devices limits the usefulness of these proof-of-principle experiments. Lower energy devices with increased functionality, so-called 'smart' pixels, are being developed. There is a need to separate the three functions performed by the device; detection, thresholding and modulation (or emission). This will only be achievable with the integration of between several and a hundred electronic gates between the detectors and the modulator (or emitter) of each pixel. Thus there are two directions which will eventually converge to a similar family of devices. One adds optical 'ports' to VLSI, the other adds electronics to an optical port.

It is a desirable goal to decouple, as much as possible, the design of each component within a system. Free-space photonic switching is currently in a phase of technology development. It is likely that every electro-optic,

optoelectronic, optical and mechanical component that is currently being used will be changed in future systems. There is latitude for improvement in almost every aspect of each component. Decoupling would simplify the independent development of components. However, this is not yet possible to a significant degree. The aim of this paper is to emphasize the interdependence of each component within a system and show that it is vital to consider the overall system performance when judging the impact of improvements in each component or sub-system.

High density interconnections are required in a switch fabric. The fabric is the part of the switch which routes data from the input to the required output. The input to the *switch* is not in a format suitable to send directly to the fabric. It includes the routing information required by the computer controlling the switch, the path hunt processor, and signalling protocol information that must be extracted and processed. The input data must also be re-synchronized and bit-aligned. Therefore, the operating wavelength of the fabric is unconstrained. It does not need to match the transmission wavelength. Similarly, with demultiplexing, the fabric data rate does not need to match the transmission data rate.

2. Devices

The suitability of optically bistable devices providing high interconnection density in a switching fabric is being assessed. Each two-dimensional array provides data regeneration in a manner similar to electronic gates. Thus, although the devices must switch states at the fabric data rate, high output contrast and low loss are not required. Any comparison with systems using data 'transparent' devices, such as lithium niobate waveguides, is complicated since they operate as relational rather than 'logical' (or latching) devices[6].

The interdependence of each component can be illustrated by considering the devices used in a free-space switch. The switching energy of the most promising device demonstrated (GaAs Symmetric Self Electro-optic Effect device: S-SEED) is low enough (~5pJ) to allow the operation of small arrays (~250) at slow speeds (<MHz) with a single 10mW diode laser powering the whole array. One effect of operating these devices with the incorrect wavelength (~2nm from optimum) is a reduction in contrast from ~6:1 to ~2:1[7]. The optimum wavelength is temperature dependent due to the temperature dependence of the GaAs bandgap.

The output wavelength stability of a 'single-mode' diode laser is poor. The emitted wavelength is a narrow line only in a small range of current and temperature. These lasers are attractive because of the relative ease with which they can be modulated, low cost and small size. However, the emitted wavelength at constant current may vary by 2nm or more after the current has been changed since a constant laser temperature may not be reached for several microseconds after the current pulse. An external modulator or a sophisticated laser structure may be required unless a device such as a S-SEED, which is relatively insensitive to contrast and wavelength since it is a differential device, is used. A system which is tolerant to a range of contrasts is advantageous since it allows a reduction in sensitivity to both device temperature and laser wavelength.

Device area is another factor which determines the performance required by the other components. The device switching energy is linearly dependent on its area[7]. Thus, it is desirable to use the smallest possible devices. However, small device area has drawbacks. The lens f-number required to efficiently couple the light from the laser into the device must be small. For example, whereas a diffraction limited f/3 lens will couple 99% of an aberration-free 850nm beam incident on it into a 10μm diameter device, a f/1.5 lens is required if a 5μm diameter device is used. In addition, the depth of focus of the spot size required by the smaller device is four times smaller. A six-axes goniometer may be required to align the array of devices with the array of focussed beams. This may be both the largest and most expensive component in an experimental system. The smaller device size necessitates higher precision in all 6 axes: by a factor of four in tilts and translation along the optical axis and by a factor of two in roll and the other translation axes.

Another effect of a decrease in device area involves the other optical components. The decrease in f-number required can be achieved either by increasing the spot size of the collimated beam incident on the lens or decreasing the lens focal length. Any other lenses in the system, such as those used in the interconnect are affected by these changes. The usable aperture of the other lenses (the diameter which is corrected for aberrations if a diffraction limited optical system is required) must accommodate any increase in the collimated spot size. In addition, any decrease in focal length entails a magnification change. The spacing between the array of laser sources, typically provided by a phase grating or a microlaser array, is determined by the magnification.

Device spacing (S) is another parameter which is strongly coupled to the specification of the other components. Small device spacing is required to maximize the number of devices within the field of view of the lens. The flatness of the field required is determined by the depth of focus, image tilt introduced optically and device tilt uncorrected by the device mount. In addition, the allowed distortion introduced by the lens over this field is dependent on the type of interconnect used and the device area. Consequently, the specification of the lens is highly dependent on the device spacing.

3. Array Generation

Phase gratings are often used as power splitters to divide the power from the source into a square array (NxN) of equal power beams. The performance of a phase grating couples and constrains the number, size and spacing of beams since the period must simultaneously satisfy three constraints.

i) The phase grating period P is equal to $2\lambda f/S$ (typically P~1mm)[8].

ii) The number of beams (N) determines the size (<P/N) and number of features (~N) within one period.The minimum feature size it is possible to fabricate (typically >1μm) thus determines the minimum period size.

iii) Aliasing, which results in power non-uniformity, may occur if insufficient periods are sampled by the beam. No significant degradation in uniformity due to this effect is noticed if the ratio of the diameter of the Gaussian beam to the period is greater than ~3.

Fortunately, small arrays (N<64) of closely spaced (S=40μm) devices and readily available, fast (f/#<1.5) lenses are compatible with these constraints. Device spacings less than ~15μm result in both undersampling of the grating period by the beam and a requirement to use fast, short focal length lenses with large angular fields (>8 degrees). Device spacings of greater than ~100μm require fast, long focal length lenses (>18mm) with large angular fields (>28 degrees). The requirement, with this low fill-factor, of such a large field is so undesirable that alternative illumination methods must be considered[9].

Diffractive array generation may constrain the laser wavelength more tightly than the device characteristics. The distance of the focussed beams at the corners of the array from the optical axis is $\sqrt{2}(N-1)\lambda f/P$. Consider the situation with N=16, S=20μm and a device diameter of 5μm[3]. In this case, an error in wavelength of 2nm changes this distance by 0.5μm. However, the position shift, 2μm, with a larger array (N=64) may not be negligible.

4. Optical Interconnect

Two digital, free-space switching system demonstrations have been constructed using S-SEEDs[2,3]. Both use the crossover interconnect which is topologically equivalent to the shuffle[10]. This interconnect was chosen because of its unique properties of being, in principle, both lossless to power and optical resolution. Other interconnects which are topologically equivalent to the shuffle involve either anamorphic magnification of the image, the use of a separate lens or series of lenses for each channel or an array of lenses. These alternatives are unattractive since the demonstration systems are intended to operate with diffraction-limited performance to maximize energy coupling into the small devices.

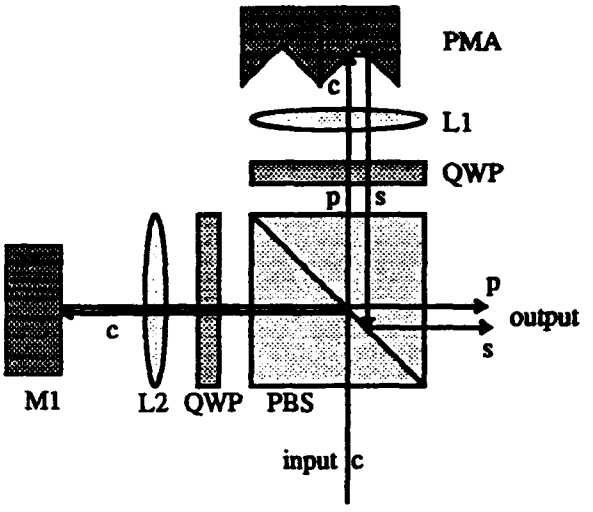


Figure 1. Schematic of the optical components in the crossover interconnection, p, s and c are polarization states.

The output of the crossover interconnect are two arrays of beams; one array is a copy of the incident array, the other is the 'crossed' version (Figure 1). In these demonstrations, the array is generated using a phase grating. The two arrays of beams are therefore mutually coherent. Two beams, one from each array, are incident on the same area of each S-SEED to minimize device area. A feature of the crossover is that the two arrays of beams have orthogonal polarizations and interference is avoided. The drawback with this technique is that a complicated optical arrangement is required to 'losslessly' combine the two beams on the S-SEED along with another required to read out its state. The arrangement involves a triple isolator (a polarizing beam splitter with three quarter wave plates attached to it), two high quality lenses and two patterned mirrors which must both be moved in four axes (Figure 2).

In addition, the interconnect itself requires a double isolator, two lenses, a mirror to provide the straight connection and an array of roof mirrors to provide the crossed paths. The roof mirror array is also mounted on a four axes micropositioner. The precision to which it is necessary to align the degrees of freedom in this optical arrangement is linearly dependent on the magnification between the S-SEED array and the array of roof mirrors. Thus, it is impossible to decouple the design of the interconnect from the design of the rest of the system since the focal lengths of the lenses used throughout the system, determine the precision to which it is necessary to fabricate the array and the quality of the optomechanical components used.

5. Uniformity

A system based on S-SEEDs performing logical decisions on data inputs has been constructed[3] (Figure. 2). In such a system, the uniformity of the power levels in the array of beams is important. Differential gates operate correctly only with a small variation (~20%) in the uniformity.

Image plane misalignment is another source of non-uniformity. A system with six image planes and involving six passes through a polarizing beam splitter has been operated[3]. Non-uniformity couples the components since the angular performance of lenses and beam splitters can only be specified if the non-uniformity introduced by the image planes can be measured.

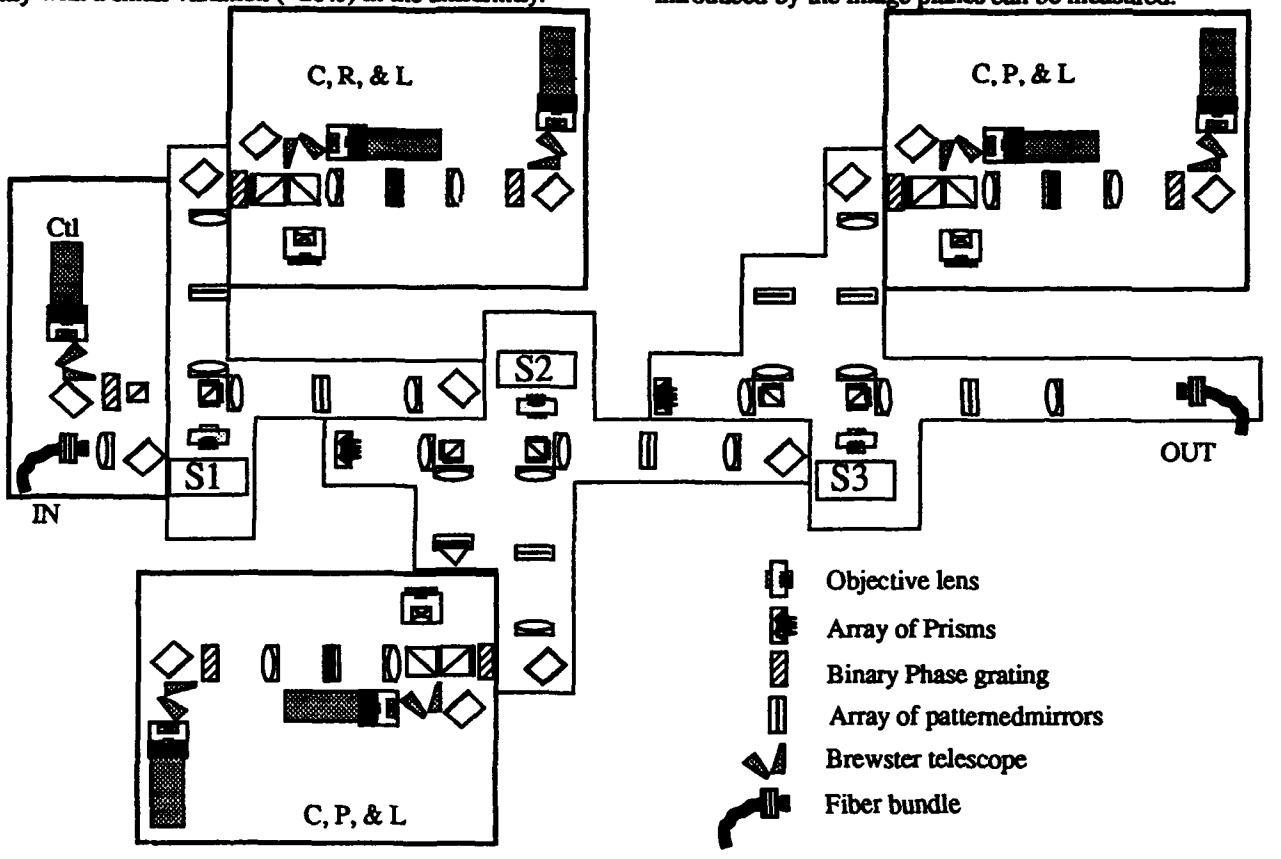


Figure 2. Schematic of a demonstration system which interconnects 3 S-SEED arrays (S1-3).

How this variation is divided between the many possible sources, the non-uniformity 'budget', is another source of 'coupling' between components. Typically, the source array (BPG) contributes +/-4%. This may be dependent on the minimum feature size and sampling error and is therefore coupled to the specification of the other components.

The performance of each lens in any system degrades at higher field angles. Thus one would expect that after passing through several lenses, even though they may be well-corrected, the off-axis beams would be aberrated more than those in the center of the field. Another source of degradation of off-axis beams is the small angular field of polarizing beam splitters. The transmittance of p-polarized light drops to ~95% of the zero field transmittance at a field of 5 degrees.

Similarly, the allowable variation in the phase grating is dependent on the non-uniformity introduced by every other component. It is not helpful to blindly demand improved performance in some characteristic of a component since it is rarely achievable without cost. For example, the field of view of a PBS can be increased using high index glasses which give rise to higher fresnel losses. The field of lenses may be increased by an increase in focal length or adding elements, both of which may be undesirable.

6. Conclusion

This paper has detailed some of the ways in which the specification of each component of a digital free-space photonic switch are coupled. Such systems may ultimately be capable of providing massive connectivity of high speed signals. The production of large 2-dimensional arrays of optical devices which are cascadable has enabled a new technology. This is a recent development. Consequently, only a few free-space digital optical circuits have been constructed. The systems operate with a performance well below that achievable with conventional electronics. However, their construction validates the confident prediction of the feasibility of more viable full scale systems. It also enables the assessment of both components and architectures in a test-bed system, providing feedback to improve individual aspects of the overall system.

Oftentimes, substantial improvements in individual components are possible only at the expense of other aspects of the system. This mistake is avoided by channelling the developer's attention on the system as a whole rather than individual components. The design, construction and successful operation of complex systems are important milestones in the development of a new technology. They play an invaluable role in focussing the attention on the practicality of free-space digital optics. Only by the construction of such demonstration systems is it possible to prove that the technology is feasible.

7. Acknowledgments

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Extended Generalized Shuffle Network Architectures for Free-Space Photonic Switching

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Abstract

A new class of switching topologies known as Extended Generalized Shuffle (EGS) networks is presented, and we show that the flexibility of these network makes them well-suited for photonic switching applications. We then analyze the hardware costs (# S-SEED arrays) and various operating characteristics (blocking probability, fault-tolerance, and system downtime) of these network topologies. We also present a new type of switching node (a 2-module) for use in EGS networks, and we show that 2-modules can be efficiently implemented using available optical logic devices. It is shown that an optical implementation of these networks may yield a cost-effective way to capitalize on the bandwidth and parallelism of free-space optics.

1. Introduction

To efficiently utilize the bandwidth and parallelism offered by free-space optics, new switching network topologies must be developed that can capitalize on the novel benefits of photonics while circumventing its short-comings. In particular, the topologies must (1) take advantage of 3D connectivity between planar arrangements of optical logic devices, (2) use interconnections that are easy to implement in optics, (3) require low fanin and fanout on the logic devices to maintain large noise margins and signals levels, (4) offer a high degree of fault-tolerance for the emerging logic devices, and (5) be flexible enough to adapt to changing technologies. In addition, the topologies should provide very low blocking probabilities and should permit multi-casting operations for switching of broadband video and data traffic in the future.

We will describe a new class of network topologies called Extended Generalized Shuffle (EGS) networks that satisfy all of these requirements[1]. We will also describe a new type of simple switching node (called a 2-module) which can be used effectively for routing data within an EGS network. We will then study the unique trade-off between hardware cost and blocking probability within the EGS class of networks. Finally, we will analyze the fault-tolerance and the system availability of EGS networks that are implemented using "real world" devices which may exhibit failures.

2. Background on EGS networks and 2-modules

An N-input, N-output multi-stage interconnection network (MIN) contains multiple stage of nodes (node-stages), and each consecutive pair of node-stages is connected by the links within a link-stage (Fig. 1). Nodes provide the active routing of data, while links passively transport data from one node-stage to the next. The nodes within a MIN can be implemented in many different ways[2], and the functionality of the node will affect many of the operational characteristics of the MIN. In a photonic implementation of a MIN (Fig. 2), the nodes can be implemented using optical logic device arrays in which the data signals are modulated beams of light propagating orthogonal to the device arrays (such as Symmetric SEED or S-SEED arrays)[3]. The link-stage connections can be provided by directing these beams of light through free-space using bulk optical components (lenses, mirrors, etc.). Control of a MIN is often placed in a centralized processor which calculates available paths through which new data can be routed, and the results of this path hunt operation are injected as control signals into the nodes of the MIN.

EGS networks[1] are a broad class of MINs that do not place any restrictions on the number of nodes within the node-stages or on the number of node-stages within

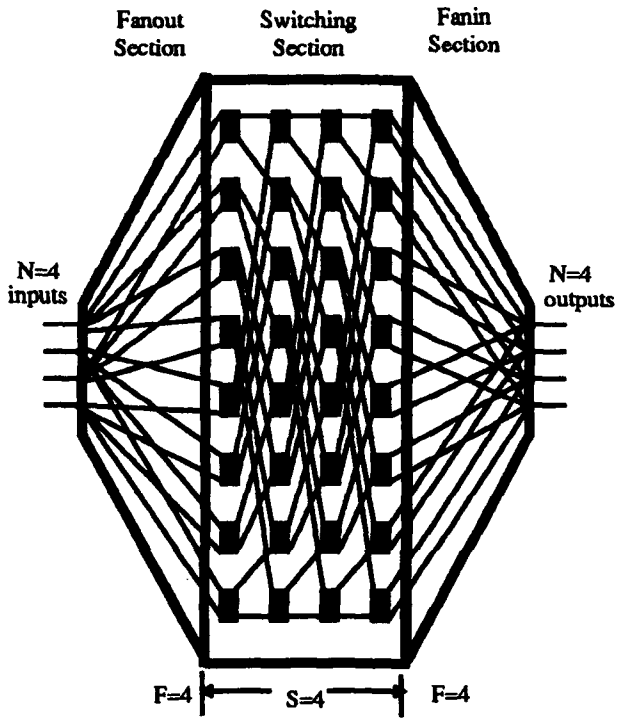


Figure 1. 3 sections of N-input, N-output EGS network.

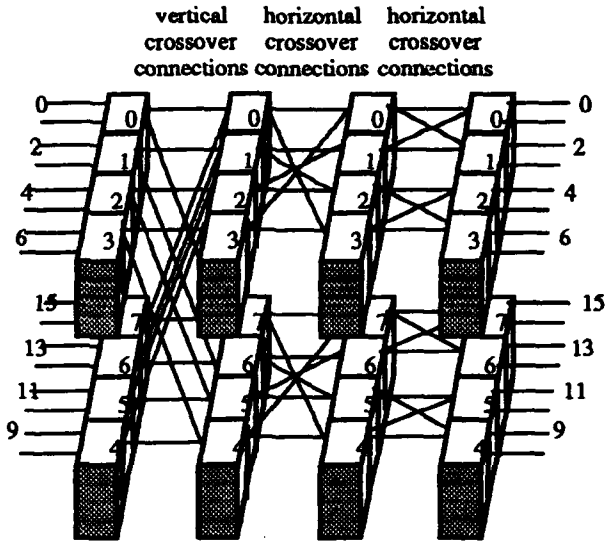


Figure 2. 3D implementation of EGS network.

the MIN. In addition, EGS networks do not require the nodes in the network to have any particular functionality, so acceptable EGS networks can be designed using nodes with n inputs and m outputs, where n and m can be any positive integers. The only requirement placed on EGS networks is that the link-stage connections be topologically equivalent to the connections in the perfect shuffle[4]. Thus, any of the proposed photonic interconnection schemes that provide connections between planar device arrays and are topologically equivalent to the perfect shuffle (such as the 3D crossover)[5] can be used to implement a photonic EGS network

We will limit our analysis to a small subset of the general EGS class of networks. This subset will have N-inputs, N-outputs, a fanout section, a switching section, and a fanin section (Fig. 1). We will also limit our analysis to 2-input, 2-output switching nodes. If the fanout of the network is F, then each input port is connected to F links entering the first stage in the switching section. If the fanin of the network is also F, then F links from the last stage of the switching section are connected to each output port. As a result, every node-stage in the switching section must contain NF/2 2-input, 2-output switching nodes. The switching section in the center of the network contains S node-stages. Thus, the triplet (N,F,S) can be used to uniquely specify the dimensionality of an EGS network having the topology shown in Fig.1. The particular EGS network in Fig. 1 is defined by (N,F,S)=(4,4,4). If the fanout and fanin sections are implemented using optical logic devices acting as binary splitters and binary combiners, respectively, then the total number of node-stages (T) required in an EGS network defined by (N,F,S) is $T = S + 2\log_2 F$. The size of the device arrays in EGS network implementations is primarily determined by the network fanout, because an EGS network defined by (N,F,S) will require a device array of size:

$$\sqrt{NF} - by - \frac{\sqrt{NF}}{2}$$

Thus, the (4,4,4) network in Fig. 1 would require 8 node-stages with NF/2=8 nodes per node-stage, and each device array would be of size 4-by-2, as illustrated in Fig. 2.

We have limited our analysis to 2-input, 2-output nodes. A 2-module is a new type of 2-input, 2-output node that was developed for use in photonic switching applications. A 2-module OR's the two inputs together and passes the results on to the two output ports only if the gate is enabled by a control signal. This control signal can be injected into the network using many different schemes[6]. However, because of its simplicity, a single 2-module can be implemented using a single S-SEED[3] if an electronically-controlled SLM is placed in the path of the clock signals (spot arrays) that are di-

rected at the S-SEED array, as was demonstrated in an experimental prototype.[5] The electronic processor controlling the SLM can permit only one of the two inputs entering a 2-module to be enabled (clocked in the previous node-stage), and the other input must be disabled (unclocked in the previous node-stage). Thus, the use of 2-modules adds new constraints to path hunt and routing algorithms for EGS networks.

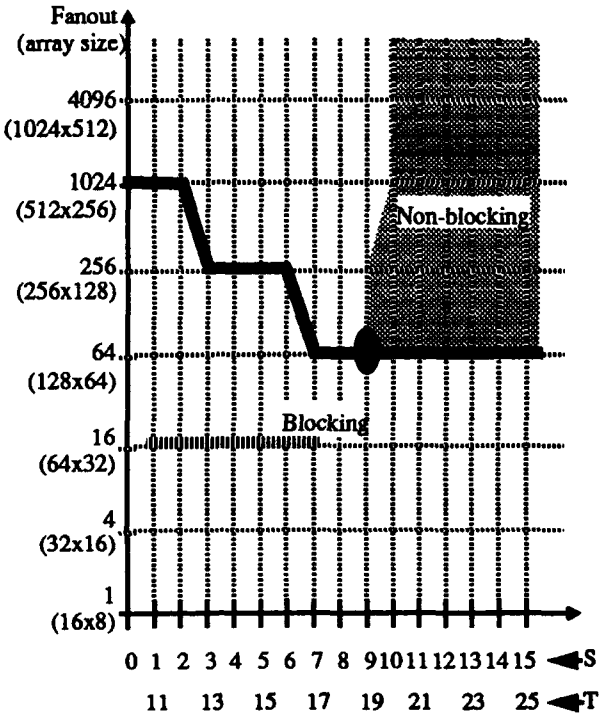


Figure 3. Required F vs. S (F vs. T in gray region) for N=256 non-blocking EGS network.

3. Operating characteristics of EGS networks

The EGS class of networks covers a broad range of networks that includes both strictly non-blocking networks and networks with finite blocking probabilities. They can also be used for point-to-point operations or multicast operations. Analytical models have been developed to characterize the performance of both blocking and non-blocking EGS networks, and the accuracy of these models has been tested and validated by computer simulations. These analytical models have shown that any N-input EGS network can be operated as a strictly non-blocking network if the fanout F and the number of stages S are increased beyond certain threshold levels. There are a large number of possible combinations of F and S that can produce strictly non-blocking operation, and these many combinations are shown by the solid black line in Fig. 3 for a network with N=256. (Note: The corresponding device array size is shown below each F value). This F vs. S plot indicates that for non-blocking operation, larger values of F will typically require smaller values of S, and smaller values of F will typically require larger values of S. Thus, EGS networks can capitalize on advances in optical fields of view and device array sizes, because these advances will permit larger values of F and smaller values of S. Fig. 3 also shows a F vs. T plot indicating the total number of node-stages required for strictly non-blocking operation (the gray region). The optimum operating point using current devices (which tend to have smaller sizes) is indicated by the black dot in Fig. 3, and it shows that a strictly non-blocking photonic EGS network with N=256 inputs will require 19 device arrays of size 128-by-64. The optimum operating points have been calculated for strictly non-blocking EGS networks of various sizes (N), and the results are shown in Table 1.

Table 1. Hardware requirements for non-blocking EGS networks.

# network inputs (N)	# logic gates per device array	# device arrays
16	8 x 16	10
32	16 x 32	13
64	32 x 64	15
128	32 x 64	18
256	64 x 128	19
512	64 x 128	23
1024	128 x 256	24
2048	256 x 512	26
4096	256 x 512	28

Although some switching applications require strictly non-blocking operation, many applications can tolerate small amounts of blocking within the network. The hardware costs of photonic EGS networks can be greatly reduced if the application can tolerate finite blocking probabilities, because F and S can typically be reduced from the values shown in Table 1 for strictly non-blocking operation. This effect was analyzed using computer simulations that monitor the blocking probability as S is varied in an EGS network with fixed N and F. The

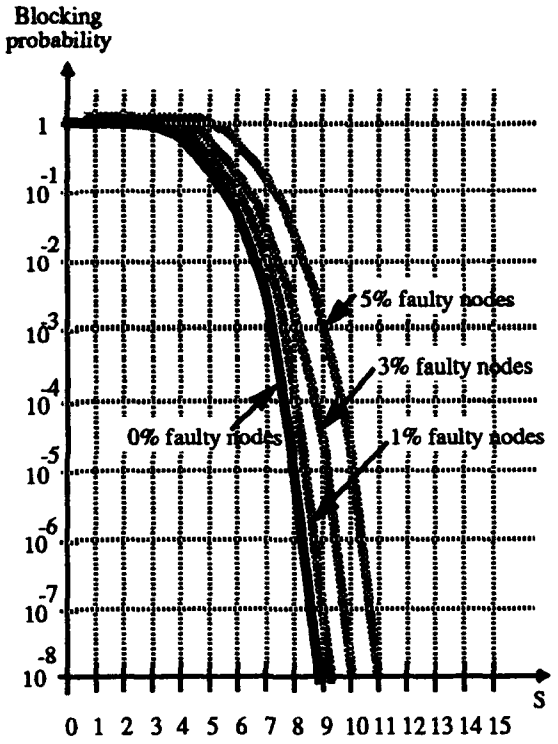


Figure 4. Blocking probability vs. S for *N=256, F=16 EGS network.*

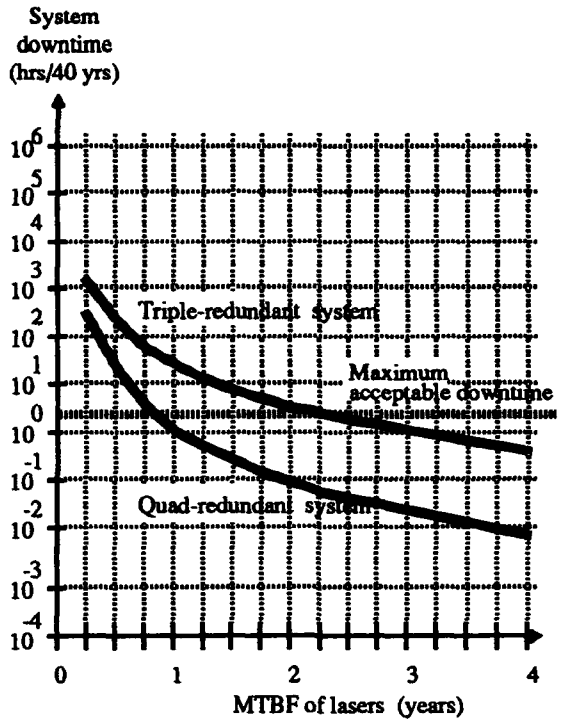


Figure 5. System downtime vs. MTBF of lasers in N=256 EGS network.

results for a network with N=256 and F=16 (shown by the dashed line in the blocking region of Fig. 3), are plotted by the solid dark line in Fig. 4, and the resulting blocking probabilities drop rapidly as S is increased. If a blocking probability of 10^{8} is acceptable, then an N=256 EGS network with S=9 and F=16 would be sufficient. Since this corresponds to a network with T=17 node-stages of size 64-by-32, the savings in hardware cost over the values in Table 1 should be evident.

The blocking probability simulations were also used to study the effects of faulty nodes on the operation of photonic EGS networks. The solid gray line plots in Fig. 4 show that the blocking probability will increase as faulty nodes are added to the switching section of the EGS network, but the increases are relatively small. As a result, a few extra stages can be added to the network during the design phase to permit the network to tolerate these faults and still maintain acceptable blocking probabilities. Catastrophic faults (such as laser failure) can still occur within the network, and the only solution to this problem is to add redundancy. The amount of required redundancy is related to the MTBF of the lasers. For an N=256, F=16, S=9 network, the system downtime was calculated as a function of the MTBF of the lasers, and Fig. 5 shows that triple- or quad-redundancy may be required to yield acceptable system downtimes (< 2 hrs. in 40 yrs.) for telecommunication applications.

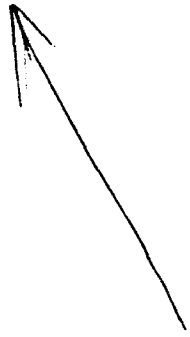
4. Conclusions

The EGS class of networks offers designers of photonic switching systems many degrees of freedom to customize the network to the developing technologies. In addition, its low hardware costs, low blocking probabilities, and high degrees of fault tolerance make it an ideal candidate for many photonic switching applications.

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S-SEED-Based Photonic Switching Network Demonstration

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Abstract

A prototype digital free-space photonic switching fabric has been demonstrated. It consists of three cascaded 16x8 arrays of Symmetric Self Electro-optic Effect Devices used as logic gates that implement part of a multistage interconnection network. We discuss the architecture, device tolerancing, optical system design, and optomechanical design. This optical circuit was successfully configured as a fully operational array of 32 independent 2x2 nodes and operated at 100kHz.

Introduction

Research in free-space photonics as a way of exploiting the large parallelism or spatial bandwidth of optics is a topic of current interest[1]. Up to this time, system experiments with Symmetric Self Electro-optic Effect Devices (S-SEEDs)[2] have demonstrated increasingly complex interconnection of arrays, using only the latching functionality of S-SEEDs, and up to 32 (4x8) S-SEEDs in each array[3,4]. The experiment described in this paper represents the first demonstration of array *logic* with S-SEEDs, and demonstrates the functionality required to implement multistage switching and computing systems[5]. The emphasis of this work is to investigate the constraints and limits of currently proposed techniques for implementing free-space digital optical logic systems. These limits set specific requirements on the optical and mechanical performance of the system.

The primary purpose of this paper is to present a detailed discussion of the major issues involved in implementing a free-space photonic interconnection network. An experimental test-bed was constructed for this investigation to identify and to gain insight into the critical practical issues which can affect system performance. These issues include the accumulation of signal level non-uniformity and its effect on device performance, optical and opto-mechanical complexity trade-offs, system modularity and reliability, and the development of analysis and alignment tools and techniques. The identification of these critical issues is necessary to make the architectural, device, optical, and optomechanical modifications required to bring this technology to fruition.

Architectural Issues

The fundamental goal in any switching architecture is to provide connectivity between input ports and output ports in a controlled fashion. Most architectures are multistage interconnection networks (MIN's) with stages of switching nodes (node-stages) connected by stages of links (link-stages), as in Figure 1.

The routing of the data occurs in the switching nodes, and the routed data is passed from one stage to the next stage via the connecting links. Switching networks typically consist of several types of sub-units that perform different functions necessary to the overall system operation. Sub-units include the controller, the line interface, and the switching fabric. Due to the high degrees of specialized processing required in the controller and the line interface, these functional sub-units are more easily implemented via all-electronic implementations. The operation of the switching fabric may be able to capitalize on the features of free-space optics, because it requires a large number of relatively simple interconnections.

Two basic components within any switching fabric are the nodes

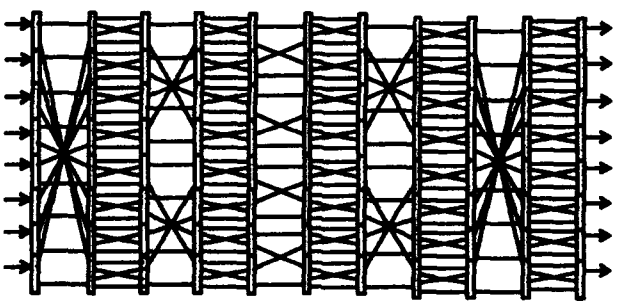


Figure 1. A Multistage Interconnection Network.

and the interconnections. The simple node shown in Figure 2 has two inlets and one outlet, so it is called a 2x1 node.

It is comprised of two AND gates and one OR gate logically connected to form a multiplexer circuit. If the AND gates are placed on one device array and the OR gate is placed on another device array, then the combination of the AND gate array, the optical interconnections, and the OR gate array creates a node-stage that can be used in a MIN. The node also requires two enable signals to be directed at the input AND gates. These enable signals determine which of the two inputs will be routed through to the output of the 2x1 node. Two 2x1 nodes (appropriately connected) can be used to implement a 2x2 node[5].

The connections within the node and link-stages implement the crossover interconnection. This is topologically equivalent to the shuffle interconnection which has been shown to be useful for many communication and computing applications.

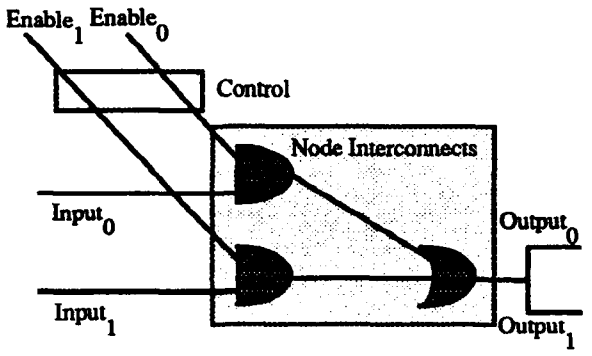


Figure 2. Schematic of a 2x1 node.

In addition, the crossover interconnections can be implemented in optics using relatively simple, low-loss optical hardware[6]. For a fabric with N 2x1 nodes in each node-stage and crossover interconnections, full-connectivity between the input ports and output ports is achieved in the fabric with only log2(N)+1 nodes.

An experimental test-bed was designed which would demonstrate (1) the functionality of the link-stage connections, (2) the functionality of node-stage connections, (3) the parallel operation of several 2x1 switching nodes, and (4) the operation of a working input interface into the network. The hardware shown in Fig. 3 is only a portion of a crossover switching network, so it does not permit full-connectivity between all of the input ports and output ports. The devices used were three S-SEED arrays with 128 S-SEEDs in each array arranged in eight rows and sixteen columns of devices as shown in Figure 4.

The devices in the second stage are operated as logical AND gates, while the devices in the third stages are operated as logical OR gates. The AND gates in the second stage are optically connected to the OR gates in the third stage to create an 8x8 array of 2x1 switching nodes.

The devices in the first stage of the experimental test-bed are operated as OR gates (similar to the devices in the third stage). The first device array provides an input interface for the experimental test-bed, because it receives input signals that are launched into the network on optical fibers. Each of these input fibers can carry binary-encoded information from a different source, and the information from many fibers can be simultaneously routed through the network. To correctly image the output from a group of fibers onto the first device array, the fibers are tied together to form an input fiber matrix. At the OR gate, the format of the data is converted from the single-rail format used in the fiber matrix to the dual-rail (or

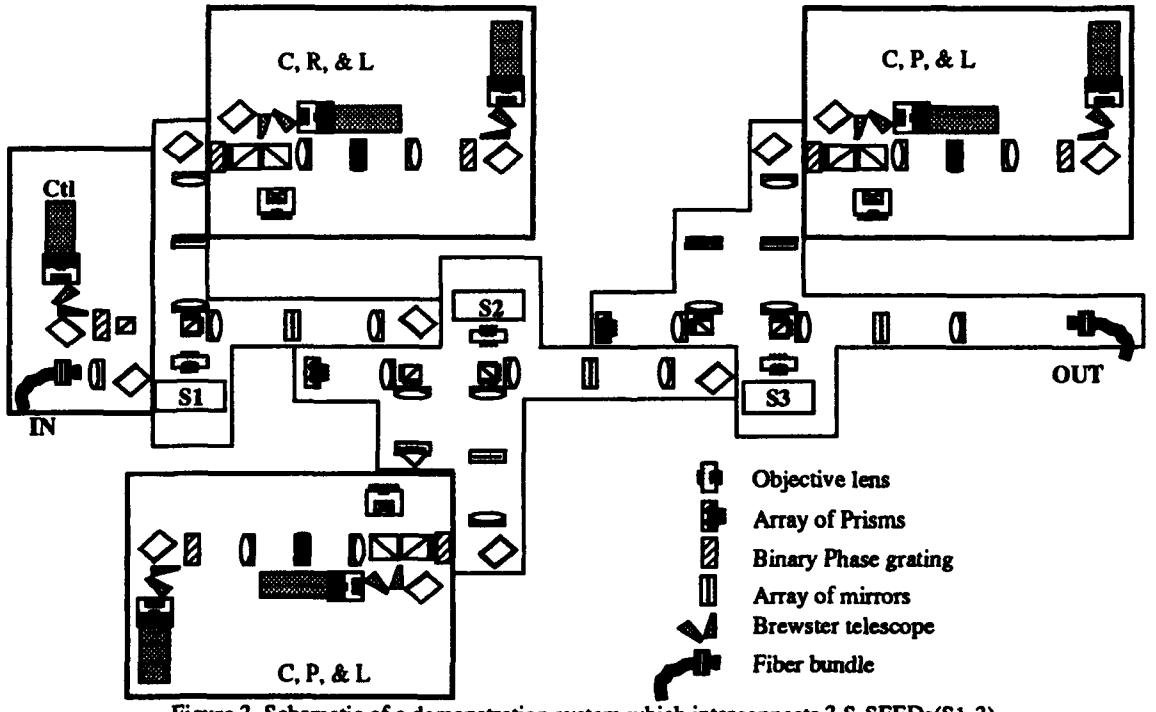


Figure 3. Schematic of a demonstration system which interconnects 3 S-SEEDs(S1-3).

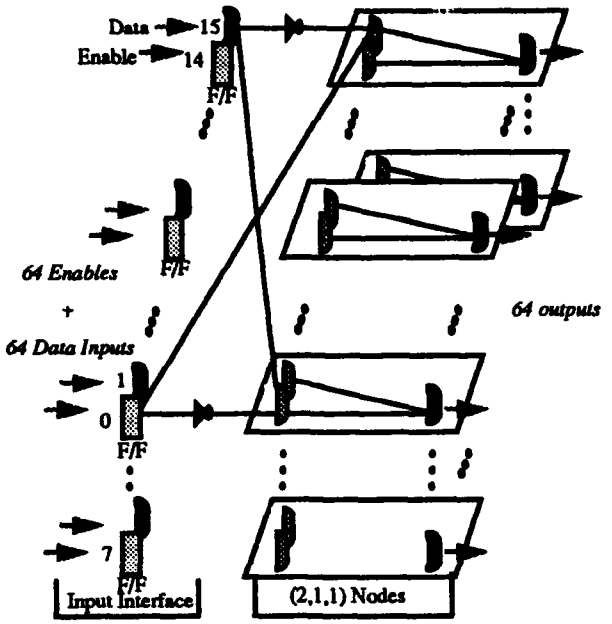


Figure 4. Schematic of the demonstration system showing 3 stages of S-SEEDs interconnected using crossovers.

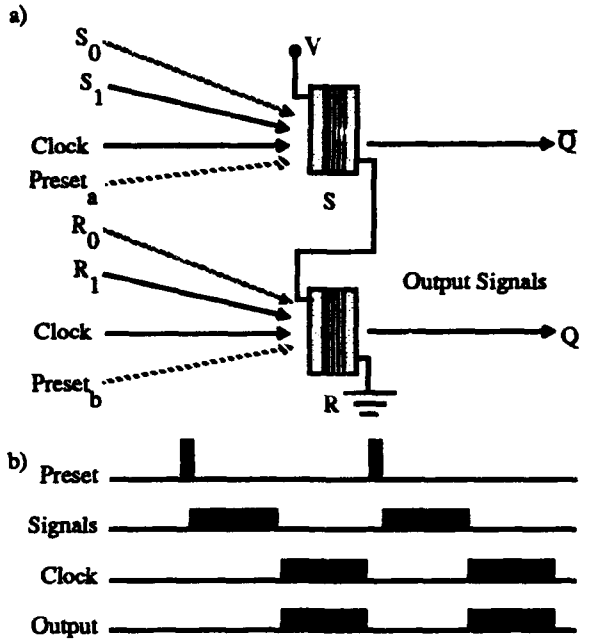


Figure 5. a) Inputs, outputs and b) timing sequence required for S-SEEDs.

differential) format used by the S-SEED logic gates. This single-rail to dual-rail conversion requires that each of the OR gates in the first array be preset to the logic "0" state before the single-rail data arrives. The state of the devices in the first array are subsequently read out and transmitted to the devices in the second array.

The unused devices in the first array were used as flip-flops (in Fig. 4-F/F) to store the control bits that ultimately enable the desired AND gates in the second stage. We were able to use the flip-flops in the first stage to simulate the functionality of a SLM for the second stage. Thus, various control signals can be directed at the 64 2x1 switching nodes to test their functionality within the experimental test-bed.

Symmetric SEED Functionality

The S-SEED is essentially an optical set-reset latch, which can be made to simulate a logic gate[7]. A latch has a single signal input, whereas a gate has at least two signal inputs, with their levels determining whether the gate will switch. The S-SEED is a differential device, each input and output is composed of two beams, as shown in Figure 5(a). The ratio of the powers in these beams determines the logic state it represents. The S-SEED does not emit light therefore a set of two bias or clock beams are required in addition to the input data beams (signal beams). In operation, first the signal beams set the state of the device, and subsequently, the clock reads the state (Figure 5(b)). The device has gain if the signal beams are not present simultaneously with the clock beams, and if the clock beams have higher power. This is referred to as time sequential gain. The output from a S-SEED is thus 2 beams which are reflected from both the R window (Q) and S window ($\overline{Q}$), as in Figure 5(a).

The state of the output is the ratio of the power in the Q beam to the power in the $\overline{Q}$ beam. It is important therefore that the two read beams are equal in power before reflection. The operation of a S-SEED is determined by the form of the bistable power transfer characteristic. The ratio of the signal powers is defined as the input contrast ratio. If the input contrast is increased from zero, the reflectivity of the S window switches from a low value, R1, to a high value, R2, at an input contrast value equal approximately to the ratio of the absorbances of the 2 windows: T=(1-R1)/(1-R2). The reflectivity of the other window (R) switches from R2 to R1. The transition point (ideally) occurs at an input contrast of 1/T=(1-R2)/(1-R1) when the input contrast is reduced from a high value. The ratio, R2/R1, of the 2 reflectivities is the output contrast.

The output contrast can be as high as 6 in these devices[2]. The measured contrast in this experiment was only 3.2+/-0.1. The drop in performance from the optimum could be explained by the use of a laser wavelength not matched exactly to the ideal detuning from the exciton absorption feature of the S-SEED. Of the total power incident on the S-SEED objective lens, only 31% is reflected regardless of which state the device is in, since half of the power is strongly reflected and half weakly reflected. The output contrast and the total output power (taking into account other measured losses) were used to calculate the reflectivities of the two states: R1=50% and R2=15%. Measurements of the bistable transition point indicate that T=1.4+/-0.2 (the difference from the calculated input contrast of T=1.7 is probably due to photocarrier surface recombination).

Consider a S-SEED used to implement a two input logic gate. The logic state represented by the input is determined by to the ratio of the powers in the S beams to the powers in the R beams. This input requires two sets of beam-pairs. The (0,1) and (1,0) signal inputs produce an input contrast of unity which is within the bistable region. With this input the device will retain the state it was in before the signals were incident.

A preset beam is used to remove any possible ambiguity. Before

the signal beams are incident, the preset beam is incident on only one window (Figure 5(a)). For example, if the preset beam is incident on the S window (preset$_s$ in Figure 5(a)), the output state is high reflectivity for the beam incident on the R window (Q) and lower reflectivity for the S window ($\overline{Q}$). Thus, an input contrast with a value above 1/T maintains the gate in the same state to which it has been preset. The device thus simulates an OR gate. The output (Q/$\overline{Q}$) is high for any input apart from (0,0) which is the only possible input with an input contrast less than 1/T. If an AND is required, the preset is incident on the R window.

A difference in attenuation of each of the two beams which constitute a differential pair is defined as local non-uniformity. Variation in power levels of each of these differential pairs across the array is defined as global non-uniformity. We wish to find the maximum allowed fractional variation ($\Delta P(g)/P$) above and below the average power (P) for correct operation of the device as any two-input logic gate. This will occur when one of the signal pairs has input powers equal to $P+\Delta P$ and $(P+\Delta P)/C$ incident on the S and R windows and simultaneously the other signal has powers of $P-\Delta P$ and $(P-\Delta P)/C$ incident on the R and S windows. In these circumstances $\Delta P/P$ is given by;
$\Delta P(g)/P=(T-1)(C+1)/[(T+1)(C-1)]$. Therefore, if there is no local non-uniformity, $\Delta P(g)/P=+/-32\%$(for this and all calculations that follow it is assumed that C=3.2 and T=1.4).

If the local variation in the individual powers of each beam is as severe as the global variation, the maximum fractional variation ($\Delta P(g,l)/P$) that is allowed, provided that C>T, is reduced to; $\Delta P(g,l)=(T-1)/(T+1)$. In this circumstance, the maximum local and global non-uniformity allowed is reduced from +/- 32% to +/-17%.

The introduction of an attenuator($\alpha<1$) into the path of the $\overline{Q}$ beams will cause a shift in the input contrast; the ratio of the input powers in the ideal (0,1) and (0,0) inputs will be increased by $1/\alpha$ making the former more tolerant to non-uniformity whereas the latter will be less tolerant[8]. This attenuation can be achieved using different reflectivity mirrors for the Q and $\overline{Q}$ beams before they are incident on the S-SEED.

When the local non-uniformity is zero, the optimum attenuation is T/C. This leads to a large increase in $\Delta P(g)$ which is possible because the input contrast ratio is no longer dependent on the global non-uniformity. In this case, $\Delta P(g)$ is limited by the precision with which the local non-uniformity can be maintained, the uniformity of the device (variation in T), and the precision to which it is possible to introduce the attenuation. For example, the optimum α for our system in this circumstance is 0.44. An effective attenuation of 0.56 is provided when gold and chrome are chosen as the mirrors for the Q and $\overline{Q}$ beams respectively. The use of this non-optimum attenuation would reduce $\Delta P(g)/P$ from being unlimited to +/-82%. This is equivalent to a factor of 10 between the highest power and lowest power beams in the array (1+0.82)/(1-0.82).

If the local non-uniformity is equal to the global non-uniformity, the optimum α is $(T/C)^{1/2}$. In these circumstances, the maximum allowed variation in the uniformity of each beam in the array is given by $\Delta P(g,l,\alpha)/P=(C^{1/2}-1)/(C^{1/2}+1)$. In our case, $\alpha=0.8$ is ideal. With this attenuation, $\Delta P(g,l,\alpha)/P$ is increased from +/-17% to +/-28%.

Experimental System Description

System Hardware Overview. To implement a multistage switching network using S-SEEDs, optical hardware must perform the following functions:

Input Interface: a 2-dimensional array of input data streams must be generated on the same pitch as the S-SEED arrays.

Control: an array of control signals must be generated to determine the input selected at each of the 64 2x1 switching nodes.

Beam Array Combination: four beam arrays (2 signal arrays, 1 power/clock array and 1 control array) must be combined and imaged onto the S-SEED array, and then the reflected clock output array must be relayed to the next S-SEED array. This function is responsible for much of the complexity in the optical hardware.

Power Supply (Clock) and Preset Generation: the array of uniform intensity beams used as the power supply/clock must be generated. To set the logical functionality of each S-SEED, an array of Preset beams may also be required.

Interconnection: a crossover interconnection operation must be performed on the data array from the previous stage. This includes a fanout of 2 and a spatial "folding" of the data array image.

Alignment: this includes the provision of incoherent illumination (to avoid Talbot image effects), view ports to visually inspect the alignment, and enough degrees of freedom (fold mirrors, positioners, etc.) to align the multiple spot arrays.

The hardware required for this experiment was constructed as a series of three optical hardware modules (OHMs), using commercially available optics and a custom designed opto-mechanical mounting system. The first OHM (with S-SEED array S1 in Fig. 3) provides the input interface function and stores control information for the array of 2x1 nodes formed by the next two S-SEED arrays. The last two OHMs (with S-SEED arrays S2 and S3 in Fig. 3) are mirror images of each other (vertically) and each contains hardware for beam combination, power/preset, interconnection and alignment. These last two OHMs have slightly different interconnection optics, so that the second OHM implements one link stage of the crossover network interconnection, while the third OHM implements the connections required for the 2x1 switch nodes shown in Fig. 4. The outputs of the third S-SEED array are then imaged onto a camera or onto an output fiber bundle array.

The input OHM provides 128 inputs to the system in the form of 64 data streams and 64 simulated control inputs. The data streams are generated by a square matrix of 64 multimode fibers driven by LEDs. The control inputs are generated by a beam passing through an 8x8 binary phase grating (BPG), which generates an 8x8 array of collimated beams. Identical control signals are thus delivered to all of the nodes in this experiment. These inputs are combined by a polarizing beam splitter (PBS), and then enter the beam combination optics. The fiber bundle output spot array undergoes a 10x demagnification along the path to the S-SEED array.

The beam combination optics use space multiplexing[9,10] to spatially interlace these input beams with the power, preset, and output beams. The control and fiber input arrays are split by the beam splitter adjacent to the S-SEED labeled S1 in Fig. 3, and are reflected from an array of mirrors patterned on a transparent

substrate in the 2 image planes. After reflection, the input arrays are recombined by the PBS and imaged onto the S-SEED array. This S-SEED array makes use of the preset beams to convert the single ended fiber and control inputs to differential signals. In this case, low power preset beams are incident on one diode of each S-SEED during the switching cycle. Each S-SEED is thus switched to the differential "zero" state in the absence of a light pulse from the input fiber or control array, and to a differential "one" when a light pulse of greater intensity than the preset is present. When the states of these S-SEEDs are read out by the clock beams, the single-rail system inputs are thus converted to differential output signals to be cascaded into the next OHM.

To read out these states, the clock laser beam is split 256 times to form the 128 spot pairs needed for the 16x8 array of devices. The computer designed BPGs[11,12] were placed at a pupil of the optical system (in object, or "collimated-beam" space) to generate the clock spot array for each S-SEED array. To generate the equal intensity spot pairs needed by the S-SEEDs, multiple imaging[13] with 2 BPGs was used. A 1x2 BPG produced 2 spots of identical intensity, in addition to low intensity higher orders. These higher orders were blocked by a spatial filter, and the spot pair was multiply imaged 128 times by a second BPG. Generation of the 256 clock beams in this manner ensures that the intensities of the two beams in each clock beam pair are identical, and that they remain so even in the presence of laser noise or power fluctuations. This helps reduce the signal beam local non-uniformity discussed above. The preset beams are combined with the clock beams just before the second BPG, and thus only one preset spot per S-SEED is generated. The clock spot pairs are reflected from the S-SEEDs, and are transmitted through the transparent portions of the patterned mirrors.

This output signal array is then permuted to implement the crossover interconnection[6]. This permutation is accomplished with a beam splitter to fan out the signal by two, followed by imaging operations on the two copies. The copies are either spatially "folded" by the prism or retroreflector array, or directly re-imaged via a plane mirror. The permuted copies are recombined by the beam splitter and propagate into the beam combination optics.

The digital regeneration at each stage restores the amplitude, synchronization, and beam quality of the signals transmitted to the next stage. Assuming that the outputs of one S-SEED array can be successfully interconnected to the next S-SEED array, these OHMs can, in principle, be cascaded indefinitely to create a multistage interconnection network. The regeneration at each OHM significantly lessens the problems of crosstalk, signal skew, and overall system size limitations for high speed operation.

Optical System Overview. The digital regeneration performed on the signals at each S-SEED array allows us to determine the total system performance by modeling and optimizing the path through one and a half OHMs. Specifically, we model the path from the clock laser in one OHM to the S-SEED array in that OHM, then through the interconnection and beam combination sections of the next OHM to the next S-SEED array. This modeling is especially useful because all of the OHMs following the input interface OHM are identical, except for changes in the periods of the interconnection retro-reflector arrays. The optical system for one OHM can be divided into optical power supply, interconnection, and beam combination sections. All three of these sections contain intermediate image planes, and telecentric image spaces. All of the lenses in the OHM are operated at infinite conjugates.

The optical power supply collimates and circularizes the clock and preset laser beams, and generates the required arrays of beams. The power supply optical path is from the laser and Brewster telescope, through the 1x2 BPG, and then through the spatial filter relay. Two lens types are used in the optical power supply: 5mm focal length laser collimating lenses and 40mm focal length achromatic doublet lenses to image the spots from the 1x2 BPG onto and off the spatial filter. A single stripe (index-guided) AlGaAs laser was used which had both a single longitudinal and transverse mode at 850nm. The astigmatism of the laser was specified as less than 2μm. A Brewster telescope was used to circularize the beam. The single clock beam is split by the 1x2 BPG and the pupil defined by this BPG is imaged by the spatial filter relay lenses to the 16x8 BPG. The output of the optical power supply is the array of 256 collimated clock beams, and 128 collimated preset beams at the pupil defined by the 16x8 BPG.

The interconnection and beam combination sections use two types of lenses: 42mm focal length relay lenses and 7.79mm focal length objective lenses. The relay lenses image the spot arrays onto and off the patterned mirrors and retroreflector arrays, and the objective lenses image the spot arrays onto and off the S-SEED arrays. The optics in these sections operate over a +/-1.56 degree field of view. Along the path from the 16x8 BPG to the second S-SEED, six spot image planes are formed. Each afocal relay transfers the array of collimated beams formed by the 16x8 BPG to the entrance pupil of the next relay. The patterned mirrors, S-SEED arrays and retro-reflectors arrays all lie in conjugate image planes. In these planes, the power supply and signals are arrays of focussed spots. The imaging between the patterned mirrors and S-SEED arrays has a magnification of 5.4:1 or 1:5.4 (42/7.79). This allows the relay lenses to operate at a higher f-number, facilitating aberration control as well as system alignment and stability. Along the path from the BPG to the second S-SEED array, the image passes through 11 lenses, and a total of 132 surfaces (including beam splitters, etc.). Eight of the lens-passes are through the 42mm relay lenses, and 3 of the passes are through the 7.79mm objective lens.

The device switching energy is proportional to its area. Thus a small device is necessary to maximize system speed. The small size (5μm width) of the S-SEED windows requires a well corrected optical system. The aberration contributions of each of the 11 lenses must be small and/or "balance" the contributions of other lenses. The goal of the optical system design was to have a "diffraction limited" wavefront (Strehl ratio greater the 0.8) at the second S-SEED.

Two factors in this design help to minimize the total aberration accumulation: system symmetry, and the relatively slow speed (high f-number) of the relay lenses. The symmetry of this optical design allowed distortion and coma to be corrected at each relay pair. The aberration total then consists of spherical aberration, astigmatism, and field curvature contributions. To limit the accumulation of these aberrations, the relay lenses used were of the symmetric (Plossl) eyepiece form. These lenses were constructed from pairs of commercial achromatic doublets. The

42mm focal length relay lenses were illuminated by beams with a 99% intensity diameter of about 6mm. Since the e^{-2} diameter of the Gaussian beam is only about 2/3 of the 99% diameter, the "effective f-number" (beam diameter/focal length) is greater than for uniform illumination. The relatively high "effective f-number" operation of the relay lenses resulted in only small contributions from these lenses.

The S-SEED objective lens is of particular interest, since its characteristics drive much of the rest of the system design. The primary characteristic of interest is the f-number of this objective lens, because of the flat field, (f)sinΘ distortion (to match the sinΘ BPG diffraction), and extremely low aberration performance required. The required f-number of this lens is surprisingly low, since the transmission of a Gaussian beam with little (< 1%) truncation represents an effective "stopping down" (decrease in the aperture size) of the lens. This results in an increase in the "effective f-number" at which the lens is being used, and thus an increase in the spot size. The largest f-number lens which enables a 99% coupling solution is a ~f/1.7 lens. This solution also requires that the lens diameter is about 1.7 times the beam waist diameter. The e^{-2} waist spot diameter is then 3.3μm.

The optical design of the modular optical hardware was analyzed and optimized by modeling with CODEV optical design software. Raytracing shows that while the individual elements are all well corrected, significant aberration does accumulate over the total path. The system performance is limited primarily by the accumulation of a quarter wave of spherical aberration. The system distortion is only about 0.1% due to the system symmetry, and this results in a 0.3 μm shift of the position of the outermost spot in the array. The field curvature and astigmatism present in this system increase the system's sensitivity to defocus.

The quality of the optical components and the beams used to connect the devices was assessed using a combination of focal plane image evaluation ("star test), interferometry, and scanning slits and pinholes. The star test and scanned slits and pinholes were used to measure the spot size and intensity profile of the beam at various points in the path, and at various field angles. In addition, through-focus beam-scans were performed to measure the depth of focus. These measurements indicate the precision to which it is necessary to align the components to couple a given percentage of the spot's energy into the 5μm S-SEED windows.

The optical quality of the power supply was a major limitation to the total system performance. Diffraction effects at the collimating lens and the difficulty in centering the laser chip in the center of the small field of the collimating lens result in degradation of the optical quality of the source. This was quantified by measuring the spot size when the collimated beam is focussed with a well-corrected 200mm focal length lens. Only 93% of the power in the collimated beam fell within a 200μm area. The size of the Gaussian waist was measured to be 1.3 times the size of the diffraction limited spot.

The optical quality of the beams after 8 relay lenses and 3 objective lens passes has a major effect on the energy coupled into the S-SEED. To examine the wavefront after such a long train of elements, a self-referencing interferometer was necessary. A modified point diffraction interferometer was constructed and used to assess the wavefront quality of the beam. It was found that the on-axis beam had accumulated about 3/4 wave (peak-to-valley) of positive spherical aberration (~ 3 times the Rayleigh criterion for a "diffraction limited" system). The presence of this aberration was confirmed by measuring the through focus spot size with a scanning pinhole. It was found that only 60% of the power incident on the S-SEED was contained within the central 5μm diameter. This 40% loss is due to the accumulation of optical aberration. The loss did not vary significantly across the 1.56 degree field. With the star test, we noticed the presence of a small amount of astigmatism at 1.56 degrees. The sagittal and tangential foci were separated by up to a few microns at the edge of the field. Figure 6 shows measurements of the through focus spot shape and size taken with a scanning 2μm slit, for both the on-axis spot (Figure 6(a)), and an off-axis spot at 1.56 degrees (Figure 6(b)). Measurements were taken at -10, 0, +10, and +20μm around the plane of best axial focus. These plots show the system sensitivity to defocus, and even the best focus spot size is clearly larger than is appropriate for highly efficient coupling into a 5μm S-SEED.

Mechanical System Overview. The design of the opto-mechanical system was determined by the precision and stability required to maintain the arrays of focussed spots in registration with the arrays of S-SEEDs. Each S-SEED in the three arrays has three pairs of beams (clock and two signals) and a single preset beam incident upon it. On each 5μm by 10μm window, the preset and clock beams are adjacent to the two cross-polarized signal beams. Reliable, error-free operation of

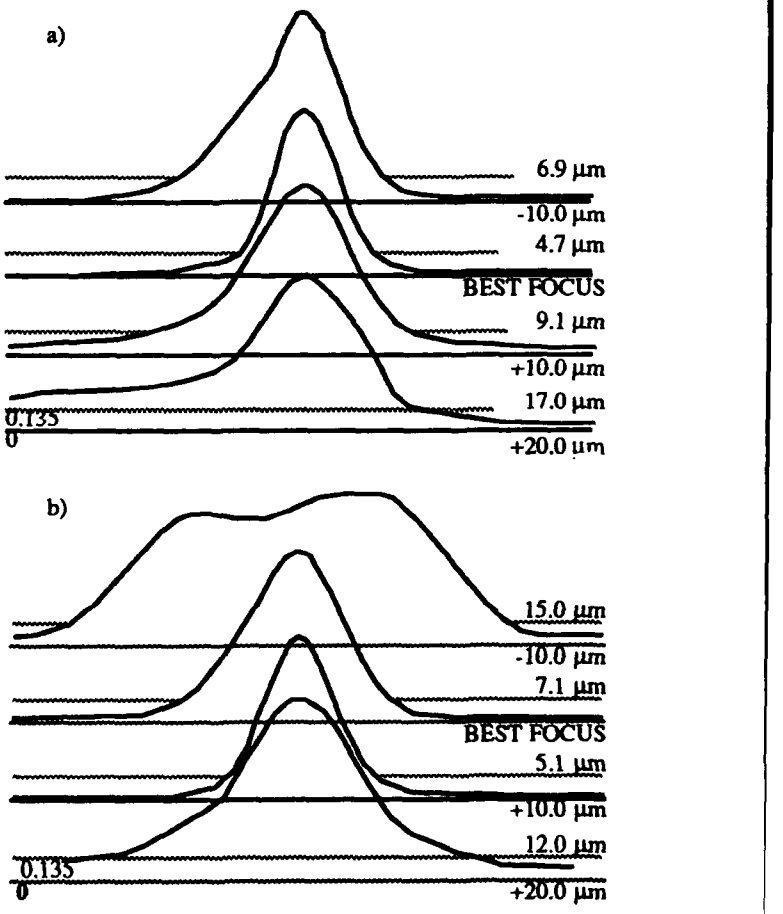


Figure 6. a) On-axis and b) Off-axis through-focus spot scans.

the entire system was only obtained if the alignment of every clock, preset, and signal spot was aligned to within 0.5 μm of the ideal lateral position on the 5 μm wide window and to within 5μm along the optical axis. This lateral tolerance translates in the object space (array of collimated beams) to an angular tolerance of 13 arc seconds. This precision requires that the correct angular orientation about the optical axis (roll) be set to 8 arc minutes.

The optical components of each OHM were mounted in v-grooves milled into jig-plate aluminum. Each stage requires only three v-grooves milled into the plate to mount seven lenses, two patterned mirrors and two retroreflectors. In addition to minimizing the number of mechanical components, the use of a plate with milled v-grooves also ensures that there is a well-defined mechanical axis. The optical and mechanical axes within each stage and between stages are made colinear to a precision of less than one arc minute using fold mirrors. The lenses were centered to less than one arc minute. The v-groove mounting technique ensures that this centration was maintained when the lenses are mounted in the system. Focus is obtained by simply sliding the lens along the v-groove.

The adoption of a v-plate to mount the components has been entirely successful. It minimizes cost by greatly reducing the number of mounts required by providing rotation and defocus adjustment and ensuring minimum tilts. In addition to forming a stable base for the components, it allows the system to be constructed in a much smaller area than would otherwise be possible.

Discussion and Conclusion

To examine the test-bed functionality, two experiments were performed. Cascaded arrays of latches were demonstrated, followed by cascaded operation as logic gates with preset beams and asymmetric attenuators. Low speed operation was verified by using a clock rate of a few Hertz and visually examining a magnified image of the output of the third S-SEED array, detected by a CCD array camera system. High speed operation was verified by imaging the third array's outputs onto detectors. Alignment was achieved by visually inspecting each intermediate image plane (with a CCD camera system), and also by maximizing the total photocurrent generated in each S-SEED array for each array of beams.

To demonstrate cascaded latching, the three stages were cascaded with each of the two interconnect paths between stages 1 and 2 and between stages 2 and 3 blocked (four permutations). The input fiber matrix and control laser were used to set the devices of the first array into known states. The successful transfer of those states into the second and third arrays via the four different paths confirmed that the devices could be operated as latches, and verified the continuity of all of the interconnection paths. Despite the fact that no athermalization of the optomechanics was attempted, errors only occurred when the temperature of the system was varied by +6/-7^{0}F about 72^{0}F room temperature. The stability of the optomechanics was tested by operating the system successfully without a shock absorbing table for several days.

The experiment was modified to incorporate gold mirrors for the Q beams and chromium mirrors for the $\overline{Q}$ beams in the patterned mirrors in an attempt to balance the sensitivities of the (0,0) and (1,0) inputs (α=0.56). The calculated tolerance to local non-uniformity was +/-12% with α=0.56. The local non-uniformity tolerance is thus approximately equal to the measured local non-uniformity, to within the measurement error (approx. +/-5%). Simultaneously, the calculated tolerance to global non-uniformity was +/-62%. That is, the highest power beam could be greater than four times more powerful that the lowest power beam ({1+0.62}/{1-0.62}).

The full truth table (4 combinations of inputs) was input into every gate in the second and third arrays. All of the gates in each array worked for all possible inputs. The system operated correctly as an array of 32 independent 2x2 nodes. The optical control input could be switched electronically from logical low to high with the result that the two outputs of each of the 2x2 nodes were exchanged.

The output power from each fiber at the input to the switch was 46μW. Vignetting in the collection optics and decreased absorption due to the broadband (100nm) illumination (from the LED fiber drivers) resulted in an effective input power of 0.3μW, which limited the first stage switching speed to 100kHz (33kbps system data rate). Approximately 3mW of 850nm laser power was incident on the BPGs, resulting in about 1 mW within the 256 spots at each S-SEED array (4μW per clock beam), with losses mainly due to the BPGs and multiple small polarization leakages. The minimum signal power cascaded from one array to the next was about 150μW per array, (900nW and 300nW for the "high" and "low" states of each signal input to the next S-SEED array). The incident differential power was thus 600nW. The loss in the signal path was due to S-SEED absorption (70%), loss at the retro-reflector arrays implementing the crossover connections (50%), the patterned mirrors for the space multiplexed beam combination(50%), and misalignment, Fresnel, and polarization losses. The actual system speed of 100kHz is less than the maximum theoretical speed of 200kHz due to fiber input losses, asymmetric attenuator losses, and signal non-uniformity effects.

In this experiment, individual logic gates are interconnected. While enabling the investigation of many critical system issues and allowing a great deal of architectural and opto-mechanical flexibility, a higher level of pixel integration ("granularity") may provide an advantage. The introduction of appropriate additional functionality[14,15] at each pixel may significantly lower the optical system power requirements, the opto-mechanical complexity, and the overall system size. However, decisions concerning the integration of amplification, combinatorial or sequential logic, and memory must be based on the total system tolerancing, since small changes in device characteristics may have dramatic and widespread system effects.

In conclusion, three 16x8 arrays of S-SEEDs have been operated as logic gates and interconnected to form a preliminary implementation of 3-dimensional small scale integration (384 gates). The logic performed implements part of a multistage switching network. Although its overall alignment and optical tolerances are quite constrained, we have demonstrated operation for over 6 days continuously in a laboratory, and for more than 3 days outside of the laboratory, before disassembling parts of the system to perform further testing.

The primary purpose of this demonstration system was to investigate the practical trade-offs required in free-space technology development. In keeping with this purpose, the

optical hardware modules developed for the original demonstration have also been used in subsequent experiments investigating the operation of larger device arrays. To accommodate these larger system experiments new optical designs are being tested, as well as new S-SEED device arrangements.

One supplementary experiment was the successful operation of a 128 (16x8) array of integrated S-SEED 2x1 nodes[16]. The operation of the array of 128 2x1 switching nodes on a single substrate represents the first time (to our knowledge) such a large array of higher functionality, or "smart," pixels has been demonstrated. Another later experiment demonstrated the interconnection of two 512 (32x16) S-SEED arrays. The cascading of two 512 S-SEED arrays doubles the size of the previously reported largest optical interconnection demonstration[17].

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Large Arrays of Symmetric Self-Electro-Optic Effect Devices

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Abstract

We demonstrate 8 × 16 arrays of electrically addressed and 64 × 128 arrays and 128 × 256 arrays of optically addressed Symmetric SEEDs and discuss the performance of these devices.

For optical processing to become a reality, large arrays of optical processing gates are required with low energies and fast switching speeds. Arrays of symmetric self electro-optic effect devices (S-SEEDs) with as many as 2048 devices (64 × 32) have been made using batch fabrication procedures that process an entire wafer of devices at once [1,2]. In this paper we describe the extension of that work to arrays with 8192 devices (128 × 64) and 32768 elements (256 × 128). We also demonstrate 8 × 16 arrays of symmetric SEED modulators [3] with individual electrical access to the devices. The performance and uniformity of the arrays are more than acceptable to continue systems experiments with these types of devices.

The S-SEED consists of two quantum well p-i-n diode modulators connected electrically in series with a power supply. Like all SEEDs, the S-SEED makes use of the change in absorption that occurs with a change in applied electric field across the quantum well regions of the diodes [4]. The S-SEED has the characteristics of a set-reset latch and can perform logic functions by using a preset beam [3]. The device has many desirable qualities for system experiments such as high (time sequential) gain, signal re-timing and logic level restoration, and operation over several decades in power levels due to the differential nature of the device. Like the earlier arrays of S-SEEDs, these devices were reflection mode devices [5]. The material was grown by molecular beam epitaxy (MBE) and contained 71 periods of 100Å quantum wells with 35Å $Al_{0.3}Ga_{0.7}As$ barriers. The p-i-n diode mesas were located on 20μm centers and had 5μm×10μm optical windows. The total array sizes were therefore $(2.56mm)^2$ and $(5.12mm)^2$ for the 8K and 32K arrays respectively. A photograph of the 8K array appears in Fig. 1, and of the 32K array in Fig. 2. A photograph of a section of the 32K array is shown in Fig. 3.

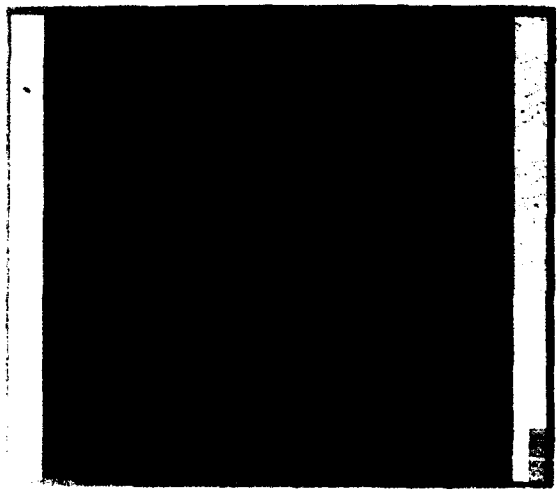


Figure 1. Photograph of an 8K (128 × 64) array of S-SEEDs.



Figure 2. Photograph of a 32K (256 × 128) array of S-SEEDs.

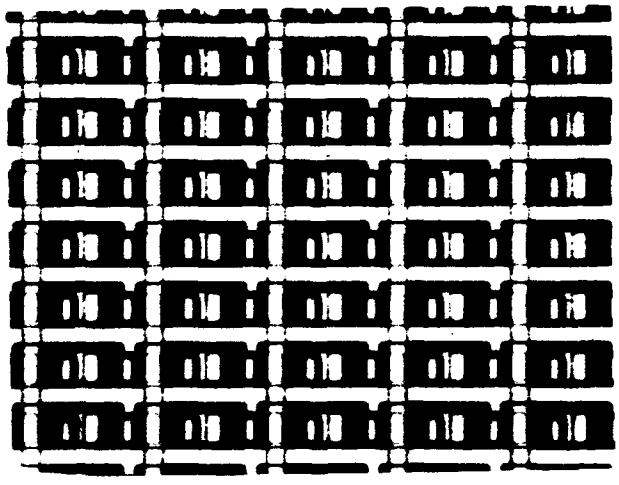


Figure 3. Photograph of part of the 32K (256 × 128) S-SEED array, which shows greater detail.

The 32K arrays were processed together with the (8 × 16) arrays of individually electrically addressed S-SEEDs (discussed later in this paper). These required interconnection metal cross-overs and thus two levels of interconnect metal. Instead of adding another insulation level and another metallization level to the processing sequence, we decided to use one of the ohmic metal levels, already in the processing sequence, for the second level of interconnects. We ran ohmic metal leads under the existing insulation level and directly over undoped semiconductor areas between devices. The soundness of this strategy was truly tested when this approach was also used (for the first time for arrays of optically addressed S-SEEDs) in the design of the 32K array. As can be seen in Fig. 3, a bias lead crosses a ground lead at every device.

Initially all of the fabricated arrays were forward biased so that the p-i-n diode modulators that make up the S-SEEDs luminesced. Over 50% of the 108 8K arrays and 32% of the 19 32K arrays that were made had uniform luminescence in over 99% of the devices within each array. All of these arrays also had reverse bias breakdown voltages greater than 40 volts for all devices in the array. One array of each type was packaged. Sample measurements on a small number of devices showed that better antireflection coatings as well as a slightly thicker quantum well region compared to our previous devices yielded improved contrast ratios of ~4:1 at 6 volts and ~7:1 at 15 volts with incident optical power below ~50μW. The operating range of the devices was measured by supplying equal power beams to the two diodes of the S-SEED and checking that the device could hold either state indefinitely. This operating range was from ~800nW limited by the leakage currents flowing in the diodes to ~500μW limited by saturation of the quantum well material. Switching energies have not yet been measured, but energies comparable to previous devices (1.5pJ at 10 volts) are expected.

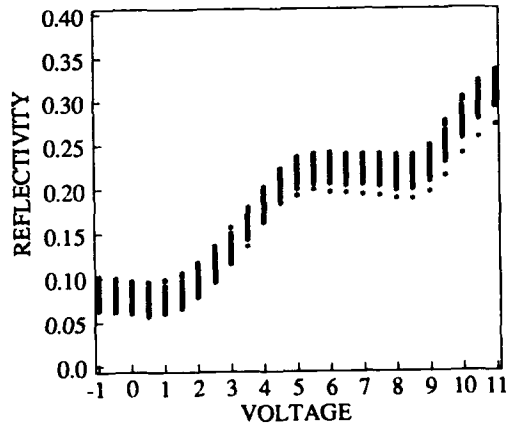


Figure 4. Reflectivity measurements for every 8th device in every 8th row of the 128 × 64 array of S-SEEDs.

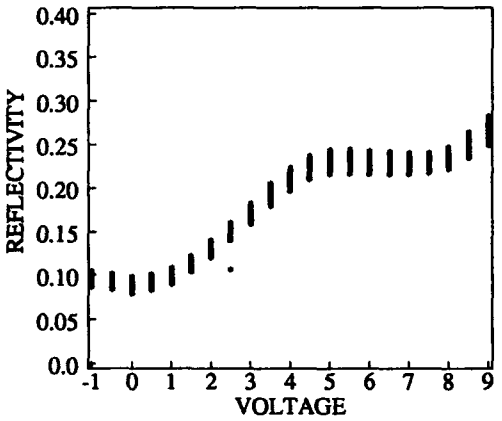


Figure 5. Reflectivity measurements for every 16th device in every 16th row of the 256 by 128 array of S-SEEDs.

The responsivity and reflectivity were measured on a sample of 128 devices uniformly spaced for each of the two different arrays, corresponding to every 8th or 16th device in every 8th or 16th row for the 8K and 32K arrays respectively. Figs. 4 & 5 show the reflectivity as a function of voltage for the 128 sample devices in each of the two arrays showing excellent uniformity across both arrays. The test was repeated for every device in the 128 × 64 array. Only 21 of the 8192 devices (0.25%) failed to have negative resistance required for bistability. Since the test required 20 hours to complete for the 8K array, every device in the 32K array was not measured.

A device can be made that modulates a pair of light beams in a complementary fashion by electrically modulating the node between two diodes of a symmetric SEED [3]. The quantum well diodes in the 8 × 16 array of electrically addressed S-SEEDs that we present here had 5μm × 5μm optical windows. The spacing between the two diodes of the S-SEEDs was 20μm and the spacings between S-SEEDs was 160μm and 80μm for the horizontal and vertical directions respectively. A photograph of the array is shown in Fig. 6. The spacings between S-SEEDs were increased in the electrically addressed devices to allow space for the electrical access leads. A photograph of an enlarged section of the array, showing greater detail, appears in Fig. 7. Also, the total chip area for the array of 128 electrically addressed devices was equal to the chip area for the 32,768 optically accessed devices because the chip needed to be large enough for the 132 (128 + 4 DC bias) bonding pads on the periphery of the chip. An array was packaged for testing.

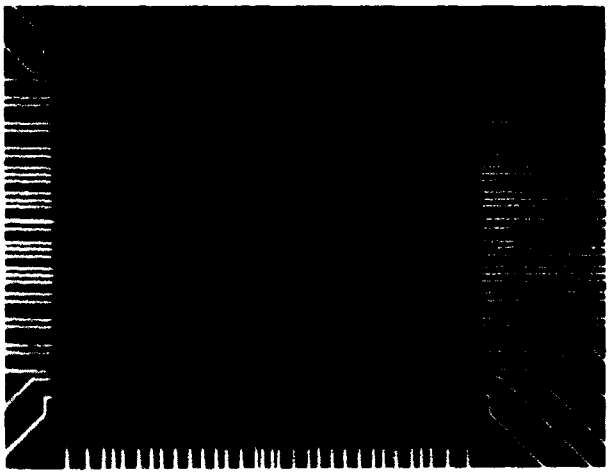


Figure 6. Photograph of the 8 × 16 array of electrically addressed S-SEEDs.

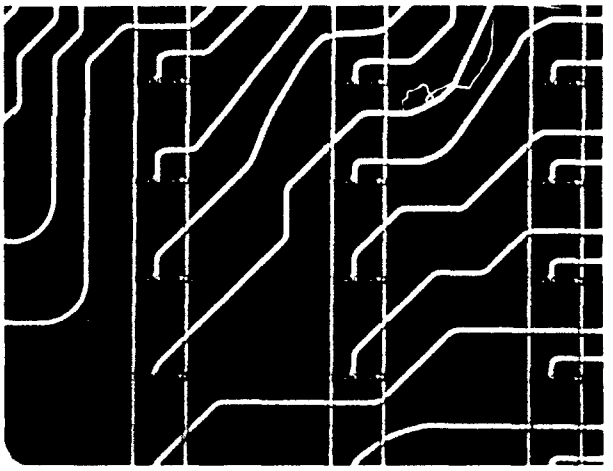


Figure 7. Photograph of part of the 8 × 16 array of electrically addressed S-SEEDs, which shows greater detail.

Reflectivity and responsivity were measured for these electrically addressed devices as well. All devices in the array worked correctly, as can be seen in Fig. 8, which shows the reflectivity as a function of voltage for each device in the array. The device array was actually mounted on a custom hybrid integrated circuit containing 128 50 ohm resistors, one for each input. We modulated one of the devices with a digital word generator and were able to obtain clean modulation beyond 1 Gb/s as shown in Fig. 9.

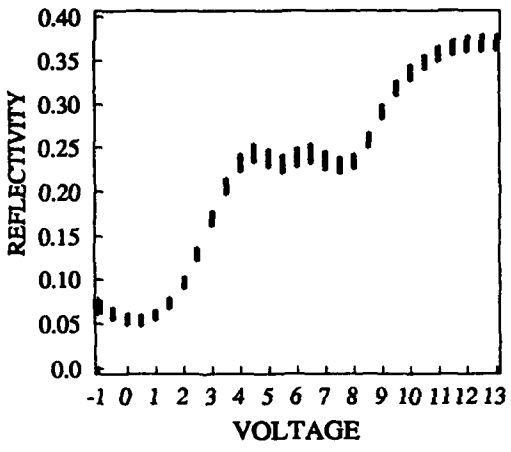


Figure 8. Reflectivity measurements for every device in the 8 × 16 array of electrically addressed S-SEEDs.



Figure 9. Modulation at 1 Gb/s of an electrically addressed S-SEED from the 8 × 16 array. Top trace is the data input, center trace is the uncomplemented optical output and the bottom trace is the complemented optical output. Horizontal scale is 1 ns/div.

In conclusión we have built and tested 128 × 64 and 256 × 128 arrays of symmetric self electro-optic effect devices. We also have built and tested 8 × 16 arrays of individually electrically addressed S-SEED differential quantum well modulators. This work further demonstrates that quantum well optoelectronic devices can indeed be made in large quantities. The performance and uniformity of the arrays is more than acceptable to continue systems experiments with large numbers of optical devices.

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Integrated SEED Photonic Switching Nodes, Multiplexers, Demultiplexers, and Shift Registers

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Abstract

We describe both a 4 x 4 array of integrated SEED based 2 by 1 photonic switching nodes and a 32 x 16 array of optoelectronically connected S-SEEDs that can be optically configured as an array of 2 x 1 switching nodes, multiplexers, demultiplexers and shift registers.

Introduction

The division between optical processing and electronic processing with optical interconnections can be a fuzzy one at best. Because of the limited functionality achievable in "all-optical" logic gates, a growing interest is seen in "optical" processing elements made using optoelectronic devices with greater functionality [1]. Large scale integrated optoelectronic chips of quantum well self electro-optic effect devices (SEEDs) have been made [2,3] with fast switching times and low operating voltages and energies. The processing elements in these chips, the symmetric SEEDs (S-SEEDs) [4], have limited processing capabilities, in that they are set-reset latches and can be made to perform logic functions by pre-setting the device to a given state. We can, in theory, achieve arbitrary logical functionality by using a separate group of quantum well detectors similarly configured to the field effect transistors in CMOS and NMOS circuits to drive a S-SEED configured as an output modulator [5]. These devices have many desirable qualities including time sequential gain, effective input-output isolation, signal level and timing regeneration, wavefront quality restoration, and operation over decades in power levels due to the differential nature of the devices.

In this paper, we describe the first integrated arrays of these devices. In the first array of devices, each device or processing element has the functionality required to implement a photonic switching node. In the second array of devices, elements can be configured as photonic switching nodes as well as multiplexers, demultiplexers, or shift registers. Since these arrays were made using the same batch fabrication procedures that have yielded the large S-SEED arrays [6], we feel that the capability now exists to make large scale optoelectronic circuits of arbitrary functionality.

SEED 2 x 1 Photonic Switching Nodes.

The function $E=A\cdot B + C\cdot D$ implements a switching node with two data inputs and one data output (a 2 x 1 node) if A and C are the two input channels and B and D are the two control channels.

If control input B is a logic "1" and control input D is a logic "0", then output E is equal to data input A. Like-

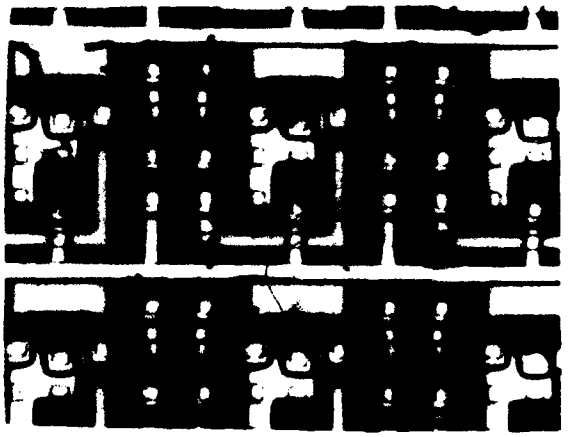


Fig. 1 Photograph of a section of the 4 x 4 array of 2 x 1 switching nodes.

wise, if control input B is a logic "0" and control input D is a logic "1" then output E is equal to data input C. The device arrays are differential in that the logic state of each data and control input as well the output are represented by the ratio of optical powers of two light beams. An input has a logic "1" state when the uncomplemented input is greater than the complemented input (e.g. A > $\overline{A}$).

A photograph and schematic diagram of the first array are shown in Figs. 1 and 2. The functionality of this circuit has been previously demonstrated by electrically connecting S-SEEDs on different chips [5]. The integrated 4 x 4 arrays have 5 μm x 5 μm optical windows, with each pair of input and output windows on 20 μm centers. The unit cell size is $(55\ \mu m)^2$ which is slightly larger than two S-SEED devices with the same window size [3], although three S-SEEDs would be required to implement this function [7].

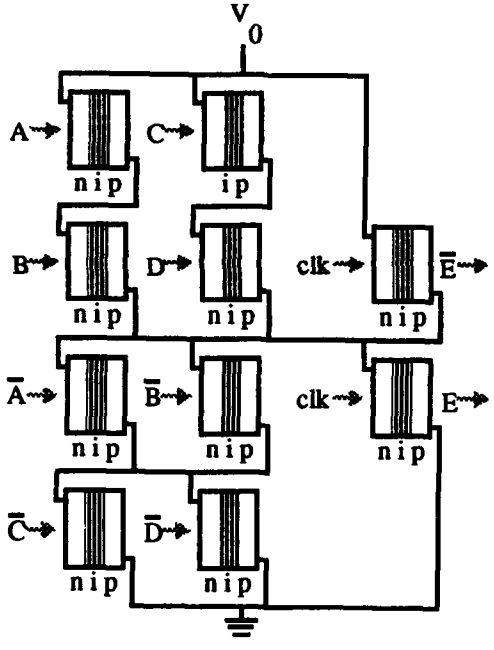


Fig. 2 Schematic diagram of a 2 x 1 switching node.

We tested the operation of the array using two differential quantum well modulators to provide the input signals to one of the switching nodes. An acousto-optically modulated Ti:Sapphire laser provided a pair of control beams, B and $\overline{D}$, (these are logically equivalent) and a current-modulated semiconductor laser diode provided the other pair of control beams, $\overline{B}$ and D. A semiconductor laser diode provided the pair of equal power clock beams which in turn are modulated by the device as the complementary outputs. Input A was modulated with an alternating "0 1 0 1" pattern and input C was modulated with a "0 0 1 1" pattern. The control of the device alternated between selecting input A and input C every 4 bits. An oscilloscope photograph showing that output E has the correct functionality is shown in Fig. 2b. We tested all 16 devices in the array and they all gave the correct outputs.

The switching speed of the devices of 10 μs was limited by the incident signal powers which were only ~333 nW and ~667 nW for the "low" and "high" states of the differential inputs. We can define a required differential optical energy as the difference in power multiplied by the switching time. If a single input were supplied it would need this much energy. The required differential input energy per input is then ~3.3 pJ at 9 volts, which compares favorably with the 2.5 pJ at 15 volts required for the S-SEED arrays with the same window sizes. The extra energy is expected, since the integrated switching node capacitance is greater than that of S-SEEDs. Less optical power may be required to build a photonic switching system from these gates than from S-SEEDs, because the number of gates, and thus the number of clock beams, is less. In addition, since two stages of logic gates are normally required to implement a 2 x 1 switching node, fewer stages of integrated switching nodes are needed in a multistage network.

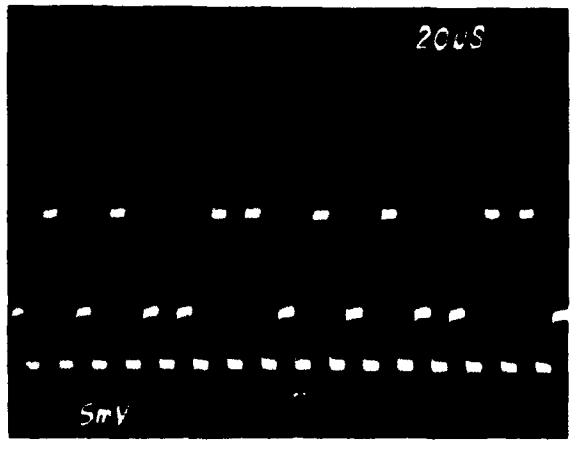


Fig. 3 Experimental demonstration of a 2 x 1 photonic switching node (Input data signals were "0 1 0 1" and "0 0 1 1" and control alternated every 4 bits between inputs A and C.)

SEED 2 x 1 Photonic Switching Nodes (Type II)

A photograph and schematic diagram of part of the second array is shown in Figs. 4 and 5. Neighboring S-SEEDs are connected by an optoelectronic transmission gate consisting of a pair of back-to-back quantum well photodiodes. These photodiodes implement the function of a transmission gate in MOS circuits, essentially transferring the voltage from one S-SEED to another. Three S-SEEDs and two of these optoelectronic transmission gates make up a single 2 x 1 switching node. The array consists of a 32 x 16 array of S-SEEDs and since three S-

SEEDs makes up a switching node, it can be configured as a 10 x 16 array of switching nodes.

All optical windows are 5 μm x 5 μm. The distance between S-SEED inputs (i. e. between A and $\overline{A}$ or A and E) is 20 μm. The distance between control inputs (B to B or B to D) is also 20 μm.Control inputs and data inputs (e. g. A and B) are separated by 10 μm. Switching nodes may be located on 60 μm x 40 μm centers for a 10 x 16 array or 80 μm x 40 μm centers for a 8 x 16 array. In the latter case, there is an unused S-SEED between nodes and all data inputs (A to C to the next A, etc.) are on 40 μm centers.

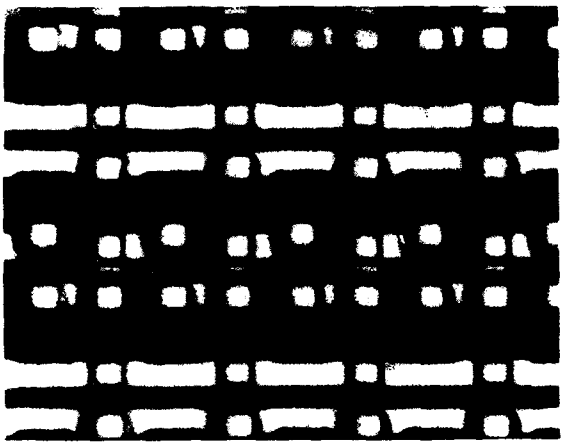


Fig. 4 Photograph of part of the second switching node array.

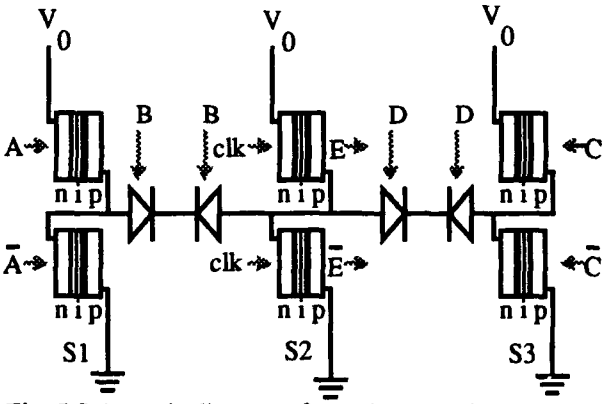


Fig. 5 Schematic diagram of part the second array configured as a switching node

In the experiment to test the operation of a switching node, the data signals, A, $\overline{A}$, C, and $\overline{C}$, and the control signals, B and D, are were generated using differential quantum well modulators. A 1 x 2 binary phase grating split each output from the control differential modulator (i. e. B and D) into the two beams that are required by the back to back diodes. The output signal is shown in Fig. 6.

The maximum speed of ~1 μs was limited by the power of the control signals, which in this case, were ~760 nW and ~1.5 μW for the "low" and "high" control beams respectively. Thus, the required differential control beam energies were ~750 fJ. For the node to function properly, the signal beam powers must be greater than the control beam powers, otherwise the unselected input can influence the output state of the node. In our experiment, the signal beam powers were ~1.8 μW and ~3.6 μW and ~1.3 μW and ~2.5 μW for the low and high states of inputs A and C respectively. In this case the required signal optical energies were 1.3 pJ and 1.8 pJ for the two inputs.

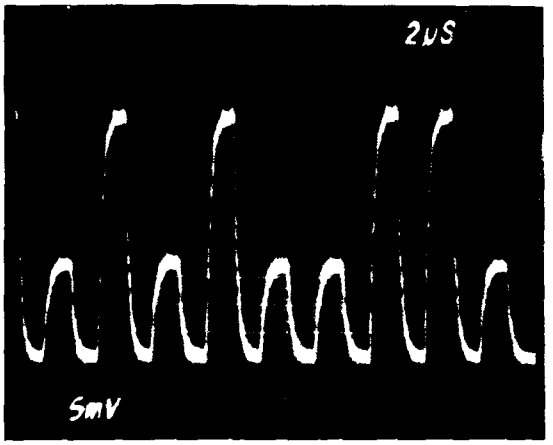


Fig. 6 Experimental results demonstrating operation of the second array as a 2 x 1 switching node.(Input data signals were "0 1 0 1" and "0 0 1 1" and control alternated every 4 bits between inputs A and C.)

We have also tested an 8 x 16 array of 2 x 1 switching nodes operating concurrently using input data generated by a S-SEED array acting as a memory. The experimental set-up is shown in Ref. [8] with the first S-SEED in that experiment used to generate the data and second S-SEED array in that experiment replaced by this array of 2 x 1 nodes. The S-SEED windows are oriented vertically. We will call the output a logic "one" when the top diode has greater reflectivity than the bottom one. The left half of the input S-SEED array was set to a logic "one"and the right half of the S-SEED array was set to a logic "zero". The outputs from a 4 x 8 section of this array are shown in Fig. 7a. The outputs from this array were imaged onto the array of 2 x 1 switching nodes using a crossover interconnection network [9].

The input to the switching node array (output of the crossover interconnection network) consists of two overlapped images, one identical to the S-SEED output and one with a left to right inversion caused by the prism in the crossover network. The left S-SEED, S1 in Fig. 5, of each 2 x 1 node had a logical input equal to the logical output of the S-SEED array (non-altered image) as shown in Fig. 7a, while the right S-SEED, S3, of each 2 x 1 node had a logical input equal to complement of the logical output from the S-SEED array (inverted image) as shown in Fig. 7b. Therefore, each 2 x 1 switching node

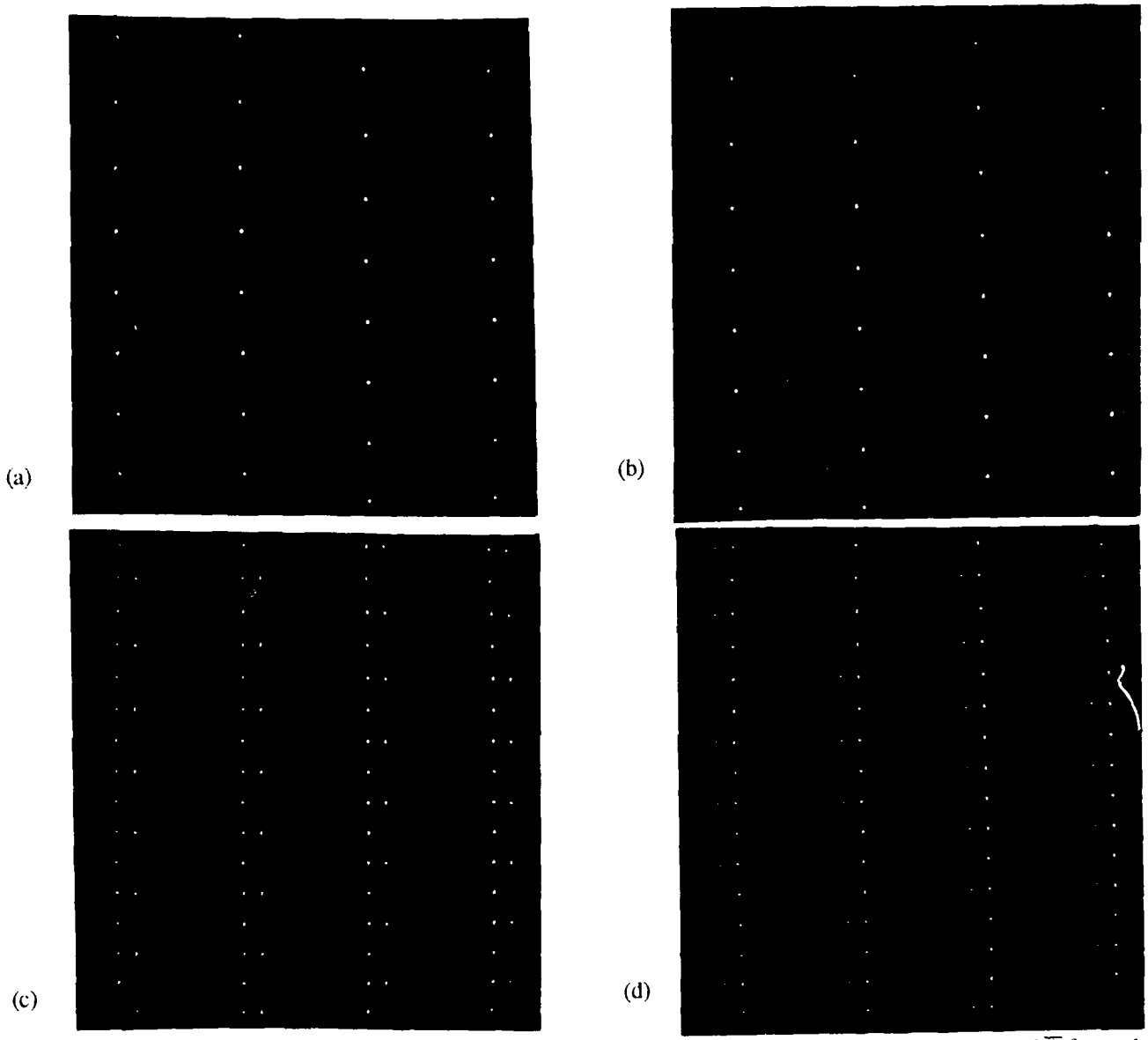


Fig 7 Inputs and outputs from a 4 x 8 section of 2 x 1 switching nodes operating concurrently a) inputs A and $\overline{A}$ for each device, b) inputs C and $\overline{C}$ for each device, c) output for B=1 and D=0 (input A selected) and d) output for B=0 and D=1 (input C selected) Recall the S-SEEDs are naturally inverting.

had one of its two data inputs as a logic "one" and the other of its data inputs as a logic "zero" (see Figs. 7a and 7b).

A single set of control beams was generated by passing the output of a laser diode through a 32 x 8 binary phase grating. The control signal selected either data inputs A and $\overline{A}$ or data inputs C and $\overline{C}$ by moving a mirror in the system to direct the control beams to their appropriate transmission gates. Since there was only a single set of control beams all nodes were controlled the same.

The data outputs from the array of 2 x 1 switching nodes are shown in Figs. 7c and 7d for a 4 x 8 section of switching nodes. In these figures, there are eight columns of spots arranged in four groups of two. Recall that two diodes of a particular S-SEED are oriented vertically. In Fig. 7c, the 1st, 3rd, 5th, and 7th columns are the control beams which are incident on transmission gates, B, to the left of the center S-SEED, S2. In this case, the control beams selected input A. The 2nd, 4th, 6th, and 8th columns are the output beams E and $\overline{E}$. Since the S-SEEDs are naturally inverting, output E is equal to the complement of input A. In Fig. 7d, the control beams selected input data C and $\overline{C}$ (i. e. B=0, D=1). In this Figure, the 2nd, 4th, 6th and 8th columns are the control beams which are incident on transmission gates with control

input D, to the right of the center S-SEED, S2. The 1st, 3rd, 5th and 7th columns are the outputs E and $\bar{E}$. Again, output E is inverted from input B due to the inverting nature of the S-SEEDs. For the 8 x 16 array of nodes, correct operation was observed for 124 out of 128 devices for both logic "ones" and logic "zeros" on each node input. The four devices that did not work correctly had debris on the device windows. No crosstalk was found between adjacent 2 x 1 nodes in the center of the array.

SEED Multiplexers and Demultiplexers

A single 2 x 1 switching node was also tested as a 2 x 1 multiplexer. As a multiplexer, first one input is selected and then the other. The A and C input data were generated using differential quantum well modulators. The clock beams incident on the A modulator were out of phase to the clock beams incident on the C modulator. The control beams were generated by a third differential modulator. The light beams incident on this modulator were not modulated. The output clock beams were modulated at twice the data rate of the input clocks. In this experiment the data inputs were "0 1 0 1" and "0 0 1 1". The multiplexer output is shown in Fig. 8.

The 2 x 1 switching node was also tested as a demultiplexer. Two laser diodes generated the set of input beams incident on the center of the three S-SEEDs. Two additional laser diodes each generated one of the sets of clock and control beams. Fig. 9 shows the data input and data outputs. The data input was chosen so that when demultiplexed it would have outputs of "0 1 0 1" and "0 0 1 1". Correct operation of the device was observed.

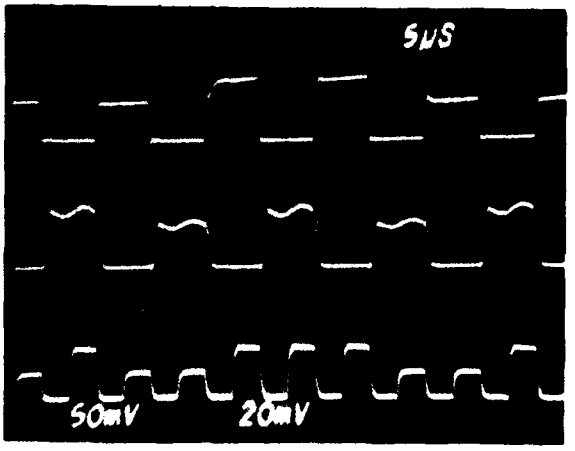


Fig. 8 Experimental results demonstrating operation of the second array as a 2 x 1 multiplexer. The top two traces are the input data traces and the bottom trace is the output trace.

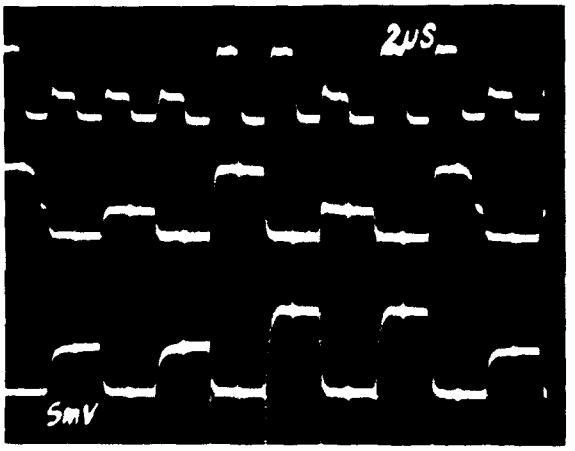


Fig. 9 Experimental results demonstrating operation of the second array as a 2 x 1 demultiplexer. The top trace represents the data input and the bottom two traces are the multplexed outputs.

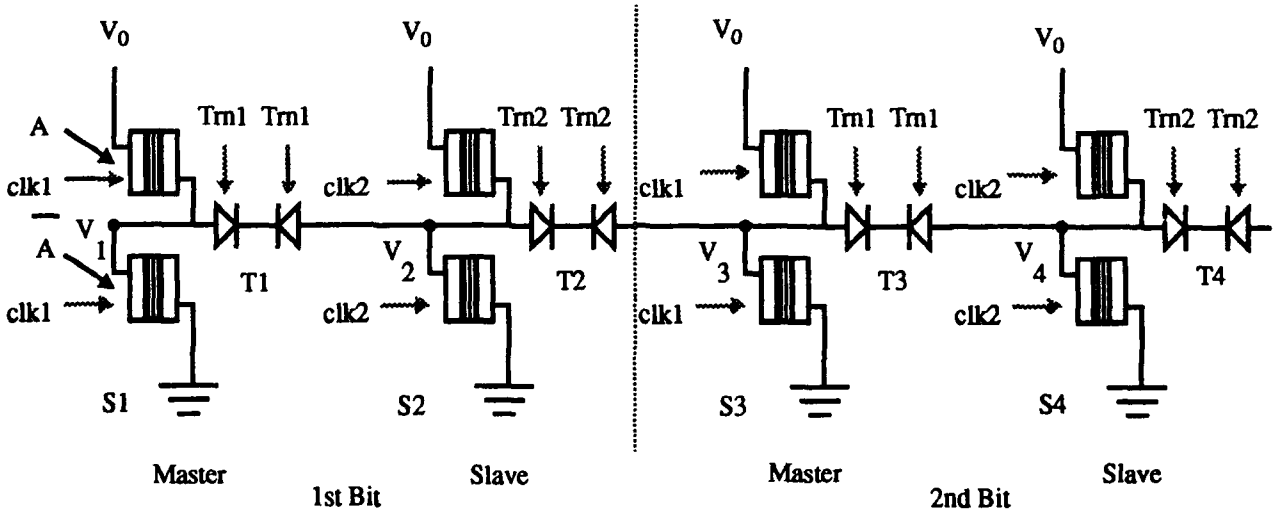


Fig. 10 Schematic diagram of the array configured as a shift register.

SEED Shift Register

The array can be also configured as a shift register as shown in Fig.10. The operation of the device is described below. First, the input signals set the state of the first S-SEED, S1. Then simultaneously, the clock beams, clk1, and transfer beams, Trn1, are applied. The clock beams provide an output signal from S1 and hold the state of S1 while transfer beams, Trn1, transfer that state to S2. The power in the transfer beams must be less than that of the clock beams to ensure that S1 retains its state. Otherwise, V_1 will be influenced by V_2 and S1 may lose its state. Then, clock beams, clk2 and transfer beams Trn2 are applied to S-SEED S2 and transmission gate T2 to read the state of S2 and transfer the voltage on S2 to S3. Simultaneously, the input signals are applied setting the new state of S1. Analogous to electronic shift registers, the odd numbered S-SEEDs are called master flip-flops and the even numbered S-SEEDs are called slave flip-flops. Because of the two-cycle nature of the clock beams, two S-SEEDs (a master-slave flip-flop) holds one bit of information. Thus, 2N S-SEEDs implement a N bit shift register.

We demonstrated 2, 4, and 8 bit shift registers using part of the array. A pair of semiconductor laser diodes generated the complementary input data stream which consisted of a logic "one" followed by seven logic "zeros". Four additional semiconductor lasers provided the clock, transfer, complement clock, and complement transfer beams. Binary phase gratings produced either 2, 4, or 8 replicas of the input beams [10]. The parallel outputs from the 2nd, 4th, 6th, and 8th bits of the 8 bit optical shift register along with the data input are shown in Fig 11.

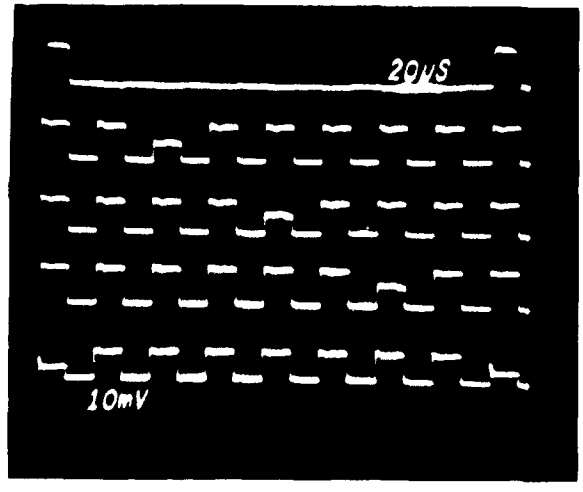


Fig. 11 Optical input and parallel outputs from the 2nd, 4th, 6th and 8th bits of the 8 bit optical shift register.

Conclusion

In conclusion, we have built and tested arrays of integrated SEED based 2 x 1 photonic switching nodes, multiplexers, demultiplexers and shift registers. The arrays were made using the same batch fabrication procedures as our previous S-SEED arrays. We have tested individual switching nodes, multiplexers and demultiplexers, have operated a 8 x 16 array of switching nodes concurrently, and have built an eight bit shift register using these arrays. The performance of the arrays is good enough to continue to conduct photonic switching systems experiments with these devices.

Acknowledgment

We would like to thank S. J. Hinterlong for supplying the laser diodes used in our experiments and the members of the photonic switching technologies group for their help with the system of ref. [8] that was used in the operation of the 8 x 16 array of SEED switching nodes.

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Multistage Reconfigurable Optical Interconnection Network Using Polarization Switch Arrays

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Abstact

In this paper, we propose a multistage optical interconnection network using polarization switch arrays which is capable of realizing a multichannel reconfigurable optical interconnection network. The basic operation has been demonstrated with two-stage 4x4 network testbed using liquid crystal light valves (LCLVs). Furtheremore, the feasible channel number as a function of the optical beam size and the routing algorithm for the 8x8 nonblocking crossconnect network are discussed. Finally, a concept of the extended 16x16 Banyan network suitable for the integrated structure is presented.

1. Introduction

Because of the high-bandwidth, high-speed transmission, parallel multibeam inputs, and the absence of mutual interference, an optical free-space interconnection is considered to be promissing to overcome the data transfer bottleneck in the conventional electrical interconnections between computer equipments, circuit boards, and LSI chips. Therefore, many attempts have been made to achieve the practical implementation of the technology. Some of such attempt are found in [1], [2], [3].

In this paper, we propose a multistage optical interconnection network using polarization switch arrays which is capable of realizing a multichannel reconfiguable optical interconnection network. We present the two-stage 4x4 interconnection network testbed using liquid crystal light valves (LCLVs) and its loss property. Furthermore, an improved structure based on the "minimized-path-length-difference" concept and a nonblocking self-routing algorithm for the 8-input 4-stage modified optical Banyan network are discussed. Finally, the integrated structure for the compact multichannel implementation of the network is proposed.

2. 4x4 Optical Interconnection Testbed with Input and Output Fiber Arrays

Fig. 1 shows the block diagram of the 2-stage 4x4 optical Banyan network testbed. Input and output fiber arrays are used to demonstrate the multichannel interface to the optical fiber networks. We used liquid crystal light valves (LCLVs) for the polarization control devices. The network reconfiguration is made by controlling the light of LED array which illuminates the back surface of the LCLV.

Table 1 shows the measured fiber-to-fiber insertion loss. Since there exist 4!(=24) different interconnection configurations, we measured losses for all 24 cases and averaged the values. The measured value is the sum of the loss of optical elements along the optical path, including 12 dB deadloss of two beam

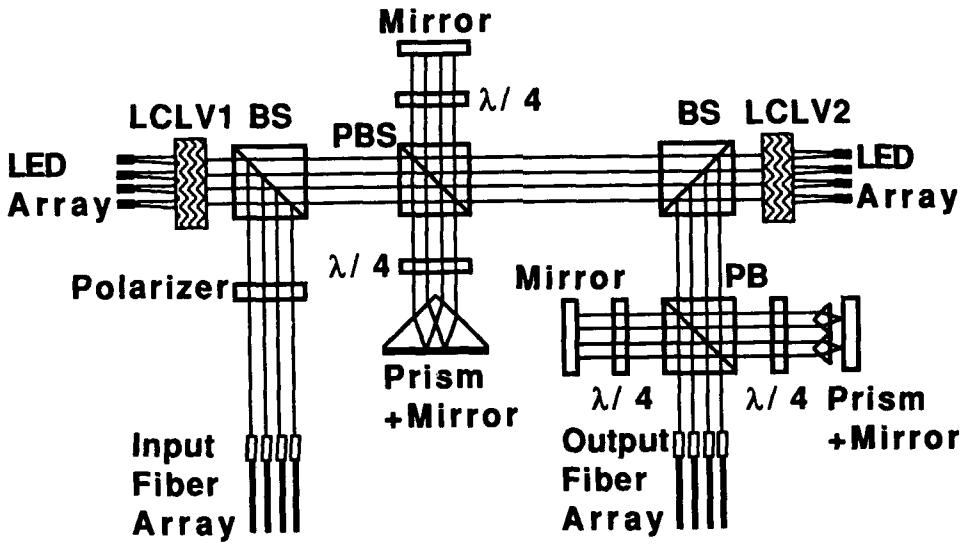


Figure 1. 2-stage 4x4 optical Banyan network testbed

path, including 12 dB deadloss of two beam splitters, 3.5 dB reflection loss of two LCLVs, and the fiber coupling loss which is estimated to be about 8 dB. In order to decrease these losses, not only the improvement of each component but also the reduction of the total travel length of the optical beam is imortant because it increases the difficulty in the precise alignment of the optical components, causing the mis-alignment losses.

		output channel			
		0	1	2	3
input channel	0	25.2	32.4	30.9	34.5
	1	40.5	22.8	35.2	30.4
	2	27.3	34.0	24.4	29.4
	3	35.3	28.2	32.2	23.2

(dB)

Table 1 Avaraged loss values

3. Multistage Implementation of the Optical Network

3.1 Analysis of the Feasible Channel Number

The optimal design of the multistage optical switch can be achieved by obtaining the feasible channel numbers N and the beam diameter ω_0 (at the emission at the input port) in such a way that the beam spread of the neighboring beams after traveling the length L should not overlap with each other. Fig. 2 shows a model of optical beams traveling through our optical network. Here, let λ be the wavelength of the beam, ω_0 be the beam diameter at the emission from the input port, where N Gaussian beams separated with each other by the distance d, ω be the beam diameter at the distance L and d(N+1) be the length of PBS, equivalently the basic size of the switch, and ΔL be the length of the beam which travels outside the PBS, then it follows that

$$\omega = \omega_0 \sqrt{1 + (\lambda L/(\pi \omega_0^2/4))^2} \qquad (1)$$

where,

$$L = \log_2 N[2d(N+1)+\Delta L]. \qquad (2)$$

Using these equations and the condition that $\omega < d$, we can calculate the relation between N and ω_0 as shown in Fig. 3. It can be observed in Fig. 4 that if the beam diameter

ω_0 at the emission ranges from 0.5 to 0.9, for example, then 32 input channels can be accomodated in the PBS with the size being 30 mm, which is shown by the shaded area in Fig. 3.

3.2 Minimized-Optical-Path-Length-Difference Concept of the Optical Switch Design

The basic optical configuration of the interconncection network proposed in [2] has such characteristics that the optical path length of the bypass mode is much shorter than that of the exchange mode. Since signals will pass various optical routes depending on the asigned interconnection configurations, such problem will arise that the amplitude of the optical pulse as well as its arrival time will differ for each bit sequence or packet at the output port. To solve this problem, we introduce a new optical configuraton as shown in Fig. 4, where the difference of optical path

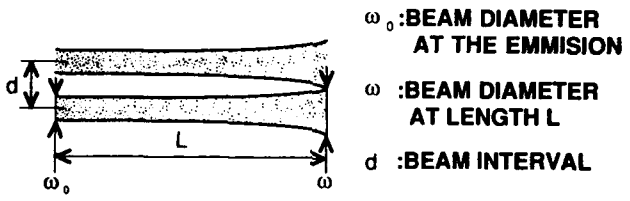


Figure. 2 A model of optical beam in the network

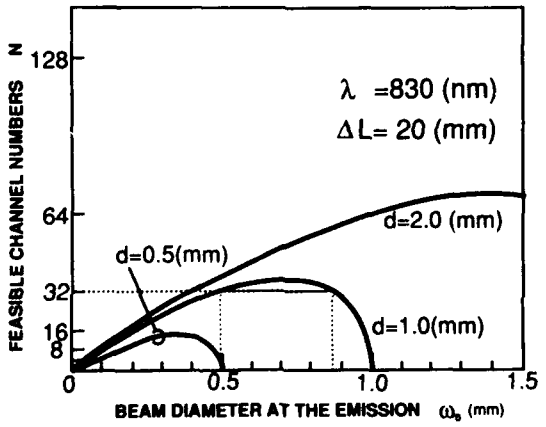


Figure 3. The relation between the beam diameter and the feasible number of input channel

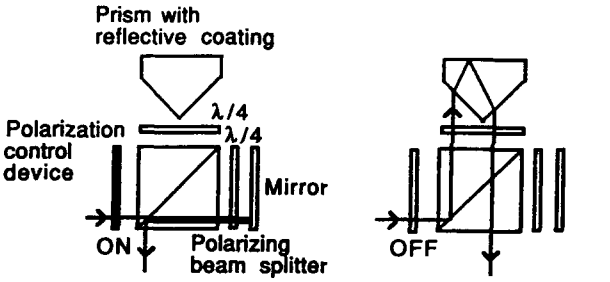


Figure 4. Improved basic configuration based on the "minimized-optical-path-length-difference" concept

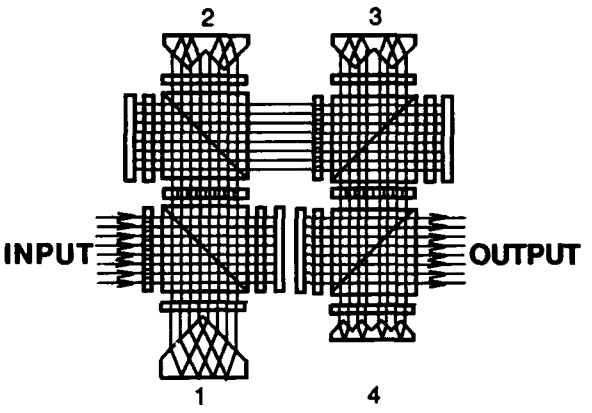


Figure 5. A new configuration of 8-channel modified Banyan network

in two modes is minimized. Based on this configuration, we designed a new 8-channel modified Banyan network as shown in Fig. 5. The advantage of the proposed configuration would be easier alignment than the circularly multistage network, as proposed in [3].

3.3 Routing Algorithm for the 8x8 Modified Banyan Network

We have proposed a 3-stage 8x8 optical Banyan network [2]. As it has some blocking interconnection cases in such a network, the configuration should be rearranged to achieve the nonblocking characteristics and its polarization-controlled routing algorithm should be considered. It is possible to modify

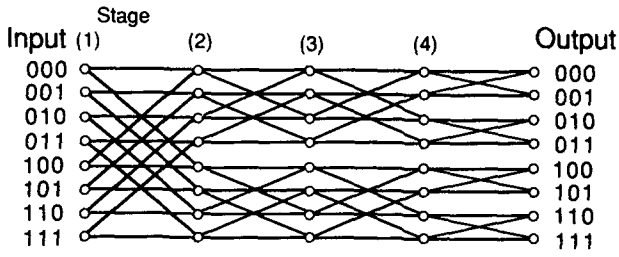


Figure 6. Equivalent circuit of the 8-channel modified Banyan network

it by inserting a redundant second stage and by taking advantage of the property that two beams entering into the same switch node are either P or S polarized, we can get the non-blocking network as shown in Fig. 5. The configuration shown in Fig. 4 has been designed by taking this nonblocking condition into account.

The control algorithm for the polarization switches at each stage to achieve the required network routing is given by the following two logic equations.

For 1st ,3rd, and 4th stage:
SC= PS XOR (NB(M) OR FB(M)) (3)

For 2nd stage:
SC= PS XOR FB(2). (4)

where, SC is the state of the polarization switch (=0: off and =1: on), PS is the polarization of the input beam at each switch element (=0: p-polarized and =1: s-polarized), and NB(M) and FB(M) are the Mth bit of the binary represented address of each switch element at each stage and that of the destination output node to be reached, respectively.

In order to confirm the nonblocking property of the above algorithm, we simulated the routing of the network by a computer. Since there are 8!(=40320) different interconnection configurations in the 8x8 network, we checked all of these cases and found out none of them are blocking.

4. A Proposal of A Two-Dimensionaly Arranged Multi-Channel Optical Interconnection Network

Our goal is to search for the highly parallel optical interconnection network architecture and integrated structure, which can be made compact. Fig. 7 shows one of such examples. It is a three stage cascaded 16x16 nonblocking Banyan network, which we call "Cross-Banyan network". Its equivalent circuit is shown in Fig. 8. Since this switch can be constructed by stacking many identical building block components, it is easily fabricated and suitable for the compact implementation. It remains to be investigated to achieve proper nonblocking network configuration based on this concept.

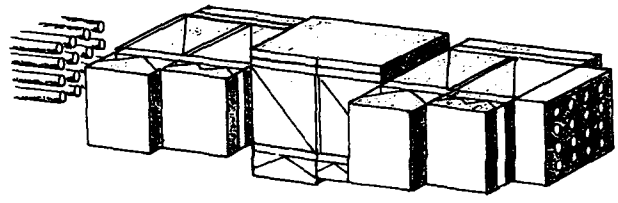


Figure 7. Integrated structure for 16x16 interconnection network

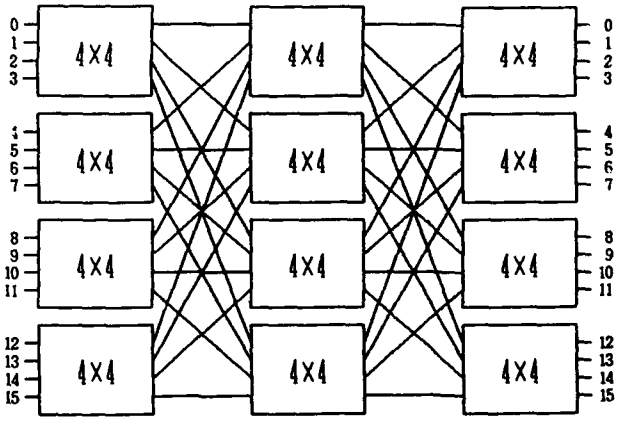


Figure 8. Equivalent circuit of the 16x16 interconnection network

5. Summary

We measured the loss and crosstalk properties of the 4x4 optical switch testbed using LCLVs for polarization switch devices, and analyzed

the maximum number of feasible input channels. 32 channels arranged in one dimension are found to be feasible. Also, the new configuration of modified Banyan network as well as two-dimensionally arranged multichannel optical inteconnection network have been proposed. The future problem is to prove the nonblocking crossconnection routing property of the latter and to fabricate a compact multi-channel interconnection module using liquid crystal polarization switch arrays.

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Broadcast Star Network Based on a Planar Waveguide Medium

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Abstract

This paper proposes the use of a two-dimensional planar optical waveguide as a broadcast medium in a semiconductor-wafer scale optical interconnection network. The use of a 2-D guide as a substitute for a conventional star coupler is seen to eliminate the need for optical fiber or integrated optical waveguides together with all precision alignments between the waveguides, sources, and detectors. Received optical power is shown to scale inversely with the number of stations in the network, just as for the case of the star-coupler-based network, with an additional network-size-independent loss of at most 13 dB. The proposed scheme is capable of providing a 7 Mb/s interconnection channel for each pair of elements in a 256-element planar array of electronic circuits.

Introduction

Techniques for using optics to replace wire interconnections between electronic circuits have generally fallen into two categories: the one-dimensional waveguide cases which use optical fibers or integrated waveguides and the three-dimensional techniques which transfer optical signals through free-space using imaging lenses or holograms [Ref. 1]. While guided wave interconnections are efficient in their use of optical energy, they require precision alignments at the ends, occupy more area than integrated circuit wires, and do not take advantage of the non-interacting property of optical signals. They are most appropriate for applications requiring the interconnection of relatively large electronic circuits over significant distances.

Imaging, using lenses or holograms, is capable of spatial interconnection densities approaching one connection per square wavelength (about one micron for optoelectronic sources). Furthermore, such techniques do exploit the non-interacting nature of optics. Free space architectures, however, share a serious problem: propagation path lengths must be approximately equal to, or greater than, the image linear dimensions to avoid impractically large numerical apertures. For the case of interconnections between pairs of N element arrays, for example, this means that not only will propagation delays increase as $N^{1/2}$, but also the packing efficiency (elements per unit volume) will fall as $N^{-1/2}$.

This paper proposes the use of a two-dimensional planar configuration which takes advantage of the special properties of optical signals and yet does not have many of the disadvantages of previous proposals. The scheme has many of the features of an optical broadcast network based on a star coupler [2] without the need for either the individual guided waves, and their associated optical alignments to sources and detectors, or the coupler itself. The price paid for these simplifications is an excess loss penalty of about 13 dB and a large dynamic range requirement on the optical receivers, compared with the complete star coupler network.

The proposed broadcast technique is discussed here in the context of an application involving a wafer-scale multi-processor computer. The additional possibility of wafer cascading, which leads to a densely packed three-dimensional interconnection architecture, is discussed briefly.

A Planar Broadcast Network

Figure 1 shows two views of a planar-waveguide-based network in which the various layers which

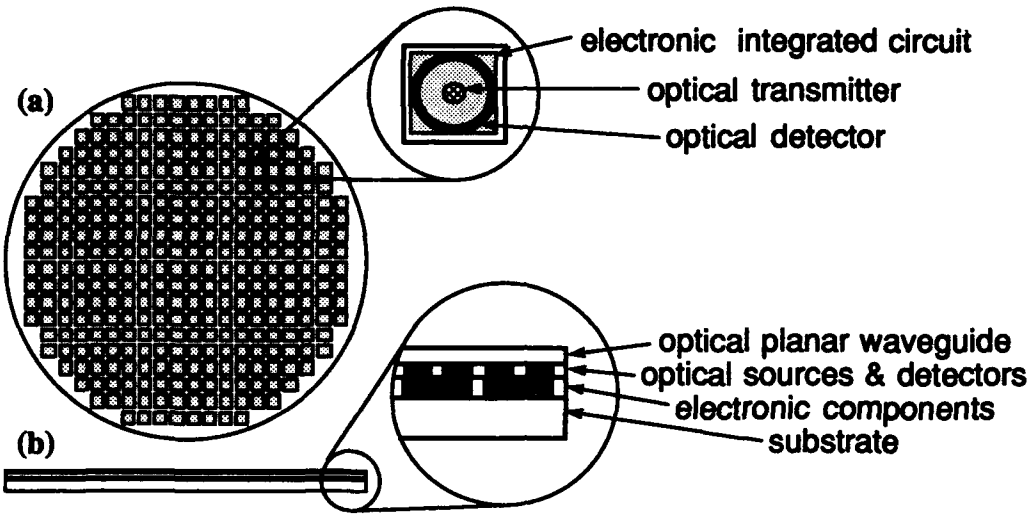


Figure 1. Top (a) and edge (b) views of a proposed wafer-scale network of electronic circuits (e.g. microprocessors) interconnected via a two-dimensional optical waveguide. The planar waveguide distributes signals from each optical transmitter to all receivers in a broadcast and select mode.

make up the electronic and optical components are identified. A hybrid layered structure may be implemented with a Si electronics layer and a III-V compound layer for the optical devices to avoid the need for true optoelectronic integration. In the figure, each element in a planar array of electronic processors is in electrical contact with an optical source and an optical detector used for communications with the other elements.

The top layer, adjacent to that containing sources and detectors, is the optical guiding layer which is designed to confine light to propagate within the plane. The guide may be designed to support one or more nodes of the optical field in the dimension perpendicular to the plane, corresponding to the analogous cases of single and muli-mode cylindrical guide.

Light propagates in the plane in much the same way that radio waves travel along the surface of the earth: signals coupled omnidirectionally into the guide at any point on the disc are broadcast to every receiving element on the wafer. The material may be either silica, deposited on the optoelectronic substrate, or a semiconductor with appropriately wide bandgap to minimize propagation loss. To avoid standing wave patterns, the edges of the wafer are coated so that the optical signals are absorbed rather than reflected.

Coupling of light from vertically emitting sources into the guide may be accomplished with high efficiency using perturbations in the waveguide [Ref. 3]. The coupling strength between the guide and the detectors is discussed below along with other issues that determine the optical power distribution.

Previous proposals for the use of planar optical guides have concentrated on their use as a point-to-point interconnection medium with planar optical elements on the surfaces (or external to the guide) used to image and direct the light [Ref. 4-5]. In contrast, a true broadcast mode of operation is exploited in the present proposal.

Optical Power Distribution

There are three dominant factors which determine the fraction of transmitted power that is detected by a particular receiver: geometry, propagation loss, and waveguide-to-detector coupling strength (see Figure 2). Broadcasting from a point source in two dimensions results in a received signal strength which is proportional to the angle, θ, subtended by the detector at a distance l from the source. The detected signal strength will fall as $1/l$, unlike the case of broadcasting in three dimensions, where the signal strengths fall as $1/l^2$. For a detector diameter d, and a wafer diameter D, the smallest subtended angle is:

$$\theta_{min} \sim d/D.$$

A 1 millimeter diameter detector at the maximum distance from a source on a 4-inch wafer results in a signal spreading loss of about 25 dB.

Since the signal strength depends on the detector linear dimensions while the detector's capacitance (and therefore its bandwidth) depends on its area, the

geometry of the detector should be appropriate to minimize area, such as a ring or an "X". Also, the detector must be only weakly coupled to the waveguide to avoid shadowing other detectors, as discussed below.

Propagation loss, in a well designed waveguide, will be dominated by the signal absorbed by other detectors along the path from source to desired detector. In the example shown in Figure 2, the signal must pass $(n-1) \sim D/d$ detectors to cross the wafer. If the coupling between the waveguide and the detectors is set such that the fraction, C, of guided light passing a detector is absorbed ($C < 1$), then the portion of the transmitted light arriving at the nth detector is

$$(1-C)^n .$$

Since the coupling into the nth element is also C, the detected signal will be proportional to

$$C(1-C)^n .$$

The coupling strength which maximizes the signal in the last detector is just

$$C = 1/n,$$

so that the detected signal is given by

$$P_{det} = P_{trans}\,(\theta/2\pi)\,(1/n)\,(1-1/n)^n .$$

For n larger than a few, the last factor becomes

$$(1-1/n)^n \sim 1/e$$

and the minimum detected power is

$$P_{det} = P_{trans}\,(d/D)^2 / (2\pi e).$$

Finally, for the geometry considered here, this becomes

$$\boxed{P_{det} = (P_{trans}/8e)\,(1/N),}$$

where N is the total number of elements in the array.

The relationship above gives the minimum detected optical signal power for the planar-waveguide network. This should be compared with the best possible case which is that of optical power distribution by an ideal star coupler. In this case

$$P_{det} = P_{trans}/N,$$

so that the penalty for using the planar configuration is seen to be at most $1/8e$, or 13.4 dB, and in both networks the received power falls as $1/N$.

Detectors nearer to the transmitter will receive a significantly stronger signal. The maximum detected signal is given by

$$P_{det} = (P_{trans}/2\pi)\,(1/N)^{1/2},$$

so that the dynamic range (ratio of maximum to minimum signal strengths) encountered at the receivers is

$$\boxed{R = (4e/\pi)\,(N)^{1/2}.}$$

The distribution loss and dynamic range are plotted as functions of N for a 4-inch diameter wafer in Figure 3. Implications of these results for the network capacity are discussed below.

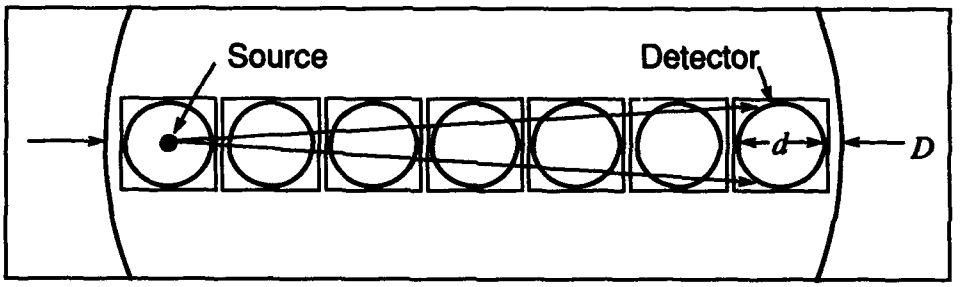


Figure 2 The minimum detected signal (i.e., that detected when transmitter and receiver are at the maximum separation) is determined by the linear dimensions of the detector and wafer and the absorption of signal due to intervening detectors (see text)

Sample System Parameters

As an example of the application of such a network, sample parameters are obtained for a single-channel time-division-multiplexed data bus which provides communications among microprocessors in a wafer-scale multiprocessor array. Assuming a 4-inch diameter semiconductor wafer equally divided into N local computation regions allows, for example, approximately 30 square millimeters per element, or about that of a microprocessor chip with 10^4 gates, when $N = 256$. This area will contain electronic logic and storage as well as an optical transmitter and receiver.

We can estimate the maximum receiver data rate by assuming that a receiver sensitivity of 1000 photons per bit will be achieved, this is 100 times more than the quantum limit for a bit error rate of 10^{-9}. An integrated optoelectronic receiver operating at 1.3 μm wavelength, and occupying only about one

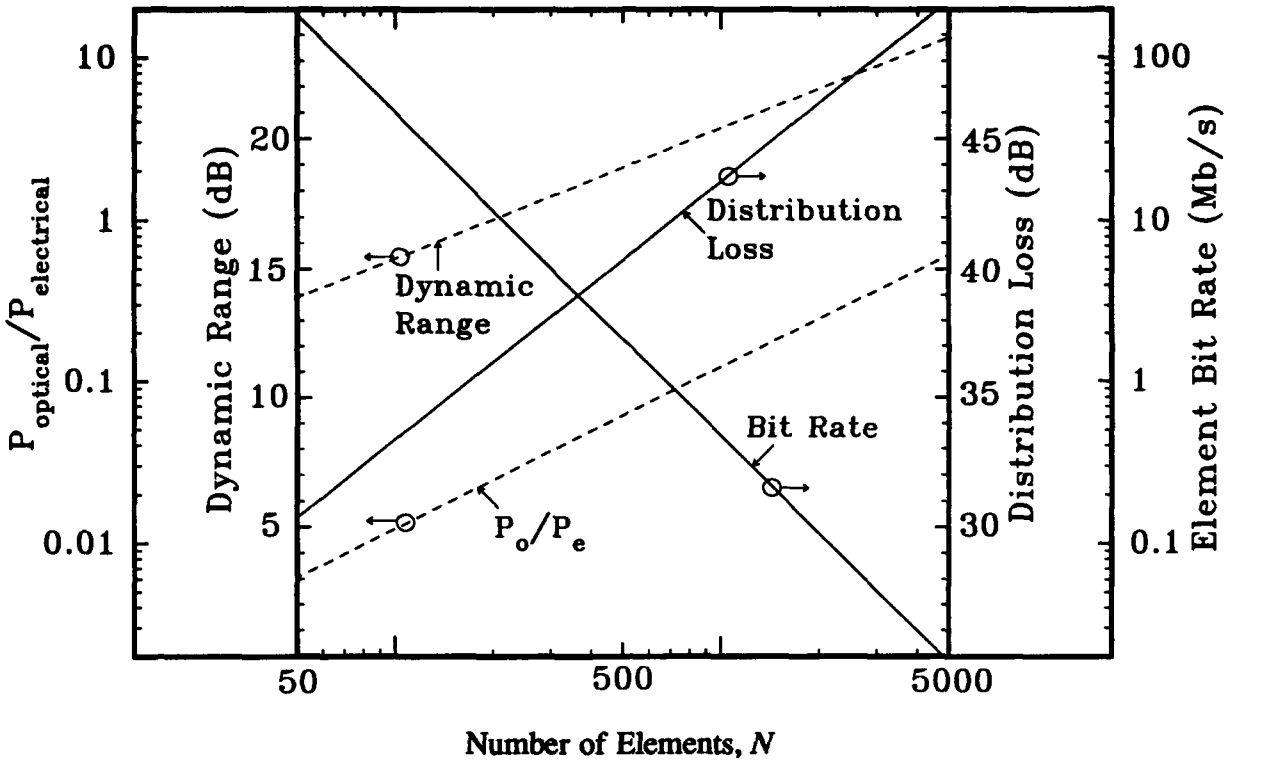


Figure 3. This graph shows the range of parameters anticipated for a wafer-scale microprocessor array interconnected by a planar optical bus plotted as a function of N, the number of elements, and assuming a 4-inch diameter wafer.

square millimeter of chip area, has already been demonstrated with a sensitivity of 5000 photons-per-bit[Ref 6]. Sufficient electronic gain to bring the signal level to that appropriate for the logic circuits would also be required.

For transmitter powers of 1 mW and power distribution loss calculated as discussed above, the maximum received bit rate is found to be just under 1 Gb/s for $N = 256$. This bandwidth is then divided by the number of element pairs to determine the bit rate available on average to each pair (about 7 Mb/s in this case). The results are plotted as a function of N in Figure 3.

Finally, the dc power dissipated by the optical sources must be compared with that expected from the electronics. This ratio, assuming that the optical components dissipate 20 mW of power per element, is also plotted in Figure 3. It shows that power dissipation by the optical components will not be a significant issue for $N < 5000$.

The resulting network might be operated in a manner similar to that of an Ethernet bus, although the time-division-multiplexed channel capacity is as much as 1000 times greater and the propagation time is less than one nanosecond. In use, the full bandwidth would be available for individual data transfers but this must be done sequentially since there is only channel. If even greater capacities are required, the optical bandwidth of the medium may be exploited using wavelength multiplexing. Multiple channels might operate in parallel at different wavelengths or wavelength routing could be used with tunable optical sources or detectors. Such optical broadcast systems have been explored extensively for telecommunications applications and have been demonstrated using both conventional (direct) optical detection and optical heterodyne detection [Ref. 7].

It will ultimately be necessary to move data on or off of the single wafer discussed here. This can be done using optoelectronic interface units. However, in order to achieve communications between wafers without restricting the total data flow rate, parallel interconnections will be desirable. One way to accomplish this is through the use of point-to-point communications links between corresponding elements on adjacent cascaded wafers. Coupling between arrays may be accomplished using optical interconnections, although electronic connections may be adequate for this purpose. The resulting system completely interconnects a three-dimensional array with minimum latency.

Conclusions

A proposed optical communications network based on a planar broadcast medium is capable of providing high-capacity, low-latency interconnections among elements of a two-dimensional wafer-scale array without the need for optical alignments. Such a network operating in a single-channel time-division multiplexed mode might provide for all the communications needs of a multi-processor composed of many microprocessors on a single wafer. In combination with wavelength multiplexing techniques, this network provides access to optical bandwidths and offers the potential for dynamic reconfigurability through wavelength signal routing.

Acknowledgment

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Optoelectronic Shuffle/Exchange Network for Multiprocessor Architectures

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Abstract

A 3-D optoelectronic multistage shuffle/exchange concept is proposed. It provides low time skew and pipelined routing for a large 2-D array of processing elements.

Introduction

The perfect shuffle (PS) [1] is one of the most studied interconnection patterns for multiprocessor architectures. PS links are coupled to arrays of local 2x2 exchange/bypass switches to form shuffle/exchange networks. These networks perform arbitrary permutations of the elements in multistage interconnection networks for applications such as routing and sorting [2,3]. The PS of a 1-D array results by interleaving the elements of the first half of the array with those of the second half, with the first and last elements remaining unchanged in their position. For example, the PS of the 8 element array, {1,2,3,4,5,6,7,8}, is {1,5,2,6,3,7,4,8}. For a processing element (PE) array of size N, a single stage of a shuffle-exchange network contains a PS of size N followed by N/2 exchange/bypass units. Recently the sufficient number of stages required for an arbitrary permutation was proved to be no greater than 3log(N)-3 [4]. Therefore, the total number of active switches required in such permutation networks grows as Nlog(N). Thus, multistage permutation networks are appropriate for applications in which the number of elements is large enough to preclude the use of a crossbar switch, whose complexity would grow as N^2.

Implementing the PS interconnection in 2-D electronic technologies is difficult for large PE arrays. The communication requirements of the PS limit the useful array size and bandwidth of electronically implemented PSs due to time skew and coupling between signals as well as to the large amount of circuit real estate required for communication paths. To overcome these limitations, free-space optical versions of the PS have been proposed [5,6,7]. These optical PSs replace the physical electronic paths in a PS with free-space optical paths by combining imaging optical elements and simple shift variant optics to achieve the regular PS interlaced pattern.

Folded Perfect Shuffle

The Folded Perfect Shuffle [8] (FPS) was developed to take advantage of the natural 2-D input/output array format of optics, yet maintain the ability to effect the traditional 1-D PS pattern, with its simplest 2x2 exchange/bypass switch requirements. The key advantage of this approach is that the size of the PE array is not limited to the 1-D space-bandwidth product (SBWP) of the optical system, but by the 2-D SBWP. For example, a 1-D optical implementation of a 1024 node PS would require a very stringent optical design with a SBWP product of ~1024, whereas the folded PS implementation would require an optical system with SBWPs of only

~32 along each dimension -- a much more tractable criterion.

The FPS approach is based on encoding the 1-D array of nodes into a rastered or folded 2-D array, as shown in Figure 1. The optical system required to implement the FPS pattern consists of four appropriately positioned imaging lenses that magnify and overlap the four quadrants of the folded input array. Proper registration and interlacing of the overlapped quadrants can be achieved by demagnifying and skewing the input array, shown schematically as a spatial encoding input mask. If the input array is considered to be made up of "point source" elements, the required interlacing can also be accomplished via a skew of the four imaging lenses with respect to one another [9], thereby formatting the input and output arrays on rectilinear grids. Figure 1 shows the input and output PE locations of the FPS for N = 16. The output array is a rastered PS of the input array, identically formatted, but inverted by the imaging system.

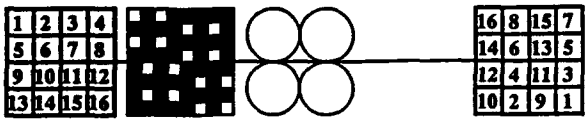


Figure 1. Basic Folded Perfect Shuffle Concept (exploded view).

Coupling the FPS to Exchange/bypass Switches

For many multiprocessor applications, the PEs will be electronic, necessitating optoelectronic interfaces between the array and the FPS network. With appropriate folding optics, the FPS can interconnect PE arrays located in the same physical plane, through electronic exchange/bypass switches also located in the PE plane. Several configurations are possible to achieve the required routing of the shuffled array. Figure 2 depicts one approach which requires that the array of sources be all aligned in polarization. The source array is imaged, through polarizing beam splitters onto a mirror plane, where two passes through a quarter-wave plate rotate the polarization and pass it through the FPS optics, via the polarizing beam splitters and folding optics, back to the array. The PEs are arrayed on a 2-D rectilinear grid. The optical FPS network performs a FPS operation on the output source array and folds the result back onto the input detector array -- essentially shuffling the array back onto itself. Electronic exchange/bypass switches, located between pairs of PEs, switch the signals according to control signals and route the signals either back to the emitter array, and to the next FPS stage, or to the PEs after the multistage routing is completed. Figure 3 is a top view of the optical folding network which shows some of the ray paths for the top row of an 64 element FPS interconnection in the network of Figure 2.

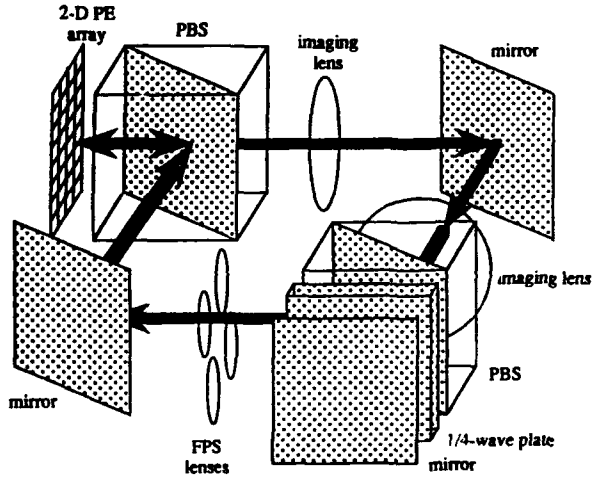


Figure 2. 3-D View of Proposed Network.

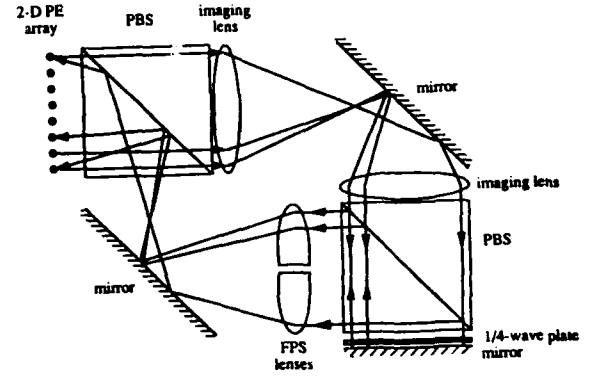


Figure 3. Top View of Proposed Network.

Only one source and detector for each PE as well as one exchange/bypass switch for each pair of PEs are required for applications

in which the multistage shuffle/exchange can be implemented using a single physical stage, with looping back of the signals to synthesize a multistage switch. The optical FPS imaging system can be configured to shuffle the source array onto a corresponding detector array, slightly displaced from the source array, as depicted in Figure 4. Each PE will require local intermediate storage to hold data segments as they pass through each stage of the network. Each PE will also require appropriate opto-electronic interface circuitry, such as multiplexers, demultiplexers, and amplifiers. If a self-routing or packet switching scheme is employed, each PE will require decoding circuitry as well.

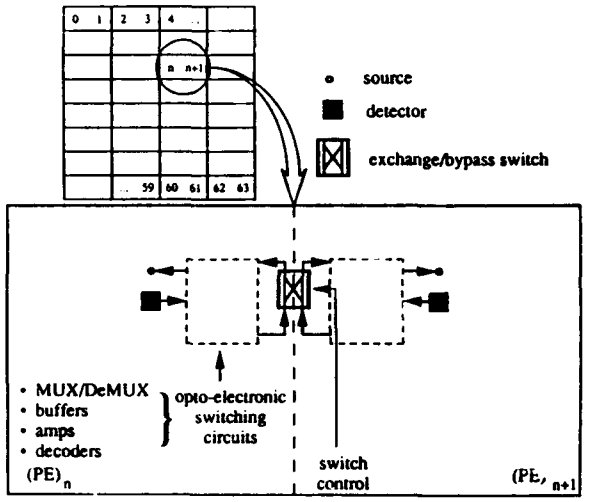


Figure 4. PE Plane for Non-pipelined Stages.

Pipelined Network

A key feature of this opto-electronic shuffle/exchange concept is the potentially large 2-D space-bandwidth product (SBWP) of the optical system, with respect to the number of PEs in the array. For multiprocessor architectures in which N is a few thousand or less, the latency of the multistage network can be dramatically reduced by configuring it as a pipeline. Figure 5 is an example schematic of a PE I/O layout required to implement a multistage pipelined permutation network. For each stage of the network, a source/detector pair is required at each PE site as well as an exchange/bypass switch for each pair of PEs. The sources and detectors can be arrayed in an interleaved fashion as shown in the figure for M = 4 stages. Since the FPS optical system achieves the FPS interlacing by magnifying by a factor of two, the source array at each PE site will be a factor of two smaller than the detector array, as shown in the figure. The resulting network consists, therefore, of M interleaved FPSs connecting interlaced but distinct arrays of sources and detectors at the PE plane. As the signals propagate through a stage of the network, the exchange/bypass switches pass the detected signals from one stage onto the spatially displaced emitters of the next stage. At the final stage, the data are fed out of the routing network and into the PE.

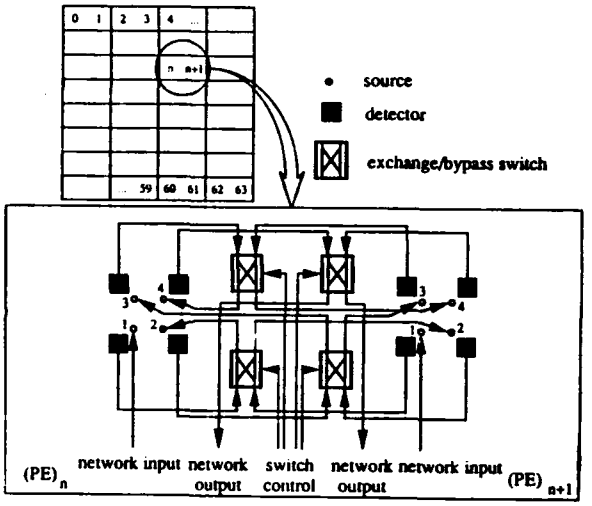


Figure 5. PE Plane for Pipelined Stages.

The pipelined network is achieved by using a single optical arrangement for the FPS routing. This is made possible by the low utilization of the optical SBWP product, for any single stage, for PE arrays of moderate size (N~1024). Since the number of stages required for an arbitrary permutation network grows only as log(N), the total SBWP requirement for the pipelined shuffle/exchange network will grow only as Nlog(N). Here the SBWP for the FPS optical system is defined as the optical blur spot size divided by the total area of the PE array. Each of the four FPS imaging lenses must meet the SBWP criterion. Obviously, the alignment and registration tolerances of the source and detector arrays must be sufficient to fully utilize the SBWP product of the optics. This SBWP can be fully utilized only if the opto-electronic elements can be placed

anywhere within the particular PE boundary that they serve. This implies that the digital processing components of the PE will be interspersed between the sources and detectors. If the Opto-electronic Integrated Circuit (OEIC) designer does not have the flexibility to place optoelectronic elements in any location, then the lower bound on the FPS optical SBWP requirements will be increased by a factor $1/\eta$, where η is the fraction of PE area allowed to contain optoelectronic I/O elements. As an example, for a network capable of arbitrary permutations on an N=1024 array, the optical SBWP must be greater than $3N\log(N)/\eta$. For η=.5, the optical SBWP must be greater than approximately 250×250.

Assuming high-bandwidth sources and detectors, the data rate and network reconfiguration time will be determined by electronic switch speed limits. The limiting latency in the network will be due to the round trip delay of the optical signals in the FPS optics. For a PE array that is several inches on a side, a reasonable FPS optical system will be approximately 1 foot in length. Accounting for the return trip through the folded optical system leads to a latency estimate of about 2 nanoseconds per stage. Since the FPS imaging optics are not telecentric, there is a variation in interstage path lengths across the elements of the shuffled array. The largest difference is between the first or last element in the array (which gets shuffled to itself in the optics) and a PE located near the center of a quadrant (which will have the shortest optical path length through the FPS system). The path differences will manifest themselves as time skews between PEs, and must be corrected for synchronous operation. For an array that is several inches across, the worst case time skew is about 50 picoseconds, with a FPS optical system that is about a foot in length. For longer optical systems, the time skew will be less -- there is a direct tradeoff, therefore, between latency/stage and skew/stage in the FPS system.

Table 1 summarizes the estimated performance capabilities of the proposed opto-electronic shuffle/exchange network, as limited by the optics. Clearly, current capabilities in the integration of opto-electronics and digital IC technologies are insufficient to exploit the advantages of the FPS. A major underlying assumption of this paper is, therefore, that OEIC technology will develop to a level where sources and detectors designed for free-space operation can be reliably integrated with digital electronics on a large scale. When this becomes a reality, the shuffle/exchange concept outlined in this paper will be able to significantly exploit the advantages of optical interconnects for multiprocessor architectures.

Table 1. Estimated Performance of Folded Optoelectronic Shuffle/Exchange Network

Number of PEs, N		>1024
Latency per stage		~2 nsec
Skew per stage		~50 psec
Optical SBWP requirements		
- non-pipelined:		> N
- pipelined:	arb. permutation	> $3N(\log N)/\eta$
	sorting	> $N(\log^2 N)/\eta$

Acknowledgments

Several useful discussions with J. J. Levy and R. A. Athale are gratefully acknowledged.

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Two-Dimensional Reconfigurable Interconnect in a Planar Optics Configuration

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Abstract

An experiment is described which shows the feasibility of combining a liquid crystal light valve beam deflector with a holographic lenslet array in a solid optics configuration.

Introduction

The constraining of an optical beam within a block using total internal reflection (TIR) offers a number of advantages for optical system construction, namely: modularity; compactness; mechanical stability; lack of turbulence; and reduced number of interfaces. The optical devices are placed on the surface of the block at the spots of TIR, and index-matched to the block. If the sources are similarly mounted, then there is the potential to define the whole arrangement of devices on one face of the block with microlithographic precision. Because of the power of this concept for optical computing, a special term has been coined, "three-dimensional planar optics" [1].

One important optical element for the practical realisation of this concept is the off-axis lenslet array with short focal length. This permits the interfacing of a planar source array, emitting normal to the plane, to a substrate mode which propagates by TIR along the substrate. It is functionally equivalent to the prism/or grating coupler in 2-D integrated optics. Moreover, when placed at the output, it allows increased receiver aperture without increasing the area of the receiver itself. We have fabricated holographic lenslet arrays of 390 μm focal length in 100 x 100 formats [2].

The optical devices, placed between the input and the output at the spots of TIR of the substrate beam, should either work off-axis (Fig.1), or be interfaced with components of a similar nature. For this study, we have chosen a device which works off-axis, namely a smectic liquid crystal light valve (LCLV) [3]. A grating written on the LCLV will deflect the substrate mode beam. The methodology for programming such a beam deflection device using an electrically addressed SLM has been demonstrated in a free space configuration [4]. The writing of spatially multiplexed gratings to such a device in order to deflect several beams simultaneously was not demonstrated at the time due to the lack of a memory effect in the liquid crystal layer. However, bistable ferroelectric liquid crystal light valves have since been fabricated [5], which would, in principle, allow the time sequential writing of gratings.

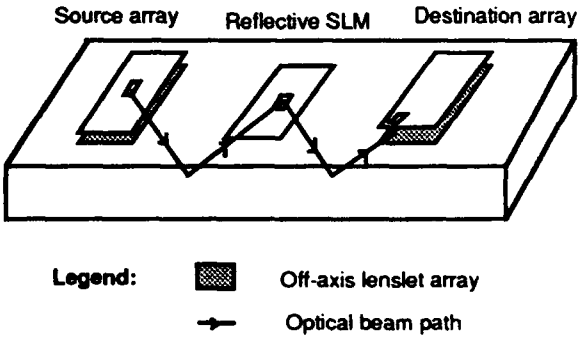


Figure 1. Schematic diagram of 2D reconfigurable interconnect.

Applications

The application areas for 3D planar optics are numerous and widespread. In this discussion we highlight two examples from the more restricted applications for space variant interconnect. Int the first place, we consider programmable N x N circuit switches for multicomputer and telecomms interconnects. In the second place, we deal briefly with the separate cases of fixed and programmable fan-out elements for neural networks. In the circuit switch application, the salient advantage of the beam deflector configuration is that the link insertion loss is independent of the parallelism of the interconnection network [4]. This is important when compared with other optoelectronic switching options such as the matrix-vector-multiplier optical crossbar, where the losses scale at least linearly with the number of links, and commonly are quadratic in the number. Such quadratic losses will impact system performance for 32-way computer links at 100 MHz [6]. With improved devices and system design, this upper bound may be improved, probably to 64-way links at 1 GHz. However, higher levels of parallelism should be foreseen. Moreover, a second advantage of the beam deflector compared with this option, is the facility of the planar optics configuration for imaging arrangements, compared with anamorphic beam expansion. With regard to telecomms traffic where the parallelism is higher, but the data rate is lower, link loss is also an important consideration. Also of relevance is whether a convenient scheme can be devised for interfacing the lenslet array directly to fibre, albeit the NA's of the lenslets would have to be reduced for efficient coupling.

With regard to neural networks, the system loss is less of a consideration. Moreover, the layering of such networks conceptually fits in with the possibilities for modularisation in planar optics. For example, one module might act as one layer of the network, which is functionally composed of: a fan-out element; a space-variant weighting; a fan-in; and a non-linear thresholding. The modules, which are each a separate block with associated devices and optical elements, might be interfaced with one another to high precision using etching techniques. Therefore, a high connectivity can be maintained between the layers of the network, which is not possible with electronic implementations. For the fixed interconnection module, the fan-out and weighting are performed by a computer generated hologram, and the fan-in and thresholding are carried out by either an all-optical non-linear array or a smart SLM. For the programmable interconnection module, the fan-out and weighting would be carried out by a real-time holographic recording device.

Experimental details

The schematic arrangement of the experiment is shown in Fig.2.

The light source is an Ar laser which enters the glass block by a prism coupler. A convenient size for the block was 30 x 10 x 1 cm^3, which allowed a suitable spacing of the white light projection used to write the grating, and the stereo microscope used to view the focal plane pattern above the gelatin film. In addition, it allowed 25 cm beam path between the deflector and the hologram, so that a relatively large deflection distance was achieved at the hologram.

The LCLV was the same as that investigated in [3], namely a ferroelectric liquid crystal/ amorphous silicon photoconductor sandwich made by STC Technology Ltd.,UK. The thicknesses of both the liquid crystal and the amorphous silicon were about 2 μm. The off-axis performance of the ferroelectric liquid crystal is good up to quite large angles. The diffraction efficiency of a low spatial frequency grating written on this device is a few per cent. The theoretical maximum for a binary amplitude grating is 10%, but incomplete angular switching in the liquid crystal attenuates this by a further factor. It is anticipated that the new generation of bistable liquid crystal devices,which provide full angular switching, will show diffraction efficiency close to the theoretical maximum. This lenslet array has a focal plane about 2 mm above the surface of the photographic emulsion. The lenslets are on 100 μm centers, and accept beams at an angle of 45° ± 3° with about 5% diffraction efficiency. The recording is in bleached silver halide of thickness 7 μm, for which we would expect a typical diffraction efficiency of 20%. For layers of either dichromated gelatin or photopolymer, the typical efficiency would be higher than 60%. All the components were index matched to the glass block using paraffin, which was convenient for demonstration purposes because it does not dry. The beam from an Ar laser was focussed by a 40x microscope objective and

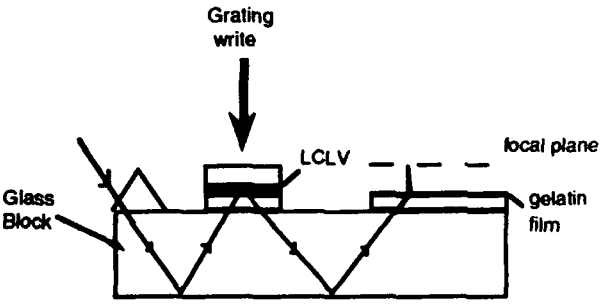


Figure 2. Schematic layout of components for beam deflector experiment.

imaged onto the lenslet array using a 160 mm focal length lens.

Results

When a 10 lp/mm grating is written on the LCLV, then two diffracted spots appear in the focal plane of the output lenslet array (Figs. 3(a) and 3(b)). These are the +1 and -1 diffracted orders of the substrate mode beam. The diffracted spots are displaced by about 10 lenslets from the central spot, and this in accord with the expected diffraction from a 10 lp/mm grating on the LCLV. The beam was weakly focussed on the lenslet array, and the spot size at the LCLV was about 1 mm. Due to the finite spot size and the overlapping nature of the lenslets in this particular hologram, the zero order spot consists of a number of spots. The first order spot consists of only one resolvable spot, and we assume that surrounding spots were below the threshold of the camera. In a practical arrangement (see Fig.1), the spot size would be smaller and the lenslets would not be overlapping.

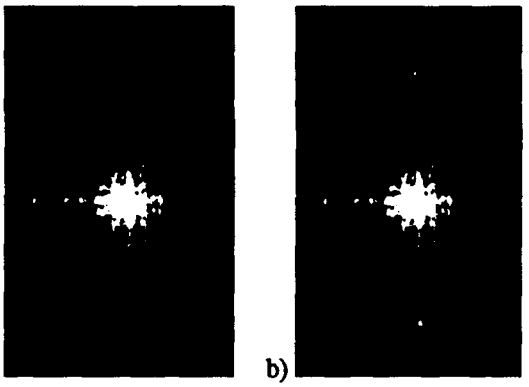


Figure 3. Focal plane array: a) without grating; b) with grating.

System analysis

Certain projections can be made for the applications to circuit switching and neural networks using this configuration. With regard to the circuit switch application, the resolution and total aperture of the light valve are critical parameters. The operating range of the grating beam deflector is between a minimum grating frequency and twice that frequency, so that higher diffraction orders do not introduce cross-talk [7]. In the same reference, a 1-D grating deflector has been analysed in the case where cross-talk limits the channel capacity. It is found that when the minimum grating frequency is 200 lp/mm and the aperture is 50 mm, then the maximum number of channels is 75. In order to increase the capacity to 100, one must either increase the min. grating frequency to 340 lp/mm or increase the aperture to 85 mm. In the 2-D case treated here, the channel capacity will be squared, but the resolution of the LCLV allows a minimum grating frequency of only 35 lp/mm. Therefore, the maximum channel capacity, extrapolating on the basis of this theory, is about 2000 channels.

In order to understand whether such a channel capacity might be maintained in a practical system, we estimate typical component values and then alignment tolerances. If the min. grating frequency is 35 lp/mm and we wish to have N distinguishable, equally spaced spots in the first diffracted order, then the aperture of the diffracting element should be N/35 mm. If we retain the overall SLM aperture of 50 mm used earlier, then we find that the overall channel capacity should be reduced to 1600, i.e. N=40. In order that the LCLV aperture does not increase the total deflection range required, a lens should be added between the LCLV and the microlens array. The destination array can now be made more compact. However, it would be beneficial to make the source array of similar dimensions as the LCLV, in order to reduce alignment sensitivity. For example, if the aperture of the lenslets is 1.3 mm, and their numerical aperture is commensurate with that of the source, say 0.2, then their focal length is 6.5 mm. The axial alignment tolerance of the sources can now be calculated for a channel capacity of 1600. The axial misalignment of the sources produces a beam divergence which should be sufficiently small that 40 times this divergence will be less than the total deflection angle available from the LCLV. In this case this allows a tolerance of 20 μm, which should be readily attainable. The tolerance along the planar axes is less critical because the positions and frequencies of the gratings recorded on the LCLV can be adjusted to accommodate small planar misalignments. The total deflection angle available from the LCLV at 850 nm is about 2°, so that the lenslet array should have this angular acceptance.

With regard to the fixed interconnect neural network application, the grating element performs the functions of fan-out and weighting. For example, we have fabricated uniform (unweighted) 1-D fan-out elements for a 1:9 fan-out with intensity variations of ±7% using a grating period of 500 μm [8]. We would expect variations of a similar order for a binary weighted fan-out, i.e. coding zeroes and ones. More levels can be conceived, but the number would be ultimately limited by the intensity variation. We intend to make a 2-D fan-out to avoid the loss in efficiency from cascading two 1-D elements. In order to ensure that the destination array is in the Fourier plane of the fan-out elements, a lens would be inserted between the array and the fan-out element.

Conclusions

The experiment shows the feasibility of building a ruggedised programmable beam deflector. The immediate potential of such a device can be approximately estimated from the system analysis. At the level of 64 channels the overall efficiency of the link compares favourably with a matrix-vector-multiplier approach with linear loss. In the latter case the efficiency can be no better than 1.6% because of the fan-out losses. In the present approach, if we were to use lenslet arrays of 60% efficiency, and a phase modulating light valve which gives a 5% efficiency at 50 lp/mm [9], then the overall efficiency would be nearly 2%. Furthermore, the extension of the space variant interconnect concept to the construction of modular fixed and programmable neural networks is indicated.

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Geometrical Analysis of 3-D Optical Interconnections

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Abstract

A geometrical approach to the numerical representation and analysis of 3-D optical interconnections and 3-D architectures is presented. The application to the algorithm and system design is discussed.

I. Introduction

In photonics systems the free space light beams for the interconnection of arrays are the important elements. Projective geometry deals with elements which are invariant with respect to a projection. These elements are points, lines and planes. The motivation for the ongoing work in this field is to study the utilization of the massive parallelism of digital optics on the algorithm level. For this purpose (amongst others) ideas are applied which have been suggested already one century ago by F. Klein (Erlanger Programm), J. Pfluecker and H. Grassmann [1].

The purpose of applying the presented framework is (at least) twofold. First, projective geometry is chosen because of its dual concepts (for each object, theorem and property a dual object, theorem and property exists) [2]. Second, after their transformation into Grassmannian spaces 3-D patterns and 3-D architectures may be represented by polytopes [3]. Hence, algorithms and techniques developed in computational geometry may be applied to the evaluation and analysis of optical interconnections and architectures [4]. Combinatorial algorithms are defined on polytopes with the solutions located at their vertices [5]. Therefore, the ideas and results of three strong and traditional fields may be utilized for photonics system research: Projective geometry, computational geometry and mathematical optimization techniques. But the present paper may be viewed only as a first step towards the solution of this class of problems.

II. Lines, Pencils and Bundles

The mathematical framework applied throughout this paper transforms lines into points and certain sets of lines (in the following called pencils and bundles) into lines (more precisely, into algebraic manifolds) on higher dimensional Grassmannian spaces. For the description of an arbitrary line in 3-D four parameters are needed. Therefore, the set of the real quadruples (x_0, x_1, x_2, x_3), indicated by P_3, is assumed for the definition set of 3-D optical interconnections.

Lines in 3-D interconnecting the points (x_0, x_1, x_2, x_3) and (y_0, y_1, y_2, y_3) are transformed into points

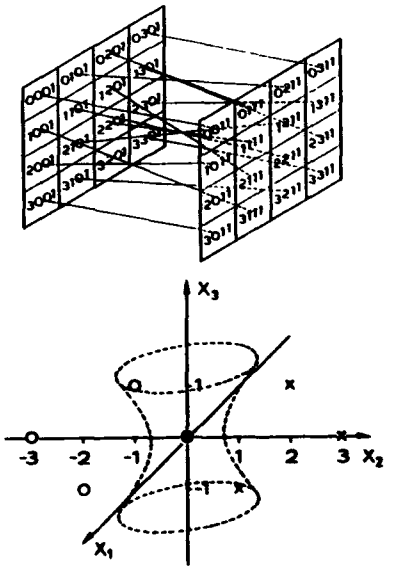


Figure 1. Definition of $S_{2-D}^{SGPS}(2,2;2,2)$ in P_3 (above). $S(2,2)$ shuffle (crosses) and unshuffle (circles) in $G_{3,1}$ (below). (SGPS for symmetric generalized perfect shuffle. The 3-D hyperbola represents symbolically the Pfluecker quadric. $G_{3,1}$ for the Grassmannian space of lines in P_3. $x_1 = x_4 = x_5 = 0, x_6 = -1$.)

on a 6-D hyperbolic quadric (Pfluecker quadric) by the bijection $x_iy_j - x_jy_i$ $(i \neq j = 0,1,2,3)$. To each point in $G_{3,1}$ a hyperbolic plane through zero exists being the dual geometric object of a line in 3-D. Lines which intersect lie on the same hyperbolic quadric and have a certain orientation assigned with zero. The orientation of all the other lines and hyperbolic planes is nonzero according to the evaluation of a polynomial of 2nd degree [6].

Similar, arbitrary lines in 4-D, 5-D etc. are transformed into higher dimensional Grassmannian spaces, in the following called $G_{n,1}$ $(n \geq 3)$. In particular, expressing lines in an n-dimensional space by the following scheme

$$\begin{pmatrix} x_0^{(0)} & x_1^{(0)} & x_2^{(0)} & \cdots & x_n^{(0)} \\ x_0^{(1)} & x_1^{(1)} & x_2^{(1)} & \cdots & x_n^{(1)} \end{pmatrix}$$

and forming $\begin{pmatrix} n+1 \\ 2 \end{pmatrix}$ different determinants of size 2×2 gives the Grassmannian coordinates (of 1st order). This bijection transforms lines from the projective space P_n into the Grassmannian space $G_{n,1}$. In contrast, the set of points in $G_{n,1}$ which lie on a hyperbolic quadric may be interpreted as the (Veronesian) space V_n^2 of the projective dimension $\begin{pmatrix} n+1 \\ 2 \end{pmatrix}$ -1. Thus, (at least) three different spaces and their relationships may be considered for the analysis and synthesis of 3-D interconnections and architectures (Fig. 2).

Grassmannian spaces carry a minimum point geometry but are nonlinear (except trivial cases) though linear subspaces may be constructed. Another advantage of $G_{n,1}$ is their relationship to the geometry of skew-symmetric matrices [2].

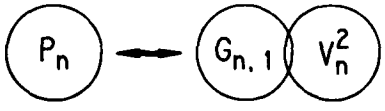


Figure 2. Spaces for the geometrical analysis.

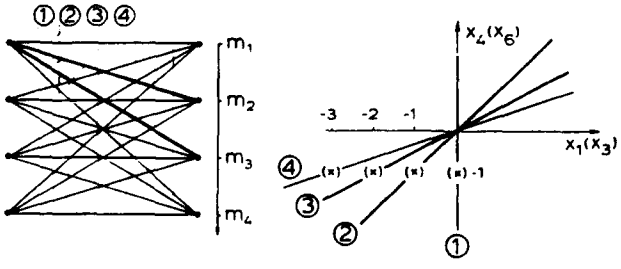


Figure 3. 2-D bipartite graph representing a planar multistage interconnection network (MIN) with four 4×4-switches (lhs). The 1st bundle (lhs) is transformed into four points (×) in $G_{3,1}$ with the coordinates (x_i). For this simple example the dual hyperplanes are the lines through the origin (m_i = 1 for i=1,2,3,4).

A bundle is a set of lines through a given point if (at least) any two lines lie in one plane. Another advantage of Grassmannian spaces is the mapping of bundles into lines (more precisely, into algebraic manifolds). The presented notation of a bundle simply corresponds to geometric ray optics. Throughout the present paper bundles are applied to model the edges of a node of a bipartite graph. [For the purpose of this paper a bipartite graph is the triple (V_1, V_2, E) where in the symmetric case $\mid V_1 \mid = \mid V_2 \mid$ (V for vertices, E for edges). A bipartite graph represents a MIN for the purpose of the decomposition of a given permutation.]

Bundles and lines may be combined representing (hyperbolic, elliptic and parabolic) nets [7]. The limit case of a parabolic net (all lines in parallel) is called a parabolic pencil. For the purpose of this paper a pencil is a set of lines within a plane and parallel to each other with equal orientation [8]. Therefore, a pencil is the proposed model for interconnections established by means of frequency division multiplexing techniques (FDM) and frequency conversion methods (FC) [9]. Pencils and bundles may be expressed by Pfluecker coordinates and evaluated numerically.

III. Cross Ratio and Projective Distance

Throughout the ongoing work projective transformations are applied for the design of algorithms and architectures of photonics systems. But in the projective space P_n no simple metric to measure distances exist [7]. Throughout the Erlanger program [1] the invariances between different geometries were analysed. An important invariance in projective geometry is the cross ratio (CR) originally expressing the ratio of distances between four points on a projective line [8]. In particular, given the points M_1, M_2, M_3 and M_4 with the coordinates $m_1 < m_2 < m_3 < m_4$, then the cross ratio is defined to be

$$CR(M_1M_2M_3M_4) = \frac{(m_3 - m_1)/(m_2 - m_1)}{(m_4 - m_3)/(m_4 - m_2)} \qquad (1)$$

and Eq.(1) may easily be generalized to any projective dimension [7]. The CR remains invariant with respect to any projective transformation in P_n as well as in $G_{n,1}$.

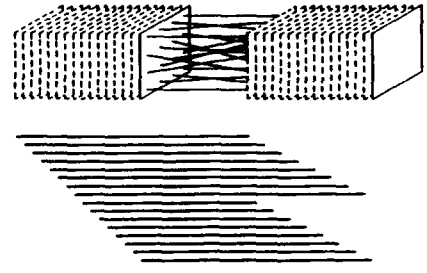


Figure 4. Interconnection of data in the frequency domain (above). $S_{3-D}^{NSGPS}(2,2;2,2;2,8)$ for the interconnection of two 4×4×4×16 data cubes (NSGPS for non-SGPS). Frequency pencil for the $S(2,8)$ pattern(below).

Eq.(1) corresponds with the Hilbert metric [10] expressing the distance between two lines inside a cone (cf. the 1st bundle on the lhs in Figure 3 and the bundle of lines in $G_{3,1}$ on the rhs) by applying the log-function to both sides of Eq.(1).

Eq.(1) is independent of the distance between the interconnected edges of a bipartite graph (the CR of distances between points on a projective line remains constant during any projection). By means of this measure we are able to evaluate the projective distance between bundles of lines in 3-D. But this quantity may also be applied to evaluate the distance between the corresponding points on a hyperbolic quadric. Thus, Eq.(1) and the addressed Hilbert metric may be applied to express the CR and the projective distance between bundles of hyperplanes in $G_{n,1}$. (A bundle of hyperplanes through the origin of $G_{n,1}$ is the dual object of a bundle of lines in P_n.)

IV. Polytopes

A polytope is simply a polygon in a d-dimensional space ($d \geq 3$). For the purpose of applying optimization techniques only bounded polytopes (BP) and their convex hull Conv(BP) will be considered. If the number of edges equals the dimension of the polytope the volume of a d-simplex (in 2-D it is a triangle, in 3-D it is a tetraeder etc.) may be evaluated analytically (all coordinates linearly independent) or numerically (dependent coordinates), respectively [11]. But the computation of the volume of an arbitrary polytope is a difficult problem [12].

Example : Throughout the paper the permutation P of the numbers 1,2,...,16 into the sequence 1,9,5,13,3,11,7,-15,2,10,6,14,4,12,8,16 will be considered.

For the ongoing work the vertices of the polytope (points in a Grassmannian space), their dual hyperplanes (which generate the dual polytope) and their relationships (collineation, correlation) are of interest. But for the final step (general photonic system design) the geometry of the polytope is also important. The geometry means edges, vertices, faces, facets, the height, diameter and paths of a polytope. The first four quantities constitute the Euler equation. But faces, facets, height and diameter of a polytope are also important for the solution of linear programming (LP) problems on convex polytopes [3].

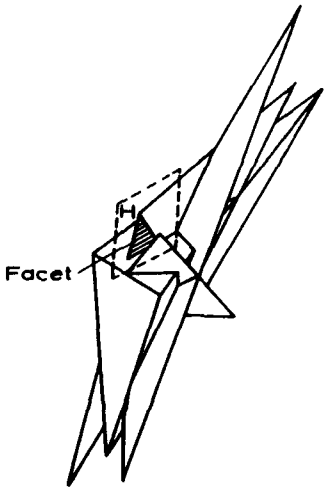


Figure 5. Polytope in $G_{3,1}$ representing the permutation P of the Example. [H is a supporting hyperplane defining a facet [5]. $x_3 = x_5 = x_6 = 0$.]

The existence of a polytope representing an interconnection pattern is assumed. Then the convex hull of the (vertices of a) polytope prescribes a (linear) system of inequalities

$$AX \leq B \tag{2}$$

which may be deduced from the coordinates of the edges by means of some linear algebra. For example, the convex domain in Fig. 1 (rhs) is bounded by $x_3 = -x_2+3, = x_2/2, = (x_2-3)/2$, and $= -x_2$ from which A and B may be deduced. Eq.(2) may be viewed as the constraint conditions of a LP problem [5]. The set of more than one row in Eq.(2) determines a volume which is called a halfspace (HS). A (non-trivial) face of P is determined by $F = P \cap HS$. A facet is a face of dimension d-1 (Fig. 5). The volume of a polytope may be expressed by

$$V(P) = \sum_k V(F_k). \tag{3}$$

whereby $V(F_k)$ is the volume of the k-th face [3].

V. Evaluation of Interconnections

Interpreting the coordinates of $G_{n,1}$ as the vertices of a polytope interconnected by undirected edges any regular and nonregular interconnection pattern may be represented by a d-dimensional polytope ($d = \binom{n+1}{2}$). Therefore, the evaluation of interconnections in Grassmannian spaces means the evaluation of the corresponding polytope. Several possibilities were considered:

(1) Quadratic forms (sum of squares of the coordinates)
(2) Absolute differences between the lengths of these vectors.
(3) Volume of the (convex) polytopes made up by the coordinates.

The quadratic form $\sum_i X_i^2$ is easily deduced from the equation for the Pfluecker quadric by appropriate substitutions [1] but it takes into account the contribution even of parallel arranged vectors. For N^2 interconnections the number of $N^2(N^2-1)/2$ differences have to be considered and this analysis may be extended to a statistical analysis of the absolute vector differences (Figs. 6 and 7). A small volume of the polytope (or a small difference between the vectors) expresses a local pattern whereas a large volume (difference) represents a global pattern [13].

The question arises about the most appropriate choice

of the free parameter (4th, 5th etc. coordinates). From the theoretical framework we know that the transformation of lines defined in P_n into $G_{n,1}$ is a bijection. Further, the kernel of $G_{n,1}$ is assumed to be zero iff n is an odd number which is a result of symplectic geometry [2]. (Kernel means the set of lines in P_3 which is mapped into the zero element in $G_{n,1}$.) From this we simply may conclude that the 4th, 5th etc. coordinate has to be chosen in a way to avoid equivalent coordinates in $G_{n,1}$ for different coordinates in P_n.

The next question arises whether the free parameter is able to carry architectural information or not. The presented analysis shows that for each distance between the arrays (3rd coordinate) there exists a global mimimum of the absolute vector difference (Fig. 6) and

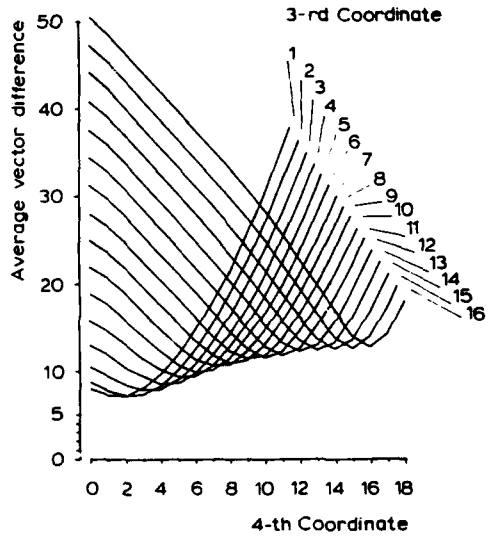


Figure 6. Average value of the absolute vector difference vs 4th coordinate for the interconnection of 8×8 (=64) data elements by $S_{2-D}^{SGPS}(2,4;2,4)$.

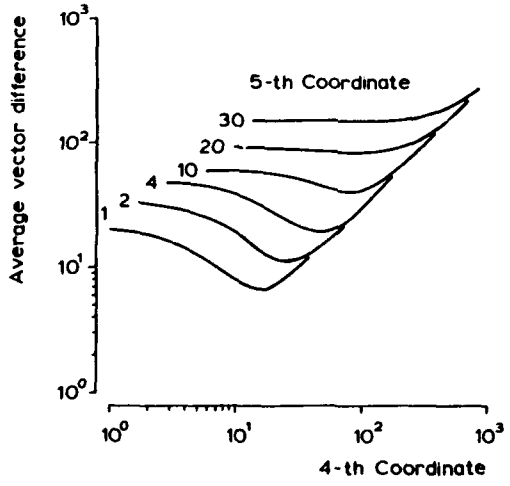


Figure 7. Average value of the absolute vector difference vs 4th coordinate for a distance of 8 units (3rd coordinate) and two free parameters (4th and 5th coordinate).

a similar behaviour is expected for other geometrical quantities of the polytope. Analysing the influence of additional free parameters (5th coordinate etc.) shows similar results. In particular, in a certain range (which depends on the other coordinates) the average vector difference has a global minimum with respect to the 5th etc. coordinate (Fig. 7).

VI. Decomposition of Permutations

Similar to the representation of regular and nonregular optical interconnections a given permutation may be transformed. For the distributed control of nonblocking MINs the requested permutation has to be decomposed into its reducible permutations and the binary numbering of the latter complements the tag for the self-routing scheme. Permutations are decomposed most successfully by coloring the bipartite graph which represents the MIN. There, the switches equal the vertices and the edges are the paths from an input switch to the corresponding output switch (Fig. 3 lhs).

If the bipartite graph is completely connected (all edges intersect) the whole system lies on a single quadric. Then instead of coloring the edges of a graph the two sets of points on the quadric (each representing the graph seen from the lhs and rhs, respectively) may be colored (Fig. 1). Further a path through a 3-D MIN is made up of intersecting lines which lie on a single quadric after their transformation. Therefore, the geometrical representation of a MIN by different polytopes for each stage and their analysis is of current interest.

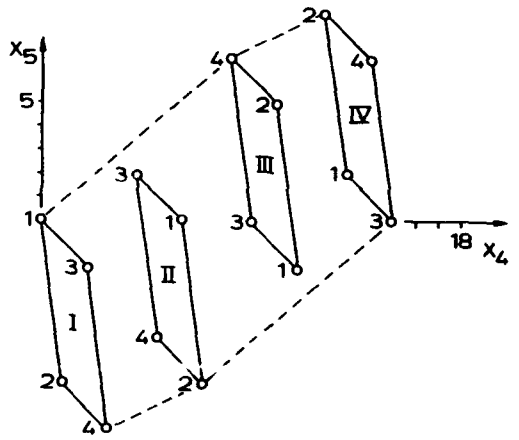


Figure 8. 2-D lay-out of the decomposition of permutation P. The (forward) polygon in Fig. 8 is generated by P seen from the lhs. An equivalent (backward) polygon is generated if P is seen from the rhs (Fig. 1). [The four rectangles represent the reducible permutations (I, II, III, and IV) and 1, 2, 3, and 4 means different colors. The convex hull is indicated by the dashed line. $x_1 = x_2 = x_3 = 0, x_6 = -1$.]

Algorithm:
Given a permutation of N^2 elements and a MIN with k×k-switches.
(1) Transform a permutation into $G_{n,1}$ according to a 2-D lay-out (Fig. 8) or a 3-D lay-out (Figs. 5 and 9).
(2) Subdivide the transformed permutation simply into k parts with N^2/k elements each [14].
(3) Start with an arbitrary coloring of the 1st permutation of the original (forward) polytope.
(4) Color the tranformed bipartite graph by interactive coloring the vertices of the forward and backward polytopes.

[The algorithm has to be applied to each of the reducible permutations in (2) until the MIN is homogeneous (equally sized switches).]

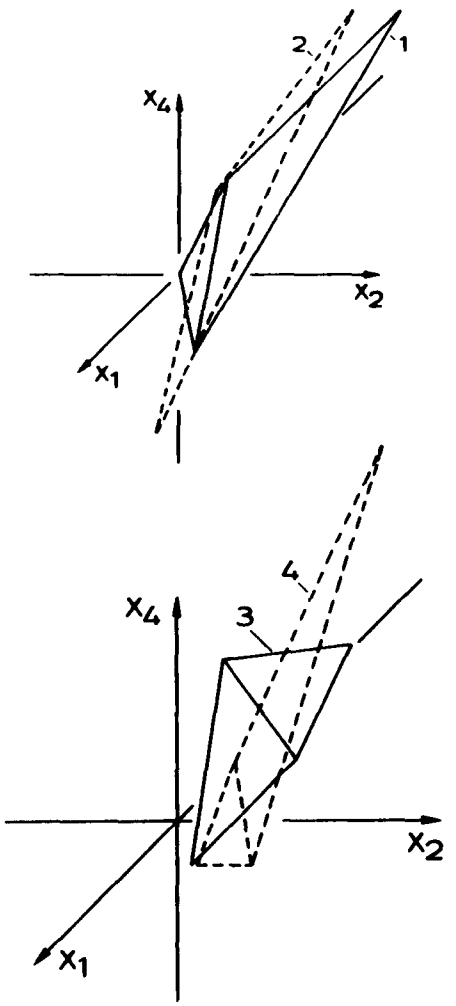


Figure 9. Decomposition of the permutation into (intersecting) 3-D polytopes representing the colored walks (1, 2, 3, and 4) through the complete polytope.

The final result represents colored walks through the polytope (Fig. 9). Several models are known (traveling salesman etc.) and their solutions have been presented [5].

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Microbeam Optical Interconnections Using Microlens Arrays

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Abstract

Free-space interconnection of widely spaced pixels may be implemented using microlenses, rather than conventional imaging. Advantages, problems, and studies of system capacity are discussed.

Introduction

Free-space optics offers a means of exploiting the large bandwidths of optical signals and the high densities of optical imaging[1]. Many of the free-space optical computing and switching systems proposed and constructed thus far have relied on conventional imaging using bulk lenses[2]. The optical systems in these experiments must provide large space bandwidth products (SBWP) since they offer high resolution over the entire image field.This is acceptable since a large fraction of the device array area is commonly used for optical I/O, due to fabrication[3] or cross talk issues[4]. However, in many applications, the percentage of the total area occupied by the optical I/O windows will decline as the amount of functionality per pixel is increased (e.g. "smart pixels" as in Fig. 1[5]). If the number of optical I/Os remains large, then the object and image fields provided by the lenses must grow. The requirement of high resolution across larger fields will continue to increase the cost and complexity of conventional optical solutions. Additionally, the increased field angles of the beams propagating between the lenses may introduce unwanted polarization effects at the polarization beam splitters and retarders.

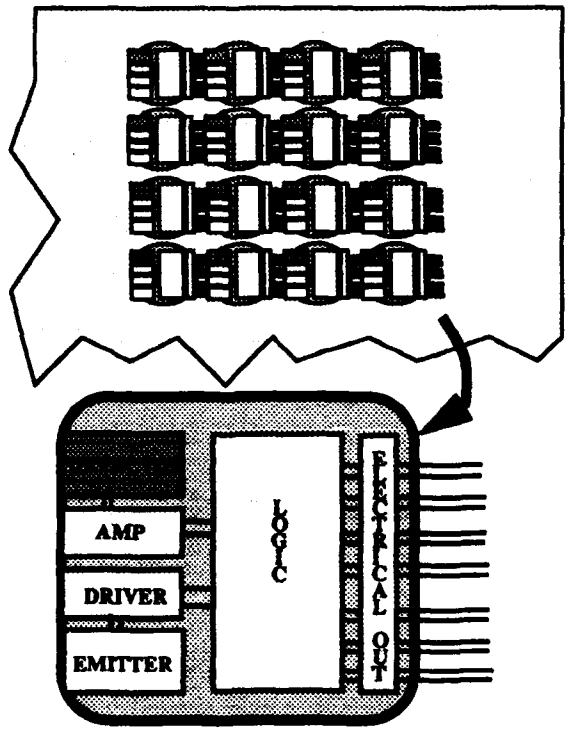


Figure 1. "Smart" pixels with optical/electrical I/O

Since the large SBWP of the bulk lenses is not being fully utilized in these applications, it seems reasonable to investigate means by which the required high resolution (<10 μm) can be supplied only at the optical I/O windows, or groups of windows. One means of doing this is to provide a separate optical relay system for each pixel, as shown in Fig. 2.

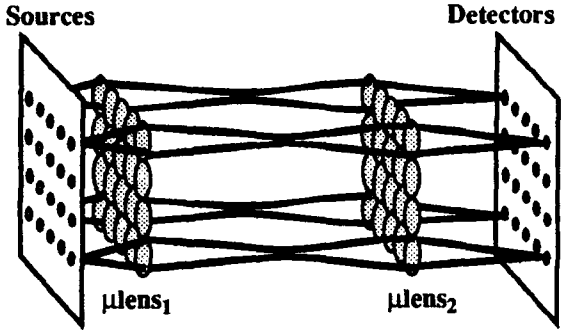


Figure 2. Microlens relay: simplest case.

These "micro-beam relay" systems have several attractive advantages. They may provide high resolution, but only at the sources and detectors, where the high resolution is required. Field dependent aberration contributions are negligible since each microlens images on-axis and only spherical aberration must be controlled. Fabrication of arrays of simple, (possibly aspheric) microlenses appears to be possible at low cost. The small diameters and short focal lengths of these microlenses may allow the design of compact optical systems. All of the "microbeams" propagate at the same angle, so angular effects at the polarizing beam splitters and retarders are no longer present. Finally, there also exists the potential for a high degree of parallelism. Thousands of parallel high speed connections could be supported in a volume less than that of a (1 inch)^3 beam splitter.

The use of microlens arrays for optical interconnections was proposed by Iga et al in 1982[6]. More recently there has been renewed interest in the use of microlens arrays for optical interconnection and switching[7-12]. Specific applications of microlenses include board-to-board optical interconnections, chip-to-chip or between multichip modules, planar or substrate-mode optical systems, space-variant facetted hologram interconnections, and 1-D and 2-D fiber array interconnection.

In this paper, we investigate these "connection capacity" issues for a microlens systems supporting thousands of high speed (500 Mbps) channels. Fundamental to this study is the fact that practical system designs must incorporate mechanical and optical tolerancing data. We will assume that the signal sources emit (or modulate) coherent light with a Gaussian intensity profile at a wavelength of 850nm. Such sources might include SEED-type modulators or surface emitting microlasers. We will also assume that two-dimensional arrays (of size NxN) of sources and detectors will be used. We wish to maximize the linear number of channels, N, under the assumption that the maximum area of the "smart pixel" chip is less than (20mm)^2. To support thousands of connections in this area, the microlens diameters will be less than about 500 μm, hence diffraction effects will be significant. Further practical considerations are that the detector and modulator/emitter areas must be minimized to allow high speed operation with low power dissipation and/or lasing thresholds. Similar arguments apply to the minimization of power loss. To simplify this initial analysis, we will assume that the emitter/modulator and detector areas are identical and that the microlenses may be approximated by ideal thin lenses. Thick lens and aberration effects will be the subject of a later study.

The effects of diffraction on the system size and performance have not been extensively explored. Diffraction effects are significant since their presence introduces power loss, crosstalk, and (in some schemes) coherent artifact noise. The minimization of diffraction effects can greatly impact the total number of channels supported in a given volume, and especially the system's optical and mechanical tolerances.

Microlens Relaying of Gaussian Microbeams

A Gaussian beam propagation model[13] is illustrated in Fig. 3. This figure illustrates the symmetric relay case, where ideally $z_1=z_4$, $z_2=z_3$, and $f_1=f_3$. The divergence of the Gaussian beams may be expressed in terms of the beam irradiance e^{-2} radius;

$$w(z)^2 = w_0^2 \left(1 + (z/z_R)^2 \right),$$

where z is the propagation distance, w_0 is the e^{-2} radius of the input waist, and

$$z_R = Rayleigh\ Range = \pi w_0^2 / \lambda$$

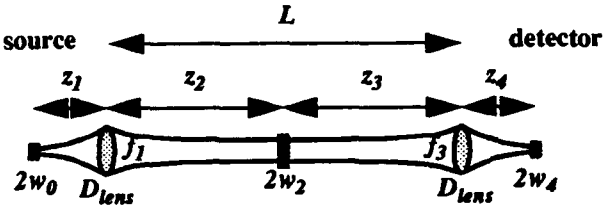
The distance to, and size of the intermediate waist, w_2, can be expressed in terms of the magnification factor, α:

$$z_2 = f + \alpha^2 (z_1 - f)$$

$$w_2 = \alpha\, w_0$$

where $\alpha = w_2/w_0 = |f| / \sqrt{\{ (z_1 - f)^2 + z_R^2 \}}$.

The diameter of the microlens is determined by the divergence of the source radiation, the source to microlens distance, z_1, and the desired amount of clipping of the Gaussian beam at the microlens. This amount is expressed by the clipping ratio,



f = microlens focal length
z = waist to microlens distance
D_{lens} = microlens diameter
$2w$ = waist diameter at e^{-2} points

Figure 3. Gaussian beam relay by thin lenses.

k = *clipping ratio* = $D_{lens} / 2w_{lens}$

where $w_{lens} = w(z_1)$, and the power loss for several clipping ratios is shown in Fig. 4. Note that when k=1.52, or D_{lens}=3w_{lens} only 1% of the beam power is lost, and that when k=2.12, only 0.1% of the power is lost. Clipping thus causes power loss which can lead to crosstalk between channels, but it also can have dramatic effects on the basic function of relaying the waist of the emitter/modulator to the detector. As shown in Fig. 5, clipping by the lens can cause the relayed waist's position and size to be changed from that predicted for an infinite lens (no clipping). The diffraction effects caused clipping at the microlens aperture can be viewed as an effective change in the input waist radius, w_0^{eff}[14].

This change in the effective input waist radius changes the size and location of the intermediate waist, w_2. The amount of change can be quite significant, even for small amounts of clipping, as shown in Fig. 6. These changes also have a large impact on the "first order" design of these microlens systems and for clipping ratios less than k=2.12, they should be taken into account. For clipping ratios greater than k=2.12, or 0.1% power loss, the diffraction effects are small, and may be ignored in this analysis.

$$w_0^{eff} = w_0 \left(1 - e^{-x^2/2} \cos[px^2/4\pi] \right)$$

where $p = 2\pi z_1 / z_R$, $x = (k)\sqrt{2} / w_{lens}$, and $k > 1$.

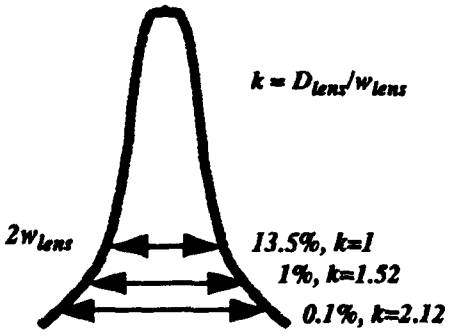


Figure 4. Clipping ratio, k, and energy loss.

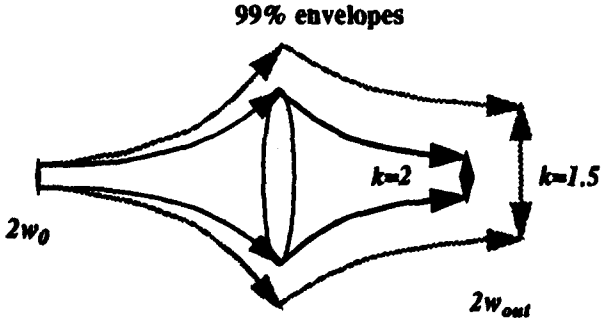


Figure 5. Effects of clipping on output waist.

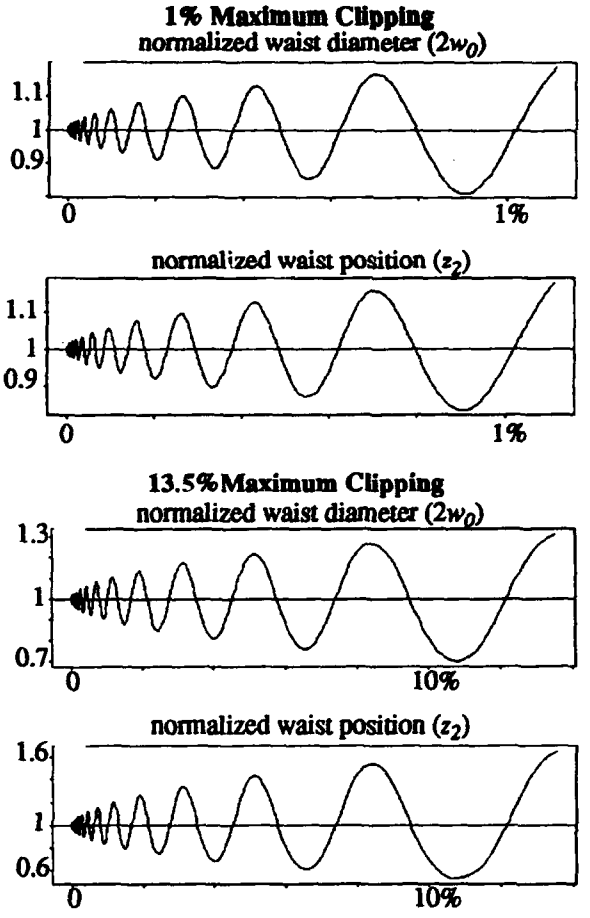


Figure 6. Intermediate waist size and position normalized to the unclipped size and position plotted against percentage of power clipped.

Connection Capacity

The design space for even the simple microlens system of Fig. 3 has six primary free parameters: the source waist radius, w_0, the microlens focal length, f, the source-to-microlens distance, z_1, the distance between microlenses, L, the acceptable clipping ratio, k, and the maximum number of channels that may be supported on the $(20mm)^2$ chip. In practice the design space includes more than just these six parameters, since the required alignment tolerances in three dimensions, for three of the four planes must also be taken into account. We can gain some analytical insight into this design problem by establishing the following constraints to minimize the number of free parameters, then using graphical techniques, investigate the trade-offs between the remaining free parameters.

We would like to maximize the distance, L, between the microlenses for most of the applications mentioned in the introduction. A minimum required propagation distance common to most of these applications is

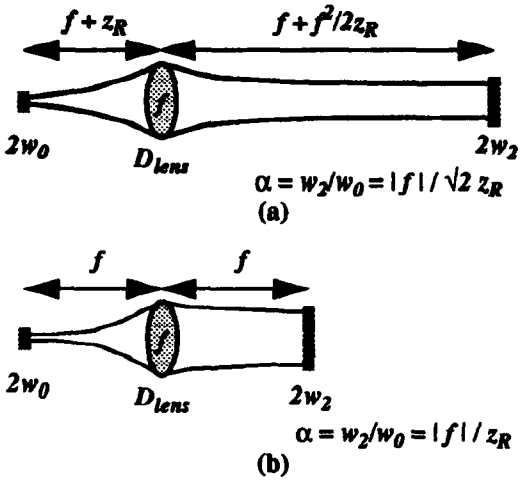


Figure 7. Gaussian beam "collimation":
(a) maximum lens-to-waist distance
(b) minimum divergence

$$L > ND_{lens}$$

or that the distance between microlenses be at least as large as the linear dimension of the chip. As will be shown in the next section, tolerancing arguements can justify the use of a clipping ratio of k=2.12, which fixes another parameter, but still leaves us 4 free variables. We can interrelate the variables z_1, f, and w_0 by examining two definitions for "collimation" of Gaussian beams. One definition of collimation (Fig. 7a) maximizes the distance between the lens and the intermediate waist, z_2, while the other definition (Fig. 7b) minimizes the divergence. These definitions define z_1 in terms of f and w_0, which allows the generation of plots such as those in Figs. 8 and 9. These plots show the maximum number of channels, f-number, and resultant chip dimension as a function of microlens focal length, for a range of source/detector sizes (specified as the 99% diameter, $3w_0$). The number of channels supported by the first collimator, within the $(20\text{mm})^2$ chip size limit, is maximized for small source sizes (≈10 μm 99% diameter), focal lengths (<1mm), and the microlens must be fairly fast (< F/3). The second collimator definition can support a similarly large number of channels using larger source sizes (≈150 μm 99% diameter), and focal lengths (10mm). Such large source sizes are less desirable, but the very slow (F/30) microlenses are attractive due to aberration and optomechanical tolerance considerations.

While this analysis can estimate the maximum channel capacity and performance of the microbeam relay system of Fig. 3, the realization of such a system will further require that the system has low loss and reasonable optomechanical tolerances. As an example of these tolerances, the next section discusses a relay system for the first collimation case, with k=2.12, 10μm source/detector diameters (99%), using f=868μm D_{lens}=313μm microlenses, and L=20mm, which supports 64x64 channels in a square matrix.

Optical and Mechanical Tolerancing

The microlens relay system of Fig. 2 has four element planes which must be aligned to one another in all three dimensions. The tolerancing of the example system described above was analyzed via a computer model which accounts for the clipping induced variations described earlier. The parameters w_0, z_1, f_1, L, f_3, D_{lens1}, and D_{lens3} were individually varied over +/- 10% of their nominal values. The corresponding percentage changes in output waist size and position (w_4 and z_4) were plotted(figure 10), along with the percentage change in the energy coupled into the 10μm detector. These plots provide some insight as to the critical

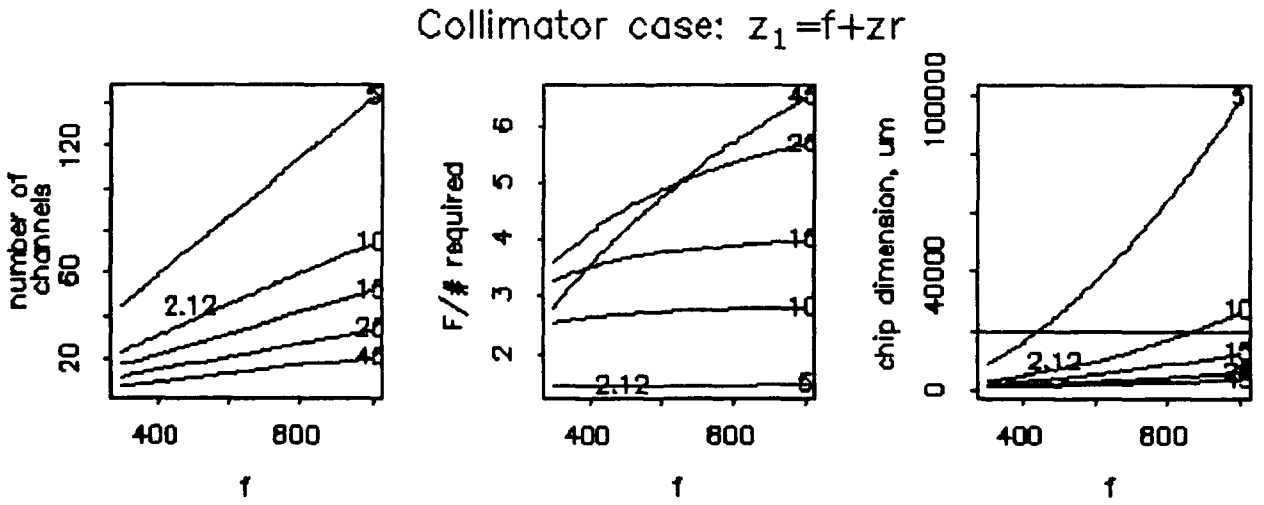


Figure 8. Linear number of channels supported, f-number, and resultant linear chip dimension versus focal length, for $3w_0$=5,10,15,25,45 μm, for the first collimator case.

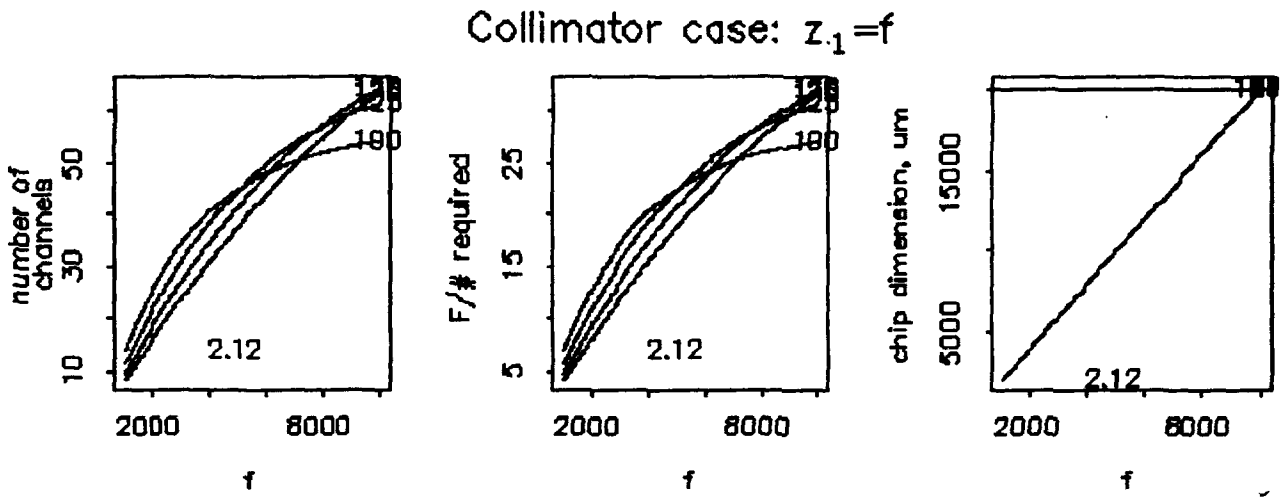


Figure 9. Linear number of channels supported, f-number, and resultant linear chip dimension versus focal length, for $3w_0$=100,125,150,175 μm, for the second collimator case

optomechanical tolerances in our example system. The changes induced by +/- 10% variations of w_0, D_{lens1}, and D_{lens3} were less than 5% and are not plotted. The more indirect effect of changing the design clipping ratio can be seen in Fig. 11, where a clipping ratio of 1.52 is used. For both the k=2.12 and the k=1.52 cases, the variables which impact the energy coupling the most are the source-to-microlens spacing, z_1, and the focal length of the second microlens, f_3. The change in clipping ratios represents only a 0.9% change in energy clipping at the microlenses, but it almost doubles the coupling sensitivity for these two variables. The sensitivity to variations in microlens focal length is disturbing, since the focal length variations of many refractive and holographic microlens arrays is typically 5-10%. Diffractive microlenses provide better uniformity. Fast diffractive lenses may be a source of polarization aberration when used with polarized beams.

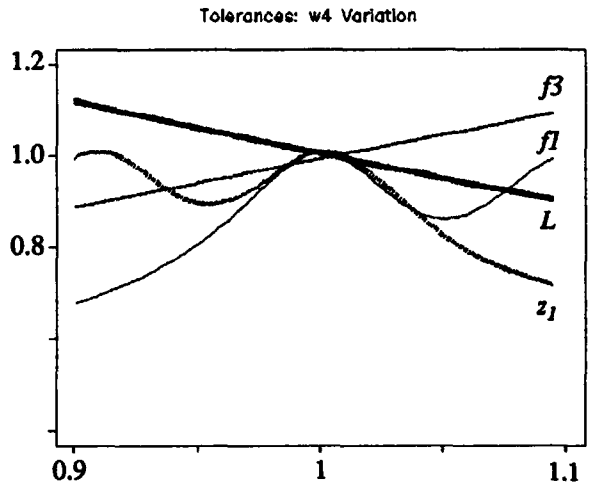
The tolerances at each element plane for an additional 10% loss over the nominal case are summarized in Table 1. Assuming the source array is fixed, the two microlens arrays and the detector array must be aligned relative to the source array. The large diameters and low divergence of the beams at the two microlens arrays result in the relatively loose tolerances in those planes, while the small beam sizes at the detector array result in tighter tolerances.

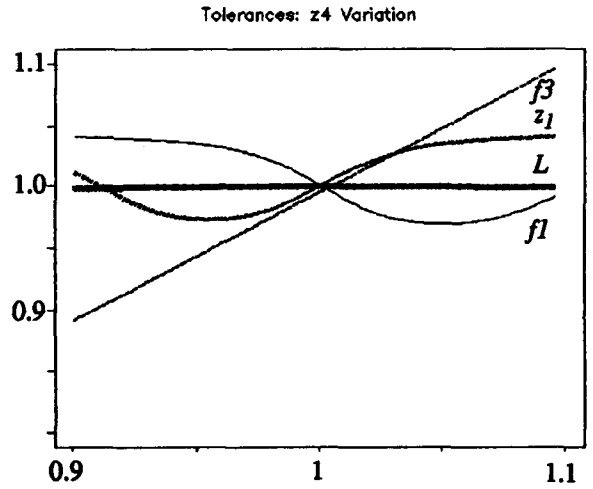
A significant amount of tolerancing work remains to be done. This current model only accounts for energy losses due to clipping at the microlenses and detector in the absence of aberrations. While this may be an accurate representation for some applications, most misalignments will also introduce aberration. For the symmetric system considered here, coma and distortion should cancel, and spherical aberration may be correctable by the use of aspheric microlenses. If diffractive microlenses are used, the Petzval sum will be also zero, leaving only astigmatism to correct. The small aperture and focal lengths of these lenses scale the magnitude of the aberrations and help the situation, but further modeling and experimentation will be necessary to evaluate the actual severity of this issue. Additionally, these misalignments will introduce lateral shifts in the beam positions relative to the microlenses and the detector. The current model only accounts for this clipping at individual microlens planes. Finally, the cumulative effects of several parameter variations should be modeled. The individual analysis done so far highlights the critical parameters, but does not identify any "balancing", or amplifying effects that may occur when the parameters are varied together, as they would be in a real system.

In contrast to conventional optical systems, the "first-order" design of these system can be complex. In bulk optical designs, the lens positioning generally must be constrained in x and y to sub-millimeter tolerance, in z to 10-100μm tolerance, and in tilt to arc minutes. For these small microlens systems, the overall tolerances appear more constrained, but not unreasonably so.

Conclusions

We present a study of the design issues for microlens array free-space optical interconnection systems. The effects of beam clipping have been studied and found to dramatically influence the design and tolerancing of microbeam interconnection systems. An example system capable of supporting over 4,000 parallel high speed channels is described and toleranced. System optical and mechanical tolerancing issues appear reasonable. Areas for further study include aberration accumulation, and cumulative alignment tolerancing.





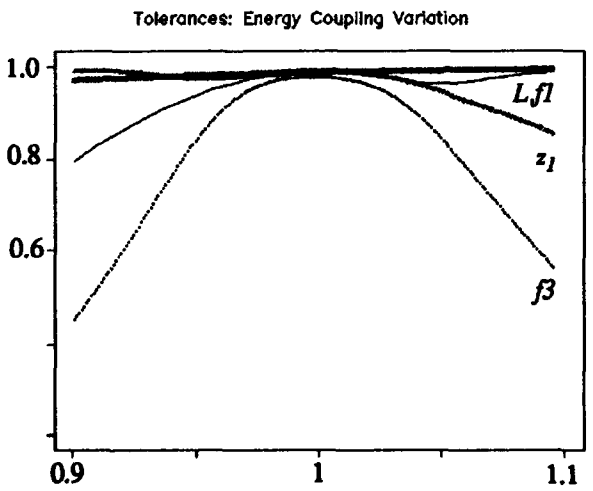
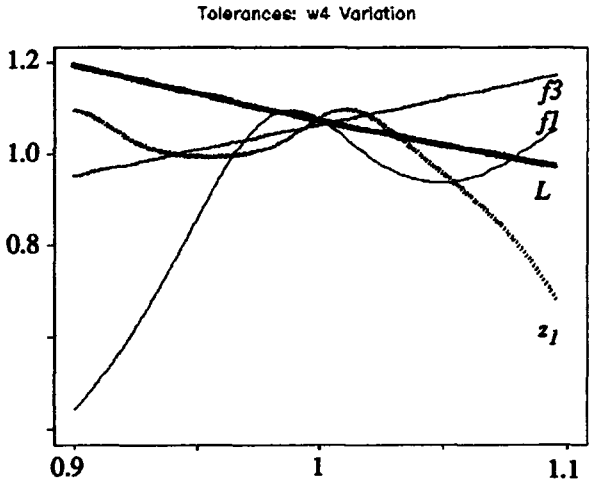
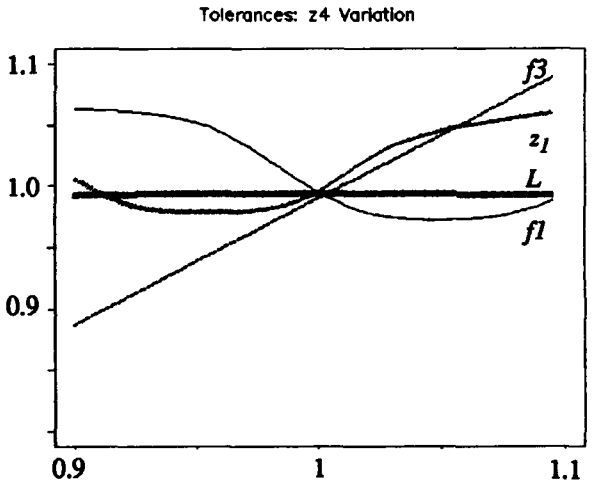


Figure 10. Optomechanical tolerances expressed as a relative change from the nominal case plotted against a +/- 10% change of system parameters, for a clipping ratio *of* k=2.12.





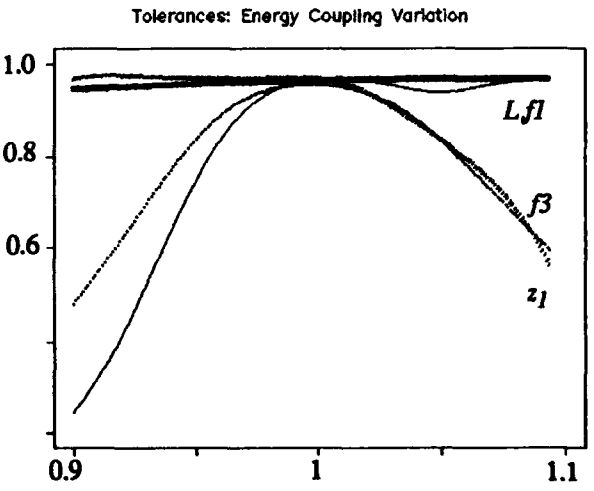


Figure 11. Optomechanical tolerances expressed as a relative change from the nominal case plotted against a +/- 10% change of system parameters, for a clipping ratio *of* k=1.52.

Table 1. Tolerances for additional 10% loss:

	Microlens1 Plane	**Microlens 2 Plane**	**Detector Plane**
	Beam diameter(99%) = 225μm, Lens diameter 313μm		*Beam diameter (99%) = 10μm, Detector size = 10μm*
Lateral displacement(2):-	**100μm**	**100μm**	**2.9μm**
Defocus:-	**64μm**	**~mm's**	**14μm**
64x64 on 313μm centers			
Rot. about optical axis:-	**25 arc minutes**	**25 arc minutes**	**44 arc seconds**
Tilts(2):-	**16 arc minutes**	**4.9 degrees**	**3.5 arc minutes**

Acknowledgments

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Time-Division Switching

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Ultrafast All-Optical Fiber Soliton Logic Gates

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Abstract

We demonstrate a cascadable soliton dragging NOR-gate with a switching energy of 5.8 pJ, a fan-out of six and a potential speed of 0.2 TBit/sec. This is one example of a novel time domain chirp switch architecture in which digital logic is based on time shift keying. We also show a hybrid switch consisting of a semiconductor waveguide followed by a polarization maintaining fiber, and we describe the application of a handful of these ultrafast gates to a 100 Gb/s soliton ring network.

The commonly accepted wisdom for all-optical switches is that a π-phase shift must be achieved through the interaction between two pulses in less than an absorption length. However, by changing to a time domain chirp switch architecture (TDCS) that is based on time shift keyed logic, we show that less than a $\pi/20$ phase shift is required from the nonlinear interaction, which leads to switching energies approaching one picojoule. We first describe a 5.8pJ switching energy, all-optical NOR-gate that is based on soliton dragging in fibers [1]. This three-terminal, cascadable gate satisfies all requirements for a clocked digital optical processor. We then elucidate the TDCS architecture and prove the mechanisms by demonstrating a hybrid version consisting of a semiconductor waveguide followed by a polarization maintaining fiber. Finally, we design a 100 Gb/s soliton ring network to illustrate the considerations in system applications of the ultrafast gates.

Soliton Dragging Logic Gates

The all-fiber logic gate operates based on time shifts from soliton dragging in a clocked digital system. In time shift keying a "1" corresponds to a pulse that arrives within the clock window and a "0" either to no pulse or an improperly timed pulse. In soliton dragging two temporally coincident, orthogonally polarized pulses interact in the fiber through cross-phase modulation [2] and shift each others velocities. The velocity shift converts into a time shift after propagating some distance in the fiber. For the NOR-gate the fiber length is trimmed so that in the absence of any signal the power supply or control pulse C arrives within the clock window and corresponds to a "1". When either or both signals are incident, they interact with the control pulse through soliton dragging and pull C out of the clock time window.

The insert in Fig. 1 shows a schematic of the NOR-gate that consists of two birefringent fibers connected through a polarizing beam splitter with the output filtered by a polarizer. The control pulse C, which provides gain and logic level restoration, propagates along one principal axis in both fibers and corresponds to A NOR B at the output. The two signal pulses A and B are polarized orthogonal to C and are blocked by the polarizer at the output. The signals are timed so that A and C coincide at the input to the first fiber and B and C coincide (in the absence of A) at the input to the second fiber.

Figure 1 shows the experimental apparatus for testing a single NOR-gate. We obtain $\tau\sim$ 500fsec pulses near 1.685μm from a passively mode locked NaCl color center laser in which a 2mm thick quartz birefringent plate limits the bandwidth and, thus, intentionally broadens the pulses [3]. The input stage separates the control C, signals A and B, and clock beams, and stepper motor delay stages are used to time properly signal B and the clock. The two fibers are 75m and 350m long, have a polarization dispersion of about 80psec/km, and exhibit a polarization extinction ratio better than 14:1. The control pulse output and the clock are directed to a correlator to measure the time shifts.

The correlation of the clock with the NOR-gate output is illustrated in Fig. 2. The dotted box corresponds to the clock window, and we see that C arrives within this window when no signal is present. When A=1 or B=1, C shifts between 2 to 3 psec out of the clock window; the shift from A is larger since C can time shift in both fibers. When A=B=1, C shifts by about 4psec. In this example the signal energies are 5.8pJ each and the fanout or gain (control out / signal in) is six. The control pulse energy in the first fiber is 54pJ and is reduced to 35pJ in the second fiber because of coupling losses.

To prove the cascadability and fan-out of the logic gate, we implemented an all-optical multivibrator or ring oscillator by connecting the NOR-gate as an inverter and feeding the output back to the input (A = 0, B = previous output from gate). We placed a 50:50 beam splitter at the output and sent half of the output through a delay line to the B input. The correlator was set to the center of the clock time window. As Fig. 3 shows, with the feedback blocked the output is a string of 1's. When the feedback is added, the output becomes an alternating train of 1's and 0's whose period is twice the fiber latency (1.75 μsec).

Time Domain Chirp Switch Architecture

Soliton dragging logic gates are one example of the more general TDCS architecture that is applicable to materials other than fibers. As shown in Fig. 4, the TDCS consists of a nonlinear chirper followed by a soliton dispersive delay line and has two orthogonally polarized inputs. In the absence of a signal pulse, the control pulse propagates through both sections and arrives at the output within the clock window. For a cascadable switch the self-induced chirps on the control in both sections must balance, and the output pulse must resemble the input. Adding the signal pulse creates a time varying index change that chirps the control pulse and shifts its center frequency [2]. Then, as the control pulse propagates through the soliton dispersive delay line, the frequency shift is translated into a time change. Since a fundamental soliton acts as a particle, even a slight shift in the center frequency can cause the complete soliton to shift in time, which results in good contrast within the clock window. Furthermore, since the chirps from group velocity dispersion and nonlinearity are balanced for a soliton, cascadability can be satisfied by using solitons.

The key feature of TDCS is that for high-bit rate, short pulse applications the TDCS requires less nonlinear interaction and, consequently, less switching energy than other all-optical switches. For example, a Mach-Zehnder interferometer requires a π-phase shift from the interaction, whereas by using solitons in a TDCS we find that the nonlinear interaction in our demonstrated switch is less than $\pi/20$ [4]. Because solitons shift as a unit, solitons permit the effect in the nonlinear chirper to be accumulated through the entire length of the dispersive delay line. The trade-off is that TDCS have a long latency, which restricts their usage to feed-forward applications. As a proof of principle, we demonstrated a soliton dragging logic gate with a switching energy of 1 pJ and a fan-out of 28. In this experiment the nonlinear chirper was 30 m of moderately birefringent fiber ($\Delta n\sim 10^{-5}$) and the dispersive delay line was 2 km of polarization maintaining fiber [5].

To confirm the mechanisms in the TDCS architecture, we implemented a hybrid TDCS in which the nonlinear chirper is a 2.1 mm AlGaAs waveguide and the dispersive delay line is a 600 m polarization maintaining soliton fiber. We use the instantaneous nonlinear index change in AlGaAs near 1.7 μm, which is in a wavelength range below the two photon absorption edge. In this wavelength range we find that $n_2 \sim 3\times 10^{-14}\text{cm}^2/\text{W}$ and that the material is isotropic (e.g. cross-phase modulation is two-thirds of self-phase modulation). We obtain a π-phase shift from self-phase modulation with less than a 10% absorption, and we find that the nonlinear absorption originates primarily from three photon absorption. Furthermore, time resolved pump-probe measurements confirm that the nonlinearity is instantaneous on the 500 fs time scale of the pulses.

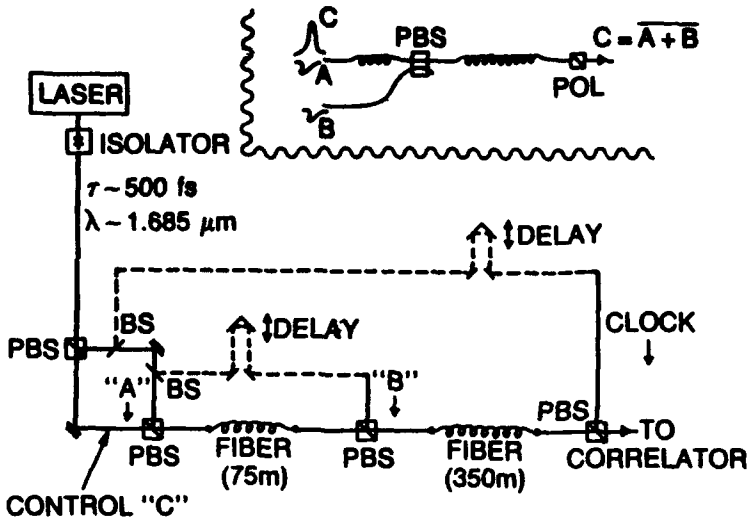


Fig. 1. Experimental configuration for testing an all-optical NOR-gate. The insert shows a simplified schematic of the NOR-gate.

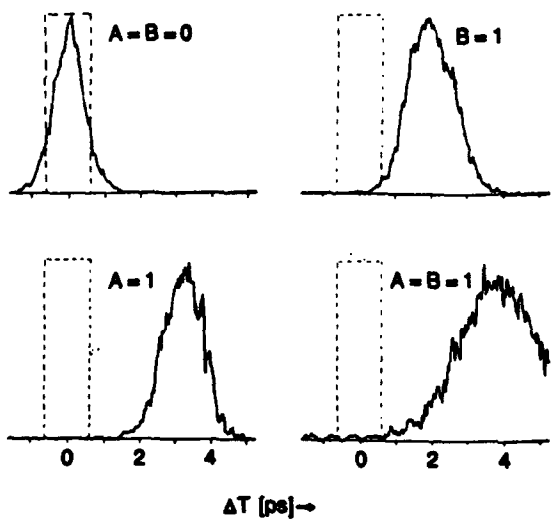


Fig. 2. Correlation of the NOR-Gate output with the clock.

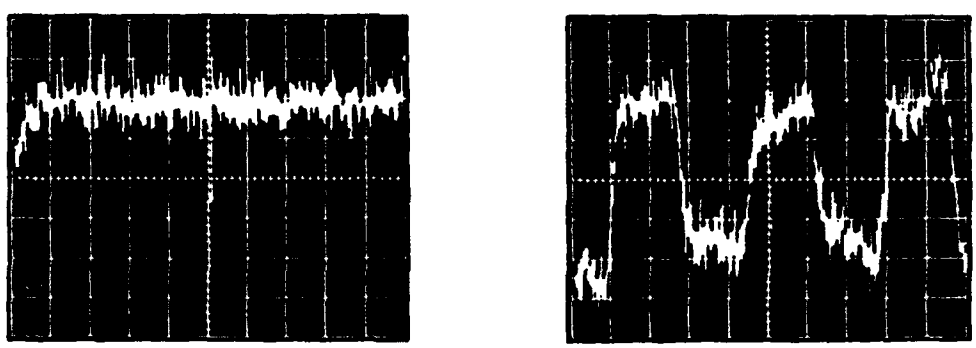


Fig. 3 Output from an all-optical multivibrator in which a NOR-gate is configured as an inverter and the output is fed back to the input. Feedback blocked on the left and feedback added on the right.

The hybrid TDCS and the corresponding time shift keyed data are shown in Fig. 5. In preliminary experiments the signal energy in the waveguide is 11.3 pJ and the control energy is 96.5 pJ. Because of mode mismatch and poor coupling into the fiber, the control energy exiting the fiber is 30.2 pJ, which means that the device fan-out or gain is 2.7. These semiconductor results represent the first step toward a compact, all-semiconductor TDCS.

Potential Applications of Ultrafast Gates

Ultrafast gates may enhance the capabilities of telecommunication networks whenever it is the bandwidth of the switch that limits the system performance. Four application arenas include: nodes in ring networks, demultiplexers at the end of transmission fibers, header reading in self-routing packet switching and time slot interchangers. To illustrate the architectural considerations in using ultrafast gates, we have designed a self-routing packet, 100 Gb/sec, soliton ring network serving a few hundred user nodes [6]. The slotted ring is a "light-pipe" in which the data remains in optical format throughout the network and converts to electronics only at the host and destination nodes. In this strawman example we select a trivial protocol:

[1] if *ForMe* then remove packet and replace with empty packet; or,

[2] if *Empty* and packet queued in buffer, then replace empty with new packet.

The design focuses on the network access nodes (Fig. 6), where the ultrafast gates are used to decode the header. The code matching logic module operates at the bit-rate to check if the header matches the local address or corresponds to an empty packet, and the module outputs are electronic signals that control a network of routing switches. The delay in the upper arm compensates for the latency in the logic module. The exchange/bypass network routes the incoming packet or a new packet, operates at the packet rate, and can be reconfigured in the time guard band between packets. When the packet reaches its destination, it is bit-rate down-converted to speeds accessible by electronic shift registers. An optical phase-lock loop is used to synchronize the local clock to the ring data, and erbium-doped fiber amplifiers are used to compensate for the insertion and splitter losses.

Block diagrams of the code-matching logic modules and the exchange/bypass network are shown in Fig. 7. In the first gate of the code-matching logic module the header is inverted and logic level and timing restoration is performed. An empty packet is assigned an all one header to maintain clock synchronization. One AND-gate detects if the packet is empty, while the XOR-gate and the other AND-gate detect if the packet should be read. If READ is true, then the optical exchange/bypass network routes the incoming packet to the bit-rate down converter and switches an empty packet on-line. If the EMPTY and QUEUE bits are both on, the empty packet is replaced with the new packet. Only one input to each routing switch is used to avoid cross-talk. Further details on the various modules as well as failure safeguards and the scavenger network node are described in Ref. [6].

By using bit-rate switches and guaranteeing bit-level synchronization, we can implement a "logic tuner" rather than a physical tuner (as in wavelength division multiplexing (WDM)). For example, the frequency filter in a WDM system is replaced by the local node address, and we transmit to different users by different codings of the header. In this time division multiplexed (TDM) system each node shares the same physical representation, which makes tasks such as broadcast simpler. Also, for the TDM case the hardware in each node can be identical and the architecture is easily adapted to a packet switching environment. From this study we find several issues that arise when trying to implement the soliton ring network:

[1] in the 100 Gb/s régime, the logic gates must have a switching energy at or below 1 pJ in order to maintain the optical power requirements at reasonable levels;

[2] even for a system with just a few ultrafast gates, the logic gates must be cascadable, restoring both timing and amplitude, for a robust implementation;

[3] optical amplifiers with high saturation power, in the range of 0.3 W, are needed for ultrafast, all-optical transport systems; and

[4] clock extraction and packet injection synchronization at the bit-level are major issues for an ultrafast network.

In summary, we have presented a TDCS that performs logic using time shift keying in a clocked digital optical processor. Soliton dragging is one example of a TDCS architecture

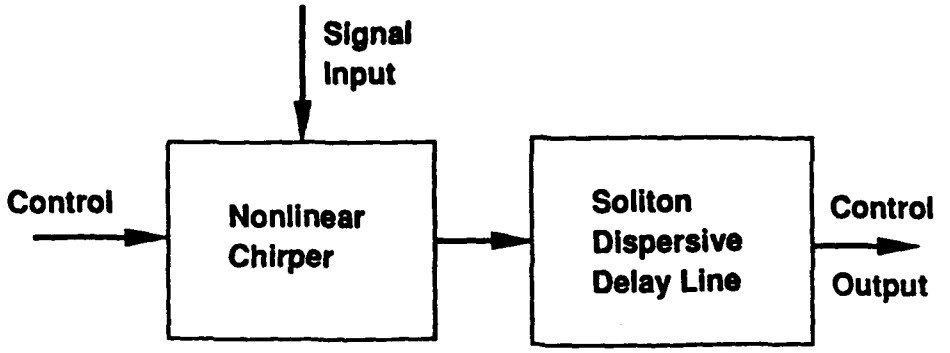


Fig. 4. General architecture for an all-optical time domain chirp switch (TDCS).

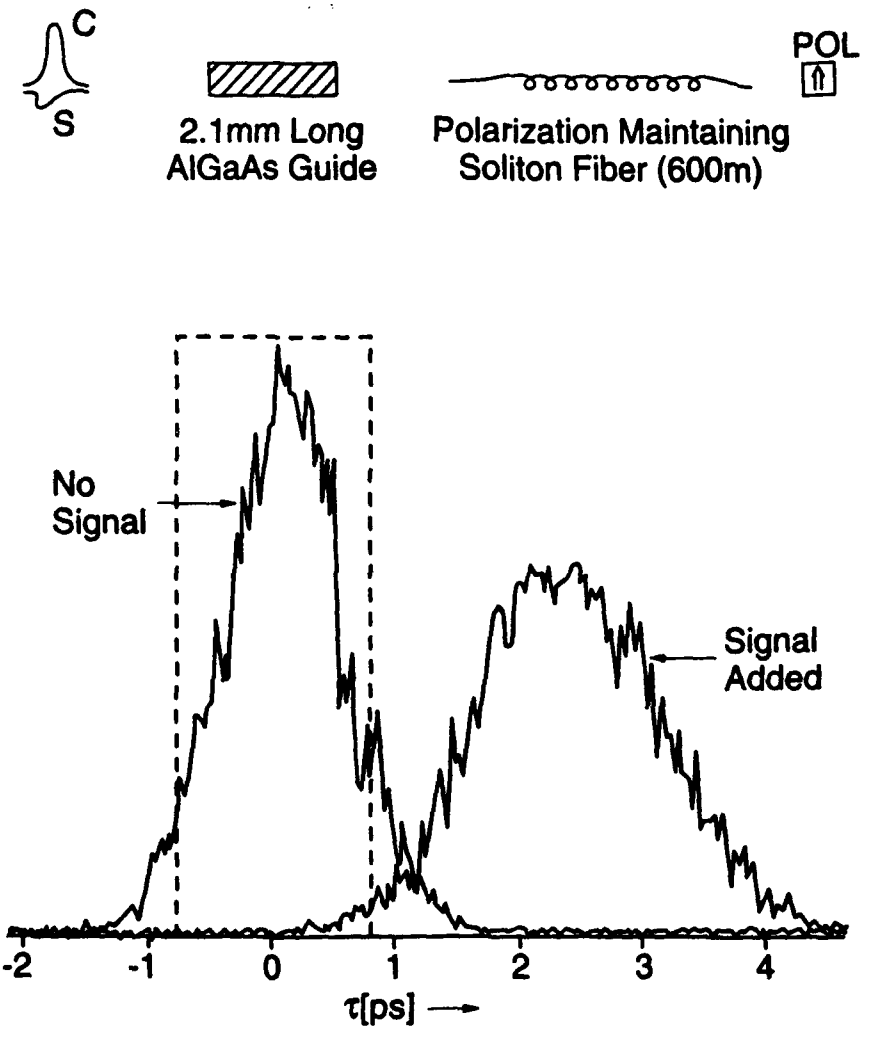


Fig. 5. Hybrid TDCS in which the nonlinear chirper corresponds to a 2.1 mm long AlGaAs waveguide. The cross-correlation of the clock with the control pulse is also shown for a signal energy of 11.3 pJ and a fan-out of 2.7.

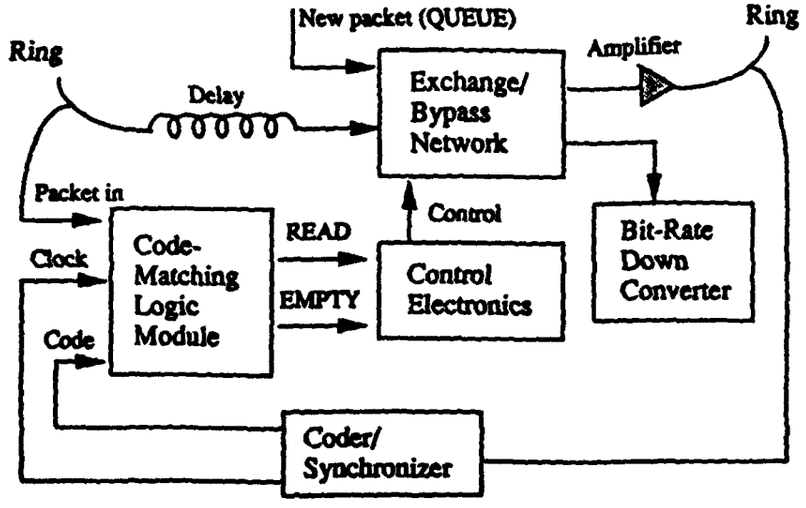


Fig. 6. Schematic of a network access node in the soliton ring network.

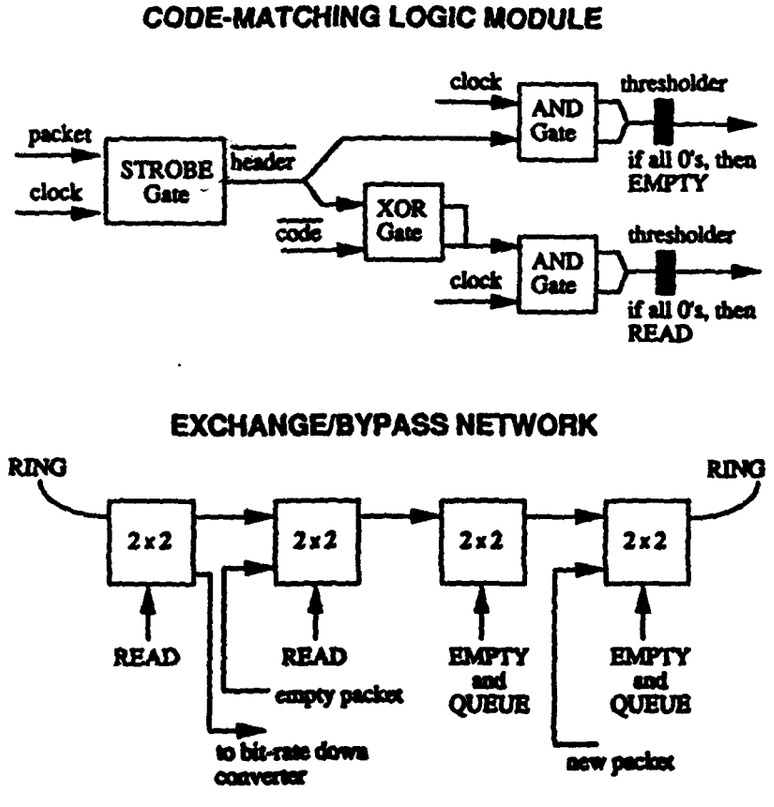


Fig. 7. Block diagrams of the code-matching logic module and the exchange/bypass network. The code-matching logic module contains the ultrafast soliton gates, while the exchange/bypass newtork consists of slower electro-optic switches.

implemented in fiber form that has yielded the lowest switching energy of any all-optical gate because of the separation between the nonlinear interaction and the soliton dispersive delay line. A hybrid TDCS that uses an AlGaAs waveguide proves the mechanisms in the TDCS architecture and represents the first step toward a compact, all-semiconductor TDCS. Finally, we presented the design of a 100 Gb/s soliton ring network to illustrate the opportunities and complexities that ultrafast gates create.

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92-17271

GEO Modules and All-Optical Time Slot Interchangers

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Abstract

We design an all-optical time slot interchanger using Generalized Exclusive-Or modules, which are boolean and connectivity complete logical abstractions of soliton dragging logic gates. Time difference techniques are used to implement a feed-forward time-slot interchanger that does not require memory or feedback.

Introduction

Recently ultrafast, cascadable, all-optical soliton logic gates with gain that satisfy all requirements for digital optical processors have been demonstrated in optical fibers [1,2]. The logic is based on time shift keying in which a "1" corresponds to a pulse that arrives within the clock window and a "0" to either no pulse or an improperly timed pulse. In a NOR gate using a 425 m length of fiber, switching energies as low as 5.8 picojoules have been obtained. Although the latency (or transit time in the gate) is ~2μsec, the processing speed for a pipelined input can be up to 0.2 THz. Efficient utilization of these high-speed, long latency gates requires architectures based on serial processing in the time domain that can exploit the bandwidth and "hide" the latency [3].

A Generalized Exclusive-OR (GEO) module is a boolean and connectivity complete logical representation of the aforementioned soliton dragging logic gate. For designing systems and architectures we use GEO-modules as a design tool to abstract from the physical implementation of the soliton logic gates. One key advantage of this approach is that the system architecture is independent of the device hardware, allowing devices to be upgraded provided their functionality remains the same. In addition, all-optical designs using GEO-modules can lead to minimal component implementation of many important functions because the GEO-module logic is closely tied to the physics of the fiber gates.

We present a catalogue of applications for combinatorial GEO-modules such as buffers, NOR-gates, and routing switches. Also, we demonstrate the utility of using the GEO-module as a design tool by designing several versions of feed-forward time slot interchangers (TSI). By utilizing a feed-forward architecture, the inherent operating speed limitation imposed by the latency in a typical TSI using feedback or memory is eliminated.

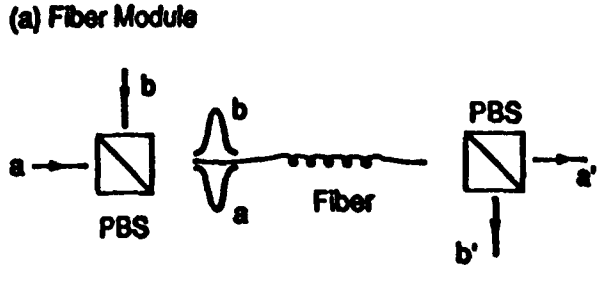


Figure 1. (a) Basic building block for a soliton dragging logic gate, (b) A generalized exclusive-OR (GEO) module.

Generalized Exclusive-Or Modules

The fundamental building block in soliton dragging logic gates is a birefringent fiber surrounded by two polarizing beam splitters (PBS), as shown in Fig. 1a. In soliton dragging two orthogonally polarized pulses interact through cross-phase modulation and impart a frequency chirp upon one another. This phase shift translates to a time shift after propagating in a dispersive delay line causing a pulse to arrive outside the predetermined clock window. For the discussion here, the details of the switch hardware or implementation are not as important as the functionality which the soliton dragging gate represents. More generally, we can replace the fiber module by a four-port GEO-module, (Fig. 1b), with inputs a and b and outputs a' and b', where $a' = a \cdot \bar{b}$ and $b' = \bar{a} \cdot b$. In other words, the input along one axis propagates to the output along the same axis unless blocked by the other input.

A single GEO-module can implement an inverter as shown in Fig. 2a. An inverter consists of a clock (CLK) or power supply "1" input along one axis and a signal input along the other. The output along the CLK axis will be the complement of the signal. Since the two outputs of the GEO-module are orthogonally polarized, both outputs can be combined using a polarization combiner to implement an XOR gate.

Two GEO-modules can be interconnected to provide high functionality. By using each GEO-module as an inverter, we have implemented a broadcast switch to generate multiple copies of the input (provided the power supply is larger than the signal) as shown in Fig. 2b. Since the signal is replaced by a new CLK pulse, this configuration can also serve as a pulse regenerator or a clock-ANDer to restore the logic level and signal timing. The NOR-gate described in ref. [1] is shown in Fig. 2c. Along the CLK axis we find A NOR B and along the orthogonal axis we find A AND B. Note that A and B act in series allowing the same idea to be extended to an N-input NOR gate. Since a NOR-gate is boolean complete, GEO-modules must also be boolean complete. For the same hardware used in the NOR gate we can also implement a routing switch (Fig. 2d). Note that this is a logic switch (the logic value of A is routed) rather than a physical switch (i.e. in a physical switch the photons corresponding to signal A would be routed). By interconnecting two such routing switches with two 3 dB couplers we can implement a directional coupler: since a directional coupler is connectivity complete, a GEO-module must also be connectivity complete.

Because the GEO-module is a passive element, obtaining gain requires a clock (CLK) input, or power supply "1", with amplitude greater than the signal input. In addition, the output of interest must be along the axis corresponding to the CLK. For example the NOR-gate in Fig. 2c has a CLK or "1" input and the output is along the same axis; in fact the gate has been experimentally demonstrated to have a gain of six. On the other hand, if the gate is used as an AND-gate there is no gain since the output is only signal B. A complete system can be built using gates without gain, but then clock-ANDers must be installed periodically in the system to restore the logic level and timing.

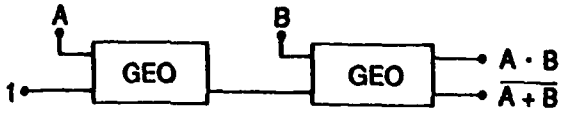
(a) Inverter



(b) Broadcast or Buffer



(c) NOR-gate and AND-gate



(d) Routing Switch

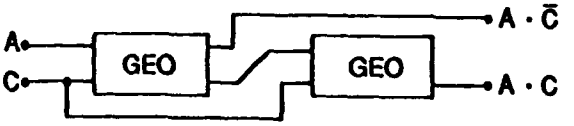


Figure 2. Combinatorial GEO-Module Configurations: (a) inverter, (b) broadcast or buffer switches, (c) NOR and AND-gates, and (d) routing switches.

All-Optical Time Slot Interchanger

As we use time multiplexing to achieve parallelism in time, a programmable TSI that can rearrange the ordering of two data units A and B traveling in series is necessary to provide communication between time multiplexed processes. Depending on the value of a control signal, the ordering of two serially transmitted packets, A and B, will either remain intact (BAR state) or they

will interchange time slots (CROSS state). One method for changing time slot sequencing is to store the data in random access memory and then read it out in the desired order. Since present memory access times are much slower than the GEO-Module switching times this method would limit the overall operating speed of any such device. Another design which incorporates a feedback loop to reorder time slots requires that the time slots to be operated on must be separated by more than a gate latency [4]. The restriction that A and B must be separated by more than a gate latency is prohibitive for ultrafast processing when gates with large latency are used.

However, by using a feed-forward architecture which eliminates the need for a discrete optical memory or feedback we design a TSI which can reorder adjacent time slots and is not limited by the latency of the gate. The principle behind the feed-forward designs is to use an input stage to generate copies of the time multiplexed input sequence. The copies are then time delayed and recombined to generate two signals: one with the original ordering, the other with ordering interchanged. Each signal is then individually processed by a control circuit after which the signals are combined through a wired-OR at the output. Dependent upon the control signal the input will arrive at the output in either the BAR or CROSS state. We present three designs for the feed-forward TSI: 1) a design that requires 3 GEO

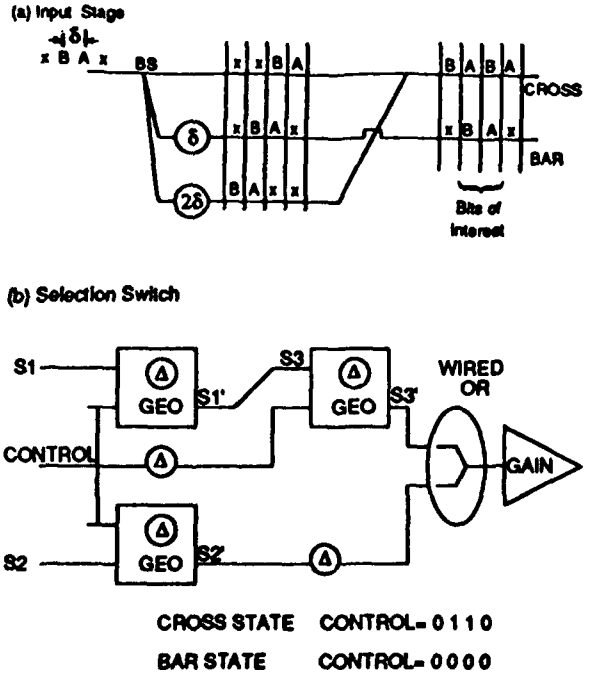


Figure 3. Feed-forward time slot interchanger; a) Input stage, b) Selection switch.

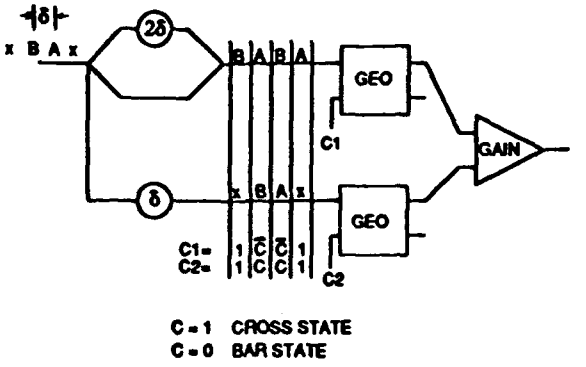


Figure 4. Minimal component design of feed-forward TSI.

modules and one common control; 2) a design requiring two GEO modules each with independent control and, 3) a design which requires three GEO modules each with independent control

The input time multiplexed sequence consists of time slots temporally spaced by δ units. In the first design, three copies of the input are made and two are passively time delayed by δ, and 2δ units, respectively. The undelayed and 2δ delayed copy are then combined using a wired-OR gate as shown in Fig. 3a. This interchanges the order of the time slots A and B on signal S_1. Note that the wired-OR gates can be used to combine the signals provided we guarantee that two ones do not arrive simultaneously and interfere at the wire-OR: this requires that two time slots be left blank on either side of the time slot pair being operated upon. A three GEO-module selection switch picks one of two bit streams (Fig. 3b), as determined by the control signal CONTROL which is coded to look only at the bits of interest. Because of the various wired-OR's an amplifier is required at the output to restore signal levels for cascadability. Also, an amplifier will probably be required at the input to compensate for splitting losses.

The next design is a minimal component feed-forward TSI. As a consequence of reducing the number of GEO-Modules from three to two an increase in complexity of the control signals is required. This design has an identical input stage as the previous design which provides signals S_1 and S_2. Each signal is fed into a separate GEO-Module with independent control sequences coded to look at the time slots of interest as shown in Fig. 4. As before a wired-OR is used to combine the signals providing a single output. The drawback with both this design and the previous design is that the two blank time slot restriction reduces system throughput for pipelined operations by fifty percent. In addition, simplicity of system design scales very poorly

with increasing numbers of time slots to be interchanged.

By including one extra GEO-Module with an independent control to the previous design we can design a completely feed-forward TSI without any blank bit restrictions. As with both previous designs the input time multiplexed sequence must be copied in triplicate and two copies delayed by δ and 2δ units,

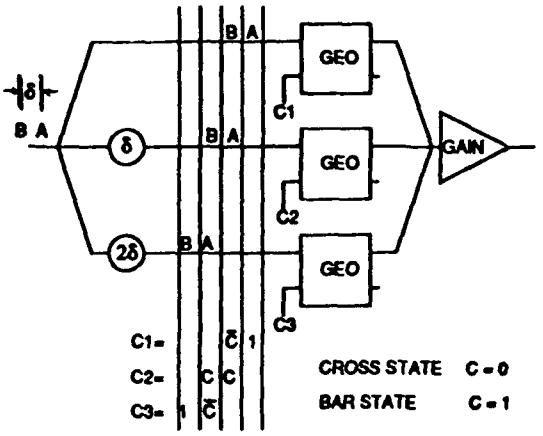


Figure 5. Feed-forward TSI without blank time slot restriction.

respectively. However, unlike the previous designs wired-OR gates are not used to recombine the delayed signals to interchange time slots. Instead, each signal is passed to a separate GEO-Module with independent control which is appropriately coded to look at its individual time slot pair of interest. Because there are no blank time slot restrictions the control sequence must operate at the same bit rate as the input time multiplexed signal in order to operate on adjacent time slot pairs. Table 1 shows the individual control sequence codes for the j^{th} time slot pair, (corresponding to time slots A and B). A state table for the CROSS and BAR states is shown in Table 2. The undetermined outputs (‡) will not interfere with the operation of the TSI since they occur outside the time window of interest.

Summary

GEO-modules are a logical representation of ultrafast, all-optical soliton logic gates that can be used for design purposes. In addition to being boolean and connectivity complete, GEO-modules maximally exploit the device physics and, therefore, lead to minimal component implementation of all-optical functionalities. We have demonstrated a time slot interchanger design which utilizes feed-forward techniques to eliminate the need for feedback or memory, thereby masking the latency.

Table 1. Control Sequence for non-restrictive TSI.

C_1	$\overline{C^i}$	1^i	$\overline{C^j}$	1^j
C_2	C^i	C^j	C^j	C^k
C_3	1^j	$\overline{C^j}$	1^k	$\overline{C^k}$

Table 2. State table for CROSS and BAR output of non-restrictive TSI design.

Bar State: C=0					Cross State: C=1				
S_1	x	x	B	A	S_1	x	x	B	A
C_1	$\overline{C^i}$	1	1	1	C_1	$\overline{C^i}$	1	0	1
S_1'	‡	0	0	0	S_1'	‡	0	B	0
S_2	x	B	A	x	S_2	x	B	A	x
C_2	C^i	0	0	C^k	C_2	C^i	1	1	C^k
S_2'	‡	B	A	‡	S_2'	‡	0	0	‡
S_3	B	A	x	x	S_3	B	A	x	x
C_3	1	1	1	$\overline{C^k}$	C_3	1	0	1	$\overline{C^k}$
S_3'	0	0	0	‡	S_3'	0	A	0	‡
Output	‡	B	A	‡	Output	‡	A	B	‡

‡ -undetermined output

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Demonstration of a Novel Optical Code Division Multiplex System at 800 Mchips/s

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Abstract

A novel code division multiple access system using Alberta codes and complementary correlation is demonstrated at 800Mchips/s. Completely passive optical multiplexing and demultiplexing is performed throughout. Complementary correlation allows code orthogonality because bipolar electrical signals are generated from unipolar optical ones. The correlator is implemented optoelectronically with an array of metal- semiconductor- metal photodiodes. We show that the bit error rate performance of the system is not degraded by the presence of multiple channels, and that zero cross talk is nominally achieved. An unusual property of such systems is confirmed: that the bit error rate on a channel can be reduced by the presence of an interfering channel if the two transmitters are not chip synchronous.

Introduction

In code division multiplex transmission a unique coded sequence of pulses is sent to represent a bit on each multiplexed channel. By correlating the received signal with the appropriate bit pattern, a particular channel can be extracted from the multiplexed signal. Efficient code division operation requires that the channel codes be orthogonal, that is, the cross- correlation obtained between a signal sent using one code and a receiver set to a different code, be zero. Non- orthogonal codes produce noise contributions from every signal present.

Intensity modulation optical signals have only positive values. Crosscorrelations between nonzero, positive- only signals cannot equal zero. Codes for optical code division systems therefore attempt to minimise the crosscorrelation noise, holding each crosscorrelation below some limit [1,2].

Another approach to optical code division multiplex is the technique of complementary correlation [3]. It has been proposed that the complementary correlation operation can be implemented directly in a photodetector and that with correctly chosen codes (A-codes), the crosstalk between channels can be made zero [4]. For full orthogonality the address code bits and the signal bits must be synchronously combined at the transmitter. There is no requirement for synchronising the receivers.

We report here the experimental demonstration of a complementary correlation receiver that can select among five code- division channels, each operating at 50Mb/s, carried at a multiplexed line rate of 800 Mb/s. The high speed of the system is a direct result of performing the correlations in the photodetectors rather than in subsequent logic.

The Complementary Correlation Receiver

The complementary correlation receiver is shown in Fig. 1. It consists of sixteen GaAs *metal- semiconductor- metal photodiodes* configured to have one common contact. The multiplexed optical signal is delivered to these photodiodes through a power splitter and a set of delay lines of lengths that differ by one chip interval. Complementary correlation is the process of correlating a signal with a "target" pattern, and simultaneously with the complement of that pattern, and subtracting the two. The operation can be expressed as

$$A(t)=\sum_{n=0}^{N} S((t+nT)\{T(nT)-[U(nT)-T(nT)]\}$$

where U(nT) *is the unit step function*, T is the bit interval, N is the length of the correlation sequence, and T(nT) is the "target" code for which the receiver is correlating. Because of the subtraction, A(t) is a bipolar signal even if S(t), the incoming multiplexed signal. is not. Letting

$$R(t)=\sum_{n=0}^{N} S(t+nT)T(nT) \text{ and}$$

$$W(t)=W=\sum_{n=0}^{N} S(t+nT)U(nT)$$

(W = the weight *of the channel code*)
it follows that

$$A(t) = 2R(t)-W.$$

This signifies that the output of the complementary correlator is twice the correlation of signal with target, minus the Hamming weight of the codes (which are assumed all to have the same weight). A-codes are defined [4] to have crosscorrelations which are equal to half the Hamming weight at the decision time t=0, when the channel code and target ate time *aligned.* At other times the only constraint is that the crosscorrelation is less than the weight. With these codes the *crosscorrelation* signals are zero at t=0, and negative otherwise while the autocorrelation signal is positive (and equals W(t)) for all the codes. The target channel is isolated from this signal simply by removing negative values.

The optoelectronic complementary correlation is achieved by biassing positive the photodetectors corresponding to ones in the channel code, and biassing negative the others (i.e. the complement of the code). The photocurrents from the two groups subtract in the load.

The A- codes used in the experiment are 8 bits long, and support five orthogonal channels. (The code sets were determined by searching. Sets supporting up to seven channels have so far been found.) The receiver is supplied with *sixteen photodetectors.* Four negatively- biassed detectors at each end of the code word are needed to ensure that the orthogonality conditions are met. The transmitted codes are separated by four blank bits for the

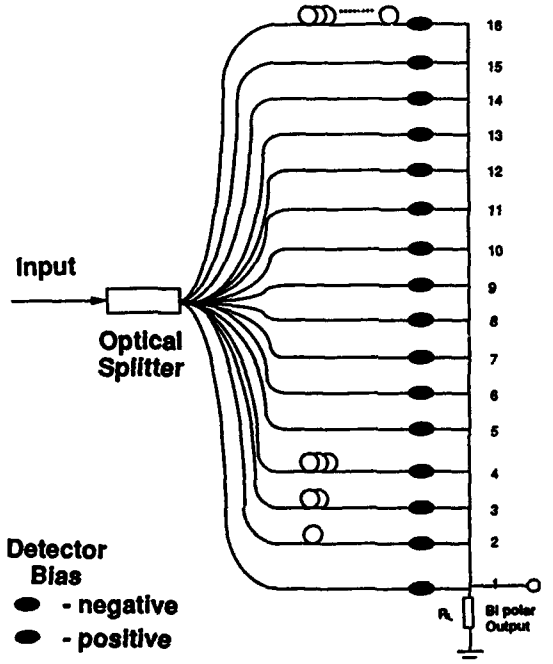


Figure 1. Configuration of the complementary correlator for a code of length 8. The address of the receiver is set by the polarity of the bias voltage applied to each of the 16 photodetectors.

same reason. The data rate of the multiplexed signal is therefore sixteen times the data rate of a single channel. For comparison, prime codes require 25 bits to multiplex five channels.

Experimental Demonstration

The experiment performed is shown in Fig.2. Two of the five A-codes were formed from a single electronic pulse by means of coaxial delay lines. The pulse rate was 50MHz, corresponding to the data rate on a single channel, the pulse width was less than 500 ps, permitting 16 pulses to be interleaved. The coded pulse streams for each channel modulated a laser diode operating at 850nm, and the optical power was combined in a fibre power splitter. As each code has weight four, only four coaxial delay lines were required in each transmitter.

After transmission over a short length of graded index optical fibre the multiplexed signal was decoded in a complementary correlation receiver. The biases on the detectors could be set for complementary correlation with the code for either of the two channels. The direct output of the correlator is shown in Fig 3.

The bit error rate for one of the channels, measured after regeneration of the NRZ signal from the clipped waveform, is shown in Fig.4 as a function of average received optical power per detector. The error rate for the channel alone, and in the presence of the signal from the other channel are shown. There is no evidence that the presence of the second channel worsens the bit error rate, and we conclude that the codes are effectively orthogonal as intended. There is no error floor down to an error rate of 10^{-7} at a received power of -16dBm per detector (-4dBm per receiver). This was the measurement limit in the experiment, set by difficulties in synchronising the correlated signal to the error rate test set in the presence of the correlation delay. (Clock recovery was not attempted in this experiment.)

Since the responsivity of the particular msm detectors used was about a factor of 3 lower than reported values, we conclude that the system could reach a bit error rate of 10^{-7} at a received power of -21dBm per detector

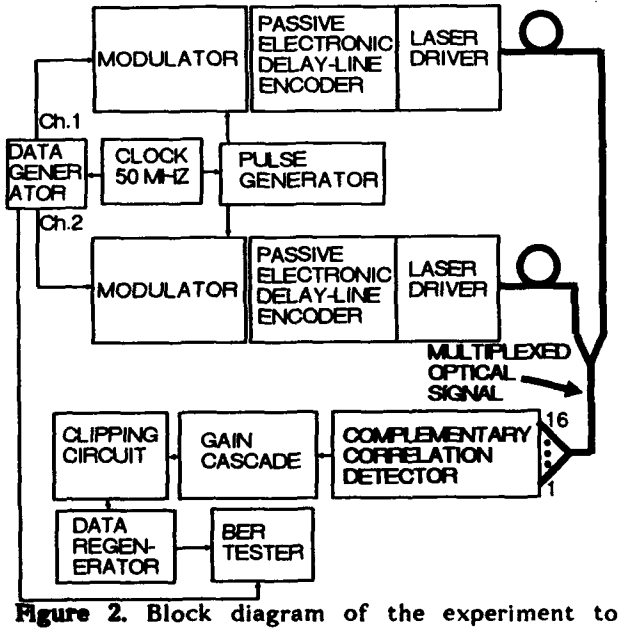


Figure 2. Block diagram of the experiment to demonstrate two channels of a five channel CDMA system using complementary correlation.

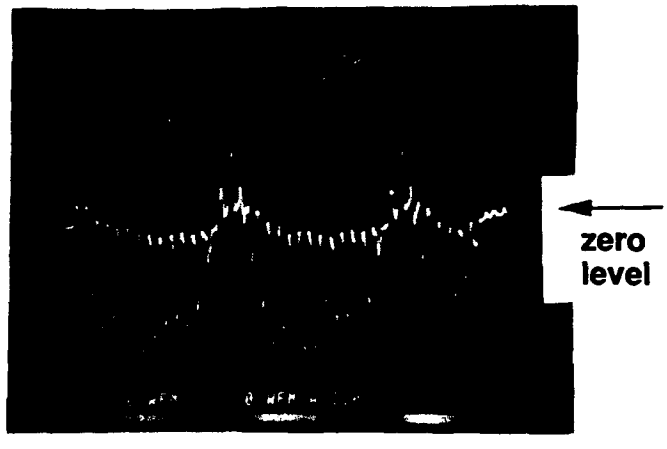


Figure 3. Bipolar electrical signal at the output of the complementary correlator detector. By setting the "zero" level as shown the positive going correlation peaks are separated from the rest of the waveform.

(-9dBm per receiver) with msm photodiodes, and is very likely capable of rates to 10^{-9} usually required. Other detectors, for example avalanche photodiodes, could of course be used in a similar photocurrent- summing configuration to obtain greater sensitivity.

A peculiarity of the system is the slight improvement of the error rate when the second transmitter is running, visible in Fig.4. This enhancement was consistently observed on both channels. An analysis of asynchronous cdma using A- codes and complementary detection indicates that the bit error rate of the correlated channel can be improved by the presence of slightly asynchronous interfering channels.

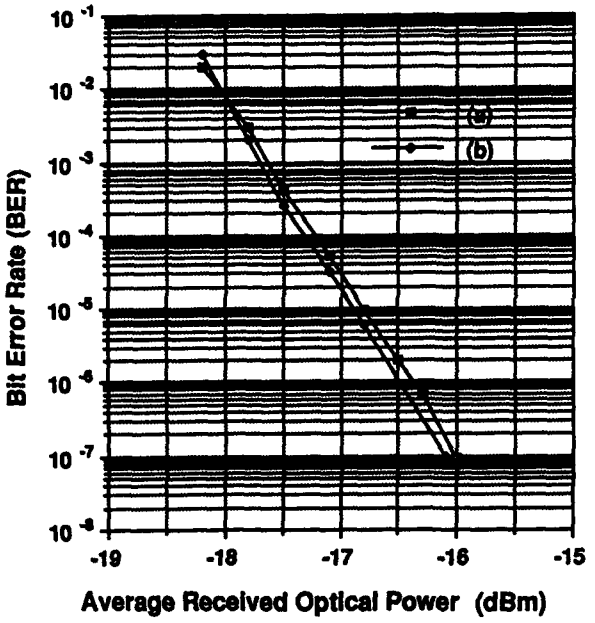


Figure 4. Bit error rate (BER) as a function of average received power per chip at the complementary correlation detector. (a) No intefering transmitters in the system, (b) one interfering transmitter in the system.

This is because the interfering channels actually force the overall correlated signal in the negative direction, better isolating the positive-going pulses of the correlated signal.

Since complementary correlation is performed within the photodetector array the need for wideband electronics in the receiver is minimised to two analogue operations - the correlated signal needs to be amplified and clipped. The correlation receiver does not require to be synchronised to the multiplexed signal, and clock recovery can be done at the channel, rather than the line rate. The transmission speed in the experiment was limited by the switching speed of the laser. Very fast pulses can, however, be obtained, and A- codes could be formed from them by passive fibre delay- line networks. With such a system we anticipate that very high cdma rates could be obtained.

Acknowledgment

The contributions of J.Noad and colleagues at the Communications Research Centre to the construction of the complementary correlation detector are gratefully acknowledged.

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Photonic Packet Switch Based on a VSTEP Two-Dimensional Array

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Abstract

Photonic ATM switches, using two-dimensional arrays as buffer memories and routing fabrics are discussed. Possible switch performance is estimated based on a vertical-to-surface transmission electro-photonic devices(VSTEP).

1.Introduction

High-speed packet switches, which can handle wide-bitrate-range data streams in an integrated manner, are expected to play an important role in future broadband networks. Introduction of photonic technology to very high-speed packet switches has been proposed[1]-[6]. Among these high-speed packet switches using photonic technology, the packet switch, using VSTEP's (Vertical to surface transmission electro-photonic devices)[7][8] as optical buffer memories, is expected to achieve high switch performance in small size[5]. The VSTEP two-dimensional (2D) array can be used not only as memories but also header-driven routing fabrics[9]. This paper discusses a photonic packet switch using VSTEP 2D array as buffer memories and a header-driven routing fabric with priority control.

2.Photonic packet switch structure

There are four category of high-speed packet switches, namely, crosspoint, input, output and shared buffer packet switches. Crosspoint and output buffer packet switches have advantage in switch control ease. However, they require relatively large amount of buffer memories. The shared buffer packet switch requires the smallest amount of buffer memories. However, switch control is so complicated to be accomplished by current optical functional devices. The input buffer packet switch requires relatively small amount of buffer memories and switch control is easier than the shared buffer switch. Thus, the input buffer photonic packet switch is suitable for the near future implementation. Figure 1 shows a block-diagram of the most simple input buffer photonic packet switch, which consists of optical buffer memories and an N x N routing fabric with priority control. The input line utilization for the input buffer switch is usually limited to 50-60% by packet contention. Thus, very high link speed ,as high as 10 Gbps, is desirable for this photonic packet switch to have advantage over electronic packet switches.

2.1.Buffer memory

The buffer memory sends out packet cells to the N x N routing fabric in first-in, first-out manner. Massively parallel interconnection capability of the VSTEP 2D array, based on free-space light beam propagation, is very effective in achieving high buffer memory throughput. Figure 2 shows a structure of a buffer memory using

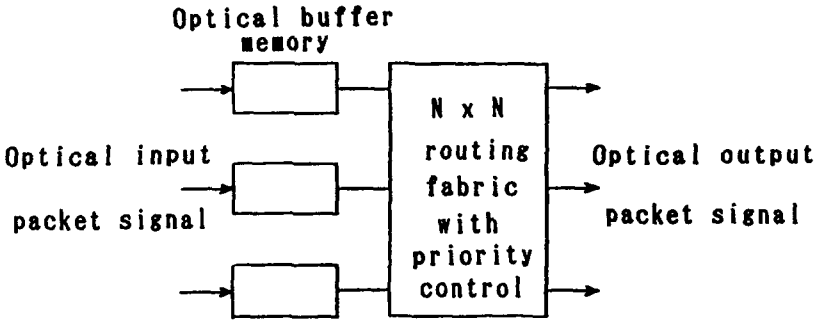


Fig. 1 Input buffer photonic packet switch

VSTEP. An input packet signal, with cell length p, is led to an optical shift register, which consists of VSTEP 1D array opto-electronic interface circuits and an electronic shift register, and converted to a p-bit parallel configuration. Optical signals from the shift register are distributed to a (d-column) x (p-row) VSTEP 2D memory array. One column of the VSTEP 2D memory array store parallel configuration optical signals in a write period. Write optical signal speed is reduced to (packet cell speed) x 2/p due to the parallel operation. Therefore write optical signal speed is only 47 Mbps, even though packet cell speed is 10 Gbps in case that p=424 (the cell length is 53 byte.). In a read period, stored optical signals are send back to the shift register and converted to a serial-bit configuration output packet cell. VSTEP switching energy is expected to be reduced less than 10 fJ for a several-tens Mbps optical signal. This switching energy is possible on condition that p=424, d=30 to satisfy cell loss rate less than 10^{-10} for 50-% input link utilization, 0.1-mW optical shift register output power and 6-dB free-space interconnection loss.

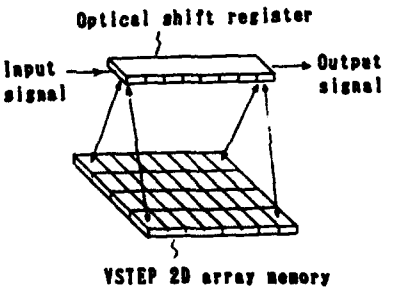


Fig. 2 Buffer memory using VSTEP

2.2.Routing fabric with priority control

The VSTEP 2D array can also be used as the N X N header-driven routing fabric with matrix-vector multiplier structure as shown in Fig. 3. The optical packet signal from the buffer memory is distributed to one column of the (N-column) x (N-row) VSTEP array. The output optical signal from each row of VSTEP's is combined to an optical output signal. For each row of the VSTEP array, a bias signal V1-V3 is applied through a resistance.

Figure 4 shows the timing chart for this routing fabric. The VSTEP bias voltage V1, V2 and V3 are raised to Vh during time slot T1, T2 and T3, respectively. After that, bias signals are kept to V1 during cell transmission time. The optical packet signal has header bit at time slot T1, T2 or T3, When the optical header bit synchronizes with the time slot that the bias signal is Vh, the VSTEP is turned to the ON state[9]. When the optical header bit does not synchronize with the bias signal, the VSTEP remain in the OFF state. During the OFF state, the data bits of the optical packet signal is not transmitted, because it is absorbed in the VSTEP. The ON state VSTEP functions as an optical amplifier, which transmits optical data bits

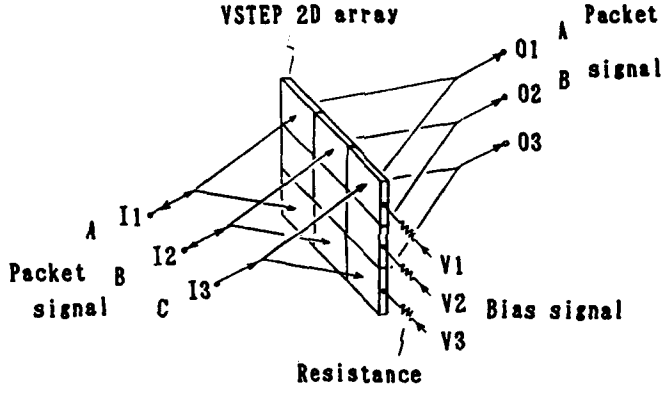


Fig. 3 Routing fabric with priority control

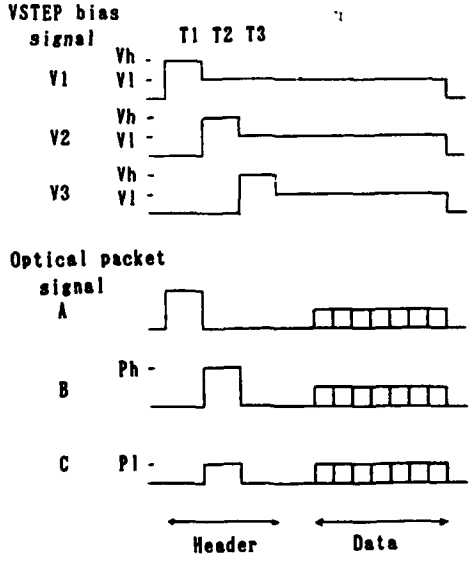


Fig. 4 Timing chart

during V1 bias signal has been applied. In this way, optical packet A and B, in Fig. 4, can be self-routed to the specific output port O1 and O2 in Fig. 3, respectively. The ON state VSTEP can cope with the 10-Gbps data bits in its optical amplifier operation.

Priority control can also be achieved using same structure, preventing optical packet signals from collision at the output port. For example, both optical packet signal B and C, in Fig. 4, have header bit at time slot T2. However, header bit optical power of the packet B is larger than that of the packet C. As a result, the VSTEP, to which the packet B has been injected, is turned to the ON state faster than the VSTEP, to which the packet C has been injected, with increase in in injection current. Increase in injection current causes drop in VSTEP applied voltage due to the function of the resistance. Thus, the VSTEP, to which the packet C has been injected, can not be turned to the ON state. In this way, priority control can be achieved by changing optical power of the header bit.

The accepted optical packet is amplified by the turned ON VSTEP. By half reflection coating on the reverse side facet of the VSTEP, the accepted optical packet is transmitted to not only the output but also the input port. Thus, by detecting the back-propagated optical packet signal, the buffer memory control circuit know whether the optical has been accepted or rejected. In case of rejection, the buffer memory sends again same packet signal to the routing fabric in the next cell transmission time.

3.Conclusion

The photonic packet switch, using the VSTEP 2D arrays in the buffer memory and routing fabric, is proposed. The massively parallel interconnected buffer memory structure using VSTEP's is effective to obtain very high cell speed, as high as 10 Gbps. The proposed header-driven routing fabric using the VSTEP 2D array can cope with the 10-Gbps cell data bits in optical amplifier operation. Priority control can also be achieved using same structure. By using the proposed buffer memory and routing fabric, the photonic packet switch can provide extremely high performance.

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Photonic Fast Packet Switch With Gain

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Abstract

We demonstrate self-routing of optical data through a photonic packet switch with optical gain. A semiconductor optical amplifier is used to simultaneously amplify packets and detect address headers. The system described here uses a hybrid of optical switching and electronic control which results in a flexible system combining the advantages of both technologies. The switch is transparent to the bandwidth of the optical data thus allowing essentially unlimited payload bit rate. The user data rate in the present experiment is 1.24 Gb/s.

Introduction

Packet switching has become an attractive means of transferring digital information across high speed communications networks. The self-routing of packets using a photonic switch that is transparent to the optical information bandwidth [1] has several advantages over electronic switching, including flexibility of data format and the ability to avoid electronic speed bottlenecks. It has been shown [2] that in photonic packet switching data transfer rates for the information content of a packet (the payload) can be made independent of the address header data rate. Thus even for very high capacity systems, electronics can be used to detect and decode the address header and to control the routing switch. Since the address header of a packet is small compared to the payload, this approach does not significantly decrease the information transfer efficiency. Using a hybrid of optical switching and electronic control results in a flexible system which combines the advantages of both technologies.

One limitation of previous photonic packet switch demonstrations has been optical losses within the switching fabric. In the present paper we demonstrate a hybrid self-routing photonic packet switch that uses a semiconductor optical amplifier to compensate losses and provide a net optical gain. Furthermore, the semiconductor optical amplifier simultaneously detects [3] the address header as well as amplifying the incoming packets. By combining the functions of optical amplification of the packet and detection of the address header, the system architecture is simplified. The results described here show operation at a payload data rate of 1.24 Gb/s, but the payload data rate is limited only by the optical bandwidth of the system and could, in principle, be many tens of gigabits per second.

Experimental System

Fig. 1 shows the experimental arrangement. A DFB transmitter laser at 1.3 microns wavelength is directly modulated at 1.24 Gb/s with a NRZ format using an Anritsu ME522A data generator. The data generator was programed to provide packets with 9-bit address headers at 155 Mb/s and 48 byte payloads at 1.24 Gb/s. This format is set by available instrumentation limits, but in practical systems larger address headers and payloads would be used. Each packet begins with a single start bit (at 155 Mb/s) that provides the timing information for decoding the address header and routing the packet. As no external timing is needed, the system is applicable to asynchronous transfer mode (ATM) switching networks [4]. In particular, the header rate of 155 Mb/s and the payload size of 48 bytes conform to CCITT standards for ATM packets.

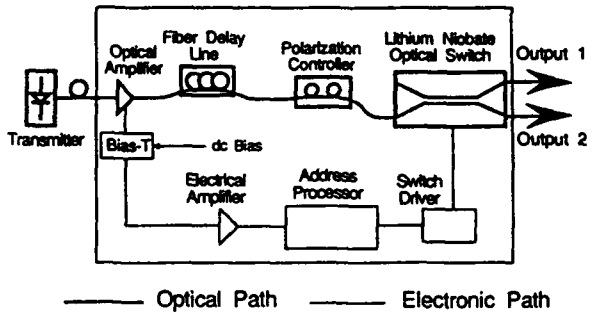


Fig. 1: Experimental photonic packet switching system

At the input to the packet switch the optical signal (at a power level of -15 dBm) enters the semiconductor optical amplifier/detector. The optical amplifier compensates losses in the switching system and also functions as a detector [3] for the address header, thereby eliminating the need for a separate optical receiver. The junction voltage of the optical amplifier is ac-coupled through a bias tee to a broadband electrical amplifier which drives the address processor. The measured electrical frequency response of the optical amplifier when used as a detector is shown in Fig. 2. The measured detection bandwidth was 363 MHz, which limits the data rate of the address header to less than about 600 Mb/s. The start bit preceding the address triggers a clock at the address header bit rate which in turn clocks the address bits into a shift register while ignoring the payload data. The output of the shift register controls a driver circuit which sets the state of the optical switch. The optical switch in these experiments consists of a 2x2 $LiNbO_3$ directional coupler with fiber pigtails [5]. Depending on the value of the address bit, the driver circuit changes the state of the $LiNbO_3$ switch to either the cross or bar state, thus routing the information to either of two outputs.

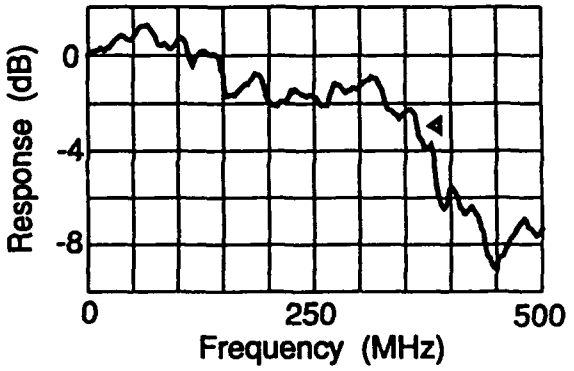


Fig. 2: Electrical frequency response of the optical amplifier

The input packets are delayed by a length of optical fiber which matches the delays of the detector, amplifiers and address decoder circuitry. This ensures that the complete packet arrives at the $LiNbO_3$ switch immediately after the switch state has been set. A polarization controller sets the polarization of the light entering the switch. For correct operation individual packets must be separated in time. A guard band between packets allows sufficient time for switch reconfiguration to occur between packets. In the present experiment, the guard band is approximately 45 nsec to ease initial experimental timing adjustments. We believe that it will be

possible to reduce this guard band to approximately the reconfiguration time of the $LiNbO_3$ switch (a few nanoseconds).

The fiber-to-fiber gain of the optical amplifier is about 10 dB. The total optical losses in the packet switch are around 8 dB, comprising 5 dB in the $LiNbO_3$ switch, 2 dB in an optical isolator at the input to the optical amplifier, and 1 dB of other losses. The net gain of the overall packet switch is about 2 dB.

Results

Fig. 3 is an oscilloscope trace of the two optical switch outputs showing correct routing of packets with a 155 Mb/s header data rate and a 1.24 Gb/s payload rate. The data generator at the transmitter produced packets with alternating addresses consisting of either 8 zeros or 8 ones. The address headers of the packets can be seen in Fig. 3 in the form of the start bit (a one) followed by either zeros or ones. The system routed the packets successfully, with no noticeable errors in packet destination. The difference in background light intensity between switched and unswitched packets is due to noise from spontaneous emission within the optical amplifier. No attempt was made to reduce this background noise, but it would be a straightforward matter to significantly decrease it by inserting a narrow band optical filter into the system.

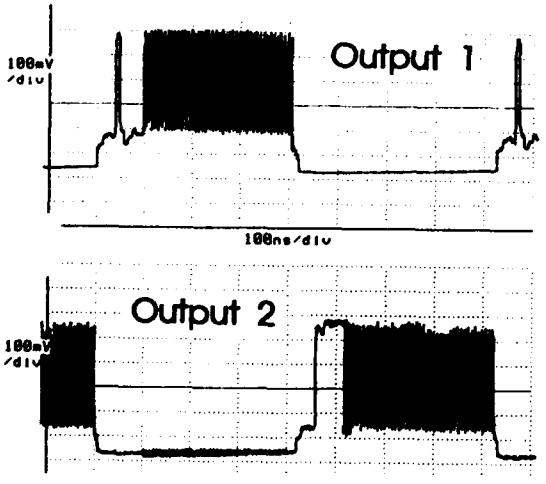


Fig. 3: Oscilloscope trace of the two optical switch outputs

Conclusions

We have demonstrated a flexible photonic packet switch with optical gain. The switch uses a hybrid approach which takes advantage of the flexibility of electronics to process the header information at a fixed data rate, while allowing optical information to flow through the system at an arbitrary rate (in this case 1.24 Gb/s). Losses in the switch are compensated using an optical amplifier. The system architecture is simplified by using a single device both as the optical amplifier and also as the detector for the address header.

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Monolithically Integrated InP Photonic Circuits for Optical Processing in Very High Speed Optical Loop

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Abstract

Passive Access Node Switches, consisting in two cascaded switches and two detectors, have been successfully monolithically integrated on InP substrates.

Introduction

Optical rings have found many applications in high speed Local Area Networks (LANs). Generally, such rings are formed by point to point optical transmission links, implying optical to electrical conversions at each node. These repeated conversions affect the reliability, generate jitter, increase the susceptibility to electromagnetic interferences and limit the bit rate to that allowed by the node processing electronics.

A novel optical ring system design, called the Very High Speed Optical Loop (VHSOL), has been recently proposed (1).

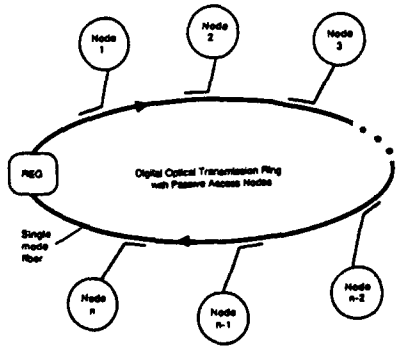


Figure 1: The Very High Speed Optical Loop

In contrast to the conventional ring structures, the VHSOL (Figure 1) preserves the transparency of the loop. Each node accesses the ring in a purely optical way. The loop was designed to operate at 2.4 Gbits/s with a packet transfer mode. Packets on the VHSOL posseses their own header field, but their information field can be formatted to accomodate standard ATM (Asynchronous Tranfer Mode) packets.

The key component of the VHSOL is the Passive Access Node (PAN) which provides the interface to the main optical fiber ring. The PAN is built as two cascaded optical switches followed by two integrated detectors (Figure 2).

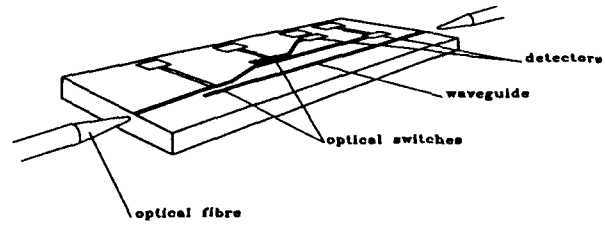


Figure 2: Schematic of the PAN switch

The first switch (access switch) performs an access control function so that the PAN can operate in a listening, receiving or transmitting state. The second switch (correlation switch) is used as an optoelectronic correlator for synchronization and address interpretation purposes. The PAN thus performs a self-routing function based on fully optical header interpretation.

In the listening state, a small amount of the optical power is tapped by the access switch. In this operating state, the address contained in the headers of the packets are continuously monitored by the PAN. The interpretation is based on a correlation technique using the correlation switch, the integrated detector and a narrow band receiver (2). When the PAN recognises its own address, the access switch goes into the receiving state, picking enough light for data interpretation. The optical

signal then goes to the second detector which is coupled to a broadband receiver. The PAN can also transmit informations to other users, taking the advantage of the access switch as a depletion modulator to write information on empty packets (continuous light stream) passing through the node.

In this paper, we present results on fully integrated PAN switches fabricated on InP. Both directional coupler and total internal reflection switches are discussed.

Structure and fabrication of InP PANs

Passive Acess Node Switches have been designed and fabricated on InP substrates. Two options have been pursued for the switches: the carrier depletion directional coupler (CDDC) (3) which operates with a reverse bias and the total internal reflection (TIR) switch (4) which uses carrier injection. The receivers are GaInAs pin detectors coupled to the GaInAsP waveguides by evanescent field coupling (5). The structure is grown by Chloride Vapour Phase Epitaxy in a two step process. The waveguides and the photodiodes are grown during the first step. Then, the photodiode regions are protected by SiO_2 and all the layers are chemically etched down to the InP layer separating the waveguide and the absorbing layer. The InP cladding layer and the contact layer are then locally grown. The same approach is used for the CDDC and TIR switches; The doping of the layers depending on the switch type (Figure 3).

This technology allows highly efficient switch and detector structures without any compromise on the device design. The p region of the 100 μm long photodiodes is achieved by localized Zn diffusion through a Si_3N_4 mask and the rib waveguides are etched by reactive ion etching in a CH_4/H_2 mixture.

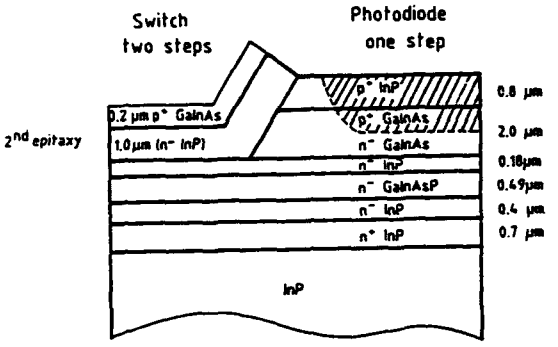


Figure 3a: Epitaxial structures for TIR-PAN

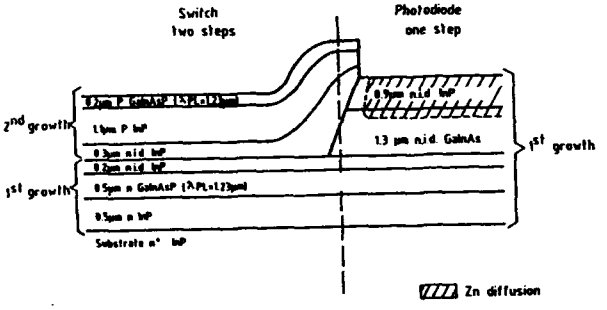


Figure 3b: Epitaxial structures for CDDC-PAN

Figure 4 shows a PAN switch based on TIR technology. Devices with intersecting angles of 2°, 3° and 4° have been realized. The active region is as small as 100 μm long for 4° angle leading to very short devices (~ 1 mm long). The CDDC devices are larger (2, 3 and 4 mm long coupling region) which makes the CDDC-PAN switches ~ 1 cm long.



Figure 4: SEM photograph of a PAN switch with TIR technology

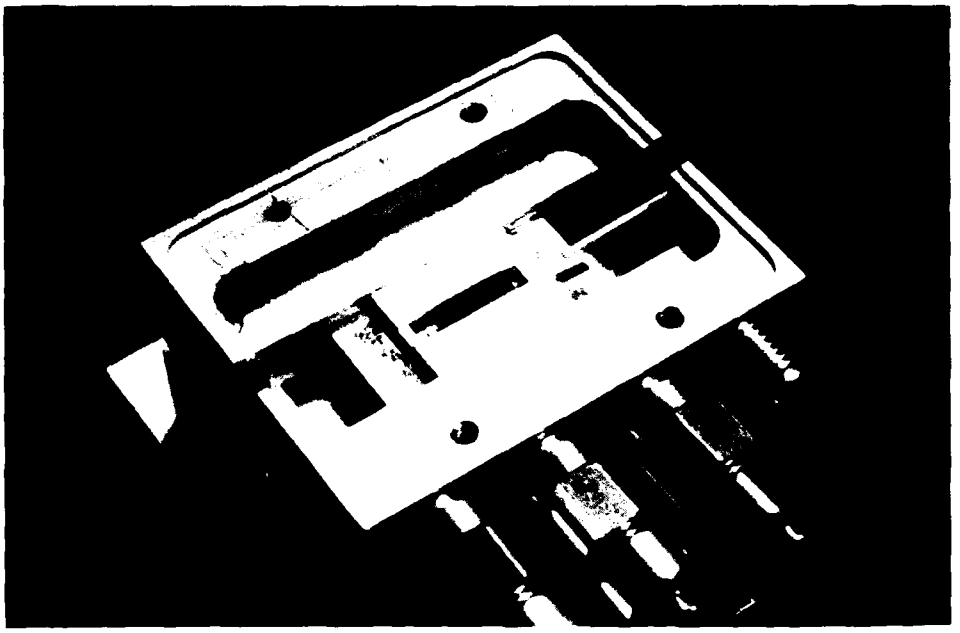


Figure 5: Photograph of high frequency module

After cleavage, the devices are mounted in a module compatible for high frequency operation providing all the necessary optical and electrical interfaces (Figure 5). The PAN switch requires only one fiber in and one fiber out which reduces the pigtailing problem to a similar case to the laser one. Couplings losses of 3 dB/facet can therefore be expected.

Results and discussion

First processed devices exhibit all the desired functionalities although further refinement will be needed to fullfil all the system requirements. The waveguide losses measured by the Fabry Perot technique were found to be below 1dB/cm indicating that the second epitaxial growth introduces no significant degradation. Discrete and integrated directional couplers exhibit complete switching at ~ -6 V for 4 mm long devices and ~ -10 V for 3 mm long devices (Figure 6). The driving current of the TIR switches with 4° angle was 240 mA and was confirmed to be polarization independent (Figure 7). The detectors, strongly coupled to the waveguides, exhibit an absorption of 2060 dB/cm which means that nearly all the light is detected with 100 μm long devices. The detectors exhibit low dark current < 1 nA at -10 V. The capacitance of the order of 1 pF on n^+ InP has been reduced to ~ 0.3 pF on semi-insulating InP and using an air bridge technology to isolate the bonding pads.

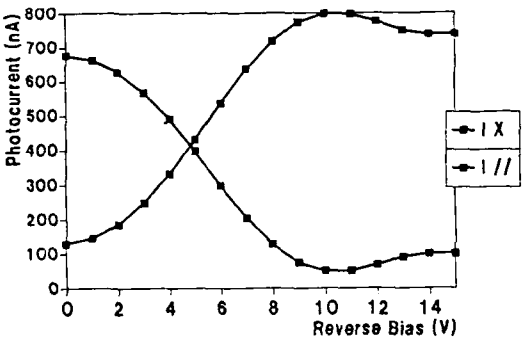


Figure 6: Switching characteristic at 1.52 μm (TE polarization) of the correlation switch (second switch) recorded with the integrated detectors. The CDDC-PAN switch is in the listening state (the access switch is unbiased).

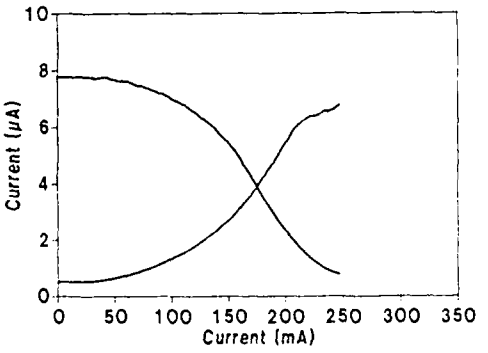


Figure 7: Switching characteristic at 1.52 μm of a TIR switch (2° angle) recorded with the integrated detectors.

Preliminary high frequency tests have shown that in the first generation of CDDC-PANs grown on n^+ InP the speed is limited to 600 MHz due to a high switch capacitance (3pF/mm) (6).

Further improvement of the characteristics of the PAN switches is currently under investigation. Especially, the use of semi-insulating substrates is meant to reduce the capacitances and to lead to higher speed devices. Also, the adjustment of the composition of the quaternary of the waveguide (7) to increase the bandfilling effect in the devices is expected to lower the driving voltage of CDDC and driving current of TIR switches. By increasing the bandgap wavelength of the GaInAsP waveguide material from 1.24 μm to 1.4 μm, the efficiency of the refractive index change at 1.52 μm produced by carrier injection increases as illustrated on Figure 8.

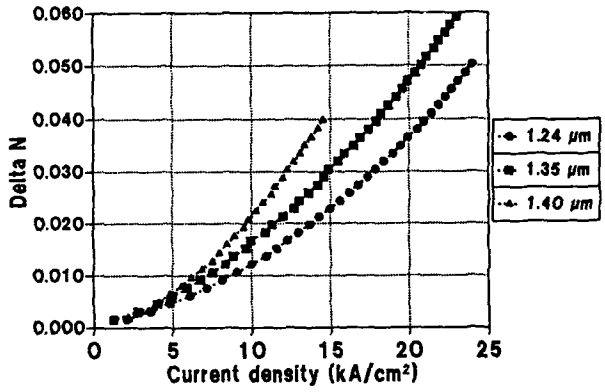


Figure 8: Refractive index change produced at 1.52 μm by carrier injection for various compositions of the GaInAsP waveguide. Same efficiency is measured in TE and TM polarizations.

However, when the composition of the waveguide material get too close to the test wavelength (1.52 μm), the losses are also increased. The best compromise has been found for 1.35 μm where the waveguide losses are still below 1dB/cm.

Conclusion

Passive Access Node Switches, consisting in two cascaded switches and two detectors have been monolithically integrated on InP substrates and functionalities have been demonstrated with both CDDC and TIR technologies.

Acknowledgments

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Wavelength-Division Switching

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Capacity of Multiwavelength Optical-Star Packet Switches

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ABSTRACT

We consider here the capacity of multiwavelength optical star networks as applied to high-speed packet switching fabrics. We review the limits of this capacity that are imposed by the optical power budget and the tunable range of the optical components. We also analyze the limitation that is caused by insufficient bandwidth in the switch-control channel which controls the switch-element settings, such as the wavelength settings of the output port receivers.

We find that this limited switch-control bandwidth can be a major factor limiting the switch capacity, and that the packet length and the control-channel bit rate are key parameters. A comparison is made of coherent and direct detection as applied to such networks, with the finding that for ATM (Asynchronous Transfer Mode) coherent detection is not required since the switch capacity is not (for the parameters assumed) limited by the power budgets. For the case of longer packets, however, a much higher capacity can be achieved with coherent than with direct detection. Overall capacities ranging from several hundred Gbits/s to greater than one Tbit/s are projected.

I. Introduction

An issue of considerable interest in the field of high-speed network and switch design is to find the practical limits to the achievable bandwidths of switching and routing networks made of passive optical stars and multiwavelength tunable lasers and receivers. In previous work, we[1] and others[2] have discussed the limitations due to power budget limitations and available optical spectrum on the capacity of switches which use such multiwavelength optical star networks at the core of the switch fabric. Henry[2] has given an argument which illustrates a third capacity limit due to the bandwidth available within the switch for communicating the switch control functions to the crosspoint elements of the switch.

In this paper, we briefly review the power-budget and tuning-range limitations, and consider the effect on switch performance of the signaling channel. We integrate these concepts together into a composite performance picture and give two concrete examples which illustrate the impact of these limits on switch design and application.

II. Star-Network Capacity

We consider here the network shown in Fig. 1. An NxN broadcast optical star has a set of N lasers operating at a set of N unique, and fixed, wavelengths. The star itself is usually assumed to be made of several ($\log_2 N$, to be exact) stages of 2x2 fiber couplers, interconnected in such a way that each input wavelength is distributed uniformly over all of the N output fibers.

At each of the star's outputs there is a tunable receiver which is capable of tuning over the entire range of wavelengths of the input lasers. Each of these receivers must be instructed to tune to the desired wavelength for the receipt of the packet destined for that output port. This implies that there must be a communications channel for signaling and control between the input ports and each of the output port receivers. The bandwidth of that channel will limit how fast the switch can be reconfigured, and therefore becomes another limit to switch performance. Contention resolution and packet buffering are not considered here.

The switch capacity, C, is defined as

$$C = B \cdot N,$$

where, B is the bit rate of the transport through the star, and N is the number of independent wavelengths, or packets, simultaneously being transmitted through the star. N is also the size of

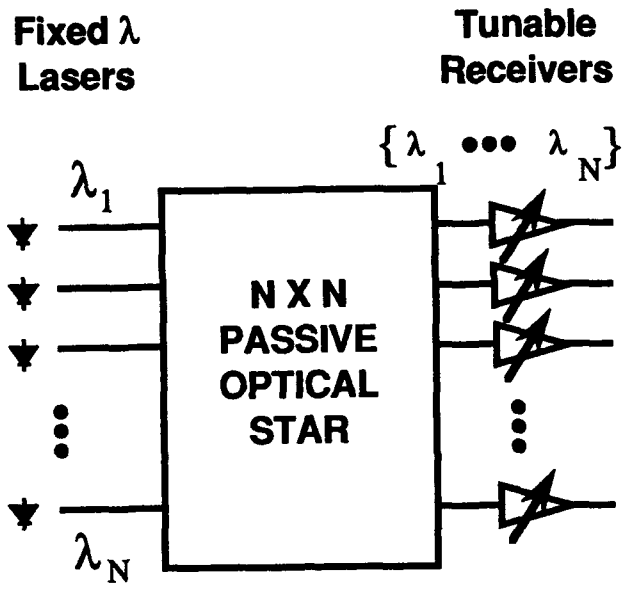


Figure 1. Multiwavelength optical star switch network with tunable receivers and fixed wavelength lasers.

the star. This definition excludes the effects of overhead and contention on the throughput of the switch.

II.1 Power Budget Limits

In Fig. 2, we show a plot of switch capacity versus star size N, including results calculated from experimental receiver sensitivity data[1] for both coherent and direct detection receivers, curves plotted as the loci of best receiver sensitivities, and a theoretical line of capacity versus N for a receiver sensitivity of 100 photons per bit. This plot is obtained by calculating the splitting loss, 1/N, which just exactly brings the total power budget to zero at a given bit rate for a given receiver sensitivity and for an assumed set of additional losses. At a constant bit rate (the line for 5 Gbit/s is shown in the figure) N may be increased up to the value for which the splitting loss is equal to the net available power budget. This is done for each experimental data point, and finally a locus is drawn representing the best results. In doing so, we have assumed a transmitter power of 1 mW, a 3 dB margin, 1 dB for connector losses, and 6 dB for filter losses. We have also accounted for the excess losses in the star coupler at a rate of 0.2 dB per stage of 2x2 couplers.

The equation for the power budget capacity limit is given by[3][2][1],

$$B \cdot N = \frac{P_T \cdot L \cdot \beta^{\log_2 N}}{h\nu \cdot n_p}, \qquad (1)$$

where P_T is the transmitted laser power, L is a loss allowance, β is the loss per stage of the star coupler, N is the size of the star, h is Plancks constant, ν is the optical frequency, and n_p is the receiver sensitivity in photons per bit. For ideal receivers, where performance is limited only by photon-counting fluctuation in the incident laser light, n_p is a constant, independent of bit rate, whose value is typically between 10 and 20, depending upon the details of the modulation and detection schemes. A value more representative of practical heterodyne receivers is $n_p = 100$ photons per bit. For lossless couplers, $\beta = 1$, resulting in B·N = 7.5 Tbits/s at a wavelength of 1.5 μm, independent of N. For lossy couplers, β is still close to 1, and B·N decreases slowly with increasing N, as shown by the dotted line in Fig. 2, for a loss of 0.2 dB per coupler. This corresponds to β = 0.955, and results in a very gradual decrease in B·N from 7.5 Tbit/s at N = 1 to B·N = 4.7 Tbit/s at N = 1024.

It is seen that the additional sensitivity of the coherent receiver is potentially very attractive for achieving very high capacitites, well beyond the limits imposed by ordinary direct detection. This is especially true at the lower bit rates (bit rate decreases as one moves to the right on this figure). Three recent data points are also shown for the use of an erbium-doped fiber amplifier with direct detection[4]. These optical amplifier results are nearly as good as the coherent detection results and represent one possible means for extending the power budget limits of direct detection systems, although it must be remembered that current fiber amplifier bandwidths limit the available spectrum to about 30 nm.

II.2 Tuning Limits

The second limit on capacity is due to the limited tuning range of the lasers or receivers. Although the fiber low-loss region extends over a wavelength range of several tens of nanometers, current tunable optoelectronic devices have a much more limited tuning range. Three-section tunable distributed Bragg reflector (DBR) laser diodes have continuous tuning ranges on the order of 3 to 4 nm, and maximum discontinuous tuning ranges of about 10 nm[5]. Some tunable filters have wider tuning ranges, but the really high-speed tunable filters[6] only exist in the form

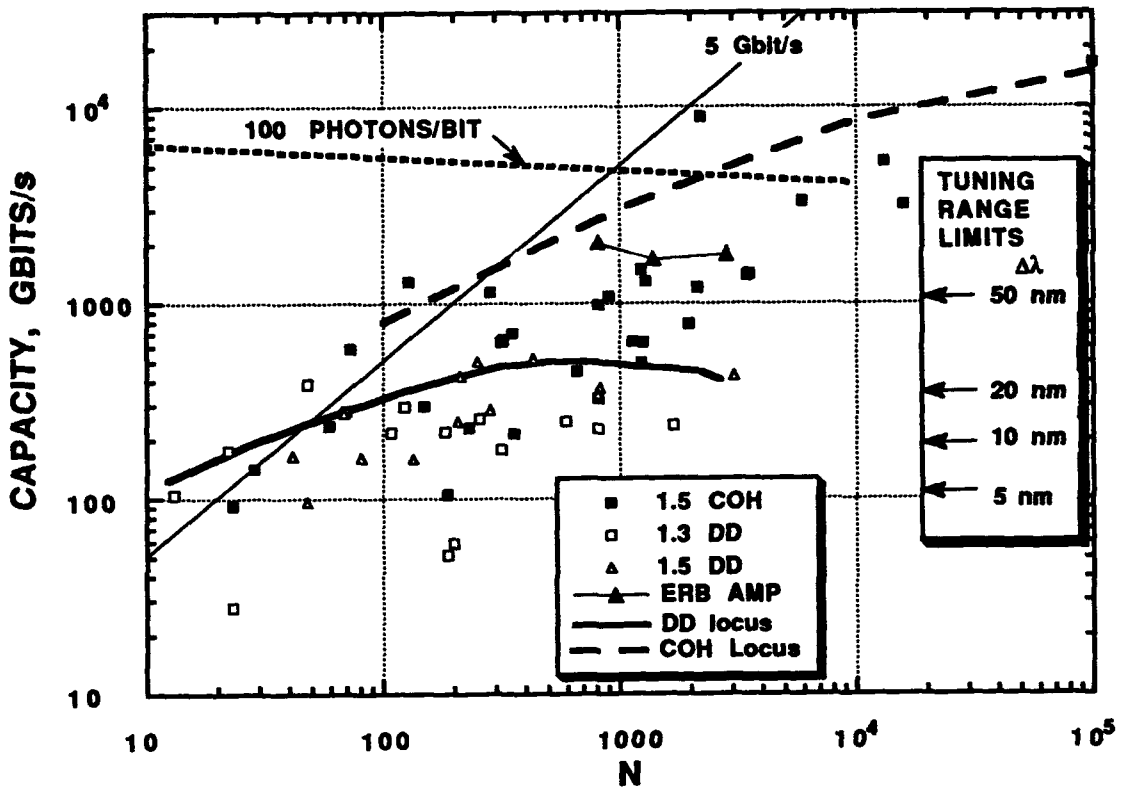


Figure 2. Experimental capacities for direct detection (DD), DD with erbium fiber amplifiers, coherent detection (COH), and their loci. Also, capacity for 100 photons per bit receiver sensitivity.

of laser diode distributed feedback (DFB) amplifiers which have very limited tuning ranges (6 Å) with only 8 independent high-speed channels having been demonstrated so far. It would appear that the most promising means for producing a high-speed tunable receiver of large channel capacity is to use coherent detection with a high speed tunable local oscillator[7].

The limited tuning range of either lasers, or receivers, gives a limit to the switch capacity given by[1]

$$B \cdot N = \Delta\Omega/\rho,$$

where $\Delta\Omega$ is the total optical frequency range over which either the laser or receiver may be tuned, and ρ is a channel-spacing factor given by the ratio of the optical channel spacing to the bit rate, $\delta\nu/B$. The value of ρ commonly ranges from 10 to 20 in research experiments. The value of ρ determines the crosstalk between channels. Theoretical values as low as $\rho = 2$ have been predicted for crosstalk penalties less than 0.5 dB[8]. A value of $\rho = 6$ is assumed here. This gives the set of tuning limits shown in Fig. 2, for various tuning ranges. It is seen that for current values of tuning ranges in the 5 to 10 nm range, the tuning limits are much more restrictive than the power budget limits. It is reasonable to assume that considerable improvement in the tuning range limits will be possible.

II.3 Signaling Limits

We now consider the limits imposed by the communications bandwidth available within the switch to *communicate* the desired switch settings to the switching elements, whether they are electronic or optical, and whether they are arranged in an NxN crosspoint array, or in a set of tuned receivers as shown in Fig. 1. This generality derives from the fact that the switching process in its essence consists of sorting N inputs into N outputs. This requires an address specification of $\log_2 N$ bits for each address, or $N\log_2 N$ bits altogether to set the entire switch. In

the case of output-port receiver tuning, these bits must be communicated to the output ports to tell the receivers to which input wavelength to tune. Note, however, that we are not including the time required to compute the new switch settings, that is, to resolve the contention for the output ports.

If C is the overall switch capacity, N is the number of inputs, and P is the length of a packet, then $C = N \cdot P/T_s$, where T_s is the time the signaling channel takes to transmit all of the packet addresses to the output ports. Each packet requires $\log_2 N$ address bits. If the rate of packet transmission is $N \cdot B/P$, then the required capacity of the signaling channel is

$$C_s = \frac{N \cdot B}{P} \cdot \log_2 N,$$

or,

$$\frac{C_s}{C} = \frac{\log_2 N}{P}. \qquad (2)$$

The switch capacity C can then be written

$$C = C_s \cdot \frac{P}{\log_2 N} = K \cdot \frac{PB_s}{\log_2 N}, \qquad (3)$$

where B_s is the bit rate of each of the signaling channels, and K is the number of the signaling channels.

We examine two special cases of Eq. 3. The first is for K = 1, the one-bit-bus, and the second is for $K = \log_2 N$, the $\log_2 N$-bit-bus.

$$\text{CASE I:} \quad C = \frac{P \cdot B_s}{\log_2 N} \quad [\text{one-bit-bus}], \qquad (4)$$

$$\text{CASE II:} \quad C = P \cdot B_s \quad [\log_2 N\text{-bit-bus}]. \qquad (5)$$

It is seen that a critical parameter in both cases is the product of the packet length and the signaling channel bit rate, PB_s. One would normally choose B_s as large as is practical for the technology of choice, but the packet length is usually dictated by issues outside the realm of technology, such as the desired service needs and standards issues. We consider the effect of packet length in the next section.

Equation (2) gives the signaling channel capacity, C_s, required to achieve any switch capacity, C, in terms of the size of the network, N, and the packet length P. If C is taken to be the power budget limit associated with a receiver sensitivity of n_p photons per bit, Eq. (1) gives the result

$$C_s = \frac{P_T \cdot L}{h\nu n_p P} \cdot \log_2 N \cdot \beta^{\log_2 N}. \qquad (6)$$

A critical factor in Eq. (6) is the packet length, P. In the next section we will discuss two examples: ATM, for which P is 424 bits; and Data, for which P is assumed to be 16,000 bits. The result of these two widely divergent assumptions for the same 100 photons per bit receiver as earlier is shown in Fig. 3, in which the required control channel capacity is plotted versus the size of the network, N. Whereas for ATM, a control channel capacity of approximately 100 Gbits/s is required, for the Data case, a control channel capacity of only a few Gbits/s is sufficient. This serves to emphasize the importance of the packet length on the overall capacity of the switch, and illustrates the relative difficulty of achieving the full power budget limited capacity of networks of this type.

III. ATM and Data Transmission Examples

Two examples which lie at almost the extreme opposite ends of the packet length range are the cases of ATM (Asynchronous Transfer Mode) and computer data transfer, refered to here simply as "Data." For ATM, the packet length P has been set at 48 bytes of data plus 5 bytes of header, which gives a total of 53 bytes or 424 bits for P. For Data, we assume for contrast a packet length of 2000 bytes. We also assume a signaling bit rate B_s = 1Gbit/s. We therefore obtain

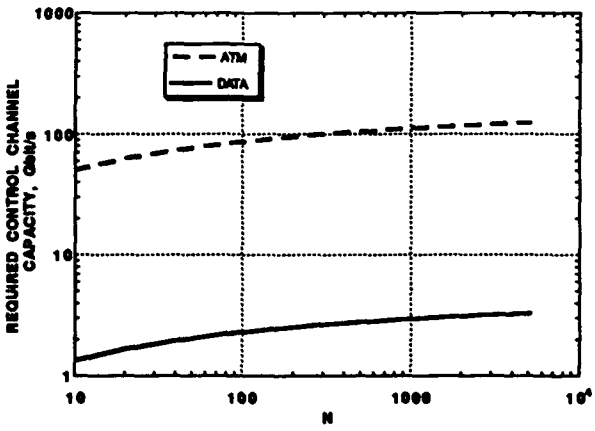


Figure 3. The control channel capacity required to achieve the power-budget limited star capacity for a transmitter power of 1 mw and receiver sensitivity of 100 photons/bit."

ATM: $P \cdot B_s = 424$ Gbits/s,

Data: $P \cdot B_s = 16$ Tbits/s.

In Fig. 4, we have plotted the four combinations of ATM and Data transmission using both the one-bit-bus and the $\log_2$N-bit-bus, assuming that the bit rate for the actual optical transmission through the star is B = 5 Gbits/s.

Consider first the ATM case. For small N, the capacity is just given by the product of B and N, and increases linearly with N. For the one-bit-bus, at a relatively low value of N = 20, the one-bit-bus limit is encountered. At higher values of N, the capacity decreases logarithmically with N, the maximum capacity being about 100 Gbits/s at N = 20.

Still considering ATM, but with a $\log_2$N bit-wide-bus, the signaling limit is not encountered until N = 85, above which the capacity C stays constant at a value of 424 Gbits/s ($P \cdot B_s$). In neither of these ATM cases do the power budgets play a significant factor in limiting the switch capacity, but a significant improvement in capacity may be had by going to the parallel bus structure.

On the other hand, for the Data case, where the packets are 2000 bytes long, the situation is changed. Referring to Fig. 4, it is seen that for increasing N the capacity is limited by the power budgets for N beyond about 100. For Direct Detection, this is true for all N > 100, and the capacity peaks out at less than 1 Tbit/s at N ~ 600. For the Coherent case, the power budget limit continues to increase for all N shown on the figure. The signaling limit does restrict the capacity if a one-bit-bus is used, but not until the capacity has reached well past the 1 Tbit/s level.

Also, in the Data example, the use of an erbium fiber amplifier with direct detection appears to achieve all of the capacity that the 1-bit bus will allow.

The impact of these examples can be summarized as follows (with the assumptions on operating and signaling bit rates, and packet length):

1. For short packets such as in ATM, the power budget limitations on optical star networks are not likely to be the limiting factors. Instead, the signaling bandwidth within the switch is much more significant, and the benefit from going to a parallel bus structure for that signaling is dominant. In particular, there is not much point in using coherent transmission, with the possible exception of achieving high-speed tuning.

   In addition, there is no real reason for going to large star size; the full benefit of the star network is achieved for N ~ 100.

2. For long packets such as in computer data transactions, the power budgets do matter, and coherent is advisable if maximizing the capacity is the objective, however, using an erbium doped fiber amplifier with direct detection may still achieve the same capacity. In either case, star sizes of N ~ 1000 - 4000 are required if maximum capacity is the goal.

   The signaling limit does imply that at the extreme of large N a benefit is had from going to a parallel bus for signaling, but the need here is not as imperative as it was in the ATM case. It might in fact be better to work to increase the signaling bit rate, B_s, than to try to implement the parallel bus.

IV. Summary

We have considered the limitations to capacity of a multiwavelength optical star packet switch, and in particular the limit imposed by insufficient bandwidth in the signaling or control channel which tells the output port tunable receivers to which wavelength they should tune. We have found that much depends on the packet length, and in particular the product of the packet length P and the signaling channel bit rate B_s. For short packets, such as in ATM, the power budgets are not a significant factor, and the bandwidth of the signalling channel is dominant. Increasing that bandwidth by the use of a parallel bus is indicated.

For long packets, the example used was P = 2000 bytes, the power budget is much more important and the signaling channel less so. In this case, coherent detection adds significantly to the total switch capacity.

The comparison between capacities achievable for the ATM and Data cases indicates that it will be difficult to utilize the capabilities of the emergent multiwavelength technology to its fullest in switches designed to carry ATM cells of the current cell length. There are still advantages to the optical designs for ATM, however, which

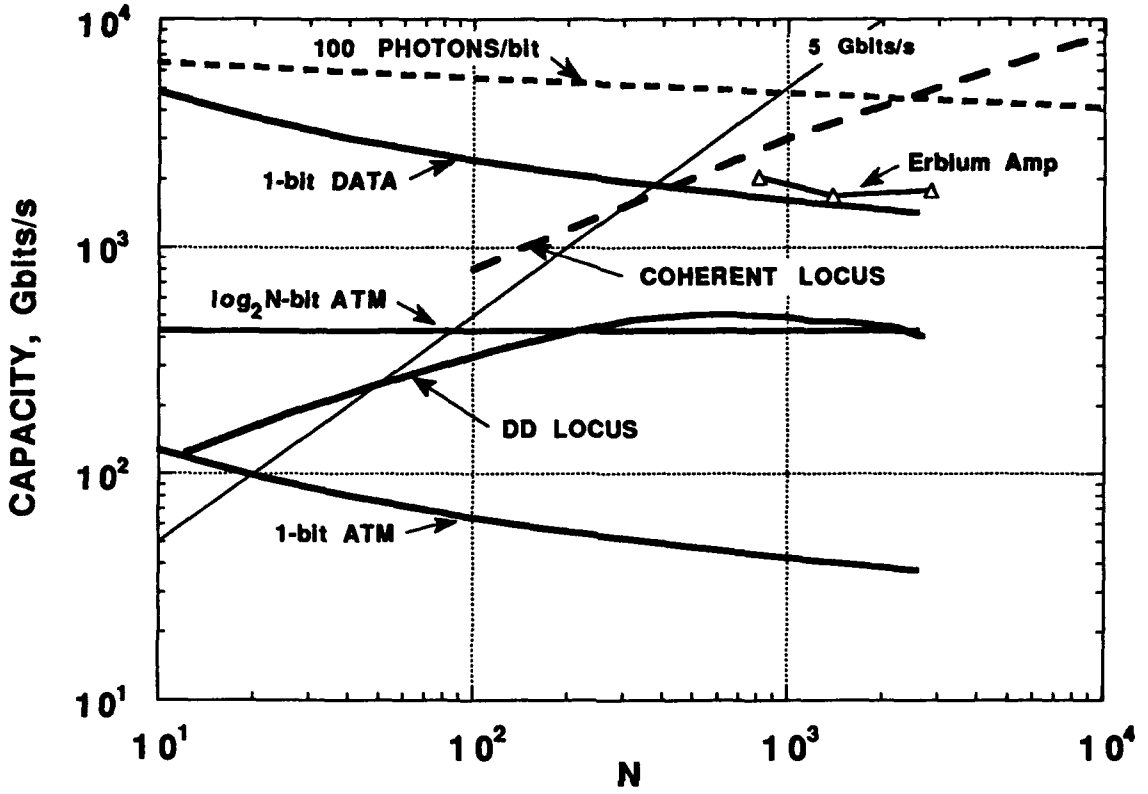


Figure 4. Combined capacity limits due to power budgets and signaling for both ATM and DATA examples.

include the potential for several hundred Gbit/s switches in a single stage, with a simple means for implementing broadcast, selective multicast, and prioritized traffic types.

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Fast Optical Triggering and Wavelength Switching using a Distributed Bragg Reflector Laser with a Saturable Absorber

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Abstract

An integrated wavelength converter based on a DBR laser including a saturable absorber is presented. Optical triggering with nanosecond reponse time has been recorded with 100 μW optical control power. Also, 1 ns duration wavelength switching between two adjacent modes has been achieved.

Introduction

Recent advances in the field of tunable semiconductor lasers have stimulated research studies on new optical switching concepts and architectures making efficient use of the wavelength domain.

In the specific case of ATM-type systems, cells (data packets) can be encoded in the wavelength domain so as to determine a physical path through the switching network (wavelength routing) [1,2,5].

However, the useful tuning range of semiconductor lasers is still restricted to 10-20 nm and thus the capacity of any switch fabric based on wavelength routing remains somewhat limited, in terms of number of available wavelength multiplexed channels.

In order to increase further this capacity, the integrated wavelength converter (IWC), recently demonstrated by Kondo et al [3], is an attractive device which can be used, for instance, as an optical gateway between stages of a multistage wavelength switching network.

The IWC is a tunable laser which can be optically triggered by external light; if this external signal is carrying binary data via intensity modulation, the IWC translates the incoming signal into an image signal, the wavelength of which can be tuned by electrical means. Thus wavelength conversion is being achieved by using a single component.

The aim of this paper is to present new results on high speed optical triggering and wavelength switching using an IWC based on a new laser featuring a DBR-type structure in conjunction with a saturable absorber section.

Characteristics of the laser

The laser, made by 3-step LPE, has a 3-section active-passive DBR [4] structure, as represented in figure 1, and is driven by 3 independent current sources through 3 isolated electrodes. A special design of the electrode pattern [6] allows for non-uniform pumping of the active (amplifying) section, a part of which is behaving as a saturable absorber. The role of the center section actually is to adjust the saturable absorber characteristics; thus, it will be referred to as the saturable absorber control (SAC) section.

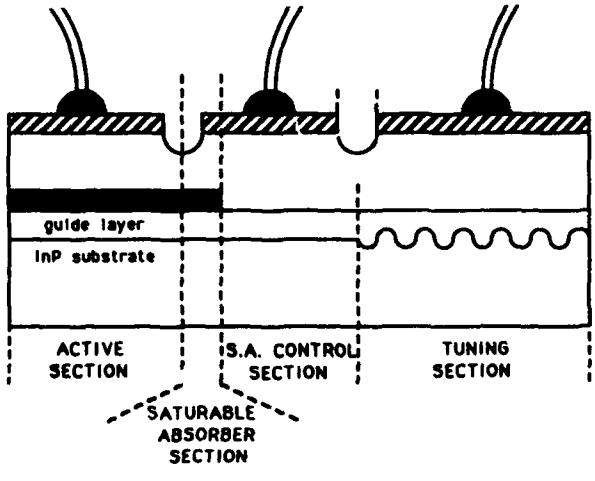


Figure 1 : 3-section DBR laser including a saturable absorber

The lengths of the active section, the SAC section and the Bragg section respectively are 300 µm, 100 µm and 500 µm. The saturable absorber zone is 10 µm long. The threshold current typically is 50 mA and wavelength tuning over 24 Å, involving 3 modes, has been obtained. Continuous tuning is limited to 12 Å.

The L-I characteristic exhibits a bistable region for a range of values of the drive current in the active section; the width of the bistable region can be modified by tuning the drive current in the SAC section, as represented in figure 2.

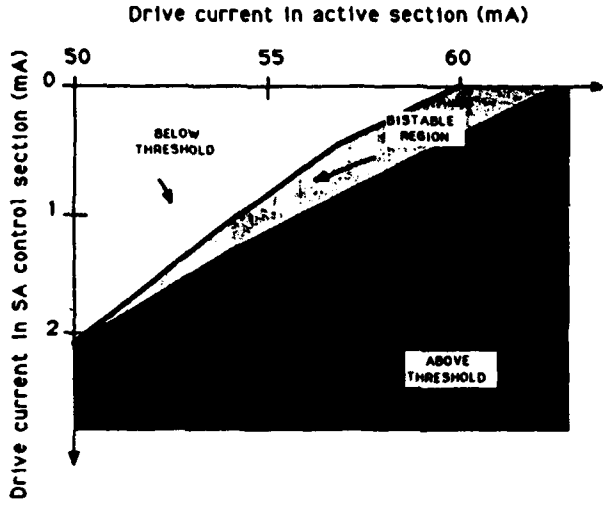


Figure 2 : Bistable operation conditions

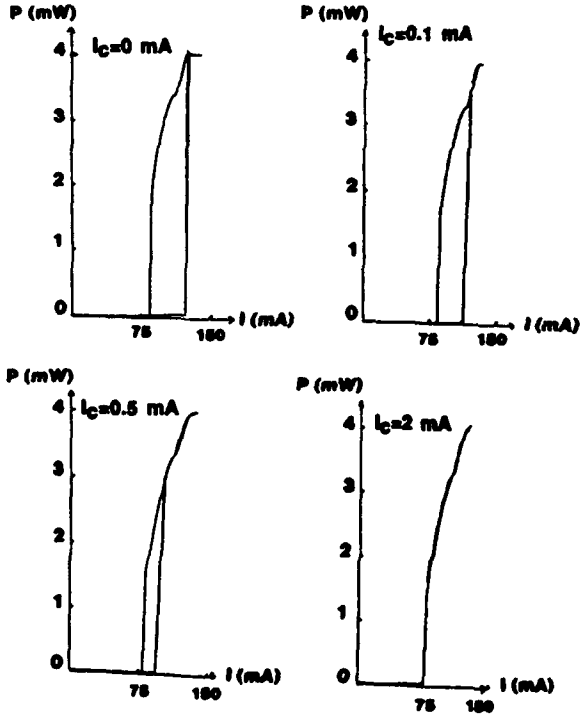


Figure 3 : Control of hysteresis cycle : I : current in active section, Ic: current in SAC section.

nsequence, the tuning of the drive current in th... section modifies the width of the hysteresis cycle which is characteristic of the bistable regime.

Figure 3 shows that the bistable operation conditions can be adjusted with a remarkably low value of this current: no hysteresis can be seen when the current exceeds 2mA.

Experimental Set-Up

The experimental set-up is represented in figure 4. The laser is electrically-controlled via a PC computer. We have designed and built up a specific circuit for the control of the lasing wavelength. The values of the drive current corresponding to the various lasing modes (ie the different wavelengths) were stored into an electronic memory. The control circuit basically consisted of a RAM and a 200 MHz digital-to-analog converter in order to transform binary data into actual drive voltage values; a driver circuit was located close to the chip.

The optical control of the laser chip was achieved by launching into it the optical wave emitted by a conventional DFB laser (control laser). Tapered fibers have been used to provide good coupling efficiencies.

The wavelength switching speed measurements have been realised by means of a Fabry-Perot filter, which was used to convert wavelength modulation into intensity modulation.

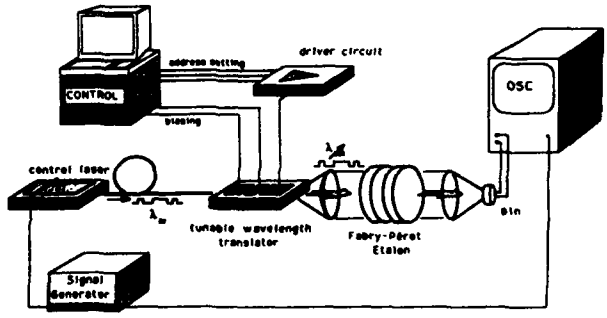


Figure 4 : Experimental Set-Up

Optical triggering

For the optical triggering experiments, the laser was biased below threshold and close to the bistable operation (electrical) conditions (see figure 2). The laser could be switched on and switched off by applying about 100 microwatt peak power optical trigger pulses (launched into the chip). The emitted power, when the laser was switched on, was depending on the actual biasing conditions : when the drive current into the SAC section was decreased down to zero, the emitted power in the on state was observed to increase up to 3 mW.

Figure 5 shows the optical triggering process at low rate (10 kHz) and the characteristic reshaping of the incoming signal. The control laser was modulated by a sine wave.

Figure 6 shows high rate operation (100 MHz). Optical triggering has been observed up to 300 MHz repetition rate, limited by the pulse generator driving the control laser.

The ultimate speed of the process has been evaluated by driving the control laser by means of a low - repetition rate fast rise time pulse generator. The results are shown in figure 7 (optical control pulses with 200 ps rise time) and figure 8 (triggered output signal with about 500 ps rise time).

As expected, the rise time was depending on the peak power of the control laser : for a 50 μW peak power control pulse, the rise time of the triggered pulses was about 1 ns.

The optical triggering has been found to be polarisation insensitive, proving that the physical mechanism involved in the process relies on absorption of the trigger light.

Wavelength switching

Wavelength switching has been investigated following the step tuning approach, which we consider to be the most promising for future applications.

A Fabry-Perot interferometer, with 3000 GHz free spectral range and a finesse in the order of 50, has been inserted between the laser under test and the photodetector. By adjusting the electrical drive voltage of the interferometer, it was possible to use the transmission peak as a wavelength discriminator, although the non-linear transfer function was a limiting factor for accurate measurements.

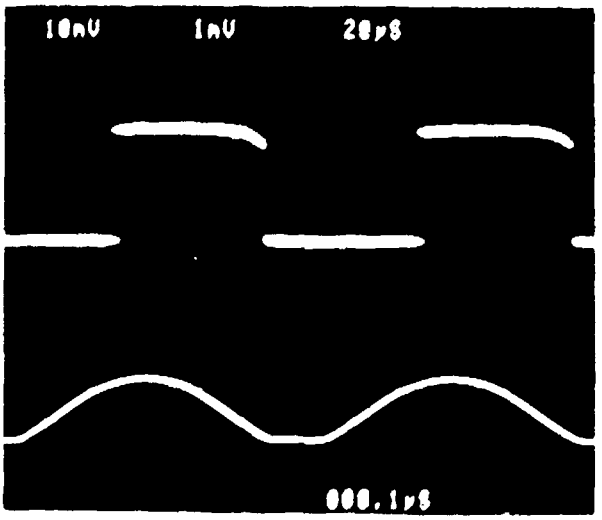


Figure 5: Optical triggering at low rate :
bottom trace: optical control signal,
top trace : triggered optical output

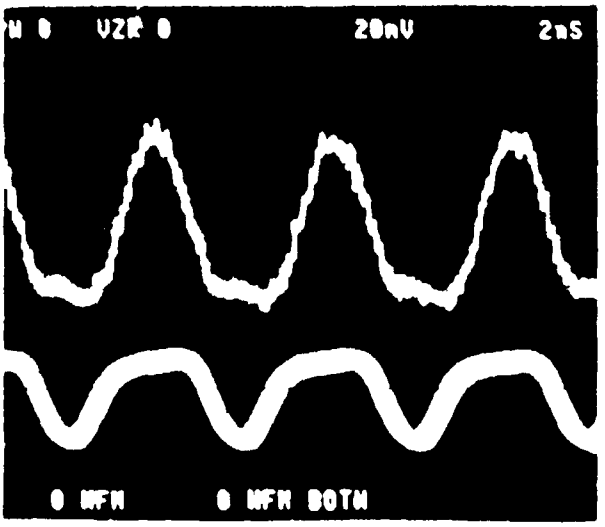


Figure 6: Optical triggering at high rate :
bottom trace: optical control signal,
top trace: triggered output signal

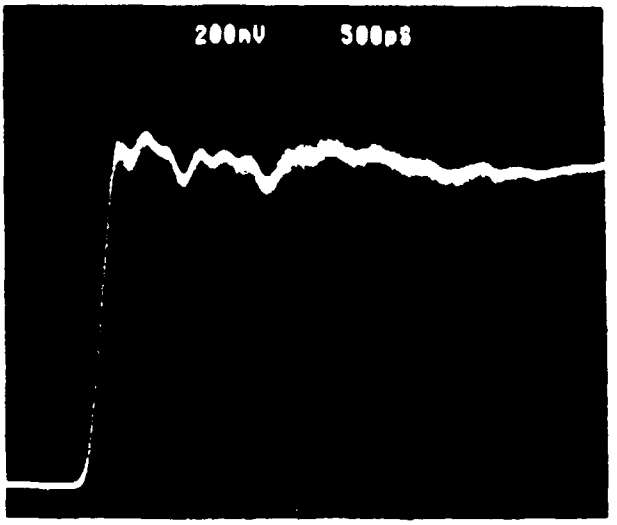


Figure 7 : Optical control signal :
rise time : 200 ps, peak power 100 μW

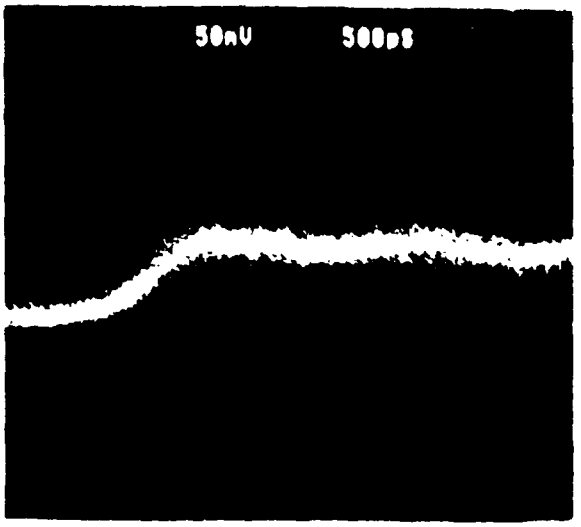


Figure 8 : Triggered output signal
rise time : 500 ps

Figure 9 shows the risetime of the electrical drive signal, which is about 2 ns, limited by the Digital-to-Analog converter speed, with 20 mA amplitude.

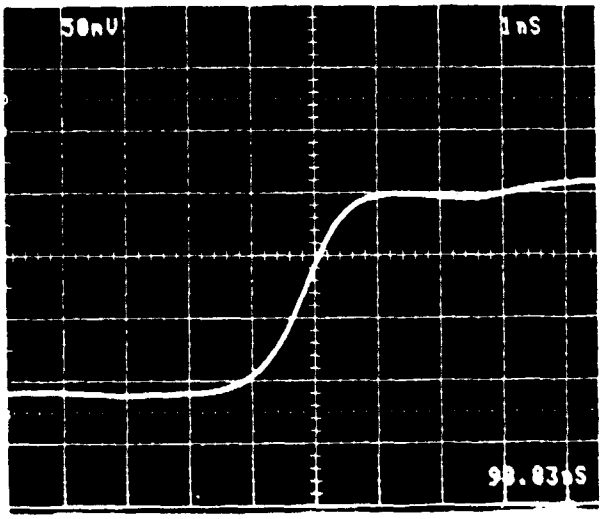


Figure 9: Wavelength switching :
Electrical control pulse.

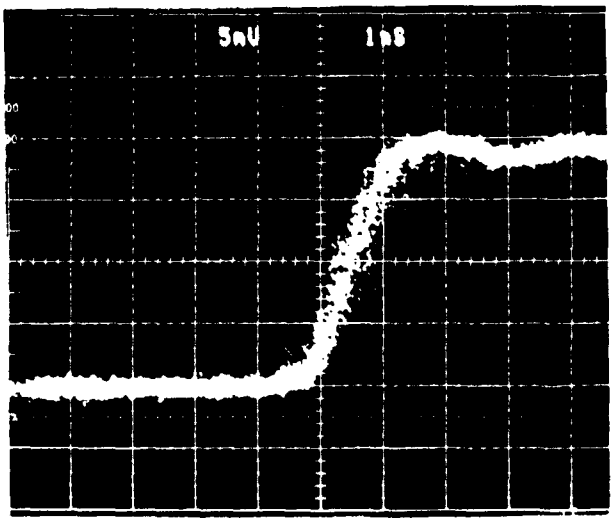


Figure 10: Wavelength switching :
Optical output after conversion from wavelength modulation to intensity modulation : the rise time of the oscilloscope trace represents the duration of the tuning process, with good accuracy.

Figure 10 shows a 1 ns typical response time for the switching between two adjacent modes . This result shows that the step tuning approach (mode hops) can provide characteristic response times depending only on the laser characteristics, as the observed tuning duration is less than the rise time of the electrical control.

Conclusion

We have reported new results on fast optical triggering and wavelength switching using a 3-section DBR laser with a saturable absorber region. The device has exhibited interesting features, especially a small optical control power, of the order of 100 μW, and nanosecond (wavelength switching) or sub-nanosecond (optical triggering) response times.

. The typical operation speed recorded here suggests that such a component could be adequate for ATM-type optical switching at about 600 Mbit/s.

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Error-Free Operation of Wavelength Conversion Laser for Multistage Photonic Cross-Connect Node

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Abstract

A wavelength conversion laser application to wavelength-division photonic cross-connect system is presented. We successfully achieved error-free operation in wavelength switching at a 125-Mbit/s data rate.

1. Introduction

B-ISDN requires a throughput in excess of 50 Gbit/s, even in a subscriber loop for full-motion video transmission. To provide the network capacity and to provide flexibility, optical signal processing technology is used, especially that of optical wavelength-division multiplexing. We have already proposed such configuration of photonic cross-connect nodes that perform non-blocking cross-connection with two stages by utilizing multi-wavelength selective filters(MWSFs)[1]. In our proposed configuration, a large capacity can be provided with multistage connection, and signal wavelength conversion will be essential at the connecting stage between two groups of the basic switches when connected by multiple stages. In the connecting stage, use of wavelength conversion devices (WCDs) such as wavelength conversion lasers(WCLDs) has the advantage of hardware scale reduction in large-scale connecting systems, thus eliminating electronic circuits such as O/E or E/O converters.

In this paper, we report the first error-free operation of our WCLD[2] in optical signal wavelength conversion. We have successfully achieved its wavelength switching at a data rate of 125 Mbit/s, and have shown the applicability of the device to large-scale photonic cross-connect systems, together with cross-connect channel number estimation.

2. Multistage connection of photonic cross-connect node

Fig. 1 shows one of the multistage configurations for our proposed photonic cross-connect system[1]. At the interswitch connection stage, wavelength multiplexed optical signals transmitted through wavelength multiplexed link from the 1st basic switch are distributed to the MWSFs by optical star coupler and only the desired wavelength signals are sent to the star coupler and then wavelength selective filter(WSF) corresponding to the desired 2nd basic switch. Each signal through each WSF is wavelength-converted at WCD and transmitted to the 2nd basic switch through the link. The switching or connecting principle in the 2nd switch is the same as for the 1st. In this multistage connection, wavelength conversion for the 2nd switch is achieved without O/E conversion.

The channel number in each basic switch is defined by the number of multiplexed wavelengths in the switch board. The maximum number of cross-connect channels in this system for m-multiplexed wavelengths is given as m^3.

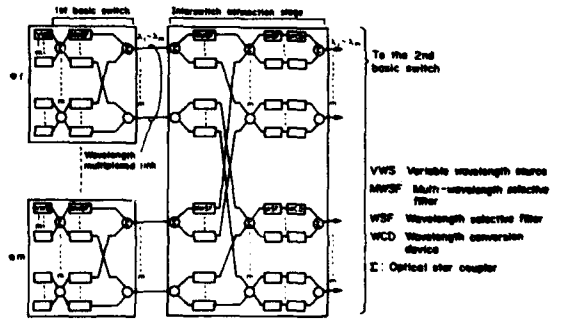


Figure 1. $m^3 \times m^3$ multistage photonic cross-connect node configuration

3. Wavelength conversion experiments with a WCLD

When WCLDs are used as WCDs in the inter-switch connection stage described above, the cross-connect channel number is limited by the optical input and output level of WCLD for wavelength conversion. We conducted experiments on wavelength conversion with WCLD.

3-1 Experimental setup

The setup for the wavelength conversion experiment with a WCLD is shown in Fig. 2. The input and output signals use a directional-division scheme, namely the output signal from the WCLD is taken out by lens coupling at the same active region facet that the signal is injected. The reason for this is, for the WCLD sample we tested, the optical output power from the DBR region facet was less than that from the active region facet by more than 6 dB, so that it gets some drawback to output the wavelength-converted signal from the WCLD's DBR region facet for optical output level margin in the stages following WCLD. This is because the optical power-splitting loss is the one factor that limits the cross-connect channel number after WCLD. In this setup, the input and output signals are attenuated by 3 dB through the optical coupler, but the output level is still 3 dB-plus more than from DBR region by the simpler optical coupling system.

The input signal wavelength λ_{in} is 1.52788 μm, and the data rate is 125 Mbit/s(RZ). Input signal polarization is set to TE injection to WCLD with the polarization controller(PC).

The output signal is put into O/E through an optical band-pass filter(BPF) (10-nm FWHM) and only the wavelength-converted signal is received at the O/E for error detection.

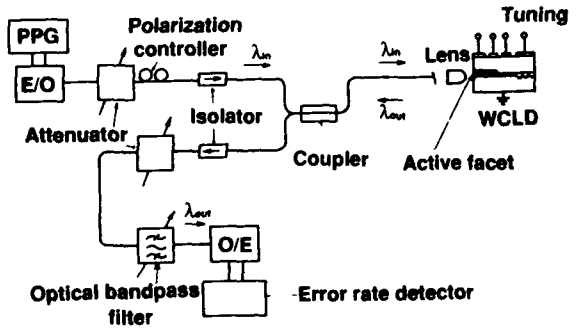


Figure 2. Wavelength conversion experiment setup

3-2 Experimental results

The optical output waveform of WCLD under wavelength conversion operation is shown in Fig. 3. The input signal is wavelength-converted and put out with good eye opening. Figure 4 shows the error rate characteristics of the WCLD output signals when the converted output wavelengths (λ_{out}) are 1.53672 and 1.53760 μm. Error-free operation with error rates below 10^{-10} was confirmed for both outputs. The receiver sensitivities at 10^{-9} of the error rate were -37.6 and -36.7 dBm, and power penalties from E/O to O/E direct transmission without the WCLD were 2.0 and 2.9 dB. This power penalty is mainly due to the on-off ratio of WCLD with different current bias conditions.

Under this type of setup, the output level margin for optical loss from the optical coupler output to O/E sensitivity was measured as 16 dB.



H: 2 ns/div.

Figure 3. WCLD output waveform (λ_{out}=1.53672 μm)

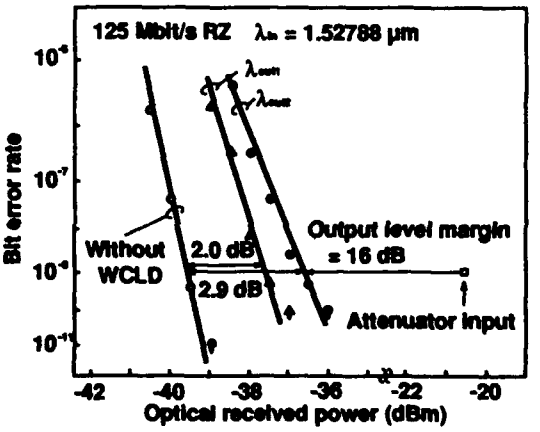


Figure 4. Error rate characteristics of wavelength-converted output

4. Estimation of maximum number for cross-connect channels

The maximum number of cross-connect channels after WCLD can be estimated based on the output level margin of WCLD. Assume that the effective gain/loss at the MWSF and WSF after WCLD is 0 dB. The O/E receiving optical power penalty caused by interchannel crosstalk at the filters is 1 dB, and excess loss of an optical star coupler is 0.5 dB. Fig. 5 shows the maximum channel number estimation based on the above assumption. For the 16 dB of the output level margin in the experiment, 5 channels can be connected after WCLD at each switching board. The total channel number in the system can then be estimated to be 5^3=125 under 5-wavelength mutiplexing. When WSFs show a gain with a DFB-LD type active filter[3], the cross-connect channel number increases. Suppose the effective(fiber-to-fiber) gain of WSF is 10 dB. The wavelength number m then becomes 15 and the total channel number 15^3=3,375.

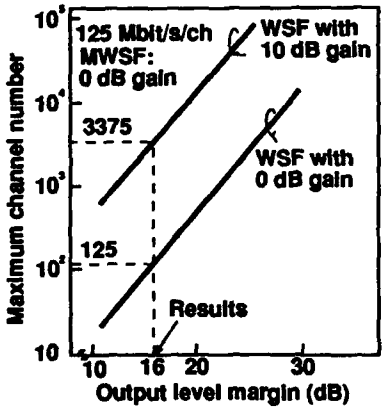


Figure 5. Maximum channel number estimation from output level margin

5. Conclusion

We conducted experiments on the applicability of WCLD to a wavelength-division photonic cross-connect system and estimated the maximum channel number for the system. Error-free operation of optical wavelength conversion was confirmed at a data rate of 125 Mbit/s, and WCLD has proved to have functionality for making high-throughput cross-connect nodes a reality.

Acknowledgments

The authors wish to thank Dr. H. Takanashi, Dr. T. Sakurai, Dr. S. Yamakoshi, and T. Touge for supporting their work.

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Wide-Wavelength-Tunable Active Filter with a λ/4-Shifted Distributed Feedback Structure with Independently Current-Injected Tuning Waveguide

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Introduction

Wavelength division multiplexing of optical signals has attracted increasing interest in fiber communication and photonic switching systems for the large amount of signals that can be processed. Wavelength tunable filters are indispensable for the selection of multiplexed optical signals, with tunability one of the most significant characteristics because this limits the number of signal channels.

DFB active filters have several advantages over passive filters. Their amplification exceeds 10 dB, and they have a narrow transmission bandwidth below 0.1 nm when biased just below the threshold. Electrical wavelength-tunability exceeding 1 nm is achieved by using current injection and a variety of waveguide structures.

The two major structures reported thus far for DFB widely tunable active filters with different tuning mechanisms are shown in Fig. 1.

In the phase-shift-controlled DFB structure in (a), tuning was done with effective change of the phase-shift of corrugation with refractive index change by current-injection in the tuning layer of the center region [1]. The transmission spectrum changes its shape in the stopband region as shown schematically in the figure. A 0.95 nm tunability has been reported[1]. This electrical tunability is limited by the stopband width, however, and a large improvement is not expected. In the same way, a two-section Fabry-Perot filter[2] with 1.5 nm tunability has the limitation of its mode-spacing.

In the tunable twin-guide-distributed feedback (TTG-DFB) structure[3] in (b), the tuning layer is formed above a conventional DFB laser structure. The currents to the tuning and active layers can be independently injected into each region. Tuning is done by equivalent refractive-index changing by current-injection in the tuning layer. The transmission spectrum shifts over its stopband without changing shape. This structure is expected to provide wide tunability. A 1.35 nm tunability with TTG-DFB structures have been demonstrated[3]. The limitation of the tuning was due to the insufficient suppression of the second-peak transmission gain. To achieve wide tunability, suppression of other wavelengths except the transmission wavelength is important. When the second-peak transmission gain can be suppressed, tuning can be extended over a second peak wavelength.

In this paper, we demonstrate a 1.55 μm-wavelength active filter with a wavelength-tunability of more than 4 nm using a λ/4-shifted DFB structure. An 1.4-μm-composition tuning waveguide layer with independent current injection and a λ/4-shifted corrugation with a large coupling coefficient were adopted. Structure, fabrication, and the characteristics of the filter are described.

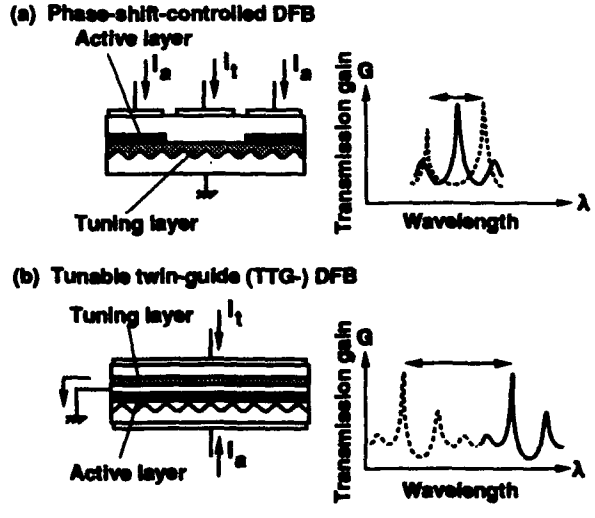


Figure 1. Schematic structures of two tunable DFB active filters : (a) phase-shift-controlled DFB structure, and (b) tunable twin-guide- (TTG-)DFB structure

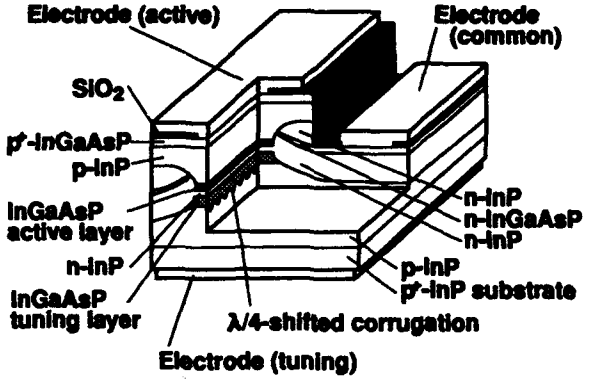


Figure 2. Schematic of the fabricated filter. Outer mesas are not shown for simplicity.

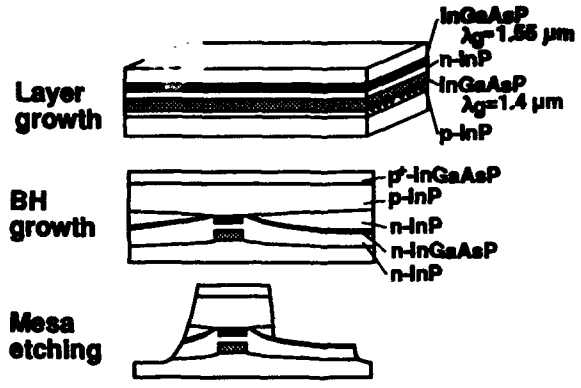


Figure 3. Fabrication process of the filter. After these process electrodes in Fig.3 was formed.

Structure of the Fabricated DFB Filter

Figure 2 is a schematic of the filter we fabricated. This structure is basically similar to the TTG structure. The structure consists of an independently current-injected tuning waveguide layer and an active layer. The tuning and active layers are separated by an n-InP layer on a p^+-InP substrate.

We adopted two specific features to improve the suppression of the sencond peak gain. One puts the independently current-injected tuning waveguide directly over the corrugation. This structure provides a large coupling coefficient for wavelength selectivity as well as a large optical confinement in the tuning layer for a wide tuning range. Second, the λ/4-shifted corrugation enables us to obtain sufficient wavelength selectivity.

We used a buried heterostructure for optical and current confinement and developed buried-heterostructure adapted for independent current injection. This is similar to the flat-surface buried heterostructure (FBH) laser structures[4]. To make the common n-type-electrode, the embedding layers beside the active and tuning layers are n-type. The key is the use of a quaternary etch-stop layer between the n-InP layers. This structure enabled a flexible current blocking structure with a common electrode.

Fabrication

The fabrication process is shown in Fig.3. The structure was formed by four-step liquid-phase epitaxy (LPE).

First, a p-InP buffer layer was grown on a p^+-InP substrate. The λ/4-shifted corrugation was formed about 60 nm deep. The coupling coefficient was evaluated to be 70-80 cm^{-1} by comparing experimental and calculated spontaneous-emission or transmission spectra.

Next, a 1.4-μm-composition InGaAsP tuning layer, an n-type InP separation layer, and a 1.55-μm-composition InGaAsP active layer were grown on the p-InP buffer layer with the λ/4-shifted corrugation. To increase the wavelength tunability the 1.4-μm-composition layer was used to the tuning layer for a large refractive-index change by the band-filling effect. The. tuning layer thickness, n-InP separation, and active layer were about 0.3 μm, 0.15 μm, and 0.15 μm, respectively.

A buried heterostructure was formed using two-step LPE growth as in Ref. 4. This included n-InP, n-InGaAsP etchi-stop, n-InP, p-InP, and p-InGaAsP contact layers. The active layer was about 1.2 μm wide.

Next, two-step mesa etching was done (not shown in Fig. 2 for simplicity). The first etch was selective and exposed the n-contact layer. The second etch was done down to the substrate and diminished InP junction area to decrease leakage current. The first mesa was 18 μm wide and the second 38 μm wide.

The electrodes as shown in Fig. 2 were then formed.

Facets were formed 300 μm apart with cleavage. Both facets were then AR-coated.

Characteristics

Figure 4 shows the light output versus the active layer current I_a at room temperature for several tuning layer currents I_t. With no tuning current, the threshold current

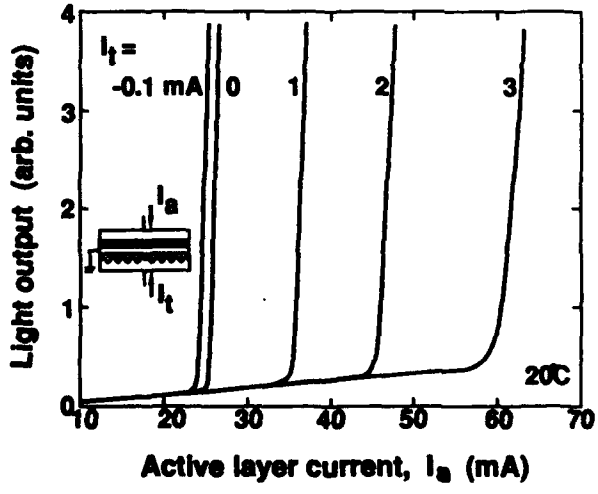


Figure 4. Light output versus active layer current Ia for several tuning layer currents It. Measurement was done at 20 °C.

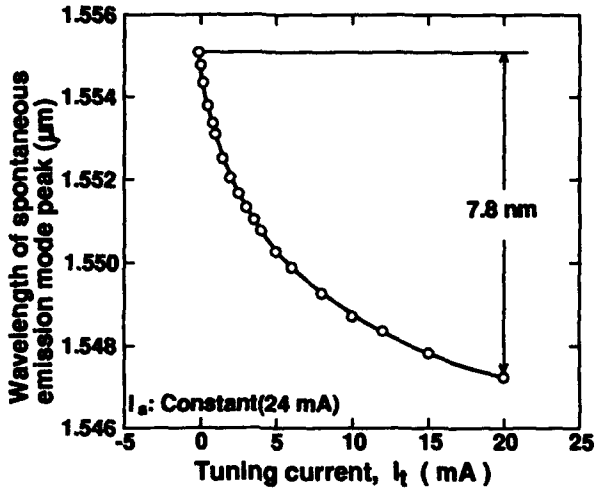


Figure 5. Wavelength shift of the spontaneous emission with tuning current. The active layer current was kept 24 mA which is below threshold for all tuning current.

was 25.4 mA. Lasing was achieved with the tuning currents from -0.1 mA to 3 mA. The device acts as an active filter when biased just below the threshold current. Tuning can be done in this tuning current region. The threshold current increased with the tuning current due to the increased optical loss in the tuning layer caused by injected carriers. At a tuning current of 3 mA, the increase of the threshold current was enlarged, presumably due to insufficient current confinement at a high bias current.

In Fig. 5, wavelength shifts in the spontaneous emission mode peak with tuning current were plotted at a fixed active layer current of 24 mA which was below the threshold for all conditions. A 7.8-nm shift can be achieved

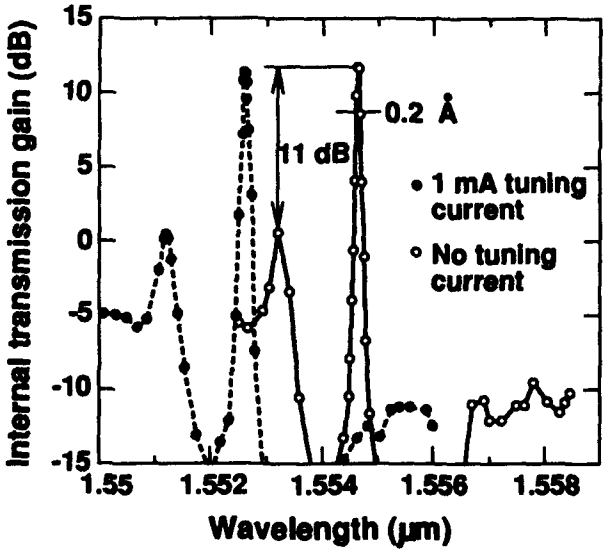


Figure 6. Measured transmission gain spectrum of the fabricated filter at no tuning layer current and 1 mA.

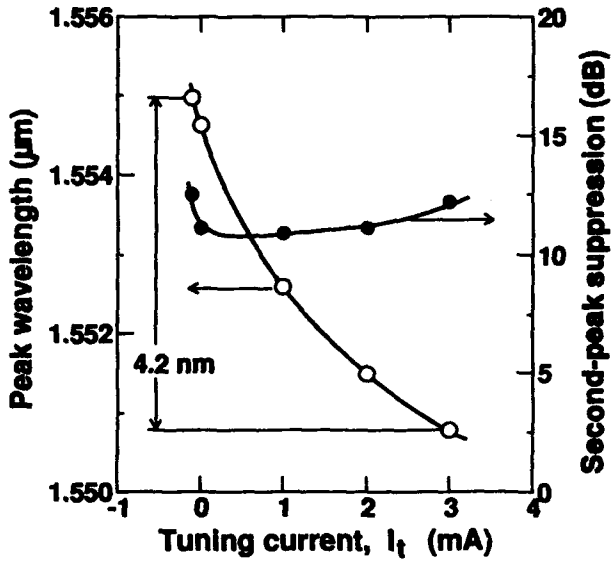


Figure 7. Transmission peak wavelength shift and second-peak suppression ratio of the filter with tuning layer current. Active layer current were changed to obtain same peak gain around each threshold current.

with a 20 mA injection.

Figure 6 shows the transmission gain spectrum of the filter for two different tuning layer currents I_t. TE polarized light was injected. Open circles show the transmission gain with no tuning current. Solid circles show the gain with 1 mA of tuning current.

With no tuning current, the active layer current was 0.98 I_{th}. The transmission gain spectrum reflected the $\lambda/4$-shifted corrugation. The transmission peak occurred almost at the center of its stopband. Transmission peak wavelengths were around 1.5546 μm. The peak gain was 12 dB and the 3 dB-bandwidth was 0.2 Å. The suppression ratio was 11 dB.

At a tuning current of 1 mA, 9.9 mA was added to the active layer current to compensate for optical loss and to achieve the same peak gain achieved with no tuning current. The peak wavelength shifted 2 nm. The transmission gain spectrum shape was maintained similar to that at no tuning current, as is expected with this device structure.

Measurements were carried out for several tuning layer currents in the same way as above. In Fig. 7, the peak wavelength and the suppression ratio of the second peak transmission gain are plotted as a function of tuning current. 4.2 nm tuning was achieved with an injection from -0.1 mA to 3 mA. This tuning width is, to our knowledge, the largest reported for active filters. The wide tuning width was attained with large suppression of the second peak gain with the $\lambda/4$-shifted corrugation and a large coupling coefficient as well as a large change of refractive index in the tuning layer (λ_g=1.4 μm). The suppression of the second peak was kept nearly constant at more than 11 dB.

The limitation of the tuning width of the fabricated filter was the increase in threshold current, with the increase of optical loss caused by current injection in the

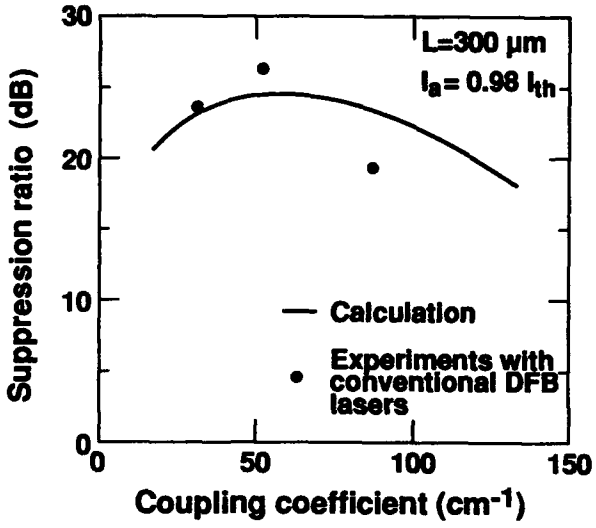


Figure 8. Calculated suppression ratio and experimental one by use of conventional λ/4–shifted DFB laser structure devices with different coupling coefficient.

tuning layer. As shown in Fig. 5, the refractive-index change wasn't saturated. Thus, if the active layer current could compensate for the optical loss in the tuning layer, tuning-width over 8 nm could be obtained. Multiple-quantum well(MQW) active layers are promising. On the other hand, MQW waveguide[6] as the material of large refractive index change by current injection with small increase of optical loss to tuning layer is another possible way.

Discussion

The suppression ratio of the measured filter, 11 dB, was rather low compared with that expected. Using a mode-coupled equation we made calculations and did preliminary experiments with the suppression ratio. In Fig.8, the curve shows the calculated suppression ratio versus the coupling coefficient of the corrugations. Solid circles are experiment data with conventional λ/4-shifted DFB laser structures. The suppression ratio is expected to exceed 20 dB.

The coupling coefficient of the measured tunable filter was 70-80 cm^{-1}. With these coupling coefficient, the suppression ratio more than 20 dB is expected from the calculation. Further investigation of the discrepancy of the measured filter will improve the suppression.

Conclusion

We have developed a λ/4-shifted DFB active filter with an independent current-injected tuning waveguide. We showed this structure to be suited to tunable filters with a wide wavelength tunability of 4.2 nm, no change in the gain spectrum shape, and a large anticipated suppression ratio.

Acknowledgments

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1-Gb/s Wavelength Filtering with Distributed Bragg Reflector Laser Filters in Two-Channel System Experiments

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Abstract

Wavelength switching, two-channel experiments with Distributed Bragg Reflector (DBR) laser filters are reported, with bit error rate = 10^{-9} with -25 dBm input power at 1 Gb/s.

1. Introduction

To fully exploit the advantages of optics for switching applications, the wavelength dimension should be utilised. An optimum photonic switching architecture probably combines optical space and wavelength switching with electronic time switching. Tunable emitters and tunable optical filters are key devices for developing such systems. A category of devices that are particularly interesting is the one comprising tunable laser diodes, that can be operated *either* as emitters (when biased above the oscillation threshold) *or* as narrowband filters (biased below the threshold). Filtering has previously been demonstrated in tunable two-section Fabry-Perot lasers [1], in tunable multi-section DFB lasers [2], [3], [4] and in tunable two-section [5] and three-section [6] DBR lasers.

Attractive features of such devices are 1) the simultaneous filtering and amplification function, 2) the narrow filter bandwidth making them ideal for High Density Wavelength Division Multiplexing (HDWDM), 3) the possibility to electrically detect the bit-stream in the selected wavelength channel by measuring the change in quasi-Fermi levels over the active section, 4) the option to use them as FSK to ASK demodulators in wide-deviation FSK systems, due to the intrinsic narrow bandwidth of several GHz, 5) fast electrical wavelength tuning. The multi-functional properties gives them an advantage over other types of filters, allowing a smaller total number of devices to be deployed. One should, however, also mention some problems: Temperature and current stabilisation is required, the active filters add noise to the signal, they are polarisation dependent and they show a nonlinear behaviour due to gain saturation when operated with too high input powers [7]. The latter causes severe problems at high bit rates.

Here we report on the successful operation of a three-section DBR laser as a reflection filter, in two-channel experiments with bitrates of 140 Mb/s, 600 Mb/s and 1 Gb/s. Our results represent, to the best of our knowledge, the first two-channel system experiments with DBR laser filters (previous multi-channel system experiments have used DFB lasers [3], [8]) and the first bit error rate measurements with active DBR filters at gigabit/second bitrate. One of the main reasons to use DBR lasers rather than DFB lasers is that a larger total tuning range can be achieved [9], and hence more channels utilised.

2. Experimental setup and filter characteristics

The experimental setup is schematically shown in Fig. 1. The DBR filter was a three-section, butt-joined device [10], with a 520 μm long Bragg section, a 100 μm phase section and a 190 μm long active section. The bandgap wavelength of the passive sections is 1.30 μm and that of the active section 1.55 μm. The total tuning range was 5 nm, and the single-current (i.e. with the phase and Bragg section electrically connected) continuous tuning range 1.7 nm. The lasing wavelength was 1.53 μm. Two other, similar DBR lasers were used as emitters. One was externally intensity modulated at the frequency f_1, the other was directly intensity modulated at the frequency f_2. Light was coupled into the active section of the filter with a tapered fibre lens. The coupling efficiency was estimated to be - 8 dB. Polarisation maintaining fibres were used throughout, and care was taken to align the polarisation of the different devices.

First the DBR filter was characterised with respect to its bandwidth as a function of injected current into the active section. This was done by using one of the DBR-emitters as frequency tunable light source, careful calibration of frequency change versus tuning current, a

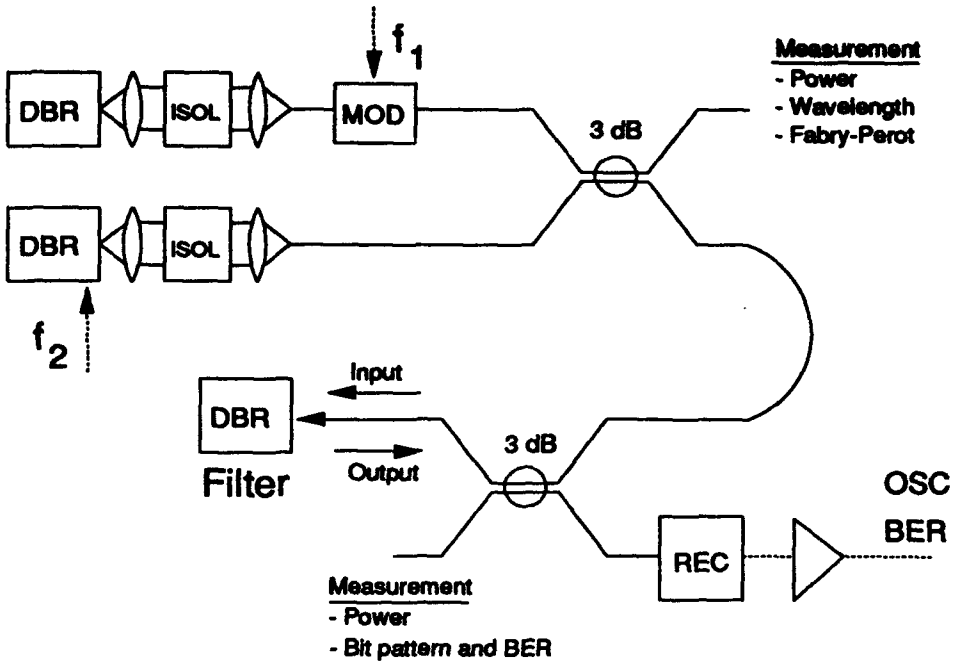


Figure 1. Experimental setup. ISOL = optical isolator, MOD = lithium niobate Mach-Zender amplitude modulator, REC = hybrid PIN/FET module. Lasers were temperature stabilised to within +/- 0.03 K, and current stabilised to within +/- 0.05 mA.

chopper inserted in the beam path and by using the filter in its electrical detection mode ([4], [5]) and lock-in detection technique. The result is shown in Fig. 2. At high biases and large input powers, the typical non-linear behaviour, due to gain-saturation, is seen.

3. Low-speed system experiments (140 Mb/s)

Initial experiments were done at 140 Mb/s. The directly modulated DBR laser (f_2 = 140 Mb/s) was used as signal source, and the filter was electrically tuned to the signal. Using an optimised 140 Mb/s receiver, the minimum input optical power to the DBR filter (by input power we understand the mean power level in the tapered fibre immediately before the DBR filter) to achieve a bit error rate (BER) of 10^{-9} in the receiver after filtering, was -27 dBm at $I/I_{th} \approx 0.97 - 0.98$.

This was poorer than expected, but can be understood by considering the chirping behaviour of the source DBR-laser under direct modulation. The dynamic line-width was measured with a scanning Fabry-Perot, and found to be 2 - 20 GHz, critically depending on exact biasing and current modulation depth. This large chirping, caused by current leakage from the active to tuning sections, occurs in spite of a large dark, zero-bias resistance between the sections of about 80 kΩ. It causes a spread out of the power into a frequency span much larger than the filter bandwidth, thus limiting the filter response, and is a highly unwanted effect.

4. High-speed system experiments (600 Mb/s and 1 Gb/s)

For high-speed experiments an externally modulated DBR laser was used as source. To simulate the behaviour of a multi-channel system, the second laser was direct-modulated at 100 Mb/s (a frequency chosen to reduce the chirp, also the bias conditions of this laser was chosen to minimize the chirp so that the bandwidth of the perturbing channel was about 5 GHz), operated at high power (-20 dBm in the tapered fibre) and used as a frequency-tunable perturbation channel. A 2.4 Gb/s optimised receiver was used.

The filtering properties were studied as function of signal input power and separation between the signal and the perturbation channel. Received bit-patterns after the filter were studied on an oscilloscope, and BER were measured. The exact modulation frequencies were chosen so that they were not multiples of each other. Also the bit sequence lengths were different.

Fig. 3 shows the BER characteristics for a 600 Mb/s signal, with and without perturbation. We see less than 2 dB penalty due to cross-talk from the perturbing channel, at frequency separations larger than 12 - 15 GHz. For smaller separation the BER degraded rapidly. For instance, at 10 GHz separation the cross-talk penalty was 9 dB. The behaviour was similar at a signal bit frequency of 1 Gb/s. Fig. 4 shows the BER characteristics (at a bias of the filter I/I_{th} = 0.97) for the two cases with only the signal and the signal plus the perturbation (-20 dBm

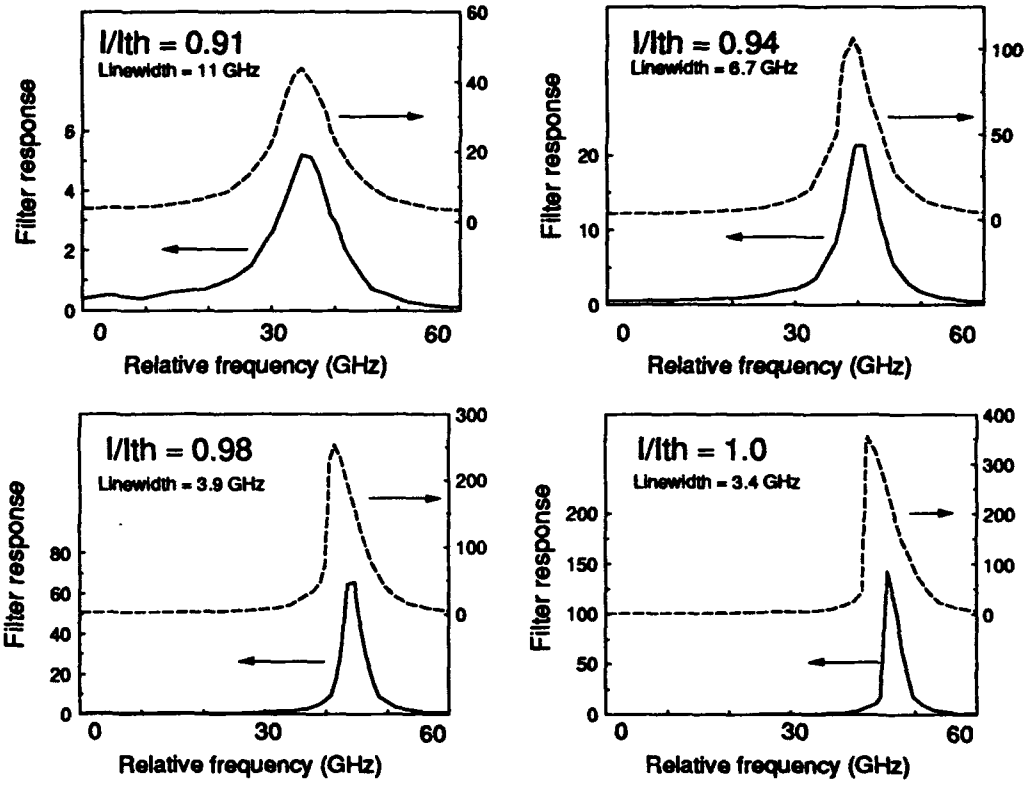


Figure 2. Filter bandwidth measured with -20 dBm (dashed) and -30 dBm (solid) input power, measured in fibre before coupling. Linewidths correspond to the low-power case.

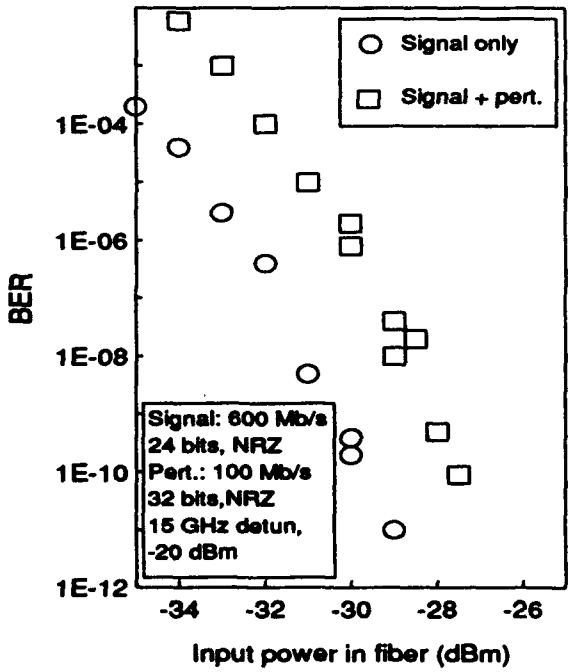


Figure 3. BER in 600 Mb/s experiment.

perturbation power). Once again, only small penalty is seen for channel separation larger than 15 GHz, and the BER degrades rapidly at channel separation smaller than 10 GHz.

The insertion of the filter degraded the detector sensitivity, defined as the received total (signal + amplified spontaneous emission, ASE) mean power level required to achieve BER = 10^{-9} at 1 Gb/s, by approximately 3 dB. However, subtracting the ASE part from the total power reaching the receiver, the *signal* sensitivity was equal to that of the sender/receiver system alone, without any active filter. We could thus not observe any degradation due to beat-noise or signal distortion introduced by the filter, in this experiment, within an experimental accuracy of +/- 1 dB.

Fig. 5 shows the received signal when the DBR filter was tuned to the 1 Gb/s signal source, in the presence of the perturbing channel at a 15 GHz distance from the signal. Changing the tuning current of the filter (and slightly modifying the active current to maintain the same I/I_{th}) the perturbing channel could be filtered and detected instead, Fig. 6.

5. Conclusion

Successful operation of DBR active filters at 1 Gb/s is reported. The experimental conditions used, with a strong perturbation channel which simulates cross-talk from several neighbouring channels in a multi-channel experiment, indicate that it should be possible to operate the device with at least 5 - 10 wavelength channels, each

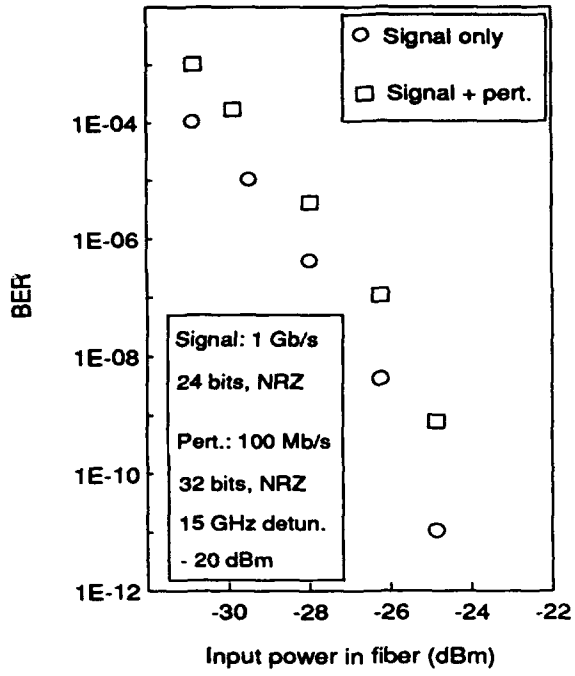


Figure 4. BER in 1 Gb/s experiment.



Figure 5. Received bit pattern when the filter was tuned to the 1 Gb/s signal.

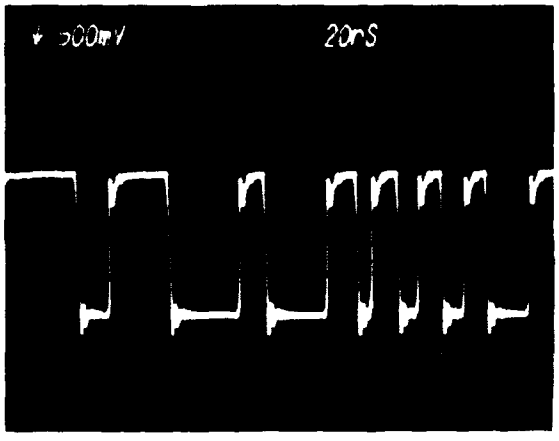


Figure 6. Filter tuned to the 100 Mb/s perturbing channel.

at 1 Gb/s or more. We foresee that future devices, with 1) better cross-talk through reduced coupling coefficient in the Bragg grating section and with both mirrors being Bragg-reflectors (to reduce residual Fabry-Perot side-modes) and operation in transmission rather than in reflection, 2) larger tuning range through improved design, smaller material bandgap and inclusion of quantum wells in the passive sections, will be able to sustain a larger number of channels.

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Frequency Conversion by Four-Wave Mixing in Semiconductor Laser Amplifiers: How to Relax the Filter Problem?

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In Ref.1 an all optical frequency conversion method was reported, which is based on nearly degenerate four-wave mixing (NDFWM) and homogeneous gain saturation in semiconductor laser amplifiers (SLA). This method promises a frequency conversion range up to about 10 THz (depending on the gain bandwidth of the SLA), a conversion efficiency η of more than 0 dB, the frequency conversion of a given data signal simultaneously to several frequencies and finally data transparency. However, it restricts the bit rate to $\leq$ 1 Gbit/s. In two experiments a successful operation of this method was demonstrated [2, 3]. A disadvantage of this frequency conversion method are the severe requirements on the resolution of the optical filter, which is necessary to select the converted data signal out of a multicomponent spectrum generated at the output of the SLA. In this paper we investigate how to relax the requirements on the selectivity of the optical filter.

The principal arrangement of the considered frequency conversion method is shown in Figs. 1, 2. Three optical waves, the signal wave (input power $P_{s,in}$, output power P_s, frequency f_s), the pump wave ($P_{p,in}, P_p, f_p$) and the converter wave ($P_{c,in}, P_c$, f_c), are coupled via optical fibers and fiber couplers into a SLA. The signal wave and the pump wave have a frequency spacing $\Delta f_s = |f_p - f_s|$ and cause carrier density modulation at the beat frequencies Δf_s and multiples of Δf_s. The refractive index change associated with this carrier density modulation generates new spectral components around the pump and signal wave. Fig. 2 shows schematically the most adjacent and in general strongest

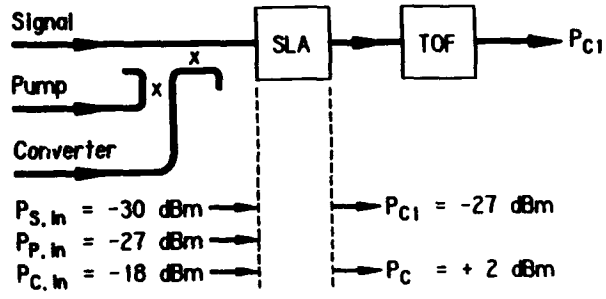


Fig. 1: Schematic representation of the frequency converter. The converted data signal P_{c1} is selected by the tunable optical filter TOF. The indicated light powers correspond to an experiment.

components with the optical powers P_1, P_2, P_3 and P_4. As the carrier density modulation affects the entire gain spectrum of the SLA, frequency conversion to any frequency f (wavelength λ) within the entire gain spectrum is achieved by means of the injected converter wave. The frequency spacing between the converter wave and the pump or signal wave, respectively, ($|f_c - f_p| \geq 10$ GHz) is in general sufficiently large to avoid NDFWM between the converter wave and the two other injected waves. The output spectral components P_{c1} and P_{c2} in Fig. 2 represent frequency converted (wavelength shifted) replica of the input signal. The frequency components P_{c3} and P_{c4} have a more complicated structure [4]. With a tunable optical filter (Figs. 1, 2) the converted signal P_{c1} is selected out of the total output spectrum.

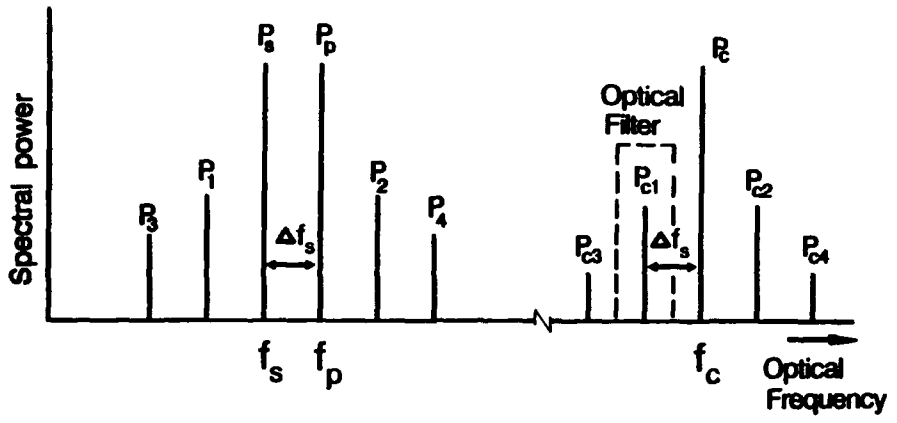
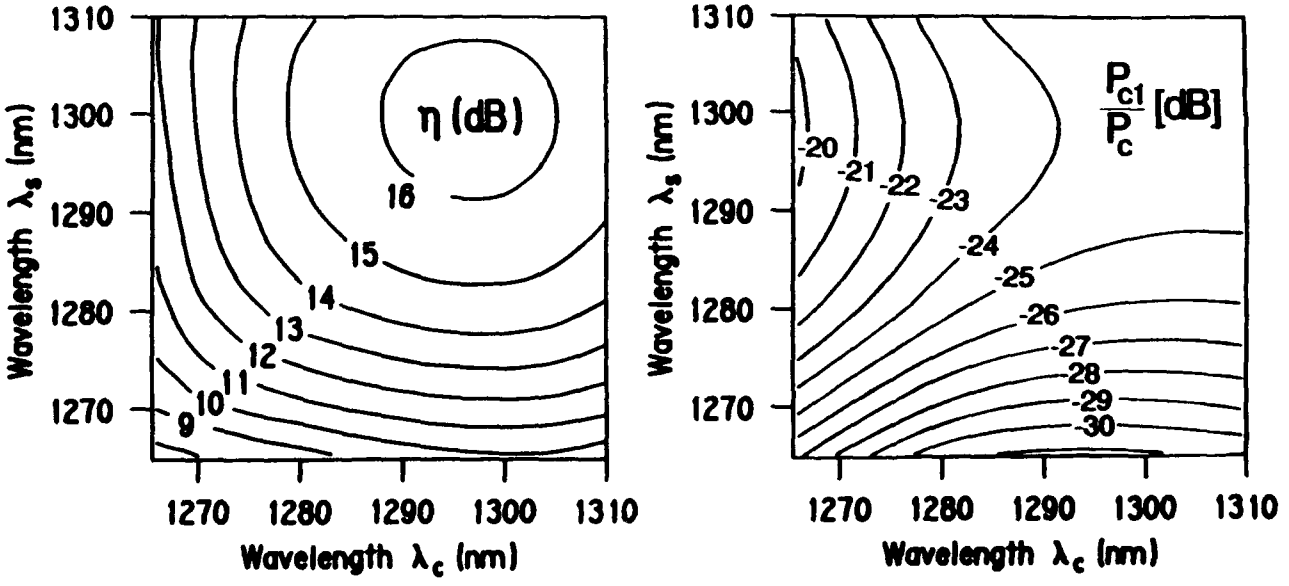


Fig. 2: Schematic spectrum at the amplifier output. Δf_s is the frequency spacing between the signal and pump wave.

The requirements on the filter selectivity are tremendous. The frequency spacing Δf_s between the converted signal wave P_{c1} (the center frequency of P_{c1}) and the two adjacent frequency components P_c and P_{c3} is restricted by the efficiency of ND-FWM to $\Delta f_s \leq 1$ GHz [5]. As realistic optical filters exhibit a limited selectivity only it is necessary to increase the ratios P_{c1}/P_c and P_{c1}/P_{c3}. Operating the frequency converter with maximum conversion efficiency $\eta = P_{c1}/P_{s,in}$, the converted signal power P_{c1} is in general 20 or 30 dB smaller than the output power P_c of the converter wave. Figs. 3 and 4 depict an example of calculations with the operation condition described in the figure caption. The realization of a useful frequency converter implies therefore to optimize the ratios $\eta = P_{c1}/P_{s,in}$, P_{c1}/P_c and P_{c1}/P_{c3} simultaneously.



Figs. 3, 4: Contour lines of constant values $\eta = P_{c1}/P_{s,in}$ and P_{c1}/P_c in the λ_c, λ_s-plane, where λ_c, λ_s are the wavelengths of the converter and signal wave, respectively. The calculations are performed for the set of input powers: $P_{s,in}$ = -30 dBm, $P_{p,in} = P_{c,in}$ = -6 dBm.

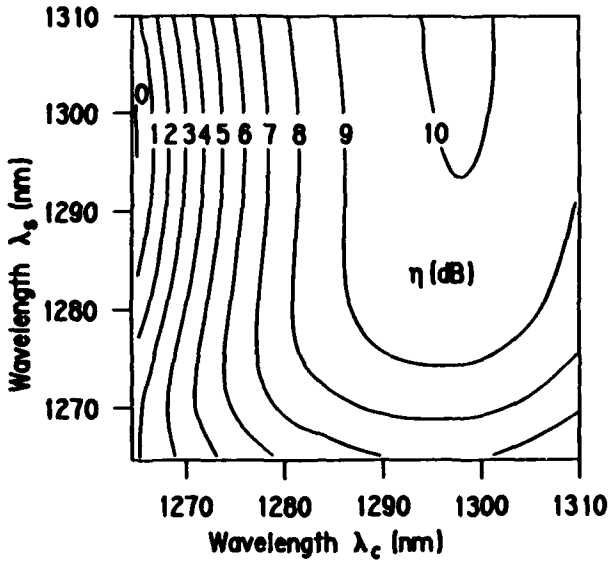


Fig. 5: Calculated contour lines for the conversion efficiency η in the λ_c, λ_s-plane for the injected powers $P_{s,in} = P_{p,in}$ = -6 dBm and $P_{c,in}$ = -8 dBm

The refractive index change associated with the carrier density modulation in the SLA is larger in its real part than in its imaginary part. Consequently the generation of P_{c1} is primarily an effect of angle modulation of the converter wave at the beat frequency Δf_s. The ratios P_{c1}/P_c and P_{c1}/P_{c3} can be modified by the modulation index. A larger modulation index is obtained by an increase of the input powers until P_s and P_p reach the saturation output power [4, 6].

As Figs. 5, 6 and 7 show, calculations revealed that the optical input powers $P_{s,in}$, $P_{p,in}$ and $P_{c,in}$ can be chosen appropriately, that firstly the conversion efficiency η is larger than 0 dB and secondly the frequency components adjacent to the frequency converted data signal P_{c1} are smaller or at least comparable with P_{c1} over a sufficiently large range of λ_s, λ_c-values.

This relaxes the requirements on the selectivity of the optical filter. However, it is not a satisfying solution for the filter problem. Such a solution seems only be possible by an appropriate increase of the frequency spacing Δf_s, which is restricted by the carrier lifetime in the SLA.

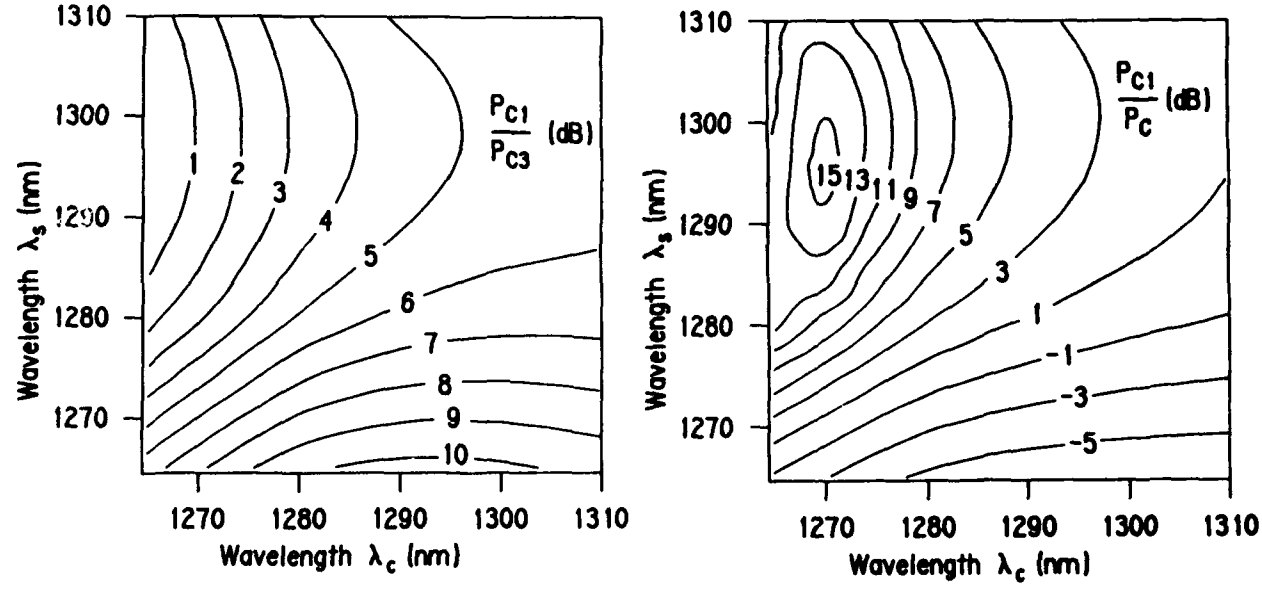


Fig. 6, 7: Calculated contour lines for the power ratios P_{c1}/P_c and P_{c1}/P_{c3} in the λ_c, λ_s-plane. The injected light powers are the same as in Fig. 5.

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Multi-Divisional Switching

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Photonic Time-Multiplexed Permutation Switching Using the Dilated Slipped Banyan Network

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Abstract

A modification of the classical banyan switching network architecture is called the dilated slipped banyan. This architecture is recursive and switching networks of any size perform permutation switching under a simple switching rule. They also exhibit column-control and dilation, properties that are particularly relevant to guided-wave and free-space photonic technologies. A photonic switching network, with this dilated slipped banyan architecture, is proposed as the hub of an all-optical active-star local-area network.

Introduction

A new switching network architecture, called the *Dilated Slipped Banyan Network (DSB)*, is proposed for the hub of a *photonic* active-star Local Area Network (LAN). A lithium niobate implementation of a classical 4-by-4 banyan architecture was proposed[1] for bit-interleaved time-multiplexing. The DSB has properties, described herein, that make it more general in size and more amenable to lithium niobate implementation than the classical banyan. Furthermore, since the active-star LAN application could use a word-interleaved data format instead of a bit-interleaved format, the hub switch need not be bit-synchronous with the data.

Recursive Construction

A DSB(N) has N inputs, N outputs, and *order g*, where $N = 2^g$. A DSB(1) is built from a single 2-by-2 switch. Its only input connects to this switch's upper left port and its only output to the upper right port. The switch's lower ports on each edge are not used. A DSB(N) is constructed recursively from a DSB(N/2). A DSB(N) consists of three interconnected subnetworks: a distribution stage at the left and DSB(N/2) subnetworks at the upper right and lower right. The N/2 outputs of each DSB(N/2) subnetwork are identically the N outputs of the overall DSB(N). The distribution stage has one column with N switches, and the N inputs to the overall DSB(N) connect to the upper left port of each switch in this distribution stage. The lower left ports on each switch in this distribution stage are not connected to inputs but are used in the recursion.

For $n = 0$ *to* $N/2-1$, the n-th and (N/2 + n)-th switches in the distribution stage connect to the n-th switch in the leftmost column of the upper right and lower right DSB(N/2) subnetworks. Upper ports on these switches connect *straight across* and lower ports connect in *criss-cross*. This *slipped* inter-stage connection pattern has more *cross-overs* than the classical banyan. Figure 1 illustrates the recursion and *slipped* inter-stage connection in a DSB(8).

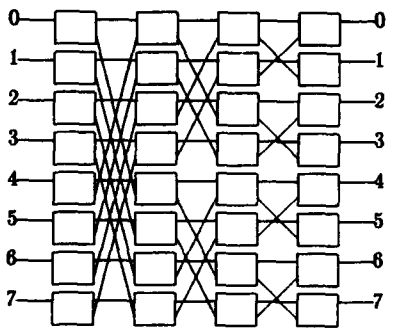


Figure 1. 8-by-8 Dilated Slipped Banyan Network

Construction from elementary 2-by-2 switches suggests lithium niobate technology. A high degree of integration is expected, but a design has not yet been attempted. The DSB(N) is seen to be N switches *high* and $g + 1$ columns *deep*. Since inputs and outputs connect to both ports on the edges of the classical banyan network, the classical banyan is $N/2$ switches *high* and g columns *deep*. The benefits of the DSB are felt to be worth these modest penalties.

Column-Control and Dilation

Consider the configurations of any rectangular network in which all the switches in the same column are always in the same state. The parallel electronic signal that controls the network is simplified from one *signal per switch* to one *signal per column*. This *column-control*[2] restricts a DSB to only $2^{g+1} = 2N$ different specific configurations. Not only are these shown to be sufficient, only half of them will be used.

A network configuration is *dilated*[3] if no internal switch is used simultaneously by more than one path through the network in any legal configuration. Every path through a dilated configuration is immune to *first-order* crosstalk at the switches. Every configuration of a column-controlled DSB is *dilated*.

Column-control and dilation are significant to lithium niobate technology. Besides reducing the complexity of the binary control-word and the number of drivers needed to operate the DSB, column-control reduces the interface pins on the chip and simplifies the internal connection to the switches' electrodes. However, the ability to adjust individual control voltages for each switch in a column is lost. The resulting penalty is higher crosstalk per switch than with individual switch-control. While dilation is important to lithium niobate because the switches exhibit high cross-talk, dilation is even more important in a DSB, because crosstalk is exacerbated by column-control and by the extra column of switches.

Consider paths to follow one of two *rails* through a DSB, depending on whether a path exits a switch from its upper or lower output. In a DSB, a path *changes rails* only in a switch in the *crossed* state. Since network inputs and outputs are connected to upper ports on both edges of the network, all paths must begin and end on upper *rails*. Thus, paths may only change *rails* an even number of times. If a binary ONE in the control word places all the switches in a column into the *crossed* state, then every control word for a column-controlled DSB must exhibit *even ones parity*. Of the $2N$ possible control words for a column-controlled DSB(N), only those N with even parity are useful.

Configurations and Control

Each of these N useful configurations of a column-controlled DSB(N) provides paths for N simultaneous one-to-one input-output connections. The resulting N^2 paths cover the N^2 combinations of N inputs to N outputs. Thus, any given input and output are connected together in exactly one of these N configurations. While most circuit-switched applications allow blocking for concentration between network terminals and network resources, internal network architectures are usually either non-blocking[4] [5] or have a load-dependent, low probability of blocking. While *permutation networks* are typically inadequate for such general applications, a special circuit-switched application is presented where only this *full accessibility* is required.

Each row in Figure 2 corresponds to one of the eight configurations of a DSB(8). The first column is the number T of a configuration and the next-to-last column is the control code that places the DSB(8) into its T-*th* configuration. If the entry in row T and column I of the table is J, then some path in configuration T connects input I to output J. For example, input 4 connects to output 5 in configuration 1. Control code 0011 effects this connection (and seven others with it) on Figure 1 by placing the eight switches in each of the first two columns into the *bar* state and the eight switches in each of the last two columns

config. T	input 0	1	2	3	4	5	6	7	control code	perm-utation
0	0	1	2	3	4	5	6	7	0000	(0)(1)(2)(3)(4)(5)(6)(7)
1	1	0	3	2	5	4	7	6	0011	(01)(23)(45)(67)
2	2	3	0	1	6	7	4	5	0110	(02)(13)(46)(57)
3	3	2	1	0	7	6	5	4	0101	(03)(12)(47)(56)
4	4	5	6	7	0	1	2	3	1100	(04)(15)(26)(37)
5	5	4	7	6	1	0	3	2	1111	(05)(14)(27)(36)
6	6	7	4	5	2	3	0	1	1010	(06)(17)(24)(35)
7	7	6	5	4	3	2	1	0	1001	(07)(16)(25)(34)

Figure 2. Configuration Schedule and Control for N=8

into the *crossed* state. In configuration 0, every input is connected to the output with same number, by placing all switches into the *bar* state.

The control-code that places a DSB(N) into configuration T is the g-bit Gray Code for integer T, concatenated with an even-parity bit at the low-order end. The numbering rule for configurations is such that $B(J) = B(T)$ *ezor* $B(I)$. Here $B(K)$ is the binary code for integer K and *ezor* is the bit-wise *exclusive-or* function. This numbering rule identifies the output J to which input I is connected in configuration T. Rewriting the numbering rule as $B(T) = B(I)$ *ezor* $B(J)$, identifies the configuration T in which input I is connected to output J.

Rewriting the numbering rule as $B(T) = B(J)$ *ezor* $B(I)$, if input I is connected to output J in configuration T, then input J is simultaneously connected to output I. Each configuration of a column-controlled DSB corresponds to a permutation of its port numbers. These N permutations are the identity permutation, $T=0$, and $N-1$ pair-wise permutations. The permutations corresponding to each configuration are tabulated in the notation of *permutation cycles* in the rightmost column of Figure 2.

Let a DSB(N) reconfigure in time-multiplexed fashion by sequencing through its N configurations, in numerical order, in N consecutive time-slots. Let it repeat this sequence of configurations, cyclicly, every *frame*. Since consecutive Gray Code-words are *binary adjacent*, only one bit changes from one time-slot to the next. Since the parity-bit must also change, two bits in the control word change state from one time-slot to the next. The right column of a DSB changes state in every time-slot, the next column in every other time-slot, etc.[6]

Time-Multiplexed Active Star LAN

In a *star* architecture, a LAN's terminals are placed at the ends of the *arms* and the *hub* contains some common resource, like a *passive* bus or coupler or an *active* switching network. In a *half-duplex star* LAN, the I-th terminal has an *up-link* that connects its transmitter to the hub's I-th input and a *down-link* that connects the hub's I-th output to its receiver. In an *active star* LAN that serves N terminals, the hub contains an N-by-N switching network that simultaneously connects the up-links to the down-links in different configurations.

Let a time-multiplexed DSB(N) be used at this hub and let all the terminals be synchronized to its *time-slot clock*, not necessarily to a common *bit block*. If terminal I must transmit to terminal J, I holds this data until time-slot T, where $B(T) = B(I)$ *ezor* $B(J)$, and then transmits on its up-link. Only J will receive it. If I simultaneously receives on its down-link, it knows the data came from J. There is no contention in the LAN.

Consider a LAN with 16 terminals. Let the link data rate be 1.7 *Gbps* and let each time-slot contain 1024 bits of data and an 80 *ns* guard band that is free of data. Then, the duration of a time-slot is $1024 / 1.7 + 80 = 682$ *nsec*. If the identity configuration is skipped in the time-multiplexed schedule of configurations, the duration of a frame is $.682 \times 15 = 10.2$ μ*sec*. The frame rate is the inverse, 98 *K frame/sec*. Since each terminal may transmit 1024 *bits* to every other terminal once per frame, the effective data rate between *every pair* of terminals is $1.024 \times 98 = 100$ *Mbps*. This LAN is functionally equivalent to a *fully-connected network*, that would have 240 links, each at 100 *Mbps*. The gross

LAN throughput is 24 *Gbps*, with no loss of efficiency from multi-hopping, as in a ring architecture.

Conclusion

The *Dilated Slipped Banyan Network* has been described and its demonstrated properties are seen to match well with an implementation in lithium niobate and an application as the time-multiplexed hub of an active-star LAN. It is proposed that the LAN's transmitters, receivers, up-links, and down-links be implemented in single-mode photonics technology and that the central switch be specifically implemented in lithium niobate. The bit-rate could be high, limited only by the transmitters and receivers, and easily changed as the technology advances, when and if the need arises.

Acknowledgments

Some of this work was performed at AT&T Bell Labs in Murray Hill, NJ.

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Broadband Computer Network Based on Optical Subcarrier Multiplexing

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Abstract

A low-cost multichannel optical network testbed is described based on optical subcarrier multiplexing with low-coherence self-pulsating laser diodes and multimode fiber links. The testbed uses commercially available 790nm self-pulsating laser diodes (SP-LDs), multimode fiber, and GaAs OEIC single-chip receivers. The choice of these components virtually eliminates the laser beat-noise and modal noise and thereby makes the implementation practical. Potential applications of the network include workstation clusters, multiprocessor interconnection, and switch emulation.

1. Introduction

An optical passive-star network consists of a number of stations interconnected in a star topology by means of a central passive optical coupler. These networks offer a reliable and inexpensive means for implementation of local-area and room-area networks, multiprocessor interconnection networks, I/O buses, and workstation clusters. Optical subcarrier multiplexing (SCM) provides a means to divide the aggregate bandwidth of the optical medium in an optical passive-star network into multiple protocol-independent channels, each offering a fraction of the aggregate bandwidth. A network testbed to evaluate the SCM technology and its likely applications to computer-system interconnection are the subject of this paper.

The basic concepts of optical subcarrier multiplexing are described in [1]. On the transmitter side, the data in each channel modulates a subcarrier signal in the electronic domain. A variety of modulation techniques such as PSK, FSK, or ASK can be employed here. The modulated subcarrier in turn modulates a laser transmitter by intensity-modulation. The star coupler superimposes the individual subcarrier signals and broadcasts them to the receivers. The detector in each station receives all the subcarrier channels. One of the channels can be separated from this composite signal by mixing with a local oscillator which is tuned to the frequency of the subcarrier used to modulate the original signal. The demodulated signal is then amplified and detected to yield the original data.

SCM has several merits as compared to other optical multiple-access methods. There is no need to control the transmitting wavelengths of the lasers as in wavelength-division multiplexing (WDM). Tuning is performed in the electronic domain which is faster and less expensive as compared to optical tuning required in a WDM network. There is no central network clock operating at the aggregate speed and the channels are asynchronous and independent; this results in high availability and reliability.

Although the application of subcarrier multiplexing to multiple-access networks (N to N) has been suggested by Darcie [1], subsequent studies have been restricted to its use for broadcast CATV distribution (1 to N) [2]. The latter systems use longwave (1300nm or 1550nm) optoelectronics and single-mode fiber technology. The high cost of the optoelectronic components (typically Indium-Phosphide devices) associated with such an implementation relative to a shortwave (Gallium-Arsenide devices) implementation makes it unattractive for computer interconnection and networking applications. Even the

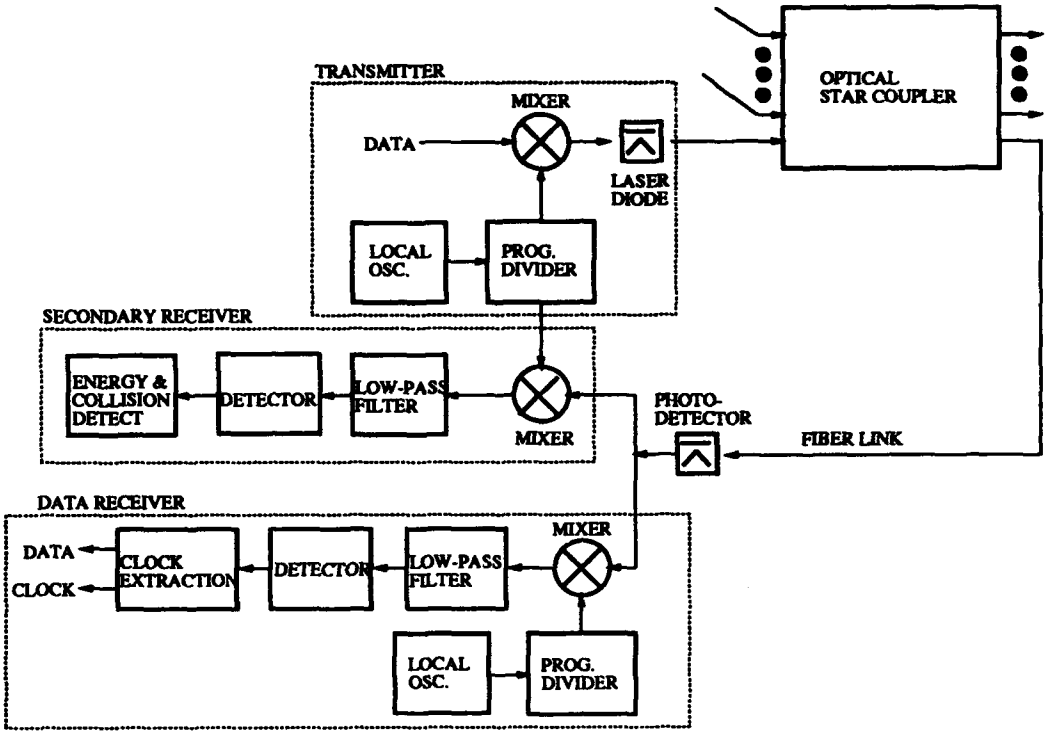


Figure 1: Functional block diagram of the SCM testbed.

feasibility of such an implementation in a multiple-access (N to N) application is in doubt because of the problems of laser beat-noise [3] and modal noise.

In this paper, we describe the construction and operation of a broadband network testbed based on SCM. The testbed uses commercially available 790nm self-pulsating laser diodes (SP-LDs), multimode fiber, and GaAs OEIC single-chip receivers. In addition to the low cost of these components, this choice virtually eliminates the laser beat-noise and modal noise and thereby makes the implementation practical.

The motivation for designing this testbed is two-fold. The first is to study the feasibility of the technology in a multiple-access environment. The second is to investigate possible applications of such a high-speed multichannel network in computer-system interconnection and networking. The technology characteristics of the testbed are described in [4]. This article will concentrate on the system-design and applications of the testbed.

2. System Description

The SCM network testbed consists of five stations connected to a central optical passive star-coupler by means of duplex fiber-links. The aggregate bandwidth of the network is divided into a number of channels of equal bandwidth. The number of channels was chosen to be equal to the number of stations, so that each station may be assigned a distinct receiving channel. This choice was made only for simplicity and convenience; in practice, a number of stations can be made to share each receiving channel. The maximum number of stations on a single coupler is limited by the power-budget and noise constraints. With the technologies used, we estimate the limit to be in the range of 16 to 32 stations with 100-meter links. Larger networks can be constructed by the use of bridges.

2.1. Network Interface

Figure 1 illustrates the functional blocks associated with the physical interface of each station. Each station has a data receiver that is set to receive a distinct channel. The station receives all its data on this channel. The station is provided with a transmitter that can be tuned quickly to any of the five channels. The transmitting channel is selected based on the destination of each packet. A secondary receiver is provided to monitor the transmitting channel. This enables the station to check if the channel selected for transmission is busy prior to transmission of data, as well as to detect collisions after the transmission starts.

Each station has one laser diode and one photodetector. On the transmitter side, a local oscillator generates the subcarrier used to modulate the

data to be transmitted. The frequency of the subcarrier determines the channel in which the data is transmitted. The local oscillator output is passed through a programmable divider before modulating the data signal; the programmable divider allows the frequency of the modulating carrier to be varied, thereby accomplishing channel-selection.

A photodetector receives the composite optical signal and converts it to a broadband electrical signal. This signal is then fed to the data- and secondary-receiver subsystems. Each of these receivers then extract one of the channels independently by combining the composite signal with a locally generated signal at the carrier frequency of the desired channel. Because the secondary receiver is used to monitor the transmitting channel, its local-oscillator frequency is the same as that of the signal used to modulate the transmitter. Therefore, a separate local-oscillator is not required. When the transmitting channel is changed by means of the programmable divider, the secondary receiver simply follows the transmitter. The output of the mixer is passed through a low-pass filter to isolate the selected channel from other signals. Data from the channel is then extracted by a detector. The detector output is used to check for the presence of energy due to other transmissions in the channel prior to transmission as well as for collisions during a transmission.

The data receiver consists of a mixer and low-pass filter to extract the desired channel as in the case of the secondary receiver. An independent local-oscillator is used in this case to select the received channel. A fixed oscillator is used in our testbed because of the static assignment of stations to receiving channels. Dynamic assignment can be allowed by passing the local-oscillator output through a programmable divider. The output of the mixer is passed through a low-pass filter and detector. The detector output constitutes the received-data from which the receiver-clock can be extracted.

2.2. Technology

Our implementation uses short-coherence self-pulsating lasers operating at 790nm wavelength. The unmodulated self-pulsation frequency of the laser is approximately 2.2 GHz. This limits the aggregate network-bandwidth available to approximately 1 GHz. The bit-rate of each of the five channels was therefore set at 200 Hz. The modulation scheme used is QPSK, allowing a raw transmission rate of 200 Mb/s for each channel. The optical output of each laser is coupled into a 50/125 μm multimode fiber link. A fused-fiber star coupler was used at the hub. The detectors used are integrated GaAs IMSM detector/preamplifier devices.

2.3. Medium-Access Protocol

The SCM testbed allows a number of different medium-access protocols to be investigated. Broadly, there are two ways in which the multiple channels could be used: (i) one of the channels may be used as a control channel through which accesses to the remaining channels are scheduled, or (ii) each of the channels may be used independently with its own medium-access protocol. We have chosen the latter because of its flexibility in configuring the channels. In our first experiments, we intend to operate each channel independently with the CSMA/CD protocol. In this case, if a station P wants to send a message to another station Q, P first tunes its transmitter to the receiving channel of node Q. This automatically tunes P's secondary receiver to the same channel. If a transmission is detected by the secondary receiver, P waits till the channel is idle. P transmits its packet when the channel is idle. A retry is performed in the event of a collision. Many variants of CSMA/CD have been developed to minimize the probability of collisions and these are applicable to our system.

For high-speed networks, the above protocol generally works better than a baseband CSMA/CD protocol on the network with a single channel operating at the aggregate bandwidth. This is because, in CSMA/CD, the effective channel capacity decreases when the ratio of the propagation-time in the link to the packet-transmission time is increased [5]. Our method divides the high-bandwidth channel into many lower-bandwidth channels thereby improving the total capacity.

The efficiency of the protocol depends to a large extent on how fast the transmitters and receivers can be tuned to a channel. Because the transmitter and receiver sections in the testbed work on the same principle, the tuning delays are of the same order. In our system, the selection can be accomplished in approximately 100 subcarrier cycles (500 ns for a 200 Mb/s channel).

3. Applications

We intend to use the SCM testbed to investigate a number of computer-system applications. These applications are characterized by short distances (typically 100 meters or less, at most 1 kilometer), and the need for high bandwidth and low latency. The first application we intend to study is a peer-to-peer network cluster of high-performance workstations. A typical cluster in this case consists of a small number

(say 16) of workstations cooperating on a distributed application. The multichannel CSMA/CD protocol suits this application because of its inherent parallelism.

A second application for the technology is in interconnecting a number of workstations to a central file-server in the client-server model of computing. The traffic in this case is highly skewed, with most communication directed to or from the file-server. The following assignment of channels provides maximum parallelism in this case. Each channel is designated as the communicating channel for a subset of the client workstations and the stations in this subset communicate with the server only on this channel. This allows multiple simultaneous communication sessions between the clients and the server. A slightly different design is needed in the network interface at the server. The detector output in this case fans out to multiple adapter boards, each of which acts as a separate server port.

A third application is that of a multiprocessor interconnection network. The SCM testbed in this case emulates a multiple-bus interconnection network. Low latency is critical to this application. The testbed has a setup delay of the order of 1 μs, which is much larger than that of an electrical bus. The SCM technology, however, offers the advantages of low cost and longer distances. A special case of this configuration is when the number of channels is equal to the number of stations, allowing each station to be assigned a distinct receiving channel. This effectively emulates a nonblocking circuit-switch without the cost of a central switch, and provides high reliability.

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Role for Reconfigurable Wavelength Multiplexed Networks and Links in Future Optical Networks

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Abstract

Network design, implementation and paths to exploiting optical fibre bandwidth are reviewed. Experimental network measurements on installed fibre are reported using fibre amplifiers and optical switches.

Introduction

Wavelength routing is a method of building a high capacity network infrastructure which exploits the inherently large transmission bandwidth of optical fibre [1]. The networks use cross-connected wavelength division multiplexing elements, such as grating based devices [2], to access the bandwidth and provide interconnections. Component loss may be compensated for by using optical amplifiers such as the erbium doped fibre amplifier [3].

In principle any logical transmission path may be set up over a given physical cable or fibre network; the path being defined by virtue of the wavelength and the chosen optical interconnect field. Indeed more complex reconfigurable networks are possible using optical switches in the interconnect field. The key driving force behind these networks is the increased capacity, at reduced cost, made possible by removing the need to install new cables and duct routes which contribute a significant proportion of the installation costs of new systems [4].

The paper will outline the basic principles of wavelength routing and discuss experimental network demonstrations in both the laboratory and field environment. If these networks are to be viable control, management and planning issues must be addressed and the paper outlines some of these issues. Finally, the extension of the principles to reconfigurable networks will be described and an early experimental demonstration discussed using a 4 x 4 lithium niobate digital optical switch array [5].

Wavelength Routing

Wavelength Routing Principles

Wavelength routing principles may be outlined with reference to a simple star network structure, figure 1. This is one of a class of "hard wired" wavelength routed networks which includes chain, ring and tree and branch networks [6].

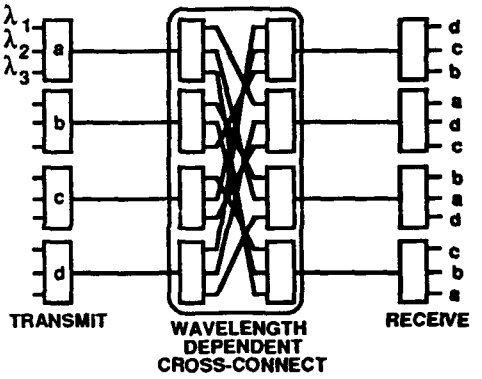


Figure 1. Wavelength Routed Star Network.

If we consider the transmit node a; the three wavelengths from this node are multiplexed and transmitted to the central wavelength dependent cross-connect where they are demultiplexed and re-multiplexed with channels from other input fibres. These are then transmitted to the receive nodes b, c, d with wavelength 1 going to node b, wavelength 2 to node c and wavelength 3 to node d. The same wavelengths are used by transmit node b where now wavelength 1 is transmitted to c, 2 to d and 3 to a. The wavelengths are reused in a similar fashion by the other nodes as shown.

The star network has the least number of lossy multiplexing elements in any one transmission path. It is also the most efficient in its utilisation of the wavelength domain and requires only N - 1 wavelengths to fully interconnect an N noded network compared with N(N - 1) wavelengths for a passive star network formed using couplers at the central cross-connect [7].

Application areas

The topology of the wavelength routed star network maps in well into existing BT telecommunication networks. Figure 2 shows the upper level of the optical fibre network which interconnects the 10 main sector switching centres

in London. The network comprises three star networks centred on each of the central switching centres. The outer switching centres are then linked using a ring network; a further ring network which interconnects the central switching centres is not shown.

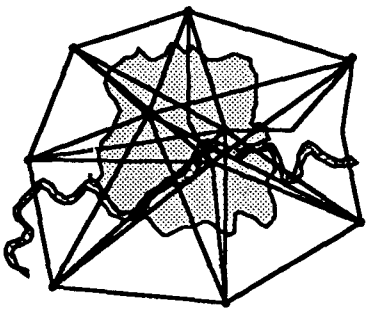


Figure 2. The London Optical Fibre Network.

This network of point to point optical fibre systems is constructed using 96 fibre cables and carries a mix of 140 Mbit/s and 565 Mbit/s optical systems. 1 + 1 network protection is used with, for example, alternative radial routes being provided by a second radial link and a single section of the ring.

Network demonstrations

Laboratory Demonstrations

Initial studies were carried out in the laboratory. A number of commercial six channel grating based wavelength division multiplexers were purchased in the 1.5μm operating window. These devices have a 12nm channel spacing in the range 1.5μm to 1.56μm and a typical channel bandwidth of 2.4nm. Early work included the demonstration of unamplified star networks with 50km range [8,9]. This range was extended to 90km using a single stage of semiconductor optical amplification located in the demultiplexed path at the central node. More recently a six wavelength branching network , based upon a star network, has been demonstrated with optical path protection and route diversity [10,11], figure 3.

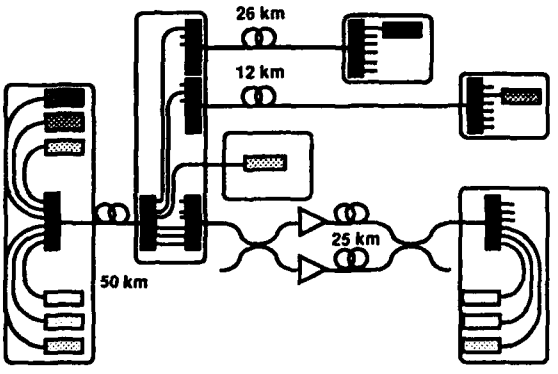


Figure 3. Six Wavelength Branching Network.

The lower wavelength channels were routed over short unamplified links; total link lengths up to 76km at 650 Mbit/s were demonstrated. The high wavelength channels, falling within the gain profile of the aluminium co-doped erbium fibre amplifier, were amplified and routed over 25km output links. The output signal from the central wavelength dependent cross-connect was split using a 3dB coupler into two fibre amplifiers feeding the separate transmission paths; these paths were recombined at the receiver using a second 3dB coupler. The optical path was selected by pumping the appropriate amplifier. In this way it was possible to provide both optical path protection and compensation for optical component loss. In practice, path failure would be sensed at the receiver and signalled to the second amplifier over a separate control network. This could be provided over the alternative route or by way of a completely separate management network. This network protection scheme does not, however, protect against terminal equipment failure.

Field demonstrations

In addition to laboratory demonstrations we have carried out a series of experiments on installed fibre cables in the London Network. A range of routes were made available and are shown in bold in figure 4.

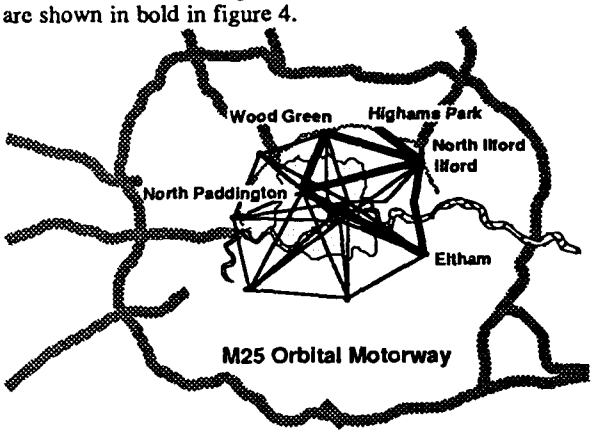


Figure 4. Field Demonstration Fibre Routes.

These routes were centred upon the Ilford sector switching centre and included shorter local fibres for unamplified demonstrations. The M25 London orbital motorway is shown to give some idea of the extent of the network.

In these first demonstrations fibres radiating from the Ilford exchange were used. These were loop back spliced at the remote exchanges to allow experimental star networks to be constructed with terminal equipment located in a single exchange location, figure 5. Terminal equipment was constructed using commercially available grating based wavelength division multiplexers, distributed feedback lasers and optical receivers. The receivers

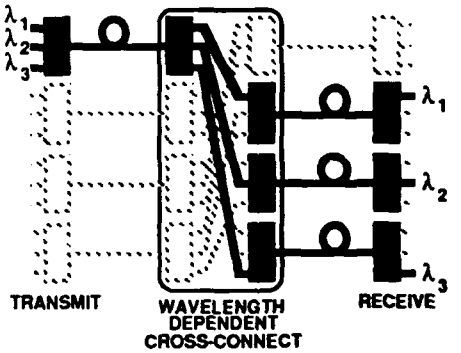


Figure 5. Experimental Demonstrator

incorporated full timing recovery at 622Mbit/s. Three DFB based transmitters were built operating at 1.536, 1.548 and 1.560μm. These were colocated at one node. Three separate receive nodes were constructed . Low back reflection connectors were used to interface to the transmission fibres.

Unamplified Demonstration. The first demonstration was of an unamplified network. The Ilford North route was used for the transmit node with the receive nodes using the two Highams Park fibre pairs and the Wood Green fibre pair. All routes operated with 1 in 10^9 error rates, or better, at 622Mbit/s. Transmission distances of ~22km were achieved with operating margins between 2 and 5 dB. Operation over the 42km Ilford North / Wood Green link was just possible with little margin. Results are summarised below :

Transmit Wavelength	*Receive Distance*	*Sensitivity*	*Margin*
Ilford North - Highams Park			
1.560 μm	21.9 km	-34.8 dBm	5 dB
Ilford North - Highams Park			
1.548 μm	21.9 km	-33.3 dBm	2 dB
Ilford North - Wood Green			
1.536 μm	41.9 km	-34.4 dBm	0 dB

The Ilford North - Wood Green system corresponds to a transmission distance equivalent to the diameter of the London network.

Amplified demonstration. These transmission distances were extended using optical amplifiers at the central node. Optical isolators were used on both the amplifier input and output to prevent lasing instabilities arising from reflections. Isolators are essential for optical amplifiers in operational networks. The North Paddington route was used for the transmit node; an erbium doped fibre amplifier boosted the signal power into the central node. Using a second stage of optical amplification, immediately after the central node, a transmission distance of 89km with 12dB operating margin was demonstrated for the 1.56μm channel over the second North Paddington fibre pair. Transmission distances of 63km and 83km were achieved with margins of 5dB and 1dB for the receivers using the Highams Park and Wood Green fibre pairs respectively. Both routes had only a single stage of optical amplification in the transmit side of the network. Results are summarised below :

Transmit Wavelength	*Receive Distance*	*Sensitivity*	*Margin*
North Paddington - North Paddington			
1.560 μm	88.8 km	-34.7 dBm	12 dB
North Paddington - Highams Park			
1.548 μm	63.2 km	-32.8 dBm	5 dB
North Paddington - Wood Green			
1.536 μm	83.2 km	-34.4 dBm	1 dB

The maximum demonstrated transmission distance of ~89km is approximately equivalent to twice the diameter of the London network.

Path Protection. Optical path protection and route diversity was demonstrated for the 1.56μm channel using a commercially available electromechanical optical switch [12]. The switch was located in the "North Paddington" receive path of the amplified demonstration discussed above. The alternative route was provided over a fibre pair loop back sliced at Eltham. The two possible routes had transmission distances of 89km and 86km respectively. The output of the central node was split using a 3dB coupler and transmitted over the two paths; the optical switch was located at the receive terminal. The primary route was the North Paddington fibre pair with the secondary route, via Eltham, being selected when the receive power fell below a preset level. The switch incorporated optical splitters and receivers to monitor optical power levels and processing electronics to activate the automatic switchover of the optical paths. Results are summarised below :

Receive route	*Distance*	*Sensitivity*	*Margin*
North Paddington	88.8 km	-34.7 dBm	6 dB
Eltham	85.6 km	-34.6 dBm	3 dB

Optical Network Control and Management.

The introduction of optical amplification and optical path protection increases the complexity of optical nodes within the optical network. As optical networks become more complex the need to control and monitor their status becomes important. If optical networking is to become a reality these issues must be addressed for both optical components and optical transmission technologies. Some aspects of the relationships between the electronic and optical control schemes will be addressed in the next paragraphs.

There is an increasing trend towards centralised network control and management. This is largely a software issue and will require large scale databases and other computer programs to gather network information, process this information and to maintain information on the network status. This immediately raises questions as to the amount of information involved and the speed of response to network changes, for example in the event of a path failure. Undoubtedly there will be the need for a certain degree of local control and processing with the control and management being organised in a layered fashion - each layer passing the minimum of information to the higher level. Optics may provide the ability to automatically switch routes using optical sensing and in time optical self healing networks may be possible allowing simplification of network managements and control software.

Network monitoring will be necessary to predict component failure, for example pump laser degradation in an optical amplifier, allowing programmed repair and maintenance. Additionally where an optical path has failed in a complex optical network (comprised of many sections of optical loss, network flexibility points and optical amplifiers) the ability to monitor the status of individual components and sections will be necessary. This will allow the fault to be localised enabling the working elements in the optical link to be returned to service.

The optical network will form an additional layer in existing plesiochronous and future, synchronous and asynchronous, transmission systems [13, 14]. The control of this optical layer will be provided over a separate network carried on either the same fibre paths or a physically separate network [15]. Network information may be concentrated and combined with control information from elec-

tronic levels and functions. This information may be carried to a central network manager using the SDH hierarchy [14] or another suitable transmission format.

It is likely that optical control functions, for example amplifier gain control, will be implemented using local microprocessors and element managers. This will give individual optical elements, or groups of optical elements, a degree of autonomy and will allow remote programming and interrogation of optical elements. This ability to download network control functions may be used to minimise unwanted information flow in the control network, improving the response time and reducing the complexity of the higher level control systems. The use of microprocessors to locally control optical elements will also enable the control network to be implemented as and when the centralised management software is developed.

Flexible Networks

Network control and management is just one issue in the move towards transparent optical networks. If these networks are to be truly reconfigurable it will be necessary to maintain signal levels within well defined limits.

Figure 6 shows a potential network building block. It comprises a multiplexing element, an amplifier with isolators on both the input and output, the transmission fibre, a second stage of amplification, a demultiplexer and finally an optical cross-point switch. If the element is to be cascadable the input optical power must equal the output optical power.

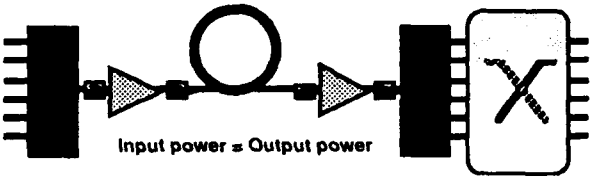


Figure 6. Basic Network Building Block.

Important parameters are the input signal power per channel, the signal to noise ratio and the maximum allowable multiplexed power in the transmission fibre determined by laser eye safety limits and working practices. Parameters of concern for the amplifier are the gain,crosstalk, saturated output power and noise figure. Optical loss of the wavelength division multiplexing components, the optical cross-point and their polarisation dependent losses are important as is the loss of the fibre. Finally if dual window working or optical path protection is required additional components, such as couplers and switches, will be necessary.

Obviously there will be a limit to the number of elements which may be cascaded. This may arise from one of a number of limiting effects. For example signal to noise degradation in the amplifier chain saturation effects due to the accumulation of spontaneous emission, bandwidth concatenation effects in the multiplexing elements or, for long haul systems, the onset of fibre nonlinearities.

What are the basic component requirements for these networks? In the immediate future wavelength independent optical switch arrays with low insertion loss and low polarisation dependence are required. In the longer term the flexibility of this class of networks could be increased by using reconfigurable tunable multiplexing elements, wavelength converters and tunable sources and receivers.

Reconfigurable Network Demonstration

As a first step in the demonstration of these reconfigurable network nodes we have extended our demonstrator to include a polarisation independent lithium niobate 4 x 4 digital optical switch array from Ericsson [5], figure 7. This has been located in the 1.56μm path and in this first demonstration has been configured to demonstrate the concept of capacity switching [13].

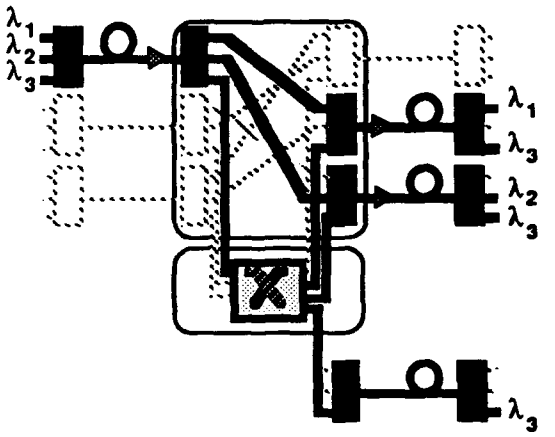


Figure 7. Reconfigurable Network Demonstration.

Initial measurements have been made in the London optical fibre network where we have demonstrated the switching of a 622Mbit/s optical channel from a long haul route with a total transmission distance of ~84km to a local node colocated with the central node. Further experimental measurements are in progress.

Conclusions

Using two stages of erbium doped optical fibre amplifiers we have demonstrated wavelength routed optical networks with ~89km range with 12dB margin. This would enable such networks to serve an area equivalent to the area enclosed by the M25 London orbital motorway with optical margins of ~6dB. This takes in major business and financial centres which generate ~40% of the traffic carried by the BT network.

Wavelength division multiplexing and wavelength routed optical networks will allow the transmission network to expand to meet the growing and changing demands of our customers. This expansion may be met using the existing fibre infrastructure at reduced costs. The optical transport layer enables routing and restoration to be carried out optically simplifying the electronic node and offering the prospect of increased reliability. Furthermore the networks are transparent and compatible with analogue transmission systems, plesiochronous systems and future synchronous and asynchronous networks. Indeed all these systems may be mixed on to a single transmission fibre.

In conclusion configurable transparent optical networks are the first step towards the exploitation of the monomode fibre transmission bandwidth.

Acknowledgments

The authors are grateful to Chris Joannides and Fred Blayney of BT Worldwide Networks for their assistance in making routes available in the London main optical fibre network; to Per Granestrand and Lars Thylen of the Fiber Optics Research Center, Ericsson Telecom A B, Stockholm for the use of the 4x4 lithium niobate switch; and, finally, to Paul Brown and Martin Greatbanks of BT Laboratories for their work in constructing the terminal equipment.

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92-17283

Combined Photonic Time-Division and Wavelength-Division Switching Network

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Abstract

Photonic switching systems can generally be divided into three categories: space-division(SD)[1][2], time-division(TD)[3], and wavelength-division(WD)[4]. However, for important goals, such as transmission and management of large amounts of video information, a combined system must be used for high degrees of multiplexity.

This paper proposes a combined photonic TD and WD switching network for a photonic switching system. This paper compares the number of optical devices required for this proposed structure with conventional structures. And, finally, This paper shows how the proposed structure can further reduce the total number of optical devices required.

Introduction

Broadband ISDN is expected to offer full-motion video services at rates of about 150Mb/s. An immediate goal for a photonic switching system is to accommodate the management and transfer of such large volumes of video information. Eventually, more than 100,000 terminations will be required in the switching system.

Switching methods generally can be divided into circuit switching and ATM switching methods. It is difficult to realize photonic ATM switching systems[5][6], because they need complex traffic control, and optical logic devices are not developed so much. Therefore, the photonic switching system will be based on circuit switching at first.

To make use of the photonic features which are high-speed, broad bandwidth, and non-induction, the authors are planning the switching system without using optical-electronics converters.

As the capacity of channels increases, optical interconnection becomes more difficult. Therefore, it is an important technical issue to construct the switching system hardware as small as possible.

A Combined Photonic TD and WD Switching Network

A switching system mainly consists of a switching network, a call processor, line subscriber circuits, and terminal equipment. Each line subscriber circuit sends information from terminal equipment to the switching network and a control signal to the call processor. The switching network switches the information according to the call processor. Photonics will first be introduced to the switching network.

To make such a large capacity switching network, the three categories must be combined, because it is difficult for an individual method to achieve sufficient multiplexity. Since the total multiplexity in the combined TD and WD switching network is given by the product of TD and WD

multiplexity, the combined network is much more efficient than the individual networks.

A tunable wavelength filter and a converter are used for WD switching. Then, a bistable laser diode memory and an optical switch are used for TD switching.

Fig.1 shows the proposed switch element(SE) using combined TD and WD techniques. A tunable wavelength filter, a bistable laser diode (BSLD) memory, an optical switch, and a tunable wavelength converter are cascaded to form a switch element. In the switch element, an input optical signal is selected by the filter. Then, its time-slot and wavelength are switched to an arbitrary time-slot and an arbitrary wavelength.

Fig.2 shows the configuration of the combined TD and WD switch module using the switch elements. Switch element groups are arranged at every crosspoint and consist of a splitter, multiple switch elements, and a combiner. The input optical signals are distributed by the splitter, and are directed to all the switch elements. The combiner sums the cumulative output from the switch elements.

It is possible for the combined TD and WD switch module to expand line capacity by adding additional switch element groups according to the number of highways required. The number of elements in a switch element group is determined according to the current system properties.

Fig.3 is the operation principle for a switch element where the WD multiplexity is 2 and the TD multiplexity is 4. Optical signals are TD-multiplexed in a bit-interleave format and then WD-multiplexed onto each input highway. The tunable wavelength filter periodically extracts an optical signal (time-slot T_1 and wavelength λ_1). The BSLD memory then stores the filter's output signal during the time frame, and the optical switch reads the signal stored in BSLD memory at time-slot T_3 in the frame. Finally, the tunable wavelength converter transforms wavelength λ_1 of the optical switch output signal to wavelength λ_2.

In the switch element, high-speed switching is required by the tunable wavelength filter, the BSLD memory, and the optical switch. However, high-speed switching is not required for the tunable wavelength converter, because it operates during the call set-up phase.

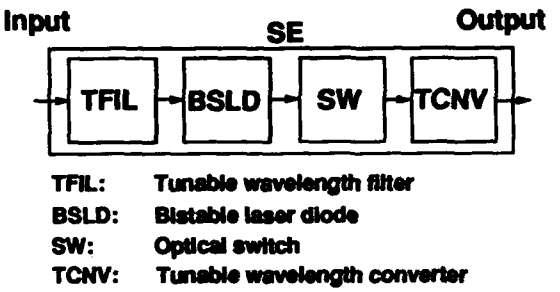


Figure 1. Proposed switch element (SE)

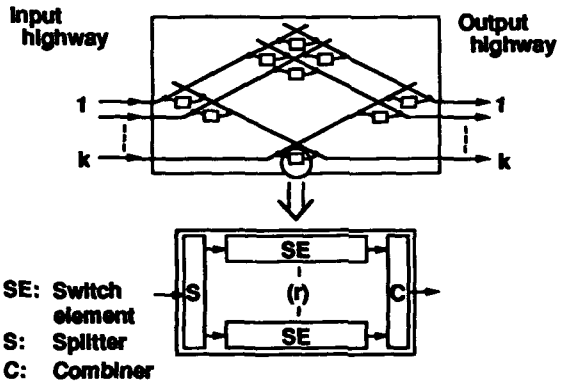


Figure 2. Switch module configuration

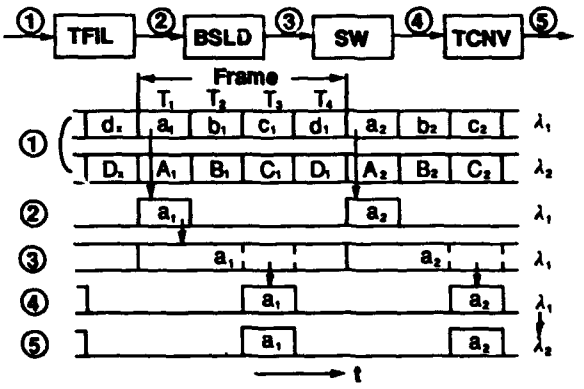


Figure 3. Operating principle

A large switching network can be constructed by connecting TD and WD switch modules together in a multi-stage configuration. Fig.4 shows a three-stage construction. In this configuration, if the TD multiplexity is 100 and the WD multiplexity is 10, the capacity of the switching network is 100,000 channels.

Number of optical devices required

Fig.5 is a calculation model to compare the number of optical devices required for the proposed structure and the conventional structures. The model corresponds to a two-stage structure. Every switch has $m\,n$-input and $m\,n$-output, and is strictly nonblocking. M-links are provided between individual first stage and individual second stage.

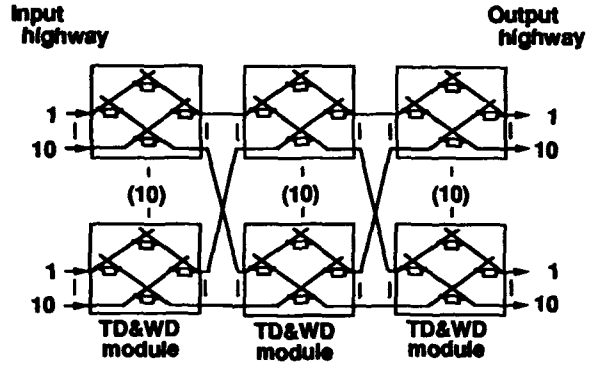


Figure 4. A combined TD and WD *switching network*

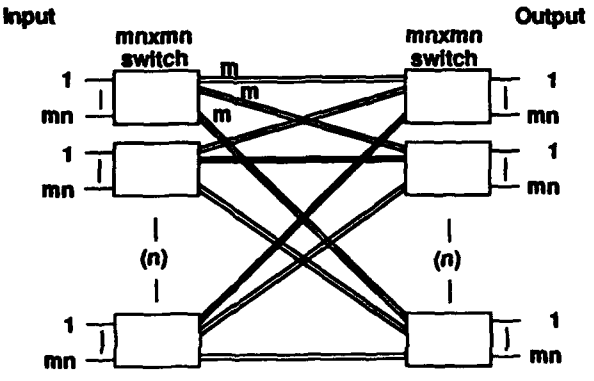


Figure 5. Calculation model

Table 1 lists the number of optical devices required for the proposed TD and WD switching network, the conventional TD and WD switching networks, and the conventional TD switching network without WD switching. In this comparison, WD multiplexity is n and TD multiplexity is m. The number of highways is n in the TD and WD switching networks, and n^2 in the TD switching network.

The conventional TD&WD-A structure is based on applying the tunable wavelength filtering technique to internal time switching, and the TD&WD-B structure is based on applying the tunable wavelength transformation technique to an internal time switch[7].

As shown by this table, the number of required optical switches can be reduced by introducing WD technology to the TD switching network. The proposed structure can further reduce the amount of BSLD memory required by introducing both tunable wavelength filtering and conversion techniques to the TD switching network. The proposed structure needs both a tunable wavelength filter and a converter. However, as listed in the table, the total number of tunable wavelength filters and converters required for the proposed structure is equal to the number required for the conventional TD&WD-A structure and the TD&WD-B structure.

In summary, the proposed architecture seems suitable for combined photonic TD and WD switching in a small hardware package.

Conclusion

A combined photonic TD and WD switching network has been proposed for a photonic switching system. The proposed structure is

Table 1. Number of required optical devices

		WD multiplexity: n		TD multiplexity: m		
Structure		TFIL	TCNV	BSLD	SW	Total
Proposed TD&WD		mn^2	mn^2	mn^2	mn^2	$4mn^2$
Conv.	TD&WD-A	$2mn^2$	—	$2mn^2$	$2mn^2$	$6mn^2$
	TD&WD-B	—	$2mn^2$	$2mn^2$	$4mn^2$	$8mn^2$
	TD	—	—	$\simeq 4mn^2$	$\simeq 8(m+n)n^2$	$\simeq (12m+8n)n^2$

more economical to construct than conventional structures because of the introduction of both tunable wavelength filtering and conversion techniques into the TD switching network. This switching network can expand the line capacity to 100,000 channels.

Acknowledgment

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High-Speed Wavelength Switching Experiment for Wavelength-Division and Time-Division Hybrid Switching Networks Using $LiNbO_3$ Fabry–Perot Tunable Wavelength Filters

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Abstract

Fast wavelength switching of less than 0.4 ns has been realized when using a $LiNbO_3$ tunable filter. This permits wavelength-division and time-division hybrid switching networks to adopt a 2-Gbps bit-interleaved signal form.

1. Introduction

Wavelength-division (WD) and time-division (TD) hybrid switching networks are expected to be one of the strong candidates for future broadband ISDN (B-ISDN) H_4 signal (around 150 Mbps) STM switching networks[1]. In these switching networks, high-speed wavelength switching operation of tunable wavelength filters is necessary. Recently, to confirm the feasibility of an 8 WD and 4 TD hybrid switching network to cater for 100 Mbps signals, a wavelength switching experiment was demonstrated with a TD multiplexed signal in a byte-interleaved signal form with 6.7 ns guard-time. Wavelength switching within the guard-time was accomplished[2], by using phase-shift-controlled DFB LD tunable wavelength filters[3]. However, a bit-interleaved signal form is more suitable for the hybrid switching network than that of a byte-interleaved signal form, because of the amount of hardware required for the time switch, used for the hybrid switching networks. To employ the bit-interleaved signal form, improvement in the wavelength switching time is required for tunable wavelength filters. Wavelength switching in times of 1-ns has been reported, using a DFB LD tunable filter[4]. However, this type of filter with wavelength tuning principle is based on the effective refractive index change due to the carrier injection effect, lacks the possibility of achieving less than 1-ns wavelength switching time. This is mainly doe to the value of the carrier life time.

In this paper, for achieving high-speed wavelength switching, we propose an application of a $LiNbO_3$ Fabry-Perot (LN FP) tunable filter to the WD&TD hybrid switching network. The resultant high-speed wavelength switching of less than 0.4 ns permits the WD&TD hybrid switching networks to adopt a 2 Gbps bit-interleaved signal form.

2. WD and TD hybrid switching network

Figure 1 shows a proposed WD and TD hybrid switching networks. It is constructed by combining WD and memory matrix time (MMT) switching techniques[5]. In the WD&MMT switching network, WD and TD multiplexed input optical signals from input ports are split into r and they are sent to individual tunable wavelength filters. Here, a specific wavelength signal is selected from the multiplexed optical signal after every time-slot. Extracted output optical signals undergo opto-electronic conversion and are then applied to the MMTs. Signals are then exchanged between arbitrary time-slots and are transmitted from arbitrary output ports to wavelength tunable E/Os. Finally, the tunable wavelength E/Os, which

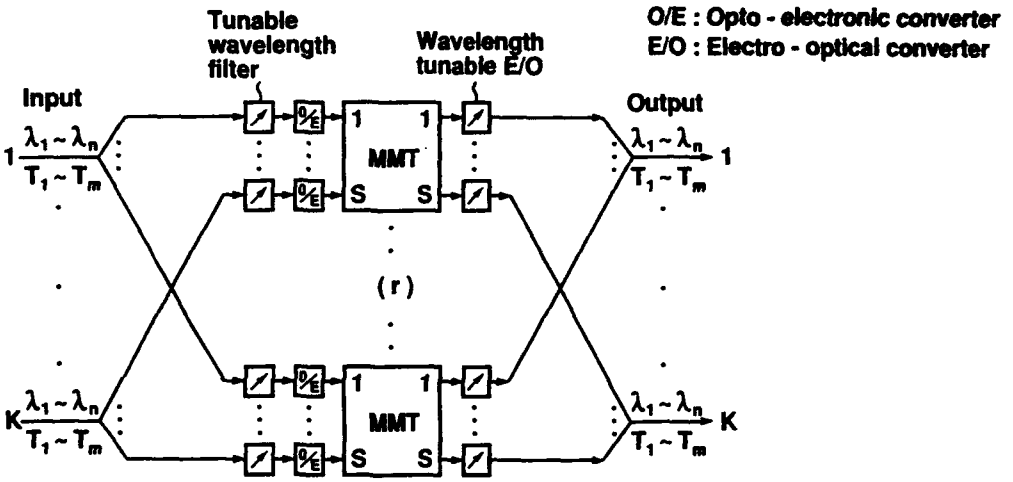


Fig. 1 WD&MMT switching network

include wavelength tunable laser diodes (LDs), convert the MMT output signals to an arbitrary wavelength optical signal after every time-slot. Subsequently, these signals are transmitted to the output port. In brief, the WD&MMT switching network can exchange optical signals multiplexed in both wavelength and time domains among arbitrary input and output ports.

In the WD&TD hybrid switching network such as the WD&MMT switching network with a bit-interleaved signal form, high-speed wavelength switching operation of tunable filters is necessary. For example, when eight B-ISDN H_4 signals are TD multiplexed in a bit-interleaved return-to-zero (RZ) signal form , less than 0.4-ns wavelength switching time, corresponding to half of one time-slot duration, is necessary.

3. $LiNbO_3$ Fabry-Perot tunable filter

The electro-optic effect response time is as low as 10 ps[6]. However, the wavelength switching time for a $LiNbO_3$ Fabry-Perot (LN FP) wavelength filter, based on the electro-optic effect, is basically determined by the time constant for the load resistance connected to the electrode and electrode capacitance (less than a few picofarads). The LN FP tunable filter, therefore, has a capability of wavelength switching in times of less than 0.1 ns. The LN FP filter structure is shown in Fig. 2, indicating an 8-μm width optical waveguide fabricated on the X-cut $LiNbO_3$ substrate and electrodes connected to both sides of the optical waveguide. The LN FP tunable filter, which has a 3-dB down bandwidth of 0.26Å and a free-spectral-range of 5.5Å (finesse = 21.8), was designed by setting waveguide length (cavity length) at 1 mm and by coating for 87-% reflection at both facets, taking 0.02-dB/mm waveguide loss into account. Anti-reflection coated cleaved-ended single mode optical fibers were coupled with the optical waveguide.

Figure 3 shows the measured transmission ratio for the LN FP tunable filter. The free-spectral-range, 3-dB down bandwidth and finesse were 5.9Å, 0.3Å, and 19.7, respectively.

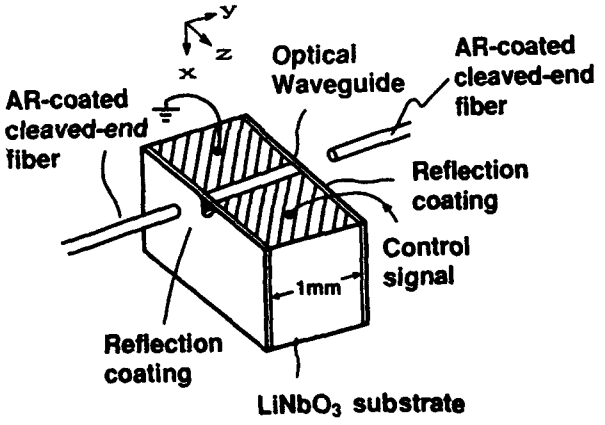


Fig. 2 An LN FP tunable filter structure

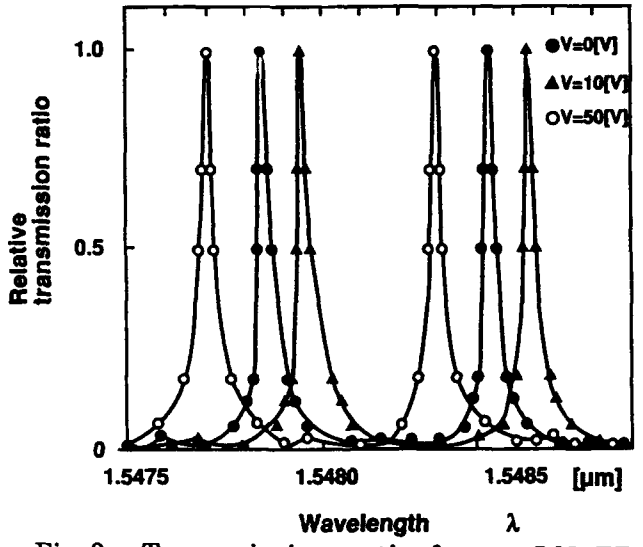


Fig. 3 Transmission ratio for an LN FP tunable filte

With applied voltages of 10 and 50 V, respective filter selecting wavelength shifts of 0.9 and 4.5Å were achieved, while also maintaining constant transmission characteristics. The wavelength tuning coefficient (the ratio of wavelength shift to applied voltage :$\Delta\lambda/\Delta V$) may be further improved by using structures which maintain stronger optical and applied electric field confinement.

4. Wavelength switching experimen

The wavelength switching experimental setup for the LN FP tunable filter is shown in Fig. 4. Two light carriers from laser diodes, with wavelengths were λ_1 and λ_2, were combined and led to an external modulator (MOD). Channel separation between λ_1 and λ_2 was 0.9Å. Using an LN modulator, the WD multiplexed light could be intensity-modulated at 1.2-Gbps or 2-Gbps RZ signals with 50 % duty. The modulated optical signal was then transmitted to the LN FP tunable filter. Because the RZ signal is assumed to be a TD multiplexed signal in a bit-interleaved form, the wavelength switching operation, therefore, must be accomplished, while the signal logic level is returned to zero. The filter selecting wavelength was switched by the electronic signal from a control signal generator bit by bit.

Figure 5 (a) shows a 1.2-Gbps input signal for a tunable filter, which is composed of both λ_1 and λ_2 wavelength signals. The filter selecting wavelength was sequentially switched between

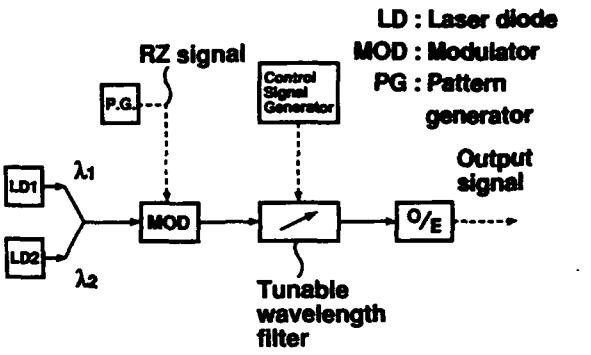


Fig.4 Wavelength switching experimental setup for an LN FP tunable wavelength filter

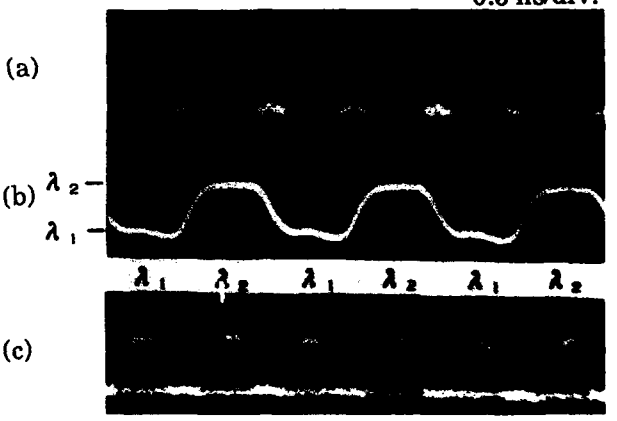


Fig. 5 Signal waveforms
(a) 1.2-Gbps input signal for an LN FP filter
(b) LN FP filter control signal
(c) LN FP filter output signal

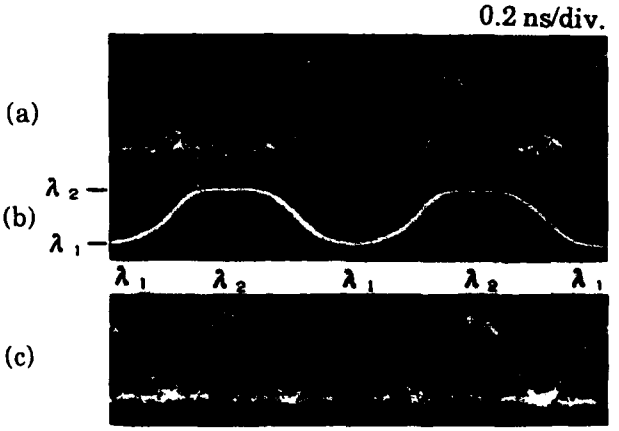


Fig. 6 Signal waveforms
(a) 2-Gbps input signal for an LN FP filter
(b) LN FP filter control signal
(c) LN FP filter output signal

λ_1 and λ_2, according to the control signal, whose amplitude was set to be 10 Vp-p, as shown in Fig. 5 (b). The tunable filter output signal shown in Fig. 5(c), was observed using an opto-electronic converter (O/E) with 5-GHz bandwidth.

In conclusion, using the LN FP tunable filter, wavelength switching in times of less than 0.4 ns between two wavelength signals has been successfully carried out. To confirm the possibility of even faster wavelength switching times, an experiment using a 2-Gbps RZ signal was also performed. Figure 6(a) shows a 2-Gbps input signal for the tunable filter. Using the signal shown in Fig. 6(b), the filter selecting wavelength was also sequentially controlled between λ_1 and λ_2. Finally, the λ_1 and λ_2 wavelength signals were sequentially selected at individual time-slots(Fig. 6(c)). These results indicate the possibility of adopting a 2-Gbps bit-interleaved signal form in the WD&TD hybrid switching networks, using the LN FP tunable filter.

5. Conclusion

Application of an LN FP tunable filter to WD&TD hybrid switching networks has been proposed. High-speed wavelength switching of less than 0.4 ns has been successfully performed, using the LN FP tunable filter. This makes it possible to use a 2-Gbps bit-interleaved signal form in the WD&TD hybrid switching networks. The high-speed wavelength switching operation among multi-wavelength signals will be achieved with an improvement in the wavelength tuning coefficient for the LN FP tunable filter.

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Logic and Control

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All-Optical Control Circuits for Photonic Switching

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ABSTRACT

This paper describes promising optical technologies for high-speed processing and discusses their essential applications to all-optical control circuits for photonic switching.

1. INTRODUCTION

Future communication services will require high-speed and intelligent control circuits as well as broadband information switching equipment. For switching equipment, optical switches are attractive because of their inherent broad bandwidth and immunity to induction. Various types of optical switches such as space-, time-, and frequency-division switches have been studied so far. For control circuits, the required functions fall into two categories, high-speed simple functions and low-speed intelligent functions. New optical technologies will be demanded for the former functions, though electronics will play an important role for the the latter as it does today.

For high-speed optical processing, the following optical technologies are available: 1) the use of optical processing partially through electronics; 2) the use of passive waveguide components; and 3) the use of optically activated optical devices. These applications to control circuits for photonic switching may include short pulse generation, optical signal filtering, and clock synchronization.

This paper describes some of these circuits that have been studied in our laboratories.

2.OPTICAL CELL GENERATOR USING A GAIN-SWITCHED LD

A high-speed optical cell switch for the photonic asynchronous transfer mode system will be a key technology for the future large-capacity communication systems. We have proposed an ultrafast optical cell generator[1] that uses a gain-switched semiconductor laser diode and Ti:$LiNbO_3$ optical switches (Fig. 1).

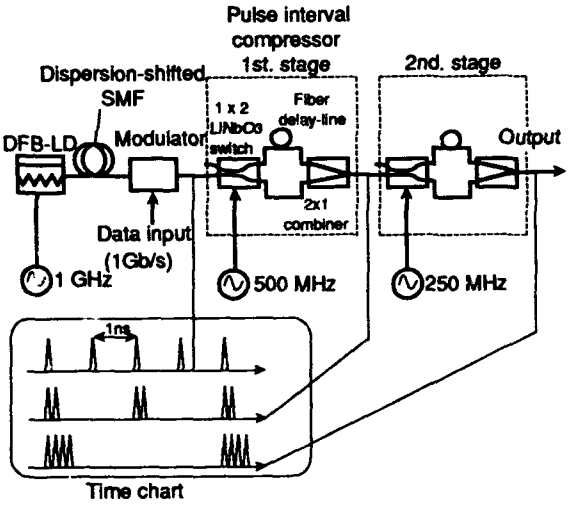


Fig. 1 Ultrafast optical cell generator

In this experiment, optical pulses emitted from the gain-switched DFB laser diode are coupled into a dispersion-shifted single-mode fiber to shorten pulse width. The obtained optical pulse series features a 1 GHz repetition rate and a 19 ps pulse width. These pulses are modulated by an optical intensity-modulator. The modulated optical pulses enter two stages of the pulse interval compressors. Each compressor consists of a 1x2 optical switch, two optical fiber delay lines, and a 2x1 optical coupler. At the first compressor, the 1x2 switch alternately sends pulses to the two delay lines by using a driving signal with a frequency of 500 MHz. These delay lines give

the pulses a relative delay, and the 2x1 coupler recombines the pulse with a pulse-width interval. As a result, two pulses are output from the first compressor every 500 ns period. At the second compressor, the frequency of the driving signal applied to optical switch is half of that used in the first stage. Thus a four bit optical cell signal was generated. The output was monitored with a streak camera having a 10 ps resolution. The experimental results are shown in Fig. 2. The bit rate of observed optical cell was about 40 Gb/s.

Although this circuit uses driving signals of less than 1 GHz, optical cell signals of several tens of Gb/s can be generated. The bit rate of optical cell signals is mainly determined by their pulse width. Because the generation of 6 ps full-width optical pulse using the gain-switched LD and pulse compression fibers have been reported, 160 Gb/s cell generation will be possible.

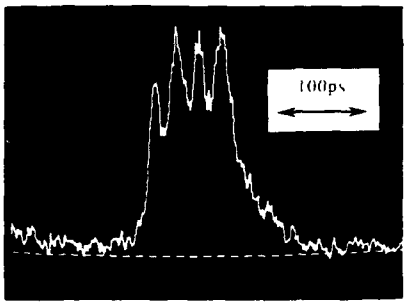


Fig. 2 40 Gb/s four-bit optical cell

3.OPTICAL SIGNAL PROCESSING USING PASSIVE WAVEGUIDES

Signal processing using passive optical waveguides as a delay medium has the advantage of being able to process broadband signals, because optical waveguides have a large available bandwidth. This section describes an optical transversal filter[2] and a pattern matching circuit[3] fabricated with high-silica waveguides. These circuits are similar in configuration and are constructed of optical power splitters, delay lines, and combiners. Progress in low-loss guided-wave devices ensures the use of long waveguides and stable operation.

3.1 Optical transversal filter

A configuration of an optical transversal filter is shown in Fig. 3. Optical signals introduced into the filter are tapped, weighted and then coherently combined. In this filter, any weighting coefficients, including complex numbers, can be set by using tunable optical power splitters and phase shifters. The distribution ratio achieved by each tunable splitter corresponds to the respective absolute value of the complex coefficient value. Phase shifters determine the argument of the complex coefficients.

The monolithically integrated filter was fabricated with embedded high-silica single-mode waveguides[4] on Si by flame-hydrolysis deposition and reactive-ion etching. The core was 6 mm wide 6 mm high. The relative refractive index difference was 0.7%. The tunable splitter is a symmetrical Mach-Zehnder interferometer, constructed to include two directional couplers, two arms, and a thin-film heater on one arm. Tuning function is carried out by using temperature-dependent refractive index change based on the thermo-optic effect. The heater shifts the optical carrier phase. The output of the splitter can be changed from 0 to 1 by shifting the phase difference between the two arms from 0 to p. The phase shifter is a waveguide on which a thin-film heater is attached. The unit delay length was a 1 cm-long waveguide (unit delay = 50 ps). Thus, the frequency characteristics have a periodic shape every 20 GHz. The optical combiner is constructed by connecting 9 directional couplers in a reverse tree structure.

Figure 4 shows the frequency characteristics of the low-pass filter. The solid line shows the measured characteristics and dotted line shows the theoretical characteristics calculated from the transfer function derived using the tap coefficients. The close agreement between them shows that this filter could be designed having any frequency characteristic.

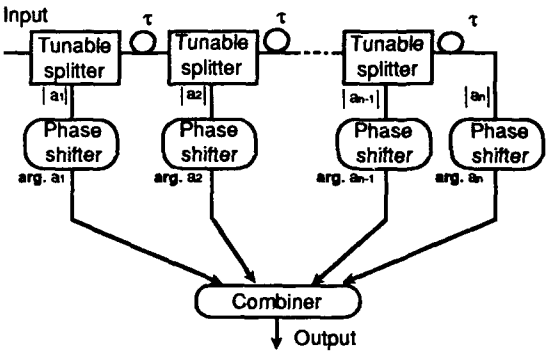


Fig. 3 Optical transversal filter

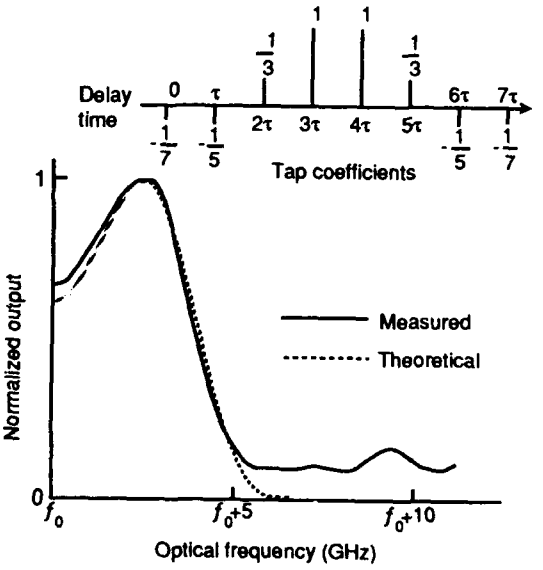


Fig. 4 Low-pass filter frequency characteristics

3.2 Optical pattern matching circuit

The schematic diagram of an optical pattern matching circuit is shown in Fig. 5. This circuit can detect any specified pattern in an optical signal sequence by correlation with a tapped delay line structure. The four-bit pattern matching circuit consists of a serial-parallel converter comprising a 1x4 optical power splitter and four delay-lines, a decoder with four phase shifters, and a 4x1 optical power combiner. PSK input signals are converted to parallel signals with serial-parallel converter. Optical carrier phases of the parallel signals are respectively shifted so that only those of the specified pattern are in-phase. The maximum output power is obtained when in-phase signals are coherently combined. The pattern to be detected is set at the phase shifters by changing the electric power to the heaters.

Figure 6 shows the pattern matching responses (upper traces) and the respective input patterns (lower traces). The maximum output was desirably obtained when MMMM apears in the input signal sequence. The extinction ratios measured when the input patterns differ from the MMMM pattern by one or two bits were respectively 5.3 dB and 13.2 dB.

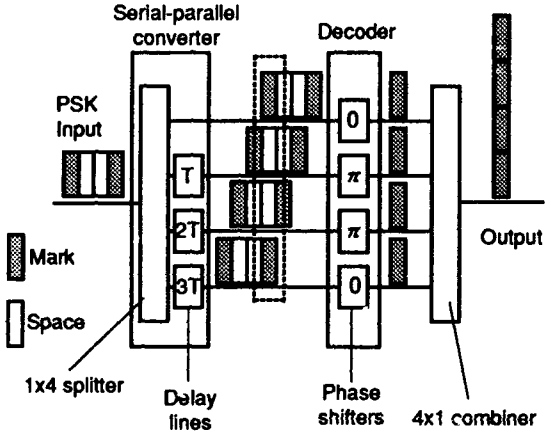
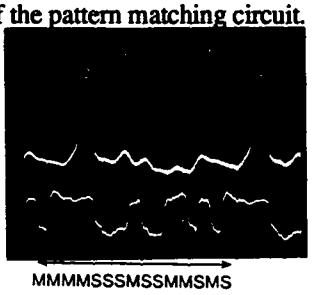
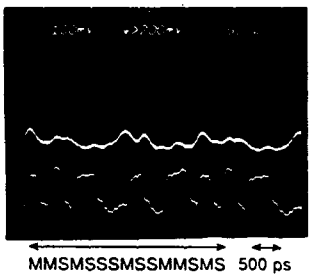


Fig. 5 Optical pattern matching circuit

An application to ATM-based photonic cell switching is also demonstrated by using this pattern matching circuit as a routing controller. Optical cells are sent through an 1x2 $LiNbO_3$ switch, and when the pattern matching circuit detects MMMM of four-bit PSK routing control signals, the output triggers a 4.3 ns electrical pulse to drive the optical switch. Cell signals and routing control signals were synchronized but not multiplexed for experimental convenience. 32 bits intensity-modulated optical signals at 10Gb/s were used as cells. An 1.1. ns guard-time was provided for each cell. Figure 7 shows the measured output signals from the optical switch. Optical cells were appropriately switched according to the MMMM detection. These results confirm the routing control capability of the pattern matching circuit.



(a) MMMM is in input



(b) MMMM is not in input

Fig. 6 Oscilloscope traces
Upper : pattern matching response
Lower: input pattern
The pattern set at the phase shifters is MMMM

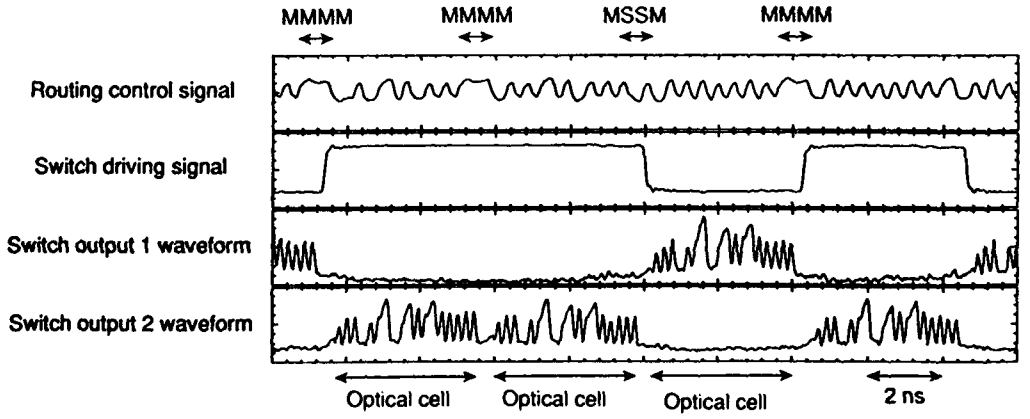


Fig. 7 Results of an optical cell switching experiment

4. ALL-OPTICAL SYNCHRONIZATION CIRCUIT

All-optical system synchronization and clock regeneration are the most important function for high-speed digital communication systems. We have recently proposed an all-optical synchronization circuits using a semiconductor laser-diode-based self-excited oscillator[5].

This all-optical synchronization circuit is shown schematically in Fig. 8. The self-excited oscillator consists of a semiconductor laser diode with an anti-reflection coating facet and an external cavity in which a quarter-wave plate is inserted. Self-excited oscillation is caused by polarization mode competition between the TE and TM waves. The quarter-wave plate converts a TE wave into a TM wave and vice versa. When no light is injected into the oscillator, it alternately emits the TE and TM waves. The output is obtained by choosing either the TE or TM waves. If the intensity-modulated light input is injected and the clock frequency of this input light is near the self-excited oscillation frequency, intensity-modulated synchronized clock output light is obtained.

In our experiment, the input light was a TM wave emitted by a DFB laser, and the TE component was chosen as the self-excited clock output. To obtain 10 GHz operation, the optical path length of the cavity was shortened to around 7 mm. A 10 GHz RZ "1010" pattern intensity-modulated light, was used as input. The waveform of the output is synchronized to that of input light as shown in Fig. 9. The average power of the input and the synchronized output lights were 150 mW and 500 mW, respectively. This experimental shows that the circuit has the potential for high-frequency operation.

The self-excited oscillation frequency is mainly determined by the cavity length. High-frequency operation will be possible because the periodic carrier density change in the laser diode is small.

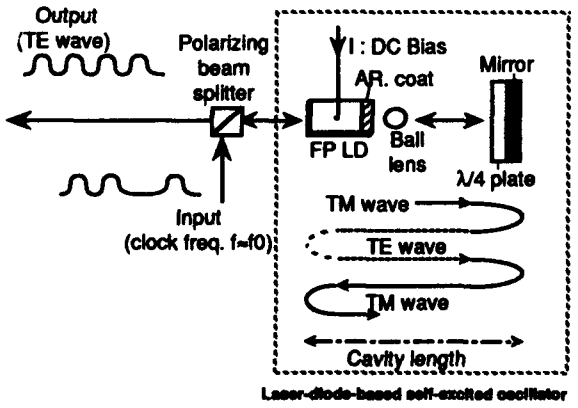


Fig. 8 All-optical synchronization circuit

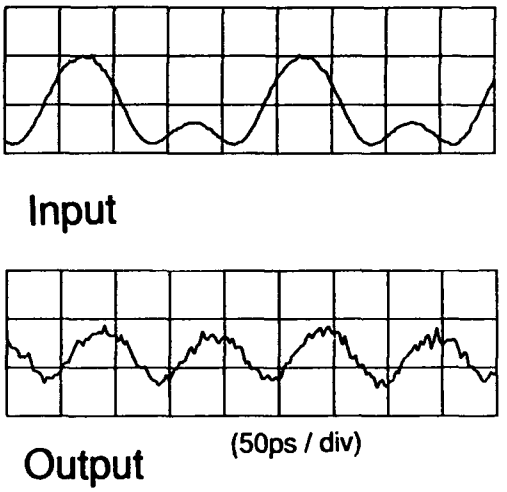


Fig. 9 Waveforms of input and synchronized clock output

5. CONCLUSION

Optical control circuits for photonic switching have been described. Our experiments demonstrate the potential of high-speed operation obtained by using optical technology. Although these all-optical control circuits are still in the basic research stage, they will play an important role in future photonic switching systems.

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Control Injection in Free-Space Photonic Switching Architectures

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Abstract

We compare four different methods of injecting control signals into photonic switches, and we study their effects on network performance, system complexity, and system packaging.

1. Introduction

All photonic switching architectures require control information to be injected into the nodes of the network fabric to permit appropriate routing of the traffic. A typical photonic switch (Figs. 1-4) consists of nodes arranged in stages (node-stages) which are separated by optical links (link-stages). Every node in every node-stage must have control signals routed into it in addition to the data inputs and data outputs, and depending on the reconfiguration rate of the network, the aggregate bit-rate of the control inputs entering a node-stage can sometimes be as high as the aggregate bit-rate of the data passing through a node-stage. Thus, it should be apparent that the problem of control injection is not at all a trivial problem. Control injection is an important aspect of photonic switches that should probably by given more attention, because the manner in which control is injected into the network has a large effect on the performance and operating capabilities of the network. This paper will study these effects for four different control injection schemes: 1) a distributed control scheme with self-routing packet headers, 2) a centralized control scheme with self-routing packet headers, 3) a centralized control scheme with spatial light modulators (SLMs), and 4) a centralized control scheme with direct node injection.

2. Network model for the analysis

In order to make a fair comparison, we must first make some assumptions and set up some constraints to bound the problem and put each of the different control injection schemes into a framework that can be suitably analyzed. Although the results of this paper will be general in nature, the specific network that will be modeled within this paper is an Extended Generalized Shuffle network[1] having N=256 inputs, 17 node-stages, and 2048 nodes per stage. The general systems that will be studied are free-space photonic switching systems with multiple stages of planar device arrays (such as S-SEEDs[2] or smart pixels) connected via imaging optics, with fiber bundles routing the data into and out of the system (Figs. 1-4).[3]

The network model will be operated as a time-division multiplexed (TDM) switch, because this application places the most demanding requirements on the reconfiguration rates and the control injection hardware. In particular, the target TDM network for this analysis will switch DS-0 signals (8-bit time-slots) carried in 155 Mbps data streams. Thus, there will be 2430 time-slots in each 125 microsecond frame, and network reconfiguration must occur once every 51 nanoseconds. The time-slots intervals, with duration $T_{time\text{-}slot}$, are separated by guard-band intervals of time $T_{guard\text{-}band}$, so we can define the bandwidth utilization as $U=T_{time\text{-}slot}/(T_{time\text{-}slot}+T_{guard\text{-}band})$. A low bandwidth utilization implies that the system will waste more bandwidth for control injection, so data rates within the network fabric often need to be increased to accommodate the incoming data stream. To avoid this problem, the bandwidth utilization should be maintained as high as possible. In any TDM system, four basic components are required. These include (1) the path hunt processor, (2) the control memo-

ry (and any associated memories used for isolation), (3) the memory-switch interface, and (4) the switching node logic. New call requests are sent to the path hunt processor, which determines an idle path through which the new call data can be routed. The results of path hunt are stored as control signals in the control memory, and they are read out and routed to the primary and shadow memories of a double-buffered memory. For all of the analyses below, we will assume that double-buffered memories are used, so data can be read of the shadow memory while new data is being written into the primary memory. The data is read out of the control memory in cyclic fashion (one control word is read out every time-slot), and it is routed through the primary and shadow memories to the control-switch interface (which can be either electronic or optical) to the switching node logic, where the control signal is used to actively route the data through the node. The control signals on the memory-switch interface can be transitioning only during the guard-band interval, and they must be stable while data is passing through the node during the entire time-slot interval. The comparisons below will show that these four basic TDM components can be physically distributed very differently in different systems.

3. Analysis of four control injection schemes

For each of the four control injection schemes listed above, we will study several architectural characteristics. These characteristics include the required node complexity, the complexity of the optical hardware, the required optical field of view, the tolerance to faulty nodes, the bandwidth utilization, the control memory requirements, the pinout/bandwidth requirements on the memory-switch interface, and the available space on the device or SLM substrates for memory-switch interface traces. Some general parameters that will be used within the analyses below include the number of inputs (N), the bitrate in the network fabric (B), the number of bits per time-slot (b), the number of node-stages (s), the number of control inputs per node-stage (n), and the number of time-slots that are concatenated to create a larger time-slot (c). For the analysis below, we will set N=256, B=155 Mbps, b=8, s=17, n=2048, and c=1.

3.1 Distributed control with self-routing packet headers

In the distributed control injection scheme based on self-routing packet headers, the four basic components for control injection are all contained within the node, as shown in Fig. 1. Incoming time-slots (with call request headers) are buffered and synchronized at the input of the network before being routed through the network nodes.The first $\log_2 N$ bits in each packet contain header information that is used for routing the raw data bits in the packet payload, so the guard-band interval (when control signals are loaded) occurs while the first $\log_2 N$

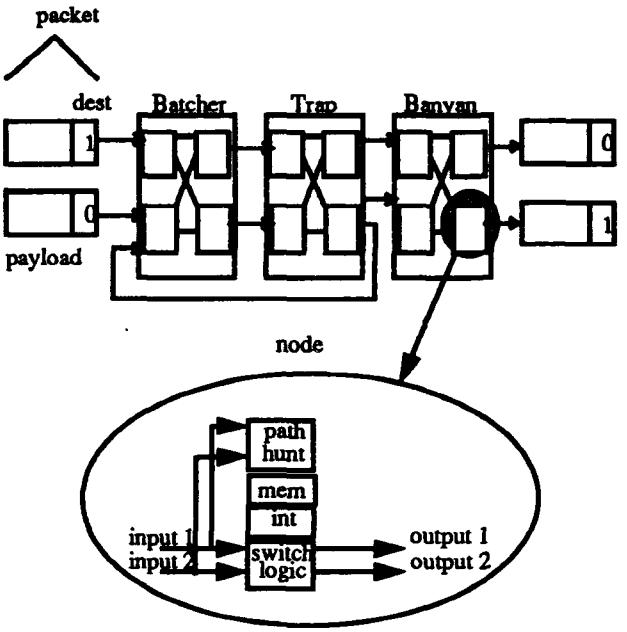


Figure 1. Self-routed distributed control.

bits are being routed.. The header information is processed by the local path hunt processor in each node, and the results of path hunt operations are stored in the localized control memory. The output of the control memory is tied directly to the local switching logic, so the packet header can then be routed to the desired node in the next stage, where the entire process is repeated by another node. Thus, the packet header flows along the same path as the packet itself, and the raw data follows the header. The control memory must hold the control bits for the entire duration of the packet. This control injection scheme requires relatively complicated logic for the path hunt processor within each of the nodes, so it also requires large fields of view for lenses imaging over the device substrate. An S-SEED implementation of the node would require 128 S-SEED devices, while a smart pixel implementation would require 106 transistors.[4] The optical hardware complexity is relatively complicated for this system, and the system is not very tolerant of faulty nodes. The bandwidth utilization is given by $U=(bc)/(bc+\log_2 N)$, so for the N=256 network implemented with a Batcher-banyan topology, the bandwidth utilization is a relatively low 0.50. However, the network requires only 33,664 (2x1)-bit memories

3.2 Centralized control with packet headers

The centralized control injection scheme based on packet headers places the path hunt processor functions in a centralized location, and the control memories have been distributed within front-end processors across all of the inputs to the network. The memory-switch interface and the switching logic are still contained within

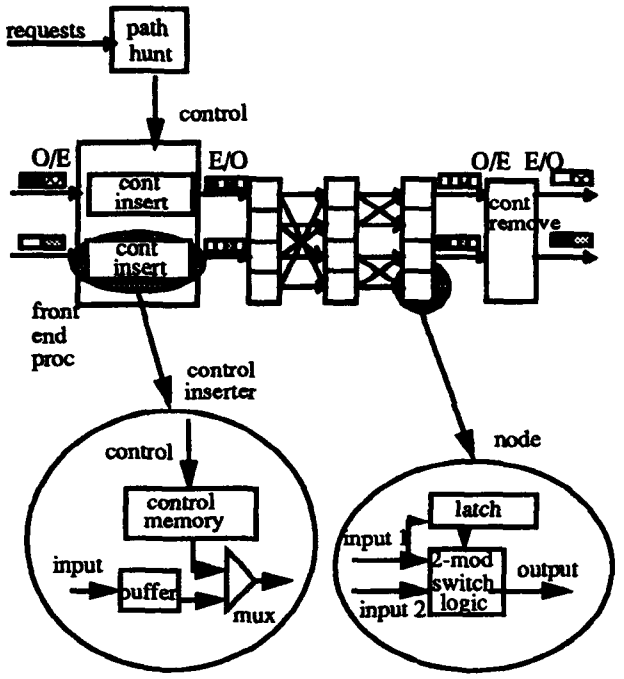


Figure 2. Centralized control with packet headers.

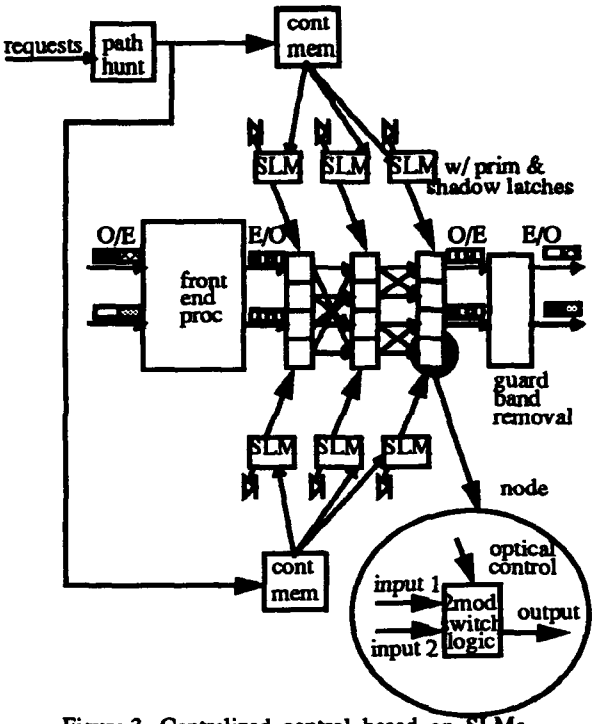


Figure 3. Centralized control based on SLMs..

each of the nodes, but a latch has also been added to the nodes (Fig. 2). Call requests are transmitted to the centrally-located, electronic path hunt processor, and the results are routed to the electronic control memory in the front-end processor. During the guard-band interval, the incoming time-slot is buffered at the input, and the control information from the control memory is multiplexed onto the input line and is directed into the nodes. While this control information is being routed through the nodes, the latches within the nodes extract the control bits and store them to provide appropriate routing within the nodes. The buffered data within the front-end processor can then be routed through the switching logic based on the control bits that are stored in the latches. Since the path hunt processor has been removed from the node, a typical node with a shadow memory requires only a few logic gates. Thus, the field of view on lenses imaging over the device substrate with these nodes is relatively small. Unfortunately, the optical hardware is still somewhat complicated, and the scheme is not very tolerant to node faults, because an error in a single node can corrupt the control bits in many nodes. The length of the guard-band interval is directly related to the number of node-stages, because U=(bc)/(bc+s). Thus, for the N=256 network with s=17 node-stages, b=8, and c=1, this results in a very low bandwidth utilization of 0.32. This network also requires 2048 (2430 x 17)-bit control memories and 34,816 1-bit latches within the nodes.

3.3 Centralized control with SLMs

In the centralized control injection scheme based on SLMs, electronic control signals are produced by a centrally-located, electronic path hunt processor and stored in an electronic control memory located near the path hunt processor. The output of the control memory is then transferred into the SLMs, where the control signals are converted into optical signals before being routed onto the device arrays within the photonic network, where the switching logic within the node is implemented by optical logic devices or by smart pixels. The SLMs in this analysis were modeled as double-buffered memories (requiring a primary latch and a shadow latch to be associated with each pixel).The actual state of the SLM pixel is modified when a new bit is loaded into the shadow register, and the amount of time required to change the state of a pixel is denoted T_{SLM}. A SLM pixel can only be modified during the guard-band interval. In the system of Fig. 3, M=2 SLMs are shown associated with each node-stage, and each SLM is used to control a different region of the optical logic devices in a node-stage. As in the previous scheme, the nodes can be greatly simplified to a few logic gates, so the lens field of view required for these nodes is relatively small. However, the optical hardware is very complicated because of the addition of the M SLMs. This scheme is very tolerant to node faults, because a faulty node affects only paths through that node. In addition, the N=256 network requires only 17 (2430 x 2048)-bit control memories, but each SLM pixel must have a pair of 1-bit registers (primary and shadow latches) associated

with it. The bandwidth utilization is U=(bc)/(bc+T_{SLM}), and this can be increased by decreasing the time required to switch all of the SLM pixels, T_{SLM}. The use of a double-buffered memory separates the writing of the control bits into the primary memory from the loading of the shadow memory and the switching of the SLM pixels. For a SLM with double-buffered control memories,the control bits can be written into the primary memory while data is being passed through the nodes, but all of the control bits for all of the nodes must be written into the primary memory within a time-slot interval. The time required to write all of the control bits is determined by the bandwidth of the pinouts on the SLM package. If we use a simple multiplexing scheme that places X control bits on a single SLM pinout, then the number of pinouts on the SLM package is n/(MX)+ $\log_2$X, and the number of pinouts is minimized when X=(n/M)*ln(2). The bandwidth on each SLM pinout must be capable of supporting a bitrate of BX/(bc). Thus, if B=155 Mbps, M=1, X=16, n=2048, b=8, and c=1, then the resulting control scheme requires a SLM package with 132 pinouts, and each pinout must support a bitrate of 310 Mbps, which still requires a relatively ambitious electronic packaging design.

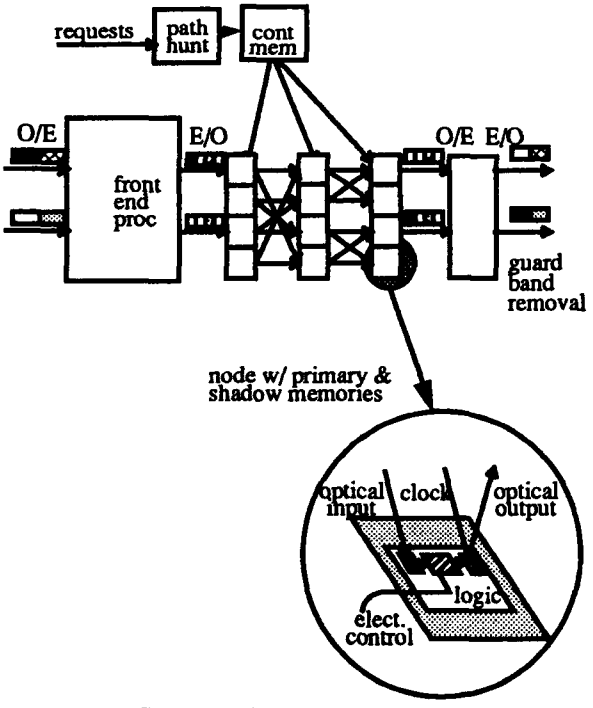


Figure 4. Centralized control based on direct control injection.

3.4 Centralized control with direct injection

In the centralized control injection scheme based on direct control injection into nodes, the centrally-located electronic path hunt processor stores control signals in an electronic control memory, and the electronic output of the control memory is transferred directly onto the substrate and into the nodes that are implemented by optical logic devices or smart pixels (Fig. 4). All of the control signals must be modified during the guard-band interval. The nodes are very simple in this scheme. but the lens field of view must be large enough to provide space on the device substrate for control signal traces. The optical hardware is very simple, and the scheme is very tolerant of faulty nodes. The N=256 network requires only 17 (2430 x 2048)-bit control memories along with 69,632 1-bit latches within the nodes.The bandwidth utilization is U=(bc)/(bc+T_{node}), which can be increased by decreasing the node switching time, T_{node}. Since double-buffered memories are used within the nodes, the primary memories can be loaded while data is passing through the nodes. The time required to load the primary memories is determined by the pinout and bandwidth constraints placed on the device array package, and this operation must be completed within a time-slot interval. If we use a simple multiplexing scheme that places X control bits on a single package pinout, then the number of pinouts on the array package is n/X+$\log_2$X, and the number of pinouts is minimized when X=n*ln(2). The bandwidth on each device package pinout must be capable of supporting a bitrate of BX/(bc). Thus, if B=155 Mbps, X=16, n=2048, b=8, and c=1, then the resulting control scheme requires a device package with 132 pinouts, and each pinout must support a bitrate of 310 Mbps. In effect, the pinout problems on the SLM package from the previous approach have simply been shifted to the device package.

Table 1. Problems in control injection schemes.

● = potential problem	Dist. control based on self-routing packets	Cent. control based on self-routing packets	Cent. control based on SLMs	Cent. control based on direct control
Node complexity	●			
Optical hardware complexity	●	●	●	
Optical field of view	●			
Tolerance to faulty nodes	●	●		
Bandwidth utilization	●	●		
# pinouts on memory-switch int			●	●
Bandwidth on mem-switch int			●	●
Available space for traces			●	●

4. Conclusions

Each of the control injections schemes described above has its own advantages and disadvantages, and the potential problems for each approach are shown in Table 1.These potential problems have been identified for the particular architecture that the authors were examining, and different architectures will undoubtedly encounter a different set of problem areas. In addition, these problem areas will shift around as optical technologies continue to improve, so this table should be treated as a temporally unstable entity. Nevertheless, several general trends have been identified as a result of this analysis. First, it is clear that the bandwidth utilization and the reconfiguration rate of a network are inversely related (fast reconfiguration results in lower bandwidth utilization), and the worst bandwidth utilization problems are encountered with the control injection schemes that employ packet headers. Secondly, aggregate bit-rates required for control injection are directly related to the network reconfiguration rate (fast reconfiguration results in high control bit-rates). Thus, most of the problems related to control injection are encountered when a network has high reconfiguration rates. Although this point may seem obvious, the resulting problem areas shown in Table 1 indicate that the solutions to these problems may require research in some areas that were not previously tied to photonic switching. In particular, future photonic switching netowrks that require high reconfiguration rates will undoubtedly reqûire smart pixel capabilities, because at a minimum, the switching nodes will need to have primary latches and shadow latches associated with them. In addition, high-performance, high-density electronic I/O will probably need to be integrated with-inthe smart pixel packages (or SLM packages) to permit access between the electronic path hunt processor and the switching nodes. Thus, optical researchers must begin working with electronic packaging researchers to provide both electronic I/O and optical I/O on the devices of the future. The results outlined within this paper have also shown that control injection must be considered at a very early stage in any photonic switch design, because many network characteristics are determined by the choice of a control injection scheme.

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Optical Connections

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Progress in Optical Interconnection Technologies and Demonstrators under the ESPRIT II OLIVES Program

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Abstract

OLIVES combines the skills of nine organisations to develop optical interconnect technologies and demonstrators. A review is given of the aims and progress to date.

Introduction

OLIVES (Optical Interconnections for VLSI and Electronic Systems) is a three year collaborative project which commenced in January 1989 and combines the complementary skills of four major electronics companies (STC, Siemens, Plessey and Thomson-CSF), a chemical company (Akzo) and five academic institutions (University College London (UCL), Foundation for Research and Technology, Hellas/RCC, Centro Nacional de Microelectronica (CNM), Interuniversitair Microelectronic Centrum (IMEC), and Eldgenössishe Technische Hochschule Zurich (ETH)). Some of the key aims and achievements to date in this project are described.

Subsystem Demonstrators

Four major demonstrators of optical interconnect subsystems are under construction, each at a different level within the hierarchy of system construction. These are supplemented by major technology demonstrators of low-power high-density optical interfaces, described in the following section, and of GaAs/Si technology.

Module/Subsystem Interconnects - The Optical Bus Demonstrator

Figure 1 shows an optical realisation of a conventional electrical time division multiplexed bus. A number of nodes (eight in this case) separated by 0.5 - 5 m are connected by multimode ribbon fibre through an array of passive star couplers. The demonstrator will have an aggregate bit rate of 6 Gbits/s but the same technology is capable of total rates up to 32 Gbits/s, which exceeds the projected performance of even the most ambitious electrical busses. Multiple instances of the basic unit shown could be combined to achieve a total rate of 100s of Gbits/s.

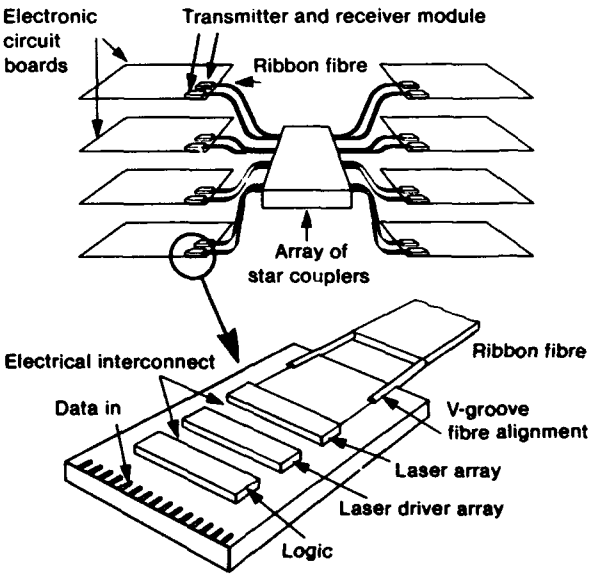


Figure 1. Module interconnects - optical bus

At each node is a compact array transmitter and receiver module based on silicon motherboard opto-hybrid technology[1]. This uses silicon v-grooves to align the fibres and provide reflective structures, solder bump self alignment of the laser and receiver arrays, and a high density interconnect on the silicon substrate to make electrical connections to the hybridized driver chips and passive components. This is the key to achieving the integration density required to minimize the size and power dissipation of the modules. The simulated dissipation of a transmitter array hybrid operating at 32 Gbits/s is 15W, and that of the receiver is similar.

Backplane Interconnects - The Mastercard Demonstrator

Figure 2 shows the concept of the mastercard demonstrator[2] for backplane interconnects. The 'mastercard', which is fabricated from a conventional borosilicate mask plate as used in the micro-electronics industry, is provided with computer generated holographic elements. These holograms, which have a grating constant of 1.2μm, deflect the beams to direct them to the required electronic daughterboard and split the power to provide fanout. Collimation optics, contained in the packages of the emitters and receivers, eliminates the requirement to realise this function holographically and improves the overall performance. Early mastercards, assembled for clock distribution with a fanout of 4, gave a measured optical clock skew of 100ps, an excess loss of 7 dB and a non-uniformity between the 'receiving' elements of 0.9 dB.

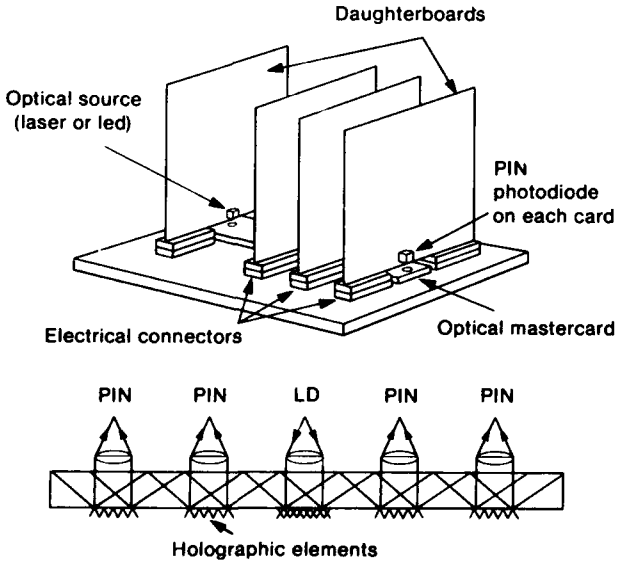


Figure 2. Backplane Interconnects - Mastercard

The principal advantage of this scheme is the reduction of the volume required for the interconnection. For example, in an 8 board system, the clock distribution network occupies some 120 cm^3 in conventional electronic technology (using co-axial cables), while the optical mastercard occupies only 5 cm^3. The gains when more boards are required, or where multiple data paths are to be provided, are even more spectacular.

Board/MCM Interconnects - The Waveguide Array Demonstrator

Figure 3 shows a schematic of an optical overlay to a silicon multichip module[3]. Conventional electrical interconnects are used for the short distance interconnections, while arrays of silica-on-silicon waveguides in the overlay provide the long distance parallel data connections. The demonstrator will comprise an eight channel parallel link using a single mode waveguide array, laser diode arrays and photo-receiver arrays. The pitch of these arrays is 125 μm. The waveguides are fabricated by flame-hydrolysis. Silicon micro-etching is used to produce submounts and alignment features for the assembly of the demonstrator.

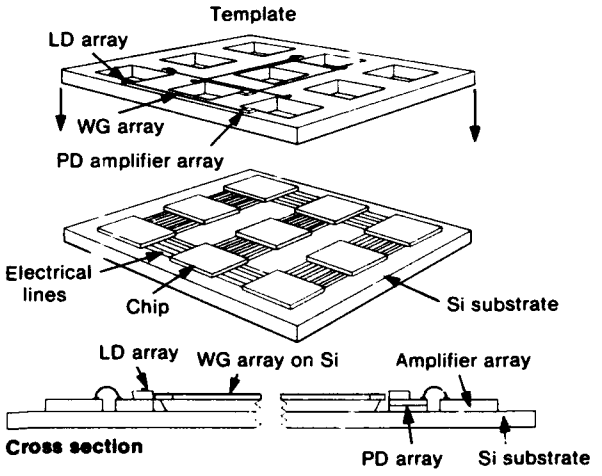


Figure 3. MCM interconnects - waveguide array

Chip Interconnects - The Chip Level Clock Distribution Demonstrator

Within a single chip the delay (typically 0.5 ns or more with state of the art technology) caused by the conversion of electrical signals to optical signals and back again makes the use of optical interconnection for data unattractive in most instances. Clock signals, however, are distinguished by a requirement to minimise differential delay. The superior fanout capability of optics allows electrical buffer stages to be eliminated and path length differences minimised, the main sources of chip-level skew. Figure 4 is a schematic of the chip level clock distribution demonstrator[4]. A laser diode adjacent to the chip is reflected onto a multiplexed computer generated holographic element, realised as a relief structure etched in silicon with an SF_6 plasma and metallised with Ti/Au to improve the reflectivity. The light is focused by the hologram onto four photodiodes on the chip. A diffraction efficiency into the first order of 39% has been measured with the binary holograms realised to date, close to the theoretical maximum of 40%. Calculations of the improvement in clock skew in a typical chip give an estimated reduction from 2 ns to 350 ps with a fanout of 17 which is easily achievable, corresponding to an increase in maximum speed from 50 MHz to nearly 300 MHz.

Technology Development

The programme includes a significant effort devoted to optimisation of the optical pathways (i.e. holographic elements and waveguides), parts of which are described above. In addition, there are tasks to develop specific optoelectronic components and component hybridization techniques.

Optoelectronic Interfaces

A key component of several of the demonstrators is a receiver array. A monolithic 8-element array has been designed and fabricated[5] on a commercial ECL process. One variant of this is designed for solder-bump mounting of a photodetector array which was also fabricated within the programme. The entire 8-element array is about 2.3 mm square and gives an ECL-compatible output. The first samples of this device have a measured total power consumption of 280 μW, including the output buffers, a delay of 1.4 ns, and a minimum input level for the '1' state of 7 μA. No measurable inter-channel crosstalk has been detected. The area of a single channel is equivalent to that of 4 ECL gates. This device (or its wirebond variant) will be used in several of the demonstrators. In addition, CMOS receivers have been designed operating at 50 MHz with a power consumption of only 1.17 mW per channel and a 4 μA sensitivity[6].

Figure 5 shows an array of 64 reflective MQW modulators based on the asymmetric Fabry-Perot design[6,7]. These are substrate entry devices designed for flip-chip mounting. With a 5V drive signal, a contrast ratio of up to 3 dB with a loss of 2 dB has been achieved. This was with a device of 100 μm diameter having 47 quantum wells of 110Å. A free space interconnection of adjacent VLSI chips will be assembled, based on this type of modulator, to demonstrate the potential of these devices for optical interconnects with very low power.

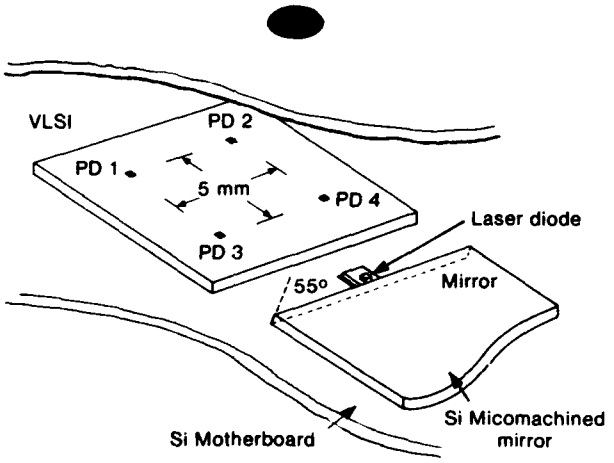


Figure 4. Chip level clock distribution

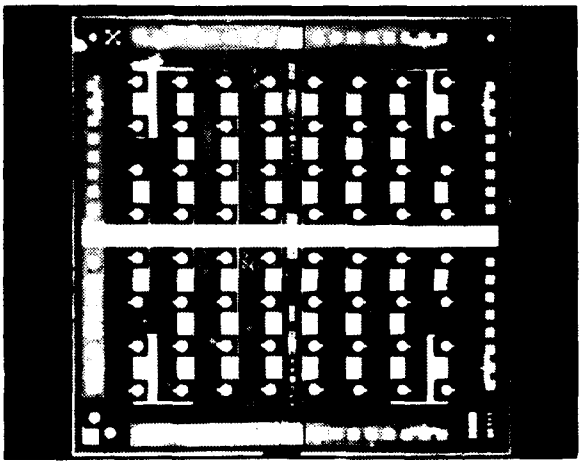


Figure 5. 64 element MQW modulator array

Component Hybridization

Several methods for the precision mounting of optoelectronic components are under development within the project. The most flexible of these is solder bump mounting, where the surface tension of molten solder is used to pull the components into precise alignment. Figure 6 shows a 3-layer assembly made with this technique. This comprises a modulator array, similar to that described above, flip chip bonded onto a silicon mount together with a (simulated) diffused glass array, using a combination of high melting point (300°) and low melting point (180°) SnPb solders[6]. The alignment accuracy between the top and bottom layers was assessed using verniers and found to be better than 2 μm. A flux-less technique for the mounting of lasers and laser arrays based on AuSn eutectic solder has also been developed[1], and arrays have been mounted using this process with no observable performance degradation.

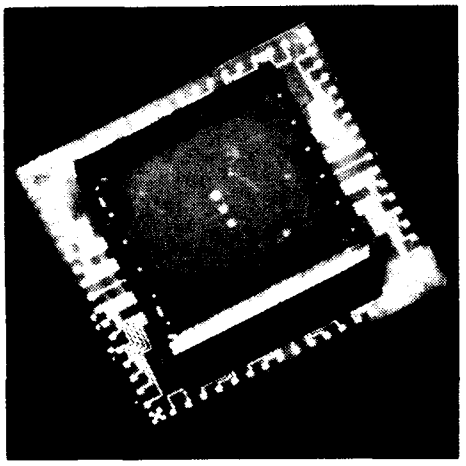


Figure 6. Three layer solder - bumped assembly

Other Activities

Other activities include a critical assessment of the demonstrators against the system requirements of the industrial partners and the investigation of certain other possibilities, notably direct, high density, free space interconnects between adjacent parallel boards and optical backplane busses. In addition there is an ambitious task to demonstrate the technology for monolithic integration of MQW modulators with CMOS circuitry. A key achievement of this activity is the demonstration of both growth and pre-growth substrate preparation at a temperature of less than 400°C.

Acknowledgments

The author would like to acknowledge the assistance of all the members of the OLIVES team. The work was supported by the Commission for the European Communities under project 2289.

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Space-Variant Holographic Optical Elements for Switching Networks and General Interconnects

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ABSTRACT

To realize optical interconnects of arbitrary design, space-variant optical elements are necessary. For such applications planar holographic optical elements (HOE) offer the highest degree of flexibility and ease of production, however their diffraction-based operation gives rise to chromatic aberrations. If semiconductor lasers with poor wavelength stability are used as optical sources, the problem of chromatic aberrations can seriously limit the operation of a HOE. In this work estimates for the number of independent space-variant interconnects, their spatial tolerances and their wavelength stability are considered.

1. INTRODUCTION

Optical interconnects enable the transmission of ultra high frequency signals with small crosstalk and rather low waste energy per interconnection. As a consequence the superposition principle, transmission lines in free space may cross each other without interaction. This is in sharp contrast to electrical interconnects which exhibit strong crosscoupling effects especially with high data rates.

Two applications for optical wiring concepts can be identified, namely, fixed pattern chip-to-chip (or board-to-board) interconnects/1,2/ and reconfigurable switching networks or bus systems where the interconnect path is selected out of a number of fixed interconnects by means of so-called exchange bypass modules (EBMs) /3,4,5,6,7/. In all free space interconnect concepts the dimension perpendicular to the planes containing the electronics and the transmitters and/or the detectors is used.

Chip to chip interconnects can, for obvious reasons, be made in the space above or below the chip plane if free space optics is used. Optical fibers provide an optical alternative to free space chip-to-chip interconnect systems, however for complex interconnect systems it may be difficult to make a suitable fiber structure. Common to all solutions of optical interconnecting systems are planes containing the electronics, the transmitters (e.g. laser diodes/8,9/) or receivers (photodiodes) at the other end of the interconnecting stage. Since the free space optical interconnects are rather short and accordingly free from dispersion, the upper cutoff frequency of the optical interconnect is determined mainly by the electronic elements. Even with long range interconnects data rates of up to 10 GHz were reached /10/. Therefore, the limits for chip-to-chip interconnects and switching networks are mainly determined by the heat dissipation problems in the transmitter and receiver planes and not by the effects of optical propagation.

In this publication only the optical features of short range optical interconnects shall be discussed, as are:

- --- interconnect concepts,
- --- packing density,
- --- scaling laws,
- --- crosstalk,
- --- chromatic tolerances,
- --- sensitivity to misalignements,
- --- packaging concepts.

2. INTERCONNECT CONCEPTS

A general feature of optical interconnects is that light must leave the board/chip-

plane in order to give room for the interconnect fabric, i.e., the light leaves the board-plane perpendicularly (or some angle). Optical elements necessary for such interconnects are:

--- collimating or focussing elements, and
--- deflecting elements.

From the point of view of realizing such elements, gratings, or more general, holograms seem the most promising. These elements may be planar and can be configurated in arbitrary manner as dictated by the design. As has been shown/11/ HOEs can be used to collimate and also to deflect light (collimation embraces deflection).

However, diffractive elements typically redistribute the incoming light into several diffraction orders which result in a waste of the light necessary to drive the next stage. The concentration of the light into one diffraction order can be achieved either by using thick holograms /12,13/ or by using blazed grating structures/14,15,16/. Thick HOEs are generated by the exposure of thick light sensitive material, e.g., dichromated gelatin (DCG) to a two beam interference pattern. Blazed HOEs are generated with the help of lithographic techniques. The difference between the two approaches is that thick or volume HOEs have a high carrier frequency, whereas due to their realization as phase relief structures and due to difficulties with computing and writing computer generated HOEs have a lower frequency content. Despite these physical differences both approaches are subject to similar physical tolerances since the network or interconnect geometries especially have very similar character.

2.1.SWITCHING NETWORKS

Switching networks enable the arbitrary interconnection of N inputs with N outputs. The straightforward solution to this problem is the crossbar which requires N^2 switches. One proposed optical solution /17/ works with a spread of the input signals into matrix form and masking to get the output which causes a fanout loss of N. Cascaded switching networks on the other hand save switches and have the advantage that only small fanout values are necessary /7/. Such networks usually consist of planes containing switches in matrix arrangement which carry out exchange bypass operations for next neighbouring channels and of interconnect modules, e.g., made from HOE-array optics (Fig.1). These interconnect modules provide space-variant permutations. The light from each channel is collimated and

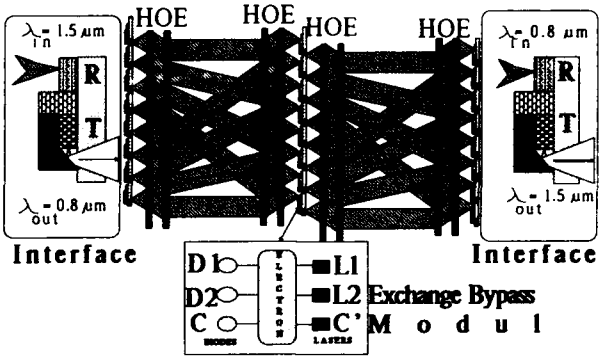


Fig.1 Schematic for a 3D-optical switching network. The network allows for the interconnection of N inputs with N outputs in arbitrary order. It consists of several identical stages having a transmitter plane, an optical free-space permutation network using HOE-arrays, and a receiving plane with photodetectors as inputs. These planes are working electronically and allow for logical next neighbor operations and are in this design assumed bifacial.

deflected in a predetermined manner. The HOEs collimate, deflect, and focuse the light originating from the transmitter plane onto the receiving plane in such a manner that each transmitter is connected to one receiver in the wanted order. That means each interconnected transmitter/receiver pair requires a different (space-variant) set of optical elements.

In Figure 2 several approaches to cascaded switching networks are shown (1 stage of such a network only). Fig.2.1 shows a realization using space-variant CGH-arrays. These arrays are preferably used with in-line arrangements, since the frequency range for the CGH is rather small on the condition that the numerical aperture of the laser is below 0.2. Fig.2.2 shows an arrangement with DCG HOE. Here an in-line arrangement can only be attained if one additional mirror is used per stage. The optical path length is about $\sqrt{2}$-times larger than in the previous case. Due to the high spatial carrier frequency the HOE is very sensitive to variations of the laser frequency with temperature.

So far, both functions (focusing and deflecting) are carried out by one HOE, nevertheless, for reasons of symmetry at least two HOEs are necessary per stage. We now consider arrangements where the collimating and the deflecting functions are assumed by different HOEs. Such an arrangement is called a "close cascade"/18/,19/. The primary advantage of the close cascade is

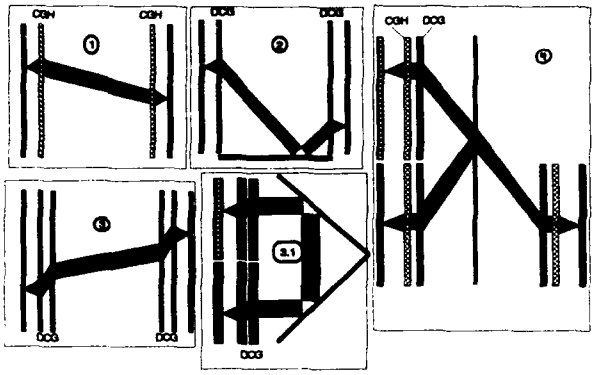


Fig.2 Interconnect philosophies using holographical optical elements for the stage of a 3D-free-space switching network.
2.1.) Computer generated holograms used for collimation and deflection.
2.2) Volume-HOE-version (DCG) incorperating a mirror to make in-line geometry possible.
2.3) Use of the close cascade of two Volume-HOE (DCG) each one at the transmitting end and one at the receiving end of the stage.
2.3.1) Same as before but designed for reflected light electronical planes.
2.4) Combination of CGH and Volume-HOE(DCG) to provide for the collimating and the deflecting functions of the interconnect.

that the chromatic aberrations of the holographic interconnect can be minimized and can be made to depend only on the remaining deviation angle necessary for permutations. Further, the generation of an array of identical collimating lenses is more easy than a more complex HOE. The seperation of the functions enables for the deflecting HOE-array the use of nearly plane waves during the exposure of the HOE alleviating the production process considerably. The close cascade of two DCG-HOEs is represented in the arrangement of Fig.2.3. The first array consists of identical HOE-lenses, the task of the second DCG-HOE is to redirect the nearly-planar incident waves according to the permutation or interconnect rules realized in the stage. The addition of two mirrors or a rectangle prism allows the same principle to be applied also in reflected light (Fig.2.3.1). If the expense in computation time can be reduced the use of CGH elements within a network structure becomes more attractive. Therefore, the combination of CGH lens arrays with DCG deflection holograms is a suitable choice, since the advantages of both techniques can be exploited. The main advantage is the ideal correction of the lens aberrations for the collimating lens array (Fig.2.4). This combination is applicable for setups in transmitted light and, with the addition of one mirror, also in reflected light. Due to the uncompensated high carrier frequency of the DCG-HOE the main disadvantage of such a solution is its wavelength sensitivity. This disadvantage can be overcome if a grating having the same spatial carrier frequency as the DCG-HOE is added, but, needless to say, the reduction in wavelength sensitivity is paid for a by a loss of efficiency and a reduction in the signal- to- noise ratio. Stray light becomes the main problem of cascaded HOEs.

2.2.CHIP-TO-CHIP INTERCONNECTS

Similar interconnect philosophies can be applied to chip-to-chip interconnects /20,21,22/. Here the interconnect geometries are not as regular as those of switching networks. Since the interconnection is made on the same chip or board, solutions similar to Fig. 2.3.1 are suitable. The reflecting mirror or prism should be subdivided to reduce weight and space needs. The plate thickness of the light guiding plate should be greater than required by diffraction theory (typically a few mm's to provide mechanical stability). Fig. 3 shows a proposal with a stacked interconnect plate. The in/out-coupling of the light is taken over by a close cascade array. If permutations or other irregular interconnect patterns are not required the second HOE can be replaced by a blazed grating. The grouping of the chip in- and outputs in lines or rows should not be a

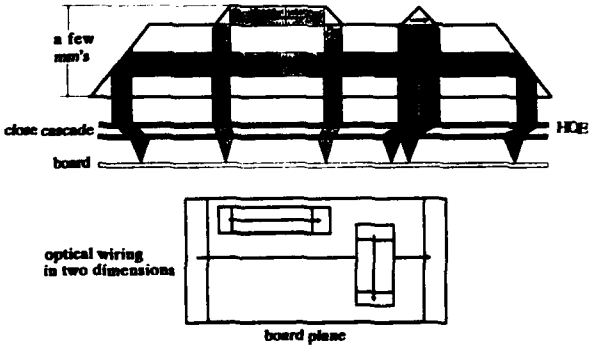


Fig.3 Chip to chip interconnect system using volume holograms of the DCG-type. The HOE combination provides for the focusing and the reflective optics for the light deflection. The deflecting element is stackable for 1D and 2D applications.

severe restriction on design freedom. As a matter of course, from the very beginning of the network design of the electronic circuitry should take into account the needs of the optics.

The deflecting HOE can of course make permutations in the line geometry itself without requiring a change in the light guiding plate thickness. Also, two-dimensional interconnects could be arranged (Fig.3, below), in the sense that single lines (or groups of lines) or rows can be connected with the help of a single element. Full flexibility can be attained with the design of Fig.2.3.1 at the cost of weight and space for the optical elements.

The same optical system may be used in case of board-to-board interconnects (see Fig.4). Here also the area above the board plugs can be used to make arbitrary board-to- board interconnects, but the positioning accuracy for the loci of the laser transmitters becomes a major difficulty. To achieve the desired operation the interconnecting HOE inputs must coincide with all of the single laser diode positions. The mechanical lateral and axial tolerances of such a setup are dealt with in chap. 5.

The simple interconnect pattern discussed above can be expanded, e.g., by inclusion of fanout elements in form of phase relief gratings (Fig.5). The fanout signals are redirected by an additional HOE-array. In this way an achromatic clock distribution system can be included in a general bus system.

The tolerance stability of the 90^0-deflection can be improved by using pentaprisms (Fig.6). Such a device is invariant against tilt, but, responds strongly to lateral shifts. A shift of the device by s gives rise to a ray shift of -2s in the receiving plane. This enables the adjustment of small production tolerances of the HOEs.

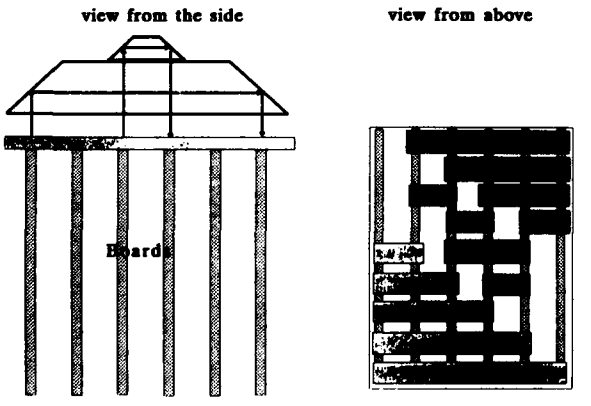


Fig.4 Board to board interconnect system. The device is similar to that of Fig.3, except that the light path length is larger due to the greater distances to be covered.

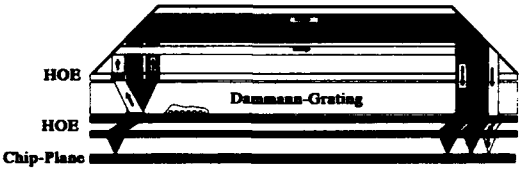


Fig.5 Clock distribution incorporated into chip to chip interconnect. For this purpose a Dammann grating is used as fanout element.

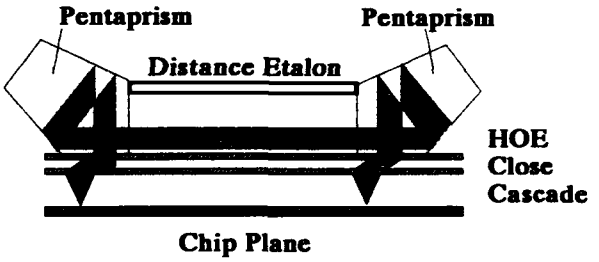


Fig.6 Pentaprisms used as reflecting devices.

3. PACKING DENSITY AND SCALING LAWS

All free space interconnect schemes more or less exploit the dimension perpendicular to the chip surface to install the 3-dimensional interconnects.

Because of the similarity between interconnect structures for switching networks and for chip-to-chip interconnects, the following discussion assumes the geometry represented in Fig.7. For our estimates a few simplifications of the interconnection geometry will be useful. Throughout our discussion full symmetry between the transmitting and receiving ends of the interconnecting stage is assumed. The HOEs are assumed thin (compared with the interconnection length) and planar. The length of the arrays is a. Since the greatest distance to be bridged in the array is on the order of a, it is adequate to make the distance between the arrays also a. In this way the inclination angle for permutations is smaller than 45 degrees and for a shuffle permutation typically < 25 degrees. The subapertures of the single HOEs are quadratic in size to guarantee a high

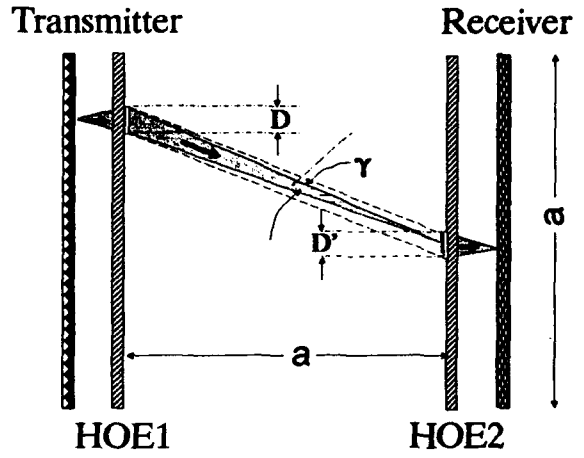


Fig.7 Scheme for the estimation of the diffraction effects of the light passing from the transmitting side to the receiving side of one stage of a switching network.

fill factor. Due to the focusing properties of the first HOE, the intensity distribution in the second HOE-plane can be calculated using Fraunhofer approximations. The intensity distribution has a $\mathrm{sinc}^2 x$-character provided constant illumination is assumed in the first HOE-plane. If a sub-HOE in the first HOE-plane has an edge length of D, then the spread D' in the second HOE-plane is:

$$D' = 2a\lambda/D,$$

where D' is assumed to be the distance between the first positive and negative minima of the diffraction spot. More than 80% of the light (encircled energy) is saved in this way (Fig.10.). Since symmetry D=D' is assumed, the extension of 1 pixel in the HOE-plane is:

$$D = \sqrt{2a\lambda}. \qquad (1)$$

a/mm	D/μm	N	$\sqrt{N}$
1	41	590	24
2	59	1150	34
5	93	2890	54
10	130	5917	97
50	292	29320	171

Table 1 Scaling of a space-variant interconnect stage with varying distances a between the transmitting and receiving end of the stage. The lateral dimension of the transmitter/receiver plane are assumed equal to the distance a.

Since the number of channels in one dimension is given by $\sqrt{N} = a/D$, the number of channels which can be packed into one plane is:

$$N = a/2\lambda. \qquad (2)$$

For $\lambda = 0.85$ μm and varying dimensions a (distance between transmitting and receiving end of the stage, being assumed equal to the lateral dimensions of transmitter/receiver plane), Table 1 lists the necessary pixel sizes, and numbers of possible interconnects.

4. CROSSTALK

For a worst case estimate of crosstalk a matrix array of transmitters and detectors is assumed. The elementary cell of such a periodic structure is assumed to have an area F_{EC} and the detector an area of F_{PD}. The area of the entire array is F_{AR}. The HOEs have a diffraction efficiency η. Due to free space propagation between the two planes containing the HOE-arrays and due to vignetting at the rim of the receiving HOE, there is a free space loss characterized by a diffraction masking factor κ. The angle characteristic of the laser is assumed to be well within the aperture of the collimating HOE. The crosstalk will be estimated for the case that the aperture angle is illuminated with constant intensity which is zero outside this angle. For the sake of simplicity the diffraction efficiency of all HOEs are equal and the main part of the stray light is undiffracted light. We consider here a cascade of 4 HOEs, two on the transmitting and two on the receiving side of the stage (Fig.1). The light flux for the signal beam and the stray

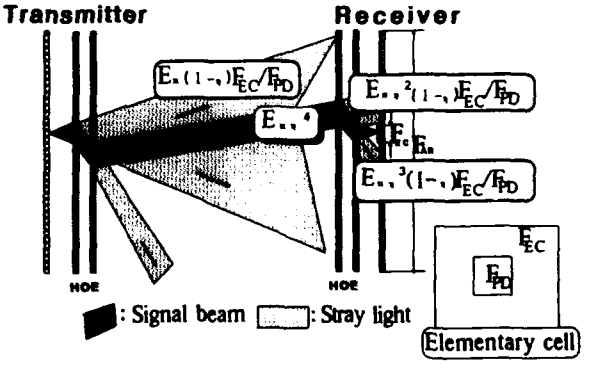


Fig.8 Schematic of one stage using close cascade HOEs for an estimate of crosstalk

between neighboring channels.
η: diffraction efficiency, κ: diffraction loss, F_{EC}: area of the elementary cell of the HOE-array(equal to area of single sub-HOE), F_{PD}: light sensitive area of the detector in the receiving plane.

light are depicted in Fig.8:
detected signal intensity: $\sim E\kappa\eta^4$,
noise term 1: $\sim E(1-\eta)F_{PD}/F_{EC}$,
noise term 3: $\sim E\kappa(1-\eta)\eta^2F_{PD}/F_{EC}$,
noise term 4: $\sim E\kappa(1-\eta)\eta^3F_{PD}/F_{EC}$,
where noise term 1 results from the contributions of all N laser diodes (here all lasers are assumed to be in the on-state) and the noise terms 3 and 4 come from neighbouring pixels (in the Fig.8 ray paths from neighbouring pixels have been omitted to keep the figure clear). For a worst case estimate we consider a pixel in the center of the array. With these terms a signal/noise ratio S/N can be established:

$$S/N=[\kappa\eta^4/((1-\eta)(1+\kappa\eta^2+\kappa\eta^3))]*F_{EC}/F_{PD}. \quad (3)$$

The main gain in S/N is due to the fill factor F_{EC}/F_{PD} of an elementary cell. The light sensitive area F_{PD} should be chosen as small as possible as compared to the area of the elementary cell F_{EC} but of course at least as large as the Airy-disc of the signal beam and, in real situations, should actually be several disc diameters large. For a typical example with F_{EC}/F_{PD} = 100, η = 0.9, κ = 0.8, then S/N = 220 or 23 dB.

The S/N-ratio grows considerably if the packing density decreases, i.e., if the number of necessary interconnects per board area is well below the diffraction limit (Eq.(2)). As a typical example consider 256 (16x16) interconnects per 50x50 mm^2 device area. From packaging density considerations the area of each sub-HOE is 3x3 mm^2 and a fill factor of 10^4 (F_{PD}=30x30μm^2) and therefore a S/N > 40 dB. In the case of chip-to-chip interconnects, from Fig.3, the first term does not contribute to Eq. (3) since the majority of stray light harmlessly leaves the device. Therefore, even when HOEs having medium diffraction efficiencies are used, it is possible to realize a low noise optical interconnect.

To avoid speckle maintaining the mutual incoherence of the single lasers is of utmost importance /23/. Otherwise "hot spots" in the speckle pattern can degrade the situation considerably. In any event, a crosscoupling of the lasers must be avoided to guarantee the independence of the individual channels.

5. CHROMATIC TOLERANCES

As mentioned above, the chromatic aberrations of HOEs restrict their usefulness to some extent. For our discussion we assume the laser diode to operate in a single mode both axially and transversally. Nevertheless, the laser frequency is a function of both temperature and laser current. The temperature of the device depends on the number of switching events that occur within the network per time interval. There exist proposals to switch pairs of laser diodes wherein each pair transmits the signal and the negation of the signal or, similarly, to use codes with alternating on/off states. In this way one diode is always in the on-state delivering a constant temperature for the pair as a whole. This alleviates the situation to some extent but is paid for with factor 2 in channel capacity. An alternative solution - the Manchester Code - uses the transitions between low and high signals to define the message. A better solution is to use an achromatic HOE array and very low threshold currents for the laser diode.

However, if the purpose of the HOE is to deflect or to focus light no achromatic HOE is possible. A combination of two HOEs can reduce the chromatic aberrations if the carrier frequency of the HOE is high as in the case of volume or DCG-HOEs. The close cascade/18,19/, therefore, considerably increases the flexibilty of the HOE-concept.

For an estimate of the effects of wavelength drifts or variations across an array once again the system of Fig.1 is used. The most obvious effect of a wavelength change is a change in the direction of the diffracted beam. For volume HOEs a second more notorious effect is that the diffraction efficiency requires the fulfillment of the Bragg condition. Thus, a change in λ leads to reductions in the diffracted intensity and, with increasing λ, to increased crosstalk.

Variations in the direction of the diffracted beam lead mainly to a decrease in the signal intensity and a corresponding increase in stray light. The distance between the transmitting and the receiving HOEs is responsible for this. This distance can be large in the case of chip-to- chip interconnects or must be great enough to allow for permutations in the geometric order of different beams as is necessary in switching networks.

In a first approach it is possible to neglect the Bragg-effect, since the wavelength tolerance is mainly determined by the geometrical mismatch. Therefore, the wavelength tolerance for the laser can be

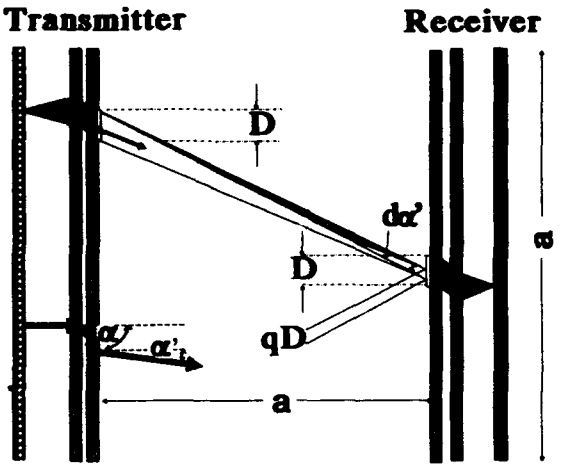


Fig.9 Scheme for the estimation of the wavelength tolerance of the HOE-fabric. α: diffraction angle of focusing HOE, α': resulting deflection angle due to the necessities of the permutation network, dα': mismatch angle due to wavelength shift of the transmitter, q: mismatch factor .

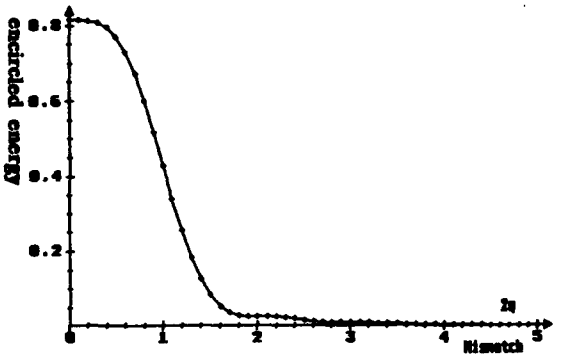


Fig.10 Encircled energy of a stage using close cascade HOEs in dependence on the mismatch due to a wavelength shift.

estimated with the help of the grating equation. For our discussion the geometry given in Fig. 9 is used. The primary ray from the laser is incident upon the collimating HOE, is diffracted in the direction α, where, for the first diffraction order the following holds:

$$d \sin \alpha = \lambda$$
$$d' (\sin \alpha + \sin \alpha') = \lambda,$$

with d and d' being the grating constants of the cascaded HOEs and

$$\sin \alpha' = \lambda(1/d' - 1/d).$$

The first derivative $\partial\alpha'/\partial\lambda$ is then:

$$\lambda \, \partial\alpha'/\partial\lambda = \tan \alpha'$$

or

$$\partial\lambda/\lambda = \partial\alpha'/\tan \alpha'. \qquad (4)$$

For a given $\partial\alpha'$ and α' the allowable $\partial\lambda$ can be estimated. $\partial\alpha'$ is determined by the allowable shift of the center of gravity of the deflected light beam in the plane of the receiving HOE. Allowable in this sense means that a shift of the central ray gives rise to a loss in efficiency and an increase in the stray light within the setup. If the distance between consecutive arrays is a and a 20% shift of the main ray against the aperture of the single HOE is acceptable (meaning a loss of 2% of the encircled energy by the subaperture of a HOE, see Fig. 10) $\partial\alpha'$ becomes:

$$\partial\alpha' \le q \, D/a = q \sqrt{2\lambda a} \qquad (5)$$

or, using Equ.(2):

$$\partial\alpha' \le q/\sqrt{N}.$$

With this value and a α' of about 25 degree, which is typical for the perfect shuffle permutation, we arrive at:

$$\partial\lambda = \lambda \, q/\tan \alpha' \sqrt{N}. \qquad (6)$$

Equation (6) holds only for diffraction-limited design.
Consider for example: λ = 0.85 μm, α' = 25 deg., q = 0.2, N = 1024, which yields $\partial\lambda$ = 11nm.

This estimate is however only valid for phase relief gratings. Further reductions in the transmitted energy are due to the Bragg-effect. Using Kogelnik's estimate a variation of about λ=11nm leads to reductions in the diffraction efficiency of only 1-2% (see ref. /13/).

As will be shown in the next chapter these values have to be further modified. The strict coupling between the values of a and N for diffraction limited design must be given up in favour of a more realistic design in face of mechanical tolerances to be met. This will also reduce even further the allowed wavelength variation for coarse arrays.

To illustrate this tolerance reduction in more detail the case of a rather coarse

array (16x16) covering an area of 50x50 mm^2 is now considered. The photosensitive area of the detector is assumed again to be 30x30 μm^2, the F-number, F♯, of the focusing HOE is 1, and q=0.2. A wavelength drift of $d\lambda$ causes an angle deviation $d\alpha'$:

$$d\alpha' = qD/a.$$

This angular deviation causes a lateral displacement of the focus:

$$\xi = (qD^2/a)F\sharp.$$

Given the above values $\xi = 36\mu m$, which is too large to be tolerated. Although a diffraction limited design for 16x16 channels allows for a $d\lambda = 22nm$ at 850nm, such a coarse array is by a factor 2 more sensitive to wavelength drifts than a diffraction limited array for 256 channels. The wavelength induced lateral shift makes mandatory a low F-number design for the focusing elements.

6. SENSITIVITY TO MISALIGNEMENT

In the following it is assumed that the HOE-arrays are ideal, i.e. free from pitch errors. The close cascade is composed of a collimating array of identical HOE-lenses and a deflector array for nearly plane waves, each deflected into different directions. The whole interconnect fabric uses two close cascades for symmetry reasons. These arrays must be mutually adjusted in such a way that the light from the laser diode arrives in full strength at the detecting diode. Each array of elements has 6 degrees of freedom in space. If the relative distances are fixed by mechanical distance etalons, then there exists only 3 degrees of freedom for each close cascade, two lateral translations and one rotation about the array normal.

An estimate for the lateral adjustment tolerance is now given. If the laser diode is shifted laterally by ξ from its ideal position, the aperture angle is u, and the HOE-diameter, D, then the following geometric relation holds (see Fig.11):

$$\zeta = qD^2/(2a \tan u). \qquad (7)$$

For example, if q = 0.2, D = 1.5mm, a = 50mm, u = 20^0, then ξ = 12.4 μm, which corresponds to N = 1024 interconnects. For the diffraction limited packaging density the tolerances become extremely small:

$$\zeta = q\lambda/\tan u, \qquad (8)$$

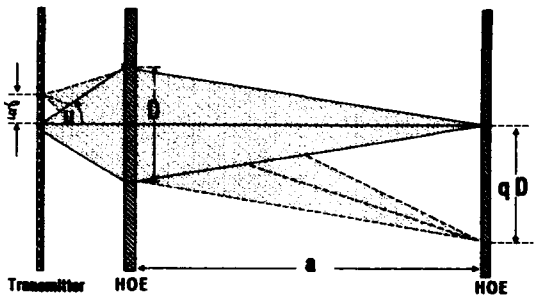


Fig.11 Scheme for the calculation of lateral misalignement tolerances.

For example, if q = ±0.2, D = 1.5mm, a = 50 mm, u = 20^0, then ζ = 12.4μm, which corresponds to N = 1024 interconnects. For the diffraction limited packaging density the tolerances become extremely small:
i.e. for q = 0.2, u = 26^0 (corresponds with F♯ = 1), $\zeta = 0.4\lambda$.

The distance etalons should, under optimum conditions, guarantee the focus length due to the Rayleigh limit to an accuracy ζ/24/:

$$\zeta = \lambda/2(\sin^2 u), \qquad (9)$$

which, using above values, yields $\zeta = \pm 2.6\lambda$. A more relaxed condition would tolerate a defocussing by:

$$\zeta = p/(4\tan u),$$

with p being the cross section of the photodiode. This gives a defocus value $\zeta = p/2$ for F♯ = 1.

The most critical interface area is, therefore, the focus region between the laser and first HOE and between the last HOE and the photodetector plane. The interfacing of plane waves is not so critical if the variation of the deflection angles of the different plane waves is kept below 30^0. With the above given value q = 0.2 the lateral and axial tolerances are on the order of a few 100 μm.

7. PACKAGING

In this section possibilities are discussed for adjustment support systems that could help with the design and construction of such cascaded networks (see e.g. /25/). In a cascaded setup, distances between different optical elements (here HOE-arrays), the directions of light beams which are coupled to the HOE-arrays, and the directional spectrum originated by the previous stage can be fixed beforehand.

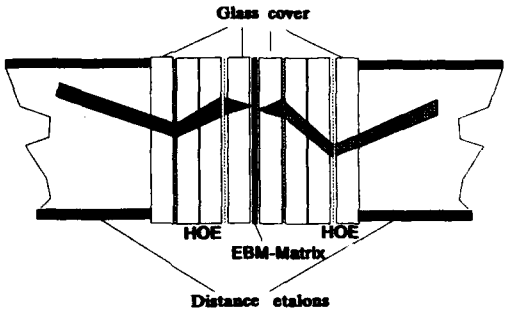


Fig.12 Proposal for the packaging of an on-line switching pipeline for switching applications.

Distances such as focus distances or distances between the different stages can be fixed by distance etalons (Fig.12). Lateral positions on the HOE-arrays can be measured by means of integrated fiducials and, after adjustment, the position can be fixed using cement. For high numerical aperture systems, the accuracy of the etalon length must be greater than usual because of the reduced depth of focus.

The directions frozen into the HOE-array have also fairly small tolerances which must be satisfied during the recording of the HOE. These tolerances are typically on the order of a few minutes of arc. For bus interconnects other optical elements, mirrors or right angle prisms, also must be included in the design, which introduces additional degrees of freedom which must be taken accounted for.

SUMMARY

Table 2 is a summary of the typical tolerances discussed in this work. The tolerances are given for a switching network stage upon which the discussion has been based. Three examples have been considered. The same dimensional parameters have been used throughout so that for a 50mm cube we initially assume a rather coarse design and end up with the diffraction limited design. Of course the figures derived are valid only in the context presented but as a general rule it can be followed that the number of possible space-variant interconnects scales only linearly with the dimension of the stage and inverse linearly with the wavelength used. The adjustment and production problems increase considerably if one approaches the diffraction limit. In the latter case accuracies must be obeyed typical for VLSI manufacture. Furthermore, the size of the stage should keep within the limits that optics can handle easily.

Summary for free-space space-variant HOE-interconnects

$a = 50\,mm$, $\lambda = 850\,nm$, $p = 30\,\mu m$

Number of Interconnects		Comparable Technology
N = 256 (16x16) (coarse array)	D = 3 mm $d\lambda$ = 11nm ξ = 20 μm ζ = 15 μm S/N = 43 dB	Precision Mechanics
N = 1024 (32x32)	D = 1.5 mm $d\lambda$ = 11 nm ξ = 9 μm ζ = 15 μm S/N = 37 dB	Precision Optics
N = 30000 (172x172) (diffraction limited)	D = 0.3 mm $d\lambda$ = 2.1 nm ξ = 0.4 μm ζ = 2.2 μm S/N = 23dB	Photolithography

Table 2 Summary of the tolerances for a single interconnect stage with a distance of 50 mm between the transmitting and the receiving planes.

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Multiplexed Tunable Resonated Holograms for Reconfigurable Optical Interconnects

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Abstract

Enhanced diffraction efficiency of a grating placed inside an optical resonator is reviewed. This concept, implemented with multiplexed holograms inside a tunable resonator, can be used for reconfigurable optical interconnects. Experimental results on resonated holograms and tunable resonators are also presented.

Introduction

The benefits of using optics for interconnects between electronic processors lie mainly in the fact that optics offers highly parallel operation, low crosstalk, and high bandwidth. If optical switches are incorporated in the system to permit reconfiguration of the interconnect network, greater system flexibility can be achieved.

The enhanced efficiency of holograms placed in optical resonators has been proposed for the use in passive interconnects [1-3], for active devices [4], and for dense wavelength division multiplexing [5]. If a diffraction grating is placed inside a resonator, such as a Fabry-Perot resonator, its interaction length, and consequently its efficiency, can be significantly increased because of multiple paths of the optical beam inside a cavity in resonance. As a result, a combination of the characteristics of diffraction gratings and optical resonators is achieved: 1) the direction of light can be changed and 2) the efficiency of the diffracted beam exhibits peaks similar to that of a Fabry-Perot resonator and can be enhanced, if the cavity is in resonance. If the cavity can be tuned, the features of resonated holograms can be utilized for switching of light beams in optical interconnects, because the diffracted beam can be turned on or off. Multiplexed holograms, recorded in a volume holographic material, placed in a resonator will permit reconfiguration of one-to-many interconnects: as the cavity is tuned, different sets of holograms are selected.

We also present our experimental results on efficiency enhancement of resonated holograms and on tunable resonators. Fabry-Perot resonators are fabricated using two reflection Lippmann holograms instead of typical multilayer dielectric coatings or metallic mirrors. Simultaneous recording of two high efficiency reflection gratings removes mirror alignment problems. In addition, slanted reflection gratings can be used for the mirrors which permits the resonance direction to be designed at any arbitrary angle.

Resonated Holograms

The simplest case of a resonated hologram is a diffraction grating, of either reflection or transmission type, placed inside a Fabry-Perot resonator. In resonance, the peak diffraction efficiency is a function of the initial hologram efficiency and the characteristics of the cavity: mirror reflectance and cavity losses. Derivation of the effective efficiency of resonated holograms can be found in Ref. 2. The effective efficiency of a hologram inside a Fabry-Perot resonator in resonance is:

$$Y = \frac{H(1-R)a_1}{[1-R(1-H)a_{12}]^2} \qquad (1)$$

where H is the initial hologram efficiency, R is the mirror reflectance, and a_1 and a_{12} are absorption coefficients for one pass and round trip pass in the cavity, respectively. For example, if the initial diffraction efficiency is 1% the effective efficiency in a Fabry-Perot cavity increases to 25% in a lossless cavity with mirror reflectances 99%. In the more general case of a four mirror resonator the effective efficiency may increase up to 100% if the structure is lossless. If the cavity is out of resonance, the effective efficiency is suppressed. Figures 1 and 2 show the peak efficiency of resonated holograms in a single and a double Fabry-

Perot cavity for the more realistic case where 1% round trip cavity loss was assumed, i.e. $a_{12} = 0.99$ and $a_1 = 0.995$ in Eq. (1). These curves illustrate how the efficiency of the grating and mirror reflectances can be optimized to achieve the strongest efficiency enhancement effect. It should be noted that the efficiency enhancement occurs only for low initial hologram efficiency. Interestingly, the effective efficiency characteristics of a Fabry-Perot resonated hologram are the same whether the resonator is placed in the direction of the incident beam, as shown in Fig. 1, or in the direction of the diffracted beam. This feature can be helpful in designing structures with multiplexed holograms.

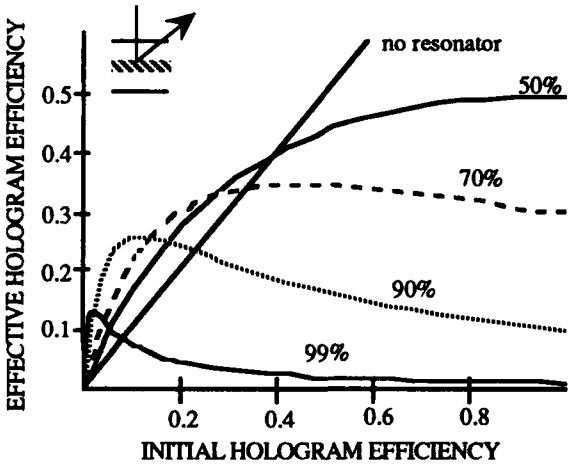


Figure 1. Effective diffraction efficiency of a grating placed inside a Fabry-Perot resonator for different values of mirror reflectance and for 1% round trip absorption loss in the cavity.

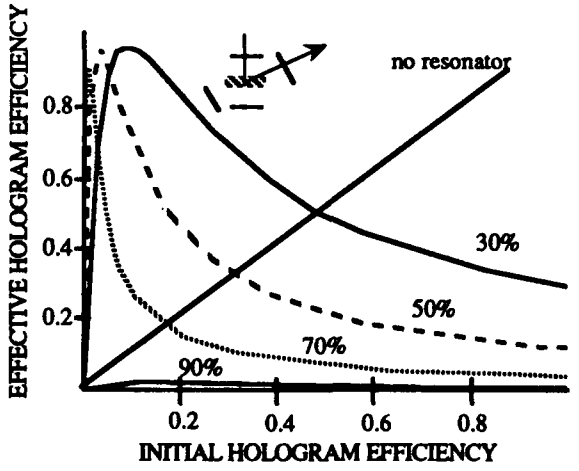


Figure 2. Effective diffraction efficiency of a grating placed inside a four mirror resonator for different values of mirror reflectance and for 1% round trip absorption loss in the cavity.

Reconfigurable Interconnects

The resonated hologram structures can be used for switching, if a tuning mechanism is introduced in the structure, as shown in Fig. 3. Tuning can be achieved by modulation of the refractive index inside the cavity using electrooptic substrates, e.g. PLZT, liquid crystal, or by mechanical modulation of the cavity length. A single diffraction order of the resonated hologram can be switched on or off using a tunable Fabry-Perot resonator or a four mirror resonator (see Figs. 3a and 3b). The contrast ratio of the switch is strictly dependent on the contrast of the resonant cavity, i.e. the ratio of the maximum to the minimum transmitted intensity. This contrast, for a lossless cavity is:

$$C = \frac{T_{max}}{T_{min}} = \left(\frac{1+R}{1-R}\right)^2 \qquad (2)$$

Thus, with mirror reflectances ~ 95%, 30dB contrast of the diffracted beam can be achieved. Because the slope of typical Fabry-Perot resonators is steep, high contrast modulation of the diffraction efficiency can be achieved with small driving signals.

Figure 4 shows a possible interconnect configuration where the resonated hologram is a multiplexed volume hologram. The input beam is incident on the structure at an angle θ, not within the range of the resonant cavity. The hologram placed inside the resonator diffracts the beam into the resonator. In one resonance condition, a set of multiplexed holograms is enhanced to provide an interconnect pattern. The diffraction

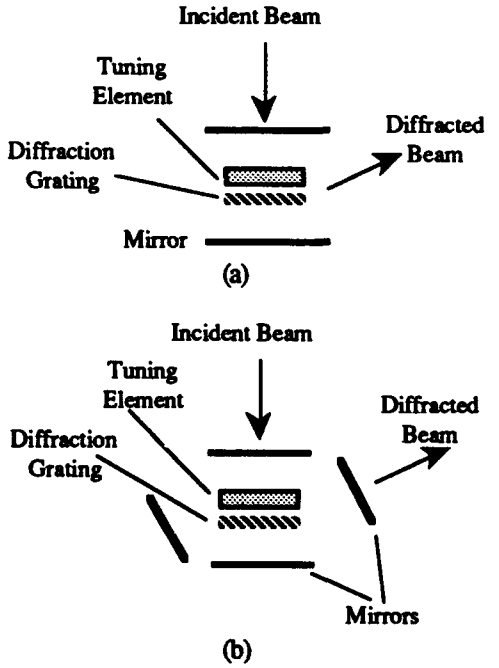


Figure 3. (a) Fabry-Perot resonated grating (b) Four mirror resonated grating.

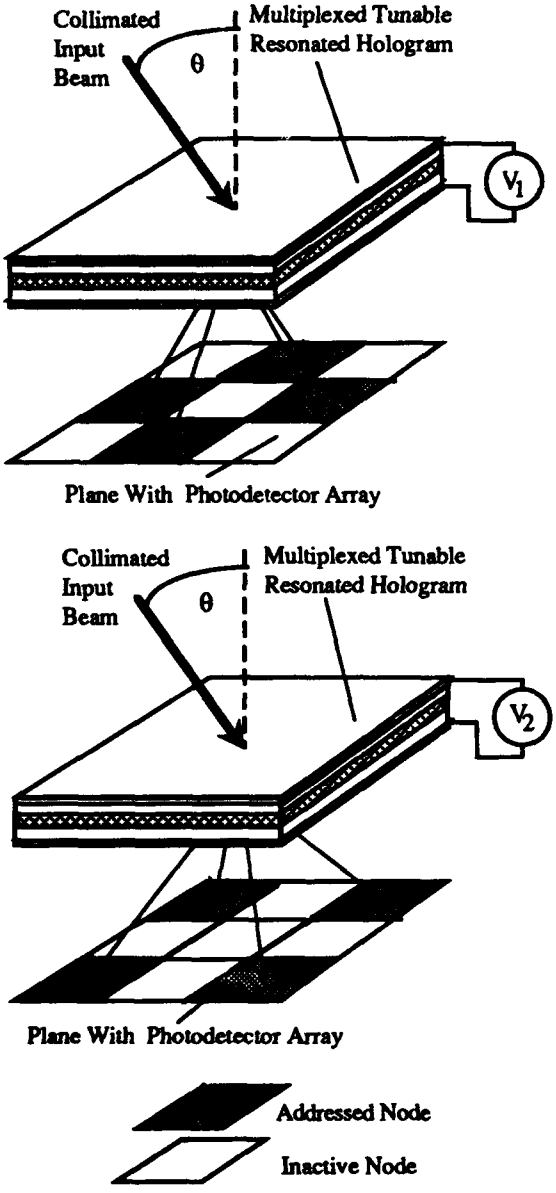


Figure 4. Reconfigurable optical interconnect using a multipled resonated hologram in a tunable cavity.

angles are designed to match the angles at which resonances occur. If the cavity is tuned to a different resonance condition, by less than the free spectral range of the Fabry-Perot resonator, another set of multiplexed holograms is enhanced, and a different interconnect pattern is formed. These interconnect patterns are prerecorded in the multiplexed hologram. The diffracted beams of one multiplexed hologram may range over several free spectral ranges of the resonator. In order to maximize the angular range of the interconnect the cavity length has to be kept small. With a 100 μm cavity length the useful angular range (about 4 free spectral ranges) is ±7°. Because the number of channels that can be incorporated in the interconnect is proportional to the resonator finesse (ratio of resonance

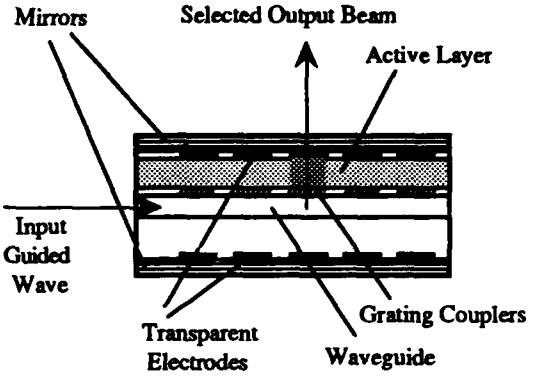


Figure 5. Array of tunable resonated waveguide grating couplers.

peak separation to the peak width), high finesse is desired in this case. The finesse of a lossless resonator depends only on mirror reflectance:

$$F = \frac{\pi\sqrt{R}}{1-R} \qquad (3)$$

To achieve crosstalk levels less than -20dB the interconnect channel separation should be at least five times larger than the resonance peak width. Thus in a resonator with mirror reflectances 95% about 12 independent channels can be supported.

Yet another interconnect configuration uses an array of gratings and tunable resonators (see Fig. 5). The efficiency of the gratings may be independently enhanced if the corresponding resonator is tuned to resonance. This structure is particularly suited for the use with waveguides and grating couplers and could be used for back plane interconnects. The ends of the waveguide can be polished and coated with high reflection coatings to form an integrated optics verion of a 3 mirror or 4 mirror resonated hologram.

Experimental Results

Holographic Resonators

Fabrication and alignment difficulties of resonator mirrors can be alleviated if holographic reflection gratings are used [6]. In this process, two reflection holograms are recorded simultaneously in holographic material thin film coatings deposited on both sides of a substrate. As a result, two self-aligned mirrors are obtained. After processing of the holographic material a good quality fringe pattern can be observed under illumination with a diverging beam, even if ordinary glass substrates are used.

We used dichromated gelatin (DCG) holographic material of thickness 15 μm, spin coated on glass substrates. Lippmann holograms were recorded using collimated argon laser beams and were designed for reconstruction with 633 nm He-Ne laser beams. The spectral half-width of the reflection gratings was

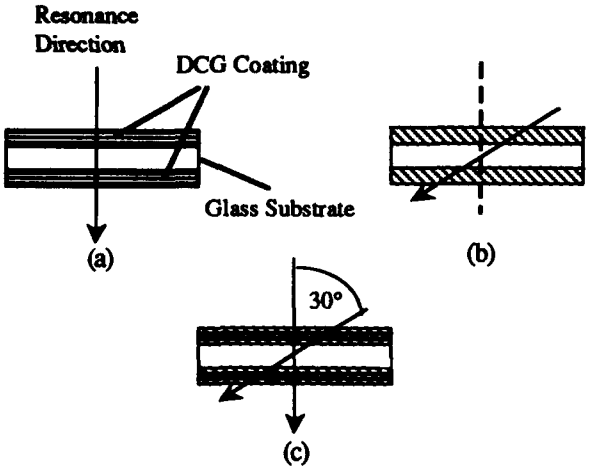


Figure 6. Holographic Fabry-Perot resonators: (a) with Lippmann gratings, (b) with slanted gratings, (c) and with multiplexed gratings.

~ 40 nm. At the peak wavelength, the reflectance was typically 95%. With these resonators we obtained a finesse of 20 using glass substrates coated with the holographic material on both sides, as shown in Fig. 6a. Maximum contrast of 52 was obtained. The reduced finesse in comparison with the theoretical value for the given reflectance was attributed to the absorption losses in the cavity. A variety of free spectral ranges was achieved using glass substrates of thickness between 140 μm and 2.5 mm.

Using the holographic method we have recorded slanted gratings and achieved resonances at angles perpendicular to the Bragg planes, as shown in Fig. 6b. Optimization of the recording and processing parameters in the case of slanted resonators was more difficult than in the case of normal resonators because of the DCG film properties. Due to nonuniform film swelling during processing the peak wavelength shifts, as well as the Bragg planes become distorted. However, we have obtained finesse and contrast values similar to the normal resonators. We have also fabricated multiplexed Fabry-Perot resonators which can be utilized for the four mirror resonated gratings, as shown in Fig. 6c. One set of gratings had Lippmann hologram Bragg planes for reconstruction with light incident normal to the plate. The other set of gratings was slanted. To ensure independent operation of the two sets of gratings the angle between their wavevectors had to be greater than 15°. The diffraction efficiency of the multiplexed resonators was decreased to less than 50% because of saturation of the holographic material. The multiplexed resonators can be improved if the recording and processing are optimized.

Tunable Resonators

Tunable holographic Fabry-Perot resonators were recorded on liquid crystal cells with nematic liquid crystal of thickness 6 μm (see Fig. 7a) and glass

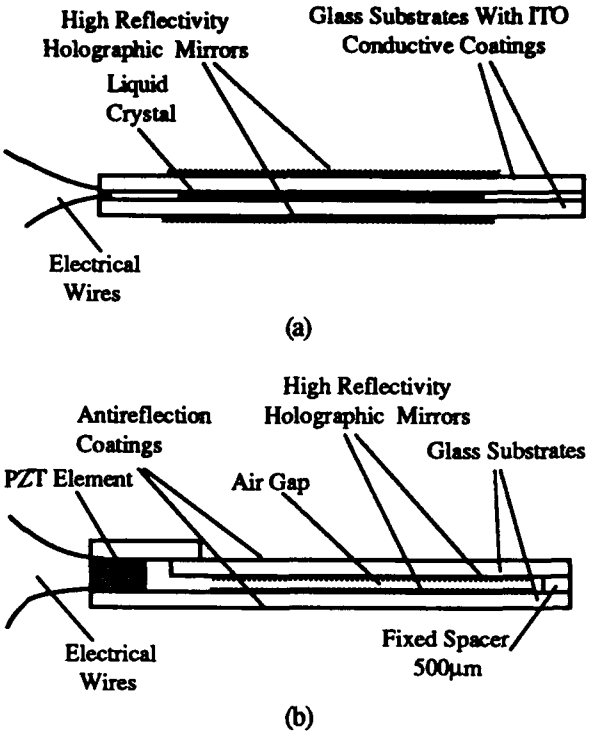


Figure 7. Tunable holographic Fabry-Perot resonators: (a) using a liquid crystal cell (b) using a piezoelectric transducer.

thichness 500 μm. Tuning over one full free spectral range was achieved by changing the bias voltage by ~1V to change the refractive index seen by the incident polarized beam. The finesse of the liquid crystal tunable resonator was ~5 owing to some scattering caused by glass spacers inside the cell, absorption losses, and index mismatch between the liquid crystal and the glass substrates.

Piezoelectric transducers (PZT) were used as another tuning mechanism (see Fig. 7b). In this case two glass plates with holographic material coatings were attached permanently to a PZT, and the reflection gratings were recorded. The separation between the mirrors could be set by selecting the thickness of the spacers. Typical spacing of 500 μm was used. However smaller spacings could be potentially obtained using glass microrods, as is done in fabrication of liquid crystal cells. The resonator was tuned by applying voltage to the PZT which moved the two plates apart, and effectively changed the round trip phase shift between the mirrors. Because only an air gap was used between the mirrors, and the substrates were coated with anti-reflection layers, the finesse was higher than in the case of the liquid crystal resonator, up to ~10, and the maximum fringe contrast was 37. The voltage used to tune the resonator by one full free spectral range depended on the type of PZT and the size of the plates, and ranged between 30V and 400V.

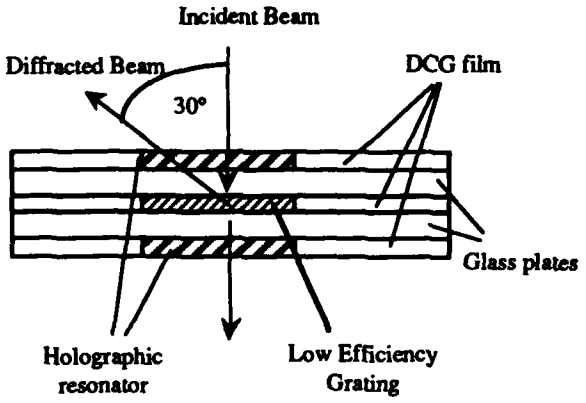


Figure 8. Resonated hologram structure.

Passive Resonated Holograms

We have performed preliminary experiments with holographic resonators used to enhance the efficiency of weak diffraction gratings. A slanted holographic grating with 2% efficiency, designed for deflecting an incident normal beam at a 30° angle, was protected with a glass cover slide and used as substrate to fabricate a slanted holographic Fabry-Perot resonator, as shown in Fig. 8. With the resonator, efficiency enhancement by a factor of 8 was observed. Because this resonated hologram was fabricated on a passive glass substrate, it was tested by observing the angular characteristics using a diverging beam focused on the plate.

Conclusions

We proposed the use of tunable multiplexed resonated *holograms for reconfigurable interconnects*. We demonstrated an enhancement of diffraction efficiency by a factor of 8 when a grating was placed inside a Fabry-Perot resonator. This demonstrator was fabricated using holographic techniques. Because the structure is based on a resonance effect, potentially high contrast modulation can be obtained if teh cavity length is tuned. We presented a simple method of fabricating tunable Fabry-Perot resonators in which simultaneously recorded holographic reflection gratings are used to replace traditional metallic or dielectric mirrors. Holographic resonators can be fabricated on any transparent substrate, they do not require any alignment, and they can be multiplexed to form extremely compact multiple mirror self-aligned resonators. We demonstrated tunable resonators fabricated with the holographic technique. Tunable resonators can be used to enhance and modulate the diffraction efficiency of gratings placed inside the resonators. The potential applications of this technology are for optical interconnects, optical modulators and switches, beam scanning, and efficient coupling into waveguides.

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Lightwave Interconnections Using Spatial Addressing

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Abstract

A novel architecture for free-space optical interconnections in 1×N switching is proposed. A 1×16 switch that uses the architecture is implemented and demonstrated at 200 Mb/s.

1. Introduction

The metallic interconnections needed to link processors and memories in advanced parallel processing systems cause wiring congestion and suffer from undesired electromagnetic effects. The performance of multi-processor systems for real time processing is currently handicapped by the unsatisfied need for high interconnection speed and large fan-out. Free-space optical interconnections appear to be the best way of overcoming these problems[1]. To more fully use spatial parallelism, which is one of the inherent characteristics of free-space optics, many array devices such as laser diode, micro lens, and detector arrays, are being actively researched[2],[3]. Many free-space switching networks using spatial light modulators have been proposed[4],[5]. However, these modulators limit the network switching speed to the microsecond order. Moreover, driving the modulators requires particular control circuits and interconnections.

To settle the dilemma associated with free-space optical switching, we propose a novel free-space optical interconnection architecture named LISA (Lightwave Interconnections employing Spatial Addressing). LISA combines optical array devices with simple electrical logic circuits to form 1×N switches. Large fan-out and high-speed switching characteristics can be obtained because LISA utilizes free-space optics for interconnections while integrated electrical circuits perform the switching operations. First, this paper presents LISA's addressing principle and structure, then it describes the implementation of a 1×16 LISA that achieves 200 Mb/s data switching operation.

2. Principle and Structure of LISA

LISA comprises an input processing, free-space optical interconnection, and N output processing sections. Data and address signals are simultaneously transmitted from the input processing section to the N output processing sections through the free-space optical interconnection section. Each output processing section has a unique address which takes the form of a binary pattern. Transmitted data can only pass through the output processing section whose address agrees with the transmitted address. One feature of LISA is its ability to apply the space parallelism of free-space optics to addressing.

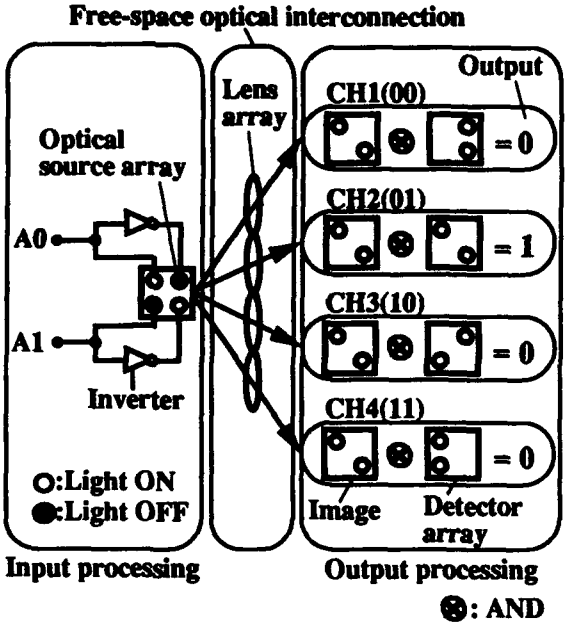


Figure 1. Principle of spatial addressing.

Fig.1 shows the principle of spatial addressing in LISA. In Fig.1, a 2×2 optical source array, four lenses and four detector arrays perform 1×4 addressing.

A binary address is input in parallel to the input processing section. The address signal is 2 bits long and each bit is input in parallel through input terminals A0 and A1. Each bit differentially drives two optical sources on the source array, with one optical source being driven with the bit and the other with the inverted bit. In this way, the input address signal is converted into an optical pattern on the optical source array. The optical pattern shown in Fig. 1 corresponds to the address signal (A0, A1)=(0, 1).

The free-space optical interconnection section forms duplicate optical pattern images, the number of which equals the number of lenses. The duplicated images are received by a series of detector arrays. Each detector array contains the same number of detectors as of input address bits, and has a unique pattern of the detectors such that only in the addressed array are all detectors activated by the signal pattern.

The output processing section following each detector array performs AND operations on the outputs of the detectors. Accordingly, only the output processing section whose assigned address agrees with the transmitted address outputs "1", all others output "0". In this way, LISA easily realizes the addressing function by just forming optical patterns on the source array.

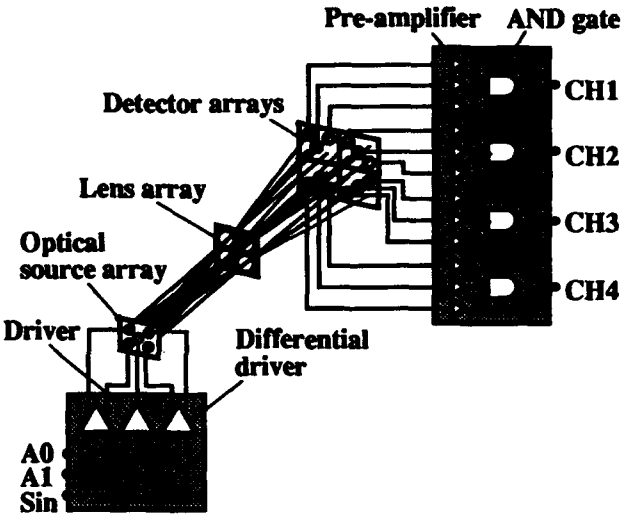


Figure 2. Structure of a 1×4 LISA.

Table 1. Input/output relationships of LISA

Input			Output			
A0	A1	Sin	CH1	CH2	CH3	CH4
0	0	DATA	DATA	0	0	0
0	1	DATA	0	DATA	0	0
1	0	DATA	0	0	DATA	0
1	1	DATA	0	0	0	DATA

Fig.2 shows the structure of a 1×4 LISA applying the addressing method mentioned above. Two address bits (A0, A1) and data (Sin) are connected to the input processing section. The optical source array is composed of 5 sources. Four of them are for addressing and the other one is for data transmission. The lens array has 4 lenses to obtain four images of the optical pattern. Each detector array is composed of 3 detectors; two of them are for addressing and the other is for data detection. At each output processing section, the outputs of these three detectors are amplified and input to an AND gate. The result of the AND operation is output from each output channel. Table 1 lists input/output relationships of the 1×4 LISA shown in Fig. 2. Input data is output only from the output channel which is designated by the input address as shown in Table 1.

Table 2. Specifications of the fabricated 1×16 LISA.

Array devices		Device	Spacing	Array size
	Source	LD (λ=780nm)	12mm	3x3
	Lens	Plano-convex D=15mm, f=80mm	16mm	4x4
	Detector	PIN-PD D=500μm	6mm	3x3
Optical system	L=345mm, lf=230mm, lb=115mm α=0.5			
Processing device	ECL100K			

D:Diameter

LISA can be easily extended to a 1×N switch. LISA's free-space optical interconnections provide large fan-out characteristics. Estimations considering aberration and diffraction of the lens array indicate a possible fan-out of over ten thousand [6]. Also, since the switching operation is carried out locally at the input/output processing sections, high speed integrated electrical circuits can be applied without suffering interconnection problems. LISA is therefore suitable for interconnections from a processor to a large number of memories and for interconnections to distribute real time data to a large number of processors in multi-processor systems. It is also possible to apply LISA to a self-routing switch network because switching is performed only at the input side.

3. Experiment

To confirm the feasibility of LISA, a 1×16 LISA was fabricated. The specifications of the fabricated LISA are summarized in Table 2. A 3×3 laser diode (LD) array (wavelength: 0.78 μm, element spacing: 12 mm) was used as the optical source array. A 4×4 lens array was fabricated by arranging 16 plano-convex lenses (D=15mm, f=80mm) with 16 mm spacing on a glass substrate. Four detector arrays comprising 5 PIN-PDs with unique arrangements were fabricated. The spacing between the LD array and the plane of the detector arrays was set to 34.5 cm. Lateral magnification of the optical system was 0.5.

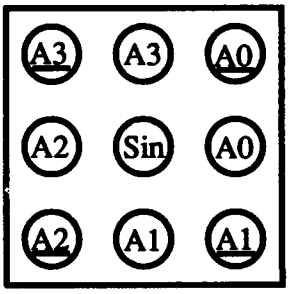


Figure 3. Signal arrangement on the LD array.

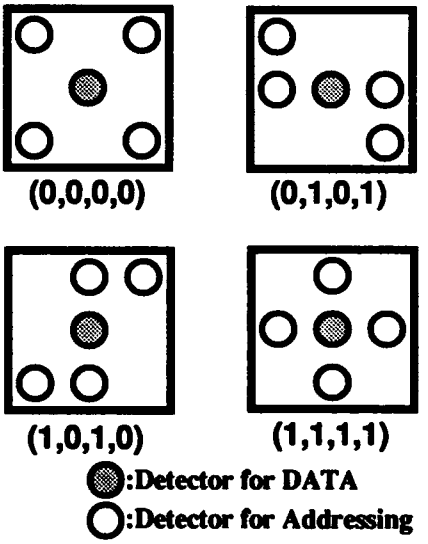


Figure 4. Detector arrangements.

Input/output processing sections were fabricated with ECL 100K series devices.

Input signal arrangement on the fabricated LD array is shown in Fig.3. The center LD is used for data transmission and the other 8 LDs are for addressing. For instance,

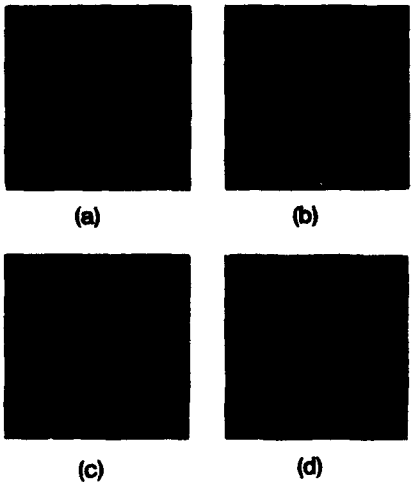


Figure 5. Examples of the optical pattern.

when the address (A3 A2 A1 A0)=(0101) is input to the input processing section, LDs, A3, A2, A1, and A0 in Fig.3, are active. The four fabricated detector arrays have different detector arrangements. Fig.4 shows the detector arrangements. At each detector array, the center detector is for data detection, and the other four detectors are for addressing. The addresses of the fabricated 4 detector arrays are,{ (A3 A2 A1 A0) = (0000), (0101), (1010), (1111) }.

Fig.5 (a)~(d) show examples of the optical patterns formed by the fabricated optical system. Fig.5 (a) shows optical patterns when all LDs on the LD array are driven. This is an example of a broadcast interconnection. Fig.5 (b)~(d) express the optical patterns when the input addresses are (0000), (1111), (1010), respectively. In these three cases, the data signal is transmitted only to the corresponding address channel.

The fabricated 1x16 LISA was first tested to confirm addressing operation. Signals pulsed at 100MHz and 50MHz were input to the input terminals, A2 and A3 respectively. Output address signals from each output processing section were observed. Fig.6 shows the observed input/output address signals. In the figure, the upper two traces are the input address signals, and the other four traces are output address signals from each output channel. The address signal is output only from

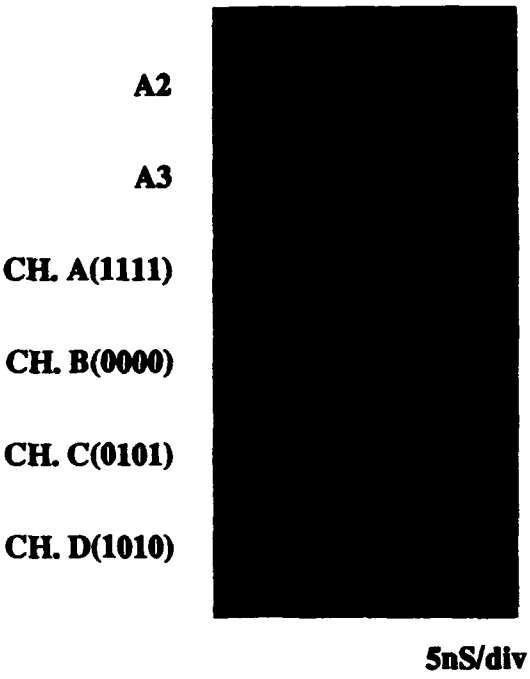


Figure 6. Observred input/output signals.

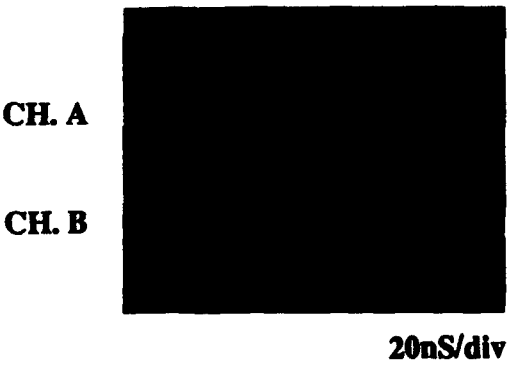


Figure 7. Switching operation for 200Mb/s.

the output channel designated by the input address signals; A2 and A3.

Next, the switching of a 200Mb/s data signal was demonstrated. Fig.7 shows an example of switching operation, where the word pattern "0,1" at 200 Mb/s and repetition pulses at 25 MHz were used as the data and the address signal. The figure indicates that switching operation between two output channels is correctly performed for each data byte.

4. Conclusions

A novel architecture for free-space optical interconnections has been proposed, which is comprised of optical array devices and simple electrical logic circuits. The architecture, named LISA for Lightwave Interconnections employing Spatial Addressing, acts as a 1×N switch. A 1×16 LISA was implemented and switching of 200 Mb/s data was demonstrated.

Acknowledgments

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Linked InGaAs/InP Multiple Quantum-Well Modulator Arrays for Neural Network and Photonic Switching Applications

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Abstract

The fabrication of a 10x1(10) array of line-addressed coupled quantum well modulators, operating at 1.41μm, is described.

Introduction

Square arrays of InGaAs/InP MQW modulators are attractive devices for high speed switching of optical signals, especially where operation in transmission simplifies the system design. For example, simple 4x4 arrays have been used in demonstrations of i) parallel optical interconnect with the modulators driven by standard high speed CMOS to provide a capacity of 100 MBit/s x 16-channels [1] and ii) an opto-electronic implementation of neural network operating at 50MBit/s[2] . The electrical addressing of individual devices in such arrays becomes more dificult as the number of elements increases, with packaging of such large arrays for use in transmissive mode posing further problems. For some applications, as in the neural network demonstrator shown in Fig. 1, individual modulators need not be addressed, and more extensive systems can be built and packaged by linking individual modulators *during the fabrication scheme*, to provide line-addressed arrays. Furthermore, by applying the technique of double-sided epitaxy [3], to the modulator-detector pair, and linking rows of devices in orthogonal directions on the two faces of the substrate material, a considerable miniaturisation of the experimental design may be achieved.

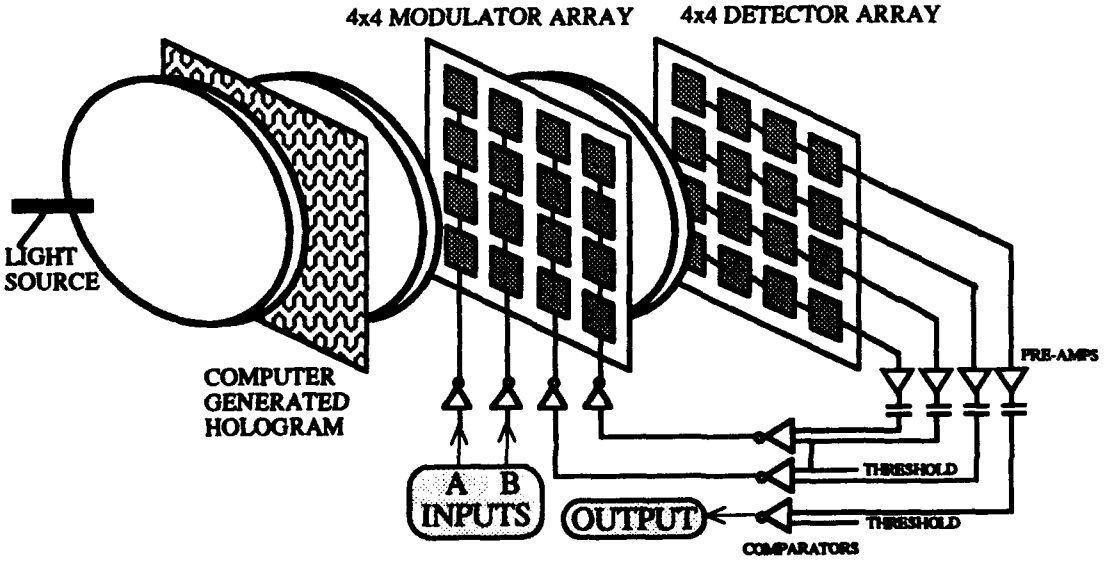


Figure 1. Optoelectronic network to recognise exclusive-or (EXOR) combination in input streams A, B

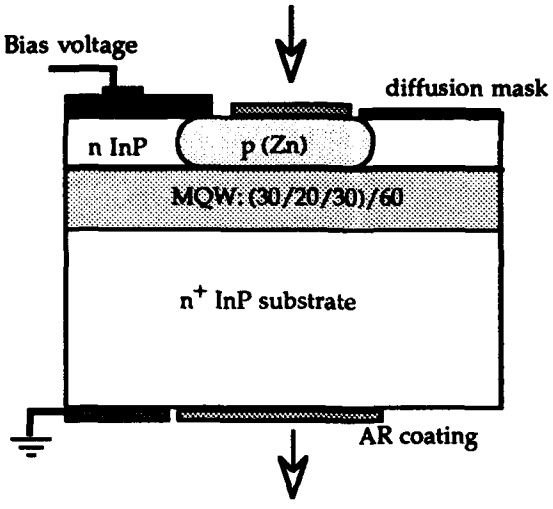


Figure 2. Schematic of planar CQW modulator

Growth and Fabrication

However, even for a single-sided version, a high yield MQW growth and fabrication process is necessary to realise this linked-modulator design. In this report, the use of a coupled-well structure avoids the need for the offset bias (10 or 15V) of a conventional MQW design[1], thereby allowing operation at lower voltages and, therefore, lower dark currents; while a planar processing approach simplifies the two-level metallisation procedure.

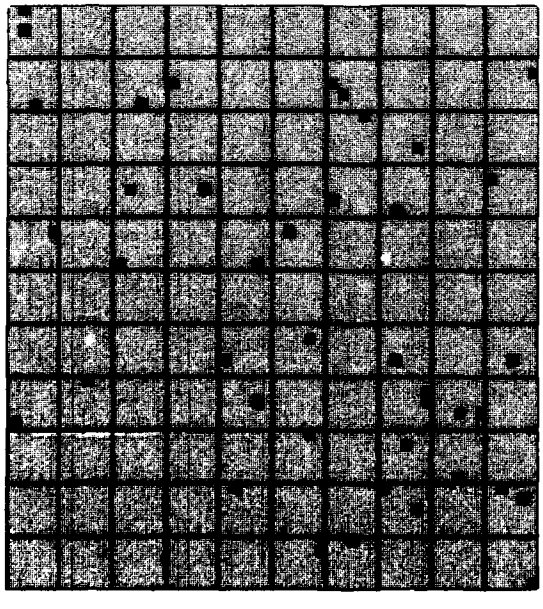


Figure 3 Wafer map of leakage currents of 2750 modulators at -10V ($I_{leakage}$<10nA in light grey)

The layer structure for the planar coupled quantum well device shown in Fig. 2 is grown using gas-source MBE[4] with a symmetrical well of two 30Å InGaAs layers separated by a thin 20Å InP region, and a barrier width of 60Å. A two-dimensional array of 45μm diameter modulators is then fabricated at a repeat distance of 125μm using selective diffusion of zinc through a silicon nitride window. After the deposition of anti-reflection coatings on both sides of the wafer, an initial metallisation pattern is defined to allow for the automatic wafer probing of devices across the slice. Results of the measurement of dark current in the centre of a slice are shown in Fig. 3, with a yield of nearly 99% at a reverse bias of 10V (2750 devices).

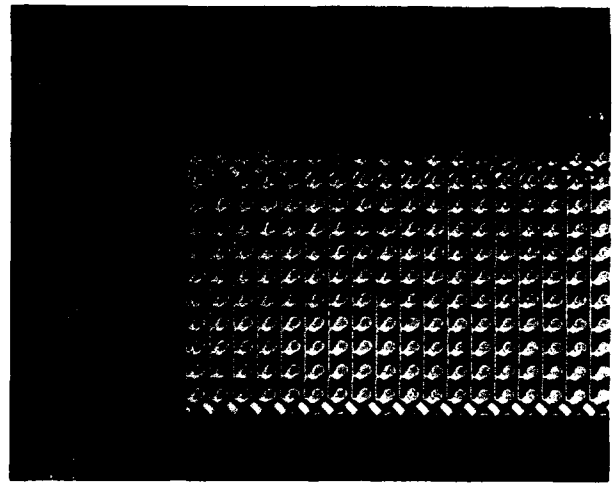


Figure 4. 10x1(10) array of modulators

Assessment and Packaging

Measurements on individual devices in transmission using a micro-FT-IR spectrometer show a modulation of 1.2dB (with a FWHM of 12nm) at a wavelength of 1.41μm and at a reverse bias of 6V - increasing to 1.8dB at 10V. After identification of a 10x10 array of modulators with a 100% yield, a second level of metallisation is deposited using a Ti-Au sputtering method and is patterned by a lift-off technique, connecting lines of 10 devices to a single bondpad. The full array is then bonded onto an 18-pin leadless chip carrier (modified for operation in transmission) as shown in Fig. 4. Dark current measurements made at the completion of the fab-rication process show no increase in leakage (Fig. 5); and the capacitance of individual modulators, typically 0.43pF at an operating voltage of 6V, increases to 10.1pF for a row of 10 modulators with track and common bondpad, to be further increased by 0.5-0.65pF by the lead wires in the packaged array.

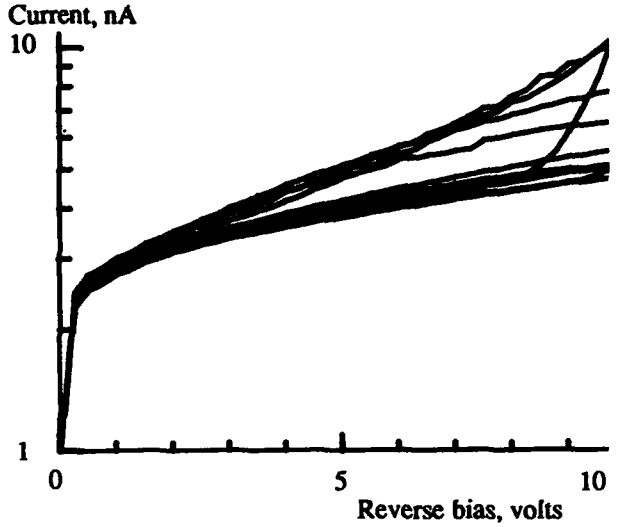


Figure 5. Leakage currents of packaged array of 10 line-addressed modulators

Improvement in Spatial Uniformity

Larger arrays are possible by re-positioning the bondpads, and by improvements in the spatial uniformity of the MQW spectral response. Using gas-source MBE, but with conventional solid sources for the gallium and indium, the position of the exciton peak of a MQW structure is uniform to within 4nm over a circular area 8mm in radius from the centre of a 50mm wafer; by replacing the solid sources with organo-metallic compounds, the area over which a comparable uniformity is achieved is increased fivefold (Fig. 6) Finally, the yield of individual modulators is determined predominantly by the density of electrically active defects in the epilayer. Typical *total* defect densities (both electrically active and inactive) are 200-500 cm^{-2} with inactive defects (ovals and other minor features) accounting for 80-90% of this total.

In summary, a method has been described of fabricating and assessing linear arrays of MQW modulators, which, together with the use of a double-sided epitaxy technique, will allow a more compact implementation of photonic switching and neural network designs.

Acknowledgments

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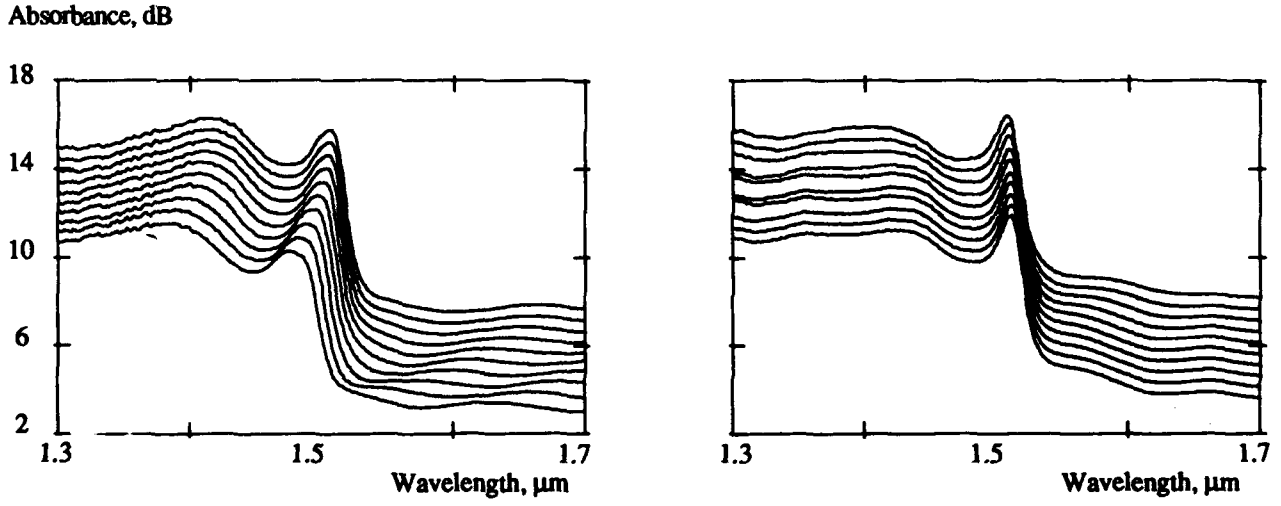


Figure 6. Comparison of radial uniformity of MQW layers grown by a) GS-MBE b) CBE, measured at 2mm intervals

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Asymmetric Fabry-Perot Multiple Quantum-Well PIN Diodes and S-SEEDs for Intra-Chip Optical Interconnections

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Abstract

We consider optical intra-chip interconnection schemes using Asymmetric Fabry-Perot Multiple Quantum Well PIN Diodes and compare the corresponding switching energies with that of an electrical interconnection with the same bandwidth.

1 Introduction

With advances in VLSI and WSI technology, the realization of high speed electronic systems becomes increasingly limited by the performance of metallised tracks. It has been suggested that optics can provide potentially a low-energy and broad-band communication interface within electronic processors (1-4).

In an optical interconnect the electrical signal lines are replaced by optical transmitters, imaging optics such as holograms, and photo-detectors. Comparison of optical and electrical interconnects using LEDs and lasers have already been presented by Kostuk and Feldman et al.(1,3). Feldman and et al. have also briefly considered the use of MQW modulators and silicon photodiodes in optical interconnects and show that they offer shorter break-even line lengths than for a laser, i.e. when the electrical interconnection switching energy is equal to the optical interconnection switching energy for the same link bandwidth.

Recently normally-off asymmetric Fabry-Perot MQW PIN diode modulators /photodetectors have been demonstrated (5) having high contrast and quantum efficiency at operating voltages of less than 5V. This offers electrical compatibility with MOS electronics for integrating an array of such devices with high-speed electronic islands for wafer scale communication (6).

In this paper we consider two optical interconnection schemes, the first consists of an Asymmetric Fabry-Perot (AFP) MQW-PIN modulator with a detector and derive a formal expression for the switching energy for different device sizes taking into account the contrast ratio and insertion loss of the diode. In the second scheme we propose a novel differential transmission and bistable detection system using Asymmetric Fabry-Perot Symmetric-Self Electrooptic Effect Devices(7) (AFP S-SEED). We show that in both cases the switching energy and thus the break-even line length can be considerably reduced by decreasing the area of the devices. The results are compared with switching energy required for a 2μm CMOS electrical interconnection and the break-even line length is plotted as a function of the optical link loss.

2 Asymmetric Fabry-Perot MQW-PIN Diode Transmitter / Receiver

The optical interconnection scheme considered is illustrated schematically in Fig.1. The light from an external laser source is fanned-out to an array of reflective modulators. The reflected light signal is then imaged one-to-one onto a similar array of devices which are each biased in series with a load transistor and then

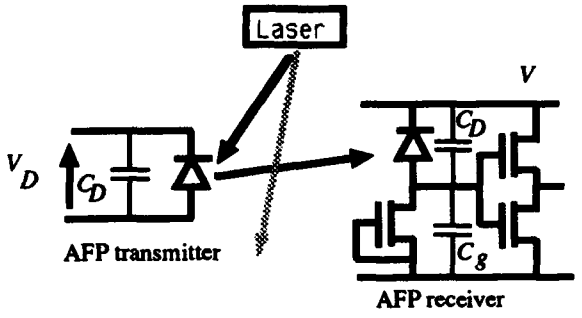


Figure 1 Schematic representation of first optical interconnection schemeusing asymmetric Fabry-Perot transmitter / receiver.

directly connected to the input gate of an inverter stage without any electronic gain stage. The rise-time, τ_o, is defined as the time required to charge the input gate voltage of the receiver from 10% to 90% of its final value, V. This implies that a modulator such as an AFP diode exhibiting a high contrast ratio of c >10:1 (i.e. the ratio of maximum to minimum reflectivity) should be used since it is tolerant to changes of the threshold voltage level of the following detection stage. The rise-time can be expressed as a function of the input optical power, the capacitance of the input inverter gate stage, C_g, the device capacitance, C_D, and the photon energy, E_P (units in eV) in the form of

$$\tau_o = 2V\,(C_g + C_D)\,\frac{E_P}{\eta_L P_i} \qquad (1)$$

The optical energy dissipated is given by $2\tau_o P_i$. The link efficiency, η_L is defined as

$$\eta_L = (1 - \Gamma_D)\,.\,\eta_H\,.\,\eta_D\left[1 - \frac{1 - \Gamma_D}{c}\right] \qquad (2)$$

where Γ_D is the insertion loss of the modulator, η_H is efficiency of the imaging hologram, η_D is the internal quantum efficiency of the device and the term in the bracket represents the minimum reflectivity of the modulator in the off-state.

Electrical energies are also dissipated to switch the state of the modulator, and to charge/discharge the capacitance of the photo-detector and input gate of the receiver stage. The total switching energy is the sum of both the electrical and optical energies dissipated. The electrical energy required to switch the state of the modulator does not depend upon fan-out F, so the switching energy can be expressed in the form of

$$E_o = 2F\,(C_g + C_D)V\left\{V(1 - 1/c)^2 + 2\frac{E_P}{\eta_L}\right\} + C_D V^2 \qquad (3)$$

3 Asymmetric Fabry-Perot MQW-PIN S-SEED Differential Transmitter/Receiver

The optical power reaching the detector determines the input gate voltage of the receiver. Since this power can fluctuate and the receiver has a fixed threshold, spurious switching can occur in the receiver. This problem can be overcome by using differential transmission and detection methods. The technique proposed here is to use bistable AFP S-SEEDs in a novel differential receiver circuit as shown in Fig.2. In the transmitter A pair of normally-off AFP diodes are connected in series and the driving voltage is applied at the central node to modulate the input light signals in complementary fashion. The reflected light signals are imaged onto a similar pair of AFP diodes operating as AFP S-SEED (7) with the central node connected to the receiver input gate stage. In the input receiver the gate voltage changes from high to low depending on the relative powers of the two optical signals.

The rise time is given by (6)

$$\tau_o' = 2(C_g + 2C_D)V\,\frac{E_P}{\eta_L' P_i} \qquad (4)$$

and the corresponding optical energy dissipated can be

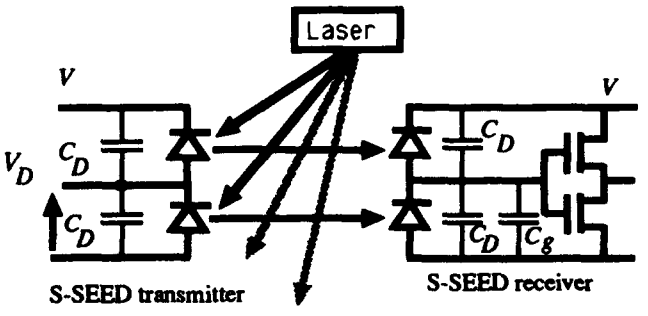


Figure 2 Schematic representation of second optical interconnection scheme using Asymmetric Fabry-Perot S-SEED transmitter / receiver devices.

expressed as $2\tau'_o P_i$. In this case, the optical link efficiency, η'_L, is defined as .

$$\eta'_L = (1 - \Gamma_D)\eta_H \eta_D (1 - 1/c) \quad (5)$$

The total switching energy can be written in a similar form as Eq.(3), but in this case the resistive load is replaced by a capacitive load of another AFP diode;

$$E_o' = F\,(C_g + 2C_D)V\left\{V + 4\frac{E_P}{\eta_L'}\right\} + 2C_D V^2 \quad (6)$$

4 Comparison of the optical interconnection schemes with an Electrical Interconnection

The switching energy of the optical interconnection schemes is compared with the electrical interconnection shown in Fig.3 for a 2μm CMOS process since this is currently in use. For a given rise-time, we define the break-even line length as the electrical transmission distance at which the optical interconnection switching energy is equal to electrical interconnection switching energy. The break-even line length is evaluated for different AFP diode sizes and the results are plotted in Figs.4 and 5 as a function of optical link loss. For the typical values (5) given in Table1 the overall optical loss is approximately 10dB as indicted by a vertical dashed line in Figs.4 and 5. The rise-time of electrical interconnection is calculated for different break-even line lengths. The optical power required to achieve the same rise as in an electrical case for the same break-even line length time can be evaluated from Eqs.(1) and (4) for the two optical interconnect systems. The results obtained are summarised in Table2.

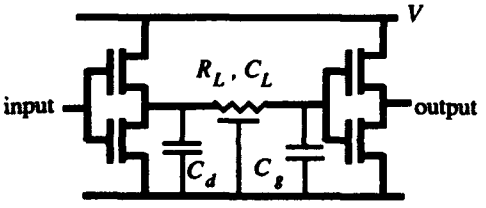


Figure 3 Schematic circuit diagram of an electrical interconnection.

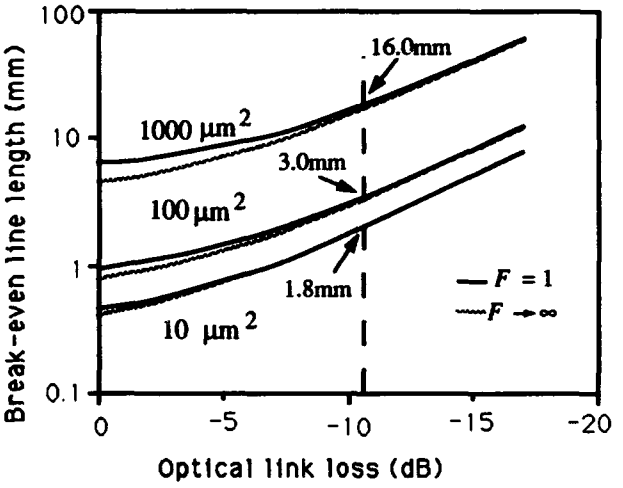


Figure 4 Break-even line length of asymmetric Fabry-Perot transmitter/ receiver compared with 2μm CMOS technology.

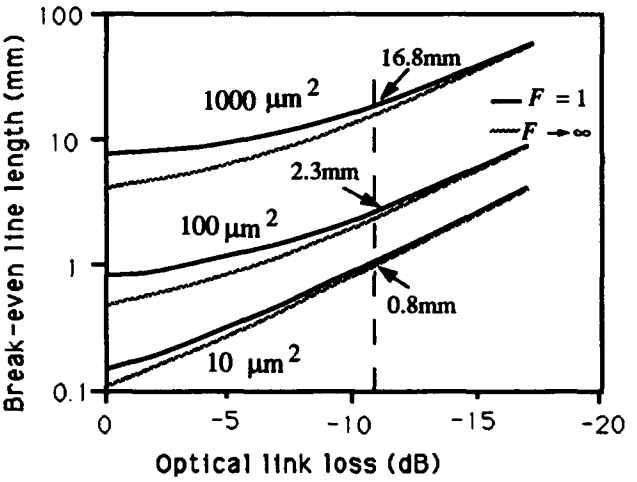


Figure 5 Break-even line length of asymmetric Fabry-Perot S-SEED transmitter/ receiver compared with 2μm CMOS technology.

Table 1

Supply voltage V =5V	Contrast ratio c 10:1
C_L ~ 0.7 pF/cm C_g = 16fF (for 2 μm CMOS) C_D = 182 aF / μm²	Insertion loss Γ_D 3dB AFPM quantum efficiency η_D 80%
Quantum energy of photons E_P = 1.45 eV	Hologram efficiency η_H 30%

Table 1 Typical parameters for the interconnection devices.

Table 2

η_L = 10%	Device size (μm^2)	Break-even line length (mm)	Rise time (nsec)	Optical power (mW)
AFP T/R	1000	16.0	24.9	1.2
	100	3.0	4.7	1.1
	10	1.8	3.2	0.8
S-SEED T/R	1000	16.8	26.2	2.1
	100	2.3	3.9	1.95
	10	0.8	1.6	1.78

Table 2 Comparison of optical and electrical interconnection schemes assuming optical link efficiency of 10%.

5 Discussion & Conclusion

From Figs.4 and 5 we see that the break-even line length increases steeply when the optical link loss rises to above 10dB. For 10dB optical insertion loss the break-even line length decreases from 17mm to 1mm as the device size is decreased from 1000μm^2 to 10μm^2. For the AFP S-SEED system the break-even line length decreases even further as the device area is decreased. In this case the resistive load is replaced by a capacitive load and, therefore, we expect the switching energy to reduce further as we scale down the device size. However, in practice the minimum device size is limited by the need to align imaging optics and also by the need to provide electrical connections to the device.

For a 10 dB optical insertion loss the optical power required for the AFP modulator system is about 1mW (or 64 mW for an array of 8 x 8), and for AFP S-SEED is about 2mW (or 128 mW for an array of 8 x 8) which within the range of the present laser diodes. However, the performance of AFP modulator / detector system is susceptible to variations of the optical power.

From the results obtained in Table2, the rise-time varies from 26 nsec to 1.6 nsec as the device size is decreased from 1000μm^2 to 10μm^2. These results do not take into account the capacitance of electrical connections of AFP diodes, since this depends on the mask design of the array, which tend to slightly increase the switching energy in both schemes.

In conclusion a novel differential scheme has been proposed for optical intra-chip interconnection which is more tolerant to optical power fluctuations than single modulator / detector link. It also offers lower switching energies for the optoelectronic devices less than 100μm^2 in size provided the alignment of the imaging optics can be achieved. Both schemes discussed require less switching energy than the electrical interconnection link distances greater than 2-3 mm for 100μm^2 device size.

Acknowledgment

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Optical Railtap Systems for Guided-Wave Optical Interconnects

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Abstract

An integrated-optical system for dense, guided wave interconnection of digital signals with many modulators and few lasers is described.

Introduction

Guided-wave optical interconnections offer many potential benefits for high performance integrated electronic systems [1]. These include higher packing density, lower noise, lower propagation delay, and frequency-independent network designs. Their major impediment to practical use, apart from being a new, unproven technology with little reliability data, has been the lack of a technology for practically integrating the components required to translate between electrical and optical signals. Most previously proposed schemes for guided-wave interconnects have required directly or externally modulating one laser or LED for each interconnection, often multiplexing many signals onto one optical interconnect to ease the relative expense. In effect, a multichip carrier, monolithic chip, or fully integrated wafer having thousands of high-frequency signals would require hundreds of multiplexed interconnection systems within an extremely small volume. This implies the optical interconnections will need to be fabricated in-place, effectively creating a printed optical circuit board. Such an optical circuit board would however be extremely low density, able to support many times the number of isolated waveguides than required in the available space. If small, efficient optical transmitters and receivers could be integrated into the optical circuit board so each optical interconnect would behave as an idealized electrical connection, the multiplexing could be discarded and the individual interconnects could be accomplished optically.

The Optical Railtap System

One of the primary challenges in developing a technology for integrated optical interconnection networks is being able to densely integrate waveguide transmitters that can be driven by the available electrical signals. A new solution to the problem of converting the electrical signal to optical form in an optical interconnect is provided through the use of a new device we call an optical railtap system. The system consists of an optical rail and a sequence of railtaps, as shown schematically in Figure 1. A passive optical waveguide, or rail, routs optical power around the package and acts as an optical power supply. The optical rail runs near the edge of every IC in the package and an optical tap switch is connected to every output pin. The purpose of the railtap is to convert the electrical data stream coming off of the IC output pin into light levels representing "1"s and "0"s, and to direct the optical data stream onto an optical channel that routes it to a receiver, which drives an input pin of the receiving IC. The railtap is a compact electro-optic modulator that is driven directly by the IC output electrical signal. Complementary taps, as illustrated in Figure 1, ensure that a constant amount of energy is extracted by each tap from the rail, regardless of the state of the logic signal, thus suppressing

crosstalk onto the rail. Each tap uses only a small fraction of the available light in the rail to create the routed signal. Since only a small fraction of the light is switched at each tap, only a small voltage is required, compared with conventional switches, and many optical signals can be generated from the optical power from a single CW laser. Figure 2 shows the result of a beam-propagation method simulation of 5 consecutive taps along a rail. Each tap switches approximately one percent of the optical power in the rail into one of two channels determined by the signal level on the electrode. The voltage used in this simulation is only 15% of the half-wave voltage for a Mach-Zehnder switch of the same length. Resolution is lost reproducing this picture, but it can be seen that light is switched to the left channels in the second and fifth tap and to the right in the first, third and fourth taps.

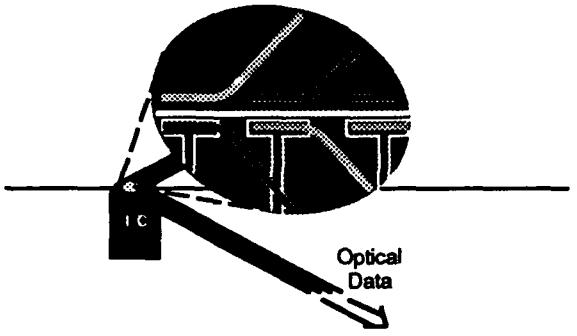


Figure 1. Schematic View of a Railtap for Optical Interconnects.

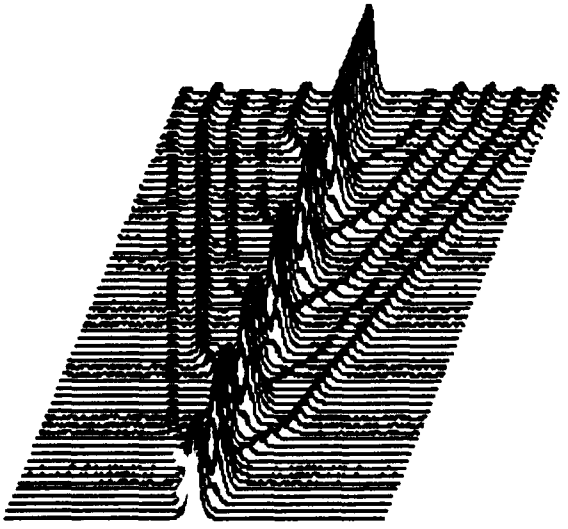


Figure 2. Simulation of 5 Consecutive 1%Taps

Figure 3 depicts the application of a railtap system to a multiline optical interconnection network. For railtaps fabricated in E-O polymer materials, the small optical signal can be modulated by a 1 volt electrical signal on a tap 1 mm long. The output of the IC is loaded only by the 0.1 pF tap instead of the electrical interconnection network, thus permitting systems designers to significantly increase the speed and reduce the power dissipated in the output drivers of VLSI chips. Additionally, optical signals can be exploited for fanout by using more optical power and passive waveguide splitters without any increase in the capacitive load on the electronic driver. The net result is that for high-speed logic a small, uniform, predictable electrical load for each signal pin can be achieved in a wide variety of configurations and applications.

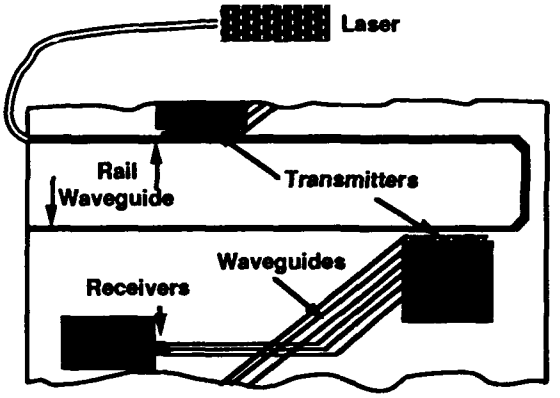


Figure 3. Railtap-based Optical Interconnects

A prototype railtap system has been built and demonstrated in electro-optic polymer materials[2]. The dimensions of one such device are shown schematically in Figure 5. The polymer was made electro-optic by electric field poling, and waveguide channels were made by selective photobleaching. The railtap was driven asymmetrically and modulated in a complementary fashion. Shown in Figure 4 are the intensity line scans of the output endface of the 3 port railtap. In each case the central spot is the optical rail, the signal line is on the right and the complementary signal is on the left. In the righthand picture the signal is applied and a strong beam appears in the signal channel, with almost no light in the complementary channel. In the lefthand picture, the complement of the

signal is applied and almost no light appears in the signal channel, while a strong peak appears in the complementary channel. In both cases, the optical power left in the central rail is almost unchanged. This is a critical feature for multiple taps, since coupling of the signal level to the rail intensity will contribute crosstalk to subsequent taps. Good complementary modulation of this device was observed up to 6 dB of modulation depth, much more than would generally be required in a railtap system.

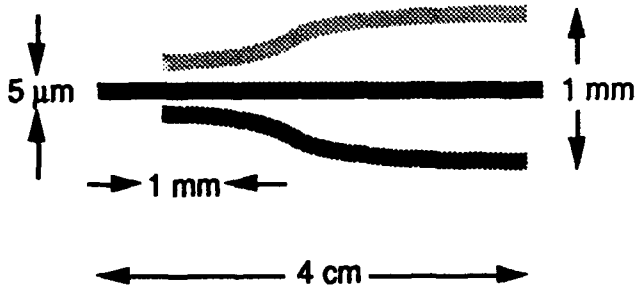


Figure 4. Dimensions of a Sample Single Element Railtap.

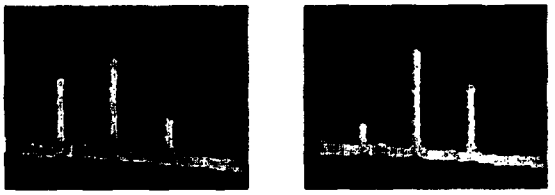


Figure 5. Intensity Line Scan Of the Railtap Endface Showing Complementary Modulation.

Figure 6 shows the measured frequency response of the test railtap. The upper trace is the signal from the railtap when driven with +15 dBm of electrical power for a drive voltage of 3.6 V peak to peak. The railtap response is flat from 50 Hz all the way out to approximately 20 MHz. Although at this point the RC roll-off of the electrode structure begins to reduce the signal, a signal is seen out to 100 MHz. The lower trace is

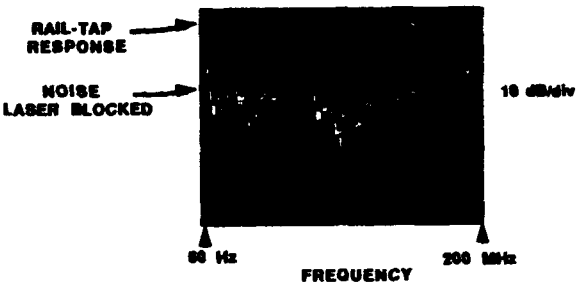


Figure 6. Frequency Response of the Test Railtap[2]

the noise measured with the laser light blocked from entering the device. The vertical axis is a log scale with 10 dB/div (electrical), showing a clear signal more than 30 dB above noise. At higher frequencies rf pick-up is observed.

With the development of new, stable electro-optic polymer materials[3], it is expected that the optical railtap system will soon be tested in practical applications to determine the true potential benefits of this device for highly integrated electronic systems.

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Novel Devices

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Quantum-Well Fabry–Perot Electro-Absorption and Refraction Modulators and Bistability

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INTRODUCTION

Following the demonstration of the absorption reflection modulator [1], many workers [2-10] have used Fabry-Perot resonators to improve the limited contrast ratio of these multiple quantum well light modulators. Most experiments have been in the normally on (Non), spectral region where absorption increases with field. Using field dependent GaAs/AlGaAs quantum well absorption data, we have created a model that calculates the reflectivity and contrast ratio of resonant and non-resonant modulators in both the normally off (Noff), region where absorption decreases with field, and the normally on (Non) spectral regions for use with photonic devices such as the self-electrooptic effect device (SEEDs). The calculations include both electro-absorption and electro-refraction effects.

When such a modulator is placed within a Fabry-Perot resonator we find that the change in reflectivity caused by electro-refraction can be quite comparable to the change due to electro-absorption in certain spectral regions. The model gives the optimum number of wells and reflectivity values required to make a resonator at any wavelength for a given quantum well structure. These results also show that with a resonator bistable operation of a SEED at wavelengths longer than the exciton is possible.

ELECTRO-ABSORPTION AND REFRACTION

The field induced changes in the optical absorption spectrum of a reverse biased diode are shown in Fig. 1a as obtained from photocurrent measurements. Also included is α_b of bulk GaAs. The absorption coefficient is scaled to the GaAs well thickness only. $\delta\alpha$ is shown in Fig. 1b at two representative fields and $\delta\alpha_{qw}$. The Kramers-Kronig changes in refractive index associated with this change in absorption are given by [11]:

$$\delta n(\omega) = (c/\pi)\, P \int_0^\infty \frac{\delta\alpha(u)\,du}{u^2 - \omega^2}$$

where P indicates the principal value of the integral. δn is shown in Fig. 1c. The $\delta n(E,\lambda)$, shown in Fig. 1c, is relative to the $E = 0$ quantum well dispersion $\delta n_{qw}(\lambda)$. The latter can be estimated from $\delta\alpha_{qw}$ relative to that of bulk GaAs shown plus the slowly varying dispersion of the bulk GaAs. In all calculations that follow we include the estimated dispersion of the quantum well $\delta n_{qw}(\lambda)$.

REFLECTION MODULATOR

Quantum well electro-absorption reflection modulators are grown with a multilayer dielectric mirror of reflectivity r_2 beneath the intrinsic quantum well region. The front surface has a reflectivity r_1 which when antireflection coated equals 0. The round trip MQW transmission (excluding the rear mirror reflection coefficient r_2 and assuming $r_1 = 0$) in the on (low loss) state is given by

$$t_{on}^2 = \exp(-2N\alpha_{on}L_w) = \exp(-2a_{on}N)$$

where a_{on} is the absorption per quantum well, N the total number of quantum wells and we assume that all loss is associated with the well thickness L_w and ignore the barrier thickness. The reflectivity is not affected by electro-refraction in the absence of a Fabry-Perot (FP) resonator.

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A modulator is off when the absorption is high, α_{off}, and on when the absorption is low, α_{on}. Measures of the modulator performance are the change in the reflection coefficient, δR, and the contrast ratio CR.

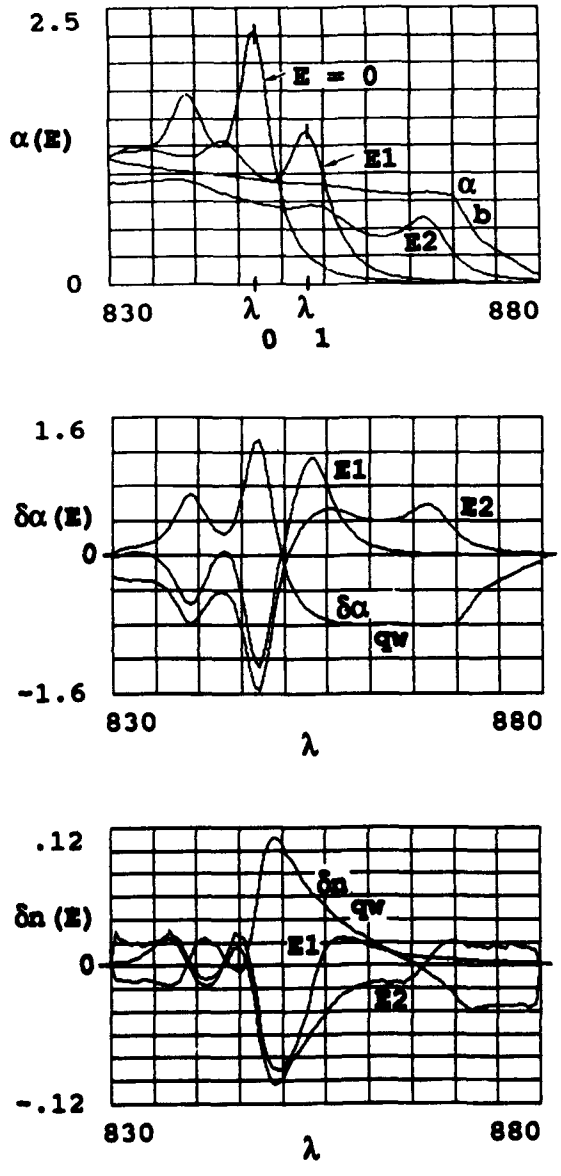


Fig. 1 a: Absorption spectrum at fields E = 0, E1 = 9.0 V/micron and E2 = 16.5 V/micron. The exciton is at λ_0 = 847 nm. λ_1 = 853 nm and 866 nm (red shift region) are wavelengths of interest. The MQW material is x = 0.3 AlGaAs barriers (35Å) and GaAs wells of L_w = 95Å.
b: $\delta\alpha = \alpha(E) - \alpha(E=0)$ for E1 and E2.
$\delta\alpha_{qw} = \alpha(E=0) - \alpha_b$.
c: Electro-refractive and quantum well index change calculated from the Kramers-Kronig relation.

These can be expressed in terms of a figure of merit

$$f = \alpha_{off}/\alpha_{on}$$

which at λ_0 for field E2 is f = 3.1 and at λ_1 for field E1 is f ≈ 6. For the longer λ_1 f is near 60. We shall compare only the first two examples herein.

The change in reflectance between the two states is

$$\delta R = R(on) - R(off) = r_2 t_{on}^2 [1 - t_{on}^{2(f-1)}]$$

and the contrast ratio

$$CR = R(on) / R(off) = t_{on}^{-2(f-1)}$$

δR and CR are a function of $a_{on}N$, the absorption per pass (the loss) in the highly transmitting state (low loss), for various values of the figure of merit f. These are universal performance curves. As an example consider operating at field E2 and at λ_0 where from Fig. 1 f = 3.1 and a_{on} = .007. If N = 60 then $a_{on}N$ = .42 and from Fig. 2 δR = .34 and CR = 5.9.

Without a FP resonator, operation at λ_0 results in a Noff device, while operation at λ_1 is Non. When a modulator is placed in a symmetric SEED

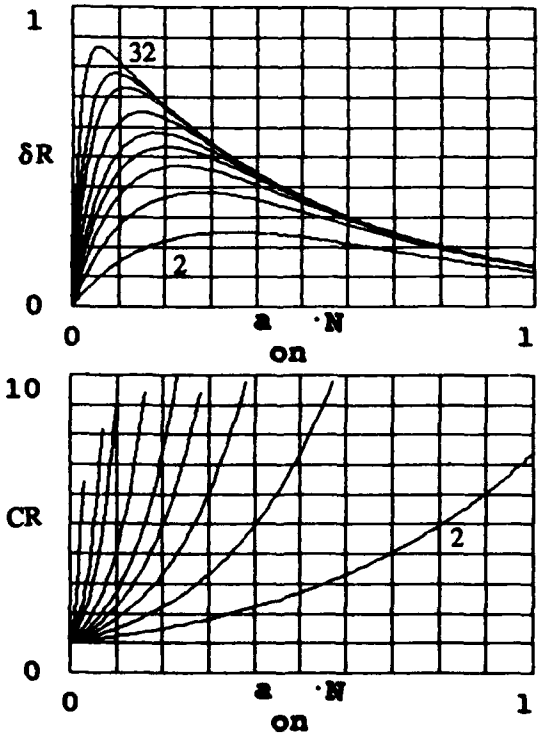


Fig. 2a,b: Maximum change in reflectivity δR and contrast ratio CR as a function of $a_{on}N$. The increasing curves represent values of f = 2, 3, 4, 5, 6, 8, 12, 16, 32. r_2 = 1 and r_1 =0.

configuration of two diodes in series where bistability is the desirable feature then the figure of merit [12] to be maximized is approximately $\delta R[1-R(on)]$. The maximum occurs for $\delta R = .50$, which also implies $R(on) = .50$. The above criterion is based on the switching energy being proportional to the difference in reflectivity of the diodes in the first stage multiplied by the minimum absorption of the diode in the following stage.

FABRY-PEROT REFLECTION MODULATOR

In the following we will discuss the use of Fabry-Perot resonators to improve the performance of the quantum well modulators. By using FP resonators, both Non and Noff operation is possible at any wavelength. This allows the design of bistable modulators at the longer wavelength λ_1 where the highest R_{on} is obtainable.

If the front surface reflectivity r_1 differs from zero a Fabry-Perot (FP) resonator results. r_1 and/or the number of quantum wells N can be adjusted to match the input optical beam so that there is no reflected energy at a given field. This matching for R_{off} can be with either α_{on} or α_{off}, requiring only different values of r_1 or N. With a different applied field the resonator is no longer matched and reflected energy results. Contrast ratios greater than 100 have been observed in Non devices [4,9] and Noff [6,9] devices. One can show that the required reflectivity r_1 for matching of a FP modulator on resonance is given by

$$r_1 = r_2 t_{off,on}^2$$

for respectively Noff and Non operation. The reflectivity, when the match is broken, as a function of wavelength, λ, is given by

$$R = r_2 \frac{\left(t_{on} - t_{off}\right)^2 + 4t_{on}t_{off}\sin^2\phi}{\left[1 - t_{on}t_{off}r_2\right]^2 + 4t_{on}t_{off}r_2\sin^2\phi}$$

where ϕ is a function of λ and E, because of electrorefraction. If electro-refraction were absent then the FP resonance can be placed exactly on the wavelength for which the resonator was designed and it does not shift when the field is applied. Thus at the desired wavelength, $\phi = 0$. The change in absorption breaks the matching condition $t_{on} \neq t_{off}$ and a finite reflectivity results. Note the symmetry which implies the same peak reflectivity with a given N for matching with either Noff or Non operation, though the required r_1 is different. When electro-refraction is included, δn is large enough, in some regions of the spectrum, to shift the δn such that the reflectivity is significantly enhanced in the unmatched state.

The effects of electro-absorption and refraction can be quite comparable. Observe in Fig. 3a the calculated FP reflection spectrum, both with and without the δn of electro-refraction. With E = 0 and the FP resonance near the exciton the resonator is matched. The application of the field E2 reduces the loss and the resonator is no longer matched. δn is a maximum at about 849 nm which shifts the FP resonance toward shorter wavelengths and we find that $\delta R_{max} = .35$ at 848.5 nm if the FP resonance is shifted from the exciton to 848 nm. In Fig. 3b observe the increase of δR from .22 to .35 with the inclusion of δn electro-refraction effect. For a FP (neglecting δn) the calculated R_{on} of .22 is less than the $\delta R = .34$ of a 60 quantum well modulator ($r_1 = 0$) which though only has a CR = 5.9. Inclusion of δn increases R_{on} to .35 which is close to the δR

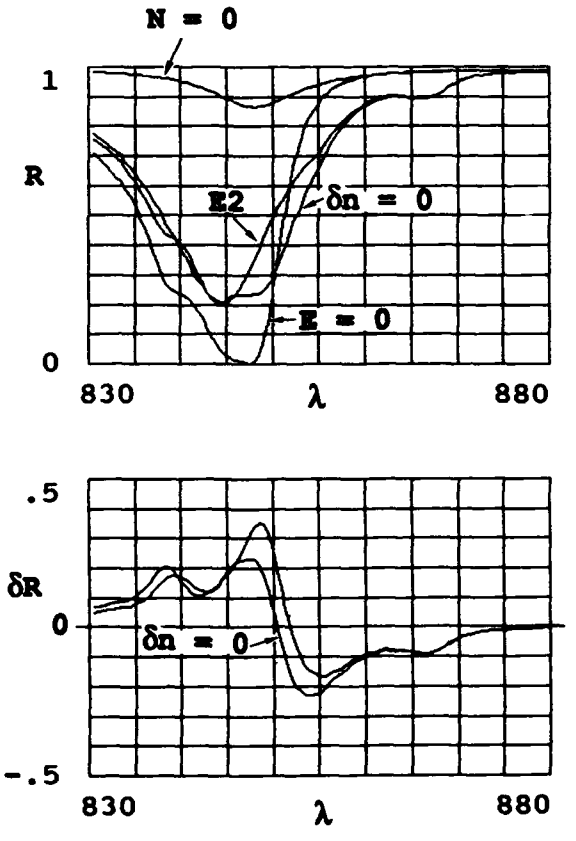


Fig 3 a: Reflection spectrum of a FP resonator with $r_1 = .31$ and $r_2 = .96$. N=0 shows that the FP resonance has been placed at the 848 nm. N = 26 is required for matching in the Noff case. The curves for E2 both with and neglecting refractive index changes ($\delta n = 0$) are shown.

b: δR with electro-absorption only (smaller value) and with electrorefraction included (greater effect).

obtainable with the $r_1 = 0$ modulator (no FP) but with CR >> 1 indicating that a FP has comparable δR to a similar modulator but with increased CR.

A symmetric SEED, constructed of two Noff modulators placed in series, operating at λ_0 is bistable. This is because the absorbed energy decreases with increasing voltage drop across the device which is positive feedback implying bistability. At λ_1 a non FP modulator is Non and a SEED device would only show a threshold effect. However a FP modulator operating λ_1 can be designed either Non or Noff. When the Noff design (requiring greater N than for Non) is placed in a Symmetric SEED configuration it is potentially bistable.

The use of a resonator with a red shift device to obtain bistable operation was long ago recognized by Ryvkin [13]. Advantages of this approach are that at λ_1 the figure of merit f is larger so that a greater δR is possible than at the exciton wavelength λ_0, albeit with increased N and complexity.

If one evaluates the contrast ratio CR at resonance (E = 0 so δn = 0) as a function of N one can determine N required for matching as shown in Fig. 4. The positive cusps correspond to a Noff device while the negative ones indicate an Non device. Double cusps indicate the possibility of making either of these devices at the same wavelength, only by using different values for N. Note at λ_1 that Noff operation requires higher N and/or r_1. Note also that increased r_1 reduces the number of wells required for matching, thus the applied voltage. However the switching energy will not be reduced because the capacitance is inversely proportional to N.

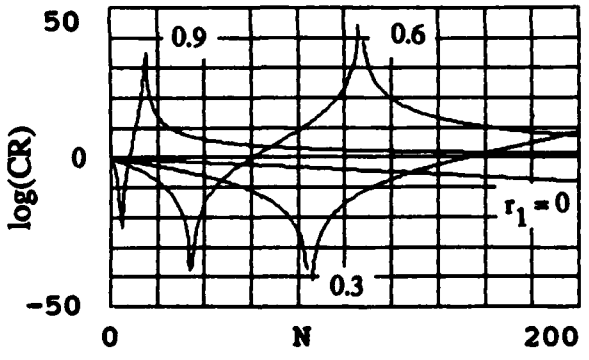


Fig. 4 Log_{10} CR = R(E1)/R(E=0) vs N, with the FP resonance at λ_1 = 853.5 nm. The front mirror r_1 = 0, 0.3, 0.6, 0.9

CONCLUSIONS

To understand a FP enhanced quantum well modulator it is necessary to include quantum well dispersion, electro-absorption and electro-refraction effects. With electro-absorption only, the FP modulator would have a smaller δR than a non resonant modulator but with electro-refraction included δR of a FP modulator can exceed the non resonant modulator. Significant effects also occur at wavelengths longer than the exciton wavelength λ_0. It has also been proven that for a given N, the peak δR is independent of a Noff or Non matching. We have also discussed how a SEED device can be made bistable at λ_1 using a Noff FP modulator. The results are qualitatively valid for any quantum well electro-absorption modulator.

ACKNOWLEDGMENTS

We appreciate stimulating discussions with D. A. B. Miller and A. L. Lentine in the early stages of this work.

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92-17295

All-Optical, High-Contrast Asymmetric Fabry-Perot Modulator

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Abstract

We have demonstrated all-optical modulation of a normally off asymmetric Fabry-Perot etalon with a non-linear GaAs/AlGaAs multiple quantum well spacer. Large changes in reflectivity were observed giving an extremely high contrast ratio of 160:1 with less than 1 dB insertion loss. We have determined the nature of this modulation to be due to strong absorption and refractive index changes in the non-linear spacer.

Reflection modulation in non-linear asymmetric Fabry-Perot etalons has recently received a lot of attention. High contrast ratios have been reported by several authors by suitable electro-optic modulation of the absorption in the etalon cavity [1,2]. These methods however give rise to large insertion losses due to the limited amount of absorption modulation that can be produced In this work we have experimentally investigated the modulation characteristics of an asymmetric Fabry-Perot with a non-linear multiple quantum well (MQW) cavity when optically excited and have obtain a very high contrast ratio with a considerably reduced insertion loss. We have analysed the intensity dependence of the etalon reflectivity and have determined that the modulation is due to the combined effects of absorptive and dispersive changes around the excitonic absorption peak of the MQW.

The principle of reflection modulation of an asymmetric Fabry-Perot etalon is as follows. An asymmetric Fabry-Perot etalon has mirrors of unequal reflectivities. The reflectivity R of the etalon at a reflection resonance mode is given by,

$$R = \frac{R_f(1-\frac{R_\alpha}{R_f})^2}{(1-R_\alpha)^2} \qquad (1)$$

where R_f is the front mirror reflectivity, R_b is the back mirror reflectivity and R_α is given by,

$$R^2_\alpha = (R_f R_b)\ \exp(-2\alpha d) \qquad (2)$$

for absorption coefficient α and cavity thickness d. With R_f substantially less than R_b and no absorption in the cavity, the etalon reflectivity at resonance is high. With an absorbing cavity, the effective reflectivity of the back mirror is lowered and the etalon reflectivity at resonance is correspondingly smaller. From (1) above it can be seen that with the following condition:

$$R_f = R_b\ \exp(-2\alpha d) \qquad (3)$$

the etalon reflectivity is zero on resonance and the cavity is said to be impedance matched. Hence intensity modulation of the absorption in the cavity modulates the etalon reflectivity providing the basis of an optical switch with a theoretically infinite contrast ratio and potentially low insertion loss.

To implement this effect in an actual device we used the strong non-linear absorption changes around the band edge of a GaAs/AlGaAs multiple quantum well [3]. The structure was grown by MOVPE and consists of a dielectric stack mirror with a reflectivity > 97% at the operating wavelength of 853nm, grown on an undoped GaAs substrate. On top of this a GaAs(95Å)/$Al_{0.3}Ga_{0.7}As$(69Å) multiple quantum well structure was grown forming a nonlinear etalon cavity. The front reflectivity is that of the air/semiconductor interface and is approximately 32%.

The heavy hole exciton wavelength was chosen to be close to a mode of the etalon by choosing 95Å wells and the well number was chosen such that the absorption by the exciton almost gave impedance matching conditions at low input intensities. This is a normally off device in that the reflectivity is low at low optical intensities.

The reflectivity spectrum of the device is shown in figure 1. aswell as the transmission profile of the MQW. The absorption and hence the transmission profile of the MQW was obtained by anti-reflection coating a piece of the sample and using the Bragg mirror to give a double pass of the light.The transmission spectrum shows a heavy and light hole exciton feature, the heavy hole exciton is at 850nm. The reflection spectrum shows three minima in the vicinity of the excitons. The lowest minimum is at 853.4 nm , 3.5 nm to the low energy side of the heavy hole exciton peak. The reflectivity in this particular case is 0.5% ,showing almost complete impedance matching at this wavelength. The presence of the other two reflection minima and the steepness of the curve above 853.4nm (much steeper than expected for such low finesse device) is due to the strong refractive index dispersion around the exciton peaks in addition to the strong absorption variation. Both effects have a large impact on the reflectivity of an asymmetric cavity such as this.

The reflectivity of the device was measured as a function of intensity at 853.4nm where the lowest reflection point in figure1. occurs. Figure 2 shows the corresponding changes when optical powers up to 120mW were focussed on the sample.The reflectivity measurements were carried out using an argon ion pumped Titanium-Sapphire laser. To reduce any thermal effects in the sample the exciting beam was pulsed using an acousto-optic modulator giving 1μs pulses at a repetition rate of 1kHz. The beam was focussed on the sample to a measured spot size of 7.5μm and the measurements were made using both an oscilloscope and lock-in amplification. All measurements were normalised against a highly reflecting infra-red mirror with a reflectivity >99.9% at 853.4nm.The reflectivity is seen to increase from 0.5% to approximately 80% giving an extremely high contrast ratio of 160:1 when the input intensity is varied from zero to 120mW. This behaviour is due to the saturation of the excitonic absorption due to phase space filling and fermion exchange[3].

In order to investigate the precise nature of this large change in reflectivity we also measured the non-linear absorption in the MQW using the anti-reflection coated piece of the sample. This is shown in figure 3 where we have plotted αd, the absorption coefficient times the cavity width, versus incident power at 853.4nm. From this, equation (1) was used to calculate the reflectivity as a function of incident power. This is shown in figure 4 where where we have also reproduced the experimental data of figure 2 for comparison. While the experimental and calculated values agree at low intensities there is a wide divergence at higher

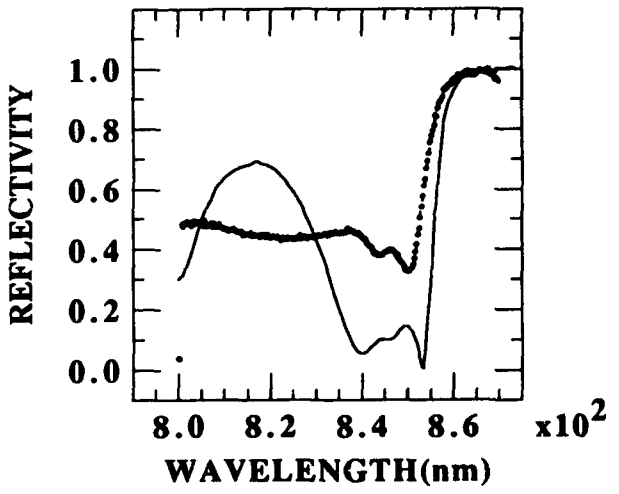


Figure1. Reflection spectrum of AFP (light line) and transmission spectrum of MQW spacer(heavy line)

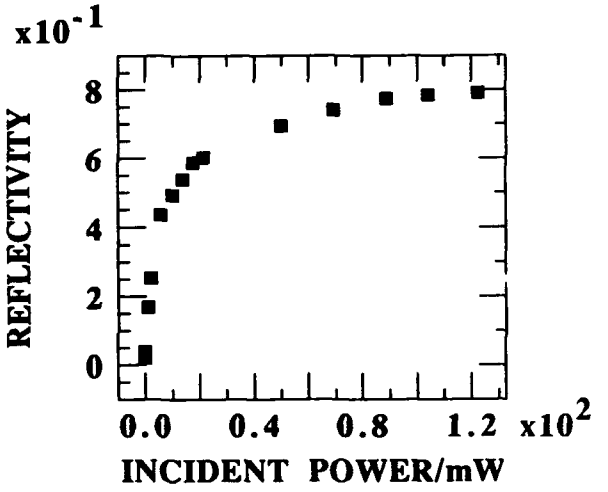


Figure2. Reflectivity of AFP at 853.4nm as a function of incident optical power.

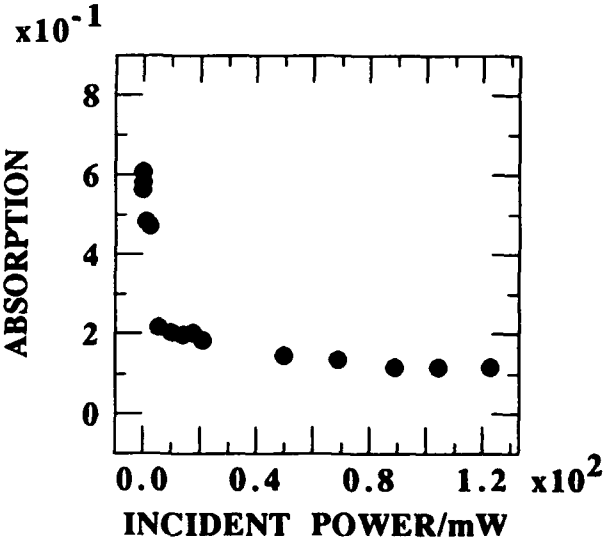


Figure 3 Absorption saturation of MQW at 853.4nm

intensities with the experimental values greater than the calculated ones.The agreement at low intensities is consistent with absorption saturation of the excitonic resonance at high optically induced carrier densities in the MQW.
The divergence at high intensities indicates that there is an additional change in refractive index occuring. A negative change in refractive index would reduce the optical path length in the cavity and changes the operating condition from the low on-resonance state to the highly reflecting off-resonance state.
From the difference in reflectivities in figure4 we determined the change in refractive index at the operating wavelength as a function of incident power This is shown in figure 5 where we have plotted the (negative) change in refractive index Δn versus incident power and shown it to saturate at approximately -0.06.

An empirical fit based on,

$$\Delta n(p) = \delta n_S \frac{p/p_S}{1+\frac{p}{p_S}} \qquad (4)$$

where δn_S is the maximum index change and p_S is the saturation power is also shown. We have obtained a saturation power of approximately 7mW which from our measured spot size and the cavity absorption corresponds to an optically generated free carrier density in the wells of 3.2×10^{18} cm^{-3}. This figure is in agreement with previous work [4].

In conclusion we have demonstrated optical modulation of a normally-off asymmetric Fabry-Perot structure and have obtained an extremely high contrast ratio and very low insertion loss. We have determined that the large changes in reflectivity obtained can be attributed to a combination of absorption and refractive index saturation resulting from the saturation of excitonic absorption in the multiple quantum well cavity. The characteristics of the device are good for an optically addressed modulator.

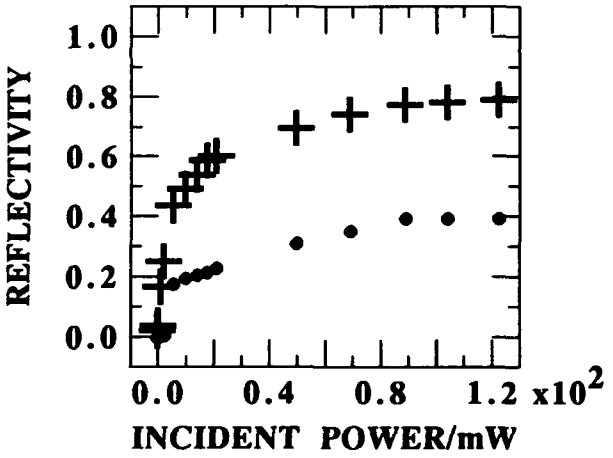


Figure4 Comparison of measured AFP reflectivity (crosses) with reflectivity calculated from absorption saturation alone(dots) as a function of input power.

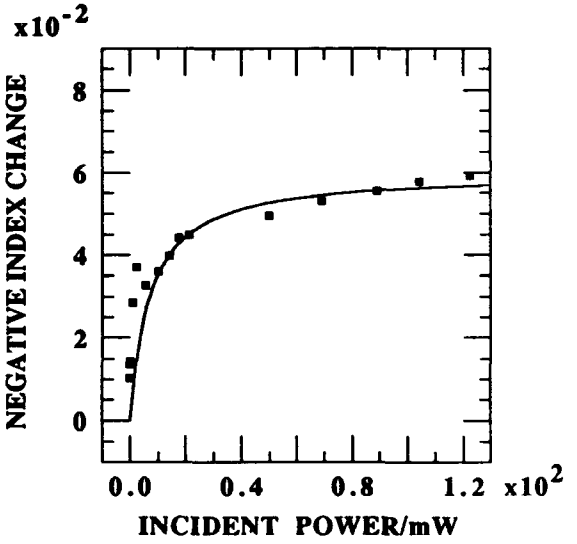


Figure 5. Measured negative change in refractive index of MQW at 853.4 (points) calculated from the data of Fig.4. Also shown is an empirical fit based on Eqn.4. in text.

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92-17296

Low-Threshold Optical Bistability in Bulk GaAs Etalons

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Abstract

A nonlinear Fabry-Perot device with a 2 μm bulk GaAs spacer has been optimized numerically. A corresponding sample, grown by molecular beam epitaxy, exhibits thermally stable switching with contrasts of 8:1 and thresholds as low as 1 mW.

Besides the switching behavior, we present measurements of the dependence of switching threshold and contrast on spotsize and wavelength detuning.

Introduction

A promising device for parallel optical computing is the nonlinear Fabry-Perot (NLFP), where a nonlinear refractive index change related to optical carrier excitation in a semiconductor layer is amplified inside a Fabry-Perot cavity. Research activity in this field [1,2,3] has evolved towards all-epitaxially grown structures; the use of alloy and multiple quantum well material; thermally stable operation; and, recently, towards biased and array operation.

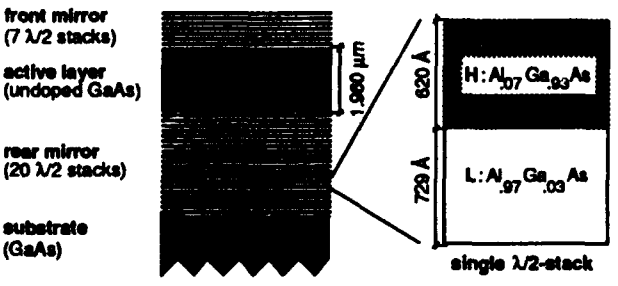


Figure 1. Layout of the 2 mm bulk GaAs NLFP.

Device optimization and design

Bragg reflectors

The two Bragg reflectors are formed by λ/4 $Al_xGa_{1-x}As$ stacks of alternating high and low refractive indices, by changing the aluminium concentration. For the high index layer, a choice of x = 0.07 guarantees transparency at the operating wavelength, whereas in the low index layer, some GaAs-monolayers improve the growth quality of AlAs giving an effective x = 0.97. The two values of refractive index lead to a typical stopband width of 100 nm.

The optimum rear reflectivity being $R_b = 1$ for reflective type devices, the front mirror reflectivity R_f, and therefore the number of layers, is determined by the impedance matching condition [4,5]

$$R_f = R_b \cdot \exp(-2\alpha L)\,, \qquad (1)$$

for a given nonlinear spacer layer of length L and intensity absorption α (at operating conditions λ,N).

Spacer layer

To determine the principal design parameters, namely the operating wavelength λ and the length of the active layer L, we minimize the threshold intensity, using a numerical model which is based on the solution N(I) of a self-consistent steady-state carrier density rate equation, where I is the intensity in the cavity:

$$\frac{I\cdot\alpha(N)}{h\nu} - \frac{N - N_0}{\tau_{rec}} = \frac{\partial N}{\partial t} = 0\,. \qquad (2)$$

The optical properties α(λ,N) and Δn(λ,N) are interpolated from published experimental data [6]. (A recombination time τ_{rec} = 4 ns and a carrier density at thermal equilibrium $N_0 = 10^{15}$ cm^{-3} are assumed.)

Our simulations suggest an optimum operating wavelength for dispersive nonlinearity about 20 meV below the absorption edge (1.425 eV in bulk GaAs), with a refractive index change $\Delta n \approx 0.03$ and a residual absorption $\alpha \approx 200\ cm^{-1}$.

In agreement with theory [4,5], an almost proportional decrease of the threshold intensity with spacer length is predicted. We expect an optimum cavity length between 0.5 and 1.0 µm, below which the robustness with respect to growth parameters, as well as the range of allowable detuning, is strongly reduced.

Nevertheless, we chose a spacer of 2 µm (Fig. 1) for our first design, in order to have it more robust.

Linear characteristics

A low intensity reflection spectra of the grown sample (Fig. 2) shows the stop band of the Bragg reflectors with a reflectivity of ≈98 % below the band gap of the spacer layer ($\lambda > 870$ nm). A Fabry-Perot resonance with a minimum reflection of 10 % is located at 882 nm. The FWHM of 0.9 nm with a free spectral range of 30.7 nm corresponds to a finesse of 34.

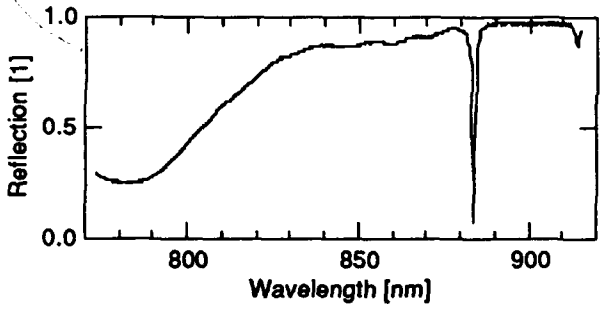


Figure 2. Reflection spectrum of sample #360.

To reduce the influence of growth calibration errors, sample #360 was grown as a wedge (by stopping the sample rotation during 10 % of the spacer growth). Perpendicular to this gradient we found a resonance wavelength change of 1 nm per mm. In a central disk of 10 mm diameter the total change is ≤2 nm. (Fig. 3)

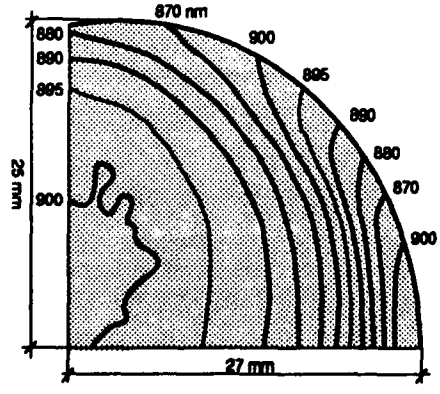


Figure 3. Resonance contour lines on wafer #360.

Nonlinear measurements

For the nonlinear measurements, sub-microsecond pulses with a repetition rate of 10 kHz, to avoid sample heating, were generated from the cw-output of an Ar-laser pumped Ti:Al_2O_3 laser by means of an acousto-optic modulator (Fig. 4).

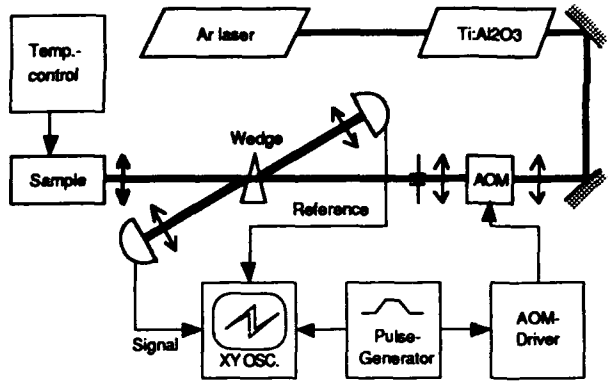


Figure 4. Experimental setup used.

Nonlinear refractive index measurements

Using lock-in detection to measure the shift of the FP-resonance with increasing intensity, the nonlinear refractive index change in the GaAs material has been studied. The predicted saturation behavior has been found and our estimated change of refractive index with intensity $\Delta n/\Delta I \approx 3 \cdot 10^{-5}\ cm^2/kW$ [8] is in agreement with a similar study [2] and our model (Eq. 2), provided the effect of diffusion is accounted for. (cf. spotsize dependence measurements)

Bistable switching

Looking at the nonlinear response in reflection, switching contrasts higher than 8 to 1 (Fig. 5), and switching powers as low as 1 mW have been observed.

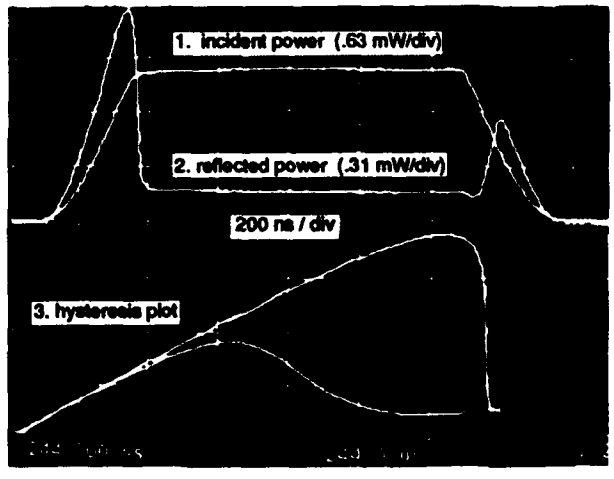


Figure 5. Incident and reflected intensity vs. time, and the corresponding plot of reflected vs. incident intensity.

Critical slowing down has been observed close to the switching threshold, from which we estimate an approximate switching energy of 15 pJ.

Due to the low threshold, thermally stable (>1 s) switching is possible with heat sinking through the 0.5 mm GaAs substrate only.

Detuning dependence

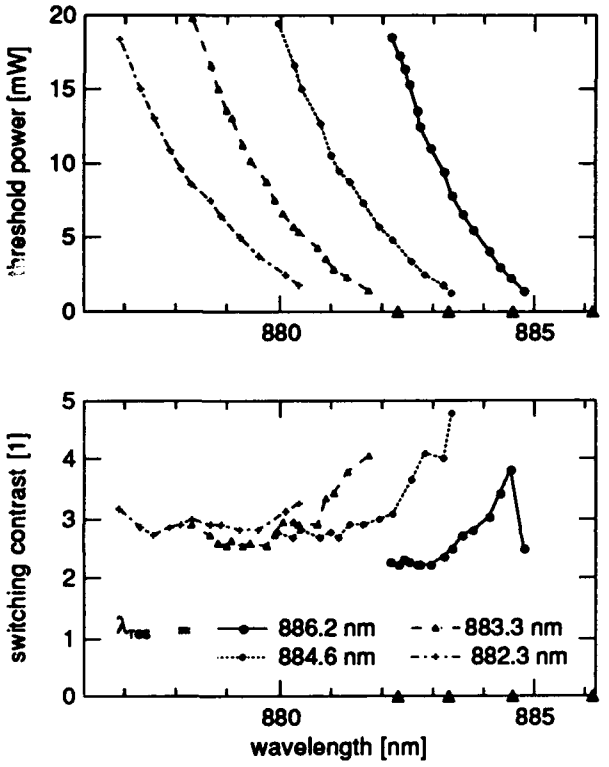


Figure 6. a) Threshold power vs. operating wavelength and b) corresponding switching contrast for different resonance wavelengths.

The dependence of the switching on the detuning was investigated for different resonance wavelengths by measuring at different locations on the wafer.

As predicted [5], bistable operation starts about 1 FWHM below the resonance wavelength at a minimum threshold. For a higher detuning, the threshold increases strongly, with ≈3 mW/nm (Fig 6a), almost independent of the resonance wavelength. The corresponding contrast (Fig. 6b) does not depend as strongly on the detuning; we find an increase towards long wavelengths with a maximum at 883 nm, where the impedance matching condition is best fulfilled.

The observed dependence of the switching threshold is an important issue for system tolerances: assuming that the device gain is sufficient to accommodate a threshold tolerance of 10 %, the operating wavelength would be restricted to within a range of 0.1 nm.

Spotsize dependence

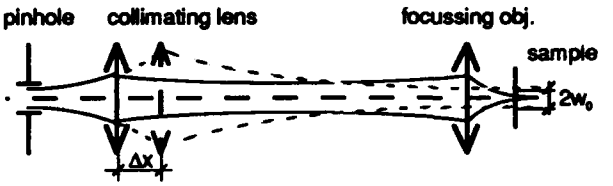


Figure 7. Setup using a spatial filter with a movable collimator to change the numerical aperture of the focussing objective.

In order to determine the influence of carrier diffusion and diffraction, we studied the switching behavior for different spotsizes using the varying collimator setup shown in Fig. 7, which produces gaussian spots with beam waists between 2 and 20 μm.

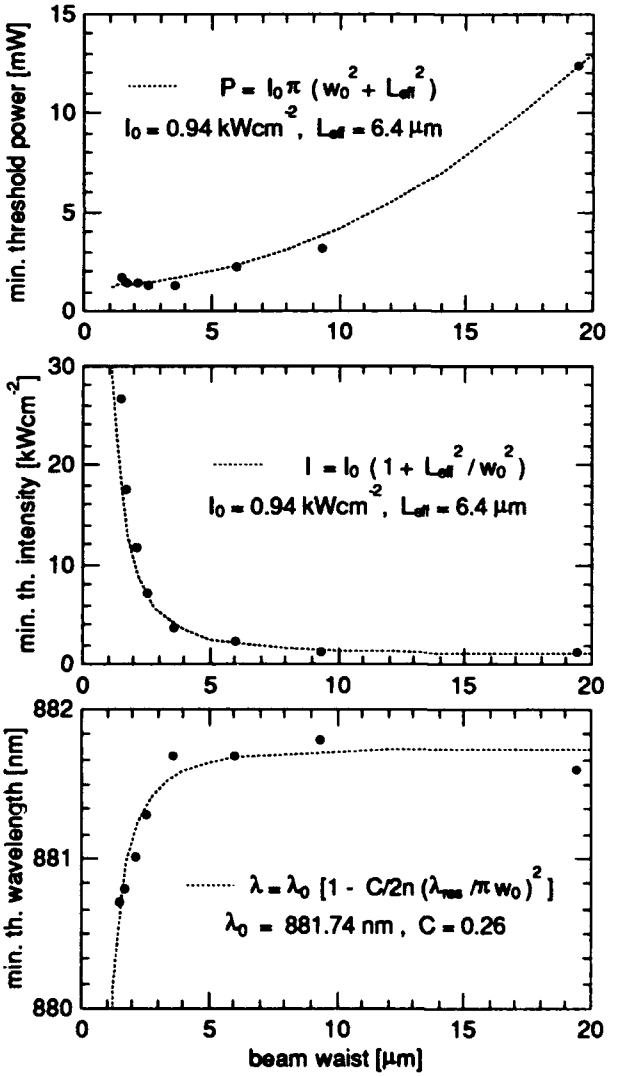


Figure 8. a) Minimum threshold power, b) intensity and c) required detuning vs. beam waist (λ_{res} = 882.85 nm).

As expected, the threshold power scales with the spot area, down to a minimum at a beam waist of ≈3 μm (Fig. 8a). From a simple fit, which assumes a diffusion limited spotsize in the limit of vanishing beam radius, we find an effective diffusion length $L_{eff} = 6.4$ μm and, for asymptotically large spots, a threshold intensity $I_0 = 0.94$ kW/cm^2.

Note that the strong influence of diffusion on the threshold intensity at small spotsizes (Fig. 8b) helps to explain the low values for n_2 found in our nonlinear refractive index measurements.

For the switching contrast a slight increase of less than 25 % towards small spots is observed.

The minimum detuning required for bistable switching diverges for beam waists below 2.5 μm (Fig. 8c). This diffractive resonance broadening is modeled in the curve fit by a detuning increase proportional to the change of the resonance wavelength with incidence angle ($\Delta\lambda \sim NA^2$). It can explain the threshold power increase observed below 2.5 μm beam waist in Fig. 8a, however, carrier density dependent recombination may also be significant.

Conclusions

Thermally stable switching with a contrast as high as 8:1 and a threshold as low as 1 mW has been observed in a nonlinear Fabry-Perot device with bulk GaAs spacer. These results compare favorably with results reported for devices with MQW spacer material.

Measurements with variable spotsize indicate that carrier diffusion dominates the switching power for spotsizes smaller than 12 μm diameter (NA=.05). Below about 4 μm diameter (NA=.14) diffraction and carrier dependent recombination effects become important.

While today's MBE growth techniques should allow for reproducible devices over mm^2 areas, the strong wavelength dependence of the threshold tends to limit the achievable gain and requires precise control of the source wavelengths on the order of about 0.1 nm.

Acknowledgments

We would like to thank M. Proctor, C. Wüthrich and Dr. N. Collings as well as Profs. F.K. Reinhart and R. Dändliker for helpful discussions and encouragement. This research is supported by a grant of the Swiss National Science Foundation.

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Optical Latch and AND Gate Based on an InGaAs/InP Light Amplifying Optical Switch

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Abstract

An optical latch is proposed and integrated monolithically. The basic structure of the device consists of a light amplifying optical switch (LAOS), which is operated as an optical bistable switch and formed by the vertical integration of a heterostructure phototransistor (HPT) and a light emitting diode (LED), and another HPT integrated on the same chip and electrically connected in series to the LAOS device. The additional HPT acts as an optical control which gates the electrical current of the bistable switch. The functionality of the optical latch is experimentally demonstrated. An optical AND gate is also demonstrated using a discrete HPT component with a similar configuration as latch circuit but with lower electrical bias.

I. Introduction

Optical switching devices are of much interest in optical computing systems, especially for optoelectronic integrated circuits (OEICs). Several types of optical bistable switching devices have previously been developed with OEICs, such as, the self electro-optic effect device (SEED), the double heterostructure optoelectronic switch (DOES), a light amplifying optical switch (LAOS), which is an integration of a heterostructure phototransistor (HPT) with a light emitting diode (LED), and the pnpn switch. With the exception of the SEED, all of these switches have demonstrated a similar switching I-V curve composed of a high-impedance off-state, a low-impedance on-state and a differential negative resistance region connecting the two as shown in Fig. 1 for a LAOS device. Most of these switches can be triggered on by a light pulse but cannot be turned off by an optical signal. Instead, the electrical bias to the device must be reduced to near zero [1, 2]. This is not practical for the operation in OEICs, since this requires additional circuitry and all devices must be turned off at the same time.

There are two techniques for realizing an all-optical bistable switch using the LAOS devices. The first technique (parallel type) places an optically sensitive control element in parallel with the switch. When this element is enabled by the control light it reduces the bias across the switch to a voltage lower than the holding voltage (V_H), thus the switch turns off. Without the control light, the switch functions normally. Matsuda et al. [3] has reported an all-optical bistable switch with set/reset light pulses using a shunting HPT to control the optical bistable switch.

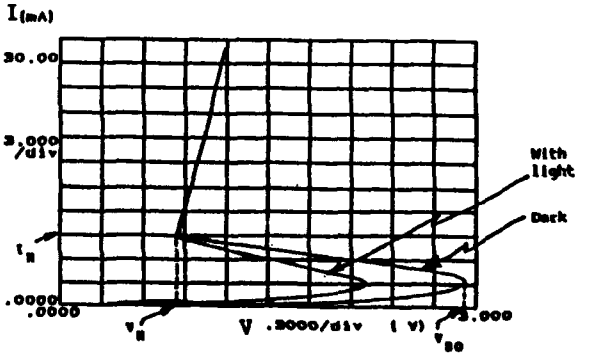


Figure 1. I-V Characteristics of a Light Amplifying Optical Switch (LAOS)

We have utilized a similar HPT shunting a LAOS device configuration but have set the bias above the break-over voltage (V_{BO} in Fig.1). In this way an optical inverter, with memory, has been demonstrated [4]. We have also demonstrated optical OR and NOR gates using a set of parallel-connected HPTs shunting the LAOS device [5].

The second technique of controlling the bistable switch with light (series type) places the optically sensitive control element in series with the switch so that the current passing through the switch device can be optically controlled. In this case, the switch functions normally while the element is kept on by the control light. When the control light is off, the current through the switch is reduced below the holding current and the switch is turned off.

It is appropriate that the light sensitive element has a comparable layer structure to the bistable switch, so that monolithic integration of the control element with the switch is realizable. The HPT is a good candidate for the control element of the LAOS device, since an HPT is part of the LAOS and thus readily available on the same chip.

This paper presents the realization of two series types of light controllable optical bistable switches as described above. We have demonstrated experimentally that this device functions as both an optical latch and a logic AND gate, depending upon the electrical bias conditions.

II. Device Structure and Fabrication

The optical latch and AND gate are formed by series connecting an HPT and a LAOS device. The LAOS is a series connection of an HPT and a double heterojunction LED, which has positive electrical and optical feedback that causes switching from a low current state to a high current state through a negative differential resistance region as shown in Fig. 1. The structure and the equivalent circuit of the optical latch and the optical AND gate are shown in Fig. 2. The HPT serves to gate the electrical power to the LAOS and thus it turns the LAOS on and off (or prevents it from turning on). The HPT is activated by a control light signal and thus all-optical bistable switching is realized. The structure consists of two parallel integrated mesas: the LAOS device and the control HPT. The epitaxial layers for these devices were grown on a semi-insulating InP substrate using gas-source molecular beam epitaxy (GSMBE). The layers were grown in the following order: a p-InGaAs stop etch layer (0.002 μm, 1 x 18^{18} cm^{-3}), a p-InP buffer layer (0.5 μm, 2 x 10^{18} cm^{-3}), a p-InGaAs bottom contact layer (0.05 μm, 1 x 10^{18} cm^{-3}), a p-InP cladding layer (0.5 μm, 2 x 10^{18} cm^{-3}), an undoped InGaAs active layer (0.2 μm), an n-InP cladding layer (0.1 μm, 2 x 10^{18} cm^{-3}), an n-InGaAs feedback control layer (0.1 μm, 1 x 10^{18} cm^{-3}), an n-InP feedback control layer (0.1 μm, 2 x 10^{18} cm^{-3}), an n-InGaAs collector (1.5 μm, 2 x 10^{16} cm^{-3}), a p-InGaAs base (0.1 μm, 1 x 10^{18} cm^{-3}), an

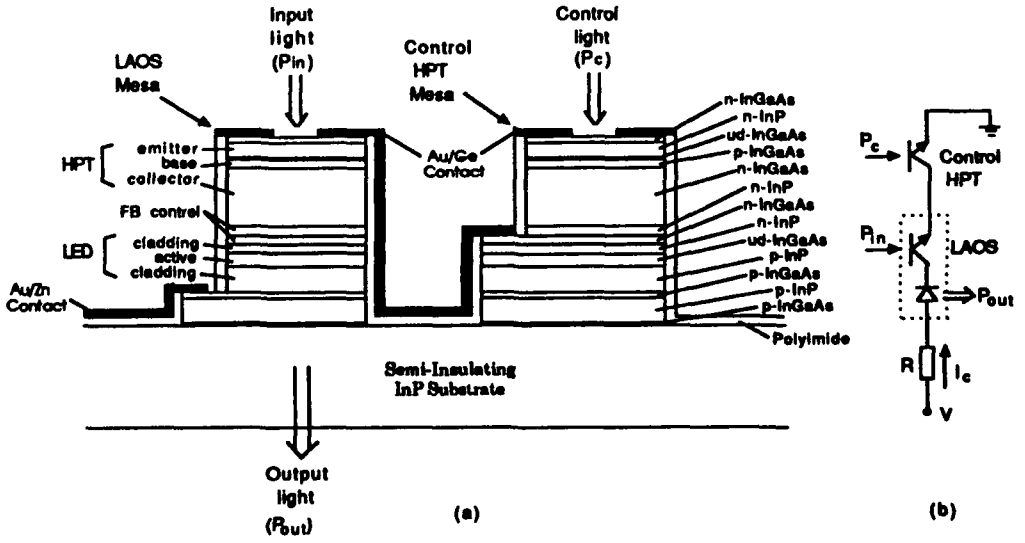


Fig. 2 Schematic cross section and the equivalent circuit of the integrated optical latch and optical AND gate

undoped InGaAs set-back layer (0.01 μm), a p-InP emitter (0.2 μm, 5 x 10^{17} cm^{-3}), an n-InGaAs top contact layer (0.05 μm, 5 x 10^{19} cm^{-3}). The LAOS mesa utilizes all of these layers and the control HPT consists of only the top five layers of another mesa (the lower potion of that mesa is electrically bypassed). Therefore only one MBE growth sequence is required. The mesas were etched into squares of about 380 μm on a side. The n-type emitter and collector contacts were fabricated by the lift-off of evaporated Ge/Au/Ni while the p-type bottom contacts were fabricated by the lift-off of evaporated Au/Zn/Au.

III. Experimental Results

The devices were tested on a probe station and probed with micromanipulators. The incandescent lights from the microscope illuminator and a fiber illuminator were used as the input and control signals, respectively. The I-V curves were measured using a semiconductor parameter analyzer. The common emitter current gain of a typical HPT was found to have a maximum of approximately 75 at a collector current of 10 mA and a dark avalanche breakdown voltage (BV_{CE0}) of about 5 V.

The experimental results of the optical latch are shown in Fig. 3(d). The electrical bias to the latch was set at 4.5 V, which supplies the LAOS device with a voltage below but near the break-over voltage (V_{BO}) so that the LAOS can be operated as a bistable optical switch. This means that an input light signal can switch the LAOS "on" and it stays on after the input light signal is no longer present. Figure 3 shows that the input light signal has no effect on the device current, unless the HPT is turned on by the control light. It is also shown that an input light signal turns the LAOS on and it stays on until the HPT is turned off. As a result, optical latching is enabled/disabled by the control light through the HPT. Thus, the functionality of the optical latch has been demonstrated. The speed of operation and the input/output power have not been measured. However, it is expected that the speed of the device is determined by the delay time of the HPT, which should be on the order of 10 ns.

The optical AND gate has been demonstrated, using an external HPT component connected in series with the LAOS device and using the input port of the LAOS as input A, and the control HPT input as input B. The AND gate was biased at a voltage of 2 V, which is larger than V_B so that the I-V curves of HPT and LAOS cross each other to form operating points; but

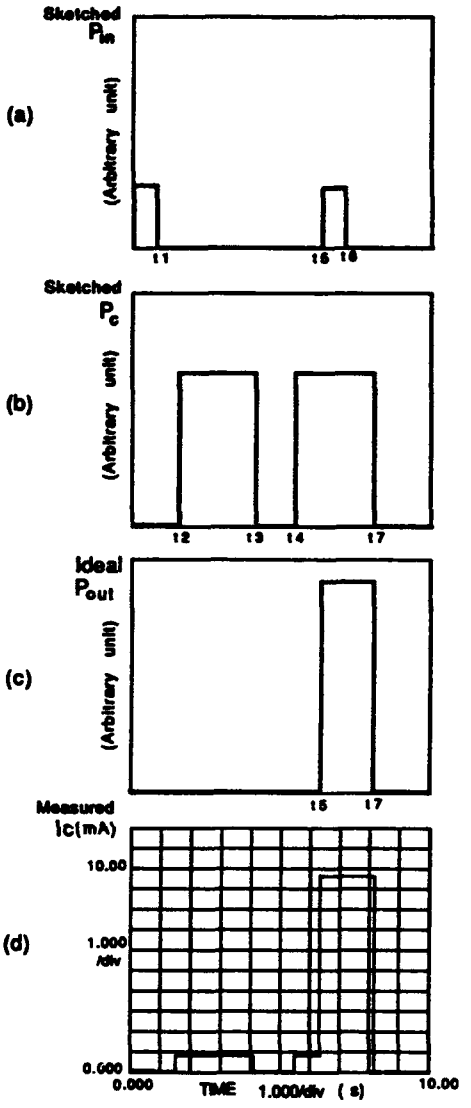


Fig. 3 Experimental demonstration of the optical latch operation with (a) input light, (b) control light, (c) ideal output, (d) measured output waveform of device current (I_C), using an integrated HPT connected in series with the LAOS device

small enough to prevent the gate from latching. When either input is not present there is no current flows in the circuit, the gate is in the off-state. When the light of either input A or input B is incident on the LAOS or the HPT, respectively, the existing current is the dark current of the LAOS or that of HPT. Thus, the gate is still in the off-state. When both lights of input A and input B are present, sufficient current will flow in the gate circuit to give an on-state. The results are shown in Fig. 4.

IV. Device Improvement

The present integrated device is not

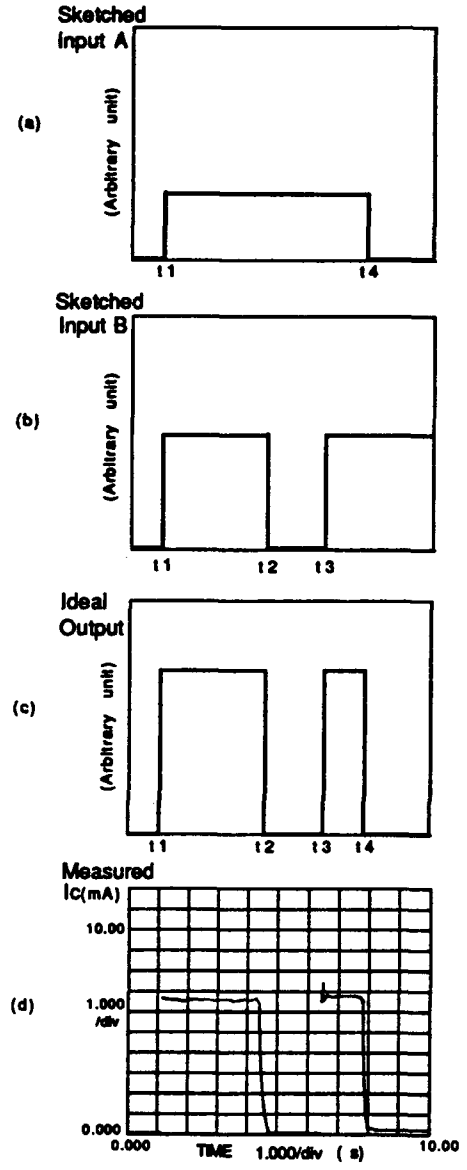


Fig. 4 Experimental demonstration of the optical AND gate operation with (a) input A, (b) input B, (c) ideal output, and (d) measured output waveform of device current (I_c), using an external HPT connected in series with the LAOS device

suitable for forming large arrays which are useful in optical parallel processing, due to the problem associated with the alignment of two different input light signals. Thus, we are designing a vertical integration of the gate HPT with the LAOS device in order to form a stacked pixel of an optical latch or AND gate, as shown in Fig. 5. This type of structure requires using different wavelengths for the control and input signals and has the advantage of getting rid of external contacts between the mesas, increasing the device density and providing increased flexibility in forming some types of array structures.

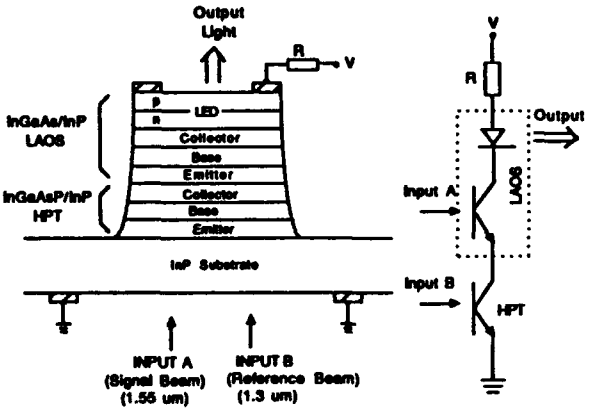


Fig. 5 Schematic cross section and equivalent circuit of an optical AND pixel

Acknowledgments

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Optical Bistable Arrays: Prospects for Ultimate Performances

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ABSTRACT

A theoretical analysis of the optimum operating characteristics of a GaAs/GaAlAs non linear Fabry-Pérot étalon is presented. Both the impedance matching conditions between the front and back mirror reflectivities and the obtention of a minimum critical threshold intensity are merged into a simple relation involving the cavity parameters and the active layer material characteristics. Submilliwatt threshold powers are predicted by this optimization. A further reduction by more than one order of magnitude is expected when extending the optimization to laterally restricted microresonators which leads also to an optimum pixel size.

INTRODUCTION

Epitaxial Fabry-Perot cavities including III-V non linear active media and integrated Bragg reflectors already show much flexibility in their design since the finesse (and hence the bistability threshold) depends on the product of the two mirror reflectivities, while the switching contrast depends on their ratio. For an arbitrary set of cavity parameters there is an optimum absorption coefficient α that minimizes the threshold while another optimum value is required for optimizing the reflective contrast ratio. The cavity design can be made even more flexible if one includes α among the adjustable parameters, which can be achieved by tuning the temperature or adjusting the cavity resonance and the operating wavelength accordingly.

We demonstrate here that the simultaneous optimization of both the contrast and the minimum threshold intensity in the presence of a saturating dispersive non linearity can be formulated in the form of simple expressions which can be set in terms of design rules for the cavity parameters. Prospective arguments are finally given for further improvements in pixellated structures.

SIMULTANEOUS OPTIMIZATION OF CONTRAST AND THRESHOLD

In a Fabry-Perot étalon with front and back reflectivities R_f and R_b respectively the impedance matching condition for optimum contrast at resonance is given by:

$$R_f = R_b e^{-2\alpha D}$$

where D is the nonlinear medium thickness. The common parameters and relations describing the behavior of a non linear Fabry-Perot étalon are recalled in table 1.

Assuming for the moment a non linear index change of the form $\delta_{NL} = n_2 I$, enhanced by carrier generation, it has been shown[1] that n_2 is proportional to α. This helps defining a new parameter[2]:

$$I_b = \frac{\alpha\lambda}{2\pi\,|\,n_2\,|}$$

$$\frac{I_{cav}}{I_{incident}} = K\frac{1}{1+F(\phi-\phi_0)^2}$$

$$R_a = (R_f R_b)^{1/2} e^{-\alpha D}$$

$$K = \frac{(1-R_f)(1+R_b e^{-\alpha D})(1-e^{-\alpha D})}{(1-R_a)^2 \alpha D} \approx \frac{F(1-R_f)}{2}$$

$$F = \frac{4R_a}{(1-R_a)^2}$$

$$\mathcal{F} = \frac{\pi}{2}F^{1/2}$$

***Table 1:** Common parameters and relations used throughout this paper in the high finesse limit ($\mathcal{F} \gg 1$). ϕ is the single pass phase shift and ϕ_0 the initial dephasing.*

which scales the intensities for the dispersive non linearities.

Using the notation and expressions of [3], in the high finesse limit, the critical intensity for the onset of bistability is simply expressed as

$$I_c = \frac{2\sqrt{3}\left(\alpha D + \frac{1}{2}(\tau_f + \tau_b)\right)^3}{9\,\tau_f \alpha D} I_b$$

where $\tau_f = 1 - R_f$ and $\tau_b = 1 - R_b$ are the front and back mirror losses respectively. If α is now considered as an adjustable parameter, it is straightforward to minimize the critical intensity with

$$(\alpha D)_{opt} = \frac{\tau_f + \tau_b}{4}$$

leading to the following expression:

$$(I_c)_{opt} = \frac{3\sqrt{3}}{8} I_b \frac{(\tau_f + \tau_b)^2}{\tau_f}$$

Here the sum of the mirror losses is considered as constant. On the other hand, in the high finesse limit, the impedance matching condition can be expressed as

$$\tau_f - \tau_b = 2\alpha D$$

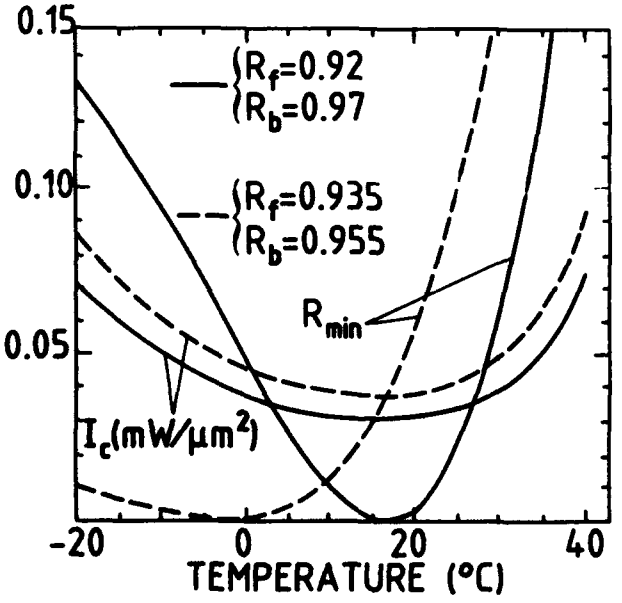


Fig.1: Optimization conditions of both the minimum reflectivity and the minimum threshold power with the absorption, through temperature for two sets of mirror reflectivities. Simultaneous optimization can be met for a proper adjustment of these parameters.

Therefore if we combine these two conditions, the simultaneous optimization can be expressed in a very simple form

$$\frac{\tau_f}{3} = \tau_b = \alpha D$$

which leads to a minimum threshold intensity

$$(I_c)_{opt} = 2\sqrt{3} I_b \tau_b$$

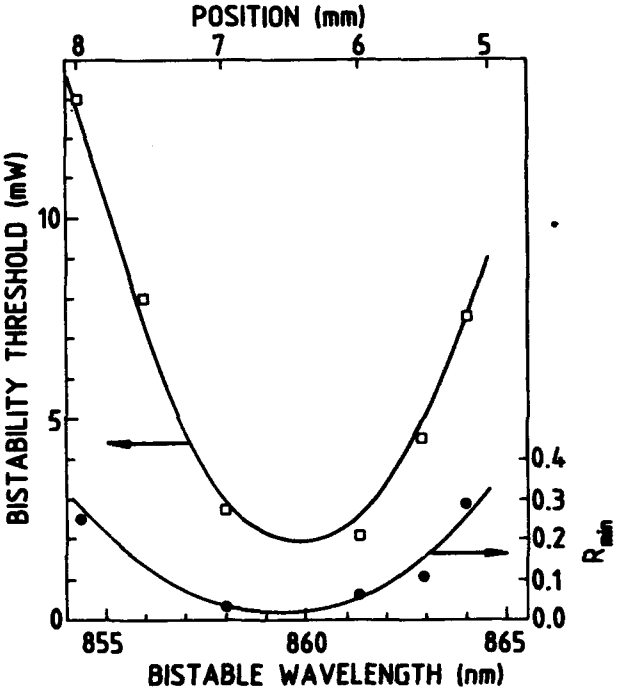


Fig.2: Simultaneous optimization of the reflective contrast ratio and minimum threshold power obtained by tuning the cavity resonance through a MBE-grown sample thickness gradient. The étalon was excited by a 6 μm diameter light spot.

Note that a single degree of freedom is left in the adjustment of all the parameters needed for optimizing simultaneously the reflective contrast and the threshold intensity. In fig.1 are sketched both the threshold intensity and reflectivity minimum as a function of the overall absorption via temperature tuning for two different sets of mirror reflectivities. Simultaneous optimization can be met for a proper adjustment of these parameters according to the above mentionned equations. This has been also observed on a MBE-grown sample (fig.2) including 130 periods of a 10 nm barrier and 10 nm well GaAs/$Ga_{0.5}Al_{0.5}As$ MQW active layer with respectively 91.7% and 97% reflectivity mirrors, where the absorption is tuned by moving the operating point on the sample, through thickness non uniformities.

THRESHOLD MINIMIZATION IN THE PRESENCE OF SATURATION

The saturation behaviour of the dispersive non linearity can be accurately described by a classical saturation law of the non linear contribution to the round-trip phase $\delta(I)$:

$$\delta(I) = \delta_s \frac{I/I_s}{1+I/I_s}$$

where I_s is a saturation intensity and δ_s is the maximum phase shift which corresponds to a maximum possible index change δn_s such that

$$\delta_s = \frac{2\pi D}{\lambda}\delta n_s$$

We define a critical finesse[4]

$$\mathcal{F}_c = \frac{2\pi}{\delta_s} = \frac{\lambda}{\pi \delta n_s D}$$

below which bistability cannot be obtained. In the high finesse limit and with optimized conditions fulfilled the finesse becomes

$$\mathcal{F} = \frac{\pi}{3\alpha D}$$

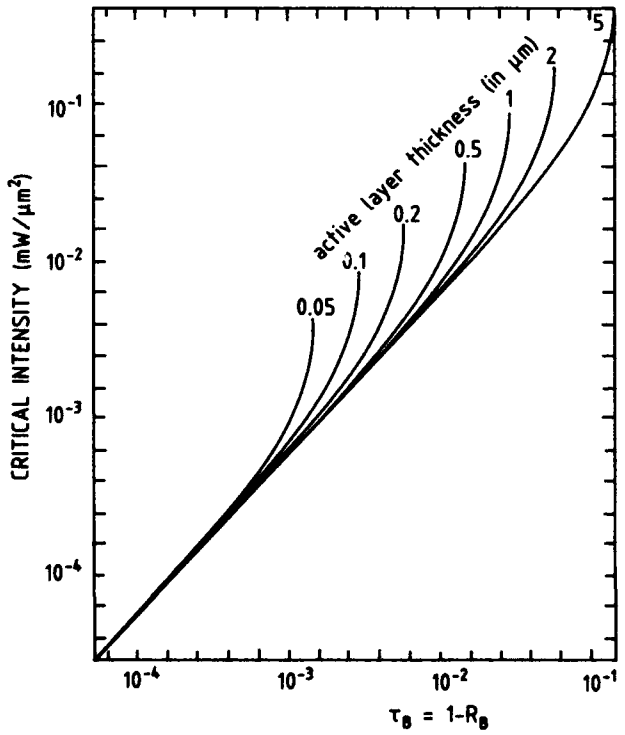


Fig.3: Plot of the critical intensity as a function of the only adjustable parameter τ_b of an optimized cavity, for various active layer thicknesses. The effect of the dispersive saturation becomes sizeable as the cavity finesse approches the critical finesse. The parameters used in the calculation are $\delta n_s = 2.4\ 10^{-2}$, $\lambda = 0.84\mu m$ and $\alpha I_s = 2.86\ 10^5 W/cm^3$

$$F = \left(\frac{2}{3\alpha D}\right)^2$$

and

$$K = \frac{3F\tau_b}{2}$$

At low intensities $I \ll I_s$, $\delta n = n_2 I$ with $n_2 = \frac{\delta n_s}{I_s}$: the usual property n_2/α = Constant becomes αI_s = Constant. This was checked by our experimental results[5]. From [6], the critical initial detuning from resonance Φ_{oc} is a solution of

$$\delta_s = \frac{8}{9}\Phi_{oc}\frac{F\Phi_{oc}^2/3}{F\Phi_{oc}^2/3 - 1}$$

and the critical incident intensity writes

$$I_{oc} = \frac{I_s}{3K}(F\Phi_{oc}^2 - 3)$$

which accounting for the optimum conditions ($\alpha D = \tau_b$) becomes

$$I_{oc} = (\alpha I_s)D\frac{(F\Phi_{oc}^2 - 3)}{2}$$

For a given active layer thickness, we can express the dependance of I_{oc} on the optimization parameter τ_b by reexpressing Φ_{oc} and F in terms of τ_b, in the functional form

$$I_{oc} = f_D(\tau_b)$$

The calculation is performed through parametric relations assuming $x = \sqrt{F}\,\Phi_{oc}$ and $y = \sqrt{F}\,\delta_s$. From the expression of δ_s it comes $y = 8x^3/9(x^2 - 3)$. The results can be seen on fig 3. As long as the finesse remains high, the active layer is far from saturation and the threshold intensity is proportional to the absorption. The effects of saturation become sizeable when $\mathcal{F}$ gets closer to $\mathcal{F}_c$ through the increase of τ_b. In this region the threshold intensity increases very rapidly. The curves stop at $\mathcal{F} = \mathcal{F}_c$.

IMPLICATION ON THE GEOMETRICAL DESIGN OF BISTABLE CAVITIES

From the previous expressions we can express simple formula for the design of an optimized cavity including a dispersive saturating active medium for a given reduced finesse f defined as

$$f=\frac{\mathcal{F}}{\mathcal{F}_c}$$

and express the length of the various components of the cavity i.e. the active layer thickness D and the mirror thicknesses D_f and D_b in terms of the number of periods N_f and N_b. The reduced finesse f in the optimized conditions becomes

$$f=\frac{\pi\delta n_s}{3\alpha\lambda}$$

Therefore for a desired factor f, α must match

$$\alpha=\frac{\pi\delta n_s}{3f\lambda}$$

From it we deduce the active layer thickness requirement

$$D=\frac{\tau_b}{\alpha}=6f\tau_b D_s$$

where

$$D_s=\frac{\lambda}{2\pi\delta n_s}$$

The mirror thicknesses D_f and D_b can be calculated as a function of τ_b. The transmission coefficients at Bragg conditions write[7]:

$$\tau_b=\frac{4n_a}{n_s}\left(\frac{n_L}{n_H}\right)^{2N_b}$$

$$\tau_f=\frac{4n_{air}}{n_a}\left(\frac{n_L}{n_H}\right)^{2N_f}$$

where n_a is the active layer index, n_s the substrate index, n_H the higher index and n_L the lower index in Bragg mirrors. The optimized conditions lead to

$$N_b-N_f=\frac{\ln\left(\frac{n_s}{3n_a^2}\right)}{2\ln\left(\frac{n_L}{n_H}\right)}$$

An optimized structure has therefore a fixed difference between the number of periods in each mirror and $N_b-N_f=7$ for the parameters of fig.4. Finally if p is the period of the Bragg mirrors, their total length derives from the preceeding expressions:

$$D_f+D_b=\frac{p}{2\ln\left(\frac{n_H}{n_L}\right)}\left(2\ln\left(\frac{4}{\tau_b}\right)-\ln\left(\frac{3n_a^2}{n_s}\right)\right)$$

The overall length L can be expressed as a function of the sole τ_b

$$L=6f\tau_b D_s+\frac{p}{2\ln\left(\frac{n_H}{n_L}\right)}\left(2\ln\left(\frac{4}{\tau_b}\right)-\ln\left(\frac{3n_a^2}{n_s}\right)\right)$$

or as a function of N_b as well, through their mutual relation. This is graphically sketched on fig.4 where a straightforward correspondance is made between τ_b and the number of periods N_b in the back mirror, thus providing a simple rule for the cavity design. Very low thresholds are expected with ultrashort active layers and high finesse cavities. As the finesse increases exponentially with the number of periods in a Bragg reflector, still modest overall resonator thicknesses are required.

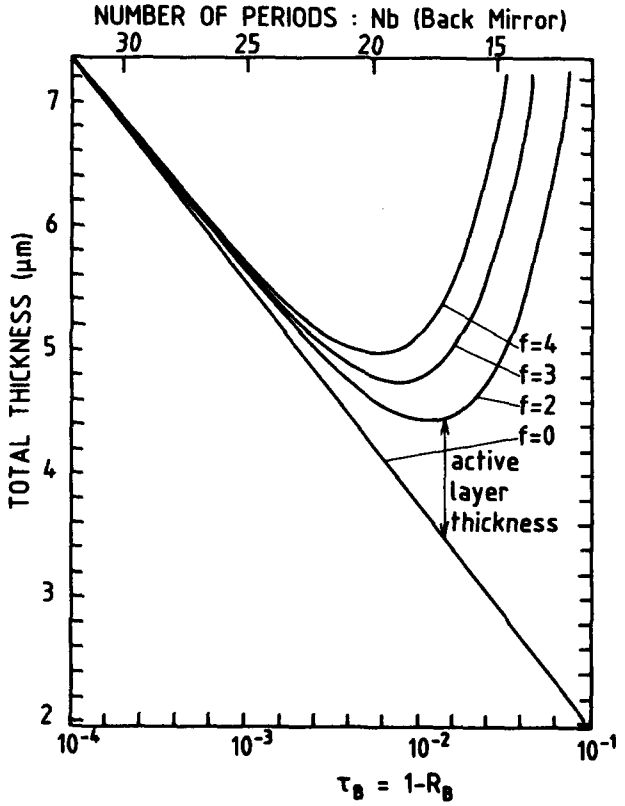


Fig.4: *Overall thickness of a Fabry-Perot structure as a function of the optimization parameter τ_b for various values of the reduced finesse. The case $f=0$ gives the thickness of the mirror stacks. The minimum thickness is situated between 4 and 5 μm. The parameters used in he calculation are $\delta n_s=2.4\ 10^{-2}$, $n_a=3.5$, $n_s=3.6$, $n_H=3.52$, $n_L=3.0$, $\lambda=0.84\mu m$. This leads to $N_b-N_f=7$*

PROSPECTS FOR ULTIMATE PERFORMANCE ON BISTABLE ARRAYS

A further reduction in the threshold intensities may be expected from the reduction of the excited region through pixellation with a scaling factor proportional to the pixel area. The validity of this assessment is limited by diffraction with a minimum area of the order of $(\lambda/n)^2$ and by the decrease of the confinement factor which reduces the excitation efficiency and lowers the finesse. Within this frame a reduction of about two orders of magnitude of the threshold and switching energy can be expected from miniaturization down to the diffraction limit. Prospective values can be deduced on the basis of actual typical performances[8] and lead to switching powers in the microwatt range and switching energies of the order of a few tens of femtojoules.

CONCLUSION

We have shown that nonlinear integrated Fabry-Perot resonators show some flexibility for the simultaneous optimization of both the reflective contrast ratio and the critical intensity. The saturation properties of the dispersive nonlinearity have been included in the analysis and lead to simple criteria in terms of the cavity parameters. When going down to wavelength-size excited areas in pixellated structures a reduction by two orders of magnitude is expected before the effects of diffraction become dominant.

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92-17299

Bistable Diode Laser Amplifiers Used as Optical Repeaters or High-Sensitivity Clock-Synchronized Receivers

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Abstract

We present some experimental studies of the sensitivity of a GaAs/AlGaAs DH bistable diode laser amplifier (BDLA) when used as an optical repeater or as a high sensitivity clock synchronized optical receiver. Sensitivity of -34 dBm and -40.5 dBm have been measured, respectively. The optical bistability of interest is based on an intensity induced change of refractive index. A large usable optical gain is also measured in these experiments.

Introduction

Bistable semiconductor diode laser amplifiers are interesting because of their potential applications in future photonic switching systems, including optical thresholding, optical logic, digital signal processing and optical computing[1-5]. In particular, they will find applications in optical routing of high data rate optical signals in a network, high speed optical interconnects and wavelength division switching systems[6]. Bistable semiconductor diode laser

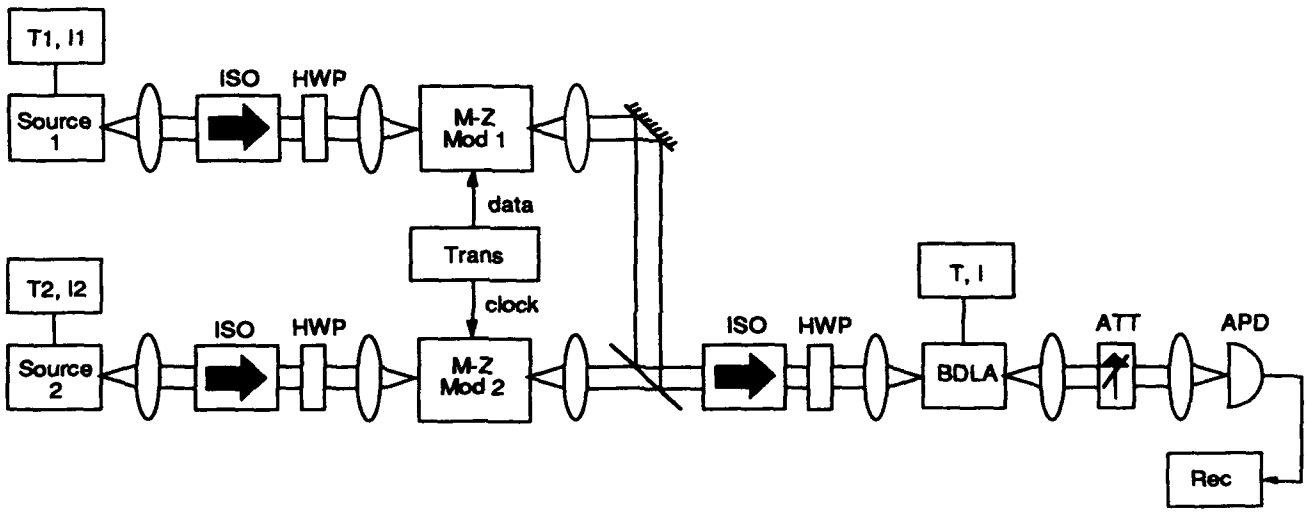


Figure 1. Experimental setup to study the sensitivity of the bistable diode laser amplifier as an optical repeater

[Source : semiconductor source laser. T,I: temperature and current injection control. ISO: optical isolator. HWP: half-wave plate. M-Z mod: Mach-Zehnder modulator. Trans: transmitter. BDLA: bistable diode laser amplifier. ATT: variable attenuator. APD: avalanche photodiode. Rec: receiver.]

amplifiers (dispersive type) are also the most efficient photonic switches in terms of switching energy per unit gain[1]. In this paper, we study the sensitivity of a bistable semiconductor diode laser amplifier when used as an optical regenerator and when used as a high sensitivity clock synchronized optical receiver.

Experimental clock synchronized results and discussion

Optical bistability based on the intensity induced change of refractive index can be observed with the most common type of Fabry-Perot semiconductor lasers operated slightly below the lasing threshold. When a sufficient amount of light is coupled into a Fabry-Perot semiconductor laser biased just below threshold, the carrier density inside the active region will be decreased due to stimulated emission. As a consequence of this, the index of refraction in the active region will increase and may result in optical bistability if the wavelength of the injected light is properly tuned to the long wavelength side of one of the Fabry-Perot resonances of the laser amplifier.

In our experiments, two GaAs/AlGaAs DH lasers (Hitachi HLP1400) operated well above threshold were used as sources to provide two single-wavelength beams. One beam (clock beam) was modulated by a Mach-Zehnder modulator at a clock rate of 140 MHz, the other (data beam) by another Mach-Zehnder modulator with a 140 Mbit/s, 2^{10}-1 bit, return-to-zero data pattern. The clock beam was tuned by temperature and current injection to the long wavelength side of one of the Fabry-Perot resonances of the bistable amplifier. The detuning was about 0.35 Å (the spacing between two adjacent Fabry-Perot peaks is 2.85 Å or 124 GHz). The wavelength of the data beam was tuned close to another Fabry-Perot resonance. The timing was adjusted such that the data slightly leads, or is in synchronism with, the clock at the input of the bistable diode laser amplifier. The optical signal power in the clock beam was adjusted to be just below the switch-up point of the hysteresis loop in the output vs. input relationship of the bistable diode laser amplifier. Hence, the bistable amplifier will switch up whenever there is a "1" in the data beam and remains high through the clock pulse duration.

In the first experiment, the sensitivity of a bistable diode laser amplifier used as an optical repeater was measured. The schematic of the experimental setup is shown in figure 1. The bistable laser diode that was used in the experiment was the same type of laser as the sources except that it was biased just below threshold. Because of the detuning dependence of the switching power[7], both the source lasers and the bistable amplifier were temperature stabilized by Peltier TE coolers. The power in the data beam was adjusted so that the bistable diode laser amplifier was well switched. The output

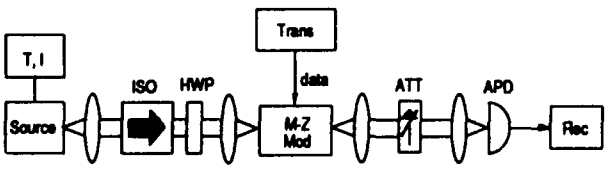


Figure 2. Calibration of APD

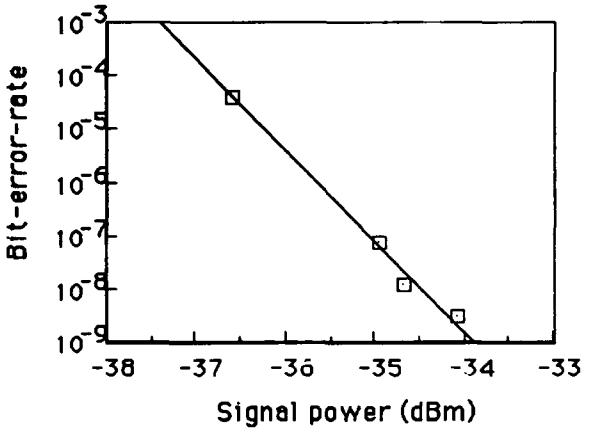


Figure 3. Sensitivity of BDLA as an optical repeater

from the bistable amplifier was progressively attenuated and detected by an avalanche photodiode (APD), the sensitivity of which was calibrated to be -40 dBm (figure 2). This -40 dBm sensitivity limit, measured at 140 Mbit/s, is a convolution of the noise from the incident laser source and the APD itself. Bit-error-rate measurements were then performed on the most intense beam going through the bistable diode laser amplifier. Figure 3 shows the experimental results. A sensitivity of -34 dBm at a bit-error-rate of 10^{-9} was measured. ON/OFF ratio of the output signal was 4.5:1. An usable gain,

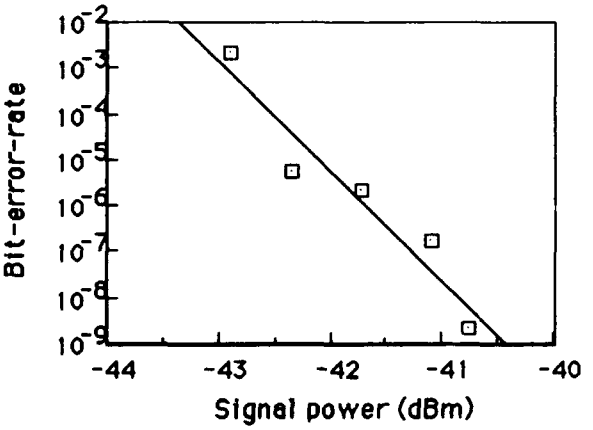


Figure 4. Sensitivity of BDLA as a clock synchronized optical receiver

which is defined as the ratio of the signal power at the output to the signal power in the data beam at the input after coupling losses, of 24 dB was also measured. It should be emphasized that this gain is greater by almost 10 dB when compared to the typical fiber-to-fiber gain of a traveling-wave semiconductor laser amplifier. These results indicate the potential of a bistable diode laser amplifier being used as an optical repeater in a communication link or as a signal booster in a distributed network to reamplify the optical signal when it drops below 500 nW. Since a bistable diode laser amplifier is a digital amplifier, it is expected that the noise characteristics will be better, as compared to a linear amplifier such as the traveling-wave amplifier. In addition, it should be stressed that the optically regenerated signal is clock synchronized with the clock signal.

In the second set of experiments, the sensitivity of the bistable diode laser amplifier used as a high sensitivity clock synchronized optical receiver was measured. The experimental setup was similar to that shown in figure 1, except that the variable attenuator was used here to progressively attenuate the data beam before going through the bistable diode laser amplifier. Bit-error-rate measurements were performed on the output data from the bistable amplifier (at the clock wavelength). The coupling loss was determined by comparing the measured small signal gain of the bistable amplifier to the theoretical value, and was found to be 7.3 dB. Figure 4 shows the experimental results. A sensitivity of -40.5 dBm in the coupled power was measured. This corresponds to about 5,000 photons per bit. It should be emphasized that this number should not be compared with the theoretical detection limit of 38 photons per bit in an ASK direct detection receiver with an optical amplifier [8]. Here, at the signal power level of 5,000 photons per bit, the device can switch, the data can be recovered in synchronism with the clock, and logic functions can be performed.

The wavelengths of the two source lasers used in the experiments are about 6 mode spacings apart. One is 3 mode spacings away from the maximum Fabry-Perot resonance of the bistable diode laser amplifier to the long wavelength side, the other is 3 mode spacings away from the maximum to the short wavelength side. In practice, the two source lasers can be tuned close to any two Fabry-Perot resonances as long as they are not too far away from the maximum peak. It is noticed that the optical detuning of the data beam to have maximum sensitivity was about 0.1 Å, which is about the minimum detuning for the bistable amplifier to show nonlinearities. This can be easily understood because the power in the clock beam was just below the value at which it can switch the amplifier by itself at the particular clock detuning, namely, 0.35 Å in this case. It should also be noticed that the recovered signal at the output is at the clock wavelength. Thus, the above experiment can be seen from a different perspective: the clock beam is being controlled by a weak data beam through the bistable amplifier. It is interesting to realize that with 5,000 photons per bit, an optical signal at a certain wavelength can control a much stronger optical signal at a wavelength corresponding to many mode spacings away.

Summary

We have studied the sensitivity of a bistable semiconductor diode laser amplifier when used as an optical repeater and when used as a high sensitivity clock synchronized optical receiver. The results indicate the potential of bistable diode laser amplifiers to be used in communication and photonic switching systems. Bistable diode laser amplifiers are very efficient, relatively low noise, high gain, optical switches.

We are pleased to acknowledge the financial support from NSF (contract number: ECS-8818797) and DARPA (contract noumber: DAAH01-89-C-0067).

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92-17300

Surface-Emitting Laser Logic

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ABSTRACT

We describe a new class of optical logic devices which consist of integrated phototransistors and surface-emitting lasers. The devices function as optical neurons having high gain and, as arrays, are ideal for neural networks, parallel optical signal processing and optical computing applications.

Here we describe our efforts to build an ideal optical switch based on the monolithic integration of a heterojunction phototransistor (HPT) with a vertical-cavity surface-emitting laser (VCSEL) diode. To date we have demonstrated high optical gain (> 20 overall, > 200 differential) with the discrete components connected in series. Our devices are ideally suited for parallel optical signal processing which is currently regarded as the most promising research area for achieving significant increases in computational throughput relative to purely electronic based information processing. Parallel optical processing has been severely hampered by the lack of several basic "building block" devices such as optical switching devices that exhibit low-switching energy, high optical gain (fan-out capability) and high contrast. Devices should be: easy to fabricate (use of self-aligned VLSI technology), microscopic in size, and readily integrable with other optoelectronic components without being adversely affected by external optical feedback.

Our basic "unit cell", which we call a surfaCe-Emitting Laser Logic (CELL) device, consists of two components, a photodetector with electrical gain and a low-threshold VCSEL. While each of these components has been demonstrated in prior work [1-2], we describe properly scaled, integrable, proton implanted, optimized versions of HPT and VCSEL components and hybrid operation of the pair. In the basic operation of the device, incident light generates photocurrent in the detector element which is internally amplified and then used to drive the laser element above threshold. This optical-electrical-optical conversion is the basis upon which the device achieves insensitivity to external optical feedback (optical feedback to the VCSEL will not affect the input to the HPT). The devices are ideal for high-density, 2-D arrays which convert images from one wavelength to another or from incoherent to coherent light. The CELL also has an important advantage over photothyristors devices; whereas these devices are latching and need to be reset electrically, the CELL does not. Each CELL acts as an independent thresholding optical amplifier. Ultimately our goal is to monolithically integrate the HPT with the VCSEL (see Fig. 1) and then fabricate them into 2-D arrays. Since both the input and output images are directed perpendicular to the arrays, CELLs will be useful for parallel signal processing, multichannel interconnections, neural networks and visual displays. CELLs can also be configured as latching devices, in which case they would function as image memories capable of capturing and storing a 2-D image until the array is reset.

In order to achieve a high-gain optical device that is cascadable and insensitive to feedback, we use the light actuated current switching capability of a high-gain AlGaAs/GaAs HPT and a low-threshold, high-power AlGaAs/GaAs VCSEL. The n-p-n HPT, grown by MBE, consists of a wide-band-gap ($Al_{0.35}Ga_{0.65}As$) emitter and narrow-band-gap (GaAs) base and collector regions. The wide-band-gap emitter inhibits the base-to-emitter hole injection current and significantly increases the HPT gain. We electrically isolated the HPTs using shallow proton implants. We employ a bi-layer structure consisting of a layer of electroplated gold covering a layer of photoresist as an ion blocking mask and also as a mask to form self-aligned electrical contacts. The input clear apertures of the HPTs are 15 μm and the implant mask diameters are 50 μm. The phototransistor common-emitter, floating-base characteristic exhibits 10 mA photogenerated current for 120 μW of absorbed light power (176 μW incident) at 800 nm. We measured the frequency response of the implanted HPT using a sync-pumped dye laser and found it to be > 200 MHz (limited by the bandwidth of the measurement system). The MBE grown VCSELs consist of a 19 period p-type distributed Bragg reflector (DBR), a four quantum-well (100 Å) active region and a 27.5 period n-type DBR. We electrically isolated the VCSELs in a manner similar to that used for the HPTs by using deep-proton implants [2]

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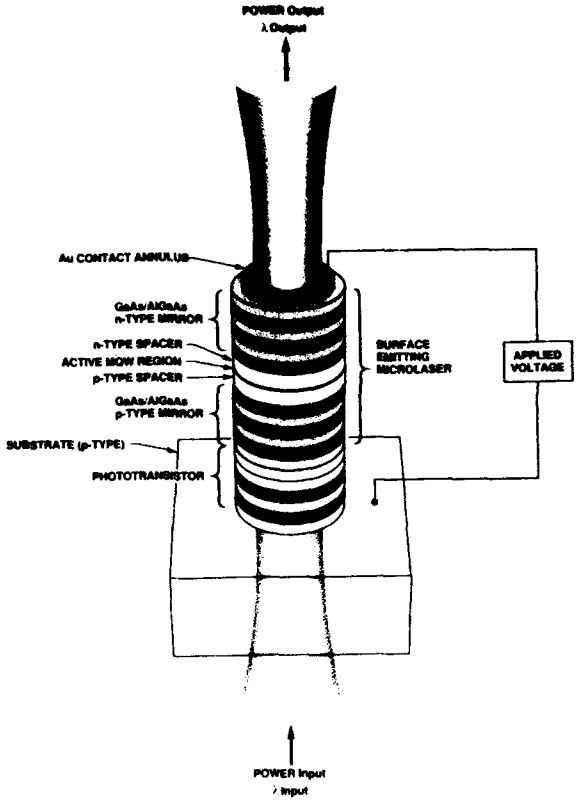


Figure 1. Illustration of a surfaCe-Emitting Laser Logic (CELL) device in one of its possible configurations.

with 15-μm-diameter implant masks and self-aligned contacts. Implants result in funneling of the injected current into the VCSEL diode. The CW room-temperature laser diode L-I characteristic exhibits 2.5 mW laser-light output power at 850 nm for 10-mA injection current.

In Fig. 2 we show the calculated energy diagram of a CELL and the equivalent circuit of the integrated structure. R_n and R_p refer to the series resistance of the n-type and p-type mirrors, respectively. R_p dominates the series resistance of the VCSEL resulting in non-ideal laser diode behavior. The large R_p is due to voltage spikes at the AlAs/AlGaAs valence-band interfaces arising from equilibrium charge transfer which are apparent in the energy diagram shown in Fig. 2a. In practice we incorporate ~100-Å-thick $Al_{0.58}Ga_{0.42}As$ steps at each interface of the p-type DBR to reduce this resistance to a level on the order of the n-type mirror.

In Fig. 3 we show the VCSEL diode output power as a function of the input power to the HPT for the pair connected in series as shown in Fig. 2b with an 8.0 V bias. The CELL has both high overall optical gain (> 20 at peak) and high differential optical gain (> 200 at peak). The threshold switching power for the device is 40 μW input power and unity gain occurs at 75 μW input power. The output power from the CELL saturated at 2800 μW for input powers greater than 140 μW. The on (above threshold)/off (below threshold) contrast of the CELL is 2780, (40 μW input produced 0.9 μW output and 120 μW input produced 2500 μW output). We have also converted 680-870 nm input light to

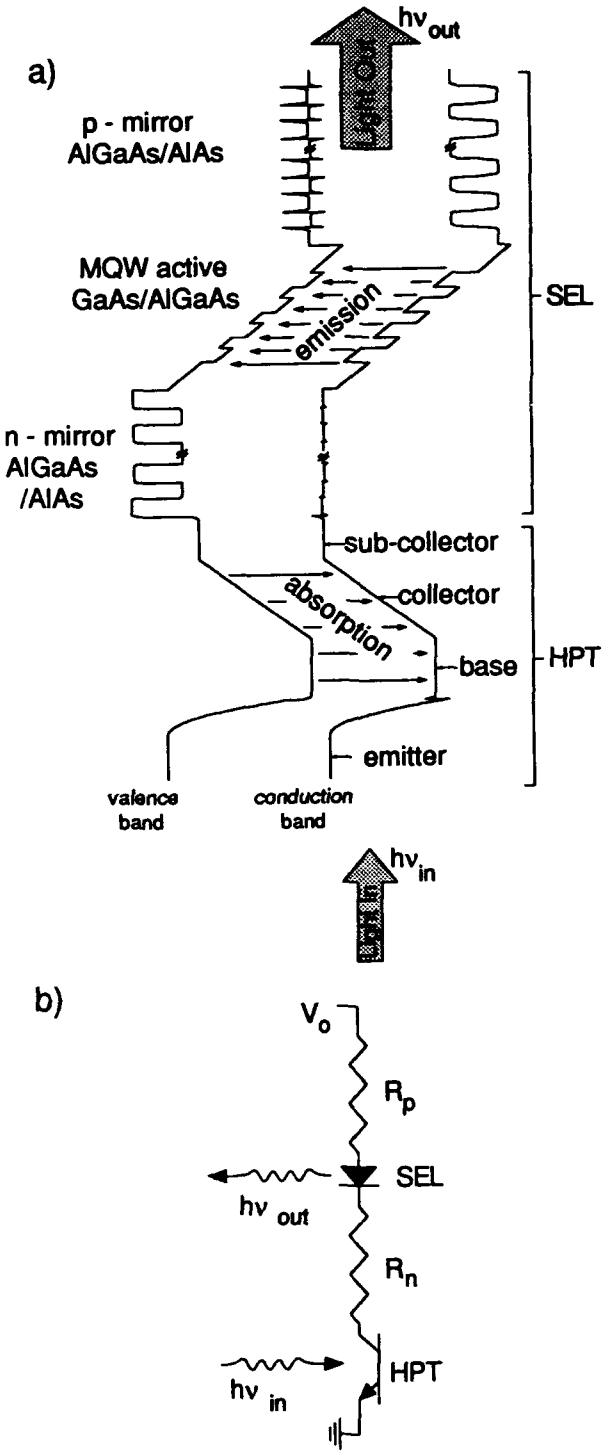


Figure 2. a) Calculated energy diagram of the integrated CELL (The diagram in a) is to scale with the exception that the 4-QW active region is expanded five times), and b) equivalent circuit of the optical neuron. $R_{n(p)}$ = resistance of n(p)-mirror, V_o = bias voltage. Only the lowest-energy conduction band is shown, i.e. the Γ-valley is shown for the GaAs layers while the X-band is shown for the AlAs layers.

850-870 nm converts longer wavelengths to shorter). Increasing the Al composition in the emitter and using InGaAs in the collector, base and quantum-well regions of the VCSEL, the wavelength conversion range can be significantly expanded. We also demonstrated cascadability of the devices by using optical feedback. A fraction of the VCSEL output power at 850 nm was directed onto the HPT and then the 800-nm input to the HPT was removed at which point we observed latching of the CELL.

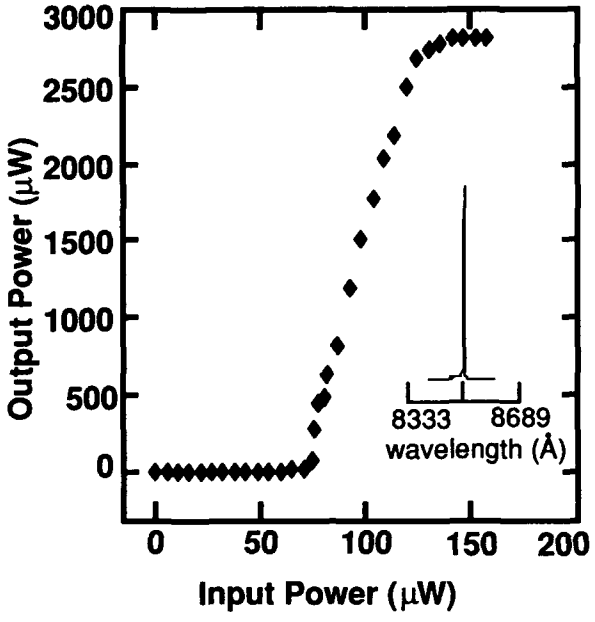


Figure 3. Room-temperature CW output power versus input power of a CELL. The HPT and VCSEL are connected in series as shown in Fig. 2b with the HPT in the floating-base configuration. The input and output wavelengths are 800 and 850 nm, respectively. The output diameter of the VCSEL is 15 μm. Input power has been corrected for reflection loss at the air/GaAs interface.

In conclusion, we have described a new device ideal for applications that require high-optical gain, cascadablity, and insensitivity to external optical feedback. CELLs can be operated as optical switching, optical bistable, or light amplification devices. To date we have demonstrated high optical gain using discrete components connected in series. We are presently fabricating 2-D arrays of devices in which the HPT and VCSEL diode are monolithically integrated. A natural application for these arrays are neural networks. Using a holographic optical element, one can realize a global configuration of an optical neural network in which CELLs perform optical neuron functions. Another property of the CELL worth exploring is the intermediate connection between the VCSEL and HPT. This internal connection provides us with additional flexibility in choosing the nature of the input and output optical signals. For example, CELLs can be configured as latching devices by allowing optical feedback via the high reflector at the HPT-VCSEL interface, in which case, as arrays, they would function as image memories capable of capturing and storing images. These devices can perform Boolean algebraic functions such as AND, OR using two beam combinations or as XOR by combining CELLs and HPTs. The slope of the output versus input curve can be modified to be either binary-like for digital functions or sigmoidal-like for neural functions (the curve shown in Fig. 3 is nearly sigmoidal and as such suitable for neural-network functions). As a final example, NxN out-of-plane arrays of individually addressable Wannier-Stark modulators [3] may be used to control inputs to arrays of CELLs (the input intensity for the HPT is below the excitonic saturation intensity of the Wannier-Stark modulators).

ACKNOWLEDGMENTS

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92-17301

Polarization-Independent Optical Waveguide Switch with Parabolic Potential Quantum Well

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Abstract

In a parabolic quantum well, the shift in the optical transition energy due to the quantum confined Stark effect is independent of the carrier effective mass. This fact enables us to realize polarization-independent waveguide optical switches. An absorption-type switch with $GaAs/Al_{0.3}Ga_{0.7}As$ equivalent parabolic quantum wells is fabricated with molecular beam epitaxy. Both transverse-electric and transverse-magnetic mode lights exhibit an on/off ratio of 10dB at an applied voltage of 3.5V at 844nm wavelength. To our knowledge, this is the first polarization-independent waveguide optical switch based on the electric-field-induced effect in the semiconductor quantum well.

1 Introduction

Carrier confinement in semiconductor quantum wells(QWs) results in extremely large exciton binding energy and oscillator strength when compared with those of bulk crystals. Under an electric field applied perpendicular to the QW layer, the energy of the fundamental absorption edge shifts by a large amount without severe line broadening of the exciton resonance. This well-known quantum-confined Stark effect(QCSE) enables one to utilize QWs for high-speed low-voltage optical waveguide modulators. Polarization-independent waveguide optical switches are very important in photonic switching networks. Polarization-independent semiconductor waveguide switches based on the injected carrier effect [1,2], or the linear electrooptic effect [3,4], have been reported. However, no attempt has been made to realize polarization-independent switching in a QW waveguide. This paper describes the first polarization-independent waveguide switch utilizing QWs.

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2 Numerical Analysis

Recently, besides QWs with rectangular potential shape, several kinds of QWs with modified potential shapes have been studied both theoretically and experimentally [5]-[13].

In the rectangular potential QW(RQW), the energy shift of the ground state due to the QCSE is proportional to the effective mass of the particle and that is expressed as

$$\Delta E = -\frac{1}{24}\left(\frac{15}{\pi^2} - 1\right)\frac{m^* e^2 F^2 L_z^4}{\hbar}.$$

Here, F is the electric field applied, L_z is the well thickness, and barrier height is assumed to be infinite for simplicity. On the other hand, the energy shift ΔE in the parabolic potential QW(PQW) [8]-[13] is given by

$$\Delta E = -\frac{e^2 F^2 L_p^2}{16 V_0}$$

where V_0 is the potential height difference between the potential at $z = \pm L_p/2$ and that at $z = 0$, and barrier height is approximated to be infinite[14]. In the PQW, the energy shift is independent of the particle effective mass, and therefore, the energy shift of the 1 electron-1 heavy hole (1e-1hh) exciton is equal to that of the 1 electron-1 light hole (1e-1lh) exciton. This effective mass independence of the excitonic transition energy shifts is a unique feature

of the PQW. Only transitions associated with light holes can interact with transverse magnetic(TM) mode light in a QW waveguide, while transitions involving both heavy and light holes interact with transverse electric(TE) mode light. Therefore in the RQW which is usually used, TM mode light cannot be modulated sufficiently as compared with TE mode light. We have calculated the absorption coefficient in both RQW and PQW, considering the 1e-1hh, 1e-1lh and 1e-2hh transitions. Both free carrier and the excitonic transitions are considered. We compared the calculated absorption spectra in the PQW and RQW, and have predicted that the TE-TM polarization-independent optical switching based on the above effect will become possible in a PQW waveguide under a reasonably low applied electric field[14].

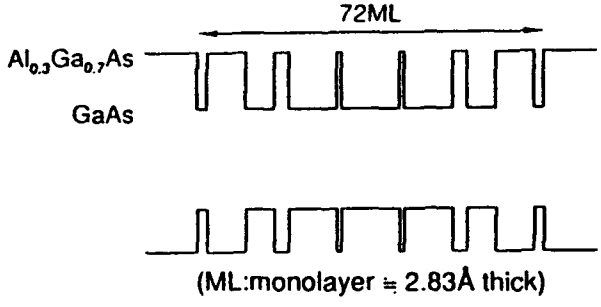


Figure 1: Schematic of the equivalent PQW structure employed. Superlattice layer thicknesses are 2ML,8ML,6ML,3ML,10ML,1ML,12ML,1ML,10ML, 3ML,6ML,8ML and 2ML, respectively. This set is sandwiched by 50Å thick $Al_{0.3}Ga_{0.7}As$ barriers.

For the fabrication of the PQW structure, the Al composition in the AlGaAs layer must be varied parabolically. However, it is very difficult and almost impossible in the growth with molecular beam epitaxy to fabricate a PQW, especially multiple PQWs with good uniformity, by gradually changing the material composition. In order to mimic a truely parabolic QW, we employ an equivalent PQW structure composed of $GaAs/Al_{0.3}Ga_{0.7}As$ as shown in Fig.1, which is designed according to a general method described in Ref.[13]. The $Al_{0.3}Ga_{0.7}As$ layers of thickness $[(N-0.5)/10]\cdot L_z/20$ were placed at a distance $(N-0.5)L_z/20$ from the well center and the remaining material was GaAs. Here, we chose $L_z = 200$Å and N=3.

We have confirmed numerically and experimentally the energy shifts of 1e-1hh, 1e-1lh and 1e-2hh transitions are almost equal in the equivalent PQW, as shown in Fig.3 [14]. Figure 2 shows calculated results of the electric field dependence of the excitonic transition energies at room temperature in the equivalent PQW shown in Fig.1, obtained with a variational method. It can be clearly seen the energy shift is almost independent of the effective mass of the particle. From this result, it is confirmed

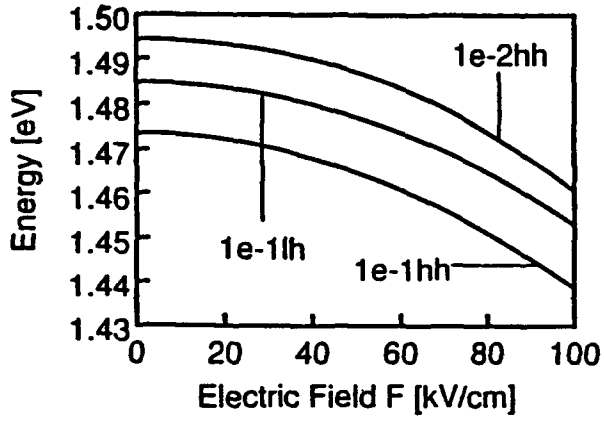


Figure 2: The field dependence of the energy of the excitonic transition at room temperature calculated for the equivalent PQW, shown in Fig.1.

that this equivalent structure has the unique property of the PQW, in which the energy shift of the excitonic absorption peak is independent of the particle mass. Figure 3 indicates the shift of the excitonic transition energies against the applied field obtained from the results of absorption current measurement at 80K. It can be seen that the energy shifts of the RQW [GaAs(125Å)/$Al_{0.3}Ga_{0.7}As$(57Å)] are different in magnitude from each other. On the other hand, in the PQW, the energy shift of 1e-1hh, 1e-1lh and 1e-2hh are almost identical. This result verifies the properties predicted for the PQW that the energy shifts of the excitonic transitions are independent of the effective mass of the particle involved.

Figure 4 shows the calculated absorption coefficient of the equivalent PQW as a function of applied field with the wavelength as a parameter. The wavelengths are chosen so as to be placed where the absorption is small at zero field and increases remarkably with the field especially for the TM mode. At a wavelength λ of 848nm, the absorption coefficients are almost identical at the field about 75kV/cm, but the absorption for TE mode at zero field is large. At λ of 850nm, absorption coefficients for both TE and TM mode lights are almost zero at zero field, and then meet again at 6×10^2cm^{-1} with an applied electric field of 90kV/cm. This means that if we change the applied field from 0 to 90kV/cm, we will be able to obtain a polarization-independent absorption-type waveguide optical switch with high on/off ratio. A similar switch can be obtained at λ=852nm.

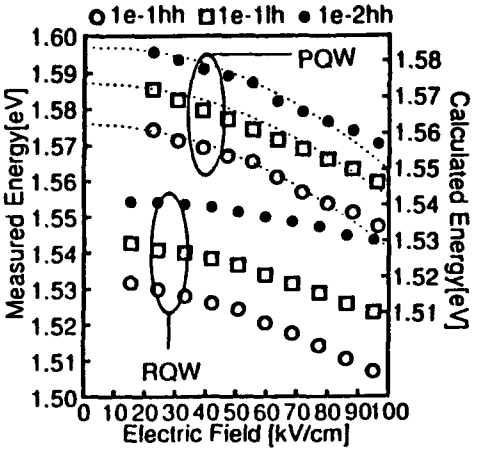


Figure 3: Applied field dependence of excitonic transition energies at 80K obtained from measured absorption current spectra, and numerical calculation (dotted curves).

3 Experimental Result

The sample structure fabricated with molecular beam epitaxy is a p-i-n diode with an intrinsic waveguide layer embedded between p and n clad layers grown on an n^+-GaAs (100) substrate. The planar waveguide layer consists of 17 periods of undoped equivalent PQW wells fabricated as the $GaAs/Al_{0.3}Ga_{0.7}As$ superlattice structure as described in the previous section, each separated by undoped 50Å $Al_{0.3}Ga_{0.7}As$ barrier layers. The thickness of waveguide layer is 0.428μm, and it supports only the lowest order TE and TM modes.

An Ar-laser pumped tunable Ti-sapphire laser was employed as the light source. After polarizing the light into TE or TM mode, it was focused on to the entrance facet of the cleaved sample with a 100× microscope objective. The outgoing light was monitored on either a video camera or an optical power meter, after magnifiication through a 20× microscope objective.

Figure 5 shows the experimental result. At 3.5V reverse bias (at 110kV/cm field), the on/off ratio for TE mode is equal to that for TM mode and both are about 10dB. Therefore, polarization-independent switching with an on/off ratio of 10dB has been achieved with a switching voltage of 3.5V at a wavelength of 844nm.

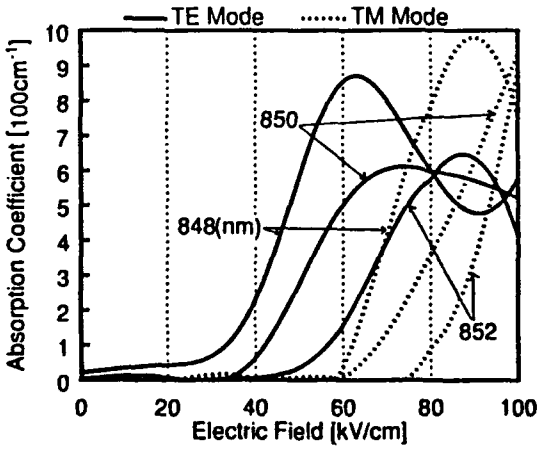


Figure 4: Calculated absorption coefficient *vs.* applied field at several wavelengths in the equivalent PQW shown in Fig.1.

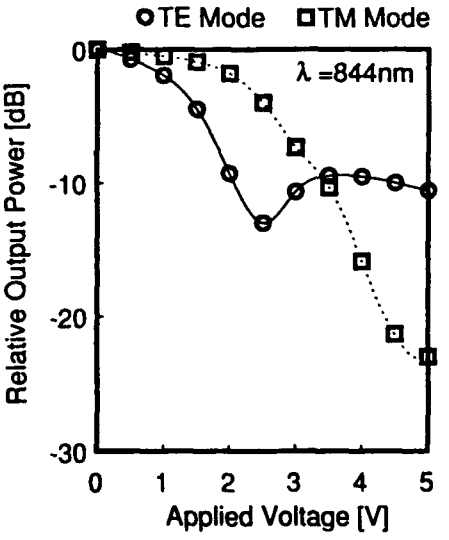


Figure 5: Measured modulation characteristics of the PQW absorption type waveguide optical switch with length of 448μm, at a wavelength of 844nm.

Between 2.5V and 5V, there exists a peak in the TE mode output. This characteristic is similarly seen in the calculated curves for the TE mode shown in Fig.4. We explain this phenomenon as follows: When the reverse bias voltage increases from zero, the absorption coefficient increases as the 1e-1hh exciton peak shifts over, decreases when the peak has left, and then rises again with the approach of the 1e-1lh exciton peak. For this reason, the absorption coefficient of TE mode light displays an initial overshoot which meets a monotonous rise of the absorption coefficient of TM mode light, giving polarization independent optical switching. This is easily achieved with the PQW because the light hole energy shift is enhanced.

In this experiment a polarization-independent on/off ratio of about 10dB was obtained. However, some of better experimental results upon more refined arrangements have just been obtained, and will be published elsewhere.

We have fabricated also a similar p-i-n diode sample with $GaAs/Al_{0.3}Ga_{0.7}As$ RQWs waveguide layer, and have confirmed that, at wavelengths where the insertion loss at 0V reverse voltage for TE mode is almost equal to that for TM mode, we can modulate the TE mode light but scarcely the TM mode light. At a wavelength of 860nm, as shown in Fig.3(a), the insertion loss at 0V for TE mode is measured as 26.6dB, and that for TM mode is 23.9dB. It is clear that TM mode light is hardly modulated. At a much longer wavelength of 862nm, as shown in Fig.3(b), the insertion loss at 0V for TE mode is reduced to 24.5dB, and that for TM mode is 23.6dB, and both are nearly equal. Still TE mode light is modulated, but TM mode light is hardly modulated. These results confirm that we can achieve polarization-independent optical switching with the PQW, but not with the RQW.

4 Conclusion

We have fabricated a $GaAs/Al_{0.3}Ga_{0.7}As$ waveguide optical switch with equivalent parabolic quantum wells by using molecular beam epitaxy. Both TE and TM mode lights exhibit an on/off ratio of 10dB at a common reverse voltage of 3.5V at 844nm wavelength. To our knowledge, this is the first polarization-independent waveguide optical switch based on the electric-field-induced effect in the semiconductor quantum well.

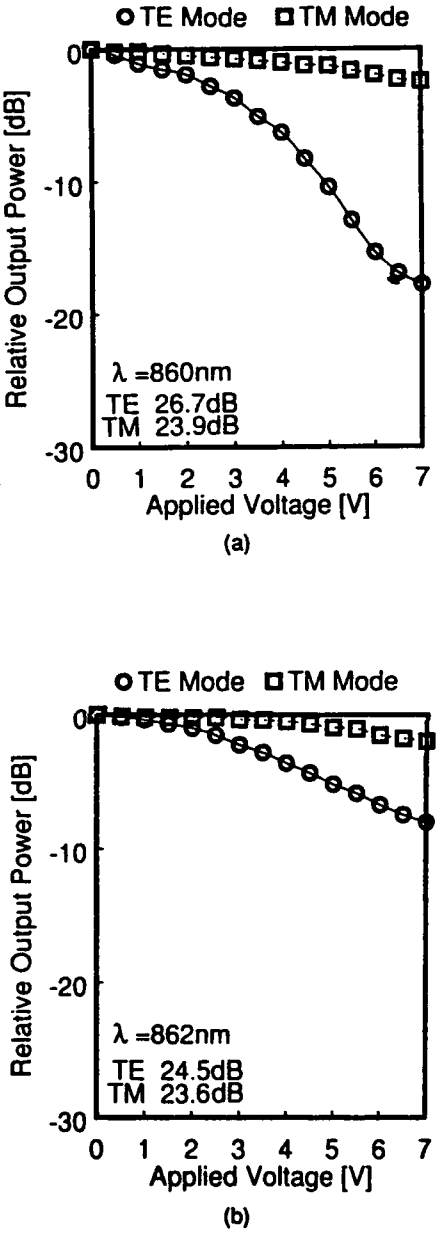


Figure 6: Measured modulation characteristics of the RQW absorption-type waveguide optical switch with length of 457μm for (a) λ=860nm, (b) λ=862nm.

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92-17302

High-Speed Wavelength and Spatial Switching with a Y-Coupled Cavity Laser

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Siemens Elektrik Lorenz AG

ABSTRACT:

Spatial switching and wavelength of 2 GHz, wide range tunability of 23 nm and high AM and FM bandwidth of > 3 GHz is demonstrated with a new integrated interferometric injection laser.

Introduction: For photonic switching there is a growing interest in III/V semiconductor based functions. Such components offer the capability of optical and electrical integration with other semiconductor devices even under low cost aspects. Based on interferometric principles /1/ we have developed a new InGaAsP/InP device with a wide range electronic tunability of 23 nm: the Y-coupled cavity integrated interferometric injection (YCC-I^3) laser /2-4/. For optical switching applications we consider this all active Y-shaped waveguide as a basic structure.
In this paper we present single mode wavelength tuning and wavelength switching of the interferometric YCCL. The capability for spatial switching is provided by operating the device as an absorption/amplifier switch below laser threshold. To demonstrate the high speed features of the device we report on AM and FM as well as wavelength switching results in the GHz regime.

Device structure: The schematic structure of the YCCL is given in fig. 1. The device was made in a two stage epitaxy process by LPE and MOVPE, more details are reported in /2/. The lateral carrier and photon confinement is achieved by a planar buried heterostructure process with semiinsulating InP blocking layers (SIBH structure). This structure offers excellent high speed capability due to low parasitic capacitance.

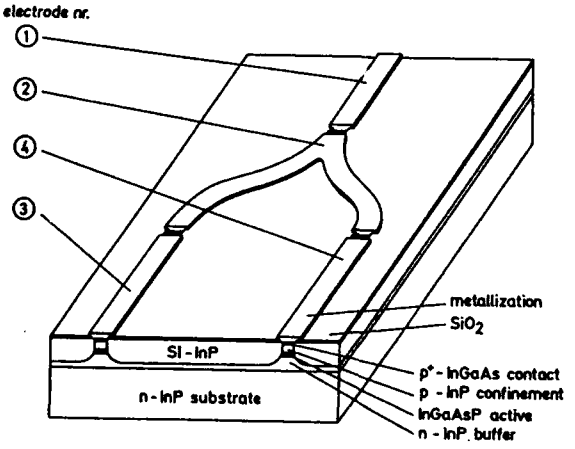


Fig. 1: YCCL structure

Principle of Operation: The YCCL is electrically segmented in four sections which can be addressed independently. Since all sections operate as active waveguides, additional losses from the curved waveguides and the Y-coupler can be compensated.

The interferometric laser operation is achieved due to the Y-coupling of the Fabry-Perot (FP) sub-cavities 1-2-3 and 1-2-4 between the cleaved facets 1 and 2 (see fig. 2). Different optical path lengths in the sub-cavities are adjusted by variation of the carrier densities. Such a compound resonator meets the requirements of single mode operation and tunability /1/.

Wavelength Tuning: Minimum total threshold current of a 1.2 mm long device is 145 mA at 25°C and maximum output power exceeds 5 mW. Wavelength tuning is demonstrated for a 1300 nm device. Making use of the extremely wide tuning range, 12 wavelength channels with spacing of 2 nm were arbitrarily defined (fig. 3) by applying appropriate currents. Side mode suppression up to 25 dB is obtained in the centre of the tuning range. These results demonstrate the capability of the device for applications in WDM systems.

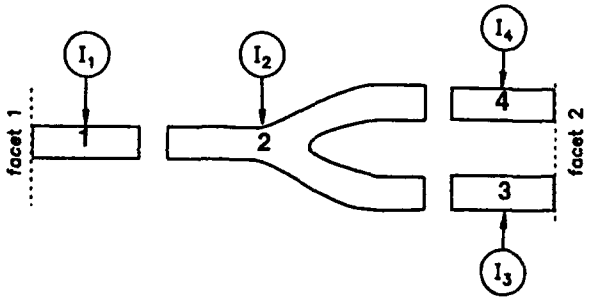


Fig. 2: Electrical segmentation scheme of the YCCL

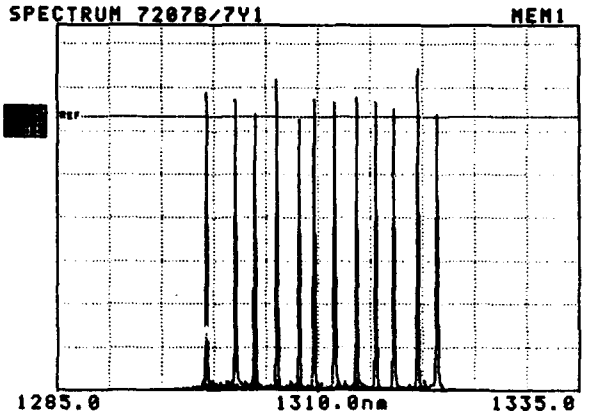


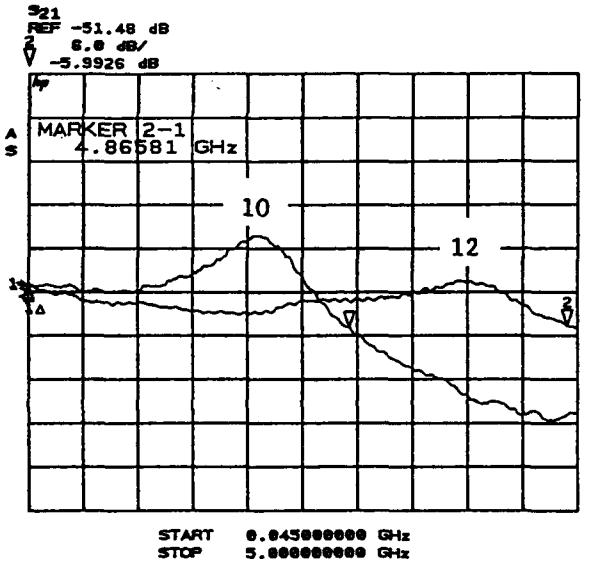
Fig. 3: Linear plot od 12 superimposed single mode emission spectra (channels) with a 2 nm wavelength spacing.

AM and FM Characteristics: To determine the high speed characteristics, an amplitude modulation signal was superimposed to DC-current I_1. High optical 3dB cut-off frequencies above 3 GHz were obtained. Results of AM response and corresponding optical spectra are plotted in fig. 4.

The FM response was measured with a scanning Fabry-Perot interferometer up to 2.8 GHz resulting in 330 MHz/mA efficiency.

Wavelength Switching: Switching between two interferometric modes was realized by superimposing of 30 mA square wave modulation (NRZ) on section 3 resulting in a shift of the FP spectra of 1-2-3 with respect to 1-2-4 (see fig. 2). Fig. 5 indicates the two corresponding interferometric laser-modes under switching operation. The wavelength switching could be realized up to 2 GHz.

Spatial Switching: To perform spatial switching with the YCCL, the device is operated below lasing threshold to achieve optical transparency only. As shown in fig. 6 light is injected into facet 1, and segments 3 and 4 are addressed as absorption modulators to switch the injected light to the output ports A and B at facet 2. The optical output signal was monitored with an infrared Vidicon camera. The measured near-field pattern are given in fig. 6. The achieved extinction ratio between optical on and off state exceeds 20 dB.



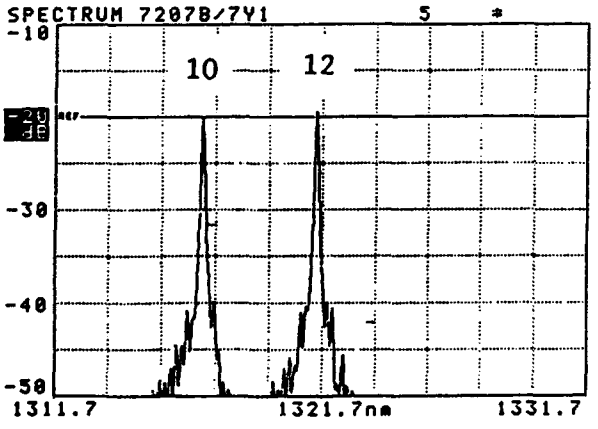


Fig. 4 AM small signal response (trace 10 and 12) and corresponding optical single mode spectra of channel 10 and 12.

Conclusions: With a new integrated interferometric injection laser in a Y configuration, lasing and switching features were demonstrated. Ultra wide tunability of 23 nm was achieved. Wavelength switching between interferometric modes up to 2 GHz and a modulation speed (AM and FM) exceeding 3GHz was obtained. Taking advantage of light splitting and amplification by the all active Y configuration, the basic device structure offers spatial switching as well. By cascading such all active power splitters the realization of fast matrix switching arrays appears feasible.

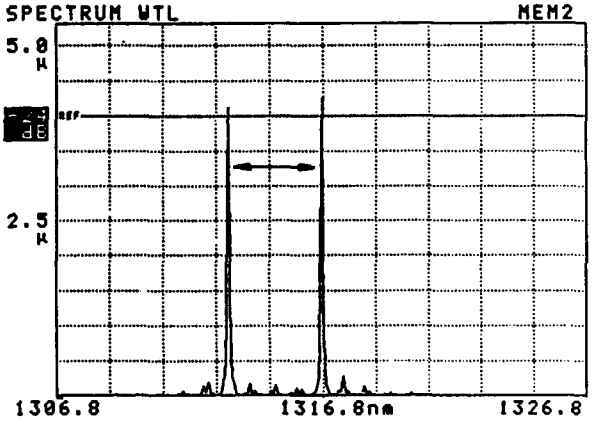
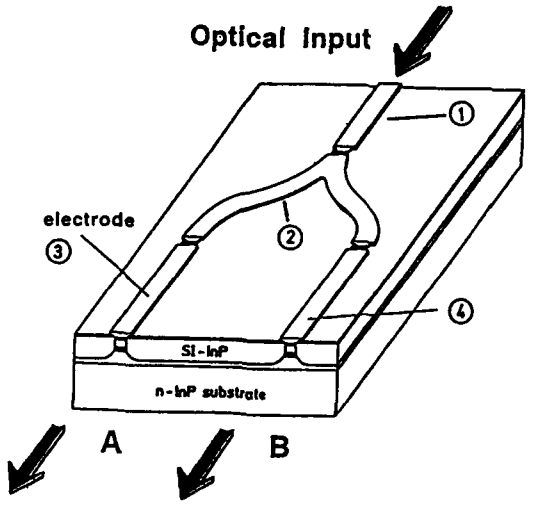


Fig. 5: Wavelength switching between 2 single mode channels with 2 GHz. For higher frequencies the switched mode (lower wavelength) disappears.



Optical Output Signals

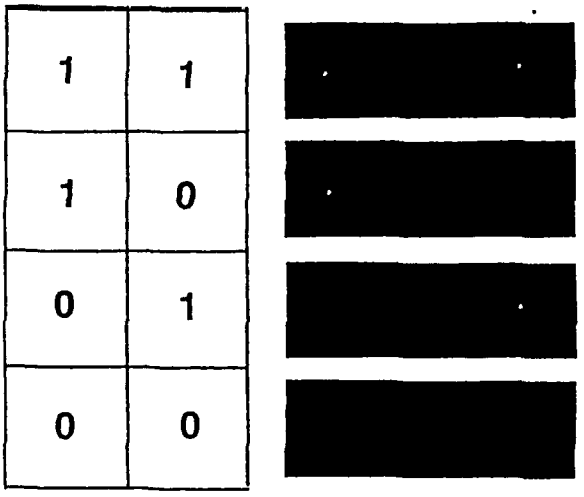


Fig. 6: Spatial Switching of injected laser light (1300 nm) coupled into segment 1. The optical output signals are indicated by near field spots.

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92-17303

Experiment and Applications of Picosecond On-Off Switching Using a Pair of Picosecond-On/Nanosecond-Off GaAs Etalons

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Abstract

Two GaAs etalons, each having a 30 ns recovery time, were connected in series, defining a logic function with a fast turn-on/turn-off time. Applications to routing, multiplexing, data generation and bit permutation are discussed.

Introduction

Semiconductor nonlinear Fabry-Perot etalons are promising devices for performing optical logic and switching operations in systems in which operational speed, throughput and interconnectivity are critical. An important characteristic of a logic or switching device is the number of operations it can perform in a given time. This figure is limited by both the device turn-on time [≅1 ps for GaAs nonlinear etalons (1)] and the turn-off time.

Nonlinear etalon recovery times range from 30 ns in bulk GaAs devices (Fig.1), to 3 ns in multiple-quantum-well samples, to 30 ps in very thin, 0.135 μm and 0.3 μm, "windowless" samples (with high switching energy) and 30 ps in small diameter (< 0.5 μm) microresonators (2,3,4). Therefore, to our knowledge, the fastest acceptable cycle time demonstrated in nonlinear etalons has been 30 to 70 ps (5). Further reduction of these recovery times will be limited by switching energy and the ability to focus to a small spot size.

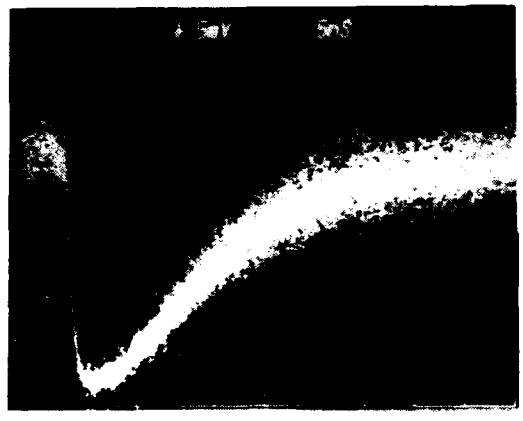


Figure 1. Bulk GaAs nonlinear etalon switch and recovery.

An architectural approach to decreased cycle time is possible. Two devices may be connected in series, one performing a logic operation with a fast turn-on and the other acting as a fast disable switch (6). The motivation for this approach, slow carrier recombination, and the method used, turn-on/disable, are similar to those seen in some photoconductive switching (7). For example, both devices may originally be in a reflective state [Fig. 2(a)]. A probe beam is transmitted through the first gate only after the gate has been switched [Fig. 2(b)], and the probe is routed to the output only until the second device is switched [Fig. 2(c)]. If the probe beam contains data, high-speed routing and logic operations may be performed. After a segment of data has been routed to an output, succeeding data may pass through the etalon pair to another pair for processing.

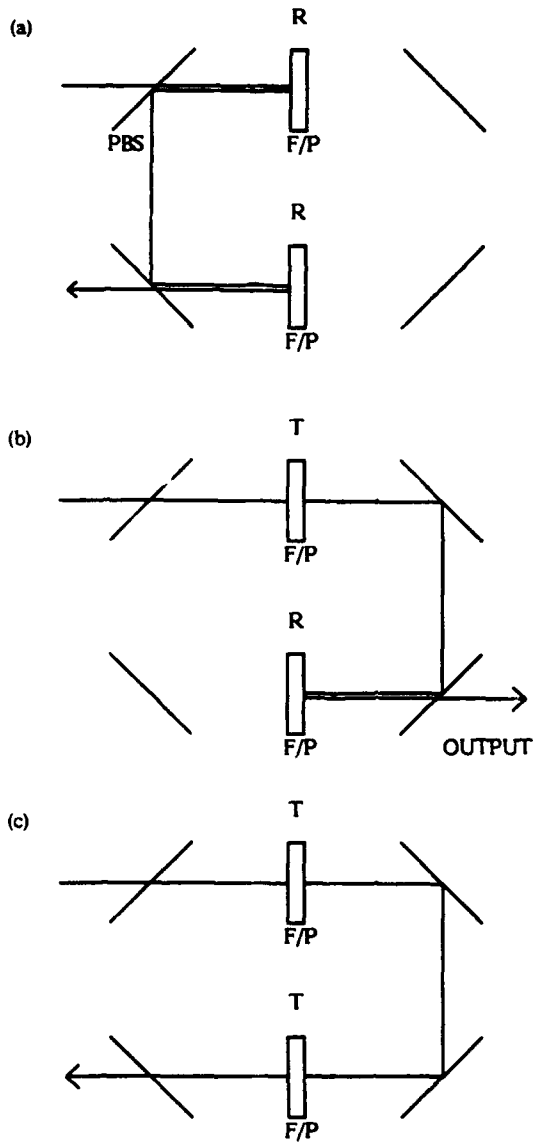


Figure 2. States of the device pair are determined by the states of the individual devices: (a) before operation, (b) during operation, and (c) after operation.

Device pairs may be linked to perform multiplexing, demultiplexing, self routing, bit permutation, and logic operations.

Experiment Results

An etalon pair defining a fast turn-on/turn-off operation was constructed. The devices were grown by molecular beam epitaxy (MBE) and have a GaAs spacer and integrated mirrors made of $\lambda/4$ stacks of AlAs and GaAs. Individually, the etalons exhibited a fast turn-on (detector limited response is seen in Figure 3) and recovered in 30 ns. A slight variance in the spacer thickness across a sample allows selection of the Fabry-Perot transmission-peak wavelength. Thus device operation (ON, OFF) is configurable using the probe wavelength and the input spot location.

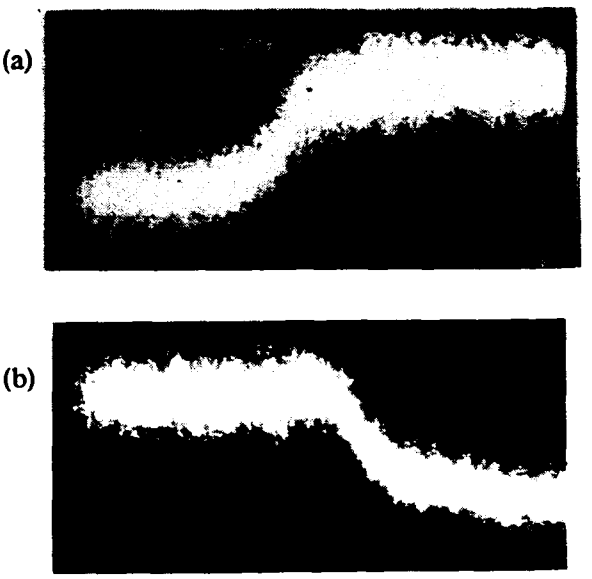


Figure 3. Single GaAs etalon (a) ON and (b) OFF operations (200 ps/division).

Two experiments were performed. In the first, a 50 ns probe pulse was used to represent a lengthy packet of input data pulses. The detector response time is 200 ps. The pump laser was tuned to 830 nm in order to be absorbed by the etalon spacer, and the probe wavelength was 880 nm.

Two etalons were connected in series as in Figure 2, and the output is seen in Figure 4. The signal contrast is ≅4:1. Figure 4(b) shows the result of adding a delay of ≅300 ps before cutoff, defining a longer extraction period.

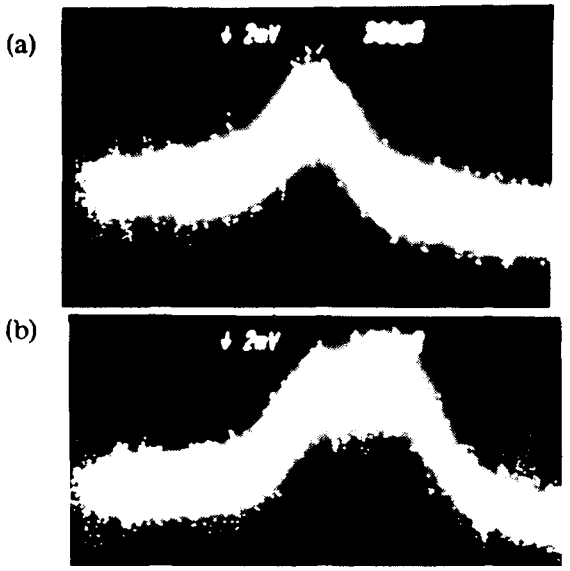


Figure 4. Device pair operation with (a) no and (b) ≅300 ps delay (200 ps/division).

In the second experiment, the pump and probe pulses were ≅10 ps full width/half maximum, 825 nm and 877 nm respectively, and were produced with a frequency-doubled Nd:YAG laser synchronously pumping two dye lasers (LDS 821). The experimental set-up for Figure 2 is seen in Figure 5; a split/delay/recombine technique was used to split the probe pulse into a pulse doublet, probe-1 and probe-2, separated by 40 ps. The response time of the detector is 90 ps; therefore, probes 1 and 2 were viewed separately by blocking one leg of the split/delay/recombine section (Figure 6). The pump pulse was split into an ON and an OFF pulse, also separated by 40 ps, which went to the first and second etalons respectively.

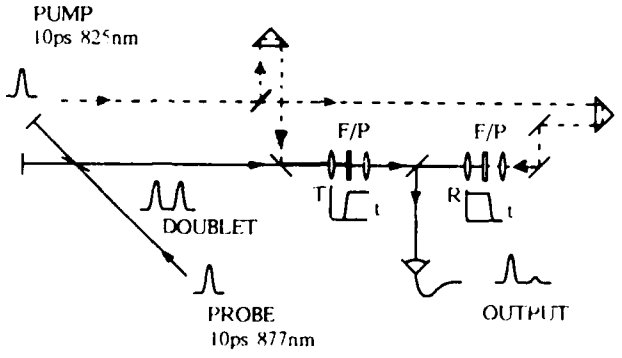


Figure 5. Device pair experimental set-up with pump (10 ps, 825 nm) and probe (10 ps, 877 nm).

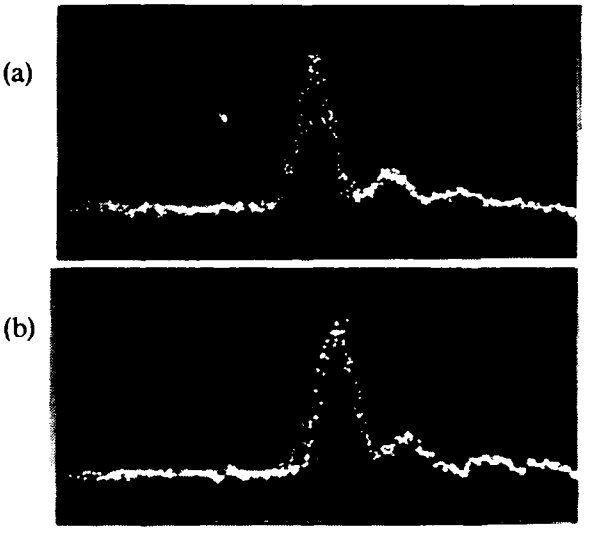


Figure 6. The probe pulse was split into a doublet seperated by 40 ps (100 ps/div.). (a) The detector limited response to the first 10 ps pulse is shown, second pulse blocked. (b) The second pulse is shown, first blocked.

At the begining of the experiment both etalons were in a reflective state. Then the On-pulse switched the first etalon, allowing the probes to pass through. Probe-1 was reflected by the second etalon to the output. Then the OFF-pulse switched the second etalon, routing probe-2 away from the output. Schematically the experiment timing (Figure 7) is that the extraction operation was turned on just before probe-1 went through the etalon pair and turned off just afterwards. Similarly probe-2 was extracted by delaying the ON and OFF pulses by 40 ps. Results are seen in Figure 8. Some triggering jitter is seen in Fig. 8(b), but the identities of probes 1 and 2 are known by the probe-pulse blocking procedure mentioned above.

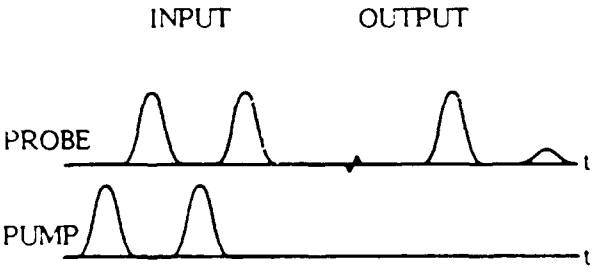


Figure 7. Timing scheme of the experiment extracting probe-1.

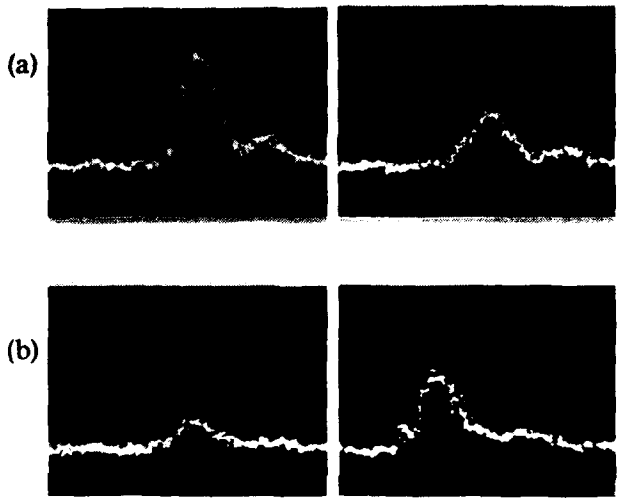


Figure 8. Results of the switching experiment (100 ps per division). (a) Extracting the first probe pulse: probe-1 on the left (probe-2 blocked) and probe-2 on the right. (b) Extraction of the second probe pulse.

We calculated that the spacer region of each etalon absorbed ≅24 pJ of pump energy in the 10 μm spot, and that the etalon finesses were ≅7 and ≅9. Measuring the performance of the individual devices, contrast increased with greater switching energy and with greater delay between pump and probe; therefore, the contrast of the etalon pair was limited by available switching energy and poor pump-pulse and probe-pulse shapes. Individual device contrast greater than 6 has been reported using only 3 pJ of switching energy (8), and switch-on time of a MQW etalon has been reported to be 1 ps (1). Therefore, cavity quality at λ_{probe}, mirror transmission at λ_{pump}, and pulse shape and duration, may be readily improved, increasing signal contrast and allowing the extraction of time windows as short as a few picoseconds.

Applications

The on-state of the device pair (defined by the timing of turn-on and disable pulses) may be very short, or it may be longer than the device recovery time (by refreshing the state of the first switch). This control over the timing and duration of the state of a switch suggests interesting applications. The probe beam may contain data, in which case routing may be performed by switching multi-bit packets. It should be noted that the probe beam follows the same exit path (Fig.2) before turn-on and after disable; so the flow of data through the etalon pair is perturbed only during operation of the pair. A series of etalon pairs may be used for demultiplexing (or multiplexing) by having the first etalon pair extract the first bit from the data stream, and having succeeding data flow on to the second pair where the second bit is extracted, etc. (figure 9).

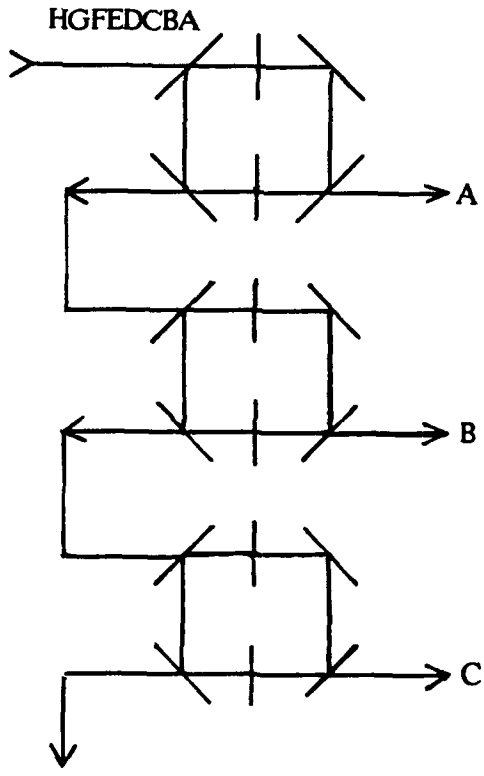


Figure 9. A series of etalon pairs, each extracting a successive bit in turn, may perform time demultiplexing.

More generally, each etalon pair may extract any desired bit. A data stream may be generated by extracting unwanted pulses from a continuous stream. Bit permutation (e.g. ABCDEF... → BHCFED...) may be done by having the first switch pair extract the B bit, the second extract H, etc. These bits are used to switch a slow-recovery holding element, and the elements are sampled in order and the result multiplexed. Multiplexing, permutation and demultiplexing may be combined to perform time multiplexed routing.

In most demultiplexing or routing applications, a slow detector is used to determine the value of the bit of interest. If there are n bits within the detector response time, bit energies E_X (bit to be extracted) and E_d (other bits) and extractor signal contrast C, then the detected energy is $E_d = CE_X + E_1 + ... + E_{n-1}$. Comparing the two extreme cases, $E_d(E_X=1; E_1=E_2=...=0) > E_d(E_X=0; E_1=E_2=...=1)$ only if $n<(C+1)$. This condition limits n for absolute-threshold determination of E_X. With $C\cong 2.2$ (Fig. 8), n=3, and 3:1 demultiplexing may be done. For some applications (e.g. final detection of a demultiplexed signal) differential or self-referenced determination of E_X may be used in which E_d is compared with $E_T=E_X+E_1+...+E_{n-1}$. In this case, $n \leq (C-1)R$ where R is the resolution of the comparator, and a much higher n:1 demultiplexing may be done. Coupling this approach with a much-improved signal contrast would enable demultiplexing a bit stream of a few hundred Gbit/s. Even without improved contrast, the data extraction approach shown here can be thought of as having generated a 25 Gbit/s very short data stream (removed either bit from a pair). By using short pump pulses, this approach may be used to remove undesired bits from a continuous stream of pulses, generating data at a rate of a few hundred Gbit/s.

Conclusions

We have shown that the operating period of a series pair of optical switches can be determined by the delay between switching of the first and second gates rather than the device recovery time. Therefore it can be of long duration or it can be as short as a few times the device turn-on time. We have used etalons that have a 30 ns recovery time to extract a 40 ps time window from an input stream. Shorter pump and probe pulses should improve contrast and shorten the extracted time window to a few picoseconds. The data extractor may be expanded to perform operations such as multiplexing, demultiplexing, self routing, bit permutation and data generation. Although recovery times in switching elements may be decreased, low-switching-energy high-speed devices such as nonlinear etalons will probably continue to have asymmetrical response times. Therefore, this architectural approach that trades device cycle time for system complexity and has unique memory properties will have application.

This research was supported by the Rome Air Development Center (F30602-89-C-0177), NSF Lightwave Technology (EET-8808393), and by the Optical Circuitry Cooperative.

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Photonic Switching Device by Integration of Heterojunction Phototransistor and Laser Diode

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Abstract

High gain and very sensitive photonic switching device is developed by integrating directly and vertically a hetero-junction phototransistor and a laser diode. The device switches on with a very low input power of ~10nW and emits output power of ~4mW under continuous wave condition. The minimum switching energy is estimated to be as low as *80fJ*.

I. Introduction

Recently, there are increasing interests in optical signal processing and optical computing. In such fields, optical functional devices which have various functions such as photonic switching, optical amplification, and optical bistability are greatly demanded. Thus far, we have proposed and developed the optical functional devices by integrating directly and vertically a heterojunction phototransistor (HPT) and a light-emitting diode (LED) [1-4]. The device has been understood a kind of optoelectronic integrated devices (OEID) rather than optoelectronic integrated circuits (OEIC) [4]. In the device, the output was the incoherent light and relatively low power, since the output portion of the device was an LED. Furthermore, the internal optical feedback was intentionally suppressed in order to obtain the linear relationship between input and output powers.

In this work, we have developed a very sensitive and high gain photonic switching device by integrating an HPT and a laser diode (LD) and by utilizing the internal optical feedback effectively. In Chapter II, the device structure and the fabrication process are described. In Chapter III, the characteristics of the component parts of the photonic switching device are described. In Chapter IV, switching characteristics are described. In Chapter V, the results obtained are summarized.

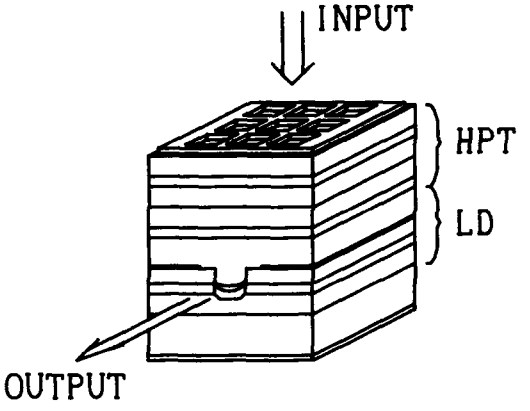


Figure 1. Schematic diagram of the photonic switching device.

II. Device Structure and Fabrication

Figure 1 shows the schematic diagram of the integrated device fabricated in this work. The device is composed of an HPT and an LD with PBC (p-substrate buried crescent) configuration.[5] The crystal wafer for the device was grown by three-step liquid-phase epitaxy (LPE). In the first step, the current blocking layers of p-InP, n-InP, and p-InP were grown on a p-InP substrate. Then, after the formation of the groove with

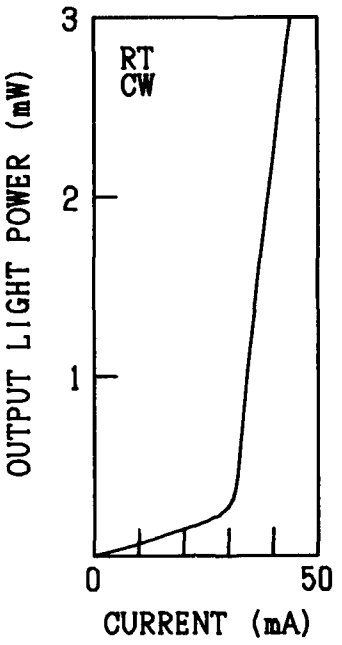


Figure 2. Output light power-current characteristic of LD part.

2μm width on the wafer, the layers of p-InP cladding, undoped InGaAsP active (λ_g=1.3μm), n-InP cladding, and n-InGaAsP (λ_g=1.2μm) were grown at the second LPE. By these growth processes, we can obtain a stripe geometry LD. The HPT composed of n-InP buffer, undoped n-InP collector, p-InGaAsP base (λ_g=1.2μm), and n-InP emitter was grown at the third LPE. After the growth, the AuGe/Ni/Au mesh electrode was deposited on the epilayer side and the AuZn/Au electrode was deposited on the back (substrate) side, followed by sintering them in H_2 atmosphere. Then, the wafer was cleaved and bonded on the Ag heat sink, and the device dimension was 250x300μm^2.

III. Characteristics of component parts of photonic switching device

Figure 2 shows the output light power-current characteristic of the LD part. The LD was operated in continuous wave condition at room temperature, and the threshold current I_{th} was 30mA. The differential quantum efficiency for one facet was 23.6%. From the near- and the far-field patterns, it oscillated in a stable single transverse mode. The oscillation wavelength was about 1.30μm at I=1.06I_{th}. For the photonic switching operation, the optical feedback from the LD to the HPT at the low current injection level ($\ll I_{th}$) is very important, where only

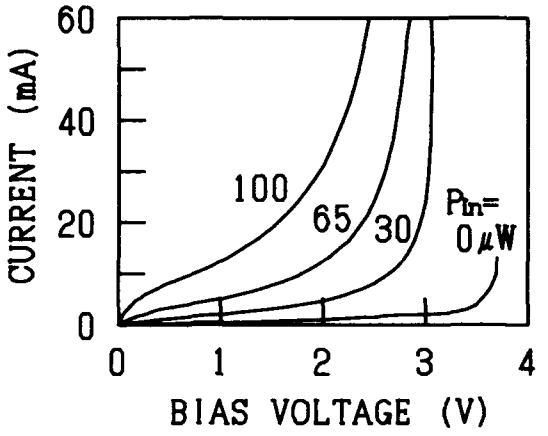


Figure 3. Bias voltage-current characteristics of HPT.

spontaneous emission is emitted from the LD. From the measurement of the spontaneous emission spectra, the laser emitted the light with the wavelength from -1.2 to -1.4μm at the low current injection level.

An example of the bias voltage-current characteristics of the HPT part is shown in Fig.3 where the input power is taken as a parameter. Since the measurement for the HPT part only is difficult due to the feedback effect from the LD to the HPT, it was made for the HPT fabricated from the wafer without the LD. The wavelength of the input light was 1.15μm. From Fig.3, it is found that the conversion gain from light to current is about 400 when the bias voltage V_{hb} was 4V and the load resistance was 60Ω. It is found that the conversion gain depends on the bias voltage. This is due to the early effect caused by the low doping concentration in the base layer and due to the avalanche multiplication effect caused by the high field in the region of high bias voltage. The bias voltage dependence of the conversion gain affects the operation of the photonic switching device as described later. From the measurement of the spectral response, it was found that the HPT can response even to the wavelength of 1.2-1.3μm although the responsibility becomes very weak. Since the LD emits the spontaneous emission from 1.2 to 1.3μm, the weak feedback occurs from the LD to the HPT.

IV. Photonic switching characteristics

The optical feedback is positive and it functions to increase the current through the device. The positive feedback causes a negative differential characteristic to the output light power-bias voltage relation, and thus the switching operation becomes

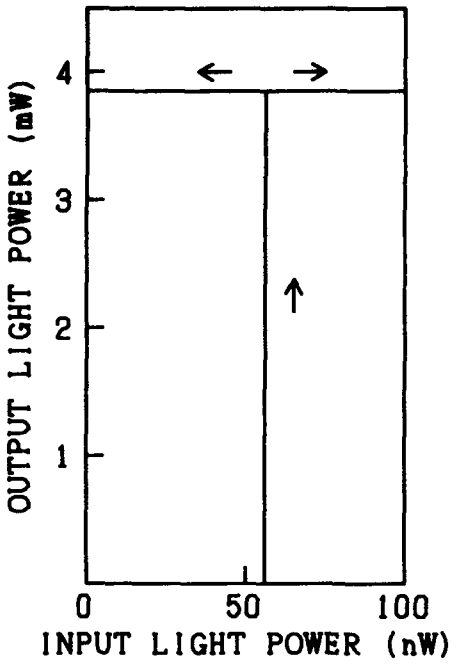


Figure 4. Photonic switching characteristic.

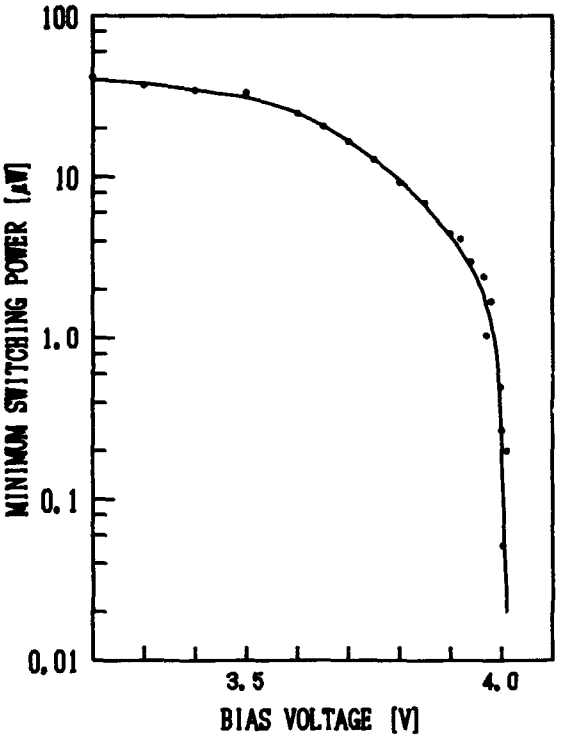


Figure 5. Minimum switching power as a function of bias voltage.

possible. The switching characteristics of the device is shown in Fig.4 where the bias voltage is 4.01V and the load resistance is 50Ω. The device was switched on with very low input power of 56nW. It emitted large output power of ~4mW and was at the ON state in cw lasing condition at room temperature. The wavelengths of the input and output lights were 1.15μm and 1.30μm, respectively. Therefore, the optical gain, which is defined here by the ratio of the output power to the input switching power, is as large as ~1×10^5. In the other device, the minimum switching power of ~10nW was achieved. The high gain is due to the realization of the lasing oscillation and the effective utilization of the optical feedback from the LD to the HPT. The current flow under the internal optical feedback is expressed as follows:

$$I = \frac{\{q/(h\upsilon)_{in}\}GP_{in} + I_{dark}}{1 - k\eta G}, \qquad (1)$$

where $(h\upsilon)_{in}$ and P_{in} are the photon energy and the optical power of the input light, respectively, G the conversion gain of the HPT, η the internal quantum efficiency of the LD under the LED mode, k the feedback constant from the LD to the HPT, and I_{dark} the dark current of the device without feedback. Since both η and G are dependent on the bias voltage and the current flow of the device, the effective gain $G/(1-k\eta G)$ is greatly increased by adjusting the bias voltage. In this situation, the very small input P_{in} causes the relatively large increase of I and succeedingly the values of η and G are increased. Due to the positive feedback, the device turns to the ON state with small input power. Figure 5 shows the minimum input power required for switching on as a function of the bias voltage. As can be seen from the figure, the switching power is greatly decreased with increasing the bias voltage.

The energy required for the switching was measured by using optical pulse input. The intensity of the input pulse was changed to the value with which the device was switched to the ON state for the various pulse width. The wavelength of the input pulse was 1.15μm. Figure 6 shows the results obtained for the two photonic switching devices. The minimum switching energy is as small as 80fJ. At present, the device size is as large as $300\times250\,\mu m^2$. The switching energy is consumed to charge up the capacitance between the emitter and the base layers. Thus, the smaller switching energy can be further expected to reduce the surface area of the HPT.

The detailed results on the photonic switching characteristics including

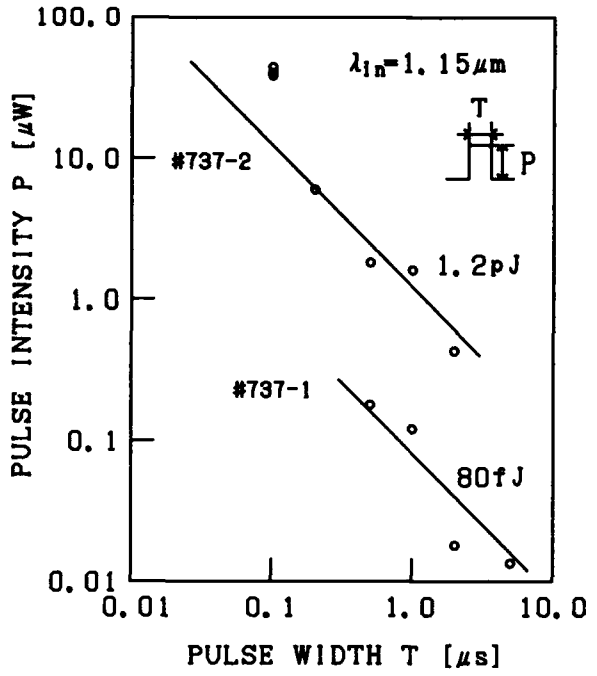


Figure 6. Switching power as a function of pulse width of input light.

quantitative consideration of the optical feedback will be reported elsewhere [6].

V. Summary

A photonic switching device has been achieved by a vertical and direct integration of an HPT and an LD. The device has been switched with a very low input power of ~10nW and emitted a power of 4mW under continuous wave condition. The large gain is due to the achievement of lasing oscillation and the internal optical feedback. The switching energy have been as low as 80fJ and can be decreased by reducing the surface area of HPT.

Acknowledgment

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92-17305

Low-Power High-Gain Optoelectronic Switch Based on Quantum Stark Effect and Its Use in Logic Operations

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ABSTRACT

A low optical power switching device is demonstrated by using quantum Stark effect in a specially designed base-collector region of a heterojunction bipolar transistor.

I. INTRODUCTION Quantum Confined Stark Effect (QCSE)[1-4] holds a great deal of promise for active switching devices controllable by light and/or electronics. This effect allows one to tailor the device response to such a great extent that at least in principle a number of powerful devices can be conceived and demonstrated.

The first demonstration of active logic devices based on QCSE was the self electro optic effect device (SEED), where the optical(or the electronic) state of the device could be altered by light intensity[4]. A variation on the SEED device was introduced by including an external transistor to amplify the photocurrent, so as to allow electronic gain in the device[5]. This allowed the use of low optical power consistent with semiconductor laser diode technology. High gain was obtained at the University of Michigan by integrating a multiquantum well(MQW) structure into the base-collector region of an HBT[6,7], thus producing a versatile device compatible with the HBT technology, p-i-n modulator and laser technology. The device can be switched by optical or electronic signals and these features will be explored in this paper. Also a better design understanding has now allowed us to have a very high gain in the device.

II. THE MQW-HBT CONTROLLER - MODULATOR The potential of the negative resistance region of the I-V characteristics of a p-i(MQW)-n structure was realized by Miller et al[8] and used to develop the SEED. Using a resistor in series with the p-i-n diode, the device can be shown to have efficient switching behaviour.

In order to make the SEED more compatible with the optical power levels available in OEIC technology, it is important to have built-in electronic gain in the device. Gain is also essential for larger tolerance in the devices as well as large fan-out and cascadability. Such gain can be realized by using an HBT with a MQW in the base collector region[6,7]. This device provides a number of advantages. The vertical structure of the HBT facilitates the developement of a large potential across the base-collector region to cause QCSE. The base terminal provides extra controllability for efficient optical and electronic coupling. The entire structure for n^+-p-i(MQW)-n MQW-HBT and the p-i(MQW)-n modulator can be grown epitaxially in one step. It is conceivable that the p-i-n structure could also form a laser which would be grown in the same planar growth. The structure is therefore very compatible with OEIC applications.

A schematic of the integrated MQW-HBT is shown in Fig 1. The MQW-HBT is shown in a circuit where it is controlling a modulator. The heterostructures for the controller-modulator is grown by us using MBE. The structure and the fabrication process are described elsewhere[7]. The fabricated devices showed common-emitter current gain from 30 to 60. The high offset in V_{CE} is due to the presence of heterostructure and MQW at the base-collector region. A modulator device exhibits a very low leakage current(a few pA at 8V). The device operating characteristics were measured by using an AlGaAs diode laser (λ =853nm) and HP4145B semiconductor parameter analyzer.

Fig 2 shows the measured I-V charateristics for two different switching conditions. In the figures the load lines are also shown. Fig 2(a) shows the collector current-voltage for different values of optical power at zero base current,while Fig 2(b) shows the results for different base currents at fixed optical power. Thus efficient switching can be carried out by optical or electronic signals. The

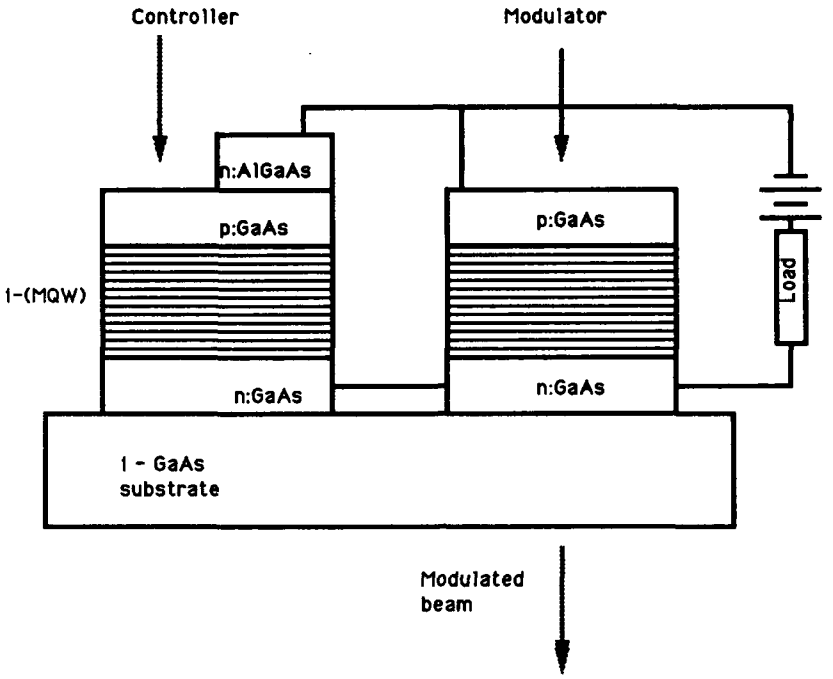


Figure 1 An MQW-HBT structure along with a p-i(MQW)-n modulator.

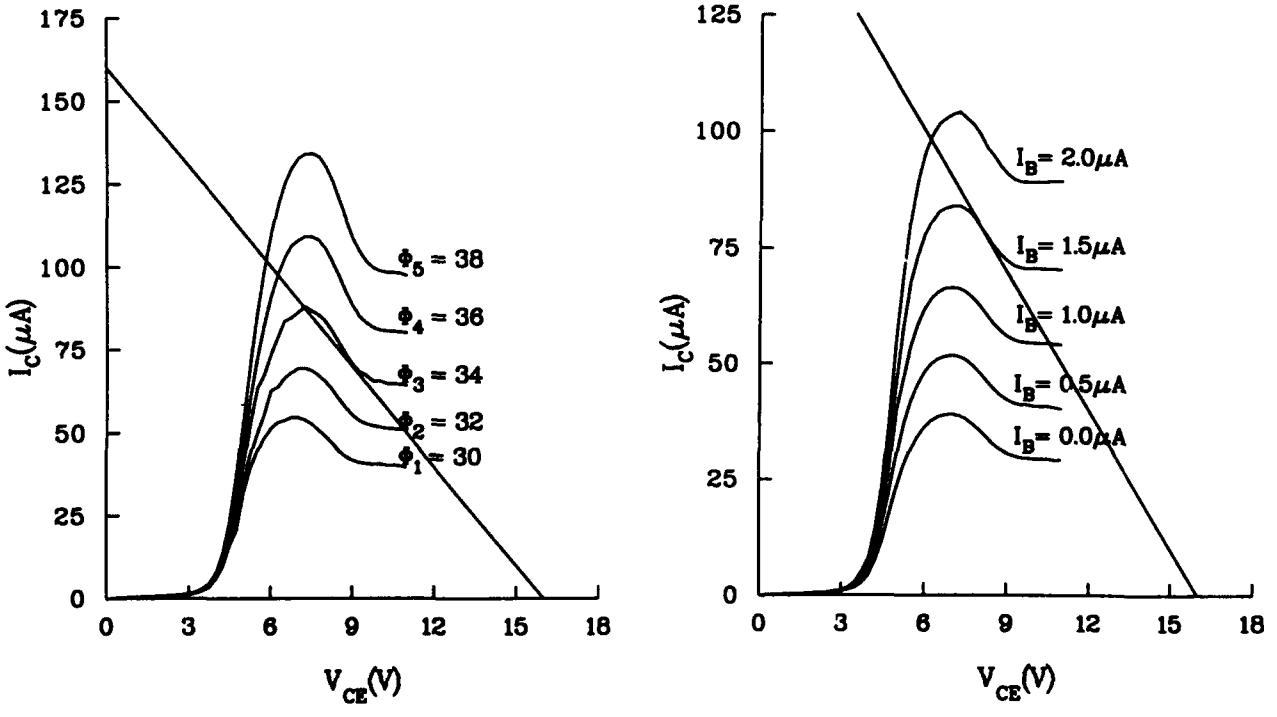


Figure 2 Collector current versus collector-emitter voltage characteristic of the MQW-HBT. (a)At $I_B = 0\mu A$, for different illumination levels. The illumination(Φ) is indicated by the diode laser drive current in mA.(b) For different base bias at constant illumination(Φ = 27mA).

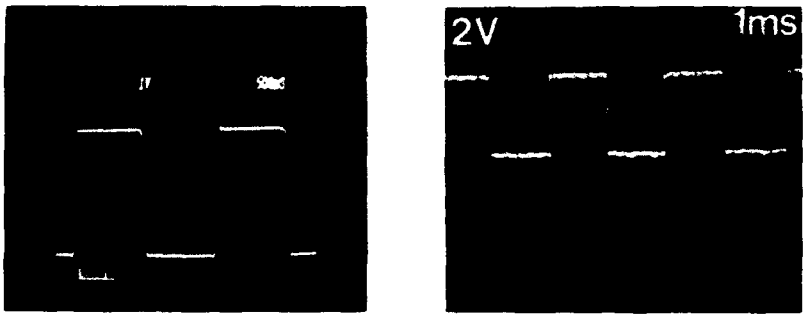
important point to realize is the presence of amplification of photocurrent, which provides for higher sensitivity to light and reduced load resistance. Another point is that the I-V curves can be shifted either by optical power or base bias. Also the non-linear gain characteristic of HBT makes the negative differential resis-
stronger than in the simple p-i-n structure.

Fig 3 shows oscilloscope traces of MQW-HBT switching. From this figure it is evident that a swing of 5 V is acheived by a small change in the input optical power or base bias.

The temporal response of the device was also studied. The response time is primarily limited by the RC time constant of the bipolar, which is about 1 nsec.

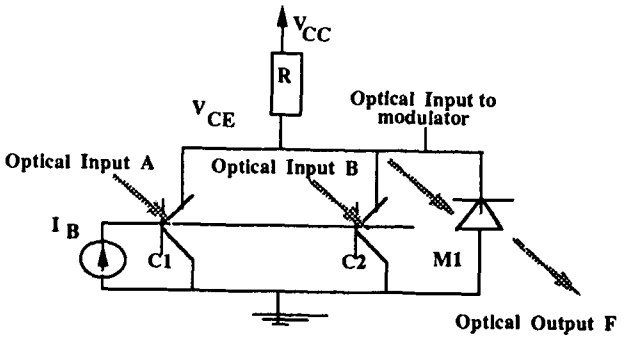
The device was also used to realize an optical logic gate. Fig 4(a) shows the circuit for NOR logic operation. Two MQW-HBTs(C1,C2) and a modulator(M1) are connected in parallel. The collector-emitter voltage(V_{CE}) of the controllers drive the modulator.

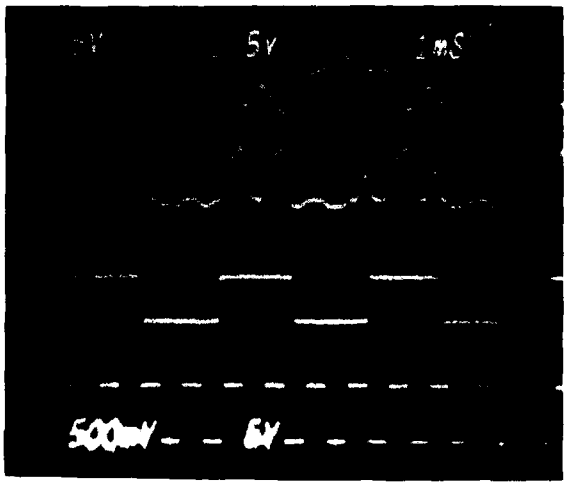
The input signals to the gate(A and B) are incident on the two MQW-HBTs. The gate output(F) is from the modulator. The modulator (M1) modulates a constant



(a) (b)

Figure 3 Oscilloscope traces of switching of MQW-HBT.(a) With illumination modulation between $\Phi = 32$ and $\Phi = 36$ and $I_B = 0\mu A$. (b) With base bias modulation between $2.0\mu A$ and $1.0\mu A$ at $\Phi = 27$.





(a) (b)

Figure 4 (a) The NOR gate circuit. A and B are inputs to the gate. F is the output of the gate. (b) Oscilloscope traces for operation of the NOR gate. The top trace(for F) is in 500mV scale, the rest of the traces are in 5V scale.

intensity beam to generate F . Fig 4(b) shows the operation of the circuit. The two traces at the bottom are the inputs A and B . The trace just above it is for V_{CE}. The topmost trace is the modulator output F. From the figure it can be seen that V_{CE} is high only when both inputs A and B are low. The apparent phase delay between V_{CE} and the inputs(A & B) is due to the mechanical choppers used for modulation. The trace for ouput F is almost an inverted replica of V_{CE}. The inversion is due to the particular operating point choosen. Hence the circuit is actually performing an OR operation, for positive logic. By moving the operating point to a higher voltage the device can perform a NOR operation.

In summary we have demonstrated the performance characteristics of an MQW-HBT device which can be switched optically or electronically. Simple logic operation has also been demonstrated.

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Dynamic Optical Grating for Laser Beam Steering Applications

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ABSTRACT

A linear grating fabricated with quantum well reflection modulators was demonstrated. Addressing each stripe individually allowed angular control of the diffracted laser beam.

INTRODUCTION

Devices for controlling the direction of an optical beam or the spatial patterns of illumination produced by a laser have been very limited in the past, and confined almost entirely to mechanical methods, such as galvanic mirrors. A method whereby this spatial control can be performed electronically with no moving parts will allow much faster and more reliable control of optical beams.

Spatial light modulators, devices in which optical properties of the material are spatially controlled, have previously been very large compared to the wavelength of light, and have therefore been useless for obtaining diffraction patterns. Recently, higher resolution SLMs have been reported that allow interference properties to be exploited [1], however, their complex structure is clearly a limitation to obtaining higher resolution. Present semiconductor technology, however, allows the use of quantum well devices to make much smaller spatial light modulators where diffraction effects dominate. Since these devices are intrinsically very fast, and can be made lithographically, they are useful in rapidly controlling far-field patterns of illumination and obtaining beam steering through diffraction. These devices can work in transmission mode, where the light passes directly through the quantum well region, or in reflection mode, where external or integrated mirrors are used to enhance reflectivity changes and contrast.
In this work we demonstrate the possibility of laser beam control with a dynamic grating constructed of Fabry-Perot reflection modulators. Other dynamically controlled gratings have been reported in the past, however, they operated at much longer microwave wavelengths [2]. By using quantum wells and lithographically defining stripes on the wafer, we obtain control of the far field pattern in the optical regime. Since the far field is a Fourier Transform of the spatial reflectivity of the device, we can steer a laser beam by imposing a pattern that oscillates spatially on the stripes. The deflection angle of the modes being given simply by the grating formula $d\sin(\theta)=m\lambda$. Power efficiencies and accurate beam profiles can be calculated from the Huygens-Fresnel integral [3].

DEVICE DESCRIPTION

To demonstrate this idea, we fabricated such a structure working in the reflection mode in the GaAs/AlGaAs system. The reflective mode is preferred for two reasons. Since in this material the substrate is opaque to the appropriate wavelength, constructing a transmissive device would require the removal of the substrate. Furthermore, by working in the reflection mode, we can obtain higher contrast and lower loss due to the interaction of the Fabry-Perot cavity with the quantum wells. The epitaxial growth of the material is explained previously [4]. In brief, the material was grown on a n-type GaAs substrate using molecular beam epitaxy (MBE). The mirrors composing the Fabry-Perot cavity consisted of 1/4 wave stacks of AlAs and $Al_{0.33}Ga_{0.67}As$. The bottom mirror was n-doped and had a calculated reflectivity of 98.8%, while the top mirror was p-doped with a reflectivity of 50.3%. The cavity contained 19 undoped quantum wells. The total reflectivity of the device changed from about 10% to 76% when a 5 volt bias was applied. The reflectivity of the device as a function of wavelength for various applied bias voltages is shown in Fig. 1. We then used a wet etching technique to fabricate 15 stripes, each being 10 μm wide and with a 2 μm wide gap. The stripes were individually contacted with an ohmic contact pattern around the edge of the wafer. Fig. 2 is a photograph of the fabricated device.

The device was tested using a tunable Ti:Sapphire laser. The laser beam was tuned roughly to the Fabry-

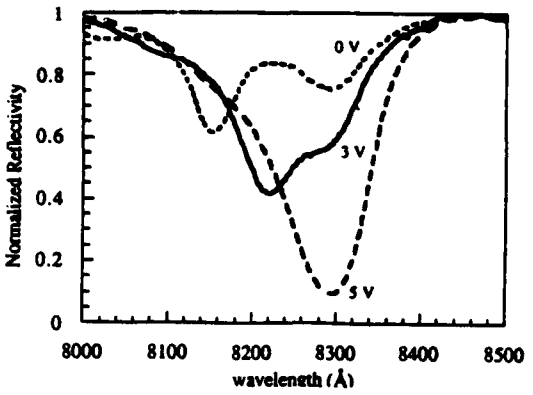


Figure 1. Reflectivity as a function of wavelength at various reverse bias voltages.

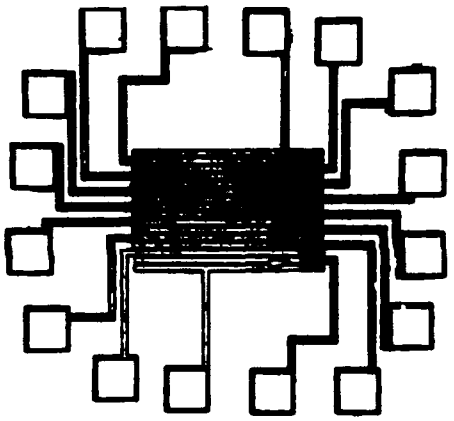


Figure 2. Photograph of grating device.

Perot mode of the device and focused down using a single lens. When illuminating the device it is important to have a large enough spot size to illuminate as many of the stripes as possible without getting reflections from other parts of the wafer, such as the contact pads. In this case the diffracted beam was deflected with a small mirror onto an imaging lens and a silicon CCD camera . The device was packaged and wire bonded to allow an external bias to be applied to the stripes.

EXPERIMENTAL RESULTS

The experimental results are displayed in Fig. 3. Next to each plot of intensity vs position, we have noted what pattern of reflectivity was imposed on the stripes. In the figure a "1" implies a reflective state, and a "0" implies a non-reflective state. In the first plot, where all the elements are in a reflective state, we see the main reflected peak to the left and a peak corresponding to spatial frequency of the isolation mesas to the right. Since this peak is due to the reflectivity difference between the mesas and the stripes, it occurs with differing intensity in almost all plots. Had the mesas been smaller in size, this peak would be

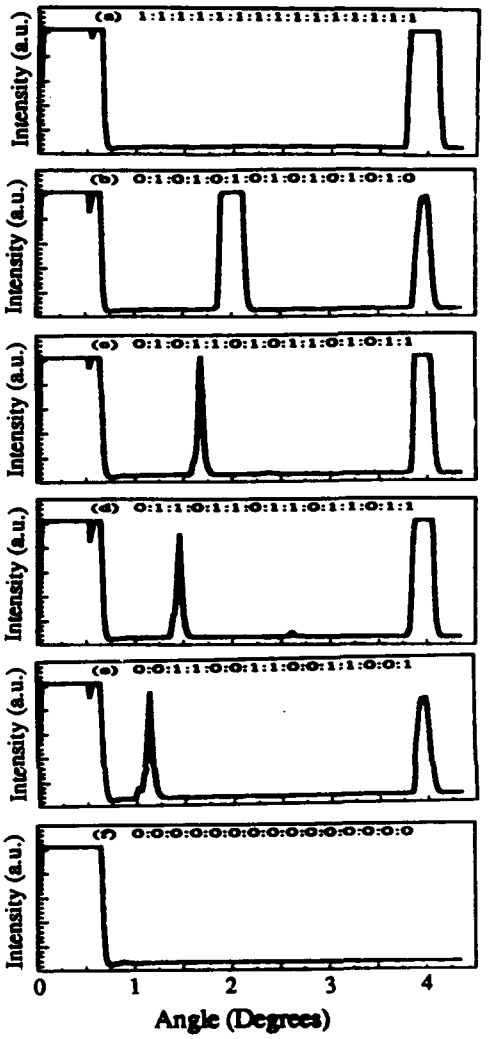


Figure 3. Intensity versus angle for various stripe configurations. "0" corresponds to low reflectivity and "1" to high reflectivity.

correspondingly reduced. The main reflected peak on the left is due to the DC reflectivity value of the pattern, and is the main power loss mechanism. In the second plot (b) the pattern 1:0:1:0:1... causes a main peak to occur in the center of the range. The position of this peak corresponds to the spatial frequency imposed on the stripes and is twice the stripe period (24 μm). In the next three figures (c,d,e), we see this peak move to the right as the spatial frequency decreases. The final plot (d) corresponds to all the elements in the off state, and we see only the main reflective peak. The peak due to the mesas disappears in this plot since our off state reflectivity corresponds roughly to the reflectivity of the mesa regions.

The optical characteristics of such a device are simple to compute. The continuous scanning angle obtainable from such a device corresponds to twice the grating period. This is simply because the maximum

spatial frequency that can be imposed on the stripes in with the stripes alternately on and off, which defines an imposed grating with period twice that of the stripes. Although this scanning angle is small in our demonstration (2 degrees), larger angles were also obtained from other patterns that used smaller stripes. However, the larger scanning angle made imaging onto the camera impossible. Simple optical lithography can produce grating spacings on the order of 2 μm, allowing an achievable scanning angle of 12 degrees. Larger scanning angles can be obtained either through more sophisticated lithography, such as holographic or electron beam, or by using a higher order mode.

DISCUSSION

In most applications, the resolution of the device is the most significant characteristic. If we define the resolution as the angular distance from the maximum of the mode to the adjacent minimum, then from simple grating theory [2] we know the resolution is given by $\Delta\Theta = 1 / Nd$, where Nd is the total width of the grating. The maximum number of resolvable beams is then equal to the number of stripes used. Since there are no fundamental limits to the number of stripes and the size of the grating, the performance of such a device can be tailored to one's needs.

The efficiency is also simple to calculate. If the mesas are made small compared to the width of the stripes, then the efficiency will be dependent on the harmonic content of the signal imposed on the stripes. In simple reflection geometry devices, such as demonstrated, a great deal of power is wasted through absorption in the stripes that are off, or reflection in the main lobe. These can be both be decreased using modulators that change the phase and not the amplitude. If an external Fabry-Perot cavity is employed,the wasted beam in the main lobe can be reflected back onto the device and dramatically increase the efficiency.

CONCLUSION

We have demonstrated a novel beam steering technique, using an electrically controlled dynamic optical grating. There appear to be no fundamental limitations to the fabrication of much higher performance devices that have diverse applications.

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