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NTATION PAGE

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1. AGENCY USE ONLY (Leave blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	10/15 91	10/1/90-9/30/91 End of FY Letter

4. TITLE AND SUBTITLE
Holographic Optical Interconnects for Multichip Modules.

5. FUNDING NUMBERS
N00014-91-J-4022
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6. AUTHOR(S)
Dr. Michael R. Feldman

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
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8. PERFORMING ORGANIZATION REPORT NUMBER

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11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

The primary purpose of this research is the development of a prototype multichip module incorporating high efficiency, high connection density optical interconnects. During year 1, individual components are to be designed, fabricated and tested. Various methods to achieve and maintain alignmentbetween the components are to be developed and tested experimentally. The results of this work are to be used to develop components for a demonstration system, termed"system 1" that is to be completed during year 2.
This report describes results of this project for the first 3 months, from July 1, 1991 - Oct 1, 1991. The work has been divided into 4 tasks. CGH's, Photodetectors, Laser Diode research and System Integration. Preliminary progress has been made in each of these areas. In addition, plans for the coming year are presented.

14. SUBJECT TERMS
Holograms, binary optics, laser , optical interconnects multichip modules, photodetectors.

15. NUMBER OF PAGES
8

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
None	None	None	None

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C	- Contract	**PR**	- Project
G	- Grant	**TA**	- Task
PE	- Program Element	**WU**	- Work Unit Accession No.

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FY 91 End of Fiscal Year Letter

(01 Oct 1990 - 30 Sep 1991)

ONR CONTRACT INFORMATION

Contract title:	Holographic Optical Interconnects for Multichip Modules
Performing Organization:	University of North Carolina at Charlotte (UNCC)
Principal Investigator:	Dr. Michael R. Feldman
Contract Number:	N00014-91-J-4022
R & T Project Number:	pakg002---01
ONR Scientific Officer:	Robert W. Schwartz

Enclosure (1)

Statement A per telecon Robert Pohanka
ONR/Code 5000
Arlington,VA 22217-5000

NWW 7/23/92

A. Description of Scientific Research Goals:

The primary goal of this research is the development of a prototype multichip module incorporating high efficiency, high connection density optical interconnects. During year 1, individual components are to be designed, fabricated and tested. Various methods to achieve and maintain alignment between the components are to be developed and tested experimentally. The results of this work are to be used to develop components for a demonstration system, termed "System 1," that is to be completed during year 2. Results from the fabrication and testing of the System 1 MCM will be used to design the final prototype system, the System 2 MCM, in year 3.

The System 1 MCM will contain 4 GaAs laser array I.C.'s, 64 Si I.C.'s and CGH's for ~512 connections. The GaAs chips will contain 32 edge-emitting lasers per chip. Each laser will have a fanout between 1 and 5 for connections within the module and to output ports. The System 2 MCM will be the final prototype module, incorporating 16 laser array I.C.'s. Improved versions of the CGH's and detectors will also be incorporated. 32,768 connections will be demonstrated.

The work has been divided into 4 tasks. The goals for the first year for each task are listed below:
Task 1: CGH's
(1) Develop improved encoding algorithms, for high efficiency, low F#, large deflection angle CGH's. (2) Design, fabrication and testing of prototype CGH's. (3) Development of CAD software for multichip module holographic interconnects. (4) Design and fabricate CGH for system 1.

Task 2: Photodetectors.
(1) Develop improved photodetector designs. (2) Perform computer simulations of detectors and detector circuitry. (3) Fabrication and testing of experimental photodetector chips for system 1. (4) First year goal: fabrication of Si photodetectors with rise times < 3 nsec.

Task 3: Laser Diode Research
(1) Development and fabrication of edge-emitting laser array chips for system 1. (2) Simulation and development of surface-emitting lasers.

Task 4: System Integration
(1) Evaluate materials which possess appropriate mechanical, electrical, optical and thermal properties, for the translator chip substrate. (2) Develop and test methods of bonding Si chips, GaAs chips and laser mirrors with required alignment accuracy. (3) Develop and test methods of aligning CGH's to substrate. (4) Modelling of thermal management techniques.

B. Significant Results in the past year

Work on this project began July 1, 1991. Thus, these results cover the first 3 months of the first year.

Task 1: CGH's
A prototype CGH for a single 1:1 connection at an angle of 0 degrees was fabricated. This CGH had an F# of 1.0 and diffraction efficiency of 89%. This is the highest reported efficiency for an F/1 CGH. (An F/1 CGH is needed to collect most of the light diverging from the laser.) Several CGH encoding algorithms were developed, including (1) an efficient algorithm for converting holograms designed with CODE V to discrete functions with higher diffraction efficiency than previous approaches and (2) a modification of the IDO encoding algorithm to apply to interconnects with large deflection angles. CGH's designed with these methods have been incorporated into a prototype holographic structure that will be fabricated shortly. The holographic structure includes subholograms designed with various encoding methods and deflection angles. An in-house data format for CGH's for a CAD system has been developed. A CAD framework based on this data format that allows conversion between various standard formats is also under development.

Summary:
- Prototype CGH for 1:1 connection fabricated
- Several CGH encoding algorithm developed

- Design of holograms to test encoding methods has been completed
- CAD data format developed. CAD framework is under development.

Task 2: Photodetectors.
Several improved photodetector designs have been developed, including a design based on an ion-implanted intrinsic well and the use of a grating on the surface of the detector. These designs and several others have been incorporated into a silicon optoelectronic test chip. The chip has been fully designed and partially simulated. During the next 1 -2 months the simulations will be completed and the chip will be fabricated at MCNC.

Summary:
- Development of several improved detector designs
- Design of CMOS photodetector chip to test detector designs and circuits

Task 3: Laser Diode Research
During this period the design and layout of edge-emitting laser array chips has been completed. The laser chip dimensions will be 300 μ x 1 cm x 300 μm. The center-to-center distance between lasers will be 250 μm. The precise location and layout of the underbump metallurgy has also been specified. We anticipate the completion of the first laser array chips by the end of November.

Task 4: System Integration
The structure of the first test system MCM was developed. The MCM substrate will be quartz. Holograms will be fabricated on one side by deposition of silicon, and electrical connections (Al/PI) will be fabricated on the opposite side. This substrate will define the position of the components with respect to one another. Mirrors will be used to redirect laser output from the edge emitting lasers to the holograms. These parts will be fabricated by anisotropically etching silicon such that the resultant features contain a beveled edge (54.7 degrees w.r.t. the surface). The reflector surface will be coated with gold and the mirror will be positioned on the substrate using C4 technology. Electrical connection between the components and the substrate will be obtained using C4 joints. These solder joints will also provide the component to substrate alignment. This alignment is a critical aspect to the success of this project. The solder will be deposited on the substrates of the lasers, detectors and mirrors. These devices will be fabricated such that they have pads of solder-wettable material that are of precise dimensions. The solder bumps fabricated on the substrate will be of two different heights (to obtain maximum transmittance of the laser output) and will be composed of eutectic Pb/Sn solder.

Summary:
- Substrate and material choices
- Development of fabrication techniques and process sequences
- Developed method for alignment of the holograms to the bonding pads
- Determined method of redirecting output of laser beam
- Choice of eutectic Pb/Sn solder for low temperature joining
- Determination of suitable underbump metallurgy
- Process design/layout to obtain different bump heights

C. Plan's for next year's Research

By Sept. 30 1992, we will be 3 months into year 2 of this project By this date we plan to achieve all of the research goals for year 1 outlined in section A, as well as to make significant progress toward completion of many of the year 2 goals. More specifically, we plan to (1) complete the design, fabrication and assembly of the test system MCM and (2) Complete the fabrication of the holograms and detector chips for the System 1 prototype.
We plan to complete fabrication of the CGH's, the photodetector chips, and laser chips for the test system by mid December 1991. By March, 1992 we plan to have the test system MCM fully assembled and tested. Work on the System 1 MCM will begin in January of 1992. We plan to fabricate the holograms, detector chips and laser chips by July, 1992.

D. List of Publications/Reports/Presentations

1. Papers Published in Refereed Journals

2. Non-Refereed Publications and Published Technical Reports

3. Presentations

a. Invited

M. R. Feldman, "Holographic Optical Interconnects for Multichip Modules," To be presented at NEPCON West 1992

b. Contributed

1) W. H. Welch, J. E. Morris & M. R. Feldman, "Design and Fabrication of Radially Symmetric Computer Generated Holograms," OSA Annual Meeting, 1991
2) M. R. Feldman & I. Turlik, "Holographic Optical Interconnects for VLSI Multichip Modules" Presented at VLSI & GaAs Workshop, 1991
3) M. Y. A. Raja & Y. Aktas, "Highly Directional Spontaneous Emission from Periodic Quantum Wells" OSA Anual Meeting, 1991

4. Books (and sections thereof)

The following book chapters are under development:

1) Design Issues in Optical Processing
Editor: John N. Lee
Publisher: Cambridge University Press
Contribution: Chapter 6, Comparison Between Holographic and Guided-wave Interconnects for VLSI Multiprocessor Systems

Enclosure (2)

2) Optical Interconnection - Current Status and Trends
Editor: Drs. H. John Caulfield and Christopher S. Tocci
Publisher: Artech House Publishers
Contribution: Part 2, Motivational Aspects: An Introduction to the Current I/O Problem

E. LIST OF HONORS/AWARDS

Name of Person Receiving Award	Recipient's Institution	Name, Sponsor and Purpose of Award

Enclosure (3)

F. Participants and their Status

Name: Dr. Michael Feldman
Status: Faculty, UNCC

Name: Dr. Yasin Raja
Status: Faculty, UNCC

Name: Iwona Turlik
Status: Faculty, UNCC

Name: Gretchen Adema
Status: Researcher, MCNC

Name: Dr. Paul Magill
Status: Researcher, MCNC

Name: Jim Morris
Status: Graduate Student

Name: Hudson Welch
Status: Graduate Student

Name: John Childers
Status: Graduate Student

Name: Muana Nakkar
Status: Graduate Student

Name: Niang Hangzo
Status: Graduate Student

G. Other sponsored research during FY90:

Title: Computer Generated Holograms for Semiconductor Laser Diodes
Sponsor: AMP, Inc., Winston-Salem, NC.
Amount: $28,000
Time Charged: AcademicYear: 5%
Summer: 22%
Start Date: Nov. 1990
End Date: Nov. 1991

Title: Computer Generated Holograms for Optical Disk Head
Sponsor: Eastman Kodak Company, Rochester, NY.,
Amount: $6,500
Time Charged:
AcademicYear: 5%
Summer: 5%
Start Date: Jan. 1991
End Date: July 1991

Title: Iterative Encoding Methods for Computer Generated Holograms
Sponsor: Army Research Office
Amount: $15,000
Time Charged:
AcademicYear: 5%
Summer: 5%
Start Date: April 1991
End Date: December 1991

Title: Design of Optical Components for a Solid-State Bar Code Reader
Sponsor: Hand Held Products Charlotte, NC.
Amount: $5,700
Time Charged:
AcademicYear: 5%
Summer: 2%
Start Date: June 1991
End Date: Oct. 1991.

H. SUMMARY OF FY91 PUBLICATIONS/PATENTS/PRESENTATIONS/HONORS/PARTICIPANTS (Number Only)

	ONR	non ONR
a. Number of Papers Submitted to Referred Journal but not yet published:	0	1
b. Number of Papers Published in Refereed Journals:	0	0
c. Number of Books or Chapters Submitted but not yet Published:	1	0
d. Number of Books or Chapters Published:	0	0
e. Number of Printed Technical Reports & Non-Referred Papers:	0	1
f. Number of Patents Filed:	0	0
g. Number of Patents Granted:	0	0
h. Number of Invited Presentations at Workshops or Prof. Society Meetings:	1	1
i. Number of Contributed Presentations at Workshops or Prof. Society Meetings:	0	0
j. Honors/Awards/Prizes for Contract/Grant Employees: (selected list attached)	0	0
k. Number of Graduate Students and Post-Docs Supported at least 25% this year on contract grant:	4	2
Grad Students: TOTAL	4	2
Female	1	1
Minority		
Post Doc: TOTAL		
Female		
Minority		
l. Number of Female or Minority PIs or CO-PIs		
New Female		
Continuing Female		
New Minority		
Continuing Minority		