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Quarterly Progress Report
for

**Design and Packaging of Fault Tolerant
Optoelectronic Multiprocessor Computing Systems**

Sponsored by
Defense Advanced Research Projects Agency
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Grantee

The Regents of the University of California
University of California, San Diego
La Jolla, CA 92093

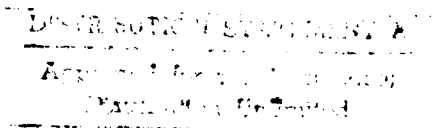
Reporting Period:
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1. Program Goal

The goals for the the project are primarily to develop the packaging technology, by integrating silicon CMOS chips, detectors, modulators, diffractive optical elements and/or photorefractive nonlinear crystals in a packagable design. On the secondary basis, we would model package systems and establish a data-base for CAD, and investigate the design of fault tolerant optoelectronic systems. The results of our investigation for this quarter are summarized below.

2. Progress Summary

2.1 Opto-Electronic Packaging

We have been developing an approach for solving the alignment problem between microstructures on different sides of an optical substrate. This technique will allow us to build compound and complex optical systems for compact optoelectronic packages. The basic idea is to use fresnel lenses with the focal length equal to the thickness of the substrate to transfer positional information from one side of the substrate to the other. The procedures of this alignment is as follows: An e-beam writer is used to print several of these alignment lenses on the peripheral together with the first set of microstructures at the center on one side of the substrate [Fig.1.(a)]. Photoresist is spun on the backside of the substrate. A collimated laser beam is focused onto the photoresist using the fresnel lenses that were fabricated in the first step [Fig.1.(b)]. The focused beams expose the photoresist at points exactly on-axis with the lenses, resulting in an exposure of the photoresist on the backside [Fig.1.(c)]. This photoresist pattern of the focal spots is then etched into the glass substrate [Fig.1.(d)]. The substrate is then cleaned and a metal layer is evaporated onto this side [Fig.1.(e)] to create a ground plane for the e-beam writer. The e-beam writer is now able to locate the pitches/punctures in the substrate [Fig.1.(f)] because the cambridge e-beam exposure system used at UCSD can carry out a routine to find the center of gravity of the

transferred focal spots . The experimental results are shown in Fig.2. The transfer of the alignment mask from one side of a 1.5 mm thick substrate to the other side was accomplished. These transferred points can be immediately used to align features which are supposed to be printed on the backside of the substrate. The alignment accuracy of this approach is mainly determined by the accurate controlling the illuminating angle of the Argon laser beam (90° to the normal of the surface) during the exposure of the photoresist (Fig.1(b)). This angle can be controlled well within $\pm 0.03^\circ$, resulting in an alignment accuracy of $\pm 0.8 \mu\text{m}$. [Ref.1, Appendix A]

As the first packaged system design study, we have chosen a reconfigurable optical interconnection system known as the Correlation Matrix Tensor Multiplier (CMTM). Fig.3. (a) shows the optical table setup of the CMTM that was previously demonstrated at UCSD [Ref.2]. Fig.3.(b) shows the packaged version of CMTM that we are currently implementing. Two linear CGHs and two Fourier Transform (FT) CGHs are being designed to be integrated with a LiNbO_3 photorefractive crystal (PRC) on one surface of a glass substrate of dimension 40x40x26 mm for 5x5 array interconnections. The L-shaped arrangement of components prevents the Fresnel reflected light from the crystal/glass interface going to the detector. This results in an improved SNR over the simpler linear arrangement. The system is also designed to take advantage of the e-beam lithographic alignment accuracy ($0.1 \mu\text{m}$) by aligning all of the optical elements on the same side of the substrate. System considerations such as thickness of the substrate, off-axis angle, and size of input pixels were incorporated into a design program to allow tradeoffs between these system parameters and device parameters such as minimum feature size and the number of phase levels. In order to eliminate the astigmatism that is so prevalent in these types of off-axis optical systems, we utilized the Orthogonal Cylindric Diffractive Lens (OCDL) for the FT CGHs. Further improvements in CGHs design include using the more general polynomial aspheric phase func-

tion in Code V to eliminate residual spherical and coma aberrations. Fig.4 shows the impulse response of the system before and after Code V optimization. Currently, work is being conducted to generate the e-beam data for these general aspheric type diffractive optical elements. [Ref.3, Appendix B]

Research for the next quarters will concentrated on: (1) fabrication of components for the CMTM package; (2) investigation of the alignment and stacking of several diffractive elements and substrates for low f-number lenses; (3) investigation of the application of PRC for self-alignment in packaging.

2.2 Opto-Electronic CAD

The first step for CAD modeling of a module or a system, which is composed of optical (CGH, PRC) and optoelectronic (processing elements with transceivers) components, is to generate a model for each component. A standard format of the netlist has been established for optoelectronic interconnection system design (see the Appendix C). The netlist format accounts for the following aspects in system design: (1) Imperfect array of processing elements due to yield issues. It is important to take into account possible faults as early as possible at the design stage. The ability of using imperfect components will also significantly reduce the manufacturing cost. (2) Intra-module placement. In order to get a compact physical design for the module, an optimum mapping from logical components to physical components inside a module is necessary. This takes relative positions of each components (processing elements, CGH ...) inside a module into consideration as well as short distance electronic connections. (3) Inter-module place and route. The relative placement of each module within a system is important to reduce the volume of the packaged optoelectronic system. The format provides the system designers with the ability to specify the module layout and routing. (4) Optical versus electrical interconnects. This format provides the selections of both optical and electronic type interconnections that the designers would like to choose.

In order to meet the requirements of generating different CGH arrays based on given interconnection netlist and packaging scheme, we have also extended our CGH CAD design program to handle this design in a modular fashion. In our modular design program, an object-oriented approach is used to build complex CGH arrays from a few basic primitives, in which, an object is an individual holographic element. Fig.5 shows a users' menu of an array of a few kinds of HOEs. To make interconnection CGHs, we take a netlist as the input; from the netlist and the chosen packaging scheme, we calculate the position and offsets of the CGHs that will be used to create the interconnections. An example of designing a 2D perfect shuffle interconnect network is shown in Fig.6. Fig.6(a) shows an assumed optical scheme for a 2D perfect shuffle interconnection. Fig.6(b) shows its netlist input. From these, we can calculate the offset for each lens. Fig.6 (c) shows the array of the interconnect CGH for the 2D perfect shuffle.

In order to create a CAD system in which CGH arrays mentioned above can be generated automatically, we are going to create a generalized e-beam fringe writing algorithm for more types of HOEs next quarter.

2.3 Fault Tolerance and Testing in Opto-electronic Computing

We have been investigating the twin butterfly interconnection network which exploits random permutations to reduce contention and improve fault tolerance. Fig.7 illustrates how a twin butterfly provides alternate routes around a faulty switching element, as compared to a "fat" or dilated butterfly that has equivalent hardware cost but offers no fault tolerance. Some important considerations in switching element design for twin butterfly are: (1) test the switching elements before packaging to ensure good system yield, and (2) test the packaged system to detect and recover from component failures during operation. These functions are added to the normal routing functions required for a nonblocking switch

such as handshaking and buffering.

Fig. 8 shows the switching element design to realize the routing functions. During each cycle data packets could arrive and leave a switching element through the data modulators and detectors. We are time-multiplexing the modulator output so that few modulators need be used to improve the scalability of the network. Handshaking signals are transmitted and received by the CTS ("clear-to-send") modulators and detectors. Two counters in the block labeled sequencing logic synchronizes all the events in other blocks. We have added a pair of detectors to receive control signals that includes clocking and switching between different modes of operation(initialization, testing, and routing). The testing additions to support fault tolerant operation will be the primary agenda for the coming quarter.

Reference

- [1] W. Daschner, R. Stein, and S. H. Lee, "Alignment and assembly Of diffractive elements for optical system packaging", submitted to OSA Annual '92 Meeting at Albuquerque, N.M..
- [2] J. E. Ford, Y. Fainman, and S. H. Lee, "Array interconnection by phase coded optical correlation", Opt. Lett. **15**, 1088-1090(1990).
- [3] H. Takahashi, D. Zaleta, J. Ma, J. E. Ford, Y. Fainman, and S. H. Lee, "Packaged optical interconnection system based on correlation matrix-tensor multiplier algorithm", submitted to OSA Annual '92 Meeting at Albuquerque, N.M..

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Statement A per telecon William Miceli
ONR/Code 1264
Arlington, VA 22217-5000

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Accession For	
GRAB	☒
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Unpublished	☐
Classification	
By	
Distribution/	
Availability Codes	
Avail and/or	
Special	
A-1	

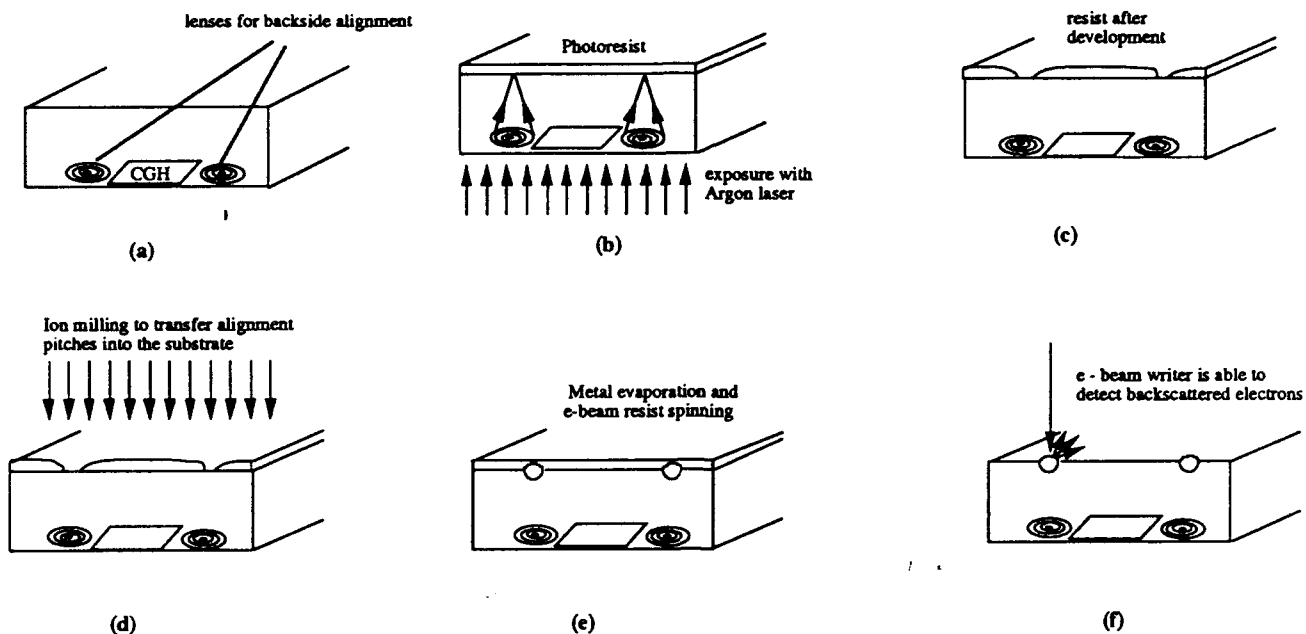


Fig.1. The procedures for the alignment of microstructures on opposite sides of the optical substrate with respect to each other.

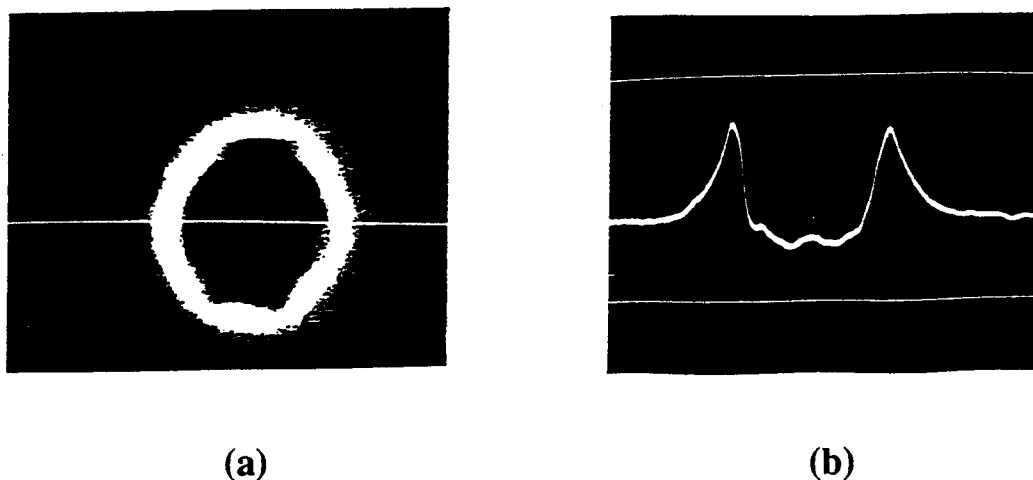


Fig.2. Experimental results of transferring the alignment mask from one side of the substrate to the other side. (a) SEM microphotograph of the edge of the etched alignment hole taken from the e-beam writer. The horizontal line shows scan direction for lock on routine of Cambridge e-beam exposure system. (b) Center of the two outer slopes of the intensity of backscattering electrons is used to find center of gravity of the hole.

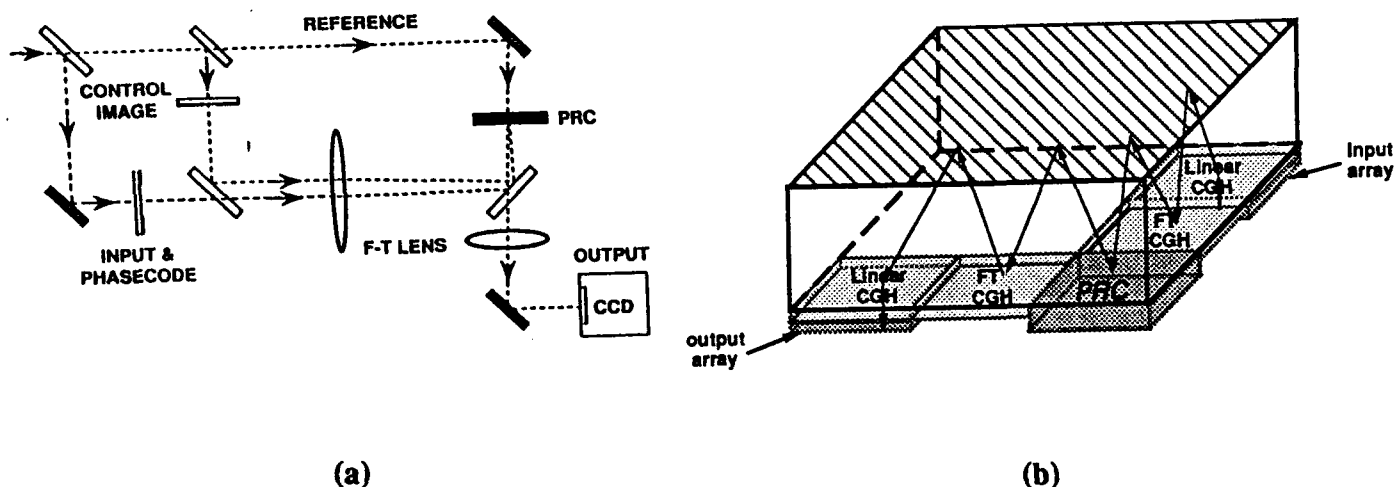


Fig.3. Original table setup and its packaged version of CMTM system. (a) Original table setup CMTM system. The control image is Fourier transformed into a photorefractive crystal (PRC) and is recorded by interfering with a reference beam. In the phase of interconnection, the phase coded input is Fourier transformed into the PRC, and the inverse Fourier transform of the reconstruction produces the output which is the correlation of the input with the control image. (b) Packaged version of the CMTM system. The Fourier transformed control image is pre-recorded in the PRC. The phase coded input is first bent to a certain angle by a linear CGH, and then is Fourier transformed by a FT CGH into the PRC. The reconstruction is Fourier transformed and then bent again to be normal to the output detector array.

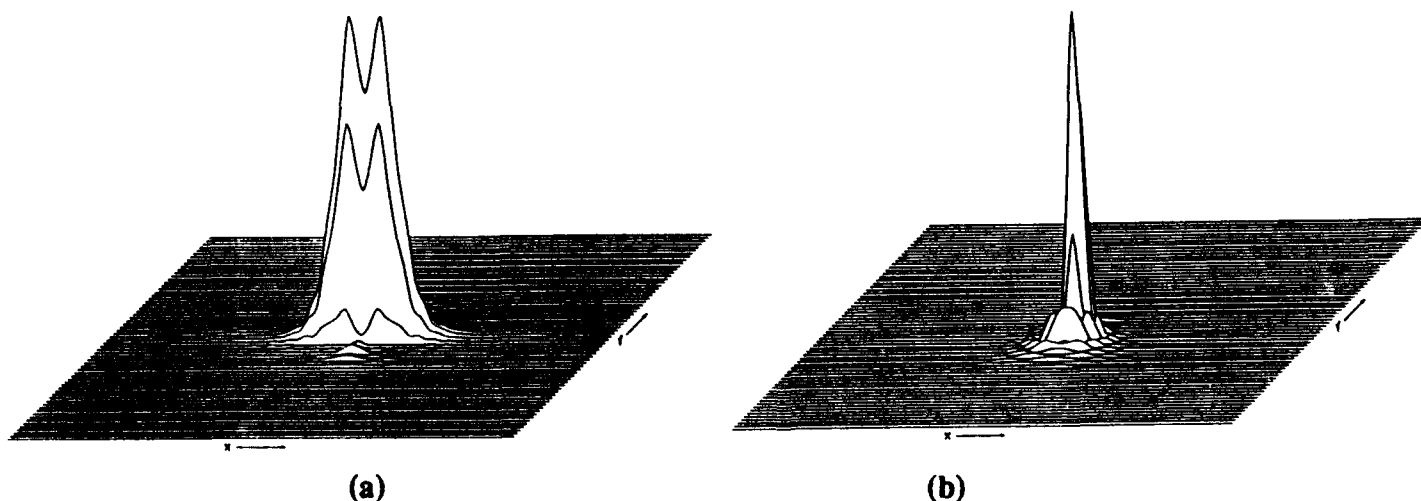


Fig.4. The impulse response of the packaged CMTM system. (a) Before Code V optimization, the diameter of the circle with 90% energy encircled is $59.0\text{ }\mu\text{m}$. (b) After Code V optimization, the diameter of the circle with 90% energy encircled is $9.4\text{ }\mu\text{m}$.

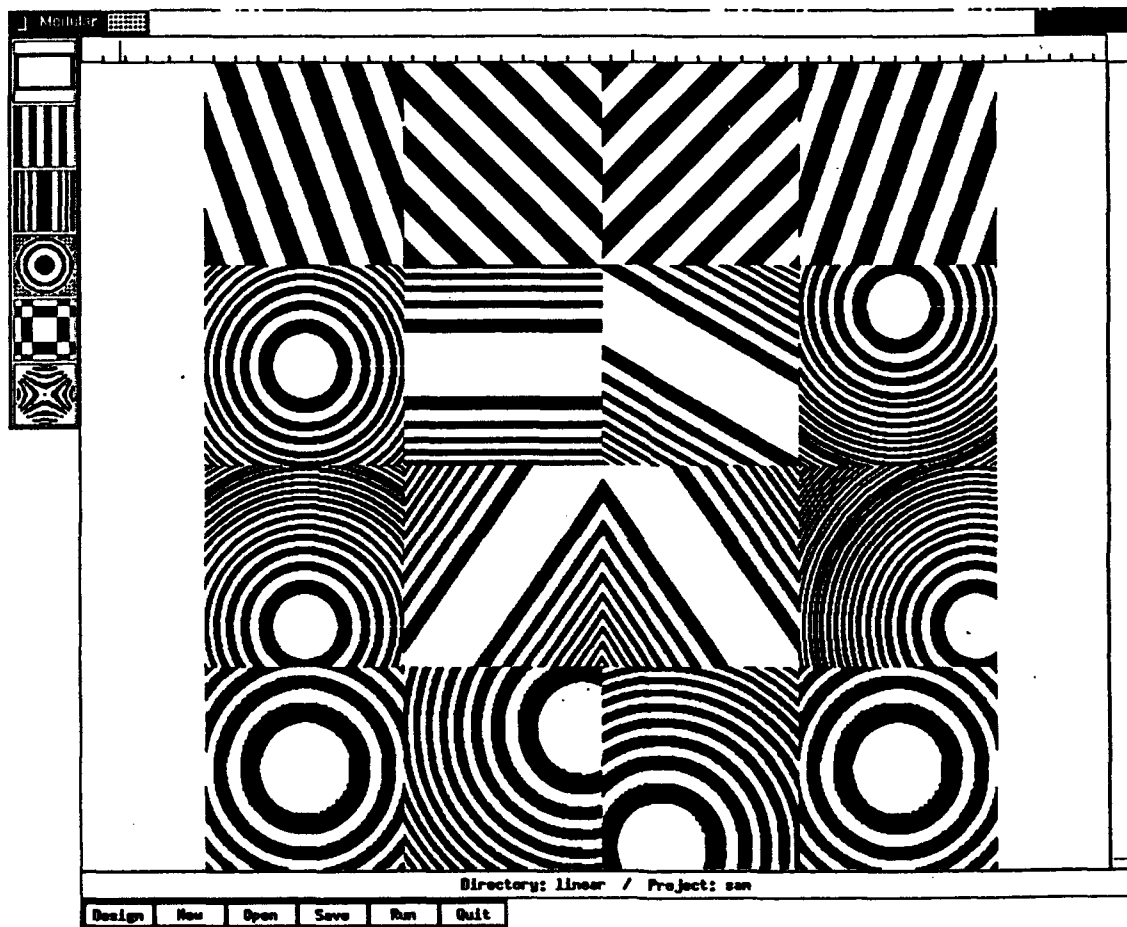
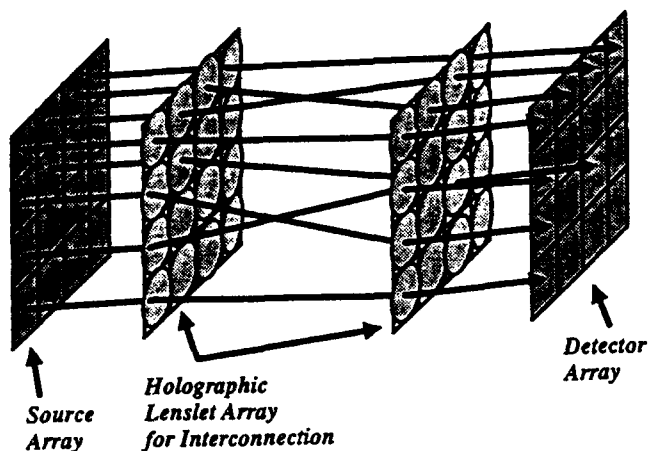


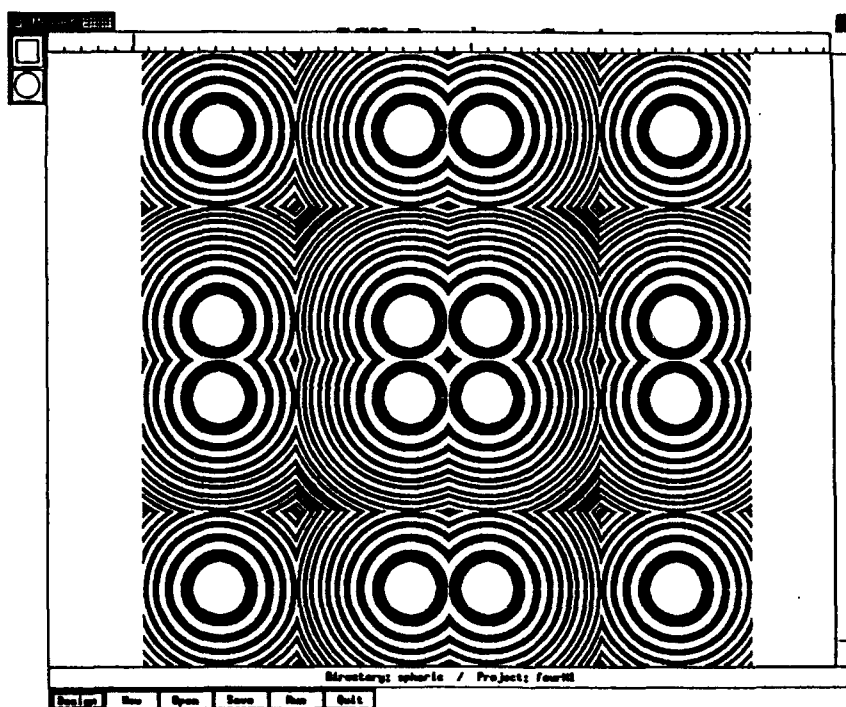
Fig.5. A users' menu (on the left) and a design layout which shows an array of different type of holographic elements generated by our new modular design program.



S0_0:datam	D0_0:datad	0	S(0,0)	■	■	D(0,0)
S0_1:datam	D0_2:datad	0	S(0,1)	■	■	D(0,1)
S0_2:datam	D0_1:datad	0	S(0,2)	■	■	D(0,2)
S0_3:datam	D0_3:datad	0	S(0,3)	■	■	D(0,3)
S1_0:datam	D2_0:datad	0	S(1,0)	■	■	D(1,0)
S1_1:datam	D2_2:datad	0	S(1,1)	■	■	D(1,1)
S1_2:datam	D2_1:datad	0	S(1,2)	■	■	D(1,2)
S1_3:datam	D2_3:datad	0	S(1,3)	■	■	D(1,3)
S2_0:datam	D1_0:datad	0	S(2,0)	■	■	D(2,0)
S2_1:datam	D1_2:datad	0	S(2,1)	■	■	D(2,1)
S2_2:datam	D1_1:datad	0	S(2,2)	■	■	D(2,2)
S2_3:datam	D1_3:datad	0	S(2,3)	■	■	D(2,3)
S3_0:datam	D3_0:datad	0	S(3,0)	■	■	D(3,0)
S3_1:datam	D3_2:datad	0	S(3,1)	■	■	D(3,1)
S3_2:datam	D3_1:datad	0	S(3,2)	■	■	D(3,2)
S3_3:datam	D3_3:datad	0	S(3,3)	■	■	D(3,3)

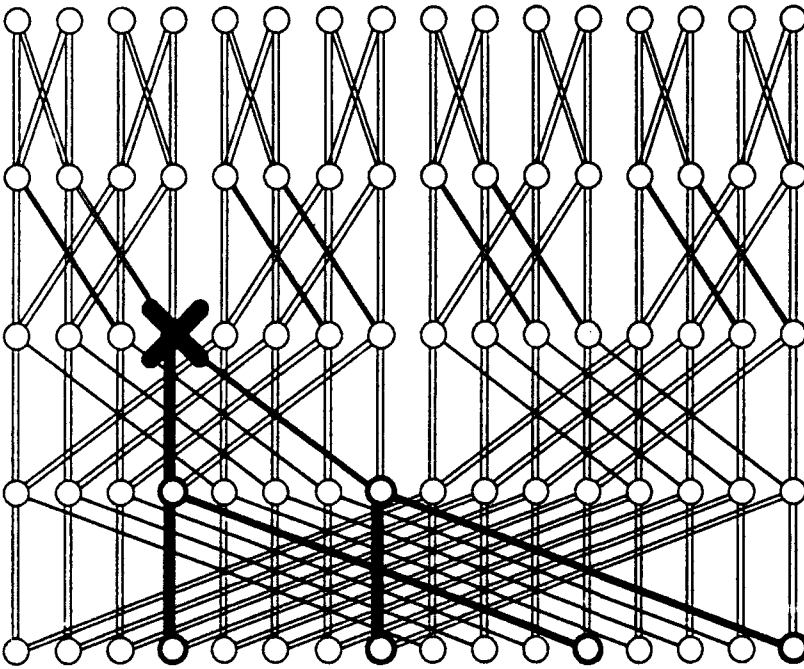
(a)

(b)

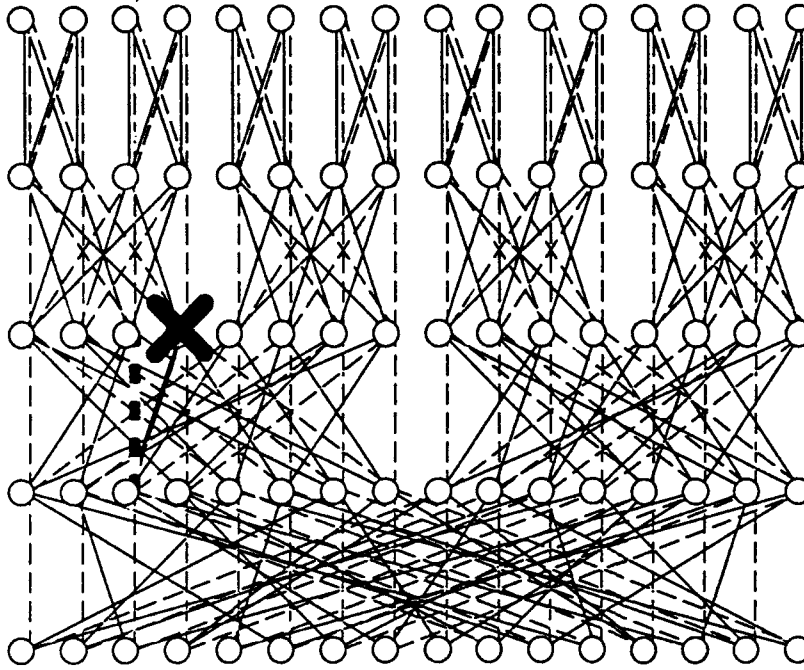


(c)

Fig.6. An example of CAD design of a 2D perfect shuffle interconnect network.
(a) System layout. (b) Netlist. (c) CGH array



(a)



(b)

Fig. 7. The comparison of fault tolerant properties between a fat butterfly and a twin butterfly. (a) A fat butterfly, it can tolerate single link failures since all links are duplicated, but cannot handle the more severe switching element failure. A faulty node at i th stage could propagate backward to blocks 2^i inputs. (b) A twin butterfly, the solid lines represent the regular butterfly, while the dash lines represent the permuted butterfly. Messages can route around faulty switches to mask the fault. It could take as many as 2^i faults at i th stage to completely block an input.

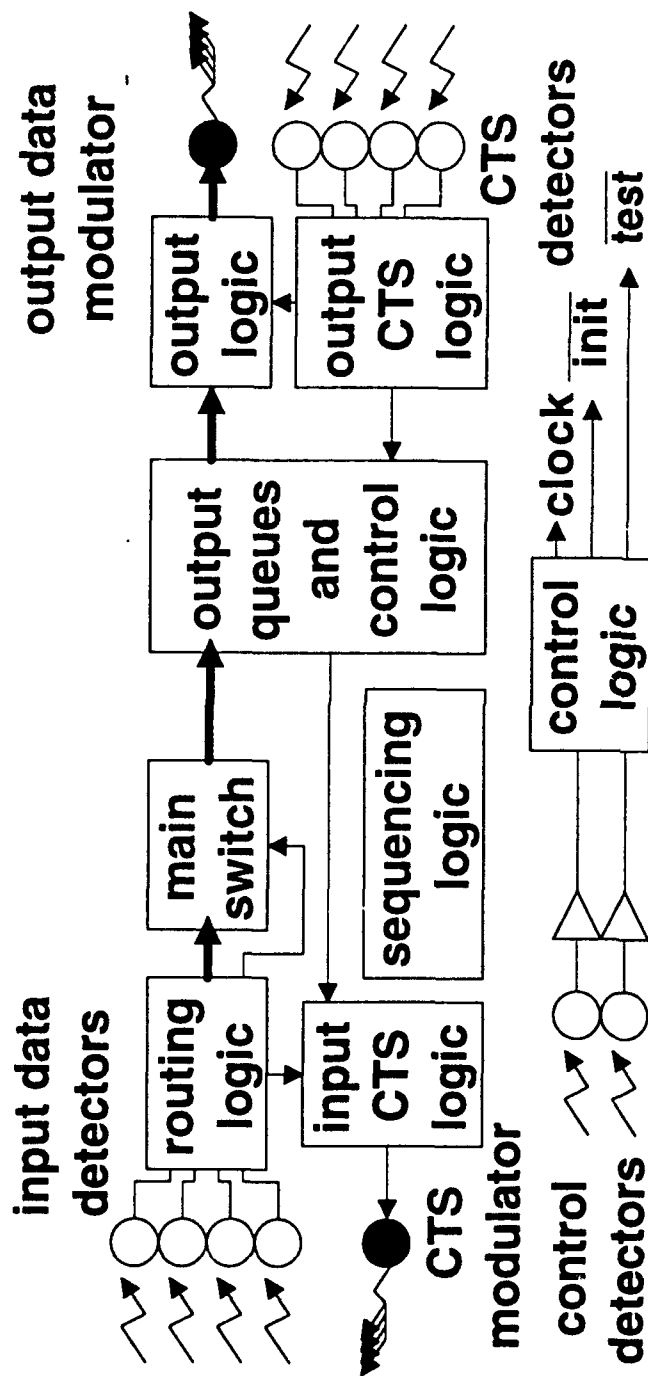


Fig.8. Block diagram of twin butterfly switching element design. This design uses pipelining to improve throughput. It has three operations modes: initialization, normal routing, and testing, toggled by the signals received by the control detectors. During test modes it will mask detector failures and reconfigure output stage to avoid faulty switching elements.

Appendix A

Summary submitted to OSA Annual '92 Meeting

Alignment and Assembly of Diffractive Optical Elements for Optical System Packaging WALTER DASCHNER, ROBERT STEIN AND SING H. LEE University of California San Diego - Free-space optical interconnects for microelectronics and multiprocessor parallel computing systems offer better scalability because less silicon area will be occupied by interconnections, faster clock speed and higher bandwidth at power levels comparable to pure electronic systems. For stability and ruggedness optoelectronic systems that combine optics with electronics based on free space optical interconnection, need to be packaged. In packaging these types of systems, diffractive optical elements (DOEs) are often used because their fabrication is compatible with VLSI fabrication and they can be flexibly designed by computer. The volume of the packaged system depends on the f-number of the DOE utilized in the system. The smaller the f-number, the more compact the packaged system. Lower f-number DOEs can be obtained by stacking more than one DOE together. Stacking more than one DOE together also helps to achieve larger diffraction angles to facilitate longer distance interconnects. The problems to be solved in stacking more than one DOE together are (a) accurate alignment between DOEs on the opposite sides of one substrate or between DOEs on separate substrates, (b) bonding or assembly of separate substrates. In this presentation, the alignment and assembly procedures for stacking more than one DOE together will be discussed, and the experimental results shown.

Appendix B

Summary submitted to OSA Annual '92 Meeting

Packaged optical interconnection system based on correlation matrix-tensor multiplier algorithm. H. TAKAHASHI, D. ZALETA, J. MA, J. E. FORD, Y. FAINMAN, S. H. LEE. UC-San Diego. --- A unique method to achieve high fanout optical interconnections based on correlation matrix-tensor multiplier (CMTM) algorithm has recently been demonstrated.¹ We present a new packaged version of this optical system that is amenable to integration with opto-electronics. In this system, a random phase-encoded input array is optically correlated with a recorded control pattern which stores the pre-determined interconnections utilizing photorefractive four-wave mixing. A random phase plate, a LiNbO₃ crystal, and two computer-generated holograms (CGH) have been integrated on one surface of a glass substrate of dimensions 80x80x44 mm. The CGHs (12 mm aperture) are designed by Code-V and fabricated using direct-write e-beam lithography. The correlated output is observed by a CCD camera. Optical interconnection between 5x5 arrays is demonstrated. Reconfiguration between the pre-stored interconnections is possible by using wavelength multiplexing to store different control patterns in the photorefractive crystal. Details of the system design and experimental results are described.

1. J.E.Ford, Y.Fainman, and S.H.Lee, "Array interconnection by phase coded optical correlation," Opt.Lett.15,1088-1090(1990).

Appendix C

Optoelectronic Netlist Format Version

documentation section

This section stores the miscellaneous information about this design.

*DOC
AUTHOR Joe Smith
CREATED 01/01/92
MODIFIED 03/03/92
PROJECT Cray-YMP-OE
etc.

virtual grid section

This section defines the virtual coordinate space. Since we are assuming a regular array of modules, this is taken to correspond to the total number of modules fabricated.

*GRID
X 16
Y 16

intra-module placement section

This section details the internal structure of a module, the locations of devices within a module are given in a relative coordinate.

symbollic name, device type (mod, det, reflector, elec), x offset, y offset

*MODULE
X 4
Y 4
clockd D 0 0
clockm M 0 1
datam M 0 2
datad1 D 1 0
datad2 D 1 1
elec E
hoppad R 3 3
etc.

module placement section

This section tracks the current placement or coordinates of the modules.

node name, x, y, fixed or relocatable

*PLACE
S000 0 0 F
S001 0 1 R
S002 0 2 F
etc.
S255 15 15 R

inter-module connection section

This section specifies the logical connection between the devices. The entries are sorted according to the source node. Each line contains a signal in the format: *source node, destination node, link type*. The actual physical distance between two interconnected devices can be computed using the module locations, module size and the offsets of the devices within the modules. Link efficiency, reliability, etc. can be added easily in the future.

*NET
S000:clockm S019:clockd O ← an optical link from the clock modulator of node S000 to
S000:datam S013:datad1 O the clock detector of node S019
S000:datam S017:datad2 O ← a second output from S000:datam indicates fanout > 1
S000:elec S006:elec E ← an electrical link between node S000 and node S006
S001:clockm S012:clockd O
etc.
S007:datam S009:hoppad O ← a long distance optical link from the data modulator of node
S009:hoppad S027:datad1 O S007 to data detector No. 1 of S009 via a hoppad (reflector)

end

*END