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6. AUTHOR(S)

A.I. Akinwande, P. Bauhahn, T. Ohnstein
J. Holmen, B. Speldrich, D. Arch

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Honeywell Sensor and System Development Center
10701 Lyndale Avenue South
Bloomington, Minnesota 55420

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13. ABSTRACT (Maximum 200 words)

We summarize our third quarter progress and discuss fourth quarter plans for the development of an edge emitter based vacuum triode with performance goals of 10 μA/μm emission current density at less than 250V and which can be modulated at 1 GHz for 1 hour. Fabrication of four process runs of field emitter diodes were completed. Initial testing indicates promising results. Current densities of 5 μA/μm were measured on selected devices. Continuous emission for >70 hours was measured on devices with emission currents in the 5 μA range. Maximum currents of 155 μA for 100 μm long devices were also measured; these emission currents are a factor of ten higher than previously measured from an edge device. Design of a triode emitter mask set was completed this quarter and a mask set was ordered. Thermal finite-element-analysis (FEM) of the triode structure indicates that ionic heating from the anode is the principal mechanism for large temperature rises at the emitter edge.

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Quarterly Technical Report

RF Vacuum Microelectronics

4/01/92 - 6/30/92

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10701 Lyndale Avenue South
Bloomington, Minnesota 55420

RF Vacuum Microelectronics
Quarterly Technical Report
4/01/92 - 6/30/92

I. Background

The objective of the RF Vacuum Microelectronics Program is to establish the technology base for the fabrication of practical, high performance gated vacuum emitters and to develop a new class of RF amplifiers based on these vacuum microelectronic emitters. Our technical approach is to utilize thin film technology and surface micromachining techniques to demonstrate an edge emitter based vacuum triode with emission current density of 10 μA/μm at less than 250V which can be modulated at 1 GHz continuously for 1 hour. Figure 1 shows a schematic cross section of the type of our thin film edge emitter approach. Based on our experience with fabricating and testing edge emitter devices, our efforts on this program will be focussed on developing a highly stable, uniform and reliable current emission from the edge. We intend to achieve these qualities by

- use of thin film (200Å) edge emitters with small uniform radius of curvature
- use of refractory metal emitter structure to prevent electromigration and burnout
- use of comb emitter structures to prevent premature emitter burnout during edge formation
- use of current equalization series elements to set bias currents

This program to develop an edge emitter triode started on October 1, 1991. The baseline portion of the program is for 18 months with the above mentioned objectives as goals. Upon successful completion of this phase, an option phase for 12 months can be implemented by DARPA where the objective will be to achieve 10 GHz modulation with the edge emitter device.

II. Technical Progress During Quarter

Key Achievements (4-1-92 to 6-30-92)

- Completed four fabrication runs of diode field emitter devices.
- Demonstrated current densities of up to 5 μA/μm on diode field emitters.
- Demonstrated current emission of up to 155 μA for a single diode field emitter.
- Demonstrated >70 hours continuous field emission at currents greater than 5 μA for a 48 μm long diode field emitter.
- Completed the design of the triode field emitter and ordered masks.
- Carried out thermal FEM analysis on triode emitters showing that ionic heating from anode is responsible for the large temperature increases at the emitter.
- Demonstrated high resistivity polysilicon thin films for current limiters in field emission devices.

III. Technical Progress

III-1 Task 1.

The objective of this task is to develop an edge emitter structure with high emission current and high reliability. The goal is to achieve current density emission of 5A cm^{-2} operating continuously for one hour at a gate voltage less than 250 Volts.

The technical approach is to fabricate field emitter diodes using the comb edge emitter structure shown in Figure 1.0-1. Each comb element has a series resistor for bias stabilization. Several emitter materials and configurations will be used to determine the structure to be used in the vacuum transistor.

During this quarter we demonstrated field emission from thin film edges. The emission currents are a factor of ten higher than previously reported results (150 μA vs 10-15 μA). Emission current density as high as 5 μA / μm of edge width has also been demonstrated. The devices also operated for longer period of time (≈ 70 hours) without burn out than previously reported. We completed four fabrication runs and testing on one of the fabrication runs.

There are three sub-tasks for Task 1 - test structure design, emitter fabrication and emission Testing. We have completed the test structure design sub-task and 50 % of the emitter fabrication and emission testing sub-tasks. A discussion of the past quarter results are as follows:

Sub-Task 1.1 Test Structure Design

The design activity was reported in the last quarterly report. A mask set of the field emitter diodes was procured and it is being used in the fabrication of the field emitter diodes reported here.The mask set has seven device chips and two chips for process monitoring. We plan to make design changes to the mask set to make arrays of edges that will meet the 5A cm^{-2} (equivalent to 10 μA/μm) and 5 mA total current program objective. The new mask set will consist of five layers.

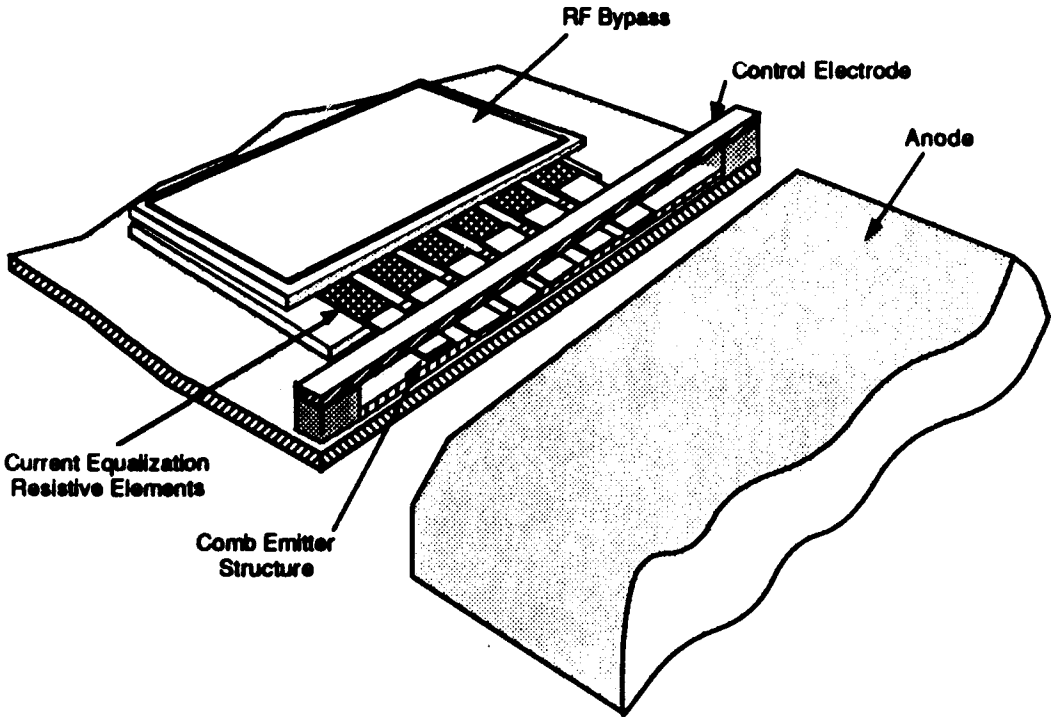
Sub-Task 1.2 Emitter Fabrication

We have completed the fabrication of four runs of edge emitter diodes. A description of the runs and the device or material properties the devices are intended to study is given below.

Run 5316 Q1 - First Diode Run

The objective of this run was to (i) verify the process and masks and (ii) to study the influence of emitter thickness on the performance of the devices. The run consisted of 12 wafers - 9 quartz substrates and 3 silicon substrates with 1.4 μm of thermally grown oxide. The emitters of the devices were split into three groups (i) 200 Å TiW, (ii) 300 Å TiW and (iii) 400 Å TiW each consisting of three quartz wafers and one silicon wafer. The fabrication process is summarized in Figure 1.2-1. The resistors are 2500 Å of sputtered TaN. The process evaluation tests show the resistors have a sheet resistance of 1 MΩ / square. Other process parameters evaluated are metal sheet resistances, insulator leakage currents, breakdown and contact continuity. The final step was the etch of the sacrificial layers and a cavity in quartz. A cavity depth of 0.5 μm was expected after 10 minutes BOE etch. The test results are reported in the next section.

Technical Approach



- **Thin-film (≈200 Å) edge emitters for enhanced emission**
- **Refractory metal comb emitter structure to prevent burn-out**
- **Current equalization with resistive elements to stabilize emission**
- **RF bypass of the current equalization elements to obtain RF gain**
- **Submicron control electrodes for reduced capacitance**
- **Out-of-plane anode**

Figure 1.0-1 Illustration of the vacuum transistor with a comb edge emitter structure and series current equalization elements.

Vacuum Microelectronics

TWO TERMINAL DEVICE

PROCESS OUTLINE

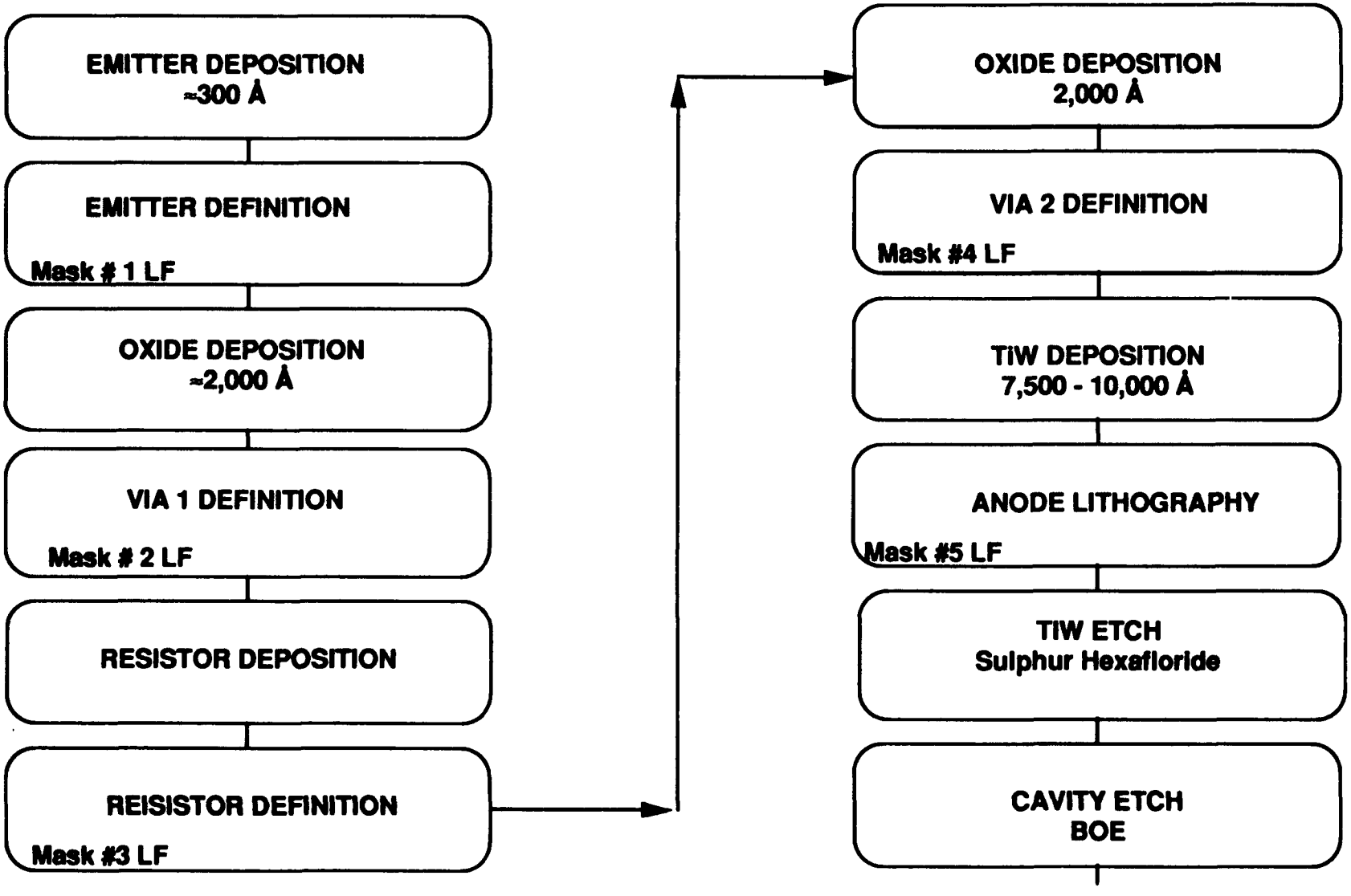


Figure 1.2-1 Process flow for the fabrication of field emitter diode with comb emitters and series current equalization elements.

Run 5316 - Q2 - Second Diode Run

The objective of the run was to study the influence of emitter thickness on the performance of the devices. The run consisted of 12 wafers - 9 quartz substrates and 3 silicon substrates with 1.4 μm of thermally grown oxide. The emitters of the devices were split into three groups (i) 200 Å TiW, (ii) 300 Å TiW and (iii) 400 Å TiW each consisting of three quartz wafers and one silicon wafer. The only difference between this run and the first run is the processing of the contact between the emitter layer and the resistor layer.

Run 5316 Q3 - Third Diode Run

The primary objective of the run was to study the influence of emitter material on the performance of the devices. The run compares three refractory metals which have work functions of about 4.5 eV. - TiW, WNx, WSix. The secondary objective of the run was to compare TaN and sputtered boron doped polysilicon resistors. The run consisted of 12 wafers - 9 quartz substrates and 3 silicon substrates with 1.4 μm of thermally grown oxide. The emitters of the devices were split into three groups (i) 250 Å TiW, (ii) 250 Å WNx and (iii) 250 Å WSix each consisting of three quartz wafers and one silicon wafer. Each group of wafers were further split into two sub-groups. The first sub-group has 2500 Å of TaN resistors and consisted of two quartz wafers and one silicon wafer. The second sub-group consisted of one quartz wafer and had 2500 Å of sputtered boron doped poly silicon. Presently the devices are in testing.

Run 5316 Q4 - Fourth Diode Run

The objective of this run was to (i) study the effect of the emitter thickness on the emitter current and (ii) to study the influence of emitter thickness on the performance of the devices. The run consisted of 12 wafers - 8 quartz substrates and 4 silicon substrates with 1.4 μm of thermally grown oxide. The emitters of the devices are split into four groups (i) 200 Å WNx, (ii) 400 Å WNx (iii) 200 Å WSix and (iv) 400 Å of WSix each consisting of two quartz wafers and one silicon wafer. The resistors were 2500 Å of sputtered TaN. The process evaluation tests show the resistors have a sheet resistance of 1 MΩ / square. The run has been completed and will be tested next quarter.

Sub-Task 1.3 Emission Testing

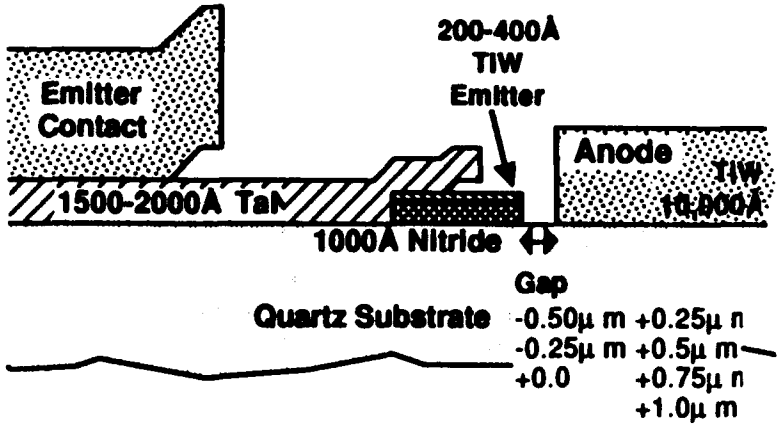
We started electrical tests, evaluation and analysis of the field emission devices from the first diode and the third diode runs. Most of the data reported here are for the first run.

5316-Q1 - First Diode Run.

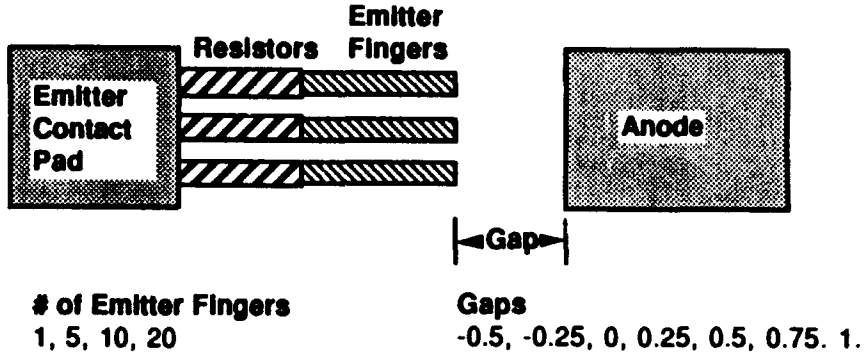
The fabrication conditions have been summarized above. Three wafers with TiW emitters were etched in BOE to remove the sacrificial layers and create a cavity in the quartz substrate between the the emitter and the anode. The device cross section after the cavity etch is shown in Figure 1.3-1. The wafers were degreased in (i) heated acetone, (ii) heated isopropyl alcohol and (iii) DI water. The wafers were loaded into the vacuum test chamber and baked in the intro chamber at 110 °C for 1 hour. The wafers were then loaded into the ultra high vacuum chamber (pressure ≈ 5×10^{-9} Torr).

The wafers have the following characteristics

Field Emitter Test Structure



Cross Section of Field Emitter Test Structure



Top View of Field Emitter Test Structure

- Comb structure
- Thin-film emitter
- Thin-film resistor

- Emitter with and without combs
- Emitters with and without resistors
- Novel structures to determine electron trajectory
- Novel structures to determine positive ions or secondary electrons

Figure 1.3-1 Illustration of a completed diode after the etch of the sacrificial layers.

Vacuum Test Chamber

Vacuum Chamber

- All parts compatible with Perkin-Elmer PHI 430 MBE system
- Pressure $\leq 5 \times 10^{-9}$ torr
- 2.75-in ports for micro-manipulators
- Wafer stage capable of X, Y travel ±0.75 in, Z travel 2-in and 360° rotation
- Transfer stage capable of receiving 3-in wafers and heating wafers to 700°C

Data Acquisition

- 386-based data acquisition system
- Keithley 237 power supplies
- Keithley 617 multimeter
- Triax cabling

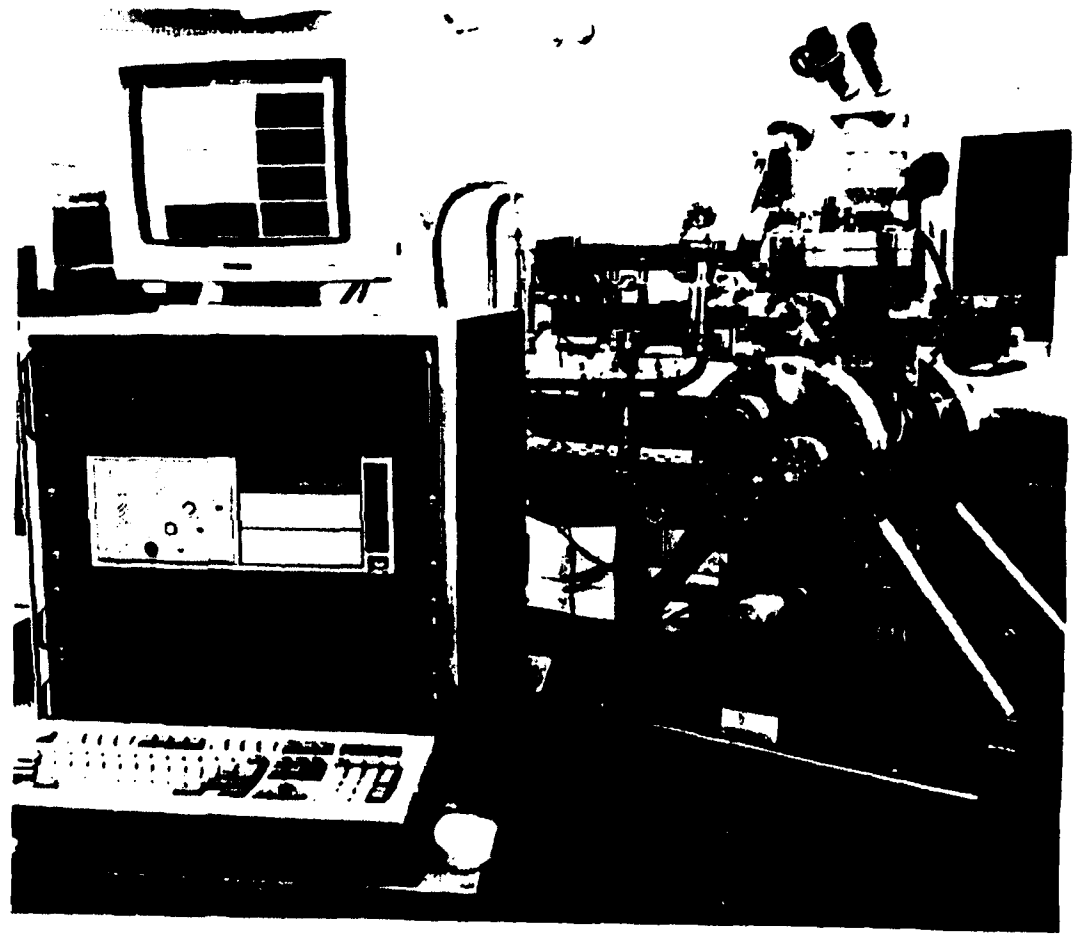


Figure 1.3-2 The computer automated vacuum test station.

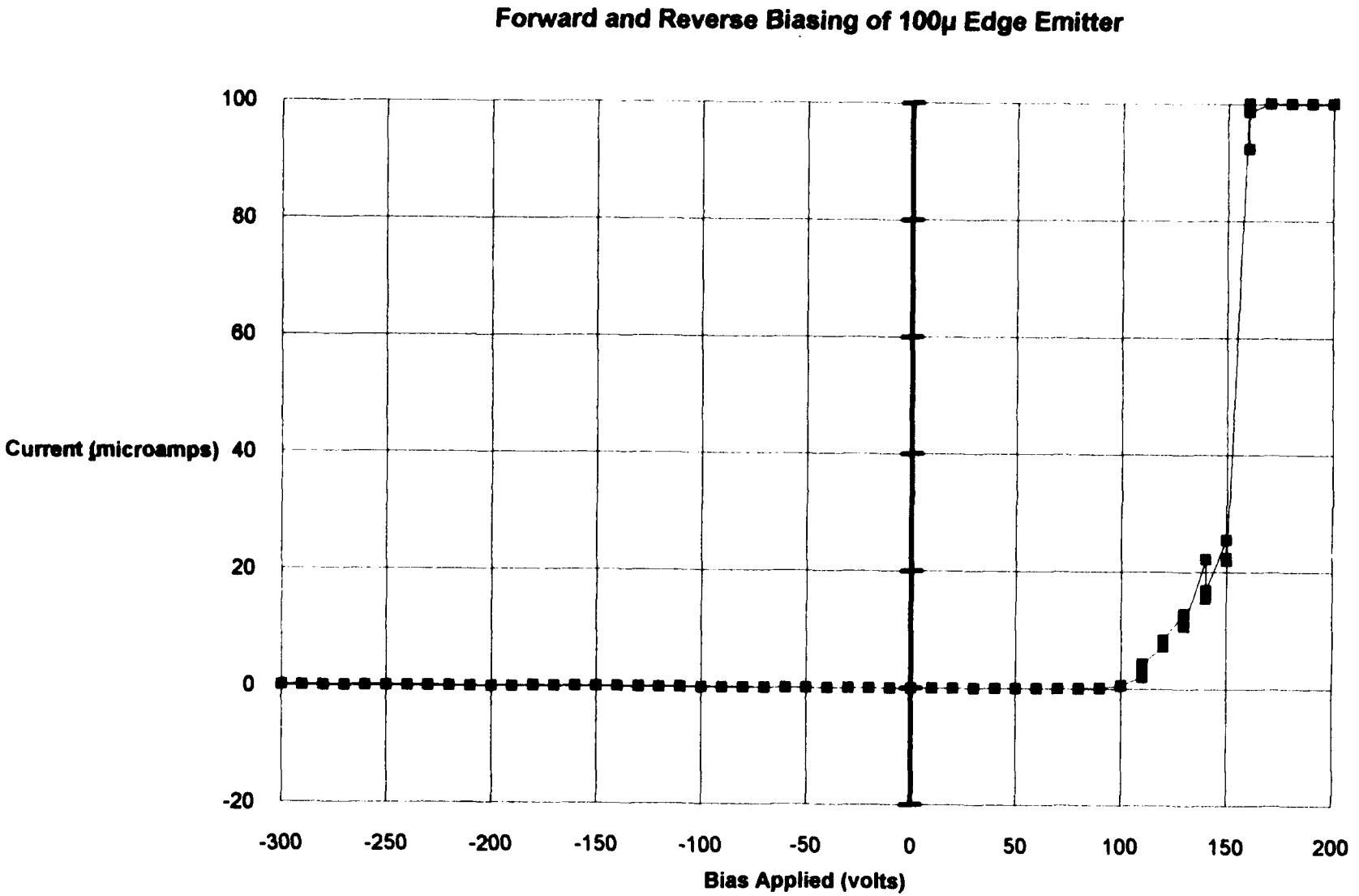


Figure 1.3-3 IV characteristics of an edge emitter diode. The particular device has a width of 100 μm and had been at a current bias of 50 μA for 1000 minutes prior to the measurement of the data shown.

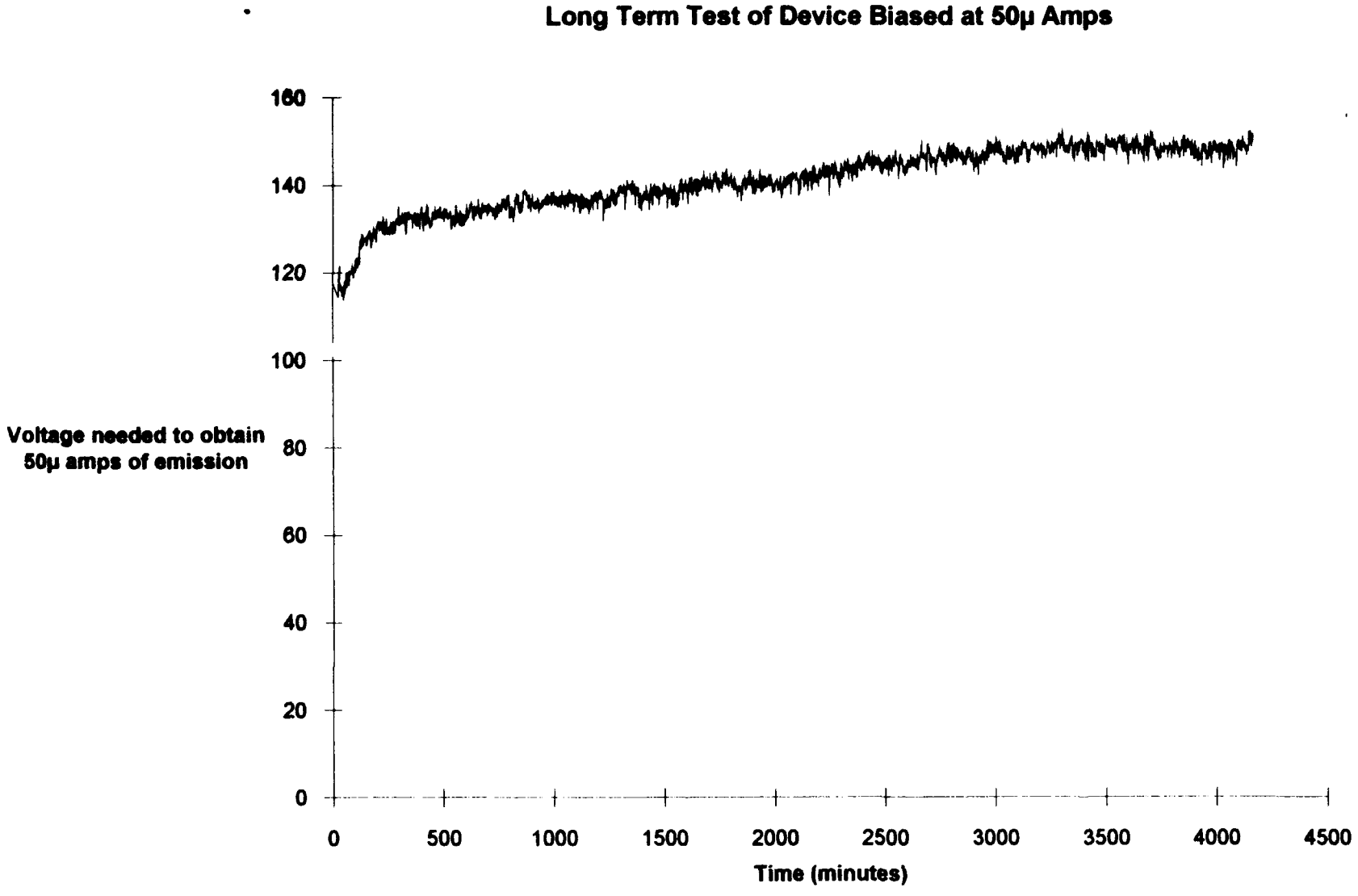


Figure 1.3-4 Long term testing of a 100 µm long continous edge.

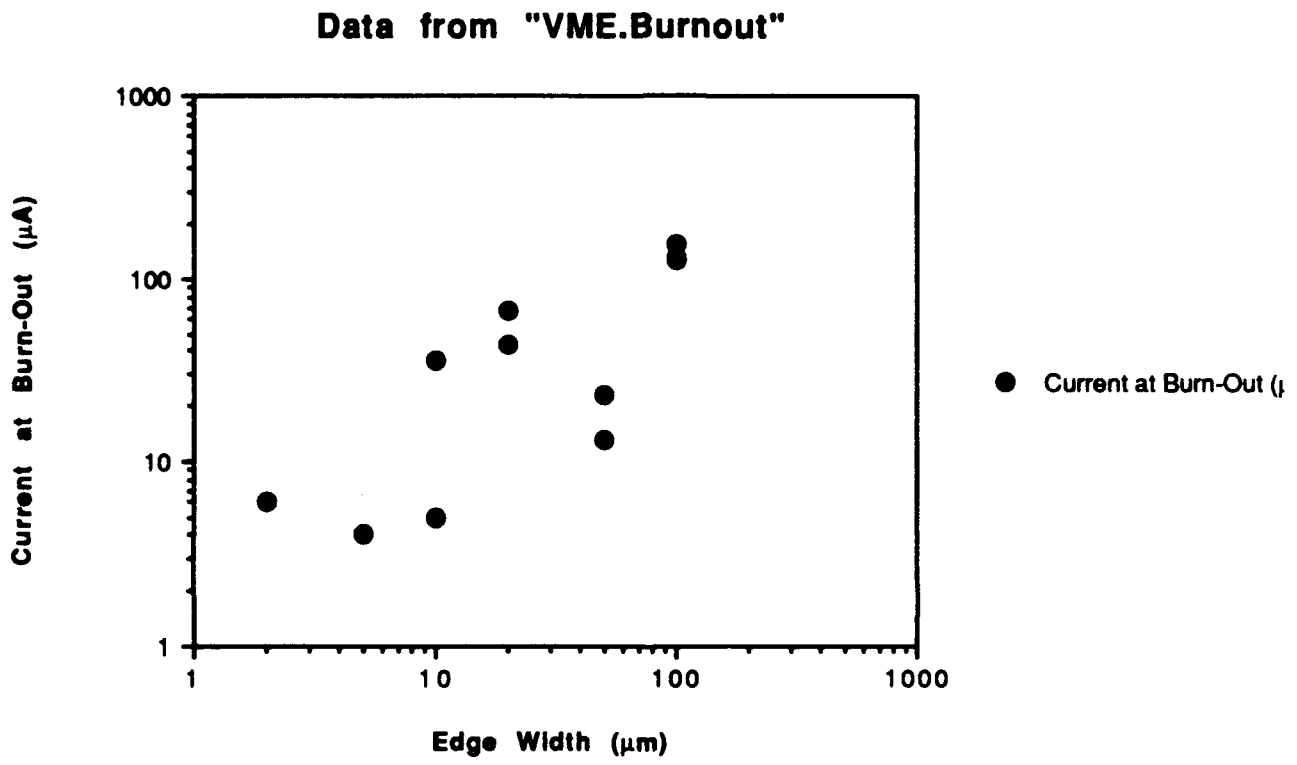


Figure 1.3-5 Current at burn-out vs the edge width. The data is from two dies on the same wafer.

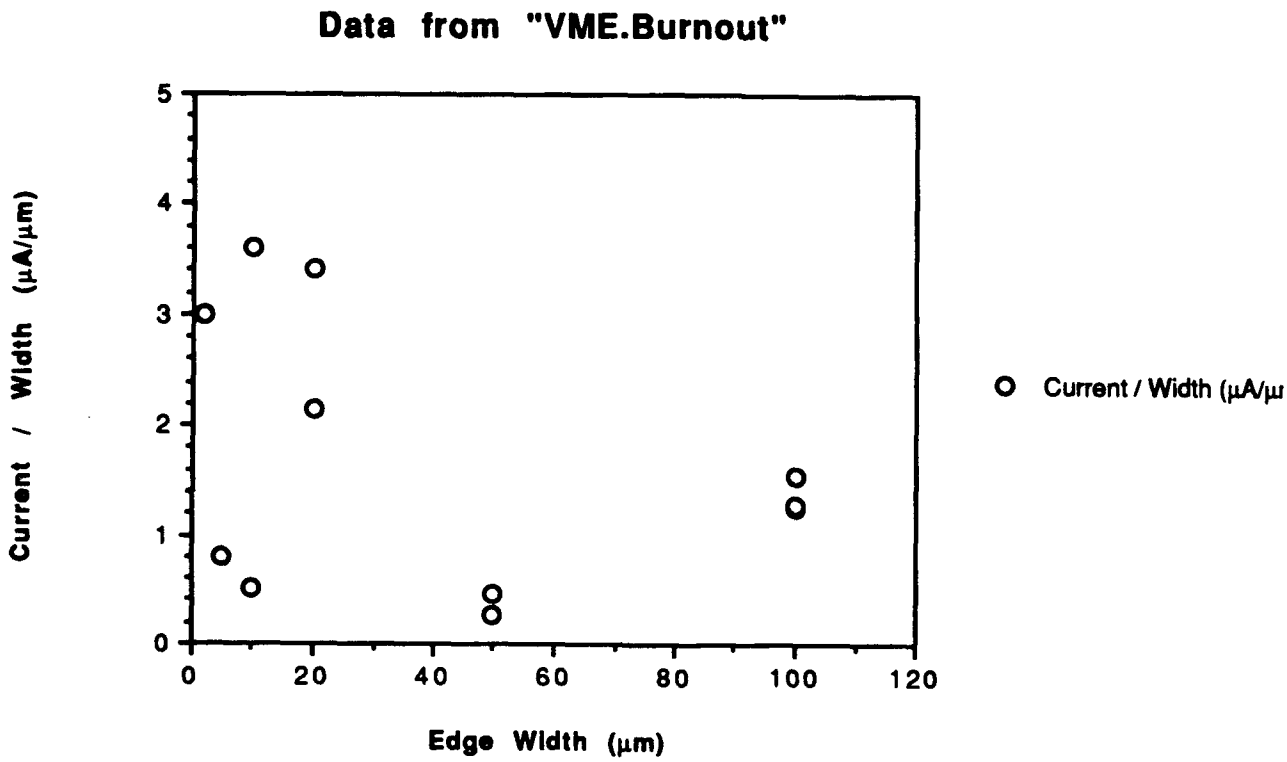


Figure 1.3-6 Current/width vs the emitter width. of devices shown in previous figure.

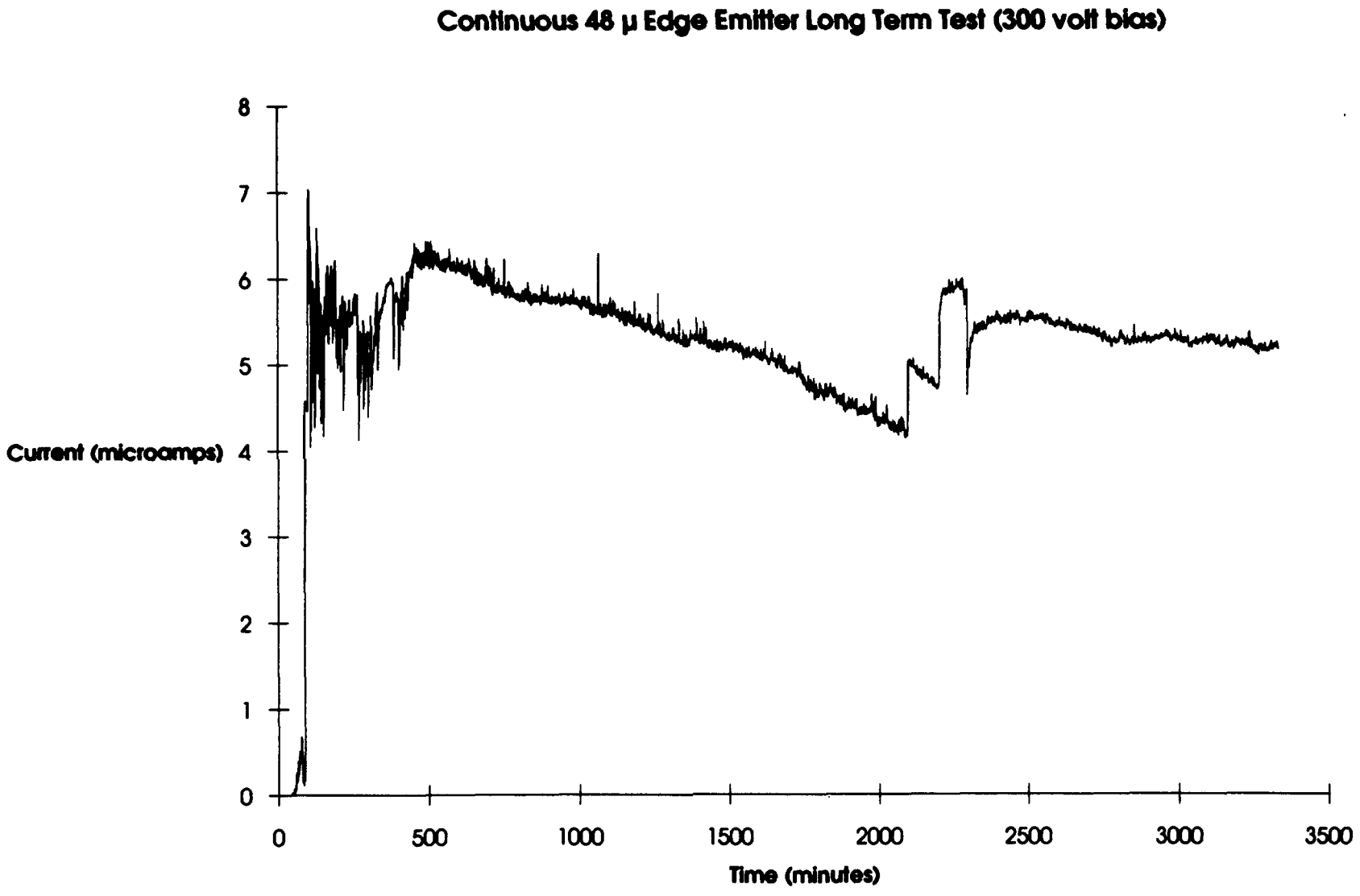


Figure 1.3-7 Long term test of a 48 µm wide edge.

Parameter	Wafer # 5316-Q1-01	5316-Q1-04	5316-Q1-07
Emitter Material	TiW	TiW	TiW
Emitter Thickness	200 Å	300 Å	400 Å
Sac Layer Thk 1	2000 Å	2000 Å	2000 Å
Resistor Material	2,5000 Å TaN	2,5000 Å TaN	2,5000 Å TaN
Resistor Rsh	1MΩ/square	1MΩ/square	1MΩ/square
Sac Layer Thk 2	2000 Å	2000 Å	2000 Å
Anode Material	1 μm TiW	1 μm TiW	1 μm TiW

We are using the computer automated test system shown in Figure 1.3-2 and acquiring data on a 24-hour basis. Below is a summary of the test results.

Devices tested to date include devices with and without combs and devices with and without resistors. The devices have varying gaps between the emitter and the anode.

1.3.1 Emission Current of Devices with Long Straight Edges

We have tested numerous devices with long straight edges varying from 2 μm wide edges to 100 μm wide edges. The highest current measured is about 155 μA on a 100 μm wide device. Figure 1.3-3 shows a typical IV diode characteristic for a 100 μm wide device in both the forward and reverse direction. The particular plot shows a current maximum of 100 μA set by the current compliance. These devices have also been allowed to run at 50 μA for over 24 hours without burn out. Attempts to run the device at 100 μA for long periods of time did not succeed because the device burnt out after only 1 hour of operation. Figure 1.3-4 shows a typical long term test of the device of a device biased at 50 μA for over 1000 minutes. We do not know the reasons for burn-out at the present moment, but we are conducting auxiliary tests such as electromigration in vacuum.

1.3.2 Emission Uniformity

We have taken emission current data on devices that are 2 μm - 100 μm wide. The data was taken by sourcing current and measuring voltage. We determined from the measurement the current at which the device burns out instantaneously by stepping the current source and measuring voltage. Figure 1.3-5 is a plot of the current at burn-out vs the emitter width for two die on a wafer with an emitter of 200 Å TiW and a 1 μm thick anode. The same data is re-plotted as Emission Current / Unit Width vs Emitter width in Figure 1.3-6. It is interesting to note that the highest current / unit width is about 3 μA/μm and that while we can not claim to have uniform emission we can conclude that emission is not from a single point. The data still leaves the question whether the burn-out is due to material properties or is due to edge roughness. We shall be able to ascertain this when we test edges made from other materials.

1.3.3 Long Term Emission Tests

A device with a 48 μm long edge was left under bias for >3900 minutes (≈70 hours). The device was tested by ramping up from 0 V to 300 Volts in steps of 10 V. Data was taken every 5 seconds and the duration the device was at any particular bias was 3 minutes. At the end of the ramp, the device remained at 300 V. Figure 1.3-7 is a plot of current vs time. At 3900 minutes the device was still operational. From the current and value of the resistors at the probe tip, we can deduce that the actual voltage bias of the device when the IR drop is taken into account is about 180 V. Thus the device had a current of 6 μA at 180 V, which is quite good.

1.3.4 Emission from Comb Edges without Series Resistors

The initial tests were done with 10 MΩ resistors at each probe tip. While the devices did not have any on-chip resistors they had external resistors that stabilized current and prevented burnout. These tests ramped up the voltage from 0 V to 300 in steps of 10 V. The device was usually left at 300 V for as long as desired. Typically the devices turned on at 250 Volts and the maximum current at 300 V was typically 2 - 10 μA. We found that the current was limited by the off-chip resistors on the probe tips. When the bias voltage was increased beyond 300 V, the current increased rapidly. Many devices were left on long term tests overnight or over a weekend. The devices did not burn-out even though the current fluctuated

1.3.5 Emission from Comb Edges with Series Resistor

The devices are field emission diodes with 5 μm wide fingers and 10 MΩ TaNx series resistors The devices have four, six and eight fingers. The emitter / anode separation is estimated to be 4,000 Å. The gap was formed by two sacrificial oxide layers deposited by PECVD. We determined the device turn-on voltage and the device burn-out current. The electrical tests were performed by sourcing current and measuring voltage with a voltage compliance set at 500 V.

The devices turned on at a higher voltage than comparable devices without series resistor, as expected. The devices also have lower transconductance as expected. The devices with eight fingers burned out at a higher current than the devices with six fingers - which in turned burnt out at a higher current than the devices with four fingers. At present we do not completely understand the data but the trend is encouraging. We are conducting more tests to determine the source of the burn-out and the implications of the results.

Task 2 Process Development

The focus of this task is to conduct a careful study of materials and processes used to fabricate vacuum microelectronic devices and investigate the best possible combination of approaches to obtain the desired device characteristics including high transconductance, low capacitance, low-leakage currents and high reliability.

Sub-task 2.1 Emitter Materials Study

2.1.1 Atomic Force Microscopy of Thin Film Edges

We conducted measurements to determine the surface roughness and the edge roughness of thin films. The main objective of the experiment was to determine the intrinsic short range roughness of thin films used in the emitter of field emission and also determine the roughness introduced on the edges by the thin film definition process.

Approach: Three wafers with 1.4 μm of silicon dioxide, 1000 Å of silicon nitride and 200 Å of TiW were fabricated. One wafer was patterned with edges using the ion mill for the TiW and C_2F_6/CHF_3 for the nitride layer, the second wafer was patterned using SF6 for TiW and nitride layers, and the third wafer was not patterned. 1 cm x 1 cm pieces were loaded and scanned under an Atomic Force Microscope after calibration.

Unpatterned Surface

A 20 μm x 20 μm scan was done at a scan rate of 2 Hz. Area statistics shows that the average height of the surface is 9.7 Å with a RMS roughness of 27.1 Å and an average roughness of 21.5 Å. This is the composite roughness for the silicon substrate, the 1.4 μm oxide, 1000 Å of silicon nitride and 200 Å of TiW. The probe tip used however has a radius of curvature that is quite large. We should use sharper tips in future measurements.

Edges Patterned in SF6 Plasma

Figure 2.1-1 is a projected profile of an edge scanned at .5 Hz. The observed sidewall may be steeper than shown because the tip is not sharp. The observed slope may result from the side wall bumping into the side wall of the edge. A step of about 400 Å is observed but the TiW thickness is only 200 Å. It may be a profile from the probe tip. The observed step height of 1300 - 1400 Å is correct however. We also see the the top edge has some short range roughness probably due to the resist patterning. The implications of this for the uniformity of edge emission is not quite clear at this point.

Edges Patterned in Ion Mill System and C2F6/CHF3 Plasma

Figure 2.1-2 is a projected view of .5 Hz scan of an edge defined by ion milling and C_2F_6/ CHF_3 plasma. The etch did not stopped at the silicon nitride/silicon dioxide interface. The small fingers are 2000 Å high and about 0.6 μm wide. Figure 2.1-3 is the tip of one of the fingers. As in the previous sample we could not tell if the side walls are real of they are an artifact of the scanning tip. There is also a short range roughness of the metal edge as in the previous sample.

2.1.2 Etch Studies of Emitter Materials.

The objective of this study is two-fold. The first is to investigate methods of chemically polishing the edge after its definition by lithography and etch. The second objective is to determine which materials would etch selectively with respect to other metals that will allow the formation of tapered edge emitters as shown in Figure 2.1-4. The laminated emitter structure has a very thin edge (100 - 150 Å) and has low resistance due to increased thickness away from the edge.

We deposited 5000 Å of TiW, WNx, and WSix on silicon substrates with 1.4 μm of oxide and 1000 Å of silicon nitride. The metals were etched for short times in 10:1 H_2O H_2O_2 mixtures at 60 °C, 50 °C, 40 °C and 30 °C.We determined the etch rate from thickness and sheet resistance measurements. The results indicate that TiW and WNx etch at a faster rate than WSix. This indicates that it would be possible to make the tapered edge shown in Figure 2.1-4 if WSix is the center and thinner conductor and TiW or WNx is the outer and thicker conductor. We are also evaluating the data to determine the optimum temperature for the formation of the tapered edge.

2.1.3 Dielectric Studies

In the first quarter of 1992, a study of the dielectric films used in the VME structures was started to determine the quality of the films. As there will be high electric fields present in the structures, the dielectric films must be of high quality for electrical isolation between the emitter, anode and control electrodes. This means that the films must exhibit low leakage currents and high breakdown fields. The dielectric films used in the VME structures include both silicon nitride and silicon dioxide films deposited by sputter deposition and also by plasma enhanced chemical vapor deposition (PECVD).

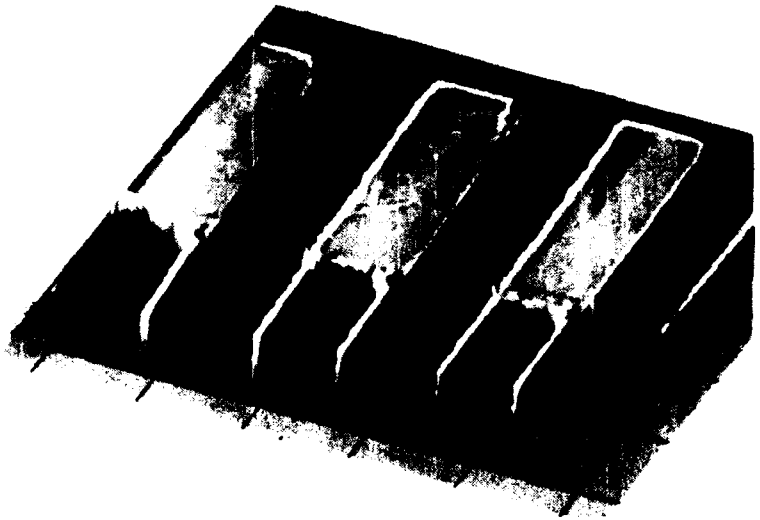


Figure 2.1-2 AFM profile of an edge scanned at 0.5 Hz. The device was patterned in an ion-mill system and in C_2F_6/CHF_3 plasma.

Figure 2.1-3 Closer view of edge emitter AFM scanned at 0.5 Hz. The device was patterned in an ion-mill system and in C_2F_6/CHF_3 plasma.

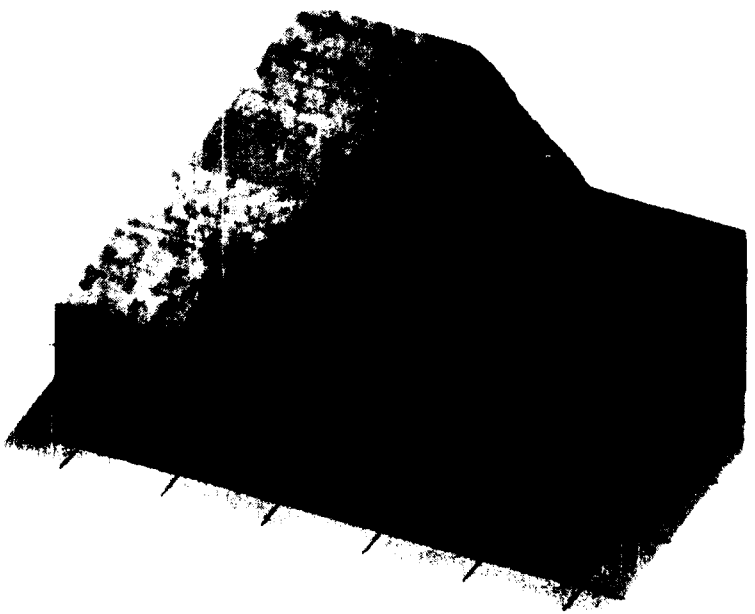


Figure 2.1-1 AFM profile of an edge scanned at 0.5 Hz. The device was patterned in SF6 plasma.

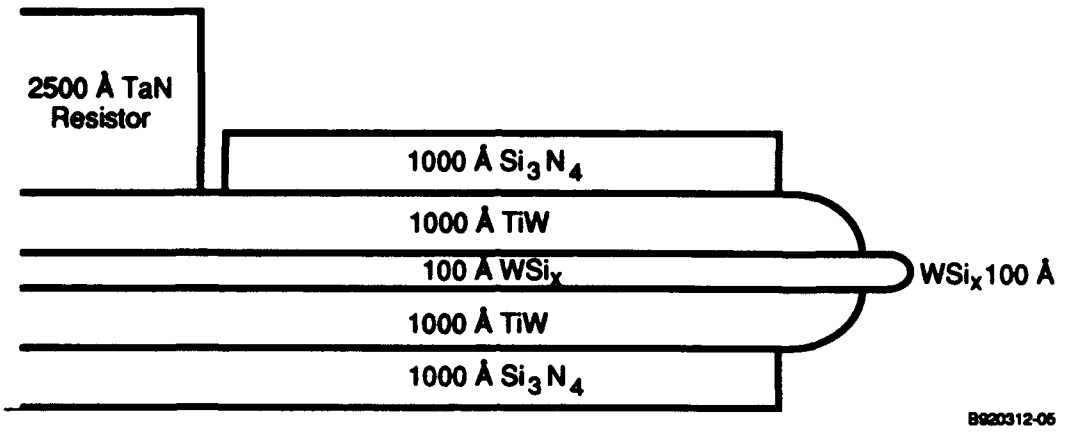


Figure 2.1-4 Laminated emitter structure for burn-out prevention and high emission current.

The following dielectric films were included in the study: sputtered silicon nitride, plasma-enhanced chemically vapor deposited (PECVD) silicon nitride, sputtered silicon dioxide and PECVD silicon dioxide. Capacitor structures were fabricated using each of the dielectric films to test the leakage current and breakdown field strength. The dielectric films used for this study varied in thickness from 500Å to 5000Å thick films. Current versus voltage measurements were made on the capacitor structures to measure the dielectric breakdown strength and current leakage of the films. The leakage currents in the films were measured for applied fields up to 1.0e7 V/cm. The films were measured in the as-deposited state and after subsequent anneals in forming gas (N_2 and O_2) at temperatures of 250 °C, 300°C, 350°C and 500 °C.

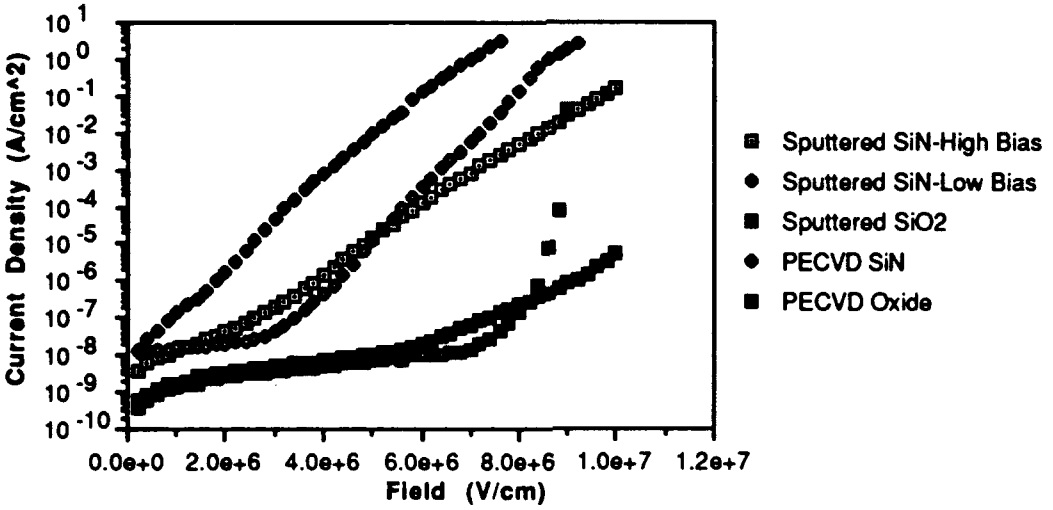


Figure 2.1.4. Composite Plot Of Current Density Versus Field For As-Deposited Dielectric Films

Figure 2.1.4 shows the measured current density versus electric field curves for each of the films in the as-deposited state with no annealing. The silicon nitride films show relatively high leakage currents that increased with the applied field even though actual breakdown of the films does not occur until fields above 8.0 x 10^6 V/cm or higher. The high-bias sputtered silicon nitride and the PECVD oxide did not breakdown even at a field of 1.0 x 10^7 V/cm. Breakdown fields of $\geq 10^7$ V/cm are considered to be very good for silicon dioxide and silicon nitride.

The oxide films showed very low levels of leakage current, below 10^{-7} A/cm^2 (10^{-3} pA/μm^2), for fields up to 8.0 x 10^6 V/cm for the sputtered oxide and up to 6.0 x 10^6 V/cm for the PECVD oxide. These results indicate that the oxide films may provide better dielectric isolation between the active layers in the diode and triode structures.

The dielectric films were annealed at temperatures up to 500 °C to see if there would be any improvement in the properties of the films. There was little change in the current-voltage characteristics of any of the silicon nitride films with annealing .

In the second quarter of 1992, experiments were focused on the sputtered and PECVD oxide films because of the lower levels of leakage current measured in these films. The experiments involved heat treatments or annealing of the films at temperatures up to 500 °C to try to

decrease the leakage current and increase the breakdown field of the oxide films. The annealing of the films could accomplish this by densifying the films and by allowing any trapped gases in the films to escape.

Capacitor test structures were fabricated using the oxide films and incorporating annealing cycles after the deposition of each layer - bottom electrode, oxide film and top electrode. Capacitor test structures which were not annealed were also fabricated at the same time for comparison to the annealed structures. The capacitor structures were evaluated using current-voltage measurements for leakage current and breakdown field. The results of the testing of these structures did not show any significant improvement in the properties of the oxide films with annealing.

At this time, then, it is concluded that incorporating an anneal of the dielectric films in the diode and triode structures would not be of benefit to the dielectric isolation between the electrodes. The oxide films should still provide good isolation between the emitter, anode and control electrodes as the current levels are less than 10^{-7} A/cm^2 (10^{-3} pA/μm^2) up to fields of 6.0 x 10^6 V/cm (240 volts for 4000Å thick film).

2.1.4 High Resistance Thin Films for Current Equalization Elements

Two material systems were developed for the sputter deposition of high resistance materials for VME current equalization applications. TaNx and Si resistor films can be sputtered to meet device specifications. Results on TaNx were reported in last quarter's report.

Sheet resistance values in the meg ohm/square range can be achieved for these materials for films in the ~1000-3000 Å thickness range. The process can be tailored to yield desired properties, and the imposition of a substrate bias can be included to enhance step coverage, while maintaining specified film characteristics.

The TaNx system utilizes reactive sputtering in a nitrogen environment to produce films that vary in sheet resistance from <10 ohms/square to >>1 meg ohm/square, as the nitrogen concentration (%N_2 in Ar) is varied from 10-80% (see figure 2.1.5).

The high resistance Si films are sputtered from a boron doped Si target (~70 ohm cm resistivity). ~1-2 meg ohm/square can be achieved in doped Si films ~1000-3000Å in thickness (see figure 2.1.6).

A thin (~200-300 Å) Si_3N_4 protect layer is sputtered (*in situ*) to cap the sputtered resistor film. The incorporation of the protect cap is necessary to minimize subsequent oxidation effects and/or anomalous sputter etching effects that can result in a low resistance surface layer formed during the backsputter cleaning sequences which are implemented just prior to the sputter deposition of additional layers.

Diode device runs have been made to evaluate high resistance TaNx and doped Si thin film resistors. The film thickness was controlled to ~2500 A to enhance step coverage. A substrate bias was also imposed during the sputter deposition to further improve the step coverage. Initial testing indicates that these resistor structures are behaving as specified.

Task 3 Triode Development

The focus of this task is to develop a three-terminal vacuum microelectronics structure suitable for integration into an RF amplification structure.

Figure 2.1-5 NITROGEN CONCENTRATION (%N2 IN Ar)

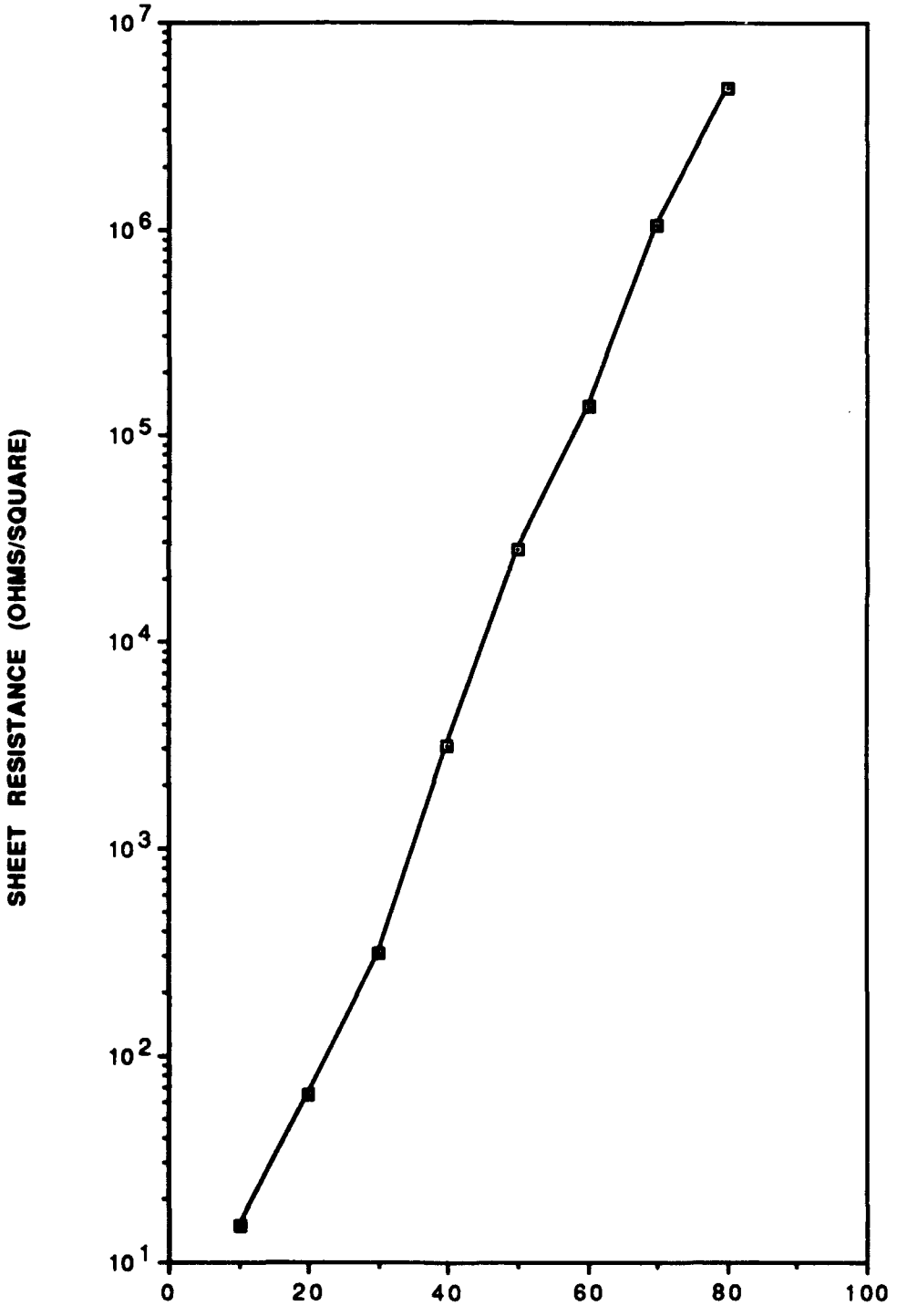
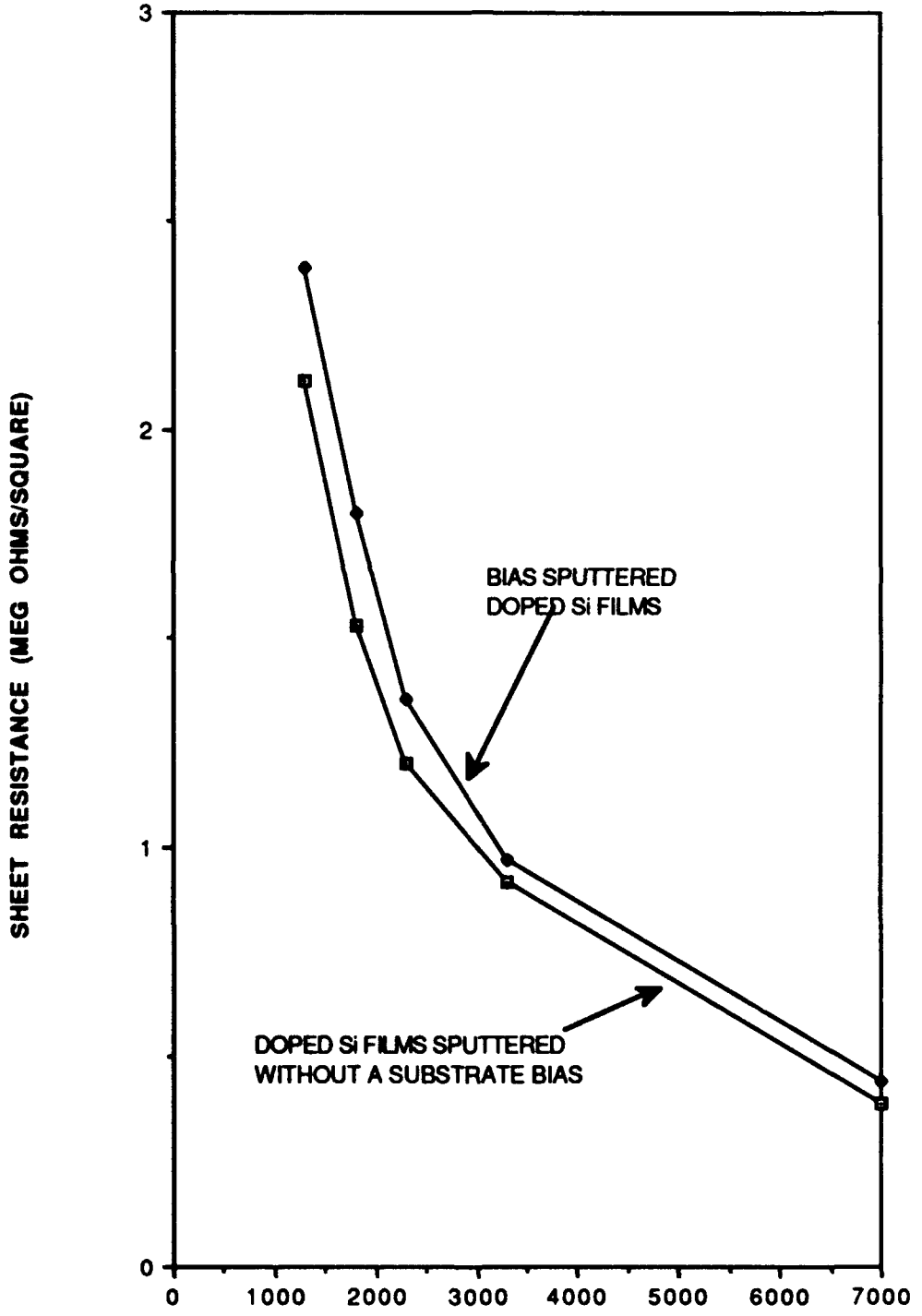


Figure 2.1-5 NITROGEN CONCENTRATION (%N2 IN Ar)

Figure 2.1-6 Si FILM THICKNESS (ANGSTROMS)

SHEET RESISTANCE OF BIAS AND ZERO BIAS SPUTTERED DOPED SILICON FILMS AS A FUNCTION OF THICKNESS



Subtask 3.1 Triode Development

3.1.1 Design Considerations Triode Design

The primary factor limiting the gain of the field emission triode is related to the magnitude of the current which can be extracted from the device emitter as indicated by the transconductance g_m:[1]

$$g_m = \partial I/\partial V = I/V = I/V*(2+b/V)$$

where I is the emission current, V the control electrode-emitter bias and b is a constant. From this expression it is clear that being able to obtain high emission with low operating voltages is a very high priority for maximizing gain. At microwave frequencies the parasitic capacitances are also significant as shown by the unity current gain cutoff frequency f_τ:

$$f_\tau = g_m/(2\pi C_{in})$$

This expression is readily derived from the simplified device equivalent circuit in Figure 4.2-1.

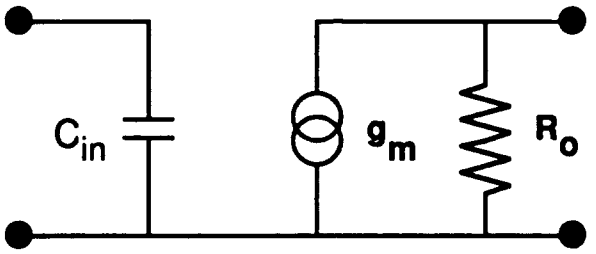


Figure 4.2-1 Field emission triode equivalent circuit defining the parameters used in the current gain cutoff frequency calculation

This figure of merit is quite useful for comparing active devices but it ignores the effect of parasitic resistances and control electrode-to-anode feedback capacitance C_{ac}. The power gain cutoff frequency, f_{max}, includes these effects

$$f_{max} \approx f_\tau/(2\sqrt{r_1 + 2\pi R_g C_{ac}})$$

where R_g is the control electrode access resistance indicated in the equivalent circuit in Figure 4.2-2.[2] While such cutoff frequencies are informative, within the operating bandwidth the power gain G_p is more important to the system designer since it affects both the efficiency and performance of the finished amplifier. This is related to the (matched) impedances presented at the device terminals.

---

[1] "Microwave Field-Effect Transistors--1976", C. A. Liechti, IEEE Transactions on Microwave Theory and Techniques, Vol. MTT-24, No. 6, June 1976, pp.279-300

[2] "Physical properties of thin-film field emission cathodes with molybdenum cones", C.A. Spindt, I. Brodie, L. Humphrey, and E.R. Westerberg, Journal of Applied Physics, Vol. 47, No. 12, December 1978, pp. 5248-5268.

$$G_p = g_m^2 R_o R_{in}$$

where R_o and R_{in} are the load and source impedances, respectively. At microwave frequencies these numbers are constrained to a few multiples of 50 ohms by bandwidth requirements and device parasitic capacitances. All of these factors make high transconductances extremely important in the microwave frequency range. An example of the effects of low transconductance can be seen in the limited microwave capability of conventional thermionic emission vacuum tube triodes. In contrast, the high average current densities and transconductances of solid state devices has been used to extend their operation to frequencies greater than 100 GHz. For microwave frequency operation, similar capabilities must be demonstrated by field emission triodes which makes high average current density a crucial consideration in their development.

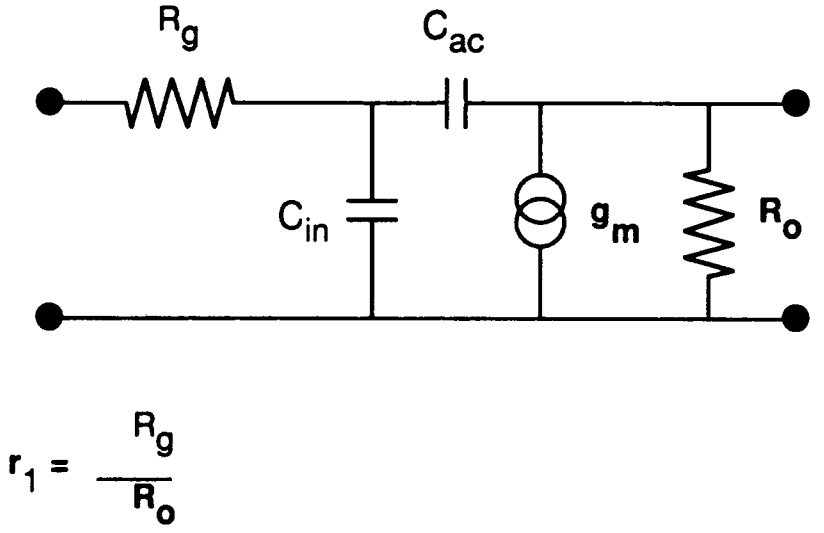


Figure 4.2-2 Simplified field emission triode equivalent circuit with the parameters used in the expression for the power gain cutoff frequency

With submicron geometries planar edge emitter triodes can have significantly lower parasitic capacitances than other field emission devices. However, at this early stage of development, such geometries require more complex processes and almost all of our efforts are directed towards the higher priority task of increasing the current density capabilities of the device. There are a number of phenomena which may be limiting currents. Some of them are listed in Table 4.2.1-1.

Table 4.2.1-1
Phenomena Potentially Limiting Field Emission Currents

Mechanism	Reasons for Believing	Reasons for Rejecting
Joule heating of emitter film	Emitter is very thin and thermally well isolated	Calculations indicate very small temperature rises should occur for measured film parameters
Film is so thin that it may not be continuous resulting in excessive heating and electrostatic force enhanced failures	While the film thickness measurements agree with the expected values the atomic force microscope indicates that there is some variability	The film resistance is quite close to bulk parameter values but is this sufficient?
Heating of the anode during operation ejects ions which strike the emitter at high velocity causing overheating	Diode failures give evidence of emitter melting, in some cases away from the edge.	Vacuum around device may be deficient for reasons unrelated to anode heating
Test system vacuum is too poor to avoid plasma breakdown	Breakdowns with poor vacuum have been observed to give damage similar to that observed	Present vacuum, measured with an ion guage in the chamber indicates a vacuum better than 10^{-8} torr
Electromigration limits film current density	Possible film thickness nonuniformity along with vacuum heating may lead to failure	The same film in vacuum can handle currents as high as several milliamps in the same area

Using measured film resistances, the calculated temperature rise due to joule heating in the emitter film appears to be less than a few tens of degrees, at most, for projected current densities. However, the film properties may be somewhat different towards the emitting edge for actual devices and electrostatic forces may play some role in increasing this resistance if the film is nonuniform. From the observations which have been made this does not appear to be the case for diodes. It should be a much smaller issue for triodes where stress in the emitter films is much lower.

Since the films appear uniform under a scanning electron microscope they were also measured with the atomic force microscope. The indicated standard deviation of the film height was about one-fourth the film thickness of test samples which still leaves some questions but the failed diodes which have been observed give little evidence that they failed mechanically.

Frozen droplets of previously molten metal are seen on both the emitter, and in some cases, on the anode of diodes which failed in poorer vacuums. This is consistent with gas plasmas. The latest devices carry much higher currents before failure but they have been vacuum baked at elevated temperatures prior to testing. This was not possible in with our older systems. Postmortem inspection of some of the diodes which operated at currents above 100 μA will be carried out in the near future to better understand their characteristics. This inspection, along with testing of diagnostic devices on the same wafers, is expected to provide the basis for achieving higher currents.

As materials are improved, processes are optimized and better vacuum conditioning techniques developed, higher performance triodes will be realized.

3.1.2 Triode Mask Set Features

The triode mask set is designed to investigate the benefits of various anode and emitter structures. Figure 3.1-1 has a composite view of the overall reticle. Experimental and theoretical investigations indicate that ion emission from the high temperature anode during operation is one of the more significant factors in the failure of diode emitters. This mask set contains devices to investigate techniques for reducing these failures in triodes while minimizing reliability degradation related to external circuit effects. Test structures to measure dielectric breakdown, surface leakage, metal film resistance, step coverage, alignment accuracy, pattern definition and via yields are also included to verify the performance of the materials and diagnose the cause of device failures.

The typical device layout in Figure 3.1-2 has multiple parallel emitter fingers sandwiched between an upper and a lower control electrode. The emitter is connected to the lower pad, the control electrodes to the right pad and the anode to the top pad. A layer of dielectric between the upper control electrode and the emitter supports the former in this design but for some of the devices a dielectric bridge is used for support as inferred in the 3-dimensional drawing in Figure 3.1-3. The variety of triode structures is indicated in the following tables of emitter and anode designs.

The basic emitter designs are listed in Table 4.3-1.

Table 4.3-1
Basic Emitter Design Configurations Used in Triode Mask Set

Emitter Configuration	Purpose
Multiple Emitter Fingers with Series Resistors	To enforce current uniformity across the width of the emitter for greater current capability and increased reliability
Multiple Emitter Fingers without Series Resistors	To compare with previous design and establish limits for resistor requirements
Monolithic Emitter with Series Resistor	To demonstrate the maximum current in a small area while minimizing capacitive parasitics with some local current runaway protection

These emitters are used with the anode configurations described in Table 4.3.2 and Figure 3.1-4. Such designs are intended to increase the area of electron impact for reduced heating and ion emission which appears to be implicated in some emitter failures at high current densities.

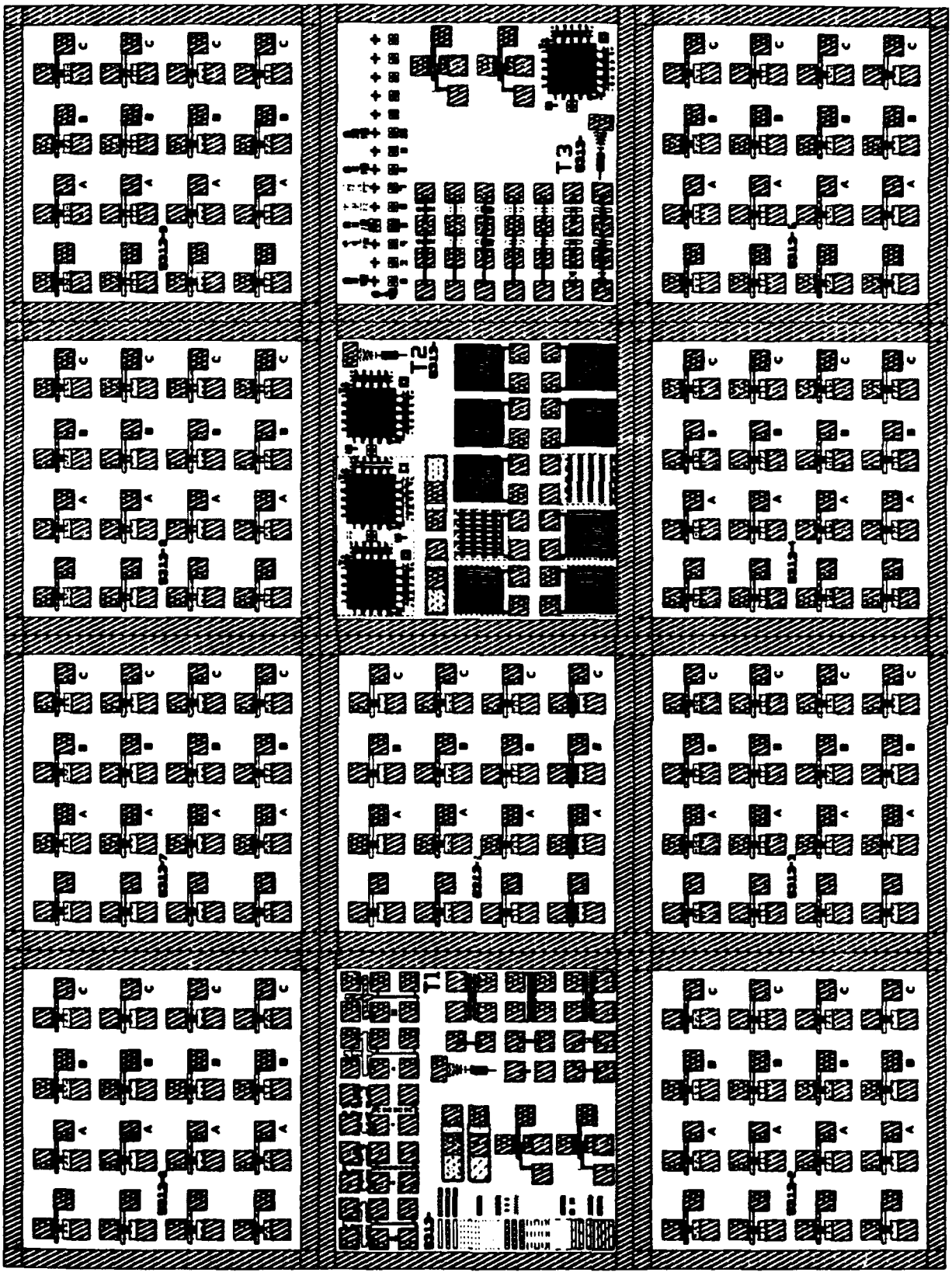


Figure 3.1-1 Composite view of the overall 5313 reticle showing the 3 test and 9 triode device dies to be fabricated and tested.

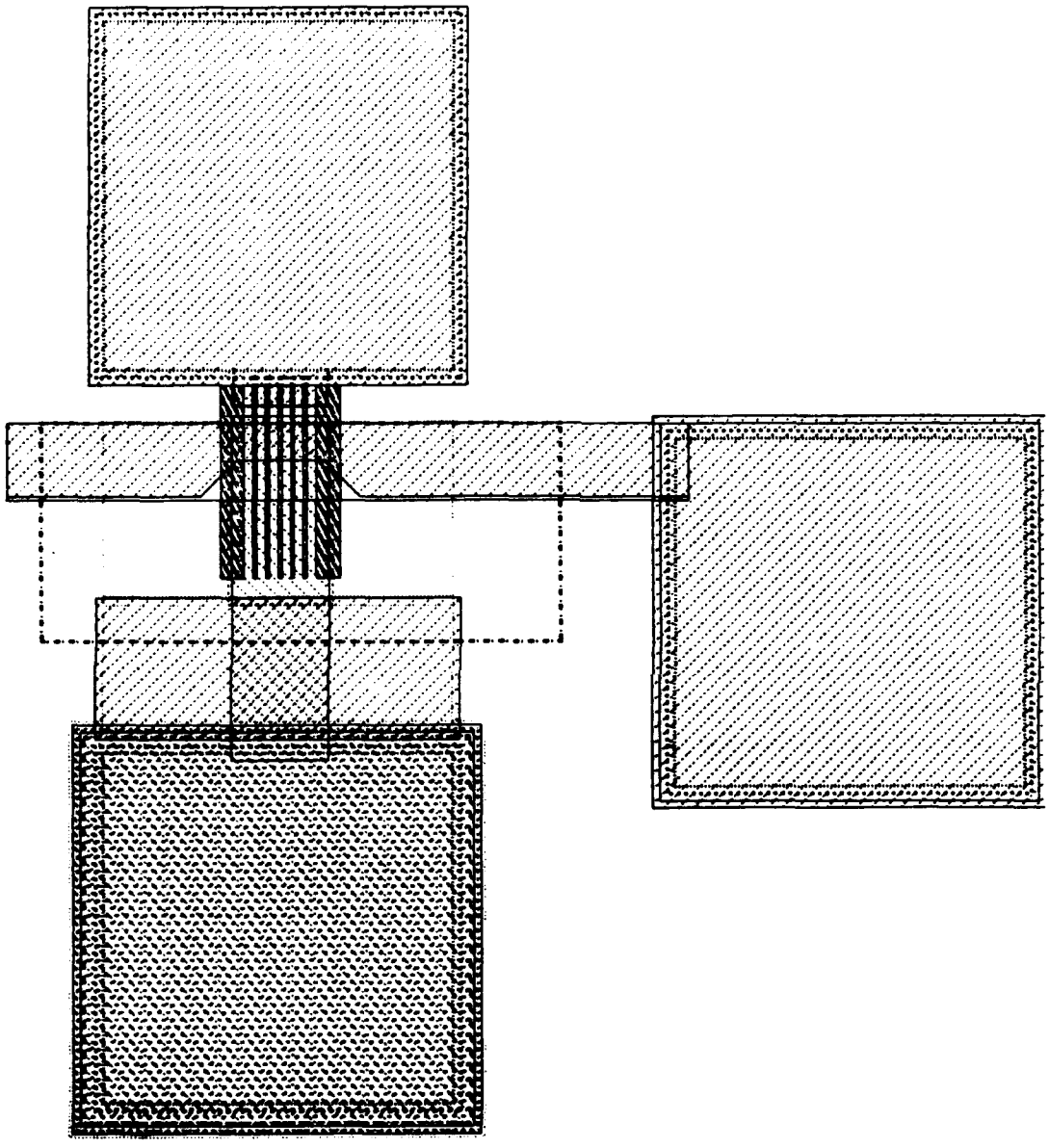


Figure 3.1-2 Typical device structure with multiple emitter fingers and parallel between upper and lower control electrodes. The anode is at the top, the emitter at the bottom and the control electrode pad on the right of the figure.

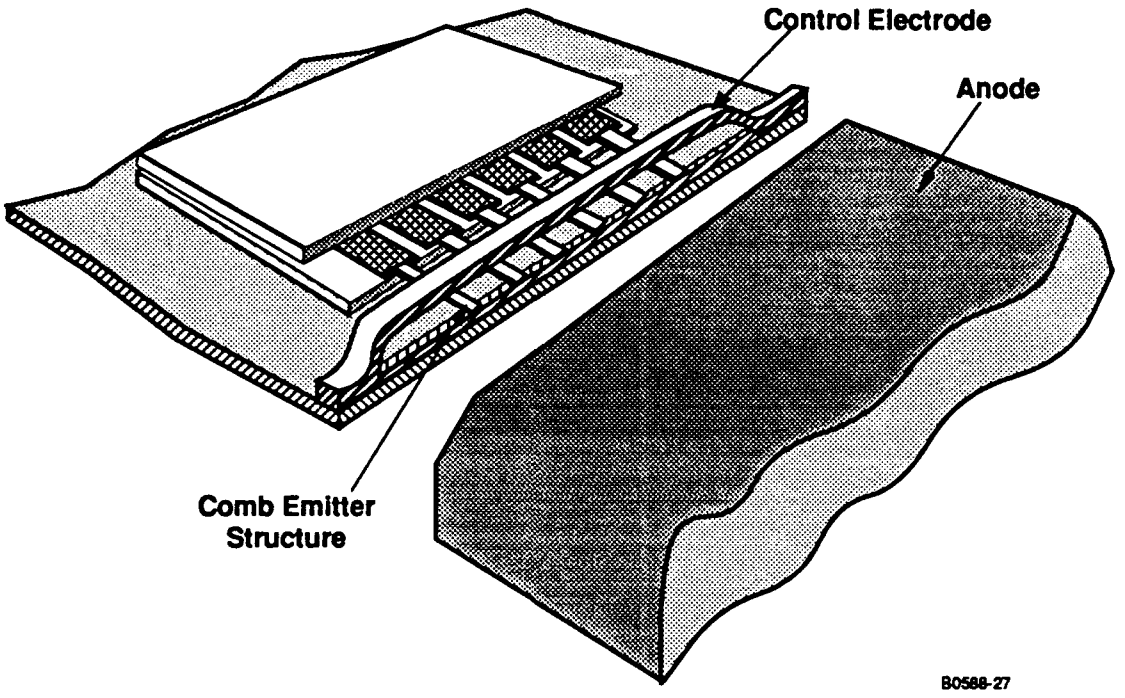
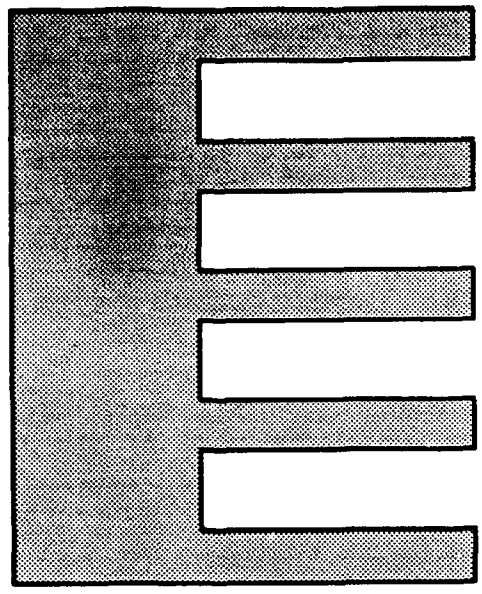
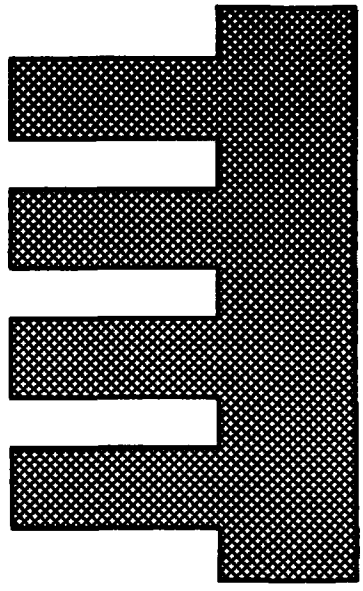


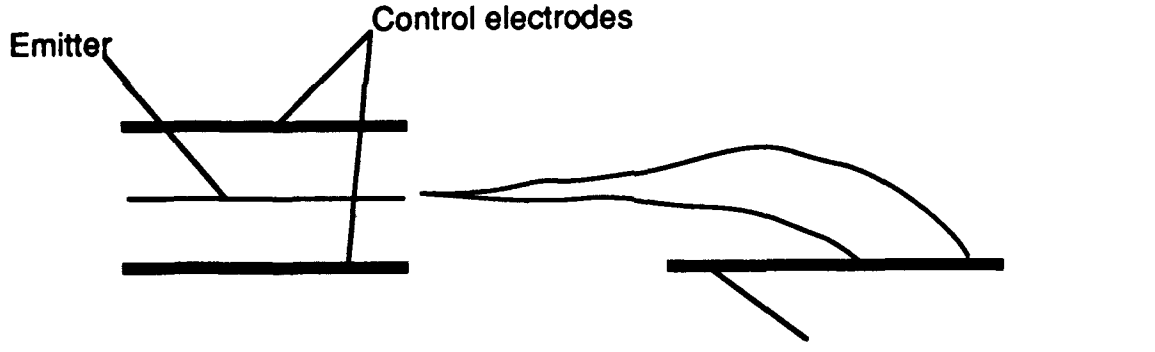
Figure 3.1-3 Three dimensional drawing of the emitter and control structure of a field emission triode conceptually similar to the devices being fabricated on the 5313 mask set



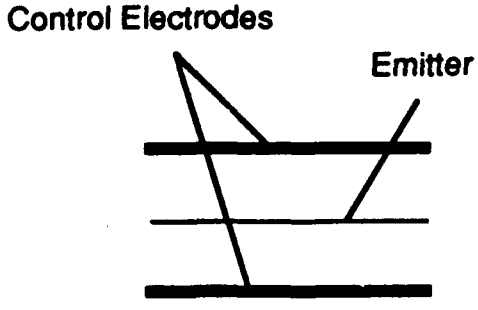
Emitter with multiple fingers



"Zigzag" anode for distributed electron collection to reduce localized heating



Reduced height anode for distributed electron collection



Multilayer thick anode for maximum heat dissipation

Figure 3.1-4 Various anode structures used in the triode mask set.

Table 4.3.2
Description of Field Emission Triode Anode Configurations

Anode Configuration	Purpose
Thick refractory metal layer	Improved heat conduction anode for greater operating current
Reduce height anode	Electron impact should be spread over a larger area since many electrons may miss the edge of the anode closest to the emitter
"Zigzag" anode	Anode fingers are aligned with gaps between emitter fingers to increase the area of electron impact

To investigate the effects of control electrode geometries their lengths have been varied from 3 to 20 microns in different structures. While much shorter lengths will eventually be needed, the processing costs are not presently justified. The geometries fabricated can be used to determine the effects of control electrode lengths for future designs.

The layouts are based on self-aligned patterning of the emitter and resistor layers to minimize the achievable spacing between the emitter fingers. By defining the length of the fingers separately from their width irregularities in their shape will be avoided.

Because of the reduced spacing between the control electrodes and the emitter as well as the balanced configuration we expect that field emission triodes from this mask set will deliver greater maximum current densities than the test diodes. At the same time the control electrode voltages required for this current will be smaller that the operating voltages for the diodes.

3.1.3 Triode Finite Element Modeling

Modeling Objective
Under emission, the triode is usually found to "burn out" after some time of operation. The objective of the modelling effort this quarter was to model the anode and emitter heating during operation and determine if temperature rises have significant potential to be responsible for device failure.

Model
The triode is modeled in two dimensions. The geometry is the same as that modeled in previous electrostatic analysis work (see 2nd Quarterly Report). The FEM code used is ANSYS and the only difference from previous modeling is that the variable of interest is not the peak electrical field, but the peak temperatures [of the emitter and anode].

The anode is heated up by a power equal to IV, but the source of heat in the emitter is less clear. There are two competing heating explanations: power dissipated by emitter resistance (ohmic heating = i^2R), and power dissipated by liberated ions streaming back to the emitter from the anode (a release of potential energy which is also equal to iV). This model investigates and compares heat generated in the emitter by both possibilities. The calculations are done the following way:

$i = 5\ \mu A/\mu m$ (equates to $50\mu A$ for a $10\ \mu m$ emitter)
$V = 300$ Volts
$R = \rho * L_{emitter}/(t_{emitter} * width) = (4.5e\text{-}5\ \Omega\text{-cm})(4\mu m)(10^4 \mu m/cm)/(.025\mu m * 10\mu m)$
$= 7.2\ \Omega$

The power is then calculated and divided by the volume over which it is applied. This is input as a heat generation rate:

Anode heat generation rate: $h_{anode} = iV = (5e\text{-}6\ A/\mu m)(300)/((L_{emitter})(t_{emitter}) = (2.5\ \mu m)(1\ \mu m))$
$= \mathbf{0.0006\ W/\mu m^3}$

Emitter heat generation rate, iV: $h_{emitter,\ iV} = (5e\text{-}6)(300)/((.2\mu m^*)(.025\mu m)) = \mathbf{0.300\ W/\mu m^3}$
*All the ions are assumed to hit the exposed part of the emitter which extends beyond the nitride sheath 0.2 μm.

Emitter heat generation rate, i^2R: $h_{emitter,\ i2R} = (5e\text{-}6)^2(7.2\Omega)/((4)(.025)) = \mathbf{1.8e\text{-}9\ W/\mu m^3}$

The boundary conditions are that the bottom of the substrate (20 μm away from the device) is fixed at a temperature of 25°C--though the substrate is actually more like 500 μm thick, it has been found that the solutions aren't sensitive to thickness for the range of values modeled. Ambient conditions are defined to be 25°C. This value must be subtracted from the load case solutions to find ΔT.

Since all of the structures are packaged in a vacuum, the exposed surfaces are considered adiabatic and have not been assigned any convection coefficient. In reality, the temperature solutions determined by finite elements for the emitter show temperature increases of significant proportions such that radiation heat transfer is likely to be a significant source of cooling at the emitter tip. However, this analysis was only meant to gauge the potential for thermal damage and was not intended to pinpoint specific temperatures accurately and therefore the effect of thermal radiation heat transfer has been ignored.

Material properties used for modeling are as follows:

$k_{Silicon}$ = 141.2 W/m-°C
k_{SiO2} = 1.38 W/m-°C
k_{SiN} = 2.0 W/m-°C
k_{TiW} = 20 to 95 W/m-°C

The thermal conductivity of TiW is unknown and therefore high and low values for TiW are used to bound the problem. Since the alloy TiW is 90% tungsten, it is possible that its thermal conductivity mimics pure tungsten (k = 95 W/m-°C at a temperature of 2000 K); likewise, titanium has a thermal conductivity of only 20 W/m-°C. These values were used as upper and lower estimates of the range of possible thermal conductivity values for the alloy TiW. Note that it is very possible that the alloy has a thermal conductivity lower still than the individual values for either tungsten or titanium--sometimes the effect of small impurities (Ti) in a pure material crystal lattice (W) have an effect on thermal conductivity which is out of proportion to the volume ratio. Therefore, the thermal effects of an emitter made from a low thermal conductivity material should be noted under the knowledge that these effects could be further exaggerated if the film conductivity is even poorer.

Results

Eight load cases have been evaluated and are described below.

Load Case	Thermal Conductivity used for TiW	Load Case Description
1	95 W/m-°C	i^2R heating spread over the entire emitter film
2	20	i^2R heating spread over the entire emitter film
3	95	i^2R heating applied only to the emitter tip (the first 0.2 μm which extends beyond the nitride sheath)
4	20	i^2R heating applied only to the emitter tip (the first 0.2 μm which extends beyond the nitride sheath)
5	95	iV heating applied only to the emitter tip (the first 0.2 μm which extends beyond the nitride sheath)
6	20	iV heating applied only to the emitter tip (the first 0.2 μm which extends beyond the nitride sheath)
7	95	iV heating applied only to the first 2 μm of emitter tip
8	20	iV heating applied only to the first 2 μm of emitter tip

Raw Data:

Load Case	$T_{emitter--max}$	$T_{emitter--avg}$	$T_{emitter--min}$	$T_{anode--peak}$	$T_{anode--avg}$
1	38.77°C	38.72°C	38.67°C	56.19°C	54.02°C
2	38.80	38.72	38.64	66.39	59.98
3	38.77	38.72	38.67	56.19	54.02
4	38.80	38.72	38.64	68.39	59.98
5	3392.00	1751.00	109.20	81.96	73.62
6	1320.00	738.40	156.78	69.72	67.62
7	1806.00	958.30	110.50	81.95	73.61
8	843.30	500.50	157.65	69.72	67.61

Conclusions

- Ohmic heating does not produce a significant temperature rise in the emitter. Even when concentrated in the emitter tip, it does not generate any significant temperature gradient. [Compare load cases 1 through 4]

- It has also been theorized that ionic heating is occurring in addition to ohmic film heating; results show the potential from this type of heat flux applied to the emitter tip results in a temperature rise of as much as 3367°C over ambient under worst case conditions. [Compare load cases 5 through 8]

- iV heating concentrated in the emitter tip (the 0.2 μm which extends unprotected beyond the nitride sheath) tends to result in the greatest temperature rise. The thermal conductivity of the emitter film plays a large role here. If k = 95 W/m-°C, some of the heat is allowed to conduct away and the temperature rise is to 1320°C. If however, k = 20 W/m-°C, then there is a relatively large resistance to thermal conduction and the heat builds up such that the temperature rises to 3392°C (melting point of W is 3660 K, that of TiW is unknown to the author). Therefore, it is obvious how powerful of an effect the TiW film thermal conductivity has upon temperature rise. Since tungsten has such a high melting temperature and low vapor point, it is an ideal metal for this application, however, if the ratio of W to Ti could be increased, or if pure tungsten could be sputtered as the emitter material, it is believed that this would improve the heat transfer aspects and therefore the resulting operating temperature of this device. [Compare load cases 5 and 6]

- Load cases 7 and 8 are similar to 5 and 6 except the region that the heat is concentrated in is increased. Rather than place all the heat in only the first 0.2 μm it is spread out over the first 2.0 μm of the emitter (from the tip on back). While temperature rises are significant, peak temperatures are 1806°C and 843°C for k_{TiW} = 20 and 95 respectively, they are significantly lower than the previous load case. Again, there is a large difference in peak temperatures depending upon the emitter film's thermal conductivity. The lower temperatures may be traced to the fact that much of the heat is placed in regions of the emitter which aren't as thermally isolated as the emitter tip and are more easily conducted away to the substrate.

Three figures are enclosed of model results. Figure 3.1-5 is a view of the emitter/control electrode structure showing the temperature profile of the emitter for load case 5 (the temperature scale is on the right in degrees Centigrade). Figure 3.1-6 is a close-up plot of the thermal gradient of the emitter for the same load case. Finally, figure 3.1-7 is a overall view of the emitter/anode structure in which several thermal contour plots have been overlaid in order to better see the isotherm contours (the temperature scale on the right does not apply in general except to the emitter tip itself).

IV. Plans for Next Quarter

- Redesign the field emitter diode mask set to obtain a diode array. This new mask set will be geared towards achieving the $SAcm^{-2}$ and 5 mA total current objective.

- Evaluate cermet as an emitter material. Indications are that cermet (such as TaN/Si_3N_4 or $CrSi_2/SiO_2$) have low-work functions which may be practical for field emitter devices.

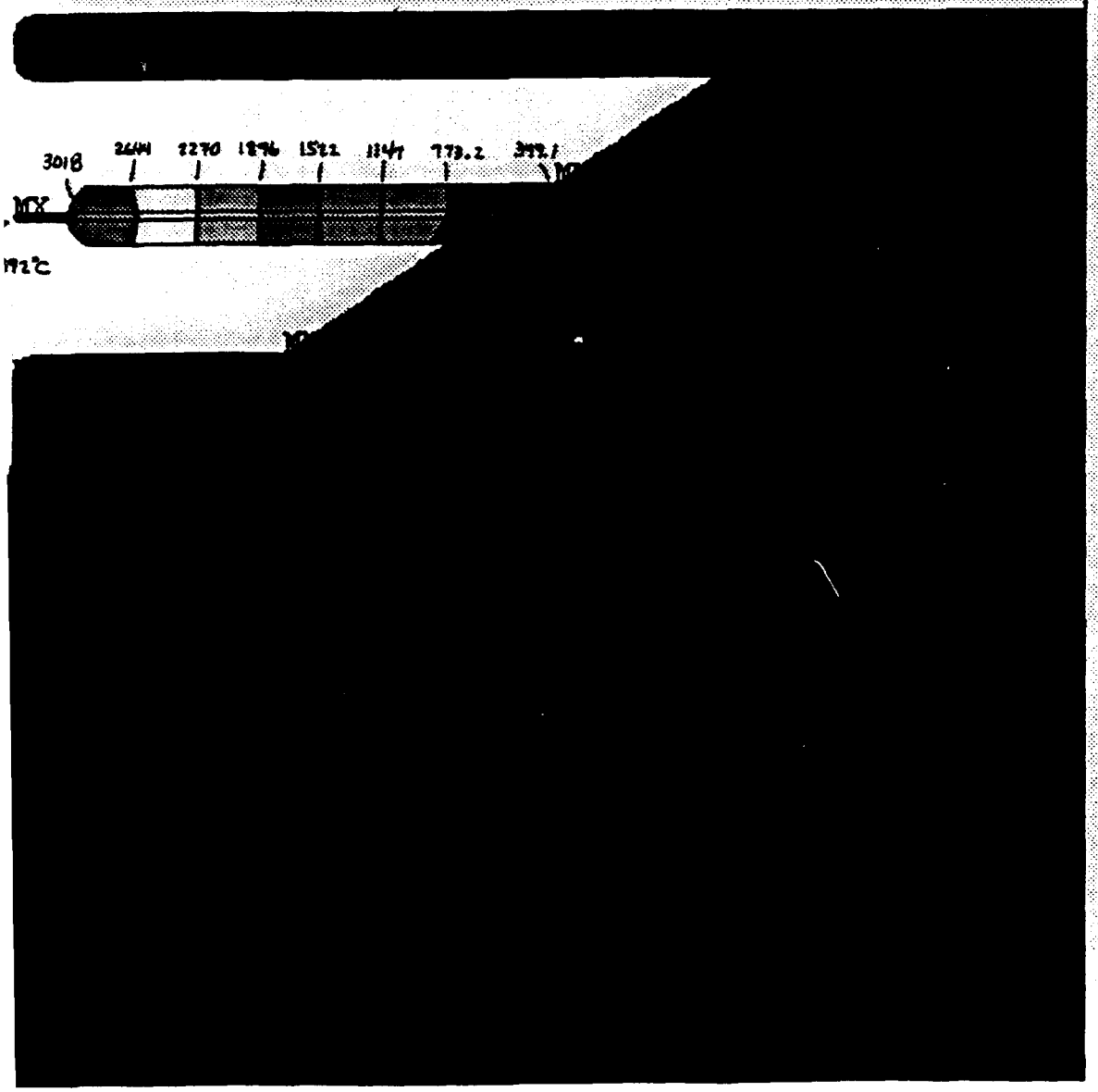
- Continue testing of diodes processed in last quarter. Determine sources of device burn-out. We also plan to determine the uniformity of emission by using a phosphor screen to observe emitted electrons.

- Study the effect of emitter material, layer thickness, smoothness and anode material on the maximum current and transconductance of the devices.

- Carry out further atomic force microscopy experiments to study the roughness and continuity of the deposited metal emitter films.

- Process and test two emitter triode fabrication runs. Demonstrate uniform current emission. Demonstrate modulation of the triode.

e 3.1-5 A thermal contour view of the triode emitter and control electrode
ructure. This load case is heated through ion bombardment which imparts an energy
ual to i*V which is concen-trated in the volume of the emitter tip (specifically, the
gion extending beyond the nitride sheath). The peak temperature is 3392°C which is
ry near the melting point of Tungsten (3387°C).

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*YF  =20.71
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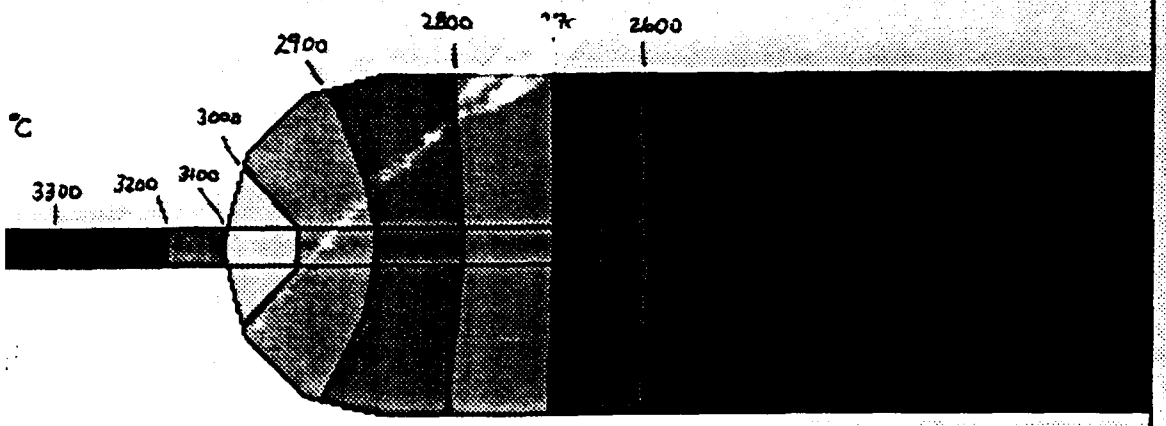
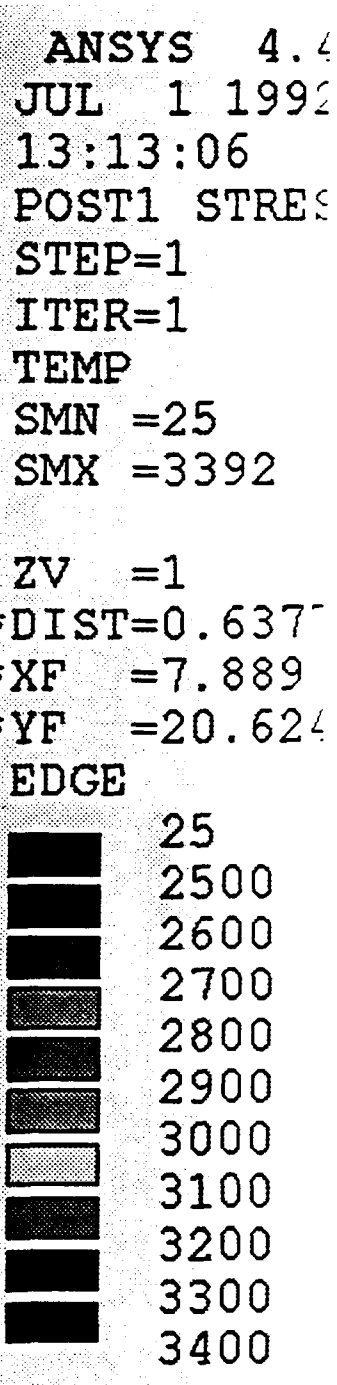
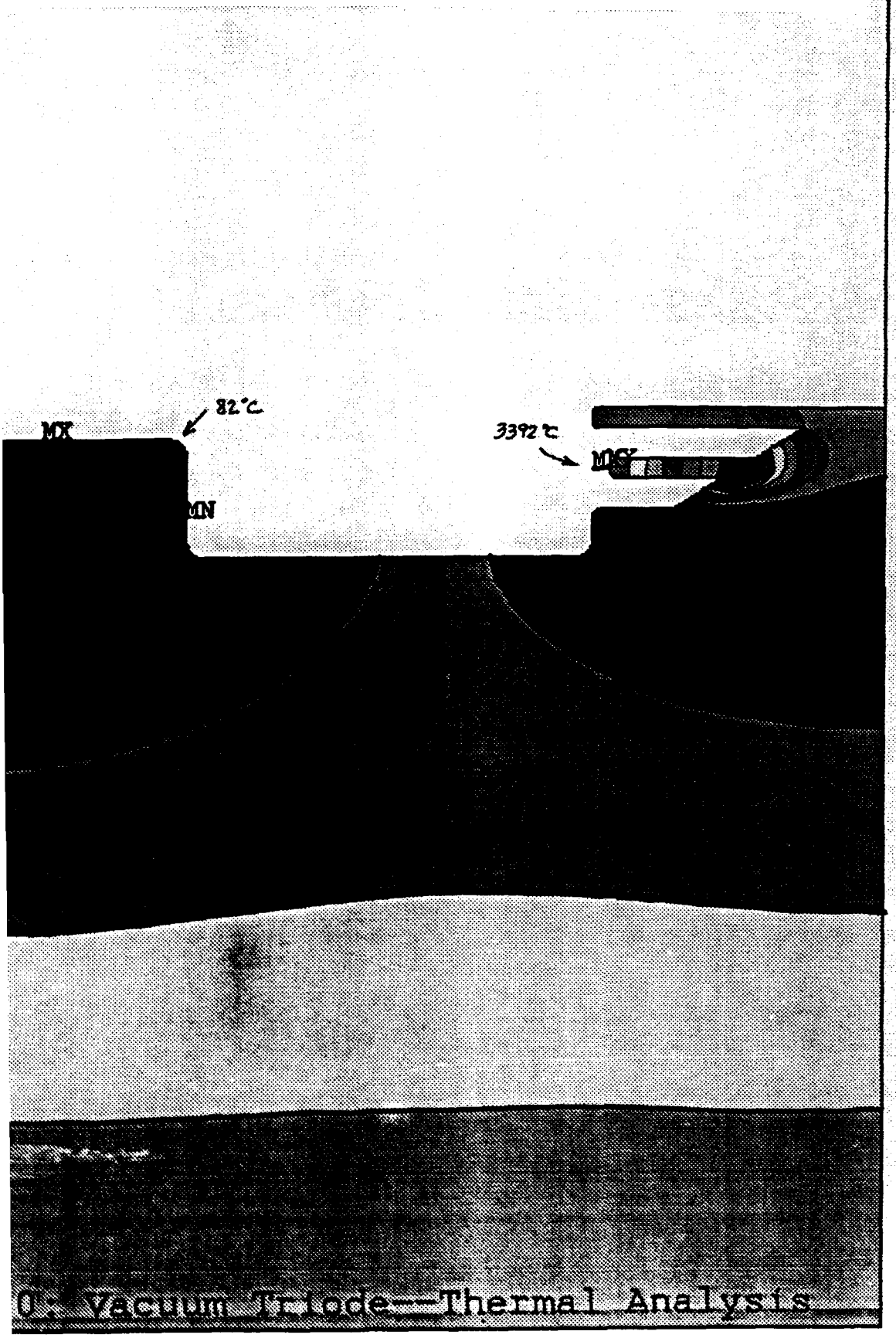
e 3.1-6 A close-up of the thermal contour of the emitter structure from figure 1.





3.1-7 An overall thermal contour plot of the triode structure. Note that there are o heat sources: the emitter and the anode, the emitter is much hotter so there are ıny more contour gradients surrounding it (the temperature scale to the right only ɔlies to the emitter, the rest of the contours are simply meant to show isotherm lines wn into the substrate).

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*YF  =19.18
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      1147
      1522
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      2644
      3018
      3392

 POST1 STRE
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 ITER=1
 TEMP
 SMN =65.27
 SMX =81.95

 ZV  =1
*DIST=9.295
*XF  =5.07
*YF  =19.18
```