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6. AUTHOR(S)

Mr Dave Rowe

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Sierra Monolithics, Inc
103 West Torrance Blvd, Suite 102
Redondo Beach, CA 90277

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The ultimate goal of this program is to design, fabricate and test an ultra-wideband DDS based upon superconducting JJ logic technology which has direct insertion applications in present and future DOD Radar, Communication, or ECM systems. The phase I objectives are to define the DDS system parameters, develop the DDS architecture for the identified system, perform detailed circuit designs and a system performance appraisal. In addition, a teaming arrangement with a superconducting foundry will be evaluated for Phase II device evaluation.

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103 West Torrance Blvd., Suite. 102
Redondo Beach, CA 90277

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1. IDENTIFICATION AND SIGNIFICANCE OF THE PROBLEM

Low instantaneous bandwidth (<200 MHz) direct digital synthesizers (DDS) are finding many uses in military systems such as agile Radars, Low Probability of Intercept (LPI) communications and ECM systems. In each case the system performance is limited by the instantaneous bandwidth of the DDS. For instance, in LPI communication the detection probability decreases with increasing bandwidth. Similar performance degradations are present in Radar and ECM applications which are traceable to the output bandwidth of the DDS.

By using superconducting Josephson Junction technology, a superconducting DDS (SDDS) can be fabricated with an instantaneous output bandwidth which is many times higher than the best GaAs or Silicon based synthesizers. For instance, using conservative performance parameters for JJ logic, an SDDS with an output bandwidth of 4 GHz is shown to be practical. This allows direct instantaneous synthesis of microwave signals for Radar applications, direct PN spreading and frequency hopping for covert communication applications with multi-GHz bandwidths, ultra-wideband communication links, etc.

In addition, an SDDS can greatly reduce the complexity, cost and power consumption of systems such as MILSTAR. By using an SDDS capable of generating the full 2 GHz instantaneous bandwidth, the complex chain of multiplications, upconversions and switched LO's is avoided.

2. PHASE I TECHNICAL OBJECTIVES

The ultimate goal of this program is to design, fabricate and test an ultra-wideband DDS based upon superconducting JJ logic technology which has direct insertion applications in present and future DOD Radar, Communication, or ECM systems. The phase I objectives are to define the DDS system parameters, develop the DDS architecture for the identified system, perform detailed circuit designs and a system performance appraisal. In addition, a teaming arrangement with a superconducting foundry will be evaluated for Phase II device evaluation.

3. PHASE I APPROACH

In this section, the proposed DDS architecture and superconducting logic design will be presented:

3.1 Proposed Architecture

The basic architecture for the DDS will be conventional: Phase Accumulator, Sine-Function Generator, and Digital-to-Analog Converter. The accumulator has a digital input which is proportional to the desired output frequency and the accumulator output is the instantaneous phase of the sine-wave being produced. This operation is accomplished by adding the input word to the accumulated output word each clock cycle. The sine-ROM converts this phase word into an amplitude word each clock cycle. The output of the sine-ROM is converted to an analog signal by a digital-to-analog converter (DAC) and this analog signal is filtered and amplified to form the output of the SDDS system. A simplified block diagram showing this operation is presented in Figure 3.1-1. The detailed architecture, spurious performance and system characteristics are fully described in Section 4.2.

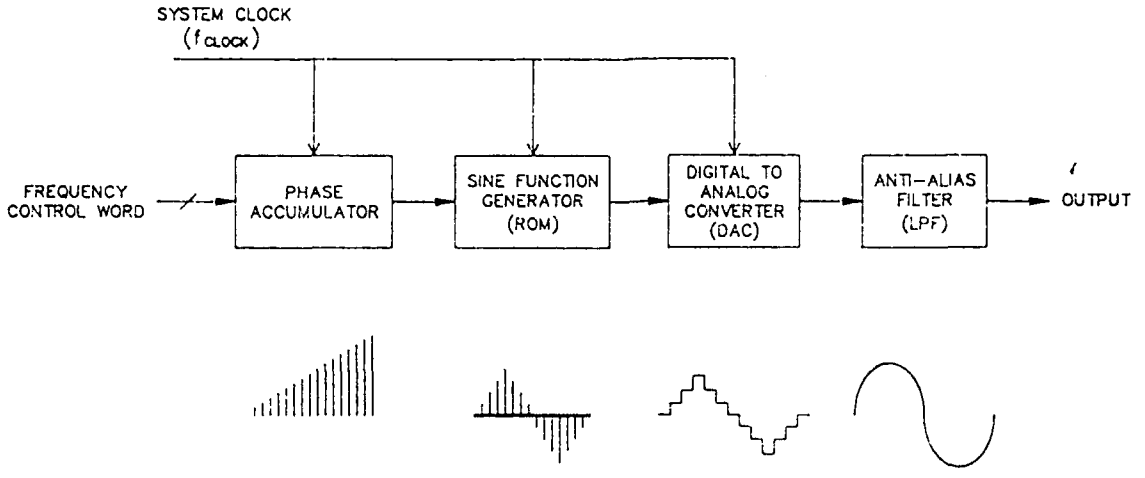


Figure 3.1-1: DDS Block Diagram

3.1.2 Accumulator Approach

For speed reasons, it is necessary to design the accumulator in a pipelined fashion. This eliminates the carry look-ahead operation in the adder and allows the accumulator to operate with an overall speed commensurate with the speed of a single adder/latch cell. With this architecture, it is also possible to design the accumulator so that it is expandable by simply connecting the carry output of the previous stage to the carry input of the following stage. Thus, a 32-bit accumulator can be fashioned from four 8-bit accumulators.

As shown in Section 4.2.3.1, optimum DDS performance is achieved when the phase word is 2-bits longer than the amplitude word. In consequence, the accumulator will be designed with a 10-bit output structure, to match the performance capabilities of the phase IIb 8-bit DAC.

As discussed in Section 4.2.2.1, we will include a toggling "carry in" circuit to minimize accumulator and sine-ROM induced spurs.

3.1.3 Sine-Function Generator

A simple full sine function look-up ROM having an input phase word of 6 bits, and output amplitude word of 4 bits requires a core memory of 64 x 4 = 128 bits. However, a phase quadrant architecture will be utilized, see Section 4.2.3.3. This will reduce the sine-ROM core memory requirement to 16 x 3 = 48 bits.

As the two most significant stages of the phase accumulator are used to control the quadrant of the output waveform, it requires only a simple modification to incorporate a two bit phase control at this point, enabling quadraphase PSK to be performed. We will

design the sine-ROM logic to incorporate this quadraphase modulation feature.

Section 4.2 goes into extensive detail on techniques for algorithmicly reducing the ROM size without compromising the spurious performance of the SDDS. We have chosen a reduction technique known as the 4-2-2 algorithm. The reader is directed to section 4.2 for the impact of this sine-ROM design on chip size and system performance.

3.1.4 Digital-to-Analog Converter Approach

The DAC is the most critical item in a DDS system, and ultimately limits the speed and spurious performance. TRW has recently developed a superconducting 4-bit DAC. Section 3.3.3 gives details on the design and performance of this device.

3.2 Superconducting Logic

3.2.1 Description of Superconductive Logic Architectures

The superconductive SDDS will incorporate Josephson integrated circuits which uniquely combine the fastest logic gates with the lowest power dissipation of any integrated circuit technology. As shown in Figure 3.2-1, the power delay product of Josephson latching gates can be more than 1000 times smaller than the best semiconductors. Other non-latching architectures provide even lower power consumption. The unique performance characteristics of Josephson electronics, combined with the maturity of a niobium Josephson integrated circuit technology, makes possible the development of an ultra-low power, multi-gigahertz wideband SDDS.

Several logic gate architectures have been developed for digital Josephson junction (JJ) applications in recent years. These gate

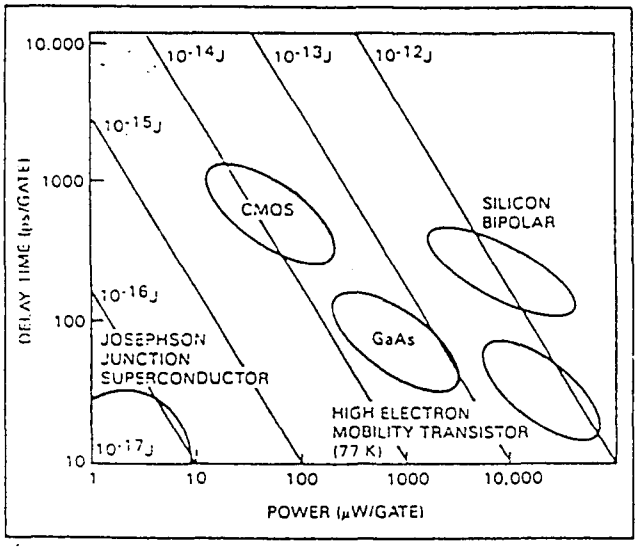


Figure 3.2-1: Power-Gate Delay Comparisons for Josephson Latching Logic Technologies

architectures are primarily based on either voltage-state latching (VSL) or single flux quantum (SFQ, non-latching) logic operation.

In VSL circuits, logic operation is performed with JJ's switching from a superconducting zero-voltage (logic "0") state to a resistive-voltage (logic "1") state. Examples of VSL logic architectures include the best known modified variable threshold logic (MVTL) as well as the four-junction logic (4JL) and the current injection logic (CIL).

Non-latching SFQ logic operation involves detection of the presence ("1") or absence ("0") of fast picosecond voltage pulses in Josephson circuits. A good example of SFQ logic is the recently developed rapid single flux quantum (RSFQ) logic family. The less mature SFQ logic offers the best speed and power performance in Josephson logic circuits. This program will use a combination of the best attributes of these two logic architectures for the implementation of the circuits in the SDDS.

For our SDDS latching logic circuit development, we will use logic gates from the MVTL family. The MVTL gates exhibit wide operating margin, short gate delay, and high current gain. Furthermore, their high speed operation has been successfully demonstrated by others in large-scale Josephson logic and memory circuits in a micro-processor at clocking speeds above a GHz. The MVTL family consists of OR, AND, 2/3 majority gates and a timed-invertor. Together they allows implementation of the required logic functions in the SDDS. A circuit schematic of a MVTL OR gate is shown in Figure 3.2-2. The MVTL OR provides a basic function of input/output isolation and is used to construct other gates in the family. The MVTL gate incorporates an asymmetric, 2-junction, superconducting quantum interferometer device (SQUID) with a single input control line.

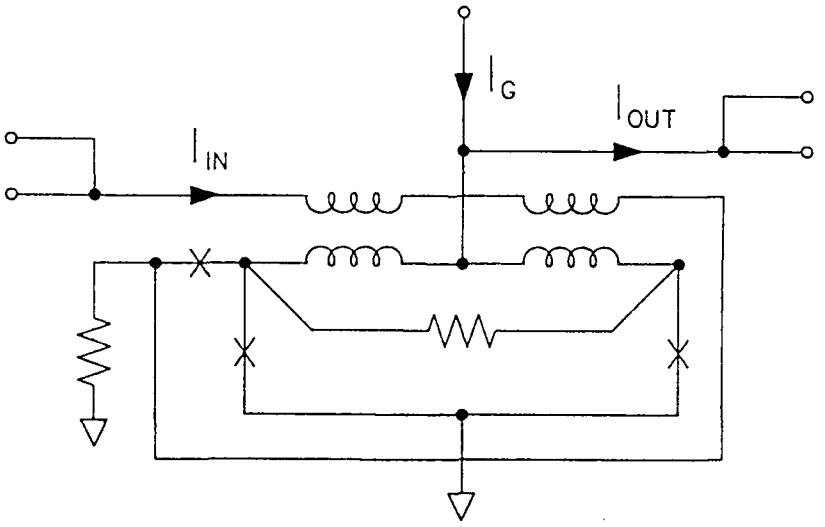


Figure 3.2-2: Schematic of MVTL OR-gate

To provide high current gain, the input is first magnetically coupled to, and then directly injected into the SQUID. MVTL OR gates with gate delays of 10-25 ps have been routinely fabricated and tested using 5 μm gate structures. Gate delays of 2.5 ps and smaller have been measured by others using gates with a smaller 1.5 μm junctions, Figure 3.2-3. Established MVTL gate designs from TRW Josephson microcell library will expedite SDDS logic circuit development. These logic cells have been successfully

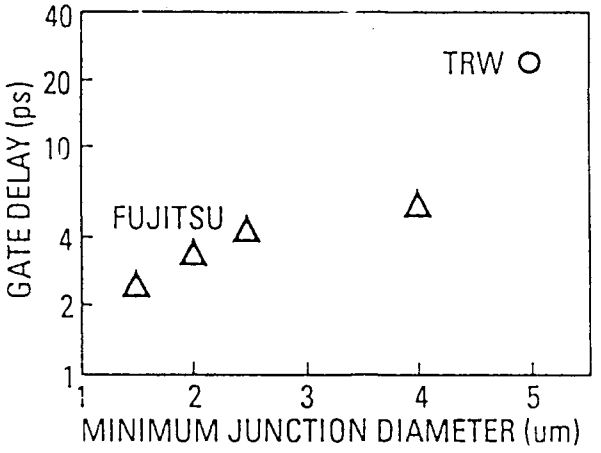


Figure 3.2-3: Measured MVTL gate delays for different juncion sizes

used to implement SSI and MSI level of logic function integration including digital multiplexers and shift registers. The SDDS can be fabricated using a standard TRW niobium process which is well established for both digital and analog Josephson circuits, Figure 3.2-4.

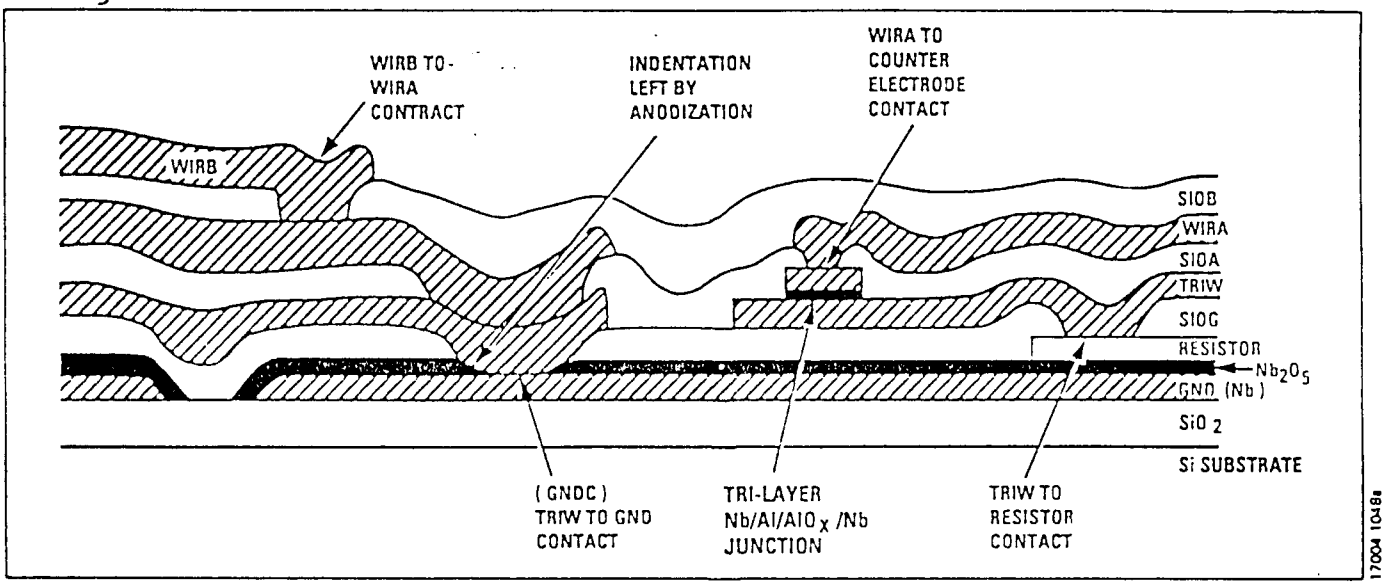


Figure 3.2-4: Cross-Sectional Profile of JJ-110A

On-chip high speed test techniques will be employed to characterize the high speed operation of the SDDS and its components. One technique utilizes an on-chip bypass logic test

circuit to measure critical path delays (sum of gate and line propagation delays). This technique will, e.g., allow the measurement of critical path delay in the sine-ROM to determine maximum access time. A second technique employs an on-chip Josephson waveform sampler to perform equivalent time sampling of high speed transient waveforms with picosecond resolution.

3.3 Circuit Implementation

3.3.1 Accumulator Implementation

The pipelined accumulator incorporates basic MVTL gates along with SSI and MSI logic functions such as shift registers and full adders. The accumulator is powered using three-phase clock signals with offset sinusoidal waveforms. The three-phase clocked design provides several important advantages: reduced junction punch-through probability; elimination of DC Josephson latches required when logic gates reset; and reduction of ground bounce noise. In addition, multi-phase clocking simplifies sequential logic design.

Figure 3.3-1 shows the logic diagrams of a 1-bit full adder and a 1-bit shift register used in the accumulator. The adder is constructed from logic AND, OR, and XOR functions implemented in MVTL gates and is designed to operate with a three-phase clock. The latching characteristic of the MVTL gates and the use of a three-phase clock eliminate the use of latches at the sum and carryout outputs. The de-skewing latches at the adder outputs consist of a simple series of three OR gates each powered from a different clock phase. The 1-bit shift register is also designed for three-phase operation. The data shift, load, and hold functions allow the shift register to operate in a variety of configurations including parallel-in/serial-out, serial-in/parallel-out, and data hold.

The accumulator will utilize existing circuit and cell designs available from TRW's microcell library. The cell design will be optimized as necessary for operation at 4 GHz and higher clock rates.

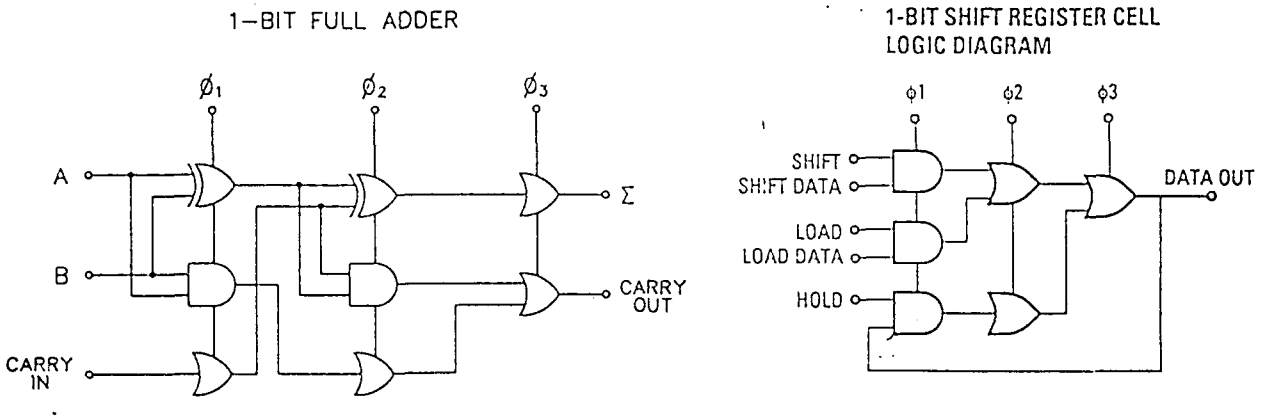


Figure 3.3-1: 1-bit Full Adder and 1-bit Shift Register

3.3.2 Sine-ROM Implementation

The sine ROM in the SDDS will be implemented in VSL. The main requirements of the sine ROM are sub-nanosecond access time and high storage density. To meet these requirements, we will use existing high speed Josephson ROM cell designs from TRW's microcell library. Figure 3.3-2 shows the circuit schematic of the "1" and "0" ROM cells. The "1" cell consists of a symmetric 2-junction SQUID with a single control (word) line. The cell features a wide bias margin (+/- 33%) and a compact layout. The "0" cell uses a modified two-junction SQUID configuration with one junction removed and the other replaced with a short. The "1" cell output is capable of driving a MVTL gate without the use of a buffer. Figure 3.3-3 shows a block diagram of a Josephson ROM. The peripheral logic consists of an OR-tree address decoder which is implemented with MVTL gates. To reduce the ROM access time, cell layout and placement will be optimized to minimize logic and line propagation delays.

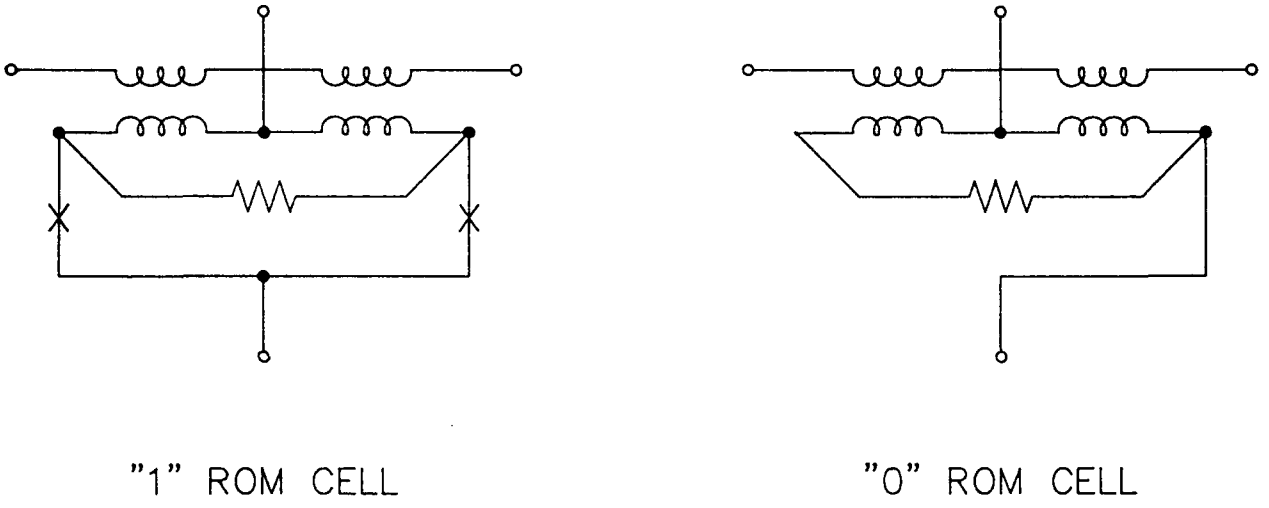


Figure 3.3-2: Josephson ROM Cells

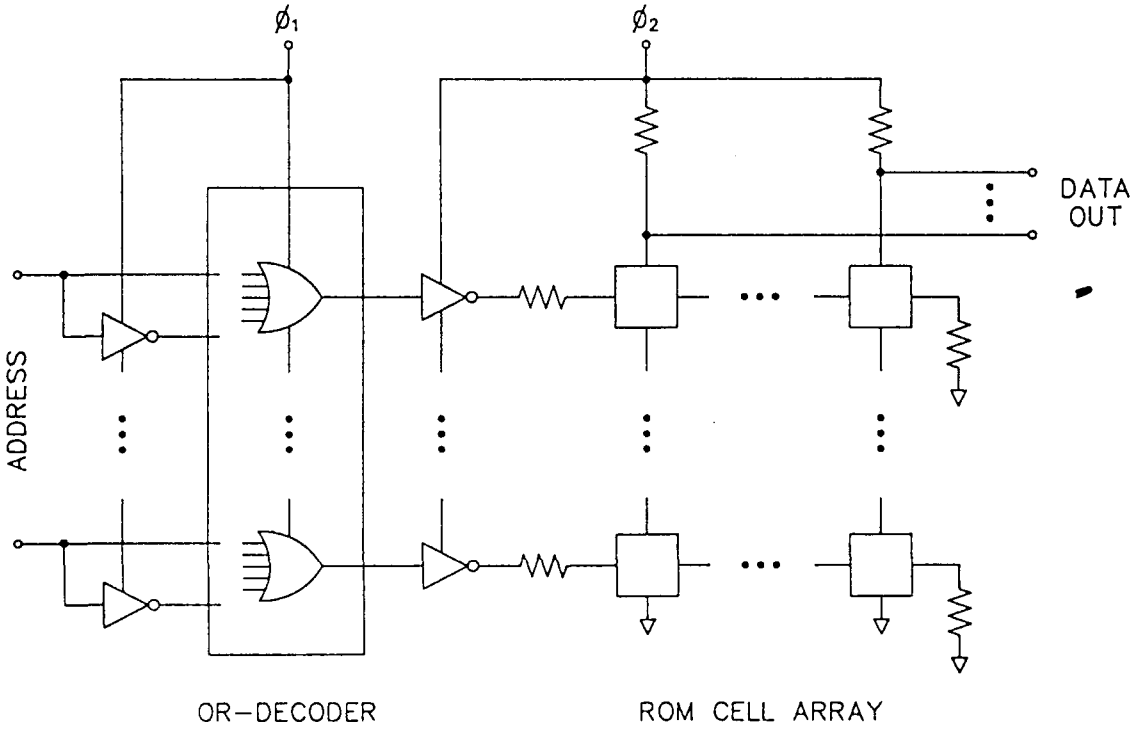


Figure 3.3-3: Josephson ROM Block Diagram

3.3.3 Digital to Analog Converter (DAC) Implementation

The DAC will be implemented using a superconducting single flux quantum (SFQ) ripple counter design, Figure 3.3-4. The flip

flops of the counter successively divide a reference clock by two and establish the exact binary voltages across the flip flops. The generated voltages are related to the frequency (f) by the a.c. Josephson relation $V=K_0f$ where K_0 is universal quantum of flux ($1/K_0 = 483.6 \times 10^{12}$ Hz/V). The outputs of the counter flip flops are fed into output buffer flip flops which are gated by binary

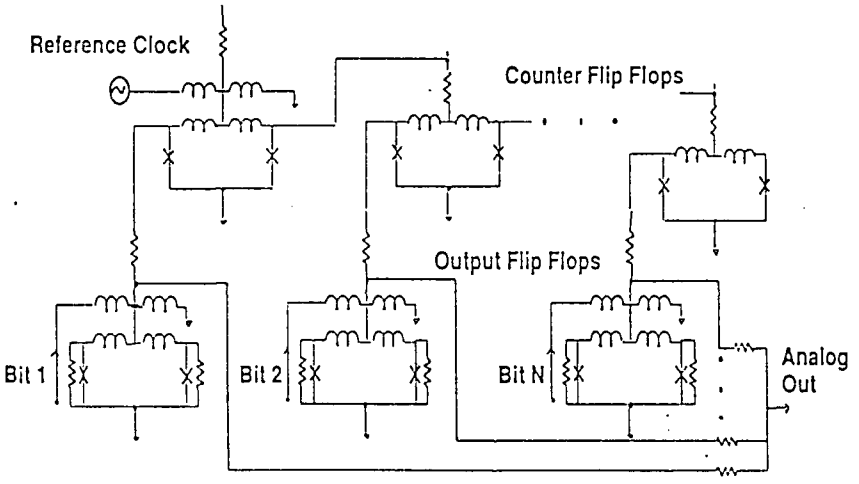


Figure 3.3-4: Asynchronous, Lowpower, Fast DAC

logic levels applied to their flux bias inputs. The outputs are summed by equal output resistors to produce the analog output current.

This DAC architecture has several important advantages: 1) Asynchronous operation: no clock needed to reset latching circuits; 2) Minimal output transients when the input changes; 3) Low power, since no junctions switch to the gap; 4) Fast operation, output flip flops may be turned on and off at gigahertz rates; 5) Requires only N equally matched resistors.

3.3.4 Output Filter

The output filter is used to separate spurious, high frequency artifacts from the slower, sine-wave output. The superconducting DAC averages a signal stream of very high speed pulses (few pico-second wide, micro-volt amplitude). In addition to the desired signal, the 4-bit DAC output contains pulse harmonics ranging from 20 to 200 GHz. Since the SDDS output frequencies are only a few GHz, the wide frequency spread between signal and artifact makes filter designs relatively easy.

Superconducting filters are well-suited to the task of rejecting spurious components. The very low loss of superconductors at microwave frequencies leads to sharper filter cutoff and lower ripple than can be achieved with normal metal filters.

3.3.5 Output Amplifier

The output of the DAC is a few tens of microvolts and therefore requires amplification to be useful in a typical system. An output amplifier will be constructed using GaAs HEMT technology and will operate at the temperature of the superconducting components. The low temperature operation assures that the white noise spectral density of the output will be sufficiently low for target insertion systems such as MILSTAR.

4. PHASE I PROGRESS

4.0 Introduction

This section covers the work performed in phase I of this SBIR program. It consists of a detailed study of the optimum architecture and circuit implementation for a superconducting direct digital synthesizer. In particular, section 4.2 addresses the detailed sine-ROM reduction algorithms necessary to reduce the sine-ROM size so as to make this component buildable in present technology and still meet the target MILSTAR synthesizer requirements. Section 4.3 covers the detailed simulated and measured performance of TRW's niobium process and section 4.4 addresses the problem of efficiently cooling the synthesizer to cryogenic temperatures. The next section reiterates the performance specifications of the target insertion system.

4.1 Target Performance Specifications

The ultimate goal of this program is to insert superconducting DDS technology into a military system, therefore a set of system specifications were established based upon the requirements of the MILSTAR synthesizer and are shown in the following table:

Clock rate	10 GHz
Bandwidth	2 GHz
Frequency resolution	4 Hz
Spurious Content	-47dBc max
Control word	32-bits
Latency	< 5 nS

The detailed architecture, sine-ROM implementation and superconducting circuit designs that follow are based upon these target performance requirements.

4.2 System Architecture Study

The SDDS architecture consists of three basic elements: a Phase Accumulator, a Sine-Function Generator, and a Digital-to-Analog Converter (DAC). In addition an anti-alias filter is included at the output of the DAC. The Phase Accumulator and Sine-Function Generator section of the DDS is often referred to as a Numerically Controlled Oscillator (NCO).

The Phase Accumulator is a digital integrator, it simply adds the input frequency control word to the previously accumulated total, once each period of the master clock. The frequency control word may be thought of as an incremental phase step, and the output of the phase accumulator therefore represents the instantaneous phase of the required output wave-form. The phase accumulator periodically overflows representing a new cycle of the output wave-form. In consequence, the output frequency is a function of the input frequency control word, the master clock, and the size, in bits, of the phase accumulator. A more detailed discussion of the phase accumulator is presented in Section 4.2.2.

The accumulated phase information is presented to the Sine-Function Generator. The Sine-Function Generator is, or is functionally equivalent to, a Read-only-Memory (ROM) which is programmed with a sinusoidal phase to amplitude transfer function. For this reason the Sine-Function Generator is often simply referred to as the sine-ROM. A more detailed discussion of the Sine-Function Generator is presented in Section 4.2.3.

The sinusoidal amplitude information from the ROM is then presented to the DAC, which convert the digital data word into an analog voltage output. The DAC is usually the device that ultimately limits the performance of a DDS system. A more detailed discussion of the DAC is presented in Section 4.2.4.

The output of the DAC is therefore a series of rectangular analog pulses. The width is equal to the master clock period, and the amplitude is equal to the instantaneous amplitude of the required output frequency. Ideally the frequency spectrum of this waveform should only contain the required output frequency, the master clock frequency, and the sum and difference components of these two frequencies. An anti-alias low pass filter with a cut off at the Niquist rate should therefore eliminate all but the required output frequency. However, due to truncation of the output of the phase accumulator, amplitude quantization of the sine-function generator, and the analog accuracy limitations of the digital-to-analog converter, other frequency components occur in band. These other extraneous in-band frequency components are referred to as frequency spurs. The ratio of the worst case frequency spur to the amplitude of the desired output frequency is defined as the spurious performance of the DDS. A more detailed discussion of the DDS spurious performance is presented in Section 4.2.5.

4.2.2 Phase Accumulator

The function of the Phase Accumulator is to generate, store and output the phase information relating to the desired output frequency. The next phase value is calculated as the sum of the current phase information, stored in the accumulator, and the Frequency Control input word, see Figure 4.2-1. This phase information is updated once every cycle of a precision, external, high speed, master clock input (f_{Clk}). The Phase Accumulator, having a finite size, overflows periodically and this overflow rate then represents the desired output frequency (f_{Out}). The relationship between the output frequency and the clock frequency is therefore given by:

$$f_{Out} * \text{Accumulator Capacity} = f_{Clk} * \text{Frequency Control word.}$$

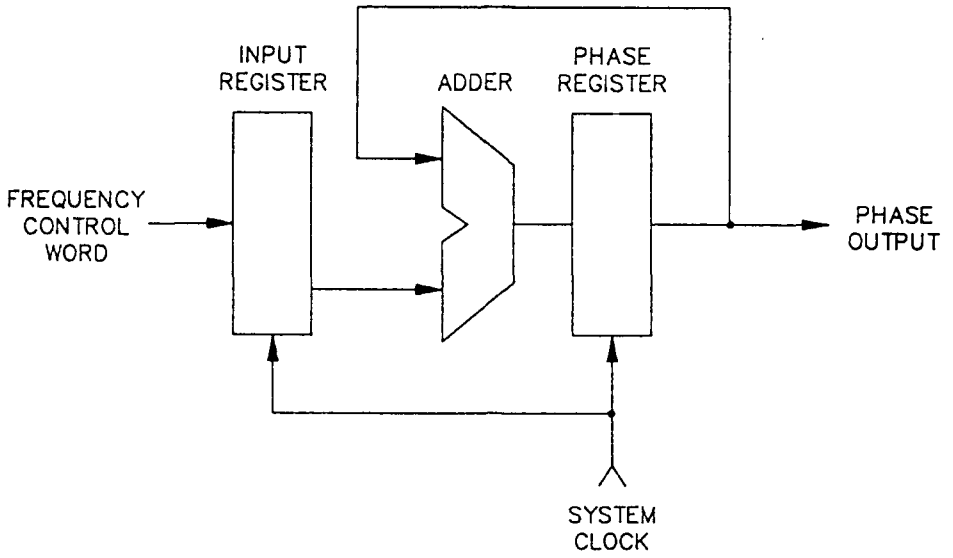


Figure 4.2.1: Phase Accumulator Block Diagram

4.2.2.1 Phase Accumulator Architecture

There are two basic phase accumulator structures; one uses data in the pure binary format, and the other uses data in binary-coded decimal (BCD) format. For a standard, pure binary two's complement phase accumulator of length M bits, the total capacity is 2^M states, and for a BCD phase accumulator, the total capacity is $10^{M/4}$ states. For equal capacities, the BCD accumulator requires approximately 20% more stages than the pure binary accumulator. The only advantage of the BCD phase accumulator, is that if the master clock frequency is an integer power of ten and the output frequencies are expressed as decimal values, the frequency control values can be input directly to the phase accumulator without transformation into the pure binary format. In certain applications where only specific decimal output frequencies are required, the BCD phase accumulator could be advantageous. However, as the BCD phase accumulator requires a more complex arithmetic logic structure involving a three stage carry propagate which limits the maximum operational speed, we elected to consider only the pure binary phase accumulator. The output frequency is therefore given by:

$$f_{Out} = F_r * f_{Clk} / 2^M,$$

where: F_r = value of the Frequency Control word.

Since the DDS is a sampled data system, the maximum output frequency is limited by the Nyquist criteria to 1/2 of the sampling clock frequency, f_{Clk}. In practice, due to difficulty in building anti-alias filters with very sharp roll-off characteristics, the maximum output frequency is usually limited to about 40% of the master clock frequency. The master clock frequency is therefore usually selected to be about 2.5 times the maximum required output frequency.

The minimum resolution of the output frequency is given by setting $F_r = 1$, hence:

$$\text{frequency resolution} = f_{Clk} / 2^M.$$

Therefore, for a given clock frequency and required output resolution the minimum length of the accumulator is given by:

$$M \geq \log_2(f_{Clk}/\text{frequency resolution}).$$

For the target specifications of f_{Clk} = 10 GHz with a frequency resolution of 4 Hz, the required length of the phase accumulator is therefore calculated to be 32 stages (bits).

In a conventional parallel full adder architecture, a carry generated in the least significant stage may have to be propagated through each individual stage, up to the most significant stage. There is a carry propagation delay time associated with each individual stage of a full adder, of at least one AND-OR logic gate. A conventional 32 stage parallel full adder cannot therefore operate faster than 32 gate propagation delay times. In order to overcome this speed

limitation phase accumulators usually employ a pipelined architecture. In a pipelined architecture, the accumulator is split into several smaller sections, each section having a correspondingly shorter propagate delay time. The carry out from each section is then processed by the subsequent section during the following clock cycle. To achieve the absolute maximum possible processing speed the phase accumulator is pipelined into single stage sections. As each stage is delayed by one clock period from the preceding stage, each stage of the input and output data has also to be delayed appropriately. This is referred to as skewing and de-skewing the data. The architecture of the pipelined phase accumulator is shown in Figure 4.2-2. Although this pipelined architecture allows the accumulator to operate at the maximum clock rate, the delays associated with skewing introduce an input to output latency:

$$\text{Latency} = (M + 1)/F_{Clk}.$$

For our 32 stage phase accumulator operating at 10 GHz the latency is only about 3 nS, which is no significance in most systems including MILSTAR.

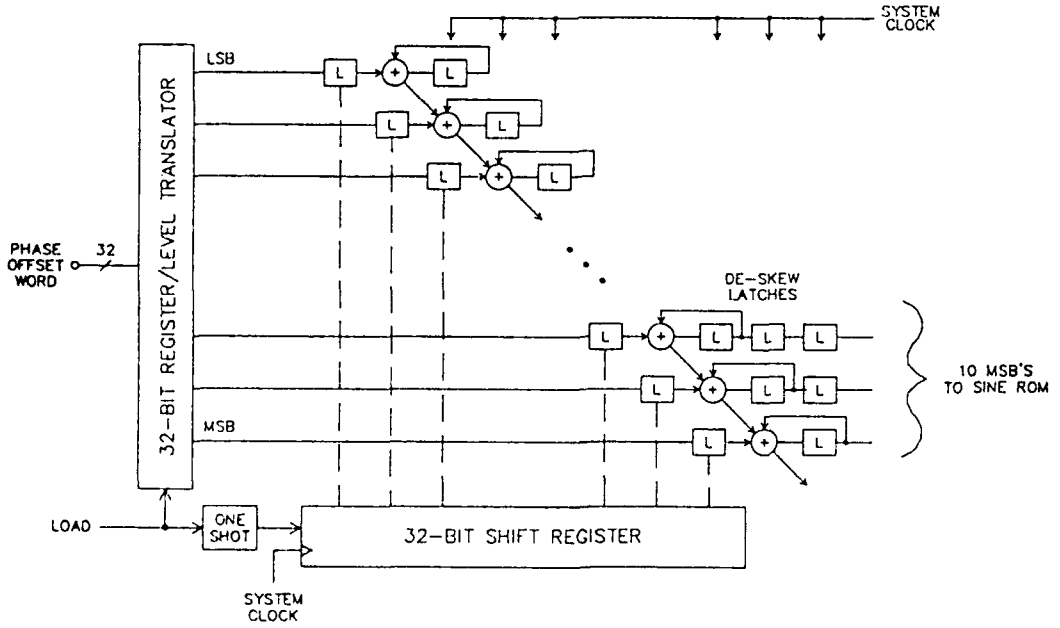


Figure 4.2.2: Pipelined Phase Accumulator Architecture

It is unnecessary to use the full length of the accumulator phase word to address the Sine-Function Generator (ROM). Therefore only the most significant N stages of the phase accumulator are de-skewed for output to the ROM. As the DAC is usually the critical component that ultimately limits system performance, the number of output stages used is a function of the system spurious requirements and the accuracy of the DAC. In order to support a spurious performance of -47 dBc, a DAC with at least 8 bits of resolution, and an accumulator phase word output of at least 10 bits are required, see Nicholas, et. al. [1]. It should be noted that the spurious performance indicated in reference [1] is only achieved if the input phase word is odd, or a toggling carry-in is added to the least significant stage. We will employ the toggling carry-in in order to preserve the frequency resolution of the input frequency control word.

4.2.3 Sine-Function Generator (ROM)

The function of the Sine-Function Generator is to translate the linear phase word "X" from the accumulator into a sinusoidal amplitude function "Y" for the DAC. The basic transfer function of the ROM is therefore defined by the relationship:

$$Y = K*2^{(P-1)}*\sin(2*Pi*X/2^{N})$$

where: K = amplitude scaling factor (approximately = 1)
P = number of bits in the double amplitude word "Y"
N = number of bits in the 2*Pi phase word "X".

4.2.3.1 ROM Addressing

Since the DAC has a limited accuracy and resolution, it is both impracticable and unnecessary to use the full length of the accumulator phase word to address the ROM. However, if the phase

word truncation is too short, the resulting output amplitude errors will dominate and exceed the basic resolution and accuracy of the DAC. The optimum phase word length therefore occurs when the amplitude output errors due to accumulator phase truncation are approximately equal to the basic resolution of the DAC. The worst case amplitude output errors will occur when the rate of change of the transfer function is a maximum. The maximum rate of change of the basic transfer function is given by:

$$dY/dX\Big|_{max} = K*2^{(P-1)}*2*Pi/2^{N} = K*Pi*2^{(P-N)}$$

This shows that if P = N, a one bit phase truncation error will translate into a three bit (Pi = 3.14) amplitude error. Thus, in order not to amplify the phase truncation errors, it is necessary that the resolution of the phase word be at least two bits (a factor of four) greater than that of the output amplitude word. Figure 4.2-3 shows for a P = 8 bit output, how the amplitude errors are reduced significantly by increasing the phase resolution from N = 8 bits to N = 10 bits.

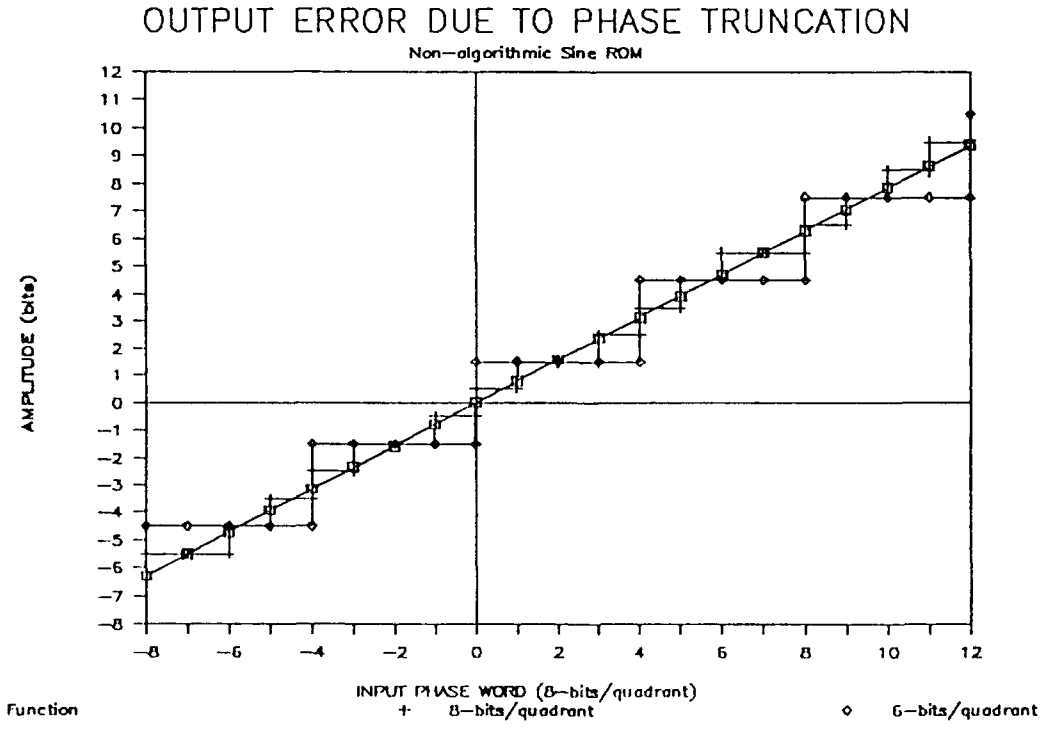


Figure 4.2-3: Ouput Error Due to Phase Truncation

4.2.3.2 Accumulator Phase Truncation Errors

As amplitude round-off quantization is performed at the midpoint of the phase increments, the maximum phase quantization errors occur at the beginning or end of the phase increments. Figure 4.2-4 shows details of the amplitude errors associated with the first thirty-two phase increments for a phase truncation (N = 10 bits) and amplitude quantization (P = 8 bits). Figure 4.2-5 shows all the amplitude errors associated with a full quadrant of the sinusoid. The worst case error for this configuration is 0.88 of a bit.

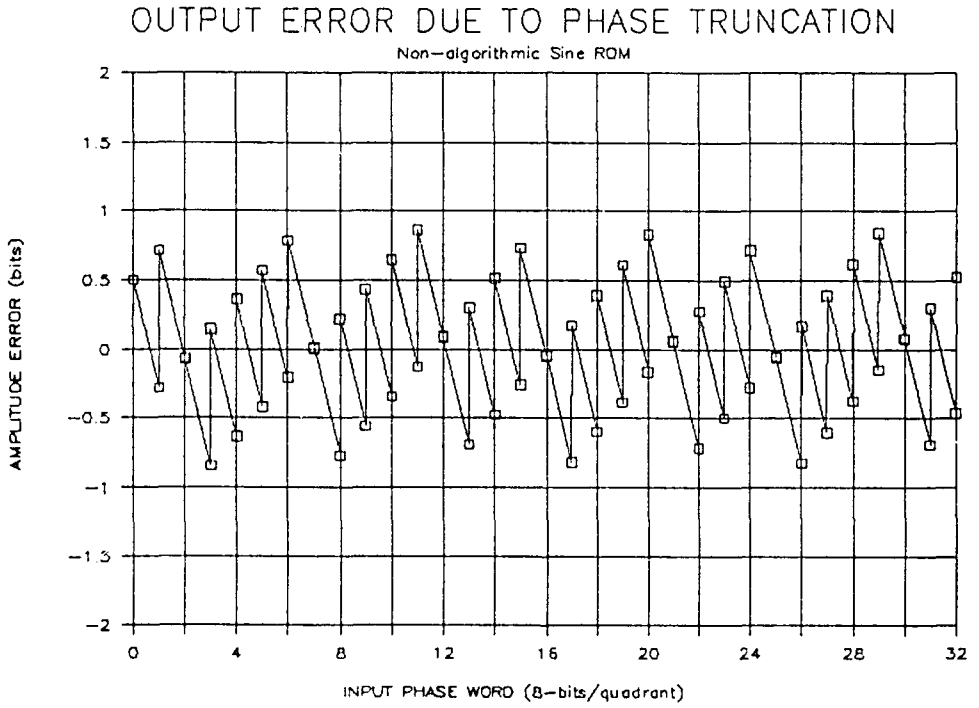


Figure 4.2-4 Output Error Due to Phase Truncation

Increasing the length of the phase word beyond two bits greater than the amplitude word yields very little improvement in the overall error. Table 4.2-1 shows the maximum errors in an 8 bit amplitude output word for various input phase word lengths. For example, increasing the phase word from ten to eleven bits doubles the ROM memory requirements, but only reduces the maximum output error by 0.18 of a bit.

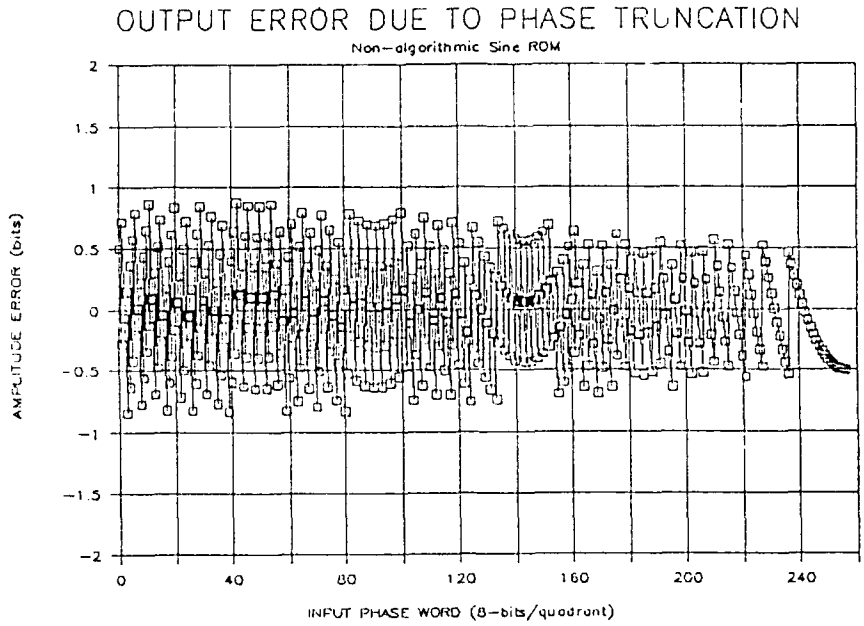


Figure 4.2-5: Output Error Due to Phase Truncation

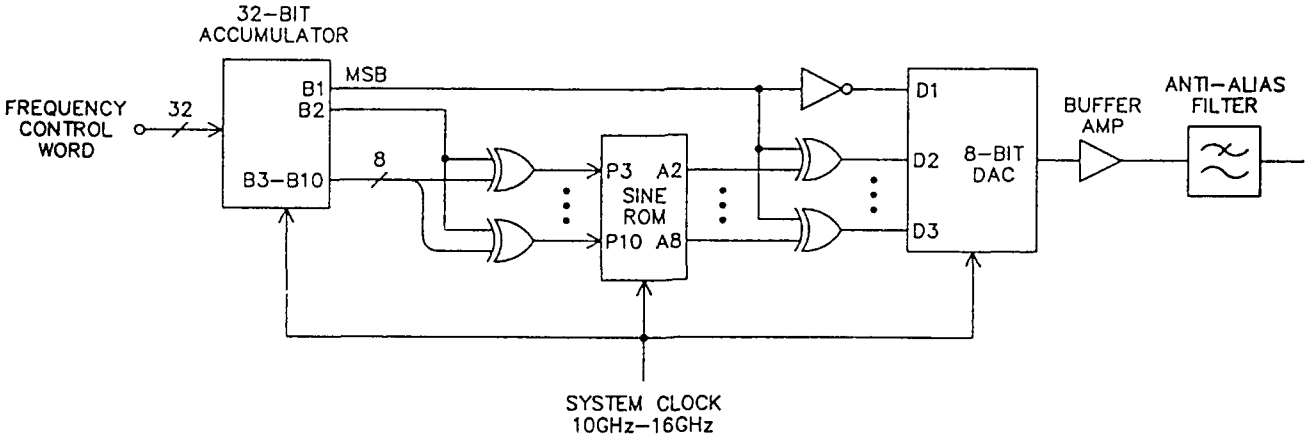
PHASE WORD LENGTH (bits)	MAXIMUM AMPLITUDE ERROR (bits)
8	2.015
9	1.274
10	0.877
11	0.692
12	0.593

Table 4.2-1: Maximum Amplitude Error as a function of Phase Word Length for an 8-bit Amplitude System

4.2.3.3 ROM Core Memory Size Requirements

A simple full sine function look-up ROM having an input phase word of N bits, and output amplitude word of P bits requires a core memory of $P*2^N$ bits. Thus, for the MILSTAR DDS application having N = 10 bits and P = 8 bits, the ROM core requirement is 8192 bits. Since a ROM of this size would compromise the speed and power of the DDS, a number of ROM reduction techniques are employed.

Firstly, the sine function, like all trigonometric functions is symmetrical about the principal quadrant axes. In consequence, it is only necessary to fully characterize the sine function in the first quadrant. The other quadrants are generated by complementing either: the phase word for the second quadrant, the amplitude word for the third quadrant, or both the phase and amplitude words for the fourth quadrant. In this way the memory requirements are reduced by over a factor of four, to $(P-1)*2^{(N-2)}$ bits (1792 bits for MILSTAR). In order to avoid having to perform a true "two's complement" arithmetic operation requiring full arithmetic logic units, a "one's complement" operation is used. This requires only an array of "exclusive OR" gates, see Figure 4.2-6. However, care must be exercised in generating the sine function, by introducing a 1/2 bit offset in both phase and amplitude. The sine function



4.2.6: Sine Function Generator: Simplified Block Diagram

for the "ones complement" ROM is therefore given by:

$$Y = K*2^{(P-1)}*\sin(2*Pi*(X+1/2)/2^{N})-1/2$$

phase offset

amplitude offset

Since the two most significant stages of the phase accumulator are used to control the quadrant of the output waveform, it requires only a simple modification to incorporate a two bit phase control at this point, enabling quadraphase PSK to be performed.

It should be noted that this ROM reduction technique introduces no additional errors over that of the full sine-ROM approach.

The second approach to sine-ROM reduction is based upon the fact that the sine function is approximately linear for small angular deviations:

$$\sin(X + dX) \simeq \sin(X) + \cos(X)*dX.$$

In consequence, linear interpolation can be effectively performed over a limited range of phase values. As the maximum curvature of the sine function occurs at the peak (Pi/2) position, this region is the most resistant to linear interpolation. However, even in this region, linear interpolation over a span of 41 phase increments (8 bit/quadrant phase word) does not cause an amplitude error of more than $\pm$ 1/2 bit (7 bit amplitude word), see Figure 4.2-7.

An effective method of implementing this linear interpolation was introduced by Sunderland et. al. [2]. Higher compression ratios than that of the basic Sunderland architecture have been

achieved, see Nicholas et. al. [3], but at the expense of further circuit

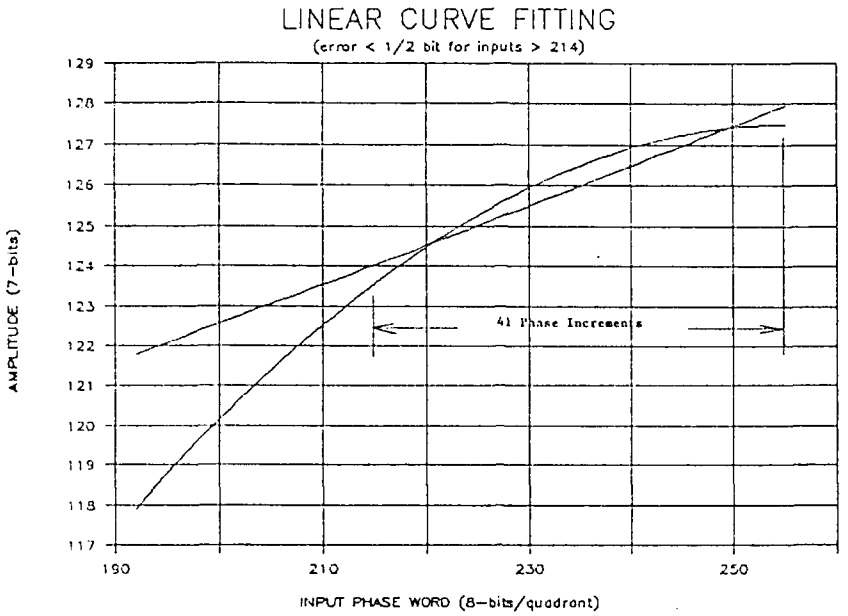


Figure 4.2-7: Linear Curve Fitting

complexity and reduced accuracy. In consequence, we elected to employ the basic Sunderland architecture. This architecture, shown in Figure 4.2-8, replaces the single large ROM by a much smaller coarse and fine ROM combination, whose outputs are added together to reconstruct the full sine function. Addressing of the course and fine ROM's is accomplished by segmenting the quadrant phase word into three sections: the most significant section, the mid section, and the least significant section. The coarse ROM is addressed by the most significant and mid sections of the phase word, and the fine ROM is addressed by the most significant and least significant sections of the phase word. The total number of bits in the mid and least significant sections define the span over which the linear interpolation is performed. For example, if there is a total of five bits in the mid and least significant sections, linear interpolation will be performed over $2^5 = 32$ phase increments, which satisfies the $\pm$ 1/2 bit maximum amplitude error discussed above. However in high speed logic design, different levels of address decoding could

introduce synchronization problems between the coarse and fine ROM sections, therefore the number of bits in the mid and least significant sections of the quadrant

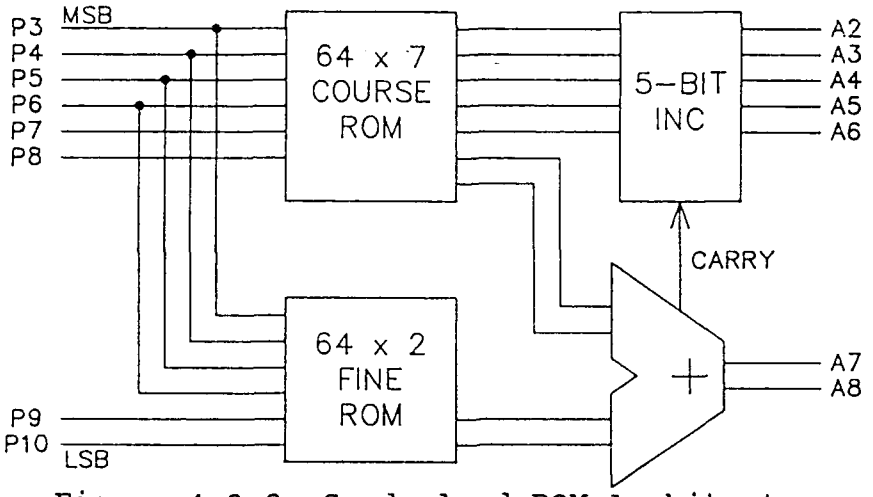


Figure 4.2-8: Sunderland ROM Architecture

phase word need to be the same. In consequence the phase word was divided into the four most significant bits, the two mid section bits and the two least significant bits. This is referred to as a 4-2-2 segmentation. In this 4-2-2 segmentation, the coarse ROM contains 64 words of 7 bits, and the fine ROM contains 64 words of 2 bits. The total memory size is therefore 576 bits, which represents an overall compression ratio of 14.2/1.

It should be noted that unlike the ROM reduction by symmetry, this ROM reduction technique does introduce additional errors over that of the full single sine ROM approach. The reason for this is two fold. Firstly, the fine ROM values are used repeatedly in combination with different coarse ROM values. In consequence the fine ROM value is a compromise of the ideal values required for each coarse ROM value. Secondly, the individual round off errors of $\pm$ 1/2 bit associated with both the coarse and fine ROM's may be additive, resulting in combined errors approaching $\pm$ 1 bit.

4.2.3.4 ROM Core Algorithm Development

An algorithm for determining the programations for the coarse and fine ROM cores was developed. This algorithm is designed to achieve a "best fit" to the ideal sine function. The "best fit" is designed to minimize the absolute magnitude of the individual errors.

4.2.3.5. Algorithmic Induced Errors

As indicated in section 4.2.3.3. above, the linear interpolation compression algorithm does induce additional errors. Using the MILSTAR DDS as an example (N = 10 bits and P = 8 bits), Figure 4.2-9 shows the amplitude errors over a full sinusoidal quadrant using the Sunderland 4-2-2 architecture. The worst case error for this configuration is 1.27 bits, as compared to an error of 0.88 bit without the algorithm. This error introduces a small increase in the spurious content of the SDDS of about 1dB. This slight degradation in spurious performance is deemed acceptable considering it reduces the ROM size by an overall compression ratio of 14.2/1.

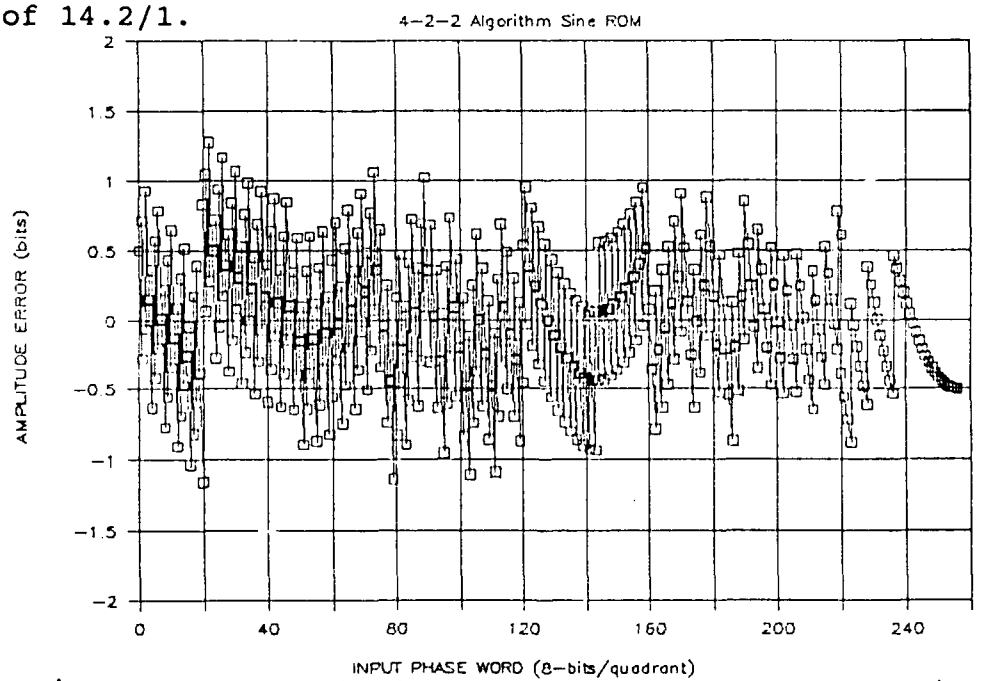


Figure 4.2-9: Output Error Due to Phase Truncation

4.2.4 Digital-to-Analog Converter (DAC)

The sinusoidal amplitude information from the ROM is then presented to the DAC which convert the digital data into an analog output. This conversion process is a very critical step, and the DAC is usually the device that ultimately limits the performance of a DDS system. This is because each bit of information, from the most to the least significant, must generate a precise binary-related analog output to an accuracy better than that of the least significant bit. In addition, the transitions between input states must occur without glitches, otherwise the spurious content will be limited by the glitch energy and not the resolution of the DAC. Remarkably, the TRW DAC does not suffer from either of these problems. Since it is a quantum mechanical device, the quantization levels are precisely defined by fundamental physical constants. In addition, the output of the DAC is a temporal sum of precise pulses which produces no transitional glitches.

4.3 Circuit Design and Simulation

As a part of the teaming relationship between SMI and TRW, TRW has supplied design and simulation results for the circuit elements to be used in this program. We have used these results in predicting circuit performance in the following sections.

4.3.1 Accumulator and ROM

TRW has developed a Josephson logic and memory cell library containing latching gates such as MVTL OR, OR-AND, INVERT, as well as read-only memory (ROM) cells. MVTL logic margins and maturity provide the lowest risk path to a demonstration of a superconducting DDS. Figure 4.3-1 is a layout of a niobium MVTL OR and its measured threshold characteristics. The threshold curves define the boundaries between the zero voltage "0" state

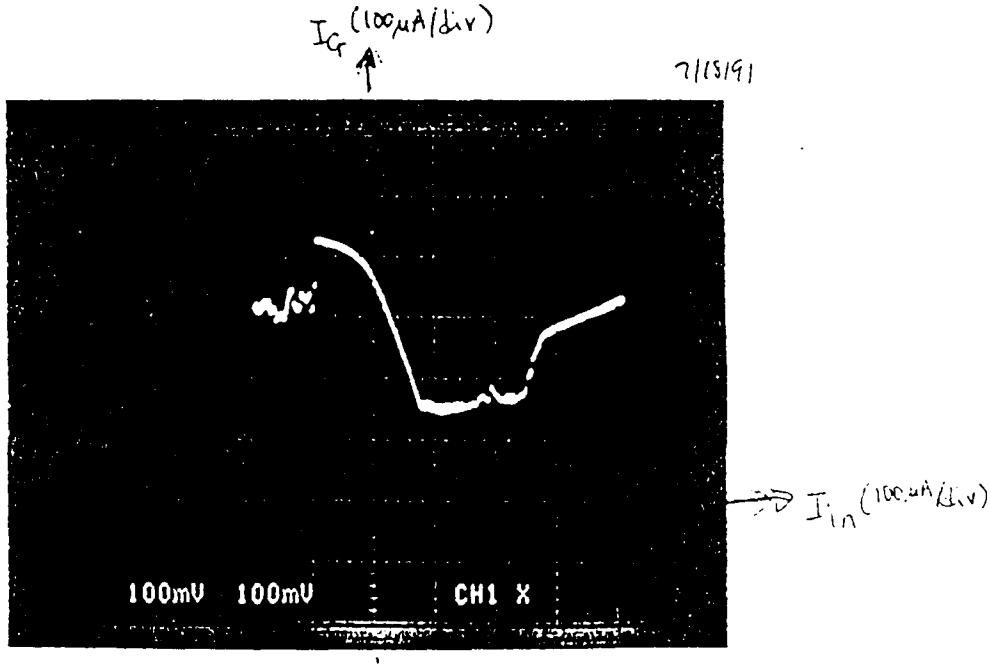


Figure 4.3-1: MVTL OR Threshold Characteristics

and the latched voltage logic "1" state. The gate bias margin and gain obtained from similar threshold curves are ± 33% and 2.5, respectively. High speed gate delay testing of a 40-gate chain and waveforms obtained with the Josephson fast waveform sampler (see Figures 4.3-2 (a) &(b)) further indicate that within the existing design rules, we have designed our basic cells optimally as illustrated by the agreement of our data with the circuit simulation shown in Figure 3.2-3.

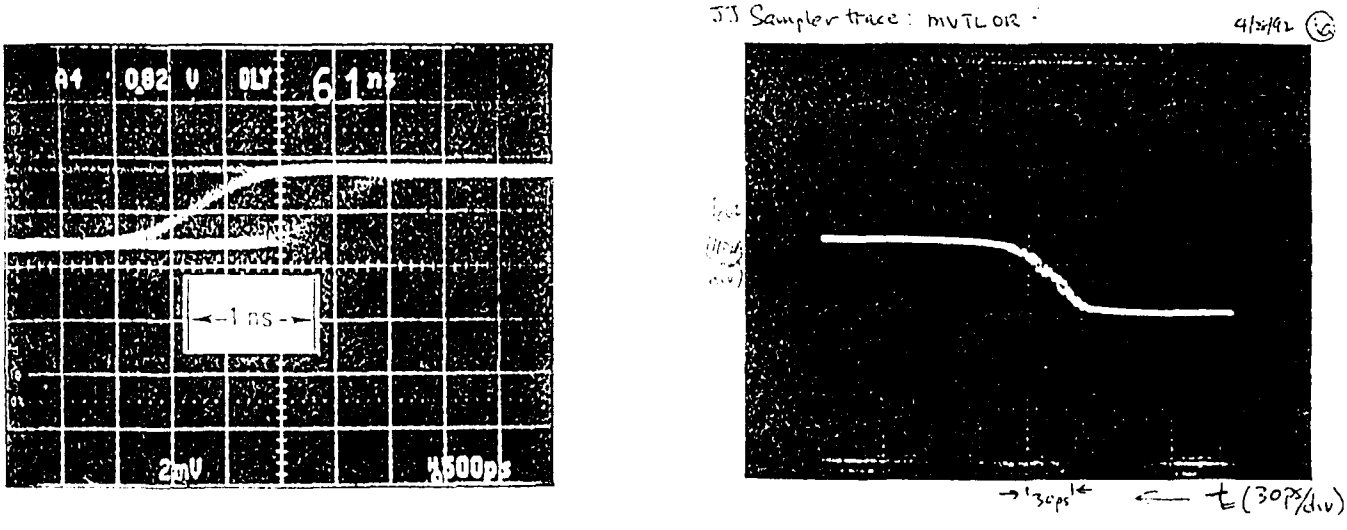


Figure 4.3-2: (a) Measured Gate Delay in a 40 Gate Chain
(b) Sampler Trace of MVTL OR Output

Figure 4.3-3 shows the layout of a niobium ROM cell. The cell provides a compact design for the sine ROM in the SDDS. The measured read margin of the ROM cell is ± 30%, in close agreement with simulation.

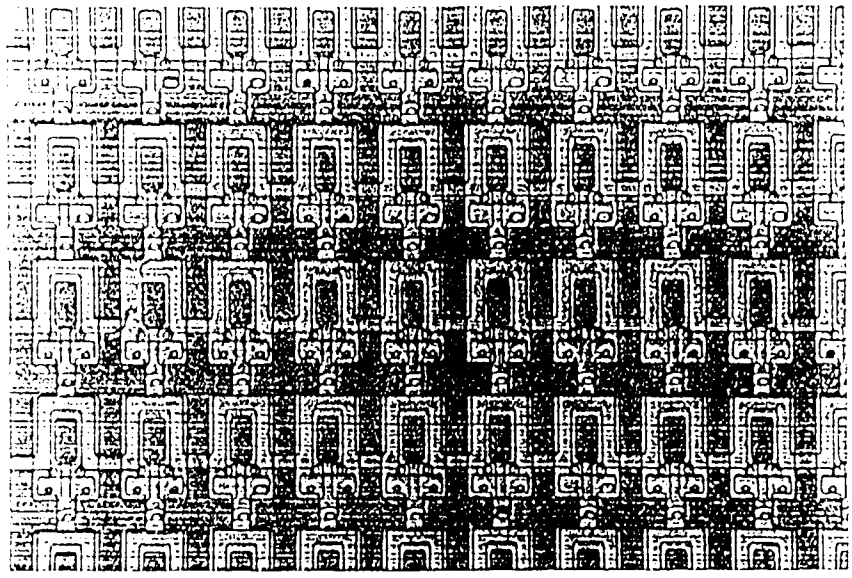


Figure 4.3-3: Section of Josephson ROM Array

Using the basic cell library, TRW designed, fabricated, and tested building blocks with SSI, MSI, and LSI gate complexity. The building blocks currently include shift registers, data registers, adders, multipliers, decoders, counters, and multipliers. Figure 4.3-4 shows functional operation of a 3-phase clocked 4-bit shift register. High speed operation of a 1-bit shift register at clock frequencies up to 5 GHz has been confirmed by circuit simulation. Similar speed performance for the 1-bit full adder design is also confirmed by simulation, Figure 4.3-5.

4.3.2 Digital-to-Analog Converter (DAC)

Figure 4.3-6 is a photomicrograph of one bit cell of a 5 bit DAC fabricated with the Nb process. Four bits of this 5 bit DAC have been successfully tested at input data rates of up to 200 kHz.

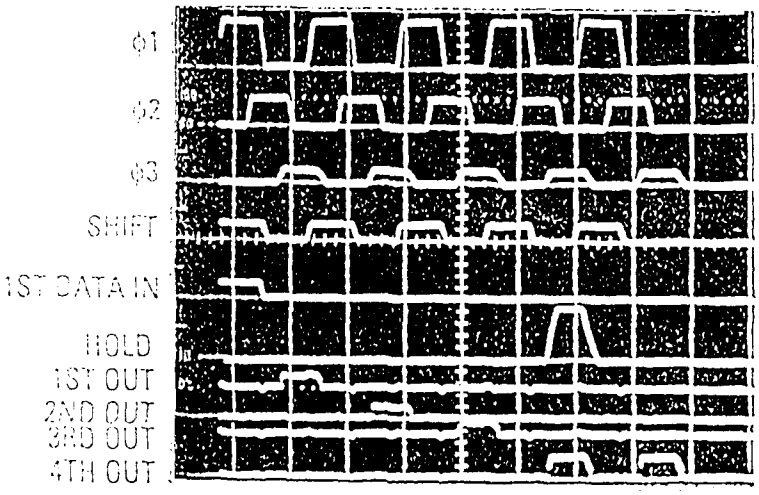


Figure 4.3-4: 4 Stage Shift Register Operation

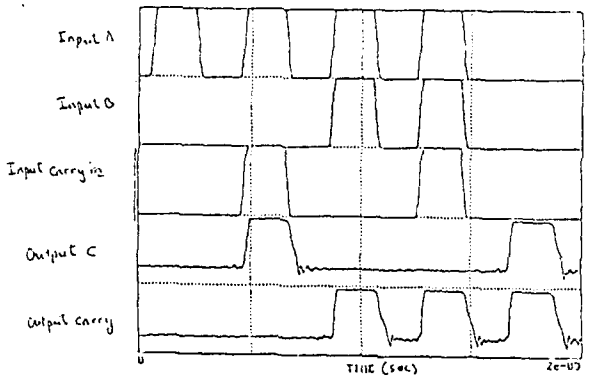


Figure 4.3-5: Simulation of MVTL Full Adder at 2.5 GHz Clock Rate

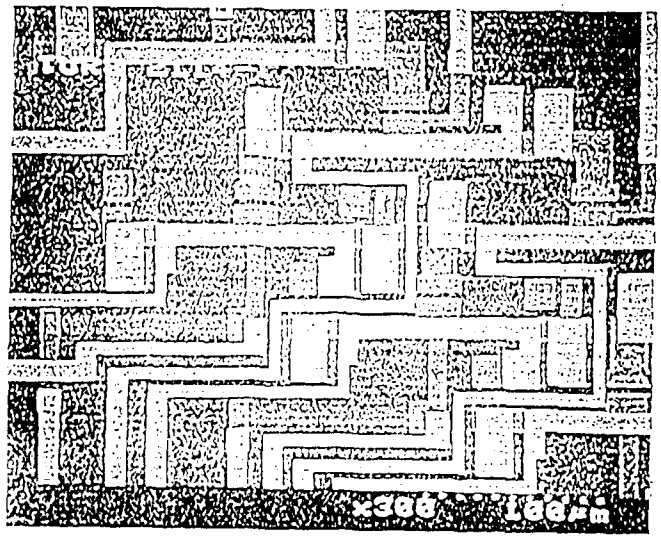


Figure 4.3-6: Photomicrograph of One Bit Cell of a Nb DAC

Figure 4.3-7 shows laboratory data for 2 bit operation. The upper trace is the analog output and the bottom two traces are

the digital inputs. Figure 4.3-8 shows: (a) the full output with 4 input bits (digital input is not shown) and (b) a portion of the output.

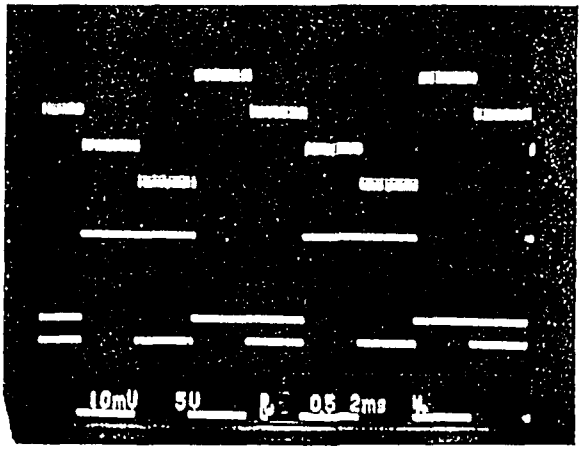
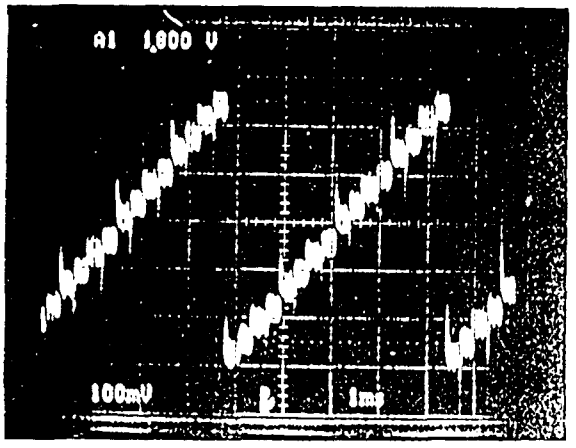
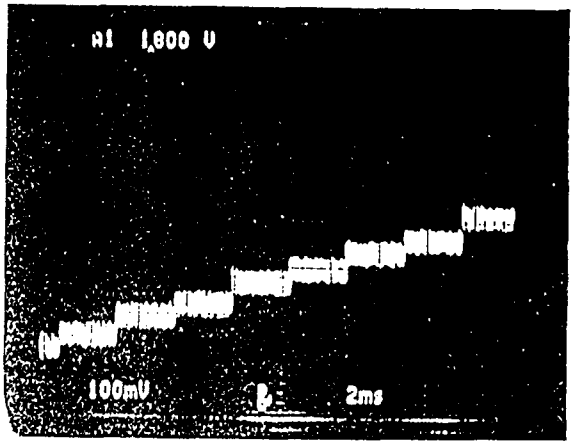


Figure 4.3-7: Operation of a 2 Bit DAC



(a)



(b)

Figure 4.3-8: Operation of a 4 Bit DAC

The resolution and clocking rate of the DAC depends on the upper frequency limit of the most significant bit (msb) flip flop. The msb flip flop in the counter chain has been tested at

approximately 60 GHz. The output flip flop of the least significant bit (lsb) for a N bit DAC would be 60 GHz/(2^N). Thus the lsb output of the 4 bit DAC is running at 3.75 GHz providing nominal DAC output rates of 1-2 GHZ. With layout changes and fabrication refinements, the msb frequency can be increased to above 200 GHz which will be sufficient for the required 4 GHz output bandwidth.

4.3.3 Low-Pass Filter

Low-pass filtering of the DAC output eliminates pulse harmonics from reaching the final SDDS output. The filter must have sufficient bandwidth to respond to changes in the DAC level while also being sufficiently narrow so that pulse harmonics are effectively rejected.

Figure 4.3-9 shows the simulation of a simple 3-pole low pass filter acting on pulses from the superconducting DAC logic elements. Rapid DAC switching from 8 to 0 to 4 to 0 is shown. The filter introduces an additional delay of only 30 ps while essentially eliminating the sharp pulse structures from the logic signal outputs.

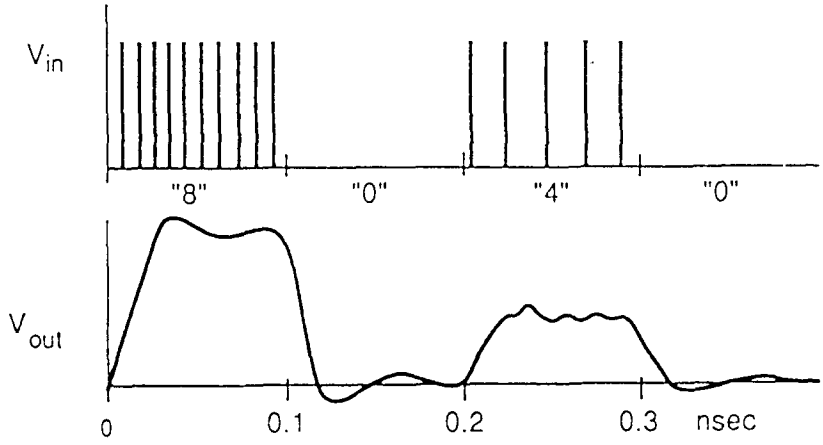


Figure 4.3-9: Simulation of a 3-pole Low Pass Filter

References

1) H.T Nichols III and H. Samueli, "An Analysis of the Output Spectrum of Direct Digital Frequency Synthesisizers in the Presence of Phase-Accumulator Truncation." Proc. 41st annual Frequency Control Symposium USERACOM, Ft. Monmouth, N.J.,MAy 1987, pp.495-502

2) D.A. Sunderlan, R.A. Strauch, S.S. Wharfield, H.T. Peterson, and C.R. Cole, "CMOS/SOS Frequency Synthesizer LSI Circuit for Spread Spectrum Communications" IEEE Journal of Solid State XCircuits, vol. SC-19, pp.497-505, Aug 1984

3) H.T Nichols III and H. Samueli, "The Optimization of Direct Digital Frequency Synthesizer Performance in the Presence of Finite Word Length

3.4 Conclusions

In summary, we have carefully defined the architecture, circuit implementation and testing methodology which will yield an operational SDDS meeting the system requirements targeted for a MILSTAR synthesizer. Sierra will propose a two Phase Program for Phase II. Phase IIa will be a basic operating chip set clocked at 4 GHz will be developed as a proof-of-concept synthesizer and will be used to refine chip-to-chip interconnection techniques. In phase IIb, the sine-ROM will be redesigned for the required accuracy of a MILSTAR synthesizer and an 8-bit DAC will be developed from the existing 4-bit DAC. The logic elements will not change between phases, however, phase IIb will incorporate more aggressive design rules to increase the operating speed of the synthesizer from 4 GHz to 10 GHz.

The result of the Phase II program will be a synthesizer with the following characteristics:

Clock rate	10 GHz
Output Bandwidth	2 GHz
Frequency resolution	4 Hz
Non-harmonic spurs	-47 dBc max
Harmonic spurs	-47 dBc max
Control word	32 bits
Phase control	2 bits (quadraphase)
Latency	< 5 nS

The SDDS will have by far the highest clock frequency, largest instantaneous bandwidth and lowest power consumption of any direct digital synthesizer existing or proposed in the world today.