Research & Development

(2)

R|D

Semiconductor-Metal Eutectic *Composites for High Power* Switching

Final Report

Q. Nguyen
P. Rossoni
M. Levinson
B.M. Ditchek

Research supported by the SDIO Innovative Science and Technology Office and managed by ONR under Contract No. N00014-86-C-0595

GTE Laboratories Incorporated
40 Sylvan Road
Waltham, MA 02254

GTE

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

This report reviews the accomplishments of a research program that sought to develop a totally new material for high-power transistor switching. The material, which we have generally referred to as SME for semiconductor-metal eutectic, is a composite with a high density of aligned, micron-sized metallic rods embedded in a matrix of a semiconductor. This material differs dramatically from silicon, the material used to fabricate almost all other conventional high-power transistors. Silicon is a single-phase pure material. Devices are fabricated from this material through the use of thin-film techniques to incorporate junctions in the surface which enable switching. The composite material contains internal junctions throughout the bulk of the material. Further, it consists of a two-phase equilibrium structure, which because of concerns for defects in the semiconductor, has never before been demonstrated to be of electronic quality, that is, suitable for the fabrication of high-quality devices like high-voltage transistors.

The initial goal for this program was to be the first to take a particular two-phase composite SME material, consisting of a silicon matrix and tantalum disilicide metallic rods, and demonstrate that it could be made into a bulk transistor that utilized the Schottky junction at the interface between the semiconductor and metal phases to pinch off the channels within the semiconductor matrix. Within the first three years of the program, this was accomplished with the demonstration of a device that blocked 1 kV, a high value for a silicon device.[1] The program was renewed for a more developmental phase with the goal of demonstrating a 50 A, 10 kV switch within the next three years, a combination of properties that has never been achieved for a silicon-based transistor, despite the many years of development on conventional silicon transistor devices. This program was well on the way to demonstrating such a goal, when circumstances associated with internal GTE affairs caused the premature termination of the program approximately 15 months early. Within the allotted period, the critical interim goals of 6 kV blocking voltage and the ability to parallel devices for higher current were clearly demonstrated.[2]

The purpose of this report is to summarize accomplishments and the state-of-the-art in SME devices as well as to try to build some excitement regarding this technology so that its unique concept and approach are not abandoned simply because of GTE's exit from this development effort. The potential of this approach is sufficiently high and the concept sufficiently unique that further evaluation and testing should be performed.

Section 2 will review SME transistor fabrication techniques and dc and pulsed properties. Modeling has been used extensively in this program to develop an understanding of the unusual properties of these devices, and this will be reviewed in this section for direct comparison with experimental results. This section will close with a comparison of the SME device performance with the performance of three other terminal devices, like the SIT and the MOSFET. Section 3 will address the materials aspects of these devices. It will show how microstructures features like size, interrod spacing, the distribution of interrod spacing, and rod divergence affect device prop-

erties. The state-of-the-art of materials development for these applications will be reviewed, and based on experimental and modeling results, the potential for advanced materials to generate enhanced transistor properties will be evaluated. Finally, Section 4 will assess the implications of SME transistors for pulsed power applications and will summarize and make recommendations for future work. The final report submitted to ONR at the conclusion of the first three years of the program is included in the Appendix. It includes details that may serve as a useful reference for the new data included in this report. Recent publications are also included in the Appendix.

2. SME TRANSISTORS

The operation of an SME transistor is schematically shown in Figure 1. Current flowing from a source to a drain must pass through a gate. Reverse biasing this gate can expand the depletion zone around the rods under the gate and pinch off the current channels. Although a broad discussion of microstructure effects will be reserved for the next section, it is necessary to make several points regarding the material at this point to help the reader understand basic transistor properties. First, for the benchmark material in which we have made all transistors, the Si-$TaSi_2$, the rod density is about 1.6×10^6 rods/cm^2. Average interrod spacing is about 7 μm, and the diameter of a typical rod is 1 μm. The rod distribution is not regular, as a lithographically deposited structure would be. Rather the rods appear to distribute themselves in the walls of an irregularly shaped cell. Thus current moving from the source to the drain must move around the rods, creating an elongated, twisted path and a higher resistance than would be expected based only on the dimensions and the carrier concentration of the semiconductor matrix. The actual arrangement of the rods is different in the bulk of the material relative to the surface due to slight misalignment of the rods. Maximum divergence of the rods relative to the normal surface has been measured to be 6°. This has been found to be an important defect that alters the blocking voltage properties of the SME transistor.

2.1. SME Transistor Fabrication

SME transistor fabrication really starts with the crystal growth process. Si and Ta are placed in a crucible in a ratio that establishes the net composition as that of the eutectic between Si and $TaSi_2$. The crucible is heated to the eutectic temperature, approximately 1400°C, then contacted on the melt surface with a single crystalline Si seed. In our case, a Si crystal with a (111) orientation was most frequently used for the seed. After equilibration, the seed is raised at a fixed rate, approximately 20 cm/hr, resulting in the pulling of a SME crystal with the microstructure discussed above. Crystals grown this way generally have a Si matrix carrier concentration between 1 and 3×10^{15} cm^{-3}. The crystal is then oriented, sliced into (111) wafers, and suface polished. After this step, the wafers are ready for processing into devices.

Figure 1 also shows the concentric ring design used for the source, gate, and drain contacts of test devices. Fabrication of the device started with oxidation of the SME wafer. Oxidation rates were found to be essentially the same as for Si. The gate contact was produced in vias in the oxide. A cobalt disilicide film was used that forms a Schottky contact to the Si and an ohmic contact to the rods. In certain cases, the gate film was implanted with B to create a p/n junction at the interface with the matrix Si to minimize leakage. The source and drain ohmic contacts were fabricated similarly only substituting an As implant for the B to generate a n^{++} contact and a good ohmic contact to the n-type Si matrix.

2.2. Transistor Properties – DC Operation

The typical transfer characteristic of a semiconductor-metal eutectic transistor is shown in Figure 2. The basic characteristics of the device are similar to those of a conventional metal-semiconductor field effect transistor, or MESFET. Both display a linear region at low voltage, determined by the series resistance, and a saturation region. For a power device, the linear region should be as steep as possible (that is, resistance should be small), the saturation current should be large, and the maximum drain voltage, indicative of the maximum voltage the device will hold-off, should also be high.

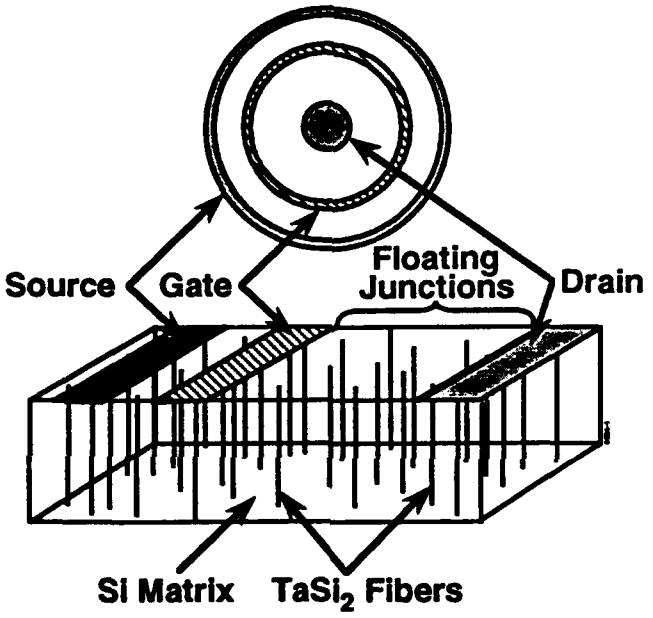


Figure 1. SME transistor geometry.

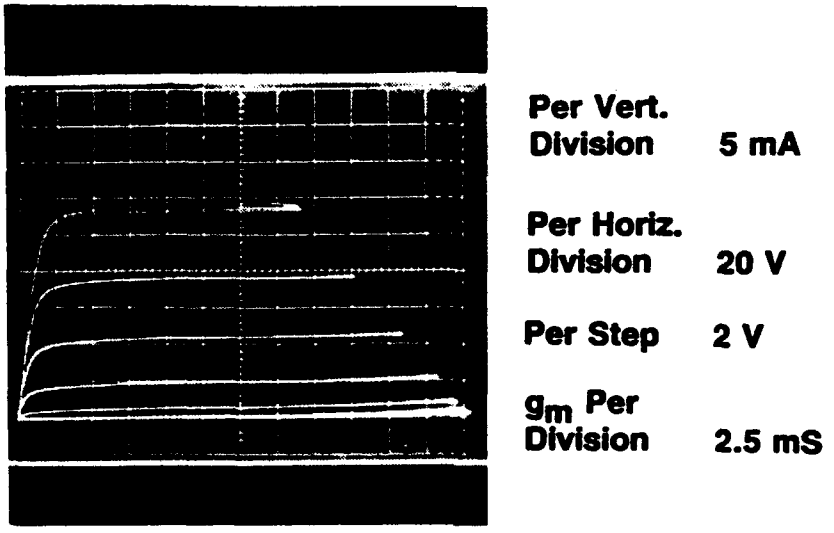


Figure 2. Characteristics of a Si-$TaSi_2$ SME transistor.

Over the course of this program, the factors that affect these parameters, the initial slope, the saturation current, and the maximum blocking voltage of SME devices, have been evaluated in detail. Empirical studies included correlation of device properties with variations in the spacings of the device dimensions, including gate-to-drain spacings and wafer thickness, changes in the device geometry from a concentric ring to a more conventional rectangular design, and material characteristics, such as resistivity. Results from these studies will be presented in this section. With the hopes of achieving clarity, the data will be presented in separate sections on blocking voltage, saturation current, and series resistance. All data presented were taken from dc tests of the transistors on either a Textronix 571 or a Sony/Textronix high-power curve tracer. Pulsed measurements will be presented in the following section.

2.2.1. Blocking Voltage

The highest blocking voltage achieved in a SME device on a dc test to date is 2.2 kV. A curve trace for this device is shown in Figure 3. This high blocking voltage is remarkable when one considers that the maximum breakdown voltage expected for a conventional Si device with a comparable carrier concentration of 10^{15} cm^{-3} is only 0.3 kV based on an avalanche breakdown mechanism.[3] The observed breakdown voltage of SME devices is unusual, in that it does not depend on the carrier concentration (at least within this range), but rather depends on two geometric factors, the gate-to-drain distance and the wafer thickness, as well as temperature and heating effects.

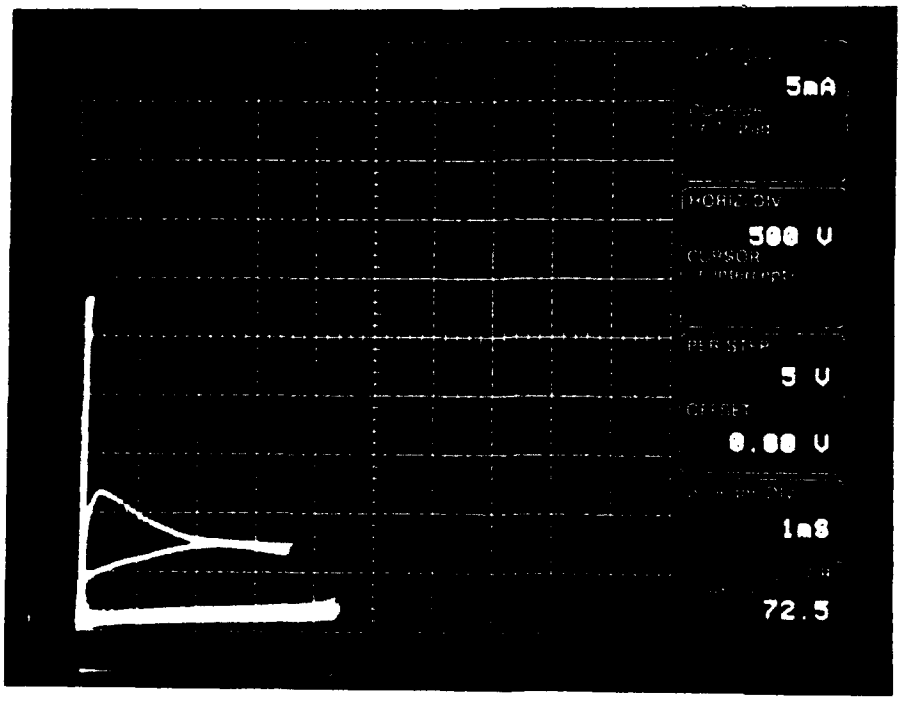


Figure 3. Transfer characteristics of a 2.2 kV SME transistor.

Figure 4 shows how wafer thickness and gate-to-drain distance affect the blocking voltage. The graph shows data on devices from several wafers that were first tested at a 10 mil thickness, then reduced in thickness from the backside by either a polishing or etching step, and retested. This was continued until wafer thickness was about 2 mils. The data on devices with 137 μm gate-to-drain distances was data previously reported in the report dated April 1990 (in Appendix A). The larger spacings used since that time were chosen to achieve higher breakdown voltages. As shown for the 500 μm gate-to-drain spacing data, higher voltages were achieved. However, the desired voltages were not observed until wafer thicknesses were reduced to only 2 mils.

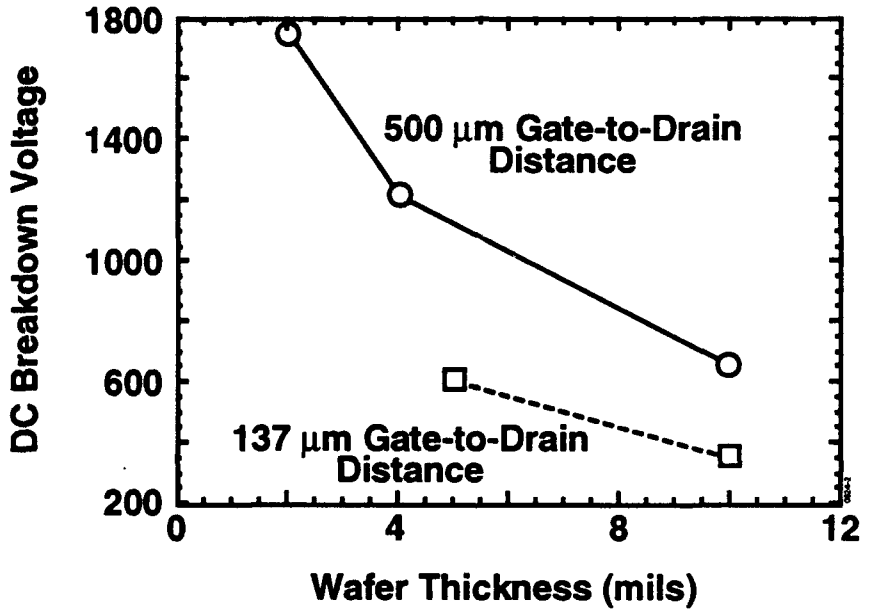


Figure 4. DC breakdown voltage vs wafer thickness.

The effects of wafer thickness and gate-to-drain distance shown in Figure 4 have been consistently observed in all samples. The maximum blocking voltage is predictably about 40 kV/cm multiplied by the gate-to-drain distance in thin wafers (the multiplier is higher in pulsed tests, as will be seen in Section 2.3). Both effects have been explained in terms of the divergence of the floating junctions and their effect on the "effective" gate-to-drain distance. The models used to explain the results will be discussed in great detail in Section 2.4.

For the device shown in Figure 3, the saturation current exceeds 30 mA. With the high voltages involved and the long times required to achieve the curve trace (approximately 17 ms), the device under test can get hot. Heating during the period of transistor testing can affect leakage currents and give a false indication of breakdown even before avalanching can occur. Thus the data in Figure 4 can be partially affected by thermally induced leakage. Nevertheless, it is clear that the trend of increased breakdown with reduced thickness or increased gate-to-drain distance is certain, as it has been substantiated with pulses too short to enable heating, about 1 μs.

2.2.2. Saturation Current

The saturation current is an important parameter for a power device in that it reflects the maximum current switched for a given device. For the SME device, all concentric ring devices were test structures, designed to determine maximum blocking voltage rather than demonstrate high switching current. To increase the saturation current, a new oval structure, as shown in Figure 5, was used to increase device area. Thus in this section, it is important to discuss the saturation current in a normalized sense that will enable the reader to evaluate potential switching capability. All data in this section will be for transistors on wafers that were thinned to 2 mils, because that is the case that yields the highest blocking voltages.

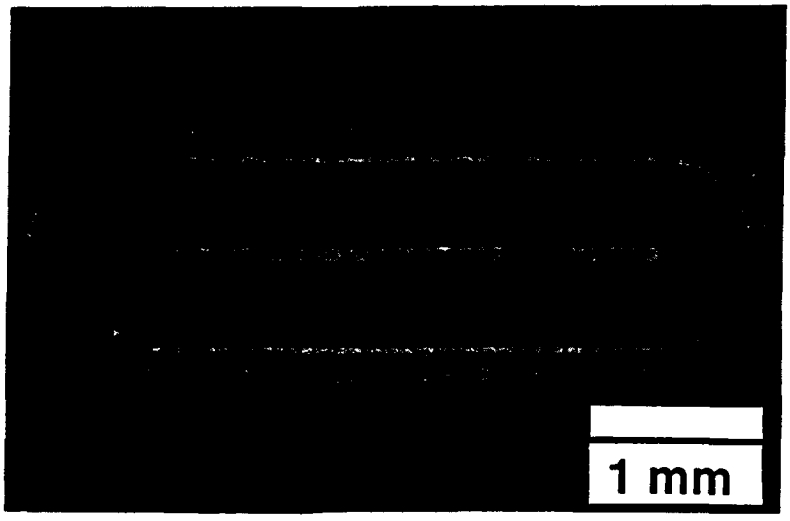


Figure 5. Oval structure for high-current devices.

The saturation current can be normalized either of two ways. If the current is normalized with respect to the surface area of the wafer, A_s, occupied by the transistor, a switching current density is specified that is relevant to the size and, presumably, cost of the device. The current can also be normalized with respect to the cross-sectional area for current transport, A_c. In the concentric ring design, the cross-sectional area for current transport changes since there is current crowding as current moves from the large diameter source contact to the small diameter drain contact. An averaged value, which is less dependent on the specific geometry, is given by

$$A_c = 2\pi t\,(r_{source} - r_{drain})/\ln\,(r_{source}/r_{drain}). \qquad (1)$$

In this equation, t is the wafer thickness, r_{source} is the inner diameter of the source contact, and r_{drain} is the outer diameter of the drain. Using this cross-sectional area, a current density is attained which is more indicative of the physical current density, and is a preferred parameter when comparing this device to other power devices. Sample data, covering several wafers and different device designs, is shown in Table 1. The uncertainty in the cross-sectional current density, J_c, is

larger than in the surface area current density, J_s, because of a substantial uncertainty in the wafer thickness of about ± 25%. Surface current densities range from 0.36 A/cm² to 1.2 A/cm², and cross-sectional current densities range from 15 to 26 A/cm². The saturation currents are considered representative and typical, but it should be noted that even in a given wafer, considerable variability in I_{sat} is observed.

Table 1. Sample Data for Various SME Devices

Device No.	G-D Distance (μm)	r (Ω-cm)	I_s (mA)	R_s (Ω)	J_c (A/cm²)	J_c (A/cm²)
85-5 N11	500	46	30	5000	1.21	26
85-29 H9	1000	31	25	1667	0.36	15
70-24 C16 (Oval)	500	17	77	172	0.98	19

The table shows that increasing the gate-to-drain distance to achieve high voltage adversely affects the switchable current per unit surface area of the wafer but does not substantially lower the current normalized to the cross-sectional area. Although the surface area normalized currents may be considered low, the cross-sectional current density is high. This will be discussed further in Section 2.5.

To create devices to switch large currents, it will be necessary to parallel devices. Figure 6 shows the transfer characteristics of a "device" that is composed of four devices in parallel, each with the saturation current shown in the insert. The total saturation current for the net paralleled device is approximately equal to 80% of the sum of the saturation currents for each of the four devices. Improved techniques for wire bonding, or using metallizations directly on the wafer, would likely result in even better efficiency in paralleling. This result indicates that the creation of large current switching devices, as well as high blocking voltage devices, will be possible through the paralleling technique.

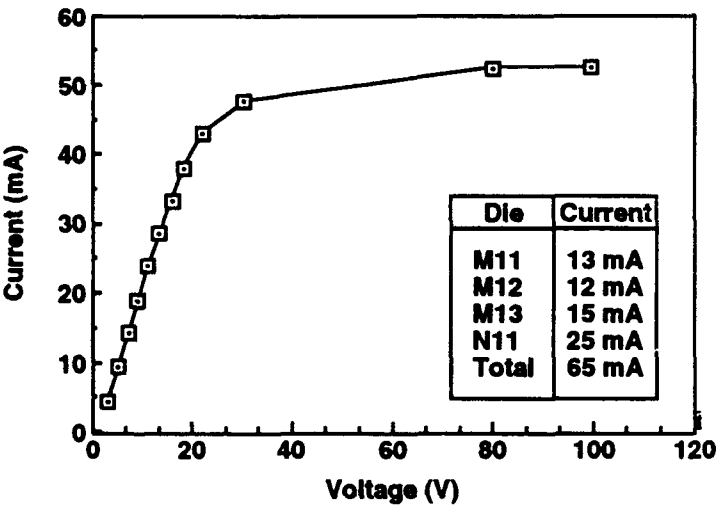


Figure 6. Transfer characteristics of a parallel device.

2.2.3. Series Resistance

Table 1 also shows the series resistance for each device, calculated as the ratio of 50 mV with the drain current at 50 mV. This may be compared with the expected resistance based on the resistivity measured for the particular wafer and the "effective" cross-sectional area and length of transport. When the comparison is made for these 50 μm thick devices, agreement is excellent, indicating that the contacts are good and that the entire thickness is being utilized as the current channel.

As a result of the relatively high resistivity of these wafers (good devices require a resistivity exceeding 10 to 15 Ω-cm), the long gate-to-drain distances needed to achieve high voltage, and the small size of the devices, the series resistance of these devices tends to be high. As in the oval, large area device, small series resistance can be achieved by scaling-up the size of the device to achieve high currents.

2.3. Transistor Properties – Pulse Tests

The three circuits employed to pulse test SME devices are shown in Figure 7. The highest voltage pulses were generated with the spark coil circuit shown in Figure 7(a), with either the 4 kV Xenon flash coil, which generated a 700 ns pulse, or a 25 kV automotive spark coil, which generated a longer 80 μs pulse. These tests were operated with the gate of the transistor shorted to the drain so that maximum saturation currents flowed through the transistor during pulse testing. Figure 8 shows the voltage waveform in a 1200 V test for a SME device with a 500 μm gate-to-drain spacing and a conventional MOSFET rated at 500 V. The figure shows that the SME device readily supports the high-voltage pulse, but the MOSFET does not. An example of the voltage waveform with the automotive coil is shown in Figure 9 as a 1000 μm gate-to-drain distance device is tested. The device is clearly demonstrated to support a full 6 kV. Above 6 kV, the device breaks down, indicating that 6 kV for this device is the maximum blocking voltage.

It should be noted that all devices tested using this circuit were tested in the same probe station used for the dc tests, but the entire wafer, including the device under test, was immersed in transformer oil. Devices not immersed in transformer oil did not support a high voltage and showed to the observant eye a spark between metal probes contacting the device.

Figure 10 shows the results of pulse test measurements of breakdown voltage on several devices with different gate-to-drain distances at different wafer thicknesses. As for the dc tests, the breakdown voltage increases as the thickness decreases, supporting the concept that the divergence of the rods limits the breakdown voltage in thick wafers.

In the pulse tests described above, the SME transistor assumes a passive roll; however, using the circuit in Figure 7(b), the high-voltage pulses can be generated using the switching capability of the transistor itself. By passing a current through an inductor and test transistor, connected in series, the magnetic field stored in the inductor is converted into a high-voltage pulse at the drain of the transistor as the transistor is switched from the on-state to the off-state by the –10 V output of the pulse generator. The pulse generator responds with a 6 μs wide pulse with a 20 ns rise and fall time.

A voltage pulse generated with this circuit using a 10 mil thick SME transistor is shown in Figure 11. The pulse generator results in the switching of 60 mA and the generation of a 0.5 kV pulse within the time period of 5 μs for the pulse. The rise and fall time for the –20 V pulse from the pulse generator is only 20 ns. As the voltage curve has not saturated, it is clear that a longer pulse would have generated a higher voltage. With a slight modification of the circuit so that a 10 Ω resistor is placed in series with the transistor and the oscilloscope is set to track the voltage drop across the resistors [Figure 7(c)], the current pulse can be measured. This is also shown in Figure 11, and an expansion of the time scale at the switch opening portion is shown in Figure 12. The current drops from its maximum to minimum value in approximately 15 ns. Thus, the opening time of the switch has been shown to be 15 ns or less. With a faster pulse, the opening time for the switch may be shown to be faster.[2]

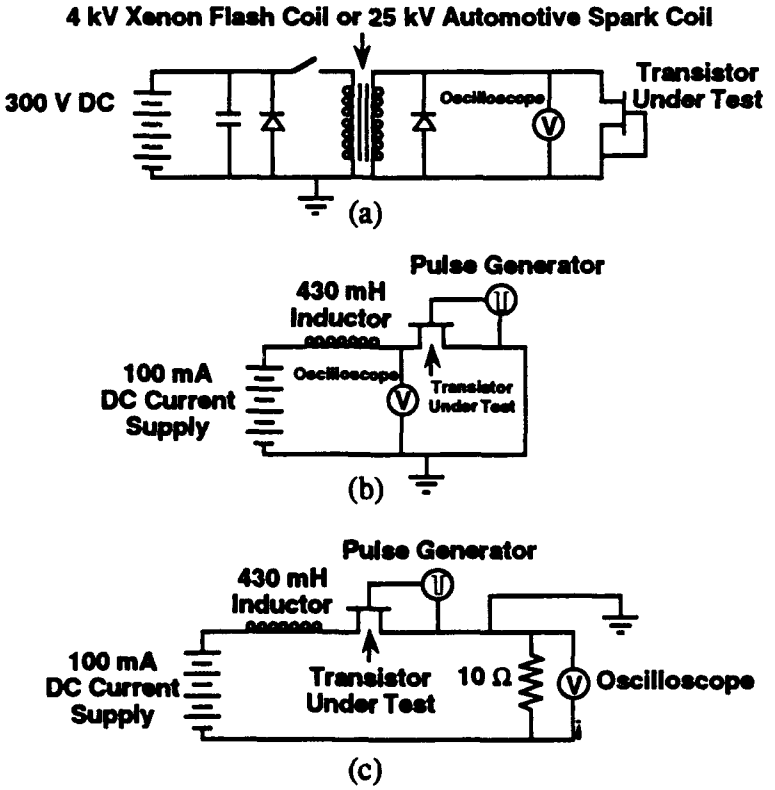


Figure 7. Circuit diagrams employed to pulse test SME devices.

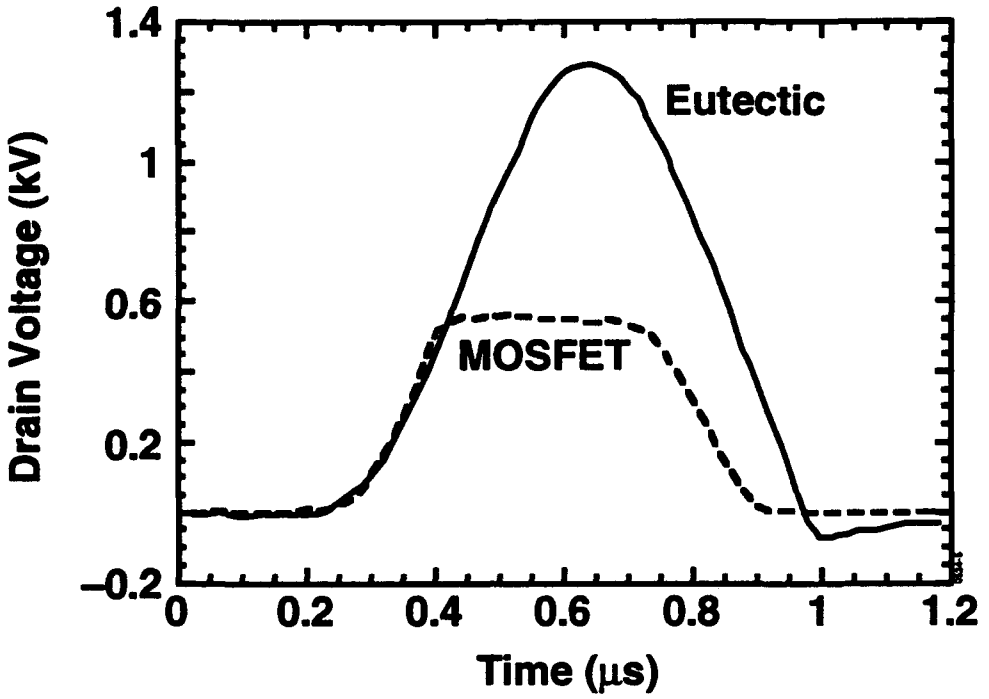


Figure 8. Voltage waveform of a SME device and a conventional MOSFET in a 1200 V test.

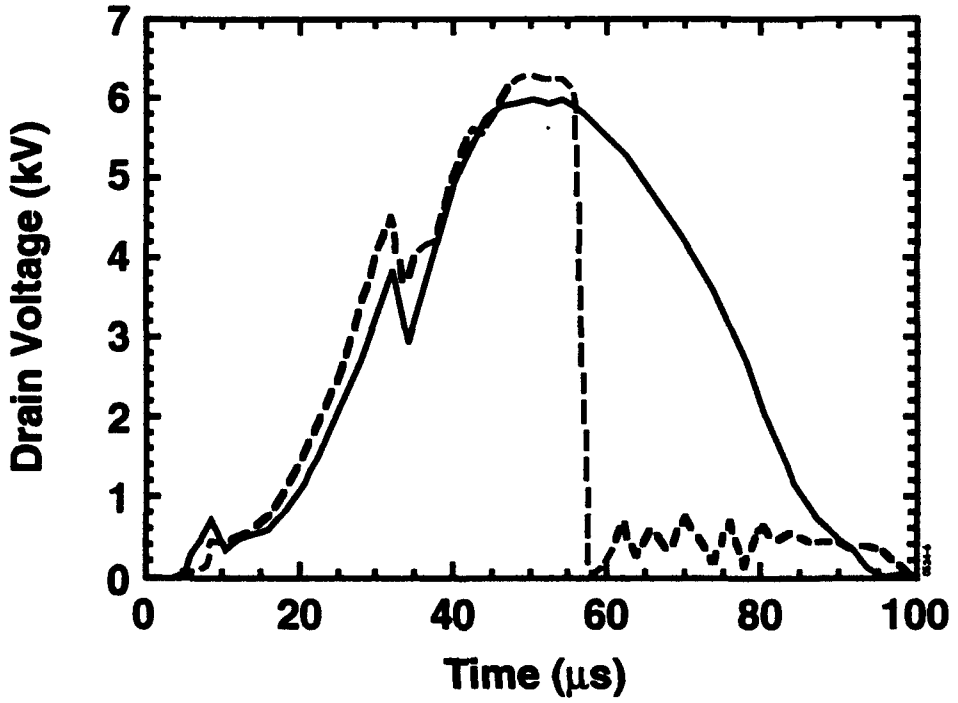


Figure 9. Voltage waveforms of a SME transistor under pulsed test. The solid line shows a full 6 kV waveform supported by the device. Above 6 kV, the device breaks down, as shown by the dashed line.

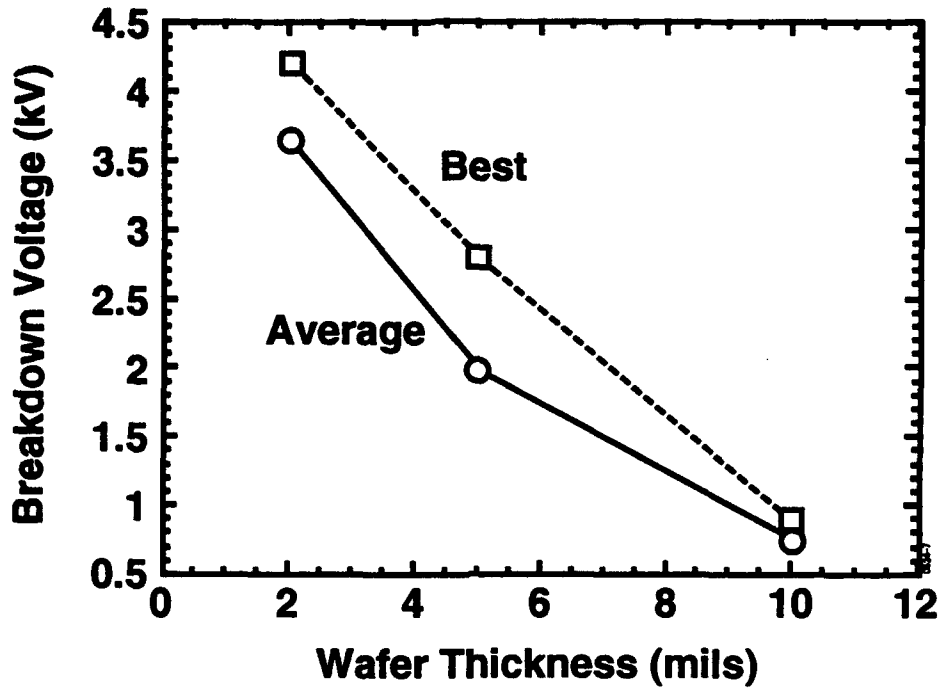


Figure 10. Breakdown voltage vs wafer thickness in pulse test.

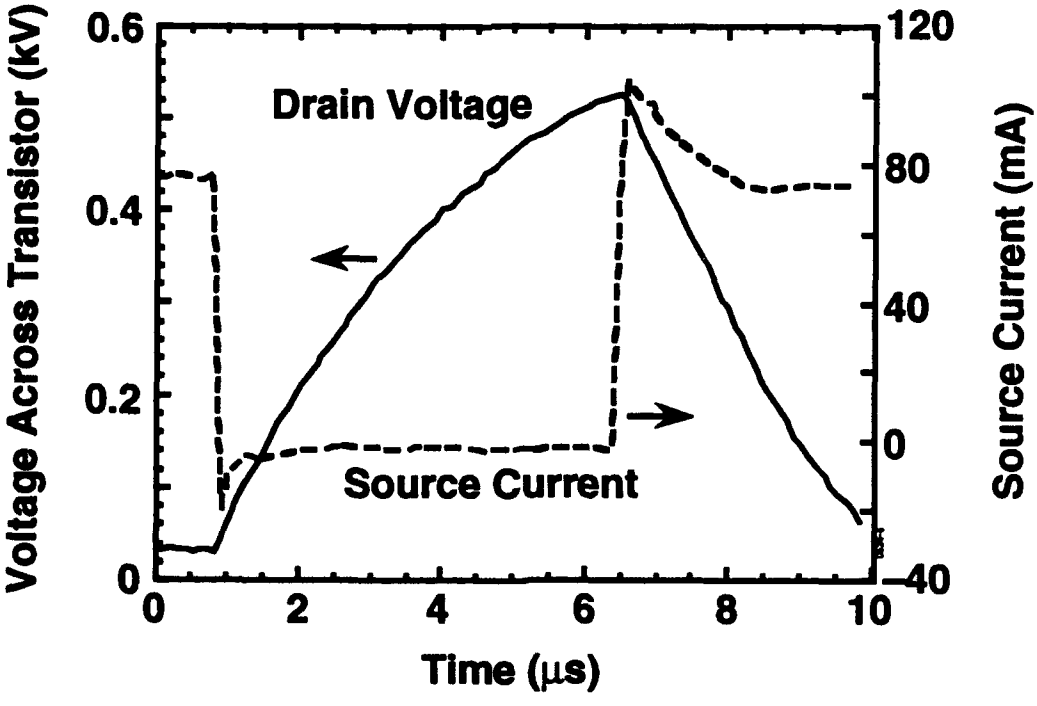


Figure 11. A voltage and current pulse generated with the inductive circuit using a SME transistor.

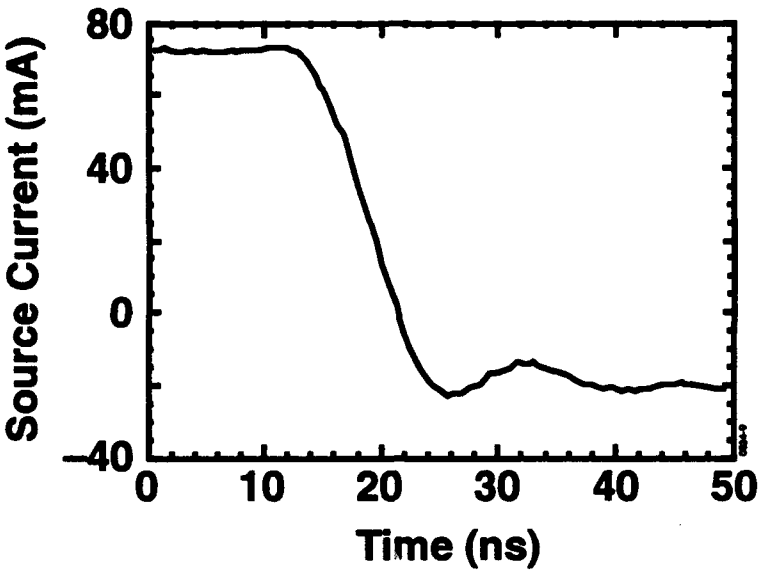


Figure 12. Current waveform at switch opening portion in Figure 11 with the time scale expansion.

2.4. SME Transistor Modeling

Computer simulations were run to develop an understanding of the unusual features of SME transistors, such as a blocking voltage that scales linearly with the gate-to-drain distance, the wafer thickness effects and transients, as well as to predict the properties of an optimized device. Computer simulations were performed using PISCES-IIB software. It models two-dimensional distributions of potential, electric field, and carrier concentrations for arbitrary device geometries and bias conditions.

2.4.1. Model for Breakdown Voltage

PISCES has been used to model the effects of the floating junctions on avalanche breakdown. Since this study has been reported several times in previous publications,[4,5] only a brief description will be given here. PISCES was used to model a 100 μm × 5 μm area with seven 1 μm diameter rods, spaced 8 μm apart with a Si matrix of carrier concentration, 5×10^{14} cm^{-3}. The first rod, closest to the source, is the gate rod; the other 6 rods, which extend toward the drain, are floating. The model indicates that as the drain voltage is increased, the depletion zone extends toward the first floating junction. When V_d is large enough, the depletion zone intersects the first floating rod, and the potential distribution and maximum electric field become clamped. Further potential increases are dropped at the first floating gate until its depletion zone punches through to the next floating junction and its potential distribution is clamped. This process continues until the depletion region expands beyond the last floating gate and may then extend into the drain.

This model explains why the breakdown voltage is associated with the gate-to-drain distance and why avalanching is avoided even when the carrier concentration is high. Since the maximum electric field is clamped by the floating junctions, an average electric field is in place between the gate and drain contacts. In our model, the average field was about 50 kV/cm. In practice, the pulse tests have yielded about 4 kV for a 500 μm gate-to-drain spacing, or about 80 kV/cm, and 6 kV for a 1000 μm spacing, or about 60 kV/cm. DC tests have yielded slightly lower average fields, but as we said before, these results may be limited by thermal affects.

2.4.2. Model for Transients

Transients have also been modeled using PISCES.[6] Figure 13 shows the calculated turn-on response of a model device from a starting drain voltage of V_d = 50, 200, and 300 V. In each case, the model indicates a rapid initial current rise and then a slow tail that increases as the drain voltage is increased. The higher the initial drain voltage, the longer the tail.

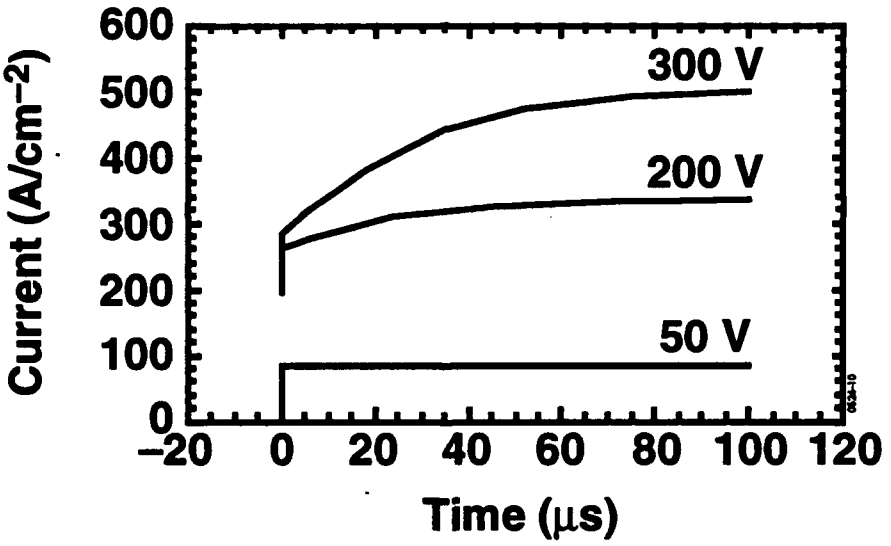


Figure 13. Simulated SME transistor turn-on response for different V_d.

The physical explanation for the long tails may be as follows. During the turn-on process, the first carriers to transit the gate region must pass through the extended depletion zone before they can force current at the drain. The transit time will decrease significantly as the depletion region collapses back toward the gate. The rate of this collapse will be determined by the gate-source and gate-drain capacitances. Thus the turn-on transient may be slower than the turn-off with a time constant that would increase with increasing V_d. Additionally, there is another effect associated with guard rings in conventional devices. The floating junctions exchange charge with the bulk semiconductor as their potential shifts. During the turn-on process, the charging of the floating junctions occurs by minority carrier current or leakage and is relatively slow. During this time, the depletion zones of the floating junctions are larger than when they are neutral, thus constricting

the current channel and producing a long time-constant tail to the drain current during turn-on. The opposite occurs during the turn-off process as the floating junctions discharge by a majority carrier process. Experimental results consistent with this model have been observed.

2.4.3. Model for Optimized Performance

In this case, the model was used to answer the question, What is the ideal microstructure for obtaining high-voltage breakdown, particularly, suppressing breakdown while achieving high on-state conductance? The primary requirement is that the gate depletion zone must reach the first floating junction before avalanche breakdown occurs. This condition defines the carrier concentration, N_d, such that the maximum permissible N_d is the one that yields a depletion zone equal to the spacing between rods, s. Higher N_d would lead to avalanche breakdown before the field limiting capabilities of the floating gates take effect and lower N_d would result in a lower voltage drop per unit distance and a lower conductance.

Analytically determining N_d for various microstructures characterized by s, the spacing between rods, and r, the radius of a rod, and using PISCES to compute I-V characteristics to obtain breakdown voltage and conductance, various microstructures were evaluated.[7] The results are plotted in Figures 14 and 15. Figure 14 shows a figure of merit, $V_L\sigma_V$, plotted as a function of the interrod spacing. V_L is the breakdown voltage per unit length and σ_V is the conductivity, equal to L/R_sA, where L is the source-to-drain distance, A is the cross-sectional area for current transport, and R_s is the series resistance measured from the slope of the linear portion of the computed I-V curves. Figure 14 shows that $V_L\sigma_V$ is approximately inversely proportional to s, for constant s/r. Optimum s/r values lie between 1 and 4.

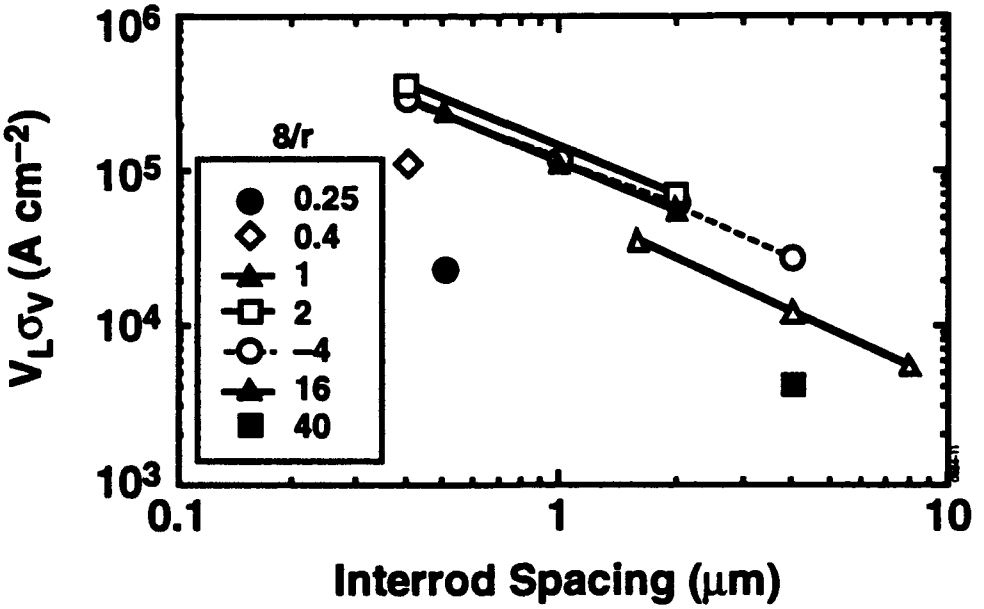


Figure 14. $V_L\sigma_V$ vs interrod spacing, s, for different s/r ratios.

The data in Figure 15 are presented to enable a comparison of these floating gate devices with conventional devices. Basically, it shows that for any given microstructure above a critical breakdown voltage, the SME floating gate device will have superior conductance. For the Si-$TaSi_2$-like microstructure characterized by r = 0.5 μm and s = 8 μm, above about 1000 V, the SME device should be superior to conventional devices. However, with more idealized microstructures, with small s and a s/r ratio between 1 and 4, very significant improvements can be realized even at low breakdown voltages. These results will be compared to experimental results in the following section.

It should be noted that the optimization was performed with the rods distributed in a lattice-like structure with perfectly repeating interrod spacings between each rod. As mentioned in Section 2, the Si-$TaSi_2$ microstructure is such that the rods are distributed within the walls of a cell-like network. The effect this irregularity has on the ideal interrod spacings and radii are unknown.

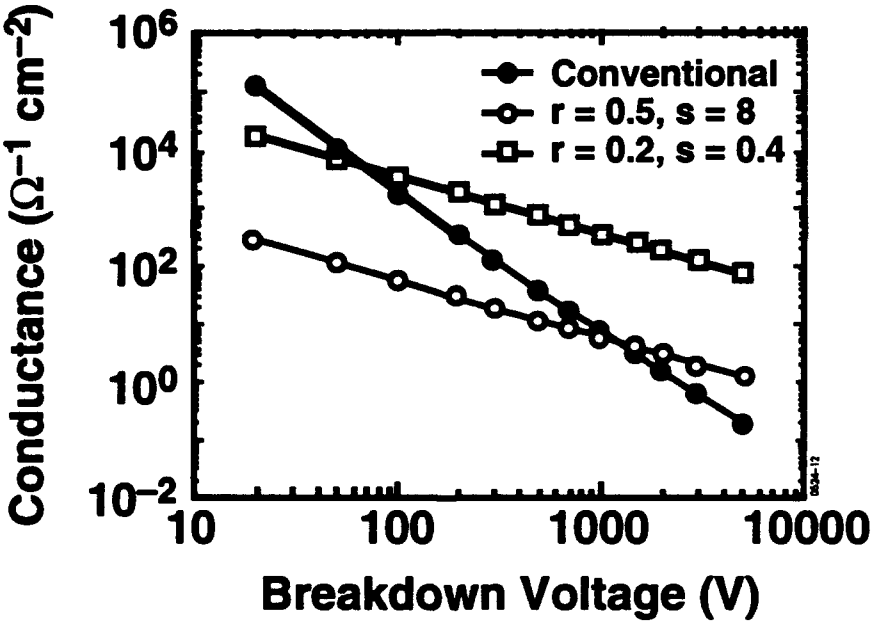


Figure 15. Optimum areal conductance vs breakdown voltage for conventional devices and SME devices with two combinations of junction radii and spacing.

2.5. SME Device Assessment

In this section, a comparison will be made between the pulsed power properties of conventional Si-based devices and that of the SME device. This is done in two ways. First, the graph in Figure 16 shows the specific on-state resistivity, the inverse of the conductivity, shown in Figure 15, as a function of the maximum blocking voltage. The figure makes a comparison of the experimental SME data with the model SME data shown in Figure 14, data for MOSFETs, and theoretical expectations based on the unipolar limit. The plot makes several points.

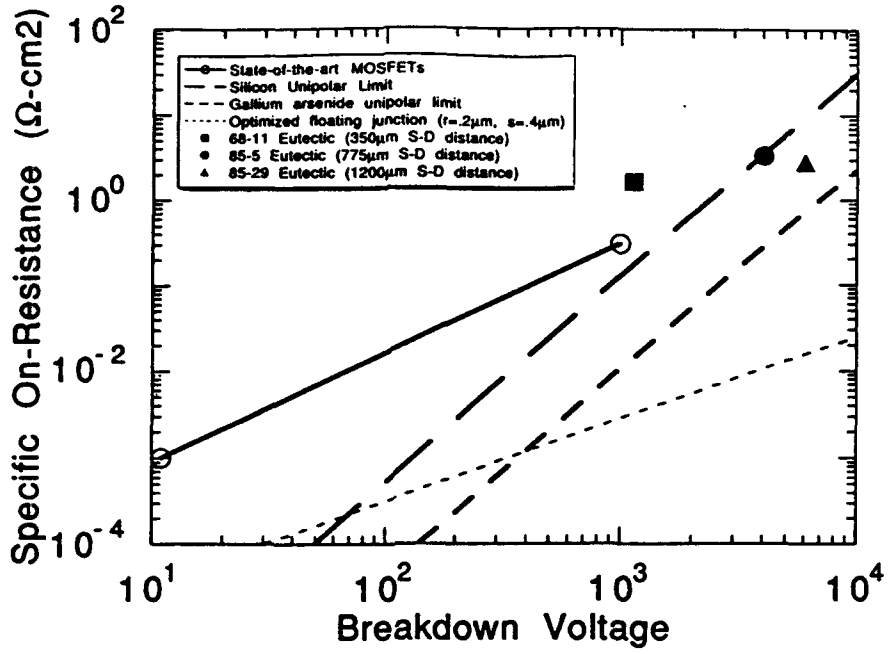


Figure 16. Specific resistance vs breakdown voltage for SME devices and MOSFETs. Theoretical expectations based on the unipolar limit have also been shown.

1. SME devices exceed the blocking voltage capability of MOSFETs and approximately extend along the same line.
2. The experimental SME devices are not quite as good as predicted from the model with Si-$TaSi_2$-like dimensions. The deviation is likely caused by anomalies in microstructure and carrier concentration.

3. The 6kV SME device exceeds the Si unipolar limit.

4. Microstructure refinements in SME devices could result in uniquely high-power devices.

For another comparison, Table 2 compares SME device properties with high-power devices that are being investigated by the pulsed power community.[8,9] Data on five conventional devices and the SME are shown. Comparisons are made for maximum blocking voltage, maximum forward current density, and switching speed. In this comparison, the SME device clearly holds its own. It has the highest blocking voltage (which can be readily increased with a larger gate-to-drain distance) and the best switching time. It lags only in current density.

The data in this table should be cautiously compared. No doubt measurement techniques and criterion are varied from device to device. The table includes several footnotes that try to uncover these differences. Nevertheless, the authors believe that the data in Table 2 indicate sufficient merit for SME devices in high-voltage, high-power switching and that further testing and comparison by an independent testing laboratory or a government laboratory is warranted.

Table 2. Comparison of SME Devices with Other High-Power Devices

	Bipolar	GTO-Thyristor	MOSFET	SIT	MOS-Thyristor	SME
Hold-Off Voltage	500	2500	1000	500	3000	6000
Forward Current Density (A/cm2)	40	100	10	10	325	26
Switching Speed	200 kHz	20 kHz	2 MHz	2 MHz	1 μs Turn-Off	<15 ns Turn-Off

3. MATERIALS AND MICROSTRUCTURAL ISSUES IN SME DEVICES

Just as it is for a conventional transistor, the properties of a SME device are dependent upon the device processing steps, such as oxidation, metallization, etc. But since the processing of an SME device is so simple, it requires only two masks, the truly important materials processing step is crystal growth. For an SME device, that is the step that determines the spacing between junctions and the carrier concentration. Thus the question arises as to how this step can be modified to improve devices. Also important is the SME material itself. Clearly, the Si-$TaSi_2$ system is device worthy, but are there other device worthy eutectic materials? These are some of the types of questions that will be addressed in this section.

3.1. The Effect of Crystal Growth

Directional solidification of the benchmark Si-$TaSi_2$ system by the Czochralski technique results in a crystal with a Si single-crystal matrix and a second phase of $TaSi_2$ rods aproximately aligned along the growth direction. The crystal on average has 1.6×10^6 rods/cm^2, with an average diameter of 1.0 μm. But this is only the average; in actuality, there is a variation of rod size and density.

The variation in rod density in the Si-$TaSi_2$ system has been investigated during this program using image analysis methods within the scanning electron microscope (SEM). Figure 17 shows the results of two scans along the diameter of wafers, in which the SEM image analysis system was used to sequentially measure the number of rods in a given area, in this case 85 μm on a side, as the SEM translation stage moved the sample from one point near the wafer circumference along the diameter until the opposite circumferential point was reached. In Figure 17(a), the counts are for a wafer cut from a crystal grown with the crystal rotated counterclockwise to the crucible at 6 rpm. Figure 17(b) shows the results for a wafer cut from a crystal in which the crystal was not rotated but the crucible was rotated at 12 rpm. It should be understood that during Czochralski growth, rotation of the seed and/or crystal is used to promote needed thermal symmetry. The deviation from the average rod count of about 130 per 7225 μm^2, 1.8×10^6 rods/cm^2, is about 30% less for the latter case than for the former. The result points to the fact that homogeneity can be promoted with enhanced crystal growth techniques.[10]

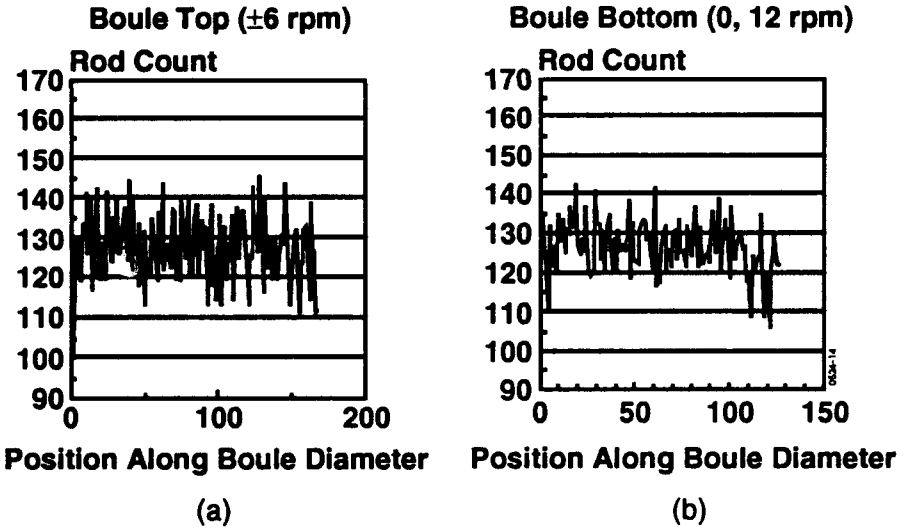


Figure 17. Counts of $TaSi_2$ rods in 85 μm square frame vs position for wafers grown with seed and crucible rotation of (a) (±6) rpm and (b) (0, 12) rpm, respectively.

But, how does this impact the device properties? The data presented in Figure 18 attempt to respond to this question. They show the breakdown voltage as a function of position in a wafer for wafers cut from crystals grown with the ±6 rpm condition and the (0, 12) rpm condition that leads to improved homogeneity. They imply that the ±6 rpm case results in poor homogeneity in properties relative to the (0, 12) rpm case. The crystal grown at ±6 rpm results in devices placed in the center of wafers having low breakdown voltage relative to that for devices placed near the edge. These data are cautiously submitted. They need to be repeated many times before they can be truly accepted. Further, more must be done to assure consistency in wafer size, carrier concentration, device size, and all the many other parameters that could affect this result to ensure the comparison is valid. Nevertheless, the data are included because of their importance. They could indicate that modifications in the crystal growth process could further improve device performance.

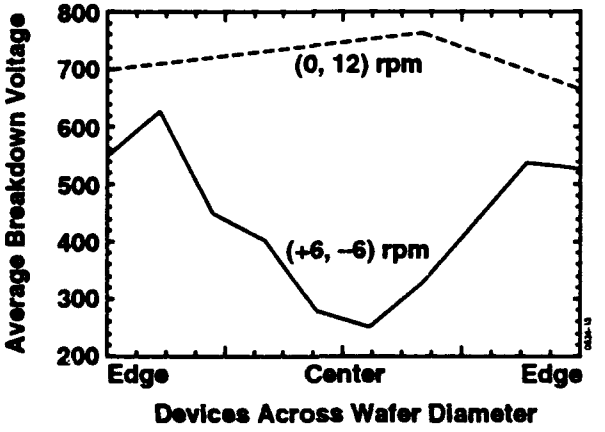


Figure 18. Breakdown voltage as a function of position in a wafer for wafers cut from crystals grown at different conditions.

Previously, rod divergence has been measured on the wafers cut from crystals grown at ±6 rpm to be a maximum of 6°. The divergence of the rods is important because it reduces the effective gate-to-drain distance and reduces the breakdown voltage and forces the use of wafers thinned to 2 mils to achieve high voltage. Thus one interpretation of Figure 18 is that the ±6 rpm condition causes more variability of the rod divergence than the improved (0, 12) rpm condition. If so, a modification of the convective conditions in the melt, as the change in rotation of the seed and crucible causes, can not only affect rod density and rod density variations, but also the rod divergence.

There is additional evidence that convection can affect rod microstructure. The first portion of the eutectic to crystallize just under the Si seed always displays a much finer rod structure than found below the necked portion of the crystal. Also, previous attempts to use a float zone technique for crystal growth instead of the Czochralski technique has also led to a much finer microstructure using the same pull rate of 20 cm/hr.

There is clearly much to learn regarding the effect of crystal growth conditions on the ultimate properties of SME devices. Further studies could lead to quantum improvements in SME device properties, as expected from the modelling studies shown in Figures 14 and 15.

3.2. The Effect of Materials System

Unfortunately, Si-$TaSi_2$ is not the ideal material for SME devices. In addition to a desire for increased rod density and reduced rod divergence, there is also a desire for higher Schottky barrier height. To appraise the potential of other eutectic systems offering better properties for SME devices, this program included a materials effort to evaluate other silicon-silicide eutectics and GaAs-based eutectics. All GaAs-based eutectics are expected to have a higher Schottky barrier height by virtue of the larger bandgap and are therefore of interest. Included in this phase of the program was a subcontract to Dr. Larry Kauffman at ManLabs, Inc., to use computational techniques to determine pseudo-binary systems that would possess eutectic phase diagrams and have minor components of a metallic phase.[11]

The experimental studies of other Si-based eutectics investigated five other silicide containing eutectics, but none was found to offer any advantages to the Si-$TaSi_2$ system. Experimental studies were also performed on GaAs eutectics containing metallic phases of MoAs, CrAs, and GdAs. The MoAs containing SME had an irregular microstructure, while the CrAs system had too large a volume fraction of metallic phase. The GaAs-GdAs eutectic had a very promising microstructure shown in Figure 19. This system is very attractive because of its regular microstructure, finer interrod spacing for a given pull rate, and expected higher Schottky barrier height. This system is unfortunately difficult to grow because the metallic component reacts with the boron oxide encapsulant used to grow GaAs in the liquid encapsulated Czochralski technique.

Kauffman has also indicated that borides should form eutectics with GaAs, and these systems should also be examined. Further efforts on the crystal growth of these systems and the GdAs containing system could prove very fruitful.

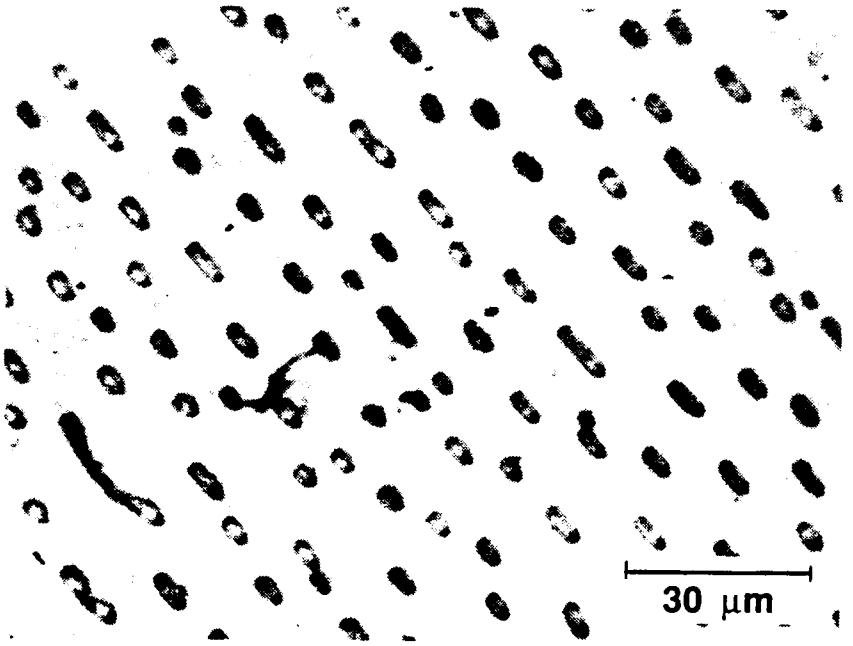


Figure 19.Scanning electron micrograph of the GaAs-GdAs eutectic grown by the Bridgman technique.

One other technique has been investigated during this program to develop a higher barrier height material. This is to convert the Schottky junctions in the Si-$TaSi_2$ to p/n junctions. This would be beneficial because the leakage from the Schottky junctions would be significantly reduced, and the carrier concentration, and therefore the current switching capability, would also likey be increased. Substantial progress toward this goal has been achieved in this program. It has been shown that the $TaSi_2$ rods can be completely removed from a 10 mil thick wafer. With wafers having the metallic component removed, diffusion studies with a Boron source have been conducted. However, a test to determine the success of this diffusion step is difficult to develop and has delayed completion of this task. Nevertheless, this is a very promising approach and, if properly pursued, will likely lead to significantly improved devices.

4. IMPLICATIONS FOR PULSED POWER APPLICATIONS AND SUMMARY

During the course of this program, many scientific and engineering milestones have been completed.

From a materials science perspective, it has been shown for the first time that a two-phase equilibrium structure can perform as the basis for electronic devices. Prior to this, only single-phase or metastable structures such as superlattices have been considered suitable for electronic devices. The accomplishments of this program will hopefully set the precedent for a wide range of new materials for electronic applications.

In device physics, it has been shown for the first time that floating junctions can extend the breakdown voltage of depletion mode devices beyond the avalanche breakdown limit. This is a major innovation in semiconductor device physics that will hopefully lead to a new generation of high-voltage, high-current devices.

In pulsed power, it has been shown that semiconductor-metal eutectic devices offer the three ingredients of high voltage, high current, and rapid opening times. Although the current state-of-the-art in SME does not excel in each of the three categories relative to conventional devices, they clearly have a place in the competetive, well-developed field of high-power devices. This is particularly impressive in the light of the small program.

Nevertheless, commercialization of SME devices and realization of their full potential will take additional development. The following research and development program is recommended to complete the development of these novel devices.

1. A high-voltage, high-current SME prototype device should be demonstrated and tested using methods already employed to evaluate conventional devices such as the SIT or the MOS-controlled thyristor. Initially, we proposed a 100 A, 10 kV test. A similar goal should be pursued and tied to a specific application. The program should include growth of large diameter crystal, fabrication of large area devices, packaging of devices, and testing of devices. The actual opening time for the switch should be measured. It could be significantly less than the upper limit of 15 ns demonstrated in this program.

2. A next-generation material should also be developed for a substantial leap in the current handling capability of an SME device. An enhanced material that would exceed the switching capability of MOS-controlled thyristors and other advanced conventional devices in all three categories of high voltage, high current, and switching time would need to have a higher barrier height, a finer interrod spacing, and an

increased carrier concentration in the semiconductor matrix. Three possibilities for achieving this have already been discussed: 1) a growth technique that leads to finer interrod spacing in the Si-$TaSi_2$ system, 2) GaAs based eutectics, and 3) Si-$TaSi_2$ with the Schottky junctions converted to p-n junctions. A long-term research program dedicated to achieving an order of magnitude improvement in the capabilites of solid-state switches should include a program that pursues all three approaches. All three have a good probability for success.

In summary, SME devices have great potential for pulsed power switching as well as other applications, and the technology is very close to being ready for commercialization. Therefore, it is unfortunate that due to extraneous circumstances, GTE has discontinued its research and development program in this area. It is our recommendation that some method of seeing the work through to a successful conclusion be sought and implemented.

5. REFERENCES

1. B.M. Ditchek, T.R. Middleton, P.G. Rossoni, and B.G. Yacobi, Appl. Phys. Lett. 52, 1147 (1988).

2. Q.V. Nguyen, P.G. Rossoni, M. Levinson, and B.M. Ditchek, Proceedings of 20th International Symposium on Power Modulator, Myrtle Beach, SC (1992).

3. S.M. Sze, Physics of Semiconductor Devices, Wiley, New York (1969).

4. M. Levinson, P.G. Rossoni, W.W. Byszewski, and B.M. Ditchek, Proceedings of 19th Power Modulator Symposium, San Diego, CA (1990).

5. M. Levinson, P.G. Rossoni, F. Rock, and B.M. Ditchek, Electron. Lett. 26, 777 (1990).

6. M. Levinson, Q.V. Nguyen, P.G. Rossoni, and B.M. Ditchek, ONR Review, CA (1991).

7. P.G. Rossoni, M. Levinson, and B.M. Ditchek, *J. Appl. Phys. 70*, 2861 (1991).

8. B.J. Baliga, IEEE Spectrum, p. 42 (March 1981).

9. C. Braun, Proceedings of the 4th SDIO/ONR Pulse Power Meeting, p. 88 (1991).

10. Q.V. Nguyen, T.R. Middleton, J. Hefter, and B.M. Ditchek, AACG Crystal Growth Conference, Fallen Leaf Lake, CA (1991).

11. L. Kauffman and B.M. Ditchek, *J. Less Common Metals 168*, 115 (1991).

Appendix A
Final Report (April 1990)

Research &
Development

Semiconductor-Metal Eutectic Composites for High Power Switching

Final Report for Contract N0014-86-C-0595

B.M. Ditchek
M. Levinson

Submitted to
Dr. Gabriel Roy
Office of Naval Research
800 North Quincy Street
Arlington, VA 22217-5000

April 1990

GTE Laboratories Incorporated
40 Sylvan Road
Waltham, MA 02254

GTE

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

1. INTRODUCTION

Semiconductor-metal eutectic (SME) composites, with a microstructure composed of an array of metallic rods distributed throughout a semiconductor matrix and formed by the directional solidification of a eutectic mixture, represent a new class of electronic materials with the potential to enhance and expand the capabilities of high-power, solid-state switching technology of most interest to the pulsed power community as well as other areas including photodetection. The objective of this three-year program has been to establish the materials science and device principles necessary to assess the feasibility of high power switching devices based on SME materials.

In this report, the most important results of the SME studies over the course of this contract will be reviewed. Important contributions have been made in the growth of these materials, including growth factors that affect the rod structure and in the identification of new GaAs-based SME systems. The development of high power transistors in the Si-$TaSi_2$ 'benchmark' system will be discussed and it will be shown that the rapid progress that has led to 1 kV blocking voltage devices can probably be continued to yield true high current, high voltage opening switches. The goals of materials development and bringing the device development to the point of assessing pulsed power capabilites have been met.

This program has followed a radical approach to the development of advanced electronic materials and, in particular, high power opening switches. SME materials differ from the single-phase materials that have been used to create electronic devices in the past in that they contain two phases in equilibrium with each other. Long held tenets of semiconductor device physics required that the semiconductor be made free of any second phase. It was believed that metallic inclusions would lead to high leakage currents and low-voltage breakdown. The development and demonstration of SME composite materials for high-voltage operation in this program has given credibililty to this radical approach and has reduced the credibility of the old semiconductor tenets thereby opening up device design to freer thought, and, hopefully, more innovation.

2. EUTECTIC COMPOSITE MATERIALS

2.1 Si-Based Eutectic Systems

The directional solidification of the Si-$TaSi_2$ eutectic composite yields a material with a rod-like distribution of the $TaSi_2$ phase in a Si matrix. The eutectic composition corresponds to about 2 v/o $TaSi_2$. The scale of the eutectic microstructure is determined by the growth rate, such that $\lambda^2 v$ is a constant, where λ is the average interrod spacing and v is the growth rate. The constant has been determined in these studies to be 1.25×10^{-5} cm^3/h. All devices have been fabricated in material grown at 20 cm/h and contained an average interrod spacing of about 8 μm.

The growth technique employed is called Czochralski crystal pulling and is analogous to the most common technique for growing large Si crystals for the electronics industry. After the melting of a charge of the eutectic composition a Si seed is lowered onto the melt surface, given time to thermally equilibrate, and then pulled up at the fixed rate of 20 cm/h. The composite boule solidifies as the seed is pulled. This process of directional solidification yields the eutectic rod-like microstructure with the rods oriented along the growth direction.

Initially, the boules grown had polycrystalline Si matrices. Fabrication of devices on these substrates always led to excessive leakage and nearly ohmic, nonrectifying behavior. It was found, however, that composites with a single-crystal Si matrix could be obtained using certain techniques. Growth of a single-crystal matrix eutectic depends primarily on using the exact eutectic composition and minimizing certain impurities. Due to loss of Si as SiO and the meltback of a fraction of the seed, maintaining the eutectic composition can be difficult. Nevertheless, proper balancing of the two effects can be achieved and numerous boules with single crystal matrices have been grown. Originally, all boules were grown with a (111) single crystal matrix of Si and all devices were fabricated in (111) material. Studies of the effect of orientation on microstructure were conducted, however, leading to composite boules with (110) and (100) orientations as well. (The results of this study are discussed later.)

For this program, Si-$TaSi_2$ boules were typically grown with a diameter of about 2 cm and

weighed between 50 and 100 gms. A photograph of a typical single-crystal matrix (111) boule is shown in Fig. 1. The eutectic microstructure in a typical transverse section is shown in Fig. 2. The figure shows that the rods in the eutectic are neither arranged in a regular lattice-like array nor distributed in a strictly random pattern. Examinations of many such sections has revealed a kind of cellular structure. The interrod spacing in the cell walls is less than the average interrod spacing. For the case of $\lambda = 8$ μm, our estimates indicate that the spacing within the cell walls averages only about 4.5 μm. The interior of the cell walls exhibits a very low rod density and covers an area with a diameter several times the average interrod spacing. Studies of the transport properties of the composites have indicated that the cellular nature of the rod distribution tends to limit the conductivity at a much higher carrier concentration than it would for a regular 8 μm interrod spacing distribution and, therefore, the irregularity of the structure, contrary to intuition, offers advantages to the device performance.

Examination of longitudinal sections of the boule also indicates that the rods are not all perfectly aligned and that some divergence of the rods relative to the wafer normal may exist. Using the EBIC technique discussed in Section 3, the maximum divergence of the rods has been measured to be 6 ^{o} relative to the wafer normal. Rod misalignment has been shown to be a microstructural factor adversely affecting switch performance (Section 5.3).

Since the $TaSi_2$/Si Schottky barrier is higher on n-type Si than on p-type, the Si used in the charge was always lightly doped with the n-type dopant, phosphorous. Carrier concentrations of the composite boules, 1 to 3 x 10^{15} cm^{-3}, were several times larger than the carrier concentrations of the Si charge, indicating that the Ta was probably contaminated with an n-type doping element, such as P. Segregation of the dopant along the axis of the boule indicated complete mixing in the melt and a segregation coefficient that was similar to that for n-type dopants in Si, about 0.3.

Studies of the Si composite boules took two approaches. First, to develop an understanding of the growth factors affecting microstructure, particularly, the rod density, rod misalignment and the matrix orientation. Second, to determine if any other Si-based eutectics offered a microstructure more favorable to device development.

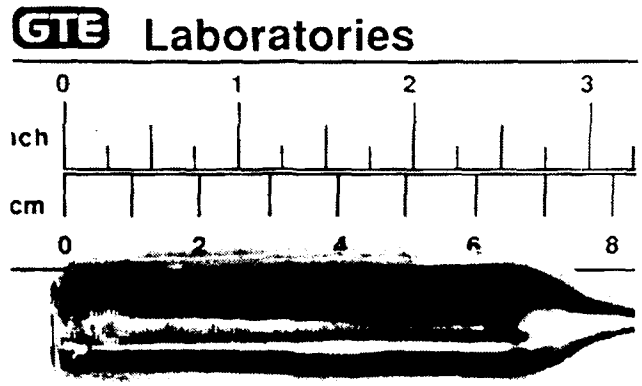


Figure 1. Photograph of a typical single-crystal (111) matrix Si-$TaSi_2$ eutectic composite.

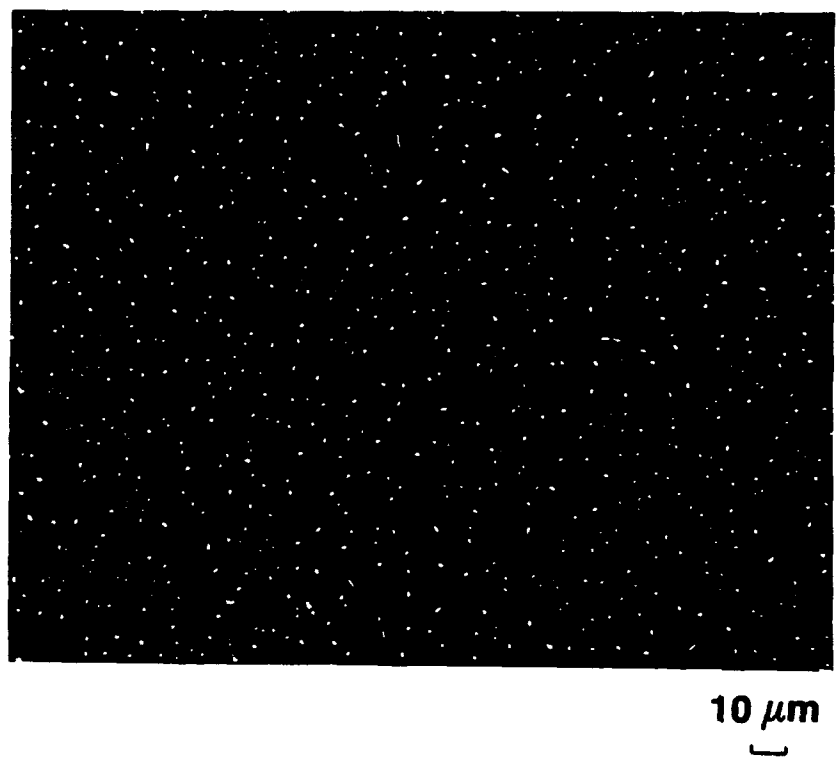


Figure 2. A transverse section of a Si-$TaSi_2$ eutectic composite. Note the cellular arrangement of the $TaSi_2$ rods.

The classic theory of eutectic solidification implies little or no affect of melt convection on the interrod spacing. Laminar flow leads to a boundary layer that is much larger than the interrod spacing, which according to the theory of eutectic solidification is comparable in extent to the maximum compositional variations in the melt extending outward from the melt-solid interface. Nevertheless, these materials are grown under the turbulent melt conditions of Czochralski growth, and temperature fluctuations and growth rate variations are expected. Analysis of these effects proceeded using an image analysis technique performed in a JEOL JXA-840II scanning electron microscope (SEM). Data image acquisition and processing was done using a Tracor Northern 5500 system. The system was used primarily to count the number of rods in a given area, typically 90 μm x 90 μm. Using this technique diameter scans and areal scans were made to correlate average rod density and rod density variations across a wafer with growth parameters.

The microstructural analysis indicated two effects important for understanding and designing devices with this material. Firstly, the wafers contain a variation in rod density that maps out a spiral. It originates near the wafer center and spirals to the wafers edge. A quarter section of a wafer that has been analyzed is shown in Fig. 3. The number of rods within a 80 μm^2 area vary from a high of 100 to a low of 60, all within the same wafer. Indications are that these variations depend on the rotation rate of both the seed and crucible. Secondly, the actual rod density averaged over the entire wafer, decreases slightly as the orientation of the Si matrix goes from (111) to (100) or (110) and as the rotation rates of the seed and crucible are increased. In addition, rapid rotation rates, about 30 rpm, was noted to yield large excursions in composition, such that parts of the wafer contained single phase Si regions without the $TaSi_2$ rods.

Studies of GaAs-based eutectics, to be discussed in detail in the following section, indicate that the spiral distribution of interrod spacings changes along the boule axis. Thus, the rod density at one point, (x,y,0) at the surface of a wafer is different from the rod density at another point a distance *l* below the surface point (x,y,*l*). Divergence or misalignment of the rods is required to explain this. This implies that the divergence of the rods which reduces the blocking voltage of a device and places restrictions on the maximum usable thickness of a wafer and, therefore, the current handling ability of the device, is partly caused by the effect that leads to the spiral pattern.

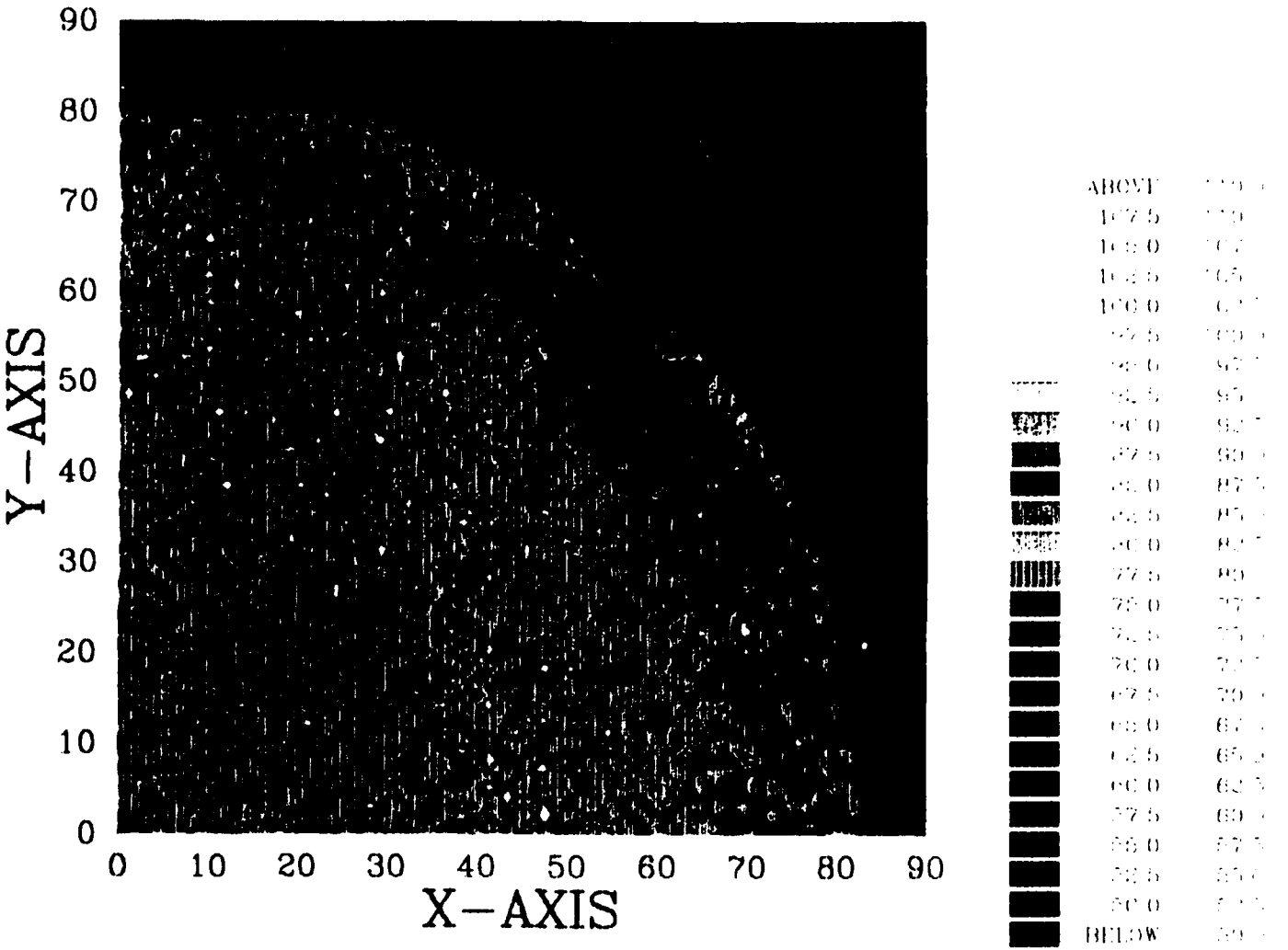


Figure 3. A color coded contour plot of the rod density of a quarter section of a wafer. The analysis area for each pixel in this case is 5000 μm^2. The numbers on the right refer to the number of rods counted in a pixel of a given color. The figure demonstrates the swirl-like distribution of rods in a wafer.

The swirl pattern is almost certainly caused by the temperature fluctuations during growth in a Czochralski crystal growth system. The temperature fluctuations yield growth rate variations and this, through the $\lambda^2 v$ = a contant rule, causes a variation in the interrod spacing. Improved uniformity would probably be expected in Bridgman growth but this technique cannot be applied to growth of the high temperature Si-based systems. It is known that a magnetic field can be used to minimize temperature fluctuations but even the thermal nonuniformities in the system can lead to growth rate variations due to seed rotation. Improved uniformity may come from maximization of thermal symmetry in the growth system and optimized rotation rates.

Many other Si-silicide eutectics exist in addition to the Si-$TaSi_2$ system. The systems listed in Table I were grown and their microstructure characterized. Micrographs for each system, showing the variations in the volume fraction of the silicide phase are shown in Fig. 4. Table I lists the $\lambda^2 v$ constant, and the rod diameter, d, for each system at a growth rate of 10 cm/h. An examination of the values of $\lambda^2 v$ for each system shows that the constant decreases as the volume fraction of the silicide phase increases, such that, the $d^2 v$ value is nearly constant for all the Si-silicide systems. This leads to a similarity of these systems that does not point to an advantage of one eutectic system over the Si-$TaSi_2$.

2.2 GaAs-Based Eutectics

The purpose of studying GaAs-based eutectics was to identify and develop new eutectic composites with enhanced properties. The most desirable property expected was that of a higher Schottky barrier height. Barrier heights in this system are expected to be at least 0.7 eV, or better than half the bandgap of GaAs. Thus, these systems should enable high power devices with reduced leakage currents and more temperature stability.

GaAs-based eutectics were essentially virgin territory. Only one reference was known to us: a paper by Reiss and Renner[1] on three GaAs rod-like eutectics, GaAs-CrAs, -MoAs and VAs. The approach we took was to re-examine these three systems and use phase diagram calculations followed by experimental work to evaluate others. Microstructure of the GaAs-CrAs and the GaAs-MoAs are shown in Fig. 5. Both systems were grown by the high pressure, liquid encapsulated Czochralski (LEC) technique. Encapsulation and the growth and synthesis

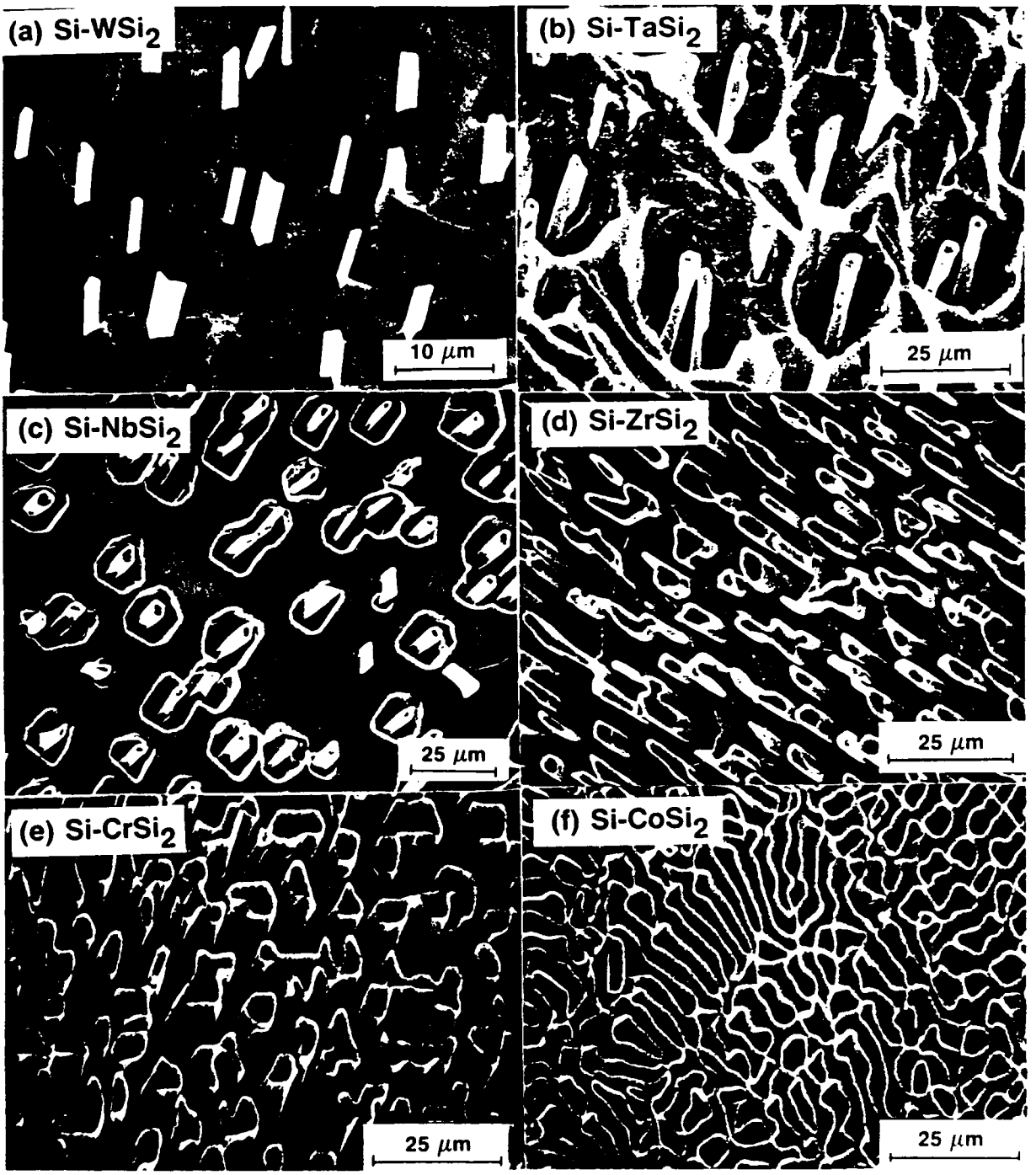


Figure 4. Scanning electron micrographs of Si-based eutectics. The Si phase has been etched back to reveal the silicide phase. All composites were grown at 2 cm h except for the Si-WSi_2 eutectic, which was pulled at 10 cm h.

TABLE I. Microstructural parameters for Si-silicide eutectics.

Eutectic	f(%)	$\lambda^2 v$(10^{-8}cm^3/h)	$d^2 v$(10^{-8}cm^3/h)	d(10^{-4}cm) at v = 10 cm/h
Si-WSi_2	0.9	1150	20	1.4
Si-$TaSi_2$	2.2	1250	13	1.1
Si-$NbSi_2$	2.8	1050	30	1.7
Si-$ZrSi_2$	19	75	17	1.3
Si-$CrSi_2$	29	90	30	1.7
Si-$CoSi_2$	55	90	18	1.3

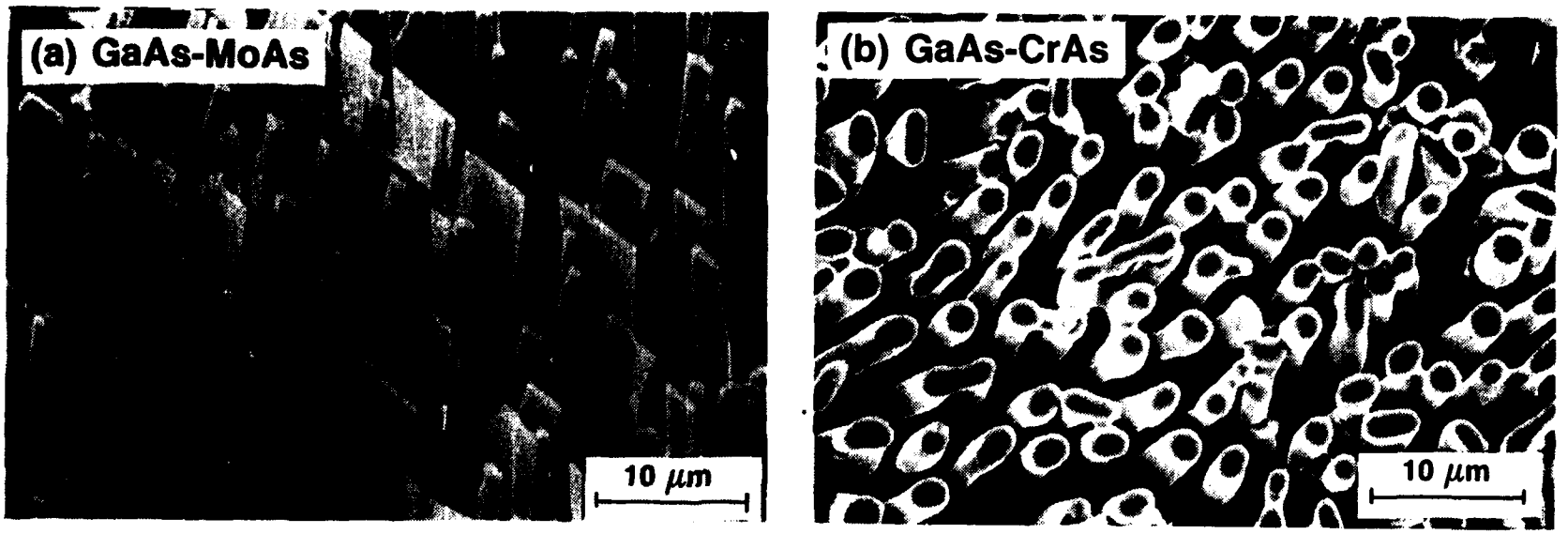


Figure 5. Scanning electron micrographs of two GaAs-based eutectics. The microstructure of the GaAs-MoAs eutectic is shown in (a) and the microstructure of the GaAs-CrAs eutectic is shown in (b). Both were pulled at 6 cm/h.

under high pressure are techniques needed to suppress loss of the volatile As component. The GaAs-CrAs system is a rod-like eutectic with a volume fraction of metallic phase that is too large for device applications. Device applications are also precluded by the interconnectivity of the CrAs rods. The GaAs-MoAs system tends to yield a very irregular distribution of the MoAs phase. The As-Mo phase diagram has several different arsenides in it and these probably also appear in the composite as As is lost. The GaAs-VAs system was not investigated because a V source of reasonable purity was not available.

Phase diagram calculations intended to help identify additional GaAs-based eutectics were conducted by Dr. Larry Kaufman of ManLabs Inc. using CALPHAD techniques. This work was performed under subcontract to the main program. The systems listed in Table II have been identified as having eutectic compositions using this technique. Calculated eutectic compositions and temperatures are listed for each system. The GaAs-CrAs and GaAs-MoAs systems, with known eutectic compositions, were used as controls and the computed values compared very favorably with experimental values from our work and that of Reiss and Renner.

Of the other systems present only the GaAs-GdAs system was grown. This system and others containing rare earth arsenides are difficult to grow using the LEC technique because the rare earth reacts with the encapsulant forming a rare earth oxide that is impenetratable by the seed. Using Bridgman techniques the GaAs-GdAs system was grown. The microstructure of a cross-section is shown in Fig. 6. The system does have a volume fraction of the metallic phase that is appropriate for device development. Use of this system will require development of better techniques for growing it that will provide better composition control than the currently used Bridgman technique offers and enables routine growth with a single crystal matrix. Experiments have been performed substituting $BaCl_2$ for B_2O_3 encapsulant. But even though the chloride doesn't react with rare earths, it does melt at a higher temperature and it is not as simple to work with as the oxide. Nevertheless, this system is very promising and with sufficient effort it should be possible to fabricate device quality material. As shown in Fig. 6, the GaAs-GdAs also offers the advantage of a slightly reduced interrod spacing relative to the Si-$TaSi_2$ system.

Growth studies of the GaAs-borides have not been carried out to the point of verifying the

TABLE II. Eutectic phase diagrams calculated using CALPHAD techniques.

System	Eut. Comp.	Eut. Temp.(K)
GaAs - CrAs	0.208	1459
- MoAs	0.040	1506
- NdAs	0.031	1507
- GdAs	0.026	1510
- TiB_2	0.156	1444
- ZrB_2	0.039	1500
- HfB_2	0.003	1503

GaAs-GdAs EUTECTIC

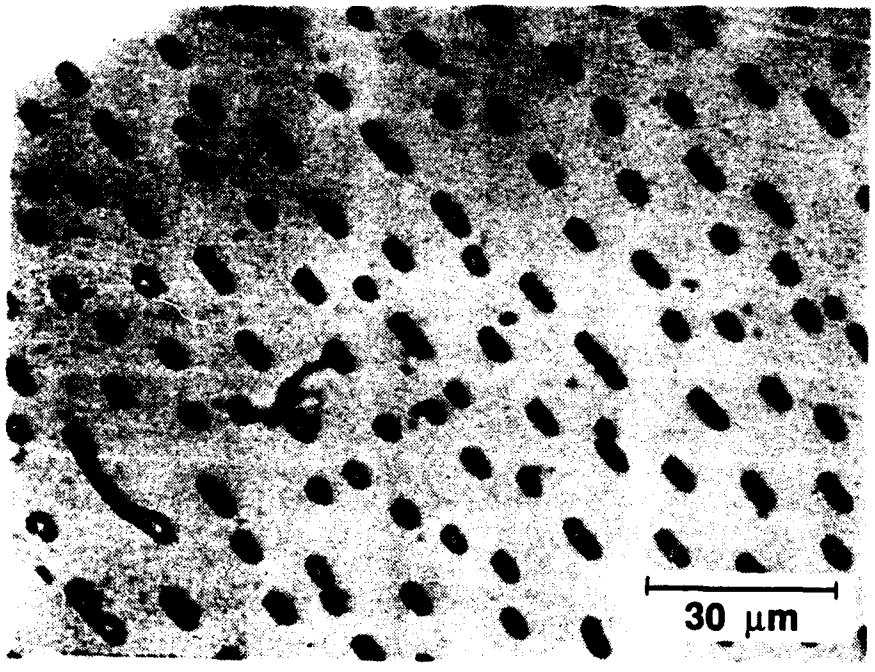


Figure 6. Scanning electron micrograph of the GaAs-GdAs eutectic grown by the Bridgman technique.

ManLabs prediction of a eutectic in this system. If these predictions are correct, it should offer a low volume fraction rod-like structure. Presumably the boron, which is isoelectronic with Ga, will not affect the conductivity of the GaAs lattice.

The GaAs-CrAs system, simple to grow and with a microstructure that is easy to analyze, has been used for studies of the effect of convection on the rod structure. Reference has been made to these studies in the previous section on Si-based systems. Composites were grown in a system with a transverse magnetic field. The magnet is used in crystal growth studies to suppress turbulent convection and reduce temperature fluctuations in Czochralski growth.

Composite boules grown in a magnetic field were sliced into wafers and etched. The etched wafers reveal a sharp spiral pattern which from a micrograph of the spiral line, clearly represents a region in the wafer with a large interrod spacing and rod diameter. Thus, the spiral pattern, except for the additional sharpness caused by the application of the magnetic field, is similar to that observed in the Si-$TaSi_2$ system. Micrographs are shown in Fig. 7. In Fig. 7(a) a longitudinal cut shows the rods along their axis and the periodic change that results. The transverse wafer contains the spiral and Fig. 7(b) shows a micrograph of this area indicating the change in rod density observed along the spiral line. In this case, the interrod spacing variations are sufficiently large as to be readily observed without image analysis techniques.

The etched wafer is shown in Fig. 8 in a sequence that shows how the spiral changes along the boule axis. The micrograph in part (a) was taken, the wafer was polished and re-etched after removal of 25 μm, or one quarter of the banding period apparent from Fig. 7(a). This micrograph from this position is shown in Fig. 8(b). The distribution of the spiral is slightly different in (b) vs (a). This was continued until 100 μm was removed. After 100 μm removal, the length of the banding period, the original spiral distribution is re-established. This technique allows construction of a three dimensional distribution of the rod density variations and clearly leads to the conclusion that divergence of the rods is required to accomodate the density changes along the axial direction.

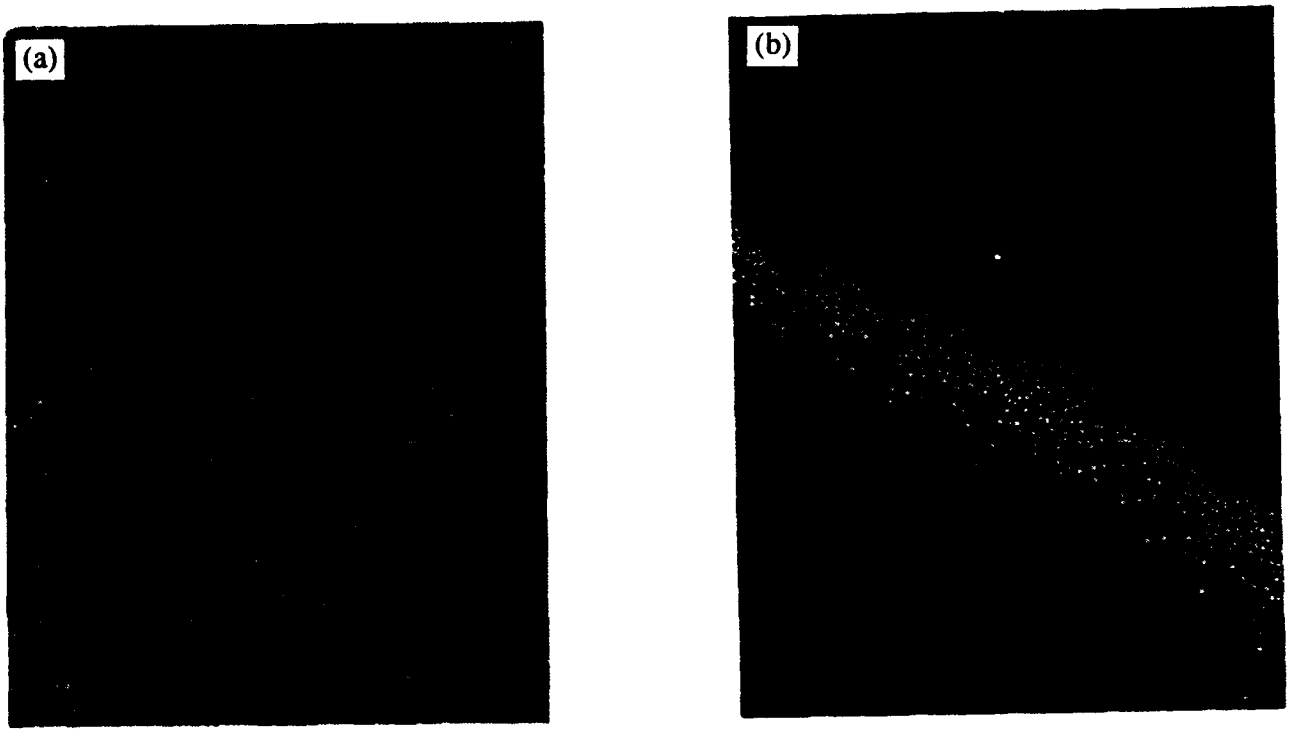


Figure 7. Optical micrographs of (a) axial and (b) transverse sections of the GaAs-CrAs eutectic grown in a magnetic field (2.5 kG). The axial slice shows periodic rotational bands, with a spacing of 100 μm. The transverse slice, intersecting these bands, shows a spiral pattern. (b) shows a micrograph of one section of this spiral indicating that the contrast is due to a change in interrod spacing. For (b) the magnification is 185 x.

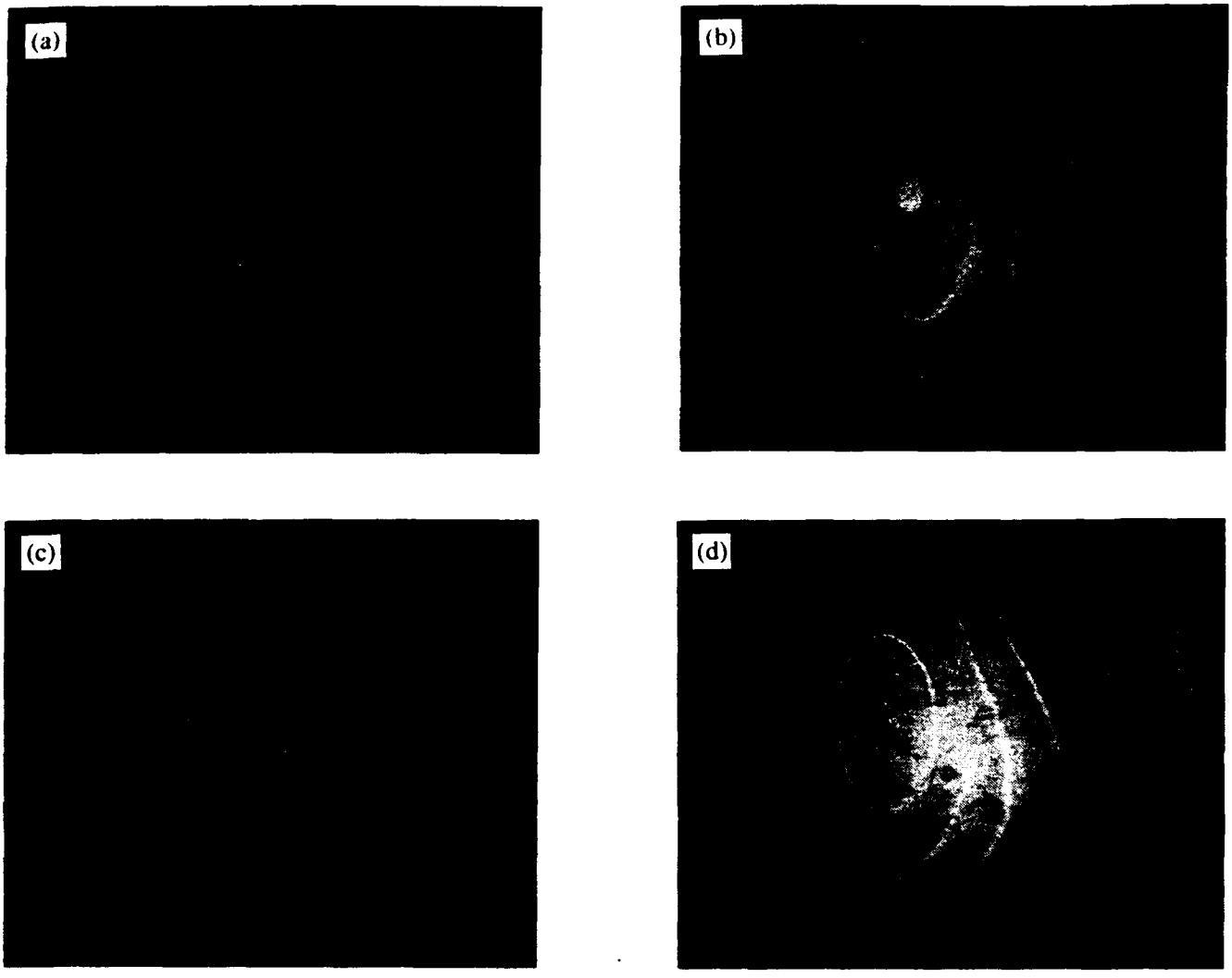


Figure 8. Optical photographs of an etched GaAs-CrAs wafer showing the spiral pattern. From (a) through (d) each photograph is separated from the next by removal of 25 μm from the surface. Thus (d) indicates the spiral pattern 100 μm below the surface of the wafer with the spiral pattern shown in (a). In (a) and (d) the spiral pattern is equivalent because 100 μm corresponds to the band separation as shown in Fig. 7. Changes in the spiral pattern with depth are a record of the temperature fluctuations and growth rate changes that occured during the crystal growth.

3. EUTECTIC COMPOSITE DIODES

Diodes have been fabricated and characterized in the Si-$TaSi_2$ system. Diodes have led to determination of the Schottky barrier height, the actual carrier concentration of the Si matrix and evidence that the rods are continuous through the thickness of a wafer. Techniques developed for the fabrication of the two contacts needed to generates diodes or any electronic devices, including transistors, will be discussed first. This will be followed by a brief summary of diode characterization techniques employed.

3.1 Diode Contacts

Fabrication of electronic Si-$TaSi_2$ eutectic devices requires the formation of ohmic and Schottky contacts. The necessary Schottky contacts are grown into the material, of course, but contact to the desired group of rods must be made without creating additional current leakage paths. The best approach would be to contact the rods without contacting the Si. This is very difficult to reduce to practice so that other techniques had to be sought. The best alternative was to contact the rods with a film that also formed a Schottky barrier with the Si surface in between the rods. It was reasoned that as long as the Schottky barrier for the metallic film with the Si exceeded the Schottky barrier of the *in situ* junctions and the area of the surface Si contact was small relative to the $TaSi_2$/Si junction area, the effect of this junction on diode capacitance or currents would be small.

The rectifying contact that proved the best of the several types examined was a $CoSi_2$ film. For this contact, the wafer is annealed in wet oxygen to grow a 0.3 μm thick oxide. Vias are opened in the oxide using standard lithographic practices where the rectifying contacts are desired. Following this 800 A of Co is evaporated by e-beam methods onto the substrate $CoSi_2$ is formed in the openings by a rapid thermal anneal at 800 C for 12 s. Unreacted Co on the oxide is removed using a nitric acid etch. This self-aligned silicidation process is schematically shown in Fig. 9.

Ohmic contacts can be fabricated by any technique that will provide a metal/n^+ surface layer. Two techniques have been used. In the first technique, Au-Sb films are evaporated onto the ohmic contact openings in the oxide and then subject to a 400 C anneal for 1 h. At

this temperature, above the Au-Si eutectic, the Au reacts with the substrate and the ohmic contact is formed via the Sb-doped n^+ layer at the junction. Since the eutectic film is irregular and discontinuous in most cases, it is necessary to evaporate an additional metallic layer, usually, another Au film on top of the reacted film. The second approach yields a more robust, uniform contact. In this technique a $CoSi_2$ film is formed as it was for the Schottky contact. To form the n^+ contact at the silicide/Si junction, As is implanted at 100 kV with a flux of 10^{14} cm^{-2}. Movement of the As from the surface of the silicide film to the junction was performed with another rapid thermal anneal at 800 C to 900 C for 10 s. In exacting applications, this ohmic contact was preferred.

3.2 Diode Characteriztion

Diodes have been characterized using a variety of techniques including, current-voltage (I-V), capacitance-voltage (C-V), deep level transient spectroscopy (DLTS) and electron-beam-induced-current techniques (EBIC). A number of important conclusions resulted from these studies that are relevant to device development for high power applications. Some of these are discussed briefly in the following.

- The I-V characteristics of the diodes were nearly ideal. The forward characteristics indicated an ideality factor of 1.1 and reverse bias resulted in leakage currents that were nearly constant below 10 V and comparable to the expected value based on the Schottky barrier height. The Schottky barrier height was determined to be 0.62 eV.
- The C-V characteristics indicated that the junctions acted as coaxial capacitors rather than parallel plate capacitors as expected from the rod-like shape of the junctions. At high reverse bias voltages, the capacitance was lower than expected probably because of overlap of the depletion zones of neighboring junctions.
- DLTS indicated good quality Si surrounded the junctions. The concentration of electrically active Ta-induced levels was found to be inconsequentially small. Other traps, probably related to dislocation-induced levels were found to be inhomogenously distributed.
- EBIC techniques gave the first graphic images of the depletion zones surrounding the rods. It showed that expansion or contraction of the depletion zone could be affected by a reverse or forward bias, repectively. Furthermore, by relating the actual rate of increase of the depletion zone with reverse bias voltage to that expected for a cylindrical junction based on Poisson's equation, EBIC was used as a method for accurately determining the carrier

concentration of the Si matrix. SEM and EBIC micrographs of several $TaSi_2$ rods in a Si matrix at zero bias and with a 5 V reverse bias voltage are shown in Fig. 10.

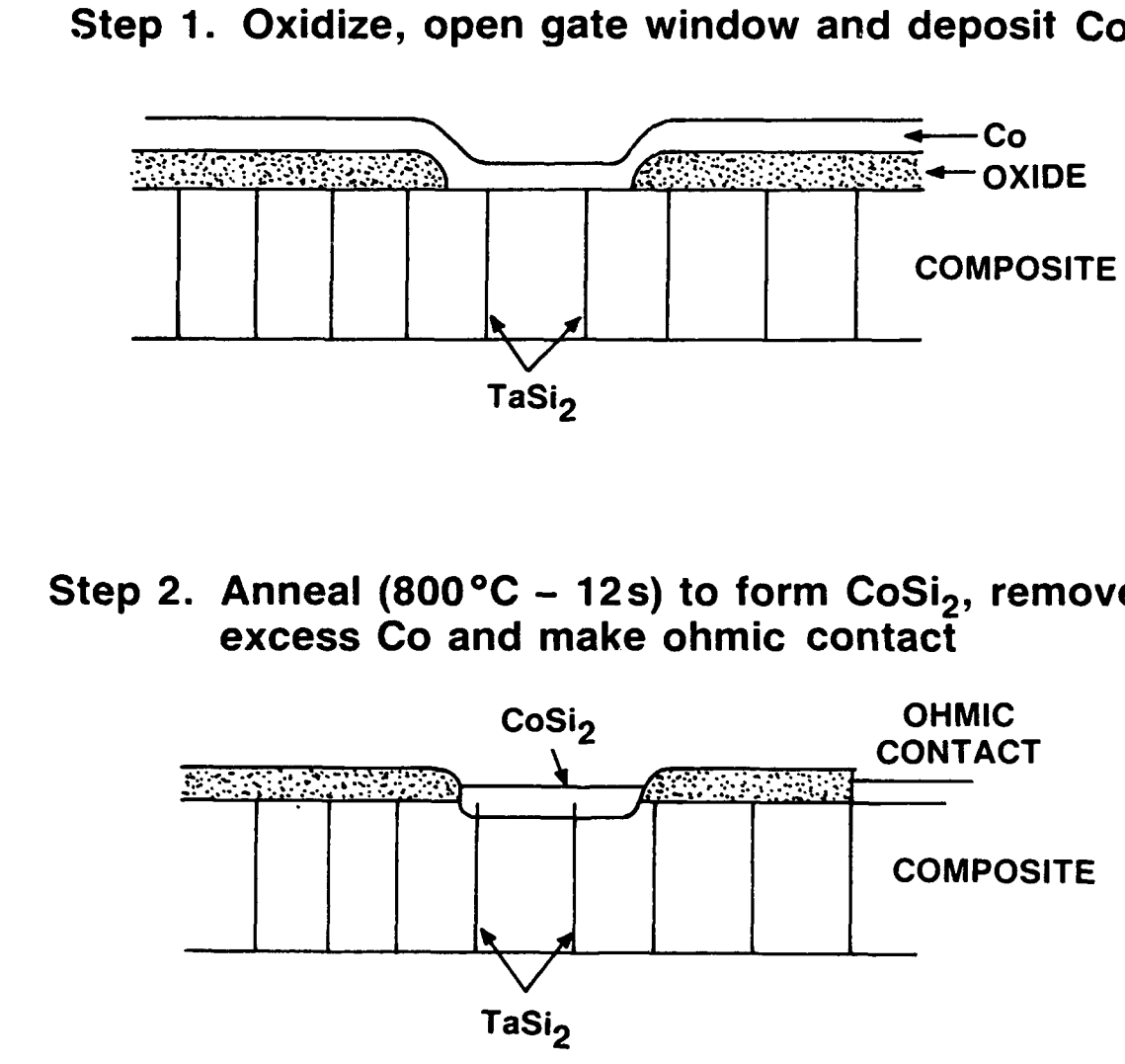


Figure 9. Schematic showing method used to form self-aligned $CoSi_2$ gate contacts.

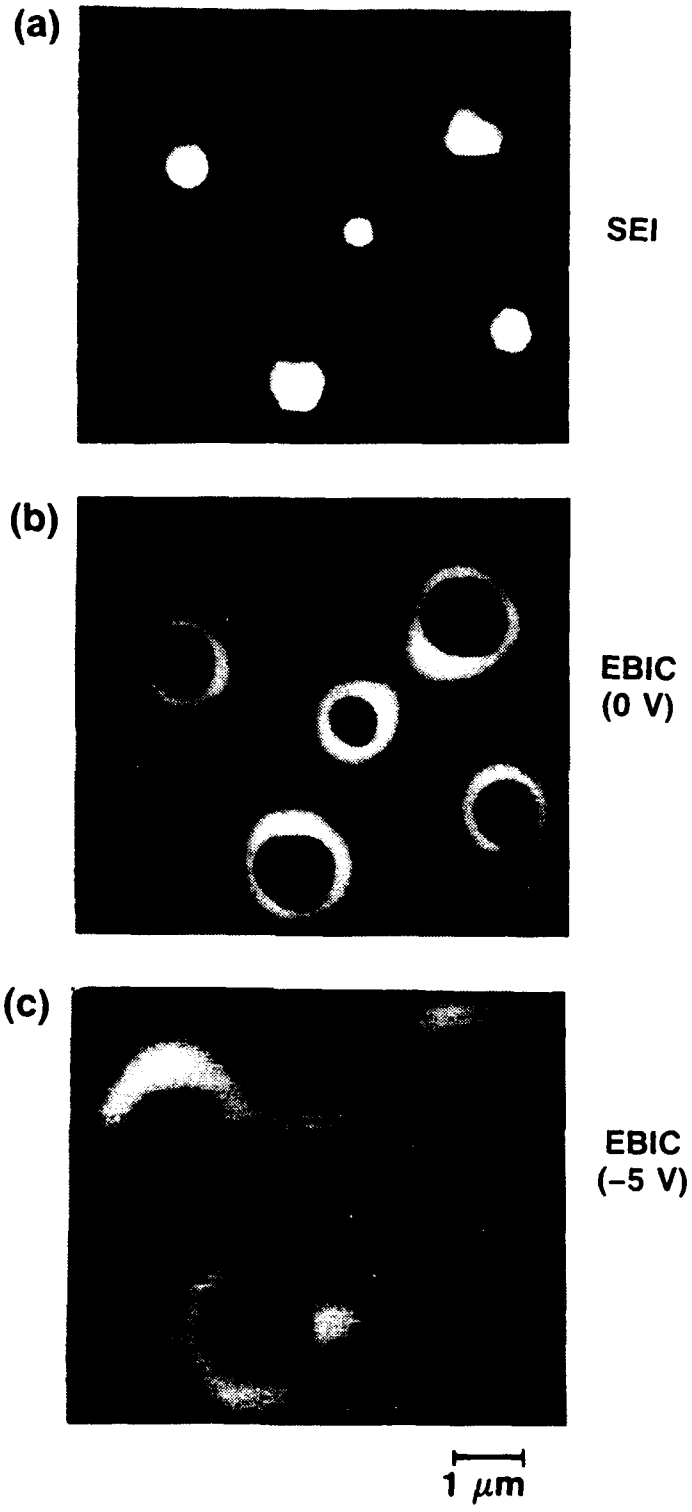


Figure 10. Scanning electron micrographs showing EBIC images of the depletion zones around rods without a bias voltage (b) and with a 5 V reverse bias (c).

4. Transport in Eutectic Composite Materials

In the design of high power opening switches or transistors, the series resistance and transconductance of the device, both of which depend on the basics of transport in the device material, must be optimized. Thus, understanding the physics of electron transport in eutectic composites, is clearly important for device design.

At the beginning of the program, it was clear that the transport of electrons in this composite material would be affected by the presence of the *in situ* depletion zones. If depletion zones are small and do not consume a volume fraction significantly larger than the volume fraction of the second phase, $TaSi_2$, about 2 %, then the composite resistivity should be that of the Si matrix. In the other extreme, if depletion zones are sufficiently large to cause intersection of depletion zones around neighboring rods, then the material should be in the 'pinched-off' state and have a resistivity that is much higher than the Si matrix resistivity given by its carrier concentration and mobility.

The effect of the depletion zones on transport in regions between these extremes was determined from an analysis of the Hall effect and EBIC techniques. As discussed in the previous section, EBIC provides a technique for accurately measuring the carrier concentration in the Si matrix. For a given rod diameter, since the depletion zone size is a function of the carrier concentration and the applied bias voltage only, fitting the EBIC measured depletion zone size to its functional dependence on reverse bias voltage provides a sensitive measure of the local carrier concentration of the Si matrix.

With the Si matrix carrier concentration and the Hall effect carrier concentration, the effect of depletion zone volume on the composite transport properties was analyzed based on a model by Read.[2] Read analyzed the composite resistivity and Hall effect of a semiconductor with an array of parallel space-charge cylinders in a semiconductor. The model, developed long before directionally solidified eutectics were of interest, was originally applied to dislocation arrarys. Read considered that the *in situ* space charge cylinders could affect transport by scattering directly from space charge cylinders, reduction in the average concentration of charge carriers, and distortion of the current streamlines.

Considering the large interrod spacings relative to the room-temperature electron-mean-free path, the first effect is negligible. Hence, the actual mobility of the electrons in the semiconductor matrix will not be affected by the *in situ* depletion zones. The second effect is simple to consider; due to the volume of material in the depletion zones the carrier concentration averaged over the entire composite volume will be less than the localized carrier concentration of material between the depleted zones. In a composite with rods of radius r_o and a rod density N_r, the volume fraction of the depleted material, ε, is

$$\varepsilon = \pi (r_o + W)^2 N_r, \qquad (1)$$

where W is the depletion zone width. The average concentration is given by

$$\langle n \rangle = n(1-\varepsilon). \qquad (2)$$

The final effect of current streamlining was included through a definition of the current streamlining function, $g(\varepsilon)$, according to

$$g(\varepsilon) = \langle E_x \rangle_n / \langle E_x \rangle, \qquad (3)$$

where the x direction is the direction of current flow, $\langle E_x \rangle_n$ is the electric field in the x direction averaged over the normal n-type material between the space-charge cylinders, and $\langle E_x \rangle$ is the applied electric field in the x direction averaged over the entire composite volume. In the limit of a very small volume fraction of depleted material, ε, $g(\varepsilon) = 1$. In the other extreme when ε approaches unity and neighboring depletion zones overlap, the voltage drop occurs primarily over the depleted volume, so that $\langle E_x \rangle_n$ and, therefore, $g(\varepsilon)$ tend to zero. An understanding of depletion zone limited transport in the eutectic composites depends on determining the $g(\varepsilon)$ function particular to the composite system.

Continuing with the Read analysis, the current density averaged over the entire composite volume, $\langle J_x \rangle$, is given by

$$\langle J_x \rangle = q\mu \langle n \rangle \langle E_x \rangle_n, \qquad (4)$$

where μ is the carrier mobility. Substituting the measurable quantity $\langle E_x \rangle$ and the matrix carrier concentration n,

$$\langle J_x \rangle = q\mu n(1-\varepsilon)g(\varepsilon)\langle E_x \rangle. \qquad (5)$$

From Eq. 5 the composite resistivity, ρ_c, is

$$\rho_c^{-1} = q\mu n(1-\varepsilon)g(\varepsilon). \qquad (6)$$

Thus, the ratio of the composite resistivity to the inherent resistivity of the semiconductor matrix is

$$\rho_c/\rho = [(1-\varepsilon)g(\varepsilon)]^{-1}. \qquad (7)$$

Eq. 7 describes the increase in resisitivity resulting from the depletion of carriers and current streamlining around the depleted zones. The composite resistivity, ρ_c, is a measurable parameter. The Hall effect measurement performed on the composite sample with the magnetic field aligned along the axis of the silicide rods provides a carrier concentraion and mobility to be denoted by n_H and μ_H, respectively. Read, using an approach similar to that in Eqs. 4 and 5, showed that these parameters are related to the Si matrix carrier concentration values according to

$$n = n_H[(1-\varepsilon)g(\varepsilon)]^{-1} \qquad (8)$$

and

$$\mu = \mu_H. \qquad (9)$$

The Hall mobility, which depends on the ratio of electric fields and therefore cancels out the $g(\varepsilon)$ term, is independent of the current streamlining factor or the depletion zone volume fraction and represents the physical mobility of electrons in the semiconducting matrix. However, the carrier concentration derived from the Hall effect actually underestimates the semiconductor-matrix carrier concentration by the factor $(1-\varepsilon)g(\varepsilon)$. Thus,

experimentally obtaining n using the EBIC technique and performing the Hall effect to obtain n_H yields the ratio of the composite resistivity to the matrix resistivity. This ratio describes the increase in composite resistivity due to depletion zone limited transport and can be related to both ε (which can also be estimated from the EBIC measurement) and $g(\varepsilon)$.

Hall and EBIC measurements made on composite wafers having a rod density in the range of 1.4 to 1.6 x 10^6 cm^{-2} and covering a wide Hall carrier concentration range are shown in Table III. The ratio of the composite resistivity to the matrix resistivity is plotted in Fig. 11 as a function of the actual carrier concentration, labeled by n_{EBIC} to denote the method used to obtain it. The data show that with a carrier concentration exceeding about 2 x 10^{15} cm^{-3} and less ε than about 0.05, the depletion zones have a minimal effect on resistivity. Below this critical value, however, ε becomes sufficiently large to cause the composite resistivity to significantly exceed the semiconductor matrix value. Since the maximum value obtained for ε is only 0.1, the analysis suggests that it is $g(\varepsilon)$, or the current streamlining effect, that is primarily responsible for the resistivity increase. When ε = 0.1, $g(\varepsilon)$ = 0.15. This sensitivity of $g(\varepsilon)$ to ε is suprising. Read showed that for a regular hexagonal array, $g(\varepsilon)$ is approximately equal to 1-ε when ε is small. Thus for Read's regular lattice of space charge cylinders, $g(\varepsilon)$ would be about 0.9 and the increase in resisitivity would have been minimal. The sensitivity of the eutectic composite to ε is probably attributable to the lack of regularity in the spacing of the rods and their distribution into a cellular network.

V. Samalam[3] at GTE Laboratories has performed an analytical study of these effects and found that percolation theory can explain these results if it is assumed that the rods are distributed in cell-like structures with the density of the rods on the wall of the cell given by a Poisson distribution.

TABLE III. Depletion zone limited transport.

Sample*†	ρ_c (W-cm)	μ_H (cm^2/V-s)	n_H (x 10^{15} cm^{-3})	n_{EBIC} (x 10^{15} cm^{-3})	$\frac{n_{EBIC}}{n_H}\left(\frac{\rho_c}{\rho}\right)$	ϵ
1	1.0	800	7.60	8.50	1.1	0.040
2	2.9	820	2.60	3.40	1.3	0.045
3	3.0	830	2.50	3.60	1.4	0.045
4	4.4	940	1.50	2.20	1.5	0.060
5	9.0	900	0.77	1.50	1.9	0.085
6	15.7	950	0.42	1.25	3.0	0.090
7	44.6	935	0.15	1.10	7.3	0.100

*Wafers from 3 different boules
†N_r = 1.4 – 1.6 x 10^6 rods/cm^2

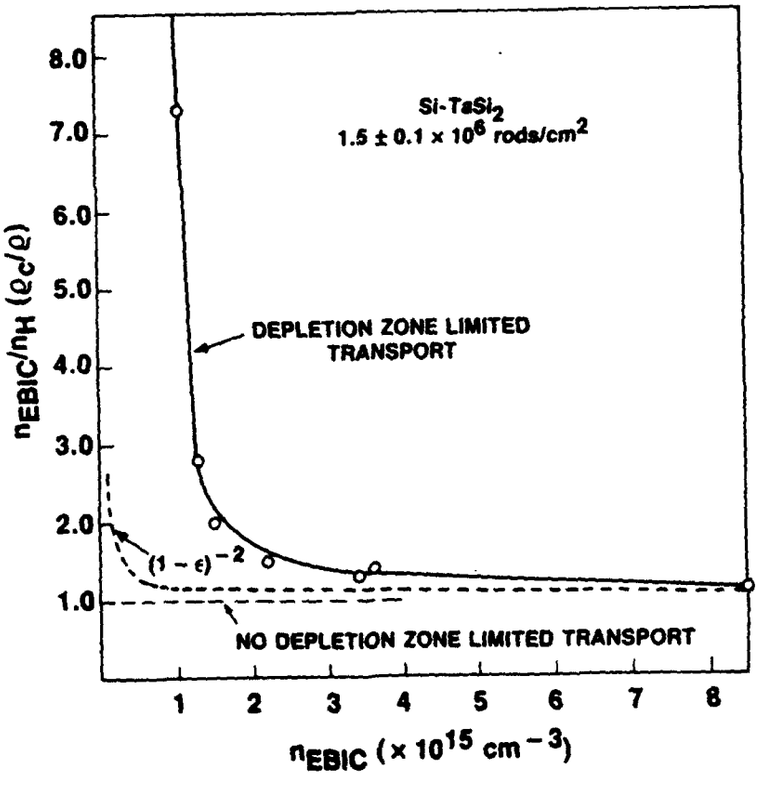


Figure 11. Correlation of the EBIC and Hall carrier concentration ratio (n_{EBIC}/n_H) as a function of the matrix carrier concentration. The significant increase in this ratio below 2 x 10^{15} cm^{-3} is due to depletion zone limited transport.

5. EUTECTIC COMPOSITE TRANSISTORS

5.1 Transistor Design and Fabrication

Eutectic composite transistors have been designed and fabricated using a basic concentric ring design. The outside and inside ring constitute the source and drain, respectively, so that current must pass under the central ring gate contact. Thus, biasing the gate enables expansion of the depletion zones in this region and current 'pinch-off'.

Ohmic and gate ring contacts were made essentially the same way as the comparable diode contacts. A quarter section of the surface contacts of a typical device is shown in Fig. 12. As will be explained in a later section, characterization of transistors made it clear that divergence of the rods under the ohmic contacts limited blocking voltage. Contacts were developed that resolved these issues by forming source and drain surface films that contacted the matrix Si only and not the metallic rods. A schematic of the process is shown in Fig. 13 .

For this contacting procedure, the rods within the ohmic contact rings are etched back just over 1 μm. The cylindrical areas are refilled with resistive polycrystalline Si by a CVD process. The excess Si coated on the wafer surface is removed in a planarization process. Following this, the wafer may be processed as a virgin wafer using the $CoSi_2/n^+$ process for ohmic contacts. The surface silicide metallization contacts either the conducting matrix Si or the resistive polycrystalline Si, without reaching the recessed $TaSi_2$ rods. Devices made using this contacting process, did display comparably low surface resistance, but further evaluation will be required to determine if it elevates the blocking voltage.

5.2 Transistor Characteristics

Understanding the nature of transistor action in eutectic composites and assessing the implication for high power switching is an important part of this program. In this section, the basic features of eutectic composite transitors will be reviewed. The use of advanced characterization and modeling techniques and the first pulsed power tests will be presented in subsequent sections. The present understanding of eutectic composite transistors and its potential impact on pulsed power is reviewed in the final section.

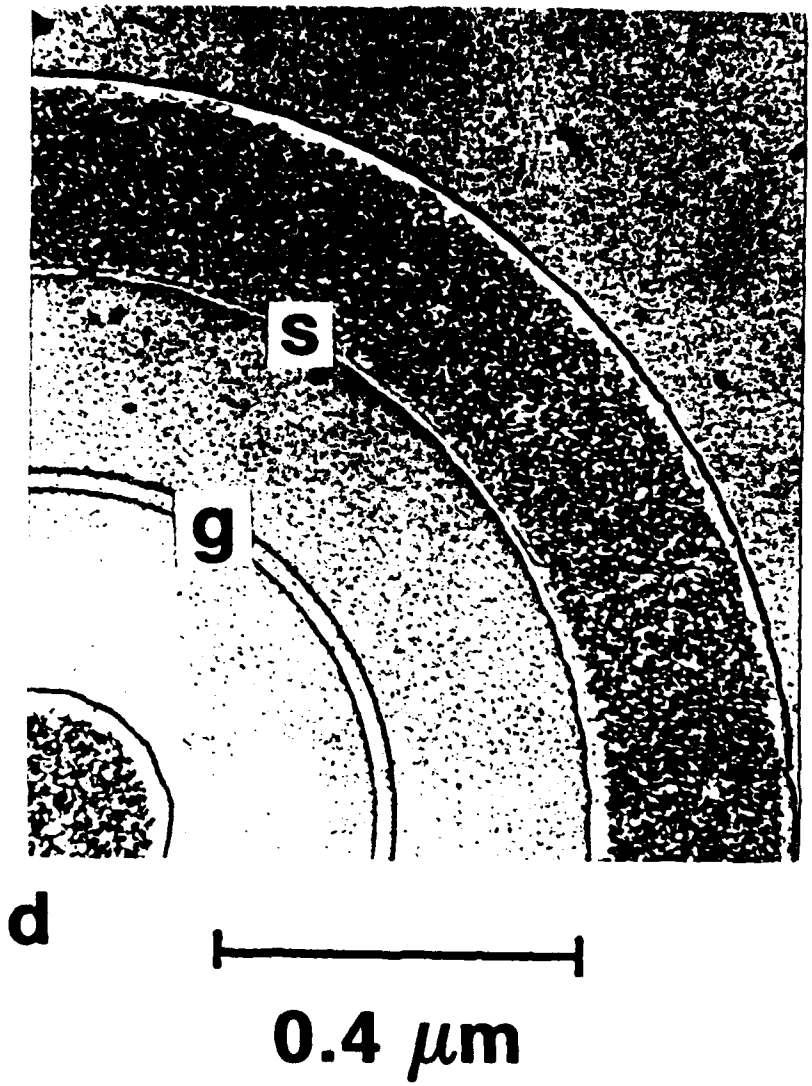
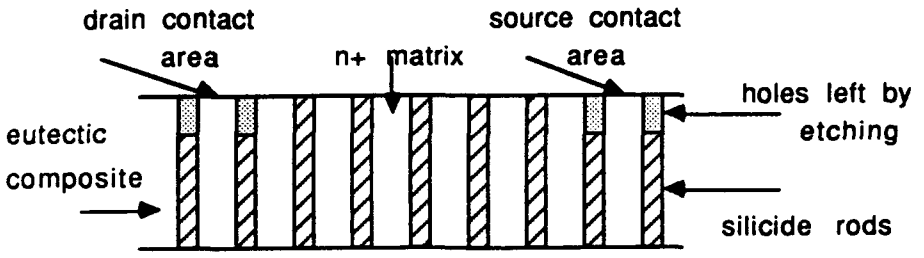
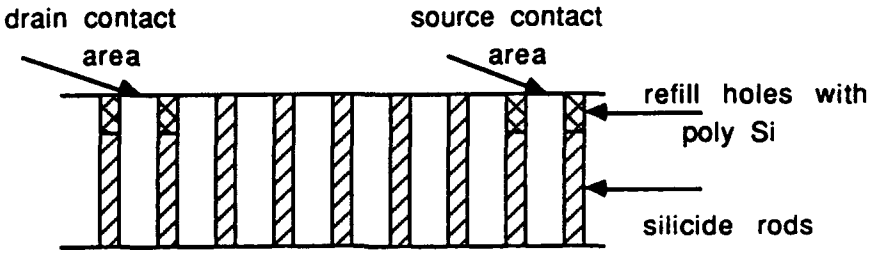


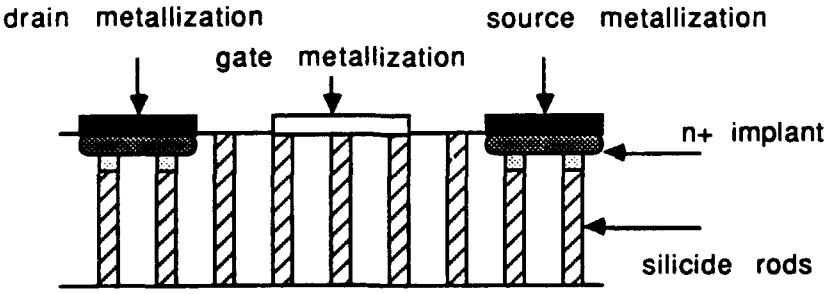
Figure 12. A quarter section of the concentric ring pattern of source, drain and gate contacts used to fabricate the transistor.



Step 1: Etch back rods in source and drain areas



Step 2: Deposit high resistivity poly Si and planarize



Step 3 : Implant into source and drain areas and deposit metallizations.

Figure 13. Schematic procedure for fabricating ohmic contacts that are insulated from the metallic rods of a eutectic composite.

An example of the current-voltage characteristics of a eutectic composite transistor with the drain current plotted against the drain voltage for different gate voltages is shown in Fig. 14. The device shown blocks 1000 V. The basic characteristics of the device are similar to those of a conventional metal-semiconductor field effect transistor (MESFET). Both display a linear region at low voltage and a saturation region at higher voltages. MESFETs also display a third region, a breakdown region, that is not characterisitic of the eutectic composite transistor. Studies of these devices have varied the dimensions of the concentric ring contacts, the thickness of the wafer, and, over a small region, the carrier concentration. Before a discussion of the effects of these parameters, several points can be made on the device's basic characteristics.

• The series resistance of the device, taken as the slope of the unbiased curve in the limit of small drain voltages, is in agreement with the value expected from the composite resistivity and the device dimensions assuming the entire thickness of the wafer is used for transport. This and the ability to 'pinch-off' the device verifies that it is indeed a 'bulk' transistor.

• The drain current in the pinch-off condition, *defined as that point* at which an increase in the bias voltage does not result in a further decrease in the drain current, varied significantly from device to device. Minimum drain currents for the pinch-off condition measured at 200 V were 2% of the unbiased saturation value. Thus, for example, in a device with a 20 mA saturation current, pinch-off attained with a -12 V bias at a 200 V drain potential was 400 μA. This may be considered high for a Si p-n junction device but, considering the dimensions of the device and the low height of the Schottky barrier, these leakage currents are in-line with expectations. In general, transistor leakage currents were significantly lower than the diode reverse bias currents when compared for similar voltage and surface contact area.

• Characteristics of the transistors were also measured as a function of temperature. Heating devices from 22 C to 75 C severely degraded the device properties as the leakage current (measured at -12 V gate and 10 V drain) increased by a factor of 17. The increase can be largely explained by thermal activation over the small Schottky barrier. Higher Schottky barrier systems would not be expected to be as temperature sensitive.

• At sufficiently high drain voltages devices became leaky and broke down. Breakdown was observed to be catastrophic and destroyed device characteristics. However, device breakdown was observed at significantly higher voltages than expected for conventional planar devices when compared at a similar carrier concentration.

The properties of eutectic composite transistors and the realization of their potential for high blocking voltage became apparent after a study of the effects of device dimensions, carrier concentration and resistivity on device blocking voltage. Results from this study are presented in Table IV. For five different devices the table gives the carrier concentration and resistivity of the wafer, the gate to drain (g-d) distance, the wafer thickness and the voltage at breakdown, V_{max}. Different entries for the same device corresponds to measurements at different wafer thicknesses. The wafer thickness was found to have a significant effect on the breakdown voltage. The device labeled SiTa 61 #25 illustrates the effect. Measurement of the device on the original 500 μm thick wafer indicated catastrophic failure at 50 V. Exceeding 50 V on the drain resulted in a loss of the characteristics. After thinning the wafer from the side opposite that with the surface contacts, the same device was retested. Thinning the wafer to 250 μm resulted in recovery of the device. Retested the device yielded similar characteristics with half the original saturation and current and a breakdown voltage of 350 V. Thinning the wafer further to 125 μm, and retesting yielded another halving of the saturation current and a new breakdown voltage of 600 V. This value is at least three times the blocking voltage of a conventional planar device in a wafer of the same 3×10^{15} cm^{-3} carrier concentration.

The data in Table IV also shows that the breakdown voltage increases with the gate-to-drain spacing. This observation and the thickness effect indicates that devices breakdown via a 'punch-through' mechanism. In this mechanism, failure occurs when the depletion zone extends to the drain. A model, schematically illustrated in Fig. 15, based on this failure mode can be used to explain both the thickness and the gate-to-drain spacing effects. SEM longitudinal micrographs and EBIC both reveal that some rods are misaligned. Maximum misalignment has been measured to be 6^{o} relative to crystal axis (or wafer normal). Thus, as shown in the figure, assuming maximum misalignment, separation of the gate and drain contacts, as they are extended by contact to the rods, is dependent on the wafer thickness. When the surface gate-to-drain spacing is 140 μm, at the bottom of a 500 μm thick wafer

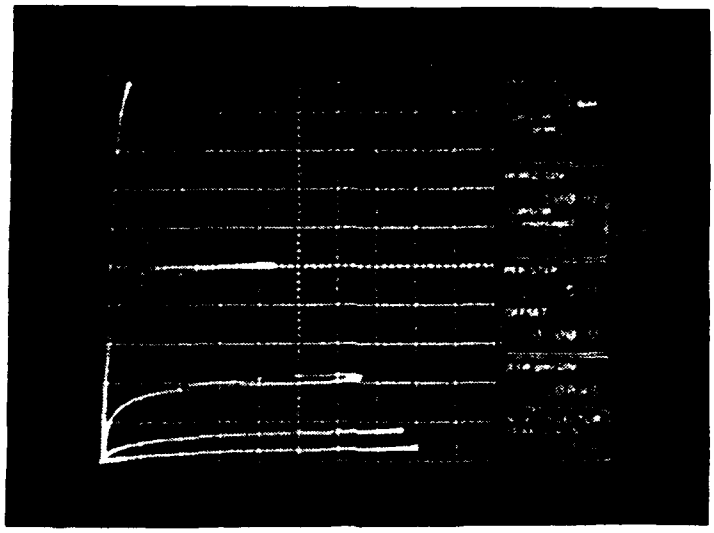


Figure 14.The transfer characteristics of a Si-$TaSi_2$ eutectic composite transistor that blocks 1000 V.

Table IV. Factors Affecting the Maximum Blocking Voltage

Wafer	Carrier Concentration (10^{15})	Resistivity (Ω-cm)	g-d Distance (μm)	Thickness (μm)	V_{max} (V)
SiTa 61 #25	3	8	137	500	50
SiTa 61 #25	3	8	137	250	350
SiTa 61 #25	3	8	137	125	600
SiTa 61 #41	2	12	150	500	90
SiTa 61 #41	2	12	150	250	250
SiTa 61 #41	2	12	150	125	500
SiTa 59 #31	1	18.5	180	250	500
SiTa 59 #31	1	18.5	180	125	700
SiTa 59 #47	1	50	62	250	40
SiTa 68 #9	1	18.5	250	125	1000

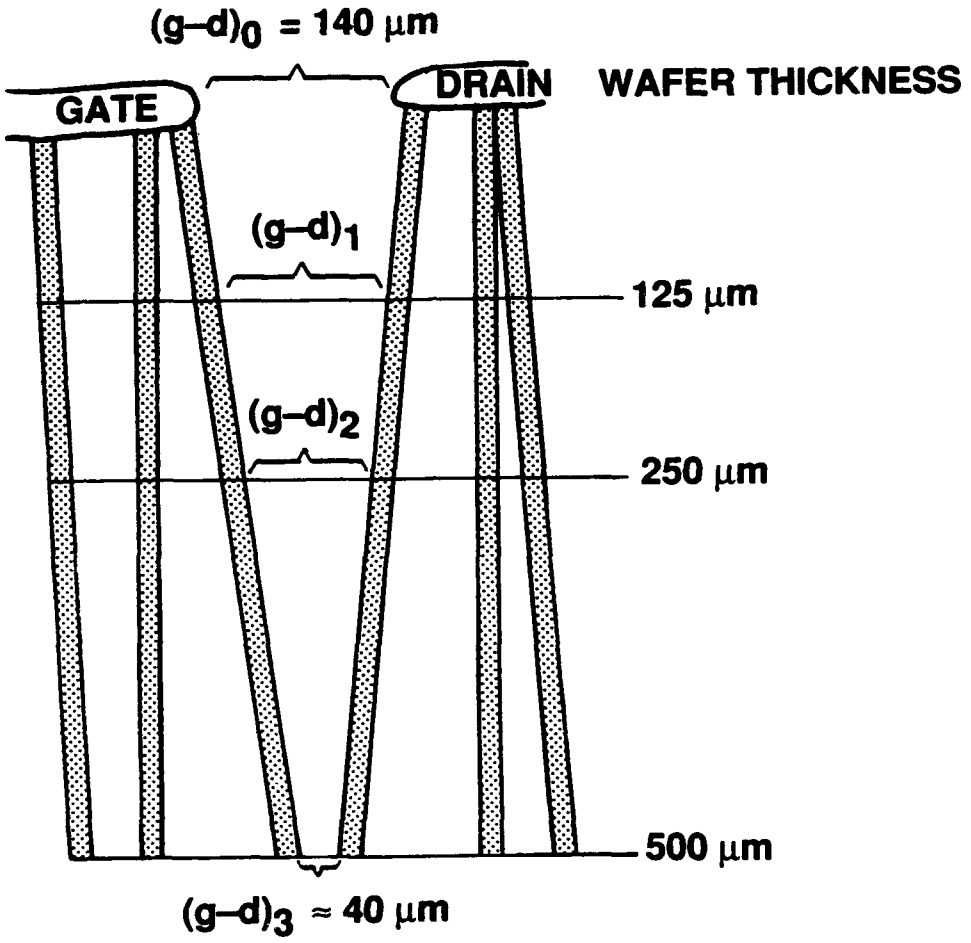


Figure 15. A schematic model showing how the effective gate to drain distance changes as a function of wafer thickness due to rod divergence.

the effective separation of the gate from the drain is only 40 μm. Similarly for a 250 μm wafer thickness, the separation is only 90 μm and so on.

5.3 EBIC Characterization

Conventional electron-beam-induced current (EBIC) techniques applied to the characterization of eutectic diodes have been used to obtain graphic images of the depletion zone around a $TaSi_2$ rod and have enabled a quantitative determination of the Si matrix carrier concentration. The EBIC technique played an important role in diode evaluation. During the latter part of this program, experimentation began on the development of a new three terminal EBIC technique which may be as important for transistor devices as conventional EBIC has been for diodes. Both techniques involve the generation of scanning electron microscope images which show perturbations of device operation due the electron-hole pairs created by the electron beam incident on the sample. In conventional EBIC, a signal corresponding to the the current collected in a diode junction is used to form the image. It allows the visualization of the depletion regions and relative minority carrier collection efficiency of the junction rods in these devices. An image showing the annular depletion zones around the $TaSi_2$ rods was shown in Fig. 10. This technique graphically confirms the basis of transistor action in these devices, and gives additional information on uniformity of material and device characteristics.

The new three terminal technique uses the electron beam generation of electron-hole pairs to alter the local electric fields in the current channels of the device. The beam-generated carriers will tend to momentarily reduce any potential differences and electric fields. As a result, depletion widths in the gate region will decrease, thereby increasing the drain current. In these SME transistors, this effect is only pronounced at partial pinch-off in regions where current crowding occurs due to velocity saturation of the carriers. This technique can therefore be used to visualize the location and extent of current crowding in different regimes of device operation by recording images as a function of gate and drain voltage. Information can therefore be gained on the characteristics and uniformity of the transistor effects in different areas of the device.

To implement this technique, we have devised a common-source circuit (Fig. 16) where the

current amplifier is placed so that the gate current, due to the conventional EBIC effect, and the drain current have opposite polarities, and so yield opposite contrast and can be distinguished. Fig. 17 shows a three-terminal EBIC micrograph of a eutectic composite transistor. The gate depletion zones are imaged as lighter contrast, and current crowding in areas of excess current flow is imaged as dark regions extending from the gate towards the drain.

This technique, still in its infancy, promises to be very important for understanding current voltage and breakdown characteristics. As indicated above the depletion zones extending from the gate are imaged as the light region in Fig. 17. The ablility to follow the extent of the depletion zone enables comparison with models and may provide important data on theories of breakdown. The dark image areas indicate high current flow and represent areas of nonuniformity which may play an important role in surface breakdown phenomena. In both cases with additional work, the three terminal EBIC technique may provide the needed experimental verification of the results of numerical modeling of eutectic composite transistors.

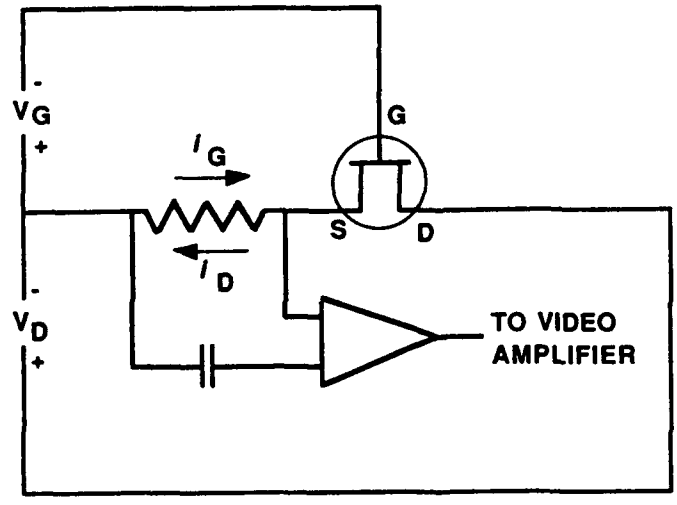
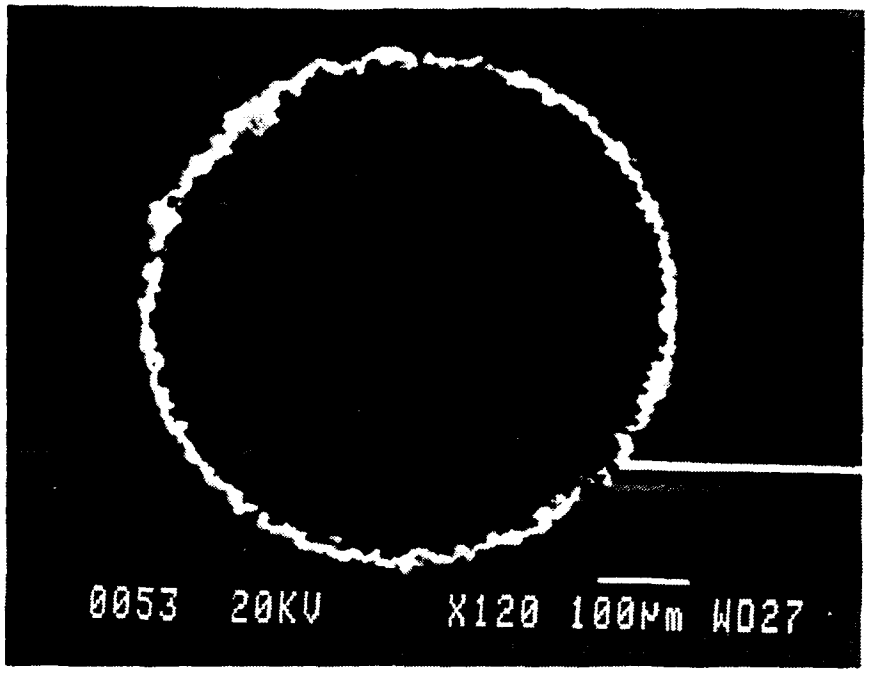


Figure 16. The circuit diagram used for the three terminal EBIC technique.

(a)



(b)

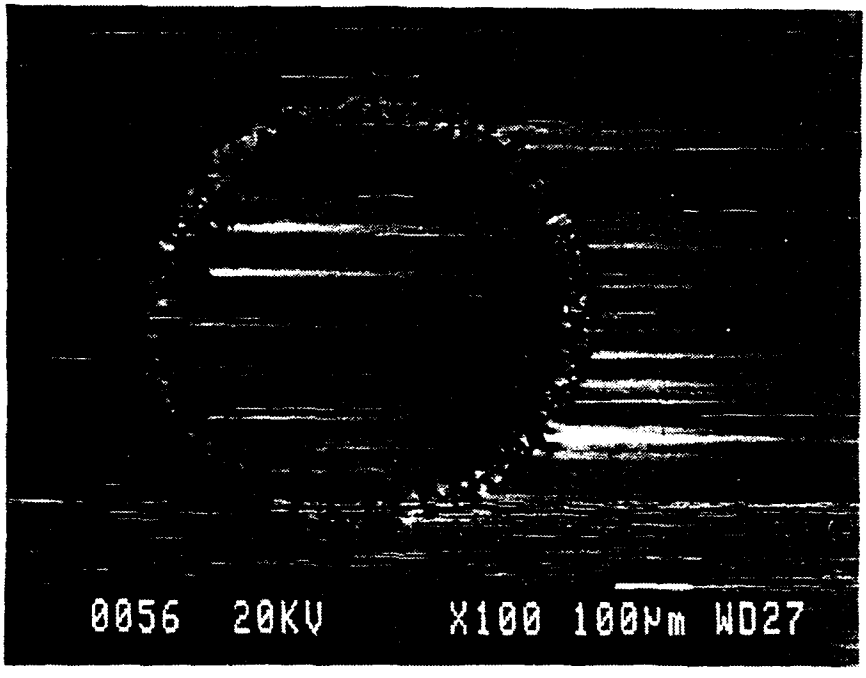


Figure 17. Three terminal EBIC micrographs of a eutectic composite transistor with (a) no gate bias and (b) a 10 V reverse bias. Both transistors have a source to drain voltage of 90 V. The dark channels emanating from the gate ring indicate regions of current saturation.

5.4. Modeling of Transistor Characteristics

Numerical modeling studies of SME transistors were undertaken both to determine the effects of device and material parameters on transistor performance and to understand the origins of their unusual resistance to avalanche breakdown. Computer simulations were performed using the PISCES code. The PISCES software models two-dimensional distributions of potential and carrier concentrations for arbitrary device geometries and bias conditions. The version used was PISCES-IIB of Stanford Electronics Laboratories on a Digital VAX 11/785 mainframe computer.

One unique feature of these devices is that the $TaSi_2$ rods which lie between the source, gate, and drain contacts are not electrically contacted. These rods and their associated depletion regions float to potentials that are determined by the device parameters and external voltages. We have performed extensive numerical simulations to study the effects of the floating rods in high voltage operation, and have shown that they are responsible for the striking breakdown resistance of SME transistors.

Two types of simulation experiments were performed. In the first, the effect of floating junctions on device breakdown was studied. The second was aimed at optimizing material and device parameters for pulsed power applications.

Two basic simulation geometries, shown in Fig. 18, were compared to study the effects of floating junctions. The conventional case, used as a control (left diagram), has one gate junction close to the source. The other case (right diagram) has six equally spaced floating rod-shaped junctions between the gate and drain. With six floating junctions, the simulation uses the maximum number of electrodes that can be handled by the PISCES software. Simulations were specified for n-type Si with uniform impurity concentrations of 0.5 - 5 x 10^{15} cm^{-3} . PISCES-IIB allows the placement of a simple lumped resistance on a given electrode. This capability was exploited to account for floating rods, which were simulated by inserting the maximum allowable resistance (10^{31} Ω) on the floating rods and biasing them to the drain.

To simulate the operation of the transistor, the source was held at 0 V, the gate electrode (the

first rod) was biased to -2 V, and the drain electrode was stepped from 0 to 200 V in 10 V increments. The potential versus distance from the source is shown in Fig. 19 and the maximum electric field versus drain potential is shown in Fig. 20 comparing the two cases with and without floating rods.

For the conventional case without floating junctions, the potential increases parabolically with distance similarly to conventional planar junctions. The maximum electric field increases monotonically with increasing drain voltage. In the case with floating rods, the depletion zone at the gate rod expands with increasing voltage as in the conventional case, but only until it intersects the depletion zone of the first floating rod. This latter rod then floats in potential with further increases in applied voltage so that its depletion zone expands towards the next floating rod. In this way, the applied voltage is spread across successive floating rods. The electric field at the gate rod reaches a maximum when the drain voltage is sufficient to extend its depletion zone to the first floating rod. It is then clamped at this value as the drain voltage is increased. Eventually, the same maximum field is attained at the first floating rod, and so on. The actual value of this field depends on the interrod spacing and the carrier concentration, but by proper design it can be made lower than the avalanche field.

The results of this model clearly indicate that the floating rods inhibit avalanche breakdown and result in a larger depletion zone than would be found in a classical planar junction device. In a conventional device without floating rods, the maximum electric field increases as the drain voltage increases until it reaches the critical value for avalanche breakdown. With the floating rods, however, as the drain voltage is increased the field reaches a maximum that may be significantly lower than the critical field for avalanche breakdown. Thus, even as the drain voltage is increased to a value significantly beyond that required to yield avalanche breakdown in a conventional device, avalanche breakdown is avoided because the field never reaches a value sufficient to cause impact ionization. However, avalanche will eventually occur by a 'punch-through' mechanism when the depletion region expands to reach the drain contact and no additional floating rods are available to accommodate further voltage increases. Figure 21 shows how the electric field increases after punch-through of the depletion zone to the drain in a small gate-to-drain distance device. Therefore, the maximum blocking voltage of the device is determined by the gate-to-drain spacing, rather than the carrier concentration as in conventional devices. This distance can in principal be designed to yield

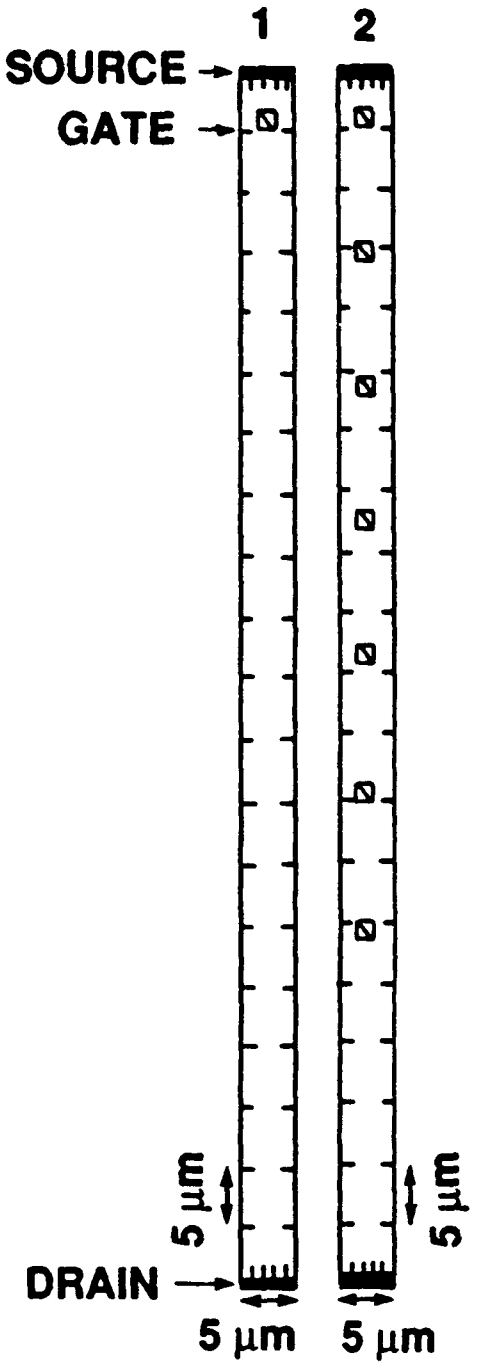


Figure 18. Model simulation geometries: gate rod only (left): with floating rods(right).

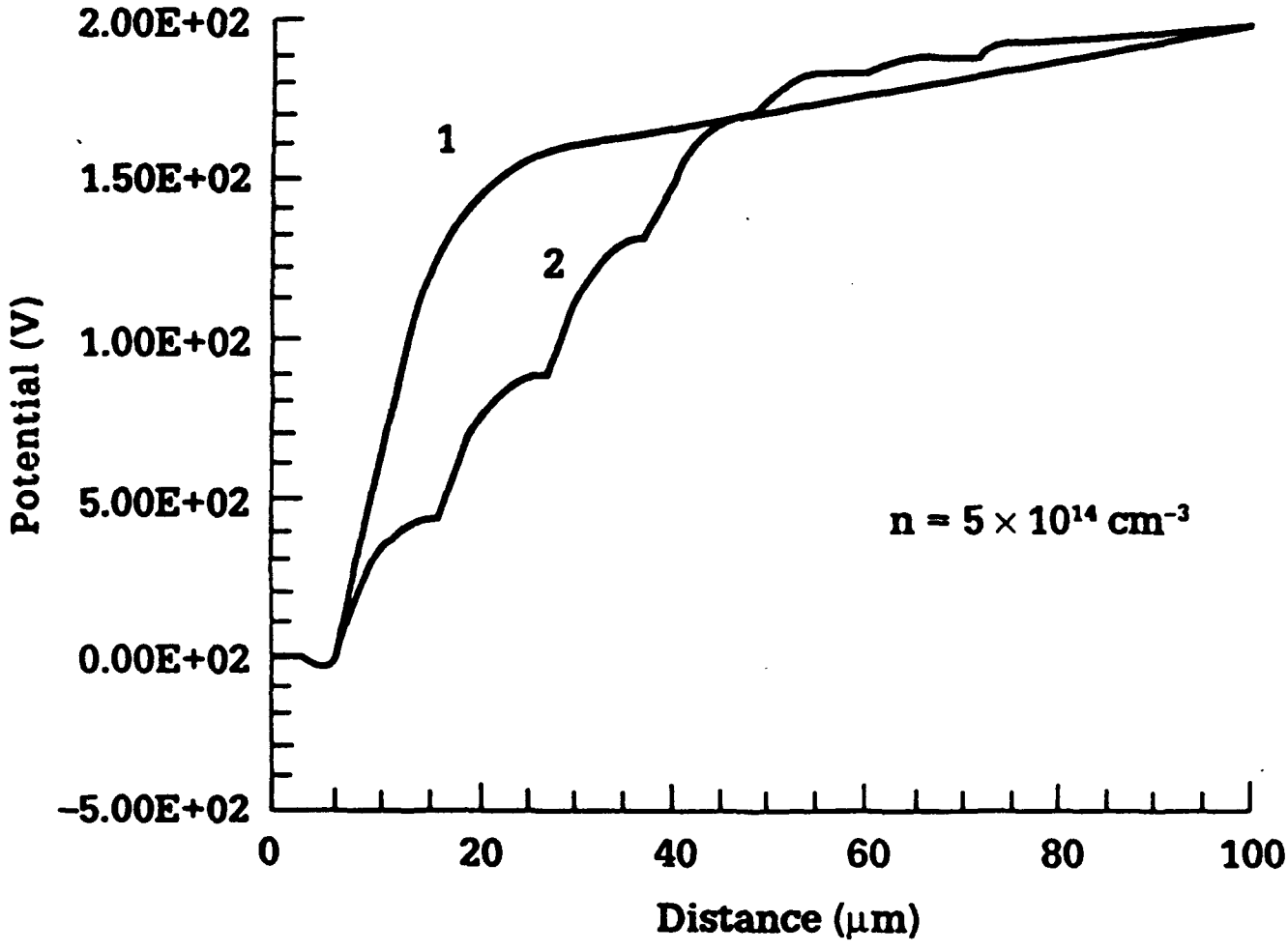


Figure 19. Potential vs. distance from the source: (1) gate rod only; (2) with floating rods.

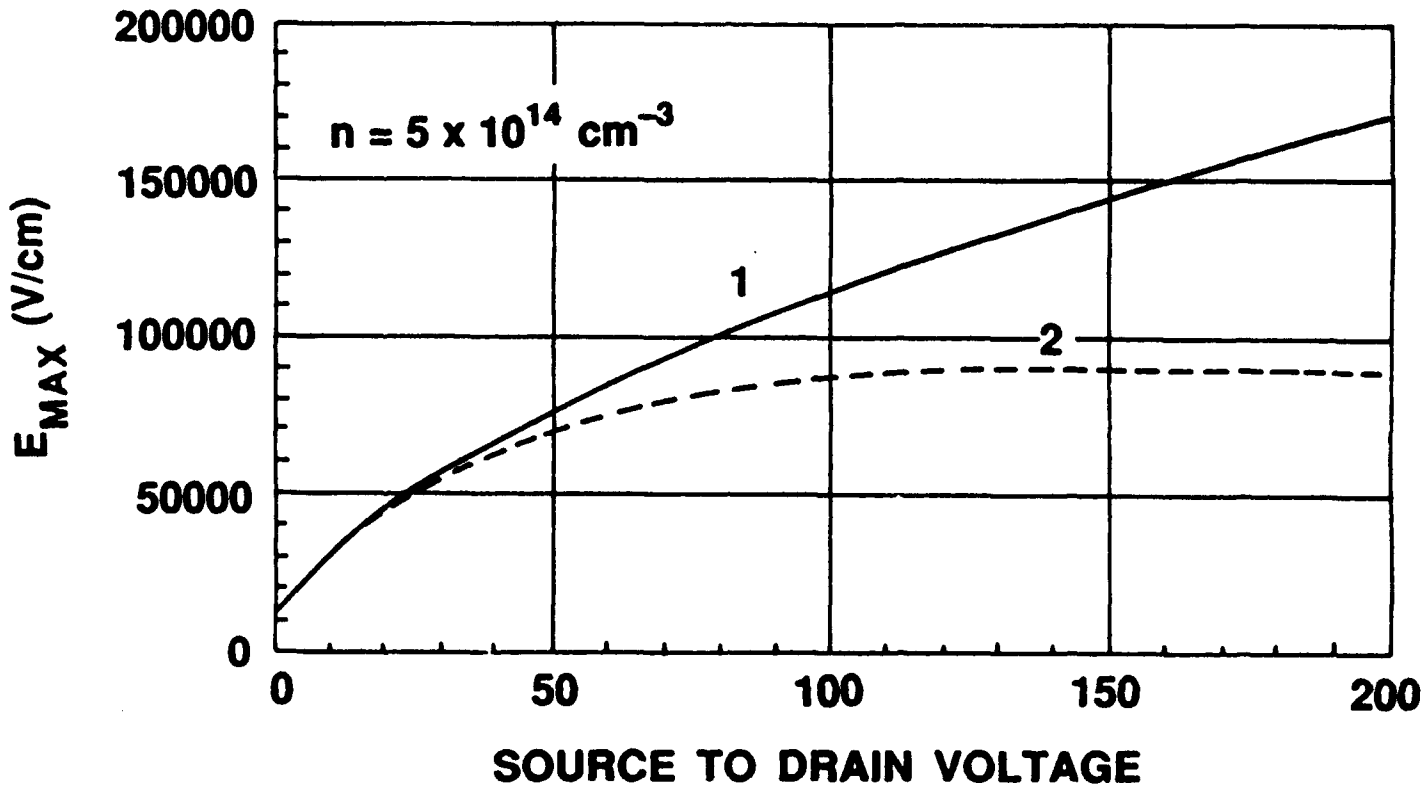


Figure 20. Maximum electric field vs. drain voltage: (1) gate rod only; (2) with floating rods.

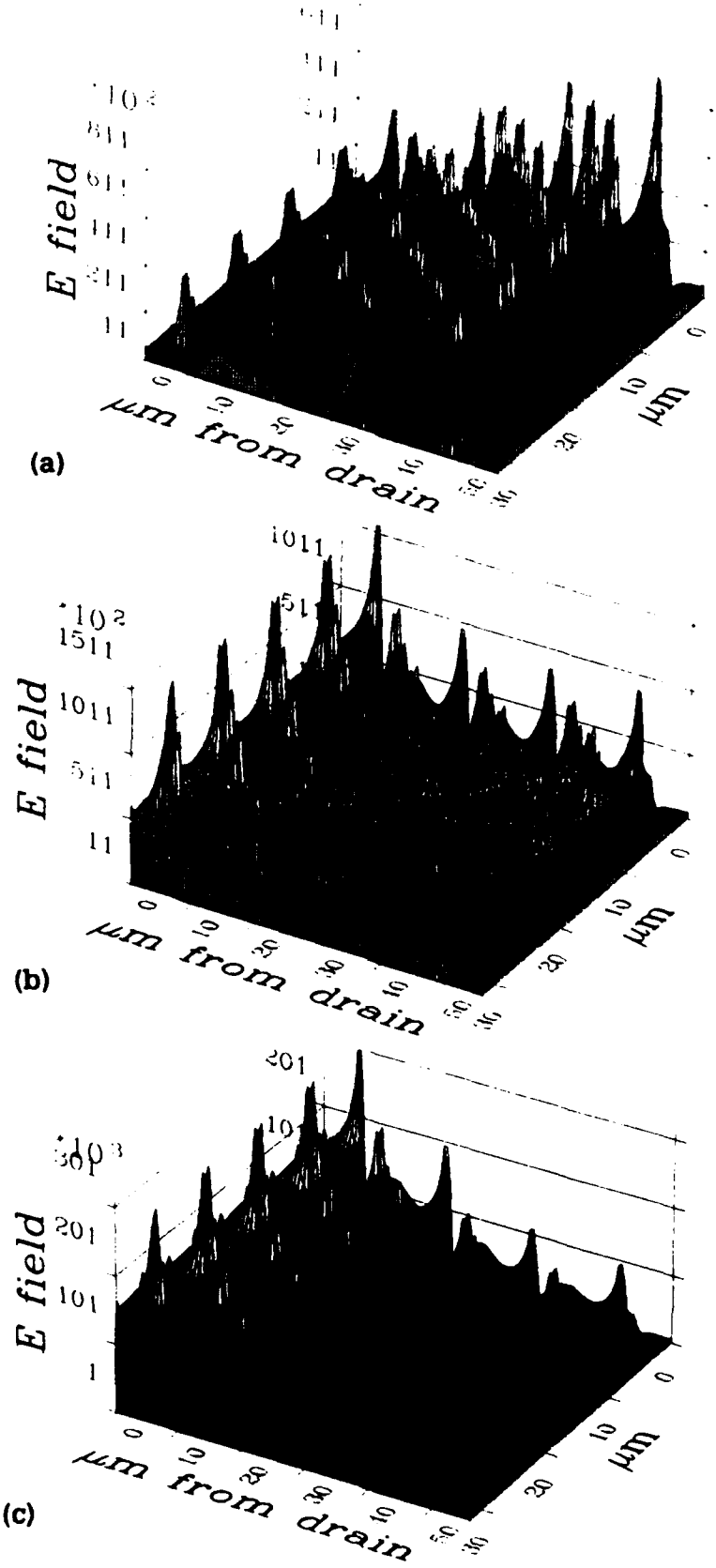


Figure 21. Model predictions of the electric field as a function of distance from the drain for the case of no gate bias and (a) 100 V_{sd}, (b) 200 V_{sd}, and (c) 400 V_{sd}. At low drain voltages E_{max} saturates. Once the depletion zone reaches the drain, an increase in the drain voltage causes the field at the last rod to exceed the saturation E_{max} and eventually cause breakdown.

an arbitrarily large blocking voltage.

Further model calculations were used to investigate the ways that these devices could be optimized for simultaneous high voltage and high current operation. This was done by calculating the carrier concentration required to hold the maximum electric field to a given value less than that of the avalanche field for different interrod spacings. The saturation current density in each case was also determined. A microstructure with floating rods similar to that shown in Fig. 18 was modeled to determine the carrier concentration which yields a saturation E_{max} of 100 kV/cm. This maximum field was chosen because it is conservatively below the value that would lead to avalanche breakdown. The average electric field in the gate-drain region and the gate-drain distance needed to hold off 1000 V were also calculated. The microstructure was then scaled uniformly to different interrod spacings and rod diameters, keeping the volume fraction of the rods constant (as would be the case with real eutectic systems).

Table V. Model calculations of SME transistor parameters for combinations of carrier concentration and interrod spacing that will yield a maximum electric field of 100 kV/cm.

Rod spacing	Avg. Field at E_{max}	G-D distance for V_{SD}=1000 V	N_D	J_S
4 μm	5.08×10^4 V/cm	200 μm	5.9×10^{15} cm^{-3}	6500 A/cm^2
7	5.37×10^4	186	3.3×10^{15}	3300
23	5.44×10^4	184	1.0×10^{15}	870

The results are shown in Table V for interrod spacings of 4, 7, and 23 μm. Although the gate-to-drain distances needed to hold off 1000 V are similar in all three cases and the spatially averaged field remains nearly constant at about one-half E_{max}, the carrier concentrations and saturation current densities at zero gate bias are quite different. The highest current is found at the smallest interrod spacing. The conclusion from these modeling studies is clear. Eutectics with higher rod density should be able to switch much higher currents than low rod density devices because of the higher matrix carrier

concentration without a degredation in the maximum hold-off voltages. In principle, then, eutectic composite transistors should be able to switch high voltages and high currents.

5.5 Pulsed Tests

Throughout the program, transistor characterization has been done using curve tracers in an essentially dc mode. At the high voltage, high current range, dc testing lead to some device heating. For this reason, and because the ultimate application of these devices is in pulsed applications, high voltage devices were prepared for pulsed testing. Devices with dimensions designed to hold-off 2000 V (assuming that the average field between gate and drain must be less than 50 kV/cm) have been processed and subject to an initial test. The high voltage properties were tested using a high voltage gas discharge apparatus schematically illustrated in Fig. 22. This equipment is capable of delivering 100 ns pulses of 2 - 10 kV.

A preliminary measurement on a device shows breakdown at lower than the intended 2000 V and passage of 5 A of current. The test is an indication that at these high voltages, surface breakdown may limit the device. Because the $TaSi_2$ rods extend through the thickness of the device, the applied potentials appear at both top and bottom surfaces, as well as in the interior. This suggests that surface passivation of both surfaces may be required before testing. Surface breakdown issues will have to be examined in future studies.

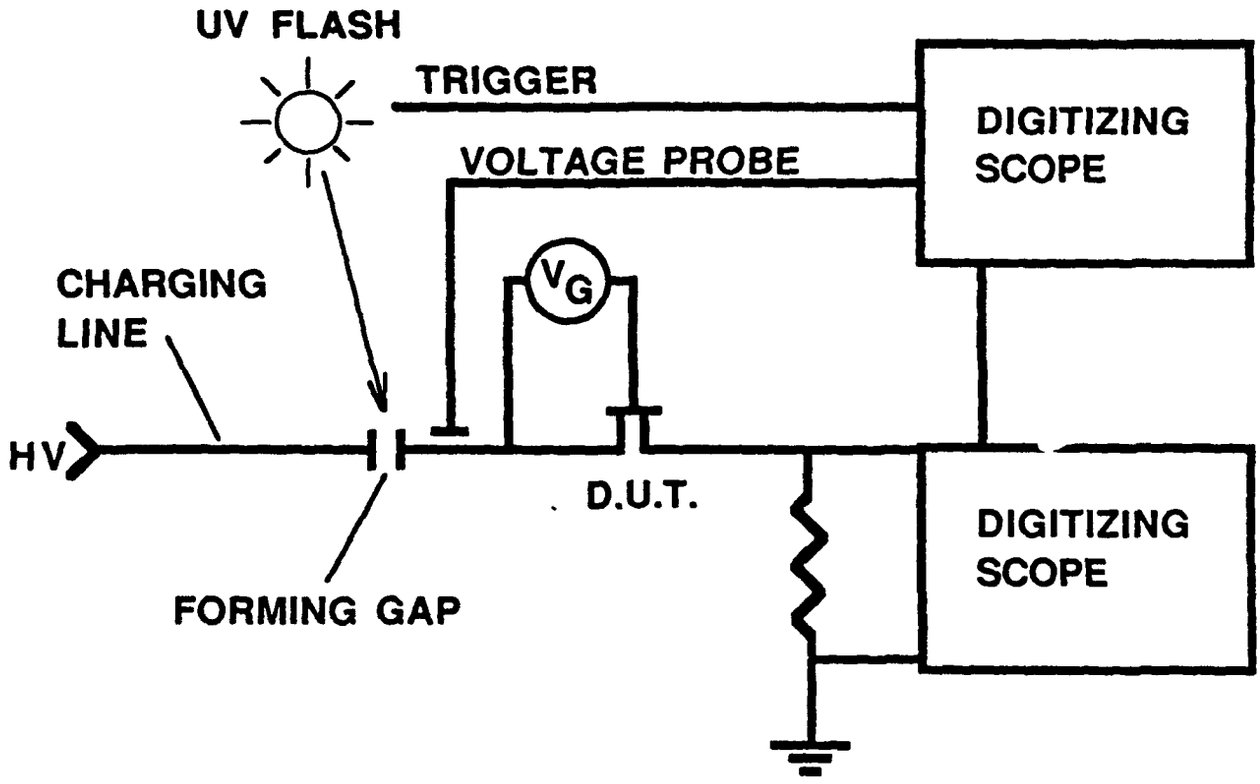


Figure 22. Schematic diagram of the high voltage plasma discharge apparatus.

6. IMPLICATIONS OF PULSED POWER

Semiconductor-metal eutectic composites offer many intriguing opportunities for pulsed power devices. Experimentally, the maximum hold-off voltage demonstrated to date is 1000 V, but all the experimental and theoretical studies derived in this program indicate that significantly higher voltages could be handled, and most importantly, that eutectic composite devices should be possible that can hold off substantially higher voltages than conventional planar junction devices. According to the model and experimental support attained to date, a 50 kV device can be made if the gate to drain spacing is maintained at 1 cm.

Achievement of high current also appears to be possible with eutectic composite devices. Assuming a 1 in diameter wafer, which is typical of those currently grown, and achievement of about 100 A/cm^2, which is typical of current devices, efficient use of chip space in a device with a 0.2 cm gate-to-drain spacing to derive a 10 kV hold-off voltage would enable switching of about 50 A. Development of techniques for growing 2 in diameter composite boules, would yield 200 A. Orders of magnitude improvement could be obtained if the current density were increased. Modeling suggests that development of eutectic composite with finer interrod spacings could yield the substantial current increases desired and, thus, also points to the need for continuing studies of new materials systems and factors that affect the interrod spacing in known systems.

Progress towards demonstration of higher voltage, higher current devices will require continued work on the dual research fronts of materials and devices. With the currently available material, devices can be envisioned that can block high voltage and switch high currents. High current switching depends on fabrication of large area devices or connecting large devices in parallel. This may impose stringent demands on structural uniformity of the Si-$TaSi_2$ material. Observations on device yield within a wafer have not indicated any correlation with device size, but since all devices on a given wafer are not active, that is yield per wafer is not 100 %, building devices that cover an entire wafer may undergo yield limitations.

Increases in current switching beyond that possible with large area devices can result from the development of new materials. This program has pointed towards the need for materials

with better alignment of rods to enable use of thicker wafers, higher barrier heights to reduce leakage and temperature sensitivity and, most importantly, higher rod density to allow for higher carrier concentration.

Since the devices are intended for pulsed power applications, more work will need to be done on testing under pulsed conditions and, any unexpected limitations imposed by this should be understood using modeling techniques. This is one aspect of this research that must be expanded.

Furthermore, the concept of floating junctions developed in this work may have implications for pulsed power devices that go significantly beyond SME devices. Incorporation of floating junctions to increase the current and voltage capabilities of conventional devices, possible using advanced processing techniques, holds considerable promise for the general field of solid-state opening switches.

7. REFERENCES

1. B. Reiss and T. Renner, Zeitschrift fur Naturforshung 21, pp. 546-548 (1966).

2. W. T. Read, Philos. Mag., 46, 111 (1955).

3. V. J. Samalam, J. Appl. Phys., 67, 2165 (1990).

Appendix B
Recent Publications

IEEE
Conference Record of the

1992 Twentieth
Power Modulator Symposium

HIGH VOLTAGE SEMICONDUCTOR-METAL EUTECTIC TRANSISTORS FOR PULSED POWER SWITCHING APPLICATIONS

Q.V. Nguyen, P.R. Rossoni, M. Levinson and B.M. Ditchek
GTE Laboratories Inc., Waltham, MA 02254

Abstract

High power transistors for pulsed power switching applications based on semiconductor-metal eutectic (SME) composites are described. Experimental devices with 6 kV blocking voltage have been demonstrated. The ability to parallel devices for higher currents has also been demonstrated. In addition, transient simulations and speed measurements have shown fast opening switch capacity with response times of less than 15 ns.

Introduction

Using conventional transistor technology for pulsed power switching would reqiure the development of devices with high on-state current and high blocking voltage. The main obstacle for devices to block voltages in excess of 1 kV is avalanche breakdown. Avalanche breakdown occurs when carriers overcoming the barrier at the gate gain sufficient energy when accelerated by the large electric field in the depletion zone to cause multiple ionization of bound charge carriers. The maximum breakdown voltage is determined by carrier concentration. A low carrier concentration is needed for high blocking voltage, which has an adverse effect on the on-state current. This breakdown mechanism together with basic junction physics limits conventional devices with reasonable size to high voltage or high current but not both.

Semiconductor-metal eutectic (SME) composites represent a new class of electronic materials which have a very unique microstructure. These materials contain arrays of micron-sized metallic rods imbedded in a single crystal semiconductor matrix. They are formed directly during the crystal growth process from the melt. The rods form parallel, cylindrical Schottky junctions with the semiconductor and provide the basis for novel electronic and opto-electronic devices, especially high power transistors. Performance exceeding that of conventional devices has been demonstrated in SME materials based on the Si-$TaSi_2$ system [1,2].

In this paper, state-of-the-art SME devices will be described and the effect of composite microstructure on the properties of the devices will be discussed. In addition, the speed measurements will also be presented.

Device fabrication and characteristics

The device geometry is shown in Fig 1. A standard concentric ring structure was used to fabricate transistors. A $CoSi_2$ film was used for all contacts. Ohmic contacts at the source and drain were formed with As^+ implants. Rectified gate contacts were formed with B^+ implant. More detailed information on processesing can be found elsewhere [3].

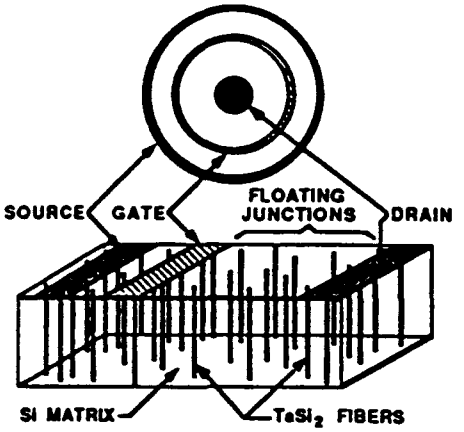


Fig. 1. SME transistor geometry.

Figure 2 shows a typical transfer characteristic of a SME device. The basic characteristics of the device are similar to those of a conventional MESFET in that they display a linear region and a saturation region. For high power applications, the resistance should be small, the saturation current should be large and the hold off voltage should be as high as possible.

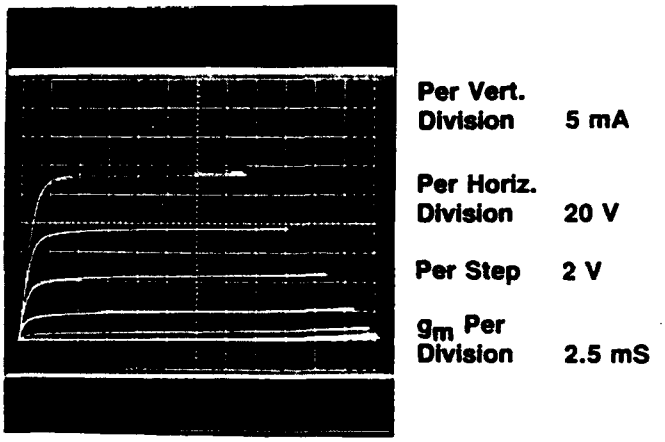


Fig. 2. Characteristics of a Si-$TaSi_2$ SME transistor.

Device properties and discussions

DC operation

Transfer characteristics of a SME transistor designed with the gate-drain distance of 500 μm are shown in Fig. 3. A blocking voltage of 2.2 kV was demonstrated. This high blocking voltage is remarkable when it is compared with the 0.3 kV maximum breakdown voltage expected for a conventional Si device with the same carrier concentration of 10^{15} cm^{-3} based on an avalanche

breakdown mechanism. The observed breakdown voltage of SME devices is unusual, in that it depends on two geometric factors, the gate-drain distance and the wafer thickness rather than on the carrier concentration as in conventional devices.

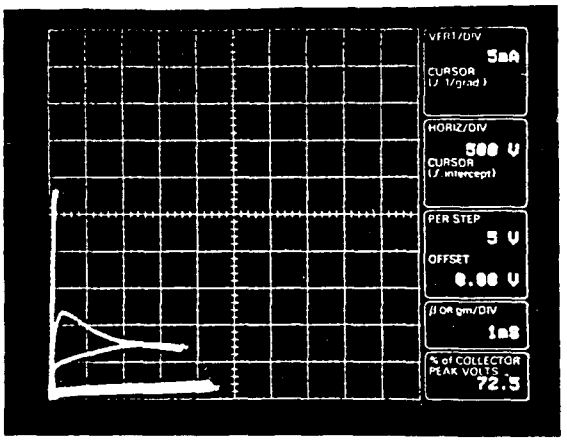


Fig. 3. Transfer characteristics of a 2.2 kV SME transistor.

Figure 4 shows how wafer thickness affects the blocking voltage in both dc and pulse tests. The pulse test results will be discussed in the next section. The graph shows typical data on devices from a wafer that was first tested at a 10 mil thickness, then reduced in thickness from the backside by chemical etching and retested. This was continued until wafer thickness was about 2 mils. The blocking voltages were found to dramatically increase with the decrease of wafer thickness. This dependence on wafer thickness has been related to misalignment of the metallic rods [3].

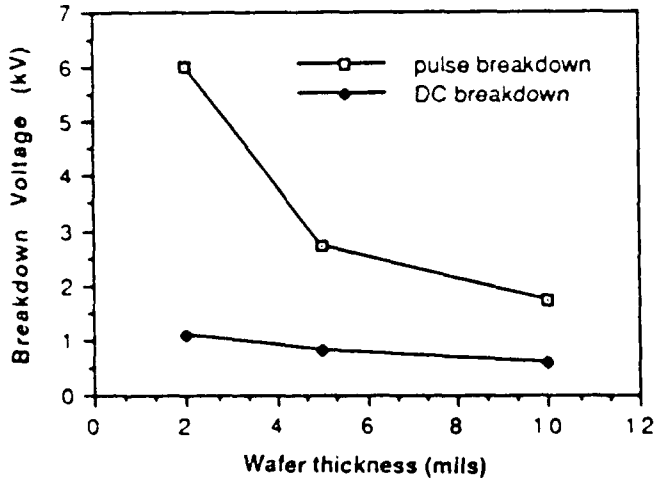


Fig. 4. Blocking voltage vs. wafer thickness for dc and pulse tests.

The saturation current in power devices is an important parameter since it reflects the maximum current switched in a given device. In SME devices, the concentric ring structure was used to optimize the blocking voltages rather than the saturation currents. To increase the saturation current, a new oval structure as shown in Fig. 5 was used to increase device area.

Fig. 5. Oval structure for high current devices.

The saturation current can be normalized in 2 ways. One approach is based on the wafer surface area occupied by the device. This gives surface current density, J_S. The other approach is based on the cross-sectional area for current flow. This gives cross-sectional current density, J_C. With the concentric ring structure, current flowing from large source ring to the small drain causes current crowding phenomena. An average cross-sectional area for current transport, A_C is given by

$$A_C = 2\pi t\,(r_{source} - r_{drain})/\ln(r_{source}/r_{drain}). \qquad (1)$$

In this equation, t is the wafer thickness, r_{source} is the inner diameter of the source contact and r_{drain} is the outer diameter of the drain. Using this cross-sectional area, a current density is attained, J_C, which is more indicative of the physical current density than J_S, and is a preferred parameter in comparing this device with other power devices. Sample data, covering several wafers and different device designs, is shown in Table 1. The uncertainty in the J_C is larger than in the J_S due to a subtantial uncertainty in the wafer thickness estimated to be 25%. Surface current densities range from 0.36 A/cm^2 to 1.2 A/cm^2 and cross-sectional current densities range from 15 to 26 A/cm^2.

Table 1. Sample data of various SME devices

Device	G-D (μm)	ρ (Ω-cm)	I_S (mA)	R_S (Ω)	J_S (A/cm^2)	J_C (A/cm^2)
85-5 N11	500	46	30	5000	1.27	26
85-29 N9	1000	31	25	1667	0.36	15
70-24 C16 (Oval)	500	17	77	172	0.98	19

The table shows that increasing the gate-drain distance to achieve high blocking voltage adversely affects the switchable current per unit surface area of the wafer but does not subtantially lower the cross-sectional current density. Although the surface current density may be considered low, the cross-sectional current density is high.

To boost the switching current of SME devices, devices can be connected in parallel. Fig. 6 shows the transfer characteristics of a device which is composed of 4 devices in parallel each with the saturation current shown in the insert. The saturation current of this parallel device is equivalent to 80% of the total saturation current of 4 individual devices. The loss may be due to the extra resistance introduced by the wire bonding process.

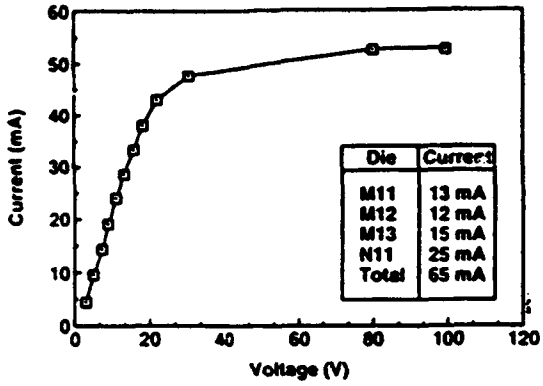


Fig. 6. Transfer characteristics of a parallel device.

This result indicates that the fabrication of large current switching devices, as well as high blocking voltage devices will be possible through the paralleling technique.

Table 1 also shows the series resistance for each device, calculated as the ratio of 50 mV with the drain current at 50 mV. This may be compared with the expected resistance based on the resistivity measured for the particular wafer and the effective cross-sectional and length of transport. When the comparison is made for these 2 mils thick devices, agreement is excellent, indicating that the contacts are good and that the entire wafer thickness is being utilized as the current channel.

Pulse operation

Pulse tests on SME devices were performed with the two circuits shown in Fig.7. The highest voltage pulses were generated with the spark coil circuit shown in Fig. 7a with either a 4 kV Xenon flash coil, which generated a 700 ns wide pulse, or a 25 kV automotive spark coil, which generated a longer 80 μs pulse. These tests were performed with the gate of the transistor shorted to the drain, so that maximum saturation currents flowed through the transistor during pulse testing.

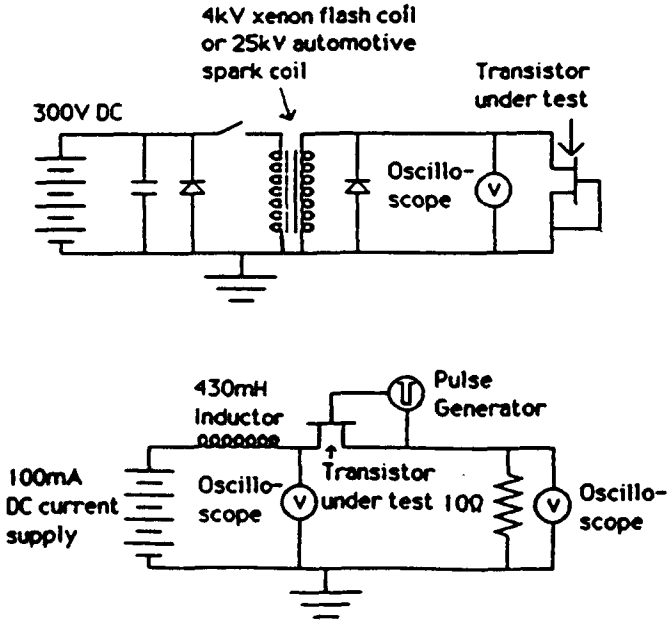


Fig. 7. (a) Spark coil circuit for high voltage pulse test and (b) Inductive circuit for high voltage and high current pulse tests.

An example of the voltage waveform with the automotive coil is shown in Fig. 8 as a 1000 μm gate-drain distance SME device is tested. The device is clearly demonstrated to support a full 6 kV. Above 6 kV the device breaks down, indicating that 6 kV for this device is the maximum blocking voltage. During high voltage testing, wafers were immersed in transformer oil. Without transformer oil arcing occurs and damages devices under test.

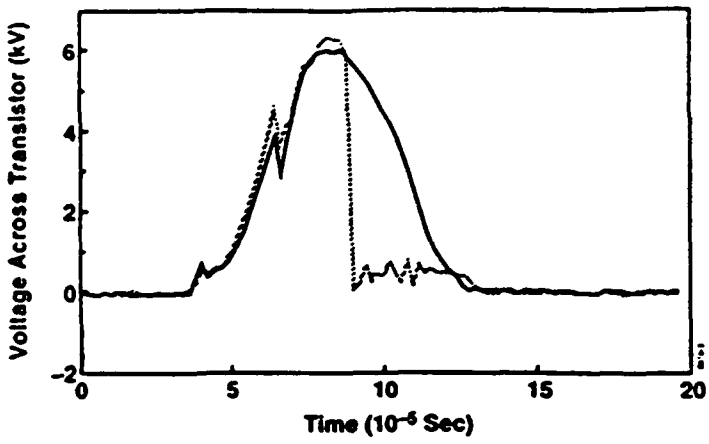


Fig. 8. Voltage waveforms of a SME transistor under pulsed test. The solid line shows a full 6 kV waveform supported by the device. Above 6 kV, device breaks down as shown by the dashed line.

The effect of wafer thickness on the breakdown voltage in pulsed tests is shown in Fig. 4. As in dc tests, the breakdown voltage increases as the thickness decreases.

In the pulsed tests described above, the SME transistor assumes a passive role, however, using the circuit in Fig. 7b, the high voltage pulses can be generated using the switching capability of the transistor itself. By passing a current through an inductor and test transistor connected in series, the magnetic field stored in the inductor is converted into a high voltage pulse at the drain of the transistor as the transistor is switched from the on-state to the off-state by the -10 V output of the pulse generator. The pulse generator has a 6 μs wide pulse and a 20 ns rise and fall time.

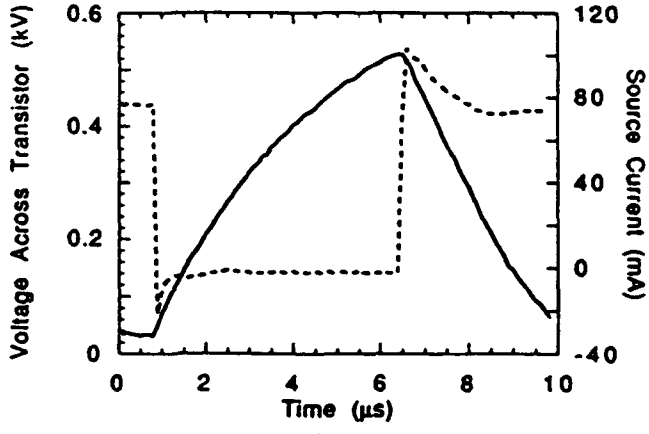


Fig. 9. The solid line is a voltage pulse generated with the inductive circuit using a SME transistor. The dashed line is a current pulse.

A voltage pulse generated with this circuit using a 10 mil thick SME transistor is shown in Fig. 9. The pulse generator results in the switching of 60 mA and the generation of a 0.5 kV pulse within 5 μs for the pulse. To measure current pulse, a 10 Ω resistor is connected in series to the source and the oscilloscope is set to track the voltage drop across the resistor as shown in Fig. 7b. The current waveform is also shown in Fig. 9 and an expansion of the time scale at the switch opening portion is shown in Fig. 10. The current drops from maximum to minimum value in approximately 15 ns. Therefore, the opening time of the switch has been shown to be 15 ns or less.

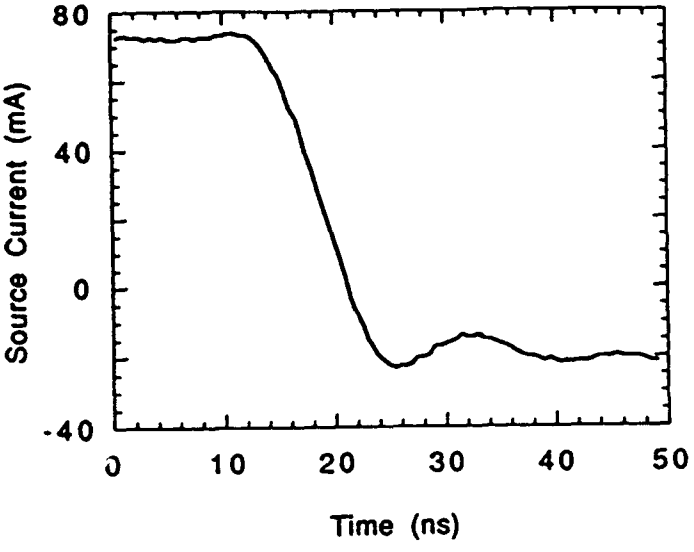


Fig. 10. Current waveform at switch opening portion in Fig. 9 with the time scale expansion.

Summary

Transistors fabricated from SME materials have been shown to possess properties suitable for pulsed power applications. Blocking voltage up to 6 kV, moderate current density up to 26 A/cm^2 and rapid opening times, less than 15 ns, have all been demonstrated. Based on these performance parameters, SME devices should take their place among other high power devices, including SITs, MOSFETs and Thyristors.

Acknowledgements

Technical assistance of Mr. T. Middleton in the crystal growth and device processing is greatly appreciated. This work was supported in part by the Strategic Defense Initiative Office/Innovative Science and Technology (SDIO/IST) and managed by the Office of Naval Research under contract N00014-86-C-0595.

References

1) B.M. Ditchek, T.R. Middleton, P.G. Rossoni and B.G. Yacobi, "Novel high voltage transistor fabricated using the in situ junctions in a Si-$TaSi_2$ eutectic composite", Appl. Phys. Lett. 52, 1147 (1988).

2) B.M. Ditchek and B.G. Yacobi, "Semiconductor-metal eutectic composites for high power switching", SPIE Space Structure, Power and Power Conditioning 871, 148 (1988).

3) B.M. Ditchek and B.G. Yacobi, "Microcharacterization and novel device applications of semiconductor-metal eutectic composites", Jpn. J. Appl. Phys. 27, L2155 (1988).

Proceedings of the

FOURTH SDIO/ONR PULSE POWER MEETING 1991

June 20–21, 1991

University of Southern California
Los Angeles, CA 90089-0484

PROGRESS IN THE DEVELOPMENT OF SEMICONDUCTOR-METAL EUTECTIC TRANSISTORS FOR HIGH POWER SWITCHING

M. Levinson, Q. V. Nguyen, P. G. Rossoni, and B. M. Ditchek

GTE Laboratories Incorporated
40 Sylvan Road, Waltham, MA 02254

Abstract — Semiconductor-metal eutectic composite transistors have the potential for very high hold-off voltages combined with low on-state resistance. We have performed computer simulations and experimental studies of the effects of composite microstructure on Si-$TaSi_2$ composite device performance. They show how microstructural control can lead to enhanced hold-off voltage and on-state conductance, and affect response speed. Improved composite microstructures were achieved by modifying crystal growth procedures.

I. INTRODUCTION

We have previously demonstrated a new class of high power transistors based on Si-$TaSi_2$ semiconductor-metal eutectic (SME) composite materials.[1-3] These devices are bulk field-effect transistors with the potential for very high voltage operation, due to the unique device physics afforded by the composite microstructure. The device geometry is shown in Fig. 1. Source-drain current flows between the cylindrical Schottky junctions formed by the metal fibers and the semiconductor. Application of a bias to the gate contact expands the depletion zones of the junctions accessed by the contact, pinching off the current channels and controlling the drain current.

The high voltage properties of these devices arise from the uncontacted junctions which lie between the gate and drain contacts. These junctions float in potential in a manner similar to guard rings and spread increasing drain potential over successively larger distances. With proper carrier concentration and interjunction spacing, avalanche breakdown is suppressed. Breakdown will eventually occur at the drain voltage where the gate depletion region reaches the drain contact. Therefore, the avalanche breakdown voltage is determined primarily by the gate-drain distance, rather than the carrier concentration as in conventional devices. It can, in principle, be made arbitrarily large, although in practice the maximum device hold-off voltage may be determined by external factors such as surface breakdown.

We have previously reported Si-$TaSi_2$ SME transistors with hold-off voltages of 1000 V, made with material of carrier concentration which would yield avalanche breakdown at a maximum of 300 V in conventional devices.[2,3] We have also demonstrated high quality Si epilayers grown on Si-$TaSi_2$ composite substrates, which should allow the integration of these devices with conventional

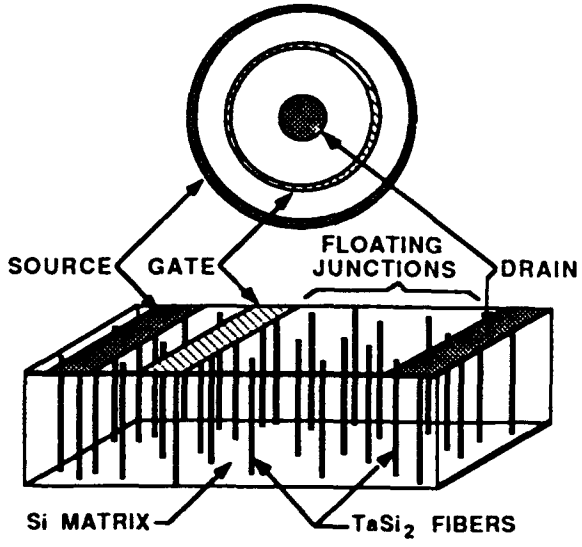


Fig. 1. SME transistor geometry.

Si circuitry.[4]

Here we describe computer simulations which show how composite microstructure could be optimized to simultaneously provide high hold-off voltage and low on-state resistance. A new electron microscopic technique was used to graphically observe the relationships between microstructure and electronic performance, including the effects of the floating junctions. We have also performed transient simulations and response speed measurements to identify factors affecting switching speed. Si-$TaSi_2$ material with improved microstructure was obtained by modifications of crystal growth procedures.

II. MICROSTRUCTURE OPTIMIZATION

In conventional high power semiconductor devices, maximum hold-off voltages are in general determined by avalanche breakdown. The breakdown voltage, V_B, is a greatest for planar junctions and is approximately inversely proportional to the carrier concentration. However, the on-state conductivity per unit junction area, σ_A, is also determined by the carrier concentration and the length of material needed to support the depletion zone at breakdown, with the result that $\sigma_A \propto 1/V_B^2$. Therefore, high voltage devices must have large cross-sectional area to achieve acceptably low on-state series resistance.

In SME devices, on the other hand, V_B is not directly determined by the carrier concentration, but rather is proportional to the gate drain distance. Increasing drain potential is spread over a continuously greater distance as the gate depletion zone expands towards the drain and "picks up" successive rows of floating junctions. This process may continue until the depletion zone reaches the drain contact where, with further voltage increases, avalanche will occur. In this case, $\sigma_A \propto 1/V_B$. Therefore, for a given microstructure, there exists a cross-over point in V_B above which the SME device can, in principle, have lower σ_A than any conventional transistor.[5]

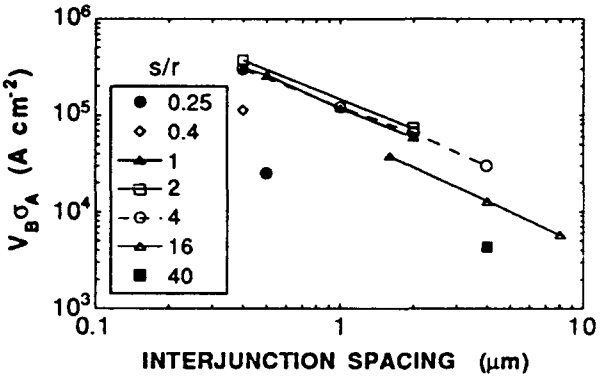


Fig. 2. Calculated $V_B\sigma_A$ vs. interjunction spacing, s, for various spacing/radius ratios.

In order to determine the effects of composite microstructural parameters on σ_A, simulations were performed using the PISCES-IIB code.[5,6] Cylindrical junctions of radius r were placed in a square array with interjunction spacing s. The primary criterion was to determine the maximum carrier concentration, N_D, that can be sustained without avalanche breakdown occurring. This condition corresponds to the N_D which yields a junction depletion zone width at avalanche just equal to s. In other words, as the drain bias, V_D, increases, the gate depletion zones expand, but just at the point where avalanche breakdown would occur, the depletion region intersects that of the next floating junction, which then floats in potential and takes on any succeeding increase in V_D.

Depletion widths at breakdown were calculated as a function of r and N_D using simulations of impact ionization in a cylindrical geometry. For a given r and s, N_D for a depletion width equal to s was used to simulate device I-V characteristics, from which σ_A was calculated. Because V_B is proportional to the gate-drain distance, and σ_A is inversely proportional, a useful figure of merit for comparing composite parameters which does not depend on distance is $V_B\sigma_A$. The results are shown in Fig. 2 as a function of s for a number of s/r ratios. For a constant r, performance improves with decreasing interjunction spacing, s, because higher N_D can be used without avalanche occurring, thus

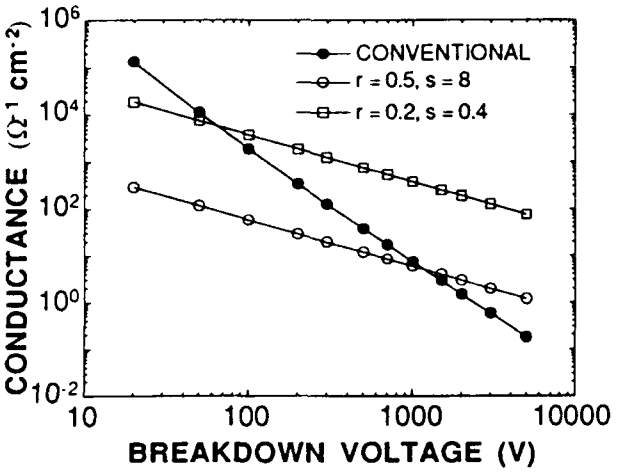


Fig. 3. Optimum areal conductance vs. breakdown voltage for conventional devices and SME devices with two combinations of junction radii and spacing.

lowering σ_A. The optimum s/r ratio is about 2:1. At lower values, σ_A is reduced by the smaller cross-sectional area of the current channels, while at higher values, a lower N_D is needed to prevent breakdown.

Fig. 3 compares the predicted optimum σ_A as a function of V_B for two sets of r and s values and for conventional semiconductor devices using planar junctions. For r = 0.5 μm and s = 8 μm, similar to existing Si-$TaSi_2$ composites, the optimum SME device will have higher conductivity than conventional devices for V_B in excess of ~1 kV. For example, σ_A should be greater by a factor of ~15 for V_B = 10 kV. However, devices made using a hypothetical denser composite with r = 0.2 μm and s = 0.4 μm could be superior to conventional ones for any V_B above ~ 50 V. In this case, σ_A could be up to ~50 times greater than in conventional devices for V_B = 1 kV and ~1000 times greater for V_B = 10 kV.

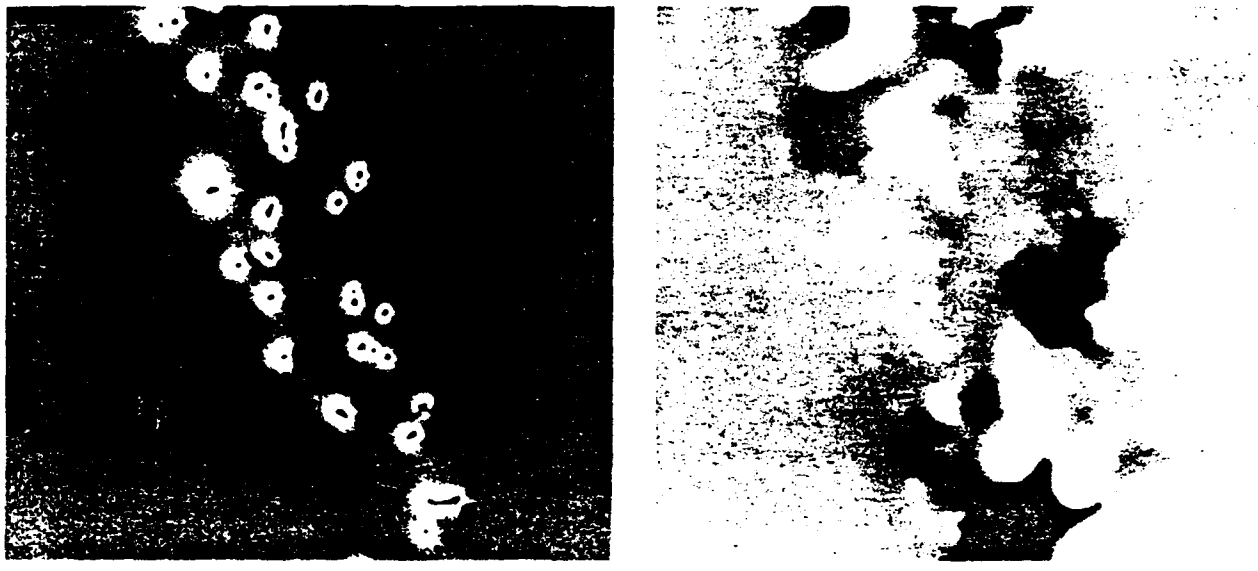
III. ELECTRONIC MICROCHARACTERIZATION

In addition to the effects of idealized SME microstructural parameters, real composites may have properties which vary on a microscopic scale because the active junctions are self-assembled during crystal growth and are not as uniform in size, shape, and spacing as those used in the simulation models. Previous studies showed that the spacing and arrangement of the $TaSi_2$ junctions in actual materials can have a large effect on current transport.[7,8] Therefore, the optimization of these devices will require a more detailed understanding of the relation between material microstructure and device electronic properties.

Recently, we devised a new three-terminal electron-beam-induced conductivity (TTEBIC) technique[9] which images the microscopic current characteristics of field-effect transistors during device operation and shows their relation to device structure. Image contrast is generated in the scanning electron microscope using variations of drain current which arise from electron-beam-induced perturbations of the electric fields within the device. In these images, darker contrast indicates areas where the drain current is constricted. The active areas of gate depletion zones are thus made visible and can be imaged at different points in the device I-V characteristic.

Fig. 4 shows a portion of the gate ring of an SME transistor. The electron beam is incident on the surface of the wafer opposite the contacts, and the drain is to the right of the image. Fig. 4(a) shows a conventional charge collection image of the ends of the $TaSi_2$ junctions which are accessed by the gate contact. The depletion zones appear as bright annuli around the fibers. In Fig. 4(b) at V_G = 0 V and V_D = 10 V, the dark areas of the TTEBIC image show those regions of the gate where the current is concentrated. It is seen that they are not uniformly distributed along the gate. They appear where the spacing between $TaSi_2$ junctions is greatest. These and other images show that non-uniformities of fiber distribution can result in delayed drain current saturation (the "knee" of the I-V curve occurring at higher V_D) and excess leakage current at pinch-off.[9]

Comparison of Figs. 4(a) and 4(b) also graphically shows the effect of the floating junctions. The right-hand dark regions are



(a) (b)

Fig. 4. (a) Conventional EBIC image of a portion of an SME transistor gate. (b) TTEBIC image of the same region showing the principle current channels.

seen to lie to the right of the junctions accessed by the gate contact. These current-limiting areas are therefore created by junctions which are floating, and they are supporting a portion of the drain potential.

IV. CRYSTAL GROWTH

The crystal growth process is a crucial factor in the performance of SME devices because they rely on the operation and interaction of multiple junctions which are self-assembled during growth. Although the growth rate determines the average $TaSi_2$ fiber density, and thus the average interjunction distance, the work described above highlights the need for good microstructural uniformity on both a macroscopic and microscopic scale. Such uniformity can only come from a detailed understanding and control of composite crystal growth.

We have made progress in uniformity control by studying the effects of crucible and seed rotation rates in the Czochralski crystal growth used for these materials. Fiber densities were determined by automated counting of the number of fibers ends visible in a sequence of 85 μm square frames along a diameter of polished wafers.

It was found that by eliminating rotation of the seed, smaller variations in the fiber density were obtained. A wafer from a portion of a

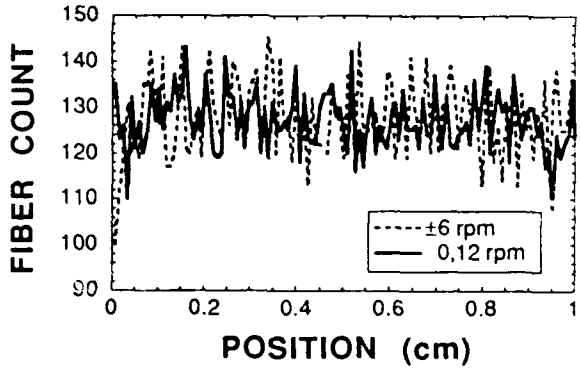


Fig. 5. Counts of $TaSi_2$ fibers in 85 μm square frames vs. position for two wafers grown with seed and crucible rotation of ±6 rpm and 0, 12 rpm.

a boule grown with no seed rotation and crucible rotation of 12 rpm exhibited a mean fiber count of 127.0 with a standard deviation of 6.85, compared to one grown with seed rotation of 6 rpm and crucible counterrotation of -6 rpm, which yielded a mean and standard deviation of 127.6 and 8.40, respectively. Fiber counts vs. position for the two wafers are shown in Fig. 5.

Although these measurements are on too large a scale to predict improvements in individual device performance by using material grown without seed rotation, they would at the least infer better device yield. Measurements of microscale uniformity in this material are in progress.

V. TRANSIENT RESPONSE

The response speed of SME transistors will be affected by transit time delay and parasitic capacitance and resistance in the same way as conventional FET's. But a major question is how, if at all, these properties will be affected by the floating junctions. The floating junctions in SME transistors create a depletion region whose length varies greatly between the on-state, where it is simply the length of the gate contact region, and the off-state, where it extends over a large portion of the gate-drain distance and depends on V_D. Therefore, it is expected that the transit time would differ between the turn-on (closing switch) and turn-off (opening switch) processes.

When the device is in the process of turning off, carriers which have passed through the gate contact depletion region will not contribute further to transit delays because their motion will be accompanied by current in the drain contact. Therefore, the turn-off process should not be greatly affected by the floating gates, but should be governed by parasitic capacitance and resistance as in conventional metal-semiconductor FET's.

During the turn-on process, on the other hand, the first carriers to transit the gate region must pass through the extended depletion zone before they can force current at the drain. The transit time will decrease significantly as the depletion region collapses back toward the gate contact. The rate of this collapse will be determined by the gate-source and gate-drain capacitances. Thus the turn-on transient may be slower than that of turn-off, with a time constant that would increase with increasing V_D.

There is an additional phenomenon that may affect the turn-on response of floating junction devices. It is commonly observed in devices using guard rings.[10] The floating junctions exchange charge with the bulk semiconductor as their potential shifts. During the turn-off process, they float towards the drain potential and lose charge by a majority carrier current to the drain. During turn-on, however, the opposite charging process must occur by minority carrier current or leakage and is relatively slow. During this time, the depletion zones of the floating junctions are larger than when they are neutral, thus constricting the current channel and producing a long time-constant tail to the drain current during turn-on.

PISCES simulations of SME transistor transient behavior illustrate this effect. Fig. 6 shows the calculated turn-on response of a model device for V_D = 50, 200, and 300 V. A constant value of load resistance was used, so that the on-state operating point is moving up the *I-V* curve with increasing V_D. At V_D = 50 V, the device is in the linear region in the on-state, so the gate depletion zones are not greatly

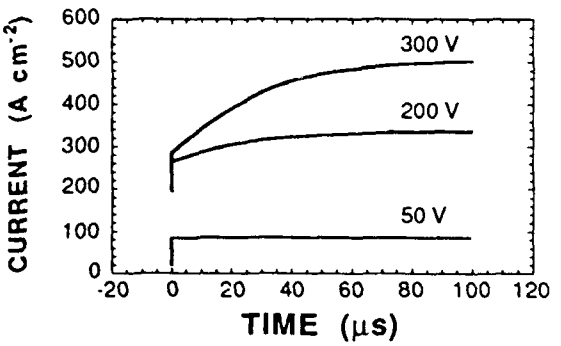


Fig. 6. Simulated SME transistor turn-on response for different V_D.

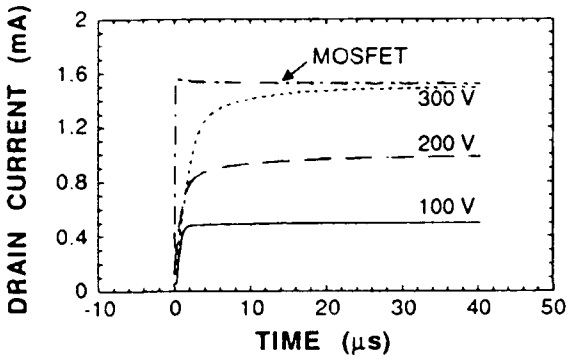


Fig. 7. Measured turn-on response of a Si-$TaSi_2$ transistor for different V_D. Conventional power MOSFET shown for comparison.

extended, and the floating junctions are neutral. However, at V_D = 200 and 300 V, the drain current is saturating and the floating junctions are active. Slow tails in these transients are seen whose magnitudes increase with V_D.

Experimental turn-on transients are shown in Fig. 7 for a Si-$TaSi_2$ device at V_D = 100, 200, and 300 V, again with a constant load resistor. A conventional power MOSFET is shown for comparison. The data show slow tails of increasing magnitude with increasing V_D, in agreement with model predictions. However, the time constants are faster than expected. This is likely due to larger than ideal reverse leakage current in the floating junctions of the actual device.

On the other hand, as expected, PISCES simulations showed much faster turn-off characteristics, on the order of a few hundred ps, although the very small simulation geometry leads to small capacitances. Measurements of the device shown in Fig. 7 revealed a turn-off transient of 20 ns, which is limited by the speed of the test circuit.

VI. CONCLUSIONS

The above work shows that SME transistors have the potential to simultaneously provide very high blocking voltages and low on-state resistance. As opening switches, they should be capable of very fast response speeds, although charging effects in the floating junctions which enable their high voltage performance can limit turn-on response in closing switch applications. We have also shown the importance of microstructural uniformity for the achievement of optimum device properties, and how higher junction density could lead to even lower on-state resistance while maintaining high blocking voltages. Improved composite microstructures will require better crystal growth methods, and we have made some progress by optimization of the seed and crucible rotation rates.

ACKNOWLEDGEMENTS

The assistance of J. Hefter and T. Middleton is gratefully acknowledged. This work was supported in part by the Strategic Defense Initiative Office/Innovative Science and Technology (SDIO/IST) and managed by the Office of Naval Research under contract N00014-86-C-0595.

REFERENCES

[1] B. M. Ditchek, T. R. Middleton, P. G. Rossoni, and B. G. Yacobi, "Novel high voltage transistor fabricated using the *in situ* junctions in a Si-$TaSi_2$ eutectic composite," Appl. Phys. Lett. **52**, 1147 (1988).

[2] M. Levinson, P. G. Rossoni, F. Rock, and B. M. Ditchek, "High voltage floating gate array transistors," Electron. Lett. **26**, 777 (1990).

[3] M. Levinson, P. G. Rossoni, W. Byszewski, and B. M. Ditchek, "High Voltage Bulk MESFET Using *In-Situ* Junctions," *Proc. 1990 Nineteenth Power Modulator Symposium, San Diego, CA*, (IEEE, New York, 1990), 347.

[4] M. Levinson, M. Tabasky, C. Sung, G. Hamill, D. H. Matthiesen, K. Ostreicher, and B. M. Ditchek, "Silicon Epitaxial Growth on Si-$TaSi_2$ Eutectic Composite Substrates," Appl. Phys. Lett., in press.

[5] P. G. Rossoni, M. Levinson, and B. M. Ditchek, "Floating junction effects in semiconductor-metal eutectic transistors," J. Appl. Phys., in press.
[6] PISCES-IIB, Stanford Electronics Laboratories, Stanford, CA
[7] B. M. Ditchek, B. G. Yacobi, and M. Levinson, "Depletion zone limited transport in Si-$TaSi_2$ eutectic composites," J. Appl. Phys. **63**, 1964 (1988).
[8] V. K. Samalam, " Si-$TaSi_2$ eutectic composites as an example of a percolation system," J. Appl. Phys. **67**, 2165 (1990).
[9] M. Levinson, P. G. Rossoni, and B. M. Ditchek, "Electrical microcharacterization of semiconductor-metal eutectic transistors by three-terminal electron-beam-induced-conductivity," J. Appl Phys., in press
[10] M. K. Johnson, A. D. Annis, J. N. Sandoe, and D. Coe, "An analysis of the dynamic behavior of field-limiting ring-passivation systems," IEEE Trans. Electron Dev. **36**, 1203 (1989).

M. Levinson, photograph and biography not available at the time of publication.

Q. V. Nguyen, photograph and biography not available at the time of publication.

P. G. Rossoni, photograph and biography not available at the time of publication.

B. M. Ditchek, photograph and biography not available at the time of publication.

Floating gate effects in high-power semiconductor-metal eutectic composite transistors

P. G. Rossoni, M. Levinson, and B. M. Ditchek
GTE Laboratories Incorporated, 40 Sylvan Road, Waltham, Massachusetts 02254

(Received 11 February 1991; accepted for publication 24 May 1991)

Novel field-effect transistors (FETs) with unusual high-power capabilities have been demonstrated previously. They are fabricated using the grown-in metal-semiconductor junctions of semiconductor-metal eutectic composite materials. Here, computer modeling has been used to examine the relation between their exceptional resistance to avalanche breakdown and the effects of floating gate junctions between the gate and drain. Calculations are presented that show how composite geometry and materials parameters could be optimized to give extremely large off-state blocking voltages combined with low series resistance. These transistors should, in principle, be capable of an on-state power dissipation lower than that of any conventional high-voltage FET device.

I. INTRODUCTION

We have recently demonstrated Si-$TaSi_2$ semiconductor-metal eutectic (SME) transistors with the ability to block voltages up to three times higher than those expected for conventional planar devices of similar carrier concentration.[1,2] They are fabricated using the grown-in Schottky junctions of directionally solidified Si-$TaSi_2$ eutectic composite materials, which contain arrays of rod-shaped, metallic $TaSi_2$ fibers in a single-crystal Si matrix. This structure is formed during crystal growth from the melt.[3]

The transistor, made using a wafer cut perpendicular to the $TaSi_2$ rods, is shown schematically in Fig. 1. Current flowing between the Ohmic source and drain contacts passes between the rods. A gate is formed by those rods that are accessed by the gate contact. The gate contact consists of a $CoSi_2$ layer that provides a metallic contact to the $TaSi_2$ rods, but maintains a rectifying contact to the silicon matrix. The depletion zones of the rod junctions expand with the application of a reverse bias to limit the current channels and provide transistor action.[1,4]

Since the $TaSi_2$ rods are found throughout the material, junctions appear not only under the gate contact but also in the regions between the contacts (Fig. 1). Previous computer modeling has demonstrated that the outstanding high-voltage properties of these devices result from the uncontacted junctions between the gate and drain.[2] These floating gates function in a manner similar to field-limiting rings (guard rings),[5,6] allowing the gate electric fields to be distributed over the gate-drain distance and postponing avalanche breakdown. The $TaSi_2$ rods also affect current transport properties via reduction of effective cross-sectional area and behavior of their associated depletion zones.[4]

Here, we have used model calculations to explore in detail the effects of device parameters such as rod diameter, inter-rod spacing, and carrier concentration on the action of these floating gates and the overall high-power performance of SME transistors. We show how these parameters could be optimized to simultaneously achieve large off-state blocking voltages and low on-state series resistance. A theoretical comparison of SME transistors with conventional ones shows that SME transistors could, in principle, provide high-power performance superior to any conventional field-effect transistors (FET). These results are qualitatively similar to model calculations that demonstrated the advantages of floating gates in GaAs metal-semiconductor (MES) FET devices.[7]

II. MODEL

Computer simulations were performed using PISCES IIB software.[8] It models two-dimensional distributions of potential, electric field, and carrier concentrations for arbitrary device geometries and bias conditions. Geometries were used that resemble those of experimental Si-$TaSi_2$ composite transistors. Materials parameters for n-type silicon with uniform dopant concentrations $N_D = 1 \times 10^{14}$–1.1×10^{17} cm^{-3} were used, and junction rods were specified as Schottky contacts with a barrier height of 0.6 eV.

Avalanche breakdown behavior was examined by using the PISCES impact ionization simulator. It was found that the breakdown voltages V_B (defined as the voltage where the reverse current reaches twice the reverse saturation value) of cylindrical junctions were about 20% larger than the values of Sze and Gibbons.[9]

For each set of device parameters, transistor I-V characteristics were calculated. Characteristics typical of field-effect transistors were obtained, with an initial linear portion of the curve followed by saturation at higher drain voltages V_D. Series resistance in the on-state R_s was calculated from the slope of the linear region.

In Sec. III, we describe the effects of composite parameters on V_B. In Sec. IV, the results of Sec. III are used to explore the ways device parameters could be optimized to yield the highest conductance for a given V_B. In Sec. V, SME devices are compared with conventional FETs.

III. AVALANCHE BREAKDOWN EFFECTS

The effects on avalanche breakdown of variation in interrod spacing s and N_D were examined using simulation

 0021-8979/91/052861-05$03.00

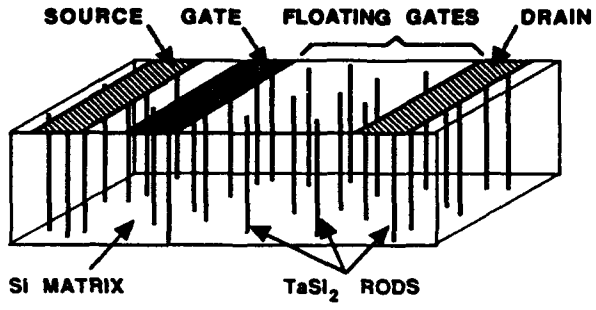
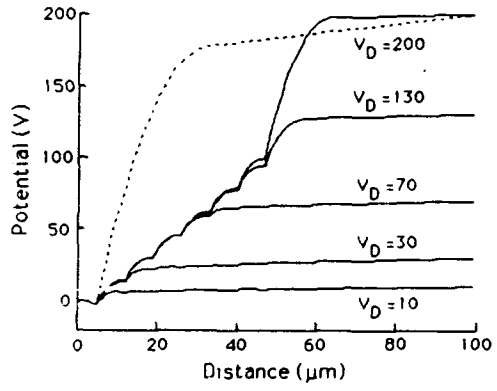


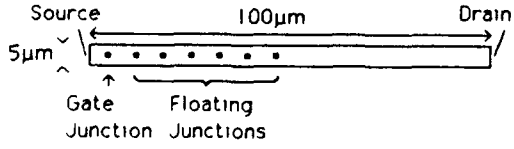
FIG. 1. Schematic diagram of the semiconductor-metal eutectic composite transistor.

geometries representing a $100 \times 5\text{-}\mu m^2$, 1-$\mu$m-thick section of SME transistor. Each contained a contacted gate rod followed by six floating gate rods [Fig. 2(b)]. The maximum allowable nine electrodes included two Ohmic source and drain contacts and seven rectifying contacts for the gate and floating gate rods. Floating rods were simulated by inserting the highest allowable lumped resistance (10^{31} Ω) biasing to the drain.

To minimize computation time, fixed-dimension square cross-section rods of 1 μm on a side were used. Calculations using a finer grid to explicitly include the effects of junction curvature showed that the square rods gave results very similar to those of round rods with a diameter equal to the dimension of the square, presumably because values calculated using the coarse grid of the square rods were averaged over the grid cell, thus reducing the effects of sharp corners. However, these calculations were not intended to predict precise breakdown voltages, but rather to compare the effects of variations in array parameters. More accurate calculations explicitly including rod radius were used in Sec. IV.



(a)



(b)

FIG. 2. (a) Potential vs distance for different V_D. The dashed line represents the case without floating gates for $V_D = 200$ V. (b) Simulation geometry: $50 \times 9\text{-}\mu m^2$, 1-$\mu$m-thick slice with 1-$\mu m^2$ square rods comprising one contacted control gate and six floating gates.

The field-limiting effects of the floating rods can be seen for several values of V_D in the potential distributions shown in Fig. 2(a). For comparison, the case without floating junctions is included for $V_D = 200$. Here, $N_D = 5 \times 10^{14}$ cm^{-3}, the junction spacings s are 8 μm (for the cases with floating junctions), the source was held at 0 V, and the contacted gate was biased to -2 V. At $V_D < \sim 20$ V all the potential is dropped across the gate-rod depletion zone. However, as V_D is increased, the gate depletion zone intersects that of the first floating rod, and the potential distribution and maximum electric-field magnitude E_{max} at the gate rod become clamped. Further potential increases are dropped at the first floating gate until its depletion zone punches through to the next floating gate and its potential distribution is clamped. This process continues until the depletion region expands beyond the last floating gate. Further voltage increases are dropped at the last gate, as no more floating gates are available.

If the rod geometry, spacing, and N_D are such that depletion zone punch through to the next floating rod occurs before avalanche breakdown, then breakdown will be suppressed. The drain potential, which would be dropped entirely at the gate in a conventional device, is distributed over the floating junction array as V_D is increased. Breakdown will eventually occur when the depletion zone expands past the last floating gate, or when it reaches the drain contact. As a result, total V_B will be determined only by the length of the floating junction array, and not by N_D and gate geometry as in conventional devices. In SME transistors the array length is equal to the gate-drain distance.

Simulations where N_D and s were varied yielded results that are consistent with the depletion zone punch-through mechanism described above. With increased N_D for a fixed s, a larger voltage is required before punch through occurs. Therefore, the values at which the voltage drop and maximum electric field E_{max} are clamped also increase. Similarly, larger s for fixed N_D also results in a higher punch-through voltage, and thus larger clamped values of voltage drop and E_{max}.

To test the validity of linear rod layouts as applied to the semirandom distribution of experimental SME transistors, a comparison was made between a staggered rod layout, where the rods were alternated between the two sides of the simulation grid, and a linear rod configuration. The staggering of junctions resulted in increased clamping fields, as expected from the larger inter-rod distances. The saturation current and R_s for both layouts were not appreciably different.

Data derived from these simulations predict that in experimental SME transistors made from Si-$TaSi_2$ eutectic composites with $\sim$1-μm-diam $TaSi_2$ rods spaced an average of 8 μm apart (although with a quasirandom distribution) and $N_D = 1\text{–}3 \times 10^{15}$ cm^{-3}, the floating gate rods

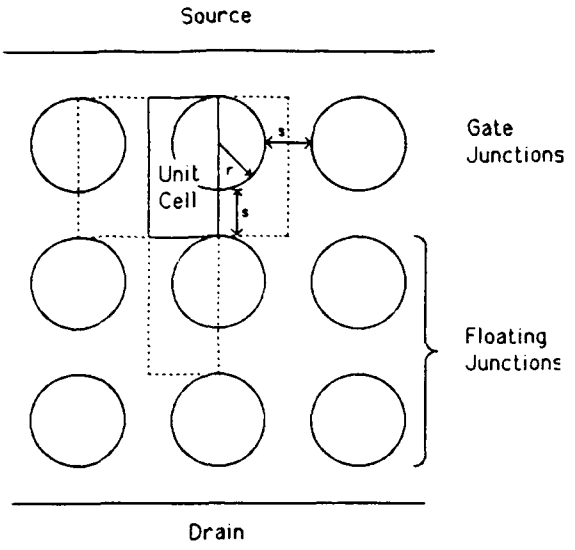


FIG. 3. Simulation geometry with a square array of rods of radius r and inter-rod spacing s.

should clamp E_{max} at a value less than that required for avalanche breakdown. The maximum voltage supported by the floating gates should be $\sim 5\times 10^4$ V/cm of gate-drain distance. Both these predictions are in good agreement with experimental results.[1,2]

IV. OPTIMIZED POWER SWITCHING CAPABILITIES

In this section we investigate the ways in which the floating gate array parameters can be optimized to simultaneously suppress breakdown and yield high on-state conductance. The primary requirement is that the gate depletion zone must reach the first floating junction before avalanche breakdown occurs. Thus, the maximum permissible N_D is determined by the condition that the depletion width at the point where avalanche breakdown would occur is just equal to s. Higher N_D will lead to avalanche breakdown before the field-limiting capabilities of the floating gates can take effect. Lower N_D will result in a lower voltage drop per unit distance, and therefore a larger array length for the same total V_B, and lower conductance.

In these calculations, round rods of radius r were used in a square array with spacing between rods s as shown in Fig. 3. In each case, a sufficiently fine grid to accurately represent the round rod cross sections was used. For a given r and s, the N_D that just yields breakdown when the depletion width is equal to s was determined analytically, as was the corresponding breakdown voltage per unit cell V_B^C. The maximum voltage drop per unit length V_L, was calculated as V_B^C/L_c, where $L_c = 2r + s$ is the unit-cell length. The total breakdown voltage of the device can be determined as $V_B = V_L L$, where L is the array length. The I-V characteristic was then simulated and the volume conductivity, $\sigma_v = L_c/R_s\ A$, was calculated where R_s is the series resistance in the on state found from the slope of the linear region and A is the cross-sectional area of the simulation geometry. The results are summarized in Table I. The conductance per unit cross-sectional area, $\sigma_A = \sigma_V/L_c = 1/R_s\ A$, was also calculated.

It may be noted that these results appear to be conservative because the maximum N_D for the case of 0.5-μm radius and 8-μm spacing is predicted to be 6×10^{14} cm^{-3}, although avalanche suppression was observed in experimental SME devices with approximately this geometry and $N_D \approx 1$–3×10^{15} cm^{-3} (Ref. 2).

Because V_B is proportional to L, arbitrarily large V_B can, in principle, be obtained with a sufficiently long array, although in practice it may be limited by external factors such as surface breakdown. However, σ_A is inversely proportional to array length. For the purposes of comparing floating gate array parameters, a figure of merit that is independent of array length can be defined as $V_L\sigma_V = V_B\ \sigma_A$. The higher this value, the higher the on-state conductance, and the lower the series resistance, for a device of a given V_B.

TABLE I. Calculated optimum carrier concentration N_D, breakdown voltage per unit length V_L, series conductivity σ_v, and $V_L\sigma_v$ for various combinations of rod radius r and spacing s.

r (μm)	s (μm)	s/r	N_D ($\times 10^{15}$ cm^{-3})	V_L ($\times 10^4$ V/cm)	σ_v (Ω cm)$^{-1}$	$V_L\sigma_v$ ($\times 10^4$ A/cm^2)
2.0	0.5	0.25	83	3.6	0.69	2.5
1.0	0.4	0.40	110	5.9	1.93	11
0.4	0.4	1.0	93	11	2.65	30
0.5	0.5	1.0	68	10	2.48	26
1.0	1.0	1.0	29	9.1	1.30	12
2.0	2.0	1.0	13	8.1	0.73	5.9
0.2	0.4	2.0	73	16	2.40	37
1.0	2.0	2.0	10	11	0.65	7.3
0.1	0.4	4.0	53	18	1.68	30
0.25	1.0	4.0	17	15	0.82	12
0.5	2.0	4.0	7.4	13	0.51	6.6
1.0	4.0	4.0	3.2	11	0.26	3.0
0.1	1.6	16.0	4.2	11	0.33	3.7
0.25	4.0	16.0	1.4	9.8	0.13	1.3
0.5	8.0	16.0	0.63	8.8	0.07	0.57
0.1	4.0	32.0	0.7	6.6	0.07	0.43

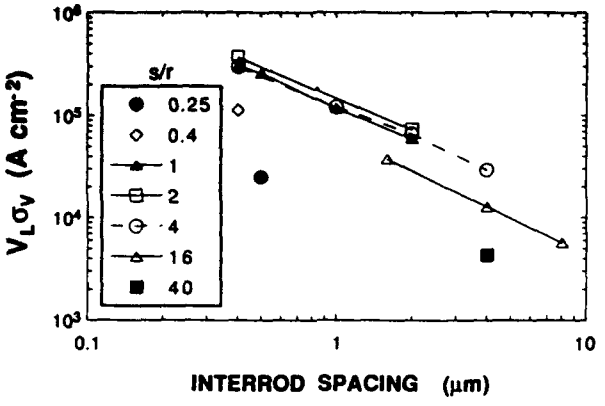


FIG. 4. $V_L\sigma_v$ vs inter-rod spacing s for different s/r ratios.

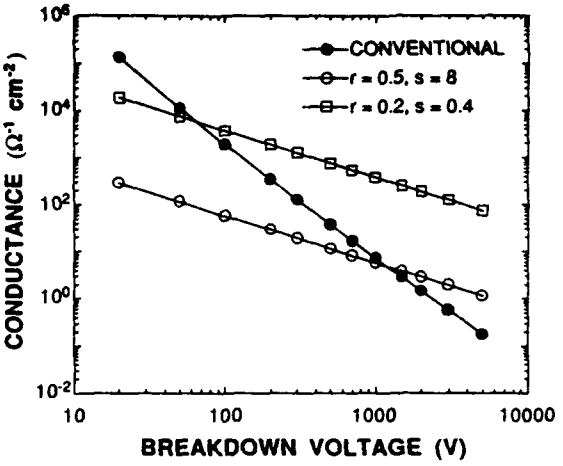


FIG. 5. σ_A vs V_B for optimal conventional semiconductor devices and two SME composites: $r = 0.5$ μm, $s = 8$ μm; $r = 0.2$ μm, $s = 0.4$ μm.

Values of $V_L\sigma_v$ are given in Table I. In Fig. 4 they are shown as a function of s for all sets of r and s values used and are grouped according to s/r ratio. It is seen that $V_L\sigma_v$ is approximately inversely proportional to s, for constant s/r. This relationship arises because, as the spacing between rods is made smaller, the required depletion width at breakdown is also decreased, so the optimum N_D increases, as does σ_v. The fraction of cross-sectional area of undepleted semiconductor between the rods where the current flows, equal to $s/(2r+s)$, remains approximately constant.

It is also seen from Fig. 4 that the optimum s/r ratio lies between 1 and 4, with a slight maximum at 2. This latter value occurs where the rod diameter $2r$ is equal to the spacing s. σ_v decreases with higher values of s/r because lower N_D is needed to accommodate the increased interrod spacing. σ_v also decreases with lower s/r because the cross-sectional area taken by the undepleted semiconductor is reduced relative to that of the rods and their associated depletion zones.

The condition that the gate depletion zone reach the first floating junction just before avalanche breakdown does not adversely affect the gate bias necessary to deplete the semiconductor region between the gate rods. The depletion zone need only extend half way into the gate channel since a mirror image depletion zone extends from the neighboring gate rod (see Fig. 3). For example, the optimized geometry shown in Fig. 5 with $r=0.2$ μm and $s = 0.4$ μm pinches off at a gate bias of -3V for $V_{SD} = 10$ V (by comparison $V_B^C = -8$ V).

The condition of constant s/r corresponds to that found in directionally solidified eutectic composite materials. The two phases have constant volume fractions, and the rod spacing and radius are determined by the crystal-growth parameters. Although real eutectic systems have irregular distributions of the rods rather than a square array, these calculations should give a good approximation of their properties. These results predict that, for a given eutectic system, smaller rod spacing will give improved transistor performance. Furthermore, the optimum eutectic will have average s/r between 1 and 4, and therefore the volume fraction of the metal phase, equal to $\pi r^2/(2r+s)^2$, in the range ~9%–35% (assuming that the desired rod structure can be achieved). For comparison, the existing Si-$TaSi_2$ materials have about 2 vol % $TaSi_2$, corresponding to an s/r value of 16, and the smallest rod spacing achieved is 8 μm.

V. COMPARISON TO CONVENTIONAL SEMICONDUCTOR DEVICES

In conventional FET devices, the optimum σ_A for planar junctions is inversely proportional to the square of V_B,[10] neglecting the small variations of avalanche field and mobility with N_D. However, in SME devices σ_A is inversely proportional to V_B, rather than its square. Therefore, for a given SME material σ_A can be greater than any conventional FET for V_B greater than a certain value. Calculated values demonstrating these relationships are shown in Fig. 5 for two SME materials. It is seen that existing Si-$TaSi_2$ devices, where $s = \sim 8$ μm and $s/r \approx 16$, should be capable of outperforming any conventional FET for $V_B > \sim 1000$ V. SME transistors have successfully blocked voltages in excess of 1000 V with carrier concentrations of 1×10^{15} cm^{-3}. Optimized SME transistors with $s = 0.2$ μm and $s/r \approx 2.0$ should yield higher σ_A than conventional devices when $V_B > \sim 50$ V.

The suppression of avalanche breakdown using floating junctions could also be applied to bipolar devices. For example, the maximum blocking voltage of a thyristor is determined by avalanche breakdown of the anode-gate junction. By fabricating such devices with floating junctions in the intergate region, the advantages of higher σ_A and/or V_B could also be achieved.

VI. SUMMARY

The field-limiting effects of floating junction arrays, believed to be responsible for the Si-$TaSi_2$ eutectic composite transistor's ability to block unusually high voltages, have been investigated via computer modeling. The clamping fields and voltage drop per unit length were shown to vary as expected, increasing with increasing carrier con-

centration and inter-rod spacing. It was shown that for floating junction arrays, the product of maximum blocking voltage and on-state conductivity is constant for a given rod radius and inter-rod spacing. Optimum values of this product were determined as a function of rod radius and inter-rod spacing. It was found that this product increases with decreasing inter-rod spacing, and for a given spacing, the highest values are achieved with the rod diameter within a factor of 2 of the inter-rod spacing, corresponding to a rod volume fraction of ~9%–35%. It was further shown that, for a given set of array parameters and desired maximum blocking voltage, the SME transistor could, in principle, provide higher conductivity than any conventional FET device.

ACKNOWLEDGMENTS

This work was sponsored in part by the Strategic Defense Initiative Office/Innovative Science and Technology (SDIO/IST) and managed by the Office of Naval Research under contract No. N00014-86-C-0595.

[1] B. M. Ditchek, T. R. Middleton, P. G. Rossoni, and B. G. Yacobi, Appl. Phys. Lett. **52**, 1147 (1988).
[2] M. Levinson, P. G. Rossoni, F. C. Rock, and B. M. Ditchek, Electron. Lett. **26**, 777 (1990).
[3] B. M. Ditchek, J. Hefter, T. R. Middleton, and J. Pelleg, J. Cryst. Growth **102**, 401 (1990).
[4] B. M. Ditchek, B. G. Yacobi, and M. Levinson, J. Appl. Phys. **63**, 1964 (1988).
[5] Y. C. Kao and E. D. Wolley, Proc. IEEE **55**, 1409 (1967).
[6] M. S. Adler, V. A. K. Temple, A. P. Ferro, and R. C. Rustay, IEEE Trans. Electron Devices **ED-24**, 107 (1977).
[7] M. Levinson, P. G. Rossoni, S. Butler, and B. M. Ditchek (unpublished).
[8] Stanford Electronics Laboratories, Stanford, CA.
[9] S. M. Sze and G. Gibbons, Solid-State Electron. **9**, 831 (1966).
[10] See, for example, K. Shenai, R. S. Scott, and B. Jayant Baliga, IEEE Trans. Electron Devices **ED-36**, 1811 (1989).

IEEE
Conference Record of the

1990 Nineteenth Power Modulator Symposium

sponsored by
Naval Surface Warfare Center
U.S. Army LABCOM, ET&DL
Air Force Wright Research and Development Center
Air Force Weapons Laboratory
The Electron Devices Society of
The Institute of Electrical and
Electronics Engineers, Inc.

in cooperation with
The Advisory Group on Electron Devices

and under the management of
Palisades Institute for Research Services, Inc.

Library of Congress Catalog Card No.: 89-82657

Available from
IEEE Single Copy Sales
445 Hoes Lane
Piscataway, NJ 08854

Printed in USA

A HIGH VOLTAGE BULK MESFET USING *IN-SITU* JUNCTIONS

M. Levinson, P. G. Rossoni, W. W. Byszewski, and B. M. Ditchek
GTE Laboratories Incorporated, Waltham, MA 02254

Abstract

A new bulk MESFET based on semiconductor-metal eutectic composite materials is described and its application to pulsed power switching is discussed. Numerical modeling of these transistors has shown that it should be possible to design them to hold off very large voltages, and device and materials parameters which should optimize their performance have been identified. Experimental Si-$TaSi_2$ SME devices have shown breakdown voltages more than three times that expected for conventional semiconductor junctions of the same carrier concentration, in agreement with the model.

Introduction

Extension of conventional transistor technology to the pulsed power conditioning regime would require the development of devices with "on-state" currents in excess of 1 kA and blocking voltages of 50 kV. The main obstacle to engineering such high power devices is the existence of avalanche breakdown. It is this breakdown mechanism, together with basic junction physics, that limits conventional devices of reasonable size to either high voltage or high current but not both.

This paper discusses a new class of transistors that should allow the attainment of both high voltage and high current in a single opening switch. They are based on the unique microstructure of a new kind of electronic material: semiconductor-metal eutectic (SME) composites. These materials contain arrays of rod-shaped metallic regions imbedded in a single crystal semiconductor matrix. They are formed directly during crystal growth from the melt. The rods form parallel, cylindrical Schottky junctions which fill the bulk of the material and provide the basis for a number of novel devices [1-6], including the transistors considered here.

Field-effect transistors can be fabricated with these materials which take advantage of their unusual properties to overcome the limitations imposed by avalanche breakdown in conventional devices. We describe numerical modeling which reveals in detail the physics underlying these avalanche-inhibiting effects and shows that these devices could, in principle, be designed to hold off arbitrarily large voltages, limited only by external factors such as surface breakdown. Experimental results using Si-$TaSi_2$ composite devices are then presented which are in good agreement with the model calculations. This approach should lead to the development of devices which are capable of both high voltage and high current in a single switch.

Device modeling

The semiconductor-metal eutectic transistor geometry [2] is shown schematically in Fig. 1(a). The metal rods, arrayed perpendicularly to the wafer surface, create rectifying Schottky junctions with the semiconductor. A gate contact, which provides a metallic contact to the rods but maintains a Schottky contact to the semiconductor, is formed between the ohmic source and drain contacts. Current flowing from the source to the drain passes between the depletion zones surrounding the gate rods. An external gate voltage can be used to expand the depletion zones of the rods accessed by the gate contact and, by decreasing the volume of non-depleted

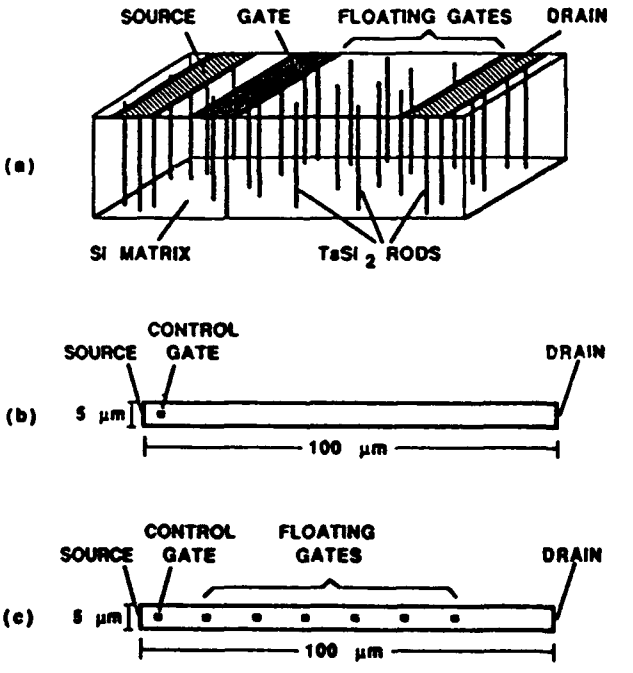


Fig. 1. a) Semiconductor-metal eutectic transistor geometry; geometries for PISCES simulations: b) no floating rods; c) six floating rods.

semiconductor, reduce the source-drain current to provide transistor action.

One unique feature of this device is that the rods which lie in between the gate and drain contacts are not contacted and are therefore isolated from the external circuit. These junctions float in potential in such a way as to spread the applied drain voltage over a greater distance than the width of a single junction. This mechanism is similar to the well known "guard ring" effect, and can limit the maximum electric field magnitude to a value which is lower than the breakdown field.

Computer simulations of devices with and without floating rods were performed using the PISCES code [4,7]. The PISCES software models two-dimensional distributions of potential and carrier concentrations for arbitrary device geometries and bias conditions. The version used was PISCES-IIB of Stanford Electronics Laboratories on a Digital VAX 11/785 mainframe computer.

Two types of simulation were performed: In the first, the effect of floating junctions on device breakdown was studied. The second was aimed at optimizing material parameters and device geometry for high power applications.

The two basic simulation geometries are shown in Figs. 1(b) and 1(c). The conventional case, used as a control [Fig. 1(b)], has one gate junction close to the source. The other case [Fig. 1(c)] has six equally spaced floating rod-shaped junctions between the gate rod and the drain. With six floating junctions, the simulation uses the maximum number of electrodes that can be handled by the PISCES software. Simulations were specified for n-type Si with uniform impurity concentrations of 0.5 - 5 x 10^{15} cm^{-3} PISCES-IIB allows the placement of a simple lumped resistance on a given electrode. This capability was exploited to account for floating rods. Floating rods were simulated by specifying the maximum resistance (10^{31} Ω) for each rod and biasing it to the drain.

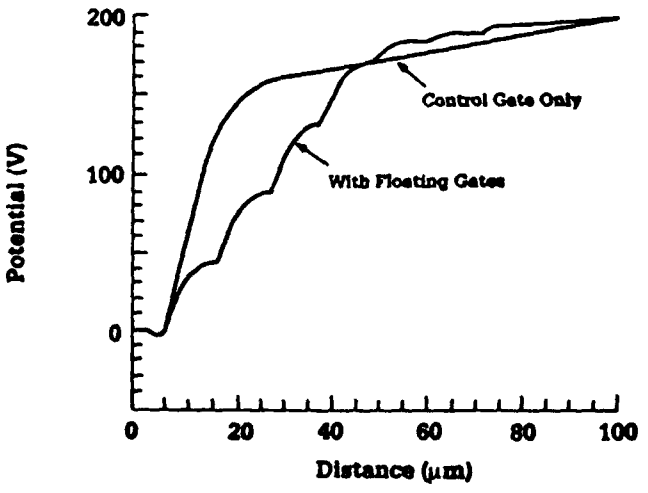


Fig. 2. Potential vs. distance from the source calculated for the geometry of Fig. 1 at a drain voltage of 200 V, with and without floating gates.

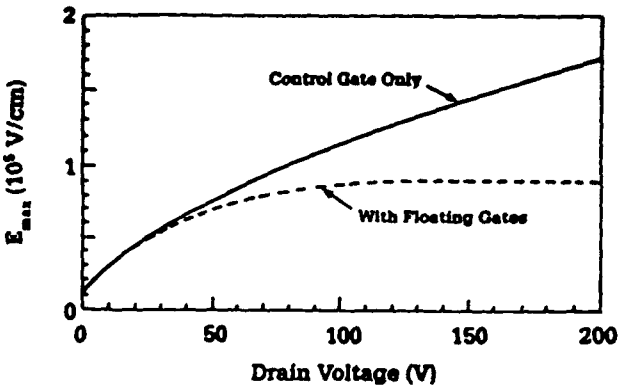


Fig. 3. Maximum electric field vs. drain voltage for the geometry of Fig. 1 showing the field clamping effect of the floating gates.

To simulate the operation of the transistor, the source was held at 0 V, the gate (the first rod) was biased to -2 V, and the drain was stepped from 0 to 200 V in 10 V increments. Potential versus distance from the source is shown in Fig.2 and the maximum electric field magnitude versus drain potential is shown in Fig. 3 comparing the two cases with and without floating gate rods.

For the conventional case without floating junctions, the potential increases parabolically with distance similarly to conventional planar junctions. The maximum electric field magnitude increases monotonically with increasing drain voltage. In the case with floating gate rods, the depletion zone at the gate rod expands with increasing drain voltage as in the conventional case, but only until it intersects the depletion zone of the first floating rod. With further voltage increase, this latter rod floats in potential so that its depletion zone expands towards the next floating rod, and the maximum electric field at the gate rod is clamped. Eventually, the maximum field at the first floating rod is clamped when its depletion zone reaches the next floating rod, and so on. The actual value of the clamping field depends on the interrod spacing and the carrier concentration, but with the proper parameters it can be made lower than the avalanche field.

The results of this model clearly indicate that the floating rods inhibit avalanche breakdown.

Table I

MODEL DEVICE PARAMETERS
MAXIMUM FIELD MAGNITUDE $E_{max} = 10^5$ V/cm

Rod spacing (μm)	Avg. field at E_{max} (V/cm)	G-D dist. for V_{max}=1000 (μm)	N_D (cm^{-3})	J_S (A/cm^2)
4	5.08×10^4	197	5.9×10^{15}	6000
7	5.37×10^4	186	3.3×10^{15}	3300
23	5.44×10^4	184	1.0×10^{15}	870

However, breakdown will eventually occur by a "punch-through" mechanism when the depletion region expands to reach the drain contact and no additional floating rods are available to accommodate further voltage increases. Therefore, the maximum blocking voltage of the device is determined by the gate-drain spacing, rather than the carrier concentration as in conventional devices. This distance can in principal be designed to yield an arbitrarily large blocking voltage, limited only by external factors such as surface breakdown.

Further model calculations were used to investigate the ways that these devices could be optimized for simultaneous high voltage and high current operation. This was done by holding the maximum electric field magnitude to a value less than that of the avalanche field, and calculating the corresponding carrier concentration, N_D, and saturation current density, J_S, for different interrod spacings. A microstructure with floating rods similar to that shown in Fig. 1 was modeled to determine the carrier concentration which yields a saturation E_{max} of 100 kV/cm. This maximum field was chosen because it is conservatively below the value that would lead to avalanche breakdown in silicon. The average electric field magnitude in the gate-drain region and the minimum gate-drain distance needed to hold off 1000 V without "punch-through" were also calculated. The microstructure was then scaled uniformly to different interrod spacings and rod diameters, keeping the volume fraction of the rods constant (as would be the case with real eutectic systems).

The results are shown in Table I for interrod center-to-center spacings of 4, 7, and 23 μm. Although the gate-drain distances needed to hold off 1000 V are similar in all three cases and the spatially averaged field remains nearly constant at about one-half E_{max}, the carrier concentrations and saturation current densities at zero gate bias are quite different. The highest current density is found at the highest carrier concentration, which corresponds to the smallest interrod spacing.

These results are important because they indicate that semiconductor-metal eutectic transistors can be designed to hold off high voltages while at the same time having relatively high carrier concentrations and therefore high current density. In contrast, conventional semiconductor switches must use low carrier concentration material to achieve high voltage blocking capability. They therefore require large conducting areas to provide low on-state resistance.

Experimental Semiconductor-Metal Eutectic Transistors

SME transistors were fabricated [2,3] using 500 μm thick Si-$TaSi_2$ composite wafers cut normal to the growth axis so that the $TaSi_2$ rods were perpendicular to the wafer surfaces. Carrier concentrations were 1-3 x 10^{15} cm^{-3}, and the areal rod density was about 1.6 x 10^6 cm^{-2}, yielding average interrod spacing of ~8 μm.

Wafers were thermally oxidized at 1000 C to form a 0.3 μm oxide layer. The oxide was patterned and opened to form central drain and concentric source and gate contact areas as shown in Fig. 4. The gate

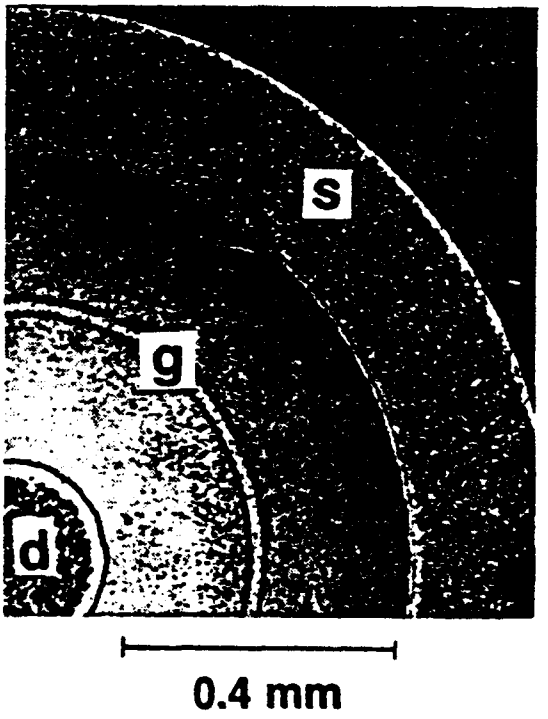


Fig. 4. Micrograph of semiconductor-metal eutectic transistor, showing source and gate contacts surrounding the central drain contact.

contact was formed using a 0.2 μm $CoSi_2$ layer which maintained a Schottky barrier to the bulk Si matrix while providing metallic contact to the $TaSi_2$ rods [1]. Source and drain contacts consisted either of annealed Au-Sb films or P implanted n^+ layers. After electrical measurements, some processed devices were successively thinned by mechanical polishing and remeasured, showing the effects of thickness on device performance.

The transfer characteristic of a typical device is shown in Fig. 5 (Ref. 3). For this carrier concentration and interrod spacing, the modeling results indicate that the maximum electric field at the rods will be less than the avalanche breakdown field due to the effect of the floating rods. (The model indicates that the clamping field will be ~1 x 10^5 V/cm. The avalanche field for planar junctions of this carrier concentration is 3 x 10^5 V/cm, but the actual value will be greater due to the small volume over which the maximum field occurs in the cylindrical geometry.) We therefore expect that breakdown will only occur when the depletion layer punches through to the drain contact where the electric field can increase to the breakdown value. The breakdown voltage will be given approximately by the product of the average electric field and the gate-drain distance. Modeling indicates that the average field will be about 5 x 10^4 V/cm.

Predicted and measured breakdown voltages, V_B, for devices with several gate-drain spacings, which were successively thinned and remeasured, are listed in Table II. They are all lower than the values which would be predicted from the calculated average field and the actual gate-drain spacing.

One effect which should lower the effective breakdown voltage is that of rod divergence [3]. The $TaSi_2$ rods are not perfectly parallel, with a maximum divergence of about +/- 6°. This

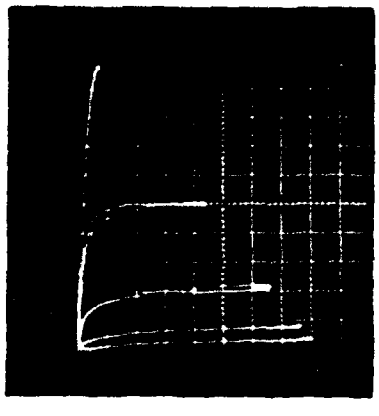


Fig. 5. Transfer characteristic of a typical device.

Table II

MEASURED AND PREDICTED BREAKDOWN VOLTAGES

N_D (10^{15} cm^{-3})	Thickness (μm)	G-D Dist. (μm)	Effect. G-D Dist. (μm)	V_B (meas.) (V)	V_B (predict.) (V)
3	500	137	33	50	165
3	250	137	85	350	425
3	125	137	111	600	555
2	500	150	46	90	230
2	250	150	98	250	490
2	125	150	124	500	620
1	250	180	128	500	640
1	125	180	154	700	770
1	250	62	10	40	50
1	125	250	224	1000	1120

divergence will result in an effective gate-drain distance at the backside of the wafer which is shorter than the actual contact spacing by a factor 2t*tan(6), where t is the wafer thickness. Corrected for this effect, the measured V_B are in reasonable agreement with the predicted values, although still somewhat lower in all but one case as shown in Table II. However, these numbers of up to 1000 V may be compared with the theoretical maximum breakdown voltage of ~200 V for planar Si junctions in this range of carrier concentration.

Also of interest are the current density and the switched power density. The calculated current density for the 7 μm spacing device shown in Table I is 3300 A/cm^2. The corresponding switched power density is 1.6 x 10^8 W/cm^3. These values may be compared with up to ~50 A/cm^2 and ~3 x 10^6 W/cm^3 observed in experimental devices with ~8 μm interrod spacing. It is believed that the experimental figures are lower both because the carrier concentrations were lower by a factor 3 and because the rod distribution is not uniform. The rod distribution pattern has been shown to have a substantial effect on current transport in these materials [8,9]. However, the model results indicate the potential for high power switching of devices made with improved materials.

Conclusions

The unique properties of semiconductor-metal eutectic materials can be exploited to yield a new class of transistors. These devices hold great

promise for the development of high voltage, high current, voltage controlled pulsed power switches. We have demonstrated experimental devices with breakdown voltages far in excess of those expected for planar junction devices made from similarly doped semiconductor material. We have also explored the physics of these devices by numerical modeling to identify the mechanisms which lead to elevated blocking voltages. The origins of these effects are now understood, and it should be possible to make SME devices which hold off arbitrarily large voltages, subject only to external factors such as surface breakdown. This modeling work has also included a study of materials and device parameters needed to optimize both high voltage and high current capability in the same device.

Acknowledgements

The assistance of T. Middleton in material and device fabrication is gratefully acknowledged. This work was supported in part by the Strategic Defense Initiative Office/Innovative Science and Technology (SDIO/IST) and managed by the Office of Naval Research under contract N00014-86-C-0595.

References

1. B. M. Ditchek and M. Levinson, "Si-$TaSi_2$ *in situ* junction eutectic composite diodes," Appl. Phys. Lett. **49**, 1656 (1986).

2. B. M. Ditchek, T. R. Middleton, P. G. Rossoni, and B. G. Yacobi, "Novel high voltage transistor fabricated using the *in situ* junctions in a Si-$TaSi_2$ eutectic composite," Appl. Phys. Lett. **52**, 1147 (1988).

3. B. M. Ditchek and B. G. Yacobi, "Microcharacterization and novel device applications of semiconductor-metal eutectic composites," Japan. J. Appl. Phys. **27**, L2155 (1988).

4. M. Levinson, P. G. Rossoni, F. Rock, and B. M. Ditchek, "High voltage floating gate array transistor," Electron. Lett. **26**, 777 (1990).

5. B. M. Ditchek, B. G. Yacobi, and M. Levinson, "Novel High Quantum Efficiency Si-$TaSi_2$ Eutectic Photodiodes," Appl. Phys. Lett. **51**, 267 (1987).

6. M. Levinson, E. Eichen, P. G. Rossoni, and B. M. Ditchek, "Si-$TaSi_2$ Photodiodes With High Efficiency and High Spatial Resolution from the UV to 1.06 μm," *Conf. on Lasers and Electro-Optics, 1990 Tech. Digest Series Vol. 7*, (Opt. Soc. of Amer., Washington, D.C.), 464 (1990).

7. PISCES-IIB, Stanford Electronics Laboratories, Stanford, CA, USA

8. B. M. Ditchek, B. G. Yacobi, and M. Levinson, "Depletion zone limited transport in Si-$TaSi_2$ eutectic composites," J. Appl. Phys. **63**, 1964 (1988).

9. V. K. Samalam, " Si-$TaSi_2$ eutectic composites as an example of a percolation system," J. Appl. Phys. **67**, 2165 (1990).

HIGH VOLTAGE FLOATING GATE ARRAY TRANSISTORS

Indexing terms: Semiconductor devices and materials, High field effects, Field effect transistors

A new high voltage field-effect transistor is described. It features an array of uncontacted gate elements between the main gate and the drain which float so as to inhibit avalanche breakdown. Good agreement is obtained between model predictions and the performance of experimental devices fabricated in Si–$TaSi_2$ semiconductor–metal eutectic material. Transistors are demonstrated which hold off up to 1000 V, compared with the avalanche breakdown potential of 300 V or less expected for conventional devices made with similarly doped silicon.

A principal factor limiting high voltage capability in semiconductor devices is avalanche breakdown. Achieving a high breakdown voltage usually requires a low carrier concentration and a large depletion width. Low carrier concentrations and large depletion widths produce high series resistance, and so limit on-state current densities.

We have previously demonstrated novel bulk field-effect transistors,[1] as well as diodes[2] and photodiodes,[3] made with semiconductor–metal eutectic (SME) materials. Here we show that novel aspects of their structure can circumvent some of the restrictions imposed by avalanche breakdown in high voltage devices. They present the possibility of very high voltage switching together with high on-state current density. As unipolar devices, they should be more radiation insensitive than bipolar devices.

The transistor geometry[1] is shown in Fig. 1*a*. These devices are made using semiconductor–metal eutectic material which is grown from a melt containing a eutectic mixture of silicon and tantalum disilicide.[4] It contains a quasi-regular array of parallel rod-shaped regions of metallic $TaSi_2$ imbedded in a single crystal silicon matrix. The $TaSi_2$ rods, which are oriented perpendicular to the surface of the wafer, form Schottky junctions with the semiconductor. The gate contact provides metallic contacts to the rods underneath it, but maintains a blocking contact to the semiconductor. The depletion zones of these rods vary with gate bias, thus controlling the drain current.

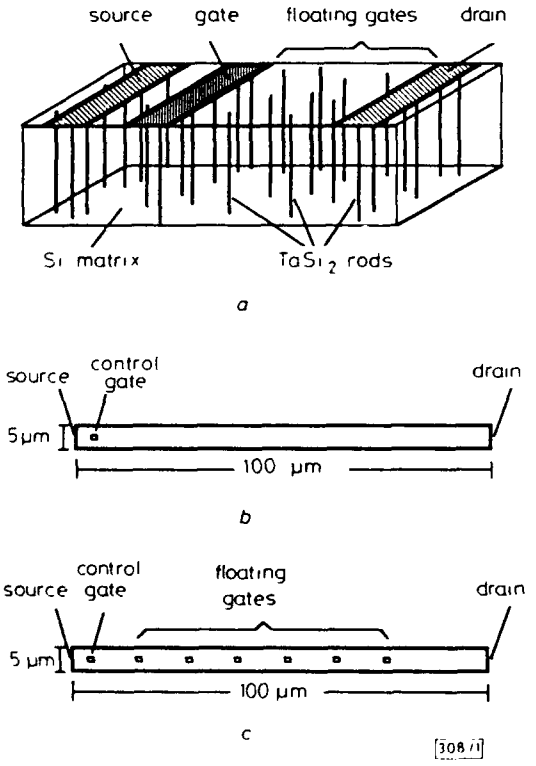


Fig. 1 *Semiconductor–metal eutectic transistor geometry*
a Device structure
b Control gate model
c Floating gates model

A unique feature of this device is the rods which lie between the gate and drain. During device operation, these junctions behave as uncontacted gates which float to potentials determined by the device parameters and external voltages, in a manner similar to guard rings. To study the effects of these floating gates, computer simulations were performed using the PISCES-IIB code (Stanford Electronics Laboratories). Two simulation geometries were used. The first, used as a control, had one contact main gate rod of 1 μm square cross-section adjacent to the source, as shown in Fig. 1*b*. The other case, Fig. 1*c*, has six floating gate junctions at 11 μm intervals between the main gate and the drain, PISCES-IIB allows the placement of a simple lumped resistance on a given electrode. Floating junctions were simulated by inserting the maximum resistance ($10^{31}\,\Omega$) and biasing them to the drain. Simulations were specified for *n*-type Si with uniform donor concentrations of $0{\cdot}5\text{–}5 \times 10^{15}\,cm^{-3}$. These parameters were chosen to approximate those of existing SME devices. Similar floating gate effects were observed in simulations using a range of carrier concentrations and inter-rod spacings, and with staggered rather than in-line rod layouts.

The potential at the centre of the channel as a function of distance from the source is shown in Fig. 2. The maximum

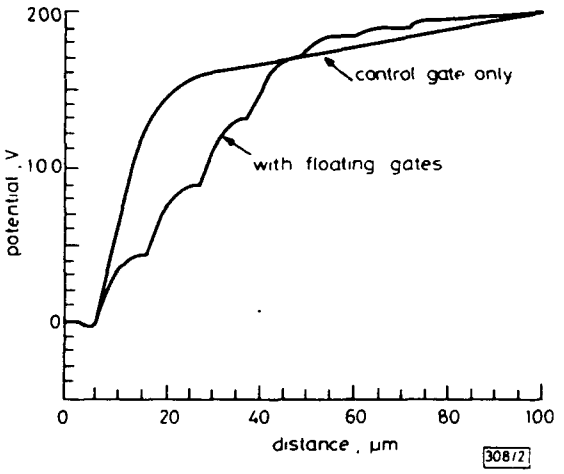


Fig. 2 *Potential against distance from source*
Control gate bias = −2 V
Drain bias = 200 V

electric field as a function of drain potential is shown in Fig. 3. The carrier concentration is $5 \times 10^{14}\,cm^{-3}$, and the control gate bias is −2 V. In the case without floating gates, the maximum electric field increases monotonically with increasing drain voltage, as in conventional planar junctions. When floating gates are incorporated, the control gate depletion zone expands with increasing voltage as before, but only until it reaches the first floating gate. Beyond this point, the floating gate rises in potential as its depletion zone expands towards the next floating gate, and the maximum electric field at the control gate is clamped. The same maximum field is attained at the first floating gate when its depletion zone reaches the second floating gate, and so on. The actual value of the clamping field varies with the spacing between the floating gates and the carrier concentration. It can be made lower than the avalanche field by proper design.

Breakdown will eventually occur when the depletion region expands beyond the floating gate array and no additional floating gates are available to accommodate further voltage increases. At some voltage, the avalanche field will be attained at the last row of floating gates unless the depletion zone reaches the drain contact first and a 'punch-through' mechanism occurs. This latter effect occurs in SME transistors, as the array length is equal to the gate-drain spacing. The maximum blocking voltage of the device is primarily determined by the length of the floating gate array, rather than the carrier concentration as in conventional devices. This distance can in principal be designed to yield an arbitrarily large

Table 1 MEASURED AND PREDICTED BREAKDOWN VOLTAGES

Carrier concentration	Wafer thickness	G-D distance	Effective G-D distance	V_{max} measured	V_{max} predicted
$10^{15}\,cm^{-3}$	μm	μm	μm	V	V
3	500	137	33	50	165
3	250	137	85	350	425
3	125	137	111	600	555
2	500	150	46	90	230
2	250	150	98	250	490
2	125	150	124	500	620
1	250	180	128	500	640
1	125	180	154	700	770
1	250	62	10	40	50
1	125	250	224	1000	1120

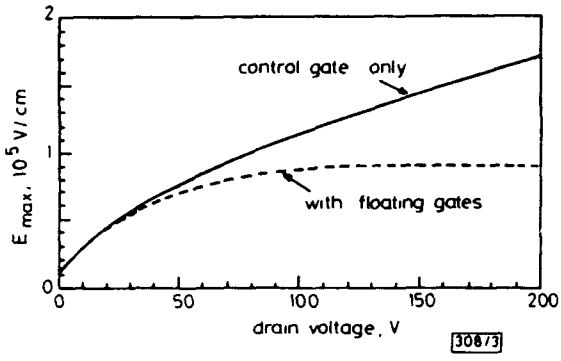


Fig. 3 *Maximum electric field against drain voltage*

blocking voltage, limited only by external factors such as surface breakdown.

SME transistors were fabricated as previously described,[1] with a central drain and concentric annular gate and source contacts. Carrier concentrations were $1–3 \times 10^{15}\,cm^{-3}$, and the rod density was about $1·6 \times 10^{6}\,cm^{-2}$, yielding average interrod spacing of $\sim 8\,\mu m$. Different size devices were fabricated, with gate-drain distances in the range $62–250\,\mu m$.

For these carrier concentrations and interrod spacings, the model predicts that the maximum electric field will be clamped lower than the avalanche breakdown field. We therefore expect that breakdown will only occur when the depletion layer punches through to the drain contact. The breakdown voltage will be given to a good approximation by the product of the calculated average electric field and the gate-drain distance.

One effect which lowers the effective breakdown voltage in these devices is that of rod divergence.[4] The $TaSi_2$ rods are not all perfectly parallel, but exhibit a maximum divergence of about $\pm 6°$. The divergence will result in an effective gate-drain distance at the backside of the wafer which is shorter than the actual contact spacing by a factor $2t \tan(6)$, where t is the wafer thickness.

Measured and predicted breakdown voltages for devices with several gate-drain spacings, which were successively thinned and remeasured, are listed in Table 1. The measured voltages are in good agreement with the predicted values after correction for rod divergence. These value of up to 1000 V may be compared with the theoretical breakdown voltage of 100–300 V for planar Si junctions in this range of carrier concentration.

In summary, we have modelled and demonstrated the suppression of avalanche breakdown by floating gate arrays in semiconductor–metal eutectic field effect transistors. These devices can, in principle, be designed for an arbitrarily large breakdown voltage. Good agreement was obtained between model predictions and experimental breakdown voltages, which were more than three times larger than those expected for planar junctions in silicon of the same carrier concentration.

The assistance of T. Middleton in the crystal growth and device fabrication is gratefully acknowledged. This work was sponsored in part by the Strategic Defense Initiative Office/Innovative Science and Technology (SDIO/IST) and managed by the Office of Naval Research under contract N00014-86-C-0595.

M. LEVINSON
P. ROSSONI
F. ROCK
B. M. DITCHEK

GTE Laboratories Incorporated
40 Sylvan Rd.
Waltham, MA 02254, USA

24th November 1989

References

1 DITCHEK, B. M., MIDDLETON, T. R., ROSSONI, P. G., and YACOBI, B. G.: 'Novel high voltage transistor fabricated using the *in situ* junctions in a Si–$TaSi_2$ eutectic composite', *Appl. Phys. Lett.*, 1988, **52**, pp. 1147–1149

2 DITCHEK, B. M., and LEVINSON, M.: 'Si–$TaSi_2$ *in situ* junction eutectic composite diodes', *Appl. Phys. Lett.*, 1986, **49**, pp. 1656–1658

3 DITCHEK, B. M., YACOBI, B. G., and LEVINSON, M.: 'Novel high quantum efficiency Si–$TaSi_2$ eutectic photodiodes', *Appl. Phys. Lett.*, 1987, **51**, pp. 267–269

4 YACOBI, B. G., and DITCHEK, B. M.: 'Characterization of multiple *in situ* junctions in Si–$TaSi_2$ composites by charge-collection microscopy', *Appl. Phys. Lett.*, 1987, **50**, pp. 1083–1085