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QUARTERLY TECHNICAL REPORT No. 2

**SETA Support for the DARPA Microelectronics Technology
Insertion Program of the Microelectronics Technology Office**

Sponsored by:
Defense Advanced Research Projects Agency
Microelectronics Technology Office
Microelectronics Technology Insertion Program
ARPA Order No. 8500 Program Code Nos. 2E20 and 2D10
Issued by DARPA/CMO under Contract No. MDA972-92-C-0029

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Booz·Allen & Hamilton Inc.

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1. Introduction

Booz • Allen & Hamilton provides DARPA's Microelectronics Technology Office a broad range of SETA support under contract MDA972-92-C-0029. This report describes activities during the second quarter of this contract. The main programs supported were the Microelectronics Manufacturing Programs, the Transition of Optical Processors to Systems Program, the Digital Gallium Arsenide Insertion Program, and the Artificial Neural Networks Program.

This report is organized by subtask areas covered in the Statement of Work, indicating for each subtask Task Objectives, General Methodology, Technical Results, Important Findings and Conclusions. The final section of this report reviews contractual, administrative, and financial considerations. Appendices present all deliverables from Booz • Allen and special consultants providing MTO support via this contract.

2. Task 3.1: Engineering and Technical Support Services

2.1. Subtask 3.1.1: Engineering and Technical Integration and Coordination

Task Objectives: The objective of this subtask is to serve as liaison for various MTO programs, help identify and develop new programmatic opportunities, and explore pathways for technology transfer.

Individual Taskings: *General Methodology, Technical Results, Important Findings, and Conclusions.* Booz • Allen serves as a primary liaison between MTO, funded contractors, and the technology community at large for the programs supported under this contract. Booz • Allen fills this capacity in several ways, including: regular phone contact with contractors; on-site visits to contractor facilities; and participation in conferences, workshops, and symposia. Contractor activities are monitored in informal on-site visits, workshops, and regularly scheduled In Progress Reviews (IPRs). During the second quarter of this contractual effort, Dan Butler, program manager, and other Booz • Allen employees met with contractors and other parties involved in contractual efforts on ten separate occasions to serve as liaison for MTO and monitor progress toward each program's objectives. These meetings included:

Microelectronics Manufacturing

ISMSS '92

SEMICON WEST Manufacturing Equipment Convention

11th Annual Dataquest Briefing at SEMICON WEST

SEMATECH Rapid Thermal Processing (RTP) Temperature Control
Workshop

Digital Gallium Arsenide

GPS JPO Review

Martin Marietta Missile Systems Insertion Project Review

Transition of Optical Processors to Systems

Martin Marietta's Pattern Recognition System Design
Review

General Electric's Antenna Null Steering Processor Third Status
Meeting

Hughes Aircraft Co.'s Optical Control of Phased Array Radar
Preliminary Design Review

Texas Instruments Phased Array Radar Program Review

While the trips listed above are described in greater detail in the trip reports (see Appendix 1), several interesting findings are noted here. At the request of the MTO Director and MMST Program Manager, Graydon Larrabee and Mark Connor attended SEMICON West, the largest semiconductor manufacturing trade show in the nation, and noted several findings of interest to the MTO MMST and the new "flexible, intelligent" (FIMM) manufacturing programs. At the SEMICON West Trade Show, for instance, it was noted that this year the MESC standards cluster tool was prominently featured. The cluster tool market is expected to more than triple between 1991 and 1996. The Dataquest Briefing at SEMICON West highlighted a surplus capacity in 4 Mbit dRAMs, but the U.S. is lagging in the move to a larger diameter wafer. At the ISMSS '92 symposium, "Applying Vision in Automated Semiconductor Manufacturing Equipment Seminar," presenters discussed work-in-process (WIP) and run-by-run (RbR) control which can modify equipment recipes based on *in-situ* measurements, correcting for equipment drift. There is a need for a common manufacturing standard, however. This same need was noted at the SEMATECH RTP workshop, and RTP does not yet appear to be required or desired by companies as a process tool. As IC feature sizes decrease, it may become the tool of choice, but models, a common manufacturing standard, and comparison metrics need to be established first.

Based on progress to date and the material presented by Martin Marietta Radar and Missile Systems Division at the June 3, 1992 program status review, DARPA decided to terminate Martin Marietta's RF Hellfire digital gallium arsenide insertion project. Martin Marietta reported that due to technical and design difficulties, the project would be 100% overrun in both time and cost.

The IC design difficulties noted in this program for the last eighteen months are similar to those noted in an another insertion project with difficulties in time and cost overruns – the E-Systems Greenville Division RC-135 Project. Neither contractor had internal GaAs expertise or IC design capability and as a consequence were totally dependent on their subcontractors. Both prime contractors appeared to lack even the necessary expertise to oversee the work of their subcontractors.

2.2 Subtask 3.1.2: Technical Studies and Assessments

Task Objectives: The objective of this subtask is to provide technical expertise to translate microelectronics performance benefits into operational benefits. This requires performing systems analyses and providing background information on technical and programmatic aspects of a wide variety of operational and developmental military systems.

Individual Taskings: *General Methodology, Technical Results, and Important Findings and Conclusions.* Key personnel used a variety of analytic methods to conduct technical studies and assessments. Expertise available within the team of key personnel was supplemented as necessary by corporate resources and special consultants to provide MTO with the most robust analysis available. Several study activities initiated under this subtask are described below.

Flexible, Intelligent Manufacturing: Booz-Allen personnel continued to provide technical support to the efforts of the MTO Director and MMST Program Manager to create a small, "flexible, intelligent" wafer fabrication facility (FIMM) by the end of the decade. This support included supplying the Director with technical data to help craft the cost and technical parameters of the program. Details of this research are in Appendices 1 and 2. This data was culled from personal expertise, as well as industry and SEMATECH sources. Also, developments were monitored both in the United States and abroad, as reported by the foreign and national press. This helped insure that the MTO Director had the most accurate, up-to-date data on which to base her program decisions. Assistance was rendered to aid her to devise long and short range goals for the program, and to communicate those goals to industry, military, and government personnel, as shown in Appendix 3.

Look Back at GaAs: The MTO Director requested an overall review of DARPA's Digital Gallium Arsenide programs. Booz•Allen developed a study plan and identified resources using the GaAs contractor files. A survey of over 100 leaders and key participants, including figures from industry, academia, and government, in the GaAs programs was initiated. A questionnaire queried them on significant accomplishments, corporate commitment, and their overall comments on DARPA's impact on GaAs technology and the industry. Responses are still being received and a series of extensive interviews is planned as the next step in this review.

Developments in A/D Converters: The MTO Deputy Director requested that research be done to identify potential developments in A/D converters. Again, Booz•Allen used a survey approach to collect data for this effort. Experts within Booz•Allen and in special consulting capacities were queried on A/D mission requirements and interesting foreseeable developments. A short Special Technical Report was generated in May, and a copy is attached as part of Appendix 1.

IC Manufacturing Research: In the first quarter, Booz•Allen initiated a concerted effort to study IC manufacturing processes and issues to provide the best possible support to members of MTO staff involved in designing a new DARPA program for microelectronics manufacturing. During this reporting period, Graydon Larrabee and Mark Connor, at the request of the MTO Director and MMST Program Manager respectively, attended SEMICON WEST and studied the state-of-the-art equipment in microelectronics manufacturing. Efforts in this area will continue, focusing on specific manufacturing processes, developments, and challenges.

2.3 Subtask 3.1.3: Technical Documentation

Task Objectives: The objective of this subtask is to provide writing, editing, production, and technical document coordination.

Individual Taskings: *General Methodology, Technical Results, and Important Findings and Conclusions.* The level of support required for this subtask varies according to the needs of the MTO Directors and Program Managers. Technical documentation generated this quarter included view graphs and briefings; brochures; and providing support and assistance in preparing articles for publications.

View Graphs and Briefings: A total of 28 new and revised view graphs (all presented in Appendix 3) were produced during the second quarter of this contract. Many of these taskings required rapid turn around and absorbed a significant portion of available resources. To ensure as rapid a response time as possible, Booz•Allen scheduled all other non-urgent taskings around these quick turn around requests.

A number of these individual view graphs were part of two new briefings developed for the MMST Manager, based on Booz•Allen research and analysis. One briefing was on Microelectronics Manufacturing Processing and Equipment and a second was on Contamination Free Manufacturing. In addition, a revised edition of the Microelectronics Manufacturing Briefing was produced for the MMST Program Director and a new set of the view graphs for the MTO Office Briefing was delivered to the MTO Director.

Brochures: Booz•Allen drafted two brochures during the second quarter. The first brochure focused on the soon-to-be completed DARPA programs in Digital Gallium Arsenide. The objective of this brochure is to inform the technology community at large (government, industrial, and academic, with primary emphasis on the private sector) of the goals and results of DARPA's programs to develop digital GaAs technology and the supporting industrial infrastructure. It is intended to provide interested parties an overview of progress and a list of key contacts in the industry (including foundries and GaAs insertion contractors). A full draft of this brochure has been designed and delivered to the GaAs Program Manager for his review.

The second brochure is intended to review the MMST program and generally promote the new strategic approach to microelectronics manufacturing represented in this DARPA program. The brochure will be based on the first video Texas Instruments produced on the MMST program. A draft of this brochure had been delivered to the MMST Program Manager and is awaiting his review. Production of both of these brochures awaits approval by DARPA.

Article Support: Booz•Allen supported efforts by the Digital Gallium Arsenide Program Manager to prepare an article for publication in III-V Review. This effort included securing photographs and illustrations for the article, and conducting a literature search to provide him with up-to-date information on the performance of various reconnaissance platforms, including the P-3C J-STARS, and UAVs during the Persian Gulf War.

Special Comments, Implications for Further Research: While the level of effort required to support this subtask has dropped off during this quarter (particularly during July when a majority of MTO personnel were in California attending the annual DSRC presentations), periods of high demand for these services are expected to continue throughout the period of performance. To ensure rapid turn around, Booz•Allen will continue the general approach of scheduling all other, non-urgent taskings around those requiring rapid turn around.

3. Task 3.2: Management and Administrative Support Services

3.1 Subtask 3.2.1: Program Planning and Control

Task Objectives: The objective of this subtask is to provide MTO with planning and control assistance. It includes providing schedule and resource visibility to assure that contract objectives are being achieved and tracking performance, schedule, action items, and subcontracted efforts.

Individual Taskings: *General Methodology, Technical Results, and Important Findings and Conclusions.* Activities in this subtask complement efforts in Subtask 3.1.1 (Engineering and Technical Integration and Coordination) and are carefully coordinated to ensure complete follow through on action items.

Funding Questionnaire: A major task begun during this quarter was the development and dissemination of a contractor funding and status questionnaire which enables DARPA program manager's to have a snapshot view of the status of their various contracts and to identify potential funding and performance problems. In addition, the questionnaire helped accomplish the MTO goal of verifying that all FY 92 committed funding had been obligated to the proper contracts, and provides the necessary data for DARPA to prepare FY 93 incremental funding paperwork.

To carry out this task, a draft of the contractor funding questionnaires was developed using direction from the COTR. Then it was further modified to incorporate revisions suggested by the COTR and the MTO program managers. After the questionnaire was developed in finished form, other SETA contractors for MTO program managers were briefed on how to collect the necessary information. Questionnaires were faxed out to POCs at the contracting companies and responses were received and entered into a computer database. At this stage, data collection is still proceeding and the results will be delivered to the COTR and the program managers early next quarter.

Special Comments, Implications for Further Research: The majority of Booz•Allen's senior program management resources on this contract are committed to Subtasks 3.1.1 and 3.2.1. The level of effort expended has been significant. Travel requirements and other planned activities indicate that the level of effort will remain high. This factor is a serious consideration in budgeting funds and managing resources available to support MTO, and it will weigh heavily in staff development decisions.

Booz•Allen is developing software that will be able to electronically transfer the data collected by other MTO SETA contractors and incorporate it into the MTO Financial Tracking System being developed by Booz•Allen. This will save considerable time and effort and will improve the accuracy of the FTS data base.

3.2 Subtask 3.2.2: Facilities and Logistics Support

Task Objectives: Under this task, Booz•Allen is to provide the personnel and resources to conduct unclassified and classified technical conferences and workshops, including planning, organizing, conducting mailings, and providing conference materials and audio-visual equipment for these conferences.

Individual Taskings: *General Methodology, Technical Results, and Important Findings and Conclusions.* Key personnel planned and administered the 193-nm lithography SBIR workshop on May 7, 1992 as well as planned the GaAs Insertion Workshop scheduled for November 20, 1992. In addition, the Booz•Allen office was the site of a planning meeting for the Flexible, Intelligent Microelectronics Manufacturing (FIMM) program in May.

Booz•Allen participates in various aspects of conference planning, ranging from limited support to total support, as determined by the role of other participants and as directed by MTO staff. Planning activities include identifying, inviting, soliciting, and registering participants; locating and pricing facilities to secure the optimal location (informal competitive bidding process); arranging logistics such as catering, equipment rental, conference set up; and providing follow up as necessary (generating notes and proceedings to document outcomes, thanking participants, etc.).

3.3 Subtask 3.2.3: Documentation Management and Control

Task Objectives: The objective of this subtask is to coordinate program documentation activities by building and maintaining accurate data bases on programmatic information.

Individual Taskings: *General Methodology, Technical Results, and Important Findings and Conclusions.* Taskings in this area are designed to support program planning efforts covered in Subtasks 3.1.1 and 3.2.1 and provide MTO staff with maximum visibility and flexibility to manage programs.

Financial Tracking System: The main effort initiated under this subtask is the design and development of the Financial Tracking System, a relational database designed to track funds expended under all MTO contracts. The overall objective of this database is to provide MTO staff with better visibility of the expenditure of funds so that MTO resources can be more efficiently budgeted, committed, and obligated. The database will also enable MTO staff to identify potential problems or funding shortfalls before crises develop. The database will register the receipt of contract deliverables and track financial information indicated in such reports. When deliverables are late or financial data is either not included or insufficient, a letter report will be generated and sent to the delinquent contractor, following approval by the responsible MTO program manager.

During the second quarter, the database, using Fourth Dimension software, was further developed. Contract and financial data which had been gathered from various sources relating to the Photonics and TOPS programs were entered into the database. To fill gaps in available data, questionnaires were sent to TOPS and Photonics contractors. As these questionnaires were

returned, the data was entered into the financial tracking system database. In addition, in some cases where better data was not available, deliverable due dates were extrapolated from contract information and existing deliverables. Data gathered in these ways will be checked against the separate Contractor Funding Status Questionnaire (see Subtask 3.2.1) to ensure the accuracy of the information in this database. The development and maintenance of this database consumed a substantial part of Booz • Allen's resources in this quarter.

Other Document Management Taskings: Other documentation management and control taskings include: continued, biweekly updating of a point-of-contact database using Hypercard software for the GaAs and manufacturing programs; and implementing the direction of the Program Manager to organize the GaAs and manufacturing program files. In addition, work has begun on organizing a central program file at MTO which would include contract, funding and deliverable data on all MTO Contracts. It is anticipated that this last effort will grow and be further developed in the next quarter of this contract.

3.4 Subtask 3.2.4: Administrative Program Support

Task Objectives: The objective of this subtask is to provide administrative program support for the MTO Director, Deputy Director, and staff.

Individual Taskings: *General Methodology, Technical Results, and Important Findings and Conclusions.* Many individual taskings in a broad range of areas were accomplished under this subtask.

Administrative Taskings: Administrative taskings performed during this reporting period included arranging the fabrication of two new copies of a display using an MMST wafer; shipping supplies to the DSRC in California; and obtaining various documents (magazine articles, the Congressional Yellow Book and Congressional budget language).

3.5 Subtask 3.2.5: Transition Plan/Scheduling/Phasing

Task Objectives: The objective of this subtask is to provide a detailed Transition Plan outlining the strategy and methodology for transitioning the program support services performed under this contract to a follow-on contractor.

Individual Taskings: *General Methodology, Technical Results, Important Findings and Conclusions.* The general methodology used to accomplish all taskings was designed to ensure complete documentation of activities and the development of stand alone, easily transferable deliverables (databases, special technical reports, and so on). The objective in doing this is threefold: first, it

provides MTO with complete records and thereby enhances the ability of MTO staff to manage programs effectively; second, it causes the development of products and services that can be completely transferred to MTO staff for direct use; and third, it ensures that transitioning to a follow-on effort will be smooth and efficient.

4. Conclusions

4.1 Special Comments

Booz•Allen supplied a high level of support during the second quarter of the MTO SETA contract. No technical problems were encountered and no significant hardware was developed or purchased.

This quarter saw significant contributions by the special consultants added to the contract in the first quarter. In particular, Mr. Graydon Larrabee responded to several special taskings from the MTO Director related to the FIMM program, and attended several conferences at her direction. Dr. Barbara Yoon was also added to the contract as a special consultant during this period.

Booz•Allen continued to monitor the expenditure of contract funds using the five internal sub-accounts:

- GaAs Support
- TOPS Support
- MTO Administrative Support
- Technical Support
- Microelectronics Manufacturing Support

As of the monthly Status Report for February 1992 (second monthly report), financial status is tracked by the five sub-accounts with overall status reported on the summary status worksheet. Due to increased MTO tasking for Booz•Allen to support the Artificial Neural Networks Program, Booz•Allen recommends that a sixth sub-account be added to track resource expenditures in this technical area.

4.2 Implications for Further Research and Support

During the next quarter, Booz•Allen will continue to provide a high level of support to the Microelectronics Technology Office, including responding to new taskings and requests. The data gathering for the Contractor Funding Questionnaire will be completed and the results delivered to the COTR and responsible program managers. Booz•Allen continued to develop the Financial Tracking System this quarter, and it is anticipated that this will become fully

operational for the Optics and Photonics contracts during this next quarter. In addition, it is anticipated that efforts will commence to create a central program file at MTO, creating a filing system for all of MTO's current contracts based on ARPA order number. Work will continue on the Gallium Arsenide Insertion Workshop and support and documentation will continue to be provided for briefings by the MTO director, Deputy Director, and program managers. In technical support of the FIMM program, computational modeling of FIMM fabs and conventional fabs will be performed in cooperation with SEMATECH. Modeling of manufacturing costs for logic and dRAMs will examine the roles of escalating capital and development costs.

APPENDIX 1

SPECIAL TECHNICAL REPORTS & TRIP REPORTS



SPECIAL TECHNICAL REPORT No. 2

A/D and D/A Conversion Survey Results

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In support of DARPA's advanced A/D converter program, Booz•Allen has conducted a survey among the firm's technical experts supporting numerous military clients, to solicit opinions on the most exciting A/D converter applications. A common theme among the views expressed was a desire to extend the speed and/or resolution as well as lower the power dissipation of *monolithic* converters. Using monolithic versus hybrid converters as well as utilizing more and more powerful digital signal processing (DSP) techniques permits the replacement of expensive and less reliable filters and precision analog components.

Much attention has been focused on the achievement of very high speed and very high resolution in A/D and D/A conversion. The myriad applications requiring ADCs and DACs typically stress either high speed (samples/sec) or high resolution (bits). The following lists the current state-of-the-art for monolithic converters:

4 bits @	2-3 GS/s
5 bits @	2.5 GS/s
8 bits @	1 GS/s
12 bits @	20 MS/s
14 bits @	10 MS/s

Primarily, digital GaAs technology is used to produce these high performance converters; alternatives to GaAs include submicron Si and InP. In general, complementary bipolar technology is pushing improvements in speed; while BiCMOS permits increased levels of integration. Heterojunction bipolar transistor (HBT) GaAs technology is currently being applied for advanced monolithic converters. Hybrids are still envisioned to be the choice of the most advanced converters for the time being. Issues associated with the GaAs monolithic converters include density, yields, interoperability with existing technologies, packaging constraints, the absence of CAD support, and the potential high cost. Additional concerns include the need for on-chip thermal and EM modeling. Also, at this time, memory-intensive applications cannot keep pace with the converter advances; memories need to improve. Short term goals (~5 years) for advancing converters are:

4-6 bits	@	8-12 GS/s
8-10 bits	@	3-6 GS/s
12-16 bits	@	100-200 MS/s

Foreseeable communications applications typically focus on digital radio technology. The high performance converters would permit digital filtering in lieu of much of the analog processing. The Joint Multimode-Multiband Digital Radio or

"Speakeasy," envisioned for the late 90's, will incorporate A/D conversion at the IF in the near term and conversion at the RF in the long term. Digital radar applications also seek the direct digitization of wideband RF that permits the use of powerful DSP techniques such as cyclostationary signal processing, detection of ultrawide signals, and higher order statistics. These techniques offer the ability to detect signals that are undiscernible today.

The higher converter speeds would permit the use of more robust coding schemes that incorporate more overhead than is now acceptable. For instance, multigigabit rate systems without coding require a SNR at 13-15 dB; however, using error detection and correction (EDAC) techniques reduces the requirement to 5-7 dB, yielding an 8 dB savings in transmitter power. Also, improved signal detection with direct rather than baseband sampling and instantaneous image processing are conceivable with higher converter performance.

Finally, high-temperature superconductive (HTSC) converters are another thrust. Rome Lab is conducting a terahertz technology effort utilizing sub-millimeter wave (approaching 1 THz) HTSC devices with integrated planar structures to include converters. Both A/D and D/A converters can use Josephson junctions (JJ) to improve performance. Superconductive quantum interference devices (SQUIDs), such as JJs, are used to form very simple converters with very rapid switching (10 to 30 ps) times. Also, the HTSC converters only consume 1/1000 of the power of more conventional converters. Serial HTSC converters have been demonstrated at 15 bits and 100 MS/s; and, 30 bits and 100 kS/s. Parallel HTSC converters, though limited to ~10 bits are capable of speeds up to 10 GS/s; a typical parallel HTSC converter is 6 bits at 3.5-5 GS/s. HTSC devices are still relatively new (late 1986) and thus pose considerable challenges including thermal management, immature fabrication techniques, and unestablished reliability.

Trip Report

Sematech Plasma Etch FTAB
Austin, Texas
April 22-23, 1992

At the request of Mr. Zachary Lemnios, DARPA/MTO, Booz•Allen & Hamilton Inc., attended the Plasma Etch Focus TAB. Sematech was requested to mail a copy of the proceedings directly to Mr. Lemnios.

The morning of the first day was devoted to more extended versions of the presentations given at the Plasma Damage Workshop by Professors Fonash and Viswanathan.

An off-line conversation was held with Professor Fonash because of questions raised by several attendees that plasma damage to the silicon substrate did not matter because it would be corrected by subsequent processing steps or by an ozone clean. A status report on a joint Advanced Materials/Sematech project seemed to contradict some of Professor Fonash's results.

The off-line conversation with Professor Fonash elicited the following information:

(1) Plasma damage mechanisms and effects are not well understand. This was echoed in the Advanced Materials presentations. Apparently, this has not mattered much in the past (as reflected by the comments of process engineers in attendance); however, Professor Fonash points out that the Japanese have become very concerned about plasma damage and much work in the area is on-

going in Japan, and as device sizes continue to shrink, plasma damage is going to be very important.

(2) Ions present in plasmas can cause charging in oxides which result in flatband voltage shifts due to trapping. This effect will be more pronounced in smaller device sizes.

(3) Professor Fonash does believe that spectroscopic ellipsometry could be used for real-time process control. Problems with this approach is that two ports would have to be created and the alignment of the light is critical (the criticality of the alignment would not make process engineers very happy), and some area on the wafer would have to be dedicated which would not please the business people worried about device yields.

The presentations by the companies as well as the overview of the plasma etch thrust area by Sematech all confirm Mr. Lemnios' suspicion that Sematech is concentrating only in incremental improvements to existing equipment rather than on the future.

Trip Report

SEMATECH Rapid Thermal Processing (RTP) Temperature Control Workshop Santa Clara, California May 1, 1992

Mark P. Connor attended the subject workshop for Mr. Zachary Lemnios, DARPA/MTO. Dr. Lawrence A. Larson, Implant/RTP Development Leader at SEMATECH, will forward two copies of the proceedings in approximately two months to Booz•Allen for further distribution; however, copies of the view graphs presented are attached.

Four major areas were discussed: (1) temperature measurement techniques and control requirements for RTP processes; (2) RTP process insertion requirements; (3) modeling applications of RTP tools; and, (4) standardized metric to compare RTP tools.

(1) Current temperature control techniques have an error of $\pm 10^{\circ}\text{C}$. SEMATECH's goal is ± 3 in the near-term, however, members indicated a need for ± 0.5 . Pyrometry can still be used and improved for temperature measurement, but the limit is being reached. Other methods such as IR spectral correlation, local expansion of grating, speckle interferometry, acoustic wave propagation, and multi-wave pyrometry with emissivity correction, among others are being aggressively pursued.

(2) Having a capable technology alone is not sufficient for insertion. Acceptance by managers within the realms of cost, throughput, and fab management must be considered. Drivers for RTP insertion into likely processes, e.g. silicide anneal and gate oxidation, include a low D_t , complex processes, and larger wafers. SEMATECH estimates RTP to become economically more desirable than expected furnace technology with 0.33μ line widths. IBM, however, stated that RTP will not be required for their 0.25Gbit DRAM, but quality issues with polysilicon contacts above 1000°C may justify its use.

(3) Modeling applications include cluster tools. Most members were concerned about throughput, overhead down time, fab management, equipment redundancy, and cost.

(4) Users of RTP equipment seem to be inundated with supplier spec sheets comparing their RTP product to some specification which is not common among suppliers, making product comparisons difficult and time consuming. SEMATECH was asked and will attempt to provide a common metric by which all RTP equipment can be judged. Many issues need to be resolved to complete this task effectively; in the interim, SEMATECH will produce a collection of all the vendors and their claims in one document.

In summary, RTP does not yet appear to be needed or accepted by member companies as a process tool. As feature sizes decrease and tighter tolerances are required, RTP may become a tool of choice, most likely incorporated as a cluster tool. Members consider 0.33 μ technology with temperatures above 1000°C for silicide anneals and gate oxidations to be the initial insertion thresholds and criteria. Until then, models and comparison metrics need to be established.

Trip Report

SEMICON/WEST 92 San Francisco, California June 14-21, 1992

Mark P. Connor attended the convention at the request of Mr. Zachary Lemnios, DARPA-MTO. The convention consisted of numerous conferences, a symposium, a Dataquest briefing (attended by Mr. Graydon Larrabee, Booz•Allen Special Consultant), and a semiconductor manufacturing equipment exhibition. Of these Mr. Connor attended the ISMSS '92 symposium, "Applying Vision in Automated Semiconductor Manufacturing Equipment Seminar," and the equipment exhibition.

The ISMSS consisted of four sessions:

1. manufacturing performance characterization;
2. personal empowerment, teamwork, and organizational systems;
3. productivity tools and systems; and,
4. evolving technology.

The first talk of session one focused on the tests needed to upgrade from trend charts to control charts in semiconductor manufacturing, given the fast changing processes requiring hundreds of reliable control charts. Tests involving the variance and mean were proposed. The second talk considered an optimization of the die probe process, using Taguchi techniques, within existing production constraints that minimized probe needle resistance and increased die-per-wafer yield. Next was a talk that developed an IC performance prediction model from a small set of measurable parameters responsible for the variation in fabricated parts. From the resulting predictions the parts could be properly binned. The fifth talk addressed the estimation of semiconductor yield from equipment particle measurements, given that this contamination is the dominant source of particulates in mos* fabs today. Monitoring supplier quality at PPM levels was discussed. Using the lot acceptance rate as a metric was demonstrated to be inadequate; however, a line PPM metric proved effective. Finally SEMATECH stated the need of IC manufacturing for future factories, e.g. micro-environments, modular-cluster tools, point-of-use purity, etc.

Session two was somewhat more generic, focusing on the such topics as (1) development, application, and leverage of teams in manufacturing; (2) de-layering and self-directed work teams in an integrated manufacturing organization; (3) employee empowerment; (4) manufacturing integration through EBI; (5) transforming production into world class manufacturing; (6) establishing teams in a 24 hour, 7 day work week

environment; and, (7) the implementation of total quality management (TQM) in a semiconductor manufacturing operation. Clearly, the talks focused on people and managing group dynamics.

Session three illustrated first how productivity can be enhanced through manufacturing ownership of work-in-process (WIP) control. Second, a run-by-run (RbR) process controller was introduced which, through in-situ measurements, was able to modify, either gradually or rapidly depending on out-of-limits parameters, equipment recipes. By incorporating post process measurements the models can be updated for equipment drift. A similar approach was taken in the next talk titled, "Application of Feed-forward Control to a Photolithography Stepper." The remaining talks were:

1. "Competitive Manufacturing through Total Productive Maintenance;"
2. "Paperless Manufacturing for IC Assembly;" and,
3. "From Spreadsheets to Simulations: A Comparison of Analysis Techniques for IC Manufacturing Performance."

Session four incorporated many topics covering technology, partnerships, teamwork, factory-based environments, models, etc. All of these talks pertained to evolving technology for future IC manufacturing factories, equipment, and management. Below is a list of the talks:

1. "Cooperative Research and Technology Transfer;"
2. "Long-Term Partnering for Success-A Teamwork Approach for Positive Results;"
3. "Customer Vendor Partnership for Furnace Upgrade;"
4. "Bulletproofing New Product Fab Implementation;"
5. "A Virtual Factory-Based Environment for Semiconductor Device Development;"
6. "Comparison of Statistically-Based and Neural Network Models of Plasma Etch Behavior;" and,
7. "Object-Oriented SECS Programming System."

Talk number six (above) on neural network models was particularly interesting. The motivation behind using such models was based on the fact that the practical plasma processes at the equipment level are presently beyond theoretical comprehension. Hence to model plasma etch behavior, a six input parameter, feed-forward error back-propagation (FFEBP) algorithm was employed. The results were compared to the traditional, statistically-based plasma etch models involving Response Surface Methods (RSM). The neural networks proved to be more accurate with faster run times, using fewer data points

for training. Furthermore, neural networks customized for a particular application yielded more optimal performance.

The vision seminar was more technically oriented, yet very applicable to the envisioned factory-of-the-future. Vision in machines will assist in automated manufacturing, alignment requirements, defect testing, sorting needs, process control, etc. Since this was the first seminar on the topic, most of the talks were fundamental in how machine vision is attained and processed. The final talks included a demonstration, and applications of vision in manufacturing yield, wafer alignment, inspection, and optical character recognition (OCR). The talks are listed below:

1. "Lighting and Optics Techniques;"
 2. "Vision Sensors and Cameras;"
 3. "Machine Vision Algorithms;"
 4. "Workshop: A Demonstration of Machine Vision Applications in Semiconductor Manufacturing;"
 5. "Machine Vision in Semiconductor Manufacturing, A Six-Sigma Approach;"
- and,
6. "Machine Vision Techniques for Wafer Alignment, Inspection, and OCR."

The exhibition was large, encompassing the entire Moscone Center. Most of the exhibits were U.S. The areas included gases and chemicals; test and handling equipment; front-end equipment; plat-panel displays; among others. Everything from MCM pick-and-place machines to complete mini-fabs with two day turn-around times were displayed. Overall, I got the impression that each manufacturer is pursuing their own work towards future-factory needs; however, with the absence of, for example, equipment interface standards, equipment is not compatible with each other. Clearly to minimize costs, shorten development times, and permit multi-vendor compatibility partnerships need to be fostered as well as national equipment standards and benchmarks. Nevertheless, exciting progress is being made in manufacturing equipment to address tomorrow's needs.

FACSIMILE COVER SHEET

TO: Dr. Arati Prabhakar - DARPA
Mr. Dan Butler - Booz-Allen & Hamilton

FAX: 703-696-2201 - DARPA
703-525-3754 - BA&H

FROM: Graydon Larrabee

FAX 214-980-7224

RE: SEMICON West Trade Show

Overall, this was one of the best and most professional quality SEMICON West shows I have attended.

This was certainly the year of the MESC standards cluster tool. Two new cluster tool systems from CVC and PMT were on the floor. Both used the Brooks Automation central handler. The PMT system will be marketed in Japan by Cannon and one other Japanese company. Watkins Johnson had their MESC compatible cluster tool on the floor. Novellus does not exhibit at the show but was taking customers to their plant to see their cluster tool. Bob Therrien, CEO Brooks Automation, is talking with LAM and Genus to use his central handler for their cluster tools. He was very optimistic. Bob indicated that MRC had sold two PVD cluster systems; they use the Brooks handler also. AG associates (RTP house that merged with RAPRO) were pushing MESC compatible process modules.

TIN, a research house in San Francisco indicated that the cluster tool market was \$1.04 billion in 1991 and would grow to \$3.6 billion in 1996 - a 28.2% CAGR! Dan Hutchison at VLSI research forecasts that PVD cluster tools will grow at 26.5% CAGR reaching \$1.5 billion in 1996.

2 PAGES, INCLUDING THIS ONE

Nikon and Canon disclosed plans to begin shipping their phase-shift illumination system i-line steppers. This will extend resolution to 0.35 microns and will improve depth of field. The Canon stepper also has a 22mm square field and a new focus and levelling system. These announcements are important because it means phase shift masks and excimer laser steppers will have to wait for the 0.25 micron technology node. I'm not sure what effect this will have on GCA's competitive stance.

There were vendors of process control sensors and software at the show for the first time. SITE Services Inc has an impressive "develop end point control" sensor and software system. They claimed it was being used on the SVG tracks. I encouraged them to look at using the sensor for other thin film work and they indicated they'd be thinking about it. I've requested literature from a number of vendors.

SEMATECH's first spin-off company - Fourth State Technology Inc was at the show. Terry Turner (a TI assignee) has formed the company. They have a line of sensor-based equipment that monitors plasmas. The product bypasses the usual local matching network that monitors power, and places the monitoring device in situ.

Regards

A handwritten signature in cursive script, appearing to read "Graydon", written in dark ink.

FACSIMILE COVER SHEET

TO: Dr. Arati Prabhakar - DARPA
Mr. Dan Butler - Booz-Allen & Hamilton

FAX: 703-696-2201 - DARPA
703-525-3754 - BA&H

FROM: Graydon Larrabee

FAX 214-980-7224

RE: SEMI Standards Activities, June 15-18th San Francisco CA

I attended SEMI meetings and participated in three standards activities. Alan Weber and I are technology architects for the SEMI U.S. Regional Integration Division. We both made presentations; mine emphasized technology trends and standards needs in the areas of process control, micro environments and CFM. The reaction from the attendees was "WOW that's an enormous amount of work!". There is going to be a lot more education and interacting to be done here. Alan and I are going to cooperate in this activity. Jim Greed is the division chairman and indicated that this was exactly what he wanted.

Technology architects are being assigned to all SEMI divisions. Allen and I have been asked to coordinate their technology forecasting activities and standards recommendation activities. I will work with Allen through SEMATECH.

I attended a new committee being formed to set standards for sub-0.1 micron particle manufacturing. This did not go well at all. There was a surprising lack of knowledge of the technical problems involved with sub-0.1 micron particle detection and how it relates to manufacturing. I've decided to let this committee churn for a while because several attendees (equipment vendors, standards vendors) had a number of hidden agendas; they want business, development \$\$ etc. I'm not sure this committee will get off the ground.

Regards



1 PAGES, THIS ONE

FACSIMILE COVER SHEET

TO: Dr. Arati Prabhakar - DARPA
Mr. Dan Butler - Booz-Allen & Hamilton

FAX: 703-696-2201 - DARPA
703-525-3754 - BA&H

FROM: Graydon Larrabee

FAX 214-980-7224

RE: ISMSS Meeting, June 15-16th, San Francisco CA

Overall, this year's meeting was not as good as other years. One of the problems was the lack of international speakers for This "International SMSS"! It was too focussed on U.S. activities.

Jim Morgan, CEO of Applied Materials (AMAT) gave the keynote address. I have attached two of his charts showing the AMAT view of where the industry is going. He pointed out the AMAT has shipped over 850 multi chamber systems. Sam Wood asked him about the MESC cluster tool standards and Morgan gave the standard company response that they were the standard! He made it clear that partnerships on process modules were expensive and AMAT needed up front money to pay for the interfacing. A complaint on AMAT's unwillingness to work in partnerships was answered by "use SEMATECH or SRC!". Morgan sees the following trends in equipment prices, MTBF and R&D costs relative to 1981-85:

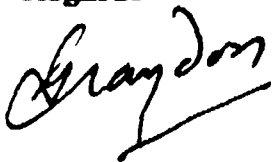
	1981-85	1986-90	1991-95
Equip prices	1	2-3	3-4
MTBF	---	~100 hrs	250 hrs
AMAT R&D	\$105M	\$270M	\$610M

4 PAGES, INCLUDING THIS ONE

Don Rose, Intel, discussed "Productivity Enhancement". He argued that yields were now high enough that new ways to enhance productivity needed to be found. The capital costs for 64Mbit technology node will be \$120k per one wafer start per week (WSPW). This will rise to \$240k for the 256Mbit. He wants to run equipment at 90% utilization and we will need a 2X improvement over the next few years. He "doesn't mind paying 2X for equipment if 2X output can be obtained". He was very negative on cluster tools claiming their throughput was just too slow. He was also negative on in situ metrology for process control. He wants equipment throughput of "60 to 90 to 100 wafers per hour"!

There were two good real time process control papers. One of Emanuel Sach's students described an adaptive model based control methodology for silicon epitaxy. One of Costos Spanos' students described feed-forward control of a lithography stepper. Mark Conner at Booz-Allen has copies of the charts. You should take a few minutes to review them. I asked Costos to join us at the July 15th DSRC Process Control workshop.

Regards

A handwritten signature in cursive script, appearing to read "Graydon", with a horizontal line underneath.

CONTAMINATION IN THE M-BIT AGE

Items	1989	1990	1991	1992	1993	1994	1995	1996	1997	1998	1999	2000
Device (Dram Mass Production)	1M			4M			16M			64M		
Design Rules	1.2 ~ 1.0 μ m			~0.8 μ m			0.6 ~ 0.5 μ m			0.4 ~ 0.3 μ m		
Water Size	6" ϕ			8" ϕ			8" ϕ			8-12" ϕ		
Defect Size	0.1 μ m			0.1 μ m			0.05 μ m			0.03 μ m		
Defect Density	0.04/cm ²			0.04/cm ²			0.02/cm ²			0.01/cm ²		
Cleanroom Class	Class 10 (0.1 μ m)			Class 1 (0.05 μ m)			Class 0.1 (0.02 μ m)					
(Wafer Process Zone)	Temperature $\pm 0.1^{\circ}\text{C}$			Clean Inert Gas Atmosphere Purity 99.9999%								
Filter Capability	0.1 μ m Filtration >99.9999%			0.05 μ m Filtration 99.9999%			0.02 μ m Filtration 99.999999%					
Processing System Cleanliness	0.2/cm ² (0.1 μ m) Outgas 1ppm			0.01/cm ² (0.05 μ m) Outgas 1ppb			0.005/cm ² (0.02 μ m) Outgas 10ppt					
Ultra Pure Water	18M Ω , cm 0.5/cc (0.2 μ m)			18.25M Ω , cm 10/A (0.05 μ m)			18.25M Ω , cm 1/A (0.03 μ m)					
Ultra Pure Gas	99.999999% Moisture 100ppb			99.999999% 100 ~ 10ppt			99.9999999% 10 ~ 0.1ppt					

2M153-06/E2673.06

Source: MITI



INCREASING SYSTEM VALUE

Issues	1981 - 85	1986 - 90	1991 - 95
Configuration	Stand Alone Batch	Multichamber S-W	Integrated Cluster
Control	Manual	Microprocessor	Host Computer
Communications	Display	SECS I & II	Real Time
Material Handling	Manual	Automated, Cassette to Cassette	Factory Automation (AGV)
Wafer Size	4-6 in.	6-8 in.	8-12 in.
Contamination Specs	None	Particles	Particles, Organics and Heavy Metals
Process Specs	Catalog	Customer Specific	Co-Development
Safety	UL - Shock, Noise	Regional, Customer's	Environmental
Service	Standard Service	Tailored Support	Equipment Partnership
MTBF Specs	---	~ 100 Hours	250 Hours
Infrastructure	Regional	International	Global
Total AMAT R&D Expenditure ('000)	\$105,000	\$270,000	\$610,000 (Est.)
Equipment Price (Normalized)	1	2-3	3-4

2M153-16/E2673.16

FACSIMILE COVER SHEET

TO: Dr. Arati Prabhakar - DARPA
Mr. Dan Butler - Booz-Allen & Hamilton

FAX: 703-696-2201 - DARPA
703-525-3754 - BA&H

FROM: Graydon Larrabee

FAX 214-980-7224

RE: 11th Annual Dataquest Seminar, June 17th - San Francisco

The agenda for the seminar is attached. I have copies of all the charts and can make copies for you if you want any of them.

Peggy Wood did an excellent analysis of the equipment market trends, particularly for the Japanese market. 1991 Japanese company share of wafer fab equipment is shown in the second chart. Peggy pointed out that the U.S. is still a major supplier of CVD and PVD equipment to Japan. She argues that the U.S. increased its market share in Japan because the Japanese have been switching their fabs from dRAM's to logic and this drives CVD and PVD sales. Also, these systems are single wafer processes which lowers throughput and means more CVD and PVD systems for line balancing. Her argument is supported by decreased stepper and track sales in 1991. Peggy feels the 1991 increase in U.S. share is not a trend (possibly an anomaly from the dRAM to logic shift in Japan). She forecasts that 16Mbit dRAM equipment sales will occur in 1993. Overall she feels 1992 equipment sales will be down 10 to 14%. The attached escalating wafer fab equipment costs chart shows a continued 11% to 24% increase per year, which is a concern for all of us.

Joe Grenier did financial benchmarking of U.S. equipment manufacturers. He admitted that he had little data on Japanese equipment manufacturers. Looking at normalized sales growth since 1982 shows worldwide industry growing 4X, U.S. companies 2.8X and Japanese companies 9X !! Applied material grew at a healthy 7X, outperforming all U.S. companies. However, when sales growth were normalized to 1988; Novellus outperformed all U.S. companies at 3X while Applied Materials was with other U.S. companies at 1.2X (see charts).

~~9~~ PAGES - INCLUDING THIS ONE

10

As shown in the chart on capacity utilization, there is an enormous overcapacity for 4 Mbit dRAMs. This has delayed 200 mm fab plans in Japan (see chart). The percentage of fabs still using 4 inch is too high in the U.S. and Europe to be competitive. Also, the U.S. is lagging in the move to large-diameter wafers (see chart on large diameter).

A new analyst (new to me) Lane Mason, discussed "The 1 Gb DRAM: ROI or RIP" (RIP means rest in peace here). He was simply wrong! He does not understand the dRAM market. He could not even answer a question on whether development costs or fab costs were increased faster! I was sitting next to Jacques Vuye (manages Intel's competitive intelligence activities) and he agreed with me.

Jacques offered to help us (DARPA and myself) by supplying competitive intelligence, industry trends etc. I intend to take advantage of the offer because Intel, under Jacques' guidance has a world class competitive intelligence activity. He is concerned, as I am, about SEMATECH's competitive intelligence activities. He is sending a "strong analyst" to join the SEMATECH group July 1st (last name is Kim).

Let me know if you want copies of these or other charts.

Regards

A handwritten signature in cursive script, appearing to read "Graydon".

BOOZ, ALLEN & HAMILTON Inc.
Defense Technologies Division

MEMORANDUM

Ballston
3 June 1992

To: Dr. Andrew Yang
DARPA/MTO

From: Kurt Hinds ^{PH}

Subject: Martin Marietta's TOPS Pattern Recognition Systems Design Review
(SDR) Trip Report

Martin Marietta's Systems Design Review (SDR) for the TOPS Pattern Recognition program took place on 28 May 1992 in Denver, CO. Attendees included Scott Lindell, Mike Henry, et. al. from Martin; Joe Horner from Rome Lab; Bill Friday of MICOM; as well as representatives from HDL and the USAF.

Martin's goal is to develop a flyable 2-D optical correlation system for pattern recognition, the System for Passive Optical Pattern Recognition or SPOTR. Martin has chosen the FOG-M's mission profile as the basis for the SPOTR performance requirements; in addition, demonstrations are to take place aboard a UH-1 helicopter, therefore the helicopter environment dictates the SPOTR's physical requirements (size, environment). Martin has studied and modeled the missile profile to generate the pertinent system requirements; i.e. latency, throughput, location accuracy, probability of recognition, and false alarm number. These requirements have been spelled out in the "SPOTR Requirements Document, May 1992." The physical requirements for the SPOTR (for all the optics, hardware, and power) are: less than 1 cubic foot (space), less than 40 pounds (weight), and less than 150 watts (power dissipation). These figures are not TOPS requirements. These requirements do relate to a possible spinoff program to take place at Eglin. However, for TOPS, meeting these figures would be desirable, though not crucially necessary. Scott Lindell stated that absolutely no extra effort or funds would be expended to reach the aforementioned physical goals. Justifications for the system requirements were presented at the review and appear to be in order; actually the system location goal has been reduced from 1 foot down to 15 centimeters.

On two occasions, October 1991 and March 1992, Martin gathered image data at MICOM's test range. MICOM's Remote Seeker System (RSS) missile and cameras were used for the data collection and will be used for the demonstration. The final demonstration is to take place with the same configuration as the data collection

scenarios. A question was raised regarding how difficult would it be to adapt the SPOTR to another target, say a T-72 tank? Image data (comprehensive) would be required in order to generate the appropriate filters; however, this filter generation process is not terribly time consuming (approximately several minutes per filter with current processing). Therefore, the complete filter generation process for a new target could probably be accomplished within about a day's time.

Bill Friday is coordinating with Martin for the use and scheduling of facilities at MICOM. Friday stated that the field demo (helicopter) could be run at faster than the 40 knots used for the data collection in order to induce faster processing. Martin rejected this option claiming 70 knots versus 40 knots would change little in terms of the processing required. In addition, at 40 knots during the data collection, they experienced some resonant effects which Martin believes ironically induced harsher environmental effects on the equipment. Therefore, it appears 40 knots will be the demo speed of the helicopter.

Program Manager Scott Lindell presented his program risk assessment. The key concern at this time is the Spatial Light Modulator (SLM) performance and availability. Martin is considering up to five options for the SLMs. A ferroelectric liquid crystal (FLC) and magneto-optic spatial light modulator (MOSLM) are the two primary devices under consideration. In addition, Martin also has and may consider a liquid crystal light valve (LCLV) and an LCTV. A final option is a deformable mirror device (DMD). Martin does not have a DMD to evaluate. Joe Horner from Rome Lab stated there is perhaps a 50/50 chance that a DMD from Texas Instruments may be available sometime this summer. Nonetheless, the performance and availability of the SLMs is Martin's chief concern. Martin is looking toward an August decision time to specify their SLM choice. The next most pressing concern for Martin in terms of programmatic risk is the induced environment (heat, crosstalk, EMI, etc.) on the compact correlator. This issue has not been addressed yet, though it will be studied soon. Regarding the high speed 2-D detector array, Martin's studies are leaning toward Dalsa's 128x128 array; however, there has been significant lag time in getting the Dalsa arrays. Joe Horner asked whether the Sematex 256x256 array had been ruled out. Martin has been unsatisfied with the performance of the Sematex device due to significant design flaws. Martin's plan is to go with the 128x128 array, although it would not be difficult to jump up to a 256x256 device should an acceptable array become available.

In summary, Martin Marietta's Pattern Recognition program appears to be on track, though the SLM issue could prove to be troublesome. I also perceive that Martin is making a concerted effort to consider and "market" this pattern recognizer beyond what is expected for the TOPS program (the Eglin effort as an example). No specific action items are pending.

BOOZ, ALLEN & HAMILTON Inc.
Defense Technologies Division

MEMORANDUM

Ballston
5 June 1992

To: Dr. Andrew Yang
DARPA/MTO

From: Kurt Hinds k^{mh}

Subject: General Electric's TOPS Null Steering Processor Third Status Meeting
Trip Report

General Electric Co.'s third status meeting (~one year of work) for the TOPS Null Steering Processor took place on 21 May 1992 in Syracuse, NY. Attendees included Dan Friedman and staff from GE and Jim Davis, Brian Hendrickson, and others of Rome Lab.

GE's goal is to design, build, and demonstrate a ruggedized acousto-optic multiple sidelobe canceller for radar jamming in a multipath environment. Program manager Dan Friedman summarized GE's achievements on the Acousto-Optic Null Steering Processor (AONSP) to date:

- After analyzing several alternate architectures, the baseline architecture still corresponds to the original.
- Preliminary simulation runs indicate that the top-level performance goals are achievable.
- Early component evaluation and studies indicate that the Bragg delay lines and integrators will be the limiting items for the AONSP.
- Design Plan has been submitted to Rome Lab; Annual Summary Technical Report is in progress
- Program is essentially on schedule; funding is OK through the year

Friedman discussed several specific accomplishments:

- Top level requirements have been established.
- Measurements and studies of the critical components (laser(s), Bragg cells, integrator, detector) are in progress, some early data has been reported.
- Photorefractor enhancement mode testing is underway at Rockwell.

- Simulation code is in checkout (with primitive jamming signals), has provided preliminary performance data.
GE stated a need to accelerate these tests; they are looking into several options to access and use a more powerful, parallel processor to expedite this process.
- Under this contract, the demonstration will take place in the lab.; demos with actual radars will require follow-on.

Regarding the critical components studies, Paul Ruterbusch of GE detailed the current status. For the laser source, the key concern is operation with very low noise characteristics. GE is currently evaluating candidates from A-B Laser, AMOCO Laser, COHERENT Laser, and SPECTRA-PHYSICS Laser. Although more tests are to be run, the preference at this point is the product(s) from COHERENT (50 mW available now, 100 mW planned for end of 1992, 250 and 500 mW planned for 1993+).

GE has obtained the results of a Bragg cell materials evaluation study by Harris Corp. and is awaiting another study by P. Banerjee of UAH. The Harris study rated Pb_2MoO_5 , GaP, and TeO_2 highly. GE is concerned about the availability of Pb_2MoO_5 and is thus leaning toward using TeO_2 . The buy decision will be made after consideration of both of the aforementioned reports.

For the integrator, GE is considering Rockwell's photorefractor and liquid crystal light valves (LCLV) from Hughes, Control Optics, and Seiko Instruments. One concern raised was the effects of aging on the Hughes LCLV under evaluation; apparently leakage on the edges results in reduced usable area.

Finally, many detector vendors have been contacted. Photo-multiplier tubes (PMT), avalanche photodiodes, and PIN photodiodes are being pursued. The leading candidate at this point is a PIN photodiode.

Attached on the following page is a summary of the status of the critical components.

GE's program is well-organized and methodical. No major concerns arose from this status review meeting. No specific actions items are pending.



CONCLUSIONS

GE Aerospace
O&RSD

LASER

Good candidates that should meet the AONSP requirements if they scale with power
Need to test and verify performance of higher power lasers

BRAGG CELL

Need to purchase Bragg cells and test

INTEGRATOR (LCLV)

Preliminary evaluation done

Need to optimize electronics drive and finish evaluation of present LCLV's
Need to compare results against other LCLV's (Control Optics) and the photorefractor

DETECTORS

Have good candidate detector

Need to test and verify performance in heterodyned test configuration
Should pursue alternative vendors

BOOZ, ALLEN & HAMILTON Inc.
Defense Technologies Division

MEMORANDUM

Ballston
29 June 1992

To: Dr. Andrew Yang
DARPA/MTO

From: Kurt Hinds

Subject: Hughes Aircraft Co.'s TOPS Optical Control of Phased Array Preliminary Design Review Trip Report

Hughes Aircraft Co.'s Preliminary Design Review (PDR) for the TOPS Optical Control of Phased Array occurred on 9 & 10 June 1992 in Fullerton, CA. Attendees included J. J. Lee and staff from Hughes Ground Systems Group (GSG); H. W. Yen, Willie Ng, and Greg Tangonan from Hughes Research Lab (HRL); and Brian Hendrickson, Norm Bernstein, and Don Hildebrand of Rome Lab. A copy of the attendees list is attached.

Ray Tang of Hughes GSG opened the review by pronouncing the program ahead of schedule and under budget. Tang also mentioned several possible systems for the optically controlled phased array. The Army's Ground-Based Radar (GBR) (X-band) could benefit from improved discrimination of warheads versus decoys. The GBR is a program that was previously cut, but is now part of SDI; it is envisioned as a replacement for the Patriot. The GBR, with 1 (to perhaps 2) GHz instantaneous bandwidth, is planning the use of switched coax delay lines. Using photonics is under consideration, though photonics is viewed as being a very new method of implementing the time delays for the phased array. Other possible applications are with multifunction radars for search, track, fire control, and/or ECM missions that require wide instantaneous bandwidth. Hughes has had contact with SDC in Huntsville regarding the multifunction radars.

J. J. Lee, Program Manager, reviewed Hughes' objectives for the program:

- Develop optoelectronic components for phased array applications
- Apply photonic technology to enhance system performance of phased arrays
- Demonstrate the unique features of a photonic array antenna with:
 - wide instantaneous bandwidth
 - low loss for signal distribution
 - compact, flexible feed network

Hughes' specific goals are:

- Design, develop, fabricate, and test a fully functional 2-D conformal array consisting of 24 X 4 wideband elements
- 24 channels divided into 8 subarrays with each channel controlled by an 11-bit time shifter (5 bits photonic and 6 bits electronic)
- Capable of transmitting and receiving over ± 60 degree scan in the azimuth plane controlled by a true time delay network and RF/digital fiber optic links
- Operating at L-band from 850 to 1400 MHz over a ~50% bandwidth

Hughes did not have a specific radar system to design to, thus a study of radar parameters was undertaken to develop a sense of possible applications. Hughes has developed detailed parameters for both the 96 element test array (for demonstration) and an expanded system (5000 elements). The following potential applications resulted from the radar study:

- The time shifter beam steering design allows for use of high bandwidth waveforms for target decorrelation and subsequent non-coherent integration to obtain benefits of Swerling II amplitude statistics.
- The design allows for coherent processing of long dwell waveforms to obtain super range resolution (from high bandwidth waveforms) and two-dimensional imagery (range and doppler).
- Distribution of the receiver into the antenna via the T/R modules provides for the possibility of performing digital, adaptive beam forming for ECM cancellation purposes.

J. J. Lee reviewed the photonic array analysis. Hughes concluded that for the 96 element array a time shifter with 7-8 bits was required. However, it was deemed not sensible to implement that many bits with fiber optics (losses too high). Thus a compromise was hatched - 5 bits optically and 6 bits electronically. Hughes time shift delay implementation is computationally superior to a phase shift delay approach. Brian Hendrickson reminded Hughes that the demonstration system is not a truly viable system and that Hughes needs to address issues related to real systems in the course of their design. Hendrickson also raised the possibility of using waveguide detectors (under development at HRL for Rome) instead of the electronic time delays prescribed for the TOPS program. This could provide an all-optical implementation. J. J. Lee promised to consider this option within his current technical and time considerations.

H. W. Wen of HRL presented an overview of the photonic time-shifter development. Hendrickson expressed a concern that the photonics developers are not providing the radar designers with the proper design data. Bob Loo, also of HRL, briefed the 5-bit optical delay module design. Some discussion on the laser source took place. Hughes intention is to use lasers from Seastar of Victoria, BC. Seastar has modified Mitsubishi lasers. Hendrickson is concerned about whether Seastar is a reliable source and how the laser may affect the radar design (dynamic range, noise figure). He suggested Ortel's 10 GHz laser as an alternative. Hughes seemed reluctant due to high cost and Hendrickson stressed that Hughes should not allow cost to be the overriding concern on the optics portion of this system.

In summary, to paraphrase Brian Hendrickson's assertions, the antenna/radar design appears on track, but the optics portion is iffy. Hendrickson stressed to Hughes the need to remember to emphasize the photonics! Dialogue among the GSG staff and HRL staff needs to improve.

As for interim demonstrations, Hughes believes a laboratory-type demo is possible at CDR, scheduled for March 1993.

BOOZ, ALLEN & HAMILTON Inc.
Defense Technologies Division

MEMORANDUM

Ballston
6 August 1992

To: Dr. Andrew Yang
DARPA/MTO

From: Kurt Hinds

Subject: Texas Instruments TOPS Optical Time Delay Networks for Phased Arrays
Program Review Trip Report

Texas Instruments (TI) held their Program Review for the TOPS Optical Time Delay Network (OTDN) for Phased Arrays on 14 and 15 July 1992 in Dallas, TX. Attendees included Program Manager Chris Hemmi, Carl Takle, Greg Magel, Mark Boysel, et. al. from TI and Brian Hendrickson, Norm Bernstein, Richard Payne, et. al. from Rome Lab.

TI briefed both the TOPS OTDN program as well as Rome Lab's related Optical Time Shifter Network (OTSN) program which is a risk reduction study for the OTDN. The OTSN's goal is to demonstrate the micromechanical membrane routing switch that is to be incorporated in the OTDN. An issue arose over the OTSN study. Due to a lack of personnel availability, the OTSN study completion is to be delayed from Sept 92 to approximately Feb 93. B. Hendrickson is concerned about this negatively impacting the OTDN schedule. TI acknowledged Hendrickson's concerns and have promised to diligently avoid any delays.

TI's OTDN program objective is to develop a compact optics network to improve the instantaneous bandwidth performance of large active electronic steerable arrays (AESAs). The frequency band for the phased array is 2-4 GHz. The time delay network is to be a silicon photonic integrated circuit with polysilicate glass (PSG) optical waveguides, micromechanical membrane switches, and 11 bits of delay. TI's demonstration array will consist of 16 x 4 elements with +/- 60 degree scan.

TI is reporting an expected 58-64 dB insertion loss at this time. This is deemed unacceptable (~30 dB off target) for the demonstration. Discussion at the review provided the consensus that a hybrid approach (optical and electronic delay) is the preference over a poor all-optical delay demonstration. B. Hendrickson suggested considering other options; for instance, using GaAs time delay networks for the smaller delays may be necessary as a compromise. TI is to take this under consideration. (See attached chart)

Regarding an interim demonstration, TI believes their prototype network chips will be completed and ready for demo around October 1993.

OPTIONS FOR REDUCED INSERTION LOSS

- **SCALE BACK TO 9-BIT NETWORK**
 - MATCHES 16 ELEMENT ARRAY REQUIREMENTS
 - REDUCE OPTICAL LOSSES 3-4 dB, INSERTION LOSS 6-8 dB
- **IMPLEMENT SMALLER DELAY BITS IN GaAs MMIC**
- **IMPROVE RF-OPTICAL-RF CONVERSION LOSS OR LASER TOI**
- **REDUCE OPTICAL LOSS**
- **PARTITION OTDN INTO TWO NETWORKS WITH INTERMEDIATE OPTICAL OR ELECTRONIC AMPLIFICATION**

APPENDIX 2

**SPECIAL CONSULTANT
DELIVERABLES**

APPENDIX 3

VIEWGRAPHS AND BRIEFINGS



MICROELECTRONICS MANUFACTURING PROCESSING AND EQUIPMENT

May 21, 1992

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**DARPA and SEMATECH
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5/21/92

MICROELECTRONICS MANUFACTURING PROCESSING AND EQUIPMENT

Goal: To establish ULSI process capabilities, real time process controls and an equipment base for low cost flexible semiconductor manufacturing

Critical Elements:

Process Control

In-situ process control
In-situ inspections
Physical process models

Process Capability

Streamline process
5 layer interconnect
Full planarization

Process Tools

Model based designs
Wide process latitude



MICROELECTRONICS MANUFACTURING PROCESSING AND EQUIPMENT

ULSI STREAMLINE PROCESS

Parameter	Conventional CMOS	MMST 4K Demo	MMST 1000 Wafer Demo (FY 93)	ULSI Streamline Process
Minimum CD (microns)	0.5	0.6/0.35	0.35/0.25	0.18
Interconnect metal	2/3 layer	2 layer	2 layer	5 layer
Mask levels	14	13	13	10
Implant steps	10	9	9	2
Inspect steps	50	30	13	0
Wet steps	25	34	29	0
Total steps	250	180	158	<100



MICROELECTRONICS MANUFACTURING PROCESSING AND EQUIPMENT

TASK / SUBTASK GOALS

Task	Subtask	Current State of the Art	Result Of This Program
Real Time Process Control	Process control	End point detection	Complete in-situ product level control
	Inspection	Off line/look ahead wafers	In-situ inspections
	Process models	Ex-situ inspection	Integrated CIM feedback
ULSI Process Capability		Empirical	Physical
	Process sequence	200-300 steps (30% wet)	<100 steps (all dry)
	Interconnect Planarization	3 Layer Local Mechanical/chemical Ion implant	5 layer / multiple ground Full wafer Planar depositions Plasma deposition
Tool Synthesis	Dopant		
	Design	Empirical	Process model based synthesis
	Functional	Batch Narrow process capability	Single wafer Wide process latitude



MICROELECTRONICS MANUFACTURING PROCESSING AND EQUIPMENT

KEY PROCESS AREAS MMST CLUSTER TOOLS CONVENTIONAL TOOLS

Rapid Thermal Process
LPCVD
Oxidation
Anneal

Etch Process
Patterned
Strip

Photoresist Process
Develop
Silylation

Non LPCVD
PECVD
Sputter

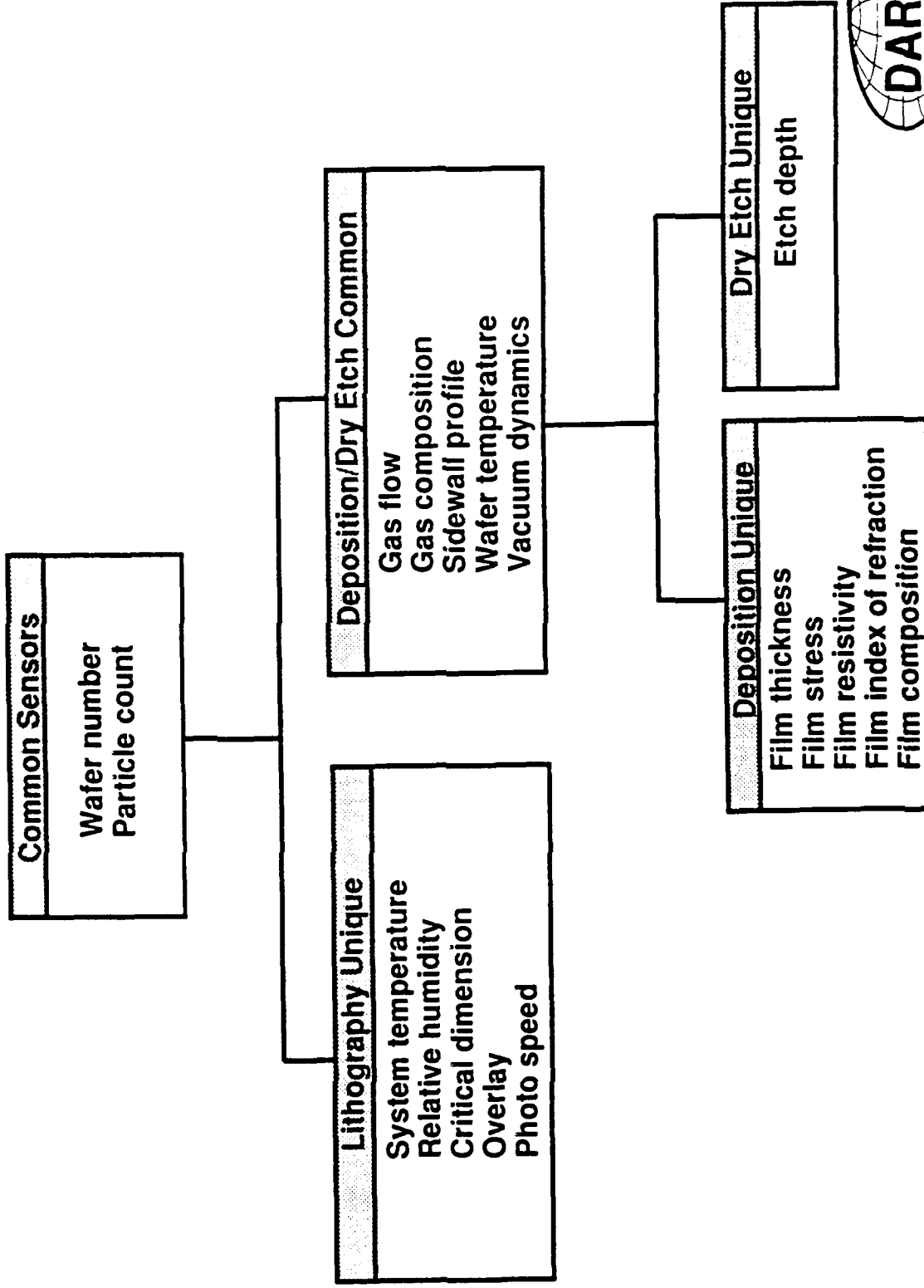
Ion Implant
Implant

Wet Process
Clean steps
Particle removal

Lithography
Coat
Expose
Conventional develop



MULTIPLE APPLICATIONS OF IN-PROCESS SENSORS



COMMENTS ON SEMATECH PLANNING CONFERENCE PRESENTATION OF APRIL 23 - 24, 1992

Program	Emphasize	De - emphasize
FURNACE & IMPLANT		
Furnace	RTP	Vertical furnace
Cluster tools	Single wafer gate stack	—
Rapid Thermal Process	RTP control	Selective Si (?)
Implant	Low cost cluster I ²	—
MULTI - LEVEL METALS		
Metalization > Dielectric	Alternative to CMP	—
Etch	Downstream etch In-situ characterization	—



RECOMMENDATIONS

FY 93

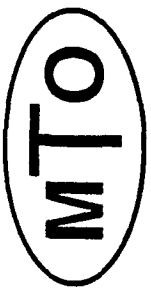
FURNACE & IMPLANT

New dopant incorporation techniques	1.0M
Cluster HIPOX development	0.5M
Standard RTP lamp subsystem	0.5M
Fundamental RTP thermal modeling	1.0M

MULTI-LEVEL METALS

Fundamental chamber modeling	2.0M
Cluster tool development	2.0M





CONTAMINATION FREE MANUFACTURING

May 21, 1992

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Program Manager**

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FAX: (703) 696-2201**

E-mail: zlemnios@DARPA.mil

5/21/92

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MICROELECTRONICS MANUFACTURING ULTRACLEAN SEMICONDUCTOR PROCESSING

Goal: To establish semiconductor manufacturing metrology, tools
and methods for zero defect ULSI components

Critical Elements:

Metrology

Particle detection
Particle removal

Chemistry

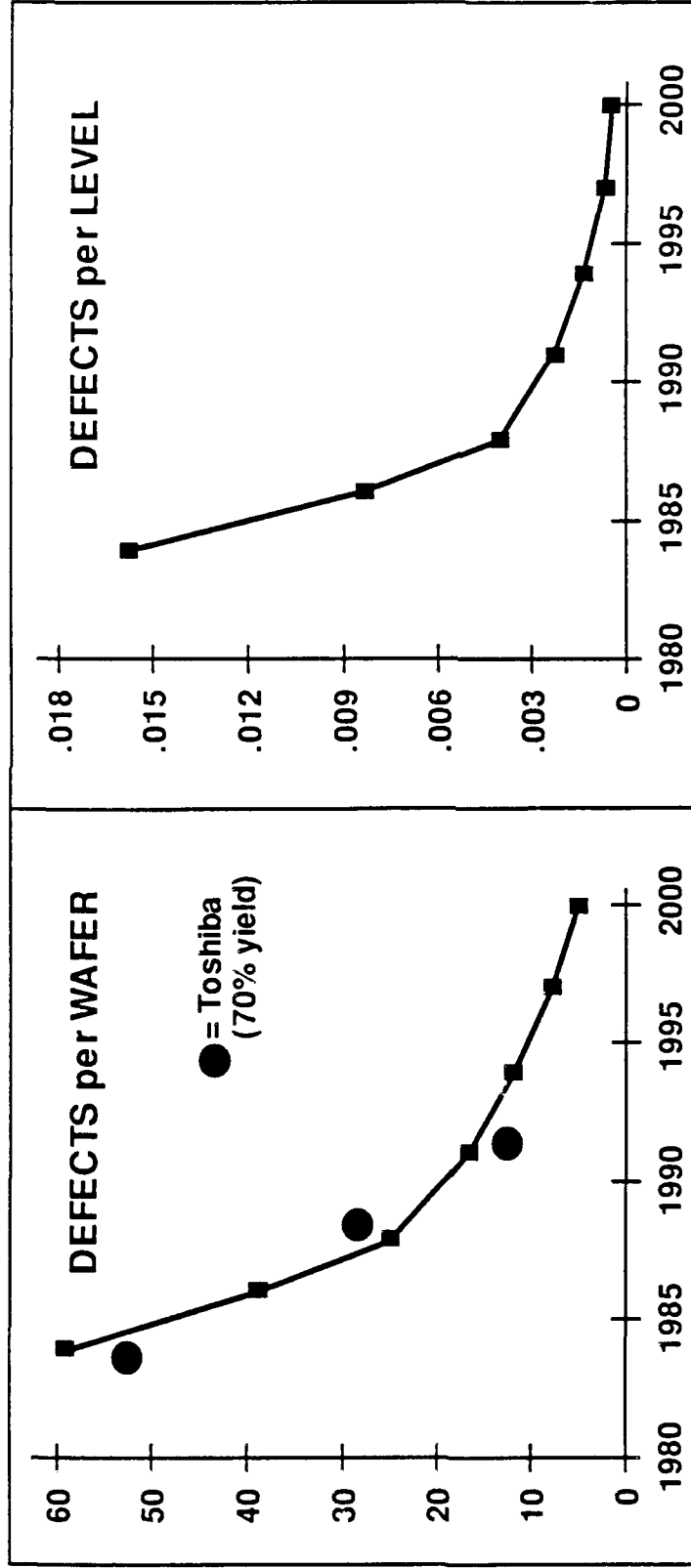
Point of use
PPT purity

Tools

In-situ clean



DEFECT REDUCTION TRENDS



Yield %	Year	Chip Size (CM ²)	Defect Density Defects/CM ²	Defects/ 200mm Wafer	Mask Levels	Defects/CM ² per Mask Level
90	1984	0.59	0.1883	59	12	0/01589
90	1986	0.9	0.1235	39	15	0.00823
90	1988	1.4	0.0794	25	20	0.00397
90	1991	2.0	0.0556	17	24	0.00231
90	1994	3.0	0.0370	12	28	0.00132
90	1997	4.5	0.0247	8	32	0.00077
90	2000	6.5	0.0171	5	32	0.00053



CONTAMINATION FREE MANUFACTURING

4

TASKS

1992 | 1993 | 1994 | 1995 | 1996 | 1997

ALL DRY PROCESS

pre-oxidation clean process



pre-gate clean (RCA clean replacement)



pre-implant clean



dry resist process (248-nm)



dry resist process (193-nm)



field oxide strip



STAND ALONE FACILITY

point of use chemistry / distribution



clean space (class 1K - 10K + portable class 1)



vibration solution



MICRO / MINI ENVIROMENTS

interface standards (mechanical / electrical)



CFM optimized microenviroments (wafer level)



CFM optimized minienviroments (tool level)



TOOL & PROCESS DEFECT ELIMINATION

material optimization (tribology, reaction)



contamination detection/ discrimination / elimination



in-situ tool cleaning



TECHNOLOGY DEMO



COMMERCIAL TOOL



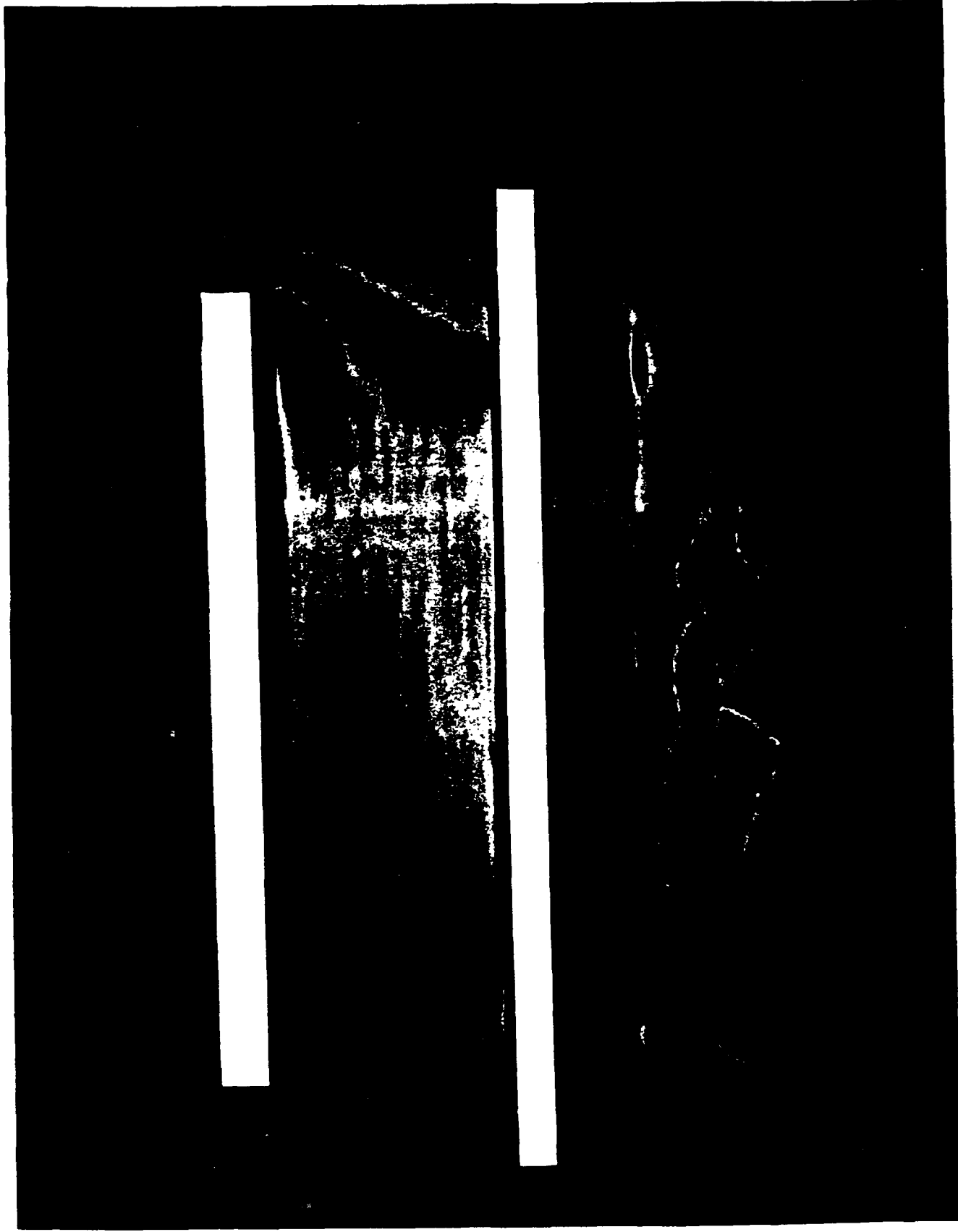
PRODUCTION USE

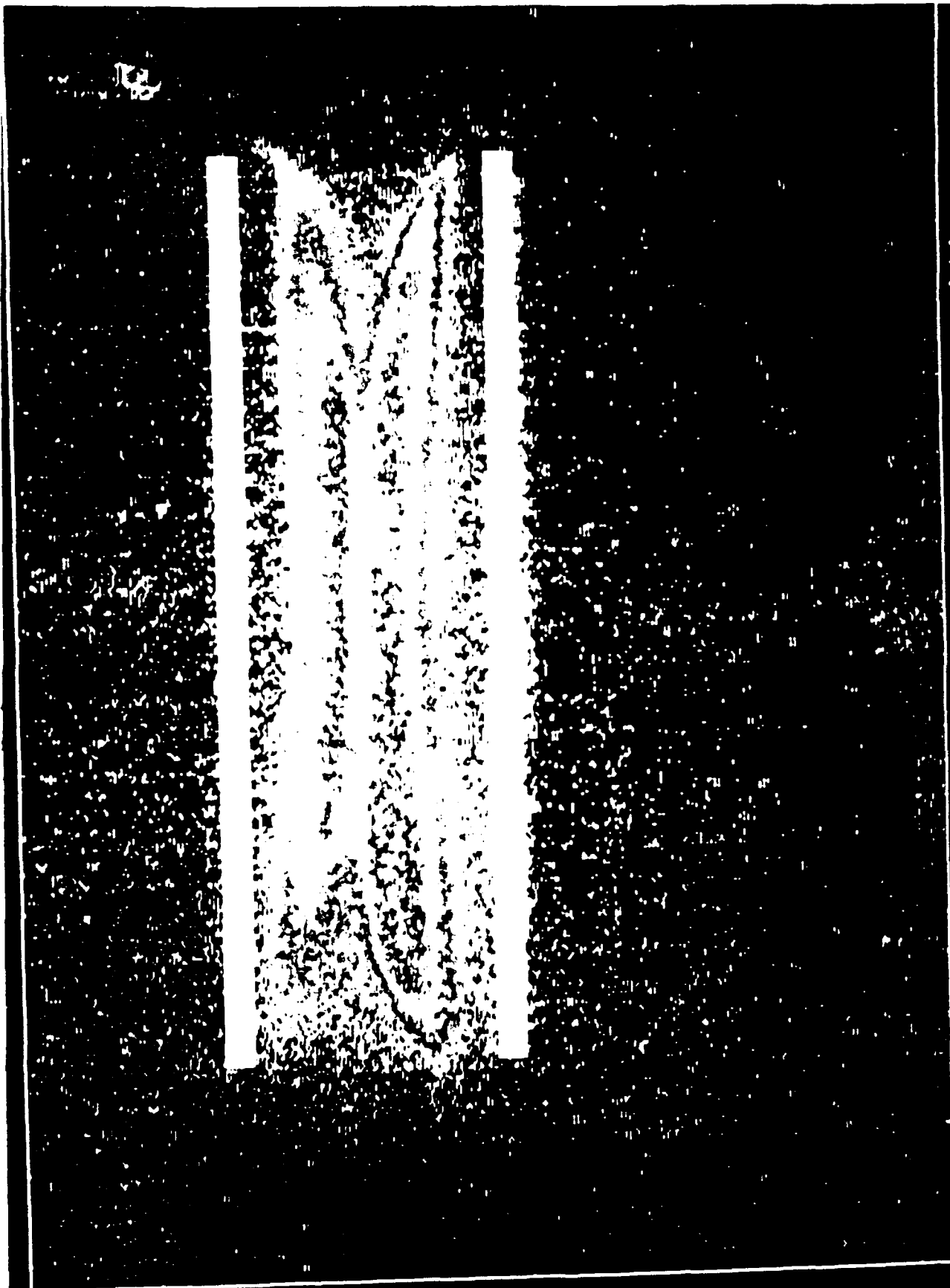


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5/21/92

Measured Cl Emission Line in DRYTEK Polysilicon Etch





Press button to make menu reappear at cursor position

MICROELECTRONICS MANUFACTURING ULTRACLEAN SEMICONDUCTOR PROCESSING

Task/Subtask Goals

Task	Subtask	Current State of the Art	Result of this Program
In-situ metrology	Data collection Data reduction	Manual inspection None	Automatic inspection CIM coupled
Point of use chemistry	Particles/ml Trace metallics Trace ionics Volatile contaminants	200 (0.50 μm size) 10^{10} atom/cm ² 0.01 ppb 0.01 ppb	<2 (>0.03 μm size) < 10^8 atom/cm ² <0.005 ppb <0.001 ppb
Gas distribution filtration & particle removal			
In-situ tool clean		Ex-situ mechanical clean	In-situ plasma clean
Wafer level particle detection and removal	Detection removal	0.25 μm particles N ₂ , wet strip	0.03 μm particles Laser, gas phase



COMMENTS ON SEMATECH PLANNING CONFERENCE PRESENTATION OF APRIL 23 - 24, 1992

Program	Emphasize	De - emphasize
1. Contamination Prevention and Reduction	In-Situ Detection Low PPT Detection Limits	None
2. Wafer Cleaning	Gas Based Cleaning	Wet Bench Equipment Megasonic Cleaning Immersion Cleaning
3. Materials Analysis and Improvement	Point-of-Use Liquids Improved MFC	SIMS/HIBS Development Liquid delivery system
4. CFM Research Center	*Defect Formation Plasma Dynamics Solid State Sensors *CFM beyond 2000 (R & D)	Megasonic Cleaning

* = New



RECOMMENDATIONS

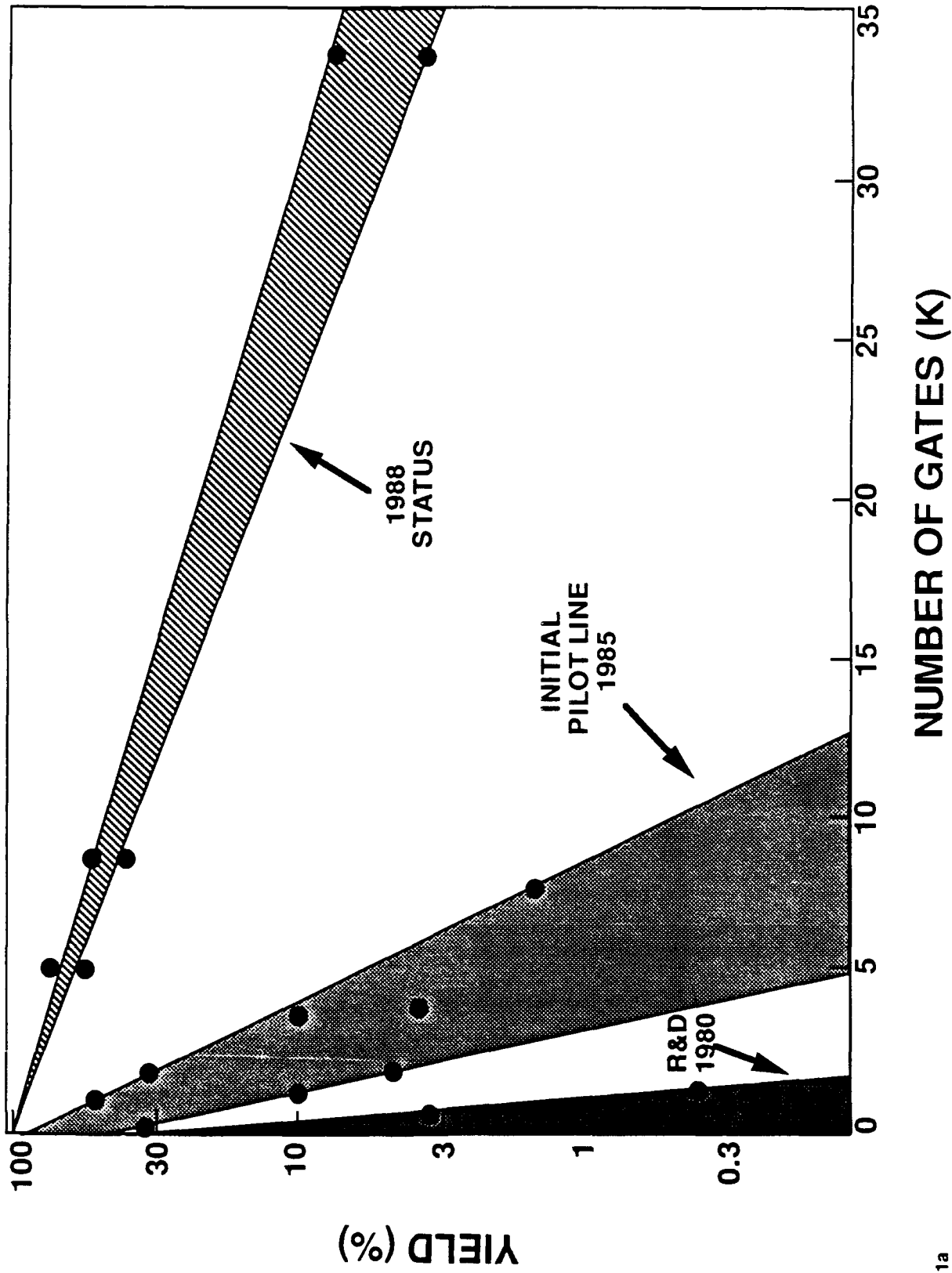
FY 93

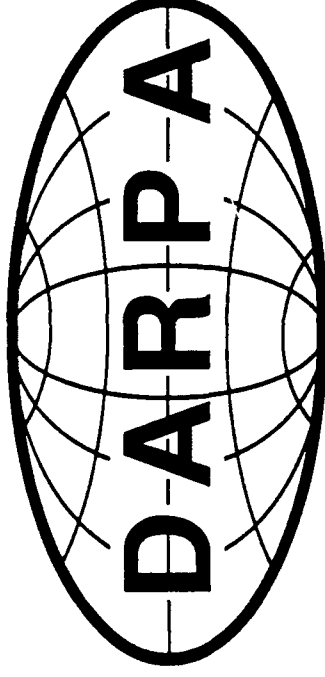
Greater emphasis on all dry processes Pre-oxidation clean Dry resists Field oxide strip	1.0M
Develop point-of-use chemistries Low particulate reactions Advanced filtering/metering	1.0M
Extend CFM Research Center Fundamental CFM modeling Advanced microenvironments In-situ process sensors	2.0M





DIGITAL GaAs YIELD VS. COMPLEXITY



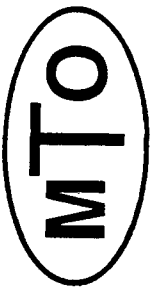


NEW STRATEGY FOR MICROELECTRONICS MANUFACTURING

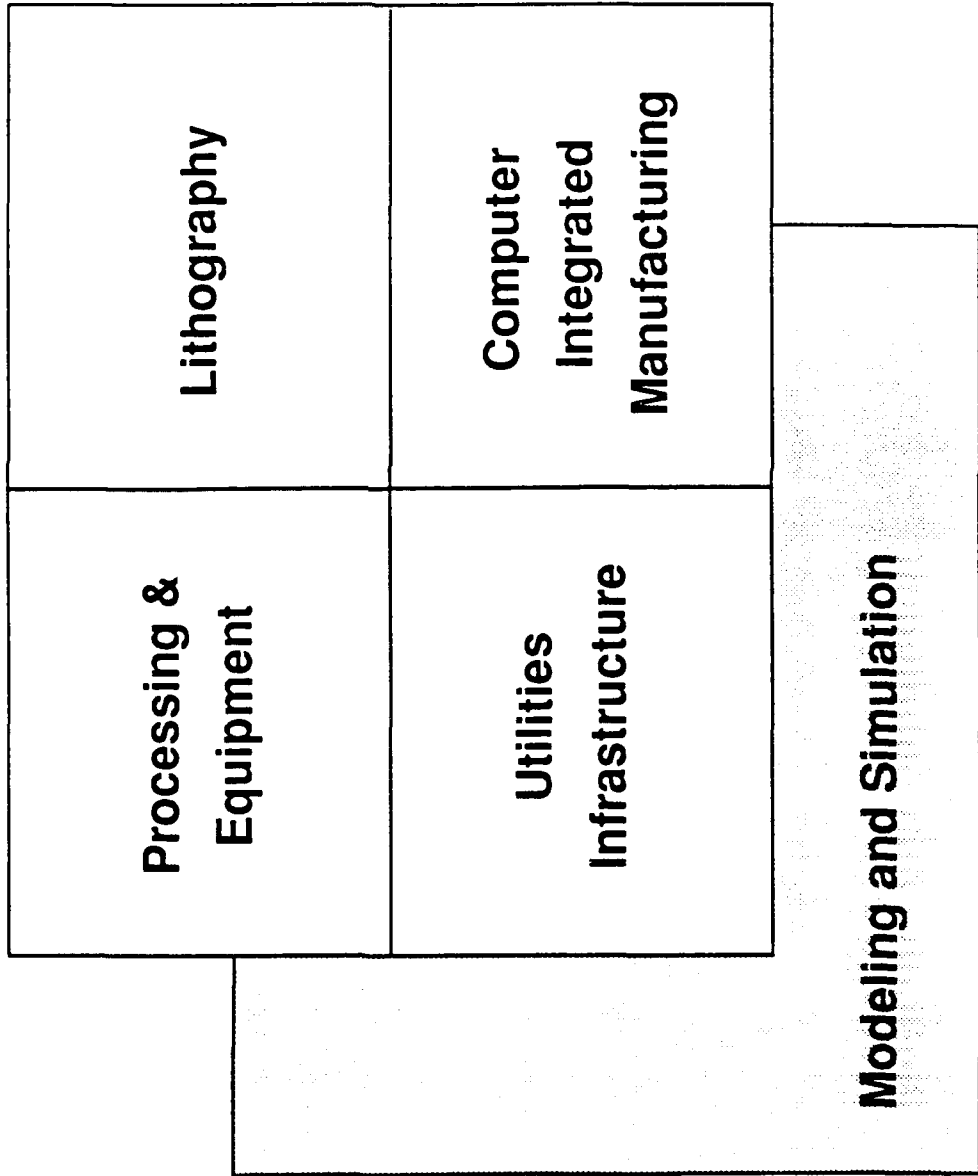
**Sven Roosild
Deputy Director
Microelectronics Technology Office**



FLEXIBLE INTELLIGENT MICROELECTRONICS MANUFACTURING

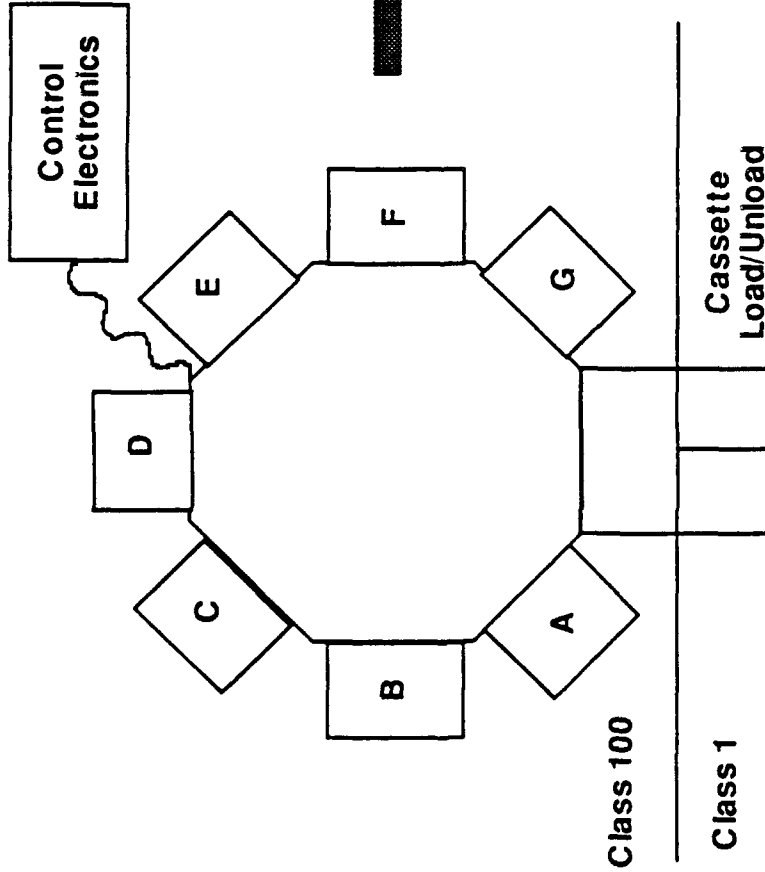
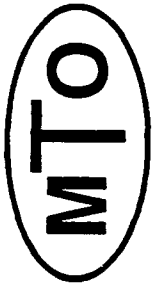


Key Elements

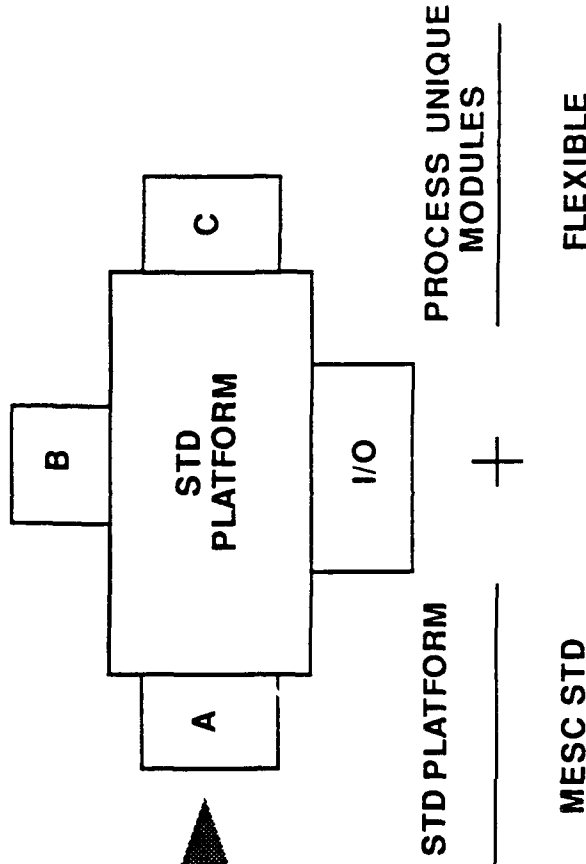




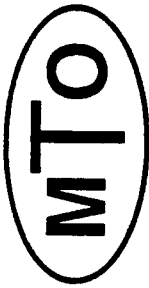
CONCEPTS IN MODULAR CLUSTER TOOLS



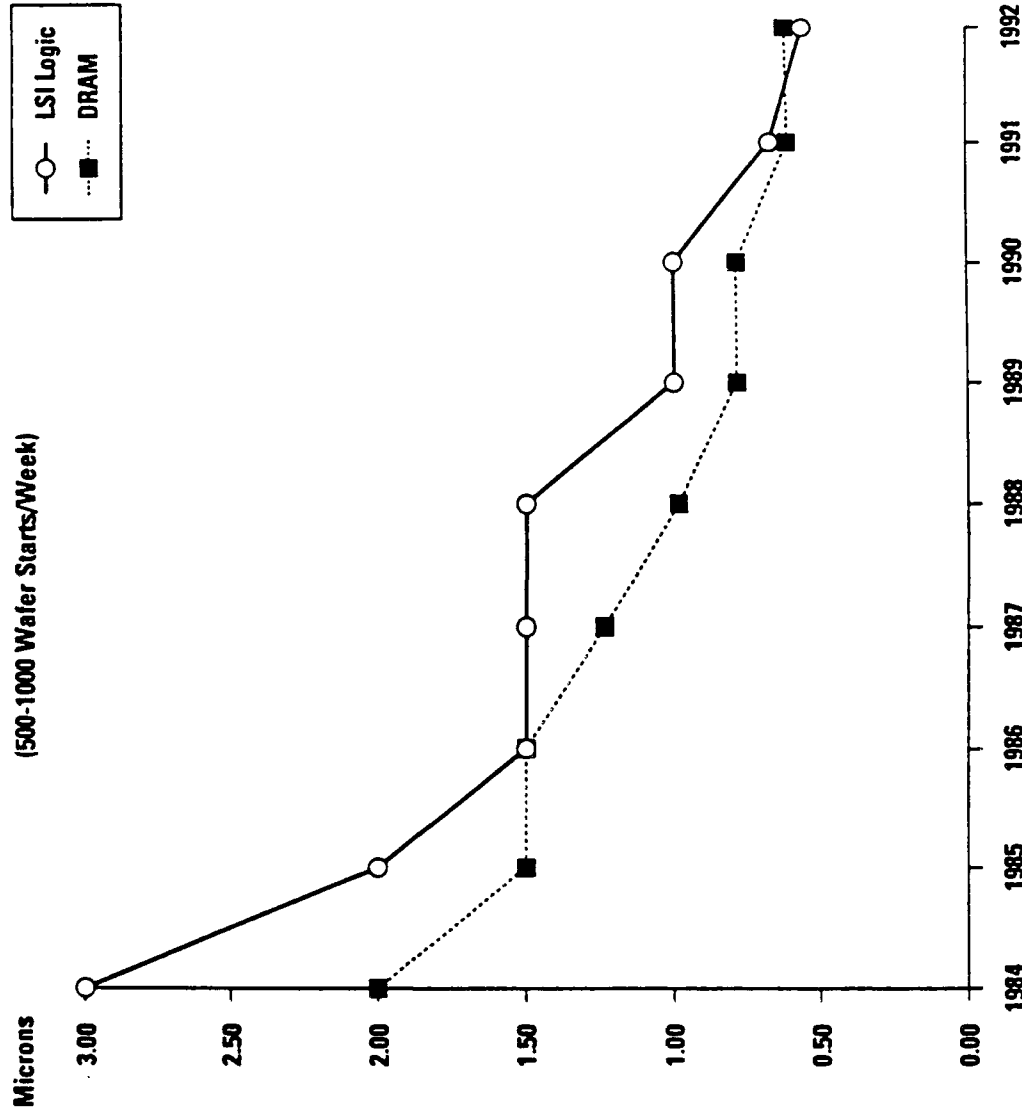
- High cost \$1-2M
- Large footprint 100 ft² Class 1/100
- Reliability? 40 hr MTBF



- Low cost \$100K platform +100K/module
- Small footprint 20 ft² Class 1000 integrated clean environment



LEADING-EDGE LINEWIDTHS LOGIC vs. DRAM



Source: VLSI Research and LSI Logic (for Own Linewidths)



FLEXIBLE INTELLIGENT MICROELECTRONICS MANUFACTURING



<u>TODAY'S STATE-OF-THE-ART FAB</u>	<u>GOAL: FLEXIBLE INTELLIGENT FAB</u>
Large volumes of a single part type	Many part types, many processes in any volume
25,000 wafers/month of DRAMs minimum	Minimum of 1,000 wafers/month of high-value-added, differentiated products (logic, ASICs)
\$500M entry cost (\$1.5B by 2000)	~ \$50M entry cost
3-year life for fixed capacity	Clusters and CIM form factory "backbone" for inexpensive, rapid upgrades and capacity growth

TIME HORIZONS FOR FY 1988 - 92 PROGRAMS

0.8 μ	0.5 μ	0.35 μ	0.25 μ	0.18 μ	0.13 μ	0.1 μ
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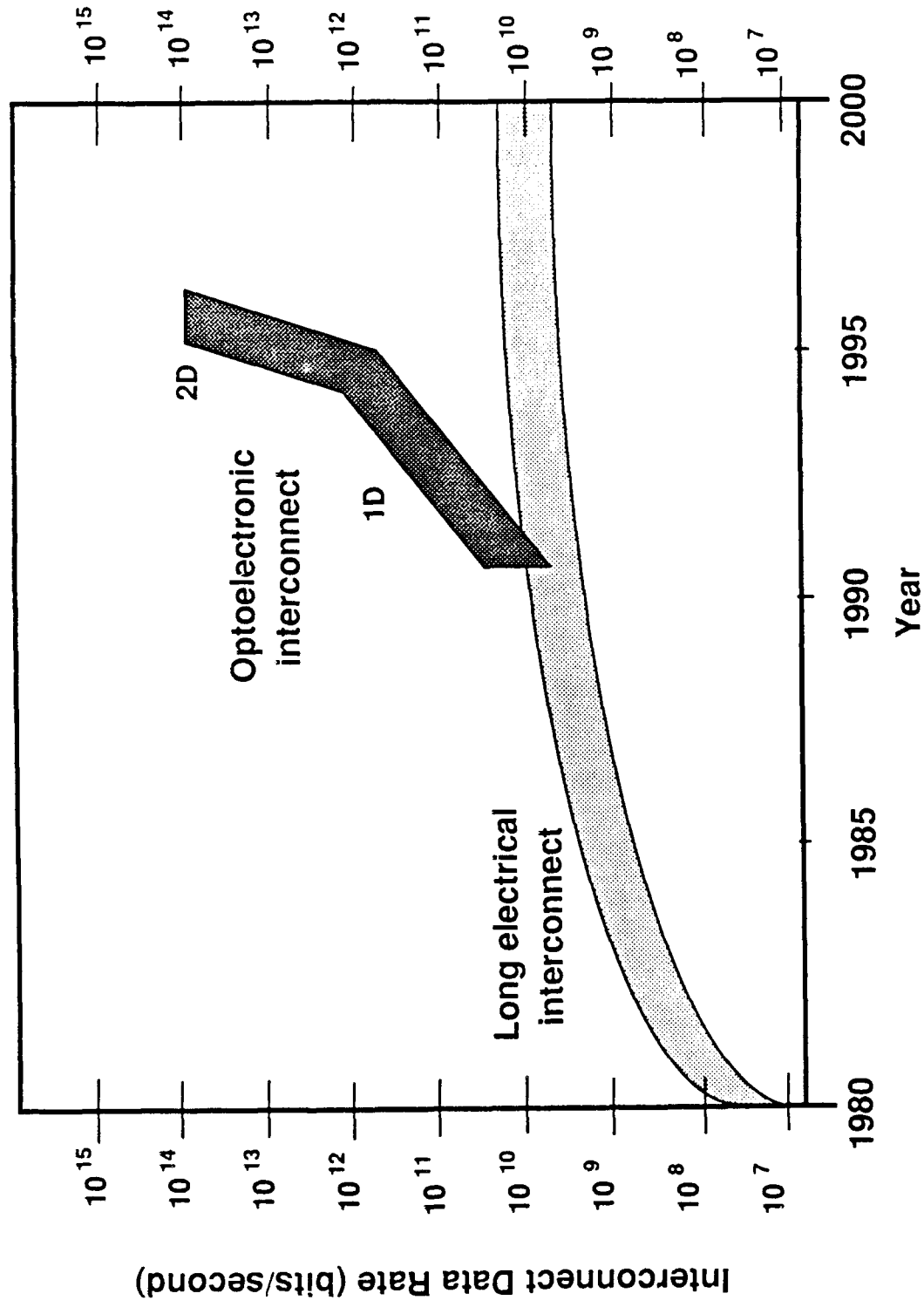
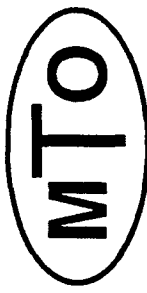
SEMATECH

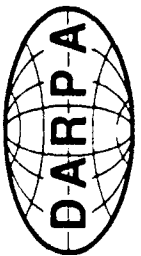
M M S T

193nm / X - Ray Lithography

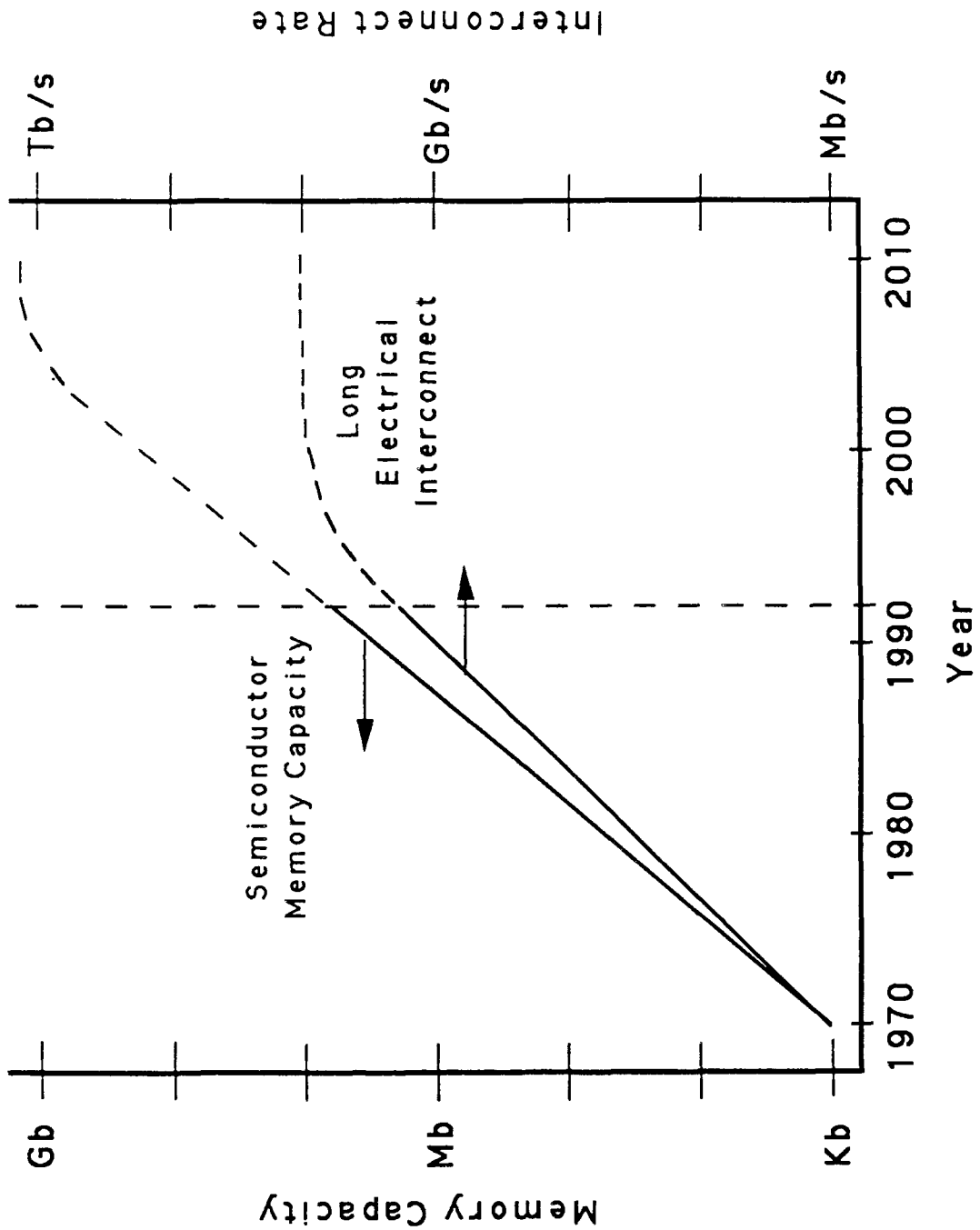
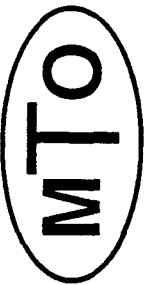


OPTOELECTRONIC INTERCONNECTS FOR INFORMATION PROCESSING





TRENDS IN MICROELECTRONICS





HOW SMALL IS SMALL?



Human hand
~0.1m wide



Grain of sand
~1 mm



Human hair
50-100 microns
wide



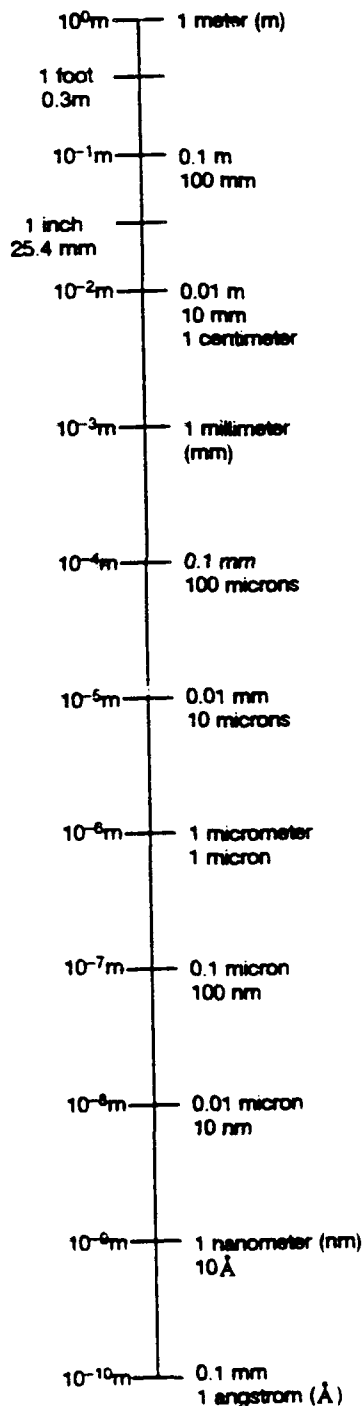
Smoke particle
~4 microns



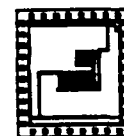
DNA ~2 nm wide



Atoms 1-4 Å



Printed circuit board
0.05-1 m wide



Integrated circuit chip (die)
~10 mm wide



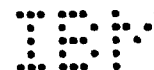
Micromechanical
components
10-1000 microns wide



Transistor on integrated circuit
2-20 microns wide
(smallest feature ~0.8 micron)



Quantum electronics structures
~200 Å wide



Atomic lettering using
scanning tunneling microscope
65Å high



THE CHALLENGE



Today



The microelectronics manufacturing challenge for 2000 is to make ...

- 10^8 interconnected transistors/cm²
- With 10^{-5} cm features
- Across 700 cm²
- For as few as 10 wafers
- Turn around in a few days
- For $\sim 10^1$ dollars/cm²

APPENDIX 4

STANDARD FORM 298

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

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6. AUTHOR(S) Daniel H. Butler, Jr.					
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