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ELECTRONICS RELIABILITY FRACTURE MECHANICS

VOLUME 1. CAUSES OF FAILURES OF SHOP REPLACEABLE UNITS AND HYBRID MICROCIRCUITS

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Final Report for Period May 1987 - September 1991

FLIGHT DYNAMICS DIRECTORATE
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This technical report has been reviewed and is approved for publication.

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This is the first of two volumes. The other volume (WL-TR-91-3119) is "Fracture Mechanics."

The objective of the Electronics Reliability Fracture Mechanics (ERFM) program was to develop and demonstrate a life prediction technique for electronic assemblies, when subjected to environmental stresses of vibration and thermal cycling, based upon the mechanical properties of the materials and packaging configurations which make up an electronic system.

A detailed investigation was performed of the following two shop replaceable units (SRUs):

- Timing and Control Module (P/N 3562102)
- Linear Regulator Module (P/N 3569800)

The SRUs are in the Programmable Signal Processor (3137042) Line Replaceable Unit (LRU) of the Hughes AN/APG-63 Radar for the F-15 aircraft.

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BLOCK19. ABSTRACT *(Continued)*

- **Failure Analysis of Failed Field SRUs**
  Nineteen failed modules were obtained from Warner Robins Air Logistics Center for failure analysis. There were five confirmed failures of each of the two part numbers investigated. Failure mechanisms identified include electrical overstress, physical damage, oxide insulation defect, short due to particle, and contamination.
- **Life Models**
  The following failure mechanisms were selected for modelling in this program:
  - hybrid microcircuit failure from mobile ionic contamination (observed in the failed field modules)
  - hybrid microcircuit failure from surface contamination (observed in the failed field modules)
  - bond wire fracture (documented in the other volume, "Fracture Mechanics")
  - plated through hole fracture (documented in the other volume, "Fracture Mechanics")
- **Special Fabrication/Inspection**
  Two serial numbers of each of the two SRUs were fabricated. The four modules were specially inspected at various steps in the production process so that the location and size/severity of each of the significant latent defects would be known/bounded.
- **Combined Environments Reliability Test**
  The four specially fabricated/inspected modules were subjected to a thermal/power cycling reliability test. The modules underwent nearly 500 thermal cycles, between ambient temperature and temperatures much higher than in normal flight, without failure.

The key results of this investigation are:

- Procedures for determining the cause of field failures of electronic assemblies in an ongoing military program were developed and used successfully.
- Techniques were developed to perform special inspection at various steps in a production process so that the location and size/severity of selected significant latent defects is known/bounded.
- A relatively simple test setup was developed for thermal/power cycling reliability testing of avionics modules.
- The mode and mechanism of ionic contamination induced failure of a hybrid microcircuit were identified.
- A method was developed for using a high temperature/bias screen to bound the ionic contamination induced voltage shift that could occur in deployment.
- A method was developed to predict the effects of varying distributions of ionic contamination on the electrical behavior of a transistor. By determining the lowest acceptable gain of the transistor for proper operation of the hybrid, the time-to-failure for the hybrid was determined from the model.
- These APG-63 Radar modules are very durable.

BLOCK 12. PERSONAL AUTHORS

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Dr. Alan H. Burkhard was the WL (Wright Laboratory) project engineer. The technical contributions of WL by Dr. Burkhard and Chris Leak are gratefully acknowledged.

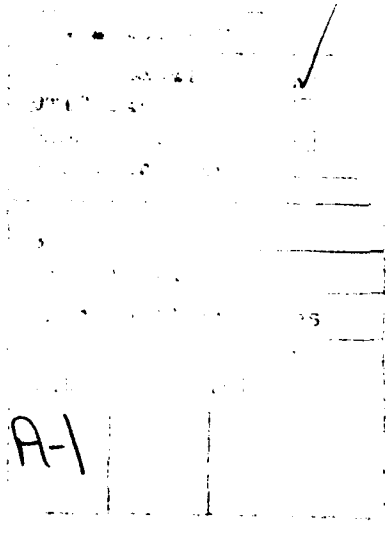
Warner Robins Air Logistics Center, GA, provided failed field modules for failure analysis. WR-ALC also provided serviceable modules for help in checking out the test station for the Combined Environments Reliability Test.

The Hughes Aircraft Company program team included more than 400 people representing four of Hughes' seven major groups:

- Electro-Optical & Data Systems
- Radar Systems
- Training & Support Systems
- Industrial Electronics

The following companies were subcontractors:

- MetroLaser; Irvine, CA — holographic interferometry (HI) nondestructive inspection (NDI)
- Newport Corporation; Fountain Valley, CA — provided HI facility under subcontract to MetroLaser
- Spectron Development Laboratories; Costa Mesa, CA — HI NDI
- Olganix Corporation; Reseda, CA — dynamic tomography



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ABBREVIATIONS, ACRONYMS, AND SYMBOLS

ADS	Automated Data System
AES	Auger Electron Spectroscopy
AF	Air Force
AFWAL	Air Force Wright Aeronautical Laboratories (now WL)
AMRAAM	Advanced Medium Range Air-to-Air Missile
ANSI	American National Standard Institute
ASARS	Advanced Synthetic Aperture Radar System
ASME	American Society of Mechanical Engineers
ATE	Automated Test Equipment
AVIP	Avionics/Electronics Integrity Program
AVO	Avoid Verbal Orders
CDRL	Contract Data Requirements List
CERT	Combined Environments Reliability Test
CLIN	Contract Line Item Number
CRT	Cathode Ray Tube
CTE	Coefficient of Thermal Expansion
DC	Date Code
DMM	Digital Multimeter
DOD	Department of Defense
DTS	Digital Test System
DUT	Device Under Test
EDSG	Electro-Optical & Data Systems Group
EDX	Energy Dispersive X-Ray
EMI	Electromagnetic Interference
ERFM	Electronics Reliability Fracture Mechanics
ESD	Electrostatic Discharge
ESS	Environmental Stress Screening
FaAA	Failure Analysis Associates
FAR	Failure Analysis Report
FFOP	Failure Free Operating Period
FIEE	Symbol for AFWAL Environmental Control Branch (now WL/FIVE)
FIVE	Symbol for WL (formerly WRDC) Environmental Control Branch (formerly FIEE)
FVR	Failure Verification Report
HAC	Hughes Aircraft Company

HE	Heat Exchanger
HI	Holographic Interferometry
HTFB	High Temperature Forward Bias
HTRB	High Temperature Reverse Bias
IC	Integrated Circuit
IDC	Interdepartmental Correspondence
IEEE	Institute of Electrical & Electronics Engineers
IPC	Institute for Interconnecting & Packaging Electronic Circuits (formerly Institute of Printed Circuits)
IR	Infrared
IRPS	International Reliability Physics Symposium
ISTFA	International Symposium for Testing & Failure Analysis
JSME	Japan Society of Mechanical Engineers
LRU	Line Replaceable Unit
MDR	Material and Deficiency Report
MFHBMA	Mean Flight Hours Between Maintenance Actions
MOS	Metal-Oxide-Semiconductor
MSIP	Multi-Staged Improvement Program
MTR	Module Test Results
MUX	Multiplexer
NDI	Nondestructive Inspection
PA	Product Assurance
PIND	Particle Impact Noise Detection
P/N	Part Number
PSP	Programmable Signal Processor
PTH	Plated Through Hole
PWB	Printed Wiring Board
QA	Quality Assurance
RADC	Rome Air Development Center (now Rome Laboratory)
RF	Radio Frequency
RGA	Residual Gas Analysis
RSG	Radar Systems Group
SAM	Standard Avionic Module
S/N	Serial Number
SEM	Scanning Electron Microscope
SOW	Statement of Work

SPIE	Society of Photo Instrumentation Engineers
SRU	Shop Replaceable Unit
SSD	Static Sensitive Device
SSR	Solid State Relay
STE	Special Test Equipment
SwRI	Southwest Research Institute
TC	Temperature Coefficient
TFR	Trouble and Failure Report
TLD	Thermoluminescent Detector
TS	Test Specification
TSD	Technology Support Division
TTL	Transistor-Transistor Logic
USAF	United States Air Force
VCR	Video Cassette Recorder
WL	Wright Laboratory (formerly WRDC; formerly AFWAL)
WR-ALC	Warner Robins Air Logistics Center
WRDC	Wright Research & Development Center (formerly AFWAL; now WL)

1.0 INTRODUCTION

The program overview is summarized in Refs. 1-1, 1-2.

1.1 BACKGROUND

Electronic assemblies at all levels of assembly, component, printed wiring board (PWB) and Line Replaceable Unit (LRUs) employ many combinations of equipment. The reliability (performance over time) of these assemblies is dependent upon the degeneration processes initiated by the interaction of the design and manufactured (package) configuration with the operational and environmental stresses imposed during its period of usage. In general, life limiting failure mechanisms generally arise from the configuration and use of materials which interact with one or more environmental parameters such as temperature, relative humidity, nuclear radiation, electrical potential gradients, mechanical fatigue cycling and corrosive chemicals. The manifested failures in electronic assemblies have been found to most often originate at the interface between different materials, at high stress sites and/or at sites where latent defects preexisted within the electronics.

Studies by many investigators have identified that the environmental stresses of vibration and thermal cycling significantly contribute to the failure rate of modern electronics (Ref. 1-3). Vibration and thermal cycling induce mechanical stress and strain in the materials and interfaces. The effects of cyclic stress and strain loading on materials have been extensively studied and modelled under the technical disciplines of fatigue analysis, linear elastic fracture mechanics and nonlinear fracture mechanics. In general, this work has been for structural materials used as load carrying members of large structures such as airframes or space structures as opposed to microscale structural configurations typical to an electronic assembly.

Over the past 15 years technical work to understand and in some cases model the reliability of specific failure prone sites within an electronic assembly has been accomplished. Generally this work has been done for a specific problem using techniques such as linear fracture mechanics, curve fitting of experimental data, fatigue analysis, and chemical reaction rate relationships. The focus of the Electronics Reliability Fracture Mechanics (ERFM) program was to bring this work together in a coherent manner so that Failure Free Operating Period (FFOP) predictions can be made based upon material properties and/or defect characteristics for the environmental effects of vibration and thermal cycling.

ERFM is a follow-on of a program called "Latent Defect Life Model & Data," which Hughes Aircraft Company performed under contract to the Air Force during the period 1984-1986 (Ref.

1-3). The conclusions and recommendations of that investigation led to the ERFM program, which Hughes performed under contract to the Air Force during the period 1987 - 1991 and which is documented here.

The life prediction technique demonstrated in the ERFM program will be used in future equipment acquisitions under the Avionics/Electronics Integrity Program (AVIP) by the Air Force (Ref. 1-4). Additionally it will permit an equipment manufacturer to translate reliability requirements to levels of quality, and appropriate manufacturing methods. These shall be expressed in terms of needed material properties and defect characteristics in the shipped product.

1.2 OBJECTIVE

The objective of the Electronics Reliability Fracture Mechanics (ERFM) program was to develop and demonstrate a life prediction technique for electronic assemblies, when subjected to environmental stresses of vibration and thermal cycling, based upon the mechanical properties of the materials and packaging configurations which make up an electronic system.

1.3 ORGANIZATION OF THIS REPORT

The ERFM program is documented in a two-volume report:

Volume 1, Causes of Failures of Shop Replaceable Units and Hybrid Microcircuits (WL-TR-92-3015), covers a detailed study of field failures in two APG-63 Shop Replaceable Units (SRU), evaluation of the latent defects hidden in these SRUs fresh off the production line, development of analytical models for hybrid microcircuit contamination failure mechanisms and special combined environment reliability test on the selected SRUs.

Volume 2, Fracture Mechanics (WL-TR-91-3119), covers the technical efforts to investigate the feasibility of using existing fracture mechanics technology to analyze the durability of microscale elements typically used in modern electronics.

Papers summarizing several aspects of the program have been presented at symposia. They are cited in the respective sections of this report.

2.0 SELECTION OF SHOP REPLACEABLE UNITS (SRUs)

2.1 INTRODUCTION

The most commonly available data about field failures in deployed avionic equipment is part replacement data. This data gives a good indication of what was replaced to make the item functional again but does not give any insight as to why the item failed. Therefore, two shop replacement units (SRUs) were selected for a detailed study to identify the specific failure modes and mechanisms inducing deployment failures.

2.2 DESCRIPTION OF SELECTED SRUs

The two SRUs shown in Figures 2-1 and 2-2 were selected for use in this study. These SRUs were the most practical selection based upon the selection process outlined in section 2.3. This selection process balanced competing factors such as specimen availability, technical requirements, and cost to conduct failure analysis.

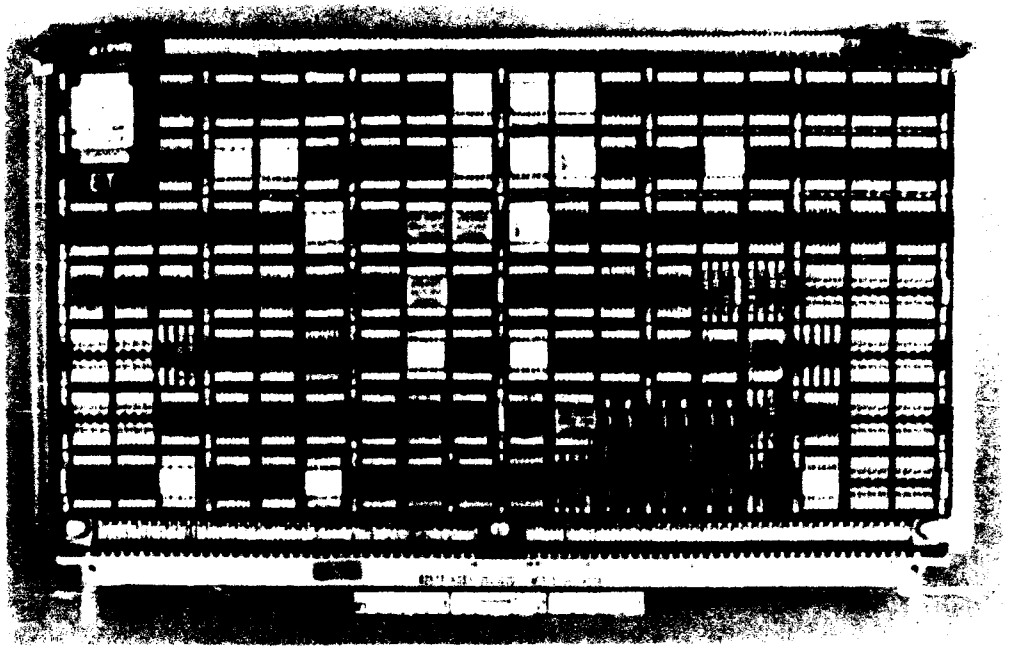
The SRUs are in the Programmable Signal Processor (PSP) (3137042) Line Replaceable Unit (LRU) of the Hughes AN/APG-63 Radar for the F-15 aircraft.

The 2102 module is a digital module consisting of two printed wiring boards (PWBs) bonded to a heat exchanger, through which coolant air flows. The dominant part type is an integrated circuit flatpack. The leads are formed in a "gull wing" shape and soldered to the surface of the PWB. A flow-under thermal transfer adhesive is applied under the parts.

The configuration of the Timing and Control Module changed from P/N 3562102 to 3562102-5 approximately July 1980 at APG-63 Radar Set 628 and subsequent. The change from P/N 3562102 to 3562102-5 added four jumper wires and a diode to reduce noise spikes and to increase the amplitude of the Blanking Pulse. The P/N 3562102 SRUs that were in Radar Sets 561 through 627 were upgraded to the –5 configuration (Radar Set 561 was the initial APG-63 Radar to use the 042 LRU). Thus all the Timing and Control Modules in the field, as well as those currently in production, are the –5 configuration.

The 9800 module is an analog module consisting of a PWB bonded to a heat exchanger, through which coolant air flows. The parts having the major contributions to failures are three hybrid microcircuits (denoted U1, U2, and U3 in Figure 2-2) and a power transistor (Q1).

The configuration of the Linear Regulator Module changed from P/N 3569800 to 3569800-10 approximately October 1984 at APG-63 Radar Set 918 and subsequent. The change from P/N 3569800 to 3569800-10 added two capacitors (C16 and C17) to provide additional filtering for the +12 VDC power form. The –10 configuration was not retrofitted to earlier sets. Thus the older sets in the field differ slightly from those currently in production. However, the differences are insignificant for ERFM.



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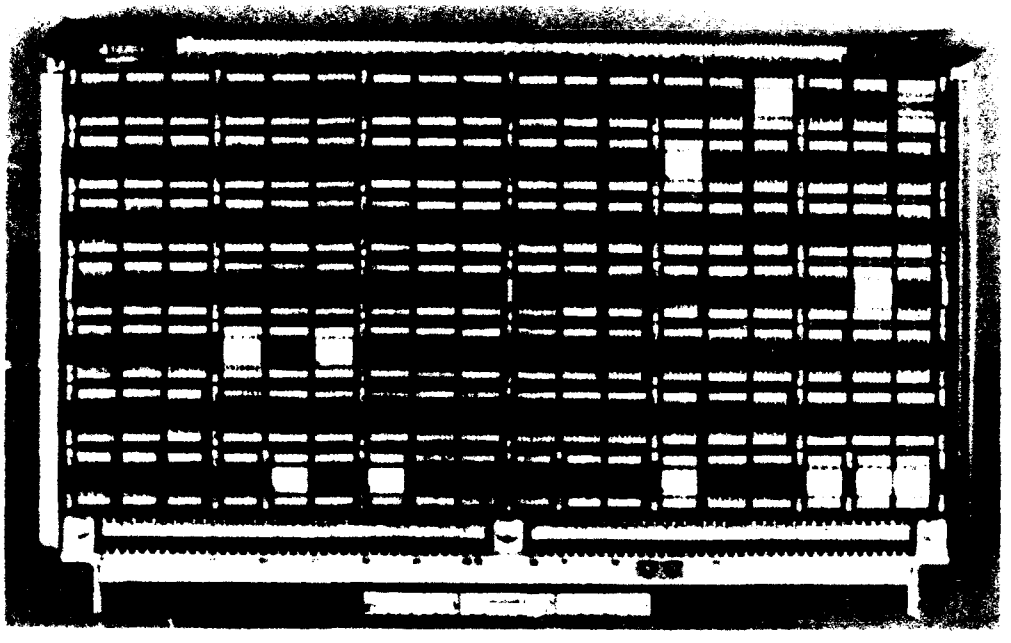

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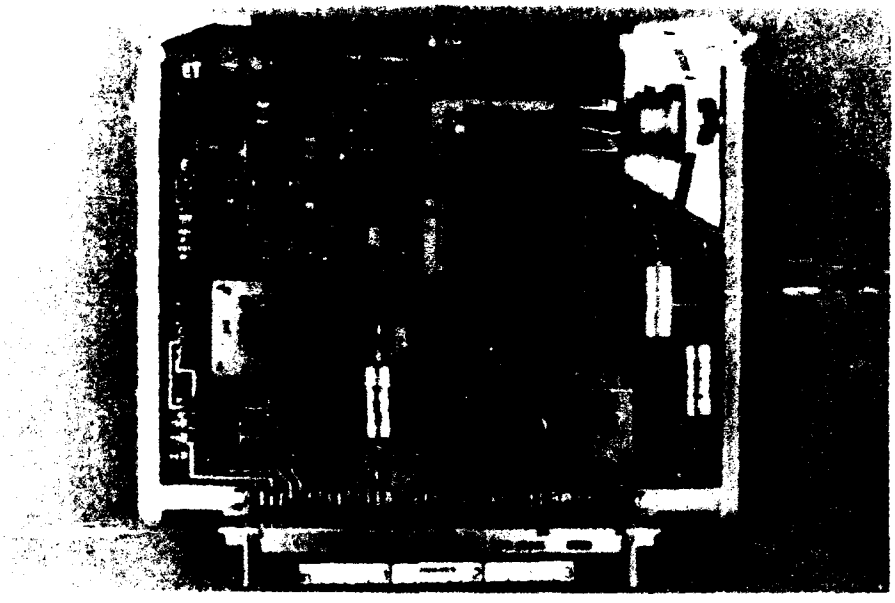
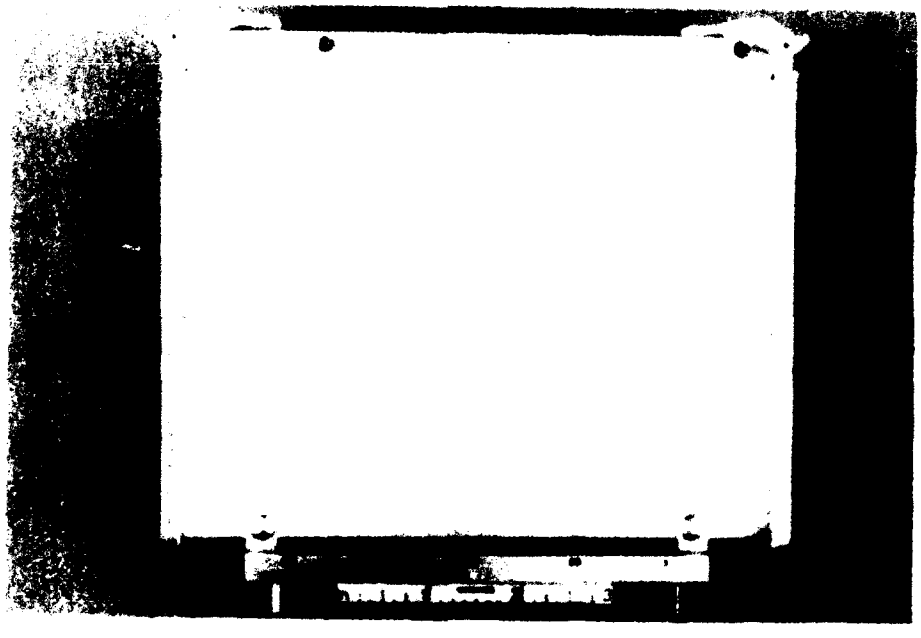
Figure 2-1. Timing and Control (2102) Module



PRINTED WIRING BOARD



HEAT EXCHANGER (DISSIPATOR)

Figure 2-2. Linear Regulator (9800) Module. The Three Large Square Components are Hybrid Microcircuits U1 (Upper Right), U2 (Lower Right), and U3 (Left).

2.3 SELECTION PROCESS

The SRU (shop replaceable unit) determination was conducted from May 1987 to June 1988. The process started with the selection criteria listed below:

- An Air Force program
- Presently in production
- Currently in operational usage in an Air Force aircraft
- Majority of failures induced by vibration and thermal cycling.

After looking at several programs, a variety of component types on SRUs and hardware availability were added to the criteria list.

2.3.1 Program Selection

Four Hughes production programs were considered. They are ASARS, AMRAAM, APG-63, and APG-70. The ASARS and AMRAAM programs, which have very low production rates, would not provide the field data and SRU availability required by the ERFM program. The APG-70 program was in early production. Only a few operational radar sets were in the field. The requirements would be very difficult to satisfy because of APG-70 level of maturity; the acquisition of field data and failed parts/assemblies would present major problems for the ERFM program. All APG-70 repairs were being accomplished at Hughes under an interim contractor repair contract, and the USAF did not expect to have an organic depot capability before 1991. Hughes continued to produce APG-63 spares for the USAF with delivery of current orders extending into late 1989. There's an abundance of APG-63 field data available, and the USAF has a fully established depot repair facility for this system. APG-63 failed parts and assemblies for destructive and nondestructive analysis will be easier to acquire than APG-70 parts, and the availability of test equipment for use during testing will also be more accessible. Based on these facts, APG-63 was selected as the program to pursue in the determination of the SRUs for the ERFM program.

2.3.2 Unit Selection

Several SRUs were identified as having the "majority of its failure rate induced by the environmental stresses of vibration and thermal cycling effects." Historically, the digital and power supply SRUs have been much more susceptible to vibration and thermal cycling than the RF modules in the Receiver-Exciter LRU. In production in the factory, the Receiver-Exciter Unit on the APG-70 program is not subjected to LRU aging (thermal cycling and vibration) as are the processor LRUs.

Though state-of-the-art technology was not one of the items listed for consideration, this consideration will enhance the usefulness of the results of the ERFM Program.

Considering all of the above-mentioned items and comparing APG-63 and APG-70 LRUs, the Programmable Signal Processor was chosen. The PSP (3137042) LRU has the most current technology of the APG-63 LRUs, i.e., Standard Avionic Modules (SAMs). The PSP digital and power supply modules more closely resemble the comparable modules in the APG-70 LRU (3173044) than any other APG-63/APG-70 comparison.

2.3.3 Module Selection

Data were analyzed from the in-house environmental stress screening records and the system acceptance test data base at Hughes Aircraft Company (see Table 2-1). Other data sources included field maintenance actions collected on the Air Force 66-1 data base over a 5-year period (see Table 2-2), and the Avionics Depot Test Set at Warner Robins Air Logistics Center (WR-ALC) in Georgia (see Table 2-3). These data indicate the relative failure rates of candidate 042 modules, as well as their susceptibility to thermal cycling and vibration. To achieve the program objectives, it was desirable that the selected modules had relatively high failure rates, although it was not a requirement to select the highest failure-rate modules or those most susceptible to thermal cycling and vibration.

There is a subtlety in the data shown in Table 2-1. The environment being imposed when the failure was detected is listed. This is not necessarily the environment that caused the latent defect to grow into a failure. However, the data shown in Table 2-1 are adequate to establish the relatively susceptibility of the modules to environmental stresses.

TABLE 2-1. VIBRATION AND THERMAL CYCLING FAILURES OF 042 MODULES

	Unit Aging			System Burn In			
Part Number	Low	High	Ambient	Low	High	Ambient	Sample No.
3523103	16	6	2	0	4	0	353
*3523108	61	6	6	4	7	4	353
3523125	12	1	1	1	2	3	304
*3562100	41	9	9	4	5	7	353
*3562102	18	6	17	3	4	10	353
3562107	0	0	18	0	1	5	353
*3569800	6	7	3	4	1	0	353
*Finalist							

TABLE 2-2. FIELD FAILURE HISTORY OF 042 MODULES

Part Number	Intermediate Maint. Actions	*MFHBMA (Hrs)
3523103	27	13,114
3523108	55	6,438
3523125	522	2,713
3562100	26	13,618
3562102	118	3,001
3562107	53	6,681
3569800	51	6,943
*Sample taken over 5 years and 354,073 flight hours		

TABLE 2-3. WR-ALC REPAIR DATA FOR 042 MODULES

Part Number	Description	Period	No. of Repairs
3562100	Control Interface	Sep 81 - Oct 87 (73 Months)	48
3523108	Program Memory and Control	Jul 81 - Dec 87 (77 Months)	95
3562102	Timing and Control	Aug 81 - Dec 87 (75 Months)	245
3569800	Linear Regulator	May 86 - Oct 87 (17 Months)	88

A preliminary analysis of the field maintenance actions and in-house environmental stress screening and acceptance test records narrowed the module selection to four candidates. Listed by part number, they were 3523108, 3562100, 3562102, and 3569800 (see Table 2-1). Upon further analysis of Warner Robins Air Logistics data and the Air Force's ability to support the ERFM program with failed field assets, the Timing and Control Module (P/N 3562102) and the Linear Regulator Module (P/N 3569800) were selected as the best representative modules to meet the criteria established above. They represent the best variety of component types and latest technology with available hardware to support this program.

2.4 VERIFICATION OF THE SELECTION

Following the initial decision, efforts were devoted to evaluating the feasibility of implementing these SRUs into the program requirements. Specific emphasis was placed on the following aspects:

1. Definition of the SRU fabrication and testing cycle to define entry points for item evaluation in the build cycle.

2. Identification of test equipment to support CERT testing.
3. Identification of additional failure data to supplement previous data analysis findings.
4. Receipt from the USAF depot at WR-ALC, processing and analysis of unserviceable SRUs (10 each P/N 3562102 and P/N 3569800).

Each of these aspects was analyzed and assessed to determine its impact on the selection of the two SRUs. Essentially, we evaluated the adaptability of two selected SRUs to program follow-on tasks.

2.4.1 Review of SRU Fabrication Process

The two SRUs selected are currently in production in different Hughes manufacturing areas.

The 3562102 Timing and Control Module is fabricated and tested at the contractor's manufacturing facility in El Segundo, California. This will permit ready access to evaluation by ERFM personnel during the various phases of fabrication and test.

The typical fabrication process for digital modules consists of (in sequential order):

1. Manufacture of the Printed Wiring Board.
2. Bond the PWB to the Heat Dissipator/Manifold (P/N 3562150-25 PWB Assembly).
3. Airflow test of the PWB Assembly.
4. "Kitting" of the PWB Assembly and the applicable components into a Manufacturing Kit. This Kit is then usually put into a bonded store room and released to be assembled at a later date.
5. Mount components (mechanized assembly) and operator review.
6. Mount components (manual assembly) and operator review.
7. Assembly (Module) Conditioning. This is a 23-hour test that consists of changing the temperature from –60 degrees (C) to +95 degrees (C) at the rate of 15 degrees (C) per minute.
8. First functional test (test T1) and subsequent rework.
9. Second functional test (test T2) and subsequent rework.
10. Inspection of SRU by PA/QA function.
11. Bond components and parylene coat the SRU. Inspection of bond and parylene coat.
12. Inspection of SRU by PA/QA function.
13. Power On Screening.
14. System Burn In.

The 3569800 Linear Regulator Module is kitted (parts assembled for build) in El Segundo, California, forwarded to the contractor's facility in South Carolina for assembly, and returned to El Segundo, California, for final processing and test. The fabrication process is as follows:

1. Manufacture of the PWB.
2. Bond the PWB to the Heat Dissipator/Manifold (P/N 3569805-1 Regulator Subassembly).
3. Airflow test of the Regulator Subassembly.
4. "Kitting" of the Regulator subassembly and the applicable components into a Manufacturing Kit. This Kit is then shipped to Hughes-South Carolina for assembly.

   All required test (including Assembly/Module Conditioning), rework, and inspection is performed in South Carolina. Bonding components and parylene coating the SRU, as well as inspection of bond and parylene coat, are also performed in South Carolina.
5. Return of the complete SRU to Hughes-El Segundo.
6. Power On Screening.
7. System Burn In.

ERFM personnel have determined that this flow of hardware during fabrication will not impede the ability to inspect hardware in conjunction with program plans.

The 3569800 SRU uses three hybrids (two part types). These hybrids are built by numerous vendors, including Hughes. It would be simpler to inspect the hybrids during their fabrication if they are made by Hughes than if they are made by another vendor. Thus having Hughes as a qualified supplier for these key parts is an advantage of selecting this SRU. It appeared that the procurement of the hybrids for the two 9800 modules to be fabricated for ERFM can be directed to Hughes. The hybrid suppliers will be investigated in more detail in Section 4.0.

Further planning will be required (Section 4.0) to determine the actual points of inspection of hardware by ERFM personnel in the fabrication cycle. However, the conclusion reached in this cursory evaluation is that the fabrication of both SRUs lends itself to ERFM program requirements. There is no reason evident from the fabrication cycle evaluation to not select the 3562102 and 3569800 SRUs as candidates for this program.

2.4.2 Identification of Test Equipment

There will be a requirement to test both SRU types during CERT testing. Preliminary evaluation of available test equipment used in production was made to determine impact on the LRU selection process. Factors such as test equipment needs, availability and cost effectiveness were evaluated.

The Timing and Control Module, P/N 3562102, is a digital device, which is tested at the module level by general purpose digital test equipment operated with special software and

interface adapters. This equipment is the DTS-70 Multipurpose Digital Tester built by Hewlett Packard. This equipment is no longer procurable from the Original Equipment Manufacturer, nor is there surplus equipment available for use by the ERFM program. In addition, the cost of this or similar equipment does not lend itself to a cost effective approach to CERT testing. The most cost effective approach appears to be selection of a Power On Screening Station to perform a DC powered test of the 3562102 SRU. Although this testing is not an in-depth testing of the circuit card, it does provide a means of powering this SRU in a CERT environment. Several options to supplement this testing to provide in-depth digital testing are:

- Removing the digital module periodically for electrical testing at ambient using the manufacturing DTS-70 tester.
- Removing the digital module periodically for electrical testing while slaved in an 042 LRU subjected to high and low temperature in an environmental chamber.
- Periodically uncovering the digital module while at high/low temperature and quickly monitoring it for signs of failures by means of infrared thermography and/or holographic interferometry.

These options appear feasible and will be explored in detail in Section 6.0. Thus powering and monitoring present a problem with the digital module. It would be the same problem with any digital module, not just the 2102. It does not appear to be so difficult a problem as to "deselect" a digital module for ERFM.

The Linear Regulator Module, P/N 3569800, is an analog device, which is tested at the module level by the Linear Regulator Test Station. This station is used in manufacturing and has the capability to test other F-15 Radar modules. This test station will perform a complete functional test of the Linear Regulator Module and can be used in conjunction with CERT testing. Future tradeoffs planned for follow-on tasks are the evaluation of using this Linear Test Station with stripped down capability (ability to test only P/N 3569800) or designing a comparable test setup with general purpose test equipment. With either approach, there appears to be the capability to CERT test this module with adequate test equipment capability. These options will be explored in detail in Section 6.0.

2.4.3 Failure Data Analysis

The initial selection of the Timing and Control Module, P/N 3562102, and the Linear Regulator Module, P/N 3569800, was based on specific manufacturing history data and data provided from field failures. Since the initial selection decision, activity focused on obtaining supporting documentation that can be used in the life modelling process. All available sources of data were evaluated for application to program needs.

The USAF 66-1 data base was used in the initial selection process to confirm that both SRUs experience a relatively high frequency of failure that can be useful to ERFM program requirements. AFM 66-1 data provide the relative failure rate between Programmable Signal Processor SRUs but do not provide the detailed information necessary to draw conclusions regarding the cause of failure. Necessary information such as temperature, vibration, printed wiring board integrity and soldering problems are not available nor reported in the AF system.

The evaluation of Material . efficiency Reports was suggested by the AF as another possible source of field failure data. This source was not pursued as such data are very general in nature and do not contain documentation pertinent to the needs of this program. This decision was made by ERFM personnel after consultation with F-15 Radar Program personnel knowledgeable of MDRs and their content.

The primary source of data that is relatable to environmental screening, parts failure, PWB and soldering problems is manufacturing records. For each failure experience during various cycles of manufacturing test, an internal document called a Trouble and Failure Report (TFR) is used. TFR information is incorporated in a database for access by F-15 Program personnel. Initial documentation from TFRs was assembled for a selected group of SRUs in the Programmable Signal Processor Unit. This listing included the Timing and Control Module (3562102) and the Linear Regulator Module (3569800) to show that these SRUs are indeed candidates for the ERFM program. Recent data analysis efforts were devoted to looking in-depth into this data base and to evaluating all known failures of these two SRUs. New data from modules produced for spares and retrofit kits were included in this upgraded effort. The breakdown of this data shows the distribution of failures of these modules by parts, solder connection and other categories. In addition, this analysis effort was able to provide supplemental information regarding module failures at low, high and ambient temperature. These data are shown in Appendix A.

Another source of manufacturing data was uncovered. This was a report recently initiated in manufacturing to reflect any failures of modules during the various test cycles from module level through system level test. Data in this report duplicate TFR information (unit and system level) and add only module test information. This module information primarily reflects parts and workmanship problems in initial testing of modules following assembly. These data, since recently recorded, reflect only a sample of data and as such are of limited value to the ERFM program.

From the standpoint of SRU selection, there is no reason to change SRUs due to failure data considerations.

2.4.4 Analysis of Unserviceable SRUs

To supplement the analysis of failure data, an agreement was reached with Warner Robins Air Logistics Center (WR-ALC) to provide unserviceable (suspected failure) SRUs to the contractor for evaluation (see Section 3.0). Warner Robins agreed to provide 10 each of P/N 3562102 and 3569800 for failure analysis by the contractor. As of June 1988 (the date of the final SRU recommendation by Hughes to the AF), two each 3562102 and two each 3569800 SRUs had been received for evaluation. All four SRUs were fault isolated to defective component parts. Detailed analysis of soldering, printed wiring boards and failed components was in process. The verification of the suspected failures of the first two 2102 modules and the first two 9800 modules to be analyzed by Hughes provided more evidence that these SRUs are appropriate choices for the ERFM program. (The analysis of unserviceable SRUs, which was completed in 1989, is described in Section 3.0.)

2.5 CONCLUSIONS

The program should be the F-15 Radar APG-63, based on program maturity and asset availability. The APG-63 program also satisfies the SOW criteria that the selected program be an "Air Force program," "in production" and "currently in operational usage."

The LRU should be the Programmable Signal Processor because it most closely resembles the newer APG-70 signal processor from a current technology standpoint.

The SRUs should be the Timing and Control Module (P/N 3562102) and the Linear Regulator Module (P/N 3569800). Both modules satisfy all the selection criteria established above. They both come from Air Force programs that are currently in operational usage, their failures are predominantly induced by the environmental stresses of vibration and thermal cycling, they offer the latest technology and variety of component types, and there are sufficient field data and available hardware to support further analysis and review.

3.0 FAILURE ANALYSIS OF FAILED FIELD SRUs

This investigation is summarized in Ref. 3-1.

3.1 SUMMARY

Nineteen (19) shop replaceable units (SRUs) of the APG-63 radar that experienced failure in the field were subjected to detailed failure analysis. In all cases analysis was initiated at the module level by Hughes prior to any repair work being performed by the depot. Nondestructive techniques were utilized to verify failures and to isolate the failure to an integrated circuit, a hybrid, the printed wiring board (PWB), or an interconnect. In all cases in which a failure was verified, a hybrid or IC was found to be the cause. The component was then removed and a detailed failure analysis was performed. Of the 19 SRUs received as field failures for analysis, 7 tested good when received and were returned without further analysis; 10 had components removed and analyzed following failure isolation; and 2 had components removed following failure isolation, but the failures could not be verified following removal. Failure mechanisms identified include electrical overstress, physical damage, oxide insulation defect, short due to particle, and contamination. These results were employed to help select the failure mechanisms for modelling in this program.

3.2 INTRODUCTION

3.2.1 Approach

Failure data were located and collected, and failed field modules were analyzed. The sources of failure data are listed in Table 3-1.

TABLE 3-1. SOURCES OF FAILURE DATA

- **FAILURE DATA ANALYZED**

  FIELD
  FACTORY
  RADC PART FAILURE ANALYSIS

- **FAILURES ANALYZED BY PROGRAM TEAM**

  FAILED SRUs FROM FIELD
  UP TO 20 PROVIDED BY AIR FORCE
  SUPPLIED BY WARNER ROBINS AIR LOGISTICS CENTER

3.2.2 Analysis of Available Failure Data

Field data from Warner Robins Air Logistics Center (WR-ALC) and from the USAF 66-1 data base were examined. Neither of these sources provides the detailed data required for the ERFM program. They list parts removed, not verified failures. They do not state how or when failures occurred or the mechanism of the failure.

Another source of field data – Material Deficiency Reports (MDR) – was suggested by the Air Force at the quarterly walk-through talk-through presentation in May 1988. The ERFM program team is familiar with MDRs, and MDRs do not have the data needed for ERFM. Therefore, Hughes did not analyze MDRs.

Factory data in the form of Trouble and Failure Reports (TFRs) were examined. They do not show the detail needed for ERFM. Environmentally related failures are documented only for the Line Replaceable Unit (LRU), not the SRU.

Another source of manufacturing data - Module Test Results (MTR) - was uncovered. This is a report recently initiated in manufacturing to reflect any failures of modules during the various test cycles from module level through system level test. Data in this report duplicate TFR information (unit and system level) and add only module test information. This module information primarily reflects parts and workmanship problems in initial testing of modules following assembly. The data, since recently recorded, reflect only a sample of data and as such were of a limited value to the ERFM program.

RADC part failure data are another source which was examined and did not prove fruitful. RADC is under contract to WR-ALC to perform failure analysis of specific failed parts. However, none of these part types is used in the SRUs selected in the ERFM program.

The conclusion from analyzing the available failure data is that these data are not adequate for the purposes of ERFM. Because of the scarcity of detailed failure data for the selected SRUs, the field failures analyzed by the program team became more important for identifying the locations and causes of failures.

3.2.3 Organization of Section

The remainder of this section describes the analysis by the program team of failed field SRUs. Section 3.3 describes the flow of hardware. Section 3.4 describes the analysis techniques used. Section 3.5 describes the results of the individual failure verifications and analyses. Section 3.6 describes the overall results. Section 3.7 presents the conclusions derived from this investigation. Section 3.8 presents recommendations for further work. Section 3.9 lists the failure mechanisms selected on the basis of these results for modelling in this program.

3.3 FLOW OF HARDWARE

3.3.1 Source of Hardware

Warner Robins Air Logistic Center (WR-ALC) is the Air Force Logistic Center that is responsible for the SRUs selected for this study. An agreement with WR-ALC, as outlined in Table 3-2, was established for the timely flow of failed SRUs for use in this study.

TABLE 3-2. AGREEMENT WITH WR-ALC

- UP TO 10 EACH OF 2102 AND 9800 SRUs
- ONE EACH AT HUGHES AT A TIME
- NOT TESTED OR REPAIRED BY WR-ALC
- WR-ALC NOT TO SEND "HANGAR QUEENS" OR "DOGS"
- HUGHES NOT TO DESTRUCTIVELY ANALYZE BOARDS
- HUGHES MAY REMOVE AND DESTRUCTIVELY ANALYZE PARTS

3.3.2 Flow of Hardware within Hughes

Once the failed SRUs were received by Hughes, the Support Systems Organization, in Long Beach, California, performed diagnostic testing on the modules to isolate the failure to a specific component on the assembly. The timing and control module (P/N 3562102) first underwent a unit level diagnostic test in which the module was monitored while installed in a PSP LRU connected to a computer that simulated the other LRUs in an operating radar set. This test has been found to accurately identify the cause of failure 75 percent of the time, assuming a failure exists. If a failure was not indicated by the unit level test, a module level test was performed under ambient, hot, and cold conditions while the module was monitored. If a failure of the module still was not detected, the module was transported to the Hughes Radar Systems Group, in El Segundo, California, for a critical timing test. If this test did not indicate a failure, the SRU was returned to WR-ALC and a different SRU was requested.

The unit level test performed by Support Systems on the linear regulator module (P/N 3569800) allowed for testing of the module at hot and cold temperatures, as well as at ambient, by way of a heat gun and cold spray. This test has shown itself to be 98 percent effective in identifying cause of failure when a failure exists. If the SRU passed this test, module level

testing was performed at Radar Systems Group. If the module passed all tests, it was returned to Warner Robins Air Logistics Center and a different SRU was requested.

Once a failure was isolated on either of the two types of SRUs, the module would be transported to the Technology Support Division (TSD) of Hughes, El Segundo, California. TSD would verify the failure and, through functional testing and continuity checks, determine if the failure was caused by a fault in a device, the circuit board, or an interconnect/solder joint.

3.3.3 Return of Hardware

Following failure verification and fault isolation by TSD, the SRU was returned to Support Systems to be shipped to WR-ALC. In the case of an IC or hybrid device being identified as the cause of failure, the component was removed and sent back to TSD for detailed analysis before the module was returned to the Air Force.

3.4 FAILURE ANALYSIS TECHNIQUES

As described in the previous section, the SRUs were first evaluated by Support Systems and, if necessary, RSG to isolate the cause of the failure. Once that was accomplished, the module was delivered to the TSD Failure Analysis Group for investigation. Following is a brief description of some of the methods used in the analysis of failed components to determine the cause of failure or failure mechanism (Refs. 3-2 through 3-4). This is meant to be a representative list of the many techniques applied in the analyses to be described. Some of the analyses may not have required the use of all of these techniques, and some may have incorporated others not discussed here.

3.4.1 Analysis of Modules by TSD

Prior to component failure analysis being initiated, TSD performed both failure isolation and verification on each module. The following sections describe this process.

3.4.1.1 Failure Isolation

Failure isolation is first performed th the module completely intact. Repeated tests at lower and lower levels of integration are performed until the failure is isolated to the component level. Once isolated, the failed component is removed from the module. The suspect component is then delivered to the Failure Analysis Group for analysis.

3.4.1.2 Failure Verification

Once received by TSD, failed component electrical characteristics are examined. The initial examination is performed at very low current levels (10 microamps maximum). This ensures that the failure will not be exacerbated and that new failures will not be induced. Typically, a

curve tracer is used so that the exact shape of the current-voltage curve can be seen and documented.

Later, extensive parametric tests and functional tests are performed per the specification. This will detect any anomalous behavior by the part. Additional specially designed tests may be needed to fully characterize the failure.

Once the failure is fully characterized electrically, the analysis can proceed to other techniques.

3.4.1.3 Evaluation of Other Inspection Techniques

In addition to electrical methods of verifying and investigating failures, some recently developed nondestructive inspection (NDI) techniques were evaluated for application to the ERFM analyses. The techniques evaluated included digital X-ray laminography and holographic interferometry. Digital X-ray laminography was evaluated for its potential to radiographically differentiate between the front and back sides of the two sided timing and control module. Holographic interferometry was considered for use in identifying flawed solder joints and PWBs on the failed assemblies.

A requirement of Hughes' agreement with Warner Robins was to return the modules in repairable condition. To be certain that the components were not being affected by the radiation dose from the X-ray procedure, Dr. M. Reier of Hughes performed a review of the components, with respect to their radiation hardness, and also determined the total dose received by the components. The results of this review, documented in Appendix B, indicated that the radiation dose experienced by the components was well below the threshold for any potential damage.

The digital X-ray laminography technique evaluated was a film based method, which digitized films taken of the subject at eight different angles and then reconstructed a series of planar images representing the entire thickness of the sample. This approach failed to produce reconstructed images of sufficient resolution to evaluate the desired features of the microelectronic assembly. Other nonfilm based methods for performing laminography, which directly digitize the images and use more accurate handling systems, may ultimately provide better resolution.

Holographic Interferometry (HI) has been shown to be effective in evaluating PWB assemblies (Ref. 3-5). However, after closely evaluating the technique and the type of results it offered, it was decided that detailed visual inspection of the modules could yield most of the same results. HI appears to be better suited to a process control or production inspection role where relatively large numbers of assemblies can be evaluated in an automated or semi-

automated fashion. HI of a small number of modules, one or two at a time, would not have been cost effective.

An investigation also was made of the feasibility of identifying ionic contaminants responsible for hybrid microcircuit failure due to mobile ionic contamination. A technique for doing this using Auger Electron Spectroscopy (AES) has been developed and used successfully on various glasses which are used in nonelectronic applications(Refs. 3-6 through 3-8). However, the technique requires cooling the sample to liquid nitrogen temperatures, and the question remains as to whether or not AES would have sufficient sensitivity to detect the low levels of ionic contamination which can cause inversion in semiconductor devices. For these reasons development of the technique for application to microelectronic components was not deemed to be warranted.

3.4.2 Component Failure Analysis

A "typical" failure analysis for an integrated circuit or transistor is described below. This is a general flow, and not all steps may be required and they may not be performed in the exact order as listed. Each failure analysis is different. Data learned at any step may lead to changing the order of testing, adding tests, or repeating tests.

3.4.2.1 External Visual Examination

Perform external visual examination and photodocument markings and anomalies.

Purpose: To detect conditions external to the package that may contribute to the failure.

Looking for: Cracks in leads, frit and solder connections, solder bridging, voids in frit, scratches, contamination at seals and solder surfaces, broken leads, and incorrect part type (as indicated by markings).

Risk: Nondestructive. No risk.

3.4.2.2 Electrical Testing

Electrical tests would be performed in three steps: curve tracer testing, functional/parametric testing per specification, and specialized testing as required.

*a. **Electrical Testing - Curve tracer (current-voltage) testing.***

Purpose: To characterize (nondestructively) the pin-to-pin electrical characteristics of the device.

Looking for: Shorts, opens, leakage currents, low breakdown voltage, breakdown curve shape, walk-out.

Risk: Minimal.

b. Electrical Testing - Automated functional and/or Bench testing.

Purpose: If no problems were found with the curve tracer, to determine if device is out of specification with respect to parametric specifications and function.

Looking for: Conformance to parametric specification conformance to output truth table; temperature dependence of failure.

Risk: Potentially destructive in that ATE test voltages may cause failure to clear or may cause a borderline failure to degrade. However, initial curve tracer tests will minimize this risk.

c. Specialized Testing

It may be necessary to use tests beyond what is called out in the specification to fully characterize the failure, or to gather data on possible causes of the failure. These may include unusual biasing, temperature, temperature cycling, vibration, and others singularly or in combination.

3.4.2.3 Particle Impact Noise Detection (PIND) Test

Purpose: To detect loose particles inside the package.

Looking for: Presence of particles inside package cavity that may have caused short.

Risk: Nondestructive to the IC die. It may dislodge shorting particles and cause loss of the failure. Electrical tests must be repeated if original failure was a short and particles are indicated. Used in conjunction with X-ray examination.

3.4.2.4 X-Ray Examination

Purpose: To detect internal anomalies prior to delidding.

Looking for: Voids in die attach, open bond wires, misbonded bond wires, changes in position of particles before and after PIND testing.

Risk: Nondestructive, however, has the potential to alter threshold voltages and other electrical characteristics, if exposures are not limited.

3.4.2.5 Leak Testing

Purpose: To determine if hermetic seal has failed.

Risk: Potentially destructive because the test medium can be introduced into the package and react with internal contaminants, thereby slightly altering the original failure.

3.4.2.6 Residual Gas Analysis (RGA)

Purpose: To determine the internal gas composition of the package.

Risk: Puncture of the package may damage the die by physical contact or the package may be broken. Therefore, RGA is performed only when findings indicate that the internal atmosphere of the device may be contributing to the failure (such as when moisture may be involved).

3.4.2.7 Internal Visual Examination

Purpose: To detect and photodocument visual anomalies.

Looking for: Incorrect wire bonding, evidence of high current in the bond wires, evidence of manufacturing errors (masking errors, photoresist contamination, human spittle, etc.), melted metallization, suboxide arc-overs, metallization voids and electromigration, die cracks, die attach anomalies, loose or adhering particles.

Risk: Destructive to the package. Internal atmosphere can no longer be sampled if RGA was not performed previously.

3.4.2.8 Internal Probing

Purpose: To test discrete circuit elements on the die.

Looking for: Electrical characteristics of individual suspect circuit elements, exact location of shorts or leakage currents.

Risk: Potentially destructive or destructive. While careful probing can be performed in a nondestructive manner, metal scribing used to isolate components changes the die circuit configuration and may damage oxide layers.

3.4.2.9 Scanning Electron Microscope/Energy Dispersive X-Ray Analysis (SEM/EDX)

Purpose: To detect and photodocument anomalies not resolvable or observable by optical examination. Analyze elemental content of materials in the device or contaminants on the die.

Looking for: Anomalies too small to be seen under optical examination such as electrostatic discharge (ESD) damage, metallization step coverage, and intermetallic compounds. Elemental identification of contaminants and particles.

Risk: Potentially destructive because electron beam can degrade sensitive junctions. Areas can become negatively charged and ionic sensitive mechanisms can be altered. Risk is minimized by full electrical characterization prior to SEM examination.

3.4.2.10 Chemical/Plasma Layer Removal

Purpose: To remove glass and metallization layers one at a time, to view sublayers and diffusions for anomalies and photodocumentation. This step would be repeated for each layer until the anomaly or failure is found.

Looking for: Anomalies that had been hidden by upper layer(s).

Risk: Failure sites and/or normal function can be lost or altered.

3.5 SUMMARY OF FAILURE ANALYSES

During the course of this phase of the ERFM Program, 10 P/N 3562102 and 9 P/N 3569800 SRUs were received from Warner Robins Air Logistics Center for detailed failure analysis. Detailed documentation is provided in the Failure Verification Reports (FVRs) and Failure Analysis Reports (FARs). They were submitted to the AF as attachments to the Quarterly

Interim Technical Reports (CDRL Sequence No. 3). The cover pages of the FARs are reproduced here as Attachment C. The following provides a summary of each of the analyses including the most significant findings which lead to the conclusion of the mechanism causing each failure.

3.5.1 P/N 3562102

Ten Timing and Control modules, P/N 3562102, were received as SRUs that had reportedly failed in the field. Of these, five passed all diagnostic testing at Hughes and were returned without any further analysis being performed. Summaries of the five analyses performed on devices removed from the Timing and Control modules which had confirmed failures are presented below.

S/N 0593

The reported failure of this module, integrated circuit U2213 (54S04 Hex Inverter) pin 8 output shorted to ground, was verified at the time of the failure verification (FVR 4913). After the device was removed from the module and submitted for failure analysis (FAR 11079) the ground bond wire was found to be melted open.

Based on the results of this analysis, it was concluded that the pin 7 ground bond wire was melted open, probably due to a reverse current between the time of the failure verification and the time of the failure analysis. This failure is believed to be independent of the reported pin 8 to ground short.

Although the original reported failure of this device, pin 8 shorted to ground, was not verified in the failure analysis, close proximity of the pin 8 bond wire and an unpassivated area of the ground metallization indicate a possible intermittent conductive particle short. The device passed the PIND test, but during internal visual examination particles were found adhering to the edge of the die that were large enough to bridge the gap between the underside of the pin 8 bond wire and the adjacent unpassivated aluminum ground metallization. Possibly these or other particles caused an intermittent short that was observed during the original failure and during the failure verification. A small clearance between a bond wire and a ground metallization when accompanied by loose conductive particles has been found to be a source of failure in other devices in the past.

S/N 1003

Two integrated circuits, U1101 and U1408, were analyzed from this SRU. The U1408 read-only memory was reported to have failed during module level testing; however, no failure was found in parametric and functional testing. The reported failure of the U1101 quad line driver, 780-ohm short between pin 2 and ground, was verified. The probable cause of failure

was application of an excessive voltage at pin 2 that exceeded the collector-emitter breakdown voltage of the output transistor for this pin in the IC.

The appearance of this failure was nearly identical to that of the failure analyzed for S/N 1030 described below.

S/N 1010

The reported failure mode on the SRU, "no output on pin 15 of IC U2410, 54LS163A, four-bit counter," was verified. Pin 15 was found to have incorrect breakdown voltages, which indicated an electrical anomaly. The output transistor for pin 15 was shorted to another transistor because an area of necessary oxide insulation was missing. This short prevented correct transistor action and resulted in no output.

S/N 1015

The reported failure of IC U2414 (54S174, HEX D flip-flop) was mechanical damage to pin 15. Visual examination had revealed mechanical damage to the pin 15 output of this device. The failure was verified visually and electrically and found to be due to external mechanical damage to the lead at pin 15. All measurements indicated that pin 15 was functional, and that the failure was caused solely by the break in the external lead.

S/N 1030

The reported failure of the U1101 quad line driver, "pin 2 shorted to ground," was verified. The probable cause of failure of this IC was application of an excessive voltage at pin 2 that exceeded the collector-emitter breakdown voltage of the output transistor for this pin in the IC.

None of these five confirmed failures is relevant to ERFM. These results are evaluated further in Section 3.6.

3.5.2 P/N 3569800

Nine Linear Regulator modules, P/N 3569800, were received as SRUs that had failed in the field. Of these, two passed all diagnostic testing at Hughes and were returned without any further analysis being performed. Summaries of the seven analyses performed on Linear Regulator modules which had confirmed failures are presented below.

S/N 127

The reported module level failure of hybrid U1 (positive voltage regulator), "would not power up at cold temperature," was not verified when the hybrid was removed from the module. The device passed all tests at room and cold temperatures. The failure was observed originally on the module when the hybrid was sprayed with "minute amounts of cold spray." The failure could not be duplicated in failure analysis of the component.

S/N 300

The module level failure reported by Support Systems, "the output of hybrid U2 (negative voltage regulator) is -12.58 volts D.C., when it should have been -12.0 ±0.25 volts D.C.," was verified. Electrical tests after the hybrid was removed from the module indicated that the V09 and V011 output voltages of the hybrid were unstable and were out of tolerance. Both output voltages were approximately the same and varied between -12.63 and -12.71 volts D.C. The V09 and V011 voltages both should be from -11.94 volts D.C. minimum to -12.06 volts D.C. maximum according to the hybrid specification. Curve tracer measurements indicated that the output voltages were out of tolerance due to the 2.5 Kohm ±1% resistor between pins 21 and 24 being out of tolerance. The measured resistance was 2.3 Kohms; it should have been between 2.475 Kohms and 2.525 Kohms. The voltages (V09 and V011) came within tolerance when a 200.0-ohm resistor was connected via probing in series with the 2.3 Kohms. Both output voltages also came within tolerance after the hybrid was baked for 23 hours at +125°C due to the 2.5 Kohm ±1% resistor changing from 2.3 Kohms to 2.55 Kohms. After baking the hybrid for 23 hours, the hybrid was powered up for 36 hours to determine if the V011 output voltage would again go out of tolerance. Voltage measurements indicated that the V011 voltage remained within tolerance and was -11.999 volts D.C. after the 36 hours of operation.

Therefore, the analysis indicated that the hybrid failed due to the V09 and V011 output voltages being out of tolerance because of the 2.5 Kohm ±1% resistor between pins 21 and 24 being out of tolerance. The cause of the resistor being out of tolerance and the resistance changing during the baking of the hybrid is believed to be due to contamination too subtle to detect, since no obvious physical defects were noted on the resistor during internal examination. The hybrid may have been contaminated during manufacturing since it passed the hermetic seal tests at the start of the failure analysis.

S/N 344

Initial module level testing indicated that hybrid U3 (negative voltage regulator) failed to meet the -5.3V output requirement. However, during failure verification with all hybrids still on the module it was found that hybrid U2, not hybrid U3, was regulating incorrectly. With the module powered up, the outputs of voltage regulator hybrids U2 and U3 were monitored (-12 volts and -5.3 volts, respectively) while the following electrical tests were performed on the module:

- Continuous operation at room temperature (5-1/2 hours)
- Continuous operation at 50°C (2 hours)
- Temperature cycling from 25°C up to 55°C (3 cycles).

The output of hybrid U2 was observed to drift briefly during the continuous operation at room temperature and at 50°C. In each case the output drift lasted for approximately 2 minutes before stabilizing at the specified voltage (-12 volts). Temperature cycling the module caused the output of U2 to drop down to -11.3 volts during the first cycle and continue at the reduced voltage for the remainder of the test. The output of U3 did not change during any of the tests.

Based on the observed inconsistency of the regulated output of hybrid U2, the most likely cause of the reported failure of U3 was complete loss or significant reduction of its -12 volt input from U2. Hybrid U2 was then removed from the module for failure analysis. The -12-volt output of the hybrid drifted occasionally during the first hour of 3 hours of continuous operation at room temperature before stabilizing. Continuous operation at elevated temperatures (50°C and 60°C) and temperature cycling (-25°C to +60°C) did not reproduce the failure. The device passed particle noise impact detection (PIND) and hermeticity tests performed in accordance with MIL-STD-883C. Residual gas analysis disclosed a water vapor content of 15,000 parts per million (MIL-STD-883C allows 5,000 ppm max) and an atmosphere that was 97.5 percent nitrogen inside the hybrid package. The internal visual examination and nondestructive bond pull test did not disclose anomalies that would be related to the observed failure mode. Since the hybrid package was hermetic and still retained the nitrogen atmosphere it was sealed in, the failure was probably related to the excess water vapor sealed within the hybrid package at the time of manufacture.

S/N 428

The reported failure, "shorted, positive voltage regulator, hybrid U1," was not verified. The device passed all tests at room and high temperatures. The device was not a failure.

S/N 451

The reported failure, "negative voltage regulator, hybrid U2, does not regulate," was verified. The characteristics of the regulator transistor and its driver transistor were observed to change with time. Since the changing characteristics disappeared after a bake and since the two transistors were optically very dirty, it was concluded that the failure was due to mobile ionic contamination. It was concluded that the failure was due to either improper manufacture of the transistors or improper assembly of the hybrid.

S/N 502

The reported failure of negative voltage regulator, hybrid U2, output voltage too low, was verified. The failure was caused by the 2.5 Kohm ±1% resistor changing to 2.1 Kohm. A 2-hour bake at 125°C did not have any effect on the anomalous resistor value. However, after a number

of months of storage in ambient conditions it was found that the resistor had returned to its nominal value of 2.5 Kohm. Therefore, contamination in some form may have indeed been a contributing factor to this failure. Further review indicated that the location and mode of failure of hybrid U2 are the same as for the previously described failure of S/N 300.

S/N 555

The reported failure of negative voltage regulator, hybrid U2, "regulates at -2V," was not verified, but the hybrid was found to be a failure for regulating at -15V when it should regulate at -12V ±0.06V. The characteristics of one transistor were found to change with time, but could be returned to normal functioning by high temperature exposure. The same transistor was covered with anomalous spots. This behavior pattern is typical of mobile ionic contamination.

The P/N 3569800 results are summarized below:

S/N	Failed Component	Manufacturer	Date Code or S/N	Failure Mechanism
127	None verified	—	—	—
300	U2	Solitron	DC 8108	Contamination
344	U2	Solitron	DC 8128	Unknown; probably moisture related
428	None verified	—	—	—
451	U2	Solitron	DC 8142	Mobile ionic contamination
502	U2	Hughes	DC 8202	Contamination
555	U2	Hughes	S/N 4607	Mobile ionic contamination

The key results are as follows:

- All the confirmed failures were in hybrid U2.
- Two each were:
  - surface contamination
  - mobile ionic contamination.
- The contamination failures were equally divided between Hughes hybrids and Solitron hybrids, ruling out an untypical group of failures resulting from a bad batch at a single vendor.
- The date codes (in the years 1981 and 1982) may indicate that these failure mechanisms did not proceed to failure until more than 5 years after deployment.

3.6 RESULTS

3.6.1 Failure Analysis of Failed Field Modules

The results of the failure analyses of failed field SRUs are summarized in Table 3-3. Approximately half (9 out of 19) of the modules reported as failed at WR-ALC either tested good at the module level or had a verified failure not confirmed by subsequent failure analysis of the device. This is typical of the results of failure analysis of this type of hardware. Thus the data base consists of five confirmed failures of each module P/N.

TABLE 3-3. FAILED FIELD MODULES

PART NUMBER	SRUs FROM WR-ALC	RESULTS		
		TESTED GOOD	FAILURE CONFIRMED	NOT CONFIRMED
3562102	10	5	5	-
3569800	9	2	5	2

3.6.2 Failure Mechanisms Found

Table 3-4 summarizes the results of the failure analyses of the 10 confirmed failures. All the failures were in the active devices, rather than the solder joints or the printed wiring boards. None was from mechanical fatigue (thermal cycling and vibration).

TABLE 3-4. RESULTS OF FAILURE ANALYSES OF CONFIRMED FAILURES

P/N 3562102 - 2 ELECTRICAL OVERSTRESS - 1 BROKEN PIN - 1 OXIDE INSULATION DEFECT (NOT TIME DEPENDENT) - 1 SHORT IN INTEGRATED CIRCUIT ATTRIBUTED TO PARTICLE - NONE RELEVANT TO ERFM
P/N 3569800 - ALL IN HYBRID MICROCIRCUIT U2 - 2 MOBILE IONIC CONTAMINATIONS - 2 SURFACE CONTAMINATIONS - 1 UNKNOWN CAUSE
OVERALL FINDINGS - NO FATIGUE FAILURES - NO SOLDER JOINT OR PRINTED WIRING BOARD FAILURES

3.6.3 Statistical Evaluation of Data

The objectives of this evaluation are to determine what conclusions can be reached from this sample of five confirmed failures of each part type and what additional information would be obtained from a larger sample.

To enable these results to be analyzed statistically, it is useful to put them in a form in which they can be represented as a "yes/no" experiment. This is called a Bernoulli process.

The first form is obtained by asking the question, "Was the failure the result of the exacerbation of latent defects in the equipment by environmental stresses?" (The basis of the ERFM program and its predecessor, Latent Defect Life Model and Data, is that a significant fraction of failures is from this mechanism.)

Table 3-4 shows that the answer is "no" for all of the P/N 3562102 failures. They appear to be the result of misuse or rough handling (electrical overstress and broken pin) or latent defects that do not become exacerbated by environmental stresses (oxide insulation defect and a particle in an integrated circuit package).

Table 3-4 shows that the answer is "yes" for 4 out of 5 of the P/N 3569800 failures. The other confirmed failure (S/N 344) is from an undetermined cause. The relevant failures result from exacerbation of a latent defect (contamination inside a hybrid microcircuit) by environmental stresses (electrical stress and steady high temperature).

The second form is obtained by asking the question, "Was the failure the result of thermal cycling and/or vibration?" (This is the type of failure in the scope of the ERFM program.) None of the confirmed failures was from these mechanisms.

It is desired to evaluate the fraction of the failures in the population for which the answer to these questions is "yes." This is difficult to evaluate. However, the probability of obtaining certain outcomes can be calculated as a function of the fraction of the population. From the observed outcomes, the fraction in the population can then be inferred.

The probability P (X; n, P) of an event happening X times in n trials, as a function of the probability P of the event happening in a single trial, is given by:

$$P(X; n, P) = {}^{n}C_{X}\, P^{X}(1-P)^{n-X} \qquad (3\text{-}1)$$

where:

$${}^{n}C_{X} = n!/[X!(n-X)!]. \qquad (3\text{-}2)$$

For 5 trials, the formula becomes:

$$P(X; 5, P) = [120/(X!(5-X)!)]\, P^{X}(1-P)^{5-X}. \qquad (3\text{-}3)$$

The probability P(O; 5, P) of an event happening zero times in five trials is given by:

$$P(O; 5, P) = (1-P)^{5}. \qquad (3\text{-}4)$$

The formulas for five trials are plotted in Figure 3-1. The plot shows the following:

- The probability of an event happening zero times in five trials is a strongly decreasing function of the probability of the event happening in a single trial.
- If the probability of the event is greater than 0.2, it is more likely that the event will happen one out of five trials than zero out of five.
- If the probability is greater than 0.4, it is more likely that the event will happen two out of five trials than one out of five.

Applying these probabilities to the field failure data indicates the following:

- It is unlikely that thermal cycling and vibration are significant contributors to failures of these modules. If, for example, 1/2 (50%) of the failures were from thermal cycling and vibration, the probability of getting zero in five trials would be only 1/32 (3%). It appears unlikely that much more than 20% of the failures are from thermal cycling and vibration.
- In the same way, it is unlikely that the exacerbation of latent defects by environmental stresses is a significant contributor to failures of the P/N 3562102 SRUs. It appears unlikely that much more than 20% of the failures are of this type.
- The exacerbation of latent defects by environmental stresses appears to be a significant contributor to failures of the P/N 356900 SRUs. This is the cause or probably not much less than 60% nor much more than 80% of the failures of the 9800 modules.

The effect of increasing the sample size is shown in Figures 3-2 through 3-4. As the number of trials increases, the probability that X/n is close to P (the expected value of X/n) increases. With a relatively small sample (n=16), the distribution of probable outcomes peaks around X/n = P. However, Figure 3-4 shows that dozens of samples are required to achieve a high probability that X/n will be very close to P. It appears unlikely that obtaining a larger sample size would change the qualitative conclusions based on the sample of five.

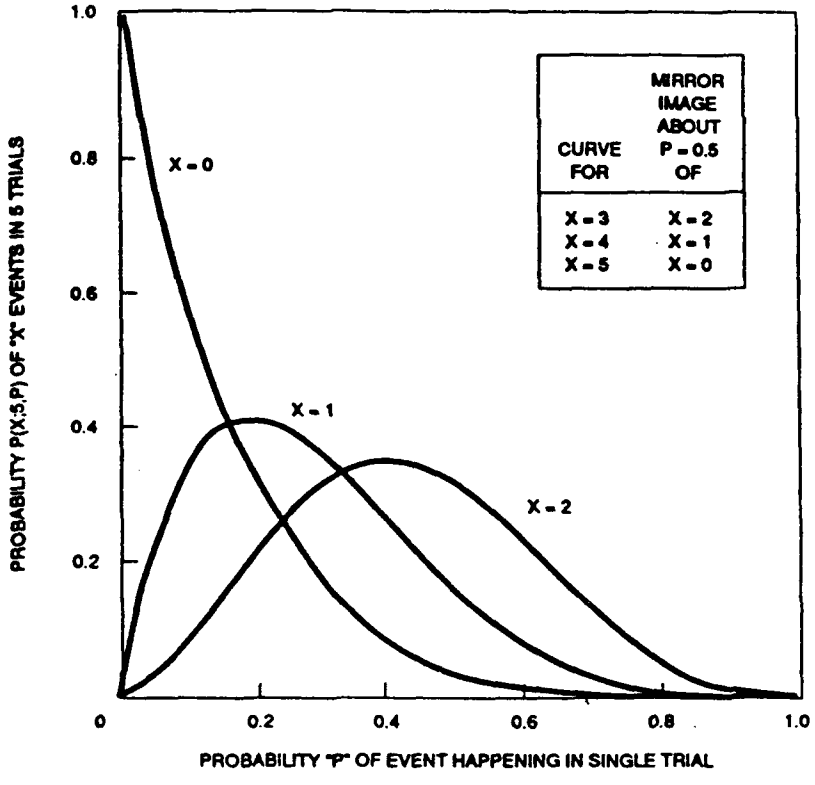


Figure 3-1. Bernoulli Process for Five Trials

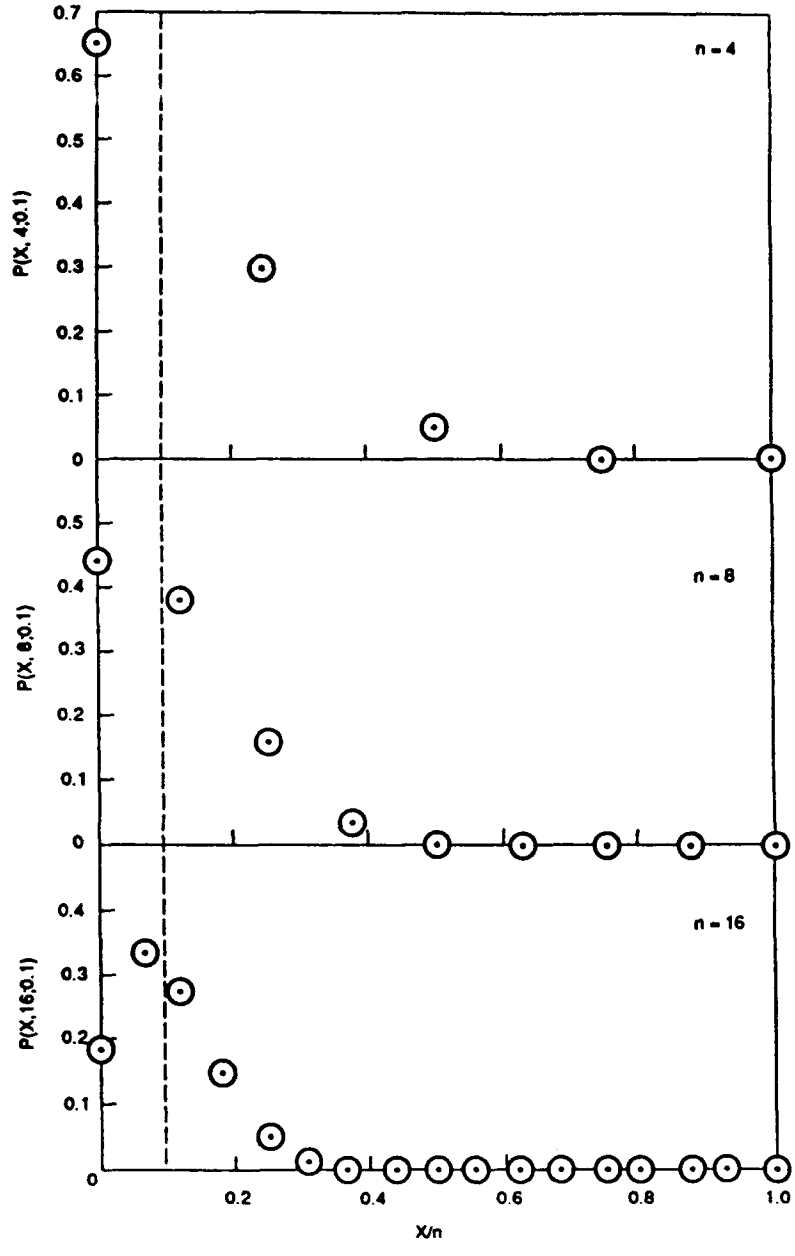


Figure 3-2. Effect of Sample Size for P = 0.1

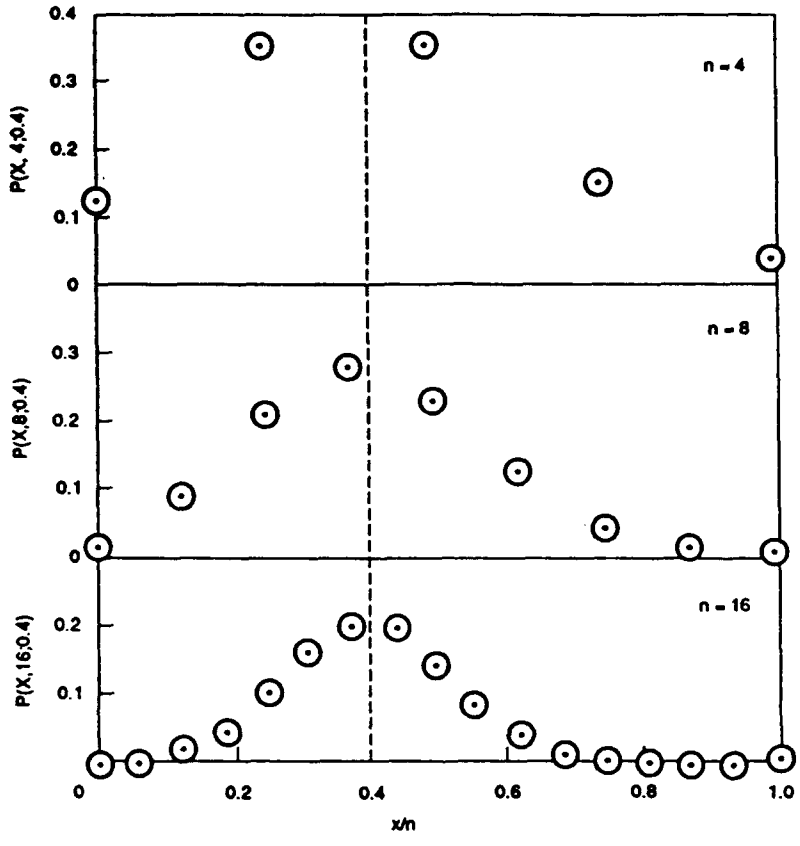


Figure 3-3. Effect of Sample Size for P = 0.4

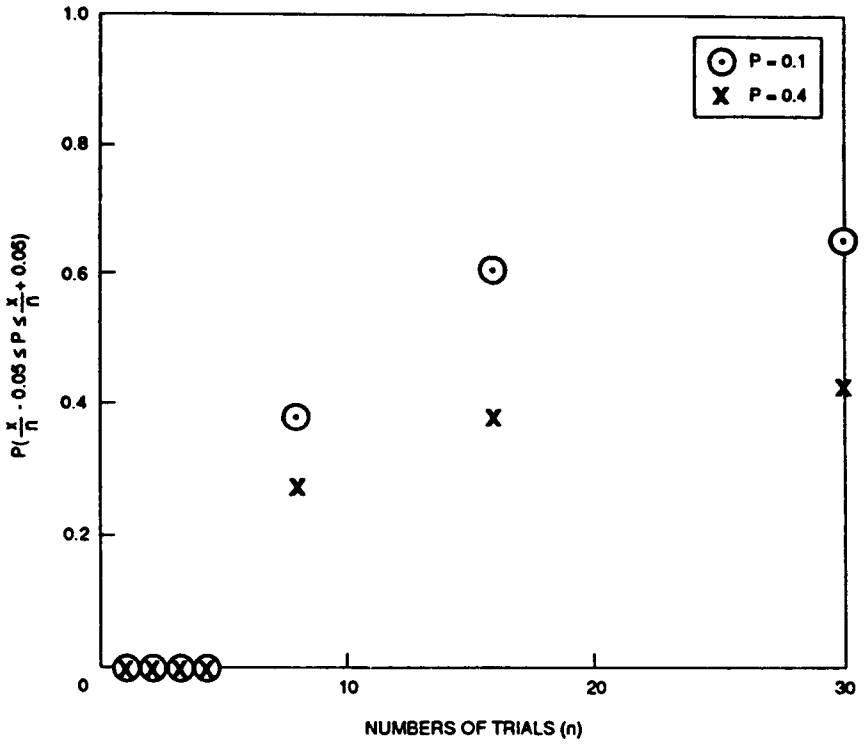


Figure 3-4. Probability that Outcome will be Within ±0.05 of Distribution

3.7 CONCLUSIONS

1. Failed field modules from the F-15 APG-63 Radar were obtained from Warner Robins Air Logistics Center for failure analysis. There were five confirmed failures of each of the two part numbers investigated. A statistical analysis of these failure data indicates that the following qualitative conclusions can be reached:
   - A significant fraction of the failures of the analog module and a small fraction for the digital module result from the exacerbation of latent defects by environmental stresses. For the digital module none of the five confirmed failures was from this result, indicating that the fraction in the total population is probably not much more than 0.2. For the analog module, four of the five confirmed failures are from this result, indicating that the fraction is probably not much less than 0.6 nor much more than 0.8.
   - These five analog modules were in deployment for more than 5 years before they failed.
   - The fraction of failures resulting from thermal cycling and vibration is small. Zero of the five confirmed failures of each part type was from this result, indicating that the fraction is probably not much more than 0.2.
   - Increasing the sample size would provide more confidence in the precise values of these fractions but probably would not change these qualitative conclusions.
2. Procedures for determining the cause of field failures of electronic assemblies in an ongoing military program were developed and used successfully. The ERFM activity did not impact the inventory of assets at WR-ALC. A small sample of failed modules was sufficient. All SRUs analyzed were returned serviceable or with only the failed component removed.
3. Standard failure isolation, verification, and analysis techniques were used. Recently developed NDI techniques - digital X-ray laminography and holographic interferometry - were evaluated and not selected for use. The conclusions regarding these techniques are as follows:
   - Digital X-ray laminography
     - It has the potential to differentiate between the sides of a two-sided module.
     - The radiation dose is well below the threshold for any potential damage to the bipolar components on these modules.
     - The film based method did not demonstrate sufficient sensitivity.
   - Holographic interferometry
     - For inspection of a small number of modules, detailed visual inspection is more cost effective.

Furthermore, identification of ionic contaminants responsible for component failure from mobile ionic contamination was concluded to be impractical due to the difficulties of performing surface analysis at liquid nitrogen temperatures.

3.8 RECOMMENDATIONS

1. Conduct an investigation like the one described here for hardware whose deployment history can be tracked by serial number. This will ensure that the sample is random and that the field failures are the first of each S/N. Several data bases having this capability are available at Hughes, including that for the APG-70 radar developed under the Multi-Staged Improvement Program (MSIP) for the F-15 aircraft.
2. Investigate nonfilm based methods for performing X-ray laminography.

3.9 FAILURE MECHANISMS SELECTED FOR MODELLING

The following failure mechanisms were selected for modelling in this program:

* 1. Hybrid microcircuit failure from mobile ionic contamination
* 2. Hybrid microcircuit failure from surface contamination
3. Bond wire fracture
4. Plated through hole fracture

The contamination modelling is described in Section 5.0. The fracture modelling is described in Volume 2.

* Observed in SRUs examined in this program

4.0 SPECIAL FABRICATION/INSPECTION

This section is summarized in Ref. 4-1.

4.1 SUMMARY

This section presents the results of Hughes' plan for the special fabrication and inspection in Task IX of two Timing and Control (2102) modules and two Linear Regulator (9800) modules on the Hughes APG-63 Radar production line. This section of the report describes how Hughes inspected these modules during the production process so that the location and size/severity of each of the significant latent defects would be known or at least bounded within known limits. The following features of the module fabrication are discussed:

- The locations in the modules for special nondestructive inspection (NDI) were selected with the aid of failure data from the ERFM program and previous investigations. The locations are:
  - inside the hybrid microcircuit and the prepackaged semiconductor parts
  - the heat dissipator
  - the bond between the printing wiring boards (PWBs) and the heat dissipator.
- The standard NDI techniques applied as well as holographic interferometry.
- Procedures established to ensure that the identity of the four specially fabricated modules was maintained during the production process.
- The steps taken to ensure that the hardware quality is representative of that resulting from the normal production process.
- Allowance for the finite yield of parts during the production process, so that all the semiconductor parts on the four specially fabricated modules will have undergone the special NDI.
- The Hughes factory and hybrid microcircuit vendor special handling requirements for the ERFM modules.
- Results of the special NDI.

4.2 REQUIREMENTS

Two serial numbers of each of the two SRUs selected in Section 2.0 were to be fabricated. The four modules were to be specially inspected at various steps in the production process so that the location and size/severity of each of the significant latent defects would be known/bounded.

4.3 ERFM FABRICATION ORDER

4.3.1 SRUs

The two SRUs were chosen after the review of the failure data, failure analysis of field SRUs and a review of the SRU fabrication process. The two SRUs selected were the Timing and Control Module (3562102) and the Linear Regulator Module (3569800). The serial numbers of the specially fabricated SRUs are listed in Table 4-1.

TABLE 4-1. SERIAL NUMBERS

P/N 3562102

SRU	Front PWB	Rear PWB
0001	3786	31074
0002	10800	71082

P/N 3569800

SRU	U1	U2	U3
1149	11650	8355	8388
1150	11789	7941	8872

4.3.2 Normal Production Process

The 2102 and 9800 modules were built per the normal production process with special attention taken to ensure that no extra care was given to this module build process. The goal was to produce a typical module through an established production line without artificially modifying the assembly to produce a superior product.

These modules were ordered as spares. When this order was placed, the APG-63 had gone out of production except for spares. The spares production process is the same as for modules to be assembled into deliverable radar systems, except for the last two of the three steps of environmental stress screening (ESS). Modules in deliverable systems are screened at the module, unit, and system levels of assembly. Spare modules are screened in a special way to subject them to environmental stresses similar to those in unit and system level ESS of deliverable systems.

4.3.2.1 Timing and Control Module

Many steps during fabrication can be automated or done manually at the requestor's option. During the early stages of fabrication parts are kitted. The kitting of parts facilitated keeping identity of parts for ERFM.

The normal quality control and inspection performed are as follows:

- Printed Wiring Board electrical test

- Airflow and pressure drop measurement
- Solder joint inspection (visual only)
- Environmental Stress Screening (ESS) (done at Module, Unit and System levels).

The typical fabrication process for the digital modules is as follows:

- Manufacture of the Printed Wiring Board.
- Bond the PWB to the Heat Dissipator/Manifold (P/N 3562150-25 PWB Assembly).
- Airflow test of the PWB Assembly.
- "Kitting" of the PWB Assembly and the applicable components into a Manufacturing Kit. This Kit is then usually put into a bonded store room and released to be assembled at a later date.
- Add components (mechanized assembly) and operator review.
- Add components (manual assembly) and operator review.
- Assembly (Module) Conditioning. This is a 23-hour test that consists of changing the temperature from -60 degrees (C) to +95 degrees (C) at the rate of 15 degrees (C) per minute.
- First test (test T1) and subsequent rework.
- Second test (test T2) and subsequent rework.
- Inspection of SRU by PA/QA function.
- Bond components and parylene coat the SRU. Inspection of bond and parylene coat.
- Inspection of SRU by PA/QA function.
- Power On Screening.
- System Burn In for three failure free cycles.

4.3.2.2 Linear Regulator Module

Hybrid Microcircuits

The hybrids used in the build of the 9800 module are purchased parts. Presently, there are three approved vendors. They are Teledyne of Dedham, Massachusetts; Data Device Corp. of Bohemia, New York; and Hughes Newport Beach, California.

Module Assembly

The typical fabrication process is as follows:

- Manufacture of the PWB.
- Bond the PWB to the Heat Dissipator/Manifold (P/N 3569805-1 Regulator Subassembly).
- Airflow test of the Regulator Subassembly.

- "Kitting" of the Regulator subassembly and the applicable components into a Manufacturing Kit. This Kit is then shipped to Hughes-South Carolina for assembly.

All required test (including Assembly/Module Conditioning), rework, and inspection is performed in South Carolina. Bonding components and parylene coating the SRU, as well as inspection of bond and parylene coating, are also performed in South Carolina.

- Return of the complete SRU to Hughes-El Segundo.
- Power On Screening.
- System Burn In for three failure free cycles.

4.4 APPROACH TO DEVELOPING SPECIAL FABRICATION AND INSPECTION PLAN

This plan (Ref. 4-2) was developed per the following factors:

- The program requirements and objectives
- The failure data for the selected modules
- The state of the art of NDI
- The characteristics of the Hughes production process.

The approach to developing the plan was as follows:

- The normal production process was examined to identify:
  - where and how the fabrication process occurs
  - what problems and pitfalls could be anticipated in the special handling required for ERFM
  - what steps provided opportunities for diversion of the hardware for special NDI.
- The failure data were examined to identify the locations in the modules and the steps in the production process at which special NDI was to be performed.
- A draft of the desired plan was prepared and was reviewed with Hughes radar production managers, Hughes hybrid microcircuit specialists, and the hybrid microcircuit vendors. A final draft was then prepared. Fortunately, little change to the draft plan was required as a result of the review.

Hughes identified the following pitfalls and methods for avoiding them:

- *Maintaining identity of ERFM hardware.* The specially inspected ERFM hardware could get lost or mixed up with the normal production hardware at a number of places in the production process. To prevent this, the following features were included in the ERFM plan:
  - A person was assigned to follow the kits through production. A backup person was available in case of the temporary absence of the primary person. The normal Hughes kitting procedure helped to maintain identity of the hardware.

- The ERFM parts not having serial numbers, such as prepackaged semiconductors, were marked to identify them as ERFM parts. Parts used more than once in a module were serialized so that the location of a specific part in the module could later be identified.
- Where a choice could be made, a manual process was selected over an automated one to enable better vigilance of the hardware.

- *Obtaining modules having the same quality as in normal production.* There was a risk of damage to the hardware when the hardware was diverted for special NDI. To prevent damage, the special NDI techniques were selected with care and transportation and handling of the hardware were minimized. There also was a risk of obtaining unusually high quality hardware. One possible cause would have been if factory personnel knew their work was being evaluated and tried harder than usual to do a good job; to prevent this from happening, efforts were under taken to shield the assemblers from knowledge of the special nature of the ERFM hardware. The nature of the factory, which processes a variety of high- and low-rate production runs, helped in this endeavor. Another possible cause would have been if more stringent than normal quality control had been performed; accordingly, we decided to perform only the normal procedures and not, for example, employ a more severe environmental stress screening regimen than is normally used.
- *Accounting for the finite yield of parts.* A finite fraction of parts typically fails a test at some point in the production process and is rejected. A replacement part then is put into the kit. In the case of hybrid microcircuits, the yield is typically 30-40%. Consequently, to obtain four modules having specially inspected parts, special provisions were made. In the case of prepackaged semiconductor parts, these provisions were facilitated by the normal production process. The parts in the ERFM kits were specially inspected and put back into the kits. If a part had later failed an electrical test, the failure would have been documented as part of the normal production process. The replacement part would have been marked, specially inspected, and put into the kit. In the case of hybrids, the ERFM program placed an order for more than the six hybrids required for the two 9800 modules. The extra hybrids can be used to replace any that fail in the CERT test; this will enable Hughes to economically satisfy the contractual requirement to deliver the SRUs to the AF fully functional at the end of the program.

In developing the plan, a number of options were considered. These options, and the rationale for the selected option, are discussed below:

- *Manual vs. automated production.* Several key steps in the production process can be manual or automated, at the requester's option. Hughes decided to specify that the preparation of parts and the soldering process be manual, rather than automated. The factory recommended that the preparation of parts (lead forming, tinning of leads, etc.) be manual to lessen the risk of mixing up the ERFM parts with those for other programs. These steps are performed manually for some programs, and the hardware quality is expected to be comparable to that for automated preparation. The factory prefers that the soldering be manual, because it is more convenient for them to do a small lot manually than with a wave soldering machine. There is a risk that the solderers will produce exceptionally high quality solder joints if they know their work will be specially

evaluated; we endeavored to prevent their learning the special nature of the ERFM program.

- *Environmental stress screening (normal vs. special).* Hughes concluded that the normal ESS process should be followed. To impose a more severe regimen could have been counter productive to the contract objectives. It could have resulted in higher quality hardware than normal and could have resulted in an untypically long failure free operating period. If a more severe ESS regimen is appropriate, it can be recommended separately from the ERFM program.
- *Where to do special inspection.* This decision was based on the failure data obtained in this contract and in previous investigations. These data indicated that failures in delivered hardware occur primarily in the parts. Defective solder joints and PWBs usually are caught in the normal inspection and quality control process and rarely show up as field failures for this class of equipment. (Solder joint and PWB field failures are expected to be more significant for more modern equipment having leadless chip carriers and more complex PWBs.) Accordingly, the plan included no inspection of solder joints or PWBs other than that in the normal production process.

4.5 SPECIAL INSPECTION AND FABRICATION PROCEDURE

4.5.1 Test Specimen Tracking and Control

4.5.1.1 Assignment of Personnel to Follow Fabrication

One person was assigned to follow the ERFM parts through the fabrication process. He ensured that ERFM parts were stopped at critically identified times to inject special NDI techniques per the Special Fabrication Route Plan. He also witnessed the assembly steps and recorded information, such as the occurrence of rework, not recorded in the usual production process.

4.5.1.2 Identification of Parts

Identification of components was a concern for the timing and control modules (P/N 3562102) but not for the linear regulator modules (P/N 3569800). The timing and control module uses over 200 active devices, with 45 different part numbers and up to 24 components of the same part number per module. The linear regulator module uses only a comparatively small number of devices which are of interest. The hybrid microcircuits are already serialized, and there is only one other instance of two components of the same part number.

Originally, Hughes had planned to maintain identity and serialization of the components through a binary code. This binary code was to be series of different colored paint dots, to be applied to the cases of the ERFM parts, such as prepackaged semiconductor devices. However, when it came time to mark the parts, a marking press became available which could easily print

standard serial numbers on the device packages. This eliminated the need for the potentially cumbersome binary code. All marking materials were epoxy inks which conform to MIL-I-43553 (Rei 4-3) and Hughes Standard HP 8-5 (Ref. 4-4) to ensure that the parts would not be damaged and that the conformal coating would adhere. This provided a permanent and easily readable serialization method. A waiver, qualifying these specially marked modules for the same uses as normal products, was obtained.

4.5.2 Special Nondestructive Inspection

4.5.2.1 Nondestructive Inspection Techniques Used Specially for ERFM Test Specimens

Several nondestructive inspection (NDI) techniques were applied to the ERFM test specimens during fabrication in addition to the normal quality assurance inspections. In some instances, the normal tests or inspections are applied with pass/fail or go/no go criteria. Where this was the case, such as in the air flow measurements performed on the heat exchangers, the raw data were retained for analysis by ERFM personnel. Where tests normally performed are done only on a sampling basis, such as in coupon testing of printed wiring boards (PWB), samples from material or component lots used in the fabrication of the ERFM modules were used.

NDI of the component parts of the modules and the finished assemblies included such techniques as holographic interferometry, X-ray inspection, hermetic seal leak testing, PIND (Particle Impact Noise Detection) testing and measurement of junction to case thermal resistance (θ_{JC}). NDI techniques applied to the hybrids used on the linear regulator modules were performed at the hybrid vendors facility. These tests will be discussed separately at the end of this section. In addition, a hybrid contamination screen was devised and implemented. This screen is discussed in Section 5.0.

Holographic interferometry (HI) was used at several points in the fabrication of the modules. Initial application of the HI was used to evaluate the integrity of the face sheet to fin stock braze on the heat exchangers. At the same time in the fabrication process, the individual PWBs were also evaluated by means of HI for interlayer delaminations. HI was also applied at later times in the fabrication process to evaluate the PWB to heat exchanger bonds, and effects of the soldering process, electrical testing, and burn-in on these bonds. The HI analysis is presented in the HI subcontractor's final report, attached as Appendix D, and is summarized in Ref. 4-5. The PWBs with which the technique was calibrated are described in Appendix E.

X-ray inspection of all active components was performed. The primary consideration for the X-ray inspection was to determine the condition of the die attach in each device. A secondary consideration was to evaluate any gold bond wires in the packages.

As stated in the special fabrication and inspection plan, Hughes did not intend to evaluate aluminum bond wires in the component packages because of the difficulty in radiographically imaging these wires. However, Hughes did look into potential techniques for doing this. Two methods were found, which with further development could have the capability to evaluate these wires in electronic component packages. These techniques are low energy X-ray and X-ray computed tomography. Unfortunately it would not have been appropriate for the ERFM program to fund the development of these techniques for this application.

Both fine and gross leak tests were performed on all active devices. Although leak testing is performed as a standard quality assurance measure at the component vendor's facility, these data were not available to Hughes. Therefore, leak testing was necessary to obtain the leak rates of the component packages for inclusion in the life model analysis.

Initially, Hughes had planned to perform junction to case thermal resistance (θ_{JC}) measurements of all active devices. This proved to be prohibitively expensive. Instead, Hughes decided to perform θ_{JC} measurements only on those components which dissipated the most power and occupied the hottest positions on the modules, as indicated by thermal analyses performed by Hughes (Appendices F and G). In addition, some devices which later were shown to exceed MIL-STD-883 X-ray requirements for die attach voiding, and occupied some of the hotter positions on the modules, were also measured for thermal resistance. The technique is described in Appendix H, and the measurements are reported in Appendix I.

NDI of the hybrid microcircuits for use on the linear regulator modules was performed at the vendor's facility since it was determined that removing the hybrids from the manufacturing environment would have posed an unacceptable risk for introducing contamination. Hughes negotiated with the vendor to make available to Hughes the results of all quality control inspections. These inspections included a lot sampling scanning electron microscope (SEM) evaluation of the metallization quality of the integrated circuit (IC) devices used in the hybrids, X-ray evaluation of the device die attach and substrate bonding, θ_{JC} measurement, leak testing, and bond pull.

4.5.2.2 Points in Fabrication Process at Which Special Nondestructive Inspection Techniques were Used

Although the linear regulator module and the timing and control module are much different in terms of complexity, the manufacturing steps are very similar. Therefore, the points in the fabrication process at which NDI was applied that will be described in this section apply to both modules.

The first point at which special NDI techniques were applied to the modules was prior to the bonding of the PWBs to the heat exchangers. Holographic interferometry was used to determine if any debonding existed in either the PWBs or in the heat exchangers. When the PWBs were

bonded to the heat exchanger HI was again applied to determine the integrity of these bonds. After this point in the fabrication-process HI was applied several more times to determine if any of the manufacturing steps affected the PWB to heat exchanger bond. These points in the fabrication process included after the reflow soldering operation, after module conditioning, after power on screening, and after system burn-in.

X-ray, leak testing, PIND testing and θ_{JC} measurements of all IC devices were performed prior to the soldering operation. Hybrid microcircuit tests were performed during the fabrication of the hybrids as described earlier.

4.5.2.3 Potential for and Risk of Damage by Special Nondestructive Inspection Techniques

Holographic interferometry was the first special NDI technique applied. This technique involved the application of some stress to the modules. The stress was in the form of heating, vibration, and bursting pressure (for the heat exchangers). The stress levels involved in heating and vibration the modules were very low (see Appendix D). As an example, heating was often in the form of the technician passing his hand over the module. In the case of applying a bursting pressure, the heat exchanger was sealed on both ends and placed in a vacuum chamber where the ambient pressure was then lowered slightly. To assure that no potential for damage to the heat exchangers existed from the pressure testing, Hughes performed an analysis of the effects of internal pressure on the heat exchangers (Appendix J). This analysis showed the stress induced by the pressure testing to be benign to the heat exchanger.

It is well documented that exposure of semiconductor devices to radiation can have effects on their operation. Since the nondestructive failure analysis of failed fielded modules included X-ray evaluation, a survey (Appendix B) of the sensitivity of the devices used on these modules to X-radiation was performed. The results of this survey showed that complete X-ray inspection of the modules was possible while staying well within safety margins for the devices.

In performing gross leak testing of device packages there is the chance of introducing the material used in the process into the device cavity, and thereby introduce potential contamination. However, if this were the case, then that package would be identified as a "leaker" and would have to be replaced. Fine leak testing involves pressurizing the packages in a helium atmosphere and then subsequently checking for leakage of helium from the package. Introduction of helium into the device cavity is not a concern since it is an inert gas. In addition, the components are required to pass leak testing as a normal procedure so the packages are designed to withstand the required time under pressure.

Measurement of θ_{JC} of a device involves applying power to at least a portion of that device. Any time power is applied to a device there is the chance of an electrical overstress occurring

which could damage the device. Care in applying the test method was used to alleviate this potential problem. If any instance of an electrical overstress was suspected the component in question would have been replaced.

4.5.3 Other Fabrication Procedures

4.5.3.1 Hybrid Microcircuit Procurement

A plan to procure 10 hybrids to be used in the build was projected to satisfy the finite yield of the hybrid build process. It was planned that parts for 20 hybrids were to be specially followed and inspected, in order to guarantee a yield of 10 hybrids. Six hybrids were required for fabrication of the 9800 modules. The remaining four hybrids were available to be used as needed to replace any attrition of parts seen through the Hughes module build. The extra hybrids are also available to be used to repair modules upon the conclusion of CERT testing if needed. It was important that a sufficient number of hybrids be built initially so that schedule delays did not occur as a result of insufficient hybrid parts.

4.5.3.2 Use of Coupon Tests to Characterize Material Properties

There was only one place in the fabrication process where coupon tests were used to characterize material properties. These coupon tests were made on the standard coupons furnished with all printed wiring boards for this purpose. These coupon tests were performed to show any delamination of the boards, plating coverage in the copper plating and resin smear at the internal trace to barrel interface. Although, this test is usually done on a sampling basis, coupons for each PWB used in the fabrication of ERFM modules were tested.

4.5.3.3 Electrostatic Discharge Protection

Standard Hughes EDSG electrostatic discharge protection procedures were followed per HPR 15010, "Protection of Static Sensitive Devices (SSDs)." A copy of this standard is attached to Ref. 4-2 as Appendix B. While the modules were being built, similar ESD Radar System practices were followed.

4.5.3.4 Environmental Stress Screening

Only the existing environmental stress screening procedure was followed as per the normal Hughes fabrication schedule. It was a conscious effort not to add or subtract from the normal production build. The modules were screened at the module, unit, and system levels. The ESS specifications used are the same as those described in Section 4.3.2.

4.5.4 Fabrication and Inspection Process

4.5.4.1 Timing and Control Module

The 2102 module was built as a normal production module with the exception that it was interrupted periodically to perform special nondestructive inspections before continuing through its normal build cycle.

The build location for the 2102 module production was chosen to be Hughes Radar System Group facility in El Segundo North. The site is capable of supporting both high and low-rate production tasks. This was especially favorable for the ERFM program because the factory is accustomed to handling special requests.

A detailed route sheet/plan with the special NDI inspection points incorporated into it is attached as Appendix K.

4.5.4.2 Linear Regulator Module

Hybrid Microcircuit

Hughes Newport Beach was selected as the supplier of the hybrids. Hughes was selected rather than the two qualified external vendors for the following reasons:

- The facility had an F-15 order for the same hybrids at the time the ERFM order was placed, enabling the ERFM devices to be put into the flow with the normal F-15 build.
- A Hughes engineer was in residence at Newport Beach to monitor a major contract for devices and could track the ERFM devices.
- It is easier to obtain the detailed information on the build from Hughes than from an external vendor.
- It is easier and less expensive to communicate with Newport Beach than with the external vendors, which are three time zones away on the east coast.

Through the results of failed field module analysis, the hybrids have been identified as the main focus of most failures on the 9800 modules. The high probability of having a hybrid related failure resulted in monitoring the hybrid fabrication process to the same degree as the module fabrication process. All sample and lot testing done by the manufacturers was required on all hybrids (100% testing). All preliminary checks of specification compliances were recorded and maintained in a data log for future reference. In addition, a screen for contamination in the hybrids was developed and implemented. The details of the hybrid contamination screen and its results are explained in Section 5.0.

A hybrid route sheet from Hughes Newport Beach is attached as Appendix L.

Module Assembly

The 9800 module was built as a normal production module with the exception that it was interrupted periodically to perform special nondestructive inspections before continuing through its normal build cycle.

To simplify the special handling, the build location was chosen to be El Segundo rather than South Carolina. Because the 9800 module production had been moved to South Carolina several years earlier, special arrangements had to be made to perform some of the fabrication and testing steps in El Segundo. In all cases, test fixtures formerly used on the El Segundo production line were found and recertified.

A detailed route sheet/plan with the special NDI inspection points incorporated into it is attached as Appendix M.

4.6 RESULTS OF SPECIAL NDI

4.6.1 Holographic Interferometry

As stated previously, the outcome of the holographic interferometry inspections is detailed in Appendix D. The HI revealed no latent defects in any of the four modules. Some interesting results were noted, such as a very effective method for evaluating heat exchanger braze integrity.

4.6.2 X-Ray, PIND, and Leak Testing

All active components to be used in the fabrication of the four modules for the ERFM Program were first serialized and subjected to several inspections as specified in MIL-STD-883C. These inspections included X-ray, hermetic seal (leak testing), and PIND (particle impact noise detection). In each one of the inspections components were found which did not meet specification requirements. Findings of these inspections are summarized below.

Part Number	Quantity Inspected	Quantity Out of Spec	Out of Spec For
932827-1B	2	1	X-Ray
38510-07006	2	1	X-Ray
932753-1B	14	3	X-Ray
932749-1B	26	2	X-Ray
932728-1B	18	6	X-Ray
932726-1B	8	1	X-Ray
932736-1B	52	2	X-Ray
932849-1B	18	1	Fine Leak
932820-215	2	1	PIND

The above findings are not a complete listing of all of the components inspected for use on the four ERFM modules, but only lists those part numbers which had at least one out of specification component.

As a consequence of the ERFM Program performing additional inspections during the fabrication of two P/N 3562102 and two P/N 3569800 F-15 APG-63 modules, 18 of the approximately 450 components supplied by Hughes RSG (Radar Systems Group) stores were found to be out of specification with respect to X-ray, leak, or PIND testing requirements. In the case of X-ray and PIND testing, MIL-STD-883C does not require 100 percent screening, but 100 percent screening is required for leak testing. Therefore, at least the one component which failed the fine leak test should not have reached the assembly line. The other 17 components which did not meet X-ray and PIND requirements must be considered to contain latent defects typical of the manufacturing process.

4.7 SPECIAL PART PLACEMENT

The parts having the highest predicted temperatures of those showing anomalous die attach are listed in Table 4-2. They were selected for measurement of junction-to-case thermal resistance (Appendix I).

TABLE 4-2. PARTS SHOWING ANOMALY IN X-RAY AND HAVING HIGH PREDICTED TEMPERATURES

Part Number	ERFM S/N	Anomaly	Predicted Junction Temperature (C)*
932820-215	2	Tilted die; excess material (also indicated particle in PIND 2 of 4 trials)	84
932730-002B	13	Void extends 3/4 of die width (within specification)	60-78
38510-07006	1	Void exceeds 50%; void extends width of die	77
*Predicted junction temperatures of other anomalous parts no higher than 73C			

Figure 4-1 shows the radiography accept/reject criteria from MIL-STD-883C, Notice 4, Method 2012.6. Figure 4-2 shows a void in one of the specially inspected ICs.

As seen in Table 4-2, one of the part types having anomalous die attach is used in a number of locations on the SRU having predicted junction temperatures varying by about 20°C. This is also true for the part type found to have excessive leakage.

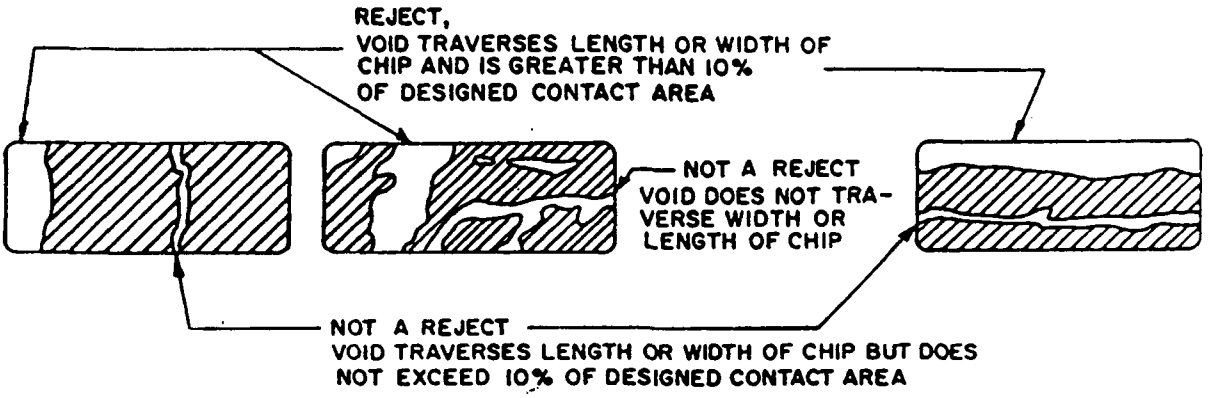


Figure 4-1. Radiography Accept/Reject Criteria

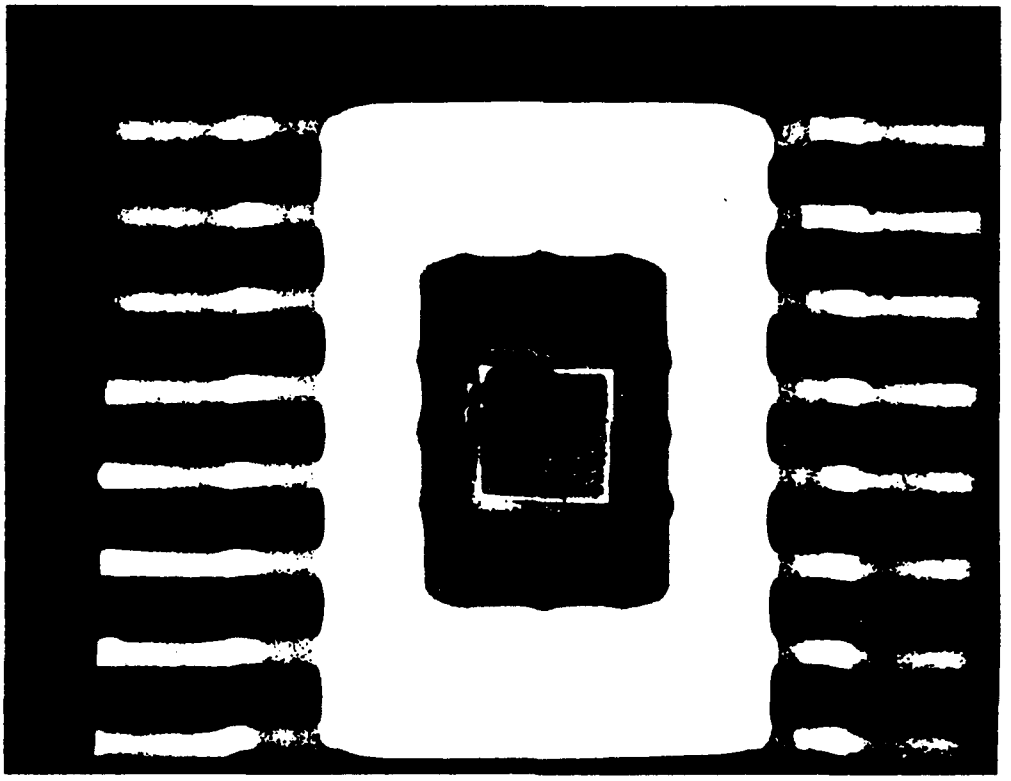


Figure 4-2. Void in P/N 932728-1B, S/N 12

These results inspired the idea of deliberately placing the anomalous parts in the locations predicted to be the hottest for the part type, thereby enhancing the probability of an early failure in the CERT – a desired outcome for the purpose of achieving the program objectives. The part placement is documented in Appendix N.

With the analog module, more hybrids were ordered and screened than were needed for the build. The hybrids showing the highest contaminant level in the special screen (Section 5.0) were selected for the two modules.

The special part placement/selection, while potentially advantageous for causing a desired early failure in the CERT, produced a potential pitfall. The specially placed/selected parts could have failed in the factory and been removed from the modules. This could have happened in the final two ESS steps, power-on screening and system burn-in, in which the modules were powered. We decided to take this risk.

4.8 RESULTS

The fabrication was a success.

A. The identity of the hardware was maintained.

B. Normal quality hardware was obtained.

   1. Abnormally high quality was avoided.

      a. The assemblers said that the presence of the ERFM team members made them nervous, thereby possibly causing the quality to be subnormal.

      b. Some assemblers were new to the job, indicating that supervision did not assign their most experienced assemblers to make the ERFM hardware abnormally high quality.

      c. Most of the assemblers assigned to the ERFM 9800 modules had never worked on the 9800 module, which could be expected to produce subnormal quality.

   2. Damage or loss resulting from the special handling was avoided.

No rejectable defects were detected by holographic interferometry. No failures (flaw precipitation) occurred in ESS. Thus the modules, containing the specially placed ICs having rejectable defects, survived all the production quality control steps.

5.0 HYBRID MICROCIRCUIT CONTAMINATION

5.1 ERFM BACKGROUND

As described in Section 3.0, field failures of the Linear Regulator Module (P/N 3569800) were analyzed as part of the ERFM program. These failures were submitted to Hughes from WR-ALC (Warner Robins Air Logistics Center). Nine of these modules were sent to Hughes for analysis. Of these nine modules, two tested good at Hughes (these failures reported by WR-ALC were never confirmed); five were confirmed to be failures; and two were confirmed to be failures at the module level but the hybrid causing the failure could not be confirmed to be a failure after it was removed from the module.

Of the seven modules confirmed to be failures, the failure was isolated to hybrid microcircuit U2 at the module level. Hybrid U2, P/N 934268, is a negative voltage regulator. Failure analyses of the seven individual U2 hybrids resulted in the following conclusions:

- Two failed due to mobile ionic surface contamination.
- Two failed due to surface contamination induced leakage currents.
- One device failed due to an unknown cause (the failure was confirmed initially, but after running the hybrid for a short period of time it recovered and could not be induced to fail again).
- Two were not confirmed to be failures.

Details of the analyses performed on the seven U2 hybrids are available in the following FARs (Failure Analysis Reports) whose cover pages are included in Appendix C:

FAR No.	Hybrid S/N	Cause of Failure
10963	451	Mobile ionic contamination
10981	300	Surface contamination
10985	555	Mobile ionic contamination
10994	127	Failure not confirmed
11002	502	Surface contamination
11033	428	Failure not confirmed
11053	344	Not determined

The preceding failure analyses did not determine the location of the failure mechanism in a specific component in each hybrid. In the case of the mobile ionic contamination failures, the

failure mechanism was implied by the behavior of the hybrid. That is, hybrid behavior would degrade after a period of time of operation. If the devices were then baked without bias, the hybrids would then function as they should for a period of time and then degrade again. This behavior is typical of mobile ionic contamination.

In the case of the surface contamination failures, a particular resistor in each hybrid was found to be out of tolerance; specifically, each was found to be too low in resistance. After a bake, the resistors would then recover to their nominal value. It was concluded that there was a surface contaminant on the resistors which could be driven off by baking.

At this point, no further detailed failure analysis was performed on any of the negative regulators. The original purpose of the ERFM field failure analysis was to determine whether mechanical failures were causing a significant number of field failures of electronic hardware. Therefore, at the point where the failure analyses determined that the hybrids had not failed due to a mechanical mechanism, the failure analyses were terminated and the cause of failure was concluded based on the data available at that point.

5.2 FAILURE MECHANISMS

Another task in the ERFM program was to model the failure mechanisms that were most often encountered during in the failure analyses performed on the hardware from the field. There were two hybrids that failed due to ionic contamination and two that failed due to apparent contamination of thick film resistors in the hybrid. Therefore, it was decided to develop models for these mechanisms:

(1) Ionic contamination induced inversion

(2) Surface contamination induced conduction.

5.2.1 Ionic Contamination Induced Inversion

If ionic contamination is present on or in the silicon dioxide that is deposited on semiconductor devices, it can alter the electrical behavior of the semiconductor device. The ionic contamination itself does not conduct current; rather it induces a mirror charge in the underlying silicon. Figure 5-1 illustrates the effect of the ionic contamination. In this illustration, the ionic contaminant is represented by "+" indicating a positive ion in the oxide over the p-n junction. The positive ions attract negative charge carriers in the underlying silicon. In the n-type diffusion, this only tends to make the surface of the n-type silicon even more n-type, an effect known as accumulation. That is, there are more negative carriers than usual which does not significantly affect the electrical behavior of the junction.

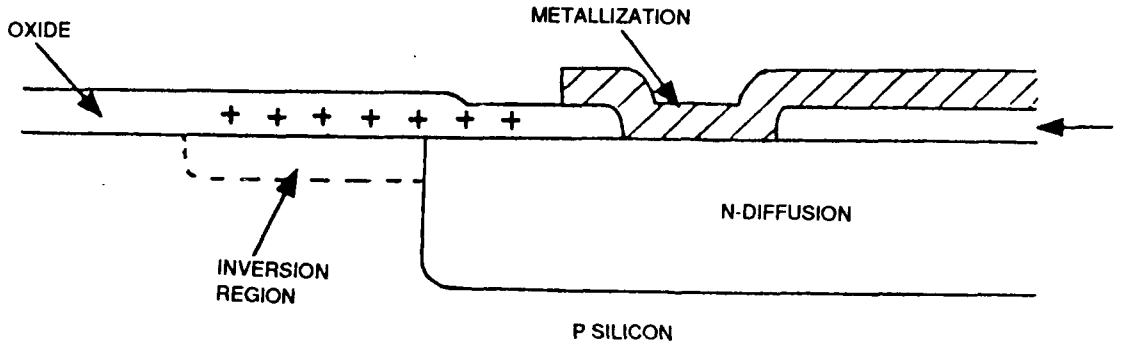


Figure 5-1. Sketch of Cross Section of Area on Semiconductor. Sodium Ions (+) in the Oxide Induce an Inversion Region in the p-Type Silicon.

In the p-type silicon, the attracted negative charge carriers offset the effect of the positive charge carriers that are present in p-type material. This tends to make the p-type material less p-type. If there are sufficient positive ionic charges in the oxide that are near the surface of the silicon in order to have the maximum effect, the positive carriers can be completely cancelled by the attracted negative carriers. This results in a condition called depletion. If the positive ionic contamination is even higher in concentration, it can attract enough negative carriers to make the surface of the p-type silicon appear to be n-type, a condition called inversion. The area where the inversion occurs is called the inversion region or inversion layer. Since the inversion layer acts as an extension of the n-type diffusion, the shape and location of the p-n junction are uncontrollably altered depending on the distribution of the contaminant in the oxide.

The inversion layer can have several different effects on the electrical properties of the p-n junction. Since the junction has been changed by the inversion layer, the leakage current may increase by orders of magnitude. Also, the breakdown voltage of the junction could be drastically decreased due to the uncontrolled doping levels in the depletion region which becomes part of the junction. In extreme cases, the n-type inversion region could bridge between two n-type diffusions previously separated by a p-type region, a condition known as channeling.

Sodium is the contaminant that is most often discussed when ionic contamination induced inversion is discussed. There are two basic reasons for this: first, sodium can diffuse fairly readily through the silicon dioxide that is present on the surface of semiconductor devices. Also, sodium is difficult to eliminate from the semiconductor fabrication process. The amount of sodium required to cause inversion in the silicon only has to be slightly higher than the concentration of the p-type dopant in the silicon. The doping levels in the silicon are typically on the order of 0.01 to 10 ppm (parts per million), which requires only 0.1 to 100 ppm of sodium in

the oxide. Even smaller concentrations of sodium could cause problems if fields on the oxide tend to drive the sodium toward the surface of the silicon and concentrate its effect.

5.2.2 Surface Contamination Induced Conduction

In this failure mechanism the contamination is directly involved in altering the electrical behavior of the circuit element. The contaminant acts as a conductor providing an alternate path for current flow reducing the effective resistance of a thick film resistor as illustrated in Figure 5-2.

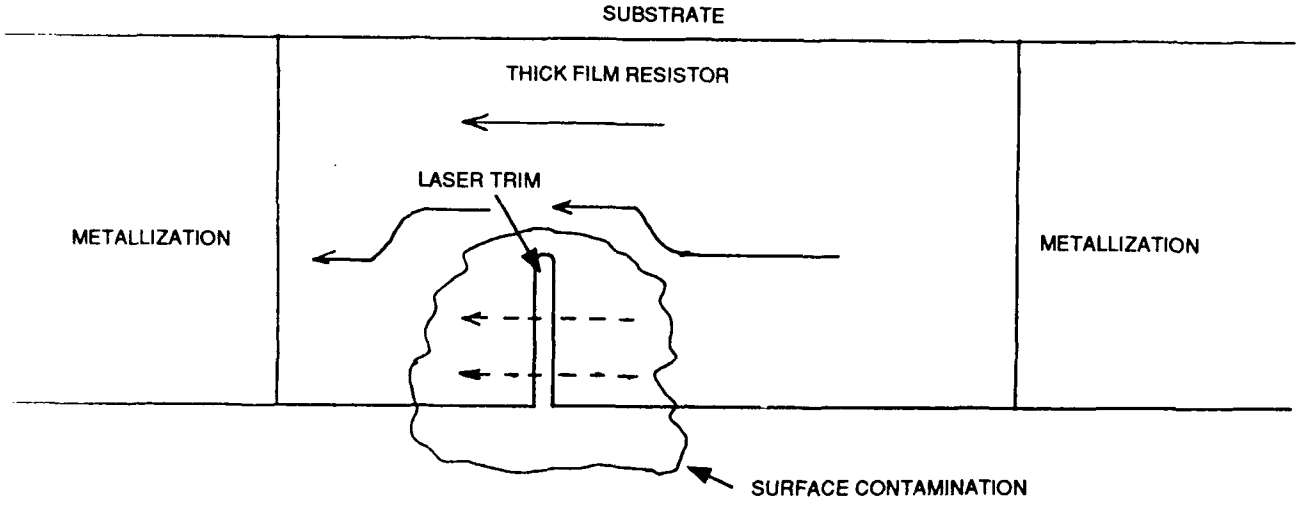


Figure 5-2. Sketch of Thick Film Resistor. Surface Contamination Causes Parasitic Current Flow (Dashed Lines) Across Laser Trim Reducing Effective Resistance of the Resistor.

When the thick film resistors are deposited, the value of the finished resistor cannot be controlled precisely enough by geometry alone. Therefore, resistors with tight tolerance requirements are deposited to be lower in resistance than required. The resistor is then trimmed to value using a laser to make a cut into the resistor element. Current is forced to flow around the laser cut through the narrowed portion of the resistor element effectively increasing the resistance of the resistor. The thick film resistors consist of metal oxides in a glassy matrix. When the laser cuts are made, the cut tends to self passivate forming an insulator over the edges of the cut area.

If the failure mechanism is present, the surface contamination diffuses through the thin insulator over the edge of the laser cut and then acts as a parasitic current path reducing the effective resistance of the resistor. In the hybrid, the specific thick film resistor affected by this failure mechanism was identified. This particular resistor value directly determines the output of the hybrid. A reduction in the resistor value reduces the output voltage of the hybrid.

5.3 ADDITIONAL ANALYSIS OF FAILED FIELD HYBRIDS

Sections 5.3 through 5.6 are summarized in Ref. 5-11.

In order to model the ionic contamination failure mechanism, additional data were required in order to determine the specific component that was being affected by the ionic contamination. In the case of the failures due to the surface contamination, a specific thick film resistor was identified as being affected by the mechanism. However, additional information was required in order to understand the failure mechanism in detail to be able to model it accurately.

5.3.1 Additional Analysis of Hybrid Failing Due to Ionic Contamination

One of the hybrids that had previously been determined to be apparently failing from ionic contamination induced inversion was subjected to additional analysis. This hybrid could be made to function correctly by baking it at 125 C for several hours with no bias applied. It could then be induced to fail by running it for several hours under normal bias conditions. The failure was manifested as an increase in the magnitude of the negative output voltage beyond specification limits. The hybrid was configured as a -12.0-volt regulator. In this configuration, the specification limits for the output voltage are -12.0 volts ±0.06 volt (±0.5%). The module that uses the hybrid imposes a specification limit of -11.75 V to -12.25 V. After the hybrid had been run for a period of time, the output increased to -14 to -15 volts.

All of the nodes in the hybrid were probed using a probe station to carefully and precisely position microprobes at various points in the hybrid circuitry. The voltages at each of the nodes were measured first when the hybrid was functioning correctly and then when the hybrid was malfunctioning. The nodes in another hybrid of the same type were also probed. This second hybrid was a hybrid that always functioned correctly. By analyzing the voltages at each of the nodes under normal and failing operating conditions and also comparing them to the voltages measured in the "good" hybrid, it was determined that the failure was associated with transistors Q1 and Q2 (see the hybrid schematic in Figure 5-3). These transistors were supposed to be matched PNP transistors. The transistors are Hughes P/N PS60071-2 which corresponds to generic P/N 2N3798. The Hughes specification for the hybrid is included as Appendix O, and the Hughes specification for the transistor is included as Appendix P. Figure 5-4 is an overall view of the interior of the hybrid with Q1 and Q2 indicated. Figure 5-5 is a photograph of Q2.

In addition to probing the hybrids to measure the node voltages, additional probing was performed. This probing was done to simulate the effects of leakage currents across various junctions of the numerous semiconductors in the hybrid. Probes were placed so that the base and emitter of a transistor were being contacted, for example. Then a decade resistor in series with

(Text continued on page 5-8.)

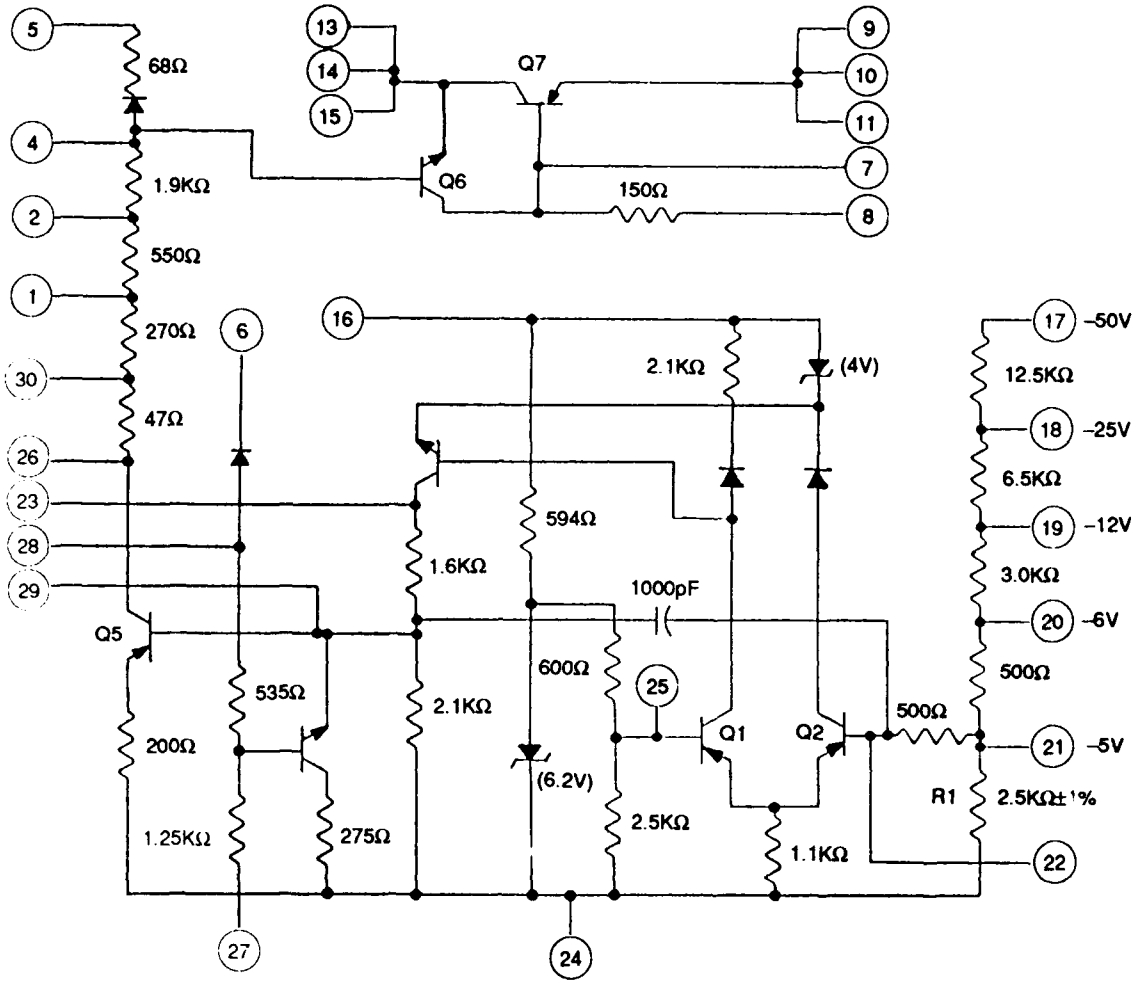


Figure 5-3. Schematic Diagram for the Hybrid

Figure 5-4. Overall View of the Negative Hybrid Interior with Q1 and Q2 Indicated

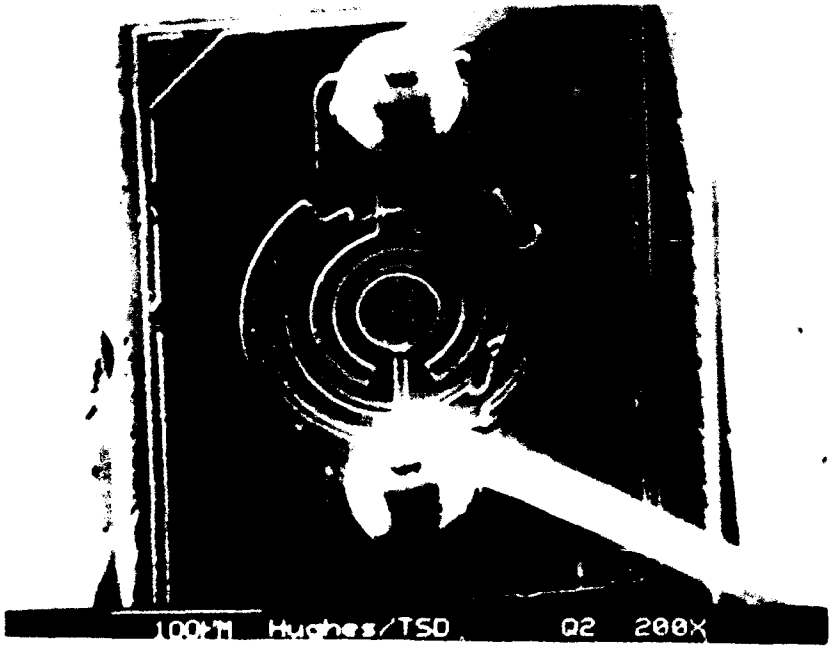


Figure 5-5. SEM Photograph of Transistor Q2

an ammeter was placed between the two points. The decade resistor was then switched until various amounts of current flowed through the parallel path to simulate a leakage current flowing across the junction. The output of the hybrid was monitored while the decade resistor was switched. This procedure was repeated until leakage currents had been simulated on all of the semiconductor devices. Transistors Q1 and Q2 were found to have the largest effect on the output of the hybrid when leakages were simulated across their base-emitter junctions. Most of the other devices required leakage currents that were orders of magnitude higher than those for Q1 and Q2 to obtain smaller effects on the hybrid output. We assume that all devices have equal susceptibilities to contamination induced leakage. Therefore, if leakages were generally induced due to contamination, Q1 and Q2 would have the largest influence on hybrid output for a given level of contamination.

Transistors Q1 and Q2 were isolated from the rest of the circuitry to measure their individual electrical characteristics. Their junction breakdown voltages were within specification limits. The base-emitter leakage current of Q1 was 7 nA which is well within the specification limit of 20 nA. The base-emitter leakage current of Q2 was 42 nA which is slightly outside of specification limits. The most significant difference between the two transistors was the value of the current gain (h_{FE}) for each of the devices. Q1 had an h_{FE} of 130 and Q2 had an h_{FE} of 10. The gains of the transistors should be matched to within $h_{FE1}/h_{FE2} = 0.85$ to 1.15.

The large difference in current gains was the most dramatic difference between the two transistors but could not be immediately explained by the other parameters. The two transistors did exhibit a slight difference in base-emitter leakage currents, but not large enough to explain the difference in current gains. For as large a difference as was seen in current gains it would be expected that the difference in leakage currents would be at least several orders of magnitude. Also, when measuring the electrical characteristics of the devices no indication of channeling was noted. The exact mechanism causing the failure was determined after a similar failure mode had been found in a new hybrid. The analysis of this new hybrid and the failure mechanism discovered to be responsible for its failure are discussed later.

The failure mechanism was, therefore, concluded to be ionic contamination induced degradation of the gain of transistor Q2. This resulted in the gain of Q2 decreasing far below that of the previously matched Q1. This apparently caused the output of the voltage regulator to increase beyond the module specification limits.

5.3.2 Additional Analysis of Surface Contamination Failures

Hybrids S/N 300 and S/N 502 apparently failed due to surface contamination on the resistor between pins 21 and 24 in the hybrid. The value of this resistor should be 2.5 Kohms ±1%. In device S/N 300 it was 2.3 Kohms and in device S/N 502 it was 2.1 Kohms. In both hybrids, the resistors returned to their nominal values after the hybrid had been baked at 125 C for 24 to 48 hours.

The hybrids were again visually examined to determine if there was any indication of contamination on the resistors, but nothing was seen in either case. The devices were submitted for SEM/EDX (Scanning Electron Microscope/Energy Dispersive X-ray) analysis. SEM examination did not reveal any indication of contaminant on the resistors. EDX analysis of the resistors did not reveal any anomalous elements on their surfaces. In both devices, the analysis was concentrated in the area of the laser trim on the resistors.

The devices were then examined using Auger analysis, a technique which is very sensitive to surface contaminants. Again, no anomalous elements were found. Traces of carbon were noted on both devices, but this is expected since the devices had been open for at least 2 months prior to Auger examination.

It was not surprising that the analysis techniques did not identify a contaminant on the resistors. Following the bakes that were performed on the hybrids, the resistors were then within specification limits. This indicates that the contaminant may have evaporated or may have been redistributed within the hybrid after the bake. Therefore, there was probably little or none of the original contamination left on the resistor.

5.4 HYBRID CONTAMINATION SCREEN

After the field failures were analyzed, two failure mechanisms were identified that were observed most often. These were ionic contamination induced inversion and surface contamination induced leakage current.

5.4.1 Hybrids Subjected to Screen

A screen was developed to identify the extent to which the identified mechanisms might be present in some new voltage regulators. These new regulators were set aside specifically for the ERFM program (see Section 4.0). (The "new" hybrids were manufactured in 1989, in comparison to the failed hybrids from the field which were built in 1981 and 1982. The new hybrids were assembled at the Hughes Tijuana hybrid facility.) They were used to test the life prediction models created as part of the ERFM program (see Section 6.0). The new hybrids, 10 negative voltage regulators and 6 positive regulators, were subjected to the screen.

The S/Ns and manufacturing dates of the various regulators are shown below. The manufacturing dates were obtained from the travelers that accompany each hybrid as it is being assembled in the fabrication facility.

Negative Regulators		Positive Regulators	
S/N	Mfr. Dates	S/N	Mfr. Dates
0480*	10/87-11/87-2/88	11650	10/88-4/89
7941	2/88-4/89	11789	11/88-4/80
8290	2/89-4/89	11836	11/88-4/89
8355	(NA)-4/89	11861	11/88-4/89
8388	(NA)-4/89	12034	11/88-4/89
8584	2/89-4/89	12183	11/88-4/89
8589	2/89-4/89		
8748	(NA)-4/89		
8872**	1/89-3/89-4/89		
8929	2/89-4/89		

NA = date not recorded (hybrid assembly was initiated on a separate traveler and then completed on the available traveler)

*S/N 0480 was initially completed in 11/87 and then reworked

**S/N 8872 was initially completed in 3/89 and then reworked

Assembly of device S/N 0480 apparently was initiated sometime before the other hybrids based on both its serial number and the dates of manufacture from the travelers. It is possible that the individual components used in this hybrid were from lots different from those of the other hybrids.

5.4.2 Development of Screen

Since contamination is the key element in the identified failure modes, it was decided that an HTRB (high temperature reverse bias) test should be performed on all of the hybrids. This is known to accelerate the effects of ionic contamination induced inversion. Following the HTRB, the devices would then be subjected to an unbiased bake which normally reverses the effects of HTRB for many forms of ionic contamination induced failure mechanisms.

A screen for the failure mechanisms found in the negative regulator hybrids was developed and consisted of the following steps (the acronyms at the beginning of each step correspond to labels used on graphs of the data from this test):

1. INEL: Initial electrical - recorded baseline data on the hybrid electrical performance

2. HTRB: Hybrids were subjected to 125 C for 48 hours; as many semiconductor junctions as possible (from external hybrid pins) were reverse biased; hybrid electrical data were remeasured after this test
3. BAK1: Hybrids were baked with no bias at 125 C for 48 hours; hybrid electrical data were remeasured after this bake
4. EL2: Remeasure electrical data (this test was included after the hybrids had been sitting for about 2 months after BAK1)
5. HTFB: Hybrids were subjected to 125 C for 48 hours; as many semiconductor junctions as possible (from external hybrid pins) were forward biased; hybrid electrical data were remeasured after this test
6. BAK2: Hybrids were baked with no bias for 48 hours at 125 C; electrical data were remeasured after this bake

The contamination screen was initially planned as documented in Ref. 4-2, Addendum No. 2. This document includes the biases to be applied during the HTRB test. The initial plan included steps (1) through (3). However, after these steps had been completed, it was noted that most of the negative regulators had shifted their output voltages following step (2), the HTRB, but then had not recovered significantly following step (3), the unbiased bake. Therefore, the screen was modified to include steps (4) through (6) to determine if any additional changes could be induced in the hybrids (Ref. 4-2, Addendum No. 3).

The biases that were applied during the HTFB test are shown below:

HTFB Bias Conditions

PIN	BIAS CONDITIONS	PIN	BIAS CONDITIONS
1	NC*	16	+10 Volts
2	NC	17	NC
3	NC	18	NC
4	GND**	19	NC
5	+5 Volts/R=1 Kohm	20	NC
6	+5 Volts/R=1 Kohm	21	GND/R=1 Kohm
7	+5 Volts/R=1 Kohm	22	NC
8	NC	23	NC
9	NC	24	GND
10	GND	25	NC
11	NC	26	-5 Volts/R=1 Kohm
12	+5 Volts/R=1 Kohm	27	-5 Volts
13	NC	28	NC
14	NC	29	+5 Volts/R=1 Kohm
15	NC	30	NC

*NC=no connection

**GND=ground (0 volts)

Notes:

1. If no resistor is indicated after a bias, connection should be made directly to the bias with no series resistor. If a resistor is indicated after a bias, that value of resistor should be inserted between the bias and the pin.
2. These conditions are for hybrid P/N 934266 (the positive voltage regulator). For Hybrid P/N 934268 (the negative voltage regulator), negative voltages of the same magnitude should be substituted for positive voltages, and positive voltages for negative voltages.

At each point where electrical measurements are indicated the following data were measured and recorded:

1. Overall hybrid functional parameters including regulated output voltage
2. Leakage currents across semiconductor junctions electrically accessible from external hybrid pins
3. Resistance values of any resistors electrically accessible from external hybrid pins.

The leakage currents were monitored as an indication of overall hybrid cleanliness as indicated by changes in the currents. The resistance values were monitored to assess the extent to which the resistor failure mechanism seen in previous hybrid failures might be present. The details of the leakage current and resistance measurements are documented in Ref. 4-2, Addendum No. 2.

5.4.3 Results of Application of Screen to New Hybrids

The 10 negative and 6 positive new regulator hybrids were subjected to the screen. The raw data taken at each step in the hybrid screen are presented in Appendix Q. The leakage current and resistance measurements did not reveal any significant information for either type of hybrid. The negative regulator hybrids had slightly more instability in the resistance measurements, but not enough to be significant.

The most significant result of the hybrid screen was the change in output voltages of the negative voltage regulators. The values of the output voltage for the negative regulators for each step in the hybrid screen are plotted in Figure 5-6. After the HTRB test, the hybrid output voltages all increased for all devices except S/N 0480, assembled at a different time than the rest of the devices and also a significantly different S/N.

The greatest change was in S/N 8584 which is shown on every graph so that it can be compared to all other devices. Also, note that the output voltages tended to stay at the high output levels all through the rest of the tests, decreasing only slightly for those showing the biggest increase after the HTRB test.

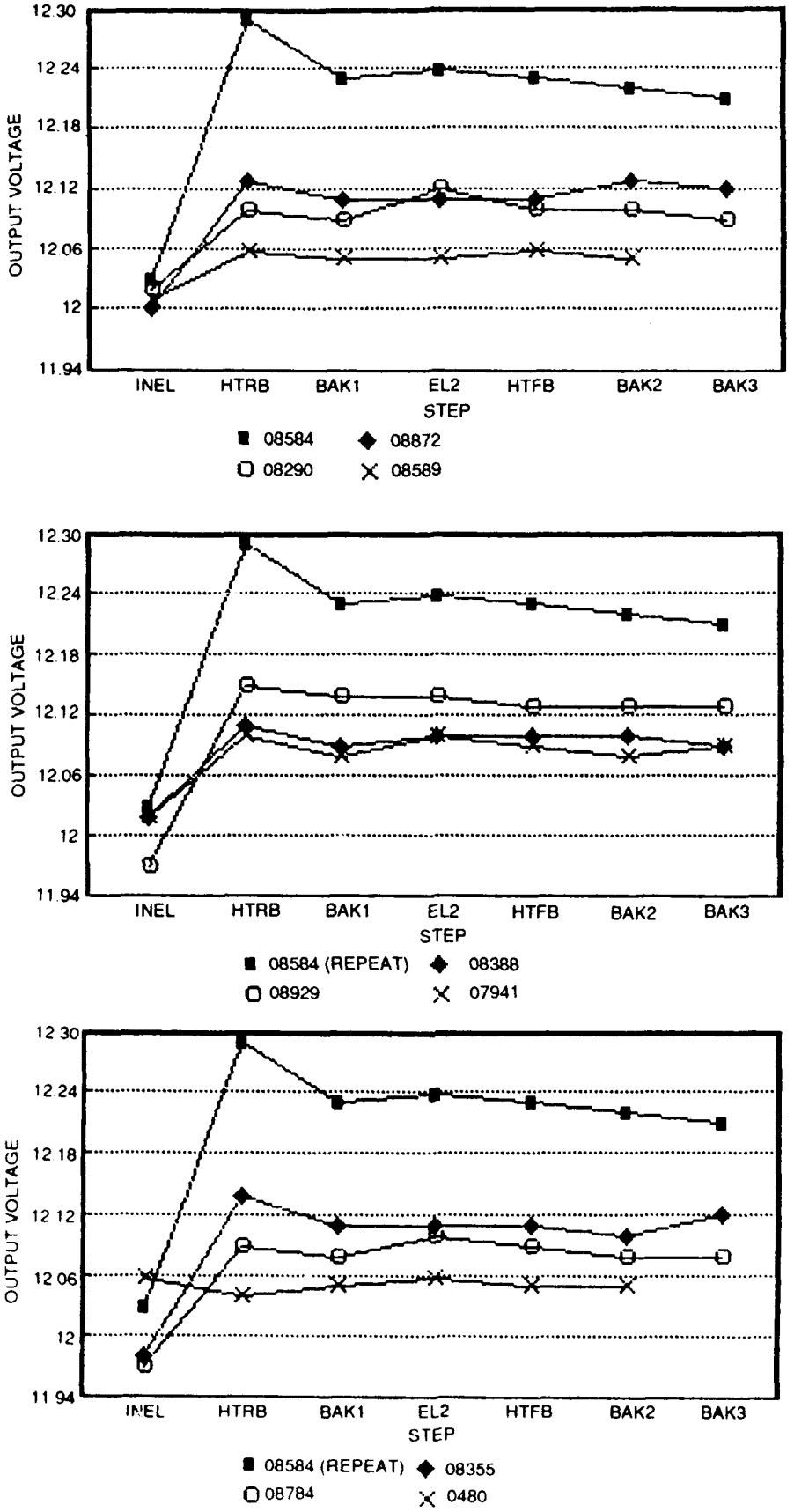


Figure 5-6. Graphs of Output Voltage at Each Step in the Hybrid Contamination Screen for Negative Regulators.

Additional intervals of HTRB were performed on the negative regulators, but their outputs never increased beyond the highest outputs observed in the HTRB performed in the screen test. This indicates that the devices have degraded to the maximum extent possible with the amount of ionic contamination present in the devices.

The output voltages of the positive voltage regulators were extremely stable all through the series of tests. Figure 5-7 shows the behavior of the positive regulators. Figure 5-8 shows expanded scales of the change in the output voltages of the positive regulators. Even on the expanded scale no significant trend is noted for the positive regulators outputs.

The screen, therefore, indicated that the ionic contamination failure mechanism is present in the new negative regulators. However, the new hybrids apparently had less contamination than the hybrids from the field as indicated by the smaller increase in output voltages. No indication of the resistor failure mechanism was distinctly noted in the new hybrids. The new positive regulators showed no indication of any of the failure mechanisms.

5.5 ANALYSIS OF NEW HYBRID

The negative regulator with the largest output voltage shift (S/N 8584) was analyzed to determine the cause of the output change. Nodes in the hybrid were probed to determine the voltage at each point. As in previous analyses of the negative regulators, the probing indicated that transistors Q1 and Q2 were causing the output voltage shift.

5.5.1 Detailed Analysis of Transistors

Transistors Q1 and Q2 were then isolated from the rest of the hybrid circuitry in order to be able to fully characterize the individual devices. The chart below shows the results of the electrical characterization.

Parameter	Measured Value(Q1 / Q2)	Specification Limit
Leakage current:		
Emitter-Base	9 nA / 36 nA	20 nA (maximum)
Collector-Base	0.5 nA / 0.3 nA	10 nA (maximum)
Breakdown voltage:		
Emitter-Base	7.6 V / 7.6 V	5.0 V (minimum)
Collector-Base	> 100 V / > 100 V	60 V (minimum)
Current Gain	120 / 25	100 (minimum)

Not only is the gain of transistor Q2 far below the specification limit, the matching between the gains of Q1 and Q2 is also well outside of the specification limit. The specification requires that h_{FE1}/h_{FE2} (where h_{FE1} is the gain of Q1 and h_{FE2} is the gain of Q2) should be 0.85 (minimum) and 1.15 (maximum). This ratio for these devices is 4.8.

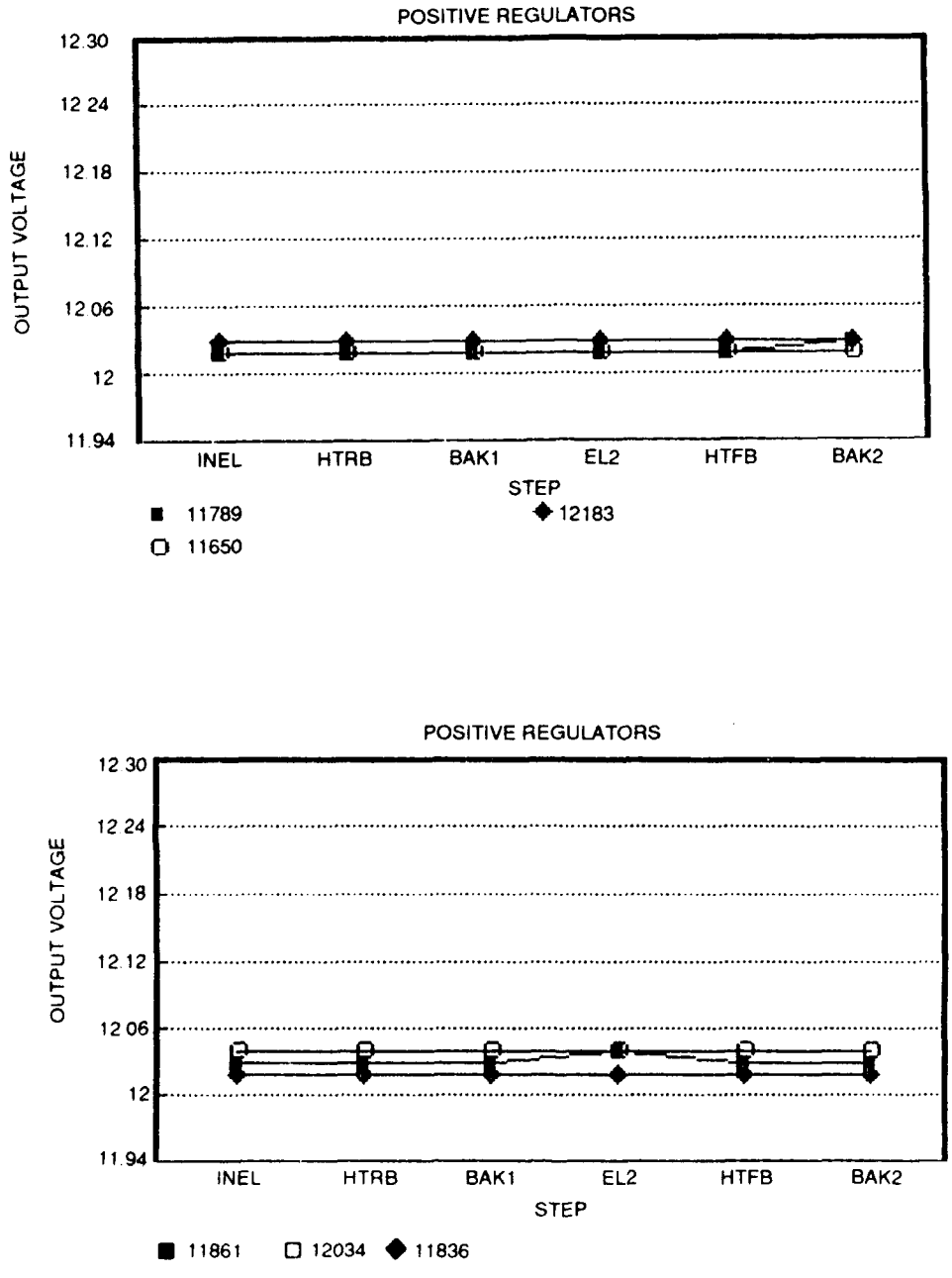
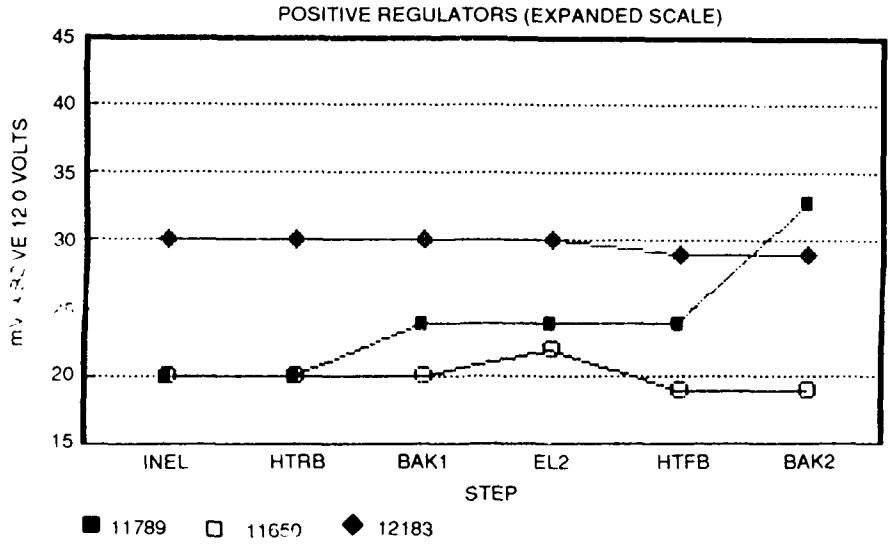


Figure 5-7. Graph of Output Voltage at Each Step in the Hybrid Contamination Screen for Positive Regulators. (Graph Axes Chosen to be Same as for negative regulators (Figure 5-6) for direct comparison.)



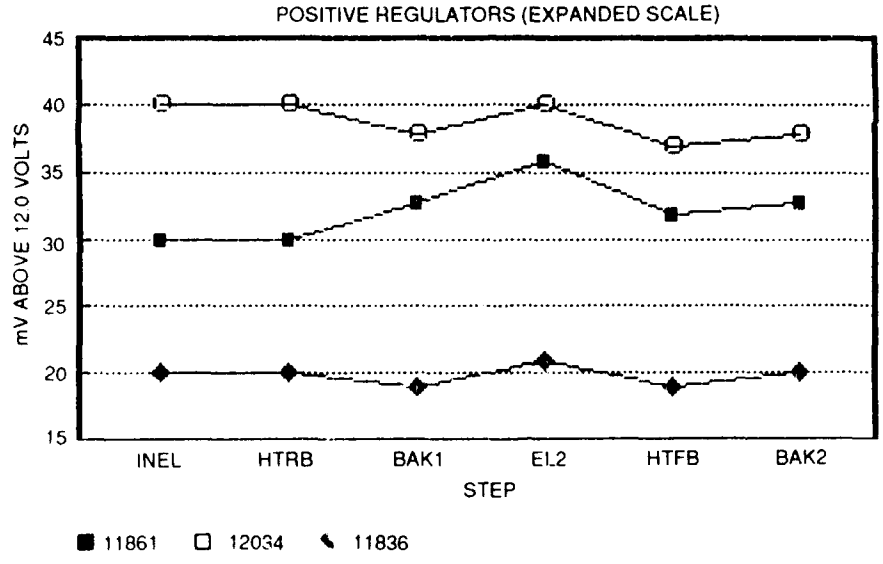


Figure 5-8. Plot of Data Shown in Figure 5-7 on an Expanded Scale. A Baseline Value of 12.0 Volts has been Subtracted from Each Output Voltage in Figure 5-7.

The large difference in the gains of the two transistors is not explained by the small difference in the leakage currents in the base-emitter junctions of the two devices. For such a large difference in gains, several orders of magnitude of difference in the leakage currents would be expected. Also, it should be noted that no evidence of a channel was noted in transistor Q2 during curve tracer measurements of its electrical characteristics.

The hybrid, negative regulator S/N 8584, was reconfigured and the transistors rebonded so that transistor parameters could be measured directly from the hybrid pins rather than having to probe to the devices every time they needed to be characterized.

In order to further evaluate the base-emitter junctions of the two devices, the ideality factor, n, was measured for device base-emitter junctions. The ideality factor appears in the diode equation:

$$I=I_S \exp(qV_f/nKT)$$

where:

I = junction current
I_S = saturation current (constant for a given device)
q = electron charge
V_f = voltage across junction
K = Boltzmann's constant
T = temperature

The value of n for a good junction varies between 1 and 2. For junctions affected by a channel the value lies between 3 and 4 (Refs. 5-1 and 5-2). In order to measure the value of n, the log of the current (I) is plotted versus the voltage (V_f) and the slope is measured. The value of n can then be calculated from the slope.

The values of n for Q1 and Q2 were measured using an automated setup that automatically applies the voltage, measures the current and calculates the value of n for various ranges of V_f. Figures 5-9 and 5-10 show the electrical data plots generated by the automated test equipment and the values of n that were calculated for Q1 and Q2. While there were differences in the values of n for device base-emitter junctions, all values were in the range of 1 to 2, verifying that there is no channel associated with either device. It can also be seen that for equivalent forward biases, transistor Q1 conducts considerably less current than Q2. This information is presented below:

Junction Current		
Junction Voltage (V_{BE})	Q1	Q2
0.12 V	10 pA	600 pA
0.20 V	100 pA	40 nA
0.30 V	1.05 nA	400 nA
0.40 V	10.05 nA	3.0 uA

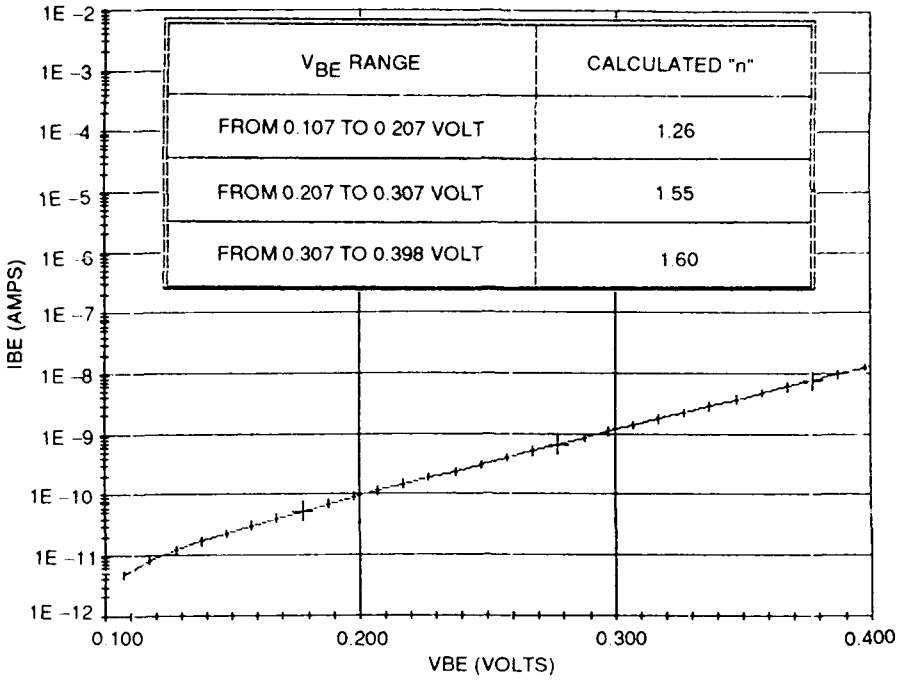


Figure 5-9. Plot of I_{BE} vs. V_{BE} for Transistor Q1. The Computed Values of the Ideality Factor, n, are Shown for Various Ranges of V_{BE}.

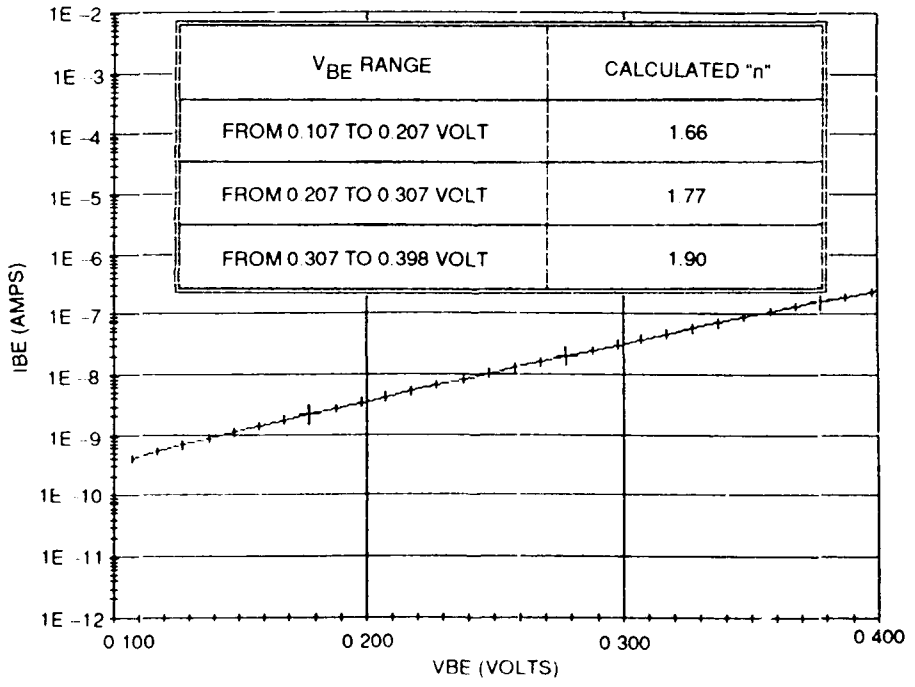


Figure 5-10. Plot of I_{BE} vs. V_{BE} for Transistor Q2. The Computed Values of the Ideality Factor, n, are Shown for Various Ranges of V_{BE}.

The cause for the higher currents in Q2 is discussed in detail in Section 5.7.3. These higher currents are directly related to the decreased current gain of Q2.

The ideality factor was also measured for the collector-base junctions. The individual behavior of this junction would have less of an influence (than the base-emitter junction) on the overall behavior of the transistor, especially on the transistor gain. The ideality factor was measured as another indication of the electrical behavior of one transistor relative to the other. Since these devices started out as a matched pair, this measurement provided more information on their present conditions.

For the base-collector junctions of Q1 and Q2, the currents for the two junctions were virtually identical except at very low forward bias voltage. The ideality factors were also very similar, again being different only at very low forward bias voltages. The differences at very low bias would not affect the behavior of the transistors at normal biases.

5.5.2 Additional Tests on Transistors

The devices were then subjected to an unbiased bake and then a period of HTRB (high temperature reverse bias). The unbiased bake was performed at 100 C for 96 hours in a nitrogen atmosphere. The HTRB was performed for 48 hours at 125 C with 5-V reverse bias on the base-emitter junction and 10 V reverse bias on the base-collector junction.

The devices were electrically characterized both after the unbiased bake and after the HTRB stress. The electrical parameters, including the ideality factor, did not change significantly after either test for either of the transistors.

The devices were examined in the SEM (scanning electron microscope) and analyzed to determine if there was any detectable contamination on the device. EDX (energy dispersive X-ray) analysis of the surface of the transistors did not reveal the presence of any contaminants.

However, EDX analysis requires that an element be present in concentrations of at least 0.1% to be detectable. There could be more than enough sodium present in the oxide on the devices to cause changes in their electrical behavior.

When sodium causes inversion in an integrated circuit, the concentration levels are on the order of 10 times the concentration of the dopants in the silicon. The dopant levels in the silicon are only on the order of 0.1 ppm to 10 ppm. Therefore, sodium concentrations of 1 ppm to 100 ppm are sufficient to cause problems. These levels will not be detected by EDX analysis.

5.6 COMPUTER MODEL OF HYBRID CIRCUIT

Previous analyses have indicated that change in gain of one of the transistors in the matched transistor pair caused the voltage output of the negative voltage regulator hybrid to change. In order to investigate the relationship between mismatch in the gains of the previously matched

transistors and the output voltage of the hybrid, it was decided to use a computer model of the hybrid circuit to simulate the behavior of the hybrid. Using this approach, different gains for each of the transistors in the matched pair were input into the computer model and then the computer model was used to determine the resulting hybrid output voltage.

5.6.1 Advantages of Computer Simulation

It would have been virtually impossible to find actual transistor chips with the correct range of gains to physically replace the transistors in the hybrid and then monitor the resulting output voltages. Also, the effort required for such an approach would have been considerable. The potential for erroneous results as the result of either mechanical damage to other components in the hybrid or contamination introduced during this type of approach would also have tended to make this type of approach unfeasible.

The only other approach that could have been attempted using actual hardware would have been to alter the function of the circuit using electrical microprobes. By probing to the interior of the hybrid and placing a resistor across the base-emitter junction of each of the transistors in the matched transistor pair, a parasitic leakage current could have been created to effectively reduce the gain of one or both of the transistors. This would still require calculation of the effective gain of the transistor in the circuit and would not be completely equivalent to actually having a transistor in the circuit with reduced gain. Again this approach would have had the possibility of erroneous results due to mechanical damage to other components in the hybrids or the possibility of the potential for contamination introduced into the hybrid.

5.6.2 Generation of Computer Model

The hybrid by itself is not a functional voltage regulator. Obviously external power supplies and input voltages have to be connected to the appropriate hybrid pins. Also, other connections and components must be applied to the hybrid depending on the desired output voltage. The hybrid is capable of supplying various regulated negative voltages (-5, -6, -12, -25 or -50 volts) depending on the input voltage applied and the various external connections. Details of the connection requirements for each voltage can be found in the Hughes Standard 934268 shown in Appendix O.

The software that was used for the circuit simulation was Microcap which is a version of SPICE. The circuit simulation included the circuitry in the hybrid plus the external circuitry and power supplies required to generate a complete voltage regulator. Initially, the circuit simulation was performed with the hybrid configured as a -5-volt regulator.

The computer model was generated by choosing a point in the circuit that was modelled and then specifying a component or components to be connected to this point. The components were

then specified that were to be connected to the other terminals of the previously selected components until the entire schematic was generated. Initially, the components were only denoted by their type and circuit number. For example, R1 for resistor number 1, C3 for capacitor number 3 and so forth. After the circuit diagram was completed, a list of the components was generated by the computer and specific values were assigned to the resistors and capacitors.

Models for various transistors and diodes have already been included in the software. Common models were chosen for each of the transistors in the hybrid circuit. Of course, care was taken to ensure that PNP models were used for PNP transistors and NPN models for NPN transistors. Simple diode models were chosen for the diodes, except in the case of the Zeners where models were chosen corresponding to the correct Zener voltage. Transistors Q1 and Q2 were modelled using the common PNP transistor model that was included in the software, except the gain was modified so that initially both transistors had equivalent gains of 120.

5.6.3 Testing the Model

The first runs of the model revealed that it took a long time (about 20 minutes) for the model to converge to a steady state solution. However, when the model did converge the hybrid circuit output voltage was very close to the specified output. The model output was -5.0002 volts when the specified output should be -5.00 volts ±0.5% (or ±025 volts).

On subsequent runs, it was discovered that the Zeners were causing the long convergence time. By replacing one or both Zeners with a power supply equivalent in voltage to the Zener voltage, the model would converge to a solution within 1 or 2 minutes. It was hypothesized that the software was having a problem with both Zeners in the circuit at the same time. Since the Zener I-V characteristic has such an abrupt discontinuity (the Zener current is zero until the Zener voltage is reached), the software seemed to be having a problem at startup, trying to reach the point where both Zeners are conducting simultaneously. However, using the power supply in place of one or both devices forces the circuit simulation to converge much more rapidly.

Using the power supply in place of one Zener caused a small shift in output voltage and replacing both Zeners with supplies resulted in a slightly higher shift. For example, with both Zeners replaced by power supplies, the output of the circuit was -5.026 volts. With the 6.2 V Zener replaced by a supply, the output was -5.020 volts and with the 4 V Zener replaced it was -5.024 volts. By trimming one of the resistors in the circuit, the offset introduced by using a supply in place of a Zener could be zeroed out without affecting the overall performance of the circuit. Most of the simulations were run with one of the Zeners replaced by a power supply in the computer model in order to speed up the convergence time. Whenever a significant change

was made in the hybrid circuit, an occasional trial run was made with both Zeners in place to confirm that the power supply was not significantly altering the hybrid circuit behavior.

5.6.4 Modelling the Regulator with Mismatched Transistors

The hybrid was then configured as a -12.00-V regulator with the resulting circuit diagram generated by Microcap shown in Figure 5-11. The individual devices in the Microcap circuit diagram have labels different from those shown in the previous circuit diagram shown for the hybrid. The transistors of interest in the Microcap generated diagram are Q12 and Q13. These transistors will still be referred to by the designation in the first schematic, Q1 and Q2, to try to avoid confusion.

The circuit was set up to provide an initial output of exactly -12.00 volts. This initial value was obtained using the gains of Q1 and Q2 both set to 120. Then the output was monitored as the gain of Q1 was decreased while holding the gain of Q2 constant. The gain of Q1 was then held constant at 120 while the gain of Q2 was decreased. Figure 5-12 shows the results of these computer simulations. It can be seen that the gain of Q2 has a much larger effect than the gain of Q1.

Additional simulations were performed where the gains of both transistors were decreased simultaneously. The results are listed:

Gain Q1 = Gain Q2 = 120; Hybrid Output = -12.00V

Gain Q1 = Gain Q2 = 50; Hybrid Output = -12.072V

Gain Q1 = Gain Q2 = 25; Hybrid Output = -12.184V

This confirmed the larger effect of Q2, causing the hybrid output to increase even with equivalent decreases in the gains of the transistors.

This explains why the negative regulator outputs always increased both in the field failures and the new devices in the hybrid screen test. Both transistors would tend to have about the same amount of contamination since they are processed the same and handled the same. But for the output to decrease, the contamination on Q1 would have to be tremendously heavier than on Q2. However, if it is about equivalent, the hybrid output increases as experienced.

5.7 MOBILE IONIC CONTAMINATION MODEL (QUALITATIVE DISCUSSION)

It has been shown that ionic contamination caused the output voltage of several negative voltage regulators to change. The failure mechanism was found to be occurring on one of a pair of matched PNP transistors. The ionic contamination diffuses through the silicon dioxide on the transistor and causes degradation of its electrical behavior.

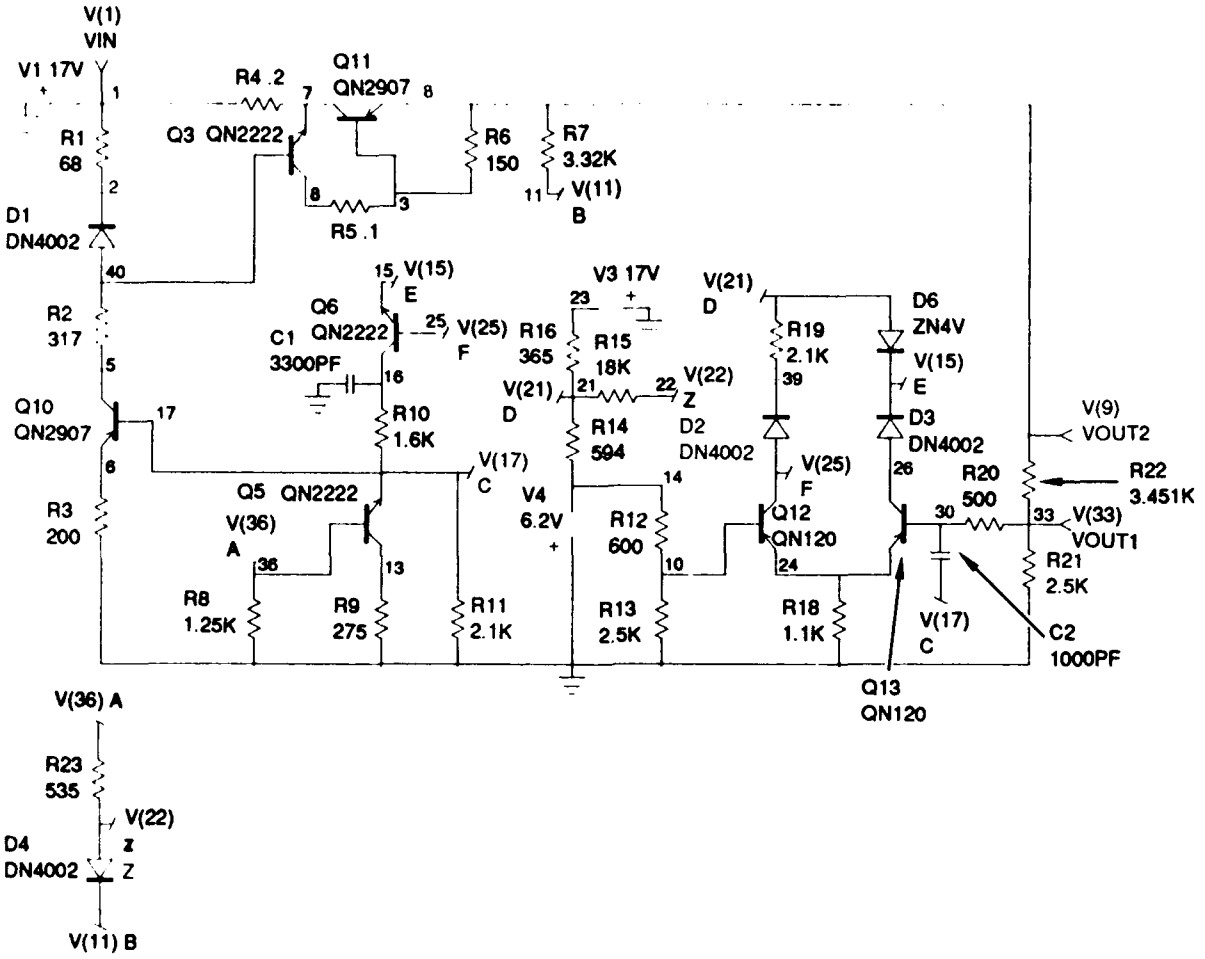


Figure 5-11. Negative Voltage Regulator Circuit Diagram Generated by Circuit Simulation Software. Includes Hybrid Circuitry Plus External Circuitry and Connections Required for a Complete Regulator. Component Labels Differ from Those in Figure 5-3. Q12 and Q13 Correspond to Q1 and Q2 in Figure 5-3. (6.2 V Zener Diode Replaced by 6.2 V Power Supply.)

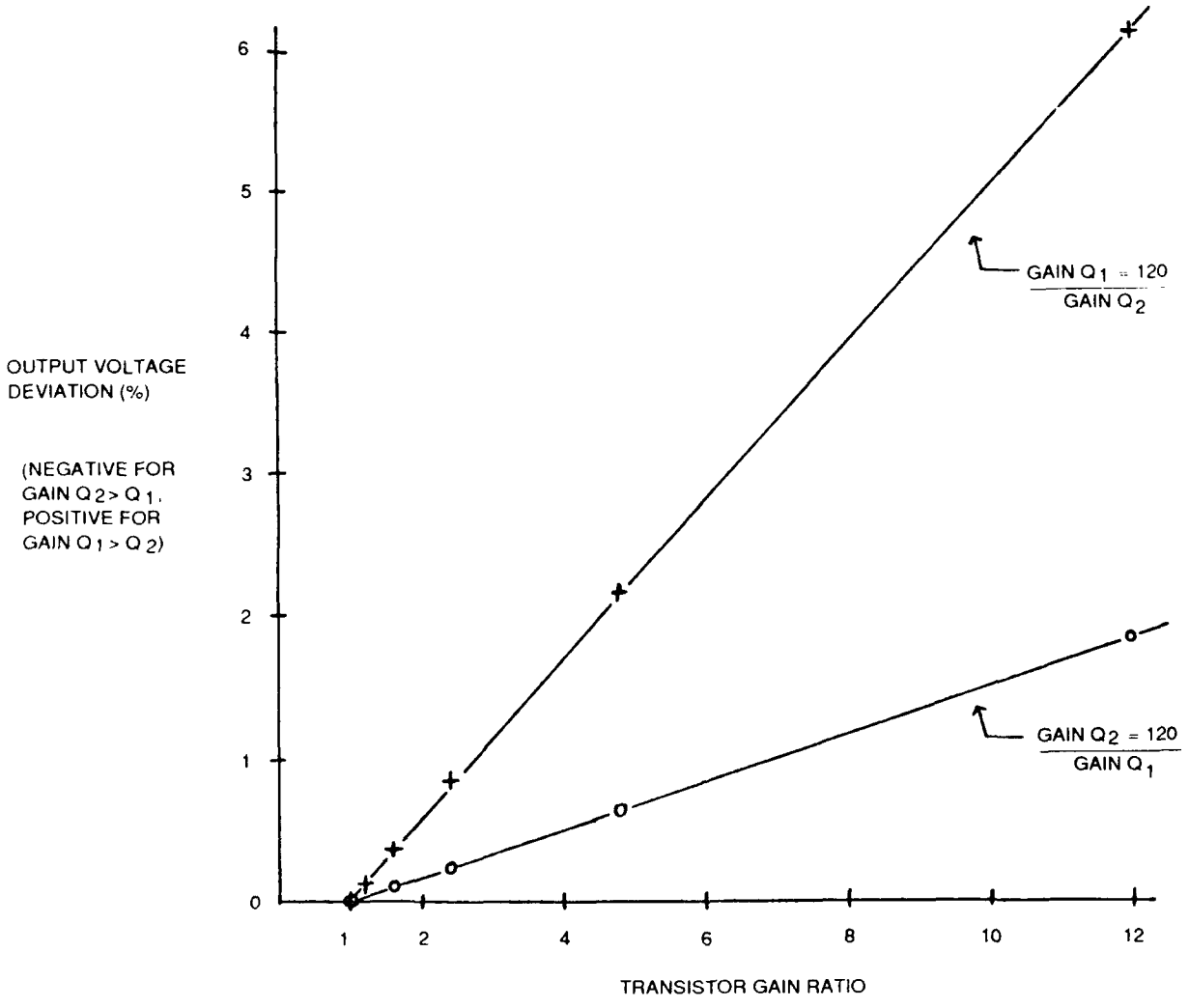


Figure 5-12. Plot of Negative Regulator Output Deviation (in %) vs. Ratio of Gains of Transistors Q1 and Q2. "+" Data Points are for the Condition where Gain of Q1 was Held Constant and Gain of Q2 was Varied. "o" Data Points are for the Condition where Gain of Q2 was Held Constant and Gain of Q1 was Varied. Data for Plots was Generated by Computer Circuit Simulation.

A model was generated to simulate the diffusion of the ionic contamination through the oxide over the semiconductor. The model also determined the resulting amount of charge that was induced in the silicon beneath the oxide and the resulting effects on the electrical behavior of the transistor.

Ultimately, the model was used to predict the lifetimes of the hybrids under known operating conditions. These hybrids were to be installed in units identical to the units in which the field failures were installed. These units were then placed in a CERT (Combined Environments Reliability Test) for a certain period of time (see Section 6.0). The CERT subjected the units to conditions that were more extreme than those that they would see in the field. Since the conditions for the CERT were carefully controlled, the stress factors could be input into the models to predict the amount of time the hybrids would operate before they failed. The failure criteria were the module specification limits for the negative regulator hybrid output voltage.

5.7.1 Detailed Transistor Description

It has been shown that the gain of the PNP transistors in the hybrids has been degraded by ionic contamination, probably in the form of sodium ions, that diffused through the passivation oxide. An initial description of the transistors was given in Section 5.3.1. This present section provides additional details needed to understand the failure mechanism that occurred in these devices.

Figure 5-5 shows a photograph of one of the PNP transistors. Figure 5-13 is a sketch of a cross section of the transistor showing how the different diffusions are located to form the p-type emitter, n-type base and p-type collector regions. The portion of the transistor that is affected by the ionic contamination is the surface of the device near the base-emitter junction. Figure 5-14 is a sketch of this area in a location where metallization passes over the base-emitter junction.

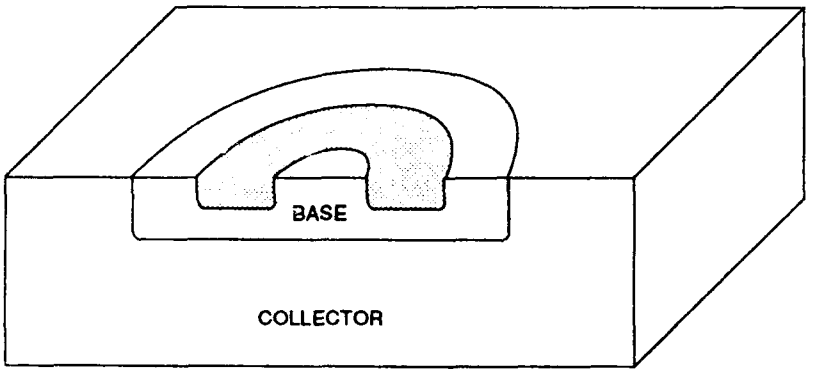


Figure 5-13. Sketch of Q_2 Cross Section Showing Positions of Base and Emitter Diffusions Relative to Collector.

When the transistor was fabricated, the n-type base diffusion was diffused into the p-type collector. In order for the base to be n-type it must have a much higher doping level than the collector diffusion into which it was diffused. The n-type dopants for the base are diffused into a portion of the collector which already contains p-type dopants. The n-type and p-type dopants tend to cancel each other at the point where the concentrations of the two dopant types are equivalent. Additional n-type dopants are added until the concentration of the n- type dopants in the base area are at least 1.5 to 2.0 orders of magnitude greater than the dopant concentration of the p-type dopants already present due to the collector doping. At this point the effects of the p-type dopants are completely overcome and the material behaves electrically as if it were n-type material.

The preceding discussion also applies to the formation of the emitter diffusion, except in this case, the p-type emitter diffusion was formed in the n-type base diffusion. As a result, the p-type emitter diffusion doping concentration is at least 1.5 to 2.0 times greater than that of the base. The doping concentration of the emitter will be very high as a result.

The doping concentration of the base diffusion can be approximated by measuring the breakdown voltage of the base-emitter junction. The breakdown voltage of the base-emitter junction was about 7.6 volts for three different samples of the transistor of interest. This corresponds to a doping level of approximately 2.5×10^{17} atoms/cc (Ref. 5-3). The emitter doping concentration will therefore be approximately 10^{19} atoms/cc.

5.7.2 Ionic (Sodium) Contamination Diffusion

When sodium ionic contamination is discussed in the technical literature, most references agree that the sodium contamination is probably introduced as an artifact during the aluminum metallization deposition process. Therefore, when it is initially introduced it can be assumed that it exists as a layer between the aluminum and the silicon dioxide passivation as indicated in Figure 5-15. There may also be some immobile sodium in the metallization and also some sodium on top of the metallization. These will be neglected for the purposes of this model.

Sodium will diffuse through silicon dioxide at a rate that is very temperature dependent. (Sodium will also diffuse through silicon nitride, an alternate passivation material, but at a rate approximately an order of magnitude slower than through silicon dioxide.) Therefore, as time goes by the sodium will diffuse into the oxide generating a distribution that can be represented as shown in Figure 5-16. The positive sodium ions will attract negative carriers in the underlying silicon. In the case of the n-type base, the additional negative carriers that are attracted to the surface will make this region more heavily doped n-type, an effect known as accumulation. In the case of the p-type emitter, the negative carriers (minority carriers in this region) that are attracted by the sodium ions will tend to make the surface region less p-type. If enough negative

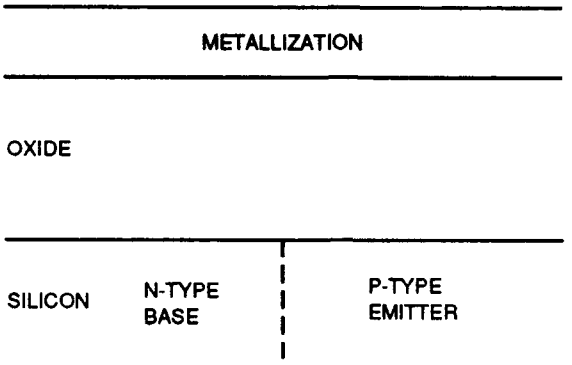


Figure 5-14. Sketch of Cross Section of Surface of Transistor Over the Base-Emitter Junction.

carriers are attracted by the ionic contamination, the surface of the p-type emitter will have more negative carriers than positive carriers and will become inverted to n-type material. The area where it becomes inverted is known as the inversion layer.

In most cases where ionic contamination in the passivating oxide is affecting the electrical behavior of a device, the contamination has inverted the silicon directly beneath the oxide. In the case of sodium or positive ionic contamination, only p-type material can be inverted. For the PNP transistor of interest, only the collector or emitter diffusions can be affected by sodium contamination. From previous discussions of the electrical behavior of the device, the emitter diffusion is the area that is being affected by the contaminant. At first, this does not seem possible since the emitter diffusion is so heavily doped

Typically, heavily doped areas are immune to being inverted since the concentration of the contaminant is not sufficient to induce enough charge in the silicon to overcome the doping in the silicon. However, for heavily doped junctions, contamination in the oxide can lead to a different type of degradation mechanism.

5.7.3 Tunneling - Failure Mechanism

During a literature search for data on the quantitative effects of ionic contamination on device electrical characteristics, a discussion of degraded gain in PNP transistors and a description of the failure mechanism were found. (Numerous other references regarding ionic contamination, sodium diffusion in oxides and the effects on semiconductor performance were reviewed. These are listed at the end of the cited references for Section 5.0.) The failure mechanism is tunneling in the base-emitter junction induced by ionic contamination in the overlying oxide (Ref. 5-2 and 5-4). The base-emitter tunneling current does not contribute to the gain of the device but does

increase the overall base current. Therefore, the gain or h_{FE} which is simply I_C/I_B (where I_C is the collector current and I_B is the base current) decreases since the collector current stays constant while the base current increases.

The failure mechanism results when the ionic contamination (sodium) inverts a portion of the p-type emitter area. Figure 5-17 represents the doping concentrations across the surface of the base-emitter junction of the transistor that was degraded by ionic contamination in the negative regulator hybrids. The n-type concentration is about 2.5×10^{17} atoms / cc in the base and becomes p-type at a concentration of about 10^{19} atoms / cc in the emitter. The transition between the two areas is depicted as a linear change (on a log scale) between these two regions. The actual transition is not important. This representation was chosen only for the purposes of the following discussion which will not be extremely dependent on the exact shape of the transition between the two regions.

Along the area of transition between the base and emitter regions, there are p-type doping levels that range from zero to 10^{19} atoms / cc. Some of these p-type levels will be subject to being inverted by ionic contamination in the overlying passivating oxide. As a result, n-type regions can be formed in the area that was formerly the transition region, resulting in very closely located highly doped p-type (represented by p+) and n-type regions. This geometry is susceptible to tunneling conduction between the two regions as opposed to the normal conduction mechanisms.

Figure 5-18 shows an energy band diagram for a p-n junction. For the n-type region, the Fermi level in the material is located nearer to the conduction band than to the valence band due to the excess number of electrons in this area. In the p-type region, the Fermi level is located nearer to the valence band due to a lack of electrons (or the presence of holes) in this area. When the p- and n-type materials are adjacent, the Fermi levels from the two materials align resulting in a potential difference between the p- and n-type regions. This potential difference is responsible for the rectifying properties of a p-n junction.

When the junction is forward biased (as illustrated in Figure 5-19), the potential difference between the p and n regions is reduced. With sufficient bias applied, the potential difference is reduced sufficiently such that current flows across the junction. With the opposite polarity applied, the junction is reverse biased and the potential difference between the two regions increases and further blocks current flow.

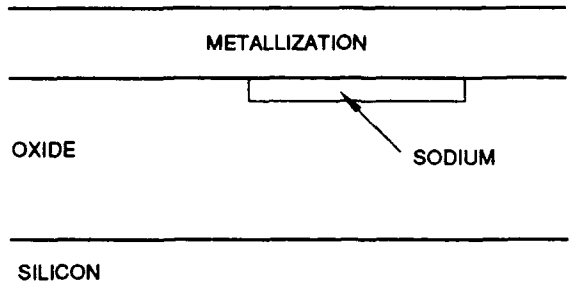


Figure 5-15. Sketch of Cross Section of Surface of Transistor Showing Initial Thin Layer of Sodium Introduced During Metallization Deposition.

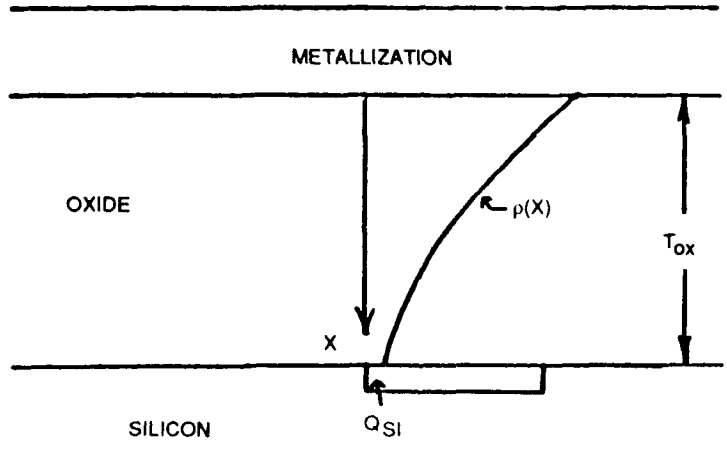


Figure 5-16. Sketch of Cross Section of Surface of Transistor After Sodium has Diffused into the Oxide. The "x" Coordinate is Distance into the Oxide from the Metallization/Oxide Interface. ρ(x) is the Amount of Sodium at Each Layer of Oxide at Distance x into the Oxide. The Sodium Distribution Induces a Charge in the Surface of the Silicon Represented by Q_{SI}. T_{OX} is the Oxide Thickness.

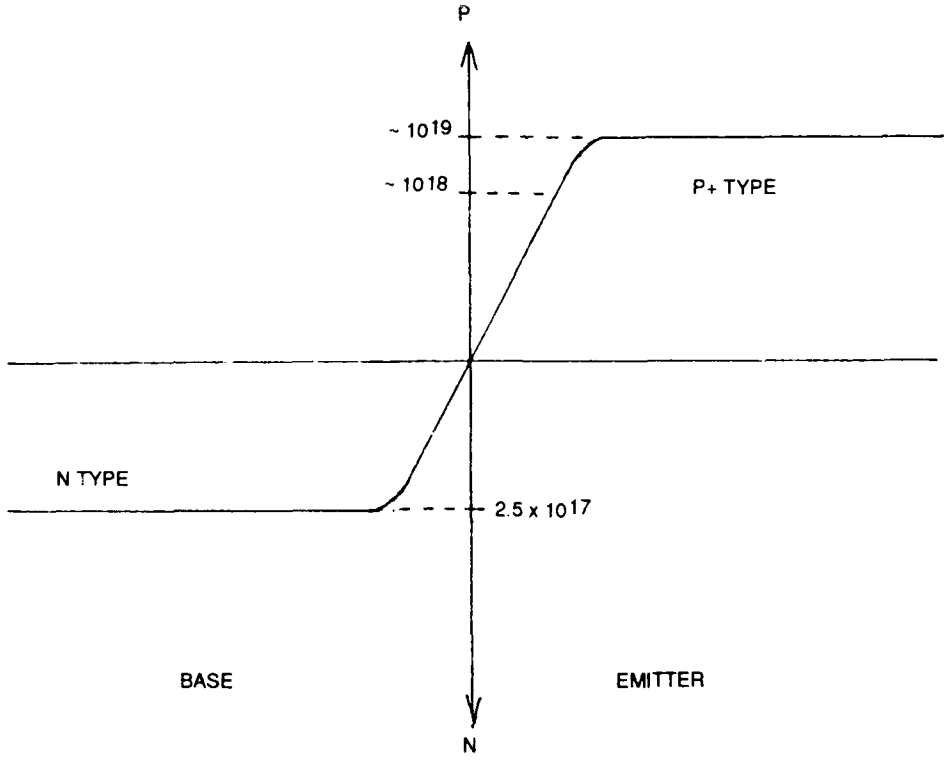


Figure 5-17. Representation of Doping Levels Across Base-Emitter Junction. Base is N-type and Emitter is P-type with Transition in Between.

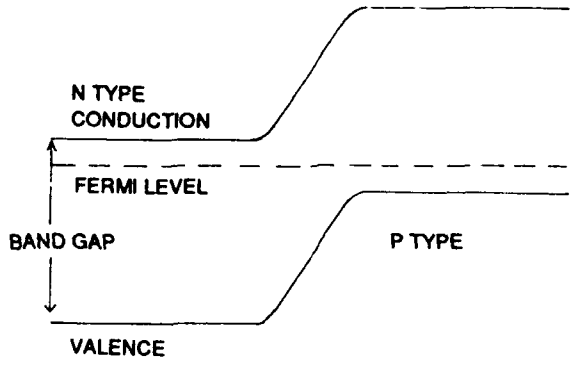


Figure 5-18. Diagram of Energy Levels in a Typical P-N Junction (Without Bias).

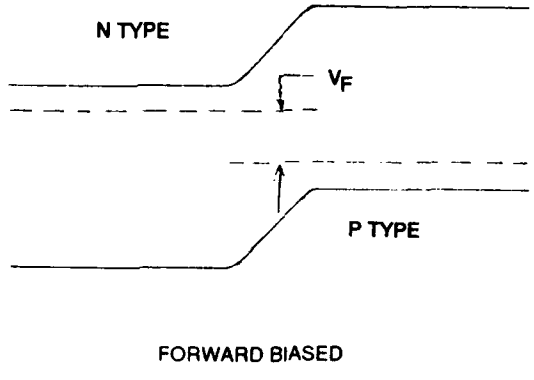


Figure 5-19. Diagram of Energy Levels in a Typical P-N Junction with Forward Bias. Energy Level Difference Between p- and n-Type Regions is Reduced by V_F, the Forward Bias Voltage.

In the case of a junction between an induced n-type region and a heavily doped p-type region, the energy band diagram can appear as shown in Figure 5-20. With the p-type region very heavily doped, the Fermi level lies within the valence band as shown. The induced n-type region is physically very close to the p-type region since it is an inverted portion of what previously was a part of the concentration gradient between normal p- and n-type regions. Under these conditions, the probability of quantum mechanical charge tunneling between the p- and n-type regions becomes significant. (Even for typical junctions there is a probability for tunneling between the two regions. However, because of the differences in the energy levels and the distances involved, this probability is extremely small. Therefore, the contribution of tunneling current to junction current under typical conditions is insignificant.)

As the amount of tunneling current increases, the base-emitter current increases with no corresponding increase in collector current in a transistor with this mechanism. Therefore, the gain of the transistor, which is defined as the collector current divided by the base current, decreases. There is no appreciable change in the reverse leakage current for a junction that is affected by this mechanism, since reverse bias increases the potential difference sufficiently that the tunneling current probability is reduced to an insignificant level.

5.7.4 Explanation for Absence of Tunneling Failure Mechanism in Positive Regulators

Positive voltage regulators, that are very similar in design to the negative regulators, were not found to fail in the field or change during the screen test. It is possible that these hybrids did contain ionic contamination in the matched transistor pair at the same levels as the matched pair in the negative regulators.

However, the matched pair in the positive regulator are NPN transistors, which are not susceptible to the failure mechanism found in the PNP matched pair in the negative regulators. NPN transistors have n-type emitters which will not be inverted by sodium (positive ion) contamination. Therefore, the tunneling failure mechanism cannot be induced in the transistors and the positive voltage regulator hybrid will not be subject to failure by this mechanism in the matched transistor pair.

5.7.5 Determination of Tunneling Current Magnitude

There are formulas for calculating the tunnel current but detailed knowledge of the base and emitter diffusions and the diffusion profiles are required. Since those data were not readily or easily available, a different approach was used for determining the tunneling current.

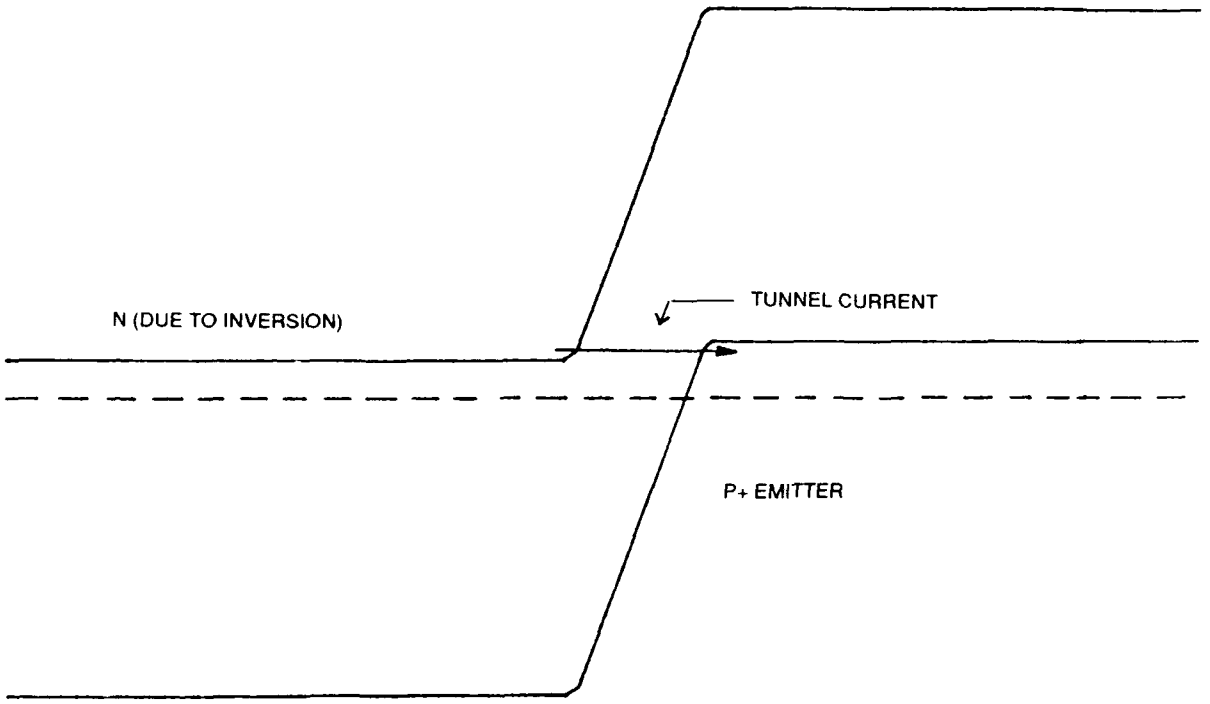


Figure 5-20. In a p-n Junction with Heavy Doping (in this Case the p-Type Material is Heavily Doped) the Fermi Level (Dotted Line) Can Lie Within the Valence Band. The n-Type Region, Formed by Inversion of a Portion of p-Region, is Very Close to the p + Region. In this Situation, the Quantum Mechanical Tunneling Probability Becomes Significant.

Ref. 5-4 is a summary of experiments on various transistor structures using an additional metallization as a gate structure to determine the effects of various contaminants on transistor parameters. The metallization was deposited over the passivating oxide above the base-emitter junction on the different transistors. Varying biases were then applied to this metallization. Since the thickness of the oxide over the base-emitter metallization was known the resulting field induced by the bias on the metallization could be determined. This induced field could then be used to simulate the fields induced by varying levels of contamination that might be in the oxide. Since the polarity on the gate metallization could be either positive or negative, the effects of either positive or negative ions could be simulated.

When the metallization was positively biased over the base-emitter of a PNP transistor, the gain of the transistor was found to decrease. This is analogous to the gain degradation that was observed on the transistors of interest from the hybrids. The article went on to explain that this was due to base-emitter tunneling current resulting from changes in the base-emitter junction induced by the field in the oxide. Other references also discuss this phenomena but do not provide as much detailed quantitative data as this reference.

Using the data from this reference, the tunneling current density vs. surface charge per unit area was calculated for the test structure. The transistor biases and nominal operating currents were also included in the data in the reference and can be chosen so that they are the same as the operating conditions for the actual transistors in the hybrid. The doping profiles for the test transistors in the reference and the actual transistor in the hybrid do not have to be known or have to be exactly the same since the failure mechanism occurs along the concentration gradient between the base and the emitter diffusions rather than at a particular concentration value. Since the diffusions in both transistors were created in similar manners, the concentration gradients would be similar enough to predict the tunneling current for the transistor from the hybrid to well within an order of magnitude, based on the data for the transistor in the reference.

Once the tunneling current has been determined for the transistor, the change in gain for the transistor can be determined. This gain change will then determine the output voltage change for the overall hybrid.

5.7.6 Hybrid Output Voltage vs. Transistor Gain Degradation

The data for the computer simulation of the hybrid circuit were used to determine the resulting output voltage for a particular value of gain for transistor Q2. The model for the ionic contamination failure was ultimately used to predict the lifetime of the hybrid under particular operating conditions. The criteria for failure was the module specification limits for the hybrid output voltage. This voltage was then used to determine the amount of gain change required for the hybrid to shift to this voltage.

5.8 MOBILE IONIC CONTAMINATION (QUANTITATIVE DISCUSSION)

The preceding section discussed the general approach for the ionic contamination model. This section provides a detailed discussion of the model with quantitative data produced by the model. The model was coded in Tasks VII and VIII, and the software was delivered to the Air Force.

5.8.1 Overall Approach

Figure 5-21 is a flow chart representing the overall model for the ionic contamination mechanism. The sodium ion diffusion model predicted the diffusion profile of sodium ions in the oxide of the transistor vs. time. Also, this model was used to calculate the resulting charge vs. time induced in the underlying silicon. The charge induced in the silicon was then input into the data from the reference on tunneling currents to predict the amount of tunneling current which was then translated into change of gain vs. time. The maximum allowable change in gain was obtained from the computer simulation of the hybrid circuit.

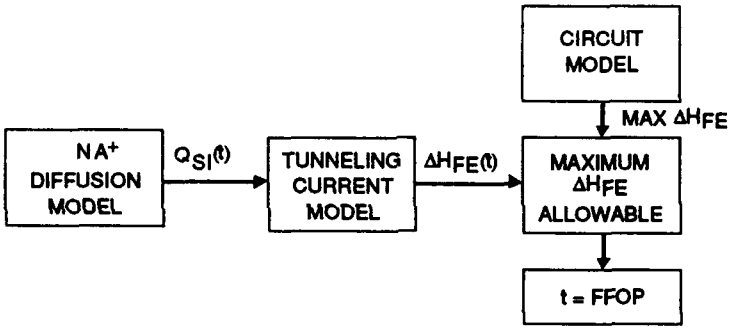


Figure 5-21. Flow Chart for Ionic Contamination Induced Inversion Model.

By observing the change in gain vs. time, the point at which the maximum allowable gain change is reached can be determined. This point corresponds to the predicted time that the hybrid will operate without failure. This time is referred to as the FFOP (Failure Free Operating Period) of the hybrid.

5.8.2 Sodium Ion Diffusion Model

Referring back to Figures 5-15 and 5-16, $\rho(x)$ represents the distribution of sodium ions in the oxide throughout its total thickness T_{OX}. Each point, $\rho(x)$, represents the charge in a layer of oxide x distance away from the metallization. The function $\rho(x)$ was calculated using standard diffusion formulas.

For an initially limited source, that is, where the source of the diffusing element is finite (Ref. 5-3):

$$C(x, t) = \frac{S}{\sqrt{\pi Dt}} \; e^{\frac{-x^2}{4Dt}} \tag{5-1}$$

where:

$C(x,t)$ = concentration of element at point x at time t

S = initial surface concentration of diffusing element

D = diffusion coefficient of diffusing element.

There would be very little difficulty in programming this equation and providing the distribution of sodium ions at any point in time. However, there are two complications that make this problem much more difficult:

(1) The above equation is for an infinitely thick medium

(2) D is dependent on temperature according to the following formula:

$$D = D_0 \exp(-E_A/KT) \tag{5-2}$$

where:

D_0 = diffusion constant at known temperature

E_A = activation energy

K = Boltzmann's constant

T = absolute temperature

These complications to the problem are solvable. The equations and model for solid diffusion are similar to heat conduction problems that have already been solved. Basically, the approach is to calculate distributions for a time and constant temperature interval and then use this as the initial point for the next interval. The initial value of the sodium ion surface concentration, S, was estimated to be on the order of 1 x 10 exp 14 atoms/cm^2 based on data from the technical literature. Of course, the actual value for this specific transistor could be orders of magnitude different from this "typical" value from the literature.

Values of E_A and D were also obtained from the literature (Refs.5-5 through 5-8). The value used for E_A was 1.4 eV and D was 2.16 x 10^{-16} cm^2/sec at 125 C.

5.8.3 Charge Induced in the Silicon

Once a distribution of sodium ions has been determined for a particular time, the charge induced on the underlying silicon can be calculated using the following formulas:

$$Q_M = \int_o^{T_{ox}} \frac{x}{T_{ox}} \rho(x)\, dx \tag{5-3}$$

$$Q_{SI} = \int_o^{T_{ox}} \frac{T_{ox}-x}{T_{ox}} \rho(x)\, dx \tag{5-4}$$

where:

Q_M = charge induced on the metallization by the sodium

Q_{SI} = charge induced in the silicon by the sodium

T_{ox} = total oxide thickness

The oxide thickness was initially estimated to be 1 micron. This value was later verified by actually cross-sectioning one of the transistor chips and measuring the oxide thickness. The measured thickness was 1.0 micron.

A computer model was developed for determining the charge induced in the silicon by a sodium ion distribution at a particular time. The amount of surface charge was determined up to a point where a "critical level" of surface charge was obtained. The "critical level" is defined as the point where sufficient charge has accumulated to degrade transistor gain sufficiently that hybrid output is outside of specification limits.

The initial calculations were simply an integration of the form

$$K_1 X \exp(-X^2 K_2) \tag{5-5}$$

If a critical level of surface charge had not been reached by the time some of the sodium ions had reached the silicon surface (the finite thickness condition), then the sodium ion distribution would have had to be numerically integrated. Numerical integration also has to be used if distributions have to be calculated for time intervals at different temperatures.

Using the quantitative data from the previously mentioned reference, it was determined that a surface charge of about 7.5×10^{-12} charges / cm^2 would correspond to the "critical level" of surface charge. With this amount of surface charge induced in the transistor, the gain of transistor Q2 would decrease to the point where hybrid output voltage would increase to the maximum module specification limit of -12.25 volts.

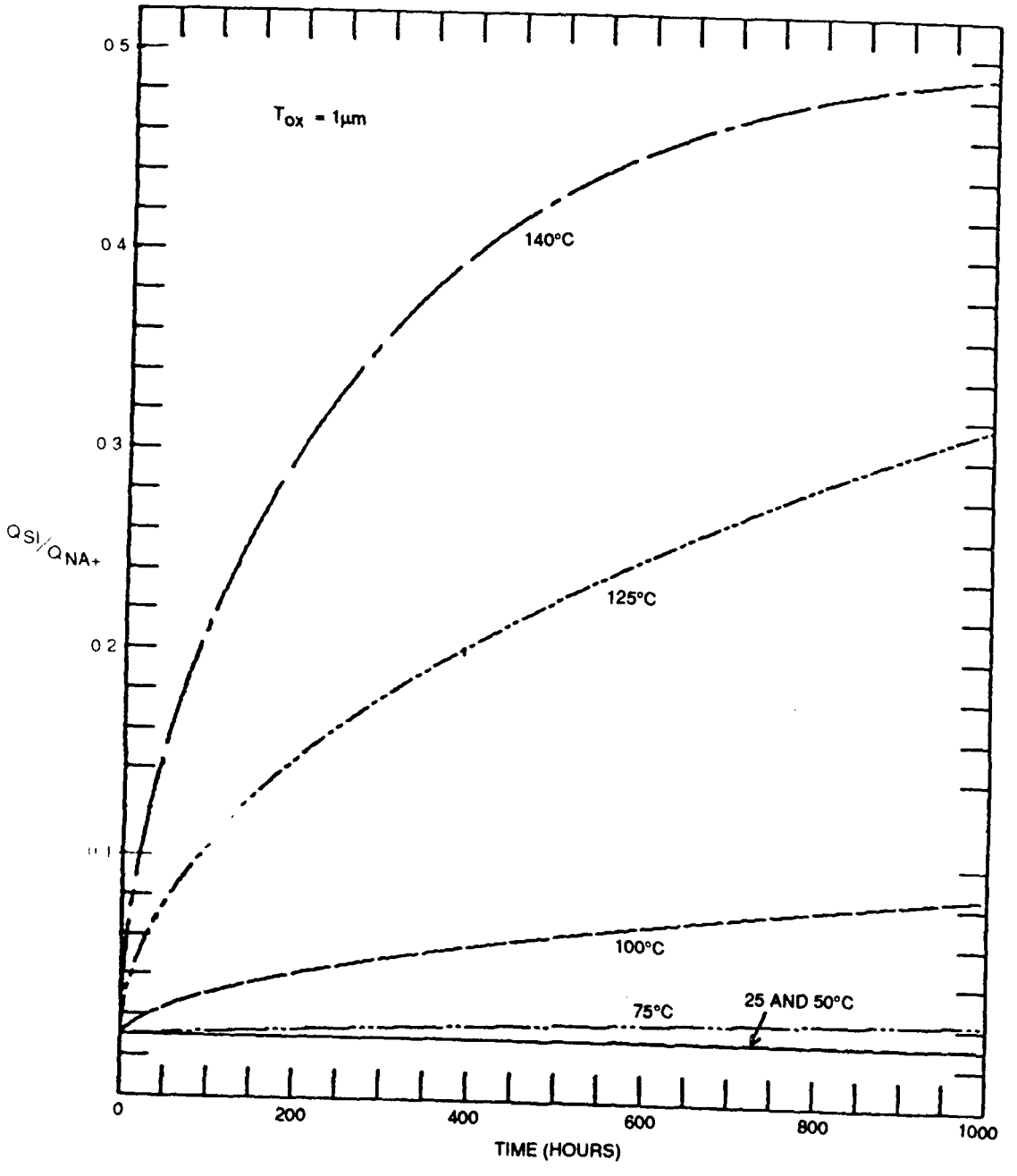
Figure 5-22 shows the initial outputs of the computer model. The graph produced by the computer shows the charge induced in the silicon (Q_{SI}) normalized to the initial sodium ion concentration (Q_{Na+}) vs. time for various temperatures. By normalizing the induced charge to the initial sodium ion charge, assumptions regarding the amount of initial sodium charge were neglected at this point. It can be seen that, at temperatures of 100 C or less, it will take thousands of hours to reach an induced silicon charge equivalent to only 10% of the initial sodium charge. For a temperature of 125 C, this time is reduced to only about 80 hours. However, in these examples the transistor could further degrade to a much larger extent if subjected to additional temperature since the sodium ions have not reached an equilibrium distribution where $Q_{SI}/Q_{Na+} = 0.5$.

If the sodium were allowed to diffuse for an infinite amount of time, the final distribution would be an even distribution of sodium throughout the thickness of the oxide. Under these conditions, the charge induced in the silicon would be equivalent to one-half of the total number of sodium ions that were initially introduced in the oxide. This amount of surface charge corresponds to having all of the sodium ions distributed halfway between the metallization and the silicon, at $x = T_{ox}/2$.

However, the contamination screen that was applied to the hybrids resulted in large voltage shifts in the hybrids in only 48 hours (see Section 5.4). One hybrid output voltage even shifted beyond the specification limit allowed by the module specification.

Even more significant is the fact that the hybrids did not degrade any more when subjected to additional high temperature testing. It was as if they had already reached an equilibrium distribution of sodium ions after only 48 hours (or sooner, since no data were taken at any intervals between the initial value and the first end point value at 48 hours).

The previous calculations and computer model assumed that the transistors were biased as they normally are in the hybrid. That is, the base-emitter junction is forward biased with only about 0.5 to 0.6 volt across the junction. However, in the HTRB step of the hybrid contamination screen, the base-emitter junction of the transistors is reverse biased with 5 volts across the junction. Since the base metallization crosses over the junction, there was a field of 5 volts across this oxide. The HTRB base bias of +5 volts with respect to the emitter tended to drive the sodium ions away from this metallization toward the junction, especially toward the emitter. This field that resulted from the HTRB test apparently had a large effect on the sodium ions.



Q_{SI} (CHARGE INDUCED IN SILICON) NORMALIZED TO Q_{Na+} (INITIAL SODIUM CONCENTRATION) VERSUS TIME FOR VARIOUS TEMPERATURES OXIDE THICKNESS (T_{ox}) IS 1 MICRON.

Figure 5-22. Output from Computer Model of Sodium Diffusion (for Normal Bias).

5.8.4 Modification of Model to Include Reverse Bias

It was decided to modify the computer model to include the field induced across the oxide by the reverse bias. (The lateral field induced across the base-emitter junction was neglected to make the geometry of the problem simpler.)

There were two approaches that were considered for including the reverse bias in the model. The first was to directly solve Fick's second law modified to include the reverse bias. The following equation (Ref. 5-9) shows this modification:

$$\frac{\partial C}{\partial t} = D\frac{\partial^2 C}{\partial x^2} - v\frac{\partial C}{\partial x} \tag{5-6}$$

In this equation, we have (Refs. 5-3 and 5-10)

$$v = \mu E = \mu\left(\frac{\text{REVERSE BIAS VOLTAGE}}{\text{OXIDE THICKNESS}}\right) \tag{5-7}$$

$$\mu = \frac{eD}{kT} \tag{5-8}$$

where:

v = velocity of the diffusing ions

μ = mobility of the diffusing ions

E = electric field across the oxide.

This approach would have been very difficult even using a computer model, especially when the effects of varying the temperature and the finite medium are taken into account.

The second approach that was evaluated, and ultimately used, was to use a mathematical device to solve the problem. First, a mathematical substitution known as Smolukhovskii's substitution (Ref. 5-10) was used:

$$C = e^{\frac{vx}{2D} - \frac{v^2 t}{4D}} C^* \tag{5-9}$$

Then Fick's second law was solved based on this new variable:

$$\frac{\partial C^*}{\partial t} = D\frac{\partial^2 C^*}{\partial x^2} \tag{5-10}$$

This was then modelled on the computer and new curves of sodium distribution vs. time were calculated for 125 C.

Figure 5-23 shows these curves for the reverse biased case and for the unbiased (or normal bias) case. It can be seen that the reverse bias greatly accelerates the diffusion of the sodium ions. The sodium ion distribution achieves an effect equivalent to an equilibrium distribution ($Q_{SI} = Q_{Na+}/2$) in only 34 hours under HTRB conditions. In comparison, Figure 5-22 shows that unbiased diffusion will require more than 1000 hours to have this same effect.

The reverse bias curve explains another detail that was seen during the HTRB performed in the hybrid contamination screen. For periods of HTRB greater than 34 hours, the sodium contamination will be driven beyond an equilibrium distribution. That is, the "average position" for the sodium ions will be closer to the silicon than that for the equilibrium condition.

The HTRB in the screen was performed for 48 hours. Examination of the data for the negative regulators presented in Figure 5-6 shows that the devices with the largest output voltage shifts did recover slightly when they were baked without reverse bias. This would be a result of the sodium ions "back-diffusing" from th distribution resulting from the HTRB. As the distribution approaches the equilibrium condition, the transistors recover slightly since the "average position" of the ions is now farther away from the silicon.

5.9 MODEL OF SURFACE CONTAMINATION MECHANISM

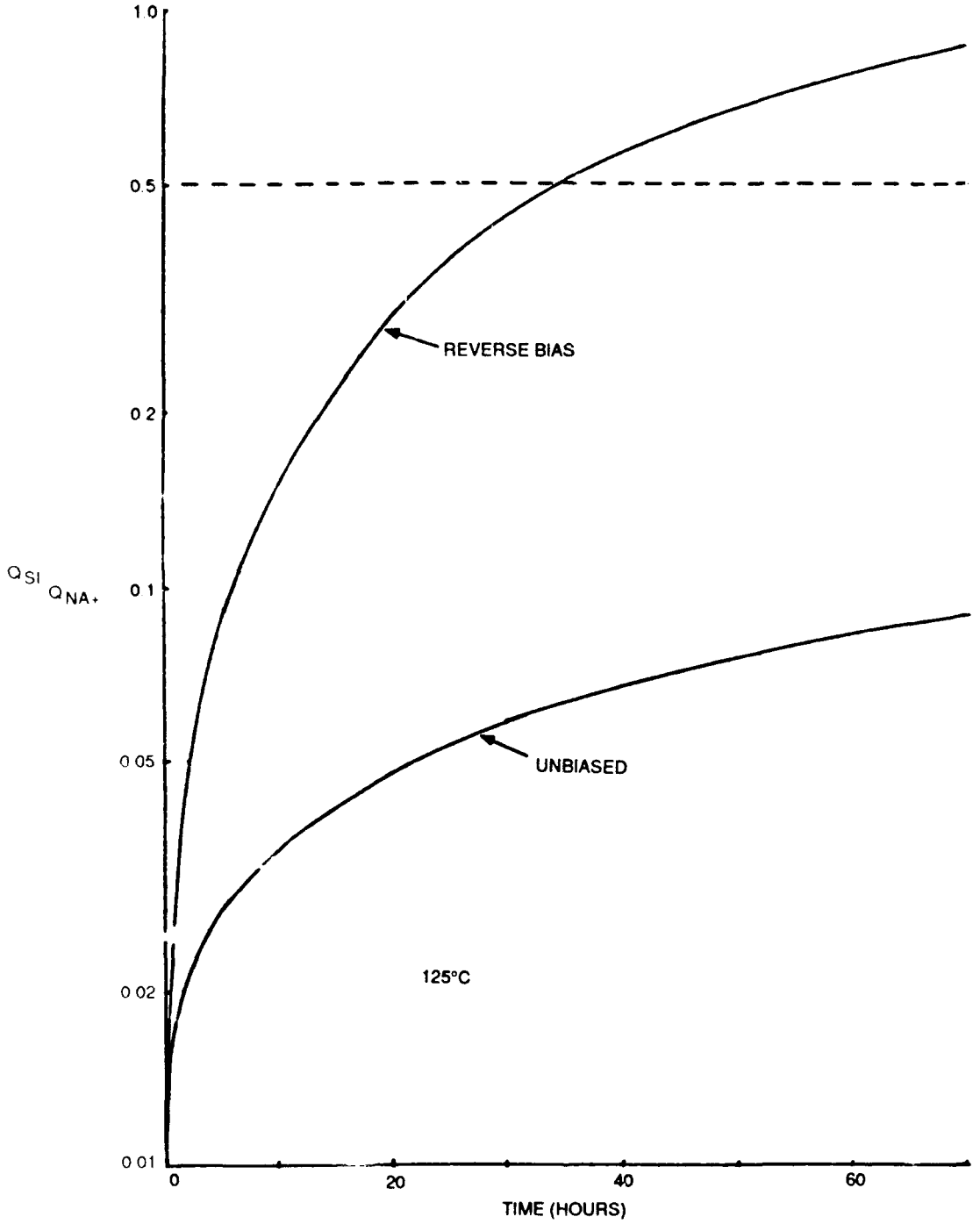
It has been shown that surface contamination caused the output voltage of some of the fielded negative regulator hybrids built in 1981 and 1982 t change. The failure mechanism was found to be occurring on a thick film resistor. Apparently, the surface contamination bridged a laser trim on the resistor causing the resistance to decrease.

Unlike the ionic contamination failure mechanism, very little data or information regarding the exact contaminant or behavior of the contaminant was available for the surface contamination mechanism. After the effects of the mechanism had been documented, an unbiased bake of the hybrids exhibiting the mechanism caused the hybrids to return to a normal operating condition. The failure could not be repeated or induced again by additional tests. Apparently, the bake caused the contamination that was initially causing the failure to disperse within the hybrid.

Additional analyses on the resistor after the hybrids had been opened did not reveal any additional information regarding the exact nature of the failure mechanism or the contaminant causing the failure.

This failure had some similarities to the ionic contamination failure mechanism. The hybrids failed only after having functioned for a period of time in the field. The failure mechanism was reversed by subjecting the hybrids to an unbiased bake.

The main difference was that the surface contamination failure mechanism could not be re-induced by additional operation of the hybrid. This difference was assumed to be due to the nature of the contamination. In the case of the ionic contamination failure mechanism, the



Q_{SI} (CHARGE INDUCED IN SILICON) NORMALIZED TO Q_{Na^+} (INITIAL SODIUM ION CONCENTRATION) VERSUS TIME FOR NORMAL AND REVERSE BIASES AT 125°C.

Figure 5-23. Plot of Data from Computer Models for Sodium Ion Diffusion for Reverse Bias and Unbiased (Normal Bias).

contamination is most likely sodium that is trapped in the oxide on the transistor. The bake only tends to redistribute the sodium within the oxide to decrease its effect on the underlying silicon. In the case of the surface contamination, the bake apparently dispersed the contaminant throughout the hybrid. There would not be a large tendency for this contaminant to return to the resistor to recreate the failure.

5.9.1 Details of the Surface Contamination Failure Mechanism

As noted previously, there was not a lot of data or information regarding the surface contamination failure mechanism. However, some details of the mechanism can be hypothesized based on the known behavior of the hybrid and the individual resistor that was affected.

The contamination that caused the failure was probably in place on the resistor when the hybrid was sealed. There are no unusual biases on this resistor that would tend to preferentially attract a contaminant that was generally dispersed in the hybrid. Also, there were two hybrids that exhibited virtually the same behavior on the same resistor. Both of the hybrids passed their initial electrical tests and then functioned in the field without failure for several years.

Because of the above reasoning, the surface contamination failure mechanism was proposed to be modelled in a manner very similar to the ionic contamination failure mechanism. It was hypothesized that a contaminant was present on the surface of the resistor at the time the hybrid was sealed. As time went by, the contaminant diffused through the passivation that forms on the surface of the resistor.

The resistor consists of a metal oxide suspended in a glassy matrix. When the resistor is deposited, it tends to self-passivate, forming a glassy oxide on the surface. When the resistor is trimmed to value, a laser cut is made in the resistor as illustrated in Figure 5-2. This laser cut is made in a regular atmosphere and also forms a self-passivating layer along the edges of the laser cut. Apparently, the contaminant is diffusing through the passivation over the edges of the laser cut and causes the resistor to decrease in value over a period of time. When the hybrid was baked, the contaminant was dispersed sufficiently that the failure mechanism could not be re-induced.

5.9.2 Model for Surface Contamination

Figure 5-24 is a flow chart of the proposed model for the surface contamination failure mechanism. (It can be seen that it is very similar to the ionic contamination model flow chart shown in Figure 5-21.) A diffusion model determines the amount of contaminant that diffuses through the surface oxide on the resistor vs. time. This contaminant acts as a conductor across the resistor laser cut forming a parasitic current path which decreases the effective resistance of the resistor.

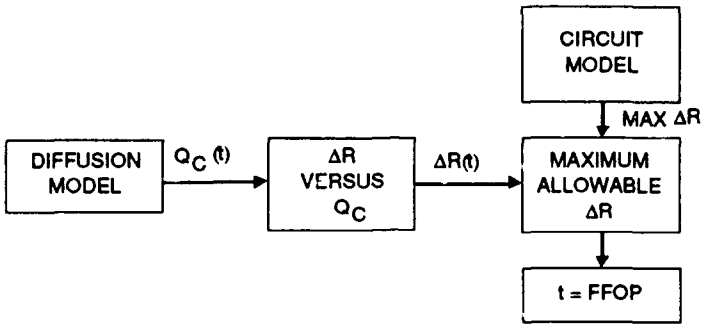


Figure 5-24. Flow Chart for Surface Contamination Failure Mechanism Model.

The amount of conducting contaminant, $Q_C(t)$, determined from the diffusion model is then converted into a resistance which is also dependent on time. The parasitic resistance and the original thick film resistor can be merged to determine the value of the overall resistance change versus time, $\Delta R(t)$.

As in the case of the ionic contamination model, the computer simulation of the hybrid circuit could be used to determine the maximum resistor change, MAX ΔR, that could be tolerated with the output of the hybrid remaining within the specification limits of the module. Using the change in resistance vs. time data generated by the rest of the model, the time at which the maximum allowable resistor change occurs can be determined. This time is referred to as the FFOP of the hybrid.

The equations for calculating the diffusion of the contaminants through the passivation on the resistor are going to be similar to those used for the ionic contamination diffusing through the silicon dioxide on the transistor. Unfortunately there are too many unknowns for the surface contamination failure mechanism to proceed any farther than the outline of the model. For example, the contaminant causing the problem was not identified. Therefore, the diffusion constants, probable amounts of initial contaminant and activation energy are unknown. Also, since the contaminant was not identified, the amount of parasitic resistance that is generated for a given amount of contaminant cannot be calculated.

A factor in this resistor which would complicate the formation of a computer model is the surface passivation. The composition and thickness of the resistor passivation would not be uniform as in the carefully grown oxide which is present on the transistor modelled previously. This could possibly be solved by the use of an "average" thickness and composition based on careful analyses of the actual resistors in the hybrids. However, this could result in large errors when comparing to a thick film resistor in an unknown hybrid.

A second factor which would tend to complicate the models is the fact that the laser trim cut would have different dimensions, especially length, from hybrid to hybrid. Careful photodocumentation of the resistors prior to sealing the hybrid could possibly provide a solution to this problem. However, in the case of the hybrids that were to be used in the CERT, this information was not available.

5.9.3 Additional Data from Hybrid Screen

The lack of a quantitative model for the surface contamination mechanism probably will not impact the determination of an FFOP for the hybrids that were placed in the CERT described in Section 6.0. The data from the hybrid contamination screen indicated no evidence of the surface contamination mechanism on the resistor between hybrid pins 21 and 24 in any of the positive or negative regulators. The largest change in percent seen in this resistor for the negative regulators was +0.04% and for the positive regulators was +0.21%.

The resistor between hybrid pins 21 and 24 is the resistor that was affected by the surface contamination failure mechanism in the hybrids from the field. The field failures exhibited changes of -8.0% and -16.0% for this resistor.

Some of the other resistors in the hybrids exhibited slightly higher percent changes in resistance during the hybrid screen. However, all of these larger percentages were associated either with resistors whose stability does not impact the output voltage or the larger percentages were associated with data measurement limitations.

In summary, the hybrid contamination screen revealed no definitive evidence that the surface contamination failure mechanism was affecting the resistors in the hybrids that were to be used for the CERT. Therefore, this failure mechanism will not be a limiting factor for the FFOP of these hybrids.

6.0 COMBINED ENVIRONMENTS RELIABILITY TEST (CERT)

This test is summarized in Ref. 6-1.

6.1 SUMMARY

The four modules, specially fabricated/inspected as described in Sections 4.0 and 5.0, were subjected to a thermal/power cycling reliability test. The modules underwent nearly 500 thermal cycles, between ambient temperature and temperatures much higher than in normal flight, without failure. This section describes the following:

- test setup
- special test equipment
- evaluation of indications of failure
- nondestructive inspection of the modules
- results.

6.2 APPROACH

6.2.1 Plan

The test plan is included here as Appendix R. The following appendices in the plan have been deleted from this report:

a. Photographs of digital module (already in Figure 2-1)

b. Photographs of analog module (already in Figure 2-2)

c. Protection of static sensitive devices (deleted for brevity; standard Hughes procedures were used)

d. Test specification for digital module (deleted for clarity because major modifications were made for the EFRM CERT)

The companion life cycle environmental profile plan is included as Appendix S. The life cycle environmental profile was developed with the aid of the following analyses:

- Failure Free Operating Period (FFOP) prediction for the test specimens, which is documented in Appendix T.
- Prediction of sensitivity of FFOP to CERT temperature range (Appendix U).
- Transient thermal analyses of modules (Appendices V and W).

6.2.2 Subsequent Modifications

The following modifications to the plan were made as a result of subsequent developments:

- The test station was modified and upgraded, as described in Section 6.5.

- Additional alarms and automatic shutdown provisions were implemented, as described in Section 6.5
- Periodic inspection of the modules using holographic interferometry (HI) was concluded to be too expensive and technically risky, and therefore was not used (see Section 6.6).
- The descope required by the reduction in the total amount of the contract (see page 1-3) resulted in the deletion of the following:
  - the final 600 of the planned 1,100 CERT thermal cycles
  - the vibration test, described in Section 5.4 of Appendix S, planned for modules surviving the CERT.
  - the post-CERT inspection using HI.

6.3 ENVIRONMENTAL STRESSES

As described in Appendix S, the environmental stresses in the CERT were selected on the basis of:

- failure analysis of failed modules of these part numbers from the field, which indicated that vibration is not a significant contributor to failures of these modules (see Section 3.0).
- a prediction (Appendix T) that the plated through holes (PTHs) in the PWBs have the shortest failure free operating period (FFOP) of any element in the modules.

Accordingly, the modules were thermal cycled between ambient temperature and temperatures much higher than in normal flight.

Thus the CERT consisted of the following combined environmental stresses:

- temperature cycling
- power cycling.

This enabled a much simpler test setup than would have been possible with vibration combined with the other environmental stresses.

With the aid of the FFOP prediction in Appendix U, the duration of the CERT was planned for 1,100 cycles. However, budget limitations forced the CERT to be terminated after just under 500 cycles. As described in Section 6.7, none of the four test specimens failed or showed any sign of aging.

6.4 TEST SETUP

The test setup is shown schematically in Figure 6-1 and in photographs in Figures 6-2 through 6-6. Its key features are as follows:

- A simple test fixture (shown in Figures 6-2, 6-3, 6-5, and 6-6) was used. An environmental chamber was not required. The modules were simply covered with

(Text continued on page 6-9.)

ERFM TR#10871

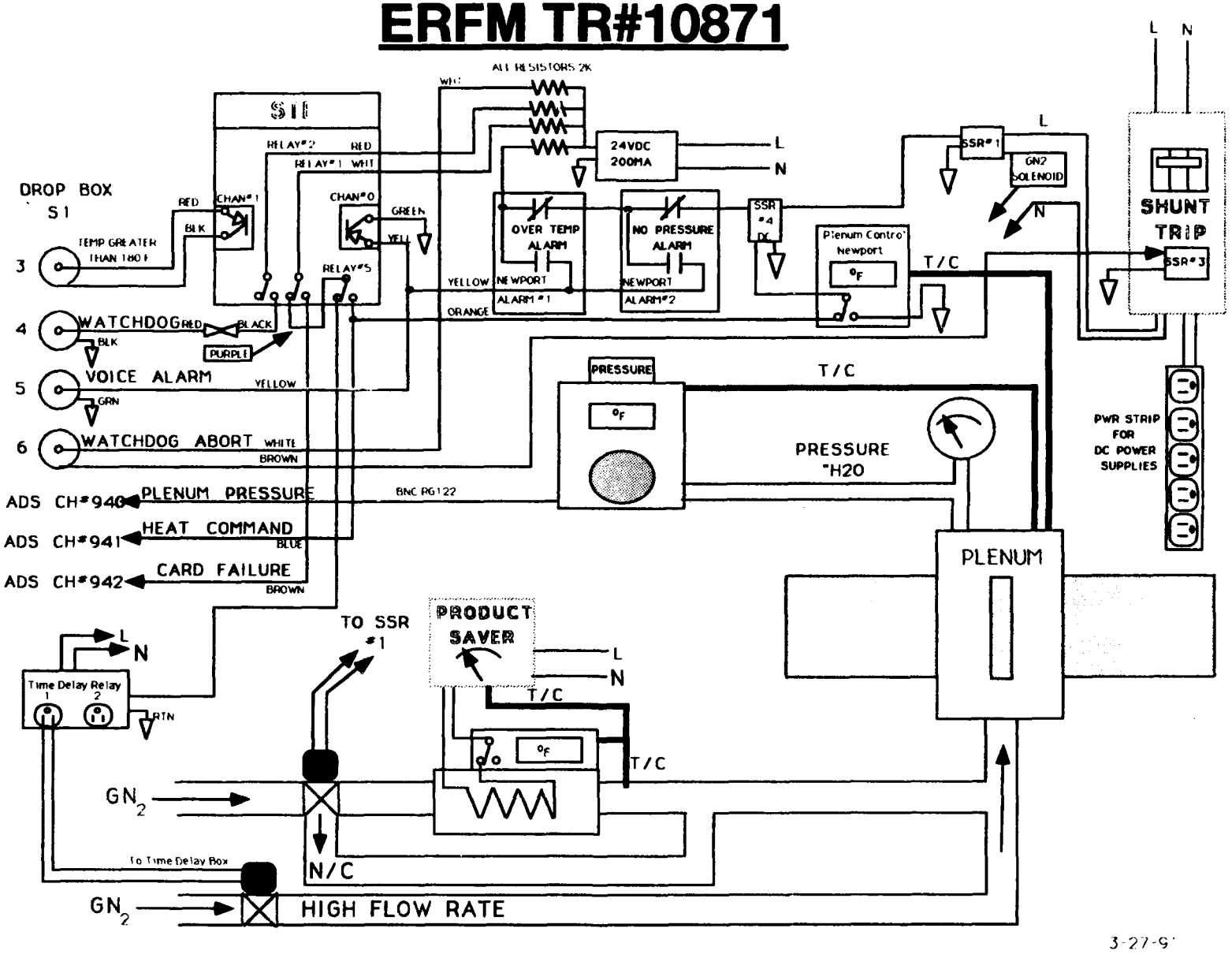


Figure 6-1. Combined Environments Reliability Test (CERT) —Test Setup Schematic

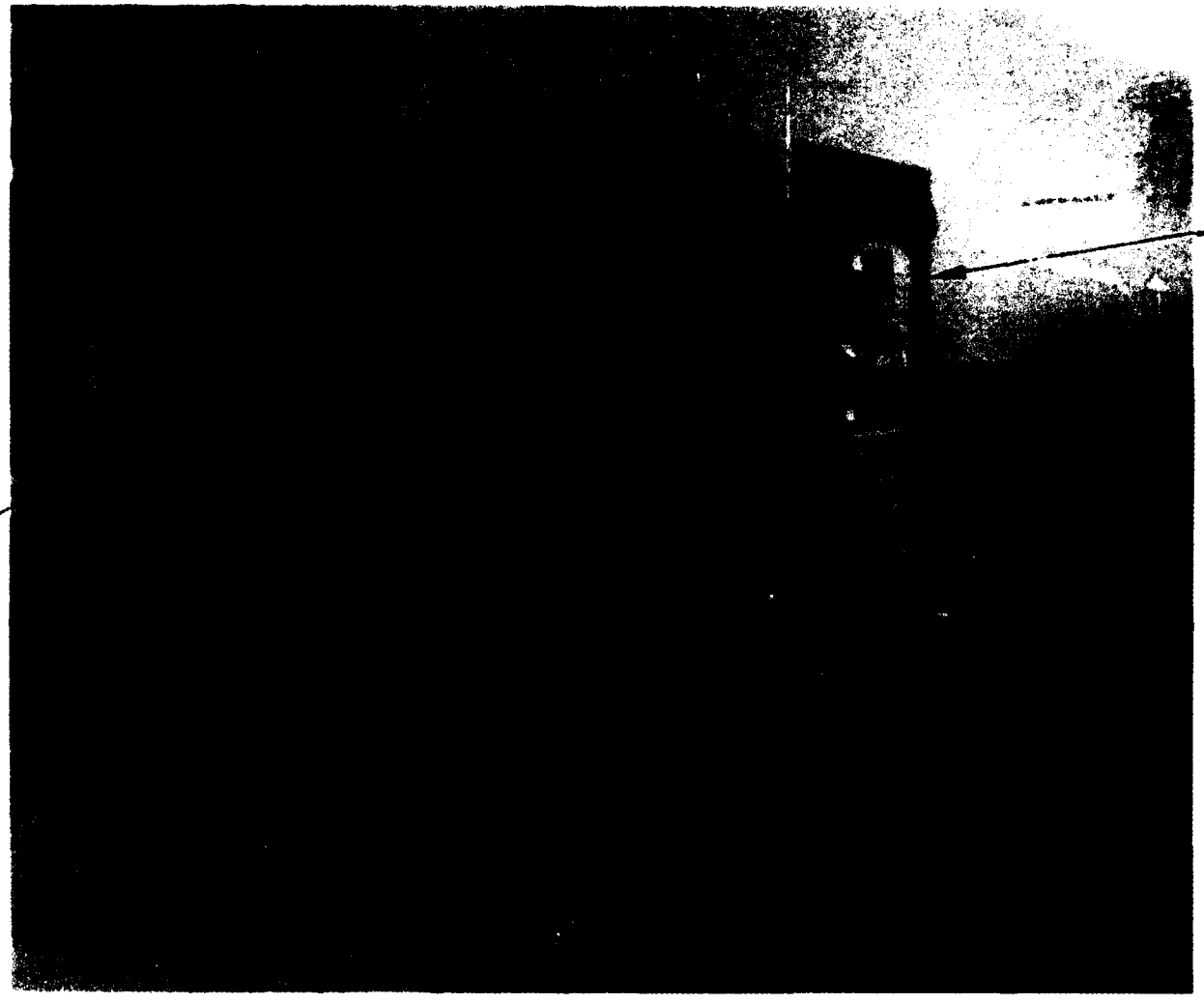


Figure 6-2. Test Fixture and Test Station

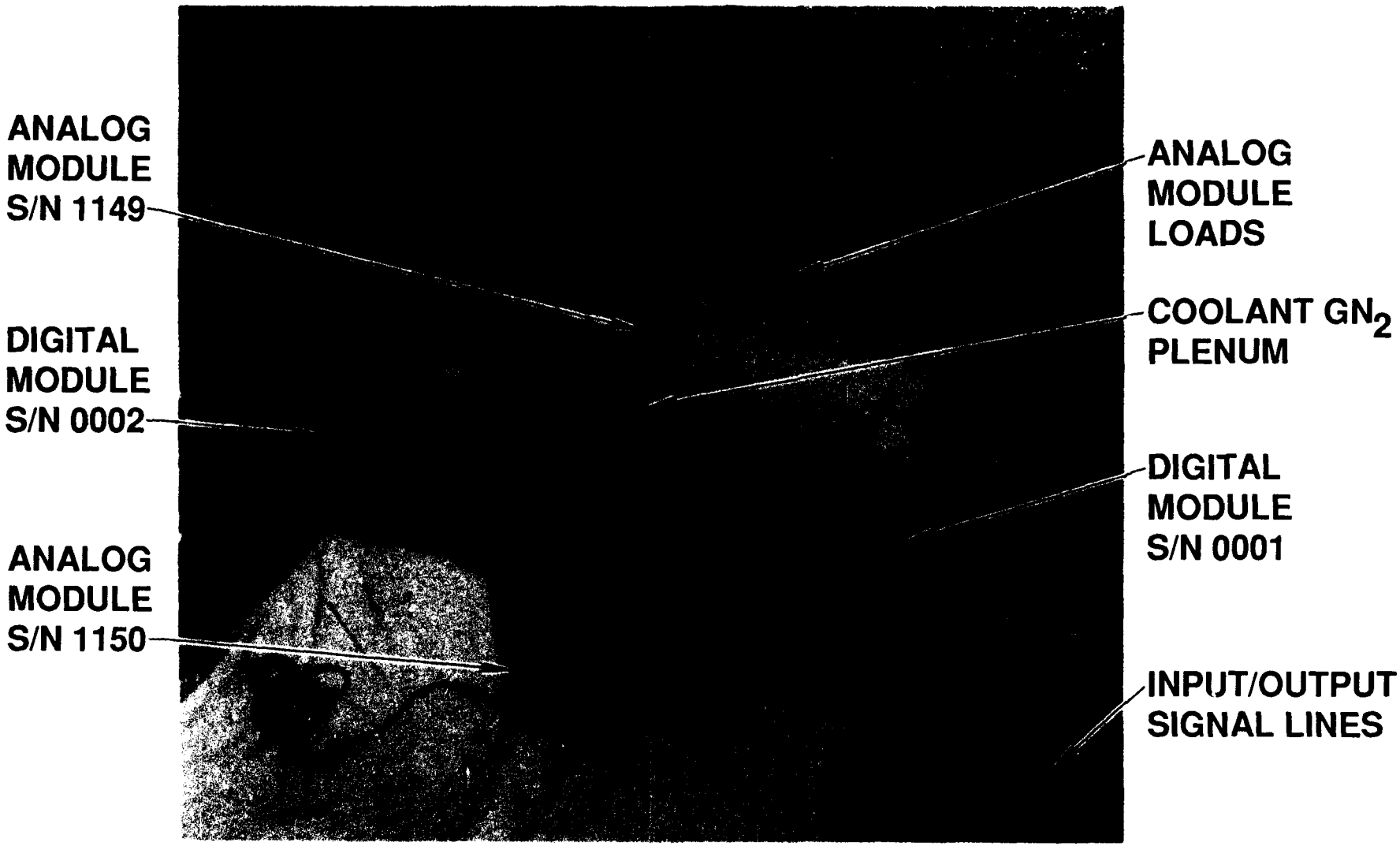


Figure 6-3. Test Fixture

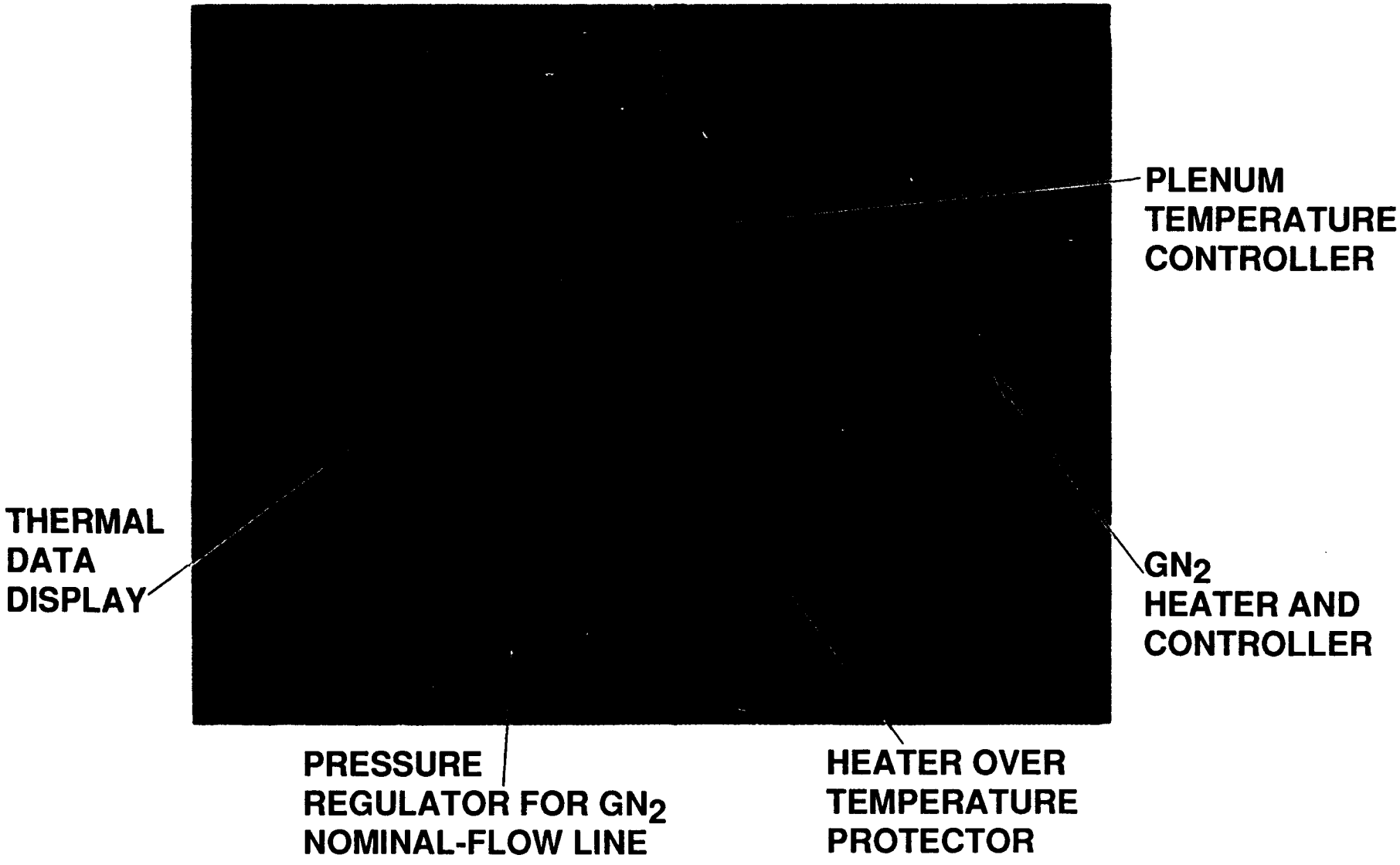


Figure 6-4. Coolant GN_2 Heater and Controllers

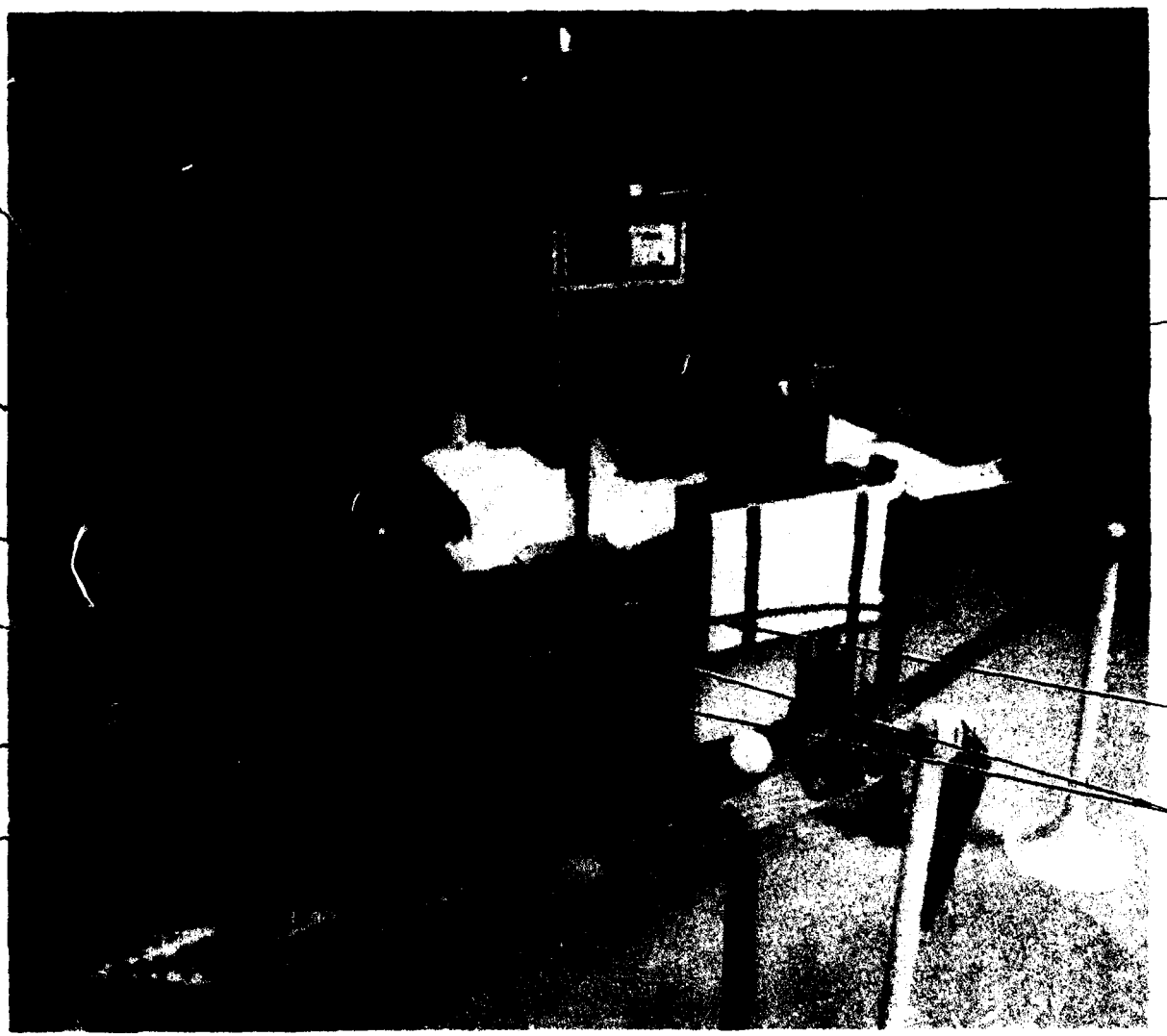


Figure 6-5. Coolant GN_2 Flow Controllers

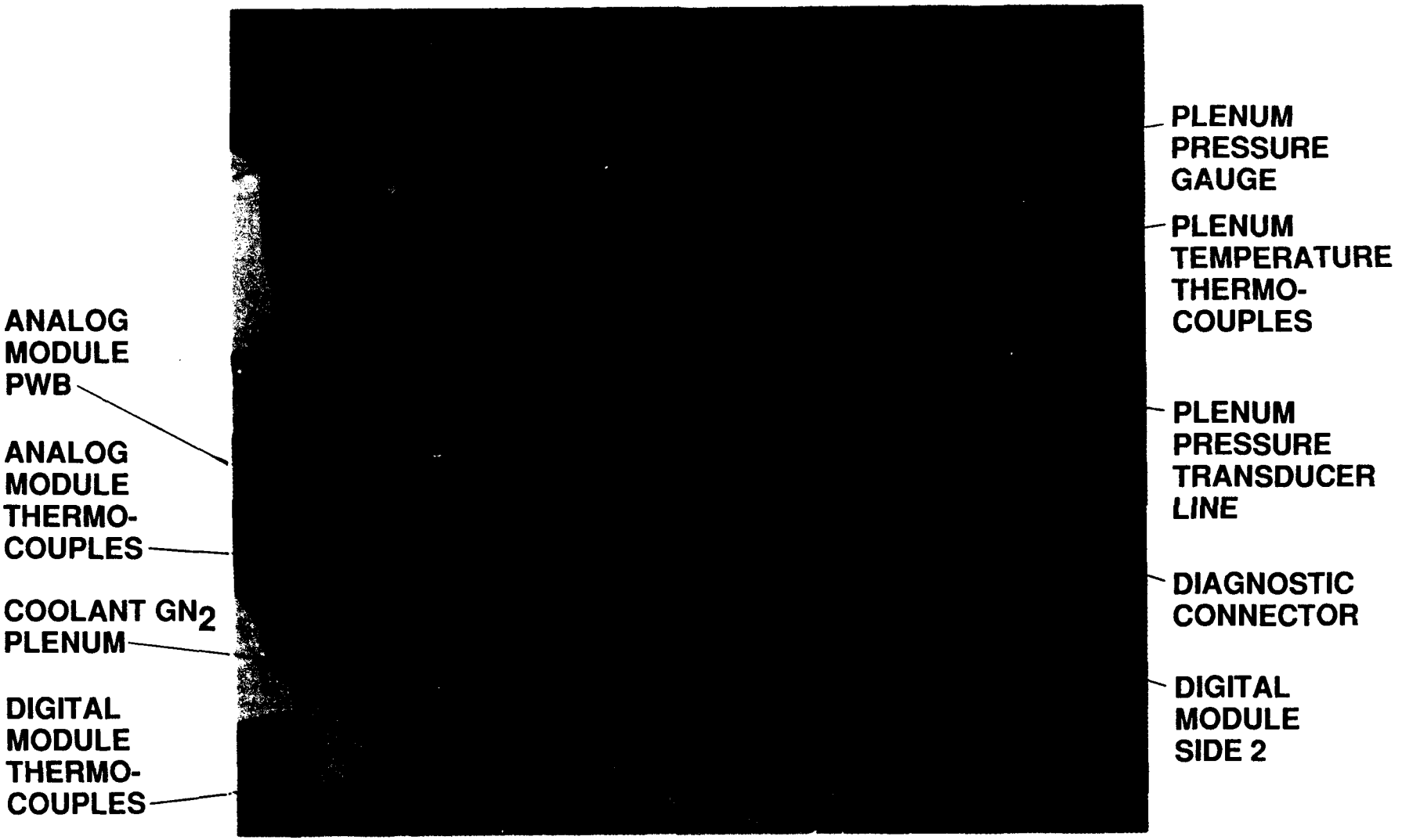


Figure 6-6. Shop Replaceable Units (SRUs) and Instrumentation

insulation, as shown in Figures 6-2, 6-3, and 6-5. The insulation materials were 1-inch-thick black foam polyurethane and 1/4-inch-thick white Fiberfrax (an asbestos replacement). Thermal surveys, described below, verified the effectiveness of the insulation.

- The thermal cycling was accomplished by cycling the module coolant inlet temperature and by on-off power cycling.
- The modules, which are forced-air cooled in flight, were cooled with gaseous nitrogen (GN2) supplied by a common plenum, as shown in Figures 6-1, 6-3, 6-5, and 6-6. Thus each of the four modules had the same coolant inlet temperature profile.
- The modules were oriented vertically (see Figures 6-2, 6-3, 6-5, and 6-6) so that they could be viewed periodically for signs of aging. They were covered with quickly removable insulation for this purpose. (Figures 6-2, 6-3, and 6-5 show the insulation on. Figure 6-6 shows the insulation off.)
- The hot part of the thermal cycle was accomplished by operating the modules with the same coolant flow rate as in flight but a coolant inlet temperature 30 C higher than nominal. The test specimen part temperatures were controlled by varying the coolant plenum temperature. The maximum plenum temperature required to produced the desired maximum test specimen temperatures was established empirically by thermal surveys, aided by steady-state thermal analyses of the modules (Appendices F and G). The thermocouple measurements were checked by comparison with the predictions of the thermal analyses, as described in Appendix X.
- The modules were cooled to ambient temperature by:
  - turning off their power
  - decreasing the coolant inlet temperature to ambient
  - increasing the coolant flow rate by a factor of about 3.5 (see Figures 6-1, 6-4, 6-5).

This succeeded in achieving a 2-hour cycle without the need for refrigeration, as verified by the thermal survey results shown in Figure 6-7. (The effectiveness of the insulation is shown in Figure 6-7 by the rapid temperature decrease when the insulation is removed.) The plenum temperature profile was established by the transient thermal analyses of the modules (Appendices V and W) and verified by thermal surveys.

6.5 SPECIAL TEST EQUIPMENT

6.5.1 Test Station Function and Operation

A custom test station, to power and monitor the modules, was designed and assembled (see Figure 6-2). This special test equipment (STE) performed the complete manufacturing functional tests on the modules.

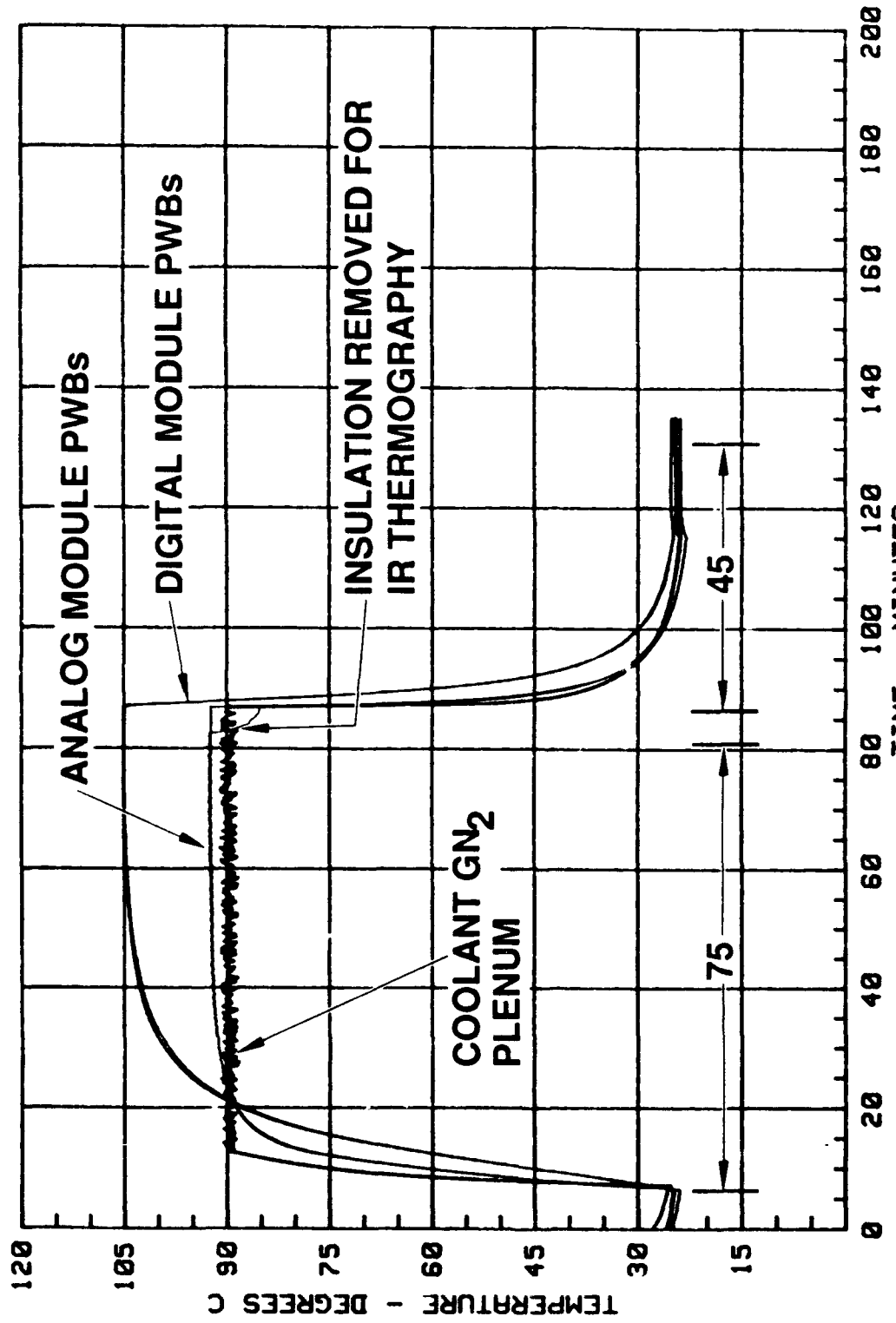


Figure 6-7. CERT Thermal Profile

In production, the manufacturing functional tests are performed with ambient-temperature coolant. Fortunately the functional performance was the same at elevated temperatures as at nominal. If this had not been the case, we would have had to establish the functional performance at elevated temperature to determine failure criteria.

For the linear (analog) modules, the test consists of monitoring the output voltages. Resistors simulated the analog module loads in a radar unit, as shown in Figure 6-3.

For the digital modules, the test consisted of:

- applying about 1,000 logic states (called test vectors) to the inputs
- reading the resultant states of the outputs
- comparing the output states to a table of expected states.

This test employed a diagnostic connector (shown in Figure 6-6), which is not present during flight. The absence of vibration enabled this diagnostic connector to be connected during environmental stressing.

The test of each of the two linear modules lasted about 1/2 minute, and the test of each of the two digital modules lasted about 2-1/2 minutes. Thus each test specimen was tested about a dozen times during each 75-minute CERT thermal cycle.

The linear module test specification (Appendix E of Appendix R) requires testing at two conditions, one of which is much higher power than the other. To prevent overheating at the higher power condition, this condition was used only for brief periods with the coolant at ambient temperature. Every time the test station was rebooted, which happened about once a week, the following sequence occurred:

Start (0 min):

- Digital module power on.
- Linear module power on at condition 2 (55 W).
- Test linear modules.

After completion of linear module test (approximately 1 min):

- Linear module power at condition 1 (15 W).
- Open valve allowing GN2 to pass through heater.

After completion of series of tests of all modules in progress 75 minutes after start:

- Power off all modules.
- Close valve that allows GN2 to pass though heater.
- Open valve for high-pressure GN2 bypass line.

120 minutes:

- Digital module power on.

- Linear module power on at condition 1 (15 W).
- Open valve allowing GN2 to pass through heater.

After completion of series of tests of all modules in progress 75 minutes after start of cycle:

- Power off all modules.
- Close valve that allows GN2 to pass through heater.
- Open valve for high-pressure GN2 bypass line.

240 minutes:

- Repeat 120- to 240-min cycle.

360 minutes:

- Repeat 120- to 240-min cycle.

6.5.2 Test Station Development

The following problems had to be overcome in the development of the test station.

- electromagnetic interference (EMI) in the test fixture
- incompatibility of digital module test patterns with ERFM test approach
- test station hardware and software problems
- false indications of digital module failures

6.5.2.1 Test Fixture

The test fixture was reworked to reduce EMI:

- Added capacitors in parallel with input lines to reduce edge rates
- Isolated and shortened clock and clear lines
- Shortened and isolated all input lines
- Minimized ground line length by installing additional bus bar
- Provided common ground point for all signals and supplies
- Unbundled and shielded output wires
- Selectively masked in test pattern

These measures appeared to reduce the EMI to an acceptable level.

6.5.2.2 Digital Module Test Patterns

We found that the test patterns presently used on the Hewlett-Packard DTS-70 are incompatible with our test approach. The patterns are used on the DTS-70 with an adapter containing multiplexers and other active circuitry. They do not represent direct input and output rates at the module connectors. Also, the masking information (that is, when to ignore certain

outputs) is not present in the patterns. Translation was impractical, due to the complexity of the adapter and the scarcity of documentation.

Since we were unable to use the existing test patterns, we had to develop our own. Developing patterns based on the circuit diagrams would be time-consuming and costly. So we decided to generate pseudo-random input vectors, apply them, and capture the resulting output states. We used these output states to compare against the outputs of the modules during the CERT. If an output changed, we assumed the module failed.

Using pseudorandom inputs, we were able to capture output patterns to create a repeatable test for the digital modules. This required some experimentation but, by modifying the input patterns and masking selected output states, we arrived at a repeatable test pattern for the outputs connected to the main Summation test frame. These comprised 103 of the digital module 276 outputs.

The remaining 173 outputs are connected to the Summation expansion box. The results from the expansion box were still unstable, after EMI reduction stabilized the main frame results. We determined that the expansion box was not synchronizing properly with the main frame.

After a fruitless pursuit of a solution to the synchronization problem, we decided to partition the test. We copied the input states to the expansion box, and ran the main frame and expansion box tests serially rather than concurrently. This yielded a stable test on nearly all the pins in the expansion box. Also, since all the inputs are operated in both tests, there is no change in the module duty cycle.

These actions achieved a stable test for all but 12 of the module 276 outputs. Six of these 12 outputs are not monitored in the factory and depot tests. The remaining six outputs are from the following integrated circuits:

IC	Output(s) Not Monitored	Dissipation (W)	Junction Temperature in Normal Operation (°C)
U1606	1	0.099	64
U2409	1	0.053	53
U2609	3	0.053	56
U2711	1	0.118	62

(The in-flight junction temperatures were predicted by the thermal analysis documented in Appendix F.) These four ICs have low dissipations and junction temperatures compared with other ICs on the module, some of which dissipate more than 0.5W and have junction temperatures over 90°C. Therefore, it was unlikely that any of these four ICs will be the first to fail in the CERT. Thus, masking these six outputs appeared to produce very little risk of compromising the program objective.

At the end of December 1990, we had a stable test for the digital modules.

6.5.2.3 Test Station Software

During the early part of the CERT in March 1991, the test station computer occasionally "crashed," shutting down the test. We isolated the cause of the computer "crashes" to memory allocation problems in the Microsoft Windows operating system.

We developed a workaround solution which provided continuous operation, but required a technician to perform a simple keyboard operation every four cycles. This would mean a maximum unattended operating period of 8 hours. Since the laboratory is manned nominally Monday morning through Saturday morning, we would be able to perform the CERT test, but we would lose a significant portion of the weekends.

To solve this problem, in April 1991 we upgraded the Test Station operating system from Microsoft Windows 2.1 to Microsoft Windows 3.0. Version 3.0 is widely known to be much more stable and serviceable than earlier versions. This proved to be true—the memory allocation crashes disappeared entirely.

The new software had one small problem. Possibly due to the longer operating time, we began experiencing random communication bus failures, after 1 to 10 hours of operation. A minor revision to the test software eliminated the problem.

6.5.2.4 Digital Module Failure Criteria

Numerous indications of failure interrupted the CERT. However, examination of the test station failure data log and of electrical performance and temperature data indicated that these failure indications are false.

During the course of test station integration and CERT, we adjusted the criteria for identifying module failures. We determined several conditions which were apparent failures, but were not due to failure of the modules under test. In most cases, these apparent failures were due to test fixture or other hardware problems:

Same Failure on Both Modules. It is extremely unlikely for both modules to fail at the same time in the same way. When such failures occur, the Summation test hardware is at fault. The same hardware is multiplexed to test both modules, producing identical failure vectors. These paired failures can begin at any time during the CERT test, and usually continue for several test iterations. We masked these failures in the CERT test.

Output Patterns. The test station software is not able to examine the captured output patterns. We examined them manually to determine the validity of several instances in which the test station reported a failure. We discarded failures which showed massive blocks of zeros on complimentary outputs, which indicated a failure of the test hardware or software.

The software upgrade virtually eliminated this false failure mode. To upgrade the operating system, we had to upgrade the test software, from Summation's "TestWindows" to "TestWAVE." This was also a desirable upgrade. According to Summation, TestWindows is no longer fully supported, and TestWAVE handles large patterns much better.

Single Event Failures. In some cases, failures occurred only once, or several times, then did not repeat. There was no pattern of the failures corresponding to test duration or instantaneous test specimen temperatures. The same module would pass repeatedly after registering a failure. These results probably were caused by remaining EMI problems in the test fixture.

To mask these failures, we programmed the test station to report a hard failure only when a module failed 10 times in a row on the same vectors. (This technique is known as filtering and is used in some Hughes Aircraft Company radar systems to reduce false alarms and "cannot duplicates.")

In one case where there appeared to be a module failure, we replaced the test specimen with one of the known good modules. The failure remained, and was presumably due to fixture or test hardware problems. We masked the pins and vectors which were failing, and continued the CERT. The ability of the Summation test equipment to mask individual signals and test vectors allowed us to minimize the effect on fault coverage.

6.5.3 Automation of Operation, Monitoring and Data Recording

The test station was integrated with the environmental test laboratory control system to enable unattended operation, monitoring, and data recording on evenings and weekends. Upon detecting a failure of one of the test specimens, the test station:

- sounded an alarm
- stored diagnostic information
- shut down the test by activating the cooldown portion of the thermal cycle shown in Figure 6-7.

Alarms and automatic shutdown also were implemented for:

- excessive plenum temperature
- coolant GN2 heater failure (plenum temperature not increasing to 180 F within specified period after heat command)
- insufficient coolant flow (excessively low plenum pressure)
- test station computer failure (watchdog timer).

These are shown schematically in Figure 6-1. The controllers and instrumentation are shown in Figures 6-4 through 6-6.

6.6 INSTRUMENTATION AND INSPECTION

6.6.1 Control and Monitoring of Test Conditions

Test conditions were controlled by a thermocouple and a pressure transducer on the coolant inlet plenum. The plenum temperature and pressure were recorded on the laboratory automated data system and displayed, as shown in Figure 6-4. The plenum temperature also was recorded on circular charts.

Thirty thermocouples were mounted with epoxy on the modules – 10 on each of the digital modules and 5 on each of the analog modules. The locations, shown in Figures 6-8 and 6-9, were chosen on the basis of the thermal analyses and the special inspection of the parts:

- highest junction temperature
- highest mounting surface temperature
- largest thermal time constant
- integrated circuits found (see Section 4.0) to have rejectable:
  - die attach
  - particles
  - hermetic seal leakage
- hybrid microcircuits for which earlier S/Ns failed in the field (see Section 3.0).

These data were recorded and displayed as shown in Figure 6-4.

The plenum temperature, plenum pressure, and module temperatures were recorded every 10 minutes. Once a week, the sample rate was increased to every 10 seconds for one CERT thermal cycle. These high sample rate data were tabulated and plotted for evaluation of trends.

6.6.2 Nondestructive Evaluation

Two methods were considered for periodic inspection of the modules to determine signs of aging:

- holographic interferometry (HI)
- infrared (IR) thermography.

6.6.2.1 Holographic Interferometry

MetroLaser, Irvine, California, was awarded a subcontract to perform a survey of optical nondestructive test methods to determine the best approaches for both on-site and off-site testing of the modules during CERT and to estimate the cost of these approaches (Ref. 6-2).

MetroLaser identified three optical techniques that would be applicable to the EFRM Program testing requirements:

- Holographic Interferometry

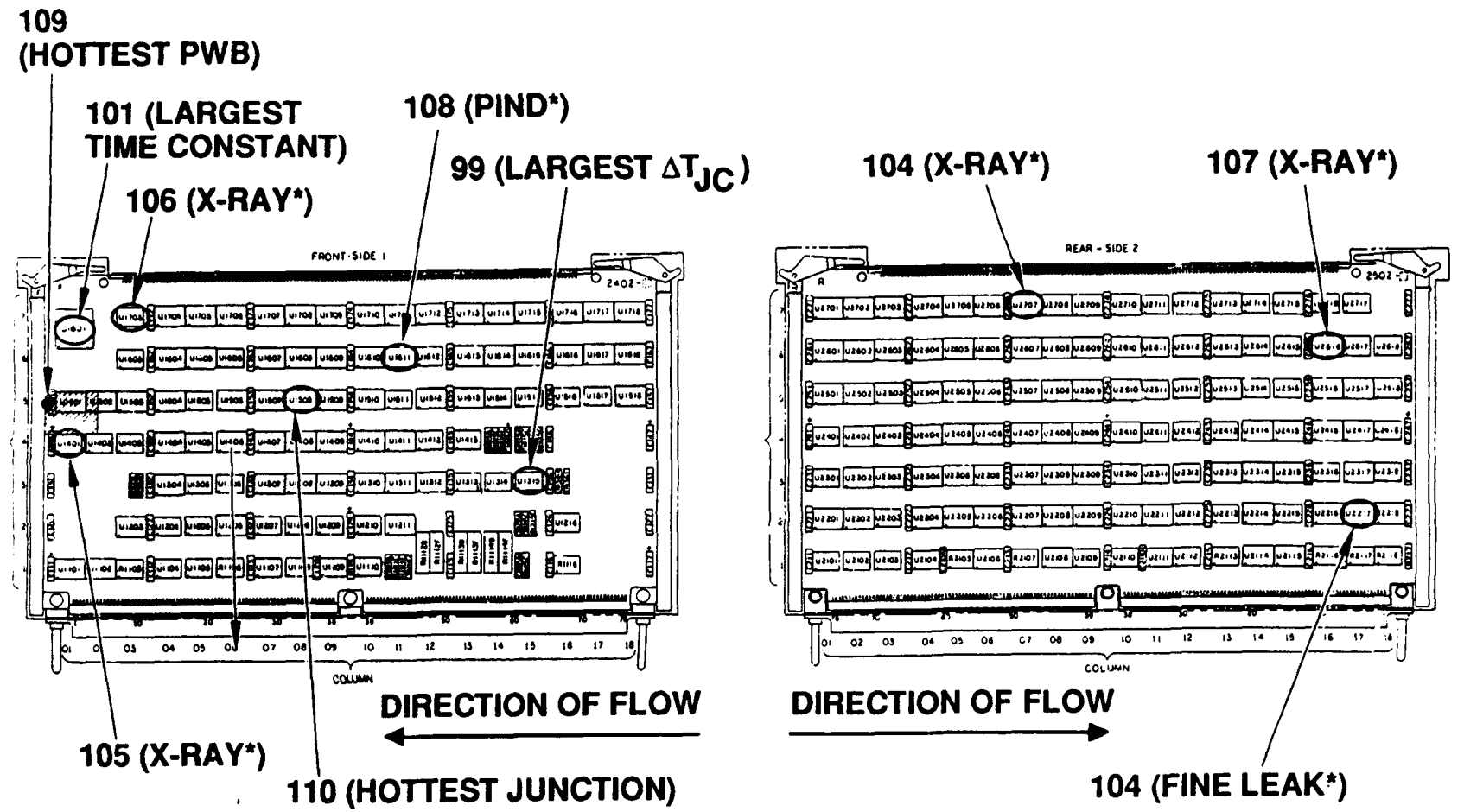


Figure 6-8. Highest Case/PWB Temperatures (°C) on Digital Module During CERT

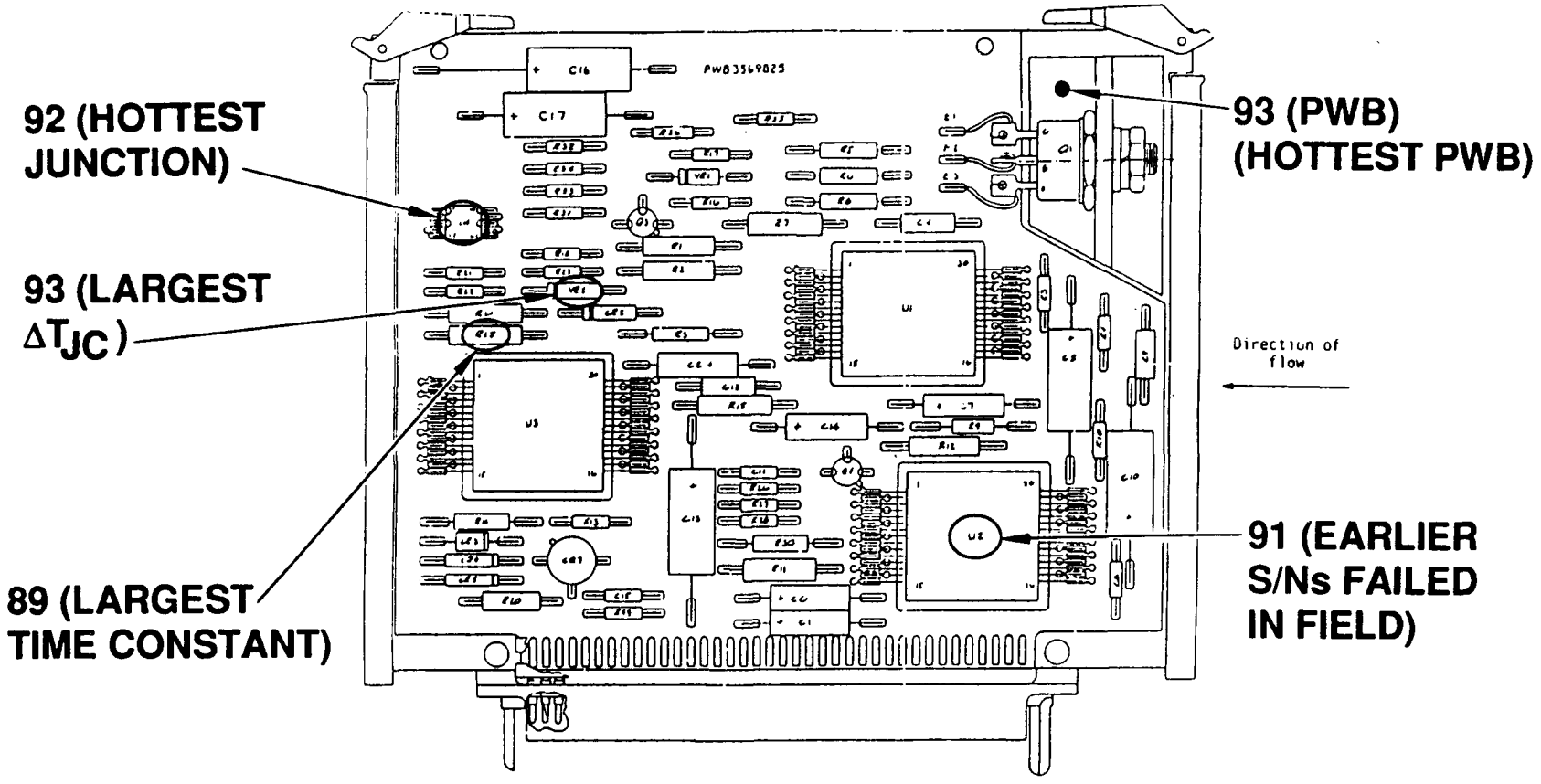


Figure 6-9. Highest Case/PWB Temperatures (°C) on Analog Module During CERT

- Electronic Speckle Pattern Interferometry (or TV Holography)
- Electronic Shearography.

Holographic interferometry was judged to be the optimum choice because of its superior resolution capability. Requirements for the monitoring of the modules during CERT required that defects such as lifted solder pads and cracked solder joints be detectable. Only holographic interferometry offered this level of resolution.

On-Site Testing: In their report, MetroLaser outlines several cost options for on-site testing depending on type of equipment and on whether Hughes were to buy or rent this equipment. Of these, the most cost effective option for the EFRM Program would be the rental of what MetroLaser refers to in their report as System 1: a Newport Research Corporation HC-1000 holocamera and associated hardware.

Besides the costs of the purchase order to MetroLaser for the on-site testing, there would be additional costs to the program from internal efforts associated with the test plan. The 35mW HeNe laser utilized in the HI test system is considered a Class 3b laser. Since the beam would not be completely enclosed in the test setup, various safety considerations must be addressed. These include an enclosure for the test area (this would be required in any event to attenuate ambient light levels) with warning signs and a flashing beacon, training and certification of the operators, a written standard operating procedure, and a laser eye exam for the operators. Also, Hughes personnel would be required to monitor and facilitate the testing while it is being conducted.

Off-Site Testing at Intervals During CERT: Testing of the modules off-site at intervals during CERT was investigated due to its significantly lower cost. Off-site HI testing would not provide the realistic stress conditions of the temperature cycling under power that on-site testing would. However, HI testing at MetroLaser was effective in the testing program performed at intervals during fabrication of the modules (see Section 4.0). Off-site testing, as quoted by MetroLaser in their report, would consist of removing the modules from CERT once each month during the 6-month environmental testing program for a 3-day sequence of HI inspection. Additional costs to the program involve Hughes personnel transporting and handling the modules.

Off-Site Testing at Failure or End of CERT: Another option considered was that of HI testing of the module off-site by MetroLaser only after they fail or at the end of CERT. This option would require at most four individual HI inspections of one day each, assuming that each of the modules fails at a different time, and at least one 3-day test sequence if none of the modules fail and they are all tested together at the conclusion of the CERT.

On-site HI was concluded to be too expensive and technically risky. Off-site testing at intervals during CERT was concluded to be of insufficient benefit to justify its cost and risk of damage to the modules from handling. Off-site testing at failure or at the end of the CERT was planned, but was deleted as part of the program descope. Thus HI was not used.

6.6.2.2 Infrared Thermography

The purpose of this effort was to detect any changes in temperature which might indicate an impending failure by taking thermograms of the units under test at the beginning of the test and at various intervals during the life test. The first set of images was used as a baseline set of temperatures, with each subsequent image compared to the baseline to detect any changes in the module temperatures. (IR thermography also was used in this way in the tests reported in Ref. 6-3.)

The fundamental concept behind this approach is the ability to electronically compare two images to detect any changes from one to the other. This is accomplished by using a specially equipped computer to digitize video images generated by the Probeye 7300 thermography unit. These images are stored on magnetic media for future use. By using the TIMS (Thermal Image Management System) software, one image can be subtracted from another, generating a third image which would highlight any differences in the original images.

This approach is only valid if both images have the same temperature range and number of levels, and if the spatial arrangement does not change from one image to the other. The latter was accomplished by building a holding fixture for the Probeye imager which is permanently attached to the base of the test apparatus, thus ensuring that the location of the imager with respect to the modules did not change each time the test is performed. The fixture is shown in Figure 6-10. The distance between the imager and the modules was approximately 20 inches to enable scanning of the entire module surface without moving the imager. The fixture had six mounting positions for the Probeye, four to view each side of the two sided modules and two to view each of the single sided modules.

Equipped with the standard optics, the Probeye 7300 will resolve temperatures of features as small as 0.05 inch at a distance of 20 inches, while the detector sensitivity is 0.1°C. This combination of spatial resolution and temperature sensitivity makes the Probeye 7300 ideally suited for this application.

The thermographic imaging was performed at the beginning of the CERT while in the hot phase (power on, 63°C coolant inlet) before cycling began. Subsequent thermograms were taken at the end of a hot phase (steady-state conditions) before transition to cold phase.

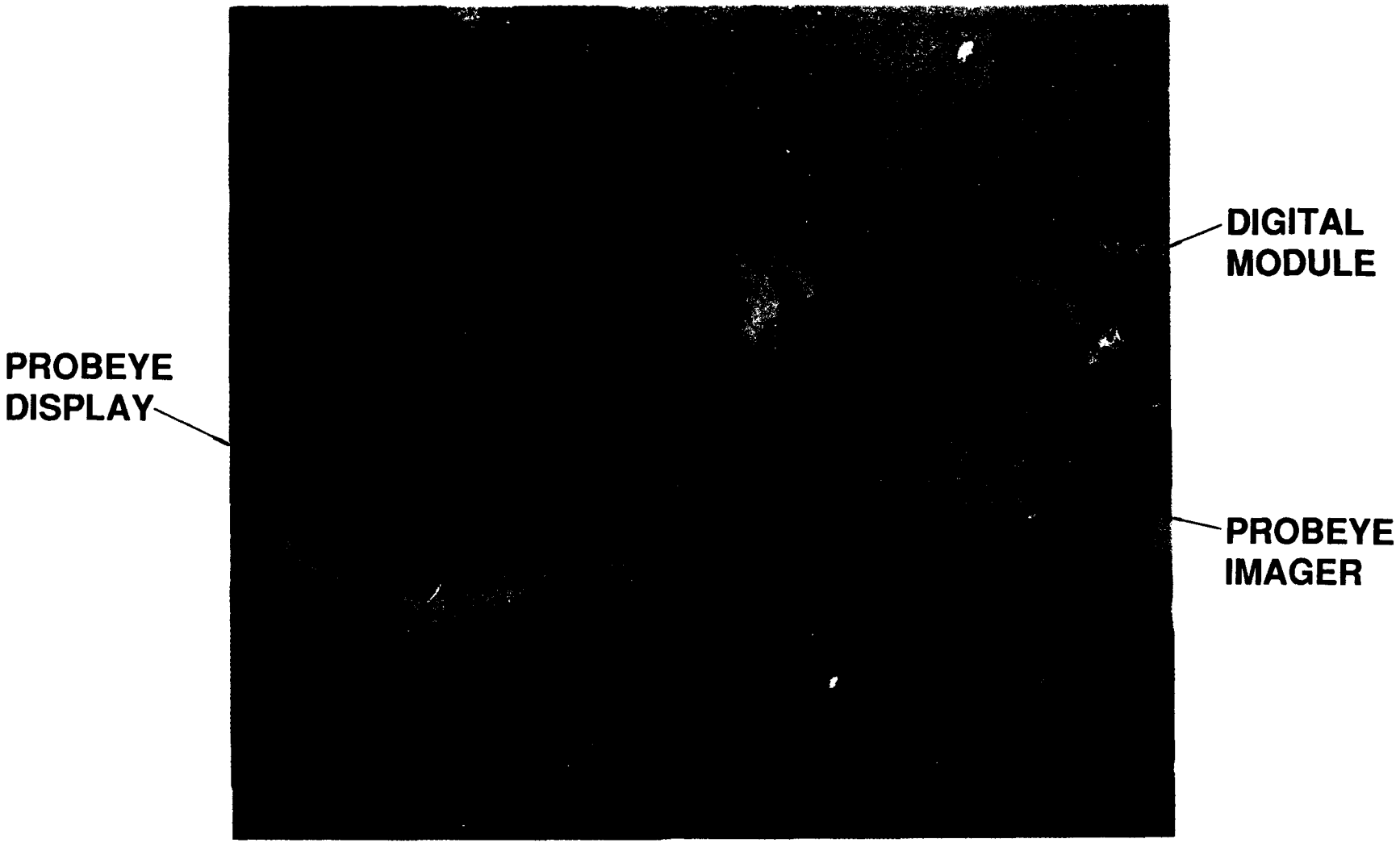


Figure 6-10. Infrared Thermography of Shop Replaceable Units (SRUs)

The temperature range and other image parameters were fine tuned during the first session, and the same settings were used for all the following measurements in order to enable accurate comparison of images.

IR thermography was used successfully, as it was in the tests reported in Ref. 6-3. It proved to be simple to use.

IR thermography was very helpful in answering questions raised by the contact (thermocouple) temperature measurements. During the CERT, some of the thermocouples indicated that some locations on the test specimens were becoming cooler. This could have been a sign of aging. However, IR thermograms showed that these temperatures were not changing. The decrease of the thermocouple outputs was attributed to debonding of the thermocouple junctions from the modules resulting from the thermal cycling. On one occasion, all the thermocouple readings on one of the modules decreased. IR thermography showed this to be due to the insulation on that module having been installed improperly after being removed.

6.7 RESULTS

The CERT was conducted during the period 22 March 1991 through 7 June 1991. It is documented in Ref. 6-4.

The module underwent nearly 500 CERT thermal cycles, between ambient temperature and temperatures much higher than in normal flight (see Figures 6-8 and 6-9) without failure.

Some of the laboratory hardware maintained at ambient temperature failed during the long-term test. For example, a wire in the watchdog timer circuit shorted on 30 May 1991. One such laboratory hardware failure caused the test specimens to stay at high temperature, rather than cycling, while unattended during the Memorial Day weekend; they operated normally afterward.

The analog modules showed only a single indication of failure in the entire CERT. Since the failure never repeated, we assumed it was spurious. As an additional precaution, we examined the data log files from the CERT, and found no significant changes in the analog module outputs during the CERT.

Thermographs were taken at the beginning of the test, approximately midway through the test, and at the end of the test (approximately 490 cycles). The purpose of this effort was to use IR thermography as a tool to detect any changes in unit temperatures during the course of the test which might indicate an impending failure. Three sets of thermographs were taken on each card tested. The temperatures were compared via image subtraction. The maximum temperature variation from beginning to end of the test found on any of the cards was approximately 2°C.

The thermocouple data and the data seen on the thermographs lead to the conclusion that no change in the peak operating temperature of the SRUs due to electronic component operation took place during the CERT.

6.8 CONCLUSIONS

- A relatively simple test setup has been developed for thermal/power cycling reliability testing of avionics modules.
- Special test equipment has been developed for powering and monitoring modules in a Combined Environments Reliability Test (CERT).
- Techniques have been developed to evaluate indications of failure in a CERT.
- Holographic interferometry has cost and technical disadvantages for periodic nondestructive inspection (NDI) during a long-term test.
- Infrared thermography is a very cost effective and powerful tool for NDI to complement contact temperature measurements during a long-term test.
- These APG-63 Radar modules are very durable.

7.0 CONCLUSIONS

7.1 FIELD FAILURES

Failed field modules from the F-15 AN/APG-63 Radar were obtained from Warner Robins Air Logistics Center for failure analysis. There were five confirmed failures of each of the two part numbers investigated. A statistical analysis of these failure data indicates that the following qualitative conclusions can be reached:

- A significant fraction of the failures of the analog module and a small fraction for the digital module result from the exacerbation of latent defects by environmental stresses. For the digital module, none of the five confirmed failures was from this result, indicating that the fraction in the total population is probably not much more than 0.2. For the analog module, four of the five confirmed failures are from this result, indicating that the fraction is probably not much less than 0.6 nor much more than 0.8.
- These five analog modules may have been in deployment for more than 5 years before they failed.
- The fraction of failures resulting from thermal cycling and vibration is small. Zero of the five confirmed failures of each part type was from this result, indicating that the fraction is probably not much more than 0.2.
- Increasing the sample size would provide more confidence in the precise values of these fractions but probably would not change these qualitative conclusions.

7.2 FIELD FAILURE ANALYSIS PROCEDURES

Procedures for determining the cause of field failures of electronic assemblies in an ongoing military program were developed and used successfully. The ERFM activity did not impact the inventory of assets at WR-ALC. A small sample of failed modules was sufficient. All SRUs analyzed were returned serviceable or with only the failed component removed.

7.3 ALTERNATIVE ANALYTICAL TECHNIQUES FOR FIELDED MODULES

Standard failure isolation, verification, and analysis techniques were used. Recently developed NDI techniques — digital X-ray laminography and holographic interferometry — were evaluated and not selected for use. The conclusions regarding these techniques are as follows:

- Digital X-ray laminography:
  - It has the potential to isolate and separately image each of the sides of a two-sided module.
  - The radiation dose is well below the threshold for any potential damage to the bipolar components on these modules.

- The film based method did not demonstrate sufficient sensitivity.

- Holographic interferometry:
  - For inspection of a small number of modules, detailed visual inspection is more cost effective.

Furthermore, identification of ionic contaminants responsible for component failure from mobile ionic contamination was concluded to be impractical due to the difficulties of performing surface analysis at liquid nitrogen temperatures.

7.4 SPECIAL FABRICATION/INSPECTION

Techniques have been developed to perform special inspection at various steps in a production process so that the location and size/severity of selected significant latent defects are known/bounded.

7.5 HOLOGRAPHIC INTERFEROMETRY ANALYSIS OF PRINTED WIRING BOARD ASSEMBLIES

Of the various stressing methods applied to the heat exchanger in this study, pressure stressing proved successful in revealing areas of debonding as verified by ultrasonic analysis.

Of the various stressing methods applied to the PWB in this study, thermal stressing proved the most successful in revealing the delaminations resulting from photoresist inclusions intentionally placed within the PWB. However, using real-time HI, only a triangular and 1/2-inch circular inclusions were found to be debonded within a pattern of inclusions that ranged in size down to 0.050 inch in diameter. Furthermore, these two inclusions (and especially the triangular inclusion) were so sensitive to the HI technique that no intentionally applied stress was necessary to cause a surface strain over them; naturally occurring environmental temperature changes were enough.

It is thus concluded that artificial delaminations are currently difficult to produce with certainty using photoresist/mold release inclusions but that, once produced, these areas can be very sensitive to thermal stressing.

Holographic interferometry has the necessary sensitivity to reveal these defects and the necessary resolution to reveal two delaminations within the 1/2-inch by 1-inch triangle. However, because of the difficulty of producing artificial defects with a high degree of certainty, the resolution limit of HI in this context has not yet been addressed.

7.6 IONIC CONTAMINATION FAILURE MODE AND MECHANISM

- The mode and mechanism of ionic contamination induced failure of a hybrid microcircuit have been identified.

- The failure mode/mechanism explains the failures of negative regulators in the field and in a screen, and it explains the absence of failures of comparable positive regulators.

7.7 IONIC CONTAMINATION SCREEN

A method has been developed for using the screen to bound the voltage shift that could occur in deployment.

7.8 IONIC CONTAMINATION MODEL

A method was developed to predict the effects of varying distributions of ionic contamination on the electrical behavior of a transistor. By determining the lowest acceptable gain of the t nsistor for proper operation of the hybrid, the time-to-failure for the hybrid was determined from the model.

Data from the hybrid screen showed good correlation to the change in transistor gain predicted by the model.

The methodology used to develop the model is applicable to other devices with different geometries than the specific device analyzed. The methodology also could be used as a basis for determining the effects of other types of charge induced fields on device electrical behavior.

Using the methodology discussed in this report, burn-in or screen times could be accurately determined based on a device geometry and electrical function. These times could be significantly decreased for some devices by selecting an appropriate electrical parameter to monitor and establishing acceptable deltas for these times based on the behavior predicted by the model.

7.9 COMBINED ENVIRONMENTS RELIABILITY TEST

- A relatively simple test setup has been developed for thermal/power cycling reliability testing of avionics modules.
- Special test equipment has been developed for powering and monitoring modules in a CERT.
- Techniques have been developed to evaluate indications of failure in a CERT.
- Holographic interferometry has cost and technical disadvantages for periodic nondestructive inspection during a long-term test.
- Infrared thermography is a very cost effective and powerful tool for nondestructive inspection to complement contact temperature measurements during a long-term test.
- These APG-63 Radar modules are very durable.

8.0 RECOMMENDATIONS

1. Conduct a field failure investigation like the one described here for hardware whose deployment history can be tracked by serial number. This will ensure that the sample is random and that the field failures are the first of each S/N. Several data bases having this capability are available at Hughes, including that for the APG-70 radar developed under the Multi-Staged Improvement Program (MSIP) for the F-15 aircraft.
2. investigate nonfilm based methods for performing X-ray laminography.

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APPENDIX A

FACTORY FAILURE HISTORY OF 2102 AND 9800 MODULES

INTERDEPARTMENTAL CORRESPONDENCE

TO: C. H. Spruck
ORG: 22-06-00

C: R. D. Ritacco
J. M. Kallis
W. W. Kusumoto

DATE: 09 June 1988
REF: 220400.88/71

SUBJECT: Factory Failure History of P/N's 3562102 and 3569800

FROM: T. C. Preston
ORG: 22-04-10

BLDG. R7 MAIL STA. 902
LOC. RE PHONE 334-4551

Per your request, all the available factory failure data gathered during Unit and System Level screening and testing of P/N's 3562102 and 3569800 are summarized herein. These data were compiled during screening and testing of approximately 450 P/N 3562102's and 400 P/N 3569800's. Tables I-III summarize the frequency of primary failures by "Failure Cause" versus "Environment" for P/N 3562102 during Unit Aging, System Burn-In and System Test, respectively. Tables IV-VI contain identical data for P/N 3569800. Listed in Table VII is a summary of the descriptions of all the failure causes.

Figures 1 and 2 describe the ESS profiles to which the subject SRU's are exposed during the Unit Aging and System Burn-In screens. Figure 3 contains a concise description of these two screens.

Figure 4 contains pie charts showing the relative frequency of occurrence of the primary failures summarized in Tables I-VI.

T. C. Preston

T. C. Preston

TCP:jc

TABLE A-1

SUMMARY OF P/N 3562102 PRIMARY FAILURES
DURING THE UNIT AGING SCREEN

FAIL CAUSE	AMBIENT	INSTALL FAILURE	TEMP CHANGE	HIGH TEMP	LOW TEMP	TOTAL	PERCENT OF TOTAL
DP	23	1	1	18	29	72	67
EW	1			1*	1	3	3
UU	5		2	8	3	18	17
UK	6			2	2	10	9
CO					1	1	1
OS					1	1	1
RH	1					1	1
IT	1					1	1
TOTAL	37	1	3	29	37	107	100

* BAD SOLDER JOINT

TABLE A-II

SUMMARY OF P/N 3562102 PRIMARY FAILURES
DURING THE SYSTEM BURN-IN SCREEN

FAIL CAUSE	AMB	INSTALL FAIL	TEMP CHANGE	HIGH TEMP	HIGH TEMP AND VIB	LOW TEMP	LOW TEMP AND VIB	TOTAL	PERCENT OF TOTAL
DP	7		3	8	1	4	1	24	64
EW	2*		2*			1*		5	14
UU						1		1	2
UK	2		1	2				5	14
ZR	1			1				2	5
TOTAL	12		6	11	1	6	1	37	100

* ONE COLD SOLDER JOINT FAILURE

TABLE A-III

SUMMARY OF P/N 3562102 PRIMARY FAILURES
DURING SYSTEM TEST

FAILURE CAUSE	QUANTITY OF FAILURES	PERCENT OF TOTAL
DP	44	67
EW	5*	8
UU	3	4
UK	4	5
CO	1	1
RH	2**	3
TE	1	1
ZR	5	8
WP	1	1
TOTAL	66	100

* ONE COLD SOLDER JOINT; ONE SOLDER BRIDGE; ONE NOT SOLDERED

** ONE NICKED JUMPER WIRE

TABLE A-IV

SUMMARY OF P/N 3569800 PRIMARY FAILURES DURING THE UNIT AGING SCREEN

FAIL CAUSE	AMBIENT	TEML CHANGE	HIGH TEMP	LOW TEMP	TOTAL	PERCENT OF TOTAL
_DP	4	1	4	8	17	55
EW		1*	2	1*	4	13
UU			2	1	3	10
UK		2	2	2	6	19
IE			1		1	3
TOTAL	4	4	11	12	31	100

* COLD SOLDER JOINT

TABLE A-V

SUMMARY OF P/N 3569800 PRIMARY FAILURES DURING THE SYSTEM BURN-IN SCREEN

FAIL CAUSE	AMBIENT	TEML CHANGE	HIGH TEMP	LOW TEMP	TOTAL	PERCENT OF TOTAL
_DP		2	5	3	10	63
UU	1			1	2	12
ZR	2	1			3	19
RS		1			1	6
TOTAL	3	4	5	4	16	100

TABLE A-VI

SUMMARY OF P/N 3569800 PRIMARY FAILURES DURING SYSTEM TEST

FAILURE CAUSE	QUANTITY OF FAILURES	PERCENT OF TOTAL
DP	4	80
RH	1	20
TOTAL	5	100

TABLE A-VII

DESCRIPTION OF FAILURE CAUSES

CO ... CONTAMINATION
DP ... DEFECTIVE PART
EW ... EQUIPMENT WORKMANSHIP
IT ... INTERMITTENT (UNIT CNV)
OS ... OVERSTRESSED
RH ... ROUGH HANDLING
TE ... TEST EQUIPMENT
UK ... UNKNOWN (MODULE CNV)
UU ... REPAIR DATA INCOMPLETE/LOST
UP ... WRONG PART
ZR ... REPEAT SYMPTOM WITH REWORK PERFORMED
RS ... RESEATED
IE ... INSTALLATION ERROR
BS ... BAD OR COLD SOLDER JOINT

APG-63 UNIT AGING ENVIRONMENTAL PROFILE

F-15 RADAR

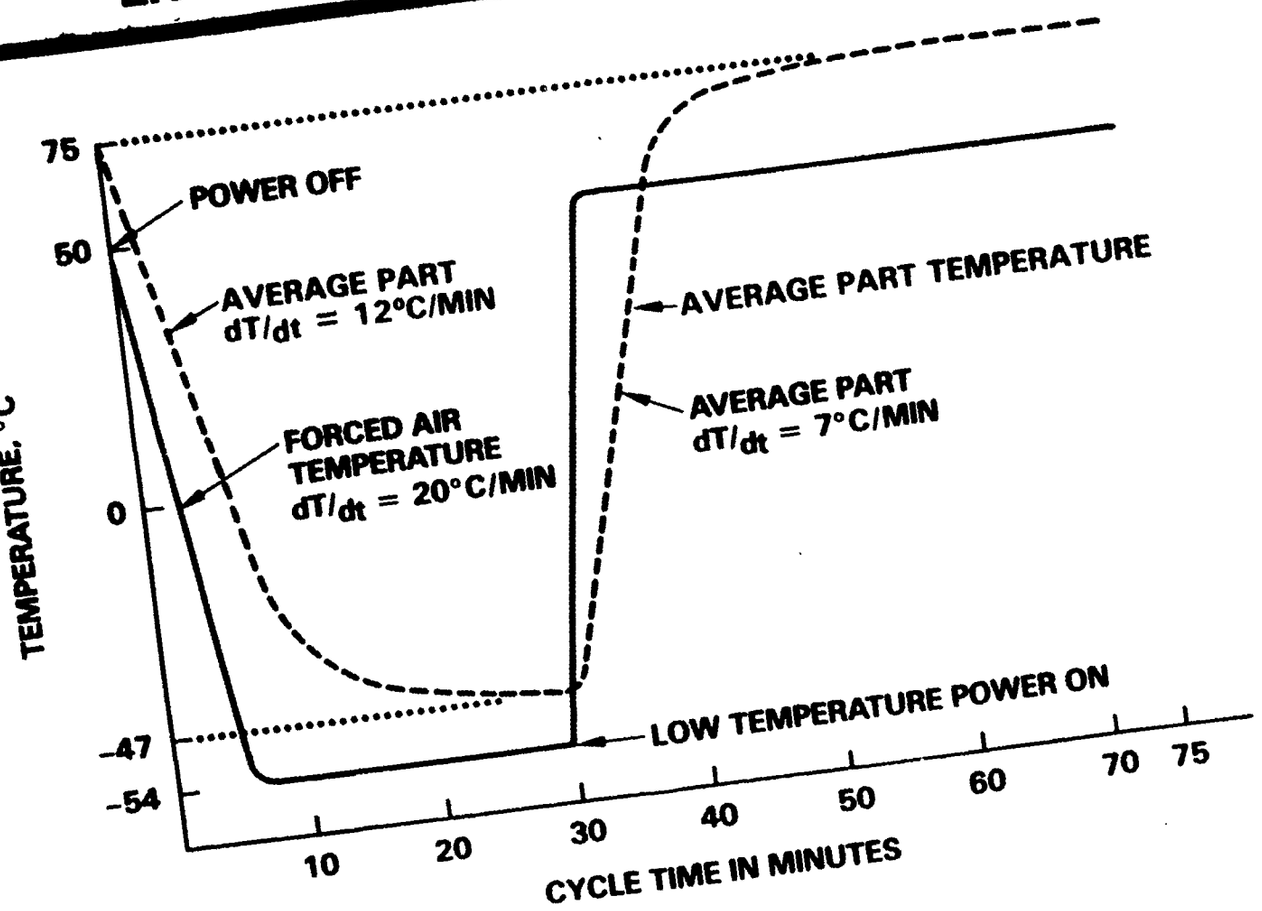

FIGURE A-1

APG-63/70 RADAR SET BURN-IN ENVIRONMENTAL PROFILE

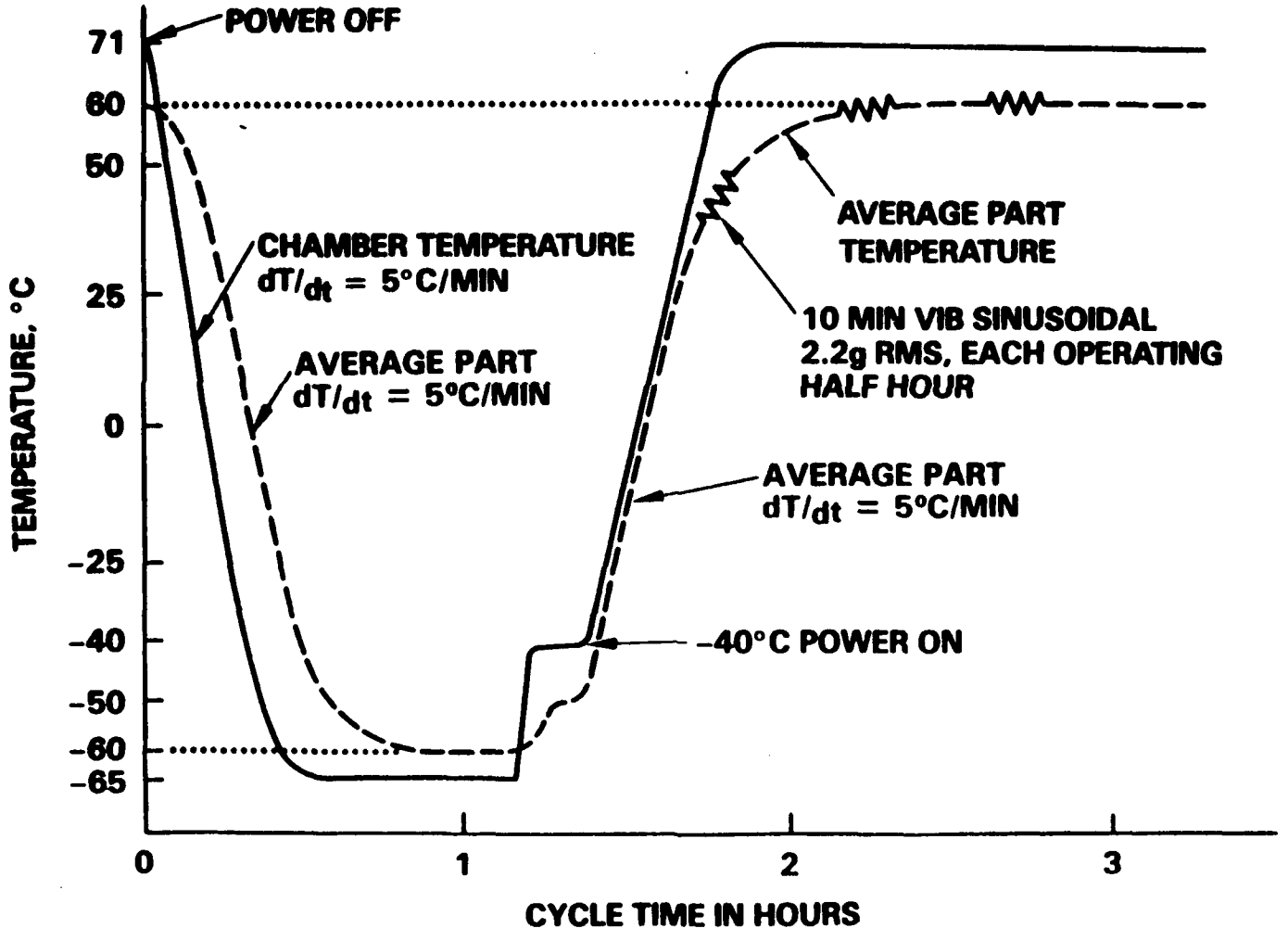

FIGURE A-2

F-15 RADAR STRESS SCREENING
REVISED SCREENS

- ASSEMBLY CONDITIONING - 23 HOURS "POWER OFF" TEMPERATURE CYCLING (-60°C TO +95°C); 46 ONE-HALF HOUR CYCLES; 15°C PER MINUTE CHAMBER TEMPERATURE RATE OF CHANGE; 5 MINUTE DWELL AT EACH TEMPERATURE EXTREME.

- UNIT AGING - 40 HOURS "POWER ON AND OFF" TEMPERATURE CYCLING (-54°C TO +50°C COOLING AIR) (PART CASE TEMPERATURE VARYING FROM -54°C TO +80°C); 32 "1.25 HOUR" CYCLES; POWER ON 60% OF THE TIME; 20°C CHAMBER TEMPERATURE RATE OF CHANGE; LAST CYCLE MUST BE FAILURE-FREE; CONDUCTED ON 4 LRU'S WHICH CONTAIN 85% OF PARTS IN RADAR SET.

- RADAR BURN-IN - 48 HOURS "POWER ON AND OFF" TEMPERATURE CYCLING (-65°C TO +71°C); 3.25 HOUR CYCLE; 5°C PER MINUTE TEMPERATURE RATE OF CHANGE; 30 MINUTES OF 2.2G SINUSOIDAL VIBRATION DURING ON PORTION OF EACH CYCLE. 15 CYCLES TOTAL; LAST 3 CYCLES FAILURE-FREE (AT LRU LEVEL); CONDUCTED ON ALL 9 LRU'S CONFIGURED AS A RADAR SET.

FIGURE A-3

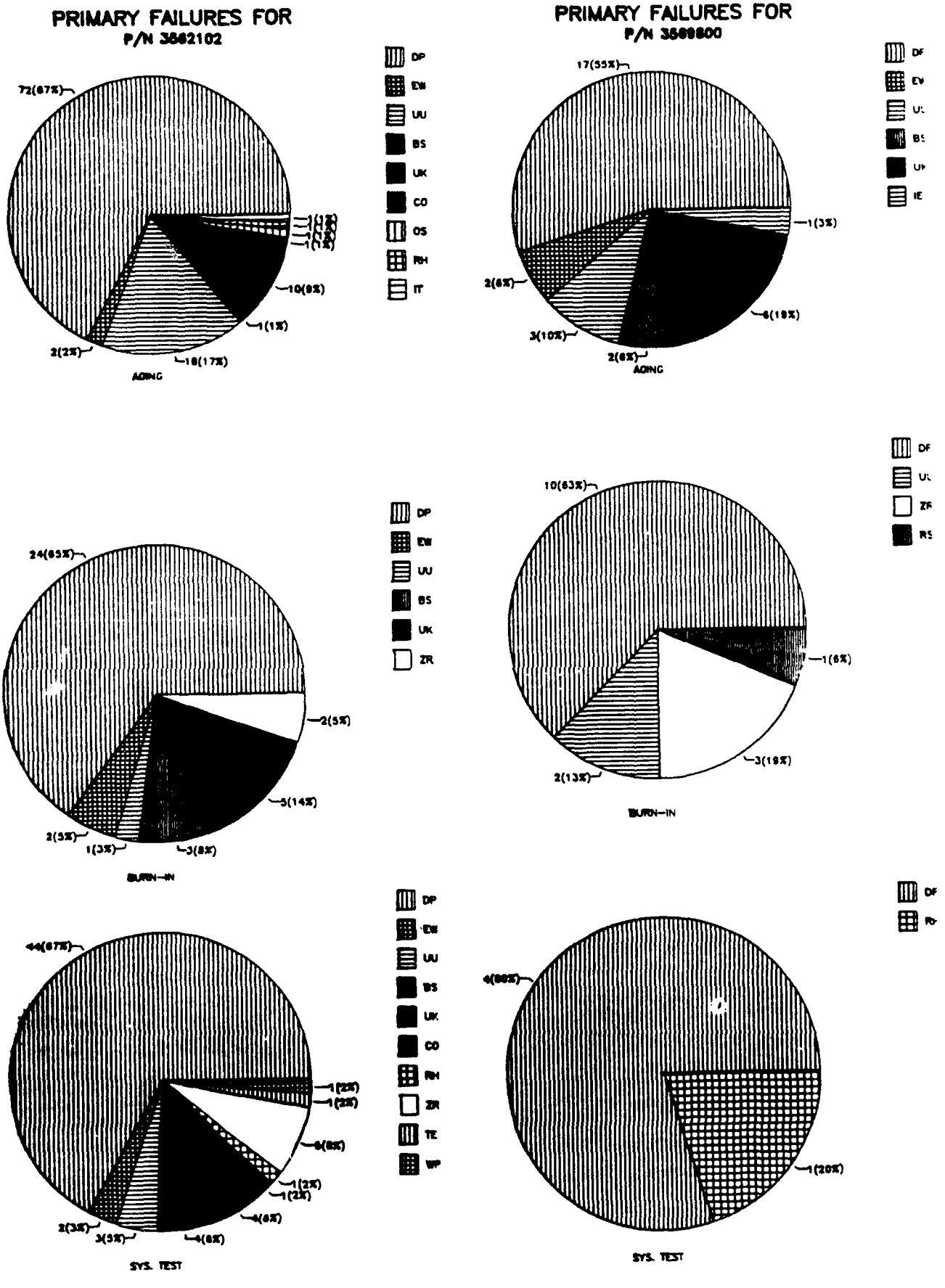
PRIMARY FAILURES FOR
P/N 3662102
72(67%)
10(9%)
1(1%)
2(2%)
18(17%)
AGING
DP
EW
UU
BS
UK
CO
OS
RH
TT
PRIMARY FAILURES FOR
17(55%)
1(3%)
2(6%)
6(19%)
3(10%)
2(6%)
AGING
24(65%)
2(5%)
5(14%)
2(5%)
1(3%)
3(8%)
BURN-IN
DP
EW
UU
BS
UK
ZR
10(63%)
1(6%)
3(19%)
2(13%)
BURN-IN
44(67%)
1(2%)
1(2%)
4(6%)
1(2%)
1(2%)
2(3%)
3(5%)
4(6%)
SYS. TEST
DP
EW
UU
BS
UK
CO
RH
ZR
TE
WP
1(20%)
SYS. TEST

FIGURE A-4

APPENDIX B

ANALYSIS OF EFFECT OF X-RAY
DOSE ON FAILED FIELD MODULES

INTERDEPARTMENTAL CORRESPONDENCE

TO: Dan Buechler
ORG 76-41-22

C: R. D. Ritacco

DATE: June 29, 1988
REF: 7641.30/1091

SUBJECT: Effect of Faxitron X-Ray Dose on Microcircuits in Dwg 3562102 and 3569800.

FROM: M. Reier
ORG: 76-41-10

BLDG. E2 MAIL STA. S107
LOC. E0 PHONE 65445

Ref: IDC 7641.30/986, March 10, 1988.

This IDC discusses the components which were analyzed in the above referenced IDC which is affixed to the present one.

The previous calculation showed that the worst case exposure was 1087 Rads at a distance of 45 inches from the x-ray target using an accelerating potential of 120KV and an anode current of 3ma.

Only active parts were considered. It was assumed that diodes, transistors, 54S and 54LS parts have a design margin at least 25 times the expected dose and did not warrant further investigation. All the parts checked in detail are made using bipolar technology which is relatively hard to total dose. There are four 54F parts shown in items 76-79 in Dwg 3562102. Data could be obtained on 54F109, 138 and 151. The 54F151 was tested to 5 KRads and showed negligible change in the parameter most sensitive to radiation. The 54F109 and 54F138 failed at 9 and 13.4 KRad, respectively. Radiation data could not be found on the 54F163. However, 54F parts are known to be hard to, at least, eight to ten KRad.

Item 36 of Dwg 3569800 is an LM119, a dual comparator, which is a class of linear devices. The radiation tests found in the literature were performed with a mix of 3×10^{11} neutrons and total gamma dose of 100, 300 and 500 KRad. Input offset voltage and input bias current passed at the 100 KRad level. Input offset current was about 50 percent above maximum specification at 100 KRad and got progressively worse at higher levels. It can be assumed that it would have passed at one KRad.

Items 34 and 35 of Dwg 3569800 are hybrids. They are high power positive and negative voltage regulators, respectively. They are both planar passivated semiconductors. They have not been tested for total dose vulnerability. However, based on their technology, they should be radiation hard to many times the anticipated exposure at the Faxitron.

Items 3-8 on Dwg 3562102 are Monolithic Memory 5301, a 256 X 4 ROM. With the exception of newer technologies such as 54FXX, digital bipolar devices are known to have total dose sensitivity levels considerably above one KRad.

Mel Reier

M. Reier, Senior Scientist/
Engineer

INTERDEPARTMENTAL CORRESPONDENCE

TO Dan Buechler C: R. D. Ritacco DATE: March 10, 1988
ORG 76-41-22 REF: 7641.30/986

SUBJECT: X-Ray Dose From the Faxitron. FROM: M. Reier
ORG: 76-41-10

BLDG. E2 MAIL STA. S107
LOC. E0 PHONE 65445

Calculations were made of the total dose absorbed by silicon based semiconductors at accelerating potentials of 80, 90, 100, 110, and 120 kV. Since no measurements were made, this report is based on those made on the Real-Time x-ray facility using LiF TLD's (thermoluminescent detectors) included as an appendix.

A brief discussion of the appendix will be presented. The LiF TLD's had been calibrated using the GR9M cobalt-60 source which emits gamma rays with an average energy of 1.25 Mev. Although silicon and LiF have a similar energy response around one Mev, their response functions differ greatly at low x-ray energies primarily due to the increasing importance of the photoelectric effect in silicon compared with LiF. In order to analytically correct the LiF calibration the x-ray spectrum had to be known. The x-ray spectrum from a tungsten target at several accelerating potentials up to 50kV was found in the literature (Ref. 2, appendix). It It was also shown to a high degree of accuracy that the wavelength at maximum intensity was inversely proportional to $V^{1/2}$ where V is the anode potential. The intensity vs wavelength of Ref. 2 was replotted as intensity vs energy and the effective x-ray energy, E, was calculated to be 1.08 Emax, where Emax is the energy at maximum intensity. It was then assumed that the relationship between Emax and V was valid up to 100kV, the operating voltage of the Real-Time x-ray, and that the shape of the spectrum for 100kV was the same as that for 50kV. Using these assumptions and the detailed analysis of the 50kV data, E for 100kV was calculated to be 40KeV. From Ref. 3 in the appendix the ratio at 40keV of the response of silicon to the TLD used in the Real-Time x-ray measurement was found to be 6.74, a number which multiplies the dose rate results from the TLD data.

Table II of the appendix is used as basis for estimating dose rates for the Faxitron at a distance of 45 inches from the tungsten anode. Although one would expect maximum dose rates would be at y=z=0, this was not always true (Table II, appendix) because of shielding by the source

and the clamp holding the experimental fixture. The maximum dose rate values from Table II at X=10, 14, and 18 inches were corrected to 45 inches assuming r^{-2} attenuation and averaged. This was multiplied by the ratio of the expected Faxitron current (3 ma) to the current used in the measurements of the appendix (0.04 ma). The result for a five minute exposure at 100kV anode potential is 755 Rad. This value can be adjusted for other accelerating voltages since the total x-ray energy is proportional to V^2. The dose in the Faxitron for a five-minute exposure at 45 inches from the target and a current of 3 ma is shown in Table I for several anode voltages near 100kV. The change in the correction for the response of silicon for the different effective x-ray energies was only about two percent and was ignored in the results.

TABLE I - FAXITRON DOSE

V(Kv)	E(KeV)	DOSE (RAD)
80	36	483
90	38	612
100	40	755
110	42	914
120	44	1087

The parts which will be exposed are found on drawings 3562102 and 3569800. All the active parts including two hybrids use bipolar technology which should not suffer any noticeable change at the dose level of a thousand rads.

Melvin Reier

APPENDIX

DOSERATE MEASUREMENTS AT THE REAL TIME X-RAY FACILITY

ABSTRACT

Measurements were made with thermoluminescent detectors (TLD) to determine the doserate (Rads (Si)/min) at numerous locations at the real time x-ray facility at an accelerating potential of 100kv. The results and the approach used will be described below.

The real time x-ray facility has been used extensively to locate flaws resulting from manufacturing defects in such commonplace items as printed circuit boards, integrated circuits, switches, etc. Since many IC types can be damaged by exposure to moderately low levels of ionizing radiation such as x-rays, a series of measurements was undertaken to map the radiation field in the vicinity of the x-ray tube.

To determine the doserate experimentally and relate it to solid-state devices the detector must have a response similar to silicon at the energies of interest. If not, a correction must be made for any difference. At the very low x-ray energies produced by a 100kv electron beam incident on a tungsten target the photoelectric effect in silicon dominates the response function. It rises rapidly as the x-ray energy is reduced. Since the x-ray spectrum varies smoothly from zero to the energy of the incident electrons and the photoelectric effect is a very sensitive function of the energy, it is essential to determine the effective energy of the spectrum unless one has a detector which has the same response as silicon. One method is to expose TLD's which have vastly different response functions at low energy. The ratio of their response (after normalizing them at 1.25 Mev using cobalt-60 where the photoelectric effect is insignificant) yields directly the effective energy of the x-ray beam at the accelerating voltage.

The response of silicon can then be interpolated or extrapolated from the two measurements.

A calibration of a TLD is made at 1.25 Mev using the GR9M cobalt-60 source which had been previously calibrated in terms of a source of known intensity at the Bureau of Standards. Combining the calibration at 1.25 Mev and the method outlined above, an absolute doserate at the effective x-ray energy can be determined. This method, which was tried initially, proved unsuccessful for the following reason. The two TLD's used were 30 percent LiF in teflon and 5 percent CaF_2:Mn in teflon. Although CaF_2:Mn has a photon effective atomic number of 16.3 and LiF one of 8.2 (Ref. 1), the response of the ones actually used was very similar because of the large amount of teflon in the TLD's. This would cause a large error in the ratio of their response at low energies, resulting in an unacceptably large error in the determination of the desired doserate for silicon.

In view of this an analytical approach was used to calculate the effective x-ray energy and the response of silicon at that energy. Ulrey (Ref. 2) measured the x-ray spectrum from a tungsten target at several accelerating potentials up to 50kv. He found that, to a high degree of accuracy, $\lambda_{max} V^{1/2} = \text{const}$, where λ_{max} is the x-ray wavelength at maximum intensity and V is the anode potential. His spectrum at 50kv was replotted as intensity vs. x-ray energy. The data are shown in Table I.

TABLE B-1

X-RAY SPECTRUM FROM A 50 KV ELECTRON SOURCE ON TUNGSTEN

λ (10^{-8}cm)	E (kev)	Intensity
.25	49.5	0
.28	44.2	3.7
.32	38.7	7.3
.4	30.9	11.7
.47 (max)	26.3	12.5
.44	28.1	12.4
.52	23.8	12.
.6	20.6	9.8
.7	17.7	6.7
.8	15.5	4.1
.9	13.8	2.5
1.	12.4	2

A numerical integration was performed to yield $\bar{E}$, which we define as the effective energy. The calculated value was 1.08 E_{max}. It was assumed that the relation, $\lambda_{max} V^{1/2} = const$, which was valid to 50kv could be applied at 100kv and that although the wavelength at peak intensity varied according to the above relation, the shape of the spectrum at 50kv is the same as that of 100kv. Therefore, E_{max} could be calculated at 100kv from the data at 50kv and the same factor, 1.08, used to calculate $\bar{E}_{100}$. The value for $\bar{E}$ at 100kv is 40 kev.

The response of numerous TLD's at different energies has been calculated by Bassi (Ref. 3). The value for silicon (Z=14) was interpolated between Z_{eff} = 15.3 ($CaSO_4$) and 10.2 (Al_2O_3). The ratio of the silicon response to that LiF (70 percent teflon) used in our measurements was 6.74. This factor multiplies all the x-ray data taken with LiF TLS's which were previously calibrated using the GR9M source.

Data were taken at various distances perpendicular to the direction of the electron beam (X axis). At each distance measurements were made in the direction of the shield door (Y axis) and in the vertical direction (Z axis) above the X axis. The TLD's were wrapped in a lucite sandwich to ensure electron equilibrium and mounted on an aluminum strip which was held in a clamp during the irradiation. (Absorption of x-rays by the lucite reduced the doserate by about one percent.) Very sharp drops in exposure in the Y or Z direction are due to shielding by the source. Occasional anomalies where the value at Y=0 was slightly less than at Y=3 in. can probably be attributed to partial shielding of the TLD at Y=0 by the clamp. All measurements were made at 100kv, 40 μ A and a bias of about 80V. The results are shown in Table II.

The largest source of uncertainty is the calibration of the TLD's which is good to about 20 percent. Other errors such as TLD placement would increase this to about 25 percent. A systematic error in the analytical approach to estimate the effective x-ray energy cannot be disatrous. If the effective x-ray energy is 60 instead of 40 kv, the factor multiplying the LiF data would be 5 instead of 6.74.

Although data were not taken at any other accelerating potentials, the doserate at other x-ray voltages may be inferred from the values at 100kv.

The total bremsstrahlung energy is proportional to the square of the accelerating voltage (Ref. 4). Although we cannot use this relation directly with the results at 100kv since the effective x-ray energy also changes with electron voltage ($\bar{E}_{100}$ = 40 kev, $\bar{E}_{80}$ = 36 kev), we can derive a fairly good estimate at some other accelerating voltage from the 100kv data.

REFERENCES

1. "Thermoluminescent Dosimetry" by A.F. McKinlay. Adam Hilger, Bristol, England, 1981, p. 36.

2. C.T. Ulrey, Phys. Rev 11 410 (1918).

3. P. Bassi et al, Inter. J Appl Radiation and Isotopes 27, 291 (1976).

4. "The Atomic Nucleus" by R.D. Evans. McGraw-Hill 1955. p. 615

TABLE B-II

X-Ray Doserates

X (in.)	Y (in.)	Z (in.)	Doserate (Rads (Si)/min)
1.5	0	0	499
1.5	1.5	0	156
1.5	3.0	0	2
1.5	0	0	453
1.5	0	1.5	5
1.5	0	3.0	.2
4.0	0	0	85
4.0	3.0	0	24
4.0	6.0	0	1
4.0	9.0	0	.2
4.0	0	0	123
4.0	0	3.0	.4
6.0	0	0	98
6.0	3.0	0	74
6.0	6.0	0	2
6.0	9.0	0	.4
6.0	0	0	57
6.0	0	3.0	2
10.0	0	0	32
10.0	3.0	0	37
10.0	6.0	0	30
10.0	9.0	0	2
10.0	0	0	26
10.0	0	3.0	39
14.0	0	0	11
14.0	3.0	0	13
14.0	6.0	0	16
14.0	9.0	1	11
14.0	0	0	15
14.0	0	3.0	20
18.0	0	0	12
18.0	3.0	0	11
18.0	6.0	0	11
18.0	9.0	0	9
18.0	0	0	11
18.0	0	3.0	11

APPENDIX C

COVER PAGES OF FAILURE VERIFICATION AND FAILURE ANALYSIS REPORTS

FVR No. 4868
ERFM
Page 1

FAILURE VERIFICATION REPORT

DATE OF RECEIPT	10/25/88	COMPONENT	ERFM Module
REQUESTER	D. W. Buechler ORG 76-41-22	FUNCTION/TYPE	
PHONE	64650 BLDG/MS E1/C132	MFR	
FAILURE REFERENCE	None	MFR P/N	
FAILURE DATE	CIRCUIT SYMBOL	HUGHES P/N	3562102
GLA/TSER	420169-31 (BK1G141B1A)	DATE CODE	S/N 1015

REPORTED FAILURE

The subject module was a field failure. The failure was isolated to device U2414 on the circuit board. Visual examination had revealed mechanical damage to pin 15 of U2414.

BACKGROUND INFORMATION

The device was a 54S174 (HEX D flip-flop). Pin 15 is the Q5 output.

RESULTS OF ANALYSIS

Electrical Measurements.

Initial probing measurements were unsuccessful because a conformal coating was present on the device and leads. The conformal coating was scraped from leads 8, 10, 12, 15 and 16 to facilitate electrical contact with probes.

Electrical probing using the Tektronix 576 transistor curve tracer verified that pin 15 was electrically open between the Q5 output and the connection on the circuit board. Additional measurements by probing between the output and ground and between the output and V_{cc} indicated that the semiconductor junctions at the Q5 output (pin 15) were intact. This was further verified by comparison with outputs Q3 (pin 10) and Q4 (pin 12).

CONCLUSION

The failure of U2414 was verified and found to be due to the mechanical damage to the lead at pin 15. All measurements indicated that the Q5 output (pin 15) was functional except for the open caused by the break in the external lead.

Peter G. Backes	N6526	D. H. Van Westerhuyzen	11/1/88	
ANALYST	JOURNAL	APPROVAL	DATE	
P. G. Backes		D. H. Van Westerhuyzen		

AR No. 10963
Program ERFM
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FAILURE ANALYSIS REPORT

DATE OF RECEIPT 5/2/88	TSD PROJECT ENGINEER
REQUESTER D. W. Buechler	
ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132	PHONE BLDG./MS
REA PHONE	GLA/TSER 400524-31 (BK1G141B1A)
COMPONENT Hybrid	FAILURE REFERENCE None
FUNCTION/TYPE Negative Voltage Regulator	DATE OF FAILURE
GENERIC P/N	FAILURE LEVEL Field
HUGHES P/N 934268	LOT NUMBER
MFG. Solitron P/N	CIRCUIT SYMBOL
DATE CODE 8142 S/N 44	MODULE S/N

ABSTRACT

The reported failure, did not regulate, was verified. In extensive testing in three different test fixtures, the hybrid exhibited widely different and inconsistent behavior. Characteristics of the regulator transistors Q1 and Q2 were observed to shift with time. All the irregular behavior disappeared after a 2 hour 125°C bake. This and the observation that the hybrid was optically very dirty led to the conclusion that the device had mobile ionic contamination.

Since this type of contamination can occur from improper assembly, and it can cause variation in device behavior with time and voltage, and since both of these conditions were observed to be present, it was concluded that the device was a primary failure due to improper assembly.

TECHNICAL COMMENTARY
☒ NOT REQUIRED
☐ APPENDED
Thomas

Z C Richardson Jr — FAILURE ANALYST — Z. C. Richardson, Jr.

N7449-21 — JOURNAL

D. H. Van Westerhuyzen — APPROVAL — D. H. Van Westerhuyzen

5/10/88 — DATE

18175 EDSG MAR 85

FAILURE ANALYSIS REPORT

DATE OF RECEIPT 7/7/88	TSD PROJECT ENGINEER
REQUESTER D. Buechler	
ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132	PHONE BLDG./MS
REA PHONE	GLA/TSER 400652-31 (BK1G141B1A)
COMPONENT Integrated Circuit (2)	FAILURE REFERENCE None
FUNCTION/TYPE ROM/Line Driver	DATE OF FAILURE 7/7/88
GENERIC P/N	FAILURE LEVEL
HUGHES P/N 932820-218/3562102	LOT NUMBER
MFG. P/N 26LS31	CIRCUIT SYMBOL U1101/U1408
DATE CODE 7928/8446DPP S/N 1003	MODULE 3562102 S/N 1003

ABSTRACT

A 932489 quad line driver and a 932820-218, 1024 bit read-only memory (ROM) were submitted for failure analysis. The latter passed the electrical test, which included logical contents, timing parameters, and input and output signals. In the case of the former the reported failure, short to ground, was verified and it was determined that the failure was secondary and was due to an electrical overstress of output A.

TECHNICAL COMMENTARY

☒ NOT REQUIRED

☐ APPENDED

Thomas

Rakin Asatourian — FAILURE ANALYST — R. K. Asatourian

L1252 — JOURNAL

D. H. Van Westerhuyzen — APPROVAL

9/13/88 — DATE

8175 EDSG MAR 85

FAILURE ANALYSIS REPORT

DATE OF RECEIPT 7/7/88

REQUESTER D. W. Buechler

ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132

REA _____ PHONE _____

TSD PROJECT ENGINEER _____

PHONE _____ BLDG./MS _____

GLA/TSER 400653-31 (BK1G141B1A)

COMPONENT Module

FUNCTION/TYPE Negative Voltage Regulator

GENERIC P/N _____

HUGHES P/N 934268-501B

MFG. Solitron P/N _____

DATE CODE 8108 S/N 124

FAILURE REFERENCE FVR 4860

DATE OF FAILURE 6/'88

FAILURE LEVEL Module

LOT NUMBER _____

CIRCUIT SYMBOL U2

MODULE 3569800 S/N 300

ABSTRACT

The reported failure, the output voltage of the hybrid (U2) is -12.58 volts D.C. when it should have been -12.0 ± 0.25 volts D.C., was verified. The analysis indicated that the hybrid failed due to the V_{09} and V_{011} output voltages being out of tolerance because the 2.5 Kohms ± 1% resistor between pins 21 and 24 was out of tolerance. The cause of the resistance being out of tolerance and changing during the baking of the hybrid is believed to be due to contamination too subtle to detect since no obvious physical defects were noted during the internal examination. The hybrid may have been contaminated during manufacturing since it passed the hermetic seal tests.

The parallel resistance noted between the base and emitter of the output transistor did not appear to be related to the reported failure.

The failure of the hybrid is judged to be primary.

TECHNICAL COMMENTARY

☒ NOT REQUIRED

☐ APPENDED Sternberg

Sergio B. Lopez
FAILURE ANALYST
S. B. Lopez

N7447
JOURNAL

D. H. Van Westerhuyzen
APPROVAL
D. H. Van Westerhuyzen

10/10/88
DATE

18175 EDSG MAR 85

FAR No. 10982
Program ERFM
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FAILURE ANALYSIS REPORT

DATE OF RECEIPT 7/7/88

REQUESTER D. Buechler

ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132

REA _____ PHONE _____

TSD PROJECT ENGINEER _____

PHONE _____ BLDG./MS _____

GLA/TSER 400654-31

COMPONENT Integrated Circuit

FUNCTION/TYPE Line Driver/High Speed, Quad

GENERIC P/N 26LS31

HUGHES P/N 932849-1B

MFG. Advanced Micro Devices P/N AM26LS31/BFA

DATE CODE 8446DPP S/N _____

FAILURE REFERENCE None

DATE OF FAILURE May 1988

FAILURE LEVEL Module

LOT NUMBER _____

CIRCUIT SYMBOL U1101

MODULE 3562102 S/N 1030

ABSTRACT

The reported failure at the module level was a probable short between output pin 2 of U1101 and V_{CC}. Probe measurements to the U1101 integrated circuit while still connected to the board verified the reported failure. The results were documented in Failure Verification Report (FVR) No. 4857. After desoldering pin 2 of U1101, pin 2 was found to be shorted to the ground pin.

After U1101 was removed from the board electrical testing indicated pin 2 was shorted to pin 8 (ground) through 890 ohms and to pin 16 (VCC) through 4,7000 ohms. Internal examination revealed evidence of electrical overstress at the pin 2 output transistor. The probable cause of failure appears to have been a large voltage at pin 2 with respect to ground which exceeded the collector-emitter breakdown voltage of the pin 2 output transistor.

The failure is considered to be secondary - cause relating to events external to the IC.

TECHNICAL COMMENTARY

☒ NOT REQUIRED

☐ APPENDED

J. L. Walker — FAILURE ANALYST

N7442 — JOURNAL

D. H. Van Westerhuyzen — APPROVAL

7/14/88 — DATE

18175 EDSG MAR 85

FAR No. 10985
Program ERFM

FAILURE ANALYSIS REPORT

DATE OF RECEIPT 8/5/88

REQUESTER D. W. Buechler

ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132

REA _____ PHONE _____

TSD PROJECT ENGINEER _____

PHONE _____ BLDG./MS _____

GLA/TSER 420040-31 (BK1G141B1A)

COMPONENT Hybrid

FUNCTION/TYPE Voltage Regulator

GENERIC P/N _____

HUGHES P/N 934268-501B

MFG. HAC P/N _____

DATE CODE _____ S/N 4607

FAILURE REFERENCE None

DATE OF FAILURE _____

FAILURE LEVEL Module

LOT NUMBER _____

CIRCUIT SYMBOL _____

MODULE _____ S/N _____

ABSTRACT

The exact reported failure, regulates at -2 V was not confirmed, but the device was found to fail by regulating at -15 V. The output voltage should be -12 ± 0.25 V. The device behavior varied with time and temperature. The device functioned correctly, then it failed, then it was restored to functionality by baking. This behavior pattern is typical of mobile ionic contamination. Since only one transistor's characteristics were observed to change and that the transistor was covered with anomalous spots, it was concluded that transistor probably had been contaminated during fabrication of the transistor. The hybrid failure was primary due to improper fabrication of one of the transistors in it.

Although the exact reported failure was not directly verified, the failure was considered verified since mobile ionic contamination can cause rapid and wide variation in transistor behavior.

TECHNICAL COMMENTARY

☒ NOT REQUIRED

☐ APPENDED

Thomas

Z. C. Richardson, Jr. — FAILURE ANALYST

N7449-60 — JOURNAL

D. H. Van Westerhuyzen — APPROVAL

8/29/88 — DATE

FAR No. 10994
~~Program~~ ERFM

FAILURE ANALYSIS REPORT

DATE OF RECEIPT 9/2/88
REQUESTER D. W. Buechler
ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132
REA _____ PHONE _____

TSD PROJECT ENGINEER J. Kallis
PHONE _____ BLDG./MS _____
GLA/TSER 420093-31 (BK1G141B1A)

COMPONENT Hybrid Circuit
FUNCTION/TYPE Positive Voltage Regulator/Hybrid
GENERIC P/N _____
HUGHES P/N 934266-501B
MFG. Hughes P/N 1040509-1
DATE CODE _____ S/N 2476

FAILURE REFERENCE None
DATE OF FAILURE 8/9/88
FAILURE LEVEL Field Failure
LOT NUMBER _____
CIRCUIT SYMBOL U1
MODULE 3569800 S/N 127

ABSTRACT

The reported failure, would not power up at cold temperature, was not verified. All testing at room temperature and at cold temperature indicated the device was electrically good. Internal examination did not reveal any defect. The results of the analysis indicated the device was not a failure.

TECHNICAL COMMENTARY
☒ NOT REQUIRED
☐ APPENDED
Sternberg

J. L. Walker — FAILURE ANALYST
N7442 — JOURNAL
D. H. Van Westerhuyzen — APPROVAL
11/88 — DATE

FAR No. 10995
Program ERFM
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FAILURE ANALYSIS REPORT

DATE OF RECEIPT 9/2/88	TSD PROJECT ENGINEER
REQUESTER D. W. Buechler	
ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132	PHONE BLDG./MS
REA PHONE	GLA/TSER 420094-31 (BK1G141B1A)
COMPONENT Integrated Circuit	FAILURE REFERENCE None
FUNCTION/TYPE 4 BIT Counter	DATE OF FAILURE
GENERIC P/N 54LS163A	FAILURE LEVEL Board Level Field Failure
HUGHES P/N 932756-1B	LOT NUMBER
MFG. Fairchild P/N	CIRCUIT SYMBOL U2410
DATE CODE 8550J S/N	MODULE 3562102 S/N 1010

ABSTRACT

The reported failure mode, no output on pin 15, was verified. Pin 15 was found to have incorrect breakdown voltages, which indicated an electrical anomaly. The output transistor for pin 15 was shorted to another transistor because an area of necessary oxide insulation was missing. This short prevented correct transistor action and resulted in no output. This was a primary failure.

TECHNICAL COMMENTARY
☒ NOT REQUIRED
☐ APPENDED
Sternberg

Z. C. Richardson, Jr. — FAILURE ANALYST
N7449-88 — JOURNAL
D. H. Van Westerhuyzen — APPROVAL
10/7/88 — DATE

18175 EDSG MAR 85

FAR No. 11002
Program ERFM
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FAILURE ANALYSIS REPORT

DATE OF RECEIPT 9/20/88
REQUESTER D. W. Buechler
ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132
REA _____ PHONE _____

TSD PROJECT ENGINEER _____
PHONE _____ BLDG./MS _____
GLA/TSER 420123-31 (BK1G141B1A)

COMPONENT Hybrid Circuit
FUNCTION/TYPE Negative Voltage Regulator
GENERIC P/N _____
HUGHES P/N 934268-501B
MFG. Hughes P/N _____
DATE CODE 8202 S/N 209

FAILURE REFERENCE FVR 4865
DATE OF FAILURE 9/20/88
FAILURE LEVEL Board
LOT NUMBER _____
CIRCUIT SYMBOL U2
MODULE 3569800 S/N 502

ABSTRACT

The reported failure, output voltage too low, was verified. The output level in testing on the board was -2.3V. Testing after removal from the board indicated that the 2.5 Kohm ± 1% resistor from pin 21 to ground was 2.1 Kohm. This should cause the hybrid to regulate at about -16V, and it was observed to regulate at -16.5V. It was concluded that there may be a testing error or an additional anomaly on the board that loaded the output to the -2.3V value.

The value of the anomalous resistor was not changed by baking at 125°C for 2 hours. This implies that the change was not caused by moisture. It is possible that the laser cuts in the thick film resistor may have healed. No cracks were observed in the thick film resistor.

The failure was due to an apparent drift in the value of the 2.5 Kohm thick film resistor. This drift was believed to be due to aging, but the exact cause of the drift was not found.

TECHNICAL COMMENTARY
[X] NOT REQUIRED
[ ] APPENDED
Steinberg

Z. C. Richardson, Jr. — FAILURE ANALYST
N74-25 — JOURNAL
D. H. Van Westerhuyzen — APPROVAL
10/13/88 — DATE

Z. C. Richardson, Jr.
D. H. Van Westerhuyzen

18175 EDSG MAR 85

AR No. 11033
rogram ERFM
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FAILURE ANALYSIS REPORT

DATE OF RECEIPT 12/16/88

REQUESTER D. W. Buechler

ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132

REA _____ PHONE _____

TSD PROJECT ENGINEER _____

PHONE _____ BLDG./MS _____

GLA/TSER 420230-31 (BK1G141B1A)

COMPONENT Hybrid

FUNCTION/TYPE Positive Voltage Regulator

GENERIC P/N _____

HUGHES P/N 934266-501B

MFG. Solitron P/N _____

DATE CODE 8035 S/N 037

FAILURE REFERENCE FVR 4869

DATE OF FAILURE 10/25/88

FAILURE LEVEL _____

LOT NUMBER _____

CIRCUIT SYMBOL U1

MODULE 3569800 S/N 482

ABSTRACT

The reported failure mode, shorted, was not verified. Neither of the reported shorts was verified. The device passed testing at room and at high temperature, and a 0.5 amp load test. The device was considered not to be a failure.

TECHNICAL COMMENTARY

☒ NOT REQUIRED

☐ APPENDED

Sternberg

Z. C. Richardson, Jr. — FAILURE ANALYST

N7449-133 — JOURNAL

D. H. Van Westerhuyzen — APPROVAL

1/12/89 — DATE

Z. C. Richardson, Jr.

D. H. Van Westerhuyzen

18175 EDSG MAR 85

AR No. 11053
Program ERFM
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FAILURE ANALYSIS REPORT

DATE OF RECEIPT 2/22/89	TSD PROJECT ENGINEER
REQUESTER D. W. Buechler	PHONE BLDG./MS
ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132	GLA/TSER 420379-31 (BK1G141B1B)
REA PHONE	
COMPONENT Hybrid	FAILURE REFERENCE None
FUNCTION/TYPE Voltage Regulator	DATE OF FAILURE
GENERIC P/N	FAILURE LEVEL
HUGHES P/N 934268-501B	LOT NUMBER
MFG. Solitron P/N	CIRCUIT SYMBOL U2
DATE CODE 8128 S/N 032	MODULE S/N

ABSTRACT

The reported failure, output drift, was verified. The hybrid (P/N 934268) had failed previously on a power supply module that was submitted for a failure verification (FVR 4906). The output of the hybrid dritted during the first hour of continuous operation at room temperature before stabilizing at -12 volts. Further attempts to reproduce the failure with functional electrical tests at elevated temperatures and temperature cycling were unsuccessful. The device passed PIND and hermeticity tests but failed a residual gas analysis (RGA) with a water content within the package of 15,000 parts per million. The internal visual examination and nondestructive internal wire bond strength tests did not reveal any anomalies. This was believed to be a primary failure.

The observed output drift may have been caused by condensation and subsequent evaporation of the excess water within the hybrid package.

TECHNICAL COMMENTARY
☒ NOT REQUIRED
☐ APPENDED
Sternberg

K. Scott — FAILURE ANALYST

N8016 — JOURNAL

Z. C. Richardson, Jr. — APPROVAL

4 May 89 — DATE

18175 EDSG MAR 85

AR No. 11079
Program ERFM
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FAILURE ANALYSIS REPORT

DATE OF RECEIPT 7/17/89
REQUESTER D. W. Buechler
ORG 76-41-22 PHONE 64650 BLDG./MS E1/C132
REA _____ PHONE _____

TSD PROJECT ENGINEER _____
PHONE _____ BLDG./MS _____
GLA/TSER 420595-31 (BK1G141B1B)

COMPONENT Integrated Circuit
FUNCTION/TYPE HEX Inverter
GENERIC P/N 54S04
HUGHES P/N JM38510/07003
MFG. Signetics P/N _____
DATE CODE 7841 S/N 593

FAILURE REFERENCE FVR 4913
DATE OF FAILURE June 1989
FAILURE LEVEL Field
LOT NUMBER _____
CIRCUIT SYMBOL U2213
MODULE 3562102 S/N _____

ABSTRACT

The reported failure of this device, pin 8 shorted to ground, was not verified in the failure analysis. Instead the ground bond wire was found to be melted open.

The ground connection was intact at the time of the failure verification. Based on the results of this analysis, it was concluded that the pin 7 ground bond wire was melted open probably due to a reverse current between the time of the failure verification and the time of this failure analysis. This failure is believed to be independent of the reported pin 8 to ground short.

Although the original reported failure of this device, pin 8 shorted to ground, was not verified in the failure analysis, close proximity of the pin 8 bond wire and an unpassivated area of the ground metallization suggests a possible intermittent conductive particle short. The device passed the PIND test, but particles were found adhering to the edge of the die that were large enough to bridge the gap between the underside of the pin 8 bond wire and unpassivated aluminum ground metallization. Possibly these or other particles caused an intermittent short that was observed during the original failure and during the failure verification. Such a small clearance between the output bond wire and the bare ground metallization when accompanied by loose conductive particles has been found to be a source of failure in other devices in the past.

TECHNICAL COMMENTARY
☒ NOT REQUIRED
☐ APPENDED
Sternberg

Peter G. Backes N7909
FAILURE ANALYST JOURNAL
P. G. Backes

D. H. Van Westerhuyzen 8/16/89
APPROVAL DATE
D. H. Van Westerhuyzen

18175 EDSG MAR 85

HOLOGRAPHIC INTERFEROMETRY OF ELECTRONIC MODULES

FINAL REPORT

Presented To:

Mr. Daniel Buechler
HUGHES AIRCRAFT COMPANY
Electro-Optical and Data Systems Group
P.O. Box 902
Building E1, M/S C132
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Presented By:

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Suite 108
Irvine, California 92714
Telephone (714) 553-0688

PURCHASE ORDER NUMBER M9-317647-KKD

November 30, 1990

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SECTION I

INTRODUCTION

This final report describes work completed during the period 1 May 1989 to 31 October 1990 under Purchase Order No. M9-317647-KKD. This work involved the nondestructive inspection by holographic interferometry (HI) of two digital timing and control modules and two analog linear regulator modules from the APG-63 radar used in the F-15 aircraft. These tests were conducted to determine the bond quality of the heat exchangers (HE) and printed wiring boards (PWB) that make up the modules. The holographic examinations performed on the individual HEs and PWBs prior to manufacturing the modules assessed the quality of the PWB laminations and the HE surface sheet-to-cooling fin bonds. Then, after mating of the PWBs to their respective HEs, the effects of various manufacturing processes upon the quality and integrity of these bonds was periodically evaluated.

This program was initially organized into eight tasks. Tasks 1 involved calibration, Tasks 2 through 7 involved HI testing, and Task 8 was the production of the final report. However, after the completion of Task 1, it was decided that a second calibration task was needed (this decision is discussed later in the report), and this new calibration task was designated Task 8 so that the task involving the production of the final report would be the highest numbered task (i.e., Task 9 under the revised program organization). Therefore, the final organization of the program was as follows, with the tasks listed in the order of completion:

Task	Function	Description
1	Calibration	First HI calibration study
8	Calibration	Second HI calibration study
2	Test	HI evaluation of four HEs and six PWBs
3	Test	HI evaluation of PWB to HE bonds before the surface mounting of static sensitive components
4	Test	HI evaluation of PWB to HE bonds after the surface mounting of static sensitive components
5	Test	HI evaluation of PWB to HE bonds after module conditioning
6	Test	HI evaluation of PWB to HE bonds after power-on screening
7	Test	HI evaluation of PWB to HE bonds after system burn-in
9	Final report	

Interim documentation was provided at the conclusion of Tasks 1 through 8 in the form of 1) a written summary of experimental procedures, results, and conclusions, and 2) a narrated 1/2 inch VHS video tape providing a complete audio/visual record of all tests. The video documentation ranged in length from approximately 30 to 70 minutes, depending on the specific task.

This report briefly discusses nondestructive HI in general and describes the tests chosen for use in this study. The equipment and fixturing are then described, including the types of stressing used. The results of each task of the program are then described in detail. Finally, a summary of the program is presented, and conclusions are discussed.

SECTION II

BACKGROUND

A. General Considerations

Holography is an optical recording process whereby a recording (called a hologram) is created by the interference of two laser beams at a photographic plate or other recording medium(Figure D-1). One beam, the reference beam, comes directly from the laser to the film, while the other, the object beam, is scattered from the object itself. Later, when the processed hologram is illuminated by the reference beam alone, the hologram creates light waves which are identical to the light waves scattered from the original object. These waves are responsible for the image the viewer perceives in the hologram.

The ability of holography to recreate 3-dimensional scenes makes it possible to apply interferometry to 3-dimensional objects. Using this process, light rays recorded in the holographic recording medium can be made to interfere with light rays from the real object, generating a set of contour lines, or fringes. These interference fringes are a measure of the amount of surface deformation between the object as initially recorded and the object recorded at a later time. This deformation may be due to minute mechanical, thermal, or environmental stress. HI is thus a precise way to determine how the surface of an object responds when minute stresses are applied.

A powerful feature of holographic interferometry is that information is obtained over the surface of a test object rather than at just a point. The hologram can clearly show those areas of an opaque test object where dimensional changes are occurring. Surface anomalies, or flaws, create abnormal or ambiguous effects in the fringes and are usually obvious even to an untrained viewer. A flaw uncovered using HI can be analyzed if its effect on the surface is understood, and it can be located accurately if its effect on the surface is localized. For holographic inspection to work, the deformation of the surface must be abrupt and must have an amplitude of about 0.05 microns (about one tenth the wavelength of light) or greater. A good candidate is honeycombed material in which the flaw is a debond between the surface and the honeycomb material beneath. If such a surface is holographically recorded and then mechanically stressed, the surface near the debonded region will generate many interference fringes when a second hologram is superimposed on the first.

During the calibration phase of this program (Task 1), various types of holographic interferometry were tested and two types were chosen for this study:

1) **Real-time Holography** - This technique allows the instantaneous, continuous monitoring of dimensional changes resulting from applied stresses by viewing a holographic image of the part superimposed on itself. In the present study, a hologram was created of the part being tested while the part was either unstressed, or was in a baseline stress condition. Then, while viewing the original part through the hologram using a video camera, a stress was applied, or an existing stress was altered. The resulting fringe pattern, due to the deformation of the surface of the part, was monitored continuously for the possible appearance of anomalies indicating underlying flaws. The image thus seen was recorded continuously on a video casette recorder (VCR).

2) **Time-average Holography** - This technique produces a hologram which is made while a component is vibrationally driven at resonance. A visual image of the vibration pattern, or modal map, is obtained. In simplest terms, the nodes, which are stationary, produce a bright recording, and the parts which move "wash out" and do not produce a bright hologram. The VCR is used here also, but only to view the frozen reconstructed image of the part.

Other types of holography were tested (for example, multiple exposure holography) but were judged inappropriate for this program.

B. Sensitivity Enhancement

A variety of sensitivity enhancement procedures were examined. Two were adopted for use in this study:

1) **Phase Shift Interferometry**: With this technique, the fringes are moved slowly by introducing a time varying path length change into either the object or reference wave. This was accomplished here by tilting a parallel glass plate in the object wave. The tilt was achieved by a motor driven mount that cycles the plate through a few degrees before returning to the beginning position. Fringes that move over a defect enhance the appearance of the defect, since time varying changes in a fringe are more easily perceived by a human operator. A defect will often manifest as a "blinking" region where the defect appears to flash on and off. Consequently, a defect which might otherwise have been lost in the overall fringe pattern and background noise can become obvious to the inspector. In fact, phase shifting provides a more accurate location of fringes even when machine vision is in use. The movement of the fringes actually adds information.

2) **Beam Tilt Correction**: If the test object has undergone rigid body motion (i.e., a simple tilt out-of-plane) not exceeding a few tens of microns during the stressing operation, then this motion can be compensated by tilting the plane of one of the images being compared in the interferogram so that it more accurately overlaps the other image. This was achieved by using a tilt plate (an optical-quality glass plate of approximately 10 mm thickness) introduced into the object beam. During reconstruction, when the image from the reference hologram was interfered with the image from the live test object itself, moving the tilt plate optically tilted the test object. The tilt plate was adjusted to minimize the number of fringes observed in the interferogram.

C. Electronic Hardware Supplied by Hughes Aircraft Co.

The HEs examined in this study were constructed by Hughes by bonding two thin metal sheets to a series of heat conducting fins to form channels to accommodate the flow of cooling air. Two of the four HEs were approximately 5 inches wide by 6 inches in length and the other two were approximately 5 inches wide by 10 inches in length. All heat exchangers were approximately 0.125 inches thick.

The PWBs examined in this study were of two types:

1) **5 inch by 5 inch**: These PWBs were composed of two layers of epoxy-impregnated glass cloth with conductive copper traces on each side of each layer, forming four distinct layers of circuitry. During this program, two PWB/HE modules were built by Hughes, each consisting of one 5 inch by 5 inch PWB bonded to one side of a HE.

2) **5 inch by 9 inch**: These PWBs were composed of seven layers of polyimide-impregnated glass cloth with conductive copper traces on each side of each layer, forming 14 distinct layers of circuitry. During this program, two PWB/HE modules were built by Hughes, each consisting of 5 inch by 9 inch PWBs bonded to each side of a HE (i.e., a total of four PWB bonded to two HEs).

During Task 3, the six PWBs were bonded to the four HEs to form two digital timing and control modules (with two PWBs per HE) approximately 5 inches wide by 10 inches long, and two analog linear regulator modules (with only one PWB per HE) approximately 5 inches wide by 6 inches long.

D. Stress Methods

The identification of a defect using HI will be successful only if the defect can be induced to cause a surface deformation when stressed. Thus, the placement and the distribution of the stressing energy may be critical to the detection of the flaw, and the choice of a stressing method is often as important as the choice of a holographic inspection technique. Fortunately, there are several good methods for making subsurface defects visible under holographic scrutiny, including thermal, vibrational, and pressure-induced stressing methods:

1) **Thermal Stressing** - This method involves raising or lowering the temperature of the part to induce a thermal expansion or contraction. Voids, delaminations, or debonds below the surface will exhibit different rates of heat transfer resulting in different rates of thermal expansion or contraction than the surrounding material, producing visible anomalies in the interferometric fringe pattern. This stressing method is not compatible with time-average holography.

2) **Vibrational Stressing** - This method involves vibrating the part at a frequency which will excite at resonance the surface over the underlying defect, while leaving the bulk of the part relatively unperturbed. At resonance, this results in a dark image over the defect superimposed on the part. This stressing method can be used with both real-time and time-average holography.

3) **Pressure Stressing** - This method involves raising or lowering the ambient pressure surrounding the part being tested. This can create a pressure differential throughout the part (often a few tens of millibars is sufficient) causing a deformation of the surface overlying a defect which is different from the deformation of the surrounding area, resulting in an anomalous fringe pattern over the defect. This stressing method is not compatible with time-average holography.

E. Holographic Interferometry Test Equipment

All HI measurements performed in this study were made at the Newport Corporation facilities in Fountain Valley, California. Initial measurements were made with a Newport Model HC-1034 Holography Workstation using a 35 mW HeNe laser. However, the bulk of the measurements were made on a Newport Model HL-3 Holography Workstation modified to contain a three watt Lexel Model 95 argon-ion laser operating at a wavelength of 514.5 nm. On both workstations, holograms were recorded on a Newport Model HC-301 Thermoplastic Plate. Using this device, holograms can be generated in about 20 seconds, and 300 or more holograms can be made on the same thermoplastic plate. Because the holograms were produced in-place (i.e., the thermoplastic plate was not removed from the

workstation), the thermoplastic plate was very easy to use with real-time and time-average holography. Object and reference beam ratios were determined using a Newport Model HC-302 Detector. Video images of the holographic interferograms were recorded on 3/4 inch video tape with a Javelin Spectar video camera, and were transcribed to 1/2 inch video tape at the conclusion of each work day.

The equipment used to implement the stressing methods discussed in the previous section are as follows:

1) **Thermal stressing** of the HEs and PWBs was achieved by one or more of the following: 1) by hand (i.e., by lightly passing a hand over the surface of the test object), 2) with a laboratory heat gun, or 3) by using a flat foil heater (Minco Thermofoil Heater Model HK5182R52.9L12B) in contact with the back of a HE or PWB (described in more detail in the next section).

2) **Vibrational stressing** was achieved using a Newport Corporation Model HC-520 Shaker System capable of producing vibrational frequencies from 250 Hz to over 200 kHz, or random "white noise" over a specified frequency interval.

3) **Pressure stressing** was achieved using a one cubic foot vacuum chamber fitted with a one square foot glass window for viewing.

Phase shift interferometry was implemented experimentally using a Newport Corporation Model HC-602 Optical Compensator. Beam tilt correction was implemented using a Newport Corporation Model HC-605 Fringe Interpretation Accessory.

F. Fixturing Developed

To securely hold each HE and PWB and facilitate the use of specific stress methods, special fixturing was developed for this study. This fixturing consisted, in part, of a universal aluminum back plate (measuring 6 inches by 10.75 inches by 0.25 inches thick) which was rigidly attached to a Newport Corporation Shaker System Model HC-520 by a single 1/4-20 bolt. The Model HC-520 Shaker provided vibrational stressing, or provided a stable mounting platform for thermal and pressure stressing.

To facilitate vibrational stressing, the HEs and PWBs were attached to the universal back plate by four 1 inch aluminum standoffs using existing mounting holes on each test piece. Vibration was thus transferred from the back plate to the test piece via the standoffs. This 1 inch displacement of the back plate allowed the mounting of all HEs and PWBs, as well as all PWB/HE modules used in this program.

Thermal stressing involved either 1) the same fixturing as described above for vibrational stressing (when warming by hand or using a laboratory heat gun), or 2) additional fixturing developed for use with the flat foil Minco Thermofoil heater. The latter consisted of an aluminum support plate (with dimensions identical to the universal back plate) which was attached to the back plate with four 1 inch standoffs to provide rigid support. The HE or PWB being tested was clamped lengthwise to this support plate along opposing edges, with the Minco Thermofoil heater between it and the support plate. The Minco heater, with dimensions 5 inches by 10 inches by 0.20 inches thick, was supplied with an adhesive backing and was mated to a 5 inch by 10 inch piece of 1/32 inch thick silicon rubber gasket material. This insulated the heater from the support plate and provided the necessary flexibility to allow the flat heater to make good contact over the entire surface of the part being stressed.

Additional fixturing was developed to facilitate pressure stressing of the HEs. This fixturing consisted of two brackets fitted with 1/32 inch thick silicon rubber gaskets, which clamped and sealed the HEs at both ends to keep the interior of the part at one atmosphere pressure as the pressure surrounding the piece was reduced. These brackets attached to the universal back plate to provide a rigid mount for HI.

SECTION III

TASK 1 - CALIBRATION

This section will describe the procedures and results of HI testing of the calibration and sample HEs and the calibration PWBs performed in Task 1.

The calibration HE examined in Task 1 contained debonded areas where a portion of the outer metal sheet was not bonded to the underlying fins, as determined by an ultrasonic technique at Hughes prior to delivery of the calibration HE to MetroLaser.

The defects introduced into the calibration PWBs examined in Task 1 were to be made of photoresist material. These photoresist inclusions were to be placed on circuit layers 2 and 3 of the 5 inch by 5 inch board, and on circuit layers 2, 7, and 13 of the 5 inch by 9 inch board. These defects were arranged in a pattern consisting of a single isosceles triangle (1/2 inch by 1 inch) and a series of circular dots ranging in size from 0.050 inch to 1/2 inch. These defects covered a rectangular area 1/2 inch by 4 inches. The 5 inch by 5 inch calibration PWB had one such pattern on each of two layers, while the 5 inch by 9 inch calibration PWB had one pattern on each of three layers.

A. Experimental Procedures and Results - Heat Exchangers

Thermal Stressing

Using real-time HI, both the calibration and sample HEs were analyzed for the appearance of surface anomalies induced by thermal stressing. Thermal stressing was achieved by 1) lightly passing a hand over the mounted HE, 2) warming the surface with a laboratory heat gun, 3) blowing hot air through the interior channels of the HE with a heat gun, and 4) baking in an oven ($T \leq 120^{o}F$). The surface of each HE responded very visibly to each thermal stress method, but no debonds were detected in either piece. The high thermal conductivity of the metal surface resulted in a rapid conduction of heat away from the local area being stressed, so that large portions of the surface deformed relatively evenly. With the exception of the cases where stressing was induced by baking in an oven, the effect of the stressing method was observed with real-time HI via the video camera over the entire duration of the test, from the initial application of heat until the HE had cooled significantly. When heating in an oven, only the cool-down phase was observed and evaluated.

Using time-average HI, both the calibration and sample HEs were analyzed after baking in an oven. Again, no debonds were detected.

Because the thermal stressing just described did not reveal the presence of flaws known to exist in the calibration HE, an alternative thermal stressing technique was developed involving a flat foil Minco Thermofoil heater. This technique was intended to heat the back surface of the HE (i.e., the side not being analyzed for debonds) and to conduct heat to the front surface through the metal fins comprising the cooling channels. Areas of either surface directly over the debonds were expected to not conduct heat so that the corresponding areas on the front surface should expand more slowly than surrounding areas, resulting in fringe anomalies over the debonds.

The Minco Thermofoil heater used in this study (described in an earlier section) was capable of generating up to 24 watts per square inch, for a total power capability of slightly over 1 kilowatt. However, total power levels in this study never exceeded 270 watts into the 5 inch by 9 inch HEs. Note that only one side of the calibration HE could be heated by this

method. The reverse side of the calibration HE had mounting bosses which prevented contact of that surface with the flat Minco heater.

The test procedures used with the Minco heater involved 1) the choice of a total heater output power (via the choice of the voltage to the heater) spanning a range of 1.5 watts to 270 watts, and 2) the choice of a heating duration spanning a range from essentially instantaneous (by turning the heater power supply on and then off as fast as possible by hand) to a duration of 5 minutes. For example, test combinations of power level and time duration encompassed (but were not restricted to) the following:

Power Level (Watts)	Duration (Minutes)
1.5	2
5	5
70	0.1
190	-instantaneous
250	1
270	0.1

Test results were recorded on video tape, and hard copies of individual frames of interest are presented below to illustrate various results.

Without exception, all combinations of power level and duration produced an initial surge of circular fringes (resembling a bull's-eye pattern) which spread outward from the center of the HE (Figure D-2) and reversed direction (collapsing inward) immediately upon the termination of heating. For heating durations greater than a few seconds, the fringe pattern on the HE surface did not return to its initial configuration at the termination of heating, indicating that the HE surface had acquired a new orientation relative to the original. The spreading pattern of fringes seen during heating was evidence of a general distortion of the entire piece as the back surface underwent thermal expansion. Because the HE was clamped firmly along each long dimension, it could only bow outward toward the video camera as it expanded, resulting in a growing bull's-eye pattern. Thus, it is concluded that the fringe pattern was not the result of a strain caused by heat transfer through the cooling fins from the back surface to the front.

Ultrasonic testing of the calibration HE at Hughes indicated significant debonding on the surface which did not contain bosses. Unfortunately, this surface had to face the flat Minco heater to provide good heat transfer, and could not be analyzed by this method of thermal stressing.

When analyzing the side with bosses, no evidence of debonding was seen on the calibration HE, even though the Hughes ultrasonic procedure showed the presence of debonds. The only internal structure of the calibration HE detected holographically during this test was the central rib running lengthwise through the part.

Thermal stressing of the sample HE using the flat foil heater produced a general distortion which bowed the entire front surface outward, resulting in the characteristic bull's-eye fringe pattern (a result similar to the calibration HE). However, unlike the calibration HE, thermal stressing of the sample HE using the Minco heater did reveal evidence of the internal cellular, finned structure of the part. No evidence of debonding was seen beneath either surface.

Vibrational Stressing

Using both real-time and time-average HI, both the calibration and sample HEs were analyzed for the appearance of surface anomalies induced by vibrational stressing.

Using the Newport Corporation Shaker System Model HC-520, each HE was mounted to the universal back plate on four 1 inch standoffs and vibrated at various amplitudes at frequencies swept manually from 250 Hz to over 200 kHz. Each part was also vibrated with random "white noise" and evaluated.

While both HEs responded to vibration with interesting and intricate mode patterns (see, for example, Figure D-3 for a time averaged interferogram of the calibration HE taken at a frequency of 53 kHz), the presence of debonds was never revealed. As with thermal stressing, the internal central rib of the calibration HE could be discerned in the mode pattern, but the internal cellular structure of the cooling channels was never evident.

Pressure Stressing

Both the HEs were analyzed for the appearance of surface anomalies induced by pressure stressing. Using special fixturing described in a previous section, the open end of each HE was sealed against rubber gasket material to contain the air inside the part at one atmosphere, and the HE was placed inside a one cubic foot vacuum chamber fitted with a one square foot window for viewing. The air surrounding the HE was then partially evacuated to create a positive pressure within the HE, thus expanding the surface of the HE not in intimate contact with an internal fin (i.e., all areas not bonded to a fin). This procedure had the effect of showing clearly the internal structure of each HE, including the cellular structure of the cooling channels(Figure D-4), and the central internal rib of the calibration HE(Figure D-5). Most importantly, the pressure stressing revealed the areas of debonding as indicated by the Hughes ultrasonic analysis (Figure D-6). The shape of the debonded area as revealed by real-time HI was identical to that shown by the ultrasonic analysis. In contrast to the calibration HE, no areas of debond were found on either side of the sample HE when using this pressure stressing procedure.

B. Experimental Procedures and Results - Printed Wiring Boards

The procedures used to stress the PWBs were identical to those used to stress the HEs, with the single exception of the application of pressure stressing. Because the PWBs do not have internal channels for cooling, they were not clamped at both ends with rubber gasket material. Instead, they were supported at each corner with the 1 inch standoffs on the universal back plate. Any air trapped within the delaminations was expected to expand when the air outside the board was partially evacuated, thus causing a surface strain, visible as an anomalous fringe pattern.

Without exception, none of the stress procedures indicated the presence of delaminations in the two PWBs, in spite of the fact that the locations of the delaminations were known and watched very closely. However, subsequent analysis of the two PWBs by Hughes revealed that an error was made in their manufacture, and the visual patterns on the PWBs thought to be delaminations were in fact not delaminated at all. Thus, the null result of all tests on both PWBs was accurate.

SECTION IV

TASK 8 - CALIBRATION

Based upon the Hughes' analysis at the conclusion of Task 1 showing that the calibration PWBs delivered for that task did not contain photoresist inclusions, two new calibration PWBs were manufactured by Hughes for a newly created calibration task called Task 8. Task 8 was performed immediately upon completion of Task 1 because of the strong relationship between these two tasks.

Particular effort was expended by Hughes in Task 8 to insure the presence of delaminations in the new calibration PWBs. Specifically, photoresist inclusions were placed on circuit layers 2 and 3 of the 5 inch by 5 inch board, and on circuit layers 2, 7, and 13 of the 5 inch by 9 inch board. In addition, mold release compound was placed on one side of the inclusions to further decrease the chance of bonding between the inclusions and the substrate in contact with the inclusions.

These calibration PWBs were analyzed in Task 8 using the same HI techniques and analysis procedures detailed in Section III, above. The results of these analyses are documented in this section.

A. Experimental Results - Printed Wiring Boards

Thermal Stressing

Using real-time HI, the two PWBs were analyzed for the appearance of surface anomalies induced by thermal stressing. Thermal stressing was achieved by lightly passing a hand over a mounted PWB or heating the surface with a laboratory heat gun.

Thermal stressing revealed the presence of two delaminated areas on the 5 inch by 9 inch board within the pattern on the lower right quadrant of the side with copper circuitry (Figure D-7). One area was associated with the 1/2 inch by 1 inch triangle, and the other with the 1/2 inch circle.

The delamination over the triangle was especially sensitive to thermal changes, and exhibited visually striking fringe anomalies from naturally occurring environmental temperature changes alone, without the application of applied heat. The delamination associated with the 1/2 inch circle was less pronounced; although it responded slightly to naturally occurring environmental temperature changes, its appearance by way of fringe anomalies was enhanced by the application of heat applied by lightly passing a hand over the 1/2 inch circle. For both delaminated areas, the application of heat using the laboratory heat gun proved to be too extreme and caused a general distortion of the entire board, without enhancing the appearance of the fringes over the delaminations. Also for both delaminated areas, the use of phase shifting significantly enhanced the visual appearance of the fringes over each delamination.

The delamination associated with the triangle consisted of two adjacent circular patterns (Figure D-7), instead of a single triangular pattern as expected. The photoresist inclusion thus appeared to be bonded to the substrate immediately above it along a line separating the two small bull's-eye patterns associated with the triangle.

Thermal stressing of the reverse side of the 5 inch by 9 inch board, and both sides of the 5 inch by 5 inch board, did not reveal any evidence of further delaminations, even though the locations of the remaining five patterns were accurately known. Neither gentle heating by hand, nor vigorous heating with a heat gun, was successful in revealing the suspected flaws.

Vibrational and Pressure Stressing

Using both real-time and time-average HI, the two PWBs were analyzed for the appearance of surface anomalies induced by both vibrational and pressure stressing. Vibrational stressing was achieved with a Newport Corporation Shaker System Model HC-520 at frequencies swept manually from to 250 Hz to over 200 kHz. Pressure stressing was achieved in a one cubic foot vacuum chamber fitted with a one square foot window for viewing. Each side of each board was evaluated in detail with both stressing methods.

Without exception, neither of these stress methods indicated the presence of delaminations in either PWB, despite the range of frequencies and pressures used. The delaminations initially seen over the triangle and circle on the 5 inch by 9 inch board were always visible due to environmentally induced thermal stresses (as described above), but neither defect changed its initial appearance during either vibrational or pressure stressing.

It was thus concluded in Tasks 1 and 8 that areas of delamination are difficult to produce with certainty using photoresist/mold release inclusions, but that once produced, these areas can be very sensitive to thermal stressing. It is evident that holographic interferometry has the necessary sensitivity to reveal these defects. Because of the inability to produce defects with a high degree of certainty, the resolution of HI in this context has not yet been addressed.

SECTION V

TASK 2

Task 2 involved the nondestructive inspection by holographic interferometry of the four heat exchangers and six printed wiring boards from which more complex electronic modules would be built in later tasks. This section presents the documentation and discussion of the Task 2 test results obtained on these HEs and PWBs prior to the manufacturing of the electronic modules.

A. Experimental Results - Heat Exchangers

Using real-time HI, both sides of each HE were analyzed for the appearance of surface anomalies induced by pressure stressing. This was accomplished by placing each HE in a one cubic foot chamber fitted with a viewing window. The chamber was then evacuated while keeping the interior of the HE at one atmosphere pressure. A reference hologram was created at 26 to 28 inches of mercury vacuum (0.07 to 0.13 atmospheres). Air was then reintroduced into the chamber to raise the pressure an additional 5 to 15 inches of mercury (0.16 to 0.5 atmospheres). Surface strains created by the increase in ambient pressure surrounding the HE were then monitored by HI.

The above procedure revealed the internal cellular structure of each HE and showed that, with two minor exceptions, each of the eight sides examined was free of debonds. The two exceptions were the reverse sides of each of the 5 inch by 6 inch HEs (i.e., the sides containing the aluminum mounting brackets). Each of these sides appeared to have a subtle linear feature, visible on the video image, indicative of a weakened bond between the underlying heat conducting fins and the surface of the HE. Neither feature was indicative of complete separation; the continuity of the underlying cellular structure was preserved in both cases. Based on a subsequent conversation with Dan Buechler at Hughes, MetroLaser concluded that the defects revealed by this analysis did not warrant rejection of the HEs. Video recordings of these test results are found within Trial 2 and Trial 4 during the first 20 minutes of the Task 2 video recording supplied to Hughes.

B. Experimental Results - Printed Wiring Boards

Using real-time HI, the six PWBs were analyzed for the appearance of surface anomalies induced by thermal stressing. Thermal stressing was achieved by both lightly passing a hand over a mounted PWB and by heating the surface with a laboratory heat gun. Without exception, HI analysis revealed no evidence of delaminations on any of the PWBs.

SECTION VI

TASK 3

At the completion of Task 2, the four HEs and six PWBs tested in Task 2 were assembled into two 5 inch by 9 inch and two 5 inch by 6 inch PWB/HE modules delivered with a plastic plenum glued onto either end and a multi-pin connector attached with rivets along one edge. The modules were analyzed by holographic interferometry in Task 3. They did not contain any electronics, so no special procedures for handling static sensitive devices were necessary. This section presents a discussion of the Task 3 test results obtained on these modules.

A. Experimental Results - Real-Time HI with Thermal Stressing

This subsection describes the results of real-time HI testing with **thermal stressing** of the four modules supplied for this task.

Using real-time HI, each side of a module with a PWB attached was analyzed for the appearance of surface anomalies induced by thermal stressing. This resulted in the testing of both sides of each 5 inch by 9 inch module, and one side each of the 5 inch by 6 inch modules. Thermal stressing in Task 3 was intended to uncover any delaminations in the PWBs, or possible voids or air trapped between the HEs and the adhesive layer used to bond the PWBs to the HEs. Note that the presence of trapped air between the PWB and the adhesive layer was considered unlikely because of the matrix of through-holes in the PWBs which would allow trapped air to escape as the adhesive was cured under elevated temperature and pressure during the manufacturing process.

Testing was accomplished by holding each module in a fixture whereby the plastic plenum at either end was securely clamped against a gasketed aluminum bracket (this is exactly the fixturing used for pressure stressing in this program). This fixturing was used for thermal stressing in Task 3 because the rivets used to mount the multi-pin connector attached to the bottom of each module covered the row of holes used to mount the HEs and PWBs for thermal stressing in the previous tasks.

Thermal stressing was achieved by both lightly passing a hand over a mounted module and by heating the surface with a laboratory heat gun. Without exception, real-time HI analyses revealed no evidence of delaminations on any of the PWBs, nor voids or trapped air between any of the HEs and the adjacent adhesive layers.

B. Experimental Results - Real-Time HI with Pressure Stressing

This section describes the results of real-time HI testing with pressure stressing of the four modules supplied for this task.

Using real-time HI, both sides of each module were analyzed for the appearance of surface anomalies induced by pressure stressing. As in previous tasks, pressure stressing was expected to reveal the presence of any debonding between the surface sheets and the cooling fins within the HEs. Also, as with thermal stressing described above, pressure stressing was expected in Task 3 to reveal possible voids or air trapped between the HEs and the adhesive layer used to bond the PWBs to the HEs.

It is important to note here that for pressure stressing to be effective in revealing debonding between the surface sheets and the cooling fins within a HE, the glue seal between the plastic plenums and the HE must be leak tight to maintain a constant pressure within the HE as the surroundings of the module are evacuated. If there is even a minor leak at the plenum/HE interface (i.e., one that would be inconsequential to the performance of the module in the end product), then sealing the input and output edges of the two plenums (as is done during pressure stressing in this program) will not keep the interior of the HE at constant pressure as the surroundings are evacuated. Thus, a pressure differential cannot be created across the HE surface and pressure stressing does not occur, rendering the test inconclusive as far as revealing debonds within the HE. (The integrity of the seal at the plenum/HE interface does not affect the ability of this test to reveal trapped air between the adhesive layer and the HE.)

According to Dan Buechler at Hughes, the glue seals between the plastic plenums and the HE are not required by the Air Force to be absolutely leak tight. The integrity of the glue seal at the plenum/HE interface is considered acceptable if it allows the module to flow a specified volume of air per unit time at a specified pressure drop between the input and output plenum. *In fact, several of the plenums were found to be loose in Task 3 along a portion of the length of the glue seal, as evidenced by an obvious movement of the plenum against the HE when applying pressure to the plenum by hand.* One glue seal was weak enough that it failed as the module was clamped in the test fixture, and could thereafter be taken on and off the HE as desired (this was the 5 inch by 6 inch module with PWB Part No. ES9499).

The fixturing used for these tests was identical to that used with thermal stressing, described above. Each module was clamped firmly at either end against silicone rubber gasket material. Note that the impression of the plenum on the gasket was examined closely at the conclusion of testing to insure the integrity of the seal during testing. The fixtured module was then placed in a one cubic foot vacuum chamber fitted with a viewing window. The chamber was evacuated and a reference hologram was created at 26 to 28 inches of mercury vacuum (0.07 to 0.13 atmospheres). Air was then reintroduced into the chamber to raise the pressure an additional 5 to 15 inches of mercury (0.16 to 0.5 atmospheres) and evidence of surface strains created by the increase in ambient pressure surrounding the module were then monitored by HI.

Without exception, no HE surface examined by HI showed the characteristic cellular pattern which was so easily created in Task 2, indicating a pressure differential was not being established. Because the impression left on the gasket material indicated that each plenum was sealed at its input or output face, it was concluded that at least one of the two plenum/HE glue seals on each module was not leak tight, thus precluding the evaluation of debonding within the HEs.

Furthermore, the examination of each module under pressure stressing did not reveal any evidence of trapped air between the adhesive layer (bonding a PWB to a HE) and the HE surface. It was therefore concluded that each PWB was bonded to its respective HE without air gaps or voids.

SECTION VII

TASK 4

At the completion of Task 3, discrete electronic components were added by Hughes Aircraft Co. to the four modules tested in Task 3. These modules were then inspected by holographic interferometry in Task 4. This section describes these results.

Only thermal stressing was used in Task 4. As explained in Section VI, above, at least one of the two plenum/HE glue seals on each module was not leak tight, which precluded the evaluation of debonding within the HEs via pressure stressing. Furthermore, the examination of each module under pressure stressing in Task 3 did not reveal any evidence of trapped air between the adhesive layer (bonding a PWB to a HE) and the HE surface. It was therefore concluded that each PWB was bonded appropriately to its respective HE without air gaps or voids, and these tests were not repeated during Task 4.

The surface mounted electronic components on each module were static sensitive, requiring that special precautions be taken when handling and analyzing them. For example, the stainless steel optical table used in this study was grounded to a water pipe in the laboratory, and a conductive wrist strap, worn by MetroLaser personnel whenever the modules were handled, was grounded to the table top. The modules were only removed from their conductive storage pouches in the vicinity of the optical table.

A. Experimental Results - Real-Time HI with Thermal Stressing

This section describes the results of real-time HI testing with thermal stressing of the four modules supplied for this task.

Using real-time HI, each side of a module with a PWB attached was analyzed for the appearance of surface anomalies induced by thermal stressing. This resulted in the testing of both sides of each 5 inch by 9 inch module, and one side each of the 5 inch by 6 inch modules. Thermal stressing in Task 4 was intended to uncover any delaminations appearing in the PWBs or any debonding between the PWBs and the underlying HEs appearing since Task 3 testing, or any anomalous movement or behavior of the surface mounted electronic components that would indicate a lack of mechanical integrity, a weak solder joint, etc.

Testing was accomplished by holding each module in a fixture whereby the plastic plenum at either end was securely clamped against a gasketed aluminum bracket (this is exactly the fixturing used for pressure stressing in Tasks 1, 2, 3, and 9). Thermal stressing was achieved by both lightly passing a hand over a mounted module and by heating the surface with a laboratory heat gun. Without exception, real-time HI analyses revealed no evidence of 1) delaminations in any of the PWBs, 2) any debonding appearing between the PWBs and the underlying HEs, or 3) any anomalous movement or behavior of the surface mounted electronic components that would indicate a lack of mechanical integrity or a weak solder joint, etc.

In spite of the absence of detectable flaws, several interesting phenomena were observed during Task 4 testing. First, each of the 5 inch by 6 inch modules contained three large electronic components in metallic packages. Upon the application of heat to achieve thermal stressing, a distinct bull's-eye pattern appeared on each of the three components (Figure 8). The bull's-eye pattern was centered on each component, indicating that the component did not undergo rigid body movement relative to the underlying PWB, but

instead the surface expanded (or contracted) toward (or away from) the camera. A full 20 fringes (approximately 5 microns) of movement was detected.

Second, the small ICs on the 5 inch by 9 inch modules underwent rigid body movement relative to the underlying PWB (but no surface distention or contraction) when subjected to thermal stressing as evidenced by the "ruler straight" fringes that appeared on each IC (as opposed to the bull's-eye pattern on the metallic components). However, each IC assumed a random orientation relative to its neighbor as evidenced by the random orientation of the straight fringes on one IC relative to the fringe orientation on an adjacent IC. Phase shifting resulted in a fascinating video display of fringes moving in all directions.

Lastly, the 5 inch by 9 inch modules (and to a lesser extent the smaller modules) exhibited very high surface contrast between, for example, the individual leads and the underlying PWB. The individual leads on the ICs were overexposed by the holocamera when the PWB or the plastic/ceramic ICs were correctly exposed, making it difficult to simultaneously image fringes on the individual leads and the underlying PWB.

SECTION VIII

TASKS 5, 6, AND 7

Tasks 5, 6, and 7 differed only in the specific processing that the modules were subjected at Hughes Aircraft Co. prior to each task. That is, prior to Tasks 5, 6, and 7, the four electronics modules were conditioned, subjected to power-on screening, and subjected to system burn-in, respectively.

Throughout Tasks 5, 6, and 7, each side of a module with a PWB attached was analyzed using real-time HI for the appearance of surface anomalies induced by thermal stressing. Testing was accomplished in a manner identical to that used in Task 4, described in Section VII, above. In each of the three tasks, preventative measures were taken to insure that the modules were not damaged by electrostatic discharge, as described in Section VII, above. Without exception, real-time HI analyses in all three tasks revealed no evidence of 1) delaminations in any of the PWBs, 2) any debonding appearing between the PWBs and the underlying HEs, or 3) any anomalous movement or behavior of the surface mounted electronic components that would indicate a lack of mechanical integrity or a weak solder joint, etc.

The same three phenomena observed in Task 4 regarding the response of the modules to thermal stressing (discussed in more detail in Section VII, above) was also observed in each of Tasks 5, 6, and 7. These included 1) the bull's-eye pattern on the three large ICs in metallic packages, 2) the rigid body motion of the small ICs, and 3) the high contrast of the solder leads relative to the underlying PWB.

SECTION IX

SUMMARY AND CONCLUSIONS

This report has presented the documentation and discussion of the evaluation of electronics modules using holographic interferometry. The program was organized into nine tasks, as discussed in the introduction to this report. The following is a brief summary of the program results, organized by task, including a statement of the conclusions reached in this program:

Task 1 saw the initial application of a variety of specialized equipment for real-time and time-average holography in the analysis of HEs and PWBs. Fixturing was developed to securely mount two calibration HEs and two calibration PWBs to facilitate the use of a variety of thermal, vibrational, and pressure stressing methods. The methodology, procedures, stress methods, and fringe enhancement techniques were selected and applied successfully in Task 1.

Of the various stressing methods applied to the calibration pieces, pressure stressing proved successful in Task 1 in revealing areas of debonding in one of the calibrated HEs, as verified by ultrasonic analysis at Hughes.

The analysis of the two calibration PWBs in Task 1 was inconclusive because of a manufacturing error which resulted in the absence of delaminations. It was decided at this point that two new calibration PWBs would be created and analyzed by HI in a new task, designated Task 8. The successful application of thermal stressing in Task 8 revealed an inclusion in one of the new calibration PWBs.

At the completion of Tasks 1 and 8, the following conclusions had been reached:

- HI has the necessary sensitivity and resolution to reveal areas of debond within the HEs when applying pressure stressing.
- Areas of delamination within the PWBs are currently difficult to produce using photoresist/mold release inclusions. Once produced, however, these delaminations are very sensitive to thermal stressing.
- HI has the necessary sensitivity to reveal thermally stressed delaminated inclusions close to the PWB surface.
- The ability of HI to reveal deeper delaminations in PWBs has not been assessed because of the difficulty of reliably producing deep delaminations artificially.
- The resolution of HI in detecting delaminations in PWBs has not been assessed because of the difficulty of reliably producing artificial delaminations smaller than 1/2 inch diameter.

Task 2 involved the testing by HI of four new HEs and six new PWBs. Based on the conclusions above, the HEs were pressure stressed and the PWBs were thermally stressed during HI analysis. Under thermal stressing, no delaminations were seen in the PWBs. Pressure stressing of the HEs revealed evidence of a minor debond in two of the parts, although it was jointly decided by MetroLaser and Hughes that these debonds were not severe enough to warrant rejection of the affected HEs from this program.

For Task 3, the four HEs and six PWBs tested in Task 2 were assembled into two 5 inch by 9 inch and two 5 inch by 6 inch PWB/HE modules delivered with a plastic plenum glued onto either end and a multi-pin connector attached with rivets along one edge. The modules analyzed in Task 3 did not contain any electronics, so no special procedures for handling static sensitive devices were necessary. Without exception, real-time HI analyses revealed no evidence of delaminations on any of the PWBs when using thermal stressing, nor voids or trapped air between any of the HEs and the adjacent adhesive layers when using either thermal or pressure stressing. Since at least one of the two plenum/HE glue seals on each module was not leak tight, the evaluation of debonding within the HEs could not be performed.

For Task 4, discrete electronic components were added by Hughes Aircraft Co. to the four modules tested in Task 3. These electronic components were static sensitive, requiring that special precautions be taken when handling and analyzing them (i.e., the optical table was grounded, MetroLaser personnel wore grounded wrist straps when handling the modules, and the modules were only removed from their conductive storage pouches in the vicinity of the optical table). Without exception, real-time HI analyses using thermal stressing revealed no evidence of 1) delaminations in any of the PWBs, 2) any debonding appearing between the PWBs and the underlying HEs, or 3) any anomalous movement or behavior of the surface mounted electronic components that would indicate a lack of mechanical integrity or a weak solder joint, etc.

For Tasks 5, 6, and 7, the modules were conditioned, subjected to power-on screening, and subjected to system burn-in, respectively, at Hughes Aircraft Co. After each process, the modules were delivered to MetroLaser and analyzed by real-time HI using thermal stressing. No physical flaws were detected in these tasks.

The work performed in Tasks 4 through 7 resulted in the following conclusions:

- ICs in metallic packages take up heat at a much greater rate than nonmetallic ICs or the PWB to which they are mounted. This results in the appearance of a distinct bull's-eye pattern centered on each of the metallic packages when heated. This fringe pattern does not by itself indicate a flaw, but indicates only that the surfaces of the ICs are expanding toward (or away from) the camera.

- When heated, the small ICs on the 5 inch by 9 inch modules will undergo rigid body movement relative to the underlying PWB as evidenced by the "ruler straight" fringes that appear on each IC (as opposed to the bull's-eye pattern on the metallic components). Each IC assumes a random orientation relative to its neighbor as evidenced by the random orientation of the straight fringes on one IC relative to the fringe orientation on an adjacent IC.

- The 5 inch by 9 inch modules (and to a lesser extent the smaller modules) exhibit very high surface contrast between, for example, the individual conductive leads and the underlying PWB. The individual leads on the ICs are overexposed by the holocamera when the PWB or the plastic/ceramic ICs are correctly exposed, making it difficult to simultaneously image fringes on the individual leads and the underlying PWB.

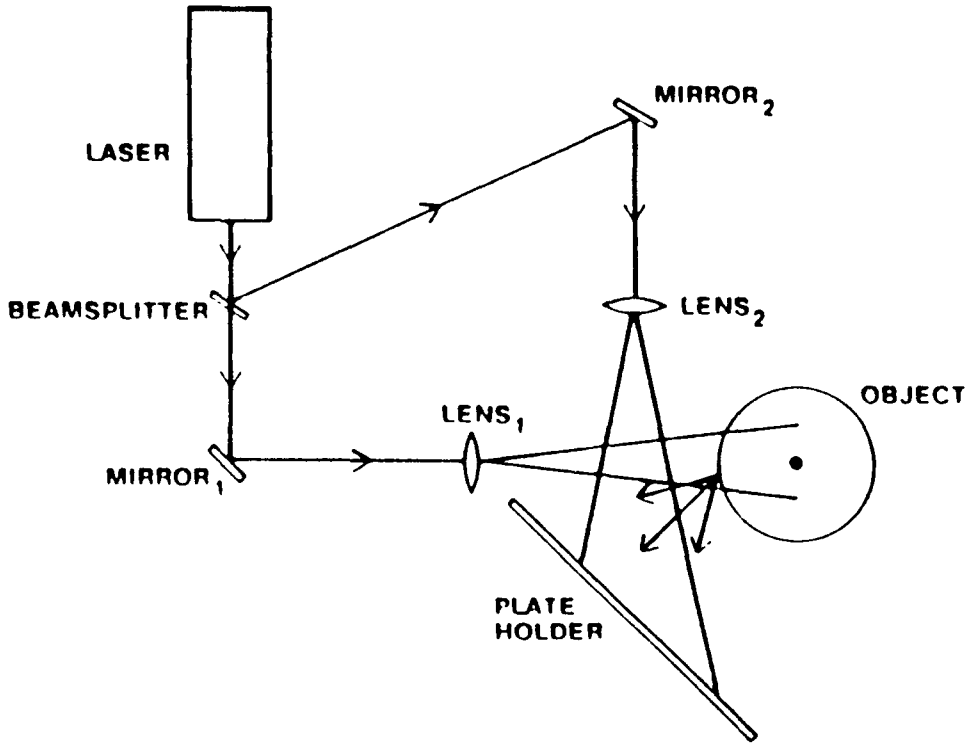


Figure D-1. Schematic diagram of typical holographic interferometry setup.

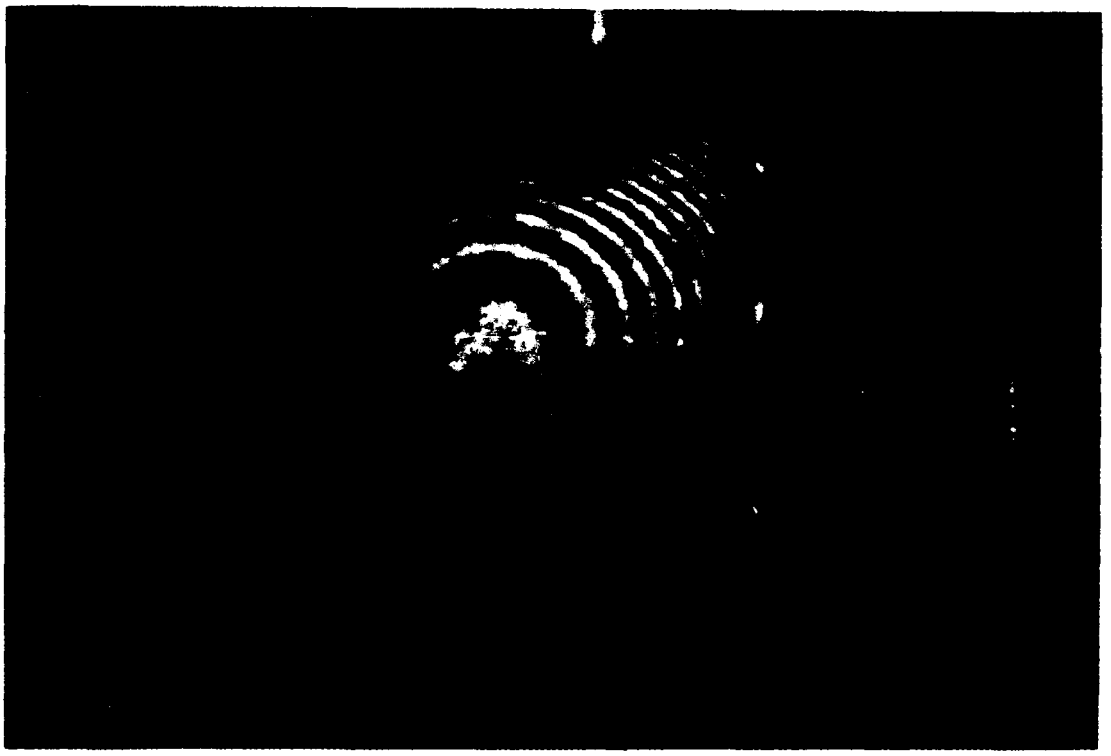


Figure D-2. Real-time interferogram of circular fringes resulting from general distortion of calibration heat exchanger as heat is applied uniformly over back surface with Minco Thermofoil Heater.

Figure D-3. Time-average interferogram of the calibration heat exchanger taken at a vibrational frequency of 53 kHz.

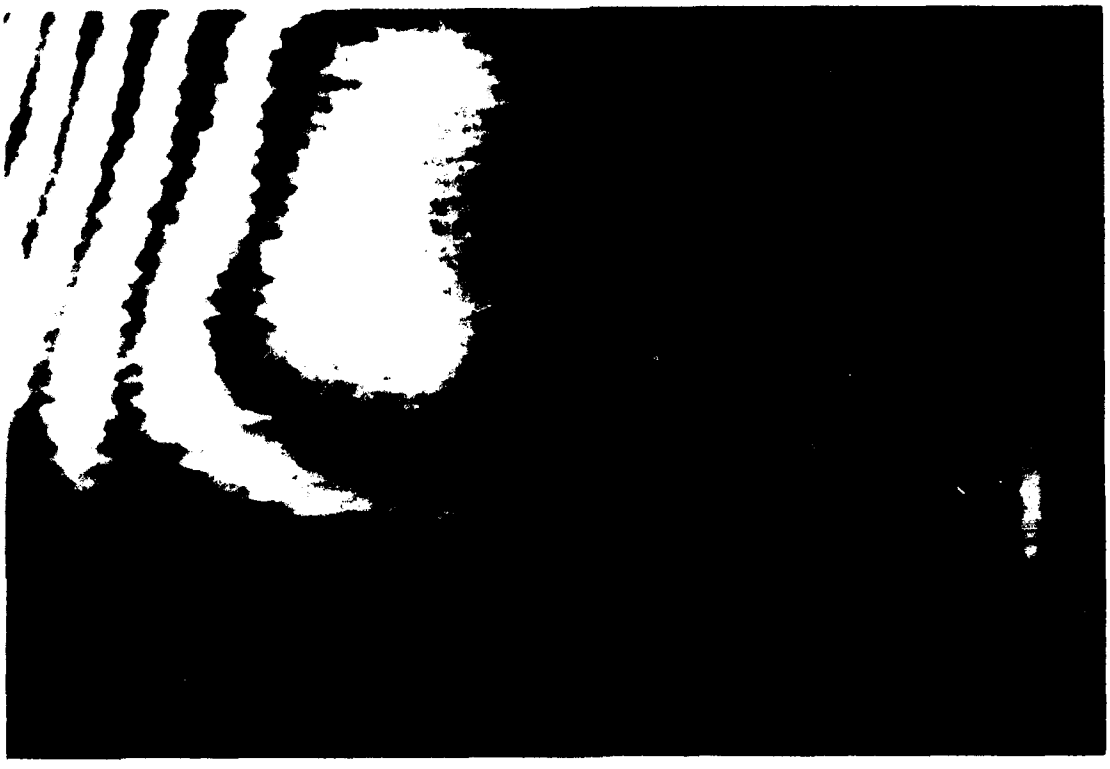


Figure D-4. Real-time interferogram showing the internal cellular structure of the sample heat exchanger cooling channels under an applied pressure stress.

Figure D-5. Real-time interferogram showing the internal central rib of the calibration heat exchanger under an applied pressure stress.

Figure D-6. Real-time interferogram of areas of debonding (ellipse) beneath the surface of the calibration heat exchanger under applied pressure stress.

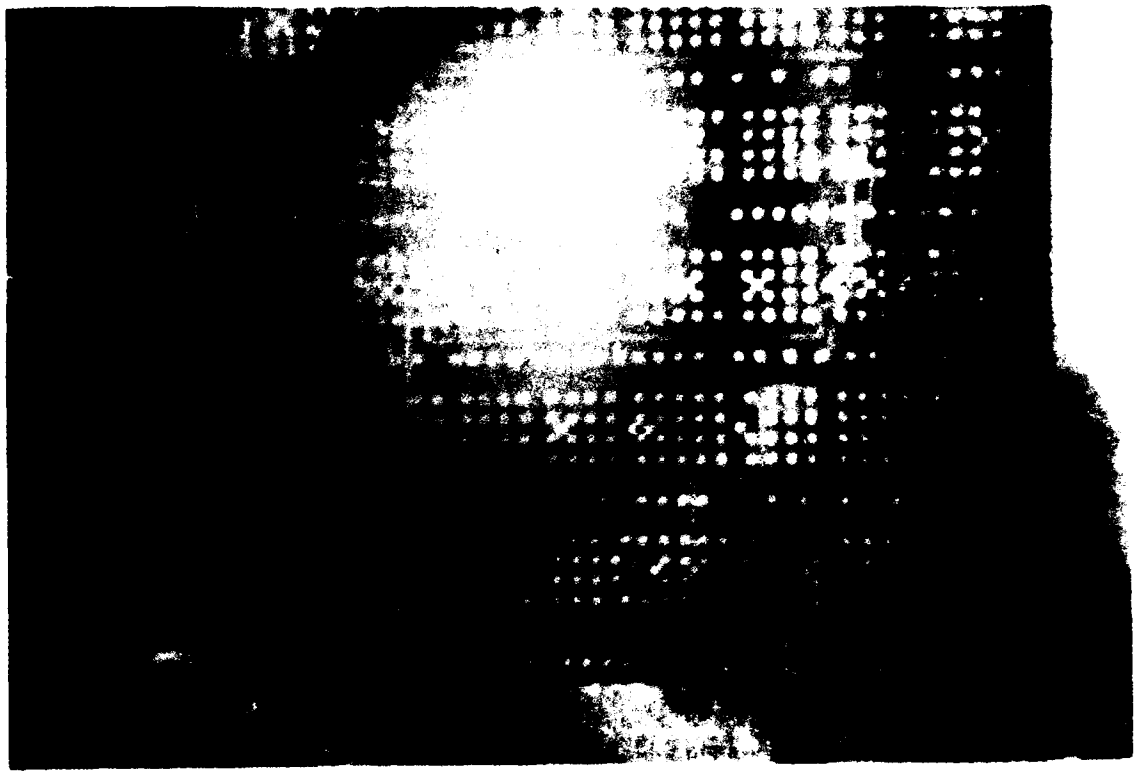


Figure D-7. Real-time interferogram revealing the presence of debonds (circled) using thermal stressing induced by naturally occurring environmental temperature changes on the 5 inch by 9 inch printed wiring board.

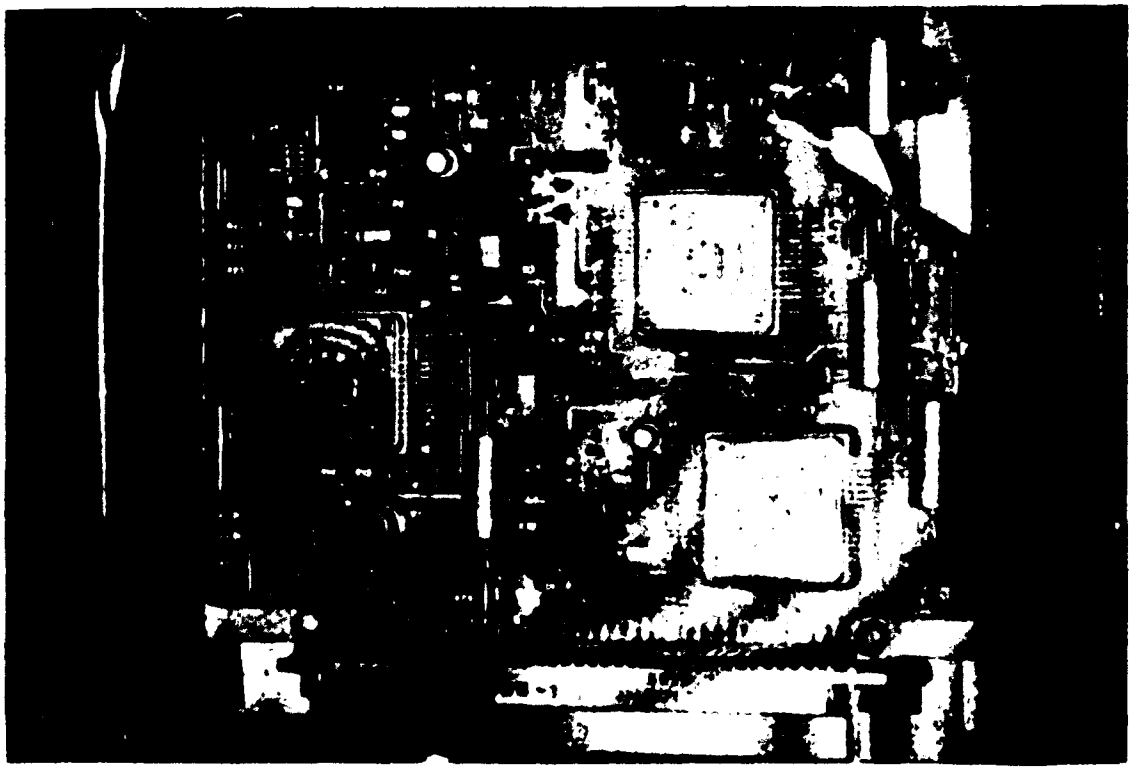


Figure D-8. Typical interferometric fringes appearing as a bull's-eye pattern on each of the three ICs in metallic packages on the analog linear regulator modules.

APPENDIX E

CALIBRATION PWBs FOR HOLOGRAPHIC INTERFEROMETRY

INTERDEPARTMENTAL CORRESPONDENCE

TO: D. W. Buechler
ORG: 76-41-22

C: M. D. Beam
J. M. Kallis
L. J. Kane
File

DATE: May 8, 1989
REF: 7631.41/1136

SUBJECT **Delaminated Printed Wiring Boards**

FROM: D. S. Huff
ORG: 76-31-41

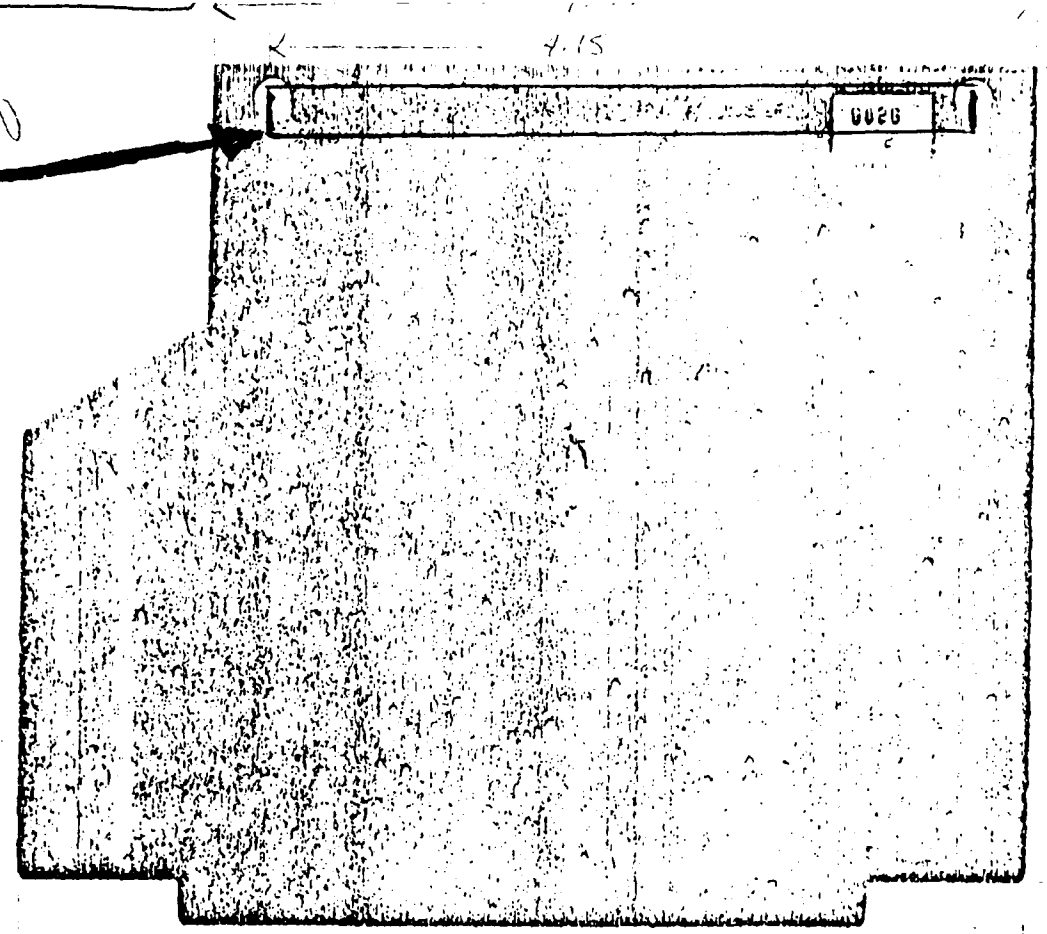
BLDG. E1 MAIL STA. C187
LOC. EO PHONE 616-6026

Technology Support Division (TSD) fabricated one printed wiring board of part number 3569825 (epoxy) and one printed wiring board of part number 3562151-30 (polyimide). Delamination was purposely induced by applying a pattern of 0.002-inch aqueous photoresist onto some of the etched inner layers, prior to lamination. The patterns fell on both copper and laminate as shown in the attached figures. They were applied to layers 2 and 3 of part number 3569825 and to layers 2, 7 and 13 of part number 3562151-30. The patterns could not be placed between layers derived from a single sheet of copperclad. Instead, they were placed between layers bonded together by prepreg. For this reason, the pattern on layer 7 fell between layers 6 and 7, instead of between layers 7 and 8, as you requested. The patterns were also applied to the coupons (layer 3 of P/N 3569825 and layer 7 of P/N 3562151-30). Delamination will be enhanced by applying heat.

D. S. Huff, MTS II
Soldering & Interconnections Group
Application Engineering Section

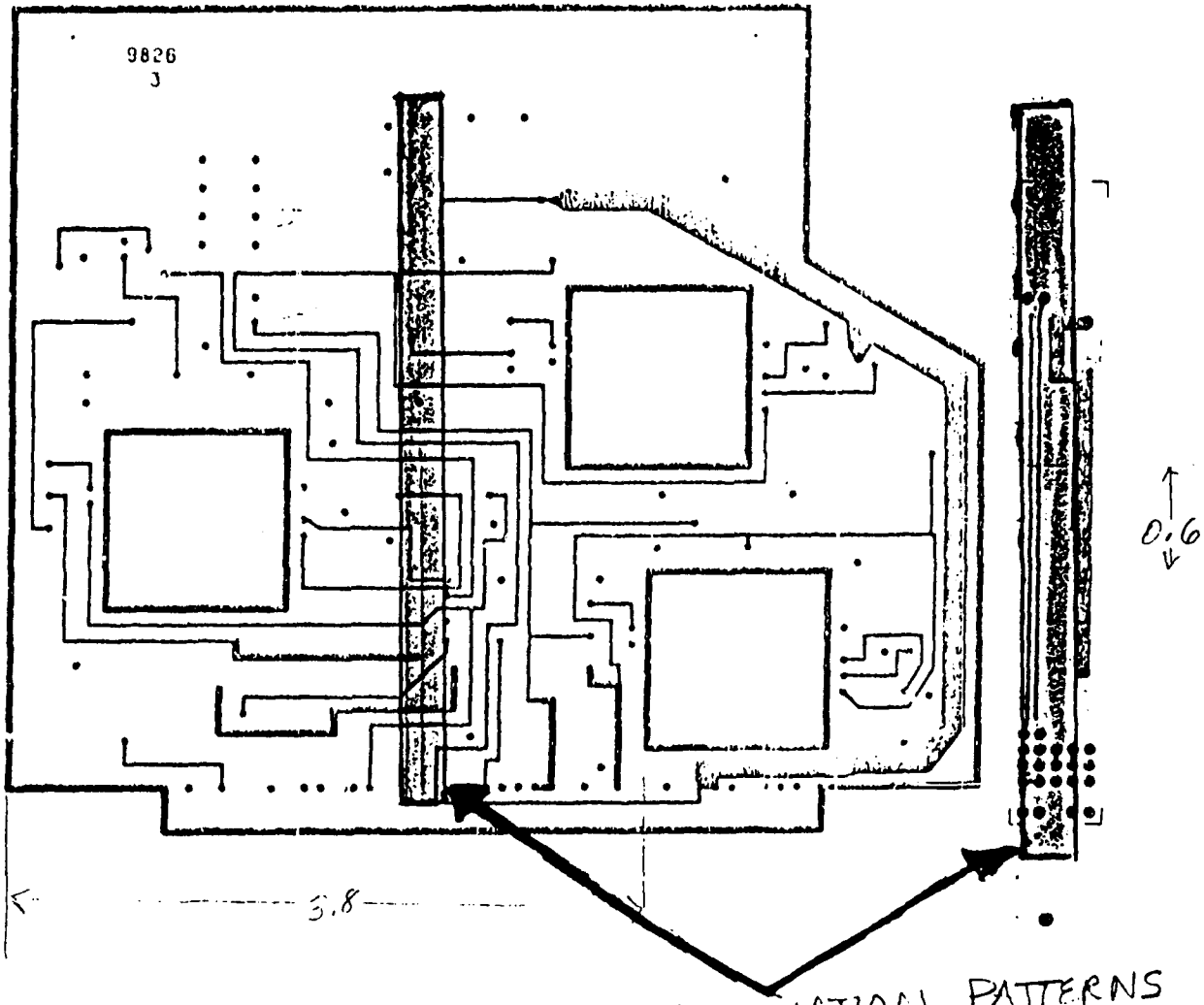
R. W. Clark, Head
Application Engineering Section

DSH/jv



LAYER 2
3580826(-)

3569825



DELAMINATION PATTERNS
APPROXIMATE LOCATIONS

LAYER 3
3580828(-)

REAR TO MATCH FRONT WITHIN .002 TOTAL
TARGET CENTERS 6.000 ±.002

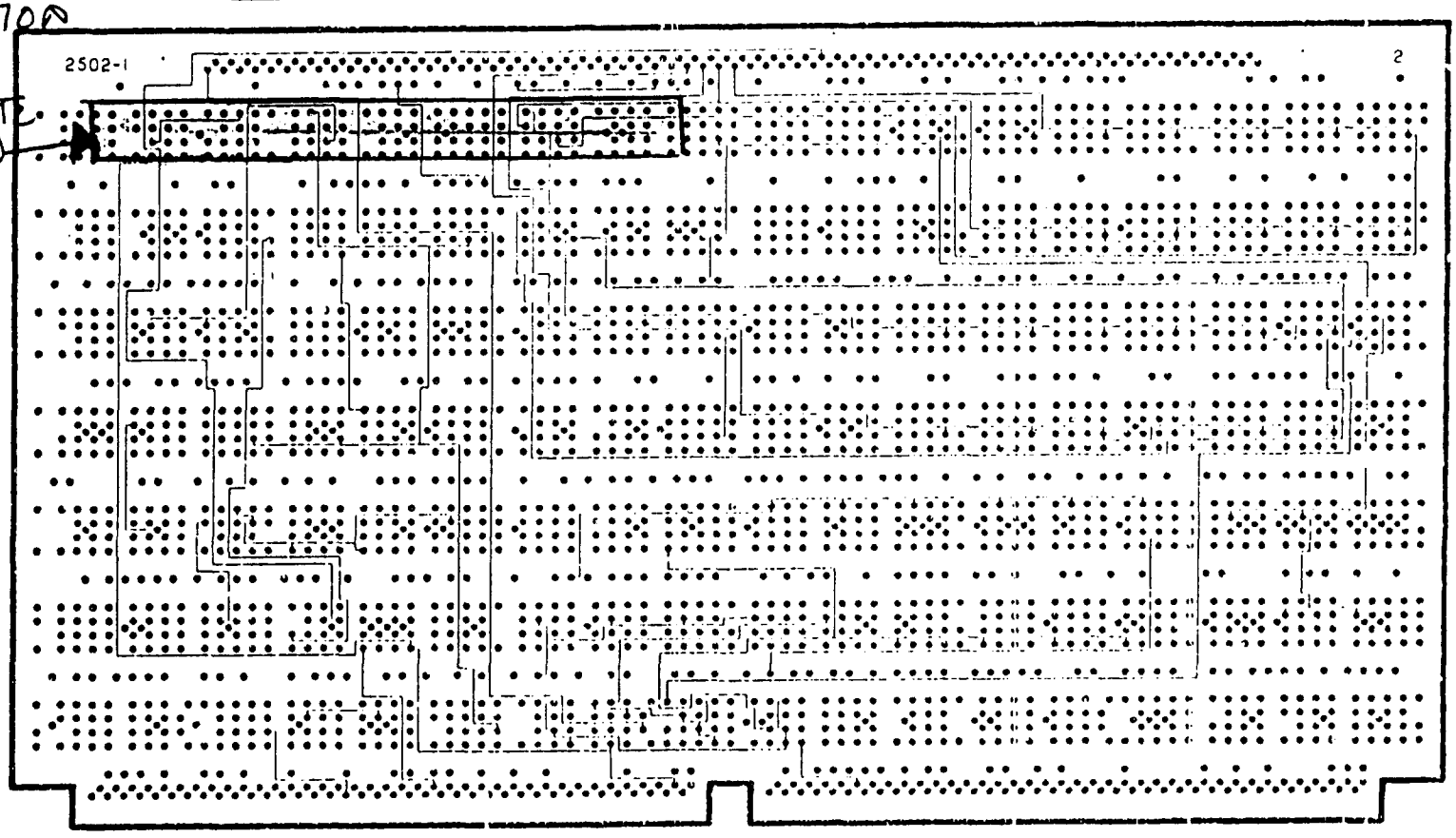
E-3

3569825

BETWEEN LAYERS 2 & 3

DELAMINATION PATTERN APPROXIMATE LOCATION

TO MATCH LAYER 1 WITHIN .002 TOTAL



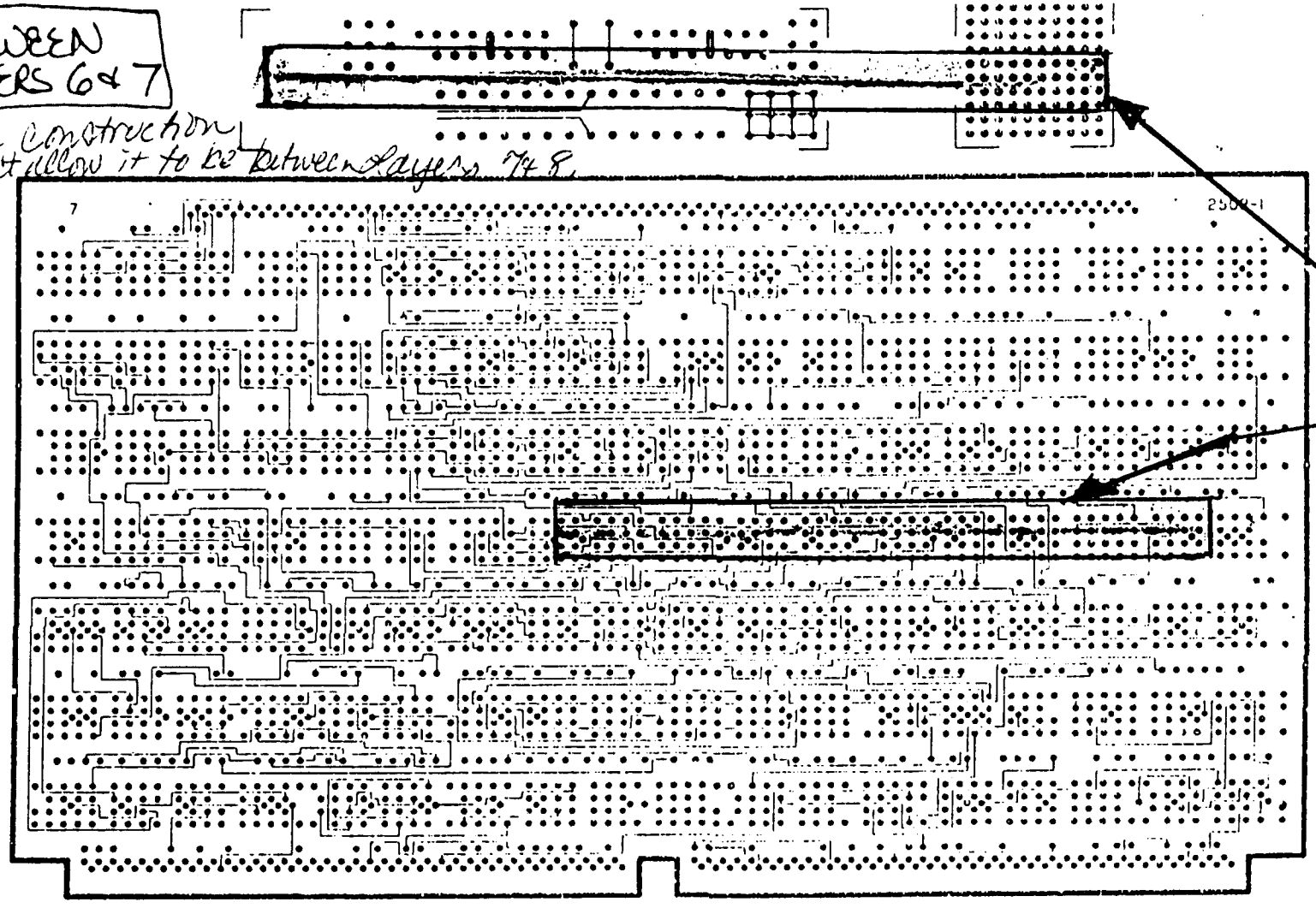
3562502-1
(3562151-30 PWB)

LAYER 2

F-4

BETWEEN LAYERS 6 & 7

DAN, the construction would not allow it to be between layers 7 & 8.



DELAMINATION PATTERN APPROXIMATE LOCATIONS

TO MATCH LAYER 1 WITHIN .002 TOTAL

E-5

3562502-1

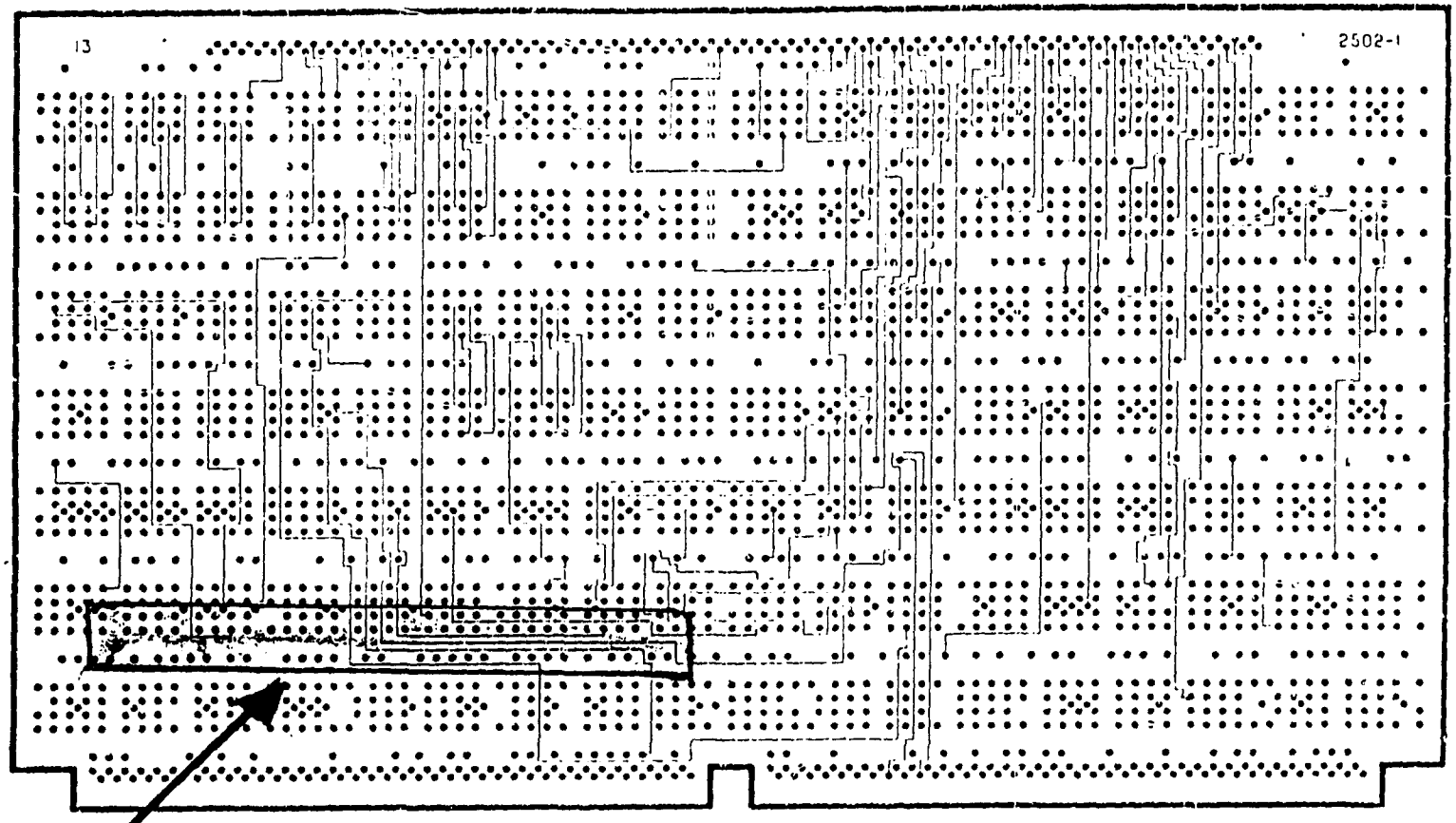
(3562151-30 PWB)

LAYER 7

SIZE B

SCA

12 & 13



TO MATCH LAYER 1
WITHIN .002 TOTAL

E-6

DELAMINATION
PATTERN
• APPROXIMATE
LOCATION

3562502-1
(3562151-30 PWB)

LAYER 13

APPENDIX F

THERMAL ANALYSIS OF THE F-15 PSP TIMING AND CONTROL MODULE

INTERDEPARTMENTAL CORRESPONDENCE

TO: R. D. Ritacco
ORG: 76-41

CC: Distribution

DATE: September 2, 1988
REF: 722620/1292

SUBJECT: Thermal Analysis of the F-15 PSP Timing and Control Module

FROM: W. J. Hoskins
ORG: 72-26-22

BLDG: E12 MAIL STA.: B103
LOC: EO PHONE: 414-6850

REFERENCE: "F-18 Thermal Library," from W. K. Hammond, dated May 23,1980. User F18LIB [12101,202], Job F18THM Seg. 1028

SUMMARY

A detailed thermal analysis of the PSP Timing and Control module in the Signal Processor unit for the F-15 aircraft has been performed. The purpose of the analysis was to predict the maximum steady-state operating temperatures of all components on the module.

The Timing and Control is a flow-through module that consists of two printed wiring boards(PWB's) mounted on a rectangular heat exchanger. The heat exchanger is made of rectangular plate finstock (7.0R-.125-.5(O)-.006Al) sandwiched between two .008 inch thick 6061-T6 Aluminum facesheets.

The module power dissipation is 47.8 Watts. The component dissipations were supplied by W. Hammond (72-26) in the Reference. The inlet air is at 29.4°C(85°F) and the air flow rate through the module is .202 lb/min.

KEY RESULTS

The hottest component is U2517 with a junction temperature of 93°C. The hottest resistor and capacitor are R1106 and C151 with case temperatures of 88°C and 67°C, respectively.

W. J. Hoskins, MTS
THERMODYNAMICS DEPARTMENT

Approved:
E. B. Curry, Section Head
THERMODYNAMICS DEPARTMENT

WJH:jw

THERMAL ANALYSIS OF THE F-15 PSP TIMING AND CONTROL MODULE

BY

W. J. HOSKINS

INTRODUCTION

A detailed thermal analysis of the PSP Timing and Control module in the Signal Processor unit for the F-15 aircraft has been performed. The purpose of the analysis was to predict the maximum steady-state operating temperatures of all components on the module.

The Timing and Control is a flow-through module that consists of two printed wiring boards(PWB's) mounted on a rectangular heat exchanger. The heat exchanger is made of rectangular plate finstock (7.0R-.125-.5(O)-.006Al) sandwiched between two .008 inch thick 6061-T6 Aluminum facesheets.

The module power dissipation is 47.8 Watts. The component dissipations were supplied by W. Hammond (72-26) in the Reference. The inlet air is at 29.4°C(85°F) and the air flow rate through the module is .202 lb/min.

ANALYSIS INPUTS

Physical Design

The PSP Timing and Control is a flow-through module that consists of two printed wiring boards(PWB's) mounted on a rectangular heat exchanger. The heat exchanger is made of rectangular plate finstock (7.0R-.125-.5(O)-.006Al) sandwiched between two .008 in thick 6061-T6 Aluminum facesheets. The facesheets are 9.5 inches long and 5.0 inches wide. The facesheets are supported on two sides by spacers that are 9.5 inches long and 0.120 inches high. The width of the spacer is .255 inches on bottom edge of the facesheet, and .472 inches on the top edge.

A printed wiring board is bonded to each side of the heat exchanger per the requirements of HPR 42001/1 (which calls for material HMS 20-2010). The printed wiring boards are made of .091 inch thick polyimide and include 14-1 ounce layers of copper. The components are mounted to the printed wiring boards to meet the requirements of HPR 31001/1. Figures 1 and 2 show the flow-through configuration of the Timing and Control module.

Coldplate Dimensions-	
Length,	9.5 inches
Width,	4.25 inches
Height,	0.125 inches
Fin Characteristics-	
Pitch,	7
Height,	0.125 inches
Offset Length,	0.5 inches
Material Thickness,	0.006 inches

Thermal Configuration

The heat originates in the components and then must travel through the case, leads and any bonding material present to the mounting surface. The heat must then enter the board and be conducted to the heat exchanger. Finally the heat is conducted through the heat exchanger to the cooling air. The 24.9°C(85°F) cooling air is forced through the inlet guide of the module at a flow rate of 0.202 lb/min. It passes through the heat exchanger and receives the heat dissipated by the components.

Operating Conditions

Power Dissipation	47.8Watts
Cooling Air	
Inlet Temperature	29.4°C(85°F)
Flow Rate	0.0202lb/min

Material Properties

Material	Thermal Conductivity
Aluminum 6061-T6	4.0 W/in°c (91 Btu/hr-ft-°F)
Polyimide	
X-Y plane	0.021 W/in°C (0.47 BTU/hr-ft-°F)
Z direction	0.01 W/in°C (0.23 BTU/hr-ft-°F)
Copper	9.7 W/in°C (218 BTU/hr-ft-°F)
HMS 20-2010	0.0066W/in°C (0.15 BTU/hr-ft-°F)
Component bond material	
Flow Under, Adhesive	.005 W/in°C
Polysulfide Paste	.0085 W/in°C

Assumption

Power dissipations less than .5mW were omitted.

ANALYSIS METHOD

A mathematical model was built to represent the heat exchanger, the printed wiring boards, and the airflow through the heat exchanger. The model was created to account for conduction and convection within and from the module. To model the air flow, one-way conductors were used . To calculate the convective heat transfer coefficient between the air flow and the heat exchanger, in-house computer software(COLDPLATE) was used. COLDPLATE is a program especially developed to determine the heat transfer coefficient, pressure drop, fin effectiveness and air exhaust temperature for a given fin, power, coldplate and cooling air conditions.

The model was analyzed using the Automated Thermal Data Processor (ATDP) computer program. This program incorporates the CINDA finite differencing thermal analysis program

with a pre-processor and post-processor developed specifically to calculate the mounting surface, case, and junction temperatures (where applicable) of each component.

RESULTS

The hottest component is U2517 with a junction temperature of 93°C. The hottest resistor and capacitor are R1106 and C151 with case temperatures of 88°C and 67°C respectively.

Table 1 provides the predicted component operating temperatures for the Timing and Control module. This table includes the power dissipation, predicted mounting surface, case, and junction temperatures (where applicable). Figures 3 through 12 give the layouts, dissipations, mounting surface temperatures, case temperatures and junction temperatures for the components on the front and rear sides of the module.

REFERENCE: "F-18 Thermal Library," from W. K. Hammond, dated May 23,1980. User F18LIB [12101,202], Job F18THM Seg. 1028

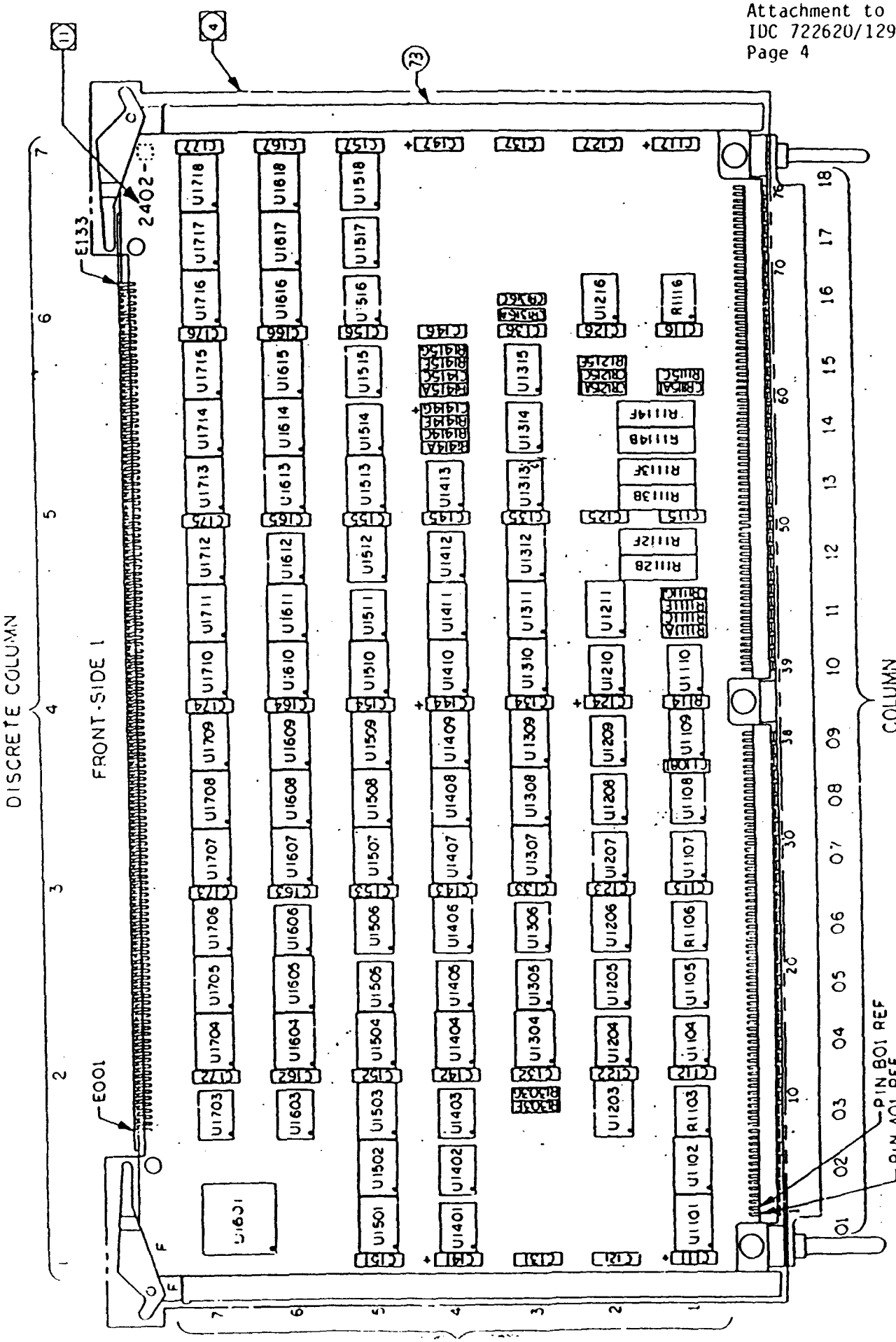


FIGURE F-1. COMPONENT LAYOUT – FRONT SIDE 1

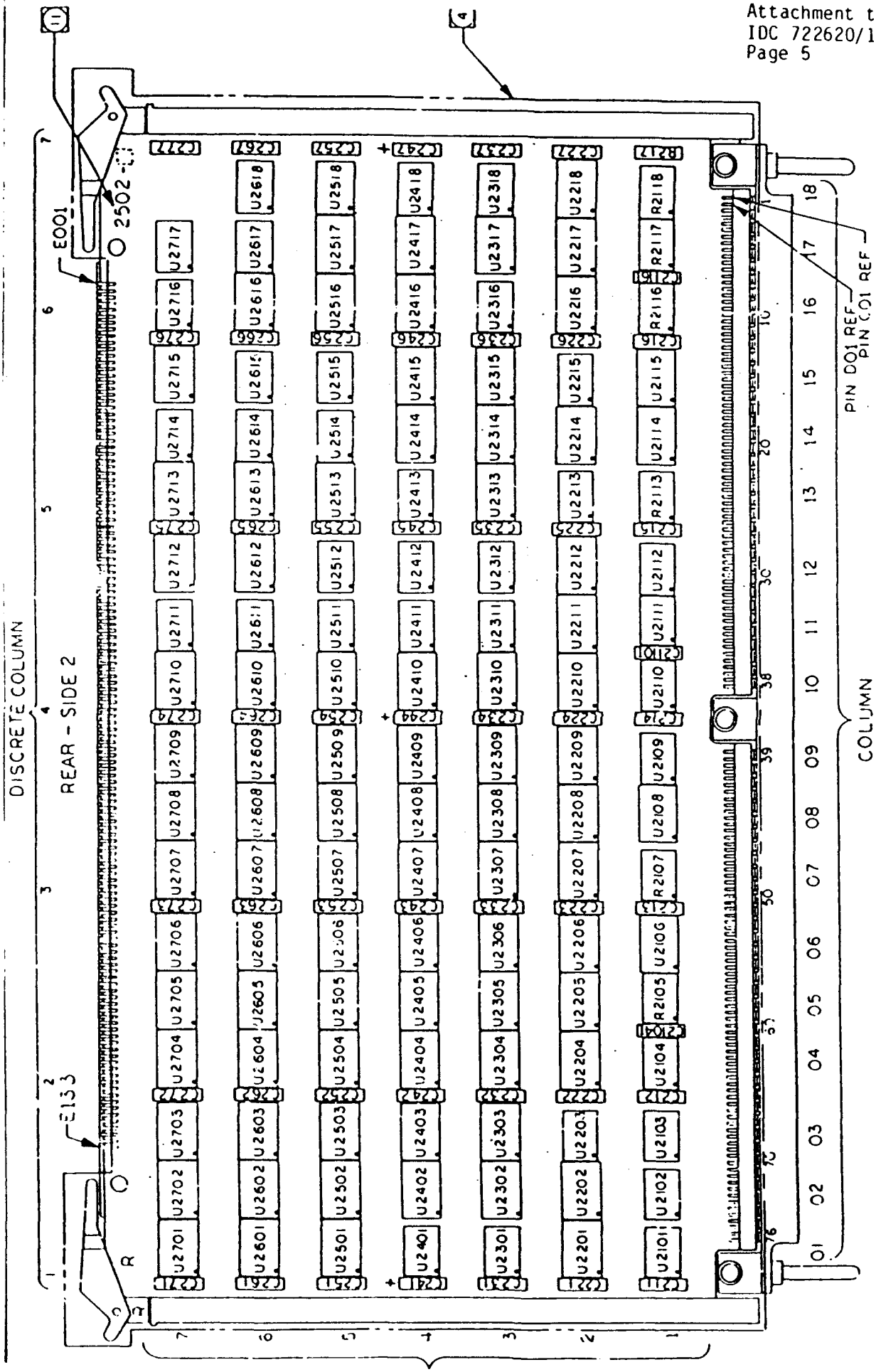


FIGURE F-2. COMPONENT LAYOUT - REAR SIDE 2

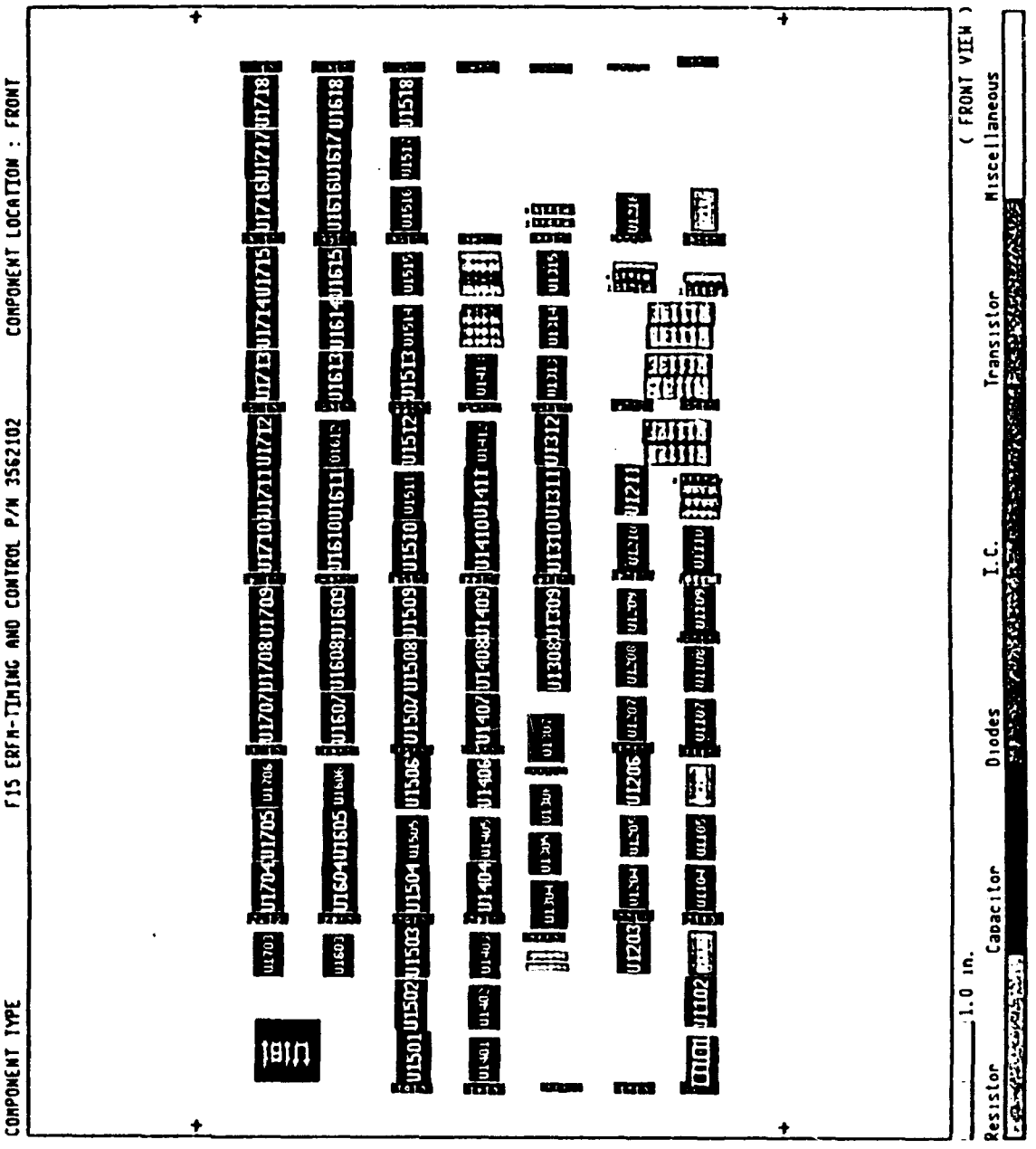


FIGURE F-3. COMPONENT LAYOUT – FRONT SIDE 1

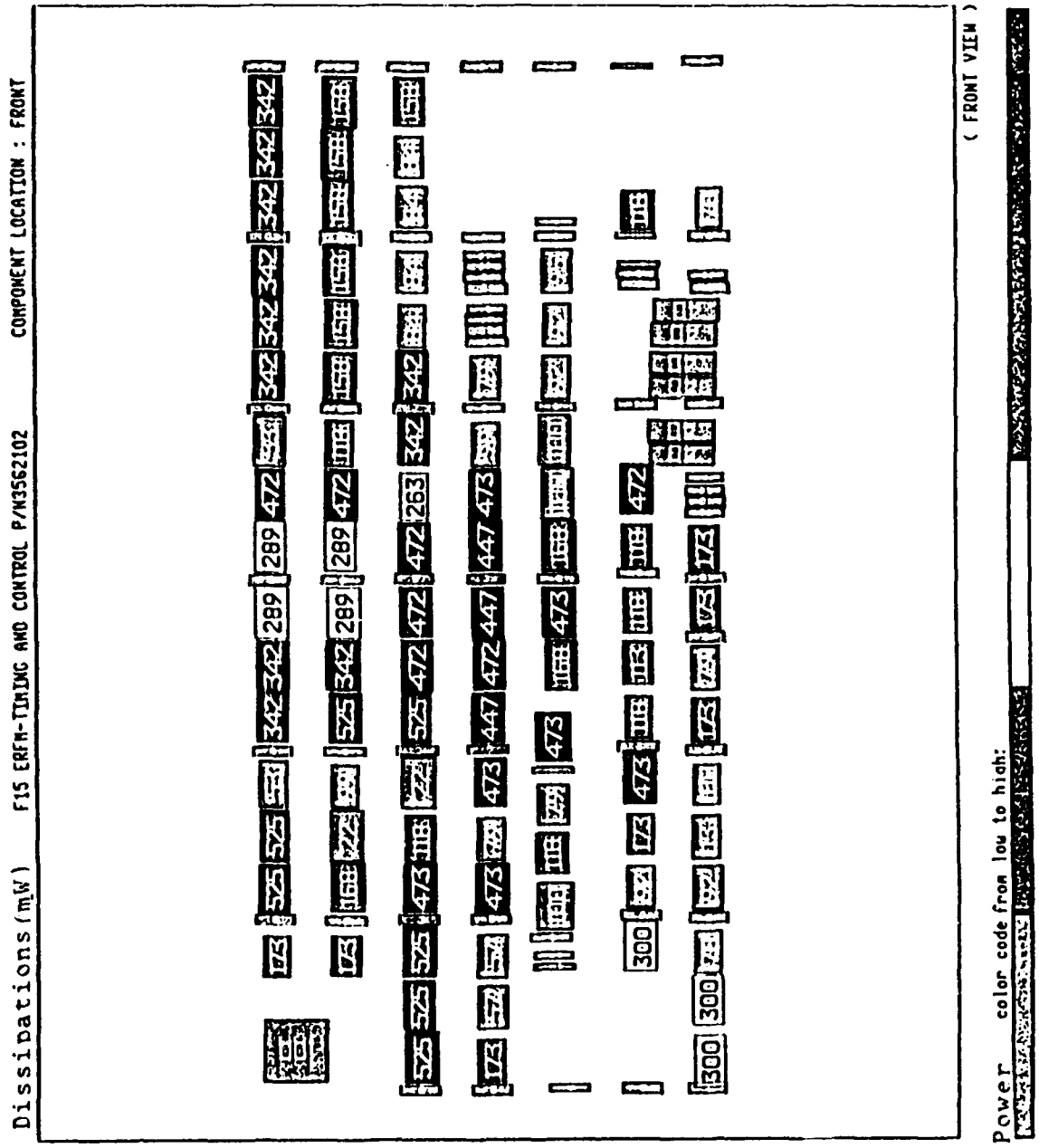


FIGURE F-4. COMPONENT DISSIPATIONS – FRONT SIDE 1

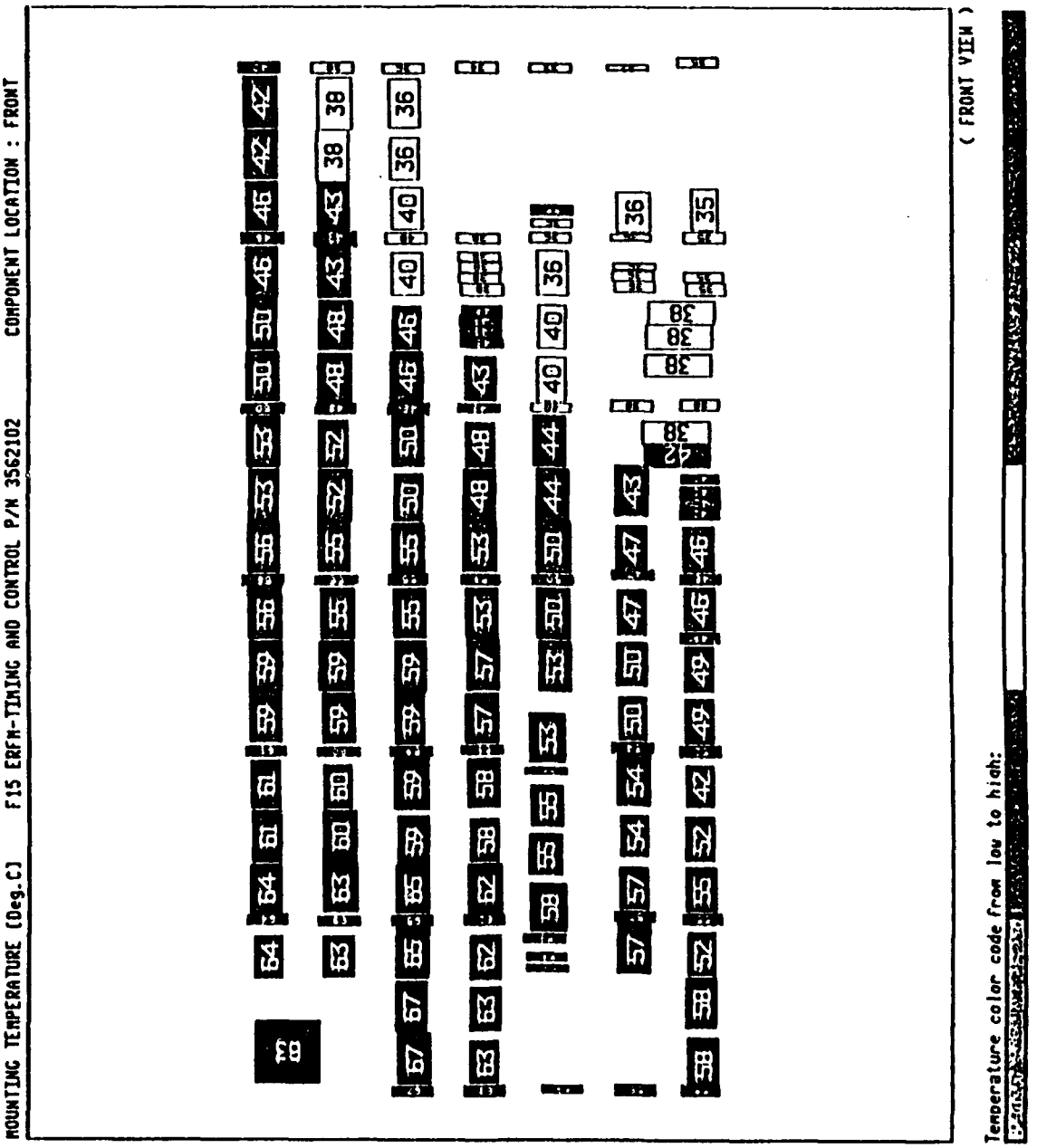


FIGURE F-5. MOUNTING SURFACE TEMPERATURES – FRONT SIDE 1

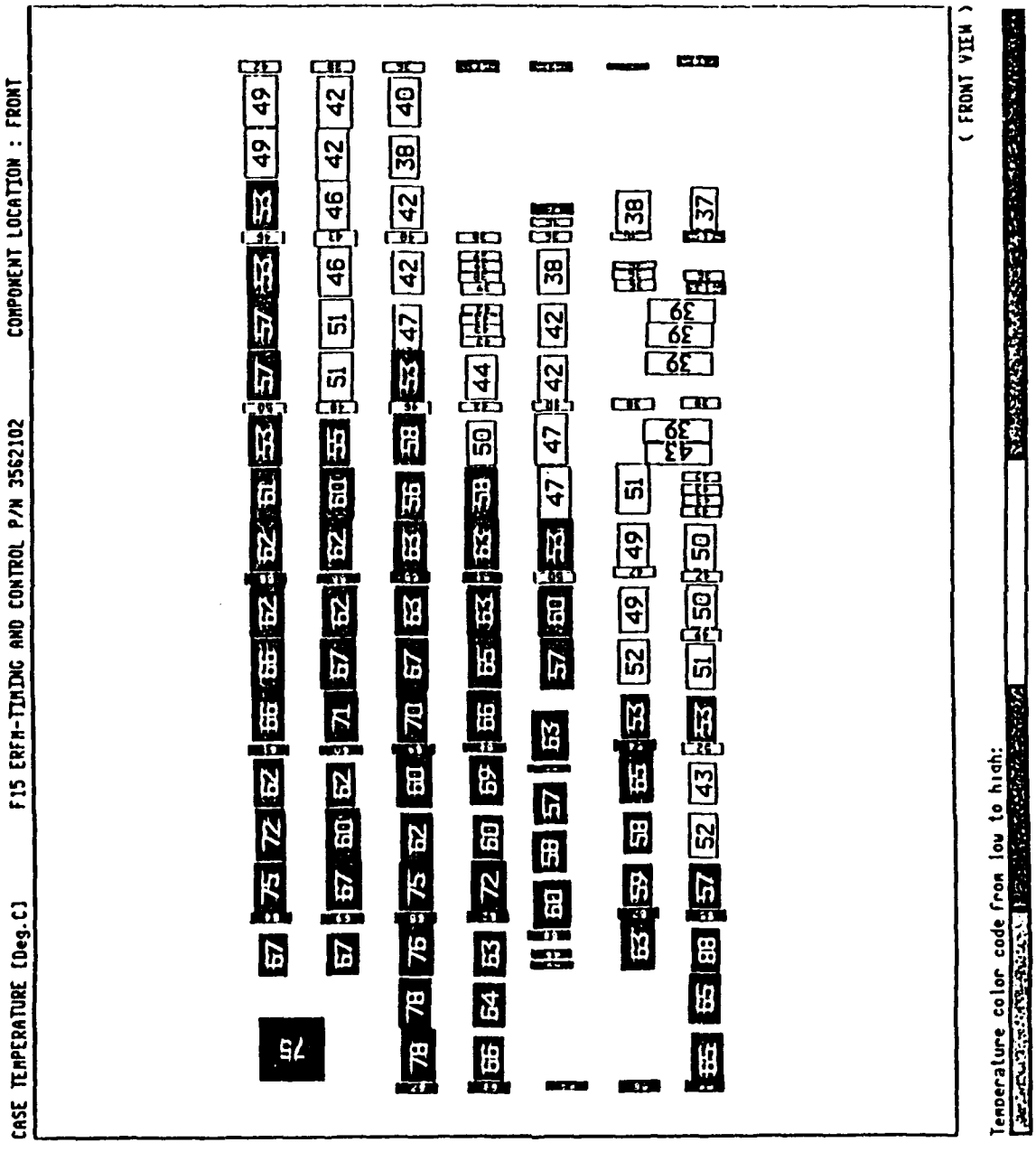


FIGURE F-6. CASE TEMPERATURE – FRONT SIDE 1

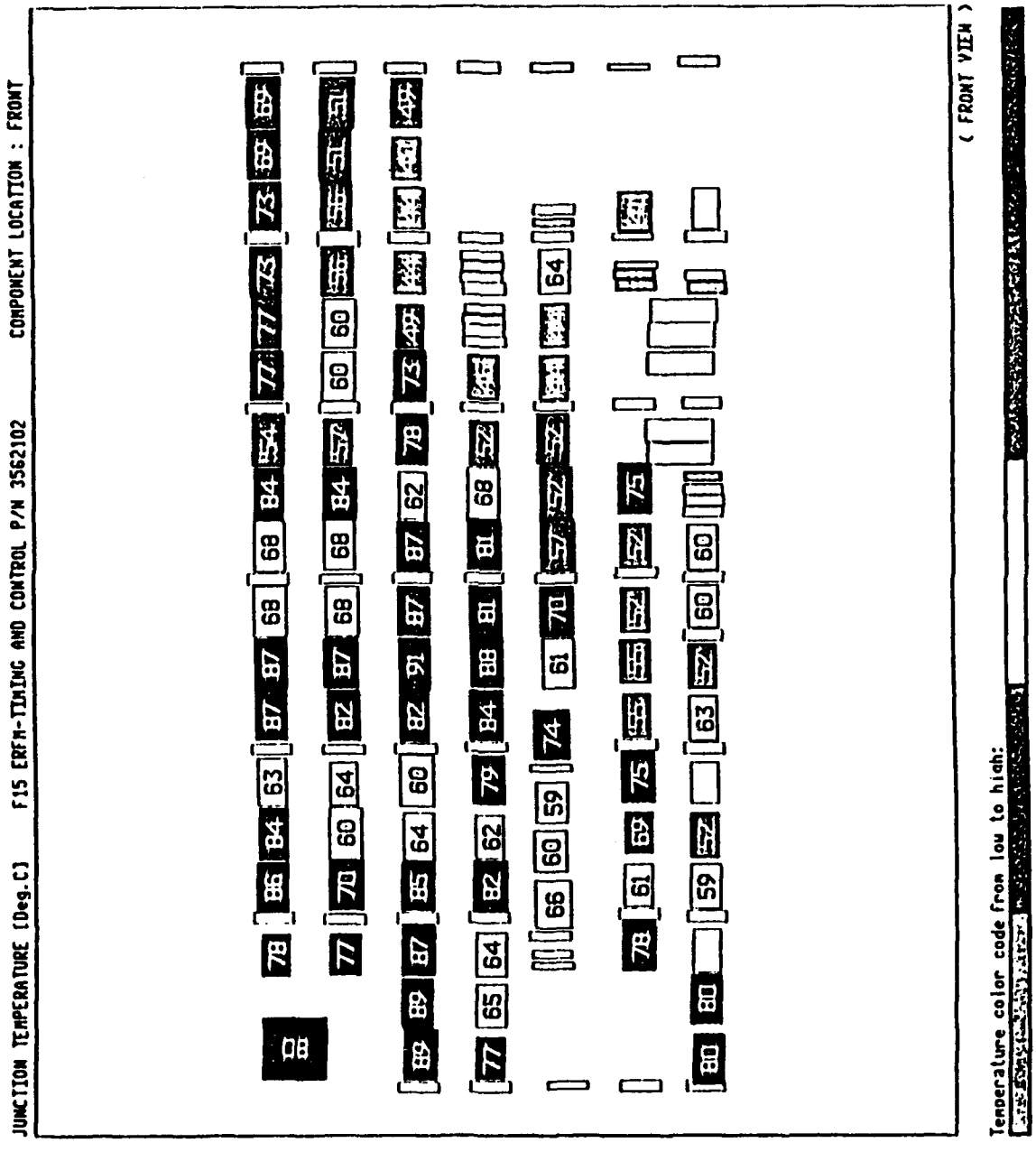


FIGURE F-7. JUNCTION TEMPERATURE – FRONT SIDE

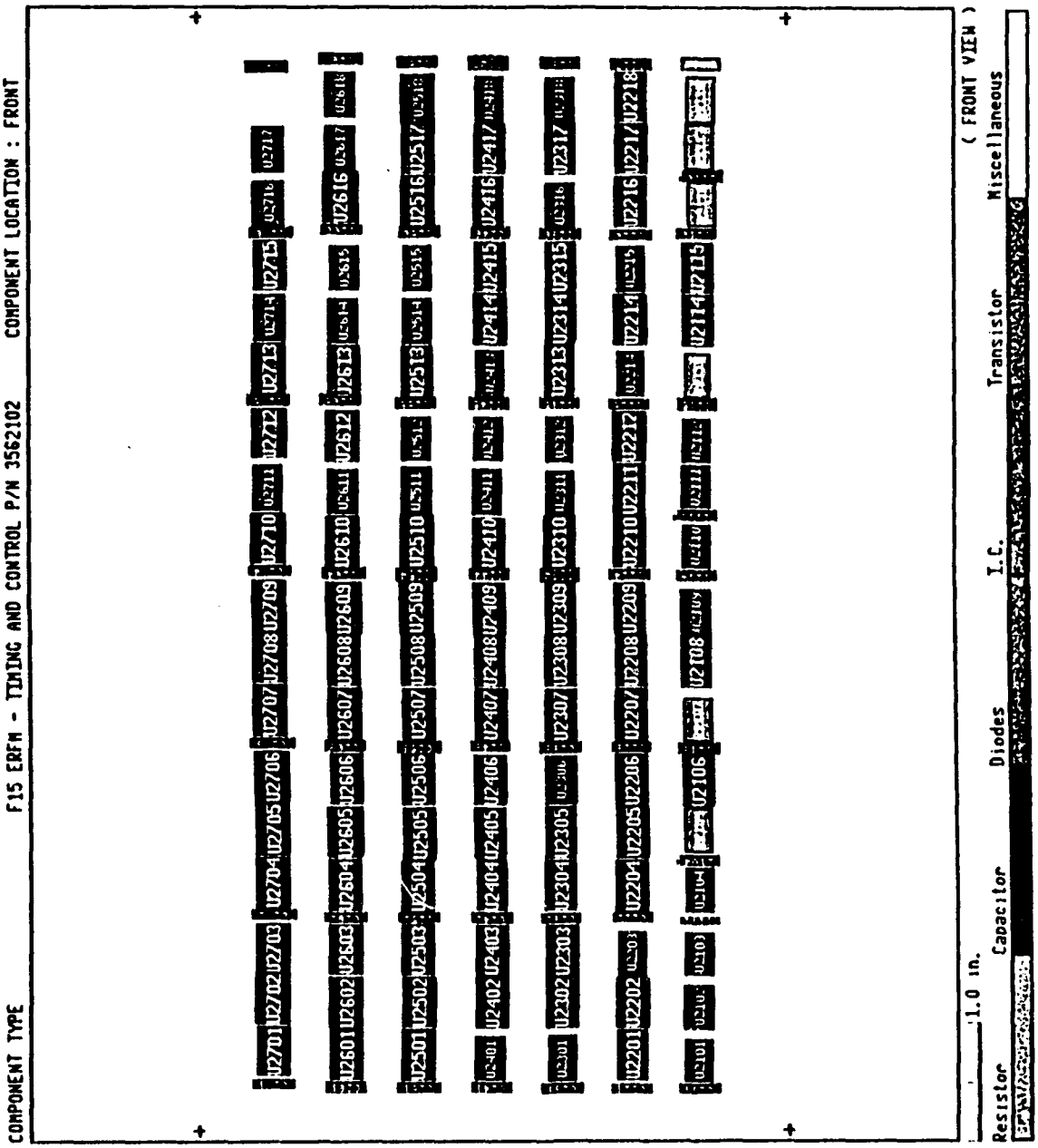


FIGURE F-8. COMPONENT LAYOUT – REAR SIDE 2

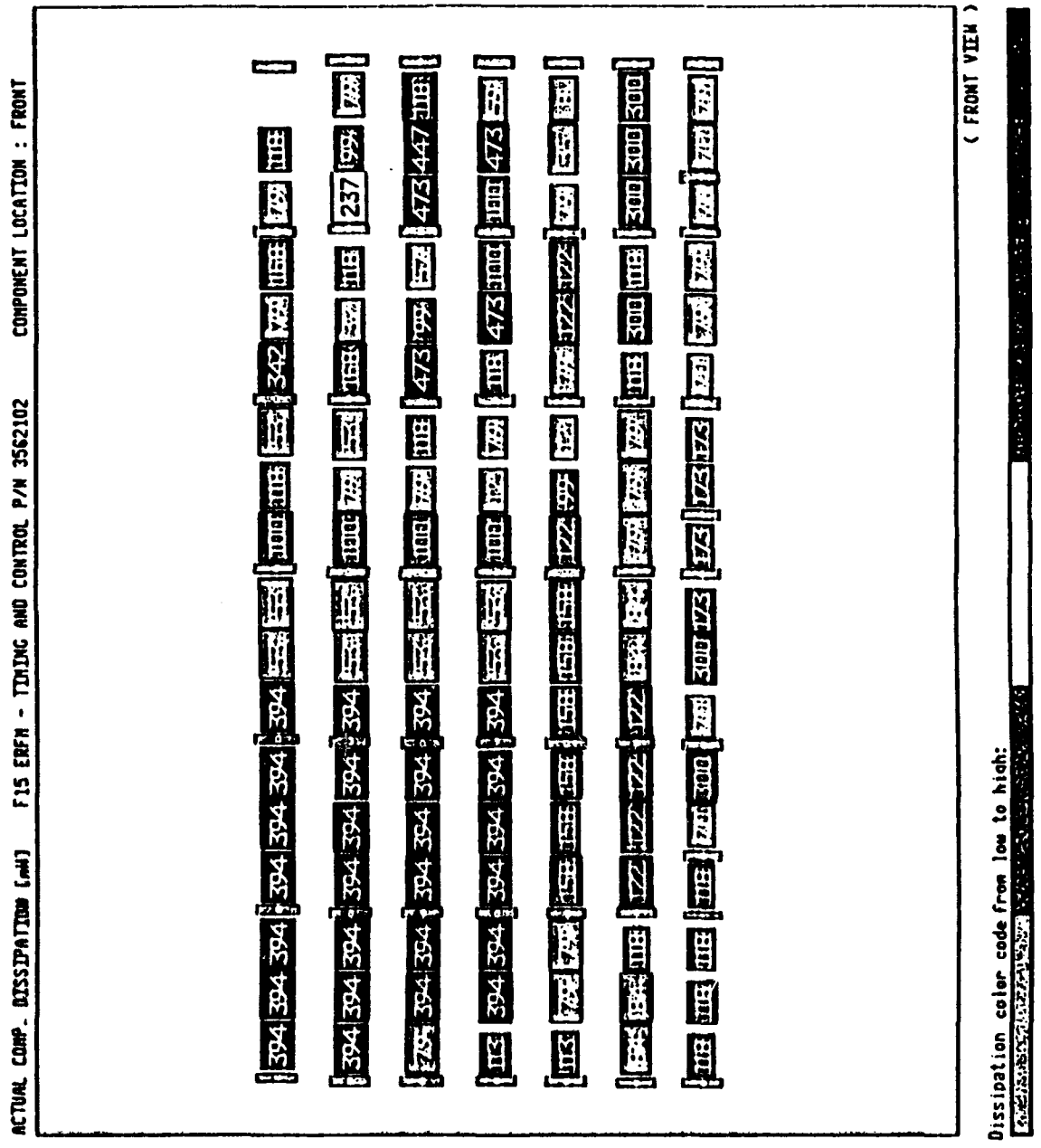


FIGURE F-9. COMPONENT DISSIPATIONS – REAR SIDE 2

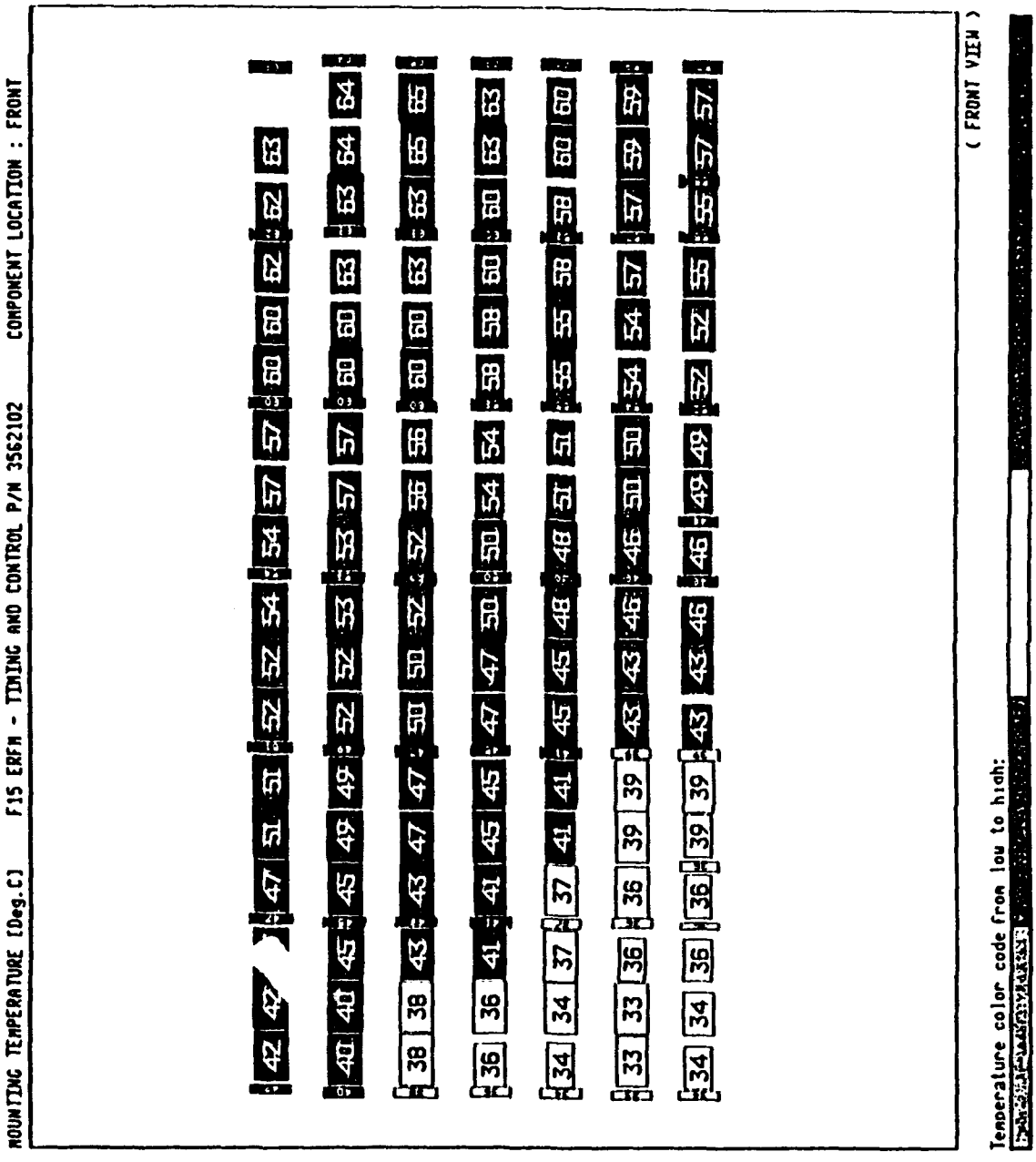


FIGURE F-10. MOUNTING SURFACE TEMPERATURE – REAR SIDE 2

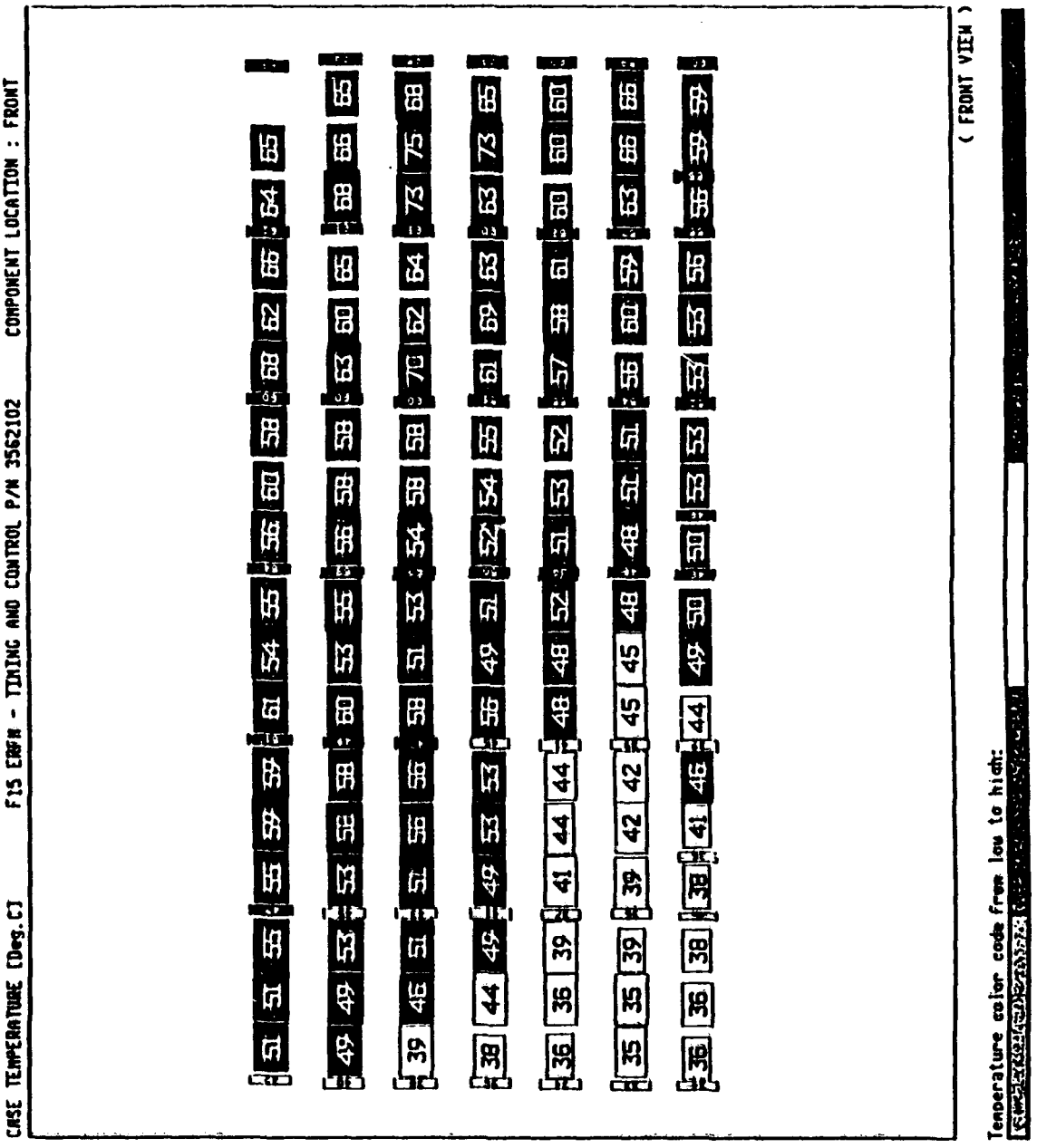


FIGURE F-11. CASE TEMPERATURE – REAR SIDE 2

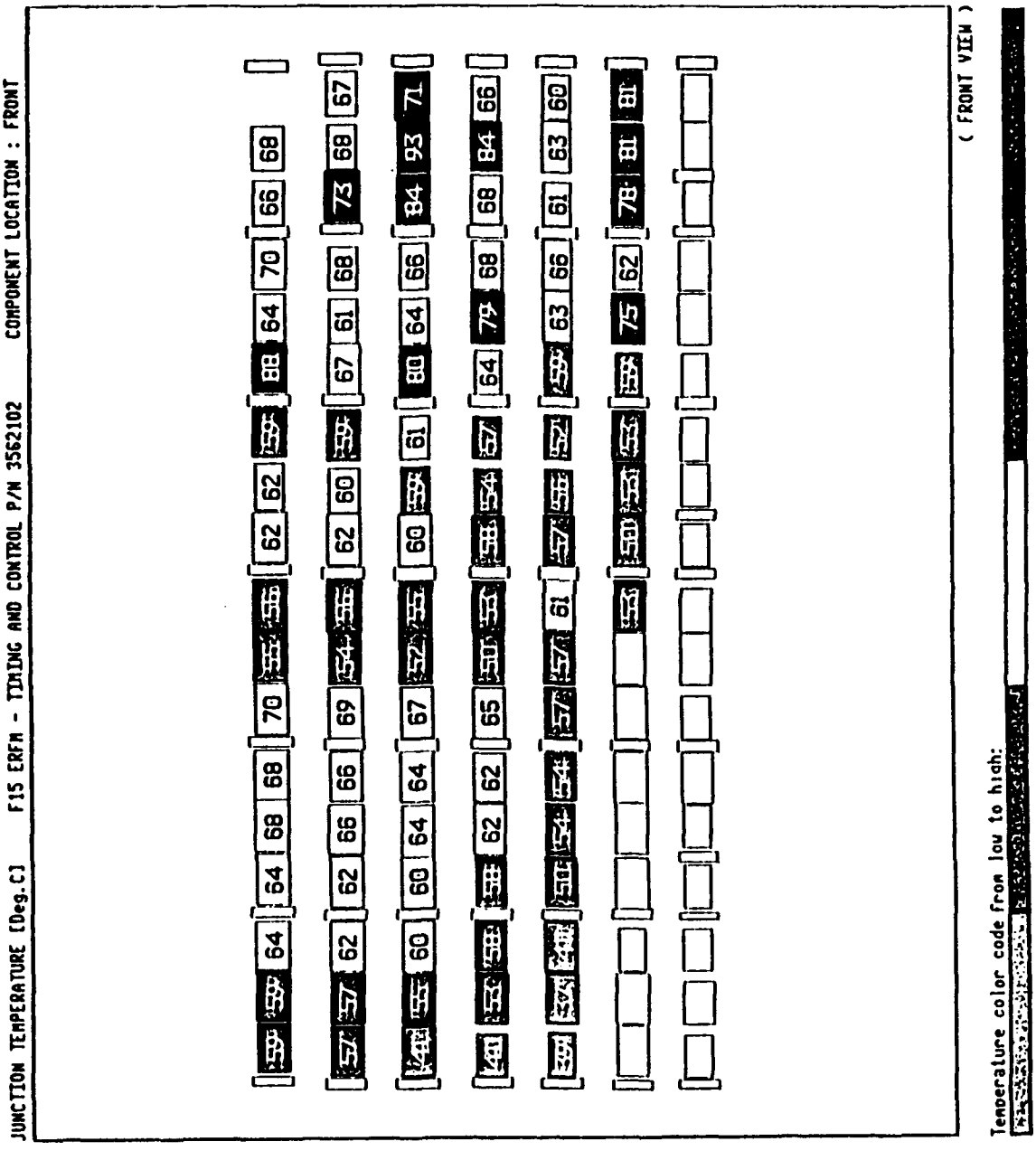


FIGURE F-12. JUNCTION TEMPERATURE – REAR SIDE 2

TABLE F-1

F-15 TIMING AND CONTROL
STEADY STATE

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1108I	905570-73B	0.000	49.	49.	
C111	M39003/02-0079	0.000	58.	58.	
C112	905570-73B	0.000	55.	55.	
C113	905570-73B	0.000	52.	52.	
C115	905570-73B	0.000	38.	38.	
C116	905570-73B	0.000	35.	35.	
C117	M39003/02-0079	0.000	35.	35.	
C121	905570-73B	0.000	58.	58.	
C122	905570-73B	0.000	57.	57.	
C123	905570-73B	0.000	54.	54.	
C124	M39003/02-0079	0.000	47.	47.	
C125	905570-73B	0.000	38.	38.	
C126	905570-73B	0.000	36.	36.	
C127	905570-73B	0.000	32.	32.	
C131	905570-73B	0.000	59.	59.	
C132	905570-73B	0.000	58.	58.	
C133	905570-73B	0.000	55.	55.	
C134	905570-73B	0.000	50.	50.	
C135	905570-73B	0.000	40.	40.	
C136	905570-73B	0.000	36.	36.	
C137	905570-73B	0.000	33.	33.	
C141	M39003/02-0068	0.000	63.	63.	
C1414G	M39003/02-0087	0.000	43.	43.	
C1415C	905570-73B	0.000	38.	38.	
C142	905570-73B	0.000	62.	62.	
C143	905570-73B	0.000	58.	58.	
C144	M39003/02-0068	0.000	53.	53.	
C145	905570-73B	0.000	43.	43.	
C146	905570-73B	0.000	38.	38.	
C147	M39003/02-0068	0.000	34.	34.	
C151	905570-73B	0.000	67.	67.	
C152	905570-73B	0.000	65.	65.	
C153	905570-73B	0.000	59.	59.	
C154	905570-73B	0.000	55.	55.	
C155	905570-73B	0.000	46.	46.	
C156	905570-73B	0.000	40.	40.	
C157	905570-73B	0.000	36.	36.	
C162	905570-73B	0.000	63.	63.	
C163	905570-73B	0.000	60.	60.	
C164	905570-73B	0.000	55.	55.	
C165	905570-73B	0.000	48.	48.	

TABLE F-1 (Continued)

F-15 TIMING AND CONTROL
STEADY STATE

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C166	905570-73B	0.000	43.	43.	
C167	905570-73B	0.000	38.	38.	
C172	905570-73B	0.000	64.	64.	
C173	905570-73B	0.000	61.	61.	
C174	905570-73B	0.000	56.	56.	
C175	905570-73B	0.000	50.	50.	
C176	905570-73B	0.000	46.	46.	
C177	905570-73B	0.000	42.	42.	
C2104I	905570-73B	0.000	36.	36.	
C211	905570-73B	0.000	34.	34.	
C2110I	905570-73B	0.000	46.	46.	
C2116I	905570-73B	0.000	55.	55.	
C212	905570-73B	0.000	36.	36.	
C213	905570-73B	0.000	39.	39.	
C214	905570-73B	0.000	46.	46.	
C215	905570-73B	0.000	52.	52.	
C216	905570-73B	0.000	55.	55.	
C221	905570-73B	0.000	33.	33.	
C222	905570-73B	0.000	36.	36.	
C223	905570-73B	0.000	39.	39.	
C224	905570-73B	0.000	46.	46.	
C225	905570-73B	0.000	54.	54.	
C226	905570-73B	0.000	57.	57.	
C227	905570-73B	0.000	59.	59.	
C231	905570-73B	0.000	34.	34.	
C232	905570-73B	0.000	37.	37.	
C233	905570-73B	0.000	41.	41.	
C234	905570-73B	0.000	48.	48.	
C235	905570-73B	0.000	55.	55.	
C236	905570-73B	0.000	58.	58.	
C237	905570-73B	0.000	60.	60.	
C241	M39003/02-0068	0.000	36.	36.	
C242	905570-73B	0.000	41.	41.	
C243	905570-73B	0.000	45.	45.	
C244	M39003/02-0068	0.000	50.	50.	
C245	905570-73B	0.000	58.	58.	
C246	905570-73B	0.000	60.	60.	
C247	M39003/02-0068	0.000	63.	63.	
C251	905570-73B	0.000	38.	38.	
C252	905570-73B	0.000	43.	43.	
C253	905570-73B	0.000	47.	47.	

TABLE F-1 (Continued)

F-15 TIMING AND CONTROL
STEADY STATE

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C254	905570-73B	0.000	52.	52.	
C255	905570-73B	0.000	60.	60.	
C256	905570-73B	0.000	63.	63.	
C257	905570-73B	0.000	65.	65.	
C261	905570-73B	0.000	40.	40.	
C262	905570-73B	0.000	45.	45.	
C263	905570-73B	0.000	49.	49.	
C264	905570-73B	0.000	53.	53.	
C265	905570-73B	0.000	60.	60.	
C266	905570-73B	0.000	63.	63.	
C267	905570-73B	0.000	64.	64.	
C271	905570-73B	0.000	42.	42.	
C272	905570-73B	0.000	47.	47.	
C273	905570-73B	0.000	51.	51.	
C274	905570-73B	0.000	54.	54.	
C275	905570-73B	0.000	60.	60.	
C276	905570-73B	0.000	62.	62.	
C277	905570-73B	0.000	63.	63.	
CR1111G	JANTX1N4150-1	0.000	42.	42.	42.
CR1115A	JANTX1N4150-1	0.000	35.	35.	35.
CR1215A	JANTX1N4150-1	0.000	36.	36.	36.
CR1215C	JANTX1N4150-1	0.000	36.	36.	36.
CR1316A	925974-1B	0.000	36.	36.	36.
R1103	M8340103M27ROJA	0.070	55.	56.	
R1106	955230-8B	0.100	52.	88.	
R1111A	RCR07G101JS	0.040	42.	43.	
R1111C	RCR07G512JS	0.040	42.	43.	
R1111E	RCR07G100JS	0.040	42.	43.	
R1112B	RLR32C348FP	0.040	42.	43.	
R1112F	RLR32C348FP	0.040	42.	43.	
R1113B	RLR32C348FP	0.040	38.	39.	
R1113F	RLR32C348FP	0.040	38.	39.	
R1114B	RLR32C348FP	0.040	38.	39.	
R1114F	RLR32C348FP	0.040	38.	39.	
R1115C	RCR07G100JS	0.040	35.	36.	
R1116	M8340103M27ROJA	0.070	35.	37.	
R114	RCR07G121JS	0.040	46.	47.	
R1215E	RCR07G270JS	0.040	36.	36.	
R1303E	RCR07G270JS	0.040	58.	59.	
R1303G	RCR07G270JS	0.040	58.	59.	
R1414A	RCR07G152JS	0.040	43.	43.	

TABLE F-1 (Continued)

F-15 TIMING AND CONTROL
STEADY STATE

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
R1414C	RCR07G102JS	0.040	43.	43.	
R1414E	RCR07G100JS	0.040	43.	43.	
R1415A	RCR07G392JS	0.040	38.	39.	
R1415E	RCR07G820JS	0.040	38.	39.	
R1415G	RCR07G330JS	0.040	38.	39.	
R217	RNC50H3161FS	0.070	57.	60.	
R2105	M8340103M27ROJA	0.070	39.	41.	
R2107	M8340103M27ROJA	0.070	43.	44.	
R2113	M8340103M27ROJA	0.070	52.	53.	
R2116	M8340103M27ROJA	0.070	55.	56.	
R2117	M8340103M27ROJA	0.070	57.	59.	
R2118	M8340103M27ROJA	0.070	57.	59.	
U1101	932849-1B	0.300	58.	65.	80.
U1102	932849-1B	0.300	58.	65.	80.
U1104	932783-2B	0.092	55.	57.	59.
U1105	M38510/30003BDX	0.013	52.	52.	52.
U1107	932730-2B	0.173	49.	53.	63.
U1108	M38510/07001BDX	0.079	49.	51.	52.
U1109	932730-2B	0.173	46.	50.	60.
U1110	932730-2B	0.173	46.	50.	60.
U1203	932849-1B	0.300	57.	63.	78.
U1204	932783-2B	0.092	57.	59.	61.
U1205	932730-2B	0.173	54.	58.	69.
U1206	932614-3B	0.473	54.	65.	75.
U1207	M38510/07003BDX	0.118	50.	53.	55.
U1208	M38510/07301BDX	0.113	50.	52.	55.
U1209	M38510/07003BDX	0.118	47.	49.	52.
U1210	M38510/07003BDX	0.118	47.	49.	52.
U1211	932820-226	0.472	43.	51.	75.
U1216	M38510/07003BDX	0.118	36.	38.	41.
U1304	932616-501B	0.100	58.	60.	66.
U1305	M38510/07003BDX	0.118	55.	58.	60.
U1306	M38510/07001BDX	0.079	55.	57.	59.
U1307	932614-3B	0.473	53.	63.	74.
U1308	M38510/34102BFX	0.168	53.	57.	61.
U1309	932614-3B	0.473	50.	60.	70.
U1310	M38510/34102BFX	0.168	50.	53.	57.
U1311	932756-1B	0.100	44.	47.	52.
U1312	932756-1B	0.100	44.	47.	52.
U1313	932783-2B	0.092	40.	42.	44.
U1314	932783-2B	0.092	40.	42.	44.

TABLE F-1 (Continued)

F-15 TIMING AND CONTROL
STEADY STATE

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U1315	928063-501B	0.095	36.	38.	64.
U1401	932730-2B	0.173	63.	66.	77.
U1402	M38510/07401BDX	0.057	63.	64.	65.
U1403	M38510/07401BDX	0.057	62.	63.	64.
U1404	932614-3B	0.473	62.	72.	82.
U1405	M38510/07001BDX	0.079	58.	60.	62.
U1406	932614-3B	0.473	58.	69.	79.
U1407	932727-1B	0.447	57.	66.	84.
U1408	932820-218	0.472	57.	65.	88.
U1409	932727-1B	0.447	53.	63.	81.
U1410	932727-1B	0.447	53.	63.	81.
U1411	932614-3B	0.473	48.	58.	68.
U1412	M38510/08001BDX	0.099	48.	50.	52.
U1413	M38510/07001BDX	0.079	43.	44.	46.
U1501	932709-1B	0.525	67.	78.	89.
U1502	932709-1B	0.525	67.	78.	89.
U1503	932709-1B	0.525	65.	76.	87.
U1504	932614-3B	0.473	65.	75.	85.
U1505	M38510/07003BDX	0.118	59.	62.	64.
U1506	M38510/07009BFX	0.022	59.	60.	60.
U1507	932709-1B	0.525	59.	70.	82.
U1508	932820-217	0.472	59.	67.	91.
U1509	932820-219	0.472	55.	63.	87.
U1510	932820-220	0.472	55.	63.	87.
U1511	M38510/07501BDX	0.263	50.	56.	62.
U1512	932746-1B	0.342	50.	58.	78.
U1513	932746-1B	0.342	46.	53.	73.
U1514	M38510/30605BDX	0.084	46.	47.	49.
U1515	M38510/30605BDX	0.084	40.	42.	44.
U1516	M38510/30605BDX	0.084	40.	42.	44.
U1517	M38510/30605BDX	0.084	36.	38.	40.
U1518	932749-1B	0.158	36.	40.	49.
U1601	930739-1B	0.100	63.	75.	80.
U1603	932730-2B	0.173	63.	67.	77.
U1604	M38510/54102BFX	0.168	63.	67.	70.
U1605	M38510/07009BFX	0.022	60.	60.	60.
U1606	M38510/08001BDX	0.099	60.	62.	64.
U1607	932709-1B	0.525	59.	71.	82.
U1608	932746-1B	0.342	59.	67.	87.
U1609	932732-1B	0.289	55.	62.	68.
U1610	932732-1B	0.289	55.	62.	68.

TABLE F-1 (Continued)

F-15 TIMING AND CONTROL
STEADY STATE

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U1611	932820-215	0.472	52.	60.	84.
U1612	M38510/07003BDX	0.118	52.	55.	57.
U1613	932749-1B	0.158	48.	51.	60.
U1614	932749-1B	0.158	48.	51.	60.
U1615	932749-1B	0.158	43.	46.	56.
U1616	932749-1B	0.158	43.	46.	56.
U1617	932749-1B	0.158	38.	42.	51.
U1618	932749-1B	0.158	38.	42.	51.
U1703	932730-2B	0.173	64.	67.	78.
U1704	932709-1B	0.525	64.	75.	86.
U1705	932709-1B	0.525	61.	72.	84.
U1706	932690-1B	0.053	61.	62.	63.
U1707	932746-1B	0.342	59.	66.	87.
U1708	932746-1B	0.342	59.	66.	87.
U1709	932732-1B	0.289	56.	62.	68.
U1710	932732-1B	0.289	56.	62.	68.
U1711	932820-224	0.472	53.	61.	84.
U1712	M38510/33701BFX	0.033	53.	53.	54.
U1713	932746-1B	0.342	50.	57.	77.
U1714	932746-1B	0.342	50.	57.	77.
U1715	932746-1B	0.342	46.	53.	73.
U1716	932746-1B	0.342	46.	53.	73.
U1717	932746-1B	0.342	42.	49.	69.
U1718	932746-1B	0.342	42.	49.	69.
U2101	M38510/07003BDX	0.118	34.	36.	39.
U2102	M38510/07003BDX	0.118	34.	36.	39.
U2103	M38510/07003BDX	0.118	36.	38.	41.
U2104	M38510/07003BDX	0.118	36.	38.	41.
U2106	932849-1B	0.300	39.	46.	61.
U2108	932849-1B	0.300	43.	49.	64.
U2109	932730-2B	0.173	46.	50.	60.
U2110	932730-2B	0.173	46.	50.	60.
U2111	932730-2B	0.173	49.	53.	63.
U2112	932730-2B	0.173	49.	53.	63.
U2114	932728-1B	0.079	52.	53.	55.
U2115	932728-1B	0.079	55.	56.	58.
U2201	932726-1B	0.084	33.	35.	40.
U2202	932726-1B	0.084	33.	35.	40.
U2203	M38510/07003BDX	0.118	36.	39.	41.
U2204	H990436-001B	0.122	36.	39.	44.
U2205	H990436-001B	0.122	39.	42.	48.

TABLE F-1 (Continued)

F-15 TIMING AND CONTROL
STEADY STATE

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U2206	H990436-001B	0.122	39.	42.	48.
U2207	H990436-001B	0.122	43.	45.	51.
U2208	932726-1B	0.084	43.	45.	49.
U2209	932726-1B	0.084	46.	48.	53.
U2210	932728-1B	0.079	46.	48.	50.
U2211	932728-1B	0.079	50.	51.	53.
U2212	932728-1B	0.079	50.	51.	53.
U2213	M38510/07003BDX	0.118	54.	56.	59.
U2214	932849-1B	0.300	54.	60.	75.
U2215	M38510/07003BDX	0.118	57.	59.	62.
U2216	932849-1B	0.300	57.	63.	78.
U2217	932849-1B	0.300	59.	66.	81.
U2218	932849-1B	0.300	59.	66.	81.
U2301	M38510/07301BDX	0.113	34.	36.	39.
U2302	932728-1B	0.079	34.	36.	37.
U2303	932728-1B	0.079	37.	39.	41.
U2304	932749-1B	0.158	37.	41.	50.
U2305	932749-1B	0.158	41.	44.	54.
U2306	932749-1B	0.158	41.	44.	54.
U2307	932749-1B	0.158	45.	48.	57.
U2308	932749-1B	0.158	45.	48.	57.
U2309	932749-1B	0.158	48.	52.	61.
U2310	H990436-001B	0.122	48.	51.	57.
U2311	M38510/08001BDX	0.099	51.	53.	56.
U2312	M38510/30301BDX	0.012	51.	52.	52.
U2313	932728-1B	0.079	55.	57.	59.
U2314	H990436-001B	0.122	55.	58.	63.
U2315	H990436-001B	0.122	58.	61.	66.
U2316	M38510/07001BDX	0.079	58.	60.	61.
U2317	932685-1B	0.035	60.	60.	63.
U2318	M38510/30001BDX	0.008	60.	60.	60.
U2401	M38510/07301BDX	0.113	36.	38.	41.
U2402	932736-1B	0.394	36.	44.	53.
U2403	932736-1B	0.394	41.	49.	58.
U2404	932736-1B	0.394	41.	49.	58.
U2405	932736-1B	0.394	45.	53.	62.
U2406	932736-1B	0.394	45.	53.	62.
U2407	932736-1B	0.394	47.	56.	65.
U2408	932690-1B	0.053	47.	49.	50.
U2409	932690-1B	0.053	50.	51.	53.
U2410	932756-1B	0.100	50.	52.	58.

TABLE F-1 (Continued)

F-15 TIMING AND CONTROL
STEADY STATE

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U2411	M38510/30301BDX	0.012	54.	54.	54.
U2412	M38510/07001BDX	0.079	54.	55.	57.
U2413	M38510/07003BDX	0.118	58.	61.	64.
U2414	932614-3B	0.473	58.	69.	79.
U2415	932756-1B	0.100	60.	63.	68.
U2416	932756-1B	0.100	60.	63.	68.
U2417	932614-3B	0.473	63.	73.	84.
U2418	M38510/07005BDX	0.059	63.	65.	66.
U2501	932728-1B	0.079	38.	39.	41.
U2502	932736-1B	0.394	38.	46.	55.
U2503	932736-1B	0.394	43.	51.	60.
U2504	932736-1B	0.394	43.	51.	60.
U2505	932736-1B	0.394	47.	56.	64.
U2506	932736-1B	0.394	47.	56.	64.
U2507	932736-1B	0.394	50.	58.	67.
U2508	932690-1B	0.053	50.	51.	52.
U2509	932690-1B	0.053	52.	53.	55.
U2510	932756-1B	0.100	52.	54.	60.
U2511	M38510/07001BDX	0.079	56.	58.	59.
U2512	M38510/07003BDX	0.118	56.	58.	61.
U2513	932614-3B	0.473	60.	70.	80.
U2514	M38510/08001BDX	0.099	60.	62.	64.
U2515	M38510/07401BDX	0.057	63.	64.	66.
U2516	932614-3B	0.473	63.	73.	84.
U2517	932727-1B	0.447	65.	75.	93.
U2518	M38510/07003BDX	0.118	65.	68.	71.
U2601	932736-1B	0.394	40.	49.	57.
U2602	932736-1B	0.394	40.	49.	57.
U2603	932736-1B	0.394	45.	53.	62.
U2604	932736-1B	0.394	45.	53.	62.
U2605	932736-1B	0.394	49.	58.	66.
U2606	932736-1B	0.394	49.	58.	66.
U2607	932736-1B	0.394	52.	60.	69.
U2608	932690-1B	0.053	52.	53.	54.
U2609	932690-1B	0.053	53.	55.	56.
U2610	932756-1B	0.100	53.	56.	62.
U2611	M38510/07001BDX	0.079	57.	58.	60.
U2612	932690-1B	0.053	57.	58.	59.
U2613	M38510/34102BFX	0.168	60.	63.	67.
U2614	M38510/30502BDX	0.032	60.	60.	61.
U2615	M38510/07003BDX	0.118	63.	65.	68.

TABLE F-1 (Continued)

F-15 TIMING AND CONTROL
STEADY STATE

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U2616	M38510/33901BFX	0.237	63.	68.	73.
U2617	M38510/08001BDX	0.099	64.	66.	68.
U2618	M38510/07001BDX	0.079	64.	65.	67.
U2701	932736-1B	0.394	42.	51.	59.
U2702	932736-1B	0.394	42.	51.	59.
U2703	932736-1B	0.394	47.	55.	64.
U2704	932736-1B	0.394	47.	55.	64.
U2705	932736-1B	0.394	51.	59.	68.
U2706	932736-1B	0.394	51.	59.	68.
U2707	932736-1B	0.394	52.	61.	70.
U2708	932690-1B	0.053	52.	54.	55.
U2709	932690-1B	0.053	54.	55.	56.
U2710	932756-1B	0.100	54.	56.	62.
U2711	M38510/07003BDX	0.118	57.	60.	62.
U2712	932690-1B	0.053	57.	58.	59.
U2713	932746-1B	0.342	60.	68.	88.
U2714	M38510/07001BDX	0.079	60.	62.	64.
U2715	M38510/34102BFX	0.168	62.	66.	70.
U2716	M38510/07001BDX	0.079	62.	64.	66.
U2717	M38510/07003BDX	0.118	63.	65.	68.

TOTAL OF PART DISSIPATIONS: 47.766 WATTS

APPENDIX G

THERMAL ANALYSIS OF THE F-15 PSP LINEAR REGULATOR MODULE

INTERDEPARTMENTAL CORRESPONDENCE

TO: J. M. Kallis
ORG: 72-26

CC: Distribution

DATE: November 7, 1988
REF: 722620/1329

SUBJECT: Thermal Analysis of the F-15 PSP Linear Regulator Module

FROM: A. T. Bishop
ORG: 72-26-22

BLDG: E1 MAIL STA.: D105
LOC: EO PHONE: 616-1048

REFERENCE: AVO, "Power Dissipations of 3569800 Module," R. M. Nicoletti to J. Kallis, dated October 26, 1988.

SUMMARY

A detailed thermal analysis of the PSP Linear Regulator module on the Signal Processor unit for the F-15 aircraft has been performed. An independent thermal analysis was also completed for the three voltage regulator hybrids U1, U2, and U3 located on the module. The purpose of both analyses was to predict the nominal steady-state operating temperatures of all components. The resulting temperatures can then be used to aid the failure analysis of the module.

The total module power dissipation is 7.8 Watts. Of the total power dissipation, the hybrids U1, U2, and U3 dissipate 2.26 W, 1.03 W, and .037 W, respectively. The component dissipations were supplied by R. M. Nicoletti (27-36) in the reference. It should be noted that the component dissipations used in the analysis were calculated by using ±18 V inputs and maximum loads as defined in TS 31325-184. The inlet air is at 29.4°C (85°F) and the module air flow rate through the module was given as .167 lb/min by W. K. Hammond (72-26).

KEY RESULTS

The hottest discrete component on the printed wiring board is U4 with a junction temperature of 67°C. The hottest resistor is R3 with a case temperature of 64°C. The pass stage transistors located inside each of the hybrids U1, U2, U3 have junction temperatures of 44°C, 36°C, and 36°C, respectively.

A. T. Bishop, MTS
THERMODYNAMICS DEPARTMENT

Approved:
E. B. Curry, Section Head
THERMODYNAMICS DEPARTMENT

ATB:lcg

THERMAL ANALYSIS OF THE

F - 15 LINEAR REGULATOR MODULE

BY

A. T. BISHOP

INTRODUCTION

A detailed thermal analysis of the PSP Linear Regulator module on the Signal Processor unit for the F-15 aircraft has been performed. An independent thermal analysis was also completed for the three voltage regulator hybrids U1, U2, and U3 located on the module. The purpose of both analyses was to predict the nominal steady-state operating temperatures of all components. The resulting temperatures can then be used to aid the failure analysis of the module.

The total module power dissipation is 7.8 Watts. Of the total power dissipation, the hybrids U1, U2, and U3 dissipate 2.26 W, 1.03 W, and .037 W, respectively. The component dissipations were supplied by R. M. Nicoletti (27-36) in the reference. It should be noted that the component dissipations used in the analysis were calculated by using ±18 V inputs and maximum loads as defined in TS 31325-184. The inlet air is at 29.4°C (85°F) and the module air flow rate through the module was given as .167 lb/min by W. K. Hammond (72-26).

ANALYSIS INPUTS

Physical Design

The PSP Linear Regulator is a flow-through module that consists of a printed wiring board mounted on one side of a rectangular heat exchanger. The heat exchanger is 6.2 inches long, 5.0 inches wide, and .165 inches high. The heat exchanger is made of rectangular plate finstock (11.0R-.125-.50-.006A1) sandwiched between two 6061-T6 aluminum facesheets, each with a thickness of .02 inches.

A printed wiring board is bonded to one of the two aluminum facesheets in the module per the requirements of HPR42001/1 (which calls for material HMS 20-2010). The printed wiring board is made of .055 inch thick polyimide and includes a 1 ounce layer of copper. The components are mounted to the printed wiring board to meet the requirements of DP31367. Figure 1 shows the flow-through configuration of the Linear Regulator module.

Coldplate Dimensions-

Length,	6.2 inches
Width,	4.25 inches
Height,	0.125 inches

Fin Characteristics-

Pitch,	11
Height,	0.125 inches
Offset Length,	0.5 inches
Material Thickness,	0.006 inches

The positive and negative voltage regulator hybrids consist of a beryllia base layer with two smaller beryllia substrates mounted on top. All components are mounted to the substrates with the exception of Q7 which is mounted directly to the beryllia base layer. Figure 2 shows the component layout inside the hybrid.

Thermal Configuration

The heat originates in the components and then must travel through the case, leads and any bonding material present to the surface. The heat must then enter the board and be conducted to the heat exchanger. Finally the heat is conducted through the heat exchanger to the cooling air. The 29.4°C (85°F) cooling air is forced through the inlet guide of the module at a flow rate of 0.167 lb/min. It passes through the heat exchanger and receives the heat dissipated by the components.

Operating Conditions

Hybrid Power Dissipation (Total, 3 hybrids) 3.3 Watts
Remaining Module Dissipation 4.5 Watts

Cooling Air
Inlet Temperature 29.4°C (85°F)
Flow Rate 0.167 lb/min

The pass stage transistor Q7 located inside each hybrid dissipates 97% of the hybrid's total power dissipation. The remaining power is distributed among the other components inside the hybrid. In the analysis, it was assumed that all of the hybrid power dissipation exists in Q7. Furthermore, it was verified that the increased power density causes less than a 1°C temperature difference in the operating temperature of the transistor.

Material Properties

Material	Thermal Conductivity
Aluminum 6061-T6	4.0 W/in°C (91 BTU/hr-ft-°F)
Beryllia	6.3 W/in°C (143 BTU/hr-ft-°F)
Polyimide	
X-Y plane	0.021 W/in°C (0.47 BTU/hr-ft-°F)
Z direction	0.01 W/in°C (0.23 BTU/hr-ft-°F)
Copper	9.7 W/in°C (218 BTU/hr-ft-°F)
Sn/Pb Solder	1.25 W/in°C (28 BTU/hr-ft-°F)
HMS 20-2010	0.0066 W/in°C (0.15 BTU/hr-ft-°F)

Component bond material

HP16-103, Type VI	.0085 W/in°C

Hybrid bonding requirements

Assembly	Material	Conductivity
Chips to Substrate	Ablebond 606-2 HMS22-1683, Type III, cl.1	.057

Assembly	Material	Conductivity
Substrate to base layer	Ablefilm 506	.020
	HMS22-1682, Type IV	
Base layer to module facesheet	HP16-146	.004
	HP16-103, Type VI	.0085

Assumption

- Component Q7, located on each of the Voltage Regulator hybrids, is mounted to the beryllia base layer with Sn/Pb solder. All other component bonding requirements are specified above.
- It was assumed that all of the power dissipation in hybrids U1, U2, and U3 exists in the pass stage transistor Q7.

ANALYSIS METHOD

A mathematical model was built to represent the heat exchanger, the printed wiring boards and the airflow through the heat exchanger. The model was created to account for conduction and convection within and from the module. To model the air flow, one-way conductors were used. To calculate the convective heat transfer coefficient between the air flow and the heat exchanger, in-house computer software (COLDPLATE) was used. COLDPLATE is a program especially developed to determine the heat transfer coefficient, pressure drop, fin effectiveness and air exhaust temperature for a given fin, power, coldplate and cooling air conditions.

The model was analyzed using the Automated Thermal Data Processor (ATDP) computer program. This program incorporates the CINDA finite differencing thermal analysis program with a pre-processor developed specifically to calculate the mounting surface, case, and junction temperatures (where applicable) of each component.

The Voltage Regulator hybrids were analyzed with in-house computer software (HYBRID) that creates a thermal model based on data base input such as physical dimensions, material properties, and power dissipations. The program automatically creates nodes, calculates conductances, and determines component mounting resistances. HYBRID then yields a thermal model that can be analyzed with the CINDA finite differencing thermal analysis program to obtain results.

RESULTS

Table 1 provides the predicted operating component temperatures for the Linear Regulator module. Tables 2 through 4 include the operating temperatures of the components located inside hybrids U1, U2, and U3, respectively. These tables include the power dissipation, predicted mounting surface, case, and junction temperatures (where applicable). Figures 3 through 22 give the layouts, dissipations, mounting surface temperatures,case temperatures and junction temperatures for the components on the printed wiring board and inside the voltage regulator hybrids.

The hottest discrete component on the printed wiring board is U4 with a junction temperature of 67°C. The hottest resistor is R3 with a case temperature of 64°C. The pass stage transistors located inside each of the hybrids U1, U2, U3 have junction temperatures of 44°C, 36°C, and 36°C, respectively.

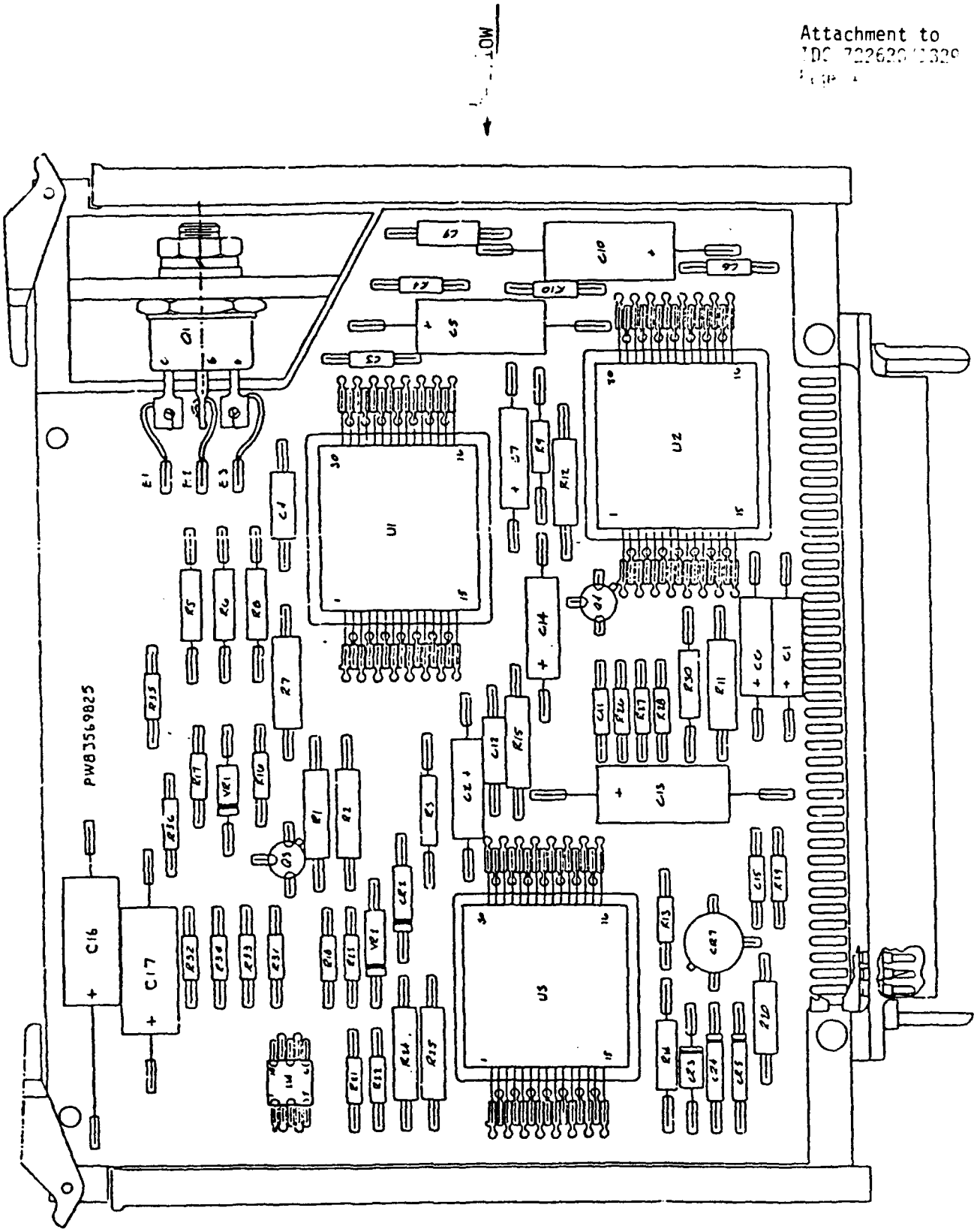


Figure G-1. F15 EFRM PSP Linear Regulator Module Component Layout on Printed Wiring Board

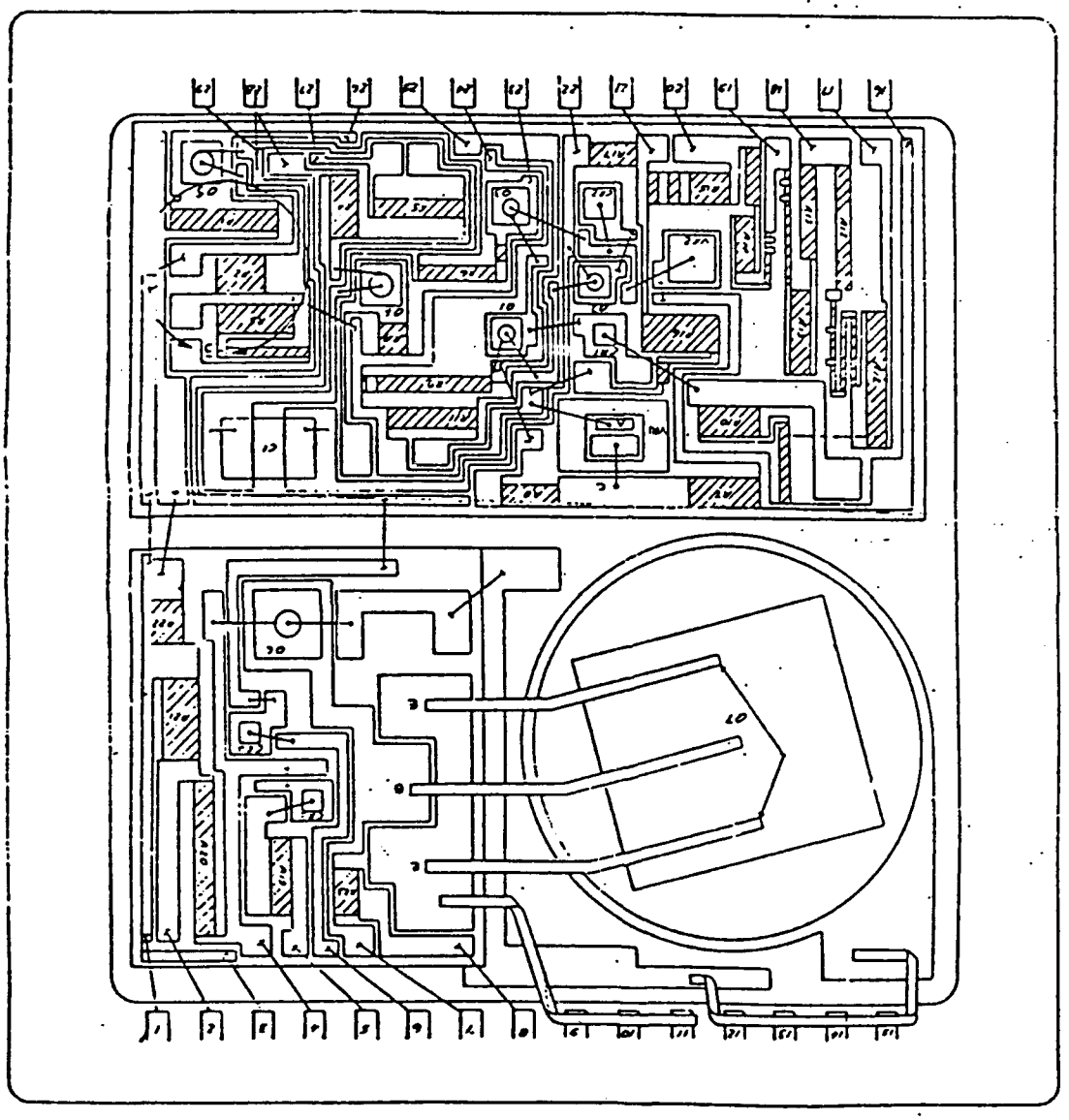


Figure G-2 Positive and Negative Voltage Regulator Hybrid Component Layout

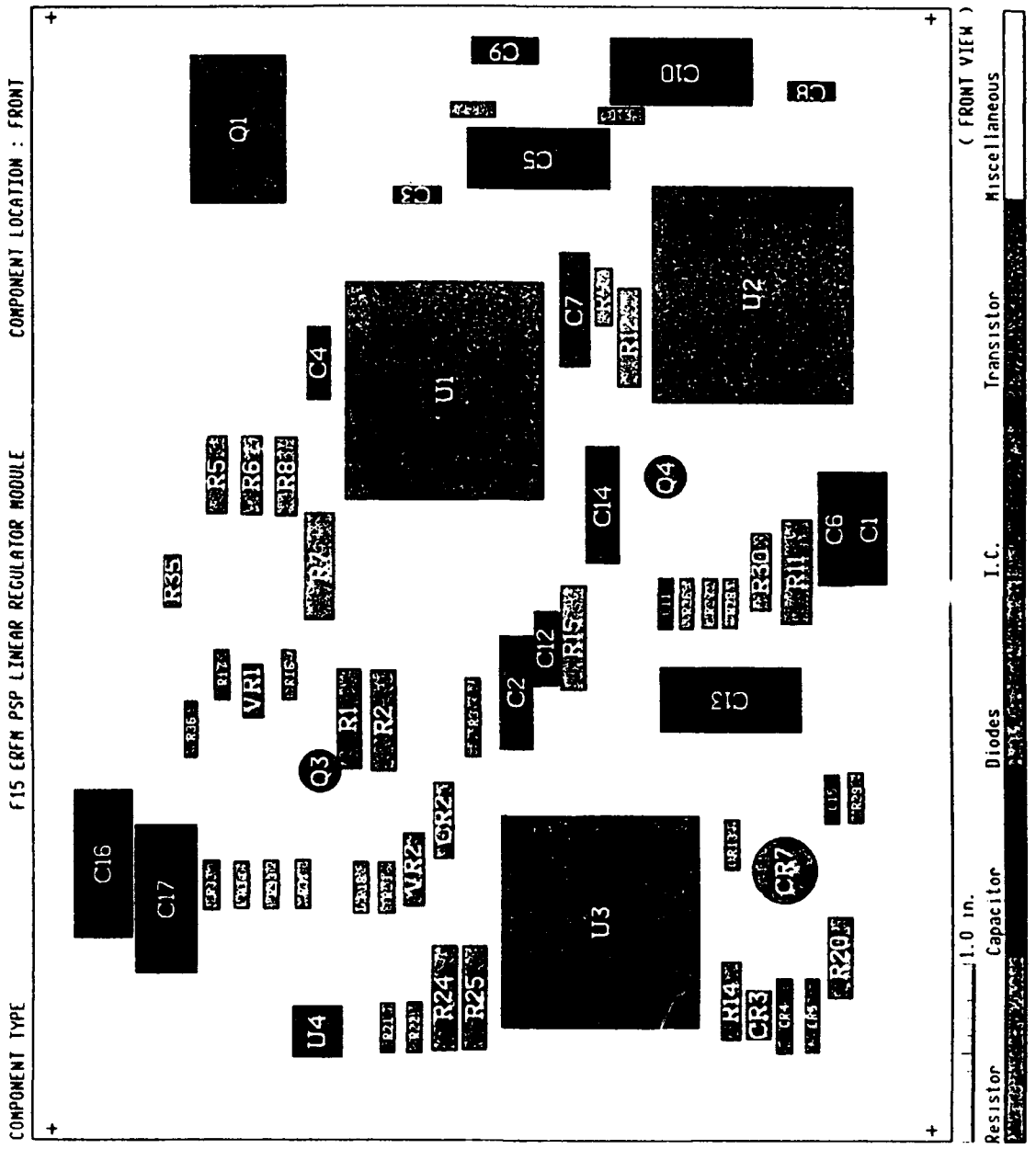


Figure G-3. Printed Wiring Board — Component Layout

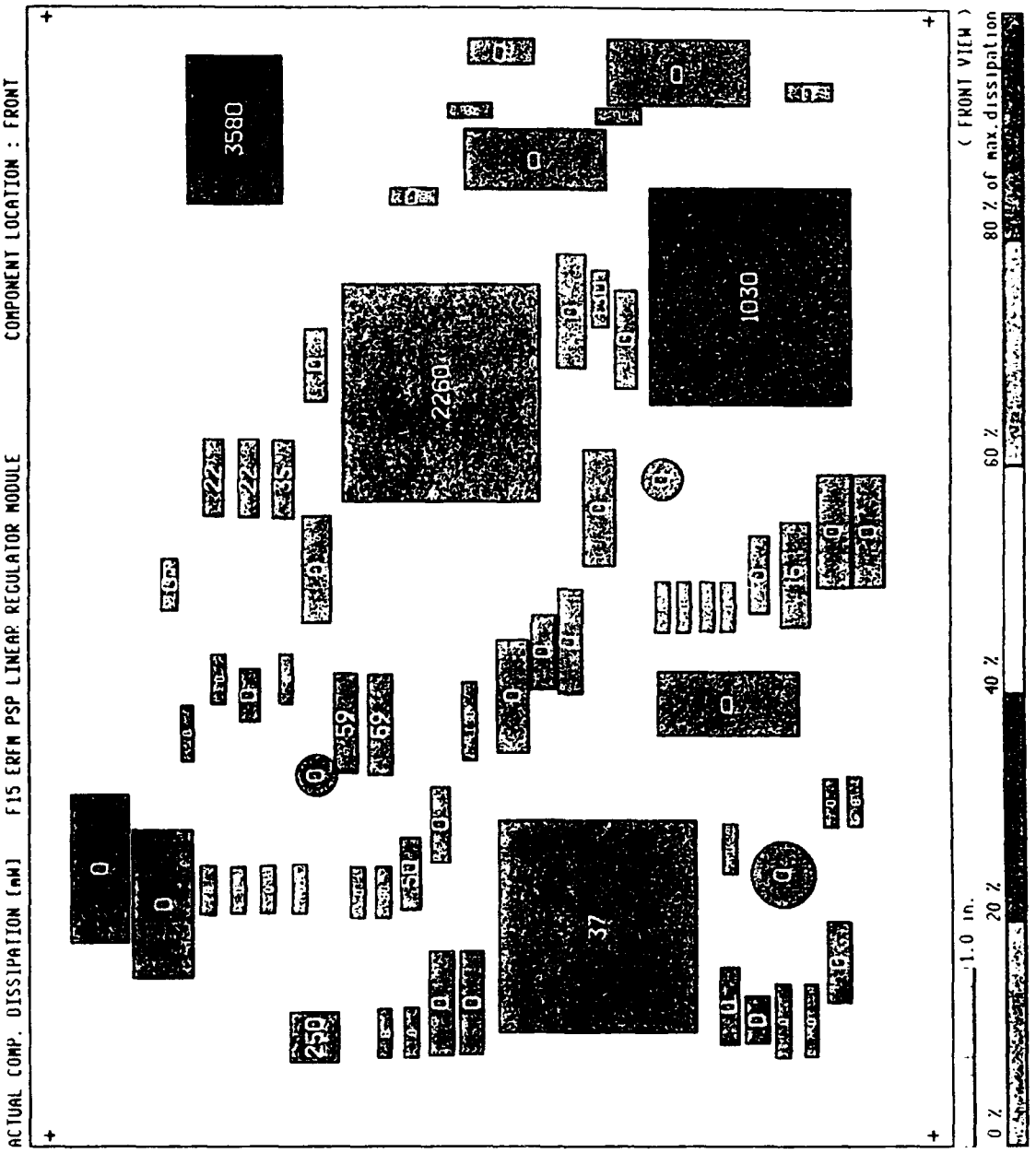


Figure G-4. Printed Wiring Board — Component Dissipations

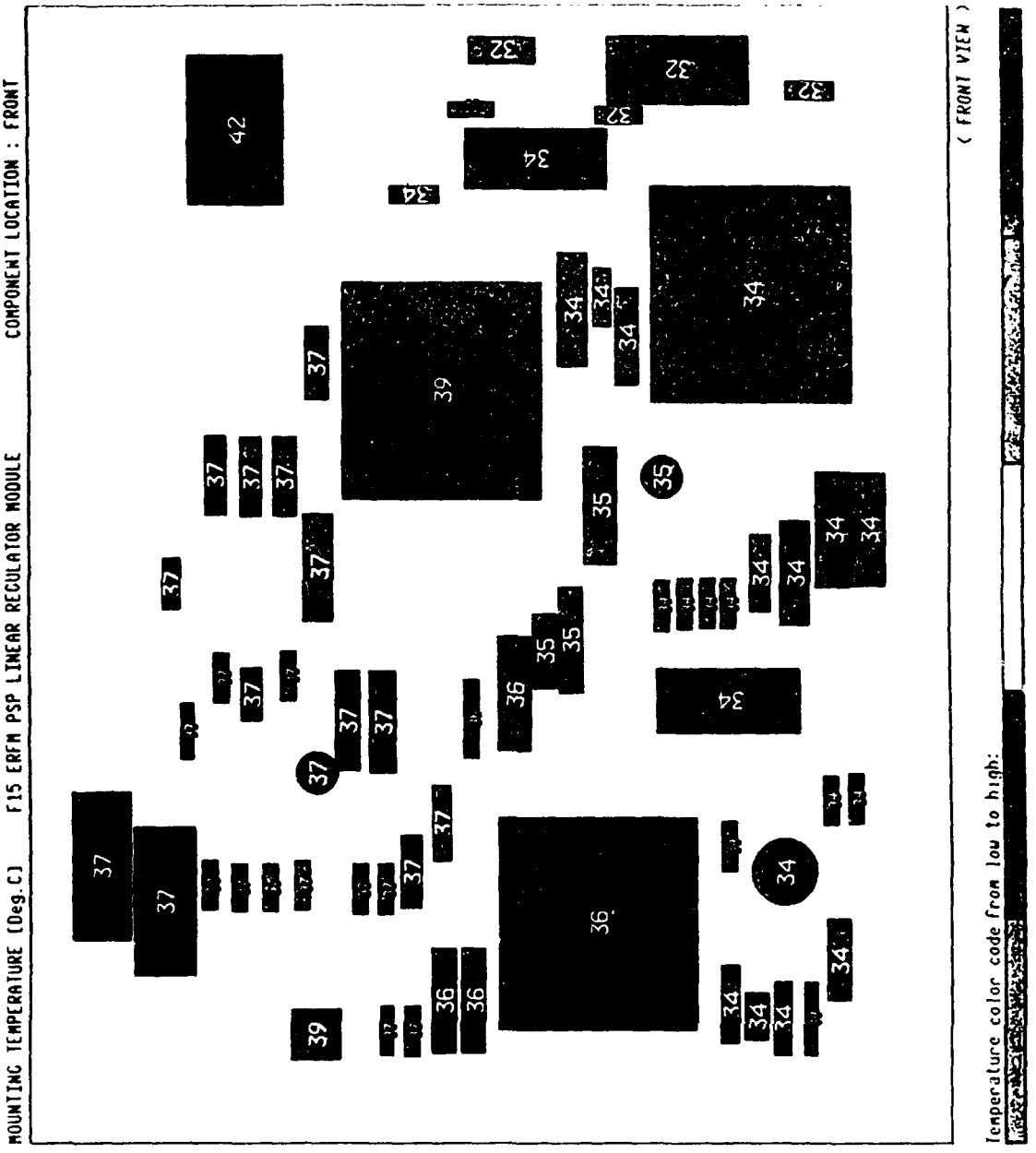


Figure G-5. Printed Wiring Board — Mounting Surface Temperatures

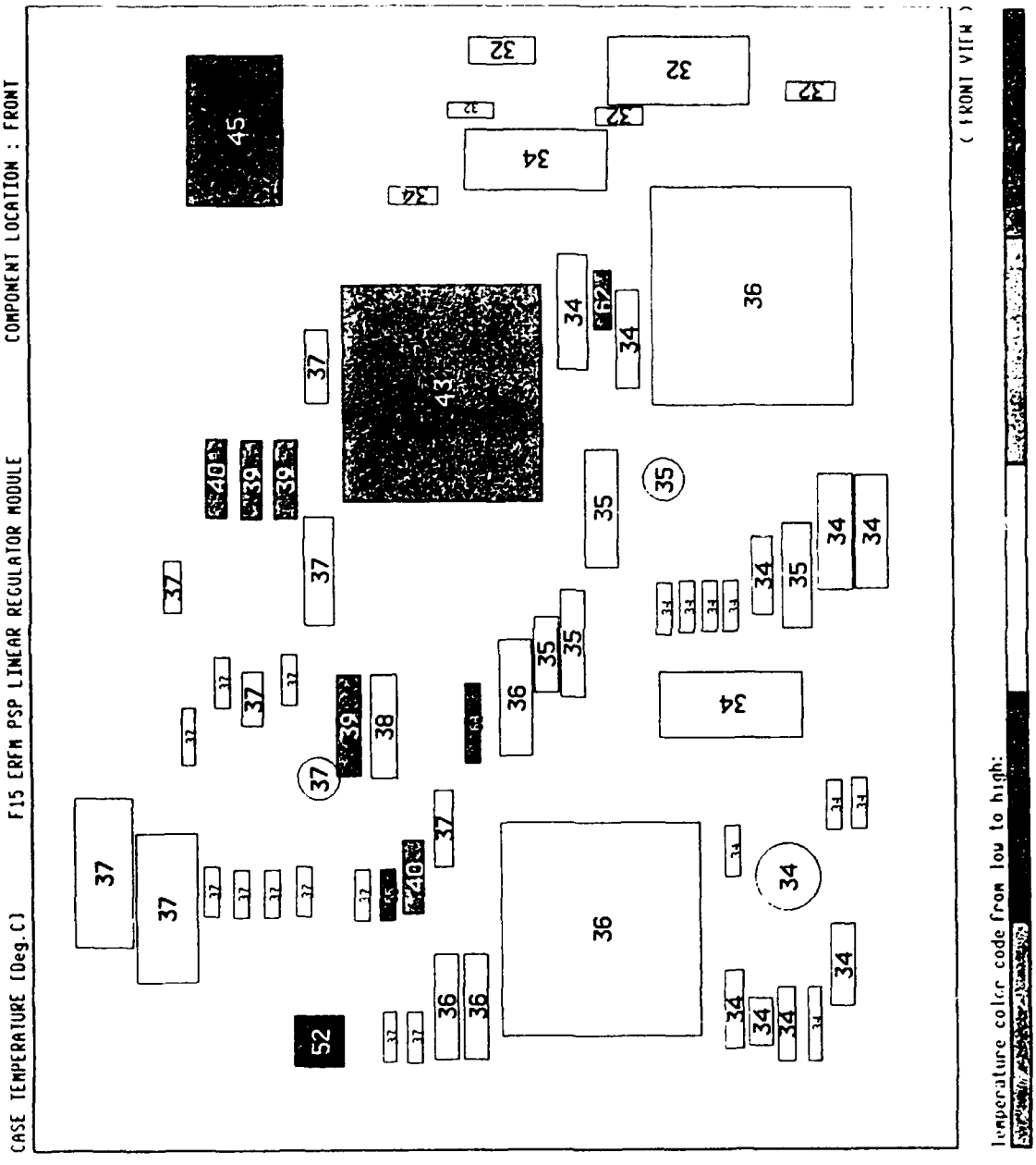


Figure G-6. Printed Wiring Board — Case Temperatures

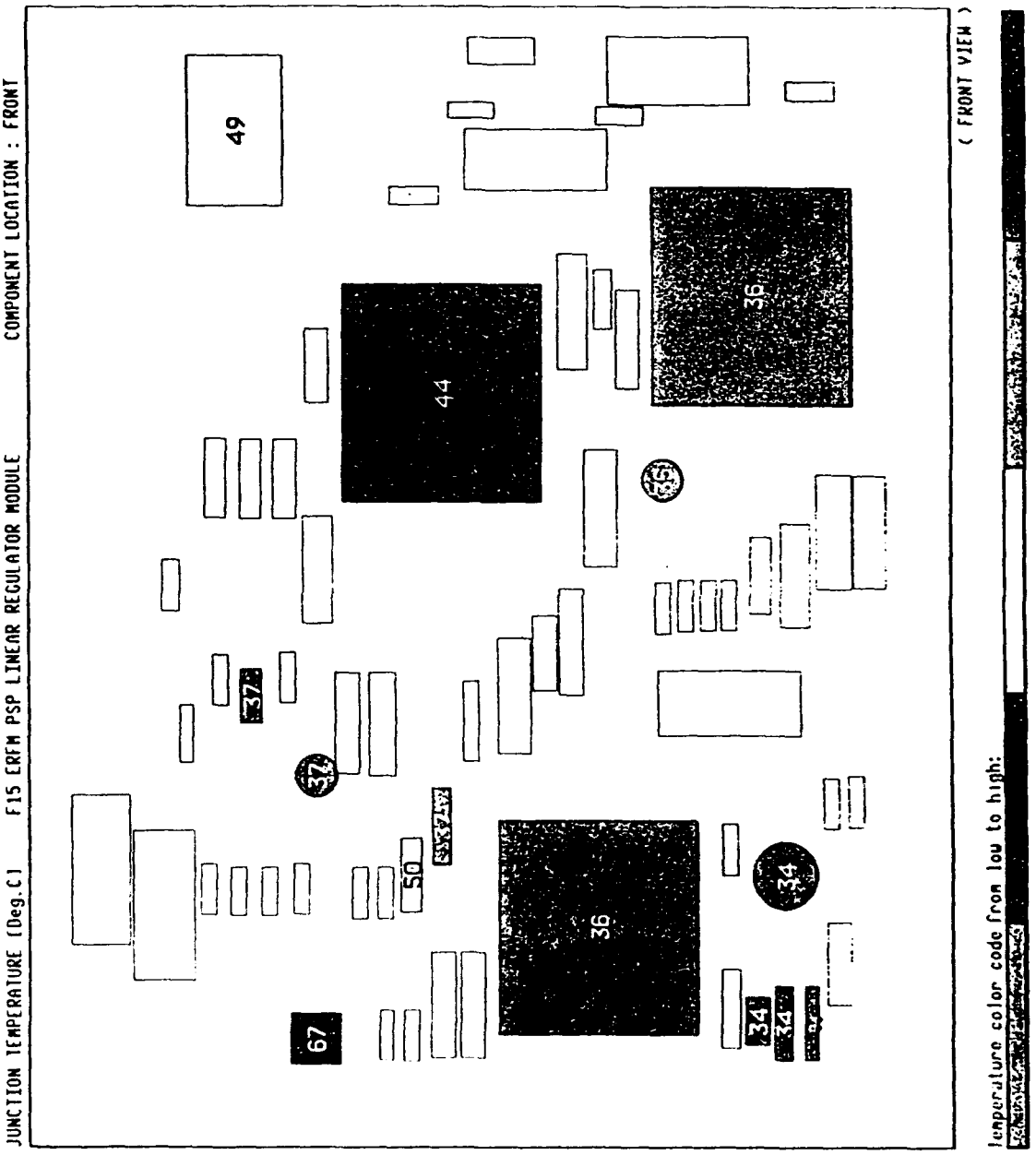


Figure G-7. Printed Wiring Board — Junction Temperatures

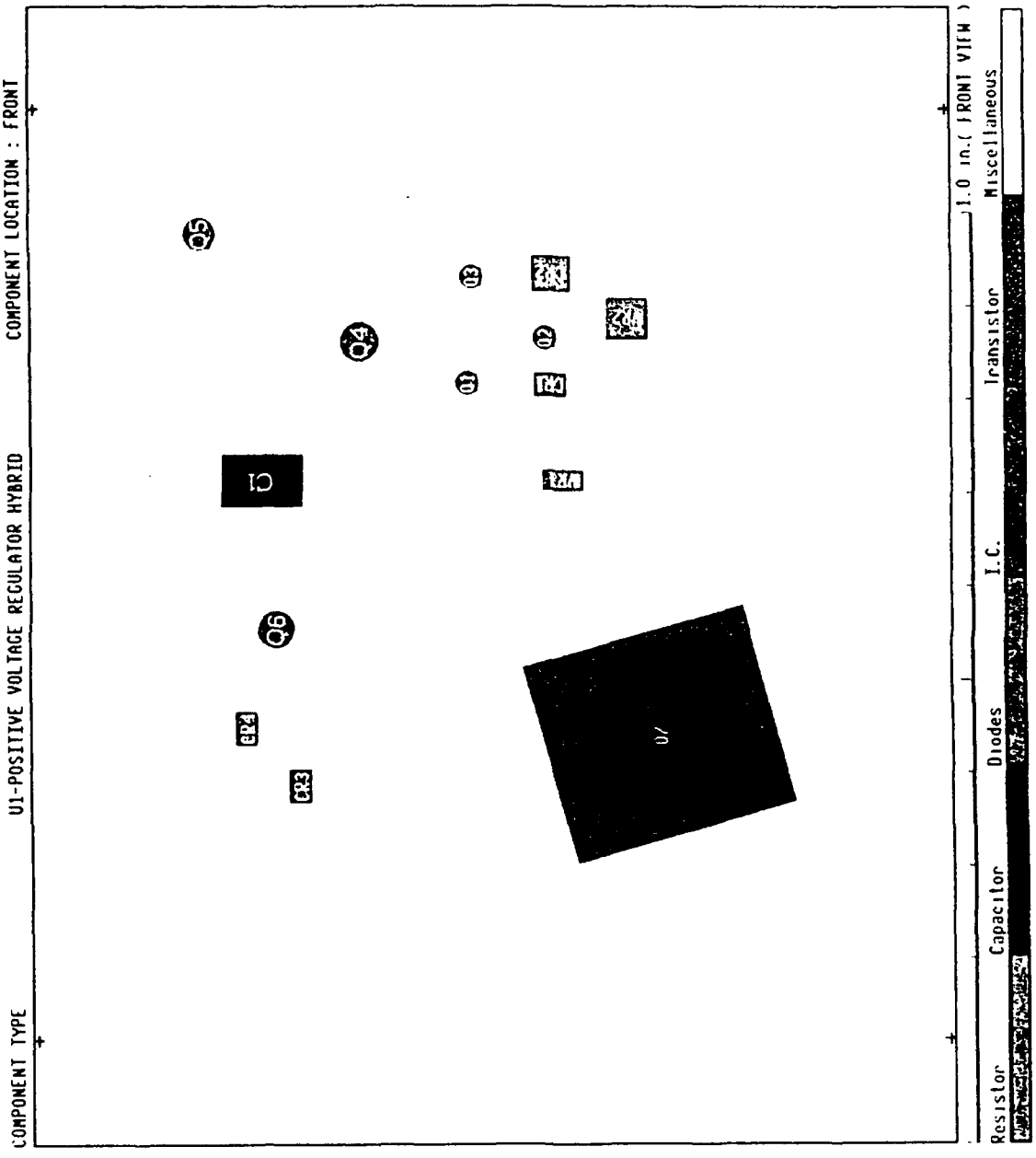


Figure G-8. U1 — Component Layout

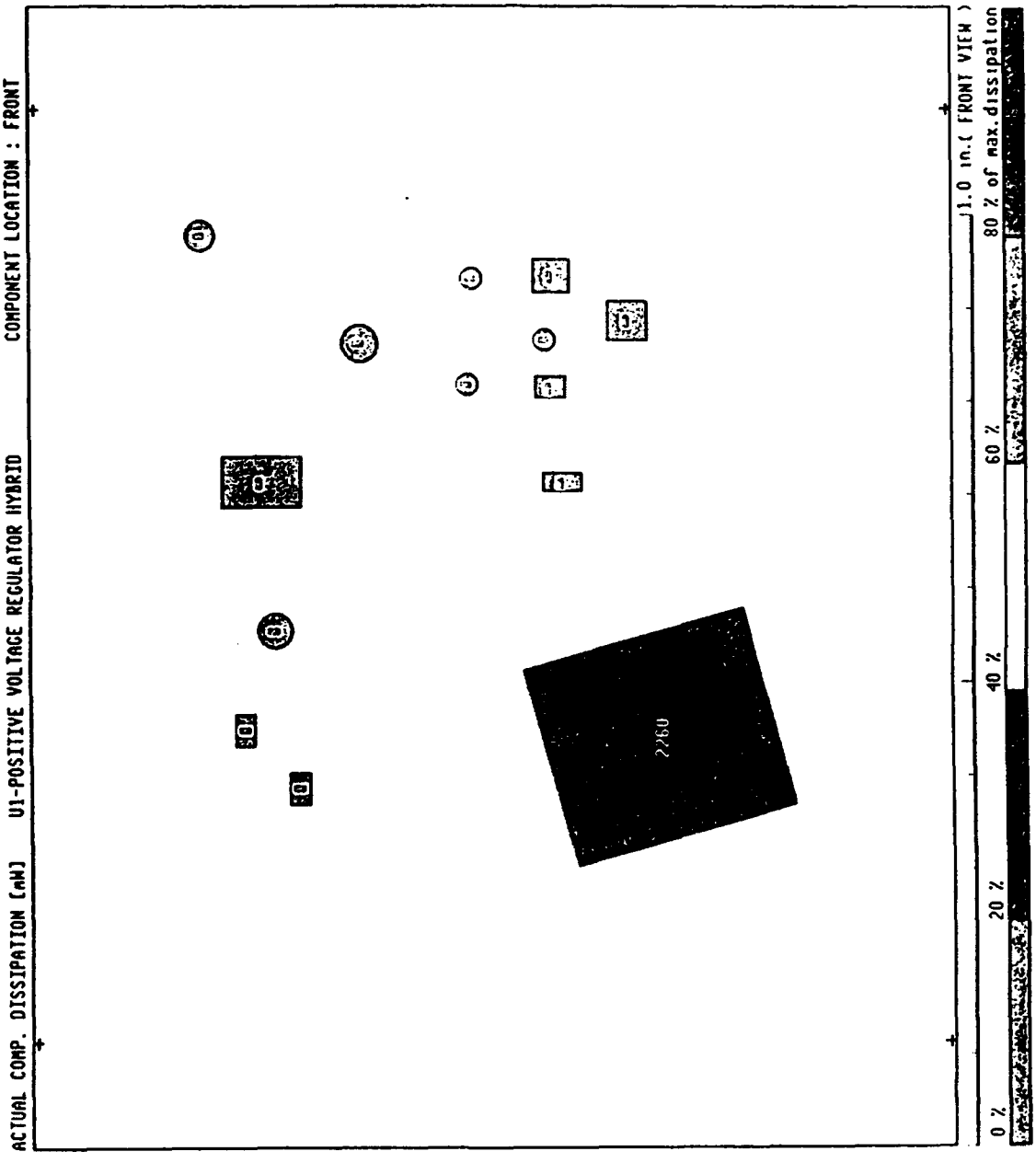


Figure G-9. U1 — Component Dissipations

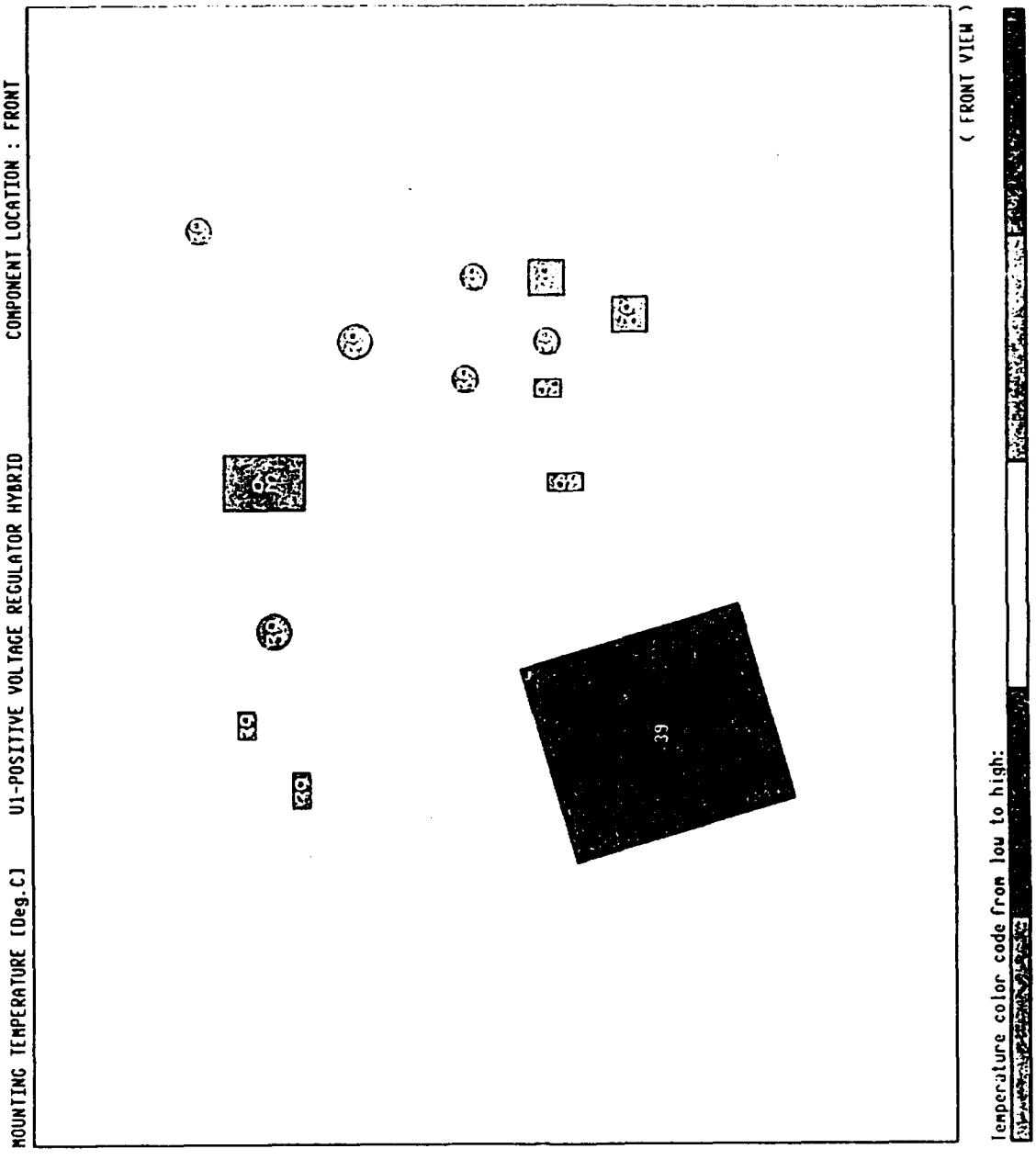


Figure G-10. U1 — Mounting Surface Temperatures

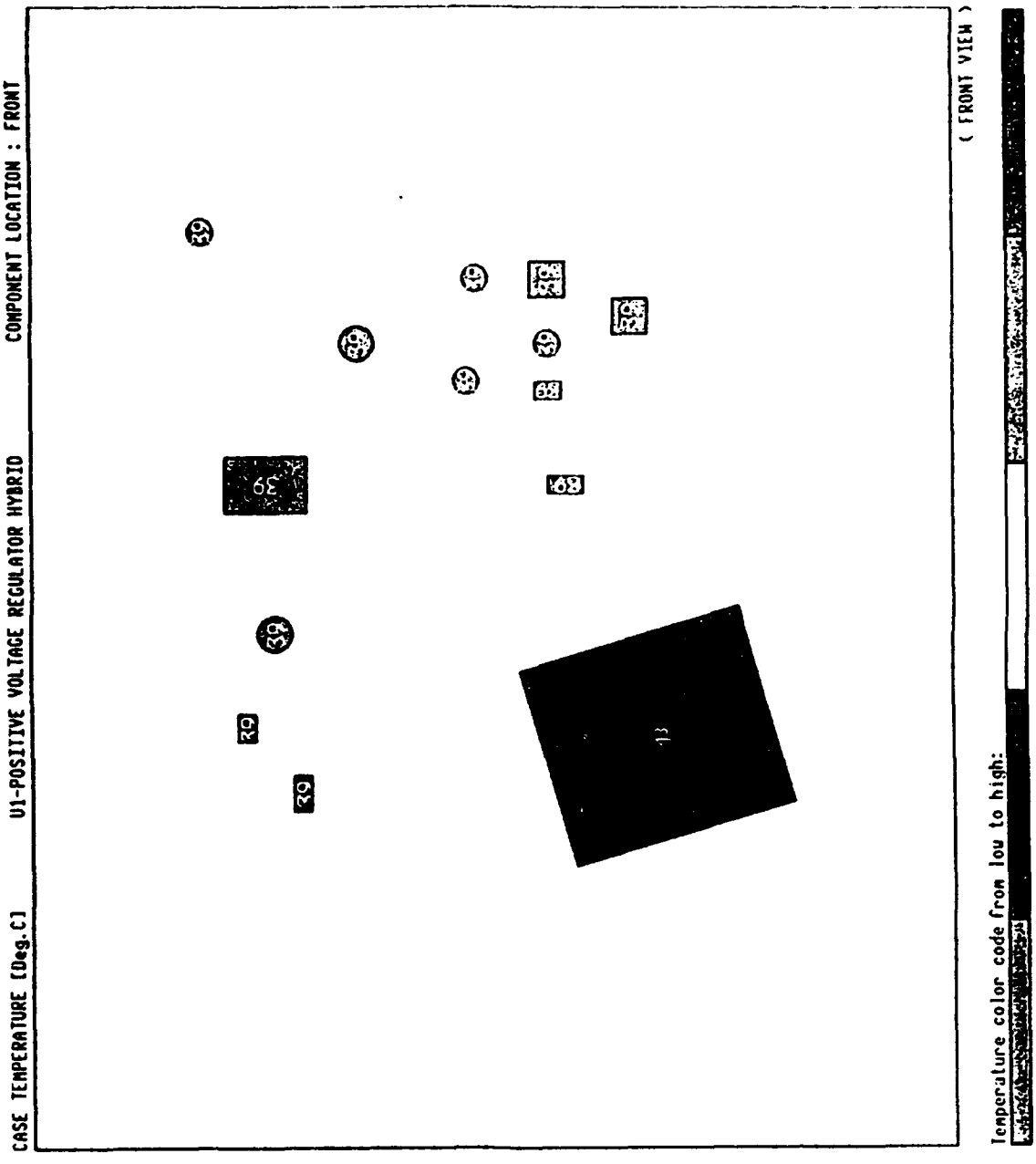


Figure G-11. U1 — Case Temperatures

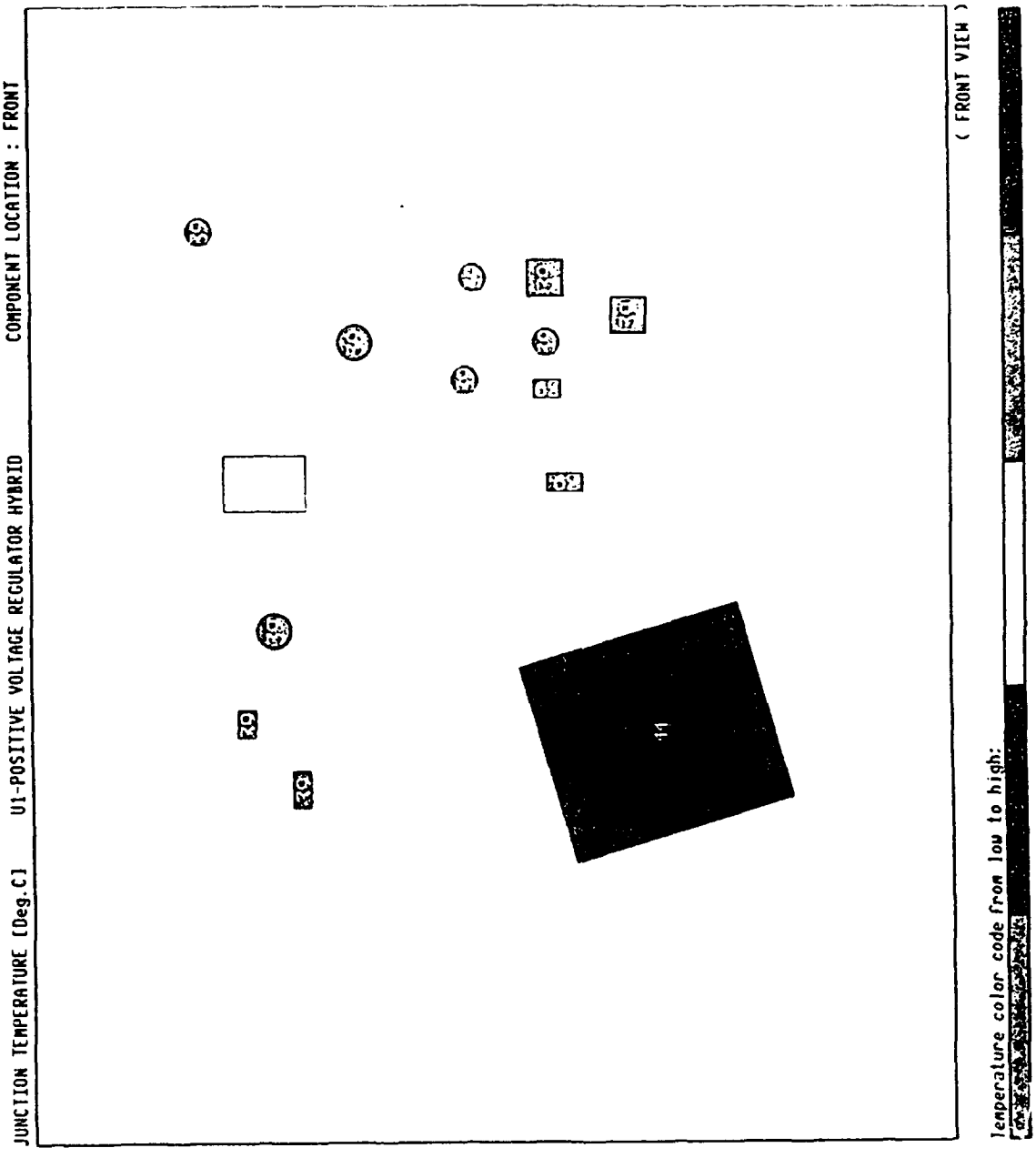


Figure G-12. U1 — Junction Temperatures

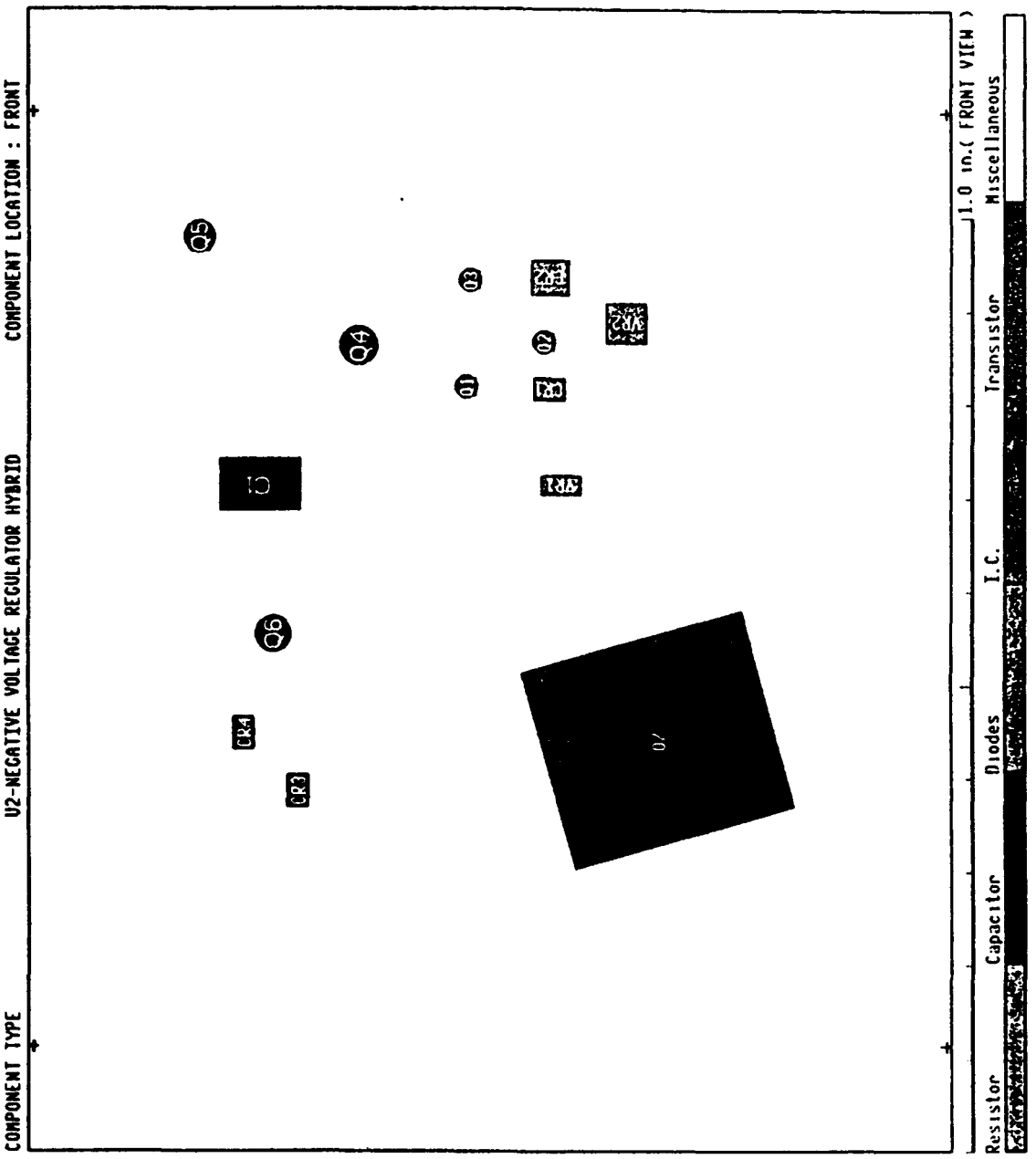


Figure G-13. U2 — Component Layout

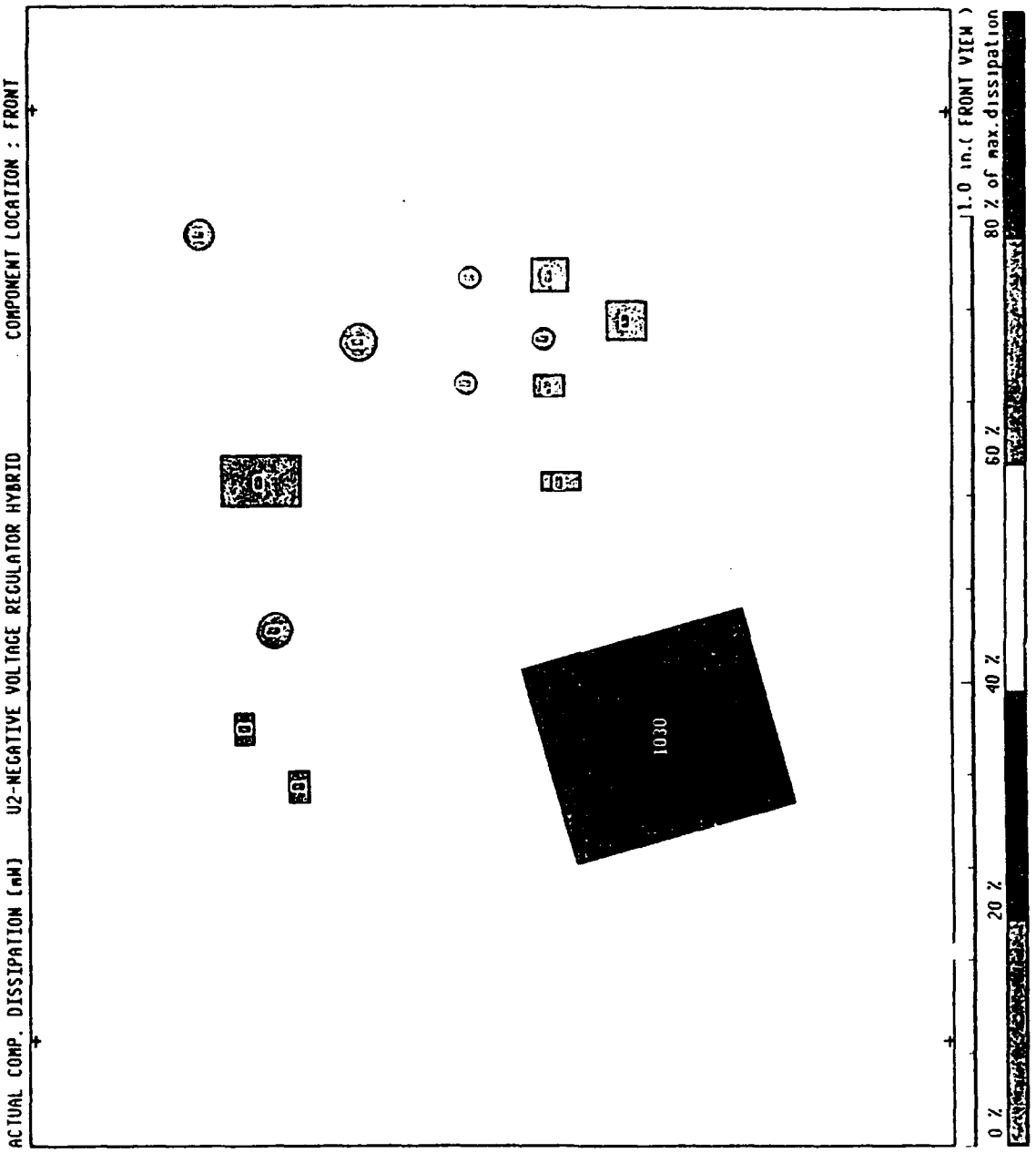


Figure G-14. U2 — Component Dissipations

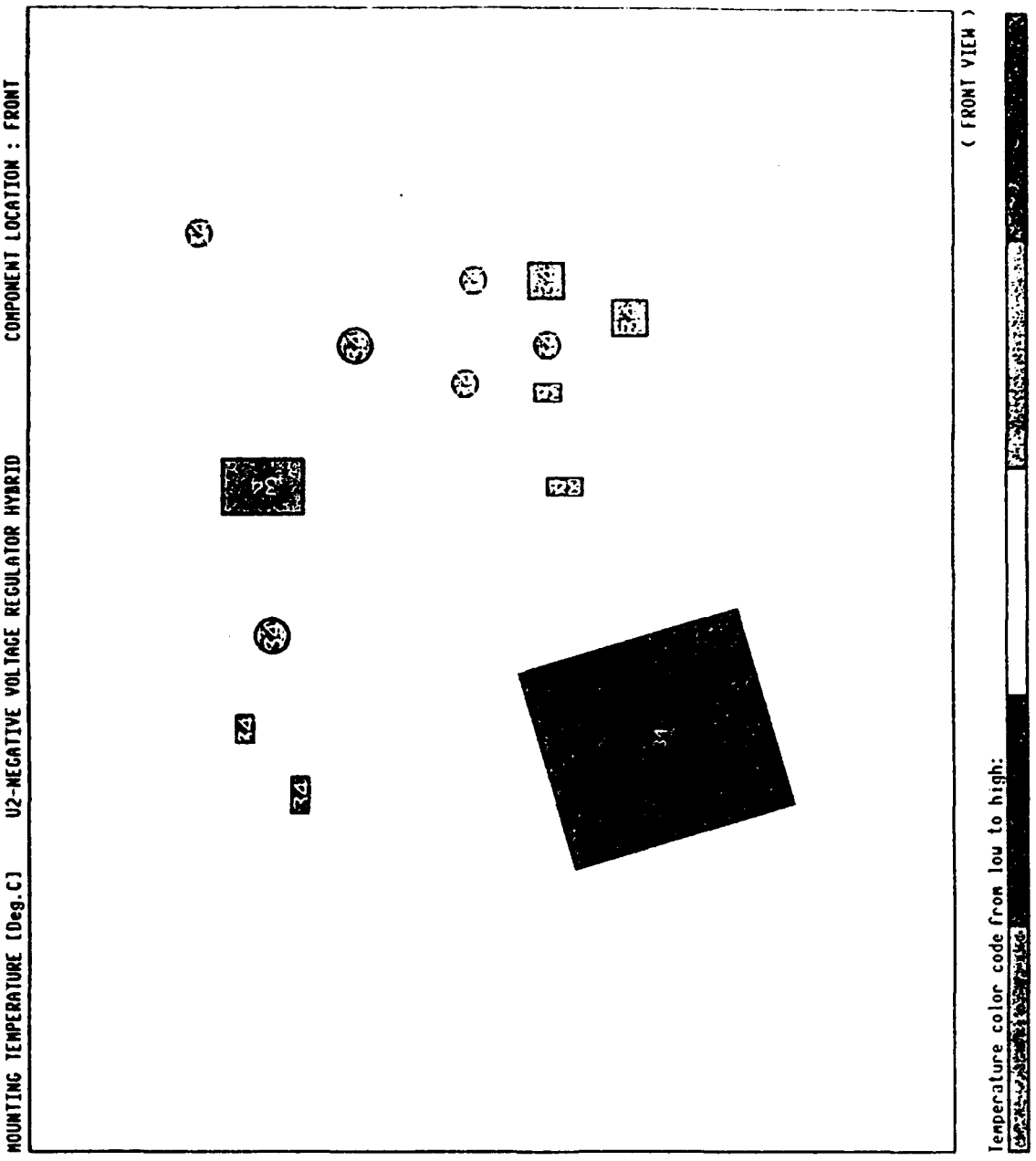


Figure G-15. U2 — Mounting Surface Temperatures

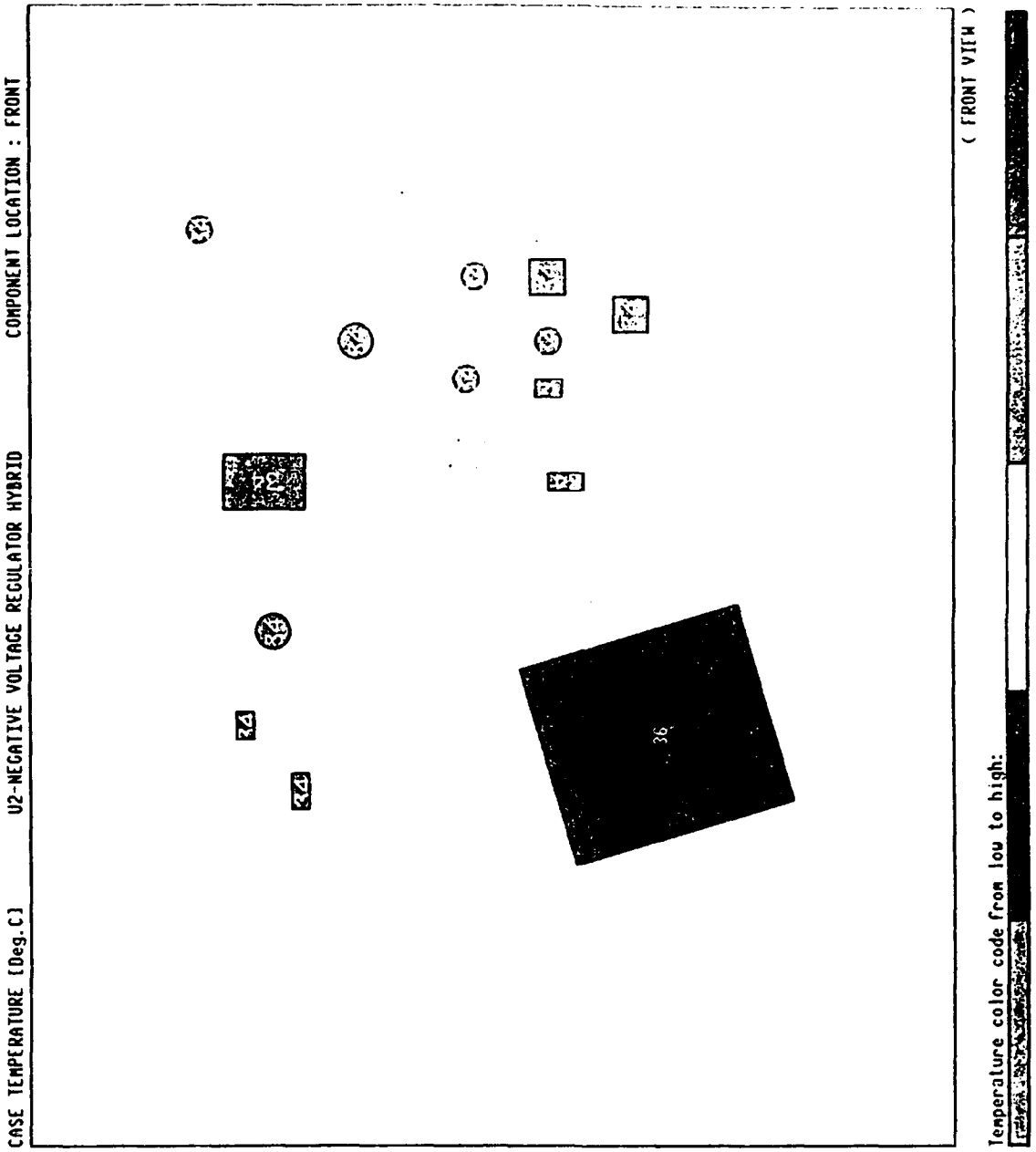


Figure G-16. U2 — Case Temperatures

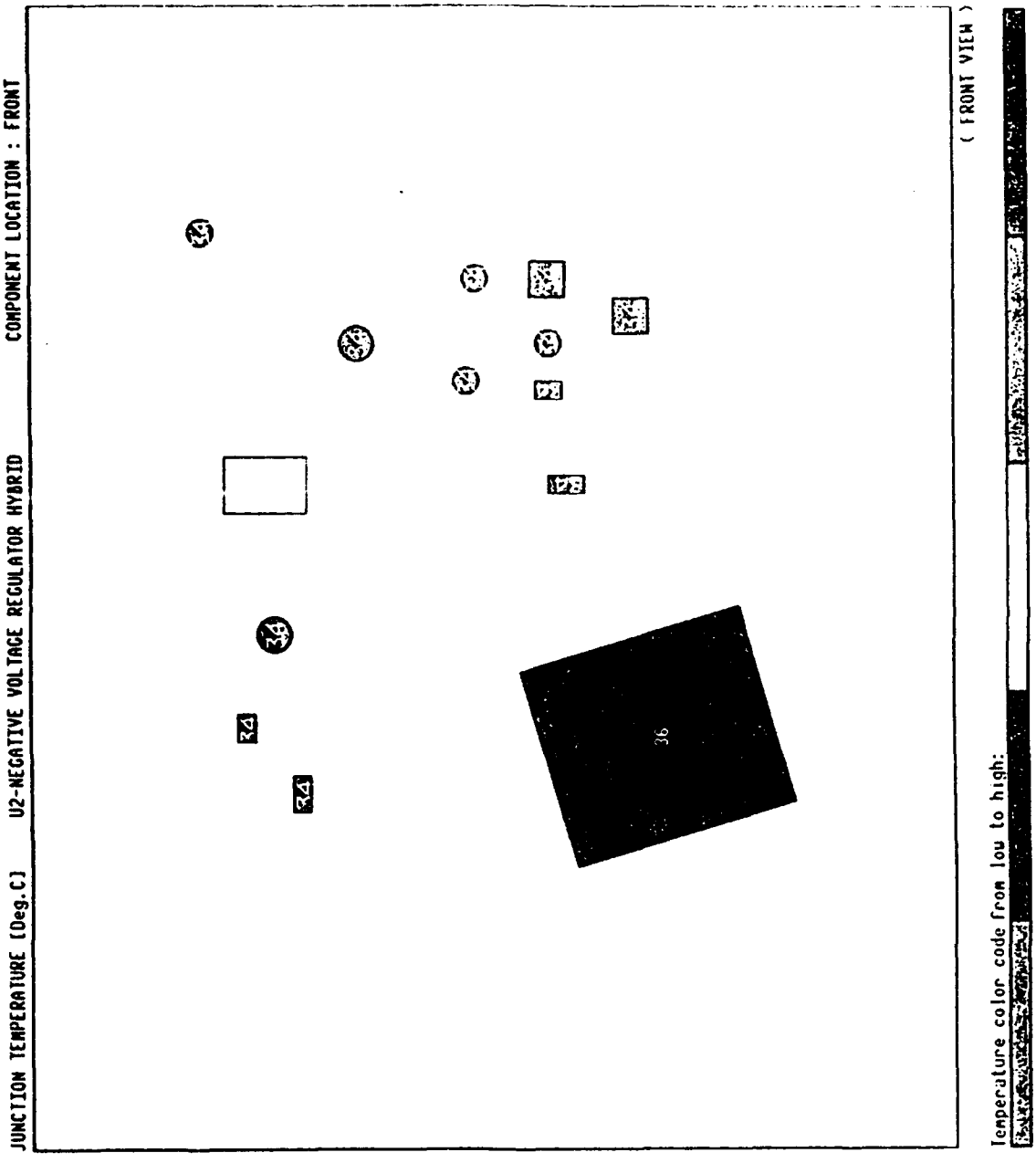


Figure G-17. U2 — Junction Temperatures

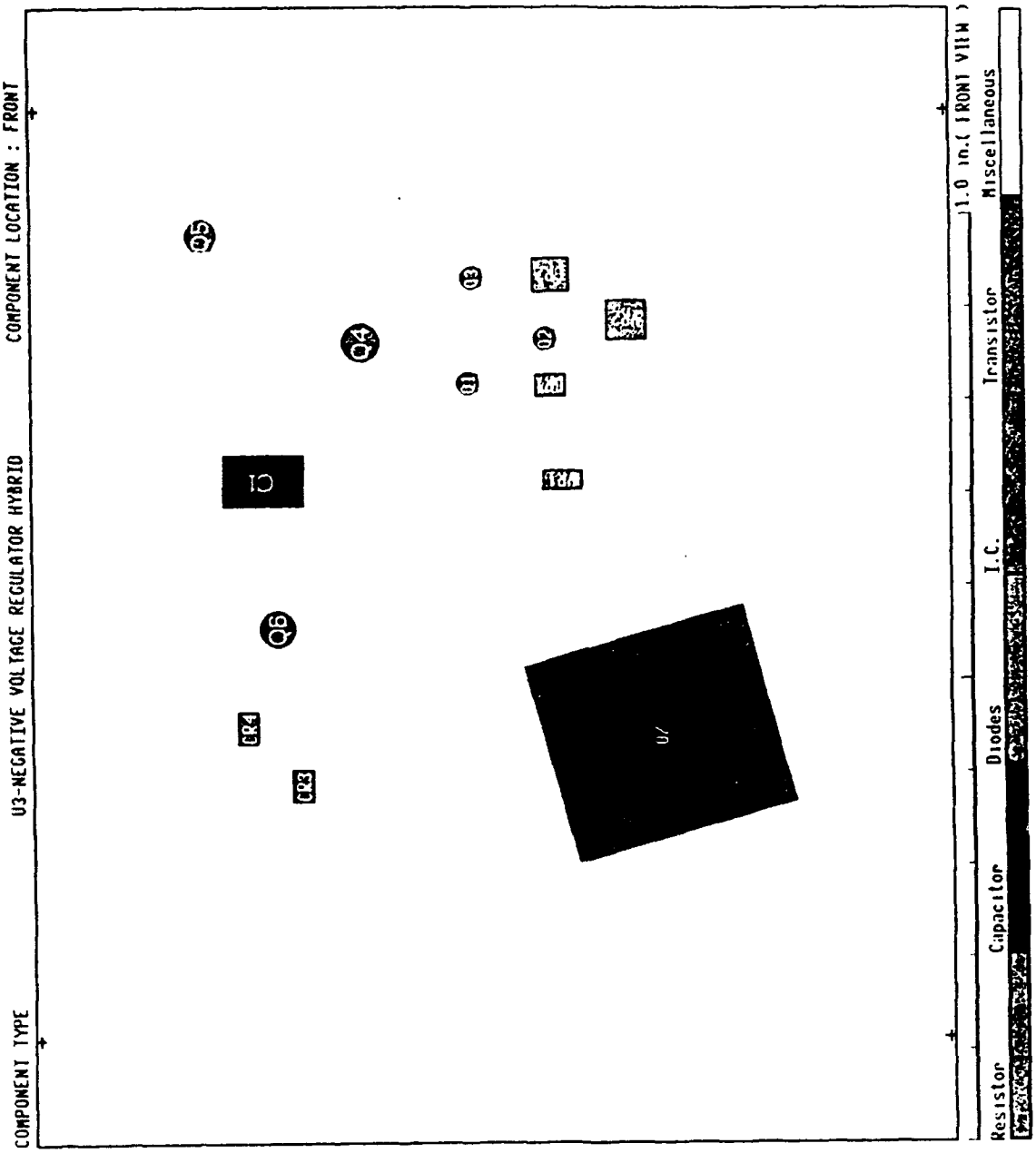


Figure G-18. U3 — Component Layout

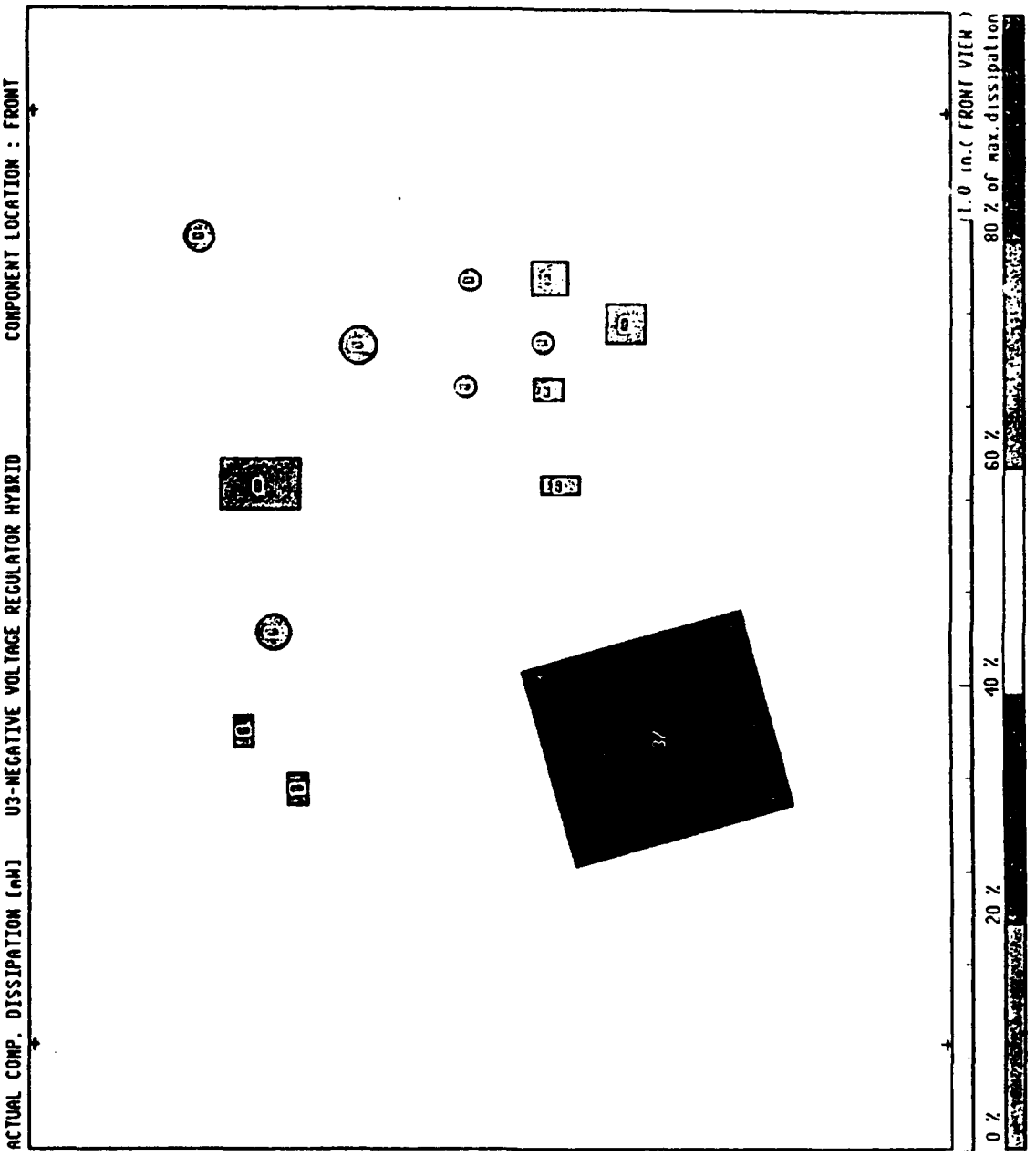


Figure G-19. U3 — Component Dissipations

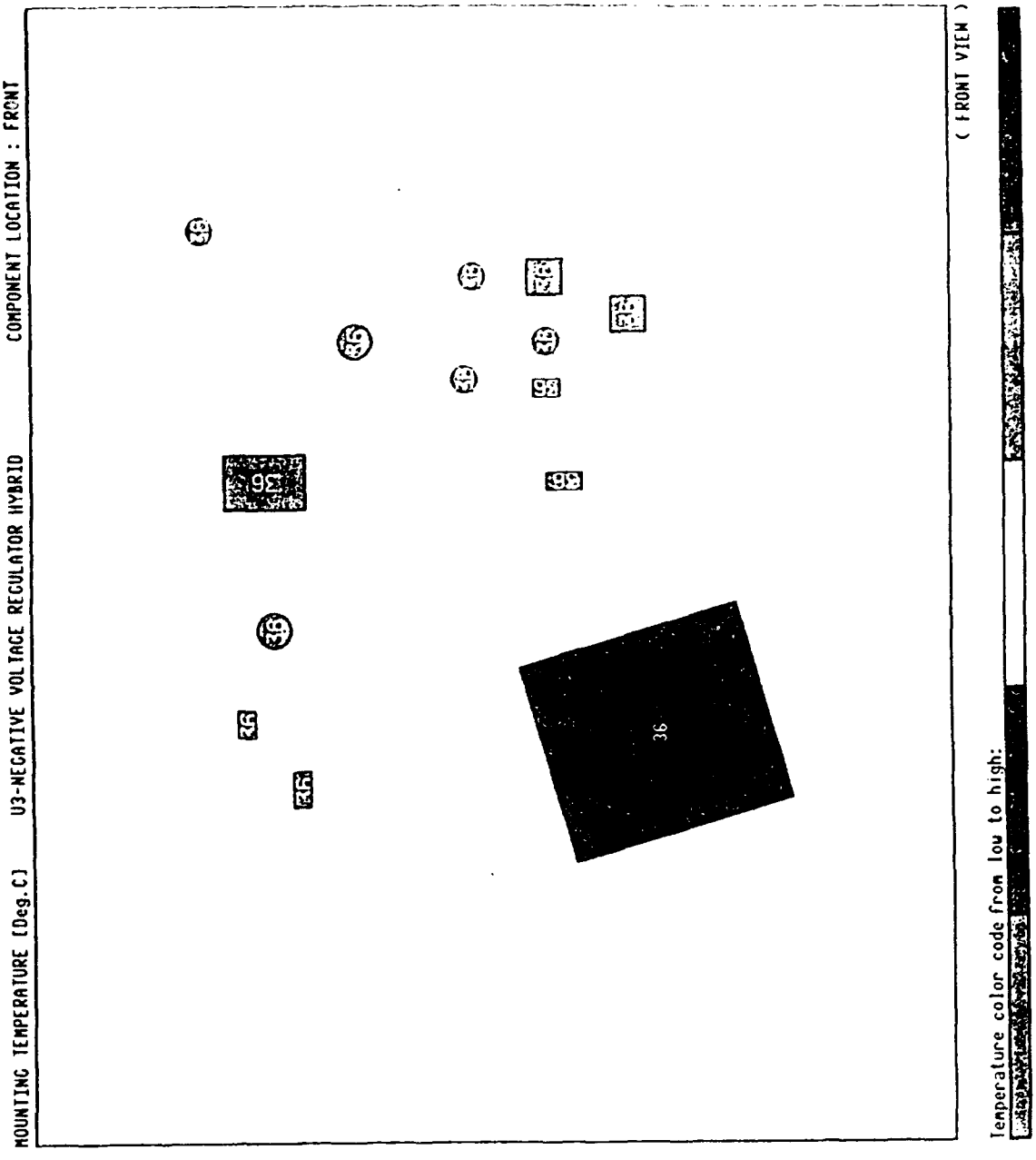


Figure G-20. U3 — Mounting Surface Temperatures

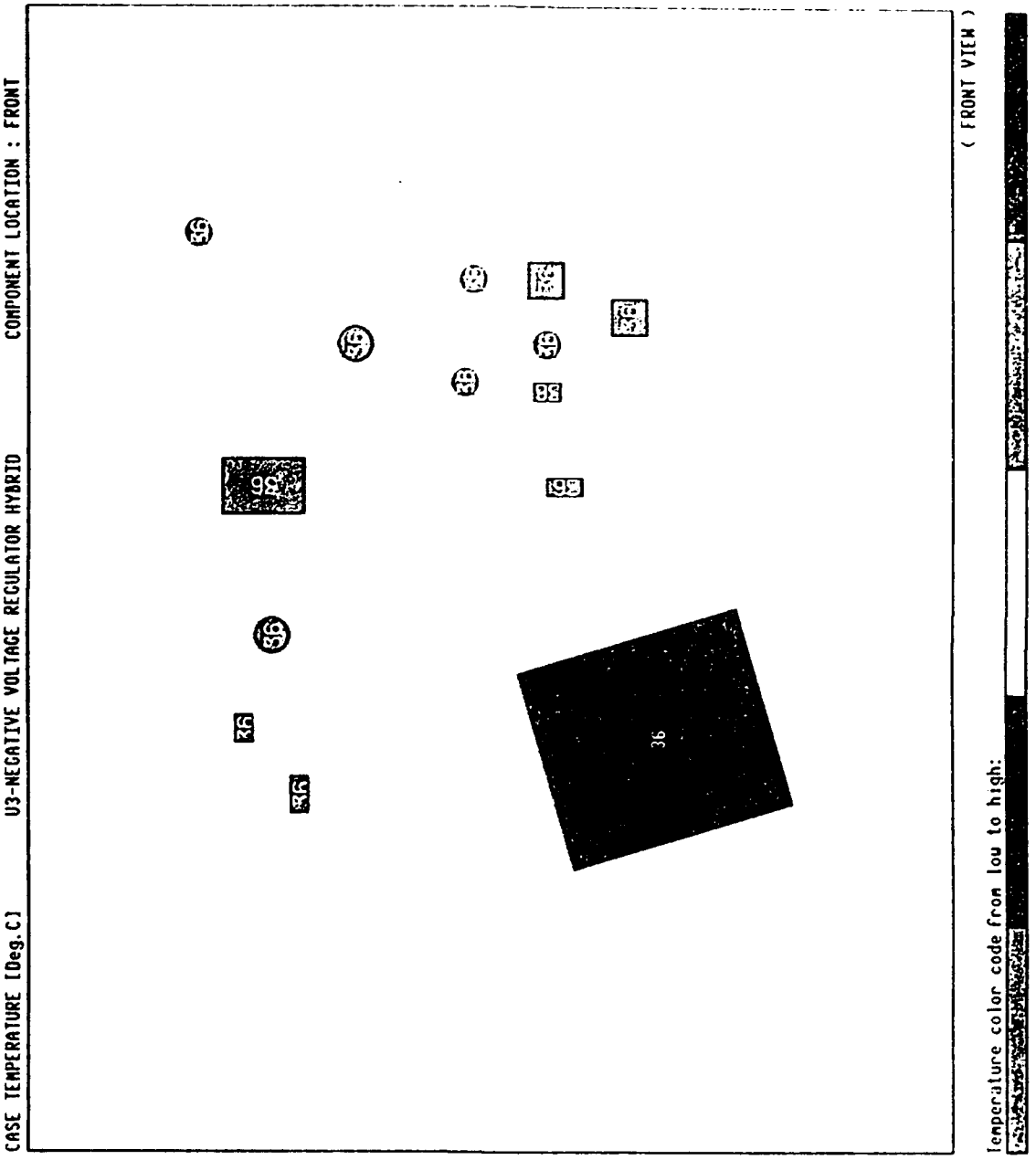


Figure G-21. U3 — Case Temperatures

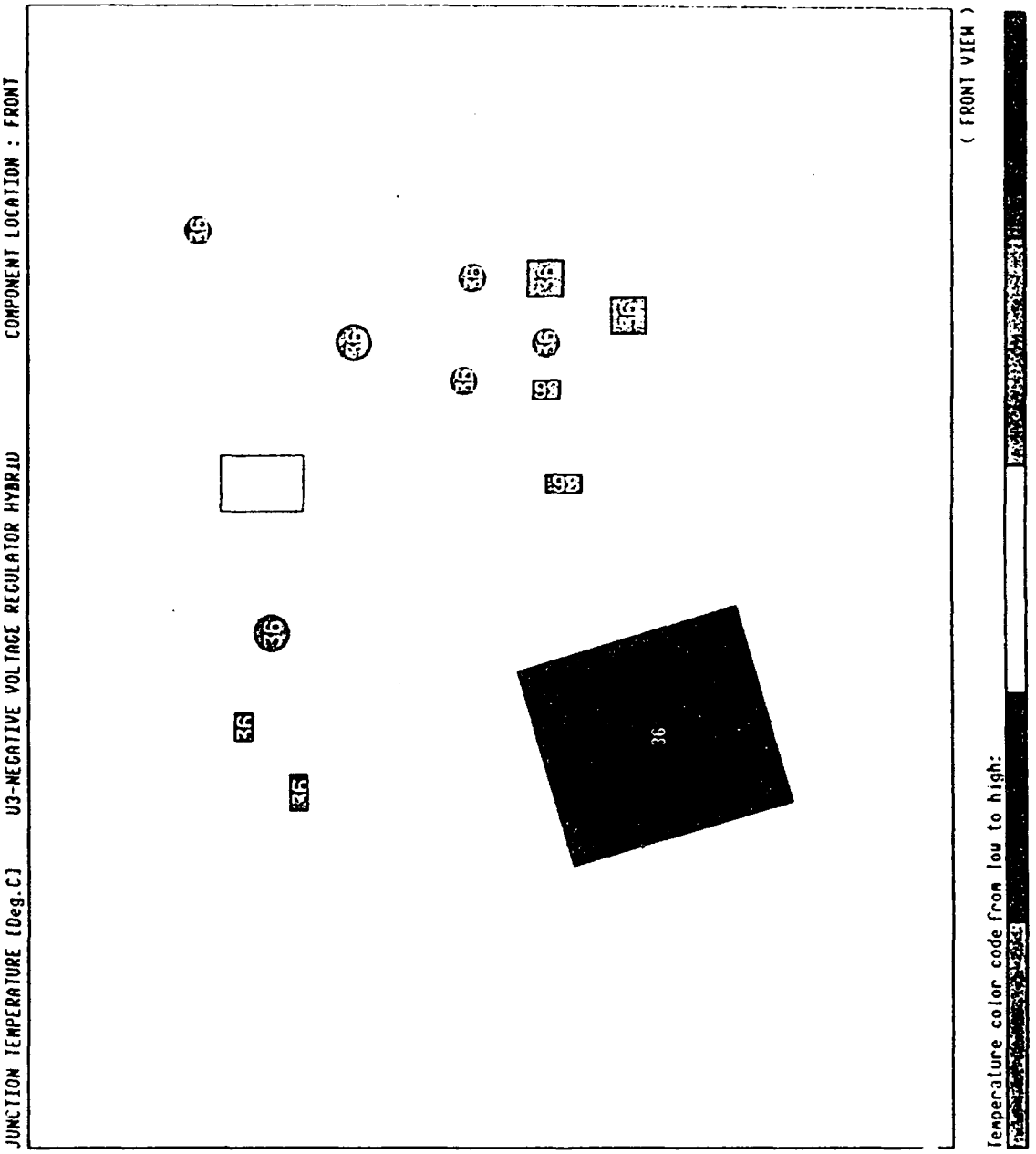


Figure G-22. U3 — Junction Temperatures

TABLE G-1
F-15 PSP LINEAR REGULATOR MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1	M39003/01-2544	0.000	34.	34.	
C2	M39003/01-2544	0.000	36.	36.	
C3	905570-49B	0.000	34.	34.	
C4	905570-103B	0.000	37.	37.	
C5	M39003/01-2541	0.000	34.	34.	
C6	M39003/01-2544	0.000	34.	34.	
C7	M39003/01-2544	0.000	34.	34.	
C8	905570-49B	0.000	32.	32.	
C9	905570-103B	0.000	32.	32.	
C10	M39003/01-2549	0.000	32.	32.	
C11	905570-49B	0.000	34.	34.	
C12	905570-103B	0.000	35.	35.	
C13	M39003/01-2549	0.000	34.	34.	
C14	M39003/01-2596	0.000	35.	35.	
C15	905570-55B	0.000	34.	34.	
C16	M39003/01-2552	0.000	37.	37.	
C17	M39003/01-2552	0.000	37.	37.	
CR2	JANTX1N3600	0.000	37.	37.	37.
CR3	JANTX1N5418	0.000	34.	34.	34.
CR4	JANTX1N3600	0.000	34.	34.	34.
CR5	JANTX1N3600	0.000	34.	34.	34.
CR7	JANTX2N2324	0.000	34.	34.	34.
Q1	928765-502B	3.580	42.	45.	49.
Q3	JANTX2N2907A	0.000	37.	37.	37.
Q4	JANTX2N2907A	0.000	35.	35.	35.
R1	RWR89SR237FP	0.059	37.	39.	
R2	RWR89SR237FP	0.059	37.	38.	
R3	RWR81S3650FP	0.130	36.	64.	
R4	RCR07G223JR	0.000	32.	32.	
R5	RWR80SR237FP	0.022	37.	40.	
R6	RWR80SR237FP	0.022	37.	39.	
R7	RNC60H2491FR	0.000	37.	37.	
R8	RWR80SR237FP	0.035	37.	39.	
R9	RWR81S3650FP	0.130	34.	62.	
R10	RCR07G223JR	0.000	32.	32.	
R11	RWR89SR511FP	0.015	34.	35.	
R12	RNC60H2491FR	0.000	34.	34.	
R13	RCR07G223JR	0.000	34.	34.	
R14	RWR80S1R00FP	0.000	34.	34.	
R15	RNC60H1540FR	0.000	35.	35.	
R16	RCR07G471JR	0.000	37.	37.	

TABLE G-1 (Continued)
F-15 PSP LINEAR REGULATOR MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
R17	RCR07G101JR	0.000	37.	37.	
R18	RCR07G102JR	0.000	37.	37.	
R20	RNC60H2611FR	0.000	34.	34.	
R21	RCR07G222JR	0.000	37.	37.	
R22	RCR07G332JR	0.000	37.	37.	
R23	RCR07G152JR	0.090	37.	55.	
R24	RNC60H6191FR	0.000	36.	36.	
R25	RNC60H6811FR	0.000	36.	36.	
R26	RCR07G681JR	0.000	34.	34.	
R27	RCR07G102JR	0.000	34.	34.	
R28	RCR07G330JR	0.000	34.	34.	
R29	RCR07G101JR	0.000	34.	34.	
R30	RWR80S1R00FP	0.000	34.	34.	
R31	RCR07G103JR	0.000	37.	37.	
R32	RCR07G133JR	0.000	37.	37.	
R33	RCR07G103JR	0.000	37.	37.	
R34	RCR07G752JR	0.000	37.	37.	
R35	RCR07G103JR	0.000	37.	37.	
R36	RCR07G103JR	0.000	37.	37.	
U1	934266-501B	2.260	39.	43.	44.
U2	934268-501B	1.030	34.	36.	36.
U3	934268-501B	0.037	36.	36.	36.
U4	H990446-001B	0.250	39.	52.	67.
VR1	JANTX1N964B	0.000	37.	37.	37.
VR2	JANTX1N827	0.050	37.	40.	50.

TOTAL OF PART DISSIPATIONS: 7.769 WATTS

TABLE G-2
F-15 PSP LINEAR REGULATOR MODULE
U1 -- POSITIVE VOLTAGE REGULATOR HYBRID (DWG 934266)

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1	C1RONFO50K1006	0.000	39.	39.	
CR1	1N3600	0.000	39.	39.	39.
CR2	1N3600	0.000	39.	39.	39.
CR3	1N3600	0.000	39.	39.	39.
CR4	1N3600	0.000	39.	39.	39.
Q1	2N2484	0.000	39.	39.	39.
Q2	2N2484	0.000	39.	39.	39.
Q3	2N2907A	0.000	39.	39.	39.
Q4	2N2907A	0.000	39.	39.	39.
Q5	2N3501	0.000	39.	39.	39.
Q6	2N4236	0.000	39.	39.	39.
Q7	2N5303	2.260	39.	43.	44.
VR1	1N825	0.000	39.	39.	39.
VR2	1NZ49A	0.000	39.	39.	39.

TOTAL OF PART DISSIPATIONS: 2.260 WATTS

TABLE G-3
F-15 LINEAR REGULATOR MODULE
U2 -- NEGATIVE VOLTAGE REGULATOR HYBRID (DWG 934268)

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1	C1RONF050K1006	0.000	34.	34.	
CR1	1N3600	0.000	34.	34.	34.
CR2	1N3600	0.000	34.	34.	34.
CR3	1N3600	0.000	34.	34.	34.
CR4	1N3600	0.000	34.	34.	34.
Q1	2N2484	0.000	34.	34.	34.
Q2	2N2484	0.000	34.	34.	34.
Q3	2N2907A	0.000	34.	34.	34.
Q4	2N2907A	0.000	34.	34.	34.
Q5	2N3501	0.000	34.	34.	34.
Q6	2N4236	0.000	34.	34.	34.
Q7	2N5303	1.030	34.	36.	36.
VR1	1N825	0.000	34.	34.	34.
VR2	1NZ49A	0.000	34.	34.	34.

TOTAL OF PART DISSIPATIONS: 1.030 WATTS

TABLE G-4

F-15 LINEAR REGULATOR MODULE

U3 -- NEGATIVE VOLTAGE REGULATOR HYBRID (DWG 934268)

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1	C1RONF050K1006	0.000	36.	36.	
CR1	1N3600	0.000	36.	36.	36.
CR2	1N3600	0.000	36.	36.	36.
CR3	1N3600	0.000	36.	36.	36.
CR4	1N3600	0.000	36.	36.	36.
Q1	2N2484	0.000	36.	36.	36.
Q2	2N2484	0.000	36.	36.	36.
Q3	2N2907A	0.000	36.	36.	36.
Q4	2N2907A	0.000	36.	36.	36.
Q5	2N3501	0.000	36.	36.	36.
Q6	2N4236	0.000	36.	36.	36.
Q7	2N5303	0.037	36.	36.	36.
VR1	1N825	0.000	36.	36.	36.
VR2	1NZ49A	0.000	36.	36.	36.

TOTAL OF PART DISSIPATIONS: 0.037 WATTS

APPENDIX H

JUNCTION-TO-CASE THERMAL RESISTANCE MEASUREMENTS

(1 of 2)

INTERDEPARTMENTAL CORRESPONDENCE

TO: Distribution
ORG:

CC:

DATE: 05/08/89
REF: 7641.10/306

SUBJECT: Thermal Resistance Test on 54LS163A, HAC 932756

FROM: S. V. Nguyen and Fremont Reizman
ORG: 76-41

BLDG: E1 MAIL STA: 128
LOC: E0 PHONE: 616-4515

PROGRAM: ERFM

INTRODUCTION

This report contains the results of the thermal resistance junction-to-case ($R_{\theta JC}$) on sixteen Motorola 54LS163A's, HAC 932756-1B, Four-Bit Binary Synchronous Counter, 16 pin flat package.

The report also covers the $R_{\theta JC}$ evaluation on two 54LS163, 16 pins dual-in-line acquired from HAC Electronic Store using both the electrical and infrared methods.

PRINCIPLES AND PROCEDURE OF THE MEASUREMENTS:

A. Electrical Method:

For the electrical method, the $R_{\theta JC}$ can be calculated by using the following:

$$R_{\theta JC} = \frac{\Delta T}{P_D} = \frac{TC * |V_1 - V_3|}{V_H * I_H}$$

Where TC (Temperature Coefficient) of the device is measured by applying a forward current (I_F) of 1 mA through the IC substrate isolation diode under a range of temperatures. TC is calculated as follows:

$$TC = \frac{|T_2 - T_1|}{|V_{F2} - V_{F1}|}$$

Temperature Coefficient Measurements:

The TC was measured on one set-up sample (S/N 1C) and on 3 test samples (S/N 6, 7, and 16) using the circuit shown in Figure 1. Pin 8(GND), 9(Load), 10(T), and 11(Q_D) were tied together and connected to the positive 1 mA supply; pin 16(V_{CC}) was connected to the negative supply.

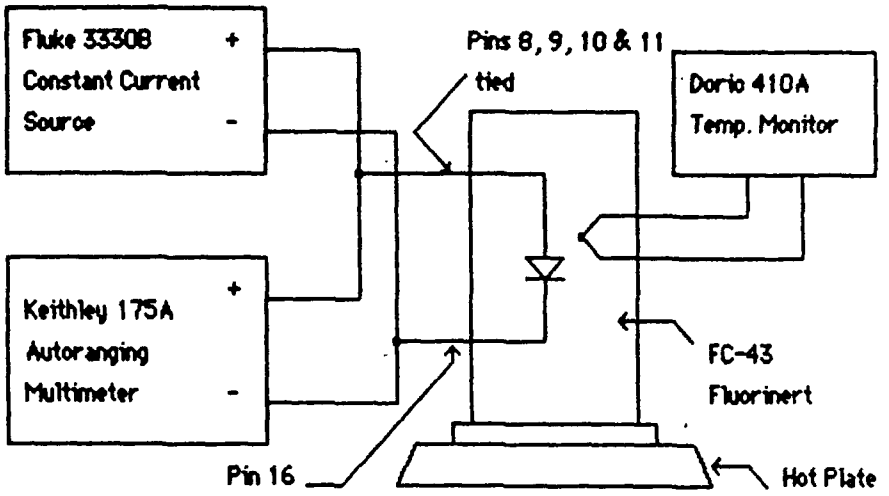


Figure H-1. Temperature Coefficient Test Circuit

The forward voltage was measured at 3 different termperatures. The average TC was calculated to be 2.3 mV/°C. The results are shown in Table I.

Specimen Number	T_1 (°C)	V_{F1}(mV)	T_2 (°C)	V_{F2}(mV)	T_3 (°C)	V_{F3}(mV)	TC (mV/°C)
1C	37.7	.5591	53.3	.5247	65.5	.4978	2.2
6	23.2	.5562	55.9	.4820	95.1	.3922	2.3
7	23.1	.5551	54.3	.4829	90.5	.3985	2.3
16	23.2	.5599	54.7	.4869	93.4	.3973	2.3

Table H-1. Temperature Coefficient Data

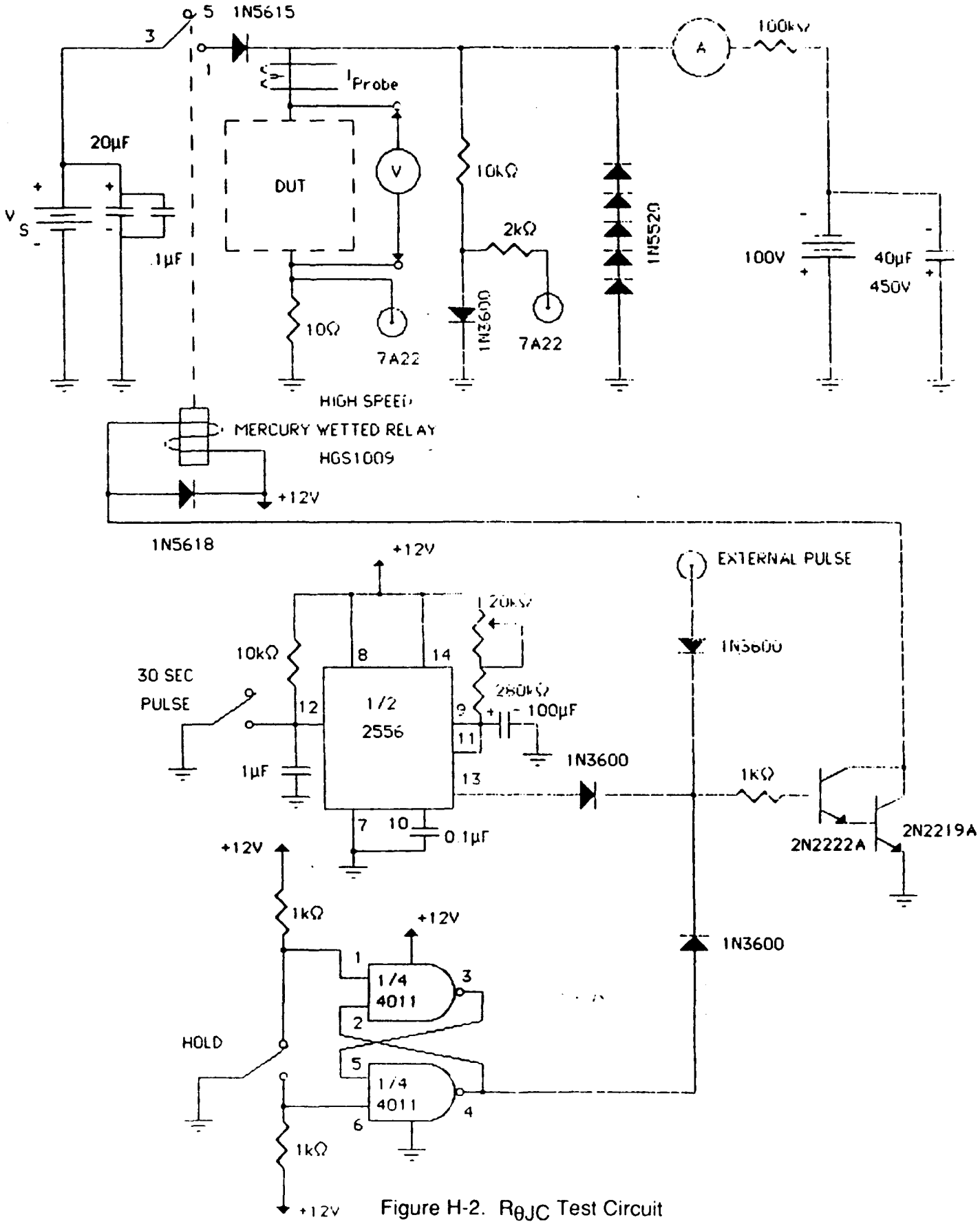


Figure H-2. $R_{\theta JC}$ Test Circuit

$R_{\theta JC}$ Measurement using the Electrical Method:

The $R_{\theta JC}$ were measured using the test circuit shown in Figure 2. The DUT operated under short circuit mode to insure that there was sufficient dissipated power to obtain an adequate resolution on the differential voltage change. The pin connections of the DUT are shown in Figure 3.

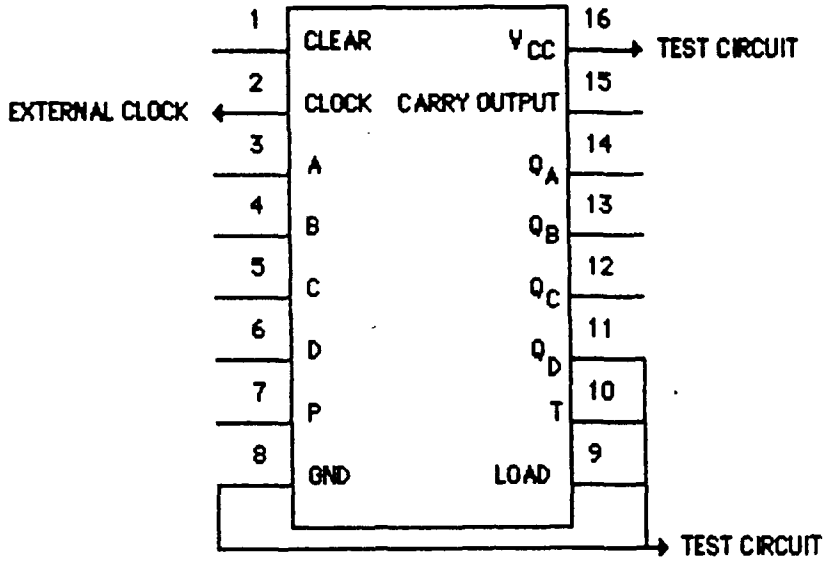


Figure H-3. Pin Connections of the DUT

The timing diagram is shown in Figure 4. where t_1 is the time at which V_1 is set as reference on the storage scope, t_2 is the heating time in which the power dissipates through the DUT, t_2= 30 seconds for this measurement. t_3 is the time at which the heating power is diverted from the DUT and the differential voltage is measured, t_3 is measured at 40 miroseconds.

During the t_2 interval, pin 2 was clocked to turn the output (pin 11) to a high state. In this mode, the DUT dissipates the highest power that is necessary for the resolution requirement mentioned earlier.

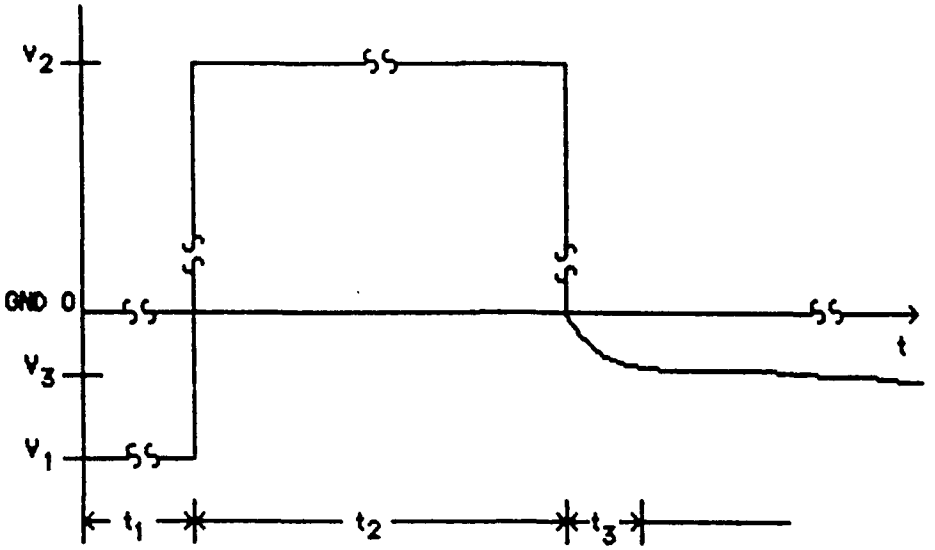


Figure H-4. Timing Diagram for Voltage Across the DUT

B. Infrared (Optical) Method

Returning to the definition of $R_{\theta JC}$:

$$R_{\theta JC} = \frac{\Delta T}{P_D}$$

If the device is delidded, it is possible to measure the temperature of the die from the infrared radiation from its surface. In this way we can locate the hottest spot on the surface and use its temperature in computing ΔT, rather than the average figure given by the large area isolation diffusion. The peak temperature, rather than the average temperature, is the important one in determining the safe operating area.

The same devices used in the electrical measurements were also measured using the Barnes CompuTherm infrared imager. This instrument provides a direct temperature measurement for all points on the surface, corrected for emissivity. The device must be delidded, but the die surface does not have to be painted black to give a known emissivity, unlike certain older infrared instruments. A temperature map of the die surface is a side benefit. The results of these measurements are shown in Table III

TEST RESULTS:

The test result of the sixteen Motorola 54LS163A's using the electrical method is shown in Table II. The infrared method has not been used on these production parts.

Specimen Number	I_H (mA)	V_H (V)	ΔV_F (mV)	$R_{\theta JC}$ (°C/W)
1	60.2	4.53	12.5	19.9
2	62.8	4.48	11.5	17.8
3	65.6	4.46	12.8	19.0
4	63.1	4.49	10.4	16.0
5	64.7	4.47	12.5	18.8
6	63.8	4.48	11.0	16.7
7	64.1	4.48	12.5	18.9
8	63.5	4.49	11.0	16.8
9	67.4	4.44	10.2	14.8
10	64.9	4.47	10.7	16.0
11	63.0	4.49	11.0	16.9
12	63.4	4.49	10.2	15.6
13	67.5	4.44	13.0	18.9
14	62.0	4.50	10.5	16.4
15	68.3	4.43	13.8	19.8
16	64.7	4.47	10.2	15.3

Table H-2. $R_{\theta JC}$ Test Results

Correlation Test:

To check the test results on the electrical method, two set-up samples (S/N 2C and 3C) were measured for $R_{\theta JC}$ using the electrical method then delidded and measured for $R_{\theta JC}$ using the infrared imager located in the Failure Analysis Laboratory.

The results of both methods are shown in Table III.

Specimen Number	ELECTRICAL METHOD				OPTICAL METHOD			
	I_H (mA)	V_H (V)	ΔV (mV)	$R_{\theta JC}$ (°C/W)	I_H (mA)	V_H (V)	ΔT (°C)	$R_{\theta JC}$ (°C/W)
2C	74.2	4.98	22.0	26.8	62.8	4.50	7.5	26.5
3C	66.5	4.99	23.0	30.2	54.7	4.50	7.7	31.3

Table H-3. Correlation Test Results between Electrical and Infrared Methods

CONCLUSION

The results obtained from the electrical method give values for $R_{\theta JC}$ which are slightly lower than the infrared method. The difference was mainly due to the junction temperature gradient across the IC chip, since not all portions of the chips dissipate the same amount of power. The infrared $R_{\theta JC}$ figures are based on the peak die temperatures.

The two methods are otherwise in good agreement. These results are therfore mutually confirmatory.

S. V. Nguyen

Fremont Reizman

APPENDIX I

JUNCTION-TO-CASE THERMAL RESISTANCE MEASUREMENTS (2 of 2)

INTERDEPARTMENTAL CORRESPONDENCE

TO	J.M. Kallis	C: D.H. Buettner	DATE: 08 June 1989
ORG	72-26	J.L. Cook	REF: 7641.20/1649
		A.E. Lange	
SUBJECT	Thermal Resistance Measurements of ERFM Components Which Did Not Meet X-Ray Acceptance Criteria	S. Sung	FROM: D.W. Buechler
		J.A. Zelik	ORG: 76-41-22
			BLDG. E1 MAIL STA C132
			LOC. EO PHONE 64650

REFERENCE: S.V.Nguyen, F. Reizman, "Thermal Resistance Test on 54LS163, HAC 932756," IDC 7641.10, dated 8 May 1989.

INTRODUCTION

X-Ray evaluation of the components to be used to fabricate the ERFM P/N 3562102 SRUs resulted in the identification of a number of the components which were out of specification with respect to MIL-STD-883C acceptance criteria for die attach. J.M. Kallis reviewed these part numbers to determine if placement of components on the SRU of the same part number would significantly effect the operating temperature of the part and thereby effect the time to failure of that part. He found that in some cases there was a significant temperature difference, as much as 20°C, for components of the same part number depending on where they were placed on the module. Therefore, placing a component with a higher thermal resistance, which would be expected for a component with a high degree of voiding in the die attach, in a position where it would operate at a higher temperature, should accelerate the failure of the device. This would be beneficial to the ERFM Program in that an early failure means that less combined environment reliability testing (CERT) would be required. In order to better predict failure free operating period the junction to case thermal resistance ($R_{\theta JC}$) of the components for which placement on the SRU might effect time to failure were measured.

THERMAL RESISTANCE MEASUREMENTS

Set up, calibration and initial thermal resistance measurements of ERFM components are documented in the reference. Junction to case thermal resistance measurements of components which did not meet die attach requirements will be detailed in this report. Measurements were taken on eight components. Only three of these parts failed to meet die attach requirements, the other parts were included in the measurements to provide a reference. Other components which did not meet die attach requirements were not measured for $R_{\theta JC}$ because it was judged that changing their position on the module would have a negligible effect on their time to failure due to the low temperatures

involved. The quantities, part numbers, and ERFM serial numbers of the components measured are as follows:

QTY	P/N	ERFM S/Ns
2	JM38510-07006	1*, 2
4	932730-002B	6, 8, 13*, 14
2	932820	1, 2*

* Denotes component which failed to meet die attach requirements.

TEST RESULTS

The results of measurements was somewhat inconclusive. Only small differences in $R_{\theta JC}$ were noted. The characteristics measured and the calculated values of $R_{\theta JC}$ appear below.

P/N	S/N	I_H(mA)	V_H(V)	ΔV_F(mV)	TC(mV/°C)	$R_{\theta JC}$(°C/W)
JM38510-07006	1*	47.0	5.500	21.5	2.1	39.6
	2	53.6	5.500	28.0	2.1	45.2
932730-002B	6	46.8	5.500	16.5	2.2	29.1
	8	47.7	5.500	15.0	2.2	26.0
	13*	46.7	5.500	18.0	2.2	31.8
	14	47.9	5.500	16.0	2.2	27.6
932820	1	68.8	5.500	7.0	2.5	7.4
	2*	69.8	5.500	8.0	2.4	8.7

CONCLUSIONS

Significant differences in junction to case thermal resistance values were not seen in the components tested. However, the parts that did not meet die attach requirements will still be placed in the hottest location on the SRUs, as long as this will not interfere with normal fabrication processes, to accelerate failure as much as possible. In this way the most efficient use will be made of ERFM Program resources.

D.W. Buechler

Approved: D.H. Van Westerhuyzen
D.H. Van Westerhuyzen, Head
Physical Evaluation Section

DWB:ik

APPENDIX J

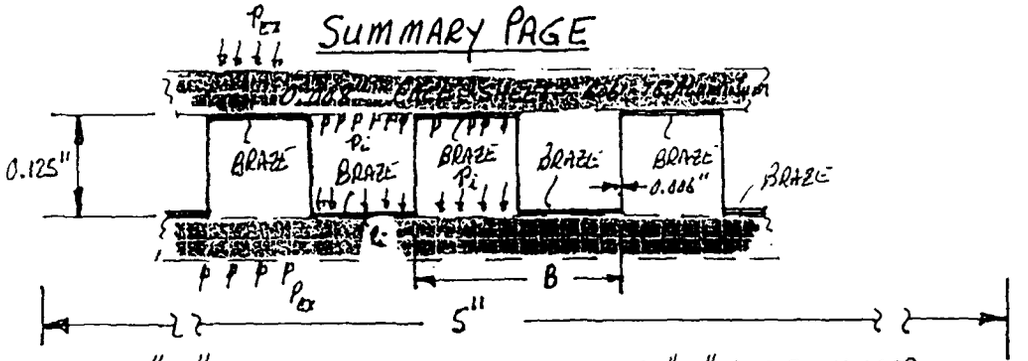
STRUCTURAL ANALYSIS OF HX SUBJECTED TO BURSTING

ANALYSIS EFFECTS of INTERNAL PRESSURE | MODEL APG-63 | REPORT NO. | PAGE

PREPARED BY F. FISHER 6 JULY 89 | SRU DISSIPATORS | 6.2 INCH x 5 INCH HEAT EXCHANGERS, 9.3 INCH x 5 INCH EXCHANGERS

CHECKED BY

SUMMARY PAGE



6.2" x 5" HEAT EXCHANGER

FIN CORE HS 6013-33-3

B = 0.0909"

FOR AN INTERNAL PRESSURE P_i

BRAZE P_i = 748 psig TO Pull BRAZE (P.1)

FIN P_i = 1848 Psig FIN IN TENSION (P.2)

BENDING FACE SHEET P_i = 1051 psig BENDING STRESS (P.2)

P_{EX} TO CHECK VACUUM

FIN CRUSHING P_{EX} = 834 Psig BUCKLING (P.2)

APPEARS HEAT EXCHANGER HAS BEEN DESIGNED FOR

100 PSIG (OPERATING)

200 PSIG (PROOF)

350 PSIG (BURST)

Full VACUUM

9.3" x 5" HEAT EXCHANGER

FIN CORE HS 6013-28-3 (P.9)

B = 0.286"

FOR AN INTERNAL PRESSURE P_i

BRAZE P_i = 238 Psig TO Pull BRAZE (P.3)

FIN P_i = 587 Psig FIN IN TENSION (P.3)

BENDING FACE SHEET P_i = 592 Psig BENDING STRESS (P.4)

P_{EX} TO CHECK VACUUM

FIN CRUSHING P_{EX} = 398 Psig BUCKLING (P.4)

APPEARS HEAT EXCHANGER HAS BEEN DESIGNED FOR

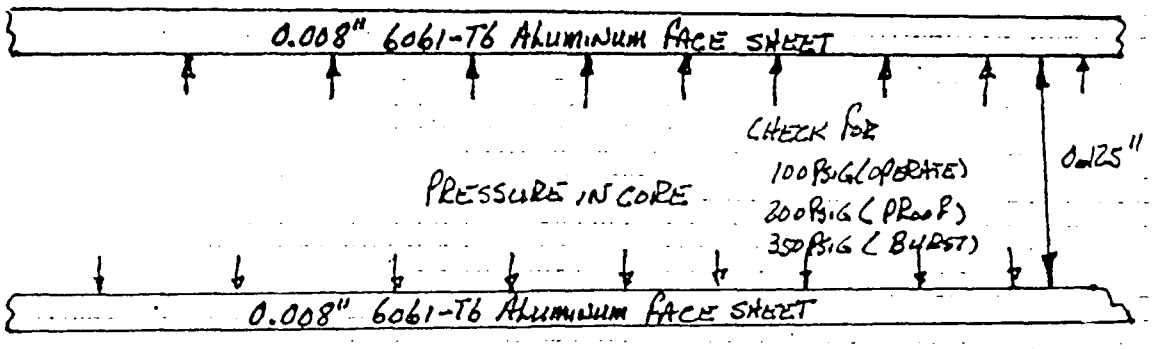
100 PSIG (OPERATING)

200 PSIG (PROOF)

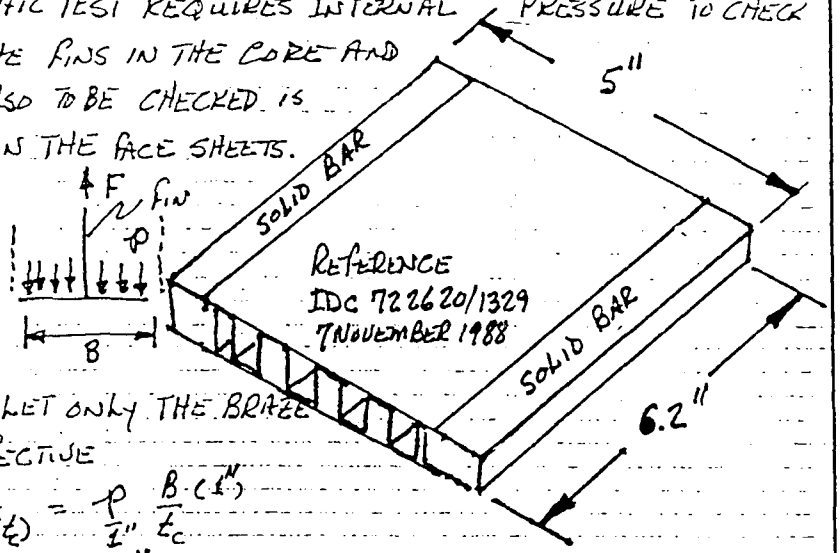
350 PSIG (BURST)

Full VACUUM

SRU DISSIPATORS (6.2 INCH x 5 INCH PLATE) HEAT EXCHANGER



A PROPOSED HOLOGRAPHIC TEST REQUIRES INTERNAL PRESSURE TO CHECK BRAZING BETWEEN THE FINS IN THE CORE AND THE FACE SHEET. ALSO TO BE CHECKED IS THE BENDING STRESS IN THE FACE SHEETS.



BRAZING STRESS:

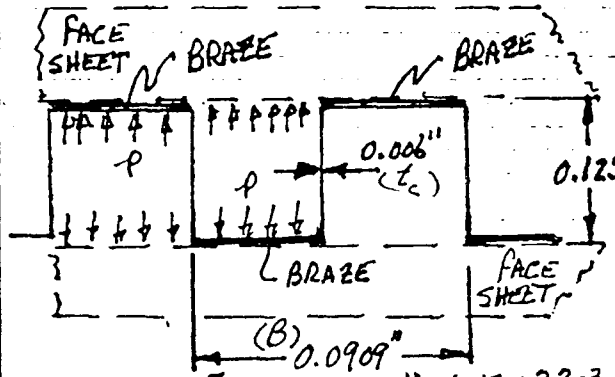
NOW FOR EACH INCH OF LENGTH

$F = p \frac{\#}{in^2} B(in)\ 1in$

IN THE WORST CASE LET ONLY THE BRAZE UNDER THE FIN BE EFFECTIVE

$$\sigma_{FIN} = \sigma_{BRAZE} = \frac{F}{1"(t_c)} = p \frac{B(1")}{1" \ t_c}$$

HERE WE HAVE $B/t_c = \frac{0.0909"}{0.006"} = 15.15$



FIN SPACING HS6013-33-3
6061-T6 ALUMINUM

ALSO THE FIN STOCK 6061-T6 $\sigma_{ult} \approx 42{,}000$ psi

$$p = \frac{42{,}000 \text{ psi}}{1.5(15.15)} = 1848 \text{ psig}$$ INTERNAL PRESSURE TO FAIL THE FIN STOCK.

NOW THE BRAZE IS GENERALLY GOOD FOR AROUND 20,000 psi AND IF WE ALLOW AN BRAZE EFFICIENCY OF 0.85 THIS GIVES

$\sigma_{BRAZE\ ALLOWABLE} = 0.85(20{,}000 \text{ psi}) = 17{,}000$ psi

IF THE FACTOR OF SAFETY IS 1.5

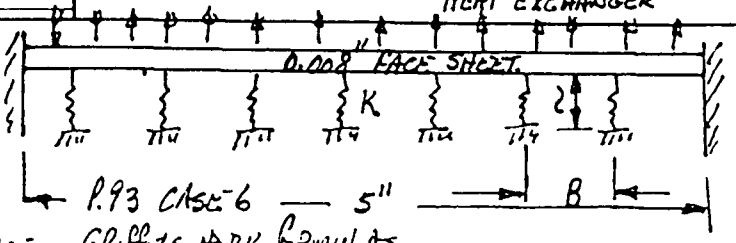
$$F.S. = \frac{\sigma_{BRAZE\ ALLOWABLE}}{\sigma_{BRAZE}}$$

OR

$$p = \frac{17{,}000 \text{ psi}}{1.5(15.15)} = 748 \text{ psig}$$ INTERNAL PRESSURE TO FAIL THE BRAZE

NEXT THE BENDING STRESS IN THE 0.008" THICK FACE SHEETS MUST BE CHECKED.

SRU DISSIPATORS (6.2 INCH X 5 INCH PLATE) HEAT EXCHANGER



BENDING STRESS IN FACE SHEET:

$$\underset{(\text{in-}\#)}{M} = -\frac{\delta}{2\lambda^2}(K_m)\ \frac{\#/in}{(1/in)^2}$$

K_m AT END = 1 MAXIMUM

WITH $\lambda = \sqrt[4]{\frac{k}{4EI}}$ EI FACE SHEET

GRIFFELS HANDBK FORMULAS FOR STRESS AND STRAIN

$$\lambda = \sqrt[4]{\frac{32.7393\times10^6\ lb/in^2}{4\times10\times10^6\ psi\ \frac{6.2"(0.008")^3}{12}}}$$

ALSO $k = \frac{K}{B} = \frac{AE}{\ell B} = \frac{6.2"(0.006")\ 10\times10^6\ \#/in^2}{0.125"(0.0909)}$

$k = 32.7393\times10^6\ lb/in^2$

$\lambda = 41.94\ \frac{1}{in}$ $\quad \lambda L = 41.94\ \frac{1}{in}\ 5in = 209.7$

NOW SUBSTITUTING

$$M = -\frac{P\ 6.2"}{2\ (41.94\ \frac{1}{in})^2} = 0.0018P$$

NOW

$$\sigma = \frac{Mc}{I} = \frac{6M}{bh^2} = \frac{6(0.0018P)}{6.2(0.008")^2} = 26.6488P$$

IF THE FACE SHEET $\sigma_{ult} = 42{,}000$ psi AND A F.S. = 1.5

$$F.S. = 1.5 = \frac{42{,}000\ psi}{26.6488P}$$

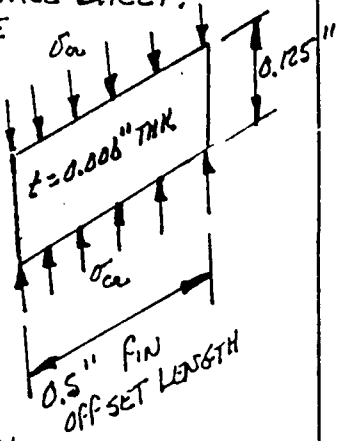
$$P = \frac{42{,}000\ psi}{1.5\ (26.6488)} = 1051\ psig$$ TO FAIL THE FACE SHEET! WITH INTERNAL PRESSURE

VACUUM CHECK FOR FIN CRUSHING:

DEVELOPE THE BUCKLING STRESS FOR SIMPLY SUPPORTED ENDS

$$F_{Cu} = A\sigma_{CR} = \frac{\pi^2 EI}{L^2} = \frac{\pi^2\ 10\times10^6\ \#/in^2\ \frac{(0.5")(0.006")^3}{12}}{(0.125")^2} = 56.8489\ lbs$$

ALSO $\sigma_{FIN} = \frac{F}{0.5"t_c} = \frac{\frac{1"}{8}P(\frac{B}{t_c})}{0.5"} = P\ \frac{15.15}{0.5}\ 0.5" = 15.15P$



NOW IF F.S. = 1.5

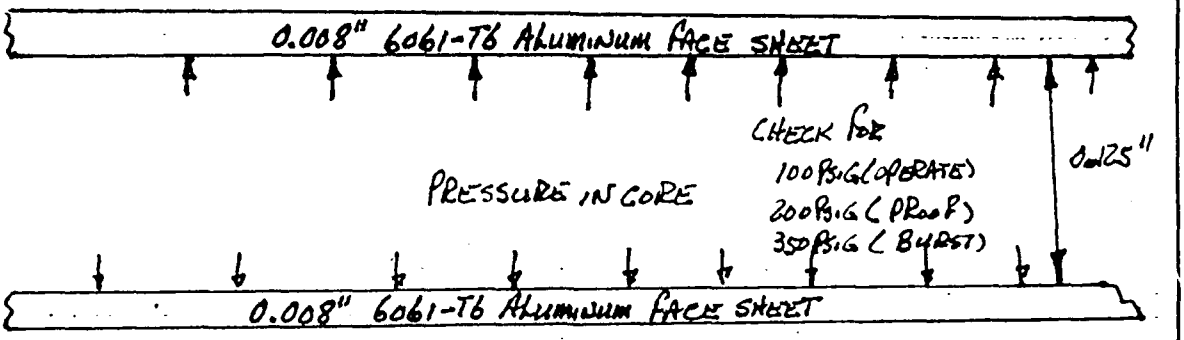
$$F.S. = 1.5 = \frac{\sigma_{CR}}{\sigma_{FIN}} = \frac{56.8489\ lbs}{0.5"(0.006")}\ \frac{1}{15.15P}$$

SOLVE FOR

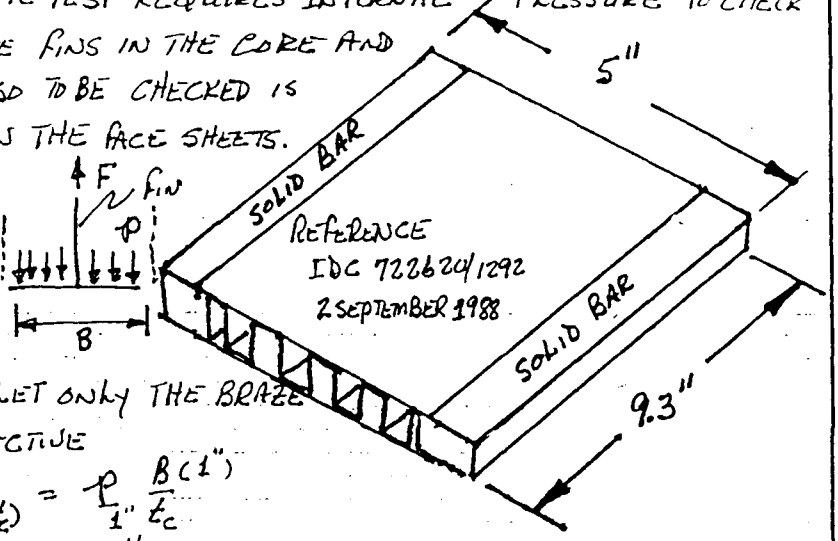
$$P = \frac{56.8489\ lbs}{1.5(0.5")(0.006")(15.15)} = 834\ \#/in^2(psig)$$ EXTERNAL PRESSURE TO CRUSH THE CORE

NOTE: VACUUM IS 14.7 psig EXTERNAL PRESSURE

SRU DISSIPATORS (9.3 INCH X 5 INCH PLATE) HEAT EXCHANGER



A PROPOSED HOLOGRAPHIC TEST REQUIRES INTERNAL PRESSURE TO CHECK BRAZING BETWEEN THE FINS IN THE CORE AND THE FACE SHEET. ALSO TO BE CHECKED IS THE BENDING STRESS IN THE FACE SHEETS.



BRAZING STRESS:

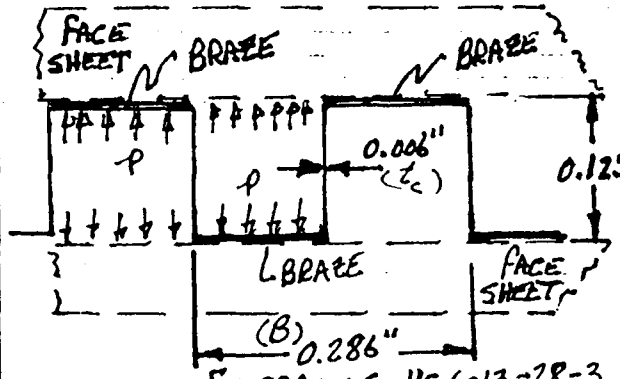
NOW FOR EACH INCH OF LENGTH

$F = P \frac{\#}{in^2} B(in)\ 1in$

IN THE WORST CASE LET ONLY THE BRAZE UNDER THE FIN BE EFFECTIVE

$$\sigma_{FIN} = \sigma_{BRAZE} = \frac{F}{1"(t_c)} = P \frac{B(1")}{1" \quad t_c}$$

HERE WE HAVE $B/t_c = \frac{0.286"}{0.006"} = 47.67$



FIN SPACING HS6013-28-3
6061-T6 ALUMINUM

ALSO THE FIN STOCK 6061-T6 $\sigma_{ult} \approx 42{,}000$ psi

$$P = \frac{42{,}000 \text{ psi}}{1.5(47.67)} = 587 \text{ psig}$$ INTERNAL PRESSURE TO FAIL THE FIN STOCK.

NOW THE BRAZE IS GENERALLY GOOD FOR AROUND 20,000 psi AND IF WE ALLOW AN BRAZE EFFICIENCY OF 0.85 THIS GIVES

$\sigma_{BRAZE\ ALLOWABLE} = 0.85(20{,}000 \text{ psi}) = 17{,}000$ psi

IF THE FACTOR OF SAFETY IS 1.5

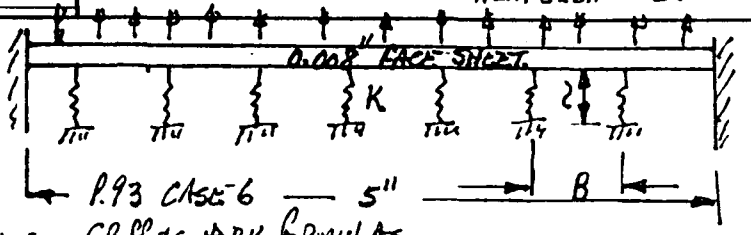
$$F.S. = \frac{\sigma_{BRAZE\ ALLOWABLE}}{\sigma_{BRAZE}}$$

OR

$$P = \frac{17{,}000 \text{ psi}}{1.5(47.67)} = 238 \text{ psig}$$ INTERNAL PRESSURE TO FAIL THE BRAZE

NEXT THE BENDING STRESS IN THE 0.008" THICK FACE SHEETS MUST BE CHECKED.

SRU DISSIPATORS (9.3 INCH X 5 INCH PLATE)
HEAT EXCHANGER



$$M_{(in\#)} = -\frac{\beta}{2\lambda^2}(K_M)\ \frac{\#/in}{(1/in)^2}$$

K_M AT END = 1 MAXIMUM

P.93 CASE 6 — 5" — B

WITH

$$\lambda = \sqrt[4]{\frac{k}{4EI}}$$

EI FACE SHEET

GRIFFELS HDBK FORMULAS FOR STRESS AND STRAIN

$$\lambda = \sqrt[4]{\frac{15.608\times10^6\ lb/in^2}{4\times10\times10^6\ psi\ \frac{9.3"(0.008")^3}{12}}}$$

ALSO $k = \frac{K}{B} = \frac{AE}{\ell B} = \frac{9.3"(0.006")\ 10\times10^6\ \#/in^2}{0.125"(0.286")}$

$k = 15.608\times10^6\ lb/in^2$

$\lambda = 31.49\ \frac{1}{in}$ $\quad \lambda L = 31.49\frac{1}{in}\ 5in = 157$

NOW SUBSTITUTING

$$M = -\frac{P\,9.3"}{\lambda(31.49\frac{1}{in})^2} = 0.0047P$$

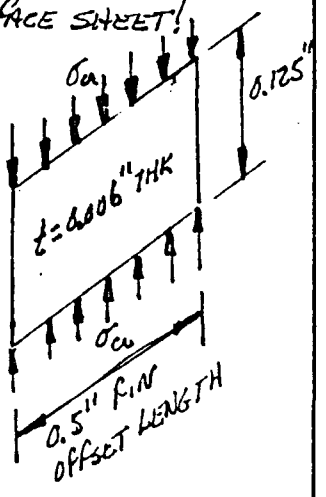
NOW

$$\sigma = \frac{Mc}{I} = \frac{6M}{bh^2} = \frac{6(0.0047P)}{9.3"(0.008")^2} = 47.2692P$$

IF THE FACE SHEET $\sigma_{ult} = 42{,}000$ psi AND A F.S. = 1.5

$$F.S. = 1.5 = \frac{42{,}000\ psi}{47.2692P}$$

$$P = \frac{42{,}000\ psi}{1.5(47.2692)} = 592\ psig$$ TO FAIL THE FACE SHEET!



VACUUM CHECK FOR FIN CRUSHING:

DEVELOPE THE BUCKLING STRESS FOR SIMPLY SUPPORTED ENDS.

$$F_{CR} = A\sigma_{CR} = \frac{\pi^2 EI}{L^2} = \frac{\pi^2 10\times10^6\ \#/in^2\ \frac{(0.5)(0.006)^3}{12}}{(0.125")^2} = 56.8489\ lbs$$

NOW $\sigma_{fins} = P(\frac{B}{t_c}) = 47.67P$

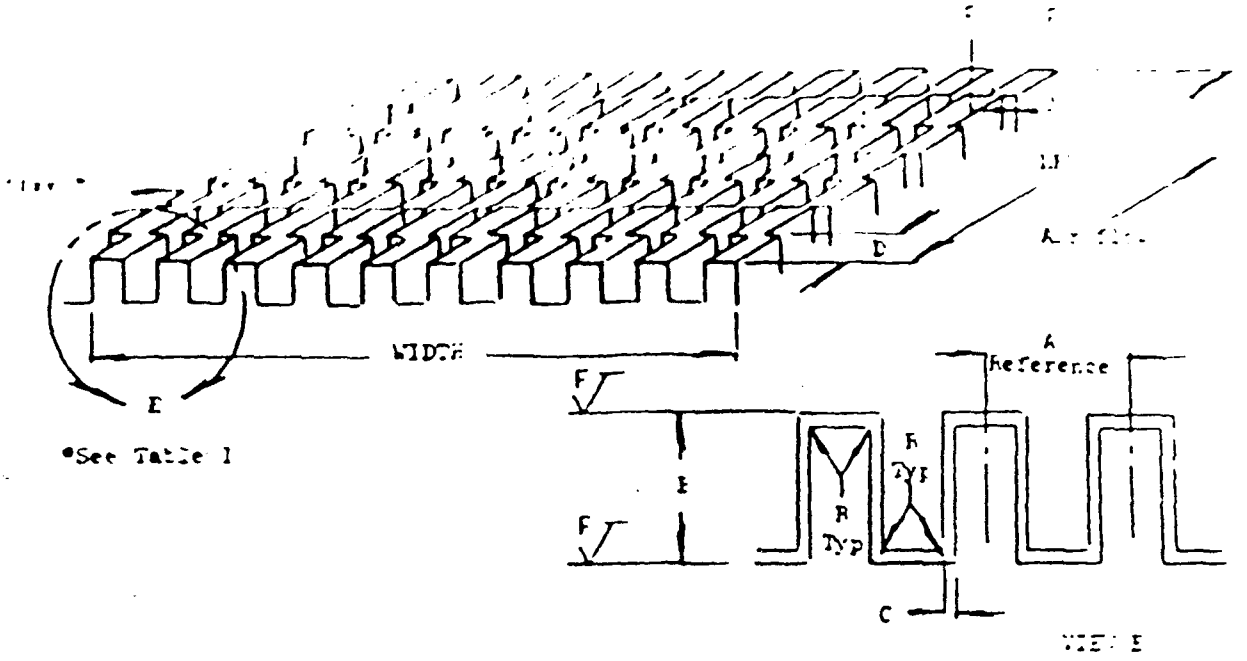
THEN IF F.S. = 1.5

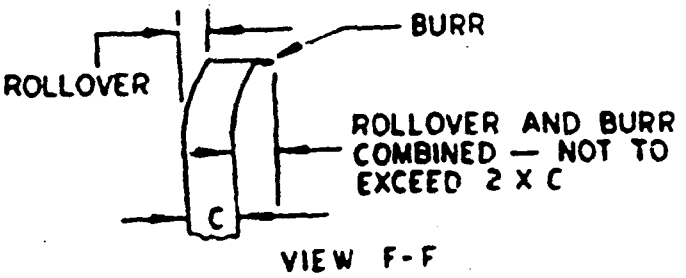
$$F.S. = 1.5 = \frac{\sigma_{CR}}{\sigma_{fins}} = \frac{56.8489\ lbs}{(0.5")(0.006")}\ \frac{1}{47.67P}$$

SOLVE FOR P

$$P = \frac{56.8489\ lbs}{(0.5")(0.006")47.67} = 398\ psig$$ EXTERNAL PRESSURE TO CRUSH CORE

NOTE: VACUUM IS 14.7 Psig EXTERNAL PRESSURE


WIDTH
E
*See Table 1
A
Reference
F
F
B
Typ
B
Typ
C


BURR
ROLLOVER
ROLLOVER AND BURR
COMBINED — NOT TO
EXCEED 2 X C
C

VIEW F-F

61

Bend radii	R = bend radii, 0.005 to 0.030 inch (0.127 to 0.762 millimeters (mm))
Material	(1) 3003 Aluminum Alloy in accordance with QQ-A-250/2, Temper F (2) 1100 Aluminum Alloy in accordance with QQ-A-250/1, Temper O (3) 6061 Aluminum Alloy in accordance with QQ-A-250/11, Temper T62 NOTE: Heat treatment of 6061 material to the T62 temper shall be performed per MIL-H-6088 (4) 6061 Aluminum Alloy in accordance with QQ-A-250/11, Temper O (5) 6951 Aluminum Alloy in accordance with MIL-B-20148 except unclad, Temper F.
Workmanship	The fin material shall be clean, sound and smooth and shall be free of foreign material, tears, holes, and loose burrs and slivers.
Finish	Unless otherwise specified: a. The fin material shall not have a combined metal displacement as a result of rollover and burr which exceeds twice the parent metal thickness, C dimension. b. The fin material shall be coated with preservation oil in accordance with MIL-STD-649.
Length	Length in the direction of air flow shall be as specified and not to exceed 12 inches (305 mm).
Width	Width transverse to the air flow shall be as specified.

7/

Inspection: A sample representative of each lot of fin material shall be selected and visually examined under 10-power magnification for conformance to the requirements of this Specification. (Use Bishop graphics hand-held 10x optical comparator (Catalog No. 3500), Bishop Graphics, Westlake Village, CA 91359 or equivalent.) The -15, -40, -54, and -73 materials shall exhibit no sharp protrusions above the convoluted surfaces (ref. Figure, view E, surface F, and Table I, note 6/.)

Packaging: Material shall be packaged in rolls having an inner diameter of 1 foot (305 mm) void of fin material with a maximum diameter of 3 feet (914 mm).

Manufacturer:

a. Kintex Inc.
210 Dingens St.
Buffalo, NY 14206-2310
FSCM no. 53076

b. Lockhart Industries, Inc.
15555 Texaco Avenue
Paramount, CA 90723-3921
FSCM no. 27110

c. Hughes-Treitler Mfg. Corp.
300 Endo Blvd.
Garden City, NY 11530-6708
FSCM no. 12536

d. United Aircraft Products, Inc.
Dayton International Airport
Box 90007
Dayton, OH 45490
FSCM no. 78943

e. Thompson Industries Ltd.
13100 South Yukon St.
Hawthorne, CA 90250-5426
FSCM no. 26002

f. Vac-Aero International Inc.
1371 Speers Road
Oakville, Ontario L6L 2X5
Canada
FSCM no. none assigned

Part Number Examples:	Description of Part Number:
HS 6013-2	One material callout. The dash number designates a size and a material as specified in Table I.
HS 6013-28	Multiple material callout. The dash number designates the size as specified in Table I. The material can be any material specified in Table I for a specific dash number, unless otherwise specified on the engineering drawing. The material chosen shall be consistent with bonding or brazing documents.
HS 6013-28-1	Specific material callout. The final dash number designates which of the materials specified in Table I for a specific dash number is required. The dash number immediately following HS 6013 designates size as specified in Table I.

Definitions

a. Rollover - Rollover (R) is the amount of plastic deflection formed during finstock stamping operation; see Figure, View F-F.

b. Burr - A burr is a turn-over edge which extends beyond the parent metal thickness; see Figure, View F-F.

TABLE J-1 SIZES

Dash No.	Ref. A 2/ Inch	Offset % of A	F (Inch) ±0.003	C (Inch) ±0.001	D (Inch) ±0.010	Fins per Inch ±1.0 Fin	Material 3/	Manufacturer 4/
1	0.105	16-33	0.100	0.006	0.530 5/	19.0	(1)	a. c. d. e
2	0.133	"	0.153	0.006	0.130	15.0	(1)	a. b. c. d. e
3	0.129		0.190	0.010	0.130	15.5	(1)	a. b. c. d. e
4	0.118		0.072	0.006	0.130	17.0	(1)	a. b. c. d. e
5	0.200		0.072	0.006	0.250	10.0	(1)	a. b. c. d. e
6	0.133		0.100	0.010	0.130	15.0	(1)	a. b. c. d. e
7	0.222		0.190	0.006	0.130	9.0	(1)	a. b. c. d. e
8	0.167		0.250	0.006	0.125	12.0	(1)	a. b. c. d. e
9	0.250		0.440	0.006	0.125	8.0	(1)	a. b. c. d. e
10	0.111		0.380	0.008	0.125	18.0	(1)	a. b. c. d. e
11	0.121		0.352	0.008	0.125	16.5	(2)	a. b. c. d. e
12	0.185		0.352	0.008	0.125	10.8	(2)	a. b. c. d. e. f
13	0.091		0.352	0.008	0.125	22.0	(2)	a. b. c. d. e. f
14	0.200		0.150	0.006	0.130	10.0	(1)	a. b. c. d. e
15 6/	0.167		0.078	0.004	0.500	12.0	(2)	a. b. d. e
16	0.125		0.153	0.006	0.125	16.0	(2)	a. b. c. d. e. f
17	0.125		0.253	0.006	0.125	16.0	(2)	a. b. c. d. e. f
18	0.091	16-33	0.300	0.008	0.125	22.0	(2)	a. b. c. d. e. f
19	0.091	40-60	0.300	0.008	0.125	22.5	(2)	b. c. d. e. f
20	0.125	16-33	0.153	0.006	0.125	16.0	(3)	a. b. c. d. e. f
21	0.125	"	0.253	0.006	0.125	16.0	(3)	a. b. c. d. e. f
22	0.125		0.153	0.006	0.125	16.0	(4)	a. b. c. d. e. f
23	0.125		0.253	0.006	0.125	16.0	(4)	a. b. c. d. e. f
24	0.125		0.364	0.006	0.125	16.0	(2)	a. b. c. d. e. f
25	0.125		0.190	0.006	0.125	16.0	(2)	a. b. c. d. e. f
26	0.125		0.364	0.006	0.125	16.0	(1)	a. b. c. d. e. f
27	0.125		0.190	0.006	0.125	16.0	(1)	a. b. c. d. e. f
28	0.286		0.125	0.006	0.500	7.0	(1)(4)(5)	a. b. c. d. e. f
29	0.100		0.275	0.006	0.125	20.0	(1)	a. b. c. d. e. f
30	0.100		0.275	0.006	0.125	20.0	(2)	a. b. c. d. e. f
31	0.111		0.300	0.006	0.125	18.0	(3)	a. b. c. d. e
32	0.100		0.250	0.006	0.125	20.0	(3)	a. b. c. d. e. f
33	0.109		0.125	0.006	0.500	11.0	(3)	a. b. c. d. e. f
34	0.125		0.125	0.006	0.125	16.0	(1)(4)(5)	a. b. c. d. e. f
35	0.125		0.250	0.006	0.125	16.0	(4)	a. b. c. d. e. f
36	0.091	16-33	0.300	0.008	0.125	22.0	(3)	a. b. c. d. e. f

10/

TABLE J-1 (CONT) 1/

Dash No.	Ref. A 2/ Inch	Offset % of A	B (Inch) ±0.003	C (Inch) ±0.001	D (Inch) ±0.010	Fins per Inch ±1.0 Fin	Material 3/	Manufacturer 4/
37	0.125	16-33	0.300	0.006	0.125 5/	16.0	(1)(4)(5)	a, b, c, d, e, f
38	0.166	↓	0.300	0.006	0.188	12.0	(4)	b, c, d, e, f
39	0.125		0.190	0.006	0.125	16.0	(4)	a, b, c, d, e, f
40 6/	0.125		0.153	0.010	0.125	16.0	(3)	a, b, c, d, e
41	0.125		0.253	0.010	0.125	16.0	(3)	a, b, c, d, e, f
42	0.166		0.300	0.010	0.188	12.0	(4)	b, c, d, e, f
43	0.286		0.125	0.010	0.500	7.0	(1)(4)(5)	a, b, c, d, e
44	0.167		0.250	0.006	0.500	12.0	(1)	a, b, c, d, e, f
45	0.100		0.190	0.006	0.125	20.0	(1)(2)(3)	a, b, c, d, e, f
46	0.133		0.300	0.008	0.125	15.0	(2) (4)	a, b, c, d, e
47	0.200		0.300	0.008	0.125	10.0	(2) (4)	a, b, c, d, e, f
48	0.286		0.100	0.006	0.500	7.0	(1)(4)(5)	a, b, c, d, e
49	0.166		0.125	0.006	0.125	12.0	(1)(4)(5)	a, b, c, d, e
50	0.166		0.125	0.006	0.250	12.0	(1)(2)(3)(4)(5)	a, b, c, d, e
51	0.121		0.352	0.008	0.125	16.5	(1)	a, b, c, d, e, f
52	0.185		0.352	0.008	0.125	10.8	(1)	a, b, c, d, e, f
53	0.091		0.352	0.008	0.125	22.0	(1)	a, b, c, d, e, f
54 6/	0.167		0.078	0.004	0.500	12.0	(1)	a, b, d, e
55	0.125		0.153	0.006	0.125	16.0	(1)	a, b, c, d, e, f
56	0.125	↓	0.253	0.006	0.125	16.0	(1)	a, b, c, d, e, f
57	0.091	16-33	0.300	0.008	0.125	22.0	(1)	a, b, c, d, e, f
58	0.091	40-60	0.300	0.008	0.125	22.5	(1)	b, c, d, e
59	0.125	16-33	0.153	0.006	0.125	16.0	(1)	a, b, c, d, e, f
60	0.125	↓	0.253	0.006	0.125	16.0	(1)	a, b, c, d, e, f
61	0.125		0.153	0.006	0.125	16.0	(1)	a, b, c, d, e, f
62	0.125		0.253	0.006	0.125	16.0	(1)	a, b, c, d, e, f
63	0.125		0.364	0.006	0.125	16.0	(1)	a, b, c, d, e, f
64 7/								
65	0.100		0.276	0.006	0.125	20.0	(1)	a, b, c, d, e, f
66	0.111		0.300	0.006	0.125	18.0	(1)	a, b, c, d, e
67	0.100		0.250	0.006	0.125	20.0	(1)	a, b, c, d, e, f
68	0.190		0.125	0.006	0.600	11.0	(1)	a, b, c, d, e, f
69	0.125	16-33	0.250	0.006	0.125	16.0	(1)	a, b, c, d, e, f

11/

TABLE J-1 (CONT) 1/

Dash No.	Ref. A 2/ Inch	Offset % of A	B (Inch) ±0.003	C (Inch) ±0.001	D (Inch) ±0.010	Fins per Inch ±1.0 Fin	Material 3/	Manufacturer 4/
70	0.091	16-33	0.200	0.006	0.125	22.0	(1)	a, b, c, d, e, f
71	0.166	"	0.300	0.006	0.188	12.0	(1)	b, c, d, e, f
72 7/								
73 6/	0.125		0.153	0.010	0.125	16.0	(1)	a, b, c, d, e
74	0.125		0.253	0.010	0.125	16.0	(1)	a, b, c, d, e, f
75	0.166		0.300	0.010	0.188	12.0	(1)	b, c, d, e, f
76	0.133	"	0.300	0.008	0.125	15.0	(1)	a, b, c, d, e, f
77	0.200	16-33	0.300	0.008	0.125	10.0	(1)	a, b, c, d, e, f

1/ Dimension metric conversions are as follows:

Inch	Millimeters	Inch	Millimeters	Inch	Millimeters
0.001	0.025	0.118	2.997	0.250	6.350
0.003	0.076	0.121	3.073	0.253	6.426
0.004	0.102	0.125	3.175	0.300	7.620
0.006	0.152	0.129	3.277	0.352	8.941
0.008	0.203	0.130	3.302	0.364	9.246
0.010	0.254	0.133	3.378	0.380	9.652
0.015	0.381	0.150	3.810	0.440	11.176
0.072	1.829	0.153	3.886	0.500	12.700
0.078	1.881	0.167	4.242	0.530	13.462
0.091	2.311	0.190	4.826	1.000	25.400
0.100	2.540	0.200	5.080		
0.105	2.667	0.222	5.639		

2/ Reference dimension "A" is based on "Fins per inch".

3/ Aluminum alloy 3003, (1), is non-heat-treatable and will be changed to an annealed temper if exposed to brazing temperatures.

4/ This column indicates manufacturer who either has tooling available or has the capability for producing tooling for the dash number specified.

5/ "D" dimensions for dash 1 only has ±0.015 inch tolerance.

6/ The fin material shall be spanked to the specified B dimension (see Figure, View E, surface [illegible]).

7/ Dash number 27 meets all requirements specified for dash number 64 and 72 and may be used where 64 and 72 are called out.

RELEASE AND REVISION RECORD

Rev	Authority	Description	Release Date	Release Approval
--	--	Initial release as MS 6013	10/3/50	--
I thru 27	--	Record of changes are contained in the document history file.	--	--
28	CMER 64653	Record change	11/26/84	T.Geneczko
29	TSER 66425	Table I, revised Manufacturer column, added footnote 6/ to dash 40 entry, added dash numbers 48 through 77.	5/20/86	A.Zyskowski
30	TSER 66425	P3: Added Vac-Aero as manufacturer "f". P4-6: Table I, revised to reflect the addition of manufacturer "f" to certain dash nos.	02/06/87	A. Roberts

RELEASED PRINT
RESPONSIBLE ENGINEERING ACTIVITY

[redacted] 76-22-20

REV 30 02/06/87 [redacted]

	8	MS 6013

14/12

2123

APPENDIX K

DETAILED FABRICATION ROUTE SHEET FOR 2102 MODULE

Procurement/Assembly of Timing & Control Module, P/N 3562102-5

PHASE 1	o Procure Parts/Materials
PHASE 2	o Assemble/Test/Parylene Coat Modules o Close Modules to Stores
PHASE 3	o Send Modules to TSD for Fracture Mechanics evaluation. o Perform Power On Screening/System Burn-In
PHASE 4	o Deliver Module to TSD

PHASE 1 Procure Parts/Materials

Oper. No.	Actionee	Description of Task or Operation
1-0001		Procure Parts/Materials Send PWBs & Heat Exchanger to TSD for holographic interferometry.
1-0003		Assemble Printed Wiring Board Assembly, P/N 3562150-025. o Etch PWB o Bond PWB to Heat Exchanger o Airflow & Pressure Drop Test. Data to be retained.*
1-0005		Package PWB Assembly and Parts into Kits
1-0007		Sends Kits to TSD for holographic interferometry of PWB to heat exchanger bond and x-ray, leak testing, and O_{JC} measurements of active devices.
1-0008		Return Kits to RSG-POD
1-0010		Release Kits to the Line

* In addition to normal fabrication processes.

PHASE 2 Assemble/Test/Parylene Coat

Oper. No.	Actionee	Description of Task or Operation
2-0020	16-23	Stencil
2-0030	16-23	Reflow solder flatpacks using machine. Check solder composition.*
2-0040	16-23	Reflow solder axial components using machine. Check solder composition.*
2-0050	16-23	Install manual components.
2-0060	16-23	Verify components and touch up. Record quantity of joints touched up.
2-0070	16-23	Operator review previous operations.
2-0080	16-23	Install pads artwork #2402-3.
2-0090	16-25	Install jumper wires artwork #2402-3.
2-0100	16-25	Install spring pins.
2-0110	16-25	Operator review previous operations.
2-0120	16-25	Clean.
2-0122	76-41	Send module to TSD for holographic interferometry of module
2-0123	76-41	Return module to RSG-POD.
2-0130	16-14	Module condition.
2-0140	32-15	Test TSC AXX.
2-0150	16-25	Operator review previous operations.
2-0155	16-26	Detrex clean per PG's P1 & P2.
2-0160	32-25	Post Test inspect IL J.
2-0162	76-41	Send module to TSD for holographic interferometry of module.

2-0163	76-41-	Return to module to RSG-POD.
2-0170	16-26	Bond wires per PG's P1.
2-0180	16-26	Adhesive clean per PG's P3 & P4.
2-0190	16-26	Adhesive bond per PG's P1 & P2.
2-0200	16-26	Operator review previous operations.
2-0210	16-26	Clean and prime per PG's P3 & P4.
2-0215	16-26	Remove extractor.
2-0220	16-26	Mask per PG's P3 & P4.
2-0225	16-26	Operator review previous operations.
2-0230	31-43	Inspect IL B.
2-0240	16-26	Parylene per PG's P3 & P4. Run No. _____/
2-0250	16-26	Demask.
2-0255	16-26	Clean connector.
2-0260	16-26	Operator self check (4X).
2-062	16-26	Install extractor.
2-0262	16-26	Inspect IL P. Thickness is:_____
2-0270	32-15	Test TSC. BXX.
2-0280	37-25 16-25	Complete item inspect IL C. Close to 08-44 project. Stores transact to 08-44-42.

* In addition to normal fabrication processes.

PHASE 3 TSD Evaluation/Power On Screening/System Burn-In

Oper. No.	Actionee	Description of Task or Operation
3-0401		Return Module to RSG-POD.
3-0410		Perform Power On Screening.
3-0412		Send Module to TSD for holographic interferometry of module.
3-0413		Return Module to RSG-POD.
3-0420		Perform System Burn-In for one cycle.

PHASE 4 Deliver Module to TSD

APPENDIX L

HYBRID ROUTE SHEET

PROGRAM Regulator | HYBRID LOT TRAVELER | QTY _____

REF. F.C. 60134 REV W | LOT NO. _____

CAUTION: STATIC SENSITIVE

OP. NO.	OPERATION	PROCESS SPEC.	QTY ACC	QTY REJ	OPR	DATE	COMMENTS REWORK INSTR.
1	CLEAN PARTS	DP 10001					
*2	SOLDER REFLOW POWER TRANSISTOR SN 96	DP 60009					
	REMOVE FLUX AND CLEAN	DP 10003					
3	MOUNT SUBSTRATES AND C1 ABLEFILM 550	DP 10006					
	CURE 2 HRS. @ 150°C (4)						BATCH#
4	ULTRASONIC BOND POWER TRANSISTOR LEADS	DP 60435					
*5	VERIFY POWER TRANSISTOR POLARITY	DP 60440					
	[ ] PS 60568-3 [ ] PS 60569-3						
*6	WELD STRAPS (1)	DP 10007					
*7	MOUNT SILICON DEVICES 36-2 (5)	DP 10008					BATCH#
	CURE .5 HRS. @ 150°C						
8	PRODUCTION IN LINE VISUAL (7)	DP 60012					RWK
*9	BOND INTERCONNECTS (AUTO)	DP 60684					MACH# TIME AM PM
	BOND INTERCONNECTS (MAN) (6)	DP 10020					MACH# TIME AM PM
*10	WIRE BOND DEVICES (AUTO)	DP 60684					MACH# TIME AM PM
	WIRE BOND DEVICES (MAN) (3)	DP 60677					MACH# TIME AM PM
11	PRODUCTION IN LINE VISUAL (7)	DP 60012					RWK
*12	REMOVE LEAD COMB FRAME	DP 10010					
*13	THETA J/C TEST (7)	DP 60049					RWK
14	FUNCTIONAL TEST (7)	DP 60440					RWK
15	DYNAMIC TRIM LASER (8)	DP 71271					
16	FIRST ELECTRICAL TEST, READ & RECORD	DP 60440					RWK
	DATA. VO1. VO20. VOR (7)						
17	PRODUCTION PRECAP VISUAL (7)	DP 60012					RWK
18	O.A. PRECAP INSPECTION (7)	Q 8-11-24					RWK
19	CLEAN ASSEMBLY AND LID	DP 10001					
20	VACUUM BAKE: 4 HRS. @ 125° C	DP 10032					
21	SEAL: SEAM WELDER	DP 60631					
22	GROSS LEAK TEST: FC 40. 30 SEC. @	DP 10014					RWK
	125° C (7)						
23	HIGH TEMP. STORAGE: 24 HRS. @ 150°C	DP 10011					
24	TEMP. CYCLE: 25 CYCLES -65 TO 150°C	DP 10015					
25	MECH. SHOCK TEST: 5 SHOCKS @ 1500 G's	DP 60074					
26	PARTICLE IMPACT NOISE TEST (7)	DP 60001					RWK
27	FINE LEAK TEST: PRESS, 4.0 HRS. @ 30	DP 10014					RWK
	PSIG He≤1 X 10 -7 CC/SEC						
28	GROSS LEAK TEST: COND. C VACUUM 1.0	DP 10014					RWK
	HR. @ 5 TORR. PRESS. 10 HRS. @ 30						
	PSIG (2) (7)						
**29	SYMBOLIZE MODULE	DP 10013					
**30	BURN IN: 168 HRS. @ 125°C (CASE)(TUB	DP 60426					
31	FINAL ELECTRICAL TEST, READ & RECORD	DP 60440					RWK
	VO1, VO 20, VOR, CALCULATE Δ's (7)						
	PER ATP 10405 -80 REV.						

APPROVALS

ORIGINATOR J. Blanchard	DATE 83-11-3	CW Cable Rev V	DATE 83-12-19	Rev V	DATE 4/05/03
RESPONSIBLE ENG.	83/11/3	Rev V	83/12/20	AUTH. FOR DISTRIB.	

PROGRAM Regulator	HYBRID LOT TRAVELER	PART NO.
REF. F.C. FC 60134 REV W		QTY
		LOT NO

CAUTION: STATIC SENSITIVE

OP. NO.	OPERATION	PROCESS SPEC.	QTY ACC	QTY REJ	OPR	DATE	COMMENTS REWORK INSTR.
32	FORM AND TIN LEADS (YELLOW GROUP)	DP 60415					
33	FINE LEAK TEST: PRESS. 4.0 HRS. @ 30	DP 10014					RWK
	PSIG He≤1 X 10-7 ATM CC/SEC (7)						
34	GROSS LEAK TEST: COND. C VACUUM 1.0	DP 10014					RWK
	HRS. @ 5 TORR. PRESS. 10 HRS. @ 30						
	PSIG (2) (7)						
35	FINAL Q.A. INSPECTION (7)	MIL-STD-883					RWK
36	SHIP						

NOTES: * Operations may be worked out of sequence per instructions from the supervisor or the cognizant process engineer.

** Operations may be interchanged per instructions from the supervisor or the cognizant process engineer.

(1) Weld appropriate straps from metallized Beryllia Substrate to package leads per applicable assembly drawing.

(2) Refer to DP 10040 for special handling of "failed units" from this test.

(3) Alternate bonding process per DP 10020, or DP 10007 (Tack down)

(4) Alternate method for mounting substrate is using Scotchcast 281 per DP 10006 and cure @ 125° C for 2 Hrs.

(5) Alternate method is using Ablebond 606-2 per DP 10008 and cure @ 125° C for 2 Hrs.

(6) Alternate method for interconnects is DP 60669 or DP 10007.

(7) If rework is required, refer to DP 10040.

(8) Dynamic Laser Trim only as required by ATP.

REWORK KEY

RWK 8,11,13 Rework per instructions on the lot traveler. Clean assembly per DP 10001 after rework. Inspect per steps 8,11 and proceed sequentially.

RWK 14,16 17,18 Same as RWK 8, 11,13.

RWK 22 Decap per DP 10040. Rework per instructions on the lot traveler. Inspect per steps 8, 11 and proceed sequentially.

RWK 26,27 28,31,33,34,35 Same as RWK 22.

APPENDIX M

DETAILED FABRICATION ROUTE SHEET FOR 9800 MODULE

Procurement/Assembly of Linear Regulator Module, P/N 3569800-10

PHASE 1	o Procure Part/Materials o Procure Hybrids from Hughes Newport Beach
PHASE 2	o Assemble/Test/Parylene Coat Modules o Close Modules to Stores
PHASE 3	o Send Modules to TSD for Fracture Mechanics evaluation o Perform Power On Screening/System Burn-In
PHASE 4	o Deliver Module to TSD

PHASE 1 Procure Parts/Materials

Oper. No.	Actionee	Description of Task or Operation
1-0001		Procure Parts/Materials
1-0002		Procure Hybrids. These Hybrids will be evaluated by TSD during various stages of fabrication. Send PWB & Heat Exchanger to TSD for holographic interferometry.
1-0003		Assemble Printed Wiring Board Assembly, P/N 3569805-005. o Etch PWB o Bond PWB to Heat Exchanger o Airflow & Pressure Drop Test. Data to be retained.*
1-0005		Package PWB Assembly, Parts, and specially evaluated Hybrids into Kits.
1-0007		Send Kits to TSD for holographic interferometry of PWB to heat exchanger bond and x-ray, leak testing, and O_{JC} measurements of active components.
1-0008		Return Kits to RSG-POD.
1-0010		Release Kits to the Line.

* In addition to normal fabrication processes.

PHASE 2 Assemble/Test/Parylene Coat

Oper. No.	Actionee	Description of Task or Operation
2-0015	AW41	Stencil per pgs H1 & H2.
2-0246	AW43	Bond Hybrids per pg 1.
2-0230	AW43	Bond and Assemble per pgs 2 thru 25 Torque pg 6 P/N _____ Tool ID No._____Stamp_____Date_____ Check solder composition.*
2-0425	AW43	Operator Review ref pags 13 & 26.
2-0550	AW52	Incircuit Check.
2-0626	AW43	Operator Review previous operations.
2-0628		Send Module to TSD for holographic interferometry of module.
2-069		Return Module to Hughes South Carolina.
2-0733	AW31	Pretest Inspect.
2-0852	AW52	Module Condition.
2-0954	AW52	Test TSC.AXX TP 3569800-03 Rev._____,TN_____
2-1026	AW43	Operator Review previous operations.
2-1134	AW31	Post Test inspect.
2-1241	AW41	Clean
2-1243		Send Module to TSD for holographic interferometry of module.
2-1244		Return Module to Hughes South Carolina.
2-1346	AW41	Bond per pg 37.
2-1430	AW31	Inspect Bonding.
2-1541	AW41	Clean per pgs 28 & 29.

2-1642	AW41	Prime per pgs 28 & 29.
2-1743	AW41	Mask areas marked with yellow per pgs 28 & 29.
2-1830	AW31	Inspect.
unknown		Parylene coat. Run No._____
unknown		Demask.
unknown		Clean connector.
unknown		Operator self check (4X)
unknown		Inspect. Thickness is:_____
unknown		Test TSC.BXX
2-2699	AW63	Move to Shipping.
unknown		Complete item inspect. Close to F-15 Stores.

* In addition to normal fabrication processes.

PHASE 3 TSD Evaluation/Power On Screening/System Burn-In

Oper. No.	Actionee	Description of Task or Operation
3-3001		Return Module to RSG-POD.
3-3010		Perform Power On Screening.
3-3012		Send Module to TSD for holographic interferometry of module.
3-3013		Return Module to RSG-POD.
3-3020		Perform System Burn-In for one cycle.

PHASE 4 Deliver Module to TSD.

APPENDIX N

PART PLACEMENT FOR ERFM P/N 3562102 MODULES

AVOID VERBAL ORDERS

90-020

TO	SOURCECODE	LOC.	BLDG.	M/S	PHONE
Zach Richardson	76-41-22	E0	E1	C132	64517

FROM	SOURCECODE	LOC.	BLDG.	M/S	PHONE
Dan Buechler	76-41-22	E0	E1	C132	64650

SUBJECT	DATE
Part Placement for ERFM P/N 3562102 Modules	03/20/90

Attached to this AVO are two sets of component maps from the assembly instructions for the F-15 P/N 3562102 module. These maps show the locations chosen for selected ERFM components. The component serial number, for the component of the corresponding part number, has been placed both below the component location and along side the component designation.

The first set of maps should be used in the assembly of the lower serial number of the two modules. The second set of maps will be used for the higher serial number of the two modules. This will assure an approximately equal number of selected components on each module.

Please see me if there is any question concerning the interpretation of these maps.

Daniel W. Buechler

c: J.L. Cool
J.M. Kallis
D.H. Van Westerhuyzen

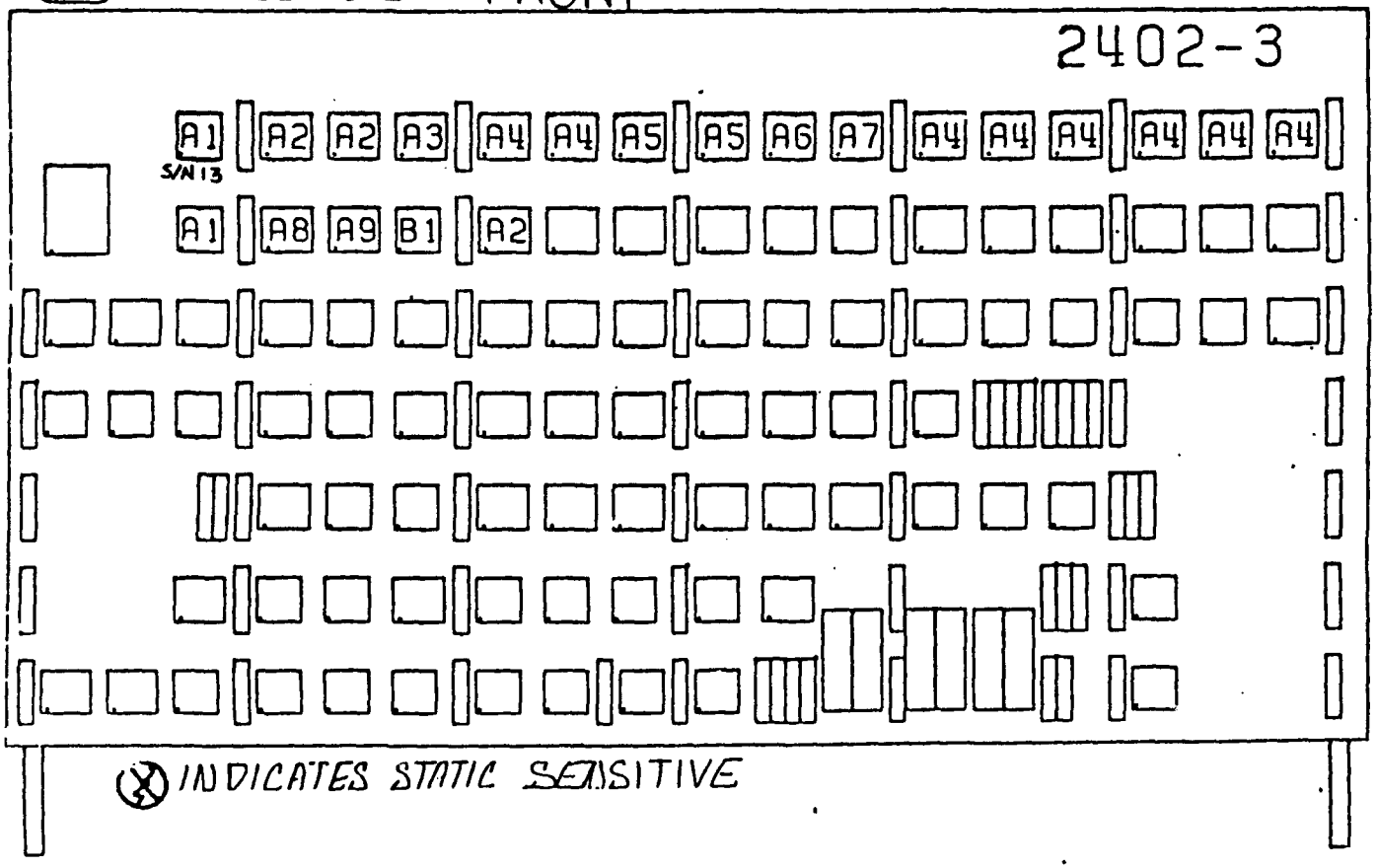
MAP FOR LOWER SERIAL NUMBER ERFM MODULE

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO.		
3562102-5	58	1

REF PG. G1 FOR SOLDER INFO. & G4 FOR MACHINE INFO.
PLACE IN HOLDING FIXTURE FRONT SIDE UP
MACHINE REFLOW SOLDER FLATPACKS

(XX) CUP LOCATORS FRONT



⊗ INDICATES STATIC SENSITIVE

⊗ F2	A1	2	932730-0028	
	(S/N 13)	U1703	U1603	
⊗ E4	A2	3	932709-0018	
		U1704	U1705	
		U1607		
⑤ ⊗ F1	A3	1	932690-0018	
		U1706		
⊗ B9	A4	8	932746-0018	
		U1707	U1708	
		U1713	U1714	
		U1715	U1716	
		U1717	U1718	
⑪ ⊗ E9	A5	2	932732-0018	
		U1709	U1710	
⊗ B3	A6	1	932820-224	
		U1711		
⑭ ⊗ D9	A7	1	M38510/33701BFX	
		U1712		
⑥ ⊗ F5	A8	1	M38510/34102BFX	
		U1604		
⊗ D8	A9	1	M38510/07009BFX	
		U1605		
① ⊗ D7	B1	1	M38510/08001BDX	
		U1606		

SUBSTITUTE PARTS
① M38510/_____BAX ⑪ H9903I6_3B
⑤ M38510/07906 BFX
⑥ H9903D7_1B OR 932711_1B
⑭ 932752_1B

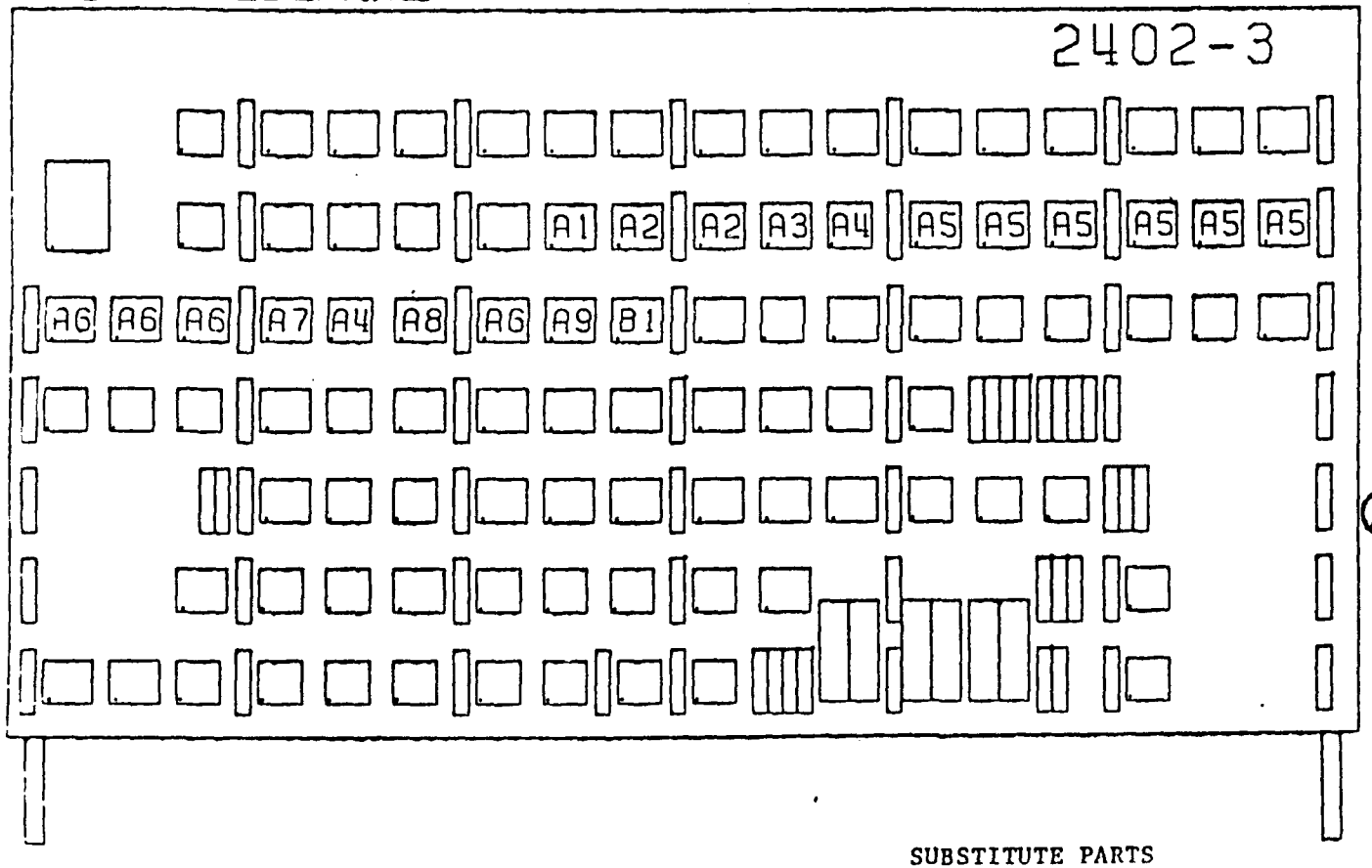
FORM 14133-SA ES

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO.	REV.	PAGE
3562102-5	58	2

REFLOW SOLDER FLATPACKS

(xx) CUP LOCATORS



⊗	A1 B9	1	932746-0018 U1608
(11) ⊗	A2 E9	2	932732-0018 U1609 U1610
⊗	A3 B2	1	932820-215 U1611
(1) ⊗	A4 D5	2	M38510/07003B0X U1612 U1505
⊗	A5 D1	6	932749-0018 U1613 U1614 U1615 U1616 U1617 U1618
⊗	A6 E4	4	932709-0018 U1501 U1502 U1503 U1507
⊗	A7 E5	1	932614-0038 U1504
⊗	A8 D8	1	M38510/07009BFX U1506
⊗	A9 B4	1	932820-217 U1508
⊗	B1 B6	1	932820-219 U1509

SUBSTITUTE PARTS
(1) M38510/_____.BAX

⊗ INDICATES STATIC SENSITIVE

(11) H970316.1B

N-4

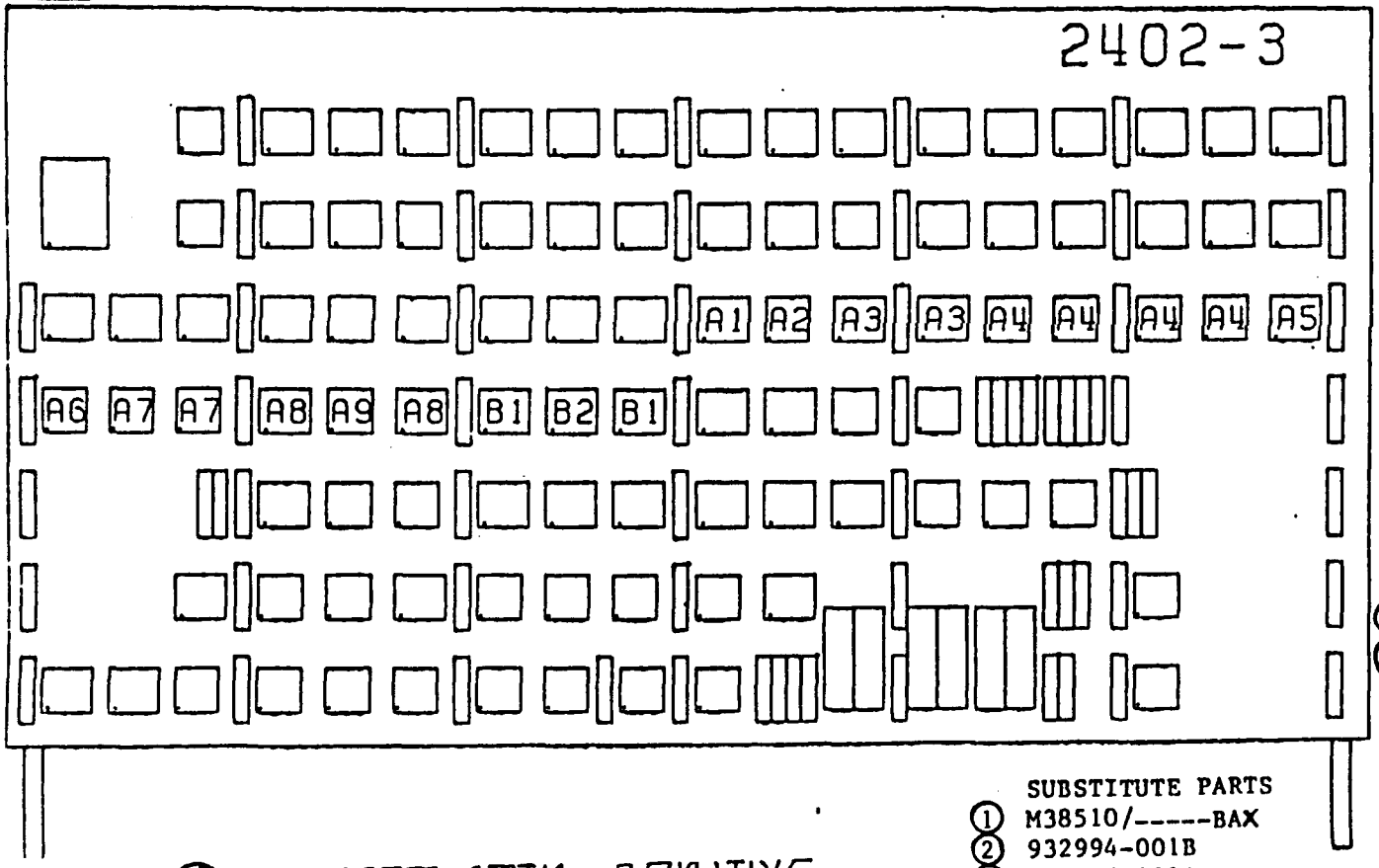
FORM 14133-5A ES

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO.		
3562102-5	5B	3

REFLOW SOLDER FLATPACKS

(XX) CUP LOCATORS



N-5

⊗ INDICATES STATIC SENSITIVE

SUBSTITUTE PARTS
① M38510/-----BAX
② 932994-001B
③ 932725-001B
⑰ H990582-10

⊗	A1	1	932820-220	
	B7	U1510		
⊗	②A2	1	M38510/07501BDX	
	F4	U1511		
⊗	A3	2	932746-0018	
	B9	U1512	U1513	
⊗	①③A4	4	M38510/30605BDX	
	C6	U1514	U1515	
		U1516	U1517	
⊗	A5	1	932749-0018	
	D1	U1518		
⊗	① A6	1	M38510/07006BDX	
	E8	U1401		
⊗	① A7	2	M38510/07401BDX	
	F3	U1402	U1403	
	A8	2	932614-0038	
	E5	U1404	U1406	
⊗	⑰ ① A9	1	M38510/07001BDX	
	D3	U1405		
⊗	B1	2	932727-0018	
	E7	U1407	U1409	
⊗	B2	1	932820-218	
	B5	U1408		

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

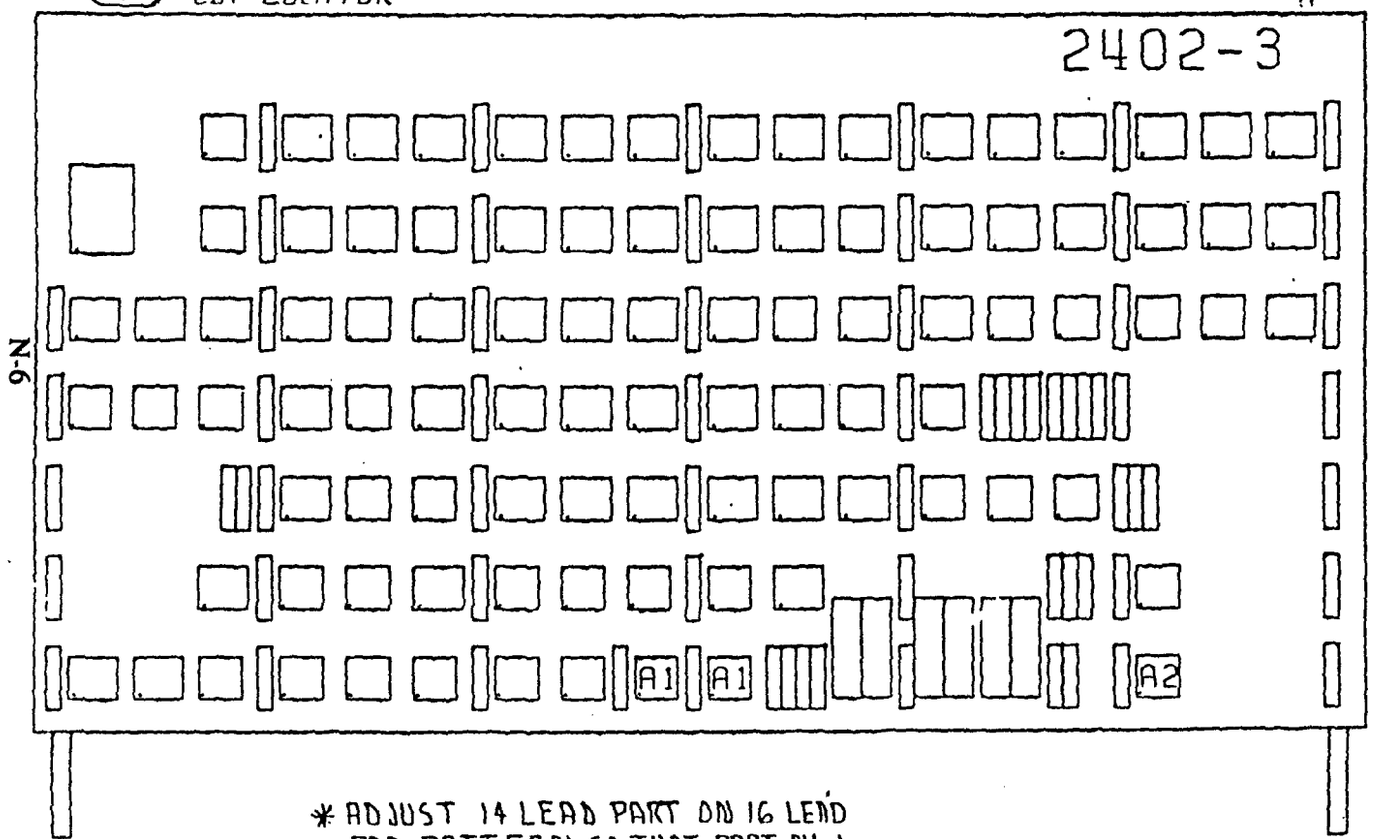
ASSEMBLY NO.	REV.	PAGE
3562102-5	58	6

A1 2 . 932730-0028
F2 U1109 U1110

A2 1 M8340103M27R0JA
H9 *A1116A

REFLOW SOLDER FLATPACKS

(XX) CUP LOCATOR



* ADJUST 14 LEAD PART ON 16 LEAD PAD PATTERN SO THAT PART NO. 1 IS LOCATED ON PAD NO. 1.

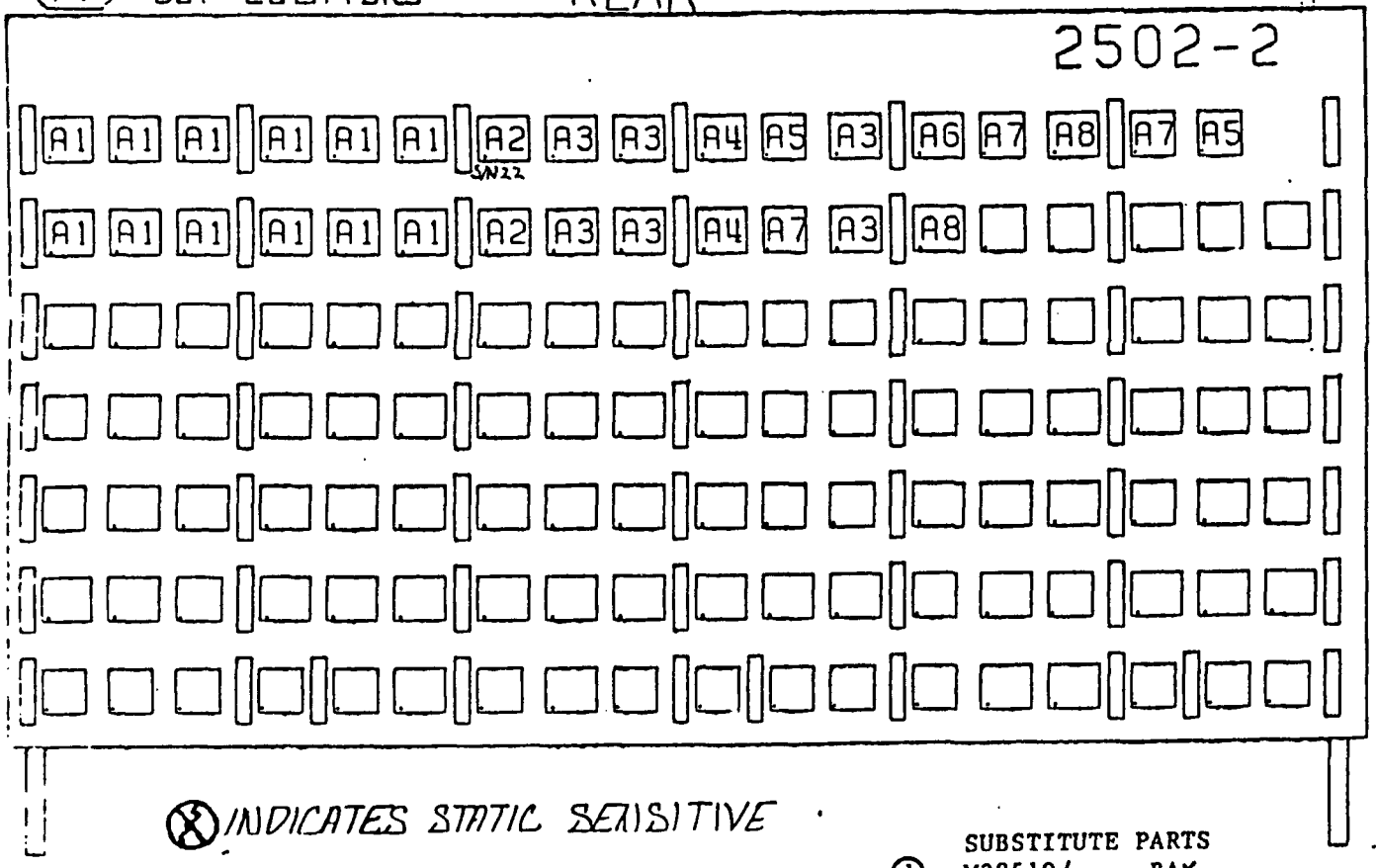
(X) INDICATES STATIC SENSITIVE

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

NO.		
5562102-5	58	7

REF PG. G1 FOR SOLDER INFO. & G4 FOR MACHINE INFO.
PLACE IN HOLDING FIXTURE REAR SIDE UP
MACHINE REFLOW SOLDER FLATPACKS

(XX) CUP LOCATORS REAR



⊗ INDICATES STATIC SENSITIVE

⊗	A1	E6	12	932736-0018
			U2701	U2702
			U2703	U2704
			U2705	U2706
			U2601	U2602
			U2603	U2604
			U2605	U2606
(12) ⊗	A2	E3	2	H990411-1B
		(SN22)	U2707	U2607
(5) ⊗	A3	F1	6	932690-0018
			U2708	U2709
			U2712	U2608
			U2609	U2612
⊗	A4	C5	2	932756-0018
			U2710	U2610
(1) ⊗	A5	D5	2	M38510/07003BDX
			U2711	U2717
⊗	A6	B9	1	932746-0018
			U2713	
(17) (1) ⊗	A7	D3	3	M38510/07001BDX
			U2714	U2716
			U2611	
(6) ⊗	A8	F5	2	M38510/34102BFX
			U2715	U2613

SUBSTITUTE PARTS
(1) M38510/-----BAX
(5) M38510/07906BFX
(6) H990307-1B OR 932711-1B
(12) 932616-501B
(17) H990582-1B

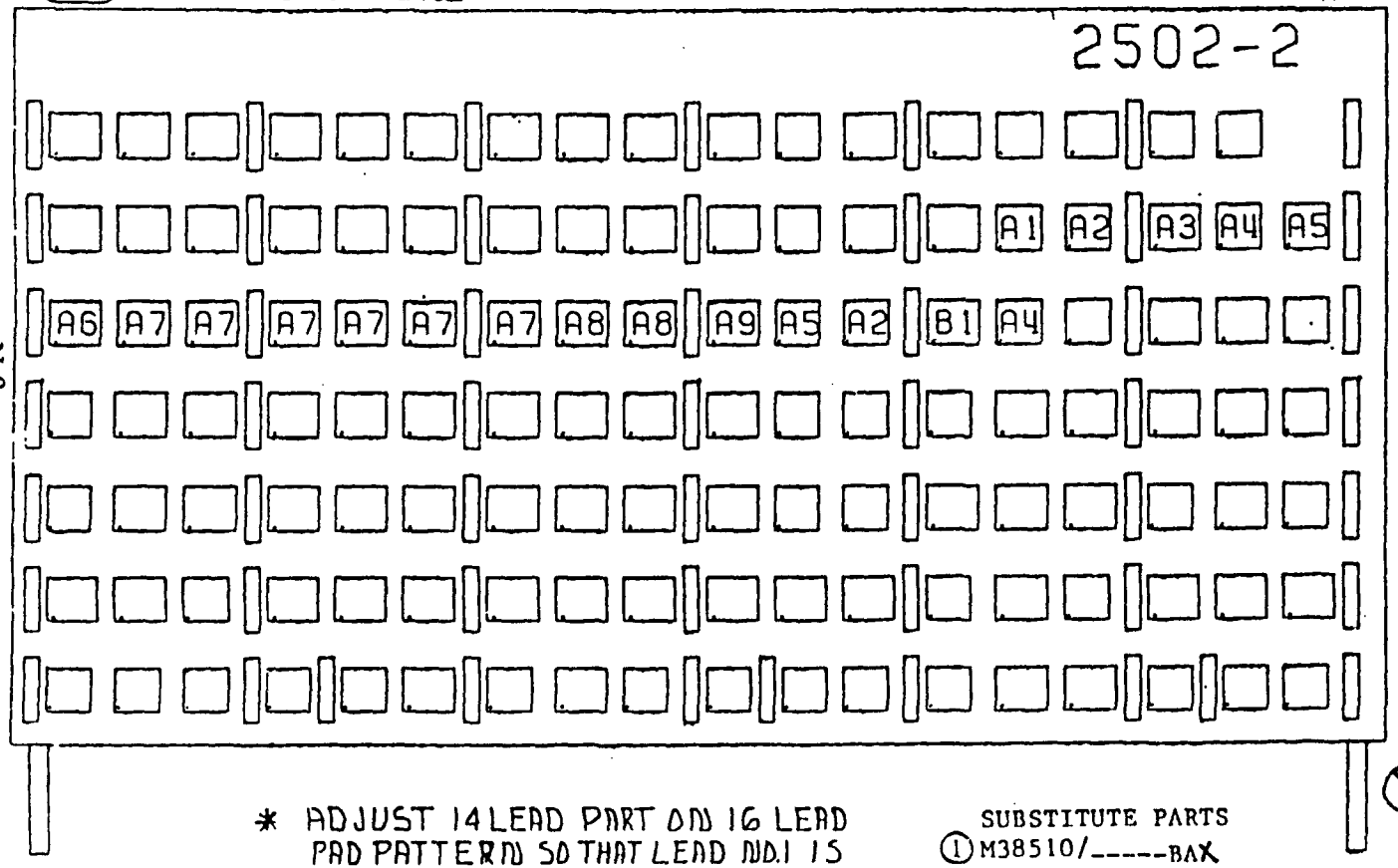
FORM 14133-SA ES

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO. 3562102-5 | 58 | 8

REFLOW SOLDER FLATPACKS

(XX) CUP LOCATORS



N-8

①	A1	1	M38510/30502BDX	
⚡	D2	U2614	—	
①	A2	2	M38510/07003BDX	
⚡	D5	U2615	U2512	
⑮	A3	1	M38510/33901BFX	
	E2	U2616		
①	A4	2	M38510/08001BDX	
⚡	D7	U2617	U2514	
⑰①	A5	2	M38510/07001BDX	
⚡	D3	* U2618	U2511	
	A6	1	932728-0018	
⚡	C9	U2501		
	A7	6	932736-0018	
⚡	E6	U2502	U2503	
		U2504	U2505	
		U2506	U2507	
⑤	A8	2	932690-0018	
⚡	F1	U2508	U2509	
	A9	1	932756-0018	
⚡	C5	U2510		
⚡	B1	1	932614-0038	
	E5	U2513		

* ADJUST 14 LEAD PART ON 16 LEAD PAD PATTERN SO THAT LEAD NO.1 IS LOCATED ON PAD NO.1

⚡ INDICATES STATIC SENSITIVE

SUBSTITUTE PARTS
① M38510/_____BAX
⑤ M38510/07906BFX
⑮ 932837-1B
⑰ H990582-1B

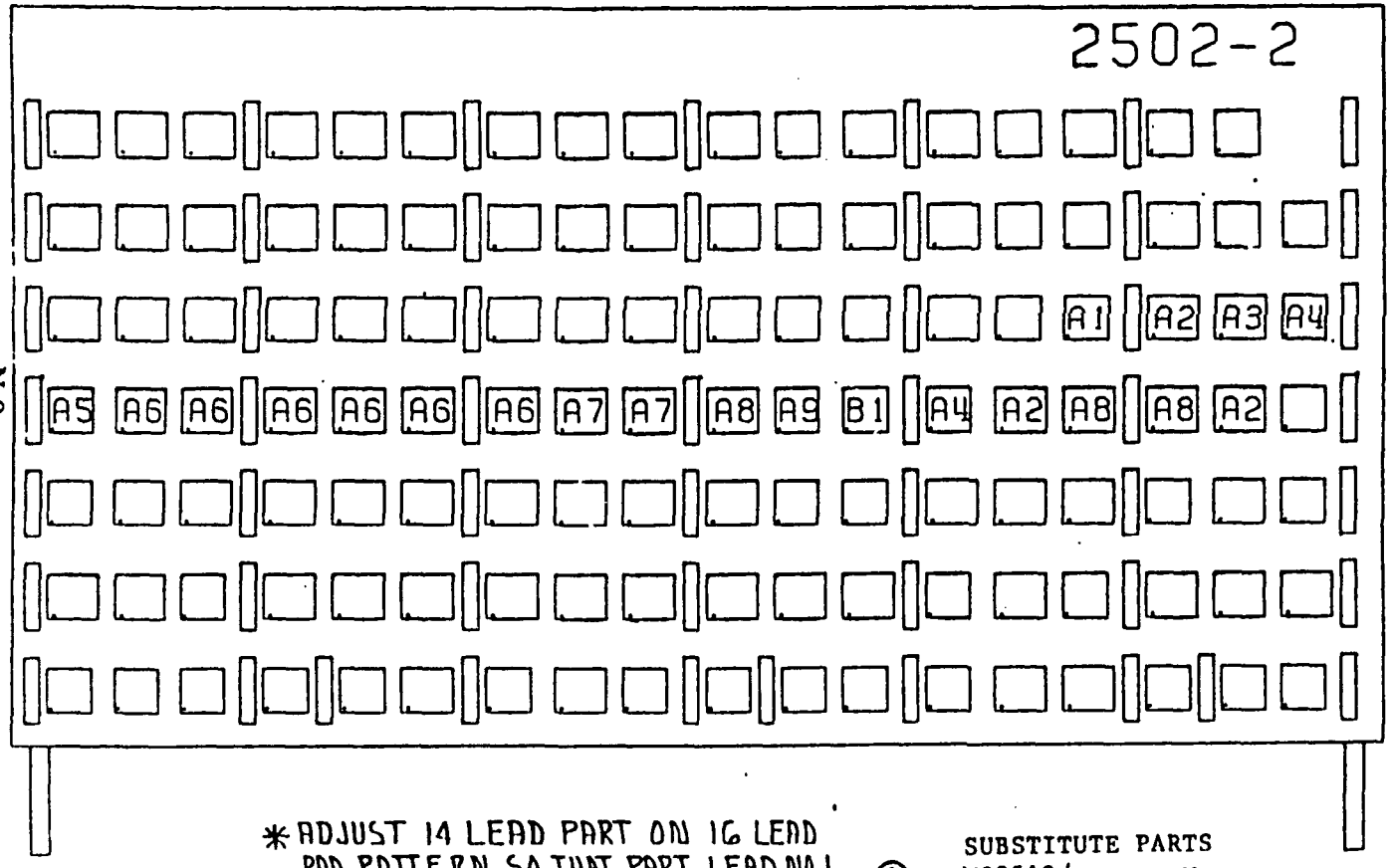
FORM 14133-5A ES

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO.	REV.	PAGE
3562102-5	58	19

REFLOW SOLDER FLATPACKS

(XX) CUP LOCATORS



① ⊗	A1 F3	1	M38510/07401BDX U2515 —
⊗	A2 E5	3	932614-003B U2516 U2414 U2417
⊗	A3 E7	1	932727-001B U2517
① ⊗	A4 D5	2	M38510/07003BDX * U2518 U2413
① ⊗	A5 D4	1	M38510/07301BDX U2401
⊗	A6 E6	6	932736-001B U2402 U2403 U2404 U2405 U2406 U2407
⑤ ⊗	A7 F1	2	932690-001B U2408 U2409
⊗	A8 C5	3	932756-001B U2410 U2415 U2416
① ⊗	A9 C2	1	M38510/30301BDX U2411
⑰ ① ⊗	B1 D3	1	M38510/07001BDX U2412

* ADJUST 14 LEAD PART ON 16 LEAD PAD PATTERN SO THAT PART LEAD NO.1 IS LOCATED ON PAD NO.1.

⊗ INDICATES STATIC SENSITIVE

SUBSTITUTE PARTS
① M38510/-----BAX
⑤ M38510/07906BFX
⑰ A990582_1B

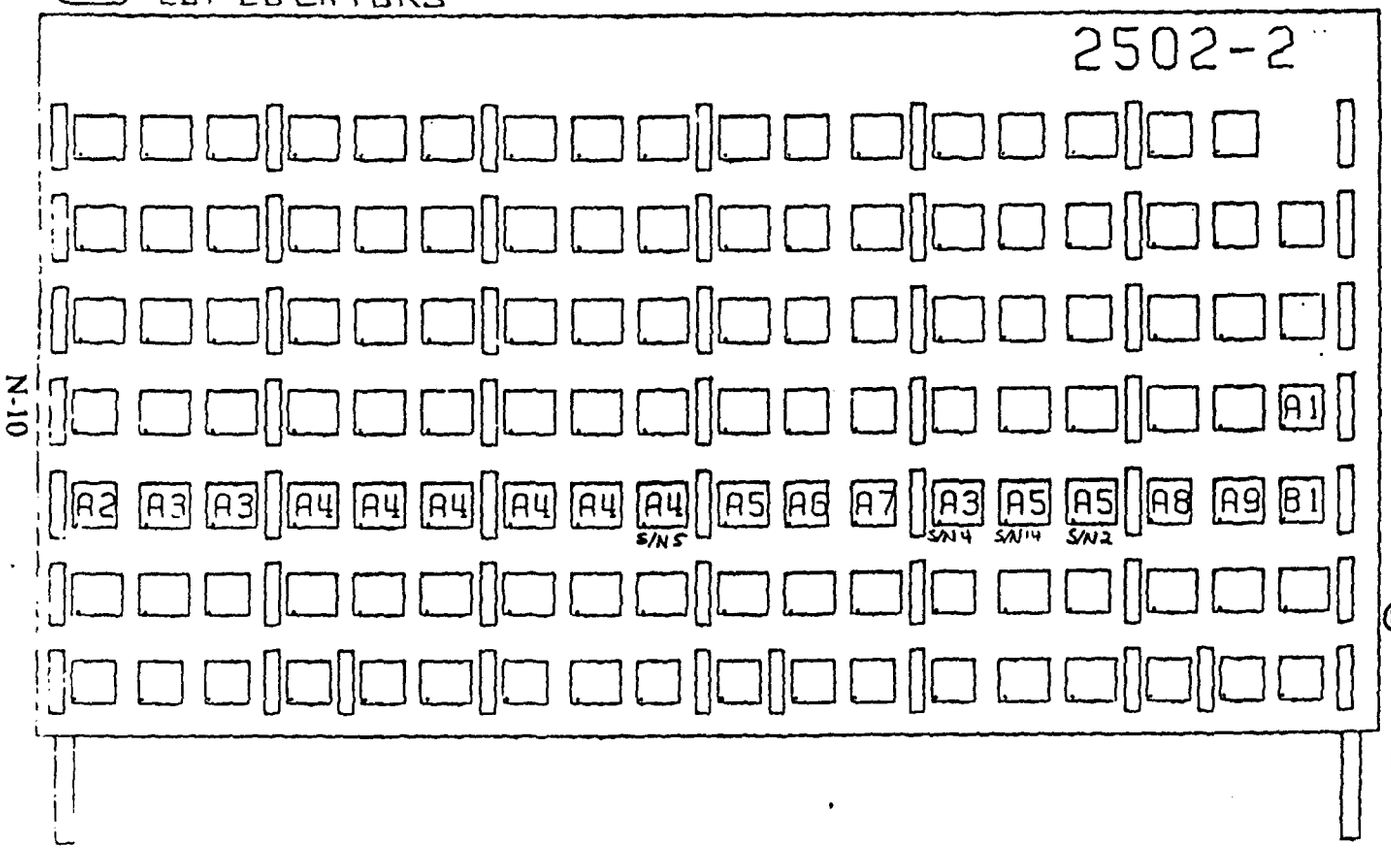
FORM 14131-50 FS

SKETCH SHEET OPER. 27

3562102-3 | 30 | 10

REFLOW SOLDER FLAT PACKS

(xx) CUP LOCATORS



⊗ INDICATES STATIC SENSITIVE

⊗ ① D6	A1	1	M38510/07005BDX U2418
⊗ ① D4	A2	1	M38510/07301BDX U2301
⊗ C9	A3	3	932728-001B U2302 U2303 (S/N4) U2313
⊗ D1	A4	6	932749-001B U2304 U2305 U2306 U2307 U2308 U2309 (S/N 5)
⑩ C7	A5	3	932753-001B U2310 U2314 (S/N 14) (S/N 2) U2315
⊗ ① D7	A6	1	M38510/08001BDX U2311
① C2	A7	1	M38510/30301BDX U2312
⑰ ⊗ ① D3	A8	1	M38510/07001BDX U2316
⑨ ⊗ C4	A9	1	932685-001B U2317
⊗ ① C1	B1	1	M38510/30001BDX U2318

SUBSTITUTE PARTS

⑰ H990582JB ① M38510/-----BAX

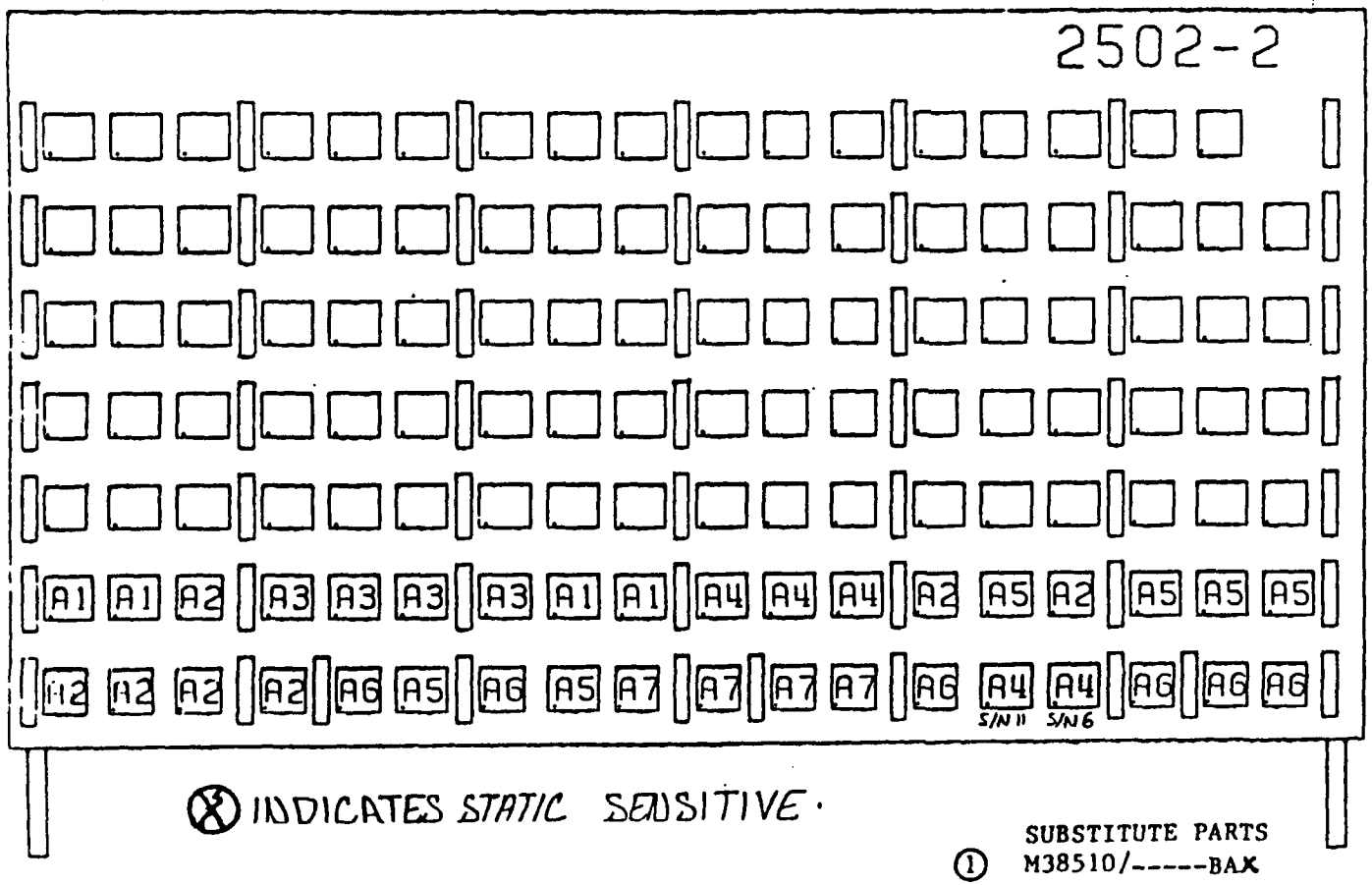
⑨ M38510/33702BFX & H990317ZB

⑩ 932753_1B

FORM 11133-5A ES

REFLOW SOLDER FLAT PACKS

(xx) CUP LOCATORS



⊗ INDICATES STATIC SENSITIVE.

SUBSTITUTE PARTS
① M38510/-----BAX
⑩ 932753-1B

⊗ C8	A1	4	932726-001B	
		U2201	U2202	
		U2208	U2209	
① ⊗ D5	A2	7	M38510/07003BDX	
		U2203	U2213	
		U2215	U2101	
		U2102	U2103	
		U2104		
⑩ C7	A3	4	H990436-001B	
		U2204	U2205	
		U2206	U2207	
⊗ C9	A4	5	932728-001B	
		U2210	U2211	
		U2212	U2114 (S/N 11)	
		(S/N 6) U2115		
⊗ B1	A5	6	932849-001B	
		U2214	U2216	
		U2217	U2218	
		U2106	U2108	
H9	A6	6	M8340103M27R0JA	
		R2105B	R2107A	
		R2113A	R2116A	
		R2117B	R2118A	
⊗ F2	A7	4	932730-002B	
		U2109	U2110	
		U2111	U2112	

REMOVE FROM HOLDING FIXTURE AND CLE
MOVE TO NEXT OPERATION ON ROUTE SHE

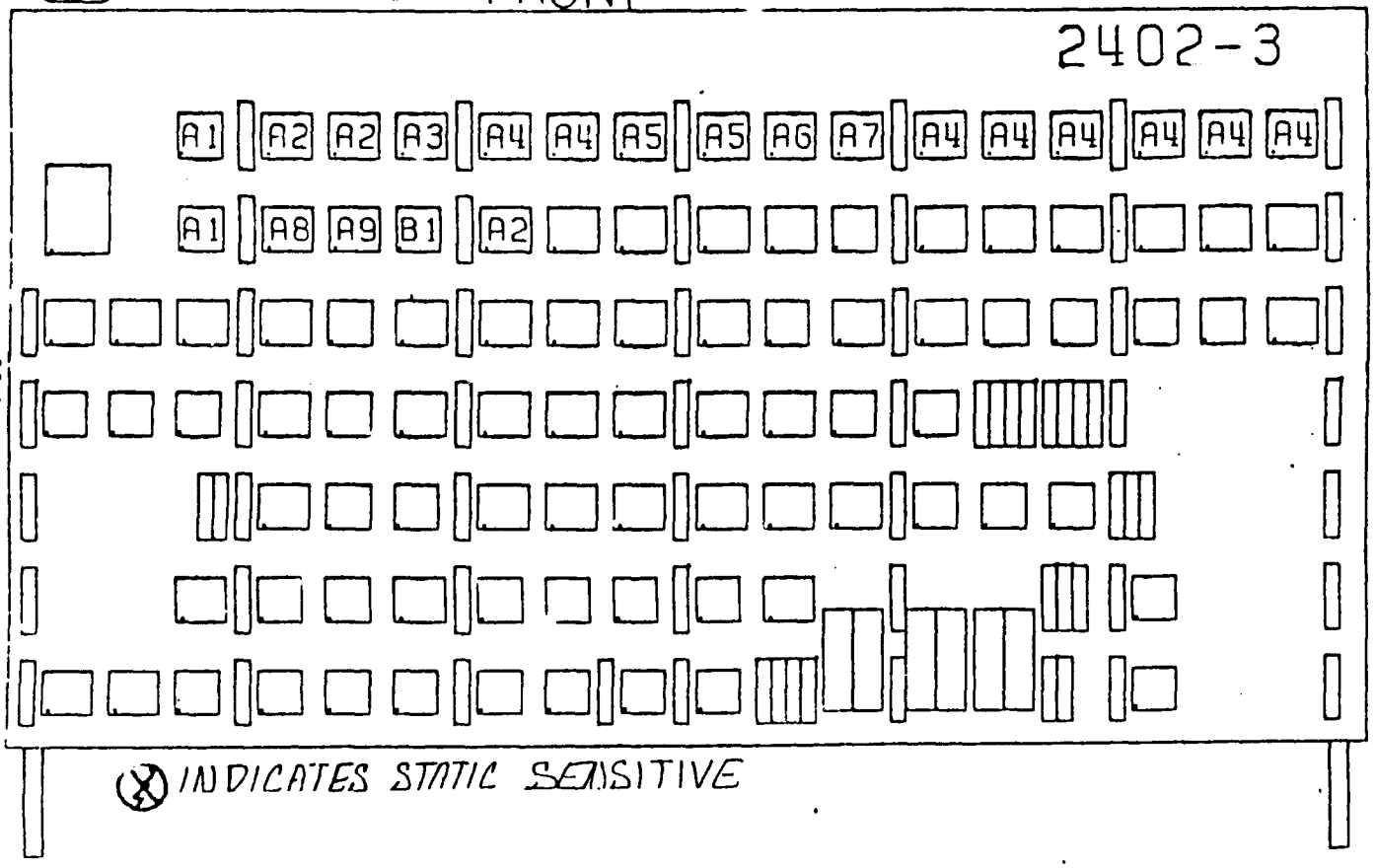
MAPS FOR HIGHER SERIAL NUMBER ERFM MODULE

SKETCH SHEET OPER. 27

5562102-3 | 50 | 4

REF PG. G1 FOR SOLDER INFO. & G4 FOR MACHINE INFO.
PLACE IN HOLDING FIXTURE FRONT SIDE UP
MACHINE REFLOW SOLDER FLATPACKS

(XX) CUP LOCATORS FRONT



⊗ INDICATES STATIC SENSITIVE

⊗	A1 F2	2	932730-002B	
		U1703	U1603	
⊗	A2 E4	3	932709-001B	
		U1704	U1705	
		U1607		
⊗	(5) A3 F1	1	932690-001B	
		U1706		
⊗	A4 B9	8	932746-001B	
		U1707	U1708	
		U1713	U1714	
		U1715	U1716	
		U1717	U1718	
⊗	(11) A5 E9	2	932732-001B	
		U1709	U1710	
⊗	A6 B3	1	932820-224	
		U1711		
⊗	(14) A7 D9	1	M38510/33701BFX	
		U1712		
⊗	(6) A8 F5	1	M38510/34102BFX	
		U1604		
⊗	A9 D8	1	M38510/07009BFX	
		U1605		
⊗	(1) B1 D7	1	M38510/08001BDX	
		U1606		

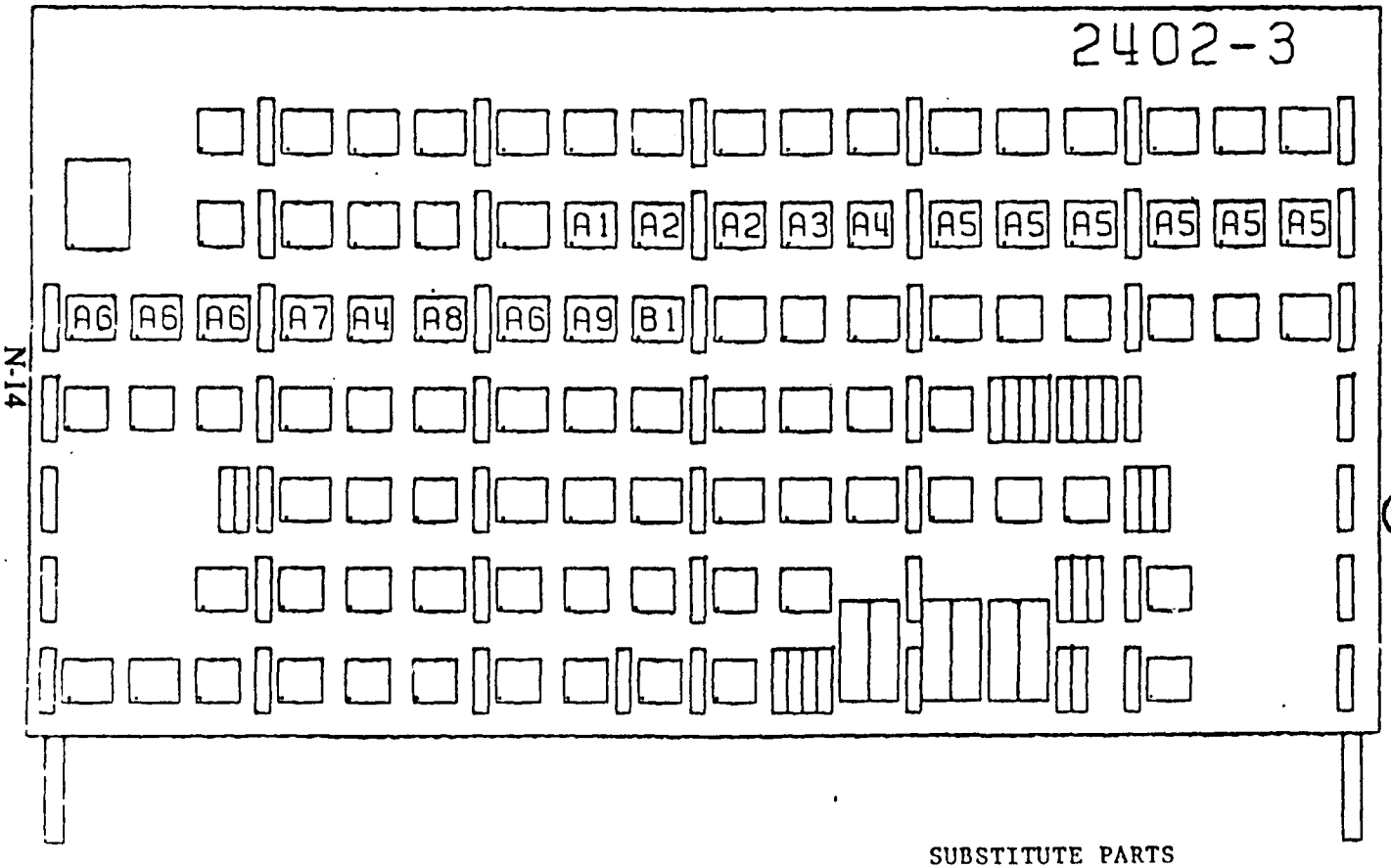
SUBSTITUTE PARTS
(1) M38510/-----BAX (11) H990316-3B
(5) M38510/07906 BFX
(6) H990307-1B OR 932711-1B
(14) 932752-1B

N-13

FORM 14133-SA ES

REFLOW SOLDER FLATPACKS

(xx) CUP LOCATORS



N-14

⊗ B9	A1	1	932746-0018
			U1608
(11) ⊗ E9	A2	2	932732-0018
			U1609 U1610
⊗ B2	A3	1	932820-215
			U1611
(1) ⊗ D5	A4	2	M38510/07003BDX
			U1612 U1505
⊗ D1	A5	6	932749-0018
			U1613 U1614
			U1615 U1616
			U1617 U1618
⊗ E4	A6	4	932709-0018
			U1501 U1502
			U1503 U1507
⊗ E5	A7	1	932614-0038
			U1504
⊗ D8	A8	1	M38510/07009BFX
			U1506
⊗ B4	A9	1	932820-217
			U1508
⊗ B6	B1	1	932820-219
			U1509

SUBSTITUTE PARTS
(1) M38510/_____ BAX

⊗ INDICATES STATIC SENSITIVE

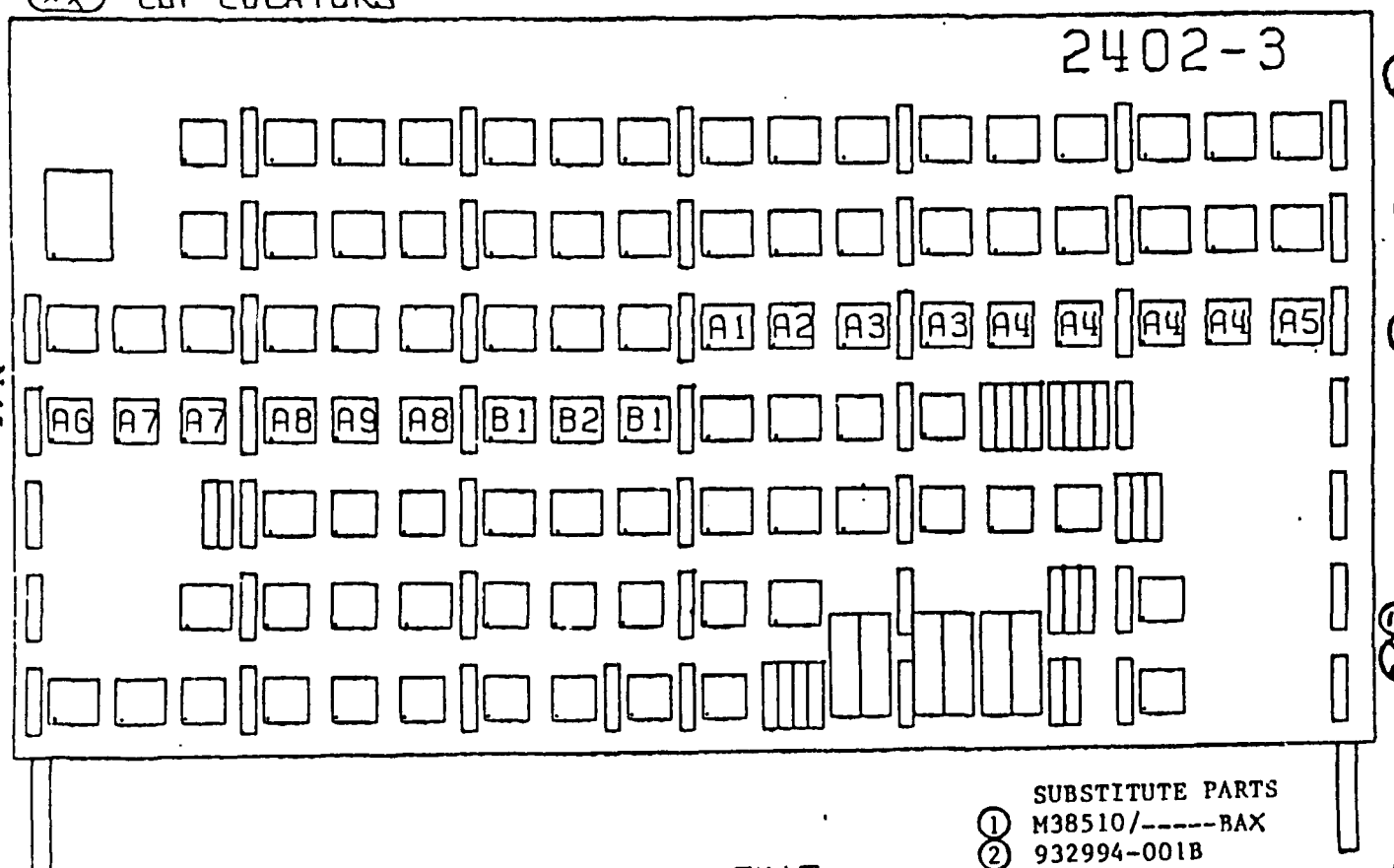
(11) H990316-1B

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO.	SHEET	REV
3562102-5	58	3

REFLOW SOLDER FLATPACKS

(XX) CUP LOCATORS



N-15

⊗ INDICATES STATIC SENSITIVE

SUBSTITUTE PARTS
① M38510/-----BAX
② 932994-001B
③ 932725-001B
⑰ H990582-10

⊗	A1 B7	1	932820-220	U1510
⊗ ②	A2 F4	1	M38510/07501BDX	U1511
⊗	A3 B9	2	932746-0018	U1512 U1513
⊗ ① ③	A4 C6	4	M38510/30605BDX	U1514 U1515 U1516 U1517
⊗	A5 D1	1	932749-0018	U1518
⊗ ①	A6 E8	1	M38510/07006BDX	U1401
⊗ ①	A7 F3	2	M38510/07401BDX	U1402 U1403
	A8 E5	2	932614-003B	U1404 U1406
⊗ ⑰ ①	A9 D3	1	M38510/07001BDX	U1405
⊗	B1 E7	2	932727-0018	U1407 U1409
⊗	B2 B5	1	932820-218	U1408

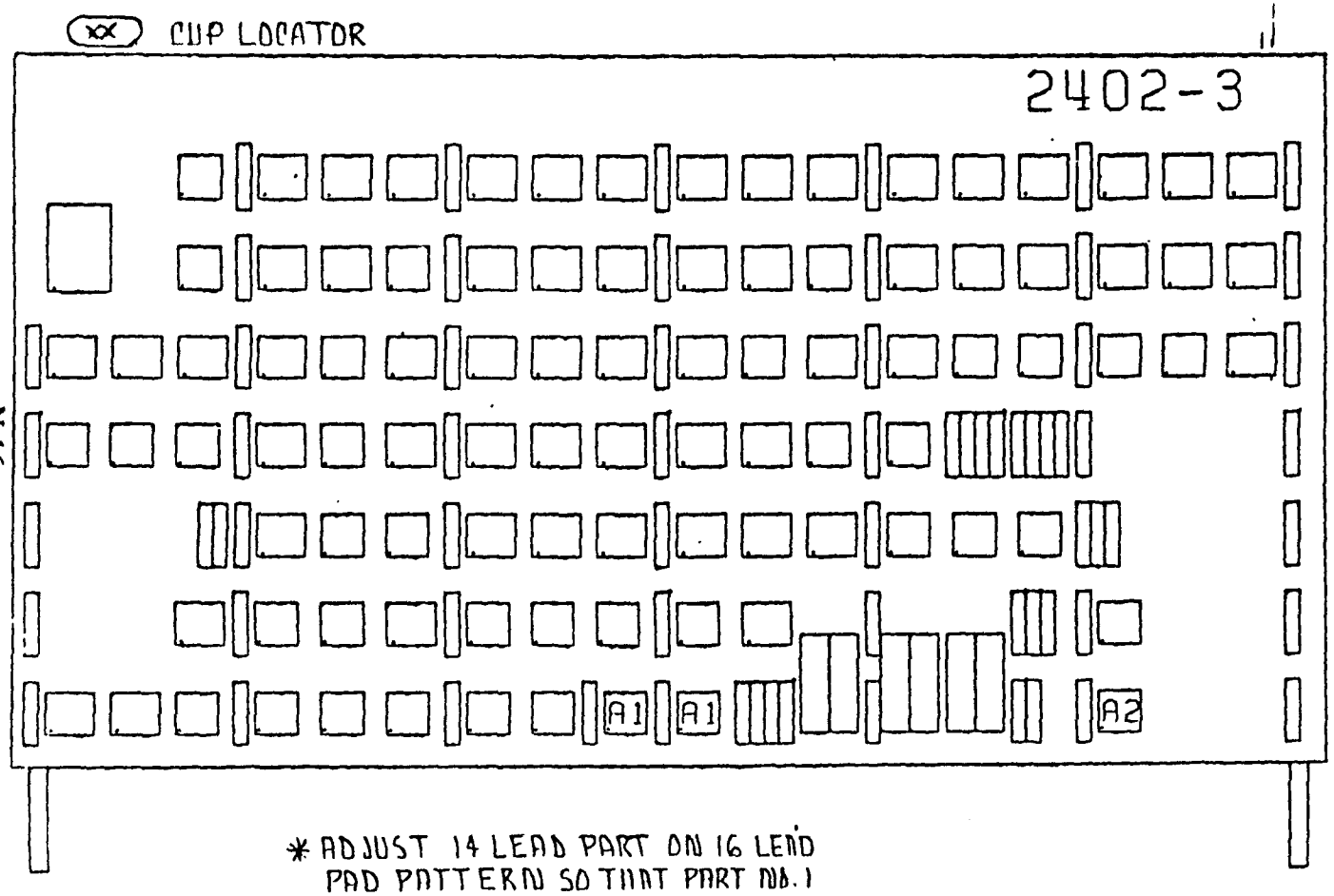
ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO.	REV.	
3562102-5	5.8	6

⊗ A1 2 . 932730-002B
F2 U1109 U1110

A2 1 M8340103M27R0JA
H9 *R1116A

REFLOW SOLDER FLATPACKS



* ADJUST 14 LEAD PART ON 16 LEAD PAD PATTERN SO THAT PART NO. 1 IS LOCATED ON PAD NO. 1

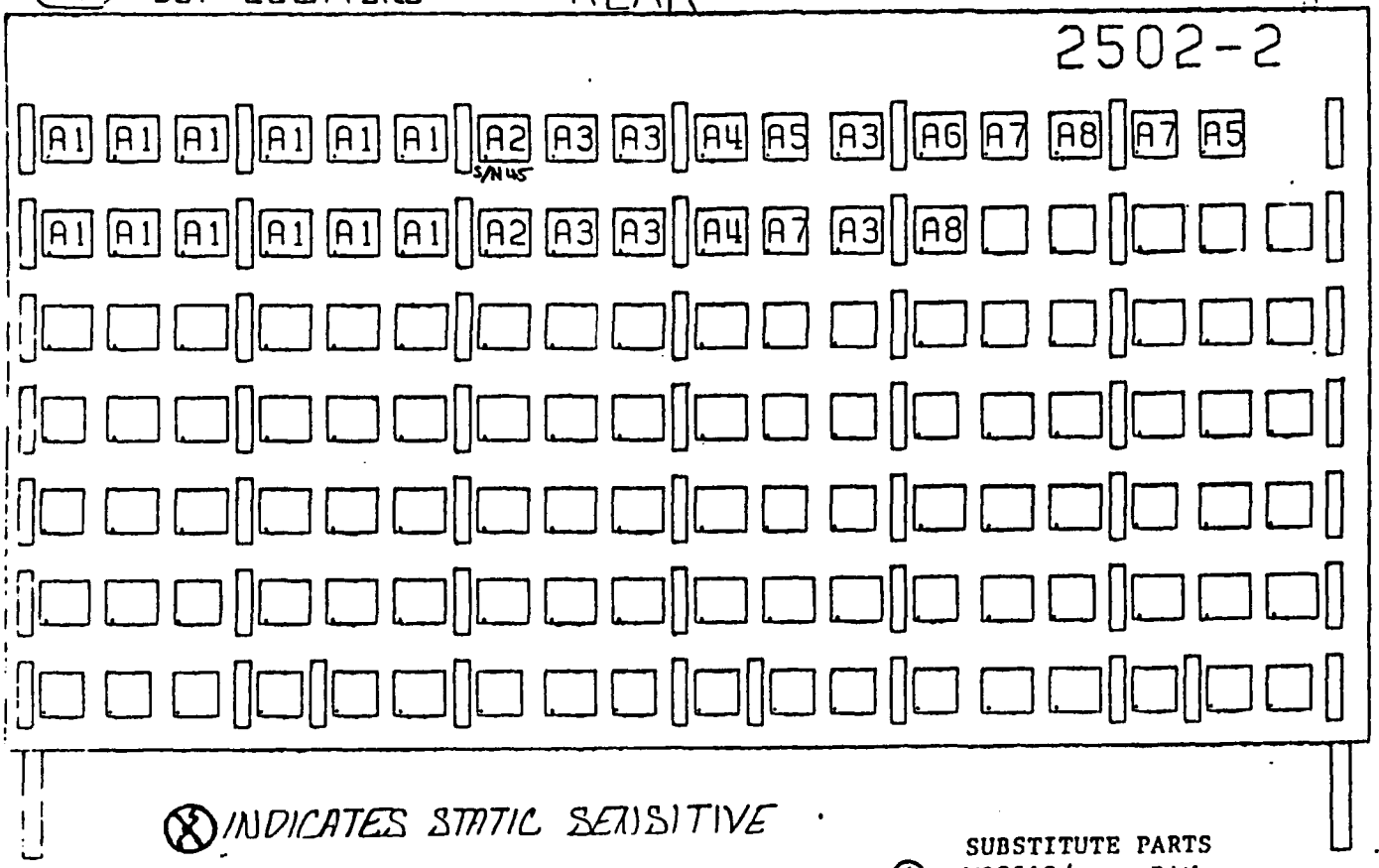
⊗ INDICATES STATIC SENSITIVE

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO.		
3562102-5	58	7

REF PG. G1 FOR SOLDER INFO. & G4 FOR MACHINE INFO.
PLACE IN HOLDING FIXTURE REAR SIDE UP
MACHINE REFLOW SOLDER FLATPACKS

(XX) CUP LOCATORS REAR



⊗ INDICATES STATIC SENSITIVE

⊗	A1 E6	12	932736-001B	
		U2701	U2702	
		U2703	U2704	
		U2705	U2706	
		U2601	U2602	
		U2603	U2604	
		U2605	U2606	
(12) ⊗	A2 E3	2	H990411-1B	
	S/N 45	U2707	U2607	
(5) ⊗	A3 F1	6	932690-001B	
		U2708	U2709	
		U2712	U2608	
		U2609	U2612	
⊗	A4 C5	2	932756-001B	
		U2710	U2610	
(1) ⊗	A5 D5	2	M38510/07003BDX	
		U2711	U2717	
⊗	A6 B9	1	932746-001B	
		U2713		
(17) (1) ⊗	A7 D3	3	M38510/07001BDX	
		U2714	U2716	
		U2611		
(6) ⊗	A8 F5	2	M38510/34102BFX	
		U2715	U2613	

SUBSTITUTE PARTS
(1) M38510/-----BAX
(5) M38510/07906BFX
(6) H990307-1B OR 932711-1B
(12) 932616-501B
(17) H990582-1B

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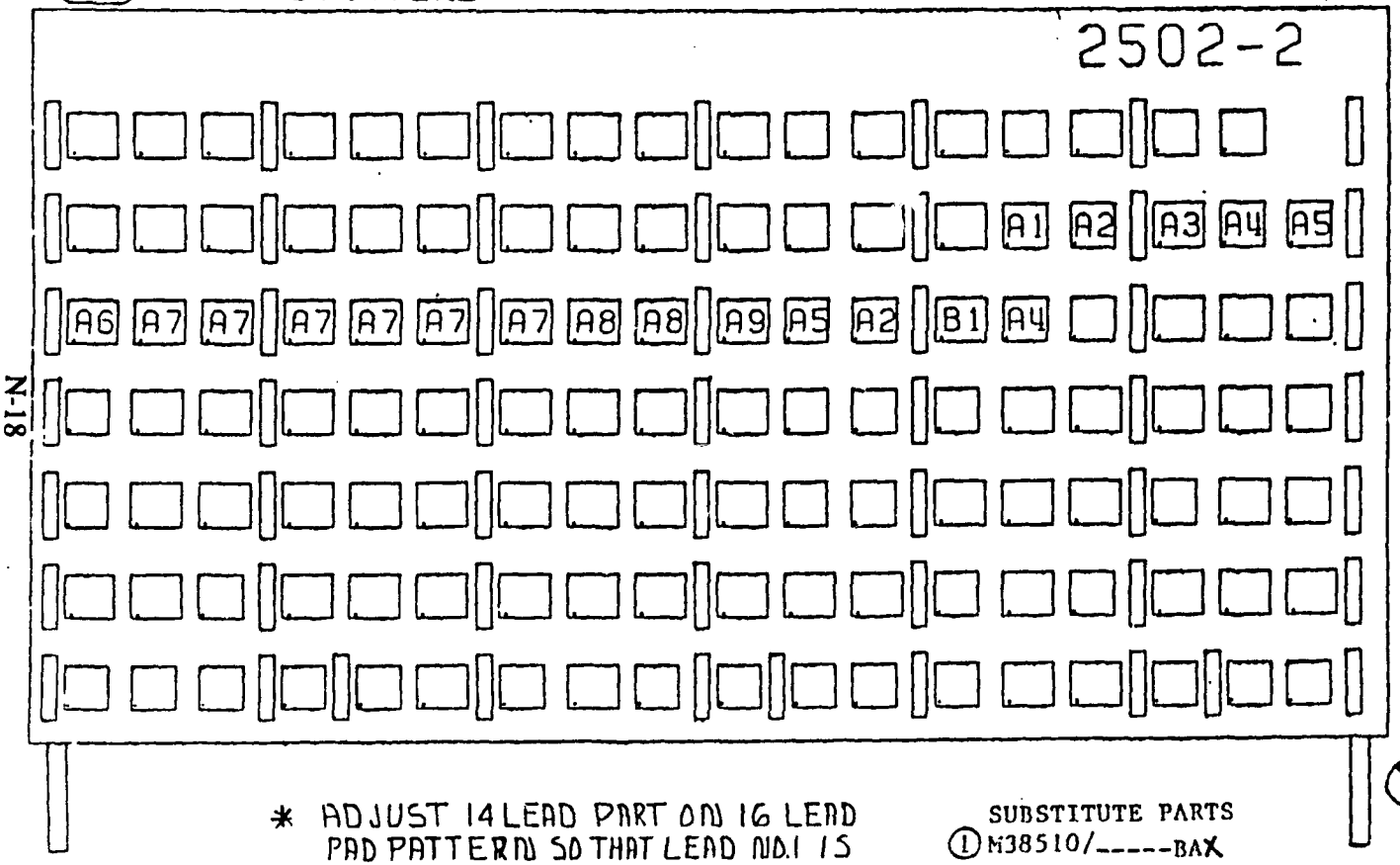
FORM 14133-SA ES

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO.		
3562102-5	58	8

REFLOW SOLDER FLATPACKS

(XX) CUP LOCATORS



N-18

① ⊗	A1 D2	1	M38510/30502BDX	U2614
① ⊗	A2 D5	2	M38510/07003BDX	U2615 U2512
⑮	A3 E2	1	M38510/33901BFX	U2616
① ⊗	A4 D7	2	M38510/08001BDX	U2617 U2514
⑰ ① ⊗	A5 D3	2	M38510/07001BDX	* U2618 U2511
⊗	A6 C9	1	932728-001B	U2501
⊗	A7 E6	6	932736-001B	U2502 U2503 U2504 U2505 U2506 U2507
⑤ ⊗	A8 F1	2	932690-001B	U2508 U2509
⊗	A9 C5	1	932756-001B	U2510
⊗	B1 E5	1	932614-003B	U2513

* ADJUST 14 LEAD PART ON 16 LEAD PAD PATTERN SO THAT LEAD NO.1 IS LOCATED ON PAD NO.1

⊗ INDICATES STATIC SENSITIVE

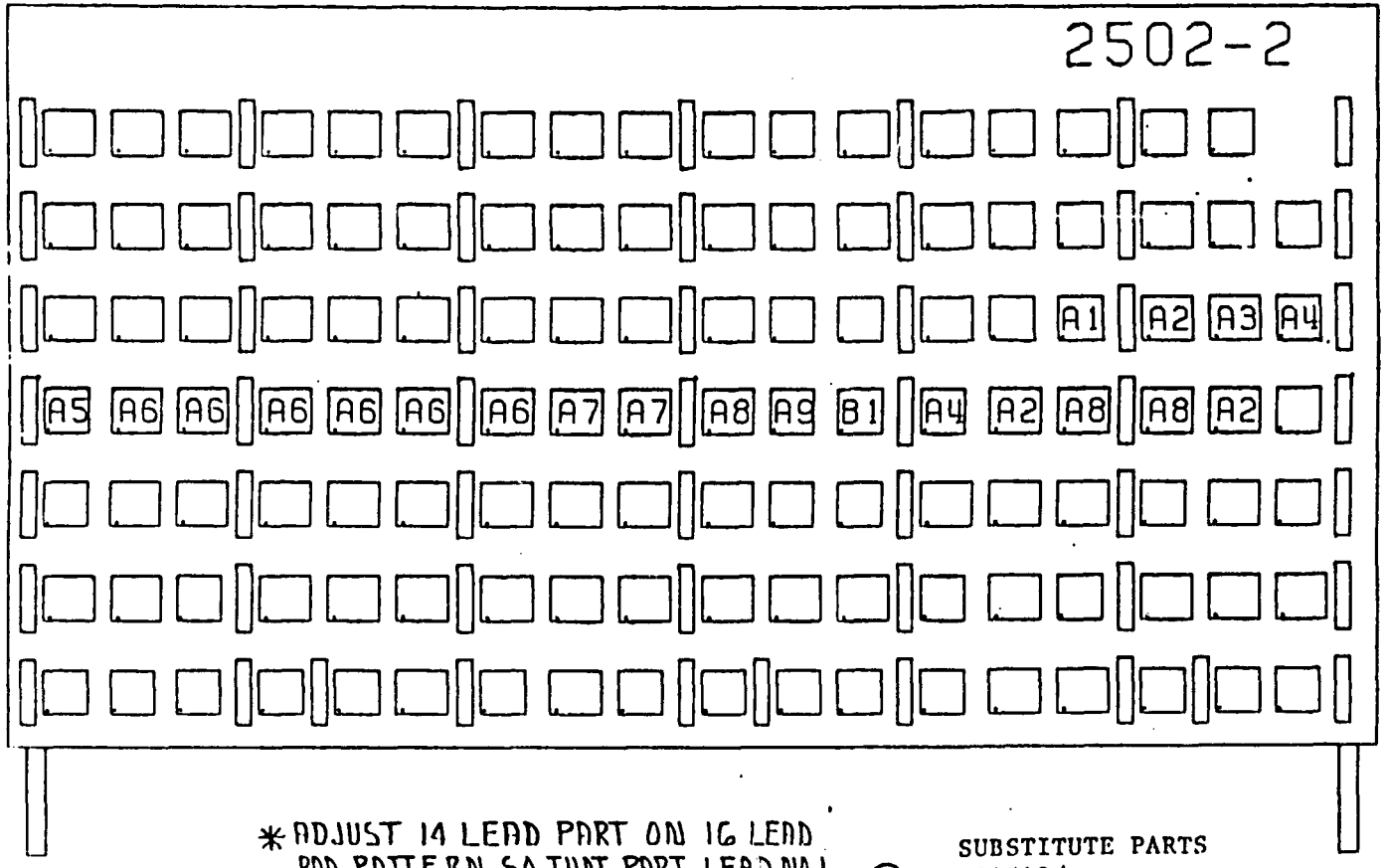
SUBSTITUTE PARTS
① M38510/_____BAX
⑤ M38510/07906BFX
⑮ 932837-1B
⑰ H9905B2-1B

FORM 14133-SA ES

ASSEMBLY NO.	REV.	PAGE
3562102-5	58	19

REFLOW SOLDER FLAT PACKS

(XX) CUP LOCATORS



N-19

① ⊗	A1 F3	1	M38510/07401BDX U2515
⊗	A2 E5	3	932614-0038 U2516 U2414 U2417
⊗	A3 E7	1	932727-0018 U2517
① ⊗	A4 D5	2	M38510/07003BDX * U2518 U2413
① ⊗	A5 D4	1	M38510/07301BDX U2401
⊗	A6 E6	6	932736-0018 U2402 U2403 U2404 U2405 U2406 U2407
⑤ ⊗	A7 F1	2	932690-0018 U2408 U2409
⊗	A8 C5	3	932756-0018 U2410 U2415 U2416
① ⊗	A9 C2	1	M38510/30301BDX U2411
⑰ ① ⊗	B1 D3	1	M38510/07001BDX U2412

* ADJUST 14 LEAD PART ON 16 LEAD PAD PATTERN SO THAT PART LEAD NO.1 IS LOCATED ON PAD NO.1.

⊗ INDICATES STATIC SENSITIVE

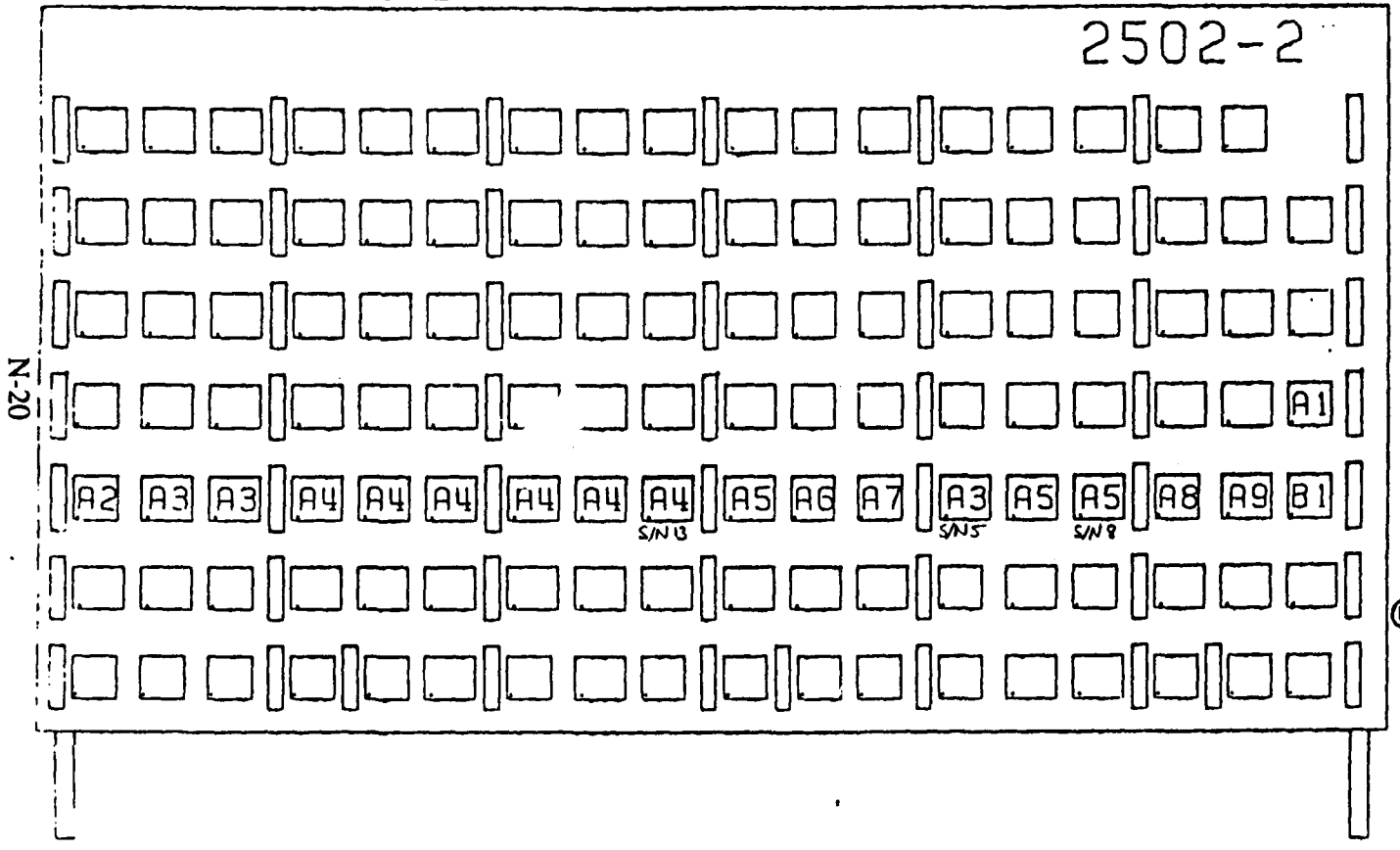
SUBSTITUTE PARTS
① M38510/-----BAX
⑤ M38510/07906BFX
⑰ A990582-1B

SKETCH SHEET OPER. 27

3562102-3 | 38 | 10

REFLOW SOLDER FLAT PACKS

(xx) CUP LOCATORS



⊗ (1)	A1 D6	1	M38510/07005BDX U2418
⊗ (1)	A2 D4	1	M38510/07301BDX U2301
⊗	A3 C9	3	932728-001B U2302 U2303 (S/N 5) U2313
⊗	A4 D1	6	932749-001B U2304 U2305 U2306 U2307 U2308 U2309 (S/N 13)
(10)	A5 C7	3	932753-001B U2310 U2314 (S/N 8) U2315
⊗ (1)	A6 D7	1	M38510/08001BDX U2311
⊗ (1)	A7 C2	1	M38510/30301BDX U2312
(17) ⊗ (1)	A8 D3	1	M38510/07001BDX U2316
⊗ (9)	A9 C4	1	932685-001B U2317
⊗ (1)	B1 C1	1	M38510/30001BDX U2318

⊗ INDICATES STATIC SENSITIVE

SUBSTITUTE PARTS

(17) H990582_1B (1) M38510/_____BAX

(9) M38510/33702BFX & H990317_2B

(10) 932753_1B

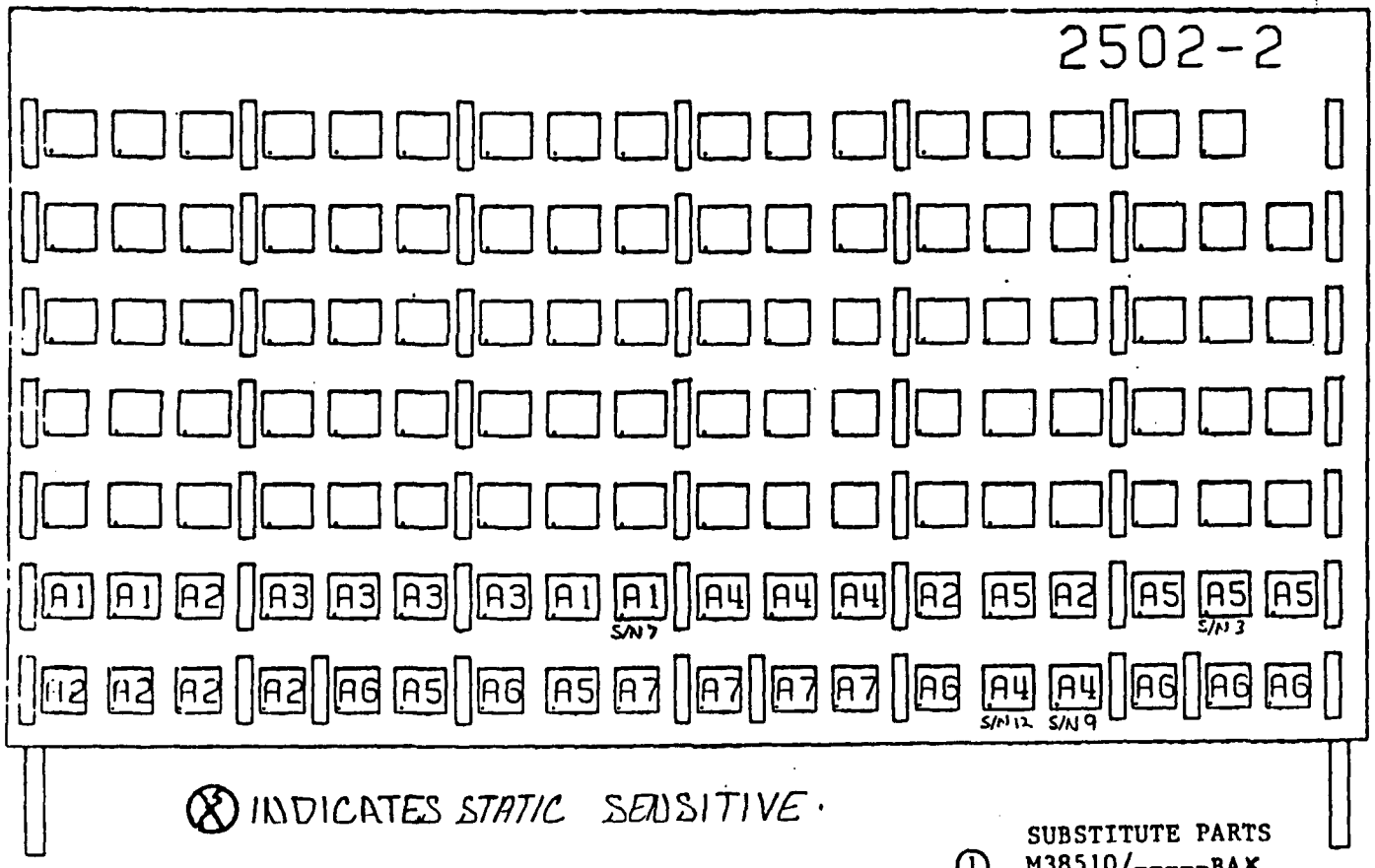
FORM 14133-SA ES

ASSEMBLY INSTRUCTIONS
SKETCH SHEET OPER. 27

ASSEMBLY NO.		
3562102-5	58	11

REFLOW SOLDER FLAT PACKS

(XX) CUP LOCATORS



⊗ INDICATES STATIC SENSITIVE.

SUBSTITUTE PARTS
① M38510/-----BAX
⑩ 932753-1B

⊗ C8	A1	4	932726-001B
		U2201	U2202
		U2208	U2209 (S/N 7)
① ⊗ D5	A2	7	M38510/07003B0X
		U2203	U2213
		U2215	U2101
		U2102	U2103
		U2104	
⑩ C7	A3	4	H9904360-001B
		U2204	U2205
		U2206	U2207
⊗ C9	A4	5	932728-001B
		U2210	U2211
		U2212	U2114 (S/N 12)
		(S/N 9) U2115	
⊗ B1	A5	6	932849-001B
		U2214	U2216
		(S/N 3) U2217	U2218
		U2106	U2108
H9	A6	6	M8340103M27R0JA
		R2105B	R2107A
		R2113A	R2116A
		R2117B	R2118A
⊗ F2	A7	4	932730-002B
		U2109	U2110
		U2111	U2112

REMOVE FROM HOLDING FIXTURE AND CLEAN
MOVE TO NEXT OPERATION ON ROUTE SHEET

N-21

APPENDIX O

HYBRID MICROCIRCUIT SPECIFICATION

STANDARD

CAUTION: THESE ITEMS ARE SUSCEPTIBLE TO DAMAGE RESULTING FROM ELECTROSTATIC DISCHARGE.

Description. This Standard includes the requirements for high power negative voltage regulator hybrid microcircuits intended for use in power supply applications.

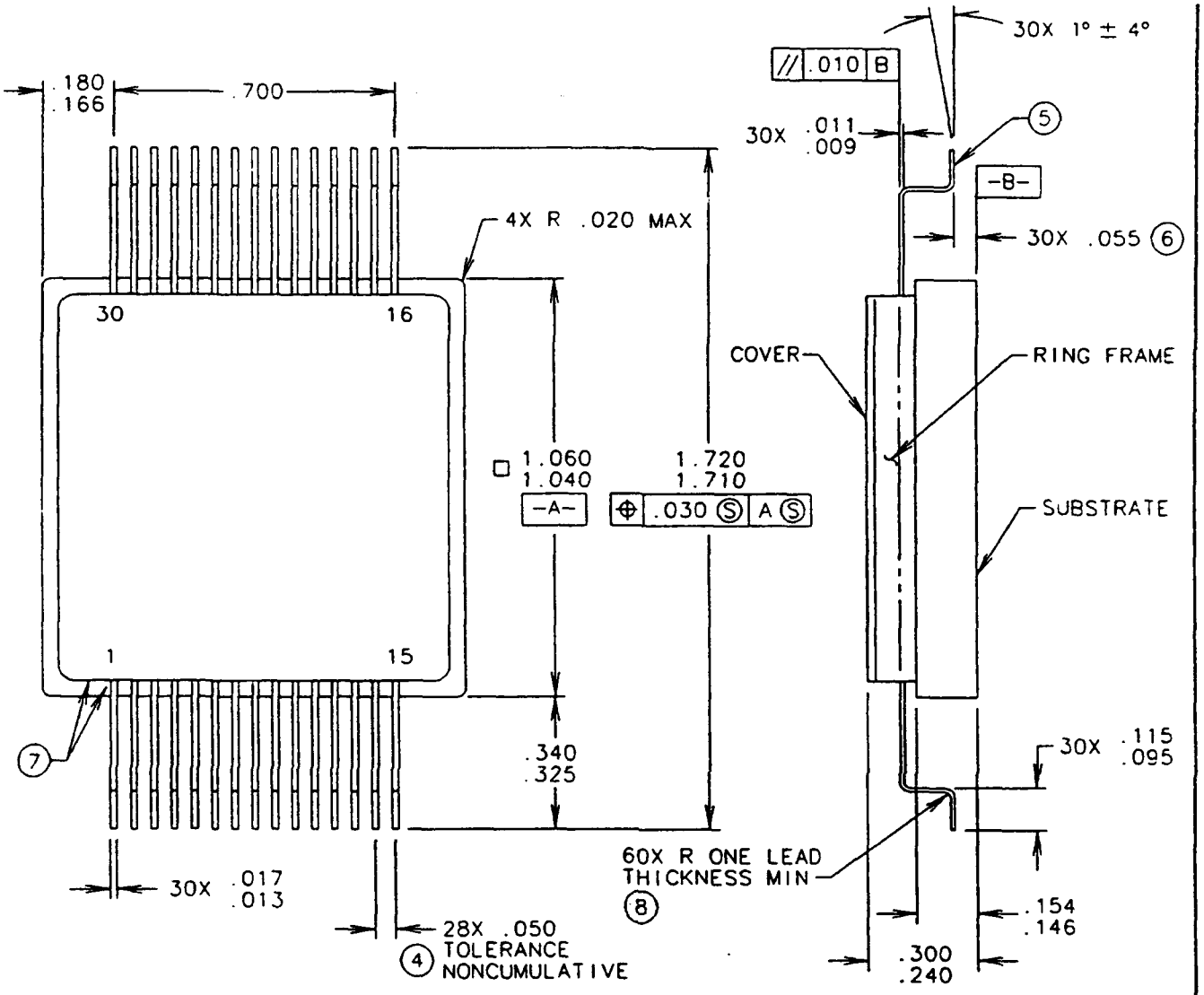
Input voltage V_I

V_O = -50 Vdc	V_I = -60 V max, -54 V min
V_O = -25 Vdc	V_I = -32.5 V max, -29.5 V min
V_O = -12 Vdc	V_I = -18.1 V max, -15.9 V min
V_O = -6 Vdc	V_I = -18.1 V max, -15.9 V min
V_O = -5 Vdc	V_I = -10.5 V max, -9.5 V min

Output current I_O

V_O = -50 Vdc	I_O = -1.1 A max
V_O = -25 Vdc	I_O = -2.7 A max
V_O = -12 Vdc	I_O = -3.8 A max
V_O = -6 Vdc	I_O = -2.2 A max
V_O = -5 Vdc	I_O = -4.4 A max

Power dissipation at T_C = +100 °C	P_d	30 W max
Junction operating temperature range	T_J	-55 to +150 °C
Storage temperature range	T_{stg}	-65 to +150 °C



1. Dimensions in inches.
2. Dimensional limits unless otherwise specified: .XXX = ±0.005.
3. Lead material shall be Kovar in accordance with ASTM F 15.

④ Dimensions to be measured to center line of leads within 0.050 external to ceramic substrate.

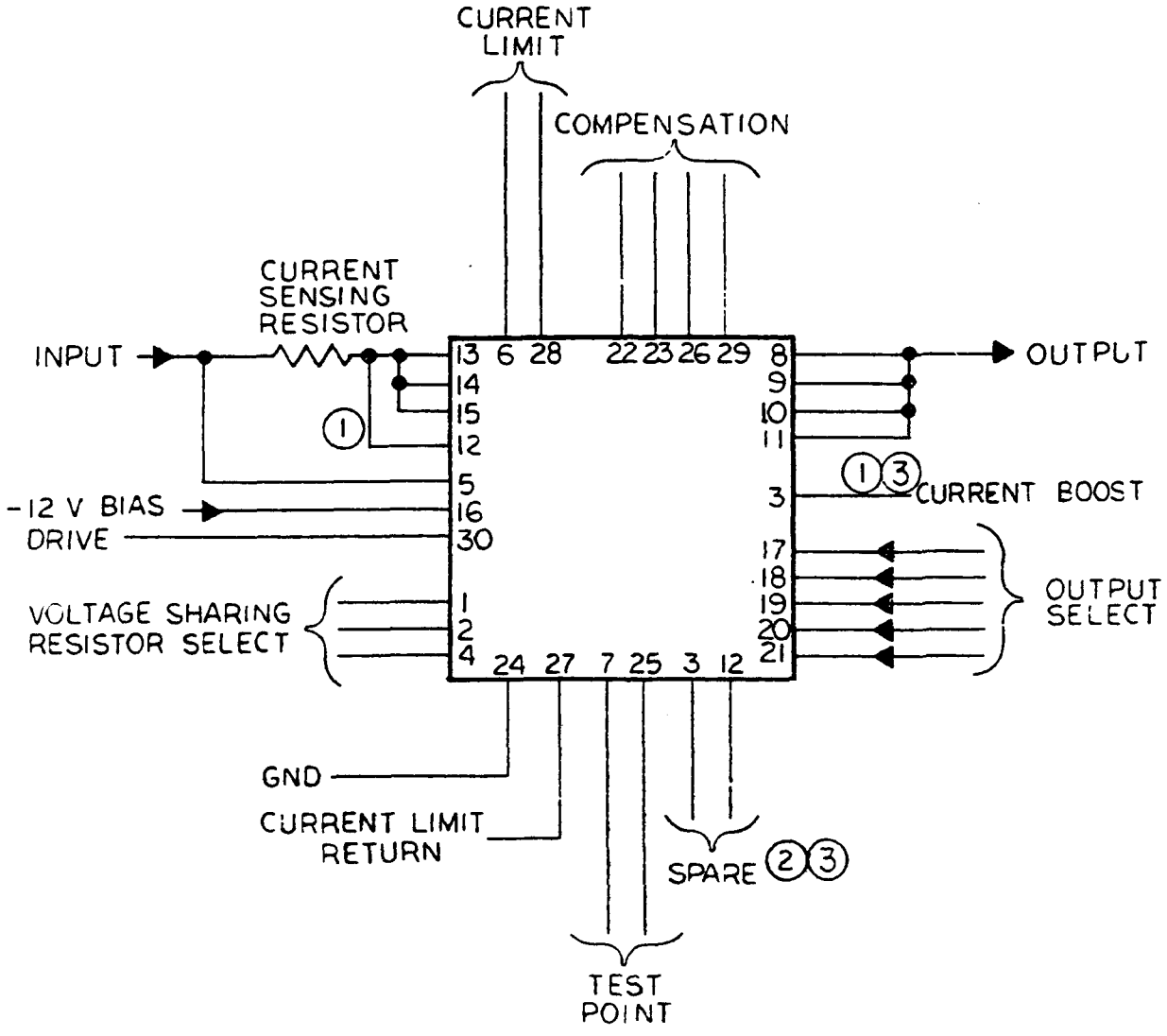
⑤ Leads shall be underplated in accordance with QQ-N-290, Class 1, 50 to 150 microinches thick, and gold plated in accordance with MIL-G-45204, Type 3, Grade A, Class 1, 50 microinches thick, minimum. Leads shall then be uniformly coated with with Sn60 or Sn63 solder 60 to 400 microinches thick (gold plating, if used, shall be removed or dissolved). Tin plate is acceptable to within 0.100 inch of glass bead, and shall cover both lead bends.

⑥ Dimension applicable with leads restrained in configuration shown. Leads shall be restrained in configuration shown for device packaging and shipping.

⑦ No. 1 lead to be identified by contrasting color bead or with 0.03 to 0.08 diameter circular dot of contrasting color placed on frame adjacent to pin 1.

⑧ Microcrazing at lead bends is acceptable (see Lead finish microcrazing requirement herein).

Figure O-1. Dimensions



(1) Pins 3 and 12 are required for dash 2B, 2C, and 502B.

(2) Pins 3 and 12 indicated as spare are applicable to dash 1B, 1C, and 501B.

(3) Pin 3 is required for dash 503B. Pin 12 must have NO internal connection for dash 503B.

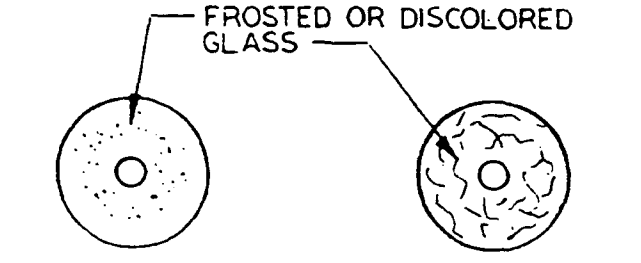
Figure O-2. Functional Diagram

Level of control. Levels of control differentiate between types and degrees of requirements and of quality assurance provisions. The levels covered in this Standard are identified by alphabetical designations corresponding to the Hughes number (dash-number) suffix letters in the Suggested Source(s) of Supply Table. Requirements in this Standard not specifically identified as applicable to a particular control level are applicable to all levels of control.

Definition of requirements. Complete requirements for the Control Level B and C items covered by this Standard are defined in this Standard and in the specification identified by the number included in the "Use with General Specification" block on page 1. The complete requirements for the dash 501 thru 600 items covered by this Standard are defined in this Standard, in the specification identified by the number included in the "Use with General Specification" block on page 1, and in Hughes Specification 932045.

Design and construction

Substrate material (inside of hybrid, except for power stage)	95 to 100 percent alumina (Al_2O_3) or beryllia or Al_2O_3 and beryllia
Semiconductors	Silicon, planar, passivated
Resistors	Thick film cermet or thin film
Capacitors	Ceramic dielectric
Enclosure type	
Bottom	Sealed, metal-to-glass (ring frame) and beryllia (external substrate material)
Cover	Gold-plated Kovar or nickel-plated Kovar. The nickel-plating thickness shall be 50 microinches (minimum).
Glass bead seals	The appearance of the glass bead seals about the package leads shall essentially be of a uniform color and texture. Areas of frosted or discolored glass arranged in a circular or donut pattern about the leads are permitted, but mottled or randomly arranged patterns of such glass are not acceptable. Examples of donut and mottled patterns are shown below.



ACCEPT REJECT

Design and construction (cont)

Lead finish delaminating	The hairline cracks that occur on the lead finish surface during lead forming shall be permitted unless they are visible at less than 3X magnification.
Dimensions	Per Figure 1 herein
Weight	60 grams maximum

Performance requirements

Mechanical shock	5 pulses at 1500 G and 0.5 ms duration in the Y_1 plane only
or	
Constant acceleration	10,000 G and 5 to 15 second duration in the Y_1 axis only

Performance requirements (continued)

TABLE O-I. CHARACTERISTICS, TEST CONDITIONS AND LIMITS

Requirement	Test Method 1/	Conditions 2/	Limits at Temperature T_C -55° C	Limits at Temperature T_C +25° C	Limits at Temperature T_C +100° C	Units
V_{O_1}		See Table IV and Figure 3	-50.50 max -49.50 min	-50.25 max -49.75 min	-50.50 max -49.50 min	V
V_{O_2}			-50.50 max -49.50 min	-50.25 max -49.75 min	-50.50 max -49.50 min	V
V_{O_3}			-50.50 max -49.50 min	-50.25 max -49.75 min	-50.50 max -49.50 min	V
V_{O_4}			-50.50 max -49.50 min	-50.25 max -49.75 min	-50.50 max -49.50 min	V
V_{O_5}			-25.25 max -24.75 min	-25.13 max -24.87 min	-25.25 max -24.75 min	V
V_{O_6}			-25.25 max -24.75 min	-25.13 max -24.87 min	-25.25 max -24.75 min	V
V_{O_7}			-25.25 max -24.75 min	-25.13 max -24.87 min	-25.25 max -24.75 min	V
V_{O_8}			-25.25 max -24.75 min	-25.13 max -24.87 min	-25.25 max -24.75 min	V
V_{O_9}			-12.12 max -11.88 min	-12.06 max -11.94 min	-12.12 max -11.88 min	V
$V_{O_{10}}$			-12.12 max -11.88 min	-12.06 max -11.94 min	-12.12 max -11.88 min	V
$V_{O_{11}}$			-12.12 max -11.88 min	-12.06 max -11.94 min	-12.12 max -11.88 min	V
$V_{O_{12}}$			-12.12 max -11.88 min	-12.06 max -11.94 min	-12.12 max -11.88 min	V
$V_{O_{13}}$			-6.06 max -5.94 min	-6.03 max -5.97 min	-6.06 max -5.94 min	V
$V_{O_{14}}$			-6.06 max -5.94 min	-6.03 max -5.97 min	-6.06 max -5.94 min	V
$V_{O_{15}}$		See Table IV and Figure 3	-6.06 max -5.94 min	-6.03 max -5.97 min	-6.06 max -5.94 min	V

See end of table for footnotes.

Performance requirements

TABLE O-I (CONTINUED)

Requirement	Test Method 1/	Conditions 2/	Limits at Temperature T_C -55° C	T_C +25° C	T_C +100° C	Units
V_{O16}		See Table IV and Figure 3	-6.06 max -5.94 min	-6.03 max -5.97 min	-6.06 max -5.94 min	V
V_{O17}			-5.05 max -4.95 min	-5.03 max -4.97 min	-5.05 max -4.95 min	V
V_{O18}			-5.05 max -4.95 min	-5.03 max -4.97 min	-5.05 max -4.95 min	V
V_{O19}			-5.05 max -4.95 min	-5.03 max -4.97 min	-5.05 max -4.95 min	V
V_{O20}			-5.05 max -4.95 min	-5.03 max -4.97 min	-5.05 max -4.95 min	V
V_{OR}		See Table IV and Figure 3	-10.10 max -9.90 min	-10.05 max -9.95 min	-10.10 max -9.90 min	V
I_{SC1}		See Table V and Figure 3	←	-0.53 max -0.10 min	→	A
I_{SC2}			←	-0.53 max -0.10 min	→	A
I_{SC3}			←	-1.0 max -0.20 min	→	A
I_{SC4}			←	-1.0 max -0.20 min	→	A
I_{SC5}			←	-1.8 max -0.3 min	→	A
I_{SC6}			←	-1.8 max -0.3 min	→	A
I_{SC7}			←	-1.5 max -0.7 min	→	A
I_{SC8}			←	-1.5 max -0.7 min	→	A
I_{SC9}			←	-3.0 max -1.5 min	→	A
I_{SC10}		See Table V and Figure 3	←	-3.0 max -1.5 min	→	A

See end of table for footnotes.

Performance requirements (continued)

TABLE O-I (Continued)

Requirement	Test Method 3/	Conditions 2/	Limits at Temperature T_C -55° C	Limits at Temperature T_C +25° C	Limits at Temperature T_C +125° C	Units
I_{OL}		See Table VI and Figure 3 herein				
I_{OL_1}		Dash 1B, 1C, 501B, 503B	←	-1.8 max -1.1 min	→	A
		Dash 2B, 2C, 502B	←	-1.8 max -1.3 min	→	A
I_{OL_2}		Dash 1B, 1C, 501B, 503B	←	-1.8 max -1.1 min	→	A
		Dash 2B, 2C, 502B	←	-1.8 max -1.3 min	→	A
I_{OL_3}		Dash 1B, 1C, 501B, 503B	←	-4.4 max -2.7 min	→	A
		Dash 2B, 2C, 502B	←	-4.3 max -2.8 min	→	A
I_{OL_4}		Dash 1B, 1C, 501B, 503B	←	-4.4 max -2.7 min	→	A
		Dash 2B, 2C, 502B	←	-4.3 max -2.8 min	→	A
I_{OL_5}		Dash 1B, 1C, 501B, 503B	←	-5.9 max -3.6 min	→	A
		Dash 2B, 2C, 502B	←	-5.8 max -3.9 min	→	A
I_{OL_6}		Dash 1B, 1C, 501B, 503B	←	-5.9 max -3.6 min	→	A
		Dash 2B, 2C, 502B	←	-5.8 max -3.9 min	→	A
I_{OL_7}		Dash 1B, 1C, 501B, 503B	←	-3.2 max -2.1 min	→	A
		Dash 2B, 2C, 502B	←	-3.2 max -2.2 min	→	A
I_{OL_8}		Dash 1B, 1C, 501B, 503B	←	-3.2 max -2.1 min	→	A
		Dash 2B, 2C, 502B	←	-3.2 max -2.2 min	→	A

See end of table for footnotes.

Performance requirements continued.

TABLE O-I (Continued)

Requirement	Test Method 1/	Conditions 2/	Limits at Temperature T_C -55° C	T_C +25° C	T_C +100° C	Units
I_{O1} (cont)		See Table VI and Figure 3 herein				
I_{O1_9}		Dash 1B, 1C, 501B, 503B	←	-6.3 max -4.1 min	→	A
		Dash 2B, 2C, 502B	←	-6.5 max -4.4 min	→	A
$I_{O1_{10}}$		Dash 1B, 1C, 501B, 503B	←	-6.3 max -4.1 min	→	A
		Dash 2B, 2C, 502B	←	-6.5 max -4.4 min	→	A
I_{O1} (extended)		Dash 1B, 1C, 501B, 503B	←	-3.0 max	→	A
		Dash 2B, 2C, 502B	←	-5.0 max -3.3 min	→	A
V_{O1}		See Table VII and Figure 3 herein		20 max		mVac p-p
V_{O2}		↕		20 max		mVac p-p
V_{O3}				20 max		mVac p-p
V_{O4}				20 max		mVac p-p
V_{O5}		See Table VII and Figure 3 herein		20 max		mVac p-p
t_{on1}		See Table VIII and Figures 3 and 4 herein	15 max	15 max		ms
t_{on2}		See Table VIII and Figures 3 and 4 herein	50 max	50 max		ms
t_{on3}		See Table VIII and Figures 3 and 4 herein	1 max	1 max		ms
t_{on4}		See Table VIII and Figures 3 and 4 herein	20 max	20 max		ms
$R_{\theta JC}$		V_{CE} = 10 V, I_C = 1 A, t = 10 Sec		1.2 max		°C/W
Current Gain		934268-504B 3/	←	5,000 min	→	...

1/ Applicable method of MIL-STD-883.

2/ In order to detect any oscillations or abnormal noise levels exceeding 20 mV_{p-p}, the output of the device shall be continuously monitored using an oscilloscope that has a minimum bandwidth of 10 MHz.

3/ Measured with collector current = 6.0 A, collector voltage = 4.0 V.

TABLE O-II. QUALITY CONFORMANCE INSPECTION

Inspection or Test	Reference 1/	LTPD Control Level B	LTPD Control Level C	Max Acc No. Control Level B	Max Acc No. Control Level C
Internal visual inspection	2017, 5/ 6/	100% Insp	100% Insp	--	--
Process conditioning	*4.5.3.1	100% Insp	100% Insp	--	--
High-temperature storage	*4.5.3.2				
Temperature cycling	1010 Cond C				
Constant acceleration or Mechanical shock	2001, Cond B (Y_1 axis only) or *4.5.2.2 and 2002 Cond B (Y_1 plane only)				
Particle impact noise test	928764				
Hermetic seal (optional)	1014.7 Cond A_1 or A_2 and C_1 or C_2, P = 30 ±2 psig for 4 hrs.	100% Insp	100% Insp	--	--
Burn-in operation	See Table III herein for conditions and limits	100% Insp	100% Insp	--	--
Electrical characteristics					
Subgroup 1 (T_C = +25 ±3 °C)	See Table I herein	100% Insp	100% Insp	--	--
V_{O_1}					
V_{O_2}					
V_{O_5}					
V_{O_9}					
$V_{O_{13}}$					
$V_{O_{19}}$					
$V_{O_{20}}$					
V_{OR}					
I_{SC_1}					
$I_{SC_{10}}$					
Θ_{T-C}					

See end of table for footnotes

TABLE O-II. (Continued)

Inspection or Test	Reference 1/	LTPD Control Level B	LTPD Control Level C	Max Acc No. Control Level B	Max Acc No. Control Level C
Electrical characteristics (cont)					
Subgroup 2 (T_C = +25 ±3 °C) I_{OL_1} $I_{OL_{10}}$ I_{OL}(extended) Dash 2B, 2C, 502B only t_{ON4}	See Table I herein	7 7/	10 7/	2	2
Subgroup 3 (T_C = +100 ±3 °C) Same inspections and tests as specified in Subgroups 1 and 2 except omit θ_{J-C}	See Table I herein	7 7/	10 7/	2	2
Subgroup 4 (T_C = -55 ±3 °C) Same inspections and tests as specified in Subgroups 1 and 2 except omit θ_{J-C} 3/	See Table I herein	7 7/	10 7/	2	2

See end of table for footnotes.

TABLE O-II. (Continued)

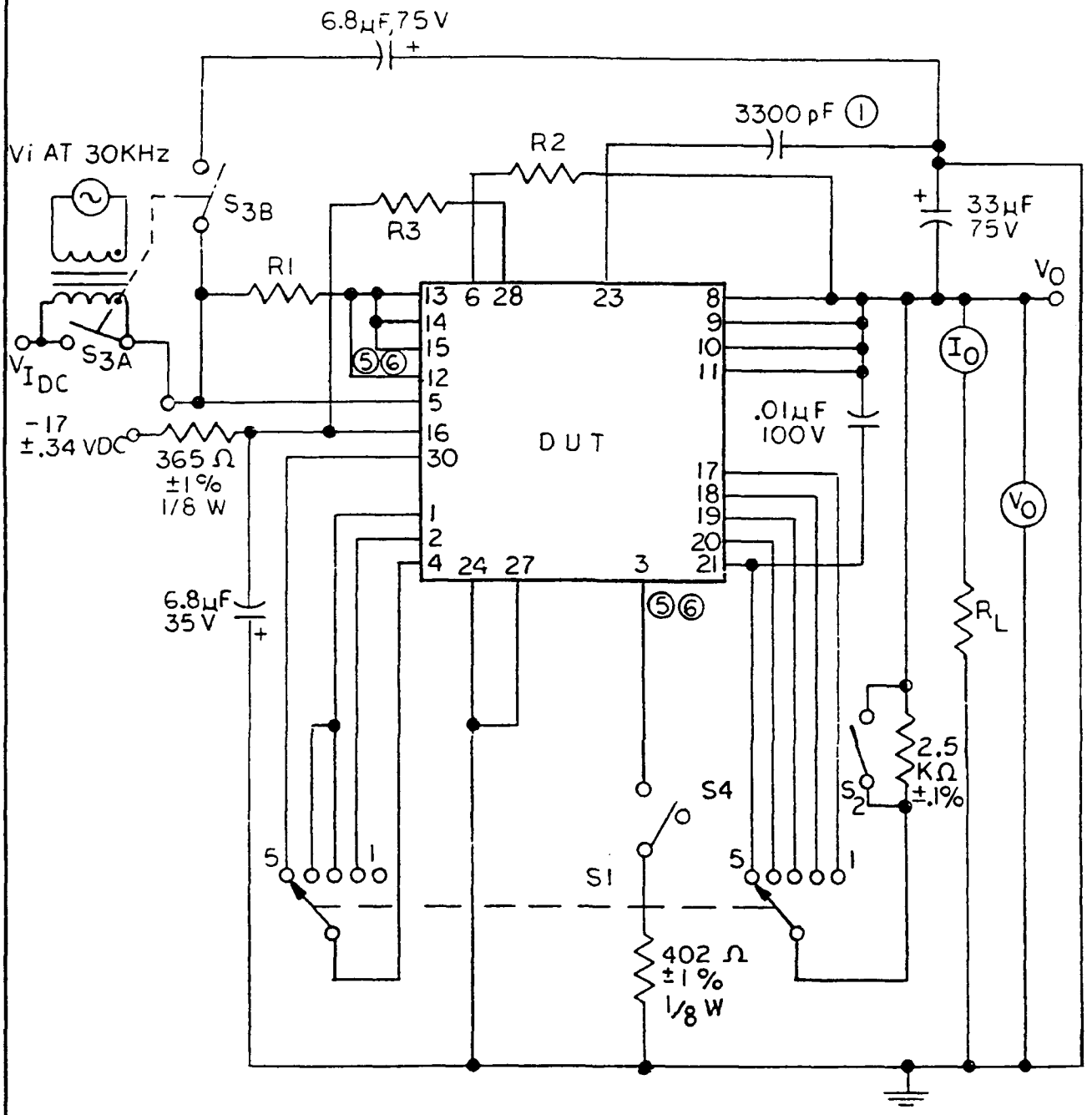
Inspection or Test	Reference 1/	LTPD Control Level B	LTPD Control Level C	Max Acc No. Control Level B	Max Acc No. Control Level C
Lead forming	See Figure 1 herein	--	--	--	--
Hermetic seal	1014.7, Condition A_1 or A_2 and C_1 or C_2, P = 30 ±2 psig for 4 hours	100% Insp	100% Insp	--	--
Lot acceptance (dash 501 thru 600 only)	4.2.2 of 932045 except hermeticity of Subgroup 4 shall be performed in accordance with Table II herein after lead forming has been performed.	2/	--	2/	--
Visual and mechanical examination 4/	2009, see design and construction for glass bead seals requirement	10	15	2	5
Inspection of preparation for delivery	*4.5.3.10	15	15	5	5

1/ Applicable method of MIL-STD-883. Numbers prefixed by an asterisk identify paragraphs in General Specification 934210.
2/ See 932045 for inspection levels.
3/ Devices shall be stabilized at -55 °C before power is applied and measurements made.
4/ At the option of the manufacturer, glass bead inspection as specified herein or 25 temperature cycles performed in accordance with MIL-STD-883, Method 1010, Condition C may be utilized to meet package integrity requirements. After the 25 temperature cycles, an hermetic seal test shall be performed in accordance with MIL-STD-883, Method 1014.7, Condition A_1 or A_2 and C_1 or C_2.
5/ 10 percent criteria does not include substrate to substrate or substrate to output pin bonds.
6/ As a minimum, the manufacturer shall meet the requirements of Method 2017.1 of MIL-STD-883 with the following modification to paragraph 3.1.3.2.7: Any metallization bridging where the separation between any two metallization paths is reduced to less than 1.0 mil, whether caused by misalignment, photographic defects, screening defects, plating defects, smears, or other causes is not acceptable.
7/ The total sample size required may be sampled from sublots produced during the 13 weeks inspection lot period. A minimum of 5 parts of each dash number from each sublot shall be tested, until the required LTPD sample size is achieved.

TABLE O-III. BURN-IN CONDITIONS AND LIMITS

Conditions	Reference 1/	Delta Limits	Percent Defective Allowable (Control Level B)
	*4.5.3.4		10%
T_C = +110 °C min to +125 °C max P_D = 20 W min See Figure 5			
Critical parameters:	See Table I herein for conditions and limits		
Test A: V_{O1}		0.15% of initial reading	
Test B: V_{O20}		Within limits specified in Table I herein	
Test C: V_{OR}		Within limits specified in Table I herein	

1/ Numbers prefixed by an esterisk identify paragraphs in General Specification 934210.



(1) This value may be increased to 3900 pF for oscillation suppression, however, in no case shall the value of the capacitor exceed 3900 pF.

2. See Tables IV thru VIII for R1, R2, R3 and R_L values.

3. S_2 closed for all tests except V_{OR}. S_{3A} and S_{3B} closed for all tests except V_{O1}, V_{O2}, V_{O3}, V_{O4} and V_{O5}.

4. S4 closed for I_{OL} (extended) dash 2B, 2C, 502B only

5. Pins 3 and 12 are required for dash 2B, 2C, 502B.

(6) Pin 3 is required for dash 503B. Pin 12 must have NO internal connection for dash 503B.

Figure O-3. Test Circuit

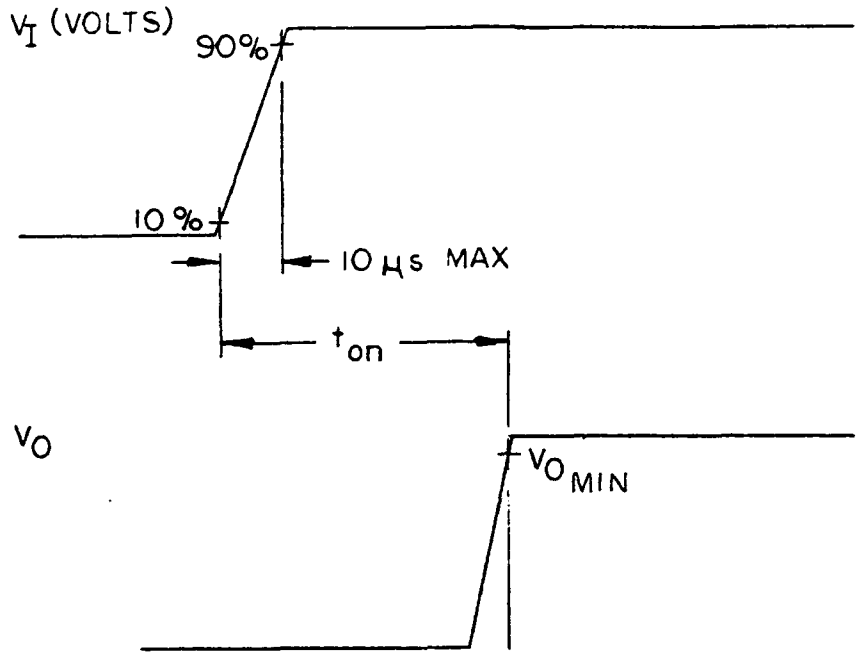
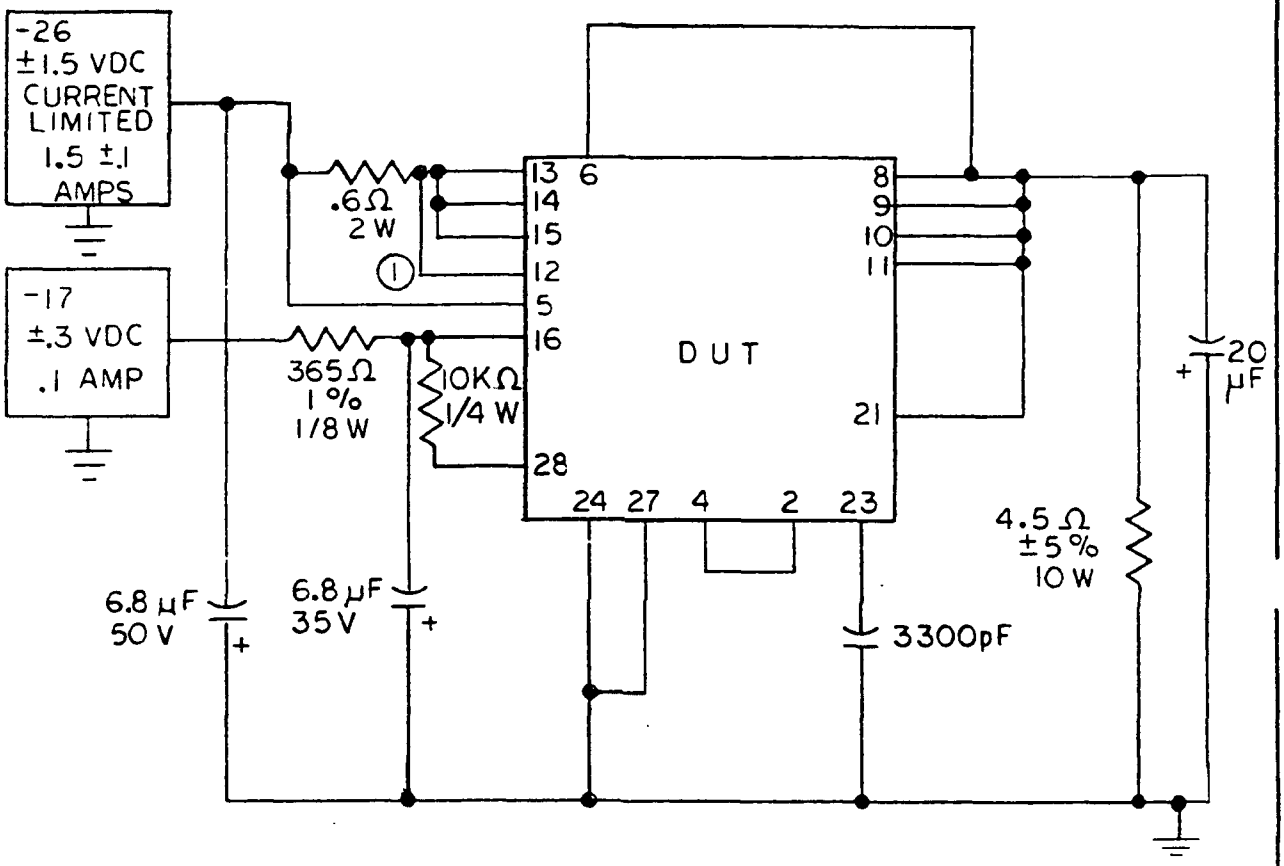


Figure O-4. Waveforms for Turn-On Time



(1) Pin 12 connection required for the Dash 2B, 2C, 502B. Pin 12 must have NO connection for dash 503B.

Figure O-5. Burn-In Test Circuit

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TABLE O-IV. TEST CONDITIONS AND PIN CONNECTIONS FOR V_O

Test	V_I	I_O	R_1 Current Sensing (Ohms, ±1%)	R_2 Current Limiting (Ohms, ±1%)	R_3 Current Limiting Bias (Ohms, ±5%)	Pin 4 Connected to	Pin 8 Connected to
V_{O_1}	-60 V	0	0.68	20.0 K	24 K	Open	Pin 17
V_{O_2}	-60 V	-1.0 A	0.68	20.0 K	24 K	Open	Pin 17
V_{O_3}	-54 V	0	0.68	20.0 K	24 K	Open	Pin 17
V_{O_4}	-54 V	-1.0 A	0.68	20.0 K	24 K	Open	Pin 17
V_{O_5}	-32.5 V	0	0.270	9.09 K	30 K	Pin 2	Pin 18
V_{O_6}	-32.5 V	-2.5 A	0.270	9.09 K	30 K	Pin 2	Pin 18
V_{O_7}	-29.5 V	0	0.270	9.09 K	30 K	Pin 2	Pin 18
V_{O_8}	-29.5 V	-2.5 A	0.270	9.09 K	30 K	Pin 2	Pin 18
V_{O_9}	-18.1 V	0	0.20	3.32 K	18 K	Pin 1	Pin 19
$V_{O_{10}}$	-18.1 V	-3.5 A	0.20	3.32 K	18 K	↕	Pin 19
$V_{O_{11}}$	-15.9 V	0	0.20	3.32 K	18 K	↕	Pin 19
$V_{O_{12}}$	-15.9 V	-3.5 A	0.20	3.32 K	18 K	↕	Pin 19
$V_{O_{13}}$	-18.1 V	0	0.41	604	10 K	↕	Pin 20
$V_{O_{14}}$	-18.1 V	-2.0 A	0.41	604	↕	↕	Pin 20
$V_{O_{15}}$	-15.9 V	0	0.41	604	↕	↕	Pin 20
$V_{O_{16}}$	-15.9 V	-2.0 A	0.41	604	↕	Pin 1	Pin 20
$V_{O_{17}}$	-10.5 V	0	0.17	0	↕	Pin 30	Pin 21
$V_{O_{18}}$	-10.5 V	-4.0 A	0.17	0	↕	Pin 30	Pin 21
$V_{O_{19}}$	-9.5 V	0	0.17	0	↕	Pin 30	Pin 21
$V_{O_{20}}$	-9.5 V	-4.0 A	0.17	0	10 K	Pin 30	Pin 21
V_{OR}	-18.1 V	0	0.20	3.32 K	18 K	Pin 1	Pin 21 thru a 2.5 kΩ ±0.1% resistor

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CODE IDENT NO. 82577

TABLE O-V. TEST CONDITIONS AND PIN CONNECTIONS FOR I_{SC}

Test	V_I	R_L	R_1 Current Sensing (Ohms, ±1%)	R_2 Current Limiting (Ohms, ±1%)	R_3 Current Limiting Bias (Ohms, ±5%)	Pin 4 Connected to	Pin 8 Connected to
I_{SC_1}	-60 V	0	0.68	20.0 K	24 K	Open	Pin 17
I_{SC_2}	-54 V		0.68	20.0 K	24 K	Open	Pin 17
I_{SC_3}	-32.5 V		0.270	9.09 K	30 K	Pin 2	Pin 18
I_{SC_4}	-29.5 V		0.270	9.09 K	30 K	Pin 2	Pin 18
I_{SC_5}	-18.1 V		0.20	3.32 K	18 K	Pin 1	Pin 19
I_{SC_6}	-15.9 V		0.20	3.32 K	18 K	Pin 1	Pin 19
I_{SC_7}	-18.1 V		0.41	604	10 K	Pin 1	Pin 20
I_{SC_8}	-15.9 V		0.41	604	10 K	Pin 1	Pin 20
I_{SC_9}	-10.5 V		0.17	0	10 K	Pin 30	Pin 21
$I_{SC_{10}}$	- 9.5 V	0	0.17	0	10 K	Pin 30	Pin 21

TABLE O-VI. TEST CONDITIONS AND PIN CONNECTIONS FOR I_{OL}

Test 1/	V_I	V_O 1/	R_1 Current Sensing (Ohms, ±1%)	R_2 Current Limiting (Ohms, ±1%)	R_3 Current Limiting Bias (Ohms, ±5%)	Pin 4 Connected to	Pin 8 Connected to
I_{OL_1}	-60 V	-49.5 V	0.68	20.0 K	24 K	Open	Pin 17
I_{OL_2}	-54 V	-49.5 V	0.68	20.0 K	24 K	Open	Pin 17
I_{OL_3}	-32.5 V	-24.75 V	0.270	9.09 K	30 K	Pin 2	Pin 18
I_{OL_4}	-29.5 V	-24.75 V	0.270	9.09 K	30 K	Pin 2	Pin 18
I_{OL_5}	-18.1 V	-11.88 V	0.20	3.32 K	18 K	Pin 1	Pin 19
I_{OL_6}	-15.9 V	-11.88 V	0.20	3.32 K	18 K	Pin 1	Pin 19
I_{OL_7}	-18.1 V	-5.94 V	0.41	604	10 K	Pin 1	Pin 20
I_{OL_8}	-15.9 V	-5.94 V	0.41	604	10 K	Pin 1	Pin 20
I_{OL_9}	-10.9 V	-4.95 V	0.17	0	10 K	Pin 30	Pin 21
$I_{OL_{10}}$	-9.5 V	-4.95 V	0.17	0	10 K	Pin 30	Pin 21
I_{OL}(extended) S_4 closed for this test only	-9.0 V	-5.94 V	0.41	604	10 K	Pin 30	Pin 20

1/ I_{OL_1} thru I_{OL}(extended) measurements shall be made by decreasing the value of the respective load resistance (R_L) to a value that will permit a maximum current reading. The maximum current reading shall not exceed the limits specified in Table I and, in addition, the output voltage (V_O) shall not fall below the value specified herein. The maximum current has been obtained when any further decrease in R_L causes V_O to be abruptly decreased to a level below the V_O specified herein.

TABLE O-VII. TEST CONDITIONS AND PIN CONNECTIONS FOR V_O

Test	V_I 1/	I_O	R_1 Current Sensing (Ohms, ±1%)	R_2 Current Limiting (Ohms, ±1%)	R_3 Current Limiting Bias (Ohms, ±5%)	Pin 4 Connected to	Pin 8 Connected to
V_{O1}	-54 Vdc +1.5 Vac pp	-1.0 A	0.68	20.0 K	24 K	Open	Pin 17
V_{O2}	-29.5 Vdc +1.1 Vac pp	-2.5 A	0.27	9.09 K	30 K	Pin 2	Pin 18
V_{O3}	-15.9 Vdc +0.7 Vac pp	-3.5 A	0.20	3.32 K	18 K	Pin 1	Pin 19
V_{O4}	-15.9 Vdc	-2.0 A	0.41	604	10 K	Pin 1	Pin 20
V_{O5}	-9.5 Vdc +0.7 Vac pp	-4.0 A	0.17	0	10 K	Pin 30	Pin 21

1/ The ac component of V_I is a 30 kHz sinusoid.

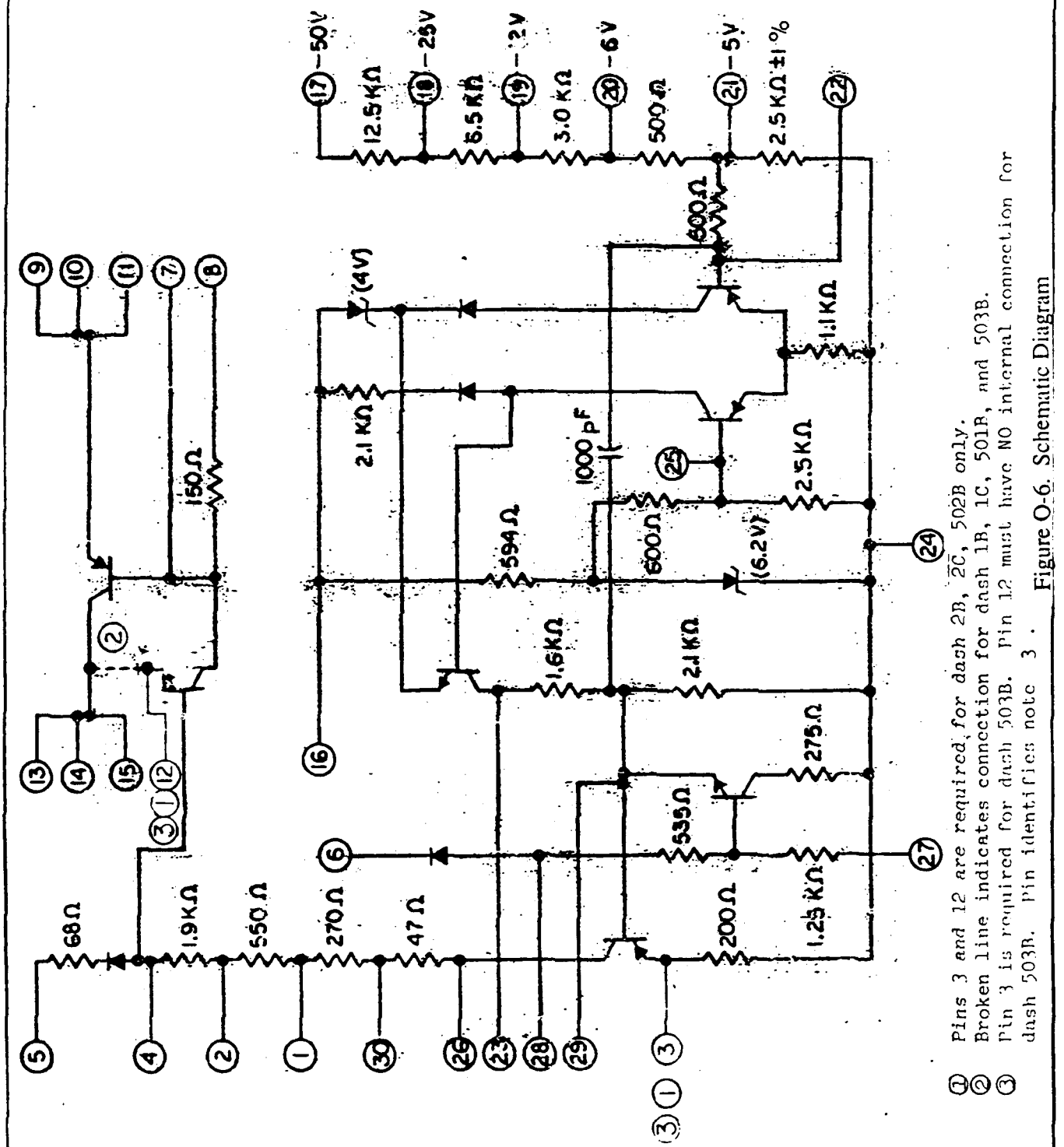
TABLE O-VIII. TEST CONDITIONS AND PIN CONNECTIONS FOR t_{on}

Test	V_I	I_O	R_1 Current Sensing (Ohms, ±1%)	R_2 Current Limiting (Ohms, ±1%)	R_3 Current Limiting Bias (Ohms, ±5%)	Pin 4 Connected to	Pin 8 Connected to	$V_{O_{min}}$
t_{on1}	-60 V	0	0.68	20.0 K	24 K	Open	Pin 17	49.75 V
t_{on2}	-54 V	-1.0 A	0.68	20.0 K	24 K	Open	Pin 17	49.75 V
t_{on3}	-9.5 V	0	0.17	0	10 K	Pin 30	Pin 21	4.97 V
t_{on4}	-9.5 V	-4.0 A	0.17	0	10 K	Pin 30	Pin 21	4.97 V

Application and design notes (for engineering information only):

1. See Figure 6 for schematic diagram.

2. 934268-504B is identical to 934268-501B except that the current gain of the complementary darlington pass-stage must be greater than 9,000.



① Pins 3 and 12 are required for dash 2B, 2C, 502B only.
② Broken line indicates connection for dash 1B, 1C, 501B, and 503B.
③ Pin 3 is required for dash 503B. Pin 12 must have NO internal connection for dash 503B. Pin identifies note 3.

Figure O-6. Schematic Diagram

PAGE		REVISION
22	934269	AH

RELEASE AND REVISION RECORD

REV	AUTHORITY	DESCRIPTION	RELEASE	
			DATE	APPROVAL
-	CMER 08166	Initial Conditional release as 934268.	--	--
A thru AG	TSER 68207-29	Records of changes are contained in the document history file.	--	--
AH	TSER 10645-35	P1: Revised Copyright notice. P11: Added Note 7/ callout 6 places. P12: Added Note 7/. P24,25: Suggested Source(s) of Supply Table, revised; removed Note 1/ callout from Teledyne.	12/19/90	A. Zahavi

RELEASE PRINT RESPONSIBLE ENGINEERING ACTIVITY		
REA ORG CODE 76-11-10		
AH REV	12/19/90 REL DATE	REL BY

Information contained on the following page identifies only the suggested source(s) of supply and the supplier's part number.

SUGGESTED SOURCE(S) OF SUPPLY

PROCUREMENT BY HUGHES AIRCRAFT COMPANY IS LIMITED TO THE MANUFACTURERS LISTED HEREIN:

HUGHES NUMBER 934268-	VENDOR ITEM NUMBER			
	ILC/DDC 1/	GML 1/ 2/	Hughes (MCD)	Hughes (TSD)
1B	Not Approved	Not Approved	1040510-3B	ESH-7001-1B
1C	Not Approved	Not Approved	1040510-3C	ESH-7001-1C
2B	Not Approved	Not Approved	1040510-4B	ESH-7001-2B
2C	Not Approved	Not Approved	1040510-4C	ESH-7001-2C
501B	CMP82100-602	1,000,036-1-2	1040510-1	ESH-7001-501B
502B	CMP82100-605	1,000,036-2	1040510-2	ESH-7001-502B
503B	Not Approved	Not Approved	1040510-5	Not Approved
504B	Not Approved	Not Approved	Not Approved	Not Approved

1/ Evaluation of the component indicated has not been completed. Procurement of indicated parts shall be limited until supplier action has been completed and shall only be approved for the F-15 and F-18 Programs.

2/ The component described by this document has been inactivated. The item is no longer procurable from this supplier.

ILC Data Device Corp., Bohemia, NY (GAGE Code 19645)
Garrett Canada, Div of Allied Signal Canada Inc., Rexdale, Ontario, Canada (GAGE Code 07217)
Hughes Aircraft Co., Microelectronic Circuits Div., Newport Beach, CA (GAGE Code 55267)
Hughes Aircraft Company, El Segundo, CA (GAGE Code 82577)
Solitron Devices, Inc., Riviera Beach, FL (GAGE Code 21845)
Teledyne Components, Dedham, MA (GAGE Code 29832)

IDENTIFICATION OF THE SUGGESTED SOURCE(S) OF SUPPLY HEREON IS NOT TO BE CONSTRUED AS A GUARANTEE OF PRESENT OR CONTINUED AVAILABILITY AS A SOURCE OF SUPPLY FOR THE ITEM(S).

SUGGESTED SOURCE(S) OF SUPPLY - (CONTINUED)

PROCUREMENT BY HUGHES AIRCRAFT COMPANY IS LIMITED TO THE MANUFACTURERS LISTED HEREIN:

HUGHES NUMBER 934268-	VENDOR ITEM NUMBER			
	Solitron	Teledyne		
1B	CJEY102	Not Approved		
1C	CJEY104	Not Approved		
2B	CJEY110	Not Approved		
2C	CJEY112	Not Approved		
501B	CJEY106	700914		
502B	CJEY108	700854		
503B	Not Approved	Not Approved		
504B	CJEY116 1/	Not Approved		

APPENDIX P

TRANSISTOR SPECIFICATION

	PROCUREMENT SPECIFICATION	PART NO. PS60071	
MICROELECTRONIC CIRCUITS DIVISION NEWPORT BEACH	2N3798 / 2N3799 CHIP PNP TRANSISTOR	FSCM NO. 55267	
		SHT 1 OF 8	REV LTR K

1.0 SCOPE

1.1 SCOPE. THIS DOCUMENT DELINEATES THE DETAIL REQUIREMENTS FOR THE ABOVE SPECIFIED HYBRID MICROCIRCUIT ELEMENTS. THESE ELEMENTS ARE INTENDED FOR USE IN CLASS B MILITARY HYBRID APPLICATIONS.

2.0 APPLICABLE DOCUMENTS

2.1 GENERAL SPECIFICATION. THIS DETAIL SPECIFICATION IS TO BE USED IN CONJUNCTION WITH THE LATEST ISSUE IN EFFECT OF GENERAL PROCUREMENT SPECIFICATION PS 60000.

3.0 REQUIREMENTS

3.1 GENERAL REQUIREMENTS. GENERAL REQUIREMENTS SHALL BE AS SPECIFIED IN GENERAL PROCUREMENT SPECIFICATION PS 60000.

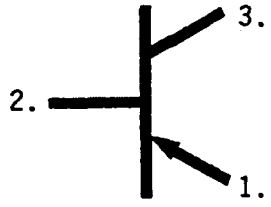
3.2 REQUIREMENT FOR APPROVED SOURCES OF SUPPLY. ELEMENTS SHALL BE FURNISHED FROM ONLY THOSE SOURCES OF SUPPLY NOTED IN THE APPENDIX A HEREIN.

NB ENGRG DOC CONT	RELEASE PRINT		
	K REV.	89/08-17 REL. DATE	EB REL. BY

INITIAL APPROVALS	DATE
PREPARED Sabrina Lay	88-08-11
CHECKED See Original	
APPROVED See Original	
AUTHORIZED BY DCN # 25037	

REV LTR	DATE	CHECKED	APPROVED	DCN
J	88-08-11			70767
K	89-08-08			73230

3.3 DETAIL FUNCTIONAL REQUIREMENTS. ELEMENT FUNCTIONAL CHARACTERISTICS SHALL BE CONSISTANT WITH THE MANUFACTURER'S PUBLISHED INFORMATION AND THE REQUIREMENTS SPECIFIED BELOW.



NOTE: THE ABOVE DIAGRAM REPRESENTS 1 DIE OF PAIR FOR "-2" and "-4".

PAD	SIGNAL
1.	EMITTER
2.	BASE
3.	COLLECTOR

3.4 DETAIL MECHANICAL REQUIREMENTS.

3.4.1 CONSTRUCTION AND MATERIALS. ELEMENTS SHALL BE CONSTRUCTED AS FOLLOWS:

SEMICONDUCTOR MATERIAL: Si

DESIGN TECHNOLOGY: Bipolar

TOP METALLIZATION: Al

BACK METALLIZATION: Au

BACK ELECTRICAL CONTACT: Cathode

3.4.2 TOPOGRAPHY AND DIMENSIONS. REQUIREMENTS APPLY TO SPECIFIC PART NUMBERS AS DEFINED IN TABLE I. BOND PAD NUMBERS ARE SHOWN IN PARENTHESIS. DIMENSIONS AND BOND PAD LOCATIONS SHALL MEET THE REQUIREMENTS OF THE APPLICABLE FIGURE. PERIMETER BOND PADS MUST BE LOCATED ENTIRELY TO THE SIDE OF THE CHIP DIAGONAL AS SHOWN AND IN THE SEQUENCE INDICATED. THOSE DESIGNATED BY AN ASTERISK MAY BE LOCATED IN THE ADJACENT CORNER. INTERIOR BOND PADS SHALL BE IN THE GENERAL AREA INDICATED.

TABLE P-I. CHIP TOPOGRAPHY

PART NO.	FIGURE
PS60071-1,-3	1
PS60071-2,-4	1 (1 OF 2 DIE)

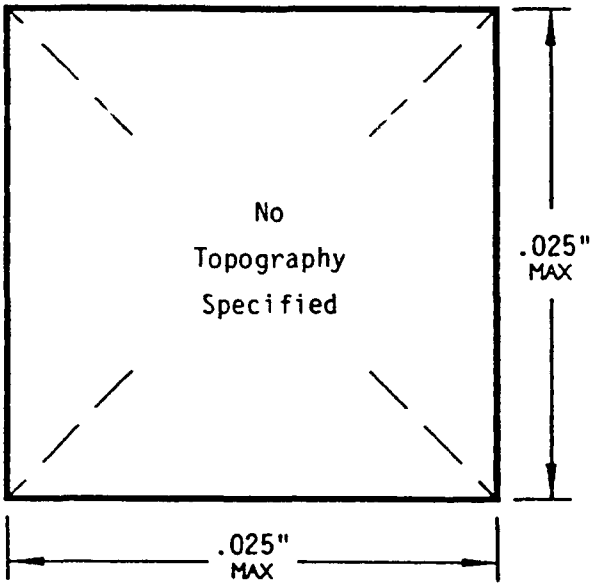


Figure P-1. Dimensions and Pad Locations

3.5 DETAIL ELECTRICAL REQUIREMENTS. ELEMENT DETAIL ELECTRICAL CHARACTERISTICS SHALL CONFORM TO THE REQUIREMENTS DEFINED IN TABLE II AND TABLE II-A FOR THE APPROPRIATE PART NUMBER.

TABLE P-II. ELECTRICAL REQUIREMENTS

PART NO.	GENERIC REFERENCE	REQUIREMENTS
PS60071-1	2N3798	STANDARD $-65°C \leq T_j \leq +200°C$ ELECTRICAL TEST PARAMETERS : TABLE IIIa
PS60071-2	2N3798 PAIR	WAFER ADJACENT PAIRS $-65°C \leq T_j \leq +200°C$ ELECTRICAL TEST PARAMETERS : TABLE IIIa
PS60071-3	2N3799	STANDARD $-65°C \leq T_j \leq +200°C$ ELECTRICAL TEST PARAMETERS : TABLE IIIb
PS60071-4	2N3799 PAIR	WAFER ADJACENT PAIRS $-65°C \leq T_j \leq +200°C$ ELECTRICAL TEST PARAMETERS : TABLE IIIb

3.5.1. HTRB. ELEMENTS SHALL BE CAPABLE OF PASSING A HIGH TEMPERATURE REVERSE BIAS (HTRB) TEST AS DEFINED HERIN. TEST CONDITIONS SHALL BE 150°C FOR 48 HOURS WITH APPLIED BIAS AND END POINT REQUIREMENTS AS DEFINED IN TABLE II-A.

TABLE P-II-A: HTRB REQUIREMENTS

PART NO.	APPLIED BIAS	END POINT REQUIREMENTS
PS60071-1 PS60071-2	$V_{CEO} = -48V$	h_{FE} AND I_{CBO} PER TABLE IIIa @ +25°C
PS60071-3 PS60071-4	$V_{CEO} = -48V$	h_{FE} AND I_{CBO} PER TABLE IIIb @ +25°C

TABLE P-IIIA. ELECTRICAL TEST PARAMETERS (PS60071-1, -2)

PARAMETER	CONDITIONS	LIMITS			UNITS
		-55°C	+25°C	+150°C	
$V_{(BR)CEO}$	I_C = 10mA, I_B = 0	--	60 Min	--	V
$V_{(BR)CBO}$	I_C = 10uA, I_E = 0	--	60 Min	--	V
$V_{(BR)EBO}$	I_E = 10uA, I_C = 0	--	5.0 Min	--	V
I_{CBO}	V_{CB} = 50V, I_E = 0	--	0.01 Max	10 Max	uA
I_{EBO}	V_{BE} = 4.0V, I_C = 0	--	20 Max	--	nA
h_{FE} 1/	I_C = 10uA, V_{CE} = 5.0V	--	100 Min	--	--
h_{FE} 1/	I_C = 500uA, V_{CE} = 5.0V	--	150 Min 450 Max	--	--
h_{FE} 1/	I_C = 10mA, V_{CE} = 5.0V	--	125 Min	--	--
$V_{CE(SAT)}$ 1/	I_C = 100uA, I_B = 10uA	--	0.2 Max	--	V
	I_C = 1.0mA, I_B = 100uA		0.25 Max		
$V_{BE(SAT)}$ 1/	I_C = 100uA, I_B = 10uA	--	0.7 Max	--	V
	I_C = 1.0mA, I_B = 100uA		0.8 Max		
$V_{BE(ON)}$	I_C = 100uA, V_{CE} = 5.0V	--	0.7 Max	--	V
f_T 2/	I_C=500uA, V_{CE}=5.0V, f=30MHZ	--	30 Min	--	MHZ
$V_{BE(1)}$-$V_{BE(2)}$ (PS60071-2)	I_C = 100uA, V_{CE} = 5V	--	±5 Max	--	mV
$h_{FE(1)}/h_{FE(2)}$ (PS60071-2)	I_C = 500uA, V_{CE} = 5V	--	0.85 Min 1.15 Max	--	--

NOTES:

1/ PULSE TEST: PULSE WIDTH ≤ 300us, DUTY CYCLE ≤ 2.0%.

2/ PARAMETER GUARANTEED BY DESIGN. NOT TESTED.

TABLE P-IIIB. ELECTRICAL TEST PARAMETERS (PS60071-3, -4)

PARAMETER	CONDITIONS	LIMITS			UNITS
		-55°C	+25°C	+150°C	
$V_{(BR)CEO}$	I_C = 10mA, I_B = 0	--	60 Min	--	V
$V_{(BR)CBO}$	I_C = 10uA, I_E = 0	--	60 Min	--	V
$V_{(BR)EBO}$	I_E = 10uA, I_C = 0	--	5.0 Min	--	V
I_{CBO}	V_{CB} = 50V, I_E = 0	--	0.01 Max	10 Max	uA
I_{EBO}	V_{BE} = 4.0V, I_C = 0	--	20 Max	--	nA
h_{FE} 1/	I_C = 10uA, V_{CE} = 5.0V	--	225 Min	--	--
h_{FE} 1/	I_C = 500uA, V_{CE} = 5.0V	--	300 Min 900 Max	--	--
h_{FE} 1/	I_C = 10mA, V_{CE} = 5.0V	--	250 Min	--	--
$V_{CE(SAT)}$ 1/	I_C = 100uA, I_B = 10uA	--	0.2 Max	--	V
	I_C = 1.0mA, I_B = 100uA		0.25 Max		
$V_{BE(SAT)}$ 1/	I_C = 100uA, I_B = 10uA	--	0.7 Max	--	V
	I_C = 1.0mA, I_B = 100uA		0.8 Max		
$V_{BE(ON)}$	I_C = 100uA, V_{CE} = 5.0V	--	0.7 Max	--	V
f_T 2/	I_C=500uA, V_{CE}=5.0V, f=30MHZ	--	30 Min	--	MHZ
$V_{BE(1)}$-$V_{BE(2)}$ (PS60071-4)	I_C = 100uA, V_{CE} = 5V	--	±5 Max	--	mV
$h_{FE(1)}/h_{FE(2)}$ (PS60071-4)	I_C = 500uA, V_{CE} = 5V	--	0.85 Min 1.15 Max	--	--

NOTES:

1/ PULSE TEST: PULSE WIDTH ≤ 300us, DUTY CYCLE ≤ 2.0%.

2/ PARAMETER GUARANTEED BY DESIGN. NOT TESTED.

4.0 QUALITY ASSURANCE PROVISIONS

4.1 ELEMENT EVALUATION. THE SUPPLIER SHALL PERFORM ELEMENT EVALUATION TESTING ON EACH LOT OF DIE PROCURED TO THIS SPECIFICATION IN ACCORDANCE WITH THE REQUIREMENTS OF PS 60000 AND TABLE IV.

TABLE P-IV. ELEMENT EVALUATION

INSPECTION / TEST	REQUIREMENT 1/	ACCEPTANCE CRITERIA
SAMPLE VISUAL		LTPD=15, C=1
SAMPLE MECHANICAL ◆ CONSTRUCTION AND MATERIALS ◆ TOPOGRAPHY AND DIMENSIONS	 3.4.1 3.4.2	LTPD=50, C=1
PACKAGED SAMPLE ELECTRICAL ◆ INTERNAL VISUAL ◆ ELECTRICAL TEST ◆ HTRB ◆ POST HTRB END POINT TESTING	 3.5 3.5.1 3.5.1	 LTPD=15, C=1
PACKAGED SAMPLE MECHANICAL ◆ BOND STRENGTH		10 WIRES 5 DIE MINIMUM 0 FAILURES

1/ REQUIREMENTS PER THE APPLICABLE PARAGRAPHS OF PS 60000 AND PARAGRAPHS OF THIS SPECIFICATION LISTED HEREIN.

5.0 PREPARATION FOR DELIVERY

ELEMENTS SHALL BE PREPARED FOR DELIVERY IN ACCORDANCE WITH THE REQUIREMENTS OF SECTION 5.0 OF PS 60000.

APPENDIX A

APPROVED SOURCES OF SUPPLY

10.1 APPROVED MANUFACTURER. ELEMENTS SHIPPED TO THIS SPECIFICATION SHALL BE PRODUCTS OF THE MANUFACTURERS LISTED BELOW WHO ARE APPROVED FOR THE APPROPRIATE PART NUMBER AS DEFINED IN TABLE A-I.

10.1.1 MOTOROLA SEMICONDUCTOR
PHOENIX, AZ 85036
(NOTE: MATERIAL NO LONGER PRODUCED BY THIS MANUFACTURER)

10.1.2 SPRAGUE SEMICONDUCTOR
CONCORD, N.H. 03301

10.1.3 TEXAS INSTRUMENTS
DALLAS, TEXAS
(NOTE: MATERIAL NO LONGER PRODUCED BY THIS MANUFACTURER.)

10.1.4

10.1.5

TABLE A-I: APPROVED SUPPLIERS

PART NO.	SUPPLIER
PS60071-1,-2	10.1.1 - 10.1.3
PS60071-3,-4	10.1.1 - 10.1.3

10.2 ALTERNATE SOURCES. A DIE PROCESSING / DISTRIBUTION FACILITY MAY BE USED AS A SOURCE OF SUPPLY FOR PRODUCT OF AN APPROVED MANUFACTURER ONLY AS DEFINED IN PS 60000.

6115140 G4

DOCUMENT CHANGE NOTICE

DCN 73230 | REV LTR —

SHEET 1 OF 1 | FSCM NUMBER 55267

PROGRAM	SYS/EQUIP NAME OR DESCRIPTION	CONTROL ITEM NAME AND NUMBER
GENERAL USAGE		PS60071

ENGINEERING DRAWINGS AND SPECIFICATIONS

NUMBER	NEW	D.V. CHG	DE-LETE	OPEN CHG	NUMBER	NEW	D.V. CHG	DE-LETE	OPEN CHG	NUMBER	NEW	D.V. CHG	DE-LETE	OPEN CHG
PS60071(REVJ)		X												

DESCRIPTION OF CHANGE

PS — SHT 3, FIG. 1, DELETE BOND PAD NUMBERS
ADD: "NO TOPOGRAPHY SPECIFIED"

SHT 4, TABLE II-A,

WAS:

PS60071-1 PS60071-2	V_{CES} = -48V	h_{FE} AND I_{CBO} PER TABLE IIIa
PS60071-3 PS60071-4	V_{CES} = -48V	h_{FE} AND I_{CBO} PER TABLE IIIb

IS:

PS60071-1 PS60071-2	V_{CEO} = -48V	h_{FE} AND I_{CBO} PER TABLE IIIa @ +25°C
PS60071-3 PS60071-4	V_{CEO} = -48V	h_{FE} AND I_{CBO} PER TABLE IIIb @ +25°C

SHT 8, ADD: TEXAS INSTRUMENTS
DALLAS, TEXAS
(NOTE: MATERIAL NO LONGER PRODUCED BY THIS MANUFACTURER)

TABLE A-I: WAS: 10.1.1-10.1.2 FOR -1,-2,-3,-4
IS: 10.1.1-10.1.3 FOR -1,-2,-3,-4

REASON FOR CHANGE PS PEVK: ADD TI AS NEW SUPPLIER. ADD TEMPERATURE REQUIREMENT.

SPECIAL INSTRUCTION

OTHER DRAWINGS AFFECTED | Yes | No X

CLASS D-I CRITERIA

AFFECTS FUNCTIONAL OR ALLOCATED CONFIGURATION IDENTIFICATION	Yes	No X	MAKES A CONTROL ITEM NON-INTERCHANGEABLE	Yes	No X	AFFECTS A CONTROL ITEM OR SYSTEM INTERFACE	Yes	No X
CAUSES A CHANGE TO TWO OR MORE CONTROL ITEMS		X	CAUSES SIGNIFICANT CHANGE IN COST		X	DELAYS DELIVERY		X

CHANGE CLASS ☒ D-II ☐ D-I

CHANGE EFFECTIVITY: 89-8-26

DISPOSITION OF ITEMS: USE

CUSTOMER APPROVAL REQUIRED: YES ☐ NO ☒

APPROVALS

PREPARED BY	DATE	ORG CODE	PRODUCT ASSURANCE	DATE	ORG CODE		DATE	ORG CODE
Sabrina Lay	89-8-1	92-86	[illegible] (MAC 0093)	[illegible] 89	92-22			
CHECKED BY	89-8-1	92-86	CRB CHAIRMAN					
RESPONSIBLE ENGINEER	89-8-1	92-86	CUSTOMER (IF REQD)			AUTH FOR RELEASE (CMO)	89 8-16	92-15
MANUFACTURING N/A						RELEASE BY	89/08-17	92-16

APPENDIX Q

DATA FROM THE HYBRID CONTAMINATION SCREEN

DATA FROM THE HYBRID CONTAMINATION SCREEN

The data in this section summarizes all of the electrical measurements performed during the hybrid contamination screen. Data is presented on the voltage outputs from the hybrids, pin-to-pin leakage currents and pin-to-pin resistances. Data is presented for both the positive voltage regulators, P/N 934266, and the negative voltage regulators, P/N 934268.

Each of the tables of voltages, leakage currents and reistances includes data columns which show the maximum and minimum values for each parameter, and the percent delta between the maximum and minimum values (the absolute delta between minimum and maximum values is shown for leakage currents).

Additional tables summarize the maximum, minimum and maximum deltas of each parameter for all the hybrids of a particular type.

The column headings correspond to the steps in the hybrid screen as follows:

Initial Build = data supplied by factory
Initial Screen = INEL
Post HTRB = HTRB
Post Bake = BAK1
Pre-Burn-in = EL2
Post Burn-in = HTFB
Step 6 = BAK2

The S/Ns of the various regulators are shown below.

Negative Regulators		Positive Regulators	
0480	7941	11650	11789
8290	8355	11836	11861
8388	8584	12034	12183
8589	8748		
8872	8929		

The next page is an index to the data.

Data and Data Summaries for Hybrid Contamination Screen

Index

SERIAL NO. 11789 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM
V01	50.001	50.030	50.04	50.040	50.036	50.034	50.035	50.040	50.030
V03		50.030	50.04	50.040	50.036	50.034	50.034	50.040	50.030
V05	25.001	25.030	25.03	25.030	25.036	25.032	25.034	25.036	25.030
V07		25.030	25.03	25.030	25.034	25.032	25.034	25.034	25.030
V09	12.002	12.020	12.02	12.024	12.024	12.024	12.033	12.033	12.020
V011		12.020	12.02	12.024	12.024	12.024	12.033	12.033	12.020
V013	5.994	6.010	6.01	6.009	6.007	6.007	6.008	6.010	6.007
V015		6.010	6.01	6.009	6.007	6.007	6.008	6.010	6.007
V017		5.010	5.01	5.013	5.024(2)	5.011	5.012	5.024	5.010
V019	4.993	5.010	5.01	5.012	5.024(2)	5.011	5.012	5.024	5.010
V0R	10.004	10.020	10.03	10.025	10.025	10.024	10.025	10.030	10.020

SERIAL NO. 11861 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM
V01	50.003	50.030	50.04	50.030	50.030	50.030	50.028	50.040	50.028
V03		50.030	50.04	50.030	50.030	50.030	50.028	50.040	50.028
V05	24.991	25.020	25.02	25.020	25.025	25.021	25.020	25.025	25.020
V07		25.020	25.02	25.020	25.025	25.021	25.020	25.025	25.020
V09	12.011	12.030	12.03	12.033	12.036	12.032	12.033	12.036	12.030
V011		12.030	12.03	12.033	12.036	12.032	12.033	12.036	12.030
V013	5.992	6.010	6.01	6.007	6.008	6.006	6.006	6.010	6.006
V015		6.010	6.01	6.007	6.008	6.006	6.006	6.010	6.006
V017		5.010	5.01	5.011	5.014	5.011	5.011	5.014	5.010
V019	4.993	5.010	5.01	5.011	5.014	5.011	5.011	5.014	5.010
V0R	9.982	10.000	10.00	9.998	10.000	9.996	9.997	10.000	9.996

SERIAL NO. 11836 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM
V01	49.999	50.030	50.04	50.040	50.042	50.035	50.032	50.042	50.030
V03		50.040	50.04	50.040	50.042	50.035	50.032	50.042	50.032
V05	24.984	25.020	25.02	25.020	25.023	25.019	25.019	25.023	25.019
V07		25.020	25.02	25.020	25.023	25.019	25.019	25.023	25.019
V09	11.994	12.020	12.02	12.019	12.021	12.019	12.020	12.021	12.019
V011		12.020	12.02	12.019	12.021	12.018	12.019	12.021	12.018
V013	5.991	6.010	6.01	6.007	6.007	6.006	6.007	6.010	6.006
V015		6.010	6.01	6.007	6.007	6.006	6.007	6.010	6.006
V017		5.010	5.01	5.012	5.011	5.011	5.013	5.013	5.010
V019	4.991	5.010	5.01	5.012	5.011	5.011	5.012	5.012	5.010
V0R	9.988	10.010	10.01	10.008	10.010	10.007	10.008	10.010	10.007

NOTES:
1. Initial Build data supplied by factory (this data not included in max/min evaluation
2. Eventhough these values are within specification limits, there is a high probability that they were recoreded incorrectly and should be 5.014. The hybrids only sat "on the shelf" for a period of time since the previous measurements of 5.013 and 5.012.

SERIAL NO. 12183 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM
V01	50.011	50.050	50.05	50.050	50.041	50.046	50.047	50.050	50.041
V03		50.050	50.05	50.050	50.041	50.046	50.047	50.050	50.041
V05	24.990	25.020	25.02	25.020	25.022	25.023	25.023	25.023	25.020
V07		25.020	25.02	25.020	25.022	25.023	25.023	25.023	25.020
V09	12.005	12.030	12.03	12.030	12.030	12.029	12.029	12.030	12.029
V011		12.030	12.03	12.030	12.030	12.029	12.029	12.030	12.029
V013	5.992	6.010	6.01	6.008	6.021	6.007	6.007	6.021	6.007
V015		6.010	6.01	6.008	6.020	6.007	6.007	6.020	6.007
V017		5.010	5.01	5.012	5.079(3)	5.012	5.011	5.079	5.010
V019	4.992	5.010	5.01	5.012	5.071(3)	5.012	5.011	5.071	5.010
V0R	9.989	10.010	10.01	10.008	10.007	10.007	10.006	10.010	10.006

3. These values are probably a recording error since the hygrids only "sat on the shelf" since the previous measurement of 5.012. Also, subsequent measurements were consistant with the 5.012 values.

SERIAL NO. 11650 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM
V01	50.008	50.040	50.04	50.040	50.045	50.038	50.038	50.045	50.038
V03		50.040	50.04	50.040	50.045	50.038	50.038	50.045	50.038
V05	25.002	25.030	25.03	25.030	25.035	25.031	25.030	25.035	25.030
V07		25.030	25.03	25.030	25.035	25.031	25.030	25.035	25.030
V09	11.998	12.020	12.02	12.020	12.022	12.019	12.019	12.022	12.019
V011		12.020	12.02	12.020	12.022	12.019	12.019	12.022	12.019
V013	5.993	6.010	6.01	6.008	6.009	6.002	6.007	6.010	6.002
V015		6.010	6.01	6.008	6.009	6.002	6.007	6.010	6.002
V017		5.020	5.01	5.012	5.013	5.011	5.011	5.020	5.010
V019	4.993	5.020	5.01	5.012	5.013	5.011	5.011	5.020	5.010
V0R	9.998	10.010	10.02	10.015	10.017	10.014	10.015	10.020	10.010

SERIAL NO. 12034 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM
V01	49.986	50.020	50.03	50.020	50.025	50.019	50.020	50.030	50.019
V03		50.020	50.03	50.020	50.025	50.019	50.020	50.030	50.019
V05	24.998	25.030	25.03	25.030	25.032	25.027	25.028	25.032	25.027
V07		25.030	25.03	25.030	25.032	25.027	25.028	25.032	25.027
V09	12.016	12.040	12.04	12.038	12.040	12.037	12.038	12.040	12.037
V011		12.040	12.04	12.038	12.040	12.037	12.038	12.040	12.037
V013	5.993	6.010	6.01	6.007	6.008	6.006	6.007	6.010	6.006
V015		6.010	6.01	6.007	6.008	6.006	6.007	6.010	6.006
V017		5.015	5.01	5.012	5.012	5.011	5.011	5.015	5.010
V019	4.993	5.015	5.01	5.012	5.012	5.011	5.011	5.015	5.010
V0R	10.003	10.020	10.02	10.020	10.021	10.018	10.019	10.021	10.018

SERIAL NO. 08355 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	49.917	50.04	50.940	50.760	50.784	50.728	50.711	50.940	50.040	1.767
V03		50.04	50.940	50.760	50.783	50.728	50.711	50.940	50.040	1.767
V05	24.959	25.05	25.420	25.330	25.346	25.321	25.312	25.420	25.050	1.456
V07		25.05	25.420	25.330	25.346	25.321	25.311	25.420	25.050	1.456
V09	11.982	11.98	12.140	12.109	12.109	12.107	12.141	12.141	11.980	1.326
V011		11.98	12.140	12.109	12.108	12.107	12.102	12.140	11.980	1.318
V013	5.998	6.00	6.018	6.019	6.013	6.017	6.016	6.019	6.000	0.316
V015		5.98	6.018	6.018	6.013	6.017	6.016	6.018	5.980	0.631
V017		4.99	4.995	4.994	4.994	4.999	4.996	4.999	4.990	0.176
V019	5.000	4.98	4.995	4.994	4.994	4.999	4.996	4.999	4.980	0.376
VOR	9.991	9.98	10.091	10.072	10.073	10.072	10.068	10.091	9.980	1.100

SERIAL NO. 00480 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	50.143	50.26	50.190	50.200	50.196	50.185	50.187	50.260	50.185	0.149
V03		50.26	50.190	50.200	50.196	50.185	50.187	50.260	50.185	0.149
V05	24.999	25.05	25.000	25.070	25.014	25.007	25.014	25.070	25.000	0.279
V07		25.05	25.000	25.070	25.013	25.007	25.014	25.070	25.000	0.279
V09	12.057	12.06	12.040	12.052	12.059	12.051	12.050	12.060	12.040	0.166
V011		12.06	12.040	12.052	12.053	12.051	12.084	12.084	12.040	0.364
V013	6.011	6.00	6.001	6.002	6.002	6.002	6.006	6.006	6.000	0.100
V015		6.00	6.001	6.002	6.002	6.002	6.006	6.006	6.000	0.100
V017		4.99	4.992	4.993	5.008	4.994	4.992	5.008	4.990	0.363
V019	5.008	4.99	4.992	4.993	5.008	4.994	4.992	5.008	4.990	0.363
VOR	9.992	9.98	9.969	9.972	9.974	9.970	9.970	9.980	9.959	0.110

SERIAL NO. 08748 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	49.676	49.720	50.490	50.410	50.422	50.410	50.394	50.490	49.720	1.525
V03		49.720	50.490	50.410	50.420	50.410	50.394	50.490	49.720	1.525
V05	24.839	24.855	25.200	25.160	25.170	25.164	25.163	25.200	24.855	1.369
V07		24.850	25.200	25.160	25.169	25.164	25.161	25.200	24.850	1.389
V09	11.980	11.970	12.090	12.082	12.095	12.088	12.083	12.095	11.970	1.033
V011		11.970	12.090	12.082	12.092	12.088	12.083	12.092	11.970	1.009
V013	5.993	5.980	5.990	6.001	6.000	6.005	6.003	6.005	5.980	0.416
V015		5.980	5.998	6.001	6.000	6.005	6.003	6.005	5.980	0.416
V017		4.980	4.983	4.986	5.001	4.993	4.990	5.001	4.980	0.416
V019	5.001	4.980	4.983	4.986	5.001	4.993	4.990	5.001	4.980	0.416
VOR	9.952	9.950	10.020	10.013	10.015	10.018	10.014	10.020	9.950	0.699

SERIAL NO. 08929 VOLTAGES

VOLTAGE	INITIAL Build(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	49.893	49.87	50.920	50.780	50.786	50.758	50.738	50.920	49.870	2.062
V03		49.87	50.920	50.780	50.785	50.758	50.738	50.920	49.870	2.062
V05	24.958	24.94	25.430	25.350	25.350	25.338	25.340	25.430	24.940	1.927
V07		24.94	25.430	25.350	25.349	25.338	25.339	25.430	24.940	1.927
V09	11.995	11.97	12.150	12.141	12.135	12.126	12.125	12.150	11.970	1.481
V011		11.97	12.150	12.141	12.135	12.126	12.125	12.150	11.970	1.481
V013	5.987	5.97	6.011	6.005	6.005	6.009	6.016	6.016	5.970	0.765
V015		5.97	6.011	6.005	6.005	6.009	6.014	6.014	5.970	0.732
V017		4.96	4.981	4.980	4.980	4.983	4.982	4.983	4.960	0.460
V019	4.985	4.96	4.981	4.980	4.980	4.983	4.982	4.983	4.960	0.460
V0R	9.976	9.95	10.076	10.058	10.059	10.058	10.056	10.076	9.950	1.250

SERIAL NO. 08589 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	50.049	50.09	50.370	50.320	50.337	50.320	50.295	50.370	50.090	0.556
V03		50.09	50.370	50.320	50.336	50.320	50.295	50.370	50.090	0.556
V05	25.020	25.02	25.160	25.140	25.136	25.132	25.126	25.160	25.020	0.556
V07		25.02	25.150	25.140	25.136	25.132	25.126	25.150	25.020	0.517
V09	12.026	12.01	12.060	12.054	12.054	12.056	12.052	12.060	12.010	0.415
V011		12.01	12.060	12.054	12.054	12.056	12.050	12.060	12.010	0.415
V013	6.012	6.00	6.005	6.006	6.009	6.009	6.007	6.009	6.000	0.155
V015		6.00	6.005	6.005	6.009	6.009	6.007	6.009	6.000	0.155
V017		4.99	4.994	4.996	4.995	4.999	4.997	4.999	4.990	0.186
V019	5.012	4.99	4.994	4.995	4.995	4.999	4.996	4.999	4.990	0.186
V0R	10.013	9.99	10.026	10.022	10.022	10.025	10.021	10.026	9.990	0.359

SERIAL NO. 08872 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	50.020	50.00	50.770	50.660	50.654	50.650	50.636	50.770	50.000	1.517
V03		50.00	50.770	50.660	50.653	50.650	50.636	50.770	50.000	1.517
V05	25.020	25.00	25.340	25.300	25.292	25.294	25.287	25.340	25.000	1.342
V07		25.00	25.340	25.300	25.292	25.294	25.286	25.340	25.000	1.342
V09	12.021	12.00	12.126	12.110	12.110	12.112	12.128	12.128	12.000	1.055
V011		12.00	12.125	12.110	12.110	12.112	12.128	12.128	12.000	1.055
V013	6.012	6.00	6.020	6.019	6.020	6.024	6.021	6.024	6.000	0.390
V015		6.00	6.019	6.019	6.020	6.024	6.021	6.024	6.000	0.390
V017		4.99	4.995	4.996	5.030 (4)	5.001	4.999	5.030	4.990	0.793
V019	5.008	4.99	4.995	4.996	5.030 (4)	5.001	4.999	5.030	4.990	0.793
V0R	10.003	9.97	10.067	10.056	10.056	10.060	10.057	10.067	9.970	0.964

Notes: 4. Probably a mistake in data entry. Should be 5.003. No reason for large change from previous entry of 4.996

SERIAL NO. 08584 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	49.975	50.16	51.650	51.380	51.385	51.271	51.227	51.650	50.160	2.885
V03		50.15	51.650	51.380	51.387	51.271	51.227	51.650	50.150	2.904
V05	24.960	25.07	25.720	25.590	25.614	25.552	25.533	25.720	25.070	2.527
V07		25.08	25.720	25.590	25.613	25.552	25.533	25.720	25.080	2.488
V09	12.013	12.03	12.292	12.238	12.241	12.226	12.216	12.292	12.030	2.131
V011		12.03	12.291	12.238	12.240	12.226	12.216	12.291	12.030	2.124
V013	6.006	6.00	6.056	6.047	6.050	6.048	6.065	6.065	6.000	1.072
V015		6.00	6.056	6.047	6.050	6.048	6.065	6.065	6.000	1.072
V017		4.99	5.017	5.015	5.015	5.018	5.015	5.018	4.990	0.558
V019	5.010	4.99	5.017	5.015	5.014	5.018	5.015	5.018	4.990	0.558
V0R	9.998	10.00	10.185	10.154	10.154	10.145	10.139	10.185	10.000	1.816

SERIAL NO. 07941 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	49.951	50.10	50.570	50.460	50.488	50.445	50.426	50.570	50.100	0.929
V03		50.10	50.570	50.450	50.486	50.445	50.426	50.570	50.100	0.929
V05	25.017	25.07	25.280	25.230	25.245	25.228	25.218	25.280	25.070	0.831
V07		25.07	25.280	25.230	25.244	25.228	25.218	25.280	25.070	0.831
V09	12.017	12.02	12.099	12.083	12.100	12.086	12.080	12.100	12.020	0.661
V011		12.02	12.099	12.083	12.096	12.086	12.081	12.099	12.020	0.653
V013	5.999	5.99	6.003	6.004	6.003	6.005	6.006	6.006	5.990	0.266
V015		5.99	6.003	6.004	6.003	6.005	6.006	6.006	5.990	0.266
V017		4.98	4.990	4.987	4.989	4.991	4.989	4.991	4.980	0.218
V019	5.000	4.98	4.990	4.987	4.989	4.991	4.990	4.991	4.980	0.218
V0R	10.008	10.00	10.060	10.045	10.049	10.048	10.045	10.060	10.000	0.596

SERIAL NO. 08290 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	50.039	50.07	50.590	50.500	50.515	50.520	50.508	50.590	50.070	1.028
V03		50.07	50.590	50.500	50.511	50.520	50.508	50.590	50.070	1.028
V05	24.990	25.00	25.220	25.190	25.197	25.205	25.200	25.220	25.000	0.872
V07		25.00	25.220	25.190	25.196	25.205	25.200	25.220	25.000	0.872
V09	12.029	12.02	12.100	12.087	12.121	12.099	12.097	12.121	12.020	0.833
V011		12.02	12.099	12.087	12.119	12.099	12.097	12.119	12.020	0.817
V013	6.007	5.99	6.010	6.005	6.048	6.012	6.014	6.048	5.990	0.961
V015		5.99	6.009	6.005	6.046	6.013	6.014	6.046	5.990	0.933
V017		4.98	4.984	4.987	5.101	4.994	4.996	5.101	4.980	2.370
V019	5.004	4.98	4.984	4.987	5.094	4.994	4.996	5.094	4.980	2.240
V0R	9.986	10.10	10.024	10.017	10.033	10.027	10.027	10.098	10.017	0.802

SERIAL NO. 08388 VOLTAGES

VOLTAGE	INITIAL BUILD(1)	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
V01	50.066	50.21	50.740	50.610	50.627	50.631	50.593	50.740	50.210	1.045
V03		50.21	50.740	50.610	50.626	50.626	50.593	50.740	50.210	1.045
V05	25.014	25.12	25.310	25.320	25.265	25.269	25.253	25.320	25.120	0.790
V07		25.12	25.310	25.310	25.265	25.269	25.253	25.310	25.120	0.751
V09	12.014	12.02	12.108	12.094	12.098	12.099	12.100	12.108	12.020	0.727
V011		12.02	12.108	12.093	12.098	12.099	12.100	12.108	12.020	0.727
V013	5.999	5.99	6.001	6.005	6.050	6.008	6.004	6.050	5.990	0.993
V015		5.99	6.001	6.004	6.049	6.008	6.004	6.049	5.990	0.972
V017		4.98	4.983	4.985	4.985	4.992	4.989	4.992	4.980	0.242
V019	4.999	4.98	4.983	4.985	4.984	4.992	4.989	4.992	4.980	0.242
V0R	9.990	9.99	10.047	10.035	10.050	10.045	10.037	10.050	9.990	0.593

SERIAL NO. 12183 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.870	1.8781	1.8782	1.8779	1.8782	1.8781	1.8782	1.8779	0.02
2-1	540.0	544.3	544.3	544.23	544.13	544.13	544.30	544.13	0.03
1-30	265.0	267.7	267.7	267.60	267.55	267.64	267.70	267.55	0.06
30-26	46.4	47.6	47.6	47.441	47.357	47.469	47.600	47.357	0.51
7-8	149.0	148.8	148.9	148.74	148.75	148.71	148.90	148.71	0.13
28-27	1.760	1.7772	1.7772	1.7772	1.7771	1.7771	1.7772	1.7771	0.01
17-18	12.500	12.522	12.522	12.522	12.523	12.524	12.524	12.522	0.02
18-19	6.460	6.501	6.501	6.5023	6.5049	6.5023	6.5049	6.5010	0.06
19-20	3.000	3.013	3.013	3.0136	3.0135	3.0135	3.0136	3.0130	0.02
20-21	500.0	498.6	498.7	498.61	498.56	498.60	498.70	498.56	0.03
21/22	490.0	493.8	493.9	493.82	494.46	493.88	494.46	493.80	0.13
24/21	2.500	2.509	2.509	2.5092	2.5091	2.5093	2.5093	2.5090	0.01
24/23	3.600	3.652	3.653	3.6531	3.6531	3.6533	3.6533	3.6520	0.04
16/25	1.180	1.1928	1.1930	1.1928	1.1924	1.1927	1.1930	1.1924	0.05
3/24	200.0	199.9	199.9	199.77	199.72	199.77	199.90	199.72	0.09

SERIAL NO. 11650 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.875	1.8779	1.8780	1.8778	1.8876	1.8777	1.8876	1.8777	0.52
2-1	540.0	546.8	546.8	546.69	546.68	546.73	546.80	540.00	1.24 (5)
1-30	268.8	270.6	270.8	270.53	270.64	270.56	270.80	268.80	0.74
30-26	47.0	47.6	47.7	47.441	47.361	47.460	47.700	47.000	1.47 (5)
7-8	150.0	148.9	149.0	148.78	149.82	148.78	149.82	148.78	0.69
28-27	1.750	1.7731	1.7732	1.7729	1.7735	1.7728	1.7735	1.7500	1.33 (5)
17-18	12.400	12.494	12.494	12.494	12.494	12.495	12.495	12.400	0.76
18-19	6.457	6.499	6.500	6.5002	6.5000	6.5002	6.5002	6.4570	0.66
19-20	3.000	3.003	3.003	3.0035	3.0034	3.0034	3.0035	3.0000	0.12
20-21	494.4	497.7	497.9	497.65	498.26	497.66	498.26	494.40	0.77
21/22	488.8	492.6	492.7	492.56	492.76	492.61	492.76	488.80	0.80
24/21	2.500	2.505	2.505	2.5052	2.5051	2.5053	2.5053	2.5000	0.21
24/23	3.681	3.648	3.648	3.6489	3.6485	3.6488	3.6489	3.6480	0.02
16/25	1.128	1.1893	1.1893	1.1894	1.1893	1.1893	1.1894	1.1280	5.16 (5)
3/24	198.0	199.4	199.4	199.26	199.37	199.26	199.40	198.00	0.70

nOTES: 5. Initial measurements performed using curve tracer. Resulted in large % delta. Later measurements all stable

SERIAL NO. 12034 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.860	1.8774	1.8773	1.8772	1.8772	1.8770	1.8774	1.8770	0.02
2-1	540.0	544.3	544.2	544.21	544.13	544.22	544.30	544.13	0.03
1-30	266.6	267.7	267.6	267.56	267.47	267.54	267.70	267.47	0.09
30-26	47.0	47.7	47.5	47.510	47.690	47.553	47.700	47.500	0.42
7-8	148.3	148.7	148.6	148.58	148.56	148.60	148.70	148.56	0.09
28-27	1.760	1.7824	1.7822	1.7823	1.7828	1.7822	1.7828	1.7822	0.03
17-18	12.420	12.475	12.475	12.474	12.475	12.476	12.4760	12.4740	0.02
18-19	6.442	6.483	6.483	6.4837	6.4836	6.4837	6.4837	6.4830	0.01
19-20	3.000	3.010	3.009	3.0102	3.0104	3.0102	3.0104	3.0090	0.05
20-21	494.4	497.5	497.5	497.45	497.50	497.47	497.50	497.45	0.01
21/22	491.1	495.1	495.0	494.94	495.78	495.00	495.78	494.94	0.17
24/21	2.488	2.504	2.504	2.5040	2.5042	2.5053	2.5053	2.5040	0.05
24/23	3.625	3.661	3.662	3.6619	3.6620	3.6622	3.6622	3.6610	0.03
16/25	1.187	1.1963	1.1963	1.1961	1.1960	1.1962	1.1963	1.1960	0.03
3/24	198.0	200.6	200.5	200.46	200.42	200.47	200.60	200.42	0.09

SERIAL NO. 11789 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.860	1.8772	1.8774	1.8772	1.8772	1.8771	1.8774	1.8771	0.02
2-1	543.3	544.1	544.1	544.11	544.05	544.09	544.11	544.05	0.01
1-30	265.5	267.3	267.3	267.27	267.25	267.28	267.30	267.25	0.02
30-26	47.1	47.6	47.6	47.501	47.551	47.497	47.600	47.497	0.22
7-8	147.5	148.9	148.9	148.74	148.84	148.74	148.90	148.74	0.11
28-27	1.766	1.7788	1.7788	1.7786	1.7785	1.7784	1.7788	1.7784	0.02
17-18	12.450	12.467	12.467	12.466	12.468	12.467	12.468	12.466	0.02
18-19	6.428	6.486	6.486	6.4865	6.4866	6.4861	6.4866	6.4860	0.01
19-20	2.987	2.999	3.000	2.9997	2.9996	2.9994	3.0000	2.9990	0.03
20-21	493.7	497.1	497.2	497.05	496.97	497.04	497.20	496.97	0.05
21/22	491.0	494.7	494.7	494.63	494.59	494.65	494.70	494.59	0.02
24/21	2.494	2.502	2.502	2.5020	2.5020	2.5021	2.5021	2.5020	0.00
24/23	3.625	3.656	3.656	3.6568	3.6573	3.6568	3.6573	3.6560	0.04
16/25	1.187	1.1946	1.1947	1.1945	1.1943	1.1944	1.1947	1.1943	0.03
3/24	198.0	200.4	200.5	200.31	200.22	200.30	200.50	200.22	0.14

SERIAL NO. 11861 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.860	1.8811	1.8800	1.8809	1.8808	1.8811	1.8811	1.8800	0.06
2-1	543.3	544.9	544.8	544.80	544.90	544.81	544.90	544.80	0.02
1-30	266.1	267.6	267.6	267.56	267.53	267.56	267.60	267.53	0.03
30-26	47.4	47.8	47.7	47.630	47.700	47.630	47.800	47.630	0.36
7-8	147.3	148.9	148.9	148.77	148.80	148.76	148.90	148.76	0.09
28-27	1.772	1.7829	1.7830	1.7826	1.7832	1.7827	1.7832	1.7826	0.03
17-18	12.500	12.538	12.538	12.538	12.539	12.539	12.539	12.538	0.01
18-19	6.457	6.511	6.511	6.5117	6.5116	6.5117	6.5117	6.5110	0.01
19-20	3.000	3.021	3.021	3.0215	3.0214	3.0211	3.0215	3.0210	0.02
20-21	495.5	499.4	499.6	499.38	499.39	499.36	499.60	499.36	0.05
21/22	492.2	495.3	495.0	495.27	497.18	495.28	497.18	495.00	0.44
24/21	2.500	2.514	2.514	2.5147	2.5153	2.5150	2.5153	2.5140	0.05
24/23	3.625	3.663	3.663	3.6635	3.6644	3.6636	3.6644	3.6630	0.04
16/25	1.1925	1.1974	1.1976	1.1975	1.1977	1.1974	1.1977	1.1974	0.03
3/24	200.0	201.1	201.1	201.04	201.66	201.06	201.66	201.04	0.31

SERIAL NO. 11836 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.861	1.8780	1.8780	1.8780	1.8778	1.8786	1.8786	1.8778	0.04
2-1	543.3	544.9	544.8	544.90	544.80	544.85	544.90	544.80	0.02
1-30	266.6	267.6	267.5	267.50	267.50	267.50	267.60	267.50	0.04
30-26	47.2	47.6	47.7	47.600	47.500	47.540	47.700	47.500	0.42
7-8	147.3	148.6	148.6	148.53	148.45	148.48	148.60	148.45	0.10
28-27	1.760	1.7823	1.7825	1.7823	1.7829	1.7823	1.7829	1.7823	0.03
17-18	12.500	12.516	12.516	12.516	12.517	12.517	12.517	12.516	0.01
18-19	6.442	6.503	6.504	6.5044	6.5043	6.5055	6.5055	6.5030	0.04
19-20	2.994	3.007	3.008	3.0070	3.0080	3.0080	3.0080	3.0070	0.03
20-21	495.5	498.4	498.4	498.40	498.40	498.38	498.40	498.38	0.00
21/22	491.1	495.0	495.0	494.97	494.93	495.00	495.00	494.93	0.01
24/21	2.500	2.510	2.510	2.5106	2.5107	2.5108	2.5108	2.5100	0.03
24/23	3.610	3.656	3.656	3.6569	3.6567	3.6573	3.6573	3.6560	0.04
16/25	1.187	1.196	1.196	1.1959	1.1957	1.1956	1.1960	1.1956	0.03
3/24	200.0	200.5	200.5	200.37	200.31	200.40	200.50	200.31	0.09

SERIAL NO. 08355 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.8810	1.8811	1.8812	1.8881	1.8810	1.8815	1.8881	1.8810	0.38
2-1	545.30	545.30	545.40	545.30	545.37	545.39	545.40	545.30	0.02
1-30	267.80	267.90	267.90	267.80	267.80	267.85	267.90	267.80	0.04
30-26	47.500	47.600	47.700	47.500	47.495	47.508	47.700	47.495	0.43
7-8	148.9	149.0	149.1	148.96	148.97	148.98	149.10	148.90	0.13
28-27	1.7817	1.7818	1.782	1.7817	1.7816	1.7817	1.7820	1.7816	0.02
17-18	12.511	12.512	12.512	12.511	12.512	12.512	12.512	12.511	0.01
18-19	6.505	6.506	6.506	6.5064	6.5062	6.5064	6.5064	6.5050	0.02
19-20	2.998	2.998	2.998	2.9984	2.9981	2.9986	2.9986	2.9980	0.02
20-21	502.1	502.1	502.1	502.05	502.04	502.06	502.10	502.04	0.01
21/22	494.7	494.7	494.8	494.72	494.18	494.18	494.80	494.18	0.13
24/21	2.507	2.507	2.507	2.5073	2.5071	2.5072	2.5073	2.5070	0.01
24/23	3.658	3.658	3.658	3.6582	3.6578	3.6577	3.6582	3.6577	0.01
16/25	1.1959	1.1958	1.1961	1.1960	1.1960	1.1956	1.1961	1.1956	0.04
3/24	200.6	200.6	200.8	200.61	200.58	200.62	200.80	200.58	0.11

SERIAL NO. 00480 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.8825	1.8826	1.8828	1.8825	1.8825	1.8827	1.8828	1.8825	0.02
2-1	546.6	546.6	546.8	546.63	546.64	546.66	546.80	546.60	0.04
1-30	267.9	267.9	268.1	267.89	267.89	267.91	268.10	267.89	0.08
30-26	47.5	47.6	47.7	47.421	47.503	47.517	47.700	47.421	0.58
7-8	148.9	148.8	149.0	148.76	148.77	148.77	149.00	148.76	0.16
28-27	1.7879	1.7879	1.7882	1.7879	1.7879	1.7880	1.7882	1.7879	0.02
17-18	12.637	12.639	12.639	12.639	12.640	12.640	12.640	12.637	0.02
18-19	6.502	6.503	6.503	6.5037	6.5035	6.5040	6.5040	6.5020	0.03
19-20	3.035	3.036	3.036	3.0361	3.0360	3.0364	3.0364	3.0350	0.05
20-21	506.3	506.3	506.5	506.34	506.34	506.36	506.50	506.30	0.04
21/22	496.0	496.1	496.3	496.09	495.59	495.59	496.30	495.59	0.14
24/21	2.509	2.509	2.510	2.5101	2.5098	2.5101	2.5101	2.5090	0.04
24/23	3.683	3.683	3.683	3.6838	3.6836	3.6836	3.6838	3.6830	0.02
16/25	1.2025	1.2027	1.2029	1.2026	1.2026	1.2026	1.2029	1.2025	0.03
3/24	199.4	199.9	200.2	199.96	200.00	200.16	200.20	199.40	0.40

SERIAL NO. 08748 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.8768	1.8768	1.8772	1.8767	1.8767	1.8769	1.8772	1.8767	0.03
2-1	545.1	545.1	545.3	545.11	545.15	545.18	545.30	545.10	0.04
1-30	267.8	267.8	268.0	267.79	267.80	267.83	268.00	267.79	0.08
30-26	47.6	47.6	48.0	47.543	47.544	47.566	48.000	47.543	0.95
7-8	148.9	148.8	149.0	148.83	148.84	148.98	149.00	148.80	0.13
28-27	1.7824	1.7826	1.7829	1.7824	1.7824	1.7826	1.7829	1.7824	0.03
17-18	12.544	12.545	12.546	12.545	12.546	12.545	12.546	12.544	0.02
18-19	6.498	6.498	6.498	6.4987	6.4985	6.4992	6.4992	6.4980	0.02
19-20	3.023	3.023	3.023	3.0234	3.0233	3.0235	3.0235	3.0230	0.02
20-21	503.4	503.4	503.5	503.42	503.44	503.44	503.50	503.40	0.02
21/22	495.6	495.5	495.8	495.60	494.81	494.80	495.80	494.80	0.20
24/21	2.578	2.578	2.578	2.5783	2.5781	2.5780	2.5783	2.5780	0.01
24/23	3.662	3.662	3.663	3.6627	3.6623	3.6622	3.6630	3.6620	0.03
16/25	1.2043	1.2044	1.2048	1.2044	1.2045	1.2046	1.2048	1.2043	0.04
3/24	200.4	200.4	200.6	200.39	200.35	200.46	200.60	200.35	0.12

SERIAL NO. 08929 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.8794	1.8793	1.8799	1.8794	1.8795	1.8795	1.8799	1.8793	0.03
2-1	544.9	544.9	545.4	544.95	544.98	545.02	545.40	544.90	0.09
1-30	267.9	268.0	268.2	267.95	267.98	268.03	268.20	267.90	0.11
30-26	47.7	47.7	48.0	47.601	47.629	47.652	48.000	47.601	0.83
7-8	148.7	148.7	149.1	148.67	148.70	148.72	149.10	148.67	0.29
28-27	1.7831	1.7832	1.7839	1.7834	1.7832	1.7834	1.7839	1.7831	0.04
17-18	12.509	12.509	12.510	12.509	12.510	12.511	12.511	12.509	0.02
18-19	6.501	6.502	6.503	6.5027	6.5024	6.5029	6.5030	6.5010	0.03
19-20	3.010	3.011	3.011	3.0113	3.0112	3.0115	3.0115	3.0100	0.05
20-21	504.7	504.8	505.2	504.81	504.81	504.85	505.20	504.70	0.10
21/22	495.4	494 4	495.7	495.47	494.82	494.83	495.70	494.40	0.26
24/21	2.498	2.498	2.499	2.4989	2.4986	2.4986	2.4990	2.4980	0.04
24/23	3.667	3.667	3.668	3.6675	3.6670	3.6670	3.6680	3.6670	0.03
16/25	1.1973	1.1973	1.1979	1.1974	1.1974	1.1976	1.1979	1.1973	0.05
3/24	200.9	201.0	201.3	200.94	200.93	201.04	201.30	200.90	0.20

SERIAL NO. 08589 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.8800	1.8799	1.8803	1.8799	1.8800	1.8800	1.8803	1.8799	0.02
2-1	545.2	545.3	545.6	545.28	545.31	545.34	545.60	545.20	0.07
1-30	268.1	268.1	268.5	268.04	268.08	268.11	268.50	268.04	0.17
30-26	47.5	47.5	47.7	47.445	47.470	47.486	47.700	47.445	0.53
7-8	148.7	148.7	149.1	148.71	148.75	148.76	149.10	148.70	0.27
28-27	1.7800	1.7799	1.7803	1.7798	1.7796	1.7801	1.7803	1.7796	0.04
17-18	12.517	12.518	12.519	12.518	12.518	12.519	12.519	12.517	0.02
18-19	6.497	6.498	6.498	6.4982	6.4980	6.4984	6.4984	6.4970	0.02
19-20	3.005	3.005	3.006	3.0056	3.0056	3.0059	3.0060	3.0050	0.03
20-21	502.1	502.2	502.6	502.15	502.14	502.18	502.60	502.10	0.10
21/22	494.5	494.5	494.9	494.50	493.94	493.96	494.90	493.94	0.19
24/21	2.499	2.499	2.499	2.4995	2.4993	2.4996	2.4996	2.4990	0.02
24/23	3.655	3.656	3.656	3.6560	3.6555	3.6557	3.6560	3.6550	0.03
16/25	1.2061	1.2061	1.2066	1.2061	1.2061	1.2063	1.2066	1.2061	0.04
3/24	200.4	200.5	200.7	200.41	200.41	200.51	200.70	200.40	0.15

SERIAL NO. 08872 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.8812	1.8813	1.8818	1.8812	1.8812	1.8812	1.8818	1.8812	0.03
2-1	545.5	545.6	545.9	545.53	545.55	545.58	545.90	545.50	0.07
1-30	268.1	268.2	268.5	268.11	268.15	268.18	268.50	268.10	0.15
30-26	48.3	48.3	48.8	48.197	48.220	48.242	48.800	48.197	1.24
7-8	148.8	148.9	149.4	148.81	148.84	148.85	149.40	148.80	0.40
28-27	1.7852	1.7853	1.7858	1.7851	1.7885	1.7853	1.7885	1.7851	0.19
17-18	12.521	12.521	12.522	12.520	12.521	12.522	12.522	12.520	0.02
18-19	6.508	6.508	6.509	6.5090	6.5089	6.5092	6.5092	6.5080	0.02
19-20	3.006	3.006	3.007	3.0069	3.0064	3.0069	3.0070	3.0060	0.03
20-21	504.8	504.8	505.2	504.82	504.82	504.85	505.20	504.80	0.08
21/22	495.8	495.9	496.2	495.82	495.28	495.32	496.20	495.28	0.19
24/21	2.506	2.506	2.507	2.5064	2.5061	2.5063	2.5070	2.5060	0.04
24/23	3.675	3.675	3.675	3.6755	3.6753	3.6755	3.6755	3.6750	0.01
16/25	1.1996	1.1996	1.2001	1.1996	1.1997	1.1997	1.2001	1.1996	0.04
3/24	202.5	202.6	203.0	202.51	202.49	202.62	203.00	202.49	0.25

SERIAL NO. 08584 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.8771	1.8772	1.8779	1.8770	1.8770	1.8771	1.8779	1.8770	0.05
2-1	545.0000	545.1000	545.6000	545.00	545.02	545.04	545.60	545.00	0.11
1-30	269.0000	269.0000	269.6000	268.94	268.98	269.02	269.60	268.94	0.24
30-26	47.7000	47.7000	48.2000	47.596	47.621	47.643	48.200	47.596	1.25
7-8	148.8000	148.8000	149.3000	148.74	148.77	148.79	149.30	148.74	0.38
28-27	1.7846	1.7847	1.7851	1.7845	1.7843	1.7847	1.7851	1.7843	0.04
17-18	12.5320	12.5330	12.5340	12.533	12.534	12.534	12.534	12.532	0.02
18-19	6.4920	6.4920	6.4930	6.4933	6.4931	6.4936	6.4936	6.4920	0.02
19-20	3.009	3.0090	3.0100	3.0100	3.0100	3.0104	3.0104	3.0090	0.05
20-21	502.0000	502.1000	502.4000	502.07	502.13	502.18	502.40	502.00	0.08
21/22	495.5000	495.6000	495.9000	495.53	494.62	494.65	495.90	494.62	0.26
24/21	2.5660	2.5660	2.5670	2.5666	2.5663	2.5665	2.5670	2.5660	0.04
24/23	3.6640	3.6650	3.6650	3.6650	3.6646	3.6647	3.6650	3.6640	0.03
16/25	1.1982	1.1983	1.1986	1.1982	1.1983	1.1983	1.1986	1.1982	0.03
3/24	201.1	201.1	201.3	201.09	201.07	201.16	201.30	201.07	0.11

SERIAL NO. 07941 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.9119	1.9121	1.9122	1.9119	1.9120	1.9120	1.9122	1.9119	0.02
2-1	553.2	553.3	553.6	553.26	553.26	553.32	553.60	553.20	0.07
1-30	271.8	271.9	272.1	271.78	271.83	271.85	272.10	271.78	0.12
30-26	47.5	47.6	47.6	47.408	47.438	47.457	47.600	47.408	0.40
7-8	153.1	153.2	153.4	153.08	153.12	153.15	153.40	153.08	0.21
28-27	1.7786	1.7786	1.7790	1.7784	1.7783	1.7787	1.7790	1.7783	0.04
17-18	12.457	12.457	12.457	12.456	12.457	12.458	12.458	12.456	0.02
18-19	6.492	6.492	6.492	6.4922	6.4920	6.4933	6.4933	6.4920	0.02
19-20	300.300	3.003	3.003	3.0032	3.0031	3.0035	3.0030	3.0030	0.00
20-21	501.2	501.2	501.6	501.22	501.24	501.26	501.60	501.20	0.08
21/22	493.9	493.9	494.1	493.88	493.35	493.41	494.10	493.35	0.15
24/21	2.491	2.491	2.491	2.4912	2.4910	2.4912	2.4912	2.4910	0.01
24/23	3.653	3.653	3.654	3.6538	3.6536	3.6537	3.6540	3.6530	0.03
16/25	1.1941	1.1942	1.1944	1.1940	1.1942	1.1942	1.1944	1.1940	0.03
3/24	200.1	200.2	200.4	200.09	200.09	200.19	200.40	200.09	0.15

SERIAL NO. 08290 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.8896	1.8900	1.8901	1.8897	1.8897	1.8898	1.8901	1.8896	0.03
2-1	544.9	545.0	545.2	544.91	544.93	544.97	545.20	544.90	0.06
1-30	267.8	267.9	268.1	267.80	267.81	267.86	268.10	267.80	0.11
30-26	47.5	47.5	47.6	47.332	47.357	47.374	47.600	47.332	0.56
7-8	XXX.X	XXX.X	XXX.X	XXX.XX	XXX.XX	XXX.XX	0.00	0.00	#DIV/0!
28-27	1.7799	1.7799	1.7802	1.7787	1.7797	1.7801	1.7802	1.7787	0.08
17-18	12.565	12.566	12.566	12.565	12.566	12.566	12.566	12.565	0.01
18-19	6.505	6.505	6.505	6.5052	6.5051	6.5055	6.5055	6.5050	0.01
19-20	3.019	3.020	3.020	3.0202	3.0202	3.0206	3.0206	3.0190	0.05
20-21	505.8	505.8	506.0	505.79	505.78	505.80	506.00	505.78	0.04
21/22	494.4	494.4	494.6	494.34	493.89	493.91	494.60	493.89	0.14
24/21	2.513	2.513	2.513	2.5130	2.5128	2.5132	2.5132	2.5128	0.02
24/23	3.657	3.657	3.657	3.6566	3.6566	3.6565	3.6570	3.6566	0.01
16/25	1.2080	1.2081	1.2082	1.2081	1.2081	1.2081	1.2082	1.2080	0.02
3/24	200.2	200.2	200.3	200.12	200.11	200.20	200.30	200.11	0.09

SERIAL NO. 08388 RESISTANCES

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	PERCENT DELTA
4-2	1.8803	1.8804	1.8804	1.8801	1.8801	1.8803	1.8804	1.8801	0 02
2-1	544.8	544.9	545.0	544.81	544.85	544.87	545.00	544.80	0.04
1-30	268.0	268.2	268.2	267.97	268.04	268.04	268.20	267.97	0.09
30-26	47.6	47.7	47.7	47.485	47.513	47.535	47.700	47.485	0.45
7-8	148.8	148.9	149.0	148.75	148.79	148.78	149.00	148.75	0.17
28-27	1.7782	1.7782	1.7783	1.7779	1.7778	1.7782	1.7783	1.7778	0 03
17-18	12.539	12.539	12.539	12.538	12.539	12.540	12.540	12.538	0.02
18-19	6.513	6.512	6.513	6.5128	6.5172	6.5126	6.5172	6.5120	0.08
19-20	3.011	3.011	3.011	3.0115	3.0115	3.0118	3.0118	3.0110	0.03
20-21	502.5	502.6	502.7	502.50	502.53	502.53	502.70	502.50	0.04
21/22	494.7	494.8	494.9	494.68	494.25	494.29	494.90	494.25	0.13
24/21	2.507	2.507	2.507	2.5071	2.5070	2.5071	2.5071	2.5070	0.00
24/23	3.652	3.652	3.652	3.6519	3.6516	3.6515	3.6520	3.6515	0.01
16/25	1.1960	1.1962	1.1962	1.1959	1.1961	1.1960	1.1962	1.1959	0.03
3/24	200.3	200.5	200.6	200.30	200.30	200.41	200.60	200.30	0.15

SERIAL NO. 12183 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	1.0E-09	4.0E-10	4.0E-10	3.0E-10	3.0E-10	2.0E-10	1.0E-09	2.0E-10	8.0E-10
4-5	6.0E-09	6.2E-09	7.0E-09	6.4E-09	7.2E-09	6.7E-09	7.2E-09	6.2E-09	1.0E-09
28-6	5.5E-09	6.0E-09	6.9E-09	6.0E-09	7.8E-09	6.3E-09	7.8E-09	6.0E-09	1.8E-09
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
14-10	2.1E-03	9.2E-05	6.1E-05	1.4E-04	6.5E-05	4.9E-05	2.1E-03	4.9E-05	2.1E-03
10-7	1.0E-10	2.0E-10	0.0E+00	3.0E-10	2.0E-10	2.0E-10	3.0E-10	0.0E+00	3.0E-10
14-7	1.5E-05	5.0E-07	3.9E-07	9.9E-07	5.5E-07	4.0E-07	1.5E-05	3.9E-07	1.5E-05
4-7	8.2E-07	4.0E-08	4.4E-08	4.0E-08	6.4E-08	4.0E-08	8.2E-07	4.0E-08	7.8E-07
4-12	3.1E-09	1.0E-10	0.0E+00	1.0E-10	0.0E+00	1.0E-10	3.1E-09	0.0E+00	3.1E-09
12-7	1.4E-05	1.4E-05	1.5E-05	1.3E-05	1.7E-05	8.2E-06	1.7E-05	8.2E-06	8.3E-06

SERIAL NO. 11650 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	1.0E-09	5.0E-10	5.0E-10	5.0E-10	3.0E-10	2.0E-10	1.0E-09	2.0E-10	8.0E-10
4-5	7.0E-09	7.5E-09	8.3E-09	7.5E-09	1.0E-08	7.8E-09	1.0E-08	7.5E-09	2.5E-09
28-6	6.2E-09	6.5E-09	7.4E-09	6.6E-09	8.6E-09	6.9E-09	8.6E-09	6.5E-09	2.1E-09
28-29	0.0E+00	0.0E+00	0.0E+00	1.0E-10	0.0E+00	1.0E-10	1.0E-10	0.0E+00	1.0E-10
14-10	1.8E-06	9.2E-07	1.2E-06	1.1E-06	1.4E-06	1.1E-06	1.8E-06	9.2E-07	8.8E-07
10-7	1.0E-10	3.0E-10	1.0E-10	4.0E-10	2.0E-10	2.0E-10	4.0E-10	1.0E-10	3.0E-10
14-7	3.1E-08	2.4E-08	2.7E-08	2.4E-08	4.0E-08	2.4E-08	4.0E-08	2.4E-08	1.6E-08
4-7	2.0E-08	6.0E-10	5.0E-10	4.0E-10	4.0E-10	4.0E-10	2.0E-08	4.0E-10	2.0E-08
4-12	1.0E-09	8.0E-10	5.0E-10	1.0E-09	8.0E-10	1.0E-09	1.0E-09	5.0E-10	5.0E-10
12-7	3.2E-08	8.0E-09	1.0E-09	9.8E-09	2.2E-08	8.1E-09	3.2E-08	1.0E-09	3.1E-08

SERIAL NO. 12034 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	8.0E-10	6.0E-10	5.0E-10	4.0E-10	3.0E-10	2.0E-10	8.0E-10	2.0E-10	6.0E-10
4-5	6.3E-09	6.9E-09	7.5E-09	6.9E-09	7.0E-09	7.0E-09	7.5E-09	6.9E-09	6.0E-10
28-6	7.0E-09	8.4E-09	8.5E-09	7.6E-09	8.9E-09	7.9E-09	8.9E-09	7.6E-09	1.3E-09
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
14-10	1.6E-06	4.0E-08	1.4E-06	1.2E-06	1.9E-06	1.4E-06	1.9E-06	4.0E-08	1.8E-06
10-7	1.0E-10	1.7E-08	1.0E-10	4.0E-10	2.0E-10	2.0E-10	1.7E-08	1.0E-10	1.7E-08
14-7	2.7E-08	2.4E-08	2.3E-08	2.2E-08	3.5E-08	2.3E-08	3.5E-08	2.2E-08	1.3E-08
4-7	1.8E-08	6.0E-10	5.0E-10	9.0E-10	6.0E-10	4.0E-10	1.8E-08	4.0E-10	1.8E-08
4-12	2.0E-09	1.1E-09	1.5E-09	1.9E-09	1.6E-09	1.9E-09	2.0E-09	1.1E-09	9.0E-10
12-7	2.6E-08	7.5E-09	7.5E-09	7.0E-09	1.5E-08	6.8E-09	2.6E-08	6.8E-09	1.9E-08

SERIAL NO. 11789 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	8.0E-10	6.0E-10	5.0E-10	4.0E-10	8.0E-10	2.0E-10	8.0E-10	2.0E-10	6.0E-10
4-5	5.0E-09	6.0E-09	6.1E-09	6.2E-09	6.0E-09	6.0E-09	6.2E-09	6.0E-09	2.0E-10
28-6	6.5E-09	7.5E-09	7.5E-09	7.6E-09	8.3E-09	7.4E-09	8.3E-09	7.4E-09	9.0E-10
28-29	0.0E+00	0.0E+00	0.0E+00	1.0E-10	0.0E+00	0.0E+00	1.0E-10	0.0E+00	1.0E-10
14-10	8.5E-06	2.1E-06	2.4E-06	2.3E-06	3.5E-06	2.2E-06	8.5E-06	2.1E-06	6.4E-06
10-7	1.0E-10	1.0E-10	1.0E-10	2.0E-10	2.0E-10	2.0E-10	2.0E-10	1.0E-10	1.0E-10
14-7	5.4E-08	2.4E-08	2.4E-08	2.3E-08	3.8E-08	2.3E-08	5.4E-08	2.3E-08	3.1E-08
4-7	1.8E-08	5.0E-10	4.0E-10	5.0E-10	8.0E-09	3.0E-10	1.8E-08	3.0E-10	1.8E-08
4-12	1.0E-10	0.0E+00	0.0E+00	1.0E-10	0.0E+00	1.0E-10	1.0E-10	0.0E+00	1.0E-10
12-7	5.2E-08	4.2E-08	4.0E-08	4.3E-08	6.5E-08	2.2E-08	6.5E-08	2.2E-08	4.3E-08

SERIAL NO. 11861 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	9.0E-10	6.0E-10	5.0E-10	4.0E-10	8.0E-10	0.0E+00	9.0E-10	0.0E+00	9.0E-10
4-5	7.0E-09	7.8E-09	8.0E-09	8.0E-09	8.2E-09	8.0E-09	8.2E-09	7.8E-09	4.0E-10
28-6	6.0E-09	6.9E-09	7.0E-09	7.0E-09	7.2E-09	7.0E-09	7.2E-09	6.9E-09	3.0E-10
28-29	1.0E-10	2.0E-10	1.0E-10	2.0E-10	2.0E-10	2.0E-10	2.0E-10	1.0E-10	1.0E-10
14-10	5.9E-07	4.7E-07	5.0E-07	4.8E-07	4.6E-07	4.7E-07	5.9E-07	4.6E-07	1.3E-07
10-7	1.0E-10	1.0E-10	1.0E-10	2.0E-10	2.0E-10	2.0E-10	2.0E-10	1.0E-10	1.0E-10
14-7	2.4E-08	2.1E-08	2.2E-08	1.9E-08	2.1E-08	2.0E-08	2.4E-08	1.9E-08	4.8E-09
4-7	1.7E-08	7.0E-10	1.0E-09	5.0E-10	1.0E-09	5.0E-10	1.7E-08	5.0E-10	1.7E-08
4-12	2.5E-09	2.2E-09	2.0E-09	2.0E-09	2.0E-09	2.2E-09	2.5E-09	2.0E-09	5.0E-10
12-7	2.4E-08	6.8E-09	6.9E-09	5.9E-09	6.3E-09	6.1E-09	2.4E-08	5.9E-09	1.8E-08

SERIAL NO. 11836 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	7.0E-10	4.0E-10	4.0E-10	4.0E-10	8.0E-10	0.0E+00	8.0E-10	0.0E+00	8.0E-10
4-5	4.8E-09	5.3E-09	5.6E-09	5.8E-09	5.1E-09	5.6E-09	5.8E-09	5.1E-09	7.0E-10
28-6	5.2E-09	6.0E-09	6.4E-09	6.2E-09	6.0E-09	6.4E-09	6.4E-09	6.0E-09	4.0E-10
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
14-10	8.2E-06	1.6E-06	1.7E-06	1.6E-06	1.4E-06	1.6E-09	8.2E-06	1.6E-09	8.2E-06
10-7	1.0E-10	0.0E+00	0.0E+00	2.0E-10	2.0E-10	1.0E-10	2.0E-10	0.0E+00	2.0E-10
14-7	1.0E-07	3.2E-08	3.3E-08	3.2E-08	3.0E-08	3.1E-08	1.0E-07	3.0E-08	7.2E-08
4-7	2.6E-08	8.0E-10	4.0E-10	6.0E-10	8.0E-10	6.0E-10	2.6E-08	4.0E-10	2.6E-08
4-12	1.0E-10	0.0E+00	0.0E+00	0.0E+00	1.0E-10	1.0E-10	1.0E-10	0.0E+00	1.0E-10
12-7	1.0E-07	8.5E-08	8.7E-08	8.5E-08	7.0E-08	6.8E-08	1.0E-07	6.8E-08	3.6E-08

SERIAL NO. 08355 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	5.0E-10	6.0E-10	6.0E-10	4.0E-10	0.0E+00	1.0E-10	6.0E-10	0.0E+00	6.0E-10
4-5	1.0E-08	1.2E-08	1.0E-08	1.1E-08	1.1E-08	1.3E-08	1.3E-08	1.0E-08	2.5E-09
28-6	9.5E-09	1.2E-08	1.0E-08	1.0E-08	1.1E-08	1.2E-08	1.2E-08	9.5E-09	2.7E-09
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
14-10	3.0E-08	2.3E-08	2.2E-08	2.2E-08	2.3E-08	2.2E-08	3.0E-08	2.2E-08	8.0E-09
10-7	3.0E-08	8.6E-08	2.7E-08	2.7E-08	2.5E-08	2.5E-08	8.6E-08	2.5E-08	6.1E-08
14-7	3.0E-08	2.1E-08	2.0E-08	2.2E-08	2.2E-08	2.2E-08	3.0E-08	2.0E-08	1.0E-08
4-7	2.3E-08	5.2E-09	5.0E-09	5.0E-09	5.2E-09	5.8E-09	2.3E-08	5.0E-09	1.8E-08
4-12	2.0E-09	2.0E-10	3.0E-10	1.0E-10	2.0E-10	2.0E-10	2.0E-09	1.0E-10	1.9E-09
12-7	3.0E-08	2.0E-07	1.9E-07	1.4E-07	3.8E-07	4.5E-07	4.5E-07	3.0E-08	4.2E-07

SERIAL NO. 00480 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	1.3E-09	1.2E-09	1.5E-09	1.3E-09	1.3E-09	1.2E-09	1.5E-09	1.2E-09	3.0E-10
4-5	1.0E-09	4.0E-10	1.4E-09	1.3E-09	1.2E-09	1.5E-09	1.5E-09	4.0E-10	1.1E-09
28-6	7.0E-09	5.0E-09	7.0E-09	7.2E-08	1.2E-09	8.5E-09	7.2E-08	1.2E-09	7.1E-08
28-29	2.0E-10	0.0E+00	0.0E+00	1.0E-10	0.0E+00	1.0E-10	2.0E-10	0.0E+00	2.0E-10
14-10	8.2E-06	4.2E-06	4.2E-06	4.3E-06	4.4E-06	4.5E-06	8.2E-06	4.2E-06	4.0E-06
10-7	5.0E-10	2.0E-10	1.0E-10	3.0E-10	2.0E-10	2.0E-10	5.0E-10	1.0E-10	4.0E-10
14-7	3.0E-08	2.6E-08	2.5E-08	2.5E-08	2.6E-08	2.7E-08	3.0E-08	2.5E-08	5.0E-09
4-7	2.5E-08	4.4E-09	4.0E-09	4.4E-09	4.7E-09	4.3E-09	2.5E-08	4.0E-09	2.1E-08
4-12	2.5E-09	5.0E-10	5.0E-10	4.0E-10	4.0E-10	4.0E-10	2.5E-09	4.0E-10	2.1E-09
12-7	3.0E-08	1.1E-07	1.4E-07	1.8E-07	4.1E-07	4.5E-07	4.5E-07	3.0E-08	4.2E-07

SERIAL NO. 08748 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	4.0E-10	4.0E-10	5.0E-10	2.0E-10	0.0E+00	1.0E-10	5.0E-10	0.0E+00	5.0E-10
4-5	6.0E-09	6.5E-09	6.0E-09	6.2E-09	6.5E-09	7.0E-09	7.0E-09	6.0E-09	1.0E-09
28-6	8.0E-09	8.2E-09	7.8E-09	8.0E-09	1.1E-08	1.3E-08	1.3E-08	7.8E-09	5.2E-09
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
14-10	1.2E-03	7.1E-04	6.3E-04	9.6E-04	5.0E-04	5.0E-04	1.2E-03	5.0E-04	7.0E-04
10-7	2.0E-10	2.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	2.0E-10	1.0E-10	1.0E-10
14-7	5.2E-06	3.2E-06	2.9E-06	4.3E-06	2.3E-06	2.3E-06	5.2E-06	2.3E-06	2.9E-06
4-7	4.1E-09	6.1E-09	5.5E-09	5.5E-09	6.0E-09	6.0E-09	6.1E-09	4.1E-09	2.0E-09
4-12	3.0E-09	6.0E-10	1.0E-09	1.0E-09	1.1E-09	1.0E-09	3.0E-09	6.0E-10	2.4E-09
12-7	5.1E-09	1.4E-07	1.6E-07	1.6E-07	2.5E-07	2.6E-07	2.6E-07	5.1E-09	2.5E-07

SERIAL NO. 08929 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	4.0E-09	2.5E-09	2.8E-09	2.5E-09	9.0E-09	2.5E-09	9.0E-09	2.5E-09	6.5E-09
4-5	6.0E-09	6.0E-09	6.0E-09	5.8E-09	6.2E-09	6.5E-09	6.5E-09	5.8E-09	7.0E-10
28-6	6.6E-09	6.4E-09	6.4E-09	6.2E-09	6.8E-09	7.2E-09	7.2E-09	6.2E-09	1.0E-09
28-29	2.0E-10	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	2.0E-10	0.0E+00	2.0E-10
14-10	2.8E-04	2.8E-06	2.8E-06	2.9E-06	2.8E-06	2.9E-06	2.8E-04	2.8E-06	2.7E-04
10-7	1.2E-09	4.0E-10	1.0E-10	4.0E-10	4.0E-10	3.0E-10	1.2E-09	1.0E-10	1.1E-09
14-7	1.0E-06	2.6E-08	2.2E-08	2.3E-08	2.3E-08	2.3E-08	1.0E-06	2.2E-08	9.8E-07
4-7	2.5E-08	6.0E-09	5.9E-09	7.5E-09	5.8E-09	6.8E-09	2.5E-08	5.8E-09	1.9E-08
4-12	2.8E-09	9.0E-10	8.0E-10	8.0E-10	8.0E-10	8.0E-10	2.8E-09	8.0E-10	2.0E-09
12-7	1.0E-06	4.8E-08	6.0E-07	6.1E-07	7.8E-07	8.1E-07	1.0E-06	4.8E-08	9.5E-07

SERIAL NO. 08589 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	6.0E-10	8.0E-10	5.0E-10	2.0E-10	0.0E+00	1.0E-10	8.0E-10	0.0E+00	8.0E-10
4-5	8.0E-09	8.2E-09	8.0E-09	8.0E-09	8.3E-09	8.9E-09	8.9E-09	8.0E-09	9.0E-10
28-6	5.8E-09	6.0E-09	5.9E-09	6.0E-09	1.0E-08	1.0E-08	1.0E-08	5.8E-09	4.5E-09
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
14-10	4.6E-06	2.4E-06	2.3E-06	2.3E-06	2.3E-06	2.3E-06	4.6E-06	2.3E-06	2.4E-06
10-7	2.0E-10	2.0E-10	1.0E-10	2.0E-10	2.0E-10	2.0E-10	2.0E-10	1.0E-10	1.0E-10
14-7	2.8E-08	1.7E-08	1.7E-08	1.7E-08	1.7E-08	1.7E-08	2.8E-08	1.7E-08	1.1E-08
4-7	2.0E-08	5.2E-09	5.1E-09	5.5E-09	6.0E-09	5.5E-09	2.0E-08	5.1E-09	1.5E-08
4-12	3.0E-09	9.0E-10	1.0E-09	6.0E-10	1.0E-09	1.0E-09	3.0E-09	6.0E-10	2.4E-09
12-7	2.8E-08	2.1E-07	2.3E-07	2.4E-07	3.8E-07	4.4E-07	4.4E-07	2.8E-08	4.1E-07

SERIAL NO. 08872 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	2.0E-09	2.2E-09	2.0E-09	2.0E-09	2.2E-09	2.4E-09	2.4E-09	2.0E-09	4.0E-10
4-5	1.4E-09	1.5E-09	1.3E-09	1.2E-09	1.4E-09	1.4E-09	1.5E-09	1.2E-09	3.0E-10
28-6	1.4E-09	1.6E-09	8.0E-10	1.3E-09	1.3E-09	1.5E-09	1.6E-09	8.0E-10	8.0E-10
28-29	4.0E-10	4.0E-10	4.0E-10	4.0E-10	4.0E-10	4.0E-10	4.0E-10	4.0E-10	0.0E+00
14-10	1.8E-04	2.9E-06	2.7E-06	2.8E-06	2.8E-06	2.8E-06	1.8E-04	2.7E-06	1.7E-04
10-7	2.0E-10	1.0E-10	2.0E-10	2.0E-10	2.0E-10	2.0E-10	2.0E-10	1.0E-10	1.0E-10
14-7	7.0E-07	2.4E-08	2.3E-08	2.3E-08	2.3E-08	2.3E-08	7.0E-07	2.3E-08	6.8E-07
4-7	2.5E-08	5.4E-09	5.0E-09	5.0E-09	5.2E-09	5.2E-09	2.5E-08	5.0E-09	2.0E-08
4-12	2.2E-09	2.0E-10	4.0E-10	2.0E-10	3.0E-10	2.0E-10	2.2E-09	2.0E-10	2.0E-09
12-7	7.0E-07	7.1E-07	6.8E-07	7.9E-07	7.0E-07	7.4E-07	7.9E-07	6.8E-07	1.1E-07

SERIAL NO. 08584 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	6.0E-10	6.0E-10	4.0E-10	2.0E-10	1.0E-10	1.0E-10	6.0E-10	1.0E-10	5.0E-10
4-5	6.0E-09	7.2E-09	6.5E-09	6.6E-09	6.6E-09	7.0E-09	7.2E-09	6.0E-09	1.2E-09
28-6	6.0E-09	7.4E-09	6.5E-09	6.7E-09	6.7E-09	6.9E-09	7.4E-09	6.0E-09	1.4E-09
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
14-10	4.1E-06	3.6E-06	2.5E-06	3.5E-06	2.7E-06	2.7E-06	4.1E-06	2.5E-06	1.6E-06
10-7	2.0E-10	4.0E-10	4.0E-10	8.0E-10	8.0E-10	3.0E-10	8.0E-10	2.0E-10	6.0E-10
14-7	6.2E-08	5.5E-08	4.2E-08	5.4E-08	4.3E-08	4.3E-08	6.2E-08	4.2E-08	2.0E-08
4-7	5.2E-08	6.0E-09	5.4E-09	5.8E-09	5.8E-09	5.8E-09	5.2E-08	5.4E-09	4.7E-08
4-12	1.6E-08	9.0E-10	4.0E-10	9.0E-10	8.0E-10	8.0E-10	1.6E-08	4.0E-10	1.6E-08
12-7	6.2E-08	1.0E-07	1.4E-07	1.4E-07	3.5E-07	4.2E-07	4.2E-07	6.2E-08	3.6E-07

SERIAL NO. 07941 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	1.0E-09	8.0E-10	1.0E-09	1.2E-09	1.0E-09	1.0E-09	1.2E-09	8.0E-10	4.0E-10
4-5	6.0E-09	7.0E-09	6.8E-09	6.7E-09	6.7E-09	7.0E-09	7.0E-09	6.0E-09	1.0E-09
28-6	7.5E-09	8.4E-09	8.0E-09	8.2E-09	1.2E-08	8.5E-09	1.2E-08	7.5E-09	4.4E-09
28-29	5.0E-10	4.0E-10	4.0E-10	6.0E-10	6.0E-10	4.0E-10	6.0E-10	4.0E-10	2.0E-10
14-10	4.4E-06	3.7E-06	3.3E-06	3.4E-06	3.4E-06	3.3E-06	4.4E-06	3.3E-06	1.1E-06
10-7	1.0E-10	2.0E-10	3.0E-10	4.0E-10	4.0E-10	1.0E-10	4.0E-10	1.0E-10	3.0E-10
14-7	2.5E-08	2.1E-08	2.2E-08	2.1E-08	2.0E-08	2.0E-08	2.5E-08	2.0E-08	5.0E-09
4-7	2.1E-08	5.0E-09	4.8E-09	5.0E-09	5.0E-09	5.0E-09	2.1E-08	4.8E-09	1.6E-08
4-12	2.5E-09	5.0E-10	8.0E-10	1.0E-09	8.0E-10	8.0E-10	2.5E-09	5.0E-10	2.0E-09
12-7	2.5E-08	7.5E-08	1.0E-07	1.8E-07	2.8E-07	3.1E-07	3.1E-07	2.5E-08	2.9E-07

SERIAL NO. 08290 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	6.0E-10	6.0E-10	5.0E-10	4.0E-10	0.0E+00	0.0E+00	6.0E-10	0.0E+00	6.0E-10
4-5	1.0E-08	1.2E-08	1.1E-08	1.1E-08	1.1E-08	1.1E-08	1.2E-08	1.0E-08	2.4E-09
28-6	1.0E-08	1.3E-08	1.1E-08	1.1E-08	1.2E-08	1.3E-08	1.3E-08	1.0E-08	2.5E-09
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
14-10	2.4E-06	2.5E-06	2.2E-06	2.4E-06	2.3E-06	2.3E-06	2.5E-06	2.2E-06	3.0E-07
10-7	5.0E-10	2.0E-10	3.0E-10	3.0E-10	2.0E-10	1.0E-10	5.0E-10	1.0E-10	4.0E-10
14-7	2.5E-08	9.2E-09	1.9E-08	1.9E-08	1.9E-08	2.0E-08	2.5E-08	9.2E-09	1.6E-08
4-7	2.2E-08	5.5E-09	4.8E-09	5.2E-09	5.2E-09	5.0E-09	2.2E-08	4.8E-09	1.7E-08
4-12	3.2E-09	1.2E-09	1.0E-09	1.2E-09	1.2E-09	1.2E-09	3.2E-09	1.0E-09	2.2E-09
12-7	2.5E-08	4.6E-08	9.0E-08	9.0E-08	2.3E-07	2.7E-07	2.7E-07	2.5E-08	2.5E-07

SERIAL NO. 08388 LEAKAGE CURRENTS

PINS	INITIAL SCREEN	POST HTRB	POST BAKE	PRE-BURN-IN	POST BURN-IN	STEP 6	MAXIMUM	MINIMUM	DELTA
26-24	5.0E-10	8.0E-10	4.0E-10	2.0E-10	9.0E-10	1.0E-09	1.0E-09	2.0E-10	8.0E-10
4-5	6.5E-09	7.1E-09	7.0E-09	6.9E-09	6.9E-09	6.9E-09	7.1E-09	6.5E-09	6.0E-10
28-6	7.4E-09	8.0E-09	8.0E-09	7.8E-09	1.1E-08	1.2E-08	1.2E-08	7.4E-09	4.4E-09
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00
14-10	3.1E-06	2.4E-06	2.3E-06	2.3E-06	2.3E-06	2.2E-06	3.1E-06	2.2E-06	9.0E-07
10-7	1.0E-10	2.0E-10	3.0E-10	3.0E-10	1.0E-10	1.0E-10	3.0E-10	1.0E-10	2.0E-10
14-7	2.8E-08	7.1E-09	1.9E-08	1.9E-08	1.9E-08	1.9E-08	2.8E-08	7.1E-09	2.1E-08
4-7	2.1E-08	1.6E-09	5.2E-09	5.6E-09	5.6E-09	5.2E-09	2.1E-08	1.6E-09	1.9E-08
4-12	3.0E-09	1.0E-09	1.2E-09	1.2E-09	1.2E-09	1.2E-09	3.0E-09	1.0E-09	2.0E-09
12-7	2.9E-08	6.9E-08	8.4E-08	8.3E-08	2.0E-07	2.4E-07	2.4E-07	2.9E-08	2.1E-07

VOLTAGE MAXIMUM RANGE TABLE

VOLTAGE	11183	11650	12034	11789	11861	11683	MAXIMUM
V01	50.050	50.045	50.030	50.040	50.040	50.042	50.05
V03	50.050	50.045	50.030	50.040	50.040	50.042	50.05
V05	25.023	25.035	25.032	25.036	25.025	25.023	25.036
V07	25.023	25.035	25.032	25.034	25.025	25.023	25.035
V09	12.030	12.022	12.040	12.033	12.036	12.021	12.040
V011	12.030	12.022	12.040	12.033	12.036	12.021	12.040
V013	6.021	6.010	6.010	6.010	6.010	6.010	6.021
V015	6.020	6.010	6.010	6.01[illegible]	6.010	6.010	6.020
V017	5.079	5.020	5.015	5.0[illegible]	5.014	5.013	5.079
V019	5.071	5.020	5.015	5.024	5.014	5.012	5.071
V0R	10.010	10.020	10.021	10.030	10.000	10.010	10.030

VOLTAGE MINIMUM RANGE TABLE

VOLTAGE	11183	11650	12034	11789	11861	11683	MINIMUM
V01	50.041	50.038	50.019	50.030	50.028	50.030	50.019
V03	50.041	50.038	50.019	50.030	50.028	50.032	50.019
V05	25.020	25.030	25.027	25.030	25.020	25.019	25.019
V07	25.020	25.030	25.027	25.030	25.020	25.019	25.019
V09	12.029	12.019	12.037	12.020	12.030	12.019	12.019
V011	12.029	12.019	12.037	12.020	12.030	12.018	12.018
V013	6.007	6.002	6.006	6.007	6.006	6.006	6.002
V015	6.007	6.002	6.006	6.007	6.006	6.006	6.002
V017	5.010	5.010	5.010	5.010	5.010	5.010	5.010
V019	5.010	5.010	5.010	5.010	5.010	5.010	5.010
V0R	10.006	10.010	10.018	10.020	9.996	10.007	9.996

VOLTAGE PERCENT DELTA RANGE TABLE

VOLTAGE	11183	11650	12034	11789	11861	11683	MAXIMUM
V01	0.02	0 01	0.02	0.02	0.02	0.02	0.02
V03	0.02	0.01	0.02	0.02	0.02	0.02	0.02
V05	0.01	0.02	0.02	0.02	0.02	0.02	0.02
V07	0.01	0.02	0.02	0.02	0.02	0.02	0.02
V09	0.01	0.02	0.02	0.11	0.05	0.02	0.11
V011	0.01	0.02	0.02	0.11	0.05	0.02	0.11
V013	0.22	0.13	0.07	0.05	0.07	0.07	0.22
V015	0.22	0.13	0.07	0.05	0.07	0.07	0.22
V017	1.36	0.20	0.10	0.28	0.07	0.06	1.36
V019	1.20	0.20	0.10	0.28	0.07	0.04	1.20
V0R	0.04	0.10	0.03	0.10	0.04	0.03	0.10

VOLTAGE MAXIMUM RANGE TABLE

VOLTAGE	08355	00480	08748	08921	08589	08872	08584	07941	08290	08388	MAXIMUM
V01	50.940	50.260	50.490	50.920	50.370	50.770	51.650	50.570	50.590	50.740	51.650
V03	50.940	50.260	50.490	50.920	50.370	50.770	51.650	50.570	50.590	50.740	51.650
V05	25.420	25.070	25.200	25.430	25.160	25.340	25.720	25.280	25.220	25.320	25.720
V07	25.420	25.070	25.200	25.430	25.150	25.340	25.720	25.280	25.220	25.310	25.720
V09	12.141	12.060	12.095	12.150	12.060	12.128	12.292	12.100	12.121	12.108	12.292
V011	12.140	12.084	12.092	12.150	12.060	12.128	12.291	12.099	12.119	12.108	12.291
V013	6.019	6.006	6.005	6.016	6.009	6.024	6.065	6.006	6.048	6.050	6.065
V015	6.018	6.006	6.005	6.014	6.009	6.024	6.065	6.006	6.046	6.049	6.065
V017	4.999	5.008	5.001	4.983	4.999	5.030	5.018	4.991	5.101	4.992	5.101
V019	4.999	5.008	5.001	4.983	4.999	5.030	5.018	4.991	5.094	4.992	5.094
V0R	10.091	9.980	10.020	10.076	10.026	10.067	10.185	10.060	10.098	10.050	10.185

VOLTAGE MINIMUM RANGE TABLE

VOLTAGE	08355	00480	08748	08921	08589	08872	08584	07941	08290	08388	MINIMUM
V01	50.040	50.185	49.720	49.870	50.090	50.000	50.160	50.100	50.070	50.210	49.72
V03	50.040	50.185	49.720	49.870	50.090	50.000	50.150	50.100	50.070	50.210	49.72
V05	25.050	25.000	24.855	24.940	25.020	25.000	25.070	25.070	25.000	25.120	24.86
V07	25.050	25.000	24.850	24.940	25.020	25.000	25.080	25.070	25.000	25.120	24.85
V09	11.980	12.040	11.970	11.970	12.010	12.000	12.030	12.020	12.020	12.020	11.97
V011	11.980	12.040	11.970	11.970	12.010	12.000	12.030	12.020	12.020	12.020	11.97
V013	6.000	6.000	5.980	5.970	6.000	6.000	6.000	5.990	5.990	5.990	5.97
V015	5.980	6.000	5.980	5.970	6.000	6.000	6.000	5.990	5.990	5.990	5.97
V017	4.990	4.990	4.980	4.960	4.990	4.990	4.990	4.980	4.980	4.980	4.96
V019	4.980	4.990	4.980	4.960	4.990	4.990	4.990	4.980	4.980	4.980	4.96
V0R	9.980	9.969	9.950	9.950	9.990	9.970	10.000	10.000	10.017	9.990	9.95

VOLTAGE DELTA RANGE TABLE

VOLTAGE	08355	00480	08748	08921	08589	08872	08584	07941	08290	08388	MAXIMUM
V01	1.767	0.149	1.525	2.062	0.556	1.517	2.885	0.929	1.028	1.045	2.885
V03	1.767	0.149	1.525	2.062	0.556	1.517	2.904	0.929	1.028	1.045	2.904
V05	1.456	0.279	1.369	1.927	0.556	1.342	2.527	0.831	0.872	0.790	2.527
V07	1.456	0.279	1.389	1.927	0.517	1.342	2.488	0.831	0.872	0.751	2.488
V09	1.326	0.166	1.033	1.481	0.415	1.055	2.131	0.661	0.833	0.727	2.131
V011	1.318	0.364	1.009	1.481	0.415	1.055	2.124	0.653	0.817	0.727	2.124
V013	0.316	0.100	0.416	0.765	0.155	0.390	1.072	0.266	0.961	0.993	1.072
V015	0.631	0.100	0.416	0.732	0.155	0.390	1.072	0.266	0.933	0.972	1.072
V017	0.176	0.363	0.116	0.460	0.186	0.793	0.558	0.218	2.370	0.242	2.370
V019	0.376	0.363	0.416	0.460	0.186	0.793	0.558	0.218	2.240	0.242	2.240
V0R	1.100	0.110	0.699	1.250	0.359	0.964	1.816	0.596	0.802	0.593	1.816

RESISTANCES MAXIMUM RANGE TABLE

PINS	21183	11650	12034	11789	11861	11836	MAXIMIM
4-2	1.8782	1.8876	1.8774	1.8774	1.8811	1.8786	1.8876
2-1	544.30	546.80	544.30	544.11	544.90	544.90	546.80
1-30	267.70	270.80	267.70	267.30	267.60	267.60	270.80
30-26	47.600	47.700	47.700	47.600	47.800	47.700	47.800
7-8	148.90	149.82	148.70	148.90	148.90	148.60	149.82
28-27	1.7772	1.7735	1.7828	1.7788	1.7832	1.7829	1.7832
17-18	12.524	12.495	12.476	12.468	12.539	12.517	12.539
18-19	6.5049	6.5002	6.4837	6.4866	6.5117	6.5055	6.5117
19-20	3.0136	3.0035	3.0104	3.0000	3.0215	3.0080	3.0215
20-21	498.70	498.26	497.50	497.20	499.60	498.40	499.60
21/22	494.46	492.76	495.78	494.70	497.18	495.00	497.18
24/21	2.5093	2.5053	2.5053	2.5021	2.5153	2.5108	2.5153
24/23	3.6533	3.6489	3.6622	3.6573	3.6644	3.6573	3.6644
16/25	1.1930	1.1894	1.1963	1.1947	1.1977	1.1960	1.1977
3/24	199.90	199.40	200.60	200.50	201.66	200.50	201.66

RESISTANCES MINIMUM RANGE TABLE

PINS	21183	11650	12034	11789	11861	11836	MINIMUM
4-2	1.8779	1.8777	1.8770	1.8771	1.8800	1.8778	1.8770
2-1	544.13	540.00	544.13	544.05	544.80	544.80	540.00
1-30	267.55	268.80	267.47	267.25	267.53	267.50	267.25
30-26	47.357	47.000	47.500	47.497	47.630	47.500	47.000
7-8	148.71	148.78	148.56	148.74	148.76	148.45	148.45
28-27	1.7771	1.7500	1.7822	1.7784	1.7826	1.7823	1.7500
17-18	12.522	12.400	12.474	12.466	12.538	12.516	12.400
18-19	6.5010	6.4570	6.4830	6.4860	6.5110	6.5030	6.4570
19-20	3.0130	3.0000	3.0090	2.9990	3.0210	3.0070	2.9990
20-21	498.56	494.40	497.45	496.97	499.36	498.38	494.40
21/22	493.80	488.80	494.94	494.59	495.00	494.93	488.80
24/21	2.5090	2.5000	2.5040	2.5020	2.5140	2.5100	2.5000
24/23	3.6520	3.6480	3.6610	3.6560	3.6630	3.6560	3.6480
16/25	1.1924	1.1280	1.1960	1.1943	1.1974	1.1956	1.1280
3/24	199.72	198.00	200.42	200.22	201.04	200.31	198.00

RESISTANCES DELTA RANGE TABLE

PINS	21183	11650	12034	11789	11861	11836	MAXIMIM
4-2	0.02	0.52	0.02	0.02	0.06	0.04	0.52
2-1	0.03	1.24	0.03	0.01	0.02	0.02	1.24
1-30	0.06	0.74	0.09	0.02	0.03	0.04	0.74
30-26	0.51	1.47	0.42	0.22	0.36	0.42	1.47
7-8	0.13	0.69	0.09	0.11	0.09	0.10	0.69
28-27	0.01	1.33	0.03	0.02	0.03	0.03	1.33
17-18	0.02	0.76	0.02	0.02	0.01	0.01	0.76
18-19	0.06	0.66	0.01	0.01	0.01	0.04	0.66
19-20	0.02	0.12	0.05	0.03	0.02	0.03	0.12
20-21	0.03	0.77	0.01	0.05	0.05	0.00	0.77
21/22	0.13	0.80	0.17	0.07	0.44	0.01	0.80
24/21	0.01	0.21	0.05	0.00	0.05	0.03	0.21
24/23	0.04	0.02	0.03	0.04	0.04	0.04	0.04
16/25	0.05	5.16	0.03	0.03	0.03	0.03	5.16
3/24	0.09	0.70	0.09	0.14	0.31	0.09	0.70

RESISTNACES MAXIMUM RANGE TABLE

PINS	08355	00480	08748	08921	08589	08872	08584	07941	08290	08388	MAXIMUM
4-2	1.8881	1.8828	1.8772	1.8799	1.8803	1.8818	1.8779	1.9122	1.8901	1.8804	1.9122
2-1	545.40	546.80	545.30	545.40	545.60	545.90	545.60	553.60	545.20	545.00	553.60
1-30	267.90	268.10	268.00	268.20	268.50	268.50	269.60	272.10	268.10	268.20	272.10
30-26	47.700	47.700	48.000	48.000	47.700	48.800	48.200	47.600	47.600	47.700	48.800
7-8	149.10	149.00	149.00	149.10	149.10	149.40	149.30	153.40	0.00	149.00	153.40
28-27	1.7820	1.7882	1.7829	1.7839	1.7803	1.7885	1.7851	1.7790	1.7802	1.7783	1.7885
17-18	12.512	12.640	12.546	12.511	12.519	12.522	12.534	12.458	12.566	12.540	12.640
18-19	6.5064	6.5040	6.4992	6.5030	6.4984	6.5092	6.4936	6.4933	6.5055	6.5172	6.5172
19-20	2.9986	3.0364	3.0235	3.0115	3.0060	3.0070	3.0104	3.0030	3.0206	3.0118	3.0364
20-21	502.10	506.50	503.50	505.20	502.60	505.20	502.40	501.60	506.00	502.70	506.50
21/22	494.80	496.30	495.80	495.70	494.90	496.20	495.90	494.10	494.60	494.90	496.30
24/21	2.5073	2.5101	2.5783	2.4990	2.4996	2.5070	2.5670	2.4912	2.5132	2.5071	2.5783
24/23	3.6582	3.6838	3.6630	3.6680	3.6560	3.6755	3.6650	3.6540	3.6570	3.6520	3.6838
16/25	1.1961	1.2029	1.2048	1.1979	1.2066	1.2001	1.1986	1.1944	1.2082	1.1962	1.2082
3/24	200.80	200.20	200.60	201.30	200.70	203.00	201.30	200.40	200.30	200.60	203.00

RESISTANCES MINIMUM RANGE TABLE

PINS	08355	00480	08748	08921	08589	08872	08584	07941	08290	08388	MINIMUM
4-2	1.8810	1.8825	1.8767	1.8793	1.8799	1.8812	1.8770	1.9119	1.8896	1.8801	1.8767
2-1	545.30	546.60	545.10	544.90	545.20	545.50	545.00	553.20	544.90	544.80	544.80
1-30	267.80	267.89	267.79	267.90	268.04	268.10	268.94	271.78	267.80	267.97	267.79
30-26	47.495	47.421	47.543	47.601	47.445	48.197	47.596	47.408	47.332	47.485	47.332
7-8	148.90	148.76	148.80	148.67	148.70	148.80	148.74	153.08	0.00	148.75	0.0000
28-27	1.7816	1.7879	1.7824	1.7831	1.7796	1.7851	1.7843	1.7783	1.7787	1.7778	1.7778
17-18	12.511	12.637	12.544	12.509	12.517	12.520	12.532	12.456	12.565	12.538	12.456
18-19	6.5050	6.5020	6.4980	6.5010	6.4970	6.5080	6.4920	6.4920	6.5050	6.5120	6.4920
19-20	2.9980	3.0350	3.0230	3.0100	3.0050	3.0060	3.0090	3.0030	3.0190	3.0110	2.9980
20-21	502.04	506.30	503.40	504.70	502.10	504.80	502.00	501.20	505.78	502.50	501.20
21/22	494.18	495.59	494.80	494.40	493.94	495.28	494.62	493.35	493.89	494.25	493.35
24/21	2.5070	2.5090	2.5780	2.4980	2.4990	2.5060	2.5660	2.4910	2.5128	2.5070	2.4910
24/23	3.6577	3.6830	3.6620	3.6670	3.6550	3.6750	3.6640	3.6530	3.6566	3.6515	3.6515
16/25	1.1956	1.2025	1.2043	1.1973	1.2061	1.1996	1.1982	1.1940	1.2080	1.1959	1.1940
3/24	200.58	199.40	200.35	200.90	200.40	202.49	201.07	200.09	200.11	200.30	199.40

RESISTANCES DELTA RANGE TABLE

PINS	08355	00480	08748	08921	08589	08872	08584	07941	08290	08388	MAXIMUM
4-2	0.38	0.02	0.03	0.03	0.02	0.03	0.05	0.02	0.03	0.02	0.38
2-1	0.02	0.04	0.04	0.09	0.07	0.07	0.11	0.07	0.06	0.04	0.11
1-30	0.04	0.08	0.08	0.11	0.17	0.15	0.24	0.12	0.11	0.09	0.24
30-26	0.43	0.58	0.95	0.83	0.53	1.24	1.25	0.40	0.56	0.45	1.25
7-8	0.13	0.16	0.13	0.29	0.27	0.40	0.38	0.21	#DIV/0!	0.17	#DIV/0!
28-27	0.02	0.02	0.03	0.04	0.04	0.19	0.04	0.04	0.08	0.03	0.19
17-18	0.01	0.02	0.02	0.02	0.02	0.02	0.02	0.02	0.01	0.02	0.02
18-19	0.02	0.03	0.02	0.03	0.02	0.02	0.02	0.02	0.01	0.08	0.08
19-20	0.02	0.05	0.02	0.05	0.03	0.03	0.05	0.00	0.05	0.03	0.05
20-21	0.01	0.04	0.02	0.10	0.10	0.08	0.08	0.08	0.04	0.04	0.10
21/22	0.13	0.14	0.20	0.26	0.19	0.19	0.26	0.15	0.14	0.13	0.26
24/21	0.01	0.04	0.01	0.04	0.02	0.04	0.04	0.01	0.02	0.00	0.04
24/23	0.01	0.02	0.03	0.03	0.03	0.01	0.03	0.03	0.01	0.01	0.03
16/25	0.04	0.03	0.04	0.05	0.04	0.04	0.03	0.03	0.02	0.03	0.05
3/24	0.11	0.40	0.12	0.20	0.15	0.25	0.11	0.15	0.09	0.15	0.40

LEAKAGE CURRENTS MAXIMUM RANGE TABLE

PINS	21183	11650	12034	11789	11861	11836	MAXIMUM
26-24	1.0E-09	1.0E-09	8.0E-10	8.0E-10	9.0E-10	8.0E-10	1.00E-09
4-5	7.2E-09	1.0E-08	7.5E-09	6.2E-09	8.2E-09	5.8E-09	1.00E-08
28-6	7.8E-09	8.6E-09	8.9E-09	8.3E-09	7.2E-09	6.4E-09	8.90E-09
28-29	0.0E+00	1.0E-10	0.0E+00	1.0E-10	2.0E-10	0.0E+00	2.00E-10
14-10	2.1E-03	1.8E-06	1.9E-06	8.5E-06	5.9E-07	8.2E-06	2.10E-03
10-7	3.0E-10	4.0E-10	1.7E-08	2.0E-10	2.0E-10	2.0E-10	1.70E-08
14-7	1.5E-05	4.0E-08	3.5E-08	5.4E-08	2.4E-08	1.0E-07	1.50E-05
4-7	8.2E-07	2.0E-08	1.8E-08	1.8E-08	1.7E-08	2.6E-08	8.20E-07
4-12	3.1E-09	1.0E-09	2.0E-09	1.0E-10	2.5E-09	1.0E-10	3.10E-09
12-7	1.7E-05	3.2E-08	2.6E-08	6.5E-08	2.4E-08	1.0E-07	1.65E-05

LEAKAGE CURRENTS MINIMUM RANGE TABLE

PINS	21183	11650	12034	11789	11861	11836	MINIMUM
26-24	2.0E-10	2.0E-10	2.0E-10	2.0E-10	0.0E+00	0.0E+00	0.0E+00
4-5	6.2E-09	7.5E-09	6.9E-09	6.0E-09	7.8E-09	5.1E-09	5.1E-09
28-6	6.0E-09	6.5E-09	7.6E-09	7.4E-09	6.9E-09	6.0E-09	6.0E-09
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	1.0E-10	0.0E+00	0.0E+00
14-10	4.9E-05	9.2E-07	4.0E-08	2.1E-06	4.6E-07	1.6E-09	1.6E-09
10-7	0.0E+00	1.0E-10	1.0E-10	1.0E-10	1.0E-10	0.0E+00	0.0E+00
14-7	3.9E-07	2.4E-08	2.2E-08	2.3E-08	1.9E-08	3.0E-08	1.9E-08
4-7	4.0E-08	4.0E-10	4.0E-10	3.0E-10	5.0E-10	4.0E-10	3.0E-10
4-12	0.0E+00	5.0E-10	1.1E-09	0.0E+00	2.0E-09	0.0E+00	0.0E+00
12-7	8.2E-06	1.0E-09	6.8E-09	2.2E-08	5.9E-09	6.8E-08	1.0E-09

LEAKAGE CURRENTS DELTA RANGE TABLE

PINS	21183	11650	12034	11789	11861	11836	MAXIMUM
26-24	8.0E-10	8.0E-10	6.0E-10	6.0E-10	9.0E-10	8.0E-10	9.0E-10
4-5	1.0E-09	2.5E-09	6.0E-10	2.0E-10	4.0E-10	7.0E-10	2.5E-09
28-6	1.8E-09	2.1E-09	1.3E-09	9.0E-10	3.0E-10	4.0E-10	2.1E-09
28-29	0.0E+00	1.0E-10	0.0E+00	1.0E-10	1.0E-10	0.0E+00	1.0E-10
14-10	2.1E-03	8.8E-07	1.8E-06	6.4E-06	1.3E-07	8.2E-06	2.1E-03
10-7	3.0E-10	3.0E-10	1.7E-08	1.0E-10	1.0E-10	2.0E-10	1.7E-08
14-7	1.5E-05	1.6E-08	1.3E-08	3.1E-08	4.8E-09	7.2E-08	1.5E-05
4-7	7.8E-07	2.0E-08	1.8E-08	1.8E-08	1.7E-08	2.6E-08	7.8E-07
4-12	3.1E-09	5.0E-10	9.0E-10	1.0E-10	5.0E-10	1.0E-10	3.1E-09
12-7	8.3E-06	3.1E-08	1.9E-08	4.3E-08	1.8E-08	3.6E-08	8.3E-06

LEAKAGE CURRENT MAXIMUM RANGE TABLE

PINS	08355	00480	08748	08921	08589	08872	08584	07941	08290	08388	MAXIMUM
26-24	6.0E-10	1.5E-09	5.0E-10	9.0E-09	8.0E-10	2.4E-09	6.0E-10	1.2E-09	6.0E-10	1.0E-09	9.0E-09
4-5	1.3E-08	1.5E-09	7.0E-09	6.5E-09	8.9E-09	1.5E-09	7.2E-09	7.0E-09	1.2E-08	7.1E-09	1.3E-08
28-6	1.2E-08	7.2E-08	1.3E-08	7.2E-09	1.0E-08	1.6E-09	7.4E-09	1.2E-08	1.3E-08	1.2E-08	7.2E-08
28-29	0.0E+00	2.0E-10	0.0E+00	2.0E-10	0.0E+00	4.0E-10	0.0E+00	6.0E-10	0.0E+00	0.0E+00	6.0E-10
14-10	3.0E-08	8.2E-06	1.2E-03	2.8E-04	4.6E-06	1.8E-04	4.1E-06	4.4E-06	2.5E-06	3.1E-06	1.2E-03
10-7	8.6E-08	5.0E-10	2.0E-10	1.2E-09	2.0E-10	2.0E-10	8.0E-10	4.0E-10	5.0E-10	3.0E-10	8.6E-08
14-7	3.0E-08	3.0E-08	5.2E-06	1.0E-06	2.8E-08	7.0E-07	6.2E-08	2.5E-08	2.5E-08	2.8E-08	5.2E-06
4-7	2.3E-08	2.5E-08	6.1E-09	2.5E-08	2.0E-08	2.5E-08	5.2E-08	2.1E-08	2.2E-08	2.1E-08	5.2E-08
4-12	2.0E-09	2.5E-09	3.0E-09	2.8E-09	3.0E-09	2.2E-09	1.6E-08	2.5E-09	3.2E-09	3.0E-09	1.6E-08
12-7	4.5E-07	4.5E-07	2.6E-07	1.0E-06	4.4E-07	7.9E-07	4.2E-07	3.1E-07	2.7E-07	2.4E-07	1.0E-06

LEAKAGE CURRENT MINIMUM RANGE TABLE

PINS	08355	00480	08748	08921	08589	08872	08584	07941	08290	08388	MINIMUM
26-24	0.0E+00	1.2E-09	0.0E+00	2.5E-09	0.0E+00	2.0E-09	1.0E-10	8.0E-10	0.0E+00	2.0E-10	0.0E+00
4-5	1.0E-08	4.0E-10	6.0E-09	5.8E-09	8.0E-09	1.2E-09	6.0E-09	6.0E-09	1.0E-08	6.5E-09	4.0E-10
28-6	9.5E-09	1.2E-09	7.8E-09	6.2E-09	5.8E-09	8.0E-10	6.0E-09	7.5E-09	1.0E-08	7.4E-09	8.0E-10
28-29	0.0E+00	0.0E+00	0.0E+00	0.0E+00	0.0E+00	4.0E-10	0.0E+00	4.0E-10	0.0E+00	0.0E+00	0.0E+00
14-10	2.2E-08	4.2E-06	5.0E-04	2.8E-06	2.3E-06	2.7E-06	2.5E-06	3.3E-06	2.2E-06	2.2E-06	2.2E-08
10-7	2.5E-08	1.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10	2.0E-10	1.0E-10	1.0E-10	1.0E-10	1.0E-10
14-7	2.0E-08	2.5E-08	2.3E-06	2.2E-08	1.7E-08	2.3E-08	4.2E-08	2.0E-08	9.2E-09	7.1E-09	7.1E-09
4-7	5.0E-09	4.0E-09	4.1E-09	5.8E-09	5.1E-09	5.0E-09	5.4E-09	4.8E-09	4.8E-09	1.6E-09	1.6E-09
4-12	1.0E-10	4.0E-10	6.0E-10	8.0E-10	6.0E-10	2.0E-10	4.0E-10	5.0E-10	1.0E-09	1.0E-09	1.0E-10
12-7	3.0E-08	3.0E-08	5.1E-09	4.8E-08	2.8E-08	6.8E-07	6.2E-08	2.5E-08	2.5E-08	2.9E-08	5.1E-09

LEAKAGE CURRENT DELTA TABLE

PINS	08355	00480	08748	08921	08589	08872	08584	07941	08290	08388	MAXIMUM
26-24	3.0E-10	5.0E-10	6.5E-09	8.0E-10	8.0E-10	4.0E-10	5.0E-10	4.0E-10	6.0E-10	8.0E-10	6.5E-09
4-5	1.1E-09	1.0E-09	7.0E-10	9.0E-10	9.0E-10	3.0E-10	1.2E-09	1.0E-09	2.4E-09	6.0E-10	2.4E-09
28-6	7.1E-08	5.2E-09	1.0E-09	4.5E-09	4.5E-09	8.0E-10	1.4E-09	4.4E-09	2.5E-09	4.4E-09	7.1E-08
28-29	2.0E-10	0.0E+00	2.0E-10	0.0E+00	0.0E+00	0.0E+00	0.0E+00	2.0E-10	0.0E+00	0.0E+00	2.0E-10
14-10	4.0E-06	7.0E-04	2.7E-04	2.4E-06	2.4E-06	1.7E-04	1.6E-06	1.1E-06	3.0E-07	9.0E-07	7.0E-04
10-7	4.0E-10	1.0E-10	1.1E-09	1.0E-10	1.0E-10	1.0E-10	6.0E-10	3.0E-10	4.0E-10	2.0E-10	1.1E-09
14-7	5.0E-09	2.9E-06	9.8E-07	1.1E-08	1.1E-08	6.8E-07	2.0E-08	5.0E-09	1.6E-08	2.1E-08	2.9E-06
4-7	2.1E-08	2.0E-09	1.9E-08	1.5E-08	1.5E-08	2.0E-08	4.7E-08	1.6E-08	1.7E-08	1.9E-08	4.7E-08
4-12	2.1E-09	2.4E-09	2.0E-09	2.4E-09	2.4E-09	2.0E-09	1.6E-08	2.0E-09	2.2E-09	2.0E-09	1.6E-08
12-7	4.2E-07	2.5E-07	9.5E-07	4.1E-07	4.1E-07	1.1E-07	3.6E-07	2.9E-07	2.5E-07	2.1E-07	9.5E-07

APPENDIX R

COMBINED ENVIRONMENTS RELIABILITY TEST (CERT) PLAN

ELECTRONICS RELIABILITY FRACTURE MECHANICS

Contract No. F33615-87-C3403

Purchase Request No. FY1456-87-02048
Project No. 2978

CLIN 0001, CDRL Sequence No. 21

ENVIRONMENTAL DESIGN CRITERIA AND TEST PLAN

Final Submittal
May 1990

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TABLE OF CONTENTS

1.0 INTRODUCTION

This Environmental Design Criteria and Test Plan (EDCTP) (CDRL Sequence No. 21) for the "Electronics Reliability Fracture Mechanics" program (Contract No. F33615-87-C-3403) defines the specific environmental design parameters and requirements for the Shop Replaceable Units (SRUs), and establishes detailed plans and procedures for the Combined Environments Reliability Test (CERT) (Task XI of the program): Environmental conditions of steady high temperature and thermal cycling (described in the companion Life Cycle Environmental Profile Plan [CDRL Sequence No. 20]) will be imposed on the energized assemblies until a failure occurs. The test will be accelerated by using higher temperatures than the SRUs normally encounter in the aircraft.

In the event no failures are precipitated due to thermal exposure, a backup test that will vibrate the electronic assemblies at room temperature with power on is planned. The purpose of the short duration sine wave, one-axis vibration would be to investigate the possibility of loose particles inside the electronic packages causing a short circuit. Details of this backup test are described in the final submittal of the companion Life Cycle Environmental Profile Plan (CDRL Sequence No. 20), May 1990.

2.0 BACKGROUND

The draft test plan was formulated in 1988 in compliance with Section 4.5 (Task V) of the Statement of Work (SOW) (Reference 1) and DOD Data Item Description DI-R-7125. Due to program redirection prompted by the results of failure analyses of SRUs that have failed in service, the SOW was modified in 1989. The CERT changed from a mission profile test with simultaneously applied thermal cycling and vibration to an accelerated test without vibration. Details of this redirection are described in the final submittal of the companion Life Cycle Environmental Profile Plan (CDRL Sequence No. 20).

This final submittal of the EDCTP consists of the following revisions of the draft plan:

- It revises the test setup and sequence per the revision of the environmental profiles.

- It answers the questions on the draft plan asked by the Air Force (Reference 1). Two of the five questions, involving vibration, are no longer relevant. The other three - "b", "c", and "e" - are answered herein.

The Shop Replaceable Units (SRUs) to be tested were selected under Task III of the program and are being fabricated under Task IX. In Task XI, thermal stressing of these specially built SRUs will be performed to determine their Failure Free Operating Period (FFOP). The FFOPs established by the test will be compared with the FFOP predictions of Task X which are mathematically derived. In this manner, the life prediction models of electronic assemblies developed under Task VI will be evaluated.

3.0 DESCRIPTION OF TEST ITEMS AND SAMPLE SIZE

The items to be tested will be two serial numbers each of a digital SRU and an analog SRU from the Hughes AN/APG-63 Radar for the F-15 aircraft. They are utilized in the radar's Programmable Signal Processor Line Replaceable Unit (LRU) (3137042) and are identified as follows:

SRU	Assy. Number	Sample Size
Timing and Control(Digital)	3562102	2
Linear Regulator(Analog)	3569800	2

Both module types incorporate a "flow-through" design with the heat exchanger an integral part of the module. Photographs of the two SRUs are shown in Appendices A and B.

The Timing and Control module is a 9x5-inch digital module. The basic module package is an assembly of two printed wiring boards (PWBs) mounted back-to-back with a platefin coldplate sandwiched in between which creates a channel through which cooling air flows. The dominant part type is an integrated circuit flatpack. The flatpack leads are formed in a "gull wing" shape and soldered to the surface of the PWB. A flow-under thermal transfer adhesive is applied under the parts.

The Linear Regulator module is a 6x5-inch analog module consisting of a single PWB bonded to a platefin coldplate through which cooling air flows. The major contributors to failures are three hybrid microcircuits and a power transistor.

4.0 DESIGN OF THE TEST

4.1 Objective

The objective of the test is to establish the Failure Free Operating Period (FFOP) of the electronic assemblies when subjected to the environmental stress of steady high temperature and thermal cycling. The high temperature limits of the parts will be used as the basis for formulating the thermal stresses. The failure data obtained from this test will help validate the analytical life prediction models of electronic assemblies developed under Task VI of the program. The operating time or number of cycles for the first failure to manifest itself as an electronic malfunction is the FFOP for that assembly. Testing will continue until each of the four SRUs has experienced electronic malfunction.

4.2 Environmental Test Method of MIL-STD-810D and Exceptions

Test Method 520.0, "Temperature, Humidity, Vibration, Altitude," of MIL-STD-810D will be followed for the test with exceptions. As implied in Section 1.0 of the Statement of Work, the life prediction technique for electronic assemblies shall be demonstrated for the environmental stress of thermal cycling only. Thus, the environmental stresses of vibration, humidity and altitude of MIL-STD-810D will not be considered for the test.

4.3 Environmental Design Parameters and Test Criteria

The SRUs will be subjected to the major environmental stress of temperature during the test. Forced air (supplemental cooling), for a fixed mass flow and varying temperature, will be imposed on the assemblies in the test cycle as specified by the Life Cycle Environmental Profile Plan(LCEPP) (CDRL Sequence No. 20) formulated under Section 4.5 (Task V) of the Statement of Work and DOD Data Item Description DI-R-7124.

4.4 Description of Testing

Varying conditions of temperature will be imposed on the powered SRUs during the test. Thermal stressing of the SRUs will be accomplished by means of channeling cooling air, in parallel through the heat exchangers built into the assemblies, in the same manner as they are cooled in actual deployment. This thermal simulation is realistic since the SRU temperatures are primarily responsive to the supplemental cooling air, not to the ambient temperature.

Cooling air temperature and flowrate to the SRUs will be automatically controlled. The first time any one of the four SRUs experiences an electronic malfunction (FFOP), the test will be stopped and the malfunctioning SRU will be removed from the test fixture for failure analysis. This procedure will be repeated until all four SRU's have malfunctioned.

From time to time, the test will be interrupted to perform visual inspection and/or infrared(IR) thermography and holographic interferometry of the components. IR scanning enables non-contact measurements to be made of true temperatures of the components, and is useful in detecting a variety of flaws in the hardware. A difference in temperature of a component from one cycle to a later cycle at exactly the same time (and environmental conditions) in the two cycles would be an indication that a flaw had developed either internal to the component or in its attachment to the board. Holographic interferometry enables identification of displacements caused by failure processes.

Prior to the test, an airflow calibration for each of the four SRUs will be performed. The calibration will relate flow in pounds per minute to pressure drop in inches of water, a control parameter during the test. Also a thermal survey will be conducted on the assemblies prior to the test.

In addition, before testing begins, the SRUs will be operated at laboratory ambient conditions to record performance data for comparison with data obtained during and after the test. The identification and environmental test history of each assembly will be documented for failure analysis purposes.

5.0 TEST SETUP AND INSTRUMENTATION

5.1 Facility and Environmental Control

The test will be conducted in the Environmental Engineering Laboratory (Building E2) of the Hughes Electro-Optical and Data Systems Group in El Segundo, California. The cooling air to the SRUs in the F-15 aircraft will be simulated. Details of temperature control for the test follow.

Thermal stressing of the SRUs will be accomplished by means of channeling air of a set temperature and flowrate through their built-in heat exchangers in the same manner as they are cooled in actual deployment. Air temperature and flowrate to each of the SRUs under test will be automatically controlled at the set point throughout the test. The facility's Environmental Control and Data Acquisition System will be used to profile the specified air temperature and pressure (flowrate) to an air supply plenum common to the cooling air inlets of the SRUs. The control signal for cooling air supply temperature and flowrate is generated by a controller. The controller receives a set point signal from the profiler. The set point is inputted to the profiler as a straight line segment time history. The profiler provides multiple time synchronized outputs to the controller. The controller compares the control sensor signals with the set point values and generates the control commands.

The modules will be cooled by dry nitrogen gas (although the term "air" is employed herein to conform to standard usage). It is more convenient to use N2 than air in a laboratory test of this type. The N2 supply temperature will be regulated by a portable air conditioning cart. Air metering orifices built into the modules will serve to properly regulate airflow to each individual SRU in the same manner as in actual deployment.

5.2 Installation and Fixturing

A major step in planning this test was establishing how to fixture the SRUs. In the actual 042 unit, there is one 2102 module and one 9800 module. Provision of one or two 042 units for this test would have been prohibitively expensive and not advantageous for obtaining information to attain the program objectives. Instead, a special purpose setup was developed to electrically power, provide coolant air for, and environmentally stress all four modules (the two 2102 modules and the two 9800 modules) at the same time.

The setup described herein was developed by a team consisting of members with expertise in radar operation and electrical testing, environmental testing, structural mechanics, and thermal engineering. It is feasible to implement and is optimum for providing information for the program. The key features of this setup are as follows:

- Both surfaces of each module will be exposed for inspection and/or photography during the test. (Before the test begins, a prediction of the time to failure of the defects on each side of each of the two specially built and inspected 2102 modules will be available.)

- The bottom connectors of the modules can be plugged into and unplugged from the test fixture without interfering with each other.

- The top connectors of the 2102 module are accessible for continuous diagnostic testing.

- The four modules are supplied by a common coolant air plenum, thus simplifying control of the coolant air.

The overall layout of the test setup is shown in Figure 5.2-1. A test fixture supports the four SRUs in card extenders. The card extenders provide the interface for electrical inputs and outputs to/from the SRUs.

The plane of all four SRUs will be vertical to facilitate viewing of the populated boards for the purpose of visual inspection and infrared thermography. A cooling air supply plenum common to the air inlets of the SRUs will be supported by the test fixture.

During the test, the SRUs will be insulated from their surroundings, and from the table on which the fixture is mounted, to prevent heat loss/gain by radiation or convection which would affect SRU temperatures in a way not representative of actual aircraft operation. The insulation will be readily removable for top-side access to each SRU.

5.3 Instrumentation, Calibration, and Accuracies

5.3.1 Instrumentation

Control and response instrumentation for the test will consist primarily of thermocouples. A pressure transducer will be utilized to control and monitor the coolant air supply plenum pressure. Two thermocouples will be located in the air supply plenum: one to control and the other to monitor the cooling air temperature.

No more than 30 thermocouples will be employed to measure the case temperature response of selected components on the SRUs. The thermocouple locations will be selected with the aid of the thermal analysis of the modules (References 2 and 3). The thermocouples will be bonded to the test items with standard techniques used in environmental testing.

5.3.2 Calibration

Prior to the start of testing, an air (N2) flow calibration will be performed. The calibration will relate flow in pounds per minute to the pressure drop (air supply plenum pressure) for each of the four SRUs. A minimum of five data points will be acquired for the calibration. The highest and lowest pressure drops will bracket the range of SRU inlet plenum pressures supplied by F-15 aircraft throughout the profiles in the test.

5.3.3 Accuracies

The accuracies of the measurement systems used to control or monitor the environmental parameters shall be as follows:

Cooling air supply plenum pressure: ±2% of reading
Cooling air supply temperature: ±2°F (±1°C)

5.4 Electronic Support Equipment to Function Test Items

The Test Station will perform the complete manufacturing functional tests on the digital and analog modules. It will also monitor the modules for functional failure during the environmental tests. A block diagram of the Test Station is presented as Figure 5.4-1.

5.4.1 Requirements

The 3562102 Timing and Control module is a digital module. For complete functional testing, it requires 116 input channels and 296 output channels, at TTL signal levels. Its power requirements are +5.1 volts at 11.6 amperes and +12 volts at 0.5 ampere.

The 3569800 Linear Regulator module is a power regulator. Complete functional testing of this module consists of supplying power, loading the outputs, and monitoring the output voltages. Its power requirements are +17 volts at 7 amperes, -17 volts at 2 amperes, and +12 volts at 10 milliamperes. The outputs will be monitored in such a way that current loading effects are accounted for.

The Test Station will perform the complete manufacturing functional tests on the digital and analog modules for periodic endpoint measurements. The complete test of the digital module will employ a special diagnostic connector which is not present during flight. It will monitor both modules for functional failure during environmental stress.

5.4.2 Summation 1032B TestSystem

The Summation 1032B TestSystem is the core of the Test Station. It provides the capability to stimulate and monitor the modules under test. The system we have configured provides 304 digital input and output channels. This is sufficient to provide simultaneous inputs to both digital modules, and to monitor the outputs of one module at a time. The receiver pods will be multiplexed so that the system can alternately monitor each digital module, electronically switching between them.

The 304 digital channels are provided by 19 DSR12 High Speed Memory Module cards, which have a stored pattern depth of 16K vectors. Since the manufacturing test consists of less than 4K vectors, this is more than adequate, and will provide space for additional vectors if needed. The DSR12 cards will each be equipped with a TTL driver and TTL receiver pod. These pods provide the TTL interface to the digital signal pins of the 3562102 modules.

A DMM10 Digital Multimeter card will be used to monitor power and other signals. These signals include the power supply voltages to all modules, and the output voltages of the linear modules. We have selected a CSSCN10 39 Channel Scanner card, to enable the DMM card to measure various points during module test.

The SigmaSeries Model 7523A Industrial Computer, included in the TestSystem, will control functional tests, electrical exercise and monitoring during environmental tests, and module power. All measurements, including functional failure indications, will be recorded on magnetic media, for archive and periodic analysis. In the event of a functional failure or unacceptable power condition, the computer will sound an alarm to remove power from the modules. Since the Summation TestSystem monitors only 304 channels simultaneously and the digital module has 296 outputs, the outputs must be multiplexed. This will be accomplished by using 19 additional receiver pods for the High Speed Memory Modules. The additional pods will be assembled together with the pods included in the TestSystem to make dual-input pods. This will permit the Test Station to monitor each digital module alternately.

5.4.3 Hewlett-Packard Programmable Power Supplies

Seven Hewlett-Packard Programmable Power Supplies are required for the four modules under test:

A model 6621A supply will provide the +12V power for the digital modules. This supply has two outputs, each capable of up to 4A at up to 20V.

Two model 6033A supplies will provide the +5V power for the digital modules. These supplies are capable of supplying up to 30A at voltages up to 6.7V.

Two additional model 6033A supplies will provide the +17V power for the linear modules. In the 20V range, these supplies can provide up to 10A.

An additional model 6621A supply will provide the -17V power for the linear modules.

A model 6624A supply will provide the +12V bias power for the linear modules. This supply has two outputs capable of 2A at up to 20V.

5.4.4 Hewlett-Packard Model 54501D Digitizing Oscilloscope

The Hewlett-Packard Model 54501D digitizing oscilloscope will be used to monitor signals during debug and operation of the Test Station. It will also provide diagnostic capability in the case of apparent functional failures. This oscilloscope will communicate with the computer via the IEEE-488 bus, and can be used for guided diagnostics of the assembled test fixtures.

5.4.5 Equipment Rack

All this equipment will be mounted in a 61-inch double-bay rack. The entire test system will be transportable, so that it can be placed near the environmental chamber or used separately.

5.4.6 Accuracies

The DMM10 Digital Multimeter card is a 4-1/2 digit multimeter with a DC voltage measurement accuracy of $\pm$ (0.01% + 2 counts). It will be used to monitor the output voltages of the linear module, and for redundant monitoring of the supply voltages to all modules.

The DSR11 Model 4410A High Speed Timing Module has a guaranteed pin-to-pin timing skew of less than ± 10.5ns. The data rate is accurate to ± 0.01%.

The Hewlett-Packard programmable power supplies will be used to monitor supply voltages and currents. Their measurement accuracies are:

Model	Voltage	Current
6621A	±(20mV+0.05%)	±(20mA+0.1%)
6624A	±(20mV+0.05%)	±(10mA+0.1%)
6033A	±(6mV+0.07%)	±(25mA+0.3%)

5.5 Protection from ESD

The test items will be handled in accordance with Hughes Standard HPR 15010 (Appendix C) to protect them from electrostatic discharge (ESD).

5.6 Equipment Required from the Government

In order to perform integration, checkout and acceptance testing of the Test Station, the contractor has obtained the loan of the following government property:

Part Number	National Stock Number	Quantity
3562102-5	5841-01-101-3770	2
3569800	5841-01-058-9023	2

The above Government Furnished Property (GFP) loaned to Hughes is serviceable.

6.0 DATA ACQUISITION

6.1 Environmental

Data obtained from the response thermocouples and the pressure transducer are routed to remote scanners that condition the electronic data. The datalogger that receives these signals converts them to temperature or pressure readings and sends them to data storage. When a temperature exceeds a triggering value or range, the datalogger sends an alarm signal.

The data acquisition computer routes the temperature data to remote CRT displays located at the test site. The data are available from the computer CRT, as listings, and/or as multi-plot time histories.

6.2 Functional

The Test Station will record the results of its monitoring functions. For the digital module, this includes periodic measurement of the power supply

voltages and currents, and a record of each functional test. In the event of a functional failure, the vector and output which failed will be identified and recorded. For the linear module, periodic measurements of input and output voltages and currents will be recorded.

All data will be recorded on a fixed disk drive in the 7523A computer. The data will be backed up at least daily on removable media, which will be stored in a separate location.

7.0 TEST PROCEDURE

7.1 Preparation

7.1.1 Perform the flowrate/pressure drop calibration as described in Paragraph 5.3.2.

7.1.2 Mount SRUs in accordance with Figure 5.2-1.

7.1.3 Connect control and response monitor channels into the Environmental Control and Data Acquisition System.

7.1.4 Connect portable air conditioning cart and Test Station.

7.1.5 Verify that the proper thermal profile is in the profiler.

7.1.6 Supply cooling air and confirm that the test items are operational.

7.1.7 Conduct thermal survey (insulation surrounding SRUs).

7.1.8 Perform pre-test performance baseline tests of all four SRUs (insulation surrounding SRUs).

7.2 Environmental Mission Profile Cycling

7.2.1 Start test cycle (insulation surrounding SRUs).

7.2.2 Monitor test item performance (Test Station) and record Environmental Control and Data Acquisition System data throughout environmental exposure.

7.2.3 Continue test until an SRU malfunction occurs.

7.2.4 Document malfunction.

7.2.5 Remove malfunctioning SRU from test fixture for failure analysis.

7.2.6 Repeat Paragraphs 7.2.1 through 7.2.5 three times.

7.3 Test Items Operation

The Test Station (Section 5.4) will operate and monitor the four modules during environmental stress. The operation of the Test Station will be extremely simple, and primarily unattended.

In each of the following steps, when operation interaction is involved, the Test Station will prompt for it. In some cases, the Station will require the operator to type a response before proceeding.

7.3.1 Initial Setup

These steps are necessary at the beginning of the environmental test, and any time the Test Station has been disconnected from the environmental control system or the modules under test.

7.3.1.1 Interface to Environmental Control System

The Test Station will prompt the operator to connect the signal lines from the environmental control system. These include the Failure Alarm, Stop Test, and No Flow signals. When these are connected, the operator will enter a response to the Station, and the Station will test all signals. This will require another operator to attend the environmental control system to ensure that the signals are properly sent and received. The Test Station screen will indicate what signal is being tested, and the verification requirements.

7.3.1.2 Electrical Connection to Module

The operator will connect the power and signal lines from the Test Station to the modules under test, including the diagnostic connectors to the digital modules. After checking for air flow, the Test Station will apply power to the modules. If the power supply currents and voltages are in acceptable ranges, the Test Station will proceed with a functional test of the modules. If this test passes, the setup is complete.

7.3.1.3 Setup Failures

A failure at any point during the setup procedure must be corrected before beginning the environmental tests. Troubleshooting aids will be included in the test software. These aids may be invoked by the operator at any time except during environmental stress.

7.3.2 Perform Electrical Tests

During environmental stress, the Test Station will continually test the modules.

7.3.2.1 Digital Module

Functional test of the digital modules consists of applying a series of logic states to the inputs, reading the resulting states of the outputs, and comparing the output states to a table of expected states. If they match, the module is functioning correctly. If they are different, the Test Station will declare a failure, sound an alarm, and store diagnostic information for analysis.

The Test Station will operate the 3562102 modules according to Test Specification 31325-172 (Appendix D), with some exceptions. This specifies DC power to the module at +5.1 volts and +12 V. The input signal sources are at standard TTL levels, and the output loads are standard TTL loads. There are

four test vector sets of approximately 800 vectors each. The test equipment called out in the specification is a Hewlett-Packard DTS-70 Digital Test System.

The Summation test system described in Paragraph 5.4.2 will provide the digital stimulus. This system is capable of providing test vectors to the unit under test (UUT) at a much higher rate than that of the DTS-70. The Summation 1032B can operate the UUT at 20MHz, compared with the approximately 1kHz rate of the DTS-70.

The module will be operated at the highest practical speed, limited mainly by the signal quality available at the test fixture due to cable length.

7.3.2.2 Linear Regulator Module

For the Linear Regulator modules, the test consists of monitoring the output voltages per Table IV of Test Specification 31325-184 (Appendix E). Any output voltage that does not meet the requirements of that table indicates a failure, resulting in an alarm and module shutdown.

7.3.2.3 General

The Test Station will also monitor the modules for electrical conditions out of the specified operations range.

7.3.3 Interrupts

The environmental system will be able to stop the electrical tests at any time, by signaling the Test Station.

7.4 Tests to Identify Electronic Malfunction

The Test Station will monitor the test items for malfunction during environmental stress. In the event of a malfunction of any module, the Test Station will record the event, remove signals and power from that module and notify the environmental control system that a failure has occurred. The environmental control system will then halt the test and issue an audible alarm. The malfunction reported by the Test Station will be verified manually.

7.4.1 Digital Module

The test system will perform the full manufacturing test on the digital modules during environmental stress.

In addition, the Test Station will monitor the current and voltage supplied to the module. If the current exceeds the limits specified in TS 31325-172 (Appendix D), the Station will treat this as a failure.

7.4.2 Linear Regulator Module

The test station will operate the 3569800 modules according to TS 31325-184 (Appendix E). The test conditions will alternate between Condition 1 and Condition 2 in Table III. The Test Station will monitor the module outputs

for compliance with table IV. If any output does not meet the requirements of Table IV, this will be considered a malfunction. In addition, the power inputs will be monitored for excessive current, which will also be considered a malfunction.

8.0 FAILURES

8.1 Failure Criteria

Functional testing of the SRUs to detect malfunction shall be in accordance with Test Specification TS 31325-169 (Reference 4). This test specification applies to the 042 LRU.

During deployment, the criteria used in removal and replacement of the SRUs are those in Technical Order 12P2-2APG63-98-15 (Reference 5).

The failure criteria in TS 31325-172 (Appendix D) and TS 31325-184 (Appendix E) will be applied to the 3562102 and 3569800 modules, respectively, to identify failures during environmental stress. These criteria are more stringent than those in TS 31325-169. Failures which would be identified in deployment will be identified during CERT testing.

8.2 Failure Analysis on Failed Items

Failure analysis on items that fail during the test will be the same as for the failed field SRUs from Warner Robins Air Logistics Center (WR-ALC) analyzed in Task III of the program.

8.3 Experimental Validation of Finite Element Calculations of Localized Static and Dynamic Temperatures and Stresses at Locations Where Failures Occurred During CERT Testing

The four modules will be instrumented during CERT testing to provide localized temperature data which will be used to validate the analytical finite element and finite difference calculations, performed in Task X, of module and device response to the test profiles.

Thermocouples will be mounted at a number of locations on the PWBs and components. The temperatures will be used to validate the module heat transfer and thermal stress models.

It is not necessary to instrument every component on the modules to validate the analytical models. Rather, it is sufficient to instrument one of each component type in order to verify the heat transfer paths as simulated in the models.

9.0 TEST SCHEDULE AND SEQUENCE

The test will start after the four specially built SRUs have been fabricated and inspected, and the Failure Free Operating Period (FFOP) predictions have been made, under Tasks IX and X of the program, respectively. The test is planned for a one-year period. A more precise test schedule must await the FFOP predictions in Task X.

Starting the test with all four SRUs, the environmental stresses will be applied until the first malfunction occurs for any one of the four SRUs. After the failed SRU is removed from the test setup, the test will be continued until a malfunction occurs in one of the remaining three SRUs. Again the failed SRU will be removed. This process is repeated until all four SRUs have malfunctioned, thus ending the test.

10.0 REFERENCES

1. M.B. Bercaw (Air Force Contracting Officer), "Comments on Data Submitted by Hughes Regarding the Environmental Design Criteria and Test Plan", letter to Hughes, 12 December 1988.

2. IDC 722620/1567, "Transient Thermal Analysis of the F-15 PSP Linear Regulator Module" from A.T. Bishop to J.M. Kallis, dated April 4, 1990.

3. IDC 722620/1570, "Transient Thermal Analysis of the F-15 PSP Timing and Control Module" from W.J. Hoskins to J.M. Kallis, dated April 9, 1990.

4. Hughes TS 31325-169, Revision C, "Test Specification Processor, Radar Signal HAC P/N 3173042-100/101/110," 18 September 1984.

5. Hughes TO 12P2-2APG63-98-15, Technical Manual, "Tape Programmed Test Procedures, Digital Radar Signal Processor, MX-10064/APG, 3173042-100/101," 1 April 1982.

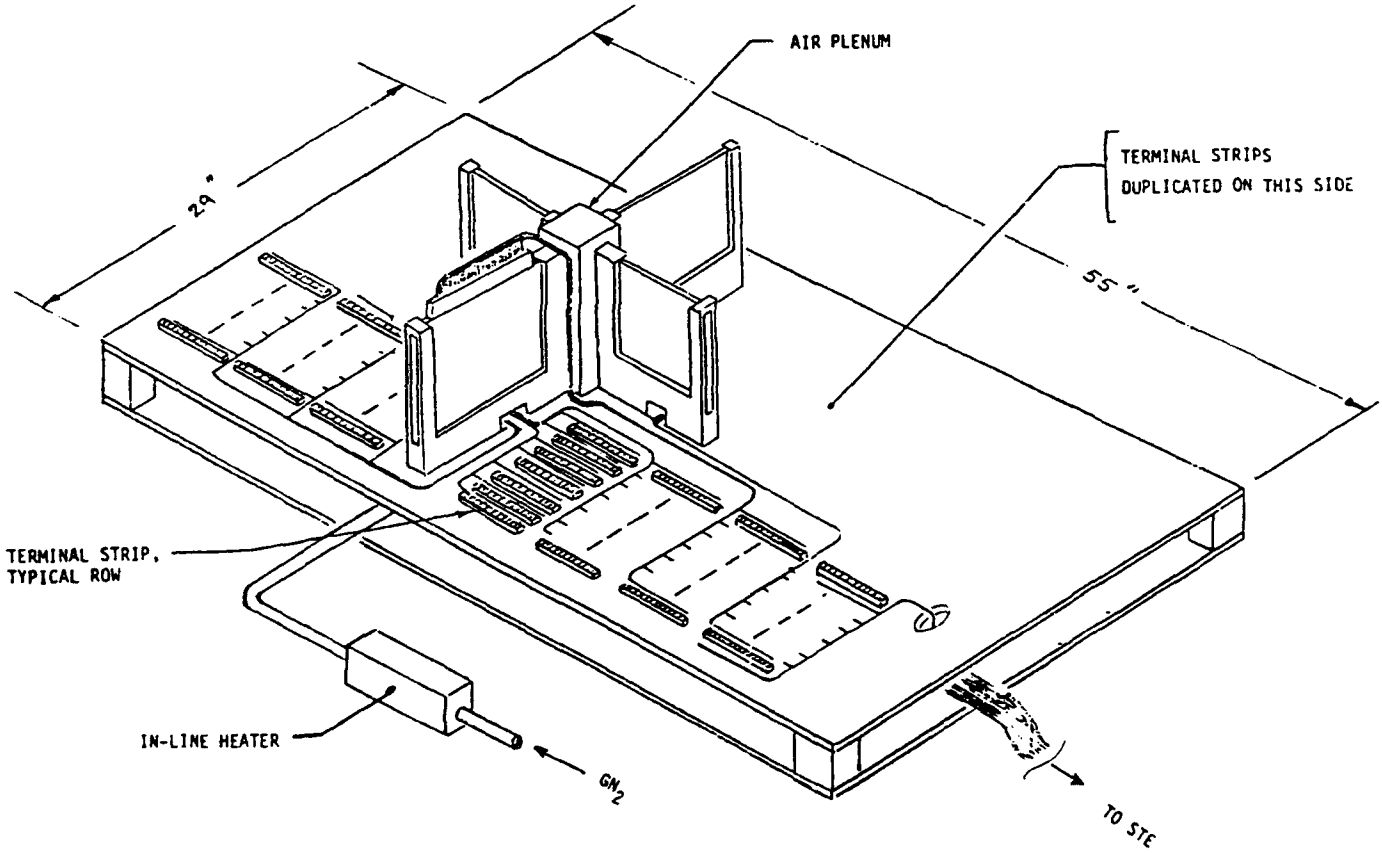

Figure R-5.2.1. Test Setup

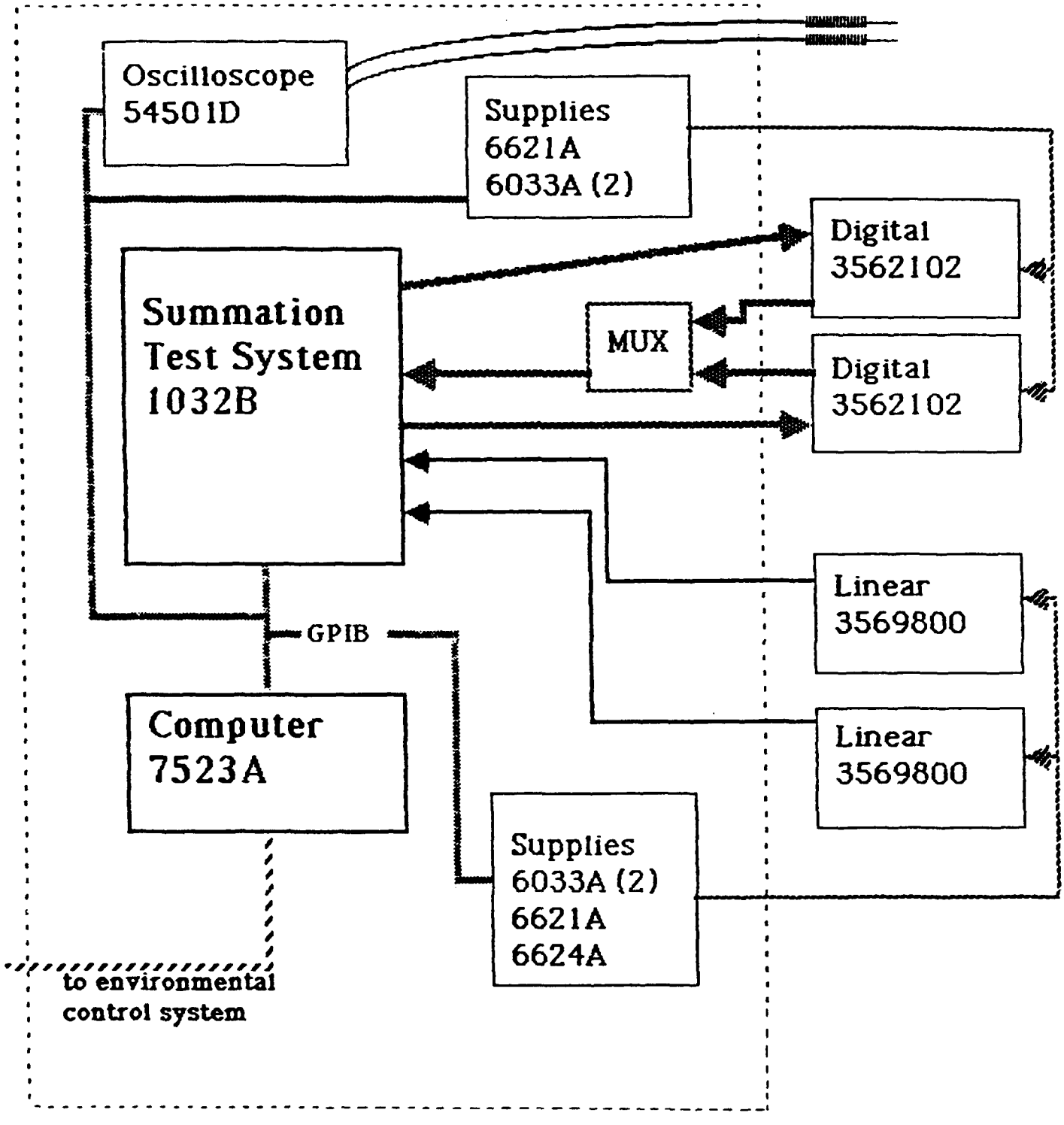

Figure R-5.4-1. Block Diagram of Test Station

APPENDIX E

TEST SPECIFICATION

MODULE ASSEMBLY 12A27

VOLTAGE REGULATOR, LINEAR

HAC PN 3569800

(TS 31325-184)

	TITLE	NUMBER	
	TEST SPECIFICATION MODULE ASSEMBLY 12A27 VOLTAGE REGULATOR, LINEAR HAC PN 3569800	TS31325-184	
		CODE IDENT NO. 82577	
		SH 1 OF 8	A REV LTR

"A" AUTHORIZED BY ECA 459295-71 (3173000 561 and UP)

ENTIRELY RETYPED TO CORRECT FORMAT, ADD TEST OMISSIONS AND INCORPORATE TEST REQUIREMENTS FOR ADDED VOLTAGE TEST ACCESSES. WAS FOUR PAGES.

M Walker
5751

ENGRG DATA DEPT	RELEASED PRINT			ATTACH
	A REV	78-11-01 REL DATE	REL BY	

REV STATUS	SH	1	2	3	4	5	6	7	8	
OF SHEETS	LTR	A	A	A	A	A	A	A	A	

INITIAL APPROVALS	DATE	REV LTR	DATE	APPROVAL	AUTHORITY
PREPARED	78.09.29	A	78-09-29		SEE ABOVE
CHECKED	78-09-29				
APPROVED	78.09.29				

9002 CC REV. 2-66

TEST SPECIFICATION
MODULE ASSEMBLY 12A27
LINEAR VOLTAGE REGULATOR
HAC PN 3569800

1. SCOPE

1.1 This specification establishes the electrical requirements for acceptance of the Linear Voltage Regulator Module Assembly (12A27), Hughes Aircraft Company (HAC) Part Number (P/N) 3569800.

2. APPLICABLE DOCUMENTS

The following documents of the latest issue in effect form a part of this specification only to the extent specified herein.

Hughes Aircraft Company

3569800	Regulator, Voltage, Linear
3569801	Regulator, Linear Schematic Diagram

3. REQUIREMENTS

3.1 Power. The following power sources shall be provided and applied as directed.

3.1.1 Positive Voltage, Variable. A source capable of supplying a voltage variable from +15 to +20 Vdc at 7 amperes minimum and with a ripple less than 0.5 volts peak-to-peak shall be applied to +17 V input terminals.

3.1.2. Negative Voltage, Variable. A source capable of supplying a voltage variable from -15 to -20 Vdc at 2 amperes minimum and with a ripple less than 0.5 volts peak-to-peak shall be applied to -17 V input terminals.

3.1.3 Positive Voltage Load Bias. A source of +12.0 Vdc $\pm$ 1.0 V with a capacity of 10 milliamps minimum shall be provided for crowbar load bias.

3.2 Cooling. When electrical power is applied to the unit, cooling air shall be provided at a minimum flow rate of 0.2 pounds per minute at an inlet temperature of +30 degrees Celcius maximum.

3.3 Connector Designations. Parallel connections to connector terminals are required. Parallel connections shall be as indicated by Table I.

TABLE I
CONNECTOR PIN ASSIGNMENTS

Function	P1 Terminations
+17 V Input	A14, B14, A15, B15, A16, B16
-17 V Input	A22, B22, A23, B23
±17 V RTN	A6, B6, A17, B17, A30, B30
+12 V Output	A31, B31, B32, B32, A33, B33
-12 V Output	A27, B27
-5.3 V Output	A12, B12
±12 V, -5 V RTN	A11, B11, A20, B20, A34, B34
Module Ident.	A5, B5
Module Ident. RTN	A3, B3
Crowbar Status (081)	A4, B4
Crowbar Status (042)	A2, B2
Module Test Access 1	A21, B21
Module Test Access 2	A1, B1
Module Test Access 3	A18, B18
Module Test Access 4	A19, B19
Module Test Access 5	A37, B37
Module Test Access 6	A9, B9
Module Test Access 7	A8, B8
Module Test Access 8	A25, B25
Module Test Access 9	A38, B38
Module Test Access 10	A36, B36

3.4 Loads. The following loads shall be provided.

3.4.1 Loads, +12 Volts. One of the following loads shall be applied to the +12 V output as directed:

(a) 6 ohms ± 5% 25 watts minimum.

(b) 2 ohms ± 5% 75 watts minimum.

3.4.2 Loads, -12 Volts. One of the following loads shall be applied to the -12 V output as directed:

(a) 24 ohms ±5% 6 watts minimum.

(b) 12 ohms ±5% 12 watts minimum.

3.4.3 Loads, -5.3 Volts. One of the following loads shall be applied to the -5.3 volt output as directed:

(a) 20 ohms $\pm$5% 2 watts minimum.

(b) 10 ohms $\pm$5% 3 watts minimum.

3.4.4 Loads, Crowbar Status. A load of 10 kilohms $\pm$5% 1/4 watts terminated to +12 Vdc per 3.1.3 shall be provided for each of the crowbar status outputs.

3.5 Electrical Verification.

3.5.1 Continuity. With no power or loads connected, the continuity between indicated terminals shall be as specified by Table II.

TABLE II

Continuity Requirements

Terminal		Resistance
+ Probe	- Probe	OHMS
J1 - A1	J1 - B1	< 0.1
A2	B2	< 0.1
A2	B4	> 1 meg
A3	B3	< 0.1
A4	B4	< 0.1
A4	B2	> 1 meg
A5	B5	< 0.1
A5	B3	2610 $\pm$ 1%
A5	B6	> 1 meg
A6	B6	< 0.1
A6	A11	"
A6	B11	"
A6	A17	"
A6	B17	"
A6	A20	"
A6	B20	"
A6	A30	"
A6	B30	"
A6	A34	"
A6	B34	"
A6	B22	> 2.5 K
A6	B25	15k - 20k

TABLE II Continued

Continuity Requirements

Terminal		Resistance
+ Probe	- Probe	OHMS
J1 - A8	J1 - B8	< 0.1
A8	B12	10k ± 10%
A9	B9	< 0.1
A9	B27	10k ± 10%
A12	B12	< 0.1
A14	B14	"
A14	A15	"
A14	B15	"
A14	A16	"
A14	B16	"
A14	B21	365 ± 10%
A14	B6	> 3k
A18	B18	< 0.1
A18	B12	8k - 11k
A19	B19	< 0.1
A21	B21	< 0.1
A22	B22	"
A22	A23	"
A22	B23	"
A25	B25	"
A27	B27	"
A31	B30	> 2k
A31	A32	< 0.1
A31	B32	"
A31	A33	"
A31	B33	"
A31	B36	10k ± 10%
A36	B36	< 0.1
A38	B38	< 0.1
A38	B22	365 ± 10%
A37	B37	< 0.1
A31	B37	10.5k ± 10%

3.5.2 Regulation. With power and loads applied, the respective outputs shall respond as specified per Table IV for each test condition of Table III.

TABLE III

Module Test Condition

Test	Input		Loads	
Condition	Input Term (1)	Requirement	Output Term (2)	Requirement
1	+17	3.1.1 at +16±0.5V	+12V	3.4.1a
	-17	3.1.2 at -16±0.5V	-12V	3.4.2a
			-5.3V	3.4.3a
			Crowbar(081)	3.4.4
			Crowbar(042)	3.4.4
2	+17	3.1.1 at 18±0.5V	+12V	3.4.1b
	-17	3.1.2 at -18±0.5V	-12V	3.4.2b
			-5.3V	3.4.3b
			Crowbar(081)	3.4.4
			Crowbar(042)	3.4.4

Note:
(1) Ref Table I, Return to ± 17V RTN
(2) Ref Table I, Return to ± 12V, -5.3V RTN

TABLE IV

Output Requirements

Function (1)	Requirement
+12V	+12.00 ± 0.25 VDC
-12V	-12.00 ± 0.25 VDC
-5.3	-5.300 ± 0.125 VDC
MTA 1	+12.0 ± 1.0 VDC
2	-6.3 ± 0.3 VDC
3	-5.3 ± 0.3 VDC
4	-12.0 ± 2.0 VDC
5	+12.00 ± 0.25 VDC
6	-12.00 ± 0.25 VDC
7	-5.3 ± 0.125 VDC
8	-5.7 ± 0.3 VDC
9	-12.0 ± 1.0 V VDC
10	+12.0 ± 0.25 VDC
Crowbar Status (081)	+12.0 ± 2.0 VDC
Crowbar Status (041)	+12.0 ± 2.0 VDC

TABLE IV Continued

Note:
(1) Ref Table I for terminal assignments. All measurements made with respect to ± 12V - 5.3V RTN.

3.5.3 Short Circuit Protection. With the module operating per Table III, Test Condition 1, the outputs shall respond per Table V as each output is shorted to its respective return. When the short is removed, the output voltage shall return to that specified for that function in Table IV.

TABLE V

Short Circuit Characteristics

Output Function	Short Ckt. Volts	Short Ckt. Current
+ 12 V	0.5 V Max.	2.5 Amp Max.
- 12 V	0.2 V Max.	0.65 Amp. Max.
- 5.3 V	0.1 V Max.	0.31 Amp. Max.

3.5.4 Over Voltage Circuit Response. With the module operating per Table III, Test Condition, 1, the -12 V output shall change to -1.0 ± 1.0 volts, the -5 V output to -0.5 ± 0.5 V, and the crowbar status to 0 ± 1 VDC upon momentary application of each of the following conditions.

(1) Short P1 A37 to P1 A27
(2) Short P1 A18 to P1 A27
(3) Short P1 A25 to P1 A27

4. QUALITY ASSURANCE PROVISIONS

4.1 Product Verification. The module configuration shall comply with drawing 3569800.

4.2 Test Conditions. Unless otherwise specified, all electrical verifications shall be conducted within an ambient temperature of 25 ± 5°C.

4.3 Test Equipment.

4.3.1 Instrument Accuracy. The instruments shall have the accuracy necessary to verify the requirements specified herein. DC voltage measurements shall be made with an instrument with an impedance greater than 1 megohm.

4.3.2 Special Test Adaptor. A test fixture is required to provide cooling air through the module per paragraph 3.2.

4.4 Electrical Test Verification. Verification of electrical requirements shall be conducted per Table VI.

TABLE VI

Electrical Verification Test

Test	Paragraph Requirement	Paragraph Test
Continuity	3.5.1	4.5.1
Regulation	3.5.2	4.5.2
Short Circuit Portection	3.5.3	4.5.3
Over Voltage Circuit Response	3.5.4	4.5.4

4.5 Electrical Verification.

4.5.1 Continuity. Verify that the requirements of paragraph 3.5.1 are met. Instrument test probe polarities must be applied as directed or erroneous readings may occur.

4.5.2 Regulation. Verify that the requirements of paragraph 3.5.2 are met. Test sequence should be conducted only following successful completion of paragraph 4.5.1.

4.5.3 Short Circuit Protection. Verify that the requirements of 3.5.3 are met. Short circuit load condition may be created by shorting normal load with wire or switch.

During test, -12 V output and -5.3 V output shall not be shorted at the same time.

4.5.4 Over Voltage Circuit Response. Verify that the requirements of 3.5.4 are met. Following each test, the module may be returned to the output condition of Table IV by removing and re-applying the -17 V input.

Notes:

(1) Referenced terminals may be identified with corresponding symbols on drawings 3569800 and 3569801.

(2) Momentary shall be equivalent to a time period of less than one second.

(3) Short or short circuit shall be equivalent to connecting the indicated terminals together with a conducting jumper which has an impedance less than 0.1 ohms.

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ENGINEERING ORDER – ~~REVISION NOTICE~~
(SEE EP 1-14 FOR INSTRUCTIONS)

CODE IDENT 88877

DWG/SPEC NUMBER: TS31225-184

DWG/SPEC TITLE: TEST SPECIFICATION MODULE ASSEMBLY 12A27 VOLTAGE REGULATOR LINEAR HAC PN 3569800

☒ EO NO. 99239 SH 1 OF 1

☐ REV NOTICE LTR ____ SH ____ OF ____

CONTROL ITEM NAME: F-15 RADAR SET

SYS/EQPT: AN/APG-63

AUTHORITY: ECA 459295-221 CCP(S): CE

CONTROL ITEM PART NUMBER	CHANGE EFF	CONTROL ITEM PART NUMBER	CHANGE EFF	CONTROL ITEM PART NUMBER	CHANGE EFF
3173000	3172555 5619UH				
(3173042)					

ZONE

DESCRIPTION

PARA 3.5.4

IS: ---- SHALL CHANGE TO -1.5 ± 1.0 VOLTS, ----

WAS: ---- SHALL CHANGE TO -1.0 ± 1.0 VOLTS, ----

DISPOSITION OF ITEMS

N/A

PREPARED BY	ORG CODE	DATE		ORG CODE	DATE
[signature]	27-51-50	79-01-04			
CHECKED BY	**ORG CODE**	**DATE**		**ORG CODE**	**DATE**
[signature]	27-51-40	79-01-04			
APPROVAL	**ORG CODE**	**DATE**	**RELEASED BY**	**ORG CODE**	**DATE**
[signature]	27-51	79-01-04	[signature]	27-11-15	[illegible]

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F1-189 A

ENGINEERING ORDER – ~~REVISION NOTICE~~
(SEE EP 1-14 FOR INSTRUCTIONS)

CODE IDENT 88277

~~SPEC~~ NUMBER: TS 31325-184

~~SPEC~~ TITLE: TEST SPECIFICATION MODULE ASSY 12A27 VOLTAGE REGULATOR LINEAR HAC PN 3569800

☒ EO NO. 25420 SH 1 OF 1

☐ ~~REVISION NOTICE NO~~ ____ SH ____ OF ____

CONTROL ITEM NAME	SYS/EQPT	AUTHORITY
F-15 RADAR	AN/APG 63	ECA 485878 CL II A

CONTROL ITEM PART NUMBER	CHANGE EFF	CONTROL ITEM PART NUMBER	CHANGE EFF	CONTROL ITEM PART NUMBER	CHANGE EFF
3173000	3173000 P701-UP				
(3173042)					

ZONE	DESCRIPTION
SH 5	TABLE II IS: A14 TO B6 ≥ 2.5K WAS: A14 TO B6 > 3K IS: A6 TO B22 ≥ 2.1K WAS: A6 TO B22 > 2.5K

DISPOSITION OF ITEMS: N/A

	ORG CODE	DATE		ORG CODE	DATE
PREPARED BY	27-50	81-06-29			
CHECKED BY	27-50	81-06-29			
APPROVAL	27-51-40	81-06-29	RELEASED BY	27-51-10	81-08-02

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APPENDIX S

CERT ENVIRONMENTAL PROFILE PLAN

ELECTRONICS RELIABILITY FRACTURE MECHANICS

Contract No. F33615-87-C-3403

Purchase Request No. FY1456-87-02048
Project No. 2978

CLIN 0001, CDRL Sequence No. 20

LIFE CYCLE ENVIRONMENTAL PROFILE PLAN
Final Submittal
May 1990

Revised January 1991
Revision Integrated into Plan April 1991

Prepared for:

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1.0 INTRODUCTION

1.1 Overview

This Life Cycle Environmental Profile Plan (CDRL Sequence No. 20) and the companion Environmental Design Criteria and Test Plan (EDCTP) (CDRL Sequence No. 21) for he "Electronics Reliability Fracture Mechanics" program (Contract No. F33615-87-C-3403) define the specific environmental design parameters and requirements and establish detailed plans and procedures for the Combined Environments Reliability Test (CERT). An air flow rate and temperature (described herein) will be imposed on the energized assemblies during the test.

This test plan was formulated in compliance with Section 4.5.1 (Task V) of the Statement of Work (SOW) and DOD Data Item Description DI-R-7124. The Shop Replaceable Units (SRUs) to be tested, which are used in the F-15 aircraft, were selected under Task III and fabricated under Task IX. In Task XI, CERT testing shall be conducted on these specially built SRUs to determine their Failure Free Operating Period (FFOP). The FFOPs established by the test will be compared with the FFOP predictions of Task X which are mathematically derived. In this manner, the life prediction models of electronic assemblies developed under Task VI will be evaluated.

This plan documents 1) the test cycle, 2) the application of the test cycle, and 3)the method used to derive the test cycle.

1.2 Background

1.2.1 Original Statement of Work

When the contract started in 1987, SOW paragraph 4.5.1 stated the following:

> 4.5.1 The contractor shall develop life cycle environmental profiles based upon the deployment use conditions for the SRUs to be CERT tested under Task XI. The life cycle profile shall be developed per MIL-STD-810D paragraph 4.2.2.2 and the Handbook for Avionics/ Electronics Integrity Requirements.

Per this requirement, Hughes collected mission profile data for the Programmable Signal Processor (PSP) Line Replaceable Unit (LRU) of the Hughes APG-63 radar in the F-15 aircraft. Hughes derived a combined environments test cycle, which is a composite of missions occurring during the majority of the hardware deployment life. Each mission has associated environmental stressors dictated by flight and/or climatic conditions. The stressors - random vibration, thermal cycling, and on/off power cycling - are applied simultaneously in a sequence that simulates a mission.

Hughes prepared the draft of this plan in 1988 (Refs. 1 and 2). The Air Force reviewed the draft plan and did not accept it as final. For acceptance, the

AF required three questions as to the acceptability of the derived profiles to be answered (Ref. 3).

1.2.2 Modified Statement of Work

During the period in which the draft plan was being prepared and reviewed, other activities in the ERFM program were indicating that the approach specified in the SOW warranted modification. Failure analysis of failed F-15 PSP modules indicated that the failures were from different environments than expected:

- all from electrical stress and steady high temperature
- none from thermal cycling and vibration.

Furthermore, the thermal/vibration environments are relatively benign:

- electronic part junction temperatures relatively low
    - digital module: below 93°C
    - analog module: below 67°C (44°C for hybrids)
- flight vibration spectral densities in avionics bay benign
    - level flight: below 0.0004 g^2/Hz
    - maneuvering flight: below 0.008 g^2/Hz

An evaluation of these results indicated the following:

- It is unlikely that the first failure in the Combined Environments Reliability Test (CERT) (Task XI) of the four SRUs fabricated in Task IX will be the result of thermal cycling and vibration - the environments in the scope of the ERFM contract.
- It could require an excessively long time for the first failure to occur in the CERT in the simulated F-15 aircraft environment.

Accordingly, it was concluded that a program redirection is warranted to make the life modeling, special fabrication/inspection, and CERT consistent with the observed failures of the APG-63 SRUs (Ref. 4).

These results were presented to and discussed with the AF. A no-cost change to the SOW was agreed upon in 1989. Its key features are as follows:

- expansion of the scope to include environments other than thermal cycling and vibration
- change of the CERT in Task XI to an accelerated test, rather than one duplicating the F-15 life cycle environment

- limitation of the CERT environments to the environments that accelerate the failure mechanisms observed in the failed field APG-63 SRUs.

The modified SOW paragraph 4.5.1 is as follows:

> 4.5.1 The contractor shall develop accelerated environmental profiles for the SRUs to be CERT tested under Task XI. The environments shall be those known to accelerate the failure mechanisms observed in the failure analysis of the SRUs examined in Task III.

This modification made the draft plan (Refs. 1 and 2) irrelevant to ERFM. It also made it unnecessary for Hughes to answer the questions asked by the AF in Ref. 3, because these questions involved simulation of the F-15 environment.

To be certain that the CERT environments include those that accelerate the failure mechanisms observed in the failed field APG-63 SRUs, Hughes waited for the failure analyses to be completed. This activity was completed in late 1989 and, consistent with the previous results, there were no fatigue failures (Ref. 5).

However, one failure in an integrated circuit (IC) was a short attributed to a particle. Shock and vibration could dislodge a particle and cause a loose particle to move inside the IC package. A conductive particle can become trapped between two electrodes and thus cause a short. This type of failure occurs randomly and instantaneously, whereas fatigue failures in the scope of the ERFM program occur by progressive deterioration of an initial defect. Therefore, this type of failure, while involving vibration, is not relevant to ERFM.

Hughes concluded that the only environments that accelerate the failure mechanisms observed in the failed field APG-63 SRUs are steady high temperature and electrical stress. Accordingly, Hughes decided not to vibrate the SRUs during the high-temperature powered life test.

The approach presented herein differs significantly from that in the draft plan in that:

- The thermal environment is accelerated, that is, the part temperatures are higher than in normal operation.

- Vibration is not applied simultaneously with thermal environmental stresses.

Thus this final submittal is a complete rewrite of the plan. While the draft plan (Refs. 1 and 2) is a valuable source of information on the APG-63 life cycle environment, it does not describe the current approach to the ERFM CERT.

1.2.3 Revision of Final Submittal

In January 1991, Section 3.0 (Approach) of the Final Submittal (May 1990) of this Life Cycle Environmental Profile Plan was revised as follows:

- Thermal cycling will be performed continuously (24 hr/day, 7 days/week).

Figure 2 (CERT Environmental Profile) was revised accordingly.

In the May 1990 submittal, Section 3.0 stated that 3 thermal cycles per day will be performed, taking an estimated 5 hr/day. During the remaining 19 hr/day, the modules will be operated with a coolant inlet temperature of 63°C.

The rationale for the approach was that failure mechanisms accelerated by thermal cycling (fatigue) were not expected to occur in the CERT and failure mechanisms accelerated by steady high temperature (hybrid microcircuit failure from contamination) were expected.

Subsequently, the Failure Free Operating Period (FFOP) predictions for these modules have been completed (Ref. 6). Contrary to the indication in May 1990, the predicted FFOP is limited by fatigue failures of the plated through holes (PTH) in the printed wiring boards (PWB) of the digital modules. The predicted FFOP, as limited by fatigue of the PTHs in the digital modules, is 1 thousand CERT thermal cycles. On the other hand, the predicted FFOP, as limited by contamination-induced failures, is infinite.

Therefore the revised CERT environmental profile will better serve the program objective. It will enable the predicted FFOP for PTH fatigue failures to be exceeded in a few months of testing and thereby provide a direct experimental comparison with the prediction. The prediction of infinite life for contamination-induced failure mechanisms cannot be verified. However, it will be tested by the revised profile because the modules will be operated at steady high temperature roughly half of the time.

WL approved this revision.

1.2.4 Current Submittal

This submittal integrates the January 1991 revision into the Plan. It provides, in hard copy and on a diskette, an updated self-contained version of the Plan.

1.3 Summary

The thermal test cycle was derived by analyzing the modules and determining what flow rate and temperature combination would result in the hottest component of each module being maintained at the following approximate limits:

- resistors and capacitors: 100°C case temperature
- semiconductor devices: 125°C junction temperature.

The total cycle time is 120 minutes. The stressors simulated during the cycle are 1) steady high temperature with electrical bias and 2) thermal cycling.

2.0 HARDWARE DESCRIPTION

The test items selected for the Electronics Reliability Fracture Mechanics Program are two serial numbers each of a digital SRU and an analog SRU from the Hughes AN/APG-63 Radar for the F-15 aircraft (Ref. 7). They are utilized in the radar's Programmable Signal Processor (PSP) Line Replaceable Unit (LRU) (3137042) and are identified as follows:

SRU	Assy. Number
Timing and Control	3562102
Linear Regulator	3569800

Both module types incorporate a "flow-through" design with the heat exchanger an integral part of the module.

The Timing and Control module is a 9x5-inch digital module. The basic module package is an assembly of two printed wiring boards (PWBs) mounted back-to-back with a platefin coldplate sandwiched in between which creates a channel through which cooling air flows. The dominant part type is an integrated circuit flatpack. The flatpack leads are formed in a "gull wing" shape and soldered to the surface of the PWB. A flow-under thermal transfer adhesive is applied under the parts.

The Linear Regulator module is a 6x5-inch analog module consisting of a single PWB bonded to a platefin coldplate through which cooling air flows. The major contributors to failures are three hybrid microcircuits and a power transistor (Q1).

3.0 APPROACH

The environmental profile is a thermal cycle of the SRUs between ambient temperature and higher temperatures than in normal flight conditions. The higher-than-normal temperatures are produced by setting the coolant inlet temperature 33°C higher than normal, with the coolant flow rate set at its normal flight value (see Fig. 1).

Thermal cycling will be accomplished by turning off the module power and simultaneously setting the coolant inlet temperature to nominally 21°C (ambient temperature) (see Fig. 2). After thermal steady state is reached, the module power will be turned on and the coolant inlet temperature will be set at its elevated value. Thus the hardware temperatures will cycle between nominally 21°C and the peak powered values. The maximum range of the resistor and capacitor case temperatures will be approximately 80°C, and the maximum range of the semiconductor junction temperatures will be approximately 100°C.

4.0 FLOW AND TEMPERATURE PROFILE DERIVATION PROCEDURE

The simplest thermal cycle for accomplishing the desired result was determined as follows. A steady state thermal analysis was performed on the digital and analog SRUs (Refs. 8 and 9). The coolant to hottest junction temperature difference was noted. This temperature difference was subtracted from the maximum junction temperature limit to get the coolant temperature for the test cycle. The power off portion of the test cycle was determined by a transient analysis of the modules (Refs. 10 and 11). The transient analysis shows time required to reach steady state.

In the CERT, the plenum pressure will be set at a value necessary to provide an amount of air equal to what the Timing and Control Module and Linear Regulator Module receive in flight. The coolant inlet temperature is then adjusted to maintain the Timing and Control module at the temperature limit. This will result in the hottest resistor on the Linear Regulator module being maintained at approximately 100°C.

5.0 OTHER ENVIRONMENTAL PROFILES

5.1 Altitude

Altitude conditions will not be simulated during the ERFM test program. The failure mechanisms associated with an altitude environment are not represented in the ERFM test item. These failure mechanisms are commonly recognized to be:

- o Leakage, rupture or explosion of sealed containers.
- o Arcing or corona from high voltage or switching.
- o Evaporation of lubricants.

Also, the effective cooling of the ERFM test items should not vary as a function of altitude. The cards under test utilize flow through cooling air as the primary path for removing the heat. In flight, the cooling air is supplied by the F-15 Environmental Control System.

5.2 Humidity

The humidity of the air surrounding the electronic modules during the various parts of their life cycle also will not be simulated in the ERFM CERT test. In the ERFM CERT tests, described in the companion "Environmental Design Criteria and Test Plan" (CDRL Sequence No. 21), the modules will be cooled by dry nitrogen gas, and the modules will not be sealed from the ambient laboratory air. Simulation of the deployment humidity history would greatly complicate the tests, with negligible benefit in terms of additional information obtained.

5.3 Power

The F-15 Radar Programmable Signal Processor, consequently the ERFM test items that are housed therein, operates in a single mode when the radar is powered. The test items shall be powered with nominal aircraft power forms.

5.4 Vibration

As discussed in Section 1.2.2, vibration will not be applied simultaneously with thermal cycling during the CERT. However, a separate vibration test is planned for any of the four modules that do not fail during the CERT. The purpose of this vibration test is to cause a short circuit, like that observed in one of the failed field modules (Ref. 5), by trapping between electrodes any loose conductive particle that may be inside a semiconductor package.

The test conditions are as follows:

- module operating
- vibration in single axis normal to plane of module
- sinusoidal dwell at frequency about 100 Hz (below natural frequency of module)
- duration limited to 1 hour (about 360,000 cycles) to avoid expending significant fraction of vibration fatigue life of module
- level 20g peak.

Hughes will attempt to select the frequency such that the particle displacement is approximately equal to the free space in a flatpack. The results of work by Aerospace Corporation (Refs. 12 through 16) will be employed.

This test differs from the particle impact noise detection (PIND) test (Ref. 17) as follows:

- It is at the module level, rather than the part level.
- The duration is longer.

- The parts are powered.

- The objective is producing electrical failure, rather than merely identifying the presence of a loose particle.

REFERENCES

1) R. D. McKain and W. K. Hammond, "Life Cycle Environmental Profile Plan (Draft)", CLIN 0001, CDRL Sequence No. 20, September 1988.

2) W. K. Hammond, "Life Cycle Environmental Profile Plan", Addendum Providing Backup Information Requested by Air Force," CLIN 0001, CDRL Sequence No. 20, November 1998.

3) M. B. Bercaw (Air Force Contracting Officer), "Comments on Data Submitted by Hughes Aircraft Regarding Life Cycle Environmental Profile Plan", letter to Hughes, 12 December 1988.

4) "7th Quarterly Interim Technical Report", CLIN 0001, CDRL Sequence No. 3, February 1989.

5) "9th Quarterly Interim Technical Report", CLIN 0001, CDRL Sequence No. 3, August 1989.

6) L. B. Duncan, J. J. Erickson, and J. M. Kallis, "Failure Free Operating Period Predictions", CLIN 0001, CDRL Sequence No. 22, January 1991.

7) J. M. Kallis, R. D. Ritacco, C. H. Spruck, W. R. Draper, T. C. Preston, and W. W. Kusumoto, "Recommendation of Two Shop Replaceable Units (SRUs) Studied in Task III for Use in Task IV through Task XIII", CLIN 0001, CDRL Sequence No. 15, June 1988, revised July 1988.

8) IDC 722620/1329, "Thermal Analysis of the F-15 PSP Linear Regulator Module", from A. T. Bishop to J. M. Kallis, dated November 7, 1988.*

9) IDC 722620/1292, "Thermal Analysis of the F-15 PSP Timing And Control Module," from W. J. Hoskins to R. D. Ritacco, dated September 2, 1988.*

10) IDC 722620/1567, "Transient Thermal Analysis of the F-15 PSP Linear Regulator Module" from A. T. Bishop to J. M. Kallis, dated April 4, 1990.**

11) IDC 722620/1570, "Transient Thermal Analysis of the F-15 PSP Timing and Control Module" from W. J. Hoskins to J. M. Kallis, dated April 9, 1990.**

12) L. W. Aukerman and R. F. Millea, "The Effect of Applied Bias on the Movement of Conductive Particles within a Semiconductor Device", Aerospace Technical Memorandum No. ATM 76(6913)-6, 30 October 1975.

13) J. W. Ellinwood, "Motion of a Contaminant in an Operational Amplifier", Aerospace Technical Memorandum No. ATM 76(6441-06)-2, 25 June 1976.

14) J. W. Ellinwood and L. W. Aukerman, "Probability that a Contaminant in an Operational Amplifier will Cause a Permanent Short During Flight", Aerospace Technical Memorandum No. ATM 76(6641-06)-3, 4 August 1976.

15) C. Sve and J. S. Whittier, "Status Report - Mechanics of Contaminant Particles", Aerospace Technical Memorandum No. ATM 78(3902)-15, 24 March 1978.

16) C. Sve and J. S. Whittier, "Mechanics of Contaminant Particles", Aerospace Technical Memorandum No. ATM 79(4441-06)-1, 20 October 1978.

17) "Particle Impact Noise Detection Test", MIL-STD-883C, Notice 5, Method 2020.6, 29 May 1997.

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*Transmitted to AF as attachment to "6th Quarterly Interim Technical Report", CLIN 0001, CDRL Sequence No. 3, November 1988.

**Transmitted to AF as attachment to 12th Quarterly Interim Technical Report", CLIN 0001, CDRL Sequence No. 3, May 1990.

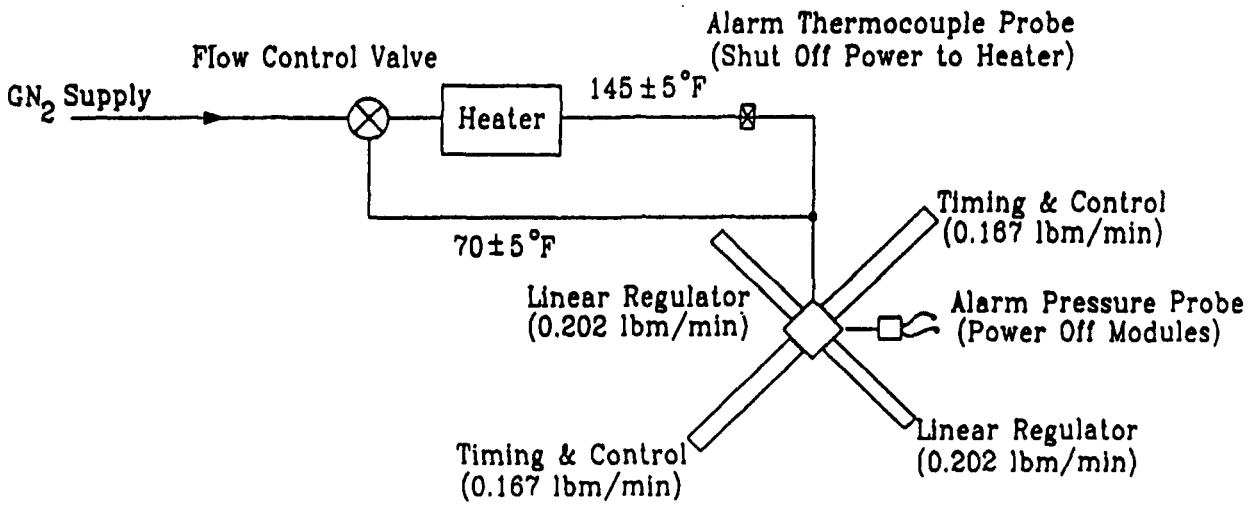

Figure S-1. Test Fixture Flow Schematic

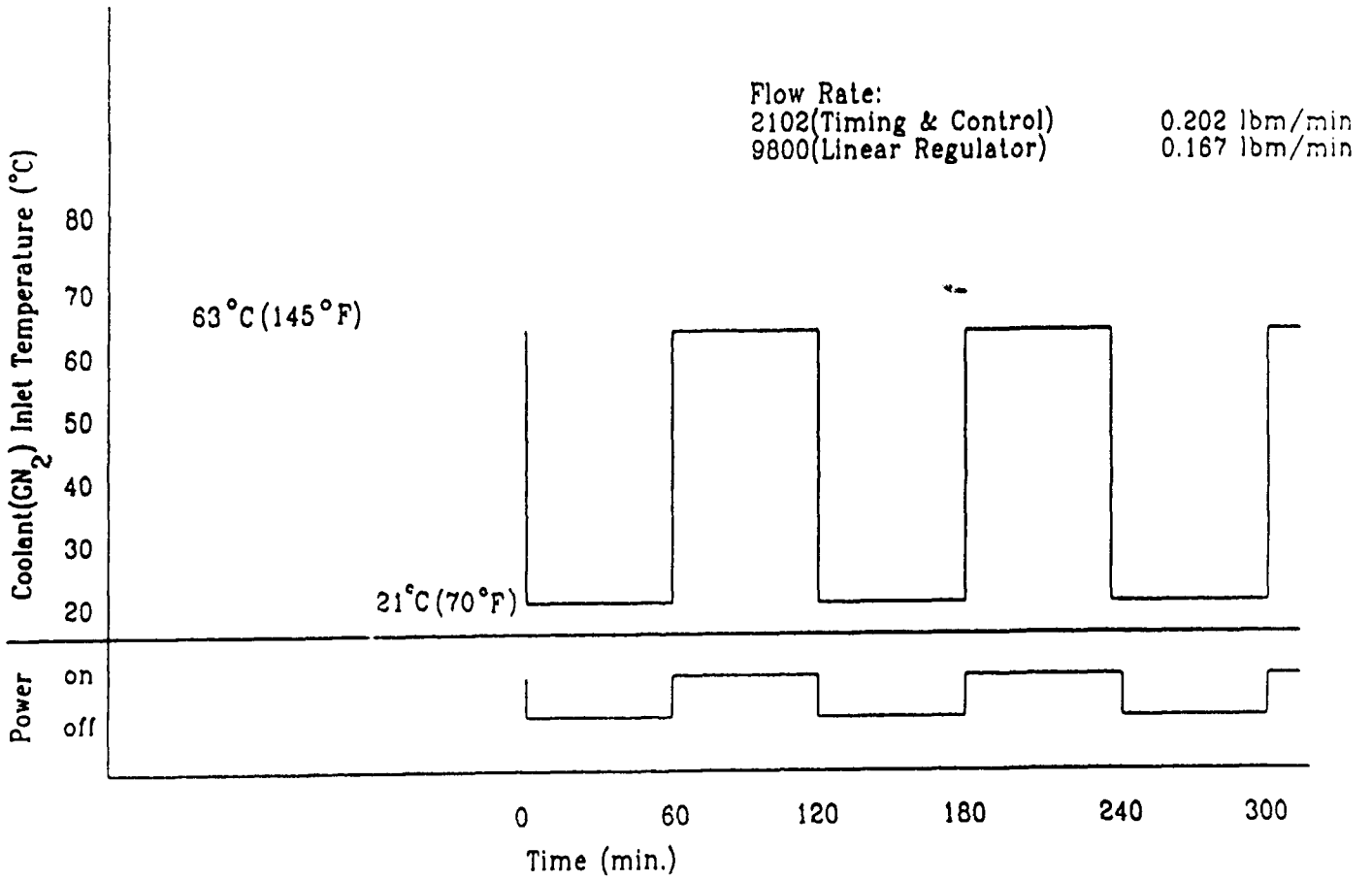

Figure S-2. CERT Environmental Profile

APPENDIX T

FAILURE FREE OPERATING PERIOD (FFOP)
PREDICTIONS

ELECTRONICS RELIABILITY FRACTURE MECHANICS

Contract No. F33615-87-C-3403

Purchase Request No. FY1456-87-02048
Project No. 2978

CLIN 0001, CDRL Sequence No. 22

Failure Free Operating Period Predictions
January 1991

Prepared for:

Wright Laboratory
Flight Dynamics Directorate
Wright-Patterson AFB, OH 45433-6553

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SUMMARY

The predicted Failure Free Operating Periods (FFOP) of the shop replaceable units (SRUs) in the Combined Environments Reliability Test (CERT), to be performed in Task XI, are as follows:

SRU NAME	SRU P/N	FFOP (CERT THERMAL CYCLES)
Timing & Control (digital)	3562102	10^3
Linear Regulator (analog)	3569800	10^6

For each P/N, the predicted FFOP is the same for each S/N built under Task IX.

The FFOP is limited by fatigue failures of the plated through holes (PTH) in the printed wiring boards (PWB). The fatigue life of the semiconductor device bond wires is predicted to be more than 1 million CERT thermal cycles. No failures from mobile ionic contamination or surface contamination are predicted in the CERT or in deployment. The contaminant concentration in these S/Ns of the hybrids in these analog modules has been evaluated as being too small to ever cause a module failure from contamination.

1.0 INTRODUCTION

This report documents Task X. The Statement of Work (SOW) for Task X is reproduced below.

> 4.10 TASK X - PERFORM FAILURE FREE OPERATING PERIOD PREDICTIONS (CDRL SEQ. #22)
>
> > 4.10.1 The contractor shall model the SRUs selected from para. 4.3.4 to determine the localized environmental conditions and stresses (temperatures, stress cycles stress, vibration) within the SRU based upon the CERT environmental profiles developed in Task V.
> >
> > 4.10.2 The contractor shall predict the Failure Free Operating Period using the models developed under Task VI for each copy of the SRUs built under Task IX utilizing its specific initial material properties, known defect population and localized environmental conditions at each potential failure manifestation location.

The SRUs selected in Task III (SOW para. 4.3.4) are described in CDRL Sequence No. 15.

The CERT environmental profile developed in Task V is described in CDRL Sequence No. 20 (Final Submittal, May 1990 [revised January 1991]). It consists of thermal cycles from 21°C (unpowered) to powered operation with a coolant inlet temperature of 63°C.

The models developed under Task VI and the special fabrication/inspection performed under Task IX will be documented in the Final Technical Report (CDRL Sequence No. 4). Tasks VI and IX also have been documented in the Monthly R&D Status Report (CDRL Sequence No. 2), the Quarterly Interim Technical Report (CDRL Sequence No. 3), and the Quarterly Presentation Material (CDRL Sequence No. 8).

2.0 SRUs BUILT UNDER TASK IX

Table 1 lists the S/Ns of the two copies of the SRUs built under Task IX, the S/Ns of the PWBs on the digital modules, and the S/Ns of the hybrids (U1, U2, U3) on the analog modules. The six hybrids placed on these two copies of the analog modules were selected by the ERFM program team on the basis of the results of the special contamination screen performed on the hybrids ordered for the ERFM program.

Attachments I and II show the locations, specified by the ERFM program team, for selected integrated circuits on these two copies of the digital module. The selections were made on the basis of the results of special NDI of the ICs performed for the ERFM program. To maintain the identity of the specially inspected ICs, the ERFM program team marked each copy of each IC with a S/N. There is a series of S/Ns for each IC P/N. The locations of the selected ICs are shown in Attachments I and II by placing the S/N below its position on the map and next to its circuit symbol.

3.0 LIFE PREDICTIONS

Life predictions have been made for fatigue failures and for contamination-induced failures. They are documented herein in Attachments III and IV, respectively.

TABLE T-1

SERIAL NUMBERS

P/N 3562102

SRU	FRONT PWB	REAR PWB
0001	3786	31074
0002	10800	71082

P/N 3569800

SRU	U1	U2	U3
1149	11650	8355	8388
1150	11789	7941	8872

ATTACHMENT I

PART PLACEMENT MAP FOR
P/N 3562102, S/N 0001

DELETED FROM FINAL REPORT
(ALREADY IN APPENDIX N)

ATTACHMENT II

PART PLACEMENT MAP FOR
P/N 3562102, S/N 0002

DELETED FROM FINAL REPORT
(ALREADY IN APPENDIX N)

ATTACHMENT III

FFOP PREDICTION
FOR
FATIGUE FAILURES

Nominal Data. Continued.

CATALOG	NAME	VERTEX	HE_MOD	BLADE_SH	BASE_SH	BASE_OR	SHOLD_SH	SHOLD_OR	LATHF_SH	LATHF_OR
40-0944	Ensor	7	L	S	E	N	S	T	S	E
40-0405	Ensor	7	D	S	R	N	I	B	S	E
43-0030	Ensor	7	D	S	I	N	I	B	I	E
43-0400	Ensor	7	L	I	R	N	I	T	R	E
44-0716	Ensor	7	D	S	E	N	S	B	S	E
35-2175	Ensor	0								
36-3000	Ensor	0								
35-2908	Ensor	0								
41-0435	Ensor	0								
35-2637	Ensor	0								
35-2451	Ensor	0								
36-3597	Ensor	0								
36-3551	Ensor	0								
36-4212	Ensor	0								
36-3066	Ensor	0								
35-2356	Ensor	0								
35-2654	Ensor	0								
41-0210	Ensor	0								
36-3503	Ensor	0								
35-2889	Ensor	0								
41-0099	Ensor	0								
38-0023	Ensor	0								
40-0186	Ensor	0								
41-0056	Ensor	0								
44-0190	Ensor	0								
36-4249	Ensor	0								
38-0811	Ensor	0								
41-0355	Ensor	0								
37-0663	Ensor	0								
36-3422	Ensor	0								
40-0573	Ensor	0								
44-0712	Ensor	0								
44-0790	Ensor	0								
40-1038	Ensor	0								
44-0148	Ensor	0								
37-0778	Ensor	0								
36-3652	Ensor	0								
37-0774	Ensor	0								
36-3455	Ensor	0								
44-1494M	Ensor	0								
44-1041M	Ensor	7	L	S	E	N	I	H	I	E
44-1407M	Ensor	7	L	S	S	N	S	T	I	E
44-0844	Ensor	0								
44-0926	Ensor	0								
50-0010	Ensor	7	L	S	E	N	I	B	I	E
50-0011	Ensor	7	L	I	E	N	I	T	E	E
35-2956	Fresno	3	X	S	I	N	X	X	X	X
41-0031	Fresno	3	X	S	S	N	X	X	X	X
38-0483	Fresno	3	X	S	S	N	X	X	X	X
35-3141	Frio	7	L	I	R	N	I	H	S	E
36-3102	Frio	7	L	I	R	N	I	H	S	E
36-4182	Frio	7	L	I	R	N	I	H	S	E
36-4027	Frio	7	L	I	R	N	I	H	S	E
35-3148	Frio	7	L	I	R	N	I	H	S	E
36-3632	Frio	7	L	I	R	N	I	H	S	E
35-2446	Frio	7	L	S	R	N	S	T	I	E
36-3882	Frio	7	L	S	R	N	S	T	I	E
41-0089	Frio	7	L	S	R	N	S	T	I	E
35-2149	Frio	9	L	S	I	N	I	B	A	E
35-3073	Frio	9	L	S	I	N	I	B	A	E
41-0003	Frio	9	L	S	I	N	I	B	A	E
38-0046	Frio	7	L	S	I	N	I	H	A	V
40-1282	Frio	7	D	S	R	N	I	B	I	E
40-0978	Frio	7	D	I	R	N	I	B	I	E
36-3889	Frio	0								
38-0001	Frio	0								
38-0194	Frio	0								
36-3962	Frio	0								
50-0093	Frio	7	L	S	R	N	I	T	I	E
35-2635	Godley	7	D	E	E	N	S	T	S	E
36-3507	Godley	7	D	S	E	N	I	T	I	E
35-2009	Godley	7	D	S	E	N	I	T	I	E
35-3068	Godley	7	D	S	E	N	I	T	I	E
36-3509	Godley	7	D	S	E	N	I	T	I	E
41-0103	Godley	7	D	S	E	N	I	T	I	E
35-2018	Godley	7	D	E	E	N	S	T	I	C
35-2886	Godley	7	D	E	E	N	I	T	I	E
37-0631	Godley	7	D	E	E	N	I	T	I	E
36-4258	Godley	7	D	E	E	N	I	T	I	E
35-3032	Godley	7	D	E	E	N	I	T	I	E
35-3128	Godley	7	D	E	E	N	I	T	I	E
35-3142	Godley	7	D	S	E	N	I	T	S	E
40-0164	Godley	7	D	S	E	N	I	H	I	E
43-0046	Godley	7	D	S	S	N	I	T	I	C
44-0825	Godley	7	D	S	E	N	S	H	I	E
38-0854	Golondrina	3	X	E	R	N	X	X	X	X

(Table continues on the following page.)

Nominal Data. Continued.

CATALOG	NAME	VERTEX	HE_MOD	BLADE_SH	BASE_SH	BASE_OR	SHOLD_SH	SHOLD_OR	LATHF_SH	LATHF_OR
36-4297	Golondrina	3	X	E	R	N	X	X	X	X
40-0980	Golondrina	3	X	R	R	N	X	X	X	X
35-2214	Gower	7	D	E	R	N	I	H	S	P
35-2890	Gower	7	D	S	I	N	S	H	E	V
35-3121	Gower	7	D	S	I	N	S	H	E	V
36-3924	Gower	7	D	S	R	N	S	T	E	V
35-3159	Gower	7	D	S	R	N	S	T	E	V
36-3481	Gower	7	D	S	R	N	S	T	E	V
36-3009	Gower	7	D	S	R	N	S	T	S	E
41-0366	Gower	7	D	S	R	N	S	T	S	E
36-3495	Gower	7	D	S	R	N	I	T	S	E
37-0673	Gower	5	D	S	I	N	X	X	E	V
40-1309	Gower	5	D	S	I	N	X	X	R	P
40-1161	Gower	7	D	E	R	N	I	T	S	E
40-1306	Gower	7	D	E	R	N	S	T	R	E
43-0359	Gower	5	D	E	I	N	X	X	E	P
43-0076	Gower	7	L	E	I	N	I	T	R	E
43-0349	Gower	5	L	S	R	N	X	X	E	P
43-0124	Gower	7	D	E	I	N	S	T	S	P
44-0287	Gower	7	D	E	I	N	S	T	S	P
44-0276	Gower	7	D	E	A	N	E	T	S	E
44-0776	Gower	7	L	E	I	N	I	T	S	E
38-0844	Gower	0								
44-0833	Gower	0								
35-3052	Lange	7	D	S	S	N	I	B	S	E
35-2854	Lange	7	D	S	S	N	I	B	S	E
35-3090	Lange	7	D	S	S	N	I	B	S	E
41-0388	Lange	7	D	S	S	N	I	B	S	E
35-2985	Lange	7	D	E	S	N	I	B	S	E
36-3508	Lange	7	D	E	S	N	I	B	S	E
36-4330	Lange	7	D	E	S	N	I	B	S	E
41-0057	Lange	7	D	E	S	N	I	B	S	E
35-3083	Lange	7	D	E	S	N	I	B	S	E
36-3542	Lange	7	D	S	R	N	I	B	A	E
35-2388	Lange	7	D	S	I	N	I	H	R	E
38-0858	Lange	7	D	S	E	N	I	B	I	E
40-0185	Lange	7	D	S	S	N	I	H	S	E
37-0057	Lange	0								
44-1043M	Lange	7	D	S	S	N	I	B	S	N
44-1320M	Lange	7	D	S	S	N	I	B	S	E
35-3034	Marcos	7	D	E	S	N	I	B	I	E
44-0440	Marcos	7	D	E	S	N	I	B	I	E
41-0062	Marcos	7	D	S	S	N	I	B	I	E
35-3123	Marcos	7	D	S	E	N	I	B	I	E
36-3575	Marcos	7	D	S	I	N	I	B	S	E
35-2394	Marcos	7	D	S	R	N	R	B	S	E
37-0734	Marcos	7	D	I	I	N	S	B	I	E
35-2938	Marshall	7	D	S	S	N	I	B	S	E
35-2464	Marshall	7	D	S	S	N	I	B	S	E
35-2858	Marshall	7	D	S	S	N	I	B	S	E
43-0295	Marshall	7	D	S	S	N	I	B	S	E
35-2157	Marshall	7	D	E	S	N	I	B	I	E
36-3104	Marshall	7	D	E	S	N	I	B	I	E
35-3013	Marshall	7	D	E	S	N	I	B	I	E
36-4282	Marshall	7	D	E	S	N	I	B	I	E
35-3144	Marshall	7	D	E	S	N	I	B	I	E
35-2430	Marshall	7	D	S	S	N	I	B	S	P
37-0503	Marshall	7	D	S	I	N	S	B	I	E
36-4174	Marshall	7	D	S	I	N	S	B	I	E
41-0002	Marshall	7	D	S	I	N	S	B	I	E
35-0166	Marshall	7	D	S	S	N	I	B	E	E
35-2636	Marshall	7	D	S	S	N	I	B	E	E
36-4271	Marshall	7	D	E	E	N	S	B	I	C
37-0633	Marshall	7	D	S	S	N	S	B	I	E
37-0628	Marshall	7	D	S	S	N	S	B	I	E
35-3155	Marshall	7	D	S	S	N	S	B	I	E
40-1275	Marshall	7	D	S	S	N	S	B	I	E
36-4291	Marshall	7	D	S	S	N	S	B	I	E
35-3055	Marshall	7	D	R	E	N	I	B	S	E
35-2874	Marshall	7	D	S	S	N	I	B	I	E
38-0099	Marshall	7	D	S	S	N	I	B	I	E
40-0355	Marshall	7	D	S	S	N	I	B	I	E
40-0527	Marshall	7	D	S	S	N	I	B	I	E
36-3692	Marshall	7	D	S	I	N	I	B	S	E
41-0426	Marshall	7	D	S	I	N	I	B	S	E
44-0473	Marshall	7	D	E	S	N	I	B	S	P
35-2887	Marshall	7	D	E	S	N	I	B	S	P
35-3014	Marshall	7	D	E	I	N	I	B	R	E
36-3074	Marshall	7	D	E	S	N	I	B	S	E
35-3104	Marshall	7	D	S	I	N	S	B	R	E
37-0756	Marshall	7	D	E	E	N	I	B	S	E
43-0405	Marshall	7	D	S	I	N	S	H	I	E
44-0296	Marshall	7	D	I	R	N	S	B	I	E
44-0472	Marshall	7	B	I	S	N	S	B	S	E
35-2988	Marshall	0								
35-2156	Marshall	0								

(Table continues on the following page.)

INTERDEPARTMENTAL CORRESPONDENCE

To: J.M. Kallis
Org: 72-26

c: Distribution

Date: 18 Dec. 1990
Ref: 722630/1284

Subject: ERFM CERT FFOP Predictions

From: L.B. Duncan
Org: 72-26-30

Bldg: E01 **MS:** D102
Loc: EO **Phone:** 616-0924

Failure Free Operating Period (FFOP) predictions were made for F15 Digital and Analog modules undergoing Combined Environments Reliability Test (CERT) as part of the Electronics Reliability Fracture Mechanics (ERFM) program. Specifically, fatigue life predictions were made for 1 mil diameter interconnect wires and plated-through-holes (PTHs) undergoing thermal cycling. The FFOP predictions are as follows:

- Digital Modules: 1 thousand CERT thermal cycles
- Analog Modules: 1 million CERT thermal cycles

The FFOP is predicted to be limited by PTH fatigue. The wire interconnects in the digital modules are predicted to last more than 0.5 million CERT thermal cycles, and those in the analog module are predicted to last more than 1 million CERT thermal cycles.

The attached report describes the analyses that were performed to support the predictions.

Prepared by: L B Duncan

L.B. Duncan, Senior Scientist
Structural Mechanics Department
Product Analysis Laboratory

ERFM CERT FFOP PREDICTIONS

IDC 722630/1284

Dated: 18 DECEMBER 1990

Prepared by: L.B. Duncan

L.B. Duncan, Senior Scientist

STRUCTURAL MECHANICS DEPARTMENT
PRODUCT ANALYSIS LABORATORY
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1.0 INTRODUCTION

Failure Free Operating Period (FFOP) predictions were made for F15 Digital and Analog modules undergoing Combined Environments Reliability Test (CERT) as part of the Electronics Reliability Fracture Mechanics (ERFM) program. Specifically, fatigue life predictions were made for 1 mil diameter interconnect wires and plated-through-holes undergoing thermal cycling.

2.0 SUMMARY

The FFOP predictions are as follows:

- Digital Modules: 1 thousand CERT thermal cycles
- Analog Modules: 1 million CERT thermal cycles

The FFOP is predicted to be limited by PTH fatigue. The wire interconnects in the digital modules are predicted to last more than 0.5 million CERT thermal cycles, and those in the analog module are predicted to last more than 1 million CERT thermal cycles.

3.0 BACKGROUND

3.1 WIRE INTERCONNECT POWER (THERMAL) CYCLING

Small diameter (0.001 inch) Al-1% Si wires are used in F-15 APG-63 integrated circuits and hybrids to provide electrical connections between chips and leadframes. The interconnect wires are ultrasonically bonded to the chips and the leadframes as described in Reference 1. The bonding process changes both the geometry of the wire cross section and the surface finish. At the bond, the round cross section of the wire is transformed into a rectangular geometry over a very short length of wire. An unsupported "heel" section, approximately a few tenths of a wire diameter in length, connects the round wire to the part of the wire that is actually bonded to the adjoining structure. The heel section is typically a few mils wide and 2 to 3 tenths of a mil thick. The surface of the heel region is characterized by deep, crack-like defects.

The interconnect wire has a coefficient of thermal expansion (CTE) that is different from the structures to which it is attached. As such, when the wire changes temperature due to temperature cycling and/or power cycling of the device, the wire changes length relative to its bonded ends. The change in length causes the wire arch to deform which induces rotation and bending at the wire heel. Repeated thermal cycling can lead to fatigue failure if the cyclical stresses are high enough.

3.2 PLATED-THROUGH-HOLE THERMAL CYCLING

Plated-thru-hole thermal cycling fatigue,which is discussed in detail in References 2 and 3, is primarily due to the mismatch of copper and PWB laminate through-thickness CTE. When a PTH/PWB structure is subjected to a change in temperature, the laminate grows or shrinks at a higher rate than the copper PTH. The PTH tends to restrain the laminate, but in doing so incurs substantial strain. If the change in temperature is large enough, the PTH can be strained well beyond the yield strength of the copper. Large cyclical plastic strain can eventuate in low-cycle fatigue and failure in fewer than 10,000 cycles.

Many other parameters affect the interaction of the PTH and the PWB. Discussions of some of the more significant parameters follow.

PTH thickness and diameter: PTH fatigue life increases as the PTH barrel thickness and diameter increase. The PTH stiffness increases as the annular cross-sectional area increases, and it is more able to resist the thermal expansion of the PWB laminate.

Laminate thickness: PTH fatigue life tends to decrease as laminate thickness increases. It has been observed that PWB through-thickness CTE tends to increase as the laminate thickness increases (Reference 2). Thicker laminates often have a higher resin content than thinner laminates (less than 0.060 inch.). Resin (epoxy or polyimide) has a much higher CTE than the glass cloth laminate reinforcement and, as such, increases the CTE of the resin/glass cloth composite. In addition, for a given PTH diameter, a thicker PWB provides a larger effective volume of material to structurally interact with the PTH which results in higher PTH thermal strains and shorter fatigue life.

Copper fatigue ductility: PTH copper ductility increases low-cycle fatigue life. Given a high level of plastic strain, a ductile copper will last longer than a stronger but less ductile copper.

Copper strength: If thermally induced strains in the copper are below the yield point, a stronger copper will have a longer fatigue life than a less strong but more ductile copper.

Matrix Glass Transition Temperature, T_g: It is often assumed that the laminate matrix (resin) has a bilinear CTE wherein a transition occurs at the glass transition temperature, T_g of the matrix. The glass transition temperature is the value at which the matrix softens and the CTE increases dramatically. Epoxy has a CTE of 30 - 90 μin/in/°C below T_g and over 200 μin/in/°C above T_g (Reference 2). In the present analysis, T_g was assumed to be 125°C, which is higher than the upper limit of the CERT.

Additional issues: As stated in Reference 2, PTH barrel fatigue failures are usually observed to occur near the central region of the barrel (near the center of the PWB laminate). It is believed that copper ductility can be less at the center of the laminate where it is more difficult to assure uniform transport of the PTH copper plating solution. Also, resin-rich pockets tend to occur near the center of the laminate where it is more difficult to extract excess resin during the PWB fabrication process. These resin-rich areas are potential sites for PTH strain concentration due to the high CTE of the resin.

4.0 FFOP PREDICTIONS

4.1 CERT THERMAL CYCLING ENVIRONMENT

The CERT thermal cycling environment is shown in Figure 1. The powered portion of the profile specifies a 63°C coolant inlet temperature. The powered condition is followed by transient periods wherein the inlet temperature of the coolant is reduced to 21°C, held for 60 minutes, then raised to 63°C and held for 60 minutes.

CERT transient thermal analyses were performed to predict component and mounting surface temperatures for the analog (Reference 4) and digital modules (Reference 5). The analyses predicted that both component and surface temperatures were higher for the digital module which has a total power dissipation of 47.8 Watts. The analog module has a total dissipation of 7.8 Watts.

Temperatures obtained from the CERT thermal analyses were used for the FFOP predictions. The wire interconnect temperature was taken to be equal to the highest junction temperature. The temperature was assumed to be constant over the entire length. The PTH temperature was assumed to be identical to the highest mounting surface temperature on each of the digital and analog modules.

The maximum junction temperatures for the digital and analog modules were as follows:

- Digital module: 134°C, component 932820, U1508, Ref. 5.
- Analog module: 100°C, component H990446-001B, U4, Ref. 4.

The maximum mounting surface temperatures for the digital and analog modules were as follows:

- Digital module: 105°C, under component 905570-73B, C151,Ref. 5.
- Analog module: 77°C, under component 928765-502B, Q1, Ref. 4.

4.2 WIRE INTERCONNECTS

Analyses were performed by Failure Analysis Associates (FaAA) to predict wire interconnect fatigue life for power cycling (Reference 1). Predictions were made for maximum wire currents of 1 to 1.5 amps. The temperature distribution along the length of the wire was computed and used to predict the bond heel rotation by means of finite element analysis. The associated wire strain range was used as input to a fracture mechanics analysis to predict crack propagation life. It was assumed that the crack initiation period was insignificant due to the very crack-like initial defects that typically are present at the wire bond heel.

Additional analysis performed by FaAA (Reference 6 and Appendix A) determined bond heel rotation for a uniform wire temperature of 134°C (digital module) relative to the adjoining structures. This condition was found to be equivalent to a power cycling current of 1.1 amps. A current of 1 amp results in a bond heel rotation equal to that caused by a uniform temperature of 100°C (analog module).

Wire bond power cycling fatigue data obtained at SwRI and Hughes (Reference 7) exhibited substantial scatter as was expected. FaAA analysis demonstrated that the observed scatter could be accounted for by considering a range of initial defect (crack) depths of 0.002 to 0.16 mil in the (assumed) 0.33 mil thick heel region. In the present analysis, the largest calculated defect depth (0.16 mil) was taken to be the largest wire interconnect defect in the CERT hardware.

The fatigue lives for the given conditions are obtained from Figure 15 of Reference 1 (see Appendix A of this report). The wire interconnect fatigue lives are approximately 1 million cycles for the digital module (134°C, 1.1 amps) and 2 million cycles for the analog module (100°C, 1 amp).

In general, it is good practice (and often a requirement) to include factors of safety in a fatigue life prediction to account for uncertainties in material properties, geometry, load levels, etc.. The magnitude of the assumed factor of safety depends upon the criticality of the prediction and the confidence to which important parameters are known. With regard to low-cycle fatigue life prediction, it is not uncommon to require a factor of safety of as much as 10 when structural failure would jeopardize the operational integrity of a component and important analysis parameters are not well known. For these ERFM FFOP predictions, a factor of safety of 2 is considered to be reasonable since the important analysis parameters are fairly well known by virtue of extensive experimentation at SwRI.

Therefore, applying a factor of safety of 2, the FFOP prediction is 0.5 million CERT thermal cycles for the digital module and 1 million CERT thermal cycles for the analog module..

4.3 PLATED-THROUGH-HOLES

At this time, the FaAA PTH fracture mechanics based fatigue crack initiation and propagation life models are under development. Therefore, in order to make CERT test FFOP predictions, the approach described in

Reference 2 was adopted. The approach utilizes strength of materials models to predict PTH strain as a function of PTH and laminate geometry and material properties. The predicted copper strain range is input to a modified Manson universal slopes strain-life equation (Reference 8) to calculate cycles to failure. In this approach, crack initiation and crack propagation are not treated explicitly. Rather, it is assumed that overall failure (fracture) of the PTH barrel occurs at the predicted number of cycles.

The subject analysis is presented in Appendix B. Various analysis parameters were adjusted to account for knowledge gained from the ERFM PTH thermal cycling tests performed at SwRI and by PTH thermal cycling finite element analysis performed by FaAA. Specifically, the following parameters were assumed:

Copper Material Properties

Young's Modulus = 16 MSI
Modulus after yielding = 0.1 MSI
CTE = 17 μin/in/°C
Ultimate Strength = 35 KSI
Yield Strength = 25 KSI
Fatigue Ductility = 0.14

PWB (Thru-Thickness) Material Properties

Young's Modulus = 0.5 MSI
CTE = 85 μin/in/°C

Geometry

PWB thickness = 0.1 in (digital), 0.036 in (analog)
PTH diameter = 0.026 in
PTH thickness = 0.0015 in

Finally, the copper fatigue ductility coefficient was chosen to calibrate the fatigue life algorithm to the observed failures of PTHs which were subjected to the MIL-T thermal cycling test profile (Reference 9) at SwRI. The assumed value of 0.14 was less than measured copper foil elongation (0.18, SwRI measurement of ERFM PTH copper foil) but is consistent with the belief that ductility at the center of a PTH can be relatively low.

Given the above, PTH fatigue failure was calculated to occur after 1995 CERT thermal cycles for the digital module and after 2.5 million thermal cycles for the analog module.

Applying a safety factor of 2 (as in Section 4.2) and rounding to one significant figure, the following FFOPs are predicted for the PTHs:

- Digital module: 1 thousand cycles
- Analog module: 1 million cycles.

5.0 CONCLUDING REMARKS

A fracture mechanics based life model was used to predict wire interconnect CERT fatigue life. Since fracture mechanics based models are not yet available for PTHs, a Coffin-Manson strain-life approach was utilized for the CERT prediction. The calculated fatigue lives were reduced by a factor of safety of 2 on life to establish the predicted FFOPs. The factor of safety is intended to account for various material property uncertainties.

6.0 REFERENCES

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2. IPC-TR-579, *Round Robin Reliability Evaluation of Small Diameter Plated Through Holes in Printed Wiring Boards*, September, 1988.

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4. IDC 722620/1567, *Transient Thermal Analysis of the F-15 PSP Linear Regulator Module*, A.T.Bishop to J.M. Kallis, 4 April, 1990.

5. IDC 722620/1570, *Transient Thermal Analysis of the F-15 PSP Timing and Control Module*, W.J. Hoskins to J.M. Kallis, 9 April, 1990.

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7. Popelar, C.F., Davidson, D.L., and Kanninen, M.F., *Investigation of Fracture Mechanics Life Assessments of Interconnect Wire Bonds Through Current Pulsing Fatigue Testing*, Southwest Research Institute, Project No. 06-2715, December 31, 1990.

8. Fuchs, H.O., and Stephens, R.I., *Metal Fatigue in Engineering*, John Wiley and Sons, 1980.

9. Davidson, D.L., Campbell, J.D., Spencer, J.E., Popelar, C.F., and Kanninen, M.F., *Thermal Cycling of Plated Through Holes*, Southwest Research Institute, Project No. 06-2715, December 31, 1990.

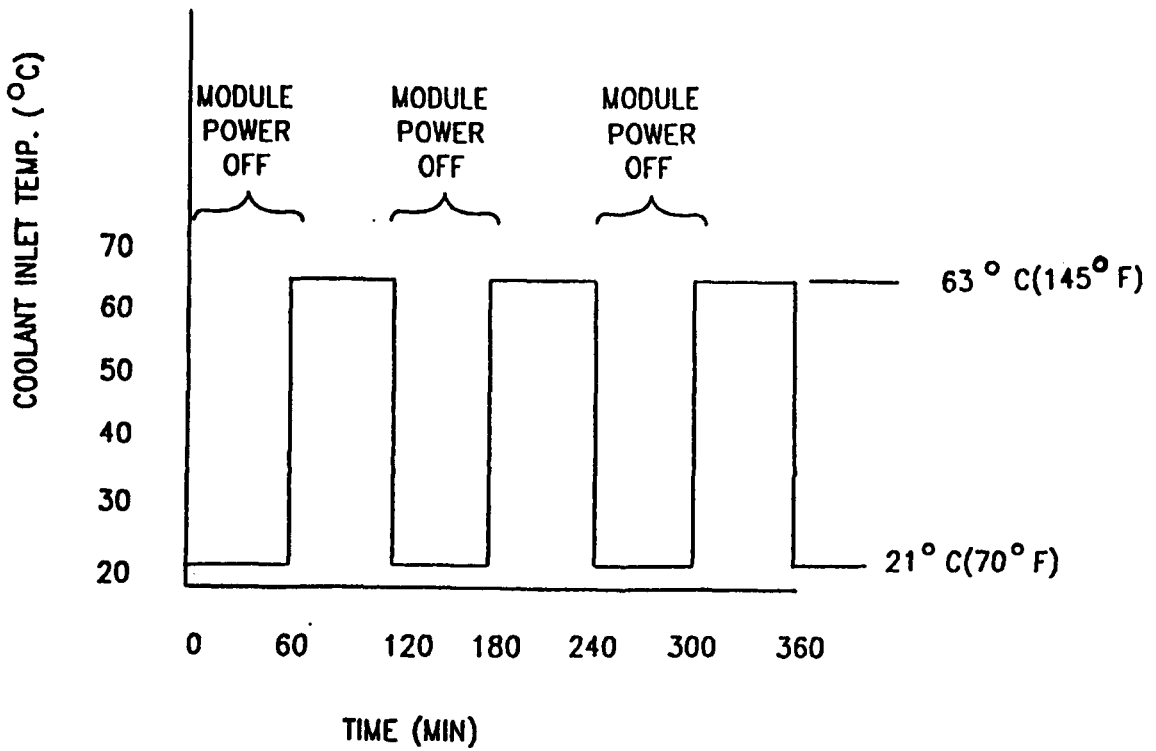


Figure 1. CERT Environmental Profile

APPENDIX A

FaAA

WIRE INTERCONNECT FATIGUE LIFE PREDICTION

Reference 6

Failure
Analysis
Associates.

Engineering and Scientific Services
149 Commonwealth Drive, P.O. Box 3015
Menlo Park, California 94025
(415) 326-9400 Telex 704216 Fax (415) 326-8072

July 26, 1990

Mr. Larry Duncan
Hughes Aircraft Company
Electro-Optical and Data Systems Group
Bldg. E0/E01, M/S D102
2000 El Segundo Blvd.
El Segundo, California 90245

Subject: Wire bond rotation for uniform temperature change.

Dear Larry:

Enclosed are some additional plots of results from our wire power cycling analysis. Figure 1 shows a comparison between wire temperature distributions for the four current values analyzed. The convective heat transfer coefficients used in each case and the maximum wire temperatures are summarized in Table 1. Figure 2 shows a plot of wire bond heel rotation as a function of current squared from the beam model analyses.

I ran the thermo-elastic analysis of the wire bond with uniform temperature that you requested last Monday. Element temperatures over the entire length of the wire loop were set to 134°C (273°F). The coefficient of thermal expansion, α, for the wire was given a value of 9.8×10^{-6} °F^{-1}, the difference between aluminum, $\alpha_{Al} = 13.8 \times 10^{-6}$ °F^{-1}, and alumina, $\alpha_{Al_2O_3} = 4.0 \times 10^{-6}$ °F^{-1}. The resulting bond heel rotation was computed to be 3.3×10^{-3} radians. Interpolation in Figure 2 indicates that this same rotation is predicted for a current of 1.1 amps in a wire bonded to an alumina carrier which is maintained at room temperature.

If you have any questions or comments regarding these results, please call us. I will be out of the office until August 6, but Dave will be here.

Very truly yours,

Robert A. Sire
Senior Engineer
Fracture Mechanics Group

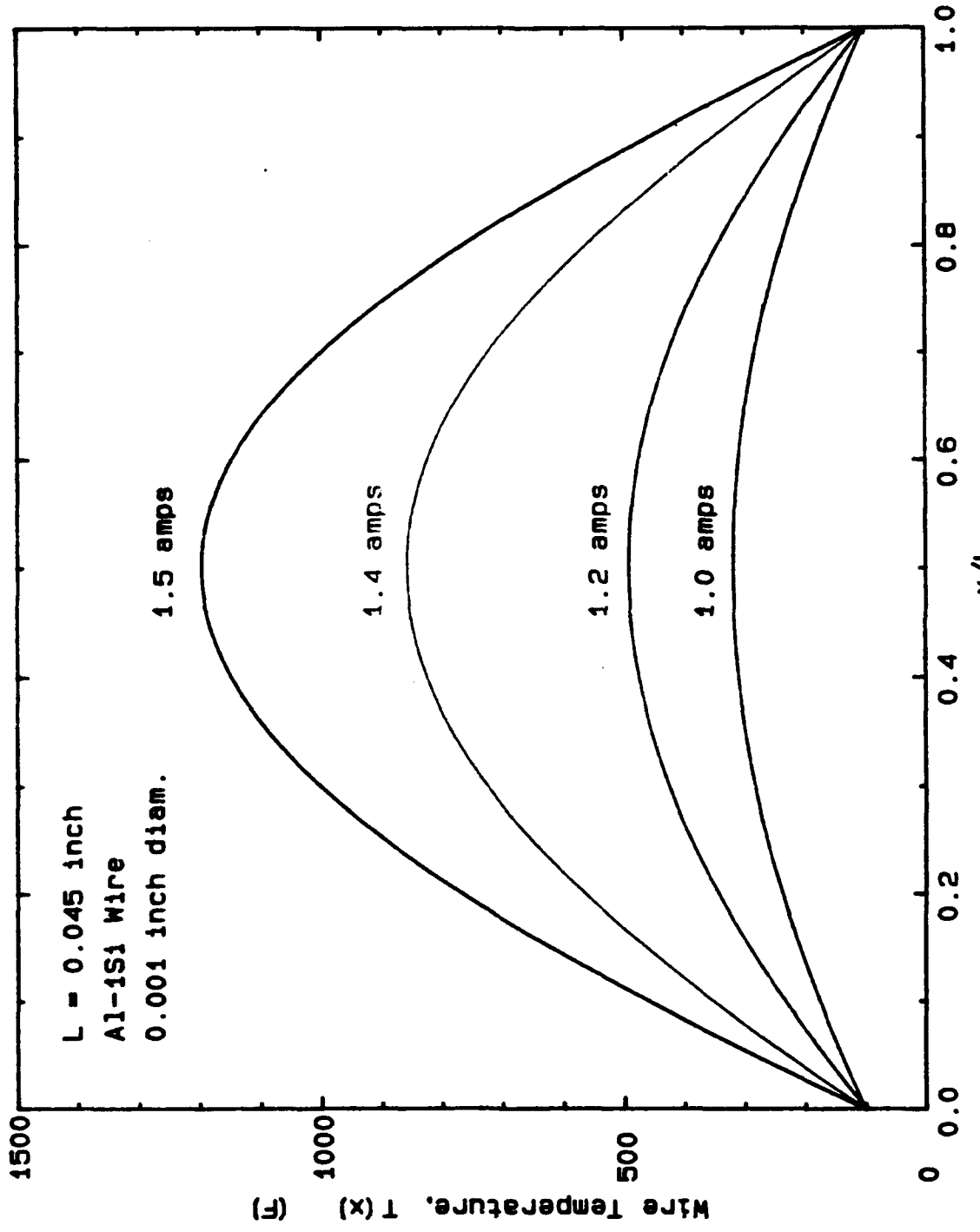
Enclosures (3)

Table 1

Convective Heat Transfer Coefficients
and Maximum Wire Temperatures
as a Function of Current for
SwRI Power Cycling Test Wires

D = 0.001 inch
L = 0.045 inch

I (amps)	h (W/in² °C)	Tmax (°F)
1.0	0.42	319
1.2	0.46	493
1.4	0.48	858
1.5	0.55	1213



Wire temperature distributions for various currents.

Figure 1

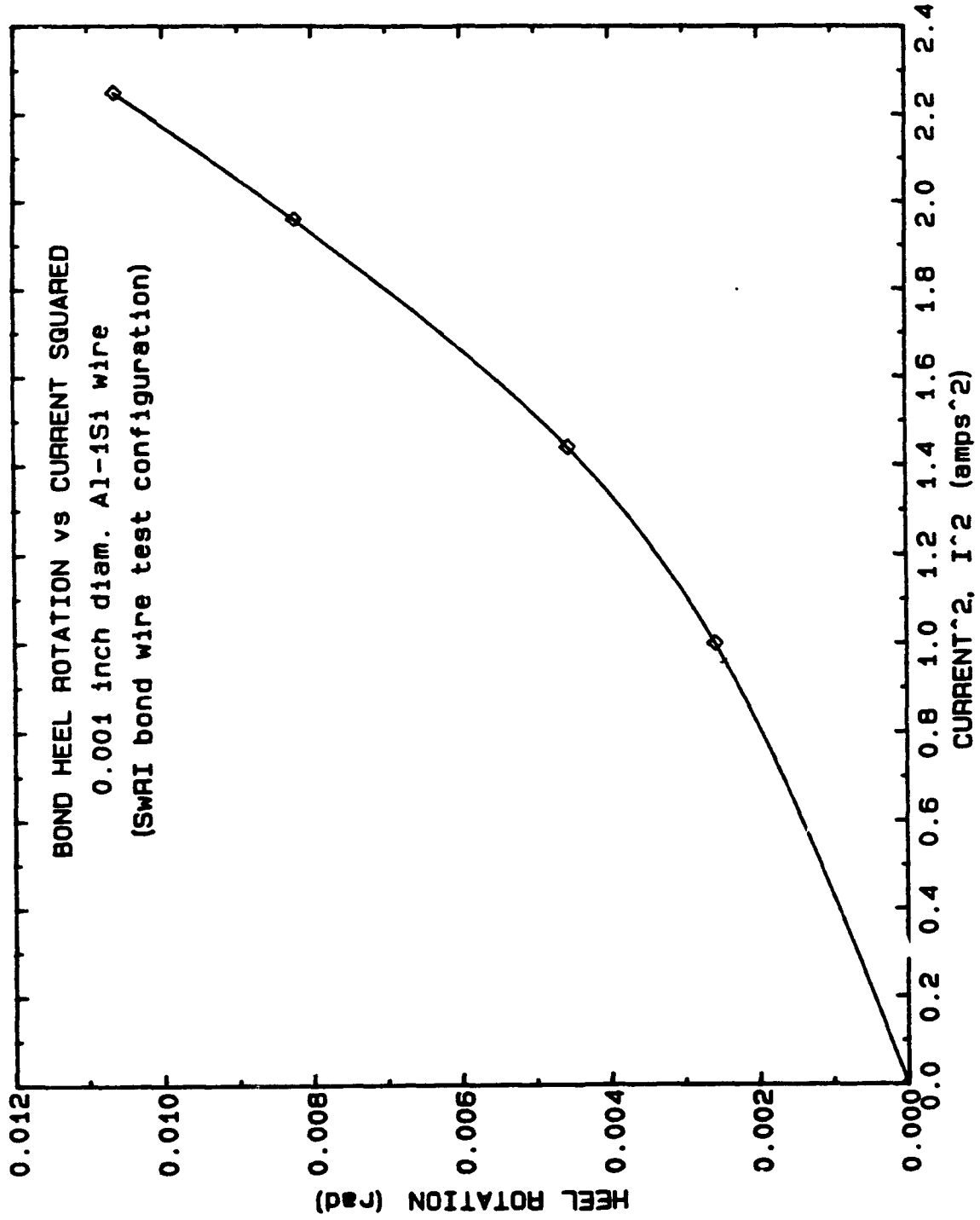

BOND HEEL ROTATION vs CURRENT SQUARED
0.001 inch diam. Al-1Si wire
(SwRI bond wire test configuration)
HEEL ROTATION (rad)
0.000
0.002
0.004
0.006
0.008
0.010
0.012
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.8
2.0
2.2
2.4
CURRENT^2, I^2 (amps^2)
rot_vs_I.plt 07-20-1990

Figure 2.

Figure 15 of Reference 1

Figure 15 of Reference 1

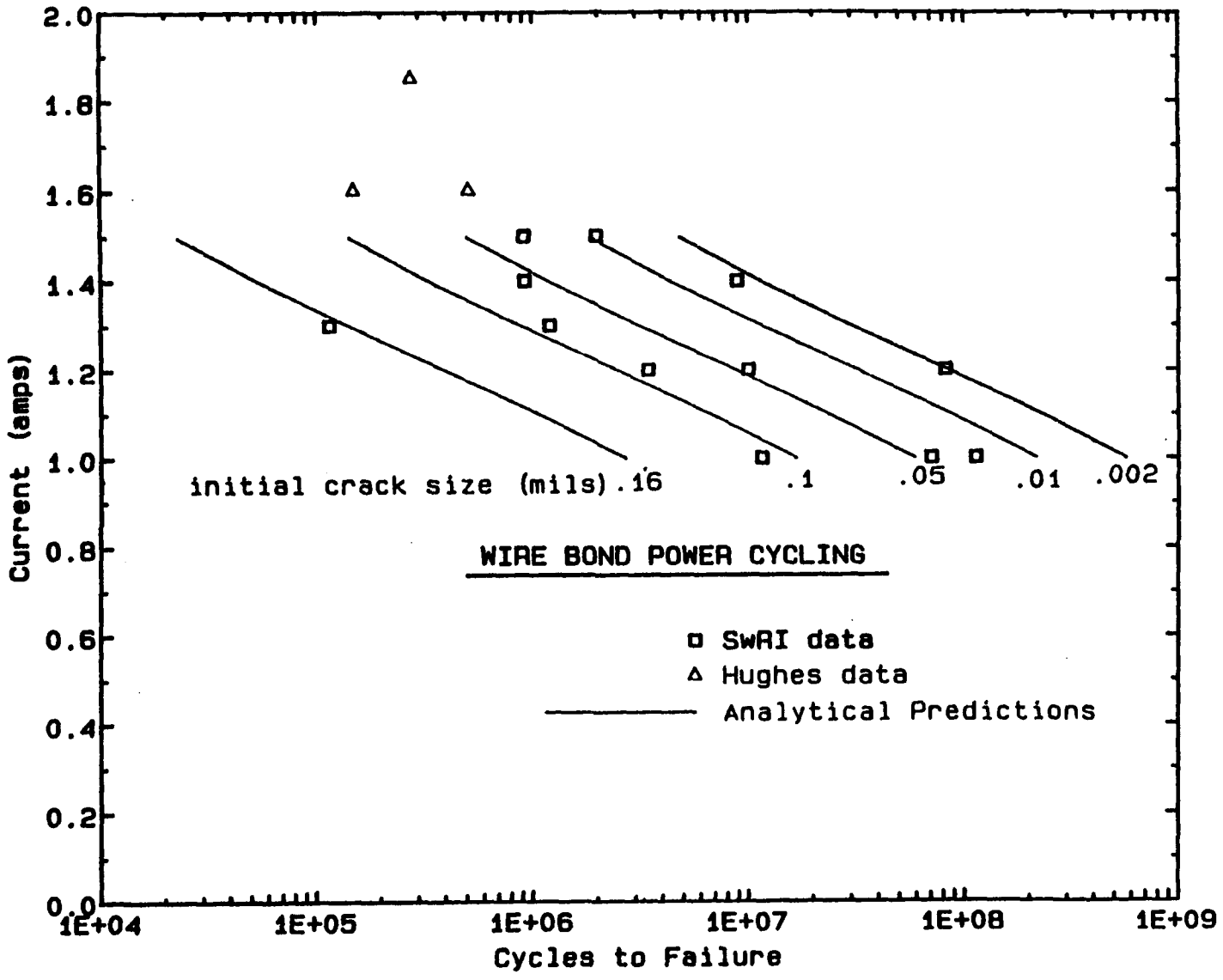


Figure 15. Cycles to failure for different current levels and initial crack depths along with experimental results from Table 2.

SWRI_MPC.DAT 12-14-1990

APPENDIX B

PLATED-THRU-HOLE CERT FFOP PREDICTION

B-1

Fatigue Life Prediction for Digital Module PTHs Subjected to Mil-T test Thermal Cycling

This worksheet is an implementation of the copper plated-through-hole (PTH) thermal cycling low-cycle fatigue equation presented in the IPC technical report, IPC-TR-579, September, 1988 (pg. 42). The equation enables the calculation of PTH cycles to failure for a given total strain range over a thermal cycling temperature range of interest.

1. The following is a calculation of the **Digital** module PTH total strain range for the Mil-T test temperature range of -65C to +125C. It is assumed that the copper PTH complies totally to the expansion of the PWB laminate.

Material Properties

$\alpha_{pwb} = 85 \cdot 10^{-6}$ CTE of PWB (in/in/deg C)
$\alpha_{cu} = 17 \cdot 10^{-6}$ CTE of Copper (in/in/deg C)

$\Delta\alpha = \alpha_{pwb} - \alpha_{cu}$
$6.8 \times 10^{-5} = 6.8 \times 10^{-5}$

Tmax = 125 Max Temperature (deg C)
Tmin = -65 Min Temperature (deg C)

$\Delta T = Tmax - Tmin$
$190 = 190$

Compute total strain range in PTH.

$\Delta e = (\Delta\alpha\Delta T) \cdot 100$ Total strain range in PTH (%)
$1.292 = 1.292$

2. Calculate total strain range in the PTH according to the equations presented in the referenced IPC report (pg. 40). These equations account for relative interaction between the PTH and the surrounding laminate, as well as plasticity in the PTH.

Additional Material Properties

$S_y = 25000$ Copper yield stress (PSI)
$E_e = 500000$ Epoxy elastic modulus (PSI)
$E_{cu} = 16 \cdot 10^6$ Copper elastic modulus (PSI)
$E_{pcu} = 0.1 \cdot 10^6$ Copper plastic (bi-linear) modulus (PSI)

Definitions

$h = 0.1$ PWB laminate thickness (in)

$d = 0.026$ PTH outer diameter (in)

$t = 0.0015$ PTH barrel thickness (in)

$\varepsilon_y = \frac{S_y}{E_{cu}}$ Copper yield strain (in/in)

0.0015625 = 0.0015625

$A_{cu} = \frac{\pi}{4}(d^2 - [d - 2t]^2)$ PTH barrel cross-sectional area (in^2)

0.00011545 = 0.00011545

$A_e = \frac{\pi}{4}([h + d]^2 - d^2)$ Laminate effective cross-sectional area (in^2)

0.011938 = 0.011938

2A. Stress in PTH assuming linear elasticity (PSI)

$$\sigma = \Delta\alpha\Delta T A_e E_e \frac{E_{cu}}{A_e E_e + A_{cu} E_{cu}}$$

$1.5786 \times 10^5 = 1.5786 \times 10^5$

2B. Stress in PTH accounting for yielding (PSI)

$$\sigma_p = \left(\Delta\alpha\Delta T + S_y \frac{E_{cu} - E_{pcu}}{E_{cu} E_{pcu}}\right) A_e E_e \frac{E_{pcu}}{A_e E_e + A_{cu} E_{pcu}}$$

26085 = 26085

Total strain in copper accounting for yielding (in/in, %)

$$\Delta\varepsilon_{cu} = \left(\varepsilon_y + \frac{\sigma_p - S_y}{E_{pcu}}\right) \cdot 100$$

1.2415 = 1.2415

Note that this value is about equal to free thermal strain , FTS (in/in)

$FTS = \Delta\alpha\Delta T$

0.01292 = 0.01292

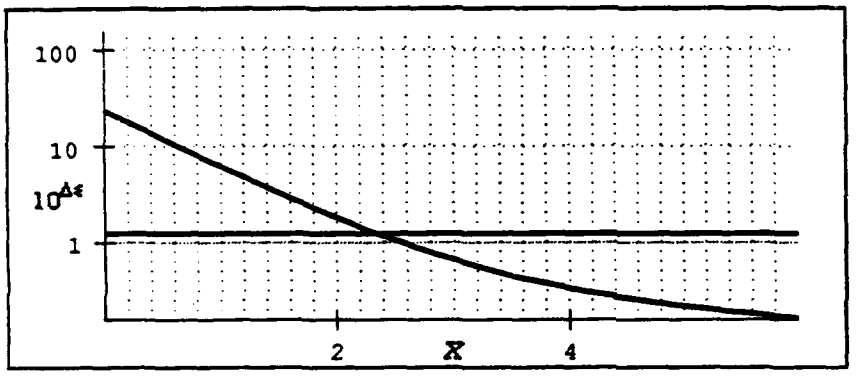
2C. Compute strain-life curve and plot against total strain in PTH

Material Properties

$Su = 3.5 \cdot 10^4$ Copper Ultimate Strength (PSI)

$D_f = 0.14$ Copper Fatigue Ductility

$$\Delta\varepsilon = 100\left[(10^X)^{-0.6} D_f^{0.75} + 0.9\frac{Su}{E_{cu}}\left\{\frac{\exp(D_f)}{0.36}\right\}^{0.1785\log\left(\frac{100000}{10^X}\right)}\right]$$



Graph is a plot of % total strain range vs. cycles to failure (10^X) for the parameter values listed . Also shown is a plot of PTH total strain range (1.24%) which intersects the life curve at approximately X=2.3, or 200 cycles to failure.

B-2

Fatigue Life Prediction for Digital Module PTHs Subjected to CERT Thermal Cycling

This worksheet is an implementation of the copper plated-through-hole (PTH) thermal cycling low-cycle fatigue equation presented in the IPC technical report, IPC-TR-579, September, 1988 (pg. 42). The equation enables the calculation of PTH cycles to failure for a given total strain range over a thermal cycling temperature range of interest.

1. The following is a calculation of the **Digital** module PTH total strain range for the CERT test temperature range of 21C to +105C. It is assumed that the copper PTH complies totally to the expansion of the PWB laminate.

$\alpha_{pwb} = 85 \cdot 10^{-6}$ CTE of PWB (in/in/deg C)

$\alpha_{cu} = 17 \cdot 10^{-6}$ CTE of Copper (in/in/deg C)

$\Delta\alpha = \alpha_{pwb} - \alpha_{cu}$

$6.8 \times 10^{-5} = 6.8 \times 10^{-5}$

$Tmax = 105$ Max Temperature (deg C)

$Tmin = 21$ Min Temperature (deg C)

$\Delta T = Tmax - Tmin$

$84 = 84$

Compute total strain range in PTH.

$\Delta e = (\Delta\alpha\Delta T) \cdot 100$ Total strain range in PTH (%)

$0.5712 = 0.5712$

2. Calculate total strain range in the PTH according to the equations presented in the referenced IPC report (pg. 40). These equations account for relative interaction between the PTH and the surrounding laminate, as well as plasticity in the PTH.

Material Properties

$S_y = 25000$ Copper yield stress (PSI)

$E_e = 500000$ Epoxy elastic modulus (PSI)

$E_{cu} = 16 \cdot 10^6$ Copper elastic modulus (PSI)

$E_{pcu} = 0.1 \cdot 10^6$ Copper plastic (bi-linear) modulus (PSI)

Defintions

$h = 0.1$ PWB laminate thickness (in)

$d = 0.026$ PTH outer diameter (in)

$t = 0.0015$ PTH barrel thickness (in)

$\varepsilon_y = \frac{S_y}{E_{cu}}$ Copper yield strain (in/in)

0.0015625 = 0.0015625

$A_{cu} = \frac{\pi}{4}(d^2 - [d - 2t]^2)$ PTH barrel cross-sectional area (in^2)

0.00011545 = 0.00011545

$A_e = \frac{\pi}{4}([h + d]^2 - d^2)$ Laminate effective cross-sectional area (in^2)

0.011938 = 0.011938

2A. Stress in PTH assuming linear elasticity (PSI)

$$\sigma = \Delta\alpha\Delta T A_e E_e \frac{E_{cu}}{A_e E_e + A_{cu} E_{cu}}$$

69793 = 69793

2B. Stress in PTH accounting for yielding (PSI)

$$\sigma_p = \left(\Delta\alpha\Delta T + S_y \frac{E_{cu} - E_{pcu}}{E_{cu} E_{pcu}}\right) A_e E_e \frac{E_{pcu}}{A_e E_e + A_{cu} E_{pcu}}$$

25366 = 25366

2C. Total strain in copper accounting for yielding (in/in, %)

$$\Delta\varepsilon_{cu} = \left(\varepsilon_y + \frac{\sigma_p - S_y}{E_{pcu}}\right) \cdot 100$$

0.52214 = 0.52214

Note that this value is about equal to free thermal strain, FTS (in/in)

$FTS = \Delta\alpha\Delta T$

0.005712 = 0.005712

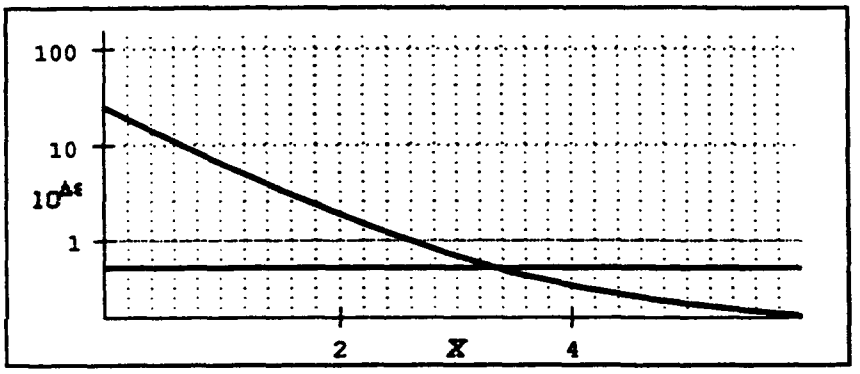
2D. Compute strain-life curve and plot against total (IPC) strain in PTH

Additonal material properties

$D_f = 0.15$ Copper Fatigue Ductility

$Su = 3.5 \cdot 10^4$ Copper Ultimate Strength (PSI)

$$\Delta\varepsilon = 100\left[(10^X)^{-0.6} D_f^{0.75} + 0.9\frac{Su}{E_{cu}}\left\{\frac{\exp(D_f)}{0.36}\right\}^{0.1785\log\left(\frac{100000}{10^X}\right)}\right]$$



Graph is a plot of % total strain range vs. cycles to failure (10^X) for the parameter values listed . Also shown is a plot of PTH total strain range (0.52%) which intersects the life curve at approximately X=3.3, or 1995 cycles to failure.

B-3

Fatigue Life Prediction for Analog Module PTHs Subjected to CERT Thermal Cycling

This worksheet is an implementation of the copper plated-through-hole (PTH) thermal cycling low-cycle fatigue equation presented in the IPC technical report, IPC-TR-579, September, 1988 (pg. 42). The equation enables the calculation of PTH cycles to failure for a given total strain range over a thermal cycling temperature range of interest.

1. The following is a calculation of the **Analog** module PTH total strain range for the CERT temperature range of 21C to +77C. It is assumed that the copper PTH complies totally to the expansion of the PWB laminate.

$\alpha_{pwb} = 85 \cdot 10^{-6}$ CTE of PWB (in/in/deg C)

$\alpha_{cu} = 17 \cdot 10^{-6}$ CTE of Copper (in/in/deg C)

$\Delta\alpha = \alpha_{pwb} - \alpha_{cu}$

$6.8 \times 10^{-5} = 6.8 \times 10^{-5}$

Tmax = 77 Max Temperature (deg C)

Tmin = 21 Min Temperature (deg C)

$\Delta T = Tmax - Tmin$

56 = 56

Compute total strain range in PTH.

$\Delta e = (\Delta\alpha\Delta T) \cdot 100$ Total strain range in PTH (%) assuing the PTH does not restrain the PWB

0.3808 = 0.3808

2. Calculate total strain range in the PTH according to the equations presented in the referenced IPC report (pg. 40). These equations account for relative interaction between the PTH and the surrounding laminate, as well as plasticity in the PTH.

Define material properties

$S_y = 25000$ Copper yield stress (PSI)

$E_e = 500000$ Epoxy elastic modulus (PSI)

$E_{cu} = 16 \cdot 10^6$ Copper elastic modulus (PSI)

$E_{pcu} = 0.1 \cdot 10^6$ Copper plastic (bi-linear) modulus (PSI)

Definitions

$h = 0.036$ PWB laminate thickness (in)

$d = 0.026$ PTH outer diameter (in)

$t = 0.0015$ PTH barrel thickness (in)

$\varepsilon_y = \frac{S_y}{E_{cu}}$ Copper yield strain (in/in)

0.0015625 = 0.0015625

$A_{cu} = \frac{\pi}{4}(d^2 - [d - 2t]^2)$ PTH barrel cross-sectional area (in^2)

0.00011545 = 0.00011545

$A_e = \frac{\pi}{4}([h + d]^2 - d^2)$ Laminate effective cross-sectional area (in^2)

0.0024881 = 0.0024881

2A. Stress in PTH assuming linear elasticity (PSI)

$$\sigma = \Delta\alpha\Delta T A_e E_e \frac{E_{cu}}{A_e E_e + A_{cu} E_{cu}}$$

24520 = 24520

2B. Stress in PTH accounting for yielding (PSI)

$$\sigma_p = \left(\Delta\alpha\Delta T + S_y \frac{E_{cu} - E_{pcu}}{E_{cu} E_{pcu}}\right) A_e E_e \frac{E_{pcu}}{A_e E_e + A_{cu} E_{pcu}}$$

24993 = 24993

2C. Total strain in copper accounting for yielding (in/in, %)

$$\Delta\varepsilon_{cu} = 100\left(\varepsilon_y + \frac{\sigma_p - S_y}{E_{pcu}}\right)$$

0.14886 = 0.14886

Note that this value is much less than the free thermal strain, FTS (in/in, %)

$FTS = (\Delta\alpha\Delta T) \cdot 100$

0.3808 = 0.3808

2D. Compute strain-life curve

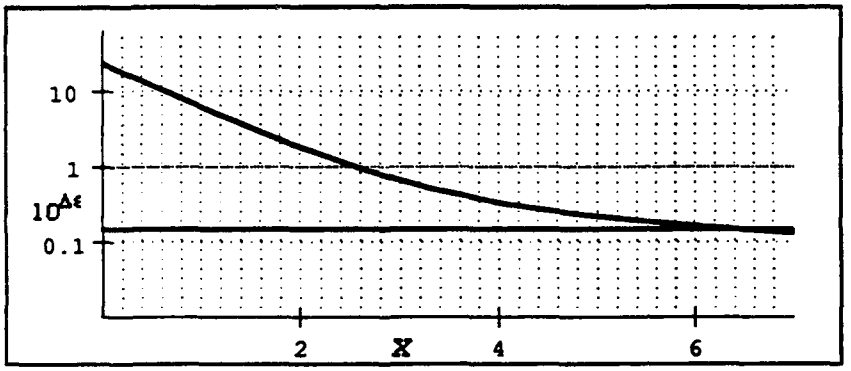
Define additional material properties

$Su = 3.5 \cdot 10^4$ Copper Ultimate Strength (PSI)

$D_f = 0.14$ Copper Fatigue Ductility

$$\Delta\epsilon = 100\left\{(10^X)^{-0.6} D_f^{0.75} + 0.9\frac{Su}{E_{cu}}\left\{\frac{\exp(D_f)}{0.36}\right\}^{0.1785\log\left(\frac{100000}{10^X}\right)}\right\}$$

Plot strain-life curve against (IPC) total strain in PTH



Graph is a plot of % total strain range vs. cycles to failure (10^X) for the parameter values listed . Also shown is a plot of (IPC) PTH total strain range (0.14%) which intersects the life curve at approximately X=6.4, or 2.5 million cycles to failure.

ATTACHMENT IV

FFOP PREDICTION
FOR
CONTAMINATION-INDUCED FAILURES

INTERDEPARTMENTAL CORRESPONDENCE

TO: J.M. Kallis
ORG: 72-26

C: D.W. Buechler
J.L. Cook
M.D. Norris
D.H. Van Westerhuyzen
J.A. Zelik

DATE: 28 January 1991
REF: 7641.20/2011

SUBJECT: FFOP Predictions for the ERFM Program

FROM: J.J. Erickson
ORG: 76-41-20

BLDG. E1 MAIL STA. C132
LOC. EO PHONE 66579

SUMMARY

Based on the experimental data obtained from the Hybrid Contamination Screen plus the model that has been developed for mobile ionic contamination, it is predicted that the negative voltage regulator hybrids will not fail due to either mobile ionic contamination or surface contamination during the CERT (Combined Environments Reliability Test) that is performed for the ERFM (Electronic Reliability Fracture Mechanics) Program. Therefore, the predicted FFOP (Failure Free Operating Period) for these mechanisms in the hybrids is infinite.

BACKGROUND

As part of the ERFM Program, some P/N 3569800 negative voltage regulator hybrids that failed in the field were analyzed and determined to have failed due to mobile ionic contamination. The mobile ionic contamination caused the gain of one of a pair of matched PNP transistors in the hybrid to decrease. This, in turn, caused the output voltage of the hybrid to become more negative to a point where the module containing the hybrid failed.

Other failed negative regulator hybrids were determined to have failed from surface contamination which caused the resistance of a thick film resistor in the hybrid to decrease. This resulted in the hybrid output voltage becoming less negative until the module containing the hybrid failed.

Figure 1 shows the circuit schematic for the negative regulator hybrid. The matched pair of transistors are Q1 and Q2. The resistor that was affected by the surface contamination is R1.

HYBRID CONTAMINATION SCREEN

Ten negative regulator hybrids were built for this program. These hybrids were subjected to a series of tests referred to as the Hybrid Contamination Screen. These tests included biased bakes (both reverse bias and normal bias conditions) and unbiased bakes in order to determine whether these devices would tend to exhibit any indication of the mobile ionic contamination or surface contamination

failure mechanisms. Following each test in the series, the parameters for the hybrids were recorded along with additional electrical data for each hybrid. The devices were also monitored for indications of these specific failure mechanisms plus any indications of any other problems that might have been exacerbated by these tests.

The Hybrid Contamination Screen resulted in the output voltage of nine of the ten hybrids becoming more negative indicating that these devices were being affected by mobile ionic contamination. Figures 2A through 2C are graphs showing the output voltages of the ten hybrids at each step in the Hybrid Contamination Screen. There was a wide range in the magnitude of the voltage change with some devices staying within specification limits while others were well beyond the limits. This indicates a wide range of the amount of contaminant within the different devices. The devices tended to reach their worst output voltage condition after the HTRB (high temperature reverse bias) test which was the first test in the sequence of tests. Those devices that had the largest voltage changes after the HTRB test recovered slightly in subsequent tests, but those devices which had smaller changes after the HTRB test were relatively stable throughout the rest of the series of tests. The devices were subjected to a total of about 450 hours at 125°C with 48 hours of these under HTRB conditions.

The hybrids selected for location U2 in the specially fabricated/ inspected SRUs are S/Ns 7941 (Figure 2B) and 8355 (Figure 2C). (All of the field failures analyzed were U2 hybrids.) For both of these S/Ns, the HTRB caused the output voltage to shift more than the amount allowed by the hybrid specification (0.06V) but less than the allowable amount at the module level (0.25V). In other words, the hybrid output voltage shift was not large enough to cause a module failure.

The hybrids selected for location U3 are S/Ns 8872 (Figure 2A) and 8388 (Figure 2B). The HTRB caused the output voltage of these S/Ns to shift 0.12V.

The Hybrid Contamination Screen did not reveal any indication of the surface contamination problem. None of the hybrids output voltages became less negative. Also, the value of the resistor which is critically affected by this mechanism was monitored following each test. No significant changes in the value of this resistor (or any of the other accessible resistors) were noted at any point in the Screen.

IONIC CONTAMINATION MODEL

A model was developed for mobile ionic contamination in order to predict the behavior of the hybrids under various operating conditions. The mobile ionic contamination causes changes in the

gain of one transistor of a matched transistor pair in the hybrid which, in turn, causes changes in the hybrid's performance. Figures 3 and 4 show a photograph of one of these transistors and a drawing representing the cross-section of the transistor. This model assumes that the mobile ionic contaminant is sodium that had been introduced under the transistor's metallization during the metallization deposition. The base-emitter junction which is affected by the contamination is initially separated from the sodium by one micron of silicon dioxide glass. (Figure 5 is a diagram representing the area over the base-emitter junction previously discussed.) As time passes, the sodium diffuses through the glass toward the base-emitter junction. Initially, when the sodium is near the glass/metallization interface it has little effect on the base-emitter junction. However, as it diffuses into the glass and gets closer to the junction, it has a larger effect and begins to induce a significant amount of charge in the silicon. The model calculates the amount of surface charge induced in the silicon for a given distribution of sodium ions in the glass.

The induced surface charge in the silicon produces degradation of the transistor's gain. This, in turn, causes a change in the hybrid output voltage which has been determined by a computer circuit simulation.

Figure 6 is a graph generated from the model showing the relative amount of surface charge induced in the silicon versus time for various temperatures under conditions of normal hybrid bias or no bias. For a particular initial sodium ion concentration, the time required for this to have its maximum effect even at a temperature of 125^{o}C would be several thousand hours under conditions of normal hybrid bias or no bias.

However, the HTRB test performed in the Hybrid Contamination Screen caused a large change in the hybrid performance in only 48 hours of reverse bias. Also, additional temperature exposure under conditions of no bias or normal bias did not result in any further degradation of the hybrids; in some cases, it improved their behavior. Obviously, the reverse bias condition has accelerated the diffusion of the sodium.

In the case of the unbiased transistor, the sodium ions will tend to diffuse due to concentration gradients until an equilibrium condition is reached where the sodium ions are evenly distributed throughout the glass. At this point, the distribution of the ions can be represented in the model by a layer of sodium ions halfway between the metal and the silicon, inducing a charge in the silicon equal to one half the charge on the sodium ions. This would represent the worst case condition for that particular transistor. If at this point the hybrid voltage output is within specification limits, it will never get any worse due to mobile ionic contamination in the transistor.

However, if the transistor is subjected to reverse bias conditions, a field can be induced in the oxide (and also at the surface of the silicon) that will tend to drive the sodium ions beyond their unbiased equilibrium condition. That is, a distribution could be generated where the "average position" of the sodium ions is represented by a layer of sodium ions that is beyond the halfway point or closer to the silicon than in the nonbiased case. Apparently, this is what occurred in the HTRB that was performed on the hybrids. The sodium ions were driven beyond the halfway point and then with additional time, proceeded to recover slightly when the "average position" of the sodium ions moved away from the silicon.

The model for the mobile sodium ion concentration was modified to include the effect of a reverse bias field. This modification predicted that the HTRB time of 48 hours at 125°C would drive the sodium ions beyond the halfway point as illustrated in the graph shown in Figure 7.

Therefore, based on both the results of the Hybrid Contamination Screen and the mobile ionic contamination model that has been developed, it appears that at this point the sodium in the transistors has been driven to the point where it has the worst effect and the hybrid outputs will never get any worse due to this failure mechanism. There is even a small possibility that they will get slightly better.

SURFACE CONTAMINATION

A model for the surface contamination failure mechanism has been developed which is similar to the ionic contamination model. In the model for surface contamination, a contaminant diffuses or migrates to a location where it is bridging portions of a thick film resistor which are normally isolated. Initially, the sketch that was used for this model showed a serpentine resistor pattern with the contaminant bridging portions of the pattern. It has been modified to show contaminant bridging a laser trim line as illustrated in the sketch in Figure 8. The basic mechanism is still the same; surface contamination bridges an area that is normally not part of the conductive area of the resistor and reduces the resistance.

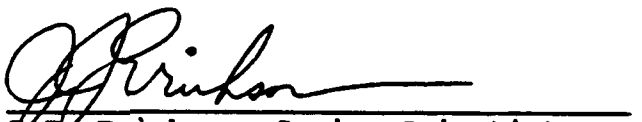
Unlike the ionic contamination failures, little quantitative data is available for the surface contamination model. Some of the failures from the field that exhibited this failure mechanism were baked during the analysis. Following the bake, the devices no longer exhibited the failure and could not be induced by testing to fail. Other devices exhibited the failure mode when initially tested but then recovered and then could not be induced by additional testing to fail. Analysis of the materials in the hybrids at the location of the resistors did not reveal any anomalous materials or contaminants. Also, the Hybrid Contamination Screen did not reveal any evidence of

this failure mode in the hybrids built for this program. Therefore, the model for this mechanism is only outlined at this point with very little detail available for a precise calculation of a FFOP. Specifically, the contaminants and their diffusion constants and conductivities are unknown.

However, no indication of the surface contamination failure mechanism has been detected in the hybrids after 450 hours of testing at elevated temperatures during the Hybrid Contamination Screen. Therefore, it is concluded that the hybrids built for this program will not fail due to the surface contamination mechanism.

CONCLUSION

Based on test data from the Hybrid Contamination Screen plus the model that has been developed for mobile ionic contamination, it is predicted that the negative voltage regulator hybrids will not fail due to either mobile ionic contamination or surface contamination during the CERT that is performed for the ERFM program.



J.J. Erickson, Senior Scientist
Reliability Physics Department

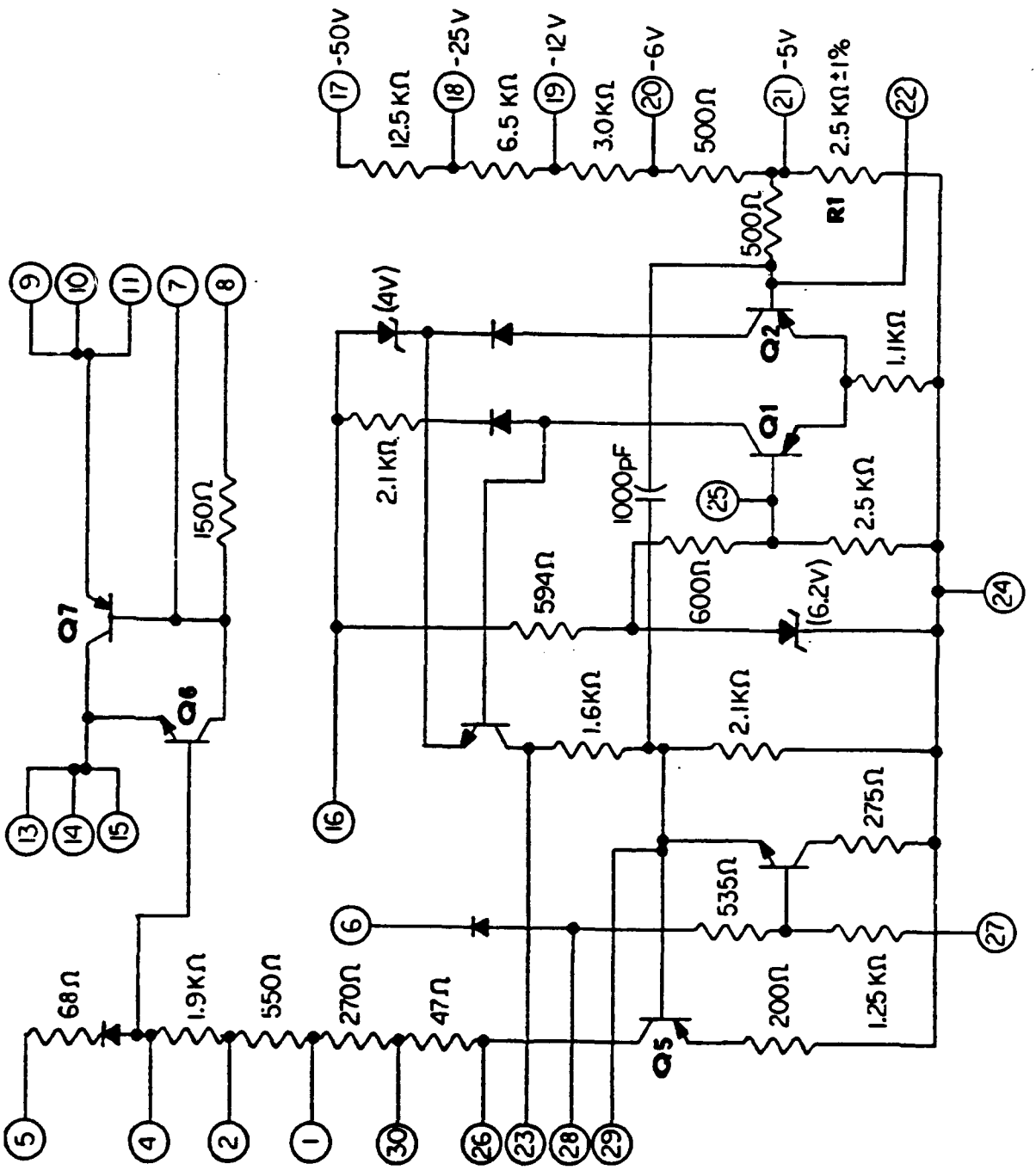


FIGURE 1. SCHEMATIC DIAGRAM FOR THE HYBRID.

FIGURE 2A

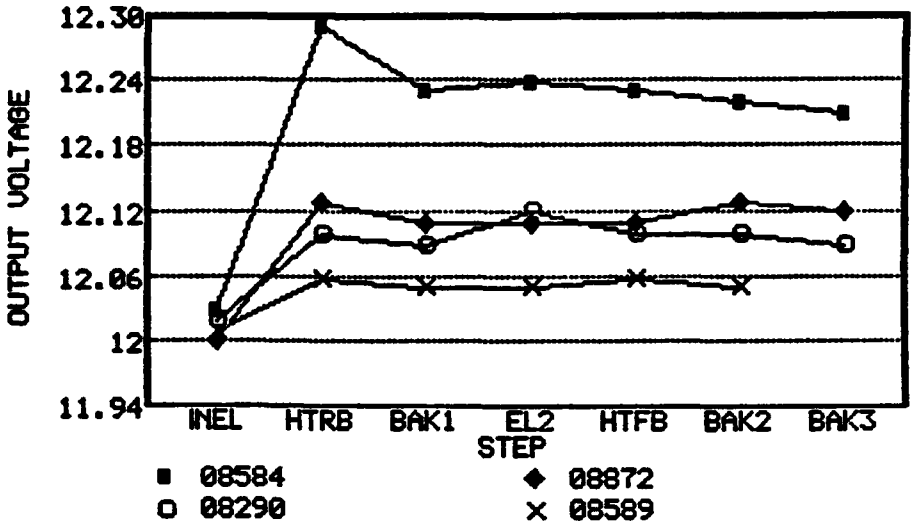


FIGURE 2B

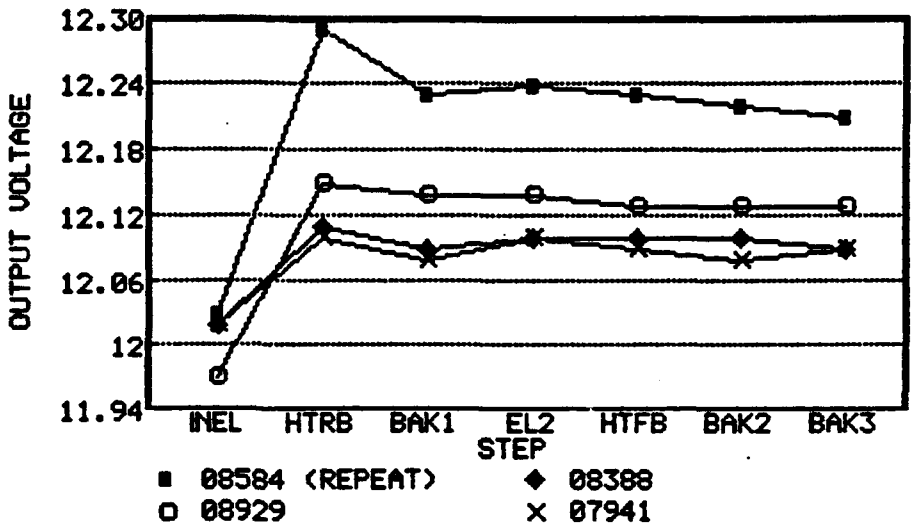
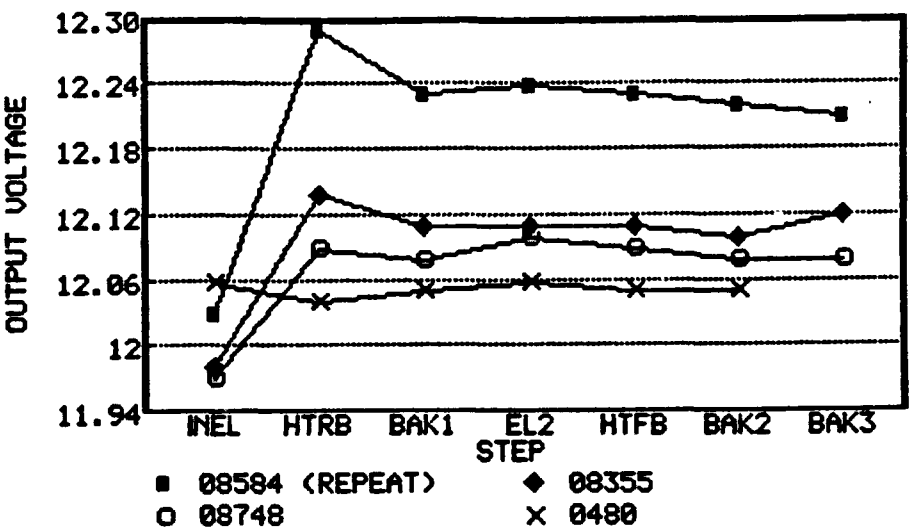


FIGURE 2C



GRAPHS OF OUTPUT VOLTAGE FOR EACH HYBRID S/N AT EACH STEP IN THE HYBRID CONTAMINATION SCREEN.

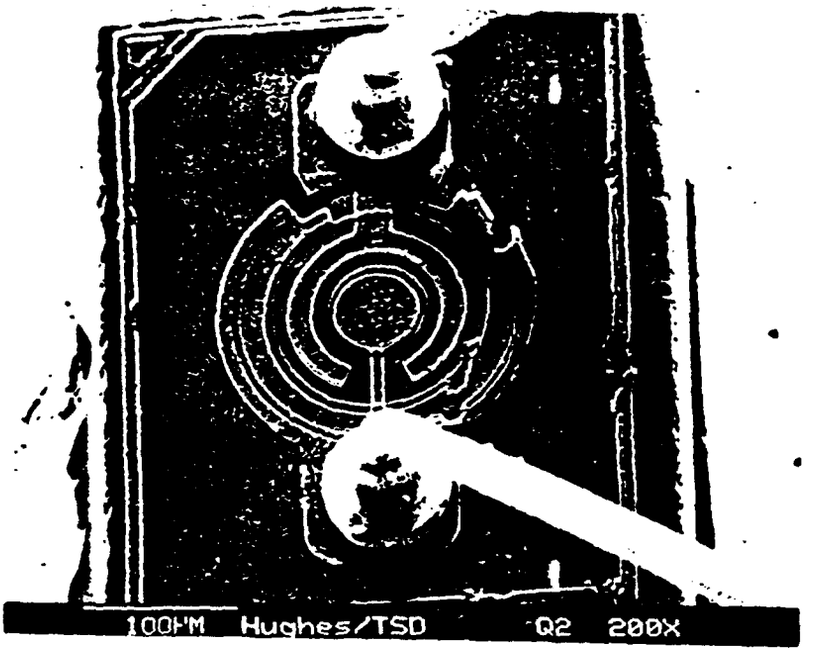


FIGURE 3. SEM (Scanning Electron Microscope) photograph of one of the transistors in the matched pair.

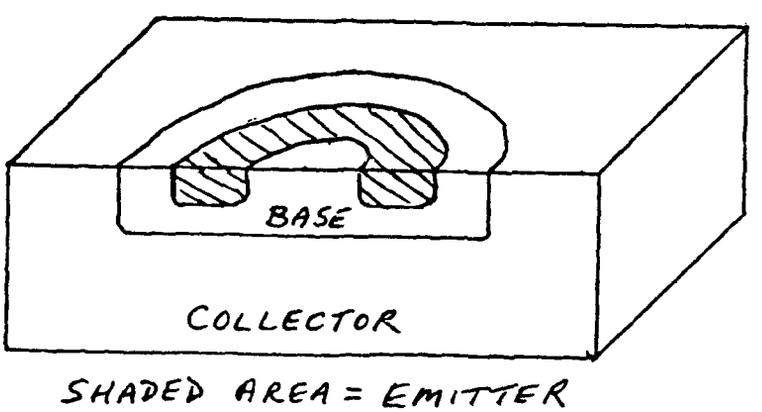


FIGURE 4. Drawing of transistor cross-section (not to scale).

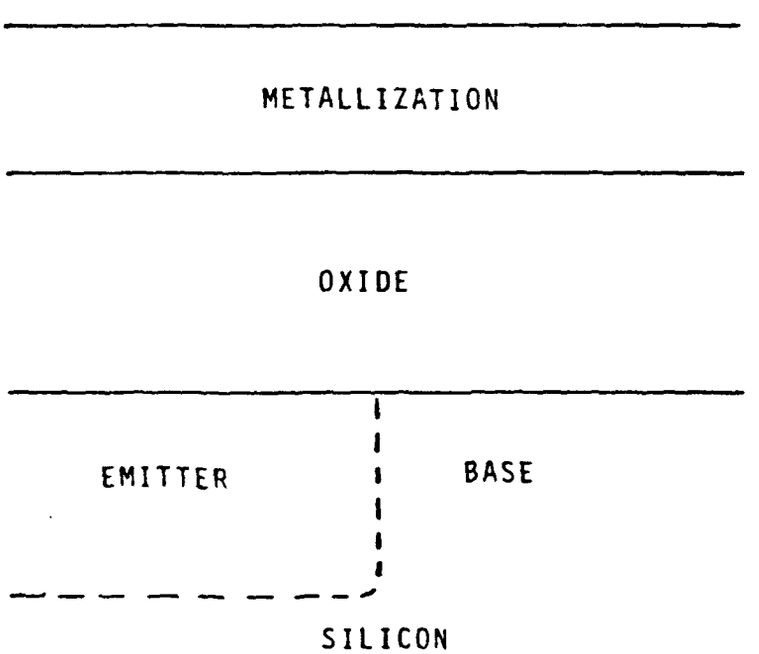


FIGURE 5. Drawing of area over base-emitter junction (not to scale).

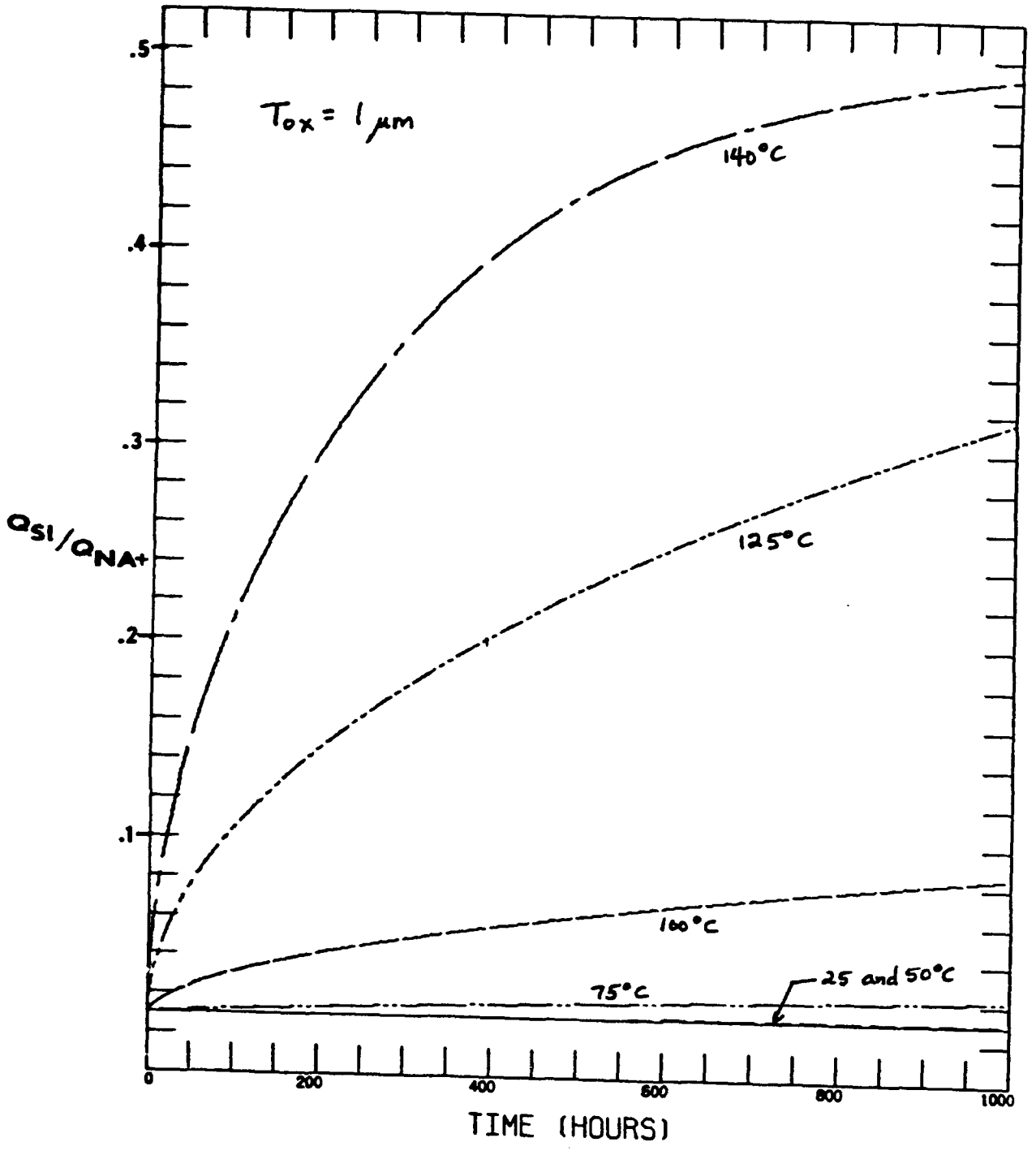


FIGURE 6. OUTPUT FROM COMPUTERIZED MODEL OF SODIUM ION DIFFUSION. Q_{SI}/Q_{NA+} (CHARGE INDUCED IN SILICON (Q_{SI}) NORMALIZED TO INITIAL SODIUM ION CONCENTRATION (Q_{NA+})) VERSUS TIME FOR VARIOUS TEMPERATURES IS PLOTTED. OXIDE THICKNESS (T_{OX}) IS ONE MICRON.

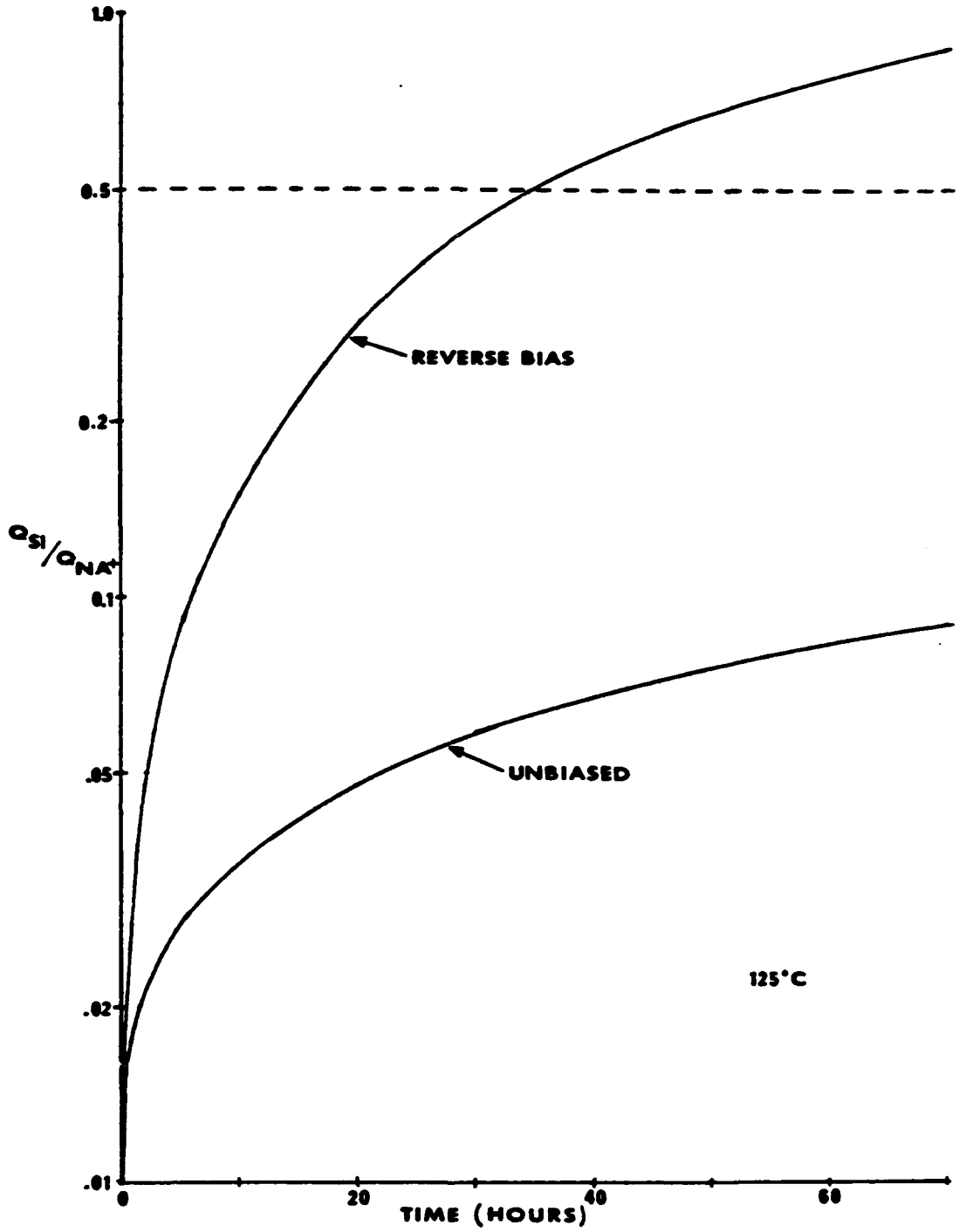


FIGURE 7. PLOT OF DATA FROM MODEL OF SODIUM ION DIFFUSION COMPARING REVERSE BIASED OPERATION TO UNBIASED (OR NORMAL BIAS) OPERATION. FOR UNBIASED OPERATION, THE CURVE ASYMPTOTICALLY APPROACHES Q_{SI}/Q_{NA+} = 0.5. UNDER REVERSE BIASED OPERATION, THE CURVE CROSSES THIS POINT AT ABOUT 35 HOURS.

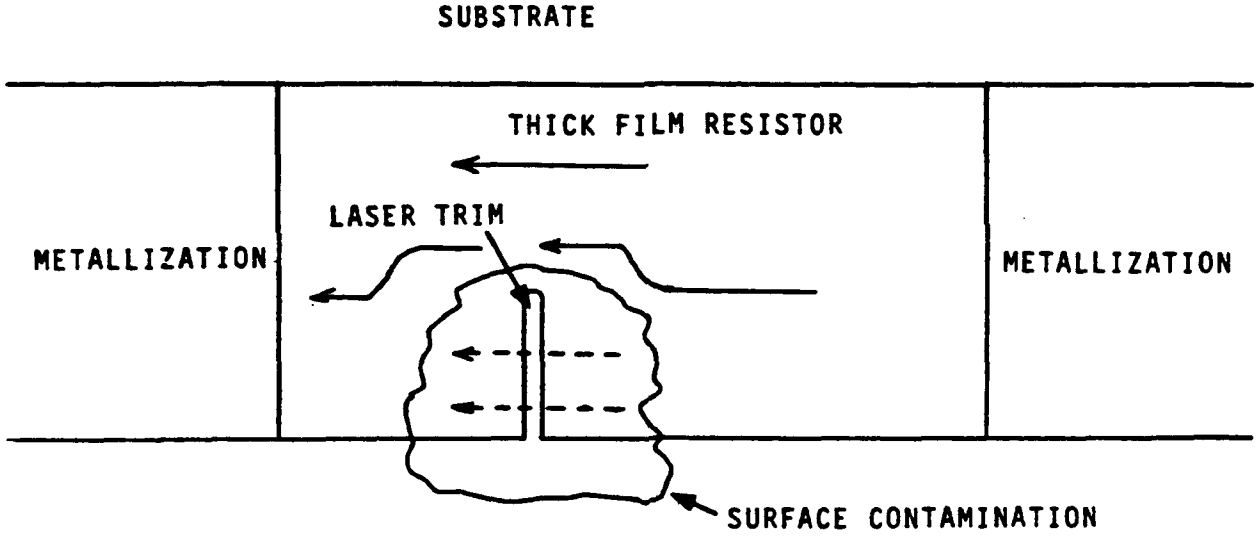


FIGURE 8. DRAWING OF SURFACE CONTAMINATION ON THICK FILM RESISTOR. SOLID ARROWS INDICATE NORMAL CURRENT FLOW. DASHED ARROWS INDICATE ANOMALOUS CURRENT FLOW CAUSED BY SURFACE CONTAMINATION.

APPENDIX U

CERT FFOP PREDICTIONS FOR SEVERAL TEMPERATURE RANGES

INTERDEPARTMENTAL CORRESPONDENCE

To: J.M. Kallis
Org: 72-26

c: Distribution

Date: 1 April 1991
Ref: 722630/1333

Subject: ERFM CERT FFOP Predictions for Several Temperature Ranges

From: L.B. Duncan
Org: 72-26-30

Bldg: E01 **MS:** D102
Loc: EO **Phone:** 616-0924

Failure Free Operating Period (FFOP) predictions were made for F15 Digital and Analog modules undergoing Combined Environments Reliability Test (CERT) as part of the Electronics Reliability Fracture Mechanics (ERFM) program (Reference 1). Specifically, fatigue life predictions were made for plated-through-holes (PTHs) and 1 mil diameter interconnect wires undergoing thermal cycling for maximum predicted component and printed wiring board (PWB) surface temperatures. In the present analysis, additional PTH fatigue life predictions are made for temperature ranges of 79, 74, and 69°C which are 5, 10, and 15 °C less than the maximum temperature range predicted by analysis (Reference 2). The present analysis was performed to assess the increase in Digital module FFOP that would result if maximum expected temperatures were not achieved in the CERT. The FFOP predictions are as follows:

ΔT (°C)	Nf (cycles)	FFOP (cycles)
84	1995	1000
79	2512	1300
74	3162	1600
69	3981	2000

where

(1) Nf = predicted cycles to failure
(2) FFOP = Nf / 2 and rounded up to the nearest 100 cycles

It is seen that a decrease of 15°C in the temperature range approximately doubles the FFOP. The sensitivity of FFOP to ΔT is plotted in Figure 2.

LB Duncan

L.B. Duncan, Senior Scientist
Structural Mechanics Department
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ERFM CERT FFOP PREDICTIONS FOR SEVERAL TEMPERATURE RANGES

IDC 722630/1333

1 APRIL 1991

Prepared by: L B Duncan
L.B. Duncan, Senior Scientist

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Hughes Aircraft Company, El Segundo, California

1.0 INTRODUCTION

Failure Free Operating Period (FFOP) predictions were made for F15 Digital and Analog modules undergoing Combined Environments Reliability Test (CERT) as part of the Electronics Reliability Fracture Mechanics (ERFM) program (Reference 1). Specifically, fatigue life predictions were made for plated-through-holes (PTHs) and 1 mil diameter interconnect wires undergoing thermal cycling for maximum predicted component and printed wiring board (PWB) surface temperatures. In the present analysis, additional PTH fatigue life predictions are made for temperature ranges of 79, 74, and 69°C which are 5, 10, and 15 °C less than the maximum temperature range predicted by analysis (Reference 2). The present analysis was performed to assess the increase in Digital module FFOP that would result if maximum expected temperatures were not achieved in the CERT.

2.0 SUMMARY

The FFOP predictions for PTH fatigue failure in the Digital modules are as follows:

ΔT (°C)	N_f (cycles)	FFOP (cycles)
84	1995	1000
79	2512	1300
74	3162	1600
69	3981	2000

where

(1) Nf = predicted cycles to failure
(2) FFOP = Nf / 2 and rounded up to the nearest 100 cycles

It is seen that a decrease of 15°C in the temperature range approximately doubles the FFOP. The sensitivity of FFOP to ΔT is plotted in Figure 2.

3.0 CERT THERMAL CYCLING ENVIRONMENT

The CERT thermal cycling environment is shown in Figure 1. The powered portion of the profile specifies a 63°C coolant inlet temperature. The powered condition is followed by transient periods wherein the inlet temperature of the coolant is reduced to 21°C, held for 60 minutes, then raised to 63°C and held for 60 minutes.

CERT transient thermal analyses were performed to predict component and mounting surface temperatures for the digital modules (Reference 2). The maximum junction temperature for the digital module was 134°C under component 932820, U1508. The maximum mounting surface temperatures was 105°C under component 905570-73B, C151.

In the present analysis, PTH life was predicted for maximumm temperatures of 5, 10, and 15°C below the predicted 105°C maximum surface temperature.

4.0 REFERENCES

1. IDC 722630/1284, *ERFM CERT FFOP Predictions,* L.B. Duncan to J.M. Kallis, 18 December 1990.

2. IDC 722620/1570, *Transient Thermal Analysis of the F-15 PSP Timing and Control Module*, W.J. Hoskins to J.M. Kallis, 9 April 1990.

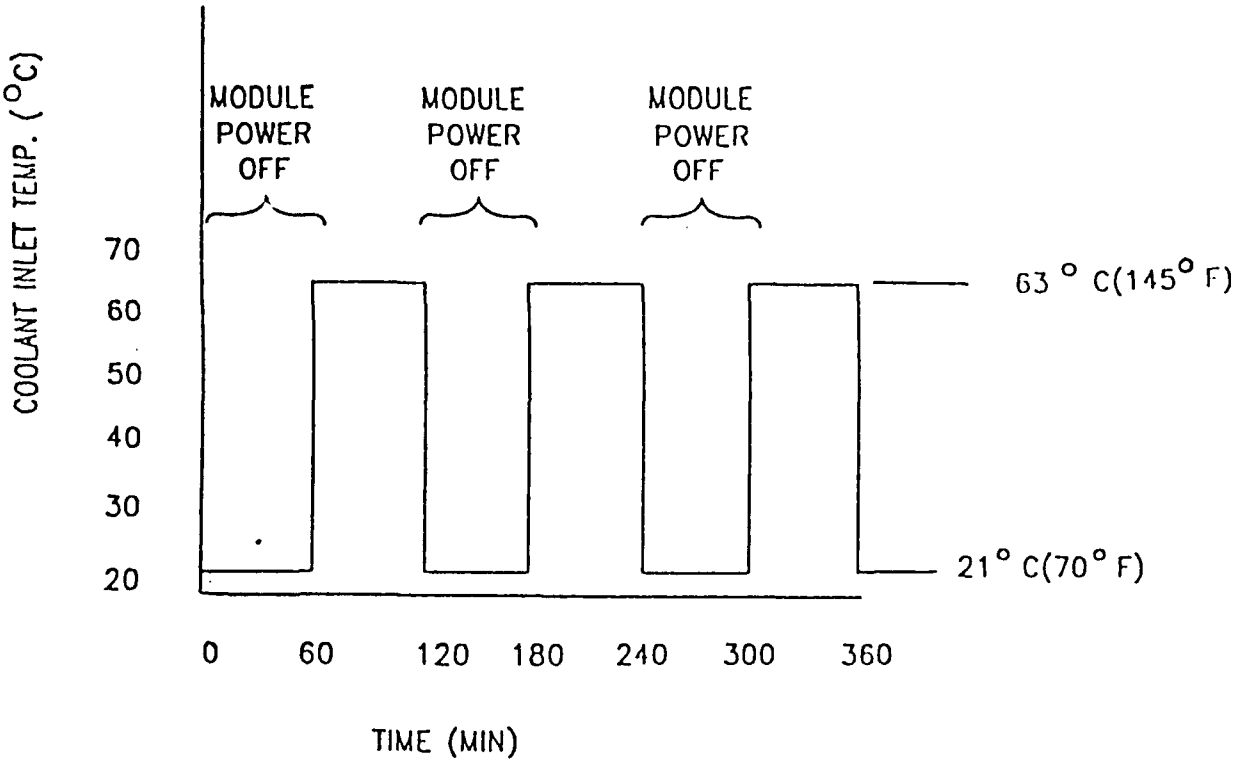


Figure U-1. CERT Environmental Profile

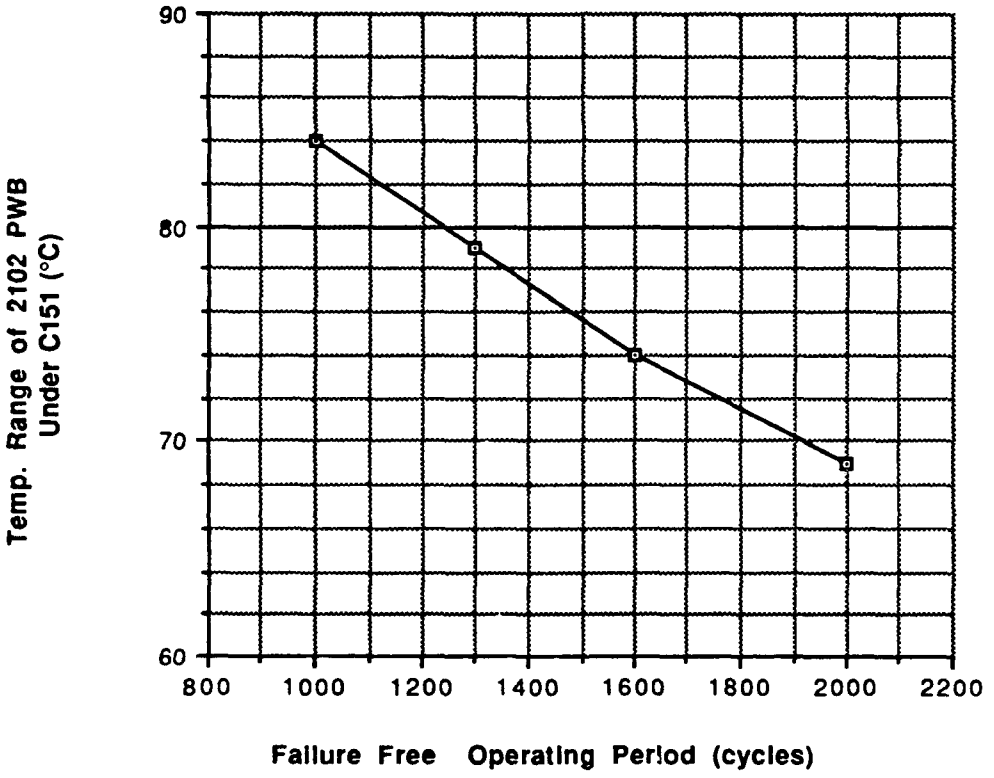


Figure U-2. Sensitivity of FFOP to ΔT in CERT Thermal Cycle

APPENDIX A

DIGITAL MODULE
PLATED-THRU-HOLE CERT FFOP PREDICTION

A-1

Fatigue Life Prediction for Digital Module PTHs Subjected to CERT Thermal Cycling from 21°C to 100°C (ΔT=79°C)

This worksheet is an implementation of the copper plated-through-hole (PTH) thermal cycling low-cycle fatigue equation presented in the IPC technical report, IPC-TR-579, September, 1988 (pg. 42). The equation enables the calculation of PTH cycles to failure for a given total strain range over a thermal cycling temperature range of interest.

1. The following is a calculation of the **Digital** module PTH total strain range for the CERT test temperature range of 21C to +100C. It is assumed that the copper PTH complies totally to the expansion of the PWB laminate.

$\alpha_{pwb} = 85 \cdot 10^{-6}$ CTE of PWB (in/in/deg C)

$\alpha_{cu} = 17 \cdot 10^{-6}$ CTE of Copper (in/in/deg C)

$\Delta\alpha = \alpha_{pwb} - \alpha_{cu}$

$6.8 \times 10^{-5} = 6.8 \times 10^{-5}$

Tmax = 100 Max Temperature (deg C)

Tmin = 21 Min Temperature (deg C)

$\Delta T = Tmax - Tmin$

79 = 79

Compute total strain range in PTH.

$\Delta e = (\Delta\alpha \Delta T) \cdot 100$ Total strain range in PTH (%)

0.5372 = 0.5372

2. Calculate total strain range in the PTH according to the equations presented in the referenced IPC report (pg. 40). These equations account for relative interaction between the PTH and the surrounding laminate, as well as plasticity in the PTH.

Material Properties

$S_y = 25000$ Copper yield stress (PSI)

$E_e = 500000$ Epoxy elastic modulus (PSI)

$E_{cu} = 16 \cdot 10^6$ Copper elastic modulus (PSI)

$E_{pcu} = 0.1 \cdot 10^6$ Copper plastic (bi-linear) modulus (PSI)

Defintions

$h = 0.1$ PWB laminate thickness (in)

$d = 0.026$ PTH outer diameter (in)

$t = 0.0015$ PTH barrel thickness (in)

$\varepsilon_y = \frac{S_y}{E_{cu}}$ Copper yield strain (in/in)

0.0015625 = 0.0015625

$A_{cu} = \frac{\pi}{4}(d^2 - [d - 2t]^2)$ PTH barrel cross-sectional area (in^2)

0.00011545 = 0.00011545

$A_e = \frac{\pi}{4}([h + d]^2 - d^2)$ Laminate effective cross-sectional area (in^2)

0.011938 = 0.011938

2A. Stress in PTH assuming linear elasticity (PSI)

$$\sigma = \Delta\alpha\Delta T A_e E_e \frac{E_{cu}}{A_e E_e + A_{cu} E_{cu}}$$

65639 = 65639

2B. Stress in PTH accounting for yielding (PSI)

$$\sigma_p = \left(\Delta\alpha\Delta T + S_y \frac{E_{cu} - E_{pcu}}{E_{cu} E_{pcu}}\right) A_e E_e \frac{E_{pcu}}{A_e E_e + A_{cu} E_{pcu}}$$

25332 = 25332

2C. Total strain in copper accounting for yielding (in/in, %)

$$\Delta\varepsilon_{cu} = \left(\varepsilon_y + \frac{\sigma_p - S_y}{E_{pcu}}\right) \cdot 100$$

0.4882 = 0.4882

Note that this value is about equal to free thermal strain, FTS (in/in)

FTS = $\Delta\alpha\Delta T$

0.005372 = 0.005372

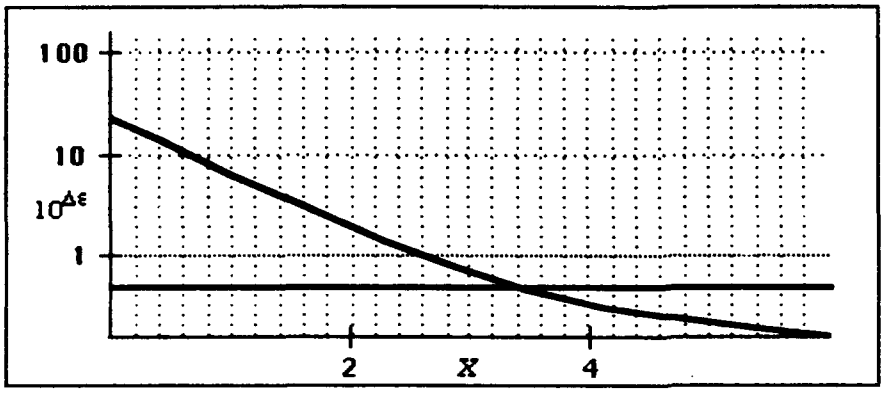
2D. Compute strain-life curve and plot against total (IPC) strain in PTH

Additonal material properties

D_f = 0.15 Copper Fatigue Ductility

$Su = 3.5 \cdot 10^4$ Copper Ultimate Strength (PSI)

$$\Delta\varepsilon = 100\left\{(10^X)^{-0.6} D_f^{0.75} + 0.9\frac{Su}{E_{cu}}\left\{\frac{\exp(D_f)}{0.36}\right\}^{0.1785\log\left(\frac{100000}{10^X}\right)}\right\}$$



Graph is a plot of % total strain range vs. cycles to failure (10^X) for the parameter values listed . Also shown is a plot of PTH total strain range (0.49%) which intersects the life curve at approximately X=3.4, or 2512 cycles to failure.

A-2

Fatigue Life Prediction for Digital Module PTHs Subjected to CERT Thermal Cycling from 21°C to 95°C (ΔT=74°C)

This worksheet is an implementation of the copper plated-through-hole (PTH) thermal cycling low-cycle fatigue equation presented in the IPC technical report, IPC-TR-579, September, 1988 (pg. 42). The equation enables the calculation of PTH cycles to failure for a given total strain range over a thermal cycling temperature range of interest.

1. The following is a calculation of the **Digital** module PTH total strain range for the CERT test temperature range of 21C to +95C. It is assumed that the copper PTH complies totally to the expansion of the PWB laminate.

$\alpha_{pwb} = 85 \cdot 10^{-6}$ CTE of PWB (in/in/deg C)

$\alpha_{cu} = 17 \cdot 10^{-6}$ CTE of Copper (in/in/deg C)

$\Delta\alpha = \alpha_{pwb} - \alpha_{cu}$

$6.8 \times 10^{-5} = 6.8 \times 10^{-5}$

Tmax = 95 Max Temperature (deg C)

Tmin = 21 Min Temperature (deg C)

$\Delta T = Tmax - Tmin$

$74 = 74$

Compute total strain range in PTH.

$\Delta e = (\Delta\alpha\Delta T) \cdot 100$ Total strain range in PTH (%)

$0.5032 = 0.5032$

2. Calculate total strain range in the PTH according to the equations presented in the referenced IPC report (pg. 40). These equations account for relative interaction between the PTH and the surrounding laminate, as well as plasticity in the PTH.

Material Properties

$S_y = 25000$ Copper yield stress (PSI)

$E_e = 500000$ Epoxy elastic modulus (PSI)

$E_{cu} = 16 \cdot 10^6$ Copper elastic modulus (PSI)

$E_{pcu} = 0.1 \cdot 10^6$ Copper plastic (bi-linear) modulus (PSI)

Defintions

$h = 0.1$ PWB laminate thickness (in)

$d = 0.026$ PTH outer diameter (in)

$t = 0.0015$ PTH barrel thickness (in)

$\varepsilon_y = \frac{S_y}{E_{cu}}$ Copper yield strain (in/in)

0.0015625 = 0.0015625

$A_{cu} = \frac{\pi}{4}(d^2 - [d - 2t]^2)$ PTH barrel cross-sectional area (in^2)

0.00011545 = 0.00011545

$A_e = \frac{\pi}{4}([h + d]^2 - d^2)$ Laminate effective cross-sectional area (in^2)

0.011938 = 0.011938

2A. Stress in PTH assuming linear elasticity (PSI)

$$\sigma = \Delta\alpha\Delta T A_e E_e \frac{E_{cu}}{A_e E_e + A_{cu} E_{cu}}$$

61484 = 61484

2B. Stress in PTH accounting for yielding (PSI)

$$\sigma_p = \left(\Delta\alpha\Delta T + S_y \frac{E_{cu} - E_{pcu}}{E_{cu} E_{pcu}}\right) A_e E_e \frac{E_{pcu}}{A_e E_e + A_{cu} E_{pcu}}$$

25298 = 25298

2C. Total strain in copper accounting for yielding (in/in, %)

$$\Delta\varepsilon_{cu} = \left(\varepsilon_y + \frac{\sigma_p - S_y}{E_{pcu}}\right) \cdot 100$$

0.45427 = 0.45427

Note that this value is about equal to free thermal strain, FTS (in/in)

$$FTS = \Delta\alpha\Delta T$$

0.005032 = 0.005032

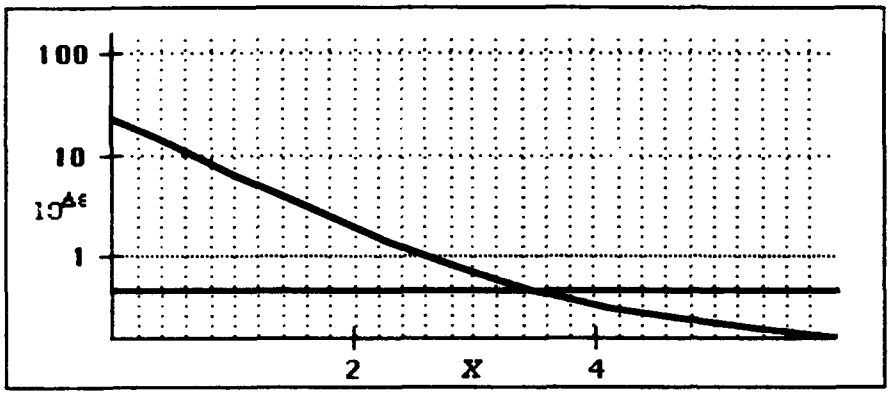
2D. Compute strain-life curve and plot against total (IPC) strain in PTH

Additonal material properties

$D_f = 0.15$ Copper Fatigue Ductility

$Su = 3.5 \cdot 10^4$ Copper Ultimate Strength (PSI)

$$\Delta\varepsilon = 100\left\{(10^X)^{-0.6} D_f^{0.75} + 0.9\frac{Su}{E_{cu}}\left\{\frac{\exp(D_f)}{0.36}\right\}^{0.1785\log\left(\frac{100000}{10^X}\right)}\right\}$$



Graph is a plot of % total strain range vs. cycles to failure (10^X) for the parameter values listed . Also shown is a plot of PTH total strain range (0.45%) which intersects the life curve at approximately X=3.5, or 3162 cycles to failure.

A-3

Fatigue Life Prediction for Digital Module PTHs Subjected to CERT Thermal Cycling from 21°C to 90°C (ΔT=69°C)

This worksheet is an implementation of the copper plated-through-hole (PTH) thermal cycling low-cycle fatigue equation presented in the IPC technical report, IPC-TR-579, September, 1988 (pg. 42). The equation enables the calculation of PTH cycles to failure for a given total strain range over a thermal cycling temperature range of interest.

1. The following is a calculation of the **Digital** module PTH total strain range for the CERT test temperature range of 21C to +90C. It is assumed that the copper PTH complies totally to the expansion of the PWB laminate.

$\alpha_{pwb} = 85 \cdot 10^{-6}$ CTE of PWB (in/in/deg C)

$\alpha_{cu} = 17 \cdot 10^{-6}$ CTE of Copper (in/in/deg C)

$\Delta\alpha = \alpha_{pwb} - \alpha_{cu}$

$6.8 \times 10^{-5} = 6.8 \times 10^{-5}$

Tmax = 90 Max Temperature (deg C)

Tmin = 21 Min Temperature (deg C)

$\Delta T = Tmax - Tmin$

$69 = 69$

Compute total strain range in PTH.

$\Delta e = (\Delta\alpha \Delta T) \cdot 100$ Total strain range in PTH (%)

$0.4692 = 0.4692$

2. Calculate total strain range in the PTH according to the equations presented in the referenced IPC report (pg. 40). These equations account for relative interaction between the PTH and the surrounding laminate, as well as plasticity in the PTH.

Material Properties

$S_y = 25000$ Copper yield stress (PSI)

$E_e = 500000$ Epoxy elastic modulus (PSI)

$E_{cu} = 16 \cdot 10^6$ Copper elastic modulus (PSI)

$E_{pcu} = 0.1 \cdot 10^6$ Copper plastic (bi-linear) modulus (PSI)

Defintions

$h = 0.1$ PWB laminate thickness (in)

$d = 0.026$ PTH outer diameter (in)

$t = 0.0015$ PTH barrel thickness (in)

Q

⊡ $\varepsilon_y = \frac{S_y}{E_{cu}}$ Q Copper yield strain (in/in)

△ 0.0015625 = 0.0015625

Q

⊡ $A_{cu} = \frac{\pi}{4}(d^2 - [d - 2t]^2)$ Q PTH barrel cross-sectional area (in^2)

△ 0.00011545 = 0.00011545

Q

⊡ $A_e = \frac{\pi}{4}([h + d]^2 - d^2)$ Q Laminate effective cross-sectional area (in^2)

□ 0.011938 = 0.011938

Q

Q

Q 2A. Stress in PTH assuming linear elasticity (PSI)

Q

⊡ $\sigma = \Delta\alpha\Delta T A_e E_e \frac{E_{cu}}{A_e E_e + A_{cu} E_{cu}}$

△ 57330 = 57330

Q

Q

Q 2B. Stress in PTH accounting for yielding (PSI)

Q

⊡ $\sigma_p = \left(\Delta\alpha\Delta T + S_y \frac{E_{cu} - E_{pcu}}{E_{cu} E_{pcu}}\right) A_e E_e \frac{E_{pcu}}{A_e E_e + A_{cu} E_{pcu}}$

△ 25264 = 25264

Q

Q

Q 2C. Total strain in copper accounting for yielding (in/in, %)

Q

⊡ $\Delta\varepsilon_{cu} = \left(\varepsilon_y + \frac{\sigma_p - S_y}{E_{pcu}}\right) \cdot 100$

△ 0.42033 = 0.42033

Q

Q

Q Note that this value is about equal to free thermal strain, FTS (in/in)

Q

⊡ FTS = $\Delta\alpha\Delta T$

△ 0.004692 = 0.004692

Q

Q 2D. Compute strain-life curve and plot against total (IPC) strain in PTH

Q

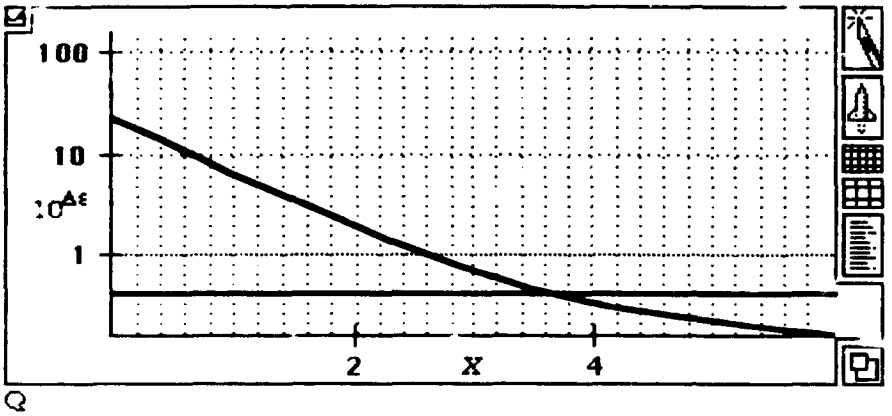
Q Additonal material properties

Q

⊡ D_f = 0.15 Q Copper Fatigue Ductility

$Su = 3.5 \cdot 10^4$ Copper Ultimate Strength (PSI)

$$\Delta\varepsilon = 100\left\{(10^X)^{-0.6} D_f^{0.75} + 0.9\frac{Su}{E_{cu}}\left\{\frac{\exp(D_f)}{0.36}\right\}^{0.1785\log\left(\frac{100000}{10^X}\right)}\right\}$$



Graph is a plot of % total strain range vs. cycles to failure (10^X) for the parameter values listed . Also shown is a plot of PTH total strain range (0.42%) which intersects the life curve at approximately X=3.6, or 3981 cycles to failure.

APPENDIX V

TRANSIENT THERMAL ANALYSIS OF TIMING AND CONTROL MODULE

INTERDEPARTMENTAL CORRESPONDENCE

TO: J. M. Kallis CC: Distribution DATE: April 9, 1990
ORG: 72-26 REF: 722620/1570

SUBJECT: Transient Thermal Analysis of the F-15 PSP Timing and Control Module

FROM: W. J. Hoskins
ORG: 72-26-22
BLDG: E1 MAIL STA: B104
LOC: EQ PHONE: 616-1121

REFERENCES:

1) IDC 722620/1292, "Thermal Analysis of the F-15 PSP Timing and Control Module," from W. J. Hoskins to R. D. Ritacco, dated September 2, 1988.

2) "F-18 Thermal Library," from W. K. Hammond, dated May 23, 1980. User F18LIB[12101,202], Job F18THM Seg. 1028

SUMMARY

A detailed steady state thermal analysis of the Programmable Signal Processor (PSP) Timing and Control (T & C) module for the F-15 aircraft had been performed and was documented in Reference 1. A transient thermal analysis of the PSP Timing and Control module representing the Combined Environments Reliability Test (CERT) conditions are documented in this report. The purpose of the transient analysis was to determine the time necessary for the module to reach its steady state temperatures given the test conditions outlined in Figure 3. The temperature history of the printed wiring board and various key components are to be used in the failure analysis of the module.

The transient thermal analysis of the module was based on the following information.

1) The physical design of the module is as outlined in Reference 1. The design consist of a heat exchanger assembly and two printed wiring board subassemblies. Figures 1 and 2 provide the component layouts for the printed wiring boards.

2) The module operating power dissipation is 47.8 Watts. The component dissipations are taken from Reference 2. The transient profile of the module power dissipation is shown in Figure 3.

3) The coolant (GN_2) flow rate through the Timing and Control module remains constant at 0.202 lb/min throughout the thermal cycling. As shown in Figure 3, the steady state portion of the analysis utilizes a 63°C coolant inlet temperature. For the first 60 minutes of the transient analysis, the inlet temperature of the coolant is 21°C. At 60 minutes, the coolant temperature is returned to 63°C and the transient analysis continues for an additional 60 minutes. The transient profile includes 3 120 minute cycles for a total transient operating time of 360 minutes. The CERT environmental profile, provided by J. M. Kallis, is shown in Figure 3.

KEY RESULTS AND CONCLUSIONS

Table 1 provides the predicted component operating temperatures for the T' & C module during its steady state operation. The table includes the power dissipation, predicted mounting surface, case, and junction temperatures (where applicable).

Figure 4 provides the temperature history of the components on the printed wiring board that have the largest time constants and thus take the longest to reach their predicted steady state temperatures. Figures 5 and 6 provide the temperature history of the hottest integrated circuit, and the component with the largest temperature difference between its case and junction, respectively. Figure 7 provides the temperature history of the hottest location on the printed wiring board. The hottest location on the board is shown as the crossed hatched region in Figure 1.

Based on Figure 4, it takes approximately 50 minutes for the components with the largest time constant to reach their steady state operating temperatures. Since the module reaches steady state before the next cycle begins, the temperature response in the subsequent cycles will be identical to that of the first cycle. The component operating temperatures at the end of each transient cycle are the same as those predicted for the steady state condition and are shown in Table 1.

W. J. Hoskins, Staff Engineer
THERMODYNAMICS DEPARTMENT

Approved:

E. B. Curry, Scientist
THERMODYNAMICS DEPARTMENT

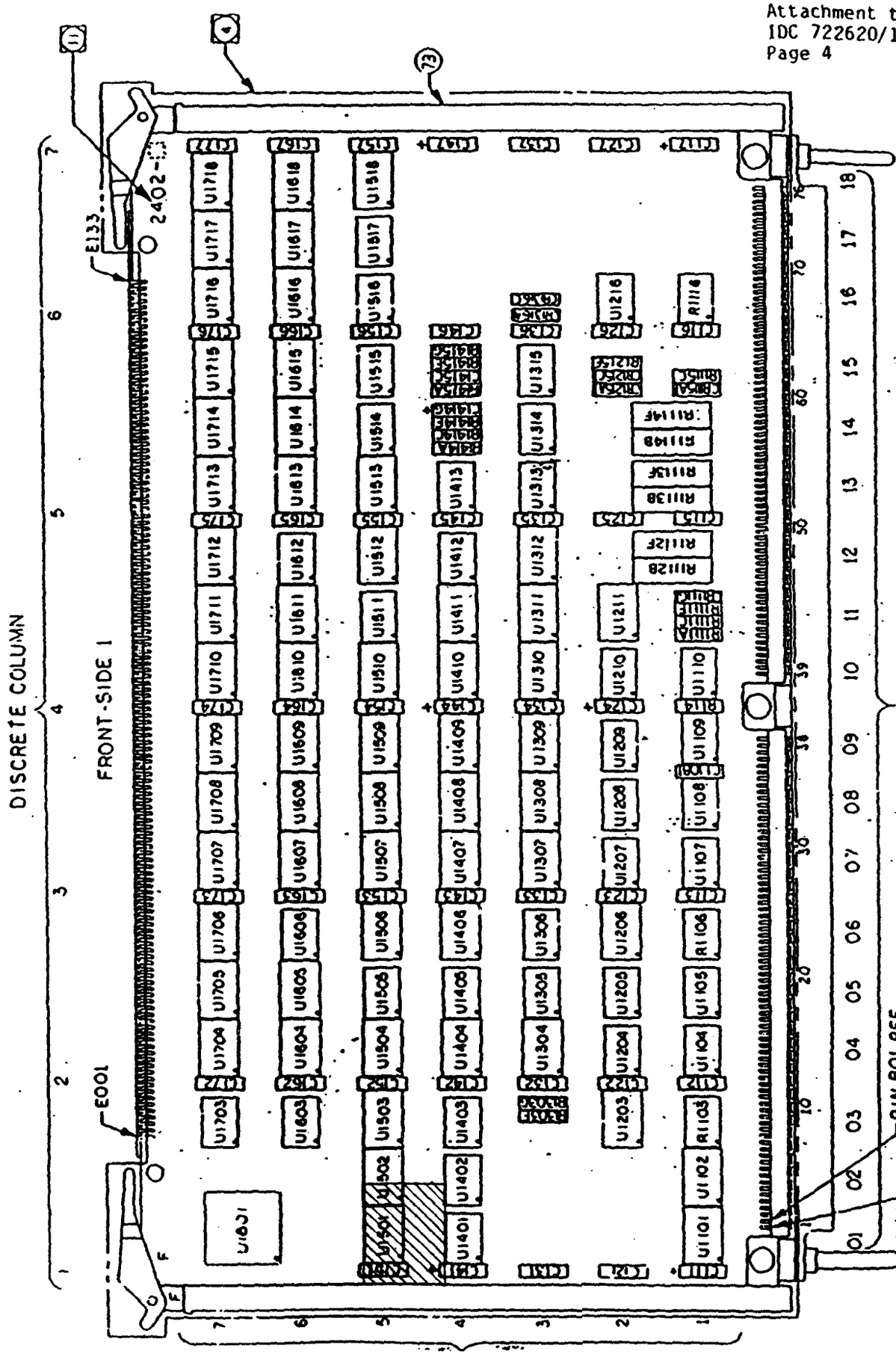


Figure V-1. Component Layout – Front Side 1

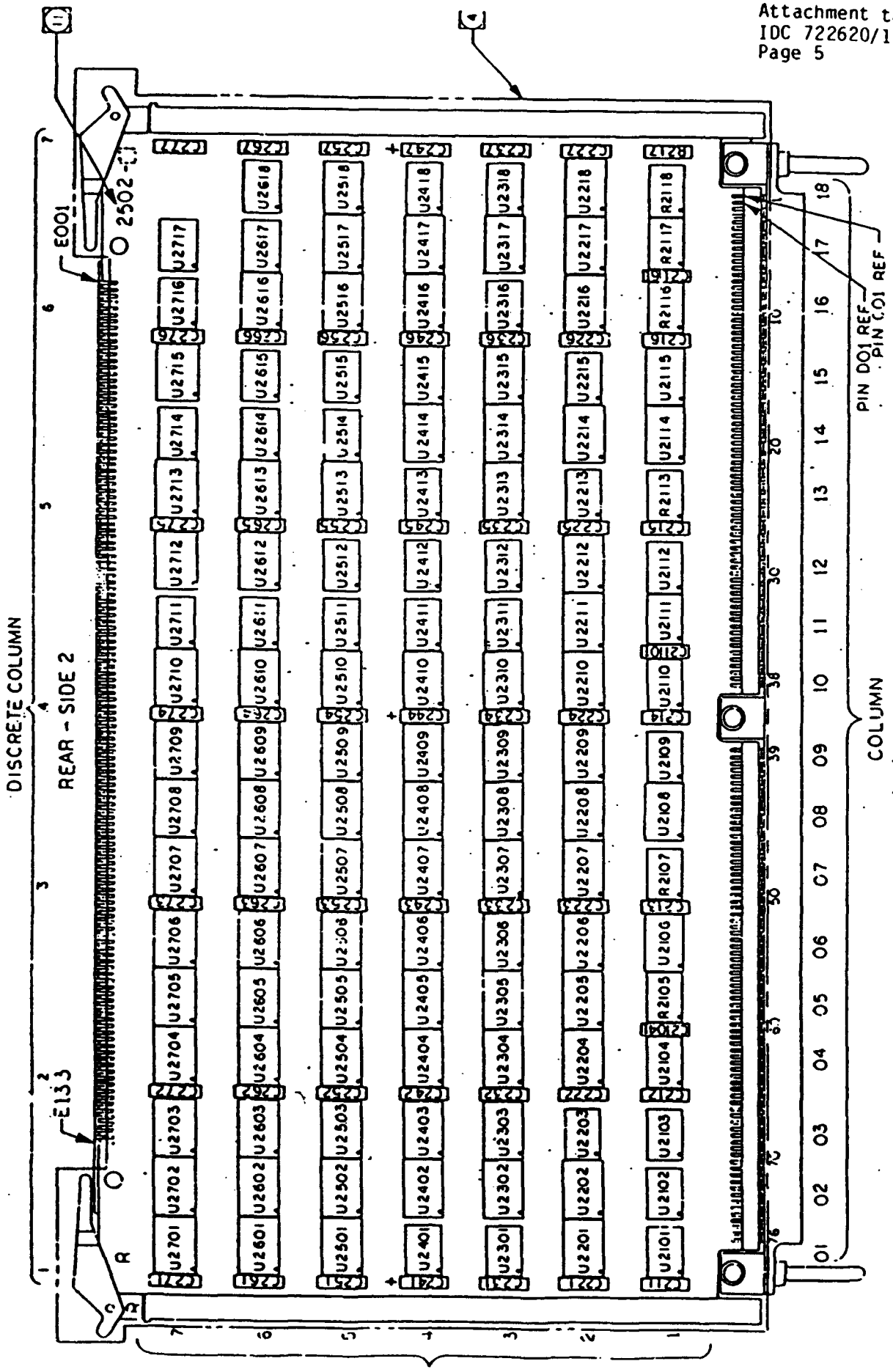


Figure V-2. Component Layout – Rear Side 2

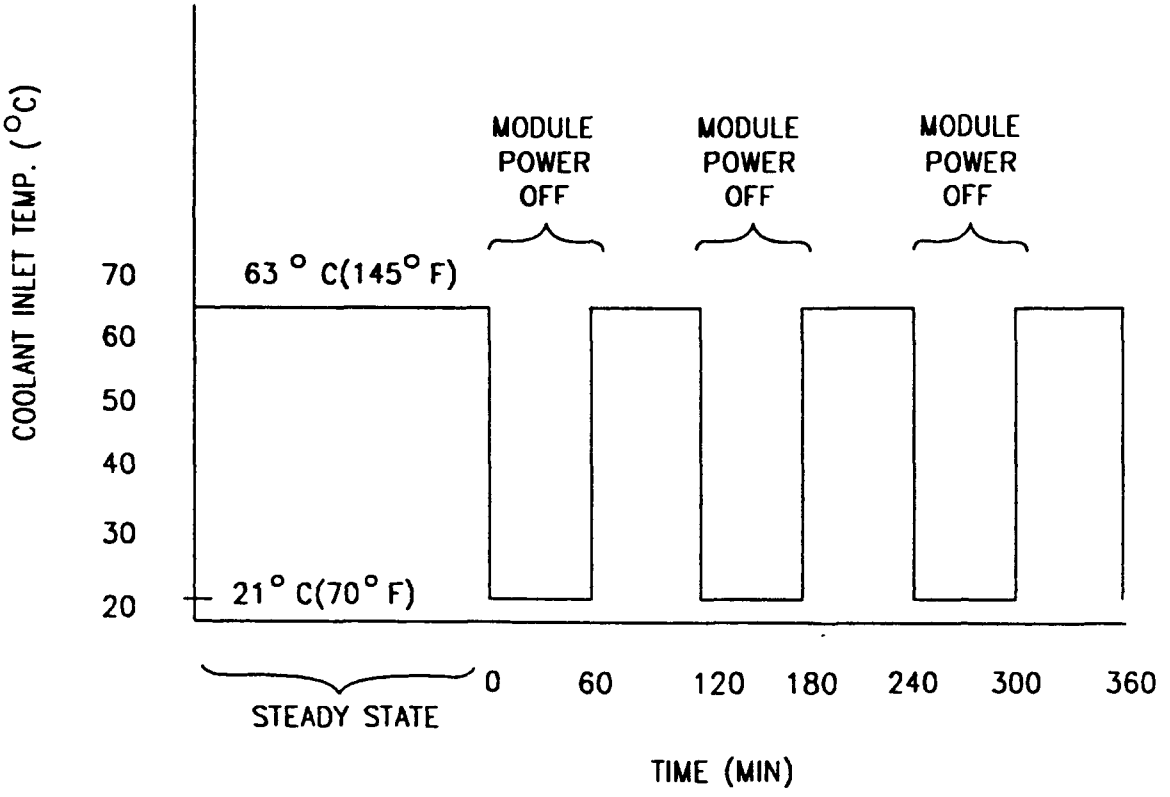


Figure V-3. F15 PSP Timing and Control Module CERT Environmental Profile

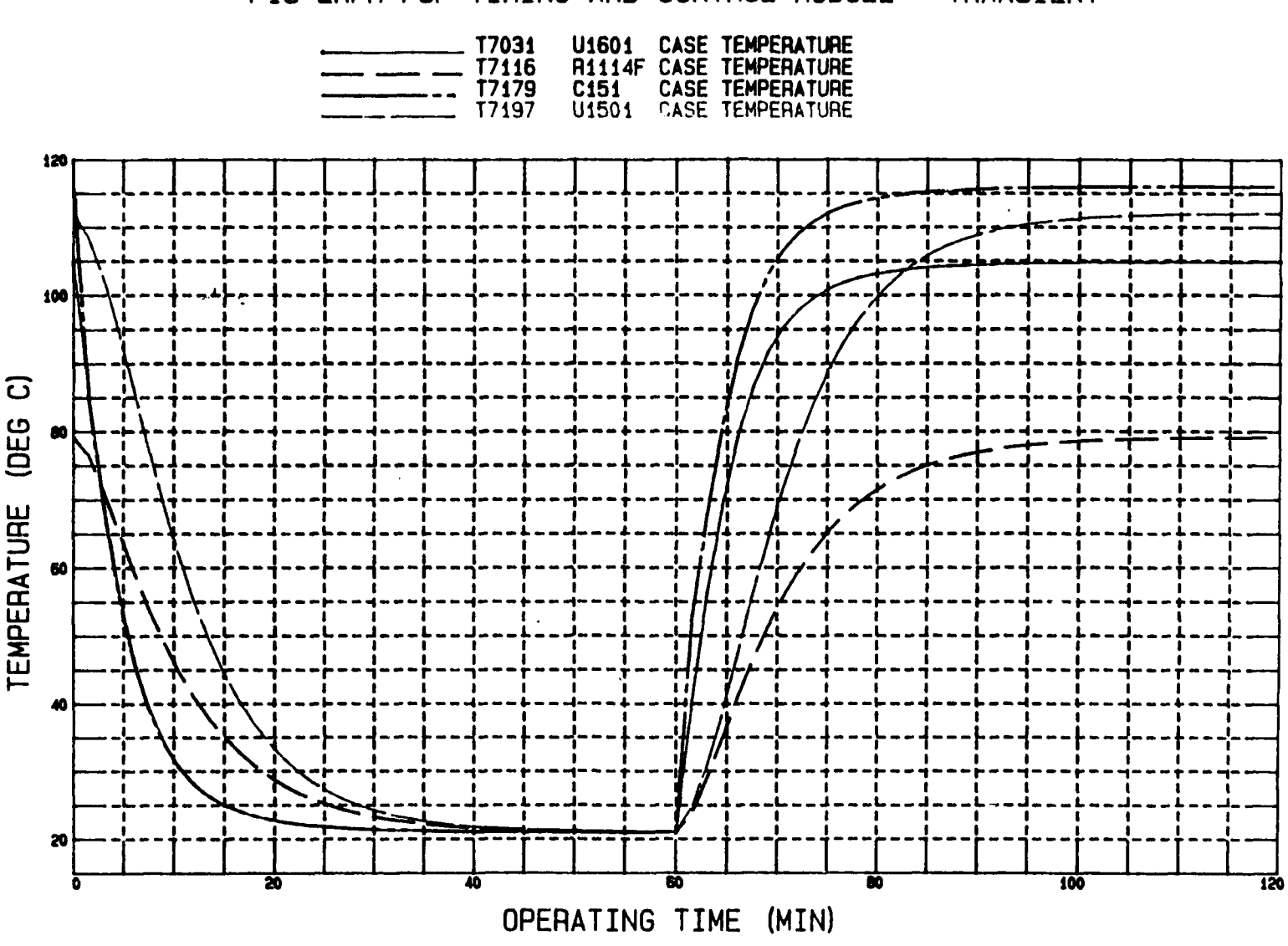


Figure V-4. Components with the Largest Time Constants

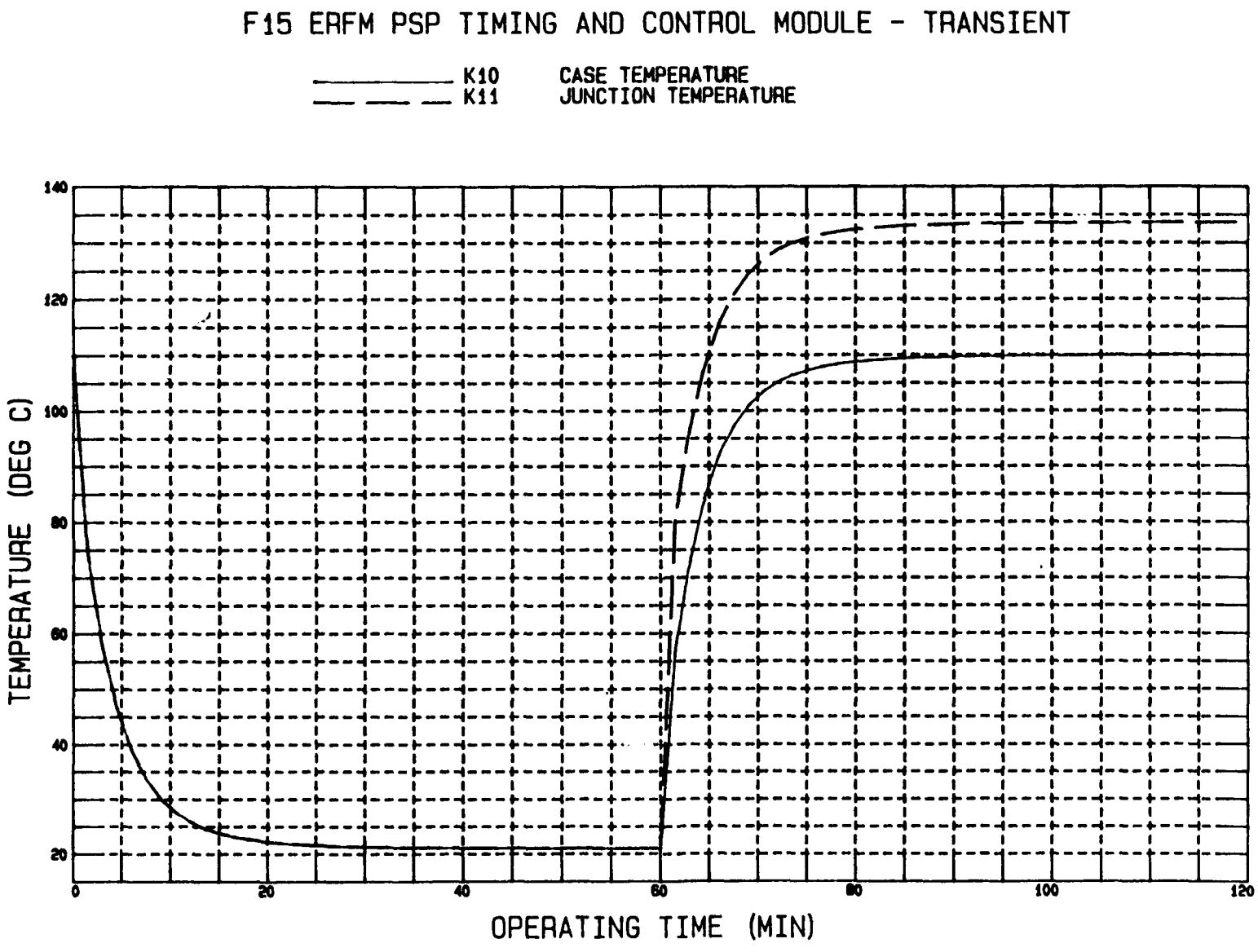


Figure V-5. Hottest Integrated Circuit (U1508)

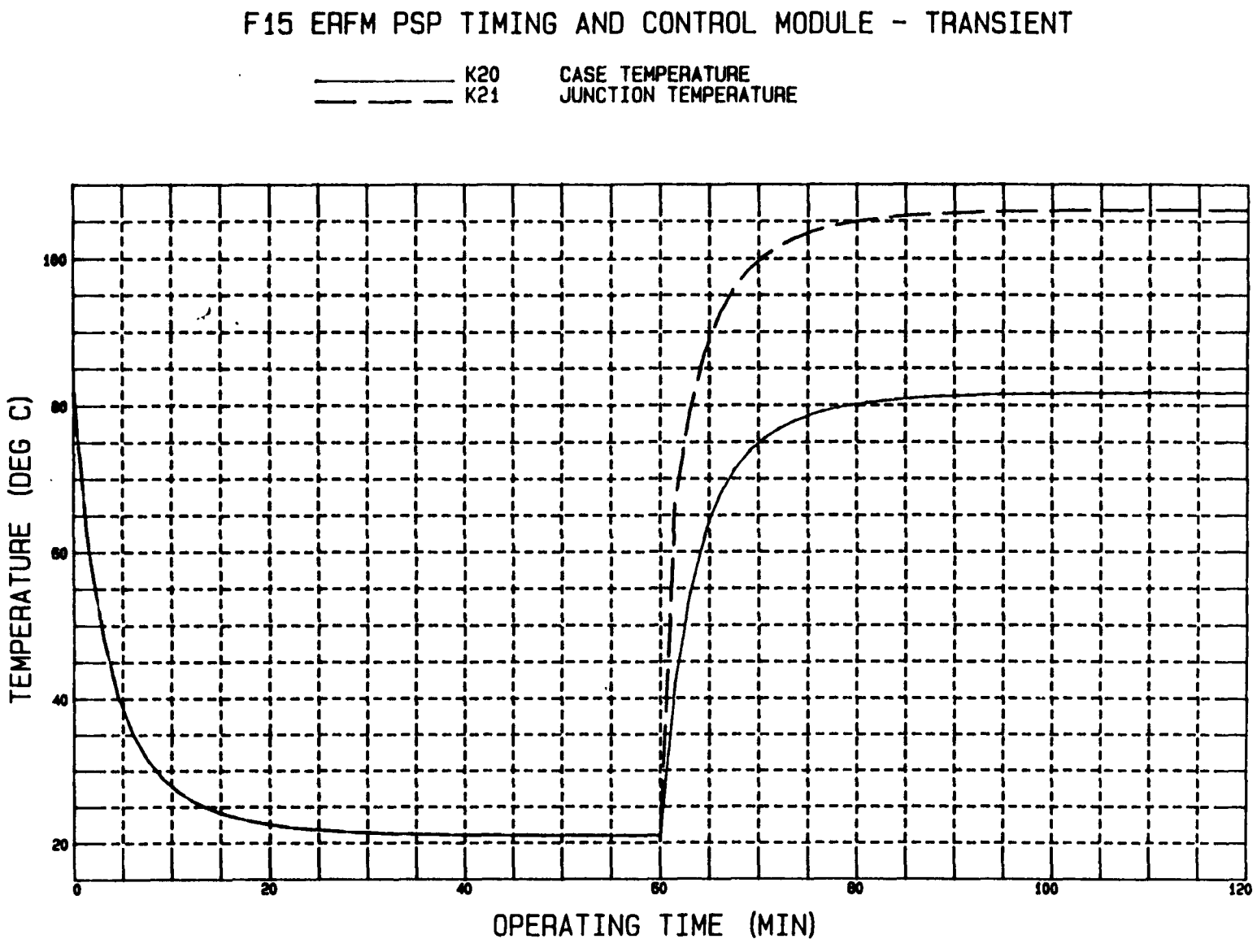


Figure V-6. Component with Highest Case to Junction ΔT (U1315)

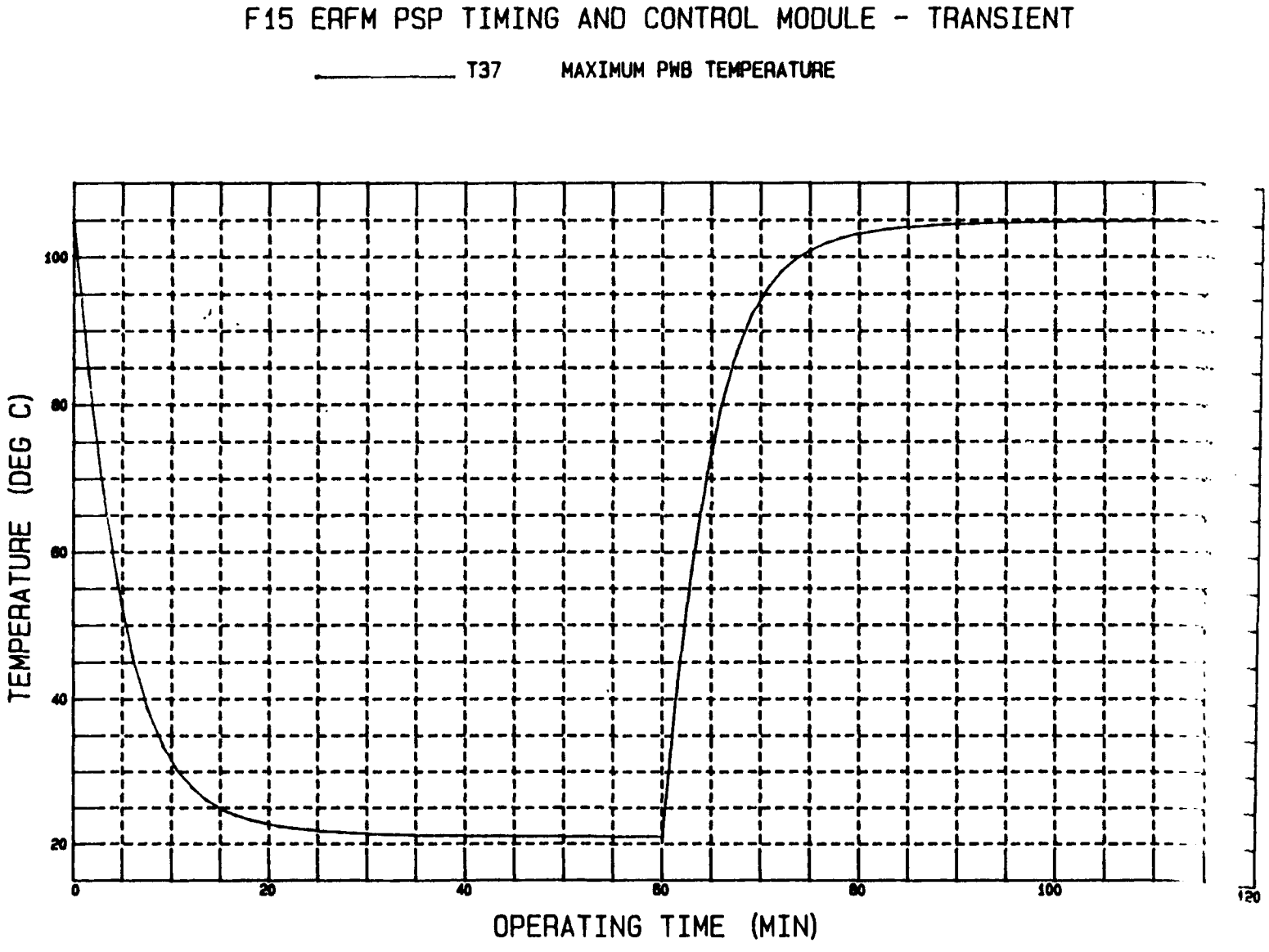


Figure V-7. Hottest Location on the Printed Wiring Board

TABLE V-1

F-15 PSP TIMING AND CONTROL MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1108I	905570-73B	0.000	90.	90.	
C111	M39003/02-0079	0.000	96.	96.	
C112	905570-73B	0.000	94.	94.	
C113	905570-73B	0.000	92.	92.	
C115	905570-73B	0.000	78.	78.	
C116	905570-73B	0.000	75.	75.	
C117	M39003/02-0079	0.000	75.	75.	
C121	905570-73B	0.000	95.	95.	
C122	905570-73B	0.000	96.	96.	
C123	905570-73B	0.000	95.	95.	
C124	M39003/02-0079	0.000	89.	89.	
C125	905570-73B	0.000	78.	78.	
C126	905570-73B	0.000	75.	75.	
C127	905570-73B	0.000	71.	71.	
C131	905570-73B	0.000	97.	97.	
C132	905570-73B	0.000	97.	97.	
C133	905570-73B	0.000	96.	96.	
C134	905570-73B	0.000	93.	93.	
C135	905570-73B	0.000	80.	80.	
C136	905570-73B	0.000	75.	75.	
C137	905570-73B	0.000	72.	72.	
C141	M39003/02-0068	0.000	100.	100.	
C1414G	M39003/02-0087	0.000	82.	82.	
C1415C	905570-73B	0.000	77.	77.	
C142	905570-73B	0.000	101.	101.	
C143	905570-73B	0.000	99.	99.	
C144	M39003/02-0068	0.000	97.	97.	
C145	905570-73B	0.000	82.	82.	
C146	905570-73B	0.000	77.	77.	
C147	M39003/02-0068	0.000	73.	73.	
C151	905570-73B	0.000	105.	105.	
C152	905570-73B	0.000	104.	104.	
C153	905570-73B	0.000	99.	99.	
C154	905570-73B	0.000	99.	99.	
C155	905570-73B	0.000	85.	85.	
C156	905570-73B	0.000	80.	80.	
C157	905570-73B	0.000	77.	77.	
C162	905570-73B	0.000	102.	102.	
C163	905570-73B	0.000	99.	99.	
C164	905570-73B	0.000	98.	98.	
C165	905570-73B	0.000	87.	87.	

TABLE V-1 (Continued)

F-15 PSP TIMING AND CONTROL MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C166	905570-73B	0.000	83.	83.	
C167	905570-73B	0.000	80.	80.	
C172	905570-73B	0.000	102.	102.	
C173	905570-73B	0.000	101.	101.	
C174	905570-73B	0.000	97.	97.	
C175	905570-73B	0.000	90.	90.	
C176	905570-73B	0.000	87.	87.	
C177	905570-73B	0.000	85.	85.	
C2104I	905570-73B	0.000	77.	77.	
C211	905570-73B	0.000	75.	75.	
C2110I	905570-73B	0.000	86.	86.	
C2116I	905570-73B	0.000	93.	93.	
C212	905570-73B	0.000	77.	77.	
C213	905570-73B	0.000	80.	80.	
C214	905570-73B	0.000	86.	86.	
C215	905570-73B	0.000	91.	91.	
C216	905570-73B	0.000	93.	93.	
C221	905570-73B	0.000	75.	75.	
C222	905570-73B	0.000	78.	78.	
C223	905570-73B	0.000	81.	81.	
C224	905570-73B	0.000	86.	86.	
C225	905570-73B	0.000	93.	93.	
C226	905570-73B	0.000	95.	95.	
C227	905570-73B	0.000	98.	98.	
C231	905570-73B	0.000	77.	77.	
C232	905570-73B	0.000	80.	80.	
C233	905570-73B	0.000	83.	83.	
C234	905570-73B	0.000	87.	87.	
C235	905570-73B	0.000	94.	94.	
C236	905570-73B	0.000	96.	96.	
C237	905570-73B	0.000	98.	98.	
C241	M39003/02-0068	0.000	80.	80.	
C242	905570-73B	0.000	85.	85.	
C243	905570-73B	0.000	88.	88.	
C244	M39003/02-0068	0.000	88.	88.	
C245	905570-73B	0.000	97.	97.	
C246	905570-73B	0.000	98.	98.	
C247	M39003/02-0068	0.000	101.	101.	
C251	905570-73B	0.000	83.	83.	
C252	905570-73B	0.000	88.	88.	
C253	905570-73B	0.000	90.	90.	

TABLE V-1 (Continued)

F-15 PSP TIMING AND CONTROL MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C254	905570-73B	0.000	90.	90.	
C255	905570-73B	0.000	98.	98.	
C256	905570-73B	0.000	100.	100.	
C257	905570-73B	0.000	102.	102.	
C261	905570-73B	0.000	86.	86.	
C262	905570-73B	0.000	89.	89.	
C263	905570-73B	0.000	92.	92.	
C264	905570-73B	0.000	91.	91.	
C265	905570-73B	0.000	97.	97.	
C266	905570-73B	0.000	100.	100.	
C267	905570-73B	0.000	101.	101.	
C271	905570-73B	0.000	88.	88.	
C272	905570-73B	0.000	90.	90.	
C273	905570-73B	0.000	92.	92.	
C274	905570-73B	0.000	92.	92.	
C275	905570-73B	0.000	98.	98.	
C276	905570-73B	0.000	100.	100.	
C277	905570-73B	0.000	100.	100.	
CR1111G	JANTX1N4150-1	0.000	83.	83.	83.
CR1115A	JANTX1N4150-1	0.000	75.	75.	75.
CR1215A	JANTX1N4150-1	0.000	75.	75.	75.
CR1215C	JANTX1N4150-1	0.000	75.	75.	75.
CR1316A	925974-1B	0.000	75.	75.	75.
R1103	M8340103M27ROJA	0.070	94.	95.	
R1106	955230-8B	0.100	92.	103.	
R1111A	RCR07G101JS	0.040	83.	83.	
R1111C	RCR07G512JS	0.040	83.	83.	
R1111E	RCR07G100JS	0.040	83.	83.	
R1112B	RLR32C348FP	0.040	83.	84.	
R1112F	RLR32C348FP	0.040	83.	84.	
R1113B	RLR32C348FP	0.040	78.	79.	
R1113F	RLR32C348FP	0.040	78.	79.	
R1114B	RLR32C348FP	0.040	78.	79.	
R1114F	RLR32C348FP	0.040	78.	79.	
R1115C	RCR07G100JS	0.040	75.	75.	
R1116	M8340103M27ROJA	0.070	75.	76.	
R114	RCR07G121JS	0.040	87.	88.	
R1215E	RCR07G270JS	0.040	75.	75.	
R1303E	RCR07G270JS	0.040	97.	98.	
R1303G	RCR07G270JS	0.040	97.	98.	
R1414A	RCR07G152JS	0.040	82.	83.	

TABLE V-1 (Continued)

F-15 PSP TIMING AND CONTROL MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
R1414C	RCR07G102JS	0.040	82.	83.	
R1414E	RCR07G100JS	0.040	82.	83.	
R1415A	RCR07G392JS	0.040	77.	77.	
R1415E	RCR07G820JS	0.040	77.	77.	
R1415G	RCR07G330JS	0.040	77.	77.	
R217	RNC50H3161FS	0.070	96.	98.	
R2105	M8340103M27ROJA	0.070	80.	82.	
R2107	M8340103M27ROJA	0.070	83.	85.	
R2113	M8340103M27ROJA	0.070	91.	93.	
R2116	M8340103M27ROJA	0.070	93.	95.	
R2117	M8340103M27ROJA	0.070	96.	97.	
R2118	M8340103M27ROJA	0.070	96.	97.	
U1101	932849-1B	0.300	96.	103.	118.
U1102	932849-1B	0.300	96.	103.	118.
U1104	932783-2B	0.092	94.	96.	98.
U1105	M38510/30003BDX	0.013	92.	92.	92.
U1107	932730-2B	0.173	90.	93.	104.
U1108	M38510/07001BDX	0.079	90.	91.	93.
U1109	932730-2B	0.173	87.	91.	101.
U1110	932730-2B	0.173	87.	91.	101.
U1203	932849-1B	0.300	96.	102.	117.
U1204	932783-2B	0.092	96.	98.	100.
U1205	932730-2B	0.173	95.	99.	109.
U1206	932614-3B	0.473	95.	105.	115.
U1207	M38510/07003BDX	0.118	92.	94.	97.
U1208	M38510/07301BDX	0.113	92.	94.	97.
U1209	M38510/07003BDX	0.118	89.	91.	94.
U1210	M38510/07003BDX	0.118	89.	91.	94.
U1211	93281[illegible]-226	0.472	85.	93.	116.
U1216	M38510/07003BDX	0.118	75.	77.	80.
U1304	932616-501B	0.100	97.	99.	105.
U1305	M38510/07003BDX	0.118	96.	98.	101.
U1306	M38510/07001BDX	0.079	96.	98.	99.
U1307	932614-3B	0.473	96.	106.	116.
U1308	M38510/34102BFX	0.168	96.	100.	103.
U1309	932614-3B	0.473	93.	103.	113.
U1310	M38510/34102BFX	0.168	93.	96.	100.
U1311	932756-1B	0.100	86.	88.	94.
U1312	932756-1B	0.100	86.	88.	94.
U1313	932783-2B	0.092	80.	82.	84.
U1314	932783-2B	0.092	80.	82.	84.

TABLE V-1 (Continued)

F-15 PSP TIMING AND CONTROL MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U1315	928063-501B	0.095	75.	77.	103.
U1401	932730-2B	0.173	100.	104.	114.
U1402	M38510/07401BDX	0.057	100.	102.	103.
U1403	M38510/07401BDX	0.057	101.	102.	103.
U1404	932614-3B	0.473	101.	111.	121.
U1405	M38510/07001BDX	0.079	99.	101.	102.
U1406	932614-3B	0.473	99.	109.	119.
U1407	932727-1B	0.447	100.	110.	127.
U1408	932820-218	0.472	100.	108.	132.
U1409	932727-1B	0.447	97.	106.	124.
U1410	932727-1B	0.447	97.	106.	124.
U1411	932614-3B	0.473	90.	100.	110.
U1412	M38510/08001BDX	0.099	90.	92.	94.
U1413	M38510/07001BDX	0.079	82.	84.	86.
U1501	932709-1B	0.525	105.	116.	128.
U1502	932709-1B	0.525	105.	116.	128.
U1503	932709-1B	0.525	104.	115.	127.
U1504	932614-3B	0.473	104.	114.	125.
U1505	M38510/07003BDX	0.118	99.	101.	104.
U1506	M38510/07009BFX	0.022	99.	99.	100.
U1507	932709-1B	0.525	102.	113.	125.
U1508	932820-217	0.472	102.	110.	134
U1509	932820-219	0.472	99.	107.	130.
U1510	932820-220	0.472	99.	107.	130.
U1511	M38510/07501BDX	0.263	92.	98.	103.
U1512	932746-1B	0.342	92.	99.	119.
U1513	932746-1B	0.342	85.	93.	113.
U1514	M38510/30605BDX	0.084	85.	87.	89.
U1515	M38510/30605BDX	0.084	80	81.	83.
U1516	M38510/30605BDX	0.084	80.	81.	83.
U1517	M38510/30605BDX	0.084	77.	78.	80.
U1518	932749-1B	0.158	77.	80.	89.
U1601	930739-1B	0.100	100.	112.	117.
U1603	932730-2B	0.173	102.	106.	116.
U1604	M38510/54102BFX	0.168	102.	106.	110.
U1605	M38510/07009BFX	0.022	99.	100.	100.
U1606	M38510/08001BDX	0.099	99.	101.	104.
U1607	932709-1B	0.525	102.	113.	124.
U1608	932746-1B	0.342	102.	109.	129.
U1609	932732-1B	0.289	98.	104.	110.
U1610	932732-1B	0.289	98.	104.	110.

TABLE V-1 (Continued)

F-15 PSP TIMING AND CONTROL MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U1611	932820-215	0.472	93.	101.	125.
U1612	M38510/07003BDX	0.118	93.	96.	98.
U1613	932749-1B	0.158	87.	91.	100.
U1614	932749-1B	0.158	87.	91.	100.
U1615	932749-1B	0.158	83.	86.	96.
U1616	932749-1B	0.158	83.	86.	96.
U1617	932749-1B	0.158	80.	84.	93.
U1618	932749-1B	0.158	80.	84.	93.
U1703	932730-2B	0.173	102.	106.	117.
U1704	932709-1B	0.525	102.	114.	125.
U1705	932709-1B	0.525	101.	112.	123.
U1706	932690-1B	0.053	101.	102.	103.
U1707	932746-1B	0.342	100.	107.	128.
U1708	932746-1B	0.342	100.	107.	128.
U1709	932732-1B	0.289	97.	103.	109.
U1710	932732-1B	0.289	97.	103.	109.
U1711	932820-224	0.472	93.	101.	125.
U1712	M38510/33701BFX	0.033	93.	94.	95.
U1713	932746-1B	0.342	90.	98.	118.
U1714	932746-1B	0.342	90.	98.	118.
U1715	932746-1B	0.342	87.	94.	115.
U1716	932746-1B	0.342	87.	94.	115.
U1717	932746-1B	0.342	85.	92.	112.
U1718	932746-1B	0.342	85.	92.	112.
U2101	M38510/07003BDX	0.118	75.	77.	80.
U2102	M38510/07003BDX	0.118	75.	77.	80.
U2103	M38510/07003BDX	0.118	77.	79.	82.
U2104	M38510/07003BDX	0.118	77.	79.	82.
U2106	932849-1B	0.300	80.	87.	102.
U2108	932849-1B	0.300	83.	90.	105.
U2109	932730-2B	0.173	86.	90.	100.
U2110	932730-2B	0.173	86.	90.	100.
U2111	932730-2B	0.173	89.	93.	103.
U2112	932730-2B	0.173	89.	93.	103.
U2114	932728-1B	0.079	91.	93.	95.
U2115	932728-1B	0.079	93.	95.	97.
U2201	932726-1B	0.084	75.	77.	82.
U2202	932726-1B	0.084	75.	77.	82.
U2203	M38510/07003BDX	0.118	78.	80.	83.
U2204	H990436-001B	0.122	78.	80.	86.
U2205	H990436-001B	0.122	81.	83.	89.

TABLE V-1 (Continued)

F-15 PSP TIMING AND CONTROL MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U2206	H990436-001B	0.122	81.	83.	89.
U2207	H990436-001B	0.122	83.	86.	92.
U2208	932726-1B	0.084	83.	85.	90.
U2209	932726-1B	0.084	86.	88.	93.
U2210	932728-1B	0.079	86.	88.	89.
U2211	932728-1B	0.079	89.	90.	92.
U2212	932728-1B	0.079	89.	90.	92.
U2213	M38510/07003BDX	0.118	93.	95.	98.
U2214	932849-1B	0.300	93.	99.	114.
U2215	M38510/07003BDX	0.118	95.	98.	101.
U2216	932849-1B	0.300	95.	102.	117.
U2217	932849-1B	0.300	98.	104.	119.
U2218	932849-1B	0.300	98.	104.	119.
U2301	M38510/07301BDX	0.113	77.	79.	82.
U2302	932728-1B	0.079	77.	79.	80.
U2303	932728-1B	0.079	80.	82.	83.
U2304	932749-1B	0.158	80.	83.	93.
U2305	932749-1B	0.158	83.	87.	96.
U2306	932749-1B	0.158	83.	87.	96.
U2307	932749-1B	0.158	85.	89.	98.
U2308	932749-1B	0.158	85.	89.	98.
U2309	932749-1B	0.158	87.	90.	100.
U2310	H990436-001B	0.122	87.	90.	95.
U2311	M38510/08001BDX	0.099	89.	91.	94.
U2312	M38510/30301BDX	0.012	89.	90.	90.
U2313	932728-1B	0.079	94.	95.	97.
U2314	H990436-001B	0.122	94.	96.	102.
U2315	H990436-001B	0.122	96.	99.	104.
U2316	M38510/07001BDX	0.079	96.	98.	100.
U2317	932685-1B	0.035	98.	98.	100.
U2318	M38510/30001BDX	0.008	98.	98.	98.
U2401	M38510/07301BDX	0.113	80.	83.	85.
U2402	932736-1B	0.394	80.	89.	98.
U2403	932736-1B	0.394	85.	93.	102.
U2404	932736-1B	0.394	85.	93.	102.
U2405	932736-1B	0.394	88.	96.	105.
U2406	932736-1B	0.394	88.	96.	105.
U2407	932736-1B	0.394	88.	96.	105.
U2408	932690-1B	0.053	88.	89.	90.
U2409	932690-1B	0.053	88.	89.	90.
U2410	932756-1B	0.100	88.	90.	96.

TABLE V-1 (Continued)

F-15 PSP TIMING AND CONTROL MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U2411	M38510/30301BDX	0.012	91.	91.	91.
U2412	M38510/07001BDX	0.079	91.	92.	94.
U2413	M38510/07003BDX	0.118	97.	99.	102.
U2414	932614-3B	0.473	97.	107.	117.
U2415	932756-1B	0.100	98.	100.	106.
U2416	932756-1B	0.100	98.	100.	106.
U2417	932614-3B	0.473	101.	111.	121.
U2418	M38510/07005BDX	0.059	101.	102.	103.
U2501	932728-1B	0.079	83.	85.	87.
U2502	932736-1B	0.394	83.	92.	100.
U2503	932736-1B	0.394	88.	96.	105.
U2504	932736-1B	0.394	88.	96.	105.
U2505	932736-1B	0.394	90.	99.	107.
U2506	932736-1B	0.394	90.	99.	107.
U2507	932736-1B	0.394	90.	98.	107.
U2508	932690-1B	0.053	90.	91.	92.
U2509	932690-1B	0.053	90.	91.	92.
U2510	932756-1B	0.100	90.	92.	98.
U2511	M38510/07001BDX	0.079	92.	94.	96.
U2512	M38510/07003BDX	0.118	92.	95.	98.
U2513	932614-3B	0.473	98.	108.	119.
U2514	M38510/08001BDX	0.099	98.	100.	102.
U2515	M38510/07401BDX	0.057	100.	102.	103.
U2516	932614-3B	0.473	100.	110.	121.
U2517	932727-1B	0.447	102.	112.	130.
U2518	M38510/07003BDX	0.118	102.	105.	107.
U2601	932736-1B	0.394	86.	95.	103.
U2602	932736-1B	0.394	86.	95.	103.
U2603	932736-1B	0.394	89.	98.	106.
U2604	932736-1B	0.394	89.	98.	106.
U2605	932736-1B	0.394	92.	100.	109.
U2606	932736-1B	0.394	92.	100.	109.
U2607	932736-1B	0.394	91.	100.	108.
U2608	932690-1B	0.053	91.	92.	94.
U2609	932690-1B	0.053	91.	92.	93.
U2610	932756-1B	0.100	91.	93.	99.
U2611	M38510/07001BDX	0.079	93.	95.	97.
U2612	932690-1B	0.053	93.	95.	96.
U2613	M38510/34102BFX	0.168	97.	101.	105.
U2614	M38510/30502BDX	0.032	97.	98.	99.
U2615	M38510/07003BDX	0.118	100.	103.	105.

TABLE V-1 (Continued)

F-15 PSP TIMING AND CONTROL MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
U2616	M38510/33901BFX	0.237	100.	105.	110.
U2617	M38510/08001BDX	0.099	101.	103.	105.
U2618	M38510/07001BDX	0.079	101.	102.	104.
U2701	932736-1B	0.394	88.	96.	105.
U2702	932736-1B	0.394	88.	96.	105.
U2703	932736-1B	0.394	90.	98.	107.
U2704	932736-1B	0.394	90.	98.	107.
U2705	932736-1B	0.394	92.	101.	109.
U2706	932736-1B	0.394	92.	101.	109.
U2707	932736-1B	0.394	92.	101.	109.
U2708	932690-1B	0.053	92.	93.	95.
U2709	932690-1B	0.053	92.	94.	95.
U2710	932756-1B	0.100	92.	95.	100.
U2711	M38510/07003BDX	0.118	95.	97.	100.
U2712	932690-1B	0.053	95.	96.	97.
U2713	932746-1B	0.342	98.	106.	126.
U2714	M38510/07001BDX	0.079	98.	100.	102.
U2715	M38510/34102BFX	0.168	100.	103.	107.
U2716	M38510/07001BDX	0.079	100.	101.	103.
U2717	M38510/07003BDX	0.118	100.	102.	105.

TOTAL OF PART DISSIPATIONS: 47.766 WATTS

APPENDIX W

TRANSIENT THERMAL ANALYSIS OF LINEAR REGULATOR MODULE

INTERDEPARTMENTAL CORRESPONDENCE

TO: J. M. Kallis CC: Distribution DATE: April 4, 1990
ORG: 72-26 REF: 722620/1567

SUBJECT: Transient Thermal Analysis of the F-15 PSP Linear Regulator Module

FROM: A. T. Bishop
ORG: 72-26-22
BLDG: E1 MAIL STA: B104
LOC: EO PHONE: 616-1048

REFERENCES:
1) IDC 722620/1329, "Thermal Analysis of the F-15 PSP Linear Regulator Module," from A. T. Bishop to J. M. Kallis, dated November 7, 1988.
2) AVO, "Power Dissipations of 3569800 Module," R. M. Nicoletti to J. Kallis, dated October 26, 1988.

SUMMARY

A detailed steady state thermal analysis of the PSP Linear Regulator module in the Signal Processor unit for the F-15 aircraft has been performed and is documented in Reference 1. The results of a transient thermal analysis of the PSP Linear Regulator module are included in this document. The purpose of the transient analysis was to determine the length of time necessary for the Linear Regulator module to reach its steady state operating temperature given the environmental profile outlined by J. M. Kallis (72-26). The temperature history of the printed wiring board and various key components can then be used to aid the failure analysis of the module.

The transient thermal analysis of the PSP Linear Regulator module was based on the following information.

1) The physical configuration of the Linear Regulator module is as outlined in Reference 1. The analysis included the modelling of a heat exchanger assembly, a printed wiring board subassembly, and detailed analysis of the three hybrids (1 unique) located on the printed wiring board. Figures 1 and 2 provide the component layouts for the printed wiring board and the hybrids, respectively.

2) The total module power dissipation is 7.8 Watts. Of the total power dissipation, the hybrids U1, U2, and U3 located on the printed wiring board dissipate 2.26 W, 1.03 W, and .037 W, respectively. The component dissipations were supplied by R. M. Nicoletti (27-36) in Reference 2. It should be noted that the component dissipations used in the analysis were calculated by using +18 V inputs and maximum loads as defined in TS 31325-184. The transient profile of the module power dissipation is shown in Figure 3.

3) The coolant (GN_2) flow rate through the Linear Regulator module remains constant at 0.167 lb/min throughout the transient analysis. As shown in Figure 3, the steady state portion of the analysis utilizes a 63°C coolant inlet temperature. For the first 60 minutes of the transient analysis, the inlet temperature of the coolant is 21°C. At 60 minutes, the coolant temperature is returned to 63°C and the transient analysis continues for an additional 60 minutes. The transient profile includes 3 120 minute transient cycles for a total transient operating time of 360 minutes. The environmental profile as provided by J. M. Kallis is shown in Figure 3.

KEY RESULTS AND CONCLUSIONS

Table 1 provides the predicted component operating temperatures for the Linear Regulator module during its steady state operation, as shown in Figure 3. Tables 2 through 4 include the steady state operating temperatures of the components located inside hybrids U1, U2, and U3, respectively. These tables include the power dissipation, predicted mounting surface, case, and junction temperatures (where applicable).

Figure 4 provides the temperature history of the components on the printed wiring board that have the largest time constant and thus take the longest to reach their predicted steady state temperatures. Figures 5 through 7 provide the temperature history of the hottest integrated circuit, the hottest chip located inside hybrid U1, and the component with the largest temperature difference between its case and junction, respectively. Figure 8 provides the temperature history of the hottest location on the printed wiring board.

Based on Figure 4, it takes approximately 50 minutes for the components with the largest time constant to reach their steady state operating temperatures. Since the Linear Regulator module reaches steady state before another transient cycle begins, it is not necessary to analyze the module for three complete cycles as shown in Figure 3. The temperature response in the subsequent cycles will be identical to that in the first cycle of the transient profile. The component operating temperatures at the end of each transient cycle are the same as those predicted for the steady state condition and are shown in Tables 1 through 4.

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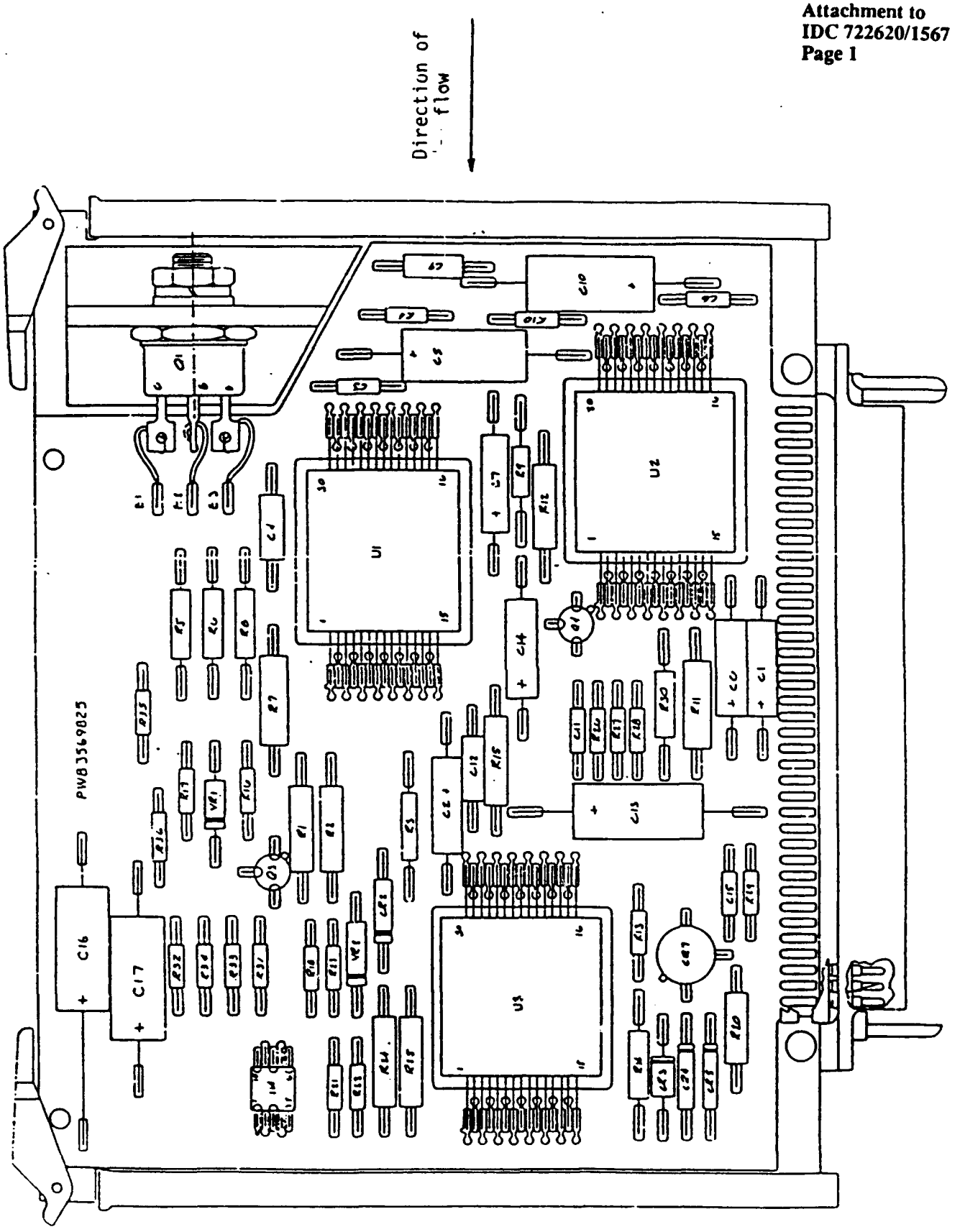

Figure W-1. F15 ERFM Linear Regulator Module Component Layout on Printed Wiring Board

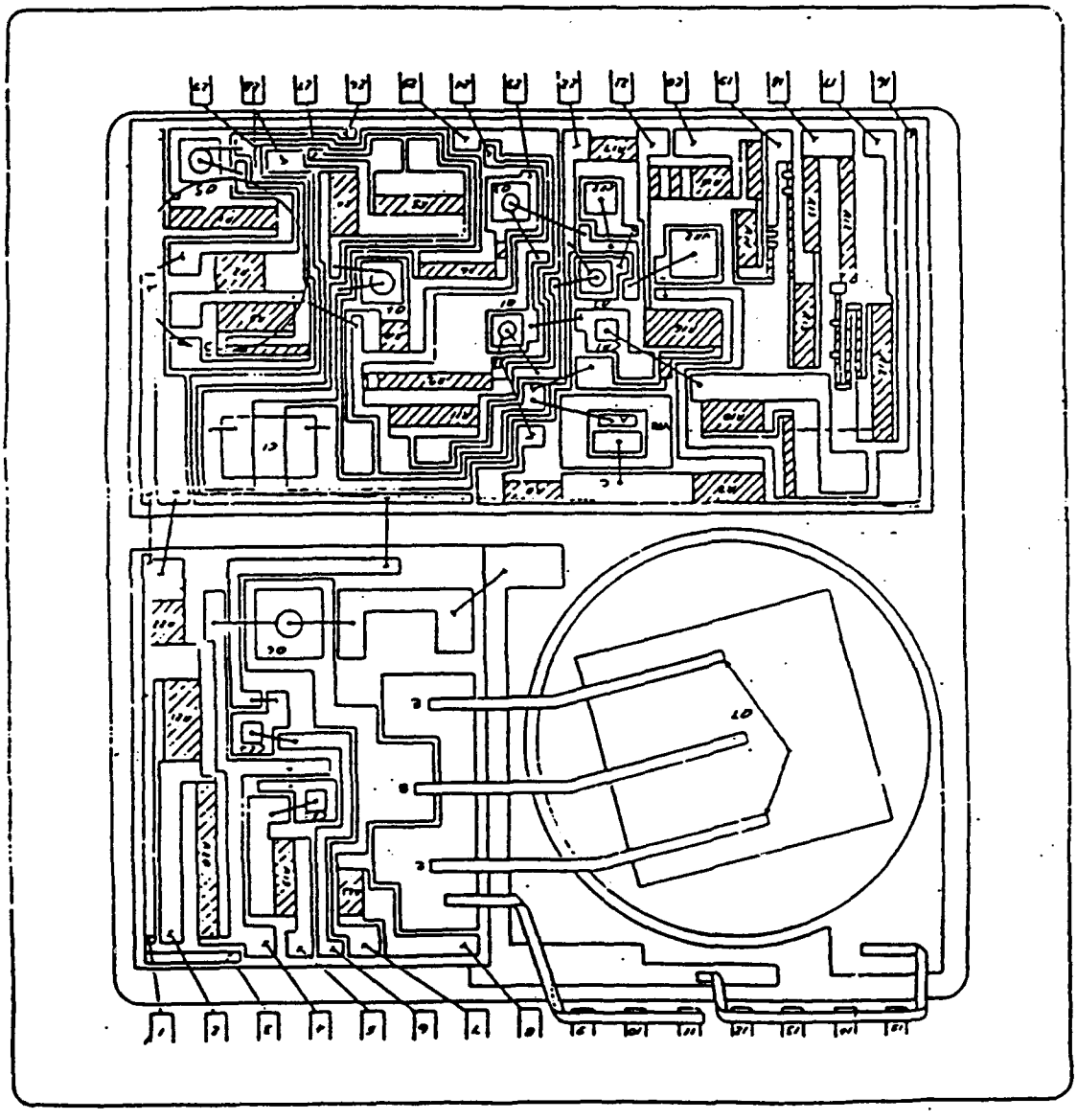

Figure W-2. Positive and Negative Voltage Regulator Hybrid Component Layout

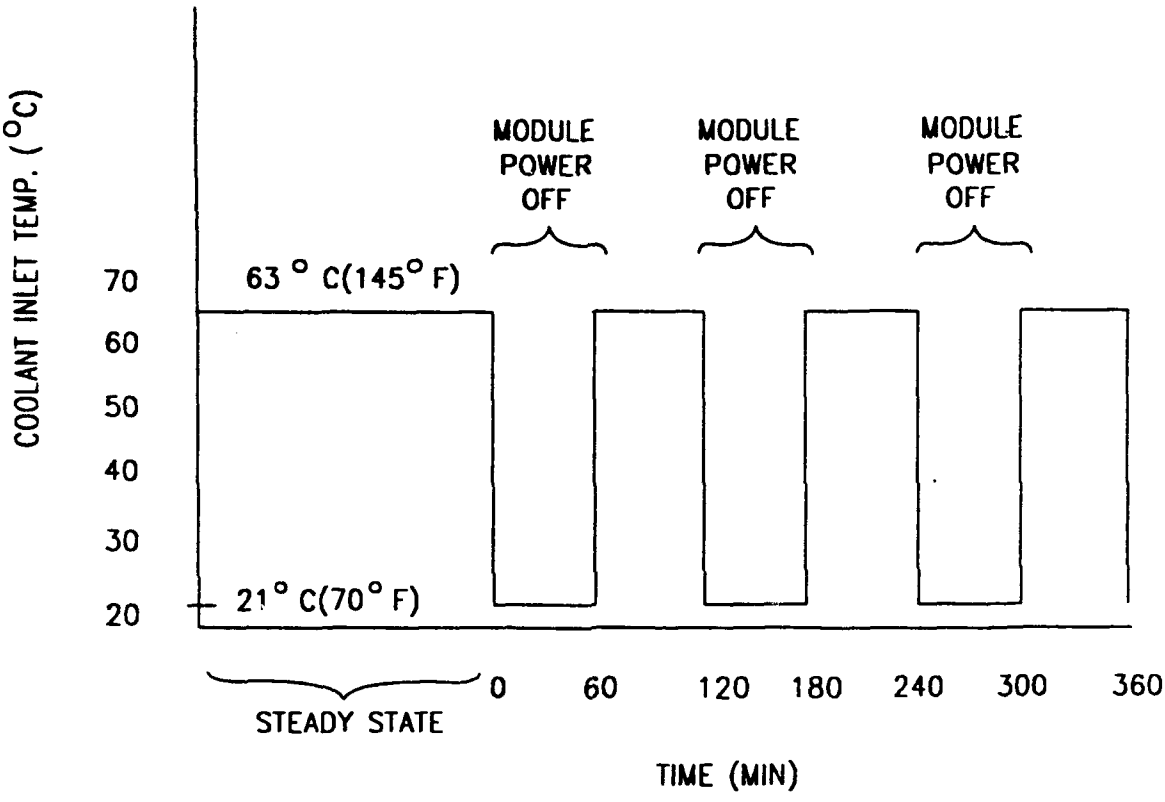

Figure W-3. F15 PSP Linear Regulator Module
CERT Environmental Profile

TABLE W-1
F-15 PSP LINEAR REGULATOR MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1	M39003/01-2544	0.000	68.	68.	
C2	M39003/01-2544	0.000	70.	70.	
C3	905570-49B	0.000	67.	67.	
C4	905570-103B	0.000	70.	70.	
C5	M39003/01-2541	0.000	67.	67.	
C6	M39003/01-2544	0.000	68.	68.	
C7	M39003/01-2544	0.000	68.	68.	
C8	905570-49B	0.000	66.	66.	
C9	905570-103B	0.000	66.	66.	
C10	M39003/01-2549	0.000	65.	65.	
C11	905570-49B	0.000	68.	68.	
C12	905570-103B	0.000	68.	68.	
C13	M39003/01-2549	0.000	68.	68.	
C14	M39003/01-2596	0.000	69.	69.	
C15	905570-55B	0.000	68.	68.	
C16	M39003/01-2552	0.000	70.	70.	
C17	M39003/01-2552	0.000	70.	70.	
CR2	JANTX1N3600	0.000	70.	70.	70.
CR3	JANTX1N5418	0.000	68.	68.	68.
CR4	JANTX1N3600	0.000	68.	68.	68.
CR5	JANTX1N3600	0.000	68.	68.	68.
CR7	JANTX2N2324	0.000	68.	68.	68.
Q1	928765-502B	3.580	77.	80.	83.
Q3	JANTX2N2907A	0.000	70.	70.	70.
Q4	JANTX2N2907A	0.000	69.	69.	69.
R1	RWR89SR237FP	0.059	70.	73.	
R2	RWR89SR237FP	0.059	70.	71.	
R3	RWR81S3650FP	0.130	70.	98.	
R4	RCR07G223JR	0.000	66.	66.	
R5	RWR80SR237FP	0.022	70.	73.	
R6	RWR80SR237FP	0.022	70.	71.	
R7	RNC60H2491FR	0.000	70.	70.	
R8	RWR80SR237FP	0.035	70.	72.	
R9	RWR81S3650FP	0.130	68.	96.	
R10	RCR07G223JR	0.000	65.	65.	
R11	RWR89SR511FP	0.015	68.	69.	
R12	RNC60H2491FR	0.000	68.	68.	
R13	RCR07G223JR	0.000	68.	68.	
R14	RWR80S1R00FP	0.000	68.	68.	
R15	RNC60H1540FR	0.000	68.	68.	
R16	RCR07G471JR	0.000	70.	70.	

TABLE W-1 (Continued)
F-15 PSP LINEAR REGULATOR MODULE
PRINTED WIRING BOARD

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
R17	RCR07G101JR	0.000	70.	70.	
R18	RCR07G102JR	0.000	70.	70.	
R20	RNC60H2611FR	0.000	68.	68.	
R21	RCR07G222JR	0.000	70.	70.	
R22	RCR07G332JR	0.000	70.	70.	
R23	RCR07G152JR	0.090	70.	88.	
R24	RNC60H6191FR	0.000	69.	69.	
R25	RNC60H6811FR	0.000	69.	69.	
R26	RCR07G681JR	0.000	69.	69.	
R27	RCR07G102JR	0.000	69.	69.	
R28	RCR07G330JR	0.000	69.	69.	
R29	RCR07G101JR	0.000	68.	68.	
R30	RWR80S1R00FP	0.000	68.	68.	
R31	RCR07G103JR	0.000	70.	70.	
R32	RCR07G133JR	0.000	70.	70.	
R33	RCR07G103JR	0.000	70.	70.	
R34	RCR07G752JR	0.000	70.	70.	
R35	RCR07G103JR	0.000	70.	70.	
R36	RCR07G103JR	0.000	70.	70.	
U1	934266-501B	2.260	74.	78.	79.
U2	934268-501B	1.030	70.	72.	72.
U3	934268-501B	0.037	69.	69.	69.
U4	H990446-001B	0.250	72.	85.	100.
VR1	JANTX1N964B	0.000	70.	70.	70.
VR2	JANTX1N827	0.050	70.	73.	83.

TOTAL OF PART DISSIPATIONS: 7.769 WATTS

TABLE W-2

F-15 PSP LINEAR REGULATOR MODULE

U1 -- POSITIVE VOLTAGE MREGULATOR HYBRID (DWG 934266)

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1	C1RONFO50K1006	0.000	74.	74.	
CR1	1N3600	0.000	74.	74.	74.
CR2	1N3600	0.000	74.	74.	74.
CR3	1N3600	0.000	74.	74.	74.
CR4	1N3600	0.000	74.	74.	74.
Q1	2N2484	0.000	74.	74.	74.
Q2	2N2484	0.000	74.	74.	74.
Q3	2N2907A	0.000	74.	74.	74.
Q4	2N2907A	0.000	74.	74.	74.
Q5	2N3501	0.000	74.	74.	74.
Q6	2N4236	0.000	74.	74.	74.
Q7	2N5303	2.260	74.	78.	79.
VR1	1N825	0.000	74.	74.	74.
VR2	1NZ49A	0.000	74.	74.	74.

TOTAL OF PART DISSIPATIONS: 2.26 WATTS

TABLE W-3

F-15 PSP LINEAR REGULATOR MODULE

U2 -- NEGATIVE VOLTAGE REGULATOR HYBRID (DWG 934268)

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1	C1RONFO50K1006	0.000	70.	70.	
CR1	1N3600	0.000	70.	70.	70.
CR2	1N3600	0.000	70.	70.	70.
CR3	1N3600	0.000	70.	70.	70.
CR4	1N3600	0.000	70.	70.	70.
Q1	2N2484	0.000	70.	70.	70.
Q2	2N2484	0.000	70.	70.	70.
Q3	2N2907A	0.000	70.	70.	70.
Q4	2N2907A	0.000	70.	70.	70.
Q5	2N3501	0.000	70.	70.	70.
Q6	2N4236	0.000	70.	70.	70.
Q7	2N5303	1.030	70.	72.	72.
VR1	1N825	0.000	70.	70.	70.
VR2	1NZ49A	0.000	70.	70.	70.

TOTAL OF PART DISSIPATIONS: 1.030 WATTS

TABLE W-4

F-15 PSP LINEAR REGULATOR MODULE

U3 -- NEGATIVE VOLTAGE REGULATOR HYBRID (DWG 934268)

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)	JUNCTION TEMP (DEG C)
C1	C1RONFO50K1006	0.000	69.	69.	
CR1	1N3600	0.000	69.	69.	69.
CR2	1N3600	0.000	69.	69.	69.
CR3	1N3600	0.000	69.	69.	69.
CR4	1N3600	0.000	69.	69.	69.
Q1	2N2484	0.000	69.	69.	69.
Q2	2N2484	0.000	69.	69.	69.
Q3	2N2907A	0.000	69.	69.	69.
Q4	2N2907A	0.000	69.	69.	69.
Q5	2N3501	0.000	69.	69.	69.
Q6	2N4236	0.000	69.	69.	69.
Q7	2N5303	0.037	69.	69.	69.
VR1	1N825	0.000	69.	69.	69.
VR2	1NZ49A	0.000	69.	69.	69.

TOTAL OF PART DISSIPATIONS: 0.037 WATTS

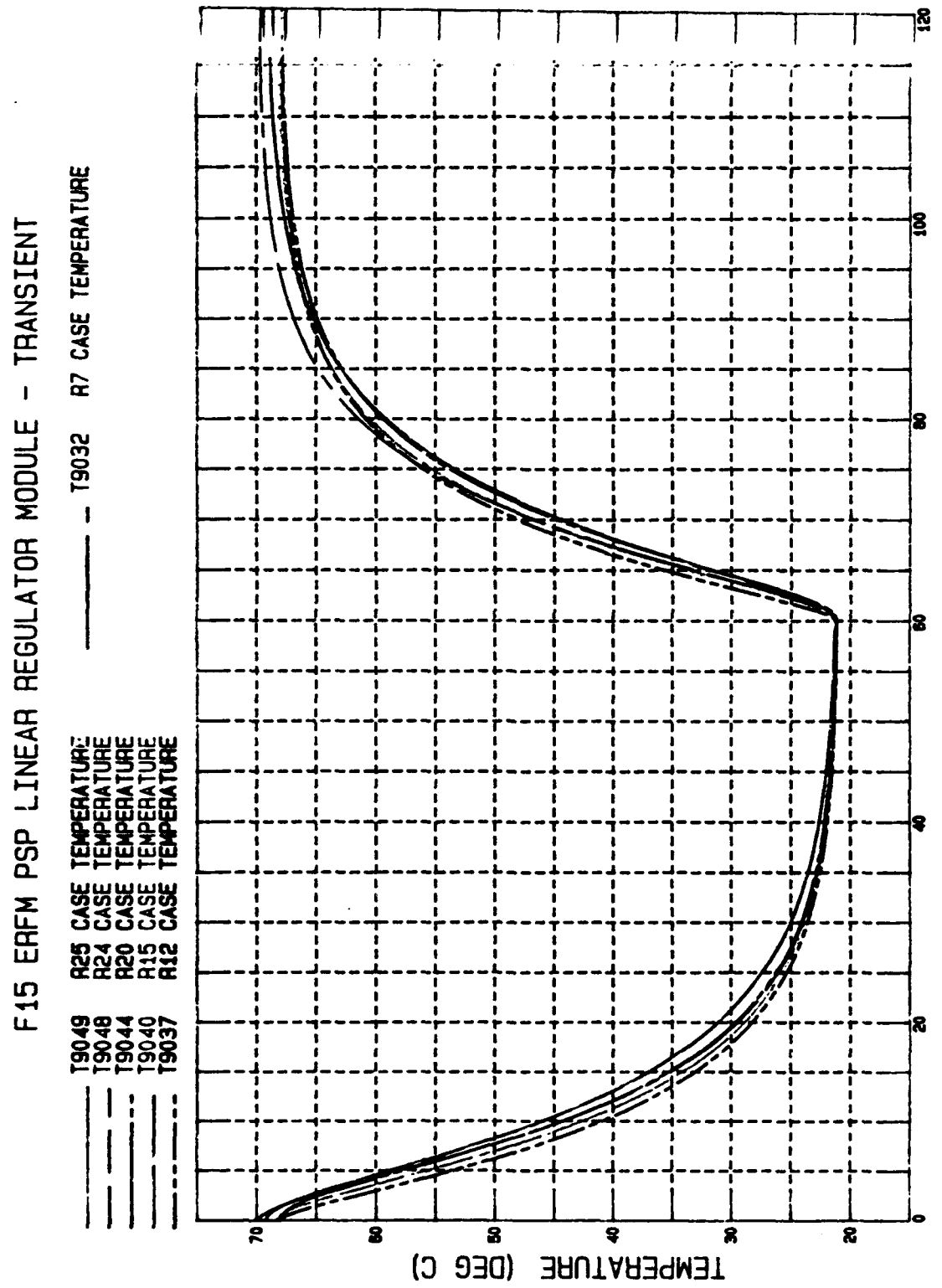

Figure W-4. Components with the Largest Time Constants

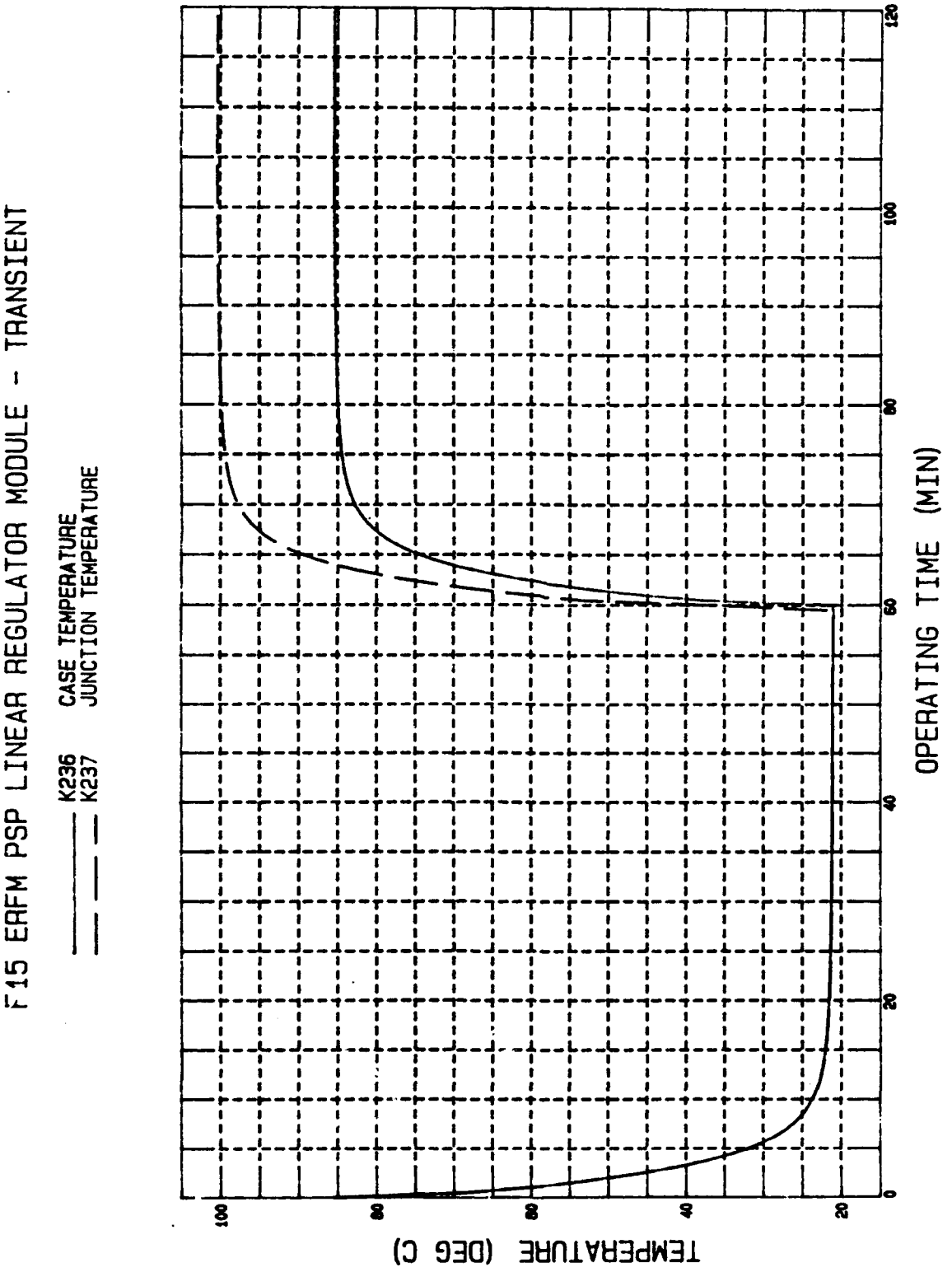

Figure W-5. Hottest Integrated Circuit (U4)

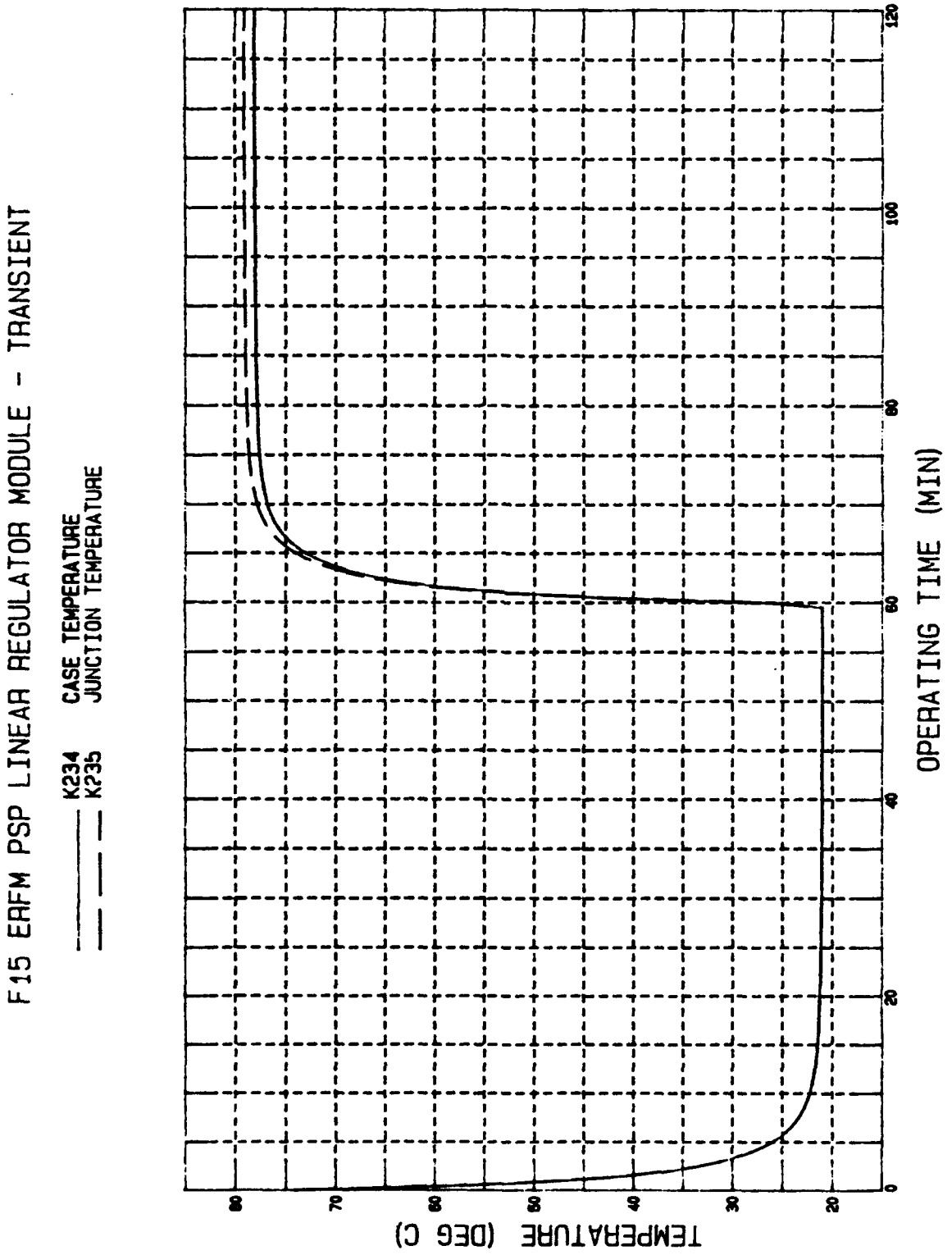

Figure W-6. Hottest Chip (Q7) Located Inside Hybrid U1

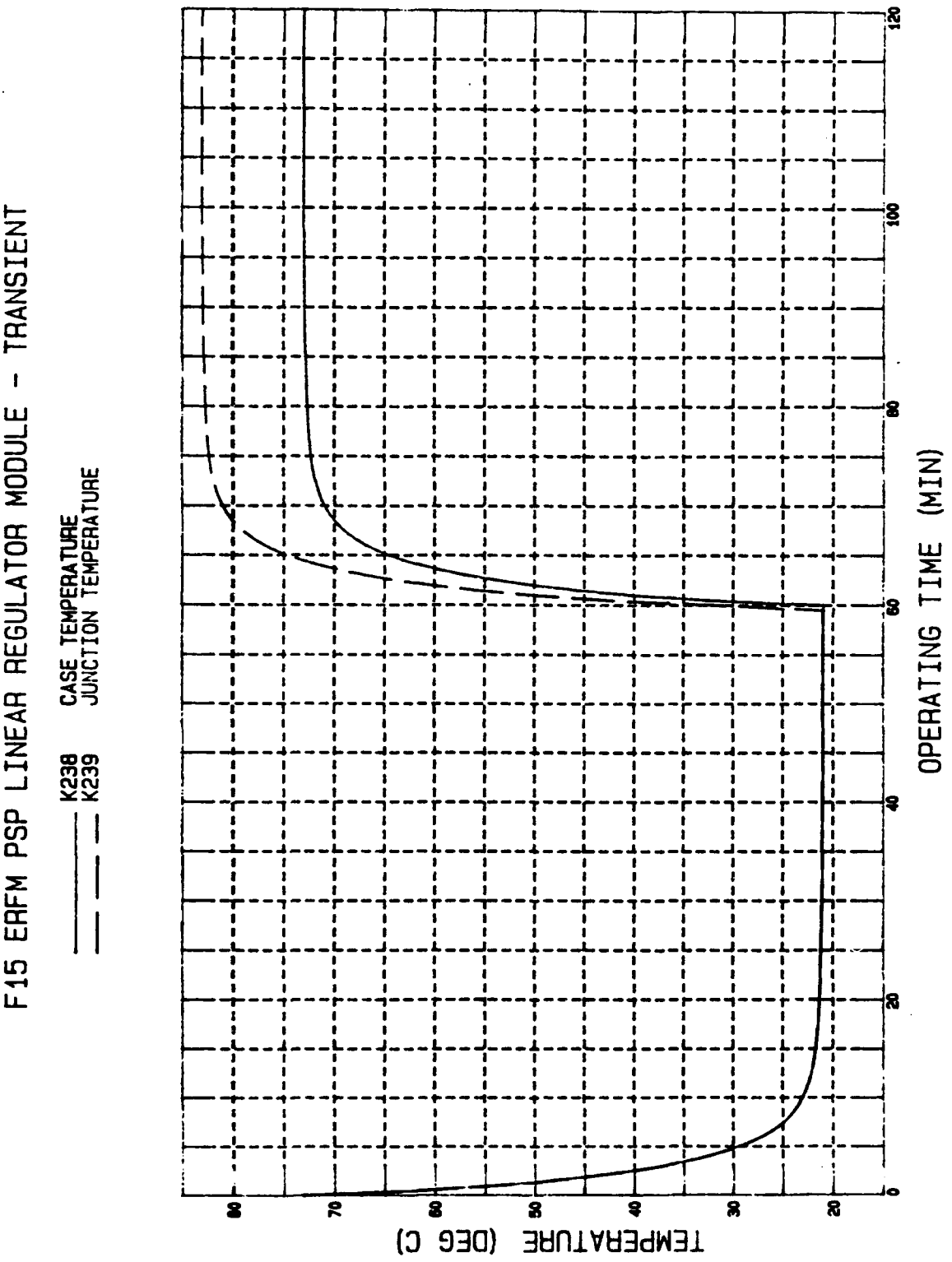

Figure W-7. Component with Highest Case to Junction ΔT (VR2)

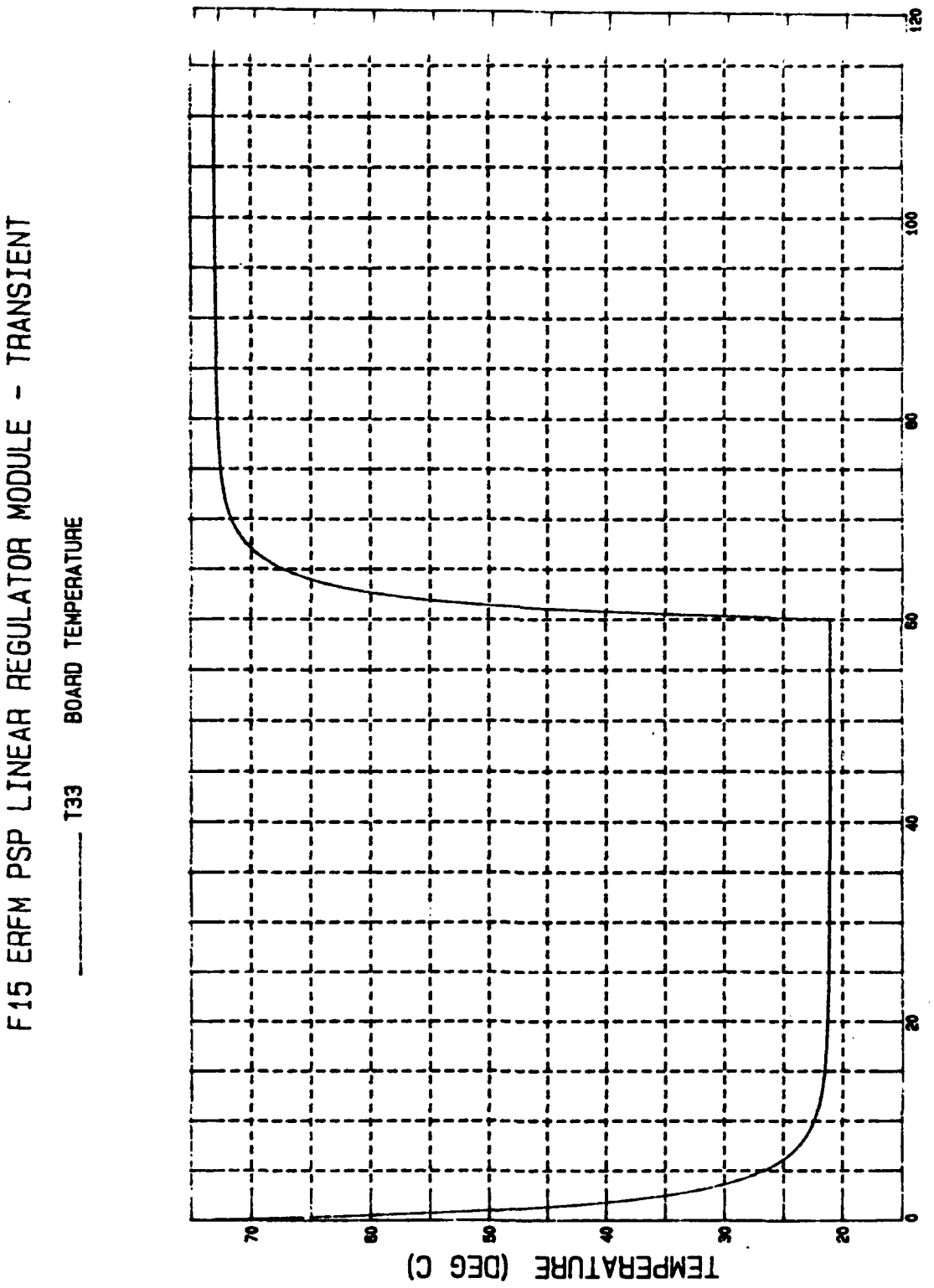

Figure W-8. Hottest Location on Printed Wiring Board

APPENDIX X

COMPARISON OF PREDICTED AND MEASURED TEMPERATURES FOR TIMING AND CONTROL MODULE

AVOID **VERBAL ORDERS**

J. M. Kallis	SOURCE CODE 72-26-10	LOC EO	BLDG E1	M/S B105	PHONE 616-6540
FROM W. J. Hoskins	SOURCE CODE 72-26-22	LOC EO	BLDG E1	M/S B104	PHONE 616-1121
SUBJECT F-15 PSP Timing and Control Module Analysis and Test Comparison				DATE 25 April 1991	

REFERENCE

IDC 722620/1292, "Thermal Analysis of the F-15 PSP Timing and Control Module," from W. J. Hoskins to R. D. Ritacco, dated September 2, 1988.

SUMMARY

A detailed steady state thermal analysis of the Programmable Signal Processor (PSP) Timing and Control (T&C) module for the F-15 aircraft had been performed and was documented in Reference 1. Since then, a thermal test has been performed on two identical T & C modules to determine the operating temperatures of selected components. The purpose of this document is to compare the test and analysis results.

The Timing and Control Module is a flow-through module that consists of two printed wiring boards(PWBs) mounted on a rectangular heat exchanger. The heat exchanger is made of rectangular plate finstock (7.0R-.125-.5(O)-.006Al) sandwiched between two 0.008 inch thick 6061-T6 Aluminum facesheets. The module power dissipation is taken to be 47.8 watts. The In-flight air inlet temperature is 29.4°C(85°F) at a flow rate of 0.202 lb/min. For the test an air inlet temperature of 27°C (81°F) is used. For comparison purposes the analytical results are based on the same 27°C (81°F) air inlet temperature.

RESULTS

The results of the test and analysis are provided in Table 1. This table provides measured temperatures for Modules 1 and 2 and the temperature predictions for the components whose temperatures were measured during the test.

The results indicate that components U1315 and U1601 have temperatures with the largest difference between the measured and analytical values. Component U1315 has a predicted temperature of 36°C and measured values of 46°C and 44°C for Modules 1 and 2, respectively. Component U1601 has a predicted temperature of 73°C and measured values of 59°C and 55°C for Modules 1 and 2, respectively. Notice that these components were predicted to have the minimum and maximum temperatures. Also, U1315 with the minimum temperature prediction has measured values greater than the prediction and conversely U1601 with the maximum temperature prediction has measured values lower than the prediction. This suggests that the temperature discrepancies might be due to the component temperatures being more coupled than in the analysis. More thermal coupling of the components would cause the temperatures of the components to be nearer the average, particularly those near the minimum and maximum.

The largest analytical uncertainty related to the thermal coupling of components occurs in the PWB. The PWB contains many partial copper ground planes whose thermal effects are accounted for by increasing the lateral thermal conductivity of the PWB. Therefore, an additional analysis was performed increasing the effective lateral thermal conductivity of the PWB from a conservative 0.34 watts/in-°C to a more realistic value of 0.914 watts/in-°C. The results of this analysis, provided in Table 2, show that the lateral conductivity is a minor factor contributing to the discrepancies. The revised temperature prediction for components U1315 and U1601 are 38°C and 72°C, respectively, only 2 and 1 degree different from the original prediction.

This indicates that there are other factors contributing to the discrepancy in the results. Most notably there may be inaccuracies in the component power dissipations, in addition there are typically flow leaks as large as 25 percent in a flow through module of this type. Both of these factors can substantially effect the test and analysis results. Neither the flow leaks nor the power were measured during the test , so they could not be compared to the analysis inputs. A report will be published which documents the details of the test procedure and results.

W. J. Hoskins, Staff Engineer

Approved by:

T. Rust, Senior Staff Engineer
THERMODYNAMICS DEPARTMENT

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T. L. Payne

TABLE X-1.

F15 PSP TIMING AND CONTROL MODULE CASE TEMPERATURE COMPARISON (°C)

Component	Measured Module 1	Measured Module 2	Predicted
C151	66 (1)	61 (-4)	65
U1315	46 (10)	44 (8)	36
U1401	59 (-5)	56 (-8)	64
U1508	64 (-1)	62 (-3)	65
U1601	59 (-14)	55 (-18)	73
U1611	59 (1)	58 (0)	58
U1703	63 (-2)	59 (-6)	65
U2217	58 (-6)	54 (-10)	64
U2616	63 (-3)	58 (-8)	66
U2707	61 (2)	57 (-2)	59

Note: Temperatures in parenthesis are measured minus predicted

TABLE X-2

F-15 PSP TIMING AND CONTROL STEADY STATE RESULTS
INCREASED LATERAL CONDUCTIVITY TO 0.914 W/IN-DEG C

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)
C1108I	905570-73B	0.000	50.	50.
C111	M39003/02-0079	0.000	57.	57.
C112	905570-73B	0.000	55.	55.
C113	905570-73B	0.000	53.	53.
C115	905570-73B	0.000	39.	39.
C116	905570-73B	0.000	35.	35.
C117	M39003/02-0079	0.000	35.	35.
C121	905570-73B	0.000	57.	57.
C122	905570-73B	0.000	56.	56.
C123	905570-73B	0.000	54.	54.
C124	M39003/02-0079	0.000	47.	47.
C125	905570-73B	0.000	39.	39.
C126	905570-73B	0.000	35.	35.
C127	905570-73B	0.000	32.	32.
C131	905570-73B	0.000	58.	58.
C132	905570-73B	0.000	57.	57.
C133	905570-73B	0.000	55.	55.
C134	905570-73B	0.000	49.	49.
C135	905570-73B	0.000	40.	40.
C136	905570-73B	0.000	36.	36.
C137	905570-73B	0.000	33.	33.
C141	M39003/02-0068	0.000	60.	60.
C1414G	M39003/02-0087	0.000	42.	42.
C1415C	905570-73B	0.000	37.	37.
C142	905570-73B	0.000	59.	59.
C143	905570-73B	0.000	57.	57.
C144	M39003/02-0068	0.000	52.	52.
C145	905570-73B	0.000	42.	42.
C146	905570-73B	0.000	37.	37.
C147	M39003/02-0068	0.000	34.	34.
C151	905570-73B	0.000	62.	62.
C152	905570-73B	0.000	61.	61.
C153	905570-73B	0.000	57.	57.
C154	905570-73B	0.000	53.	53.
C155	905570-73B	0.000	44.	44.
C156	905570-73B	0.000	39.	39.
C157	905570-73B	0.000	36.	36.
C162	905570-73B	0.000	60.	60.
C163	905570-73B	0.000	57.	57.
C164	905570-73B	0.000	53.	53.
C165	905570-73B	0.000	45.	45.

TABLE X-2 (Continued)

F-15 PSP TIMING AND CONTROL STEADY STATE RESULTS
INCREASED LATERAL CONDUCTIVITY TO 0.914 W/IN-DEG C

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)
C166	905570-73B	0.000	41.	41.
C167	905570-73B	0.000	37.	37.
C172	905570-73B	0.000	60.	60.
C173	905570-73B	0.000	58.	58.
C174	905570-73B	0.000	53.	53.
C175	905570-73B	0.000	47.	47.
C176	905570-73B	0.000	43.	43.
C177	905570-73B	0.000	40.	40.
C2104I	905570-73B	0.000	36.	36.
C211	905570-73B	0.000	33.	33.
C2110I	905570-73B	0.000	46.	46.
C2116I	905570-73B	0.000	55.	55.
C212	905570-73B	0.000	36.	36.
C213	905570-73B	0.000	39.	39.
C214	905570-73B	0.000	46.	46.
C215	905570-73B	0.000	52.	52.
C216	905570-73B	0.000	55.	55.
C221	905570-73B	0.000	33.	33.
C222	905570-73B	0.000	36.	36.
C223	905570-73B	0.000	40.	40.
C224	905570-73B	0.000	47.	47.
C225	905570-73B	0.000	54.	54.
C226	905570-73B	0.000	56.	56.
C227	905570-73B	0.000	58.	58.
C231	905570-73B	0.000	34.	34.
C232	905570-73B	0.000	37.	37.
C233	905570-73B	0.000	41.	41.
C234	905570-73B	0.000	48.	48.
C235	905570-73B	0.000	55.	55.
C236	905570-73B	0.000	57.	57.
C237	905570-73B	0.000	59.	59.
C241	M39003/02-0068	0.000	35.	35.
C242	905570-73B	0.000	40.	40.
C243	905570-73B	0.000	43.	43.
C244	M39003/02-0068	0.000	49.	49.
C245	905570-73B	0.000	56.	56.
C246	905570-73B	0.000	58.	58.
C247	M39003/02-0068	0.000	61.	61.
C251	905570-73B	0.000	37.	37.
C252	905570-73B	0.000	41.	41.
C253	905570-73B	0.000	45.	45.

TABLE X-2 (Continued)

F-15 PSP TIMING AND CONTROL STEADY STATE RESULTS
INCREASED LATERAL CONDUCTIVITY TO 0.914 W/IN-DEG C

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)
C254	905570-73B	0.000	50.	50.
C255	905570-73B	0.000	57.	57.
C256	905570-73B	0.000	60.	60.
C257	905570-73B	0.000	61.	61.
C261	905570-73B	0.000	39.	39.
C262	905570-73B	0.000	43.	43.
C263	905570-73B	0 000	47.	47.
C264	905570-73B	0.000	51.	51.
C265	905570-73B	0.000	57.	57.
C266	905570-73B	0.000	60.	60.
C267	905570-73B	0.000	61.	61.
C271	905570-73B	0.000	40.	40.
C272	905570-73B	0.000	44.	44.
C273	905570-73B	0.000	47.	47.
C274	905570-73B	0.000	52.	52.
C275	905570-73B	0.000	58.	58.
C276	905570-73B	0.000	59.	59.
C277	905570-73B	0.000	60.	60.
CR1111G	JANTX1N4150-1	0.000	43.	43.
CR1115A	JANTX1N4150-1	0.000	35.	35.
CR1215A	JANTX1N4150-1	0.000	35.	35.
CR1215C	JANTX1N4150-1	0.000	35.	35.
CR1316A	925974-1B	0.000	36.	36.
R1103	M8340103M27ROJA	0.070	55.	57.
R1106	955230-8B	0.100	53.	89.
R1111A	RCR07G101JS	0.040	43.	43.
R1111C	RCR07G512JS	0.040	43.	43.
R1111E	RCR07G100JS	0.040	43.	43.
R1112B	RLR32C348FP	0.040	43.	44.
R1112F	RLR32C348FP	0.040	43.	44.
R1113B	RLR32C348FP	0.040	39.	40.
R1113F	RLR32C348FP	0.040	39.	40.
R1114B	RLR32C348FP	0.040	39.	40.
R1114F	RLR32C348FP	0.040	39.	40.
R1115C	RCR07G100JS	0.040	35.	36.
R1116	M8340103M27ROJA	0.070	35.	37.
R114	RCR07G121JS	0.040	47.	47.
R1215E	RCR07G270JS	0.040	35.	36.
R1303E	RCR07G270JS	0.040	57.	58.
R1303G	RCR07G270JS	0.040	57.	58.
R1414A	RCR07G152JS	0.040	42.	42.

TABLE X-2 (Continued)

F-15 PSP TIMING AND CONTROL STEADY STATE RESULTS
INCREASED LATERAL CONDUCTIVITY TO 0.914 W/IN-DEG C

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)
R1414C	RCR07G102JS	0.040	42.	42.
R1414E	RCR07G100JS	0.040	42.	42.
R1415A	RCR07G392JS	0.040	37.	38.
R1415E	RCR07G820JS	0.040	37.	38.
R1415G	RCR07G330JS	0.040	37.	38.
R217	RNC50H3161FS	0.070	57.	60.
R2105	M8340103M27ROJA	0.070	39.	41.
R2107	M8340103M27ROJA	0.070	43.	44.
R2113	M8340103M27ROJA	0.070	52.	54.
R2116	M8340103M27ROJA	0.070	55.	57.
R2117	M8340103M27ROJA	0.070	57.	58.
R2118	M8340103M27ROJA	0.070	57.	58.
U1101	932849-1B	0.300	57.	64.
U1102	932849-1B	0.300	57.	64.
U1104	932783-2B	0.092	55.	57.
U1105	M38510/30003BDX	0.013	53.	53.
U1107	932730-2B	0.173	50.	53.
U1108	M38510/07001BDX	0.079	50.	51.
U1109	932730-2B	0.173	47.	50.
U1110	932730-2B	0.173	47.	50.
U1203	932849-1B	0.300	56.	63.
U1204	932783-2B	0.092	56.	58.
U1205	932730-2B	0.173	54.	58.
U1206	932614-3B	0.473	54.	64.
U1207	M38510/07003BDX	0.118	51.	53.
U1208	M38510/07301BDX	0.113	51.	53.
U1209	M38510/07003BDX	0.118	47.	50.
U1210	M38510/07003BDX	0.118	47.	50.
U1211	932820-226	0.472	44.	52.
U1216	M38510/07003BDX	0.118	35.	38.
U1304	932616-501B	0.100	57.	59.
U1305	M38510/07003BDX	0.118	55.	57.
U1306	M38510/07001BDX	0.079	55.	57.
U1307	932614-3B	0.473	53.	63.
U1308	M38510/34102BFX	0.168	53.	56.
U1309	932614-3B	0.473	49.	59.
U1310	M38510/34102BFX	0.168	49.	53.
U1311	932756-1B	0.100	45.	47.
U1312	932756-1B	0.100	45.	47.
U1313	932783-2B	0.092	40.	42.
U1314	932783-2B	0.092	40.	42.

TABLE X-2 (Continued)

F-15 PSP TIMING AND CONTROL STEADY STATE RESULTS
INCREASED LATERAL CONDUCTIVITY TO 0.914 W/IN-DEG C

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)
U1315	928063-501B	0.095	36.	38.
U1401	932730-2B	0.173	60.	64.
U1402	M38510/07401BDX	0.057	60.	61.
U1403	M38510/07401BDX	0.057	59.	60.
U1404	932614-3B	0.473	59.	69.
U1405	M38510/07001BDX	0.079	57.	58.
U1406	932614-3B	0.473	57.	67.
U1407	932727-1B	0.447	55.	65.
U1408	932820-218	0.472	55.	63.
U1409	932727-1B	0.447	52.	61.
U1410	932727-1B	0.447	52.	61.
U1411	932614-3B	0.473	47.	57.
U1412	M38510/08001BDX	0.099	47.	49.
U1413	M38510/07001BDX	0.079	42.	44.
U1501	932709-1B	0..25	62.	74.
U1502	932709-1B	0.525	62.	74.
U1503	932709-1B	0.525	61.	72.
U1504	932614-3B	0.473	61.	71.
U1505	M38510/07003BDX	0.118	57.	60.
U1506	M38510/07009BFX	0.022	57.	58.
U1507	932709-1B	0.525	56.	68.
U1508	932820-217	0.472	56.	64.
U1509	932820-219	0.472	53.	61.
U1510	932820-220	0.472	53.	61.
U1511	M38510/07501BDX	0.263	48.	54.
U1512	932746-1B	0.342	48.	56.
U1513	932746-1B	0.342	44.	51.
U1514	M38510/30605BDX	0.084	44.	46.
U1515	M38510/30605BDX	0.084	39.	41.
U1516	M38510/30605BDX	0.084	39.	41.
U1517	M38510/30605BDX	0.084	36.	37.
U1518	932749-1B	0.158	36.	39.
U1601	930739-1B	0.100	60.	72.
U1603	932730-2B	0.173	60.	64.
U1604	M38510/54102BFX	0.168	60.	64.
U1605	M38510/07009BFX	0.022	57.	58.
U1606	M38510/08001BDX	0.099	57.	60.
U1607	932709-1B	0.525	57.	68.
U1608	932746-1B	0.342	57.	64.
U1609	932732-1B	0.289	53.	59.
U1610	932732-1B	0.289	53.	59.

TABLE X-2 (Continued)

F-15 PSP TIMING AND CONTROL STEADY STATE RESULTS
INCREASED LATERAL CONDUCTIVITY TO 0.914 W/IN-DEG C

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)
U1611	932820-215	0.472	50.	58.
U1612	M38510/07003BDX	0.118	50.	52.
U1613	932749-1B	0.158	45.	49.
U1614	932749-1B	0.158	45.	49.
U1615	932749-1B	0.158	41.	45.
U1616	932749-1B	0.158	41.	45.
U1617	932749-1B	0.158	37.	41.
U1618	932749-1B	0.158	37.	41.
U1703	932730-2B	0.173	60.	64.
U1704	932709-1B	0.525	60.	71.
U1705	932709-1B	0.525	58.	69.
U1706	932690-1B	0.053	58.	59.
U1707	932746-1B	0.342	56.	64.
U1708	932746-1B	0.342	56.	64.
U1709	932732-1B	0.289	53.	59.
U1710	932732-1B	0.289	53.	59.
U1711	932820-224	0.472	50.	58.
U1712	M38510/33701BFX	0.033	50.	51.
U1713	932746-1B	0.342	47.	54.
U1714	932746-1B	0.342	47.	54.
U1715	932746-1B	0.342	43.	51.
U1716	932746-1B	0.342	43.	51.
U1717	932746-1B	0.342	40.	47.
U1718	932746-1B	0.342	40.	47.
U2101	M38510/07003BDX	0.118	33.	36.
U2102	M38510/07003BDX	0.118	33.	36.
U2103	M38510/07003BDX	0.118	36.	38.
U2104	M38510/07003BDX	0.118	36.	38.
U2106	932849-1B	0.300	39.	46.
U2108	932849-1B	0.300	43.	49.
U2109	932730-2B	0.173	46.	50.
U2110	932730-2B	0.173	46.	50.
U2111	932730-2B	0.173	50.	53.
U2112	932730-2B	0.173	50.	53.
U2114	932728-1B	0.079	52.	54.
U2115	932728-1B	0.079	55.	57.
U2201	932726-1B	0.084	33.	35.
U2202	932726-1B	0.084	33.	35.
U2203	M38510/07003BDX	0.118	36.	39.
U2204	H990436-001B	0.122	36.	39.
U2205	H990436-001B	0.122	40.	42.

TABLE X-2 (Continued)

F-15 PSP TIMING AND CONTROL STEADY STATE RESULTS
INCREASED LATERAL CONDUCTIVITY TO 0.914 W/IN-DEG C

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)
U2206	H990436-001B	0.122	40.	42.
U2207	H990436-001B	0.122	43.	46.
U2208	932726-1B	0.084	43.	45.
U2209	932726-1B	0.084	47.	48.
U2210	932728-1B	0.079	47.	48.
U2211	932728-1B	0.079	50.	52.
U2212	932728-1B	0.079	50.	52.
U2213	M38510/07003BDX	0.118	54.	56.
U2214	932849-1B	0.300	54.	60.
U2215	M38510/07003BDX	0.118	56.	59.
U2216	932849-1B	0.300	56.	63.
U2217	932849-1B	0.300	58.	65.
U2218	932849-1B	0.300	58.	65.
U2301	M38510/07301BDX	0.113	34.	36.
U2302	932728-1B	0.079	34.	35.
U2303	932728-1B	0.079	37.	39.
U2304	932749-1B	0.158	37.	40.
U2305	932749-1B	0.158	41.	44.
U2306	932749-1B	0.158	41.	44.
U2307	932749-1B	0.158	45.	48.
U2308	932749-1B	0.158	45.	48.
U2309	932749-1B	0.158	48.	51.
U2310	H990436-001B	0.122	48.	51.
U2311	M38510/08001BDX	0.099	51.	53.
U2312	M38510/30301BDX	0.012	51.	51.
U2313	932728-1B	0.079	55.	56.
U2314	H990436-001B	0.122	55.	57.
U2315	H990436-001B	0.122	57.	60.
U2316	M38510/07001BDX	0.079	57.	59.
U2317	932685-1B	0.035	59.	59.
U2318	M38510/30001BDX	0.008	59.	59.
U2401	M38510/07301BDX	0.113	35.	38.
U2402	932736-1B	0.394	35.	44.
U2403	932736-1B	0.394	40.	48.
U2404	932736-1B	0.394	40.	48.
U2405	932736-1B	0.394	43.	52.
U2406	932736-1B	0.394	43.	52.
U2407	932736-1B	0.394	46.	55.
U2408	932690-1B	0.053	46.	48.
U2409	932690-1B	0.053	49.	50.
U2410	932756-1B	0.100	49.	51.

TABLE X-2 (Continued)

F-15 PSP TIMING AND CONTROL STEADY STATE RESULTS
INCREASED LATERAL CONDUCTIVITY TO 0.914 W/IN-DEG C

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)
U2411	M38510/30301BDX	0.012	52.	53.
U2412	M38510/07001BDX	0.079	52.	54.
U2413	M38510/07003BDX	0.118	56.	59.
U2414	932614-3B	0.473	56.	67.
U2415	932756-1B	0.100	58.	61.
U2416	932756-1B	0.100	58.	61.
U2417	932614-3B	0.473	61.	71.
U2418	M38510/07005BDX	0.059	61.	62.
U2501	932728-1B	0.079	37.	39.
U2502	932736-1B	0.394	37.	45.
U2503	932736-1B	0.394	41.	50.
U2504	932736-1B	0.394	41.	50.
U2505	932736-1B	0.394	45.	54.
U2506	932736-1B	0.394	45.	54.
U2507	932736-1B	0.394	48.	56.
U2508	932690-1B	0.053	48.	49.
U2509	932690-1B	0.053	50.	52.
U2510	932756-1B	0.100	50.	53.
U2511	M38510/07001BDX	0.079	54.	55.
U2512	M38510/07003BDX	0.118	54.	56.
U2513	932614-3B	0.473	57.	67.
U2514	M38510/08001BDX	0.099	57.	60.
U2515	M38510/07401BDX	0.057	60.	61.
U2516	932614-3B	0.473	60.	70.
U2517	932727-1B	0.447	61.	71.
U2518	M38510/07003BDX	0.118	61.	64.
U2601	932736-1B	0.394	39.	47.
U2602	932736-1B	0.394	39.	47.
U2603	932736-1B	0.394	43.	51.
U2604	932736-1B	0.394	43.	51.
U2605	932736-1B	0.394	47.	55.
U2606	932736-1B	0.394	47.	55.
U2607	932736-1B	0.394	49.	57.
U2608	932690-1B	0.053	49.	50.
U2609	932690-1B	0.053	51.	52.
U2610	932756-1B	0.100	51.	53.
U2611	M38510/07001BDX	0.079	54.	56.
U2612	932690-1B	0.053	54.	55.
U2613	M38510/34102BFX	0.168	57.	61.
U2614	M38510/30502BDX	0.032	57.	58.
U2615	M38510/07003BDX	0.118	60.	62.

TABLE X-2 (Continued)

F-15 PSP TIMING AND CONTROL STEADY STATE RESULTS
INCREASED LATERAL CONDUCTIVITY TO 0.914 W/IN-DEG C

CIRCUIT SYMBOL	PART NUMBER	POWER (WATTS)	MOUNTING SURFACE TEMP (DEG C)	CASE TEMP (DEG C)
U2616	M38510/33901BFX	0.237	60.	65.
U2617	M38510/08001BDX	0.099	61.	63.
U2618	M38510/07001BDX	0.079	61.	62.
U2701	932736-1B	0.394	40.	49.
U2702	932736-1B	0.394	40.	49.
U2703	932736-1B	0.394	44.	52.
U2704	932736-1B	0.394	44.	52.
U2705	932736-1B	0.394	47.	56.
U2706	932736-1B	0.394	47.	56.
U2707	932736-1B	0.394	50.	58.
U2708	932690-1B	0.053	50.	51.
U2709	932690-1B	0.053	52.	53.
U2710	932756-1B	0.100	52.	54.
U2711	M38510/07003BDX	0.118	55.	57.
U2712	932690-1B	0.053	55.	56.
U2713	932746-1B	0.342	58.	65.
U2714	M38510/07001BDX	0.079	58.	59.
U2715	M38510/34102BFX	0.168	59.	63.
U2716	M38510/07001BDX	0.079	59.	61.
U2717	M38510/07003BDX	0.118	60.	62.

TOTAL OF PART DISSIPATIONS: 47.766 WATTS

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