SMC-TR-92-36

AEROSPACE REPORT NO.
TR-0091(6940-05)-3

On the Suitability of Non-Hardened High Density SRAMs for Space Applications

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16 July 1992

Prepared for

SPACE AND MISSILE SYSTEMS CENTER
AIR FORCE MATERIEL COMMAND
Los Angeles Air Force Base
P.O. Box 92960
Los Angeles, CA 90009-2960

Contract No. F04701-88-C-0089

Engineering and Technology Group

THE AEROSPACE CORPORATION
El Segundo, California

This report was submitted by The Aerospace Corporation, El Segundo, CA 90245-4691, under Contract No. F04701-88-C-0089 with the Space and Missile Systems Center, P.O. Box 92960, Los Angeles, CA 90009-2960. It was reviewed and approved for The Aerospace Corporation by A. B. Christensen, Principal Director, Space and Environment Technology Center. Capt. Tyron Fisher was the project officer for the Mission-Oriented Investigation and Experimentation (MOIE) Program.

This report has been reviewed by the Public Affairs Office (PAS) and is releasable to the National Technical Information Service (NTIS). At NTIS, it will be available to the general public, including foreign nationals.

This technical report has been reviewed and is approved for publication. Publication of this report does not constitute Air Force approval of the report's findings or conclusions. It is published only for the exchange and stimulation of ideas.

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UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE

REPORT DOCUMENTATION PAGE

1a. REPORT SECURITY CLASSIFICATION Unclassified	1b. RESTRICTIVE MARKINGS
2a. SECURITY CLASSIFICATION AUTHORITY	3. DISTRIBUTION/AVAILABILITY OF REPORT Approved for public release; distribution unlimited
2b. DECLASSIFICATION/DOWNGRADING SCHEDULE	
4. PERFORMING ORGANIZATION REPORT NUMBER(S) TR-0091(6940-05)-3	5. MONITORING ORGANIZATION REPORT NUMBER(S) SMC-TR-92-36
6a. NAME OF PERFORMING ORGANIZATION The Aerospace Corporation Technology Operations 6b. OFFICE SYMBOL (If applicable)	7a. NAME OF MONITORING ORGANIZATION Space and Missile Systems Center
6c. ADDRESS (City, State, and ZIP Code) El Segundo, CA 90245-4691	7b. ADDRESS (City, State, and ZIP Code) Los Angeles, Air Force Base Los Angeles, CA 90009-2960
8a. NAME OF FUNDING/SPONSORING ORGANIZATION 8b. OFFICE SYMBOL (If applicable)	9. PROCUREMENT INSTRUMENT IDENTIFICATION NUMBER F04701-88-C-0089
8c. ADDRESS (City, State, and ZIP Code)	10. SOURCE OF FUNDING NUMBERS PROGRAM ELEMENT NO. / PROJECT NO. / TASK NO. / WORK UNIT ACCESSION NO.

11. TITLE (Include Security Classification)

On the Suitability of Non-Hardened High Density SRAMs for Space Applications

12. PERSONAL AUTHOR(S) Koga, R.; Crain, W. R.; Crawford, K. B.; Lau, D. D.; Pinkerton, S. D. (The Aerospace Corporation) Yi, B. K. (Fairchild Space Company) and Chitty, R. (CTA)

13a. TYPE OF REPORT	13b. TIME COVERED	14. DATE OF REPORT (Year, Month, Day)	15. PAGE COUNT
	FROM _____ TO _____	1992 July 16	21

16. SUPPLEMENTARY NOTATION

17. COSATI CODES			18. SUBJECT TERMS (Continue on reverse if necessary and identify by block number)
FIELD	GROUP	SUB-GROUP	Single-event upset

19. ABSTRACT (Continue on reverse if necessary and identify by block number)

Several non-radiation-hardened high density static RAMs (SRAMs) were tested for susceptibility to single-event upset (SEU) and latchup. Test results indicated that at present only a few such device types are suitable for use in space applications. Several additional factors such as susceptibility to multiple-bit upsets and to radiation-induced permanent damage need to be taken into consideration before these device types can be recommended. One non-hardened SRAM device type has recently been used on a low-Earth orbit satellite, enabling the upset rate measured in space to be compared to that predicted from ground-based testing.

20. DISTRIBUTION/AVAILABILITY OF ABSTRACT	21. ABSTRACT SECURITY CLASSIFICATION
[X] UNCLASSIFIED/UNLIMITED [ ] SAME AS RPT. [ ] DTIC USERS	Unclassified

22a. NAME OF RESPONSIBLE INDIVIDUAL	22b. TELEPHONE (Include Area Code)	22c. OFFICE SYMBOL

DD FORM 1473, 84 MAR

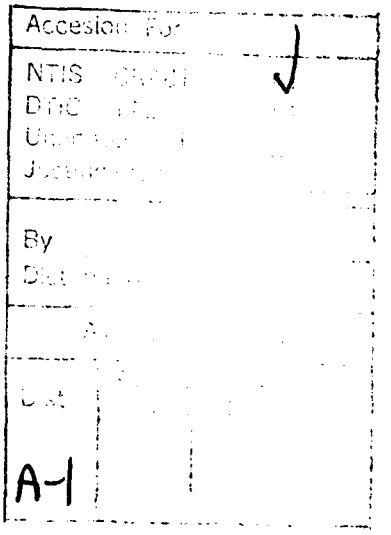
83 APR edition may be used until exhausted.
All other editions are obsolete.

SECURITY CLASSIFICATION OF THIS PAGE

UNCLASSIFIED

PREFACE

We would like to thank our Aerospace colleagues R. L. Walter, B. M. Johnson, M. Lalic, and S. H. Penzin for their generous assistance during the test preparation and the data collection periods. Thanks are also extended to members of the LBL 88-inch cyclotron staff for beam delivery.



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I. INTRODUCTION

In general, non-radiation-hardened high density static RAMs (SRAMs) offer a number of advantages over comparable radiation-hardened devices, including lower costs, greater availability, and higher density dies. Recent test reults indicate that a few non-hardened SRAM device types exhibit sufficiently low susceptibilities to single-event upset (SEU) and immunity to latchup to be considered for future space applications. However, a number of additional factors must be taken into account before non-hardened devices can be recommended for such applications. Among the factors that must be considered are the device's susceptibilities to multiple-bit upsets and permanently "stuck" bits, and the possibility of degradation due to total dose exposure.

After careful consideration of their predicted survivability in space, non-radiation-hardened high density SRAMs utilizing Hitachi 256K-bit dies were selected for use in the memory bank of a low-Earth orbiting satellite. These devices have been exposed to the space radiation environment continuously since the satellite first entered orbit; hence it is now possible to compare the measured upset rate in space for this SRAM type with the rate predicted from ground-based test data.

II. GROUND-BASED TEST PROCEDURES AND RESULTS

We have recently tested several 1 megabit (128K x 8) SRAMs for single-event upset (SEU) and latchup, along with a number of 256K-bit SRAMs, as summarized in Table 1. The test devices were irradiated at the Lawrence Berkeley Laboratory 88-inch cyclotron facility using the following ion beams: xenon (603 MeV), krypton (380 MeV), copper (290 MeV), argon (180 MeV), neon (90 MeV), nitrogen (67 MeV), and hydrogen (20, 30, and 55 MeV). The linear energy transfer (LET) values of the non-hydrogen beams were 63, 41, 30, 15, 5.6, and 3 MeV/(mg/cm^2), respectively. (Effective LET values may be obtained by dividing the actual LET by the cosine of the exposure angle.)

All tests were conducted using a proprietary, device-independent SRAM tester called the General Memory Interrogation Board (GMIB). The GMIB tester was interfaced with an Apple Macintosh computer which performed the following functions: (1) specified SRAM-specific parameters such as memory organization and read/write access times; (2) automatically recorded all relevant test information, including beam fluence and position of the test device; (3) calculated SEU and latchup cross-sections (see below), and generated a plot showing the calculated cross-sections as a function of LET; and (4) recorded test results in mass storage media to facilitate future analysis (for example, the stored data have been useful in classifying multiple-bit errors).

The cross-section, σ, is calculated using the equation:

$$\sigma = (N/F) \sec \theta$$

where N is the number of errors (counting multiple-bit errors separately), F is the beam fluence in particles/cm^2, and θ is the angle between the beam and the chip-surface normal [1].

The bias current was continuously monitored by the computer during the exposure to ions, so that latchup, if it occurred, could be recognized immediately. If it was found that a device was susceptible to latchup, the Macintosh computer was operated thereafter in such a manner as to measure the latchup sensitivity, essentially disregarding soft errors (SEU).

A brief summary of the SRAM test results is given in Table 1, which lists threshold LET values and saturation cross sections for both SEU and latchup (see also [2]). More expansive summaries of the test results are provided by cross section vs LET plots (Figures 1 through 6) for the following device types: Mosaic MSM8128SLMB, Micron Technology MT5C1008C-25, Sony CXK581000P, Sony CXK58255P, Micron Technology MT5C2568, and NEC UPD43256A, respectively. The test results for the Hitachi HM658128LP are quite similar to those for MSM8128SLMB (the same Hitachi die is used in both). As noted above, cross sections were calculated by treating all upset bits separately. Therefore, the physical sensitive regions may be somewhat smaller than the saturation cross sections indicated in the figures.

Table 1. Summary of High Density SRAM Test Results

Device Type	Manufacturer (Die type if not Mfr's)	Technology	Organization	Feature Size	SEU		Latchup	
					LET_{TH}	X-Sec	LET_{TH}	X-Sec
HM658128LP†	Hitachi	CMOS/NMOS	128K x 8	≈1 μm	4	$1x10^{0}$	72	$3x10^{-6}$
MSM8128SLMB†	Mosaic (Hitachi)	CMOS/NMOS	128K x 8	≈1 μm	4	$1x10^{0}$	72	$3x10^{-6}$
MT5C1008C-25~	Micron Technology	CMOS/NMOS	128K x 8	≈1 μm	4	$2x10^{0}$	None	None
CXK581000P	Sony	CMOS/NMOS	128K x 8	1 μm	4	$7x10^{-2}$	50	$2x10^{-5}$
CXK58255P	Sony	CMOS (6-Trans)	32K x 8	0.8 μm	10	$1x10^{-1}$	25	$8x10^{-4}$
MT5C2568~	Micron Technology	CMOS/NMOS	32K x 8	≈1 μm	3	$9x10^{-1}$	None	None
UPD43256A†	NEC	CMOS/NMOS	32K x 8	≈1 μm	3	$4x10^{-1}$	None	None
84256	Fujitsu	CMOS/NMOS	32K x 8	≈1 μm	3	$1x10^{0}$	30	$3x10^{-5}$
S32KX8	Seiko	CMOS/NMOS	32K x 8	1.3 μm	3	$1x10^{-1}$	30	$1x10^{-3}$
IDT71256*†~	IDT	CMOS/NMOS	32K x 8	1.3 μm	≈3	$2x10^{-1}$	None	None
XCDM62256*†	RCA (Seiko)	CMOS/NMOS	32K x 8	1.3 μm	≈3	$5x10^{-1}$	40	$1x10^{-3}$
EDH8832C*†	EDI (Mitsubishi)	CMOS/NMOS	32K x 8	1.3 μm	≈3	$4x10^{-1}$	20	$2x10^{-3}$
OW62256*†	Omni-Wave (Hitachi)	CMOS/NMOS	32K x 8	1.3 μm	≈3	$4x10^{-1}$	None	None

* The susceptibilities of these devices are reported elsewhere [2].

† Tested for proton induced single event upset.

~ These devices incorporate an epitaxial layer.

(1) Threshold LETs given in MeV/(mg/cm^2).

(2) Saturation cross-sections given in cm2/device.

(3) "None" indicates a cross-section < 10^{-7} cm^2/device at an LET of 100 MeV/(mg/cm^2).

A recent article [3] has shown that a device is likely to be susceptible to proton-induced upsets if the threshold LET for heavy ion-induced SEU is less than about 8 MeV/(mg/cm^2), and that an empirical relationship exists between the SEU susceptibility measured with protons and the susceptibility as measured with heavy ions. Hence, given the heavy ion-induced SEU rate for a device, the proton upset rate may be obtained without subjecting the device to proton irradiation. Nevertheless, some proton tests were performed, as indicated in Table 1. Specifically, the vulnerability (upset cross section) of the Hitachi 128K x 8 SRAM dies to 50 MeV protons was about 1 x 10^{-7} cm^2/device, whereas UPD43256A had a cross section between 1 x 10^{-11} and 1 x 10^{-10} cm^2/device.

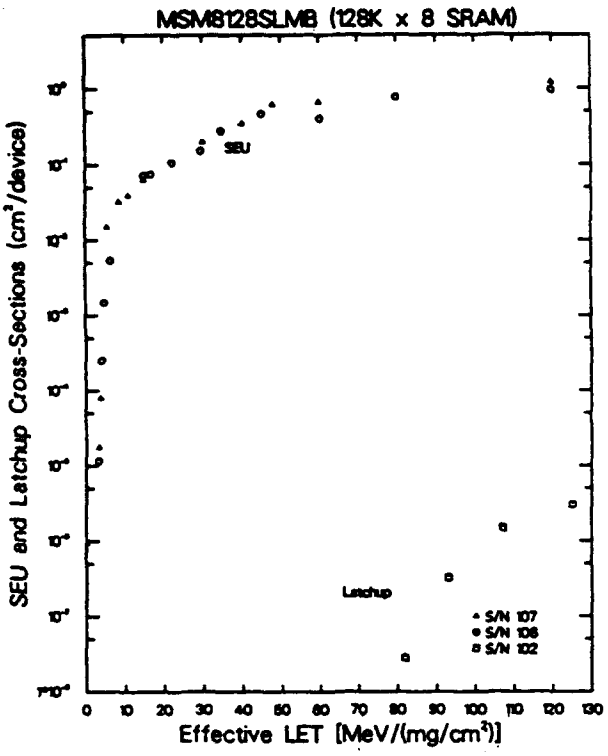

Figure 1. SEU and Latchup Results for MSM8128SLMB

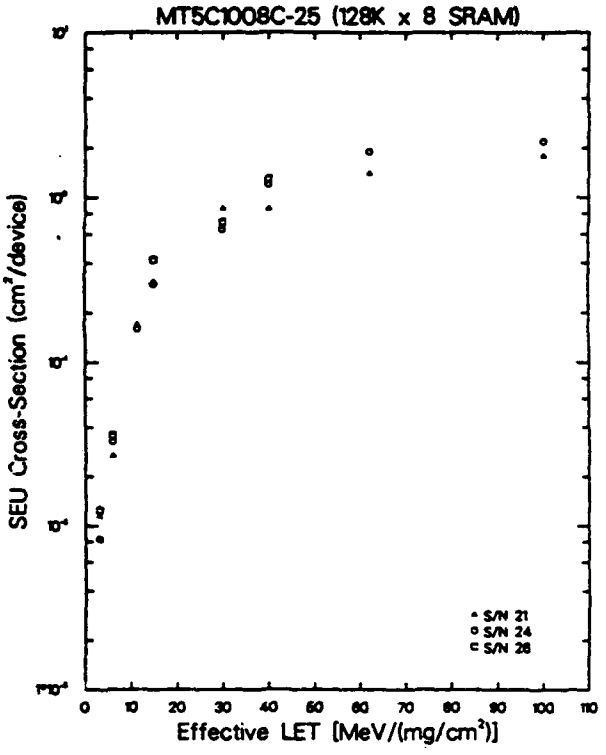

Figure 2. SEU Test Results for MT5C1008C-25

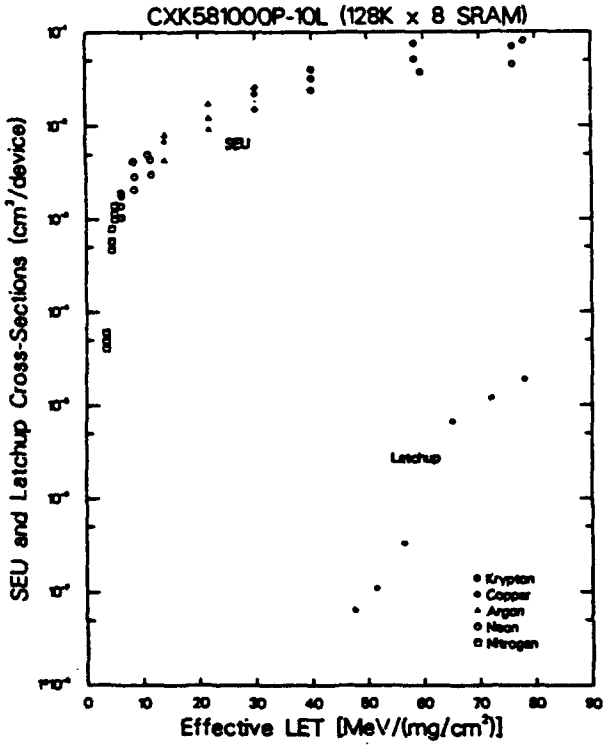

Figure 3. SEU and Latchup Results for CXK581000P

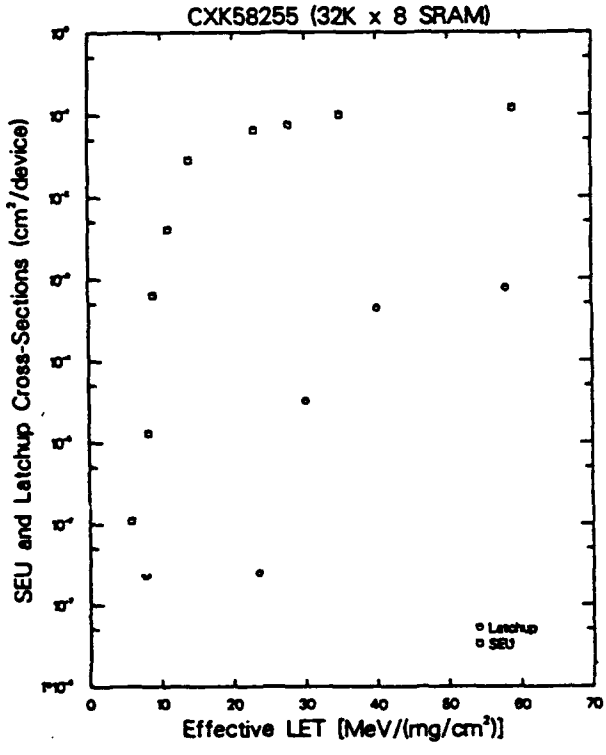

Figure 4. SEU and Latchup Results for CXK58255P

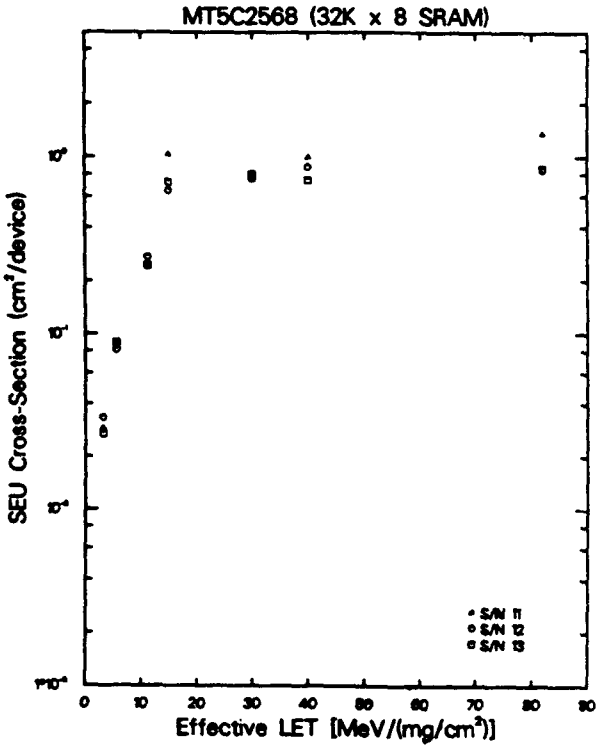

Figure 5. SEU Test Results for MT5C2568

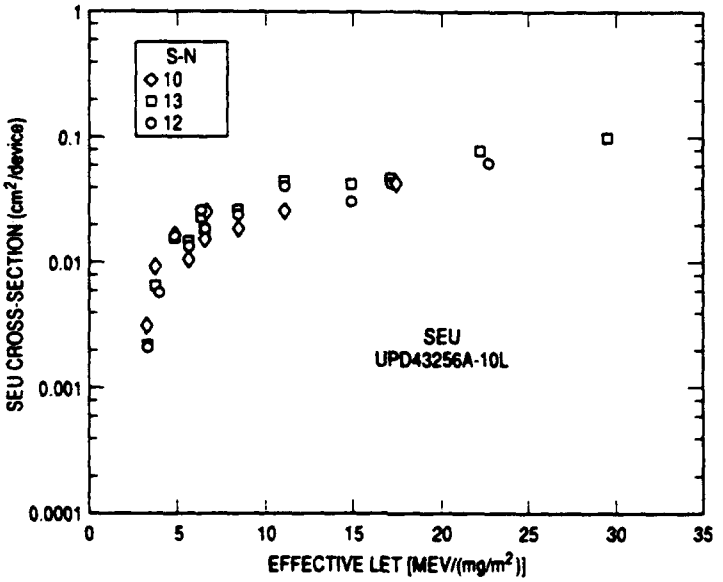

Figure 6. SEU Test Results for UPD43256A

In general, devices that are latchup prone should not be considered for space applications without additional circuitry to detect and correct this condition should it arise. However, if the threshold LET for latchup is large, the device may not undergo latchup on a short duration mission and may therefore be considered for particular applications. Approximately half of the device types listed in Table 1 might reasonably be considered for use in space, based on their susceptibility to latchup. Susceptibility to SEU must also be considered, particularly when error-detection-and-correction circuitry will not be employed. Finally, there are several additional factors that must be taken into account in evaluating the suitability of a particular device, as discussed in the following section.

III. ADDITIONAL CONSIDERATIONS

Some non-hardened high density SRAMs are relatively immune to latchup (see Table 1) and may therefore be suitable for space applications. However, several additional factors need to be taken into consideration before these devices can be recommended. In particular, a device's susceptibility to multiple-bit upsets and to radiation-induced permanent damage should also be assessed. In addition, the ability of an SRAM device type to reliably retain memory contents at reduced bias voltages may be relevant in some applications.

A. MULTIPLE-BIT UPSETS

The phenomenon of multiple-bit upsets caused by a single incident ion is well documented in the literature [2,4]. In the present study, the frequency and distribution of multiple-bit upsets for the MT5C1008C-25 and MSM8128SLMB 128K x 8 SRAM devices types were analyzed. The test devices were slowly irradiated with Kr, Cu, Ar, Ne, and N ions normal to the device surface, and the number of memory cells upset by each ion strike was assessed. Table 2 shows that percentages of multiple-bit upsets in comparison with single-bit upsets for the above device types. As can be seen, both the percentages and distributions of multiple-bit upsets differ substantially for these two device types. In particular,

(1) A higher percentage of the upsets for MT5C1008C-25 may be classed as multiple-bit upsets for LET values above 15 MeV/(mg/cm^2). (The total number of upset bits, counting multiple-bit upsets separately, was similar for the two device types.)

(2) No more than three bits were affected by a single ion for MSM8128SLMB, except when krypton was used, in which case a small percentage of four- and five-bit errors were detected. In contrast, upsets of five or more bits were common for MT5C1008C-25, particularly when krypton or copper was used as a source.

(3) Despite exhibiting multiple-bit upsets involving as many as 10 bits, in no case was more than one bit in a single MT5C1008C-25 memory byte upset. In contrast, for MSM8128SLMB, up to 37% of all multiple-bit errors affected two bits within a single memory byte (no larger multiple-bit errors were observed).

Typical cluster shapes (geometrical arrangements) of upset bits, caused by the impact of a single ion, are shown for MT5C1008C-25 in Figure 7. It is interesting to note that four upset bits tend to align as a string, rather than forming a square. Since the upsets are distributed to different bytes through proper device design (all bits in each byte are geometrically separated), the probability of a byte experiencing more than one error is reduced by several orders of magnitude in comparison with that for a single error per byte. Hence, incorporation of a single-bit error-detection-and-correction (EDAC) circuit can reduce the effective upset rate by several orders of magnitude. In contrast, for a device such as MSM8128SLMB in which multiple errors frequently occur within a single byte, the effective upset rate cannot be reduced by simple (single-bit) EDAC techniques.

Table 2. Multiple-Bit Upset Frequencies and Distributions

	# bits upset by single ion hit									
	1	2	3	4	5	6	7	8	9	10
MT5C1008C-25	(No two bits in same byte were upset)									
Kr	21%	16%	5%	5%	7%	14%	5%	16%	9%	2%
Cu	37%	11%	5%	7%	8%	20%	10%	2%		
Ar	24%	28%	29%	15%	1%	1%	1%			
Ne	90%	8%	1%	1%						
N	97%	3%								
MSM8128SLMB							Double-bit/byte errors			
Kr	49%	37%	6%	6%	2%		37%			
Cu	71%	26%	3%				19%			
Ar	78%	21%	1%				0%			
Ne	82%	18%					0%			
N	98%	2%					0%			

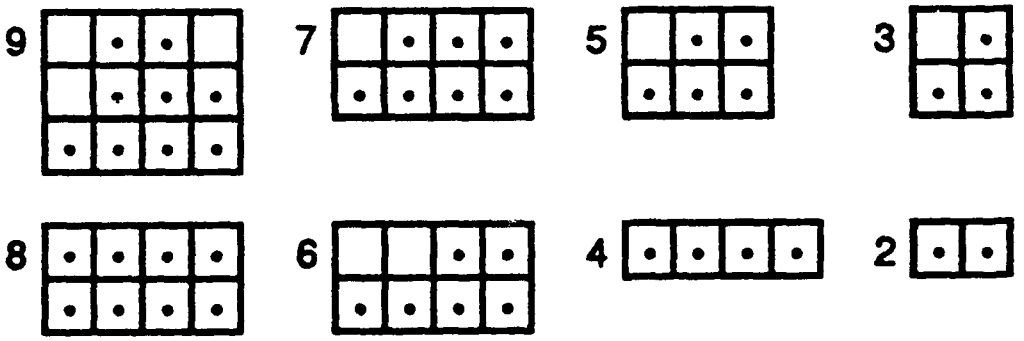

Figure 7. Typical Multiple-Bit Error Clusters (Each box represents a single location)

A second type of multiple-bit upset caused by cosmic rays occurs when an energetic ion passes parallel to the surface of the device, interacting with the two or more (possibly widely separated) memory cells. Thus, regardless of the device geometry, there remains a finite probability that any two bits in a die (in particular, two bits within a byte) may be upset simultaneously. It follows that even when a device appears immune to multiple-bit errors as described above, a single-bit EDAC may still be insufficient to ensure that all errors are corrected in the space environment.

A class of non-random upsets in high density CMOS/NMOS SRAMs has recently been reported [5]. For these upsets, it is suspected that a single upset at the control node of the word-line can cause bit errors at multiple address locations connected by the word-line. A "word-line upset" may be caused by a damaging write condition initiated by an ion in some situations. An examination of the patterns of errors for MT5C1008C-25 and MSM8128SLMB revealed no evidence suggestive of this putative upset mechanism.

B. PERMANENT DAMAGE

Some devices are susceptible to damage that is characterized by the presence of a semi-permanently stored pattern (these are sometimes called "stuck bits") in a byte. This effect was observed in both MT5C1008C-25 and MSM8128SLMB (among others) when irradiated with Cu, Kr, and Xe ions having LETs larger than 30 MeV/(mg/cm^2), but not when lower LET ions were used. Since this phenomenon is observed for device types utilizing Hitachi 128K x 8 dies (e.g., MSM8128SLMB) but not Hitachi 32K x 8 dies, the design change (shrinkage of the feature size) is presumed to be the cause of this effect. At present we do not know the critical feature size above which this effect disappears. Some "stuck bits" annealed within several minutes, whereas others did not anneal even after several months. The cross section for this phenomenon is usually several orders of magnitude below the SEU cross section; however, precise determination of the cross section is difficult due to the varying rate of annealing.

C. MEMORY RETENTION AT REDUCED BIAS

Most SRAMs retain their contents when the bias voltage is reduced as low as one or two volts. As soon as the bias voltage is returned to 5 volts, the correct information can be accessed. It follows that a large energy savings can be realized by reducing the bias voltage in those situations in which the memory is dormant for an extended period of time.

Unfortunately, the SEU vulnerability increases, in general, with decreasing bias voltage, for, while the charge collected at the sensitive nodes decreases as the voltage is lowered, the threshold charge required to overcome the present memory state decreases at a faster rate. Consequently, the upset cross section increases with decreasing bias voltage. This increased SEU vulnerability at decreased bias levels appears to be a very general phenomenon, experienced by many SRAM types.

For example, the SEU cross section for MT5C1008C-25 increased by a factor of about 2 (at all LET levels) as the bias voltage was reduced to 2.5 from 5 volts, as shown in Figure 8. This test was conducted by exposing the device to ion beams only during the time when the bias voltage remained at 2.5 volts. The SEU threshold LET measured at the reduced voltage does not differ greatly from that obtained for the same device operating at 5 volts.

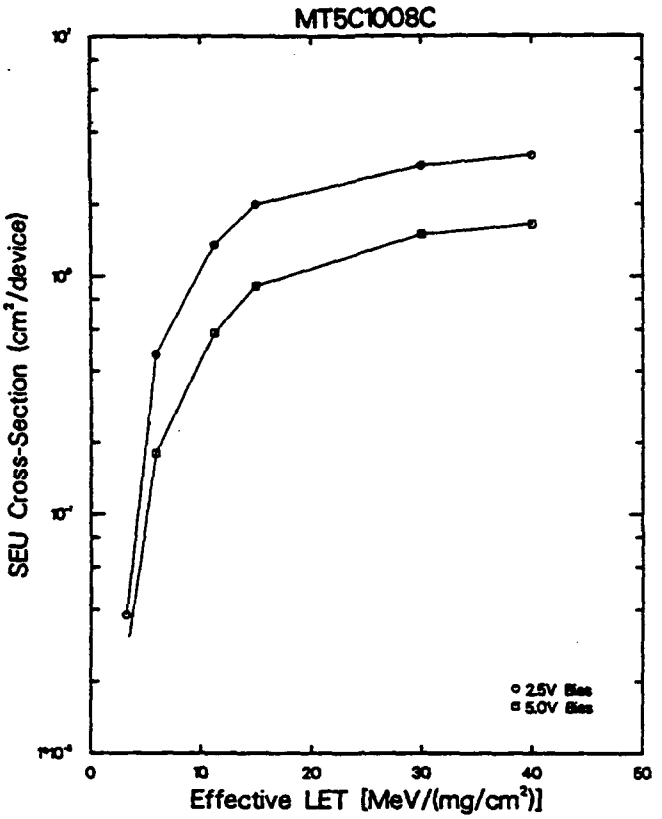

Figure 8. SEU Cross Section at 2.5 and 5.0 Volts Bias

IV. COMPARISON OF OBSERVED AND PREDICTED UPSET RATES

Non-radiation-hardened high density SRAMs utilizing Hitachi 32K x 8-bit dies were employed in the memory bank of a low-Earth orbiting satellite that was launched in the spring of 1990. The satellite has an essentially circular orbit at an altitude of 700 km and an inclination of 90°.

The 18 Hitachi die-based SRAMs used on this satellite are interrogated once each orbit (every 100 minutes) with a single-bit error detection and correction circuit. The accumulated (single- and double-bit) error counts are then periodically downlinked to the ground (to date, no double-bit errors have been observed).

Since the contents of the memory bank are replaced with a new set of data every six to eight hours, no imprint effect [6] is expected for these SRAMs. In other words, for an arbitrary bit, the probability of a "0" → "1" error is the same as the probability of a "1" → "0" error.

In this section, the in-flight SEU data will be briefly reviewed and compared with predictions derived from ground-based testing and modeling of the space-radiation environment.

A. UPSET RATE PREDICTION MODEL

Upset rates for devices utilizing the Hitachi 256K-bit dies were predicted prior to launch using the Cosmic Ray Effects on Microelectronics (CREME) program developed by the Naval Research Laboratory. Several candidate space environments can be modeled in CREME by specifying what is called an "interplanetary weather index." An index of 1 "gives the best approximation to the galactic cosmic ray flux on the given date," whereas as index of 3 models worst-case cosmic fluxes, which "are so severe that they have only a 10% chance of being exceeded by actual fluxes at any moment" [7].

The predicted upset rates for the Hitachi die (at 700 km altitude) were 2×10^{-6} upsets/bit-day for the index 3 environment and 4×10^{-7} upsets/bit-day for index 1. Since the observed (in-flight) upset rate was only 1×10^{-7} upsets/bit-day, it can be seen that interplanetary weather index 3 overestimates the true upset rate by about an order of magnitude, whereas index 1 overestimates by a factor of around 4. In the past several years upset rates for various microcircuits have been predicted using CREME with the rather conservative interplanetary weather index of 3. The above measurements indicate that for the Hitachi 256K-bit dies, 1 yields sufficiently conservative estimates of the upset rate at this altitude.

B. IMPACT OF SOLAR ACTIVITY

Figure 9 shows the daily average of single-event upsets plotted against the proton flux ($E_p > 10$ MeV), as monitored by GOES satellites in geosynchronous orbit. The proton peaks are caused mainly by heightened periods of solar activity and are often a good indicator of the existence of particle-rich solar flares, which emit their energy as particles (including heavy ions), as well as in the form of electromagnetic radiation. As is apparent from this figure, at this altitude the level of solar activity appears to have had no appreciable effect on the SEU rate. It thus appears that either: (1) only a small number of heavy ions were emitted by the sun during the time period covered by the figure; or (2) most of the heavy ions emitted by the sun were attenuated within the Earth's magnetosphere.

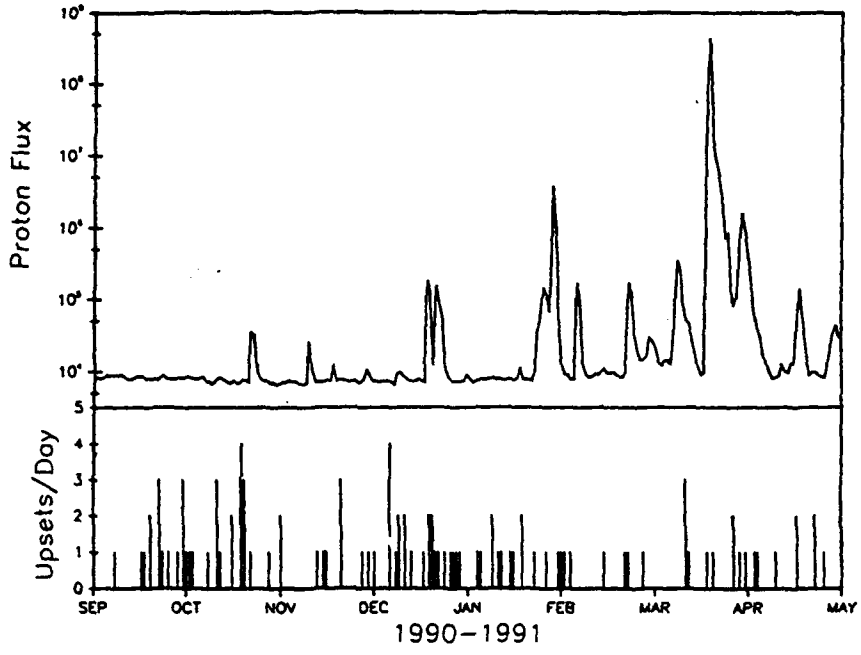

Figure 9. SEU Upset Rate vs Solar Proton Flux

C. TOTAL DOSE EFFECTS

The total dose limit of Hitachi dies is several krad(Si) under conditions of accelerated ground-based exposure to Co^{60} gamma rays. By May 1991, the cumulative dose experienced by the Hitachi dies in-flight had already approached this limit without significant detriment to performance. Apparently the slow dose rate in space, combined with continuous annealing, must have mitigated the damage due to total dose for this device type.

D. FUTURE ANALYSIS

By increasing the temporal resolution of our analysis to "upsets/orbit" rather than "upsets/day" and correlating observed upset rates with associated orbital trajectories, we should be able to identify memory errors as being either proton- or heavy ion-induced (with proton-induced upsets expected mainly in the region of the South Atlantic anomaly). This analysis is currently in progress.

V. CONCLUSION

Some non-radiation-hardened 256K-bit SRAM types appear to be suitable for use in low altitude space applications, provided that they do not latch-up. However, since the upset rate predicted by CREME (with index=3 at geosynchronous orbit) for a typical non-hardened device is several orders of magnitude greater than that predicted for a typical hardened device, it is crucial that the design of non-hardened devices minimizes susceptibility to multiple-bit upsets, and that error-detecting-and-correcting circuitry be employed.

A further disadvantage of non-hardened devices is their lower total dose tolerance. The total dose limit of many non-hardened SRAMs is about 10 krad(Si) when measured during ground-based testing, whereas radiation-hardened SRAMs can often tolerate doses up to the order of Mrad(Si). However, as noted above, accelerated ground-based exposure may lead to somewhat conservative total dose limits. In the space-radiation environment, non-hardened SRAMs may tolerate cumulative doses higher than 20 krad(Si), but the tolerance level will still not reach that attained by hardened devices.

A comparison of the upset rate in space for 256K-bit SRAMs utilized on a recent satellite with the rate predicted using NRL's CREME code shows reasonably close agreement (within an order of magnitude). No correlation was found between solar flare activity and the upset rate of these devices, suggesting that either there were no particle-rich solar flares during the period under observation, or that solar flare particles are attenuated within the Earth's magnetosphere. Future analysis of the upset data obtained from these devices should enable us to identify the cause of upset based on the orbital trajectory.

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