PROCESSING, FABRICATION, AND DEMONSTRATION OF HTS INTEGRATED MICROWAVE CIRCUITS

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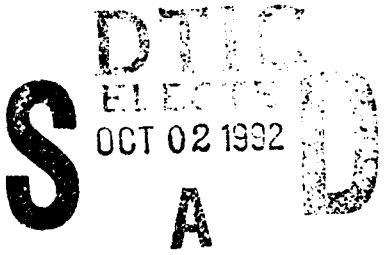

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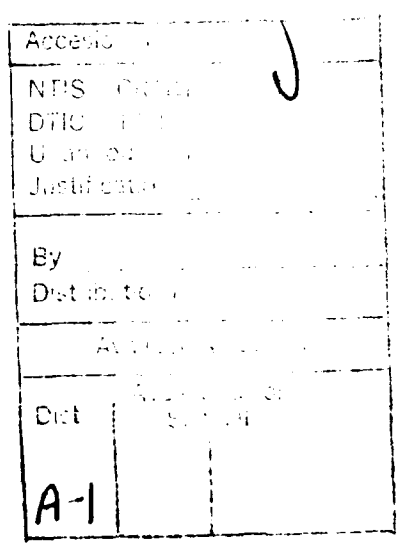

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DESCRIPTION OF PROGRESS

TASKS 1.0 and 2.1: COMPARATIVE TECHNOLOGY ASSESSMENT and INTEGRATED SUBSYSTEM SPECIFICATIONS

Because these tasks are strongly interrelated, their progress is combined here. A report describing the subsystem demonstration and its performance benefits has been prepared as a separate item and is included in Appendix A.

Volume comparisons were made between HTS microstrip transmission lines and other high Q electromagnetic structures and between HTS microstrip and high-performance multimode coupled dielectric resonator filterbanks. The results of these comparisons are shown in Tables 1 and 2. From Table 2 it is seen that the volume advantage for HTS microstrip filters increases as the number of channels increases. To this estimate must be added the qualifier that the bulkier dielectric resonator filters are usually multiplexed in numbers no greater than 12 or so in architectures that use one filter per channel. When multiplexed in the architecture used in this program (two filters per channel) the number of filters doubles and the HTS volume advantage is even more dramatic.

An assessment was made of the potential performance of HTS filterbanks for EW systems as compared with measured results to date using magnetostatic-wave (MSW) filterbanks. Assuming pulsed input signals centered at next-to-adjacent channels, we compared their rejection and the time-lapse required to attain this rejection. MSW filterbanks achieve a 55 dB rejection after about 400 nS. As reported below, a seven-pole HTS filter designed in this program has a theoretical 65 dB rejection after 110 nS. Although this is a sufficient performance goal to demonstrate the advantages of HTS vs MSW technology, by increasing the number of poles it is possible to obtain 80 or 90 dB

Table 1

Volume vs Q_u at 10 GHz

Resonator	Volume (cm^3)	Q_u ($x10^3$)
Cylindrical TE_{011} Empty	50	80
Cylindrical TE_{111} Diel. Fill.	10	10
Rectangular TE_{101} Empty	10	10
Coaxial TEM	10	10
Microstrip Gold	0.05	0.2
Microstrip HTS	0.05	10

Table 2

Low-Loss Filterbank Technology Comparison

40 Channels
Six - Pole Filters
1.3% Bandwidth
Loss < 1 dB

	C-Band 3 - 5 GHz BW ≃ 50 MHz		X-Band 6 - 10 GHz BW ≃ 100 MHz	
	Volume (cm^3)	Ch. Dens. (cm^{-3})	Volume (cm^3)	Ch. Dens. (cm^{-3})
HTS Microstrip (Without cooling)	250	0.16	60	0.67
Multi - Mode Coupled Dielectric Resonators	1600	0.03	1000	0.04
Ratio		6		17

rejection at shorter times with HTS. Such high dynamic range is made possible only by the low loss of HTS filterbanks. The dynamic range attainable from a system point of view will be studied later in this program. The implementation of a suitable high-performance filter will be explored when studying other topologies such as those using lumped elements.

The contribution of cryogenically cooled filters to a receiver system noise figure was analyzed. As opposed to operation at room temperature, where the filter noise figure is equal to its insertion loss, the noise figure of a cooled passive device is directly dependent on its loss and the ratio of its ambient temperature to room temperature. Thus, HTS filters will have a very low noise figure not only because of their low loss but also due to cooling to 77K. This makes front-end channelization very attractive, as well as the use of HTS filters for frequency preselection before a low-noise amplifier.

TASK 2.2: FUNCTIONAL COMPONENT AND SUBSYSTEM DESIGN, FABRICATION, AND TESTING

A study was conducted of various filter topologies and their potential advantages and disadvantages in meeting the goals of this program. The approach chosen is a parallel-coupled line topology with input/output tap coupling into first and last resonators. Important criteria in the choice of the structure was the substrate surface area, the frequency of the second-harmonic spurious response and the ease of implementation.

Based upon system and application considerations specified after joint discussions between WEC EW and ONR, DARPA and Air Force personnel, filters with approximate $\cos^3$ passband characteristics will be fabricated for this program. This shape will ensure that acceptable time domain responses for pulsed input signals will be achieved. Several design iterations have been performed with the goal to attain reasonable frequency selectivity and time-domain impulse response with a minimum number of poles. The result is a 7-pole filter design which approximates a $\cos^3$ function down to about 10 dB, as shown in Figure 1.

The architecture for the multiplexer originally proposed, which uses two 90° hybrids and two identical filters per channel, has been reviewed and compared with other topologies. As a result, it was confirmed as the best choice due to its flexibility and the indefinite number of channels it can support. An additional advantage is that signals outside the passband may be routed elsewhere for alternative processing without significant insertion loss.

The interaction among channels for the multiplexer architecture has been studied. The bandwidth coverage required by the application (3 dB passband crossovers) and the smooth roll-off of the approximated $\cos^3$ passbands results in a significant overlap among them. The low loss nature of the multiplexer, however, produces significant interaction among filters, distorting amplitude and phase in all filters except that nearest the input. Figure 2 shows this interaction for an unoptimized 6-pole filter response. The severe distortion of the passbands may be alleviated by separating even and odd numbered channels into the two branches of a power splitter. The 7-pole filter design mentioned above was optimized considering this even/odd power splitting. Figure 3 shows four filter passbands on one branch of the power splitter, with substantially diminished distortion. Figure 4 is a sample calculation of the time domain response of one of the filters for a 200-nS-wide pulse. A rejection of 65 dB at the center of a next-to-adjacent filter is obtained after about 110 nS, assuming zero rise/fall times.

The design for a 50 nS delay line (2-to-6 GHz operation) has been completed. The chosen configuration is a doubly-wound stripline spiral, with a pitch chosen so that cross-coupling between the delay line sections is less than -40 dB. Given the present limitation of two inches as the maximum diameter available for our double sided YBCO films, initial devices will require equal sections, each 2 inches in diameter producing 25 nS of delay. As the materials effort progresses under Task 3 and larger diameter films become available, longer delays will be achieved with single substrates.

The device reproducibility goals of the program will require systematic measurements of the substrate dielectric constant uniformity between wafers and within a

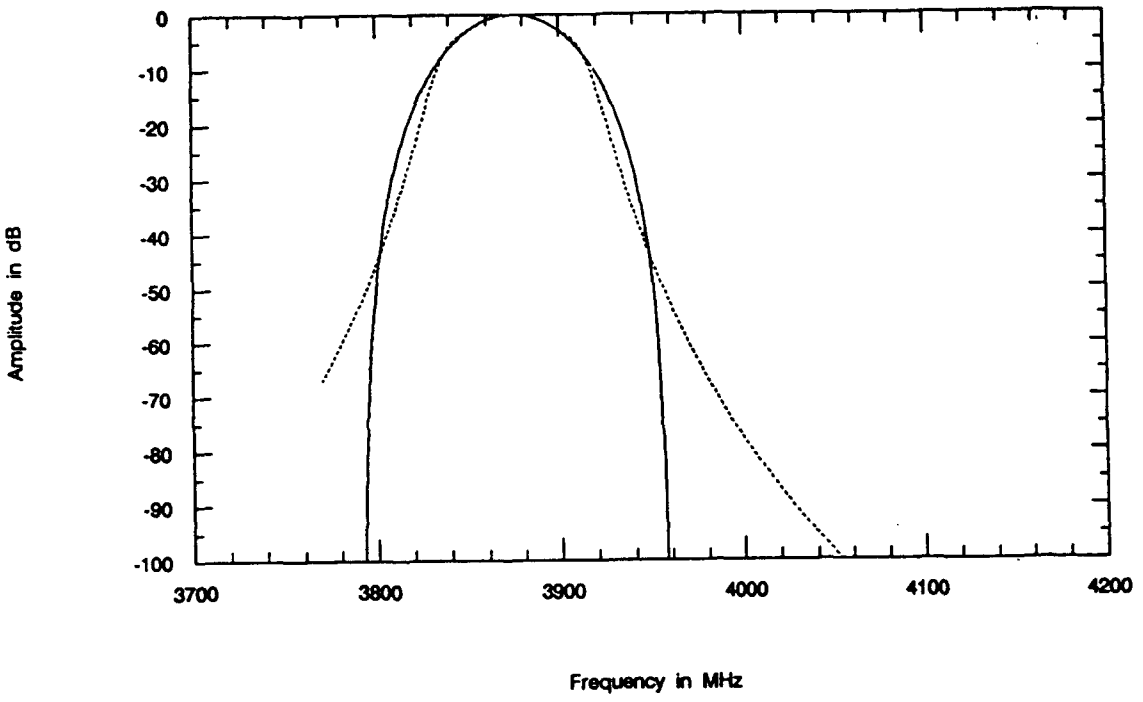


Figure 1. Seven-pole filter amplitude response as compared to a $\cos^3$ function.

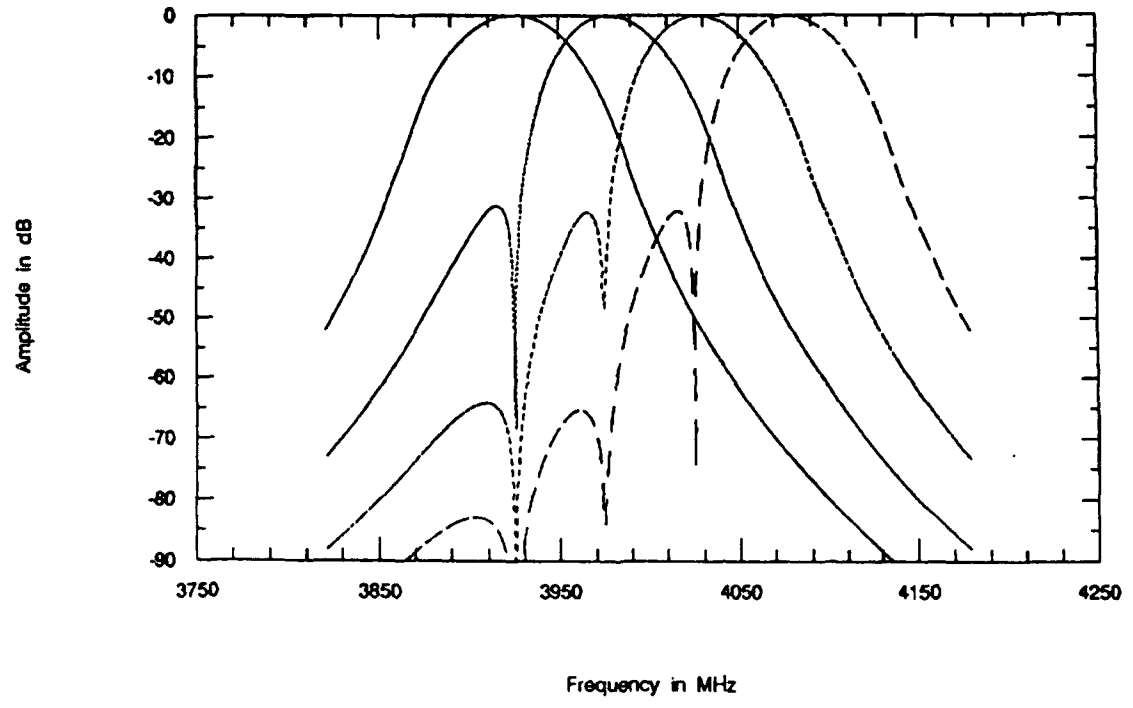


Figure 2. Distortion caused by multiplexing of 6-pole non-optimized filter responses.

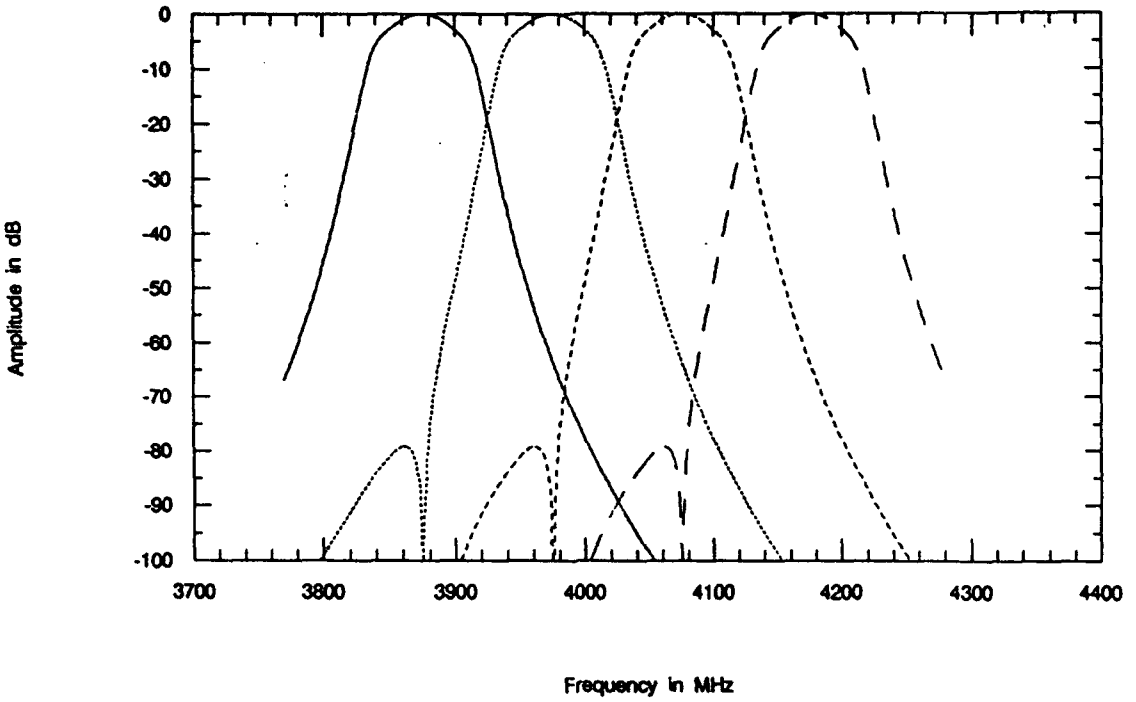


Figure 3. Optimized 7-pole filter responses on one branch of a power splitter (i.e. filters shown are 100 MHz apart in the full filterbank). Compare the greatly reduced distortion with that in Figure 2.

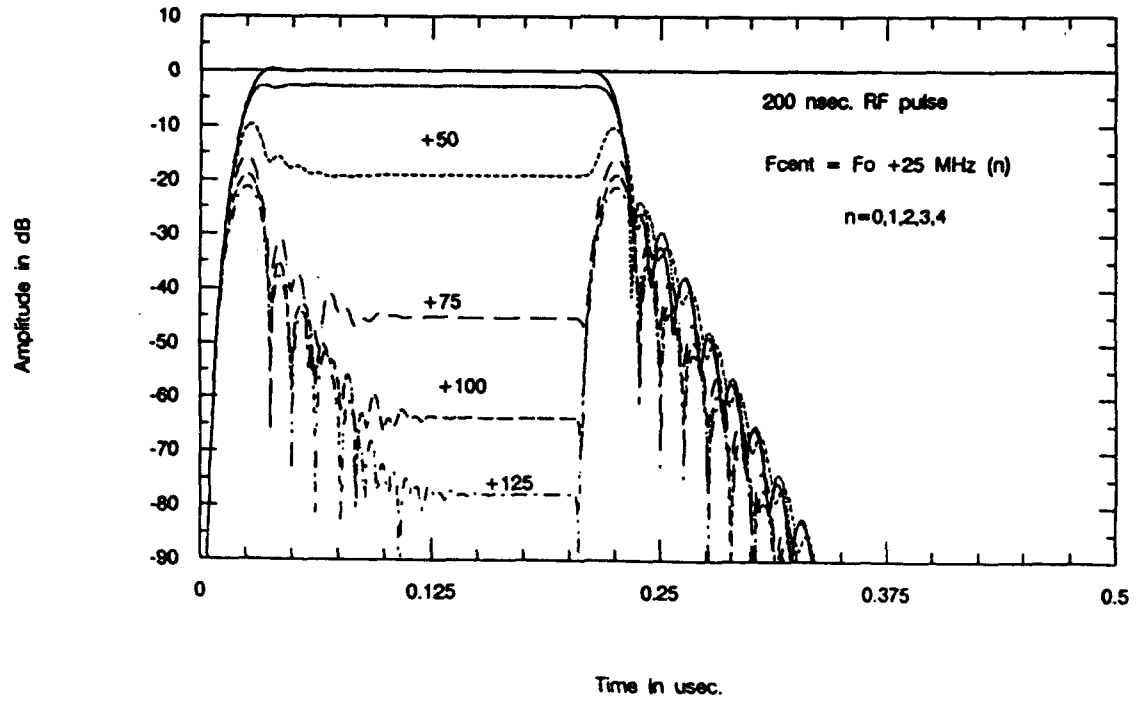


Figure 4. Calculated time-domain response for one of the filters to a 200-nS-wide pulse.

wafer. A preliminary approach to this problem, currently being studied, is the use of gold microstrip resonators on $LaAlO_3$ substrates. The objective is to avoid the use of YBCO films for this measurement, since poor quality films could show sufficient kinetic inductance as to shift the frequency response of a resonator, thus masking any dielectric nonuniformity effects. An experimental sensitivity of $\Delta\epsilon_r = 0.5\%$ is being assumed. This is based on computer modelling of filter designs with similar characteristics as those in this program. A filter performance sensitivity analysis will be carried out when a geometrical design is finalized.

The microwave package which will house the thin film HTS devices being made on this program must provide the requisite electrical and mechanical integrity to take advantage of their expected performance levels. This can be assured only if the substrates are held in intimate contact with the package. On previous programs, such as HTSSE-I, single devices were mounted in brass packages and to prevent device failure due to thermal contraction stresses, we used a complex mounting scheme involving gasketing with low-melting point ductile solders. This scheme enabled production of devices which passed the multiple cooldown and vibration tests for space qualification for that program. Our follow-on HTSSE-II program and this concurrent DARPA program call for a larger degree of device integration, with larger area substrates and correspondingly larger packages. The edge gasketing technique would not provide sufficient support for these larger, more fragile substrates.

A better structural material for the microwave packages was needed; one which would match the thermal expansion characteristics of the substrate and allow the larger devices to be mounted directly to the package by soldering. We had previously considered a material used at the Westinghouse ESG division for thermal expansion matching--an aluminum filled silicon carbide matrix which can be tailored over a limited range to match thermal expansion characteristics by varying the aluminum fill percentage. However, this material is difficult to machine, expensive, and requires new molds to be fabricated for even minor package modifications. A search of low temperature thermal

expansion data suggested that the Group VB elements, vanadium, tantalum, and niobium might serve. They all have total thermal contraction amounts which were very close to that estimated for lanthanum aluminate, for which accurate low temperature thermal expansion data is only now becoming available.

A two-inch diameter, 10 mil thick $LaAlO_3$ wafer, Au plated on one side, was soldered to a niobium disk and thermally cycled repeatedly to 77K without wafer fracture or failure of the solder bond. Niobium is rather easily machineable, is easily Au plated, has a high thermal conductivity, has relatively low electrical resistivity, and is not particularly expensive. Accordingly, it will be used for the package structural material, or as a chip carrier in packages of other (brass or stainless steel) materials. Adaptation of standard microwave packaging techniques, such as laser-weld lid sealing, for use with niobium has been started. Machining of the first package components from niobium has begun.

Prototype filter channels and delay lines will be fabricated on the currently available two-inch diameter wafers with YBCO on both sides. Layouts have been made for single channel filters comprising two parallel coupled line filters and two couplers on a two-inch diameter wafer. The resulting substrate size of 1.102 x 1.860 $in.^2$ fits onto the two-inch wafer with slight corner clipping and maximizes the available space for the active elements. All filter/coupler channels will be produced on this size substrate until larger area films are available later in the program. Similarly, the wafer layout for the stripline delay line has been fixed. Dimensioned package drawings of both were produced and were reviewed by ESG and STC personnel. An internal design review was held on July 22, 1992 at ESG and fabrication has begun.

The influence of package side-wall and lid proximity to the filter resonator elements is being analytically examined. Tests of individual filter and coupler elements are being planned to determine whether there is sufficient sensitivity to influence the internal package dimensions. The superconductive properties of the niobium package below 9K may provide a convenient method to experimentally verify the analytical results.

Past experience in the design, production, and sealing of semiconductor packages is being called upon to determine the optimum techniques for sealing the niobium package and for meeting the vibration requirements. The use of large substrates necessitates a careful analysis of loading and deformation properties of the solder/metal-contact components which hold the substrate in place. As part of the companion HTSSE-II program, which requires space qualified vibration-proof devices, calculations of g-force load factors are underway for the present package design. Design modifications will be made if the loadings or deformations are excessive and they will be incorporated into the DARPA package to allow commonality of components, providing they are not detrimental to the performance of the DARPA design.

TASK 3.1: PVD MULTILAYER FILM FABRICATION

The integration of YBCO films with a ground plane on a single wafer by off-axis sputtering proceeded as scheduled during these reporting periods. Two approaches were pursued for fabricating trilayer YBCO/insulator/YBCO structures. The first approach was to deposit YBCO on both sides of $LaAlO_3$ wafers up to two-inches in diameter. This capability was first demonstrated at Westinghouse prior to the start of the program using a substrate holder which heated the wafer to approximately 720° C solely by radiation, i.e., without directly bonding the wafer to a heated block. For this approach, the emphasis on this program has been on improving the uniformity and reproducibility of the YBCO films. The second approach for depositing trilayer structures was to use sputter-deposited epitaxial insulators. The six insulating materials studied were MgO, $LaAlO_3$, $SrTiO_3$, CeO_2, $NdGaO_3$ and $SrAlTa_2O_6$.

The most significant improvements of YBCO films deposited on both sides of wafers stemmed from modifications and additions to our deposition facilities. Film thickness uniformity was improved by adding substrate rotation about the wafer's axis. Radiation shields were added to the deposition chamber to improve substrate temperature uniformity. In the new configuration, the sputter guns and substrate heater were

essentially enclosed in an oven. The advantage of the radiation shielding was not just an improvement in temperature uniformity across the substrate but reduced sensitivity to the changing emissivity of the $LaAlO_3$ wafer as it was coated by YBCO.

At no cost to this program, a second sputtering system was assembled for deposition of films on both sides of two-inch wafers. The second chamber has been supplying coated wafers to Task 2.2 on a routine basis. The original sputtering system will be used for additional development work, particularly with deposited epitaxial insulators. Another vacuum system, large enough to coat both sides of 4-inch diameter wafers, has been ordered and will be installed in September. When the films grown in the 4-inch-wafer chamber attain the properties of those made in the 2-inch chambers, it will be used to supply films to Task 2.2. It was designed to be a completely automated prototype of a system that could be used by the Westinghouse Electronic Systems Group in Baltimore.

For the deposited-insulator approach, new insulating compounds were evaluated. At present, only $SrTiO_3$ has been shown to reproducibly form smooth, pinhole-free overlayers on YBCO. It is an excellent candidate for forming air-bridge crossovers since differential wet chemical etches are available to remove it without damaging YBCO. However, the poor dielectric properties of $SrTiO_3$ make it impractical for other applications such as in lumped-element resonators. Of the other materials which have been evaluated, only Sr-Al-Ta-O (SAT) has shown smooth film surfaces and insulating properties comparable to those of $SrTiO_3$ films. In contrast to $SrTiO_3$, bulk SAT has a relatively low dielectric constant ($\epsilon = 12$) and low loss tangent (4×10^{-5}). Alternatives to $SrTiO_3$ or SAT will be developed if the preliminary results on SAT films are too difficult to reproduce.

Although they do not appear to have a deleterious effect on the rf surface resistance of YBCO at 77K, Cu-O precipitates (boulders) on the surface of YBCO films were found to be a significant cause of pinholes in deposited insulators. The nucleation of Cu-O particles could be prevented by keeping the sputtering plasma away from potentially contaminating surfaces inside the vacuum chamber. However, a reappearance of these

precipitates had to be addressed each time one of the chambers was modified, showing that an additional understanding of the plasma dynamics is still needed. At present, precipitate-free films are being produced reliably in two of our four chambers, while a third, which was producing boulder-free films, has ceased doing so upon the installation of a new target.

For the first time, we studied in detail the in-situ post-annealing conditions on YBCO film properties. The oxygen pressure in the chamber during this step had an optimum value of approximately 20 torr. The use of higher pressures reduced T_c's from ~91 K to ~87 K. This surprising result is clearly relevant only for in-situ film growth and does not apply to bulk YBCO material formed under equilibrium conditions. For YBCO devices operated at 77 K, T_c's as close to those of bulk samples as possible are required.

TASK 3.2: MOCVD MULTILAYER FILM FABRICATION

This task has been delayed due to funding delays and internal reorganization problems at EMCORE, the subcontractor to develop the plasma-enhanced MOCVD process. Progress has amounted to defining the technical milestones, schedule, and work statement for the subcontractors EMCORE and Northwestern U. after reviewing the work that has been accomplished to advance the art since the program was initially proposed. EMCORE and Northwestern are now under contract and work is beginning on the development of CVD multilayer film fabrication approximately ten months after the contract start date. However, the delayed start of the three subtasks scheduled for performance during the first year of the program, alternate precursor development, deposition of YBCO films at Emcore, and growth of YBCO/deposited insulator/YBCO trilayers, will not affect the overall objective of Task 3.2 to have MOCVD-grown films available for device fabrication in the last six months of the program.

TASK 3.3: RF CHARACTERIZATION OF FILM PROPERTIES

The approach for evaluating YBCO films will be two-fold. Parallel-plate resonator measurements (technique due to Taber, Hewlett-Packard Labs) are made on small samples and a full-wafer, non-destructive measurement is done by replacing one end wall of a copper cavity. Calculations of TE_{011} mode fields for a cavity 5 cm in diameter and 1 cm high show good sensitivity at 17 GHz. This cavity is presently being fabricated.

CHANGE IN KEY PERSONNEL

Three changes in key personnel have been required since the program was originally proposed. Mr. T. E. Steigerwald has been named Deputy Program Manager at ESG, replacing Mr. D. C. Buck, who remains on the program in a technical role. Dr. G. S. Tompa has been named to lead the effort at EMCORE. He replaces Dr. P. Norris who is no longer at EMCORE. Dr. J. Talvacchio has acquired the duties of Mr. R. Betsch as coordinator of the MOCVD effort. Mr. Betsch is no longer employed by Westinghouse.

PROBLEMS ENCOUNTERED AND/OR ANTICIPATED

Although the start date of this program was July 24, 1991 with the approval of anticipatory spending, the contract was not signed until September 30, 1991 when the first increment of funding was received. Our current allocation is sufficient for the first year of effort, but is designated to cover the work through October 31, 1992. This places the program three months behind schedule and may necessitate a request for a no-cost extension.

FISCAL STATUS

Amount currently provided	$1,600,000
Expenditures and commitments through 7/26/92:	1,237,185 *
Funds required to complete:	3,769,203
FY93 funds required:	1,827,386

*According to the unaudited statement of cost.

APPENDIX A

HTS Sytem Insertion Demonstration Plan

A Report Submitted IAW Paragraphs 4.1 and 4.2.1 Of The SOW for the DARPA/ONR HTS Channelizer Program Contract Number N00014-91-C-0112

25 August 1992

Westinghouse Electric Corporation
Science and Technology Center
and
Electronic Systems Group

Introduction

This report is submitted in accordance with paragraphs 4.1 and 4.2.1 of the SOW for the DARPA/ONR HTS Channelizer Program.

We have defined a system insertion demonstration plan which demonstrates a significant system performance benefit as a result of high temperature superconducting component insertion. The channelized filterbank and delay line, currently under development, and a flow-through filterbank, a variant of the channelized filterbank, provide the basis for the insertion. The demonstration system would show the architecture and critical components required for a near term system insertion. The architecture defined is also the basis for development of new systems, versus existing system insertions, specifically designed with HTS components in mind. This report is divided into three sections. The first describes the benefits offered by the superconductive components. The second section describes the evolution of the system insertion architecture. Lastly, the demonstration program itself is described.

HTS Benefits

The two key features offered by passive superconductive components, not available with conventional technology, are very wideband, non-dispersive operation and very low insertion loss. At first glance, it seems obvious that these properties would make super conductive components viable replacements for many devices and components throughout the receiver chain. Indeed HTS components could be inserted anywhere in the system with some overall system benefit. There are cogent arguments, however, that the most profitable location for initial HTS insertion is at the front end of the receiver system architecture.

The first key feature of HTS passive RF components is their wide non-dispensive operational bandwidth. Because EW systems traditionally convert all frequencies to a low IF frequency for analog processing and signal detection, any wideband application in such a system must by definition be inserted toward the front end of the system. Some more recent systems with wider bandwidth receiver assets have IF frequencies in the 2-10 GHz range. These systems do provide the opportunity for insertion of a wideband HTS delay at the system IF. Operation in these IF bands can otherwise only be achieved via large and lossy lengths of transmission line. Maximum benefit of a delay line, however, is achieved when system hardware can be eliminated by RF signal storage through the delay line. Inserting the delay line at RF can eliminate the need for parallel amplification, filtering, and conversion prior to switching in a cued system configuration.

The second key feature, low insertion loss, contributes to the system in three ways: improved sensitivity, higher dynamic range and overall reduction in system size and cost. Low loss components greatly reduce or even eliminate the need for many high cost amplifiers

throughout the system architecture. This elimination of amplifiers translates to reducing system size, weight and cost while increasing system reliability. To achieve these gains with the insertion of HTS technology, however, requires sufficient amplifier hardware reductions to more than compensate for the insertion of the cryoelectronic cooler. A large scale system insertion of many HTS components makes these gains feasible. Incorporation of a single filterbank or delay line, however is unlikely to provide sufficient benefits to warrant the cost required for the insertion.

The system noise figures and hence the system sensitivity is largely established by the initial amplification stage (including devices preceding the amplifier) of a receiver. Insertion loss of components further back in the system can generally be offset by additional amplification. Significant improvements to system sensitivity can only be achieved by insertion of the low loss/noise figure components at the front end of the system. Component losses contribute directly to EW system sensitivity in the system noise figure computation. The total noise figure of the cascade of N system elements is computed via the formula:

$$f_T = f_1 + \sum_{n=2}^{N} \frac{f_n - 1}{g_{in}}$$

where g_{in} represents the total gain preceding the n^{th} stage. For passive components (at room temperature) the noise figure is equivalent to the component loss. Figure 1 depicts a graphical interpretation of the noise figure equation, showing on the y-axis the added noise figure contribution of succeeding stages to the overall system noise figure, based on the first stage noise figure-gain product ($G_1 + F_1$ dB). As can be seen from the figure, insertion of low loss components anywhere but in the front end of a conventional system has no appreciable effect on system noise figure and hence sensitivity. The dashed line sample on the plot assumes insertion immediately behind a 10 dB gain, 4 dB noise figure low noise amplifier front end. Insertion of HTS low loss components after front end amplification and downconversion in a conventional EW system architecture will move the effective first gain stage to the far right of the x axis of Figure 1, eliminating any impact of the low loss component insertion.

Dynamic range is also minimally impacted by insertion of HTS components at the back end of the receive chain. The single tone dynamic range can be interpreted as the range from the detection sensitivity to the point where the detected signal is compressed by 1 dB. Extending the low end by increasing sensitivity requires HTS insertion at the front end, as described above. Increasing the high end requires limiting the system gain to avoid saturation throughout the receive chain. This can best be done by insertion of low loss components throughout the system.

Two tone dynamic range (2TDR) is defined by the maximum input power for two equal amplitude signals producing <0.0001% spurious reports, (= 2/3 [(IP3 - G) - Sens] in dB). Improvements in 2TDR can also be achieved through the overall reduction in system gain. HTS components can also provide higher third order intercepts (IP3) than conventional configurations in which amplifiers must precede lossy components such as filters or delay lines. Two signal detection capability in a channelizer will be affected by both the filter design of the channelizer and the total dynamic range of the system. The HTS channelizer under development will provide two signal detection capability of approximately 65 dB, a 10dB or more improvement over todays channelizers. Packaging of the entire channelized receive path in a cryoelectronic environment may provide even greater two signal detection performance, due to the elimination of coupled noise. If this channelizer is inserted in an existing system, however, the total dynamic range of the system may not be sufficient to realize this improvement.

In summary, the key features of HTS passive components, low loss and wide band operation, are best utilized in systems applications when applied throughout, but especially at the front end of the system. Benefits of reduced size, weight, cost and increased reliability can also be achieved with equivalent or better performance than conventional technology.

System Insertion Development

The main objective of this task was to develop a demonstration program that would highlight the capabilities of the HTS filterbank and delay lines being developed under this contract and provide visibility into the benefits of HTS components insertion in existing EW systems. A secondary objective was to provide a logical development/demonstration plan that would lead to a complete system demonstration of an HTS based system. As described above, improvements in size, weight, cost, and reliability can be projected with the advent of HTS systems. None of these features, however are likely to show improvements in a first demonstration of HTS components. This is not uncommon with first iterations of new technologies. As a general rule, revolutionary technologies will provide performance enhancements and the other improvements come as the result of later developments in packaging and system design. Our study concluded, therefore, that the demonstration of the HTS system component insertion should concentrate on significant performance improvements and still provide the building blocks for a system that could be, in its final form, directly inserted into an existing system. Demonstration of characteristics of the technology, as opposed to system benefits, with a promise for size, etc. improvements in the future was not deemed to be adequate. Because of the developmental status of the technology and the introduction of cryo-cooling, we

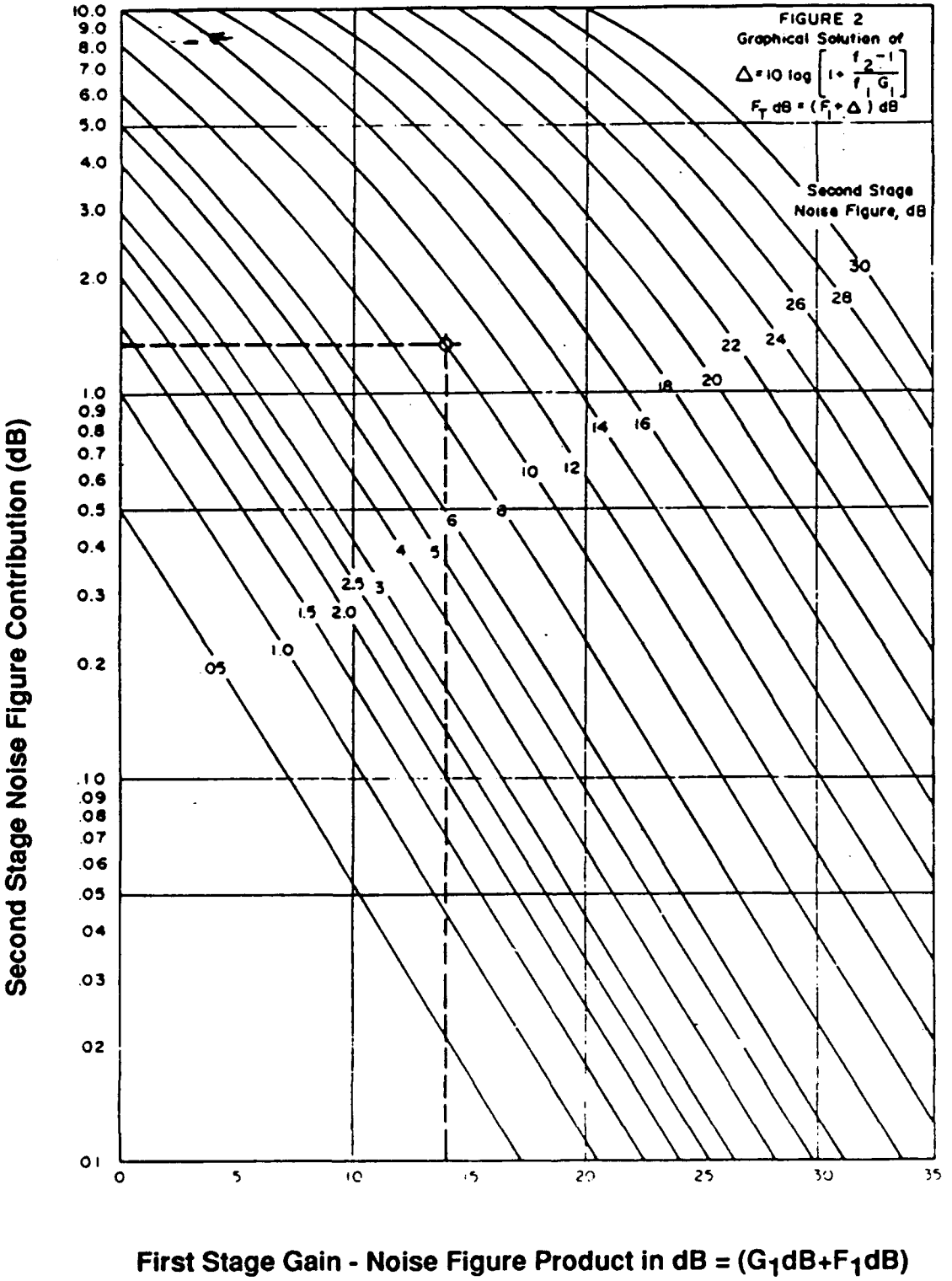


Figure 1 Noise Figure Contribution of Cascaded Elements

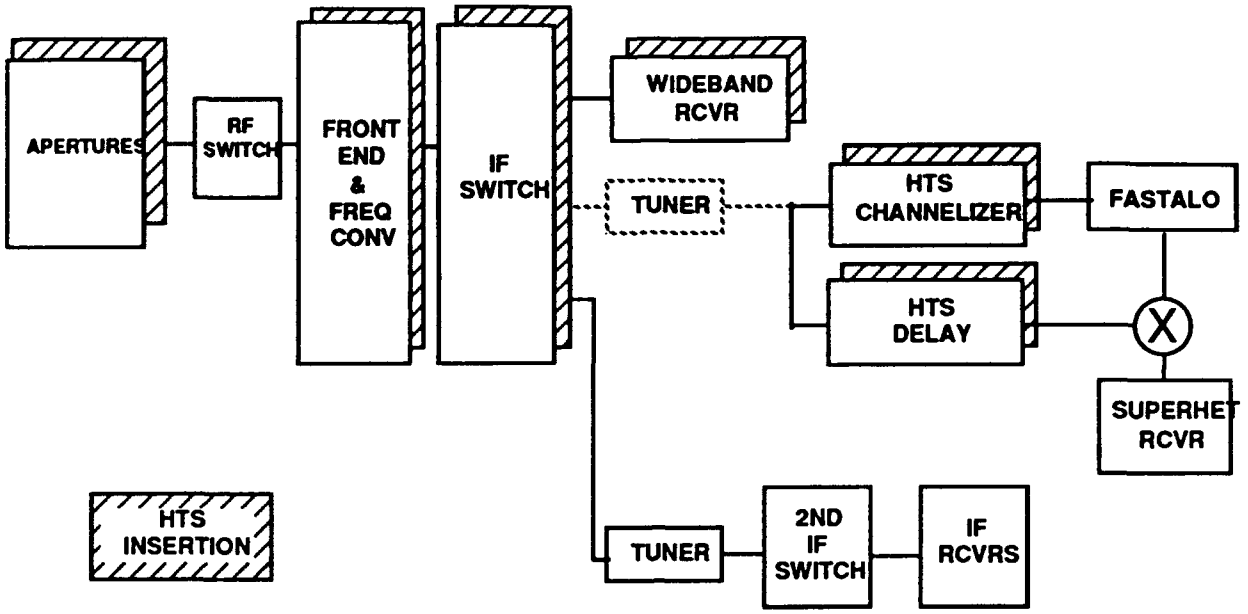


Figure 2 HTS Applications: Some Initial Thoughts

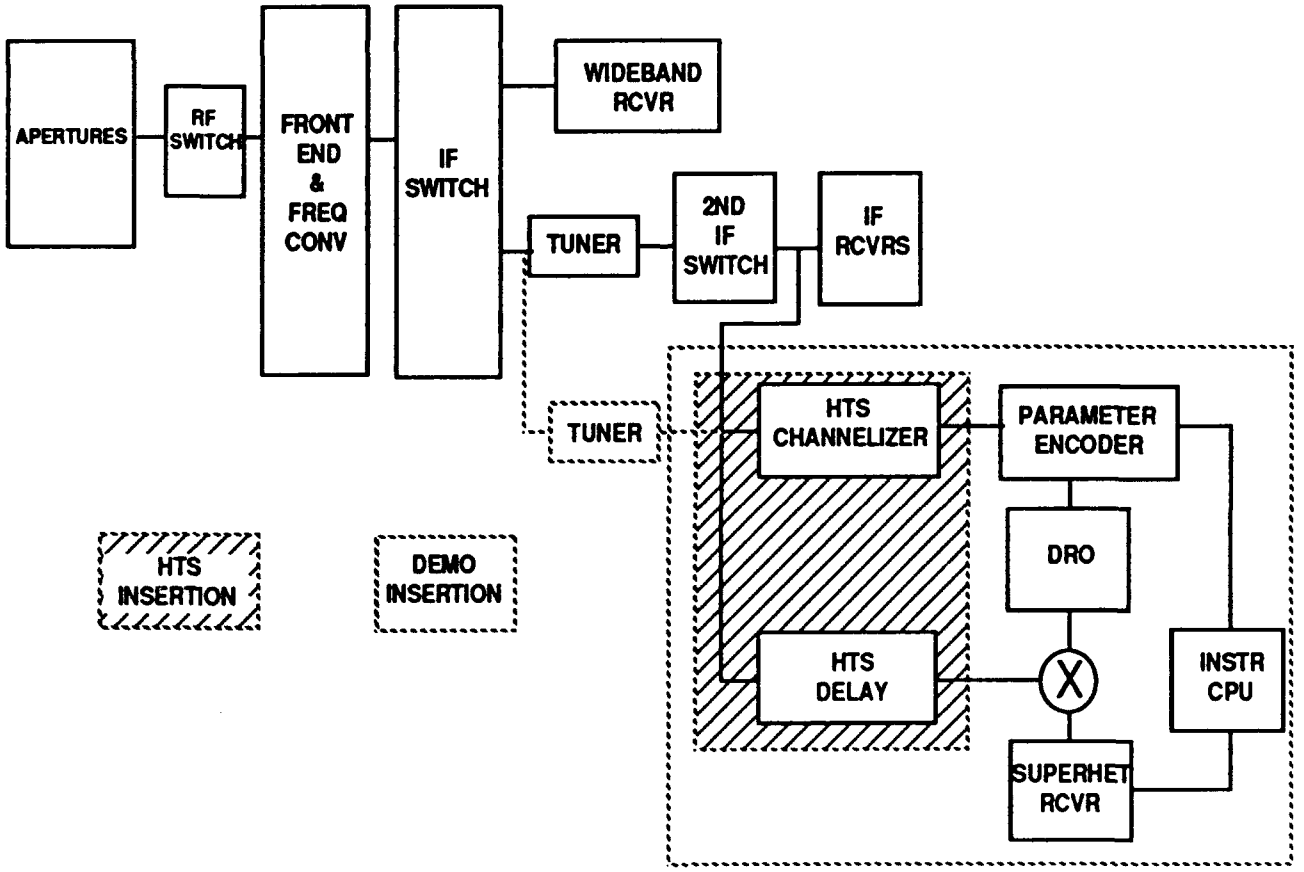
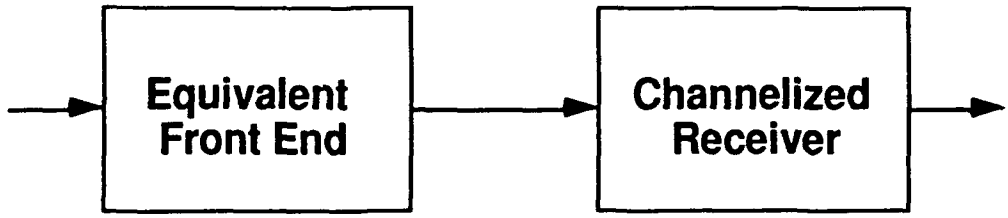


Figure 3 Channelizer Cued Superhet Application



		Conv	HTS
Gain	17.3	-1	-1
NF	15.6	25	1
IP3	23.3	15	20
Sensitivity		-70.6	-71.1
2TDR		45.7	48.5

Figure 4 HTS Channelizer at IF Minimally Improves System Performance

also concluded that the most likely initial insertion was for an ELINT application. The integration environment allows for less sophisticated packaging and, in some cases, even provides stations for testing experimental hardware. The demonstration system should, however, still show promise for insertion to tactical or other environments in the future.

The very preliminary thoughts on an insertion demonstration did not have this philosophy in mind. Initial thoughts developed a generic EW block diagram and identified numerous candidate insertion opportunities as shown in Figure 2. The elements under development on the existing program, however, included a channelizer filterbank and delay line. The most obvious application of these devices is to a channelizer cued superhet receiver configuration as shown in Figure 3. This insertion provides the same functionality as a conventional technology system, but utilizes HTS technology. Unfortunately the performance of this system offered very minimal improvement over a conventional implementation.

Figure 4 depicts the typical sensitivity and two-tone dynamic range (2TDR) enhancements achieved with the insertion of the HTS channelizer at the back end of a conventional system. The equivalent front end is the composite of the preamplifiers, filters, switching and downconversion. The associated gain, noise figure and IP3 would vary with the specific system design but the numbers shown are nominal for a state-of-the-art EW system. It

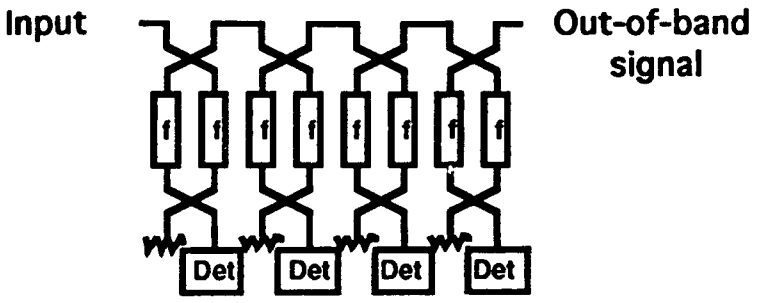


Figure 5 Channelizer Architecture

was assumed that apertures were remotely located from the receiver assets, which contributes to the high equivalent front end noise figure. The 0.5 dB sensitivity improvement and less than 3 dB 2TDR improvement would not justify the insertion of the superconducting technology.

Hence came the push to look for insertions closer to the front end of the system. Because HTS electronics can provide a package of small size, weight and power consumption, insertion at the remote aperture locations was then investigated. The other feature of the HTS channelizer which makes this insertion feasible is the architecture of the filterbank itself. This design, as shown simplistically in Figure 5, manifolds the input signal to the individual filters with very low loss couplers. Input signal which is out of band of the channelizer will flow through the channelizer with minimal loss. This feature led to the hypothesis of the system architecture shown in Figure 6. This application would allow the detection of signal in the channelizer bandwidth at very high sensitivity. With narrowband channelized detection immediately behind the aperture, the noise figure of this path will be substantially (>15 dB) reduced, with commensurate increase in sensitivity in that band. The signals outside of the channelizer bandwidth are passed through the device to be processed in the normal fashion by the existing system. The insertion loss in this path depends on the number of filters, and therefore couplers in

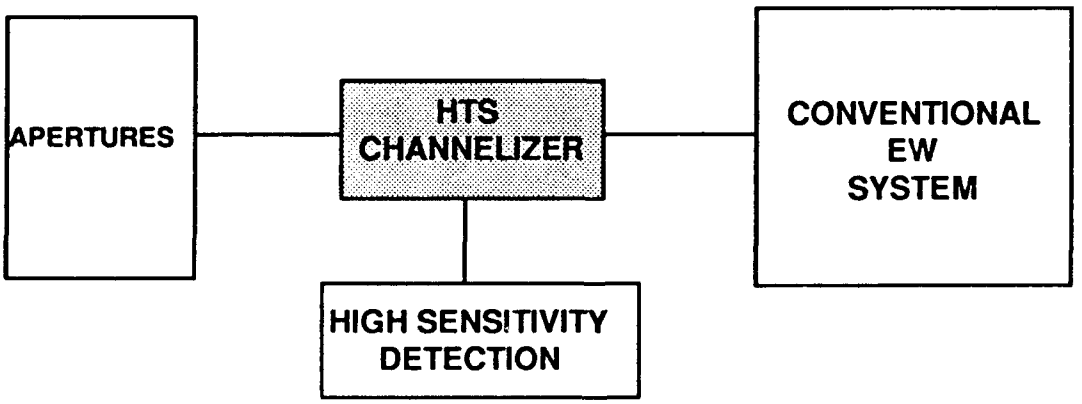


Figure 6 Channelizer Insertion Preliminary Concept.

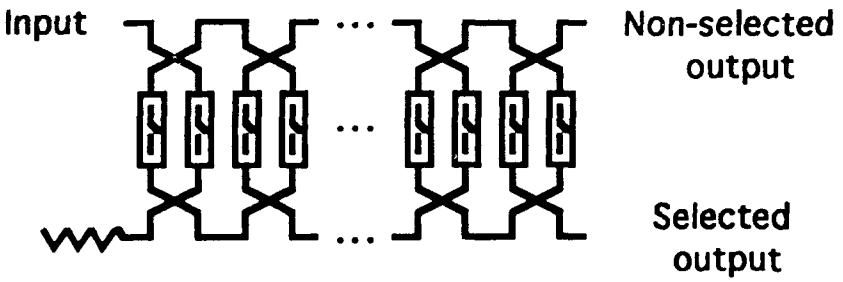


Figure 7 Flow-Through Switched Filterbank Concept of Operation

the manifold, of the channelizer.

Upon further investigation, this insertion approach was rejected for two reasons. First, there are only a limited number of applications where high sensitivity is only required for the limited portion of the frequency spectrum covered by the HTS channelizer. Secondly, and more important, was the fact that in this architecture the signals within the channelizer bandwidth would not be available for processing by the other host system components. (These might include interferometry measurements or detailed signal characterization.) The in-line nature of the channelizer in this architecture never allows in-band signals to be passed through to the existing system assets.

This problem led to the invention of the flow-through switched filterbank (FTSF). The FTSF mechanizes a three port device where the input is split between the two outputs as defined by the switch selections. As shown in Figure 7, the FTSF is similar in nature to the channelized filterbank. Instead of detectors on each filter output, however, the FTSF outputs are recombined with a manifold identical to the input manifold. Also a switch is imbedded within each of the filters, to selectively allow signal in that frequency range to pass through to the output or be passed on to the non-selected output. In this fashion, any portion of the input signal in the FTSF bandwidth can be selectively output to either of the two output ports. This overcomes the major deficiency identified previously for front end insertion of the channelizer.

The insertion concept for an EW system then evolved to the architecture shown in Figure 8. The original (Host) EW system can operate exactly as it had prior to insertion if all the switches are open, at the price of less than a dB added loss. Once again the loss is dependent on the number of filters, but this number can be kept to a minimum in the preselection function that is being performed. The improvement offered by this system are, however, still limited to the frequency range of the channelizer.

The latest step in the evolution of HTS insertion concepts expands the capability provided in Figure 8 by inserting a low noise amplifier and downconverter between the FTSF and the channelizer. This configuration, as shown in Figure 9, allows the enhanced sensitivity of the

HTS Channelizer and other components to be used throughout the total system frequency range. This sensitivity enhancement would be in the range of 8 to 10 dB over the Host system sensitivity defined in Figure 4. This equates at the system level to a *threefold increase in detection range*. Additional insertions of HTS components into EW systems can also be envisioned, including electrically small antennas, beamforming, IFM receivers, and notch filterbanks (an alternate configuration of the FTSF), but have not been considered to any extent for this demonstration/ insertion study. The insertion identified, however, has the advantage of providing not only a realistic near term insertion into an existing system, but also demonstrates major HTS components and system architecture for expansion to a totally HTS based system. Such an endeavor could not be envisioned for a first demonstration, based on prohibitive cost and development time. The system insertion depicted in Figure 9 will provide the baseline and risk reduction program around which future HTS developments could be structured.

Demonstration program description

Westinghouse has developed a two year HTS component demonstration program that will provide a vehicle for demonstrating the significant system benefits provided by HTS components and also provide the framework and system architecture for the early insertion of HTS components into an existing EW system. This program is described in detail in a White Paper entitled "High Temperature Super Conducting Switched Preselection Filter Bank". The proposed program will expand the scope of work of the present DARPA/ONR Channelizer program to include the development of the HTS Flow Through Switched Preselector shown in Figure 9 and in greater detail in Figure 10. The key feature of this program is a system concept and

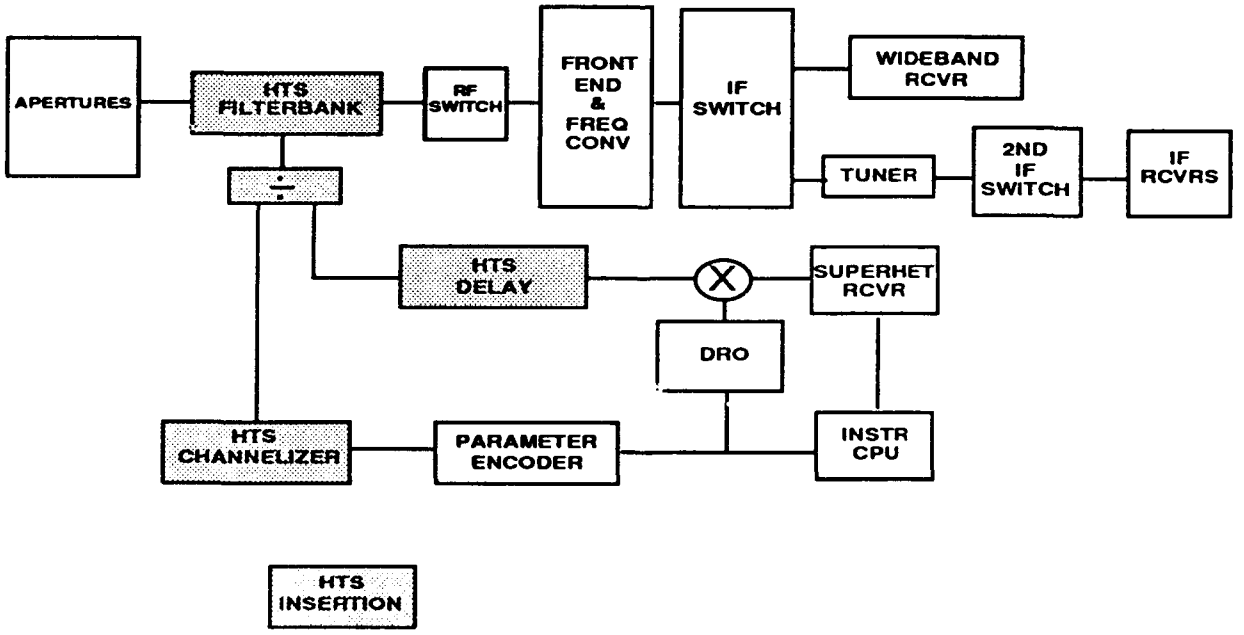


Figure 8 HTS Insertion Demonstrates Improved Performance in EW Application

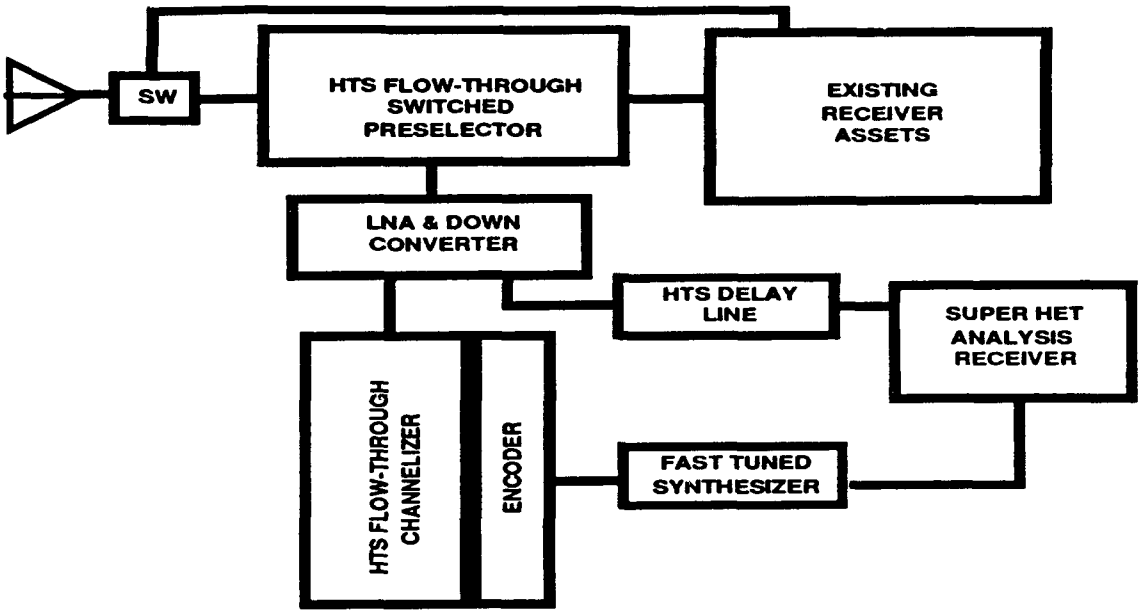


Figure 9 Recommended HTS Insertion Demonstration Architecture

architecture enabled by this device which will enable the insertion and demonstration of the HTS channelizer and delay lines in an existing EW/ELINT host system.

Multi-Phase HTS Development/Demonstration Program

The steps from the current contract leading to the demonstration of a complete HTS system inserted in a host EW system such as the one shown previously in Figure 9 are described below and shown pictorially in Figure 11.

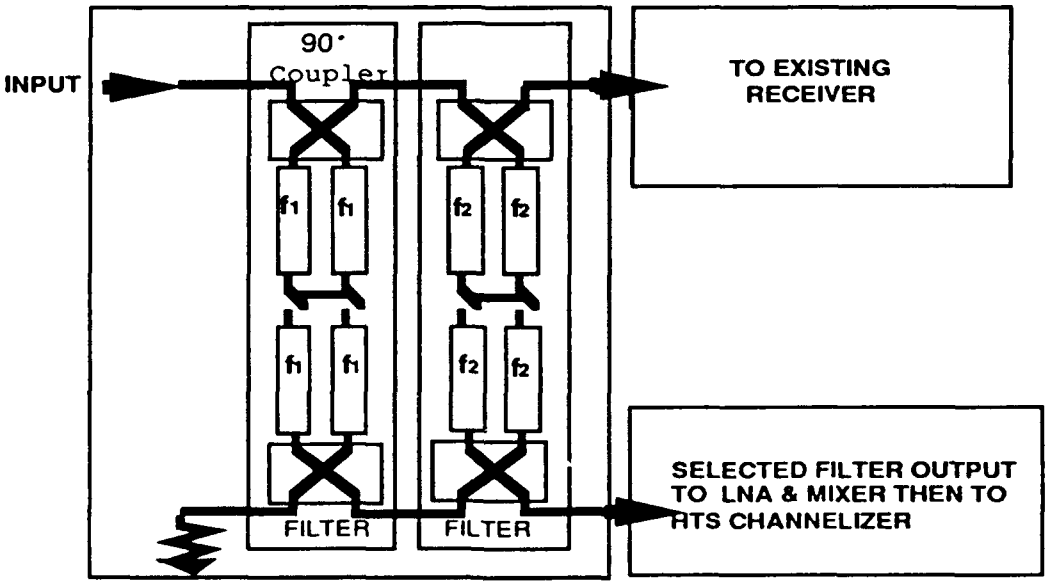


Figure 10 Proposed Flow-Through Switched Preselector

The first phase of this program is already underway with the building of the channelizer and the delay lines under the current contract. The second phase is the proposed expansion of the current program to include the Flow Through Switched Preselection as detailed in the White Paper. This phase would demonstrate that a low loss preselector could be inserted in a host system with little or no adverse impact on the host and would highlight the enhanced sensitivity attainable from HTS components placed near the front end of receiver systems. It would also demonstrate the performance of the unique HTS switched filter architecture.

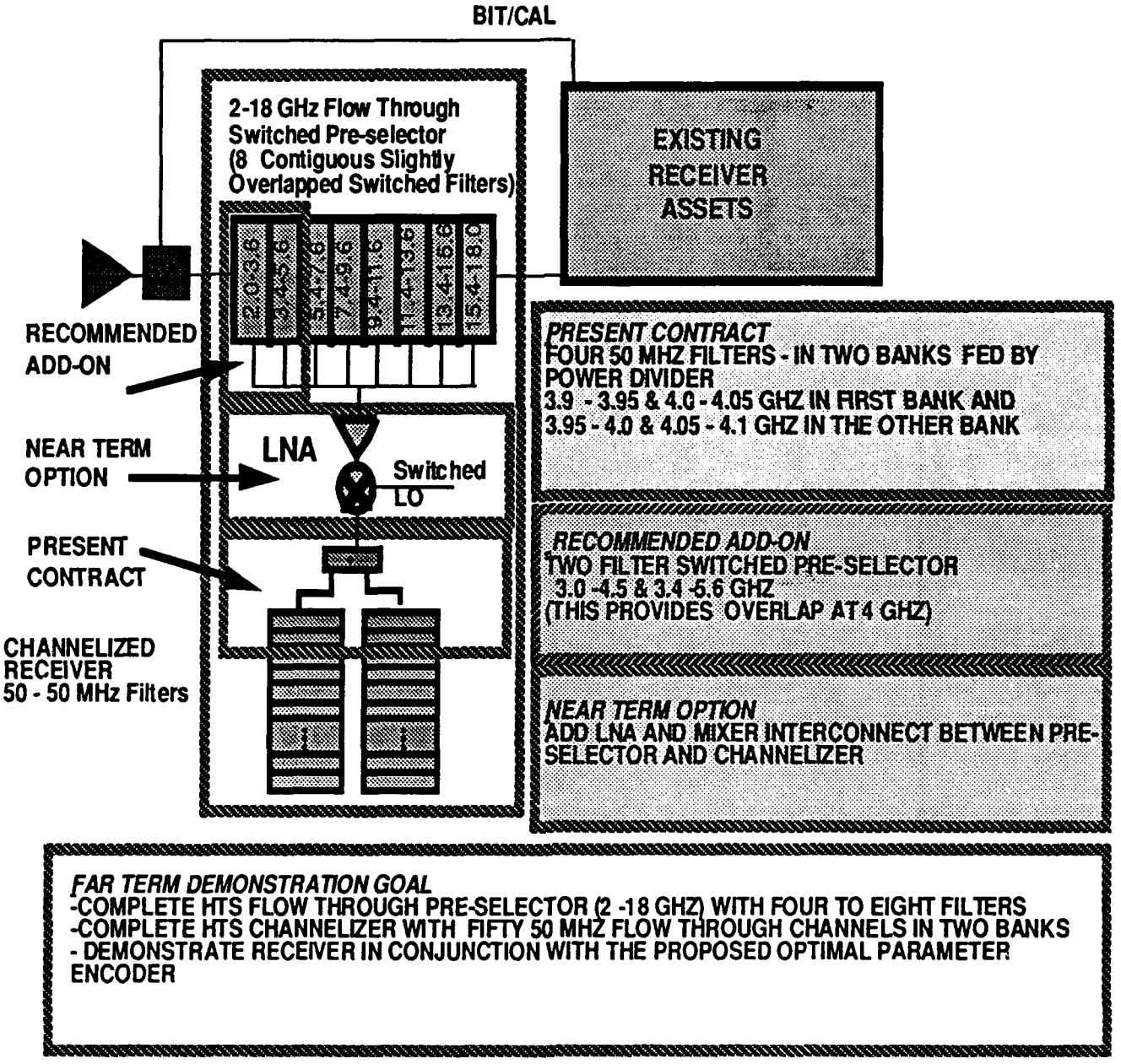


Figure 11 Multi-Phase HTS Receiver Development Program

In the next phase a low noise amplifier and down converter would be added to direct any selected 2-18 filterbank output into the channelizer at 4 GHz.

The final phase of the program would see the fabrication of the complete FTSP to cover 2-18 GHz and the expansion of the current contracts channelizer to a 20 filter, 1 GHz wide device. An existing parameter encoder would be used to demonstrate end to end receiver system performance.

At this point all the major components of an HTS architecture receiver system would have been fabricated, tested and demonstrated. The complete demonstration system could be directly inserted into an ELINT system for Demonstration Validation. The HTS demonstration system components would also serve as risk reduction for future development of HTS components and/or complete systems to be used in tactical system applications.