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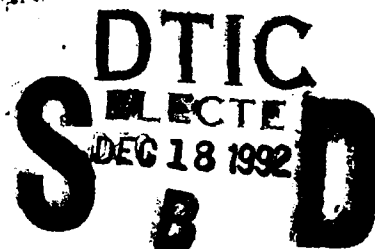


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PLANAR MONOLITHIC SCHOTTKY VARACTOR DIODE MILLIMETER-WAVE FREQUENCY MULTIPLIERS

University of Virginia

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ABSTRACT

A critical component of the millimeter-wave superheterodyne receiver is the local oscillator (LO) which is used to pump the low-noise mixer, be it a Schottky diode or an SIS junction. Frequency multipliers have been used for many years to produce LO power. Current technology uses the whisker-contacted Schottky varactor diode which is inherently very fragile, expensive to fabricate, difficult to optimize, and requires as many as three mechanical tuners. Future instrumentation will demand ever more stringent specifications on designability, performance, and reliability.

This report describes the design, fabrication, and evaluation of four planar frequency multiplier designs. The "direct-replacement" design demonstrates how a discrete planar varactor can replace a whisker-contacted varactor in a waveguide-type 75/225 GHz tripler and yield comparable performance. The fully monolithic (MMIC) balanced-varactor 80/160 GHz doubler and balanced-varactor 80/240 GHz tripler designs illustrate that MMIC technology is practical throughout the millimeter-wave band. Finally, a high-power 31/94 GHz tripler design is presented. These MMIC multipliers are the first to 1) operate over 100 GHz, 2) use coplanar waveguide extensively, and 3) use inductance cancellation to permit simultaneous tuning of the varactor at the pump, idler, and output frequencies. This research shows that through the use of modern monolithic fabrication technology optimized, fixed-tuned, and very reliable millimeter-wave frequency multipliers are feasible.

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LIST OF SYMBOLS

A	-	Cross-sectional area
A_a	-	Cross-sectional area of the anode
a	-	Specified constant
b	-	Specified constant
b_m	-	Magnetic field penetration depth
C_{avg}	-	Average junction capacitance
C_f	-	Fringing capacitance (associated with finger or whisker)
C_j	-	Junction Capacitance
C_{j0}	-	Zero-biased junction capacitance
C_p	-	Shunt capacitance
C_{pp}	-	Parallel-plate capacitance
C_T	-	Total measured capacitance
d	-	Plate separation
$\mathcal{E}$	-	Electric field
f	-	frequency
f_{nml}	-	Rectangular cavity resonant frequencies
f_s	-	Scattering frequency
G_a	-	Conductance per unit length (active region)
G_d	-	Conductance per unit length (depleted region)
G_j	-	Diode forward-biased junction conductance
g	-	Ground plane separation (CPW)
I	-	Current
I_k	-	Fourier coefficient of current
i_d	-	Diode current
J_0	-	Bessel function of first kind (order 0)

J_1	-	Bessel function of first kind (order 1)
j	-	Square root of (-1)
k	-	Integer
k_p	-	Propagation constant
k_s	-	Thermal conductivity of GaAs
k_q	-	Thermal conductivity of quartz
L_{bn}	-	Skin effect inductance in buffer at n^{th} ring
L_{buff}	-	Inductance associated with current in the buffer layer
L_d	-	Inductance per unit length
L_f	-	Finger inductance
L_n	-	Inertial carrier inductance at the n^{th} ring
ℓ	-	Integer
ℓ_a	-	Active n^- layer thickness
ℓ_a'	-	Length of undepleted region ($\ell_a - w$)
ℓ_e	-	Epitaxial layer thickness (buffer + active)
M_k	-	Complex modulation ratio at the k^{th} harmonic
m	-	Doping profile parameter
m'	-	Ionization integral constant
m_b	-	Mutual inductance
m_e	-	Electron effective mass
m_k	-	Modulation ratio at the k^{th} harmonic
m_o	-	Electron rest mass
N_0	-	Bessel function of second kind (order 0)
N_1	-	Bessel function of second kind (order 1)
N_d	-	Doping concentration
n	-	Integer

P_{DISS}	-	Dissipated power
P_{in}	-	Varactor input power
P_{norm}	-	Normalized power
P_{out}	-	Varactor output power
Q	-	Total charge
q	-	Unit charge
R_a	-	Resistance associated with the active (undepleted) layer
R_{an}	-	Active layer resistance of the n^{th} ring
R_b	-	Buffer layer resistance
R_{bn}	-	Buffer layer resistance of the n^{th} ring
RL	-	Return loss
R_{LOAD}	-	Load resistance
R_{in}	-	Input resistance
R_{OC}	-	Ohmic contact resistance
R_p	-	Parallel resistance
R_s	-	Diode series resistance
R_T	-	Thermal resistance
R_2	-	Pumped varactor resistance at 2_{nd} harmonic
R_3	-	Pumped varactor resistance at 3_{rd} harmonic
r	-	Radial distance
r_a	-	Anode radius
r_n	-	Radius of the n^{th} ring
r_{oc}	-	Ohmic contact inner radius
S	-	Junction elastance
S_{avg}	-	Average junction elastance ($1/C_{avg}$)
S_k	-	Fourier coefficient of elastance

$S_{\max}$	-	Maximum diode elastance
$S_{\min}$	-	Minimum diode elastance
s	-	Center conductor width (CPW)
$\text{TAN } \delta$	-	Loss tangent of material
T_o	-	Waveform period
t	-	Time
t_o	-	Time of elastance waveform maximum
t_m	-	Metal thickness
V	-	Voltage
V_B	-	Breakdown voltage
V_{bi}	-	Built-in potential
V_{BIAS}	-	Bias voltage
V_d	-	Voltage across the varactor diode
V_j	-	Junction voltage
V_k	-	Fourier coefficient of voltage
$V_{\min}$	-	Minimum diode voltage
w	-	Depletion region width
X_c	-	Reactance of open stub (balun)
X_k	-	Pumped varactor reactance at the k^{th} harmonic
X_L	-	Reactance of shorted stub (balun)
x	-	Cartesian coordinate
Y_o	-	Characteristic admittance
Z_A	-	Characteristic of shorted stub (balun)
Z_B	-	Characteristic impedance of open stub (balun)
Z_n	-	Embedding impedance at the n^{th} harmonic
Z_o	-	Characteristic impedance

α_n	-	Ionization rate for electrons
α_p	-	Ionization rate for holes
δ_b	-	Skin depth in the buffer layer
δ_m	-	Skin depth in anode metal
ϵ_o	-	Free space permittivity
ϵ_r	-	Relative dielectric constant
ϵ_s	-	Semiconductor permittivity
ζ	-	Complex propagation constant
η	-	Varactor efficiency
η_m	-	Multiplier efficiency
λ_g	-	Guide wavelength
μ	-	Permeability
μ_e	-	Electron mobility
μ_o	-	Free space permeability
μ_s	-	Semiconductor permeability
π	-	3.141592653589793
σ	-	Conductivity
σ_a	-	Active layer conductivity
σ_b	-	Buffer layer conductivity
σ_d	-	Depleted region conductivity
σ_m	-	Anode metal conductivity
ϕ	-	Phase factor
ω	-	Radian frequency
ω_c	-	Dynamic cutoff frequency
ω_o	-	Pump frequency
ω_s	-	Scattering frequency

CHAPTER ONE

INTRODUCTION

1.1 Program Description

The focus of this Rome Laboratory sponsored research was to explore new ideas in planar millimeter-wave component design. This research encompasses two critical components for superheterodyne receivers - the low noise mixer and the frequency multiplier.

A submillimeter-wave mixer using the University of Virginia planar Schottky diode was studied. This work examines the theoretical frequency limitations of the mixer, the high frequency loss from the n^+ GaAs layer, the dimensions of the waveguide and microstrip enclosure required for single mode propagation, and the diode parasitic reactances. This mixer design includes the circular waveguide to shielded microstrip transition, the non-contacting adjustable waveguide short circuit, the DC return, and the IF low pass filter. Large scale models (lower frequency replicas of the submillimeter-wave circuit) were used to design these sub-components so that a vector network analyzer could measure the RF performance. These scale model measurements proved valuable for the exploration of the optimum impedance required at the diode terminals. This submillimeter-wave mixer was fabricated and tested. The results indicate performance on the same level as the best whisker-contacted room temperature mixers for submillimeter wavelengths. Complete details are given in Newman, T., W. Bishop, K.T. Ng, and S. Weinreb, "A Novel Planar Diode Mixer for Submillimeter-wave applications", *IEEE Trans on Microwave Theory and Tech.*, vol. 39, no. 12, Dec. 1991, pp. 1964-1971. A copy of this paper is

included in Appendix K.

A Monolithic (MMIC) 75-110 GHz mixer incorporating the University of Virginia planar Schottky diode was also studied. The investigation included a nonlinear mixer analysis, the study of higher-order modes in the mixer structure, the analysis of propagation characteristics of enclosed microstrip on GaAs, a scale model study of a microstrip to waveguide probe, and a full RF design on the MMIC structure. This study did not include experimental data on a fabricated structure.

The core of this program was the study of millimeter-wave frequency multipliers primarily for local oscillator (LO) applications. The millimeter-wave LO is used to "pump" the low-noise mixer, be it a Schottky diode or an Superconductor-Insulator-Superconductor (SIS) junction, such that the important features of the incoming radiation are preserved upon frequency down-conversion to an intermediate frequency (IF) band where detection and signal processing techniques can be easily applied. RF power requirements range from 100 μ W to 1 mW for pumping SIS junctions and 1 mW to 10 mW for Schottky detectors. The application of current LO technology in the design of future instrumentation is highly questionable and even falls short of the design goals because of a number of design-inherent mechanical and electrical shortcomings. In the following sections of this chapter, the characteristics and performance of fundamental LO sources will be examined, clearly showing the deficiencies of the current state-of-the-art in meeting the future design goals. Frequency multiplication, an alternative method of LO power generation which has been in use for many years, will also be explored. A summary of the state-of-the-art of frequency multiplication and a brief discussion

of its shortcomings will be presented. Finally, future advances in frequency multiplier technology, the subject of this report, will be described briefly; clearly showing the scope of this research in relation to the current state-of-the-art in millimeter-wave frequency multiplier design.

1.2 Fundamental millimeter- and submillimeter-wave Oscillators

A complete discussion of fundamental local oscillator technologies is presented in Appendix A, therefore only a brief summary is presented in this section. Fundamental sources of LO power above 100 GHz may be classified as either tube-type (vacuum or gas-filled) or solid-state devices.

Gaseous and Vacuum Tube Sources

Table 1.1 summarizes the tube-type devices including the Backward-Wave Oscillator (BWO), the Gyrotron, the Klystron, the far-infrared (FIR) Laser, the Ledatron, the Magnetron, and the new Vacuum Microelectronic Microstrip Amplifier (VMMA).

TABLE 1.1 TUBE-TYPE FUNDAMENTAL LOCAL OSCILLATOR SOURCES							
DEVICE NAME	FREQUENCY	RF POWER	TUNING	SUPPORT EQUIP.	AVAILABLE	NOTES	REF.
BWO	Up to 1500 GHz	1 mW at 1500 GHz > 300 mW at 200 GHz	Wide Band > 20 %	Cooling HV DC Pwr	Commercial	Bulky Massive Magnetic	Kantorowicz 1979 Laundrie 1990
Gyrotron	Up to 614 GHz 2nd Harmonic	> 1kW at 326 GHz 1 uW at 614 GHz	Wide Band	Cooling HV DC Pwr	Research	Bulky Massive Magnetic	Brand 1990 Zaytsev 1974
Klystron	Up to 100 GHz	> 100 mW	Narrow Band < 10%	Cooling HV DC Pwr	Commercial	Bulky Massive Low Noise	Kantorowicz 1979
LASER FIR	> 150 GHz	1 nW to Watts Power varies with line	Fixed to spectral line	Cooling HV DC Pwr Vacuum Gas Supply	Commercial	Very Bulky Very Massive Very low noise	Densing 1991 Inguscio 1986
Ledatron	Up to 100 GHz	1 W at 70 GHz	> 30 %	Cooling HV DC Pwr	Research	Quasi-Optical Bulky	Mizuno 1979
Magnetron	Up to 70 GHz	>> 1 MW PULSED	Narrow Band	Cooling HV DC Pwr	Commercial up to 10 GHz	Compact Massive Magnetic	Liao 1985
VMMA	> 100 GHz Theory	> 1 Watt Theory	Wide Band > 20 %	Cooling HV DC Pwr	Research	Quasi-Planar Small Size	McGruer 1991

The most obvious problems with the BWO, Gyrotron, Klystron, FIR Laser, and Ledatron are the physical size and weight of the tube and the required support equipment. However, for laboratory use and for astronomical observation flights aboard aircraft where size and reliability are not of major concern, these units have provided years of

successful operation. As for space science applications or for array requirements, only the VMMA shows some promise due to its compact size, however such a device has yet to be demonstrated experimentally.

The various RF vacuum tubes have mixed attributes: The Gyrotron is a high power tube with a wide tuning bandwidth which may find use in millimeter-wave array applications where the LO for a large number of mixers can be supplied by a single phased-locked source. With lower output power, the Gyrotron in the second harmonic mode can be used at sub-millimeter wavelengths. The Ledatron is a two-mode free electron beam device that uses a Fabry-Perot interferometer as the circuit resonator. This device is quite bulky and is only practical in the laboratory. The Magnetron is a very high pulse-power tube which has been used in radar applications since World War II. The pulsed nature of the tube makes it unsuitable for LO sources, but is included in Table 1.1 for completeness. The reliability of vacuum tube technology is compromised by the electron gun cathode which slowly erodes with use.

Solid-State Sources

Solid-state oscillators provide a compact and light-weight alternative to tube-type oscillators. Table 1.2 through 1.4 summarizes the solid-state amplifiers and oscillators which are sub-categorized into three groups: a) two-terminal devices, b) three-terminal devices, and c) grids of two and three-terminal devices. The two-terminal devices (Table 1.2) include the Josephson Oscillators, the Resonant-Tunneling Devices (RTD), Transferred-Electron Devices (TED) or Gunn diodes, and various Transit Time Diodes (TTD) including IMPATT, BARRITT, TUNNET, QWITT, and MITATT diodes.

**TABLE 1.2 SOLID-STATE FUNDAMENTAL LOCAL OSCILLATOR SOURCES
TWO-TERMINAL DEVICES**

DEVICE NAME	FREQUENCY	RF POWER	TUNING	SUPPORT EQUIPMENT	AVAILABLE	NOTES	REF.
Josephson	100 - 430 GHz	Up to 1.84 μ W Flux Flow	Elect.	Cryogenic LV DC Pwr	Research	Low Noise Bulky	Nagatsuma 1983
RTD Quantum Well	420 GHz 712 GHz	0.2 μ W 0.3 μ W	20 % Mech.	LV DC Pwr	Research	Low Noise Compact	Brown 1990
TED Gunn	30 - 100 GHz	350 - 60 mW	Narrow Band	LV DC Pwr	Commercial	Low Noise Compact	Millitech 1990
TTD IMPATT	100 - 200 GHz	1000 - 50 mW	10 %	LV DC Pwr	Commercial	Very Noisy Bias Stable Low Eff.	Kuno 1979
TDD BARRITT	10 GHz	10 mW	10 %	LV DC Pwr	Commercial	Very Noisy Bias Stable Very Low Eff.	Sze 1985
TDD TUNNETT	Up to 338 GHz	10 mW Pulse 20 mW @500 GHz Theory	10 %	LV DC Pwr	Research	Moderate Noise Bias Stable	Nishizawa 1979 Haddad 1990
TDD QWITT	100 GHz ?	Low Power (Theory)	?	LV DC Pwr	Research	Lower Noise Bias Unstable	Haddad 1990 Kesan 1987
TDD MITATT	150 GHz	3 mW	?	LV DC Pwr	Research	Very Noisy Bias Stable	Elta 1980

The Josephson and Quantum-well oscillators, although physically intriguing, have shown relatively low output power experimentally. Most of the TTD devices have inherent instability problems and some have even demonstrated period-doubling bifurcations (sub-harmonics) and chaos. The IMPATT is inherently very noisy and many alternative TTD charge injection schemes have been employed to reduce noise and increase operational frequency; however the noise is still high compared with other fundamental oscillator devices. The TED or Gunn diode oscillator has proven low noise performance, exhibited very good reliability after initial burn-in, and is very compact. Tuning can be accomplished by mechanically varying the size of a cavity or electrically varying the bias on a varactor in a tuning circuit. Further increases in tuning frequency are possible by operating in the harmonic enhancement mode. Such a system has been demonstrated with second and third-harmonic electrical tuning from 70 to 90 GHz. A reduction of phase noise and better temperature stability is possible through the use of dielectric resonators, however these systems are typically fixed tuned. With Gunn oscillators, relatively high output power is possible up to 100 GHz, but this power drops very rapidly with further increases in frequency because of the finite semiconductor-inherent electron mobility and saturation velocity.

Other solid-state devices that are potentially useful as millimeter-wave oscillators belong to the three-terminal device group (Table 1.3) which contains the various transistor high power amplifiers and oscillators. This group includes the High Electron Mobility Transistor (HEMT) or MODFET, the pseudomorphic HEMTs, the conventional MESFET, the Heterostructure Field-Effect Transistor (HFET), and the Heterojunction

Bipolar Transistor (HBT).

Tremendous advances in transistor technology over the past decade have pushed the frequency limits above 100 GHz. Experimental amplifiers using pseudomorphic HEMTs have demonstrated better than 100 mW of power and 3 dB of gain at 94 GHz which implies that stable oscillator design should be feasible. In fact, a dielectric resonator oscillator (DRO) using a HEMT has shown good stability with greater than 1 mW of power at 38 GHz. Although this technology may replace or supplement Gunn oscillators in the near future, further increases in operating frequency will probably require many more years of research.

TABLE 1.3 SOLID-STATE FUNDAMENTAL LOCAL OSCILLATOR SOURCES THREE-TERMINAL DEVICES							
DEVICE NAME	HIGHEST OPERATING FREQUENCY	RF POWER OR GAIN	TUNING	SUPPORT EQUIPMENT	AVAILABLE	NOTES	REF.
HEMT MODFET	94 GHz	3.4 mW 2 dB	-	LV Bias Supply	Commercial & Research	Very Reliable	Smith 1986
Pseudo-morphic HEMT	94 GHz	9 mW 3.3 dB 62.7 mW 4 dB	-	LV Bias Supply	Research	InGaAs Quantum Well	Smith 1988 Streit 1991
PDD, Pseudo-morphic HEMT	60 GHz 94 GHz	100 mW 3 dB 57 mW	-	LV Bias Supply	Research	Added AlGaAs Doping	Smith 1987 Kao, 1989
MESFET	92.3 GHz	14 mW	-	LV Bias Supply	Research	InGaAs	Shellenberg, 1991
Doped-Channel HFET	94 GHz	32 mW 3 dB	-	LV Bias Supply	Research	Improved Trans-conduct.	Smith 1989
HBT	120 GHz f(max)	?	-	LV Bias Supply	Research	GaAlAs/GaAs	Asbeck 1987
HFMT in DRO	38 GHz	1 mW	Fixed	LV Bias Supply	Research	Very Stable	Wilson 1991

Planar grids of MESFETs and Gunn diodes make up the third group (Table 1.4) of solid-state oscillators. The data in Table 1.4 is for discrete device prototype systems with proven success. The technology, which has demonstrated very good performance at low frequencies, is intrinsically planar and scaling it to the millimeter-wave frequencies should be a rather straightforward procedure, although this has not yet been accomplished. The quasi-optical nature of the output makes the systems fairly bulky, but this is commonplace above 300 GHz where conventional waveguide is becoming inconveniently small.

TABLE 1.4 QUASI-OPTICAL PLANAR GRID OSCILLATORS							
DEVICE NAME	OPERATING FREQUENCY	RF POWER	TUNING	SUPPORT EQUIPMENT	AVAILABLE	NOTES	REF.
MESFET (5 X 5)	9.7 GHz	20.7 Watts ERP	Over 10 %	LV DC Pwr	Research	Discrete Devices	Popovic 1988
MESFET (10 X 10)	5 GHz	21 Watts ERP	Over 10 %	LV DC Pwr	Research	Discrete Devices	Popovic 1991
Gunn Diodes (4 X 4)	9.6 GHz	22 Watts ERP	Over 10 %	LV DC Pwr	Research	Discrete Devices Overheat Problems	York 1990

Therefore, based on the current state-of-the-art in fundamental LO design, the only viable approach for low noise, space-qualified, compact, light-weight, and reliable LO systems above 100 GHz in the near future appears to be a Gunn oscillator in cascade with a frequency multiplier. However, as with the fundamental sources, there are a number of inherent problems associated with this approach. In the next section, the state-of-the-art in millimeter-wave frequency multiplier designs will be examined, problems will be identified, and a clear direction for the present research will be disclosed.

1.3 Millimeter- and Submillimeter-wave Frequency Multipliers

A complete description of the current state of millimeter and sub-millimeter-wave frequency multiplier technology is presented in Appendix B, hence only a brief summary of the state-of-the-art is presented in this section. Table 1.5 gives a brief categorization of the types of frequency multipliers in use today for the generation of LO power up to 800 GHz.

TABLE 1.5 Categorization of Frequency Multiplier Technologies	
SYM	DESCRIPTION
B	Whisker-contacted PIN diode across output waveguide.
F	FET in a microwave integrated circuit (MIC) or monolithic circuit (MMIC).
Fb	Balanced pair of FETs in a microwave integrated circuit (MIC) or monolithic circuit (MMIC).
G	Grid or two-dimensional matrix of planar abrupt-junction Schottky diodes.
H	Whisker-contacted hyper-abrupt junction Schottky diodes across output waveguide.
I	Epitaxially-stacked P-N varactor diodes mounted across waveguide (ISIS).
M	Abrupt-junction planar Schottky diode in a planar microwave integrated circuit (MIC).
Mb	Balanced abrupt-junction planar Schottky diode pairs in a planar microwave integrated circuit (MIC).
MM	Abrupt-junction Schottky diode incorporated into a monolithic microwave integrated circuit (MMIC).
MMb	Balanced abrupt-junction Schottky diode pairs incorporated into a monolithic microwave integrated circuit (MMIC).
NL	Nonlinear transmission line
P	Planar abrupt-junction Schottky diode across output waveguide.
Pb	Balanced pair of planar abrupt-junction diodes across output waveguide.
Q	Whisker-contacted quantum well diode across output waveguide.
Qc	Whisker-contacted quantum-well diode in a coaxial mount.
S	Whisker-contacted abrupt-junction Schottky diode across output waveguide.
Sb	Balanced pair of whisker-contacted abrupt-junction Schottky diodes across output waveguide.
ST	Planar Soliton

The most widely used technology is the abrupt-junction Schottky diode in its many forms which include whisker-contacted, discrete planar, monolithic, and grid geometries. Other two-terminal devices in use are

the BIN, hyper-abrupt Schottky, ISIS, and quantum-well. FET's are also used in both Microwave Integrated Circuit (MIC) and Monolithic Microwave Integrated Circuit (MMIC) designs. Finally, distributed element frequency multiplier designs including nonlinear transmission lines and soliton wave generators have also been investigated in the laboratory.

The power available at a particular frequency is of primary importance in the design of receiver and LO systems for millimeter and sub-millimeter-wave operation. Summary of the state-of-the-art multiplier output power versus frequency is presented in Fig. 1.1. The graphs of Fig. 1.1a and Fig. 1.1b contain over 75 multipliers covering 0 to 400 GHz and 400 to 800 GHz respectively. ONLY MEASURED OUTPUT POWER IS PRESENTED HERE, and no attempt has been made to qualify the power measuring procedure. See Appendix B for references. Table 1.6 compares the many multiplier schemes using the data of Figs. 1.1a and 1.1b and the information in Appendix B.

LEGEND

- DOUBLER
- ▲ TRIPLER
- QUADRUPLER
- QUINTUPLER
- SEXTUPLER
- OTHER

Output Power (W) vs. Frequency (GHz)

Frequency (GHz)	Output Power (W)	Tube Type
0.1	10	17
0.1	1	148
0.1	0.1	152, 17
0.1	0.01	MM13
0.1	0.001	MM12, MB35
0.1	0.0001	ST41, M33, MB49, MB15, MB17, MB25, MB39, MB40, MB51, MB54, MB55, MB56, MB57, MB58, MB59, MB60, MB61, MB62, MB63, MB64, MB65, MB66, MB67, MB68, MB69, MB70, MB71, MB72, MB73, MB74, MB75, MB76, MB77, MB78, MB79, MB80, MB81, MB82, MB83, MB84, MB85, MB86, MB87, MB88, MB89, MB90, MB91, MB92, MB93, MB94, MB95, MB96, MB97, MB98, MB99, MB100
0.1	10	17
0.1	1	148
0.1	0.1	152, 17
0.1	0.01	MM13
0.1	0.001	MM12, MB35
0.1	0.0001	ST41, M33, MB49, MB15, MB17, MB25, MB39, MB40, MB51, MB54, MB55, MB56, MB57, MB58, MB59, MB60, MB61, MB62, MB63, MB64, MB65, MB66, MB67, MB68, MB69, MB70, MB71, MB72, MB73, MB74, MB75, MB76, MB77, MB78, MB79, MB80, MB81, MB82, MB83, MB84, MB85, MB86, MB87, MB88, MB89, MB90, MB91, MB92, MB93, MB94, MB95, MB96, MB97, MB98, MB99, MB100

Figure 1.1a Frequency multiplier output power versus frequency up to 400 GHz. (See Appendix B).

STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE

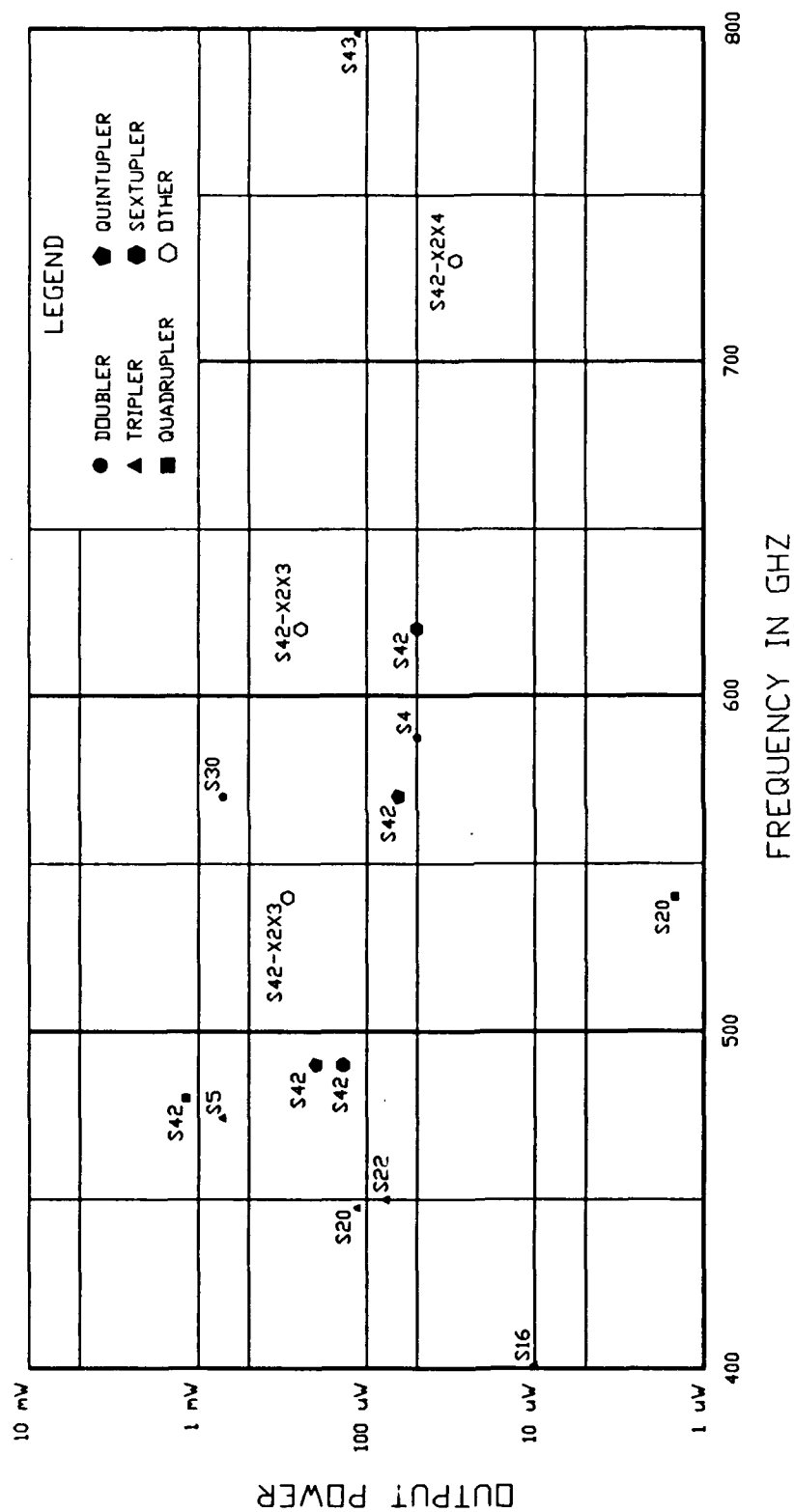


Figure 1.1b Frequency multiplier output power versus frequency from 400 to 800 GHz (See Appendix B).

Table 1.6 Frequency Multiplier Technology Attributes						
TECHNOLOGY	SYM	NUMBER OF DEVICES	MOUNT	FREQUENCY RANGE	ADVANTAGES	DISADVANTAGES
Abrupt-Junction Schottky	S	1	Whisk. W/G	60 - 800 GHz	+ Very high frequency operation	- Poor mechanically - Difficult to build
	Sb	2	Whisk. W/G	85 - 166 GHz	+ Higher power than S	- Poor mechanically - Extremely hard to build - Matched diode pair needed
	P Pb	1 2 BAL	W/G	Up to 200 GHz	+ More rugged than Sb	- Less BW than S - Lower operating freq. than S
	M Mb	1 2 BAL	MIC	Up to 94 GHz	+ Very rugged + Easy to build + Over 10 mW out + Min. mech. tuning	- Currently low frequency - Hard to optimize - Big electrically
	MM MMb	1 or 2 2 BAL	MMIC	Up to 37 GHz Up to 94 GHz	+ Very rugged + Monolithic fab + > 20 mW out + Easily optimized + Min. mech. tuning	- Currently low frequency
	G	>> 2	Planar	66 GHz	+ Power > 500 mW + Less mech. tuning	- Fab. yield prob. - Quasi-optical
Hyper-abrupt Schottky	H	1	Whisk W/G	200 - 230 GHz		- Substrate difficult to fab. - Less power than S
BIN	B	1	Whisk W/G	95 GHz	+ Improvements pending	- Same efficiency as S
ISIS	I	1	W/G	Up to 90 GHz	+ Power up to 5 Watts + Rugged	- Low power above 100 GHz
Quantum Well	Q Qc	1	Whisk W/G	Up to 280 GHz	+ Planar design pending	- Low power - Low efficiency
FET	F Fb	1 2 BAL	MIC/ MMIC	Up to 180 GHz	+ Very rugged + Easy integration with amplifiers + Min. mech. tuning	- Currently low frequency - Lower power than ISIS - Narrow band
NLTL	NL	-	Planar	100 - 110 GHz	+ Very rugged + Min. mech. tuning	- Currently low frequency
Soliton	ST	-	Planar MMIC	26 - 40 GHz	+ Very rugged + Very wide BW w/o tuning	- Difficult fab.

From the information in Fig. 1.1 and Table 1.6, a number of observations can be made about the state-of-the-art of frequency multipliers. Although the mainstay technology appears to be the abrupt-

junction Schottky diode, a closer look reveals some interesting trends.

For near watt level power requirements up to 100 GHz, the ISIS varactor in waveguide dominates; even surpassing many fundamental sources such as Gunn and Klystron oscillators near 100 GHz. Strong unwanted harmonics and noise in the output are potentially troublesome. The power of the ISIS drops quickly above 100 GHz due to the low mobility of the p⁺ material. The ISIS multiplier currently has a narrow fixed bandwidth.

For moderate power levels of 1 to 100 mW up to 100 GHz, the rugged MIC and MMIC multipliers containing planar Schottky diodes are a good choice. The MIC technology can be pressed to even higher frequencies, however optimized designs are difficult to realize due to the electrically large bonding pads needed to attach the chip to the mounting circuitry. MMIC technology circumvents this problem through tight geometrical control via the photolithographic process, thus permitting integrated circuit/device layout and a more nearly optimized multiplier design. FET MMIC/MIC fabrication technology is currently being pushed to the geometrical limit (gate lengths less than 0.1 μm) and it is not yet clear whether it will be practical to obtain high power at higher frequencies. However, Schottky MMIC technology is not limited by this geometrical constraint and so it should be appropriate for higher frequency operation. Both MIC and MMIC FET/Schottky circuits are usually narrow band since tuning is performed on the planar chip using lumped elements and transmission lines. However, wide-band matching circuits may help increase the operational bandwidth in future designs.

The whisker-contacted Schottky in the region from 100 to 300 GHz is slowly being replaced by discrete planar Schottky diodes mounted across

waveguide. However, a direct comparison of performance between the whisker-contacted and planar Schottky structures is currently lacking. Research is needed to improve bandwidth. The ruggedness of the planar structure is appealing. Mechanical tuning is still a problem with such structures and the circuitry is far from providing optimum performance.

Above 300 GHz, the whisker-contacted Schottky is currently the only technology in use due to its high cutoff frequency (small $R_s C_{j0}$ product), and low parasitic shunt capacitance. However, researchers are currently exploring ways to reduce the shunt capacitance of planar diodes by using quartz substrates or even eliminating the substrate altogether, thus forming a membrane-type structure. The size of the bonding pads must also be reduced thus making the chip rather difficult to mount. Future research on integrating the diode and mount is needed.

The more esoteric devices have mixed reviews. Hyper-abrupt Schottky, BIN and quantum-well devices have shown very little improvement over the abrupt-junction Schottky diode for multiplier applications and although research is currently underway to enhance device performance, no major improvements are anticipated. The distributed element multipliers have two major advantages: wide bandwidth without tuning, and a rugged planar structure. However, much research is needed in this area to improve the output power levels and increase the operating frequency.

1.4 Research Objectives

Although fundamental oscillators usually generate power with low unwanted harmonic content, it is frequency multiplier technology that has proven power generation in the millimeter and sub-millimeter wave bands.

Multiplier technology will continue to dominate in the foreseeable future unless higher power and lower noise fundamental sources are developed very rapidly. The major problem that limits the ability of present multiplier technology above 100 GHz to meet the requirements of future space and array projects appears to be the lack of mechanical ruggedness of both the whisker-contact and the mechanical tuning elements. Robust, wide-band, fixed-tuned multipliers for above 100 GHz are simply not available and research in this area is urgently needed.

From the discussion in Section 1.3, it is apparent that the discrete planar and monolithic Schottky technologies provide a viable solution to this problem under 100 GHz and may be a viable approach for higher frequencies as well. Therefore, the research presented in this report primarily examines the problems of extending planar technology, both discrete and MMIC, to frequencies above 100 GHz. This work centers around two key areas: multipliers containing planar varactors in waveguide, and monolithic frequency multipliers.

In Chapter Two, the theory of Schottky varactors is closely examined to develop an approach which more effectively incorporates the circuit and diode into an optimized multiplier package. In Chapter Three, planar varactor diodes fabricated at the University of Virginia are tested in a proven 75/225 GHz tripler mount that was originally designed for whisker-contacted varactors. This "direct-replacement" strategy is useful for comparing performance with whisker-contacted varactors and for yielding insight into the nature of the problems encountered when attempting to extend the planar geometry to high frequencies. However, the circuit is not optimized for the planar Schottky diodes and the true performance of

the planar diode will be somewhat shadowed by this approach. The theory of multiple frequency multiplier circuits is examined in Chapter Four. Chapter Five examines monolithic circuit technology, specifically addressing issues of transmission line choice, lumped element performance, and wafer fabrication that underscore good optimized multiplier design. Chapters Six, Seven, and Eight describe, in detail, the design and evaluation of a prototype monolithic 80/160 GHz doubler, 80/240 GHz tripler, and a 31/94 GHz tripler respectively. These MMIC multipliers are performance-optimized and essentially tunerless, thus attempting to fulfil the need for rugged, compact, and reliable sources for millimeter-wave power generation. Discrepancies between experiment and predicted results are examined in Chapter Nine. Finally, the above research is summarized in Chapter Ten by listing the important contributions of this work and by suggesting a path for future study in this challenging area of microwave technology.

CHAPTER TWO

Theoretical Analysis of Schottky Frequency Multipliers

2.1 Introduction

The heart of any frequency multiplier circuit is the nonlinearity which by nature will transform monochromatic electromagnetic energy into its harmonically-related frequency components (and non-harmonically related frequency components if unwanted oscillations are generated). Microwave power at the input frequency energizes the nonlinearity (this action is known as **pumping**) which in turn transforms a fraction of this power into its harmonically-related frequency components that also take part in the pumping process. The output power at a given harmonic is extracted through filtering. The form of this nonlinearity directly affects the efficiency of the harmonic generating mechanism and hence deserves detailed study.

This chapter presents an overview of the abrupt-junction Schottky varactor theory as applied to frequency multipliers. The chapter begins with a brief review of abrupt-junction varactor physics which culminates in a dynamic varactor circuit model. Nonlinear circuit theory and large signal solutions are introduced for the doubler and tripler in preparation for applying this analysis in later chapters of this thesis. A more detailed description of Schottky varactor theory is presented in Appendix C.

2.2 The Choice of the Abrupt-Junction Schottky Varactor

As discussed in Chapter One, the n-type GaAs abrupt-junction Schottky diode has been used successfully in millimeter and sub-millimeter wave frequency multiplier designs. The nonlinearity of the diode manifests a twofold presence: (1) in the current-voltage and (2) in the charge-voltage relationships. Both types have been used successfully in frequency multiplier designs.

A variable-resistance element or VARISTOR is a device that exploits the nonlinear current-voltage nature of the diode. Unfortunately, due to the high resistive losses in such a device, the varistor efficiency, as theorized by Page (Page, 1956), is limited to $1/N^2$, where N is the harmonic number, e.g. a doubler is limited to a maximum efficiency of 25 percent and a tripler to 11 percent. However, Page's analysis is for equal embedding-impedances at each harmonic frequency and does not consider the case of optimum embedding-impedance at each harmonic where an improvement in efficiency may be possible, hence the above limitation is not an absolute limit.

The nonlinear charge-voltage relationship which manifests itself as a voltage-variable capacitance provides a much better mechanism for harmonic generation. As proven by Manley and Rowe (Manley, 1956), the efficiency of the pure variable-reactance diode or VARACTOR can approach 100 percent assuming no resistive losses. The frequency-power formulas of Manley and Rowe are quite general and can be applied to parametric amplifiers, frequency converters, etc. In the case of the frequency multiplier, the formulas are simply a statement of conservation of energy. In all practical applications however, the diode series resistance

substantially reduces the varactor efficiency. Except for frequencies approaching diode plasma resonance, which occurs above 500 GHz in GaAs (Benson, 1985), the frequency multiplier efficiency of the varactor should be greater than for the varistor, however the bandwidth of the varistor will be greater. Therefore, the theory presented in this chapter will pertain only to varactor-based multipliers.

The n-type GaAs abrupt-junction Schottky diode is formed when a metal such as Platinum is placed in intimate contact with uniformly doped n-type GaAs. The popularity of this diode is due largely to the uniformly doped GaAs epitaxial layer which can be easily and accurately grown by Molecular-Beam Epitaxy (MBE), Metal-Organic Chemical Vapor Deposition (MOCVD), or other technologies.

Research into several other types of varactor diodes has resulted in novel designs with improved varactor characteristics. The hyperabrupt junction varactor is a Schottky-barrier diode in which the active n-layer doping is a monotonically decreasing function of distance into the semiconductor. Although the maximum to minimum capacitance ratio is larger than for the abrupt junction, the series resistance is larger, leading to lower varactor efficiencies compared with the abrupt-junction (Lundien, 1982). The Barrier-Intrinsic-n⁺ (BIN) varactor consists of a delta-doped region near the Schottky contact which under biased conditions causes the depletion region to "snap" between the charge spike and the n⁺ region resulting in a larger capacitance ratio as compared with the hyperabrupt (Jou, 1987). The series resistance for this diode is quite large due the intrinsic GaAs region thus resulting in very poor multiplier performance. The modified BIN (or δ -doped) structure retains a large

capacitance ratio, however the intrinsic region of the BIN in this case is lightly doped to lower the series resistance (Rizzi, 1990). At lower power levels, this diode may give good efficiencies. The heterojunction varactor utilizes a quantum-well structure yielding higher electron mobility which also lowers the series resistance yet retains a large capacitance ratio (Peatman, 1991).

The above varactors are considered research devices which may in the future improve multiplier performance at the device level. However, currently the most practical varactor for MMIC applications is the abrupt-junction Schottky varactor because of (1) the existence of good devices, (2) the existence of good theoretical models, (3) a well-developed fabrication process, and (4) easily grown GaAs epitaxial structure. Hence, the abrupt-junction Schottky varactor was chosen to be used as a foundation for planar multiplier development in this thesis rather than adding unnecessary complication to the multiplier design.

2.3 Abrupt-Junction Varactor Theory

2.3.1 Introduction

In this section, the abrupt-junction diode equivalent circuit and characteristic equation are developed from knowledge of device physics. Beginning with the uniformly-doped active layer profile, the charge-voltage, and capacitance-voltage relationships are derived. An avalanche breakdown model is used to determine epitaxial layer thickness and capacitance limits. Components of the series resistance are discussed and the dynamic circuit model for the varactor is specified. Circuit theory is used to develop the characteristic equation of the varactor in the

frequency domain. A complete and more general analysis is given in Appendix C.

2.3.2 Charge, Capacitance, and Voltage Relationships

Fig. 2.1 is a sketch of the doping profile of a metal-semiconductor junction defining the active and buffer layers and the corresponding doping levels.

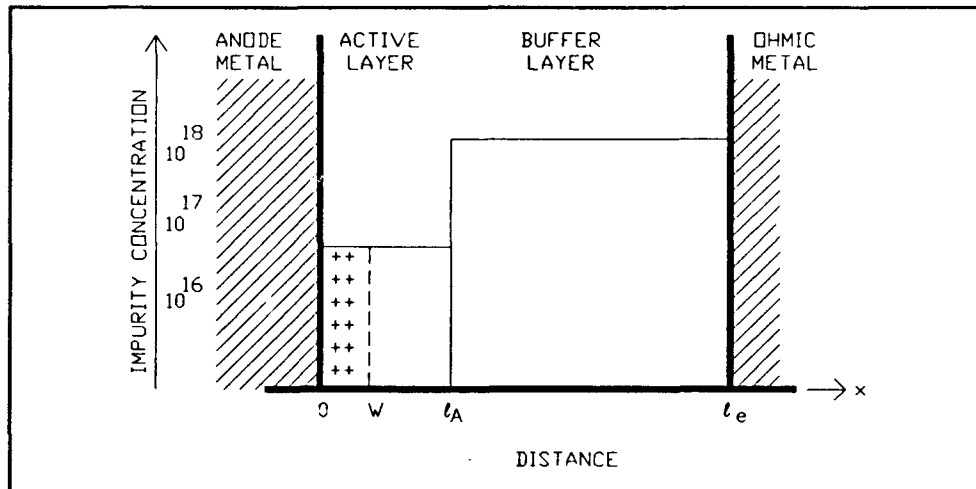


Figure 2.1 Sketch of the abrupt-junction diode epitaxial structure.

The doping profile used in abrupt-junction diodes is described by

$$N_d(x) = N_d \quad (2-1)$$

where $N_d(x)$ is the impurity concentration as a function of distance into the semiconductor from the metal and N_d is the active layer doping level which in this case is constant. In the depletion region, the ionized donor atoms have a positive charge, which induces a negative charge on the metal. Note that w is the width of the depletion region, l_A is the distance of the buffer/active layer interface from the metal at $x = 0$, and l_e is the buffer/substrate interface to metal distance.

Assuming a one-dimensional geometry, Poisson's equation can be applied to find the electric field and potential as a function of the applied voltage. The depletion region width as a function of the applied voltage is therefore

$$w(V_j) = \left[\frac{2(V_{bi} + V_j(t))\epsilon_s}{qN_d} \right]^{\frac{1}{2}} \quad (2-2)$$

where $w(V_j)$ is the depletion region width, V_{bi} is the built-in potential of the junction from thermionic emission theory, ϵ_s is the permittivity of the semiconductor, q is the unit charge, and $V_j(t)$ is the time-dependent voltage across the junction. The total charge Q in the depletion region can be found by integrating the impurity concentration over the region assuming 100% donor atom ionization. Substitution of eqn.(2-2) for w yields

$$Q(V_j) = qN_d \left[\frac{2\epsilon_s(V_{bi} + V_j(t))}{qN_d} \right]^{\frac{1}{2}} \quad (2-3)$$

The capacitance per unit area as a function of the applied voltage is found by taking the derivative of eqn (2-3) with respect to the applied voltage. After simplification, the capacitance-voltage relation becomes

$$C_j(t) = \left[\frac{qN_d\epsilon_s}{2(V_{bi} + V_j(t))} \right]^{\frac{1}{2}} \quad (2-4)$$

The elastance, $S(t)$, is defined as the reciprocal of the dynamic junction capacitance as follows:

$$S(t) = \frac{1}{C_j(t)} = \left[\frac{2(V_{bi} + V_j(t))}{qN_d\epsilon_s} \right]^{\frac{1}{2}} \quad (2-5)$$

Finally, solving eqn (2-3) for $V_{bi} + V_j(t)$ and substitution into eqn (2-5) yields the desired **ELASTANCE-CHARGE** relationship.

$$S(t) = \frac{1}{qn_d e_s} Q(t) \quad (2-6)$$

There are two important points to be noted concerning this result. First, eqn.(2-6) indicates that for an abrupt junction varactor, the elastance is directly proportional to the charge. This feature allows a simplification of the nonlinear multiplier analysis, permitting a closed-form solution. Second, eqn.(2-3) shows that the diode voltage is proportional to the square of the charge. If, for example, the pump voltage takes the functional form of a pure sinusoid, then the resulting charge will only have even harmonic components (the DC component is considered even). This indicates that the abrupt junction varactor can be used as a direct frequency doubler but if odd harmonics are required, e.g. tripler, then a non-sinusoidal voltage is required. This voltage is generated if the embedding impedances are finite and thus producing intermediate harmonics or "idlers".

2.3.3 Maximum Voltage Swing

The Schottky-barrier diode varactor regime is bounded by three important conditions. The maximum positive voltage is limited by the diode forward turn-on point, which is directly related to the built-in potential V_{bi} derived from thermionic-emission theory. Maximum reverse voltage is limited by avalanche breakdown and perhaps involving depletion-layer "punch-through" into the buffer layer.

Based on the work of Sze and Gibbons (Sze, 1966), the avalanche breakdown criterion for the generalized profile is:

$$\int_0^w a \text{Exp}\left[-\left(\frac{e_s b}{q N_d (x-w)}\right)^{m'}\right] dx = 1 \quad (2-7)$$

which is known as the ionization integral. For GaAs, $a = 3.5 \times 10^5$, $b = 6.85 \times 10^5$, and $m' = 2$.

Punch-through occurs when the leading edge of the depletion region crosses the active/buffer layer interface. If the active layer thickness is chosen such that punch-through and avalanche breakdown occurs at the same applied voltage, then the maximum possible voltage swing will be attained. In this case, the active layer thickness is determined by the depletion region width in the active layer at the point of avalanche breakdown.

2.3.4 Series Resistance

The series resistance of the Schottky diode consists of three components: the undepleted epitaxial-layer resistance, substrate resistance, and ohmic contact resistance. In the following analysis, high frequency effects such as displacement current and carrier inertia are not considered.

For the analysis of the undepleted epitaxial-layer series resistance R_s , the resistive region of interest lies between the depletion region edge and the active/buffer region interface at $x = l_n$ (see Fig. 2.1). Assuming no spreading in the active layer, a one-dimensional model with uniform cross-sectional area, the undepleted epitaxial-layer resistance for a generalized impurity profile is as follows:

$$R_s = \frac{1}{A_s q} \int_0^{\ell_s} \frac{1}{\mu_e(x) N_d(x)} dx \quad (2-8)$$

where A_s is the anode cross-sectional area, $\mu_e(x)$ is the electron mobility, and $N_d(x)$ is the impurity concentration as described in eqn. (2-1) where complete ionization has been assumed. An empirical formula for the carrier mobility was taken from (Sze, 1981):

$$\mu_e(x) = \frac{10^4}{1 + \frac{\sqrt{N_d}}{10^{\frac{17}{2}}}} \quad (2-9)$$

Substitution of eqns. (2-1) and (2-9) into eqn. (2-8) and carrying out the integration gives (after much simplification) yields

$$R_s(t) = \frac{1}{A_s q N_d} \left[\ell_s - \left(\frac{2 e_s (V_j(t) + V_{bi})}{q N_d} \right)^{\frac{1}{2}} \right] + \frac{N_d^{\frac{1}{2}}}{10^{\frac{17}{2}}} \left[\ell_s - \left(\frac{2 e_s (V_j(t) + V_{bi})}{q N_d} \right)^{\frac{1}{2}} \right] \quad (2-10)$$

which is a function of the applied voltage, but the variation is small compared with reactance of the nonlinear capacitance, hence nonlinear effects resulting from this resistance can be ignored. However, the maximum epitaxial resistance is used in the equation for total series resistance.

Assuming a cylindrical geometry, the substrate resistance R_b is the surface resistance of the substrate (Kelly, 1980):

$$R_b = \left[\frac{1}{2\pi\sigma_b\delta_b} \right] L \ln \left(\frac{r_{oc}}{r_s} \right) \quad (2-11)$$

where r_s is the anode radius, r_{oc} is the inner radius of the ohmic contact, and δ_b , is the skin depth defined as

$$\delta_b = \left[\frac{2}{\omega \mu_s \sigma_b} \right]^{\frac{1}{2}} \quad (2-12)$$

μ_s is the buffer permeability, σ_b is the buffer layer conductivity, and ω is the radian frequency.

The ohmic contact resistance R_{oc} can easily be 10^{-5} ohm/cm² and for contact areas of $< 10^{-3}$ cm², R_{oc} is very small in comparison with the other resistances and hence will be ignored (Kelly, 1980).

The total series resistance is therefore:

$$R_s = R_a + R_b \quad (2-13)$$

2.3.5 Varactor Circuit Model - Time Domain

The varactor circuit model which does not include parasitic elements is shown in Fig. 2.2. This model assumes that the Schottky diode

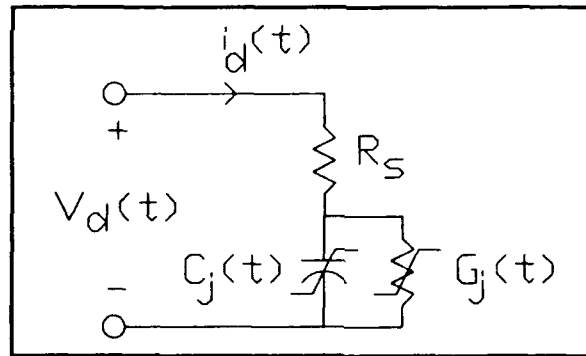


Figure 2.2 Varactor circuit model.

is biased and that the instantaneous voltage will not cause either diode forward turn-on or reverse breakdown, hence the diode is in the varactor regime and nonlinear resistive effects are neglected, i.e. $G_j(t)$.

Kirchhoff's voltage law is applied to the circuit model and the resulting integral equation relating the varactor voltage and current is

$$V_d(t) = \int S(\tau) i_d(\tau) d\tau + R_s i_d(t) \quad (2-14)$$

where $v_d(t)$ is the voltage across the varactor, $i_d(t)$ is the current through the varactor, $S(t)$ is the incremental elastance or inverse dynamic capacitance, and R_s is the total series resistance. Note that the elastance, which is time-varying, leads directly to the nonlinear behavior of the varactor.

2.3.6 Varactor Circuit Model - Frequency Domain

Let ω_0 be the multiplier input frequency, then assuming there are no unwanted spurious oscillations and chaotic effects, only commensurate frequencies of the form $k\omega_0$ are present in the voltage, current, and elastance waveforms of frequency multipliers (k is an integer).

Consider the varactor mounted in an embedding circuit as shown schematically in Fig. 2.3.

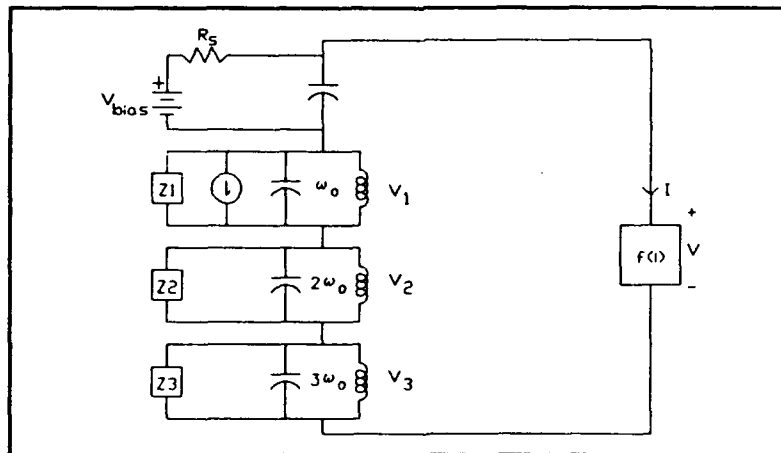


Figure 2.3 Schematic of varactor diode in an embedding circuit.

The Fourier series representation of the voltage, current, and elastance waveforms are

$$V_d(t) = \sum_{k=-\infty}^{\infty} V_k e^{jk\omega_o t} \quad (2-15)$$

$$i_d(t) = \sum_{k=-\infty}^{\infty} I_k e^{jk\omega_o t} \quad (2-16)$$

$$S(t) = \sum_{k=-\infty}^{\infty} S_k e^{jk\omega_o t} \quad (2-17)$$

Substitution of eqns.(2-15) through (2-17) into eqn.(2-14) yields the abrupt-junction varactor characteristic equation in the frequency domain:

$$V_k = R_s I_k + \frac{1}{jk\omega_o} \sum_l I_l S_{k-l} \quad (2-18)$$

where k and l are integers from $-\infty$ to $+\infty$. Note that the voltage at harmonic k is related to all harmonics of the current and elastance. In the next section, solutions to this equation are presented for the cases of the frequency doubler and tripler.

2.4 The Abrupt Junction Frequency Multiplier

The following solutions of eqn.(2-18) are based on the analysis of the abrupt junction varactor by Penfield and Rafuse (Penfield, 1962). Complete derivation of the large signal equations is presented in Appendix D. The doubler solutions are presented in subsection 2.4.1 followed by the tripler solutions in subsection 2.4.2.

Consider a pumped abrupt junction varactor with forward turn-on voltage taken to be V_{min} which gives rise to a minimum elastance S_{min} , and breakdown voltage V_B which gives rise to a maximum elastance S_{max} . The modulation ratio at that k^{th} harmonic, m_k , is defined as

$$m_k = \frac{|S_k|}{S_{max} - S_{min}} \quad (2-19)$$

where S_k is the Fourier coefficient at the k^{th} harmonic. The cutoff frequency, ω_c may be defined as

$$\omega_c = \frac{S_{\max} - S_{\min}}{R_s} \quad (2-20)$$

where R_s is the series resistance. Finally, the normalized power is defined as follows:

$$P_{\text{norm}} = \frac{S_{\max} - S_{\min}}{R_s} \quad (2-21)$$

2.4.1 Abrupt Junction Frequency Doubler

The following are large signal solutions of eqn.(2-18) for the frequency doubler. The only currents permitted are at dc (port $k = 0$), the input frequency ω_o (port $k = 1$), and the output frequency $2\omega_o$ (port $k = 2$). All other harmonics are open circuited, therefore, only $k = -2, -1, 0, 1$ and 2 are permitted. The large signal solutions are:

Input Resistance

$$R_{in} = R_s \left(2m_2 \frac{\omega_c}{2\omega_o} + 1 \right) \quad (2-22)$$

Output Resistance

$$R_2 = R_s \left(\frac{m_1^2}{2m_2} \frac{\omega_c}{2\omega_o} - 1 \right) \quad (2-23)$$

Input, Idler, and Output Reactance

$$X_k = \frac{S_{\text{avg}}}{k\omega_o} = \frac{1}{V_B + V_{\min}} \int_{V_{\min}}^{V_g} \frac{2}{k\omega_o} \left[\frac{(V_{bi} + V_j)}{qn_d e_s} \right]^{\frac{1}{2}} dV_j \quad (2-24)$$

Input Power

$$P_{in} = 8 P_{norm} \left(\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right)^2 \left(\frac{\omega_o}{\omega_c} \right)^2 m_1^2 \left(2 m_2 \frac{\omega_c}{2 \omega_o} + 1 \right) \quad (2-25)$$

Output Power

$$P_{out} = 8 P_{norm} \left(\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right)^2 \left(\frac{2 \omega_o}{\omega_c} \right)^2 m_2^2 \left(\frac{m_1^2}{2 m_2} \frac{\omega_c}{2 \omega_o} - 1 \right) \quad (2-26)$$

Dissipated Power

$$P_{diss} = 8 P_{norm} \left(\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right)^2 \left(\frac{\omega_o}{\omega_c} \right)^2 (m_1^2 + 4 m_2^2) \quad (2-27)$$

Varactor Efficiency

$$\eta = \frac{\frac{\omega_c}{2 \omega_o} - \frac{2 m_2}{m_1^2}}{\frac{\omega_c}{2 \omega_o} + \frac{1}{2 m_2}} \quad (2-28)$$

Note that for a given varactor (specified through ω_c and P_{norm}) and pump frequency ω_o , the large signal performance can be calculated if the values for m_1 and m_2 are known. The modulation ratios are interrelated, bounded by the elastance limits, influenced by the bias voltage, and proportional to the pump power at ω_o . Two external constraints are therefore imposed: (1) the elastance is fully modulated (from S_{max} to S_{min}), and (2) the circuit is optimized for maximum efficiency.

The full elastance modulation constraint sets the bias level which results in one equation relating the modulation ratios. To find the bias point, recall that the Fourier series for the elastance is

$$S(t) = \sum_{k=-\infty}^{\infty} S_k \sin(k \omega_o t + \phi) \quad (2-29)$$

where ϕ is a phase term.

Dividing both sides by $S_{\max} - S_{\min}$ yields

$$\begin{aligned} \frac{S(t)}{S_{\max} - S_{\min}} &= \sum_{k=-\infty}^{\infty} \frac{S_k}{S_{\max} - S_{\min}} \sin(k\omega_o t + \varphi) \\ &= \frac{S_o}{S_{\max} - S_{\min}} + 2 \sum_{k=1}^{\infty} \frac{|S_k|}{S_{\max} - S_{\min}} \sin(k\omega_o t + \varphi) \end{aligned} \quad (2-30)$$

However, note that

$$0 \leq \frac{S(t) - S_{\min}}{S_{\max} - S_{\min}} \leq 1 \quad (2-31)$$

Therefore eqn.(2-30) can be rewritten in the following form:

$$\begin{aligned} \frac{S(t)}{S_{\max} - S_{\min}} - \frac{S_{\min}}{S_{\max} - S_{\min}} &= \left[\frac{S_o}{S_{\max} - S_{\min}} - \frac{S_{\min}}{S_{\max} - S_{\min}} \right] \\ &+ 2 \sum_{k=1}^{\infty} \frac{|S_k|}{S_{\max} - S_{\min}} \sin(k\omega_o t + \varphi) \end{aligned} \quad (2-32)$$

Note that the term in brackets sets the symmetry point for the modulation and since maximum symmetrical elastance modulation is desired, this term is set to the midpoint of the range, i.e. 0.5, which gives S_o as

$$S_o = \frac{S_{\max} + S_{\min}}{2} \quad (2-33)$$

This leads directly to the required bias voltage, V_{bias} :

$$V_{\text{bias}} = \frac{V_B - V_{\min}}{2} \quad (2-34)$$

With the bias voltage set for symmetrical modulation, eqn.(2-32) can be rewritten as

$$\sum_{k=1}^{\infty} m_k \sin(k\omega_o t + \varphi) \leq 0.25 \quad (2-35)$$

where the equality is taken if the varactor is pumped for maximum modulation. In the case of the doubler, eqn.(2-35) becomes

$$m_1 \sin(\omega_o t) + m_2 \sin(2\omega_o t) = 0.25 \quad (2-36)$$

where the harmonic circuits are assumed to be tuned, i.e. $\phi = 0$.

The time t_o which gives rise to a maximum in the modulation waveform can be found by taking the derivative of eqn.(2-36) with respect to time and setting the result equal to zero thus yielding

$$m_1 \cos(\omega_o t_o) + 2m_2 \cos(2\omega_o t_o) = 0 \quad (2-37)$$

Solving for t_o yields

$$\cos(\omega_o t_o) = \frac{m_1}{8m_2} \left[\sqrt{1 + \frac{32m_2^2}{m_1^2}} - 1 \right] \quad (2-37)$$

The desired constraint equation for the modulation ratios (resulting from setting the bias level and input power level), is found by combining eqns.(2-36) and (2-38) to give the **breakdown limit curve** shown in Fig. 2.4 (curve A). The equation for this curve is

$$m_1 = \frac{1}{\sqrt{\frac{1}{2} + \frac{m_1^2}{32m_2^2} \left[\sqrt{1 + \frac{32m_2^2}{m_1^2}} - 1 \right] \left[3 + \left(\sqrt{1 + \frac{32m_2^2}{m_1^2}} - 1 \right) \right]}} \quad (2-39)$$

Under the maximum modulation condition, the operating point lies somewhere along the breakdown limit curve. However, for lower pump powers and under different bias conditions, the operating point can be anywhere under the curve. Points above the curve are not realizable due to the elastance limits set by the varactor.

To solve for a unique operating point, a second equation is needed. The operating point corresponding to maximum varactor efficiency was chosen. The second equation, eqn.(2-40), is simply the derivative of eqn.(2-28) with respect to m_2 and the result is set equal to zero to find

the maximum. This is curve B in Fig. 2.4.

$$m_2 = -\frac{\omega_o}{2\omega_c} + \frac{1}{2} \sqrt{\frac{\omega_o}{\omega_c} + \frac{m_1^2}{m_2}} \quad (2-39)$$

With eqns.(2-39) and (2-40), the program MathCAD¹ was used to calculate the operating point for varactors with different physical parameters. The results of this performance study are summarized in Chapter Six for the 80/160 GHz doubler. A sample MathCAD file is include in Appendix C.

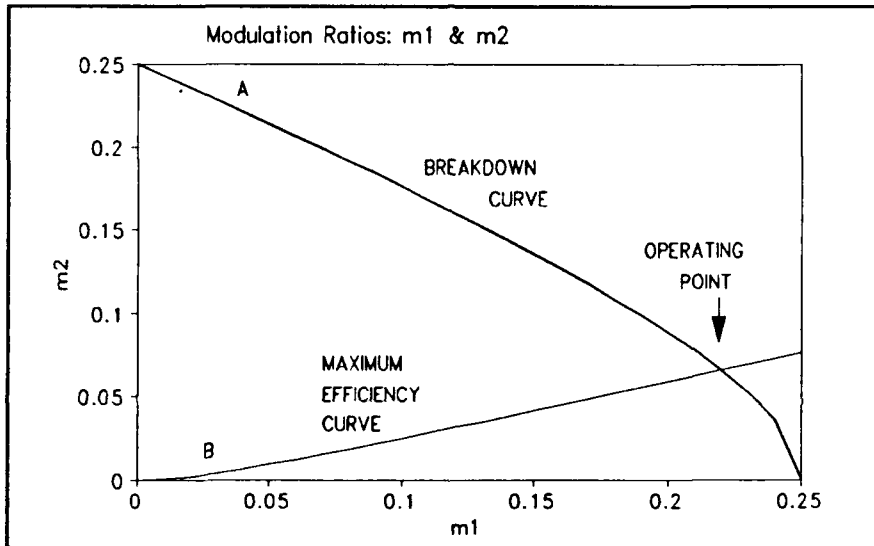


Figure 2.4 Breakdown limit and maximum efficiency curves in the m1-m2 plane.

2.4.2 Abrupt Junction Frequency Tripler

The following are large signal solutions of eqn.(2-18) for the frequency tripler. The only currents permitted are at dc (port $k = 0$), the input frequency ω_o (port $k = 1$), the idler frequency $2\omega_o$ (port $k = 2$), and the output frequency $3\omega_o$ (port $k = 3$). All other harmonics are open circuited, therefore only $k = -3, -2, -1, 0, 1, 2$, and 3 are allowed.

¹MathCAD is a product of MathSoft Inc. of Cambridge, MA

The large signal solutions for the tripler are as follows:

Input Resistance

$$R_{in} = R_s \left[\frac{\omega_c}{\omega_o} \frac{m_2}{m_1} (m_1 + m_3) + 1 \right] \quad (2-41)$$

Idler Resistance

$$R_2 = R_s \left[\frac{\omega_c}{4 \omega_o} \frac{m_1}{m_2} (m_1 + 2 m_3) - 1 \right] \quad (2-42)$$

Output Resistance

$$R_3 = R_s \left[\frac{\omega_c}{3 \omega_o} \frac{m_1 m_2}{m_3} - 1 \right] \quad (2-43)$$

Input, Idler, and Output Reactance

$$X_k = \frac{S_{avg}}{k \omega_o} = \frac{1}{V_B + V_{min}} \int_{V_{min}}^{V_B} \frac{2}{k \omega_o} \left[\frac{(V_{bi} + V_j)}{q n_d e_s} \right]^{\frac{1}{2}} dV_j \quad (2-44)$$

Input Power

$$P_{in} = 8 P_{norm} \left(\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right)^2 \left(\frac{\omega_o}{\omega_c} \right)^2 \left[\frac{\omega_c}{\omega_o} m_1 m_2 (m_1 + m_3) + m_1^2 \right] \quad (2-45)$$

Output Power

$$P_{out} = 8 P_{norm} \left(\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right)^2 \left(\frac{\omega_o}{\omega_c} \right)^2 \left[3 \frac{\omega_c}{\omega_o} m_1 m_2 m_3 - 9 m_3^2 \right] \quad (2-46)$$

Dissipated Power

$$P_{diss} = 8 P_{norm} \left(\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right)^2 \left(\frac{\omega_o}{\omega_c} \right)^2 \cdot \left[\frac{\omega_c}{\omega_o} (m_1^2 m_2 - 2 m_1 m_2 m_3) + m_1^2 + 9 m_3^2 \right] \quad (2-47)$$

Efficiency

$$\eta = \frac{3m_3}{m_1} \frac{\frac{\omega_c}{\omega_o} m_1 m_2 - 3m_3}{\frac{\omega_c}{\omega_o} m_2 (m_1 + m_3) + m_1} \quad (2-48)$$

Note that for a given varactor (specified through ω_c and P_{norm}) and pump frequency ω_o , the large signal performance can be calculated if the values for m_1 , m_2 , and m_3 are known. The modulation ratios are interrelated, bounded by the elastance limits, influenced by the bias voltage, and proportional to the pump power at ω_o . Two external constraints are therefore imposed: (1) the elastance is fully modulated (from S_{max} to S_{min}), and (2) the circuit is optimized for maximum efficiency.

As described in subsection 2.4.1, with the bias voltage set for symmetrical modulation, eqn.(2-32) can be rewritten as

$$\sum_{k=1}^{\infty} m_k \sin(k\omega_o t + \phi) \leq 0.25 \quad (2-49)$$

where the equality is taken if the varactor is pumped for maximum modulation. In the case of the tuned tripler ($\phi = 0$), eqn.(2-49) becomes

$$m_1 \sin(\omega_o t) + m_2 \sin(2\omega_o t) + m_3 \sin(3\omega_o t) = 0.25 \quad (2-50)$$

or

$$m_1 = \frac{1}{\sqrt{1 - \cos^2(\omega_o t)} \left[4 - 4 \frac{m_3}{m_1} + 8 \frac{m_2}{m_1} \cos(\omega_o t) + 16 \frac{m_3}{m_1} \cos^2(\omega_o t) \right]} \quad (2-51)$$

The time t_o which gives rise to a maximum in the modulation waveform can be found by taking the derivative of eqn.(2-50) with respect to time and setting the result equal to zero thus yielding

$$\cos^3(\omega_o t_o) + \frac{1}{3} \frac{m_2}{m_3} \cos^2(\omega_o t_o) + \frac{(m_1 - 9m_3)}{12m_3} \cos(\omega_o t_o) - \frac{m_2}{6m_3} = 0 \quad (2-52)$$

This is a cubic equation which can be placed into the following form:

$$\begin{aligned}
 x^3 + \alpha x + \beta &= 0 \\
 \text{where} \\
 \cos(\omega_o t_o) &= x - \frac{m_2}{9m_3} \\
 \alpha &= \frac{1}{3} \left[\frac{m_1 - 9m_3}{4m_3} - \frac{m_2^2}{9m_3^2} \right] \\
 \beta &= \frac{1}{27} \left[\frac{2}{27} \frac{m_2^3}{m_3^3} - \frac{m_2}{m_3} \left[\frac{m_1 - 9m_3}{4m_3} \right] - 27 \frac{m_2}{6m_3} \right]
 \end{aligned} \tag{2-53}$$

Since the roots are real, x can be found as

$$x = \left[-\frac{\beta}{\alpha} + \sqrt{\frac{\beta^2}{4} + \frac{\alpha^3}{27}} \right]^{-\frac{1}{3}} + \left[-\frac{\beta}{\alpha} - \sqrt{\frac{\beta^2}{4} + \frac{\alpha^3}{27}} \right]^{-\frac{1}{3}} + \frac{m_2}{9m_3} \tag{2-54}$$

Eqns. (2-51), (2-53), and (2-54) together form the **breakdown limit surface** for the tripler in the m_1 , m_2 , and m_3 plane. Under maximum modulation conditions, the operating point lies somewhere on this surface. For lower pump powers and under different biasing conditions, the operating point can be anywhere under the surface.

To solve for a unique operating point, two additional equations are needed. To obtain minimum loss in the second harmonic (idler) circuit, the terminating resistance must be zero. Setting eqn. (2-42) equal to zero yields the second of the three required equations for solution:

$$m_2 = \frac{\omega_c}{4\omega_o} m_1^2 + \frac{\omega_c}{2\omega_o} m_1 m_3 \tag{2-55}$$

This equation forms a second surface in the m_1 , m_2 , and m_3 plane. The intersection of the two surfaces forms a curve on which the desired operating point lies. The operating point could be found from the maximum efficiency condition as in the case of the doubler, however in certain cases, the tripler solution did not converge. Therefore, the solution for

maximum efficiency was found by using eqns.(2-51), (2-53), (2-54), and (2-55) to calculate the efficiency for a range of m_1 values and simply searching for the maximum efficiency point (hence the third equation for solution). The above calculations were performed for a number of varactors having different physical parameters. The results of this performance survey are summarized in Chapter Seven for the 80/240 GHz tripler, and Chapter Eight for the 31/94 GHz tripler. A sample MathCAD file is included in Appendix C.

2.5 The Siegel-Kerr Nonlinear Analysis Program

Use was made of the Siegel-Kerr nonlinear analysis program to confirm the results found by the Penfield and Rafuse approach and to provide a convenient tool for examining the effects of non-optimum bias level, pump power, and embedding impedances on the varactor multiplier performance. Complete details of the theory and use of this program can be found in (Siegel, 1984).

Input to this program includes data about the varactor physical parameters, pump power and frequency, embedding impedances, and bias voltage. The program output includes the port impedances, absorbed pump power, output power, and varactor efficiency. The common program variables used throughout this thesis are as follows:

CONST:		
Q	1.602192D-19	Unit charge
BOLTZ	1.38062D-23	Boltzmann constant
PI	3.14159265358979	Pi
MU	12.56637061435917D-9	Free space permeability
EPS	8.854185336732028D-14	Free space permittivity
TK	300.0	Temperature

DIODE:		
ETA	1.20	Ideality factor
PHI	1.0	Built-in potential
GAM	0.5	Gamma
CO	varactor specific	Zero-biased junction capacitance
IS	1.4D-17	Reverse saturation current
RS	varactor specific	Series Resistance
LS	0.0D-9	NOT USED- SET TO ZERO
FP	varactor specific	Pump frequency
IMPED:		
ZEMBDC	1.0D0	DC path resistance
ZER(1-3)	mult. specific	Embedding resistance - harmonics 1,2,3
ZER(4-6)	0.0	Embedding resistance - harmonics 4,5,6
ZEI(1-3)	mult. specific	Embedding reactance - harmonics 1,2,3
ZEI(4-6)	0.0	Embedding reactance - harmonics 4,5,6
LOOPS:		{Internal program Variables}
NH	6	
NLO	1	
NPTS	51	
NCURR	10	
NVLO	50	
NITER	500	
NPRINT	200	
MULT:		
NIN	1	Input port
NOUT	2 or 3	Output port - 2=doubler, 3=tripler
MLTLOOP:		
NVDC	variable	Number of bias voltages
NPAV	variable	Number of pump power levels
VDCDAT(1-10)	variable	Bias voltages
PAVDAT(1-5)	variable	Available pump powers
RES:		
ER	13.1	Dielectric constant
NDS	4.0D18	n_d for buffer layer
NDE	2.5D16	n_d for active layer
SMOB	5.5D3	Electron mobility in buffer layer
EMOB	5.5D3	Electron mobility in active layer
TE	varactor specific	Thickness of active layer
AR	varactor specific	Anode radius
CL	30.0D-4	Ohmic contact length - {nominal}
CW	30.0D-4	Ohmic contact width - {nominal}
CT	5.5D-4	Buffer layer thickness
RC	1.0	Ohmic contact resistance
RKG:		{Internal program variables}
VDINIT	0.0	
ACC	1.0D-6	
NDIM	1	
TLINE:		{Internal program variables}
Z0	50.0	
ZQACC	0.01	

2.6 Conclusions

The Schottky diode capacitance-voltage (C-V) characteristics and resistive loss were derived in this chapter. The varactor characteristics were used together with the large-signal nonlinear analysis (including the embedding-circuitry and bias voltage) to yield equations that predict the performance of the varactor frequency doubler and tripler. The Siegel-Kerr nonlinear analysis program was also introduced. These analytical tools will be used to predict the performance of the frequency multipliers described in Chapters Three, Six, Seven, and Eight.

CHAPTER THREE

Direct Replacement of a Whisker-Contacted Varactor with a Planar Varactor

3.1 Introduction

The grand challenge currently facing millimeter-wave researchers is the introduction of planar technology into the present realm of the whisker-contact. The motivation behind such work is the high reliability and low cost requirements of LO systems for ground-based radio imaging arrays and for space applications. The whisker-contact technology fails to meet such requirements because of the mechanically unstable whisker/anode contact. The mounting of such diodes into a millimeter-wave fixture (also known as a block or mount) is a very tedious task which requires highly specialized personal and rather high costs. Furthermore, the cost of space-qualifying such whisker-contacted components is enormous; and the resulting product is still of questionable reliability. The mechanical ruggedness and potentially superior performance of the planar structure makes this approach a more attractive alternative.

Despite this mechanical advantage, the electrical nature of the planar structure differs greatly from that of the whisker-contacted structure and hence issues regarding high-frequency operation are raised. Past efforts have shown that planar varactors can be used up to 300 GHz in specially designed mounts, however results were generally poor compared with the whisker-contacted counterpart in a different fixture. What is lacking is simply a direct performance comparison of a planar and whisker-contacted varactor in the same mount. This chapter presents the details

of an experimental study used to gain insight into the behavior of a planar varactor diode in a frequency tripler designed for whisker-contacting. The limitations of such discrete planar varactor circuits are also discussed.

3.2 The 75/225 GHz Tripler

The multiplier circuit chosen for this study is a 75/225 GHz frequency tripler designed by J. Archer for use at the National Radio Astronomy Observatory (Archer, 1984). This choice was made primarily because of the multiplier's availability and its proven, well-documented performance. It is currently the mainstay multiplier used in 200-290 GHz millimeter-wave LO systems at NRAO.

The circuit was designed around a 6 μm anode-diameter whisker-contacted varactor diode (5M2) fabricated at the Semiconductor Device Laboratory, University of Virginia (UVA). As shown schematically in Fig. 3.1, this diode is mounted across a reduced height output waveguide; the anode is attached to ground via the whisker wire, and the cathode (entire chip) is attached to the quartz-substrate suspended stripline. This stripline contains a low-pass filter with a 3 dB cutoff frequency at 130 GHz, and an E-plane probe into the input WR-12 waveguide. The input circuit has two degrees of freedom; one provided by the series E-plane adjustable shorting stub, and the second provided by the adjustable shorting stub (backshort) adjacent to the stripline probe. This facilitates the matching of the guide impedance to a wide range of impedances at the input of the low-pass filter. The output waveguide is coupled to the reduced-height guide via a two-section quarter-wave

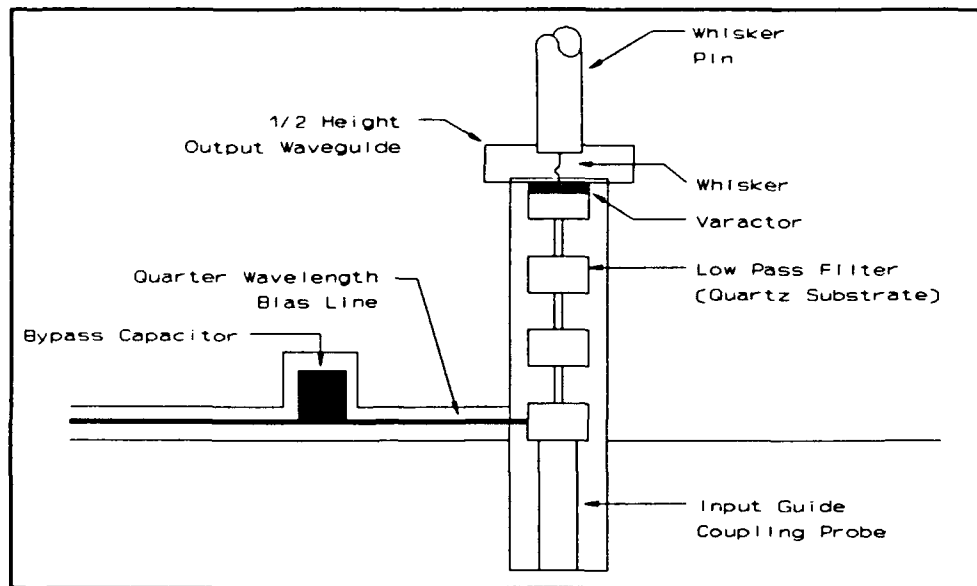


Figure 3.1 Sketch of the 75/225 GHz tripler showing the diode, input and output waveguide, and biasing circuit.

impedance transformer. This permits second-harmonic power to propagate in the wider guide (near the varactor), whereas the output waveguide is cutoff at this frequency. The transformer is thus used to implement a second harmonic reactive termination that is positioned approximately $\lambda_g/2$ (at the 2nd harmonic) from the plane of the diode. Second and third harmonic tuning is provided by a sliding backshort on the opposite side of the diode from the output waveguide. Finally, the DC bias circuit is isolated from the suspended stripline via a quarter-wavelength section of coaxial line which is attached to a large capacitor. This capacitor provides an RF short to ground which is transformed to an open at the stripline/coaxial line junction.

3.3 The UVA Planar Varactor Diode

The excellent fabrication work on the UVA planar varactor was done by M.S. student H. Dossal, hence details of the fabrication procedure are described in his thesis (Dossal, 1991) and are not presented here, however the varactor parameter specifications and mask drawings were done as part of this thesis. Mask plates were fabricated by L. Poli at the US Army Electronic Technology and Devices Laboratory, Ft. Monmouth, NJ. This prototype mask set consists of five plates which permit rectangular and tapered ohmic contact and anode contact pads, circular anodes of 4, 5, 6, and 9 microns, and finger lengths of 13, 25 and 50 microns. Also included are surface channel details, option for back-side etching, and solder pads. Appendix D contains a summary of the physical dimensions for this mask set. The mask plates are directly compatible with the prototype planar mixer diode mask set (MIXER-1) designed by W. Bishop (UVA). Over 300 geometrically identical varactors are fabricated per "batch", with overall varactor size being 10 mils in length by 5 mils in width.

Originally, the varactors were fabricated on a semi-insulating (SI) GaAs substrate, but recently a substrate removal process developed at UVA (Bishop, 1990) was applied; the SI GaAs was successfully removed and quartz was substituted in an attempt to reduce the shunt capacitance. Fig. 3.2 shows the details of a quartz-backed UVA planar varactor.

The three types of diodes examined in this study include the original whisker-contacted 5M2, the SI GaAs substrate planar, and the quartz substrate planar varactors. Physical and electrical characteristics for all three diodes are presented in Table 3.1.

TABLE 3.1 Discrete Varactor Diodes - Measured Data			
Characteristic	Whisker 5M2	Planar SI GaAs	Planar Quartz
Doping Profile	Abrupt	Abrupt	Abrupt
n ⁻ doping	$3.5 \times 10^{16} \text{ cm}^{-3}$	$1.1 \times 10^{17} \text{ cm}^{-3}$	$8.5 \times 10^{16} \text{ cm}^{-3}$
n ⁻ thickness	1 μm	0.45 μm	0.51 μm
n ⁺ doping	$> 2 \times 10^{18} \text{ cm}^{-3}$	$> 2 \times 10^{18} \text{ cm}^{-3}$	$> 2 \times 10^{18} \text{ cm}^{-3}$
n ⁺ thickness	125 μm	5 μm	5 μm
Anode diameter	6 μm	7 μm	7 μm
Size L x W x H	5 x 5 x 3 mils	10 x 5 x 2 mils	10 x 5 x 2 mils
Gamma *	0.5	0.5	0.5
Eta *	~1.1	~1.1	~1.1
R _s *	10 ohms	3 ohms	(3 ohms)
C _{jo} *	21.5 fF	38 fF	40 fF
V _{br} *	12 - 15 v	10 v	11 v

* Measurements made by H. Dossal

The series resistance for the quartz-backed planar varactor is an estimate based on measurements of the SI GaAs-backed varactor. The conventional method of measuring the series resistance (using dc currents) caused significant heating of the junction and a subsequent increase in junction temperature. The heating is attributed to the lower thermal conductivity, k , of the quartz ($k_q = 0.017 \text{ W/mK}$) compared with GaAs ($k_s = 0.46 \text{ W/mK}$) which is 27 times larger (Hoffmann, 1987). The change in junction temperature with current will result in a deceptively lower value for the series resistance.

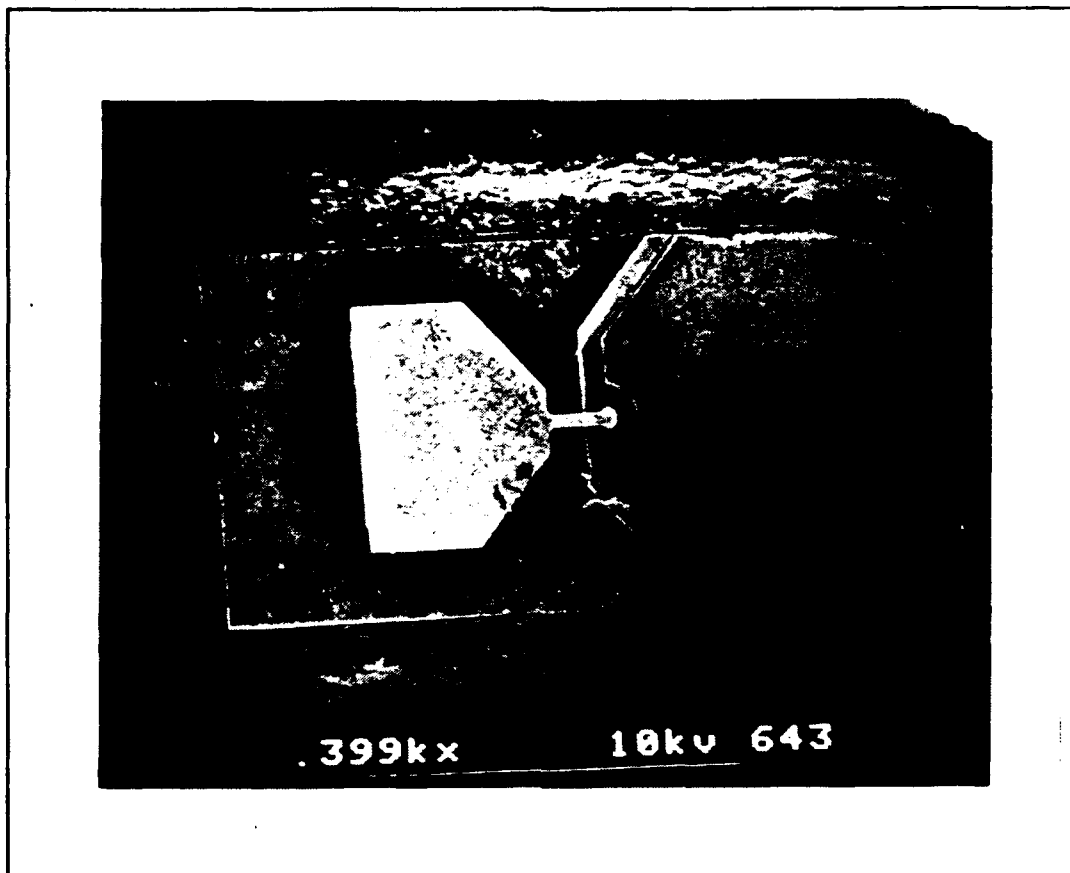


Figure 3.2 Scanning electron micrograph (400x) of the UVA planar varactor on a quartz substrate (H. Dossal).

3.4 Theoretical Tripler Performance

The following multiplier performance analysis was based on the procedure described in Chapter Two. Using the measured varactor data in Table 3.1, the tripler input and output power, input, idler, and output impedances, and varactor efficiency were calculated for 71/213 GHz and 81/243 GHz operation. These calculations are summarized in Table 3.2.

The abrupt-junction Schottky-barrier varactor is the elemental nonlinear device of this study. For a given varactor, the varactor efficiency presented in Table 3.2 provides an upper bound on the expected

TABLE 3.2 Theoretical Tripler Performance							
VARACTOR	OUTPUT FREQUENCY [GHz]	INPUT POWER [mW]	OUTPUT POWER [mW]	VARACTOR EFF. [percent]	INPUT IMPEDANCE [ohms]	IDLER IMPEDANCE [ohms]	OUTPUT IMPEDANCE [ohms]
5M2 WHISKERED	213	28.2	17.0	60	102 - j407	0 - j203	46 - j136
	243	32.9	18.6	56	92 - j357	0 - j178	43 - j119
SI GaAs PLANAR	213	23.8	14.8	62	30 - j117	0 - j 58	13 - j 38
	243	27.7	16.2	58	27 - j102	0 - j 51	12 - j 34
Quartz PLANAR	213	23.4	15.4	66	43 - j148	0 - j 74	25 - j 49
	243	29.1	18.7	64	31 - j130	0 - j 65	11 - j 43

overall multiplier efficiency, however resistive losses in the input, idler, and output circuits as well as non-optimum embedding impedances at the harmonics will substantially lower output power and efficiency. The data of Table 3.2 does not include the effects of the parasitic elements.

Analysis of the electrical nature of the multiplier must encompass not only the Schottky-barrier and series resistance, but also the varactor supporting substrate, i.e. the device package. Fig. 3.3 shows an equivalent circuit for the UVA whisker-contacted and planar varactors which includes the series inductance (L_f), the current spreading inductance (L_{buff}), and the shunt capacitance (C_p).

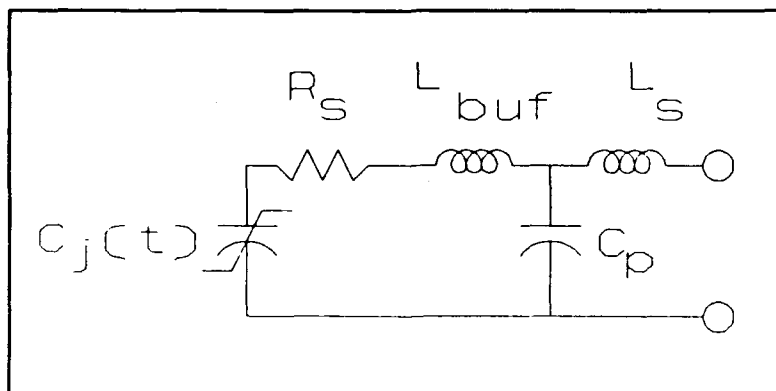


Figure 3.3 Equivalent circuit of the varactor and package.

Since the basic physics of the Schottky contact is the same in both structures, the capacitance-voltage and current-voltage relations are very similar for a given anode diameter and n^- layer doping and thickness. However, due to the geometrical configuration, the magnitudes of the parasitic elements associated with each structure are somewhat different. The most critical parasitic elements of both configurations are the shunt capacitance across the Schottky contact and the series inductance identified with the whisker wire or the contact finger. A schematic of the "pumped" varactor frequency multiplier is shown in Fig. 3.4.

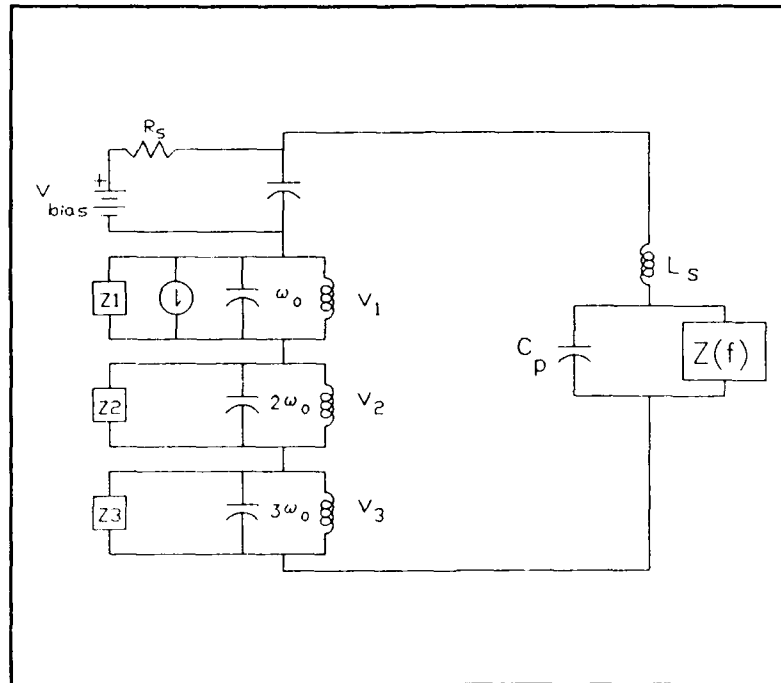


Figure 3.4 Equivalent circuit of a "pumped" varactor frequency tripler.

$Z(\omega)$ is the impedance at each harmonic as shown in Table 3.2, and Z_1 , Z_2 , and Z_3 are the embedding impedances at each harmonic.

The whisker structure has a very low shunt capacitance, C_f , (1 fF or less) but the planar diode structure has about 10 to 12 fF (Newman, 1989).

This shunt capacitance can be detrimental to multiplier operation since at 250 GHz the associated reactance is 630Ω for 1 fF but only 63Ω for 10 fF. This reactance is across $Z(\omega)$ (NOT C_j and R_s) and tends to increase the effective C_{avg} and decrease the real part of $Z(\omega)$ as seen by the embedding circuitry. Since the diode is mounted across a waveguide, the reactance can be parallel resonated at each output frequency by an adjustable backshort (sliding short circuit), however this is not the case for the input circuit.

The series inductance of the whisker/finger, L_f , is a useful parasitic element because it partially compensates for C_{avg} . The typical whisker inductance is around 0.3 nH compared with the finger inductance of around 0.02 nH (Newman, 1989), an order of magnitude smaller. However, note from Table 3.2 that the harmonic reactances of the planar varactors are also smaller.

3.5 Multiplier Mount Modifications

The NRAO tripler mount was only slightly modified to accommodate the UVA planar varactor. Fig. 3.5 shows a sketch of the modified region. To support the planar diode across the output waveguide, a flat surface was milled on the side of the whisker post such that this surface is in the plane of the top side of the quartz stripline substrate. This was done using a jig designed by P. Siegel for a similar task with planar mixer diodes. The distance between this flat surface and the mating surface of the mounting block is 3 mils, hence the varactor height had to be lapped to about 2 mils to allow adequate space for solder. Both the modified whisker post and the suspended stripline jut into the reduced

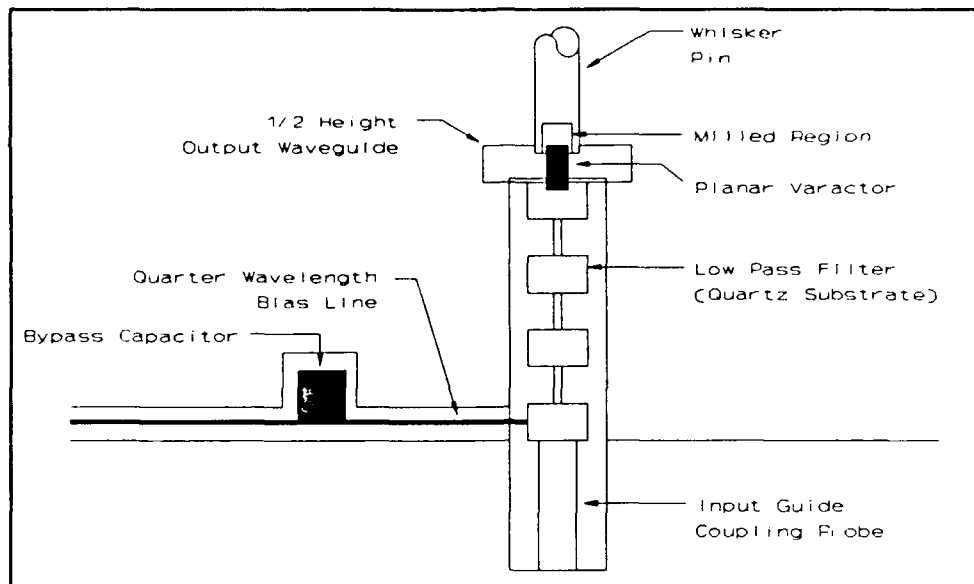


Figure 3.5 Sketch of modified region of the NRAO 75/225 GHz Tripler.

height waveguide by about 1 mil each, yielding approximately 2.5 mils overlap for soldering each diode pad. Originally, the whisker-contacted varactor was mounted to the quartz stripline prior to mounting the stripline into the channel. However in the planar case, each test diode is soldered to the modified whisker post and stripline using B20E2 solder with SuperSafe flux AFTER the stripline is mounted in the channel. Because the entire block must be heated to above 120 degrees centigrade to perform the soldering, the adhesive used in holding the quartz stripline was changed from Eccobond 910 to Sears Epoxy which remains solid at that temperature. The expertise required for this delicate soldering operation was cordially provided by N. Horner at NRAO.

Fig. 3.6 is a scanning electron micrograph of the whisker-contacted varactor diode in the tripler mount. In contrast, Fig. 3.7 is an optical photograph of the new quartz planar varactor mounted across the output waveguide of the modified mount.

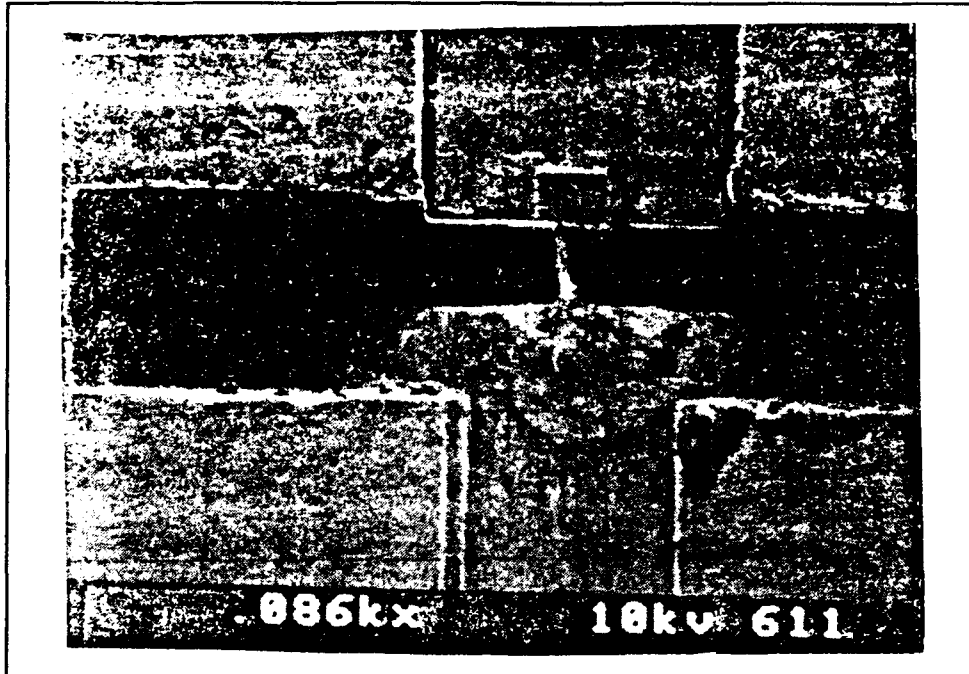


Figure 3.6 Electron micrograph (86x) of the whisker and varactor diode in the conventional 75/225 GHz NRAO tripler mount.

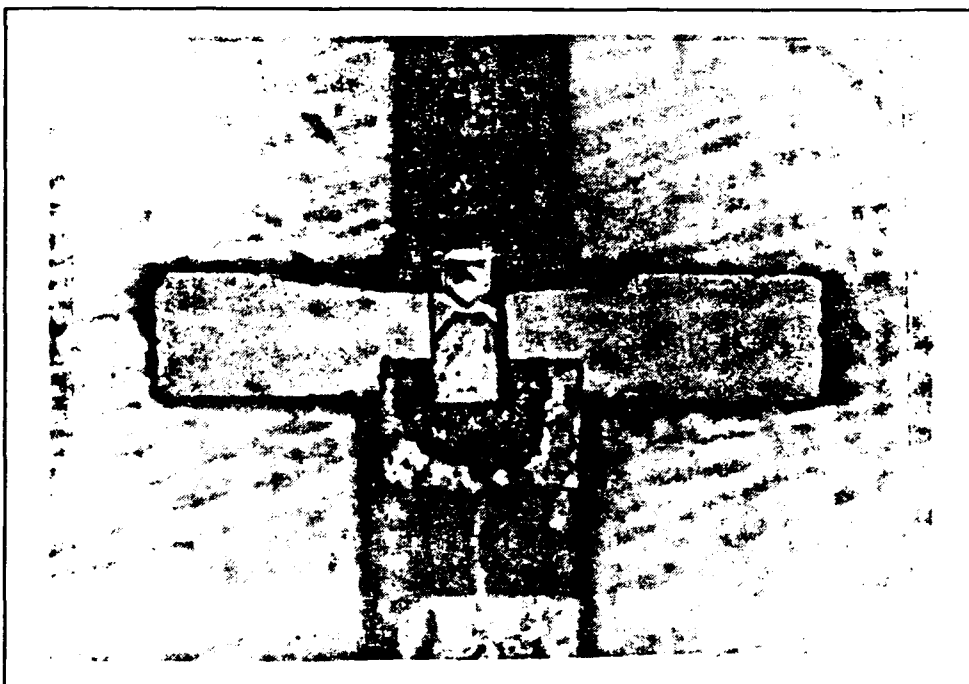


Figure 3.7 Photograph (50x) of the new quartz-backed planar varactor in the NRAO 75/225 GHz tripler. Chip metal is visible through the quartz substrate.

Both orientations of the planar diode were investigated, i.e. 1) anode pad to whisker post and 2) anode pad to stripline. Each diode under test was mounted as described and the remaining block assembly was completed. The tripler performance was measured using the test setup described in the next section.

3.6 Test Setup and Measuring Procedure

The performance of the frequency triplers was evaluated by three types of measurements: 1) Output power as a function of frequency, 2) output power versus input power, and 3) input return loss as a function of frequency. This section contains a description of the test setups and the corresponding measurement procedure.

3.6.1 Output power versus frequency

Of primary interest for all frequency multipliers is the amount of power that can be produced and delivered to a matched load at the output frequency. The test setup used to evaluate this quantity is shown schematically in Fig. 3.8. The input power source is a mechanically-tuned klystron which covers the frequency range from 73 to 81 GHz. The amount of multiplier input power is controlled by the adjustable waveguide attenuator. The three position switch is a convenience which allows: 1) measurement of input frequency via the absorption-type frequency meter together with an uncalibrated detector, 2) measurement of input power via the calibrated detector, or 3) direction of power to the input port of the frequency multiplier under evaluation. To equalize resistive losses, geometrically similar waveguides are used in the power meter and

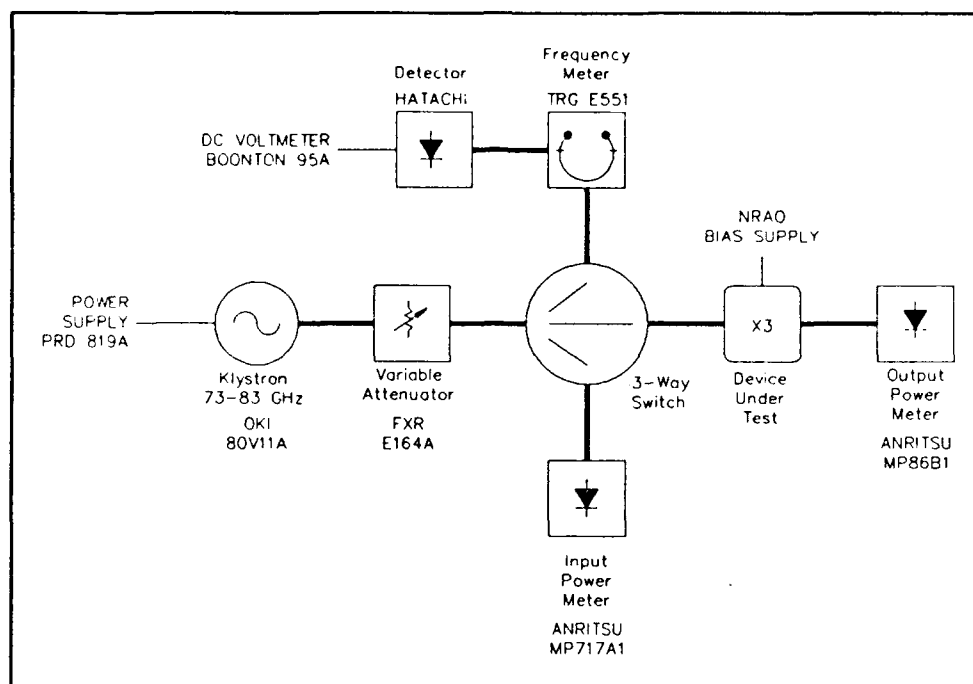


Figure 3.8 The test setup used for measuring output power as a function of frequency and input power.

frequency multiplier paths such that the measured power is within 1% of the power actually delivered to the multiplier input port. The multiplier output power is measured using an additional calibrated detector. The DC bias to the varactor is supplied by a precision current/voltage source designed and built by NRAO.

The measurement procedure is as follows: The klystron, with 2500 volts applied to the beam, is allowed to establish operation equilibrium for at least 30 minutes prior to any measurements. With a stable klystron, the adjustable attenuator is set to maximum attenuation and the 3-position switch set for frequency measurement. The attenuation is decreased until the current through the uncalibrated detector measures 5 to 10 nA. To set the klystron to the desired operating frequency, the mechanical tuning is slowly adjusted while oscillation is maintained via

adjustment of the klystron reflector voltage. The frequency is periodically checked using the frequency meter until the desired frequency is achieved. The reflector voltage is then carefully adjusted for maximum output power.

Once the klystron is adjusted to the desired frequency, the 3-position switch is moved to measure the power. The attenuation is decreased until 50 mW is achieved. The output power is measured over a few minutes period to detect any drift in power caused by inadequate klystron tuning. If drift is detected, the reflector voltage is adjusted, even to another klystron mode if needed. If the system is determined to be sufficiently stable, the power is then directed to the multiplier under test.

The varactor is initially biased near zero volts and the input sliding shorts are adjusted until some bias current is detected, indicating input RF power present at the varactor. The output sliding short is then adjusted for maximum output power. Then the bias voltage and input tuning are further adjusted (as well as small adjustments to the output tuning) until maximum possible output power is achieved.

Once the maximum power point for a given frequency is determined, the output power, the multiplier tuner positions, and the bias voltage and current are recorded. The adjustable attenuator is then set to maximum and the measurement is complete. The above procedure was performed over the frequency range from 71 to 81 GHz, in 1 GHz steps.

Unwanted forth-harmonic superimposed on the desired third-harmonic in the tripler output will result in a third-harmonic power measurement error. To check for the presence of forth-harmonic (under worst-case

conditions), various lengths of WR-3 waveguide followed by a waveguide that is cutoff at 280 GHz was inserted between the tripler output port and the power meter. This provides a reactive termination (phase was varied by adjusting the length of WR-3 waveguide) for the third-harmonic but allows the forth-harmonic to reach the power meter. The result of this experiment showed that forth-harmonic power is negligible in comparison with the third-harmonic power at the output of the tripler.

3.6.2 Output Power Versus Input Power

It is of interest to examine the multiplier behavior as a function of input power. As determined from the output power versus frequency measurements, the frequency that yielded maximum output power is chosen for the current experiment. The same test setup as described in Subsection 3.6.1 is used here. Once the klystron is set to the desired frequency, the switch is positioned to measure input power, which is varied from 10 to 70 mW in steps of 10 mW via the variable attenuator. Finally, the input power is directed to the tripler under test. The tuning procedure and recorded data are the same as in the previous measurement.

3.6.3 Input Return Loss versus Frequency

The match of the input circuit and a first order estimate of the input circuit resistive loss is determined by measuring the "pumped" input return loss. With 50 mW of power at the tripler input port, the input return loss was measured as a function of frequency from 73 to 81 GHz. The modified test setup is shown in Fig. 3.9. A -10 dB waveguide directional coupler, with directivity of better than 35 dB, is inserted

into the input line as shown. The klystron is set to the desired frequency as described in Subsection 3.6.1. The power meter is first placed at the end of the directional coupler "through" port (point A, Fig. 3.9) to measure the power at the input of the tripler. This power level is set to 50 mW using the adjustable attenuator. To establish a reference plane, the power meter is then moved to the directional coupler side arm and this reflected power is recorded when a shorting plate is placed at the tripler input port.

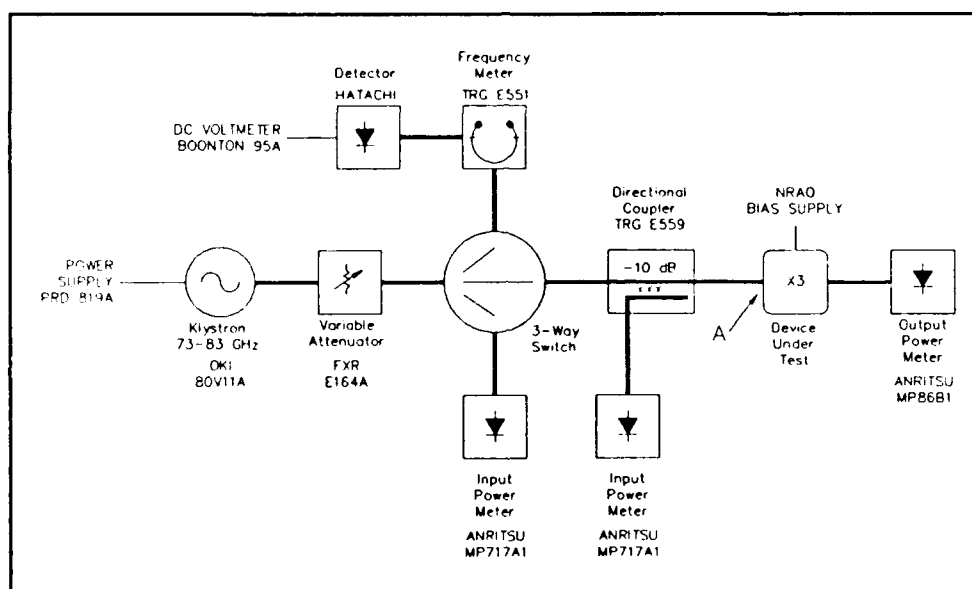


Figure 3.9 The test setup for measuring input return loss (RL) of the frequency tripler.

The dynamic range of the measurement, which is better than -23 dB, was checked only once by replacing the shorting plate with a matched waveguide termination, with the minimum detectable power taken to be 20 μ W since the accuracy of the power meter is questionable below this level due to circuit drift and unwanted noise. Finally, the shorting plate is removed and the tripler under test is connected to the directional coupler and a power meter is connected to the tripler output port. The tripler tuning

stubs and bias are adjusted (using the data of Subsection 3.6.1) for maximum output power, and the reflected power is recorded. The input return loss (RL_I) is calculated as follows:

$$RL_I = -10 \text{LOG} \frac{\text{DUT Reflected Power}}{\text{Shorting Plate Reflected Power}} \quad (3-1)$$

3.7 RF Measurement Results

The frequency multiplier test data are presented in this section. With fixed input power, the data includes measurements of output power, efficiency, and input return loss as a function of frequency. Furthermore, with fixed input frequency, the output power and efficiency are presented as a function of input power. Data were collected for SI GaAs substrate planar Schottky, quartz substrate planar Schottky, and GaAs whiskered Schottky varactors mounted in the NRAO tripler block. The efficiency presented here is multiplier efficiency, η_m , which is defined as follows:

$$\eta_m = \frac{\text{Power measured at output port}}{\text{Available power at input port}} \times 100 \quad (3-2)$$

Note that both power levels are measured at the ports of the multiplier block.

Table 3.3 summarizes the output power versus frequency measurements for the NRAO tripler block incorporating both planar and whisker-contacted Schottky diodes. The output power as a function of input power is presented in Table 3.4.

TABLE 3.3 Tripler Performance Summary
Output Power versus Frequency
50 mW input

Diode, Substrate, Mount	Input Freq. [GHz]	Output Freq. [GHz]	Output Power [mW]	Multiplier Efficiency [%]	Bias		Input RL [dB]
					V [volts]	I [mA]	
PLANAR 5,d Quartz T12	71	213	0.58	1.2	-4.041	1.91	
	72	216	0.80	1.6	-4.010	2.01	
	73	219	1.61	3.2	-3.925	0.94	-14.2
	74	222	0.95	1.9	-3.121	1.71	-18.8
	75	225	1.06	2.1	-4.312	1.01	-13.7
	76	228	0.57	1.1	-2.933	0.98	-17.5
	77	231	0.57	1.1	-3.433	0.61	-14.4
	78	234	0.24	0.5	-3.217	0.37	- 6.4
	79	237	0.17	0.3	-3.100	0.72	- 4.1
	80	240	0.14	0.3	-2.422	1.20	- 7.2
	81	243	0.12	0.2	-3.057	0.52	-12.4
PLANAR 5,c Quartz T12	73	219	1.99	4.0	-4.236	0.66	
	74	222	1.24	2.5	-3.183	1.48	
	75	225	1.08	2.2	-3.156	3.47	
	76	228	0.95	1.9	-2.925	1.05	
	77	231	0.59	1.2	-3.690	0.43	
	78	234	0.22	0.4	-3.544	0.01	
	79	237	0.17	0.3	-1.720	1.72	
	80	240	0.18	0.4	-2.278	0.81	
	81	243	0.24	0.5	-3.283	0.62	
PLANAR 5,f Quartz T12 Polarity Reversed	71	213	0.83	1.7	-5.130	1.55	
	72	216	1.29	2.6	-4.963	1.47	
	73	219	1.88	3.8	-4.565	0.27	
	74	222	0.76	1.5	-4.400	0.52	
	75	225	1.33	2.7	-4.806	0.47	
	76	228	0.54	1.1	-3.645	0.73	
	77	231	0.74	1.5	-3.580	0.90	
	78	234	0.26	0.5	-3.557	0.89	
	79	237	0.14	0.3	-4.542	0.00	
PLANAR 2,c SI GaAs T12	73	219	1.66	3.3	-3.330	1.02	-14.3
	74	222	0.89	1.8	-2.940	1.50	-17.9
	75	225	0.98	2.0	-3.420	1.01	-16.1
	76	228	0.58	1.2	-3.030	0.17	-25.0
	77	231	0.29	0.6	-2.980	0.17	- 7.7
	78	234	0.12	0.3	-2.580	0.09	- 3.8
	79	237	0.17	0.4	-2.150	1.49	- 9.4
	80	240	0.13	0.3	-2.210	0.42	-15.0
	81	243	0.07	0.1	-2.130	0.17	-15.8
PLANAR 3,a SI GaAs T17	73	219	0.96	1.9	-3.337	0.42	
	74	222	0.77	1.5	-3.124	0.17	
	75	225	0.89	1.8	-4.107	0.32	
	76	228	0.15	0.3	-4.617	0.00	
	77	231	0.08	0.2	-1.581	0.84	
	78	234	0.19	0.4	-2.624	0.84	
	79	237	0.27	0.5	-2.512	0.84	
	80	240	0.08	0.2	-2.946	0.84	

TABLE 3.3 Tripler Performance Summary
Output Power versus Frequency
50 mW input

Diode, Substrate, Mount	Input Freq. [GHz]	Output Freq. [GHz]	Output Power [mW]	Multiplier Efficiency [%]	Bias		Input RL [dB]
					V [volts]	I [mA]	
WHISKERED SM2 GaAs T13	73	219	1.84	3.7	-3.421	3.52	-17.5
	74	222	1.18	2.4	-3.132	4.57	-18.9
	75	225	1.48	3.0	-4.657	2.06	-18.6
	76	228	1.56	3.1	-3.920	2.73	-18.7
	77	231	1.56	3.1	-3.686	3.35	-13.2
	78	234	2.07	4.1	-3.362	3.14	-18.4
	79	237	1.88	3.8	-3.704	1.61	-16.0
	80	240	1.72	3.4	-3.775	0.63	-19.0
	81	243	1.12	2.2	-3.614	0.72	-19.1

TABLE 3.4 Tripler Performance Summary
Output Power versus Input Power

Diode, Substrate, Mount	Input Freq. [GHz]	Output Freq. [GHz]	Input Power [mW]	Output Power [mW]	Multiplier Efficiency [%]	Bias	
						V [volts]	I [mA]
PLANAR 5,f Quartz T12	73	219	10	0.12	1.2	-2.125	0.00
			20	0.54	2.7	-2.231	0.35
			30	0.94	3.1	-3.336	0.32
			40	1.34	3.4	-4.295	0.28
			50	1.72	3.4	-4.546	0.62
			60	2.05	3.4	-5.132	0.94
			70	2.35	3.4	-5.527	1.15
			80	2.63	3.3	-5.631	1.88
PLANAR 2,c SI GaAs T12	73	219	10	0.18	1.8	-0.895	0.06
			20	0.55	2.8	-1.260	0.65
			30	0.99	3.3	-2.036	0.65
			40	1.30	3.3	-1.950	2.36
			50	1.74	3.5	-2.500	2.66
			60	2.16	3.6	-2.680	2.36
			70	2.72	3.9	-3.410	1.53
			80	3.34	4.2	-3.930	1.95
PLANAR 3,a SI GaAs T17	75	225	30	0.15	0.5	-3.394	0.00
			40	0.26	0.7	-4.061	0.00
			50	0.42	0.9	-4.594	0.00
			60	0.64	1.1	-4.904	0.00
			70	0.81	1.2	-4.816	0.04
			80	1.04	1.3	-5.590	0.04
			90	1.21	1.3	-5.690	0.06
			100	1.47	1.5	-5.990	0.06
WHISKERED 5M2 GaAs T13	78	234	10	0.35	3.5	-0.949	0.28
			20	0.84	4.3	-1.958	0.82
			30	1.18	3.9	-2.361	1.51
			40	1.47	3.7	-2.761	2.19
			50	1.81	3.6	-3.059	2.70
			60	2.05	3.4	-2.898	3.76
			70	2.22	3.2	-3.347	3.54

Fig. 3.10 is a graph of the output power as a function of frequency for six NRAO block triplers including both planar and whiskered varactors. The whisker-contacted tripler data is from (Bailey, 1990). These data are also included in Chapter One and in Appendix B. A discussion of the tripler performance is presented in the next section.

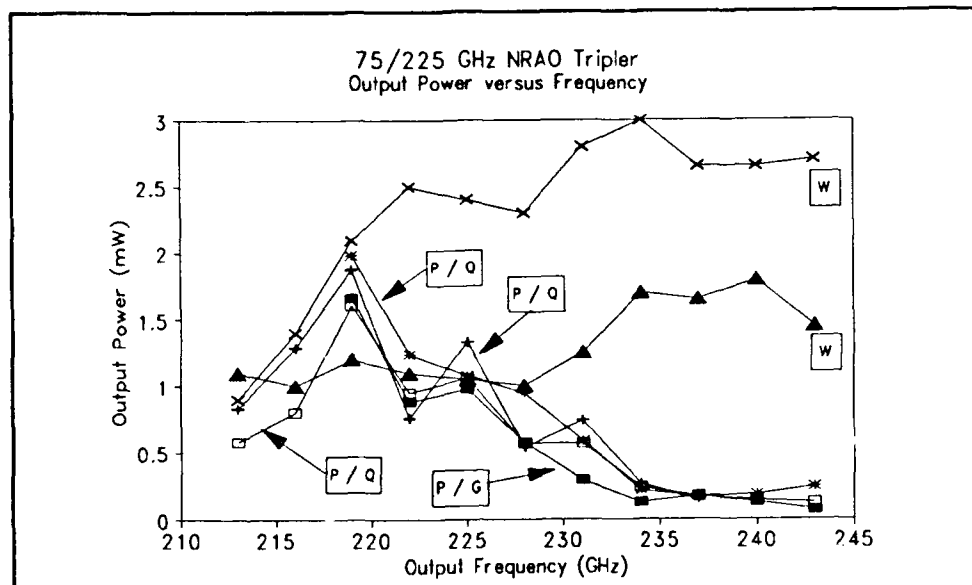


Figure 3.10 Output power versus frequency for a number of planar quartz (P/Q), planar SI GaAs (P/G), and whiskered (W) Schottky varactors in the NRAO tripler block. ($P_{in} = 50$ mW).

3.8 Discussion

The purpose of this study was to compare directly the performance of a planar and a whisker-contacted frequency multiplier. From the measurement data, it is encouraging that the best output power and multiplier efficiency is similar for the two varactor geometries. However, upon closer scrutiny, there appear a number of very important differences:

Narrow Tuning Bandwidth

One such difference is the much narrower tuning bandwidth of the planar circuit (see Table 3.3). At the lower frequency end, the input return loss measurements correlate well with the output power curve, hence it is reasonable to suggest that the input circuit mismatch strongly affects the performance at such frequencies. The input tuners (sliding shorts) are positioned at a distance from the varactor, thus it is plausible that the input cannot be tuned properly over a wide frequency range due to the large C_p .

However, at the higher frequency end, this is certainly not the case. The non-optimum embedding impedances of the idler and output are probably the cause of the poor performance. Because the zero-biased capacitance of the planar varactors is larger than for the 5M2 varactor (the planar varactor anode was made slightly oversized during fabrication) it is expected that the bias point should get progressively more negative with increasing frequency (reducing the junction capacitance in an attempt to compensate), but this was not observed.

The presence of a large shunt capacitance associated with the planar structures (specifically the high permittivity substrate material) would explain this observation. This is further supported by the slightly wider tuning bandwidth of the quartz substrate planar varactors. It is important to note that the wide tuning bandwidth of the whisker-contacted tripler is a result of many years of empirical optimized of the circuitry near the varactor.

Lower Operating Frequency

The operating frequency of the planar varactor is shifted downward as compared with the whisker-contacted counterpart. This is consistent with the extra junction capacitance as well as the presence of unwanted shunt capacitance, which also has the effect of raising the average capacitance of the varactor.

Another factor contributing of the lower operating frequency is the lack of adequate series inductance for partially resonating the reactance of the varactor diode junction. To the embedding circuits at the harmonic frequencies, the varactor capacitance appears to be slightly larger, and hence to compensate for this effect, the "best" operating point will be shifted lower.

Tripler Performance Very Sensitive to Tuner Positions

The unwanted shunt capacitance can be more easily resonated in the output circuit by the admittance of the output backshort which is adjacent to the varactor. However, because this capacitance presents a very low reactance in the output circuit, tuning points will be very sharp and difficult to achieve. This is enhanced by the fact that the output tuner affects the second-harmonic circuit. The sharp tuning effect was observed when measuring the planar varactor triplers.

Other observations

The decreasing efficiency with increasing input power over 20 mW for the whisker-contacted varactor (see Table 3.4) is predicted by theory (see Table 3.2). However, the planar varactors appear to reach maximum efficiency at very high input power levels. Since resistive losses (other than the series resistance) are assumed to be the same in both cases, the

efficiency versus power behavior for the planar varactor suggests non-optimum embedding impedances.

Planar quartz varactor (5,f) was purposely mounted in reverse, i.e. with the cathode grounded. This orientation shows a only slight alteration in performance, specifically at the high frequency end of the band, but this is not clear since this reduction may be a result of other factors such as the state of the backshorts during the measurements.

Original Design Limitations

Finally, an overview of the entire tripler design reveals a few serious limitations. First, the contacting shorting stubs, especially in the output circuit, are very unreliable and tend to deteriorate with use. As this happens, the output power level begins to fluctuate wildly as a function of tuner position and reproducibility is nearly impossible. This is the major source of error in the above measurements. Second, the second and third harmonic circuits are not well isolated. Independent tuning, especially in the idler loop, is not possible, e.g. the backshort in the output circuit also affects the idler circuit. Third, the input tuning is at some distance from the varactor hence certain diode shunting reactance in the input circuit may be difficult to tune.

3.9 Conclusions

The output power and efficiency of the millimeter-wave planar varactors are comparable to whisker-contacted varactors, however the narrow tuning range reduces the usefulness of this "direct replacement" tripler design. The larger shunt capacitance of the planar varactor lowers the operating frequency, reduces the tuning range, and increases

the tuner sensitivity. A better approach to harmonic separation is desirable. The three adjustable backshorts should be eliminated to improve reliability. Such issues motivate the integration of the varactor and the embedding circuitry. These topics are addressed in Chapters Four and Five.

CHAPTER FOUR

Multiple-Varactor Frequency Multiplier Circuits

4.1 Introduction

This section describes two, three, and four terminal configurations for multiple-varactor interconnections. The merits of each configuration are listed and single-varactor equivalent circuits are developed so that the analysis in Sections 2.4 and 2.5 may be applied. A planar realization of each circuit is also presented. In the subsequent analysis, the varactor is schematically presented as a Schottky diode, thus explicitly showing the varactor's inherent polar nature.

4.2 Circuit Fundamentals

Before analyzing the multiple-varactor configurations, two circuit definitions are necessary. These are shown in Fig. 4.1.

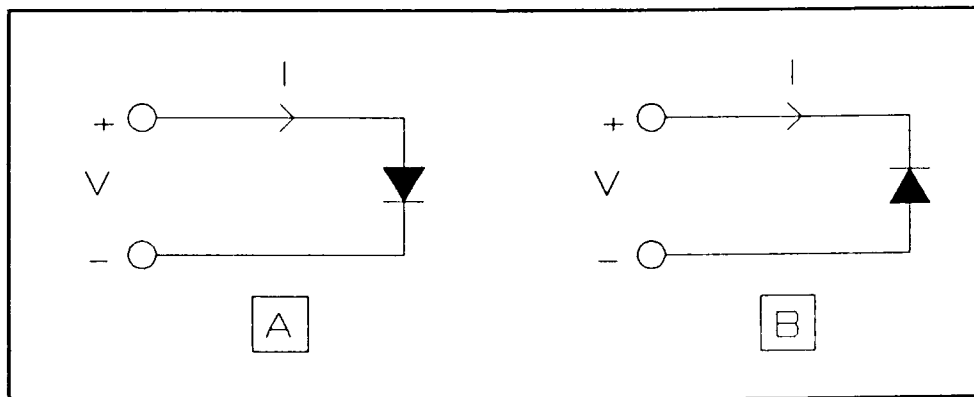


Figure 4.1 Two principle circuit configurations used in the multiple-varactor analysis.

In both circuits, the circuit element is the intrinsic Schottky-barrier junction excluding series resistance. The voltage-charge relation for the

varactor given by eqn. (2-3) can be represented as a power series

$$Q(V) = a_1 V + a_2 V^2 + a_3 V^3 + a_4 V^4 + \dots \quad (4-1)$$

where a_1 , a_2 , a_3 , etc are constants. For the circuit in Fig. 4.1a, the current-voltage relation is

$$I = \frac{dQ}{dt} = [a_1 + 2a_2 V + 3a_3 V^2 + 4a_4 V^3 + \dots] \frac{dV}{dt} \quad (4-2)$$

In the frequency multiplier circuit, the voltage $V(t)$ will be of the form:

$$V(t) = \sum_{k=-\infty}^{\infty} V_k e^{jk\omega_0 t} \quad (4-3)$$

as in eqn. (2-15). This equation is cumbersome to analyze using the power series approach, however for purposes of illustration, assume the diode voltage contains a single harmonic of the form $V(t) = \sin(k\omega_0 t)$. Substitution into eqn. (4-2) yields

$$I(t) = b_1 \cos(k\omega_0 t) + b_2 \sin(2k\omega_0 t) + b_3 \cos(3k\omega_0 t) + \dots \quad (4-4)$$

where the sign of each frequency term is positive. Note that when k is odd, $I(t)$ contains both even and odd harmonics, but when k is even, $I(t)$ contains only even harmonics. This also holds if $V(t) = \cos(k\omega_0 t)$.

Alternatively, for the circuit in Fig. 4.1b, the current-voltage relation is

$$I(t) = \frac{dQ}{dt} = [a_1 - 2a_2 V + 3a_3 V^2 - 4a_4 V^3 + \dots] \frac{dV}{dt} \quad (4-5)$$

When driven by the sinusoidal voltage $V(t) = \sin(k\omega_0 t)$, the resulting current is of the form

$$I(t) = b_1 \cos(k\omega_0 t) - b_2 \sin(2k\omega_0 t) + b_3 \cos(3k\omega_0 t) - \dots \quad (4-6)$$

Once again, with k -odd, $I(t)$ contains both even and odd harmonics, but

with k -even, $I(t)$ contains only even harmonics. The sign differences in eqns.(4-4) and (4-6) make harmonic separation possible in balanced varactor circuits. The basic analysis holds for the more general case described by eqn. (4-3).

4.3 Two-Terminal Configurations

Four possible varactor interconnections (Series, Anti-series, Parallel, and Anti-parallel) result in a two-terminal configuration. These are shown schematically in Fig. 4.2. As will be shown, only Anti-series and Anti-parallel arrangements are useful for harmonic separation.

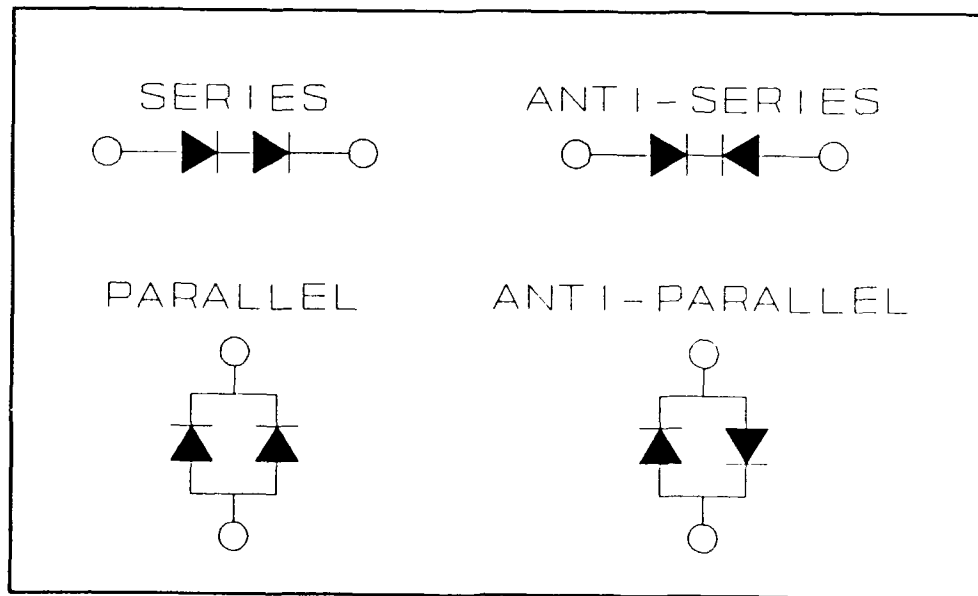


Figure 4.2 Two-terminal varactor configurations.

SERIES

Fig. 4.3 shows two varactors connected in Series under source excitation. Note that $I = I_1 = I_2$, however the voltage across each diode is $1/2 V$ assuming that both Schottky varactors have identical reverse saturation currents (an impossibility even for monolithic circuits) so

that the bias voltage from a single supply is evenly dropped across the two varactors.

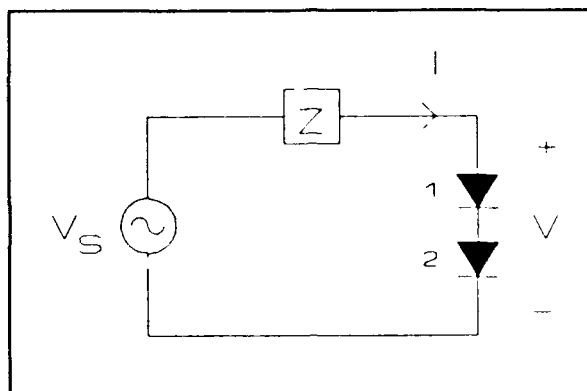


Figure 4.3 Series connected varactors in an embedding circuit.

This arrangement is more appropriate for varistors operating under forward bias. It is obvious that no harmonic separation takes place. Fig. 4.4 shows a single-device equivalent circuit for the Series arrangement.

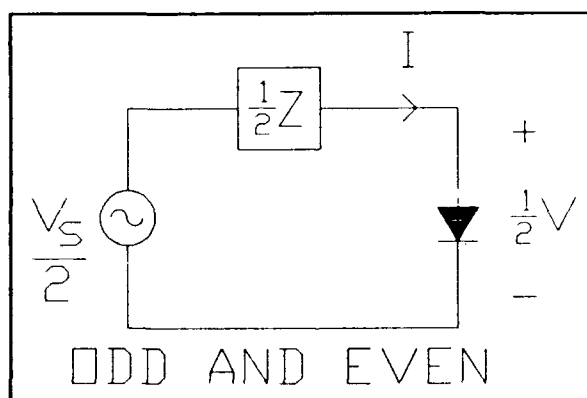


Figure 4.4 Single device equivalent circuit for the Series arrangement.

In this single-device equivalent circuit, the embedding impedances are half the two-diode value, which results in the same current but half the voltage. Absolute power levels are half that of the two-diode circuit, however relative power levels (as in efficiency) will remain unchanged.

The advantages and disadvantages of the Series arrangement as compared with a single varactor are as follows:

ADVANTAGES

- + Higher output power
- + Larger embedding impedances

DISADVANTAGES

- No harmonic separation
- Higher drive levels needed
- NOT for Schottky varactors

ANTI-SERIES

The Anti-series connection and embedding circuit are shown in Fig. 4.5. Note that I_1 takes the form of eqn.(4-4) and I_2 takes the form of eqn.(4-6), but since $I_1 = I_2 = I$, I must contain only odd harmonics.

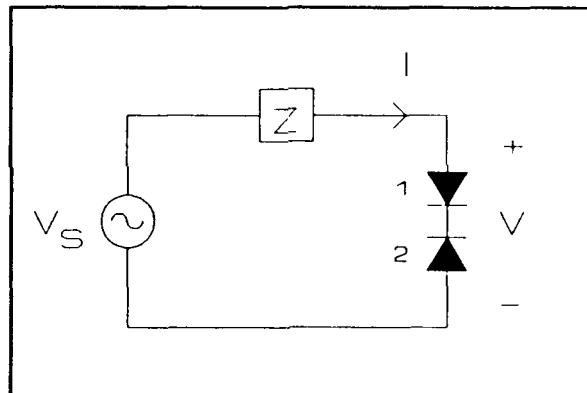


Figure 4.5 Anti-series varactors in an embedding circuit.

Note that unless each Schottky diode is individually biased, this arrangement is of limited use for Schottky varactor operation. However, for Schottky varistors or for novel varactor devices, this arrangement may be practical provided the characteristics of the nonlinearity are symmetrical, otherwise even harmonics will be generated. The single device equivalent circuit is shown in Fig. 4.6.

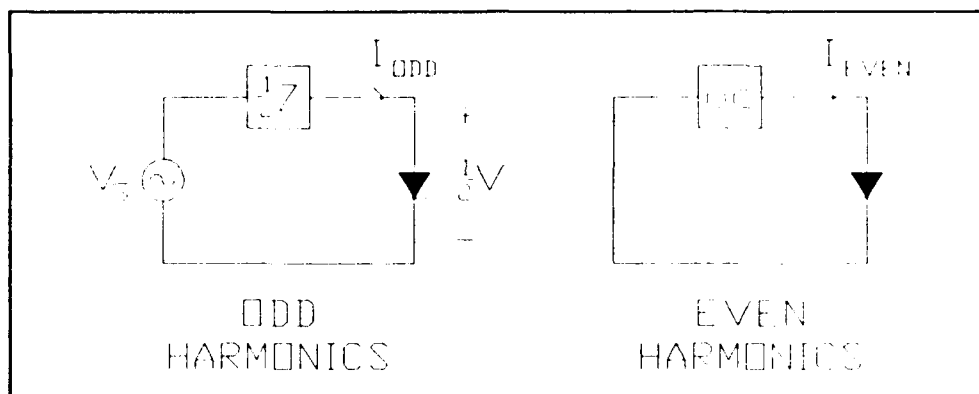


Figure 4.6 Single device equivalent circuit for Anti-series arrangement.

Note that in this case, the embedding impedance of the single-device equivalent circuit is half that of the two-diode circuit. Only odd currents are permitted and voltage across the device is half the two-diode value. Again, absolute power levels are half that of the two-diode circuit but relative power levels are the same.

The advantages and disadvantages of the Anti-series arrangement as compared with a single varactor are:

ADVANTAGES

- + Higher output power
- + Larger embedding impedances
- + Direct tripler

DISADVANTAGES

- Not practical for Schottky varactors
- Higher drive levels needed
- Identical diodes needed

PARALLEL

Consider two diodes connected in PARALLEL as shown in Fig. 4.7. This is obviously the same as a single diode with twice the area and half the impedance. Therefore without further discussion, the single-device equivalent circuit for this case is presented in Fig. 4.8. Here, the circuit impedance is twice the two-diode value resulting from the same

voltage across each varactor but with half the current. For the equivalent circuit, absolute power levels are half the two-varactor circuit values and relative power levels are the same.

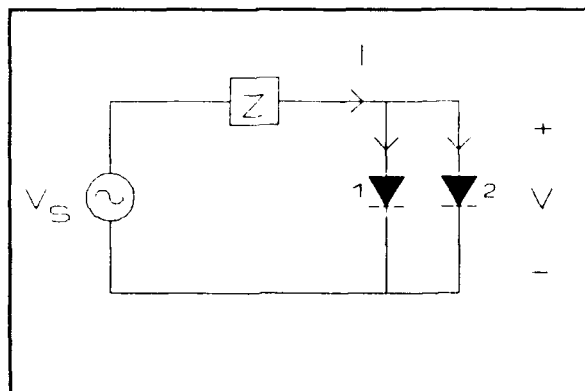


Figure 4.7 Parallel arrangement with embedding impedance.

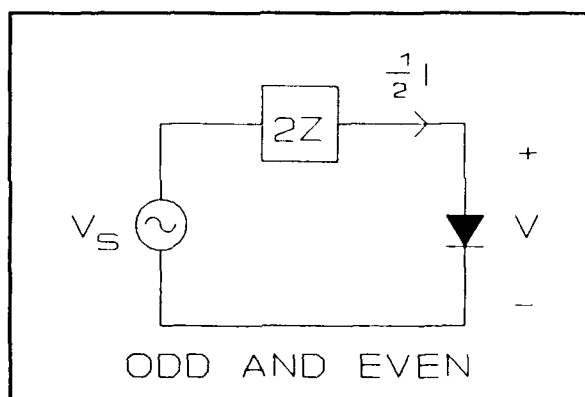


Figure 4.8 Single device equivalent circuit for the Parallel arrangement.

The advantages and disadvantages of the Parallel configuration as compared with a single varactor are:

ADVANTAGES

- + Higher output power
- + Similar bias as single device

DISADVANTAGES

- No harmonic separation
- Higher drive levels needed
- Smaller embedding impedances

ANTI-PARALLEL

The important Anti-parallel configuration is shown in Fig. 4.9.

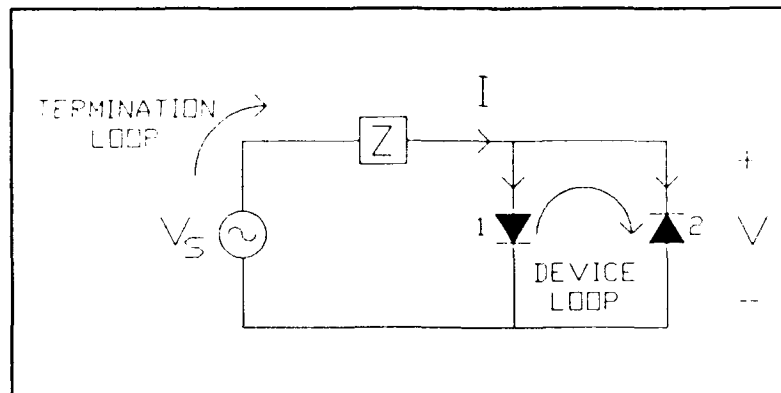


Figure 4.9 Anti-parallel arrangement with embedding circuit.

As in the Parallel case, $I = I_1 + I_2$, however in the Anti-parallel case I_1 takes the form of eqn.(4-4) and I_2 takes the form of eqn.(4-6). The magnitude and direction of the odd-order frequency terms of both I_1 and I_2 are the same, no odd harmonic currents can circulate in the device loop since the imposed voltage is common to both varactors. Hence, the odd harmonic currents with twice the individual diode value circulate in the termination loop. The even-order harmonic frequencies are opposite in direction indicating a circulating current within the diode loop. The single device equivalent circuit is shown in Fig. 4.10. The voltage across the single-device equivalent is the same as for the actual circuit, however the current is half as large. Alternatively, an equivalent varactor of twice the anode area could be used with I and Z unchanged. The even harmonic currents in the device loop should have an embedding impedance of zero ohms (neglecting diode series resistance and loop inductance). The embedding impedance of the odd harmonic frequencies is effectively twice the actual embedding impedance. For this equivalent

circuit, absolute power levels are double that of the two-diode circuit and relative power levels are the same.

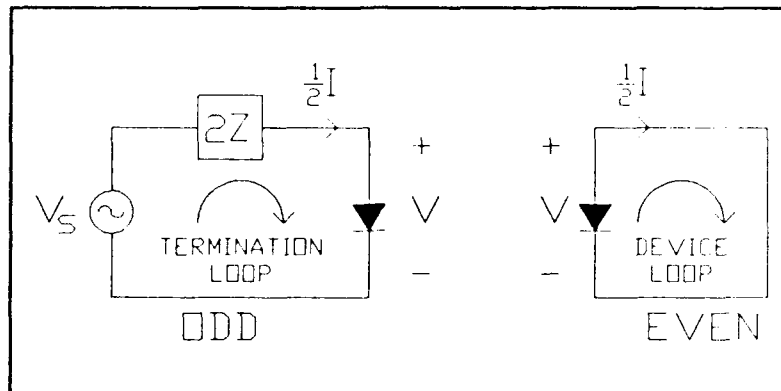


Figure 4.10 Single device equivalent circuit for the Anti-parallel arrangement.

The Anti-parallel configuration should make an efficient frequency tripler with relatively wide bandwidth since harmonic separation is possible with a minimum of external filtering which has resistive loss and limited bandwidth. However, a major difficulty with such an interconnection of Schottky varactors is the requirement of independent biasing. This biasing must be provided while not disturbing the circuit balance. One possible realization of the biased Anti-Parallel configuration is shown in Fig. 4.11.

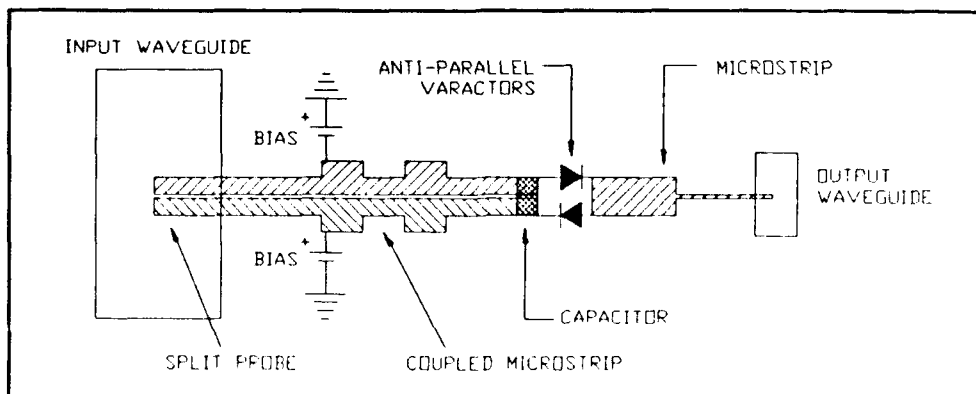


Figure 4.11 Example of the Anti-parallel configuration.

The advantages and disadvantages of the anti-parallel configuration as compared with a single varactor are as follows:

ADVANTAGES

- + Efficient harmonic separation
- + Higher output power
- + Wide bandwidth idler loop

DISADVANTAGES

- Biasing problem
- Higher drive levels needed
- Smaller embedding impedances

4.4 Three-Terminal Configurations

The two possible configurations consisting of two varactors and three terminals are the Anti-series/parallel and the Anti-parallel/series. Both are shown in Fig. 4.12.

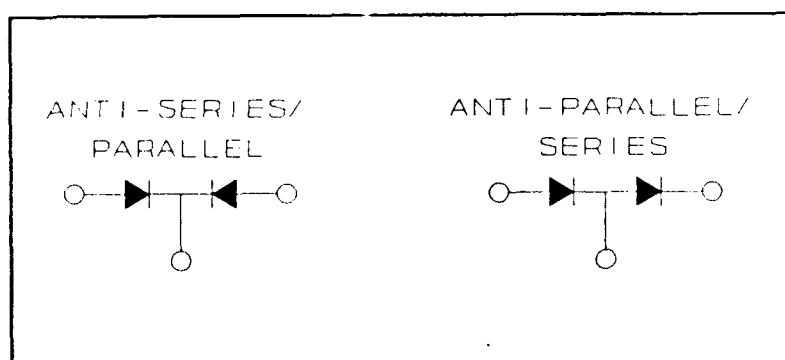


Figure 4.12 Three-terminal varactor interconnections.

The addition of the third terminal (not present in the basic Series and Anti-series arrangements) is important for harmonic separation.

ANTI-SERIES/PARALLEL

A schematic of the ANTI-SERIES/PARALLEL arrangement is shown in Fig. 4.13. The current I_1 takes the form of eqn. (4-4) however, I_2 takes on

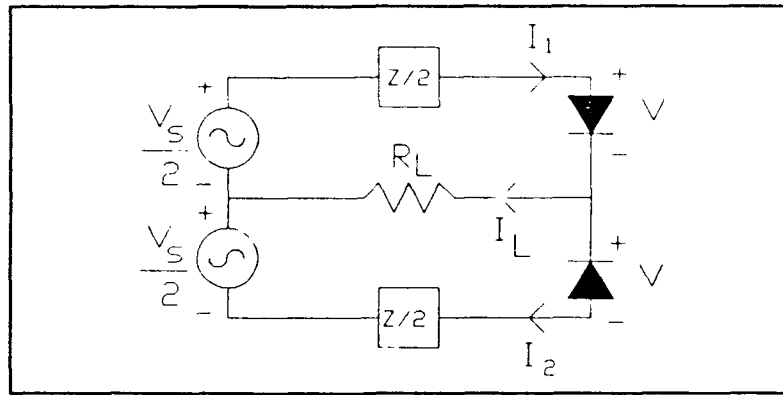


Figure 4.13 Anti-series/parallel arrangement with embedding circuit.

a slightly different form due to the negative applied voltage:

$$I(t) = b_1 \cos(k\omega_0 t) + b_2 \sin(2k\omega_0 t) - b_3 \cos(3k\omega_0 t) - \dots \quad (4-7)$$

where the odd-order terms have negative signs. The outer loop, which contains the two varactors in anti-series, will permit only odd harmonic currents to circulate as expected from the Anti-series analysis (note that even harmonics are in the outer loop but they do not circulate). However, in the two inner loops with common load impedance, $I_L = I_1 + I_2$ contain only even-order harmonic currents. The single device equivalent circuit is shown in Fig. 4.14.

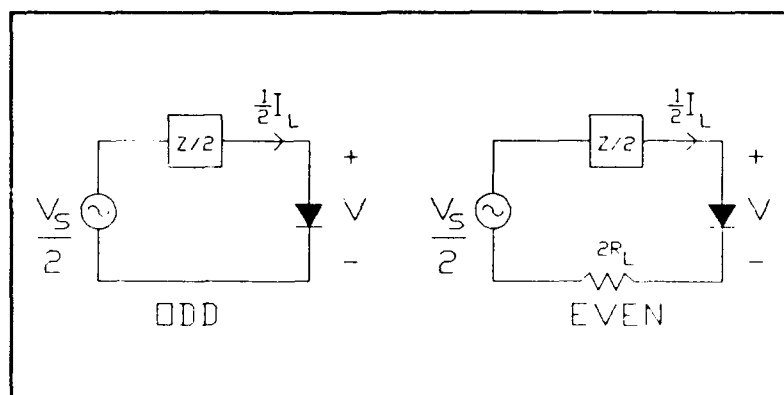


Figure 4.14 Single device equivalent circuit for the Anti-series/parallel arrangement.

In this equivalent circuit, absolute power levels are double their two-diode circuit values but the relative power levels are the same. Note that the load only appears in the even harmonic circuit (doubler) but with twice the two-diode impedance because the varactors effectively appear in parallel for the even harmonics. Note further that the source impedance appears in the even harmonic circuit as well.

This circuit is that of the popular full-wave rectifier used in power supplies. The symmetrical source is provided by a center-tapped transformer. However, at microwave frequencies, the symmetrical source can be provided by ring hybrid (rat race hybrid) or a tapered coupled line hybrid in planar circuits and by a magic tee in waveguide circuits. One example of a planar realization using the ring hybrid is shown in Fig. 4.15.

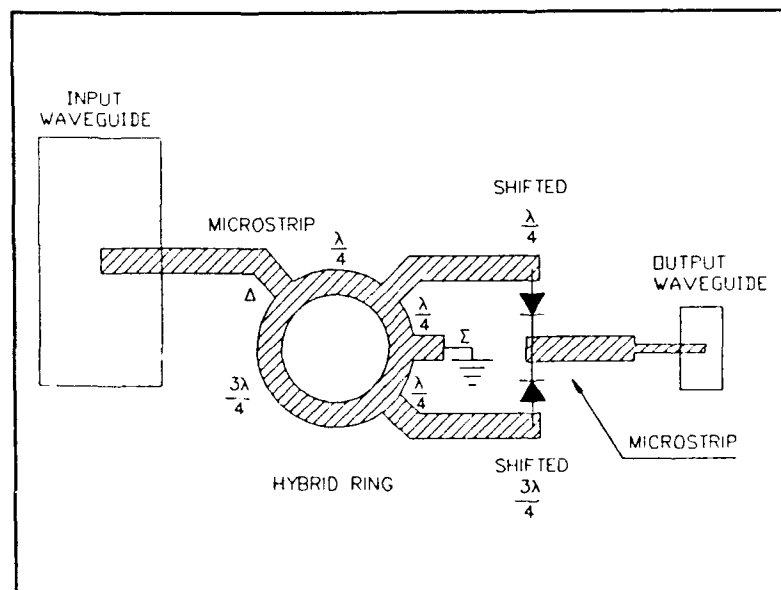


Figure 4.15 Example planar realization of the Anti-series/parallel arrangement.

The advantages and disadvantages of the Anti-series/parallel configuration as compared with a single varactor are as follows:

ADVANTAGES

- + Efficient harmonic separation
- + Higher output power
- + Larger Z_{emb} for odd harmonics
- + Frequency doubler

DISADVANTAGES

- Biasing problem
- Higher drive levels
- 180 deg. hybrid needed
- Z_{emb} not harmonic independent

ANTI-PARALLEL/SERIES

A schematic of the Anti-parallel/series arrangement is shown in Fig. 4.16. I_1 takes the form of eqn.(4-4) and I_2 the form of eqn.(4-6). Note that the $I = I_1 + I_2$ contains only odd harmonics which return through the center-tap of the transformer, hence no odd harmonics appear in the transformer secondary. The varactors are in an anti-parallel arrangement to the odd frequency harmonics.

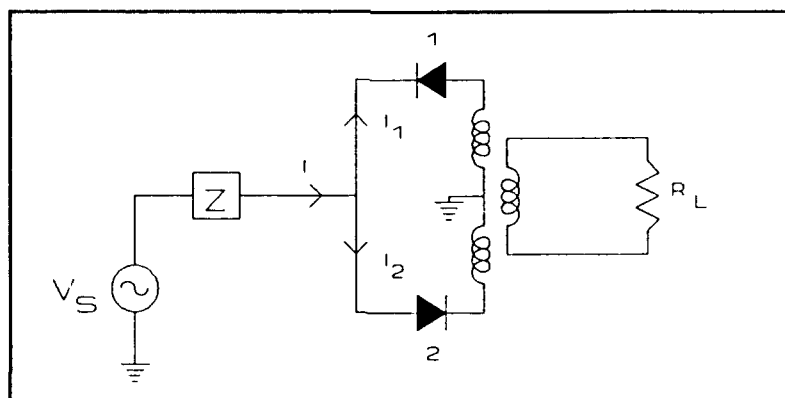


Figure 4.16 Anti-parallel/series arrangement and embedding circuitry.

The even harmonic currents circulate in the device loop, which includes the primary of the transformer. The even-order harmonics thus appear in the transformer secondary and the load circuit. This

arrangement can be thought of as the Parallel configuration except that the loop for the even currents includes the load. A single device equivalent circuit is shown in Fig. 4.17.

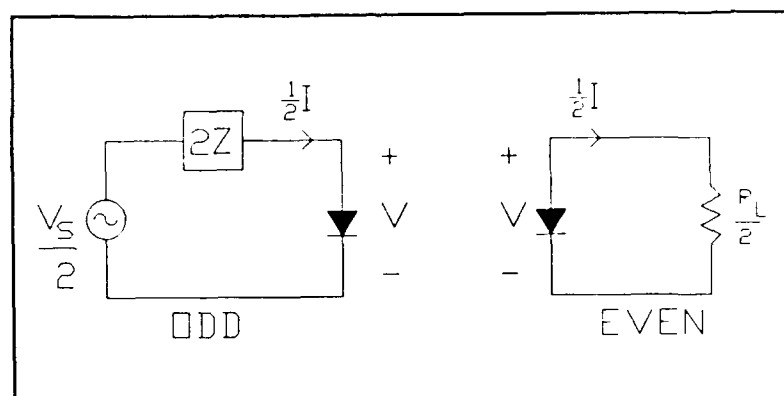


Figure 4.17 Single-device equivalent circuit for the Anti-Parallel/series arrangement.

On this equivalent circuit, the absolute power levels are double that of the two-diode circuit and the relative power levels are the same. The embedding impedances are twice the actual values for the odd harmonic currents, and half for the even harmonics currents.

This circuit behaves as a frequency doubler. At microwave frequencies, the transformer is usually replaced with a 180-degree hybrid, however these two passive devices may not perform the same at the odd harmonic frequencies, i.e. the hybrid may appear as an open circuit rather than the required short circuit. A planar realization for this configuration is shown in Fig. 4.18. The suspended stripline to finline junction is a unique form of the 180-degree hybrid. Here, the odd harmonic currents on the stripline travel through the varactors in anti-parallel and return on the ground plane and do not excite the finline. The even harmonic currents generated in the varactors excite the finline but not the stripline.

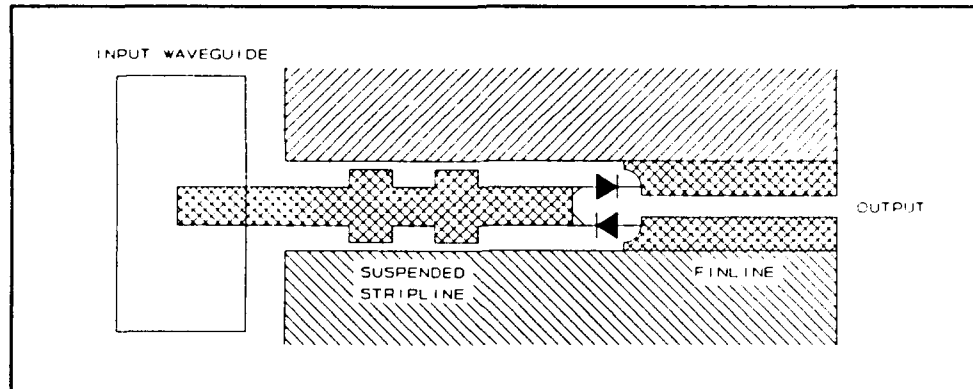


Figure 4.18 Example planar realization of the Anti-Parallel/Series arrangement (Nguyen, 1987).

The advantages and disadvantages of the Anti-parallel/series configuration as compared with a single varactor are as follows:

ADVANTAGES

- + Efficient harmonic separation
- + Higher output power
- + Larger Z_{emb} for even harmonics
- + Frequency doubler

DISADVANTAGES

- Biasing problem
- Higher drive levels
- 180 deg. hybrid needed
- Smaller Z_{emb} for odd harmonics

4.5 Four-Terminal Configurations

Up to this point, only interconnections of two varactors have been considered. It is conceivable that a balanced four varactor circuit may present some advantages over the two varactor configurations. The following analysis will examine three such arrangements: Dual Anti-parallel in series, Varactor Ring, and Dual Parallel in Series. The three configurations are shown in Fig. 4.19. The capacitors shown in the figures represent an RF short circuit.

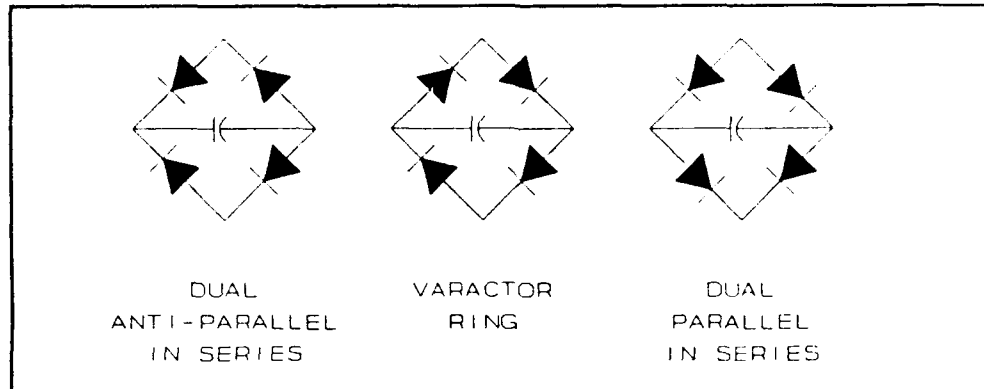


Figure 4.19 The four-terminal, four varactor arrangements.

DUAL ANTI-PARALLEL IN SERIES

Fig. 4.20 shows the Dual Anti-parallel in Series configuration.

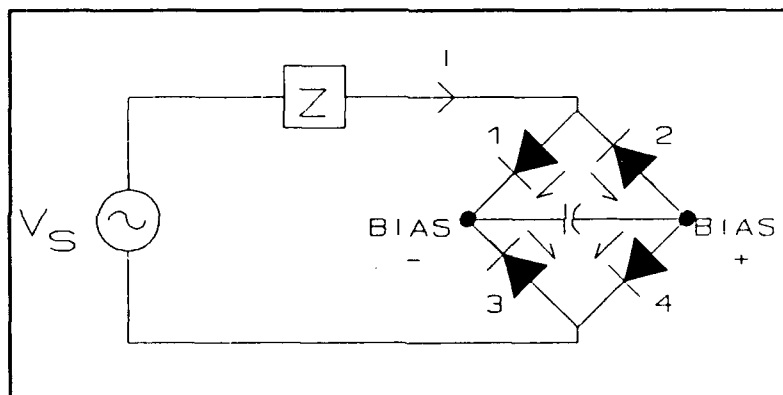


Figure 4.20 Dual Anti-parallel in Series configuration with embedding circuit.

Currents I_1 and I_4 take the form of eqn.(4-4). Currents I_2 and I_3 take the form of eqn.(4-6). By inspection, $I = I_1 + I_2 = I_3 + I_4$ contains only odd harmonics which circulate in the termination loop. The even harmonics circulate in each of the two device loops, where the bypass capacitor forms a short circuit across its terminals. A single device equivalent circuit is presented in Fig. 4.21.

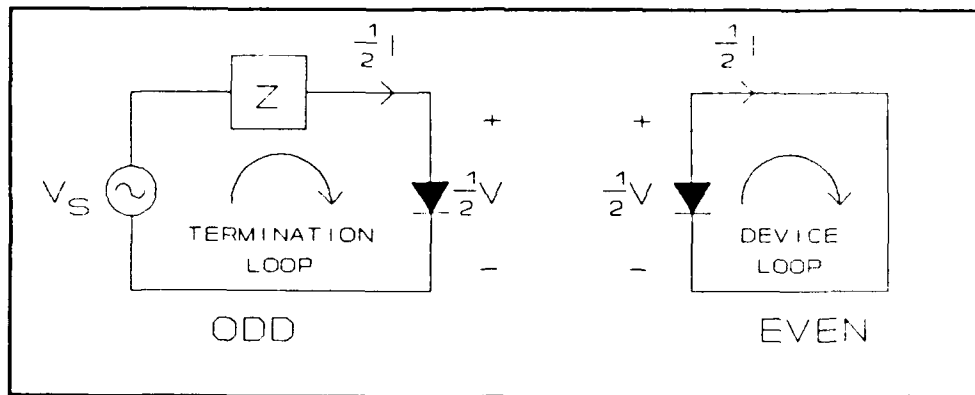


Figure 4.21 Single device equivalent circuit for the Dual Anti-parallel in Series arrangement.

The voltage across each varactor is half the applied voltage, and the current through each varactor is half of the total current. It is interesting that the odd harmonic embedding impedances for the single device equivalent are the same as in the actual circuit. All absolute power levels should be multiplied by four but relative power levels remain the same.

One possible planar realization of this circuit is shown in Fig. 4.22. Despite the biasing method that takes advantage of the circuit symmetry, this configuration suffers from the same problems as in the Series arrangement. This circuit can be used as a frequency tripler.

The advantages and disadvantages of the Dual Anti-parallel in Series configuration as compared with a single varactor are as follows:

ADVANTAGES

- + Efficient harmonic separation
- + Higher power circuit
- + Z_{emb} same
- + Frequency tripler
- + Compact idler loop

DISADVANTAGES

- Biasing problem
- Very large drive levels
- NOT for varactors

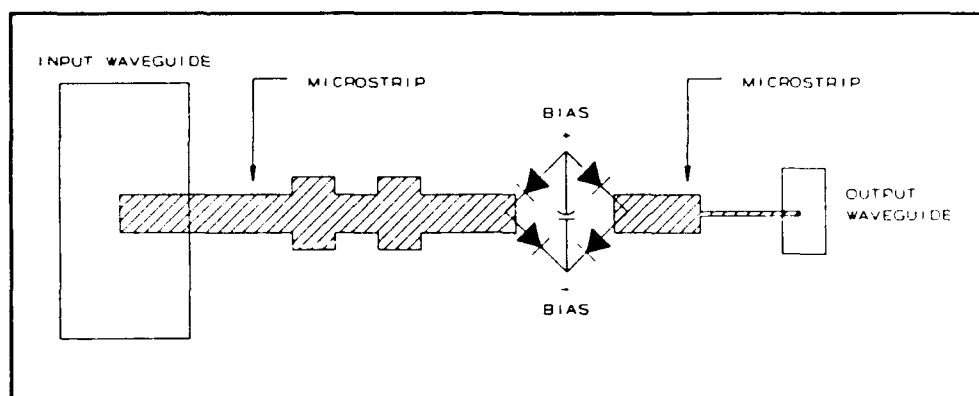


Figure 4.22 Planar realization of the Dual Anti-parallel in Series configuration.

VARACTOR RING

The Varactor Ring arrangement is shown in Fig. 2.23.

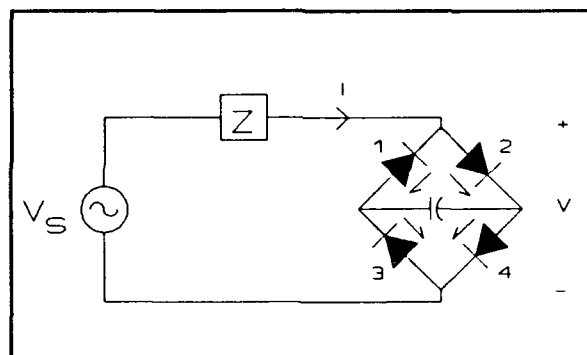


Figure 4.23 Varactor Ring in embedding circuit.

This is a slight variation on the Dual Anti-parallel in Series arrangement. Harmonic frequency separation is performed in exactly the same fashion. Under balanced conditions, there should be no current through the bypass capacitor, hence it could be removed since the even harmonic currents encircle all four varactors in the loop. The single device equivalent circuit is the same as in the Dual Anti-parallel in series case. The major disadvantage of this arrangement is that biasing of Schottky varactors is impossible without disrupting the loop balance.

The advantages and disadvantages of the Varactor Ring configuration as compared with a single varactor are as follows:

ADVANTAGES

- + Efficient harmonic separation
- + Higher power circuit
- + Z_{emb} same
- + Frequency tripler

DISADVANTAGES

- Major biasing problem
- Very large drive levels
- Very sensitive to balance

DUAL PARALLEL VARACTORS IN SERIES

The Dual Parallel Varactors in Series configuration is illustrated in Fig. 4.24.

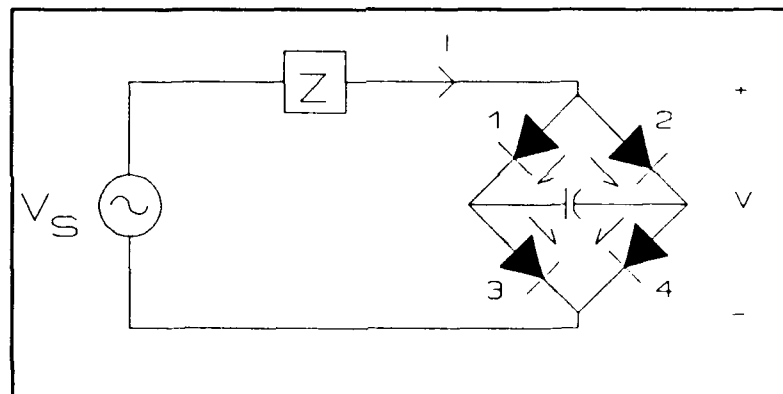


Figure 4.24 Dual Parallel in Series arrangement in embedding circuit.

It is obvious that $I_1 = I_2 = I_3 = I_4$ and of the form of eqn.(4-4). This configuration does not permit harmonic separation. The single device equivalent circuit is shown in Fig. 4.25. The embedding impedances of all the harmonics are the same as in the single device case. Absolute power levels are multiplied by four and relative power levels are the same.

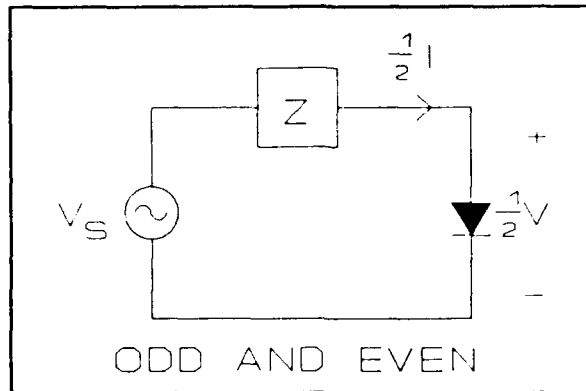


Figure 4.25 Single device equivalent for Dual Parallel in Series case.

The advantages and disadvantages of the Dual Parallel in Series configuration as compared with a single varactor are as follows:

ADVANTAGES

- + Higher power
- + Z_{emb} same
- + Higher power circuit

DISADVANTAGES

- Biasing problems
- Very large drive levels
- No harmonic separation

4.6 Discussion

The above analysis has shown that two- and four-varactor circuits provide a form of symmetry that can be used to separate even and odd order harmonics efficiently without the need for external filtering. Furthermore, the more simplified biasing requirements of the two-varactor arrangements makes such circuits more appealing than the more complex four varactor arrangements.

The Anti-parallel/series arrangement of two diodes for a doubler takes advantage of the harmonic separation yet allows for independent biasing of the varactors. The Parallel arrangement for a tripler uses the inherent harmonic separation properties very efficiently by providing a

very compact loop for idler currents. Further discussion of these specific multi-varactor arrangements are presented in Chapters Six, Seven, and Eight.

4.7 Conclusions

This chapter contains background information on the physical nature of the Schottky-barrier junction varactor which is then used to develop a circuit model and characteristic equation for the device. Using the methods proposed by Penfield and Rafuse to analyze the circuit model, the large signal solutions for the frequency doubler and tripler are then solved under maximum symmetrical swing and maximum efficiency conditions. The solutions are verified and extended using the numerical technique of Kerr and Siegel. This multiplier evaluation approach serves as the foundation for the analysis of the discrete planar varactor tripler in chapter Three, and the design of the monolithic doubler and triplers of Chapters Six, Seven, and Eight.

Attributes of multiple-varactor circuits are also examined in this chapter to provide the groundwork for balanced planar monolithic multiplier designs. Harmonic separation capability and biasing difficulties were addressed for two-, three-, and four-varactor arrangements. Single device equivalent circuits were presented so that the above multiplier evaluation can be applied directly to the analysis of these balanced circuits. The Anti-parallel/series configuration was chosen for the doubler and the Anti-parallel configuration was chosen for the monolithic tripler designs in the remainder of this work.

CHAPTER FIVE

Overview of the Monolithic Multiplier Designs

5.1 Introduction

This chapter addresses several aspects of millimeter-wave integrated circuit design, ranging from the nature of the integration itself to the specific characteristics of transmission lines, waveguide probes, lumped elements, and the fabrication procedure.

5.2 Natural Progression Toward Monolithic Circuits

Past efforts in millimeter and sub-millimeter wave multiplier circuit miniaturization have focused exclusively on the active device. A good example of this design approach is the whisker-contacted Schottky varactor mounted across waveguide, which is the mainstay multiplier in use above 100 GHz. Despite the mechanical frailty of this design, the whisker-contact works quite well in benign environments. A major disadvantage of this approach is the lack of control over many of the design variables, i.e. performance is sensitive to the amount of solder used to support the diode, position of the diode in the waveguide, etc.

Attempts to improve the mechanical nature and design flexibility for such multipliers has led to the development of planar Schottky varactors. Although the active device is small, the package size must be rather large to allow for mechanical manipulation and external circuit connections. As shown in Chapter Three, the planar device can be used in waveguide circuits, however the performance is compromised by the presence of size-large parasitic elements.

Another approach to integration is the Microwave Integrated Circuit (MIC) where the passive elements are fabricated on a printed circuit board (such as Duroid¹, CuFlon², or metallized quartz) and the active devices are soldered or wire-bonded into place. The relatively large size of the practical device package again restricts the compactness and high frequency applicability of this approach. With proven performance below 100 GHz, this hybrid technique is very important in system integration since the planar nature of the structure allows for compact and direct interconnections. Although the circuit loss associated with planar transmission lines is much greater than for rectangular waveguide, the required line lengths are much shorter, thus making planar lines practical.

The Monolithic Microwave Integrated Circuit (MMIC) approach takes this idea a step further. By fabricating much of the passive circuitry with the active devices, the device package is virtually eliminated and the planar transmission line lengths are even further reduced. Other advantages include complete component fabrication via photolithography which improves the circuit uniformity and the potential for superior performance over MIC and waveguide designs through accurate circuit layout, even achieving designs not practical by other means. The reliability is improved because of fewer circuit interconnections, cost is reduced since hundreds of multiplier chips can be made on a single wafer, and manual assembly time is reduced. The MIC approach can then be applied at the component level rather than at the individual device level. In the

¹Duroid is a trade name registered with Rogers Corp.

²CuFlon is a trade name registered with PolyFlon Corp.

future, such planarization will lead to the integration of millimeter and sub-millimeter wave oscillators, multipliers, mixers, IF amplifiers, antennas, probes etc. into small compact system packages. Until now, the MMIC approach to multiplier design has only been applied below 100 GHz. Consequently, the decision was made to investigate high frequency MMIC multiplier designs as part of this thesis. The three designs are: 1) a doubler to 160 GHz, 2) a tripler to 240 GHz, and 3) a high power tripler to 94 GHz.

5.3 Choice of Planar Transmission Line

5.3.1 Introduction

Fundamental to the MMIC design is the choice of a planar transmission line. The two most widely used planar lines are microstrip and coplanar waveguide (CPW). Coplanar waveguide offers several advantages over microstrip lines for MMIC applications. The basic geometry of CPW permits ease of parallel and series insertion of both passive and active components, i.e no via holes are required to ground active devices. Furthermore, for the fundamental mode, the dimensions of CPW can be chosen to give lower conductor loss and less dispersion as compared with microstrip. The disadvantage of CPW is that the electromagnetic field is less confined than in microstrip, resulting in an increased sensitivity to neighboring structures such as upper and lower shielding, conductor backing, lateral ground plane truncation, and line-to-line coupling. Moreover, past research into line discontinuity models has focused almost exclusively on microstrip.

For high power multiplier applications, conductor backing the CPW (CBCPW) is advantageous because it not only increases the heat-sinking capability of the substrate, but also provides for simplified chip mounting, lowers the characteristic impedance, lessens dispersion, and improves mechanical strength. The difficulties associated with conductor backing are the potential for leakage of power into surface waves or into the dielectric region between the metal planes, and unwanted coupling to neighboring lines.

Despite the advantages of CPW over microstrip, care must be taken when using the various types of CPW to lessen the unwanted effects. It is imperative that the characteristics of such lines be well understood through mathematical analysis of the line geometry or through empirical measurements on scale models. Rigorous mathematical analysis of CPW and CBCPW line geometries have been demonstrated to yield quite accurate models for calculation of line parameters. However, circuit discontinuities, i.g rectangular waveguide transitions, have not been extensively investigated, thus necessitating the use of scale models. Large scale models are useful in designing millimeter wave circuitry since the complex S-parameters at correspondingly lower frequencies can be easily measured using a vector network analyzer (VNA) and circuit de-embedding procedures. However, the validity of such scale models must be justified prior to use of such models in MMIC circuit designs. Therefore, this section is devoted to the characterization of standard CPW and conductor-backed CPW scale models and a comparison with theoretical models described in the literature.

5.3.2 Scale Models versus Mathematical Models

In this section, two types of coplanar waveguides are investigated: 1) conventional CPW and 2) conductor-backed CPW. The empirical approach indirectly measures the line impedance, guide wavelength, and attenuation per unit length by first measuring the two-port S-parameters of the line with a vector network analyzer, and then applying commercial CAD software to optimize the characteristics of an electrical equivalent circuit to fit the measured complex S-parameter data.

For comparison, a mathematical model for CPW and CBCPW, primarily based on the conformal mapping approach, was adopted from Ghione and Naldi (Ghione, 1987). Added to this model was a correction factor for the finite conductor thickness (Gupta, 1979) as well as dielectric loss (Gupta, 1979). Conductor losses were modelled using the quasi-static Green's function approach (Gopinath, 1982). The procedure used in calculating the line characteristics is described in Appendix E. The results of applying both the physical and theoretical models are summarized in the following subsections.

5.3.3 Characterization of the modelling material

A common dielectric material used in scale modelling is Stycast³, which is a hard, yet machinable material that is accurately formulated by the manufacturer to yield a desired dielectric constant. Circuit metallization is usually made using 1 to 2 mil thick copper tape having a gum adhesive backing which contains copper particles. However, measurements on scale models using copper tape for microstrip lines have

³Stycast is a trade name registered with EMERSON & CUMINGS

consistently demonstrated more loss and a lower relative dielectric constant than predicted by theory (based on the bulk dielectric material properties). This deviation has been attributed to the Stycast material itself, however the adhesive region between the copper foil and the Stycast was also suspect. In coplanar waveguide, the effects of this adhesive may be enhanced due to the very strong electric field concentrations within this region. Therefore, as a first-order evaluation, the overall dielectric constant and loss tangent were measured for two small parallel-plate structures, one using copper tape, and the other using copper foil and Ethyl Cyanoacrylate adhesive.

The structure of the small capacitors together with the equivalent circuit is shown in Fig. 5.1.

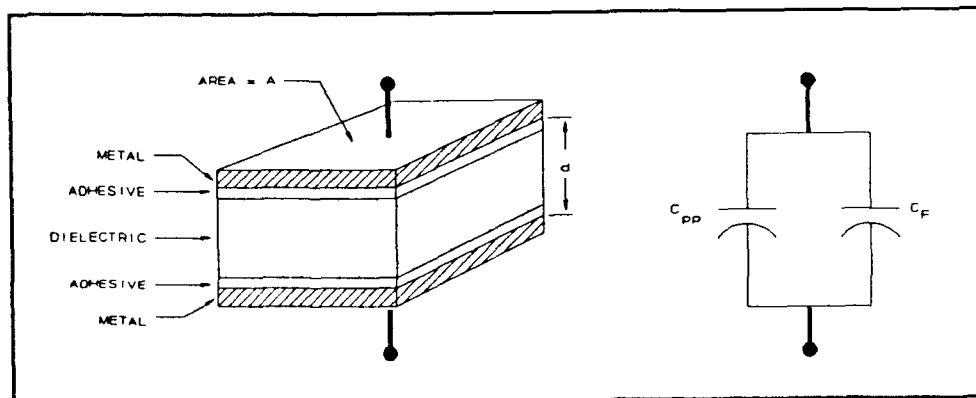


Figure 5.1 Structure and equivalent circuit for the small parallel-plate capacitors.

The total measured capacitance of the structure consists of a parallel-plate and a fringing component:

$$C_T = C_{PP} + C_f = \frac{A\epsilon_0\epsilon_r}{d} + C_f \quad (5-1)$$

where C_T is the measured total capacitance, C_{PP} is the parallel-plate capacitance, C_f is the fringing capacitance, A is the cross-sectional area,

ϵ_0 is the free-space permittivity. ϵ_r is the dielectric constant, and d is the plate separation.

All parallel plate capacitors described in this section have geometrically square plate area equal to 0.831 cm^2 with d equal to 0.224 cm . All total capacitance C_T and parallel resistance R_P measurements were made using a Boonton Type 190-A Q meter at an operation frequency between 150 and 180 MHz. Details of the measuring procedure are described in the instrument instruction manual⁴.

An air-dielectric capacitor was used to calibrate the measurements. With $\epsilon_r = 1$ for this case, $C_T = 0.4 \text{ pF}$ and the calculated C_{PP} for the capacitor geometry is subtracted from the C_T yielding the fringing capacitance: $C_f = 0.072 \text{ pF}$. Although the field patterns near the edges are affected by ϵ_r and will lead to a small measurement error, capacitance C_f is assumed to be independent of ϵ_r for this study.

With this information it is possible to calculate the dielectric constant for the Stycast HiK ($\epsilon_r = 12$) by using the measured C_T as follows:

$$C_{PP} = C_T - C_f = C_T - 0.072 \text{ pF} \quad (5-2)$$

$$\epsilon_r = \frac{C_{PP}d}{\epsilon_0 A} = 3.04 \times 10^{12} C_{PP} \quad (5-3)$$

Assuming that measured loss is dominated by dielectric loss (this is a reasonable assumption since the parallel resistance of the air dielectric capacitor was infinite), the loss tangent for the material is found from the parallel resistance measurement:

⁴"Instruction Manual for the Model 190-A Q Meter", Boonton Radio Corporation, p. 7.

$$\tan \delta = \frac{\sigma}{\omega \epsilon_0 \epsilon_r} = \frac{d}{R_p A \omega \epsilon_0 \epsilon_r} \quad (5-4)$$

where σ is the bulk conductivity, and ω the measurement frequency. The measured values for capacitance, parallel resistance, and loss tangent are summarized in Table 5.1. Capacitor "A" was made using the gum adhesive-backed copper tape. Capacitor "B" was made using copper foil with Ethyl Cyanoacrylate adhesive. These values are compared with theoretical values based on the Stycast HiK ($\epsilon_r = 12$) material specifications (Emerson & Cuming, 1980), and assuming the no adhesive layer is present.

TABLE 5.1 Measured and Theoretical Data for Capacitor Characterization			
PARAMETER	CAPACITOR A Gum Adhesive	CAPACITOR B CyanoA.	THEORY
Capacitance:	3.25 pF	3.80 pF	3.94 pF
Dielectric Constant:	9.9	11.6	12.0
Parallel Resistance:	36 k ohms	72 k ohms	119 k ohms
Loss Tangent:	0.008	0.003	0.002

It is evident from the results that the gummed adhesive with copper particles increases the loss tangent and decreases the effective dielectric constant and simply cannot be ignored. The cyanoacrylate adhesive being thinner and less lossy gives results that are closer to the parallel-plate capacitor theoretical model. The dielectric constant error of -3.3 percent is just outside the range specified by the manufacturer (± 3 percent).

5.3.4 Characterization of Conventional Coplanar Waveguide (CPW)

Two physical models were constructed based on the typical coplanar waveguide configuration shown in Fig. 5.2.

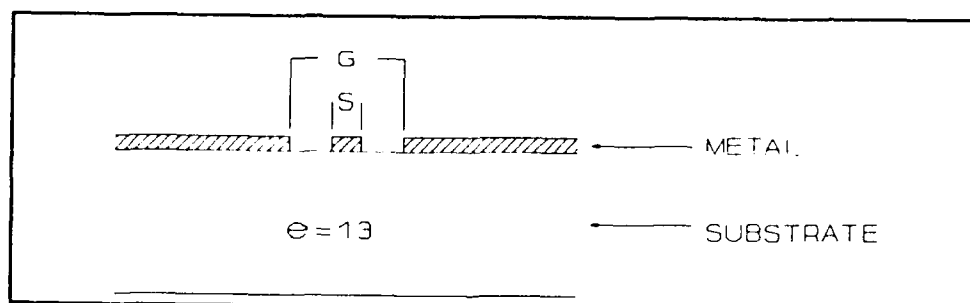


Figure 5.2 Cross-sectional view of coplanar waveguide

Line "A" uses gum-backed copper tape and line "B" uses cyanoacrylate adhesive and copper foil. Both lines are 3 inches in length and the dielectric material is Stycast HiK ($\epsilon_r = 12$) of 2.54 mm thickness.

A CPW can propagate energy in two modes: an unbalanced signal in the odd mode of coupled slotlines (known as the CPW mode), and a balanced signal in the even mode of coupled slotlines. The characteristic impedance of the two modes are different. The unbalanced CPW mode is used throughout this thesis. To excite this mode, chassis-type female SMA connectors were used at each end of the line to form a transition to coaxial cable which is also unbalanced. All four complex S-parameters of the line were measured using an HP8510 vector network analyzer. Initially, a series inductance and a shunt capacitance was included in the model of the coaxial/CPW interface, however the unbalanced nature of both CPW and coaxial lines together with the similar geometrical sizes permitted a very smooth coaxial/CPW transition resulting in the simple equivalent shown in Fig. 5.3. The equivalent circuit was optimized using

the CAD linear analysis package TouchStone⁵ to fit the response predicted for the equivalent circuit in Fig. 5.3 to the measured response. The line characteristics were then extracted from the equivalent circuit model.

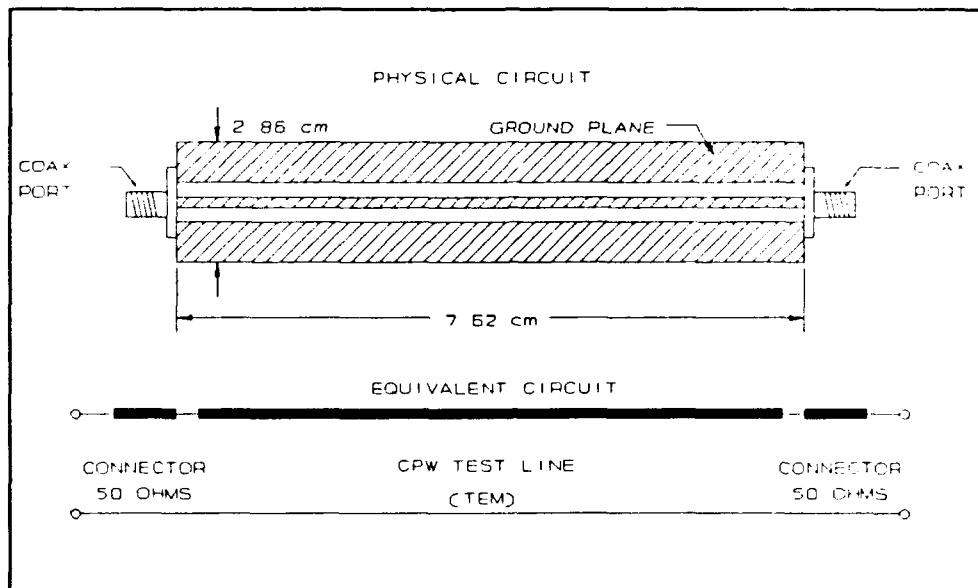


Figure 5.3 CPW test line and corresponding equivalent circuit.

Data for line "A" and line "B" are shown in Tables 5.2 and 5.3 respectively. The CPW theory predicts the behavior of the cyanoacrylate-based model (line "B") more accurately; with +1.2 percent error in line impedance and -3.7 percent error in guide wavelength. The mathematical model assumes that the metal is in intimate contact with the dielectric, a reasonable assumption for MMIC designs but clearly not the case for physical models which have finite adhesive thickness. Furthermore, the mathematical model also assumes an infinite ground plane and a very thick dielectric. However, physically increasing the area of the ground plane and the thickness of the dielectric on the models had negligible effect on the line performance.

⁵TouchStone is a product of EESoF Corporation

Table 5.2 CPW Modelling Data					
TYPE A: Gummed Copper Tape $s = 1.27 \text{ mm}$ $\epsilon_r = 9.9$ $t_m = 0.05 \text{ mm}$ $g = 2.54 \text{ mm}$ $\tan \delta = 0.008$					
Data	Frequency [GHz]	Impedance [Ohms]	ϵ_{eff}	Guide λ [mm]	Atten. [dB/mm]
THEORY	3.0	50.0	5.4	42.8	0.007
	5.0	50.0	5.4	25.7	0.011
MEASURED	3.0	47.0	4.2	46.7	0.006
	5.0	47.0	4.2	28.0	0.010

Table 5.3 CPW Modelling Data					
TYPE B: Cyanoacrylate $s = 1.27 \text{ mm}$ $\epsilon_r = 11.6$ $t_m = 0.05 \text{ mm}$ & Copper Foil $g = 2.54 \text{ mm}$ $\tan \delta = 0.003$					
Data	Frequency [GHz]	Impedance [Ohms]	ϵ_{eff}	Guide λ [mm]	Atten. [dB/mm]
THEORY	3.0	46.5	6.3	39.9	0.004
	5.0	46.5	6.3	23.9	0.006
MEASURED	3.0	47.0	5.3	41.4	0.005
	5.0	47.0	5.3	24.8	0.008

Scale models of CPW lines and related structures should be used with discretion since the lower dielectric constant of the adhesive results in a lower effective dielectric constant for the line. This effect can be minimized by using cyanoacrylate adhesive in the models.

5.3.5 Effects of Conductor-Backing CPW

The purpose of this experiment was to understand the effects of placing a conductor-back on the CPW structures (forming CBCPW), specifically the leakage of power into the dielectric region between the ground planes and any significant alteration of the guide wavelength. The

mathematical analysis of CBCPW was taken from the same references as for the CPW analysis (see Section 5.3.2).

Fig. 5.4 is cross-sectional sketch of the conductor-backed coplanar waveguide physical model. A 6 inch section of CBCPW was made using copper tape (gum adhesive) on a 2.54 mm thick Stycast HiK ($\epsilon_r = 12$) substrate.

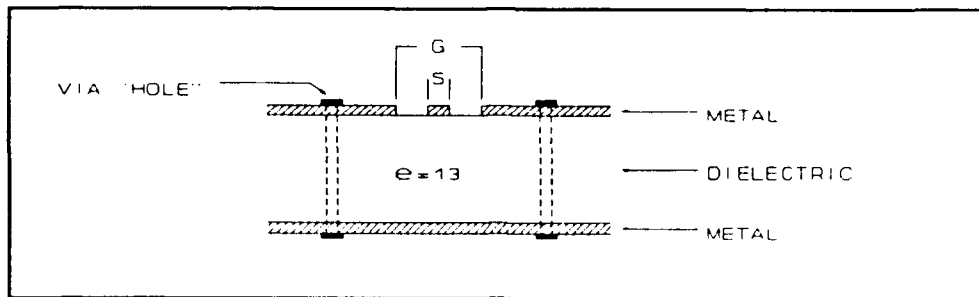


Figure 5.4 Cross-sectional view of conductor-backed CPW. (Not to scale).

To reduce unwanted coupling into the MMIC substrate, the two ground planes would be electrically connected by "via" holes through the dielectric. The via holes are simulated using two rows of 0-80 machine screws. The rows were spaced 5.5 mm apart (centered along the CPW) and screws were evenly spaced at 9.1 mm ($\lambda_g/4$ at 3.83 GHz) as shown in Fig. 5.5.

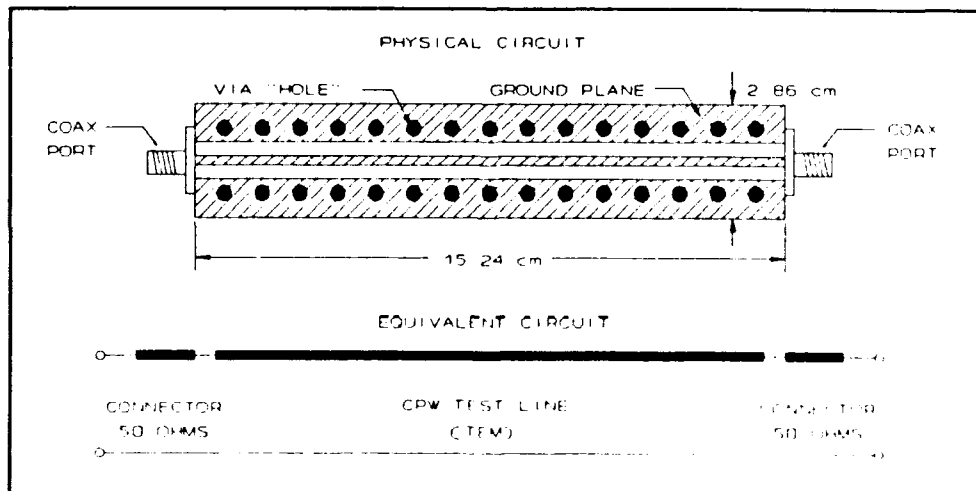


Figure 5.5 CBCPW test line and equivalent circuit.

Table 5.4 summarizes the measured and theoretical characteristics of the CBCPW lines.

Table 5.4 CBCPW Modelling Data					
Gummed Copper Tape $s = 1.27 \text{ mm}$ $\epsilon_r = 9.9$ $t_m = 0.05 \text{ mm}$ $g = 1.91 \text{ mm}$ $\text{Tan } \delta = 0.008$					
Data	Frequency [GHz]	Impedance [Ohms]	ϵ_{eff}	Guide λ [mm]	Atten. [dB/mm]
THEORY	3.0	39.7	5.6	42.4	0.008
	5.0	39.7	5.6	25.4	0.012
MEASURED	3.0	43.0	4.2	46.7	0.005
	5.0	43.0	4.2	28.0	0.008

The data in Table 5.4 indicate that the chosen theoretical model predicts an 8 percent lower line impedance and a 10 percent shorter guide wavelength than measured on the physical models. Interestingly, the guide wavelength is very similar to standard CPW made with copper tape. It was therefore postulated that cyanoacrylate adhesive would show similar results and hence was not investigated experimentally. As with CPW, scale models of CBCPW should therefore be used with caution.

Fig. 5.6 shows the $|S_{21}|$ data for the CBCPW where the onset of the dielectric slab-line mode is noted near the frequency of 3.8 GHz at which frequency the via holes are $\lambda_g/4$ apart. It is therefore important to space the via holes less than $\lambda_g/4$ of the shortest guide wavelength, preferably in a random fashion to eliminate the unwanted coupling which is greatest for periodic structures. However, such a close spacing of via holes may cause a high degree of mechanical stress in the MMIC substrate leading to long term substrate fatigue and cracking.

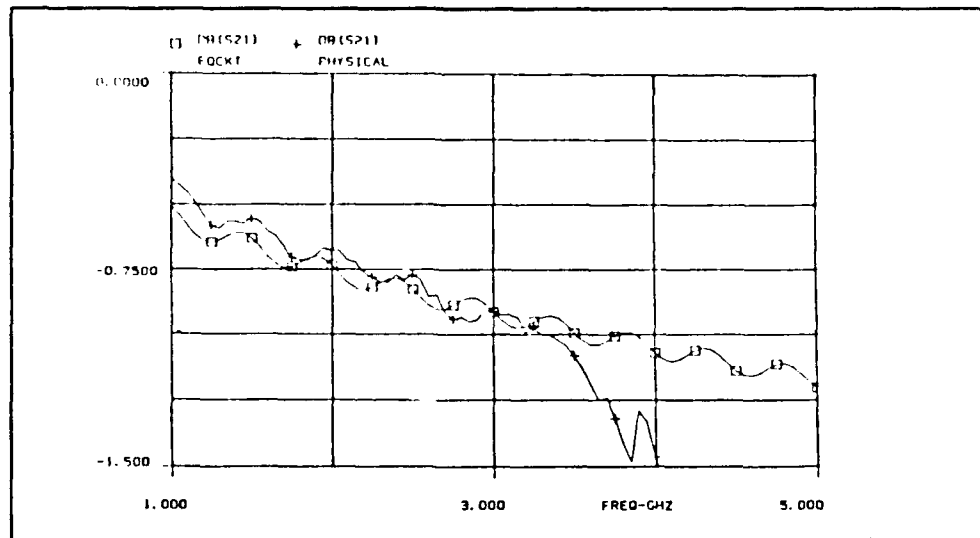


Figure 5.6 Fit of measured S21 data to the electrical equivalent circuit for CBCPW (Onset of dielectric mode is shown).

5.4 Monolithic CPW Junctions and Inverted CPW

5.4.1 Introduction

This section examines several types of CPW junctions that are used in the MMIC multiplier designs. The CPW-CPW junction is important for bias connections and tuning stubs. The CPW-Slotline junctions are needed for the balanced doubler configuration. Finally, inverted CPW was developed as a solution to the significant problems associated with conductor-backed slotline.

5.4.2 CPW-CPW Junctions

The coplanar waveguide tee junction chosen for the MMIC multipliers and the equivalent circuit are shown in Fig. 5.7. The design was proposed by Hirota, Tarusawa, and Ogawa (Hirota, 1987), however, it was slightly modified in the present work: air bridges are used across the lateral line rather than across the main line to minimize the discontinuity in the main

line. The series inductance on the lateral line and the shunt capacitance are very small.

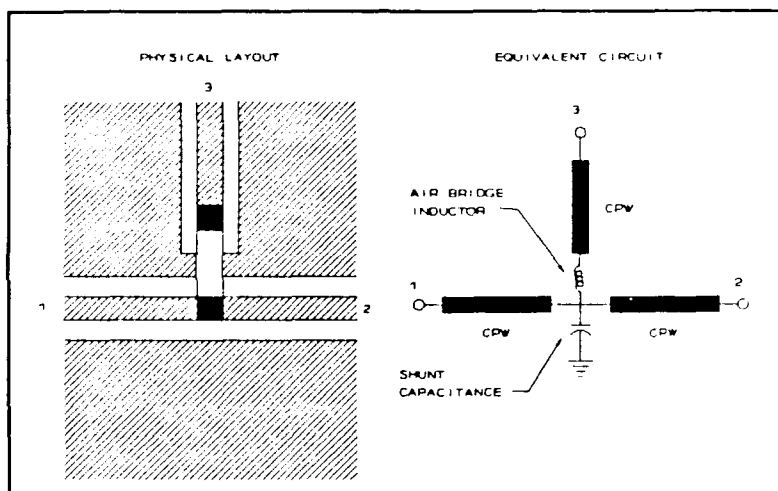


Figure 5.7 Sketch of the CPW tee junction.

5.4.3 CPW-Slotline Junctions

There are two types of CPW-slotline junctions used in the MMIC multiplier designs: a) the hybrid and b) planar balun.

a. Hybrid

The 180-degree hybrid junction is typically a four port network with a 180 degree phase shift between the two output ports. Such a hybrid is need for the ANTI-PARALLEL/SERIES doubler configuration (see Section 2.6.3). However, in CPW/slotline, the 180 degree hybrid is formed as shown in Fig. 5.8. As discussed in Chapter Two, by mounting diodes across the junction as shown, the diode pair can be driven in parallel yet out-of-phase at the odd frequencies and appear in series to drive the slotline at the even harmonics. Further details are presented in Chapter Five.

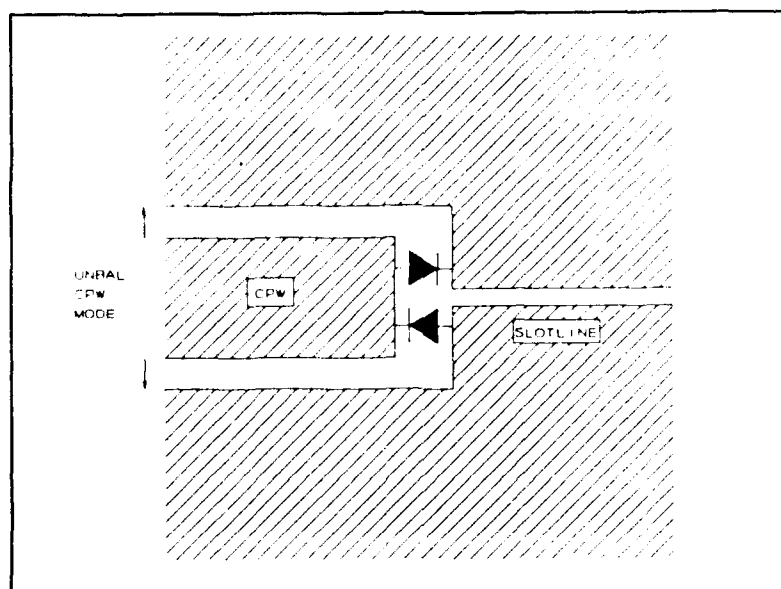


Figure 5.8 The 180-degree hybrid junction required for the doubler circuit.

b. Planar Balun

A planar balun is used in the MMIC doubler to convert the balanced slotline to unbalanced CPW. Two possible designs for the balun were considered. The first, proposed and applied by Hirota, Tarusawa, and Ogawa (Hirota, 1987) and Ogawa and Minagawa (Ogawa, 1987) uses an open circuit slotline and open circuit CPW. The balun proposed by Fouad Hanna and Ramboz (Fouad Hanna, 1982) which has been implemented recently in a double-balanced mixed design (Cahana, 1989), uses an open circuit CPW and a short circuit slotline. Fig. 5.9 shows a sketch of the balun together with the equivalent circuit which was performance optimized using Touchstone. The balun is a junction of a 50 ohm CPW with a 55 ohm slotline, hence $N = 0.9535$. The tuning reactance X_c is formed by an open circuit stub:

$$X_c = -jZ_B \cot\left(\frac{\beta L}{2}\right) \quad (5-5)$$

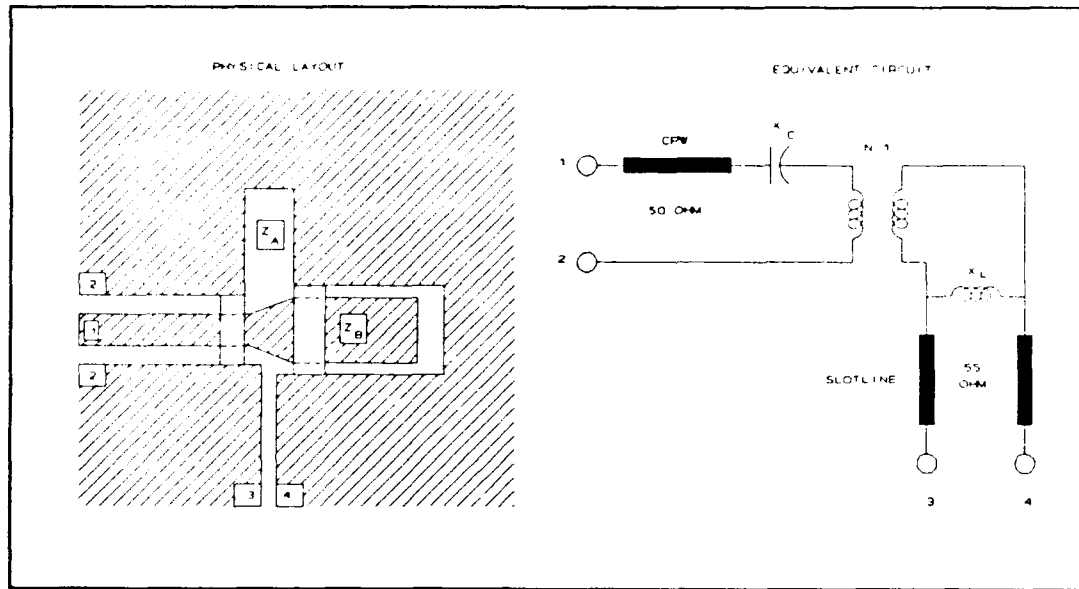


Figure 5.9 Planar balun used in the MMIC doubler (Fouad Hanna, 1982).

where Z_B is the characteristic impedance of the open stub line (28Ω), L is the physical length of the stub ($173 \mu\text{m}$), and β is $2\pi/\lambda_g$. The tuning reactance X_L is formed by the short circuit slotline stub:

$$X_L = jZ_A \tan\left(\frac{\beta L}{2}\right) \quad (5-6)$$

where Z_A is the characteristic impedance of the shorted stub line (110Ω), and L is the physical length of the stub ($188 \mu\text{m}$). Air bridges are used for current continuity as shown in Fig. 5.9. $|S_{11}|$ and $|S_{21}|$ are presented in Figs. 5.10 and 5.11 respectively.

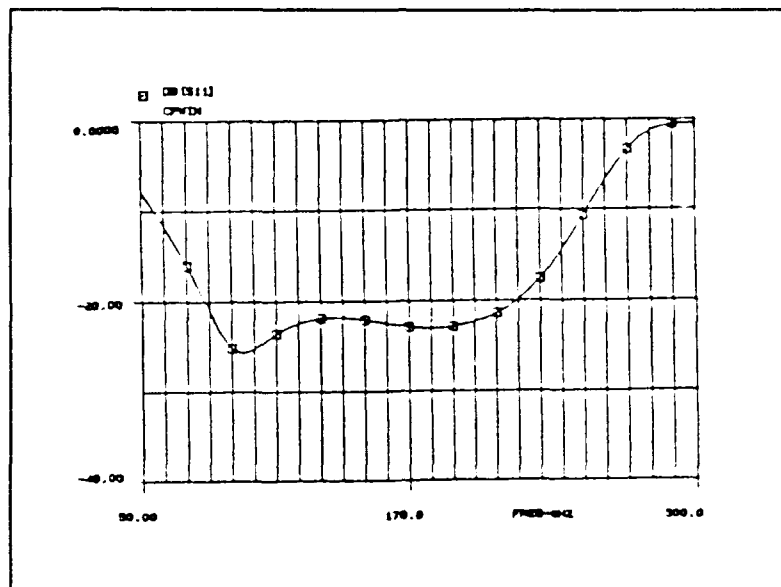


Figure 5.10 Computed $|S_{11}|$ for CPW-Slotline equivalent circuit of Fig. 5.9.

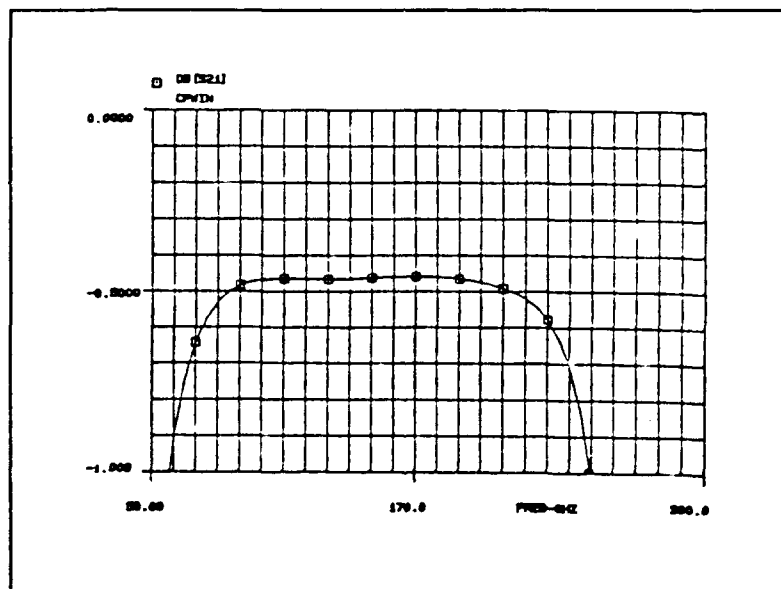


Figure 5.11 Computed $|S_{21}|$ for CPW-Slotline equivalent circuit of Fig. 5.9.

5.4.4 Slotline Characterization

The slotline, which is primarily needed for realization of the ANTI-PARALLEL/SERIES doubler configuration, was analyzed both theoretically and experimentally. For standard slotline, the dielectric constant and

impedance calculations are from Cohn (Cohn, 1969) with closed-form expressions presented by Garg and Gupta (Garg, 1976). The results compare quite well with the transverse resonance method described by Gupta, Garg, and Bahl (Gupta, 1979). There is little information in the literature on the effects of conductor thickness. Katazawa (Katazawa, 1973) indicates that the guide wavelength will increase with increased metal thickness, however no specifics were given. No slotline conductor or dielectric loss data was found other than brief mention (Shigesawa, 1988). No direct conductor-backed slotline data was found. A summary of the calculation procedure for slotline is given in Appendix E.

As a first-order check on the slotline and planar balun theory, a scale model consisting of a 1.5 inch length of $50\ \Omega$ CPW, a CPW-slotline balun, a 4 inch section of $55\ \Omega$ slotline, another CPW-slotline balun, and another 1.5 inch section of $50\ \Omega$ CPW was constructed using 2.5 mm thick Stycast HiK ($\epsilon_r = 12$), copper foil, and cyanoacrylate adhesive (see Fig. 5.12). The air bridges were made from No. 22 gauge wire soldered into place.

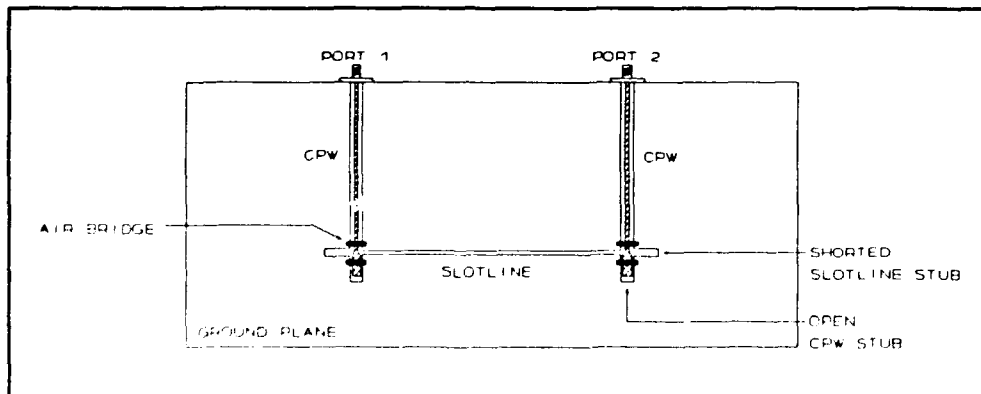


Figure 5.12 Sketch of back-to-back planar balun model.

The measured $|S_{12}|$ and $|S_{22}|$ data are presented in Figs. 5.13 and 5.14.

The measurements were made using the HP8510 VNA with reference planes at the coaxial connectors. The marker indicates the center operating frequency (22.9x scaled) with at least 43 percent bandwidth as defined by $RL > 15$ dB. The return loss was better than 20 dB over most of the band and the insertion loss was approximately 3 dB. Based on the data in Table 5.4, the 3 inches (total) of CPW line contributes about 1 dB of loss, hence the two baluns and the 4 inches of slotline contribute the remaining 2 dB. Note that the MMIC slotline lengths will be much shorter. It appears that the baluns and slotline performs as expected.

One very important outcome of the scale modelling was discovery of the adverse effects from back-side metallization of the slotline. Bottom

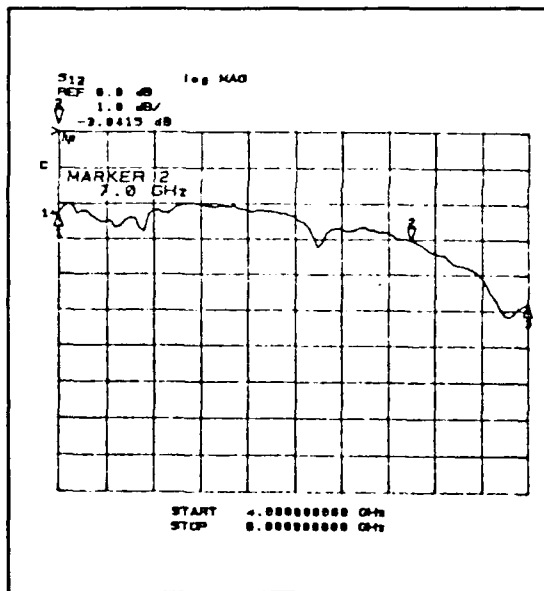


Figure 5.13 Measured $|S_{12}|$ data for the back-to-back balun.

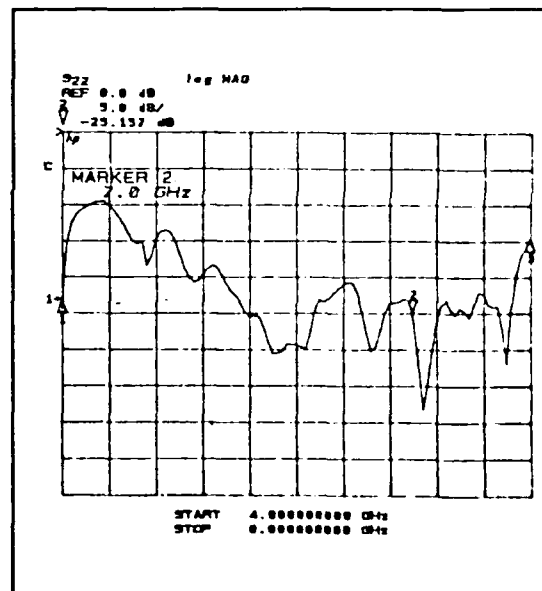


Figure 5.14 Measured $|S_{22}|$ data for the back-to-back balun.

surface metallization of the dielectric resulted in energy coupling into the unwanted slab-line mode. This moding could be "confined" by placing via holes along the slotline but problems are likely to occur near the

balun, hence conductor-backing cannot be used with slotline. The potential for inadvertent excitation of the dielectric mode in the MMIC mount is reduced by the inverted line scheme. However, great care is needed to keep CPW structures strictly symmetrical to avoid exciting the balanced mode.

5.4.5 Inverted Slotline and CPW arrangement

The inverted CPW scheme is shown in Fig. 5.15. This geometry

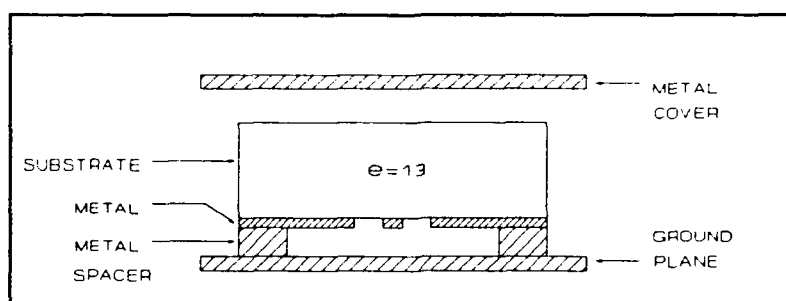


Figure 5.15 Inverted CPW configuration.

permits the application of standard CPW and slotline theory. Ground planes were placed above and below the entire balun/slotline test assembly and measurements of both $|S_{12}|$ and $|S_{22}|$ showed only a very small change compared with the open air measurements. This inverted scheme was chosen for both the MMIC 80/160 GHz doubler and the 80/240 GHz tripler circuitry.

5.5 Air Bridges and Monolithic Capacitors

5.5.1 Air Bridge Inductance

Air bridges used in the tee junction and elsewhere in the MMIC design can be modelled as a flat wire with rectangular cross section. The formula developed by Pettenpaul et al. (Pettenpaul, 1988) gives the solution to the inductance integral as a result of applying the method of

medium geometrical distances to calculate the static inductance of the conductor. The formula also includes the frequency-dependent current density over the conductor cross-section, as predicted by skin-effect theory, which results in a frequency dependent "inner" inductance (which is quite small). Numerical details are presented in Appendix E. The application of this theory to specific air bridge geometries is presented in Chapters Six, Seven, and Eight.

5.5.2 Monolithic Capacitors

The dielectric used for the monolithic capacitors is amorphous Silicon Nitride (Si_3N_4) which has a relative dielectric constant of 7.5. Parallel-plate structures with a Si_3N_4 thickness of 200 Angstroms have a capacitance of approximately $0.375 \text{ fF}/\mu\text{m}^2$. This result has been verified experimentally by S. Weinreb at Martin Marietta Laboratories.

5.6 CPW-to-Rectangular Waveguide Probe Design Study

Details of the probe design study can be found in Appendix F. The rudimentary results are summarized in Table 5.5, which includes scale model performance data for possible MMIC probe designs. The probes were oriented both transverse and longitudinally with respect to the direction of wave propagation. Each model uses WR-229 waveguide which scales as 22.9x for WR-10, 44.9x for WR-5, and 67.4x for WR-3 waveguide, where the scaled center frequencies are also given in Table 5.5. The probe chosen for the MMIC 80/160 GHz doubler and 80/240 GHz tripler input line is the inverted CPW transverse slab probe (Fig. 5.16 and Chapters Six and Seven) because 1) it forms a mechanically rigid structure, 2) the geometry is

compatible with practical GaAs substrate thickness, and 3) its bandwidth is very large. The conductor-backing requirements of the MMIC 31/94 GHz tripler (see Chapter Eight) required the CBCPW transverse slab probe in the output circuit (Fig. 5.16). This probe has been modelled independently by S. Weinreb at Martin Marietta Laboratories. He found the loss through two such MMIC-fabricated probes in a back-to-back arrangement connected with 5 mm of CBCPW to be 1.3 dB at 94 GHz (Weinreb, 1991). It is estimated that 0.6 dB is due to the CBCPW line (0.12 dB/mm) and 0.3 dB per probe.

Neither of the above probes can be used at 160 GHz or 240 GHz because the practical SI GaAs thickness would cause a prohibitively large discontinuity in the smaller waveguide. Hence, the inverted CPW transverse cantilevered probe (TYPE II with wire flag) which is also shown in Fig. 5.16, was chosen because 1) it is very easy to fabricate, 2) there is no high dielectric material in the waveguide, and 3) its bandwidth is very wide.

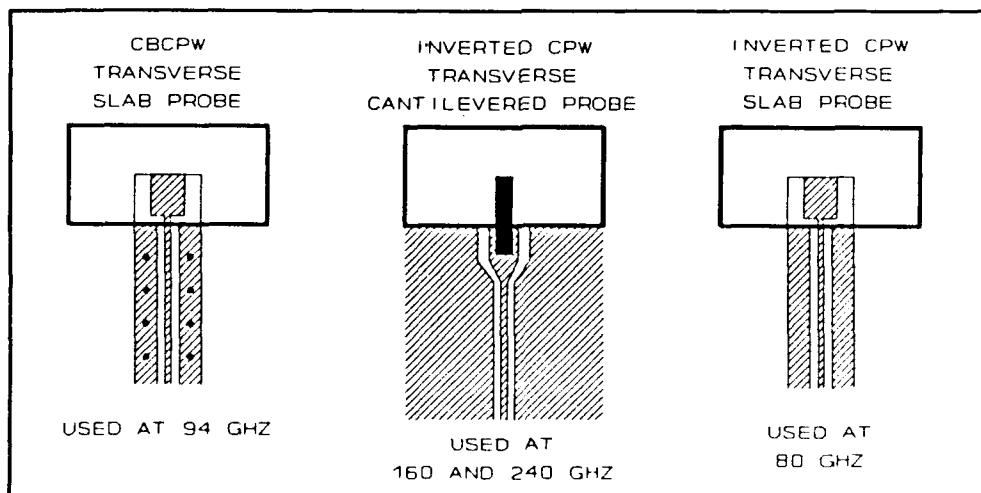


Figure 5.16 Cross-sectional sketch of all three probes used in the MMIC multiplier designs.

Table 5.5 Summary of the Probe Design Study				
Probe/ Orientation/ Line	Center Freq. [GHz]	Bandwidth [Percent]	Backshort Position mm FROM FLAG	Notes:
SLAB Transverse CPCPW	4.0 (92 GHz)	> 30	15	Coupling to dielectric mode @ 4.9 GHz
SLAB Longitudinal CPCPW	4.0 (92 GHz)	> 25	8 (probe edge)	Coupling to dielectric mode @ 4.9 GHz
SLAB Transverse Inv. CPW	3.5 (80.5 GHz)	31	19	
CANTILEVER Transverse CPCPW	3.8 (175 GHz)	> 30	20	Coupling to dielectric mode > 4 GHz
CANTILEVER Transverse Inv. CPW I (Probe: A)	4.15 (186 GHz) (279 GHz)	> 41	19	
CANTILEVER Transverse Inv. CPW II (Probe: B)	4.15 (186 GHz) (279 GHz)	> 41	18	
CANTILEVER Transverse Inv. CPW II (RIBBON)	3.65 (164 GHz) (246 GHz)	> 20	19	
CANTILEVER Transverse Inv. CPW II (WIRE)	3.6 (162 GHz) (243 GHz)	> 23	26	

5.7 Overview of the MMIC Fabrication Procedure

Fabrication of the MMIC multipliers was NOT part of this thesis, however since the microwave design included mask drawings, it was deemed important for completeness to include a condensed overview of the

fabrication process. The MMIC multiplier wafers were fabricated by S. Duncan and his group at the Martin Marietta Laboratories, Baltimore, MD.

The individual MMIC chip drawings called unit cells were drawn using AutoCAD⁶ and converted to GDS-II format using the STEP Electronics ASM 3500⁷ data translator. The group at Martin Marietta interfaced these unit cells with test devices and alignment markers thus completing the mask plate drawing. The mask plate set was made using electron-beam lithography.

The doped epitaxial GaAs was grown on base SI GaAs wafers (2 inches in diameter) using the Molecular-Beam Epitaxy (MBE) technique. The following summary of the MMIC multiplier fabrication process is courtesy of S. Duncan (Duncan, 1990). The use of mask plates are indicated in *italics*.

Front Side Processing (ALL MULTIPLIERS)

1. Plasma-Enhanced Chemical Vapor Deposition (PECVD) of 5000 angstroms of SiO₂.
2. Spin photoresist and expose *ohmic contact pattern*. Develop and etch oxide, then etch active n⁻ layer. Deposit ohmic contact metals: total metal thickness 2550 angstroms. Lift photoresist. Anneal ohmic contact. Electroplate Au onto ohmic contact (level with SiO₂).
3. Spin photoresist and expose *anode pattern*. Develop and etch SiO₂ to 4200 angstroms. Strip photoresist. Finish SiO₂ etch to GaAs and electroplate Pt and Au for anode. Spin photoresist and expose *anode pattern* again. Develop and deposit Ti and Au. Lift of unwanted metal.
4. Spin photoresist and expose *large mesa pattern*. Develop and etch SiO₂ and then etch n⁻ and n⁺⁺ GaAs. Strip photoresist.

⁶AutoCAD is a product of AUTODESK Inc.

⁷ASM 3500 is a registered trademark of STEP Electronics Inc.

5. Spin photoresist and expose *circuit metal pattern*. Develop and deposit 1500 angstroms each of Ti and Au. Lift off unwanted metal.
6. Deposit Si_3N_4 dielectric. Spin photoresist and expose *capacitor pattern*. Develop and RIE etch Si_3N_4 . Strip photoresist.
7. Spin photoresist and expose *air bridge anchor post pattern*. Develop and deposit electroplating base (Ti, Au, and Ti). Spin additional photoresist and expose *air bridge span pattern*. Develop and electroplate Au. Strip the span photoresist and etch unwanted electroplating base. Strip the anchor post photoresist.
8. If no backside processing is required (as in the 80/160 GHz doubler and 80/240 GHz tripler wafers), the backside is lapped to the desired chip thickness and the wafer is diced into individual MMIC multiplier chips.

Backside Processing (conductor-backed MMIC circuits only)

1. Lap wafer to desired thickness.
2. Spin photoresist and expose *transfer pattern*. Develop and etch transfer layer. Strip photoresist.
3. Spin photoresist and expose *via hole pattern*. Develop and RIE etch holes through SI GaAs substrate. Strip photoresist.
4. Deposit backside electroplating base (Ti, Au, Ti). Spin photoresist and expose *via-clear pattern*. Expose *backside electroplating pattern*. Etch Ti in electroplating base and electroplate Au. Strip photoresist. Etch unwanted electroplating base.
5. Wafer is diced into individual MMIC multiplier chips.

The complete description of each MMIC multiplier design is presented in Chapters Six through Eight.

CHAPTER SIX

The 80/160 GHz Frequency Doubler

6.1 Introduction

A monolithic 80/160 GHz frequency doubler was designed and fabricated. The circuit, fabricated on a semi-insulating GaAs substrate, contains not only the balanced Schottky-varactors but also the necessary embedding circuitry for coupling the input and output signals to rectangular waveguide. Fabrication was done at Martin Marietta Laboratories. Details of the design and evaluation of the frequency doubler are presented in this chapter.

6.2 Varactor Performance Study

The closed-form nonlinear analysis of Section 2.4 was applied to determine the multiplier performance as a function of the varactor design parameters. Hence, the application of eqns. (2-22) through (2-28) requires the following varactor parameters: 1) an abrupt-junction profile, 2) breakdown voltage, 3) built-in potential, 4) zero-biased capacitance, and 5) series resistance. With knowledge of the above parameters and with the maximum symmetrical pumping criterion, the analysis to predict the varactor efficiency, port impedances, and power levels for a specific frequency multiplier (multiplication factor and operating frequency) can be completed. These varactor parameters are directly related to the varactor fabrication variables.

There are two principal varactor fabrication variables that govern multiplier performance: active layer impurity concentration, and the anode

diameter. It is these two variables coupled with the avalanche breakdown / punchthrough criterion, and skin effect arguments applied to the buffer layer, that will establish all other fabrication variables. Therefore, it is important to carefully examine the multiplier performance as a function of these variables.

The varactor performance study examines the 80/160 GHz doubler performance (for maximum varactor efficiency at each point) of a single varactor having anode diameters ranging from 6 to 12 microns and active layer impurity concentrations ranging from 10^{16} to 10^{17} cm^{-3} . The results are presented in Table 6.1 and also in graphical form. The output power (Fig. 6.1), the varactor efficiency (Fig. 6.2), the input resistance (Fig. 6.3), and the output resistance (Fig. 6.4) are presented for the given range of anode diameters and active layer impurity concentrations.

TABLE 6.1 80/160 GHz Varactor Doubler Study (single varactor)											
$N_d \cdot 10^{16}$ [cm^{-3}]	d_a [μm]	L_c [μm]	V_{br} [v]	C_{jo} [fF]	C_{avg} [fF]	R_i [Ω]	R_{in} [Ω]	R_{out} [Ω]	P_{abs} [mW]	P_{out} [mW]	Var. Eff. [%]
1.0	6	3.0	64	8.6	1.9	88.9	200.7	310.0	99	41.7	42.0
	8			15.3	3.4	50.0	113.7	174.8	178	73.6	41.4
	10			23.9	5.4	32.0	73.4	112.3	281	113.9	40.5
	12			34.5	7.7	22.2	51.5	78.3	410	162.3	39.6
2.5	6	1.4	33	13.6	4.1	18.5	77.3	133.5	47	29.8	62.9
	8			24.2	7.3	10.4	44.2	75.5	86	52.0	60.5
	10			37.8	11.5	7.7	28.9	48.7	138	79.4	57.4
	12			54.5	16.5	5.6	20.6	34.1	206	111.5	54.2
5.0	6	0.8	20	19.2	7.2	6.9	41.2	73.8	31	22.1	71.2
	8			34.3	12.9	4.3	23.8	41.8	57	38.1	66.4
	10			53.5	20.1	3.1	15.8	27.0	94	57.2	60.6
	12			77.1	28.9	2.5	11.5	19.1	114	78.2	54.0
7.5	6	0.7	15	23.6	10.0	4.1	29.1	52.6	25	18.4	73.0
	8			42.0	17.8	2.7	17.1	29.9	48	31.4	66.1
	10			65.6	27.9	2.1	11.5	19.5	80	46.3	58.1
	12			94.4	40.1	1.6	8.6	13.8	125	62.2	49.6
10.0	6	0.5	13	27.3	12.5	3.0	23.3	42.1	23	16.8	72.9
	8			48.5	22.2	2.1	13.8	24.0	44	28.2	64.3
	10			75.7	34.7	1.7	9.4	15.7	75	41.1	54.9
	12			109.0	50.0	1.5	7.1	11.2	120	54.5	45.5

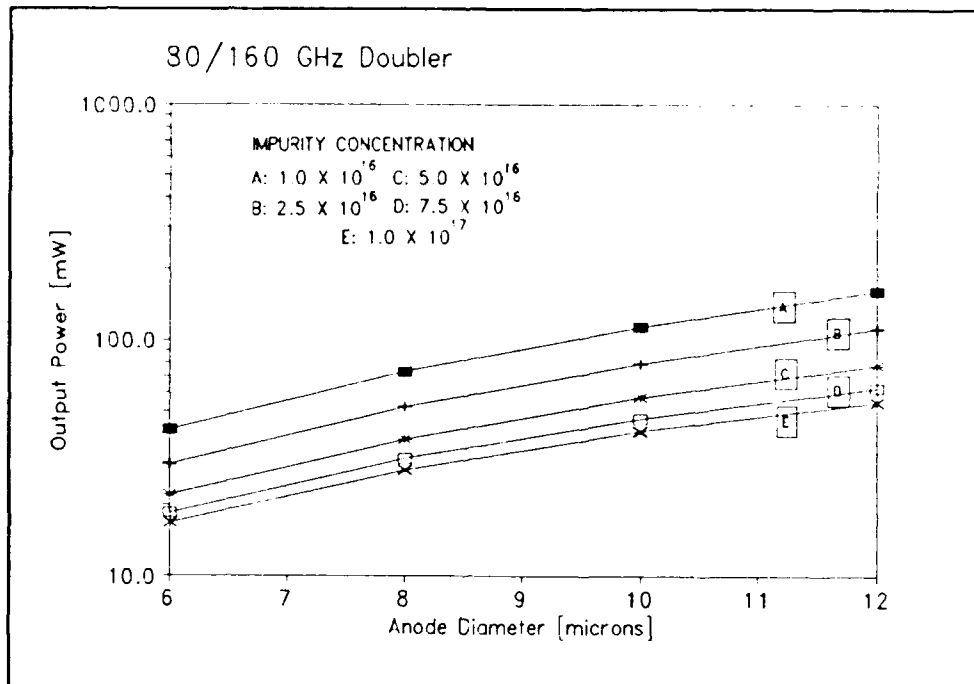


Figure 6.1 Calculated output power as a function of anode diameter. Parameter: active layer impurity concentration.

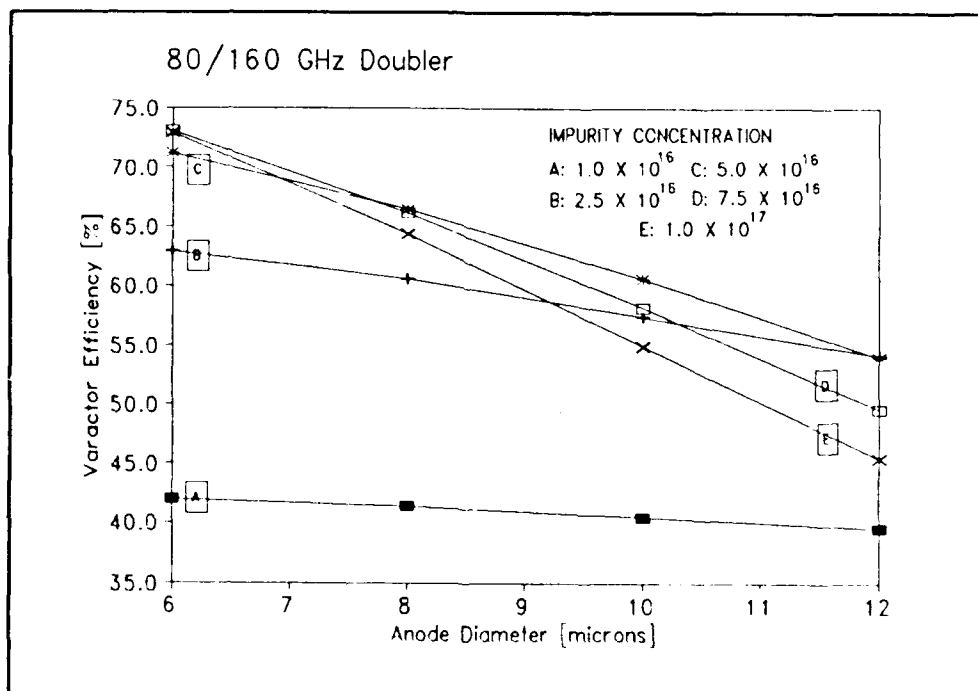


Figure 6.2 Calculated varactor efficiency as a function of anode diameter. Parameter: active layer impurity concentration.

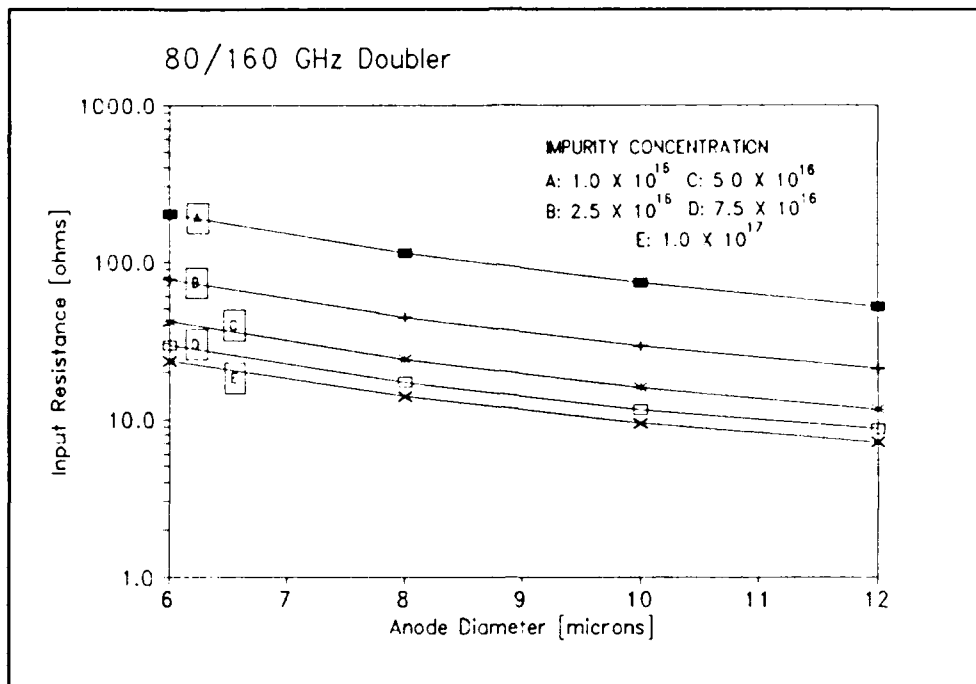


Figure 6.3 Calculated input resistance as a function of anode diameter. Parameter: active layer impurity concentration.

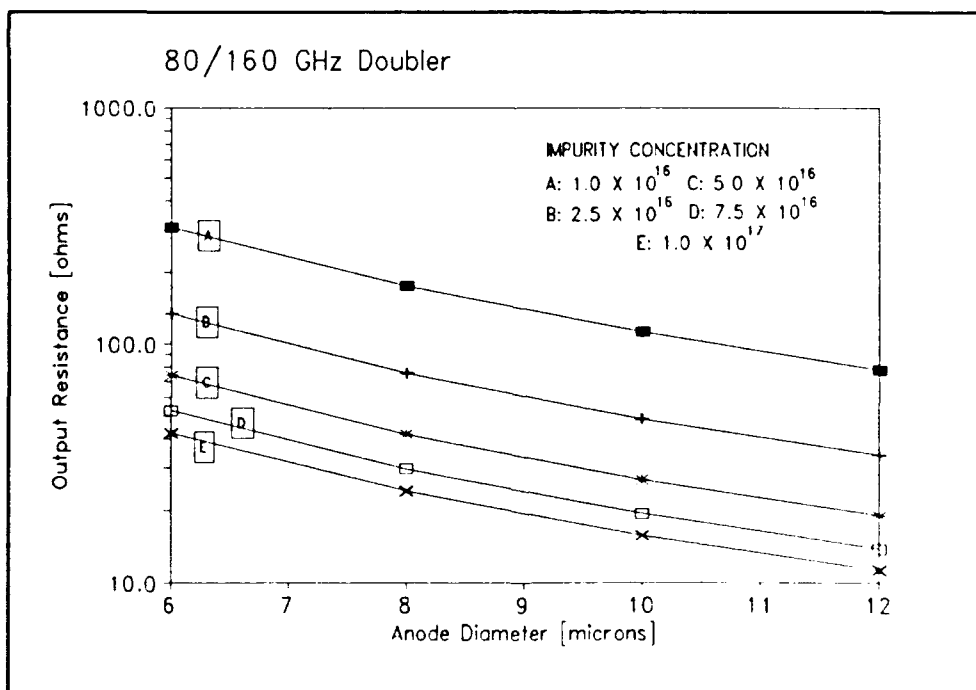


Figure 6.4 Calculated output resistance as a function of anode diameter. Parameter: active layer impurity concentration.

Fig. 6.5 shows the average junction capacitance (under the maximum symmetrical voltage swing) as calculated from eqn. (2-24).

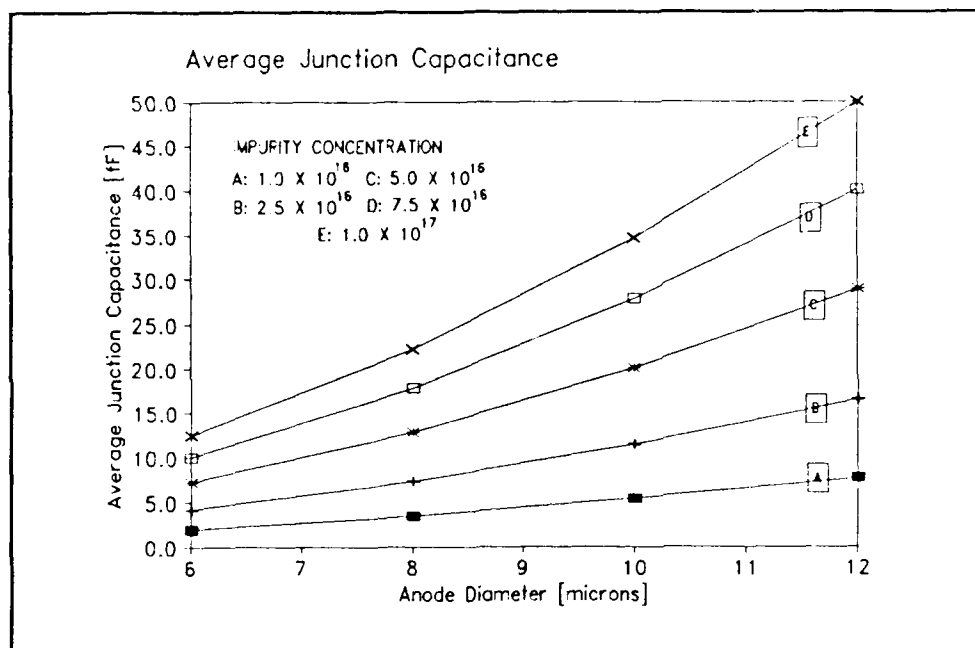


Figure 6.5 Average junction capacitance as a function of anode diameter. Parameter: active layer impurity concentration.

The above survey is for a single varactor, however since a balanced varactor arrangement (see Chapter Four) was also used in this doubler design, all power levels are twice that shown in the figures.

The doubler was designed for $P_{out} = 40$ mW per varactor. Examination of Fig. 6.1 indicates that a P_{out} of 40 mW is possible for many combinations of impurity concentration and anode diameter. However, since the goal was to provide high varactor efficiency with reasonable embedding impedances, curve D in Fig. 6.2, $n_d = 7.5 \times 10^{16} \text{ cm}^{-3}$, was chosen. Correspondingly, curve D in Fig. 6.1 indicates that a P_{out} of 40 mW is possible with an anode diameter of approximately 9 microns. The input and output impedances can easily be matched to 50Ω by relatively simple embedding circuitry.

The following varactor was chosen for the 80/160 GHz doubler:

FABRICATION VARIABLES:

Anode Diameter: 9 μm
Junction Profile: ABRUPT
Act. imp. level: $1.5 \times 10^{16} \text{ cm}^{-3}$
Active thickness: 0.6 μm
Buffer thickness: 2.0 μm
Buffer imp. lev.: $> 4 \times 10^{18} \text{ cm}^{-3}$

VARACTOR PARAMETERS:

$C_{jo} = 53 \text{ fF}$
 $C_{avg} = 23 \text{ fF}$
 $V_{bi} = 1.0 \text{ volts}$
 $V_b = -15 \text{ volts}$
 $R_s = 3.5 \text{ ohms}$

The operating point for best 80/160 GHz doubler performance using this SINGLE varactor is as follows:

Bias voltage:	-7.5 volts	
Output power at 94 GHz:	40 mW	
Absorbed power at 31 GHz:	65 mW	
Power dissipation:	25 mW	
Varactor efficiency:	62 %	
Input impedance:	14 -j 86 ohms	$Q_{input} = 6.1$
Output impedance:	24 -j 43 ohms	$Q_{output} = 1.8$

The Siegel-Kerr program (see Section 2.5) was used to verify the above performance calculations and to gain additional information about the behavior of the tripler as a function of available input power and bias voltage. The results, presented in Table 6.2, show that both calculations are in close agreement at the maximum efficiency point where the bias is -7.5 volts and the input absorbed power is 65 mW. The output power versus reverse bias is also shown in Fig. 6.6 and the varactor efficiency versus reverse bias is also shown in Fig. 6.7.

The single device equivalent circuit approach allowed the above results to be applied directly to the balanced configuration, noting that independent biasing of the two Schottky varactors was necessary. The embedding circuitry was then designed around these specified varactors assuming that the parasitic shunt capacitance across the varactors is small in comparison to the average junction capacitance and hence was ignored for this initial design.

TABLE 6.2 Large-signal Nonlinear analysis of 80/160 GHz Doubler Using Siegel-Kerr Program					
FIXED EMBEDDING IMPEDANCES:					
INPUT: $14 + j86$			OUTPUT: $24 + j43$		
BIAS VOLTAGE [V]	AVAILABLE POWER [mW]	ABSORBED POWER [mW]	OUTPUT POWER [mW]	INPUT IMPEDANCE [OHMS]	VARACTOR EFF. [PERCENT]
-5	20	18.6	9.5	$8.2 - j85.4$	51.0
	40	38.0	21.2	$10.5 - j82.0$	55.8
	60	55.0	29.6	$11.8 - j79.2$	53.8
	80	69.5	35.5	$12.4 - j76.5$	51.1
-6	20	17.1	8.7	$8.0 - j92.9$	50.7
	40	38.9	22.6	$11.0 - j89.4$	57.9
	60	59.8	34.6	$12.9 - j86.8$	57.8
	80	79.4	43.7	$14.0 - j84.3$	55.1
-7	20	12.3	5.7	$7.1 - j100$	46.1
	40	33.3	19.2	$10.5 - j96.7$	57.6
	60	55.5	33.5	$12.9 - j94.1$	60.4
	80	77.2	46.0	$14.6 - j91.9$	59.6
-8	20	7.6	2.9	$5.9 - j108$	38.0
	40	23.8	12.8	$9.0 - j104$	53.9
	60	44.9	26.9	$11.8 - j101$	60.0
	80	66.8	41.2	$14.1 - j98.9$	61.7

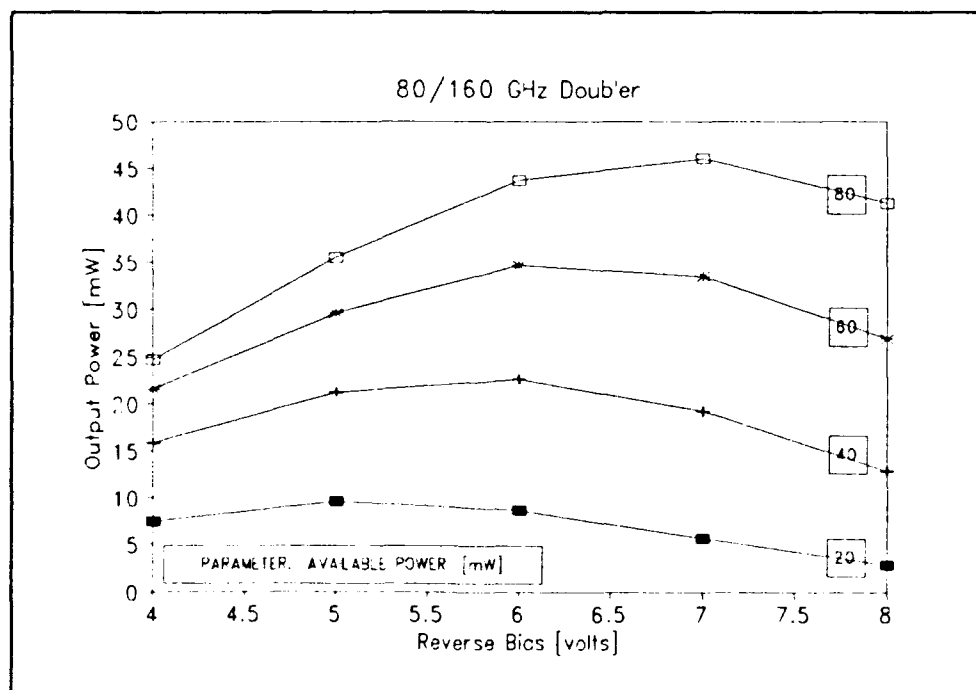


Figure 6.6 Doubler output power versus reverse bias for available powers of 20, 40, 60, and 80 mW.

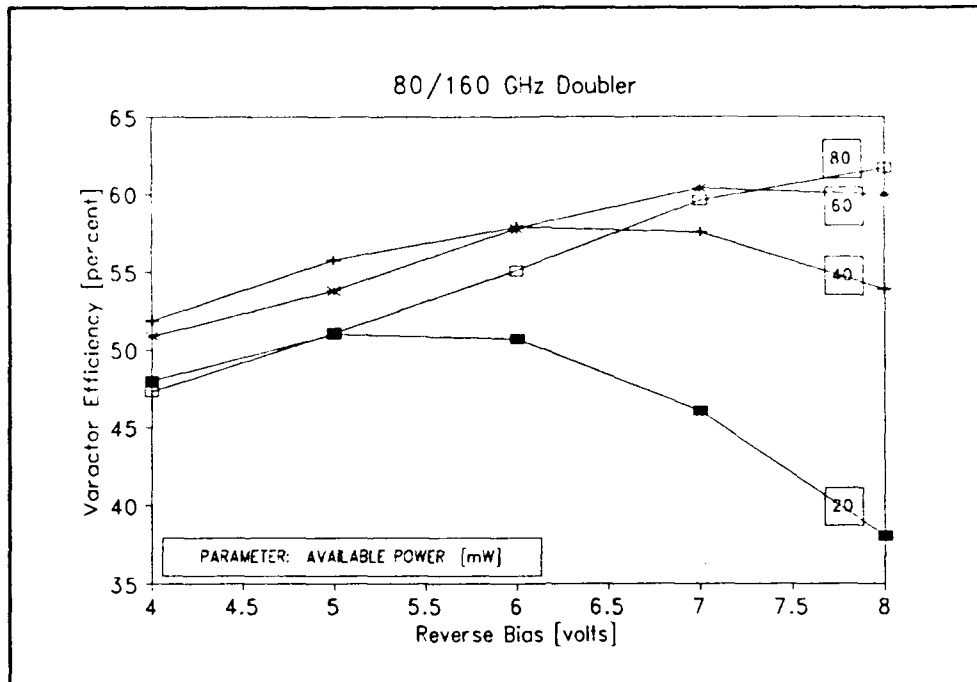


Figure 6.7 Varactor efficiency versus reverse bias for available powers of 20, 40, 60, and 80 mW.

6.3 Monolithic Circuit Design and Realization

Coplanar waveguide (CPW) and slotline were chosen as the planar transmission lines of this doubler design. The nature of the anti-parallel/series arrangement requires a balanced transmission line at the output frequency. Slotline is ideal for such application, however since the design is considered "on-chip cascable", a balun was used in the output circuit to transform the slotline back to the CPW which could, for example, drive a higher frequency doubler on the same chip. (Without the requirement of cascability, a slotline/finline transition to rectangular waveguide could be instituted). Complete details of the CPW line characteristics and discontinuities (including air bridge inductance) are presented in Chapter Five and Appendix E. The CPW transverse slab probe

(see Appendix F) was used to couple the input signal to a rectangular waveguide (WR-10). The inverted CPW transverse cantilevered probe (see Appendix F) was chosen for output coupling to a WR-5 rectangular waveguide.

The input and output circuits were designed to provide conjugate-matched embedding impedances to that predicted by the analysis of Section 6.2. Because high frequency applications of CPW and related discontinuities (tee junctions, stubs, etc.) are not well understood beyond the data from scale models presented in this thesis, a "minimum circuit complexity" approach was adopted, and therefore only relatively simple, narrow bandwidth embedding circuits were considered for the initial design.

A scale drawing of the top side lithography is shown in Fig. 6.8. Fig. 6.9 is a close-up of the region near the varactors. There is no bottom side lithography in this design, hence no via holes were required. For the purpose of discussion, the circuit can be separated into two sections: 1) the input network including bias lines (80 GHz), and 2) the output network (160 GHz).

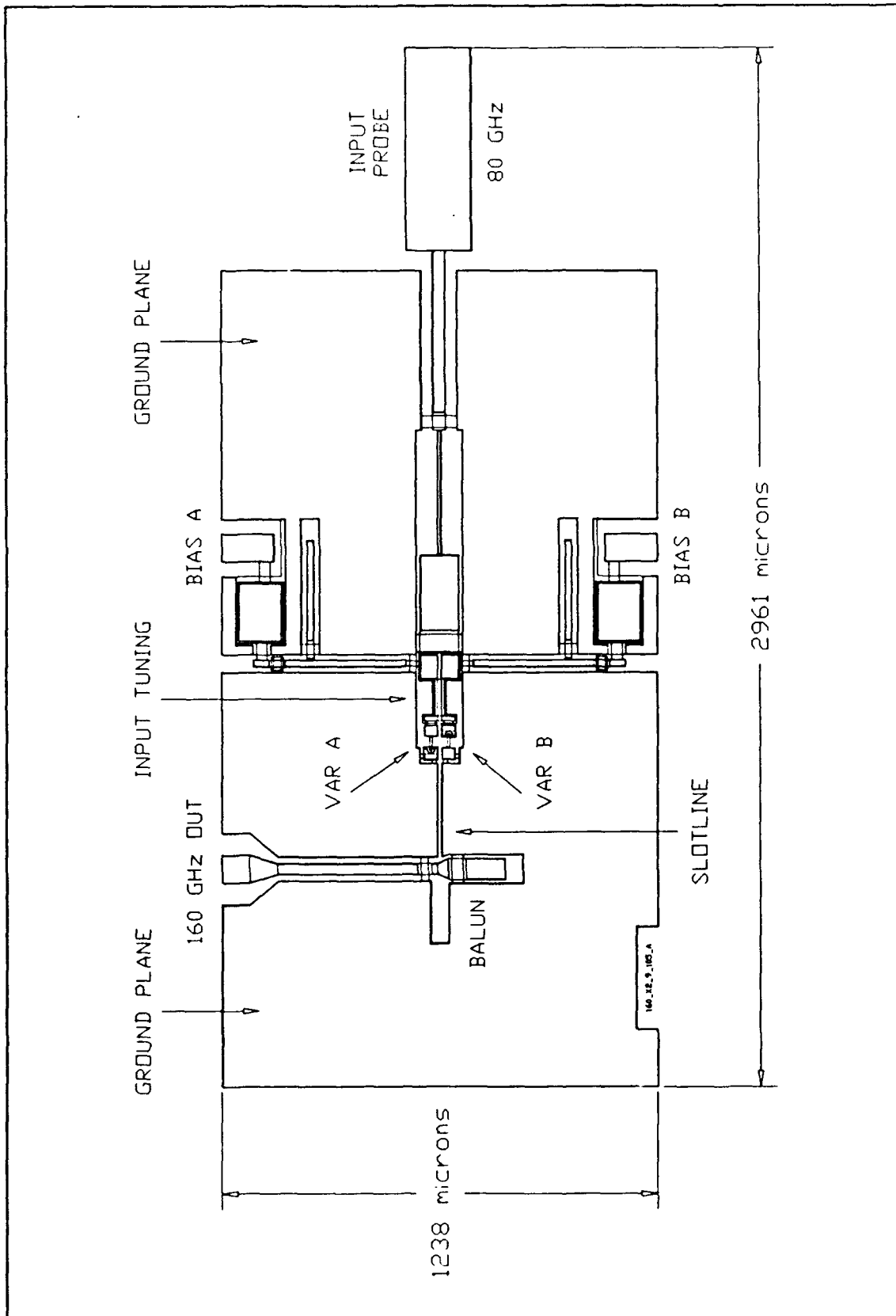


Figure 6.8 Scale drawing of the monolithic 80/160 GHz frequency doubler.

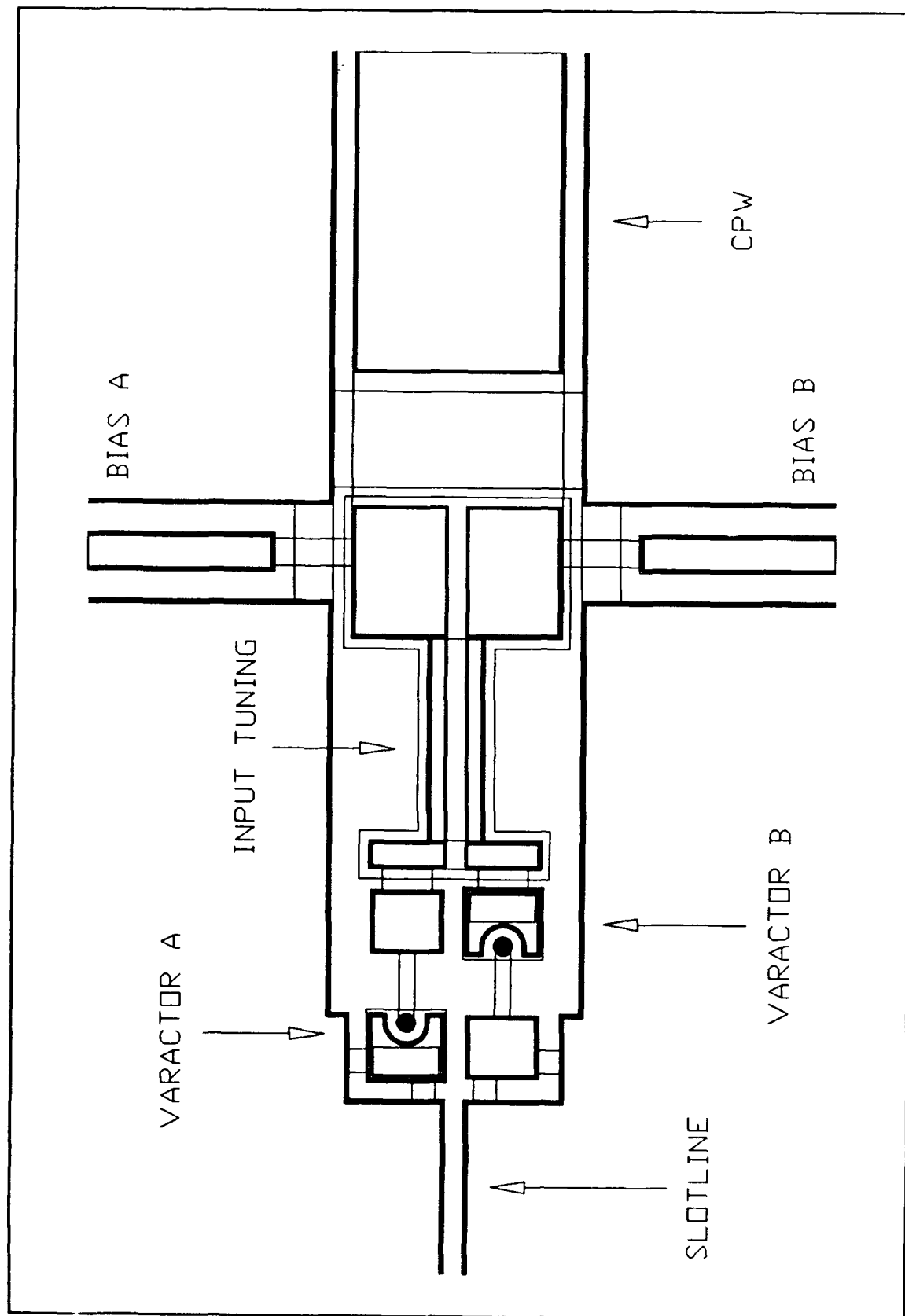


Figure 6.9 Close up of the monolithic 80/160 GHz doubler showing the varactor region.

6.3.1 Input Network including Bias Lines

The equivalent circuit for the input section is shown in Fig. 6.10.

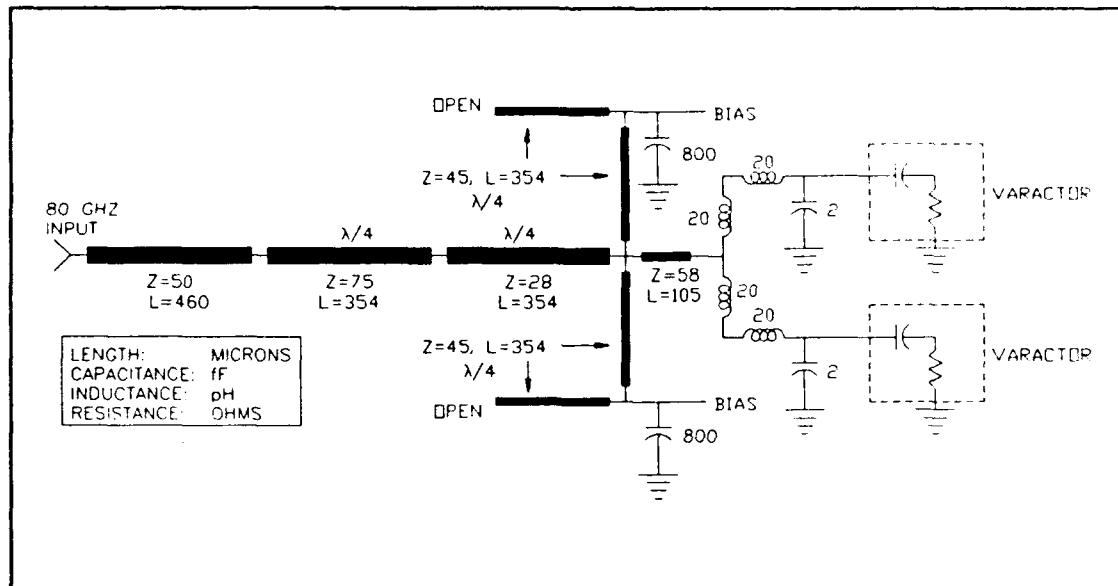


Figure 6.10 Equivalent circuit of the input section including the bias lines.

The finger inductance near the anodes provides about $+j10$ ohms toward resonating the reactance of the average junction capacitance at the input frequency (80 GHz). According the results of Section 6.2, an additional 0.25 nH of inductance is also needed (preferably near the varactors for bandwidth considerations), hence a short section (105 microns) of 58 Ω CPW was used to yield an impedance of 5 Ω real. The symmetrical bias lines are attached to the main CPW at this point. The 5 Ω real impedance is transformed to 50 Ω using a two-stage quarter-wave transformer ($Z = 28 \Omega$, length = 354 μm line followed by a section of $Z = 75 \Omega$, length = 354 μm line). A short section of 50 Ω line (length = 460 μm) connects the transformer to the input probe. The input probe flag width is 187 microns, length is 578 microns, and the gap between the flag and the ground plane metallization is 55 microns.

Each bias line consists of a quarter-wavelength $45\ \Omega$ open stub (CPW with length = 354 μm) which gives an RF short where the dc bias wire bonding pad is attached. A filter capacitor of about 800 fF (using SiN dielectric) is also attached at this point. The bias line is attached to the main CPW via an additional quarter-wavelength (80 GHz) CPW section thus producing an RF open at the tee junction of the bias line and the main CPW. Independent biasing is achieved by a stacked metal/dielectric/twin-metal strip along the main CPW as shown in Fig. 6.11. The two strips yield independent dc paths to each varactor while the entire structure appears to RF signals as a single coplanar waveguide due to the large capacitive coupling of the strips. The electrically small geometry of the structure as compared with the operation wavelength insures that unwanted moding (excitation of the parallel-plate line formed by the stacked structure) will not occur over the frequency range of interest. The parallel plate capacitance is $0.375\ \text{fF}/\mu^2$ (see section 5.5.2). The input circuitry is isolated from the 160 GHz signal by circuit balance.

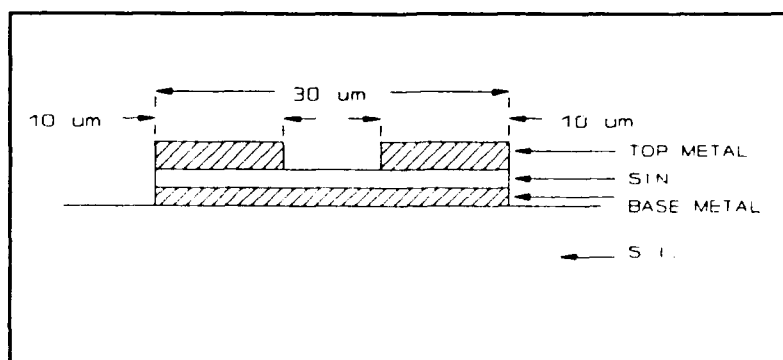


Figure 6.11 Main CPW structure for independent dc biasing of the varactors.

A summary of the input network's transmission line characteristics (including loss) is presented in Table 6.3. An estimate of the total

circuit loss through the input network (including a worst-case estimate of 0.5 dB loss through the input probe) is also given.

TABLE 6.3 Summary of CPW Characteristics Input Network.					
LINE	w [um]	s [um]	LENGTH [um]	LOSS/LEN. [dB/um]	LOSS [dB]
50 ohm	100	36	460	.000314	.14
75 ohm	130	10	354	.000534	.19
28 ohm	130	120	354	.000564	.20
58 ohm	130	29	105	.000244	.03
45 ohm	50	18	4x 354	.000574	.82
Estimated total circuit loss in the input network: (Includes 0.5 dB loss through input probe)					1.88 dB

6.3.2 Output Network

The equivalent circuit for the output network is shown in Fig. 6.12.

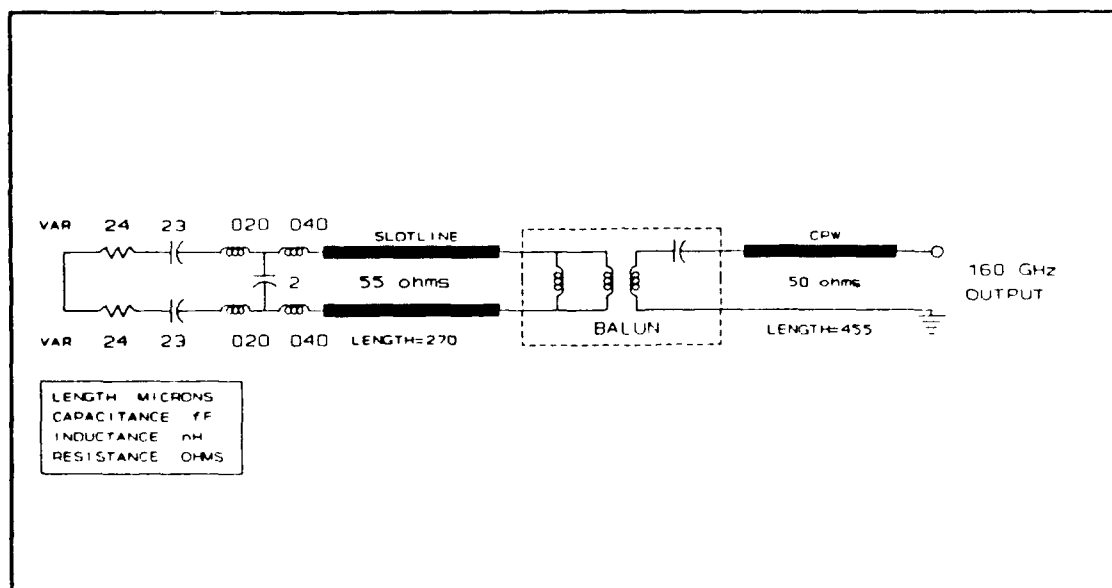


Figure 6.12 Equivalent circuit for the output network.

The varactor finger inductance nearly resonates the average junction capacitance at the output frequency (160 GHz) so additional compensation

is not necessary. The varactors (which appear in series) match the impedance of a 55 Ω slotline (slot width = 10 μm , length = 180 μm). The slotline is transformed to 50 Ω CPW through the balun structure. The balun consists of a shorted slotline stub ($Z = 92 \Omega$, length = 180 μm) and an open CPW stub ($Z = 30 \Omega$, length 163 μm). The balun is connected to the output probe via a 455 μm length of 50 Ω CPW. The output circuit is isolated from the input circuit through circuit balance.

A summary of the transmission line characteristics for the output network are presented in Table 6.4. An estimate of the total circuit loss through the output network is also given (an additional 0.5 dB of loss for the rectangular waveguide probe is included).

TABLE 6.4 Summary of CPW & Slotline Characteristics Output Network					
LINE	w [μm]	s [μm]	LENGTH [μm]	LOSS/LEN. [dB/ μm]	LOSS [dB]
55 ohm	10	---	270	?	.30
92 ohm	50	---	180	?	.10
30 ohm	100	80	163	.000597	.10
50 ohm	95	23	455	.000711	.32
Estimated total circuit loss in the output network: (includes worst-case estimate of 0.5 dB for waveguide probe)					1.3 dB

6.3.3 Embedding Impedances and Overall Doubler Performance

The embedding impedances of both networks were examined as a function of frequency. The circuit simulator TouchStone was used to calculate the embedding impedances of the input and output networks for 76/152, 80/160, and 84/168 GHz operation. These impedances are presented in Table 6.5.

TABLE 6.5 Embedding Impedances versus Frequency Balanced Doubler		
Pump Frequency	Embedding Impedances [ohms]	
	INPUT	OUTPUT
76 GHz	22.0 +j 50.0	26.8 + j 39.2
80 GHz	19.7 +j 78.8	24.0 + j 43.2
84 GHz	21.8 +j 88.2	24.4 + j 45.1

The embedding impedances presented in Table 6.5 together with the nonlinear analysis program of Siegel and Kerr were used to calculate the performance of the tripler as a function of frequency. Conductive losses in the embedding circuits were also included. The best performance at each frequency is shown in Table 6.6.

TABLE 6.6 Predicted Doubler Performance versus Frequency BALANCED OPERATION Siegel and Kerr Program					
Pump Frequency [GHz]	Bias Voltage [volts]	Available Power [mW]	Output Power [mW]	Var. Input Impedance [ohms]	Efficiency [percent]
76	-4	60	2.7	5.5 -j 85	4.5
80	-5	60	11.1	7.7 -j 82	18.5
84	-6	60	10.0	6.8 -j 83	16.6

The efficiencies presented in Table 6.6 are based on the monolithic doubler output power and the available power at the doubler input port. The 60 mW of available power was based on the 80 GHz klystron power source used for the experimental doubler evaluation.

6.4 Design Variations

Nine versions of the 80/160 GHz monolithic frequency doubler were fabricated at Martin Marietta Laboratories as described in Section 5.7 of this thesis. The variations, which are outlined in Table 6.7, show controlled variation in the two primary circuit variables: anode diameter and input tuning line length.

TABLE 6.7 80/160 GHz Doubler Variations		
CHIP NUMBER	ANODE DIA.	INPUT TUNING
160 X2 7 085 A	7	85
160 X2 7 105 A	7	105
160 X2 7 125 A	7	125
160 X2 8 085 A	8	85
160 X2 8 105 A	8	105
160 X2 8 125 A	8	125
160 X2 9 085 A	9	85
160 X2 9 105 A	9	105
160 X2 9 125 A	9	125

Also included on this wafer was a test structure used to characterize a sample varactor. The structure consists of a 8 micron diameter varactor in series with a coplanar waveguide (CoDiode structure) as shown in Fig. 6.13. Calibration structures having open anodes, shorted anodes, and open fingers were also fabricated on wafer. Wafer VD1-1 was completed on March 1, 1991, wafer VMD2-3 was completed on July 15, 1991, and wafer VDM2-2 was completed on August 1, 1991.

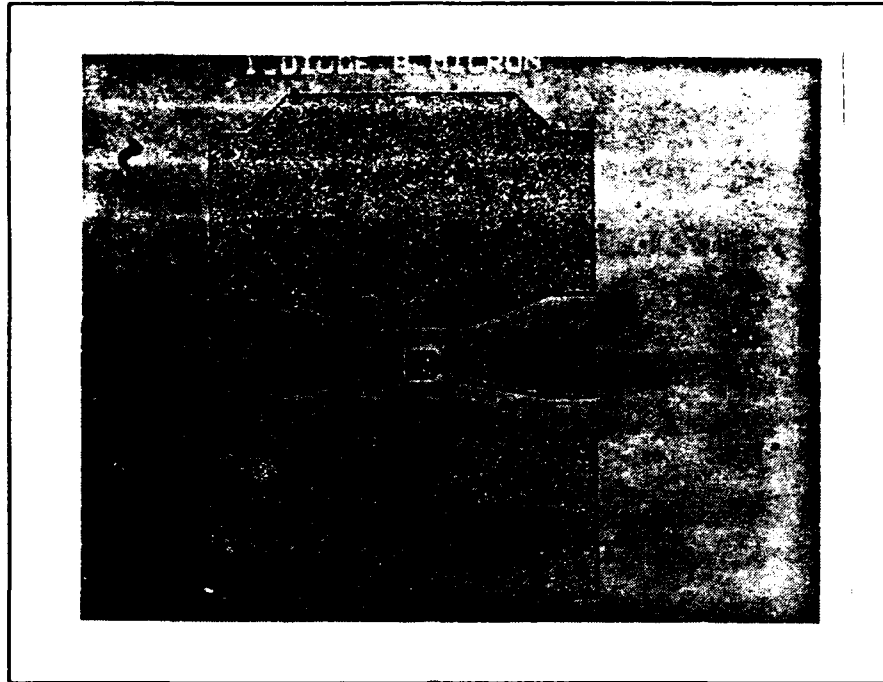


Figure 6.13 Photograph of the CoDiode structure (anode diameter is 8 μm).

6.5 Experimental Results

The doubler was evaluated on the basis of 1) a visual inspection, 2) dc characteristics, and 3) output power and efficiency versus frequency. All dc measurements were made on wafer or on an individual chip mounted on a glass microscope slide. A special mounting block was designed for the RF measurements to provide access to the input and output ports as well as for dc bias connections. A sketch of the mounting configuration is shown in Fig. 6.14.

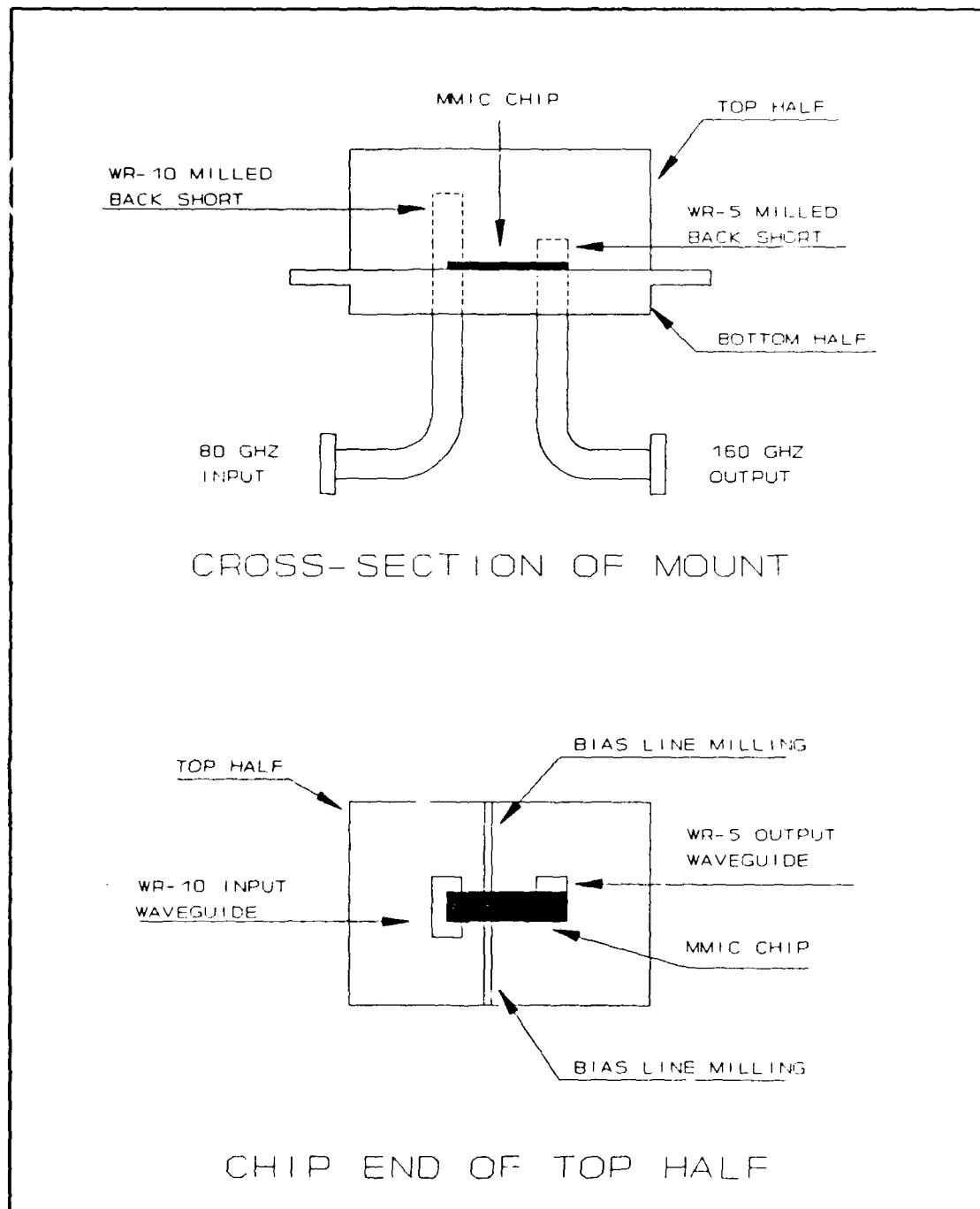


Figure 6.14 The block configuration used for RF testing the 80/160 GHz doubler (not to scale). Complete details are in Appendix G.

Fig. 6.15 shows a photograph of the upper and lower sections of the mount. A close-up of the chip area is shown in Fig. 6.16. Figure 6.17 shows the same region of the mount with the chip in place.

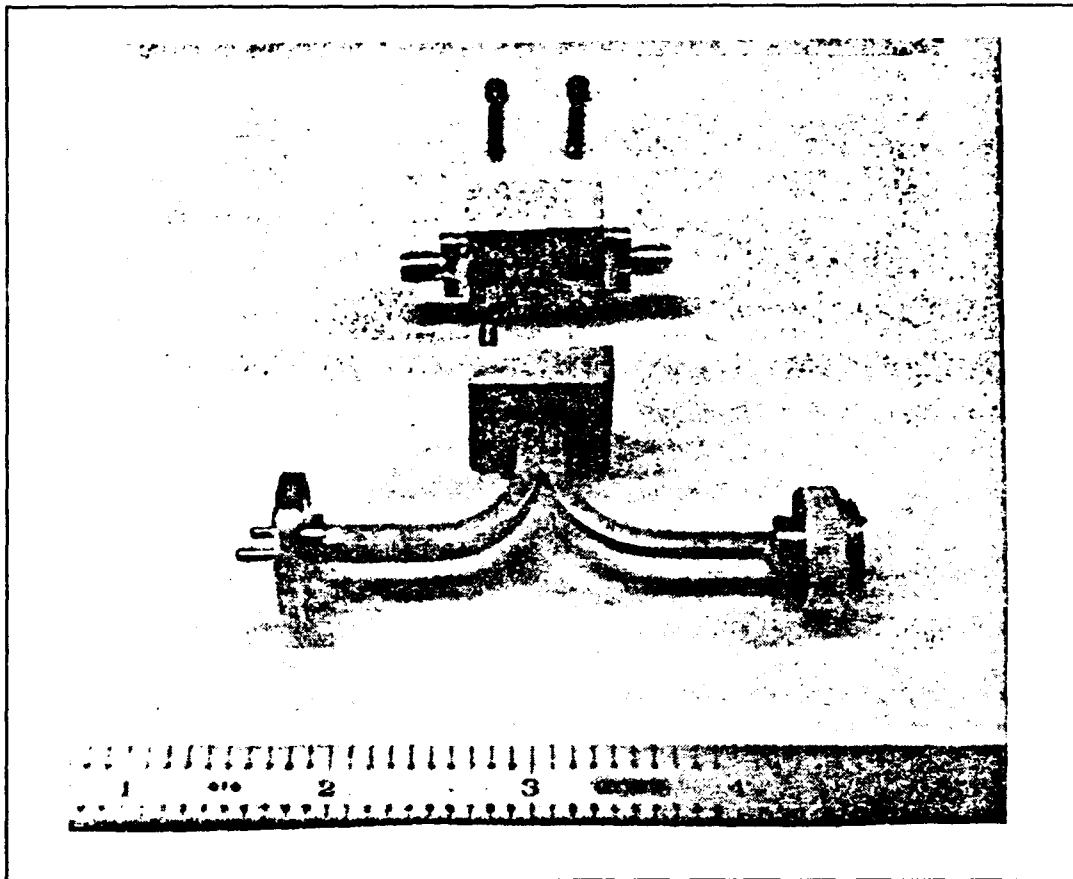


Figure 6.15 Side view of the 80/160 GHz doubler chip mounting block showing the upper and lower sections. The chip resides in the upper section (see Fig. 6.16 and 6.17).

Most of the mounting block was milled using conventional machining techniques. This excellent work was done by E. Spenceley and his group at the University of Virginia machine shop. The input and output rectangular waveguide backshorts were formed using electric-discharge machining (EDM) at the Martin Marietta machine shop. Originally only 10 to 20 mils deep, the backshorts were later milled completely through the upper section of the block so that adjustable contacting backshorts could be used. All dimensions and upper-lower block alignment were checked prior to block assembly.

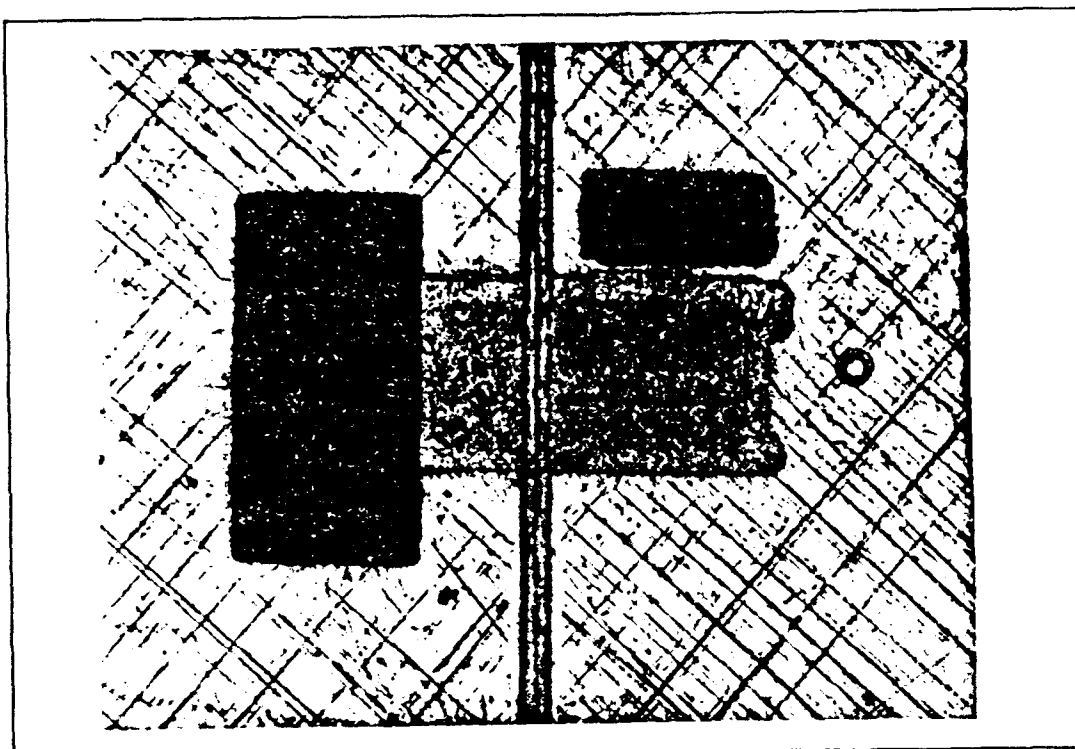


Figure 6.16 A close-up of the milled region in which the doubler chip is mounted.

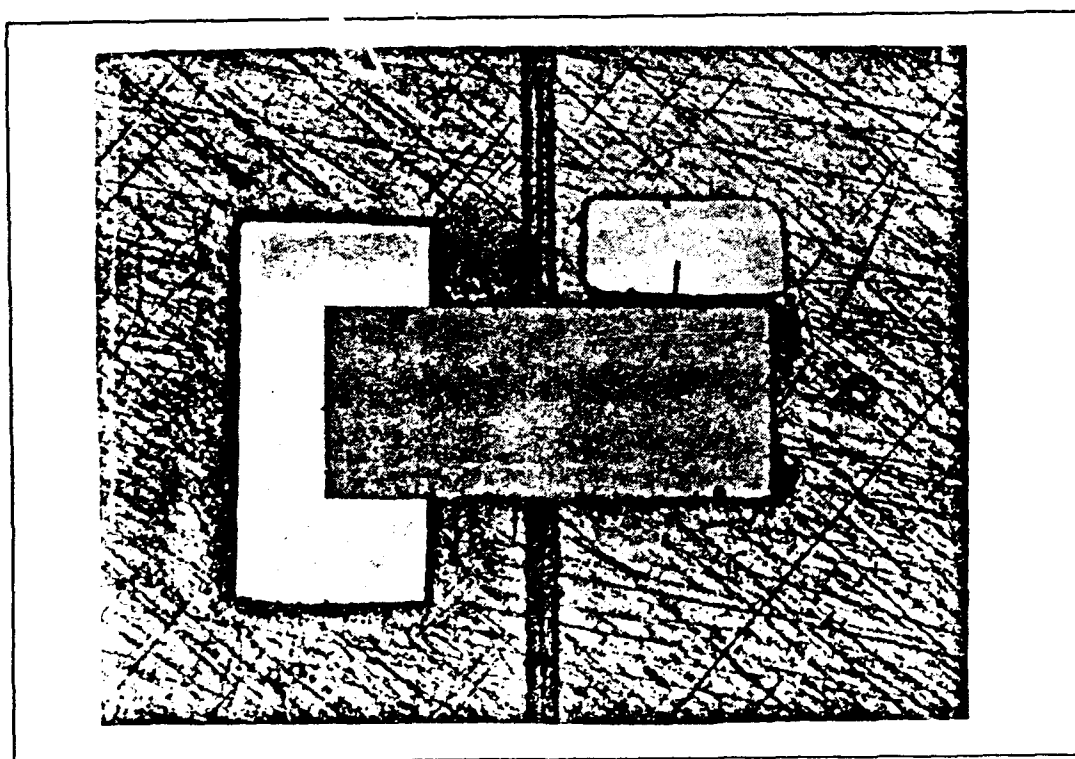


Figure 6.17 Same region of the mounting fixture as in Fig. 6.16 but with chip in place.

The lower section of the block was assembled as follows: A 90 degree E-bend was formed on a 3 inch section of WR-10 waveguide and a 90 H-bend was formed on the WR-5 waveguide. The waveguides were soldered to the lower section of the mounting block as shown, and mating surface of the block was then machined flat. Flanges were attached to the input and output waveguides and then the entire assembly was gold plated.

The upper section of the block was assembled as follows: First, Sears epoxy was used to fasten the 22 mil square chip capacitors (capacitance value irrelevant) into the recessed regions as shown and the epoxy was allowed to cure overnight. Next, a 250 mil length of 1.5 mil diameter gold wire was attached to each OSSM connector using TIX solder. The OSSM connector was attached to the block using two 2-56 machine screws. For strain relief, a small loop was made in the gold wire and the free end was attached to the chip capacitor using TIX solder.

The monolithic chip was mounted in the block as follows: A straight section of 0.7 mil diameter gold wire (length = 150 mils) was soldered to each bias bonding pad and to the output probe pad (by N. Horner, NRAO). (Initially the bias wires and the RF probe were attached using conductive epoxy, however this technique was abandoned due to the questionable uniformity of the epoxy mixture which led to poor mechanical connections upon curing). The probe wire was then cut so that the wire extended 12 mils beyond the edge of the chip. Silver epoxy was placed on the milled shelf region of the block and the chip was carefully pressed (top side down) into place. The entire block was then heated to 110 deg. C for approximately 30 minutes to cure the epoxy. Finally, the free ends of the 0.7 mil diameter gold bias wires were attached to the chip capacitors

using a small amount of indium thus completing the upper section assembly. The two halves were mated together, guided by two stainless-steel pins, and fastened by two 4-40 machine screws; the doubler was now ready for RF measurements.

Although three wafers of the 80/160 GHz doubler chips were fabricated, only the doublers of batch VMD2-2 were acceptable for RF measurements. The doublers of VMD1-1 had a very thin base metallization that caused very large resistances under the air bridges. The VMD2-3 was under plated which resulted in open anodes. Hence, all experimental results given in this section are for wafer VMD2-2.

6.5.1 Visual Inspection

Fig. 6.18 is a photograph of the 80/160 GHz monolithic frequency doubler top side processing as it appears prior to chip dicing (note that the 80/240 GHz tripler is also visible in the photograph). Fig 6.19 is a closeup view showing the bias lines, varactors, and part of the balun structure. Fig. 6.20 is a closeup of the varactor region. The lithography appears to be very well defined and no residuals of the fabrication process are evident. However, the results of overplating was clearly visible on many of the doublers. Metal near the anodes caused either short circuits or poor quality diodes to form between the anode and ohmic contact (in parallel with the designed varactor) thus rendering the chip unusable. In some cases, spots of overplated metal was visible along transmission lines hence causing line discontinuities. These chips were also rejected.

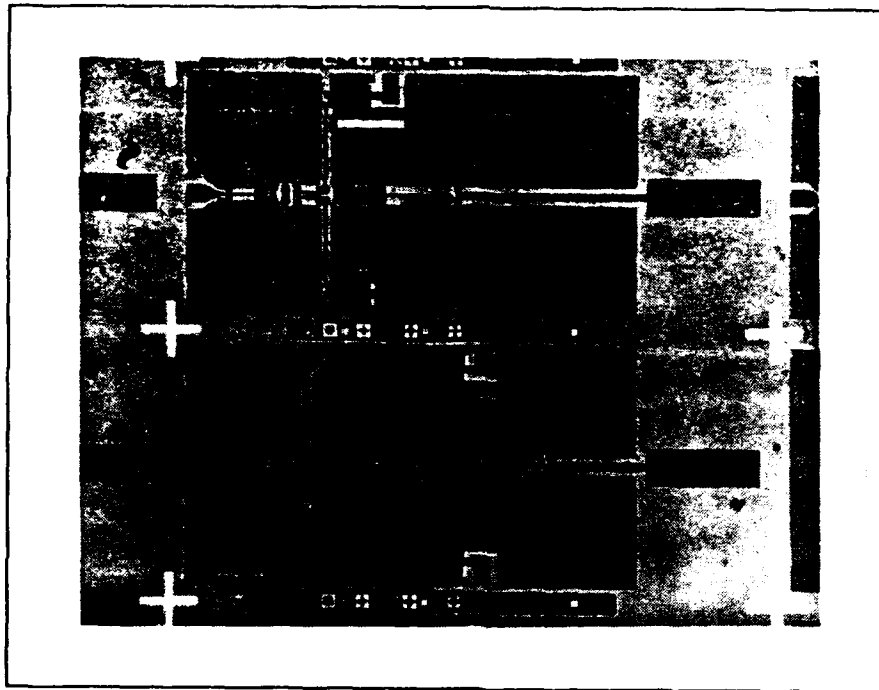


Figure 6.18 80/160 GHz doubler as it appears prior to dicing. The 80/240 GHz tripler is also visible.

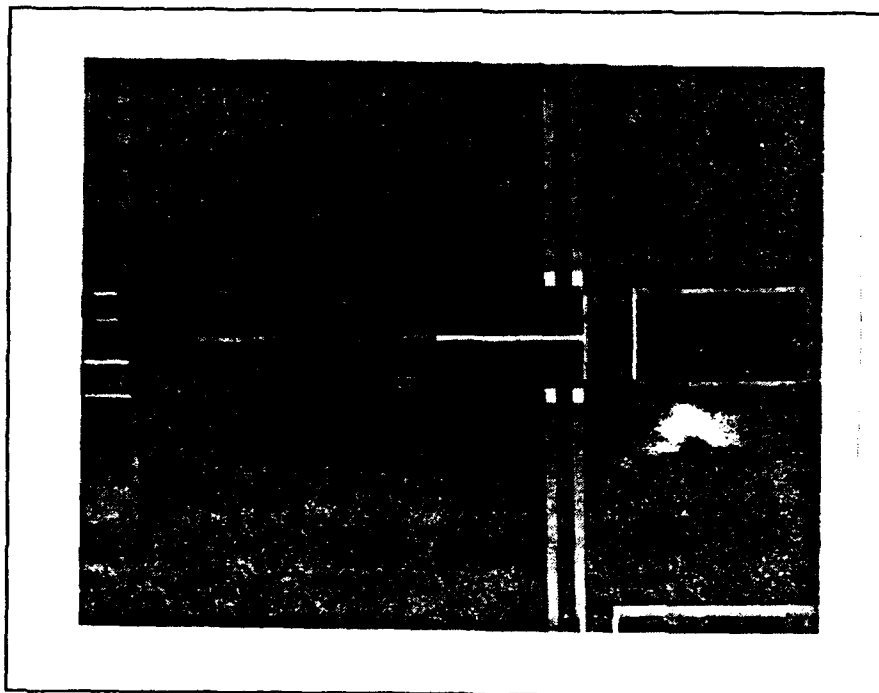


Figure 6.19 Close up of the bias lines, varactors, slotline and balun structures.

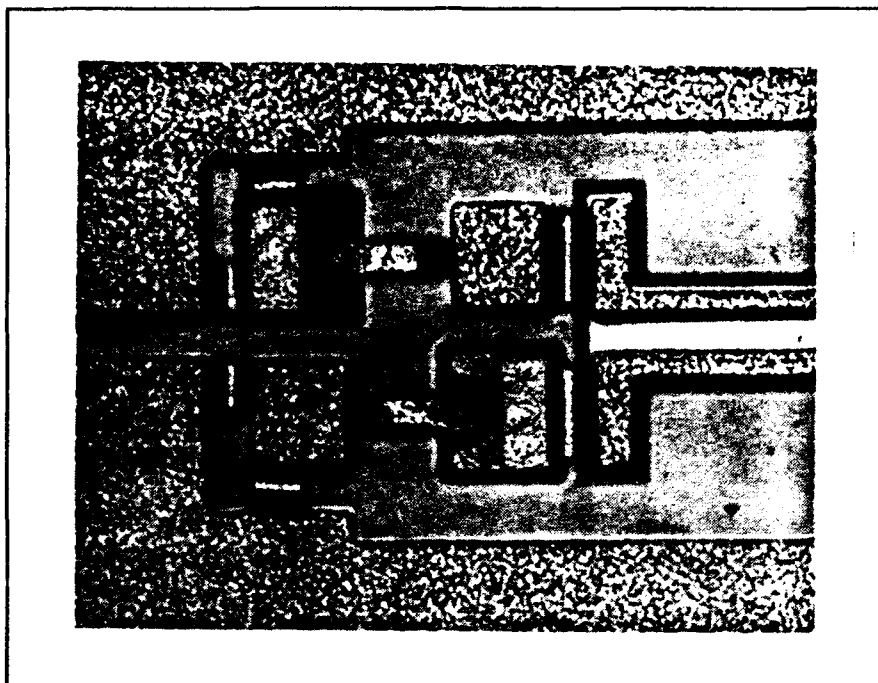


Figure 6.20 Close up of anode and ohmic contact of the 80/160 GHz doubler.

6.5.2 DC Characteristics

Forward Characteristics:

The forward I-V characteristics for a typical varactor measured on the doubler chip are as follows:

<u>Current</u>	<u>Voltage</u>
10 μ A	0.5447 v
100 μ A	0.6135 v
9 mA	0.7923 v
10 mA	0.8005 v

This data results in an R_s of 5 to 6 ohms and ΔV of 69 mV. Forward biased dc measurements were made using an HP 4145B Parameter Analyzer and a Cascade Microtech wafer prober. The varactor forward biased characteristics of the chips chosen for RF measurements, were confirmed using a current source and a four-wire probe.

Reverse Characteristics:

The typical reverse breakdown ($I = 100 \text{ uA}$) measured on the doubler varactors was between -10 to -12 volts. The typical capacitance-voltage characteristics, measured on the CoDiodes at 1 MHz, are presented in Fig. 6.21. These values compare well with the parallel-plate varactor model (see Section 2.3). For calibration, on-wafer CoDiodes having open anodes were used as a reference.

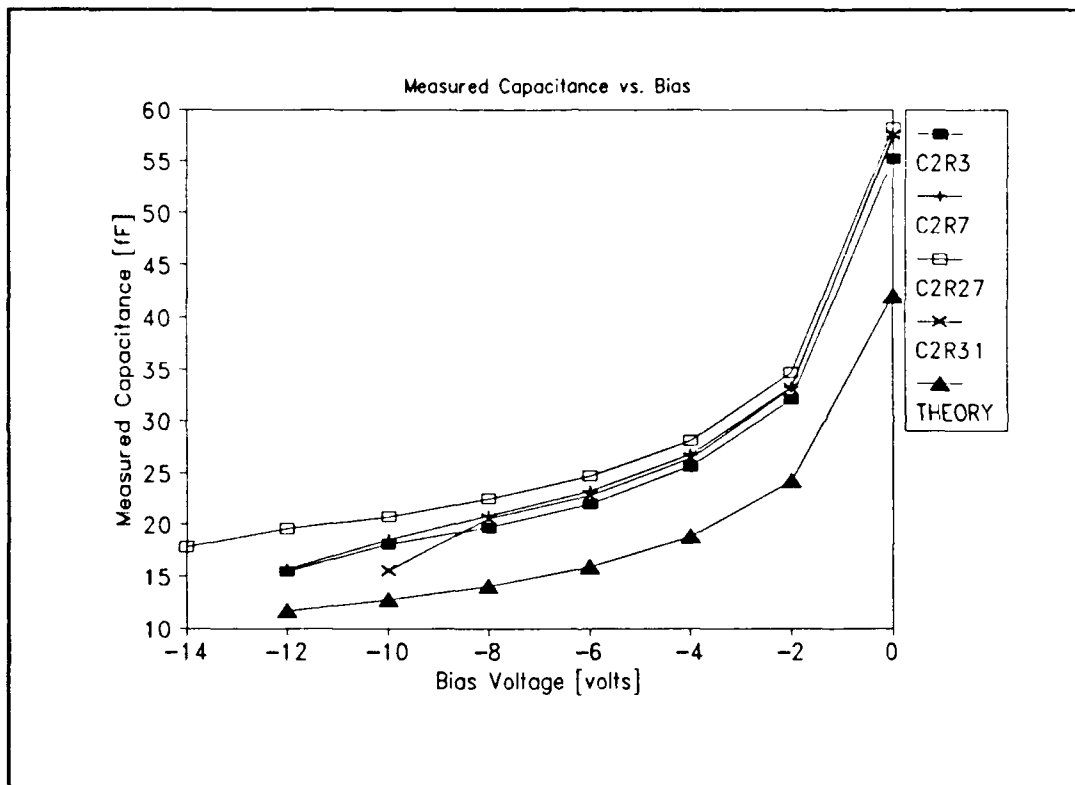


Figure 6.21 Capacitance versus reverse bias for 8 μm diameter CoDiodes on the 80/160 GHz doubler wafer. Theoretical values are included for comparison.

From the visual inspection and the dc measurements, only about 20 chips (10 percent) were candidates for RF testing. The two major causes of rejection are low reverse breakdown voltage and shorted anodes. Therefore it was impossible to obtain a sampling of all nine doubler versions.

6.5.3 Output Power and Efficiency versus Frequency

The output power was measured using the test setup shown in Fig.

6.22. (This is similar to the setup described in Chapter Three).

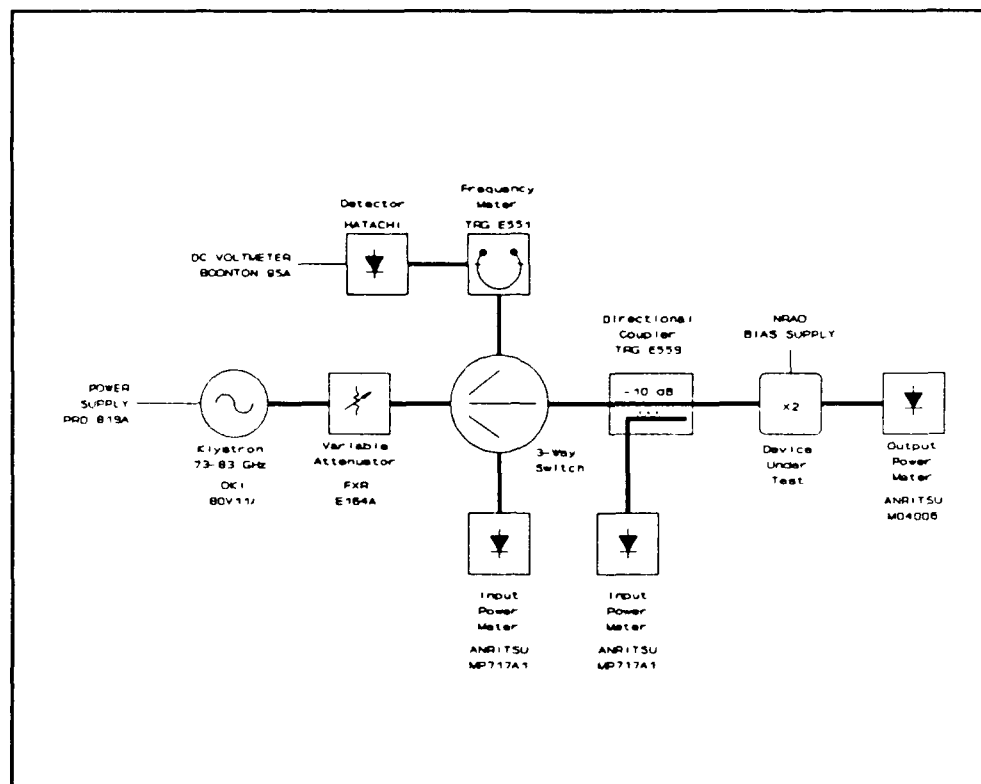


Figure 6.22 Test setup used to measure output power of the 80/160 GHz doublers.

The measured output power versus frequency for three doubler chips are shown in Fig. 6.23. The corresponding efficiencies are shown in Fig. 6.24. The input and output probe backshorts were adjusted at each frequency to yield maximum output power. Because of the many problems encountered during chip and block assembly, many of chips were destroyed by metal liftoff, scratches, excess solder, or substrate cracking. The data are for 60 mW pump power, and at each frequency, the bias voltages were adjusted for peak output power.

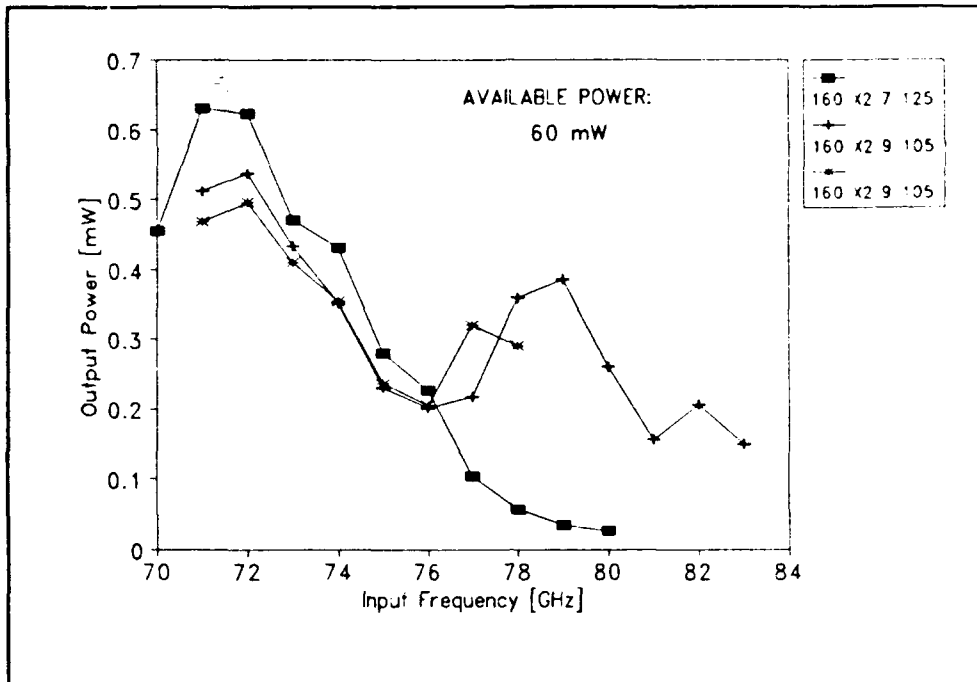


Figure 6.23 The output power versus frequency for three 80/160 GHz doubler chips. $P_{in} = 60$ mW.

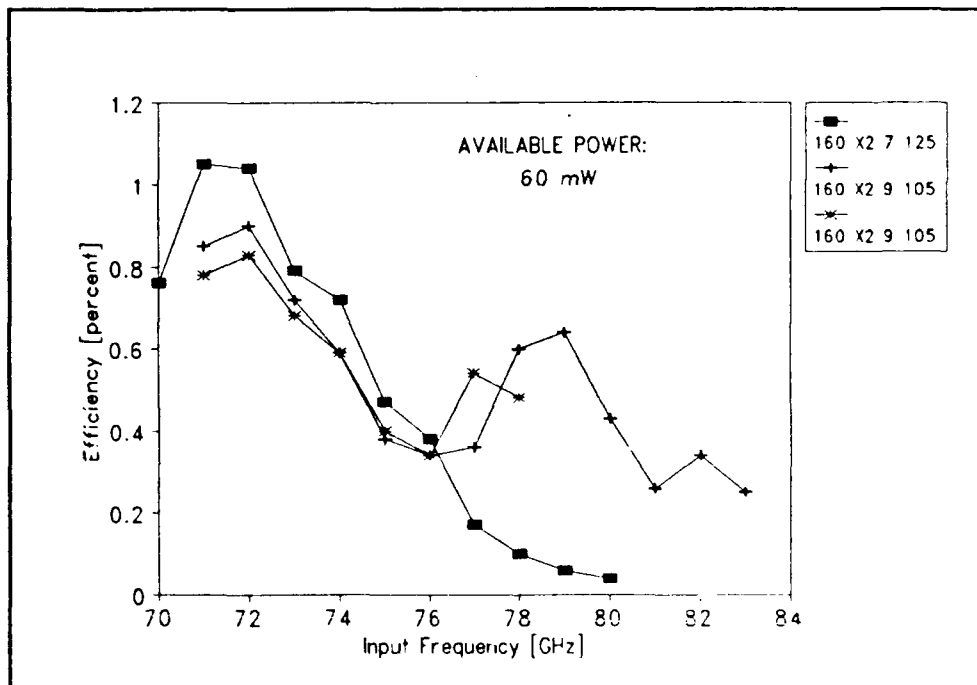


Figure 6.24 Multiplier efficiency versus frequency for three 80/160 GHz doubler chips. $P_{in} = 60$ mW.

Both bias voltages were quite similar and tended to increase with increased operating frequency from -0.6 volts at 71 GHz to -3.5 volts at 79 GHz. At the high frequency extreme, the doubler performed better with one bias very high (near -10 volts) and the other around -2.5 volts indicating improper circuit balance or improper impedance matching so that the doubler works best single-ended.

6.6 Discussion

The doubler performed best at 142 GHz with a maximum output power of 630 μ W and an efficiency of about one percent. The bias voltages at this operating point were approximately -1.0 volts. This frequency is greater than 12 percent below the design frequency. Note that a change in the anode diameter did not change the performance significantly. The very low performance is a result of improper embedding impedances at the varactors or excessive loss due to the very rough waveguide inner-surface caused by the EDM. The performance was further reduced by the poor quality of the primitive backshorts. These backshorts were non-contacting type (see Kerr, 1988), which require accurate centering inside the waveguide, however the backshort position was adjusted by hand and held in place using primitive clamps. Because of the difficulties encountered in tuning the doubler, it was decided that small signal input and output return loss measurements would not yield consistent data and hence were not attempted.

The following improvements are suggested for further development of this doubler design:

- * As will be discussed in Chapter 8 for the 31/94 GHz tripler, a shunt capacitance of 5 to 10 fF across each varactor may be present, hence causing the low operating frequency. A new design should incorporate this capacitance.
- * Eliminate EDM of waveguide in brass where possible. EDM of aluminum machines somewhat more smoothly. A split-block design should be considered so conventional machining techniques could be used.
- * Provide an air bridge across the main CPW near the input probe to improve symmetrical excitation of the CPW.
- * Use a slotline-to-finline-to-rectangular waveguide transition to improve output bandwidth and eliminate the balun (if a stand-alone doubler is required).

CHAPTER SEVEN

The 80/240 GHz Frequency Tripler

7.1 Introduction

A monolithic 80/240 GHz frequency tripler was designed, fabricated, and evaluated. The circuit, fabricated on a semi-insulating GaAs substrate, contains not only the balanced Schottky-varactors and a very compact idler circuit, but also the necessary embedding circuitry for coupling the input and output signals to rectangular waveguide. Fabrication was done at Martin Marietta Laboratories. Details of the design and evaluation of the frequency tripler are presented in this chapter.

7.2 Varactor Performance Study

The closed-form nonlinear analysis of Section 2.4 was applied to determine the multiplier performance as a function of the varactor design parameters. Hence, the application of eqns. (2-41) through (2-55) requires the following varactor parameters: 1) an abrupt-junction profile, 2) breakdown voltage, 3) built-in potential, 4) zero-biased capacitance, and 5) series resistance. With knowledge of the above parameters and with the maximum symmetrical pumping criterion, the analysis to predict the varactor efficiency, port impedances, and power levels for a specific frequency multiplier (multiplication factor and operating frequency) can be completed. These varactor parameters are directly related to the varactor fabrication variables.

There are two principal varactor fabrication variables that govern

multiplier performance: active layer impurity concentration, and the anode diameter. It is these two variables coupled with the avalanche breakdown / punchthrough criterion, and skin effect arguments applied to the buffer layer, that will establish all other fabrication variables. Therefore, it is important to carefully examine the multiplier performance as a function of these variables.

The varactor performance study examines the 80/240 GHz tripler performance (for maximum varactor efficiency at each point) of a single varactor having anode diameters ranging from 6 to 12 microns and active layer impurity concentrations ranging from 10^{16} to 10^{17} cm^{-3} . The results are presented in Table 7.1 and also in graphical form. The output power (Fig. 7.1), the varactor efficiency (Fig. 7.2), the input resistance (Fig. 7.3), and the output resistance (Fig. 7.4) are presented for the given range of anode diameters and active layer impurity concentrations.

TABLE 7.1 80/240 GHz Varactor Tripler Study (single varactor)											
$N_d \cdot 10^{16}$ [cm^{-3}]	d_a [μm]	L_e [μm]	V_{br} [v]	C_{jo} [fF]	C_{avg} [fF]	R_s [Ω]	R_{in} [Ω]	R_{out} [Ω]	P_{abs} [mW]	P_{out} [mW]	Var. Eff. [%]
1.0	6	3.0	64	8.6	1.9	88.9	301.3	167.0	95	23.5	24.5
	8			15.3	3.4	50.0	170.6	99.0	171	41.1	23.9
	10			23.9	5.4	32.0	106.4	46.5	274	61.4	22.4
	12			34.5	7.7	22.0	76.2	43.6	396	89.2	22.5
2.5	6	1.4	33	13.6	4.1	18.5	131.4	68.0	44	20.3	46.1
	8			24.2	7.3	10.4	72.9	35.7	81	34.9	43.2
	10			37.8	11.5	8.7	47.4	24.3	130	51.8	39.8
	12			54.5	16.5	6.6	34.1	20.9	193	69.7	36.2
5.0	6	0.8	20	19.2	7.2	7.9	70.6	33.0	29	16.2	56.5
	8			34.3	12.9	5.3	40.4	19.5	53	26.8	50.3
	10			53.5	20.1	4.1	26.3	13.2	88	38.4	43.4
	12			77.1	28.9	3.5	17.9	8.0	138	49.3	35.7
7.5	6	0.7	15	23.6	10.0	5.1	51.3	24.6	23	13.6	58.6
	8			42.0	17.8	3.7	28.0	12.4	44	22.0	49.7
	10			65.6	27.9	3.1	18.5	5	75	30.4	40.3
	12			94.4	40.1	2.8	12.9	5.5	120	37.2	30.9
10.0	6	0.5	13	27.3	12.5	4.0	41.6	20.5	21	12.3	58.4
	8			48.5	22.2	3.1	23.1	11.1	41	19.5	47.7
	10			75.7	34.7	2.7	14.3	5.6	71	25.6	35.9
	12			109.0	50.0	2.5	10.2	3.4	116	29.1	25.2

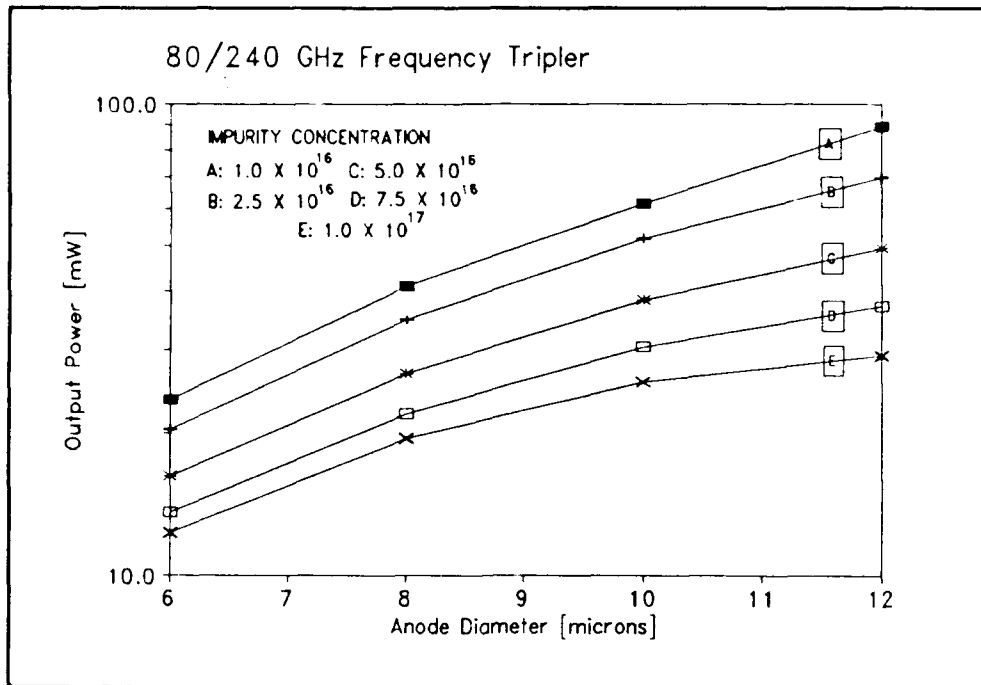


Figure 7.1 Calculated output power as a function of anode diameter. Parameter: active layer impurity concentration.

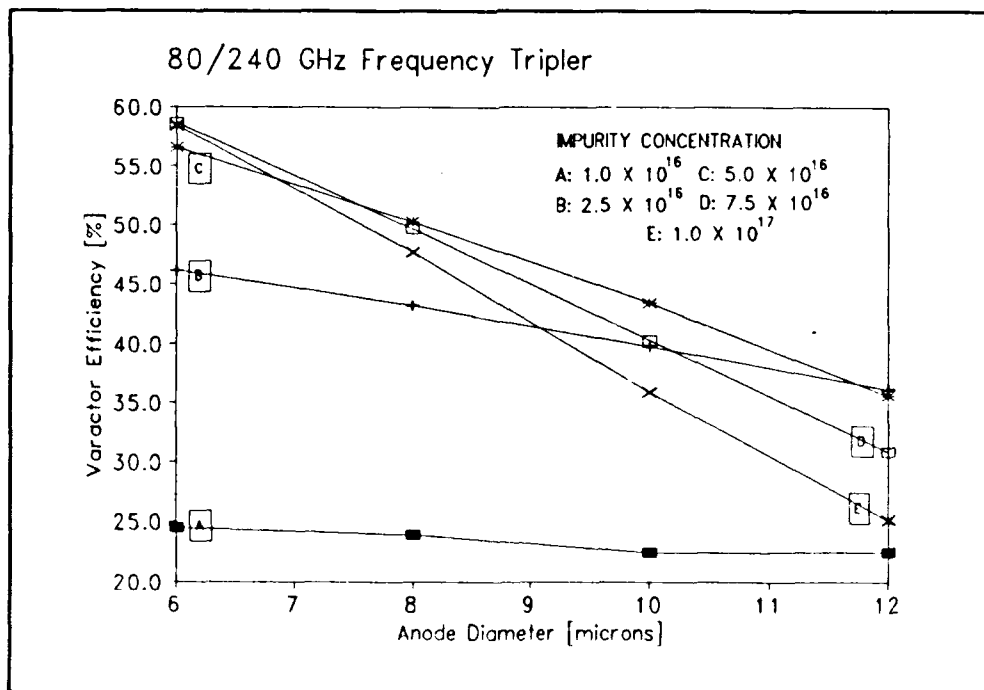


Figure 7.2 Calculated varactor efficiency as a function of anode diameter. Parameter: active layer impurity concentration.

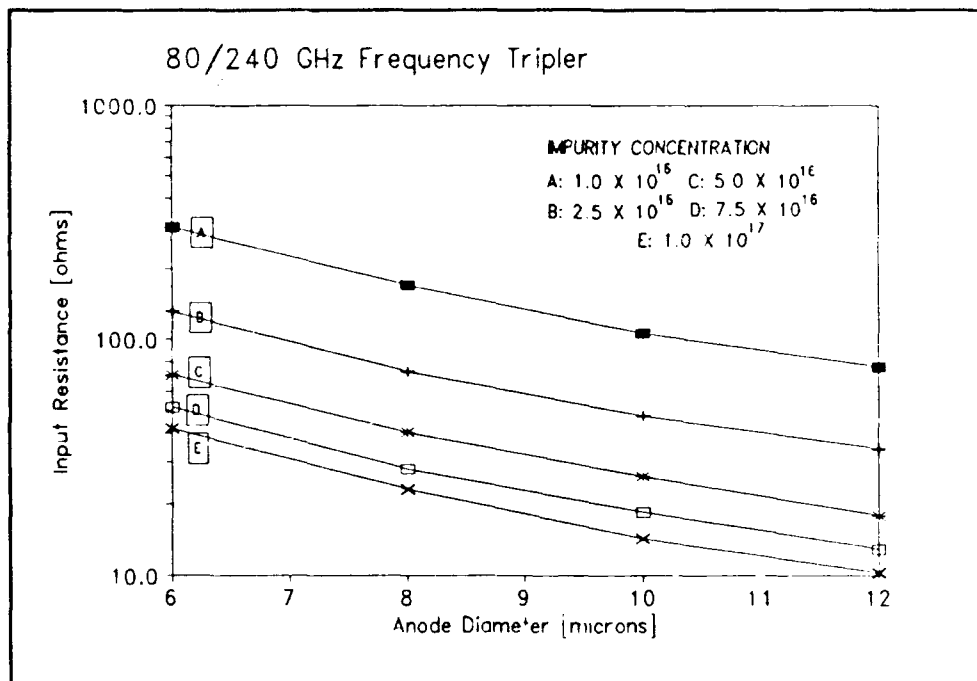


Figure 7.3 Calculated input resistance as a function of anode diameter. Parameter: active layer impurity concentration.

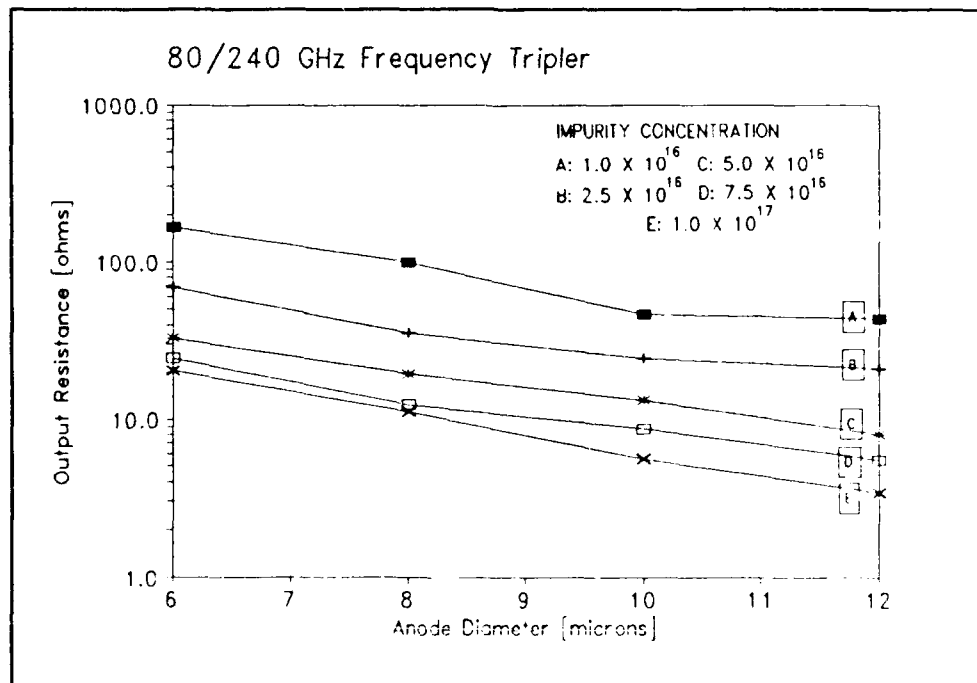


Figure 7.4 Calculated output resistance as a function of anode diameter. Parameter: active layer impurity concentration.

Fig. 7.5 shows the average junction capacitance (under the maximum symmetrical voltage swing) as calculated from eqn. (2-44).

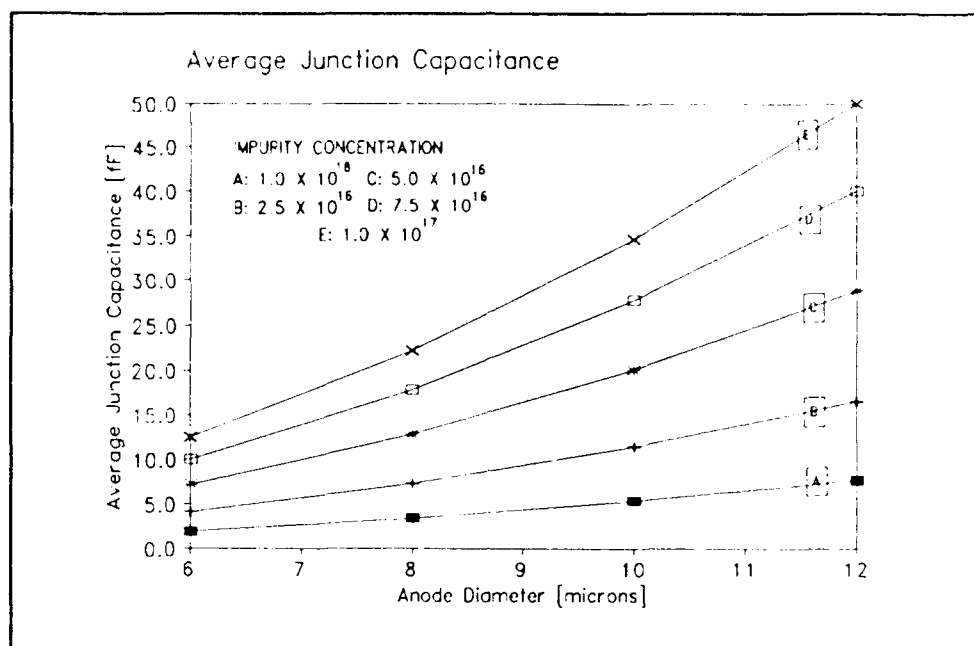


Figure 7.5 Average junction capacitance as a function of anode diameter. Parameter: active layer impurity concentration.

The above survey is for a single varactor, however since a balanced varactor arrangement (see Chapter Four) was used in this tripler design, all power levels will be twice those shown in the figures.

The tripler was designed for $P_{out} = 30$ mW per varactor. Examination of Fig. 7.1 indicates that a P_{out} of 30 mW is possible for many combinations of impurity concentration and anode diameter. However, since the goal was to provide high varactor efficiency with reasonable embedding impedances, curve C in Fig. 7.2, $n_d = 5.0 \times 10^{16} \text{ cm}^{-3}$, was therefore chosen. Correspondingly, curve C in Fig. 7.1 indicates that a P_{out} of 30 mW is possible with an anode diameter of approximately 9 microns. Figs. 7.3 and 7.4 indicate that the input and output impedances can be easily matched to 50Ω by relatively simple embedding circuitry. As a result of

this survey, the following varactor was chosen for the 80/240 GHz tripler:

FABRICATION VARIABLES:

Anode Diameter: 9 μm
Junction Profile: ABRUPT
Act. imp. level: $5.0 \times 10^{16} \text{ cm}^{-3}$
Active thickness: 0.8 μm
Buffer thickness: 2.0 μm
Buffer imp. lev.: $> 4 \times 10^{18} \text{ cm}^{-3}$

VARACTOR PARAMETERS:

$C_{j0} = 40 \text{ fF}$
 $C_{avg} = 16.5 \text{ fF}$
 $V_{bi} = 1.0 \text{ volts}$
 $V_b = -20 \text{ volts}$
 $R_s = 3.1 \text{ ohms}$

The operating point for best 80/240 GHz tripler performance using this SINGLE varactor is as follows:

Bias voltage:	-10.0 volts	
Output power at 94 GHz:	30 mW	
Absorbed power at 31 GHz:	64 mW	
Power dissipation:	34 mW	
Varactor efficiency:	47 %	
Input impedance:	34 -j 133 ohms	$Q_{input} = 3.9$
Idler impedance:	0 -j 66 ohms	
Output impedance:	18 -j 44 ohms	$Q_{output} = 2.4$

The Siegel-Kerr program (see Section 2.5) was used to verify the above performance calculations and to gain additional information about the behavior of the tripler as a function of available input power and bias voltage. The results, presented in Table 7.2, show that both calculations are in close agreement at the maximum efficiency point where the bias is -7.5 volts and the input absorbed power is 64 mW. The output power versus reverse bias is also shown in Fig. 7.6 and the varactor efficiency versus reverse bias is also shown in Fig. 7.7.

The single device equivalent circuit approach allowed the above results to be applied directly to the balanced configuration, noting that independent biasing of the two Schottky varactors was necessary. The embedding circuitry was then designed around two such varactors assuming that the parasitic shunt capacitance across the varactors was very small in comparison to the average junction capacitance.

TABLE 7.2 Large-signal Nonlinear analysis of 80/240 GHz Tripler Using Siegel-Kerr Program					
FIXED EMBEDDING IMPEDANCES: (single varactor)					
INPUT: 34 +j133		IDLER: 0 -j66		OUTPUT: 18 +j44	
BIAS VOLTAGE [V]	AVAILABLE POWER [mW]	ABSORBED POWER [mW]	OUTPUT POWER [mW]	INPUT IMPEDANCE [OHMS]	VARACTOR EFF. [PERCENT]
-6	20	19.4	6.9	23.5 -j132	35.6
	40	39.8	16.2	28.8 -j131	40.8
	60	59.3	24.2	31.6 -j130	40.8
	80	79.5	31.0	33.6 -j128	39.0
-8	20	19.2	7.5	22.3 -j137	38.9
	40	39.7	17.9	30.0 -j135	45.1
	60	59.8	28.0	34.6 -j134	46.7
	80	79.6	36.9	38.2 -j133	46.3
-10	20	15.3	5.4	15.2 -j150	35.0
	40	37.2	16.8	24.3 -j145	45.1
	60	58.0	28.0	29.8 -j143	48.3
	80	78.9	38.9	33.7 -j141	49.3
-12	20	7.6	1.6	8.6 -j169	21.4
	40	29.5	12.2	18.2 -j158	41.4
	60	51.8	24.3	25.1 -j155	46.8
	80	72.7	35.6	29.6 -j152	48.9

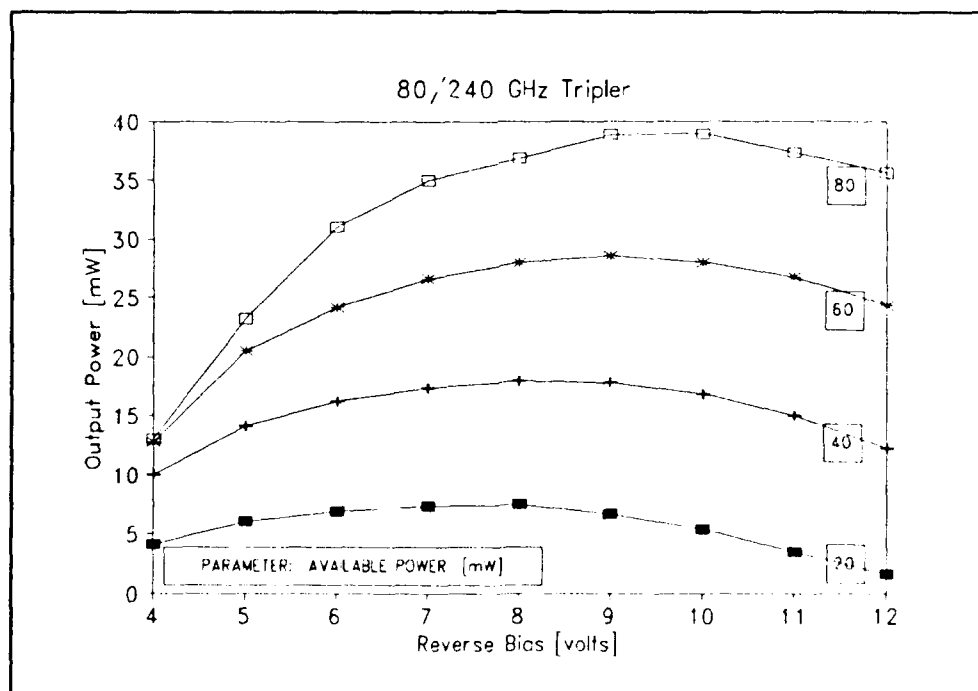


Figure 7.6 Tripler output power versus reverse bias for available powers of 20, 40, 60, and 80 mW. (single varactor)

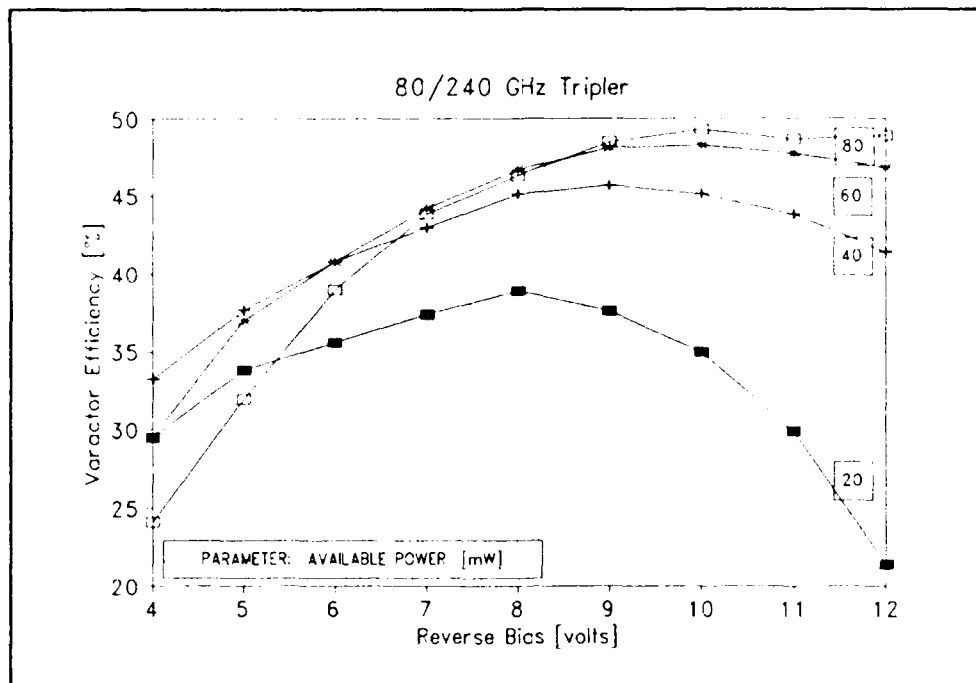


Figure 7.7 Varactor efficiency versus reverse bias for available powers of 20, 40, 60, and 80 mW. (single varactor)

7.3 Monolithic Circuit Design and Realization

Coplanar waveguide (CPW) was chosen for this monolithic tripler design. Complete details of the CPW line characteristics and discontinuities (including air bridge inductance) are presented in Chapter Five and Appendix E. The CPW transverse slab probe (see Appendix F) was used to couple the input pump signal to WR-10 rectangular waveguide. The output transition was an inverted CPW transverse cantilevered probe into WR-5 rectangular waveguide.

The input, output, and idler circuits were designed to provide conjugate-matched embedding impedances to those predicted by the analysis of Section 7.2. It is essential that circuit symmetry be preserved throughout this design to prevent unwanted propagation modes on the CPW

from being generated. Because high frequency applications of CPW and related discontinuities (tee junctions, stubs, etc.) are not well understood beyond the scaling data presented in this thesis, a "minimum circuit complexity" approach was adopted, and therefore only relatively simple, narrow bandwidth embedding circuits were considered for the initial design. However, despite the advantages of harmonic separation in balanced circuitry, the embedding circuitry is complicated by the fact that circuit elements near the varactors are within the input, idler, and output circuits simultaneously. For example, if a lumped inductance is placed near the varactor to resonate the average junction capacitance at the idler frequency, then the inductive reactance is much too large for the output circuit and too small for the input circuit. A novel solution to the problem is the "mutual tuning" approach which involves coupled inductances. The coupling is arranged such that the mutual inductance will be positive in the idler circuit and negative in the output circuit, hence resulting in simultaneous tuning. The large amount of inductive reactance needed at 31 GHz is supplied by the input network.

A scale drawing of the chip's top side lithography is shown in Fig. 7.8. Fig. 7.9 is a close-up of the region near the varactors. For the purpose of discussion, the circuit can be separated into three sections: 1) the varactors and mutually-coupled air bridges, 2) the input network including bias lines, and 3) the output network. The location where all three circuits are connected together will be referred to as the point of intersection.

Monolithic 80/240 GHz Frequency Tripler

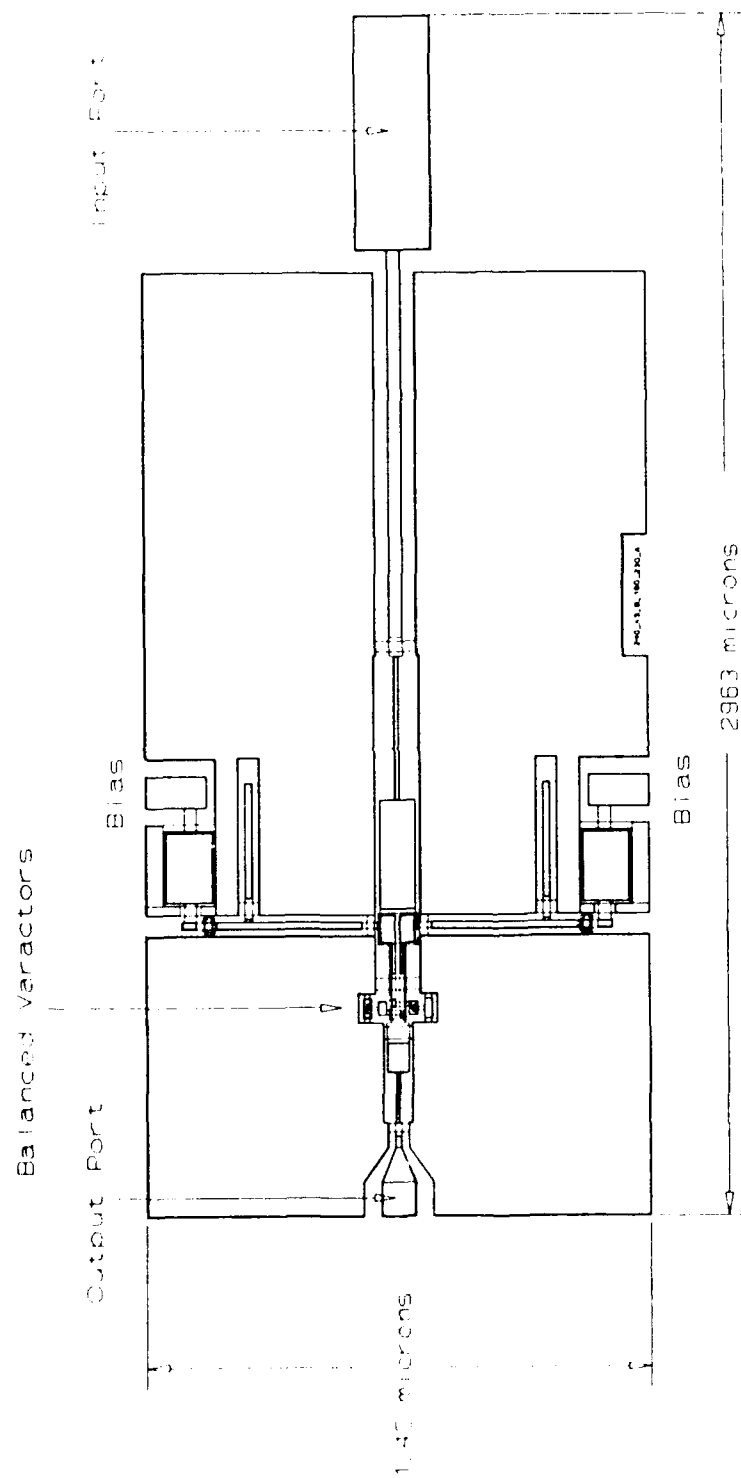


Figure 7.8 Scale drawing of the monolithic 80/240 GHz frequency tripler.

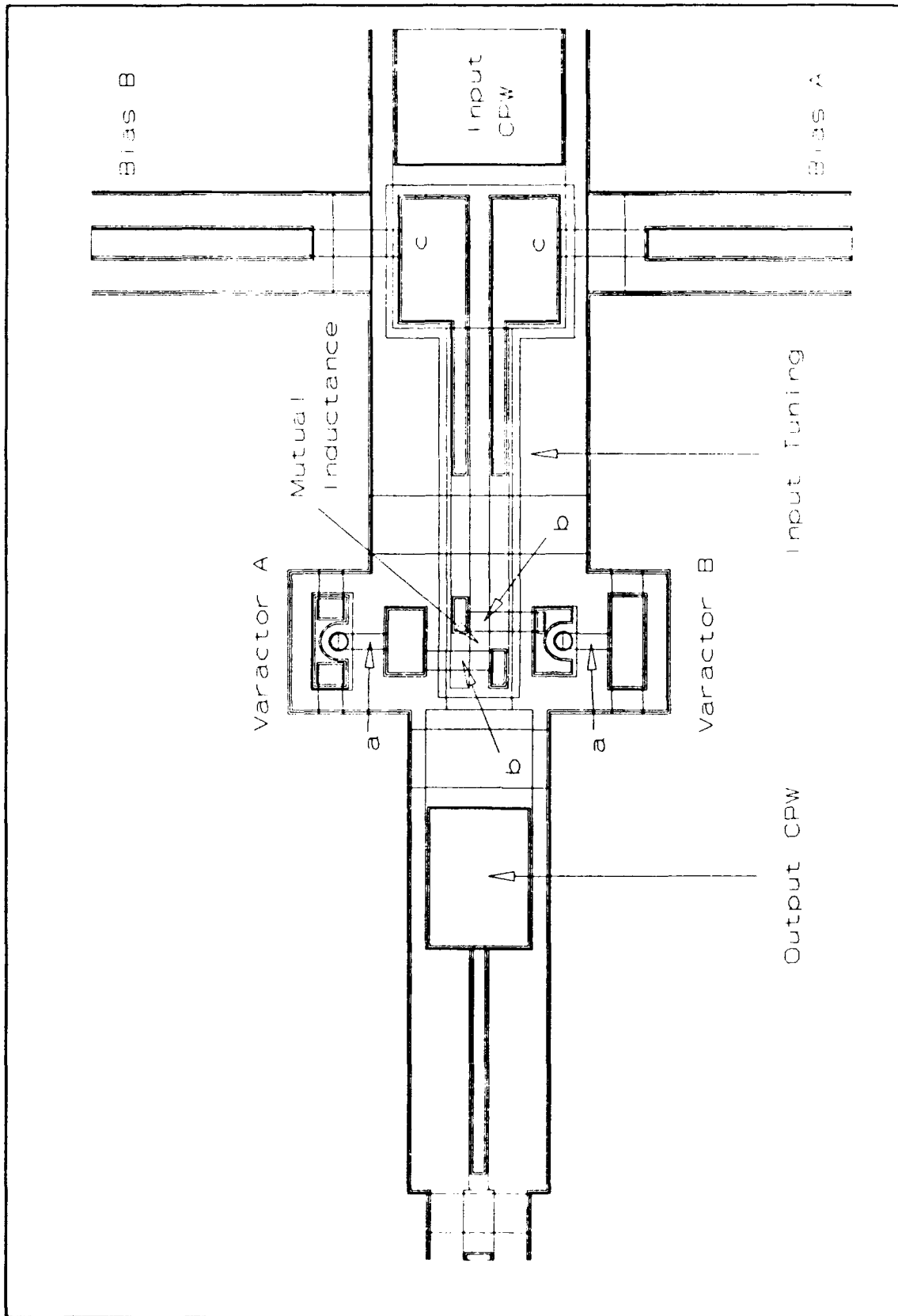


Figure 7.9 Close up of the monolithic 80/240 GHz tripler showing the varactor region.

7.3.1 Varactors and Mutually-Coupled Air Bridges

An equivalent circuit for the varactors and mutually-coupled air bridges is shown in Fig. 7.10. Each varactor anode is connected to the embedding circuitry by a short air bridge ("a" in Fig. 7.9) having about 0.014 nH inductance. The larger mutually-coupled air bridges ("b" in Fig. 7.9) attach the varactors to the main CPW.

The self-inductance of each large air bridge is about 0.027 nH as calculated by the analysis presented in Chapter Five. The mutual inductance of these air bridges, M_b , was found to be 0.011 nH by applying the formula presented in Ramo, Whinnery, and Van Duzer (Ramo, 1965) for two finite length parallel filamentary currents having a longitudinal offset (see Appendix I). As shown in Fig. 7.11, when the currents are in opposite directions, this mutual inductance is negative (case A), and when the currents are in the same direction, this mutual inductance is positive (case B).

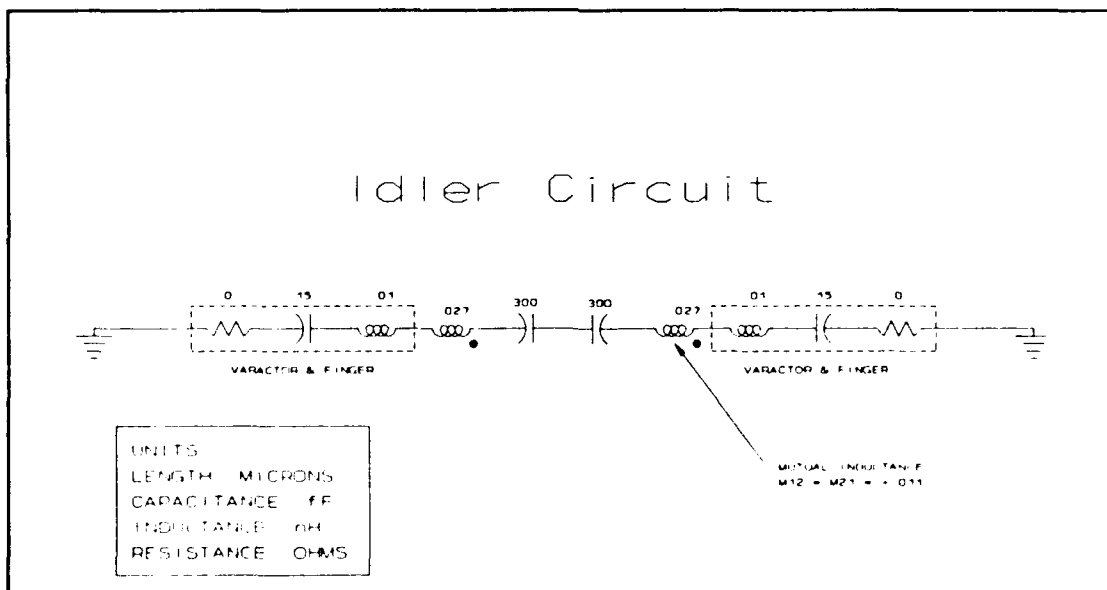


Figure 7.10 Equivalent circuit for the varactors and mutually-coupled air bridges.

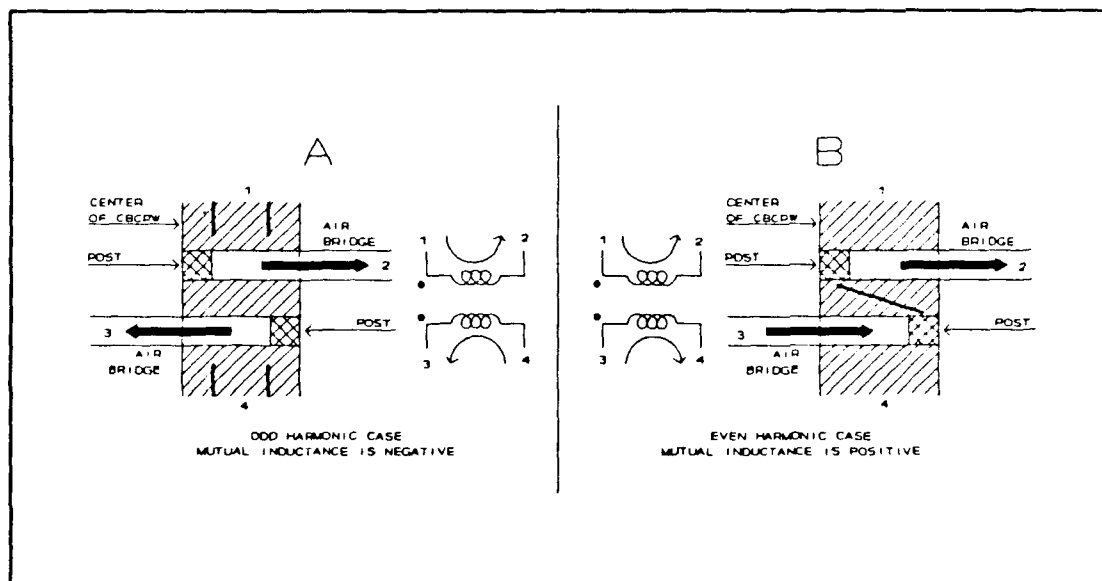


Figure 7.11 Mutual inductance (M) orientations used in the MMIC tripler design. Case A for odd harmonics (M is negative), and case B for even harmonics (M is positive). Compare with Fig. 7.9.

Table 7.3 summarizes the calculated circuit impedances at 80, 160, and 240 GHz. The total impedance as seen from the point of intersection is also given. Currents at the input and output frequencies see the two varactors in anti-parallel while the currents at the idler frequency transverse the varactor loop and see the two varactors in series. Note that in this prototype design, the parasitic shunt capacitance across the varactors was considered very small in comparison with the average junction capacitance so it was not included in the circuit model.

TABLE 7.3 Circuit impedances at the intersection point Varactors and mutually-coupled air bridges			
Component	80 GHz	160 GHz	240 GHz
Varactor:	34 -j133	0 -j66	18 -j44
Contact Finger:	+j 7	+j14	+j21
Large air bridge:	+j 14	+j27	+j42
Mutual inductance:	-j 6	+j11	-j17
Coupling capacitance:	-j 6	-j 3	-j 1
Circuit impedance at intersection:	34 -j 124	0 -j 17	18 + j 1
Diode Connection:	(parallel)	(series)	(parallel)

7.3.2 Input Network including Bias Lines

The equivalent circuit for the input network is shown in Fig. 7.12. The primary purpose of the input network is to match the impedance shown in Table 7.3 (80 GHz) to a 50 ohm source. At 80 GHz, a substantial capacitive reactance is present at the point of intersection. This reactance is resonated by a short section of 50 ohm CPW (length 160 microns) to yield an impedance of about 12 ohms real. It is at this point that the bias lines are attached to the main CPW (Fig. 7.9, point c). To match the 12 ohms real to the 50 ohms source, a two-step quarter-wave transformer (80 GHz) is used. This structure is formed using a 30 ohm (length = 354 microns) CPW followed by a 72 ohm (length = 354 microns) CPW. A 1000 micron length of 50 ohm CPW attaches the transformer to the input probe.

Each bias line consists of a quarter-wavelength (80 GHz) open stub (CPW with $Z = 45$ ohms and length = 347 microns) producing an RF short where the bias wire bonding pad is attached. A filter capacitor of about 800 fF is also attached at this point. The bias line is attached to the main CPW via an additional quarter-wavelength (80 GHz) section thus

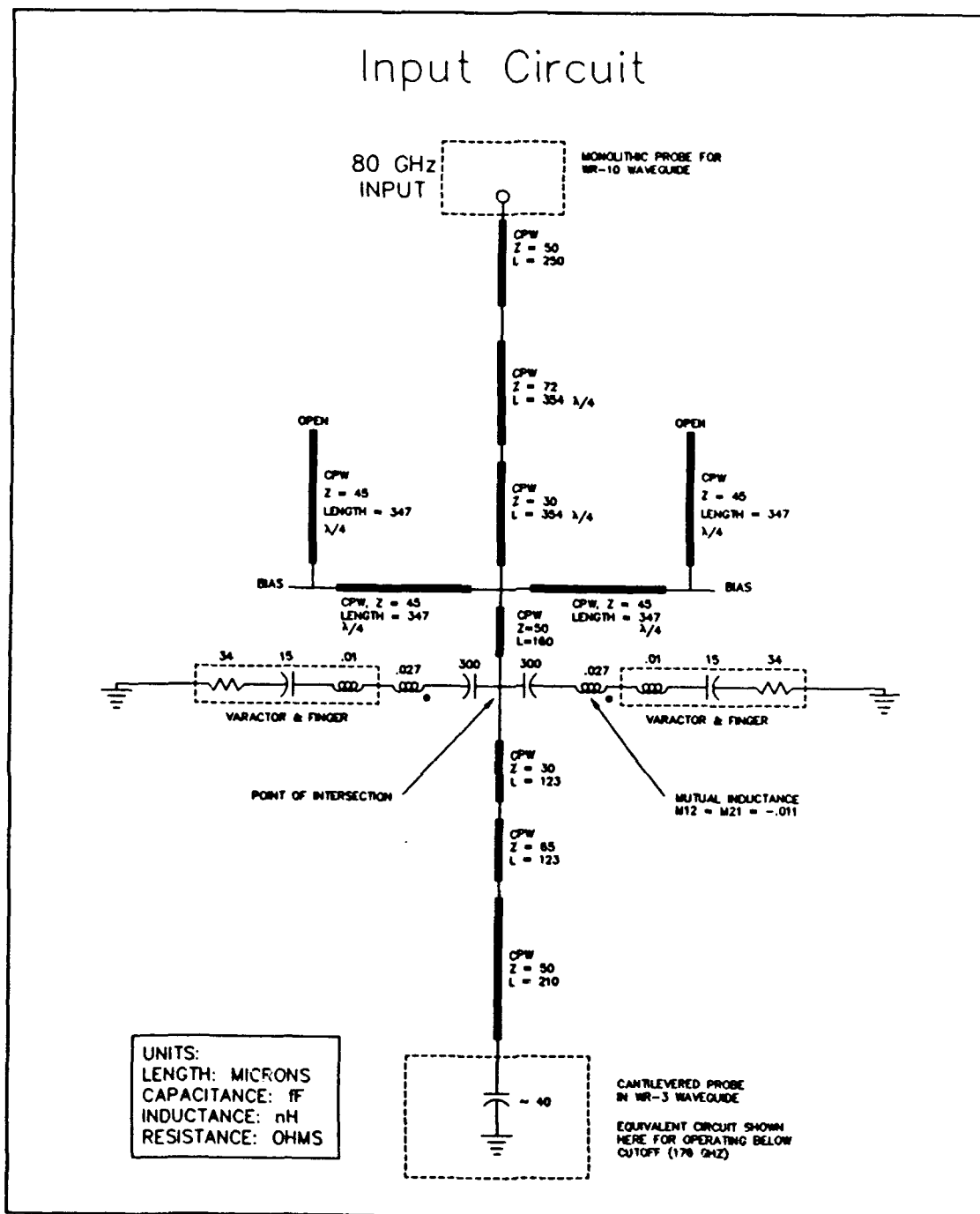


Figure 7.12 Equivalent circuit of the input network including the bias lines.

producing an RF open at the bias intersection (see Fig. 7.9, point c). Independent biasing is achieved by a stacked metal/dielectric/twin-metal strip along the main CPW as shown in Fig. 7.13. The two strips yield

independent dc paths to each varactor while the entire structure appears to RF signals as a single coplanar waveguide due to the large capacitive coupling of the strips. The electrically small geometry of the structure as compared with the operation wavelength insures that unwanted moding (excitation of the parallel-plate line formed by the stacked structure) will not occur. The parallel plate capacitance is $0.375 \text{ fF}/\mu^2$ (see section 5.5.2) with the SiN thickness of 200 angstroms.

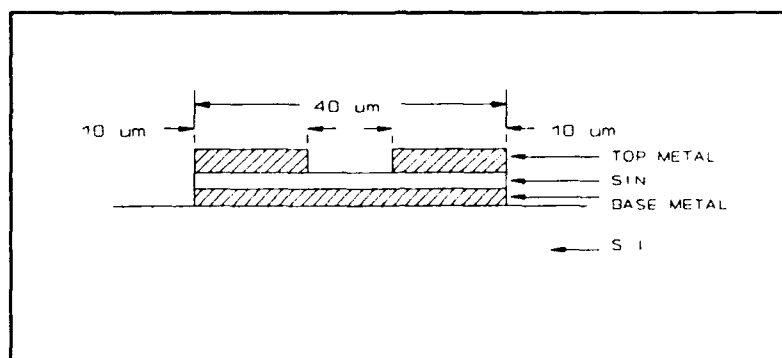


Figure 7.13 Main CPW structure for independent dc biasing of the varactors. (Not to scale).

The output circuitry was designed to appear as an open circuit at the point of intersection by considering the cutoff WR-3 waveguide as a capacitance of approximately 40 fF (a perfect open circuit was not used here due to the presence of fringing capacitance which was estimated to be about 40 fF from rough calculations based on the geometry of the structure) and adjusting the 50 ohm section of CPW in the output network to compensate. The input circuit is isolated from the idler currents because of circuit balance.

A summary of the input network's transmission line characteristics (including loss) is presented in Table 7.4. An estimate of the total circuit loss through the input network is also given (g = CPW ground plane spacing and s = CPW center conductor width).

TABLE 7.4 Summary of CPW Characteristics Input Network					
LINE	g [um]	s [um]	LENGTH [um]	LOSS/LEN. [dB/um]	LOSS [dB]
50 ohm	100	34	1000	.000314	0.3
72 ohm	110	12	354	.000504	0.2
30 ohm	110	90	354	.000374	0.1
50 ohm	110	40	160	.000284	0.1
45 ohm	50	12	4x 347	.000704	1.0
Estimated total circuit loss in the input network:					1.7 dB

7.3.3 Output Network

The equivalent circuit for the output network is shown in Fig. 7.14. Table 7.3 shows that the varactor circuit impedance at 93 GHz has a very small inductive component and hence no additional compensation is necessary. The 8 ohms real impedance is transformed to 50 ohms using a two-step quarter-wave transformer formed by a $Z = 30$ ohms, 123 microns length of CPW followed by a $Z = 65$ ohms, 123 microns length of CPW. A section of 50 ohms CPW (length = 210 microns) is used to connect the output network to the rectangular waveguide probe.

The magnitude of the input port impedance is over 10 times larger than the impedance of the output network (and varactor network) at the intersection point, hence some inherent isolation is present. A low pass filter structure was examined to improve the isolation. However, for the prototype multiplier, the filter was rejected because it was too complex for the level of understanding of high frequency CPW at the time of circuit conception. Such a filter structure (or tuning stubs) should be included in later versions of the tripler (see Chapter 8 for details of the 31/94 GHz design which incorporates tuning stubs). The output circuit

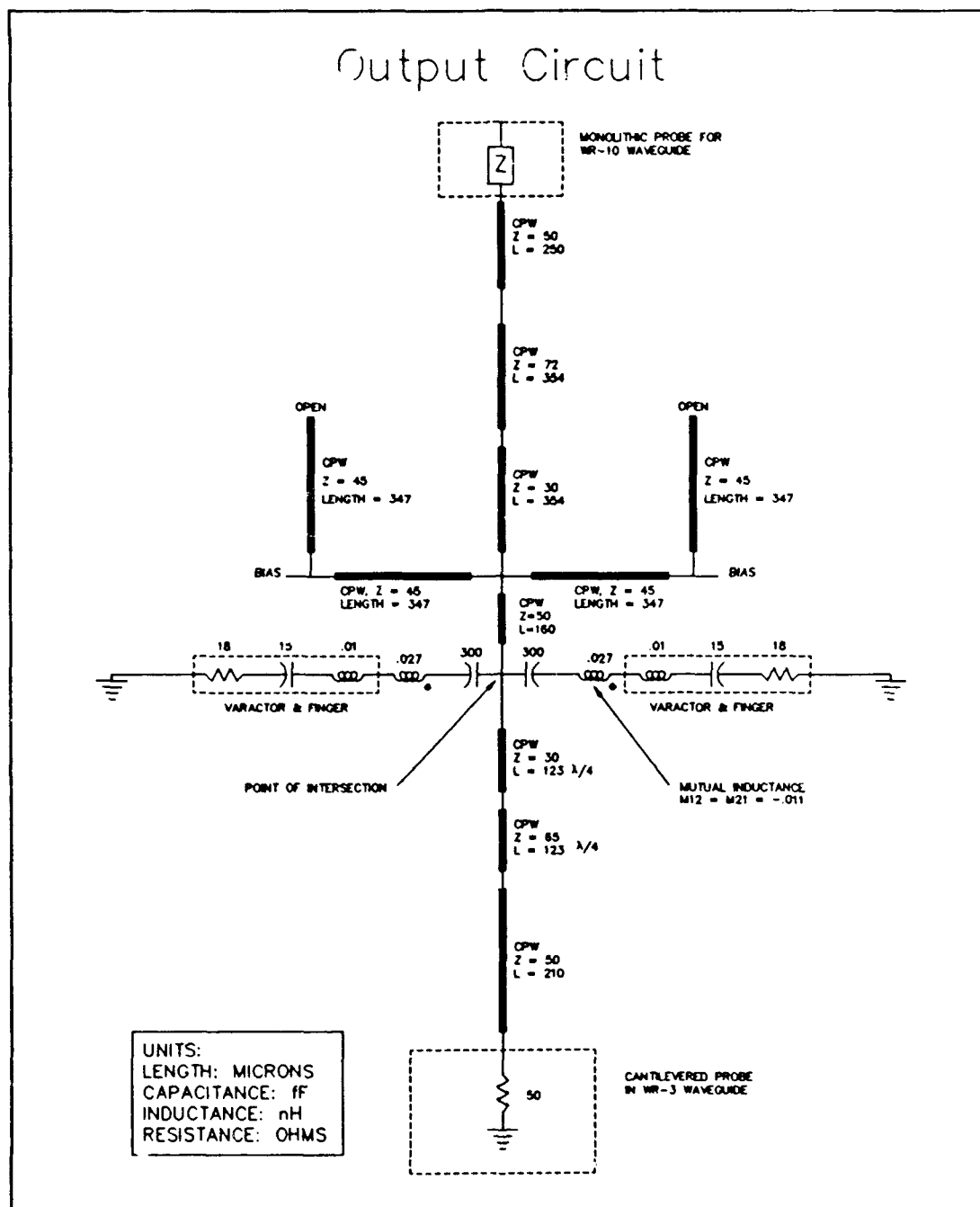


Figure 7.14 Equivalent circuit for the output network.

is isolated from the idler by circuit balance.

A summary of the transmission line characteristics (including loss) is presented in Table 7.5. Note that the input network contribution is also included. An estimate of the total circuit loss through the output

network (including an additional 0.5 dB of loss for the rectangular waveguide output probe) is also included in the total loss estimate.

TABLE 7.5 Summary of CPW Characteristics Output Network					
LINE	g [um]	s [um]	LENGTH [um]	LOSS/LEN. [dB/um]	LOSS [dB]
50 ohm	70	24	210	.000801	0.2
65 ohm	70	10	123	.001230	0.2
30 ohm	70	56	123	.001011	0.1
50 ohm	100	34	1000	.000628	0.6
72 ohm	110	12	354	.001008	0.4
30 ohm	110	90	354	.000748	0.3
50 ohm	110	40	160	.000568	0.1
45 ohm	50	12	4x 347	.001408	2.0
Estimated total circuit loss in the output network: (includes 0.5 dB for waveguide probe)					4.4 dB

7.3.4 Embedding Impedances and Overall Tripler Performance

The embedding impedances of all three networks were examined as a function of frequency. The circuit simulator TouchStone was used to calculate the impedances presented at the point of intersection by the input, idler, and output networks. Fig. 7.15 shows the REAL part and Fig. 7.16 shows the IMAGINARY part of the intersection impedance from 70 to 90 GHz. Fig 7.17 shows the REAL part and Fig. 8.18 shows the IMAGINARY part of the intersection impedance from 230 to 250 GHz.

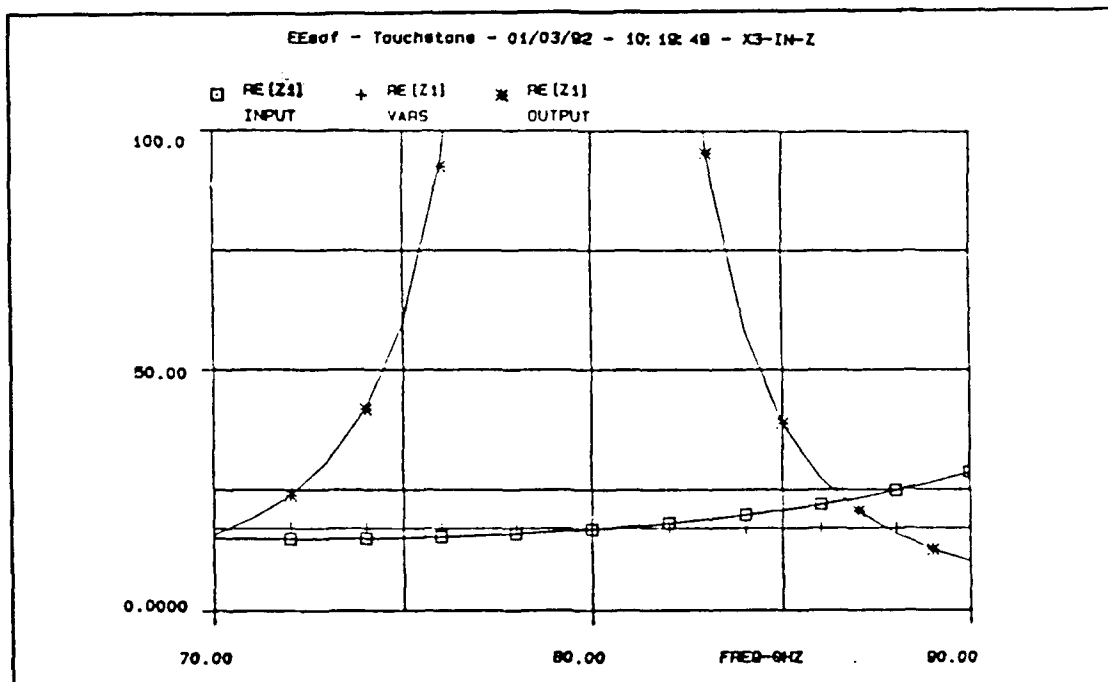


Figure 7.15 REAL part of intersection impedances for input, output, and varactor networks from 70 to 90 GHz.

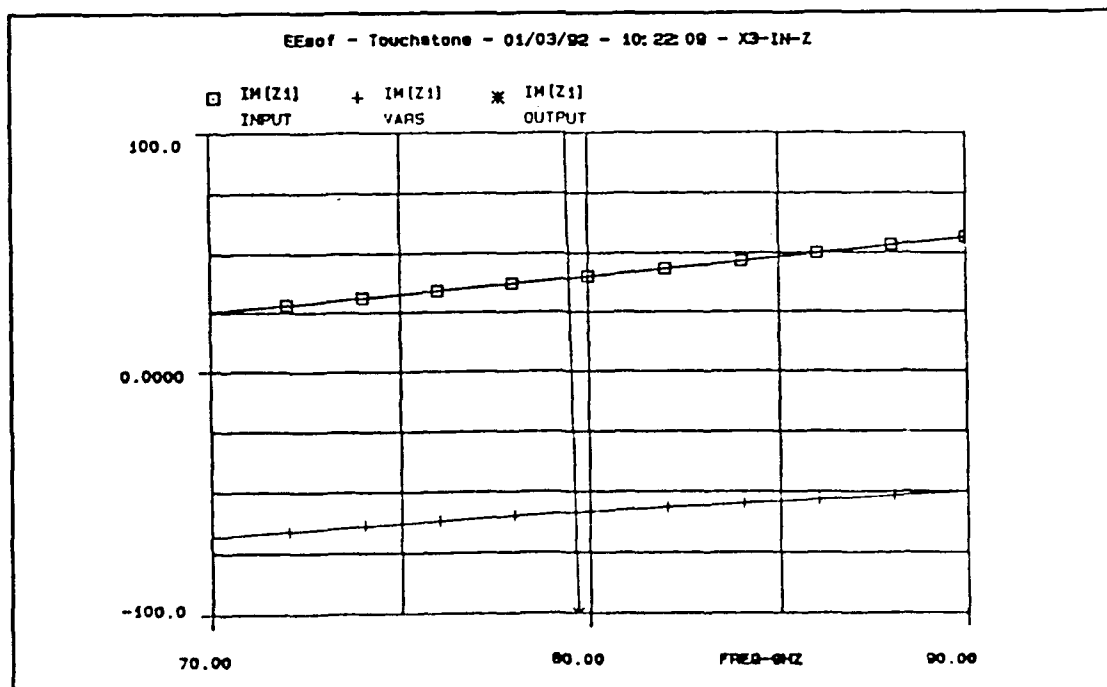


Figure 7.16 IMAGINARY part of the intersection impedances for the input, output, and varactor networks from 70 to 90 GHz.

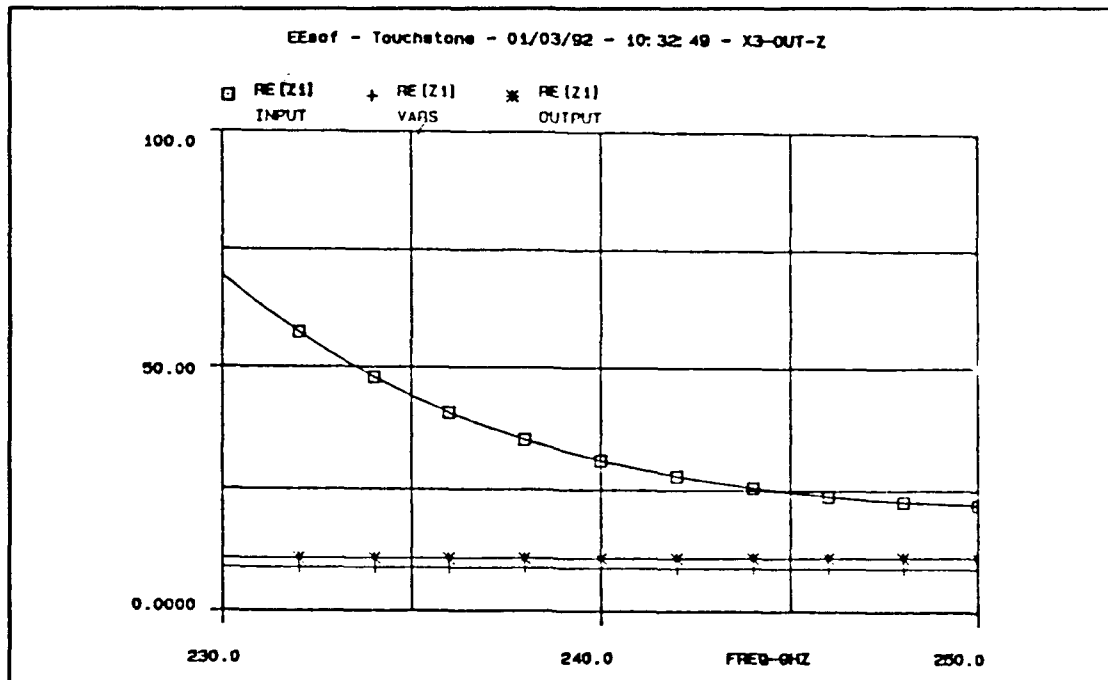


Figure 7.17 REAL part of intersection impedances for the input, output, and varactor networks from 230 to 250 GHz.

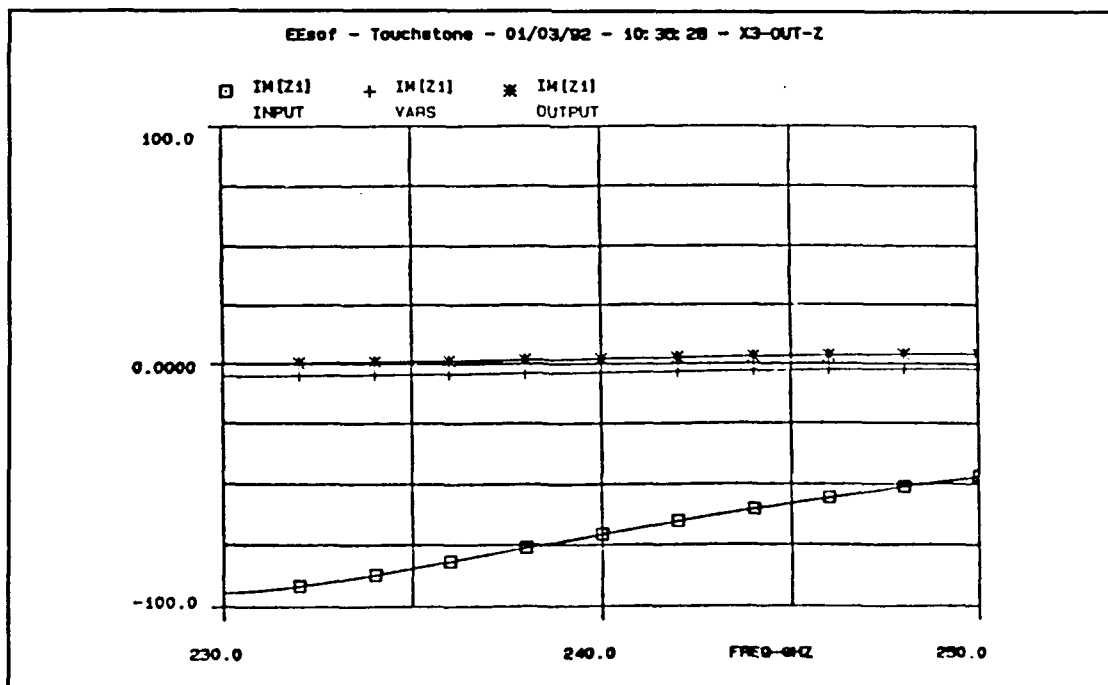


Figure 7.18 IMAGINARY part of the intersection impedances for input, output, and varactor circuits from 230 to 250 GHz.

From these data, the embedding impedances at the varactors for 75/225, 80/240, and 85/255 GHz operation were calculated and are presented in Table 7.6.

TABLE 7.6 Embedding Impedances versus Frequency 80/240 GHz Tripler			
Pump Frequency	Embedding Impedances [ohms]		
	INPUT	IDLER	OUTPUT
75 GHz	24.8 +j 65.9	0 +j 54.5	20.2 +j 38.5
80 GHz	36.8 +j 88.7	0 +j 47.7	21.4 +j 46.0
85 GHz	69.0 +j120.3	0 +j 51.1	23.2 +j 51.1

The nonlinear analysis program of Siegel and Kerr was used together with the embedding impedances presented in Table 7.6 to calculate the performance of the tripler as a function of frequency. Conductive losses in the embedding circuits are also included. The best performance at each frequency is shown in Table 7.7.

TABLE 7.7 Predicted Tripler Performance versus Frequency BALANCED VARACTOR CIRCUIT Siegel and Kerr Program					
Pump Frequency [GHz]	Bias Voltage [volts]	Available Power [mW]	Output Power [mW]	Input Impedance [ohms]	Efficiency [percent]
75	-5	100	5.6	25 -j 110	5.6
80	-6	100	7.6	25 -j 118	7.6
85	-7	100	7.2	24 -j 123	7.2

The efficiency calculations in Table 7.7 are based on the monolithic tripler output power and the available power at the tripler input port.

7.4 Design Variations

Nine versions of the 80/240 GHz monolithic frequency tripler were fabricated at Martin Marietta Laboratories as described in Section 5.7 of this thesis. The variations, which are outlined in Table 7.8, show controlled variation in the two primary circuit variables: the input tuning line length and the output 50 Ω line length.

TABLE 7.8 80/240 GHz Tripler Variations			
CHIP NUMBER	ANODE DIA.	INPUT TUNING	OUTPUT TUNING
240 X3 9 140 200 A	9	140	200
240 X3 9 140 230 A	9	140	230
240 X3 9 140 260 A	9	140	260
240 X3 9 160 200 A	9	160	200
240 X3 9 160 230 A	9	160	230
240 X3 9 160 260 A	9	160	260
240 X3 9 180 200 A	9	180	200
240 X3 9 180 230 A	9	180	230
240 X3 9 180 260 A	9	180	260

Also included on this wafer was a test structure used to characterize a sample varactor. The structure consists of a 8 micron diameter varactor in series with a coplanar waveguide (CoDiode structure) as shown in Fig. 6.13. Calibration structures having open anodes, shorted anodes, and open fingers were also fabricated on wafer.

After the design was completed, it was deemed necessary to minimize fabrication costs by fabricating both the 80/160 GHz doubler and 80/240 GHz tripler on the same wafer having an active layer doping at $6.3 \times 10^{16} \text{ cm}^{-3}$ and active layer thickness of 0.7 μm . The effect of this change is quite minor considering that for a 9 μm anode, the average junction capacitance will only change by approximately 4 fF which is

easily masked by the approximations made during the design of the embedding circuitry. Hence, no attempt was made to rework the design. Wafer VD1-1 was completed on March 1, wafer VMD2-3 was completed on July 15, and wafer VDM2-2 was completed on August 1, 1991.

7.5 Experimental Results

The tripler was evaluated on the basis of 1) a visual inspection, 2) dc characteristics, 3) output power and efficiency versus frequency. All dc measurements were made on wafer or on an individual chip mounted on a glass microscope slide. A special mounting block was designed for the RF measurements to provide access to the input and output ports as well as for dc bias connections. A sketch of the mounting configuration is shown in Fig. 7.19. Fig. 7.20 shows a photograph of the upper and lower sections of the mount. A close-up of the chip area is shown in Fig. 7.21. Figure 7.22 shows the same region of the mount with the chip in place.

Most of the mounting block machining was done using conventional milling techniques by E. Spenceley and his group at the University of Virginia machine shop. The input and output rectangular waveguide backshorts were formed using electric-discharge machining (EDM) at the Martin Marietta machine shop. Originally only 10 to 20 mils deep, the backshorts were later milled completely through the upper section of the block so that adjustable contacting backshorts could be used. Upper and lower block dimensions and alignment was checked under a microscope prior to mount assembly.

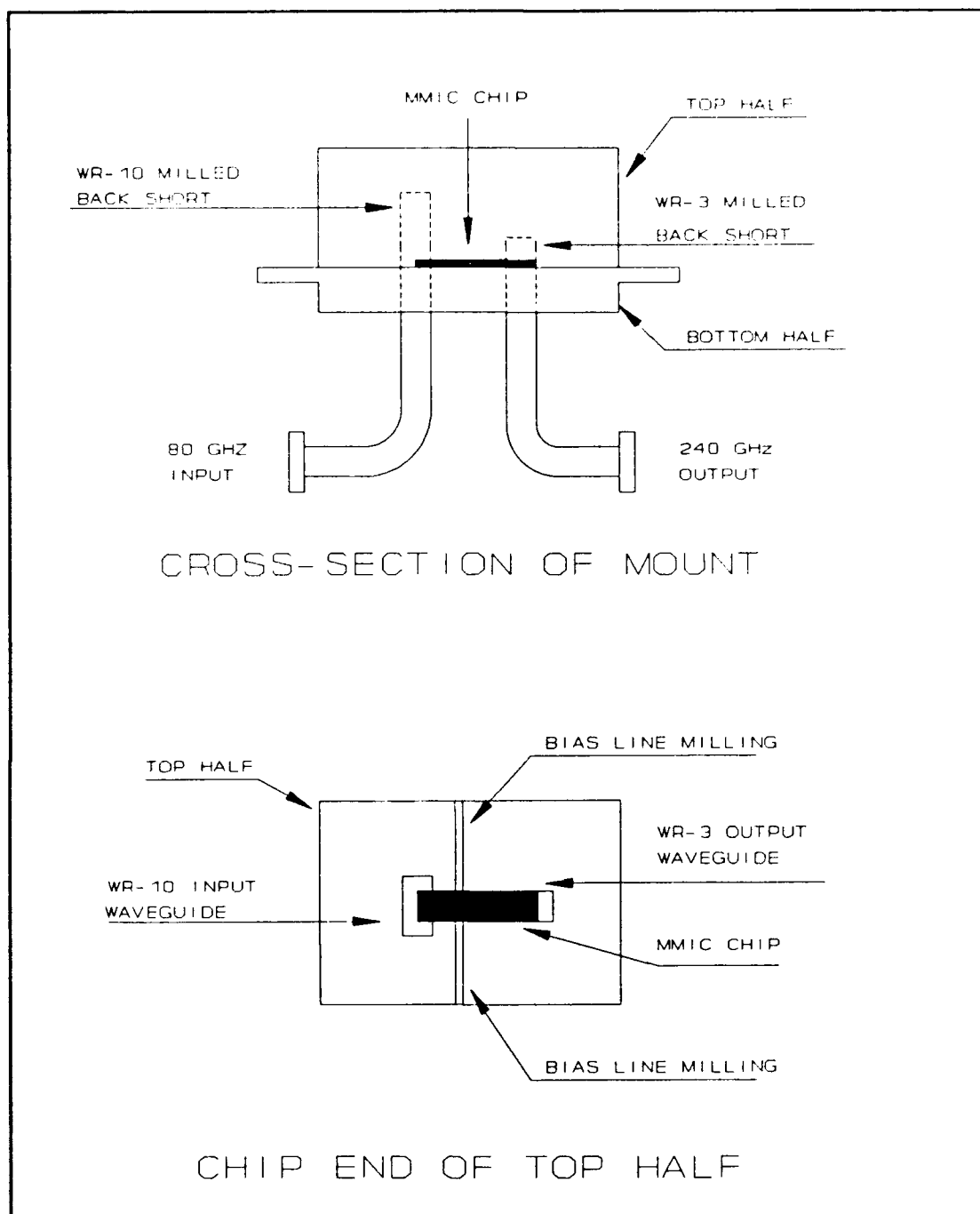


Figure 7.19 The block configuration used for RF testing the 80/240 GHz tripler (not to scale). Complete details are in Appendix H.

The lower section of the block was assembled as follows: A 90 degree E-bend was formed on a 2.5 inch section of WR-10 waveguide and a 90 E-bend was formed on a 2.5 inch section of WR-3 waveguide.

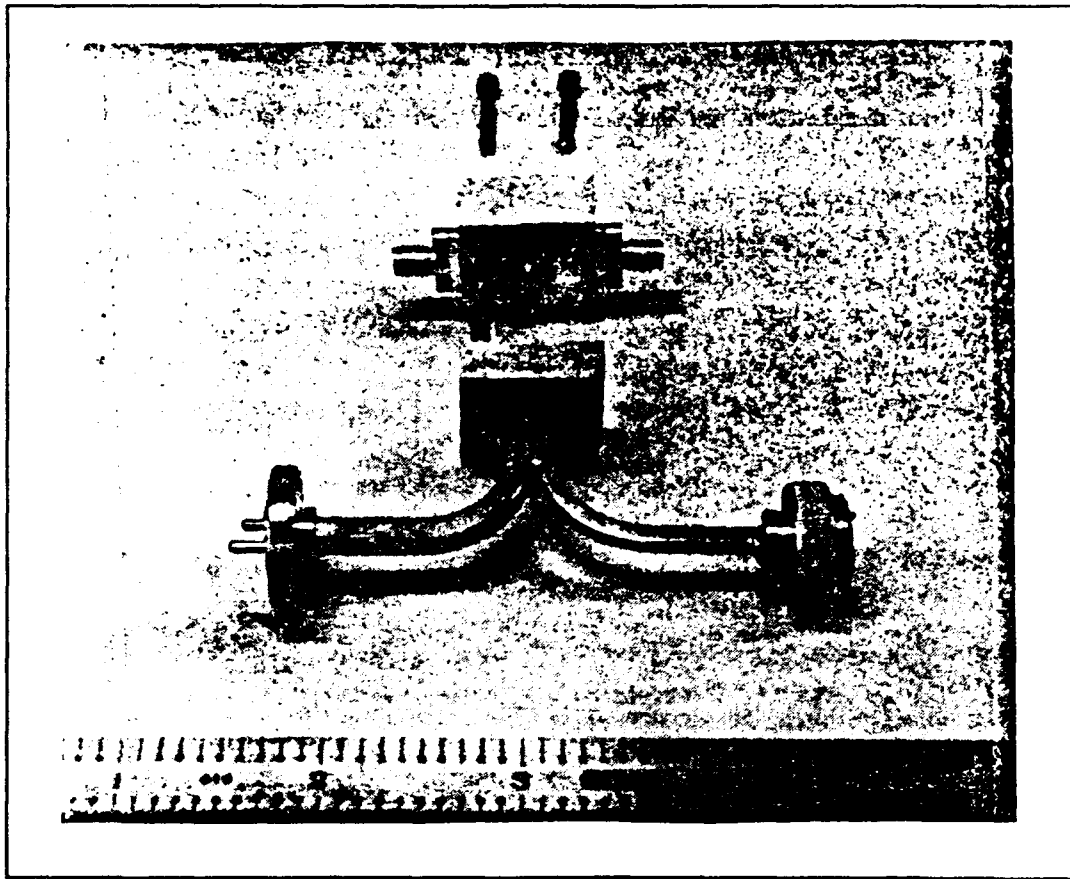


Figure 7.20 Side view of the 80/240 GHz tripler chip mounting block showing the upper and lower sections. The chip resides in the upper section (see Fig. 7.21 and 7.22).

The waveguides were soldered to the lower section of the mounting block as shown, and mating surface of the block was then machined flat. Flanges were attached to the free end of the waveguides and then the entire assembly was gold plated.

The block upper section assembly and chip mounting were performed in exactly the same manor as in the 80/160 GHz doubler mount, hence details can be found in Section 6.5. Upon assembly, the two halves were mated together, guided by two stainless-steel pins, and fastened by two 4-40 machine screws.

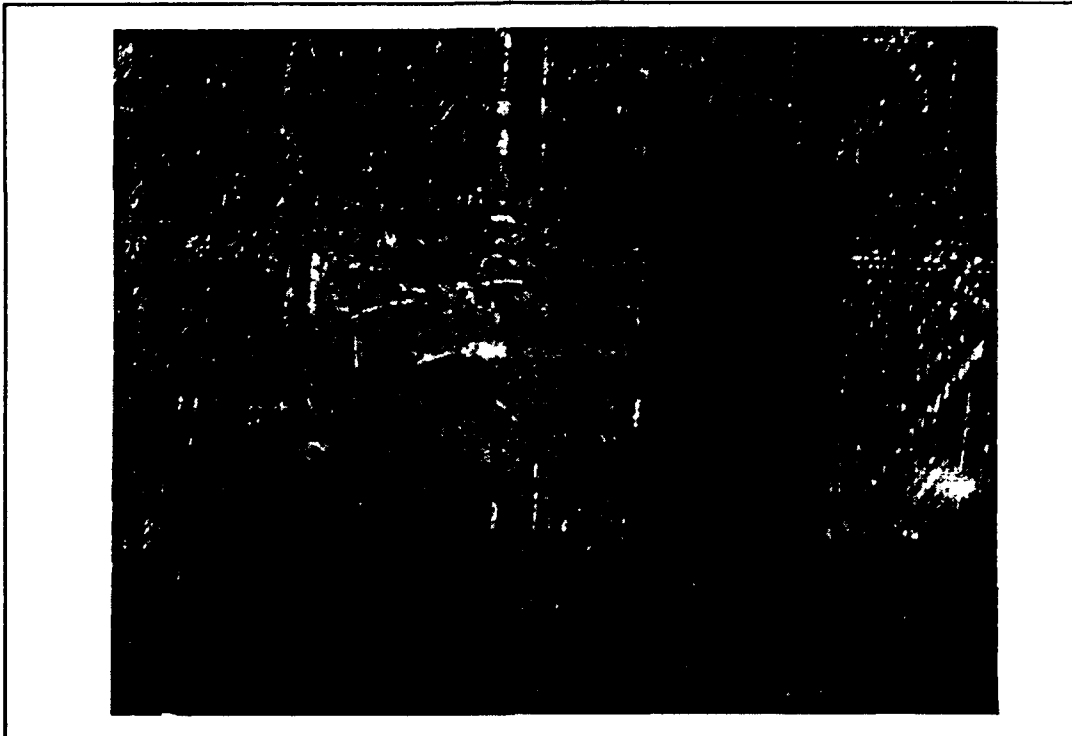


Figure 7.21 A close-up of the milled region in which the tripler chip is mounted.

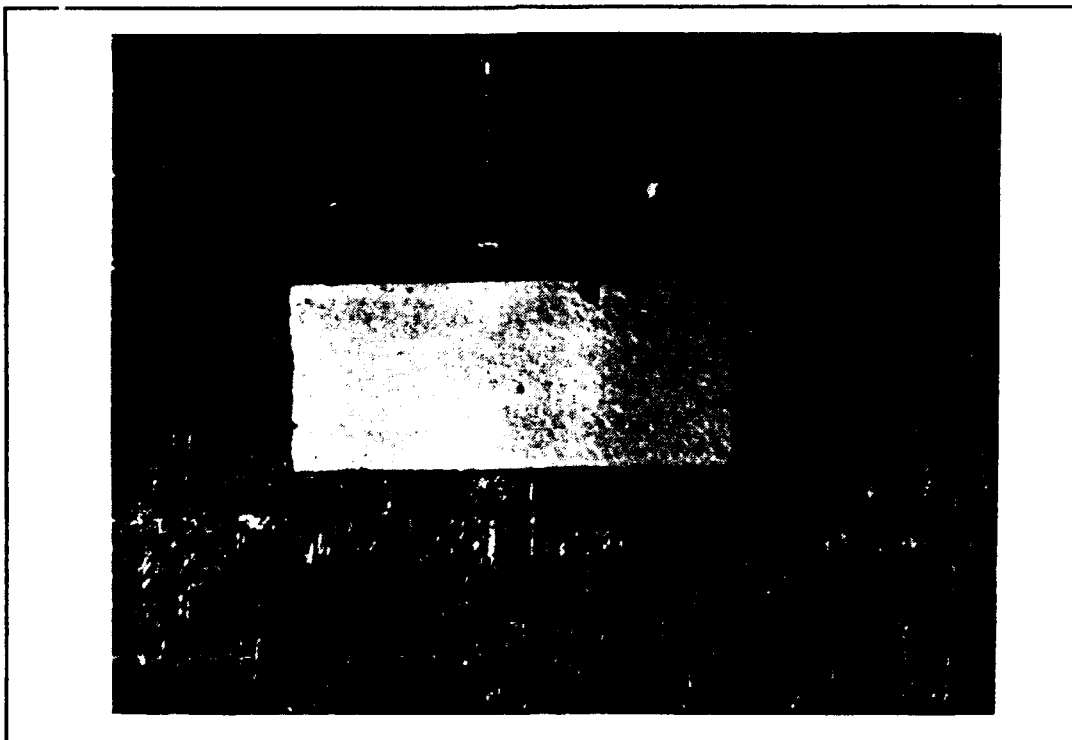


Figure 7.22 Same region of the mounting fixture as in Fig. 7.21 but with chip in place.

Although three wafers of the 80/240 GHz tripler chips were fabricated, only the triplers of batch VMD2-3 were acceptable for RF measurements. The triplers of VD1-1 had a very thin base metallization that caused very large resistances under the air bridges. The VMD2-2 was slightly over-plated which resulted in shorted anodes. Hence, all experimental results given in this section are for wafer VMD2-3 (although this wafer was slightly under-plated resulting in a low chip yield).

7.5.1 Visual Inspection

Fig. 7.23 is a photograph of the 80/240 GHz monolithic frequency tripler top side processing as it appears prior to chip dicing (note that the 80/160 GHz doubler is also visible in the photograph).

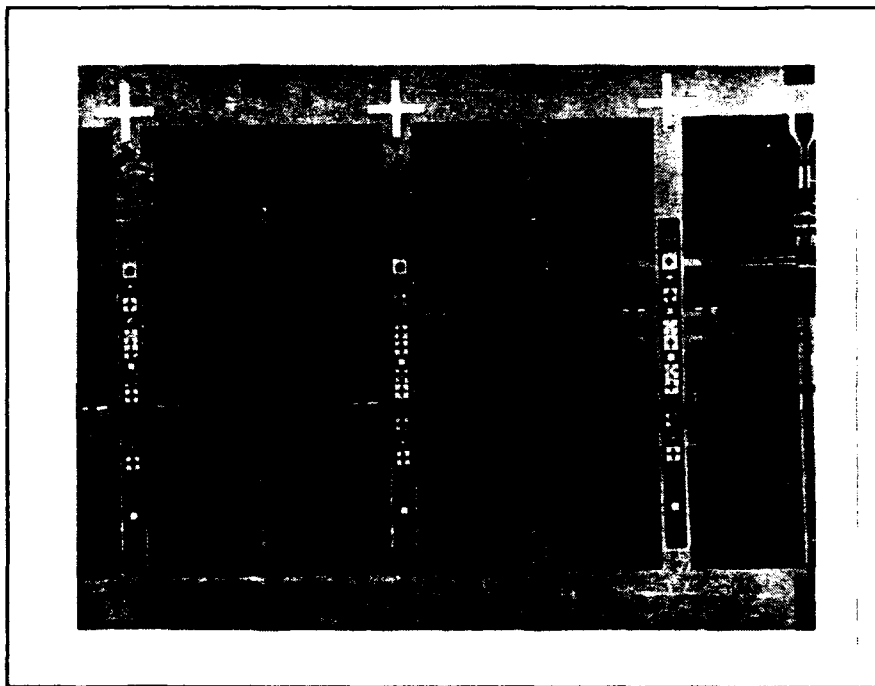


Figure 7.23 80/240 GHz tripler as it appears prior to dicing. The 80/160 GHz doubler is also visible.

Fig 7.24 is a closeup view showing the input lines, bias lines, and varactor region. Fig. 7.25 is a closeup of the mutually-coupled air bridges and varactors. The lithography appears to be very well defined and no residuals of the fabrication process were evident. However, due to fabrication problems, only about 60 percent of the wafer was processed through to completion. Many of the chips near the edges of the wafer were lost. Visual inspection showed less than 20 percent yield.

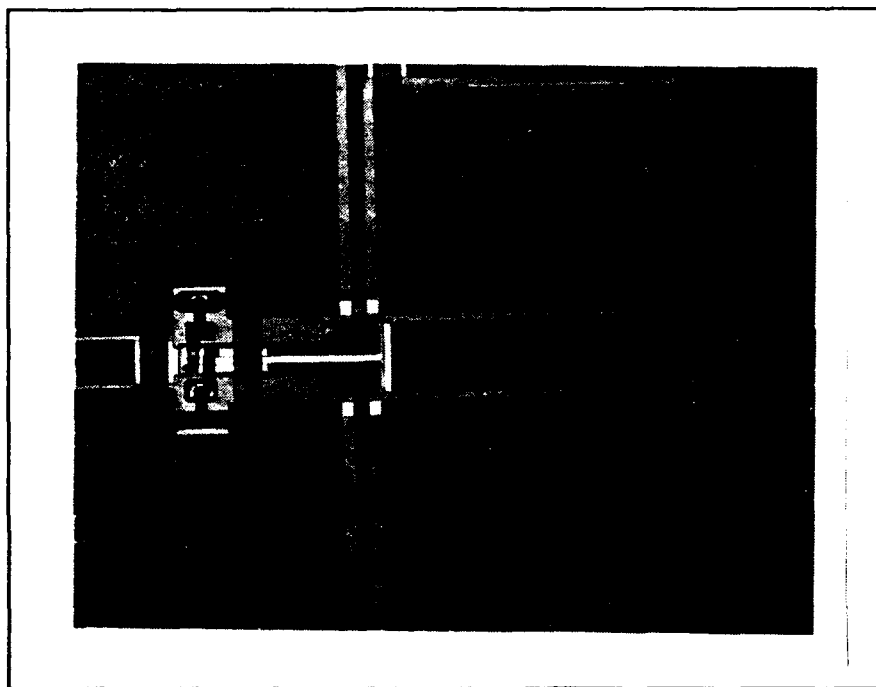


Figure 7.24 Close up of the input CPW, bias lines, and varactor region.

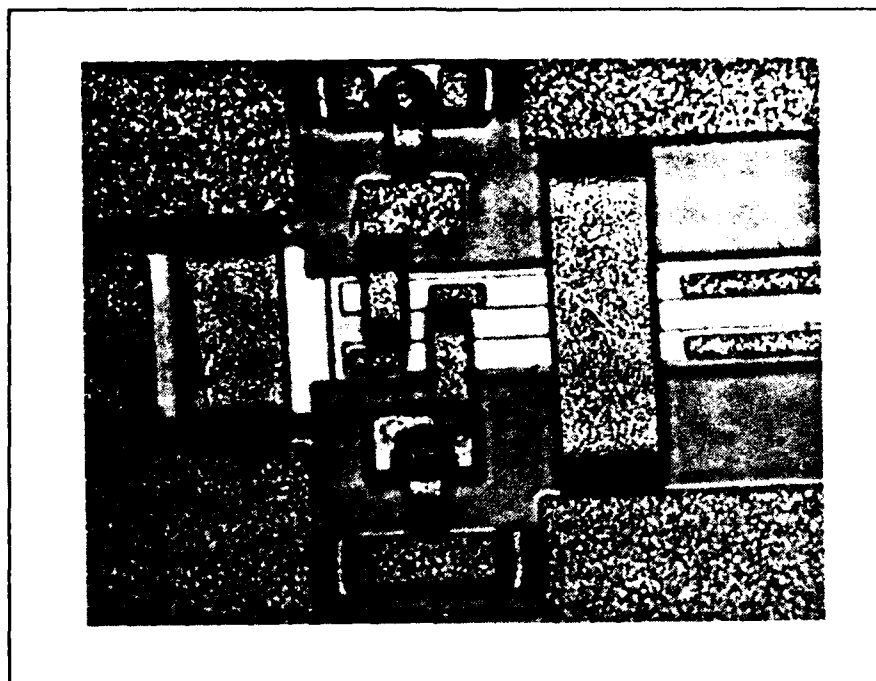


Figure 7.25 Close up of the mutually-coupled air bridges and varactors of the 80/240 GHz tripler.

7.5.2 DC Characteristics

Forward Characteristics:

The forward I-V characteristics for a typical varactor measured on the tripler chip are as follows:

<u>Current</u>	<u>Voltage</u>
10 μ A	0.5355 v
100 μ A	0.6085 v
9 mA	0.8034 v
10 mA	0.8123 v

These data results in an R_s of 6 to 7 ohms and ΔV of 73 mV. The forward biased dc measurements were made using an HF 4145B Parameter Analyzer and a Cascade Microtech wafer prober. The varactor forward biased characteristics of the chips chosen for RF measurements, were confirmed using a current source and a four-wire probe.

Reverse Characteristics:

The typical reverse breakdown ($I = 100 \text{ uA}$) measured on the tripler varactors was between -10 to -12 volts. The typical capacitance-voltage characteristics, measured on the CoDiodes at 1 MHz, are presented in Fig. 7.26. These values compare well with the parallel-plate varactor model (see Section 2.3). For calibration, on-wafer CoDiodes having open anodes were used as a reference.

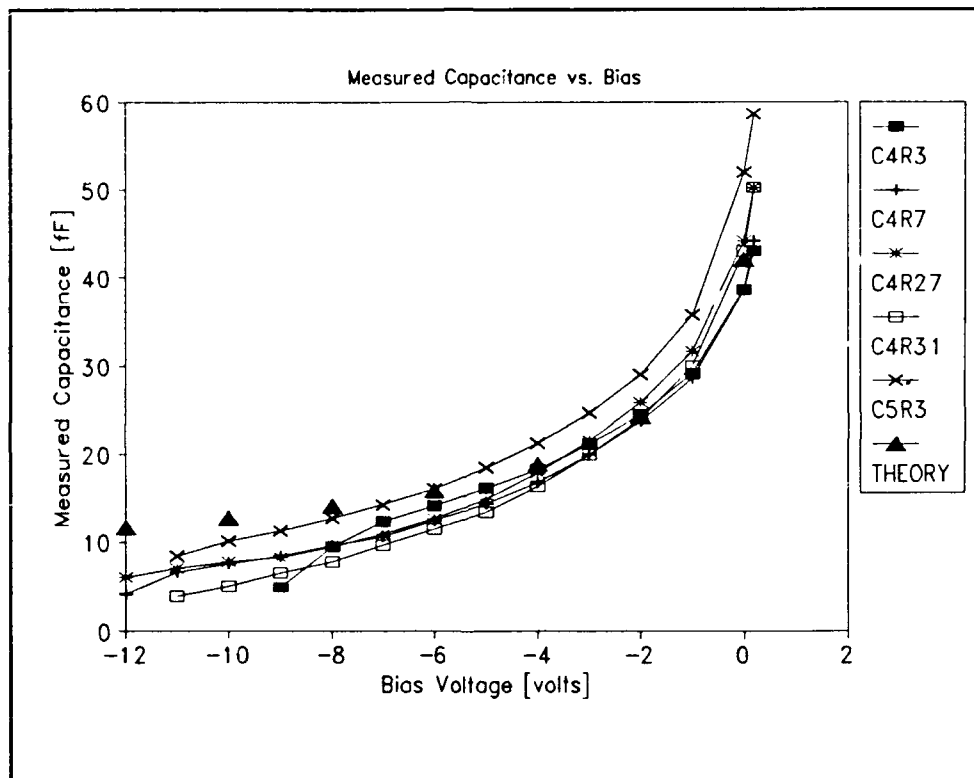


Figure 7.26 Capacitance versus reverse bias for 8 μm diameter CoDiodes on the doubler-tripler wafer. Theoretical values are included for comparison.

From the visual inspection and the dc measurements, approximately 15 chips were candidates for RF testing. The major causes of rejection were high series resistance, open anodes, and physical defects. Therefore it was impossible to obtain a sampling of all nine tripler versions.

7.5.3 Output Power and Efficiency

The output power was measured using the test fixture shown in Fig. 7.27 (similar to the setup described in Chapter Three).

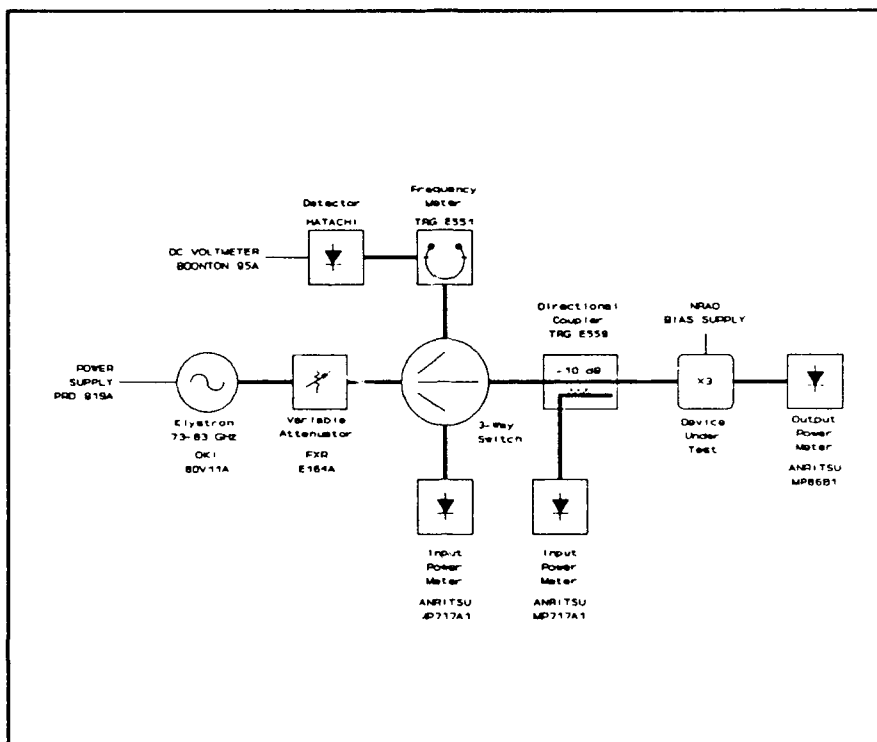


Figure 7.27 Test fixture used to measure output power of the 80/240 GHz tripler.

Because of the many problems encountered during chip and block assembly, many of chips were destroyed by metal liftoff, scratches, excess solder, or substrate cracking. RF measurements were attempted on three tripler chips (two 240-X3-9-180-200 and one 240-X3-9-180-230); the bias voltage and backshorts were adjusted for peak output power at each frequency. A maximum output power of 114 uW at 225 GHz was measured on a 240-X3-9-180-200-A chip with input available power of 110 mW yielding a very low efficiency of 0.1 percent. None of the measured triplers showed proper circuit bias; one bias voltage was always 2 to 3 volts higher than the other. This lack of circuit balance is probably due to asymmetrical

excitation of the input probe (which relies on the conductive epoxy to provide a current path between the ground planes on the chip to neutralize the ground-ground potential). Future designs should include an on-chip air bridge near the probe. The input and output probe backshort was adjusted for maximum output power at each frequency.

7.6 Discussion

The measured results show very low output power and efficiency for the 80/240 GHz tripler as designed. Due to the extreme difficulties in adjusting the tuning backshorts (especially the output port where a crude contacting-type backshort was used), it was decided that small-signal return loss measurements at the ports would not yield consistent data. However, evaluation of the prototype revealed several shortcomings in the design that must be corrected in re-designs of this tripler, hence the following suggestions for future improvements:

- * An air bridge should be used near the input probe to connect the ground planes of the CPW. This will reduce the potential for asymmetrical excitation of the CPW.
- * A low pass filter or tuning stubs should be used on the input line to better isolate the input from the third harmonic.
- * Due the unsatisfactory surface roughness caused by EDM, this machining technique should not be used for waveguides in brass fixtures. Aluminum should be used. Possibly a split-block arrangement should be considered.

CHAPTER EIGHT

The Monolithic High-Power 31/94 GHz Frequency Tripler

8.1 Introduction

Details of the design and evaluation of the high-power monolithic 31/94 GHz frequency tripler are presented in this chapter. The design is based on the 80/240 GHz tripler (see Chapter Seven), but with the incorporation of several improvements such as more effective port isolation, better thermal heat dissipation, and a more compact varactor geometry. The 31/94 GHz tripler is the most complex and the most thoroughly analyzed circuitry presented in this thesis.

The 31/94 GHz tripler specifications were driven by several on-going projects at Martin Marietta Laboratories. At least 25 mW at 94 GHz with an efficiency of greater than 5 percent is currently desired. This chapter presents the details of two design iterations, however further improvements are currently planned. This tripler illustrates the versatility of the CPW design and its potential to meet the needs of current industrial applications.

8.2 Varactor Performance Study

The closed-form nonlinear analysis of Section 2.4 was applied to determine the multiplier performance as a function of the varactor design parameters. Eqns. (2-41) through (2-55) require the following varactor parameters: 1) an abrupt-junction profile, 2) breakdown voltage, 3) built-in potential, 4) zero-biased capacitance, and 5) series resistance. With knowledge of the above parameters and with application of the maximum

symmetrical pumping criterion, the analysis to predict the varactor efficiency, port impedances, and power levels for a specific frequency multiplier (multiplication factor and operating frequency) can be completed. These varactor parameters are directly related to the varactor fabrication variables.

There are two principal varactor fabrication variables that govern multiplier performance: active layer impurity concentration, and the anode diameter. It is these two variables coupled with the avalanche breakdown / punchthrough criterion and skin effect arguments applied to the buffer layer that will establish all other fabrication variables. Therefore, it is important to carefully examine the multiplier performance as a function of these two fabrication variables. The varactor study examines the 31/94 GHz tripler performance (with maximum varactor efficiency at each point) of a single varactor for anode diameters ranging from 15 to 21 microns and active layer impurity concentrations ranging from 10^{16} to 10^{17} cm^{-3} . The results are presented in Table 8.1. These data are also presented in graphical form. The output power (Fig. 8.1), the varactor efficiency (Fig. 8.2), the input resistance (Fig. 8.3), and the output resistance (Fig. 8.4) are presented for the given range of anode diameters and active layer impurity concentrations. Fig. 8.5 shows the average junction capacitance (under the maximum symmetrical voltage swing) as calculated from eqn. (2-44).

TABLE 8.1 31/94 GHz Varactor Tripler Study (single varactor)											
$N_d \cdot 10^{16}$ [cm ⁻³]	d_s [μm]	L_e [μm]	V_{br} [v]	C_{jo} [fF]	C_{avg} [fF]	R_s [Ω]	R_{in} [Ω]	R_{out} [Ω]	P_{abs} [mW]	P_{out} [mW]	Var. Eff. [%]
1.0	15	3.0	67	53.9	12.1	15.2	117.4	58.7	171.2	87.5	51.1
	17			69.2	15.5	12.1	92.2	47.1	221.7	110.6	49.9
	19			86.4	19.4	9.9	74.4	39.0	279.2	135.7	48.6
	21			105.6	23.7	8.3	61.4	33.3	344.1	162.5	47.2
2.5	15	1.4	32	85.2	25.8	4.0	49.9	21.9	95.0	59.4	62.5
	17			109.4	33.1	3.3	39.5	17.7	124.1	74.2	59.8
	19			136.6	41.4	2.8	32.2	14.8	157.8	89.9	57.0
	21			167.0	50.5	2.5	26.9	12.9	197.3	105.5	53.5
5.0	15	0.8	20	120.4	45.2	1.9	28.2	12.5	67.3	41.1	61.1
	17			154.7	58.1	1.7	22.6	10.5	89.3	50.1	56.1
	19			193.2	72.6	1.6	18.7	9.4	115.3	58.8	51.0
	21			236.1	88.6	1.5	15.9	8.9	145.6	66.7	45.8
7.5	15	0.6	15	147.5	63.7	1.5	20.8	9.6	57.3	32.3	56.4
	17			189.5	80.5	1.4	16.9	8.6	76.6	38.4	50.2
	19			236.7	100.5	1.3	14.1	8.4	99.8	43.5	43.6
	21			289.1	122.8	1.3	11.0	8.2	126.6	46.3	36.6
10.0	15	0.5	13	170.3	78.1	1.3	17.1	8.4	53.7	25.9	51.8
	17			218.8	100.3	1.3	14.0	8.1	72.2	40.1	44.5
	19			273.3	125.3	1.2	10.7	7.2	97.8	60.3	38.3
	21			333.8	153.1	1.2	9.3	7.1	126.2	85.3	32.4

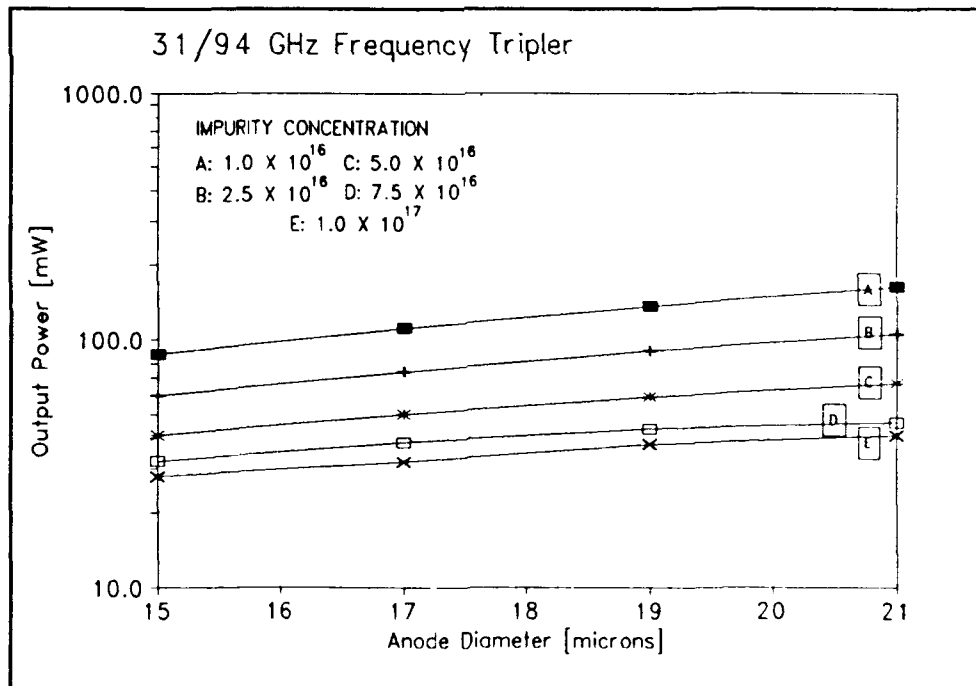


Figure 8.1 Calculated output power as a function of anode diameter. Parameter: active layer impurity concentration.

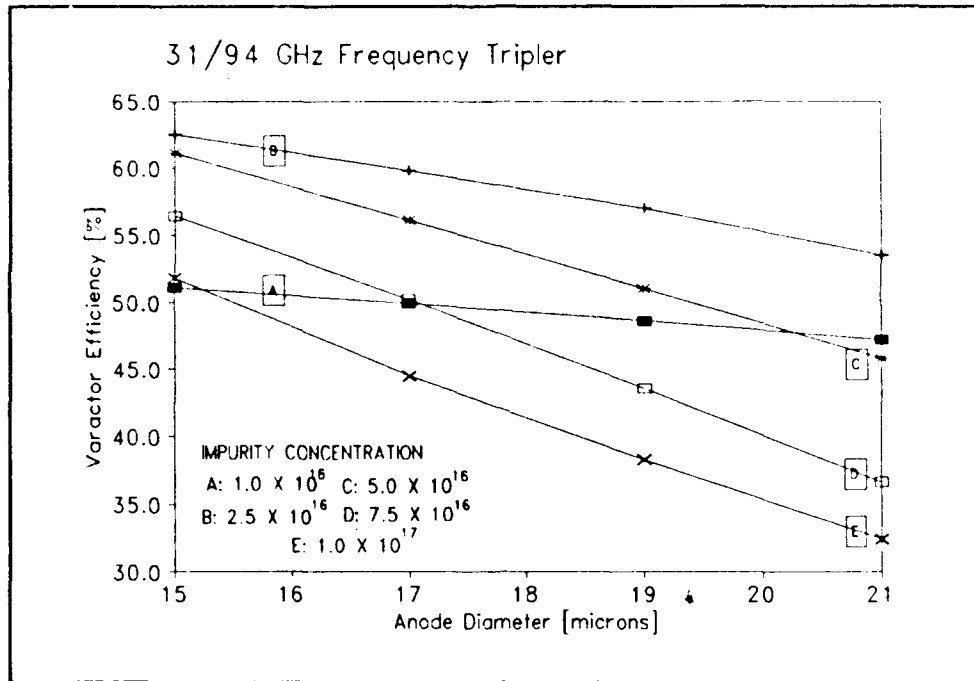


Figure 8.2 Calculated varactor efficiency as a function of anode diameter. Parameter: active layer impurity concentration.

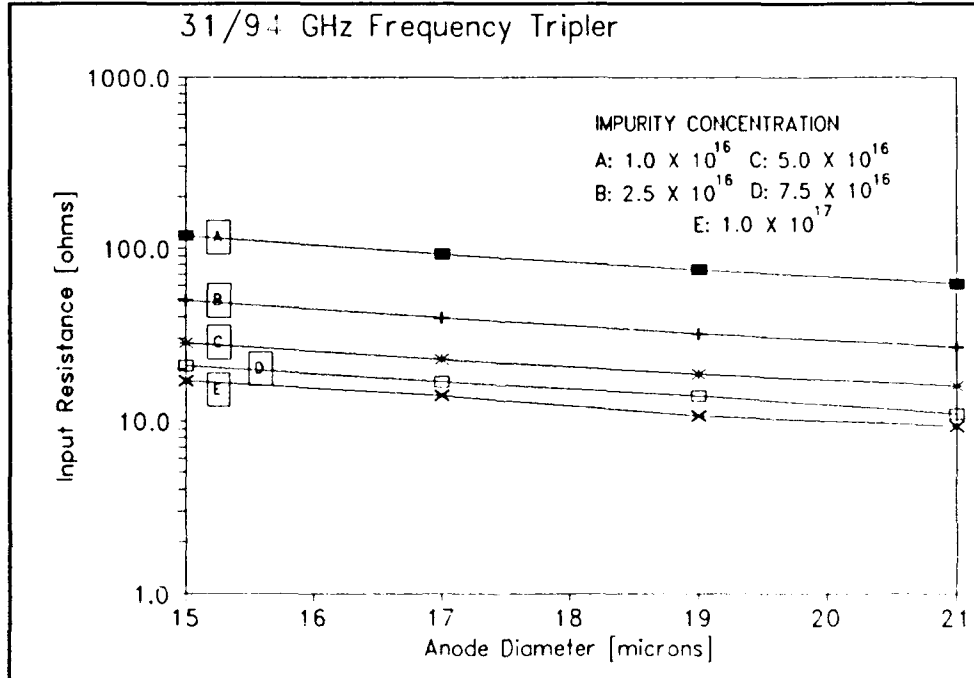


Figure 8.3 Calculated input resistance as a function of anode diameter. Parameter: active layer impurity concentration.

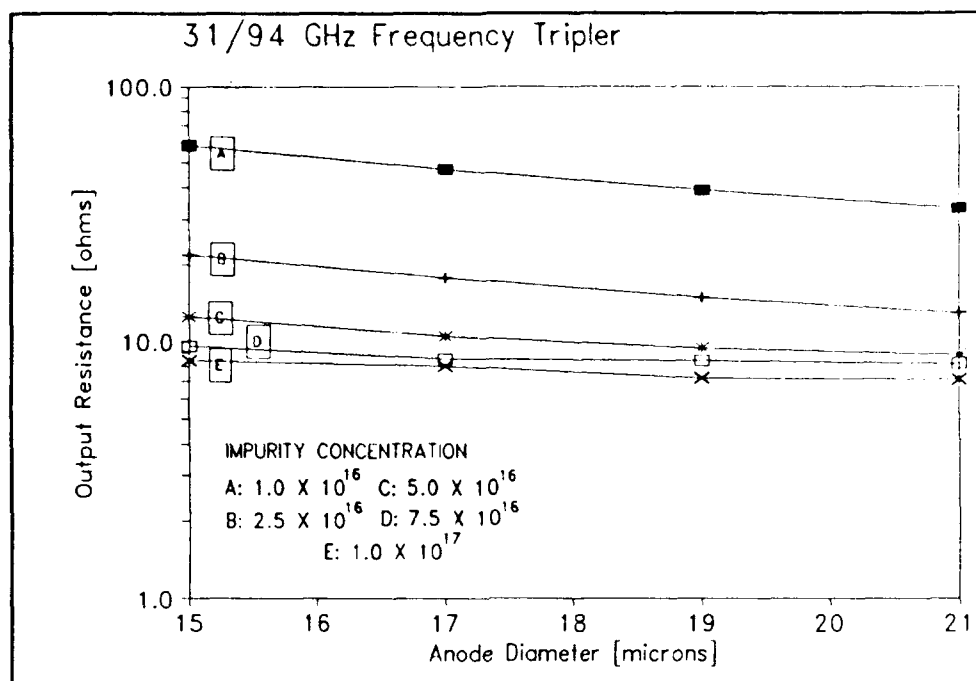


Figure 8.4 Calculated output resistance as a function of anode diameter. Parameter: active layer impurity concentration.

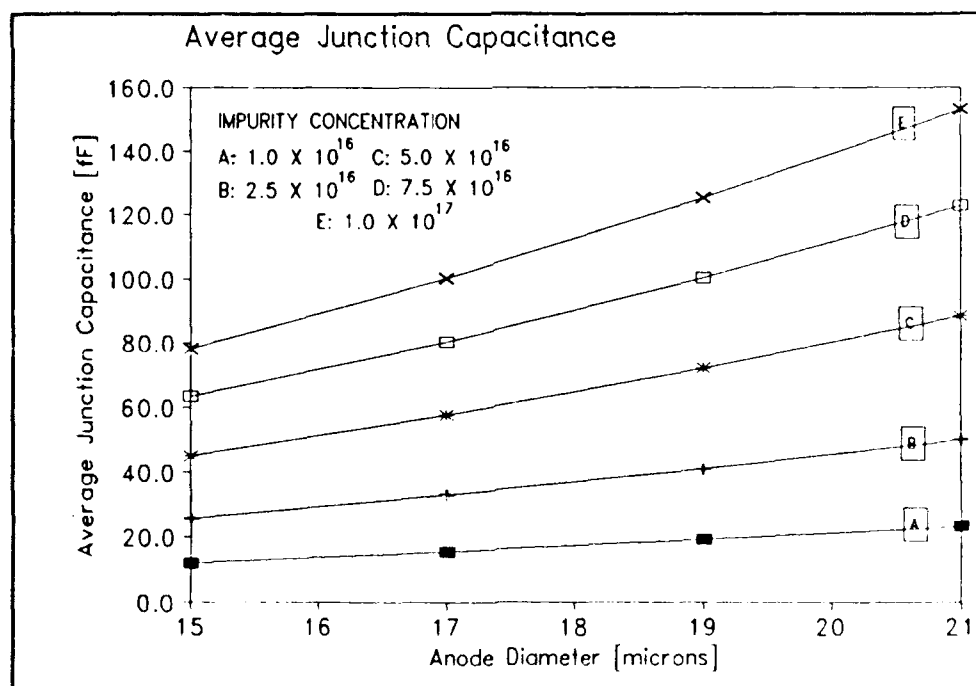


Figure 8.5 Average junction capacitance as a function of anode diameter. Parameter: active layer impurity concentration.

The above survey is for a single varactor, however since the Anti-parallel balanced varactor arrangement (see Chapter Four) will be used in this tripler design, expected power levels will be twice those shown in the figures.

The tripler was designed for $P_{out} = 100 \text{ mW}$ per varactor. Examination of Fig. 8.1 indicates that a $P_{out} = 100 \text{ mW}$ is possible for many combinations of impurity concentration and anode diameter. Because of the high power levels in this design, heat dissipation must be minimized, therefore the curve in Fig. 8.2 that yields maximum varactor efficiency was used (curve B, $n_d = 2.5 \times 10^{16} \text{ cm}^{-3}$). Correspondingly, curve B in Fig. 8.1 indicates that a $P_{out} = 100 \text{ mW}$ is possible with an anode diameter of 20 microns. The input and output impedances can easily be matched to 50 Ω by relatively simple embedding circuitry. Hence, the following varactor was chosen for the 31/94 GHz high power tripler:

FABRICATION VARIABLES:

Anode Diameter: 20 μm
 Junction Profile: ABRUPT
 Act. imp. level: $2.5 \times 10^{16} \text{ cm}^{-3}$
 Active thickness: 1.4 μm
 Buffer thickness: 3.0 μm
 Buffer imp. lev.: $> 4 \times 10^{18} \text{ cm}^{-3}$

VARACTOR PARAMETERS:

$C_{jo} = 150 \text{ fF}$
 $C_{avg} = 45 \text{ fF}$
 $V_{bi} = 1.0 \text{ volts}$
 $V_b = -32 \text{ volts}$
 $R_s = 3.6 \text{ ohms}$

The operating point for best 31/94 GHz tripler performance using this SINGLE varactor is as follows:

Bias voltage:	-15 volts	
Output power at 94 GHz:	100 mW	
Absorbed power at 31 GHz:	181 mW	
Power dissipation:	81 mW	
Varactor efficiency:	55 %	
Input impedance:	30 -j114 ohms	$Q_{input} = 3.8$
Idler impedance:	0 -j 57 ohms	
Output impedance:	15 -j 38 ohms	$Q_{output} = 2.5$

The Siegel-Kerr program (see Section 2.5) was used to verify the above performance calculations and to gain additional information about the behavior of the tripler as a function of available input power and bias voltage. The results, presented in Table 8.2, show that both calculations are in close agreement at the maximum efficiency point where the bias is -15 volts and the input absorbed power is 200 mW.

The single device equivalent circuit approach allows the above results to be applied directly to the ANTI-PARALLEL configuration, noting that independent biasing of the two Schottky varactors was necessary. The embedding circuitry was then designed around these specified varactors.

TABLE 8.2 Large-signal Nonlinear analysis of 31/94 GHz Tripler Using Siegel-Kerr Program					
FIXED EMBEDDING IMPEDANCES:					
INPUT: 30 +j114		IDLER: 0 +j57		OUTPUT: 15 +j38	
BIAS VOLTAGE [V]	AVAILABLE POWER [mW]	ABSORBED POWER [mW]	OUTPUT POWER [mW]	INPUT IMPEDANCE [OHMS]	VARACTOR EFF. [PERCENT]
-10	50	46.9	19.1	18.0 -j113	40.7
	100	97.9	45.6	22.3 -j113	46.6
	150	148.6	70.5	24.8 -j112	47.4
	200	197.1	92.1	26.0 -j111	46.7
-15	50	42.5	18.3	14.4 -j122	43.0
	100	96.5	49.4	21.9 -j120	51.2
	150	148.5	80.3	26.2 -j119	54.1
	200	199.5	109.6	29.1 -j118	54.9
-20	50	14.9	3.2	5.6 -j146	21.4
	100	66.4	30.5	13.1 -j137	45.9
	150	124.3	65.5	19.1 -j133	52.7
	200	178.2	98.8	23.3 -j131	55.4
-25	50	5.1	0.2	3.5 -j168	3.1
	100	15.2	2.3	4.6 -j163	14.9
	150	45.7	16.2	8.1 -j155	35.4
	200	107.8	52.2	14.1 -j149	48.5

8.3 Monolithic Circuit Design and Realization

Conductor-backed coplanar waveguide (CBCPW) was chosen for this monolithic tripler design to improve heat dissipation and simplify circuit

mounting. Complete details of the CBCPW line characteristics and discontinuities (including air bridge inductance) are presented in Chapter Five and Appendix E. The CBCPW transverse slab probe (see Appendix F) was used to couple the output signal to a WR-10 rectangular waveguide. At the input, a bonding pad was used so that a ribbon wire could be easily attached to the CBCPW (the other side of the ribbon wire is attached to a microstrip line on the carrier block). The bonding pad shape was designed for mating with the Cascade Microtech wafer prober.

The input, output, and idler circuits were designed to provide conjugate-matched embedding impedances to those predicted by the analysis of Section 8.2. It is essential that circuit symmetry be preserved throughout this design to prevent unwanted propagation modes on the CBCPW from being generated. Because high frequency applications of CBCPW and related discontinuities (tee junctions, stubs, etc.) are not well understood beyond the scaling data presented in this thesis, a "minimum circuit complexity" approach was adopted, and therefore only relatively simple, narrow bandwidth embedding circuits were considered for the initial design. However, despite the advantages of harmonic separation in balanced circuitry, the embedding circuitry is complicated by the fact that circuit elements near the varactors are within the input, idler, and output circuits. For example, if a lumped inductance is placed near the varactor to resonate the average junction capacitance at the idler frequency, then the inductive reactance is much too large for the output circuit and too small for the input circuit. A novel solution to the problem is the "mutual tuning" approach which involves coupled inductances. The coupling is arranged such that the mutual inductance

will be positive in the idler circuit and negative in the output circuit, hence resulting in simultaneous tuning. The large amount of inductive reactance needed at 31 GHz is supplied by the input circuit.

The first iteration of the monolithic 31/94 GHz frequency tripler chip will now be described. A scale drawing of the chip's top side lithography is shown in Fig. 8.6. Fig. 8.7 is a close-up of the region near the varactors. Not shown in the figures are the many via holes that are spaced less than 300 microns apart in a pseudo-random fashion to connect the upper and lower ground planes. For the purpose of discussion, the circuit can be separated into three sections: 1) the varactors and mutually-coupled air bridges, 2) the input network including bias lines, and 3) the output network. The location where all three circuits are connected together will be referred to as the point of intersection.

8.3.1 Varactors and Mutually-Coupled Air Bridges

An equivalent circuit for the varactors and mutually-coupled air bridges is shown in Fig. 8.8. Each varactor anode is connected to the embedding circuitry by a short air bridge ("a" in Fig. 8.7) having about 0.008 nH inductance. The larger mutually-coupled air bridges ("b" in Fig. 8.7) attach the varactors to the main CBCPW.

The self-inductance of each large air bridge is about 0.1 nH as calculated by the analysis presented in Chapter Five. The mutual inductance of these air bridges, M_b , was found to be 0.03 nH (see Appendix I for details). As shown in Fig. 8.9, when the currents are in opposite directions, this mutual inductance is negative (case A), and when the

Monolithic 31/94 GHz Frequency Tripler

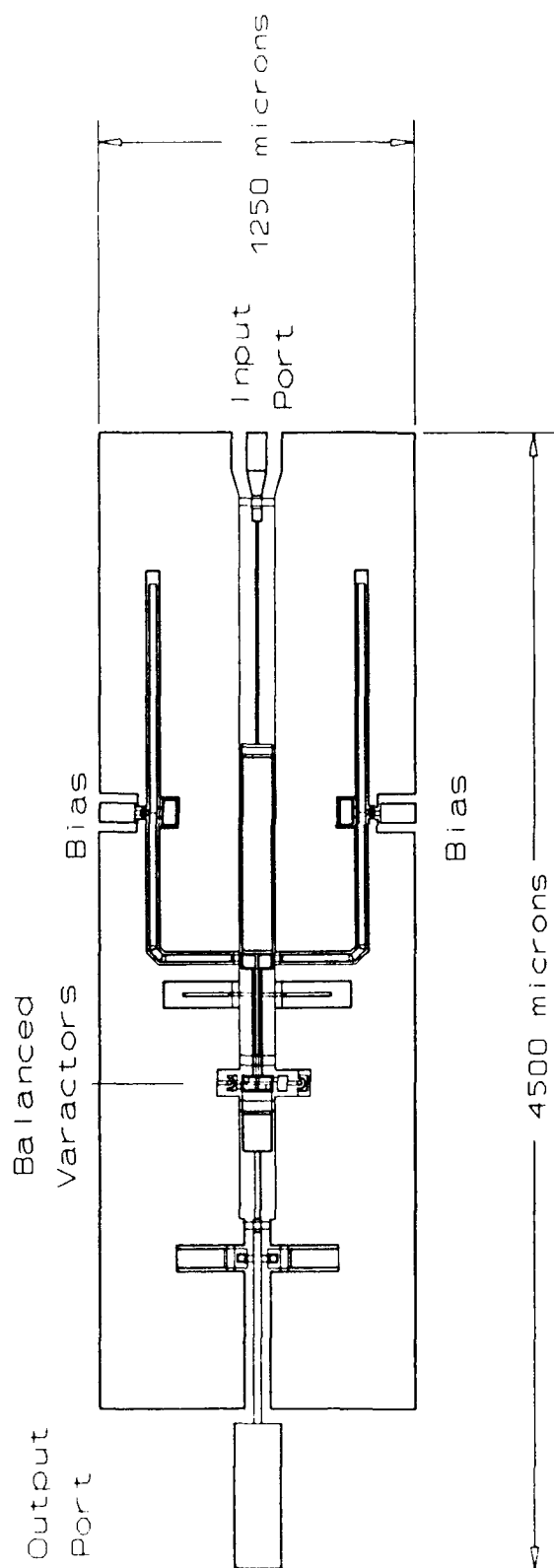


Figure 8.6 Scale drawing of the monolithic 31/94 GHz frequency tripler. (First iteration)

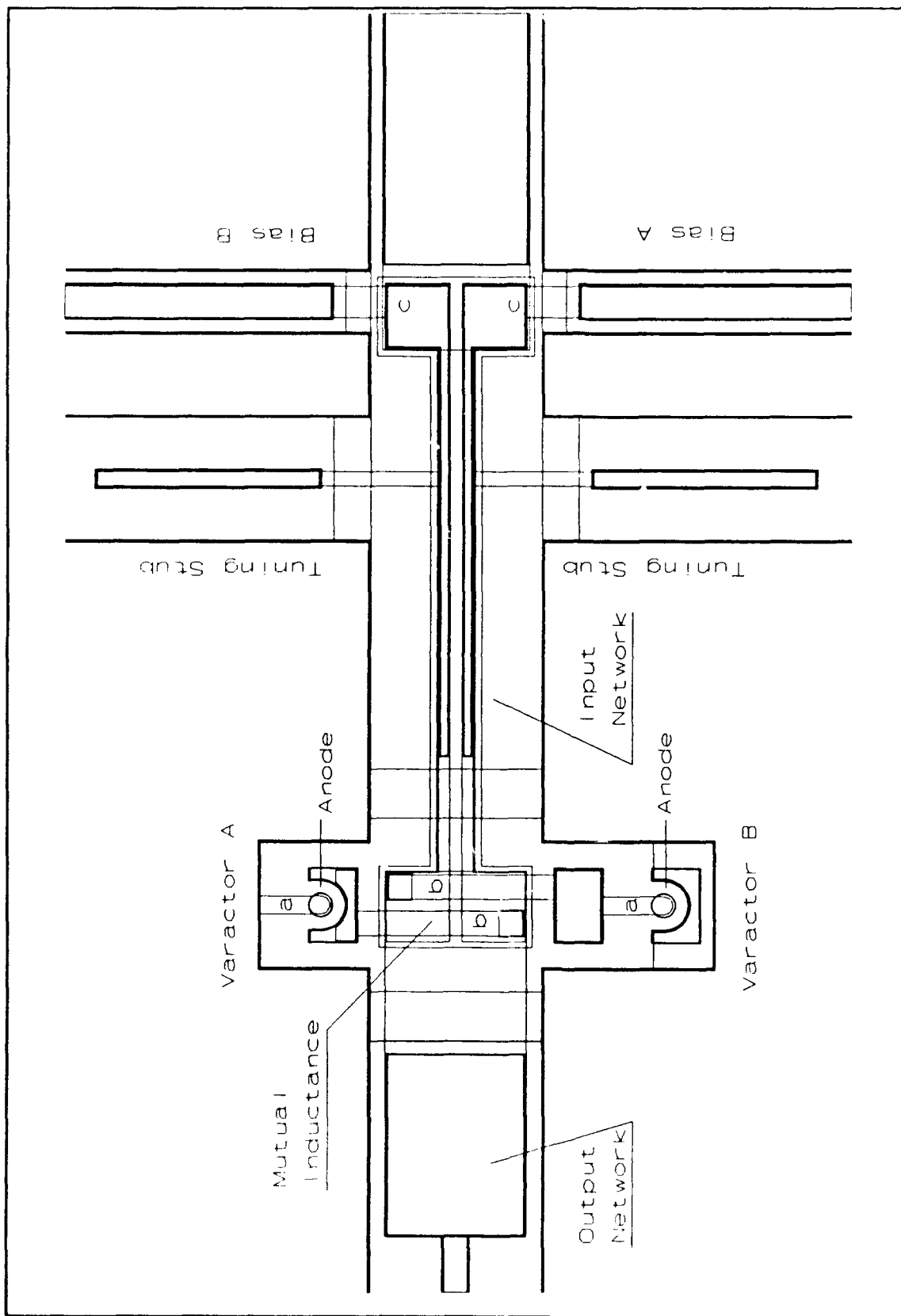


Figure 8.7 Close up of the monolithic 31/94 GHz tripler showing the varactor region. (First iteration)

currents are in the same direction, this mutual inductance is positive (case B).

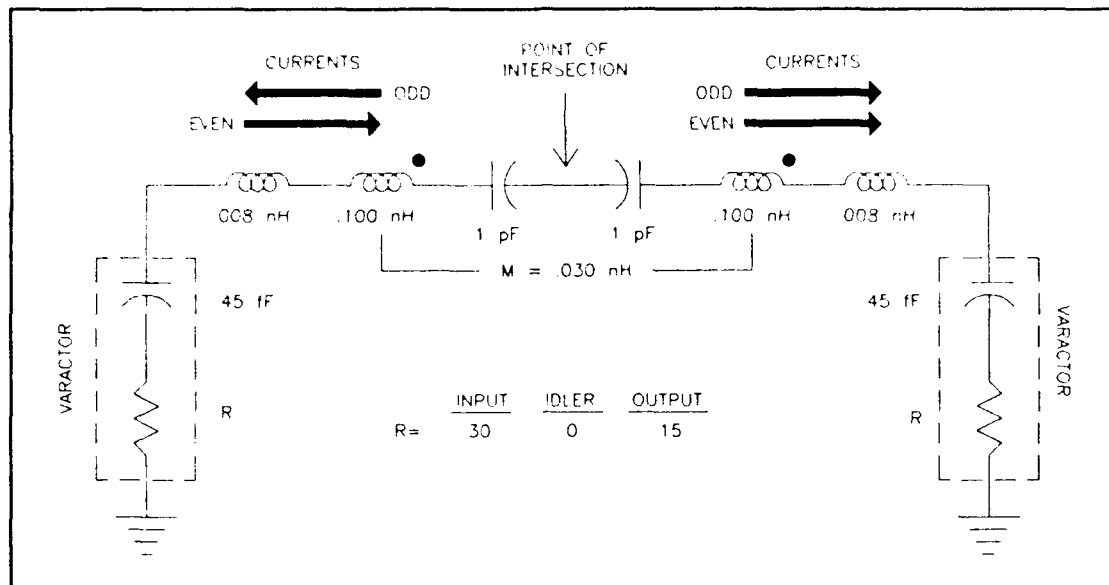


Figure 8.8 Equivalent circuit for the varactors and mutually-coupled air bridges.

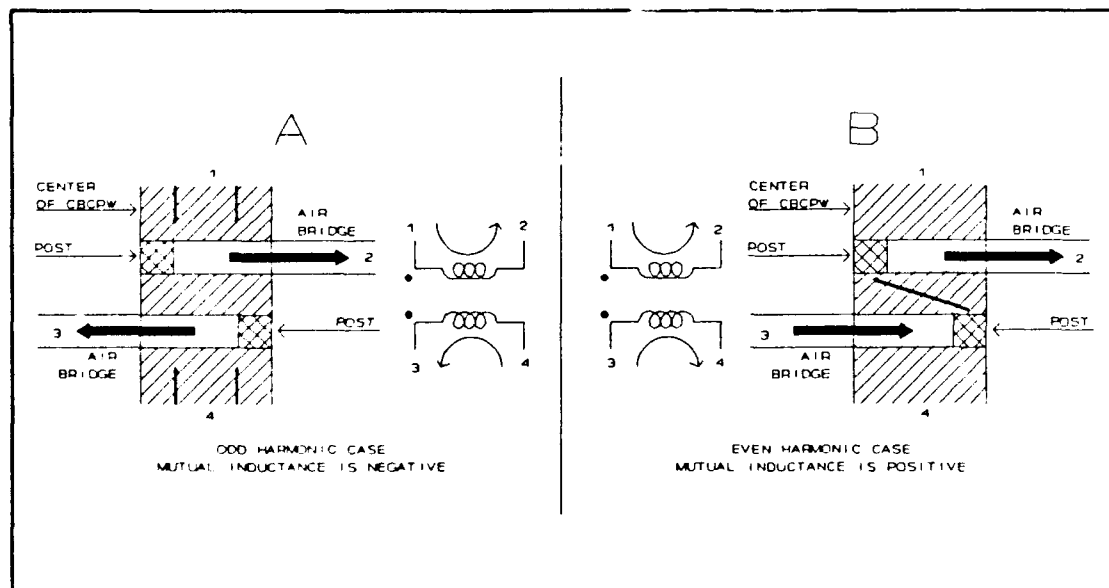


Figure 8.9 Mutual inductance (M) orientations used in the MMIC tripler design. Case A for odd harmonics (M is negative), and case B for even harmonics (M is positive). Compare with Fig. 8.7.

Table 8.3 summarizes the calculated circuit impedances at 31, 62, and 93 GHz. The total impedance as seen from the point of intersection is

also given. Currents at the input and output frequencies see the two varactors in anti-parallel while the currents at the idler frequency transverse the varactor loop and see the two varactors in series. Note that in the first iteration, the parasitic shunt capacitance across the varactors was considered very small in comparison with the average junction capacitance so it was not included in this circuit model.

TABLE 8.3 Circuit impedances at the intersection point Varactors and mutually-coupled air bridges			
Component	31 GHz	62 GHz	93 GHz
Varactor:	30 -j114.0	0 -j57.0	15 -j38.0
Contact Finger:	+j 1.5	+j 3.1	+j 4.7
Large air bridge:	+j 19.5	+j39.0	+j58.4
Mutual inductance:	-j 5.8	+j11.7	-j17.5
Coupling capacitance:	-j 5.1	-j 2.5	-j 1.7
Circuit impedance at intersection:	15 -j 52.0	0 -j 0.7	7.5+ j2.9
Diode connection:	(parallel)	(series)	(parallel)

8.3.2 Input Network including Bias Lines

The equivalent circuit for the input section is shown in Fig. 8.10. The primary purpose of the input section is to match the impedance shown in Table 8.3 (31 GHz) to a 50 ohm source. At 31 GHz, a substantial capacitive reactance is present at the point of intersection. This reactance is resonated by a short section of 55 ohm CBCPW (length 425 microns) to yield an impedance of about 10 ohms real. It is at this point (referred to as the bias intersection) that the bias lines are attached to the main CBCPW (Fig. 8.7, point c).

To match the 10 ohms real to the 50 ohms source, a two-step quarter-wave transformer (31 GHz) is used. This structure is formed using a 24 ohm (length = 886 microns) CBCPW followed by a 74 ohm (length = 886

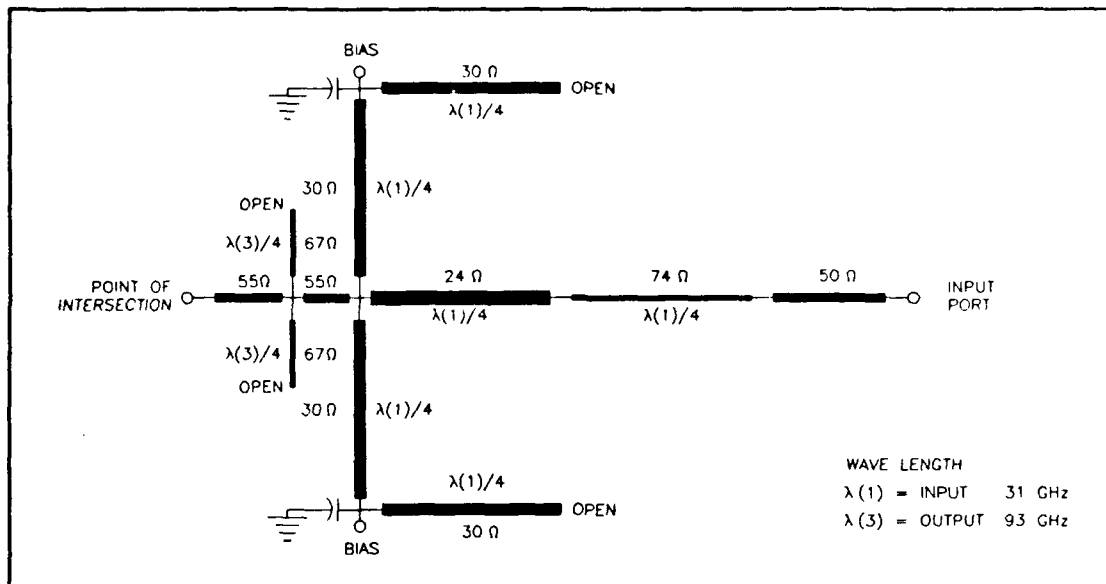


Figure 8.10 Equivalent circuit of the input section including the bias lines.

microns) CBCPW. The input port of the tripler consists of an 80 microns wide pad which geometrically matches the dimensions of an on-wafer test probe. This pad can be used with the test probe or as a bonding pad.

Each bias line consists of a quarter-wavelength (31 GHz) open stub (CBCPW with $Z = 36$ ohms and length = 886 microns) producing an RF short where the bias wire bonding pad is attached. A filter capacitor of about 1 pF is also attached at this point. The bias line is attached to the main CBCPW via an additional quarter-wavelength (31 GHz) section thus producing an RF open at the bias intersection (see Fig. 8.7, point c). Independent biasing is achieved by a stacked metal/dielectric/twin-metal strip along the main CBCPW as shown in Fig. 8.11. The two strips yield independent dc paths to each varactor while the entire structure appears as a single coplanar waveguide due to the large capacitive coupling of the strips. The electrically small geometry of the structure as compared with the operation wavelength insures that unwanted moding (excitation of the

parallel-plate line formed by the stacked structure) will not occur. The parallel plate capacitance is $0.375 \text{ fF}/\mu^2$ (see section 5.5.2). The SiN thickness is 200 Angstroms.

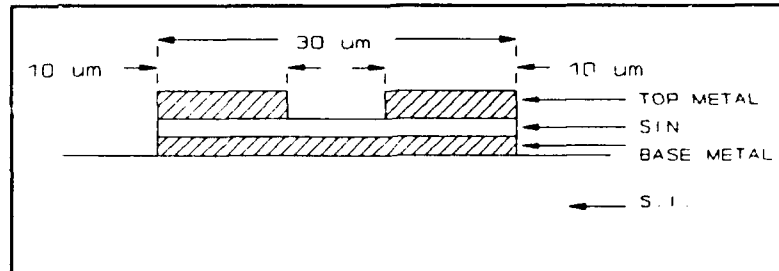


Figure 8.11 Center conductor of CBCPW structure for independent dc biasing. (Not to scale).

The input circuitry is isolated from the 94 GHz signal by a pair of symmetrical open stubs which are a quarter-wavelength long (94 GHz). The stubs are placed a quarter-wavelength (94 GHz) from the point of intersection thus yielding an RF open there. The input circuit is isolated from the idler currents because of circuit balance.

A summary of the input network's transmission line characteristics (including loss) is presented in Table 8.4. An estimate of the total circuit loss through the input network is also given (g = CPW ground-ground spacing and s = CPW center conductor width).

TABLE 8.4 Summary of CBCPW Characteristics Input Network					
LINE	g [μm]	s [μm]	LENGTH [μm]	LOSS/LEN. [dB/ μm]	LOSS [dB]
50 ohm	140	41	100	.000162	.02
74 ohm	140	10	886	.000221	.20
24 ohm	140	120	886	.000212	.19
55 ohm	140	31	425	.000182	.08
67 ohm	100	12	2x 270	.000221	.12
36 ohm	50	30	4x 886	.000361	1.28
Estimated total circuit loss in the input network:					1.90 dB

8.3.3 Output Network

The equivalent circuit for the output network is shown in Fig. 8.12.

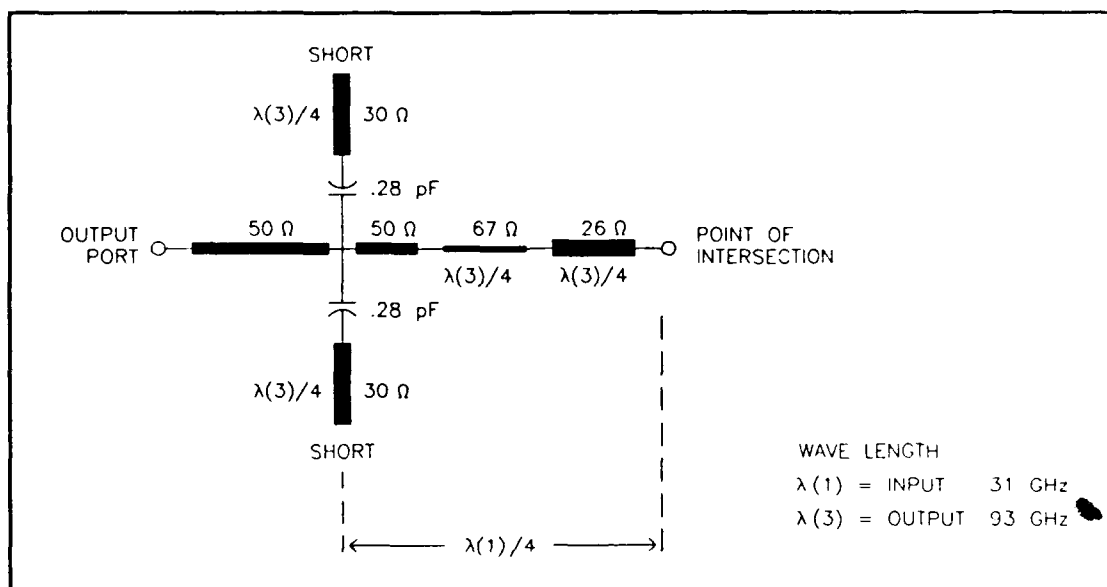


Figure 8.12 Equivalent circuit for the output network.

Table 8.3 shows that the varactor circuit impedance at 93 GHz has a very small inductive component and hence no additional compensation is necessary. The real 6.5 ohms is transformed to 50 ohms using a two-step quarter-wave transformer formed using a $Z = 26$ ohms, 270 microns length of CBCPW followed by a $Z = 67$ ohms, 270 microns length of CBCPW. A section of 50 ohms CBCPW is used to connect to the rectangular waveguide probe.

The output port is isolated from 31 GHz by a pair of special quarter-wavelength (94 GHz) shorted stubs. The stubs are attached to the main CBCPW via a series capacitance of 0.28 pF. The stubs provide an open at 94 GHz, however the capacitance series resonates the shorted stub at 31 GHz thus yielding a short where the stub/capacitor attaches to the main CBCPW. The stubs are located a quarter-wavelength (31 GHz) from the intersection point thus appearing as an RF open there. The output circuit like the input circuit is isolated from the idler by circuit balance.

A summary of the transmission line characteristics (including loss) is presented in Table 8.5. An estimate of the total circuit loss through the output network is also given. An additional 0.3 dB of loss for the rectangular waveguide probe is included in the total loss estimate. Loss associated with the input stubs is small in comparison with the loss of the output network and hence is not included in the table.

TABLE 8.5 Summary of CBCPW Characteristics Output Network					
LINE	g [um]	s [um]	LENGTH [um]	LOSS/LEN. [dB/um]	LOSS [dB]
50 ohm	140	41	355	.000300	.11
30 ohm	100	75	2x 270	.000415	.22
67 ohm	140	23	270	.000415	.11
26 ohm	140	115	270	.000366	.10
Estimated total circuit loss in the output network: (includes 0.3 dB for waveguide probe)					.84 dB

8.3.4 Embedding Impedances and Overall Tripler Performance

The embedding impedances of all three networks were examined as a function of frequency. The circuit simulator TouchStone was used to calculate the impedances presented at the point of intersection by the input, idler, and output networks. Fig. 8.13 shows the REAL part and Fig. 8.14 shows the IMAGINARY part of the intersection impedance from 26 to 36 GHz. Fig 8.15 shows the REAL part and Fig. 8.16 shows the IMAGINARY part of the intersection impedance from 84 to 104 GHz. Near the designed operating point, the input impedance was independent of the output port termination and the output impedance was independent of the input port termination.

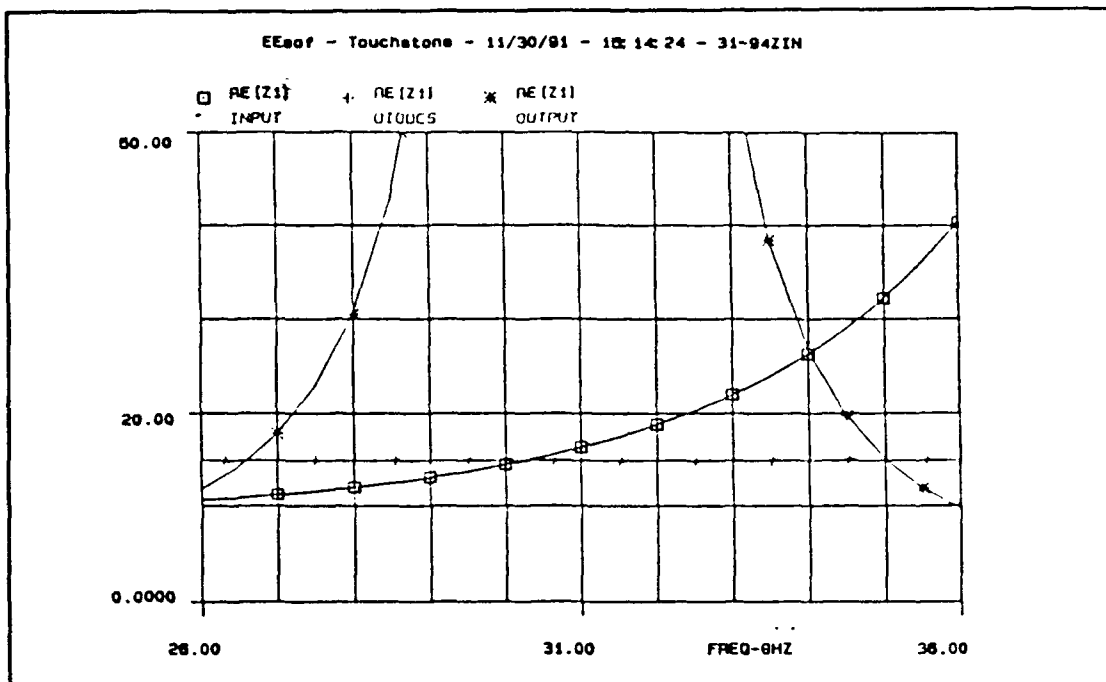


Figure 8.13 REAL part of intersection impedances for input, output, and varactor networks from 26 to 36 GHz.

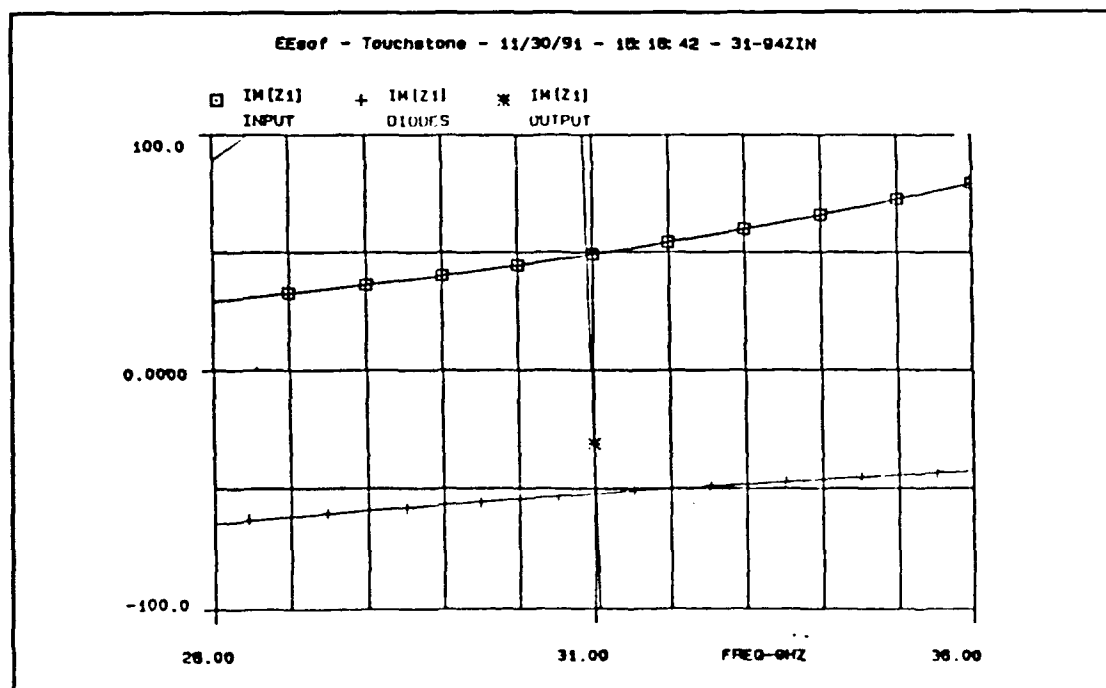


Figure 8.14 IMAGINARY part of the intersection impedances for the input, output, and varactor networks from 26 to 36 GHz.

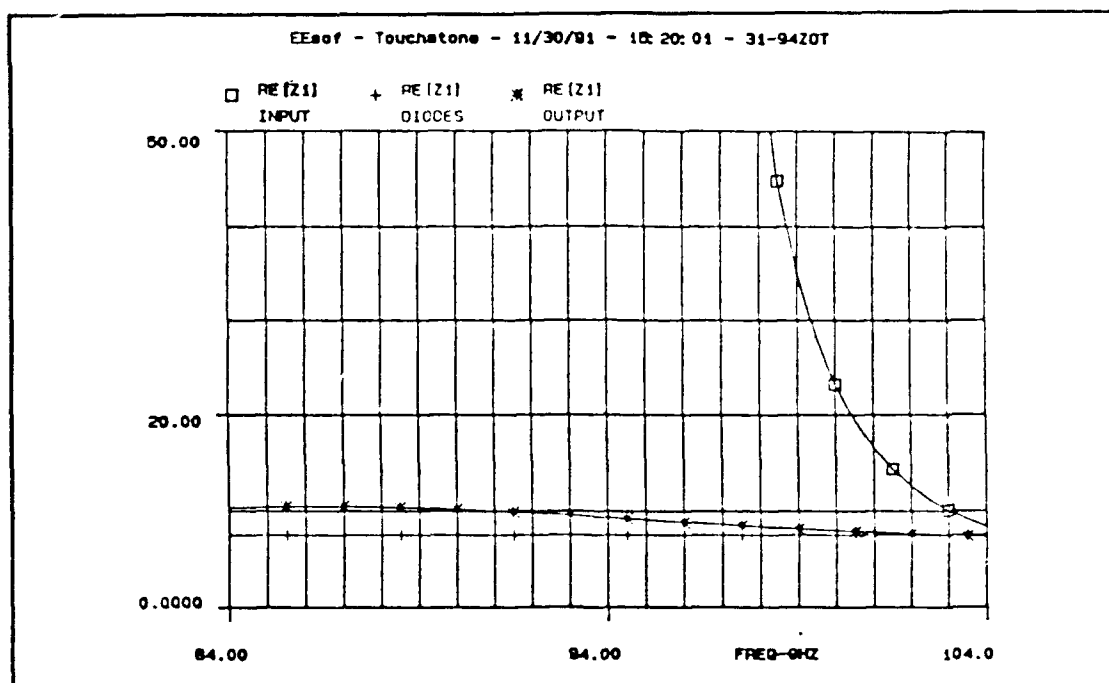


Figure 8.15 REAL part of intersection impedances for the input, output, and varactor networks from 84 to 104 GHz.

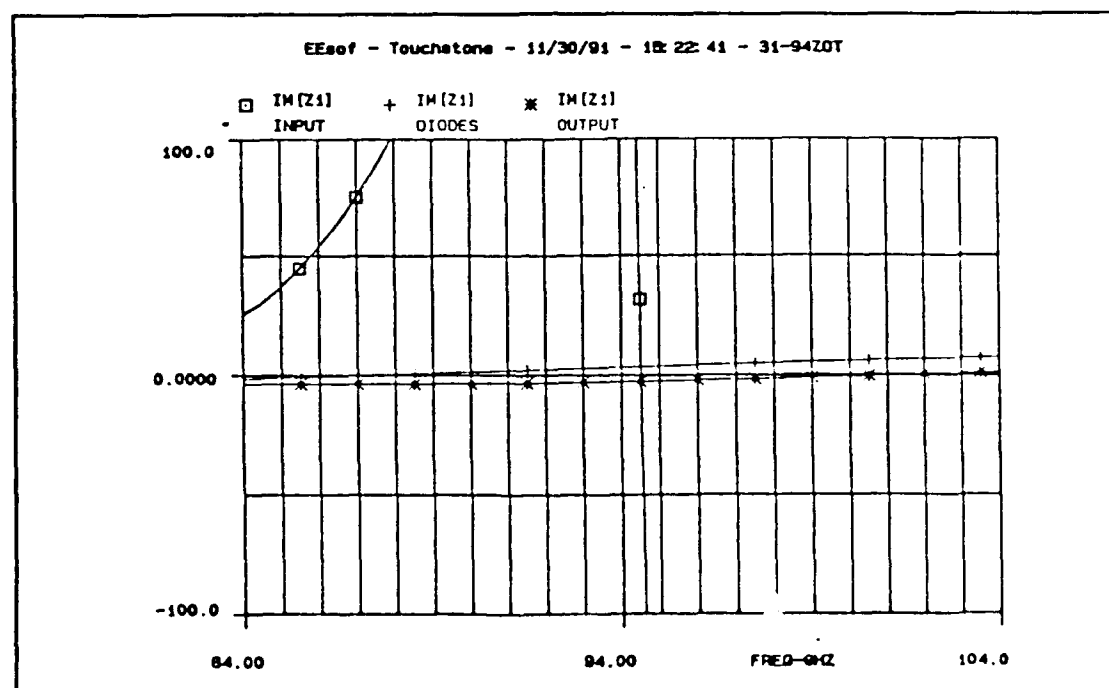


Figure 8.16 IMAGINARY part of the intersection impedances for input, output, and varactor circuits from 84 to 104 GHz.

From these data, the embedding impedances at the varactors for 29/87, 31/93, and 33/99 GHz operation were calculated and are presented in Table 8.6.

TABLE 8.6 Embedding Impedances versus Frequency First Iteration			
Pump Frequency	Embedding Impedances [ohms]		
	INPUT	IDLER	OUTPUT
29 GHz	22.0 +j 77	0 +j 47	20.6 +j 35
31 GHz	36.8 +j105	0 +j 52	19.1 +j 38
33 GHz	77.1 +j148	0 +j 55	16.1 +j 44

The nonlinear analysis program of Siegel and Kerr was used together with the embedding impedances presented in Table 8.6 to calculate the performance of the tripler as a function of frequency. Conductive losses in the embedding circuits are also included. The best performance at each frequency is shown in Table 8.7.

TABLE 8.7 Predicted Tripler Performance versus Frequency BALANCED VARACTOR CIRCUIT Siegel and Kerr Program					
Pump Frequency [GHz]	Bias Voltage [volts]	Available Power [mW]	Output Power [mW]	Input Impedance [ohms]	Efficiency [percent]
29	-10	500	123.8	26.1 -j102	24.7
31	-15	500	131.4	29.3 -j109	26.3
33	-15	500	71.8	18.4 -j113	14.4

The efficiency calculations in Table 8.7 are based on the monolithic tripler output power and the available power at the tripler input port.

8.3.5 Heat Dissipation

The nonlinear analysis suggests that for 500 mW pump power, each varactor will dissipate approximately 150 mW. A sketch of the thermal model of the varactor is shown in Fig. 8.17.

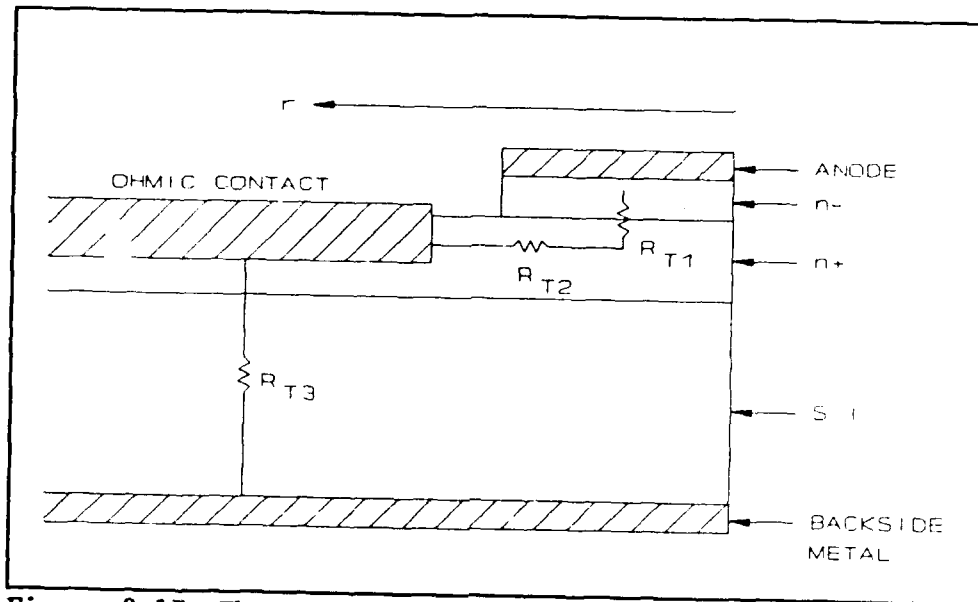


Figure 8.17 Thermal conductivity model for the varactor.

For this analysis, a worst-case scenario is depicted and the assumed heat transport mechanism is one-dimensional conduction. The thermal energy, which is primarily generated in the varactor active layer, flows into the buffer layer through R_{T1} :

$$R_{T1} = \frac{1.25 \text{ } \mu\text{m}}{k_s A_1} = 79.6 \text{ K/W} \quad (8-1)$$

where the thermal conductivity of the GaAs, k_s , is $5 \times 10^{-5} \text{ W } \mu\text{m}^{-1} \text{ K}^{-1}$ (Sze, 1981), and the anode area, A_1 , is $314 \text{ } \mu\text{m}^2$. The heat then flows through the buffer layer (with resistance R_{T2}) to the ohmic contact. This is radial conduction with R_{T2} as

$$R_{T2} = \frac{\ln \frac{r_o}{r_a}}{2 \pi k_s L_b} = 334.1 \text{ K/W} \quad (8-2)$$

with the anode radius $r_a = 10 \text{ } \mu\text{m}$, the inner radius of the ohmic contact $r_o = 13 \text{ } \mu\text{m}$, and the buffer layer thickness $L_b = 2.5 \text{ } \mu\text{m}$. The heat that flows from the ohmic contact through R_{T3} to the back-side metal which is in direct contact with the carrier block (infinite heat sink). R_{T3} is given by

$$R_{T3} = \frac{75 \text{ } \mu\text{m}}{k_s A_3} = 312.5 \text{ K/W} \quad (8-3)$$

where $A_3 = 4800 \text{ } \mu\text{m}^2$ ($80 \text{ } \mu\text{m} \times 60 \text{ } \mu\text{m}$). The total thermal resistance is

$$R_T = R_{T1} + R_{T2} + R_{T3} = 726.2 \text{ K/W} \quad (8-4)$$

The active layer temperature rise for 150 mW dissipation per varactor is therefore 109 K, which is much less than the melting temperature of the metals near the anode. The only consequence of the elevated temperature is to increase the intrinsic carrier concentration, however the intrinsic temperature i.e. the temperature at which the thermally generated carrier concentration equals the impurity concentration, is greater than 700 degrees C for $2.5 \times 10^{16} \text{ cm}^{-3}$ doped GaAs. Therefore, it is concluded that the varactor operating point will not be significantly altered as a result of the elevated temperature.

8.4 Design Variations (First Iteration)

Four versions of the 31/94 GHz monolithic frequency tripler were fabricated at Martin Marietta Laboratories as described in Section 5.7 of this thesis. The variations, which are outlined in Table 8.8, yield a

systematic yet independent modification of the input tuning and idler/output tuning. The self inductance of the mutually coupled air bridges is 0.07nH for the 50 micron overlay length, however the mutual inductance is very small (0.005nH).

TABLE 8.8 31/94 GHz Tripler Variations			
CHIP NUMBER	ANODE DIA.	INPUT TUNING	MUTUAL IND. OVERLAP
94 X3 20 50 425 A	20 μm	425 μm	< 50 μm
94 X3 20 50 500 A	20 μm	500 μm	< 50 μm
94 X3 20 109 425 A	20 μm	425 μm	109 μm
94 X3 20 109 500 A	20 μm	500 μm	109 μm

Also included on this wafer was a test structure used to characterize a sample varactor. The structure consists of a 20 micron diameter varactor in series with a coplanar waveguide (CoDiode structure) as shown in Fig. 8.18. Fabrication of the first wafer (first iteration) was completed on August 15, 1991. The measured results are described in Section 8.5.

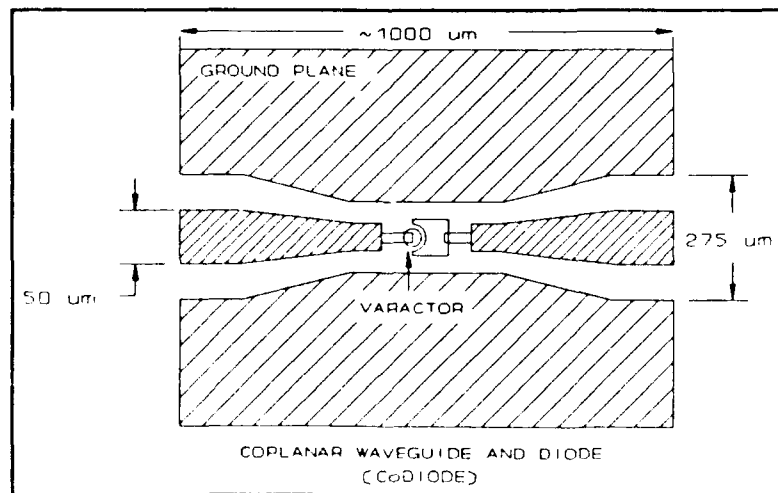


Figure 8.18 Sketch of CoDiode structure.

8.5 Results - First Iteration

The tripler was evaluated on the basis of 1) a visual inspection, 2) the dc characteristics, 3) the small signal return loss at input and output, 4) the output power and efficiency versus frequency, and 5) the output power and efficiency versus input power. All dc measurements were made on wafer or on an individual chip mounted on a glass microscope slide. For RF measurements, a "carrier" block, designed by E. Schlecht at Martin Marietta Labs, was used to provide access to the RF input and output ports as well as for dc bias connections. The carrier input port consists of a coaxial-to-microstrip transition and an approximately 1.0" length of 50 Ω microstrip. A ribbon bond wire is attached from the microstrip to the input of the tripler chip. The other end of the microstrip is attached to a female SMA connector. Input line loss is estimated to be 0.7 dB at 31 GHz. At the output, the carrier forms the rectangular waveguide section of the slab-type probe (see appendix F). A sketch of this carrier block is shown in Fig. 8.19.

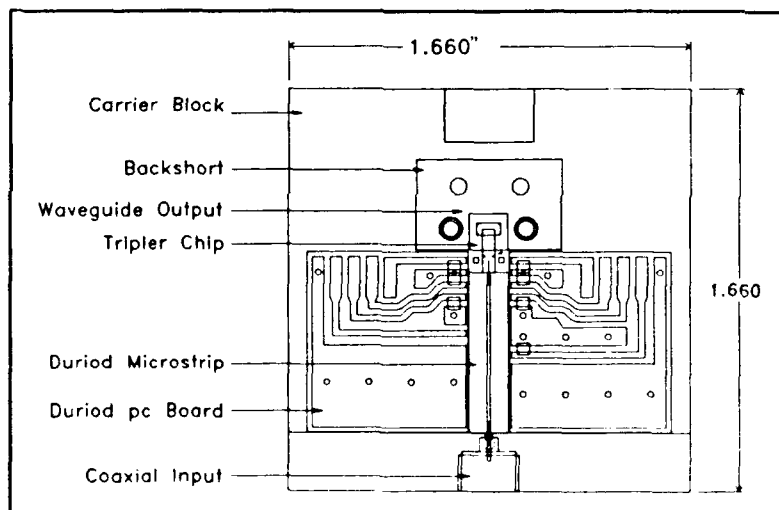


Figure 8.19 Sketch of carrier block used for RF testing the 31/94 GHz tripler. The block was designed by E. Schlecht at MML.

8.5.1 Visual Inspection

Fig. 8.20 is a photograph of the 31/94 GHz monolithic frequency tripler top side processing as it appears prior to chip dicing. The output probe is just off the left side of the photograph. Fig 8.21 is a closeup view of the varactor region showing the mutually coupled air bridges and the two wide air bridges connecting the ground planes. Fig. 8.22 is a closeup of one varactor anode and ohmic contact. The lithography appears to be quite sharp and no residuals of the fabrication process are evident. However, because of overplating, the plated metal near the anodes has formed small spurs that span the anode-ohmic contact gap on some varactors.

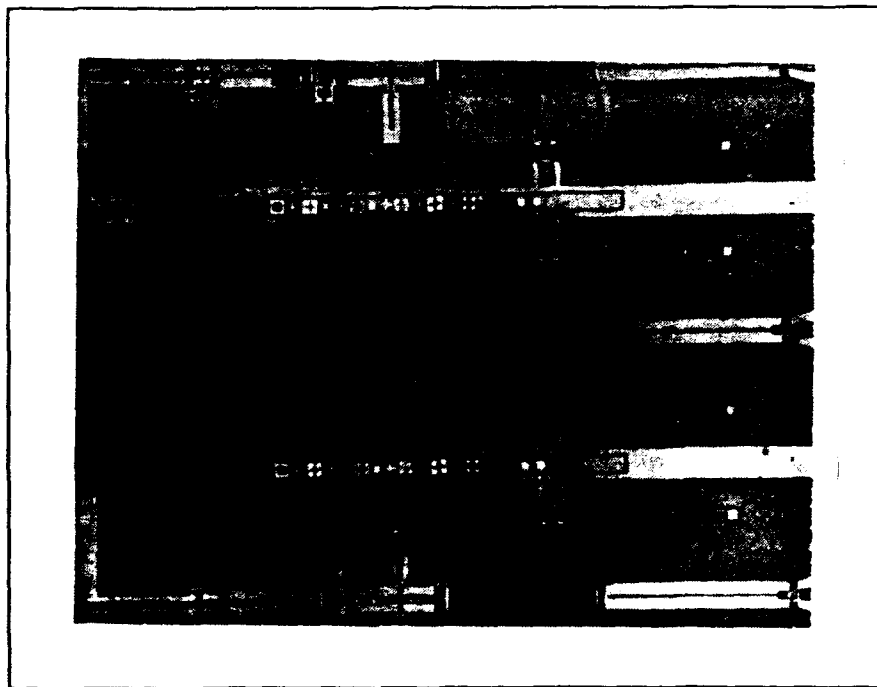


Figure 8.20 31/94 GHz tripler (94-X3-20-50-425) as it appears prior to dicing.

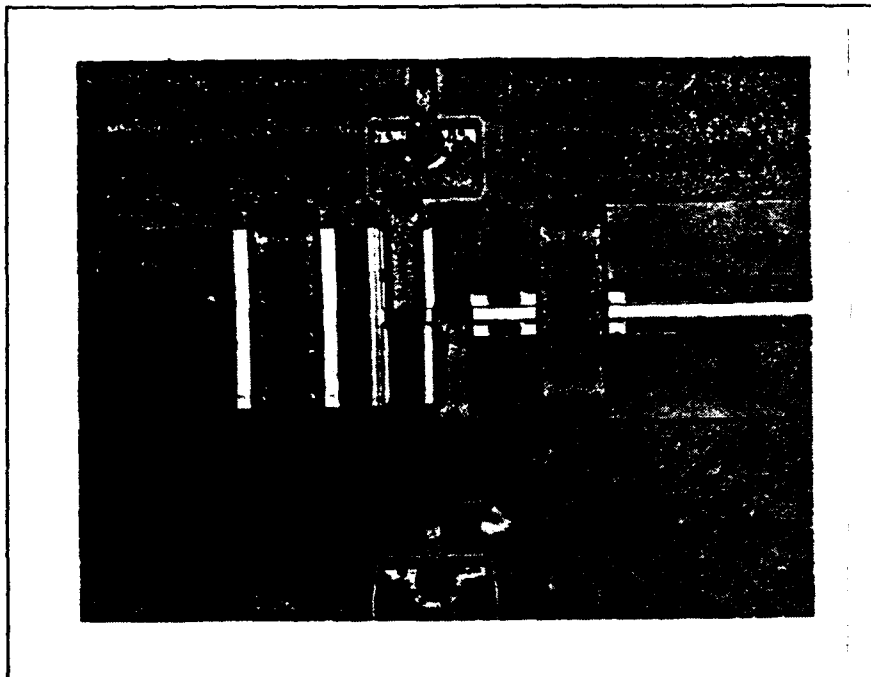


Figure 8.21 Close up of varactor region of the (94-X3-20-50-425) chip.

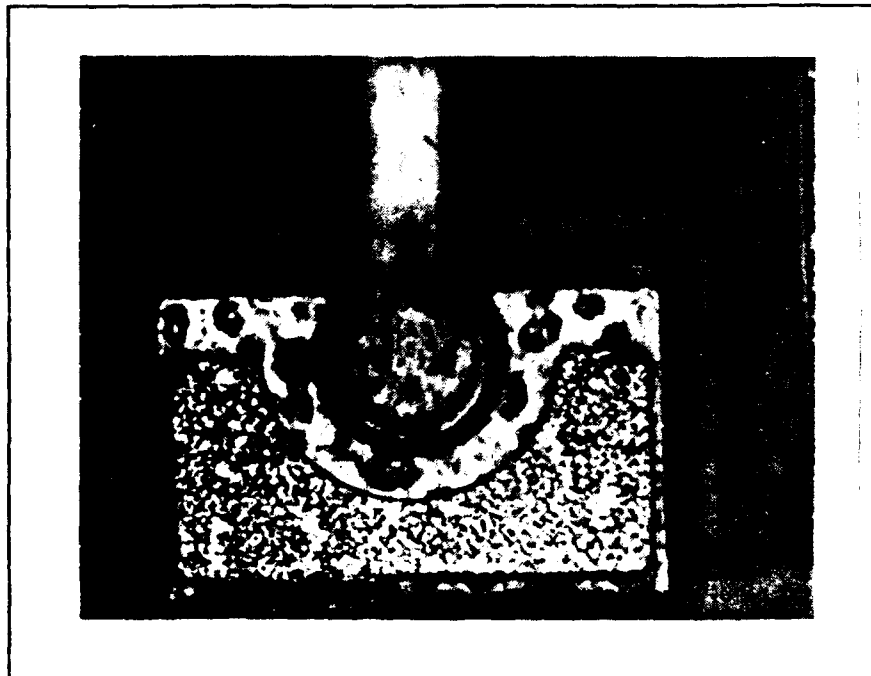


Figure 8.22 Close up of anode and ohmic contact of the (94-X3-20-50-425) chip.

8.5.2 DC Characteristics

Forward Characteristics:

The forward I-V characteristics for a typical varactor measured on the tripler chip are as follows:

<u>Current</u>	<u>Voltage</u>
10 μ A	0.495 v
100 μ A	0.560 v
9 mA	0.718 v
10 mA	0.724 v

which results in the expected R_s of 3 to 4 ohms and a ΔV of 65 mV. Forward biased dc measurements were made using an HP 4145B Semiconductor Parameter Analyzer and a Cascade Microtech wafer prober. The varactor forward biased characteristics of the individual chips chosen for RF measurements, were confirmed using a current source and a four-wire probe.

Reverse Characteristics:

The typical reverse breakdown measured on the varactors was highly irregular, varying from under -5 volts to over -20 volts. The breakdown voltage was only stable after an initial "burn-in" (similar to the "creep" phenomenon observed on some rejected mixer diodes at UVA). This sporadic behavior appears to be linked to the overplating near the anodes, however a direct cause/effect is unclear. Only chips with V_{br} over -20 volts were RF tested. The reverse saturation current, measured using an HP 4145B Semiconductor Parameter Analyzer and point probes, was greater than 1 μ A at -10 volts. This saturation current is larger than expected and is possibly related to surface states on the S.I. GaAs since it is present even if the air bridges to the varactors are removed.

The typical capacitance-voltage characteristics as measured on the CoDiodes at 1 MHz using the HP 4285A LCR meter are presented in Fig. 8.23.

For calibration, on-wafer CoDiodes having open anodes, open air bridges, and shorted anodes were measured. The measured values compare well with the parallel-plate varactor model (see Section 2.3) however the anodes seem slightly undersized (19.2 μm diameter gave best fit to measured data).

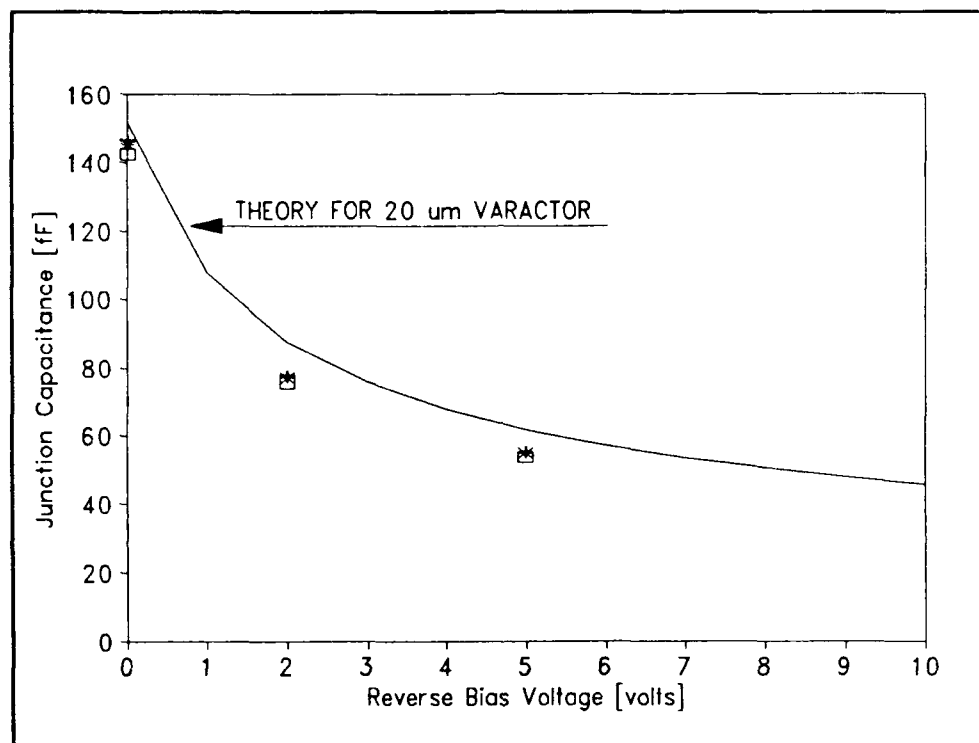


Figure 8.23 Capacitance versus reverse bias for 20 μm diameter CoDiodes on the 31/94 GHz tripler wafer. Theoretical values are included for comparison.

A careful analysis of capacitance data on 20 μm CoDiodes (measured at 1.6 GHz using the HP 8510B network analyzer and the wafer probe) was performed by A. Eskandarian (Eskandarian, 1991) at Martin Marietta Laboratories. His analysis suggests that a more correct value for V_{b1} is 0.74 volts and that the fabricated varactors were slightly oversized (21 μm diameter). A fringing component of approximately 15 fF was also found.

Small Signal Input Return Loss:

The diagram illustrates a microwave test setup for a tripler under test. The signal path is as follows:

- HP8340A SYNTH. ~15 GHz**: The signal source.
- 8 DBM**: Power level at the input of the first amplifier.
- HP8349B AMP.**: First amplifier stage.
- +15 DBM**: Power level at the input of the second amplifier.
- X2**: A doubler stage.
- Power Combiner**: A directional coupler or combiner, represented by a zigzag line with an arrow.
- LPF 47 GHZ**: A low-pass filter.
- HUGHES 8001H TWT**: A Traveling Wave Tube (TWT) amplifier.
- ISO.**: An isolator.
- LPF 47 GHZ**: A second low-pass filter.
- Power Combiner**: A second directional coupler or combiner.
- +17 DBM**: Power level at the input of the tripler.
- TRIPLER UNDER TEST**: The device being tested.
- 20**: A measurement point or power level, indicated by a downward arrow.
- HP8757A SCALAR ANALYZER**: A scalar analyzer connected to the measurement point.
- BIAS**: A biasing connection for the tripler.
- A B BIAS**: Labels for the biasing connection.
- HP6253 DUAL DC SUPPLY**: A dual DC supply providing bias for the tripler.

Figure 8.24 Test setup for measuring the input small signal return loss of the 31/94 GHz triplers.

The tuning frequency is low by about 15 percent and its variation with bias voltage is less than expected from the linear model. The small change in tuning resulting from the change in air bridge overlap is well within the measurement error. The change in tuning point resulting from a change in the input line length is more apparent in the 109 micron bridge overlap data.

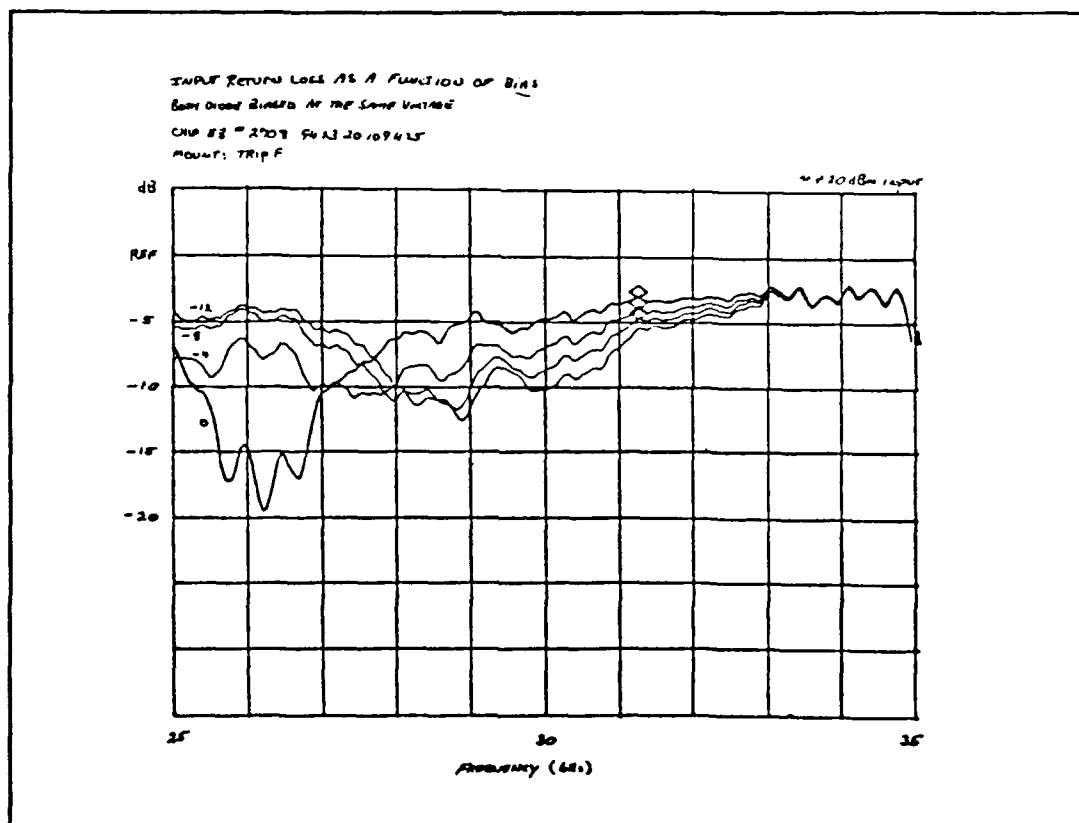


Figure 8.25 Typical plot of small signal input return loss versus frequency. The parameter is the bias voltage.

TABLE 8.9 Input Return Loss Tuning Points versus Reverse Bias									
Bridge Overlap [um]	Input Line [um]	MEASURED [GHz]				THEORY [GHz]			
		0v	-4v	-8v	-12v	0v	-4v	-8v	-12v
< 50	425	26.0	26.8	27.2	27.8	24.9	29.0	30.5	31.3
109	425	26.2	27.4	28.5	28.9	25.2	29.4	30.8	31.6
Percent Change:		+0.8	+2.2	+4.8	+2.3	+1.2	+1.4	+1.0	+1.0
< 50	500	25.6	27.4	27.6	27.8	24.1	28.2	29.5	30.4
109	500	25.8	27.0	27.8	28.0	24.5	28.4	29.8	30.4
Percent Change:		+0.8	-1.4	+0.7	+0.7	+1.7	+0.7	+1.0	0.0
< 50	425	26.0	26.8	27.2	27.8	24.9	29.0	30.5	31.3
< 50	500	25.6	27.4	27.6	27.8	24.1	28.2	29.5	30.4
Percent Change:		-1.5	+2.2	+1.5	0.0	-3.2	-2.8	-3.3	-2.9
109	425	26.2	27.4	28.5	29.8	25.2	29.4	30.8	31.6
109	500	25.8	27.0	27.8	28.0	24.5	28.4	29.8	30.4
Percent Change:		-1.5	-1.5	-2.5	-3.1	-2.8	-3.4	-3.2	-3.8

Small Signal Output Return Loss:

The small signal output return loss was measured for all four varactor versions. The test setup used for this measurement (located at NRAO) is shown schematically in Fig. 8.26.

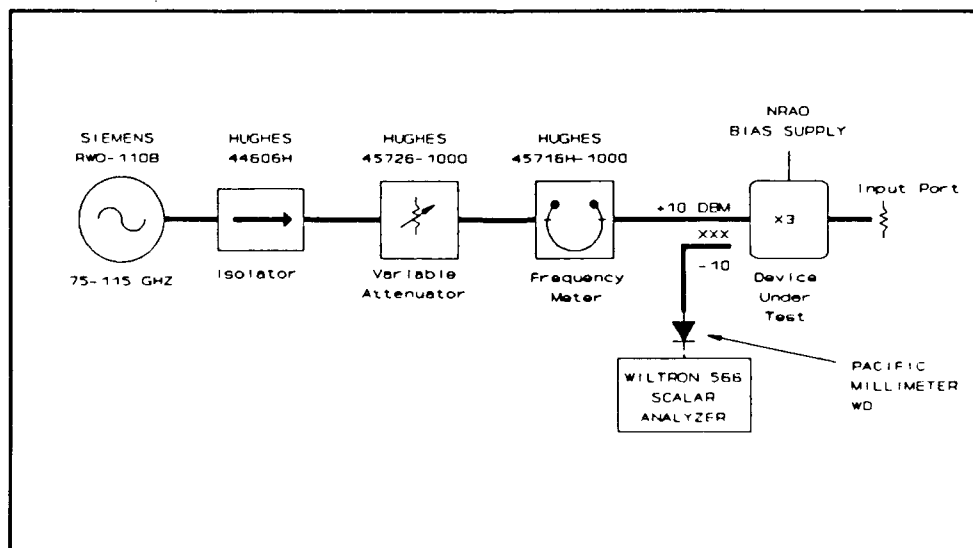


Figure 8.26 Test setup for measuring the output small signal return loss of the 31/94 GHz triplers.

A typical plot of output return loss versus reverse bias is shown in Fig. 8.27. A similar such plot was done for each version. Table 8.10 summarizes the output return loss data. The measured data is compared with calculations based on a the linear equivalent circuit model (analyzed using TouchStone). Table 8.10 also shows the percent change of the tuning frequency resulting from the given increase in either bridge overlap or input line length. The measured tuning variation with reverse bias is again much smaller than predicted using the linear circuit model, however, at bias levels near -8 volts, the tuning points are similar. The change in the input line length had very little effect of the output tuning as expected. The change in tuning point resulting from a change in the air bridge overlap is unclear.

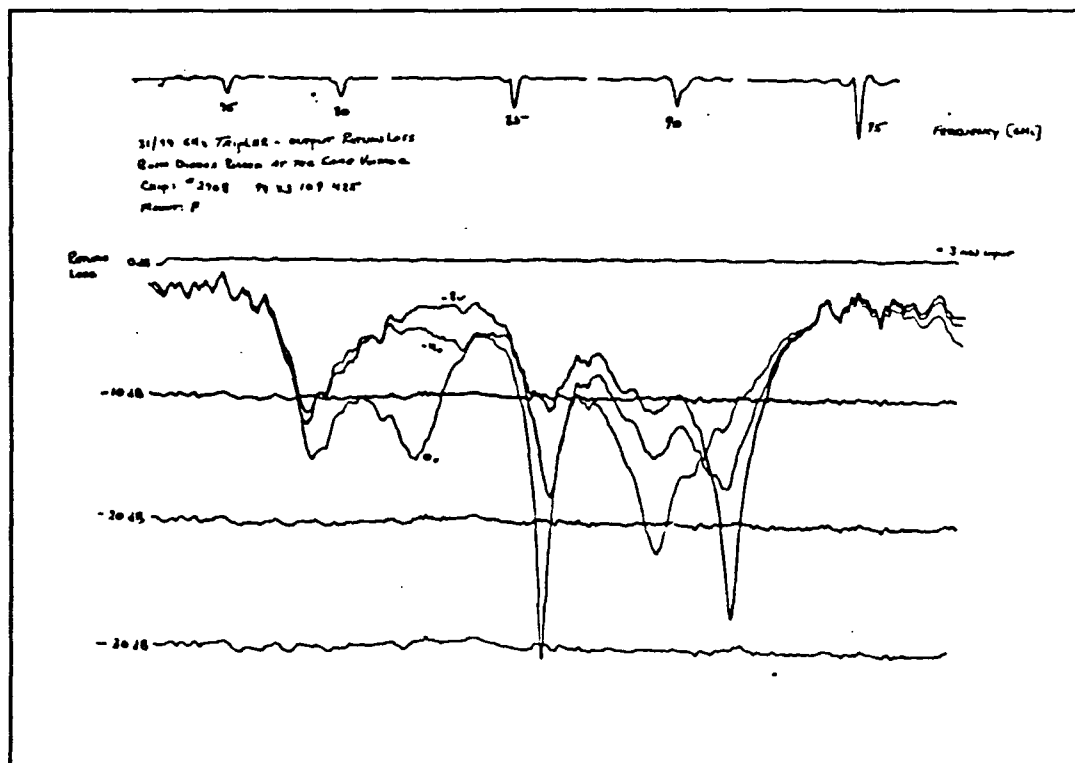


Figure 8.27 Typical plot of small signal output return loss versus frequency. The parameter is the bias voltage.

TABLE 8.10 Output Return Loss Tuning Points versus Reverse Bias							
Bridge Overlap [um]	Input Line [um]	MEASURED [GHz]			THEORY [GHz]		
		0v	-4v	-8v	0v	-4v	-8v
< 50	425	82	89	91	71	80	93
109	425	85	89	92	70	79	91
Percent Change:		+3.7	+0.0	+1.1	-1.4	+1.3	-2.2
< 50	500	83	89	91	71	80	93
109	500	85	89	91	70	79	91
Percent Change:		+2.4	0.0	0.0	-1.4	-1.3	-2.2
< 50	425	82	89	91	71	80	93
< 50	500	83	89	91	71	80	93
Percent Change:		+1.2	0.0	0.0	0.0	0.0	0.0
109	425	85	89	92	70	79	91
109	500	85	90	91	70	79	91
Percent Change:		0.0	0.0	-1.1	0.0	0.0	0.0

8.5.4 Output Power and Efficiency versus Frequency

The output power was measured using the test setup shown in Fig. 8.28.

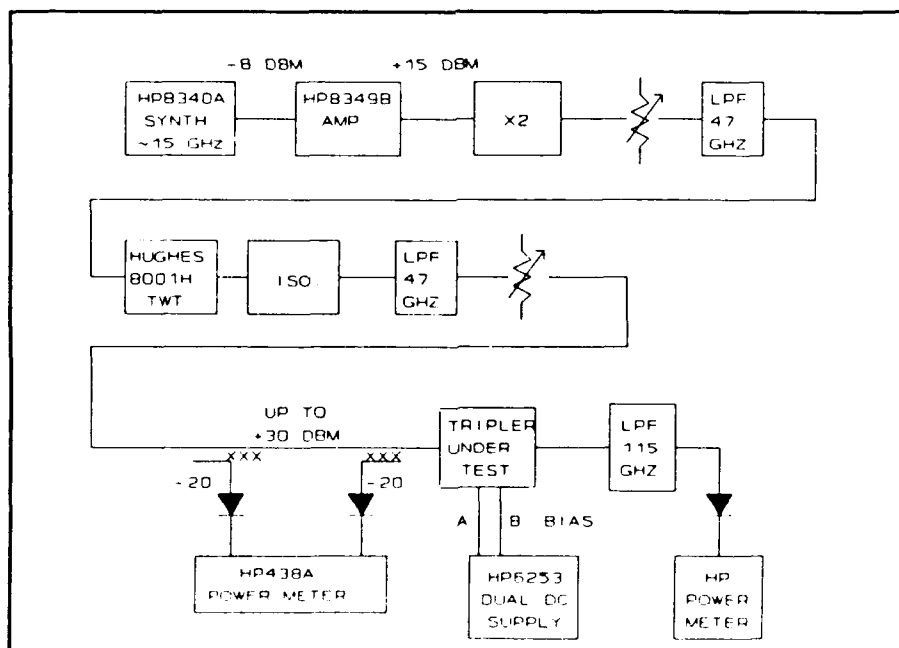


Figure 8.28 Test setup used to measure output power of the 31/94 GHz triplers.

The measured output power versus frequency for all four versions of this tripler design is shown in Fig. 8.29. The data is for 200 mW pump power and has been corrected for loss through the microstrip input line, and losses in the output waveguide and filter connecting the carrier block to the power meter. At each frequency, the bias voltages were adjusted for peak output power. These voltages were quite similar and tended to increase with frequency from 0v @ 25 GHz to -5v @ 32 GHz. The dc bias current was largest at low frequencies and decreased to zero at the higher frequencies. The corresponding efficiencies are shown in Fig. 8.30. The pumped (large signal) input return loss was also measured as a function of frequency and is shown in Fig. 8.31.

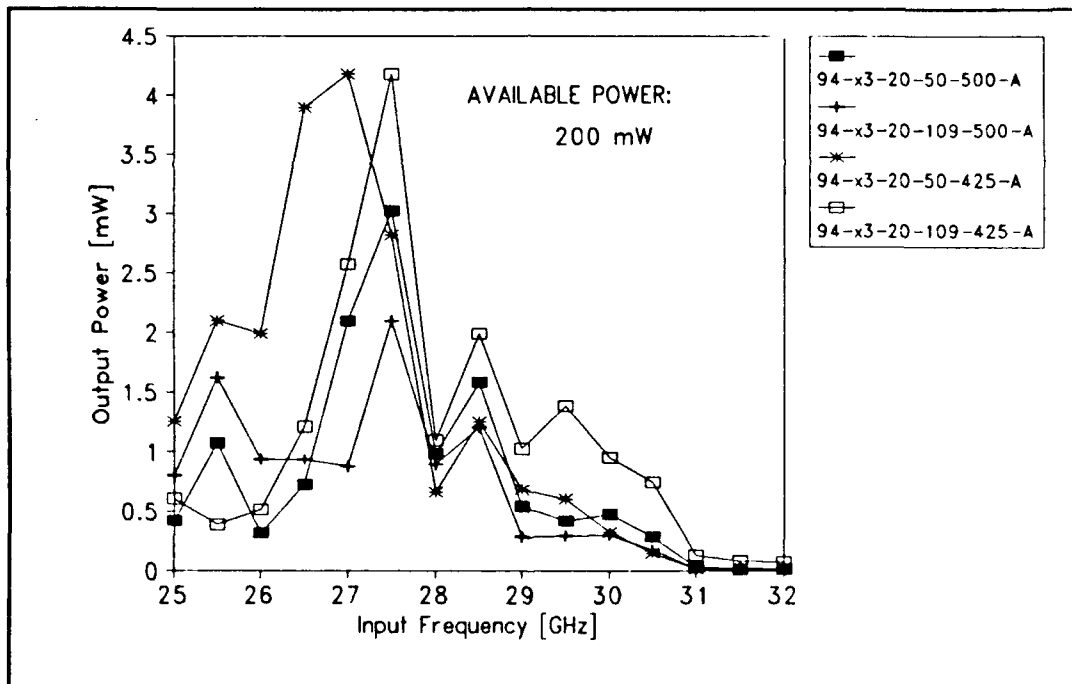


Figure 8.29 The output power versus frequency for the four versions of the 31/94 GHz tripler. (iteration one). Input power: 200 mW.

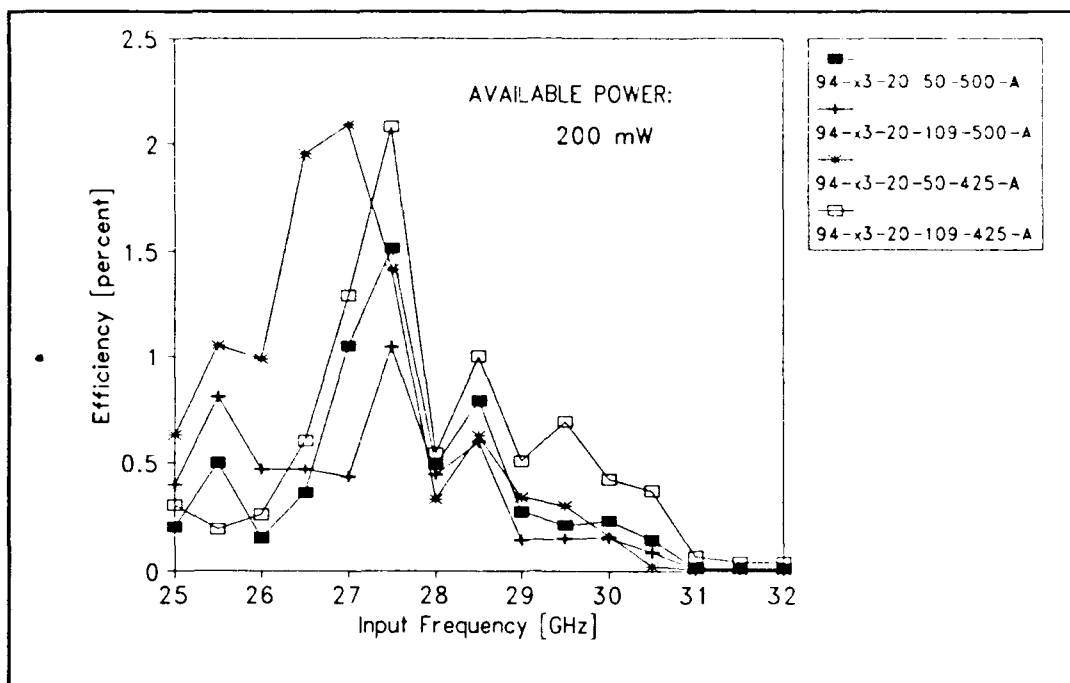


Figure 8.30 Multiplier efficiency versus frequency for four versions of the 31/94 GHz tripler (iteration one). Input power: 200 mW.

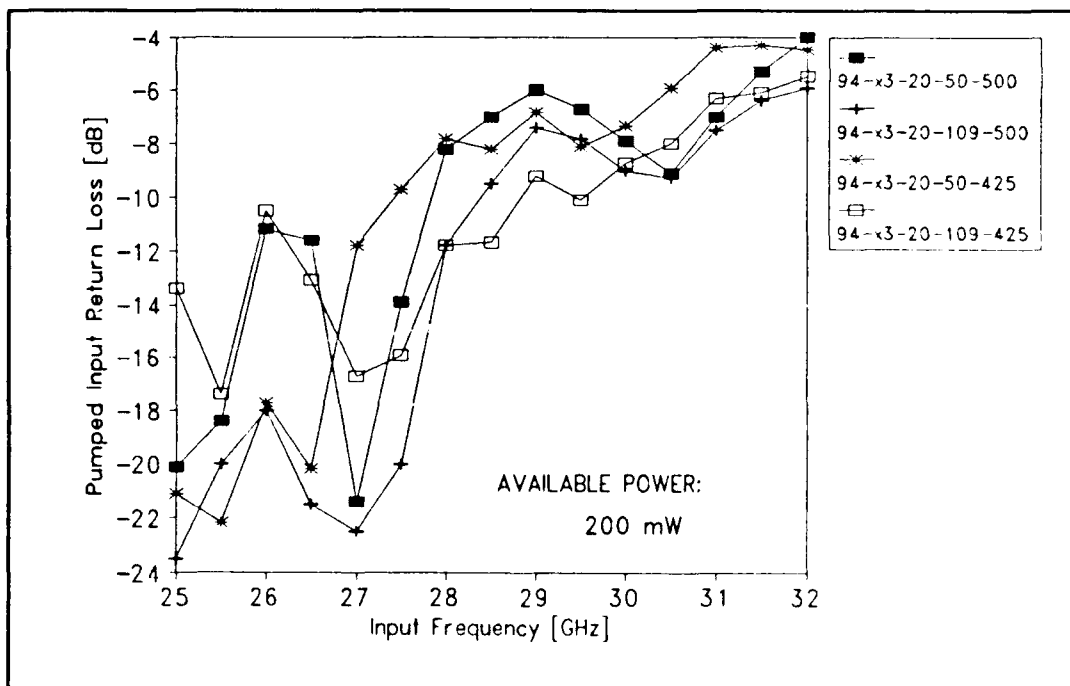


Figure 8.31 Large signal input return loss as a function of frequency. (iteration one)

8.5.5 Output Power and Efficiency versus Input Power

The measurements in Section 8.5.4 were used to find the frequency for maximum output power. At this frequency, the output power and efficiency were measured as functions of available input power. Fig. 8.32 shows the output power versus input power and Fig. 8.33 shows the multiplier efficiency versus input power.

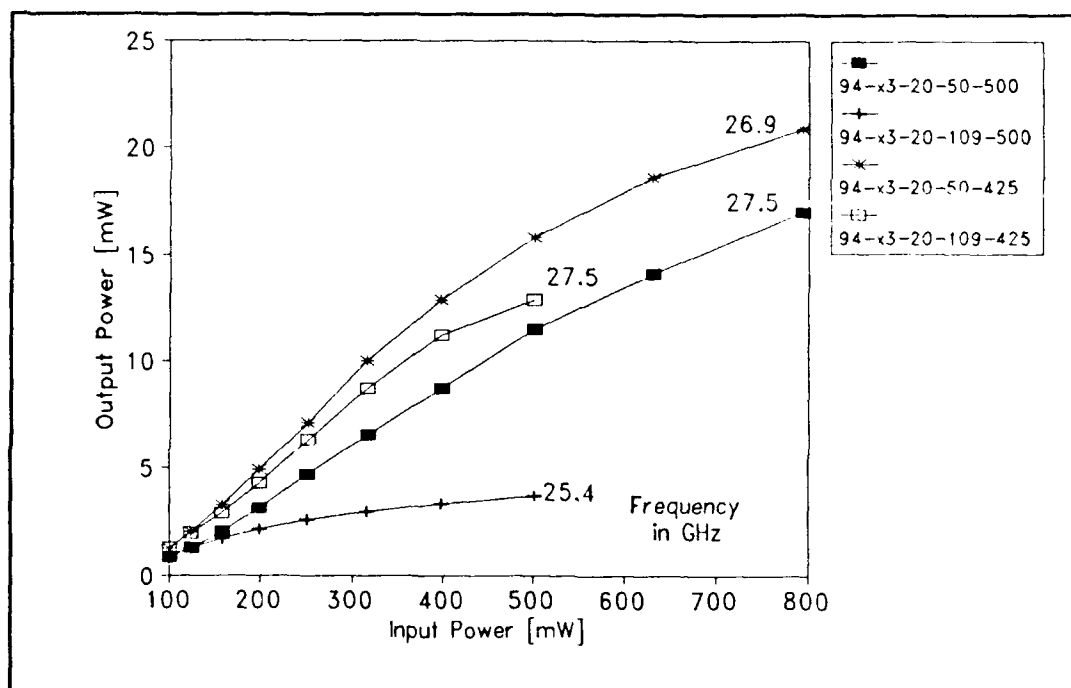


Figure 8.32 Output power versus available input power for the four versions of the 31/94 GHz tripler (iteration one).

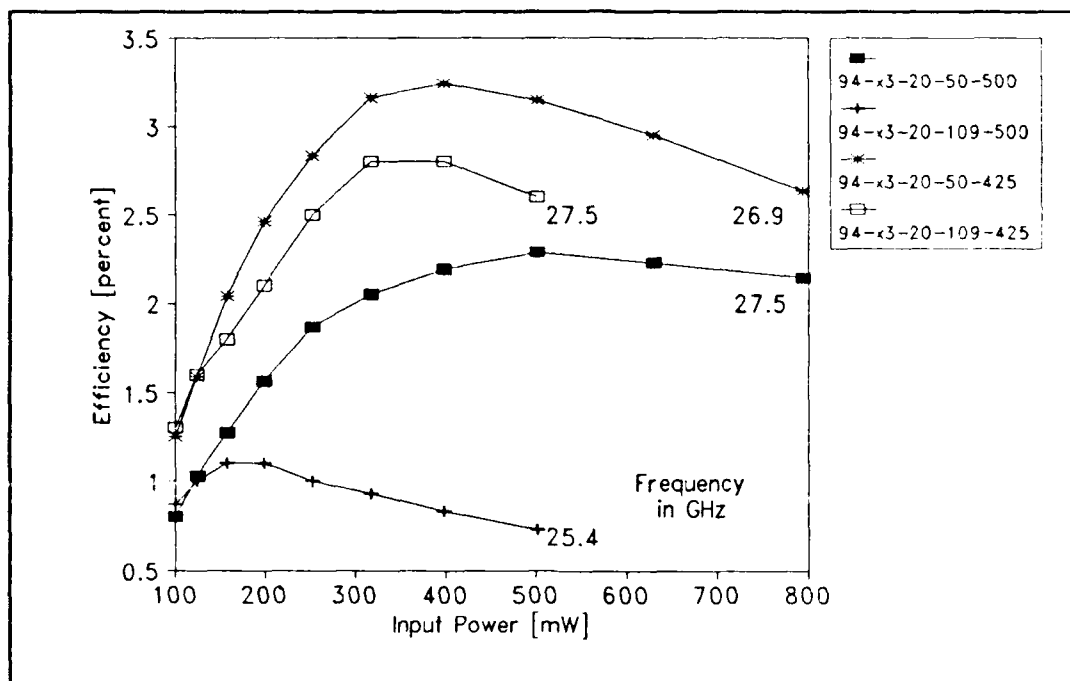


Figure 8.33 Multiplier efficiency versus available input power for the four versions of the 31/94 GHz tripler (iteration one).

8.5.6 Summary of RF Results

The best measured performance of the 31/94 GHz monolithic tripler (iteration one) is shown in Table 8.11.

CHIP/MOUNT	TYPE	FREQ FOR MAX. POWER	MAX. POWER (EFFICIENCY)	MAX. EFFIC (POWER)	INPUT RETURN LOSS
1106/G	50 425	80.7 GHz	20.9 mW (2.6 %)	3.2 % (12.9 mW)	-12.7 dB
2706/F	109 425	82.5 GHz	12.9 mW (2.6 %)	2.8 % (11.2 mW)	-15.8 dB
2107/C	50 500	82.5 GHz	17.0 mW (2.1 %)	2.3 % (11.5 mW)	-13.9 dB
1902/B	109 500	83.0 GHz	3.6 mW (0.7 %)	1.1 % (2.1 mW)	-26.7 dB

8.6 Discussion

Overall, there are three major discrepancies between the measured data and the predicted performance shown in Table 8.7: 1) The measured frequency of highest output power is about 15 percent below the design frequency, 2) the output power and efficiency are much lower than predicted, and 3) the data from the small signal return loss measurements indicate that the change in tuning point with bias is smaller than expected. Best performance occurs between 79.5 and 82.5 GHz with varactor bias near 0 volts. The output power curve appears to follow the input large-signal return loss curve thus suggesting that the input mistuning is the dominating factor contributing to the low performance.

Using the linear embedding circuit model and Touchstone, the tuning was studied as a function of changes in the physical dimensions of critical components of the embedding circuits. The results are presented in Table 8.12.

TABLE 8.12 Tuning Sensitivity Analysis	
Embedding circuit component:	Change in tuning for a 10 % change in component value:
INPUT TUNING:	
Length of open circuit stub:	< 1 percent
Position of open circuit stub:	< 5 percent
Length of shorting stub:	< 1 percent
Position of shorting stub:	< 1 percent
Series capacitance (w/ stub):	< 5 percent
OUTPUT TUNING:	
Length of open circuit stub:	< 1 percent
Position of open circuit stub:	< 1 percent
Length of shorting stub:	10 percent
Position of shorting stub:	< 5 percent
Series capacitance (w/ stub):	< 5 percent

Note that only the length of the shorting stub in the output circuit is moderately effective in adjusting output frequency of the tripler. However, for iteration one, the small-signal output return loss data suggests that output tuning is close to the design frequency. The proper length of the input tuning line was also verified. This suggests that the improper tuning may be caused by circuit elements not included in the original linear embedding impedance model.

The effect of idler tuning on output power and efficiency was studied using the Siegel-Kerr nonlinear analysis program. With the design-value of the embedding impedances taken as the references, the output power and varactor efficiency were examined for a wide range of idler impedances (including open and short). Although the input impedance is a very strong function of the idler tuning, the results, presented in

Table 8.13, indicate that the idler circuit is relatively low Q and hence the output power and efficiency are not very sensitive to the idler tuning over a range of 20 percent with reference to the design frequency.

TABLE 8.13 Idler Study 31/94 GHz Tripler					
Reference values: Maximum efficiency point as predicted by both Siegel-Kerr program and Penfield-Rafuse approach.					
Input embedding impedance: 30 +j 114			Bias voltage: -15 v		
Output embedding impedance: 15 +j 38			Available power: 200 mW		
IDLER IMPEDANCE [ohms]	ABSORBED POWER [mW]	OUTPUT POWER [mW]	Re[Zin] [ohms]	Im[Zin] [ohms]	VARACTOR EFFICIENCY [percent]
+j 85.5 (+50%)	153.5 (-23.0%)	80.9 (-26.0%)	14.5 (-50.0%)	-j 131 (-11.0%)	52.8 (-3.8%)
+j 74.1 (+30%)	168.0 (-15.8%)	92.3 (-15.8%)	20.3 (-30.2%)	-j 133 (-12.7%)	54.9 (0.0%)
+j 68.4 (+20%)	178.2 (-10.7%)	98.0 (-10.6%)	25.3 (-13.1%)	-j 133 (-12.7%)	55.0 (+0.2%)
+j 62.7 (+10%)	190.9 (-4.3%)	104.9 (-4.3%)	30.4 (+4.47%)	-j 127 (-7.6%)	54.9 (+0.0%)
+j 57.0 (REF)	199.5 (REF)	109.6 (REF)	29.1 (REF)	-j 118 (REF)	54.9 (REF)
+j 51.3 (-10%)	195.0 (-2.3%)	109.3 (-0.3%)	23.7 (-18.6%)	-j 111 (+5.9%)	56.1 (+2.2%)
+j 45.5 (-20%)	188.3 (-5.6%)	100.5 (-8.3%)	19.6 (-32.6%)	-j 108 (+8.5%)	53.4 (-2.7%)
+j 39.9 (-30%)	177.4 (-11.0%)	92.6 (-15.5%)	16.3 (-44.0%)	-j 106 (+10.2%)	52.2 (-4.9%)
+j 28.5 (-50%)	156.2 (-21.7%)	70.6 (-35.6%)	12.1 (-58.4%)	-j 105 (+11.0%)	45.2 (-97.7%)
open	80.5 (-59.6%)	0.250 (-99.8%)	4.0 (-86.3%)	-j 108 (+8.5%)	0.3 (-99.4%)
short	116.9 (-41.4%)	37.8 (-67.2%)	7.3 (-74.9%)	-j 104 (+11.9%)	32.3 (-41.2%)

The possibility of a relatively large shunt capacitance was also examined. If this shunt capacitance is across the anode to ground, its effect is devastating since it shunts the input, output, and idler

impedances simultaneously, thus resulting in non-optimum embedding impedances presented at the varactor and an overall decrease in the operating frequency. The tuning point for various shunt capacitances ranging from 0 to 50 fF is shown in Figs. 8.34 (input) and 8.35 (output).

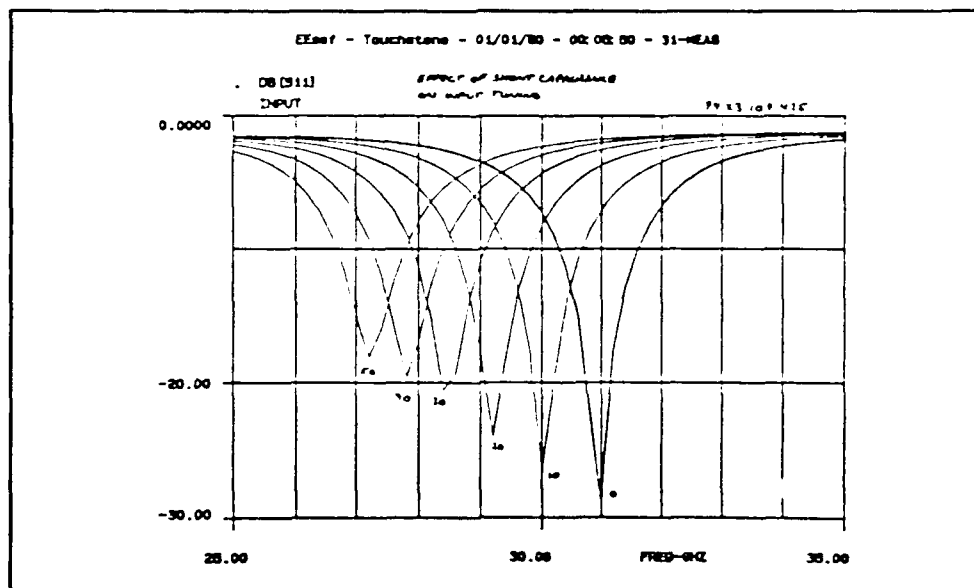


Figure 8.34 The effect of shunt capacitance on the input tuning of the 31/94 GHz tripler.

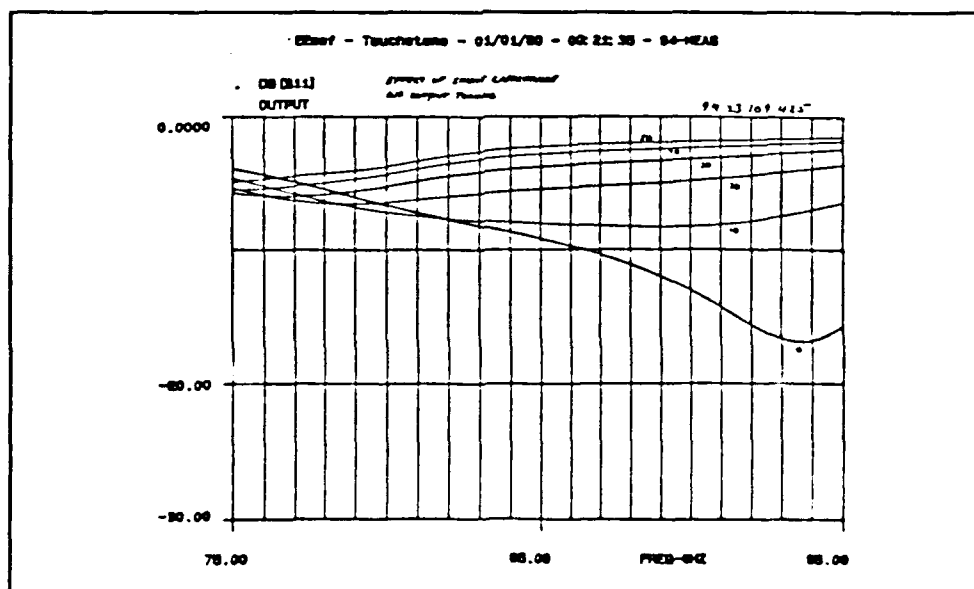


Figure 8.35 The effect of shunt capacitance on output tuning of the 31/94 GHz tripler.

The magnitude and nature of a shunt capacitance in the 31/94 GHz tripler circuit is unclear. Initially, over plating of the anodes was suspected, however scanning electron micrographs of the anode region reveal a well defined geometry without any perturbations which could lead to a significant shunt capacitance (see Fig. 8.36).

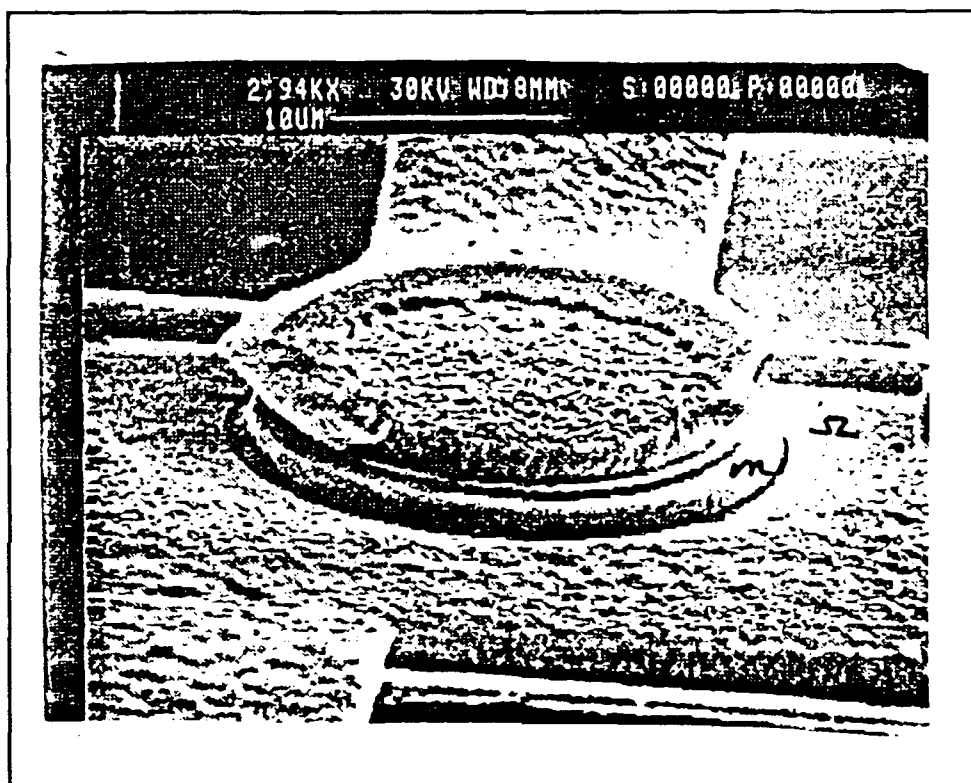


Figure 8.36 SEM micrograph of the anode region of the 31/94 GHz tripler. n- GaAs (n) and ohmic contact (Ω) region noted.

Another possibility is that some shunt capacitance results from distributed effects of the relatively long path between the varactors and the main CPW and additional capacitance may simply result from lumped capacitance between the anode/ohmic contact and the ground plane. More compact circuitry around the varactors is needed to minimize the distributed capacitance. An improved varactor geometry is shown in Fig. 8.37.

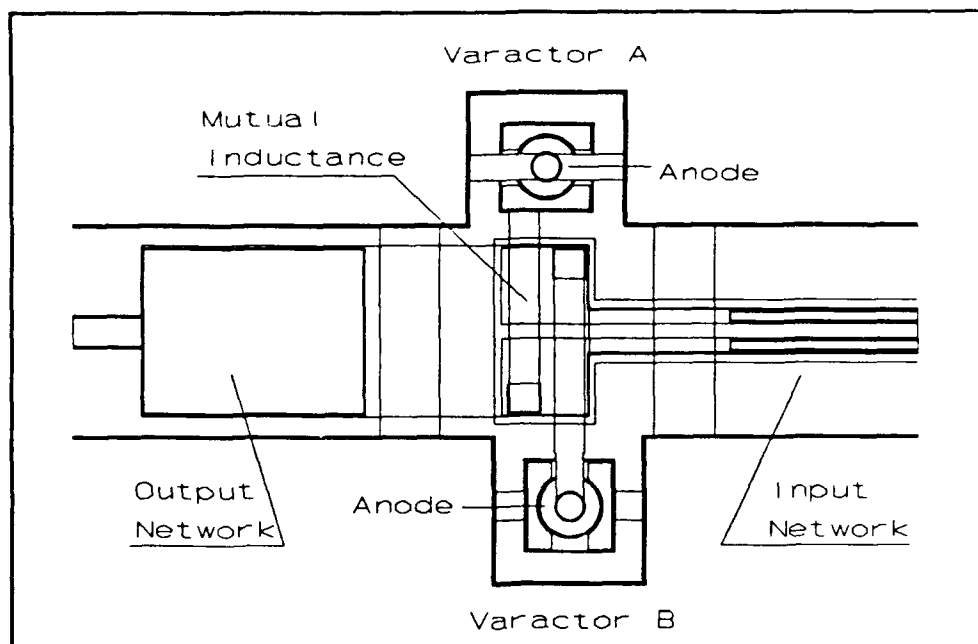


Figure 8.37 The improved geometry for the varactors in the 31/94 GHz tripler - cf. Fig. 8.7.

Although the discontinuity of the main CPW line has been minimized by this approach, a lumped component of the shunt capacitance will still be present. Since a direct measurement of the shunt capacitance in situ is difficult, a very large (310x) scale model of the ohmic contact, anode, and ground plane was constructed using Stycast ($\epsilon_r=12$) and copper tape. A sketch of the scale model (including the geometrical improvements) is shown in Fig. 8.38. The capacitance was measured using an HP 4332A LCR meter. Between the anode and ground the capacitance was 1.2 pF (4 fF scaled) and between the ohmic contact and ground was 4.6 pF (15 fF scaled). Since the varactors are in anti-parallel, one will have a 4 fF shunt and the other will have 15 fF shunt. This imbalance in shunt capacitance presents a complex tuning imbalance with unclear consequences. For the second iteration, the tripler was designed with 15 fF shunt capacitance across both diodes.

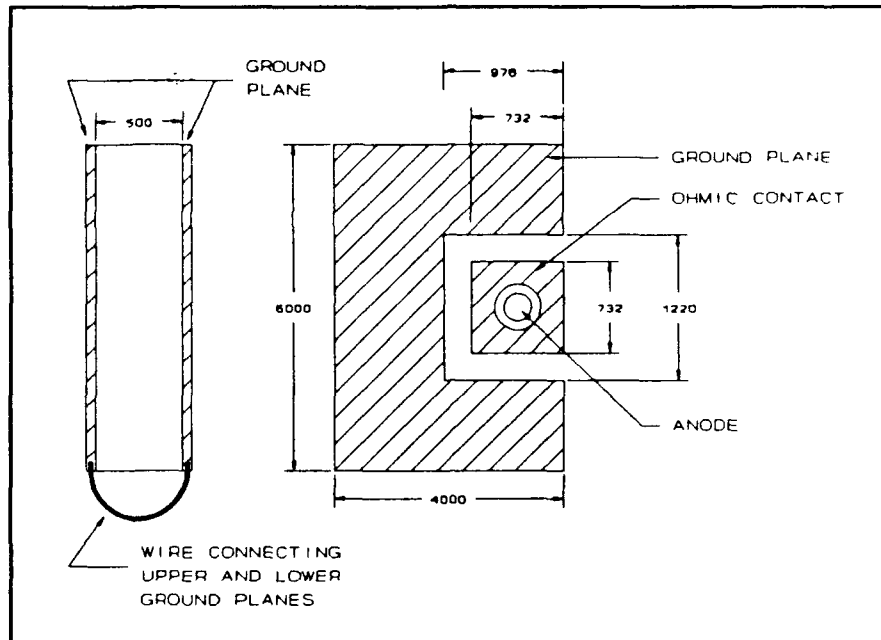


Figure 8.38 Sketch of the 310x scale model of the varactor region of the 31/94 GHz tripler. (Not to scale).

8.7 31/94 GHz Tripler Design (Second Iteration)

The 31/94 GHz tripler was redesigned using Touchstone to obtain embedding impedances for varactors with 15 fF shunt capacitance. For best performance, the length of the input CPW (used to resonate the capacitive reactance of the average junction capacitance) was shortened to 275 microns. This change gives the embedding impedances shown in Table 8.14.

TABLE 8.14 Embedding Impedances versus Frequency Second Iteration			
Pump Frequency	Embedding Impedances [ohms]		
	INPUT	IDLER	OUTPUT
29 GHz	23.1 +j 66	0 +j 63	25.4 +j 41
31 GHz	38.3 +j 92	0 +j 74	28.7 +j 54
33 GHz	77.6 +j129	0 +j 94	32.6 +j 72

The nonlinear analysis program of Siegel and Kerr was used together with the embedding impedances of Table 8.14 to calculate the performance of the tripler as a function of frequency. Conductive losses in the embedding circuits are also included. The best performance at each frequency is presented in Table 8.15.

TABLE 8.15 Predicted Tripler Performance versus Frequency BALANCED VARACTOR CIRCUIT Siegel and Kerr Program					
Pump Frequency [GHz]	Bias Voltage [volts]	Available Power [mW]	Output Power [mW]	Input Impedance [ohms]	Varactor Efficiency [percent]
29	- 5	500	43.6	9.9 -j 58	20.1
31	-10	500	54.6	10.6 -j115	37.3
33	-15	500	22.6	7.7 -j136	26.0

Five versions of the 31/94 GHz monolithic frequency tripler were fabricated at Martin Marietta Laboratories as described in Section 5.7 of this thesis. The variations, which are outlined in Table 8.16, yield modification of the idler and output tuning and the varactor diameter.

TABLE 8.16 31/94 GHz Tripler Variations Second Iteration			
CHIP NUMBER	ANODE DIA.	INPUT TUNING	MUTUAL IND. OVERLAP
94 X3 17 50 275 A	17 μ m	275 μ m	50 μ m
94 X3 17 109 275 A	17 μ m	275 μ m	109 μ m
94 X3 20 50 275 A	20 μ m	275 μ m	50 μ m
94 X3 20 109 275 A	20 μ m	275 μ m	109 μ m
94 X3 20 109 425 B	20 μ m	475 μ m	109 μ m

The 94 X3 20 109 425 B is of the same overall design as in the first iteration, however the more compact varactor arrangement was used. Fabrication was completed on October 12, 1991.

8.8 Results - Second Iteration

This tripler was also evaluated on the basis of 1) a visual inspection, 2) the dc characteristics, 3) the small signal return loss at input and output, 4) the output power and efficiency versus frequency, and 5) the output power and efficiency versus input power. All dc measurements were made on wafer or on an individual chip mounted on a glass microscope slide. For RF measurements, the carrier block designed by E. Schlecht was used. A sketch of the carrier block is shown in Fig. 8.19.

8.8.1 Visual Inspection

Fig. 8.39 is a photograph of the 31/94 GHz monolithic frequency tripler top side processing as it appears in the carrier block. The input line is just off the right side of the photograph. Fig 8.40 is a closeup view of the varactor region showing the mutually coupled air bridges and the two wide air bridges connecting the ground planes. Fig. 8.41 is a closeup of the varactor region. The lithography appears to be well defined, however there are traces of photoresist on the chips (gray regions in photographs). There is no indication of overplating.

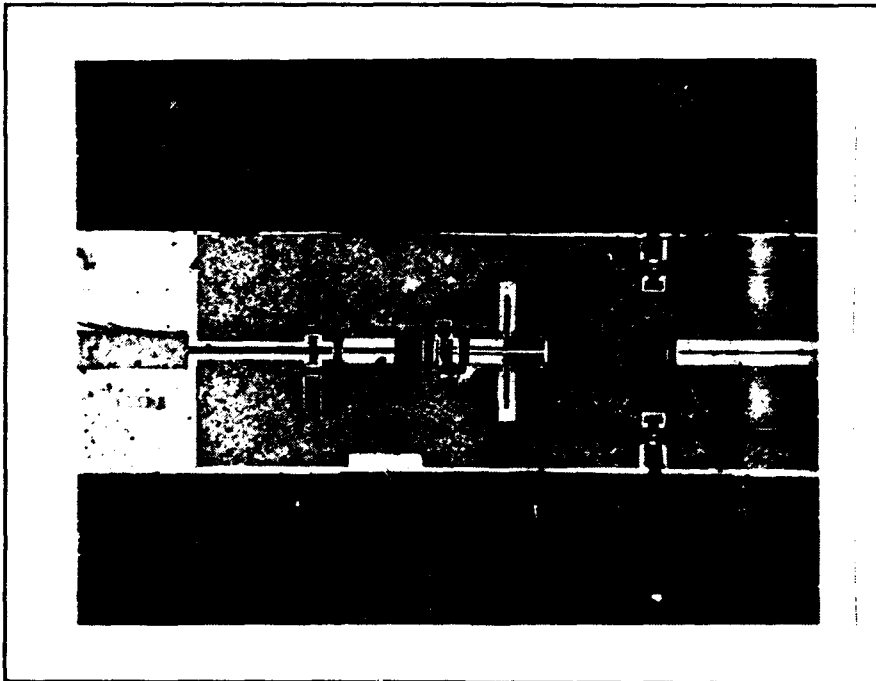


Figure 8.39 31/94 GHz tripler (94-X3-17-109-275-A) as it appears in carrier block "K".

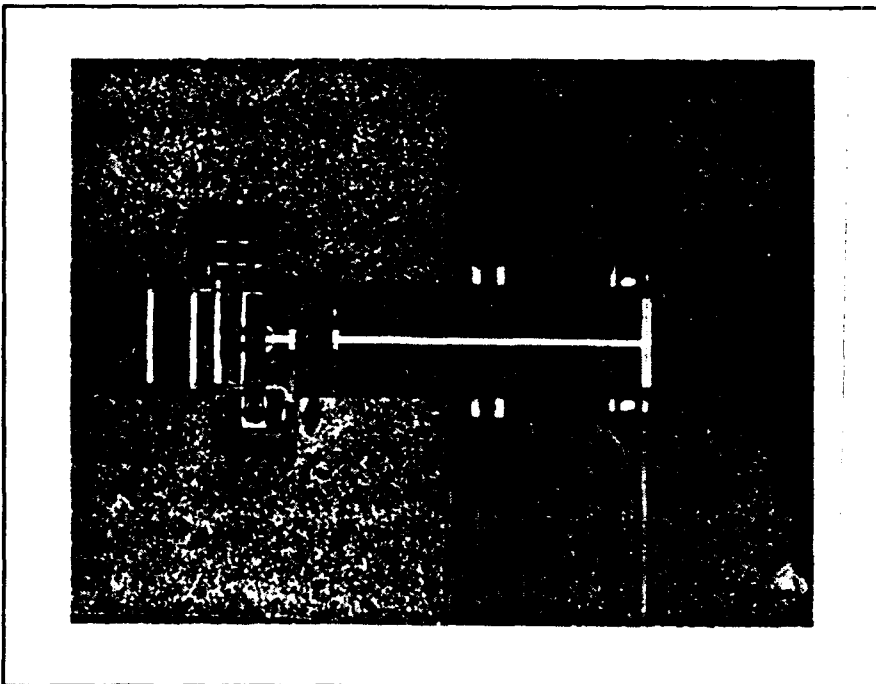


Figure 8.40 Close up of the varactor region of the (94-X3-17-109-175-A) chip.

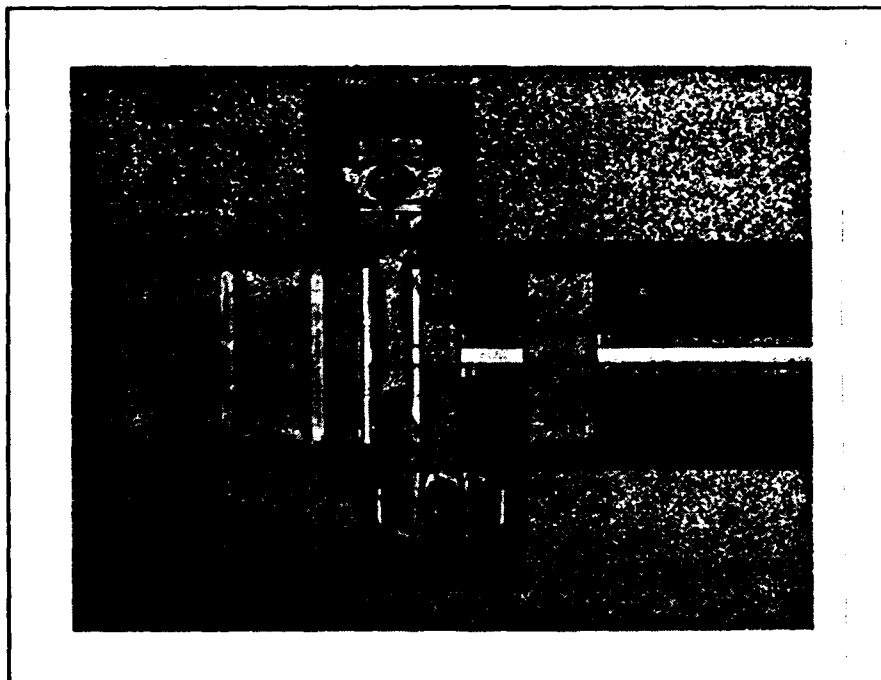


Figure 8.41 Close up of the mutually-coupled air bridges on the (94-X3-17-109-275-A) chip.

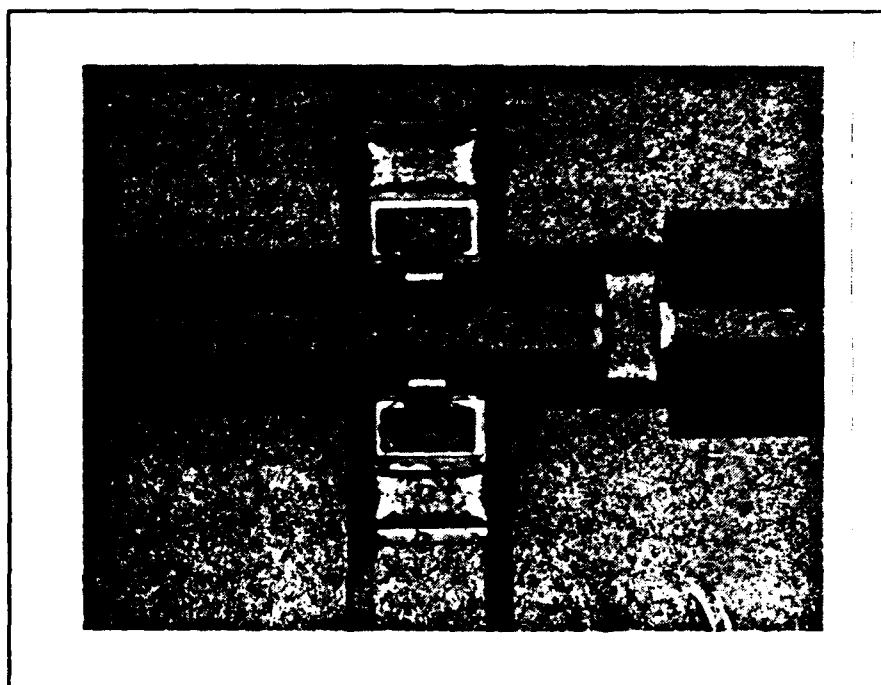


Figure 8.42 Close up of the output tuning stubs on the (94-X3-17-109-275-A) chip.

8.8.2 DC Characteristics

Forward Characteristics:

The forward I-V characteristics of many varactors were measured on the tripler chip. Typical values are as follows:

<u>Current</u>	<u>Voltage</u>
10 μ A	0.505 v
100 μ A	0.570 v
9 mA	0.732 v
10 mA	0.739 v

These data results in an R_s of 3 to 4 ohms and a ΔV of 65 mV as expected. Forward biased dc measurements were made using an HP 4145B Parameter Analyzer and a Cascade Microtech wafer prober. The varactor forward biased characteristics of chips chosen for RF measurements were confirmed using a current source and a four-wire probe.

Reverse Characteristics:

The typical reverse breakdown voltage measured in situ was typically over -20 volts (10 μ A). A leakage current of less than 1 μ A at -10 volts was measured even when the anode airbridges were removed. This current may be caused by surface states present in the S.I. GaAs (especially since RIE etching was used). No CoDiodes were included on this wafer, hence the capacitance was not measured.

8.8.3 Small Signal Return Loss

Small Signal Input Return Loss:

The small signal input return loss was measured for all five varactor versions. The same test fixture used for this measurement is shown schematically in Fig. 8.24. A typical plot of input return loss versus reverse bias is shown in Fig. 8.43. A similar such plot was done

for each version. Table 8.17 summarizes the input return loss data. The measured data is compared with calculations based on a the linear equivalent circuit model (analyzed using TouchStone). Table 8.17 also shows the percent change of the tuning frequency resulting from the given increase in either bridge overlap or anode diameter. The input tuning (both with frequency and bias variations) is very similar to that predicted by the linear models. The change in tuning with anode diameter is smaller than expected (especially at low bias voltages). The input return loss of the 94-X3-20-109-425-B was very similar to that of version A. This implies that the fringing capacitance is not distributed but is essentially a lumped capacitance associated with the anode and ohmic contact geometry (as the scale model data indicate).

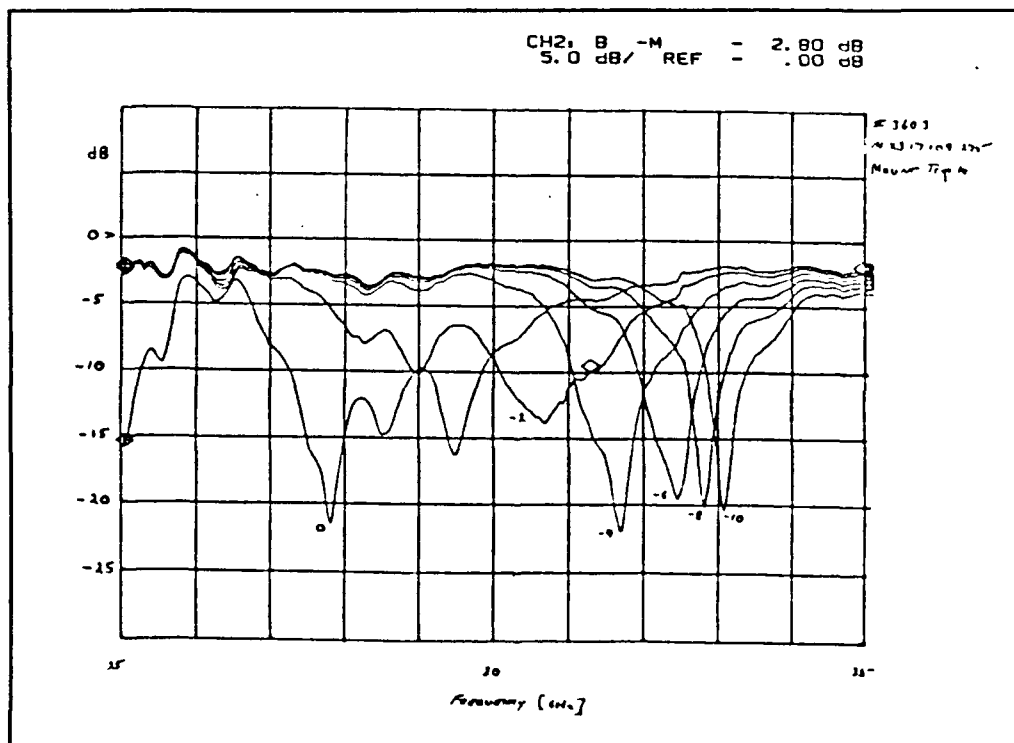


Figure 8.43 Typical plot of measured small-signal input return loss for second iteration of 31/94 GHz tripler with bias voltage as the parameter.

TABLE 8.17 Input Return Loss Tuning Points versus Reverse Bias Input line length: 275 μm									
Bridge Overlap [μm]	Anode Dia. [μm]	MEASURED [GHz]				THEORY [GHz]			
		0v	-2v	-4v	-8v	0v	-2v	-4v	-8v
50	17	28.5	30.7	31.5	32.6	27.5	30.0	31.2	32.2
109	17	28.5	30.6	31.7	32.8	27.4	30.0	31.1	32.2
Percent Change:		0.0	-0.3	+0.6	+0.6	-0.3	0.0	-0.3	0.0
50	20	27.6	29.9	30.8	31.8	26.0	28.5	29.7	31.0
109	20	28.0	29.9	30.6	31.1	25.8	28.5	29.6	30.9
Percent Change:		+1.4	0.0	-0.6	-2.2	-0.7	0.0	-0.3	-0.3
50	17	28.5	30.7	31.5	32.6	27.5	30.0	31.2	32.2
50	20	27.6	29.9	30.8	31.8	26.0	28.5	29.7	31.0
Percent Change:		-3.2	-2.6	-2.2	-2.5	-5.4	-5.0	-4.8	-3.7
109	17	28.5	30.6	31.7	32.8	27.4	30.0	31.1	32.2
109	20	28.0	29.9	30.6	31.1	25.8	28.5	29.6	30.9
Percent Change:		-1.8	-3.2	-3.5	-5.2	-5.8	-5.0	-4.8	-4.0

Small Signal Output Return Loss:

The small signal output return loss was measured for all five varactor versions. The test fixture used for this measurement (located at NRAO) is shown schematically in Fig. 8.26. A typical plot of output return loss versus reverse bias is shown in Fig. 8.44. A similar such plot was done for each version. Table 8.18 summarizes the input return loss data. The measured data is compared with calculations based on a the linear equivalent circuit model (analyzed using TouchStone). Table 8.18 also shows the percent change of the tuning frequency resulting from the given increase in either bridge overlap or anode diameter. The measured change in tuning point as a result of a change in bias voltage or a change in anode diameter is much less than predicted.

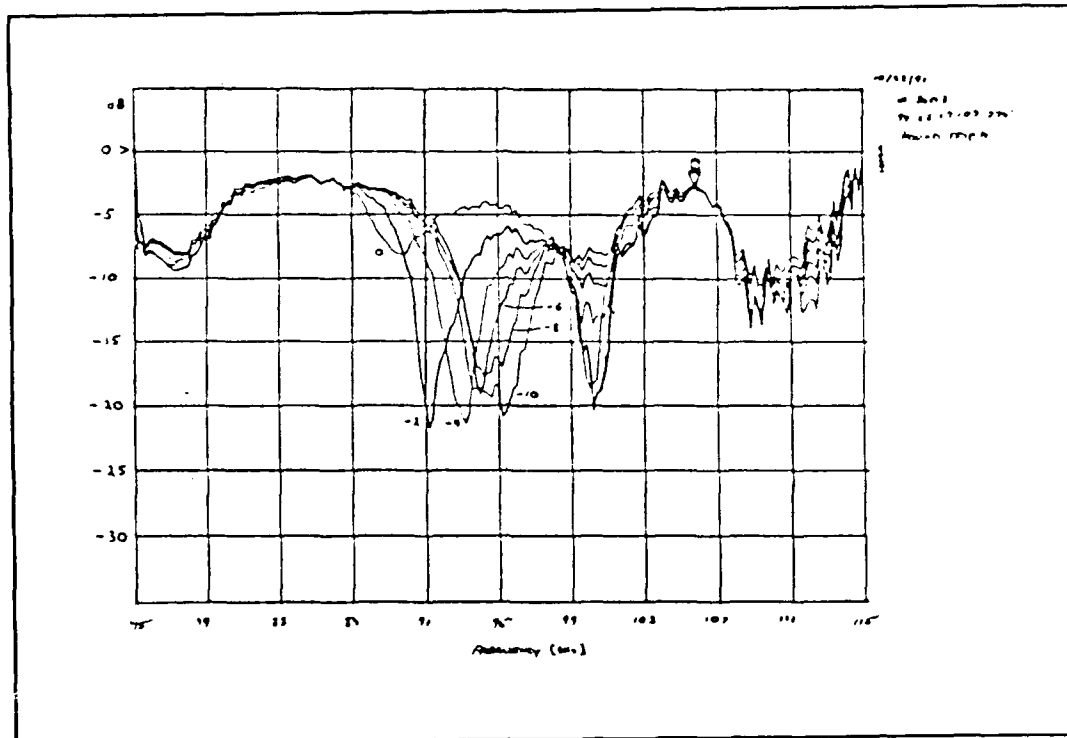


Figure 8.44 Typical small signal output return loss data for the 31/94 GHz tripler with bias voltage as the parameter.

TABLE 8.18 Output Return Loss Tuning Points versus Reverse Bias Input line length: 275 μm									
Bridge Overlap [μm]	Anode Dia. [μm]	MEASURED [GHz]				THEORY [GHz]			
		0v	-2v	-4v	-8v	0v	-2v	-4v	-8v
50	17	90.0	92.5	93.5	93.5	79.0	87.0	90.0	93.5
109	17	89.5	91.5	93.0	94.5	77.0	84.5	88.0	92.0
Percent Change:		-0.5	-1.1	-0.5	+1.0	-2.5	-2.9	-2.2	-1.6
50	20	89.0	90.0	91.0	93.0	74.5	82.0	86.0	89.0
109	20	95.5	95.5	96.0	96.5	73.0	79.0	84.0	88.0
Percent Change:		+7.3	+6.1	+5.5	+3.8	-7.9	-3.6	-2.3	-1.1
50	17	90.0	92.5	93.5	93.5	79.0	87.0	90.0	93.5
50	20	89.0	90.0	91.0	93.0	73.0	79.0	84.0	88.0
Percent Change:		-1.1	-2.7	-2.7	-0.5	-7.9	-9.2	-6.7	-5.9
109	17	89.5	91.5	93.0	94.5	77.0	84.5	88.0	92.0
109	20	95.5	95.5	96.0	96.5	74.5	82.0	86.0	89.0
Percent Change:		+6.7	+4.4	+3.2	+2.1	-3.2	-3.0	-2.3	-3.3

8.8.4 Output Power and Efficiency versus Frequency

The output power was measured using the test fixture shown in Fig. 8.28. The pumped (large signal) input return loss was measured as a function of frequency and is shown in Fig. 8.45. The measured output power versus frequency for all four versions of this tripler design is shown in Fig. 8.46. The data is for 200 mW pump power and has been corrected for loss through the microstrip input line, and losses in the output waveguide and filter connecting the carrier block to the power meter. The bias voltages were adjusted for peak output power at each frequency. As in the first iteration, the bias voltages were very similar and tended to increase with increasing frequency. The corresponding efficiencies are shown in Fig. 8.47.

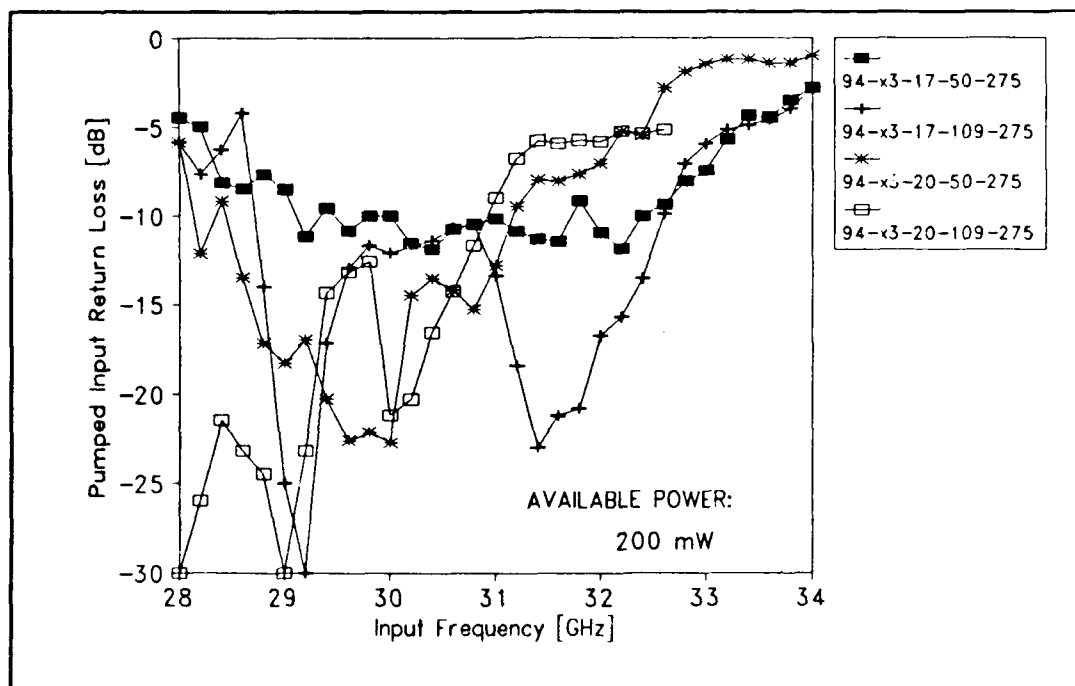


Figure 8.45 Large signal input return loss as a function of frequency. (iteration two)

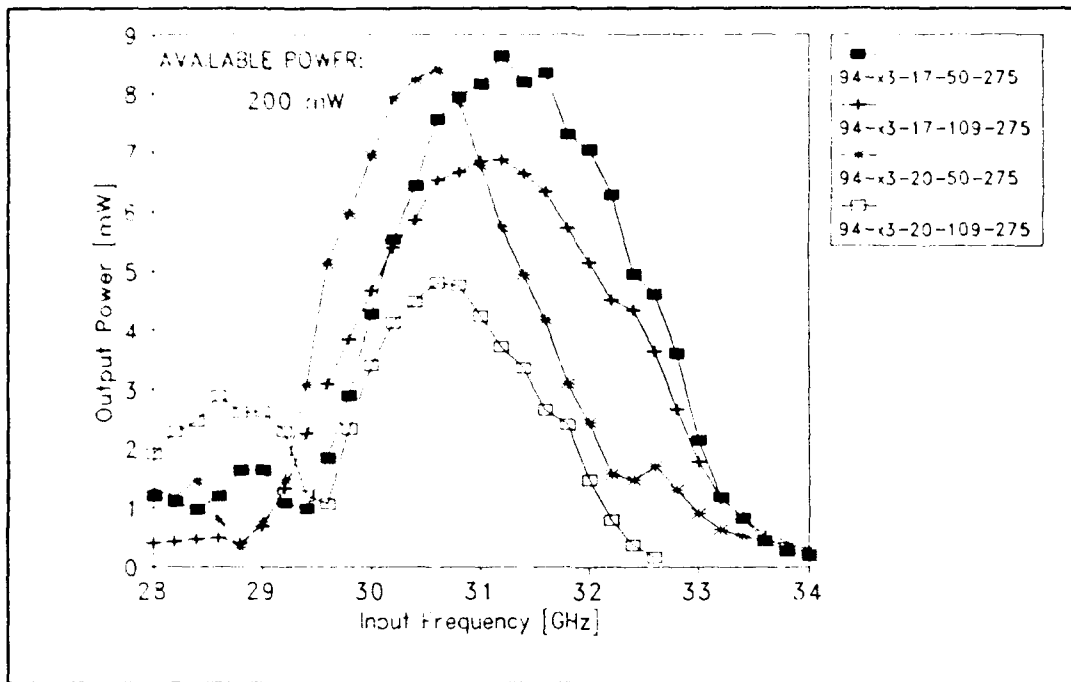


Figure 8.46 The output power versus frequency for the four versions of the 31/94 GHz tripler. (iteration two). Input power: 200 mW.

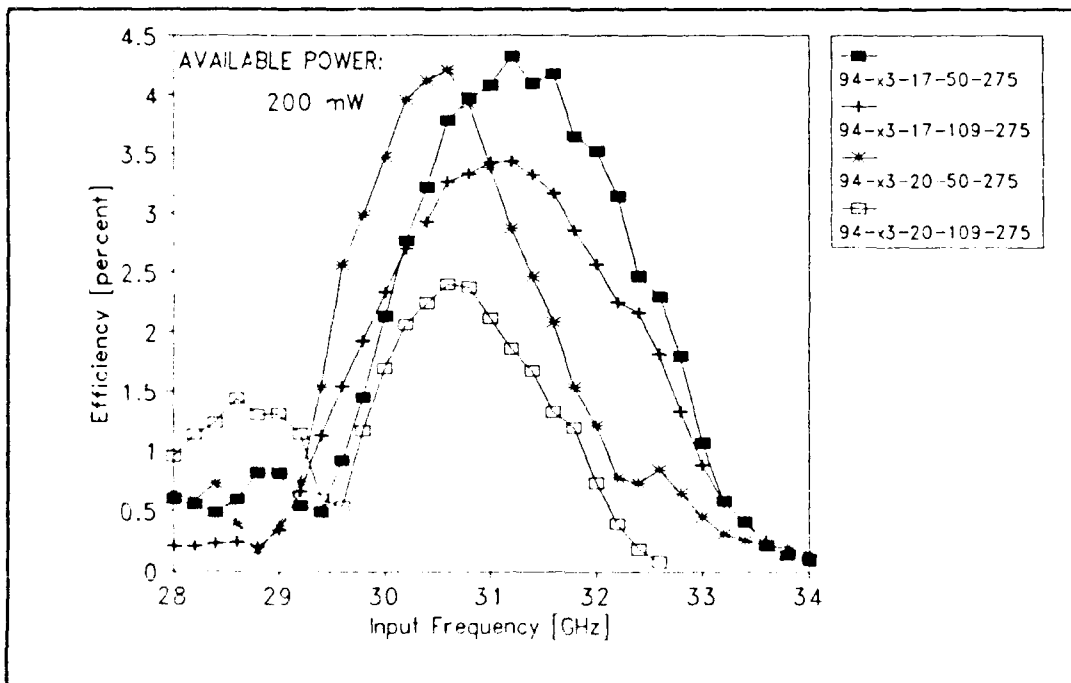


Figure 8.47 Multiplier efficiency versus frequency for the four versions of the 31/94 GHz tripler (iteration two). Input power: 200 mW.

The bias voltages range from approximately -2 volts @ 28 GHz to over -8 volts above 32 GHz. There was approximately 0.5 volts difference in the bias levels at each operating point thus indicating a slight unbalance in the circuit.

8.8.5 Output Power and Efficiency versus Input Power

The measurements in Section 8.8.4 were used to find the frequency of maximum output power. At this frequency, the output power and efficiency were measured as a function of available input power. Fig. 8.48 shows the output power versus input power and Fig. 8.49 shows the multiplier efficiency versus input power.

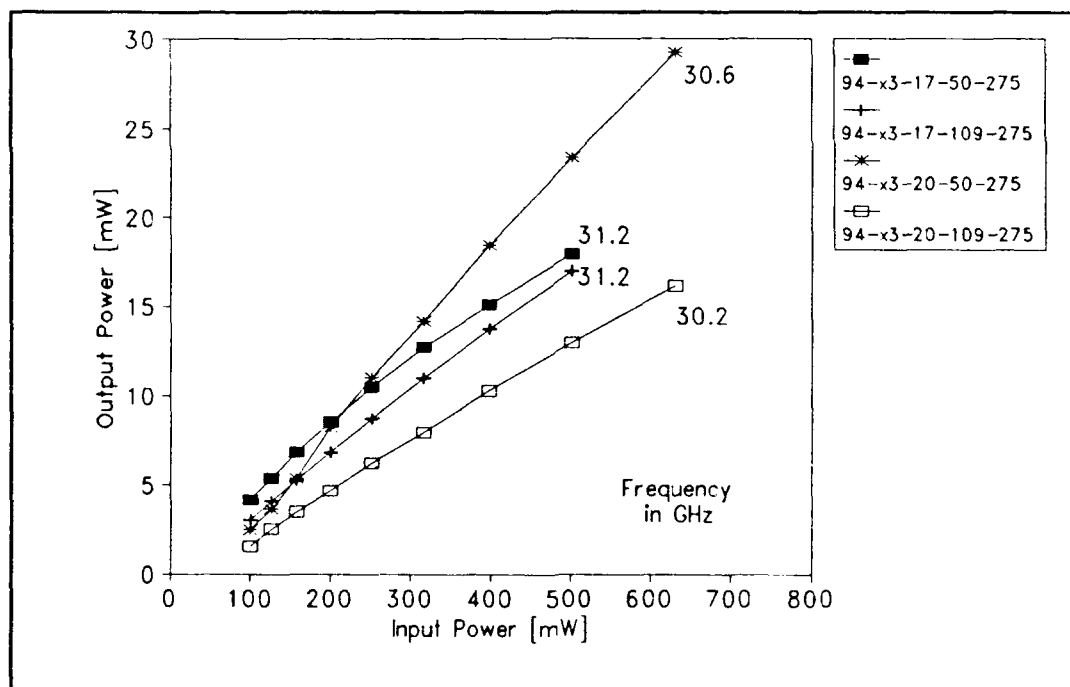


Figure 8.48 Output power versus available input power for the four versions of the 31/94 GHz tripler (iteration two).

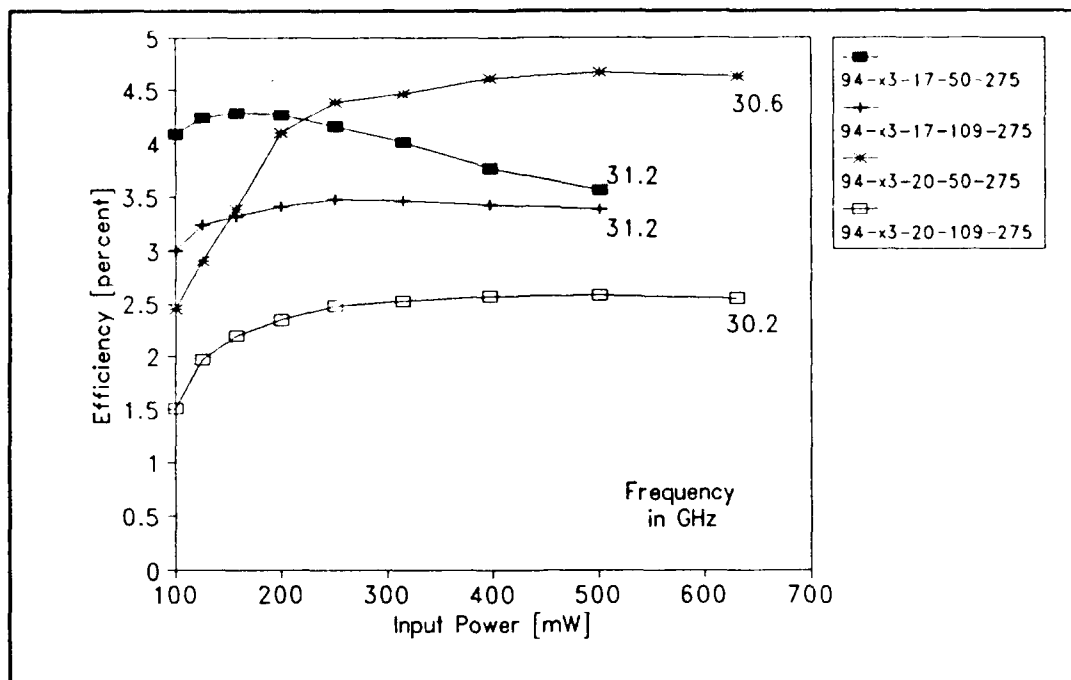


Figure 8.49 Multiplier efficiency versus available input power for the four versions of the 31/94 GHz tripler (iteration two).

8.8.6 Summary of RF Results

The best performance of the 31/94 GHz monolithic tripler (iteration two) is shown in Table 8.19.

TABLE 8.19 RF Performance Summary 31/94 GHz Tripler - Second Iteration						
CHIP/MOUNT	TYPE		FREQ FOR MAX. POWER	MAX. POWER (EFFICIENCY)	MAX. EFFIC (POWER)	INPUT RETURN LOSS
4002/D	17	50	93.6 GHz	17.9 mW (3.6 %)	4.3 % (6.8 mW)	-13.9 dB
3603/K	17	109	93.6 GHz	16.9 mW (3.4 %)	3.5 % (8.7 mW)	-16.4 dB
4304/F	20	50	91.8 GHz	29.3 mW (4.6 %)	4.7 % (23.3 mW)	-17.2 dB
3906/H	20	109	90.6 GHz	29.1 mW (4.5 %)	4.6 % (24.0 mW)	-17.3 dB

8.9 Conclusions

The performance of the 31/94 GHz tripler is summarized as follows:

- * Although the output power and efficiency are lower than expected, the results shown in Table 8.19 are encouraging.
- * The operating frequency of the second iteration tripler is very close to the design frequency.
- * The shorter length of the input line appears to compensate for the shift in the tuning caused by the 15 fF fringing capacitance.
- * The bias voltages of the pumped varactors were quite similar and indicate proper circuit balance over the desired operating range.
- * The input and output tuning as a function of mutually-coupled air bridges overlap appears to behave as expected, however because both the self and mutual inductances are varied by the change in overlap, the resulting tuning change is very small and difficult to measure.
- * The change in input and output tuning point as a function of anode diameter is smaller than expected.

Chapter Nine examines the discrepancies between the experiment and predicted results.

CHAPTER NINE

Discrepancies between Experiment and Predicted Results

9.1 Introduction

This chapter explores several discrepancies between the experimental data and the predicted performance for the 31/94 GHz frequency tripler. More details regarding the measurements can be found in Chapter Eight, and conventional circuit theory is presented in Chapter Two (diode model) and in Chapter Eight (circuit model). The discrepancies are summarized as follows:

Low Output Power and Efficiency: Even upon inclusion of resistive losses in the input and output networks, the output power and measured efficiency of the tripler are much less than predicted by nonlinear theory (including the effects of varactor series resistance). Fig. 9.1 shows the output power and Fig. 9.2 shows the tripler efficiency for two cases:

<u>Predicted (A)</u>	<u>Measured (B)</u>
- Multiplier theory (Ch.2)	- Experimental results (Ch. 8)
- Diode model (Ch. 2)	
- Embedding impedances measured on scale models (Ch.5)	
- Resistive loss based on CBCPW line analysis, test structures, etc. (Ch. 8).	

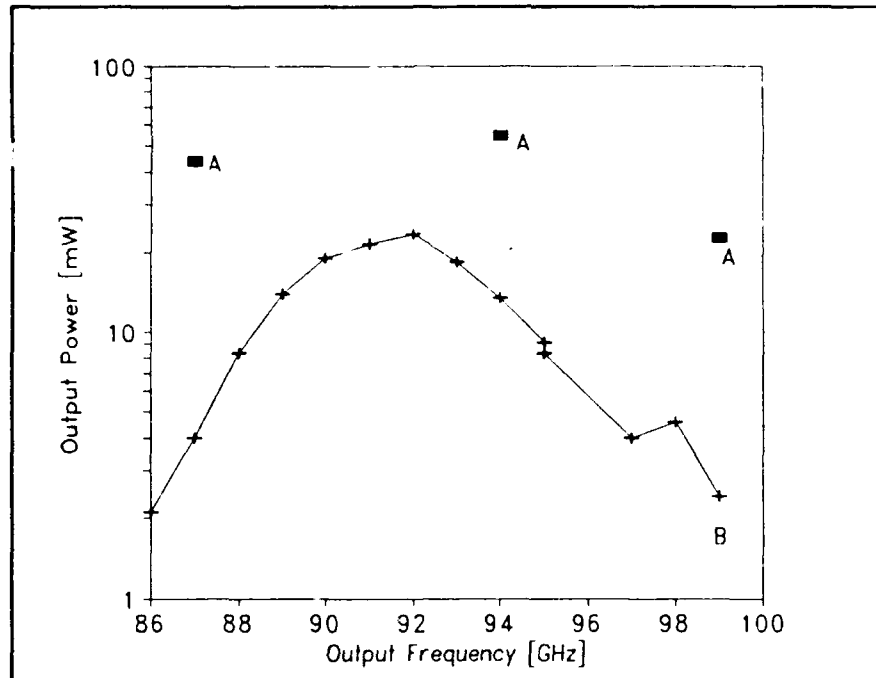


Figure 9.1 Output power versus frequency for the 31/94 GHz tripler. A) Theory, B) Measured

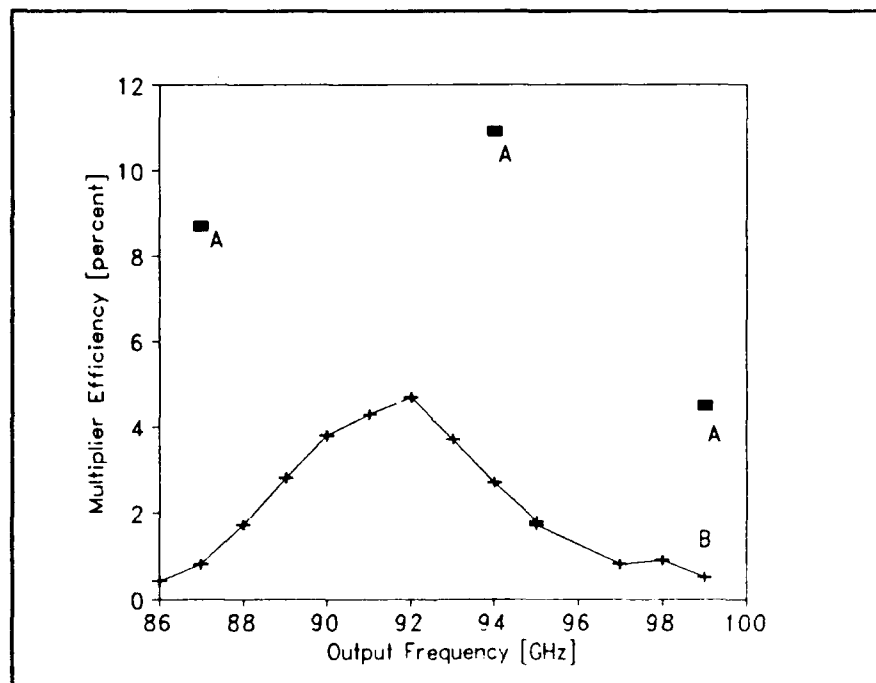


Figure 9.2 Efficiency versus frequency for the 31/93 GHz tripler. A) Theory, B) Measured.

Very narrow output tuning range: The measured small signal output return loss versus reverse bias is shown for the Fig. 8.44. The measurements indicate that the tuning range versus reverse bias from 0 to -10 volts is substantially less than predicted by the conventional theory. However, it is worth noting that the measured input tuning range compares very well with the predicted range (see Table 8.17).

Output small signal reflection is too small for the predicted mismatch at the varactor: The conventional theory predicts the small signal output mismatch to be quite large since the embedding circuits, which were designed for matching to a pumped (large signal) varactor having a resistance of 20 to 30 ohms, will not properly power match into the series resistance of the diode (3 to 4 ohms). A match into about 13 ohms at 94 GHz was inferred from comparing the small-signal data with the Touchstone circuit model by artificially varying the diode series resistance.

The reverse bias voltage for maximum power and efficiency is too low: As predicted by the nonlinear analysis for this particular varactor, the reverse bias voltage for maximum efficiency should be about -10 volts, however the measured data indicates a preferred bias of -5 to -6 volts.

The possible causes for such discrepancies are categorized as follows:

- * Both an increase in the diode series resistance and a simultaneous decrease in the diode junction capacitance as a function of frequency.
- * Unexpected behavior of the MMIC, not corresponding to the scale models.

This chapter examines the circuit theory of the varactor and surrounding geometry for a possible explanation of the observed discrepancies.

9.2 Schottky Diode Model Study - A Circuit Approach

The unusual multiplier behavior can be explained if the varactor series resistance is an increasing function of frequency (and larger than described by conventional theory), and the dynamic junction capacitance is a decreasing function of frequency (and smaller than that predicted by the parallel plate Schottky diode model). The hypothesis presented here is that the RF skin effect is preventing the current from reaching the central region of the diode (at 94 GHz, the skin depth in the anode metal is $0.25 \mu\text{m}$ and $2.5 \mu\text{m}$ in the n^+ GaAs). This reduces the apparent diode size (area), thereby increasing the apparent series resistance and decreasing the apparent junction capacitance.

As a very rough approximation, assume that the current density is uniform throughout that portion of the active layer confined by the tapered ring structure shown in Fig. 9.3. It is assumed that the current entering and leaving the diode is constricted within the skin depths δ_m and δ_b in the anode and the n^+ GaAs respectively. The current enters the depletion region through the top surface of the ring (area proportional to δ_m and leaves the depletion region through the lower surface of the ring (area proportional to δ_b). The values for δ_m and δ_b are

$$\delta_m = \sqrt{\frac{2}{\omega \mu_0 \sigma_m}} = 0.3 \mu\text{m} \quad (9-1)$$

$$\delta_b = \sqrt{\frac{2}{\omega \mu_0 \sigma_b}} = 2.5 \mu\text{m} \quad (9-2)$$

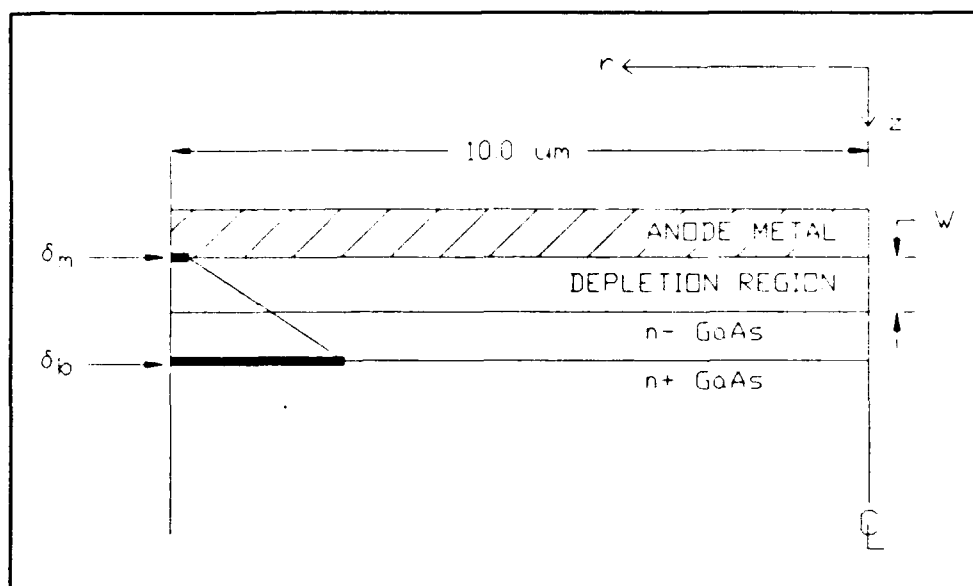


Figure 9.3 A heuristic model used to approximate the current distribution in the active layer (cross-sectional view).

where ω is the radian frequency, μ_0 is the permeability of free space, σ_b is the n^+ buffer layer conductivity, and σ_m is the metal conductivity. At 94 GHz, this model indicates an increase in the apparent series resistance by a factor of 3.5 and a decrease in the apparent zero-bias junction capacitance by a factor of 3, approximately what is needed to account for the observed performance. Therefore, in order to test this hypothesis in a more rigorous manner, two circuit models of the varactor diode were examined: 1) the concentric ring model and 2) the radial transmission line model.

9.2.1 The Concentric Ring Model

Consider the varactor structure to consist of concentric rings as shown in Fig. 9.4. This varactor model includes the following:

- 1) Resistance to z -directed currents in the active layer,
- 2) Carrier inertial inductance in the active layer,
- 3) Radial skin impedance in the buffer layer, and
- 4) Diode junction capacitance at -6 volts bias.

The concentric ring model consists of a parallel arrangement of ten $1\text{ }\mu\text{m}$ wide ring-shaped varactors. Each varactor obeys the parallel-plate capacitance model with the capacitance at -6 volts bias as given in Table 9.1. The current through each diode is considered to be purely z-directed

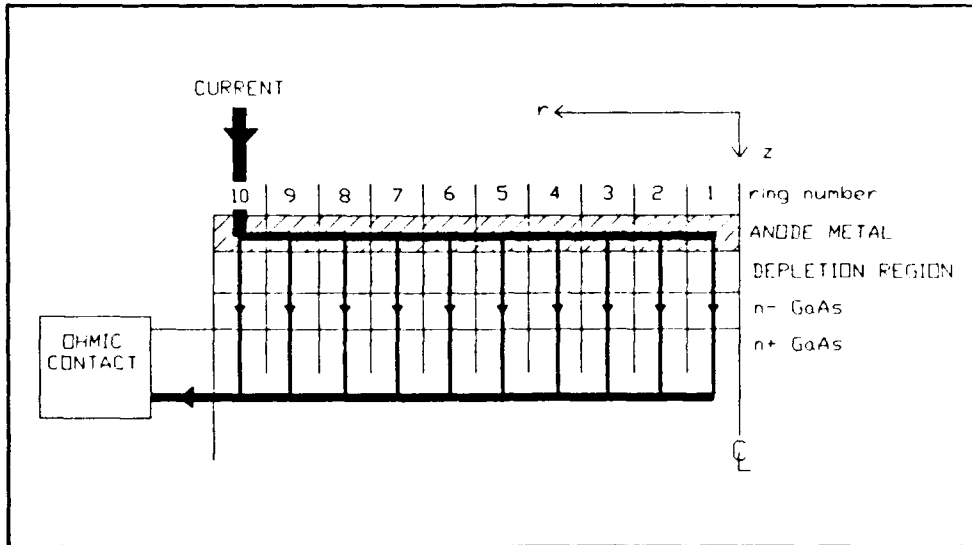


Figure 9.4 A cross-section view of the varactor showing the current distribution in the concentric ring model.

through the undepleted n^- active layer, i.e. no radial current is assumed. Each z-directed current path is tied to the radial current path in the n^+ buffer layer where the current is assumed to be confined to one skin depth in the n^+ material. The equivalent circuit is shown in Fig. 9.5.

The following varactor (chosen for the 31/94 GHz tripler) was used in this study:

Material:	GaAs ($\epsilon_r = 13$)
Substrate:	S.I. GaAs
Anode Diameter:	$20\text{ }\mu\text{m}$
Ohmic contact inner radius:	$13\text{ }\mu\text{m}$
Junction Profile:	ABRUPT
Act. imp. level:	$2.5 \times 10^{16}\text{ cm}^{-3}$, $\sigma_a = 1.1 \times 10^3\text{ S/m}$
Active thickness:	$L_a = 1.4\text{ }\mu\text{m}$
Buffer thickness:	$L_b = 3.0\text{ }\mu\text{m}$
Buffer imp. lev.:	$> 4 \times 10^{18}\text{ cm}^{-3}$ $\sigma_b = 5.0 \times 10^5\text{ S/m}$
Built-in potential:	0.8 volts
Breakdown Voltage:	-33 volts

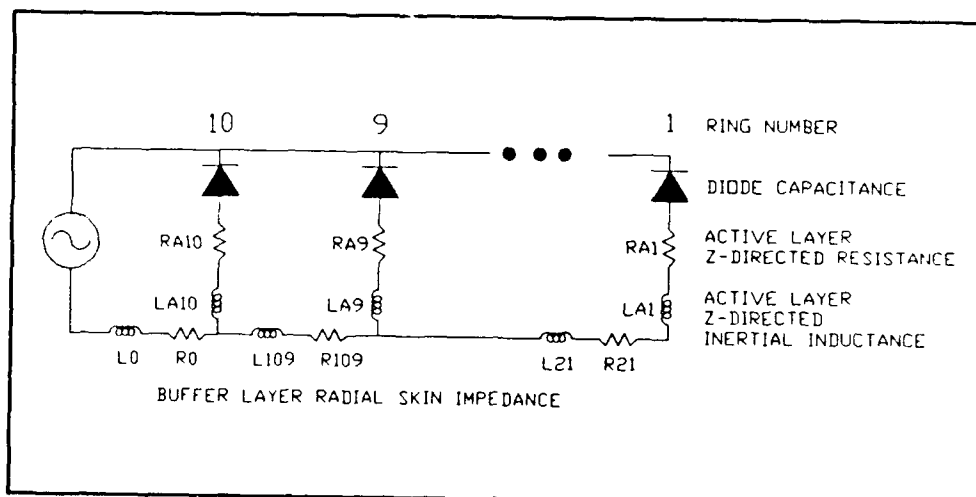


Figure 9.5 The equivalent circuit of Fig. 9.4.

A cross-sectional sketch of the varactor geometry is shown in Fig. 9.6.

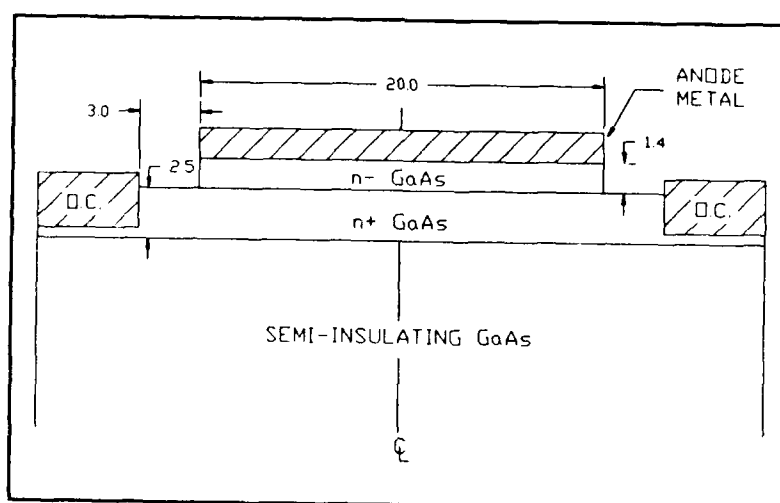


Figure 9.6 Cross-sectional sketch of the varactor used in the 31/94 GHz tripler (dimensions are in microns).

The 20 μm diameter anode consists of a 1.5 μm thick gold electrode which is in intimate contact with the 1.4 μm thick n^- ($2.5 \times 10^{16} \text{ cm}^{-3}$) GaAs active layer. The active layer resides on top of the highly doped, 2.5 μm thick n^+ ($4 \times 10^{18} \text{ cm}^{-3}$) GaAs buffer layer, with the ohmic contact spaced a radial distance of 3.0 μm from the outside edge of the anode. The varactor as well as the entire monolithic circuit are supported by a semi-

insulating GaAs substrate.

In the ring model, the area of the n^{th} ring, A_n , is simply

$$A_n = A_1 (2r_n - 1) = (3.14 \mu\text{m}^2) (2r_n - 1) \quad (9-3)$$

where r_n is the radius of the n^{th} ring. The resistance through each z-directed path of the active layer, R_{an} , was calculated as follows:

$$R_{an} = \frac{\ell_a'}{\pi \sigma_a [r_n^2 - r_{n-1}^2]} \quad (9-4)$$

where $\ell_a' = \ell_a - w_{(-6\text{V})}$ with w as the depletion width at -6 volts bias (see eqn. 2-2). The inductance resulting from carrier inertial effects in the active layer is (Champlin, 1964)

$$L_n = \frac{R_{an}}{\omega_s} \quad (9-5)$$

where the scattering frequency ω_s in GaAs is (Champlin, 1964)

$$\omega_s = \frac{q}{m_e \mu_e} = 4.375 \times 10^{12} \text{ s}^{-1} \quad (f_s = 696 \text{ GHz}) \quad (9-6)$$

with electron effective mass $m_e = 0.067 m_0$ and mobility $\mu_e = 0.6 \text{ m}^2/\text{V}\cdot\text{s}$.

The radial skin resistance through the buffer layer is found from

$$R_{bn} = \frac{1}{2 \pi \ell_b \sigma_b} \ln \left(\frac{r_n}{r_{(n-1)}} \right) \quad (9-7)$$

where ℓ_b is the buffer layer thickness (also the skin depth at 94 GHz). The inductive part of the skin impedance (94 GHz) is found from the radial skin resistance as

$$L_{bn} = \frac{R_{bn}}{\omega} \quad (9-8)$$

since the skin impedance has equal real and imaginary parts.

The z-directed components for each ring are summarized in Table 9.1.

TABLE 9.1 Diode Capacitance; Resistance and Inductance of the Active Layer				
Ring Number	Ring Area A_n [μm^2]	Capacitance C_{j_n} [fF]	Resistance R_{a_n} [ohms]	Inductance L_n [pH]
1	3.1	10.5	220.8	50.5
2	9.4	9.4	73.6	16.8
3	15.7	8.3	44.8	10.2
4	22.0	7.2	31.5	7.2
5	28.3	6.1	24.5	5.6
6	34.6	5.0	20.1	4.6
7	40.8	3.9	17.0	3.9
8	47.1	2.8	14.7	3.4
9	53.4	1.7	13.0	3.0
10	59.7	0.6	11.6	2.7

The radial components (skin effect in the buffer layer) are summarized in Table 9.2.

TABLE 9.2 Resistance and Skin Inductance of Buffer Layer		
From Ring # to Ring #	Resistance [ohms] R_{a_n}	Inductance [pH] L_{b_n} @ 94 GHz
1 - 2	0.098	0.156
2 - 3	0.057	0.091
3 - 4	0.041	0.065
4 - 5	0.032	0.051
5 - 6	0.026	0.041
6 - 7	0.022	0.035
7 - 8	0.019	0.030
8 - 9	0.017	0.027
9 - 10	0.015	0.024
10 - GND	0.037	0.059

The circuit simulation program PSPICE¹ was used to analyze the equivalent circuit of the varactor at a dc bias of -6 volts. A 1 volt peak amplitude, 94 GHz signal was imposed across the varactor and the current

¹ PSPICE is a trademark of MicroSim Corp. (Student version was used for this simulation).

(and current density) through each ring was calculated (see Table 9.3).

TABLE 9.3 Ring Varactor Currents with applied 100 GHz RF, 1 volt amplitude		
Ring Number	Current [mA]	Current Density [mA/ μm^2]
1	0.36	0.115
2	1.09	0.116
3	1.80	0.115
4	2.51	0.114
5	3.24	0.114
6	3.96	0.114
7	4.67	0.114
8	5.40	0.115
9	6.11	0.114
10	6.83	0.114

Although a larger portion of the total varactor current is in the outer rings, the current density is uniform throughout the varactor. This results in a total resistance of 2.3 ohms and capacitance of 56.4 fF which compares well to the parallel-plate diode model ($C = 58.1$ fF and $R_s = 2.3$ ohms). A similar comparison was found at different bias voltages. Therefore, this result clearly indicates that the effects of skin impedance in the n^+ layer and carrier inertia in the n^- layer cannot explain the observed discrepancies.

9.2.2 Radial Transmission Line Model

In order to confirm the results of the simpler concentric ring model, a second approach to analyzing this problem was pursued. Consider the anode and active/buffer layer as a radial transmission line as shown in Fig. 9.7. The radial magnetic field and z-directed electric field propagating along the CPW at the outer edge of the diode ($r = 10 \mu\text{m}$) will excite a TEM wave which then propagates along the radial transmission line

toward the center of the anode. The analysis here departs from the conventional radial line analysis of Montgomery (1948) and Marcuvitz (1951) in that it considers conductive loss and magnetic field penetration into the lower conductor. The hypothesis here is that magnetic field penetration may cause a significant slowing of the propagating wave as is observed along superconducting transmission lines. This slowing will increase the apparent size of the anode possibly to the extent of altering the apparent capacitance and increasing the diode resistance through a radial current density gradient or phase shift.

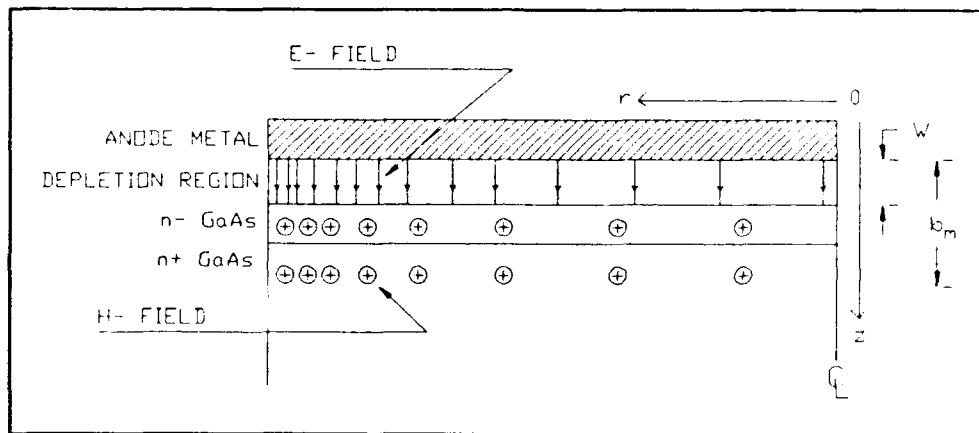


Figure 9.7 The varactor structure as a radial transmission line. The radial line extends from varactor radius 0 μm to 10 μm .

The equivalent circuit for the modified radial line is shown in Fig. 9.8.

The inductance per unit length, L_d , is

$$L_d = \frac{\mu_o b_m}{2 \pi r} \quad (9-9)$$

where b_m is the magnetic field penetration depth (taken to be 4.0 μm). The junction capacitance per unit length is

$$C_d = \frac{2 \pi \epsilon_o \epsilon_r r}{w} \quad (9-10)$$

where w is the depletion region depth.

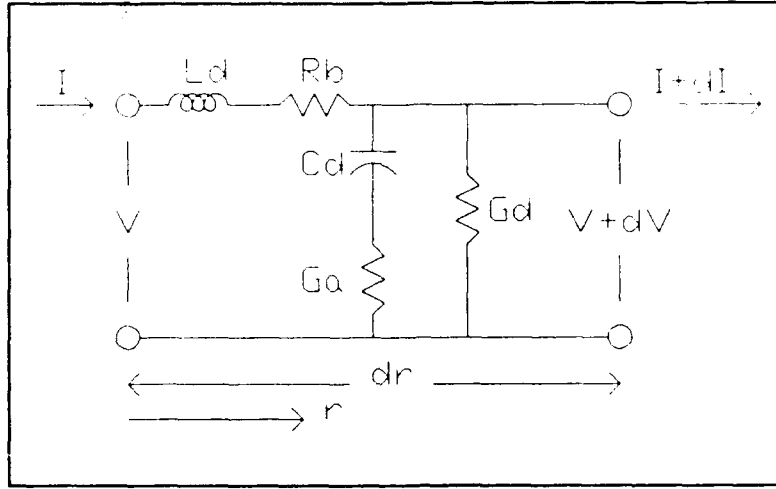


Figure 9.8 The incremental equivalent circuit for the radial line of Fig. 9.7. This circuit includes conductive losses and magnetic field penetration into the active and buffer layers.

The conductance per unit length through the depletion region is

$$G_d = \frac{2\pi\sigma_d r}{w} \quad (9-11)$$

where σ_d is the conductivity of the depletion region. The conductance through the active layer is given by

$$G_a = \frac{2\pi\sigma_a r}{\ell_a'} \quad (9-12)$$

where $\ell_a' = \ell_a - w$. Finally, the resistance per unit length through the buffer layer is given by

$$R_b = \frac{1}{2\pi\ell_b\sigma_b r} \quad (9-13)$$

Using these definitions for the incremental elements, the characteristic impedance and admittance of the radial line are

$$Z_o = \sqrt{\frac{\mu_o}{e_o e_r} \frac{b_g}{2\pi r}} - j \frac{1}{2\pi \sigma_b \ell_b k_p r} \quad (9-14)$$

$$Y_o = \frac{\frac{2\pi r}{w} \sqrt{\frac{e_o e_r}{\mu_o}}}{1 + j \frac{k_p \ell_a}{w \sigma_a} \sqrt{\frac{e_o e_r}{\mu_o}}} - j \frac{2\pi \sigma_d r}{k_p w} \quad (9-15)$$

where

$$k_p = \omega \sqrt{\mu_o e_o e_r} \quad (9-16)$$

Note that in this analysis, $Z_o \neq 1/Y_o$. By analogy with equation 33 in Sec. 8.5 of Montgomery, et al. (1948), the following differential equations for radial line voltage and current were developed:

$$\frac{1}{r} \frac{d}{dr} \left(r \frac{dV}{dr} \right) + \zeta^2 V = 0 \quad (9-17)$$

$$r \frac{d}{dr} \left(\frac{1}{r} \frac{dI}{dr} \right) + \zeta^2 I = 0 \quad (9-18)$$

where ζ , the complex propagation constant, is defined as

$$\zeta^2 = Y_o Z_o k_p^2 \quad (9-19)$$

The solutions to the eqns. (9-17) and (9-18), which are analogous to eqn. 35 Sec. 8.5 of Montgomery et al., are

$$V(r) = \left[\frac{J_1(\zeta r_o) N_o(\zeta r) - N_1(\zeta r_o) J_o(\zeta r)}{\frac{2}{\pi \zeta r_o}} \right] V(r_o) - j \frac{\sqrt{Y_o Z_o}}{Y_o(r_o)} \left[\frac{J_o(\zeta r) N_o(\zeta r_o) - J_o(\zeta r_o) N_o(\zeta r)}{\frac{2}{\pi \zeta r_o}} \right] I(r_o) \quad (9-20)$$

$$\frac{\sqrt{Y_o Z_o}}{Y_o(r)} I(r) = \frac{\sqrt{Y_o Z_o}}{Y_o(r_o)} \left[\frac{N_o(\zeta r_o) J_1(\zeta r) - J_o(\zeta r_o) N_1(\zeta r)}{\frac{2}{\pi \zeta r_o}} \right] I(r_o) - j \left[\frac{J_1(\zeta r_o) N_1(\zeta r) - N_1(\zeta r_o) J_1(\zeta r)}{\frac{2}{\pi \zeta r_o}} \right] V(r_o) \quad (9-21)$$

where the boundary condition at r_o (port termination) is $V(r_o)$ and $I(r_o)$. J_0 and J_1 are complex Bessel functions of the first kind of order 0 and 1, while N_0 and N_1 are complex Neumann functions (Bessel functions of the second kind) of order 0 and 1. Details regarding the derivation of eqns. (9-14) through (9-21) are given in Appendix J.

A MathCAD routine was written to solve eqns. (9-20) and (9-21) simultaneously for the voltage and current along a radial line having the 20 μm diameter varactor geometry and terminated at $r_o = 0$ with $V(r_o) = 1$ volt and $I(r_o) = 0$ (open circuited). The "input" impedance seen at the outer edge of the varactor ($r = 10 \mu\text{m}$) at 94 GHz is $2.2 - j 29.5$ ohms (capacitance of 57.4 fF); again this result is very similar to the parallel-plate varactor model. Thus for the given varactor geometry, the magnetic field penetration into the n^- and n^+ layers has only a very small effect on the impedance of the varactor and cannot explain the unusual measurements.

9.3 Cavity Resonance Caused by CBCPW Via Hole Spacing

An alternative explanation for the discrepancies between the predicted and measured results was found upon careful comparison of the via hole locations originally specified to the fabricator (Martin Marietta Laboratories) and those of the delivered circuit. Fig. 9.9 shows the top-side lithography of the 31/94 GHz triplers (including via hole

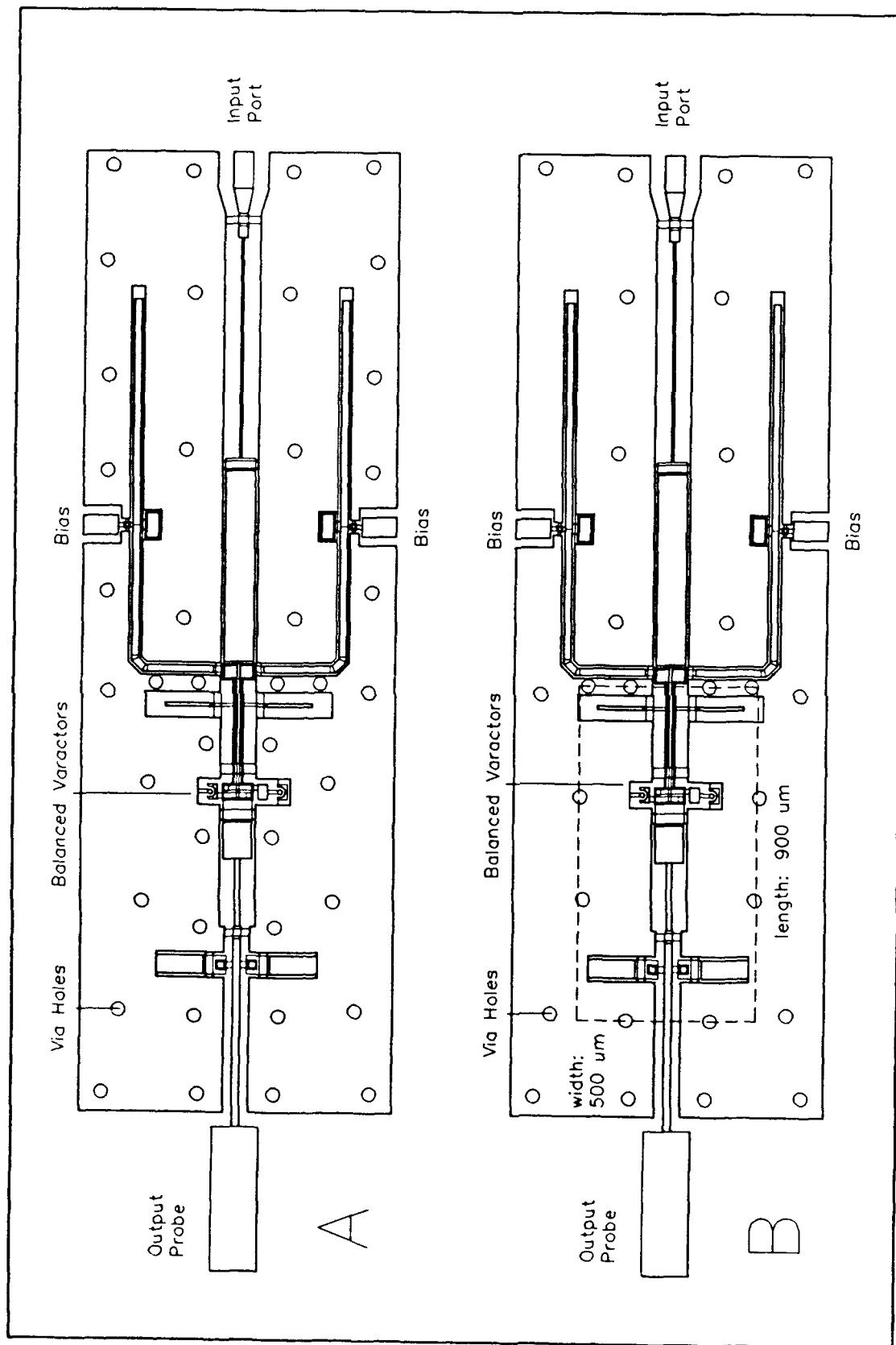


Figure 9.9 Scale drawing of the monolithic 31/94 GHz frequency tripler. (A) original specification and (B) delivered chip.

locations) for A) original specification and B) delivered chip. Superimposed on sketch (B) is a dashed line indicating the virtual walls of a rectangular resonant cavity formed by via holes. The cavity has a length of approximately 900 μm and a width of 500 μm . The height of the cavity is governed by the substrate thickness (75 μm). As a first order approximation in calculating the resonant frequencies of this cavity, eqn. 7.25 in Collin (1966) was applied:

$$f_{nm1} = \frac{c}{\sqrt{\epsilon_r}} \left[\left(\frac{l}{2(\text{length})} \right)^2 + \left(\frac{m}{2(\text{width})} \right)^2 + \left(\frac{n}{2(\text{height})} \right)^2 \right]^{\frac{1}{2}} \quad (9-22)$$

where c is the velocity of light. The three fundamental modes are

l,m,n:	0,0,1	-->	46 GHz
	1,0,0	-->	83 GHz
	1,0,1	-->	95 GHz

The accuracy of the predicted resonant frequencies as applied to the MMIC is probably no better than ± 10 percent since the cavity walls are not solid as is assumed by eqn. 9.22. However, the latter two resonant frequencies correspond well with two observed resonances (labeled "b" and "d") present in the small-signal output return loss measurements as shown in Fig. 9.10. Resonances "a" and "e" are outside the CBCPW/waveguide probe bandwidth and "c" is the desired tuning of the varactors.

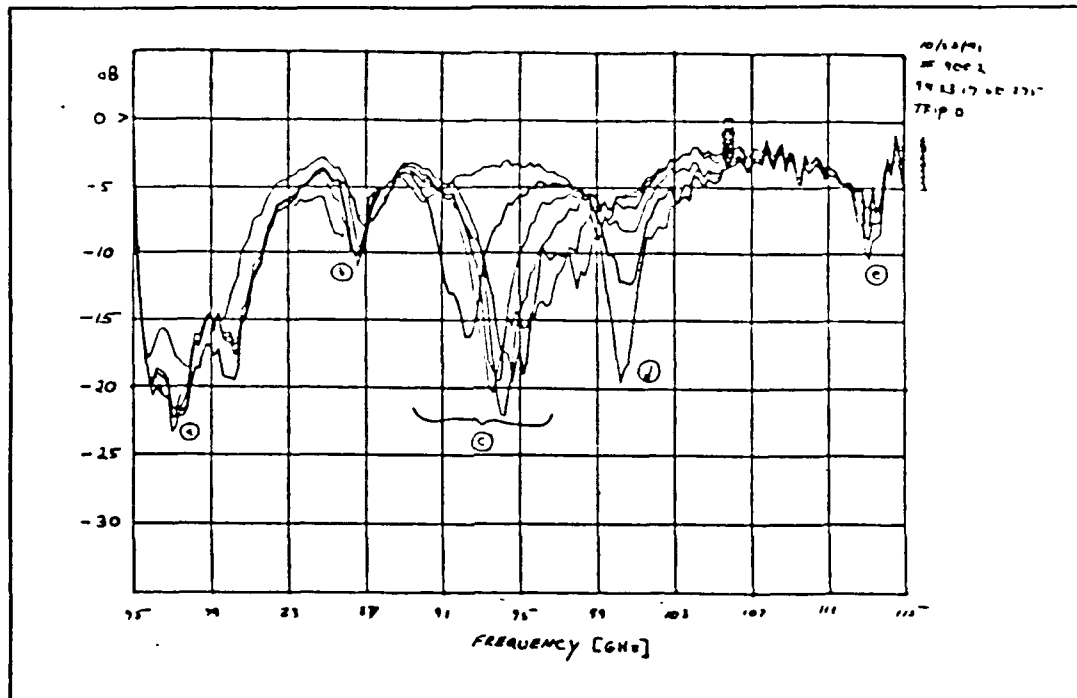


Figure 9.10 Typical small-signal output return loss measurement on the 31/94 GHz frequency tripler for five different bias voltages. (see text).

The calculations here suggest that the fixed resonances observed in the small-signal return loss measurements are indeed associated with the virtual rectangular waveguide cavity surrounding the varactors. Furthermore, the frequencies of these fixed resonances are extremely close to the varactor tuning points hence a strong interdependence is expected (notice the variation in Q of the resonances as a function of bias) together with an alteration in the embedding impedances of the varactors. Therefore, it is inferred from this study that these resonances are directly related to the observed discrepancies, however due to the complicated nature of the electromagnetic fields in the region of the varactors and cavity, no rigorous study of the phenomenon was performed. A few additional via holes in the region very near the varactors will eliminate this problem in future iterations of this tripler.

9.4 Conclusions

The via hole spacing appears to explain the observed behavior of the varactors. The skin effect in the varactor diode appears not to explain the observed discrepancies, but may be important at higher frequencies. It is interesting to note that experimentally, every type of frequency multiplier demonstrates lower efficiency and lower output power than can be explained by the nonlinear analysis and embedding-circuit loss. Under 100 GHz, the effects of skin impedance, magnetic field penetration, and carrier inertia within the varactor are much too small to contribute significantly to the observed multiplier performance. Additional experimental and theoretical studies in multiplier performance are needed in order to close the gap between circuit model predictions and the experimental observations.

CHAPTER TEN

Conclusions

10.1 Overview

Research over four and a half years has culminated in the design, fabrication, and evaluation of four integrated multiplier circuits that clearly demonstrate the potential of planar and monolithic (MMIC) technology as a viable alternative to whisker-contact technology up to 250 GHz. As a prelude to the more complex monolithic designs, a planar Schottky varactor was designed, fabricated at UVA, and evaluated as a 75/225 GHz frequency tripler for direct comparison with a whisker-contacted counterpart. The encouraging results shown in Chapter Three illustrate that planar varactor performance can equal whiskered diodes at 230 GHz. Planar technology was then immediately extended to include not only the varactor but also embedding-circuitry and waveguide probes in an optimized single chip design. This effort, the outcome of many fabricators, technicians, machinists, and other support personnel at NRAO, UVA, and Martin Marietta Laboratories has resulted in a prototype monolithic coplanar waveguide (CPW) 80/160 GHz doubler (Chapter Six) and 80/240 GHz tripler (Chapter Seven). These prototypes demonstrate the application of MMIC technology up to 250 GHz. Such MMIC designs allow for much better control of embedding-circuit parameters than is physically possible with whisker-contacted or even hybrid planar MIC designs. Current industrial applications at 94 GHz prompted the design of a CPW 31/94 GHz tripler incorporating many of the techniques developed in the higher

frequency study. Within a six month period, the 31/94 GHz tripler showed state-of-the-art performance at 94 GHz with over 25 mW of output power with an efficiency of 5 percent, thus demonstrating the flexibility of the CPW design to meet the current demands of industry.

The important ideas and concepts presented in this report of which the author considers new, novel, or unique are outlined below.

- * First fully monolithic varactor frequency doubler (80/160 GHz) and tripler (80/240 GHz) to operate above 100 GHz - The extensive background research of Chapter One shows that as a result of this research, MMIC technology now extends up to 250 GHz.
- * State-of-the-art output power at 94 GHz using a MMIC tripler - This research has resulted in the first MMIC tripler with state-of-the-art output power at 94 GHz with over 25 mW of output power.
- * First extensive use of coplanar waveguide - Coplanar Waveguide is currently considered a novelty for industrial applications due primarily to the lack of accessible CAD models. Through the use of CPW, CBCPW, discontinuities, and waveguide probes, this research demonstrates the feasibility of coplanar technology for MMIC designs in the millimeter-wave band.
- * Mutual inductance provides simultaneous tuning of the second and third harmonics in CPW triplers - The mutual inductance geometry in the MMIC tripler is useful in providing a very compact idler loop without sacrificing the tuning of the input and output circuits. *Such circuits are only possible using the techniques of MMIC technology.*
- * New hybrid MMIC RF/DC bias lines - Using a multi-layer technique, the DC bias lines run on top of the RF coplanar lines thus providing separate bias yet balanced RF excitation to the varactors.
- * First direct comparison of planar and whisker-contacted Schottky varactors. Using a well-understood tripler mount, the UVA planar varactor was directly compared with existing data for the whisker-contacted varactor. This work demonstrates that planar technology can meet and possibly exceed the performance of the whisker-contacted counterpart up to 240 GHz.

10.2 Suggestions for Further Research

The following list of suggestions is offered to the future multiplier researcher in the hope that it provides some insight into the limitations of the current state-of-the-art:

- * More innovative circuit design is needed to improve frequency isolation, increase embedding-circuit bandwidth, and lower transmission line loss, since the Schottky varactor diode has not yet demonstrated its theoretical potential.
- * Continue to explore the possibilities offered through MMIC designs. MMIC technology offers far better control over circuit parameters than can be accomplished using MIC techniques. Although conductor-backing the MMIC has the advantage of improved heat dissipation and simplified chip mounting, more work is needed to improve via hole fabrication technology to minimize resistive losses and reduce substrate cracking.
- * Expand the use of numerical methods such as finite-element analysis to examine the varactor, transmission line discontinuities, waveguide transitions, etc. Only recently, through the availability of very fast computer workstations, have such numerical methods become practical and convenient research tools.
- * Consider the nonlinear element, the embedding-circuitry, and the mounting fixture collectively in the pursuit of optimized multiplier designs. This becomes ever more important as the operating frequency is increased into the submillimeter-wave region.

As a final note, one additional suggestion is offered to the multiplier researcher: It is imperative that one understands the current state-of-the-art and uses this knowledge as a foundation for charting a new course to meet the needs of tomorrow.

APPENDIX A

Millimeter and Submillimeter-Wave Fundamental Sources

Currently, fundamental sources of LO power above 100 GHz may be categorized as either tube-type (vacuum and gas-filled) or solid-state devices. The tube-type devices have been used in laboratory measurements and in pioneering millimeter and submillimeter-wavelength astronomical observations for many years. Conventional low-noise solid-state LO sources have a striking drop in output power with increasing frequency, thus rendering them useless above about 150 GHz. However, the new technology of crystal growth by molecular-beam epitaxy (MBE) has opened the door for realization of rather novel devices that generate low level millimeter and submillimeter-wave oscillations with rather good noise performance. In this section, the advantages and disadvantages of both tube-type and solid-state LO sources will be briefly explored.

A.1 Tube-Type Oscillators / Amplifiers

Backward-Wave Oscillator (BWO) - This is a type-M (magnetic) vacuum tube containing a cavity-type slow-wave structure which supports an electron-bunching induced longitudinal RF wave that travels from the electron-beam collector to the electron gun, i.e. backwards. The BWO can be tuned up to an octave or more and can be phase-locked by varying the DC voltage between the cathode and the slow-wave structure. Output power ranges from 500 mW at 50 GHz to less than 1 mW at 1500 GHz (Kantorowicz, 1979). Modern BWO tubes can be quite small and weigh under 5 lbs, however

a kilovolt power supply and a cooling-water system are required (Laundrie, 1990). Note that Carcinotron is the trade name for BWO's manufactured by THOMSON-CSF.

Gyrotron - This is a type-M tube that provides gain from free-electrons twirling in a uniform magnetic field. This linear cyclotron gain mechanism originates with the relativistic energy dependence of the electron gyrofrequency. As the electrons interact with the oscillating electromagnetic disturbance, a phase focusing effect arises which leads to electron bunching. The upper frequency limit of a tunable Gyrotron is set by the strength of the superconducting magnetic. Operation in the second-harmonic mode of the electron cyclotron frequency has an advantage over operating at the fundamental since only half the magnetic field is required. Continuous wave (CW) power of over 200 kW at 28 GHz is possible (Hirshfield, 1979). In excess of 20 W of CW power over the 100 to 300 GHz range was also demonstrated (Brand, 1990). CW power of 1 mW at 414 GHz and 1 μ W at 614 GHz has also been reported (Zaytsev, 1974).

Klystron - This is a type-O (original) linear-beam vacuum tube which can be either an amplifier or an oscillator. The reflex Klystron is a single-cavity Klystron which operates as an oscillator by using a reflector electrode after the cavity to provide positive feedback via the electron beam. It is tuned by mechanically adjusting the cavity size. The high-Q cavity required for electron bunching strongly limits the operational tuning bandwidth. These sources have very low AM and FM noise. Small Klystrons useful for LO sources weigh under 1 lbs and can generate 100 mW at 100 GHz (Kantorowicz, 1979). However, a large DC power supply and a cooling system are required.

LASER - Far infrared (FIR) lasers are gas-filled cavity tubes that are pumped with optical radiation. This radiation via stimulated emission can be quite strong at frequencies above 150 GHz (Inguscio, 1986, Densing, 1991). The oscillation frequency is dictated by the type of gas used and it is not widely tunable (typically less than 1.5 MHz). The output power is a strong function of the gas and can vary from nanowatts to several watts. Gas laser systems are very large because of all the required support paraphernalia.

Ledatron - This is a type-M free electron beam device containing periodic circuit elements where a bunched electron beam interacts with an electromagnetic field. To overcome the smaller interacting circuit structure necessary for higher operating frequencies, the **Ledatron** uses the Fabry-Perot interferometer as a practical resonator for the generation of submillimeter waves. Two modes of operation are possible: The Fabry-Perot mode in which the electron beam reacts with standing waves and the surface wave mode which involves the interaction between an electron beam and a backward wave contained in the surface wave guided by the grating. Higher operating frequencies are possible with the Fabry-Perot mode. This tube is similar in structure to the **Orotron** developed in the U.S.S.R. Experimentally, the **Ledatron** has developed 1 W of CW power at 70 GHz (Mizuno, 1979).

Magnetron - This is a type-M tube in which the electrons emitted by the cathode move in a curved path between the cathode and the anode under the combined force of the electric and magnetic fields. The tube is electrically a slow-wave structure which is closed on itself (reentrant) where oscillations are possible only if the total phase shift around the

structure is an integral multiple of 2π radians. The tube can generate very strong pulses of RF power (over 1 MW peak power at 10 GHz) which makes radar practical (Liao, 1985). A 2.3 GHz magnetron is used in the household microwave oven. However, due to the pulsed nature of the RF power, the magnetron is of little value for LO applications.

VMMA - The Vacuum Microelectronic Microstrip Amplifier is a micrometer-dimension analog of the vacuum triode. A signal applied to the grid electrode microstrip results in density bunching of electrons which are field emitted from a cold cathode. The electrons are then collected by a positively-biased output microstrip anode. Although still in the early research stages, this technology theoretically has the potential of generating watt-level amplification up to 100 GHz, however none have ever been tested. It is proposed that geometrical alterations can increase the operational frequency to 1 THz (McGruer, 1991). External equipment such as a high voltage power supply and a cooling unit will be needed.

A.2 Solid-State Oscillators / Amplifiers

Josephson Oscillator - A Josephson junction is a voltage controlled oscillator with the potential for wide tunability and a fast tuning rate. There are three types of Josephson-effect oscillators: the resonant fluxon, the flux flow, and small junction arrays. The resonant fluxon and flux flow oscillators use long junctions with junction dimensions much larger than the Josephson penetration depth.

The oscillatory motion of the magnetic flux quanta (fluxon) in long Josephson tunnel junctions emit radiation during reflection at the edges

of the junction. Coherently adding the signals radiated by eight long junctions loosely coupled to a transmission line has produced 5 nW at 7.6 GHz (Monaco, 1988). The resonant propagating fluxon is only usable in the lower millimeter region due to the existence of a frequency limit which is typically 100 GHz. Furthermore, this fluxon occurs only at particular resonant frequencies determined by the junction length.

The flux flow type oscillators utilize the motion of a vortex array (flux flow) in long Josephson tunnel junctions. The unidirectional flux flow does not have a frequency limit up to the gap frequency of about 1 THz and it can be realized at any frequency. Experiments have demonstrated unidirectional flux flow oscillations between 100 and 430 GHz with maximum output power estimated to be 1.84 μ W at 290 GHz (Nagatsuma, 1983).

The disadvantages of the single junction source such as low impedance, low output power level, and large linewidth can be overcome by using a physical array having a large number of phased-locked junctions. A 40 junction array has been demonstrated to deliver 1 to 7 μ W of power into a 20 to 100 ohm resistive load from 350 to 450 GHz (Wan, 1989). The upper limit was established by the onset of large losses in the Lead alloy superconducting microstrip. Gold shunted Nb/AlO_x/Nb junctions have produced 1 μ W at 200 GHz and 350 GHz (Wan, 1991).

Resonant Tunneling Diode (RTD) - The RTD or Quantum-Well oscillator is a double-barrier semiconductor structure forming a quantum well containing only one quasibound-state energy level. Only electrons with longitudinal energy equal to the quasibound state energy can traverse the structure via tunneling. The applied voltage affects the availability of

such energetic electrons such that a negative conductance region occurs. This region is the basis for all of the high-speed oscillations observed to date. The RTD frequency is related to the size of the double-barrier structure and biasing. GaAs/AlAs RTD's have demonstrated $0.2 \mu\text{W}$ at 420 GHz with a tuning range of 10 percent (Brown, 1990). InAs/AlSb structures have demonstrated oscillations up to 712 GHz with output power of $0.32 \mu\text{W}$ (Brown, 1991). In these devices, shot noise is suppressed thus yielding noise levels relative to the carrier comparable to Gunn oscillators.

Transferred-Electron Devices (TED) - This is also known as the Gunn Effect oscillator, which is the transfer of conduction electrons from a high-mobility semiconductor energy valley to a low-mobility, higher energy satellite valley. This effect, found in such semiconductors as GaAs and InP, causes a negative differential resistance to occur, hence oscillations. The operating frequency is related to the diode geometry. However, when operating in a resonant circuit, i.e. cavity, the operating frequency can be increased and tuning is possible. Commercial units have demonstrated over 60 mW of CW power at 100 GHz (Millitech, 1990). The frequency can be tuned either mechanically or electrically with at least 10 mW available over a 10 percent bandwidth near 100 GHz. A greater tuning range is possible by harmonic enhancement. A third-harmonic Gunn oscillator has been demonstrated which produced about $500 \mu\text{W}$ over a tuning range from 70 to 90 GHz (Cohen, 1991). For fixed-tuned applications, the stability and noise performance can be further improved by using a dielectric resonator in the "whispering gallery" mode. Such an oscillator has been fabricated and evaluated at 90 GHz showing the improved stability and noise performance as compared with cavity-type designs (Cros, 1991).

For all current Gunn oscillator designs, the power generation decreases rapidly above 100 GHz and renders the device useless above 150 GHz.

Transit Time Diodes - The negative resistance mechanism in these devices occurs from charge injection together with transit time delay. There are many ways to inject charge into the drift region hence leading to a number of special device properties. In the **IMPATT** - **IMPact-ionization Avalanche Transit Time** diode, charge injection is via the avalanche breakdown mechanism. Experimental results of 1 Watt of CW power at 100 GHz dropping to 50 mW at 200 GHz have been reported (Kuno, 1979). These devices are extremely noisy due to the avalanche effect and, in some cases, bias oscillations (period-doubling bifurcations) and chaos have been observed (Brazil, 1981, Sobky, 1989,). The **BARRITT** - **BARRier Injection Transit Time** device uses a forward-biased p^+n or n^+p junction for charge injection. The efficiency and power are substantially lower than the IMPATT and the low mobility p-type carriers limit the operating frequency. Currently, CW power of only 10 mW at 10 GHz has been reported (Sze, 1985). Charge injection in the **TUNETT** - **TUNNELing Transit Time** diode is through a single heterojunction barrier or tunneling through a reverse-biased p^+-n junction. Oscillations as high as 338 GHz (10 mW) pulsed power has been reported (Nishizawa, 1979). However, recent computer modelling has shown that 200 mW at 100 GHz and 20 mW at 500 GHz is theoretically possible (Haddad, 1990). The **QWITT** - **Quantum Well Injection Transit Time** diode injects charge using a double barrier (quantum well) scheme. Noise is similar to that of the TUNETT. A higher frequency of operation is also expected (Kesan, 1987), however, this device has not yet been fabricated. Finally, the **MITATT** - **MIxed Tunneling**

and Avalanche multiplication Transit Time device incorporates two mechanisms for charge injection. Experimental results of GaAs MITATT structures show a CW output power of 3 mW at 150 GHz (Elta, 1980) and good noise performance is expected since the MITATT utilizes tunneling current.

Transistor Amplifiers / Oscillators - Significant advances in transistor design and fabrication technology throughout the past decade have aggressively pushed the operating frequency above 100 GHz. The mainstay of this technology is the conventional **HEMT** - **H**igh **E**lectron **M**obility Transistor or **MODFET** which is a high frequency, low noise device of GaAs/AlGaAs structure. The drain-to-source conduction is through a higher electron mobility two-dimensional electron gas in the GaAs with electrons drawn from the AlGaAs. Amplification has been demonstrated at 94 GHz with 3.4 mW output and 2 dB of power gain (Smith, 1986). A marked improvement in power performance has been shown with the addition of an InGaAs quantum-well. This **Pseudomorphic HEMT** has been demonstrated as an amplifier producing 62.7 mW at 94 GHz with 4 dB of gain (Streit, 1991), 9 mW at 94 GHz with gain of 3.3 dB (Smith 1988) and 500 mW at 44 GHz (Smith, 1991). The quantum well provides excellent electron confinement and higher electron sheet densities. The addition of AlGaAs doping on both sides of the InGaAs quantum well and planar doping techniques have greatly improved the current handling capability of the structure and f_{max} greater than 66 GHz is reported (Ng, 1989a). This **Planar Doped-Double Heterostructure Pseudomorphic HEMT** has demonstrated 140 mW of output power at 60 GHz (3 dB gain) (Smith, 1987) and 57 mW at 94 GHz (Kao, 1989). Other transistors have also shown relatively high output power in the millimeter-wave region. The **Doped Channel Pseudomorphic HFET** which is a

heterostructure FET in which the mobility in the InGaAs quantum-well is reduced by excess Indium doping to improve the transconductance and the current density by lattice straining. Note that this is technically not a HEMT since electron-mobility has been reduced. f_T greater than 45 GHz has been reported (Ng, 1989b) and at 94 GHz, 32 mW and 3 dB power gain has been reported (Smith, 1989). A review of the millimeter-wave power amplifiers using pseudomorphic HEMTs as found in (Smith, 1990). Measured performance of a conventional MESFET with ion-implanted InGaAs has shown oscillation at 92.3 GHz with output power of 14 mW (Schellenberg, 1991). Finally, conventional Heterojunction Bipolar (HBT) transistors have been fabricated using GaAlAs/GaAs Technology. The f_{max} of such devices has been determined to be above 120 GHz (Asbeck, 1987). A dielectric resonator have been used together with a HEMT yielding a stable low-noise 1 mW oscillator (DRO) at 30 GHz (Wilson, 1991).

Oscillator Grids - Recently, two-dimensional arrays of active devices have been explored as a means of achieving high power in the millimeter-wave region by free space combining the power from individual devices. A phase locked grid of 25 (5 x 5) MESFETs has been demonstrated to have a peak Equivalent Radiated Power (ERP) of 20.7 Watts at 9.7 GHz (Popovic, 1988). A 100 MESFET planar grid (10 x 10) has given 21 Watts of CW ERP at 5 GHz (Popovic, 1991). The planar nature of these arrays makes it possible to fabricate a large number of transistors using planar monolithic technology for operation above 100 GHz, however no such grid has ever been fabricated. Low frequency Gunn diode grids have been fabricated. Because of the rather poor efficiencies of the Gunn diodes, grid overheating has been a major problem. However, a recent experimental

result for a 16 element (4 x 4) grid incorporating patch antennas has demonstrated an ERP of 22 Watts at 9.6 GHz with no overheating problems (York, 1990).

APPENDIX B

Millimeter and Submillimeter-wave Frequency Multipliers

Over the past few decades, the abrupt-junction Schottky diode has been the mainstay of millimeter and sub-millimeter wave frequency multiplication circuits. Originally whisker-contacted, the Schottky diode, driven by the need to circumvent the mechanical problems associated with the whisker, has been evolving into planar geometries. Recently however, other technologies have challenged the Schottky diode, especially in the longer wavelength region. In this section, a brief discussion of the various technologies will be presented and the state-of-the-art in frequency multiplication will be summarized in tabular form. ONLY EXPERIMENTAL RESULTS ARE GIVEN HERE. The information given in the tables is organized as follows:

TYPE	Symbols that refers to the active device and mount. A complete description of the symbols are given below. These symbols is also used in Figure 1.1.
N	Multiplication factor, i.e. Doubler = X2, Tripler = X3, Quadrupler = X4 etc.
MOUNT	Type of mount used. W/G = Waveguide, MIC = Microwave Integrated Circuit, MMIC = Monolithic Microwave Integrated Circuit, COAX = Coaxial Line, GRID = Planar grid.
NUMBER OF DEVICES	The number of active devices used in the circuit. Also circuit configuration (series, balanced etc.) is noted where appropriate.
OUTPUT FREQUENCY	Output frequency range over which power was measured.
MAXIMUM OUTPUT POWER	The maximum output power measured over the OUTPUT FREQUENCY band. Also given are the efficiency and frequency at which maximum power was recorded.
MAXIMUM EFFICIENCY	The maximum multiplier efficiency measured over the OUTPUT FREQUENCY band. Also give are the output power and frequency at which maximum efficiency was recorded.
REFERENCE NUMBER	A serial number assigned to the frequency multiplier. A serial list of references appear at the end of this Appendix.
REFERENCE	The literature reference where the performance information was acquired.

The various multiplier configurations included in this summary and their corresponding symbols are given below:

B	Whisker-contacted BIN diode across output waveguide.
F	FET in a microwave integrated circuit (MIC) or monolithic circuit (MMIC).
Fb	Balanced pair of FETs in a microwave integrated circuit (MIC) or monolithic circuit (MMIC).
G	Grid or two-dimensional matrix of planar abrupt-junction Schottky diodes.
H	Whisker-contacted hyper-abrupt junction Schottky diodes across output waveguide.
I	Epitaxially-stacked P-N varactor diodes mounted across waveguide (ISIS).
M	Abrupt-junction planar Schottky diode in a planar microwave integrated circuit (MIC).
Mb	Balanced abrupt-junction planar Schottky diode pairs in a planar microwave integrated circuit (MIC).
MM	Abrupt-junction Schottky diode incorporated into a monolithic microwave integrated circuit (MMIC).
MMb	Balanced abrupt-junction Schottky diode pairs incorporated into a monolithic microwave integrated circuit (MMIC).
NL	Non-linear transmission line
P	Planar abrupt-junction Schottky diode across output waveguide.
Pb	Balanced pair of planar abrupt-junction diodes across output waveguide.
Q	Whisker-contacted quantum well diode across output waveguide.
Qc	Whisker-contacted quantum-well diode in a coaxial mount.
S	Whisker-contacted abrupt-junction Schottky diode across output waveguide.
Sb	Balanced pair of whisker-contacted abrupt-junction Schottky diodes across output waveguide.
ST	Planar Soliton

B.1 Abrupt-Junction Schottky Diode

The metal-semiconductor (Schottky-barrier) contact forms the central part of this popular two-terminal device. Donor-doped Gallium Arsenide (GaAs) is the semiconductor material of choice for diodes designed for operation above 50 GHz since the electron mobility for GaAs is large compared with that of silicon. The semiconductor wafer is generally grown using MOCVD or MBE techniques, however the substrate is different depending on the geometry, whisker-contacted versus planar designs. The

term "abrupt-junction" refers to the uniform doping characteristic of the active n^- material, i.e. the material that is in intimate contact with the metal. The Schottky diode can operate as a nonlinear resistance or VARISTOR in forward bias or as a nonlinear reactance or VARACTOR in reverse bias. In practice, a combination of both regimes is commonly employed, but the VARACTOR has a higher theoretical efficiency and is therefore preferred when operating in the millimeter-wave spectrum; however the VARISTOR shows higher efficiency in the sub-millimeter region. See Chapter Three for more details.

The most common structure of the high-frequency Schottky diode is a two-dimensional matrix of over 1000 small-diameter (less than $6\text{ }\mu\text{m}$) anodes, one of which is contacted using a very small wire often referred to by its nostalgic name "cat's-whisker" or simply "whisker" as shown in Figure B.1. The diode and whisker are usually mounted across the output waveguide of the multiplier circuit. With this structure, frequency multiplication up to 800 GHz has been reported. The excellent high-

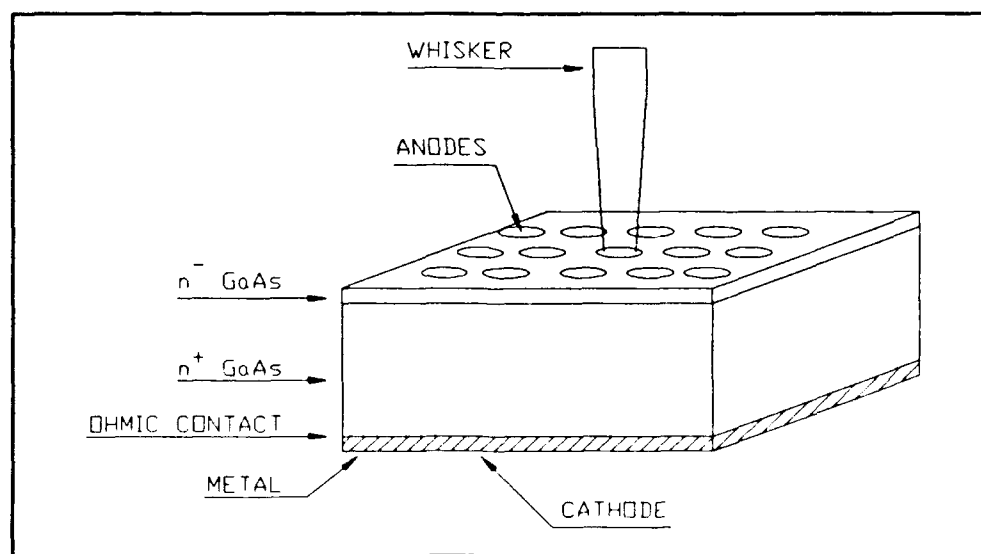


Figure B.1 The abrupt-junction Schottky diode in a classical whisker-contacted structure.

frequency performance is possible due to the structure's inherently low parasitic shunt capacitance, i.e the capacitance between the whisker and the surrounding metal of the mount, and the lower $R_s C_{j0}$ product. Balanced, whisker-contacted diode configurations have demonstrated excellent doubler performance up to 160 GHz. Table B.1 summarizes the state-of-the-art in whisker-contacted Schottky multiplier technology for doublers, triplers, quadruplers, and other higher-order multipliers.

TABLE B.1
STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE
Whisker-Contacted Schottky

TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
S	X2	W/G	1	80 - 116 GHz	11.2 mW 28 % 98 GHz	45 % 2.25 mW 95 GHz	9	Tolmunen 1967
S	X2	W/G	1	85 - 118 GHz	23 mW 12 % 100 GHz	35 % 3.5 mW 98 GHz	6b	Archer 1985
S	X2	W/G	1	110 - 170 GHz	17 mW 21 % 145 GHz	-	28a	Archer 1981
S	X2	W/G	1	110 - 170 GHz	12 mW 15 % 115 GHz	-	28b	Archer 1981
S	X2	W/G	1	170 - 260 GHz	22 mW 27 % 220 GHz	-	28c	Archer 1981
S	X2	W/G	1	190 - 220 GHz	400 uW 2 % 200 GHz	-	8a	Rothermal 1989
S	X2	W/G	1	200 GHz	6 mW	-	42a	Zimmermann 1990
S	X2	W/G	1	200 - 230 GHz	2 mW 20 % 200 GHz	-	16a	Schneider 1981
S	X2	W/G	1	268 GHz	5.5 mW 7.5 % 268 GHz	-	29a	Erickson 1981
S	X2	W/G	1	280 GHz	5 mW	-	42b	Zimmermann 1990

TABLE B.1
STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE
Whisker-Contacted Schottky

TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
S	X2	W/G	1	300 GHz	436 uW 8.5 % 300 GHz	-	22a	Takada 1978
S	X2	W/G	1	332 GHz	4 mW 20 % 332 GHz	-	5b	Erickson 1990
S	X2	W/G	1	570 GHz	700 uW 7 % 570 GHz	-	30	Erickson 1982
S	X2	W/G	1	587 GHz	50 uW 0.1 % 587 GHz	-	4	Frerking 1983b
Sb	X2	W/G	2 BAL TEE	85 - 118 GHz	23 mW 12 % 100 GHz	35 % 3.5 mW 98 GHz	6a	Archer 1985
Sb	X2	W/G	2 BAL	158 - 166 GHz	26 mW 22 % 158 GHz	35 % 12 mW 158 GHz	5a	Erickson 1990
S	X3	W/G	1	99 - 117 GHz	6 mW 15 % 107 GHz	28 % 1.4 mW 107 GHz	10	Tolmunen 1987
S	X3	W/G	1	195 - 235 GHz	-	10.5 % 3.15 mW 232 GHz	24	Erickson 1982
S	X3	W/G	1	200 - 240 GHz	6 mW 7.5 % 220 GHz	-	28d	Archer 1981
S	X3	W/G	1	200 - 280 GHz	4.5 mW 5.6 % 265 GHz	-	19a	Archer 1984
S	X3	W/G	1	200 - 290 GHz	4.5 mW 8.5 % 235 GHz	-	21	Archer 1984
S	X3	W/G	1	203.3 GHz	2 mW 3.3 % 203 GHz	-	3	Frerking 1983a
S	X3	W/G	1	210 - 270 GHz Fix Tune	758 uW 2.52 % 225 GHz	3.31 % 497 uW 225 GHz	53	Millitech 1991
S	X3	W/G	1	260 - 350 GHz	2.5 mW 3.1 % 340 GHz	-	19b	Archer 1984
S	X3	W/G	1	265 - 285 GHz	10 uW 0.1 % 270 GHz	-	8b	Rothermel 1989

TABLE B.1
STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE
Whisker-Contacted Schottky

TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
S	X3	W/G	1	280 GHz	3 mW	-	42c	Zimmermann 1990
S	X3	W/G	1	300 - 345 GHz	30 uW 0.3 % 300 GHz	-	16b	Schneider 1981
S	X3	W/G	1	300 - 350 GHz	1.5 mW 0.75 % 303 GHz	-	29b	Erickson 1981
S	X3	W/G	1	340 GHz	3 mW	-	42d	Zimmermann 1990
S	X3	W/G	1	400 - 460 GHz	10 uW 0.1 % 400 GHz	-	16c	Schneider 1981
S	X3	W/G	1	440 - 460 GHz	126 uW 1.6 % 447 GHz	-	20a	Takada 1979
S	X3	W/G	1	450 GHz	75.8 uW 1.1 % 450 GHz	-	22b	Takada 1978
S	X3	W/G	1	474 - 498 GHz	700 uW 3 % 474 GHz	-	5c	Erickson 1990
S	X3	W/G	1	789 - 807 GHz	110 uW 0.85 % 803 GHz	0.85 % 110 uW 803 GHz	43	Rydberg 1991
S	X4	W/G	1	140 - 155 GHz	2.5 mW 6 % 150 GHz	11.3 % 1.13 mW 148 GHz	11	Tolmunen 1987
S	X4	W/G	1	324 - 370 GHz	1.33 mW 5.9 % 370 GHz	7.6 % 950 uW 348 GHz	27	Millitech 1990
S	X4	W/G	1	340 GHz	300 uW	-	42e	Zimmermann 1990
S	X4	W/G	1	480 GHz	1.2 mW	-	42f	Zimmermann 1990
S	X4	W/G	1	589 - 603 GHz	1.58 uW 0.0125 % 589 GHz	-	20b	Takada 1979
S	X5	W/G	1	160 - 175 GHz	1.28 mW 3.2 % 167 GHz	4.2 % 420 uW 168 GHz	32	Tolmunen 1989
S	X5	W/G	1	490 GHz	200 uW	-	42g	Zimmermann 1990

TABLE B.1 STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE Whisker-Contacted Schottky								
TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
S	X5	W/G	1	570 GHz	65 uW	-	42j	Zimmermann 1990
S	X6	W/G	1	490 GHz	150 uW	-	42h	Zimmerman 1990
S	X6	W/G	1	620 GHz	50 uW	-	42L	Zimmermann 1990
S	X2X3	W/G	1	540 GHz	300 uW	-	42i	Zimmermann 1990
S	X2X3	W/G	1	620 GHz	250 uW	-	42k	Zimmermann 1990
S	X2X4	W/G	1	730 GHz	30 uW	-	42m	Zimmermann 1990

The lack of mechanical ruggedness associated with the whisker-contact has driven researchers to find a planar equivalent for the whisker/diode structure. As a result, a number of planar Schottky diode designs have emerged over the past decade. As shown in Figure B.2, the planar diode consists of a single anode connected to a bonding pad via a very thin metal finger or conductive bridge. To reduce unwanted parasitic shunt capacitance associated with this finger, techniques such as mesa structures, surface channels, and proton irradiation have been employed with various degrees of success. The cathode or ohmic contact, which itself forms the second bonding pad, partially surrounds the anode thus reducing the series resistance. Frequency multiplication using discrete planar Schottky diodes across a waveguide and in planar MIC structures has been reported at frequencies up to 300 GHz. Even higher frequency operation is expected in the near future because of a substrate removal processes currently being explored. The semi-

insulating GaAs substrate is removed and replaced by a lower dielectric material such as quartz (Bishop, 1990). The quartz-backed diodes can then mounted into the multiplier circuit and if

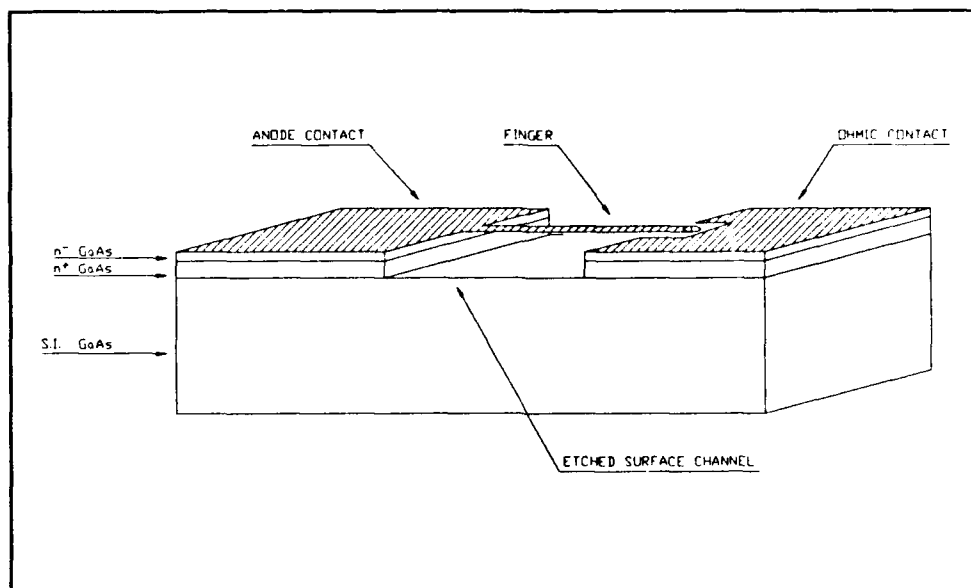


Figure B.2 One of many planar Schottky diode structures in use today.

desired, the quartz can be easily removed thus forming a membrane-type structure. Although higher frequency operation is expected from such a structure, heating problems are anticipated.

GaAs Schottky diodes have been incorporated into completely monolithic (MMIC) designs in which the diode and associated linear circuitry are fabricated together on a single GaAs chip. Operation of tunerless MMIC multipliers up to 250 GHz have been reported (this work). Furthermore, a two-dimensional grid of planar Schottky diodes has yielded excellent performance as a doubler to 66 GHz; clearly demonstrating practical quasi-optical combining techniques. Monolithic technology can be used to scale such grids to higher frequencies. Although low fabrication yields may slow the development of this

technology, operation above 100 GHz should be possible in the near future. Table B.2 summarizes the state-of-the-art in planar Schottky diode multiplier technology.

TABLE B.2
STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE
Planar Schottky

TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
Pb	X2	W/G	2 BAL	50 - 80 GHz	790 μ W 8 % 64 GHz	-	14a	Hu 1986
Pb	X2	W/G	2 BAL	80 - 100 GHz	1.25 mW 12.5 % 88 GHz	-	14b	Hu 1986
Pb	X2	W/G	2 BAL	200 GHz	10 mW 4.2 % 200 GHz	4.3 % 7.74 mW 200 GHz	26a	Cohen 1975
Pb	X2	W/G	2 BAL	200 GHz	10 mW 11 % 200 GHz	12.4 % 8.06 mW 200 GHz	26b	Cohen 1975
Pb	X2	W/G	2 BAL	200 GHz	18 mW 12 % 200 GHz	-	31a	Calviello 1979
Pb	X3	W/G	2 BAL	35 - 60 GHz	1 mW 10 % 45 GHz	-	14c	Hu 1986
Pb	X3	W/G	2 BAL	105 GHz	18 mW 25 % 105 GHz	-	31b	Calviello 1979
P	X3	W/G	1	219 - 243 GHz	3.72 mW 4.13 % 219 GHz	4.2 % 3.3 mW 219 GHz	45	Bradley 1991
Pb	X3	W/G	2 BAL	300 GHz	2 mW 2 % 300 GHz	-	31c	Calviello 1979
Mb	X2	MIC	2 SER BAL	6 - 20 GHz Broadband	10 mW 10 % 18 GHz	-	49	Bitzer 1991
Mb	X2	MIC	2 BAL	18 - 26 GHz	6 mW 8 % 18 GHz	12 % 2.4 mW 18 GHz	35	Kohler 1978
Mb	X2	MIC	2 BAL	26 GHz	6.16 mW 7.7 % 26 GHz	-	15	Ogawa 1987
Mb	X2	MIC	2 BAL	66 - 94 GHz	5 mW 5.6 % 85 GHz	-	25	Nguyen 1987

TABLE B.2
STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE
Planar Schottky

TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
M	X2	MIC	1	90 - 93 GHz	63 mW 7.9 % 92 GHz	-	23	Tahim 1987
M	X2	MIC	1	91 - 93 GHz	28 mW 17.6 % 92 GHz	-	40	Tahim 1988
M	X3	MIC	1	44 - 51 GHz	15.8 mW 7.9 % 47 GHz	-	33	Hindson 1987
Mb	X3	MIC	2 BAL	60 GHz	7.94 mW 2.5 % 60 GHz	-	17	Albin 1988
MM	X2	MMIC	1	24 - 29 GHz	43 mW 20 % 25.8 GHz	24 % 25 mW 26 GHz	12	Chu 1983
MM	X2	MMIC	2 SERIES	24 - 37 GHz	300 mW 18 % 24.8 GHz	35 % 100 mW 36.9 GHz	13	Chu 1984
MM	X2	MMIC	2 SERIES	92 - 95 GHz	22 mW 11 % 93 GHz	12 % 200 mW 93 GHz	51	Hegazi 1991
MMb	X2	MMIC	2 BAL	140 GHz	0.63 mW 1.0 % 142 GHz	1.0 % 0.63 mW 142 GHz	55	Bradley 1991
MMb	X3	MMIC	2 BAL	94 GHz	29.3 mW 4.6 % 91.8 GHz	4.7 % 23.3 mW 91.8 GHz	54	Bradley 1991
MMb	X3	MMIC	2 BAL	240 GHz	0.1 mW 0.1 % 225 GHz	0.1 % 0.1 mW 225 GHz	56	Bradley 1991
MMb	X4	MMIC	2 Series	42 - 46 GHz	1 mW 1 % 44.5 GHz	-	50	Creamer 1991
G	X2	GRID	760	66 GHz	500 mW 7.7 % 66 GHz	280 mW 9.5 % 66 GHz	18	Jou 1988

B.2 Other Diodes

Other two-terminal structures which have demonstrated non-linear behavior suitable for frequency multiplication are the hyper-abrupt

Schottky, the BIN, the ISIS, and the quantum-well or RTD. A summary of the frequency multiplier state-of-the-art using such devices is presented in Table B.3.

The hyper-abrupt junction Schottky diode is similar in structure to the abrupt-junction Schottky with the exception of the n^- layer which is doped in a highly non-uniform but monotonic manner. This diode has a larger capacitance variation as a function of voltage (capacitance ratio) compared with the abrupt-junction diode and hence should translate into more harmonic generating capability. Unfortunately, the series resistance of the undepleted epitaxial layer is larger than for the abrupt-junction Schottky and the result is a lower multiplier conversion efficiency. The hyper-abrupt junction Schottky diode has been tested near 200 GHz.

The BIN or Barrier-Intrinsic- n^+ diode contains a very highly doped yet narrow region which forms a Mott barrier as shown in Figure B.3. When voltage is applied, the depletion region "snaps" from the

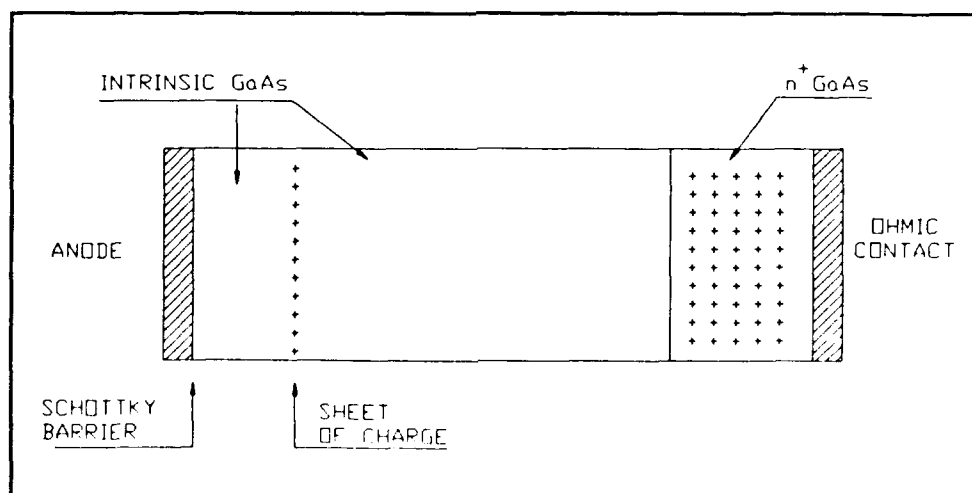


Figure B.3 Barrier-Intrinsic- N^+ diode structure in a whisker-contact geometry.

barrier to the n^+ region thus causing a comparatively large capacitance change, but here again the high resistance of the intrinsic region reduces conversion efficiency. The BIN diode has been tested as a doubler to 95 GHz. Recently, the series resistance of the BIN has been reduced by moderately doping the intrinsic region, however this structure has not yet been tested as a frequency multiplier (Rizzi, 1991). Planar two-dimensional grids of back-to-back BIN diodes yielding a symmetric C-V curve which only generates odd-harmonics have been suggested but have not yet been fabricated (Hwu, 1988).

The idea of stacking varactors was first reported many years ago with very good experimental results at 12 GHz using series-connected, epitaxial GaAs, surface barrier wafers (Irvin, 1966). However, the development of multilayer epitaxial growth techniques with GaAs material to fabricate multi-junction varactor diodes provides a new alternative for millimeter-wave power generation. This epitaxially stacked P-N varactor diode (ISIS - Integrated Series IMPATT Structure), shown in Figure B.4, has proven operation with high conversion efficiency and significantly higher power than single junction devices in the millimeter-wave region up to 100 GHz. However, due to the low hole mobility of the p^+ layers, the efficiency of the ISIS drops quickly above 100 GHz. Because of the high power-handling capacity, there are heat dissipation problems with the ISIS despite the high conversion efficiency. The ISIS has not yet been fabricated in a planar geometry, although commercial waveguide units are available from 23 to 94 GHz (Steinbrecher, 1991).

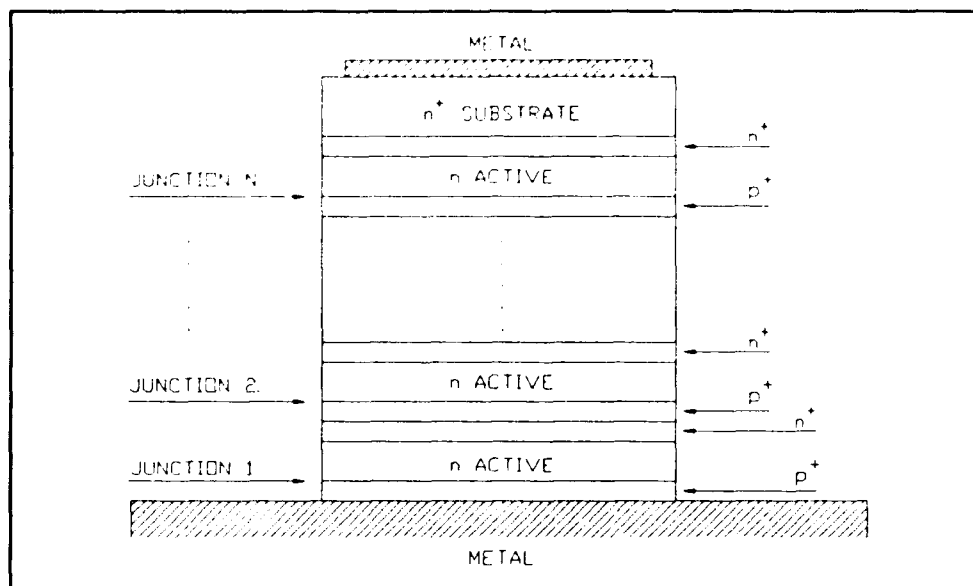


Figure B.4 The epitaxially stacked P-N ISIS structure.

The negative-resistance of the quantum-well or RTD device has been exploited for fundamental millimeter-wave oscillation, see Appendix A. However, the quantum-well structure is a doubler-barrier device which exhibits a polarity-symmetric negative-resistance region that is not limited by the $1/N^2$ multiplier efficiency relationship of conventional VARISTOR devices. The basic quantum-well structure is shown in Figure B.5. Due to the symmetry of the I-V profile, only odd-harmonic are generated. This device, in a whisker-contacted orientation, has been demonstrated as a tripler up to 280 GHz; however output power and efficiency is generally low compared with Schottky diodes. A variation of the quantum-well diode which is basically a high electron mobility varactor (HEMVAR) is currently being developed. Theoretically, this device should yield a better conversion efficiency but experimental multiplier results are pending (Peatman, 1991).

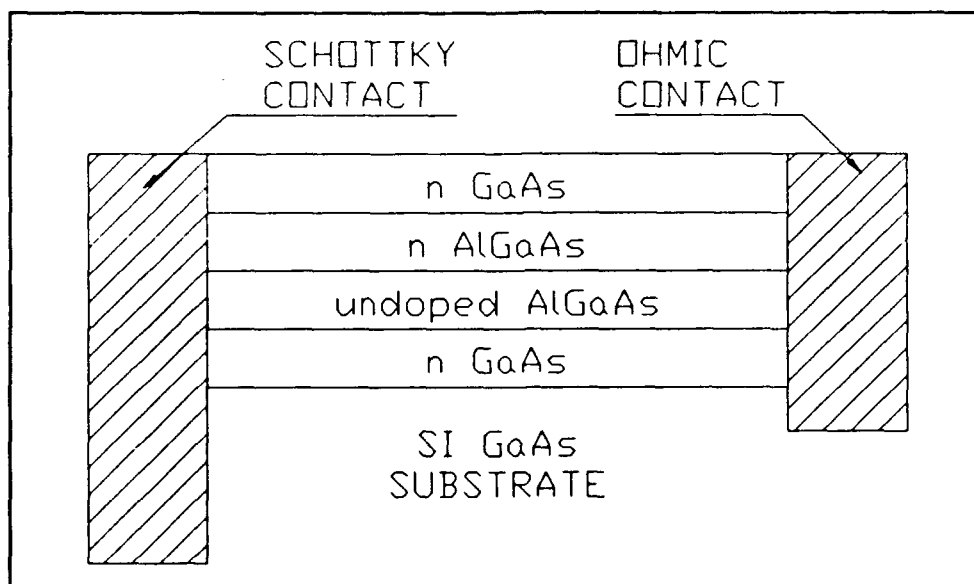


Figure B.5 The quantum-well structure shown in the whisker-contact geometry.

TABLE B.3 STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE Special Two-Terminal Devices								
TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
H	X2	W/G WHISKER	1	220 - 230 GHz	10 mW 20 % 210 GHz	-	46	Lundien 1982
B	X2	W/G WHISKER	1	95 GHz	-	14.7 %	37	Jou 1987
I	X2	W/G	1	22 GHz	7.3 W 50 % 22 GHz	-	7a	Staecker 1987
I	X2	W/G	1	35 GHz	5.5 W 60 % 35 GHz	60 % 5.5 W 35 GHz	7b	Staecker 1987
I	X2	W/G	2 Stacked	44 GHz	5 W 50 % 44 GHz	-	7c	Staecker 1987
I	X2	W/G	2 Stacked	88 GHz	280 mW 14 % 88 GHz	-	7d	Staecker 1987

TABLE B.3
STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE
Special Two-Terminal Devices

TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
I	X2	W/G	2 Stacked	94 GHz	316 mW 16 % 94 GHz	-	52a	Steinbrecher 1991
I	X3	W/G	4 Stacked	12 GHz	1 W 50 % 12 GHz	74 % 234 mW 12 GHz	48	Irvin 1966
I	X4	W/G	2 Stacker	46 GHz	500 mW 10 % 46 GHz	-	52b	Steinbrecher 1991
Q	X3	W/G Whisker	1	191 GHz	250 uW 0.61 % 191 GHz	0.61 % 250 uW 191 GHz	2	Batelaan 1987
Q	X3	W/G Whisker	1	210 - 282 GHz	1.2 mW 5 % 225 GHz	5 % 1.2 mW 225 GHz	34	Rydberg 1990
Q	X3	W/G Whisker	1	240 - 260 GHz	800 uW 1.2 % 249 GHz	1.2 % 800 uW 249 GHz	1	Rydberg 1989
Qc	X5	Coax Whisker	1	21 GHz	16 uW 0.5 % 21 GHz	-	47	Sollner 1988

B.3 Field-Effect Transistors (FET)

Recently, MESFETs and HEMTs have been used for millimeter-wave frequency multiplication in MIC and MMIC designs. The highest reported operating frequency is 180 GHz, however efficiencies have been under 15 percent. This state-of-the-art in FET multiplier technology is presented in Table B.4.

TABLE B.4 STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE FET								
TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
F	X2	MIC	1	39 - 41 GHz	20 mW 12.6 % 40 GHz	-	36	Boch 1989
Fb	X2	MMIC	2 BAL	94 GHz	4 mW 5.5 % 94 GHz	-	39	Geddes 1987
F	X2	MMIC	1	180 GHz	630 uW 10 % 180 GHz	-	44	Kwon 1991

B.4 Distributed Element Structures

Planar nonlinear lines have been recently demonstrated as millimeter-wave harmonic generators up to 110 GHz. This idea has been taken a step further by generating solitons on the line through a complex interaction of the line dispersion and the nonlinearity of the Schottky diodes spaced along the line. The soliton multiplier has been demonstrated up to 40 GHz. Table B.5 summarizes the state-of-the-art for such nonlinear transmission line structures.

TABLE B.5 STATE-OF-THE-ART FREQUENCY MULTIPLIER PERFORMANCE Distributed Element Structures								
TYPE	N	MOUNT	NUMBER OF DEVICES	OUTPUT FREQUENCY	MAXIMUM OUTPUT POWER	MAXIMUM EFF.	REF. NUM.	REFERENCE
ST	X2	Planar	-	26 - 40 GHz	16 mW 16 % 34 GHz	-	41	Carman 1991
NL	X2	Planar	-	100 - 110 GHz	2 mW 12.6 % 110 GHz	-	38	Marsland 1990

State-of-the-Art Frequency Multiplier Survey

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Update: 11/15/91

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APPENDIX C

Detailed Analysis of Schottky Frequency Multipliers

C.1 Generalized Schottky Varactor Theory

Beginning with a generalized impurity profile, Poisson's equation is applied thus yielding charge-voltage and capacitance-voltage relationships. The avalanche breakdown model is applied to determine the epitaxial layer thickness and capacitance limits. Components of the series resistance are also investigated. The Schottky-barrier junction diode equivalent circuit and characteristic equation are developed from knowledge of the physical properties.

C.1.1 Relationships for Charge, Capacitance, and Voltage

The impurity profile used in the generalized Schottky-barrier junction diodes is described by:

$$N_d(x) = N_d x^m \quad (C-1)$$

where $N_d(x)$ is the impurity concentration as a function of distance x into the semiconductor, N_d is the impurity concentration at the characteristic distance ℓ_n from the metal, and m is related to the shape of the doping profile, with $m = 1$ for linearly-graded junctions, $m = 0$ for abrupt junctions, and $m < 0$ for hyper-abrupt junctions. Fig. 3.1 is a sketch of the metal-semiconductor junction showing the active and buffer layer profiles. In the depletion region, the ionized donor atoms have a positive charge, which induces a negative charge on the metal.

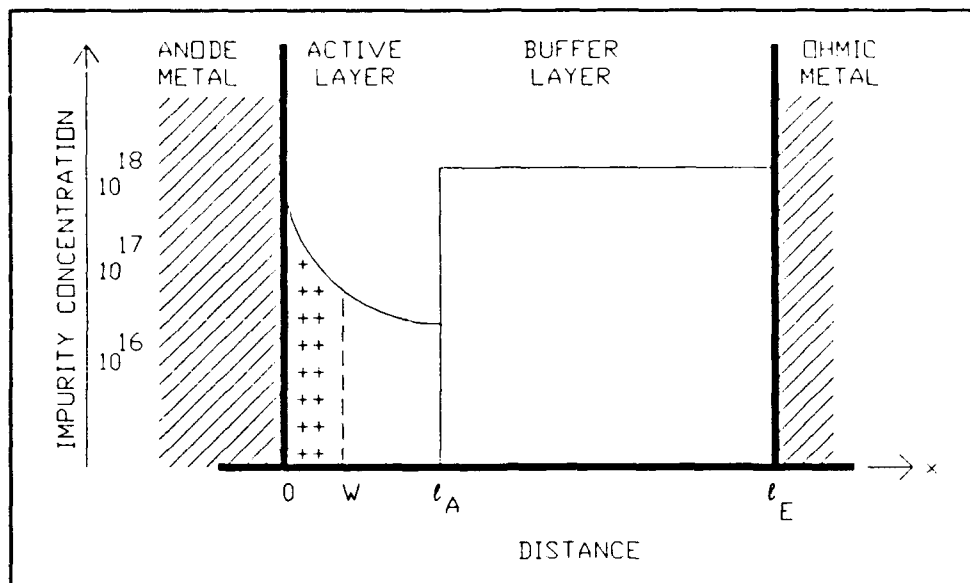


Figure C.1 Sketch of the abrupt-junction diode epitaxial structure.

Note that w is the width of the depletion region, l_a is the distance of the buffer/active layer interface from the metal at $x = 0$, and l_e is the buffer/substrate interface distance.

The electric field distribution can be easily found by assuming a one-dimensional geometry and applying Poisson's equation to the profile

$$-\nabla^2 V = \frac{\partial \mathcal{E}}{\partial x} = \frac{qN_d x^m}{\epsilon_s} \quad (C-2)$$

where V is the electrostatic potential, $\mathcal{E}$ is the electric field, q is the unit charge, and ϵ_s is the permittivity of the semiconductor. The validity of the one-dimensional assumption is assessed by examining the typical device layer thickness. The active layer thickness is about 0.5 microns which is a factor of ten smaller than the varactor anode diameter which is usually greater than 5 microns, hence the one-dimensional assumption is valid. The electric field can be determined by integration of the charge

over the depletion region. A Gaussian surface was chosen such that one side is positioned at $x = w$ and the other side at x . The flux through the surface appears only at x , such that

$$\mathcal{E}(x) = \int_w^x \frac{qN_d}{\epsilon_s} x^m dx = \frac{qN_d}{\epsilon_s(m+1)} [x^{m+1} - w^{m+1}] \quad (C-3)$$

Note that the zero field point is taken to be $x = w$, and the maximum occurs at $x = 0$.

Integration of eqn. (C-3) will yield the potential distribution as

$$V(x) = - \int_0^x \mathcal{E}(x) dx = - \int_0^x \frac{qN_d}{\epsilon_s(m+1)} [x^{m+1} - w^{m+1}] \quad (C-4)$$

To determine the potential at the edge of the depletion region, the integration in eqn. (C-4) is carried out from the metal-semiconductor junction to w :

$$V(w) = \frac{qN_d w^{m+2}}{\epsilon_s(m+2)} \equiv V_{bi} + V_j(t) \quad (C-5)$$

Here, V_{bi} is the built-in potential of the junction from thermionic emission theory and $V_j(t)$ is the applied voltage across the junction. Solving for the dynamic depletion region width $w(t)$ yields

$$w(t) = \left[\frac{(V_{bi} + V_j(t)) \epsilon_s(m+2)}{qN_d} \right]^{\frac{1}{m+2}} \quad (C-6)$$

The total charge Q in the depletion region can be found by integrating the impurity concentration (assuming 100% ionization in the region):

$$Q = \int_0^w qN_d x^m dx = qN_d \frac{w^{m+1}}{m+1} \quad (C-7)$$

Substitution of eqn (C-6) into eqn (C-7) yields the CHARGE-VOLTAGE

relationship:

$$Q(t) = \frac{qN_d}{m+1} \left[\frac{e_s^{(m+2)} (V_{bi} + V_j(t))}{qN_d} \right]^{\frac{m+1}{m+2}} \quad (C-8)$$

The incremental capacitance per unit area as a function of the applied voltage is found by taking the partial derivative of eqn. (C-8) with respect to the applied voltage. After simplification, the CAPACITANCE-VOLTAGE relation becomes

$$C_j(t) = \left[\frac{qN_d e_s^{m+1}}{(m+2) (V_{bi} + V_j(t))} \right]^{\frac{1}{m+2}} \quad (C-9)$$

The ELASTANCE $S(t)$ is defined as the reciprocal of the dynamic junction capacitance as follows:

$$S(t) \equiv \frac{1}{C_j(t)} = \left[\frac{(m+2) (V_{bi} + V_j(t))}{qN_d e_s^{m+1}} \right]^{\frac{1}{m+2}} \quad (C-10)$$

Finally, solving eqn. (C-8) for $V_{bi} + V_j(t)$ and substituting into eqn (C-10) yields the desired ELASTANCE-CHARGE relationship as

$$S(t) = \frac{1}{e_s} \left[\frac{Q(t) (m+1)}{qN_d} \right]^{\frac{1}{m+1}} \quad (C-11)$$

Note that in general, the elastance-charge relationship is nonlinear.

C.1.2 Maximum Voltage Swing

The Schottky-barrier diode varactor regime is bounded by three important conditions. The maximum positive voltage is limited by the diode forward turn-on point, which is directly related to the built-in potential V_{bi} derived from thermionic-emission theory. Maximum reverse voltage is limited by avalanche breakdown and depletion-layer punch through into the buffer layer.

Based on the work of Sze and Gibbons (Sze, 1966), the criterion for ionization is as follows:

$$\int_0^w \alpha_n \text{Exp}[-\int_0^w (\alpha_n - \alpha_p) dx'] dx = 1 \quad (\text{C-12})$$

where α_n and α_p are the ionization rates of electrons and holes respectively and w is the depth of the depletion region. Eqn. (C-14) is known as the ionization integral and for GaAs, α_n and α_p are equal:

$$\alpha_n = \alpha_p = a \text{Exp}[-(\frac{b}{\mathcal{E}(x)})^{m'}] \quad (\text{C-13})$$

For both electrons and holes in GaAs, $a = 3.5 \times 10^5$, $b = 6.85 \times 10^5$, and $m' = 2$. Substitution of the electric field distribution as given in eqn. (C-3) yields the avalanche breakdown criterion for the generalized impurity profile:

$$\int_0^w a \text{Exp}[-(\frac{e_s(m+1)b}{qN_d(x^{m+1} - w^{m+1})})^{m'}] dx = 1 \quad (\text{C-14})$$

Punch-through occurs when the depletion region crosses the active/buffer layer interface. If the active layer thickness is chosen such that punch-through and avalanche breakdown occurs at the same applied voltage, then the maximum possible voltage swing will be attained. Thus, the active layer thickness is determined by calculation of the depletion region width at the point of avalanche breakdown.

C.1.3 Series Resistance

The series resistance of the Schottky diode consists of three component parts: undepleted epitaxial-layer resistance, substrate

resistance, and ohmic contact resistance. In the following analysis, high frequency effects such as displacement current and carrier inertia are not considered.

For the analysis of the undepleted epitaxial-layer series resistance R_s , the resistive region of interest lies between the depletion region edge and the active/buffer region interface at $x = \ell_a$ (see Fig. C.1). Assuming a one-dimensional model with constant cross-sectional area, the undepleted epitaxial-layer resistance for a generalized impurity profile is as follows:

$$R_s = \frac{1}{A_a q} \int_0^{\ell_a} \frac{1}{\mu_e(x) N_d(x)} dx \quad (C-15)$$

where A_a is the anode cross-sectional area, $\mu_e(x)$ is the electron mobility, and $N_d(x)$ is the impurity concentration as described in eqn. (C-1). An empirical formula for the carrier mobility was taken from Sze (1985):

$$\mu_e(x) = \frac{10^4}{1 + \frac{\sqrt{N_d}}{10^{\frac{17}{2}}} x^{\frac{m}{2}}} \quad (C-16)$$

Substitution of eqns. (C-1) and (C-16) into eqn. (C-15) gives:

$$R_s = \frac{1}{A_a q} \int_0^{\ell_a} \frac{1}{\frac{10^{14}}{1 + \frac{\sqrt{N_d}}{10^{\frac{17}{2}}} x^{\frac{m}{2}}} N_d x^m} dx \quad (C-17)$$

Carrying out the integration yields (after simplification):

$$R_s = \frac{1}{A_a q N_d} \left[\frac{\ell_a^{1-m}}{1-m} + \frac{N_d^{\frac{1}{2}}}{10^{\frac{17}{2}}} \frac{\ell_a^{1-\frac{m}{2}}}{1-\frac{m}{2}} - \frac{w^{1-m}}{1-m} - \frac{N_d^{\frac{1}{2}}}{10^{\frac{17}{2}}} \frac{w^{1-\frac{m}{2}}}{1-\frac{m}{2}} \right] \quad (C-18)$$

Finally, substitution of eqn. (C-6) into eqn. (C-18) yields the functional dependence of the undepleted epitaxial resistance as

$$R_s(t) = \frac{1}{A_s q N_d} \left[\frac{1}{1-m} \left[\ell_s^{1-m} - \left(\frac{e_s(m+2)(V_j(t) + V_{bi})}{q N_d} \right)^{\frac{1-m}{m+2}} \right] \right. \\ \left. + \frac{N_d^{\frac{1}{2}}}{10^{\frac{17}{2}} (1-\frac{m}{2})} \left[\ell_s^{1-\frac{m}{2}} - \left(\frac{e_s(m+2)(V_j(t) + V_{bi})}{q N_d} \right)^{\frac{1-\frac{m}{2}}{m+2}} \right] \right] \quad (C-19)$$

which is a function of the applied voltage. As will be shown in Chapters 5, 6, and 7, this epitaxial resistance is small compared with reactance of the nonlinear capacitance, hence nonlinear effects resulting from this resistance is ignored, and the maximum epitaxial resistance is used in the equation for total series resistance.

The skin effect is important in the analysis of the buffer layer resistance R_b . The skin depth, δ_b , is defined as follows:

$$\delta_b = \left[\frac{2}{\omega \mu_s \sigma_b} \right]^{\frac{1}{2}} \quad (C-20)$$

where μ_s is the buffer layer permeability, σ_b is the buffer layer conductivity, and ω is the radian frequency. A cross-sectional view of the varactor cylindrical anode geometry is shown in Fig. C.2.

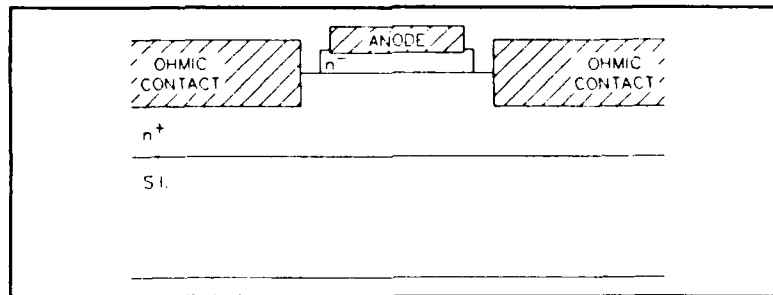


Figure C.2 Cross-sectional view of anode.

The surface resistance which is the substrate resistance for this geometry is therefore (Kelly, 1990):

$$R_b = \left[\frac{1}{2\pi\sigma_b\delta_b} \right] \ln\left(\frac{r_{oc}}{r_a}\right) \quad (C-21)$$

where r_a is the anode radius and r_{oc} is the inner radius of the ohmic contact.

The ohmic contact resistance R_{oc} can easily be 10^{-5} ohm/cm² and for geometries of $< 10^{-3}$ cm², R_{oc} is very small in comparison with the other resistances and hence will be ignored (Kelly, 1980).

The total series resistance is therefore:

$$R_s = R_a + R_b \quad (C-22)$$

C.1.4 Varactor Circuit Model - Time Domain

The active varactor circuit model which does not include parasitic elements is shown in Fig. C.3. This model assumes that the Schottky diode

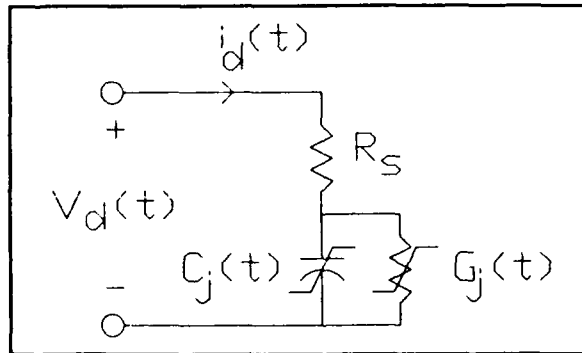


Figure C.3 The active varactor circuit model.

is reverse biased and that the total resultant of the harmonic voltage amplitude will not cause either diode forward turn-on or reverse breakdown, hence, the diode is in the varactor regime and nonlinear resistive effects are neglected.

Applying Kirchhoff's voltage law to the circuit model, the resulting integral equation relates the varactor voltage and current:

$$V_d(t) = \int S(t) i_d(t) dt + R_s i_d(t) \quad (C-23)$$

where $v_d(t)$ is the voltage across the varactor, $i_d(t)$ is the current through the varactor, $S(t)$ is the incremental elastance or inverse dynamic capacitance, and R_s is the total series resistance. Note that the elastance which takes an active part in the time integration, leads directly to the nonlinear behavior of the varactor.

C.1.5 Varactor Circuit Model - Frequency Domain

Let ω_0 be the multiplier input frequency, then disregarding unwanted spurious oscillations and chaotic effects, only commensurate frequencies of the form $k\omega_0$ are present in the voltage, current, and elastance waveforms of frequency multipliers. The goal of this section is to develop a current-voltage relation for each harmonic component.

Consider the varactor mounted in an embedding circuit as shown schematically in Fig. C.4. Following the approach outlined in

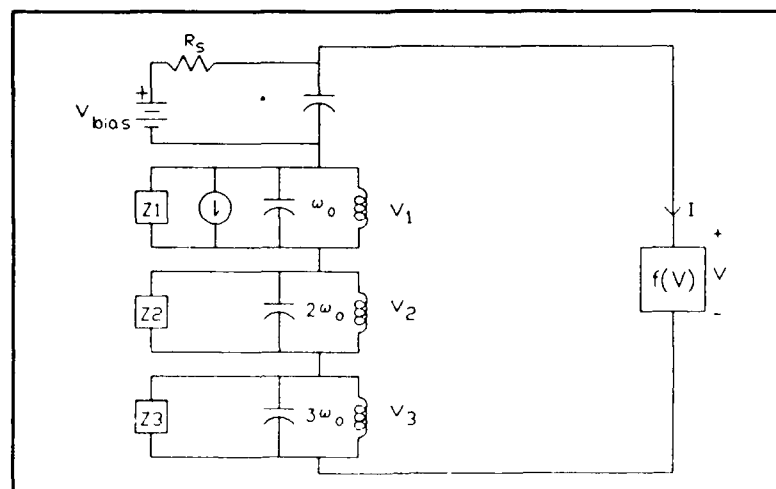


Figure C.4 Schematic of varactor diode in an embedding circuit.

Penfield and Rafuse (Penfield, 1962), the Fourier series representation of the voltage, current, and elastance waveforms are

$$V_d(t) = \sum_{k=-\infty}^{\infty} V_k e^{jk\omega_o t} \quad (C-24)$$

$$i_d(t) = \sum_{k=-\infty}^{\infty} I_k e^{jk\omega_o t} \quad (C-25)$$

$$S(t) = \sum_{k=-\infty}^{\infty} S_k e^{jk\omega_o t} \quad (C-26)$$

Since the above waveforms are real, the Fourier coefficients can be simplified as

$$V_{-k} = V_k^* ; \quad I_{-k} = I_k^* ; \quad S_{-k} = S_k^* \quad (C-27)$$

where * indicates the complex conjugate. Each of the Fourier coefficients are time-averaged values of a time waveform with a phase modifying factor:

$$V_k = \frac{1}{T_o} \int_{-\frac{T_o}{2}}^{\frac{T_o}{2}} V_d(t) e^{-\frac{j2\pi kt}{T_o}} dt = \langle V_d(t) e^{-jk\omega_o t} \rangle \quad (C-28)$$

where $\langle \rangle$ indicates the time-average operation, and T_o is the waveform period. Similarly,

$$I_k = \langle i_d(t) e^{-jk\omega_o t} \rangle \quad (C-29)$$

$$S_k = \langle S(t) e^{-jk\omega_o t} \rangle \quad (C-30)$$

Eqn. (C-23) and then eqns. (C-29) and (C-30) are substituted into eqn. (C-28) to yield

$$\begin{aligned}
V_k &= \langle V_d(t) e^{-jk\omega_o t} \rangle \\
V_k &= \langle R_s i_d(t) e^{-jk\omega_o t} \rangle + \langle \int S(t) i_d(t) e^{-jk\omega_o t} dt \rangle \quad (C-31) \\
V_k &= R_s I_k + \frac{1}{jk\omega_o} \langle S(t) i_d(t) e^{-jk\omega_o t} \rangle
\end{aligned}$$

Now, eqn. (C-25) for the current time-waveform and eqn. (C-26) for the elastance waveform is substituted into eqn. (C-31) yielding

$$\begin{aligned}
V_k &= R_s I_k + \frac{1}{jk\omega_o} \langle \sum_l I_l S(t) e^{jl\omega_o t} e^{-jk\omega_o t} \rangle \\
V_k &= R_s I_k + \frac{1}{jk\omega_o} \sum_l I_l \langle S(t) e^{-j(k-l)\omega_o t} \rangle \quad (C-32) \\
V_k &= R_s I_k + \frac{1}{jk\omega_o} \sum_l I_l S_{k-l}
\end{aligned}$$

where k and l range from $-\infty$ to $+\infty$. Eqn. (C-32) describes the varactor circuit model in the frequency domain. Note that the voltage at harmonic k is related to all harmonics of the current and elastance. In the next section, this equation will be solved for the important case of the abrupt junction.

C.2 Abrupt Junction Varactor Frequency Multiplier Solutions

C.2.1 Modulation Ratios

The characteristic equation of the varactor, eqn. (C-32), will now be solved under the abrupt junction condition of $\mu = 0$, hence eqn. (C-11) can be simplified to

$$S(t) = \frac{1}{qN_d e_s} Q(t) \quad (C-33)$$

where N_d is the impurity concentration of the uniformly-doped active layer. Note that in this case, the elastance is directly proportional to the charge. Eqn. (C-33) is solved for $Q(t)$ and the varactor current becomes

$$i_d(t) = \frac{dQ(t)}{dt} = qN_d e_s \frac{dS(t)}{dt} \quad (C-34)$$

Transforming eqn.(C-34) to the frequency domain gives

$$\begin{aligned} \sum_k I_k e^{jk\omega_o t} &= qN_d e_s \frac{d}{dt} \left[\sum_k S_k e^{jk\omega_o t} \right] \\ &= qN_d e_s (jk\omega_o) \sum_k S_k e^{jk\omega_o t} \end{aligned} \quad (C-35)$$

Since the summations and the corresponding phase factors are identical, the terms inside the summations must be equal for each k , hence

$$I_k = jk\omega_o (qN_d e_s) S_k \quad (C-36)$$

Define the **Complex Modulation Ratio**, M_k , as the normalized harmonic-specific elastance coefficient:

$$M_k = \frac{S_k}{S_{\max} - S_{\min}} \quad (C-37)$$

where $S_{\max}$ is the elastance at reverse breakdown, and $S_{\min}$ is the elastance at forward turn-on. Solving eqn.(C-37) for S_k and then substitution into eqn.(C-36) gives

$$I_k = jk\omega_o (qN_d e_s) M_k (S_{\max} - S_{\min}) \quad (C-38)$$

From eqns.(C-8) and (C-11), the diode voltage is related to the elastance as follows:

$$V_{bi} + V_j(t) = \frac{qN_d e_s}{2} S^2(t) \quad (C-39)$$

The forward turn-on voltage is taken to be the minimum voltage $V_{\min}$ which gives rise to the minimum elastance $S_{\min}$, and the breakdown voltage V_B gives the maximum elastance $S_{\max}$, hence

$$\frac{qN_d e_s}{2} [S_{\max}^2 - S_{\min}^2] = -V_{\min} + V_B \quad (C-40)$$

Expanding the square terms yields

$$qN_d e_s [S_{\max} - S_{\min}] = 2 \frac{V_B - V_{\min}}{S_{\max} + S_{\min}} \quad (C-41)$$

Finally, the eqn.(C-41) can be substituted into eqn.(C-38) to give the current at harmonic k as

$$I_k = 2 \frac{V_B - V_{\min}}{S_{\max} - S_{\min}} j k \omega_o M_k \quad (C-42)$$

Note that M_k is complex (since S_k is complex) resulting in a real current at harmonic k . Similarly, V_k is found by substitution of eqns. (C-37), (C-38) and (C-42) into eqn. (C-32):

$$V_k = R_s I_k + \frac{S_{\max} - S_{\min}}{S_{\max} + S_{\min}} (V_B - V_{\min}) \sum_r M_r M_{k-r} \quad (C-43)$$

Eqns. (C-42) and (C-43) yield the basis for calculation impedances, powers, and efficiency for the varactor multiplier.

C.2.2 Varactor Performance Calculations

Input Resistance

The varactor input impedance at the n^{th} harmonic is found as follows:

$$Z_{in} = \frac{V_n}{I_n} = R_s + \frac{R_s \omega_c}{2 n \omega_o} \frac{\sum_r M_r M_{n-r}}{j M_n} \quad (C-44)$$

where ω_c is the cutoff frequency defined as

$$\omega_c = \frac{S_{\max} - S_{\min}}{R_s} \quad (C-45)$$

Extracting the real part of eqn. (C-44) gives the input resistance:

$$R_{in} = R_s \left[1 + \frac{\omega_c}{2n\omega_o} \operatorname{Re} \left\{ \frac{\sum_r M_r M_{n-r}}{jM_n} \right\} \right] \quad (C-46)$$

Note that under normal frequency multiplier operation, the input harmonic is taken as $n = 1$.

Idler and Output Resistances

If the idler and output circuits are terminated by a tuned embedding impedance Z_k with real part R_k and imaginary part $S_{avg}/k\omega_o$, then V_k is

$$V_k = -[R_k + j \frac{S_{avg}}{k\omega_o}] I_k \quad (C-47)$$

where S_o is the average junction elastance. This equation can then be substituted into eqn. (C-43) to yield

$$0 = (R_k + R_s) I_k + \frac{jS_{avg}I_k}{k\omega_o} + \frac{S_{max} - S_{min}}{S_{max} + S_{min}} (V_B - V_{min}) \sum_r M_r M_{k-r} \quad (C-48)$$

Substituting eqn.(C-42) for I_k yields the desired equation for R_k as

$$R_k = R_s \left[\frac{\omega_c}{2\omega_o} \sum_r \frac{jM_r jM_{k-r}}{jM_k} - 1 \right] \quad (C-49)$$

Input, Idler, and Output Reactance

The varactor reactance at each harmonic simply results from the average of the junction elastance over the voltage range from V_{min} to V_B :

$$X_k = \frac{S_{avg}}{k\omega_o} = \frac{1}{V_B + V_{min}} \int_{V_{min}}^{V_B} \frac{2}{k\omega_o} \left[\frac{(V_{bi} + V_d)}{qn_d \epsilon_s} \right]^{\frac{1}{2}} dV_d \quad (C-50)$$

Input, Output, and Dissipated Power

Consider an arbitrary linear N-port network as shown in Fig. C.5.

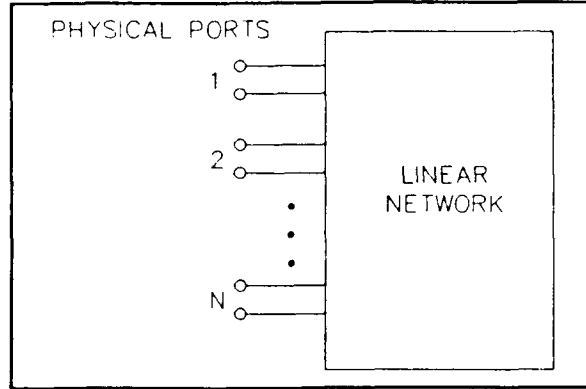


Figure C.5 Schematic of an N-port network.

The input power is found from the voltage and current at each physical port:

$$\begin{aligned} P_{in} &= \mathbf{V}^\dagger \mathbf{I} + \mathbf{I}^\dagger \mathbf{V} \\ &= \mathbf{I}^\dagger (\mathbf{Z} + \mathbf{Z}^\dagger) \mathbf{I} \end{aligned} \quad (\text{C-51})$$

where the $\dagger$ indicates the complex conjugate transpose. However, if the modulation ratios are known, the impedance at each frequency port can be considered individually, i.e each frequency port can now be treated as a linear one-port, hence

$$\begin{aligned} P_{in} &= 2 R_{in} |I_n|^2 \\ &= 8 P_{norm} \left(\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right)^2 \frac{\omega_o^2}{\omega_c^2} n^2 m_n^2 \frac{R_{in}}{R_s} \end{aligned} \quad (\text{C-52})$$

where $m_n = |M_n|$, and P_{norm} is defined as

$$P_{norm} = \frac{(V_B - V_{min})^2}{R_s} \quad (\text{C-53})$$

The output power at $k = L$ can be easily found by replacing R_{in} in eqn.(C-52) by R_{LOAD} . This gives

$$P_{out} = 8 P_{norm} \left[\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right]^2 \frac{\omega_o^2}{\omega_c^2} L^2 m_L^2 \frac{R_{LOAD}}{R_s} \quad (C-54)$$

The dissipated power is simply the difference between the output power of eqn.(C-54) and the input power of eqn.(C-52):

$$P_{diss} = 8 P_{norm} \left[\frac{S_{max} - S_{min}}{S_{max} + S_{min}} \right]^2 \frac{\omega_o^2}{\omega_c^2} \left[\sum_{k=1}^{\infty} k^2 m_k^2 + \sum_{\substack{k=1 \\ k \neq n}}^{\infty} k^2 m_k^2 \frac{R_k}{R_s} \right] \quad (C-55)$$

where the first term is the power dissipated in the series resistance and second term is the power dissipated in all of the external harmonic terminations.

Varactor Efficiency

The varactor efficiency is the ratio of the output power to the input power:

$$\begin{aligned} \eta &= \frac{P_{out}}{P_{in}} = \frac{L^2 m_L^2 R_{LOAD}}{\pi^2} m_n^2 R_{in} \\ &= \frac{L^2 m_L^2 R_{LOAD}}{\sum_{k=1}^{\infty} k^2 m_k^2 (R_k + R_s)} \end{aligned} \quad (C-56)$$

C.3 Conclusions

The above equations (based on the work of Penfield and Rafuse) permit calculation of the input, idler, and output impedance as well as the input and output power levels for a given ABRUPT JUNCTION varactor diode in multiplier circuit, if the modulation ratios are known. Placing constraints on the bias voltage and either the output power or the efficiency are necessary for calculation of the modulation ratios. This procedure is carried out in Chapter II for the doubler and tripler cases.

C.4 MathCAD Routines for Doubler and Tripler Analysis

The remainder of Appendix C contains a listing of the MathCAD routines for calculating doubler and Tripler performance as described in Chapter Two. The routines are based on the Penfield and Rafuse (1962) approach.

APPENDIX D

Geometrical Information for UVA VARACTOR-1 Mask Set

Appendix D contains a summary of the geometrical information about the UVA mask set VARACTOR-1. The set contains five mask plates: Ohmic Contact (level 2), Anodes (level 3), Anode contact (level 4), Surface Channel (level 5), and Miscellaneous (level 8). This set is directly compatible with the MIXER-1 mask set designed by W. Bishop. All unit cell drawings were made using the computer-aided drawing package AutoCAD. Dimensional information for the Ohmic Contact, Anodes, and Anode Contact features is presented here. Sections D.1 and D.2 summarize the rectangular pad and tapered pad geometries respectively.

D.1 Rectangular Contact Pads

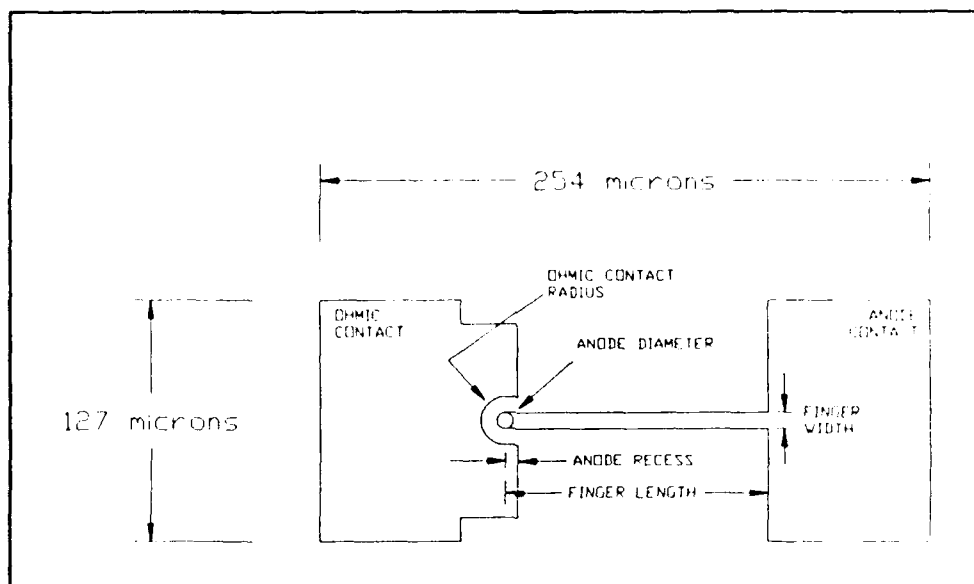


Figure D.1 Sketch of VARACTOR-1 rectangular geometry. Dimensions are given in Table D.1.

TABLE D.1 Dimensional Information Rectangular Contact Pads		
FEATURE	DIMENSION [microns]	UNIT CELLS
OHMIC CONTACT Contact Radius:	12.0	2.9 2.10 2.11 2.12
	15.0	* * *
	ANODE RADIUS:	* *
ANODE Circular: (diameter)	4.0	3.6 3.7 3.8 3.9 3.10
	5.0	* *
	6.0	* *
	9.0	* *
	Ellipse: (major/minor)	3.4 / 1.7 *
ANODE CONTACT Finger length:	25.0	4.7 4.8 4.11 4.12
	50.0	* *
	Finger Width:	3.0 * * *
	Tip Diameter:	5.0 * * *

D.2 Tapered Contact Pads

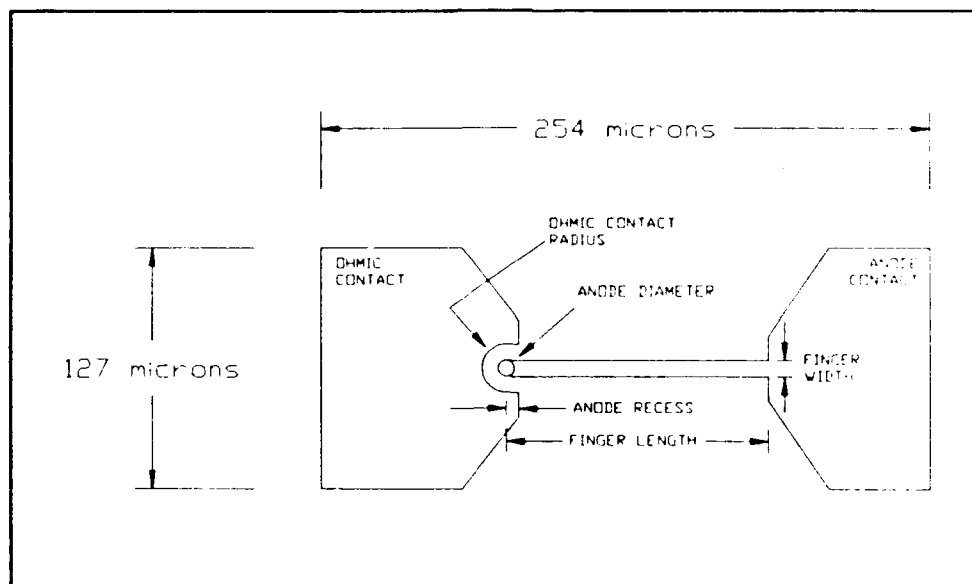


Figure D.2 Sketch of VARACTOR-1 tapered geometry. Dimensions are given in Table D.1.

TABLE D.2 Dimensional Information Tapered Contact Pads		
FEATURE	DIMENSION [microns]	UNIT CELLS
OHMIC CONTACT Contact Radius:	12.0	2.13 2.14 2.15 2.16
	15.0	* * *
	15.0	* * *
Anode Radius:	NONE	* * *
	5.0	* * *
	5.0	* * *
ANODE Circular: (diameter)	4.0	3.6 3.7 3.8 3.9 3.10
	5.0	* * *
	6.0	* * *
	9.0	* * *
Ellipse: (major/minor)	3.4 / 1.7	* * *
ANODE CONTACT Finger length:	13.0	4.9 4.10 4.13 4.14
	25.0	* * *
	25.0	* * *
	25.0	* * *
Finger Width:	3.0	* * *
Tip Diameter:	5.0	* * *

APPENDIX E

Calculations for Planar Transmission Line Parameters and Air Bridge Inductance

Appendix E includes all of the information used in the calculation of CPW, CBCPW, and Slotline parameters as well as the calculation of air bridge inductance. All of the calculations were performed using the computer program MathCAD¹.

¹MathCAD is a product of MathSoft Inc. of Cambridge, MA.

This mathCAD routine calculates the impedance, effective dielectric constant, and conductor and dielectric loss for conventional and metal-backed coplanar waveguide.

Physical parameters of coplanar waveguide:

$$\begin{array}{lll} s := 10, 15 \dots 90 & \epsilon_0 := 8.854 \cdot 10^{-18} & F := 80 \text{ GHz} \\ g := 100 & \epsilon_r := 13 & \rho := 1.42 \text{ for Gold} \\ h := 1000 & \tan \delta := 0.003 & \\ h1 := 10000 & & \lambda_0 := \frac{300}{F} \\ T := 4.0 & u_0 := 4 \cdot \pi \cdot 10^{-13} & \end{array}$$

where:

s: center strip width [microns]
g: ground plane spacing [microns]
h: bottom metal thickness [microns]
h1: metal cover height [microns]
T: metallization thickness [microns]
F: frequency [GHz]

Conductor thickness correction: Gupta, Garg, and Bahl, p. 278

$$DT(s) := \left[1.25 \cdot \frac{T}{\pi} \right] \cdot \left[1 + \ln \left[4 \cdot \pi \cdot \frac{s}{T} \right] \right]$$

$$a(s) := \frac{s}{2} + \frac{DT(s)}{2} \quad b(s) := \frac{g}{2} + \frac{DT(s)}{2}$$

Dielectric & Impedance Equations: Ghione & Naldi, MTT-35, #3, Mar. 87, p. 260

$$k3(s) := \frac{\tanh \left[\frac{\pi \cdot a(s)}{2 \cdot h} \right]}{\tanh \left[\frac{\pi \cdot b(s)}{2 \cdot h} \right]} \quad k4(s) := \frac{\tanh \left[\frac{\pi \cdot a(s)}{2 \cdot h1} \right]}{\tanh \left[\frac{\pi \cdot b(s)}{2 \cdot h1} \right]}$$

$$r(k) := \frac{\pi}{\ln \left[2 \cdot \frac{1 + \left[1 - k^2 \right]^{.25}}{1 - \left[1 - k^2 \right]^{.25}} \right]}$$

$$\epsilon_{\text{eff2}}(s) := 1 + \frac{r(k3(s))}{r(k3(s)) + r(k4(s))} \cdot (\epsilon_r - 1)$$

$$Z_0(s) := \frac{60 \cdot \pi}{\sqrt{\epsilon_{\text{eff2}}(s)}} \cdot \left[\frac{1}{r(k3(s)) + r(k4(s))} \right]$$

 Calculation of conductor loss: Gopinath, MIT-30, #7, July 82, p. 110:
 Polynomial fit to loss constant, fig. 4 of Gopinath

$$c(s) := \frac{s}{g} \quad g_0 := \frac{g}{1000} \quad \rho_s := .00628 \cdot \sqrt{F \cdot \rho}$$

$$k(s) := 15 - 26.5 \cdot c(s) + 46.5 \cdot c(s)^2 - \frac{3.95}{1 - c(s)} + \frac{.233}{(1 - c(s))^2} + \frac{4.89}{c(s)}$$

$$AC(s) := \left[\frac{k(s)}{g_0} \right] \cdot \left[\frac{\rho_s}{Z_0(s)} \right]$$

 Dielectric loss calculation: Gupta, Garg, and Bahl, Eq. 7.33

$$Q(s) := \frac{\epsilon_{\text{eff2}}(s) - 1}{\epsilon_r - 1}$$

$$AD(s) := \frac{27.3 \cdot Q(s) \cdot \epsilon_r \cdot \tan \delta}{\lambda_0 \cdot \sqrt{\epsilon_{\text{eff2}}(s)}}$$

 Guide wavelength calculation

$$\beta(s) := 2 \cdot \pi \cdot F \cdot 10^9 \cdot \frac{\sqrt{\mu_0 \cdot \epsilon_0 \cdot \epsilon_{\text{eff2}}(s)}}{\sqrt{2}} \cdot \sqrt{1 + \tan^2 \delta} + 1$$

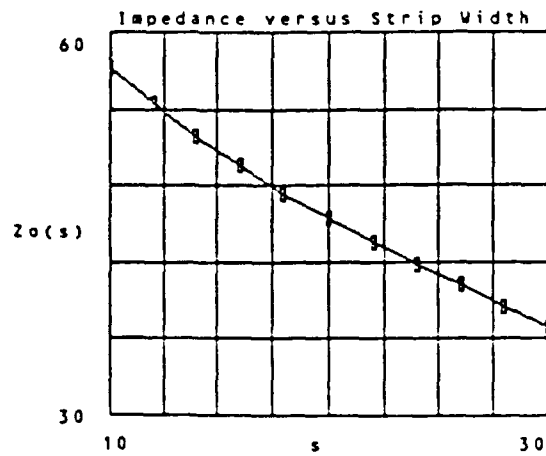
$$\lambda(s) := 2 \cdot \frac{\pi}{\beta(s)}$$

Operating frequency: $F = 31$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	eff2(s)	AC(s)	AD(s)	$\lambda(s)$
10	57.28	7.07	0.40	0.021	3636.74
12	54.39	7.07	0.41	0.021	3635.84
14	51.84	7.08	0.38	0.021	3635.05
16	49.53	7.08	0.36	0.021	3634.33
18	47.42	7.08	0.34	0.021	3633.69
20	45.45	7.09	0.33	0.021	3633.12
22	43.6	7.09	0.33	0.021	3632.61
24	41.84	7.09	0.33	0.021	3632.17
26	40.16	7.09	0.33	0.021	3631.8
28	38.54	7.09	0.34	0.021	3631.5
30	36.95	7.09	0.35	0.021	3631.27

Physical Parameters:

$g = 50$ microns $\epsilon_r = 13$
 $h = 100$ microns $\tan \delta = 0.003$
 $h1 = 1000$ microns $\rho = 1.42$
 $r = 4$ microns $\lambda_0 = 9.68$ mm

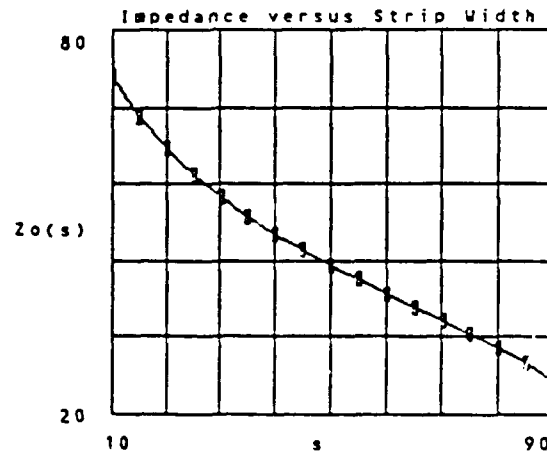


Operating frequency: $F = 31$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	eff2(s)	AC(s)	AD(s)	$\lambda(s)$
10	72.89	7	0.33	0.021	3654.66
15	66.43	7	0.25	0.021	3654.61
20	61.51	7	0.21	0.021	3654.56
25	57.47	7	0.19	0.021	3654.52
30	54.01	7	0.17	0.021	3654.49
35	50.96	7	0.16	0.021	3654.45
40	48.2	7	0.16	0.021	3654.43
45	45.66	7	0.15	0.021	3654.4
50	43.29	7	0.16	0.021	3654.33
55	41.04	7	0.16	0.021	3654.36
60	38.87	7	0.17	0.021	3654.35
65	36.75	7	0.18	0.021	3654.34
70	34.64	7	0.19	0.021	3654.34
75	32.51	7	0.2	0.021	3654.35
80	30.3	7	0.22	0.021	3654.36
85	27.92	7	0.24	0.021	3654.38
90	25.21	7	0.3	0.021	3654.43

Physical Parameters:

$g = 100$ microns $\epsilon_r = 13$
 $h = 1000$ microns $\tan \delta = 0.003$
 $h1 = 10000$ microns $\rho = 1.42$
 $T = 4$ microns $\lambda_0 = 9.68$ mm

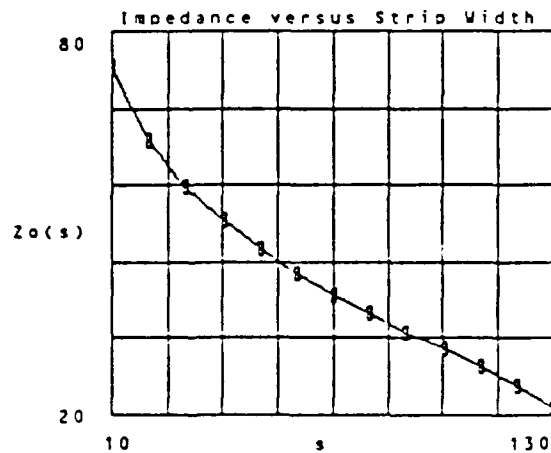


Operating Frequency: $F = 31$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	eff2(s)	AC(s)	AD(s)	$\lambda(s)$
10	74.51	7.3	0.31	0.021	3579.35
20	63.17	7.35	0.2	0.021	3566.76
30	55.37	7.39	0.16	0.022	3557.16
40	50.33	7.42	0.14	0.022	3549.34
50	45.93	7.45	0.13	0.022	3542.89
60	42.15	7.47	0.12	0.022	3537.65
70	38.33	7.49	0.12	0.022	3533.59
80	35.31	7.5	0.13	0.022	3530.74
90	33	7.51	0.14	0.022	3529.2
100	30.29	7.51	0.15	0.022	3529.21
110	27.57	7.5	0.17	0.022	3531.16
120	24.66	7.48	0.19	0.022	3535.99
130	21.11	7.44	0.37	0.022	3546.34

Physical Parameters:

$g = 140$ microns $\epsilon_r = 13$
 $h = 100$ microns $\tan \delta = 0.003$
 $h1 = 1000$ microns $\rho = 1.42$
 $T = 4$ microns $\lambda_0 = 9.68$ mm

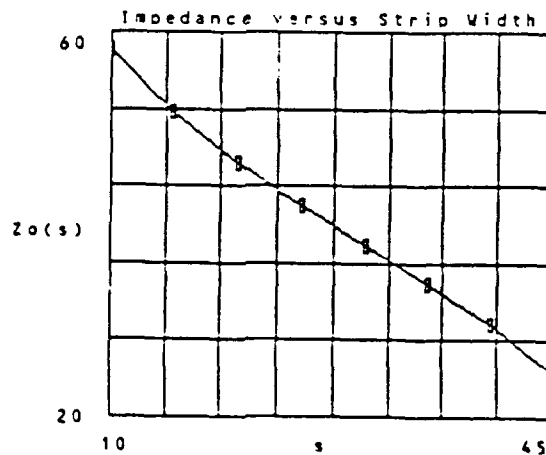


Operating Frequency: $F = 80$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	reff2(s)	AC(s)	AD(s)	$\lambda(s)$
13	53.25	7	0.72	0.054	1416.32
15	51.63	7	0.58	0.054	1416.32
20	46.39	7	0.52	0.054	1416.31
25	41.39	7	0.52	0.054	1416.31
30	37.78	7	0.55	0.054	1416.3
35	33.81	7	0.62	0.054	1416.3
40	29.69	7	0.71	0.054	1416.3
45	24.3	7	0.97	0.054	1416.31

Physical Parameters:

$g = 50$ microns $\epsilon_r = 13$
 $h = 1000$ microns $\tan \delta = 0.003$
 $h1 = 10000$ microns $\rho = 1.42$
 $T = 4$ microns $\lambda_0 = 3.75$ mm

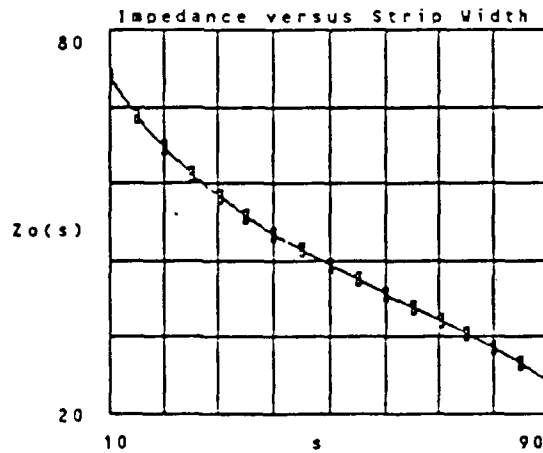


Operating Frequency: $F = 80$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	effZ(s)	AC(s)	AD(s)	$\lambda(s)$
10	72.39	7	0.53	0.054	1416.13
15	66.43	7	0.41	0.054	1416.16
20	61.51	7	0.34	0.054	1416.14
25	57.47	7	0.3	0.054	1416.13
30	54.01	7	0.28	0.054	1416.11
35	50.96	7	0.26	0.054	1416.1
40	48.2	7	0.25	0.054	1416.09
45	45.66	7	0.25	0.054	1416.08
50	43.29	7	0.25	0.054	1416.07
55	41.04	7	0.26	0.054	1416.07
60	38.87	7	0.27	0.054	1416.06
65	36.75	7	0.28	0.054	1416.06
70	34.64	7	0.3	0.054	1416.06
75	32.51	7	0.32	0.054	1416.06
80	30.3	7	0.35	0.054	1416.06
85	27.92	7	0.38	0.054	1416.07
90	25.21	7	0.48	0.054	1416.09

Physical Parameters:

$g = 100$ microns $\epsilon_r = 13$
 $h = 1000$ microns $\tan \delta = 0.003$
 $h1 = 10000$ microns $\rho = 1.42$
 $T = 4$ microns $\lambda_0 = 3.75$ mm

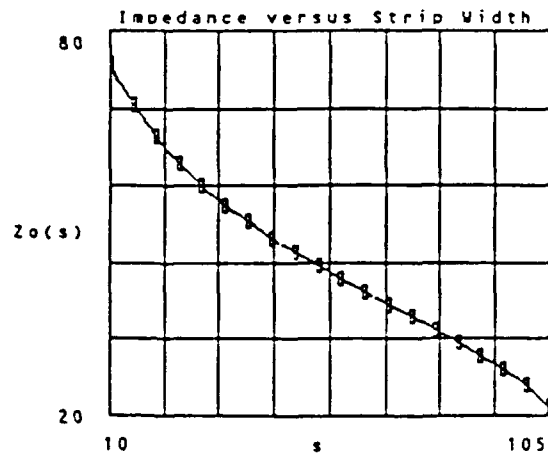


Operating Frequency: $F = 80$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	reff2(s)	AC(s)	AD(s)	$\lambda(s)$
10	74.93	7	0.51	0.054	1416.15
15	68.48	7	0.39	0.054	1416.12
20	63.57	7	0.33	0.054	1416.1
25	59.56	7	0.29	0.054	1416.08
30	56.13	7	0.26	0.054	1416.07
35	53.11	7	0.24	0.054	1416.05
40	50.4	7	0.23	0.054	1416.04
45	47.91	7	0.23	0.054	1416.03
50	45.61	7	0.22	0.054	1416.02
55	43.44	7	0.23	0.054	1416.01
60	41.37	7	0.23	0.054	1416
65	39.37	7	0.24	0.054	1416
70	37.43	7	0.25	0.054	1415.99
75	35.5	7	0.27	0.054	1415.99
80	33.57	7	0.28	0.054	1415.99
85	31.59	7	0.3	0.054	1416
90	29.52	7	0.32	0.054	1416
95	27.28	7	0.36	0.054	1415.92
100	24.7	7	0.48	0.054	1416.04
105	21.34	7	1.8	0.054	1416.07

Physical Parameters:

$g = 110$ microns $\epsilon_r = 13$
 $h = 1000$ microns $\tan\delta = 0.003$
 $h1 = 10000$ microns $\rho = 1.42$
 $r = 4$ microns $\lambda_0 = 3.75$ mm

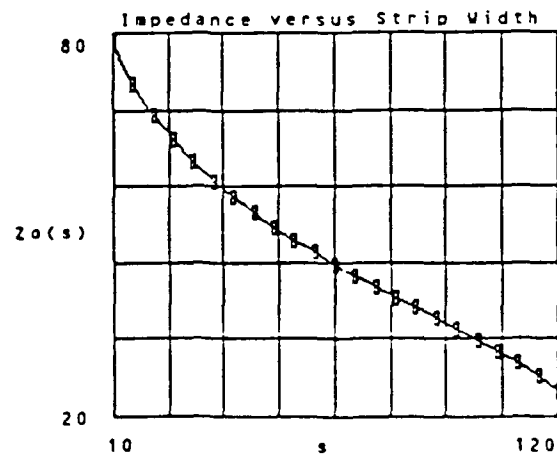


Operating Frequency: $F = 80$ GHz

um		ohms		Attenuation dB/mm		um
s	Zo(s)	effZ(s)	AC(s)	AD(s)	$\lambda(s)$	
10	78.52	7	0.48	0.054	1416.07	
15	72.08	7	0.36	0.054	1416.04	
20	67.19	7	0.3	0.054	1416.01	
25	63.2	7	0.26	0.054	1415.99	
30	59.81	7	0.24	0.054	1415.97	
35	56.84	7	0.22	0.054	1415.95	
40	54.19	7	0.21	0.054	1415.93	
45	51.78	7	0.2	0.054	1415.92	
50	49.55	7	0.19	0.054	1415.9	
55	47.48	7.01	0.19	0.054	1415.89	
60	45.53	7.01	0.19	0.054	1415.88	
65	43.67	7.01	0.19	0.054	1415.87	
70	41.89	7.01	0.19	0.054	1415.86	
75	40.17	7.01	0.2	0.054	1415.85	
80	38.49	7.01	0.21	0.054	1415.85	
85	36.84	7.01	0.22	0.054	1415.84	
90	35.19	7.01	0.23	0.054	1415.84	
95	33.54	7.01	0.24	0.054	1415.84	
100	31.85	7.01	0.25	0.054	1415.85	
105	30.1	7.01	0.27	0.054	1415.86	
110	28.25	7.01	0.29	0.054	1415.87	
115	26.21	7.01	0.33	0.054	1415.89	
120	23.84	7	0.51	0.054	1415.91	

Physical Parameters:

$g = 130$ microns $\epsilon_r = 13$
 $h = 1000$ microns $\tan\delta = 0.003$
 $h1 = 10000$ microns $\rho = 1.42$
 $T = 4$ microns $\lambda_0 = 3.75$ mm

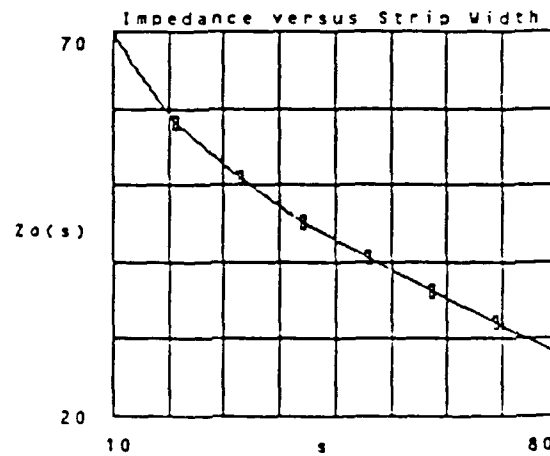


Operating Frequency: $F = 94$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	eff2(s)	AC(s)	AD(s)	$\lambda(s)$
10	69.61	7.19	0.6	0.064	1189.35
20	58.25	7.23	0.39	0.064	1186.45
30	50.82	7.25	0.32	0.065	1184.31
40	45.13	7.27	0.29	0.065	1182.67
50	40.39	7.29	0.29	0.065	1181.47
60	36.18	7.3	0.31	0.065	1180.74
70	32.23	7.3	0.35	0.065	1180.54
80	28.24	7.29	0.4	0.065	1181.09

Physical Parameters:

$g = 100$ microns $\epsilon_r = 13$
 $h = 100$ microns $\tan \delta = 0.003$
 $h1 = 1000$ microns $\rho = 1.42$
 $T = 4$ microns $\lambda_0 = 3.19$ mm

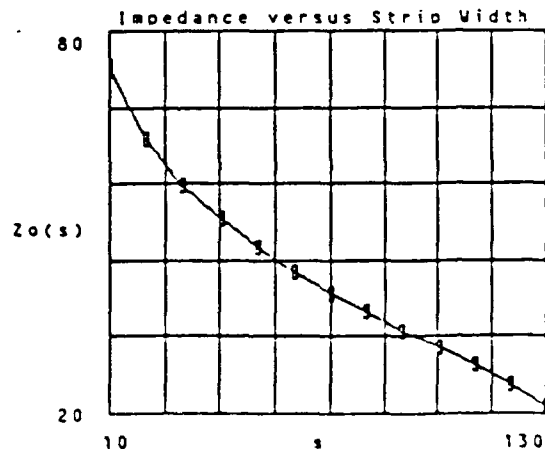


Operating Frequency: $F = 94$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	reff2(s)	AC(s)	AD(s)	$\lambda(s)$
10	74.51	7.3	0.54	0.065	1180.42
20	63.17	7.35	0.35	0.065	1176.27
30	55.87	7.39	0.27	0.065	1173.11
40	50.38	7.42	0.24	0.066	1170.53
50	45.93	7.45	0.22	0.066	1168.4
60	42.15	7.47	0.21	0.066	1166.67
70	38.83	7.49	0.22	0.066	1165.33
80	35.81	7.5	0.23	0.066	1164.39
90	33	7.51	0.24	0.066	1163.39
100	30.29	7.51	0.27	0.066	1163.39
110	27.57	7.5	0.3	0.066	1164.53
120	24.66	7.48	0.33	0.066	1166.12
130	21.11	7.44	0.34	0.066	1169.54

Physical Parameters:

$g = 140$ microns $\epsilon_r = 13$
 $h = 100$ microns $\tan \delta = 0.003$
 $h1 = 1000$ microns $\rho = 1.42$
 $T = 4$ microns $\lambda_0 = 3.19$ mm

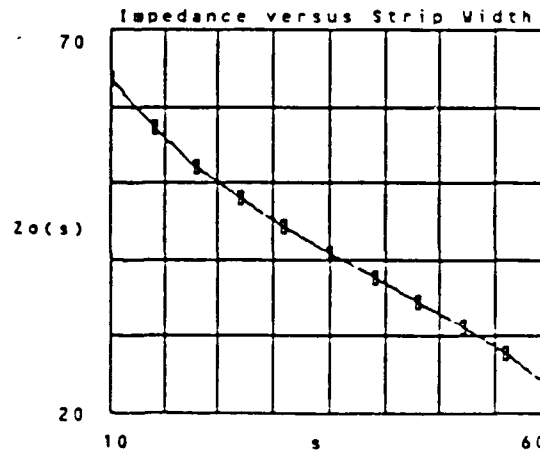


Operating Frequency: $F = 160$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	eff2(s)	AC(s)	AD(s)	$\lambda(s)$
10	63.75	7	0.9	0.107	708.14
15	57.22	7	0.71	0.107	708.14
20	52.17	7	0.61	0.107	708.13
25	47.93	7	0.56	0.107	708.13
30	44.22	7	0.55	0.107	708.13
35	40.82	7	0.56	0.107	708.12
40	37.62	7	0.6	0.107	708.12
45	34.49	7	0.66	0.107	708.12
50	31.29	7	0.73	0.107	708.12
55	27.82	7	0.83	0.107	708.13
60	23.55	7	1.45	0.107	708.13

Physical Parameters:

$g = 65$ microns $\epsilon_r = 13$
 $h = 1000$ microns $\tan \delta = 0.003$
 $h1 = 10000$ microns $\rho = 1.42$
 $T = 4$ microns $\lambda_0 = 1.88$ mm

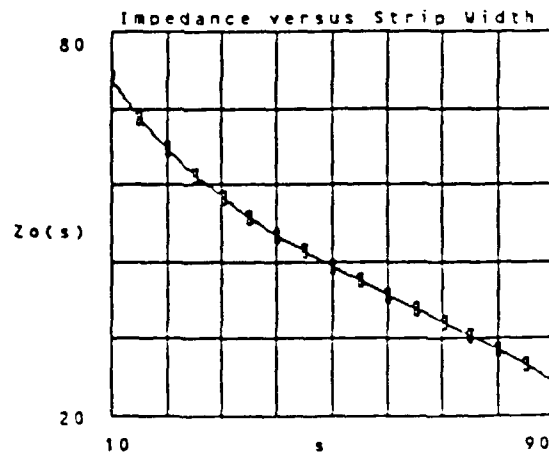


Operating Frequency: F = 160 GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	eff2(s)	AC(s)	AD(s)	$\lambda(s)$
10	72.39	7	0.75	0.107	708.39
15	66.43	7	0.57	0.107	708.08
20	61.51	7	0.48	0.107	708.07
25	57.47	7	0.43	0.107	708.36
30	54.01	7	0.39	0.107	708.36
35	50.96	7	0.37	0.107	708.05
40	48.2	7	0.36	0.107	708.35
45	45.56	7	0.35	0.107	708.34
50	43.29	7	0.35	0.107	708.34
55	41.34	7	0.36	0.107	708.33
60	39.87	7	0.38	0.107	708.33
65	36.75	7	0.4	0.107	708.33
70	34.64	7	0.43	0.107	708.33
75	32.51	7	0.46	0.107	708.33
80	30.3	7	0.49	0.107	708.33
85	27.92	7	0.54	0.107	708.34
90	25.21	7	0.58	0.107	708.35

Physical Parameters:

g = 100 microns $\epsilon_r = 13$
 h = 1000 microns $\tan \delta = 0.003$
 h1 = 10000 microns $\rho = 1.42$
 T = 4 microns $\lambda_0 = 1.88$ mm

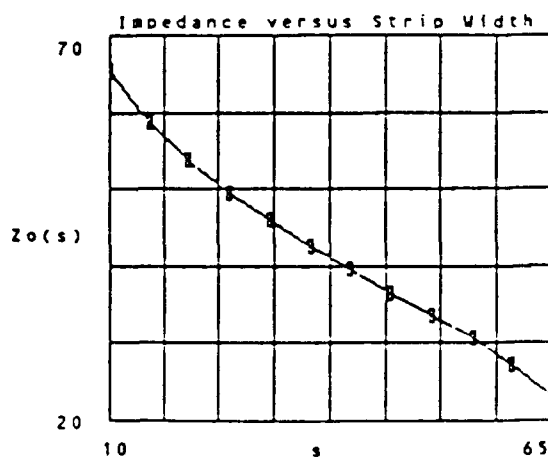


Operating Frequency: $F = 240$ GHz

um	ohms		Attenuation dB/mm		um
s	Zo(s)	reff2(s)	AC(s)	AD(s)	$\lambda(s)$
10	65.31	7	1.07	0.161	472.09
15	58.3	7	0.83	0.161	472.09
20	53.78	7	0.72	0.161	472.08
25	49.6	7	0.65	0.161	472.08
30	45.94	7	0.63	0.161	472.08
35	42.64	7	0.63	0.161	472.08
40	39.56	7	0.66	0.161	472.07
45	36.6	7	0.7	0.161	472.07
50	33.68	7	0.77	0.161	472.07
55	30.65	7	0.85	0.161	472.07
60	27.34	7	0.96	0.161	472.08
65	23.21	7	1.36	0.161	472.08

Physical Parameters:

$g = 70$ microns $\epsilon_r = 13$
 $h = 1000$ microns $\tan \delta = 0.003$
 $h1 = 10000$ microns $\rho = 1.42$
 $T = 4$ microns $\lambda_0 = 1.25$ mm



This routine calculates the impedance and line wavelength for slotline. This calculation does not include effects of metal backing.
 Ref: Garg & Gupta, MTT Aug 76, p. 532.

GHz := 1·10⁹ microns := 1·10⁻⁶

 Line parameters:

Operating frequency: f := 160

Gap width: w := 10, 20 .. 100

Dielectric Constant: er := 13

Dielectric thickness: d := 100

 Conditions and initial calculations:

er = 13 9.7 < er < 20

w

 d 0.2 < w/d < 1.0

$$\lambda_0 := \frac{3 \cdot 10^8}{f \cdot \text{GHz}} \cdot \left[\frac{1}{\text{microns}} \right]$$

0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1

TE10 surface-wave mode cutoff on line:

$$\text{TE10} := \frac{0.25}{\sqrt{\text{er} - 1}}$$

$$\text{TE10} = 0.07$$

Condition:
 0.01 < d/λ₀ < TE10

$$\frac{d}{\lambda_0} = 0.05$$

 Line Wavelength:

$$A(w) := 0.987 - 0.483 \cdot \log(\text{er}) + \frac{w}{d} \cdot (0.111 - 0.0022 \cdot \text{er})$$

$$B(w) := \left[0.121 + 0.094 \cdot \frac{w}{d} - 0.0032 \cdot \text{er} \right] \cdot \log \left[\frac{d}{\lambda_0} \cdot 100 \right]$$

$$\lambda_g(w) := (A(w) - B(w)) \cdot \lambda_0$$

Line Impedance:

$$AA(w) := 113.19 - 53.55 \cdot \log(\epsilon r) + 1.25 \cdot \frac{w}{d} \cdot (114.59 - 51.88 \cdot \log(\epsilon r))$$

$$BB(w) := 20 \cdot \left[\frac{w}{d} - 0.2 \right] \cdot \left[1 - \frac{w}{d} \right]$$

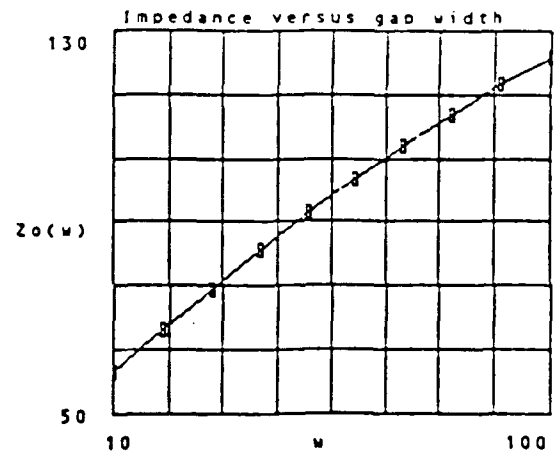
$$CC(w) := 0.15 + 0.23 \cdot \log(\epsilon r) + \frac{w}{d} \cdot (-0.79 + 2.07 \cdot \log(\epsilon r))$$

$$DD(w) := \left[10.25 - 5 \cdot \log(\epsilon r) + \frac{w}{d} \cdot (2.1 - 1.42 \cdot \log(\epsilon r)) - \frac{d}{\lambda_0} \cdot 100 \right]^2$$

$$Zo(w) := AA(w) + BB(w) - CC(w) \cdot DD(w)$$

Frequency: $f = 160$ GHz

um	ohms	um
w	Zo(w)	$\lambda_g(w)$
10	58.64	736.21
20	67.52	738.85
30	76.02	741.49
40	84.14	744.12
50	91.86	746.76
60	99.18	749.4
70	106.11	752.03
80	112.64	754.67
90	118.78	757.31
100	124.5	759.94



The following routine calculates the inductance of a straight wire with rectangular cross-section.

REF: Pettenpaul E. et al., CAD Models of Lumped Elements on GaAs up to 18 GHz, IEEE T-MTT, vol 36, Feb 1988, pp.294-304.

 Input Data: Width: w := 10 microns
 Length: l := 50 microns
 Thickness: t := 4 microns

Permeability: $\mu := 4 \cdot \pi \cdot 10^{-9}$ H/cm
 Conductivity: $\sigma := 0.410 \cdot 10^{-6}$ 1/(Ω cm)

Frequency: f := 80 GHz

Defn:

$$wt := \frac{w}{t} \quad tw := \frac{t}{w}$$

$$md1 := - \left[\frac{25}{12} \right] - \frac{1}{6} \left[wt^2 \cdot \ln \left[\sqrt{1 + tw^2} \right] + tw^2 \cdot \ln \left[\sqrt{1 + wt^2} \right] \right]$$

$$md2 := \frac{2}{3} (wt \cdot \text{atan}(tw) + tw \cdot \text{atan}(wt)) \quad p := \sqrt{\frac{2}{w} + \frac{2}{t}} \cdot \exp(md1 + md2)$$

$$Lo := \frac{\mu \cdot l \cdot 10^{-4}}{2 \cdot \pi} \left[\ln \left[2 \cdot \frac{l}{p} \right] - 1 \right] \quad \frac{Lo}{10^{-9}} = 0.025 \quad \text{nH}$$

Correction for skin effect:

$$m := \sqrt{\pi \cdot f \cdot \sigma \cdot \mu \cdot 10^9} \quad m = 0.036$$

$$Li := \frac{\mu \cdot l}{4 \cdot m \cdot w} \frac{\sinh \left[m \cdot t \cdot 10^{-4} \right] - \sin \left[m \cdot t \cdot 10^{-4} \right]}{\cosh \left[m \cdot t \cdot 10^{-4} \right] - \cos \left[m \cdot t \cdot 10^{-4} \right]}$$

$$\frac{Li}{10^{-9}} = 0.002 \quad \text{nH}$$

Total Inductance:

$$L := \frac{Lo + Li}{10^{-9}} \quad L = 0.027 \quad \text{nH}$$

APPENDIX F

Study of CPW-to-Rectangular Waveguide Probe Designs

F.1 Slab Probe Structures in Rectangular Waveguide

The slab probe is fabricated directly on the MMIC chip. Part of the chip protrudes through an aperture located in the top, (cf. sidewall couplers, etc.) of the rectangular waveguide. The probe flag which is the part of the probe that is inside the waveguide, can then be considered **transverse** if the plane of the metallization is perpendicular to the direction of wave propagation. In the **longitudinal** arrangement, the plane of metallization is parallel to the direction of propagation. Three probe structures of this nature were investigated.

a. Transverse CBCPW Probe

A sketch of the scale model for this probe structure is shown in Fig. F.1, with waveguide aperture details in Fig. F.2.

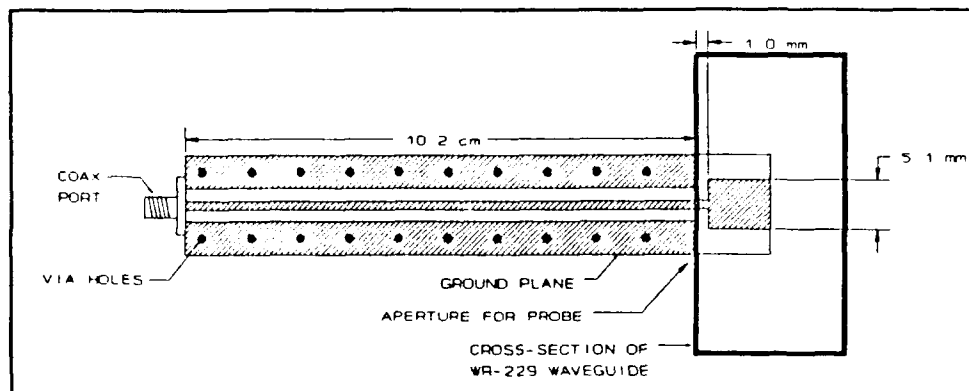


Figure F.1 Sketch of transverse CBCPW slab probe.

The probe structure was made using Stycast HiK ($\epsilon_r = 12$), 38 μm thick copper foil, and cyanoacrylate adhesive. A 10.2 cm length of CBCPW line with $g = 2.3 \text{ mm}$ and $s = 1.0 \text{ mm}$ was fabricated on 2.4 mm thick Stycast HiK

($\epsilon_r = 12$). The probe flag and substrate extend into the waveguide to 50 percent of the waveguide height. The waveguide aperture was 29 by 3.8 mm.

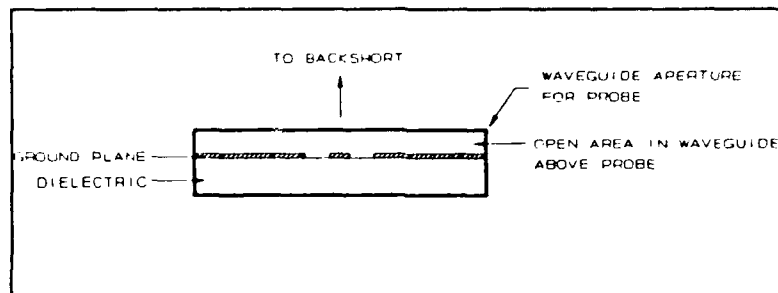


Figure F.2 Detail of waveguide aperture for CBCPW slab probe.

yielding a 1.3 mm by 29.0 mm hole in the waveguide above the CBCPW. To depict the worst-case situation, two rows (row spacing 12.0 mm) of evenly spaced 0-80 screws (screw spacing 6.4 mm or $\lambda g/4$ ($\epsilon_r = 12$) at 4.9 GHz) were positioned as shown. The transverse probe test fixture is shown in Fig. F.3. The test fixture consists of two 9 inch

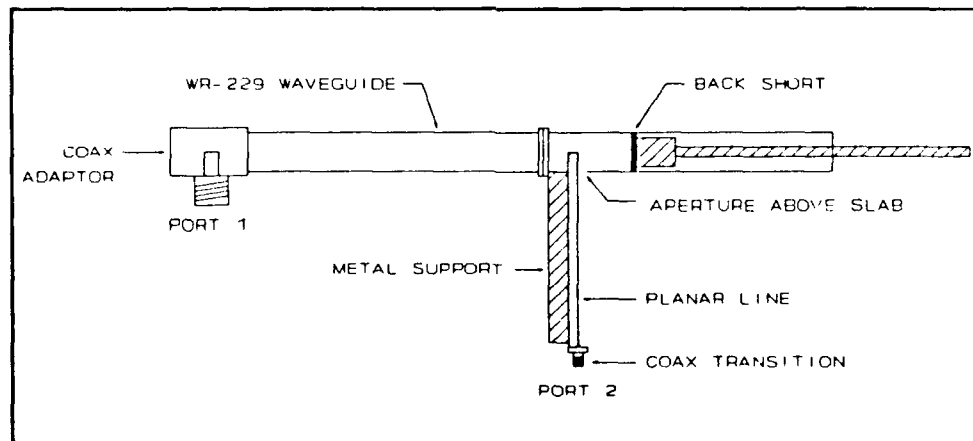


Figure F.3 Transverse probe test fixture.

sections of WR-229 waveguide. A commercial coax-to-waveguide adapter was used at one end of the waveguide thus forming port 1. The probe under test (which includes the adjustable contacting short) together with the

section of planar transmission line forms port 2.

With all ports matched and with reference planes at port 1 and port 2, $|S_{22}|$ and $|S_{12}|$ were measured using the HP8510 VNA. Time domain bandpass gating was used to eliminate a small reflection at the coax-CBCPW transition. The flag width, flag extension length from the end of the CBCPW, backshort position, and the aperture size were empirically optimized for minimum loss and impedance match ($RL > 15$ dB) over a wide bandwidth. The dimensions given in Fig. F.1 provide the best performance, with back-short positioned 14.7 mm from the flag. The results, which are shown in Figs. F.4 and F.5, indicate over 25 percent usable bandwidth ($RL > 20$ dB centered at 92 GHz) and about 0.5 dB of loss through the probe (CBCPW and waveguide loss removed). The loss was strongly dependent on the size of the waveguide opening above the probe surface where radiation was evident. The bandwidth is limited by the coupling of energy into the dielectric mode at the predicted frequency of 4.9 GHz.

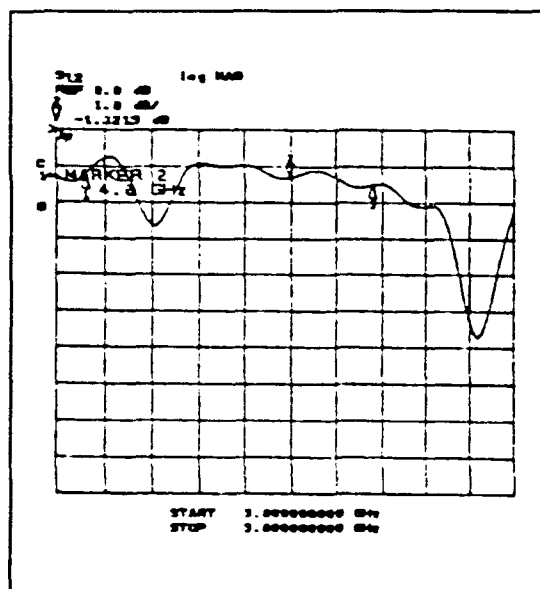


Figure F.4 Measurement of $|S_{12}|$ on the CBCPW transverse probe.

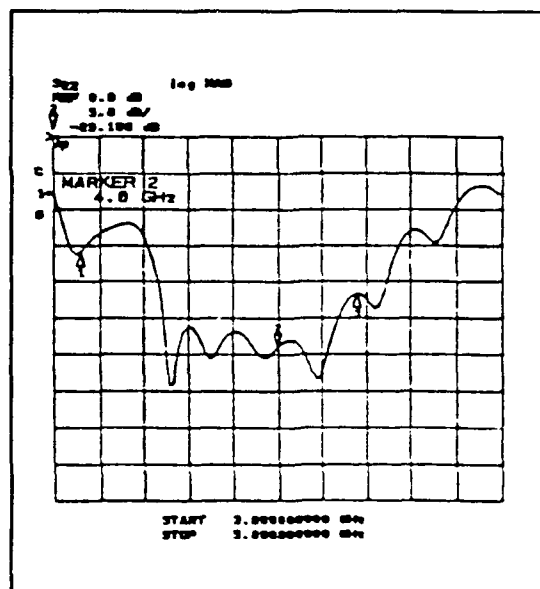


Figure F.5 Measured $|S_{22}|$ for the CBCPW transverse probe.

b. Longitudinal CBCPW Probe

Since the probe width to height ratio is about 6:1, it was of interest to investigate the probe performance when rotated 90 degrees with respect to the waveguide. A sketch of this longitudinal probe test fixture is shown in Fig. F.6.

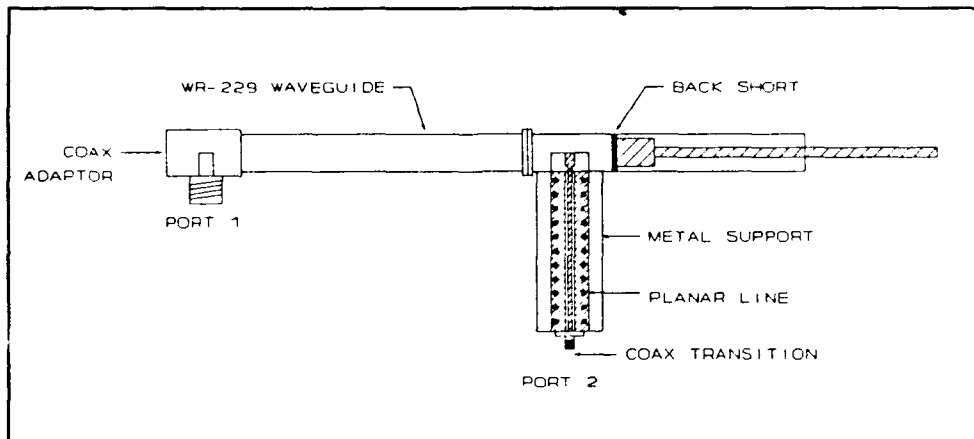


Figure F.6 The test fixture for the longitudinal probe studies.

Except for the orientation of the waveguide aperture, this probe test fixture is the same as in the transverse case. The dimensions for the probe are the same as in Fig. F.1, with the exception of the probe flag width which was increased to 6.4 mm to improve performance. The waveguide aperture orientation is shown in Fig. F.7.

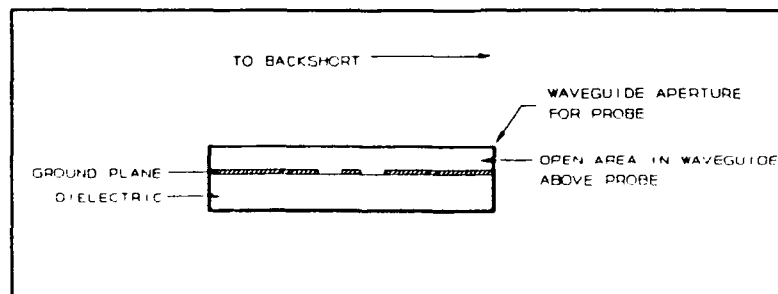


Figure F.7 Waveguide aperture for CPCPW probe.

The measured values for $|S_{21}|$ and $|S_{22}|$ are shown in Figs. F.8 and F.9 respectively. The results show about 25 percent bandwidth ($RL > 15$ dB) centered at 4.0 GHz (92 GHz scaled) with the back-short 7.6 mm from edge of the probe. The approximate probe loss is 0.5 dB with coupling in the dielectric mode at 4.9 GHz clearly visible. The radiation loss from the hole in the waveguide above the CBCPW was strongly dependent on hole size.

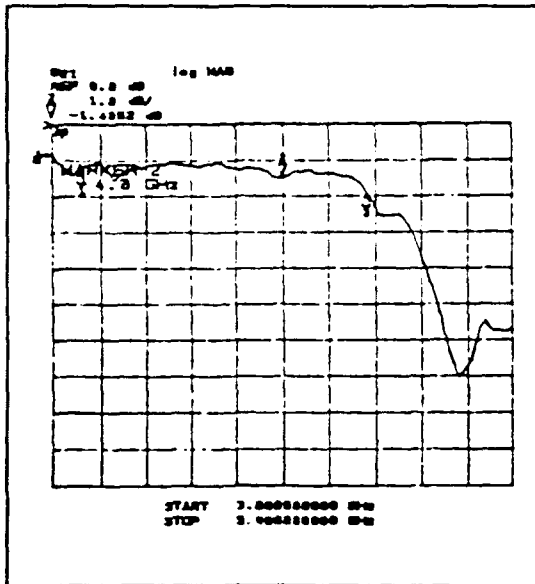


Figure F.8 Measured of $|S_{21}|$ for CBCPW long. probe.

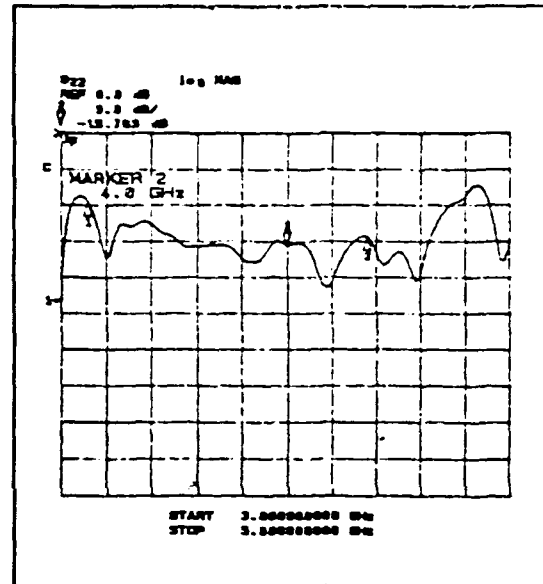


Figure F.9 Measured $|S_{22}|$ for CBCPW long. probe.

c. Transverse Inverted CPW Probe

A model of the inverted CPW and slab probe is shown in Fig. F.10. The probe structure was made using Stycast HiK ($\epsilon_r = 12$), 1.5 mil thick copper foil, and cyanoacrylate adhesive. A 12.7 cm length of CPW line with $g = 2.54$ mm and $s = 1.27$ mm was fabricated on 2.4 mm thick Stycast HiK ($\epsilon_r = 12$). The waveguide aperture for the probe is shown in Fig. F.11. Probe flag width was 5 mm and the waveguide hole above the CPW was 1.3 mm by 26.6 mm. The probe response was measured in the transverse fixture

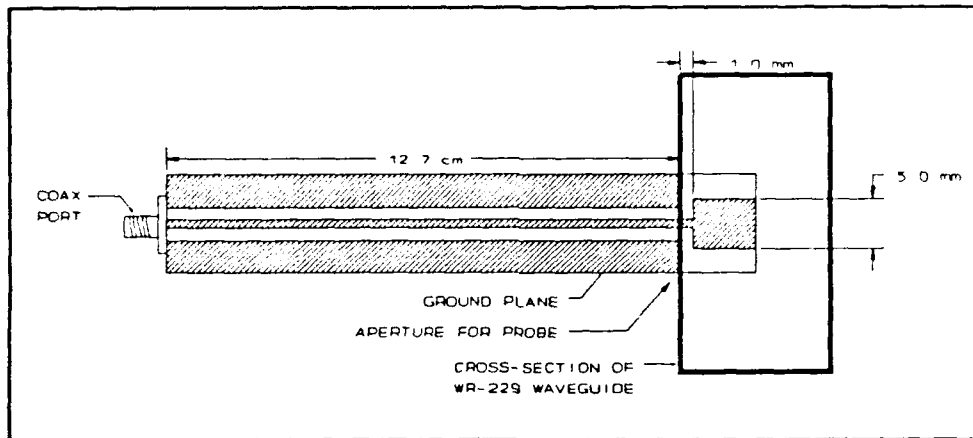


Figure F.10 Sketch of inverted CPW slab probe.

shown in Fig. F.2. With reference planes at port 1 and port 2, $|S_{21}|$ and $|S_{22}|$ were measured using the HP8510 VNA. Time domain bandpass

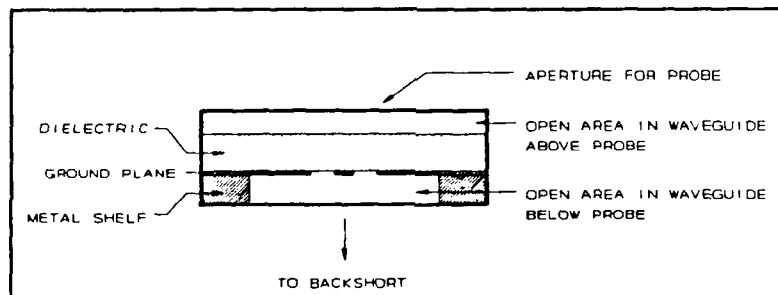


Figure F.11 Waveguide aperture for inverted CPW probe.

gating was used to eliminate a small reflection at the coax-CPW transition.

The probe performance (based on loss and bandwidth considerations) as a function of insertion depth into the waveguide was empirically investigated. The results are summarized in Table F.1. The probe depth into the waveguide was empirically optimized for minimum loss and good impedance match ($RL > 15$ dB) over a wide bandwidth. The dimensions given in Fig. F.8 gave the best performance, with back-short positioned 19.1 mm from the flag and flag depth 50 percent of the waveguide height resulting

in the S-parameter data shown in Figs. F.12 and F.13.

Table F.1 Inverted CPW Trasverse Probe Waveguide Depth Study				
Probe Depth Into Guide [percent of w/g height]	Backshort Position From Flag [mm]	Average Loss Through Probe [dB]	Probe Center Frequency [GHz]	Probe Bandwidth RL > 15 dB [GHz]
24	16.5	4.8	3.0 (69.0)	13
33	17.8	2.3	3.1 (71.3)	13
42	19.7	1.1	3.3 (75.9)	15
50	19.0	0.3	3.5 (80.5)	31
59	17.8	0.3	3.8 (87.4)	29
68	12.7	0.3	4.0 (92.0)	30

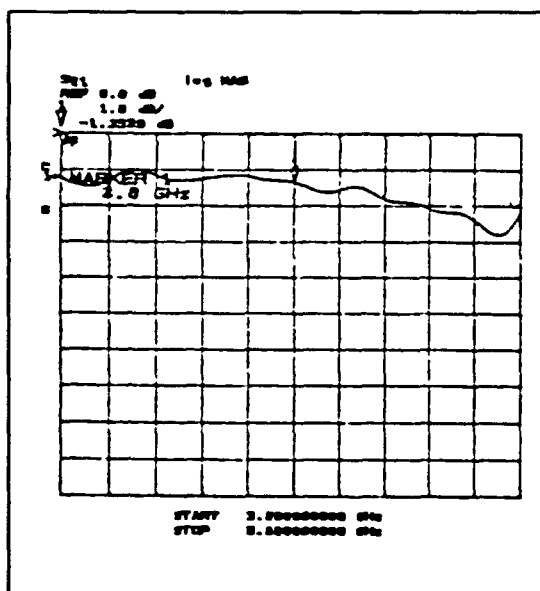


Figure F.12 Measured $|S_{21}|$ data for inverted CPW transverse probe (50% insertion depth).

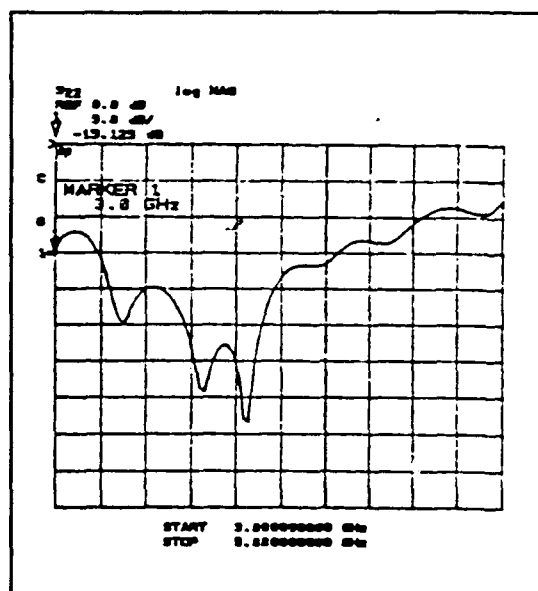


Figure F.13 Measured $|S_{22}|$ data for inverted CPW transverse probe (50% insertion depth).

F.2 Cantilevered Probe Structures in Rectangular Waveguide

An alternative probe for use at high frequencies is the **cantilevered** probe where the flag is not fabricated as part of the chip but rather is a piece of metal attached to the end of the substrate metallization in

cantilever fashion. This probe is useful for the multiplier output frequencies greater than 100 GHz since there will be no high-dielectric material inside the waveguide. Two types of cantilevered probes were investigated: a) CBCPW transverse type and b) Inverted CPW transverst type.

a. CBCPW Transverse Cantilevered Probe

A sketch of this probe is shown in Fig. F.14 with waveguide aperture shown if Fig. F.15. The probe structure was made using Stycast HiK ($\epsilon_r = 12$) and 1.5 mil thick copper tape. A 15.2 cm length of CBCPW line with $g = 2.0$ mm and $s = 1.3$ mm was fabricated on 2.4 mm thick Stycast HiK ($\epsilon_r = 12$). The probe flag extends into the waveguide to 50 percent of the waveguide height. The optimized waveguide aperture was 29.0 mm by 3.8 mm yielding 1.3 mm hole in the waveguide above the CBCPW.

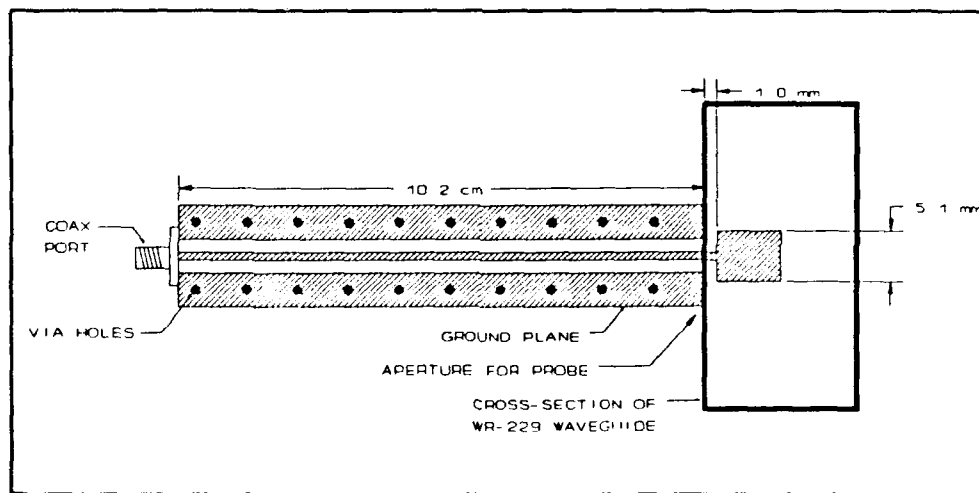


Figure F.14 Sketch of CBCPW cantilevered transverse probe.

To depict the worst-case situation, two rows (row spacing 9.5 mm) of evenly spaced 0-80 screws (screw spacing of 9.3 mm or $\lambda_g/4$ at 3.8 GHz) were positioned as shown. The results are given in Figs. F.16 and F.17.

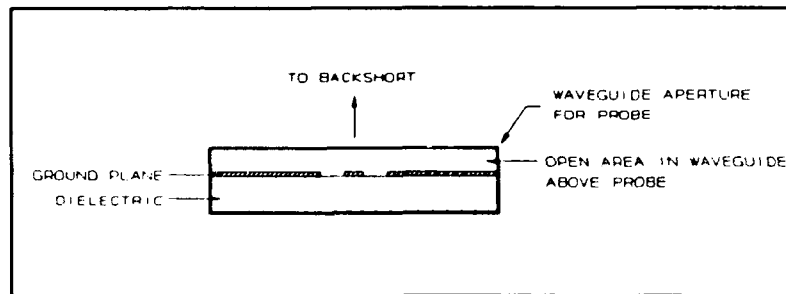


Figure F.15 Waveguide aperture for CBCPW cantilevered probe.

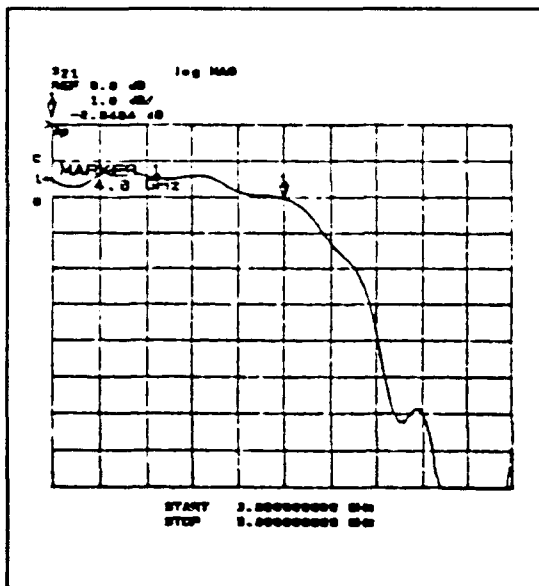


Figure F.16 Measured $|S_{21}|$ for the CBCPW cantilevered transverse probe.

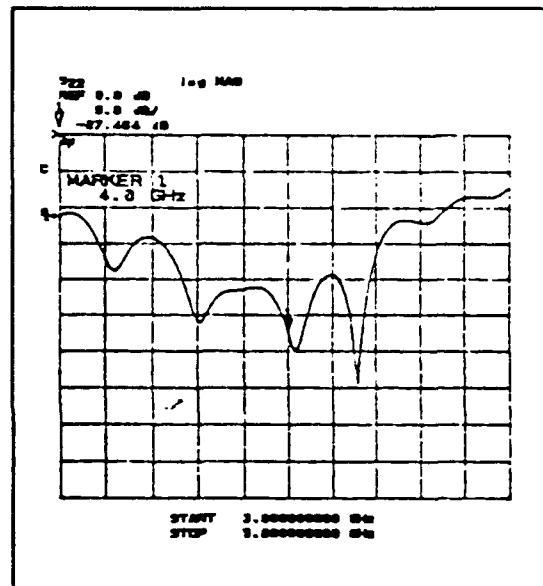


Figure F.17 Measured $|S_{22}|$ for the CBCPW cantilevered transverse probe.

The backshort was positioned 20 mm from the probe flag metal. For wide bandwidth operation, a very wide flag was needed. Probe loss was approximately 0.5 dB. Although the bandwidth appears to be greater than 30 percent centered at 3.8 GHz, as in the slab probe case, the measurement is corrupted by the onset of dielectric moding above 4 GHz. Further investigations into this probe were abandoned due to increased interest in the inverted CPW designs.

b. Inverted CPW Transverse Probe (TYPE I)

A scale model of the inverted CPW transverse probe (TYPE I) is shown in Fig. F.18 with waveguide aperture shown in Fig. F.19.

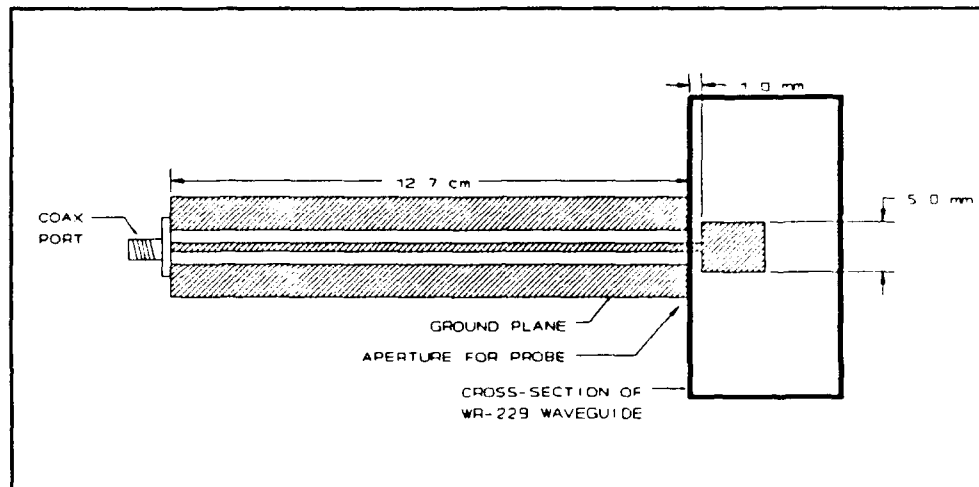


Figure F.18 Sketch of inverted CPW cantilevered probe. Shown with style A probe flag.

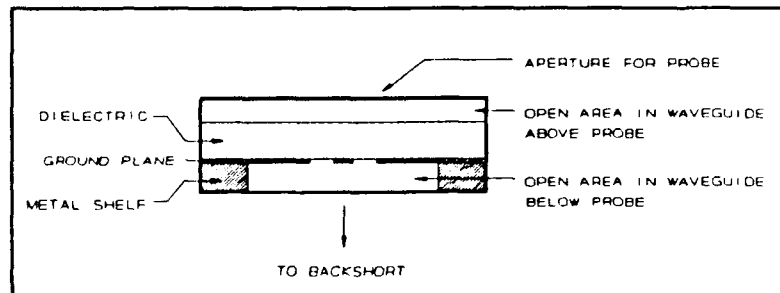


Figure F.19 Waveguide aperture for inverted CPW cantilevered probe.

The probe structure was made using Stycast HiK ($\epsilon_r = 12$), 38 μm thick copper foil, and cyanoacrylate adhesive. A 15.2 cm length of CPW line with $g = 2.54$ mm and $s = 1.27$ mm was fabricated on 2.4 mm thick Stycast HiK ($\epsilon_r = 12$). The waveguide hole above the CPW was 1.3 mm by 26.6 mm. The probe response was measured in the transverse fixture shown in Fig. F.2. With reference planes at ports 1 and port 2, $|S_{21}|$ and $|S_{22}|$ were measured using

the HP8510 VNA. Time domain bandpass gating was used to eliminate a small reflection at the coax-CPW transition.

Two styles of the probe flag (Fig. F.20) were investigated. The flag width and extension distance from the end of the CPW were varied for best performance. Measured results for flag style "A" with backshort at 19 mm from the flag are shown in Figs. F.21 and F.22, and style "B" with backshort at 18 mm from the flag are shown in Figs. F.23 and F.24.

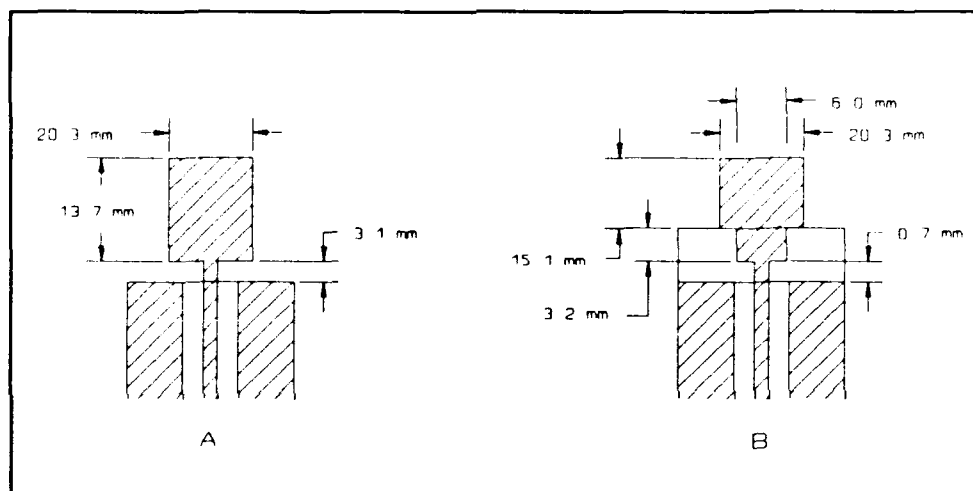


Figure F.20 Inverted CPW cantilevered transverse probe: Flag styles A and B.

The results indicate a very wide bandwidth with about 0.5 dB of loss. Although the flags shown in Fig. F.20 could be fabricated using photolithographic techniques in the MMIC design, the major disadvantage of probe style A is the weight of the very large flag and the small attachment area. Style B was an attempt to reduce the weight and increase the bonding area without additional loss or reduction in bandwidth.

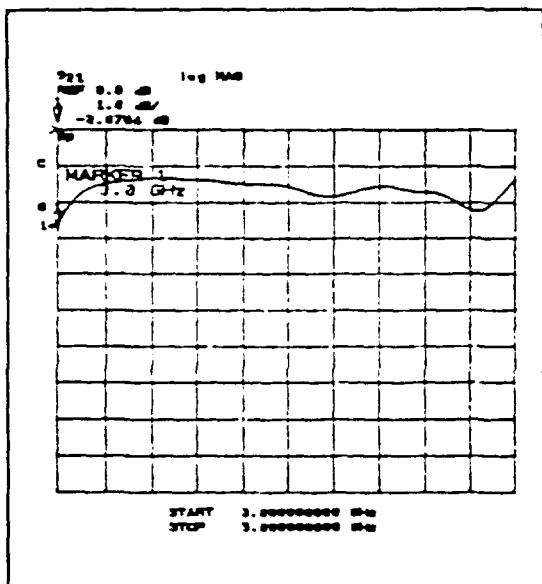


Figure F.21 Measured $|S_{21}|$ for the CPW cantilevered transverse probe A.

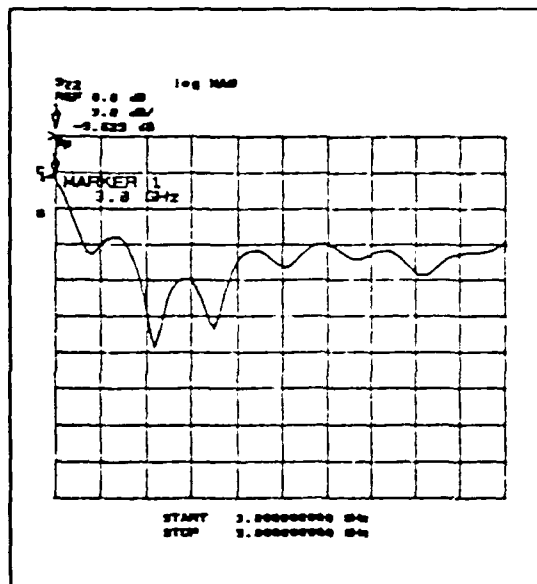


Figure F.22 Measured $|S_{22}|$ for the CPW cantilevered transverse probe A.

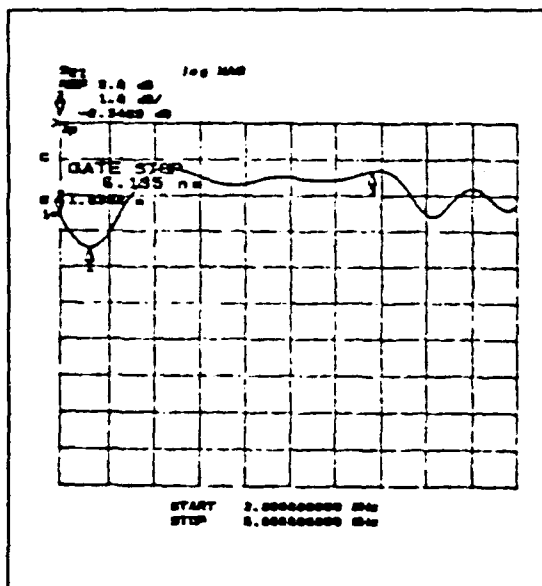


Figure F.23 Measured $|S_{21}|$ for the CPW cantilevered transverse probe B.

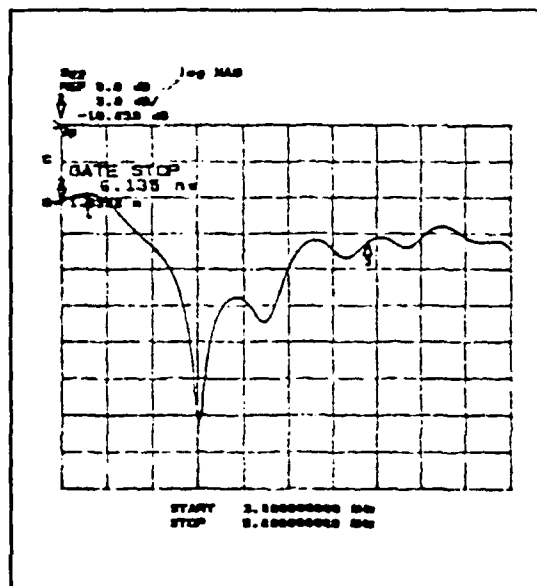


Figure F.24 Measured $|S_{22}|$ for the CPW cantilevered transverse probe B.

c. Inverted CPW Transverse Probe (TYPE II)

The unwanted additional fabrication requirements associated with the TYPE I probe stimulated the redesign of the probe flag region resulting in the TYPE II probe. The 44.9x scale model of the MMIC chip, shown in Fig. F.25, was fabricated using Stycast HiK ($\epsilon_r = 12$), 38 μm thick copper foil, and cyanoacrylate adhesive. The inverted CPW with $s = 1.5\text{ mm}$ and $g = 3.0\text{ mm}$ was tapered to $s = 5.8\text{ mm}$ and $g = 11.7\text{ mm}$ near the probe as shown. A constant impedance taper was used to increase the width of the CPW so that in the MMIC design a small gold wire or ribbon could be bonded to the end of the CPW as shown. The probe performance was measured for a 100 μm thick ribbon probe flag and for an 80 mils diameter cylindrical flag. Both flags extend into the rectangular waveguide to 50 percent of the guide height.

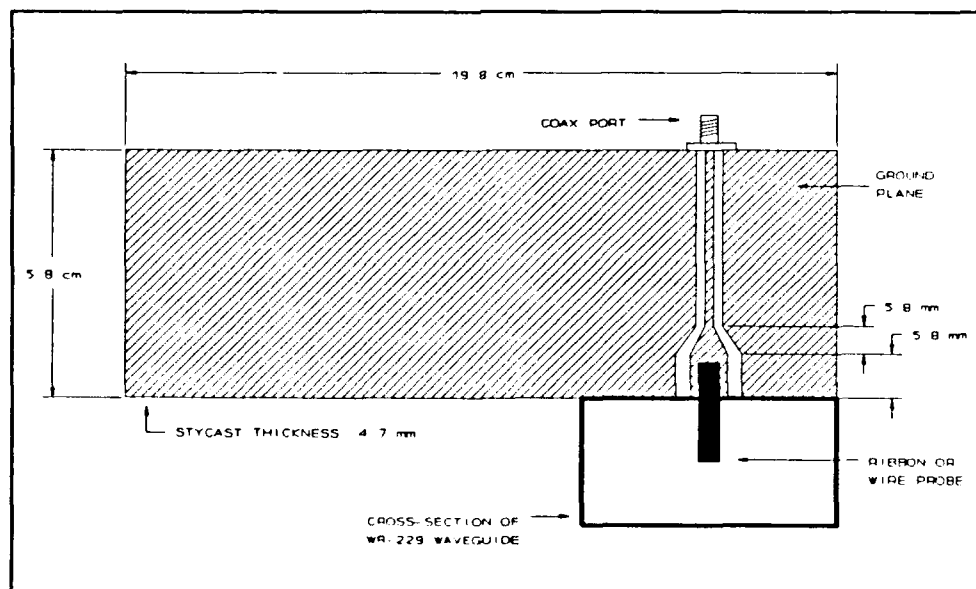


Figure F.25 Sketch of scale TYPE II inverted CPW transverse probe for both ribbon and cylindrical flag geometries.

The waveguide aperture for this probe, which is shown in Fig. F.26, is much smaller than in the previous probe designs.

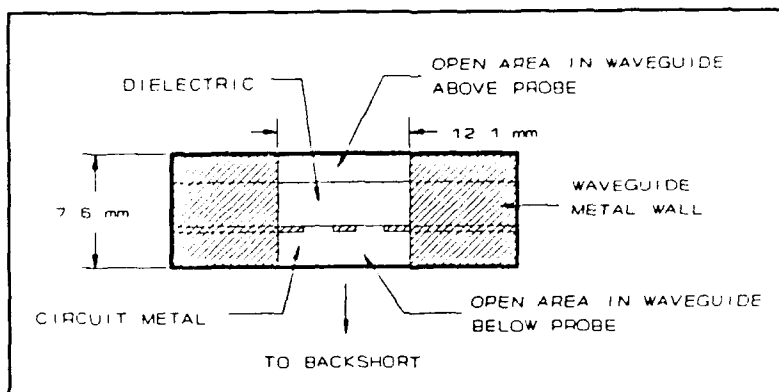


Figure F.26 Waveguide aperture used with the inverted CPW cantilevered TYPE II probe.

Measured results for ribbon flag with backshort at 19 mm from the probe flag is shown in Figs. F.27 and F.28, and for the cylindrical flag with backshort at 26 mm from the probe flag is shown in Figs. F.29 and F.30.

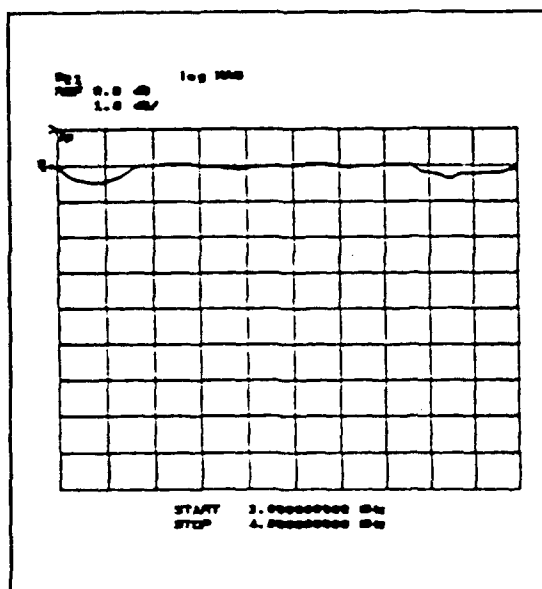


Figure F.27 Measured $|S_{21}|$ for the CPW cantilevered transverse ribbon probe.

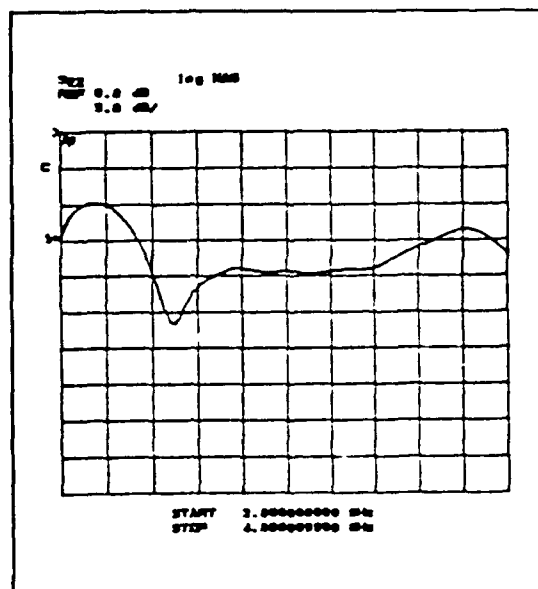


Figure F.28 Measured $|S_{22}|$ for the CPW cantilevered transverse ribbon probe.

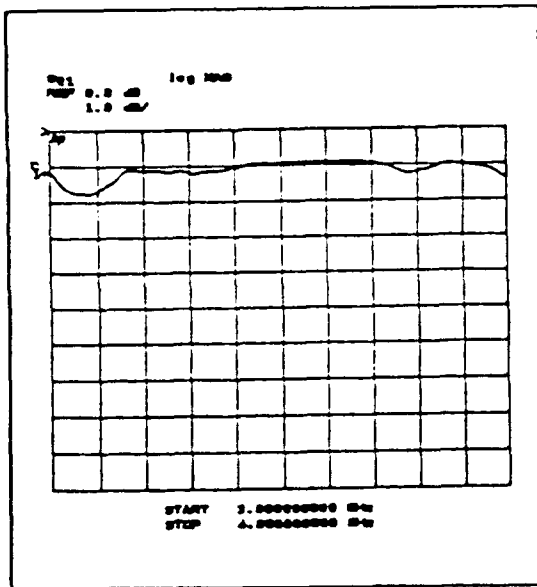


Figure F.29 Measured $|S_{21}|$ for the CPW cantilevered transverse cylindrical probe.

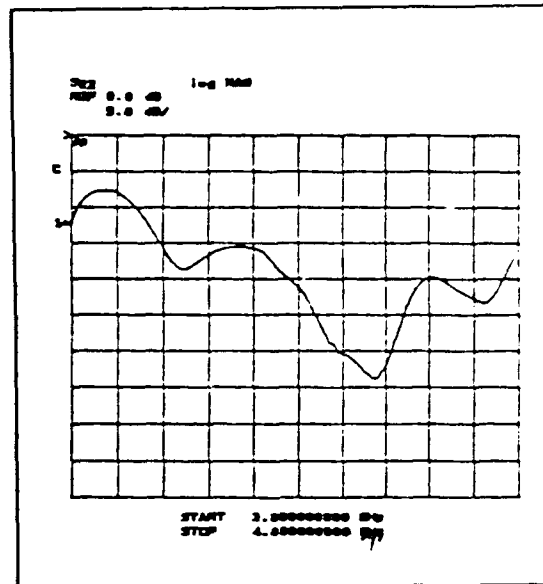


Figure F.30 Measured $|S_{22}|$ for the CPW cantilevered transverse cylindrical probe.

The cylindrical (wire) probe can be easily fabricated at 160 GHz using a 1.5 mil diameter wire and at 240 GHz using 1 mil diameter wire.

APPENDIX G

Mechanical Drawings for 80/160 GHz Doubler Mount

TOP
4-64765-023

LEFT
SIDE
4-64765-022

REAR
4-64765-021

FRONT
4-64765-021

RIGHT
SIDE
4-64765-022

BOTTOM
4-64765-024

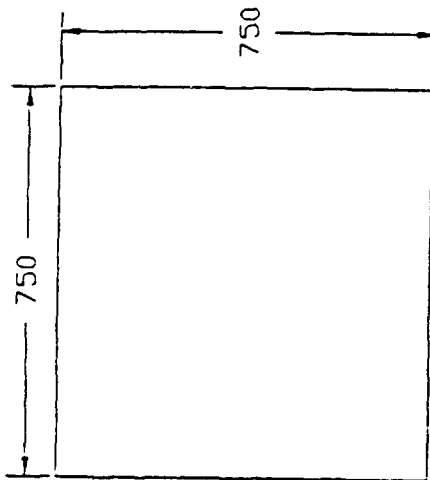
NOTE: NUMBER IN EACH BOX IS THE
CORRESPONDING DRAWING NUMBER
FOR THE VIEW. VIEW ORIENTATION
APPEARS AS SHOWN.

University of Virginia - SDI,
CHAIR OTTIESWILE, VA. 22903

FILE

BLOCK UPPER SECTION - DRAWING GUIDE

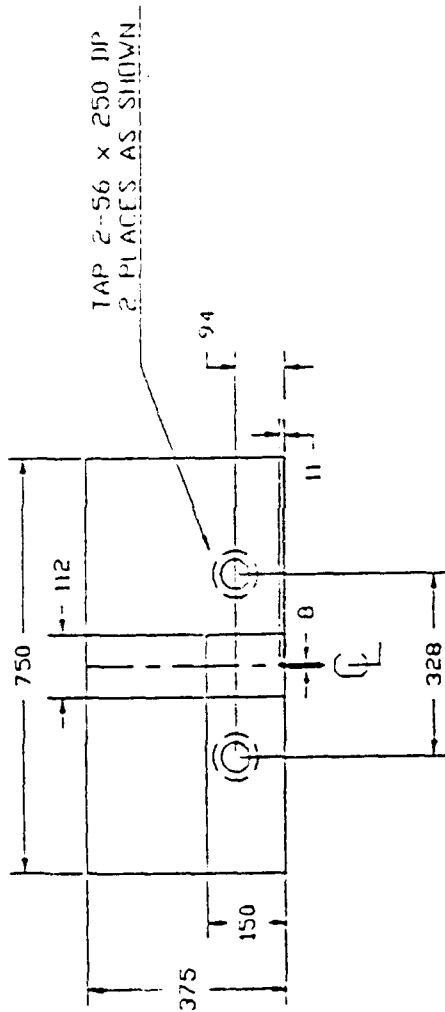
PROJECT 80/160 GHz MMIC DOUBLER - MOUNTING BLOCK	
RF D. RF B. 1 OF 1	COMPUTER DRAWING MATERIAL FINISH 160X240 DWG
SCALE NONE	DWG. NO. 4-64765-020



ALL DIMENSIONS
IN MILS (0.001")

TOLERANCE	
XXX	= ±1.0
XXX.X	= ±0.5

University of Virginia - SDL, CHARLOTTESVILLE, VA. 22903			
TITLE BLOCK UPPER SECTION, FRONT AND REAR VIEW			
PROJECT 80/160 GHz MMIC DOUBLER - MOUNTING BLOCK			
DESIGN DRAWN	R.F.B.	COMPUTER DRAWING	160X2MI.DWG
SHEET	R.F.B.	MATERIAL	BRASS
1 OF 1		FINISH	ASA B 01 LESS
SCALE	NONE	DWG. NO	4-64765-021
			REVISION



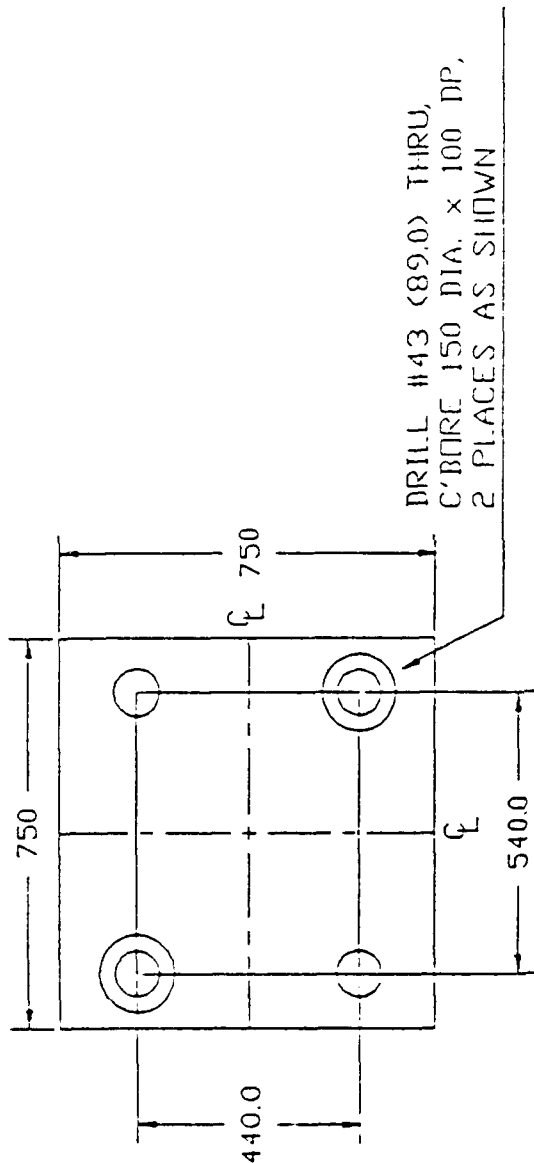
University of Virginia - SDL,
CHARLOTTESVILLE, VA. 22903

BLOCK UPPER SECTION
RIGHT AND LEFT SIDE VIEWS

PROJECT	80/160 GHz MMIC DIEBULK - MOUNTING BLOCK			
DESIGN	RF B.	COMPUTER	160X2M2.DWG	DRAWN BRASS ASA B OR LESS
DRAWN	RF B.	MATERIAL		
SHEET	1 OF 1	FINISH		
SCALE	NATURAL			DWG. TIO
				4-64/65-022

TOLERANCE
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XXX.X = 10.5

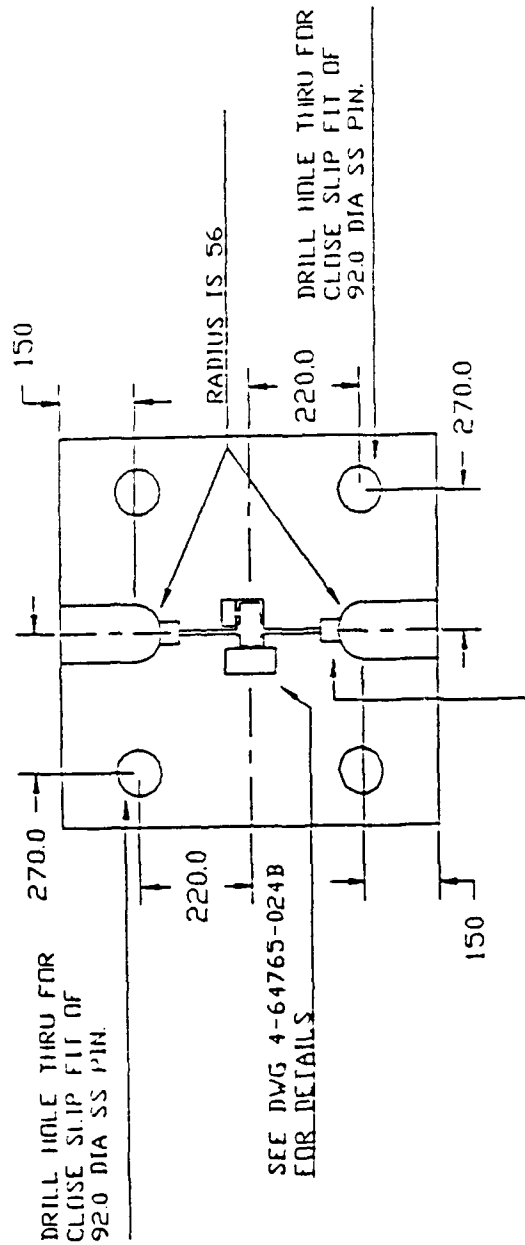
ALL DIMENSIONS
IN MILS (0.001")



University of Virginia - SDL	
CHARLOTTESVILLE, VA. 22903	
BLOCK UPPER SECTION - TOP VIEW	
PROJECT	80/160 GHz MIC DOUBLER - MOUNTING BLOCK
DESIGN	R.F.D.
DRAWN	R.F.D.
SHEET	1 OF 1
COMPUTER DRAWING	160X2H3 DWG
MATERIAL	BRASS
FINISH	ASA B OR LFSS
SCALE	1:1
DWG NO	4-64765-023

TOLERANCE	
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XXX.X	= ±0.5

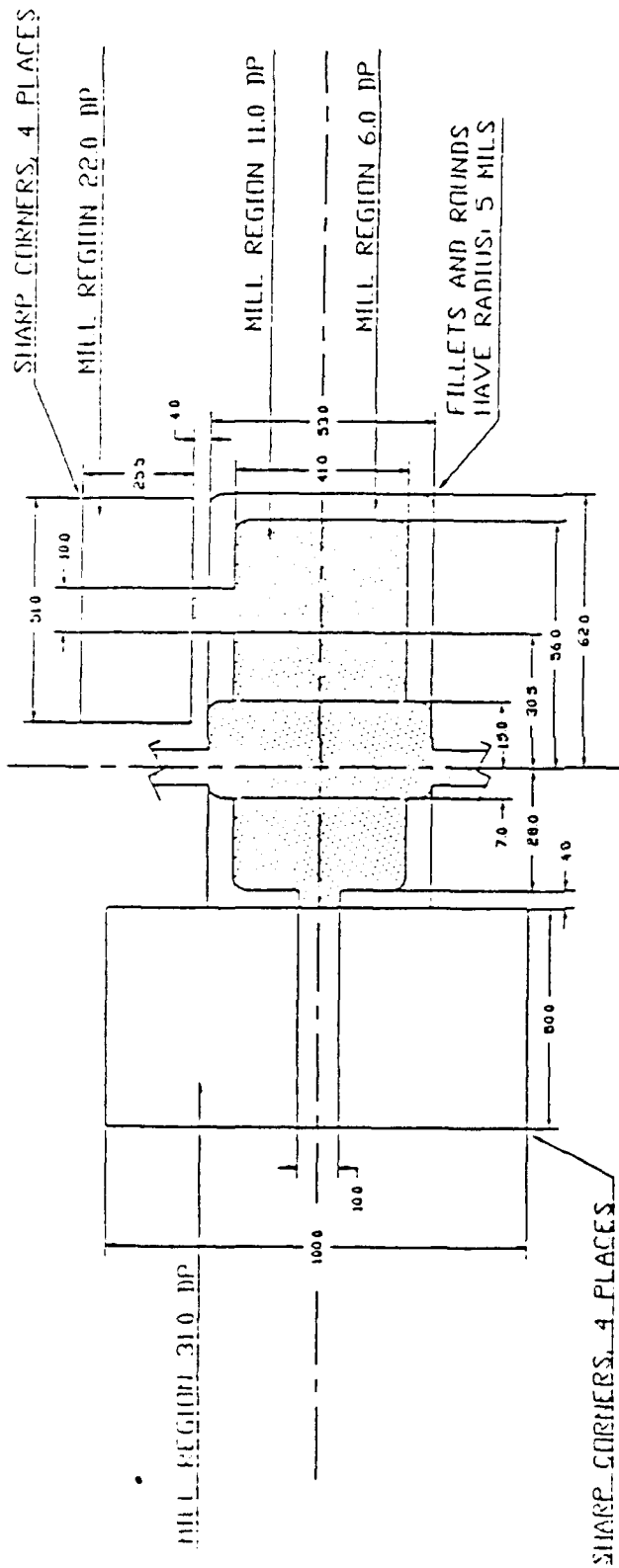
ALL DIMENSIONS
IN MILS (0.001")



University of Virginia - SDI, CHARLOTTESVILLE, VA. 22903		BLOCK UPPER SECTION - BOTTOM VIEW	
DATE	PROJECT	10/160 G12 NMC HUBBLER - MOUNTING BLOCK	REVISION
DESIGN	RF.D.	COMPUTER DRAWING	100X2M-1A DWG
DRAWN	RF.D.	MATERIAL	BRASS
SHEET	1 OF 1	FINISH	ASA 4 OR LFSS
SCALE	NONE	DWG. NO	4-64765-024A

TOLERANCE
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XXX.X = ±0.5

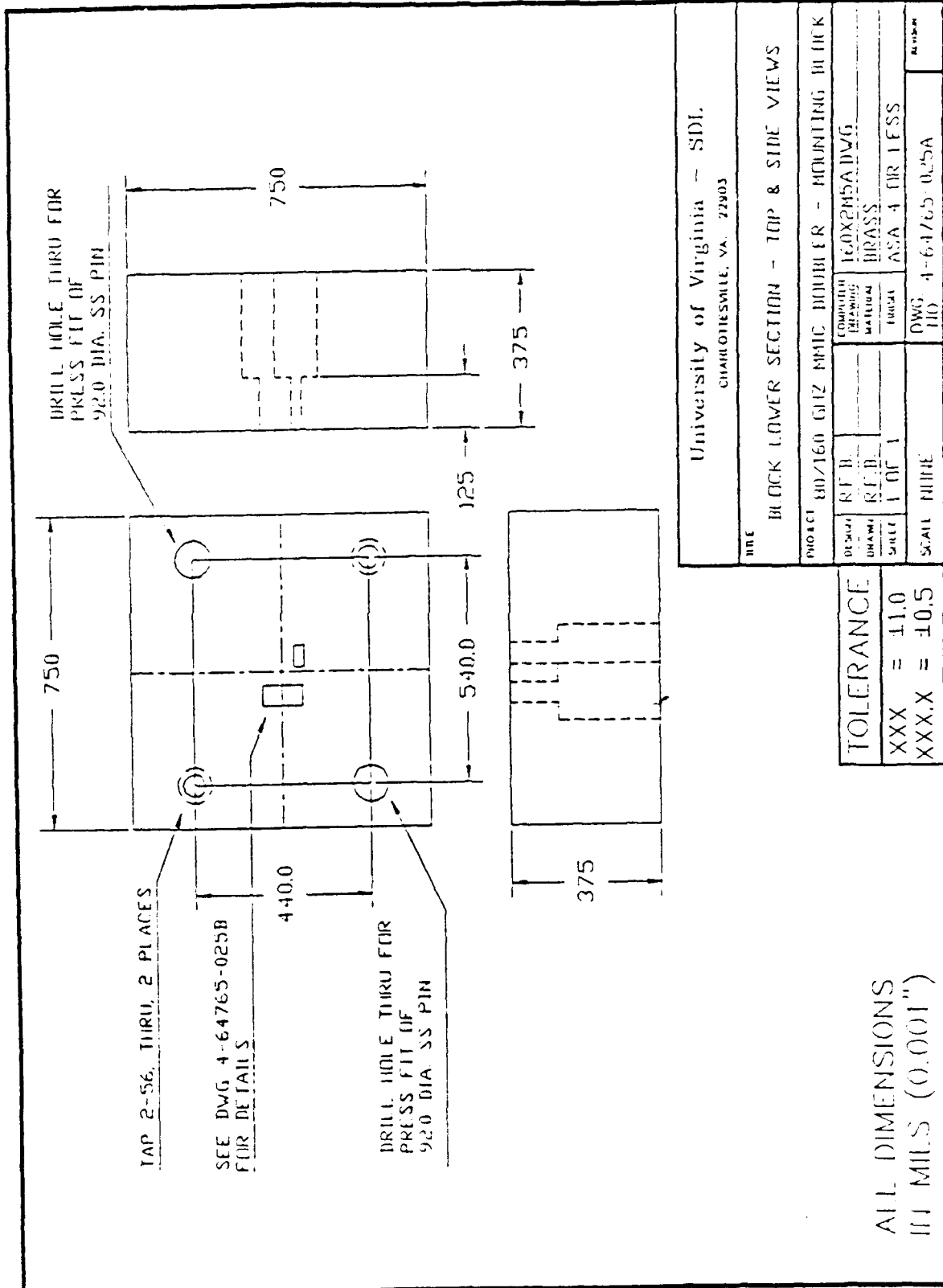
ALL DIMENSIONS
IN MILS (0.001")

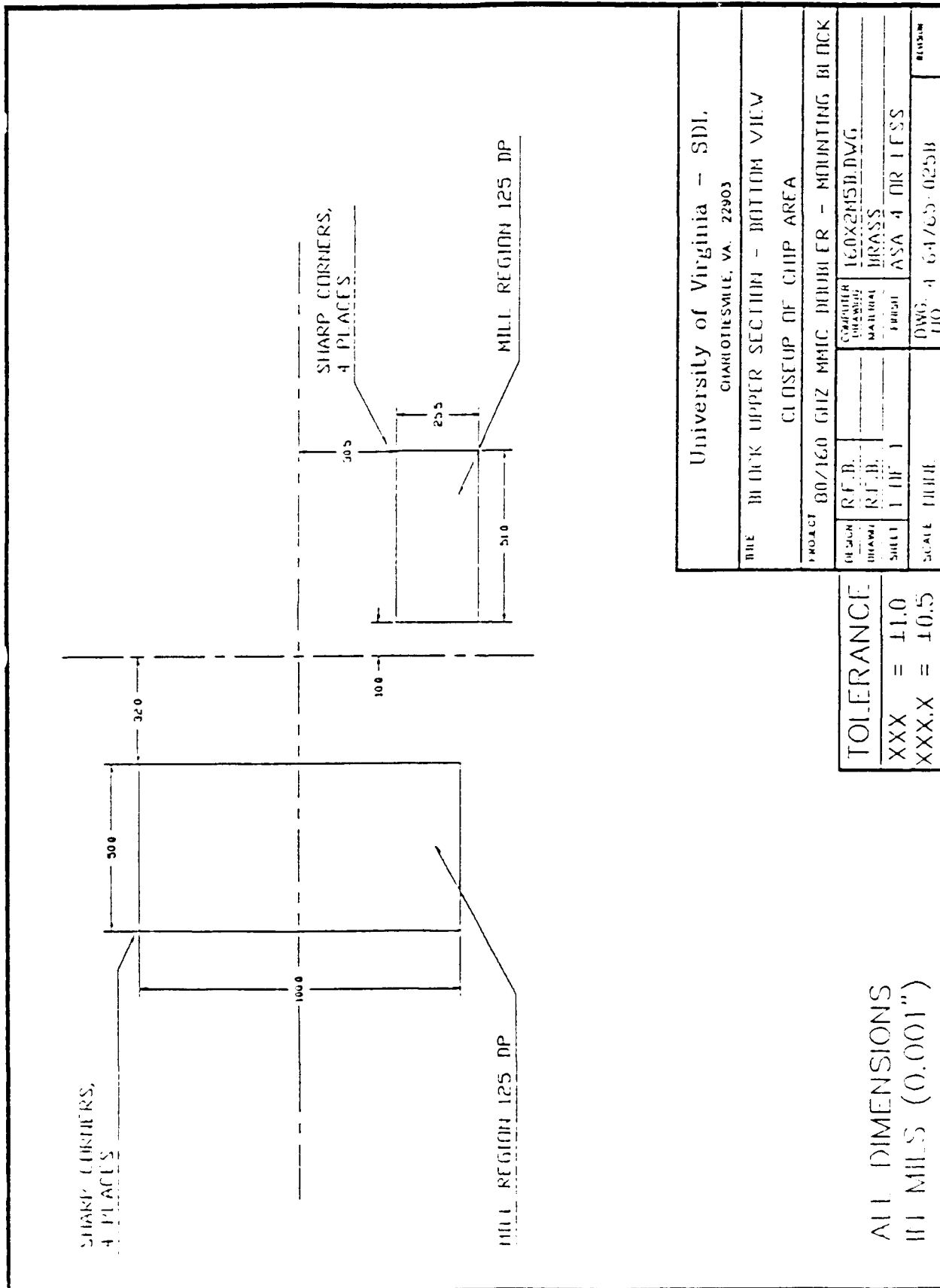


TOLERANCE
XXX = ±1.0
XXX.X = ±0.5

ALL DIMENSIONS
IN MILS (0.001")

University of Virginia - SDI. CHARLOTTESVILLE, VA. 22903			
TITLE BLOCK UPPER SECTION - BOTTOM VIEW CLOSEUP OF CHIP AREA			
PROJECT	80/160 GHz MMIC DRIVER - MOUNTING BLOCK		
DESIGN	RF.B	COMPUTER	160X24-REDAVG
QUANTITY	RF.B	MATERIAL	BRASS
SHEET	1 OF 1	FIGURE	ASA 4 OR LESS
SCALE NONE		DWG. 4-64765-024B	
		NO.	



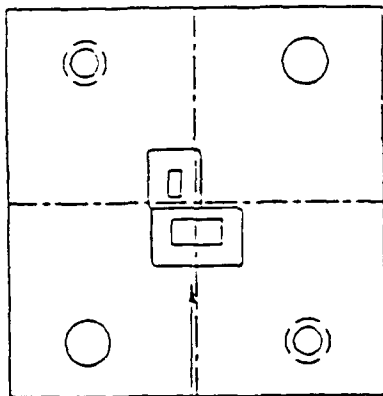


TOLERANCE	
XXX	= ±1.0
XXX.X	= ±0.5

ALL DIMENSIONS
IN MILS (0.001")

University of Virginia - SDI, CHARLOTTESVILLE, VA. 22903			
TITLE BLOCK UPPER SECTION - BOTTOM VIEW			
PROJECT CLOSEUP OF CHIP AREA			
PROJECT 80/160 GHz MMIC DRIVER - MOUNTING BLOCK			
DESIGN DRAWN	R.F.B.	CONDITION DATE	160X24MSB.DWG
SHEET	1 OF 1	MATERIAL	BRASS
SCALE	1:1	FINISH	ASA 4 PR 1 FSS
DWG. 4 64/65-025B		REVISION	

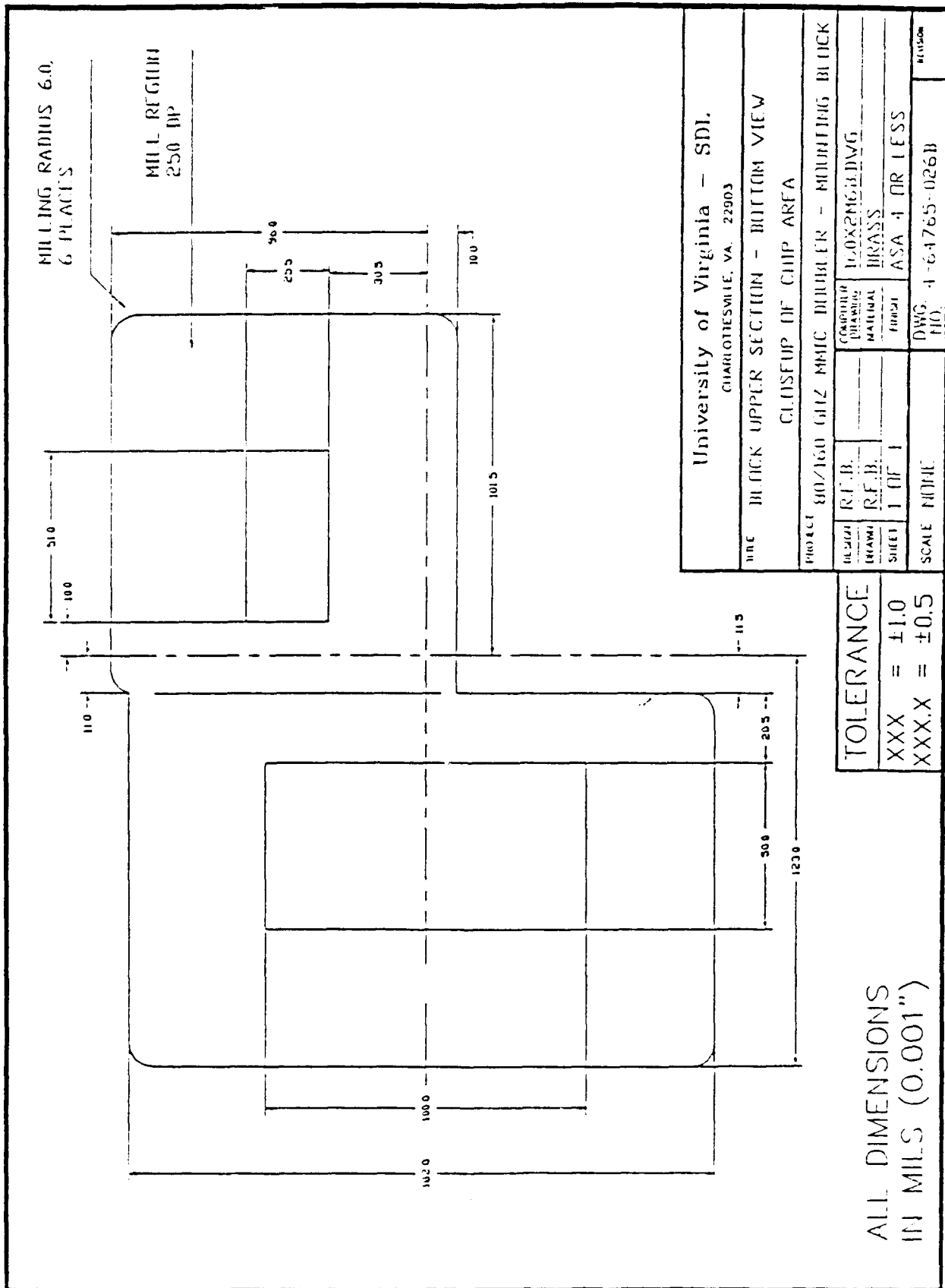
SEE DWG 4-64765-026B
FOR DETAILS



ALL DIMENSIONS
IN MILS (0.001")

TOLERANCE
XXX = ±1.0
XXX.X = ±0.5

University of Virginia - SDI CHARLOTTESVILLE, VA. 22903			
BLOCK LOWER SECTION - BOTTOM VIEW			
PROJECT 80/160 GUZ MMIC DRIVER - MOUNTING BLOCK			
DESIGN DRAWN	R.F.D. R.F.D.	COMPUTER DRAWING	160X2M6A DWG
SHEET 1 OF 1		NATURAL	BRASS
		FINISH	ASA 4 OR 1 FSS
SCALE THREE		DWG NO	4-64765-026A
		REVISED	



TOLERANCE	
XXX	= ±1.0
XXX.X	= ±0.5

ALL DIMENSIONS
IN MILS (0.001")

APPENDIX H

Mechanical Drawings for 80/240 GHz Tripler Mount

TOP
4-64765-033

RIGHT
SIDE
4-64765-032

FRONT
4-64765-031

LEFT
SIDE
4-64765-032

REAR
4-64765-031

BOTTOM
4-64765-034

NOTE, NUMBER IN EACH BOX IS THE
CORRESPONDING DRAWING NUMBER
FOR THE VIEW. VIEW ORIENTATION
APPEARS AS SHOWN.

University of Virginia - SDL

CHARLOTTESVILLE, VA. 22903

nmic

BLOCK UPPER SECTION - DRAWING GUIDE

PROJECT 80/240 GHz NMIC TRIPLER - MOUNTING BLOCK

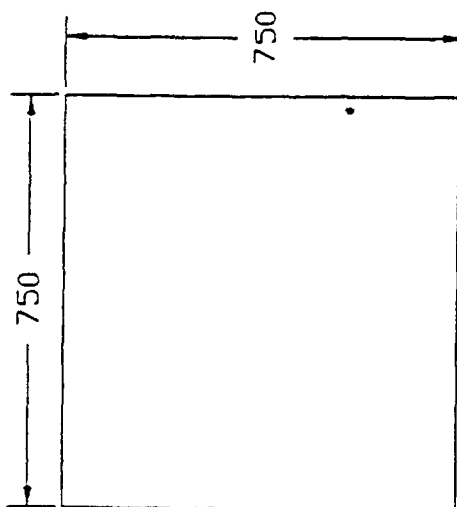
240X340.DWG

DESIGN R.F.B. COMPUTER
DRAWING R.F.B. MATERIAL
SHEET 1 OF 1 EDITION

REVISION

DWG. 4-64765-030
P10

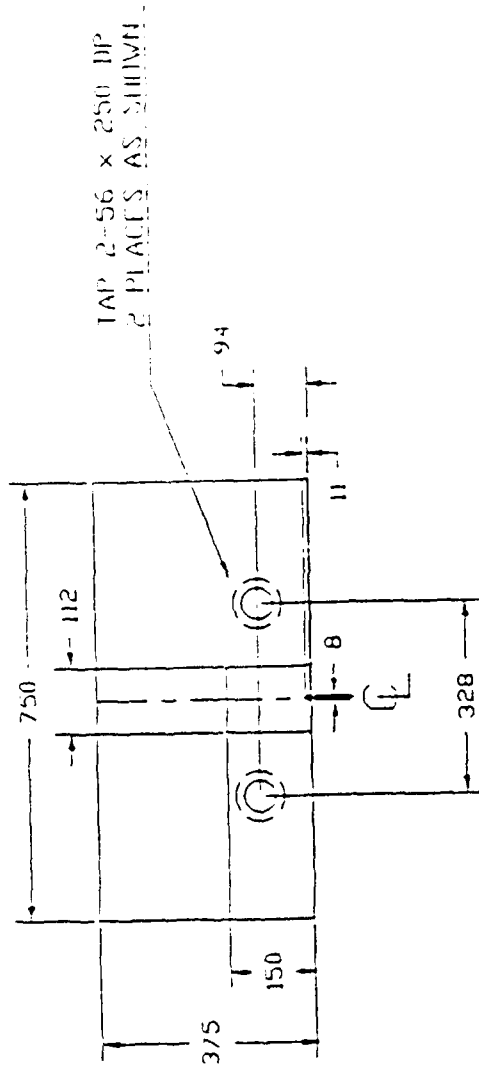
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ALL DIMENSIONS
IN MILS (0.001")

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XXX.X	= ±0.5

University of Virginia - SDL CHARLOTTESVILLE, VA. 22903			
TITLE BLOCK UPPER SECTION, FRONT AND REAR VIEW			
PROJECT 80/240 GHz MMIC TRIPLER - MOUNTING BLOCK			
DESIGN DRAWN	R.F.B.	COMPUTER PROCESSING	240X3M1.DWG
SHEET	R.F.B.	MATERIAL	BRASS
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SCALE NONE		DWG. 4-64765-031 REV	



University of Virginia - SDL
CHARLOTTESVILLE, VA 22903

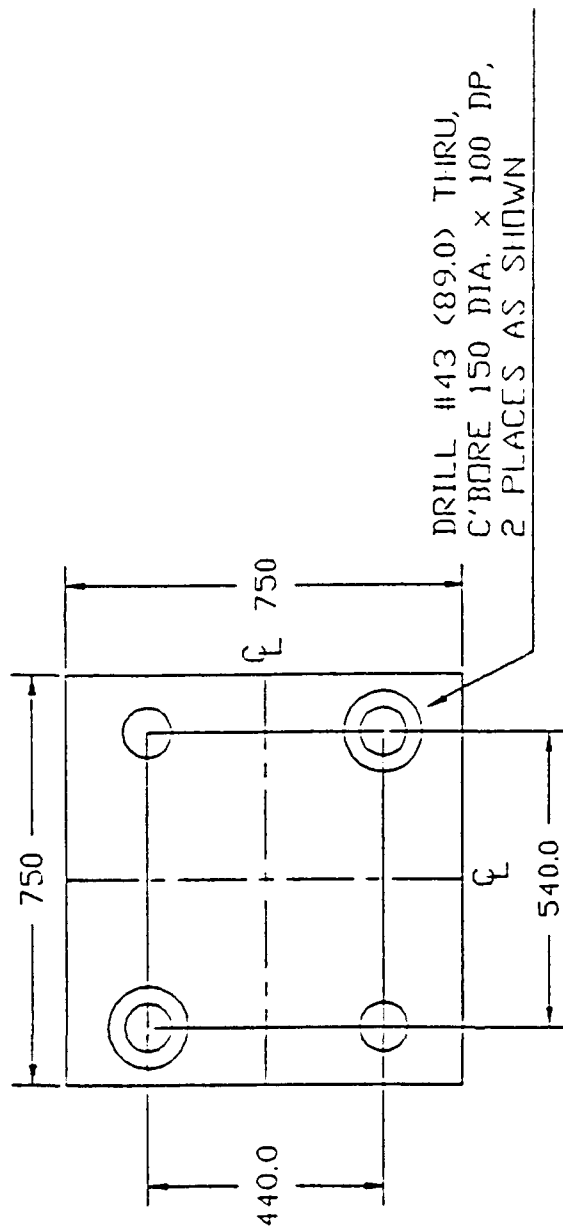
BLOCK UPPER SECTION
RIGHT AND LEFT SIDE VIEWS

PROJECT 80/240 GUZ MICRIPLEX - MOUNTING BLOCK

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XXX.X = ±0.5

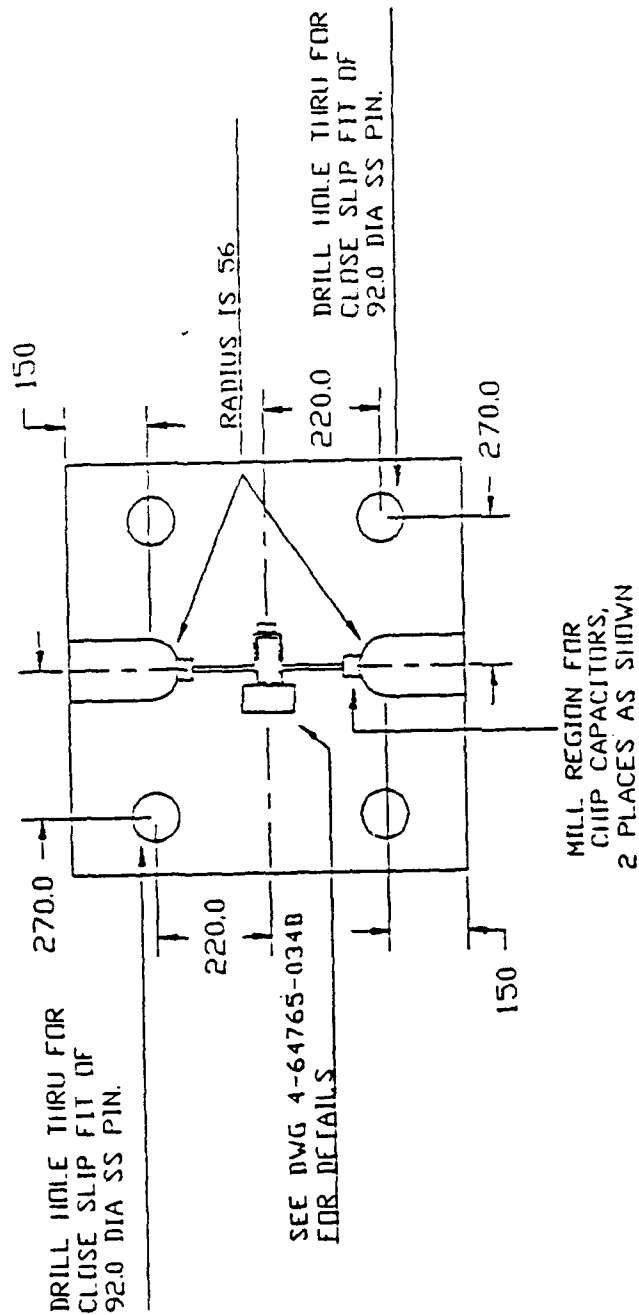
ALL DIMENSIONS
IN MILS (0.001")



ALL DIMENSIONS
IN MILS (0.001")

TOLERANCE
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XXX.X = ±0.5

University of Virginia - SDL		CHARLOTTESVILLE, VA. 22903	
TITLE		BLOCK UPPER SECTION - TOP VIEW	
PROJECT	80/240 GHZ MMIC TRIPLER - MOUNTING BLOCK	COMPUTER	2-40X3M3 DWG
	DESIGN	DRAWING	MATERIAL
	DATE	1 11 1	BRASS
SCALE		DWG. 4-64765-033	
TOLERANCE		ALL DIMENSIONS	
XXX = ±1.0		XXX.X = ±0.5	



ALL DIMENSIONS
IN MILS (0.001")

University of Virginia - SDL

CHARLOTTESVILLE, VA. 22903

TITLE

BLOCK UPPER SECTION - BOTTOM VIEW

PROJECT

100/240 GHz MMIC TRIPLET - MOUNTING BLOCK

DESIGN

R.F.B.

COMPUTER

24DX3M1A.DWG

DRAWN

R.F.B.

MATERIAL

BRASS

SHEET

1 OF 1

FINISH

ASA 4 OR LESS

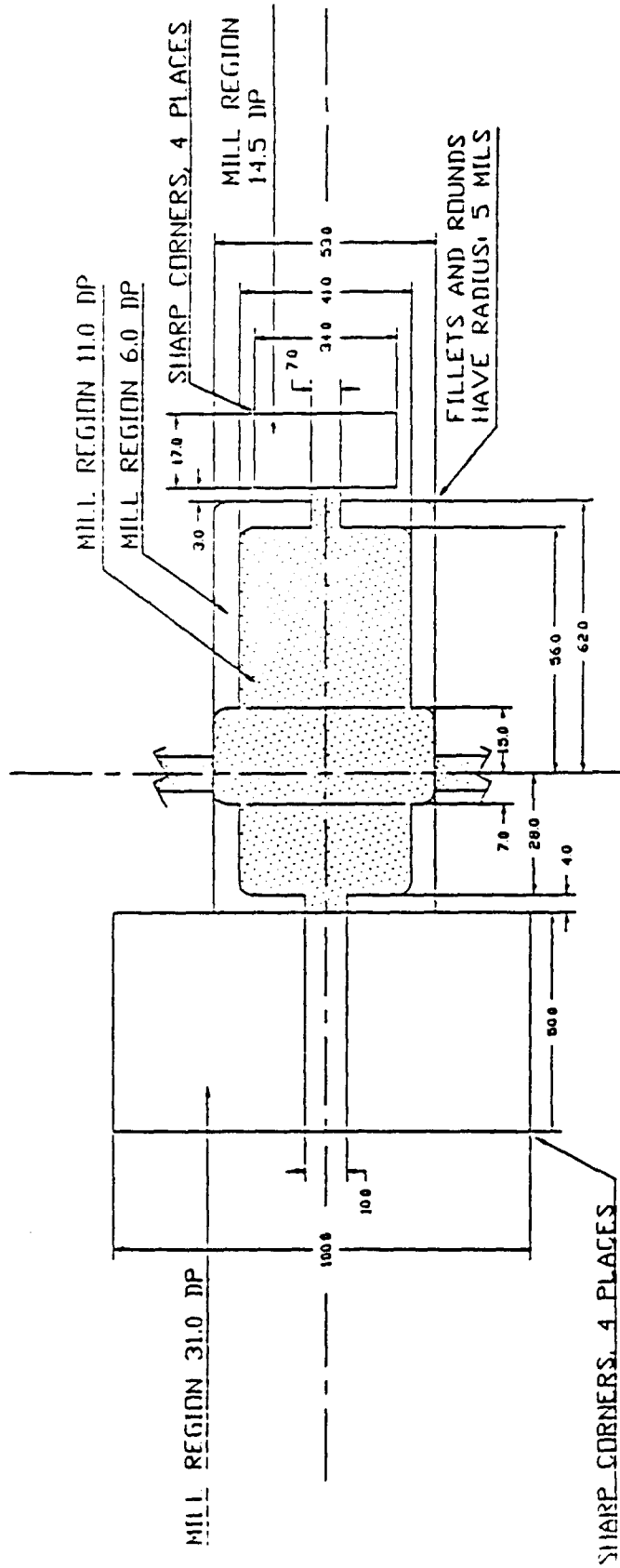
SCALE

NONE

DWG.

4-64765-034A

AS SHOWN



University of Virginia - SDI.

CHARLOTTESVILLE, VA. 22903

NAME BLOCK UPPER SECTION - BOTTOM VIEW

CLOSEUP OF CHIP AREA

PROJECT 80/240 GILZ MHC TRIPLER - MOUNTING BLOCK

TOLERANCE

XXX = ± 1.0

XXX.X = ± 0.5

DESIGN R.F.B.

DRAWN R.F.B.

SHEET 1 OF 1

SCALE NINE

COMPUTER

DATE

MATERIAL

FINISH

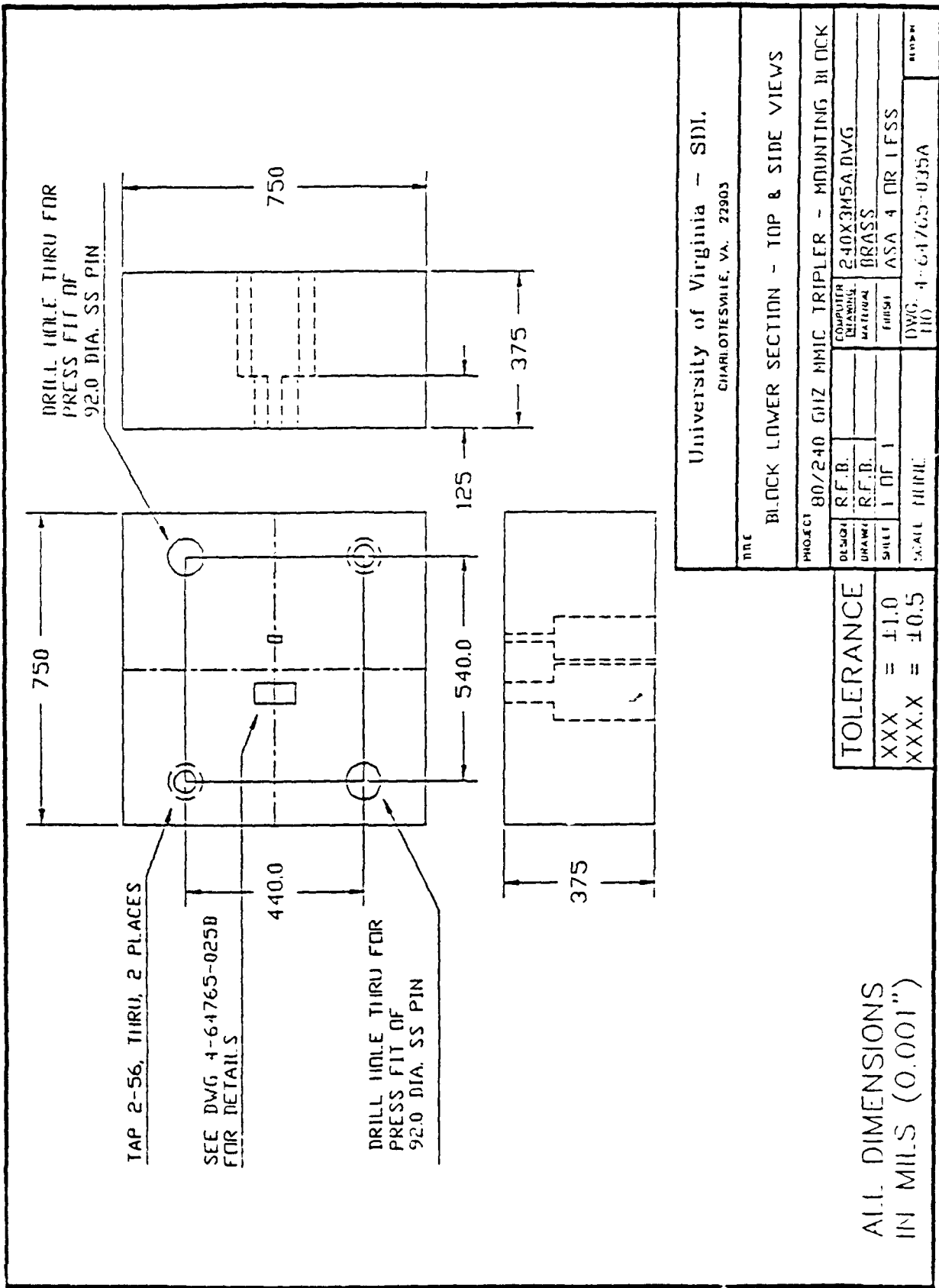
240X3M4B.DWG

BRASS

ASA 4 DR 1ESS

DWG. NO. 4-64765-034B

REVISION

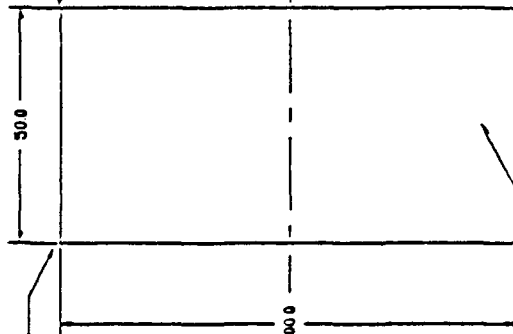


ALL DIMENSIONS
IN MILS (0.001")

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XXX.X	= ±0.5

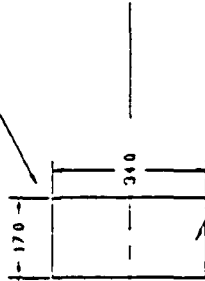
University of Virginia - SDI, CHARLOTTESVILLE, VA. 22903	
BLOCK LOWER SECTION - TOP & SIDE VIEWS	
PROJECT	80/240 GHz MMIC TRIPLER - MOUNTING BLOCK
DESIGN	R.F.B.
DATE	R.F.B.
SHEET	1 OF 1
SCALE	MMIC
COMPUTER	240X3M5A.DWG
MATERIAL	BRASS
FINISH	ASA 4 OR IFSS
DWG.	4-64765-035A
REV	110

SHARP CORNERS,
4 PLACES



MILL REGION 125 DP

SHARP CORNERS,
4 PLACES



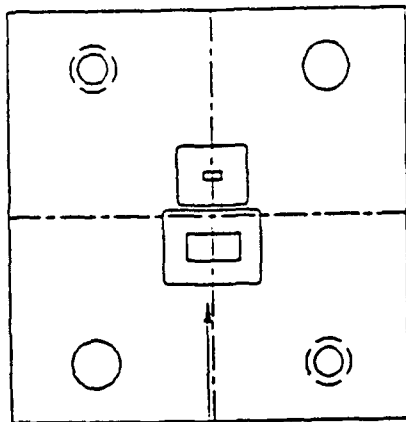
MILL REGION 125 DP

TOLERANCE
XXX = ±1.0
XXX.X = ±0.5

ALL DIMENSIONS
IN MILS (0.001")

University of Virginia - SDL, CHARLOTTESVILLE, VA. 22903		PROJECT 80/240 GHz MMIC TRIPLER - MOUNTING BLOCK	
TITLE BLOCK UPPER SECTION - BOTTOM VIEW		DESIGN R.F.D.	240X3M5B.DWG
CLOSEUP OF CHIP AREA		DRAWN R.F.D.	BRASS
		SHEET 1 OF 1	ASA 4 DR 1.5S
		SCALE NONE	DWG. 4-64765-035B
			REVISION

SEE DWG 4-64765-026B
FOR DETAILS

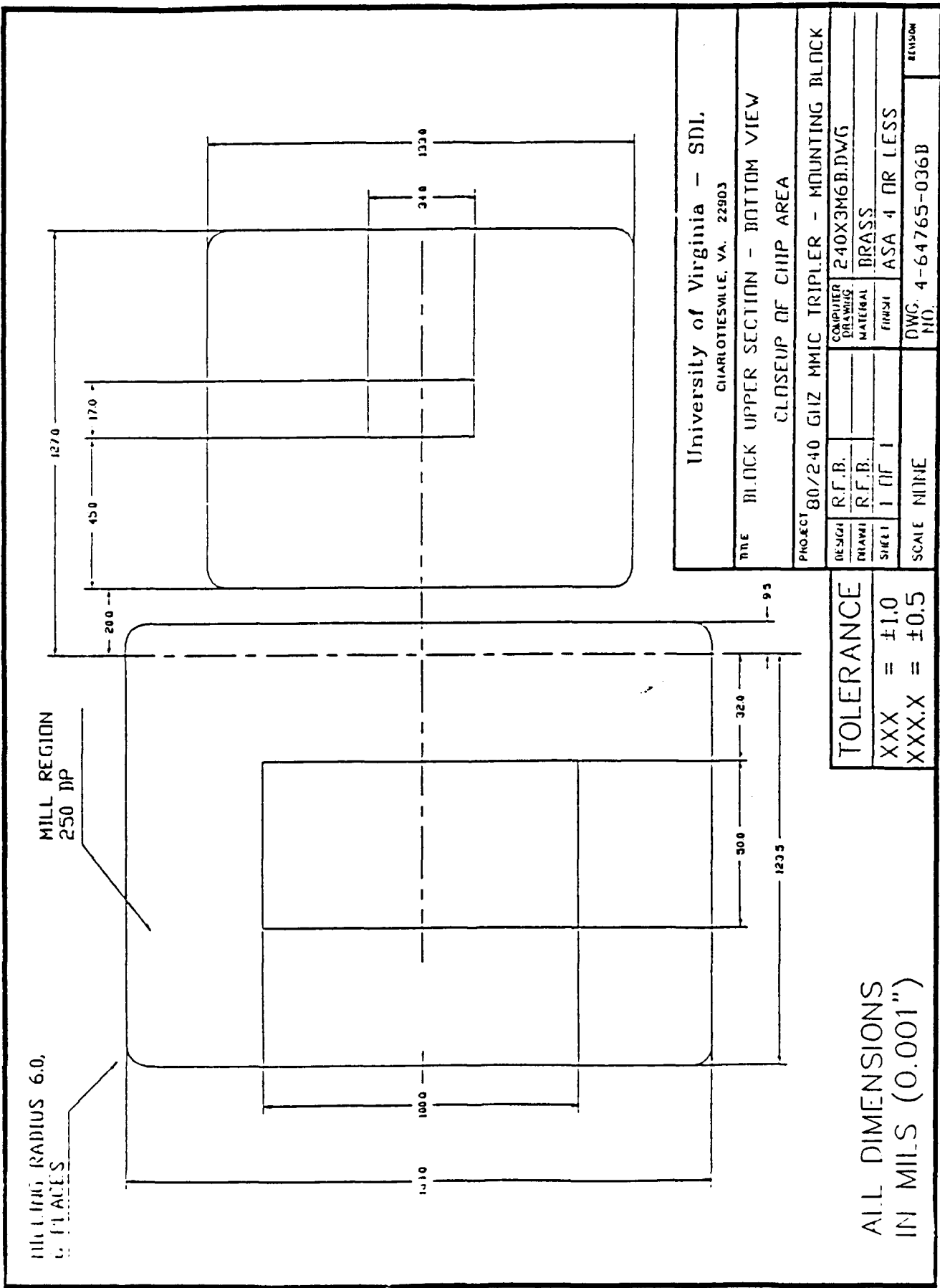


ALL DIMENSIONS
IN MILS (0.001")

TOLERANCE

XXX = ±1.0
XXX.X = ±0.5

University of Virginia - SDL CHARLOTTESVILLE, VA. 22903			
TITLE BLOCK LOWER SECTION - BOTTOM VIEW			
PROJECT 80/240 G12 MMIC TRIPLER - MOUNTING BLOCK		COMPUTER DRAWING 240X3M6A.DWG	
DESIGN R.F.D.	DATE R.F.D.	MATERIAL BRASS	
DRAWN J. D. I.	CHECKED J. D. I.	FINISH ASA 4 FIN 1 ESS	
SCALE NINE		DWG. NO. 4-64765-036A	
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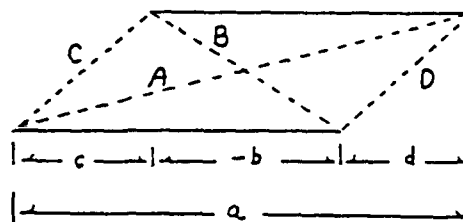
ALL DIMENSIONS
IN MILS (0.001")

APPENDIX I

Calculation of Mutual Inductance

This routine is used to calculate the mutual inductance between two filamentary currents.

REF: Ramo, Whinnery, and Van Duzer, "Fields and Waves in Communication Electronics", Wiley, NY, 1965, pp. 306-309.



Input Data:

Overall length of the two conductors:	a := 70	microns
Overlap length of the two conductors:	b := -30	microns
Left side extension:	c := 20	microns
Right side extension:	d := 20	microns
Conductor separation:	s := 20	microns

Preliminary calculations:

$$A := \sqrt{a^2 + s^2} \quad A = 72.801 \quad \text{microns}$$

$$B := \sqrt{b^2 + s^2} \quad B = 36.056 \quad \text{microns}$$

$$C := \sqrt{c^2 + s^2} \quad C = 28.284 \quad \text{microns}$$

$$D := \sqrt{d^2 + s^2} \quad D = 28.284 \quad \text{microns}$$

$$M1 := a \cdot \ln(A + a) + b \cdot \ln(B + b) - c \cdot \ln(C + c) - d \cdot \ln(D + d)$$

$$M2 := (C + D) - (A + B)$$

$$M := (M1 + M2) \cdot 10^{-4}$$

$$M = 0.009 \quad \text{nH}$$

APPENDIX J

Lossy Radial Transmission Line Equations

In this appendix, the voltage and current equations are derived for the radial transmission line that has resistive loss. Consider the incremental equivalent circuit for the radial line as shown in Fig. J.1.

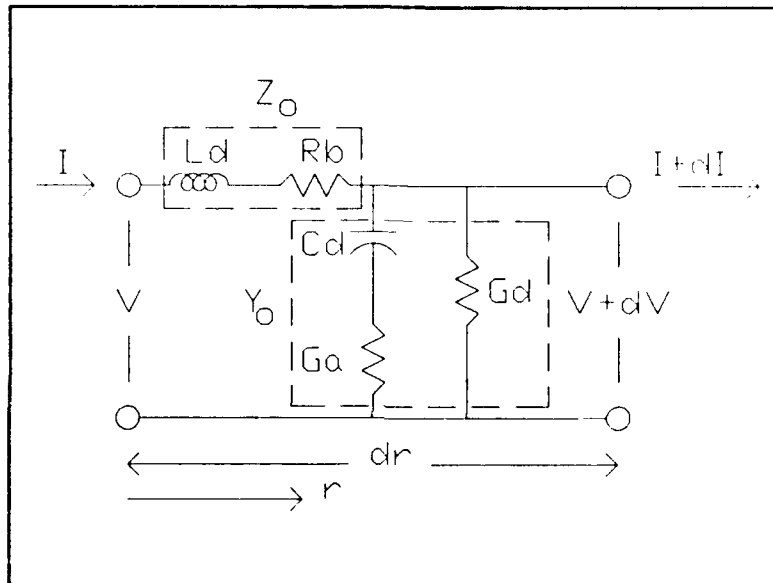


Figure J.1 The incremental equivalent circuit for the TEM radial transmission line.

In this case, Z_0 and Y_0 are the complex line impedance and admittance respectively, as described in Section 9.9.2. The impedance and admittance can be found by applying Maxwell's equations to the geometry of the line while assuming a θ -directed magnetic field and an axial or z -directed electric field. It is important to note that in the presence of resistive loss, $Z_0 \neq 1/Y_0$. Thus the radial line equations described by Montgomery (1948) and Marcuvitz (1951) (which assume a lossless line) are not applicable in this case and hence a more general set of line equations were derived.

Through the application of Kirchhoff's laws to the incremental equivalent circuit of Fig. J.1, the current and voltage along the TEM radial line must satisfy the following differential equations:

$$\frac{dV}{dr} = -jk_p Z_o I \quad (J-1)$$

$$\frac{dI}{dr} = -jk_p Y_o V \quad (J-2)$$

where

$$k_p = \omega \sqrt{\mu \epsilon} \quad (J-3)$$

with μ = permeability and ϵ = permittivity of the line. Note that V , I , Z_o , and Y_o depend on r . Eqns. (J-1) and (J-2) can be combined to form a second-order differential equation for the voltage and current as follows:

$$\frac{1}{Y_o} \frac{d}{dr} \left(\frac{1}{Z_o} \frac{dV}{dr} \right) + k_p^2 V = 0 \quad (J-4)$$

$$\frac{1}{Z_o} \frac{d}{dr} \left(\frac{1}{Y_o} \frac{dI}{dr} \right) + k_p^2 I = 0 \quad (J-5)$$

As seen from eqns. (9-14) and (9-15), $Z_o \propto 1/r$ and $Y_o \propto r$. Using this fact, eqns. (J-4) and (J-5) can be put into the form of Bessel's equation. Hence, eqn. (J-4) becomes:

$$\frac{1}{r} \frac{d}{dr} \left(r \frac{dV}{dr} \right) + \zeta^2 V = 0 \quad (J-6)$$

and similarly eqn. (J-5) becomes

$$r \frac{d}{dr} \left(\frac{1}{r} \frac{dI}{dr} \right) + \zeta^2 I = 0 \quad (J-7)$$

where

$$\zeta^2 = Y_o Z_o k_p^2 \quad (\text{J-8})$$

The form of the solutions to eqns. (J-6) and (J-7) is linear combinations of Bessel functions. Hence, the solution to the voltage eqn. (J-6) is of the form

$$V(r) = AJ_o(\zeta r) + BN_o(\zeta r) \quad (\text{J-9})$$

and the solution to the current eqn. (J-7) is of the form

$$-j \left[\frac{\sqrt{Z_o Y_o}}{Y_o(r)} \right] I(r) = AJ_1(\zeta r) + BN_1(\zeta r) \quad (\text{J-10})$$

where J_0 and J_1 are complex Bessel functions of order 0 and 1 while N_0 and N_1 are complex Neumann functions of order 0 and 1. A and B are constants to be determined. Eqn. (J-10) was found by substitution of eqn. (J-9) into (J-7) and recalling that

$$\frac{dJ_o}{dr} = -J_1 \quad (\text{J-11})$$

$$\frac{dN_o}{dr} = -N_1 \quad (\text{J-12})$$

The two unknown constants, A and B, require two boundary conditions for solution. The first boundary condition is on the voltage at radius r_o :

$$V(r_o) = AJ_o(\zeta r_o) + BN_o(\zeta r_o) \quad (\text{J-13})$$

The second boundary condition is on the current at r_o :

$$-j \frac{\sqrt{Y_o Z_o}}{Y_o(r_o)} I(r_o) = AJ_1(\zeta r_o) + BN_1(\zeta r_o) \quad (\text{J-14})$$

Solutions for A and B now follow directly.

First, solving eqn. (J-13) for A and substitution into eqn. (J-14) yields the equation for B as

$$B = \frac{j \frac{\sqrt{Y_o Z_o}}{Y_o(r_o)} J_o(\zeta r_o) I(r_o) + J_1(\zeta r_o) V(r_o)}{N_o(\zeta r_o) J_1(\zeta r_o) - N_1(\zeta r_o) J_o(\zeta r_o)} \quad (J-15)$$

Noting that

$$N_o(\zeta r_o) J_1(\zeta r_o) = J_1(\zeta r_o) \frac{d}{d(\zeta r_o)} N_1(\zeta r_o) + \frac{J_1(\zeta r_o) N_1(\zeta r_o)}{\zeta r_o} \quad (J-16)$$

and

$$J_o(\zeta r_o) N_1(\zeta r_o) = N_1(\zeta r_o) \frac{d}{d(\zeta r_o)} J_1(\zeta r_o) + \frac{J_1(\zeta r_o) N_1(\zeta r_o)}{\zeta r_o} \quad (J-17)$$

The solution for B is thus

$$B = \frac{j \frac{\sqrt{Y_o Z_o}}{Y_o(r_o)} J_o(\zeta r_o) I(r_o) + J_1(\zeta r_o) V(r_o)}{\frac{2}{\pi \zeta r_o}} \quad (J-18)$$

where the Wronskian relationship

$$J_1(\zeta r_o) \frac{dN_1}{d(\zeta r_o)} - N_1(\zeta r_o) \frac{dJ_1}{d(\zeta r_o)} = \frac{2}{\pi \zeta r_o} \quad (J-19)$$

has been used. Substitution of eqn. (J-18) into (J-13) yields the solution for A as

$$A = \frac{V(r_o)}{J_o(\zeta r_o)} - \left[\frac{j \frac{\sqrt{Y_o Z_o}}{Y_o(r_o)} N_o(\zeta r_o) I(r_o) + \frac{J_1(\zeta r_o) N_o(\zeta r_o) V(r_o)}{J_o(\zeta r_o)}}{\frac{2}{\pi \zeta r_o}} \right] \quad (J-20)$$

Finally, the solutions for the voltage $V(r)$ and current $I(r)$ along the radial line can be determined by substitution of eqns. (J-18) and (J-20) into (J-9), and then using the identity

$$J_o(\zeta r_o) = \frac{1}{\zeta r_o} \left[\zeta r_o \frac{dJ_1(\zeta r_o)}{d(\zeta r_o)} + J_1(\zeta r_o) \right] \quad (J-21)$$

yields the voltage equation (after much simplification):

$$V(r) = \left[\frac{J_1(\zeta r_o) N_o(\zeta r) - N_1(\zeta r_o) J_o(\zeta r)}{\frac{2}{\pi \zeta r_o}} \right] V(r_o) - j \frac{\sqrt{Y_o Z_o}}{Y_o(r_o)} \left[\frac{J_o(\zeta r) N_o(\zeta r_o) - J_o(\zeta r_o) N_o(\zeta r)}{\frac{2}{\pi \zeta r_o}} \right] I(r_o) \quad (J-22)$$

Similarly, substitution of eqns. (J-18) and (J-20) into (J-10) and using the identity (J-21) yields the current equation:

$$\frac{\sqrt{Y_o Z_o}}{Y_o(r)} I(r) = \frac{\sqrt{Y_o Z_o}}{Y_o(r_o)} \left[\frac{N_o(\zeta r_o) J_1(\zeta r) - J_o(\zeta r_o) N_1(\zeta r)}{\frac{2}{\pi \zeta r_o}} \right] I(r_o) - j \left[\frac{J_1(\zeta r_o) N_1(\zeta r) - N_1(\zeta r_o) J_1(\zeta r)}{\frac{2}{\pi \zeta r_o}} \right] V(r_o) \quad (J-23)$$

The above equations allow calculation of the line voltage and current when the voltage and current at $r = r_o$ (termination at r_o) is known.

APPENDIX K

Copy of paper by
T. Newman, W. Bishop, K.T. Ng, and S. Weinreb

A Novel Planar Diode Mixer for Submillimeter-Wave Applications

Tom Newman, *Member, IEEE*, William L. Bishop, *Associate Member, IEEE*,
Kwong T. Ng, *Member, IEEE*, and Sander Weinreb, *Fellow, IEEE*

Abstract—A novel mixer employing a planar GaAs Schottky diode has been designed and tested over a 300–365 GHz bandwidth at the University of Virginia (UVA). Using a planar diode eliminates the disadvantages of mechanical instability and labor-intensive assembly associated with conventional whisker-contacted diodes. The mixer design process used scale model impedance measurements both for the design of individual components and for the measurement of impedances presented to the diode terminals by the mixer mount at fundamental and harmonic frequencies. Results from these impedance measurements were then used in linear and nonlinear numerical mixer analyses to predict the mixer performance. To the best of our knowledge, this represents the first attempt at using a planar diode in a submillimeter-wave mixer, and test results indicate performance comparable with the best whisker-contacted room temperature mixers for submillimeter wavelengths.

I. INTRODUCTION

WHISKER-CONTACTED Schottky barrier diodes have been the preferred nonlinear elements for submillimeter-wave mixers for the last two decades. Planar versions of these diodes are more rugged and reliable, and can be more easily integrated into a circuit than their whisker-contacted counterparts, but they generally have had a formidable parasitic capacitance. The planar GaAs diodes used in this work, however, have an air-channel etched through the doped material between the anode and cathode bonding pads which substantially reduces this parasitic capacitance. The fabrication [1] and testing at 100 GHz [2] of these diodes have been described previously.

This paper describes a submillimeter-wave mixer designed for these diodes. A scale model was used in conjunction with the transverse resonance, finite differ-

ence, and spectral domain numerical techniques to design the individual components. The scale model was then used to measure impedances presented to the diode terminals by the mixer mount. These measured impedances were then used in nonlinear and linear mixer analyses to determine the theoretical mixer performance for two types of diodes. The intent was to present the optimum impedance to the diode terminals for each type of diode, thereby obtaining the lowest noise temperature and conversion loss, while maintaining minimal machining and fabrication requirements.

The mixer uses a novel coupling and tuning scheme from circular waveguide to shielded microstrip. Both the microstrip probe, which is printed on a quartz substrate, and the adjustable planar waveguide short circuit, which is used to tune the probe, are fabricated using photolithographic techniques. Hence they can be fabricated accurately to very small dimensions for applications at very high frequencies. The use of this coupling scheme, rather than those previously employed for waveguide mixers, reduces considerably the machining requirements for the mixer block. A target frequency range of 300–365 GHz was chosen for the design to test its feasibility in the submillimeter-wave range. The design should be useful up to a frequency at least as high as 700 GHz, when machining of the mixer block may start to present some problems.

II. MIXER BLOCK DESIGN

The mixer block design is shown in Fig. 1. The planar diode, shown in Fig. 2, consists of a block of semi-insulating GaAs topped with a thin doped epitaxial layer of GaAs. Two metal bonding pads are formed on top of the epitaxial layer, with a thin metal finger connecting the anode bonding pad to the Schottky anode. A channel is etched through the epitaxial layer between the two bonding pads, which substantially lowers the parasitic capacitance of the diode. The diode is mounted face down on a quartz substrate, as shown in Fig. 2(b), on which a microstrip circuit is formed in the mixer block. The externally combined local oscillator (LO) and RF signals are coupled into a circular waveguide through a dual-mode feedhorn [3], and then onto a microstrip by a waveguide probe tuned with a planar noncontacting adjustable short circuit. A noncontacting short circuit provides a more

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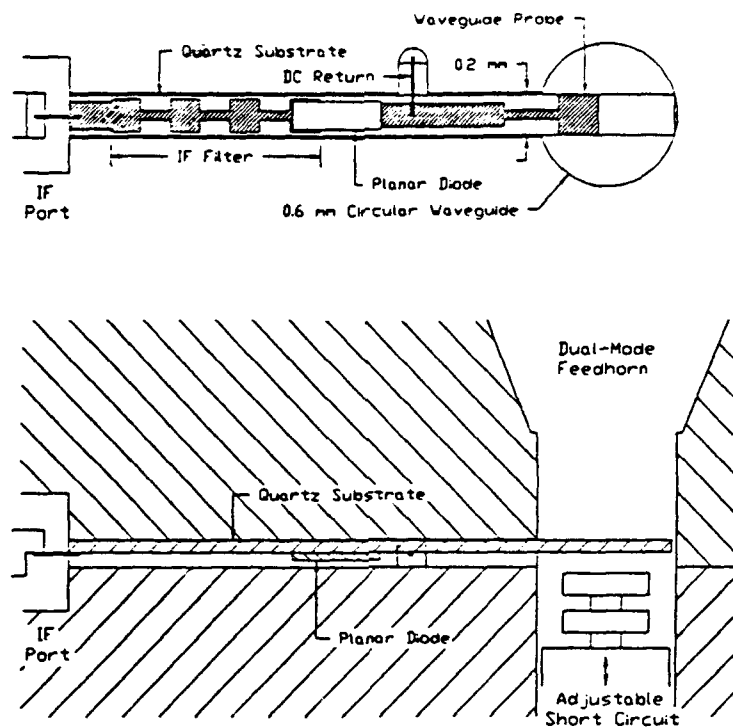


Fig. 1. Two cross sectional views of the submillimeter-wave planar diode mixer.

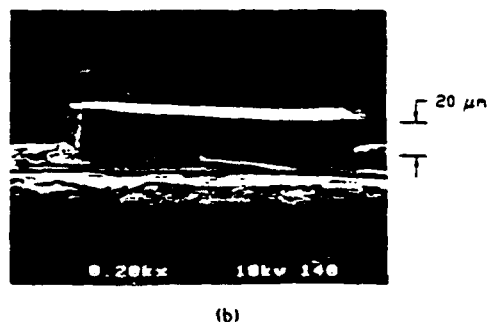
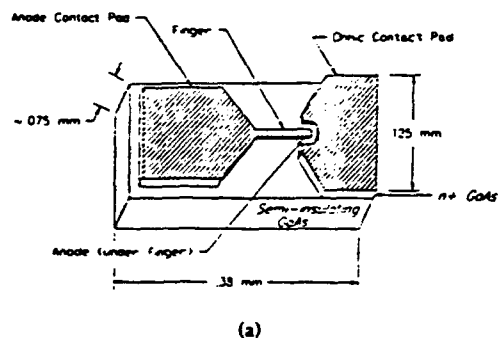


Fig. 2. (a) UVa planar diode geometry. (b) Scanning electron microscope photo of a planar diode which has been mounted face down on a quartz substrate and chemically thinned to a thickness of 0.02 mm.

repeatable short circuit than a contacting one at submillimeter wavelengths [4] and the planar version developed for this project can be accurately fabricated using photolithographic techniques. No transition to rectangular waveguide is used in the design, and no reduction in waveguide dimensions in the vicinity of the probe was found to be necessary. Using a circular waveguide and a dual-mode feedhorn allows the mixer block to be machined for use at submillimeter wavelengths but restricts the bandwidth to 25% or less. A quarter-wavelength long bond-wire connects the microstrip to ground between the diode and probe, and functions as a dc and IF return. Finally, a series of alternate high and low impedance quarter-wavelength microstrip sections between the diode and the IF port allow dc and IF power to pass through, but present nearly a short circuit in series with the diode at RF.

A. Microstrip Enclosure Design

An analysis was performed using transverse resonance and spectral domain techniques [5] to find a single mode microstrip enclosure with the largest possible cross sectional dimensions. The transverse resonance analysis was used to calculate the cutoff frequencies of waveguide modes with no metal strip present, and the more complex spectral domain technique was used to calculate cutoff frequencies with a metal strip present. Fig. 3 shows good agreement between the two analyses for narrow strips and shows the importance of using the spectral domain analysis in specifying enclosure dimensions when wide mi-

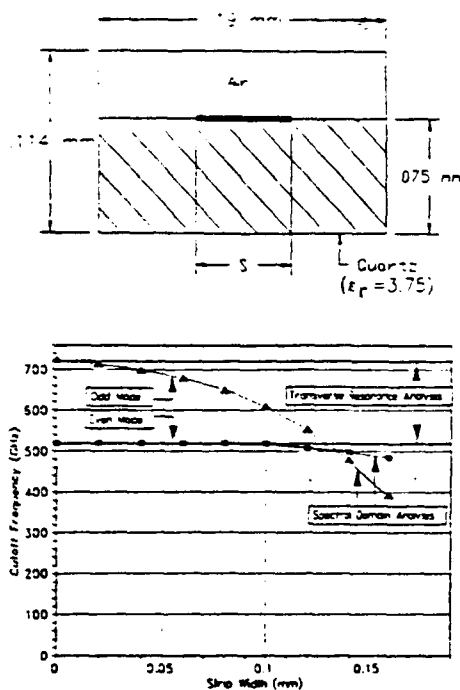


Fig. 3. Cutoff frequencies of the fundamental even and odd modes in shielded microstrip plotted as a function of strip width in an enclosure 0.19 mm wide by 0.114 mm high with a 0.075 mm thick quartz substrate.

crostrips are required. Cutoff frequencies are shown for two types of modes: 1) the lowest order even mode, which has a symmetric strip current distribution and becomes the LSM_{11} mode when there is no strip, and 2) the lowest order odd mode, which has an antisymmetric strip current distribution and becomes the LSE_{01} mode when there is no strip. In the present mixer, a quartz substrate of thickness 0.075 mm in a 0.114 mm $\times$ 0.19 mm enclosure with a 0.16 mm wide metal strip will support only a single mode for frequencies up to 390 GHz.

Maintaining single mode propagation in the shielded microstrip region is the prime determinant of the upper frequency limit for the design. Machining and handling will limit us to a 0.05 mm thick quartz substrate and a 0.07 mm $\times$ 0.135 mm enclosure, i.e., a milled slot 0.135 mm wide by 0.07 mm deep. Using this geometry with a 0.11 mm wide microstrip and with the GaAs layer thinned to 10 μ m using the techniques described in [6], the upper useful frequency for this design should be $\sim$ 700 GHz.

B. Chemical Thinning of Planar Diodes

Because the diode length is approximately one wavelength in the microstrip enclosure, the diode bonding pads should be considered as transmission line segments, rather than lumped impedances. The high dielectric constant of the GaAs substrate has the undesirable effect of lowering the cutoff frequencies of higher order modes which may propagate through the diode region. However,

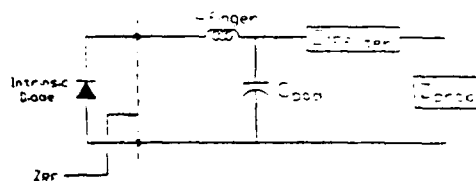


Fig. 4. RF circuit model used to obtain the impedance seen from the diode terminals. $Z_{IFilter}$ and Z_{probe} represent respectively the impedances of the IF filter and probe transition into the input waveguide.

by mounting the diode face down firmly onto a lower dielectric constant material such as quartz and etching most of the GaAs substrate from the back of the diode, the cutoff frequencies of the higher order modes were raised without compromising the physical integrity of the diode. Chemical etching has been used [6] to thin GaAs diodes to less than 5 μ m thick, but a thickness of 12 μ m was found to be sufficient to keep higher order modes from propagating. Before chemical etching could begin, the sides of the diode had to be covered to prevent the etchant from attacking the active material around the Schottky contact. This was accomplished with Apiezon-W black wax [7] which was thinned with the solvent, trichloroethane, to the point that, when a drop was brought into contact with the diode, it flowed around all four sides of the diode but not over its top, forming a meniscus due to surface tension. Once the wax had dried it was impervious to most peroxide GaAs etchants and, after etching was completed, the wax was removed with TCE. A mounted and chemically thinned planar diode is shown in Fig. 2(b).

III. SCALE MODEL DESIGN OF COMPONENTS

Large scale models of submillimeter-wave circuits allow measurement and optimization of the circuit using a microwave network analyzer. In scaling the dimension of a circuit by a factor S , the electrical characteristics of the circuit are shifted by $1/S$ in frequency (this is not generally true of conductor or dielectric loss). In the present work a scale factor $S = 45$ was used. The scale model design of the probe transition from the circular waveguide to the 50 Ω shielded microstrip, as shown in Fig. 1, was described in [8] and updated in [9], where the model design for the IF filter is also presented. The IF filter consists of a microstrip with alternating quarter-wavelength high and low impedance sections achieved by varying the microstrip width. Each section was shortened by 4% from the nominal quarter-wavelength to compensate for the fringing inductance associated with the abrupt change in width. Values were also obtained for the major parasitic elements associated with the planar diode geometry, namely the capacitance between the bonding pads, C_{pad} , and the inductance of the finger connecting the pads, L_{finger} . The results of the scale model measurements were used to derive values for the RF circuit model

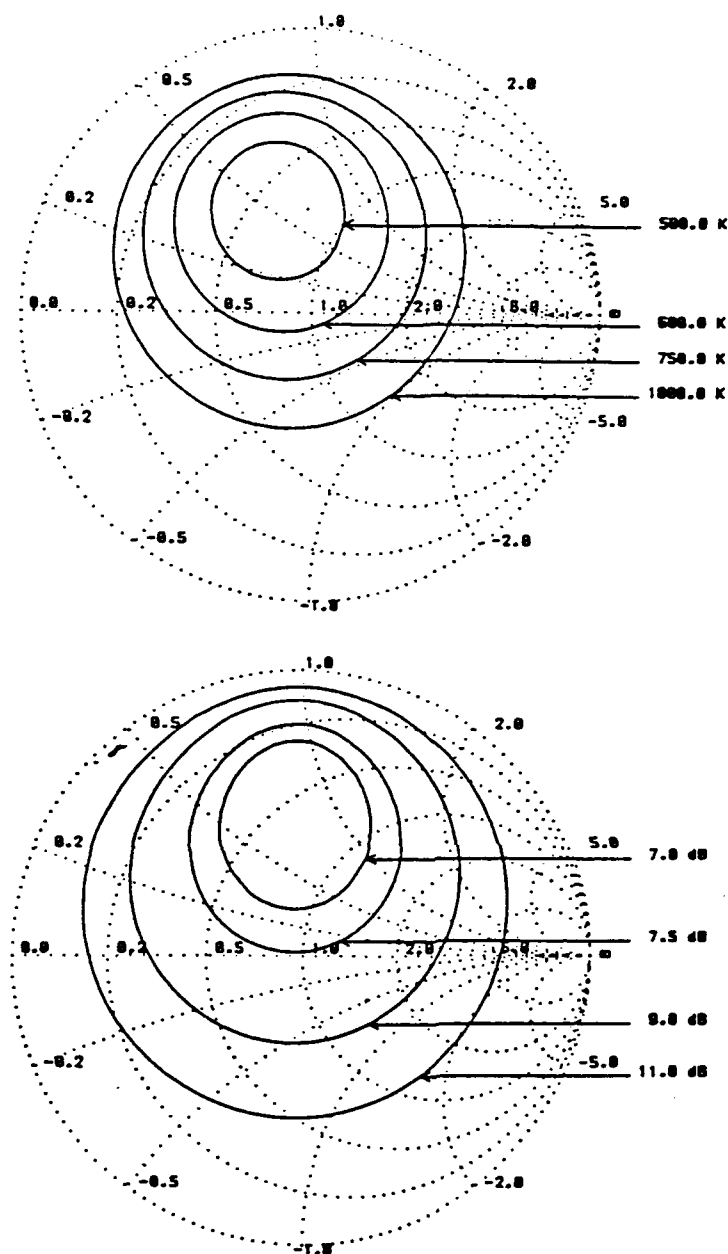


Fig. 5. Smith chart plots showing contours of constant mixer noise temperature (DSB) and conversion loss (SSB) at 345 GHz as a function of the embedding impedance at the diode terminals for a UVa SC2R4 diode with a total series resistance of 13 Ω and junction capacitance of 6.8 fF. The diode is assumed short circuited for $f > f_{LO} + f_{IF}$.

of the mixer block, shown in Fig. 4, from which the impedance presented to the terminals of the diode at the RF, Z_{RF} , could be calculated. The impedances of the IF filter, $Z_{IFfilter}$, and the waveguide probe, Z_{probe} , were modified to account for the transmission line length of the diode bonding pads and microstrip lines in front of these elements. Adjustments were made to the circuit elements by varying the diode geometry i.e., changing L_{finger} and C_{pad} , and by changing the length of the microstrip transmission line between the diode and the IF filter. In this way the design was tuned to match Z_{RF} to

an optimum value calculated for a set of measured diode parameters as described below.

IV. DIODE EMBEDDING CIRCUIT OPTIMIZATION

Providing the correct embedding impedance, Z_{RF} , seen from the intrinsic diode terminals is of primary importance in mixer design. The analysis method described in [10], [11] was employed for calculating mixer noise temperature and conversion loss as functions of Z_{RF} . This analysis includes the effects of nonlinear diode junction

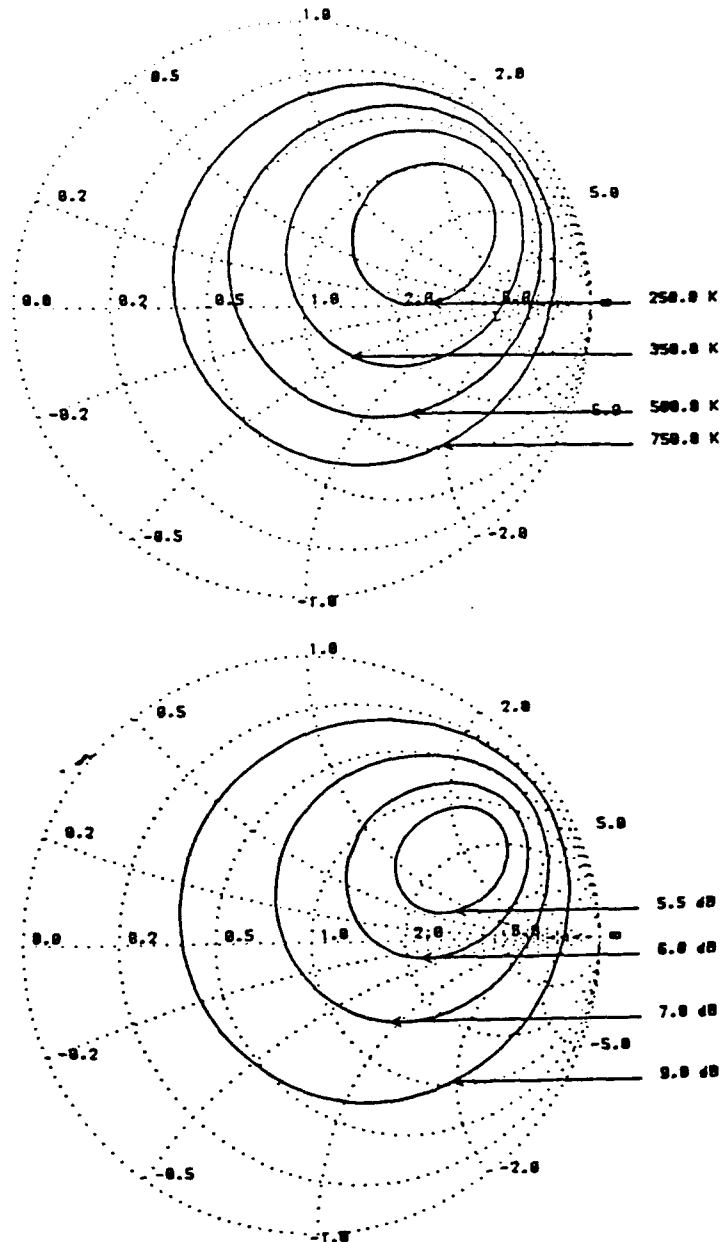


Fig. 6. Smith chart plots showing contours of constant mixer noise temperature (DSB) and conversion loss (SSB) at 345 GHz as a function of the embedding impedance at the diode terminals for a UVa SC2T1 diode with a total series resistance of 23 Ω and junction capacitance of 2.4 fF. The diode is assumed short circuited for $f > f_{LO} + f_{IF}$.

capacitance and resistance as well as shot and thermal noise generated in the diode. For analysis purposes, the diode was assumed to be terminated with short circuits at the LO harmonics and at harmonic sidebands, $nf_{LO} \pm f_{IF}$. Also the fundamental sideband impedances, $Z_{RF}(f_{LO} \pm f_{IF})$, were assumed equal, and the IF load impedance was assumed perfectly matched to the IF port. Figs. 5 and 6 show Smith chart plots of calculated contours of constant mixer noise temperature (double sideband, DSB) and conversion loss (single sideband, SSB) over all possible values of Z_{RF} . The analysis was performed at a frequency

of 345 GHz for two UVa diode types designated as SC2R4, which has a 2.5 μm anode diameter, and SC2T1, which has a 1.5 μm anode diameter. The SC2R4 diodes have a dc series resistance of 8 Ω and zero-bias junction capacitance of 6.8 fF, and the SC2T1 diodes have a dc series resistance of 15.5 Ω and zero-bias junction capacitance of 2.4 fF. An additional series resistance calculated in [12] was added to account for the skin effect in the GaAs chip at 345 GHz, which amounts to 5 Ω for the SC2R4 diodes and 7.5 Ω for the SC2T1 diodes. It is seen that the lower junction capacitance SC2T1 diodes have

less noise and higher conversion efficiency than the SC2R4 diodes.

The element values needed to produce an optimum embedding impedance, Z_{RF} in Fig. 4, for a particular type of diode were then determined. A 50 μm finger length between diode bonding pads was found necessary for both diode types. The cathode bonding pads of the SC2R4 diodes (used as the first low impedance section of the IF filter) were reduced from 0.10 mm to 0.035 mm to give the desired impedance of $30-j40\ \Omega$. This was accomplished by trimming the length of the bonding pad with a dicing saw. No such modification of bonding pad length for the SC2T1 diodes was required to give the desired impedance of $110+j115\ \Omega$.

To verify that the impedance presented to the diode terminals was equal to that calculated from the RF circuit model at both the fundamental and higher harmonic frequencies, measurements were made on the mixer scale model. Scale models used to design individual mixer components (i.e., IF filter, waveguide probe, and dc return) were constructed in a modular fashion to allow subsequent coupling together for assessment of the interactions between them. The technique of Eisenhart and Kahn [13] was used in which a miniature coaxial cable was positioned to run into the model as the dc return line and then along the microstrip to the gap between the diode bonding pads. The outer conductor of the cable was soldered to the microstrip up to one bonding pad and its inner conductor was soldered to the other bonding pad. No actual diode was used. A network analyzer was then connected to the coaxial cable with the reference plane extended to the end of the coaxial shield (the position of the diode junction in the actual mixer), and measurements were made of Z_{RF} . After making a correction to the measured data to account for a difference in the capacitance of the opened coaxial line and the capacitance of the junction region of the mounted diode, good agreement (within 10 Ω) was found between Z_{RF} calculated from the RF circuit model and Z_{RF} measured directly from the mixer scale model. Impedances at the second and third harmonic frequencies were then measured and the mixer analysis in [11] was carried out to determine their effects on the conversion loss and noise temperature. This analysis revealed that the impedances at frequencies above the fundamental play a relatively minor role in this mixer's performance. In the worst case, with the impedances at the second and third harmonics representing 50 Ω terminations, there is an increase of approximately 1 dB in noise temperature and conversion loss over the values shown in Figs. 5 and 6 which were calculated with these impedances as short circuits.

V. MIXER PERFORMANCE

The mixer block was constructed of brass in two $0.25 \times 1.0 \times 1.0$ inch halves. Details on the construction are described in [14]. Noise temperature and conversion loss of the mixer were measured from 300 to 365 GHz at room

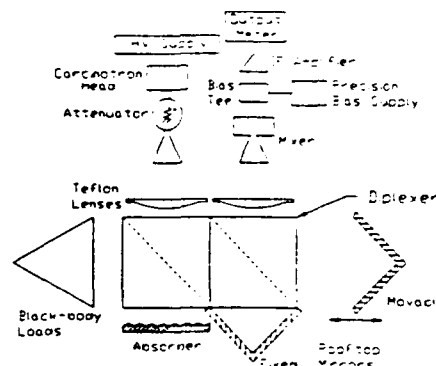


Fig. 7. Measurement set-up for 300-360 GHz mixer.

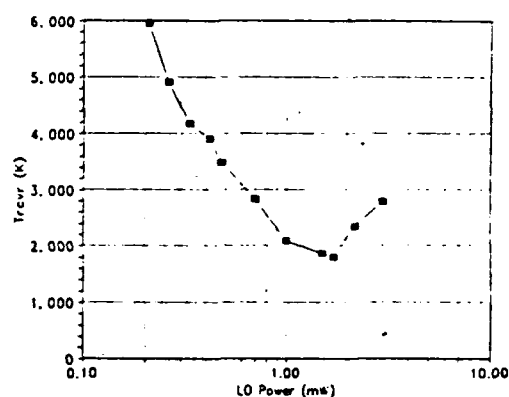


Fig. 8. Typical relation between noise performance (DSB) and LO pump power.

temperature for two types of diodes, SC2R4 and SC2T1. The measurement arrangement is shown in Fig. 7. A carcinotron [15] was used as the LO and a Martin-Puplett interferometer was used as a quasi-optical diplexer [16], [17]. Noise temperature and conversion loss measurements were made with room temperature and liquid nitrogen temperature black body sources. The 1.4 GHz IF portion of the test system is similar to that used in [2]. Optimal LO pumping was found to be obtained at about 1.4 mW measured at the mixer feedhorn position with a quasi-optical power meter [18], and optimal dc biasing was obtained for both diodes at about 0.8 V and 1.5 mA. Fig. 8 shows the typical relation between noise temperature (DSB) and LO power. The mixer response in both sidebands was assumed equal in calculating the SSB conversion loss. A 3:1 IF impedance transformer was used to match the IF output impedance to the IF test system. The IF mismatch factor was calculated from measurements on noise power reflected at the IF output, and was used to correct the measured mixer performance data. Additional corrections were made to the data to account for a 0.4 dB RF optical path loss due to the teflon lens, and for the discrepancy of 8° K between Planck's radiation law and the Rayleigh-Jeans approximation at 345 GHz in specifying the power radiated from the black body sources.

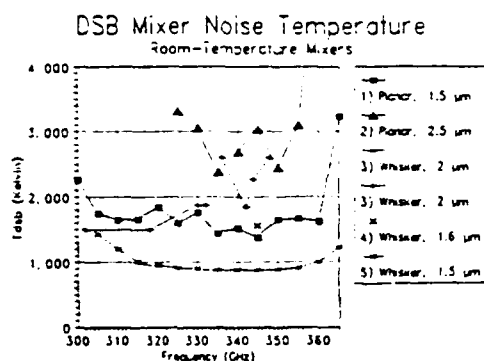


Fig. 9. Double sideband mixer noise temperature for the planar diode mixers using 1) SC2T1 diodes and 2) SC2R4 diodes. Also shown are mixer noise temperatures for other room-temperature Schottky barrier diode mixers: 3) two mixers using diodes with $\sim 2 \mu\text{m}$ anodes [20]; 4) a mixer using a diode with a $1.6 \mu\text{m}$ anode [21]; and 5) a mixer using a diode with a $1.5 \mu\text{m}$ anode [22].

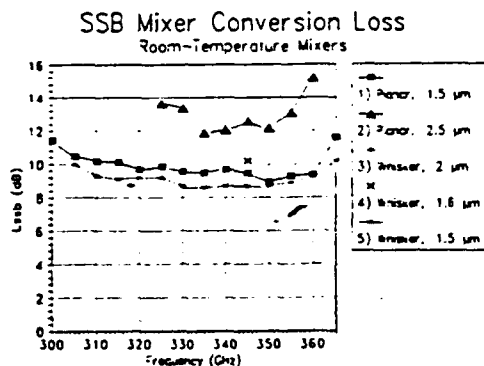


Fig. 10. Single sideband conversion loss for the planar diode mixers using 1) SC2T1 diodes and 2) SC2R4 diodes. Also shown are conversion losses for other room-temperature Schottky barrier diode mixers: 3) two mixers using diodes with $\sim 2 \mu\text{m}$ anodes [20]; 4) a mixer using a diode with a $1.6 \mu\text{m}$ anode [21]; and 5) a mixer using a diode with a $1.5 \mu\text{m}$ anode [22].

Figs. 9 and 10 show the noise temperature and conversion loss of the mixer measured at room temperature. The difference between the SC2R4 diode mixer and the SC2T1 diode mixer is about 900 K in noise temperature and 2.5 dB in conversion loss. The tunable bandwidth is much wider for the SC2T1 diode mixer due to the compensation technique used to impedance match the SC2R4 diode mixer. This resulted in a larger variation in IF filter impedance over frequency. At 345 GHz the SC2T1 diode exhibits an equivalent input noise temperature of 1370 K DSB and a conversion loss of 9.5 dB SSB. The mixer shows a useful tunable frequency range of over 20%. Both mixers exhibit about 5 dB higher noise temperature and conversion loss than the theoretical optimum values shown in Figs. 5 and 6. Up to a 1 dB increase is expected from the non-zero impedance of the higher order harmonics. An additional ~ 1 dB increase is due to losses in the waveguide and microstrip. A further ~ 1 dB increase is due to the noise contribution from the LO at the signal

and image frequencies. The remaining discrepancy is probably due to the omission of hot electron noise, intervalley scattering, and high frequency transport effects in the theoretical analysis [19]. Also shown in Fig. 9 are some of the best room-temperature mixer results reported for this frequency range [20]–[22]. These earlier results were obtained with whisker-contacted diodes in substantially different mounts, all using UVa diodes. These results show that the performance of the planar diode mixer is comparable with the best room temperature whisker-contacted diode mixers.

VI. CONCLUSION

Numerical analyses and scale model measurements have been combined effectively to yield a useful, rugged submillimeter-wave mixer design whose performance at 300–365 GHz is competitive with the best whisker-contacted type mixers made to date. This marks the first time a submillimeter-wave mixer has been designed and tested using a planar diode. The mixer block design is scalable to ~ 700 GHz with the same machining techniques used here for 365 GHz.

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