OFFICE OF NAVAL RESEARCH

FINAL REPORT

for

Contract N00014-86-K-0668

R&T No. S40001SRF02

June 1, 1986-December 31, 1991

"STRUCTURE AND RELIABILITY OF METAL CONTACTS TO GaAs"

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PROJECT HIGHLIGHTS

The project was aimed at understanding the **fundamental contact formation** mechanisms at metal/GaAs contacts, with the ultimate goal of developing structures that are **stable and reliable**. The approach was to combine electrical and microstructural characterization of as-deposited, thermally annealed and electrically stressed contacts, prepared in well-defined conditions. Strong emphasis has been placed on investigating the device degradation mechanisms in metal/III-V contacts. Devices were prepared by a variety of deposition methods. Atomically clean interfaces were formed using in-situ deposition of metals in ultra-high vacuum (UHV) onto freshly cleaved bulk GaAs(110) and MBE-grown GaAs(100) surfaces. Interfaces with controlled levels of contamination were prepared on air-exposed cleaved GaAs(110) and on chemically prepared GaAs(100) surfaces. High-resolution and analytical electron microscopy were used to determine the microstructure of the same contacts which were characterized using electrical device measurements.

Interfacial contamination was found to cause several degradation in the electrical and structural properties of the interfaces upon electrical and thermal stressing. In-situ UHV-prepared contacts thus provide a benchmark for the highest contact reliability of a particular metal/semiconductor system. Lattice matching is found to relate to the semiconductor lattice in the case of clean interfaces, but to the lattice of an oxide layer in the case of contaminated interfaces.

With the exception of metallization by a cluster deposition technique, **the stoichiometry of GaAs just adjacent to the metal layer** shows a change towards As-rich conditions, with a clear correlation between the Schottky barrier height and the amount of near-interfacial excess As. The barrier height of metals which react preferentially with As (e.g., Ti and Al) increases upon thermal annealing, while the barrier height of metals which react preferentially with Ga (e.g., Au) decreases.

Improvements in thermally stable Schottky contacts using conventional integrated circuit processing technology were found by using special substrate surface cleaning methods. As part of an effort to identify the most stable and reliable contacts to GaAs, we have investigated **refractory**

metal and metal nitride contacts. The stability of refractory metal Schottky contacts is limited due to reactivity with Ga and As, which also changes the near-interfacial stoichiometry and thus the barrier height. However, refractory metal nitrides suppress interfacial reactions at up to 800°C or more. In the case of ZrN, residual oxide was identified as the final failure mechanism upon 800°C heat treatment.

BACKGROUND

A key factor impeding broad utilization of GaAs integrated circuits is the lack of reliable metallization techniques. For semiconductor devices, two types of metal/semiconductor contacts are used: Ohmic contacts which connect the outside world to the active portion of the device and rectifying contacts which utilize the properties of the depletion region to achieve the device function, e.g., as gate contacts in field effect transistors, or for charge collection in detectors and solar cells. Despite their widespread use, two important issues remain to be resolved: the basic mechanism responsible for the observed Schottky barrier heights and the reproducibility and stability of electrical performance during annealing and aging. An unstable interface invariably results in barrier height changes and increased leakage currents for Schottky contacts and unpredictable contact resistance for Ohmic contacts. This results in unacceptable device performance at the chip level.

The problem of stable and reliable metalization of semiconductor devices is still a critical issue in device technology. For some device fabrication sequences, such as the self-aligned gate technology, the contact properties must be reliable and reproducible after heat treatment at 800°C or higher during the anneals which activate ion-implanted dopants. Also, as device dimensions decrease, more stringent constraints are placed on the properties of the metal contacts. For example, very tight control of interdiffusion and reactions at the metal-semiconductor interface is required to prevent metallic protrusions through and defect formation in the active regions of the smaller devices. In addition, the RC time constant of high-density circuits is often limited by contact and interconnect resistances.

PROJECT RESULTS

The increasing demands on contact reproducibility and stability require a thorough understanding of the fundamental contact formation mechanisms and of the factors that limit contact stability. Under this contract, we have made important and pioneering contributions to addressing these two questions for metal contacts on GaAs: we obtained clear evidence that near-interfacial stoichiometry decisively influences the Schottky barrier formation and that interfacial contamination is, in most cases, the cause of limited contact stability.

To address these two questions, we investigated Au, Ag, Al and Cr. We compared the structure, electrical properties and stability of electrical properties of "ideal" contacts deposited in-situ in UHV on cleaved GaAs(110) with contacts deposited on air-exposed GaAs(110) and in some cases with industrially prepared GaAs(100) contacts. We will describe in detail our results for four different systems: Au, Ag, Al and Cr on GaAs.

The structure and electrical properties of all contacts on GaAs were investigated by analytical and high-resolution transmission electron microscopy (TEM), combined with electrical characterization. Electron microscopy was performed at LBL's National Center for Electron Microscopy in Berkeley, using the JEOL JEM 200CX electron microscope equipped with a high-resolution pole piece (~0.25 nm point-to-point resolution) and the 1-MeV Atomic Resolution Microscope (ARM), which has a point-to-point resolution of ~0.16 nm.

Structure of Au Contacts

The as-deposited Au layer was found to be polycrystalline in all three cases, with grain diameters in the 10-50 nm range. The largest grain size was found in UHV-deposited Au samples. Some of these grains were twinned along (111) planes. Such unannealed Au layers observed in cross sections show atomically flat interfaces with GaAs.

Significant differences between these samples occur after annealing in N_2 at 405°C for 10 min (Fig. 1). For UHV-cleaved samples, the interface remains flat and abrupt despite annealing.

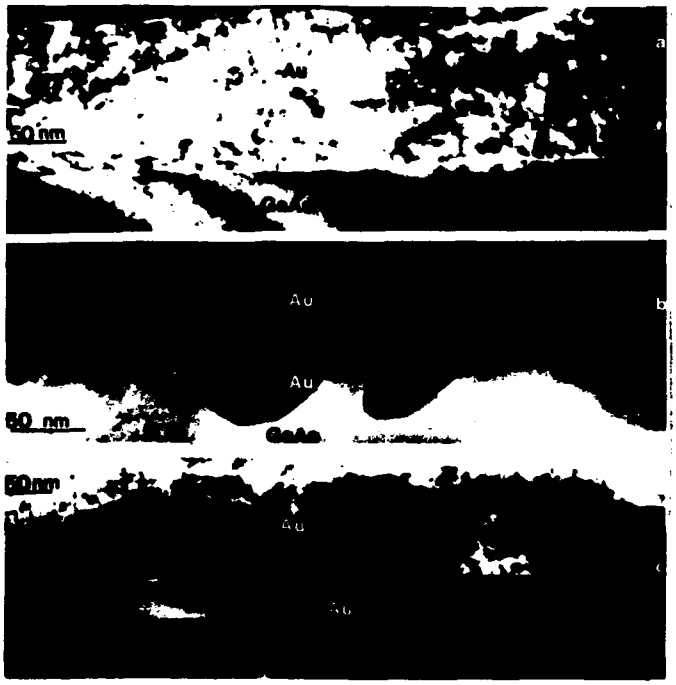


Fig. 1. Cross sections of annealed Au/GaAs interfaces. (a) Au deposited in situ on UHV-cleaved GaAs, (b) Au deposited on GaAs cleaved in air, (c) Au deposited on chemically clean GaAs.

In many cases triangular features elongated along $[011]_{GaAs}$ were observed. These features, probably voids, were formed in the Au layer directly adjacent to the GaAs substrate [Fig. 2a]. High-magnification images using the ARM showed that these areas consisted of amorphous material with embedded gold particles [Fig. 2b]. The same annealing treatment for the Au samples deposited on GaAs cleaved in air resulted in the formation of metallic protrusions at the interface [Fig. 1(b)].

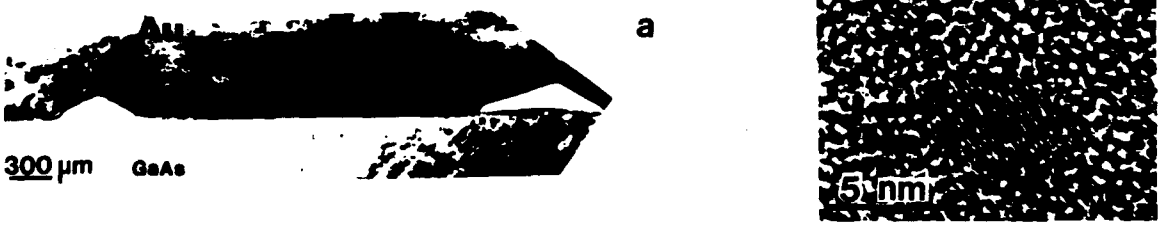


Fig. 2. (a) TEM micrograph of cross section of Au/GaAs interface from the samples prepared in situ in UHV on cleaved GaAs after annealing in N_2 at 405°C for 10 min. The image was taken in the [011] zone axis. Note void-like triangular features formed in Au adjacent to the GaAs substrate. (b) A high-magnification image of these triangular areas shows embedded Au particles inside the triangular areas.

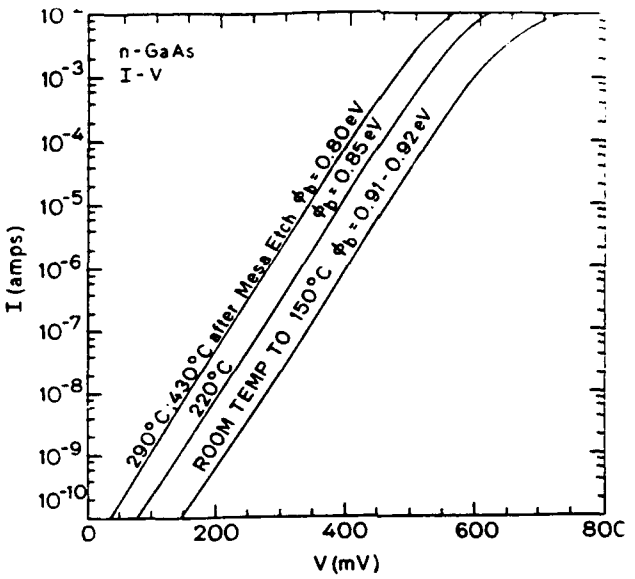
Two different shapes of protrusions were found extending into the GaAs [Fig. 1(b)]: (1) triangular protrusions whose sides are delineated by GaAs {111} planes, and (2) multifaceted protrusions delineated by GaAs {111}, {110}, and {100} planes. These two different protrusion shapes are probably related to the two different grain shapes visible in plan-view samples.

Even more complicated interfaces were observed in annealed Au/GaAs formed on chemically prepared GaAs surfaces. The gold layer was separated from the GaAs substrate by a thin oxide band (Fig. 1(c)). Oxygen was detected on the interface by energy-dispersive x-ray spectroscopy (EDX) in chemically prepared samples and in the samples cleaved in air[1]. Oxygen was not detected in samples where Au was deposited in situ on the UHV-cleaved surface. In many areas, the interface was very flat and abrupt (Fig. 1(c)). However, islands of gold with a wide range of shapes were found below the oxide layer as well. These islands were epitaxially regrown, with a much smaller defect density than in the layer above the oxide. The observation of separated islands below the oxide layer suggests that Au diffused through already existing pinholes in the oxide. The Au layer above the oxide layer has many defects, and the grain size is much smaller than that of the annealed Au deposited in UHV.

These observations show that GaAs is very sensitive to oxidation and that the morphology of the interface is strongly influenced by the surface preparation prior to Au deposition. This demonstrates that the formation of protrusions is not the result of annealing at elevated temperatures alone but is clearly affected by the semiconductor surface-preparation technique prior to metal deposition.

Electrical characterization of Au contacts

As determined from I-V characteristics, there was not a large difference in barrier height between Au diodes deposited in situ on UHV-cleaved GaAs samples (0.92 eV) [Fig. 3a] and those deposited on the samples cleaved in air (0.86 eV) [Fig. 3b]. After annealing, the barrier height decreased to 0.72 eV for both kinds of samples. A very important observation[2] is that those samples that were air-exposed before Au deposition were found to age with time and/or exposure to electrical measurements where large bias voltages were used, whereas UHV-cleaved samples were stable. This observation has important implications for the reliability of practical devices built on oxidized surfaces.



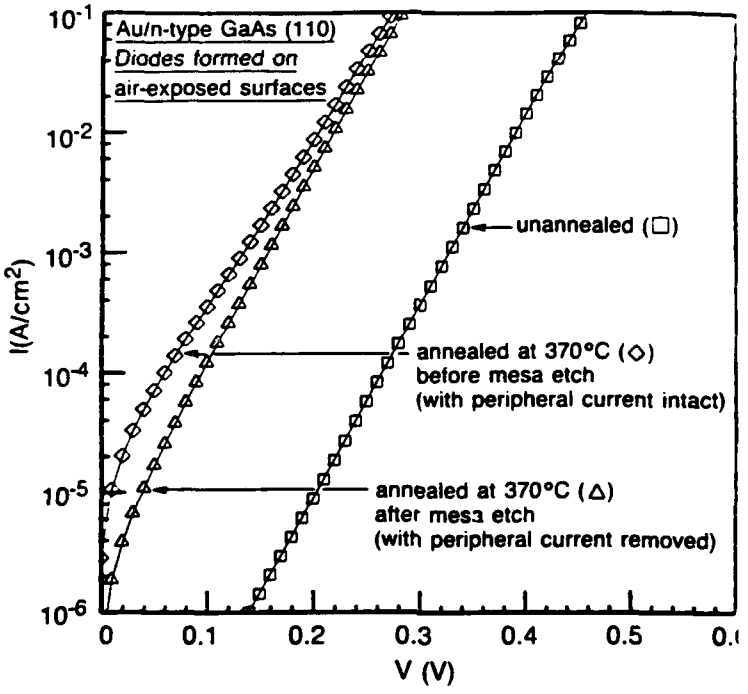


Fig. 3 I-V characteristics of Au metal contacts before and after annealing for metal deposited a) on UHV-cleaved GaAs and b) on air-exposed GaAs surface.

Structure of Ag contacts

Two kinds of Schottky diodes, similar to the first two kinds of Au diodes, were prepared for Ag deposited on clean, UHV-cleaved (110) GaAs, and deposited on air-exposed cleaved (110) substrates.

The structures of the two kinds of contacts differed significantly. The metal/substrate interface was flat in both cases (Figs. 4a and 4c) for as-deposited samples: however, in the air-exposed samples an oxide layer ~40Å thick was present on the GaAs surface. This oxide layer varied in thickness along the interface. The air-exposed diodes contained a higher density of twins and much smaller Ag grains in the metal layer than did the samples deposited in UHV conditions. As with Au, these two kinds of samples differed in interface morphology after annealing. The interface remained flat in the UHV samples, and high-resolution electron microscopy showed that $\{111\}_{Ag}$ planes were rotated slightly toward the $\{200\}_{GaAs}$ planes (Fig. 4b). Large protrusions were formed at the interface of the air-exposed samples (Fig 4d). The faceted Ag protrusions grew into the GaAs.

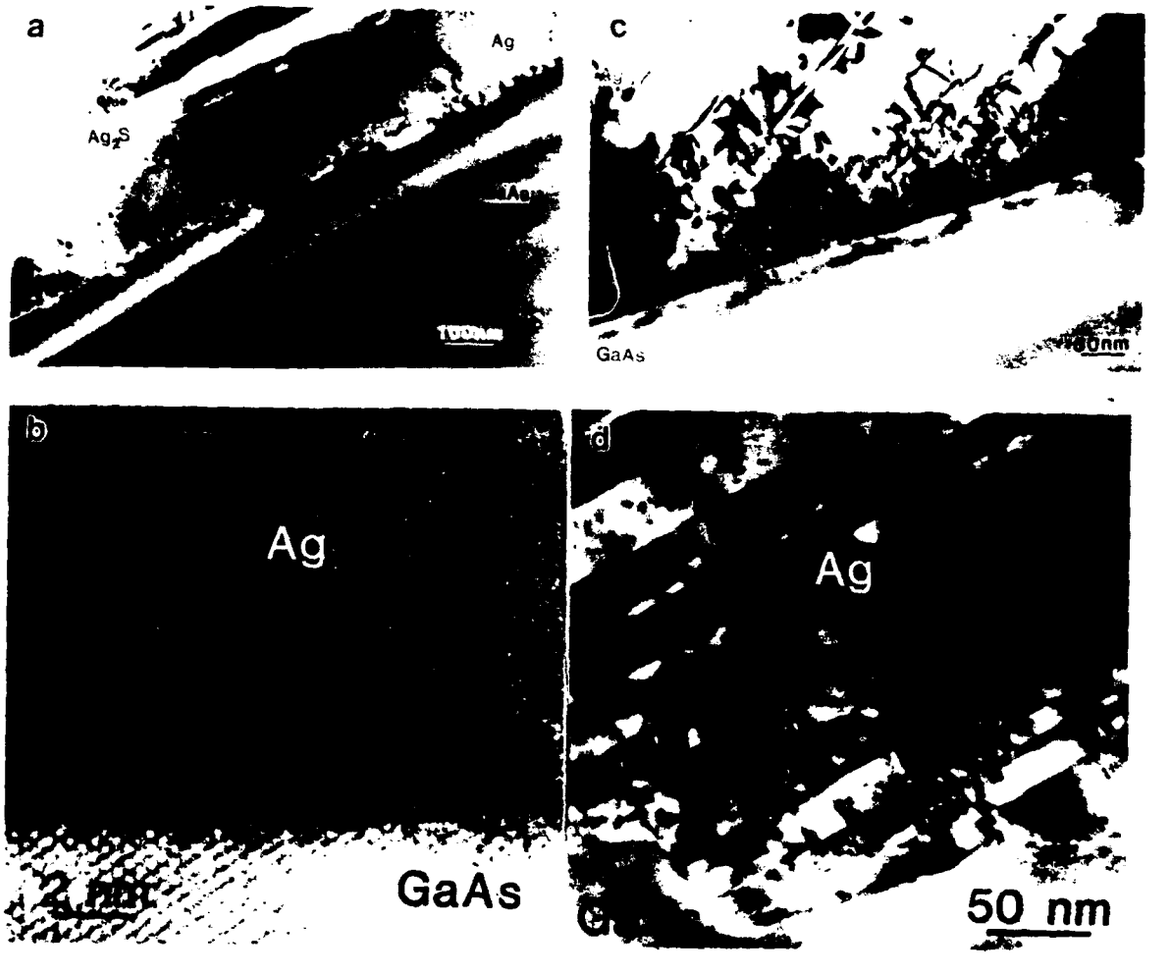


Fig. 4. Cross-section micrographs of Ag/GaAs interfaces. (a) Ag deposited in situ on UHV-cleaved (110) GaAs. Note the very large Ag grain size. (b) High-resolution image of sample prepared under the same conditions as (a) after annealing in N_2 at 405°C for 10 min. (c) Ag deposited on air-exposed cleaved (110) GaAs, showing a high density of twins and an oxide layer formed on the interface. (d) sample (c) annealed at 405°C in N_2. Note protrusion at the interface, and a twinning of the Ag layer.

After annealing, voids formed at the metal/GaAs interface in many areas, and a large portion of the Ag layer peeled off. These void formations were observed in as-deposited air-exposed samples, but adhesion decreased after annealing. Occasionally adhesion problems occurred in UHV-deposited samples as well, but the problems were not as drastic as in the air-exposed samples after annealing.

Electrical characterization of Ag contacts

The Schottky barrier height measured from I-V curves was 0.96 eV for as-deposited air-exposed samples, higher by 70 meV than that of UHV-cleaved diodes[3]. After annealing, a slight increase in barrier height 0.91 eV was observed for UHV-deposited samples, while a large decrease (0.79 eV) and leakage were observed for air-exposed samples (Fig. 5b). The large leakage current often reported in the literature[4-6] can be correlated with the adhesion problems in those samples.

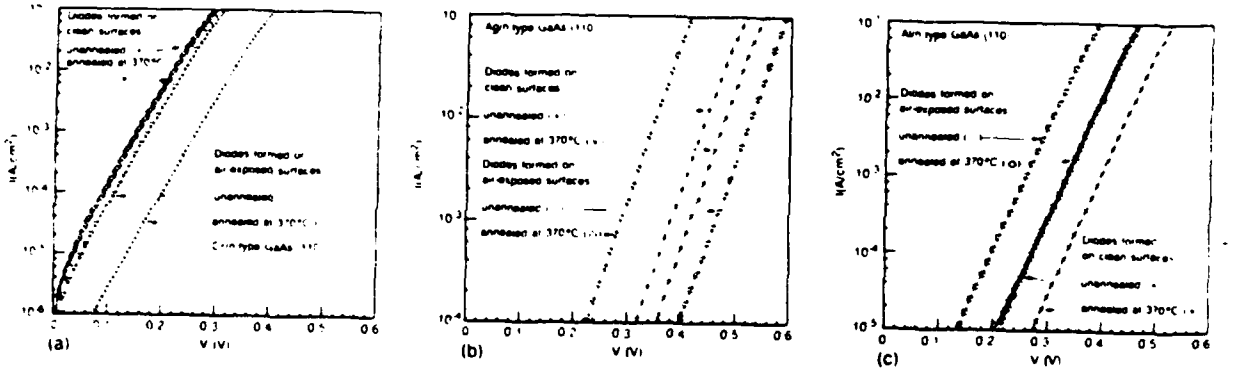


Fig. 5. Typical current-voltage (I-V) measurements for diodes a) Cr, b) Ag, c) Al formed on clean n-type GaAs (110) surfaces prepared by cleavage in UHV and on air-exposed surfaces prepared by cleavage and exposure to the atmosphere for ~1-2 hours.

Electrical aging was performed for as-deposited air-exposed and UHV-cleaved samples[1-3]. For UHV-cleaved Ag diodes, electrical aging was performed with current densities from 2×10^{-2} A/cm^2 (0.60 V) up to 1.4 A/cm^2 for reverse bias (-19 V). For the UHV-cleaved Ag diodes, no significant changes in barrier height or ideality factor were found after electrical aging under these conditions for more than 7 hours. By contrast, for air-exposed Ag/GaAs diodes, 50 min at 4.3×10^{-5} A/cm^2 (-14V) were sufficient to decrease the barrier height by 20 meV. More severe conditions of 2.3×10^{-3} A/cm^2 (-17V) for the same 50-minute period decreased the barrier height by 75 meV (Fig. 6).

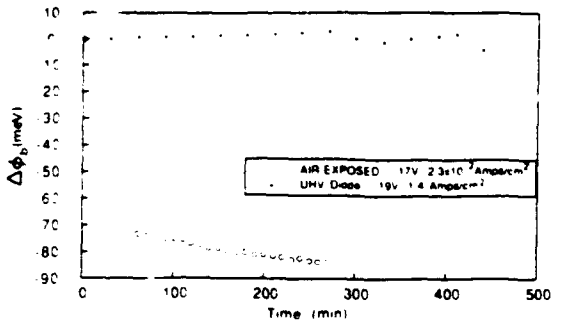


Fig. 6. Typical results of electrical aging for Ag/n-type GaAs (110) diodes formed on air-exposed and UHV-cleaved GaAs (110) surfaces. The change in barrier height is plotted as a function of the time the diodes were exposed to electrical aging.

Electrical aging reduced the barrier height difference between the two kinds of diodes without significantly changing the ideality factor of either kind of diode (n = 1.06-1.085). Thus electrical aging caused changes in barrier height but did not significantly deteriorate the near-ideal Schottky characteristics of the diodes. It was also observed that the changes in barrier height were not stable: the Schottky barrier height returned almost to its initial value (before current stressing) within about five days. Light or forward current accelerated this recovery effect.

Current stressing of UHV-cleaved diodes did not result in any structural changes, but the air-exposed contacts showed a significant change[2,3,7]. Current stressing caused a decrease in the size of the Ag grains, the formation of voids separating these grains, and poor adhesion of the metal overlayer. Local electromigration of Ag resulted in Ag accumulation in parts of the contact and thinning or void formation in other parts[7]. Electromigration of Ag in the air-exposed diodes may be the result of large local current densities due to an inhomogeneous interfacial oxide layer, which acts to block current flow over part of the area of the contact.

The observations of void formation, enhanced electromigration combined with the formation of new compounds, may explain why Ag Schottky contacts, which are known to be generally leaky, have not been applied successfully in GaAs device technology. However, this study has shown that very stable and reliable Ag contacts can be obtained if the Ag is deposited on atomically clean surfaces, such as the UHV-cleaved surfaces used for these observations.

Structure of Al contacts

For Al deposited on UHV-cleaved GaAs, a grain size of 100-300 nm was observed. The interface with GaAs remained flat and the Al (111) planes formed a small angle with the GaAs (111) planes (Fig. 7). This angle remained constant for grains with different orientations. Upon annealing at 375°C in N_2 for 10 min, the interface remained flat and the grain size did not

increase. In some areas a very thin layer (50-100 Å) of AlGaAs was formed. The formation of AlGaAs did not occur uniformly. There were large areas where this phase was not detected.[8,9]. Individual grains of Al above AlGaAs or in intimate contact with GaAs did not change the orientation relationship upon annealing. For the samples cleaved in air, the interface remained flat before and after annealing, but Al grain size decreased significantly. In some areas of the annealed air-exposed samples, a thin layer of AlGaAs was detected as well. For Al metallization, in contrast to the previously described metals (Au and Ag), no protrusions at the interface were observed for cleaved air-exposed samples after annealing. This may be due to formation of an AlGaAs phase in intimate contact with GaAs, with no As outdiffusion from the systems. In all observed cases, Al (or AlGaAs) was always found in intimate contact with the GaAs substrate. Void formation was not observed, either in as-deposited samples or in annealed ones. Aging of these contacts did not influence the interface structure.

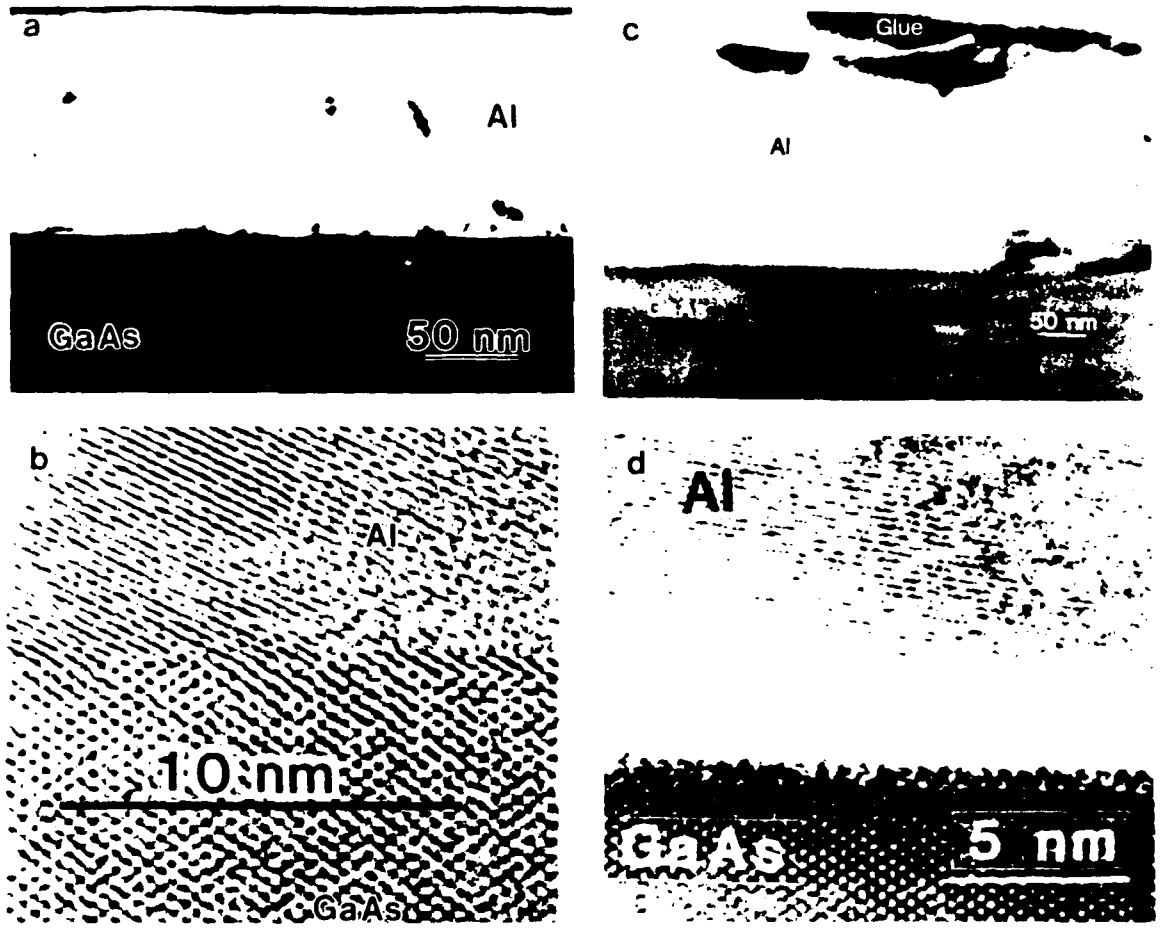


Fig. 7. TEM micrograph of cross sections of Al/GaAs interfaces (a) from the sample prepared on UHV-cleaved substrate; (b) high-resolution image of the same sample annealed at 405°C in N_2; (c) from the sample prepared on air-exposed GaAs; (d) high-resolution image of the same sample annealed under the same conditions. Note amorphous layer at the interface.

Electrical characterization of Al contacts

Al deposited in situ on UHV-cleaved GaAs formed Schottky contacts with a barrier height of 0.83 eV (Fig. 5c). After ex situ annealing for 10 min in N_2 atmosphere at 360°C or higher, the barrier height increased to 0.90 eV[3,10]. This is in contrast to the behavior of the Au diodes, where the barrier height decreased upon annealing. For as-deposited samples cleaved in air, the barrier height was lower (0.76 eV) than for UHV-cleaved samples, but a similar increase of 70 meV was observed after annealing[3,10]. The increase in barrier height for AlGaAs upon annealing has frequently been attributed to the formation of the interfacial AlGaAs with a larger bandgap[11,12]. However, recent studies showed that the barrier height of Al on n-GaAs (110) added up together with the barrier height of Al on p-GaAs to the GaAs bandgap[10]. The observed changes in barrier height are thus due to a downward shift of the Fermi level pinning position rather than the formation of AlGaAs. We have attributed this shift of the Fermi level pinning position to a change of stoichiometry due to the replacement of Ga by As[8,13].

Air-exposed Al/GaAs diodes were aged at -9.7 eV for more than 7 hours with a reverse current flow of 1.3 A/cm^2. There was a very small, almost insignificant increase of ~9 meV in the barrier height after electrical aging. No change in barrier height was noticed for UHV-deposited samples with the same aging parameters. This study shows that Al contacts are stable upon annealing. Strong adhesion between Al and the substrate exists for both UHV-deposited and air-exposed samples. No protrusions were found at the interfaces upon annealing.

Structure of Cr contacts

The TEM study of Cr layers deposited on clean UHV-cleaved GaAs surfaces consistently showed a columnar structure in the Cr layer. These columns were inclined 80°C to the interface, and this inclination was probably related to the deposition direction. The size of the columns was in the range of 4-12 nm. Voids up to 5 nm wide were formed between some of the columns. The void formation initiated in the Cr layer, about 10-15 nm from the interface with the GaAs (Fig. a).

High-resolution images of the interface taken in the ARM (1 MeV) in [100] and [110] projections show that the interface with GaAs was flat on an atomic scale [Fig. 8c]. The individual columns were misoriented with respect to each other by a few degrees.

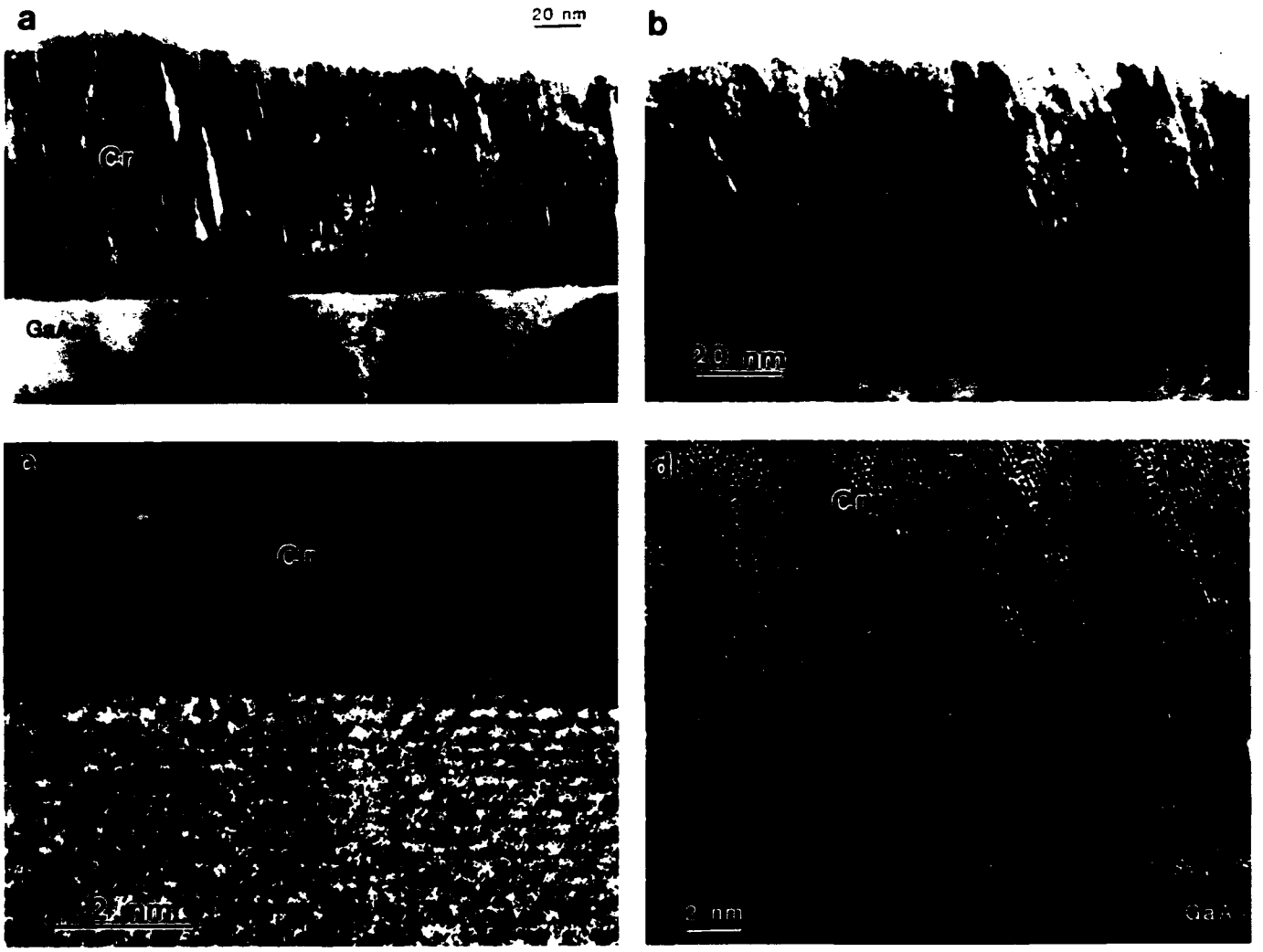


Fig. 8. TEM micrographs from Cr/GaAs interfaces: (a) low-magnification micrograph showing columnar structure of Cr with voids between columns for UHV as-deposited samples. Note that columns are almost parallel to each other and inclined ~80° toward the interface with GaAs; (b) low-magnification micrograph showing columnar structure of Cr with columns inclined in different directions to the substrate for air-exposed samples; (c) high-resolution micrograph of annealed samples deposited in UHV. (d) high-resolution image of annealed air-exposed samples. Note thick oxide layer at the interface and increased buckling of lattice planes toward the top of the layer.

For the samples with Cr deposited on the air-exposed GaAs surface, the interfaces were flat, similar to the UHV-deposited samples. A columnar structure was observed in the Cr overlayer as well, but the columns were almost randomly oriented, with a high void density between them (Fig. 8b). The columns in these samples were less than 2 nm. Extra spots of chromium oxide were detected in these samples. Annealing for 10 min in N_2 in atmospheric pressure at 370°C did not cause the formation of a new phase in either the UHV samples or the air-exposed samples. High-resolution images from annealed UHV samples show that the structure and interface abruptness remained stable after annealing. Individual columns remained slightly misoriented with respect to one another (Fig. 8c). A high-resolution image of the air-exposed samples showed an oxide layer about 1 nm thick at the interface (Fig. 8d). Voids between columns remained after annealing. The inclination directions of individual columns and lattice planes changed continuously with increasing layer thickness. The top of the layer consisted of small polycrystalline Cr grains.

Electrical characterization of Cr contacts

I-V and C-V measurements on both types of as-deposited diodes showed barrier heights of 0.66 eV for UHV-cleaved samples and 0.68 eV for air-exposed samples (Fig. 5a). This small difference was within measurement error. It shows that an oxide layer at the interface does not influence the barrier height for as-deposited samples. Similar values (0.69 eV) were reported for UHV-cleaved samples by McLean and Williams[14] , and slightly higher values (0.73 eV) were reported for Cr/GaAs (100) by Waldrop[15]. The barrier height (0.68 eV) and ideality factor (n=1.06) of the UHV-deposited contacts, as determined by I-V electrical measurements, did not change upon annealing at these temperatures (see Fig. 5a).

For air-exposed samples the barrier height increased (Fig. 5a) from 0.68 eV to 0.76 eV after annealing. The low barrier height of Cr (0.66 eV) for as-deposited samples (compared to other metals, e.g., 0.92 eV for Au) may be associated with the accumulation of As near the interface[13,16] .

Aging of Cr diodes at -19 V for more than 6 hours with a reverse current flow of 3 A/cm^2 did not change the barrier height by more than 6 meV (within experimental error) for either UHV-cleaved samples or air-exposed ones.

Pd/GaAs diodes

Studies of Pd deposited on (100) GaAs by Kuan[17], Sands[18], and Lin[19] showed that Pd disperses the oxide layer on the GaAs surface and a new "μ-phase" ($Pd_{0.56}Ga_{0.22}As_{0.22}$ according to Sands) is formed, even during room temperature deposition. These authors claimed that an oxide layer (2-3 nm) did not stop this reaction and that the oxide layer (Ga_2O_3) is not an effective diffusion barrier. Pd can penetrate it and react with GaAs. It was emphasized that GaAs need not be atomically clean before metallization with Pd. Our study of samples cleaved in UHV and cleaved in air showed that phase μ is indeed formed on air-exposed samples (Fig. 9a) but a completely new phase is formed when Pd is deposited on UHV-cleaved samples (Fig. 9b). This is an excellent demonstration that previous researchers were never dealing with truly clean samples, and certain sequences of phase formation reported in the literature are valid only for samples with impurities at the interface.

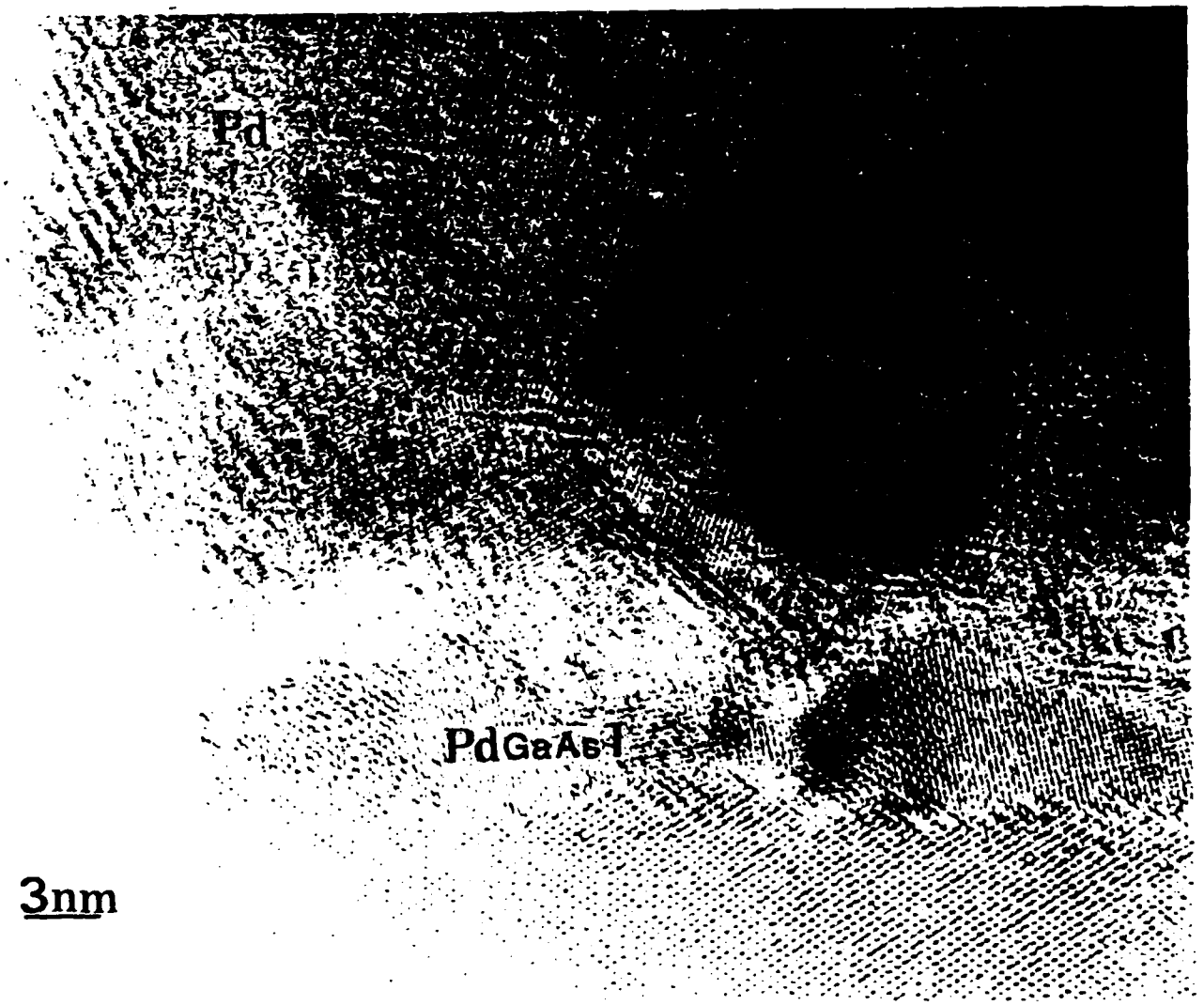


Fig. 9a: TEM micrograph of Pd sample deposited on air-exposed GaAs.

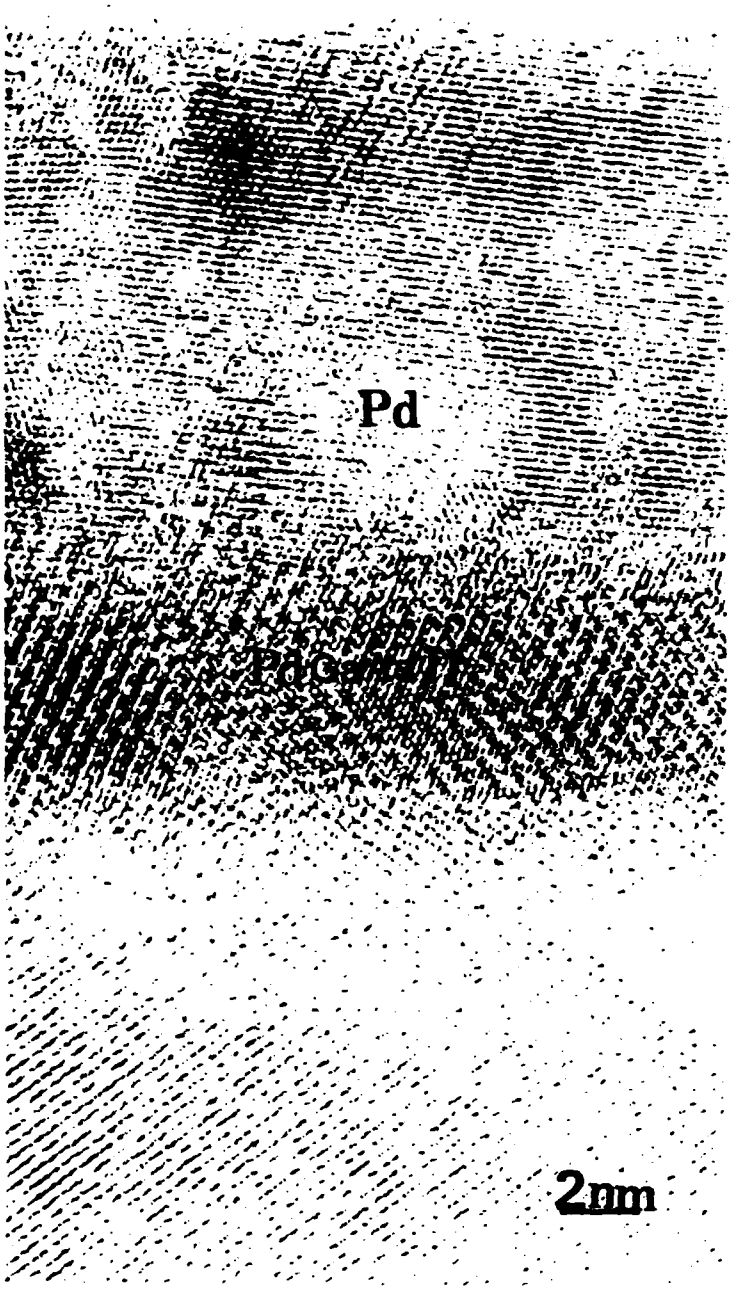


Fig. 9b. TEM micrograph of Pd deposited on UHV-cleaved GaAs.

The barrier height and ideality factor measured on UHV-deposited samples Φ_b = 0.85 eV, n = 1.05) (Fig. 10) and air-exposed samples (Φ_b = 0.84 eV, n=1.07) remained the same independent of surface preparation before annealing. The small differences in those measurements are in the experimental error range.

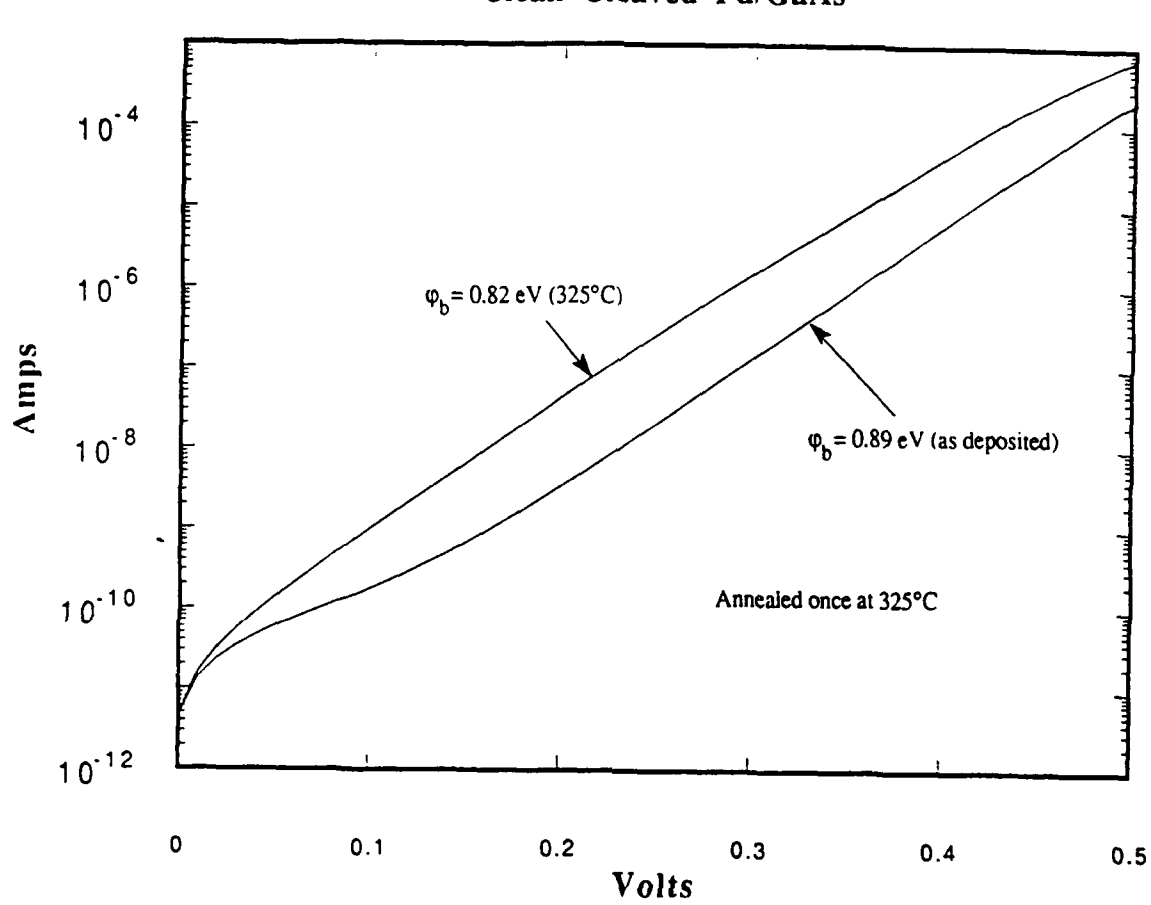


Fig. 10. I-V characteristic of Pd contacts deposited on UHV-cleaved GaAs before and after annealing.

Pd/InP diodes

Pd was deposited on n^+-InP (100) wafers doped with $5x10^{18}$ S/cm^3, which were chemically cleaned (H_2SO_4:H_20_2:H_20) for 2 min. The samples were isochronally annealed in Ar-5%H_2 ambient at temperatures from 175° to 650°C. TEM, x-ray diffraction and Auger electron spectroscopy were used to study the phase formation. The reaction began upon deposition. With subsequent annealing at 175°C, an amorphous ternary phase of approximate composition $Pd_{4.8}InP_{0.7}$ was formed. The same phase formed when deposition was performed on the substrate cleaved in UHV. No differences in the sequence of formation of new phases were found between air-exposed samples and those cleaved in UHV; therefore an extended study was carried out on (100) wafers chemically cleaned as available from industry.

For samples annealed at 215°C and 250°C, the tetragonal ternary phase Pd_5In_P was found with a=0.3928 nm and c=0.6917 nm. After annealing at 450°C, the cubic phase PdIn was observed with a=0.326 nm.

This study suggests two potentially important applications for Pd-based contacts to InP:
1) co-deposition of the PdIn phase will result in a thermally stable contact to InP
2) ternary intermediate Pd_XInP phases could be used to form laterally uniform tunneling ohmic contacts to n-InP by a two-stage reaction ($yM+Pd_XInP \rightarrow Pd_XM_y$ + InP:M where M=Si or Ge). This type of reaction has been reported for n-GaAs and may be expected for n-InP as well.

Ti/GaAs diodes

We began by studying Ti/GaAs (110) samples prepared by UHV deposition. As-deposited samples showed an atomically abrupt interface. The Ti film had a columnar structure, with an average column diameter of 6.3 nm. The electron diffraction pattern shows only the Ti ring pattern, indicating that the film is polycrystalline.

After annealing at 320°C in UHV, a layered structure was observed. The top layer was unreacted Ti of about 90 nm thickness. Between this top layer and the GaAs substrate there was an unreacted layer of about 25 nm thickness, having uniform interface morphology with the same substrate. The composition of this interfacial layer is not yet clear, but the electron diffraction pattern did identify the TiAs phase (Fig. 11). Additional phases which might be present in this layer are Ga_3Ti_2 or Ga_4Ti_5.

Fig. 11 TEM micrograph of cross-section sample of Ti deposited on UHV-cleaved GaAs after annealing at 320°C. Note formation of layers of TiAs, Ga_3Ti_2 and unreacted Ti.

Samples subjected to a series of UHV annealing up to a temperature of 450°C had a layered structure consisting of three metal layers. The top layer with a thickness near 40 nm was unreacted Ti. The second layer, of 20 nm thickness, consisted of a Ti-containing phase of as-yet undetermined composition. This intermediate layer showed uniform interface morphology with both the top Ti layer and the third layer adjacent to the substrate. This third layer is about 15 nm thick and forms a very rough interface with the substrate, i.e., protrusions are formed penetrating up to 21 nm into the substrate. Although the composition of the phases present in this third layer have not yet been definitely identified, Ga_3Ti_2 or Ga_4Ti_5 are possible candidates[20].

As for Cr/GaAs, the Schottky barrier height for as-deposited samples remain the same (Φ_b = 0.7 eV) for air-exposed and UHV-deposited samples. Further work on UHV-deposited and annealed Ti/GaAs (110) contacts and on air-exposed diodes is in progress.

Orientation Relationship in Metal/GaAs Interfaces

The orientation relationship between the metals investigated (Au, Ag, Al and Cr) for as-deposited samples was almost random for all samples. When the metals were deposited in situ on UHV-cleaved samples, the metal grains were always larger than those of the metals deposited on the air-exposed GaAs substrate. The difference in orientation relationship between differently prepared samples occurred after annealing. These differences are shown for Au in Table 1.

Table 1. Orientation relationship between Au and GaAs

Crystallographic axis	x	y	z
GaAs	011	100	$0\bar{1}1$
Type I	011	100	$0\bar{1}1$
Type IIa	411	122	$0\bar{1}1$
Type IIb	$\bar{4}11$	$0\bar{1}1$	$\bar{1}\bar{2}2$
Type III	$\bar{5}22$	455	$0\bar{1}1$

Type I orientation relationships were observed for all air-exposed samples (Au, Ag, Cr) except Al. This type of orientation relationship was explained for Au by Yoshiie and Bauer[21] as the epitaxial relationship to the newly formed Au-Ga phase, e.g., $(01\bar{1})_{GaAs} \parallel (1\bar{1}0)_{AuGa} \parallel (01\bar{1})_{Au}$ with $[01\bar{1}]_{GaAs} \parallel [001]_{AuGa} \parallel [0\bar{1}1]_{Au}$. However, formation of an Au-Ga phase is not necessary to fulfill the minimum mismatch on the interface. The mechanism is probably more general. Our data show that the Au orientation relationship for cleaved (110) GaAs surfaces depends on both the environment in which the GaAs surface was prepared before annealing and the annealing conditions, and not necessarily on the Au-Ga phases formed. The type I orientation relationship exists in annealed Au even when an Au-Ga phase is not formed, but it is characteristic of annealed Au deposited on air-exposed GaAs and exists for other metals like Ag, where this phase is not formed. A possible explanation for this behavior is that the γ-Ga_2O_3 grows epitaxially[22,23] in a type I orientation: $(011)_{Ga_2O_3} \parallel (011)_{GaAs}$ with $[100]_{Ga_2O_3} \parallel [100]_{GaAs}$. This oxide provides an excellent lattice match to Au: $d_{400}(Ga_2O_3) = 0.205$ nm, as compared with d_{200} (Au) = 0.203 nm (with similar d values for Ag and Cr) and d_{044} (Ga_2O_3) = 0.145 nm, with d_{022} (Au) = 0.149 nm. This observation would suggest that as soon as GaAs is exposed to air, epitaxial γ-Ga_2O_3 is formed, and the deposited metal epitaxially relates to the oxide already existing at the interface.

The oxide on GaAs is not a continuous layer. In the areas where the oxide is not present, twinning takes place, giving a better match at the interface, leading to a type IIa orientation relationship. A type IIb orientation was observed in most cases for Au deposited on UHV-cleaved GaAs in situ post-annealing.

The orientation relationship in UHV-deposited Au samples annealed ex situ in N_2 (405°C, 10 min, as done for air-exposed samples) was completely different and was described as type III. This type of orientation relationship was observed not only in Au/GaAs samples but also in Al/GaAs and Ag/GaAs samples. A small rotation angle (~10°) between $(111)_{Au,Ag,Al}$ planes and $(111)_{GaAs}$ planes was characteristic for all three metals (they have similar lattice parameters) deposited in situ on UHV-cleaved GaAs and annealed in N_2. This behavior was explained by As accumulation at the interface[8,13]. The metal probably tries to accommodate to the accumulated As or to the As plane in the GaAs substrate. This discussion shows that the macroscopic orientation relationship of metal grains on GaAs is very sensitive to interfacial

contamination. Comparison of the crystallographic orientation relationships of metal grains on GaAs (110) revealed distinct differences between UHV-deposited and air-exposed samples. In fact, the observation of the orientation relationship after annealing for metals with similar lattice parameters can be used as an additional tool in recognizing how clean the GaAs surface was before metal deposition. All metals deposited on air-exposed substrates follow the orientation relationship of the oxide present on the semiconductor surface.

We have used this knowledge to improve contact performance using conventional integrated circuit processing methods for several systems. For example, we have used refractory metal nitrides to minimize interfacial reactions and produce stable contacts at temperatures up to 800°C or more. .

Structure of TiN contacts

TiN thin films (~40 nm) were formed on Si-doped (100) GaAs substrates (N_D = 1.5x10^{17} cm^{-3}) by reactive sputtering deposition in a rf sputtering system. Samples capped with sputtered SiN_x on both sides were annealed at 500, 700 and 850°C in a flowing Ar ambient by using a halogen lamp rapid thermal annealing (RTA) system for 10s. Cross-sectional TEM shows columnar structure of TiN (Fig. 12).

Fig. 12. Transmission electron microscopy images of cross-sectional TiN/GaAs (a) as-deposited samples, and (b) the sample after annealing at 850°C.

The columnar grains were divided into smaller subgrains separated by small-angle grain boundaries. Optical diffraction patterns taken from such columns show a preferred orientation relationship between the TiN within one column and the GaAs substrate. The width of TiN columnar grains was 12 nm on average. Fig. 12a shows an abrupt interface with an intervening amorphous layer, probably oxide (~1.5 nm) between the as-deposited TiN film and the substrate. Electron diffraction analysis revealed that the TiN had a NaCl structure with a lattice parameter a_0 =0.424 nm. After annealing at 500°C for 10s by RTA, the uniform interface morphology deterioriated and many pocket-like protrusions have formed beneath the interface. The size of pockets increased with increasing annealing temperature. Figure 12b shows the pockets formed at TiN/GaAs interface after annealing at 850°C.

For annealing at 500°C, the average depth of penetration of these pockets was about 4 nm with a maximum of 6 nm. The average edge-to-edge spacing between pockets was about 24 nm, giving a linear density of 40 per μm. Annealing at 700°C increased the average pocket penetration depth to 5.3 nm, and decreased the average spacing between pockets to 23 nm. The sample annealed at 850°C shows that the dimension of the pockets had increased to an average depth of 6 nm; 27% of the pockets penetrated deeper than 7 nm. The maximum depth of the pockets was 10 nm as shown in Fig. 13 on the left. The average spacing between neighboring pockets for the sample annealed at 850°C decreased to 20 nm. For this annealing, more pockets were formed, and they penetrated more deeply than for the 500°C anneal.

Fig. 13
High-resolution cross-section TEM images of the TiN/GaAs sample annealed at 850°C.

The mechanism of the pocket formation is not clear. It is believed that no chemical reaction should occur at the TiN/GaAs interface even for the sample annealed at 850°C since TiN has a high thermodynamic stability and low diffusivity. It can be expected that even though TiN thin films have been used widely as diffusion barriers in Si technology[24], volatile arsenic atoms from

the GaAs substrate may be able to escape through weak points and pinholes in the thin intervening layer at the interface, and diffuse out through the columnar boundary structure of the thin film and the TiN grain boundaries during annealing at high temperatures. This extensive outdiffusion of arsenic atoms would leave excess gallium atoms at the interface near these weak points, which might form GaN within the pocket. However, this phase was not detected in our study.

Electrical characterization of TiN contacts

The current-voltage (I-V) and capacitance-voltage (C-V) characteristics of the diodes were measured on the as-deposited samples and the samples annealed at 500, 700 and 850°C. The same samples were used for the structural studies described above. Enhancement of the thermionic emission barrier height, determined from I-V characteristics[25], was observed in the samples after annealing at 500 to 850°C (Fig. 14). Concomitantly, the diode capacitance decreased with increased annealing temperature. To correlate a model consistent with the electrical properties and interface structure, the formation of these pockets was taken into account.

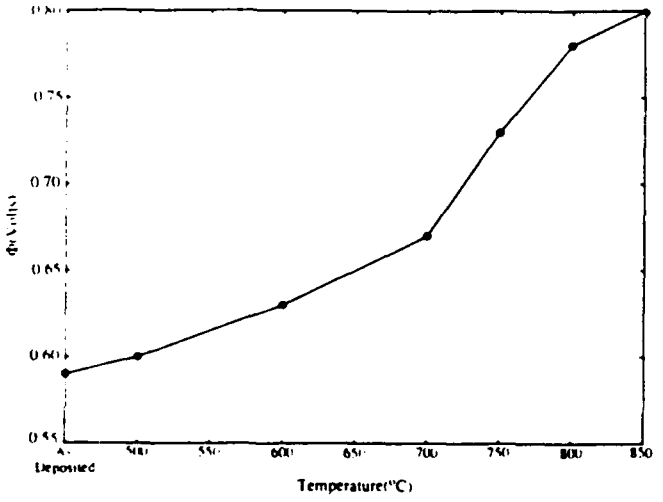


Fig. 14.
Measured barrier height Φ for TiN/GaAs contacts annealed at different temperatures.

TEM showed that the fraction of surface area occupied by the pockets increased with increasing annealing temperature. In order to explain the change in barrier height, it is necessary to assume a loss of As. This loss during annealing was confirmed by analytical TEM. The loss of only one As atom per pocket would lead to p+ doping concentration on the order of 18 cm^{-3}. The loss of As upon annealing and pocket formation near the interface might be the cause of the observed changes in electrical characteristics.

Structure of ZrN contacts

The interface structure of these contacts appears very similar to the TiN contacts described above. Fig. 15 shows a series of high-resolution TEM micrographs taken from as-deposited 850°C- and 900°C-annealed samples. The formation of protrusions under the interface can be seen. The protrusions grow larger and deeper into the substrate as the annealing temperature increases. At 900°C, the largest protrusion is about 50 Å deep into GaAs. Optical diffraction patterns from the high-resolution micrographs did not reveal any evidence for new phases in the protrusions.

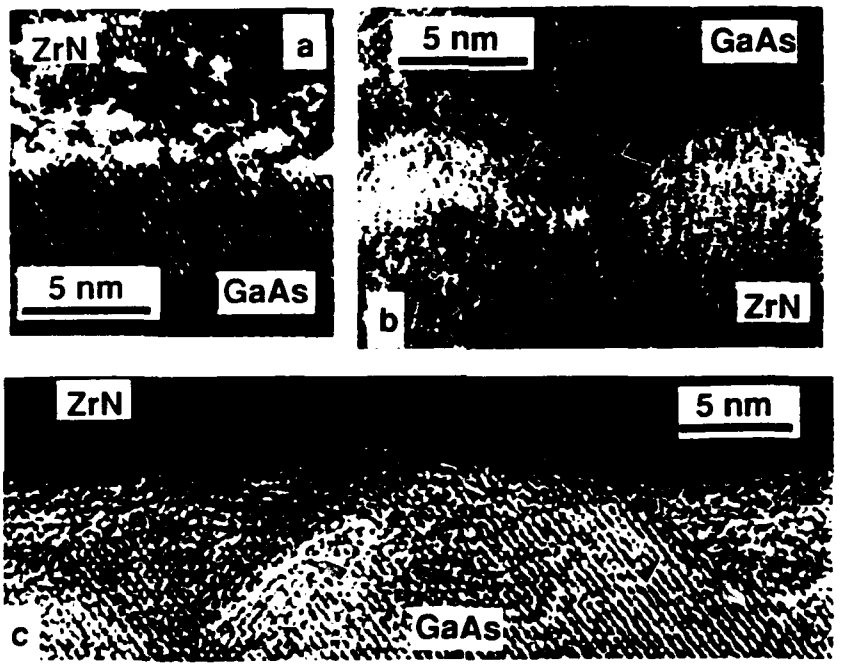


Fig. 15. Microstructure of ZrN/GaAs interface as a function of temperature, a) as deposited, b) 850°C anneal and c) 900°C anneal. Note the protrusions under the interface in b and c as marked by arrows. No sputter cleaning was performed on these samples.

Electron diffraction studies revealed ZrO_2 in the interfacial area. Therefore, an in situ cleaning of the chamber and substrate was deemed necessary for making better diodes. After reviewing the literature and the limitations of the equipment, a variation of the sputter etching method was tried. Fig. 16 shows a series of micrographs similar to those in Fig. 15 after sputter cleaning. The protrusions are noticeably smaller in the 900°C-annealed sample. After 850°C annealing protrusions are not seen.

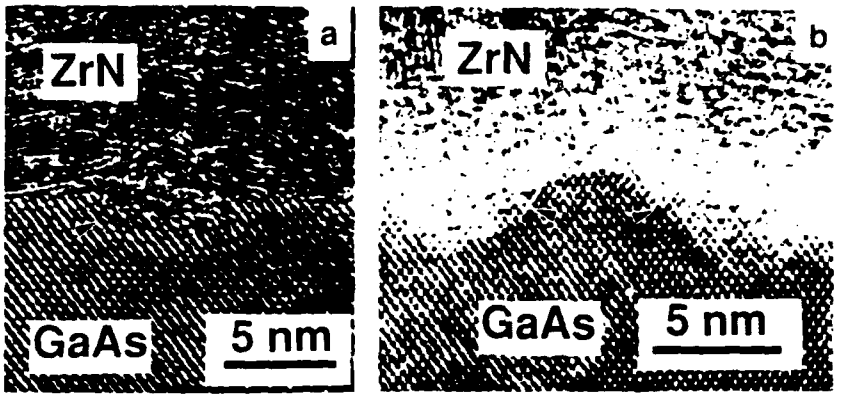


Fig. 16. Microstructure of ZrN/GaAs interface as a function of temperature, a) 850°C anneal and b) 900°C anneal. Note the reduction in size of protrusions after 900°C anneal as compared to Fig. 15. No protrusions are seen in the 850°C- annealed sample.

Electrical characterization of ZrN contacts

Fig. 17 shows the variation in the barrier height and n as a function of annealing temperature. It can be seen that the barrier height of the diodes increases with increasing annealing temperature. However, the value of n also increases and reaches 1.5 after a 900°C anneal.

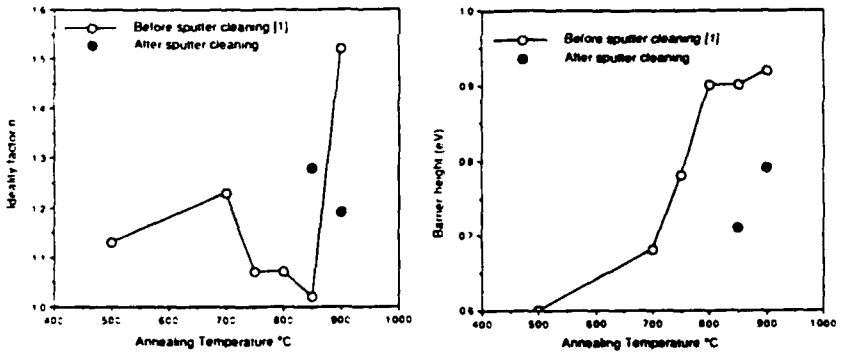


Fig. 17. Ideality factor and barrier height of ZrN/GaAs Schottky contacts vs. RTA temperature (10 s each). Contacts were prepared by sputter deposition as described in ref. [26] and after an additional sputter cleaning step.

The effect of microstructural changes after sputter cleaning are reflected in the ideality factors of these diodes. Significant improvement in the ideality factors of 900°C-annealed samples (from 1.5 to 1.19) is seen after sputter cleaning. The values of the barrier height and ideality factor are also plotted in Fig. 17 for comparison.

The observed increase in barrier height after annealing at the same temperature, for instance, 900°C, is different for sputter-cleaned and non-sputter-cleaned samples. For the sputter-cleaned samples, the increase in the barrier height is smaller. Micrographs in Fig. 16 show that the protrusions in the sputter-cleaned samples are also smaller.

There are two possible explanations for these results. The first is related to the formation of a p+ region near the interface, such as pockets (as proposed in the case of TiN contacts). If such a region is reduced, the enhancement of barrier height would be smaller, as observed in sputter-cleaned samples. On the other hand, if As is lost during annealing, there would be Ga-rich regions near the interface, e.g., in the form of protrusions. According to the Advanced Defect Model (ADM), the barrier height would increase. If smaller protrusions correspond to a smaller loss of As, then the enhancement of barrier height would be smaller. Thus, both models describe the observations well.

Stoichiometry of the semiconductor near the metal interface

Near-ideal electrical characteristics of metal/n-GaAs Schottky barriers were found for UHV-prepared samples. The lowest barrier height was for Cr (Φ_B = 0.67 eV) with the highest for Au (Φ_B = 0.92 eV)[3]. Our analytical TEM EDX results for these contacts, obtained from cross-section samples, consistently show a deviation in stoichiometry for the region within ~10 nm of the GaAs beneath the metal contact. The deviation is always in the As-rich direction compared to bulk GaAs. A stronger As-K_α peak relative to the Ga-K_α peak can be observed only for a certain time (usually less than a minute) at a given location of the electron beam near the interface, so that statistically reliable results can be obtained only by adding data from several equivalent positions of the beam along the interface.

The amount of additional As found in this near-interfacial region depends on the metal used and the thermal history of the sample. For as-deposited metals, the largest deviation from stoichiometry was found for Cr, and the smallest was found for Au. After annealing above 360°C, the Au barrier height decreased to 0.8 eV (for both UHV-deposited and air-exposed samples), while the Cr barrier height was stable for UHV-deposited samples but increased by 80 meV to 0.76 eV for air-exposed samples. Air-exposed annealed Cr/GaAs samples showed less excess As than the as-deposited structures; they were quite comparable to Au/GaAs in off-stoichiometry. Indeed, the barrier height of annealed Au/GaAs samples (0.80 eV) is also comparable to annealed air-exposed Cr/GaAs samples (0.78 eV).

The observation of excess As near the metal/GaAs interface thus correlates consistently with the observed Schottky barrier heights: the lower barrier heights correspond to more pronounced As accumulation near the metal/GaAs interface, and higher barrier heights correspond to less As accumulation[13].

In addition to the change of stoichiometry the interface structure of such metals as Au and Cr shows evidence of defects (or spacial reconstruction). High-resolution electron microscopy shows that even the most ideal Au/GaAs (110) and Ag/GaAs (110) interfaces formed in UHV conditions, which remain flat and abrupt after annealing, reveal a ~0.5-1 nm thick distorted interfacial layer, where some atom rearrangement is evident (Fig. 18). The atomic arrangement near the interface can be clearly distinguished from the bulk semiconductor, and the presence of point defects and even the possibility of dislocation formation has to be considered. This interfacial reconstruction was especially pronounced in UHV-deposited Au/GaAs samples after annealing at 405°C in N_2 for 10 min, where a clear deviation from stoichiometry in the As-rich direction was observed (Fig. 19).

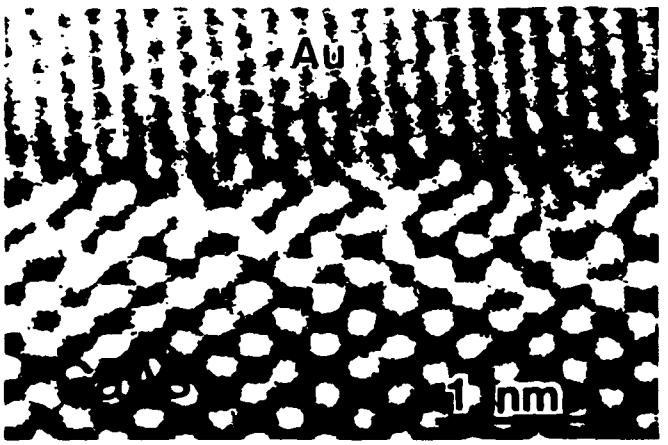
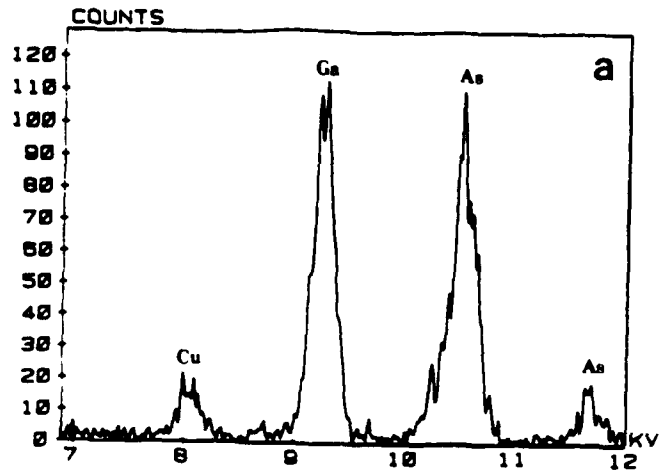


Fig. 18. High-resolution micrograph of the Au/GaAs (011) interface annealed at 405°C for 10 min in N_2 atmosphere. Note the lattice distortion in the interfacial area and the twisting of all Au planes toward the GaAs planes. A 10° angle was measured between the $(111)_{Au}$ and $(111)_{GaAs}$ planes.

In Cr/GaAs contacts, high-resolution images from annealed UHV samples show that the structure and interface abruptness remained stable after annealing. Periodic arrangements of white dots were observed at the interface in both the [001] and [1$\bar{1}$0] projections. To interpret the formation of this interfacial contrast, multi-slice image simulations were employed. These calculations showed that an ideal, unreconstructed interface structure could not explain the observations, even allowing for a wide range of sample thickness and defocus values.[27]



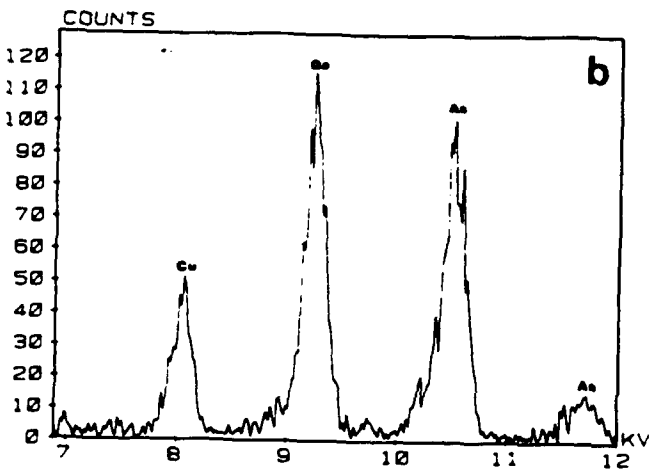


Fig. 19. EDX spectra taken (a) close to the interface with Au and (b) in the substrate far from the interface. Note higher As-K_α intensity closer to the interface.

Analytical investigation by energy-dispersive x-ray spectroscopy consistently showed the stoichiometry of the GaAs beneath the Cr to be As-rich. Therefore, to determine the defects responsible for this contrast, simplified models containing substitutional point defects that lead to an As-rich interface were considered for the image simulations. Preliminary results suggest that a periodic arrangement of Ga vacancies may be a cause of the experimentally observed contrast at the interface. However, more extensive calculations, which allow for interstitial defects and the effects of misfit stress, are necessary to determine the cause of the observed contrast.

Our study showed for the first time that the changes of stoichiometry and near-interfacial reconstruction typical of atom-by-atom deposition methods, which result in disruption of the semiconductor surface, can be avoided by forming metal-semiconductor interfaces in a novel way. In particular, a technique has been developed that makes it possible to bring preformed metal clusters into contact with clean semiconductor surfaces. The energetics of such a deposition are dramatically different from those in atom-by-atom deposition, making it possible to minimize surface disruption.

Protective ~3-nm layers of Xe were first condensed on GaAs (110) cleaved in UHV at 60K[28,29]. A metal was then deposited by evaporation onto the solid xenon layer. As a result of this deposition, metal clusters formed in and on the xenon layer, buffered from the semiconductor surface. The Xe buffer layers were sublimed upon warming to 300K so that the metal clusters were brought into contact with the undisrupted GaAs surface. In this way, atom deposition, cluster nucleation and growth occurred in the overlayer before any direct substrate contact, eliminating complications from the release of energy by metal solidification (Fig. 20a,b).

Detailed analytical and high-resolution TEM studies were performed with plan-view and cross-section samples. Analytical study did not show any evidence for excess As in the interfacial area (Fig. 21). High-resolution micrographs prepared from cross-sectioned samples showed that the interface between the clusters and the substrate is abrupt, and no reconstruction in the GaAs beneath the clusters was found (Fig. 20b).

For all these samples, the Fermi level pinning positions were determined in situ by photoemission spectroscopy. As reported earlier[28], cluster deposition in n-GaAs (110) results in Fermi level pinning positions near E_C - 0.3eV. This position is distinctly different from the pinning positions near midgap determined for the same metals when deposited atom by atom by evaporation.

The present microscopy study of cluster-deposited metals shows no evidence for semiconductor interface reconstruction or stoichiometry changes in the semiconductor which are typical of atom-by-atom deposited structure. This shows for the first time that metal/semiconductor interfaces can be formed free of bulk defects. This conclusion is based on both high-resolution and analytical electron microscopy. It is important to note that such near-ideal metal/n-GaAs interfaces do not have the Fermi level pinning positions predicted by the MIGS models[30,31] but rather have new, unusual pinning positions in the upper half of the band gap, which may be the ones typical for nearly ideal interfaces which are not influenced by defects in the near-surface semiconductor layer.

These results strongly support the idea that the usually observed Fermi level pinning positions are typical for interfaces with defects present in the semiconductor beneath the metal, formed by the release of energy upon metal sublimation on the semiconductor surface. This conclusions, together with earlier observations[8,13,32,33] of anion-rich GaAs near the metal/semiconductor interface of Schottky contacts prepared by the conventional atom-by-atom deposition methods, points toward either anion clusters[34] or anion antisite defects[35] as the dominant Fermi level pinning mechanism. Our study is unable to distinguish between these two models.

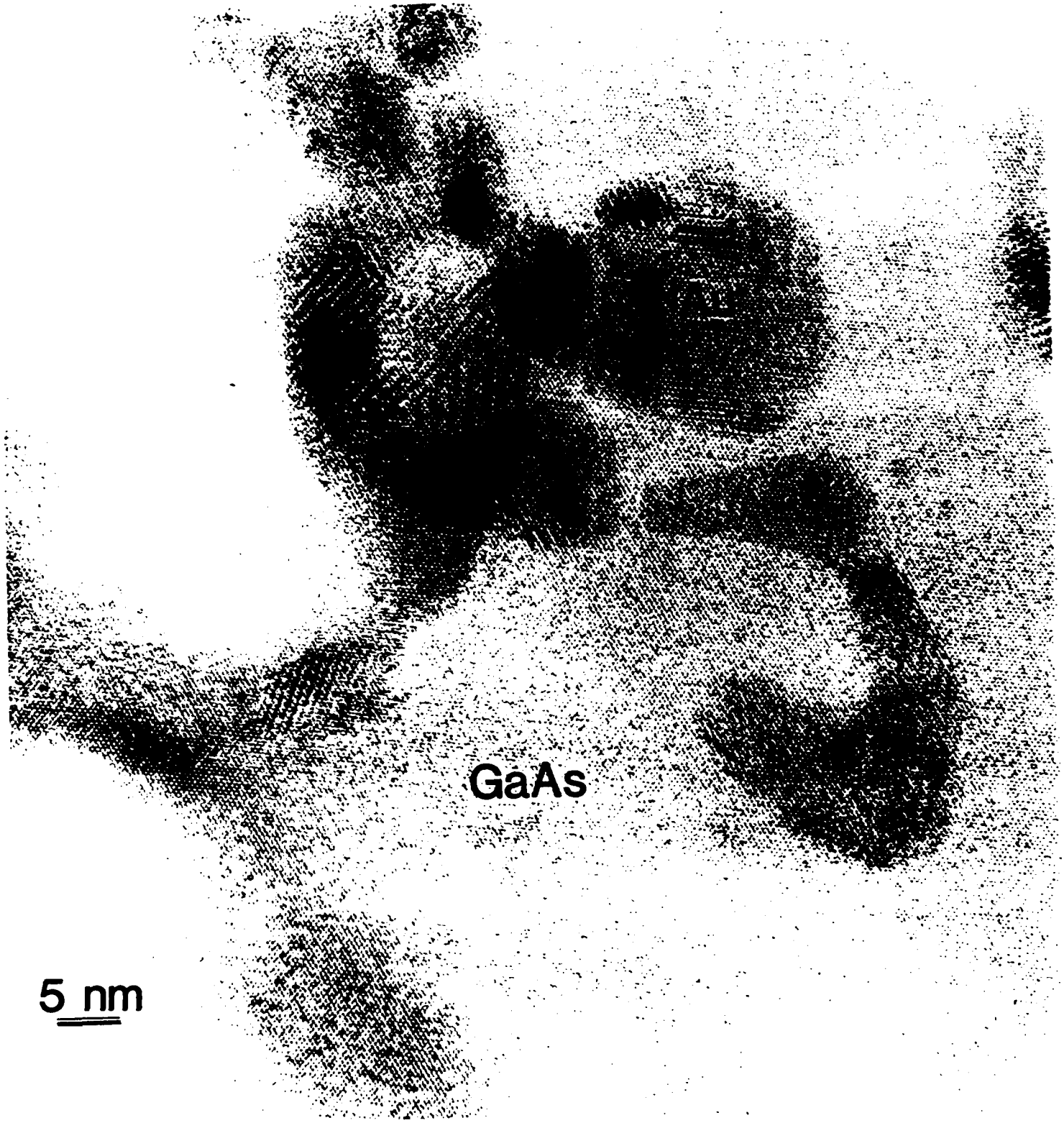


Fig. 20a. Plan-view micrograph of Au clusters deposited on the GaAs surface

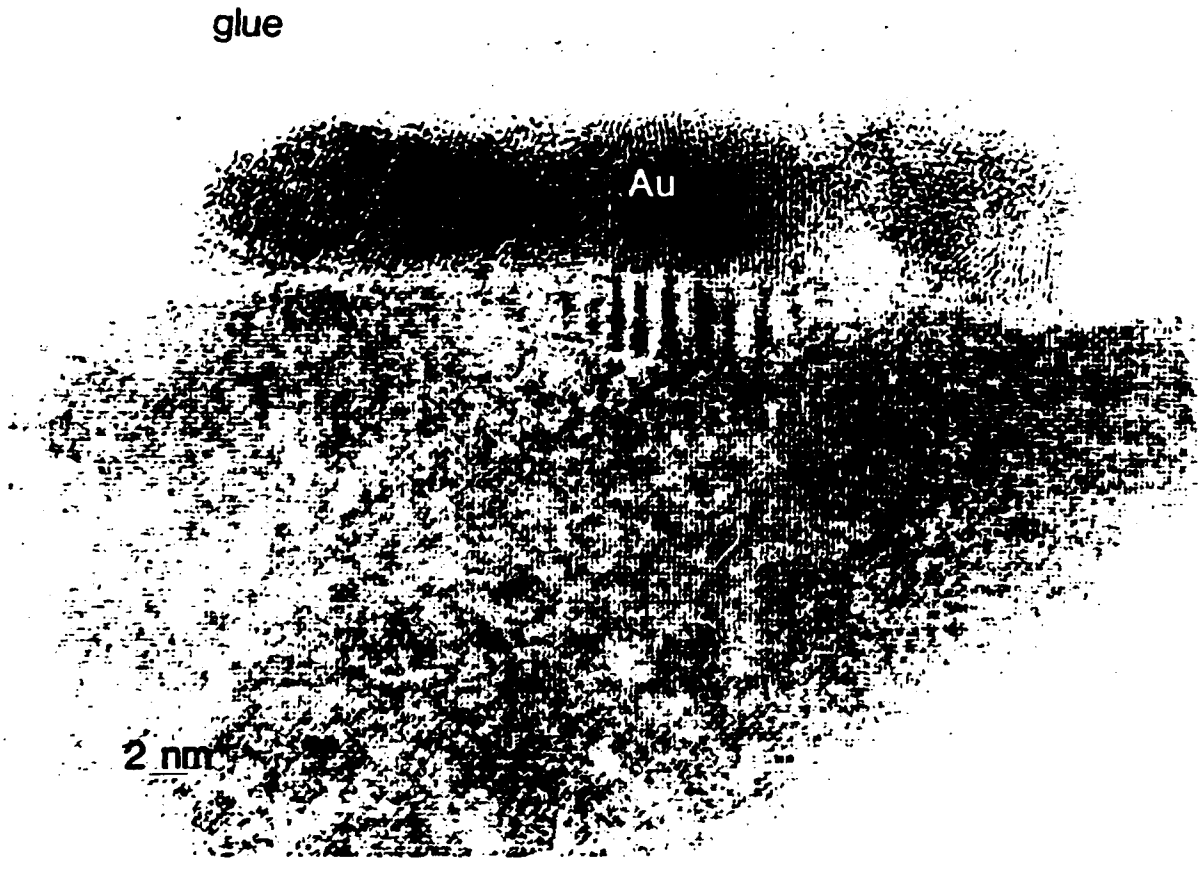


Fig. 20b. cross-section of the interface between Au clusters and the GaAs substrate.

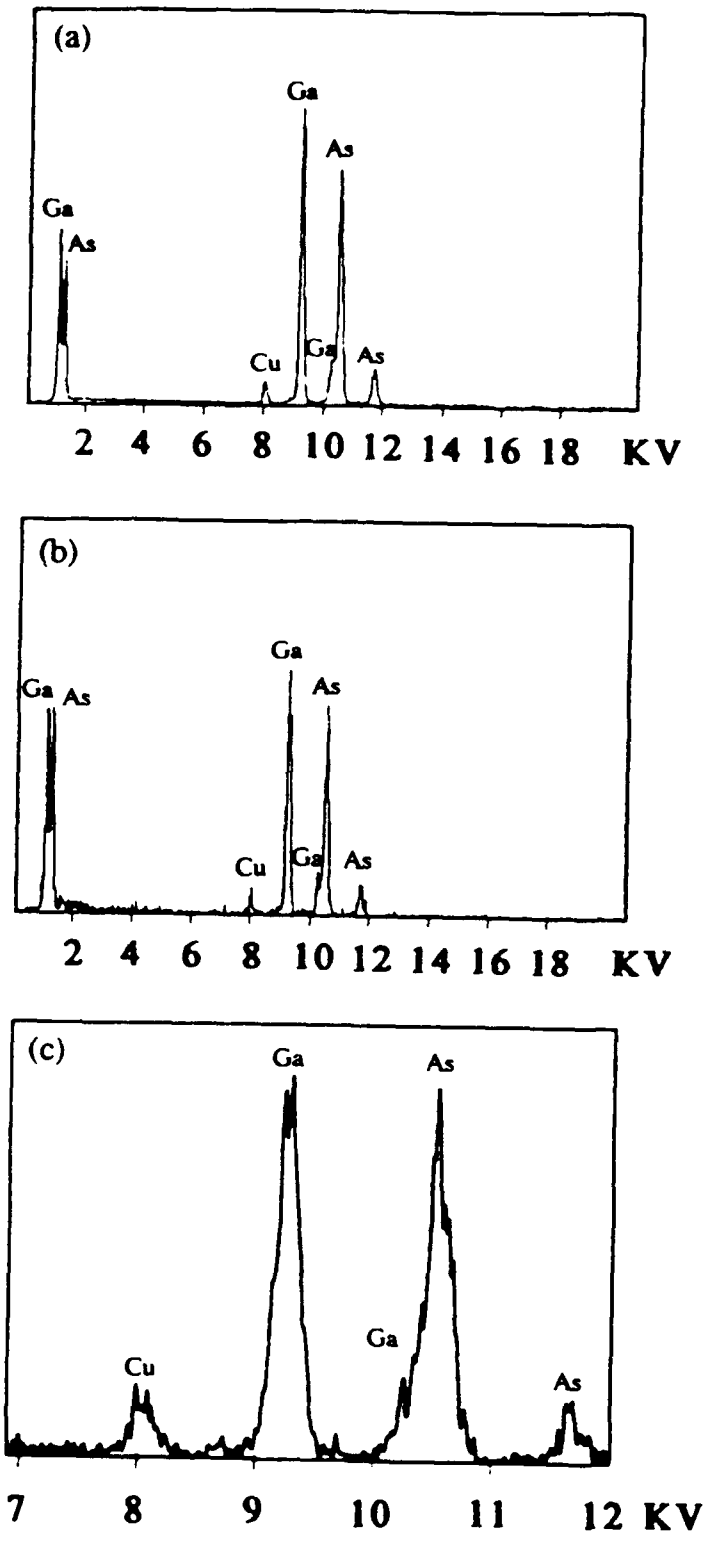


Fig. 21 EDX spectra taken in the GaAs substrate: (a) below the metal Au cluster, (b) below the Ag cluster covered by Au layer, (c) below the Au layer deposited atom by atom. The As/Ga ratio in (a) and (b) is typical for bulk GaAs; (c) shows As-rich GaAs typical for atom-by-atom-deposited Schottky contacts on GaAs.

This work led us to develop a microscopic model of metal/III-V Schottky barrier pinning, the Antisite Defect Model, with Prof. W. E. Spicer of Stanford University[36]. We hypothesize that stoichiometry-related deep level defects such as As_{Ga} antisite defects are instrumental in determining the Fermi level pinning position in traditionally prepared contacts. In contrast, cluster deposition of non-reactive metals such as Au was shown to suppress this change of stoichiometry and to result in unusual Fermi level pinning positions outside the "canonical range" of pinning energies between about midgap and 0.5 eV above the valence band maximum. This result indicates that in special cases (e.g., cluster deposition and possibly epitaxial growth of the metal overlayer) it may be possible to avoid formation of defects near the interface and thus obtain Fermi level pinning at a position different than that typical of conventionally prepared contacts.

SUMMARY

These results make it clear that any change in near-interfacial stoichiometry, e.g., by reaction of the metal overlayer with the substrate, will result in a change in barrier height and thus a change in the electrical performance of the device.

Using electrical and microstructural characterization, we have investigated a wide range of metal/GaAs systems including the metals Ti, Al, Cr, Pd and Au. The Fermi level pinning position is found to relate directly to the amount of excess As near the interface: very As-rich GaAs results in pinning near midgap and thus a low barrier height for n-GaAs; less As-rich conditions result in pinning closer to the valence band and thus a high barrier height for n-GaAs. The observation was made by comparing near-interfacial stoichiometry of different metals with low and high barrier height, and by studying the change in near-interfacial stoichiometry upon annealing.

The first evidence of the existence of As-rich layers just under the metallization was obtained by analytical TEM of cross-sectional structures. The validity of these measurements was later confirmed by the use of the same TEM technique on low-temperature MBE-grown GaAs layers. These novel epitaxial layers exhibited a stoichiometry similar to that of the near-interfacial region of metal/GaAs contacts. In this case, however, the As-rich stoichiometry extended through the entire layer and could be independently confirmed by conventional x-ray and Auger analysis.

The barrier heights (on n-GaAs) of metals which react preferentially with As (e.g., Ti and Al) increase upon thermal annealing, while the barrier heights of metals which react preferentially with Ga (e.g., Au) decrease. Interfacial contamination layers also influence the type and extent of chemical reactions at the interface, with the same correlation between near-interfacial stoichiometry and the Fermi-level pinning position.

This important result found direct application in our study of the most stable rectifying contacts on GaAs formed by refractory metals and refractory metal nitrides. It was found that the stability of such Schottky contacts is limited due to their reactivity with Ga and As, which changes the near-interfacial stoichiometry and thus the barrier height. However, a thin diffusion barrier of refractory metal nitrides effectively suppresses interfacial reactions up to 800°C or more. A more detailed study of the final failure mechanism of ZrN/GaAs Schottky contacts, which are among the most promising high-temperature stable contacts, revealed that residual oxide is involved in the failure of even these structures above 800°C. Improvements in thermally stable Schottky contacts using conventional integrated circuit processing technology were found by using special substrate surface cleaning methods. In conventionally prepared ZrN Schottky contacts, an increase in the barrier height, a decrease in the ideality factor and a decrease in the reverse breakdown voltage occurs upon rapid thermal annealing at elevated temperatures (~850-900°C). Annealing at 850°C resulted in substantial change in interfacial morphology, including the formation of protrusions related to residual inhomogeneous contamination present at the interface before metallization. The change in morphology was directly correlated with a large increase in the leakage currents in the Schottky contacts. ZrN/n-GaAs Schottky contacts which were specially processed with an extra sputter cleaning procedure resulted in contacts with more thermally stable electrical and morphological properties than those of contacts fabricated with conventional cleaning methods.

The results of this project, summarized above, allow us to predict directly the most promising strategies for the development of high-temperature stable and reliable contacts on compound semiconductors. First, utmost care must be taken with substrate cleaning to avoid residual contamination layers such as oxides. Contacts prepared by in situ UHV deposition onto freshly cleaved surfaces can serve as benchmarks of the stability achievable with a specific metallization. Second, after eliminating the influence of contamination, the contact stability is limited by interfacial processes that change the stoichiometry of the semiconductor near the interface. These processes can be chemical reactions or preferred diffusion of one of the components of the compound semiconductor into and through the metal overlayer. Contacts of refractory metals with nitride layers as diffusion barriers were shown to fulfill these requirements very well.

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Graduate Students and Postdoctorals Supported Under the Contract

Graduate Students: R. Caron-Popowich, J. Ding, P. Phatak

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Theses Resulting:

R. Caron-Popowich: "Pd and Ni Thin-Film Reactions with InP Possibilities for Metal Contacts" (PhD thesis, May 1989, University of California, Berkeley)

J. Ding: "Thermally Stable Metal/GaAs" (PhD thesis, Dec. 1989, University of California, Berkeley)

J. Ding: "Cation Exchange at the In/GaAs Interface: Structure and Morphology of the Graded InxGaxAs Layer" (MS thesis, May 1986, University of California, Berkeley)