AD-A259 441

(2)

PROCESSING, FABRICATION, AND DEMONSTRATION OF HTS INTEGRATED MICROWAVE CIRCUITS

Navy Contract No. N00014-91-C-0112

R&D Status Reports – Data Item A001
Report No. 5

Reporting Period: July 27, 1992 through October 25, 1992

Submitted by:

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R&D STATUS REPORT

ARPA Order No.: 7932

Program Code No.: htsc 051-101

Contractor: Westinghouse Electric Corp. (STC)

Contract No.: N00014-91-C-0112

Contract Amount: $5,369,203

Effective Date of Contract: 7/24/91

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Principal Investigator: G. R. Wagner

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Short Title of Work: Processing, Fabrication, and Demonstration of HTS Integrated Microwave Circuits

Reporting Period: 7/27/92 to 10/25/92

DESCRIPTION OF PROGRESS

TASKS 1.0 and 2.1: COMPARATIVE TECHNOLOGY ASSESSMENT and INTEGRATED SUBSYSTEM SPECIFICATIONS

These tasks are essentially complete as reported last time, but we are continuing to monitor the progress in other technologies and the evolving subsystems requirements as they relate to the HTS components development.

TASK 2.2: FUNCTIONAL COMPONENT AND SUBSYSTEM DESIGN, FABRICATION, AND TESTING

Filterbank and Delay Line Packaging

The packaging and characterization work reported here is related to progress made in the parallel High-Temperature Superconducting Space Experiment-II (HTSSE-II) program. We have used the filters and delay line to be delivered to HTSSE-II as test vehicles for the fabrication and packaging developments achieved in this ONR/DARPA program. Although the HTSSE-II filterbank will have different electrical characteristics from those in this program this approach is appropriate since all the packaging and characterization required for repeatable results are common to all devices made in both programs.

As mentioned in our last report, we are developing a capability for packaging HTS devices in housings made of niobium. Significant progress has been made in this area during this reporting period. Currently, our packages comprise a center piece containing glass-bead based coaxial connectors and the side walls to the package. The substrate is soldered to a carrier which is subsequently soldered to the center section of the package. Top and bottom lids are then added. Detailed drawings of the microstrip packaging concept developed in this program are shown in Appendix A. Each package will hold a filterbank channel comprising two identical filters and two hybrids.

Three soldering steps are require in the assembly. The melting points of the solders must be in decreasing order so that the soldering in a given step does not melt the solder in the previous step. The chosen solders are, at this point:

InPb for the glass beads

In for the substrate-to-carrier joint, and

InCd for the carrier-to-center piece joint.

The following packaging issues have been addressed:

- Gold plating: A technique for plating the Nb packages has been adapted and optimized from one used at our Electronics Systems Group for conventional microwave packages. It is important to plate these packages with a gold layer approximately 5 μm thick in order to improve their surface resistance and to provide the proper material for soldering the glass beads and the carriers.
- Lid welding: A laser welding technique has been developed for the hermetic sealing of niobium packages.
- Fluxless bead soldering: In a previous program we established the use of glass-bead based connectors in our microwave HTS devices. We now have developed a method which avoids the use of flux by soldering the beads in place in vacuum. This is important to prevent the possible contamination and hence degradation of the YBCO film device.
- Alternate coaxial connectors are being evaluated which could be inserted after the substrate has been mounted on a one-piece package. This is in contrast to our present arrangement, which requires the coaxial glass beads to be put in place before the substrate, making the package more complicated than would be desirable. These connectors, which are of the spark-plug type and use a knife-edge hermetic sealing feature, are being tested for cryogenic use.

- A stripline package was designed and tested for the delay line. The concept was shown to work and tested on a first 25 nS delay line built for the parallel HTSSE-II program. Detailed drawings of this package are included in Appendix B.

Filter Design of 7-Pole Filter Using 10 mil LAO

Four contiguous (3 dB crossovers) 7-pole filters with a $\cos^3$-shape passband with characteristics discussed in the last report are being designed. A power splitter is used at the input to separate the even and odd numbered filters to prevent the interaction between adjacent passbands.

These filters are being designed for 10-mil $LaAlO_3$ substrates so as to be able to fabricate one channel in a 2" diameter wafer. Each channel, as in the HTSSE-II project, comprises pairs of identical filters and hybrids, respectively.

This design is not fully optimized yet. Figure 1 shows the four passbands and Figure 2 the electrical schematic circuit.

Delay Line Designed

A 25 nS delay line has been deigned as a 1.55m long length of stripline in $LaAlO_3$. The configuration chosen is a double-wound spiral on a 10 mil thick substrate. This is shown in Figure 3. The coupling between adjacent lines in the spiral is about -50 dB. A preliminary result on a first version of this delay line, fabricated for the HTSSE-II program has a 19 nS delay instead of 25 nS, possibly due to an air gap between substrates. The package is now being optimized.

In this device, a coaxial-to-microstrip transition is made before going into the stripline delay line proper through a microstrip-to-stripline transition (see drawings in Appendix B). Using three-dimensional electromagnetic field simulation software, we have modelled these transitions and obtained return losses greater than 20 dB between 2 and 6 GHz.

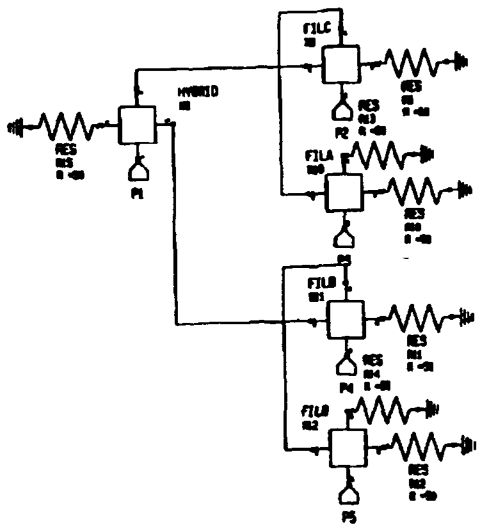


Figure 1 - Schematic diagram of the 4-channel filterbank.

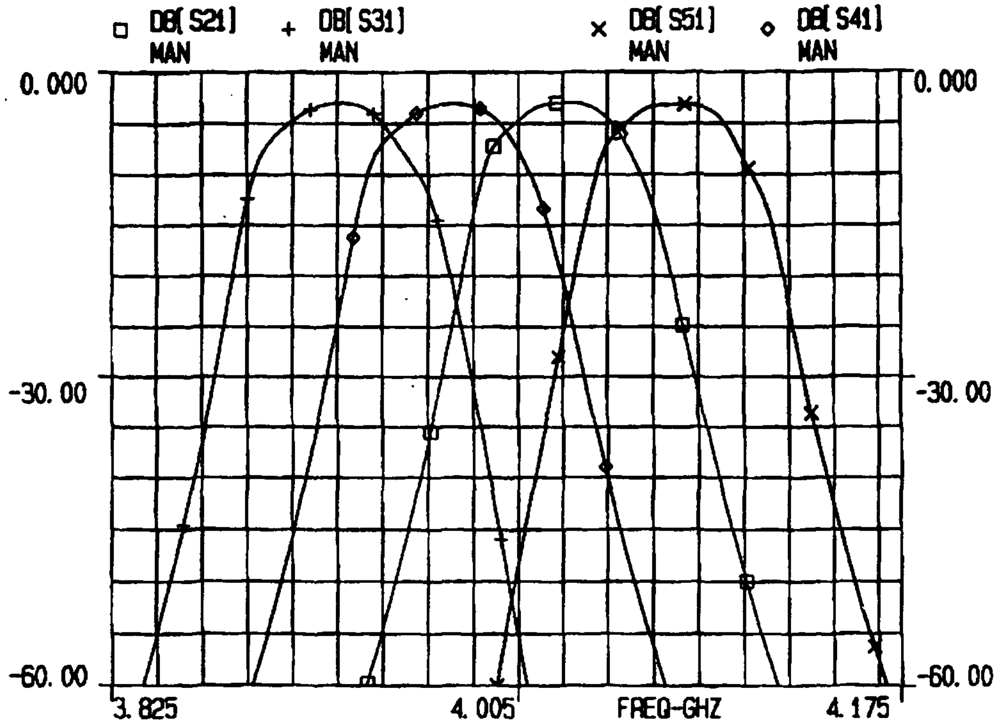


Figure 2 - Designed response for the 4-channel filterbank (7-pole filters with $\cos^3$ passband shapes).

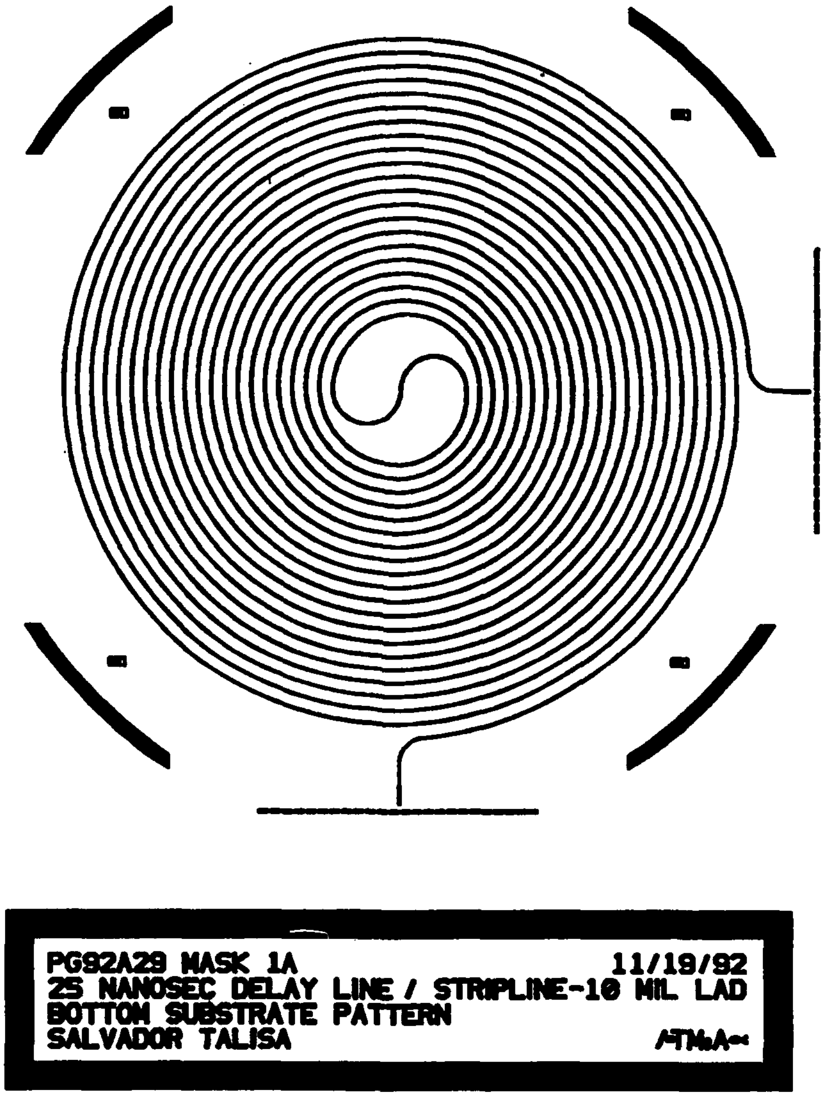


Figure 3 - Layout of 25 ns delay line on 2-inch-diameter $LaAlO_3$ substrates (stripline configuration).

TASK 3.1: PVD MULTILAYER FILM FABRICATION

Task 3.1.2, the production of YBCO films on 2-inch diameter $LaAlO_3$ wafers for fabrication of filterbanks and delay lines under Task 2.2, began at the start of this quarter. Three types of films were produced:

- Two-sided films on 10 mil thick wafers for the patterned spiral and one ground plane of stripline delay lines.
- Single-sided films on 10 mil substrates for the second ground plane required for stripline delay lines.
- Two-sided films on 20 mil thick substrates for each channel of the microstrip filterbank.

All YBCO films were deposited by off-axis rf magnetron sputtering. Two nominally-identical vacuum systems were used to produce them. The configuration of internal surfaces of the deposition chambers was optimized earlier in this program to eliminate the formation of copper oxide "boulders" which readily nucleate on the surface of a YBCO film during growth. At the same time, the sputter source, substrate, and substrate heater had to be enclosed by thermal insulation to form an oven in which the $LaAlO_3$ wafer, despite its low infrared absorption, could reach the desired growth temperature of approximately 700°C.

Under Task 3.3, the rf surface resistance, R_s, was routinely measured for the films grown on 20 mil thick substrates at 10 GHz and 77K. An R_s less than 0.5 mΩ at the operating frequency is the critical parameter used to qualify wafers for use as filters before committing them to patterning, packaging, and testing. One wafer was measured as a function of temperature in the range of 20-90K primarily to provide one of the inputs needed to determine sensitivity to small temperature deviations from 77K.

The rf surface resistance was not routinely measured for the thinner, 10 mil, wafers. The primary reason was that with additional handling of wafers intended for delay lines, there was an additional risk of introducing dust or dirt which would affect the patterning of the spiral. Since the linewidth of the spiral is 22 μm, even 1 μm particles could cause reflections and unwanted resonances in the delay line. In contrast, the linewidths for the microstrip filters are on the order of 0.5 mm and micron-sized defects are not a concern. A secondary reason for using YBCO films on 10 mil wafers without qualifying each one is that they are fragile until they reach the packaging step in which they are soldered to niobium carriers.

The development of YBCO films on 4-inch diameter wafers was scheduled to begin 9 months from the start of the contract. Instead, it will begin in December, 1992 when, at no cost to the project, a sputtering system designed for this purpose will be delivered and installed. The delivery is 5 months later than anticipated when the order for the system was placed in December, 1991.

The development of YBCO/insulator/YBCO trilayers continued in which deposited epitaxial insulators were used in place of a single crystal substrate. A summary of the dissipative properties of various insulators is shown in Figure 4 for four different insulator compounds. The error bars show the range of measured dc resistivity values in planar trilayer structures. The position on the horizontal axis is determined from data in the literature on bulk samples. The shaded areas show the minimum requirements for a number of applications. The conclusion from Figure 4 is that $SrAl_{0.5}Ta_{0.5}O_3$ (SAT) meets the dielectric loss requirements of all the applications and $SrTiO_3$ meets the requirements for most of them.

The requirements for the real part of the dielectric constant are not shown in Figure 4. Both multi-chip modules (MCM's) and, to a lesser extent, rf analog crossovers require low dielectric constants, $\epsilon \leq 6$, whereas SAT has $\epsilon \approx 25$. A set of masks has been made and the first chips processed in which the properties of insulators can be tested in the non-planar configurations encountered in practical circuits. Figure 5 shows the layout of one chip from the mask set. The test structures on this chip were designed to investigate the properties of deliberate YBCO-YBCO shorts (areas A and B), vias (C-H), and crossovers (16 devices in the center of the chip). Other chips test the effectiveness of step coverage by both YBCO and insulator layers, permit measurements of critical current densities for non-planar YBCO bridges, and allow for removal of $SrTiO_3$ supports to form air bridges for low-ϵ crossovers. The first data from such chips showed that $SrTiO_3$ insulators had a dc resistivity $\geq 5 \times 10^7$ Ω-cm in non-planar YBCO crossovers, at least as high as the lower error bar in Figure 4.

TASK 3.2: MOCVD MULTILAYER FILM FABRICATION

This task was delayed due to funding delays and internal reorganization problems at EMCORE, the subcontractor to develop the plasma-enhanced MOCVD process. During this quarter, work began at EMCORE on YBCO film growth and at Northwestern University on alternate precursors for Ba and precursors for deposited epitaxial insulators.

EMCORE films were sent to Westinghouse for evaluation. Although the critical temperatures and x-ray diffraction data were good (T_c's ≈ 87K, $\Delta\omega = 0.45°$, <5% a-axis growth), the rf surface resistance, R_s, was much higher than the 50-70 mΩ values obtained at 77K and 94 GHz at Sandia Laboratory on an earlier EMCORE film. While efforts to repeat the growth conditions used for that earlier film continued, a substrate holder was fabricated to permit growth on both sides of $LaAlO_3$ wafers.

Several precursor compounds for Ba were evaluated at Northwestern University and in the Westinghouse STC laboratory of R. G. Charles, a consultant working on this task, where a DTA vapor pressure measurement apparatus was assembled. Six compounds prepared at Northwestern were sent to Westinghouse for vapor pressure measurements. A larger batch, sufficient for several film deposition runs, of the compound, $Ba(hfa)_2$-tetraglyme, was sent to EMCORE to replace their standard Ba precursor in upcoming YBCO depositions.

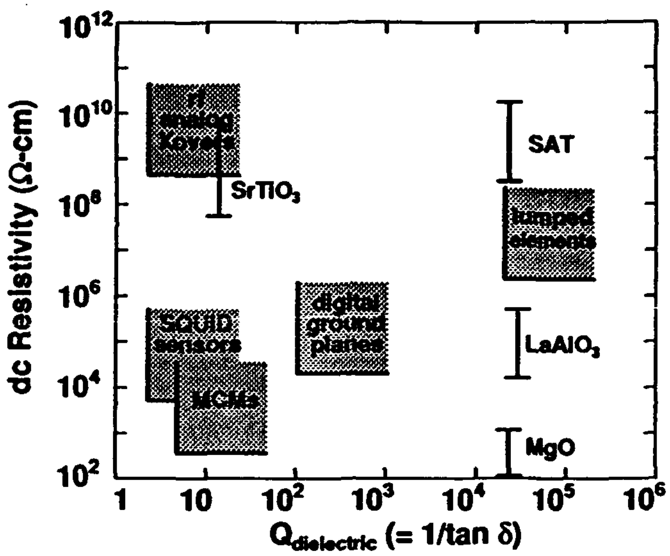


Figure 4 - Comparison of dielectric loss data for $SrTiO_3$, MgO, $LaAlO_3$, and SAT films grown epitaxially on YBCO, with the minimum requirements of several applications for dc resistivity and 1/tan δ.

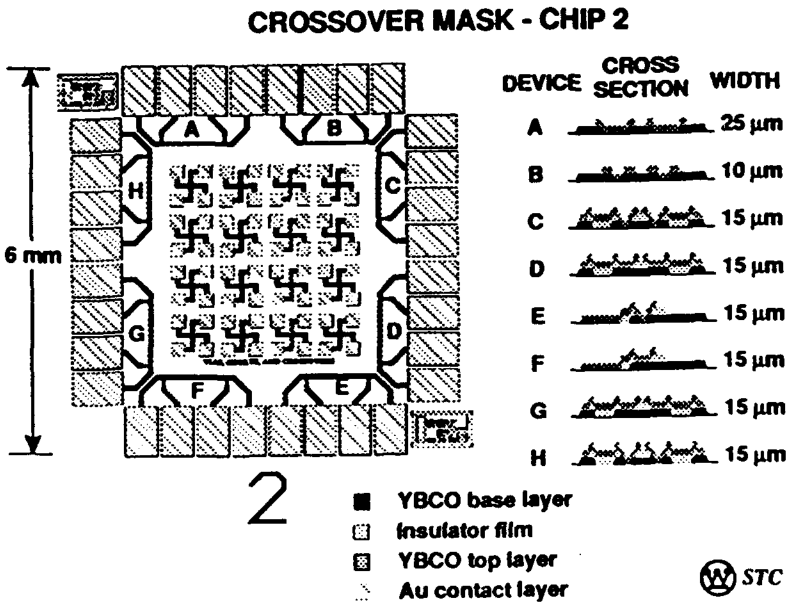


Figure 5 - Mask layout for one of the chips in a mask set designed to test YBCO and epitaxial insulator properties in practical configurations. Cross-sectional views of some of the configurations are shown in the right-hand half of the figure.

The best epitaxial insulator known at this time, $SrAl_{0.5}Ta_{0.5}O_3$ (SAT), was deposited at Northwestern University by MOCVD. An optimum growth temperature was established and both patterned and unpatterned YBCO films grown at Westinghouse were sent to Northwestern to serve as substrates for insulator growth. Another promising epitaxial insulator, $PrGaO_3$, which was developed at Northwestern prior to the start of this contract, will be deposited by MOCVD on several of the YBCO chips for evaluation at Westinghouse.

TASK 3.3: RF CHARACTERIZATION OF FILM PROPERTIES

Parallel plate resonator measurement for 1 cm^2 samples as well as 0.5" × 0.25" samples are routinely used to qualify films being developed at Westinghouse and Emcore. A copper cavity measurement set-up for 2" diameter wafers (end-wall replacement technique) is also in use. Measurements include the extraction of resonator unloaded Q (and hence surface resistance R_s) for any degree of input/output resonator coupling, so that a wide range of films qualities can be tested.

CHANGE IN KEY PERSONNEL

During this reporting period, Mr. T. E. Steigerwald has been replaced by Mr. G. K. Sinon as Deputy Program Manager at ESG, Baltimore.

PROBLEMS ENCOUNTERED AND/OR ANTICIPATED

Although the start date of this program was July 24, 1991 with the approval of anticipatory spending, the contract was not signed until September 30, 1991 when the first increment of funding was received. Our current allocation is sufficient for the first year of effort, but is designated to cover the work through October 31, 1992. This places the program three months behind schedule and will necessitate a request for a no-cost extension.

FISCAL STATUS

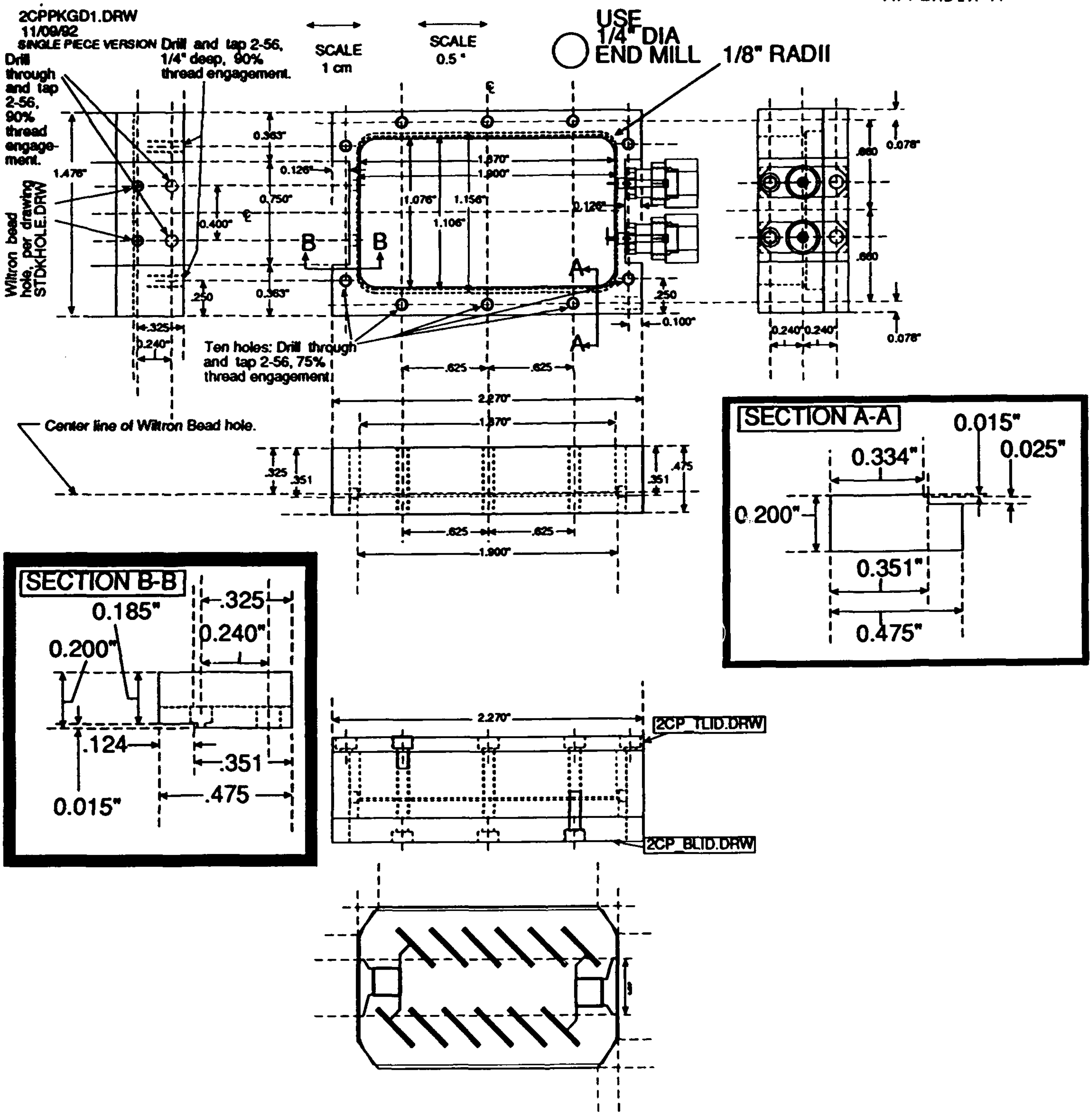
Amount currently provided	$1,600,000
Expenditures and commitments through 10/25/92:	1,490,660 *
Funds required to complete:	3,769,203
FY93 funds required:	1,827,386

*According to the unaudited statement of cost.

APPENDIX A

Filter Package Design

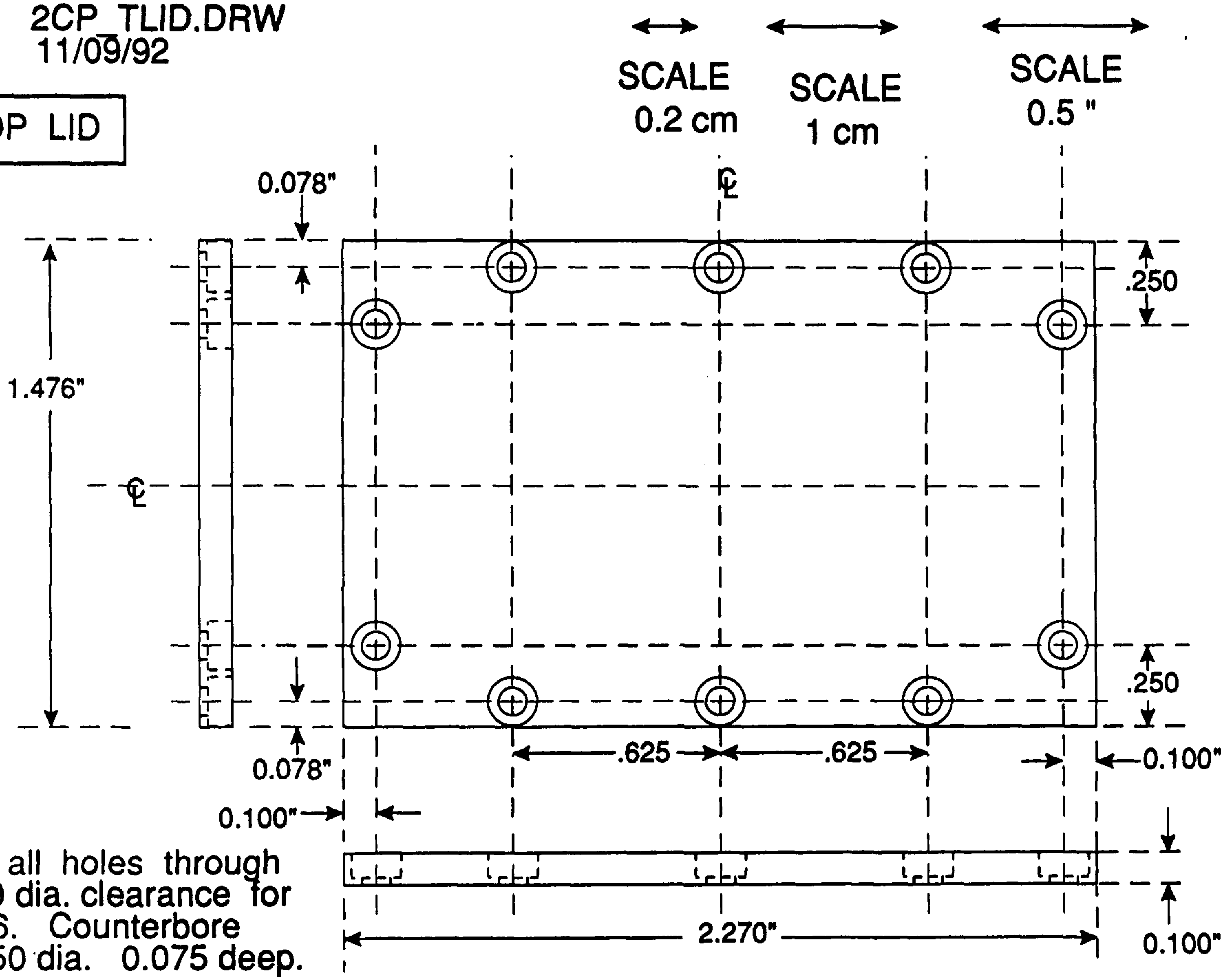
APPENDIX A



2CPPKGD1.DRW
11/09/92
SINGLE PIECE VERSION
Drill and tap 2-56, 1/4" deep, 90% thread engagement.
Drill through and tap 2-56, 90% thread engagement.
Wiltron bead hole, per drawing STDKHOLE.DRW
SCALE 1 cm
SCALE 0.5 "
USE 1/4" DIA END MILL
1/8" RADII
Ten holes: Drill through and tap 2-56, 75% thread engagement
Center line of Wiltron Bead hole.
SECTION A-A
0.334"
0.015"
0.025"
0.200"
0.351"
0.475"
SECTION B-B
0.185"
0.200"
.325
0.240"
.124
.351
.475
0.015"
2.270"
1.870"
1.900"
.625
2CP_TLID.DRW
2CP_BLID.DRW

2CP_TLID.DRW
11/09/92

TOP LID

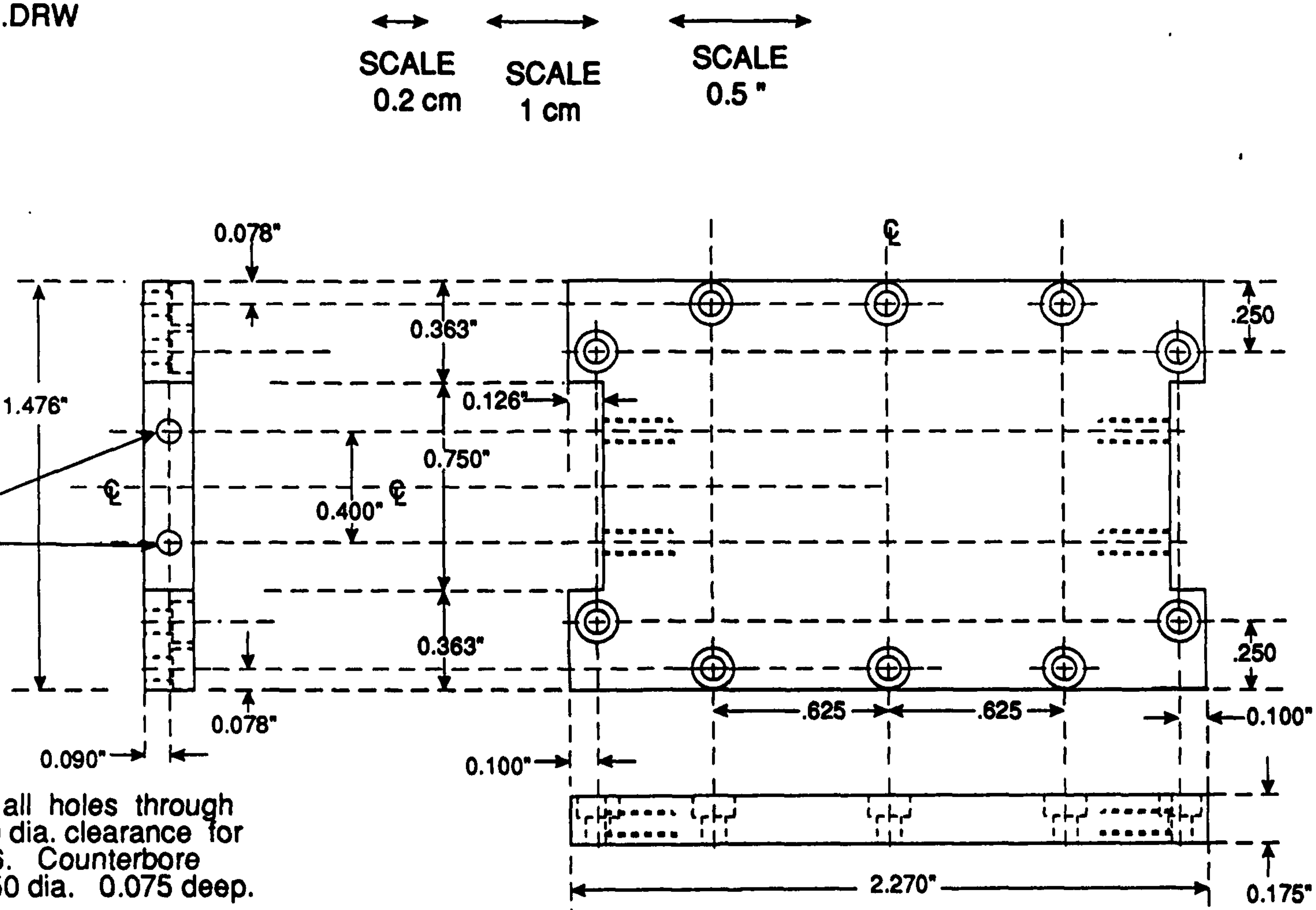


Drill all holes through .089 dia. clearance for 2-56. Counterbore 0.150 dia. 0.075 deep.

ENSURE THAT COUNTERBORED HOLES LINE UP WITH TAPPED HOLES ON BODY, 2CPPKGD1.DRW

2CP_BLID.DRW
11/09/92

BOTTOM LID

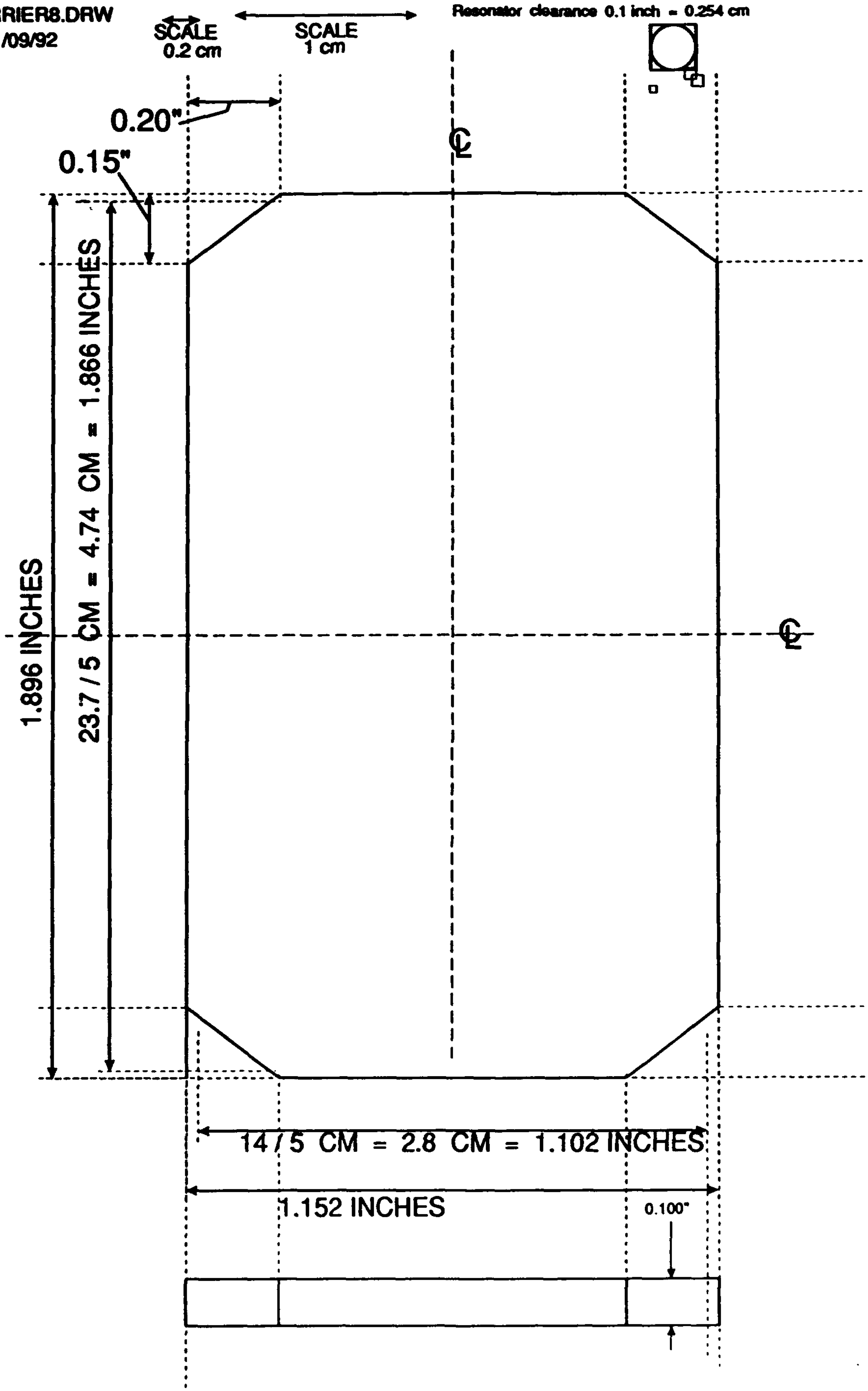


Drill 1/4" deep and tap 2-56, 90% thread engage- ment.

Drill all holes through .089 dia. clearance for 2-56. Counterbore 0.150 dia. 0.075 deep.

ENSURE THAT COUNTERBORED HOLES LINE UP WITH TAPPED HOLES ON BODY, 2CPPKGD1.DRW

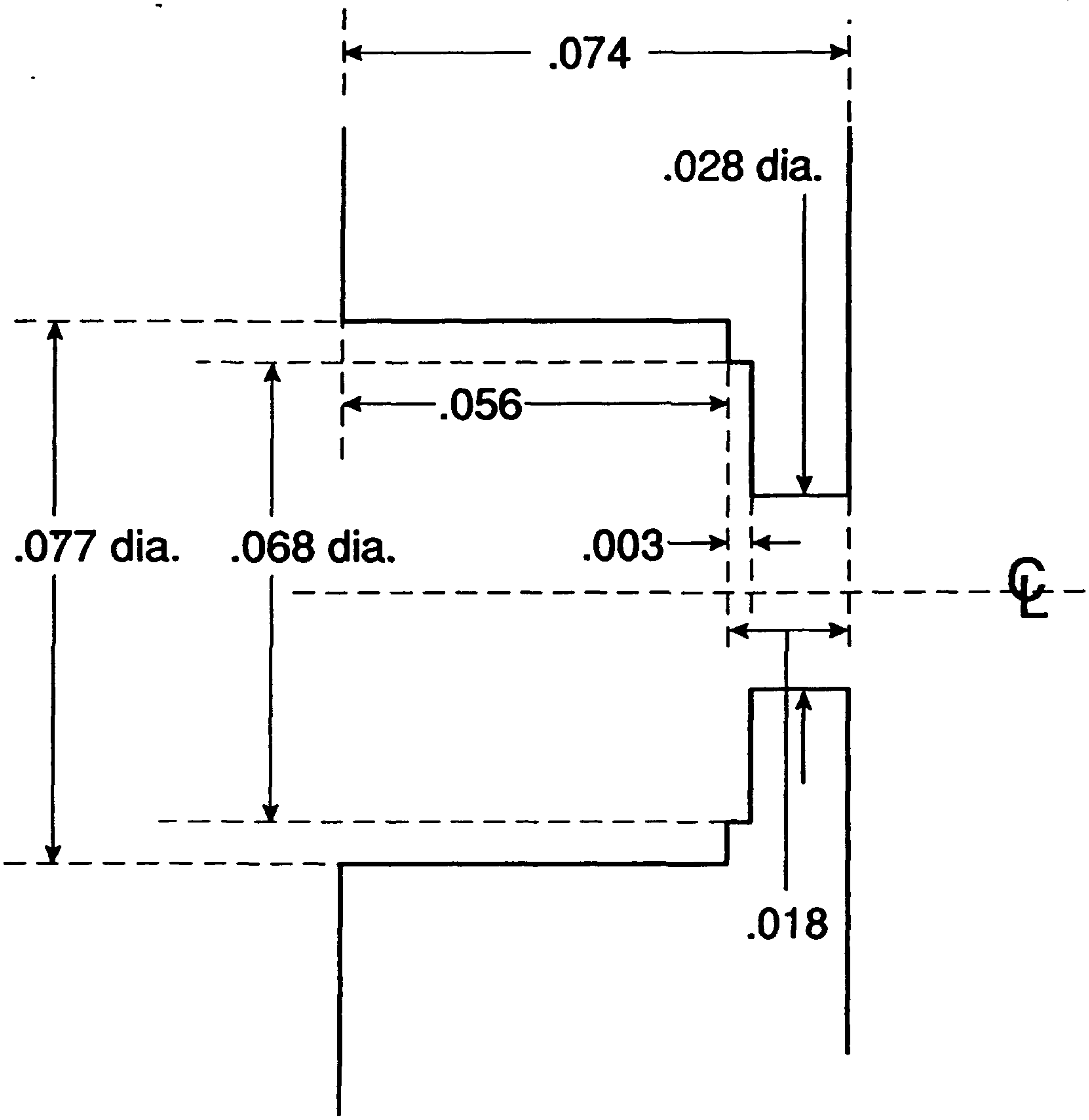
CARRIER8.DRW
11/09/92

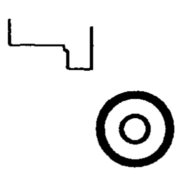


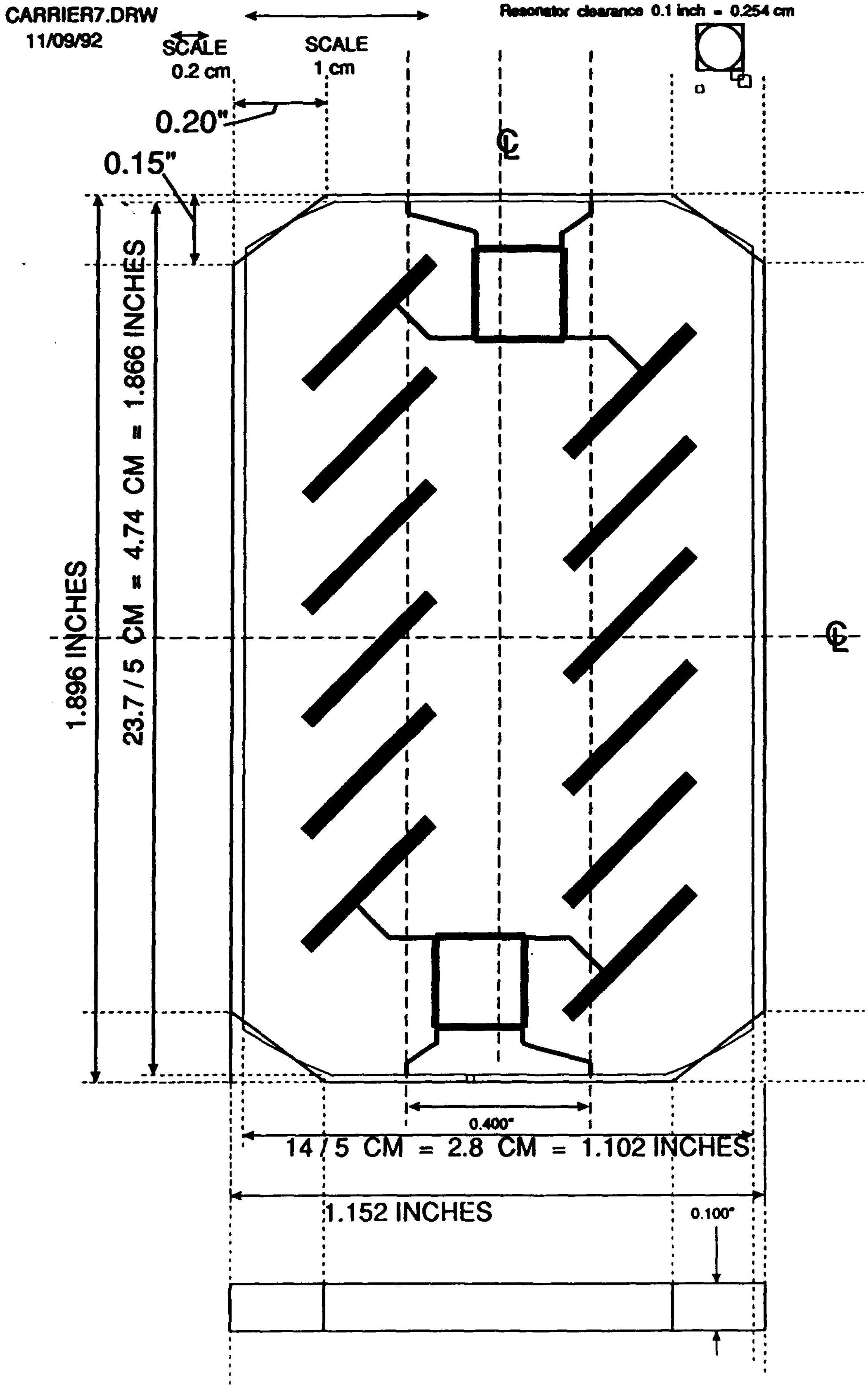
STDKHOLE.DRW
6/26/92

SCALE
0.025

Tolerances: $\pm$ 0.001, except diameters $\pm$ 0.0005
Hole concentricity $\pm$ 0.001

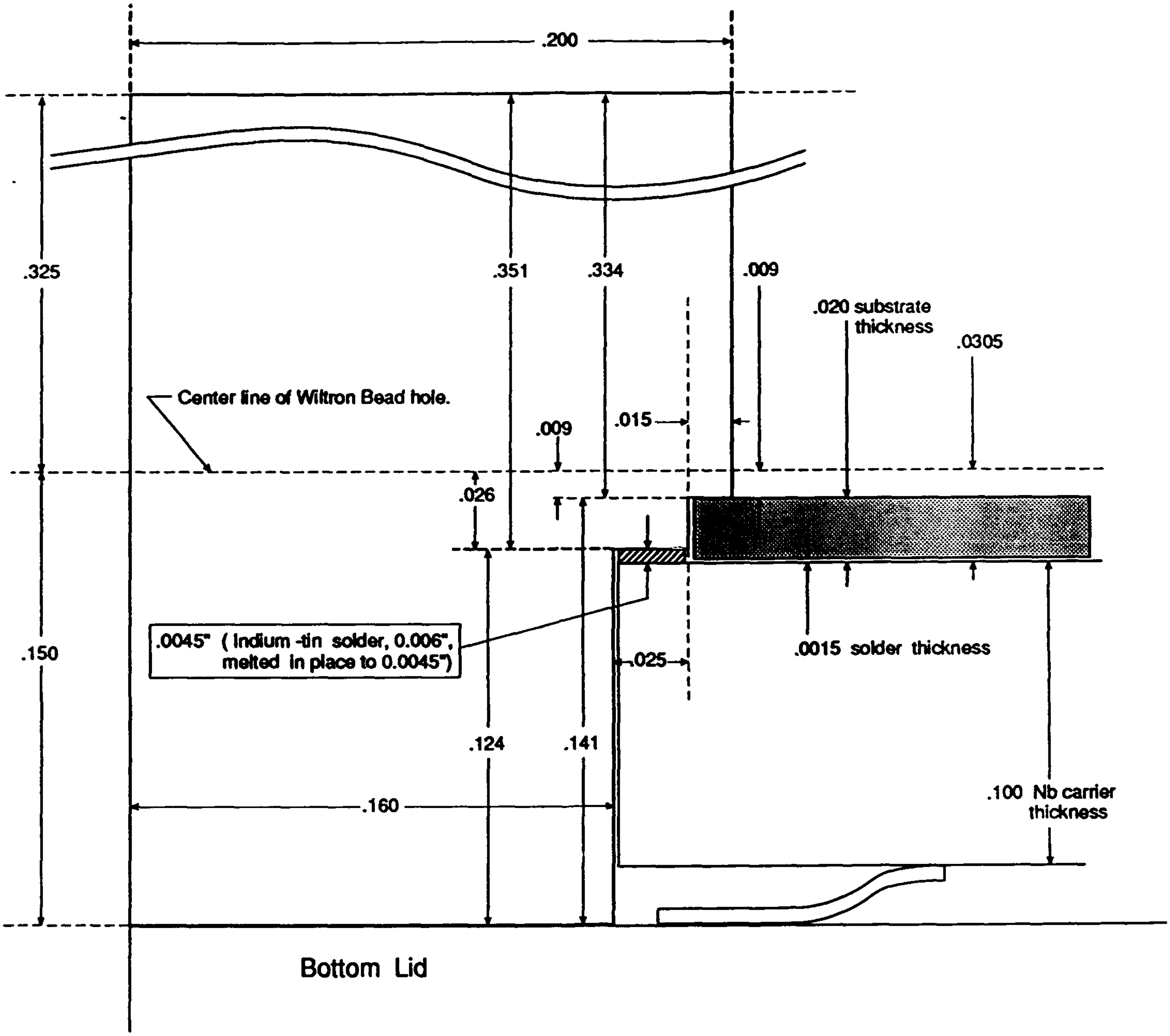


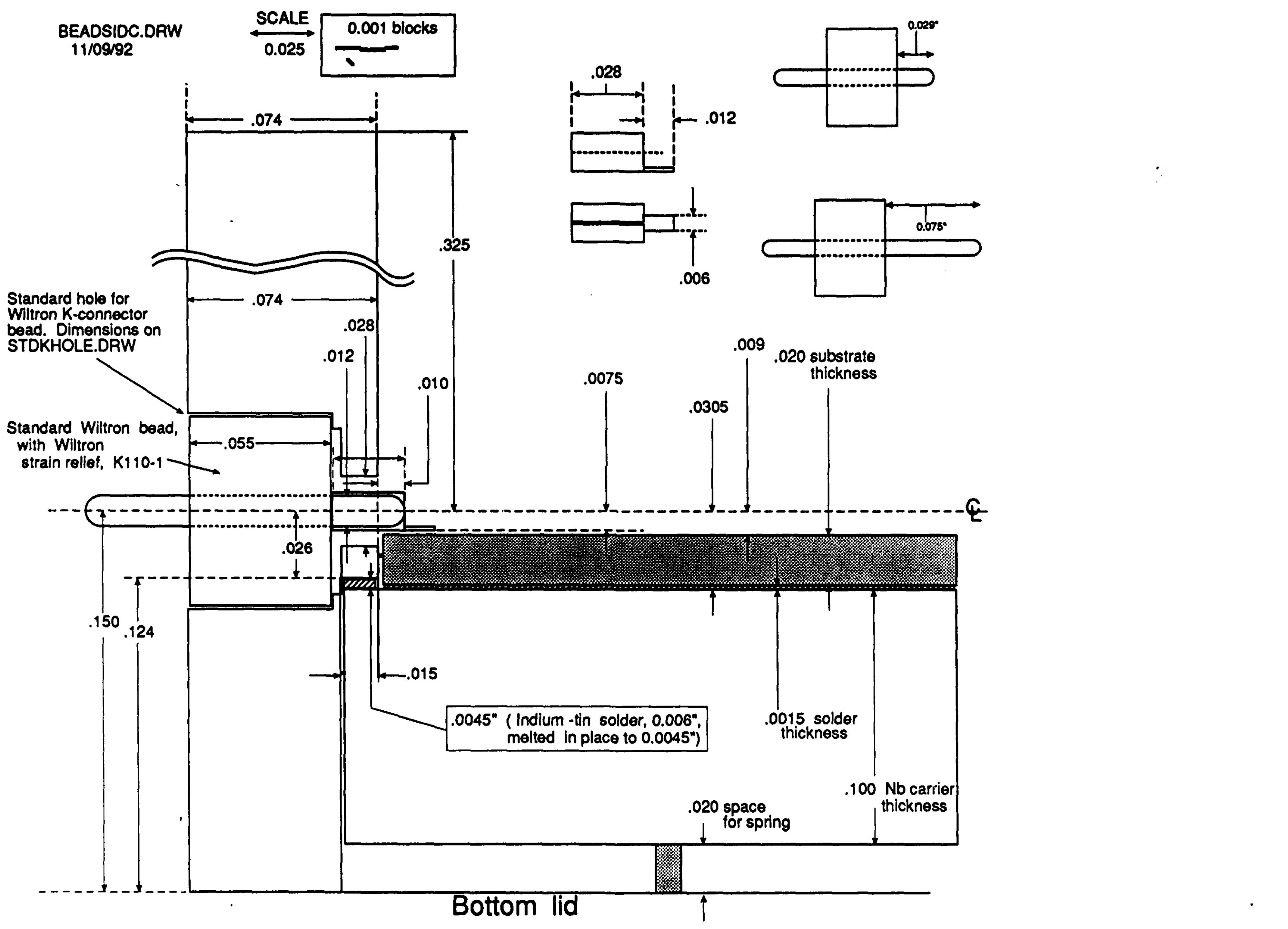



CARRIER7.DRW
11/09/92
SCALE
0.2 cm
SCALE
1 cm
Resonator clearance 0.1 inch = 0.254 cm
0.20"
0.15"
1.896 INCHES
23.7 / 5 CM = 4.74 CM = 1.866 INCHES
0.400"
14 / 5 CM = 2.8 CM = 1.102 INCHES
1.152 INCHES
0.100"

SIDEDSEC.DRW
8/04/92

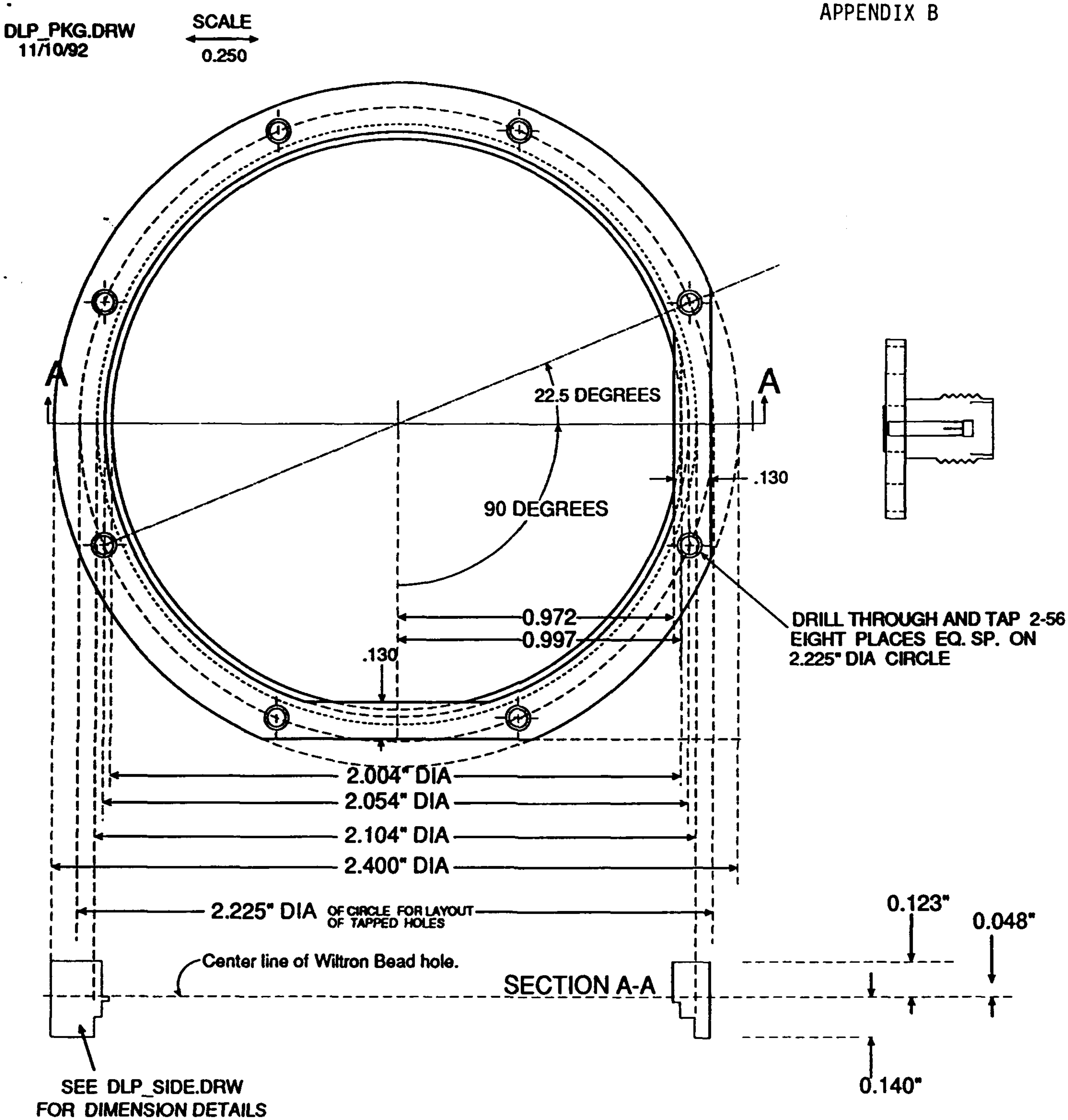
SCALE
0.025




BEADSIDC.DRW
11/09/92
SCALE
0.025
0.001 blocks
.074
.074
.325
.028
.012
.006
0.029"
0.075"
Standard hole for Wiltron K-connector bead. Dimensions on STDKHOLE.DRW
Standard Wiltron bead, with Wiltron strain relief, K110-1
.055
.028
.012
.010
.0075
.0305
.009
.020 substrate thickness
.026
.150
.124
.015
.0045" (Indium -tin solder, 0.006", melted in place to 0.0045")
.0015 solder thickness
.100 Nb carrier thickness
.020 space for spring
Bottom lid

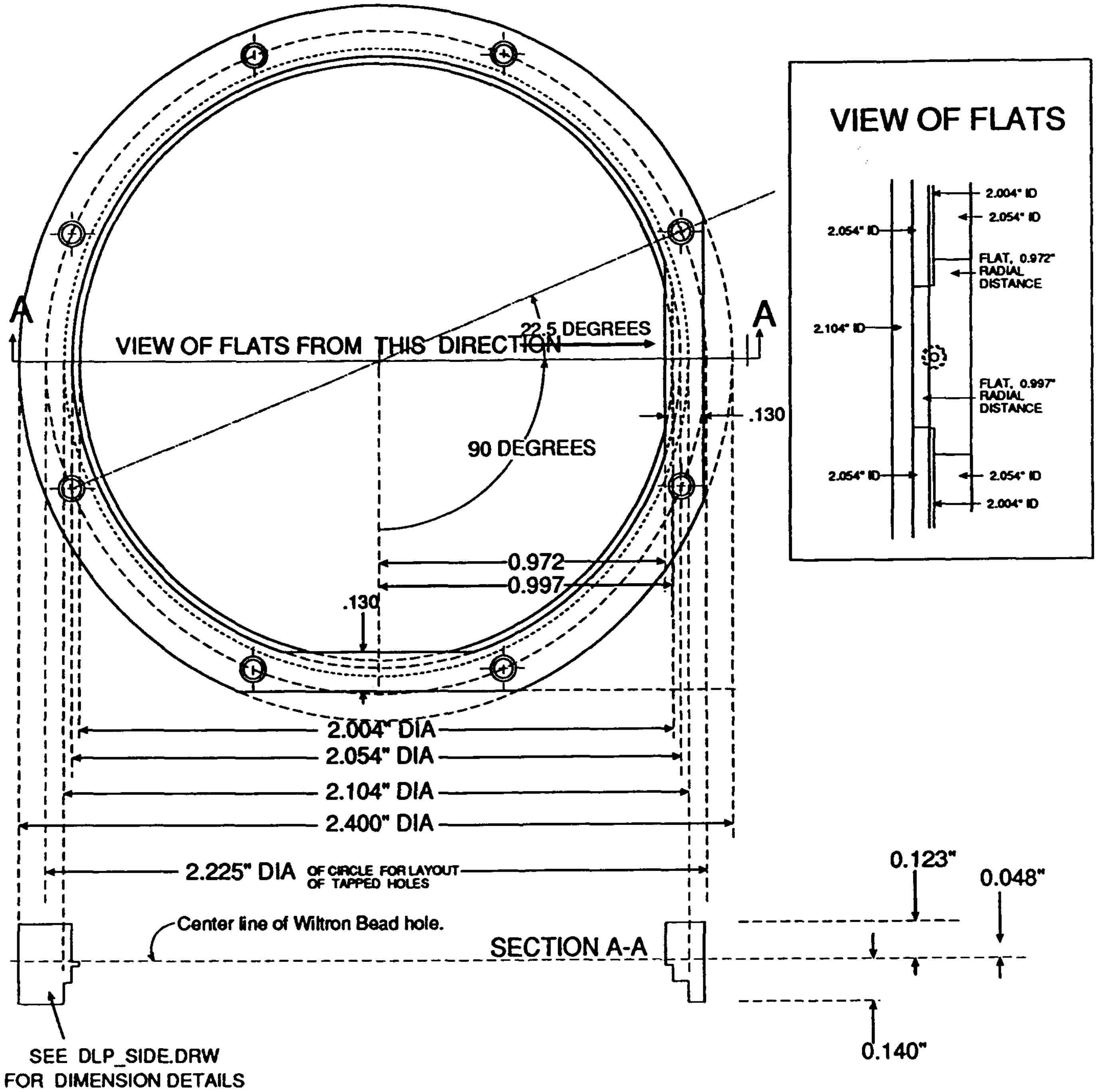
APPENDIX B

Delay Line Package Design


DLP_PKG.DRW
11/10/92
SCALE
0.250
A
A
22.5 DEGREES
90 DEGREES
.130
0.972
0.997
.130
DRILL THROUGH AND TAP 2-56
EIGHT PLACES EQ. SP. ON
2.225" DIA CIRCLE
2.004" DIA
2.054" DIA
2.104" DIA
2.400" DIA
2.225" DIA OF CIRCLE FOR LAYOUT OF TAPPED HOLES
0.123"
0.048"
Center line of Wiltron Bead hole.
SECTION A-A
0.140"
SEE DLP_SIDE.DRW
FOR DIMENSION DETAILS

DLPFLATS.DRW
11/11/92

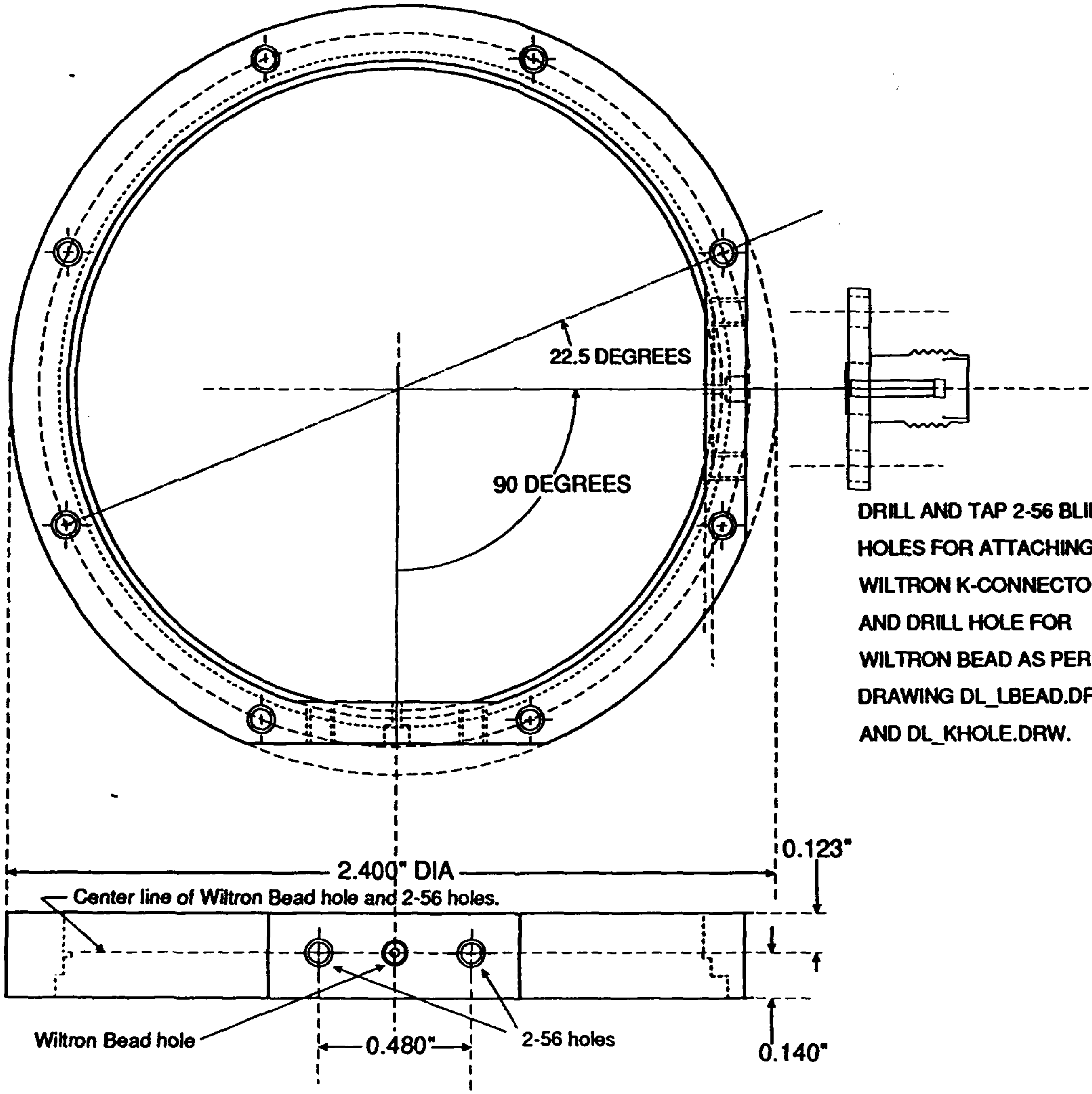
SCALE
0.250



DLP_PKG2.DRW
11/10/92

SCALE
0.250

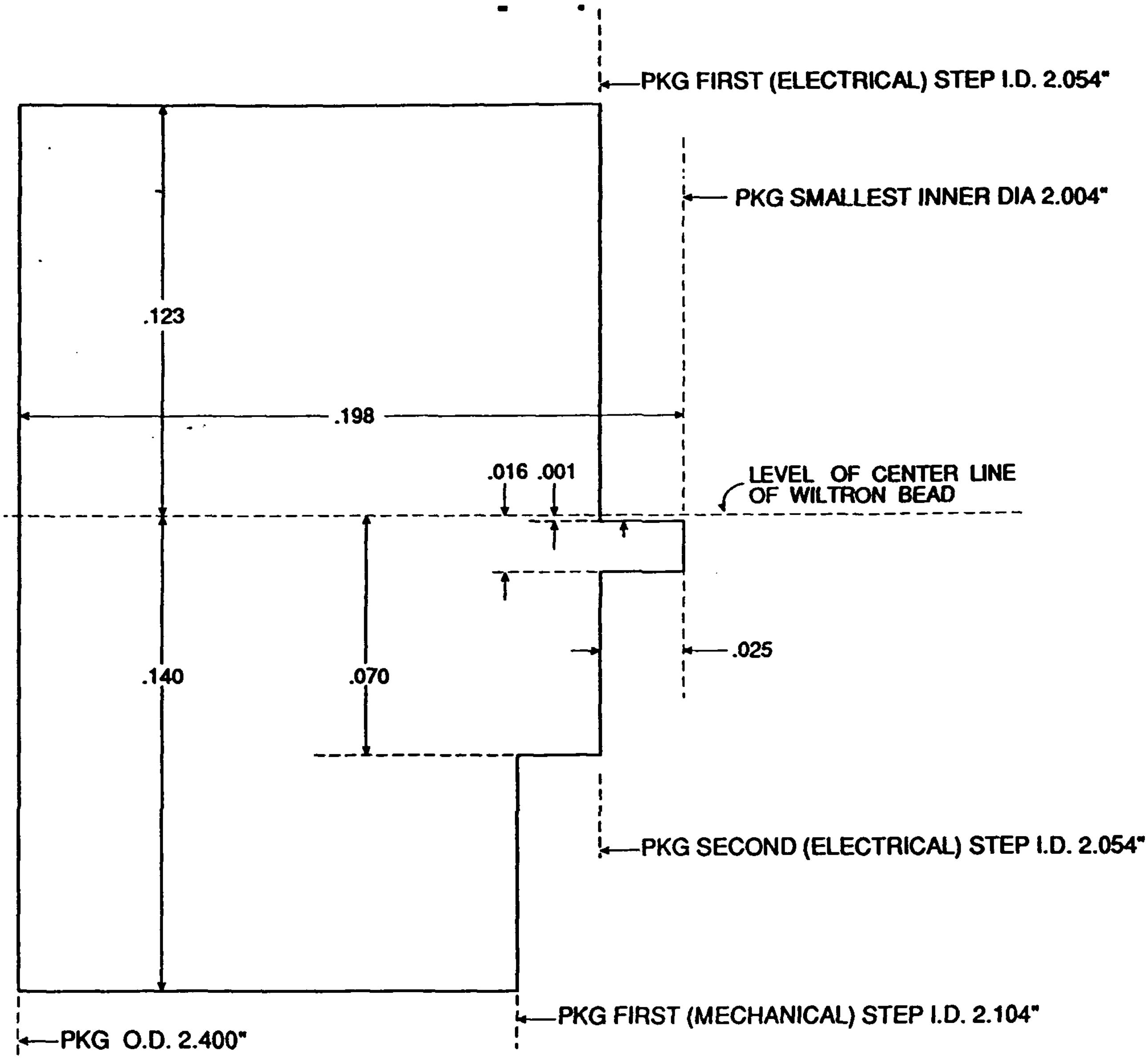
ADD HOLESFOR WILTRON BEADS
AND TAPPED HOLES FOR WILTRON K-CONNECTORS
ON FLATS



DRILL AND TAP 2-56 BLIND
HOLES FOR ATTACHING
WILTRON K-CONNECTOR,
AND DRILL HOLE FOR
WILTRON BEAD AS PER
DRAWING DL_LBEAD.DRW
AND DL_KHOLE.DRW.

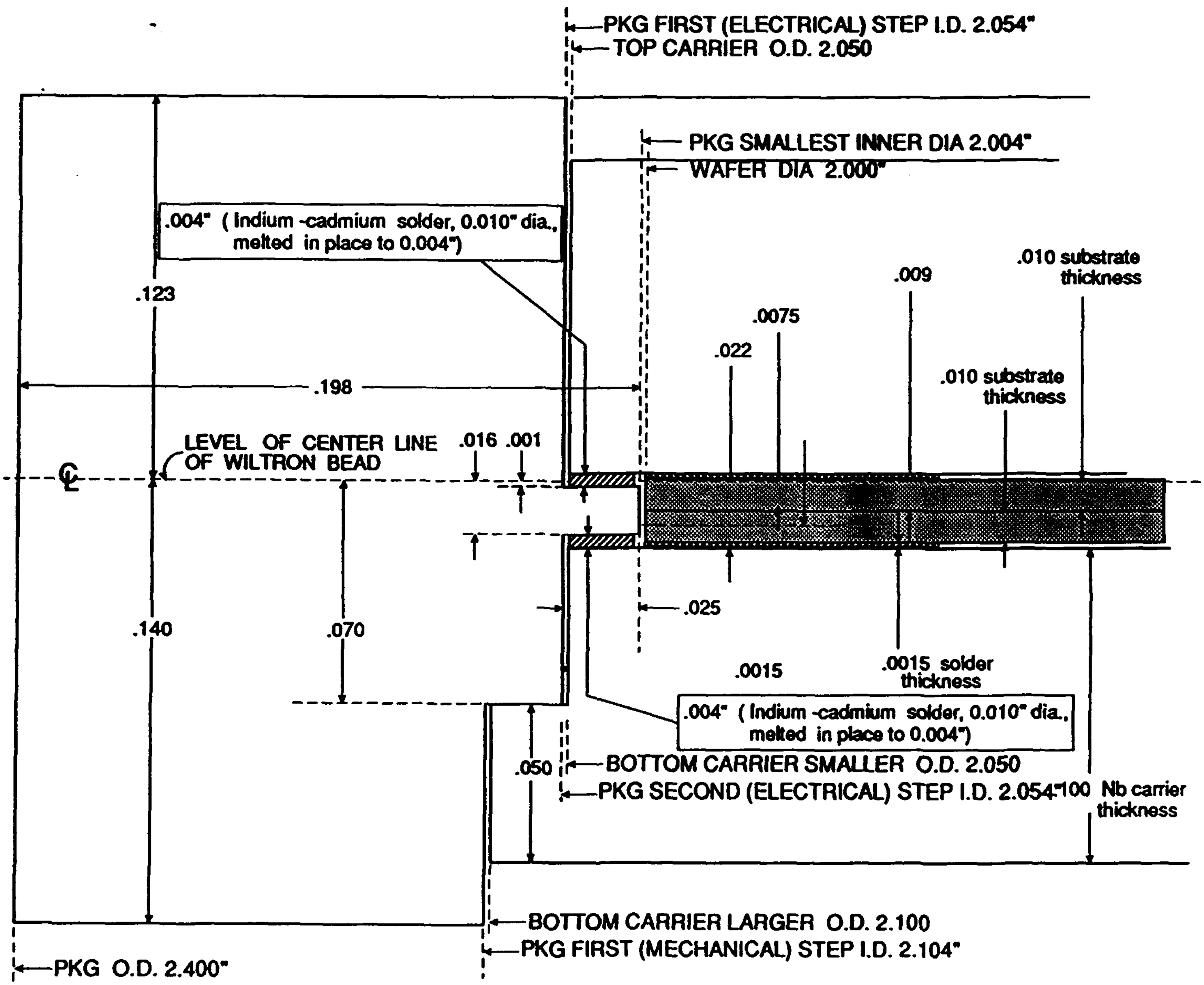
DLP_SIDE.DRW
11/10/92

SCALE
0.025

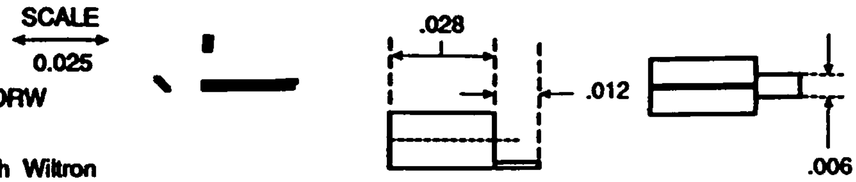


DL_CRSEC.DRW
11/10/92

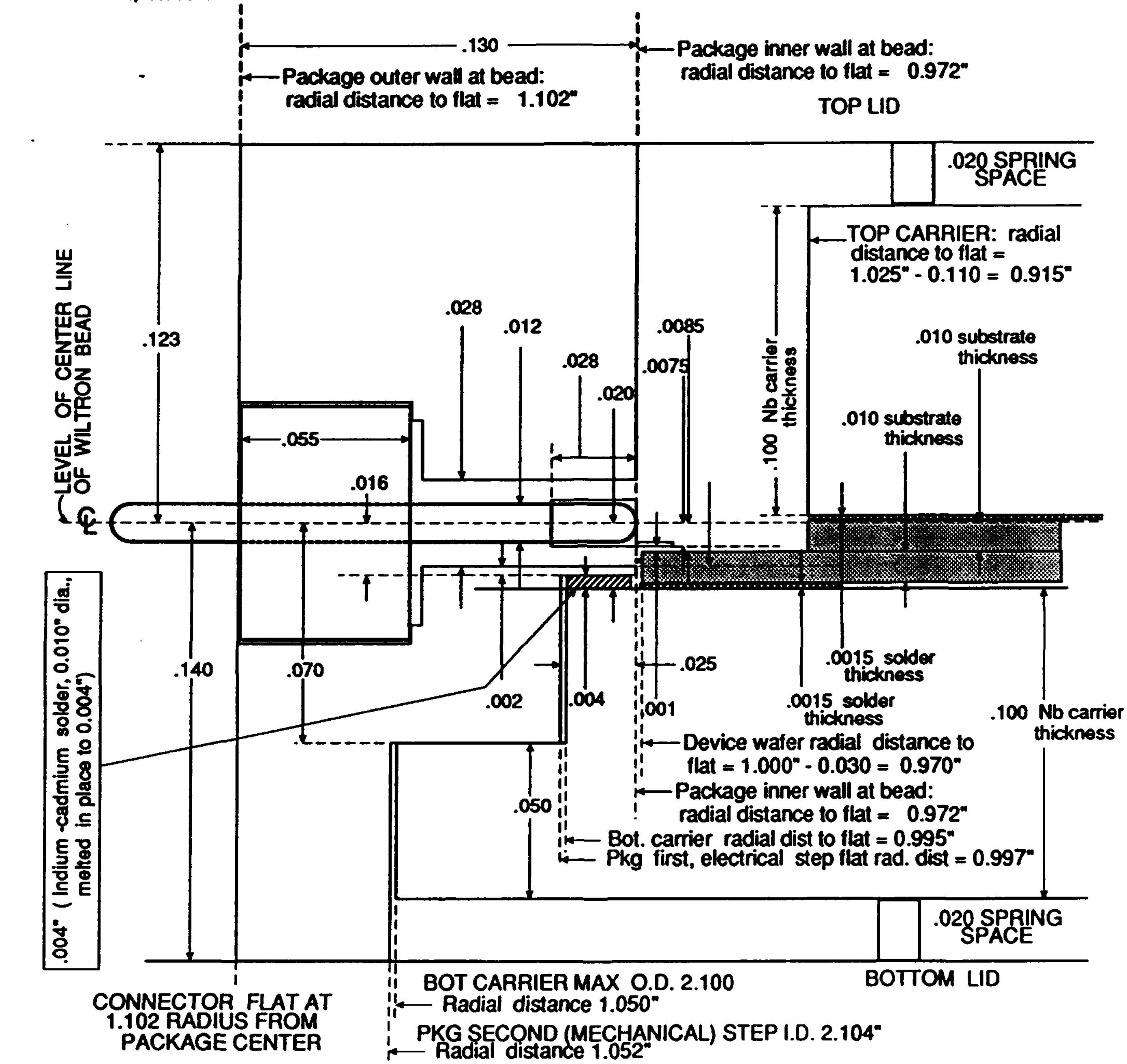
SCALE
0.025



DLPLBEAD.DRW
11/10/92
DelayLineProductionLongBEAD.DRW



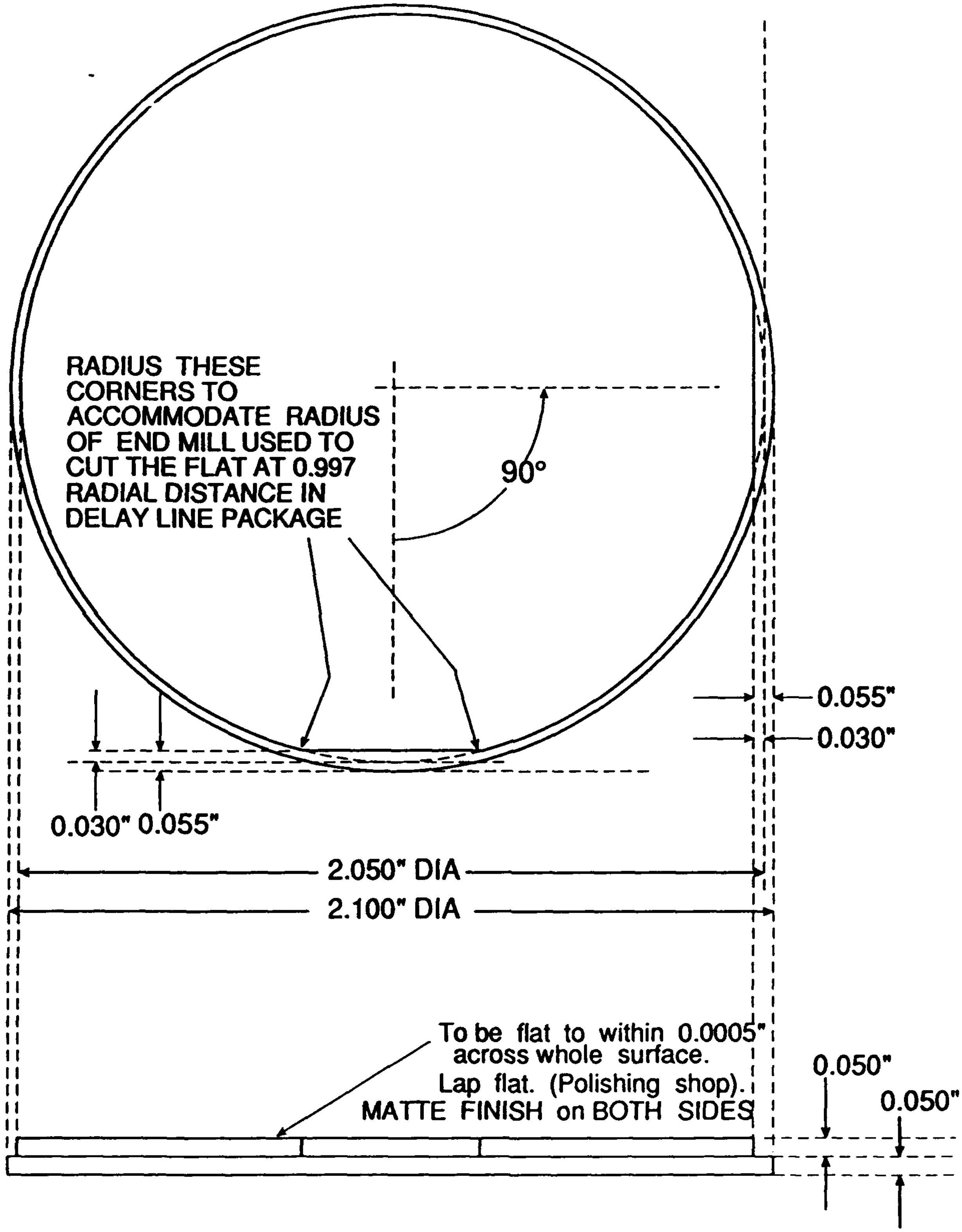
Modified bead/ longer pin, with Wiltron strain relief, K110-1



DLP_BCAR.DRW
11/11/92

SCALE
0.250

BOTTOM CARRIER

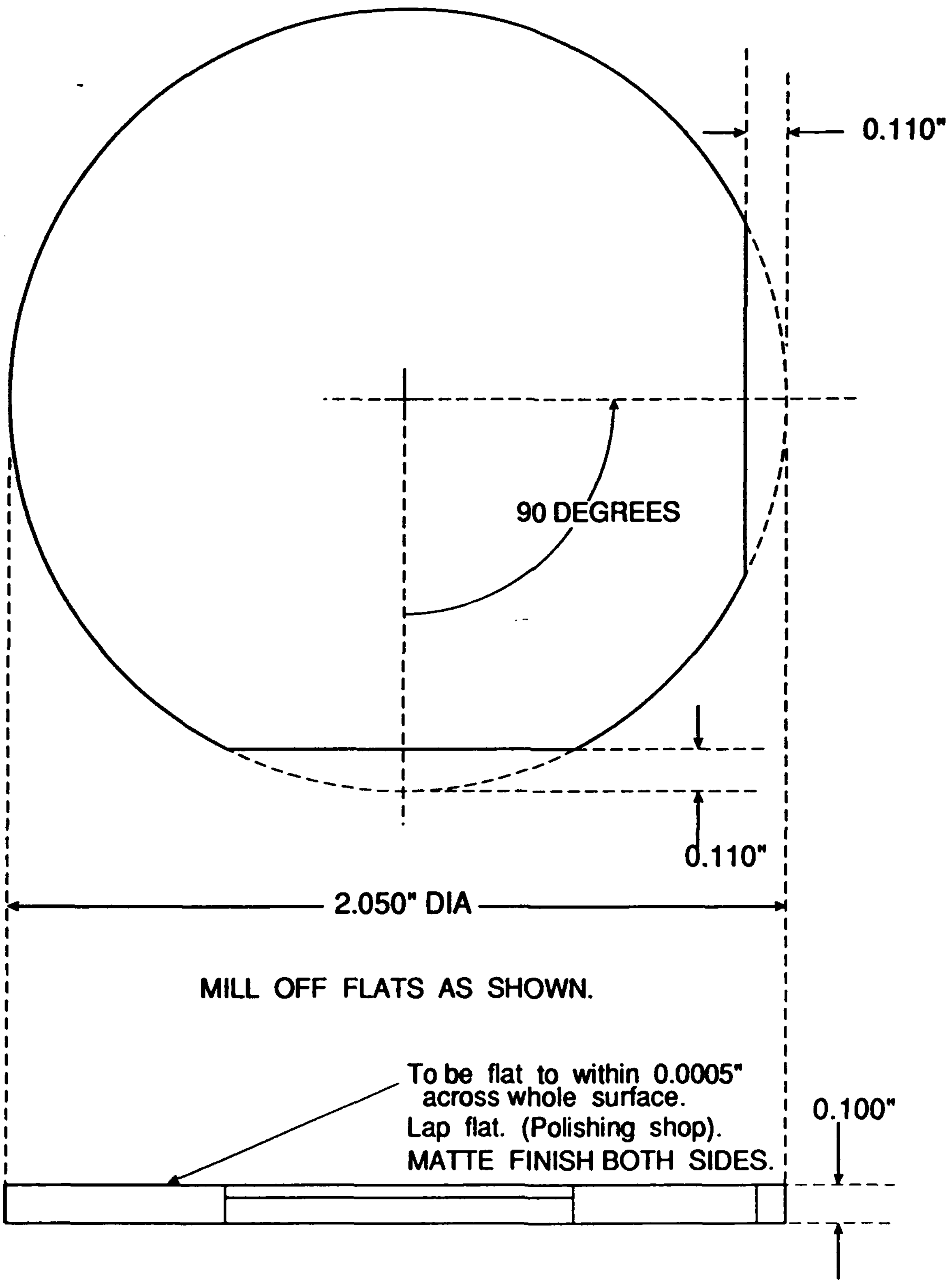


DLP_TCAR.DRW
11/10/92

SCALE
0.250

MODS: FLAT MOVED IN 0.035 FARTHER

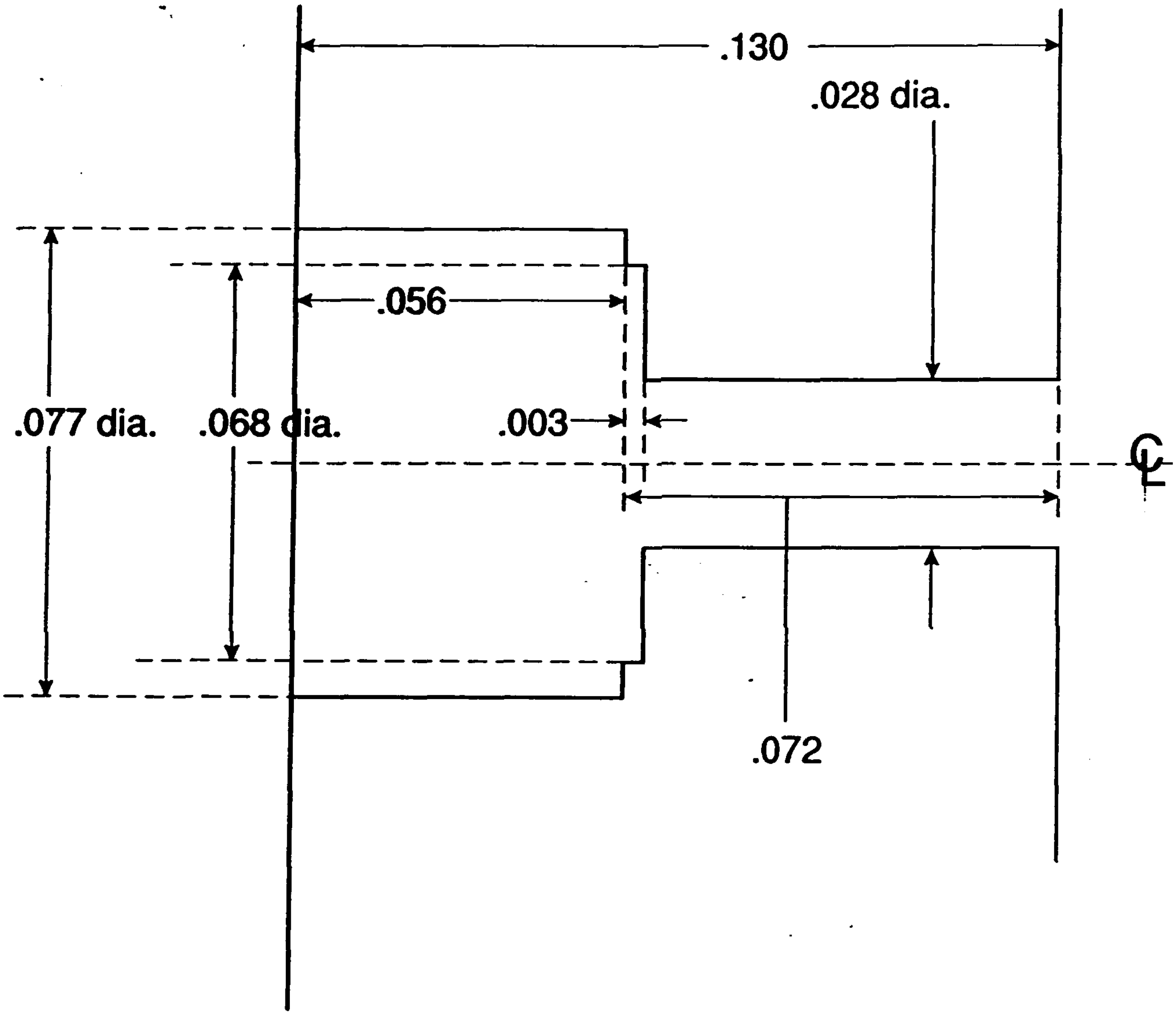
TOP CARRIER

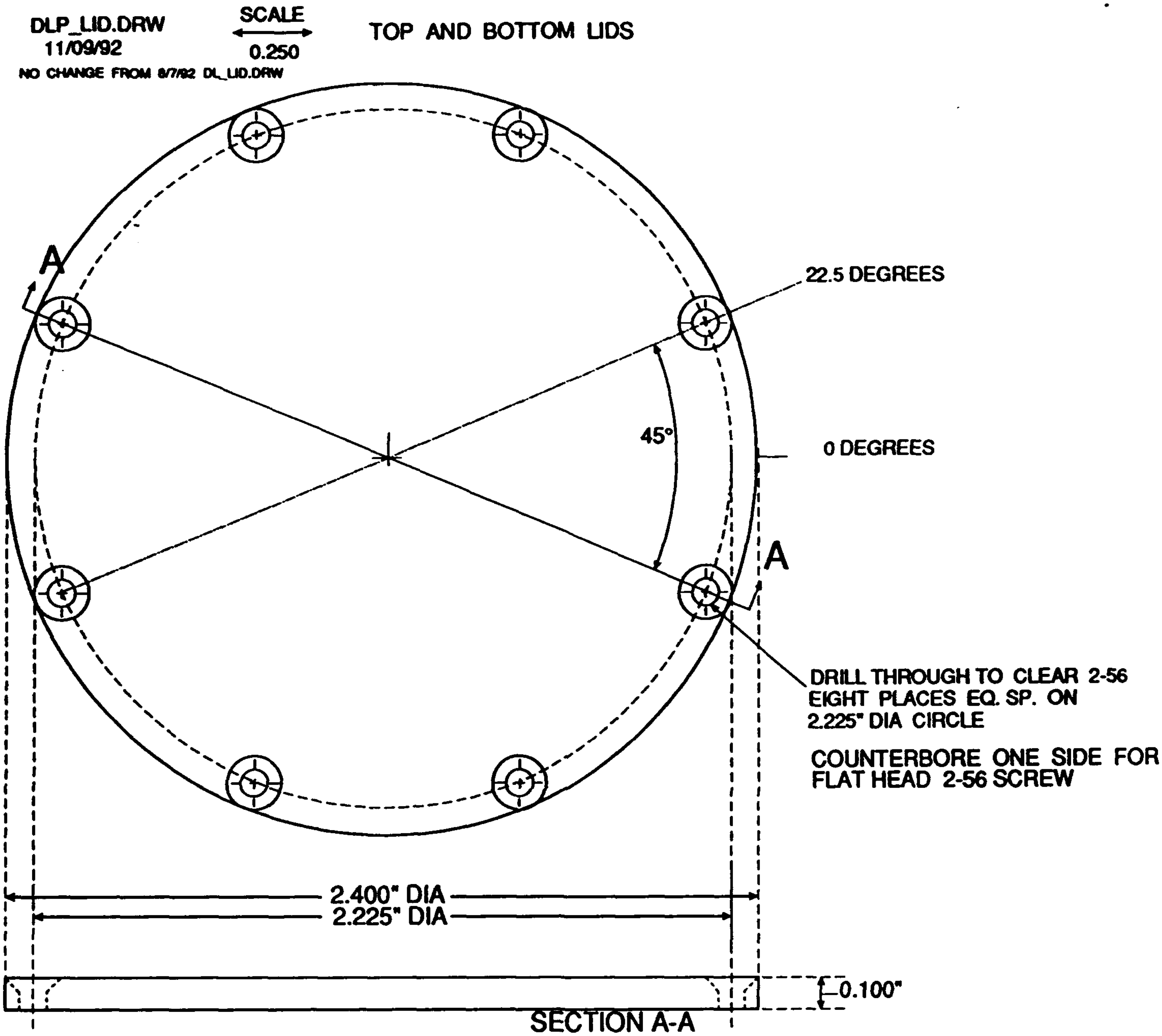


DL_KHOLE.DRW
9/22/92

SCALE
0.025

Tolerances: ± 0.001, except diameters ± 0.0005
Hole concentricity ± 0.001




DLP_LID.DRW
11/09/92
NO CHANGE FROM 8/7/92 DL_LID.DRW
SCALE
0.250
TOP AND BOTTOM LIDS
A
22.5 DEGREES
45°
0 DEGREES
A
DRILL THROUGH TO CLEAR 2-56
EIGHT PLACES EQ. SP. ON
2.225" DIA CIRCLE
COUNTERBORE ONE SIDE FOR
FLAT HEAD 2-56 SCREW
2.400" DIA
2.225" DIA
0.100"
SECTION A-A