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13. ABSTRACT *(Maximum 200 words)*
The objective of this program is to advance InGaAs materials technology to allow high performance imaging at room temperature in the 1.0-2.6 um near infrared band During Phase I, 128x128 pixel lattice-matched In.53Ga.47As focal plane arrays from 1-1.7 um were fabricated. The detectivity, D*, was 10(13) cm-Hz(.5)/W at room temperature and greater than 3x10(14) at 230K - a value very nearly background limited. The standard deviation in D* was 14% of the mean value and 98% of the pixels has a D* greater then 50% of the mean value. These results significantly advance the state-of-the-art and all of the abjectives of Phase I were met or exceeded. The goals of Phase II will be to advance the materials growth and processing technologies of lattice mismatched InGaAs so as to lower the dark current sufficiently that room temperature imaging in the 1.0-2.6 um band can be performed. This goal has proven elusive despite investments of tens of millions of dollars over more than a decade. Potential applications of this research include remote atmospheric sensing, LIDAR, satellite imaging, and near infrared spectroscopy.

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"A High Performance Room-Temperature Near-Infrared Camera"

Contract #SDIO-92/DAAL03-92-C-0040

U.S. Army Research Office (Research Triangle, NC)
Dr. Robert Trew (Technical Monitor)

Dr. Gregory H. Olsen (Principal Investigator)
Sensors Unlimited, Inc.
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SBIR Phase I Final Report
January 20, 1993

1. Project Summary

The primary objective of this program is to advance InGaAs materials technology so that high performance imaging can be performed at room temperature in the 1.0-2.6 μm near infrared band.

During Phase I, the viability of the InGaAs material system was evaluated by fabricating focal plane arrays for room temperature near-infrared imaging. Custom 128x128 pixel $In_{.53}Ga_{.47}As$ photodiode arrays were bonded, using indium bump techniques, to silicon readout multiplexers supplied by both EG&G Reticon and Rockwell International. The resultant focal plane arrays (FPAs) were sensitive to radiation in the 1-1.7 μm range.

FPAs bonded to Rockwell readout multiplexers were characterized for detectivity (D^*) and uniformity as a function of temperature. At room temperature, the detectivity measured at the peak of the spectral response ($D^*_{\lambda pk}$) was 10^{13} cm-$\sqrt{Hz}$/W. At 230K, the measured D^* was greater than $3x10^{14}$ cm-$\sqrt{Hz}$/W - a value very nearly background limited. At 230K, the uniformity was such that the standard deviation in D^* was 14% of the mean value and the yield was such that more than 98% of the pixels had a D^* greater than 50% of the mean value. FPAs were also fabricated using Reticon multiplexers but poor quality bump bonding prevented quantitative characterization.

The identification of the Rockwell variable bias multiplexer as a suitable match to the InGaAs PDAs and the resulting performance satisfied the objectives of the Phase I program.

The goals of Phase II will be to significantly advance the materials growth and processing technologies of lattice mismatched InGaAs so as to lower the dark current sufficiently that room temperature imaging in the 1.0-2.6 μm near infrared band can be performed. This goal has proven elusive despite investments of tens of millions of dollars over more than a decade.

Potential applications of this research include remote atmospheric sensing, LIDAR, satellite imaging, and near-infrared spectroscopy. The goals of the Phase II program are to extend these results to longer wavelengths using $In_{.82}Ga_{.18}As$ (sensitive to 2.6 μm) and to assemble a camera to control the FPAs. It is the intent of Sensors Unlimited to incorporate both the InGaAs FPAs and the camera into its product line.

2. Phase I Technical Objectives

The overall objective of this program is to develop a high performance room temperature camera based on the InGaAs material system for the 1-2.6 μm near-infrared wavelength range.

The purpose of the Phase I program was to construct a working 128x128 element multiplexed $In_{.53}Ga_{.47}As$ detector array (sensitive to 1.7 μm) to prove the concept of a room temperature near-infrared imaging device. Specific technical objectives were:

1. Procure 128x128 InGaAs detector arrays.

2. Procure Reticon silicon readout multiplexers.

3. Deposit indium for "bump bonds" between the detector array and the readout multiplexer.

4. Fabricate and test an integrated 128x128 multiplexer/array.

5. Design or specify an improved multiplexer for use with the extended wavelength detector arrays during Phase II.

6. Report results to contracting office via a final report.

3. Work Carried Out/Results Obtained

3.1 Fabricate 128x128 InGaAs detector arrays

The arrays were fabricated from vapor deposited epitaxial layers of $In.53Ga.47As$ which was lattice-matched to an n-type (sulfur-doped) InP substrate. A sketch of the structure is shown in Figure 1.

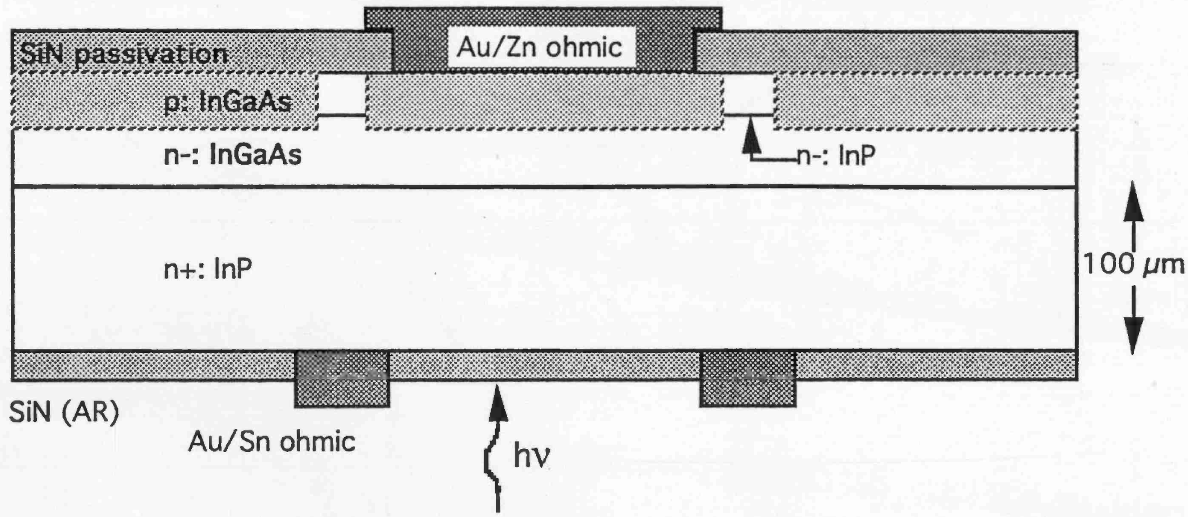

Figure 1. Photodetector structure used for the Phase I Program.

This wafer was then processed into an array of 40 x 40 μm pixels spaced 60 μm over the entire 2" diameter wafer by:

(1) The epitaxial side (front) of the wafer was coated with silicon nitride which serves both as an electronic passivant and as protection against the environment. The subsequent processing is "planar'" i.e. does not involve the etching away of epitaxial material.

(2) Using photolithographic techniques, 40 x 40 μm holes were opened in the silicon nitride.

(3) The p-n junction was formed by a Zn diffusion into the n-type epitaxial layer. The diffusion was carried out in a closed tube at 520°C using a Zn2As3 source.

(4) The front surface ohmic contacts to the p-type regions of the individual photodiodes consisted of a Au/Zn alloy sintered into the InGaAs.

(5) The substrate (back) was then lapped to a thickness of 100 μm.

(6) The backside ohmic contact to the n-type substrate consisted of an Au/Zn alloy deposited in a grid pattern. The substrate has a shorter wavelength cutoff than the active layer and is transparent to the 1-1.7 μm light. The photodiode array is backside illuminated through the substrate.

Figure 2 contains photographs of the front and back side of the wafer.

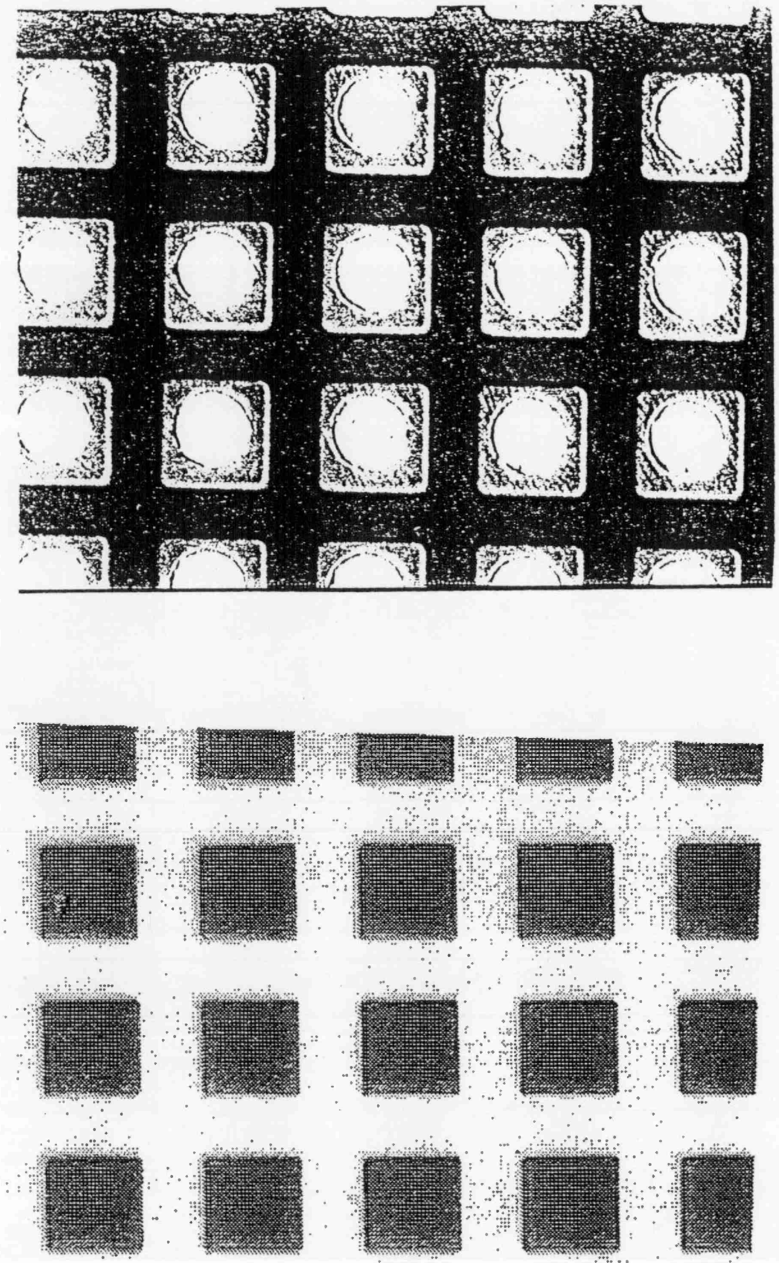

Figure 2. Front and back side of the InGaAs detector array.

3.2 <u>Procure Reticon silicon readout multiplexers</u>

The initial multiplexers used during Phase I were EG&G Reticon Model RA0128M. These devices are simply modifications of Reticon's 128x128 element silicon imaging array (RA0128N). In the imaging devices, the silicon photodiodes face the surface but are covered with a dielectric which serves both as a protectant and an anti-reflection coating. In the multiplexer, holes are opened in the dielectric and aluminum bonding pads are deposited.

The advantage of Reticon's multiplexer is that it allows custom photodiode arrays to be hybrid-integrated to a conventional silicon readout that is compatible with their family of camera support electronics. The major disadvantage is that it is designed for silicon photodiodes and is not well suited to higher dark current materials.

Figure 3 is a simplified schematic of the Reticon multiplexer when used as a silicon photodiode array:

An individual photodiode is connected to a charge storage capacitor through row and column select switches. The photodiode is "reset" by the application of a reverse bias from ϕ_X. The charge depleted from the photodiode charges the storage capacitor. The "fat zero" voltage allows the actual potential on the photodiode to be controlled to some extent. This is generally used to prevent traps in the material to be exposed which effects the linearity of the detector at low signal levels. In typical applications, the silicon photodiode is biased to $\approx$ -12V.

During the integration time, the photodiode is "de-selected" and allowed to float. The reverse potential decays through a combination of photocurrent and dark current which decreases the capacitance of the photodiode. In this sense, the signal is accumulated on the photodiode, itself.

The signal is "read" when the photodiode is next reset. The degree to which the storage capacitor is charged depends on the capacitance of the photodiode and, thus, to the signal level. When the photodiode is deselected, the signal charge on the storage capacitor is clocked out through a bucket brigade device.

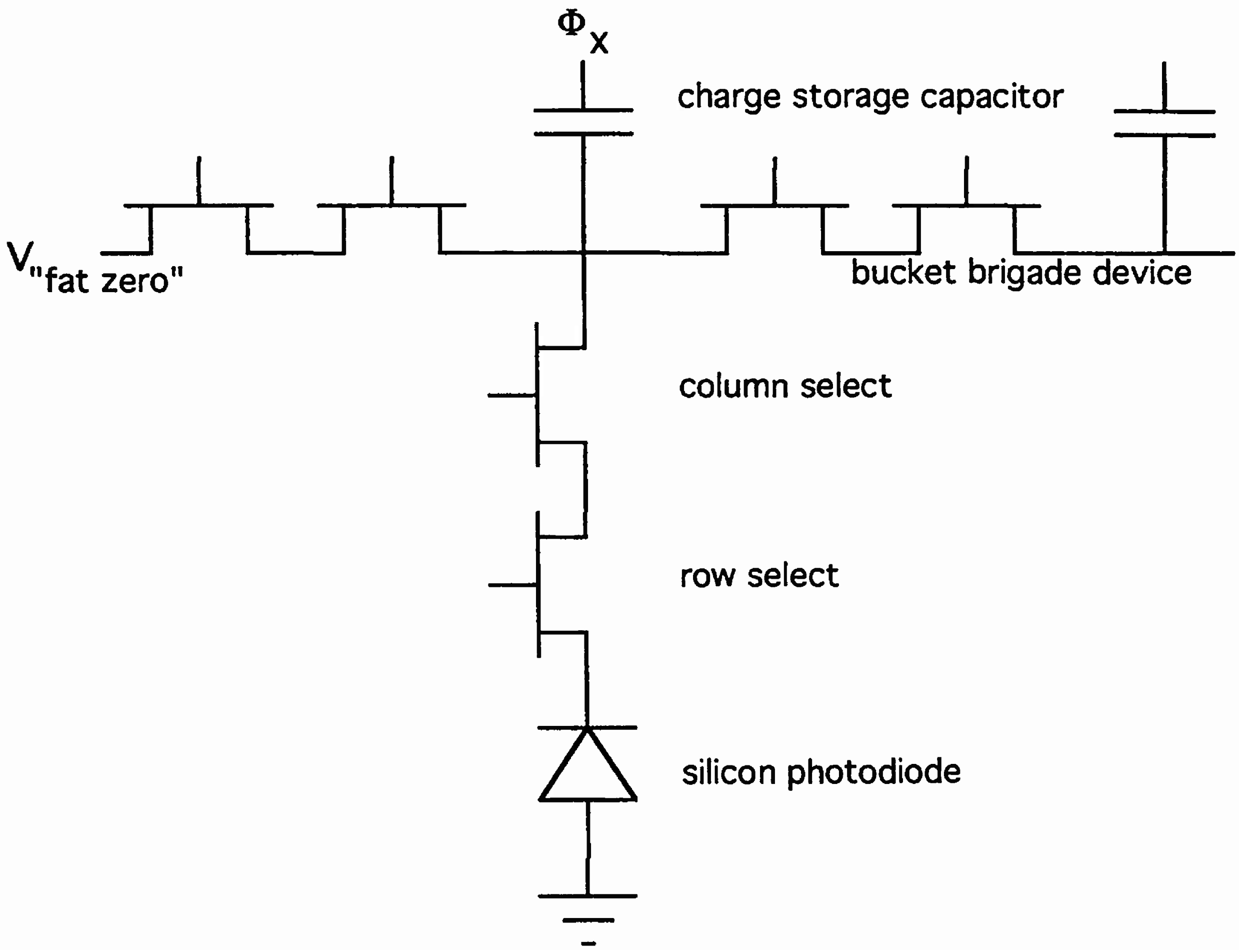

Figure 3. Simplified Schematic of Reticon RA0128N

Figure 4 is a schematic of the Reticon multiplexer after hybrid integration with an external photodiode array. The Reticon multiplexer is an NMOS device with n-on-p photodiodes. A positive voltage is used to reverse bias, i.e. reset, the photodiodes. InGaAs photodiodes are fabricated by a p-diffusion into an n-type substrate. The photodiode arrays used in this program are backside illuminated so the p-type front surface is mated to the readout multiplexer. In order to deplete the external photodiode array, a reverse bias must be applied to the n-type substrate, i.e. positive relative to the front surface. The only adjustable potential in the Reticon multiplexer is the fat zero voltage. This input has only a small adjustment range and, as a practical matter, the InGaAs photodiode arrays are biased to ≈ -3V.

As the dark current of a photodiode increases with reverse voltage, the goal is to allow the photodiode array to be operated as close to zero bias as possible while storing the integrated charge on an external capacitor. This is not possible with the Reticon multiplexer. As will be seen, the Reticon multiplexer allows the feasibility demonstration of room temperature imaging with 1.0-1.7 μm InGaAs, but does not allow for optimized performance. In addition, it will not be suitable for the Phase II effort which will be based on much higher dark current 1.0-2.6 μm InGaAs photodiode arrays.

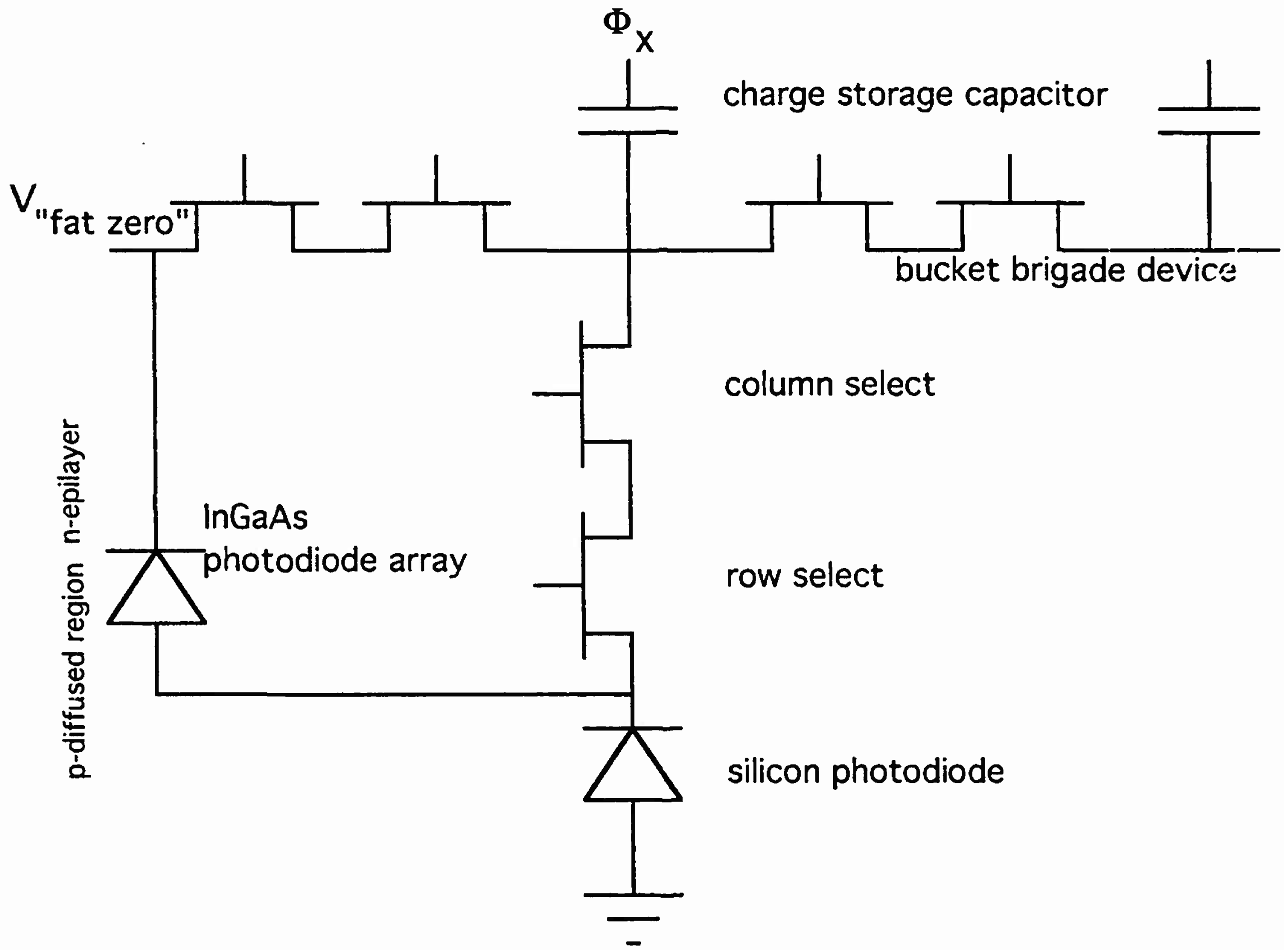

Figure 4. Schematic of InGaAs PDA bonded to Reticon Multiplexer

3.3 Specify and Procure Improved Multiplexer

It was the original intent to base the Phase I effort on the Reticon readout multiplexer. The design, specification, or identification of an improved multiplexer was to have taken place at the end of Phase I. During the course of the program, however, a Rockwell International multiplexer which has been used to evaluate mercury cadmium telluride photodiode arrays was identified. The Rockwell multiplexer has the advantage that it allows the external photodiode array to be held at a variable potential; as low as -10 mV. A schematic of the Rockwell multiplexer is shown in Figure 5 and its specifications summarized in Table 1.

In a conventional PDA/multiplexer assembly, the integrated photocurrent is stored in the capacitance of the photodiodes. The photodiode array is "reset" by the application of a reverse bias to the diodes and the sensor is allowed to "stare" by releasing the applied bias and allowing the reverse potential to decay. The charge storage capacity of the assembly depends on the reverse bias applied to the photodiodes. The accumulated charge consists of both photo-generated carriers and integrated dark current. The dark current depends both on the reverse bias and the operating temperature. In general, this scheme is not appropriate for high dark current materials.

In the Rockwell multiplexer, the signal charge is integrated in capacitance in the multiplexer which allows the photodiodes to be operated near zero bias. This allows the focal plane dark current to be minimized while maintaining the charge storage capacity of the integrated assembly.

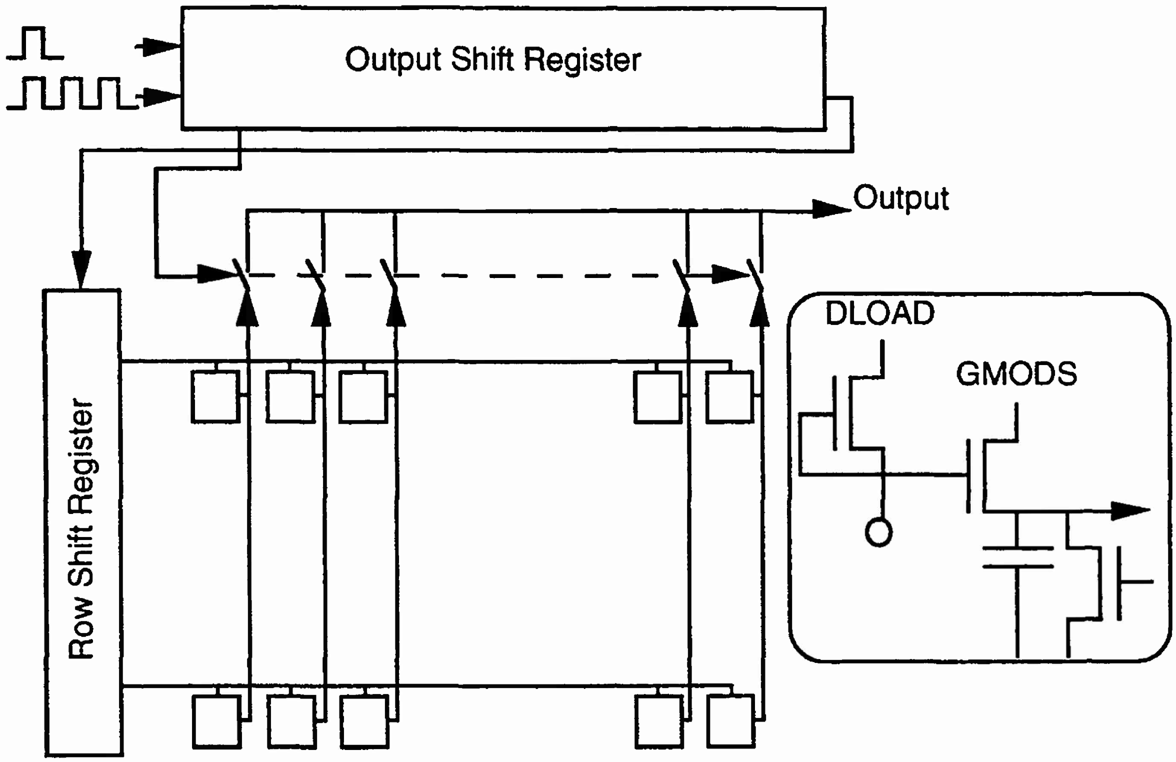

Figure 5. Rockwell CMOS Switched-FET MUX with Gate Modulation Input

Parameter	Min	Max	Units
Format	128x128		Pixels
Cell Pitch	60		μm
Input Circuit	Gate Modulation		
Supply Voltage	6	6	V
Charge-Handling Capacity	5.5	7.9	10^6 e^-
Minimum Read Noise	<50		e^-
Dynamic Range	>2	>10	10^3
Current Gain (A)	>10		10^3
Input Offset Non uniformity	<2		mV p-p
Transfer Ratio	25xA		nV/e^-

Table 1. Specifications of Rockwell Multiplexer

3.4 Bond Photodiode Array to Readout Multiplexer

The InGaAs photodiode arrays were connected to both Reticon and Rockwell multiplexers using indium "bump bonding" techniques. Bonding to the Reticon multiplexers was carried out at the Martin Marietta Central Research Laboratories in Baltimore and to the Rockwell multiplexers at Rockwell's Science Center in Thousand Oaks, CA.

Arrays of indium bumps were applied photolithographically to both the photodiode arrays and the multiplexers. The single mask used consisted of a two dimensional array of 20 μm diameter circles with a 60 μm center-to-center spacing. Both the photodiode arrays and the multiplexers were coated with photoresist then exposed with the circles aligned to the device pixels. Development left openings in the resist and the remaining resist was "lifted off" leaving arrays of circular bumps.

The actual bonding was performed using infrared aligners from Research Devices, Inc. of Piscataway, NJ. This instrument holds the photodiode arrays above the multiplexers and allows the operator to see through the InGaAs wafer with an infrared microscope. The photodiode arrays were aligned to the multiplexers and their indium bumps are carefully pressed together under controlled temperature and pressure. The procedure and the assembled device are illustrated in Figure 6. Figure 7 is a photograph of a packaged assembly with the Rockwell multiplexer.

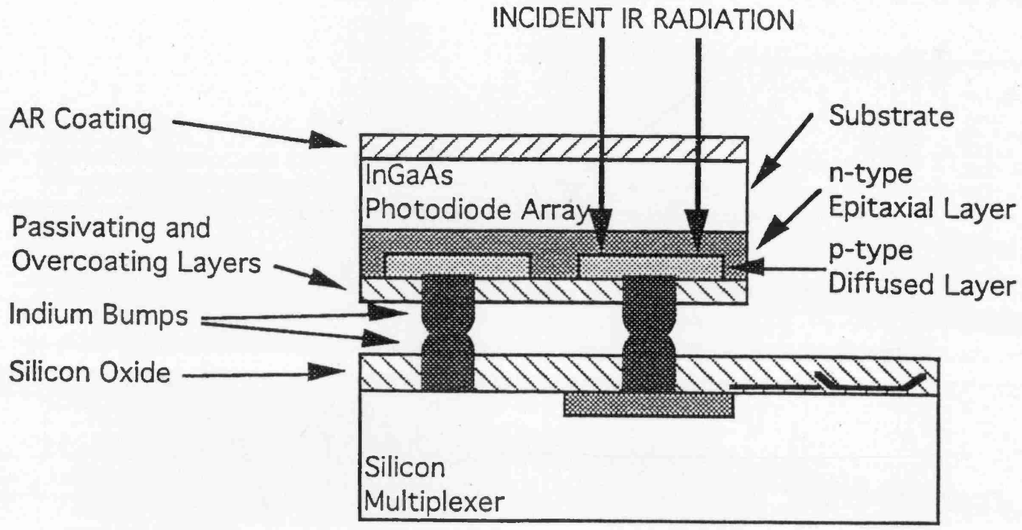

Figure 6. Schematic of InGaAs Photodiode Array Indium Bonded to Silicon Readout Multiplexer

128 x 128 InGaAs Focal Plane Array

- Sensors Unlimited InGaAs/
RI CMOS Gate Modulation Readout

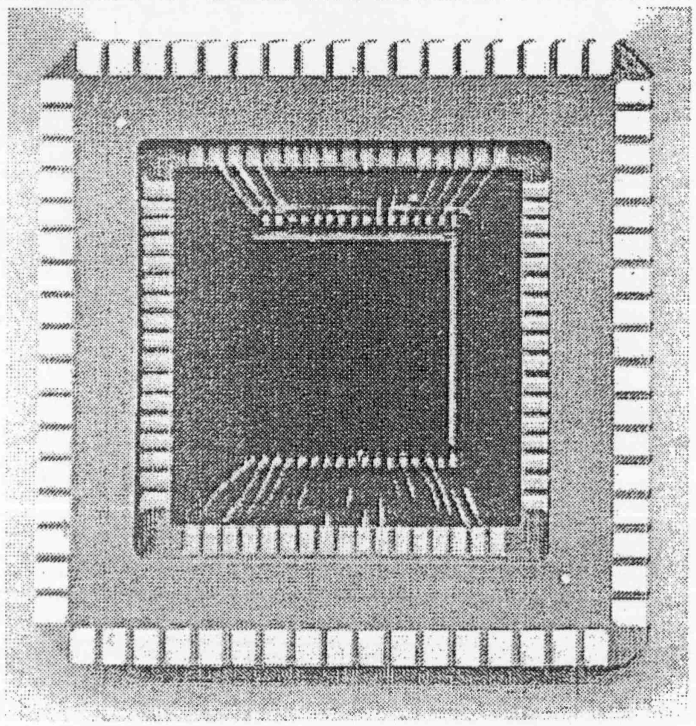

Figure 7. Photograph of InGaAs Hybrid Focal Plane Array Fabricated from InGaAs Photodiode Array and Rockwell Readout Multiplexer

3.5 Characterization of Integrated 128x128 Multiplexer/Array

The objective of Phase I of this Program was to mate a 128 x 128 element lattice-matched $In_{.53}Ga_{.47}As$ photodiode array with spectral sensitivity between 1.0 and 1.7 μm to a silicon multiplexer and to demonstrate the readout capability of the assembly.

The goals of Phase I were exceeded by the demonstration of imaging performance that far exceeded the current state-of-the-art.

Specifically, the following was demonstrated:

1) 128 x 128 element $In_{.53}Ga_{.47}As$ photodiode arrays were successfully mated to both Reticon RA0128M and Rockwell International CMOS Gate Modulation Readout multiplexers using indium bump-bonding techniques. The bonding was carried out with virtually no missing diodes due to poor bond quality.

2) Arrays mated to the Rockwell multiplexers were characterized at temperatures between 230 and 300K for spectral response, detectivity, and uniformity with performance that far exceeds the state of the art for HgCdTe and InSb photodiode arrays. This multiplexer has the further advantage of being able to apply a variety of biases to the photodiode array.

The sensor shown in Figure 7 was characterized for detectivity, D^*, spectral response, QE, and uniformity of D^* and QE. Figure 8 is a histogram summarizing the detectivity of the sensor at room temperature (300K) with the photodiode array biased to -1.3V. As can be seen, the average detectivity is 5×10^{12} cm-$\sqrt{Hz}$/W with a standard deviation 44% of the mean. The histogram indicates that more than 94% of the pixels exhibit D^* greater than 50 percent of the mean value. The true situation is, in fact, better than this as, due to problems with the multiplexers, 2 columns were not read but were included in the statistical analysis.

All the results discussed herein were obtained with the Rockwell multiplexer. As of November, 1992, a 128 x128 $In_{.53}Ga_{.47}As$ array had been "bump-bonded" to a Reticon multiplexer and is presently out at Reticon being installed in their camera. However, several difficulties have been encountered with their readout procedures, and to date, the Rockwell approach has been more successful. We will continue to pursue the Reticon approach since this offers the advantage of an existing camera and readout system.

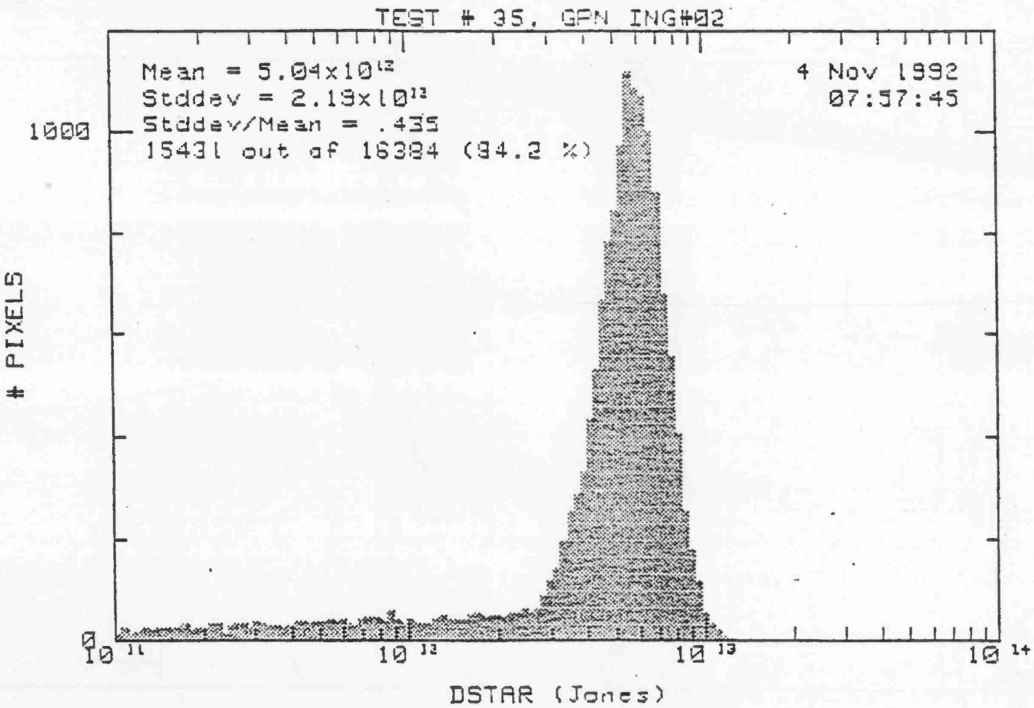

Figure 8. D* Distributions at T = 300K, V_R = -1.3V

Figure 9 is the D^* profile of the same device at room temperature but with the photodiode array operated near zero bias (ca. -10 mV). As can be seen, the profiles are very similar in terms of both uniformity and pixel yield but the average D^* is now in excess of 10^{13} cm-√Hz/W. The increase in detectivity results from a decrease in the dark current.

This performance establishes a new state-of-the-art. Comparisons with other material systems, (HgCdTe, InSb, PtSi), ***are not possible since InSb and PtSi must be cooled to liquid nitrogen temperature (77K) and the little room temperature data available on HgCdTe (see Table 3) shows it to be ten times worse than InGaAs.***

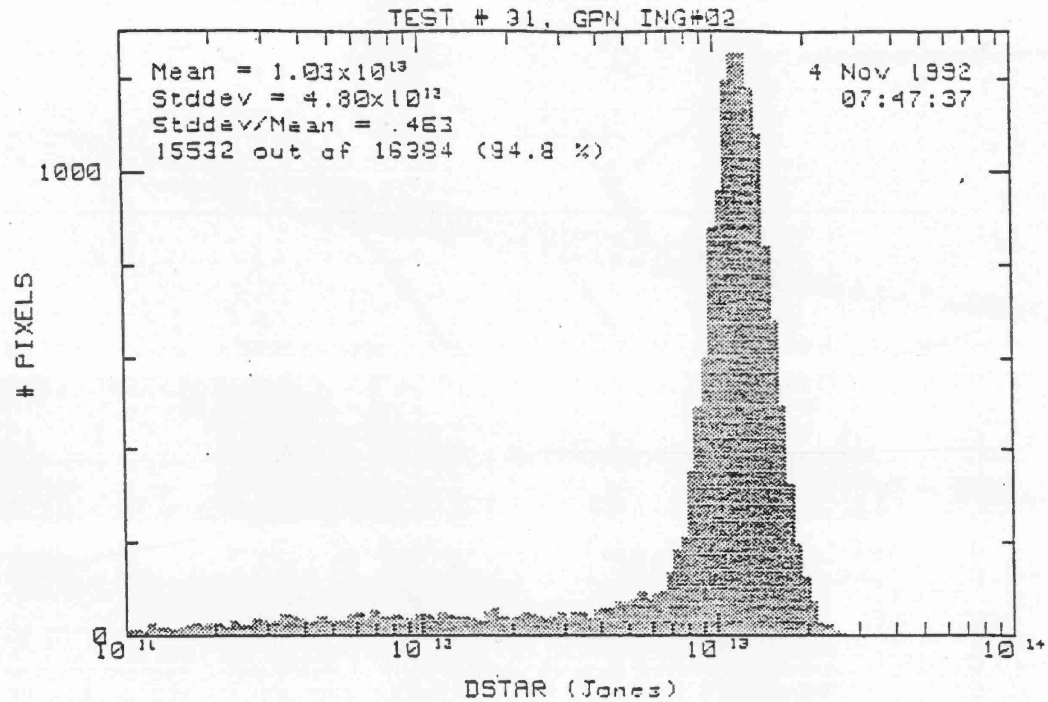

Figure 9. D* Distribution at T = 300K, V_R = -10mV

While the major goal of this Program is to develop a room temperature near-infrared camera, the sensor/multiplexer assembly was also characterized at reduced temperatures which are accessible via thermoelectric cooling. Figure 10 is the detectivity profile at 230K with the photodiode array operated near zero bias. The average D^* is 3.5×10^{14} cm-$\sqrt{Hz}$/W. ***This approaches the theoretical maximum of 4.5x10^{14} limited not by the detector but by the background scene (BLIP).***

Under these operating conditions, the distribution in D^* has tightened to 14% of the average value with 98.4 of the pixels having a D* greater than 50 percent of the mean value. The tail in the distribution towards lower D^* values that was evident in the room temperature data has largely disappeared indicating that it was likely due to non-uniformity in the dark current.

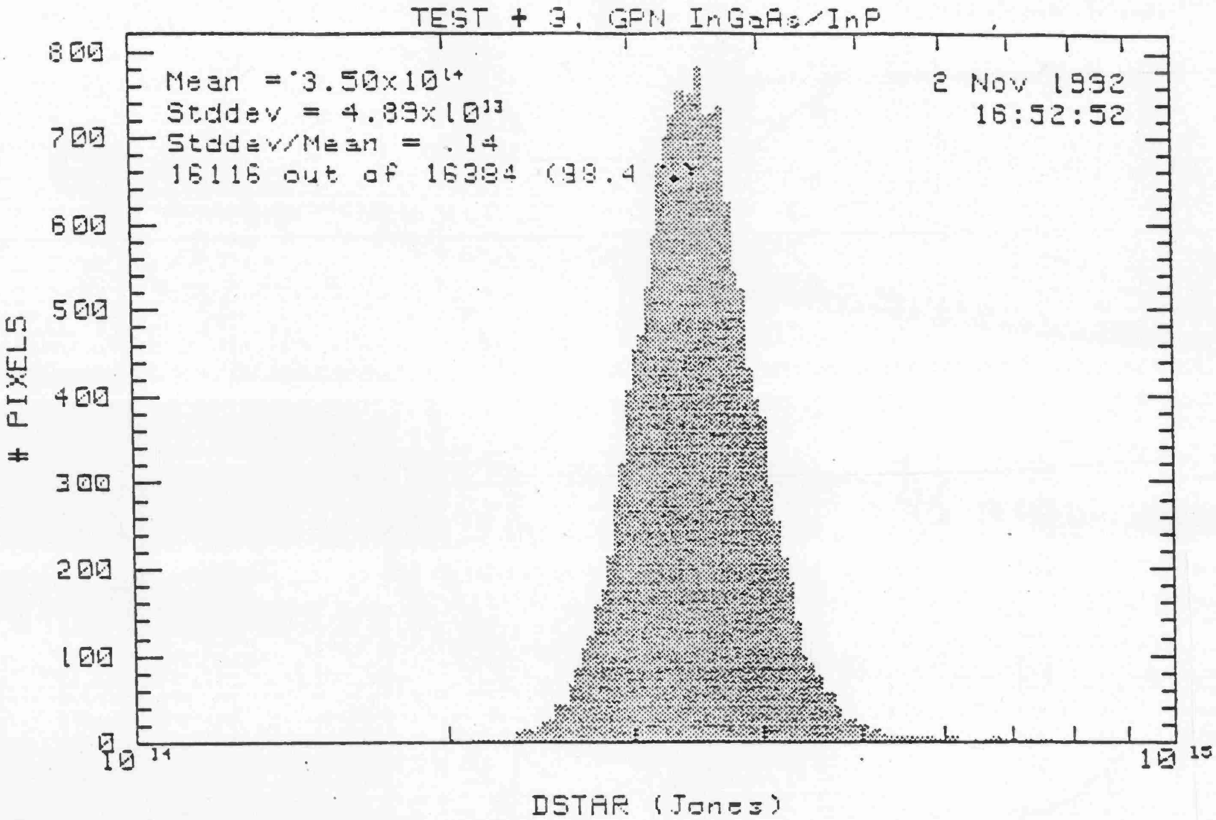

Figure 10. D* Distribution at T = 230K, V_R = -10mV

There are two key points in understanding these results. As mentioned above, somewhat more than 1% of the pixels were not read due to multiplexer problems so, in fact, more than 99% of the pixels fall within the distribution. Secondly, the device was first lowered to 200K then characterized at a variety of temperatures up to 300K. Upon warming, the photodiode array was damaged so that one corner of the device exhibited higher dark current (Figure 11). The tail of the D^* distribution comes from this "hot spot" and is not indicative of the true performance of the device.

The near BLIP detectivity of 3.5x10^{14} cm-√Hz/W at 230K improves the state-of-the-art for near-infrared two dimensional imagers by more than two orders of magnitude.

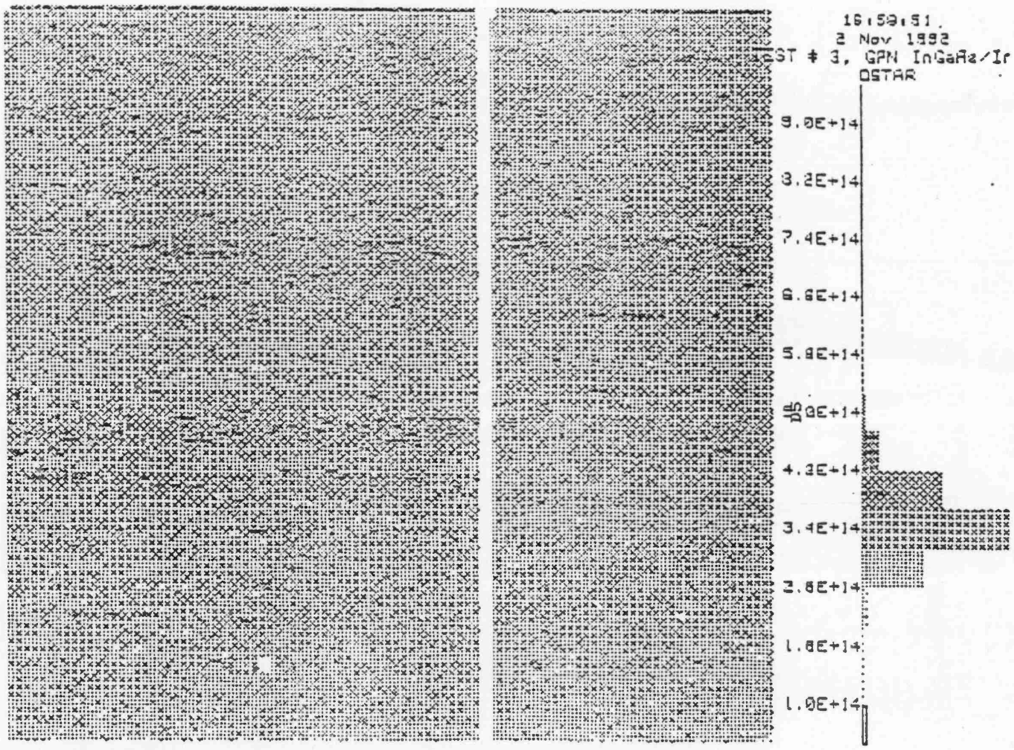

Figure 11a. D* across photodiode array at T = 230K

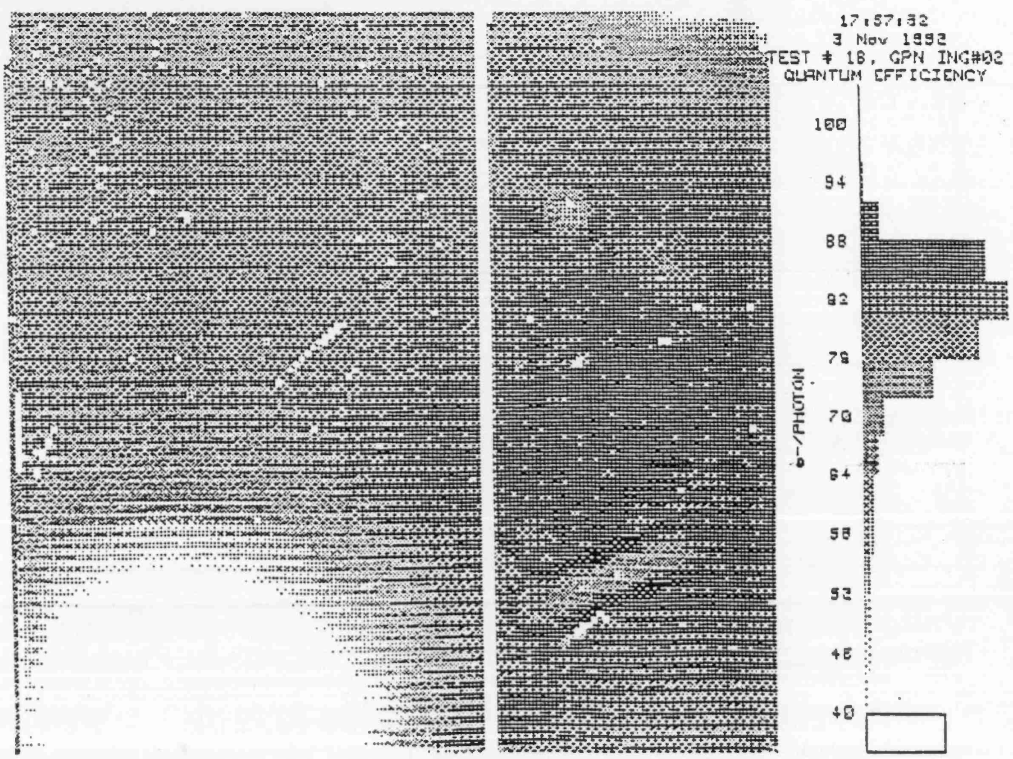

Figure 11b. D* across photodiode array at T = 300K after warming from 200K

Table 2 is a summary of the characterization of the Phase I $In_{.53}Ga_{.47}As$ photodiode array mated to the Rockwell silicon readout multiplexer. In all cases, the reported detectivity is the average of all 16,384 pixels without correcting for those not read out due to problems with the multiplexer. The same holds true for the uniformity and yield numbers. At room temperature, the data was not corrected for the high dark current in one corner of the photodiode array that resulted from mechanical stress. The uniformity and yield measured at the lowest temperature, therefore, is indicative of what can be expected from subsequent assemblies.

Temp. (K)	Bias (-V)	D^* cm-$\sqrt{Hz}$/W	Uniformity STD/MEAN (%)	Yield (%)
300	1.3	5.04×10^{12}	43.5	94.2
300	.01	1.03×10^{13}	45.3	94.8
263	.01	6.95×10^{13}	30.5	90.8
230	.01	3.50×10^{14}	14.0	98.4

Table 2. Performance of PDA/MUX Assembly

4. Conclusions and Discussion

The overall objective of this program is to develop InGaAs materials technology to where it can be used for room-temperature imaging in the 1.0-2.6 μm near infrared wavelength band. Performance at these wavelengths will require allow compositions of order $In_{.8}Ga_{.2}As$. The lattice of the active layers will be significantly mismatched to the InP substrate.

The limited objective of Phase I of the Program was to demonstrate the feasibility of the technology by integrating lattice matched $In_{.53}Ga_{.47}As$ with commercially available silicon readout electronics and characterizing the imaging performance at room temperature. Lattice matched InGaAs is sensitive to the 1.0-1.7 μm band.

Phase I was successful in two regards. The qualitative objectives were achieved in that the hybrid integration was successfully performed and room temperature imaging was observed.

> **More importantly, the performance of the hybrid focal plane array at room and thermoelectrically cooled temperatures far exceeded that achieved from any other material system despite investments of tens of millions of dollars over more than a decade.**

Table 3 contains a summary of the available data for both HgCdTe and InGaAs. It is extremely difficult to find data at exactly the same cutoff wavelengths and temperature with the same area device. RoA was determined (in cases where it was not given as such) by simply multiplying the two numbers.

	RoA(T) (Ω-cm^2)	
λco (μm)	HgCdTe	InGaAs
1.4	4 x10^4 (292K) 7 x10^6 (230K)	2.5 x10^5 (300K) 1.3 x10^8 (220K)
1.7	2 x10^2 (300K) 2 x10^5 (220K)	2.5 x10^5 (300K) 1.3 x10^8 (220K)
2.1	7 x10^1 (300K) 7 x10^3 (220K)	2.5 x10^3 (300K) 6.5 x10^5 (220K)
2.5	1 x10^1 (300K) 1 x10^3 (210K)	1.3 x10^2 (300K) 1.0 x10^5 (210K)

Table 3: Comparison of RoA Values in HgCdTe and InGaAs

For the InGaAs focal plane array developed during this program, at 230K, an average detectivity of $3.5\text{x}10^{14}$ cm-$\sqrt{}$Hz/W was measured with a uniformity such that more than 98% of the pixels exhibited detectivities greater than 50% of the mean value. This sensitivity is nearly that limited by background radiation (BLIP). At room temperature, detectivities in excess of 10^{13} were observed.

5. Phase II Activities

While the Phase I results are exciting and encouraging, they only serve to identify the challenges that will be confronted during Phase II. The performance of InGaAs is not a continuum with alloy composition. The lattice matched alloy has dramatically lower dark current (and, thus, higher detectivity) than the mismatched alloys.

The major technological objective of Phase II will be to dramatically lower the room temperature, zero bias dark current of $In_{.82}Ga_{.18}As$. This will require significant advances to both the materials and front end processing technologies. A secondary objective will be to identify and/or develop a silicon readout multiplexer which minimizes the effects of the dark current that remains.

REPORT OF INVENTIONS AND SUBCONTRACTS

(Pursuant to "Patent Rights" Contract Clause) (See Instructions on Reverse Side.)

Form Approved
OMB No 0704-0297
Expires Jun 30, 1992

1a. NAME OF CONTRACTOR / SUBCONTRACTOR	c. CONTRACT NUMBER	2a. NAME OF GOVERNMENT PRIME CONTRACTOR	c. CONTRACT NUMBER	3. TYPE OF REPORT (X one)
Sensors Unlimited, Inc.	DAAL03-92-C-0040		same	a. INTERIM / b. FINAL
b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYMMDD)	b. ADDRESS (Include ZIP Code)	d. AWARD DATE (YYMMDD)	4. REPORTING PERIOD (YYMMDD)
3490 U.S. Route 1 Princeton, NJ 08540	July 1, 1992			a. FROM b. TO

SECTION I – SUBJECT INVENTIONS

5. "SUBJECT INVENTIONS" REQUIRED TO BE REPORTED BY CONTRACTOR / SUBCONTRACTOR (If "None," so state)

a. NAME(S) OF INVENTOR(S) (Last, First, MI)	b. TITLE OF INVENTION(S)	c. DISCLOSURE NO., PATENT APPLICATION SERIAL NO. OR PATENT NO.	d. ELECTION TO FILE PATENT APPLICATIONS (1) United States (a) Yes	(1) United States (b) No	(2) Foreign (a) Yes	(2) Foreign (b) No	e. CONFIRMATORY INSTRUMENT OR ASSIGNMENT FORWARDED TO CONTRACTING OFFICER (1) Yes	(2) No
	(none)							

f. EMPLOYER OF INVENTOR(S) NOT EMPLOYED BY CONTRACTOR / SUBCONTRACTOR

(1)	(2)
(a) Name of Inventor (Last, First, MI)	(a) Name of Inventor (Last, First, MI)
(b) Name of Employer	(b) Name of Employer
(c) Address of Employer (Include ZIP Code)	(c) Address of Employer (Include ZIP Code)

g. ELECTED FOREIGN COUNTRIES IN WHICH A PATENT APPLICATION WILL BE FILED

(1) Title of Invention	(2) Foreign Countries of Patent Application
(none)	

SECTION II – SUBCONTRACTS (Containing a "Patent Rights" clause)

6. SUBCONTRACTS AWARDED BY CONTRACTOR / SUBCONTRACTOR (If "None," so state)

a. NAME OF SUBCONTRACTOR(S)	b. ADDRESS (Include ZIP Code)	c. SUBCONTRACT NO.(S)	d. DFAR "PATENT RIGHTS" (1) Clause Number	(2) Date (YYMM)	e. DESCRIPTION OF WORK TO BE PERFORMED UNDER SUBCONTRACT(S)	f. SUBCONTRACT DATES (YYMMDD) (1) Award	(2) Estimated Completion
					(none)		

SECTION III – CERTIFICATION

7. CERTIFICATION OF REPORT BY CONTRACTOR / SUBCONTRACTOR (Not required if [ ] Small Business or [ ] Non-Profit organization.) (X appropriate box)

a. NAME OF AUTHORIZED CONTRACTOR / SUBCONTRACTOR OFFICIAL (Last, First, MI)
Dr. Gregory H. Olsen

b. TITLE
President

c. **I certify that the reporting party has procedures for prompt identification and timely disclosure of "Subject Inventions," that such procedures have been followed and that all "Subject Inventions" have been reported.**

d. SIGNATURE
Gregory H Olsen

e. DATE SIGNED
1/20/93

DD Form 882, OCT 89 — *Previous editions are obsolete.* — 971/284