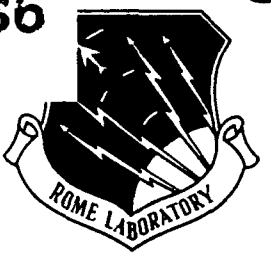
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RL-TR-93-2I, Part 2 (of two)
Final Technical Report
February 1993

STEP STRESS TESTING OF RECEIVER/TRANSMITTER UNITS

Hughes Aircraft Company

Steve Burnett, David Huch, Larry James, Stephen Mueller,
Peggy Tran

172370
93-02509



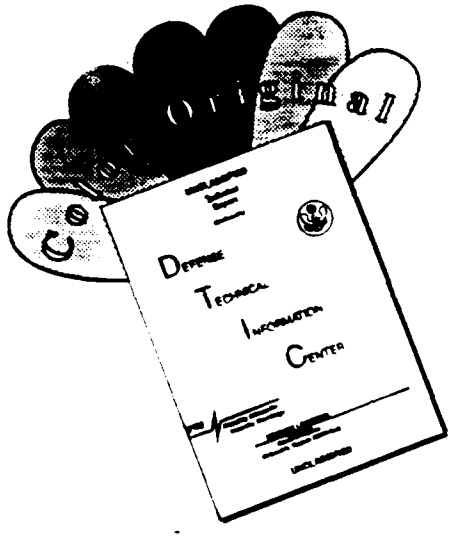
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APPROVED: T. Donovan

TIMOTHY J. DONOVAN
Project Engineer

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FOR THE COMMANDER: John J. Bart

JOHN J. BART
Chief Scientist, Reliability Sciences
Electromagnetics & Reliability Directorate

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Steve Burnett, David Huch, Larry James, Stephen Mueller, Peggy Tran

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Hughes Aircraft Company
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Fullerton CA 92634

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13. ABSTRACT (Maximum 200 words)

This report has been prepared to summarize a test validation effort for an accelerated life testing model which uses a wide parametric Bayesian Analysis Methodology. Step stress testing was performed on seven (7) Joint Tactical Information Distribution System (JTIDS) Class 1 synthesizer - detector, radio frequency assemblies. Failure data and analyses are provided. The report addresses issues concerning how to demonstrate high reliability (Mean-Time-Between-Failure values of 10,000 hours or more) on procured Air Force systems without incurring excessive testing costs.

14. SUBJECT TERMS
Accelerated Life Testing, Failure Rate (MTBF)
Step Stress Testing

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APPENDIX D

Test Data/Results

HUGHES AIRCRAFT COMPANY

INTERDEPARTMENTAL CORRESPONDENCE

TO: Dept ENB
ORG: 1A-72-XX

cc: Project Distribution

DATE: 16 March 1992
REF: 92/1A72.30/ 003

SUBJECT: **Step-Stress Test Data for UUTs**
Seven Production R/T Modules

FROM: S. D. Mueller
BLDG: 600 MAIL STA: B159
EXT: 1-8360 ORG.CODE: 1A-72-30

ABSTRACT: The Step-Stress testing of seven production (fielded) configuration Receiver/Transmitter modules was performed between the 22 January 1992 and the 13 March 1992 per contract F30602-89-D-100/009 in accordance with the approved R & D Test & Acceptance Plan (CDRL J003-001) submitted under Subcontract No. D000-07 to IIT Research Institute, Rome NY. The information contained in this ENB consists of the Step-Stress Test Data Sheets, data printouts, temperature plots, thermal log, and initial Trouble & Failure Report (if applicable) for each UUT MSN 1030, 1023, 1028, 0172, 0815, 1029, and 0993. Also provided for reference is the Thermal Test Equipment Operating Procedure. The contents herein shall be furnished to the customer upon request.

The contents of this ENB is as follows:

Step-Stress Test Data Notebook Unit Under Test: MSN 1030
(Tested: 22 & 23 January 1992) page 3

Step-Stress Test Data Notebook Unit Under Test: MSN 1023
(Tested: 06 & 07 February 1992) page 93

Step-Stress Test Data Notebook Unit Under Test: MSN 1028
(Tested: 03 & 04 March 1992) page 155

Step-Stress Test Data Notebook Unit Under Test: MSN 0172
(Tested: 04 & 05 March 1992) page 217

Step-Stress Test Data Notebook Unit Under Test: MSN 0815
(Tested: 05 & 06 March 1992) page 277

Step-Stress Test Data Notebook Unit Under Test: MSN 1029
(Tested: 10 March 1992) page 339

Step-Stress Test Data Notebook Unit Under Test: MSN 0995
(Tested: 12 & 13 March 1992) page 391

Thermal Test Equipment Operating Procedure
prepared by B. J. Armstrong page 453

The following individuals have contributions to this ENB and provided the technical support to conduct and perform the Step-Stress testing for the seven production R/T modules:

S. D. Mueller, L. N. Tsukamoto, B. J. Armstrong.

ENB Project Distribution: * Abstract only

R. A. Doctor* (Dept. Manager)
B. J. Armstrong* (Environmental Engineer)
S. R. Burnett* (Reliability Engineer)
D. Huch (Program Manager)
L. E. James (Project Manager)
S. D. Mueller (Design Engineer)
L. N. Tsukamoto* (Test Operations)

STEP-STRESS TEST DATA NOTEBOOK

UNIT UNDER TEST: MSN 1030

TEST STATUS: FAILURE CONFIRMED

(FOLLOWING LEVEL 11 STRESS)

TEST SUMMARY

STEP-STRESS		START DWELL	ANOMALY/ FAILURE	END DWELL
		22-Jan-92		
LEVEL	0	8:04		9:04
LEVEL	1	9:34		10:34
LEVEL	2	11:04		12:04
LEVEL	3	12:34		13:34
LEVEL	4	14:04		15:04
LEVEL	5	15:34	Anomaly	16:34
Retest	4	17:04		17:22
LEVEL	6	17:52		18:52
LEVEL	7	19:22	Anomaly	20:22
Retest	6	20:52		21:15
LEVEL	8	21:45	Anomaly	22:45
Retest	7	23:15	Anomaly	23:55
				22-Jan-92
		23-Jan-92		
Retest	6	0:25		1:10
LEVEL	9	1:40	Anomaly	2:40
Retest	8	3:10		4:20
LEVEL	10	4:50	Anomaly	5:50
Retest	9	6:20		7:30
LEVEL	11	8:00	Anomaly	9:00
FAILURE:			9:25	
Retest	10	9:30		9:47
Final Test	0	10:58		11:45
				23-Jan-92

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 0000): 1030 Test Date: 1/22/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0

UUT on @ 07:05 Cal Date: 1/20/92

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 07:08 (Start Freq #1) (HOUR MIN MIN) Start DWELL: 08 04 (Start Freq #2) (HOUR MIN MIN)

STEP-STRESS Level Chamber Air Temperature: 60.1 (°C) 27 60°C (Chamber thermocouple reading) Flange Temperature: 68.3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 170 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: 15 (Vdc) - 5 Volts dc: -5 (Vdc)

+15 Volts dc: +15 (Vdc) -15 Volts dc: -15 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 08 08 (HOUR MIN MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz. Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1247 (mA) - 5 Volts dc: 80 (mA)

+15 Volts dc: 116 (mA) -15 Volts dc: 502 (mA)

End TEST: 08 06 (HOUR MIN MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 0000): 1030 Test Date: 1/22/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 08:06 (HOUR MIN MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.88us/9.54us	50	4.77us/9.54us	50	
	I > Q	4.77us/9.54us	50	"	"	
	I + Q > 0	4.77us/9.54us	50	"	"	
	Q > 0	4.66us/9.54us	48	"	"	
Other Specify (dBm)	I > 0					
	I > Q					
50 (dBm)	I + Q > 0	4.77us/9.54us	50			
70 (dBm)	Q > 0	4.66us/9.54us	48			
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.88us/9.54us	50	4.77us/9.54us	50	
	I > Q	4.77/9.54us	50	"	"	
	I + Q > 0	4.42/9.54us	47	"	"	
	Q > 0	4.42/9.54us	47	"	"	

TEST Continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number: 1030 Test Date: 1/22/92

STEP-STRESS Level: 0

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rec Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rec Sig Level	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77 / 9.54	50	4.77 / 9.54	50	
	I > Q	"	50	"	"	
	I + Q > 0	"	50	"	"	
	Q > 0	4.611 / 9.54	48	"	"	
Other Specify	I > 0					
	I > Q					
50 (dBm) -? 65	I + Q > 0	4.77 / 9.54	50			
	Q > 0	4.611 / 9.54	48			
Other Specify	I > 0					
	I > Q					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.77 / 9.54	50	4.77 / 9.54	50	
	I > Q	"	"	4.77 / 9.54	"	
	I + Q > 0	4.293 / 9.54	45	4.77 / 9.54	"	
	Q > 0	4.451 / 9.54	47	4.77 / 9.54	"	

End TEST: 08 30 (HOUR MIN SEC)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number: 1030 Test Date: 1/22/92

STEP-STRESS Level: 0

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 08 50 (HOUR MIN SEC)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *comment for cable losses
50 (ch)	684	11.69	684	11.89	Pwr measured with Spec Anal on max hold for 15 sec then Mkr Search
35 (ch)	729	11.24	729	9.84	
18 (ch)	825	11.16	825	10.46	
00 (ch)	921	9.93	921	9.53	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 08 50 (HOUR MIN SEC)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 09 04 (HOUR MIN SEC)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 1/22/92

STEP-STRESS Level: 0 Tester:

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

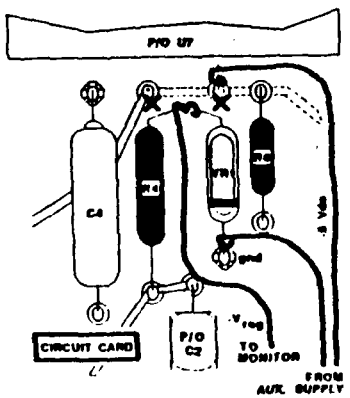
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

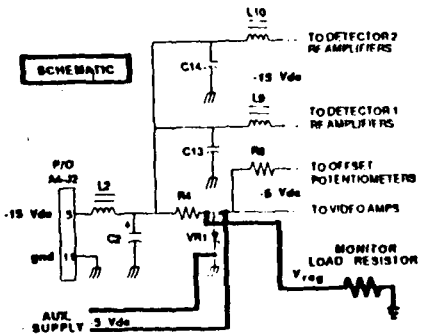
Start TEST: 08.50 (must be within)

Voltage across LOAD RESISTOR: -5.1 (Vdc) (Appendix D; nominally 5 Vdc)

End TEST: 08:51 (must be within)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 7.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

Syn #1030
Stress Level 0
1/22/92
J5 output

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 6.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than 693.0 MHz which is below the specified frequency.
Power at J12 is 6.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is less than 699.0 MHz which is be ow the specified frequency.
Power at J12 is 6.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is .1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is .1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

syn # 1030
stress level 0
1/22/92
J12 output

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (xxxx-1030): 1030 Test Date: 1/22/92

Tester: (Please & stamp below) ESG P1409

STEP-STRESS Level (xxxx 0 - 10): 1

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 09:04 (Hour Min Sec) Start DWELL: 09:34 (Hour Min Sec)

STEP-STRESS Level Chamber Air Temperature: 68.5 (°C) (Chamber thermocouple reading) Set 069

Plunge Temperature: 76.3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 78 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 5.2 (Vdc) -5 Volts dc: -5.2 (Vdc)

+15 Volts dc: +15.3 (Vdc) -15 Volts dc: -15.3 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.1 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 09:48 (Hour Min Sec)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1289 (mA) -5 Volts dc: 85 (mA)

+15 Volts dc: 117 (mA) -15 Volts dc: 510 (mA)

End TEST: 09:49 (Hour Min Sec)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (xxxx-1030): 1030 Test Date: 1/22/92

STEP-STRESS Level (xxxx 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 09:49 (Hour Min Sec)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Data	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	477/954	50	477/954	50	t
	I > 0	"	"	"		
	I + Q > 0	"	"	"		
	Q > 0	461/954	48	"		
Other Specify	I > 0					
	I > 0					
50 (dBm)	I + Q > 0	477/954	50			
	Q > 0	461/954	48			
Other Specify	I > 0					
	I > 0					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	477/954	50	477/954	50	
	I > 0	"	"	"	"	
	I + Q > 0	454/954	45	"	"	
	Q > 0	449/954	47	"	"	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 1/22/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.7us/9.54us	50	4.7us/9.54us	50	↕
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.61us/9.54us	48	4.61us/9.54us	48	
To Other Specify (dBm) 59	I > 0	4.7us/9.54us	50			I > 0 at -10.6 (bit 1)
	I > Q					
	I + Q > 0	4.7us/9.54us	50			
	Q > 0	4.61us/9.54us	48			
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0			4.7us/9.54us	50	I > 0 only @ falling edge
	I > Q	4.7us/9.54us	50	"	"	
	I + Q > 0	4.7us/9.54us	48	"	"	↕ 0 to -75 (bit 1)
	Q > 0	4.52us/9.54us	47	4.61us/9.54us	48	

End TEST 10:00 (HOUR HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 1/22/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 10:00 (HOUR HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *Increase for cable losses
50 min	684	11.69	684	11.69	
35 min	729	11.34	729	9.5	
18 min	825	10.96	825	9.96	
00 min	921	9.9	921	10.4	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 10:15 (HOUR HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 10:54 (HOUR HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number (enter SCPT): 1030

Test Date: 1/22/92

Tester: (Name & comp below)

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORED

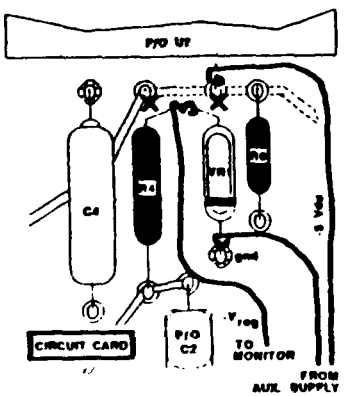
RESISTOR/ZENER DIODE MODIFICATION: At Dock: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

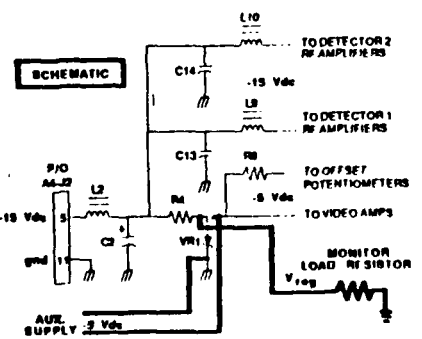
Start TEST: 10.15 (Hour Min AM/PM)

Voltage across LOAD RESISTOR: -5.1 (Vdc) (refer to Appendix D: nominally -5 Vdc)

End TEST: 10:16 (Hour Min AM/PM)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is-.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 2.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is .6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is .0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

Syn #1030 stress level 1 (SAG @ 3409 TEST) 1/22/92 J5 output

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 11.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is .6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is .0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 921.0 MHz (Spec=+9dBm minimum).

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 1.1 dBm @ 687.0 MHz (Spec=+9dBm minimum). Syn # 1030
Power at J12 is-.2 dBm @ 690.0 MHz (Spec=+9dBm minimum). stress level 1
Frequency is greater than 690.0 MHz which is above the specified frequency. 1/22/92
Power at J12 is 5.1 dBm @ 693.0 MHz (Spec=+9dBm minimum). (SYN 1030 TEST)
Frequency is greater than 693.0 MHz which is above the specified frequency.
Power at J12 is 4.5 dBm @ 696.0 MHz (Spec=+9dBm minimum). J12 Output
Power at J12 is 7.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 705.0 MHz which is above the specified frequency.
Power at J12 is 3.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 774.0 MHz which is above the specified frequency.
Power at J12 is 6.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (xxxx-xxxx): 1030 Test Date: 1/22/92

Tester: (Name & stamp below)

STEP-STRESS Level (zero - six): 2

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 10 34 (hhmm ink only) Start DWELL 11 04 (hhmm ink only)

STEP-STRESS Level Chamber Air Temperature: 76.3 Set to 77 (°C) Flange Temperature: 84.7 (°C)
(Chamber thermocouple reading) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 86 (°C)
(refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +5.4 (Vdc) -5 Volts dc: -5.4 (Vdc)

+15 Volts dc: +15.6 (Vdc) -15 Volts dc: -15.6 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 11 04 (hhmm ink only)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1349 (mA) -5 Volts dc: 81 (mA)

+15 Volts dc: 119 (mA) -15 Volts dc: 513 (mA)

End TEST: 11 05 (hhmm ink only)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (xxxx-xxxx): 1030 Test Date: 1/22/92

STEP-STRESS Level (zero - six): 2

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 11:05 (hhmm ink only)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	477ns / 954ns	50	477ns / 954ns	50	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	411ns / 954ns	48	"	"	
Other Specify	I > 0	477ns / 954ns	50			Invert Q (old test)
	I > Q					
50 (dBm)	I + Q > 0	477ns / 954ns	50			
65	Q > 0	462ns / 954ns	48			
Other Specify	I > 0					
	I > Q					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0			477ns / 954ns	50	I > 0 hung on fall edge
	I > Q	477ns / 954ns	50	"	"	
	I + Q > 0	477ns / 954ns	48	"	"	
	Q > 0	462ns / 954ns	99	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number (enter MSN): 1030 Test Date: 1/22/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig (enter)	I & Q (-Bits)	Detector 1 Lower T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Upper T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.7µs/9.4µs	50	4.7µs/9.4µs	50	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	461ns/9.4µs	48	461ns/9.4µs	48	
-10	I > 0	461ns/9.4µs	48			I70 at 12 - 20dB (RF) no noise (duty cycle changes to 48% & 52% @ -25.1)
Other: Specify	I > Q					
50 (dBm)	I + Q > 0	4.7µs/9.4µs	50			
-65	Q > 0	461ns/9.4µs	48			
Other: Specify	I > 0					
	I > Q					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0			4.7µs/9.4µs	50	I70 noisy (Det 1)
	I > Q	4.7µs/9.4µs	50	"	"	
	I + Q > 0	4.7µs/9.4µs	45	"	"	
	Q > 0	461ns/9.4µs	"	461ns/9.4µs	48	

End TEST: 11:32 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number (enter MSN): 1030 Test Date: 1/22/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST. At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 11:32 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *amount for cable losses
50 min	684	11.39	684	11.59	
35 min	729	11.0	729	11.3	
18 min	775	10.8	775	10.7	
00 min	921	9.4	921	9.93	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 11:50 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 12:04 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 1/22/92

Tester:

STEP-STRESS Level: 2

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: As Dwell; For the modified resistor/zener diode referenced, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

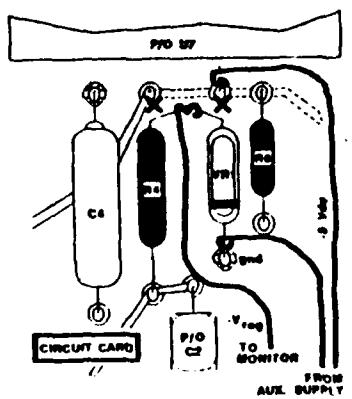
Start TEST: 11:50

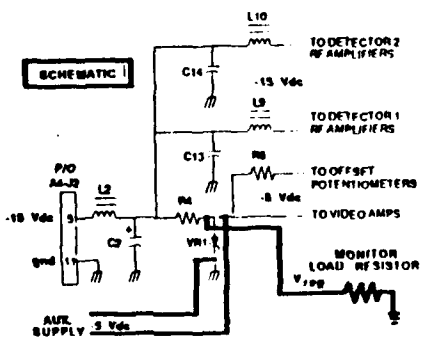
Voltage across LOAD RESISTOR: -5.13 (Vdc)

End TEST: 11:51

17

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 5.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 6.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is .8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 6.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

1/22/92

Sun Det # 1030
stress test 2
J5 output

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is .8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is-5.2 dBm @ 687.0 MHz (Spec=+9dBm minimum). 1/22/92

Frequency is less than 687.0 MHz which is below the specified frequency.

Power at J12 is 1.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 690.0 MHz which is above the specified frequency.

Power at J12 is 5.2 dBm @ 693.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 693.0 MHz which is above the specified frequency.

Power at J12 is 8.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).

Power at J12 is-3.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.8 dBm @ 732.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).

Power at J12 is-2.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.0 dBm @ 765.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).

Power at J12 is-3.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.6 dBm @ 825.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 918.0 MHz which is above the specified frequency.

Power at J12 is 7.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

Syn Bof #1030
Sheet level 2 -
J12 output

19

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. 8

Power at J12 is 10.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).

Power at J12 is-5.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.2 dBm @ 693.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).

Power at J12 is-3.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).

Power at J12 is 9.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).

Power at J12 is 10.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.8 dBm @ 732.0 MHz (Spec=+9dBm minimum).

Power at J12 is 9.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).

Power at J12 is 9.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).

Power at J12 is 9.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).

Power at J12 is-2.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.0 dBm @ 765.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).

Power at J12 is 9.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).

Power at J12 is-3.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.6 dBm @ 825.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 1/22/92

Tester: CSC R1409

STEP-STRESS Level: 3

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 12:04 (hhmm hr min) Start DWELL: 1234 (hhmm hr min)

STEP-STRESS Level Chamber Air Temperature: 84.2 (°C) Flange Temperature: 92.8 (°C)

STEP-STRESS Level Component Temperature: 94 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level.

Supply Voltages: +5 Volts dc: +5.6 (Vdc) -5 Volts dc: -5.6 (Vdc)

+15 Volts dc: +15.9 (Vdc) -15 Volts dc: -15.9 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 1240 (hhmm hr min)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1388 (mA) -5 Volts dc: 92 (mA)

+15 Volts dc: 121 (mA) -15 Volts dc: 529 (mA)

End TEST: 1241 (hhmm hr min)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 1/22/92

STEP-STRESS Level: 3

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 1241 (hhmm hr min)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Data	Detector 1 t (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77us/954us	50	4.77us/954us	50	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.61us/954us	48	"	"	
-70	I > 0	4.77us/954us	50			I 70 OK @ 70.6
Other Specify	I > Q					
50 (dBm)	I + Q > 0	4.77us/954us	50			
65	Q > 0	4.61us/954us	48			
Other Specify	I > 0					
	I > Q					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0			4.77us/954us	50	7.70 marginal - FAIL. [7] (1)
	I > Q	4.77us/954us	50	"	"	
	I + Q > 0	4.29? [illegible]	45	"	"	
	Q > 0	4.52us/954us	47	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 1/22/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 484 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.7µs/9.54µs	50	4.7µs/9.54µs	50	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.61µs/9.54µs	48	4.61µs/9.54µs	48	
70 Other: Specify	I > 0	4.61µs/9.54µs	44			I > Q at P - Rib on mid (Duty change to 44) Q - 48 Cl 2 coils
	I > Q					
40 (dBm) -65	I + Q > 0	4.7µs/9.54µs	50			
	Q > 0	4.61µs/9.54µs	48			
Other: Specify	I > 0					
	I > Q					
10 (dBm)	I + Q > 0			4.7µs/9.54µs	50	
	Q > 0					
-75 dBm	I > 0			4.7µs/9.54µs	50	I > Q noisy (~ 35.4µs/19.1)
	I > Q	4.7µs/9.54µs	50	"	"	
	I + Q > 0	4.28µs/9.54µs	45	4.61µs/9.54µs	48	
	Q > 0	4.28µs/9.54µs	45	4.61µs/9.54µs	48	

End TEST: 13:10 (HHMM 24h time)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 1/22/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 13:10 (HHMM 24h time)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measured for cable losses
50 (min)	684	11.29	684	11.49	
35 (mid)	729	10.6	729	9.8	
18 (mid)	825	10.4	825	9.8	
00 (max)	921	9.0	921	9.4	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check box)

End TEST: 13:30 (HHMM 24h time)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level

End DWELL: 13:34 (HHMM 24h time)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number (from VSWR): 1030

Test Date: 1/22/92

Tester: (Please print clearly)

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

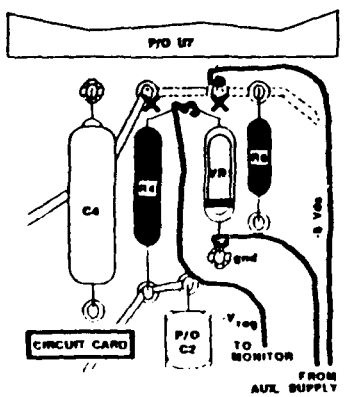
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

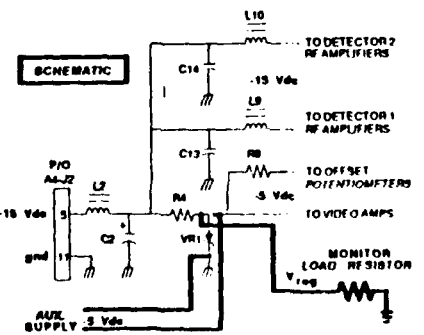
Start TEST: 13:30 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.15 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 13:31 (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





1/22/92 (SYS TEST)

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

syn Det # 1030
Stress level 3
J5 output

****

Power at J5 is 2.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 4.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 7.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is-8.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is-8.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

1/22/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 5.6 dBm @ 687.0 MHz (Spec=+9dBm minimum). Syn Det H 1030
Power at J12 is-2.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 3.4 dBm @ 693.0 MHz (Spec=+9dBm minimum). Stress test — 3
Frequency is greater than 693.0 MHz which is above the specified frequency.
Power at J12 is 5.9 dBm @ 696.0 MHz (Spec=+9dBm minimum). J12 output
Power at J12 is 6.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 699.0 MHz which is above the specified frequency.
Power at J12 is 5.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is less than 708.0 MHz which is below the specified frequency.
Power at J12 is 6.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than 711.0 MHz which is below the specified frequency.
Power at J12 is 1.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 717.0 MHz which is above the specified frequency.
Power at J12 is 5.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 723.0 MHz which is above the specified frequency.
Power at J12 is 3.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Frequency is less than 735.0 MHz which is below the specified frequency.
Power at J12 is 4.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Frequency is less than 738.0 MHz which is below the specified frequency.
Power at J12 is 3.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Frequency is less than 744.0 MHz which is below the specified frequency.
Power at J12 is 5.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Frequency is less than 747.0 MHz which is below the specified frequency.
Power at J12 is 6.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 774.0 MHz which is above the specified frequency.
Power at J12 is 6.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 828.0 MHz which is above the specified frequency.
Power at J12 is 4.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 888.0 MHz which is above the specified frequency.
Power at J12 is 7.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 891.0 MHz which is above the specified frequency.
Power at J12 is 3.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-8.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 909.0 MHz which is above the specified frequency.
Power at J12 is 6.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 918.0 MHz which is above the specified frequency.
Power at J12 is 5.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. 0

Power at J12 is 9.6 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-8.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 1/22/92

STEP-STRESS Level: 4 Tester:

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 13 34 (THUP HR MIN) Start DWELL: 14:04 (THUP HR MIN)

STEP-STRESS Level Chamber Air Temperature: 92.9 (°C) Flange Temperature: 101.9 (°C)
(Chamber thermocouple reading) 5 ft @ 94 (Thermocouple reading)

STEP-STRESS Level Component Temperature: 102 (°C)
(refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 15.8 (Vdc) -5 Volts dc: -5.8 (Vdc)

+15 Volts dc: +16.2 (Vdc) -15 Volts dc: -16.2 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 14 04 (THUP HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1407 (mA) -5 Volts dc: 94 (mA)

+15 Volts dc: 124 (mA) -15 Volts dc: 545 (mA)

End TEST: 14 05 (THUP HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 1/22/92

STEP-STRESS Level: 4

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 14:05 (THUP HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77µs / 9.54µs	50	4.77µs / 9.54µs	50	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.61µs / 9.54µs	48	"	"	
70 Other: Specify	I > 0	4.77µs / 9.54µs	50			I 70 CC @ -70dB (Ref.)
	I > Q					
40 (dBm)	I + Q > 0	4.77µs / 9.54µs	50			
65	Q > 0	4.61µs / 9.54µs	48			
Other: Specify	I > 0					
	I > Q					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0			4.770 / 9.54µs	50	I 70 meas @ -75dB (Ref.)
	I > Q	4.77µs / 9.54µs	50	"	"	
	I + Q > 0	4.39µs / 9.54µs	45	"	"	
	Q > 0	4.39µs / 9.54µs	45	"	"	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 1/22/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q -Bits	Detector 1 Limits T (spec)	Detector 1 Duty Cycle (percent)	Detector 2 Limits T (spec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.7ms/95ms	50	4.7ms/95ms	50	
	I > 0	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.6ms/95ms	48	4.6ms/95ms	48	
70	I > 0	4.6ms/95ms	48			I>0 still no noise (Rcv sig is 48) @ 70dB
Other Specify	I > 0					
46 (dBm)	I + Q > 0	4.7ms/95ms	50			
65	Q > 0	4.6ms/95ms	48			
Other Specify	I > 0					
	I > 0					
70 (dBm)	I + Q > 0			4.7ms/95ms	50	
	Q > 0					
-75 dBm	I > 0			4.7ms/95ms	50	I>0 noisy @ -75 (Ref 1)
	I > 0	4.7ms/95ms	50	"	"	
	I + Q > 0	4.7ms/95ms	45	4.6ms/95ms	48	
	Q > 0	4.29ms/95ms	45	4.6ms/95ms	48	

End TEST: 14 25 (military time)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 1/22/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 14 25 (military time)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	684	10.9	684	11.2	X Below spec in >616
35 min	739	11.1	739	9.8	
18 min	825	9.5	825	9.2	
00 min	921	8.4	921	9.3	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 14 40 (military time)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 15 04 (military time)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 1/22/92

STEP-STRESS Level: 4 Tester:

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

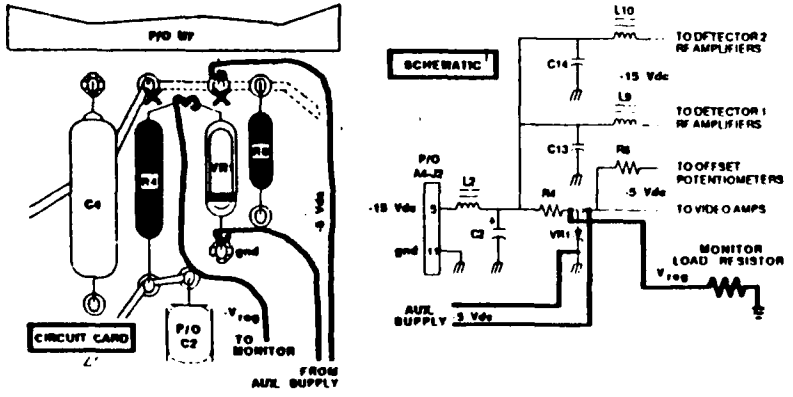
Start TEST: 14:40

Voltage across LOAD RESISTOR: -5.16 (Vdc)

End TEST: 14:41

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION FOR AUX. CONSTANT -5 Vdc SUPPLY AND R4/VR1 MONITORING



1/22/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 3.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 8.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 8.2 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 5.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 5.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 4.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

Syn Det #1030 stress test 4 J5 output

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.6 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

1/22/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

stress test of J12 output

****

Power at J12 is 8.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is less than 687.0 MHz which is below the specified frequency.
Power at J12 is-3.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than 693.0 MHz which is below the specified frequency.
Power at J12 is 3.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 696.0 MHz which is above the specified frequency.
Power at J12 is .6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 714.0 MHz which is above the specified frequency.
Power at J12 is .1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is less than 723.0 MHz which is below the specified frequency.
Power at J12 is 8.0 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 726.0 MHz which is above the specified frequency.
Power at J12 is-1.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Frequency is less than 729.0 MHz which is below the specified frequency.
Power at J12 is 2.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 732.0 MHz which is above the specified frequency.
Power at J12 is 4.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Frequency is less than 747.0 MHz which is below the specified frequency.
Power at J12 is 2.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 750.0 MHz which is above the specified frequency.
Power at J12 is 5.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 753.0 MHz which is above the specified frequency.
Power at J12 is 4.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 756.0 MHz which is above the specified frequency.
Power at J12 is 2.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Frequency is less than 759.0 MHz which is below the specified frequency.
Power at J12 is 3.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is less than 768.0 MHz which is below the specified frequency.
Power at J12 is 2.4 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 771.0 MHz which is above the specified frequency.
Power at J12 is .0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Frequency is less than 774.0 MHz which is below the specified frequency.
Power at J12 is 4.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 777.0 MHz which is above the specified frequency.
Power at J12 is .9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 831.0 MHz which is above the specified frequency.
Power at J12 is 1.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is less than 837.0 MHz which is below the specified frequency.
Power at J12 is 1.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 888.0 MHz which is above the specified frequency.
Power at J12 is 4.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is less than 891.0 MHz which is below the specified frequency.
Power at J12 is 3.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 897.0 MHz which is above the specified frequency.
Power at J12 is-3.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is less than 912.0 MHz which is below the specified frequency.
Power at J12 is 2.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 915.0 MHz which is above the specified frequency.
Power at J12 is 2.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 918.0 MHz which is above the specified frequency.
Power at J12 is 5.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 8.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is .1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.4 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is .0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.3 dBm @ 910.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

UUT Serial Number (enter 4 digits): 1030 Test Date: 1/22/92

Tester: (Name & many helpers)

STEP-STRESS Level (enter 0 - 10): 5

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 15:04 (THUR HR MIN) Start DWELL: 15:34 (THUR HR MIN)

STEP-STRESS Level Chamber Air Temperature: +100.6 (°C) Set @ +102 °C

Flange Temperature: +110.0 (°C)

STEP-STRESS Level Component Temperature: +110 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level.

Supply Voltages: +5 Volts dc: +6.00 (Vdc) -5 Volts dc: -6.00 (Vdc)

+15 Volts dc: +16.50 (Vdc) -15 Volts dc: -16.50 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 15:36 (THUR HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 146.8 (mA) -5 Volts dc: 93.3 (mA)

+15 Volts dc: 126.0 (mA) -15 Volts dc: 54.8 (mA)

End TEST: 15:37 (THUR HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number (enter 4 digits): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with sorting for Channels 50 at this STEP-STRESS Level.

Start TEST: 15:40 (THUR HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (t/T)	Detector 2 T (usec)	Detector 2 Duty Cycle (t/T)	Observations
0 dBm	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I > 0	"	50%	"		
	I + Q > 0	"	50%	4.61/9.54	48%	
	Q > 0	4.61/9.54	48%	"	48%	
Other: Specify -70 (dBm)	I > 0	4.61/9.54	48%			
	I > 0	4.77/9.54	50%			
	I + Q > 0	4.45/9.54	47%			
	Q > 0	"	47%			
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Pressure back noisy		4.77/9.54	50%	
	I > 0	4.77/9.54	50%	"	50%	
	I + Q > 0	4.13/9.54	43%	4.61/9.54	48%	
	Q > 0	4.29/9.54	45%	"	48%	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 01/23/92

STEP-STRESS Level: 5

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued.

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I > 0	"	50%	"	50%	
	I + Q > 0	"	50%	"	50%	
	Q > 0	4.45/9.54	47%	4.61/9.54	48%	
Other Specify -70 (dBm)	I > 0	4.45/9.54	47%			
	I > 0	4.77/9.54	50%			
	I + Q > 0	4.45/9.54	47%			
	Q > 0	"	47%			
Other Specify (dBm)	I > 0					
	I > 0				1	
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Present but noisy		4.61/9.54	48%	
	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I + Q > 0	4.13/9.54	43%	"	50%	
	Q > 0	4.45/9.54	47%	4.61/9.54	48%	

End TEST: 15:58 (hour:min:sec)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 01/22/92

STEP-STRESS Level: 5

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at the STEP-STRESS Level.

Start TEST: 16:01 (hour:min:sec)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *measure for cable losses
50	637.3	-3.1#	683.9	+11.4	1st Read Measured 637.2 -36.0 dBm 60
35	858.8	+11.4	729.0	+8.6	#Synth#1 is unlocked @ CH 50 & below bandwidth 684 MHz. Spectrum good @ CH 35 (off freq)
18	772.0	+10.8	825.0	+8.2	CH 18 unlocked & off freq same for CH 00. CH 35 & 00 @ same frequencies.
00	858.8	+7.8	921.0	+7.8	

Synthesizers are noisy. May effect auto measurements

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check box)

End TEST: 16:26 (hour:min:sec)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at the STEP-STRESS Level.

Need to verify anomaly Synth#1 (J5) Go to prior STRESS LEVEL 4 @ 16:34

END DWELL 16:34 (hour:min:sec)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1030

Test Date: 01/22/92

Tester: (Please fill in and stamp below)

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

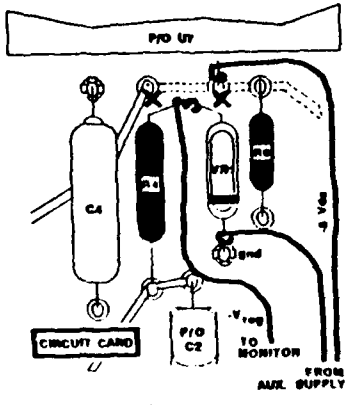
Start TEST: 15:38 (Hour Min Sec)

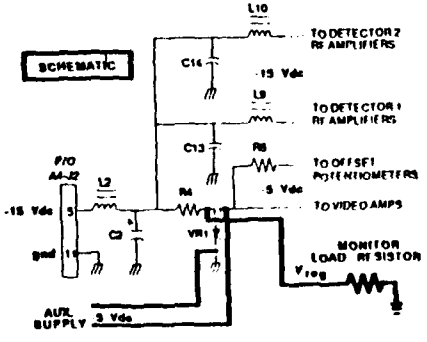
Voltage across LOAD RESISTOR: -5.177 (Vdc) (Refer to Appendix D, nominally -5 Vdc)

End TEST: 15:59 (Hour Min Sec)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is-60.5 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-66.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-60.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-64.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.1 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-63.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-60.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-62.8 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-60.8 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-63.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-65.4 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-62.4 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-60.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-62.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-59.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-60.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-59.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-58.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-60.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-63.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-66.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-59.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).

MSC 92466 TEST

1/22/92

MSN 1030
Level 5
J5 output

Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-64.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-63.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-62.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-60.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-60.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-62.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-59.8 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-62.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-59.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-58.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-63.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-63.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-62.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-60.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is-60.5 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is-66.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-64.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.1 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is-63.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.8 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.8 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-63.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is-65.4 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.4 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is-59.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).

Power at J5 is-59.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is-58.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is-63.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is-66.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is-59.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is-64.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is-63.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-59.8 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-59.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is-58.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-63.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-63.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

01/22/92

MSN 1030

LEVEL 5

J12 OUTPUT

****

Power at J12 is 8.8 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 684.0 MHz which is above the specified frequency.
Power at J12 is .5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than 690.0 MHz which is below the specified frequency.
Power at J12 is 4.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 693.0 MHz which is above the specified frequency.
Power at J12 is-5.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 696.0 MHz which is above the specified frequency.
Power at J12 is 1.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 705.0 MHz which is above the specified frequency.
Power at J12 is 4.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is less than 714.0 MHz which is below the specified frequency.
Power at J12 is 3.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is-64.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Frequency is less than 729.0 MHz which is below the specified frequency.
Power at J12 is 2.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 732.0 MHz which is above the specified frequency.
Power at J12 is 1.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Frequency is less than 735.0 MHz which is below the specified frequency.
Power at J12 is 1.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Frequency is less than 738.0 MHz which is below the specified frequency.
Power at J12 is 4.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 747.0 MHz which is above the specified frequency.
Power at J12 is 4.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Frequency is less than 750.0 MHz which is below the specified frequency.
Power at J12 is .9 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 756.0 MHz which is above the specified frequency.
Power at J12 is 2.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 762.0 MHz which is above the specified frequency.
Power at J12 is-4.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 765.0 MHz which is above the specified frequency.
Power at J12 is-3.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is less than 768.0 MHz which is below the specified frequency.
Power at J12 is 2.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 777.0 MHz which is above the specified frequency.
Power at J12 is .5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 825.0 MHz which is above the specified frequency.
Power at J12 is 1.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is .8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is less than 834.0 MHz which is below the specified frequency.
Power at J12 is 2.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 903.0 MHz which is above the specified frequency.
Power at J12 is 1.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is .8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 8.8 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is-64.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is .8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is .8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number: 1030 Test Date: 01/22/92

Tester: D. Mueller

STEP-STRESS Level: 4 (REFEST)

Return to LEVEL 4 STRESS TO VERIFY ANOMALY PREVIOUSLY OBSERVED AT LEVEL 5 SYNTH #1 (J5) UNLOCKED W/ ΔI = 35 MA

STEP-STRESS LEVEL DATA AT SAME FREQUENCY.

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 16:34 (hr:min) Decrease Temp & Voltages Start DWELL: 17:04 (hr:min)

STEP-STRESS Level Chamber Air Temperature: _____ (°C) (Chamber thermocouple reading) Set @ +4°C

Flange Temperature: _____ (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +10.2 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp, Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +5.80 (Vdc) -5 Volts dc: -5.00 (Vdc) *

+15 Volts dc: +16.20 (Vdc) -15 Volts dc: -16.20 (Vdc)

Ant. Coupler -5 Volts dc Setting: -5.11 (Vdc)

* Decrease stress of -5V from -6.00 to -5.80 caused Synth #1 (J5) to regain lock @ 16:36.

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 17:04 (hr:min)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 142.6 (mA) -5 Volts dc: 93.8 (mA)

+15 Volts dc: 123.7 (mA) -15 Volts dc: 53.9.0 (mA)

End TEST 17:06 (hr:min) decreased 4 mA from prior LEVEL 4

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number: 1030 Test Date: 01/22/92

STEP-STRESS Level: 4 (REFEST)

UUT PERPORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: OMIT (hr:min) Test Synth only.

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number (enter MSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 4 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Lmost T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Lmost T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: OMIT (Time: HR MIN) Test Synth only

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number (enter MSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 4 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at the STEP-STRESS Level.

Start TEST: 17:06 (Time: HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation (*measured for cable losses)
50 (MHz)	684.0	+11.2 ✓	OMIT		Synth #1 (J5) Data Compares to previous LEVEL 4 @ 14:25. NO FAILURE FOUND
35 (MHz)	729.0	+11.0 ✓	THIS		
18 (MHz)	824.9	+10.5 ✓	SYNTH		
00 (MHz)	921.0	+8.8 ✓			

Meas. affected by Noise present. Synthesizer #1 recovers. -5V stress pulled off freq.

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here) J5 ONLY

End TEST: 17:20 (Time: HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUE WITH LEVEL 6 STRESS End DWELL: 17:22 (Time: HR MIN)

@17:22. NO FAILURE FOUND LEVEL 5 & LEVEL 4 (RETEST)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (xxxx-xxx): 1030 Test Date: 01/22/92

Tester: (Please & stamp below) A.D. Mueller

STEP-STRESS Level (xxxx 0 - 10): 4 (RETEST)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

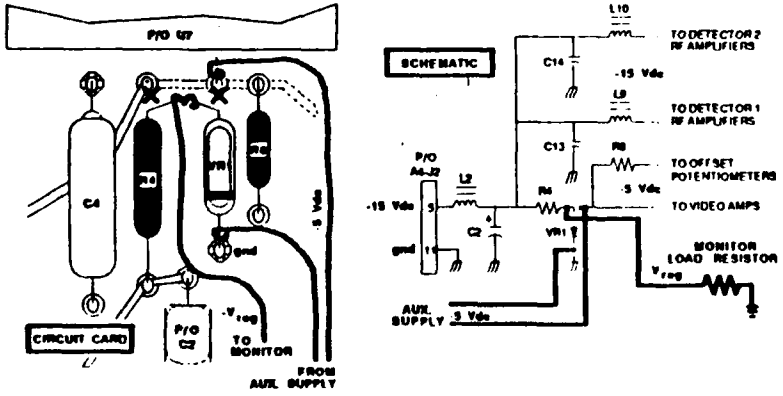
RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: OMIT (Mark RELIABLE) TEST SYNTH ONLY

Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: OMIT (Mark RELIABLE)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 7.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 2.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-1.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is .5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is .5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

01/22/92
MSN 1030
(ESC 92466 TEST)

LEVEL 4 (RETEST)
@ 17:11
J5 OUTPUT ONLY

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 6 Tester: (Name & stamp below)

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 17:22 (HHMM Hit MSH) (Program 2, Subroutine 12,) from LEVEL 4 (RESTEST) Start DWELL: 17:52 (HHMM Hit MSH)

STEP-STRESS Level Chamber Air Temperature: +109.2 (°C) (Chamber thermocouple reading) Set @ +111°C Plenge Temperature: +118.5 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +118 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increase Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.20 (Vdc) -5 Volts dc: -6.20 (Vdc) *

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.113 (Vdc)

* Synth #1 (J5) pulled off freq & unlocks @ -6.08 Vdc

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 17:54 (HHMM Hit MSH)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz. Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 148.3 (mA) -5 Volts dc: 97.9 (mA)

+15 Volts dc: 134.8 (mA) -15 Volts dc: 56.5 (mA)

End TEST: 17:55 (HHMM Hit MSH)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 17:57 (HHMM Hit MSH)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz. Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I > Q	"	50%	"	50%	
	I + Q > 0	"	50%	"	50%	
	Q > 0	4.61/9.54	48%	"	50%	
Other Specify -70 (dBm)	I > 0	4.61/9.54	48%			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.77/9.54	50%	4.61/9.54	48%	
	I > Q	4.77/9.54	50%	4.77/9.54	50%	
	I + Q > 0	4.13/9.54	43%	"	50%	
	Q > 0	"	43%	4.77/9.54	50%	

TEST Continued next page

Never not unlocked & unstable. Looking at Ant #2 Q>0 still Noisy. 1030 01/22/92

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 01/22/92

STEP-STRESS Level: 6

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 570.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I > 0	"	50%	"	50%	
	I + Q > 0	"	50%	4.61/9.54	48%	
	Q > 0	4.61/9.54	48%	"	48%	
Other Speed	I > 0	4.61/9.54	48%			
-70 (dBm)	I > 0					
	I + Q > 0					
	Q > 0					
Other Speed	I > 0					
	I > 0					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Too Noisy		4.45/9.54	47%	
	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I + Q > 0	4.13/9.54	43%	4.45/9.54	47%	
	Q > 0	"	43%	4.61/9.54	48%	

End TEST: 18:10 (Hour Min Sec)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 01/22/92

STEP-STRESS Level: 6

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 18:11 (Hour Min Sec)

Channel	Synthesizer 1 (J3) Frequency (MHz)	Synthesizer 1 (J3) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *corrected for cable losses
50 min	634.8	-2.7	683.9	+10.9	Synth #1 (J3) spectrum looks good. No longer unlocked, but is way off frequency (pulled by other synth).
35 min	681.1	+11.5	729.0	+9.8	
18 min	767.2	+13.0	824.9	+7.8	
00 min	852.9	+10.9 #	921.0	+6.6	Power good both Synths. Synth #2 on 18 looks marginal, to degrade

Monitored Synth 1 (J3) @ CH 00 during sample was drifting 852.4 MHz @ -10.9 dBm. Synthesizers are locked multiplied 17.42

Additional Testing (OPTIONAL): At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00

RADIO FREQUENCY OUTPUT TEST and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here) J12 ONLY

Auto Measurements affected by noise on sig-2

End TEST: 18:30 (Hour Min Sec)

At 18:34 terminated first plot (12 hrs max) & reload program to begin 2nd plot at 18:49. 01/24/92

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour in this STEP-STRESS Level.

End DWELL: 18:52 (Hour Min Sec)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 01/22/92

STEP-STRESS Level: 6 Tester: S.D. Mueller

UUT PERFORMANCE TEST DATA

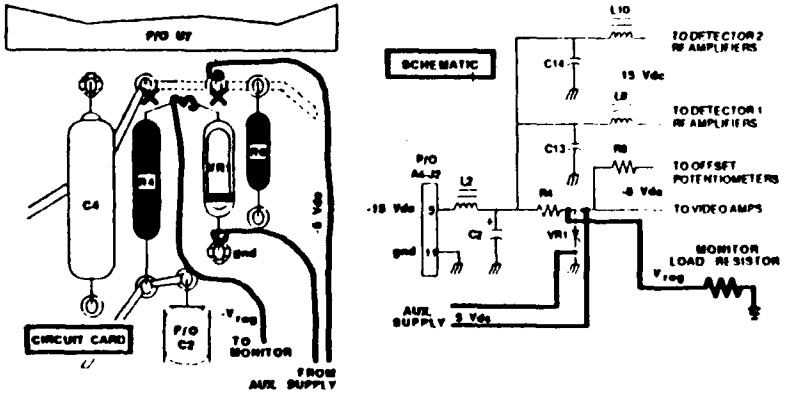
RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

Start TEST: 17:56

Voltage across LOAD RESISTOR: -5.19 (Vdc)

End TEST: 17:57

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 5.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 687.0 MHz which is above the specified frequency.
Power at J12 is 2.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 3.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 714.0 MHz which is above the specified frequency.
Power at J12 is 4.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Frequency is less than 744.0 MHz which is below the specified frequency.
Power at J12 is 6.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Frequency is less than 750.0 MHz which is below the specified frequency.
Power at J12 is 5.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Frequency is less than 756.0 MHz which is below the specified frequency.
Power at J12 is 1.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 765.0 MHz which is above the specified frequency.
Power at J12 is 3.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 774.0 MHz which is above the specified frequency.
Power at J12 is 3.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is less than 828.0 MHz which is below the specified frequency.
Power at J12 is 2.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Frequency is less than 882.0 MHz which is below the specified frequency.
Power at J12 is .9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 891.0 MHz which is above the specified frequency.
Power at J12 is .1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-10.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Frequency is less than 897.0 MHz which is below the specified frequency.
Power at J12 is 2.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 906.0 MHz which is above the specified frequency.
Power at J12 is 1.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is less than 912.0 MHz which is above the specified frequency.

01/22/92 636 466 1151
MSN 1030
LEVEL 6
@ 18:28
J12 OUTPUT ONLY

Power at J12 is-5.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is .1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-10.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number: 1030 Test Date: 01/22/92

Tester: J.D. Mueller

STEP-STRESS Level: 7

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 18:52 (hh:mm) Start DWELL: 19:22 (hh:mm)

STEP-STRESS Level Chamber Air Temperature: +117.2 (°C) Set @ +119°C (Chamber thermocouple reading) Floage Temperature: +127.1 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +126 (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.40 (Vdc) -5 Volts dc: -6.40 (Vdc)

+15 Volts dc: +17.10 (Vdc) -15 Volts dc: -17.10 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.113 (Vdc)

Both synthesizers show drift and are very dependent upon all voltages for Carrier Frequency as observed during ramp @ 19:13. Also Loading Detector = output hit w/ test data affects frequency. 19:16

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 19:22 (hh:mm)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 153.1 (mA) -5 Volts dc: 89.5 (mA)

+15 Volts dc: 131.4 (mA) -15 Volts dc: 57.4 (mA)

End TEST: 19:24 (hh:mm)

TEST continued next page

4C

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number: 1030 Test Date: 01/22/92

STEP-STRESS Level: 7

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 30 or this STEP-STRESS Level.

Start TEST: 19:58 (hh:mm)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 I (usec)	Detector 1 Duty Cycle (approx)	Detector 2 I (usec)	Detector 2 Duty Cycle (approx)	Observations
0 dBm	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I > Q	"	50%	"	50%	
	I + Q > 0	"	50%	"	50%	
	Q > 0	4.61/9.54	48%	4.61/9.54	48%	
Other: Specify -65 (dBm)	I > 0	4.77/9.54	50%			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Too noisy to measure		4.77/9.54	50%	
	I > Q	4.77/9.54	50%	"	50%	
	I + Q > 0	4.29/9.54	45%	"	50%	
	Q > 0	"	45%	4.61/9.54	48%	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (xxxx-1030): 1030 Test Date: 01/22/92

STEP-STRESS Level (zero 0 - ten 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J6) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q Bits	Detector 1 Limit T (sec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (sec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	9.77/9.54	50%	4.77/9.54	50%	
	I > 0	"	50%	"	50%	
	I + Q > 0	"	50%	"	50%	
	Q > 0	4.61/9.54	48%	4.61/9.54	48%	
	I > 0	4.45/9.54	47%			
Other: Specify	I > 0					
-70 (dBm)	I + Q > 0					
	Q > 0					
	I > 0	@ -65 4.61/9.54	48%			
Other: Specify	I > 0					
(dBm)	I + Q > 0					
	Q > 0					
	I > 0	Too Noisy See above		4.77/9.54	50%	
-75 dBm	I > 0	4.95/9.54	52%	"	50%	
	I + Q > 0	4.45/9.54	47%	"	50%	
	Q > 0	"	47%	4.61/9.54	48%	

End TEST: 20:09 (HHMM MS UNIT)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (xxxx-1030): 1030 Test Date: 01/22/92

STEP-STRESS Level (zero 0 - ten 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 19:25 (HHMM MS UNIT)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	632.8 (harmonic @ 949.2, -0.6 dBc)	-3.5	990.4	-14.4	Synth #2 (J12) used also @ 990 MHz / step attn = 1.5 dB has no harmonic
35 min	(618.4 harmonic @ 927.5, -29.8 dBc)	+11.0	990.3	-14.6	All at same frequency & power. Anomaly (See below)
18 min	844.8 No harmonic	+11.5	990.7	-13.5	
00 min	1st Atm 845.2 / Sub Atm 844.5 No harmonic	+11.0	990.3 / 990.9	-13.9	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 then Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with ULT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

End TEST: 19:57 (HHMM MS UNIT)

Tester 2. Used Freq Hop to evaluate. of six frequencies there is only 3 frequencies that appear intermittently 713 @ +11.2 dBm, 990 MHz as above and 850 @ +10.2 dBm. 1/22/92

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

RETURN TO LEVEL 6 TO CHECK ON ANOMALY SYNTH #2 (J12) A.D. Mueller 1/22/92

End DWELL: 20:22 (HHMM MS UNIT)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (nnnn MSN): 1030

Test Date: 01/22/92

Tester: (Please print clearly below)

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

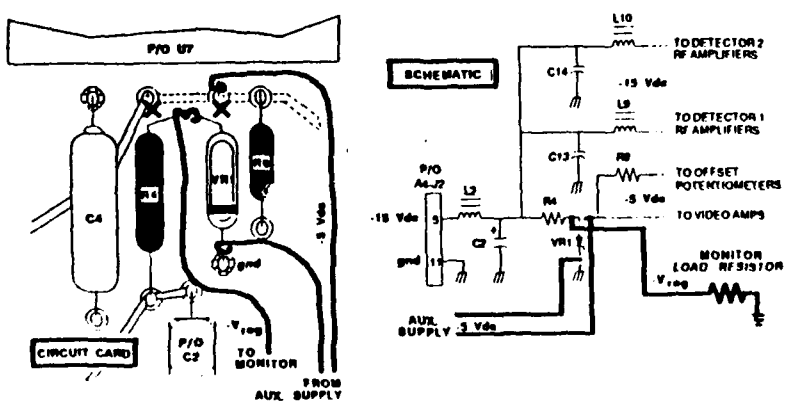
RESISTOR/ZENER DIODE MODIFICATION: As Built: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

Start TEST: 19:24 (Thrs: Hrs min)

Voltage across LOAD RESISTOR: -5.2085 (Vdc) (rnd to Appendix D: nominally 5 Vdc)

End TEST: 19:24 (Thrs: Hrs min)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter NSN): 1030 Test Date: 01/22/92

Tester: (Name & comp below)

STEP-STRESS Level (enter 0 - 10): 6 (RETEST #1)

ANOMALY AT SYNTH #2 (J12) FROM LEVEL 7 TO BE CHECKED AT LEVEL 6.

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 20:22 (HHMM HR MIN) (Programming using Manual Controller) Start DWELL: 20:52 (HHMM HR MIN)

STEP-STRESS Level Chamber Air Temperature: +109.5 (°C) (Chamber thermocouple reading) Set +111°C

Plenum Temperature: +119.5 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +118 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.20 (Vdc) -5 Volts dc: -6.20 (Vdc)

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant - 5 Volts dc Setting: -6.113 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 20:53 (HHMM HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1482 (mA) -5 Volts dc: 97.6 (mA)

+15 Volts dc: 134.8 (mA) -15 Volts dc: 564 (mA)

End TEST: 20:54 (HHMM HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter NSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 6 (RETEST #1)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: OMIT (HHMM HR MIN) SYNTH 3 ONLY

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter NSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 6 (RETEST #1)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 464 MHz. Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0			1		
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: OMIT (HHMM hrs MM) SYNTH ONLY

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter NSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 6 (RETEST #1)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 20:55 (HHMM hrs MM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measured for cable losses
50 min	634.4	-2.8 ✓	693.9	+11.0 ✓	SYNTH #2 (J12) IS ACCEPTABLE
35 min	680.7	+11.5 ✓	728.9	+9.6 ✓	
18 min	766.0	+13.1 ✓	824.9	+8.0 ✓ Slightly Low	NO FAILURE FOUND CHECKS WITH PRIOR LEVEL 6
00 min	851.8 SYNTH #1 also okay	+11.0 ✓	921.0	+5.4 ✓	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this **STEP-STRESS TEST DATA SHEET**. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

Used freq sweep (hop) Test #2 also. All frequencies appear present. /DM

End TEST: 21:13 (HHMM hrs MM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level

NO FAILURE FOUND. CONTINUE TO LEVEL 8 @

End DWELL 21:15 (HHMM hrs MM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (xxxx-1039): 1030 Test Date: 01/22/92

Tester: (Name & stamp below) S.D. Mueller

STEP-STRESS Level (xxxx 0 - 10): 6 (RETEST #1)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

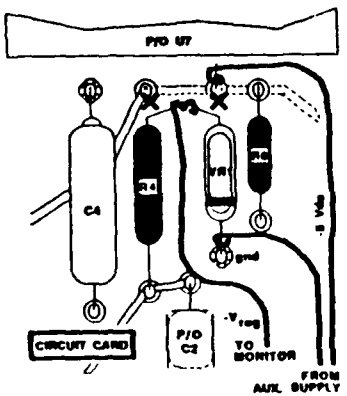
Start TEST: OMIT (TRUE RELIABILITY) SYNTHS ONLY

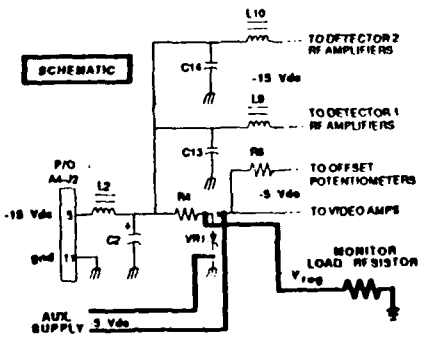
Voltage across LOAD RESISTOR: _____ (Vdc) (Refer to Appendix D; nominally -5 Vdc)

End TEST: OMIT (TRUE RELIABILITY)

50

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 6

UUT Serial Number (enter MSN): 1030 Test Date: 02/22/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 8

No FAILURE Found @ RETEST LEVEL 6 CONTINUED WITH STRESS LEVEL 8.

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 21:15 (TIME HR MIN) (Program #2, Indexed #16) Start DWELL: 21:45 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +125.0 (°C) (Chamber thermocouple reading) Set @ +127°C

Flange Temperature: +135.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +134 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: -6.60 (Vdc)

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: -17.40 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.113 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 21:45 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1576 (mA) -5 Volts dc: 84.0 (mA)

+15 Volts dc: 109.7 * (mA) Dropped below Level 0 Not current limited. -15 Volts dc: 589 (mA)

* ANOMALY SEEN

End TEST: 21:50 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 6

UUT Serial Number (enter MSN): 1030 Test Date: 02/22/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or 100 at this STEP-STRESS Level.

Start TEST: 21:52 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig (opt)	I & Q Bits	Detector 1 t (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	477/959	50%	477/959	50%	
	I > 0	"	50%	"	50%	More in the packet Data clock
	I + Q > 0	"	50%	"	50%	
	Q > 0	481/959	48%	481/959	48%	
Other Specify (dBm)	I > 0	481/959	48%			
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	NOISY		501/959	52%	
	I > 0	499/959	52%	477/959	50%	
	I + Q > 0	479/959	49%	"	50%	
	Q > 0	"	49%	"	50%	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter SSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 970.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q -Bits	Detector 1 Lower T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Lower T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I > 0	"	50%	"	50%	
	I > 0 > 0	"	50%	4.61/9.54	48%	
	Q > 0	4.61/9.54	48%	"	48%	
Other Specify -65 (dBm)	I > 0	4.69/9.54	45%			
	I > 0	4.77/9.54	50%			
	I > 0 > 0	4.61/9.54	48%			
	Q > 0	4.45/9.54	47%			
Other Specify -70 (dBm)	I > 0	VERY NOISY				
	I > 0	-70dBm 4.77/9.54	50%			
	I > 0 > 0	-70dBm 4.13/9.54	43%			
	Q > 0	-70dBm 4.29/9.54	45%			
-75 dBm	I > 0	VERY NOISY		4.77/9.54	50%	
	I > 0	4.13/9.54	43%	"	50%	
	I > 0 > 0	VERY NOISY		4.61/9.54	48%	
	Q > 0	VERY NOISY		4.93/9.54	52%	

End TEST: 22:08 (HHMM hrs MSN)

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 22:08 (HHMM hrs MSN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *comment for cable losses
50 (min)	979.0	-9.5	980.9	-14.3	Both Synthesizers fixed on single frequency & power output
35 (min)	979.8	-9.1	981.1	-13.8	
18 (min)	979.6	-8.5	980.9	-13.3	
00 (min)	979.4	-9.0	980.4	-13.6	

35: 921 MHz = 692 + 11.7dBm + 9.6 3rd 919 amplitude drops out Pulse Level

ANOMALY SEEN Both Synthesizers 01/22/92

Additional Testing (OPTIONAL): At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.
RADIO FREQUENCY OUTPUT TEST

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO

Using Freq Sweep Test #2 see single signal drift of Synth #2 (J12) Synth #1 (J5) has some of six frequencies 22:12 Current of +15V stable Low @ 10.6mA

End TEST: 22:34 (HHMM hrs MSN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

NEED TO VERIFY +15V current and both Synthesizer Output Returns to LEVEL 7 for TESTING at end of dwell

End DWELL: 22:45 (HHMM hrs MSN)

01/22/92

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1030

Test Date: 01/22/92

Tester: (Name & signature below)

STEP-STRESS Level (enter 0 - 10): 8

(924466 TEST)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

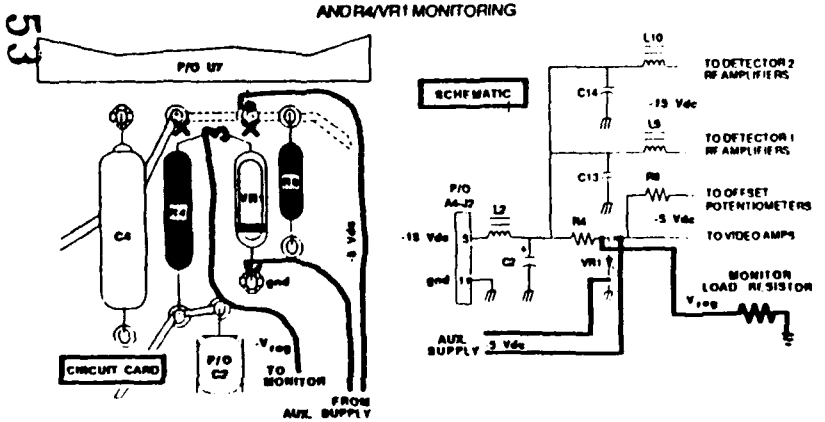
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 21:50 (Time HR:MIN)

Voltage across LOAD RESISTOR: −5.223 (Vdc) (refer to Appendix D: nominally -5 Vdc)

End TEST: 21:51 (Time HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter WSN): 1030 Test Date: 01/22/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 7 (RETEST)

FOR ANOMALY AT LEVEL 8.

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 22:45 (Thrsh HR MIN) (Decreased by Manual Control) Start DWELL: 23:15 (Thrsh HR MIN)

STEP-STRESS Level Chamber Air Temperature: +117.4 (°C) (Chamber thermocouple reading) SJT @ +119 °C Flange Temperature: +126.6 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +126 (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.40 (Vdc) -5 Volts dc: -6.40 (Vdc)

+15 Volts dc: +17.10 (Vdc) -15 Volts dc: -17.10 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.113 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 23:20 (Thrsh HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 152.8 (mA) Δ = 5mA ✓ -5 Volts dc: 89.4 (mA) Δ = 0.1mA ✓

+15 Volts dc: 131.4 (mA) ✓ Δ = 0 -15 Volts dc: 57.6 (mA) Δ = 1mA ✓

End TEST 23:22 (Thrsh HR MIN) +15V SUPPLY CURRENT CHANGE w/ PRIOR LEVEL 7 NO FAILURE FOUND

TEST continued on next page

5-4

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter WSN): 1030 Test Date: 01/22/92

STEP-STRESS Level (enter 0 - 10): 7 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 30 at this STEP-STRESS Level.

Start TEST: OMIT (Thrsh HR MIN) SYNTH'S & CURRENT ONLY

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 01/22/92

STEP-STRESS Level: 7 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued.

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q Bits	Detector 1 Limit T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: ONIT (TIME HR MIN) SYNTH'S #1 CURRENT ONLY

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 01/22/92

STEP-STRESS Level: 7 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 23:23 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *corrects for cable losses
50 (HI)	632.8 ~~1499.4~~ 1499.8	-3.51 ~~-13.8~~ -1.51	989.9	-14.4	START 100MHz/STEP 1.76MHz
35 (MID)	620.0	+11.0	990.2	-13.9	761 @ +13.0 (MID) 848 @ +11.0 (LO)
18 (LO)	761.2	+13.0	990.2	-13.4	* SYNTH #1 ANOMALY DIFFERENT CHIP FREQUENCY THAN PRIOR LEVEL 7 @ 19:29
00 (HI)	843.9	+11.0	990.3	-14.1	
CHIB	761.2	+13.0			SYNTH #2 MASKED BY VOLTAGES VALUES - AS WITH PRIOR LEVEL

Additional Testing (OPTIONAL): At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.
RADIO FREQUENCY OUTPUT TEST

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 23:51 (TIME HR MIN)

OBSERVED ANOTHER ANOMALY WITH SYNTH #1 (J5) @ CH18. SYNTH #2 (J12) STILL MASKED & CAN'T BE VERIFIED.

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

REDUCE STRESSES BACK TO LEVEL 6 TO CLEAR UP ANOMALY QUESTION. WILL BE RETEST 2. End DWELL 23:55 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE 01/22/92

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 01/22/92

Tester: L.D. Mueller

STEP-STRESS Level: 7 (RETEST)

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

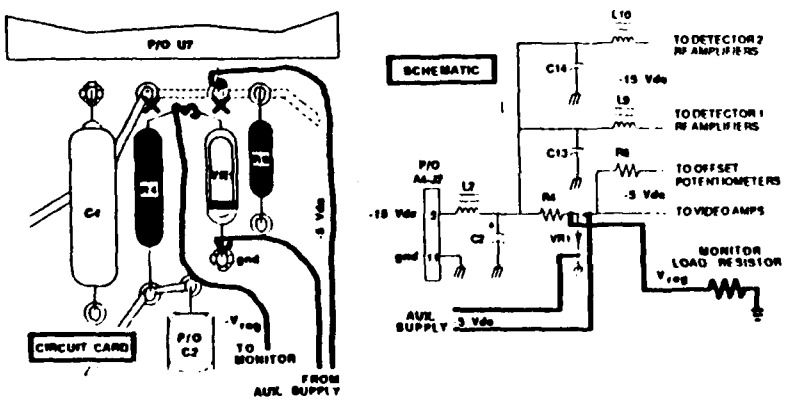
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: OMIT (TIME HR:MIN) SYNTH'S & CURRENT ONLY

Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D; nominally 1 Vdc)

End TEST: OMIT (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number: 1030 Test Date: 01/22/92 - 01/23/92

Tester: LD Mueller (92466 TEST)

STEP-STRESS Level: 6 (RETEST #2)

ANOMALY MASKED BY VOLTAGE STRESS AT LEVEL 5 AND AGAIN AT LEVEL 7. RETURN TO LEVEL 6 TO VERIFY.

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 23:55 (HOUR HR MIN) (Decrease from LEVEL 7 immediately) Start DWELL: 00:25 (TEMP HR MIN) 01/23/92

STEP-STRESS Level Chamber Air Temperature: +109.9 (°C) (Chamber thermocouple reading) Soak 111°C

Plunge Temperature: +119.6 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +118 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.20 (Vdc) -5 Volts dc: -6.20 (Vdc) SEE NOTE SHEET 4 **

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.113 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 00:35 (HOUR HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1501 (mA) Δ:19 Δ:19 -5 Volts dc: 95.0 (mA) Δ:6.4 Δ:6.6

+15 Volts dc: 132.8 (mA) Δ:2.8 Δ:2 -15 Volts dc: 56.5 (mA) Δ:0 Δ:1

End TEST 00:40 (HOUR HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number: 1030 Test Date: 01/23/92

STEP-STRESS Level: 6 (RETEST #2) (92466 TEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Inputs from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with sorting for Channels 50 at this STEP-STRESS Level.

Start TEST: OMIT (HOUR HR MIN) SYNTH'S ONLY

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 (Limit) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 (Limit) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number (enter WSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 6 (RETEST #2)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: 01:04 (HR MIN) OMIT SYNTH's ONLY

TEST continued next page

5c

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number (enter WSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 6 (RETEST #2)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 00:42 (HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *nominal for cable losses
50	634.4 (Meas @ 951.6 -1.9)	-2.8	684.0	+9.1 (@1)	All Synth #2 (J12) frequencies present.
35	680.6 (Meas @ 1021.0 - 8.4)	+11.4	729.0	+9.6 (@0.9)	
18	745.8 (No Meas)	+13.1	824.9	+7.5 (@0.7)	
00	865.3 **	+11.0	920.9	+7.8 (@1.2, @1.9)	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

** Reduced Voltage stress momentarily back to Level 0 to see effect on J5 Synth #1. All frequencies present. Increase back to Level 6 01:01

End TEST: 01:04 (HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

NO FAILURE FOUND.
INCREASE TO STRESS LEVEL 9

End DWELL: 01:10 (HR MIN)

Program #2, Interval #18

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter SN): 1030 Test Date: 01/23/92

Tester: (Name & stamp below) J. HAGG TEST

STEP-STRESS Level (enter 0 - 10): 6 (RETEST w/ 2)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

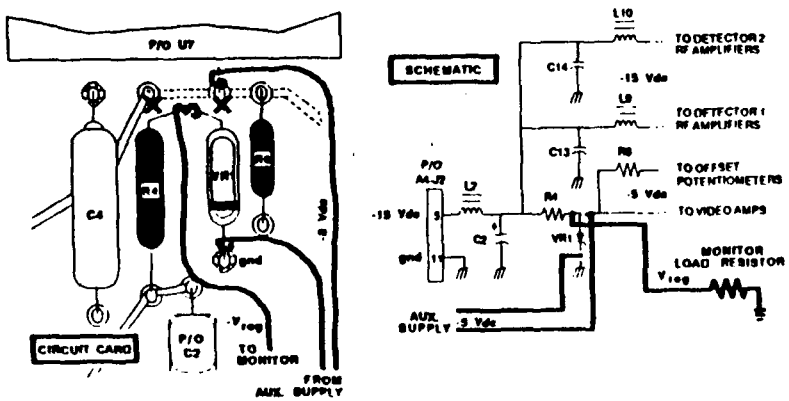
RESISTOR/ZENER DIODE MODIFICATION: As Built: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

Start TEST: OMIT (THREE MIN MIN) SYNTH'S ONLY

Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D; nominally -1 Vdc)

End TEST: OMIT (THREE MIN MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

Tester: (Please print name below)

STEP-STRESS Level (enter 0 - 10): 9

CONTINUED FROM ANOMALY CHECK NO FAULT FOUND LEVEL 8, 7, AND 6.

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 01:10 (HH:MM Hit when) (FROM ANOMALY CHECK/RETEST #2) PROGRAM #2, INTERNAL #8 Start DWELL: 01:40 (HH:MM Hit when)

STEP-STRESS Level Chamber Air Temperature: +132.8 (°C) (Chamber thermocouple reading) Set +135°C

Flange Temperature: +142.7 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +142 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.80 (Vdc) -5 Volts dc: -6.80 (Vdc)

+15 Volts dc: +17.70 (Vdc) -15 Volts dc: -17.70 (Vdc) Supply voltages not stable

Aux. Constant -5 Volts dc Setting: -5.113 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 01:49 (HH:MM Hit when)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 163.1 (mA) end Slowbreaking -5 Volts dc: 100.2 (mA) end Slowbreaking

+15 Volts dc: 120.8 (mA) end Slowbreaking -15 Volts dc: 595.50 / 599 (mA)

End TEST: 01:57 (HH:MM Hit when)

TEST continued next page

09

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -.75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 02:00 (HH:MM Hit when)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -.75 dBm

Rcv Sig Level	I & Q Data	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I > 0	"	50%	"	50%	
	I + Q > 0	"	50%	"	50%	
	Q > 0	"	50%	"	50%	
Other Specify -70 (dBm)	I > 0	4.6/9.54	48%			
	I > 0	—	—			
	I + Q > 0	—	—			
	Q > 0	—	—			
Other Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-.75 dBm	I > 0	TOO NOISY		4.93/9.54	52%	
	I > 0	4.93/9.54	52%	"	52%	
	I + Q > 0	4.29/9.54	45%	4.77/9.54	50%	
	Q > 0	4.13/9.54	43%	"	50%	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I > Q	"	50%	"	50%	
	I + Q > 0	"	50%	4.61/9.54	48%	
	Q > 0	4.61/9.54	48%	"	48%	
Other: Specify -70 (dBm)	I > 0	TOO NOISY				
	I > Q	4.77/9.54	52%			
	I + Q > 0	4.13/9.54	43%			
	Q > 0	4.29/9.54	45%			
Other: Specify -65 (dBm)	I > 0	4.45/9.54	47%			
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	TOO NOISY		4.93/9.54	52%	
	I > Q	"		5.09/9.54	53%	
	I + Q > 0	"		4.93/9.54	52%	
	Q > 0	"		4.45/9.54	47%	

End TEST 02:11 (HH:MM: MM SEC)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 02:11 (HH:MM: MM MDY)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measured for cable losses
50 min	915.8	+6.0	947.1	-4.0	Same frequencies across band ± 1 MHz
35 min	914.9	+6.8	947.1	-4.0 same	
18 min	914.5	+7.2	946.4	-2.7	CANT VERIFY STATUS
00 min	913.9	+6.8	946.2	-3.1	

Power back up on Synth #1 (J5) & #2 (J12)

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

Synthesizers fixed on single frequency due to voltage stresses.

End TEST: 02:37 (HH:MM: MM MDY)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

Need to verify Synthesizer #1 & #2 STATUS GO back to prior LEVEL 8. End DWELL 02:40 (HH:MM: MM MDY)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 1030

Test Date: 01/23/92

Tester: (Please & stamp below) A.D. Mueller (16 1466 TEST)

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

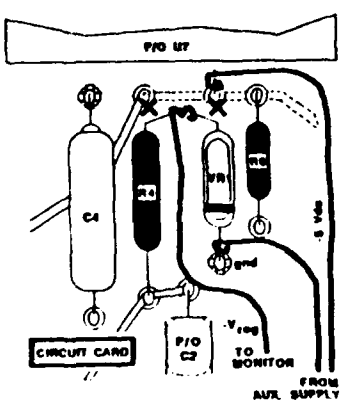
RESISTOR/ZENER DIODE MODIFICATION: A4 Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

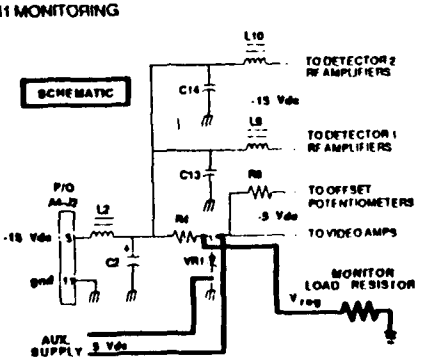
Start TEST: 01:57 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.238 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 01:57 (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number: 1030 Test Date: 01/23/92

Tester:

STEP-STRESS Level: 8 (RETEST)

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 02:40 (Decrease from LEVEL 9 manually) Start DWELL: 03:10

STEP-STRESS Level Chamber Air Temperature: +125.2 (°C) Flange Temperature: +136.5 (°C)

Set @ +127

STEP-STRESS Level Component Temperature: +134 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level.

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: -6.60 (Vdc) See NOTE Sheet 4 #4

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: -17.40 (Vdc)

Aux. Counter - 5 Volts dc Setting: -5.1 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 03:10

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 155.9 (mA) -5 Volts dc: 93.7 (mA) See NOTE Sheet 4 #4

+15 Volts dc: 123.8 (mA) -15 Volts dc: 59.3 (mA)

End TEST 03:11

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number: 1030 Test Date: 01/23/92

STEP-STRESS Level: 8 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: OMIT SYNTHESIS ONLY

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

Okay

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q Bits	Detector 1 Lmax T (sec)	Detector 1 Duty Cycle (percent)	Detector 2 Lmax T (sec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

Okay

End TEST: 0411 (TIME HR MIN) SYNTH'S ONLY

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 03:12 (TIME HR MIN) (03:31)

Channel	Synthesizer 1 (J3) Frequency (MHz)	Synthesizer 1 (J3) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation
50 (HEX)	915.5 (683.9)	-8.6 (+9.8)	978.6 (683.9)	-13.7 (+10.8) Slow to Lock	** Measurements in parenthesis ( ) are at LEVEL 0 reduced voltage stress. Temperature still set at LEVEL 8 Voltage was decreased incrementally & unstable
35 (HEX)	976.6 (729.0)	-8.2 (+9.6)	979.1 (729.0)	-13.2 (+8.3)	
18 (HEX)	976.9 (829.9)	-7.8 (+8.8)	978.3 (825.0)	-12.8 (+6.8)	
00 (HEX)	917.2 (921.0)	-8.4 (+3.6)	979.4 (920.9)	-13.3 (+3.3)	

*measured for cable losses

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

Can not identify status at LEVEL 8. Reduce Voltages to nominal to verify. All Synth #1 J3s frequencies passed however Synth #2 J12 unlocks at 5 frequencies of 51. This at LEVEL 0 Voltages.

End TEST: 03:23 (TIME HR MIN) (03:51)

**NOTE: Reduced Voltages to Level 0 at 03:25. Current +5V: 91231 ma -5V: 90.7 ma +15V: 109.7 ma -15V: 497 ma Increased voltages back to LEVEL 8 at 03:54

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

Power out at reduced voltage is reasonable for temperature extreme. Will proceed on to LEVEL 10 (Program #2, Interval #20)

End DWELL: 04:20 (TIME HR MIN)

Level 8 re-started from 03:54 to 04:20

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 01/23/92

STEP-STRESS Level: 8 (RETEST) Tester: L.D. Mullen

UUT PERFORMANCE TEST DATA

RESISTOR/ZENER DIODE MODIFICATION: As Dwdt: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

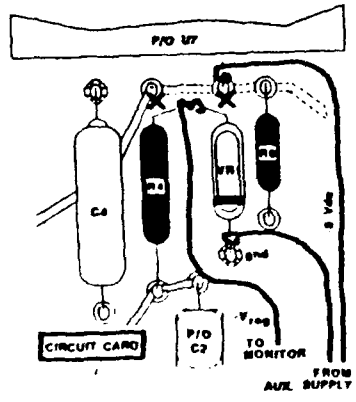
Start TEST: OMIT (Test No. only) SYNTH'S ONLY

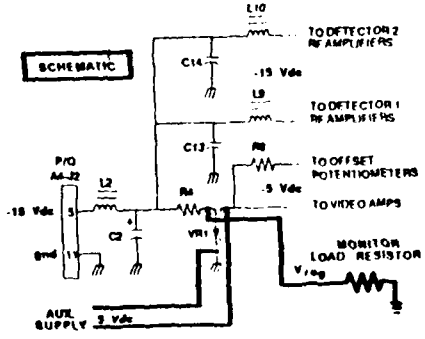
Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D, normally 1 Vdc)

End TEST: OMIT (Test No. only)

C9

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 10

Proceeding from LEVEL 8 (retest)

STEP-STRESS LEVEL DATA

Plot terminated in error. Restart Plot @ 04:45 missing transition data

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 04:20 (TTMM HR MIN) (Program #2, Interval #2a) Start DWELL: 04:50 (TTMM HR MIN)

STEP-STRESS Level Chamber Air Temperature: +140.6 (°C) (Chamber thermocouple reading) Sat @ +143°C

Flange Temperature: +152.0 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +150 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +7.00 (Vdc) -5 Volts dc: -7.00 (Vdc)

+15 Volts dc: +18.00 (Vdc) -15 Volts dc: +18.00 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.113 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 04:51 (TTMM HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 166.8 (mA) -5 Volts dc: 105.9 (mA)

+15 Volts dc: 125.8 (mA) -15 Volts dc: 62.3 (mA)

End TEST: 04:52 (TTMM HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 on this STEP-STRESS Level.

Start TEST: 04:56 (TTMM HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77/9.54	50%	4.77/9.54	50%	
	I > Q	"	50%	"	50%	
	I + Q > 0	"	50%	"	50%	
	Q > 0	4.61/9.54	48%	4.43/9.54	47%	
Other Specify -70 (dBm)	I > 0	4.43/9.54	47%			
	I > Q	—	—			
	I + Q > 0	—	—			
	Q > 0	—	—			
Other Specify ____ (dBm)	I > 0			—	—	
	I > Q			—	—	
	I + Q > 0			—	—	
	Q > 0			—	—	
-75 dBm	I > 0	NO154		4.61/9.54	48%	
	I > Q	4.93/9.54	52%	"	48%	— j.Hee
	I + Q > 0	4.79/9.54	45%	"	48%	
	Q > 0	4.79/9.54	43%	4.43/9.54	47%	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter WSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Lmost T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L(most) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	477/9.5Y	50%	477/9.5Y	50%	
	I > Q	"	50%	"	50%	
	I + Q > 0	"	50%	461/9.5Y	48%	
	Q > 0	445/9.5Y	47%	"	48%	
Other: Specify -70 (dBm)	I > 0	TO NOISY				
	I > Q	509/9.5Y	53%			
	I + Q > 0	445/9.5Y	47%			
	Q > 0	413/9.5Y	43%			
Other: Specify -65 (dBm)	I > 0	449/9.5Y	47%			
	I > Q					
	I + Q > 0					
	Q > 0					
.75 dBm	I > 0	VERY NOISY		477/9.5Y	48%	
	I > Q	NOISY		"	48%	
	I + Q > 0	NOISY		"	48%	
	Q > 0	NOISY		445/9.5Y	47%	

End TEST: 05:09 (HHMM MS MSM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter WSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 05:10 (HHMM MS MSM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	731.3	+11.0	823.1	+7.8	– typical
35 min	726.3	+11.3	821.4	+8.4	– erratic
18 min	724.4	+11.7	816.9	+9.0	– erratic diff
00 min	721.8	+11.2	814.7	+8.4	– Same

Synth #2 (J12) drift from 813 to 824 MHz

Power output good on both Synthesizers In passband.

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 05:22 (HHMM MS MSM) Rerun to exercise unit 05:48

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at the STEP-STRESS Level.

Reduce to LEVEL 9 to verify Synthesizer STATUS.

End DWELL 05:50 (HHMM MS MSM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030

Test Date: 01/23/92

Tester: L.D. Mueller

STEP-STRESS Level: 10

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

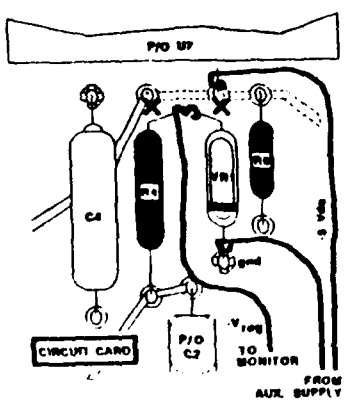
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

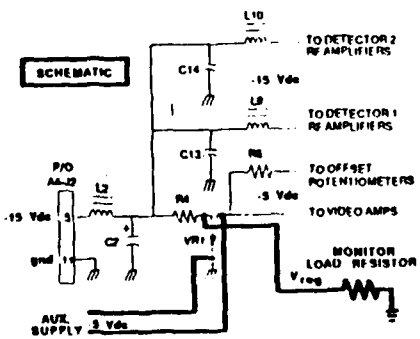
Start TEST: 04:52

Voltage across LOAD RESISTOR: -5.2517 (Vdc)

End TEST: 04:53

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

Tester: (Name & agency below)

STEP-STRESS Level (enter 0 - 10): 9 (RETEST) A.D. Mueller (GSFC)

Decrease from LEVEL 10 TO VERIFY SYNTH'S STATUS

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 05:50 (Hour Min) (Manual Control) Start DWELL: 06:20 (Hour Min)

STEP-STRESS Level Chamber Air Temperature: +133.0 (°C) Set @ +135 (Chamber thermocouple reading) Flange Temperature: +144.1 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +142 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.80 (Vdc) -5 Volts dc: -6.80 (Vdc) SEE NOTE SHEET 4 ##

+15 Volts dc: +17.70 (Vdc) -15 Volts dc: -17.70 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.113 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 06:21 (Hour Min)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 162.2 (mA) -5 Volts dc: 105.2 (mA) SEE NOTE SHEET 4

+15 Volts dc: 126.8 (mA) -15 Volts dc: 60.1 (mA)

End TEST 06:22 (Hour Min)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 1 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 9 (RETEST) (92 GSFC TEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: OMIT (Hour Min) SYNTH'S ONLY

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 9 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L(max) T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 L(max) T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					

End TEST (HHMM MS MM) OMIT SYNTH1 ONLY

TEST continued on next page

(1) 1

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1030 Test Date: 01/23/92

STEP-STRESS Level (enter 0 - 10): 9 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 06:22 (06:41) (HHMM MS MM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *minimum for cable losses
50 min	911.3 (684.0)	+6.4 (+10.8)	942.0 (684.0)	-2.41 (+10.8)	** Reduce Voltages to nominal LEVEL 0 Values recorded & incrementally Data in parentheses ( ) under these conditions
35 min	909.2 (775.0)	+7.34 (+10.7)	940.9 (738.7)	-1.36 (+10.8)	
18 min	910.4 (825.0)	+7.7 (+9.5)	941.4 (829.5)	-1.14 (+8.7)	
00 min	910.8 (920.9)	+7.03 (+4.7)	942.5 (921.0)	-1.87 (+3.1)	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

End TEST: 06:37 (06:54) (HHMM MS MM)

** NOTE: Reduce voltages to LEVEL 0 beginning @ 06:38
Return voltages to LEVEL 9 completed @ 06:59

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

Stabilize 30 minutes at LEVEL 9
CONTINUE TO LEVEL 11. End DWELL 07:30 (HHMM MS MM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter SER#): 1030 Test Date: 01/23/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 9 (RETEST) A.D. Mueller

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

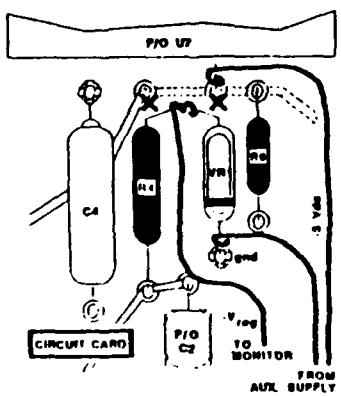
Start TEST: OMIT (TIME HR:MIN) SYNTH'S ONLY

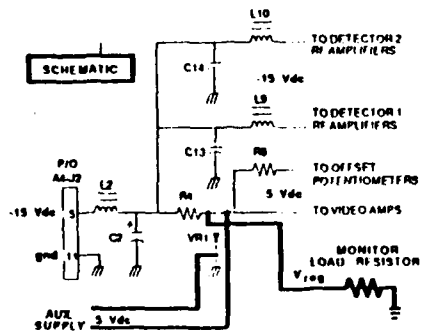
Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D, nominally 1 Vdc)

End TEST: OMIT (TIME HR:MIN)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 01/23/92

STEP-STRESS Level: 11 Tester:

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 07:30 Start DWELL: 08:00

STEP-STRESS Level Chamber Air Temperature: 148.3 (°C) Plunge Temperature: [illegible] (°C)

STEP-STRESS Level Component Temperature: (°C)

VOLTAGE STEP-STRESS During Temperature Ramp, Increment Voltage to STEP-STRESS Level

Supply Voltages: +5 Volts dc: 7.2 (Vdc) -5 Volts dc: 7.2 (Vdc)

+15 Volts dc: 18.3 (Vdc) -15 Volts dc: -18.3 (Vdc)

Aux. Constant - 5 Volts dc Setting: -51 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 07 15

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1130 (mA) -5 Volts dc: 117 (mA)

+15 Volts dc: 126 (mA) -15 Volts dc: 632 (mA)

End TEST: 07 16

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 1/23/92

STEP-STRESS Level: 11

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input From 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 08 16

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77/9.54	50	4.77/9.54	50	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.77/9.54	48	"	"	
Other Specify:	I > 0	4.77/9.54	50			
	I > Q	5.01/9.54	53			
(dBm)	I + Q > 0	4.77/9.54	48			
	Q > 0	4.53/9.54	47			
Other Specify:	I > 0			4.77/9.54	50	
	I > Q			"	"	
(dBm)	I + Q > 0			"	"	
	Q > 0			"	"	
-75 dBm	I > 0	no sig		no sig		
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number (enter MSN): 1030 Test Date: 1/23/92

STEP-STRESS Level (enter 0 - 10): 11

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.71m/4.54m	50	4.71m/4.54m	50	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.61m/4.54m	48	"	"	
50 Other Specify (dBm)	I > 0	4.71m/4.54m	50			
	I > Q	5.01m/4.54m	53			
	I + Q > 0	4.61m/4.54m	48			
	Q > 0	4.61m/4.54m	48			
65 Other Specify (dBm)	I > 0			4.71m/4.54m	50	
	I > Q			"	"	
	I + Q > 0			"	"	
	Q > 0			"	"	
-75 dBm	I > 0	d/p very noisy				
	I > Q	noisy				
	I + Q > 0	"				
	Q > 0	"				

End TEST: 09 37 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number (enter MSN): 1030 Test Date: 1/23/92

STEP-STRESS Level (enter 0 - 10): 11

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at the STEP-STRESS Level.

Start TEST: 08 00 (TIME HR MIN)

Ch (pin)	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *Measure for cable losses
50 min	sweep < 829	-24	< 659	4.9	
35 min	821	-1.0	< 655	4.7	
18 min	821	-.8	< 659	5.7	
00 min	821	-1.0	< 659	4.8	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT Real (Check here)

End TEST: 09 15 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1 hour at this STEP-STRESS Level

End DWELL: 09 00 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter SERN): 1030

Test Date: 1/23/97

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 11

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

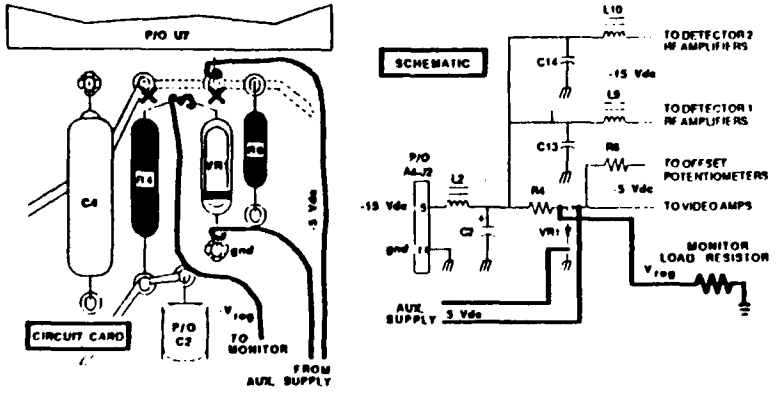
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 09:47 (Hour Min later)

Voltage across LOAD RESISTOR: 5.11 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 09:48 (Hour Min later)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

UUT Serial Number (enter MSN): 1030 Test Date: 1/23/92

STEP-STRESS Level (enter 0 - 10): 10 Tester:

-15V Power supply problem Ramp back to level 0 @ 09:48

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 09:50 (TIME HR MIN) decrease time using manual Control Start DWELL: 09:30 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 140.5 (°C) (Chamber thermocouple reading) ~~143~~ Flange Temperature: 148.5 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 150 (°C) (refer to Appendix D Table)

C2

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: 17.21 (Vdc) - 5 Volts dc: -7.20 (Vdc) These are the setting @ 09:25 per to Dwell

+15 Volts dc: +18.33 (Vdc) -15 Volts dc: -2.22 * (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

* prior to reaching Dwell @ 09:25 -15V supply changed to -7.21V (P344A Supply voltages had not been adjusted to level 10 settings

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level. These are the current @ 09:25

Start TEST: (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 187.4 (mA) - 5 Volts dc: 107.3 (mA)

+15 Volts dc: 116.3 (mA) -15 Volts dc: 3.9 (mA)

End TEST: 09:41 (TIME HR MIN) Tried cycling power off/on unit & -15V supply No detector & sigal outputs

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number (enter MSN): Test Date:

STEP-STRESS Level (enter 0 - 10):

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (1/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number (enter MSW): _____ Test Date: _____

STEP-STRESS Level (enter 0 - 10): _____

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q -Bits	Detector 1 L(max) T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 L(max) T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: _____ (HHMM MM DD)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number (enter MSW): _____ Test Date: _____

STEP-STRESS Level (enter 0 - 10): _____

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: _____ (HHMM MM DD)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *comment for cable losses
50 (hex)					
35 (hex)					
18 (hex)					
00 (hex)					

Additional Testing (OPTIONAL); RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT _____ (Check here)

End TEST: _____ (HHMM MM DD)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: _____ (HHMM MM DD)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): _____ Test Date: _____

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): _____ _____

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

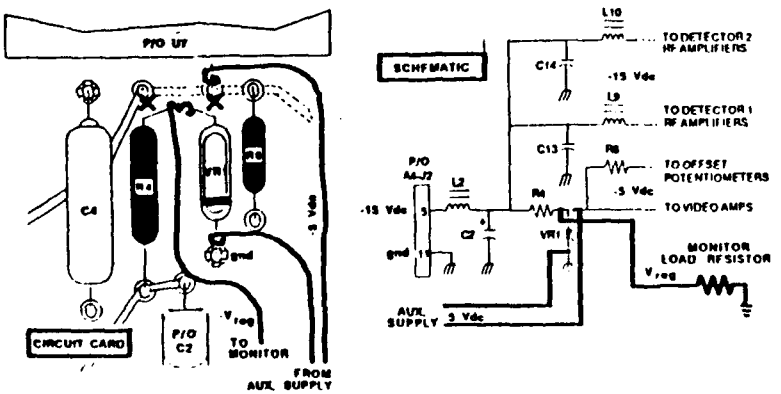
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: _____ (Hold HR:MN)

Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: _____ (Hold HR:MN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1030 Test Date: 1/22/92

Tester:

STEP-STRESS Level: 0

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 09:48 (TIME HR MIN) Prog 2 (Interval 22 (transition 40min. Stabilize 30min)) Start DWELL: 10:58 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 61.8 (°C) (Chamber thermocouple reading) Flange Temperature: 67.1 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 70 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +5.00 (Vdc) -5 Volts dc: -5.05 (Vdc)

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: off (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 11:00 (TIME HR MIN) Disconnected Pwr to Syn (TI2) 15V supply brkt + -15Vdc

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 684 (mA) -5 Volts dc: 64 (mA)

+15 Volts dc: 889 (mA) -15 Volts dc: 423 (mA)

End TEST: 11:01 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1030 Test Date: 1/22/92

STEP-STRESS Level: 0

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synchronized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 50 on this STEP-STRESS Level.

Start TEST: 11:01 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 I (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 I (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.77u / 9.54u	50	4.77u / 9.54u	50	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.611 / 9.54u	48	4.611 / 9.54u	48	
-65 (dBm)	I > 0	4.611 / 9.54u	48			
Other Specify	I > Q	5.01 / 9.54u	53			
	I + Q > 0	4.583 / 9.54u	48			
	Q > 0	4.452 / 9.54u	47			
-70 (dBm) Other Specify	I > 0			4.76u / 9.54u	50	
	I > Q			"	"	
	I + Q > 0			"	"	
	Q > 0			"	"	
-75 dBm	I > 0	Very noisy		noisy		
	I > Q	Noisy		"		
	I + Q > 0	noisy		"		
	Q > 0	noisy		"		

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter HEX): 1030 Test Date: 1/23/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L (usec) / I (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) / I (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.7µs/9.4µs	50	4.6µs/9.4µs	48	
	I > 0	"	"	4.7µs/9.4µs	50	
	I + Q > 0	4.5µs/9.4µs	48	4.6µs/9.4µs	48	
	Q > 0	"	"	4.6µs/9.4µs	48	
60 Other Specify (dBm)	I > 0	4.5µs/9.4µs	48			
	I > 0	4.7µs/9.4µs	50			
	I + Q > 0	4.5µs/9.4µs	45			
	Q > 0	4.5µs/9.4µs	45			
70 Other Specify (dBm)	I > 0			4.7µs/9.4µs	50	
	I > 0			"	"	
	I + Q > 0			"	"	
	Q > 0			"	"	
-75 dBm	I > 0	very noisy		noisy		
	I > 0	noisy				
	I + Q > 0	noisy				
	Q > 0	noisy				

End TEST 11:20 (TIME HR MIN)

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter HEX): 1030 Test Date: 1/23/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 11:20 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *minimum for stable lasers
50 min	684	11.59			Syn #2 (J12) -15V short
35 min	727	11.04			
18 min	825	11.06			
00 min	921	10.43			

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST 11:30 (TIME HR MIN)

STEP STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP STRESS The Dwell will have a duration of 1 hour at this STEP-STRESS Level

End DWELL (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSPE): 103D

Test Date: 1/24/92

Tester: (Please & stamp below)

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

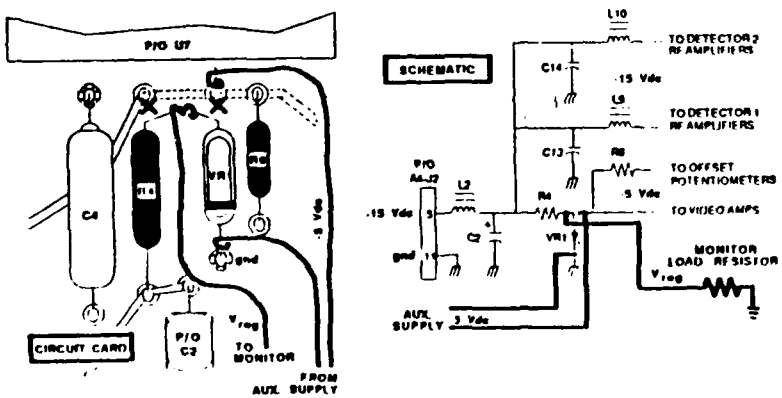
Start TEST: 11:30 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.0115 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 11:31 (TIME HR MIN)

60

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



1/23/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 1.1 dBm @ 684.0 MHz (Spec=+9dBm minimum). Syn Det # 1030 0
Power at J5 is 7.5 dBm @ 687.0 MHz (Spec=+9dBm minimum). stress level
Power at J5 is 5.3 dBm @ 690.0 MHz (Spec=+9dBm minimum). J5 output
Power at J5 is-2.4 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 6.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 1.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.4 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

TEST EQUIPMENT & CALIBRATION LOG

Maintain Log for testing conducted 1/17/92 through 1/22/92

ITEM	DESCRIPTION	Manuf. & Part No.	ID NUMBER	LAST CAL*	CAL* DUE	Item Notes
01	T/R Test Station	HAC; SPECIAL	G-132043	NCR		
02	Control Panel	HAC; SPECIAL	G-132290	NCR		
03	Signal Generator	HP; 8660C	G-128063	12/17/91	01/13/93	
04	Auxiliary Section	HP; 86631B	G-128062	NCR		
05	RF Section	HP; 86603A	G-128063	12/17/91	01/13/92	
06	Spectrum Analyzer	HP, 8568A w/ Opt E16	G-132082	12/11/91	10/30/92	
07	FET Probe	HP; 1120A	G-132255	12/19/1990	6/30/92	
08	Power Meter	HP, 436A	G-128036	6/11/91	11/24/92	
09	Power Sensor	HP, 8482A	G-128059	9/9/91	10/21/92	
10	Oscilloscope	HP, 1980B	G-132049	9/24/91	5/11/92	
11	Digital Multimeter	SystronDonner; 7344A	G-127998	6/6/91	5/11/92	
12	Digital Multimeter	HP; 3478A	H-A53624	9/6/91	6/12/92	
13	Power Splitter	MiniCkts; ZFSC-2-5	none	NCR		
14	Power Splitter	MiniCkts; ZFSC-2-5	none	NCR		
15	Reg. Power Supply	Lambda; LP-531-FM	G-132292	NCR		-15V DC
16	Reg. Power Supply	Lambda; LP-531-FM	same			+15V DC
17	Reg. Power Supply	Lambda; LP-530-FM	G-132291	NCR		+5V
18	Reg. Power Supply	Lambda; LP-520-FM	same			-5V DC
19	Computer	HP; 9845B	G-125090	NCR		
20	Flex. Disk Memory	HP; 9895A	G-125089	NCR		
21	Signal Generator					
22	Oscilloscope	Tektronix; 2465				
23	Digital Multimeter					
24	Digital Multimeter					
25	Digital Multimeter					
26	Thermal Chamber	Thermotron; S-4 w/Cntl	H-805547	9/18/91	9/2/91	
27	Data Acqtn Cntl Unit	HP; 3497A	H-42B499	11/4/91	7/29/92	
28	Computer	HP, Model 85	G-595184	N/A	NCR	
29	Power Supply, AUX.	HP 6299A Pwr Supply	H-3570A1	NCR		
30						
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41						
42						

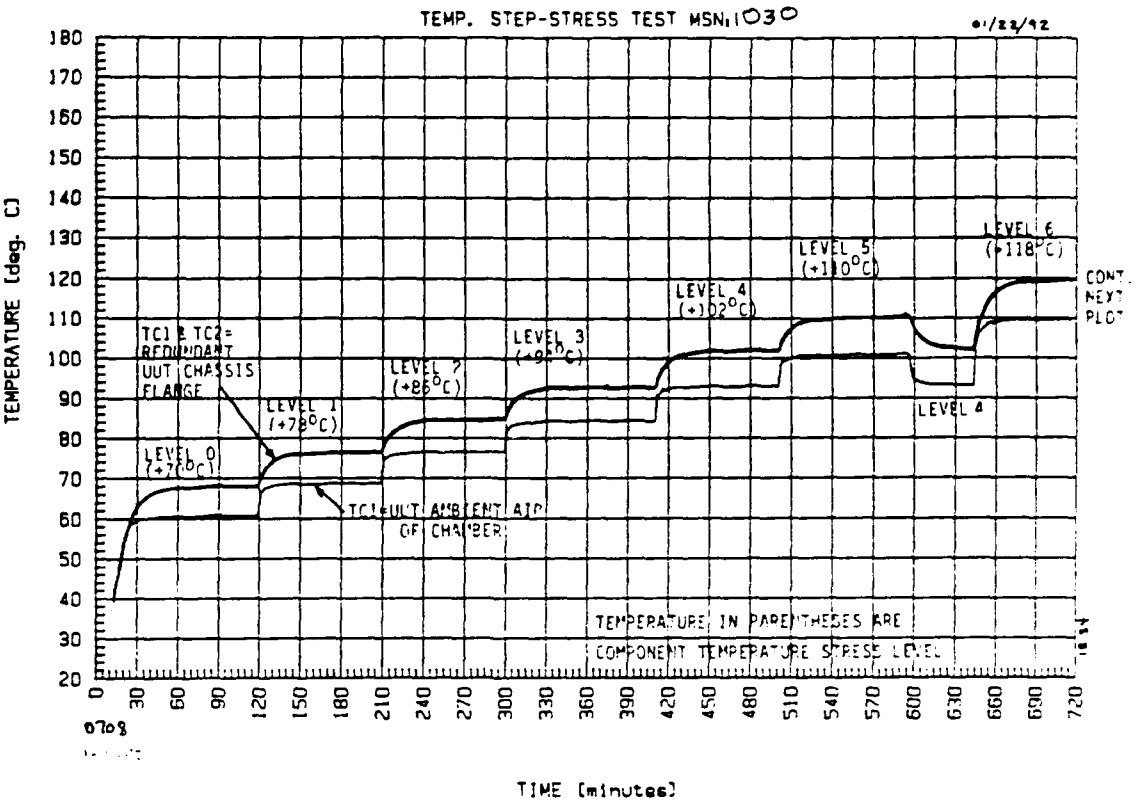
*NCR = No Calibration Required

DATE: ~~1-16-92~~ 1/21/92 TIME: ~~11:59PM~~ 07 15 Am

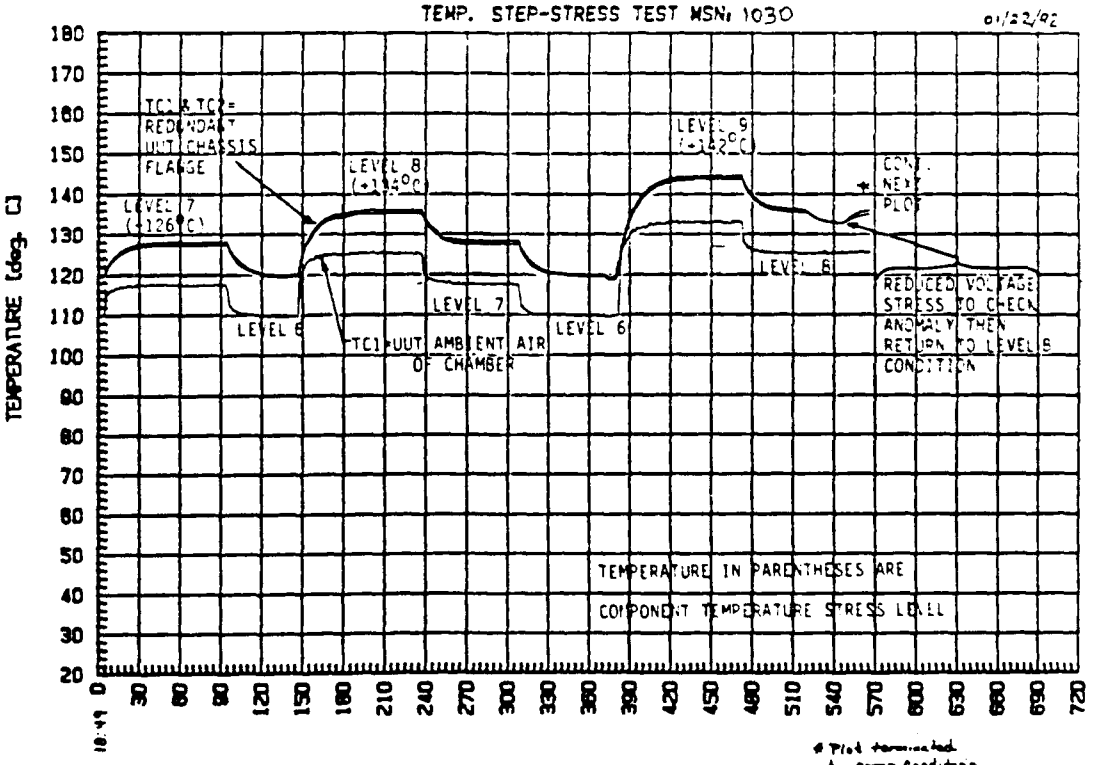
```
Synth_ref= 1499990
Freq_mod_ref= 9999990
Sp_clock_output =  0
Phase_lo_output =  1.03
Phase_if_output =  0
Up_dn_conv_lo =  3.42
313.75_lo =  15 dBm /313.75182E6MHz
```

Channel	Freq	Dn_conv_output	Synth_lo_output	Hit_sgnl_l_o
50	684	1.06	1.09	2.11
49	687	1.13	1.26	2.03
48	690	1.2	1.3	1.92
47	693	1.23	1.15	1.89
46	696	1.22	1.06	1.91
45	699	1.24	1.19	1.88
44	702	1.25	1.32	1.78
43	705	1.26	1.31	1.8
42	708	1.26	1.25	1.87
41	711	1.29	1.32	1.85
40	714	1.33	1.44	1.73
39	717	1.34	1.4	1.63
38	720	1.28	1.34	1.72
37	723	1.28	1.47	1.79
36	726	1.32	1.67	1.75
35	729	1.34	1.74	1.68
34	732	1.3	1.62	1.69
33	735	1.3	1.51	1.71
32	738	1.29	1.63	1.68
31	741	1.29	1.73	1.6
30	744	1.27	1.73	1.67
29	747	1.3	1.74	1.78
28	750	1.34	1.86	1.79
27	753	1.4	1.97	1.7
26	756	1.37	1.87	1.63
25	759	1.31	1.72	1.66
24	762	1.33	1.79	1.73
23	765	1.38	1.97	1.67
22	768	1.43	2.06	1.67
21	771	1.47	1.98	1.72
20	774	1.56	1.94	1.81
19	777	1.57	2.03	1.73
18	825	1.62	2.16	1.68
17	828	1.6	2.24	1.66
16	831	1.6	2.28	1.55
15	834	1.6	2.22	1.59
14	837	1.65	2.12	1.6
13	882	1.56	2	1.4
12	885	1.51	1.95	1.4
11	888	1.6	1.91	1.48
10	891	1.62	1.98	1.51
9	894	1.57	2.02	1.43
8	897	1.55	1.95	1.37
7	900	1.61	1.84	1.37
6	903	1.57	1.76	1.4
5	906	1.48	1.78	1.32
4	909	1.39	1.83	1.28
3	912	1.43	1.79	1.37
2	915	1.49	1.77	1.47
1	918	1.48	1.75	1.46
0	921	1.38	1.73	1.37

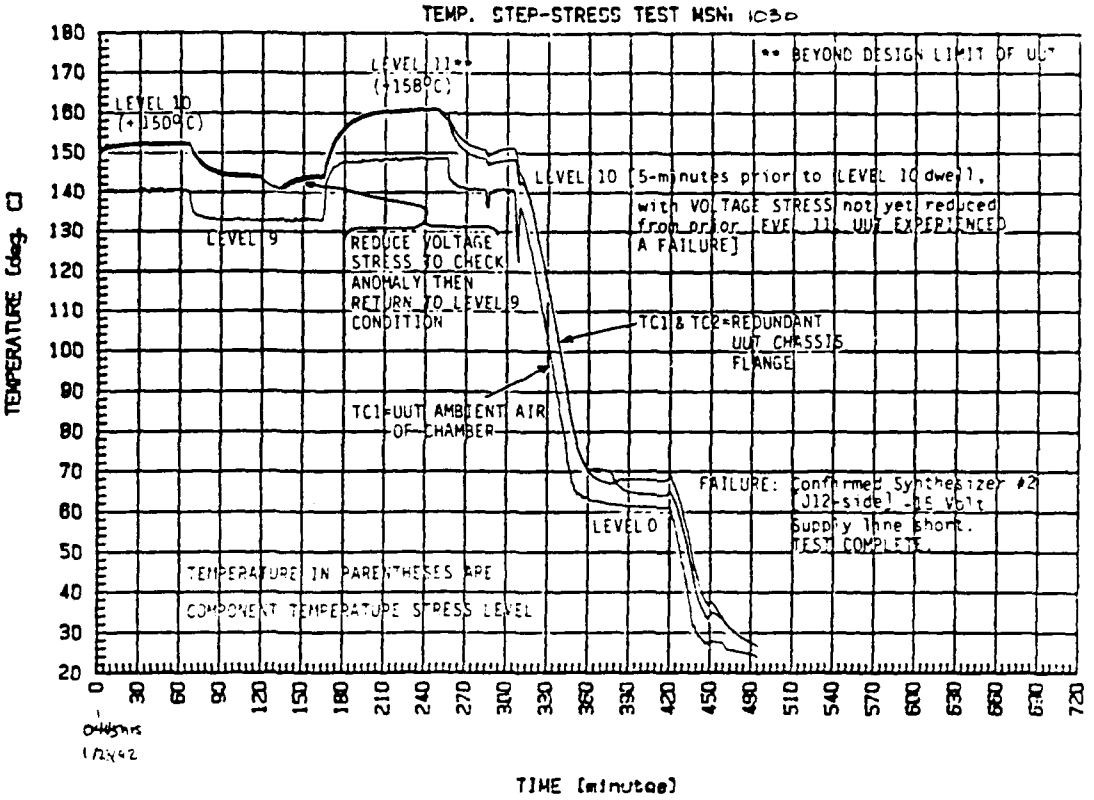
STEP-STRESS TEST MSN 1030 PLOT 1 OF 3
BEGIN TEST: 01/22/92



STEP-STRESS TEST MSN 1030 PLOT 2 OF 3
CONTINUE TEST: 01/22 & 01/23/92



* Plot terminated by error condition. Restart on #3
Plot missing ramp to LEVEL 10. Error condition with plotter.


TEMP. STEP-STRESS TEST MSN: 1030
** BEYOND DESIGN LIMIT OF UUT
LEVEL 11**
(+158°C)
LEVEL 10
(+150°C)
LEVEL 10 [5-minutes prior to LEVEL 10 dwell, with VOLTAGE STRESS not yet reduced from prior LEVEL 11. UUT EXPERIENCED A FAILURE]
LEVEL 9
REDUCE VOLTAGE STRESS TO CHECK ANOMALY THEN RETURN TO LEVEL 9 CONDITION
TC1 & TC2=REDUNDANT UUT CHASSIS FLANGE
TC1=UUT AMBIENT AIR OF CHAMBER
FAILURE: Confirmed Synthesizer #2 (J12-side) -15 volt supply line short. TEST COMPLETE.
LEVEL 0
TEMPERATURE IN PARENTHESES ARE COMPONENT TEMPERATURE STRESS LEVEL
TEMPERATURE (deg. C)
TIME (minutes)
0 30 60 90 120 150 180 210 240 270 300 330 360 390 420 450 480 510 540 570 600 630 660 690 720
180 170 160 150 140 130 120 110 100 90 80 70 60 50 40 30 20

ENGINEER'S TEST INSTRUCTION SHEET

ENGINEER: B. ARMSTRONG/S. MUELLER PHONE:

TYPE OF TEST: TEMP STRESS, DR&D
(Thermal Vacuum, Airflow, etc.)

CHARGE NO: W.A.:

PROGRAM NAME: TEST UNIT:

TEST PERSONNEL (Test Engineer, Technician, Program Support, etc.):

START DATE: 1-20-92 TESTING PERIOD:

INSTRUMENTATION AND EQUIPMENT NEEDED:

TEST PARAMETERS: MEASURE & STORE 2 TEMP. CHANNELS (CHMBR, UUT Chassis) THROUGH-OUT TEMP RANGE 61°C - 152°C. THIS TEST WILL BE PERFORMED ON (7) TERMA UUT'S.

SPECIAL INSTRUCTIONS:

Date: 1-20-92

Ancillary Test Equipment Used

Name/Description	Manufacturer	Model	Ident. No.	S/N	Calib. Due Date
DATA ACQUISITION UNIT	HP	3497A		H4284499	7/25/93
COMPUTER	HP	85B		H-A86429	N/A
PRINTER	HP	THINK JET		A08763	N/A
PLOTTER	HP	7470A		HS24478	N/A
CHMBR	THERMO-TRAN	SA		HB07307	9-2-92

Data Recorder BH

DRY-RUN

Test Data Date: 1-20-92

0800hrs: Setting up for "DRY-RUN" w/UUT USED EARLIER FOR DR&D (NOV-DEC'91)

1200 hrs: UUT instrumented (TC3, TC4) @ CHASSIS Location. TC's 1 & 2 ARE CHMBR AIR DIRECTLY ABOVE UUT ≈ 4in ABOVE UUT. Chmbr Thermal Program has been entered by B. Armstrong (written by B. Clark). Begin DRY-RUN ON "DUMMY" UUT

1400hrs: Started Prog 1 w/chamber already @ ≈30°C

1615hrs: Temp Set Pt @ 111°C. Has Successfully Transitioned from 102 to 111°C. Turning Chmbr off. Will let drift overnight and resume Dry Run #2, tomorrow.

"DRY-RUN PLOT"

Data Recorder:

DRY-RUN #2

Test Data Cont'd: Date: 1-21-92

AM: Working on "[redacted]06" plotting/printing program to print new heading on plot. ALSO INITIALIZING DATA TAPES, TWO PER UUT.

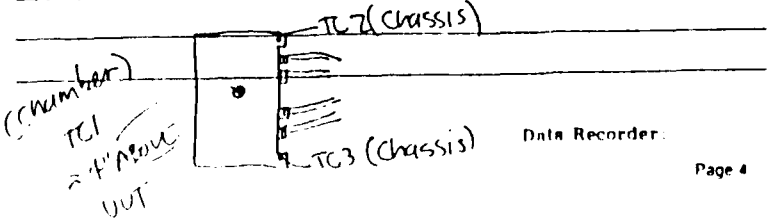
≈ 1000hrs TC4 Broke when snugged-down. Will use TC1 for Chmbr, TC2, TC3 for UUT CHASSIS Temp.

EHEZ'S INSTALLING UUT S/N 815 & Connecting cables, etc.

1130hrs UUT S/N 815 Not Working. ENGR REMOVES UUT to investigate. Possible SYNTHESIZER Prob's.

1300hrs: UUT S/N 1030 INSTALLED & CONNECTED S/N 1030 RUNS W/O INCIDENT

1330hrs. Thermal data logger program updates complete. Will use "HITCE1" W/ "[redacted]CE 2" AS back-up. Two data tapes/test are set-up for the Qual tests, which will commence tomorrow, 1-22-92 @ 700 hrs.



Data Recorder:

QUAL S/N 1030 START, P1

Test Data Cont'd: Date: 1-22-92

*0700hrs: Arrive in Lab. Check Set-up. Set-up OK. ALL TC's 25°C

0708hrs. START TRANSITION TO +61°C. PROG 1, INIT on CHAMBER (18min Ramp, 2hr Dwell) UUT Energized by [redacted] TECH, Printouts on 5min interval, Plotting on 1-min interval

0804hrs: TC1 = 60.4 TC3 = 67.7
TC2: 67.9; Temp's beginning to stabilize: Elec. Tech starting 61°C Testing. (UUT Power has been on for = 1hr)

0904hrs: Level 61°C Dwell. Ramp to +69°C Prog 2, ENTRY 2. Set Voltages to 5.2, 15.3v/c

0935hrs TC1: 68.5
TC2: 75.4
TC3: 76.3: UUT Chassis = stable, begin 69°C func'l testing

1004hrs: Complete 69°C Elec Test. Continue to dwell until = 1034hrs

1034hrs: Chmbr transitioning to +77°C, Prog 2, Entry 4

* ALL TIMES REF. W/R TO DATALOGGER CLOCK Setting near voltages

Data Recorder PA

Page 5

S/N 1030 P2

Test Data Cont'd: Date: 1-22-92

1044hrs- Tech (Cindy) have trouble getting any voltage greater than ±15.6 out of PS. He has left message w/ S. Mueller (@ home)

1105hrs- Upon conferring w/ S. Mueller over phone, a coarse adj. on 15V PS was located. Adjusting this knob allows the higher voltage levels to be reached. Elec tech starting tests.
TC1 = 76.3 TC2 = 84.3 TC3 = 84.7

1204hrs: Start transition to 85°C

1234hrs: Start Dwell (1hr)

1240: Start test
TC1 = 84.2 TC2 = 92.4 TC3 = 92.8

1304hrs: Loaded Printer w/ new paper, designate "P2"

1334hrs: Transition to 94°C

1405hrs: Start 94°C Elec Test.
TC1 = 92.9 TC2 = 101.5 TC3 = 101.9 °C

1504hrs: Start transition to +102.°C

1536hrs: Change Print paper, again (P3)

1536hrs: S Mueller starting test. TC1 = 100.7, TC2 = 109.7, TC3 = 110°C

Data Recorder: PA

Page 6

Test Data Cont'd: Date: 01-22-92

16:54 - HSN 1030 Decreased from LEVEL 6 after dwell back to LEVEL 4 to verify anomaly observed Synth #1 (J15). Manual control. Stabilize 30 min. Start test to Verify. END Dwell 17:22

17:22 - NO FAILURE FOUND LEVEL 4 RETEST. CONTINUE WITH LEVEL 6 +111°C (Program #2, Interval #12)

17:52 - START LEVEL 6 TESTS. Dwell will end at 18:52

18:34 - Begin reloading plot routine. Completed at 18:49.

18:49 - New plot begins. Still in LEVEL 6 dwell.

18:52 - Transition to LEVEL 7, +119°C Chamber setting. Anomaly w/ SYNTH #2 (J12). Completed Dwell 20:22

20:22 - Return to LEVEL 6 to CHECK, using manual CONTROL. Begin RETEST @ 20:52 SYNTH'S ONLY.

21:15 - NO FAILURE FOUND LEVEL 6 RETEST. CONTINUE TO LEVEL 8 +127°C CHAMBER SETTING (PROGRAM #2, INTERVAL #8)

22:45 - Return to LEVEL 7 to CHECK both SYNTHESIZERS & +15V SUPPLY CURRENT ANOMALIES. MANUAL CONTROL TO +119°C SETTING.

23:55 - Return to LEVEL 6 to clear up anomalies w/ SYNTHS Masked by STROBES @ LEVEL 7. Manually go to LEVEL 6, +111°C. NO FAILURE FOUND

01-23-92
01:10 - INCREASE STRESS LEVEL TO LEVEL 9 (FROM LEVEL 6 & 7 REVERTED) w/ PROGRAM #2, INTERVAL #18

02:40 - Reduce to LEVEL 8 to check Synth's STATUS (manually)

03:25 - At LEVEL 8, reduce Voltages to nominal to check STATUS. Return & incrementally. Synths are good. Re-stabilize at LEVEL 8 temp & voltage 04:20.

04:20 - Proceed to LEVEL 10 (Program #2, Interval #20).

Data Recorder

Test Data Cont'd: Date: 01/23/92

04:35 - Prior to this time plot ended in error. Last data printout @ 04:12.

04:45 - PLOT 3 begins. LEVEL 10 stabilization will be complete at 04:50. Missed all of transition on previous PLOT 2.

05:50 - Ramp back to LEVEL 9 TO VERIFY STATUS OF SYNTH'S. Also reduced voltages to nominal to observe affects. Need to re-stabilize 06:59.

07:30hrs - Ramp TO LEVEL 11, +151°C, ±7.2V, ±18.3V

≈ 08:00 hrs - TC1 = 148.3, TC2 = 159.8°C; Start Test

≈ 09:00 hrs Return to LEVEL 10

09:25 hrs 5min until dwell; -15VPS "shorts"; Record voltage/currents
09:47 hrs: End Level 10;
09:48 hrs GO TO LEVEL 0; PROG 2 INV'L 22, 40 min trans
10:58: Start +61°C Dwell; Perform tests
11:30 hrs: End test. -15V supply to synth. NO. 2 (J12) shorted
GO TO ROOM AMBIENT; USE Prog. 4

12:15 hrs: Opened chamber door
Visual inspection:
Upon cover removal, evidence substantially scorched conformal coat throughout module. Compartment A3 has numerous solder "balls" that formed during the test. These balls are on several of the IC pins and on some of the PCB etch.

Data Recorder SM/BA

HUGHES

HUGHES AIRCRAFT COMPANY

STEP-STRESS TROUBLE & FAILURE REPORT

1 PROJECT NAME

FAIL CLASS	TEST TYPE	TEST ENV	FAIL CAUSE	RELEV

FAM CODE

SYST CODE

NO. Z 7386

ORIGINATOR

2 THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE X FAILURE

3 SYSTEM SUBSYSTEM NAME	P N	S N	4 TIMER COUNTER READINGS	5 DATE	35 REFERENCES
T/R MODULE	Post number -1C3	1030	TIME 09:25 LEVEL ELAPSED 25:20 11 TO 10 HOURS CYCLES	01 23 92 MO DAY YR	

6 REPORTING FACILITY	7 REPORTED BY	ORG CODE	OPERATING LOG NO
STEP-STRESS TEST (C/L Tsukamoto)	S.D. Mueller S.D. Mueller 1/23/92	72,30	

8 TROUBLE/FAILURE OBSERVED WAS: (TEST CONDITIONS SYMPTOMS SEVERITY ETC INCLUDING "IS" AND "SHOULD BE" DATA)

TFR CONTINUATION USED ☐

-15V supply short A3 Synth (J12-side). Occured 25 minutes into decreasing ramp from Level 11 (+148°C Chamber air, +160°C Flange, ±7.2V, ±18.3V, +151°C Setpt) to Level 10 (+140.5°C Chamber air, +148.5°C Flange, +143°C Setpt, w/ voltages yet unchanged from Level 11) 5 minutes prior to stabilized dwell. -15 V total supply @ -2.23 Vdc, 3.44 A was 632 mA at Level 11. Initial visual: Solder balls on various component leads.

9 TROUBLE FAILURE OCCURRED DURING
(A) X ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE-FLIGHT OR CURSORY CHECK

10 ACTION TAKEN TO CORRECT TROUBLE FAILURE
(A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 - 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 - 29)

11 ITEM REPLACED NAME	P N	S N	12 ITEM INSTALLED NAME	P N	S N	13 DISPOSITION OF REPLACED ITEM

VERIFICATION

14 WERE OTHER TROUBLES FAILURES NOT RELATED TO ORIGINAL NOTED?
(A) ☐ NO (B) ☐ YES LIST ON NEW TFR - TFR NO _____

15 WAS REPORTED TROUBLE FAILURE VERIFIED?
(A) ☐ YES (B) ☐ NO (CHECK 16 B AND EXPLAIN)

16 FAILED ITEM NAME	P N	S N	REF DESIG	MANUFACTURER

17 NEXT HIGHER ASSY NAME	P N	S N	REF DESIG	MANUFACTURER

18 (A) ☐ REWORK REQUIRED IS (B) ☐ REWORK IS NOT REQUIRED BECAUSE

19 VENDOR REWORK ANALYSIS IS REQUIRED ☐
ITR _____ CAR _____

20 DISPOSITION OF ITEM IF NOT REWORKED

21 AUTHORIZATION BY ORG CODE DATE

REWORK & RETEST

22 LIST BELOW ALL PARTS REPLACED REPAIRED OR ADJUSTED

A CIRCUIT SYMBOL	B PART NUMBER	C S N	D MANUFACTURER	E DEFECT	F REWORK ACTION TAKEN	G RECEIVING INSP NO	H APPROVED PARTS YES	H APPROVED PARTS NO	PRI FAIL

DO NOT USE

23 OTHER REWORK ACTION

24 REWORKED BY	ORG CODE	25 RETESTED BY	ORG CODE	26 RETEST RESULTS APPROVAL	DATE

27 RETEST RESULTS REPAIRED ITEM IS ACCEPTABLE FOR
☐ UNRESTRICTED USE ☐ RESTRICTED USE ☐ NOT ACCEPTABLE (EXPLAIN IN BLOCK 30)

28 DISPOSITION OF ITEM AFTER RETEST

29 Q C

ENGINEERING

30 CAUSE OF FAILURE - COMMENTS (IF ANALYSIS NOT PERFORMED EXPLAIN)

31 BASIC CAUSE OF TROUBLE FAILURE (SELECT FROM BLOCK 1 ON REVERSE SIDE)

32 SIGNATURE ORG CODE DATE

33 CORRECTIVE ENGINEERING ACTION TAKEN (IF NONE JUSTIFY) - CONCLUSIONS

REF DOCUMENT IMPLEMENTING CORRECTIVE ACTION EO ECR ETC IS NO.

34 SIGNATURE ORG CODE DATE

11020 CS MAR 66

USE TFR CONTINUATION SHEET IF ADDITIONAL SPACE IS NEEDED

FOR RELIABILITY ANALYSIS AND FOLLOW-UP SEE REVERSE SIDE OF COPY 4

91/12

Z7386

1

STEP-STRESS TEST DATA NOTEBOOK

UNIT UNDER TEST: MSN 1023

TEST STATUS: NO FAILURES
(COMPLETED LEVEL 10)

TEST SUMMARY

STEP-STRESS		START DWELL	ANOMALY/ FAILURE	END DWELL
		6-Feb-92		
LEVEL	0	8:00		9:00
LEVEL	1	9:30		10:30
LEVEL	2	11:00		12:00
LEVEL	3	12:30		13:30
LEVEL	4	14:00		15:00
LEVEL	5	15:30		16:30
LEVEL	6	17:00		18:00
LEVEL	7	18:30		19:30
LEVEL	8	20:00		21:00
LEVEL	9	21:30	Anomaly	22:30
Retest	8	23:00		1:10
		6-Feb-92		7-Feb-92
LEVEL	10	1:40	Anomaly	2:40
Retest	9	3:10		3:30
FAILURE:			NONE	
Final Test	0	4:55		5:55
				7-Feb-92

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

Tester: (Name & rating/grade) 814-10 1557

STEP-STRESS Level (enter 0 - 10): 0

TURN UNIT ON at 07:10 (TIME) (Room Temp)

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

START PROGRAM # 1

Begin RAMP: 07:10 (TIME HR MIN)

START PROGRAM # 2

Start DWELL: 08:00 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 60.5 (°C) (Chamber thermocouple reading) set @ 61

Flange Temperature: 68.5 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 70 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: + 5 Volts dc: +5V (Vdc) - 5 Volts dc: -5 (Vdc)

+15 Volts dc: +15 (Vdc) -15 Volts dc: -15 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 08:0 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J5) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1246 (mA) - 5 Volts dc: 81 (mA)

+15 Volts dc: 112 (mA) -15 Volts dc: 196 (mA)

End TEST 08:01 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 08:01 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J5) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.12u/9.6u	47	4.12u/9.6u	48	2
	I > 0	4.8u/9.6u	50	4.72u/9.6u	49	
	I + Q > 0	4.72u/9.6u	49	4.72u/9.6u	49	
	Q > 0	4.8u/9.6u	50	4.92u/9.6u	47	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.96u/9.6u	47	4.96u/9.6u	47	
	I > 0	4.44u/9.6u	48	4.72u/9.6u	49	
	I + Q > 0	4.96u/9.6u	47	4.48u/9.6u	47	
	Q > 0	4.44u/9.6u	48	4.92u/9.6u	47	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72/9.44	49	4.72/9.44	49	
	I > 0	4.8/9.44	50	4.72/9.44	49	
	I + Q > 0	4.8/9.44	50		49	
	Q > 0	4.72/9.44	49	4.48/9.44	47	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.48/9.44	47	4.48/9.44	47	
	I > 0	4.72/9.44	49	4.72/9.44	49	
	I + Q > 0	4.48/9.44	47	4.48/9.44	47	
	Q > 0	4.64/9.44	48	4.48/9.44	47	

End TEST: 08:25 (TIME HR MIN)

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 08:25 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations
50 (MSB)	684	12.19	684	11.39	*Power measured after 15 sec thermal warm up hold
35 (MSB)	729	11.92	729	12.02	
18 (MSB)	825	11.5	825	11.4	
00 (MSB)	921	10.0	921	10.4	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check box)

End TEST: 08:40 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 09:00 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1023

Test Date: 2/6/92

Tester: (Name & stamp or initials)

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

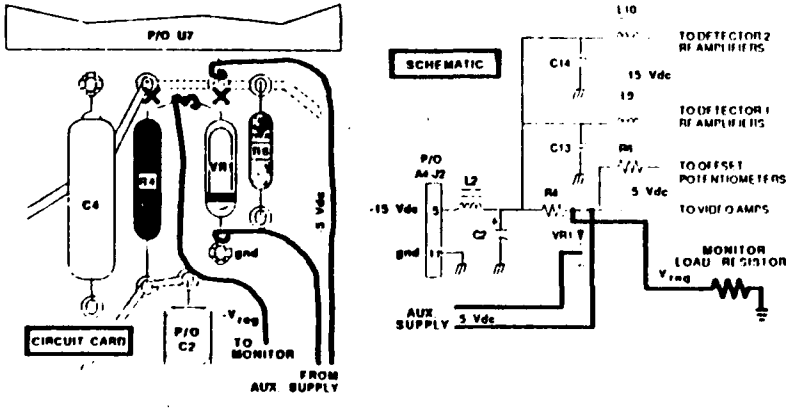
Start TEST: 08:40 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.08 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 09 41 (TIME HR MIN)

97

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND P4/VR1 MONITORING



2/6/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 4.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is .7 dBm @ 918.0 MHz (Spec=+9dBm mihimum).
Power at J5 is 1.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

Syn/Det # 1023
stress test 0
J5 output

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 12.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 717.9 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is .7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

2/6/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 6.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 5.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

Sunfest # 1030
Stress test 0
J12 output

FULL PRINT-OUT OF Power Output and Frequency [redacted]er. #

Power at J12 is 10.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.9 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 4 digits): 1023

Test Date: 2/6/92

Tester: (Name & stamp number)

STEP-STRESS Level (enter 0 - 10): 1

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 09 00 (TTUP HR MIN)

Start DWELL: 09 30 (TTUP HR MIN)

STEP-STRESS Level Chamber Air Temperature: 68.4 (°C) (Chamber thermocouple reading) 67.369

Flange Temperature: 76.1 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 78 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS During Temperature Ramp; Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: 5.2 (Vdc) -5 Volts dc: 5.2 (Vdc)

+15 Volts dc: 15.3 (Vdc) -15 Volts dc: -15.3 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 09 30 (TTUP HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 128.7 (mA) -5 Volts dc: 86 (mA)

+15 Volts dc: 112 (mA) -15 Volts dc: 50.4 (mA)

End TEST: 09 31 (TTUP HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 4 digits): 1023

Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with testing for Channels 50 at this STEP-STRESS Level.

Start TEST: 09 31 (TTUP HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Data	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	472 / 960	49	472 / 960	49	
	I > 0	480 / 960	50	"	"	
	I + Q > 0	472 / 960	49	"	"	
	Q > 0	480 / 960	50	448 / 960	448 / 960	
Other: Specify ___ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ___ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	448 / 960	47	448 / 960	47	
	I > Q	464 / 960	48	472 / 960	49	
	I + Q > 0	448 / 960	47	448 / 960	47	
	Q > 0	464 / 960	48	448 / 960	47	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter digits): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Lmsec T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Lmsec T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	472ns/96us	49	472ns/96us	47	
	I > 0	456ns/96us	50	"	"	
	I + Q > 0	456ns/96us	"	"	"	
	Q > 0	472ns/96us	49	448ns/96us	47	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	448ns/96us	47	448ns/96us	47	
	I > 0	472ns/96us	49	48/96us	50	
	I + Q > 0	448ns/96us	47	448ns/96us	47	
	Q > 0	464ns/96us	48	448ns/96us	47	

End TEST 04 52 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter digits): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 04 52 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *measured for cable losses
50 min	684	12.29	684	11.39	
35 min	729	11.52	729	11.62	
18 min	825	11.03	825	11.6	
00 min	921	10.6	921	11.6	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST 10 05 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

End DWELL 10 56 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1027 Test Date: 2/6/12

STEP-STRESS Level: 1 Tester:

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

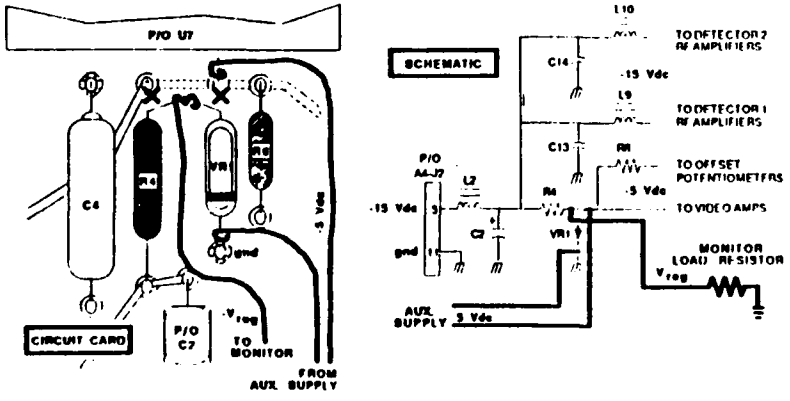
Start TEST: 10:05 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.09 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 10:06 (TIME HR MIN)

102

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



2/6/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 7.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is .4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

Synthet #1023
stress test 1

J5 output

103

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 11.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is .4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

2/6/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 7.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is less than 891.0 MHz which is below the specified frequency.
Power at J12 is 3.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

Sym/Det # 1023
Stress test 1
J12 output

104

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 735.9 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 4 digits): 1023

Test Date: 2/6/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 2

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 10:30 (TTMP HR MIN)

Start DWELL: 11:00 (TTMP HR MIN)

STEP-STRESS Level Chamber Air Temperature: 76.2 (°C) (Chamber thermocouple reading) Set @ 77

Flange Temperature: 94.3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 84 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: + 5.4 (Vdc) - 5 Volts dc: -5.4 (Vdc)

+15 Volts dc: + 15.6 (Vdc) -15 Volts dc: -15.6 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level

Start TEST: 11:00 (TTMP HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1329 (mA) - 5 Volts dc: 90 (mA)

+15 Volts dc: 113 (mA) -15 Volts dc: 514 (mA)

End TEST: 11:01 (TTMP HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 4 digits): 1023

Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -.75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 11:01 (TTMP HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -.75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	472ns / 960ns	49	472ns / 960ns	49	
	I > 0	480ns / 960ns	50	"	"	
	I + Q > 0	472ns / 960ns	49	"	"	
	Q > 0	"	"	448ns / 960ns	47	
Other: Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-.75 dBm	I > 0	448ns / 960ns	47	448ns / 960ns	47	
	I > 0	448ns / 960ns	47	472ns / 960ns	49	
	I + Q > 0	448ns / 960ns	47	448ns / 960ns	47	
	Q > 0	464ns / 960ns	48	448ns / 960ns	47	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Data	Detector 1 Latest T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Latest T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.44us/9.64us	46	4.44us/9.64us	46	
	I > 0	4.84us/9.64us	50	"	"	
	I + Q > 0	4.72us/9.64us	49	"	"	
	Q > 0	"	"	4.44us/9.64us	46	
Other Specify ___ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify ___ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.84us/9.64us	47	4.84us/9.64us	47	
	I > 0	4.72us/9.64us	49	4.84us/9.64us	50	
	I + Q > 0	4.44us/9.64us	47	4.44us/9.64us	47	
	Q > 0	4.84us/9.64us	47	"	"	

End TEST: 11:22 (HH:MM MN/AM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 11:27 (HH:MM MN/AM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measured for cable losses
50 min	684	12.1	684	11.1	± 0.4 dB w/ 4A > 9dB
35 min	729	11.7	729	11.7	
18 min	825	10.9	825	10.9	
00 min	921	*8.6	921	9.4	

Additional Testing (OPTIONAL); RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 11:35 (HH:MM MN/AM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 12:00 (HH:MM MN/AM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 2/6/92

STEP-STRESS Level: 2 Tester:

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

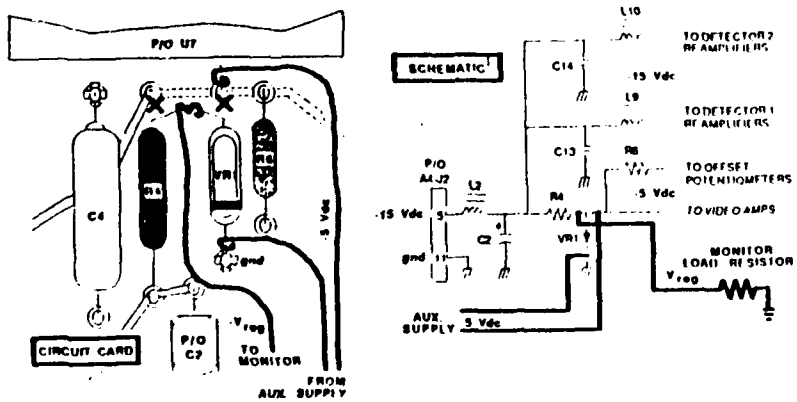
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 1:35 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.11 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 11:36 (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



2/6/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 6.5 dBm @ 687.0 MHz (Spec=+9dBm minimum). Syn 1108 # 1023

Power at J5 is 5.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).

Frequency is greater than .0 MHz which is above the specified frequency.

Power at J5 is 3.8 dBm @ 693.0 MHz (Spec=+9dBm minimum). Stress test 2

Frequency is less than .0 MHz which is below the specified frequency.

Power at J5 is 4.1 dBm @ 696.0 MHz (Spec=+9dBm minimum). J5 output

Frequency is less than .0 MHz which is below the specified frequency.

Power at J5 is 3.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).

Power at J5 is 1.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).

Frequency is greater than .0 MHz which is above the specified frequency.

Power at J5 is 8.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.5 dBm @ 732.0 MHz (Spec=+9dBm minimum).

Power at J5 is 8.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).

Power at J5 is 8.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).

Power at J5 is 3.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).

Power at J5 is 2.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).

Power at J5 is-2.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.4 dBm @ 834.0 MHz (Spec=+9dBm minimum).

Power at J5 is 5.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).

Power at J5 is 8.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).

Power at J5 is .6 dBm @ 903.0 MHz (Spec=+9dBm minimum).

Power at J5 is .6 dBm @ 906.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Power at J5 is 5.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).

Power at J5 is-3.1 dBm @ 921.0 MHz (Spec=+9dBm minimum).

Frequency is less than .0 MHz which is below the specified frequency.

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 11.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).

Power at J5 is 5.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).

Power at J5 is 3.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).

Power at J5 is 4.1 dBm @ 696.0 MHz (Spec=+9dBm minimum).

Power at J5 is 3.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).

Power at J5 is 10.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).

Power at J5 is 1.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).

Power at J5 is 8.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).

Power at J5 is 10.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.5 dBm @ 732.0 MHz (Spec=+9dBm minimum).

Power at J5 is 11.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.2 dBm @ 738.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).

Power at J5 is 8.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).

Power at J5 is 8.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).

Power at J5 is 3.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).

Power at J5 is 10.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).

Power at J5 is 10.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).

Power at J5 is 2.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).

Power at J5 is 9.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).

Power at J5 is-2.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.4 dBm @ 834.0 MHz (Spec=+9dBm minimum).

Power at J5 is 5.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).

Power at J5 is 8.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).

Power at J5 is .6 dBm @ 903.0 MHz (Spec=+9dBm minimum).

Power at J5 is .6 dBm @ 906.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).

Power at J5 is 7.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).

Power at J5 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Power at J5 is 5.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).

Power at J5 is-3.1 dBm @ 921.0 MHz (Spec=+9dBm minimum).

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Power at J5 is 3.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 3.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 3.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-1.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
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Power at J5 is 10.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 2/6/92

Tester:

STEP-STRESS Level: 3

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 12:00 (TIME HR MIN) Start DWELL: 12:30 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 84 (°C) Flange Temperature: 92.5 (°C)
(Chamber thermocouple reading) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 84.55 (°C)
(refer to Appendix D Table)

VOLTAGE STEP-STRESS During Temperature Ramp; Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: 15.6 (Vdc) -5 Volts dc: -5.6 (Vdc)

+15 Volts dc: +15.9 (Vdc) -15 Volts dc: -15.9 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 12:34 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 136.5 (mA) -5 Volts dc: 91 (mA)

+15 Volts dc: 116 (mA) -15 Volts dc: 52.5 (mA)

End TEST: 12:35 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1023 Test Date: 2/6/92

STEP-STRESS Level: 3

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -.75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level

Start TEST: 12:35 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -.75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72us/9.6us	49	4.72us/9.6us	49	
	Q > 0	4.8us/9.6us	50	"	"	
	I + Q > 0	4.72us/9.6us	49	"	"	
	Q > 0	"	"	4.8us/9.6us	50	
Other Specify (dBm)	I > 0					
	Q > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	Q > 0					
	I + Q > 0					
	Q > 0					
-.75 dBm	I > 0	4.8us/9.6us	97	4.8us/9.6us	47	
	Q > 0	4.72us/9.6us	99	4.8us/9.6us	50	
	I + Q > 0	4.48us/9.6us	47	4.48us/9.6us	47	
	Q > 0	4.64us/9.6us	48	4.48us/9.6us	47	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter 4 DIGIT): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72µs/9.6µs	99	4.72µs/9.6µs	49	
	I > 0	4.72µs/9.6µs	50	"	"	
	I + Q > 0	4.72µs/9.6µs	49	"	"	
	Q > 0	"	"	4.95µs/	47	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.8µs/9.6µs	47	4.8µs/9.6µs	47	
	I > 0	4.72µs/9.6µs	49	4.8µs/9.6µs	50	
	I + Q > 0	4.8µs/9.6µs	47	4.8µs/9.6µs	47	
	Q > 0	4.8µs/9.6µs	48	4.8µs/9.6µs	47	

End TEST: 12 55 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter 4 DIGIT): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer 1 Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 12 55 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *assumes for cable losses
50 min	684	12.1	684	11.1	✓ Pwr. >9dBm
35 min	727	11.3	729	10.92	
18 min	825	10.3	825	10.4	
00 min	921	8.2	921	9.8	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 13 10 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 13 30 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023

Test Date: 2/6/92

Tester:

STEP-STRESS Level: 3

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

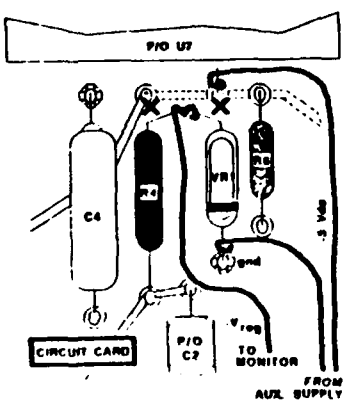
RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

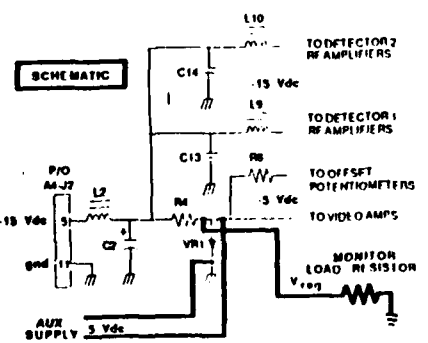
Start TEST: 13:10 (HR MIN)

Voltage across LOAD RESISTOR: -5.26 (Vdc) (nominally -5 Vdc)

End TEST: 13 11 (HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





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2/6/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

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Power at J5 is 6.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is .0 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 8.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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Syn/Ref #1023 stress test 3
J5 output

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 11.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is .0 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

2/6/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 4.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 3.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is less than 696.0 MHz which is below the specified frequency.
Power at J12 is 4.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 909.0 MHz which is above the specified frequency.
Power at J12 is-1.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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sym/det #1023

stress test 3

J12 output

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 10.2 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

Tester (Name & ramp below)

STEP-STRESS Level (enter 0 - 10): 4 DM

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 13:30 (HHMM HR MIN)

Start DWELL: 14 00 (HHMM HR MIN)

STEP-STRESS Level Chamber Air Temperature: 92.6 (°C) (Chamber thermocouple reading) +2 / 44

Flange Temperature: 101.6 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 102 (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +5.8 (Vdc) -5 Volts dc: -5.8 (Vdc)

+15 Volts dc: +16.2 (Vdc) -15 Volts dc: -16.2 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 14:00 (HHMM HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J3) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1404 (mA) -5 Volts dc 93 (mA)

+15 Volts dc: 118 (mA) -15 Volts dc 535 (mA)

End TEST: 14 01 (HHMM HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or 100 at this STEP-STRESS Level.

Start TEST: 14 01 (HHMM HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J3) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L(usec) T(usec)	Detector 1 Duty Cycle (percent)	Detector 2 L(usec) T(usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	47us/96us	49	47us/96us	49	
	I > 0	48us/96us	50	"	"	
	I + Q > 0	47us/96us	49	"	"	
	Q > 0	"	"	46us/96us	47	
Other: Specify	I > 0	46us/96us	48			
	I > 0					
12 (dBm)	I + Q > 0					
	Q > 0					
Other: Specify	I > 0					
	I > 0					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	✗ 00154		48us/96us	97	✓
	I > 0	47us/96us	49	48us/96us	50	
	I + Q > 0	48us/96us	47	48us/96us	47	
	Q > 0	46us/96us	48	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L (msec) T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 L (msec) T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	472u/964u	49	472u/964u	49	
	I > 0	482u/964u	50	"	"	
	I + Q > 0	472u/964u	48	"	"	
	Q > 0	"	"	498u/964u	47	
Other Specify 72 (dBm)	I > 0	449u/964u	47			
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	noisy		498u/964u	47	
	I > 0	472u/964u	49	484u/964u	50	
	I + Q > 0	498u/964u	47	464u/964u	47	
	Q > 0	"	"	"	"	

End TEST 14:15 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 2/6/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 14:15 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *minimum for cable losses
50 min	684	11.8	684	10.9	* Pwr is ≥ 9dBm
35 min	729	10.9	729	9.72	
18 min	825	9.6	825	10	
00 min	921	8.6	924	7.7	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT N/A (Check here)

End TEST: 14:40 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

End DWELL 15:00 (TIME HR MIN)

STEP STRESS LEVEL COMPLETE

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SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 2/6/9-

STEP-STRESS Level: 4 Tester:

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

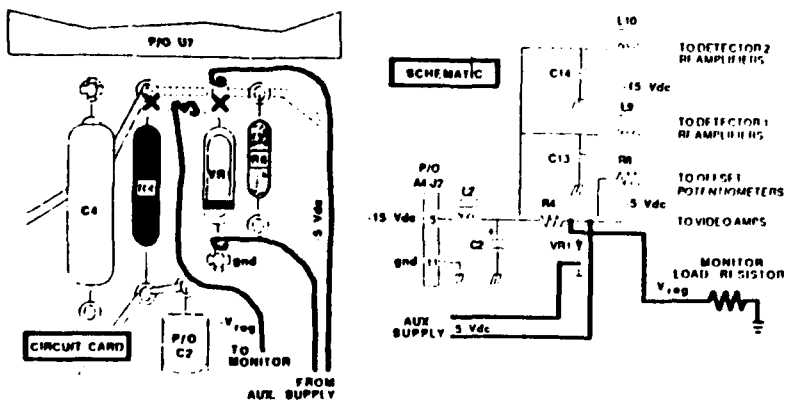
Start TEST: 14'40 (THUF HR MIN)

Voltage across LOAD RESISTOR: -5.14 (Vdc) (Refer to Appendix D, nominally -5 Vdc)

End TEST: 14 41 (THUF HR MIN)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



2/6/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

synthet #1023
stress test 4
J5 output

****

Power at J5 is-.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-7.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 3.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is-7.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 8.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is-7.5 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 3.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-8.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 11.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-7.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is-7.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is-7.5 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is-8.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

2/6/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Syn Ref # 1023
stress test 4
J12 output

****

Power at J12 is 6.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 687.0 MHz which is above the specified frequency.
Power at J12 is 2.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 3.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 693.0 MHz which is above the specified frequency.
Power at J12 is 3.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 699.0 MHz which is above the specified frequency.
Power at J12 is-3.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 703.0 MHz (Spec=+9dBm minimum).
Power at J12 is-10.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 714.0 MHz which is above the specified frequency.
Power at J12 is 8.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 753.0 MHz which is above the specified frequency.
Power at J12 is 5.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 765.0 MHz which is above the specified frequency.
Power at J12 is 7.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.7 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Frequency is less than 825.0 MHz which is below the specified frequency.
Power at J12 is 3.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is less than 831.0 MHz which is below the specified frequency.
Power at J12 is 7.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 834.0 MHz which is above the specified frequency.
Power at J12 is 6.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 909.0 MHz which is above the specified frequency.
Power at J12 is 1.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 10.5 dBm @ 634.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 637.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 703.0 MHz (Spec=+9dBm minimum).
Power at J12 is-10.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 725.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.7 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 4 digit): 1023

Test Date: 02/06/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 5

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 15:00 (HR:MIN)

Start DWELL: 15:30 (HR:MIN)

STEP-STRESS Level Chamber Air Temperature: +100.4 (°C) (Chamber thermocouple reading) Set @ +102

Flange Temperature: +110.0 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +110 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.00 (Vdc) -5 Volts dc: -6.00 (Vdc)

+15 Volts dc: +16.50 (Vdc) -15 Volts dc: -16.50 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.112 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 15:32 (HR:MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1443 (mA) -5 Volts dc: 966 (mA)

+15 Volts dc: 121.5 (mA) -15 Volts dc: 543.3 (mA) Checks okay

End TEST: 15:34 (HR:MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 4 digit): 1023

Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 15:35 (HR:MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (min) / T (min)	Detector 1 Duty Cycle (percent)	Detector 2 t (min) / T (min)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.64/9.60	48	4.64/9.60	48	
	I > Q	4.80/9.60	50	4.72/9.60	49	t / T
	I + Q > 0	4.72/9.60	49	4.64/9.60	48	
	Q > 0	11	49	4.48/9.60	47	
Other: Specify -72 (dBm)	I > 0	4.48/9.60	47			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Noise/9.60	See Above	4.48/9.60	47	
	I > Q	4.80/9.60	50	4.72/9.60	49	
	I + Q > 0	4.64/9.60	48	4.48/9.60	47	
	Q > 0	4.48/9.60	47	4.32/9.60	45	

TEST Continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1023 Test Date: 02/06/92

STEP-STRESS Level: 5

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Lmax T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Lmax T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	472/9.60	49	480/9.60	50	
	I > Q	480/9.60	50	"	50	
	I + Q > 0	464/9.60	48	"	50	
	Q > 0	"	48	464/9.60	48	
Other Specify -72 (dBm)	I > 0	448/9.60	47			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	NOISE SEE ABOVE		464/9.60	48	
	I > Q	480/9.60	50	480/9.60	50	
	I + Q > 0	464/9.60	48	448/9.60	47	
	Q > 0	448/9.60	47	461/9.60	48	

End TEST: 15:58 (TIME HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1023 Test Date: 02/06/92

STEP-STRESS Level: 5

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at the STEP-STRESS Level.

Start TEST: 16:03 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations
50 min, MID	447	+4.6	684	+8.0	* Use correcting from Cal sheet 02/6/92 & freq indicated by data. * Increase for cable losses
35 mm, MID	692	+11.2	729	+10.4	J5 synth pulled off freq & nearly unlocked. Gone as is unless ... to Cin Sam being pushed by No outputs on frequency
18 mm, MID	715	+10.6	825	+8.5	
00 mm, MID	949 off freq & unlocked	+7.4 indeterminate	921	+10.6	BEHAVIORS ARE TYPICAL NO FAILURES

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level, Tester Name & Date. ATTACHMENT ✓ (Part Level) SIZ ONLY

End TEST: 16:28 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

CONTINUE TO LEVEL 6 End DWELL: 16:30 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number (enter MSN): 1023

Test Date: 02/06/92

Tester (Name & stamp below): A.D. Mueller

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

RESISTOR/ZENER DIODE MODIFICATION: At Dwell, For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

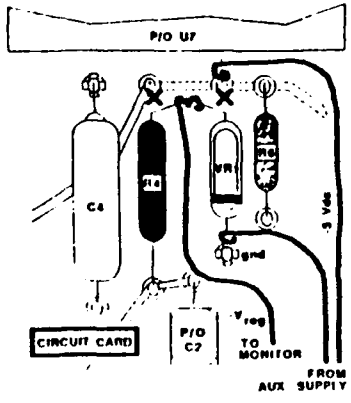
Start TEST: 15:34 (TIME HR MIN)

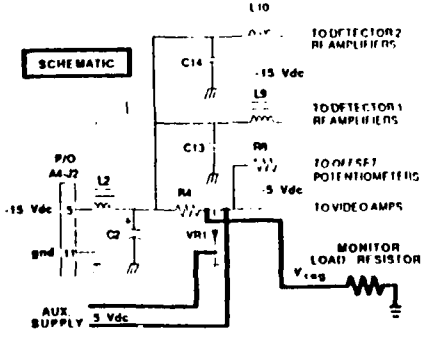
Voltage across LOAD RESISTOR: -5.156 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 15:34 (TIME HR MIN)

Cond Card Sample Removed
Still Units Unoperational by steps
(Number axis) 1Day

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





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FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 2.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than 711.0 MHz which is below the specified frequency.
Power at J12 is 5.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 732.0 MHz which is above the specified frequency.
Power at J12 is 7.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 765.0 MHz which is above the specified frequency.
Power at J12 is-5.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 828.0 MHz which is above the specified frequency.
Power at J12 is 2.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 834.0 MHz which is above the specified frequency.
Power at J12 is 4.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 885.0 MHz which is above the specified frequency.
Power at J12 is-1.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is less than 888.0 MHz which is below the specified frequency.
Power at J12 is 4.8 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 894.0 MHz which is above the specified frequency.
Power at J12 is-8.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 897.0 MHz which is above the specified frequency.
Power at J12 is 2.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 909.0 MHz which is above the specified frequency.
Power at J12 is 3.7 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is less than 912.0 MHz which is below the specified frequency.
Power at J12 is 2.1 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is less than 915.0 MHz which is below the specified frequency.
Power at J12 is-2.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is less than 918.0 MHz which is below the specified frequency.

MSN 1023 02/06/92
LEVEL 5

J12 SYNTH 2
16 26

SSG 92466 TEST

J12

Power at J12 is 6.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 2.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-8.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

MSN 1023
02/06/92
J12 LEVEL 5

SSG 92466 TEST

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter NSN): 1023 Test Date: 02/06/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 6

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 16:30 (TIME HR MIN) Start DWELL: 17:00 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +109.2 (°C) (Chamber thermocouple reading) Set @ +111

Flange Temperature: +119.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +118 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increase Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +6.20 (Vdc) -5 Volts dc: -6.20 (Vdc)

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.112 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level

Start TEST: 17:02 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz, Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1478 (mA) -5 Volts dc: 988 (mA)

+15 Volts dc: 135.0 (mA) -15 Volts dc: 5569 (mA)

End TEST: 17:03 (TIME HR MIN)

TEST continued next page

12.1

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter NSN): 1023 Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level

Start TEST: 17:03 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 I (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 I (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	464/960	48	464/960	48	
	I > Q	"	"	"	48	
	I + Q > 0	448/960	47	"	48	
	Q > 0	"	47	"	48	
Other: Specify -72 (dBm)	I > 0	448/960	47			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	448/960	47	416/960	43	
	I > Q	448/960	47	464/960	48	
	I + Q > 0	448/960	47	432/960	45	
	Q > 0	448/960	46	"	45	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.64 ~~4.72~~/9.60 SDM	48	4.56/9.60	50	
	I > Q	4.80/9.60	50	"	50	
	I + Q > 0	4.72/9.60	49	4.72/9.60	49	
	Q > 0	4.64/9.60	48	4.56/9.60	48	
Other Specify -72 (dBm)	I > 0	4.4/9.60	46			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify -72 (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0			4.48/9.60	47	
-75 dBm	I > 0	Noisy Spectrum		4.32/9.60	45	
	I > Q	4.80/9.60	50	4.48/9.60	47	
	I + Q > 0	4.48/9.60	47	4.40/9.60	46	
	Q > 0	"	47	4.16/9.60	43 Spectrum	

End TEST: 17:16 (HH:MM:SS AM)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell, Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 17:16 (HH:MM:SS AM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	# Use exit sheet if more room needed Observations
					*account for cable losses
50 (HEX)	644	+4.9 Locked	635	-2.41	J5 & J12 behaving similarly. CH 50 freq is out of bandwidth of VCO & filter, therefore Low in power.
35 (HEX)	689	+12.2	682	+10.6	
18 (HEX)	770	+11.8	764	+12.7	
00 (HEX)	844	+10.4	846	+11.6	Each CH does lock up; no longer trying to unlock.

↑ Δ off frequency ↑

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

NO FAULT

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Enter None)

OFF FREQUENCY

End TEST: 17:37 (HH:MM:SS AM)

Reload plotter now before end of dwell @ 17:39
Next plot begins at 17:57 with end of Level 7 dwell SDM

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP STRESS Level

CONTINUE TO LEVEL 7 End DWELL: 18:00 (HH:MM:SS AM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter unit #): 1023 — Test Date: 02/06/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 17:03 (TEMP HR MIN)

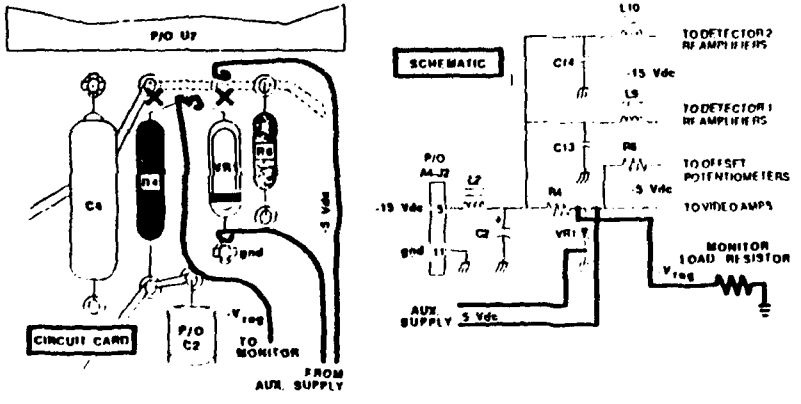
Voltage across LOAD RESISTOR: -5.173 (Vdc) (refer to Appendix D, nominally -5 Vdc)

End TEST: 17:03 (TEMP HR MIN)

Confidence Sample.
Okay @ Hot Chamber
air temp 02/06/92

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/06/92

Tester: (Name & ramp tested)

STEP-STRESS Level (enter 0 - 10): 7

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 18:00 (HR MIN) Start DWELL: 18:30 (HR MIN)

STEP-STRESS Level Chamber Air Temperature: +117.0 (°C) (Chamber thermocouple reading) Set @ +119

Flange Temperature: +127.3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +126 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp, Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +6.40 (Vdc) -5 Volts dc: -6.40 (Vdc)

+15 Volts dc: +17.10 (Vdc) -15 Volts dc: -17.10 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.112 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 18:31 (HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz, Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1507 (mA) -5 Volts dc: 86.2 (mA) decreasing (like all NSN 103c not current limited @ 5 volts)

+15 Volts dc: 124.7 (mA) decreasing -15 Volts dc: 566.3 (mA)

End TEST: 18:33 (HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 18:33 (HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz, Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 (Level) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 (Level) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	472/960	49	480/960	50	
	I > 0	"	49	464/960	48	
	I + Q > 0	"	49	472/960	49	
	Q > 0	464/960	48	480/960	45	
Other Specify -72 (dBm)	I > 0	448/960	47			
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0			432/960	45	
	I > 0			464/960	48	
	I + Q > 0			448/960	47	
	Q > 0			"	47	
-75 dBm	I > 0	416/960	43	416/960	43	
	I > 0	472/960	49	464/960	48	
	I + Q > 0	"	49	416/960	43	
	Q > 0	448/960	47	432/960	45	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number (enter MSN): 1023 Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q -Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72/9.60	49	4.64/9.60	48	
	I > Q	4.80/9.60	50	4.72/9.60	49	
	I + Q > 0	"	50	"	49	
	Q > 0	4.72/9.60	49	4.48/9.60	47	
Other: Specify -72 (dBm)	I > 0	4.48/9.60	47			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify -72 (dBm)	I > 0			4.32/9.60	45	
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.88/9.60 Same as above	43	4.16/9.60	43	
	I > Q	4.80/9.60	50	5.04/9.60	52	
	I + Q > 0	4.48/9.60	47	4.32/9.60	45	
	Q > 0	"	47	4.56/9.60	45	

End TEST 18:46 (HH:MM MM/DD/YY)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number (enter MSN): 1023 Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 18:50 (HH:MM MM/DD/YY)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *Amount for cable losses
50 min	642	+4.0	631	-4.6	J5 & J12 Synth Lock on freq when hopping. Power is still good
35 min	686	+12.0	676	+9.8	
18 min	765	+11.9	754	+12.5	Same behavior as Level 6
00 min	836	+10.0	831	+11.5	Need to check on power output which is still good

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 19:20 (HH:MM MM/DD/YY)

No Difference or Failure Found

OFF FREQ FOR 15 MHz STEP AT fc

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

Continue on to Level 8 End DWELL 19:30 (HH:MM MM/DD/YY)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 02/06/92

Tester: [signature]

STEP-STRESS Level: 7

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

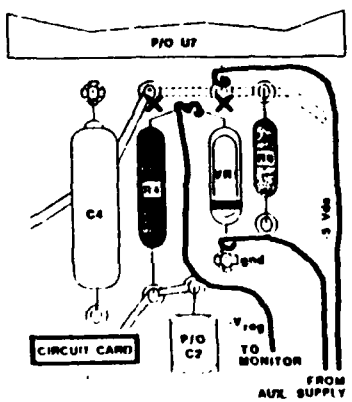
Start TEST: 18:46

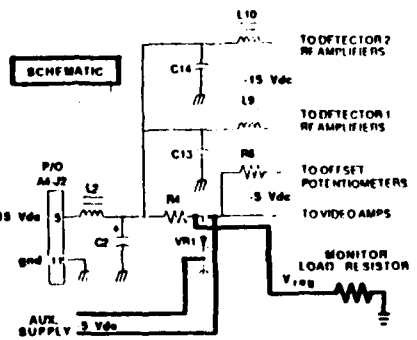
Voltage across LOAD RESISTOR: -5.189 (Vdc)

End TEST: 18:46

Conf Cent board sample
is okay JDM
Chamber smoke now.

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





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STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 02/06/92

Tester: [signature] (ESS 92466)

STEP-STRESS Level: 8

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 19:30 (HH:MM MIN) Start DWELL: 20 00 (HH:MM MIN)

STEP-STRESS Level Chamber Air Temperature: +124.8 (°C) (Chamber thermocouple reading) Flange Temperature: +135.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +134 (°C) (refer to Appendix D Table)

Set +127

VOLTAGE STEP-STRESS During Temperature Ramp, Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: -6.60 (Vdc)

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: -17.40 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.112 (Vdc)

Shift in signal output at beginning of ramp

At beginning of dwell

Next time - drift

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level

Start TEST: 20:01 (HH:MM MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1577 (mA) -5 Volts dc: 85.5 (mA) decreasing

+15 Volts dc: 116.5 (mA) decreasing -15 Volts dc: 57.3 (mA)

End TEST: 20:06 (HH:MM MIN)

Air Supplied and Running

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1023 Test Date: 02/06/92

STEP-STRESS Level: 8 (ESS 92466) [signature]

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (D/T) for each UUT Digital Output. Repeat with settings for Channels 50 at this STEP STRESS Level

Start TEST: 20 08 (HH:MM MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 (Lower) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 (Upper) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	472/960	49	488/960	50	
	I > 0	"	49	472/960	49	
	I + Q > 0	480/960	50	"	49	
	Q > 0	480/960	50	"	49	
Other Specify -70 (dBm)	I > 0	448/960	47	Noisy @ -72 dBm also		
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Noisy		464/960	48	
	I > 0	448/960	47	512/960	53	
	I + Q > 0	"	47	464/960	48	
	Q > 0	"	47	448/960	47	

LOFL

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number: 1023 Test Date: 02/06/92

STEP-STRESS Level: 8

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST. Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 604 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Data	Detector 1 Limit T (sec)	Detector 1 Duty Cycle (percent)	Detector 2 T (sec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.64/9.60	48	4.64/9.60	48	
	I > 0	4.60/9.60	50	"	48	
	I > 0 > 0	4.72/9.60	49	"	48	
	Q > 0	4.64/9.60	48	"	48	
Other Specify -70 (dBm)	I > 0	4.32/9.60	45			
	I > 0 > 0	4.80/9.60	50	Sample		
	Q > 0					
Other Specify -72 (dBm)	I > 0			4.16/9.60	43	@ -70 is 4.32/9.60 45%
	I > 0			4.96/9.60	52	
	I > 0 > 0			4.16/9.60	43	SAME @ -70 is 4.32/9.60 45%
	Q > 0			4.32/9.60	45	
-75 dBm	I > 0	Noisy SEE ABOVE		4.16/9.60	42	SEE ABOVE
	I > 0	4.80/9.60	50	4.96/9.60	52	SEE ABOVE
	I > 0 > 0	"	50	4.16/9.60	43	
	Q > 0	4.64/9.60	48	4.16/9.60	43	

End TEST 20:23 (HOUR MIN UNIT)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number: 1023 Test Date: 02/06/92

STEP-STRESS Level: 8

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST. At Dwell, Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST 20:23 (HOUR MIN UNIT) ✓ = 2nd run

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measured for cable losses
50 min	638	+11.9 /59	625	+8.3	Both synths lock on a frequency & track but drift in freq.
35 min (37)	692	+11.7 51	678	+9.8	
18 min 10	755	+11.4 86	739	+12.0	Both synths lock accurately at MHz & track.
00 min 100	821	+10.0 117	804	+11.4	CH32 735 J12 observed is 5 MHz

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell, Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check None)

Use freq Sweep test #2 to evaluate bandwidth

Compared Levels 5, 6, 7, 8 Both Synths

End TEST 20:57 (HOUR MIN UNIT)

NO ANOMALY SEEN

SYNTHS SEEM TO BE CHANGING PROPORTIONALLY FROM LEVEL TO LEVEL POWER OUTPUT IS PREDICTABLE.

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

CONTINUE ON TO LEVEL 9 End DWELL 21:00 (HOUR MIN UNIT)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 02/06/92

STEP-STRESS Level: 8 Tester: [signature]

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

RESISTOR/ZENER DIODE MODIFICATION At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 20:07 (hour min sec)

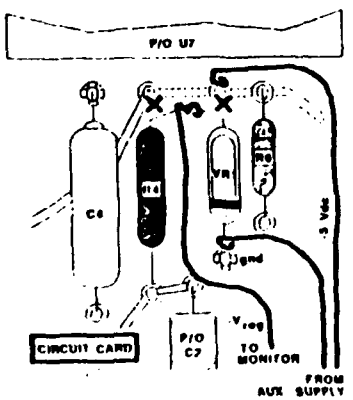
Voltage across LOAD RESISTOR: -5.202 (Vdc) (refer to Appendix D; nominally -5 Vdc)

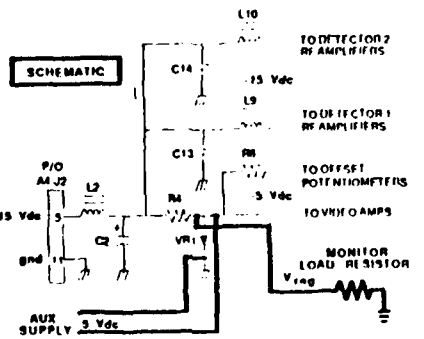
End TEST: 20:07 (hour min sec)

Comp/Cont Sample
Lock's clean still
(end of dwell
21:00

132

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 4 digits): 1023 Test Date: 02/06/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 9

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 21:00 (HHMM HR MIN) Start DWELL: 21:30 (HHMM HR MIN)

STEP-STRESS Level Chamber Air Temperature: +132.3 (°C) (Chamber thermocouple reading) Soak +135

Flange Temperature: +143.3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +142 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: + 5 Volts dc: +6.80 (Vdc) - 5 Volts dc: -6.80 (Vdc)

+15 Volts dc: +17.70 (Vdc) -15 Volts dc: -17.70 (Vdc)

Ave. Constant - 5 Volts dc Setting: -5.112 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 21:45 (HHMM HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 164.7 (mA) - 5 Volts dc: 94.7 (mA) increased

+15 Volts dc: 109.0 (mA) -15 Volts dc: 58.70 (mA)

End TEST: 21:48 (HHMM HR MIN) observations

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter 4 digits): 1023 Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 21:50 (HHMM HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	448/960	47	448/960	47	
	I > 0	464/960	48	464/960	48	
	I + Q > 0	448/960	47	448/960	47	
	Q > 0	"	47	464/960	48	
Other Specify -70 (dBm)	I > 0	432/960	45	-72 Same		
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify -72 (dBm)	I > 0		-72	432/960	45	
	I > 0					
	I + Q > 0	42%	-65 dBm	448/960	47	
	Q > 0			432/960	45	
-75 dBm	I > 0	NOISY		480/960	42	
	I > 0	448/960	47	456/960	52	
	I + Q > 0	"	47	480/960	42	-72, -70 & -65 dBm
	Q > 0	"	47	416/960	43	

TEST Continued next page

Chamber on @ 22:00 and running temp for 2 minutes

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 9

ESS 92466

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Data	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.48/9.6c	47	4.48/9.6c	47	
	I > Q	4.64/9.6c	48	4.64/9.6c	48	
	I + Q > 0	4.48/9.6c	47	4.48/9.6c	47	
	Q > 0	"	47	"	47	
Other Specify (dBm)	I > 0	-68 (4.14/9.6c	43%	Noisy, but Gets @ -72, -70 compared to -75 dBm		
	I > Q	-72 4.94/9.6c	52%			
	I + Q > 0	-72 3.84/9.6c	40%	4.04/9.6c 42% @ -70; 4.32/9.6c 45% @ -65		
	Q > 0	-70 4.16/9.6c	43%			
Other Specify (dBm)	I > 0	-72	4.0c/9.6c	42	Same @ -70	
	I > Q	-72, -70	4.8c/9.6c	50		
	I + Q > 0					
	Q > 0	-70, -72	4.0c/9.6c	42	4.56/9.6c 43% @ -65 dBm	
-75 dBm	I > 0	VERY NOISY		VERY NOISY		
	I > Q	NOISY		Looks like 50%		
	I + Q > 0	NOISY		NOISY		
	Q > 0	NOISY		NOISY		

End TEST: 22:11 (HHMP MM SS)

TEST continued next page

13 pages

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/06/92

STEP-STRESS Level (enter 0 - 10): 9

ESS 92466

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18 and 00 at this STEP-STRESS Level.

Start TEST: 22:11 (HHMP MM SS)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*account for cable losses)
50	632	-1.3	616	-15.0	
35	671	+10.7	651	-13.5	
18	738	+11.3	707	+10.4	
00	794	+9.9	750	+10.9	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO

End TEST: Question unlock & bi-modal (2 times) @ 22:28 (HHMP MM SS) Channel FOUND ANOMALY

ESS 92466

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

RETURN TO LEVEL 8 TO VERIFY (MANUAL CONTROL)

End DWELL 22:30 (HHMP MM SS)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1023

Test Date: 02/06/92

Tester (Name & stamp or sign):

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 21:48 (THHR MM:MIN)

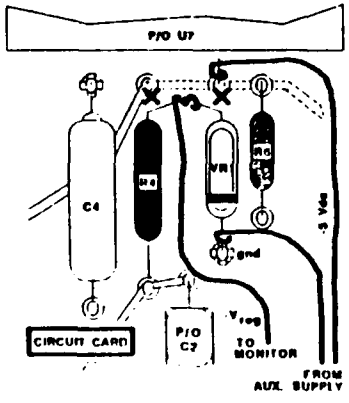
Voltage across LOAD RESISTOR: -5.219 (Vdc) (refer to Appendix D; nominally -5 Vdc)

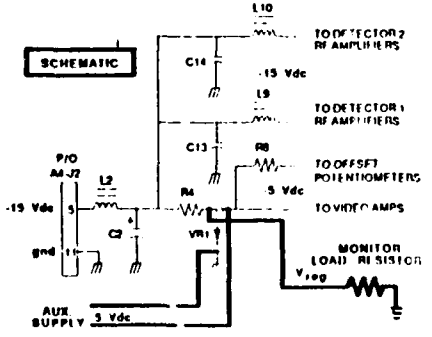
End TEST: 21:49 (THHR MM:MIN)

Conformal Coating Sample is still okay

135

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 02/06/92 (02/07/92)

STEP-STRESS Level: 8 RETEST

CHECK ANOMALY. WAS AT LEVEL 9

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS Ramp Chamber Temperature to STEP-STRESS Level, Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 22:30 (HR:MIN) Decreasing Start DWELL: 23:00

STEP-STRESS Level Chamber Air Temperature: +124.9 (°C) Flange Temperature: +136.1 (°C)

STEP-STRESS Level Component Temperature: +134 (°C)

Monitor Level 8 Temp throughout Retest

Reading for Level 8 Settings

VOLTAGE STEP-STRESS During Temperature Ramp: Increment Voltage to STEP-STRESS Level

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: −6.60 (Vdc)

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: −17.40 (Vdc)

Time Constant - 5 Volts dc Setting: −5.112 (Vdc)

Decrease to Level 0 Voltages (21:35)

Increment back to Level 8 Voltages (00:28) 02/07/92

Restabilize from 00:35 to 01:07 for Level 8 Voltages 02/07/92

Monitoring during ramp Synth 312 steadily drifting higher in frequency

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 23:07 (HR:MIN)

Settings: Freq Word (31-01 & 33-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 157.9 (mA) Δ = 0.0 -5 Volts dc: 85.5 (mA)

+15 Volts dc: 115.7 (mA) Δ = −0.9 -15 Volts dc: 57.2 (mA)

End TEST: 23:09 (HR:MIN)

CURRENTS AT LEVEL 0 VOLTAGE SETTINGS

+5: 123.2 mA -5: 81.8 mA

+15: 120.3 mA -15: 56.4 mA

TEST continued next page

(13:06 EDT) (21:56 EDT 00:02 2 to 12 clock drift) (21:40) (21:44)

ANOMALY Level 8 Voltages Connected

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STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1023 Test Date: 02/06/92 (02/07/92)

STEP-STRESS Level: 8 RETEST

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST At D: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with settings for Channels 50 at this STEP-STRESS Level.

Start TEST: 0MIT (HR:MIN) (00:13) 02/07/92 (Level 0 Voltages)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 (Level)	Detector 1 Duty Cycle (percent)	Detector 2 (Level)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	Intermittent	17% - 52%	(INTERMITTENT)	17% - 52%	
	I > Q	(Yes/Yes 50%)		(INTERMITTENT)	17% - 52%	Could be connection at input/output
	I > Q > 0	(intermittent 50%)	(INTERMITTENT only 50%)			
	Q > 0	(Yes/Yes 50%)		(INTERMITTENT)	17% - 50%	
Other Specify	I > 0					Quick look at Detectors Still good CH00 0 dBm Level 8 02/06/92 23:10 to 23:12
(dBm)	I > Q > 0					
	Q > 0					
Other Specify	I > 0					
	I > Q					
(dBm)	I > Q > 0					
	Q > 0					
-75 dBm	I > 0	(≈ 50)		(Constant 50%)		Looks like it needed time to stabilize for decrease in voltage from 8 to 0
	I > Q	(≈ 50)		(≈ 50)		
	I > Q > 0	(Less than 50%)	(17%)	(Less than 50%)	(17%)	
	Q > 0	(Less than 50%)		(Less than 50%)		

ANOMALY Level 0 Voltages Connected

ONLY INTERMITTENT MEANS SIGNAL WOULD SOMETIMES NOT BE PRESENT

MUST HAVE TEMPORARY CONNECTIONS IN DETECTOR OR CONNECTOR ASSEMBLY CIRCUIT

Could be connection at input/output

5.12 V p-p + 2.5 mV offset dc

11 SI Continued next page

(end 00:24 02/07/92)

omit temperature effects due to V-stress sequencing

Stabilize at Level 8 (21:40) Sequencing 00:34

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1023 Test Date: 02/06/92

STEP-STRESS Level: 8 RETEST

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued.

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Data	Detector 1 Limits T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Limits T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

Didn't Check @ CH. 50

End TEST: CMIT (TIME HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1023 Test Date: 02/06/92

STEP-STRESS Level: 8 RETEST 8 02/07/92

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level

Start TEST: 23:12 (TIME HR MIN) (23:45)*

J12 had a 54 MHz decrease check ch 50 pwr Level 8 to Level 9 change. Measure = 24 MHz decr. Did increase at beginning from Level 9 to Level 8 Retest 2/7

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations
50 min	638 (664)	+11.8 (+10.0)	624 (650)	-8.2 (+7.8)	*Accounts for cable losses
35 min	650 (676)	+11.5 (+10.1)	667 (693)	-8.1 (+7.9)	Retest CH 35 Synth 1 Synth 2
18 min	755 (825)	+11.4 (+10.0)	738 (825)	+12.0 (+5.8)	690 +11.4 692 MHz +11.7 666 +9.8
90 min	820 (921)	+10.0 (+3.9)	802 (921)	+11.8 (+5.1)	ANOMALY Causes V2 to Level 9

Check Synth Level

LOW THAN EXPECTED

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level, Tester Name & Date. ATTACHMENT NO (CIRCLE ONE)

End TEST: 23:34 (TIME HR MIN) (23:59)*

NOTE: Using Level 9 Voltage ⇒ Decreased Incrementally prior to data

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1 hour at this STEP-STRESS Level

RETEST INDICATES NO FAILURE OF ANOMALIES (STATUS CURRENT & DETECTED) End DWELL: 01:10 (TIME HR MIN) 02/07/92

CONTINUE TO LEVEL 10

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 02/06/92

Tester: L.B. Mueller

STEP-STRESS Level: 8 RETEST

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

Start TEST: 23:05 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.202 (Vdc) (refer to Appendix D, nominally -5 Vdc)

End TEST 23:06 (TIME HR MIN)

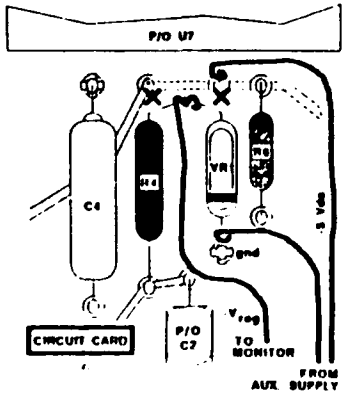
(-5.1 no Load)

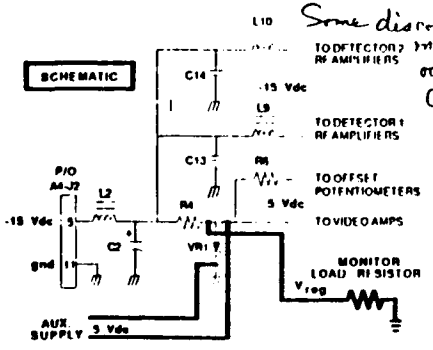
Circuit card of Sample @ beginning of Dwell shall appear clean.

LBM 02/6/92

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





Some discoloration on pc board

C 1:08 02/07/92 LBM

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/07/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 10

FROM LEVEL B RETEST

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 01:10 (TTMP HR MIN) Program #2 Interval #20 Start DWELL: 01:40 (TTMP HR MIN)

STEP-STRESS Level Chamber Air Temperature: +139.7 (°C) (Chamber thermocouple reading) Flange Temperature: +151.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +150 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +7.00 (Vdc) -5 Volts dc: -7.00 (Vdc) Increment to Level 9 then 10

+15 Volts dc: +18.00 (Vdc) -15 Volts dc: -18.00 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.112 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 01.43 (TTMP HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 171.2 (mA) -5 Volts dc: 108.4 (mA) increased again

+15 Volts dc: 122.7 (mA) -15 Volts dc: 596.5 (mA)

End TEST 01:47 (TTMP HR MIN) increased further any before

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/07/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 01:47 (TTMP HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.48/9.60	47	4.64/9.60	48	
	I > Q	4.72/9.60	49	"	48	
	I + Q > 0	4.64/9.60	48	"	48	
	Q > 0	"	48	"	48	
Other Specify -72 (dBm)	I > 0	4.16/9.60	43			
	I > Q	4.80/9.60	50			
	I + Q > 0	4.16/9.60	43			
	Q > 0	"	43			
Other Specify -72 (dBm)	I > 0			4.32/9.60	45	Same as -75
	I > Q			4.96/9.60	52	
	I + Q > 0			4.80/9.60	42	
	Q > 0			4.16/9.60	43	
-75 dBm	I > 0	See Above		3.84/9.60	40?	
	I > Q	5.12/9.60	53	4.96/9.60	52	
	I + Q > 0	4.00/9.60	42	4.00/9.60	42	
	Q > 0	4.16/9.60	43	4.16/9.60	43	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/07/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Least T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Least T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.48/9.60	47	4.48/9.60	47	
	I > Q	"	47	"	47	
	I + Q > 0	"	47	"	47	
	Q > 0	"	47	"	47	
Other Specify (dBm)	I > 0	4.16/9.60	43	—	-70	
	I > Q	4.91/9.60	52			
	I + Q > 0	3.84/9.60	40		-72 Improper Shift @ -70	
	Q > 0	4.00/9.60	42			
Other Specify -72 (dBm)	I > 0			3.84/9.60	40 @ -70 4.00/9.60 42 @	
	I > Q			4.16/9.60	43	
	I + Q > 0			3.84/9.60	40	
	Q > 0			4.00/9.60	42	
-75 dBm	I > 0	Very Noisy		Very Noisy		
	I > Q	"		Noisy ≈ 50%		
	I + Q > 0	"		Very Noisy		
	Q > 0	"		"		

End TEST 02:04 (HHMP MM MN) See above

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/07/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 02:05 (HHMP MM MN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation (*comment for cable loss)
50 min	620	-6.8	600	-24.3	will below bandwidth
35 min	648	+6.1	618	+16.5	Anomaly Synth #2
18 min	700	+11.4	633	-5.4	all below Q1 50 freq Synth 2
00 min	732	+10.9	657	+4.49	

Synth 1 drift slow! Power output J5 is reasonable

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STRESS-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 02:28 (HHMP MM MN)

Can't Verify this Level.

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

RETEST AT LEVEL 9 TO VERIFY End DWELL: 02:40 (HHMP MM MN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 02/07/92

STEP-STRESS Level: 10 Tester: J D Mueller

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

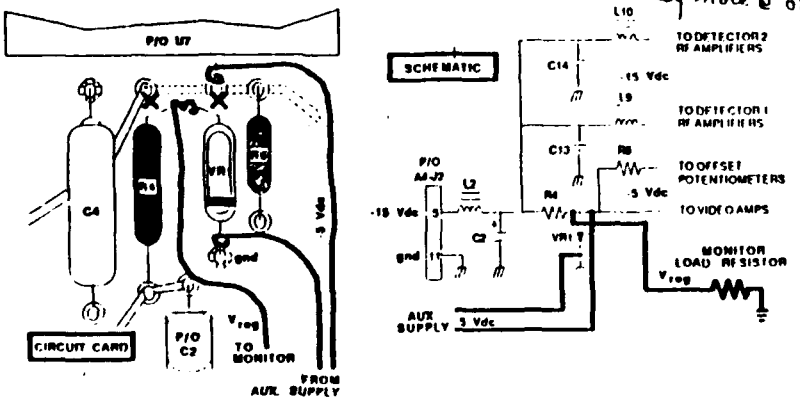
Start TEST: 01:47

Voltage across LOAD RESISTOR: -5.231 (Vdc) (refer to Appendix D, nominally -5 Vdc)

End TEST: 01:47

Confirmed Count.
Simple is darkening, but not too badly
02:29 10x
Darkening more @ 02:39 10x

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/07/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 9 RETEST L.S. Mueller

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 02:40 (HHMM HR MIN) decreasing Start DWELL: 03:10 (HHMM HR MIN)

STEP-STRESS Level Chamber Air Temperature: +1325 (°C) (Chamber thermocouple reading) Flange Temperature: +144.0 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +142 (°C) (refer to Appendix A Table)

VOLTAGE STEP-STRESS During Temperature Ramp, Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +6.80 (Vdc) -5 Volts dc: -6.80 (Vdc)

+15 Volts dc: +17.70 (Vdc) -15 Volts dc: -17.70 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.112 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 03:10 (HHMM HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 162.5 (mA) Δ = -2.2 mA ✓ -5 Volts dc: 96.0 (mA) ✓

+15 Volts dc: 110.0 (mA) ✓ -15 Volts dc: 585.4 (mA) ✓

End TEST: 03:11 (HHMM HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/07/92

STEP-STRESS Level (enter 0 - 10): 9 RETEST L.S. Mueller

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input From 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 04:15 (HHMM HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 I (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 I (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1023 Test Date: 02/02/92

STEP-STRESS Level: 9 RETEST

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Data	Detector 1 Lowest T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Lowest T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

Detectors CW'S C look okay Quick check @ 03:15 while synth is ramping via rem at 60 MHz

End TEST 03:27 (HHMP MB MIC)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1023 Test Date: 02/07/92

STEP-STRESS Level: 9 RETEST

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST. At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST 03:12 (HHMP MB MIC)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *Adjustment for cable losses
50	630 ✓	-1.9 ✓	## 615 ✓	-15.3 ✓	
35	670 ✓	+10.5 ✓	## 650 ✓	+3.4 ✓	## Synth #2 drifts quickly Synth #1 stable
18	736 ✓	+11.3 ✓	## 708 ✓	+10.6 ✓	
00	791 ✓	+10.2 ✓	744 ✓ bi-modal as before	+10.9 ✓	ALL SYNTHS CHECKS w/ PRIOR LEVEL 9

Additional Testing (OPTIONAL), **RADIO FREQUENCY OUTPUT TEST**: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check one)

End TEST 03:29 (HHMP MB MIC)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

NO FAILURE VERIFIED. COMPARES w/ PRIOR LEVEL 9 @ 22.1 02/06/92. End DWELL 03:30 (HHMP MB MIC)

STEP-STRESS LEVEL COMPLETE

LEVEL 10 HAS ALREADY BEEN REACHED. RAMP BACK TO LEVEL 0.

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1023 Test Date: 02/07/92

STEP-STRESS Level: 9 RETEST Tester: [signature]

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

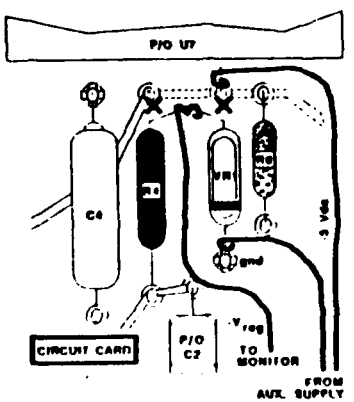
Start TEST: 03:11 (Hour Min Sec)

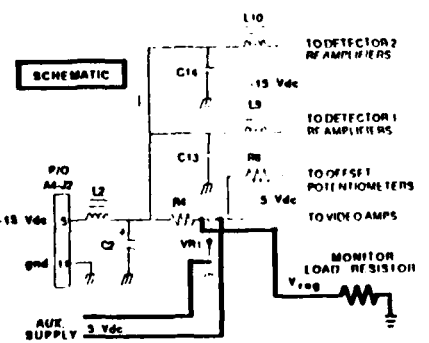
Voltage across LOAD RESISTOR: -5.207 ✓ (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 03:11 (Hour Min Sec)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 4 digits): 1023 Test Date: 02/07/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 0 FINAL J.D. Mueller

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 03:30 (HR:MIN) (Program #3 Init*1) Decrease from LEVEL 9 Retest OF LEVEL 10 (Ramp is 30 minutes) Start DWELL: 04:55 (HR:MIN)

STEP-STRESS Level Chamber Air Temperature: +61.2 (°C) (Chamber thermocouple reading) Set to +61°C

Flange Temperature: +68.8 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +70 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level: (Record settings below)

Supply Voltages: +5 Volts dc: +5.0 (Vdc) -5 Volts dc: -5.0 (Vdc)

+15 Volts dc: +15.0 (Vdc) -15 Volts dc: -15.0 (Vdc)

Asm. Constant - 5 Volts dc Setting: -5.112 (Vdc)

During Ramp Gradually Decrease Voltages in Increments completed @ 03:55

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 04:55 (HR:MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J9) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 125.2 (mA) -5 Volts dc: 80.6 (mA)

+15 Volts dc: 112.2 (mA) -15 Volts dc: 49.3 (mA)

End TEST: 04:56 (HR:MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 1 of 4

UUT Serial Number (enter 4 digits): 1023 Test Date: 02/07/93

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with wiring for Channels 50 at this STEP-STRESS Level.

Start TEST: 04:58 (HR:MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J9) = 607.35 MHz at 0 to -75 dBm

Rcv Sig (dBm)	I & Q Data	Detector 1 Level T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Level T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72/9.60	49	4.72/9.60	49	
	I > 0	4.8/9.60	50	4.80/9.60	50	
	I + Q > 0	4.72/9.60	49	"	50	
	Q > 0	4.80/9.60	50	4.42/9.60	47	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.32/9.60	45	4.44/9.60	46	
	I > 0	4.64/9.60	48	4.8/9.60	50	Slightly Degraded within tolerances
	I + Q > 0	4.32/9.60	45	4.8/9.60	50	
	Q > 0	4.45/9.60	47	4.44/9.60	46	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/07/93

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (msec) T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 t (msec) T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.64/9.60	48	4.73/9.60	49	
	I > Q	4.80/9.60	50	4.80/9.60	50	
	I + Q > 0	"	50	4.73/9.60	49	
	Q > 0	"	50	4.46/9.60	47	
	I > 0					
Other: Specify	I > Q					
(dBm)	I + Q > 0					
	Q > 0					
	I > 0					
Other: Specify	I > Q					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.48/9.60	47	4.48/9.60	47	
	I > Q	4.73/9.60	49	4.73/9.60	49	
	I + Q > 0	4.48/9.60	47	4.48/9.60	47	
	Q > 0	4.04/9.60	48	4.32/9.60	45	

End TEST: 05:16 (HHMP MM MM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1023 Test Date: 02/07/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at the STEP-STRESS Level

Start TEST: 05:16 (HHMP MM MM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*measure for cable losses)
50 min	684 ✓	+12.0 ✓	684 ✓	+11.5 ✓	All frequencies, power levels accounted for
35 min	729 ✓	+11.6 ✓	729 ✓	+11.9 ✓	
18 min	825 ✓	+11.4 ✓	825 ✓	+12.0 ✓	check okay
00 min	921 ✓	+10.0 ✓	921 ✓	+11.1 ✓	

Noise well off set point out of data.

Additional Testing (OPTIONAL), **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT (Check box)

2 runs each

End TEST: 05:45 (HHMP MM MM)

STEP-STRESS LEVEL DATA CONTINUED

ELAPSED TIME STEP-STRESS The Dwell will have a duration of 1-hour at this STEP STRESS Level

TEST COMPLETE End DWELL: 05:55 (HHMP MM MM)

Ramp to Room Ambient Program #3 Input #3

Power Unit OFF @ 05:56

02/07/92

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1023 Test Date: 02/07/93

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0 FINAL

CSG 92<66 TEST

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: As Built: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

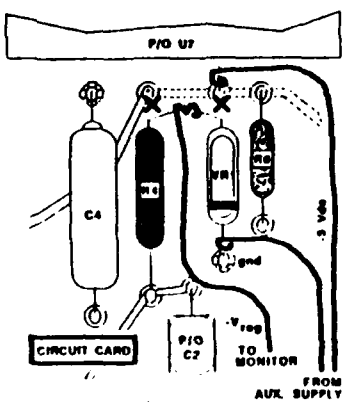
Start TEST: 04:56 (HH:MM:SS)

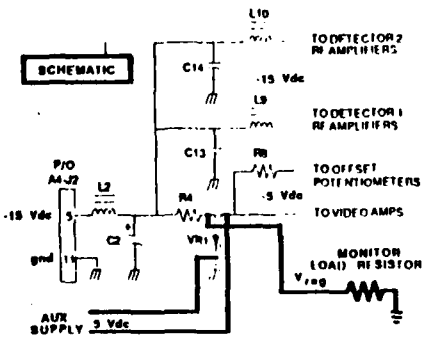
Voltage across LOAD RESISTOR: -5.062 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 04:57 (HH:MM:SS)

1417

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





Run # 1 of 2

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # MSN 1023

Power at J5 is 11.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is .5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

Synth # 1 (J5)
02/07/92 (GSC 92466 TEST)
LEVEL 0
FINAL

Noise offset's printed

Run # 2 of 2

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # MSN 1023

Power at J5 is 11.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is .3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is .5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 919.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

Synth # 1 (J5)
LEVEL 0
FINAL
02/07/92 (GSC [illegible])

Noise floor printed

Run #1 of 2

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # MSN 1023

Power at J12 is 11.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

SYNTH #2 (J12)
02/07/92
LEVEL 0
FINAL

149

Run #2 of 2

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # MSN 1023

Power at J12 is 11.2 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

SYNTH #2 (J12)
LEVEL 0
FINAL
02/07/92

Noise spikes present but within limits

TEST EQUIPMENT & CALIBRATION LOG

Maintain Log for testing conducted 02/05/92 through _____

Item #	DESCRIPTION	Manuf. & Part No.	ID NUMBER	LAST CAL*	CAL* DUE	Item Notes
01	T/R Test Station	HAC; SPECIAL	G-132043		NCR	F-A15223
02	Control Panel	HAC; SPECIAL	G-132290		NCR	
03	Signal Generator	HP; 8660C	G-128061	12/12/91	03/13/93	
04	Auxiliary Section	HP; 86631B	G-128062		NCR	
05	RF Section	HP; 86603A	G-128063	12/17/91	01/13/93	
06	Spectrum Analyzer	HP; 8568A w/ Opt E16	G-132082	12/11/91	06/30/92	
07	FET Probe	HP; 1120A	G-132055	12/18/90	09/30/92	
08	Power Meter	HP; 436A	G-128036	06/18/91	11/29/92	
09	Power Sensor	HP; 8482A	G-128059	07/09/91	10/21/92	
10	Oscilloscope	HP; 1980B	G-132049	09/24/91	08/11/92	
11	Digital Multimeter	SystronDonner; 7344A	G-127998	06/06/91	08/18/92	
12	Digital Multimeter	HP; 3478A	H-A53624	09/06/91	06/25/92	
13	Power Splitter	MiniCkts; ZFSC-2-5	None		NCR	
14	Power Splitter	MiniCkts; ZFSC-2-5	None		NCR	
15	Reg. Power Supply	Lambda; LP-531-FM	G-132292		NCR	+15Vdc
16	Reg. Power Supply	Lambda; LP-531-FM	G-132292		NCR	-15Vdc
17	Reg. Power Supply	Lambda; LP-530-FM	G-132291		NCR	+5Vdc
18	Reg. Power Supply	Lambda; LP-520 FM	G-132291		NCR	-5Vdc
19	Computer	HP; 9845B	G-128012		NCR	
20	Flex. Disk Memory	HP; 9895A	G-133309		NCR	
21	Signal Generator					
22	Oscilloscope	Tektronix; 2465				
23	Digital Multimeter					
24	Digital Multimeter					
25	Digital Multimeter					
26	Thermal Chamber	Thermotron; S-4 w/Cntl	H-B07567	09/18/91	09/02/92	
27	Data Acqtn Cntl Unit	HP; 3497A	H-[illegible]	11/14/91	07/29/93	
28	Computer	HP; Model 85B	H-AB6423		NCR	
29	Power Supply, AUX.	HP-6299A	H-357054		NCR	
30	Plotter	HP-7470A	H-512478		NCR	
31						
32						
33						
34						
35						
36	TESTED MSN 1023					
37						
38						
39						
40						
41						
42						

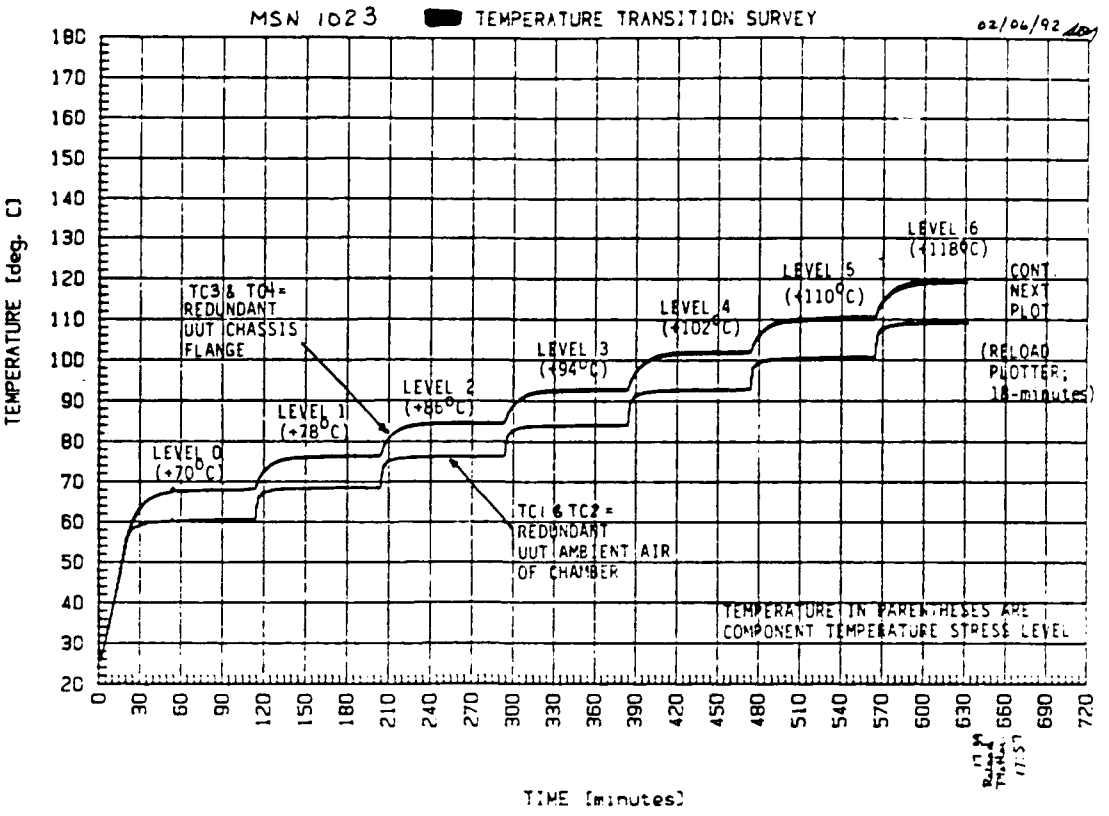
*NCR - Non-Calibration Required

150

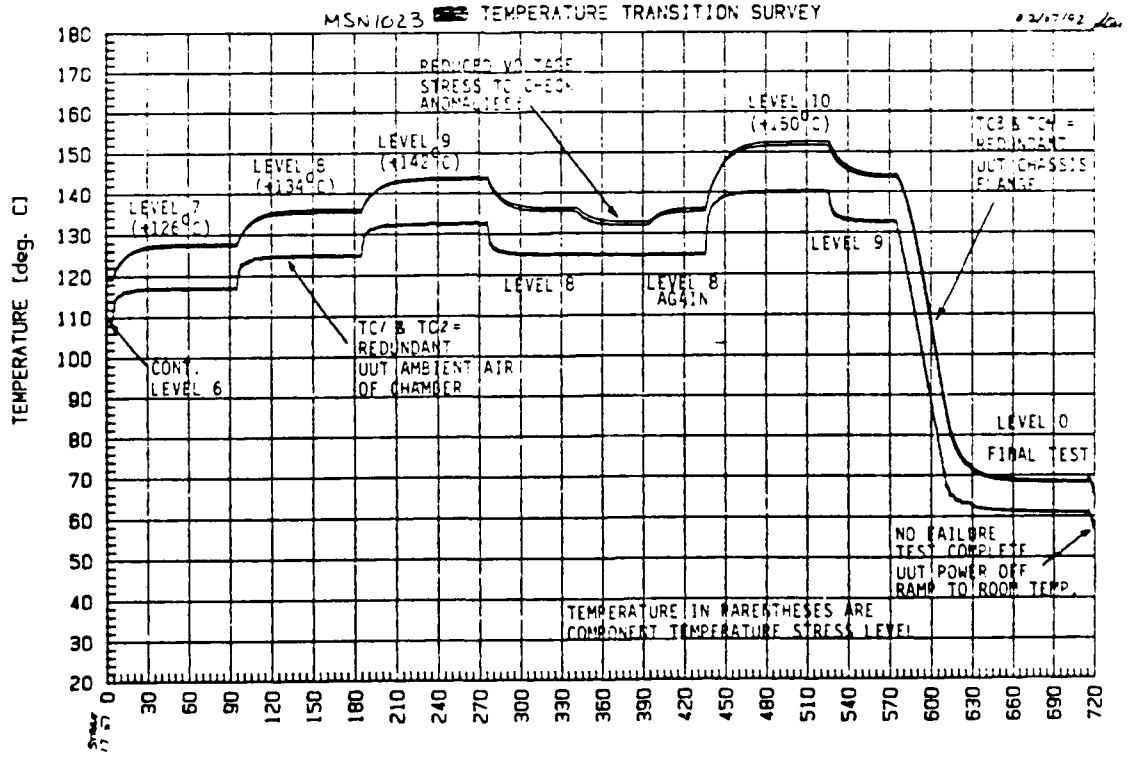
DATE: [redacted] 2/5/92 TIME: ~~3:41PM~~

```
Synth_ref= 1499990
Freq_mod_ref= 9999980
Sp_clock_output =  0
Phase_lo_output =  1.08
Phase_if_output =  0
Up_dn_conv_lo =  3.59
313.75_lo =  15 dBm /313.75183E6MHz
```

Channel	Freq	Dn_conv_output	Synth_lo_output	Hit_sgnl_l_o
(50)	684	1.05	1.19	2.08
49	687	1.11	1.25	2.1
48	690	1.17	1.15	2.03
47	693	1.2	1.06	1.93
46	696	1.21	1.2	1.94
45	699	1.24	1.39	1.99
44	702	1.27	1.39	1.97
43	705	1.24	1.27	1.85
42	708	1.24	1.25	1.79
41	711	1.27	1.33	1.84
40	714	1.3	1.35	1.9
39	717	1.3	1.29	1.81
38	720	1.31	1.43	1.74
37	723	1.32	1.7	1.82
36	726	1.34	1.83	1.92
(35)	729	1.31	1.72	1.84
34	732	1.26	1.53	1.69
33	735	1.25	1.56	1.7
32	738	1.25	1.67	1.74
31	741	1.28	1.71	1.74
30	744	1.32	1.71	1.71
29	747	1.35	1.86	1.75
28	750	1.39	2.01	1.86
27	753	1.35	2	1.89
26	756	1.27	1.8	1.76
25	759	1.25	1.78	1.64
24	762	1.3	1.94	1.66
23	765	1.39	2.02	1.74
22	768	1.48	1.97	1.72
21	771	1.56	1.94	1.72
20	774	1.58	2.07	1.83
19	777	1.55	2.14	1.94
(18)	825	1.63	2.3	1.65
17	828	1.6	2.32	1.74
16	831	1.58	2.23	1.68
15	834	1.63	2.11	1.58
14	837	1.67	2.15	1.58
13	882	1.5	1.99	1.51
12	885	1.55	1.93	1.41
11	888	1.64	1.98	1.41
10	891	1.65	2.06	1.52
9	894	1.61	2.07	1.6
8	897	1.63	1.95	1.52
7	900	1.63	1.89	1.43
6	903	1.5	1.89	1.42
5	906	1.38	1.89	1.44
4	909	1.4	1.85	1.33
3	912	1.5	1.79	1.29
2	915	1.54	1.82	1.43
1	918	1.48	1.84	1.56
(0)	921	1.43	1.79	1.57



STEP-STRESS TEST MSN 1023 PLOT 1 OF 2
BEGIN TEST: 02/06/92



STEP-STRESS TEST MSN 1023 PLOT 2 OF 2
CONTINUED TEST: 02/06 & 02/07/92
COMPLETE TEST: 02/07/92

Test Data Cont'd: Date: FEB 5 1992

UUT MSN 1023

1400hrs: START SET UP OF MSN 1023
IN CHAMBER & THERMAL PROGRAM / DATA TAPES
T24 ADDED & SAVE TO PROGRAM
T21 - CHAMBER AIR
T22 - CHAMBER AIR (REDT)
T23 - CHASSIS PLNG (A3)
T24 - CHASSIS PLNG (A2)

1600hrs; Completed Practice Run w/ UUT Energized
T23, T24 ≈ 40°C, T21, T22 = 25°C

1603hrs: Paused Programmed Scan 002: To
Resume Program hit <CONT> key
Test to tentatively start 0700hrs, Feb 6, 1992

FEB 6 1992

LDM 06 FEB. 1992 HIT <CONT> Thermal Program
0710 hrs: Start Ramp to 61°C (Prog 1, INT 1) level 0
0800hrs: Start 61°C Dwell (Prog 2, INT 1)

09 00hrs: Start Ramp to 69°C (Prog 1, Int 2) level 1
09:30hrs: Start 69°C Dwell
10 30 hrs: Start Ramp to 77°C level 2
11:00hrs: Start 77°C Dwell

Data Recorder

Test Data Cont'd: Date: Feb 6 LDM 1992

UUT MSN 1023

12:00hrs: Start Ramp to 85°C level 3
12:30 hrs: Start 85°C Dwell
13:30 hrs: Start Ramp to 94°C level 4
14:00 hrs: Start 94°C Dwell

The following is entered into LOGBOOK for MSN 1028
Step-Stress Test as recorded from Test Data Sheets
for testing Conducted 06 February thru 07 February 1992:
08/07/92

06 FEBRUARY 1992

15:00 : Start Ramp to +102°C LEVEL 5 (1-minute + 29-minute stabilization).
15:30 : Start +102°C Dwell (for 1-hour).
16:30 : Start Ramp to +111°C LEVEL 6.
17:00 : Start +111°C Dwell.
17:39 : Pause Plot. Remove Data TAPE (1 of 2).
RELOAD PLOT Routine & RUN.
17:57 : New Plot started. Next Data TAPE (2 of 2).
(Interruption of plotting was 18-minutes)
Testing was uninterrupted.
18:00 : Complete +111°C Dwell for LEVEL 6.
Start Ramp to +119°C LEVEL 7.
18:30 : Start +119°C Dwell.
19:30 : Start Ramp to +127°C LEVEL 8.
20:00 : Start +127°C Dwell.
21:00 : Start Ramp to +135°C LEVEL 9.
21:30 : Start +135°C Dwell.
21:48 : ANOMALY with +15V supply indicated
by decrease in current monitored (LEVEL 9 TEST)

Data Recorder

Test Data Cont'd: Date: 07 FEBRUARY 1992

UUT MSN 1023

06 FEBRUARY 1992 TEST DATA SHEET Records (continued)

22:28 : ANOMALIES with Synth #2 J12 (CH. 50 & 35) indicated by frequency & power output measured (LEVEL 9 TEST Continued). Complete Dwell at 22:30.

22:30 : Start decreasing Ramp to +127°C LEVEL 8 (Manual chamber controls) to CHECK ANOMALIES.

23:00 : Start +127°C Dwell. Begin testing of ANOMALIES.

21:35 : At LEVEL 8 incrementally decrease Voltage Stresses only (to nominal values typical of LEVEL 0 settings). Continue testing of ANOMALIES. NEW ANOMALY indicated w/ Detector.

07 FEBRUARY 1992 (continued testing) MSN 1023

00:28 : Still at LEVEL 8 Dwell, incrementally increase Voltage Stresses only back to LEVEL 8 settings. Continue testing of ANOMALIES once stabilized.

01:10 : Completed LEVEL 8 retest. NO FAILURES FOUND. Start Ramp to +143°C LEVEL 10.

01:40 : Start +143°C Dwell.

02:28 : Synth #2 (J12) indicates an ANOMALY. Complete Dwell to 02:40.

02:40 : Start decreasing Ramp to +135°C LEVEL 9 (Manually) to check ANOMALY.

03:10 : Start +135°C Dwell. Begin testing.

03:30 : NO FAILURE FOUND at LEVEL 9 retest therefore TESTING to LEVEL 10 is complete. Start Ramp to +61°C LEVEL 0 for FINAL TEST.

04:06 : Chamber at +61°C set point. UUT waiting stabilization.

04:55 : Start +61°C Dwell LEVEL 0 FINAL TEST.

05:55 : LEVEL 0 Dwell & TEST COMPLETE. UUT turned OFF. Start Ramp to Room Temp (Program #3 Ind #3)

This concludes entry from MSN 1023 TEST DATA SHEET Records.

Data Recorder SSN 556 02/07/92

STEP-STRESS TEST DATA NOTEBOOK

UNIT UNDER TEST: MSN 1028

TEST STATUS: NO FAILURES
(COMPLETED LEVEL 10)

TEST SUMMARY

STEP-STRESS		START DWELL	ANOMALY/ FAILURE	END DWELL
		3-Mar-92		
LEVEL	0	7:53		8:53
LEVEL	1	9:23		10:23
LEVEL	2	10:53		11:53
LEVEL	3	12:23		13:23
LEVEL	4	13:53		14:53
LEVEL	5	15:23		16:23
LEVEL	6	16:53		17:53
LEVEL	7	18:23	Anomaly	19:23
Retest	6	19:53		20:23
LEVEL	8	20:53		21:53
LEVEL	9	22:23	Anomaly	23:23
Retest	8	23:53		0:10
		3-Mar-92		4-Mar-92
LEVEL	10	0:40		1:40
FAILURE:			NONE	
Final Test	0	3:10		4:10
				4-Mar-92

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter HEX): 1028 Test Date: 3/3/92

Tester: (Name & ramp below)

STEP-STRESS Level (enter 0 - 10): 0

UUT Power ON @ 07:08 AM (Room Temp)

CAL WAS 03/02/92 AT 15:52

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 07:13 (HH:MM AM/PM) (Program #1, Interval #1)

Start DWELL: 07:53 (HH:MM AM/PM) (Program #2, Interval #1)

STEP-STRESS Level Chamber Air Temperature: 60.5 (°C) set @ 61°C

Flange Temperature: 69.1 (°C)

STEP-STRESS Level Component Temperature: 70 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 15V (Vdc) -5 Volts dc: -5V (Vdc)

+15 Volts dc: 115V (Vdc) -15 Volts dc: -15V (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

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UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 07:55 (HH:MM AM/PM)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1253 (mA) -5 Volts dc: 881 (mA)

+15 Volts dc: 115 (mA) -15 Volts dc: 501 (mA)

End TEST: 07:56 (HH:MM AM/PM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter HEX): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 07:56 (HH:MM AM/PM)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig (dBm)	I & Q -Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.8us/9.6us	50	4.8us/9.6us	50	
	I > 0	4.6us/9.6us	48	4.72us/9.6us	49	
	I + Q > 0	4.8us/9.6us	50	4.8us/9.6us	51	
	Q > 0	4.8us/9.6us	11	4.8us/9.6us	50	
Other: Specify -73 (dBm)	I > 0	4.8us/9.6us	50			BL @ -73dBm
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0 *	4.8us/9.6us	50	4.8us/9.6us	50	* little noisy
	I > 0	4.6us/9.6us	48	4.72us/9.6us	49	
	I + Q > 0	4.8us/9.6us	50	4.8us/9.6us	51	
	Q > 0	4.8us/9.6us	50	4.8us/9.6us	50	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number (xxxx MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (xxxx 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q Bits	Detector 1 t (msec) T (sec)	Detector 1 Duty Cycle (percent)	Detector 2 t (msec) T (sec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.8ms/9.6ms	50	4.8ms/9.6ms	50	
	I > Q	4.7ms/9.6ms	49	4.6ms/9.6ms	48	
	I + Q > 0	4.7ms/9.6ms	49	4.8ms/9.6ms	50	
	Q > 0	4.8ms/9.6ms	50	4.8ms/9.6ms	50	
Other Specify -73 (dBm)	I > 0	4.7ms/9.6ms	49			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1.1ms/9.6ms	11	4.8ms/9.6ms	50	
	I > Q	4.6ms/9.6ms	48	4.7ms/9.6ms	49	
	I + Q > 0	4.8ms/9.6ms	50	4.9ms/9.6ms	51	
	Q > 0	4.8ms/9.6ms	50	4.8ms/9.6ms	50	

End TEST: 08:17 (HH:MM MS MSM)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number (xxxx MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (xxxx 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 07:17 (HH:MM MS MSM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *comment for cable losses
50 min	684	13.47	684	12.67	pwr measured by mixer hold then pull each diff. reading pwr
35 min	729	12.53	729	12.13	
18 min	825	12.17	825	12.37	
00 min	921	10.9	921	12.2	

Additional Testing (OPTIONAL); RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 08:32 (HH:MM MS MSM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 08:57 (HH:MM MS MSM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1028

Test Date: 3/3/92

Tester: (Name & comp [illegible])

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

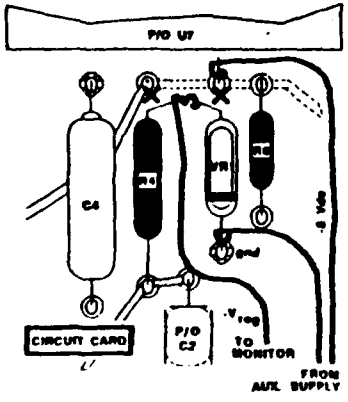
RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

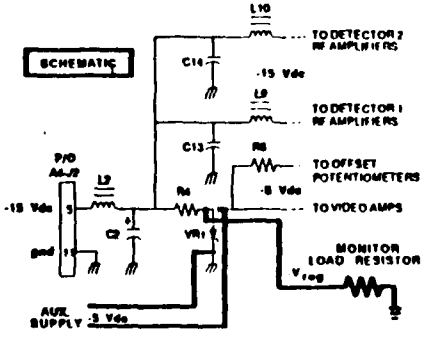
Start TEST: 08:32 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.04 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 08:53 (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





3/7/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 1.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # syn/det # 1020
stress level 0
J5 output

Power at J5 is 12.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 6.5 dBm @ 687.0 MHz (Spec=+9dBm minimum). syn/det #1028
Power at J12 is 8.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 4.8 dBm @ 693.0 MHz (Spec=+9dBm minimum). stress Level 0
Power at J12 is 6.5 dBm @ 696.0 MHz (Spec=+9dBm minimum). J12 output
Power at J12 is 7.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is less than 705.0 MHz which is below the specified frequency.
Power at J12 is 6.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 12.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).

Power at J12 is 10.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 1 Tester: (Please print name below)

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 08:53 (HHMM, Hit when)

Start DWELL: 09:23 (HHMM, Hit when)

STEP-STRESS Level Chamber Air Temperature: 65.4 / 27.8 (°C) (Chamber thermocouple reading)

Flange Temperature: 75.5 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 18 (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp, Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltage: +5 Volts dc: 15.2 (Vdc) -5 Volts dc: -5.2 (Vdc)

+15 Volts dc: +15.3 (Vdc) -15 Volts dc: -15.3 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 09:40 (HHMM, Hit when)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1299 (mA) -5 Volts dc: 87 (mA)

+15 Volts dc: 115 (mA) -15 Volts dc: 515 (mA)

End TEST: 09:41 (HHMM, Hit when)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 09:41 (HHMM, Hit when)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72u/9.6u	49	4.8u/9.6u	50	
	I > 0	4.44u/9.6u	48	4.72u/9.6u	49	
	I + Q > 0	4.8u/9.6u	50	4.92u/9.6u	51	
	Q > 0	4.8u/9.6u	50	4.8u/9.6u	50	
Other Specify -12 (dBm)	I > 0	4.8u/9.6u	50			
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	noisy		4.8u/9.6u	50	
	I > 0	4.44u/9.6u	48	4.72u/9.6u	49	
	I + Q > 0	4.72u/9.6u	49	4.92u/9.6u	51	
	Q > 0	4.8u/9.6u	50	4.8u/9.6u	50	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72us/4.6us	49	4.8us/4.6us	50	
	I > Q	4.6us/4.6us	48	4.6us/4.6us	48	
	I + Q > 0	4.72us/4.6us	49	4.8us/4.6us	51	
	Q > 0	4.72us/4.6us	49	4.8us/4.6us	50	
Other: Specify -12 (dBm)	I > 0	4.72us/4.6us	49			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		4.8us/4.6us	50	
	I > Q	4.6us/4.6us	48	4.8us/4.6us	49	
	I + Q > 0	4.8us/4.6us	50	4.8us/4.6us	51	
	Q > 0	4.6us/4.6us	50	4.8us/4.6us	50	

End TEST: 9 57 (Time: Hr Min)

TEST continued next page

16.3

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 9 57 (Time: Hr Min)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *account for cable losses
50 min	684	12.47	684	12.57	
35 min	729	12.53	729	11.93	
18 min	825	12.1 ✓	825	12.32	
00 min	921	10.7	921	11.79	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check box)

End TEST: 10 11 (Time: Hr Min)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 10 27 (Time: Hr Min)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 1028

Test Date: 3/3/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

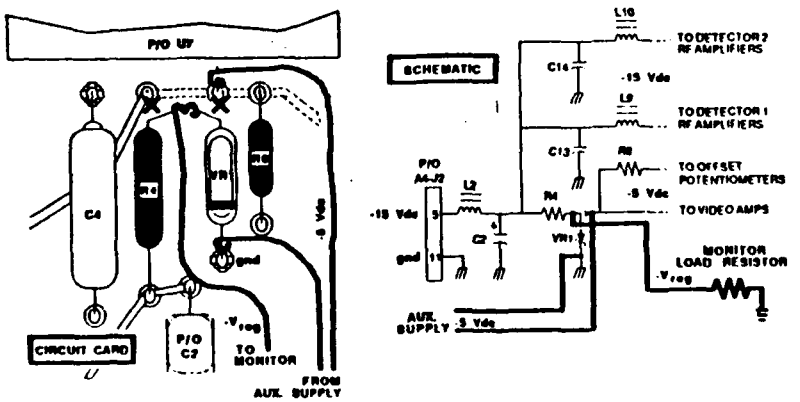
RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 10:11 (Time: HR:MIN)

Voltage across LOAD RESISTOR: -5.05 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 10:12 (Time: HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/3/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 6.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

syn/ect #1028

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

stress level 1
J5 output

Power at J5 is 12.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.3 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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7/1/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 7.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than 693.0 MHz which is below the specified frequency.
Power at J12 is 6.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is .1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).

syn/ect # 1028

stress level 1
J12 output

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 12.1 dBm @ 694.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is .1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).

Power at J12 is 10.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 3/3/92

Tester: (Name & comp below)

STEP-STRESS Level (enter 0 - 10): 2

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 10:23 (TIME HR MIN) Start DWELL: 10:53 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 76.2 (°C) (Chamber thermocouple reading)

STEP-STRESS Level Component Temperature: 86 (°C) (refer to Appendix B Table)

Flange Temperature: 81.2 (°C) (Thermocouple reading)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +5.4 (Vdc) -5 Volts dc: -5.4 (Vdc)

+15 Volts dc: +15.6 (Vdc) -15 Volts dc: -15.6 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 11:02 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1337 (mA) -5 Volts dc: 90 (mA)

+15 Volts dc: 117 (mA) -15 Volts dc: 526 (mA)

End TEST 11:02 (TIME HR MIN)

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 11:02 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (msec) / T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 t (msec) / T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72 / 9.6	49	4.80 / 9.6	50	
	I > Q	4.64 / 9.6	48	4.72 / 9.6	49	
	I + Q > 0	4.84 / 9.6	50	4.88 / 9.6	51	
	Q > 0	4.74 / 9.6	49	4.84 / 9.6	50	
Other Specify -72 (dBm)	I > 0	4.84 / 9.6	49			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1.116 noisy		4.84 / 9.6	50	
	I > Q	4.64 / 9.6	48	4.72 / 9.6	49	
	I + Q > 0	4.84 / 9.6	50	4.88 / 9.6	51	
	Q > 0	4.72 / 9.6	49	4.84 / 9.6	50	

TEST Continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q -Bits	Detector 1 Latest T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Latest T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72us/96us	49	4.84us/96us	50	
	I > Q	4.44us/96us	48	4.72us/96us	49	
	I + Q > 0	4.84us/96us	50	4.84us/96us	51	
	Q > 0	4.72us/96us	49	4.84us/96us	50	
Other: Specify -72 (dBm)	I > 0	4.72us/96us	49			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noise		4.84us/96us	50	
	I > Q	4.72us/96us	48	4.72us/96us	49	
	I + Q > 0	4.72us/96us	49	4.84us/96us	51	
	Q > 0	4.72us/96us	49	4.84us/96us	50	

End TEST 11 23 (Hour Hr Min)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 11 23 (Hour Hr Min)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *account for cable losses
50 min	684	12.37	684	12.67	
35 min	729	12.93	729	11.93	
18 min	825	11.82	825	12.32	
00 min	921	10.5	921	11.99	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 11:35 (Hour Hr Min)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 1 53 (Hour Hr Min)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter 4 digits): 1028

Test Date: 3/3/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

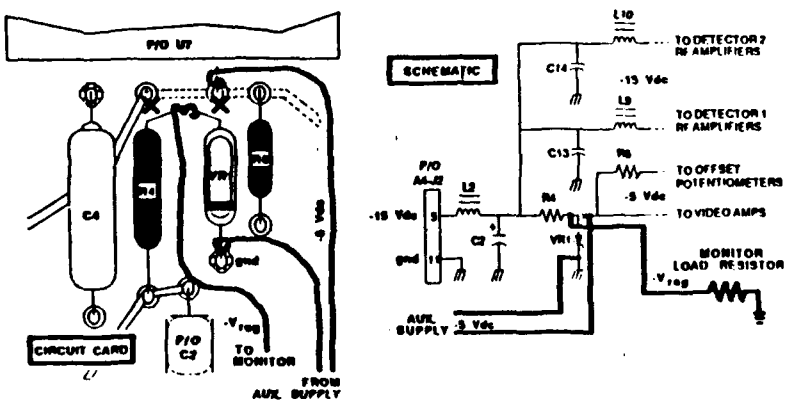
RESISTOR/ZENER DIODE MODIFICATION: At Dock: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 11:35 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.01 (Vdc) * (refer to Appendix D; nominally -5 Vdc)

End TEST: 11:36 (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/3/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 5.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).

Syn | Det #10 2r
Stress Level 2
J5 output

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] er. 0

Power at J5 is 12.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/3/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is-5.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 5.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is .1 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Syn | Det #10 2s
Stress Level 2
J12 output

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. 0

Power at J12 is 12.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is .1 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).

Power at J12 is 10.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1028 Test Date: 3/3/92

STEP-STRESS Level: 3

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 11:53 (TIME HR MIN) Start DWELL: 12:23 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 54.0 (°C) Flange Temperature: 92.4 (°C)
(Chamber thermocouple reading)

STEP-STRESS Level Component Temperature: 94 (°C)
(refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings to two)

Supply Voltages: +5 Volts dc: 15.6 (Vdc) -5 Volts dc: -5.6 (Vdc)

+15 Volts dc: +15.9 (Vdc) -15 Volts dc: -15.9 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 12:28 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1377 (mA) -5 Volts dc: 93 (mA)

+15 Volts dc: 119 (mA) -15 Volts dc: 540 (mA)

End TEST: 11:29 (TIME HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1028 Test Date: 3/3/92

STEP-STRESS Level: 3

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat each setting for Channels 30 at this STEP-STRESS Level.

Start TEST: 11:29 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72u/9.6u	49	4.8u/9.6u	50	
	I > 0	4.6u/9.6u	48	4.72u/9.6u	49	
	I + Q > 0	4.8u/9.6u	50	4.8u/9.6u	51	
	Q > 0	4.72u/9.6u	49	4.8u/9.6u	50	
Other Specify -11 (dBm)	I > 0	4.72u/9.6u	49			
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.72u/9.6u	49	4.8u/9.6u	50	
	I > 0	4.6u/9.6u	48	4.72u/9.6u	49	
	I + Q > 0	4.72u/9.6u	49	4.8u/9.6u	51	
	Q > 0	4.72u/9.6u	49	4.8u/9.6u	50	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter 4 digits): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Linear T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Linear T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72us/4.64us	49	4.64us/4.64us	50	
	I > Q	4.64us/4.64us	48	4.64us/4.64us	48	
	I + Q > 0	4.72us/4.64us	49	4.64us/4.64us	51	
	Q > 0	"	"	4.64us/4.64us	50	
Other Specify -71 (dBm)	I > 0	4.64us/4.64us	49			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.64us noisy		4.64us/4.64us	50	
	I > Q	4.64us/4.64us	49	4.64us/4.64us	49	
	I + Q > 0	"	"	4.64us/4.64us	50	
	Q > 0	"	"	4.64us/4.64us	50	

End TEST: 11:40 (Time in HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter last 4 digits): 1028 Test Date: 3/3/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 11:40 (Time in HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	684	12.1	684	10.87	
35 min	729	12.33	729	11.63	
18 min	825	11.93	825	11.62	
00 min	921	11:00	921	12.7	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label/Attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT V (Check here)

End TEST: 12:54 (Time in HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 13:23 (Time in HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 1028

Test Date: 3/3/92

Tester: (Name & activity or base)

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

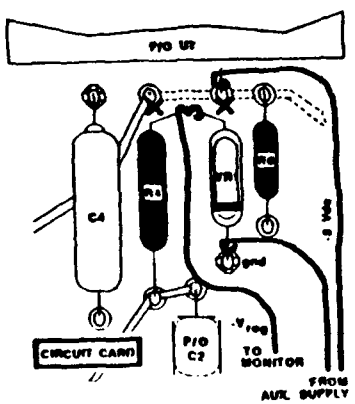
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

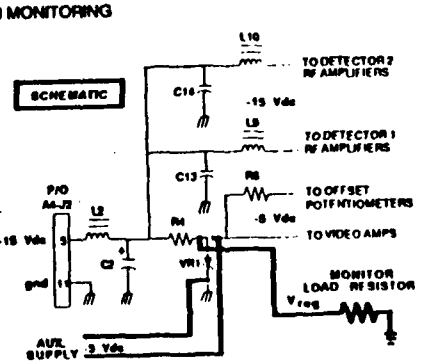
Start TEST: 12:54 (HOUR MIN SEC)

Voltage across LOAD RESISTOR: -5.08 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 12:55 (HOUR MIN SEC)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





FAIL DATA (if any) of Power Output requirements will be printed between the starred borders. 3/3/94

syn Det # 102.
Strap level 3
J5 output

****

Power at J5 is 4.1 dBm @ 880.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 11.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/3/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

9m/Def H1028
stress level 3
J12 output

****

Power at J12 is 6.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 769.0 MHz which is above the specified frequency.
Power at J12 is 8.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 897.0 MHz which is above the specified frequency.
Power at J12 is 5.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).

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FULL PRINT-OUT OF Power Output and Frequency [redacted]er. 8

Power at J12 is 6.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1028 Test Date: 3/3/92

Tester:

STEP-STRESS Level: 4

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 13:23 Start DWELL: 13:53

STEP-STRESS Level Chamber Air Temperature: 43.2 (°C) Flange Temperature: 101.2 (°C)

STEP-STRESS Level Component Temperature: 102 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 15.8 (Vdc) -5 Volts dc: -5.8 (Vdc)

+15 Volts dc: +16.2 (Vdc) -15 Volts dc: -16.2 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 13:53

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1415 (mA) -5 Volts dc: 93 (mA)

+15 Volts dc: 122 (mA) -15 Volts dc: 552 (mA)

End TEST: 13:54

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1028 Test Date: 3/3/92

STEP-STRESS Level: 4

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with cutting for Channels 50 at this STEP-STRESS Level.

Start TEST: 13:54

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.72us/96us	49	4.72us/96us	49	
	I > Q	"	"	4.64us/96us	48	
	I + Q > 0	4.72us/96us	49	4.88us/96us	51	
	Q > 0	"	"	4.8us/96us	50	
Other Specify -71 (dBm)	I > 0	4.72us/96us	49			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		4.72us/96us	49	
	I > Q	4.64us/96us	48	"	"	
	I + Q > 0	4.72us/96us	49	4.8us/96us	50	
	Q > 0	"	"	4.8us/96us	50	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (xxxx MSN): 1028 Test Date: 3/31/92

STEP-STRESS Level (xxxx 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (xxxx)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (xxxx)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.12us/16us	49	4.12us/16us	49	
	I > Q	4.12us/16us	48	4.12us/16us	48	
	I + Q > 0	4.12us/16us	49	4.12us/16us	51	
	Q > 0	"	"	4.12us/16us	50	
Other: Specify -71 (dBm)	I > 0	4.12us/16us	49			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		4.12us/16us	49	
	I > Q	4.12us/16us	48	4.12us/16us	49	
	I + Q > 0	"	"	"	"	
	Q > 0	"	"	"	"	

End TEST: 14:10 (TIME HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (xxxx MSN): 1028 Test Date: 3/3/92

STEP-STRESS Level (xxxx 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 14:10 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*measured for cable losses)
50 (xxx)	697 684 ok	12.29	684	12.57	J5 output noisy look
35 (xxx)	692 729 ok	12.33	729	10.93	freq # listed to r pwr level (marked in Red)
18 (xxx)	773 825 ok	11.5V	825	10.52V	readjusted - 5V supply to -5.7V from -5.8V
00 (xxx)	971 921 ok	9.6	921	11.1	J5 Back to normal (marked in Red)

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STRESS-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 14.45 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 14.53 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 1028 Test Date: 3/3/93

Tester: (Please print name)

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: *At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.*

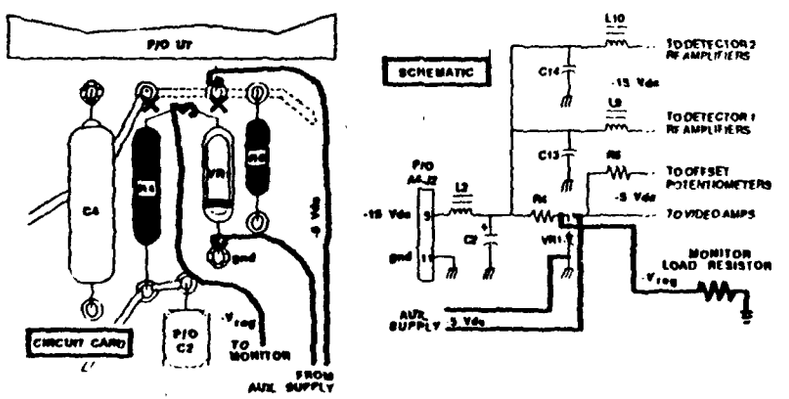
Start TEST: 14:45 (military time)

Voltage across LOAD RESISTOR: -5.1 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 14:46 (military time)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/3/92
synthesizer #1027
stress level 4

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders. J5 output

****

Power at J5 is-64.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-63.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-67.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-55.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-55.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-60.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-62.0 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-66.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-60.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-44.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-62.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-62.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-62.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-62.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-60.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-59.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.8 dBm @ 823.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-62.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-59.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-60.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-62.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-62.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-66.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-62.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-59.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 65.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-62.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-60.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-61.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-61.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-59.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-60.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 12.2 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-64.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-63.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-67.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is-55.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-55.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.0 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is-66.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is-44.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is-59.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is-59.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is-66.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-59.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-65.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is-62.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-61.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).

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Power at J5 is-59.1 dBm @ 913.0 MHz (Spec=+9dBm minimum).
Power at J5 is-60.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/3/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 7.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 693.0 MHz which is above the specified frequency.
Power at J12 is-62.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is less than 696.0 MHz which is below the specified frequency.
Power at J12 is 5.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is less than 717.0 MHz which is below the specified frequency.
Power at J12 is 5.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 738.0 MHz which is above the specified frequency.
Power at J12 is 6.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 823.0 MHz (Spec=+9dBm minimum).
Frequency is less than 824.0 MHz which is below the specified frequency.
Power at J12 is 8.5 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

Sayville + H1028
Stress level 4
J12 output

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.3 dBm @ 634.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number: 1028 Test Date: 03/03/92

Tester: A. D. Mueller

STEP-STRESS Level: 5

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 14:53 (TIME HR MIN) Start DWELL: 15:23 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +101.2 °C (Chamber thermocouple reading) Soak @ +102°C Plunge Temperature: +109.9 °C (Thermocouple reading)

STEP-STRESS Level Component Temperature: +110 °C (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increase Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.00 (Vdc) -5 Volts dc: -6.00 (Vdc)

+15 Volts dc: +16.50 (Vdc) -15 Volts dc: -16.50 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1102 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 15:36 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 144.8 (mA) -5 Volts dc: 95.2 (mA)

+15 Volts dc: 133.4 (mA) -15 Volts dc: 567.1 (mA)

End TEST: 15:37 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number: 1028 Test Date: 03/03/92

STEP-STRESS Level: 5

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or 99 at this STEP-STRESS Level.

Start TEST: 15:37 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Pins	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50%	480/960	50.0%	Changed scope from 6 div/T to 8 div/T
	I > Q	468/960	48.8%	"	50.0%	
	I + Q > 0	480/960	50.0%	"	50.0%	Total signal is 9.60 usec
	Q > 0	"	50.0%	468/960	48.8%	
Other: Specify -72 (dBm)	I > 0	480/960	50%			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	NOISY See above		480/960	50%	* explained next page
	I > Q	480/960	50%	"	50%	
	I + Q > 0	454/960	47.5%	468/960	48.8%	
	Q > 0	480/960	50.0%	"	48.8%	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter NSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 484 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Limit T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/9.60	50%	4.68/9.60	48.8%	
	I > Q	4.56/9.60	47.5%	4.56/9.60	47.5%	
	I + Q > 0	4.80/9.60	50%	4.80/9.60	50.0%	
	Q > 0	"	50.0%	"	50.0%	
Other: Specify -72 (dBm)	I > 0	4.80/9.60	50%			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Noise * See above		4.68/9.60	48.8%	* Difficult to determine duty cycle due to noise on rising edge. Increase input 3 dB.
	I > Q	4.56/9.60	47.5%	"	48.8%	
	I + Q > 0	4.80/9.60	50%	4.80/9.60	50.0%	
	Q > 0	"	50%	"	50.0%	

End TEST: 15:56 (military time)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter NSN): 1028 Test Date: 03/03/92 (03/04/92)

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 15:56 (military time)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	645.1	+4.7 (within 8 dB of 0 dBm)	628.7	-3.2 (still within 8 dB of 0 dBm)	was calibration date of comparison log recorded on data
35 min	689.7	+12.2	681.6	+12.7	
18 min	770.3	+12.9	792.7	+13.1	Both Synth's off freq but have stable locked output spectrum. Voltage pulling is occurring. This is known anomaly
00 min	844.4	+11.6	883.5	+12.3	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level Tester Name & Date. ATTACHMENT NO (Check box)

No failures found in Synth's

End TEST: 16:21 (military time)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 16:23 (military time)

MOVED WITH LEVEL 6

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 1028 Test Date: 09/03/92

Tester: (Name & Initials below)

STEP-STRESS Level (zero-based): 5

UUT PERFORMANCE TEST DATA — PERFORMANCE MONITORING

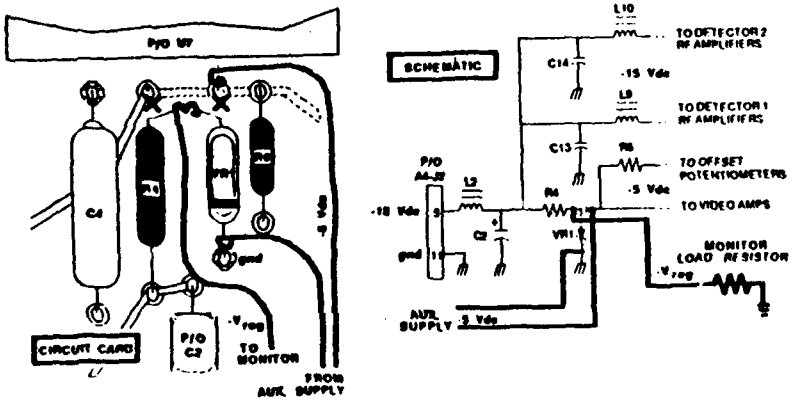
RESISTOR/ZENER DIODE MODIFICATION: At Depot: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 15:37 (Hour Min Sec)

Voltage across LOAD RESISTOR: -5.1139 (Vdc)[1] (refer to Appendix D; nominally -5 Vdc)

End TEST: 15:37 (Hour Min Sec)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 6

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 6

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 16:23 (TIME HR MIN) Start DWELL: 16:53 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +109.2 (°C) 781
(Chamber thermocouple reading) SEE +111 °C

Plenge Temperature: +119.0 (°C) 703
(Thermocouple reading)

STEP-STRESS Level Component Temperature: +118 (°C)
(refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: +6.20 (Vdc) - 5 Volts dc: -6.20 (Vdc)

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1101 (Vdc)

35 deg rotated 5.65 MHz
-10.043 V-Mass in room
@ 16:26 LDJ

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (radio) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 16:59 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1497 (mA) - 5 Volts dc: 974 (mA)

+15 Volts dc: 136.5 (mA) -15 Volts dc: 579.5 (mA)

End TEST: 17:01 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 6

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92 (9:00-14)

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with sorting for Channels 50 at this STEP-STRESS Level.

Start TEST: 17:02 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (msec) / T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 t (msec) / T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50.0	480/960	50.0	
	I > 0	468/960	48.8	468/960	48.8	
	I + Q > 0	480/960	50.0	480/960	50.0	
	Q > 0	"	50.0	"	50.0	
Other: Specify -72 (dBm)	I > 0	480/960	50.0			
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	468/960	50.0	480/960	50.0	
	I > 0	468/960	48.8	456/960	47.5	
	I + Q > 0	480/960	50.0	468/960	50.0	
	Q > 0	480/960	50.0	468/960	50.0	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 1 of 1

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 604 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q Bits	Detector 1 (Limit T (msec))	Detector 1 Duty Cycle (percent)	Detector 2 (Limit T (msec))	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50.0	480/960	50.0	
	I > Q	456/960	47.5	"	50.0	
	I > Q > 0	480/960	50.0	"	50.0	
	Q > 0	468/960	48.8	"	50.0	
Other Speedy -72 (dBm)	I > 0	480/960	50.0			
	I > Q					
	I > Q > 0					
	Q > 0					
Other Speedy (dBm)	I > 0					
	I > Q					
	I > Q > 0					
	Q > 0					
-75 dBm	I > 0	Noise Burst		480/960	50.0	
	I > Q	468/960	48.8	"	50.0	
	I > Q > 0	480/960	50.0	"	50.0	
	Q > 0	468/960	48.8	480/960	50.0	

End TEST: 17:12 (HHMM HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 1 of 1

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 17:14 (HHMM HR MIN)

35 pg dropped out 17:55 was off the oscilloscope @ 16 sec

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *comment for cable losses
50 (HEX)	63 641.2	+2.9	58 626.2	-4.3	(A) Synth #2 CH 18 signal slightly spread
35 (HEX)	44 685.0	+12.3	51 678.2	+12.6	(B) Both Synth's voltage pulling tracking error Level 4. Need to focus on CH 50 output power relationship to help CH's "Pump" of others still very good.
18 (HEX)	62 762.9	+12.6	37 708.1 (A)	+12.9	
00 (HEX)	86 835.1	+11.6	59 882.9	+11.3	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input to Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

End TEST: 17:40 (HHMM HR MIN) No Failure Found.

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUE ON TO LEVEL 7

End DWELL: 17:53 (HHMM HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 1028

Test Date: 03/03/92

Tester (Please print clearly below)

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

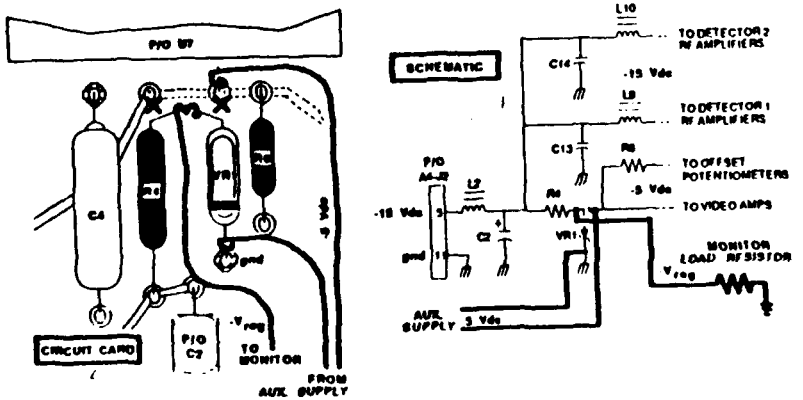
RESISTOR/ZENER DIODE MODIFICATION: As Built: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

Start TEST: 16:57 (HOUR MIN USED)

Voltage across LOAD RESISTOR: -5.1296 (Vdc) (refer to Appendix D, nominally -5 Vdc)

End TEST: 16:58 (HOUR MIN USED)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

UUT Serial Number: 1028 Test Date: 09/03/92

Tester: D.D. Mueller

STEP-STRESS Level: 7

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 17:53 Start DWELL: 18:23

STEP-STRESS Level Chamber Air Temperature: +117.7 TC1 (°C) Plenge Temperature: +127.1 TC3 (°C)

STEP-STRESS Level Component Temperature: +126 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level.

Supply Voltages: +5 Volts dc: +6.40 (Vdc) -5 Volts dc: -6.40 (Vdc)

+15 Volts dc: +17.10 (Vdc) -15 Volts dc: -17.10 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1102 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (-75 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 18:28

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rec Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1534 (mA) -5 Volts dc: 82.7* (mA)

+15 Volts dc: 1215* (mA) -15 Volts dc: 5909 (mA)

End TEST: 18:35

* Decreasing Current occurred @ LEVEL 8 w/ MSN 1030 (at 18:32:01) & LEVEL 7 w/ MSN 1023 (at 18:46:03)

TEST continued next page

No Failure Found

IS XMMU ANOMALY

SDM 09/04/92

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1028 Test Date: 09/03/92

STEP-STRESS Level: 7

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 18:36

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rec Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rec Sig (dBm)	I & Q Data	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	460/960	50.0	460/960	50.0	
	I > Q	460/960	50.0	456/960	47.5	
	I + Q > 0	480/960	50.0	480/960	50.0	
	Q > 0	480/960	50.0	480/960	50.0	
Other Specify -72 (dBm)	I > 0	468/960	48.8%			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Previous Data Missing ABOVE		480/960	50.0	
	I > Q	480/960	50.0	456/960	47.5	
	I + Q > 0	480/960	50.0	480/960	50.0	
	Q > 0	480/960	50.0	480/960	50.0	

TEST Continued next page

18:9

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Bits	Detector 1 Lmax T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 Lmax T (msec)	Detector 2 Duty Cycle (percent)	Observations
	I > 0	4.68/9.60	48.8	4.80/9.60	50.0	
	I > 0	4.80/9.60	50.0	4.68/9.60	48.8	
0 dBm	I + Q > 0	4.68/9.60	48.8	4.80/9.60	50.0	8 Bds / 1.20 msec/Bd
	Q > 0	4.80/9.60	50.0	4.80/9.60	50.0	
	I > 0	4.80/9.60	50.0			
Other Specify	I > 0					
-72 (dBm)	I + Q > 0					
	Q > 0					
	I > 0				1	
Other Specify	I > 0					
(dBm)	I + Q > 0					
	Q > 0					
	I > 0	Noise observed		4.80/9.60	50.0	
	I > 0	4.80/9.60	50.0	4.68/9.60	48.8	100% at -72 dBm
-75 dBm	I + Q > 0	4.68/9.60	48.8	4.80/9.60	50.0	8 Bds / 1.80 μsec
	Q > 0	4.80/9.60	50.0	4.80/9.60	50.0	

End TEST: 18:46 (HHMM MN MSS)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 18:47 (HHMM MN MSS)

ANOMALY J12 SYNTH

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation (*minimum for cable losses)
50 min. drift	637.8	+0.8	(A) 994.3	-12.6	(A) Could be harmonic. Fundamental not found to 10 MHz.
35 min. drift	680.4	+12.0	(B) 995.0	-12.8	(B) Appears good at single freq as what happened w/ MSW 1030, however is >> in freq.
18 min. drift	755.4	+12.4	(B) 994.5	-12.7	
00 min. drift	823.2	+10.9	(B) 994.6	-12.7	

↑ Power stable/okay ↑ Low output is >> 921 MHz Bandwidth

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 19:14 (HHMM MN MSS)

Reload Plot Routine / Data Disk #2 @ 19:08 — 19:22.

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

RETURN TO LEVEL 6 (RETEST) End DWELL: 19:23 (HHMM MN MSS)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 1028 Test Date: 03/03/92

Tester: (Name & stamp below)

STEP-STRESS Level (zero 0 - 10): 7

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

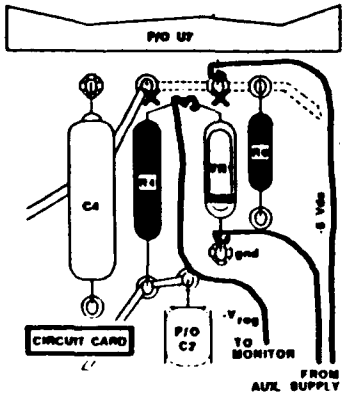
RESISTOR/ZENER DIODE MODIFICATION: At Thresh: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

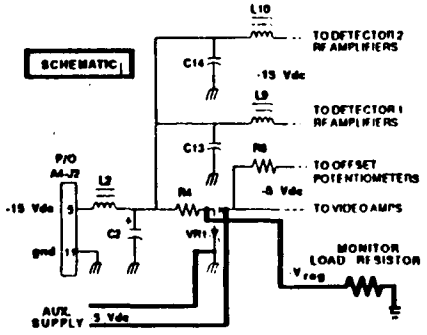
Start TEST: 19:14 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.1471 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 19:15 (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 6

UUT Serial Number (enter NSN): 1028 Test Date: 03/03/92

Tester: (Name & Initials below)

STEP-STRESS Level (enter 0 - 10): 6 (RETEST)

DECREASE FROM LEVEL 7 TO VERIFY SYNTH #2 (J11) ANOMALY.

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 19:23 (TIME HR MIN) MANUAL MODE Start DWELL: 19:53 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +110.1 (°C) TC1 (Chamber thermocouple reading) SOAK +111 °C

STEP-STRESS Level Component Temperature: +118 (°C) (Refer to Appendix B Table)

Plunge Temperature: +119.7 (°C) TC3 (Thermocouple reading)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +6.20 (Vdc) -5 Volts dc: -6.20 (Vdc)

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 19:54 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1506 (mA) Δ = +9 mA -5 Volts dc: 95.5 (mA) Δ = -1.9 mA

+15 Volts dc: 135.2 (mA) Δ = -1.9 mA -5 Volts dc: 577.0 (mA) Δ = -2.0 mA COMPARED TO PRIOR LEVEL 6

End TEST: 19:56 (TIME HR MIN) NO MAJOR DISCREPANCY w/ CURRENTS

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 6

UUT Serial Number (enter NSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 6 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Inputs	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1028 Test Date: 03/03/92

STEP-STRESS Level: 6 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued.

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q Data	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST (HHMM MS MM)

TEST continued on next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1028 Test Date: 03/03/92

STEP-STRESS Level: 6 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 20:00 (HHMM MS MM)

CHECK J12 ANOMALY

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *measured for cable losses
50	640.9	+2.6	626.6	-4.1	V = Component w/ power LE-01 6 03/03/92 @ 19 IN -19 VDC
35	684.5	+12.2	670.8	+12.5	
18	762.3	+12.6	787.0	+12.9	
00	834.2	+11.0	881.5	+11.4	

— NO FAILURE FOUND —

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 20:16 (HHMM MS MM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level

NO FAILURE PROCEED TO LEVEL B STRESS.

End DWELL 20:23 (HHMM MS MM)

(ELAPSED WAS 00:30 MM SS)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 1028 Test Date: 03/08/92

Tester: (Name & stamp below) 97166

STEP-STRESS Level: 6 (RETEST)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

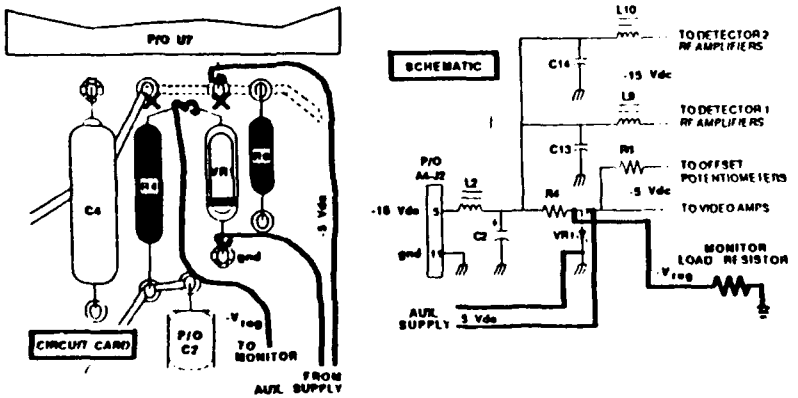
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 19:56 (Time HR:MIN)

Voltage across LOAD RESISTOR: -5.1320 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 19:56 (Time HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

Tester: (Please print name below)

STEP-STRESS Level (enter 0 - 10): 8

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 20:23 (HOUR HR MIN) Probe INPUT # 16 Start DWELL: 20:53 (HOUR HR MIN)

STEP-STRESS Level Chamber Air Temperature: +125.3 (°C) (Chamber thermocouple reading) Set @ +127°C

Flange Temperature: +135.0 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +134 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: -6.60 (Vdc)

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: -17.40 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1102 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 20:54 (HOUR HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1577 (mA) (PROCESSOR) -5 Volts dc: 85.9 (mA) # Below Level 6 and going to Level 7

+15 Volts dc: 100.0 (mA) # -15 Volts dc: 602.6 (mA) (INTERFACE)

End TEST: 20:59 (HOUR HR MIN) # For Below Level 7 & 6 by 22 mA

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 21:00 (HOUR HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	460/960	50.0%	460/960	50.0%	
	I > Q	"	50.0	468/960	48.8	8 div @ 1.20 usec/div
	I + Q > 0	"	50.0	480/960	50.0	
	Q > 0	468/960	48.8	"	50.0	
Other: Specify -72 (dBm)	I > 0	480/960	50.0*	448/960	46.7 / 46.5%	* was Low Q > 0
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Noise Below Level 7 Apply 50% Duty Cycle		480/960	50.0%	* was Low Q > 0
	I > Q	468/960	48.8%	468/960	48.8	6 div @ 1.60 usec/div
	I + Q > 0	"	48.8%	488/960	50.8%	
	Q > 0	468/960	48.8	480/960	50.0	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
	I > 0	480/9.60	50.02	480/9.60	50.0	Very clean both Data's 8 d.v. 1.60 usec/div
	I > Q	"	50.0	"	50.0	
0 dBm	I + Q > 0	"	50.0	"	50.0	
	Q > 0	"	50.0	480/9.60	50.0	
	I > 0	472/9.60	49.2	6 div 1.60 usec/div		
Other Specify	I > Q					
-72 (dBm)	I + Q > 0					
	Q > 0					
	I > 0					
Other Specify	I > Q					
(dBm)	I + Q > 0					
	Q > 0					
	I > 0	Looks like 5.10/9.60	53.3	480/9.60	50.0	
	I > Q	464/9.60	48.3	"	50.0	6 div 1.60 usec/div
-75 dBm	I + Q > 0	480/9.60	50.0	"	50.0	
	Q > 0	"	50.0	"	50.0	

End TEST: 21:17 (HHMM MM UNIT)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 21:20 (HHMM MM UNIT)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *account for cable losses
50 min	632.7 [632.7 ± 1.8]	-1.9 [-1.9 ± 1.5]	987.3	-12.5	Looking for harmonics to 1.6 GHz & 2.4 GHz
35 min	673.7 [673.7 ± 1.8]	-11.4 [-11.4 ± 1.5]	987.4	-12.5	
18 min	794.1	-12.3	987.2	-12.5	Same anomaly as Level 7. Will not Failure @ Level 6 retest. (Square 2 (J12)) No change in freq & power of appearance
00 min	804.5	-11.2	987.2	-12.4	

SINGLE OUTPUT

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

Exercise of Test #2 Frequency Sweep (J12) resulted in 1.6 GHz spikes.

End TEST: 21:38 (HHMM MM UNIT) ANOMALY IS KNOWN THIS UNIT

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

PROCEED TO LEVEL 9 STRESS End DWELL: 21:53 (HHMM MM UNIT)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 1028

Test Date: 03/03/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

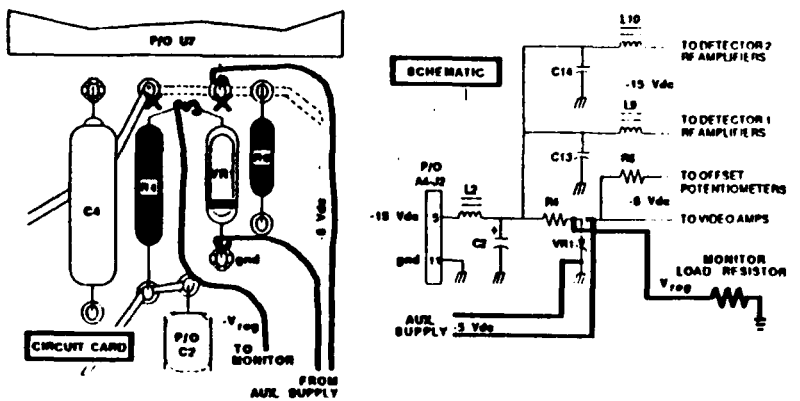
Start TEST: 20:53 (TIME RELATIVE)

Voltage across LOAD RESISTOR: -5.1598 (Vdc) (Refer to Appendix D; nominally 5 Vdc)

End TEST: 20:54 (TIME RELATIVE)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1028

Test Date: 03/03/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 9

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 21:53 (TIME HR MIN)

Start DWELL: 22:23 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +133.0 (°C) (Chamber thermocouple reading) TC1

Flange Temperature: +143.4 (°C) (Thermocouple reading) TC3

STEP-STRESS Level Component Temperature: +142 (°C) (refer to Appendix D Table)

Set @ +135°C

TC3 = +132.2

TC4 = 133.5

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +6.80 (Vdc) -5 Volts dc: -6.80 (Vdc)

+15 Volts dc: +17.70 (Vdc) -15 Volts dc: -17.70 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1103 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 22:23 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1657 (mA) -5 Volts dc: 98.2 (mA) (increasing again Known Anomaly from MSN 1030 & 1025)

+15 Volts dc: 1128 (mA) -15 Volts dc: 6144 (mA)

End TEST: 22:27 (TIME HR MIN) (increasing after 2:00 before end)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1028

Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Report with setting for Channels 00 at this STEP-STRESS Level.

Start TEST: 22:28 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (msec) / T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 t (msec) / T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50.0	4.68/960	48.8	
	I > Q	468/960	48.8	"	48.8	84.0 / 120 µsec/div
	I + Q > 0	480/960	50.0	4.80/960	50.0	
	Q > 0	"	50.0	"	50.0	
Other Specify -72 (dBm)	I > 0	480/960	50.0			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	NOISY		484/960	50.0	
	I > Q	480/960	50.0	"	50.0	6.0 / 120 µsec/div
	I + Q > 0	"	50.0	484/960	512	
	Q > 0	468/960	48.8	4.80/960	50.0	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number: 1028 Test Date: 03/03/92

STEP-STRESS Level: 9

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 604 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Lmed T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Lmed T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50.0	480/960	50.0	
	I > Q	468/960	48.8	468/960	48.8	Bdin
	I + Q > 0	480/960	50.0	480/960	50.0	
	Q > 0	"	50.0	"	50.0	
Other Specify -72 (dBm)	I > 0	468/960	48.8			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Very Noisy		480/960	50.0	
	I > Q	468/960	48.8	496/960	51.7	Ldin
	I + Q > 0	480/960	50.0	480/960	50.0	
	Q > 0	"	50.0	"	50.0	

End TEST: 22:39 (HH:MM AM/PM) OKAY Both Detectors

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number: 1028 Test Date: 03/03/92

STEP-STRESS Level: 9

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at the STEP-STRESS Level.

Start TEST: 22:40 (HH:MM AM/PM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *comment for cable losses
50 min	621.6 (3rd Rcv)	-7.3	951.3	-0.7	
	767.4 (1st Rcv)	+10.4	952.5	-1.1 (A)	(A) Power out increase
	8767.8	8.67 (B)			(B) Bi-modal at peak & drifting
35 mm	(C) 660.4	+9.1	952.0	-0.8	(C) Low in frequency
	1440	-23			
18 mm	721.6	+11.7	951.6	-0.8	
	1082	-50			
00 mm	(B) 766.6	+10.4	951.2	-0.7	
	711.4	-9.8			

Fixed Freq KNOWN ANOMALY Power is increasing as S/S-R comes back into bandwidth of VCO filter

Additional Testing (OPTIONAL): At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.
RADIO FREQUENCY OUTPUT TEST

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check one)

End TEST: 23:11 (HH:MM AM/PM)

	3rd Rcv (J5)	
50	660.3	+10.8
35	660.4	+9.2
18	721.4	+11.7
00	770.2	+10.4

DRIFT IN SYNTH #1 (J5) CH 50 & 00 IS ANOMALY. VARIES IN FREQ.

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

REVISIT LEVEL 8 TO LOOK @ SYNTH #1 CH 50 & 00 FREQUENCY End DWELL: 23 23 (HH:MM AM/PM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (from MSN): 1028

Test Date: 03/03/92

Tester: (Name & stamp in box)

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

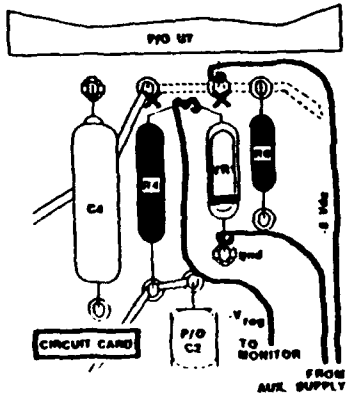
Start TEST: 22:27 (Hour Min Sec)

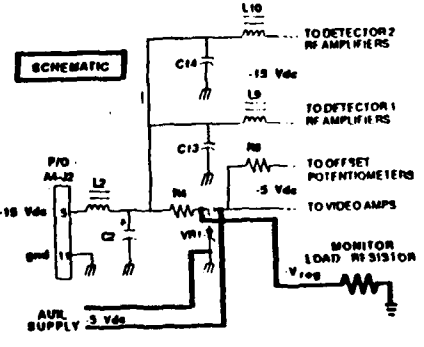
Voltage across LOAD RESISTOR: -5.1750 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 22:27 (Hour Min Sec)

003

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION FOR AUX. CONSTANT -5 Vdc SUPPLY AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

Tester: (Name & comp below) J.D. Mueller

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

VERIFY SYNTH #1 CH 50 @ 00 FREQ.

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 23:23 (HR:MN) Start DWELL: 23:53

STEP-STRESS Level Chamber Air Temperature: +125.9 (°C) Flange Temperature: +135.9 (°C)

STEP-STRESS Level Component Temperature: +134 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: -6.60 (Vdc)

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: -17.40 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1103 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 23:54 (HR:MN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 160.8 (mA) Δ = +2.7 mA -5 Volts dc: 85.1 (mA) Δ = -0.8 mA

+15 Volts dc: 104.3 (mA) Δ = +0.3 mA -15 Volts dc: 600.2 (mA) Δ = -2 mA

End TEST: 23:57 (HR:MN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: (HR:MN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz and -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ___ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ___ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03/92

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: (TIMP HR MIN)

TEST continued next page

202

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/03 - 03/04/92

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST. At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at the STEP-STRESS Level.

Start TEST: 23:58 (TIMP HR MIN) 03/03/92

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	6322 ✓	-2.03 ✓			✓ = checks w/ old data Lot 18 P 21 20 03/03/92
35 min	6735 ✓	+11.2 ✓			# used crystal — P 2778 = 2.18 from Lot GBU-127
18 min	7436 ✓	+12.2 ✓			
00 min	8038 ✓	+10.9 ✓	986 MHz (J12) ✓		

VERIFY ANOMALY J5 ONLY

Additional Testing (OPTIONAL); RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

NO FAILURE FOUND

End TEST: 00:08 (TIMP HR MIN) 03/04/92

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUE STEP-STRESS TEST WITH LEVEL 10 End DWELL: 00:10 (TIMP HR MIN)

ELAPSED TIME 00 17 HR MIN

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1028 Test Date: 03/04/92

Tester: (Please do not stamp the form)

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

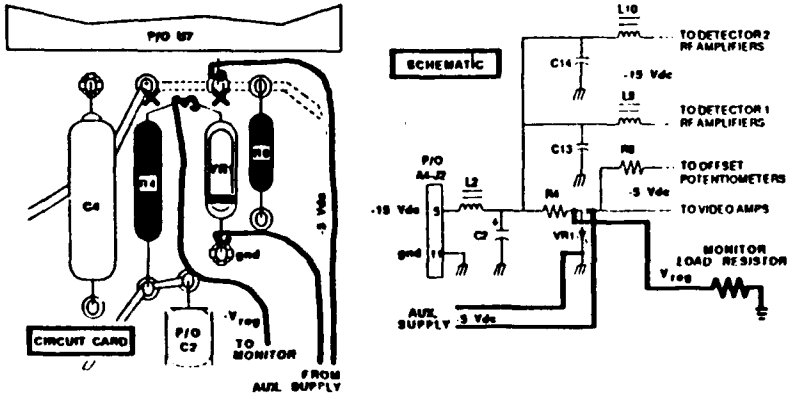
Start TEST: _____ (Hold 10 min)

Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: _____ (Hold 10 min)

203

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION FOR AUX. CONSTANT -5 Vdc SUPPLY AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/04/92

Tester: (Name & signature below)

STEP-STRESS Level (enter 0 - 10): 10 RUN WORST CASE

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 00:10 (TIME HR MIN) Start DWELL: 00:40 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +140.7 (°C) (Chamber thermocouple reading) Set To +143°C

Plunge Temperature: +151.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +150 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +7.0 (Vdc) -5 Volts dc: -7.0 (Vdc)

+15 Volts dc: +18.0 (Vdc) -15 Volts dc: +18.0 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1102 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 00:45 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1733 (mA) -5 Volts dc: 108.4 (mA)

+15 Volts dc: 1243 (mA) -15 Volts dc: 625.6 (mA) All Supply Currents Increased

End TEST: 00:46 (TIME HR MIN)

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 50 or 99 at this STEP-STRESS Level.

Start TEST: 00:50 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Data	Detector 1 I (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 I (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/9.60	50%	4.80/9.60	50.0	8 d.u (1.80 μm)
	I > Q	4.68/9.60	48.8	4.68/9.60	48.8	
	I + Q > 0	4.80/9.60	50.0	"	48.8	
	Q > 0	"	50.0	4.80/9.60	50.0	
Other Specify -72 (dBm)	I > 0	4.96/9.60	51.7			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	NOISE See Above		4.96/9.60	51.7	clear
	I > Q	4.8"/9.60	50.0	4.80/9.60	50.0	6 d.u (1.60 μm)
	I + Q > 0	"	50.0	4.96/9.60	51.7	
	Q > 0	4.96/9.60	51.7	"	51.7	

TEST Continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1028 Test Date: 03/04/92

STEP-STRESS Level: 10

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 464 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Bits	Detector 1 Limit T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/9.60	50.0	4.84/9.60	50.0	6 div. / 1.20 μsec
	I > Q	"	50.0	4.68/9.60	48.8	
	I + Q > 0	"	50.0	4.80/9.60	50.0	
	Q > 0	"	50.0	"	50.0	
Other Specify -72 (dBm)	I > 0	5.12/9.60	53.3%			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	NOISY		4.96/9.60	51.7	* 6 div. / 1.60 μsec
	I > Q	4.68/9.60	48.8	5.12/9.60	53.3	
	I + Q > 0	4.80/9.60	50.0	4.84/9.60	50.0	
	Q > 0	4.96/9.60	51.7	4.76/9.60	51.7	

End TEST: 01:00 (HH:MM MR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 1028 Test Date: 03/04/92

STEP-STRESS Level: 10

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 01:01 (HH:MM MR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation
50 min	607.0 / 911.7	-15.7 / -4.7	298.7 MAIN	+11.1	BOTH SYNTHS DRIFT w/ TIME
35 min	637.8	+1.17	782.1 MAIN	+11.2	
	955.2	-14.9			
	667.9	+10.4	986.0 MAIN	+11.2	→ #1 783@+11 dBm
	0.1001	-30.5			
	668.4	+11.5	785.5 MAIN	+10.7	→ 783@+10.8
	0.1030 6	-38.1			

SIMILIAR FIXED OUTPUTS

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box) OFF FREQ OUT OF SPAN MNA

End TEST: 01:21 (HH:MM MR MIN)

LEVEL 10 TEST COMPLETE

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

RETURN TO LEVEL 0 STRESSES End DWELL 01:40 (HH:MM MR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 1028 Test Date: 03/04/92

Tester: S D Mueller

STEP-STRESS Level: 10

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

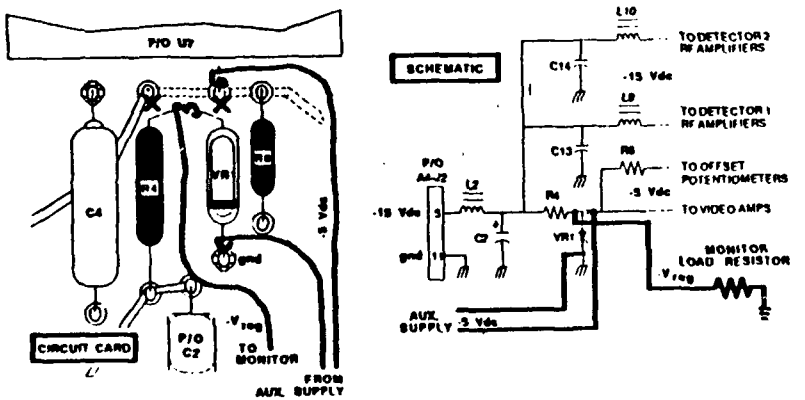
Start TEST: 00:43 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.1878 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 00:44 (TIME HR:MIN)

206

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/04/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0 FINAL

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 01:40 (HOUR HR:MIN) + 40-minute Ramp (02:20) + 30-minute Stabilization = Determined w/ thermocouple Start DWELL: 03:10 (HOUR HR:MIN)

STEP-STRESS Level Chamber Air Temperature: +68.3 (°C) (Chamber thermocouple reading) 50 + 18 = 68 F Flange Temperature: +68.3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +70 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +5.00 (Vdc) -5 Volts dc: -5.00 (Vdc)

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.00 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1101 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 03:10 (HOUR HR:MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1257.1 (mA) ✓ (A = +5) -5 Volts dc: 83.3 (mA) ✓ (A = +L)

+15 Volts dc: 113.3 (mA) ✓ (A = +5) -15 Volts dc: 501.8 (mA) ✓ (A = +L)

End TEST 03:12 (HOUR HR:MIN) NO FAILURE

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 1 of 4

UUT Serial Number (enter MSN): 1028 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: (HOUR HR:MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/9.60	50.0 ✓	4.80/9.60	50.0 ✓	
	I > 0	4.68/9.60	48.8 ✓	4.68/9.60	48.8 ✓	
	I + Q > 0	4.80/9.60	50.0 ✓	4.80/9.60	50.0 ✓ use C1	8 div / 1.20 usec/div
	Q > 0	"	50.0 ✓	"	50.0 ✓	T ✓
Other: Specify (dBm)	I > 0					
	I > 0					NO FAILURES
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.80/9.60	50.0 ✓	4.84/9.60	50.0 ✓	
	I > 0	4.68/9.60	48.8 ✓	"	50.0 use C1	
	I + Q > 0	4.80/9.60	50.0 ✓	4.92/9.60	51.2 ✓	
	Q > 0	4.80/9.60	50.0 ✓	4.80/9.60	50.0 ✓	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number (enter MSN): 1028 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q -Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/9.60	50.0 ✓	4.68/9.60	48.8 ✓	was 50
	I > Q	4.68/9.60	48.8 ✓	"	48.8 ✓	
	I + Q > 0	"	48.8 ✓	4.80/9.60	50.0 ✓	
	Q > 0	4.80/9.60	50.0 ✓	"	50.0	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					NO FAILURES
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.68/9.60	48.8 ✓	4.68/9.60	48.8 ✓	was 50
	I > Q	"	48.8 ✓	"	48.8 ✓	
	I + Q > 0	4.80/9.60	50.0 ✓	4.80/9.60	50.0 ✓	was 51
	Q > 0	"	50.0 ✓	"	50.0 ✓	

End TEST: 03:23 (HH:MM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number (enter MSN): 1028 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 03:23 (HH:MM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *measure for cable losses
50 (ch)	684.0	+12.4 ✓	684.0	+12.6 ✓	within ± 0.5 dB of set CH00 Synth #1 (J5) is LOW power
35 (ch)	728.9	+12.3 ✓	728.9	+11.9 ✓	
18 (ch)	824.9	+12.1 ✓	825.0	+12.1 ✓	
00 (ch)	921.0	+10.1 OKay 0 to 9 PASSES	921.0	+12.0 ✓	NO FAILURES

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 03:53 (HH:MM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

UNIT PASSES ALL TEST WITHOUT FAILURE End DWELL 04:10 (HH:MM)

D. Mueller 03/04/92

STEP-STRESS LEVEL COMPLETE

Ramp to Room Temp Program = 9, Level = 3 UUT power off @ 04:30 (HH:MM) 03/04/92

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter S/N): 1028 Test Date: 03/04/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

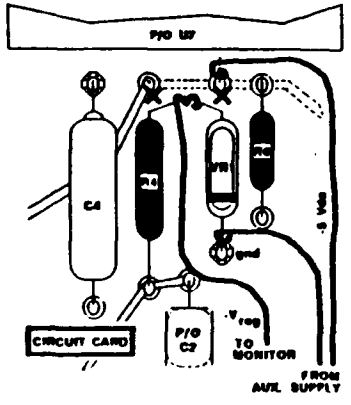
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

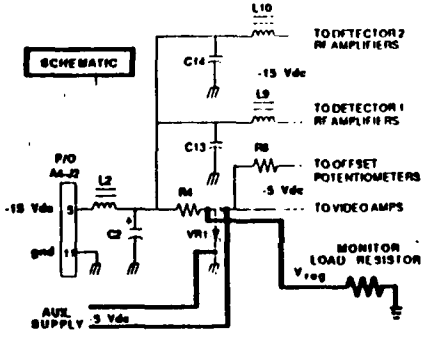
Start TEST: 03:10 (Hour:Minute)

Voltage across LOAD RESISTOR: -5.0373 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 03:10 (Hour:Minute)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 1028

LEVEL Ø FINAL
03/04/92 03:27

Power at J5 is 12.3 dBm @ 684.0 MHz (Spec=+9dBm minimum). ✓
Power at J5 is 11.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 693.0 MHz (Spec=+9dBm minimum). — Measured as +10.6 dBm PASS
Power at J5 is 11.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 729.0 MHz (Spec=+9dBm minimum). ✓
Power at J5 is 12.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.3 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 825.0 MHz (Spec=+9dBm minimum). ✓
Power at J5 is 11.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 921.0 MHz (Spec=+9dBm minimum). ✓

NO FAILURES

210

STEP-STRESS TEST

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 1028

LEVEL Ø FINAL
03/04/92 @ 03:44

Power at J12 is 12.2 dBm @ 684.0 MHz (Spec=+9dBm minimum). +12.6
Power at J12 is 10.7 dBm @ 687.0 MHz (Spec=+9dBm minimum). Measured
Power at J12 is 3.8 dBm @ 690.0 MHz (Spec=+9dBm minimum). +10.5 ✓
Power at J12 is 3.8 dBm @ 693.0 MHz (Spec=+9dBm minimum). +10.4 ✓
Power at J12 is 7.6 dBm @ 696.0 MHz (Spec=+9dBm minimum). +10.9 ✓
Power at J12 is 1.9 dBm @ 699.0 MHz (Spec=+9dBm minimum). +11.6 ✓ 1004
Power at J12 is -3.5 dBm @ 702.0 MHz (Spec=+9dBm minimum). +11.9 ✓
Power at J12 is -2.2 dBm @ 705.0 MHz (Spec=+9dBm minimum). +10.6 ✓
Power at J12 is 9.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 720.0 MHz (Spec=+9dBm minimum). +11.4 ✓
Power at J12 is 10.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 729.0 MHz (Spec=+9dBm minimum). +11.9 dBm ✓
Power at J12 is 11.4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 735.0 MHz (Spec=+9dBm minimum). +12.1 dBm ✓
Power at J12 is 11.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 741.0 MHz (Spec=+9dBm minimum). +11.7 ✓
Power at J12 is 10.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 759.0 MHz (Spec=+9dBm minimum). ALL PASSES
Power at J12 is 9.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 825.0 MHz (Spec=+9dBm minimum). +12.1 dBm ✓
Power at J12 is 8.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 834.0 MHz (Spec=+9dBm minimum). +12.3 ✓
Power at J12 is 9.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 921.0 MHz (Spec=+9dBm minimum). → +12.0 dBm ✓

Noise on cursors may hinder display on read. Check freq count for detection

NO FAILURES

TEST EQUIPMENT & CALIBRATION LOG

Maintain Log for testing conducted 03/02/92 (date) through 03/06/92 (date)

Item	DESCRIPTION	Manuf. & Part No.	ID NUMBER	LAST CAL*	CAL* DUE	Item Notes
01	T/R Test Station	HAC; SPECIAL	F-A15723		NCR	G-132043
02	Control Panel	HAC; SPECIAL	G-132290		NCR	
03	Signal Generator	HP; 8660C	G-128061	12-17-91	01-13-93	
04	Auxiliary Section	HP; 86631B	G-128062		NCR	P/O ITEM 03
05	RF Section	HP; 86603A	G-128063	12-17-91	01-13-93	P/O ITEM 03
06	Spectrum Analyzer	HP; 8568A w/ Opt E16	G-132082	12-11-91	10-30-92	
07	FET Probe	HP; 1120A	G-132055	12-14-90	04-30-92	PWR CAL
08	Power Meter	HP; 436A	G-128036	06-18-91	12-24-92	"
09	Power Sensor	HP; 8482A	G-128059	09-09-91	10-21-92	"
10	Oscilloscope	HP; 1980B	G-132047	09-24-91	08-11-92	
11	Digital Multimeter	SystronDonner; 7344A	G-127998	06-06-91	08-18-92	
12	Digital Multimeter	HP; 3478A	H-AS3624	09-06-91	06-25-92	
13	Power Splitter	MiniCkts; ZFSC-2-5	No ID ✓		NCR	
14	Power Splitter	MiniCkts; ZFSC-2-5	No ID ✓		NCR	
15	Reg. Power Supply	Lambda; LP-531-FM	G-132292		NCR	+15V
16	Reg. Power Supply	Lambda; LP-531-FM	"		NCR	-15V
17	Reg. Power Supply	Lambda; LP-530-FM	G-132291		NCR	+5V
18	Reg. Power Supply	Lambda; LP-520-FM	"		NCR	-5V
19	Computer	HP; 9845B	G-128012		NCR	
20	Flex. Disk Memory	HP; 9895A	G-133306		NCR	
21	Signal Generator					
22	Oscilloscope	Tektronix; 2465				
23	Digital Multimeter					
24	Digital Multimeter					
25	Digital Multimeter					
26	Thermal Chamber	Thermotron; S-4 w/Cntl	H-B07567	09-18-91	09-02-92	
27	Data Acqtn Cntl Unit	HP; 3497A	H-428499	12-19-91	07-29-93	
28	Computer	HP, Model 85	H-A64929		NCR	
29	Power Supply, AUX.	HP; 6299A	H-357054		NCR	-5.1V
30	PLOTTER	HP; 7470A	H-512478		NCR	
31	PRINTER	HP; THINKJET	E-A08763		NCR	
32						
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						

*NCR = No Calibration Required

CALIBRATION ROUTINE PERFORMED. 03-02-92; 15.52 PRIOR TO TEST.

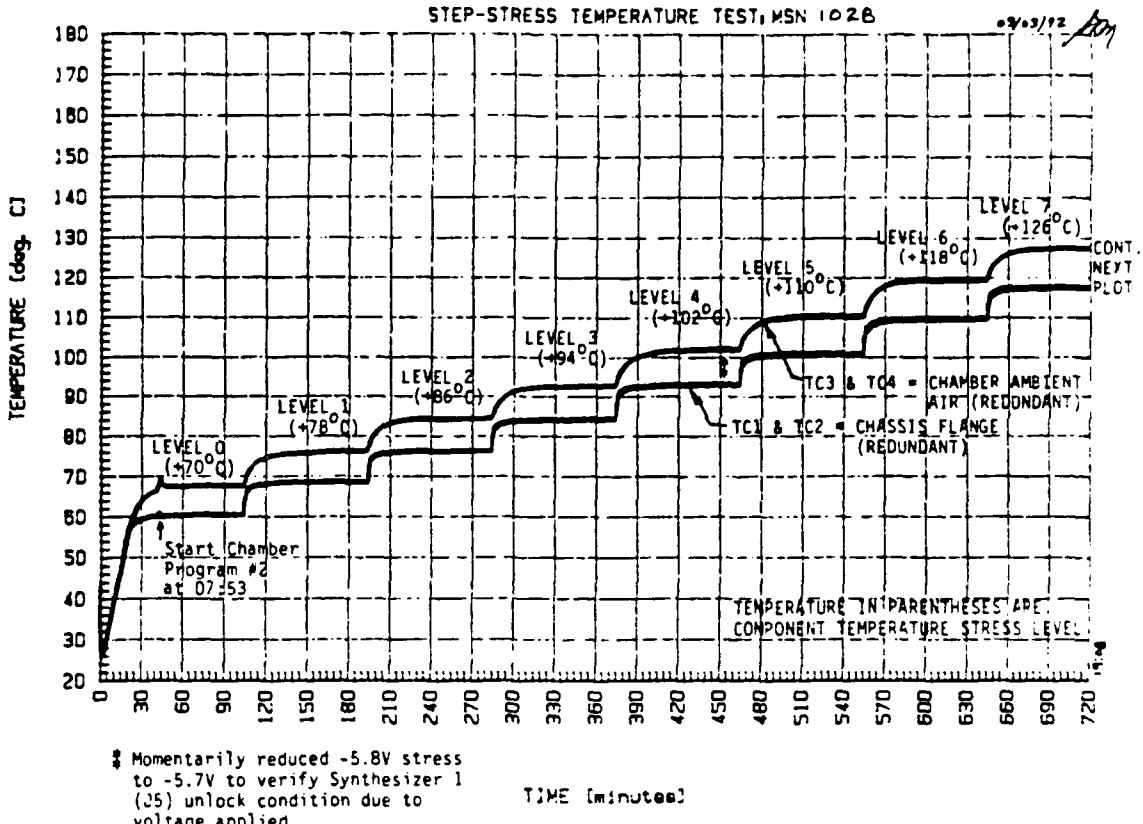
211

DATE: [redacted] TIME: [redacted]
03/02/92 15:52

STEP-STRESS TEST CALIBRATION DATA
(CHECKS 38 & 312)

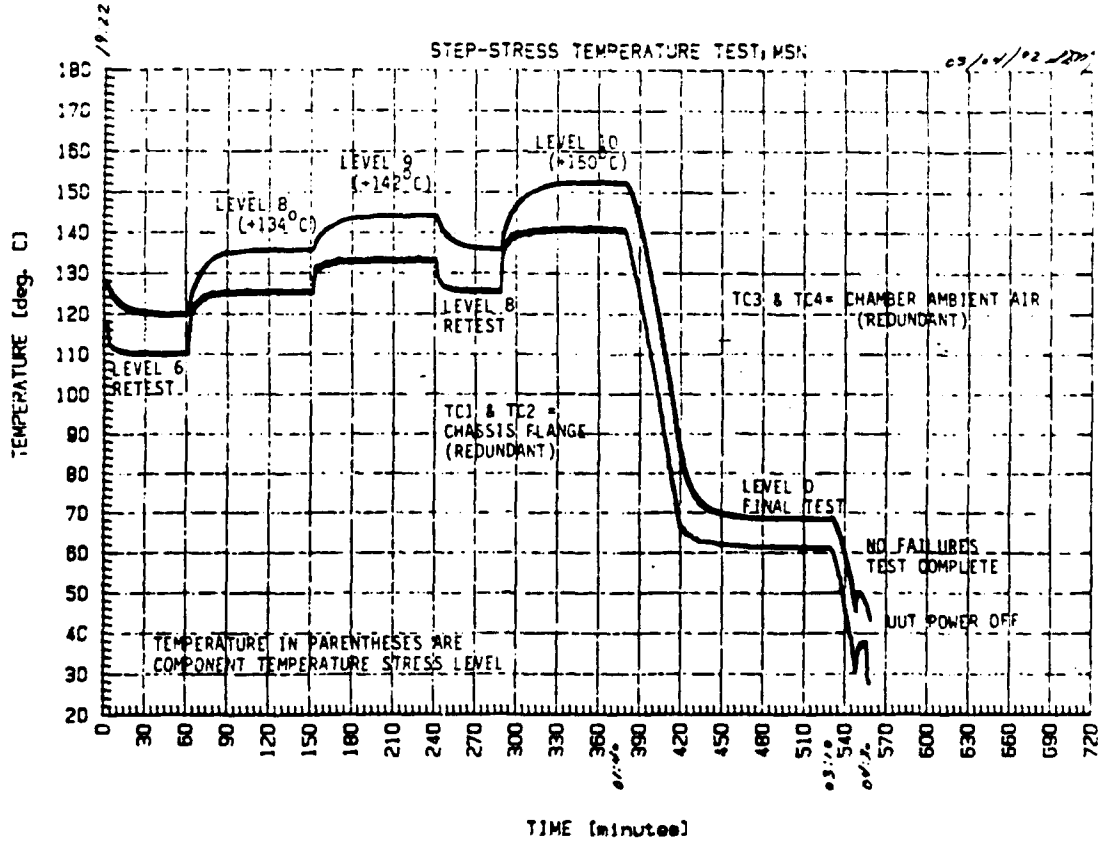
Synth_ref= 1499990
Freq_mod_ref= 9999980
Sp_clock_output = 0
Phase_lo_output = 1.12
Phase_if_output = 0
Up_dn_conv_lo = 3.37
313.75_lo = 14.9 dBm /313.75177E6MHz

Channel	Freq	Dn_conv_output	Synth_lo_output	Hit_sgnl_l_o
50	684	1.2	1.27	2.17
49	687	1.19	1.17	2.13
48	690	1.18	1.12	2.11
47	693	1.21	1.23	2.11
46	696	1.28	1.37	2.03
45	699	1.34	1.4	1.92
44	702	1.39	1.3	1.89
43	705	1.44	1.32	1.95
42	708	1.41	1.39	1.96
41	711	1.37	1.4	1.88
40	714	1.32	1.36	1.88
39	717	1.32	1.43	1.92
38	720	1.38	1.59	1.91
37	723	1.43	1.67	1.82
36	726	1.45	1.66	1.75
35	729	1.44	1.63	1.79
34	732	1.41	1.71	1.88
33	735	1.39	1.76	1.89
32	738	1.32	1.74	1.79
31	741	1.31	1.74	1.8
30	744	1.36	1.81	1.84
29	747	1.45	1.92	1.84
28	750	1.47	1.95	1.71
27	753	1.44	1.9	1.69
26	756	1.44	1.93	1.82
25	759	1.44	2	1.88
24	762	1.43	2	1.83
23	765	1.44	1.95	1.78
22	768	1.51	1.97	1.8
21	771	1.62	2.1	1.92
20	774	1.67	2.18	1.76
19	777	1.66	2.14	1.7
18	825	1.84	2.32	1.68
17	828	1.77	2.29	1.67
16	831	1.72	2.29	1.73
15	834	1.69	2.29	1.78
14	837	1.69	2.31	1.73
13	882	1.65	2.08	1.64
12	885	1.7	2.06	1.65
11	888	1.69	2.07	1.58
10	891	1.72	2.05	1.48
9	894	1.76	2.02	1.51
8	897	1.79	1.99	1.52
7	900	1.71	1.98	1.5
6	903	1.59	1.95	1.43
5	906	1.6	1.89	1.49
4	909	1.66	1.9	1.56
3	912	1.65	1.88	1.53
2	915	1.55	1.91	1.45
1	918	1.52	1.89	1.44
0	921	1.58	1.79	1.53



* Momentarily reduced -5.8V stress to -5.7V to verify Synthesizer 1 (J5) unlock condition due to voltage applied.

STEP-STRESS TEST MSN 1028
BEGIN TEST: 03/03/92
PLOT 1 OF 2



STEP-STRESS TEST MSN 1028
CONTINUE: 03/03 THRU 03/04/92
PLOT 2 OF 2

Test Data Cont'd: Date 3-2-92

Rec'd unit MSN 1028 FOR
Level 10 testing. S. Mueller will
Set-up test in [redacted] LAB. Test will
commence 0700hrs, 3-3-92 (DA)

03/02/92
18:40 - LOAD "HIT LOG" SET DAY/TIME & FORMAT NEW DISK

ESTABLISH: CHANNEL 1 TC1 (Chamber air forside)
CHANNEL 2 TC2 (Chamber air near to door)
CHANNEL 3 TC3 (Flange near door / J11 & J12)
CHANNEL 4 TC4 (Flange forside / J5 & J4)

18:51 - RUN TEST PLOT TO VERIFY TC TRACKING MSN 1028.

20:10 - REPLACED PLOTTER PEN (RIGHT). VERIFICATION RUN OKAY.

- LOAD "HIT LOG" SET DAY/TIME & REFORMAT THIS DISK SAME TC ASSIGNMENT AS ABOVE. LEFT FOR LINDY TO HIT <ENDLINE> AND LOG BELOW

03/03/92 07:08 LDM for pht
07:13 - BEGIN TEMPERATURE PLOT.

07 13 Start transition to 61°C
07 53 Start Dwell 61°C & Prog #2 Int #1 stress level 0
08 53 Stress level 0 Complete Start stress level #1
09 23 Dwell @ 69°C stress level #1
10:23 Stress level #1 Complete Start stress level #2
10 53 Dwell @ 77°C
11 53 stress level #2 Complete Start stress level #3
12 23 Dwell @ 85
13 23 Stress level #3 Complete Start stress level #4
13 53 Dwell @ 99°C

Data Recorder

Test Data Cont'd: STEP-STRESS TEST HSN 1028 Date 3-3-92

14:33 J5 output Brute lock readjusted -5V supply to -5.1Vdc from -5.8Vdc. J5 output back to normal
14:55 stress level #10 complete Start stress level #5
15:23 - Start Level 5 Dwell, set @ +102°C. D. Mueller 03/03/92
16:23 - End tests/Dwell. Ramp to Level 6.
16:53 - Start Level 6 Dwell, set @ +111°C
17:53 - End tests/Dwell. Ramp to Level 7.
18:23 - Start Level 7 Dwell, set @ 119°C.
19:04 - Found Anomaly Synth #2 (J12) @ LEVEL 7.
Freq is FIXED AT 994 MHz POWER AT -12.7 dBm
WILL RETEST AT LEVEL 6 AT END OF DWELL
19:08 - T20 SCANS COMPLETE. RELOAD PLOT ROUTINE.
BEGIN DATA DISK #2 MDM
19:12 - DISK #2 FORMATTING. VERIFIED TIME
19:22 - SCAN 001 BEGINS. PLOT 2 BEGINS
19:23 - RAMP DOWN TO LEVEL 6 FOR ANOMALY TEST. (MINIMAL NOISE) PRIOR DWELL COMPLETED
19:53 - BEGIN TEST/DWELL AT LEVEL 6, SET @ +111°C WITH RETEST NO FAILURES FOUND
20:23 - LEVEL 6 RETEST COMPLETE. RAMP TO LEVEL 8 (PROGRAM #2, INTERVAL #16.
20:53 - Start Level 8 Dwell, set @ +127°C.
21:53 - End tests/Dwell Ramp to Level 9.
22:23 - Start Level 9 Dwell, set @ +135°C
23:11 - Anomaly w/ Synth #1 (J5) Drift of CH 50 & 100 frequencies needs closer look.
23:23 - End tests/Dwell Ramp back to Level 8 (Manually) to verify anomaly.
23:53 - Begin Tests @ Level 8 (Retest) Synth #1, set @ +127°C

Data Recorder D. Mueller

Test Data Cont'd: STEP-STRESS TEST MSN 1028 Date: 03/04/92

00:10 - No Failure found @ Level B retest
Ramp to Level 10 (Prog#2, Intvl#20), set @ +143°C

00:40 - Start Dwell Level 10, set @ +143°C

01:40 - TEST COMPLETE LEVEL 10
Return to LEVEL 0. Prog#2 Intvl#22 (40-minutes)
~~Reduce V-stress incrementally over~~ Ramp.

02:10 - UNIT STABLE LEVEL 0. Begin 1-Hour Dwell

03:10 - Test/Dwell Complete. Ramp Program #3, Intvl#3 to Room Temp (18-minutes).

04:30 - UUT power OFF. TEST COMPLETE.

04:37 - OPENED CHAMBER.

04:40 - LOAD NEXT PLOT FOR A.M TEST
NEXT UNIT.

Data Recorder ADM

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STEP-STRESS TEST DATA NOTEBOOK

UNIT UNDER TEST: MSN 0172

TEST STATUS: FAILURE CONFIRMED

(DURING LEVEL 9 DWELL)

TEST SUMMARY

STEP-STRESS		START DWELL	ANOMALY/ FAILURE	END DWELL
		4-Mar-92		
LEVEL	0	6:45		7:45
LEVEL	1	8:15		9:15
LEVEL	2	9:45		10:45
LEVEL	3	11:15		12:15
LEVEL	4	12:45		13:45
LEVEL	5	14:15		15:15
LEVEL	6	15:45		16:45
LEVEL	7	17:15		18:15
LEVEL	8	18:45		19:45
LEVEL	9	20:15	Anomaly	21:15
FAILURE			20:38	
Retest	8	21:45		22:20
Final Test	0	23:35		0:35
		4-Mar-92		5-Mar-92

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0

UUT PWR ON @ 05:30 Room Temp

Returned Station Calibration of 03/02/92 @ 15:52 MDM
Maintained Cal Equipment Log

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 05:35 (TIME HR MIN) (Proc #1 / NVLAP #1) Start DWELL: 06:45 (TIME HR MIN) (Proc #2 / NVLAP #1)

Room Temp

STEP-STRESS Level Chamber Air Temperature: +60.9 (°C) (Chamber thermocouple reading) Set @ +61°C

Flange Temperature: +67.6 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +70 (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +5.00 (Vdc) -5 Volts dc: -5.00 (Vdc)

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.00 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1096 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 06:45 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1220.2 (mA) -5 Volts dc: 78.3 (mA)

+15 Volts dc: 119.7 (mA) -15 Volts dc: 499.0 (mA)

End TEST: 06:46 (TIME HR MIN)

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 0 MDM

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input From 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 30 at this STEP-STRESS Level.

Start TEST: 06:51 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (min)	Detector 1 Duty Cycle (percent)	Detector 2 T (min)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/9.60	50.0	4.80/9.60	50.0	8 dBi @ 20 mm/Hr
	I > 0	"	50.0	"	50.0	
	I + Q > 0	"	50.0	"	50.0	JEFL
	Q > 0	"	50.0	4.68/9.60	48.8	
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.80/9.60	50.0	4.80/9.60	50.0	
	I > Q	"	50.0	"	50.0	
	I + Q > 0	5.04/9.60	52.5	"	50.0	
	Q > 0	4.92/9.60	51.2	"	50.0	

TEST Continued on next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number (xxxx MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (zero 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q -Bits	Detector 1 Limit T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.84/9.60	50.0	4.80/9.60	50.0	
	I > Q	"	50.0	"	50.0	
	I + Q > 0	4.92/9.60	51.2	"	50.0	
	Q > 0	4.84/9.60	50.0	3.04/9.60	52.5	
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.92/9.60	51.2	4.84/9.60	50.0	
	I > Q	4.80/9.60	50.0	"	50.0	
	I + Q > 0	4.92/9.60	51.2	"	50.0	
	Q > 0	4.80/9.60	50.0	4.92/9.60	51.2	

End TEST: 06:58 (HHMM MM MM)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number (xxxx MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (zero 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 07:06 (HHMM MM MM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations
50 min	684	12.27	684	11.87	*measure for cable losses; pwr measured first dip
35 min	729	12.13	684	10.83	Max hold then peak
18 min	825	12.12	825	12.62	Signal < 12d above
00 min	921	11.6	921	11.2	15 sec

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 07 20 (HHMM MM MM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at the STEP-STRESS Level.

End DWELL: 07:45 (HHMM MM MM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 172

Test Date: 03/04/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA

PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

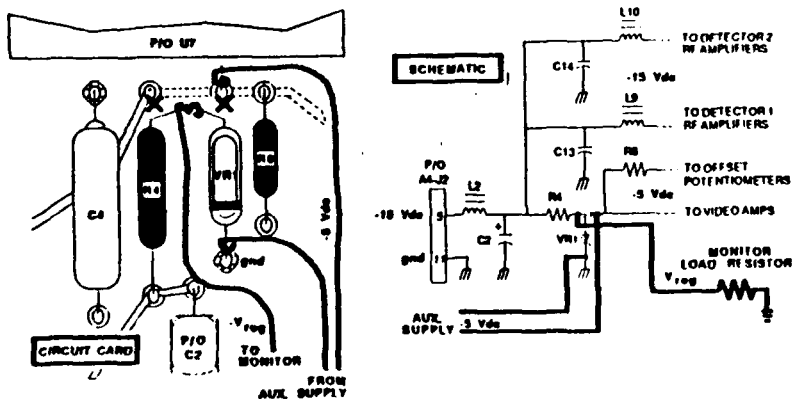
Start TEST: 06:47 (Time HR:MIN)

Voltage across LOAD RESISTOR: -5.3860 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 06:48 (Time HR:MIN)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/4/92
sn [redacted] #172
stress level 0
J5 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is-.1 dBm @ 687.9 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-5.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 8.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 4.2 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 3.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 3.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).

****

2 2 2

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 11.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 687.9 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/4/92
synthesizer U172
stress level 0
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 7.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 4.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 702.0 MHz which is above the specified frequency.
Power at J12 is 1.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 708.0 MHz which is above the specified frequency.
Power at J12 is 2.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than 711.0 MHz which is below the specified frequency.
Power at J12 is 2.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is less than 714.0 MHz which is below the specified frequency.
Power at J12 is 4.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is less than 717.0 MHz which is below the specified frequency.
Power at J12 is 2.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 723.0 MHz which is above the specified frequency.
Power at J12 is 6.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.8 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 172

Test Date: 3/4/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 1

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 07:45 (TIME HR MIN)

Start DWELL: 08 15 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 68.7 (°C) 154.7 °F (Chamber thermocouple reading)

Flange Temperature: 75.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: N (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +5.2 (Vdc) -5 Volts dc: -5.2 (Vdc)

+15 Volts dc: +15.3 (Vdc) -15 Volts dc: -15.3 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 08 24 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 126 (mA) -5 Volts dc: 41 (mA)

+15 Volts dc: 121 (mA) -15 Volts dc: 511 (mA)

End TEST: 08 25 (TIME HR MIN)

TEST continued next page

22.1

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172

Test Date: 3/4/92

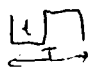
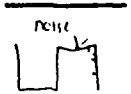
STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (1/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 08:25 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Data	Detector 1 L (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.8us/9.6us	50	4.8us/9.6us	50	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	"	"	4.85us/9.6us	48.8	
Other Specify -72 (dBm)	I > 0	4.92us/9.6us	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		4.8us/9.6us	50	noise 
	I > Q	4.80us/9.6us	500	"	"	
	I + Q > 0	5.04us/9.6us	52.5	"	"	
	Q > 0	4.8us/9.6us	50	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

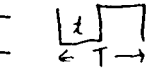
STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz. Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q -Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.8us/9.6us	50	4.8us/9.6us	50	
	I > Q	"	"	"	"	
	I + Q > 0	4.924us/9.6us	51.2	"	"	
	Q > 0	4.6us/9.6us	50	4.6us/9.6us	48.8	
Other Specify -7 (dBm)	I > 0	4.924us/9.6us	51.1			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		4.8us/9.6us	50	
	I > Q	4.6us/9.6us	50	"	"	
	I + Q > 0	4.924us/9.6us	51.1	"	"	
	Q > 0	4.6us/9.6us	50	"	"	



End TEST: 08 40 (HHMM MS MSH)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 08 40 (HHMM MS MSH)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *account for cable losses
50 min	684	12.27	684	11.77	
35 min	739	12.33	739	10.83	
18 min	825	12.02	825	12.62	
00 min	921	11.8	921	11.1	

Additional Testing (OPTIONAL); RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 08:52 (HHMM MS MSH)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 09 15 (HHMM MS MSH)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number (enter MSN): 172

Test Date: 3/4/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

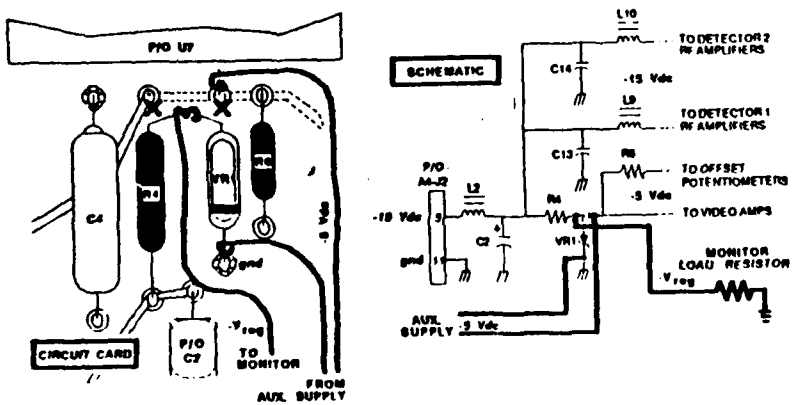
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 08 52 (HH:MM:SS)

Voltage across LOAD RESISTOR: -5.41 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 08 53 (HH:MM:SS)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/4/92
synthet #17L
stress level 1
J5 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 6.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 3.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 4.8 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 4.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.6 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is .2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

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Power at J5 is 12.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is .2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/4/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders. sn 1 at 4172

Stress level 1
J12 output

****

Power at J12 is 5.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 3.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 693.0 MHz which is above the specified frequency.
Power at J12 is 2.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 696.0 MHz which is above the specified frequency.
Power at J12 is 6.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 705.0 MHz which is above the specified frequency.
Power at J12 is 2.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 708.0 MHz which is above the specified frequency.
Power at J12 is-2.4 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is less than 714.0 MHz which is below the specified frequency.
Power at J12 is 5.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Frequency is less than 720.0 MHz which is below the specified frequency.
Power at J12 is-3.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is less than 723.0 MHz which is below the specified frequency.
Power at J12 is .8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 726.0 MHz which is above the specified frequency.
Power at J12 is 6.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 763.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.4 dBm @ 634.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.4 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is .8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.3 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 000's): 172 Test Date: 3/4/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 2

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 09:15 (Hour Hr Min) Start DWELL: 09:45 (Hour Hr Min)

STEP-STRESS Level Chamber Air Temperature: 76.3 (°C) Plenge Temperature: 81.6 (°C)
(Chamber thermocouple reading) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 56 (°C)
(refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp, Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: +5.4 (Vdc) - 5 Volts dc: -5.4 (Vdc)

+15 Volts dc: +15.6 (Vdc) -15 Volts dc: -15.6 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 09:45 (Hour Hr Min)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1501 (mA) - 5 Volts dc: 94 (mA)

+15 Volts dc: 122 (mA) -15 Volts dc: 525 (mA)

End TEST: 09:46 (Hour Hr Min)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 000's): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 09:46 (Hour Hr Min)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50	480/960	50	
	I > 0	"	"	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	"	"	465/960	48.5	
Other Specify -12 (dBm)	I > 0	492/960	51.2			
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		480/960	50	
	I > 0	480/960	50	"	"	
	I + Q > 0	504/960	525	"	"	
	Q > 0	480/960	50	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Inputs	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.8us/9.6us	50	4.8us/9.6us	50	
	I > Q	"	"	"	"	
	I + Q > 0	4.8/9.6us	51.2	"	"	
	Q > 0	4.8us/9.6us	50	4.8us/9.6us	48.8	
Other: Specify -7V (dBm)	I > 0	4.8us/9.6us	51.1			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q				1	
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		4.8us/9.6us	50	
	I > Q	4.8us/9.6us	50	"	"	
	I + Q > 0	4.8us/9.6us	51.1	"	"	
	Q > 0	4.8us/9.6us	50	"	"	

End TEST: 10:00 (Hour and Min)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 10:00 (Hour and Min)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *accounts for cable losses
50 min	684	12.27	684	11.67	
35 min	729	11.73	729	10.53	
18 min	825	12.33	825	12.5V	
00 min	921	11.5	921	11.2	

Additional Testing (OPTIONAL), RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 10:12 (Hour and Min)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 10:45 (Hour and Min)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number (enter 1xxx): 172

Test Date: 3/4/92

Tester: (Name & stamp in box)

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

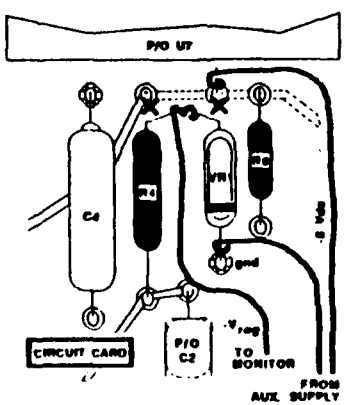
RESISTOR/ZENER DIODE MODIFICATION: At Dock: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

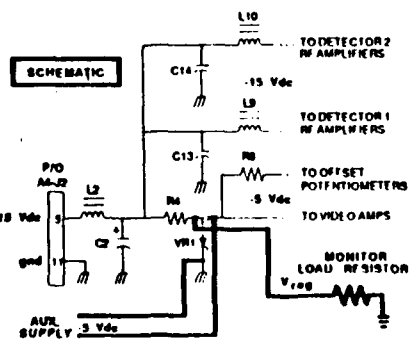
Start TEST: 10 12 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.43 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 10 13 (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





3/4/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Synth Ref. M172

stress test 2 JS output

```
**********************************************************************
Power at J5 is 6.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is .6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is .1 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-4.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 3.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 8.6 dBm @ 921.0 MHz (Spec=+9dBm minimum).
**********************************************************************
```

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

2332

```
Power at J5 is 12.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is .6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is .1 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 921.0 MHz (Spec=+9dBm minimum).
```

3/4/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

sym 10 & 17 L

stress level 1 2

J12 output

****

Power at J12 is 8.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 696.0 MHz which is above the specified frequency.
Power at J12 is 2.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 699.0 MHz which is above the specified frequency.
Power at J12 is-4.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 705.0 MHz which is above the specified frequency.
Power at J12 is 1.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 708.0 MHz which is above the specified frequency.
Power at J12 is 2.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than 711.0 MHz which is below the specified frequency.
Power at J12 is 1.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is less than 714.0 MHz which is below the specified frequency.
Power at J12 is 4.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Frequency is less than 720.0 MHz which is below the specified frequency.
Power at J12 is 4.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is less than 726.0 MHz which is below the specified frequency.
Power at J12 is 7.2 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is .8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

23.3

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is .8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 999): 172 Test Date: 3/4/97

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 3

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 10 45 (TIME HR MIN) Start DWELL: 11 15 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 54, 3 / 54.35 (°C) (Chamber thermocouple reading) Plenum Temperature: 32.2 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 44 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 15.6 (Vdc) -5 Volts dc: -5.6 (Vdc)

+15 Volts dc: +15.9 (Vdc) -15 Volts dc: -15.9 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 11 22 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 124 (mA) -5 Volts dc: 87 (mA)

+15 Volts dc: 115 (mA) -15 Volts dc: 53.6 (mA)

End TEST: 11 32 (TIME HR MIN)

TEST continued next page

234

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 999): 172 Test Date: 3/4/97

ST STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 11 25 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Data	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	48.4 / 96.4	49.8	48.4 / 96.4	50	
	I > 0	48.4 / 96.4	50	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	"	"	48.4 / 96.4	48.8	
Other Specify -12 (dBm)	I > 0	48.4 / 96.4	50			
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1.446 / 2.892	missing	48.4 / 96.4	50	
	I > 0	48.4 / 96.4	50	"	"	
	I + Q > 0	1.926 / 3.846	51.2	"	"	
	Q > 0	46.4 / 92.6	49.8	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q - Bits	Detector 1 L (nsec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (nsec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	496 ns/96 us	45.5	496 ns/96 us	50	
	I > Q	496 ns/96 us	50	"	"	
	I + Q > 0	496 ns/96 us	51.2	"	"	
	Q > 0	368 ns/96 us	48.8	496 ns/96 us	48.8	
Other: Specify (dBm)	I > 0	496 ns/96 us	50			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		496 ns/96 us	50	
	I > Q	496 ns/96 us	50	"	"	
	I + Q > 0	496 ns/96 us	51.2	"	"	
	Q > 0	496 ns/96 us	49.2	"	"	

End TEST: 11:45 (must be after)

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 11:43 (must be after)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *account for cable losses
50 min	684	12.0	684	11.3	
35 min	727	11.9	727	10.6	
18 min	825	12.2	825	11.2	
00 min	921	11.3	921	10.5	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 12:10 (must be after)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 12:15 (must be after)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 172

Test Date: 3/11/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

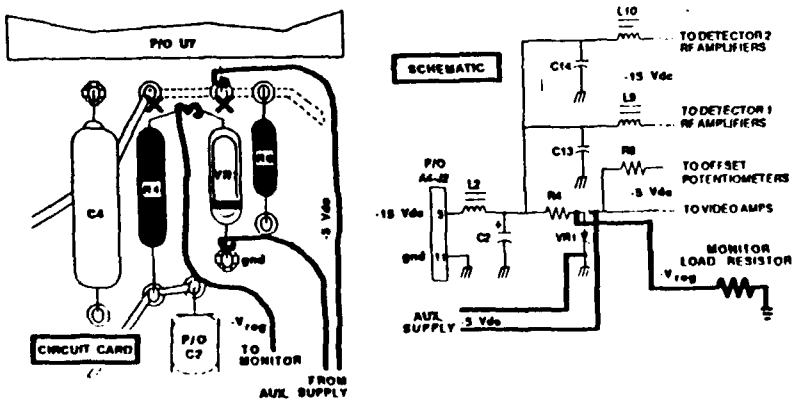
RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 12.61 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.16 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 12:0 ✓ (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/4/92
syn Def # 172
stress Level 3
JS output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 6.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 1.4 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-7.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 2.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 6.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-3.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is .7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 915.0 MHz (Spec=+9dBm minimum).

****

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 11.8 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-7.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is .7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/4/92
Sun Ref. #172
Stress level 3
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 4.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 4.4 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than 693.0 MHz which is below the specified frequency.
Power at J12 is-6.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is less than 696.0 MHz which is below the specified frequency.
Power at J12 is-2.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 699.0 MHz which is above the specified frequency.
Power at J12 is 3.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is less than 702.0 MHz which is below the specified frequency.
Power at J12 is 2.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 705.0 MHz which is above the specified frequency.
Power at J12 is .7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is less than 708.0 MHz which is below the specified frequency.
Power at J12 is 1.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is less than 714.0 MHz which is below the specified frequency.
Power at J12 is 4.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Frequency is less than 720.0 MHz which is below the specified frequency.
Power at J12 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is less than 828.0 MHz which is below the specified frequency.
Power at J12 is 4.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 10.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter NSN): 172 Test Date: 3/4/92

Tester: (Name & comp below)

STEP-STRESS Level (enter 0 - 10): 4

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 12 15 (TIME HR MIN) Start DWELL: 12:45 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 93.6 (°C) Flange Temperature: 100.7 (°C)
(Chamber thermocouple reading) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 102 (°C)
(refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 15.4 (Vdc) -5 Volts dc: -5.1 (Vdc)

+15 Volts dc: +16.2 (Vdc) -15 Volts dc: -16.2 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 13:00 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1.84 (mA) -5 Volts dc: 46 (mA)

+15 Volts dc: 125 (mA) -15 Volts dc: 5.48 (mA)

End TEST: 13:01 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter NSN): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (1/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 13:01 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L(max) T (max)	Detector 1 Duty Cycle (percent)	Detector 2 L(max) T (max)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	468ns/9.6us	48.8	488ns/9.6us	50	
	I > Q	488ns/9.6us	50	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	"	"	468ns/9.6us	48.8	
Other: Specify -17 (dBm)	I > 0	488ns/9.6us	50			
	I > Q	488ns/9.6us	50			
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1.4us	noisy	488ns/9.6us	50	
	I > Q	1.4us	noisy	"	"	
	I + Q > 0	488ns/9.6us	50	"	"	
	Q > 0	468ns/9.6us	48.8	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (xxx-xxx): 172 Test Date: 3/4/92

STEP-STRESS Level (zero 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q -Bits	Detector 1 L(max) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L(max) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.8us/9.6us	48.8	4.8us/9.6us	50	
	I > Q	4.8us/9.6us	50	"	"	
	I = Q > 0	4.92us/9.6us	51.2	"	"	
	Q > 0	4.8us/9.6us	48.8	4.8us/9.6us	49.9	
Other: Specify -12 (dBm)	I > 0	4.8us/9.6us	50			
	I > Q					
	I = Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I = Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		4.8us/9.6us	50	
	I > Q	4.8us/9.6us	50	"	"	
	I = Q > 0	"	"	"	"	
	Q > 0	4.8us/9.6us	48.8	"	"	

End TEST: 13 14 (HHMM MR MIN)

TEST continued next page

2.4(1)

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (xxx-xxx): 172 Test Date: 3/4/92

STEP-STRESS Level (zero 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 13 14 (HHMM MR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *measure for cable losses
50 min	684	12.0	684	11.27	
35 min	725	11.35	724	10.4	
18 min	825	11.82	825	11.92	
00 max	921	10.8	921	10.2	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 13 25 (HHMM MR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 15 45 (HHMM MR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 172

Test Date: 3/4/92

Tester: (Name & signature)

STEP-STRESS Level (enter 0 - 4): 4

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dock: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

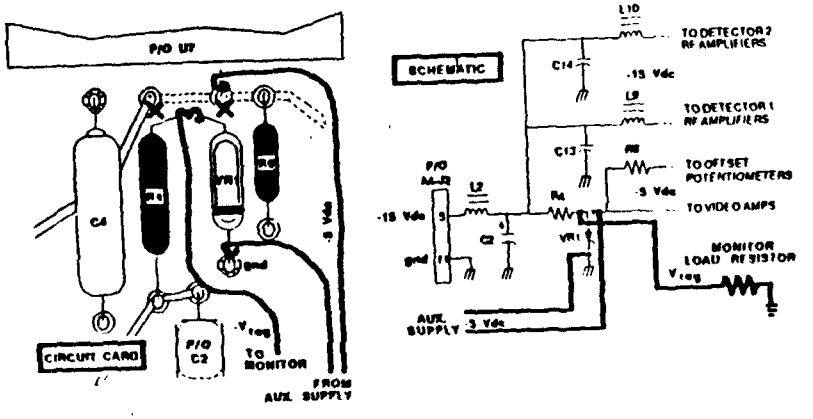
Start TEST: 13 25 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.49 (Vdc) (refer to Appendix D: nominally 5 Vdc)

End TEST: 13 26 (TIME HR MIN)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/4/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Gun/Def #172

Stress Level 4

J5 output

****

Power at J5 is 5.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 2.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-4.0 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is .0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is .1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted]er. 8

Power at J5 is 11.6 dBm @ 634.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.0 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is .0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is .1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.9 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/4/92
Syn/DC #H172
stress level 4
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 3.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-11.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is less than 699.0 MHz which is below the specified frequency.
Power at J12 is .5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 708.0 MHz which is above the specified frequency.
Power at J12 is-.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than 711.0 MHz which is below the specified frequency.
Power at J12 is-8.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is less than 714.0 MHz which is below the specified frequency.
Power at J12 is 1.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is less than 717.0 MHz which is below the specified frequency.
Power at J12 is 2.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 720.0 MHz which is above the specified frequency.
Power at J12 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 732.0 MHz which is above the specified frequency.
Power at J12 is 6.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.3 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.3 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 768.0 MHz which is above the specified frequency.
Power at J12 is 8.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Frequency is less than 894.0 MHz which is below the specified frequency.
Power at J12 is 5.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 10.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-11.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is-8.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.3 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.3 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

Tester (Name & county below): (illegible)

STEP-STRESS Level (enter 0 - 10): 5

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 13 45 (Hour Hr Min) Start DWELL: 14 15 (Hour Hr Min)

STEP-STRESS Level Chamber Air Temperature: 100.4 (°C) 42°C 102 Plenge Temperature: 107.5 (°C)

STEP-STRESS Level Component Temperature: 110 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: +6.0 (Vdc) - 5 Volts dc: -6.0 (Vdc)

+15 Volts dc: +16.5 (Vdc) -15 Volts dc: -16.5 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 14 20 (Hour Hr Min)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 141.9 (mA) - 5 Volts dc: 91 (mA)

+15 Volts dc: 127 (mA) -15 Volts dc: 56.2 (mA)

End TEST: 14 20.15 (Hour Hr Min)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -.75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or 1 this STEP-STRESS Level.

Start TEST: 14 40 (Hour Hr Min)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -.75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.6us/16us	48%	4.6us/16	50	
	I > Q	4.6us/16us	50	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.6us/16us	48%	4.6us/16us	48.5	
Other Specify (dBm)	I > 0	4.6us/16us	50			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-.75 dBm	I > 0	little noisy		4.8us/16us	50	
	I > Q	4.8us/16us	50	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	4.8us/16us	48	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 484 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L (msec) T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 L (msec) T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	484/484	48.8	484/484	50	
	I > Q	484/484	48.8 50	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	484/484	48.8	484/484	48.8	
Other Specify -11 (dBm)	I > 0	484/484	50			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	484/484		484/484	50	
	I > Q	484/484	50	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	484/484	48.8	484/484	48.8	

End TEST: 10:72 (HH:MM:SS)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 172 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 14:31 (HH:MM:SS)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *minimum for cable losses
50 min	6:84	11.57	6:84	5.21	
35 min	729	11.03	729	9.13	
18 min	825	10.92	825	10.72	
00 min	921	10.6	921	9.7	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 14:50 (HH:MM:SS)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

End DWELL: 15:15 (HH:MM:SS)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 172

Test Date: 3/4/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

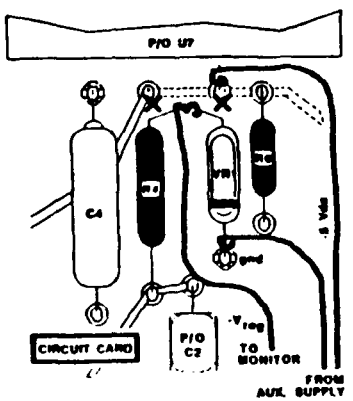
RESISTOR/ZENER DIODE MODIFICATION: As Built: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

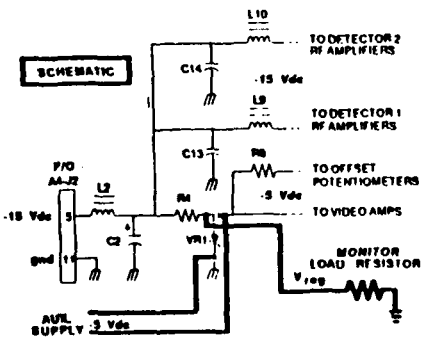
Start TEST: 14:20 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.5 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 14:30:36 (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





3/11/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Syn/Ref 4.172

Stress Level 5

J5 Output

****

Power at J5 is 7.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-2.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-3.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 7.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is .7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 5.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 2.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.5 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is .7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.5 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

3/4/92
Syn/Det. # J12.
Stress level 5
J12 output

****

Power at J12 is-2.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 684.0 MHz which is above the specified frequency.
Power at J12 is 6.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is .0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 696.0 MHz which is above the specified frequency.
Power at J12 is-7.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 699.0 MHz which is above the specified frequency.
Power at J12 is 1.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 705.0 MHz which is above the specified frequency.
Power at J12 is 5.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is less than 708.0 MHz which is below the specified frequency.
Power at J12 is-8.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than 711.0 MHz which is below the specified frequency.
Power at J12 is 2.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is less than 717.0 MHz which is below the specified frequency.
Power at J12 is-.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 726.0 MHz which is above the specified frequency.
Power at J12 is 3.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 741.0 MHz which is above the specified frequency.
Power at J12 is 7.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 753.0 MHz which is above the specified frequency.
Power at J12 is-1.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 771.0 MHz which is above the specified frequency.
Power at J12 is 5.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 828.0 MHz which is above the specified frequency.
Power at J12 is 8.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 831.0 MHz which is above the specified frequency.
Power at J12 is 2.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 834.0 MHz which is above the specified frequency.
Power at J12 is 6.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 837.0 MHz which is above the specified frequency.
Power at J12 is 4.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-7.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is less than 891.0 MHz which is below the specified frequency.
Power at J12 is-5.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 897.0 MHz which is above the specified frequency.
Power at J12 is 3.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is less than 906.0 MHz which is below the specified frequency.
Power at J12 is 2.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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FULL PRINT-OUT OF Power Output and Frequency [redacted]ser. 0

Power at J12 is-2.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is .0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-7.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-8.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-7.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 3 digits): 172

Test Date: 3/4/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 6

STEP-STRESS LEVEL DATA

PLOT PENS DAIED OUT WILL GET B ARMSTRONG TO REPLOT FROM DATA DISK 03/10/92

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 15:15 (TIME HR:MIN)

Start DWELL: 15:45 (TIME HR:MIN)

STEP-STRESS Level Chamber Air Temperature: +109.8 (°C) (Chamber thermocouple reading) 58°.111

Flange Temperature: +118.7 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 118° (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 4.25 (Vdc) -5 Volts dc: -6.20 (Vdc)

+15 Volts dc: +16.50 (Vdc) -15 Volts dc: -16.50 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 15:47 (TIME HR:MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1462 (mA) -5 Volts dc: 87.6 (mA)

+15 Volts dc: 133.6 (mA) -15 Volts dc: 582.1 (mA)

End TEST: 15:49 (TIME HR:MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 3 digits): 172

Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with settings for Channels 50 at this STEP-STRESS Level.

Start TEST: 15:53 (TIME HR:MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Data	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.68/4.60	48.8	4.80/4.60	50.0	
	I > Q	4.80/4.60	50.0	"	50.0	8 div / 1.20 μsec
	I + Q > 0	4.92/4.60	51.2	"	50.0	
	Q > 0	4.80/4.60	50.0	4.68/4.60	48.8	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.92/4.60	51.7	4.80/4.60	50.0	
	I > Q	4.80/4.60	50.0	"	50.0	1 div / 160 μsec
	I + Q > 0	"	50.0	"	50.0	
	Q > 0	4.92/4.60	49.2	4.80/4.60	50.8	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/02

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Lowest T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Lowest T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.48/4.60	48.8	4.80/4.60	50.0	
	I > Q	4.52/4.60	51.2	"	50.0	8 d.i
	I + Q > 0	"	51.2	"	50.0	
	Q > 0	4.80/4.60	50.0	4.42/4.60	48.8	
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0				1	
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.56/4.60	51.7	4.56/4.60	51.7	
	I > Q	4.80/4.60	50.0	4.80/4.60	50.0	16 d.i
	I + Q > 0	"	50.0	"	50.0	
	Q > 0	4.42/4.60	48.3	"	50.0	

End TEST: 16:03 (HHMM MM SEC)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/02

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST. At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 16:04 (HHMM MM SEC)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*comment for cable losses (See cal data table observation #3))
50	618.0 (Nom: 926.9)	-29.5 / -2.1	629.7 (Nom: 944.5)	-9.3 / -15.0	
35	667.7 (Nom: 1001.4)	+7.4 / -29.3	678.8 (Nom: 1018)	+11.2 / -37	Offset from Ch. freq is consistent with prior tests observed Synth being pulled off freq by voltage. Spectrum is present & locked
18	752.8 (Nom: none)	+13.2	760.4 (Nom: 1140)	+12.9 / -50	
00	828.2 (Nom: none)	+13.6	837.4 (Nom: none)	+13.4	

Additional Testing (OPTIONAL); **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input to Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

ANOMALY IS KNOWN OBSERVATION No FAILURES

OFF FREQ. Not visible in MMR Bottom set up spec

End TEST: 16:30 (HHMM MM SEC)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUE TO LEVEL 7 End DWELL 16:45 (HHMM MM SEC)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 172 Test Date: 03/04/92

Tester: A.D. Mueller

STEP-STRESS Level: 6

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

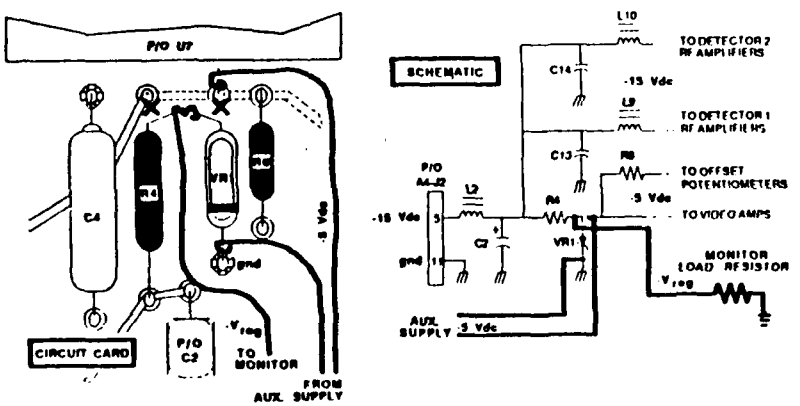
Start TEST: 15:51 (military time)

Voltage across LOAD RESISTOR: -5.5256 (Vdc) (refer to Appendix D; nominally -5 Vdc)

Aux supply: -5.1095

End TEST: 15:52 (military time)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 3 digits): 172 — Test Date: 03/04/92

Tester: (Name & stamp below) A.D. Mueller

STEP-STRESS Level (enter 0 - 10): 7

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 16.45 (TTMP HR MIN) — Start DWELL: 17.15 (TTMP HR MIN)

STEP-STRESS Level Chamber Air Temperature: +117.6 (°C) (Chamber thermocouple reading) Sat @ +119 — TC1

Flange Temperature: +127.0 (°C) (Thermocouple reading) — TC3

STEP-STRESS Level Component Temperature: +126 (°C) (refer to Appendix D Table) — TC2: 116.9, TC4: 126.7

VOLTAGE STEP-STRESS During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +6.40 (Vdc) — -5 Volts dc: -6.40 (Vdc)

+15 Volts dc: +1710 (Vdc) — -15 Volts dc: -1710 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.1096 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 17.18 (TTMP HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1506 (mA) — -5 Volts dc: 872 (mA) holding decreasing 0.4 mA

+15 Volts dc: 123.9 (mA) — -15 Volts dc: 5996 (mA)

End TEST: 17.21 (TTMP HR MIN) decreasing 10 mA — KNOWN ANOMALY

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 3 digits): 172 — Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with settling for Channels 50 at this STEP-STRESS Level.

Start TEST: 17.22 (TTMP HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	456/960	47.5	480/960	50.0	
	I > 0	480/960	50.0	"	50.0	8 div 1.20 usec/
	I + Q > 0	"	50.0	"	50.0	
	Q > 0	460/960	48.8	465/960	48.8	
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	480/960	50.0	486/960	50.8	
	I > Q	"	50.0	"	50.8	6 div 1.60 usec/
	I + Q > 0	"	50.0	480/960	50.0	
	Q > 0	472/960	49.2	480/960	50.0	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter HEX): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Lmsec T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 Lmsec T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.68/9.60	48.8	4.80/9.60	50.0	
	I > 0	4.80/9.60	50.0	4.92/9.60	51.2	8 div / 1.20 msec
	I + Q > 0	"	50.0	"	51.2	
	Q > 0	"	50.0	4.68/9.60	48.8	
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.56/9.60	51.7	4.80/9.60	50.0	
	I > 0	4.72/9.60	49.2	"	50.0	6 div / 1.60 msec
	I + Q > 0	4.88/9.60	50.8	4.72/9.60	49.2	
	Q > 0	4.72/9.60	49.2	4.80/9.60	50.0	

End TEST: 17:30 (HH:MM MM DD)

TEST continued next page

Reloaded plot 17:32 – 17:47 by Brian Armstrong. Began Test #7, Plot #2

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter HEX): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 17:36 (HH:MM MM DD)

Channel		Synthesizer 1 (J3) Frequency (MHz)	Synthesizer 1 (J3) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *compensate for cable losses
50 min	18°	656.2	-3.3	(A) 945.7	+3.7	(A) Probably is the harmonic
35 min	(B) 6°	669.0 harm: 1003.4	+7.7 -3.1	948.1	+4.6	(B) Below bandwidth of Filter & VCO; Decreasing Power Output
18 min	4°	734.8 harm: none	+13.7	947.4	+4.9	(C) Decreased power output Above bandwidth of Filter & VCO
00 min	119	804.2 harm: none	+13.5	948.8	+3.9	

SINGLE FREQUENCY & POWER ANOMALY SIGNAL REMAINS LOCKED (C)

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

Signals are locked & present. ANOMALIES are KNOWN from prior testing (MSNs 1030, 1028, 1029)

off freq out of ISSUE analyze upon

NO FAILURES

Need to watch J12 Power on Input while freq pulling.

End TEST: 18:03 (HH:MM MM DD)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at the STEP-STRESS Level.

PROCEED TO LEVEL 8

End DWELL 18:15 (HH:MM MM DD)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (refer MSPR): 172

Test Date: 03/04/92

Tester: (Name & stamp or sign)

STEP-STRESS Level (refer 6.4.10): 7

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

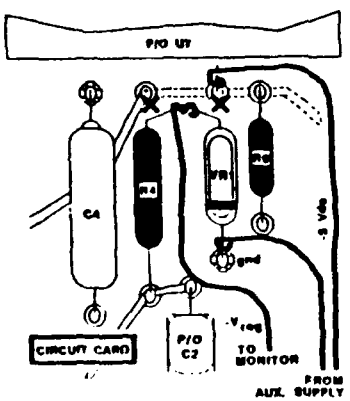
Start TEST: 17:31 (HHMM MIL MSR)

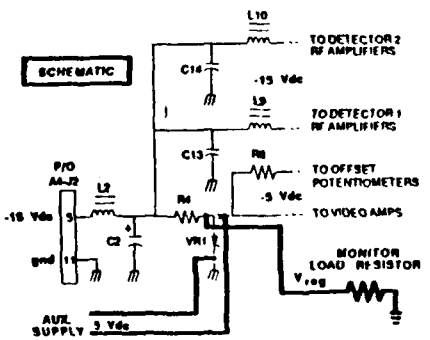
Voltage across LOAD RESISTOR: -5.5486 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 17:31 (HHMM MIL MSR)

25.1

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter legibly): 172

Test Date: 03/04/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 8

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 18:15 (TIME HR MIN)

Start DWELL: 18:45 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +126.3 (°C) (Chamber thermocouple reading) Set Point 127 °C

Flange Temperature +135.1 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +134 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: -6.60 (Vdc)

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: -17.40 (Vdc)

Ave. Constant - 5 Volts dc Setting: -5.1097 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 18:47 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1542.1 (mA) -5 Volts dc 97.1 (mA) increasing after

+15 Volts dc: 130.5 (mA) -15 Volts dc 617.3 (mA)

End TEST 18:50 (TIME HR MIN) increasing after

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter legibly): 172

Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input Power 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with settling for Channels 50 at this STEP-STRESS Level.

Start TEST: 18:50 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	464/960	48.8	468/960	48.8	8 d.u. / 1.20 usec
	I > Q	"	48.8	"	48.8	
	I + Q > 0	492/960	51.2	"	48.8	
	Q > 0	496/960	48.8	"	48.8	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	496/960	46.7	496/960	51.7	
	I > Q	464/960	48.3	480/960	50.0	6 d.u. / 1.60 usec
	I + Q > 0	496/960	51.7	"	50.0	
	Q > 0	"	51.7	488/960	50.8	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 404 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.56/5.60	47.5	4.80/9.60	50.0	
	I > 0	4.80/9.60	50.0	"	50.0	8 dio
	I + Q > 0	"	50.0	4.92/9.60	51.2	
	Q > 0	"	50.0	4.68/5.60	48.8	
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.96/9.60	51.7	4.80/9.60	50.0	
	I > 0	4.80/9.60	50.0	"	50.0	
	I + Q > 0	4.88/9.60	50.8	"	50.0	6 dio
	Q > 0	4.80/9.60	50.0	"	50.0	

End TEST: 19:00 (HHMM MS MSS)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 19:01 (HHMM MS MSS)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *corrected for cable losses
50 (HEX)	879.1 very Stable	+12.3	919.0	+10.4	Increase to 1.6 dBm span Measure @ 15 MHz span
35 (HEX)	877.8	+12.4	918.8	+10.4	
18 (HEX)	876.6	+12.4	917.3	+10.2	Power increased since lock freq is now in bandwidth.
00 (HEX)	877.3	+12.4	918.7	+10.3	

Both to First Freq Lock Manually. Will not Hop

Additional Testing (OPTIONAL); RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

Execute UUT with Test #2 Freq Sweep
Rapid hop to & programmable
Fixed Freq Lock discovery confirmed.
Both Synthesizers affected.

End TEST: 19:32 (HHMM MS MSS)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

PROCEED to LEVEL 9 End DWELL 19:45 (HHMM MS MSS)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 172

Test Date: 03/04/92

Tester:

STEP-STRESS Level: 8

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

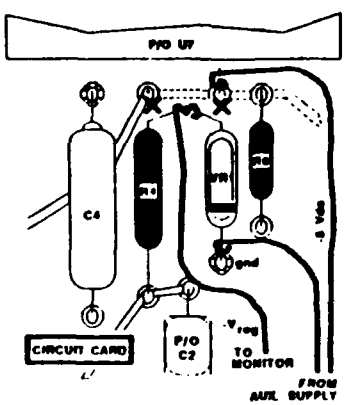
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

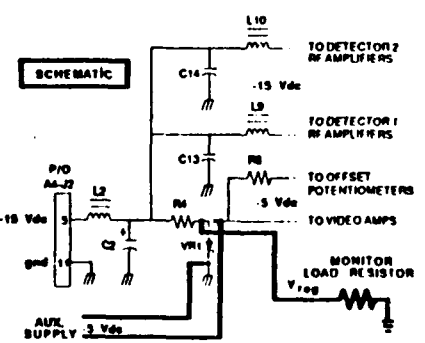
Start TEST: 18:47 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.5715 (Vdc) (refer to Appendix D, nominally 1 Vdc)

End TEST: 18:47 (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter NSN): 172 Test Date: 03/04/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 9

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 19:45 (TTMM HR MIN) Start DWELL: 20:15 (TTMM HR MIN)

STEP-STRESS Level Chamber Air Temperature: +133.1 (°C) (Chamber thermocouple reading) 56 to 135

Plenge Temperature: +113.3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +112 (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.80 (Vdc) -5 Volts dc: -6.80 (Vdc)

+15 Volts dc: +17.70 (Vdc) -15 Volts dc: -17.70 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1097 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 20:25 (TTMM HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 160.8 (mA) -5 Volts dc: 99.6 (mA)

+15 Volts dc: 130.6 (mA) -15 Volts dc: 63.48 (mA)

End TEST 20:28 (TTMM HR MIN) Same for Lamb 9

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter NSN): 172 Test Date: 03/04/92 (0.166)

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -.75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with testing for Channels 50 at this STEP-STRESS Level.

Start TEST: 20:28 (TTMM HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -.75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.56/9.60	47.5	4.56/9.60	47.5	8 div / 1.20 usec/div
	I > 0	4.68/9.60	48.8	4.68/9.60	48.8	
	I + Q > 0	"	48.8	"	48.8	
	Q > 0	"	48.8	4.56/9.60	47.5	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-.75 dBm	I > 0	4.92/9.60	51.7	4.92/9.60	51.7	6 div / 1.60
	I > 0	4.80/9.60	50.0	"	51.7	
	I + Q > 0	4.92/9.60	51.7	4.88/9.60	50.8	
	Q > 0	"	51.7	"	50.8	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Lowest T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Lowest T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > Q					
	I > Q					
	I < Q > 0					Power Supply ANOMALY 5 VOLT 8 div 1.20 mv/div
	Q > 0					7+5
Other Specify (dBm)	I > Q					
	I > Q					
	I < Q > 0					
	Q > 0					
Other Specify (dBm)	I > Q					
	I > Q					
	I < Q > 0					
	Q > 0					
-75 dBm	I > Q					
	I > Q					CH 00 & 50 Affected Both Detectors 6 div 1.60 mv/div
	I < Q > 0					
	Q > 0					

End TEST (hour hr min)

No output Detectors 1 & 2 @ 20:38 output is +4.88 Volts

Cycle -5V Supply @ 20:42 No Change

-5 Volt Supply @ -0.977V and 2.91 Amps +15V Supply decreased to 11.2 mA

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 20:45 (THUR HR MIN) AFFECTED BY ANOMALY

-5 VOLT POWER SUPPLY ANOMALY OCCURRING

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *Measured for cable losses
50 (hex)	975.0	-8.5	1023.5	-22.0	Both Synths drifting Lower by 2+ MHz
35 (hex)	974.8	-8.6	1024.3	-22.1	
18 (hex)	972.9	-7.7	1022.6	-21.6	100 MHz to 1.6 GHz Span Marker @ 15 MHz Span
00 (hex)	974.0	-8.3	1024.0	-22.1	

FIXED FREQ

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 20:59 (THUR HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

REDUCE STRESS FOR RETEST AT LEVEL 8

End DWELL: 21:15 (THUR HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 172 Test Date: 03/04/22

Tester: [signature]

STEP-STRESS Level: 9

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 20:21 (HHMM MILITARY)

Voltage across LOAD RESISTOR: -5.596 (Vdc) (refer to Appendix D, nominally -5 Vdc)

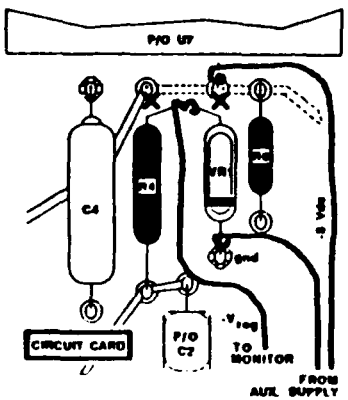
End TEST: 20:22 (HHMM MILITARY)

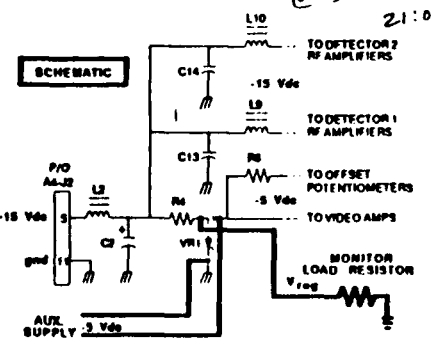
Aux Supply Not effected by -5 Volt Supply Anomaly 20:57 JDY

Aux Supply Current measured w/ HP 3478A @ 55.8 mAdc 21:03 JDY

2611

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter last 3 digits): 172 Test Date: 03/04/92

Tester: (Name & stamp below) L.D. Mueller

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 21:15 (Manual mode) (HHMM HR MIN) Start DWELL: 21:45 (HHMM HR MIN)

STEP-STRESS Level Chamber Air Temperature: +125.6 (°C) (Chamber thermocouple reading) Set @ +127°C

Flange Temperature: +135.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +134 (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: -6.60 (Vdc) Should be but IS -0.948 Volts 21:20

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: -17.40 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.1096 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 21:45 (HHMM HR MIN) FAILURE

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1505.5 (mA) Δ = -36.6 mA -5 Volts dc: 2.826 Amps

+15 Volts dc: 111.3 (mA) Δ = -19.2 mA -15 Volts dc: 607.3 (mA) Δ = -10 mA

End TEST: 21:47 (HHMM HR MIN) See Aux Supply Supplement.

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter last 3 digits): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 50 as this STEP-STRESS Level.

Start TEST: 21:50 (HHMM HR MIN) Detectors still railed at +4.96 Vdc Disconnect Detector multipin connector from Station (10,5). Measure -6.64 Vdc @ 44.6 mA

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Data	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					DETECTOR HAS SHORT 21:56
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					End 21:57
	I > 0					
	I + Q > 0					Leave disconnected. Return to Level 0
	Q > 0					
Other Specify (dBm)	I > 0					FAILURE L.D. Mueller 03/04/92
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					22:17
	I > 0					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Sign	Detector 1 Count T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Count T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					SEE SHEET 2
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: 21:57 (hour and min)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 21:57 (hour and min) W/ DETECTOR CONNECTOR DISCONNECTED

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation (*measure for cable losses)
50 min	878.1	+12.4	918.3	+10.3	SYNTH'S CHECK W/ PRIOR LEVEL 8
35 min	877.3	+12.3	918.4	+10.2	
18 min	876.2	+12.4	917.2	+10.1	NO FAILURE W/ SYNTHS.
00 min	876.7	+12.4	917.9	+10.2	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with ULT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 22:08 (hour and min)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

RETURN TO LEVEL 0 (Previous = 3, Ambient = 1) End DWELL: 22:20 (hour and min)

STEP-STRESS LEVEL COMPLETE

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SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter below): 172 — Test Date: 03/04/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 8 (RETEST)

UUT PERFORMANCE TEST DATA — PERFORMANCE MONITORING

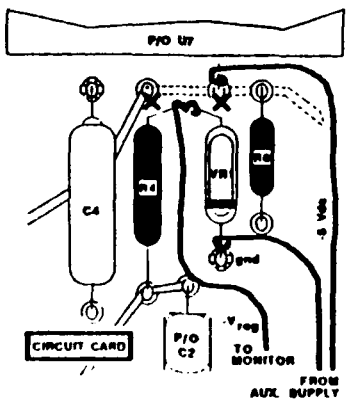
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

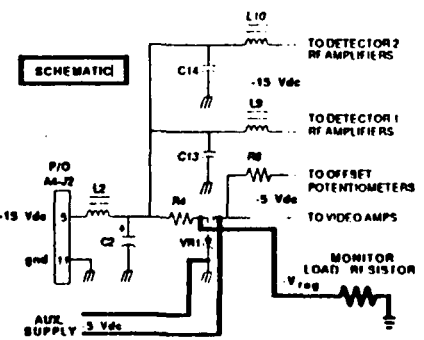
Start TEST: 21:47 (mark HR:MIN)

Voltage across LOAD RESISTOR: −5.5929 (Vdc) Δ = −0.0214 V (refer to Appendix D; nominally −5 Vdc)

End TEST: 21:50 (mark HR:MIN) Aux Supply Current = 56.1 mA

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0 FINAL

A. D. Mueller

* Detector Power Disconnected at Station Conn. J0103

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

* Begin RAMP: 22:20 (Prog 3 Initiated) Ramp = 36 min (22:56) * Start DWELL: 23:35 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +61.5 (°C) Set +61°C Flange Temperature: +68.6 (°C) *

STEP-STRESS Level Component Temperature: +70 (°C) (Refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record readings below)

Supply Voltages: +5 Volts dc: +5.00 (Vdc) -5 Volts dc: -5.00 (Vdc) *

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.00 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1095 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level

Start TEST: 23:43 * (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1173.9 (mA) Δ = -46.1 -5 Volts dc: 43.8 (mA) Δ = -39.2 *

+15 Volts dc: 125.1 (mA) Δ = 0.6 -15 Volts dc: 505.0 (mA) Δ = 5.6

End TEST: 23:48 (TIME HR MIN) Disconnected Det. again

@ 23:47
2.92 Amps
Connected Det
-0.873 Vdc

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (1/T) for each UUT Digital Output. Report with setting for Channels 30 at this STEP-STRESS Level.

Start TEST: 23:50 (TIME HR MIN) Reconnect Detector Connector

I & Q output bits are at constant +1.76 Vdc → See below

No Duty Cycle Detect

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (sec)	Detector 1 Duty Cycle (percent)	Detector 2 T (sec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	+3.92 Vdc		+3.76 Vdc		
	I > Q	+1.76 Vdc		+3.76 Vdc		
	I + Q > 0	+3.840 Vdc		+3.76 Vdc		
	Q > 0	+3.84 Vdc		+3.76 Vdc		
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

Report # 77393

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L (usec) T (sec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) T (sec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					See Sheet 2
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST 23:56 (HH:MM MM/DD) Disconnect Detector Power again

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 172 Test Date: 03/04/92 - 03/05/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 23:58 (HH:MM MM/DD) (Detector Disconnected)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *amount for cable losses
50 min	684.0	+12.8 **	684.0	+12.1 **	** Signal outputs are void if worse with Detector disconnected
35 min	729.0	+14.1	729.0	+12.7	
18 min	825.0	+14.2	825.0	+14.2	
00 min	921.0	+13.0	921.0	+12.8	

SYNTH's ARE GOOD!

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check Mark)

End TEST: 00:11 (HH:MM MM/DD)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

TEST COMPLETE -5V FAILURE ASSOCIATED WITH DETECTOR VERIFIED End DWELL 00:35 (HH:MM MM/DD)

STEP-STRESS LEVEL COMPLETE

RAMP TO ROOM TEMP @ 00:35 03/05/92 * Detector Power Disconnected

UUT POWER OFF @ 01:00 03/05/92

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 172

Test Date: 03/04/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0 (FINAL)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

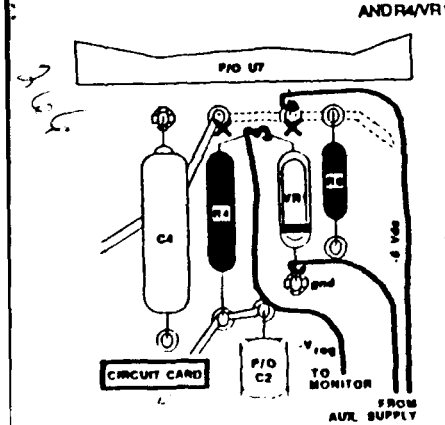
Start TEST: 23:35 (HOUR MIN SEC) Aux = -5.1095 Vdc / -5 V Power Supply Turned ON) & Detector Conn reconnected

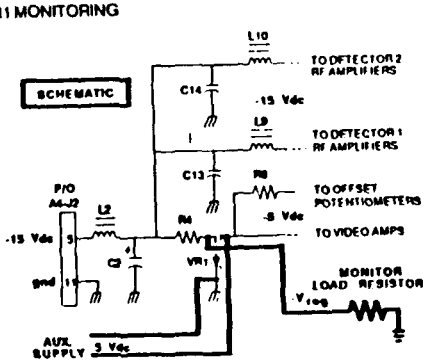
Voltage across LOAD RESISTOR: -5.3980 (Vdc) (refer to Appendix D, nominally -5 Vdc)

End TEST: 23:39 (HOUR MIN SEC) Disconnect Detector Conn. again

Aux Supply Current = 61.0 mA

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

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FULL PRINT-OUT OF Power Output and Frequency [redacted] STEP-STRESS TEST Ser. # 172

LEVEL 0 FINAL
SYNTH #1 J5
03/04/92
@ 23:58 begin
03/05/92
@ 00:05 end

(Detector computer disconnected)

Power at J5 is 12.8 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.2 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.1 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.9 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 14.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

192

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

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FULL PRINT-OUT OF Power Output and Frequency [redacted] STEP-STRESS TEST Ser. # 172

LEVEL 0 FINAL
SYNTH #2 J12
03/05/92
@ 00:05
to 00:10

(Detector computer disconnected)

Power at J12 is 12.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.5 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 14.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 14.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 14.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 14.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 14.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

TEST EQUIPMENT & CALIBRATION LOG

Maintain Log for testing conducted 03/02/92 through 03/06/92

Item	DESCRIPTION	Manuf. & Part No.	ID NUMBER	LAST CAL*	CAL* DUE	Item Notes
01	T/R Test Station	HAC; SPECIAL	F-A15223		NCR	G-132043
02	Control Panel	HAC; SPECIAL	G-132210		NCR	
03	Signal Generator	HP; 8660C	G-128061	12-17-91	01-13-93	
04	Auxiliary Section	HP; 86631B	G-128062		NCR	T/R ITEM 03
05	RF Section	HP; 86603A	G-128063	12-17-91	01-13-93	T/R ITEM 03
06	Spectrum Analyzer	HP; 8568A w/ Opt E16	G-132082	12-11-91	04-30-92	
07	FET Probe	HP; 1120A	G-132055	12-19-90	04-30-92	FOR CAL
08	Power Meter	HP; 436A	G-128036	06-18-91	12-24-92	"
09	Power Sensor	HP; 8482A	G-128059	09-09-91	10-21-92	"
10	Oscilloscope	HP; 1980B	G-132049	09-24-91	08-11-92	
11	Digital Multimeter	SystronDonner; 7344A	G-127998	06-06-91	08-18-92	
12	Digital Multimeter	HP; 3478A	H-A53624	09-06-91	06-25-92	
13	Power Splitter	MiniCkts; ZFSC-2-5	NO ID ✓		NCR	
14	Power Splitter	MiniCkts; ZFSC-2-5	NO ID ✓		NCR	
15	Reg. Power Supply	Lambda; LP-531-FM	G-132292		NCR	+15V
16	Reg. Power Supply	Lambda; LP-531-FM	"		NCR	-15V
17	Reg. Power Supply	Lambda; LP-530-FM	G-132291		NCR	+5V
18	Reg. Power Supply	Lambda; LP-520-FM	"		NCR	-5V
19	Computer	HP; 9845B	G-128012		NCR	
20	Flex. Disk Memory	HP; 9895A	G-133306		NCR	
21	Signal Generator					
22	Oscilloscope	Tektronix; 2465				
23	Digital Multimeter					
24	Digital Multimeter					
25	Digital Multimeter					
26	Thermal Chamber	Thermotron; S-4 w/Cntl	H-B07567	09-18-91	09-02-92	
27	Data Acqtn Cntl Unit	HP; 3497A	H-428499	12-19-91	07-29-93	
28	Computer	HP; Model 85	H-A86429		NCR	
29	Power Supply, AUX.	HP; 6299A	H-357054		NCR	-5.1V
30	PLOTTER	HP; 7470A	H-512478		NCR	
31	PRINTER	HP; THINKJET	E-A08763		NCR	
32						
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						

*NCR = No Calibration Required

CALIBRATION ROUTINE PERFORMED: 03-02-92; 15:52 PRIOR TO TESTING

263

USE for MSN 172 TEST
03/04 - 03/05/92

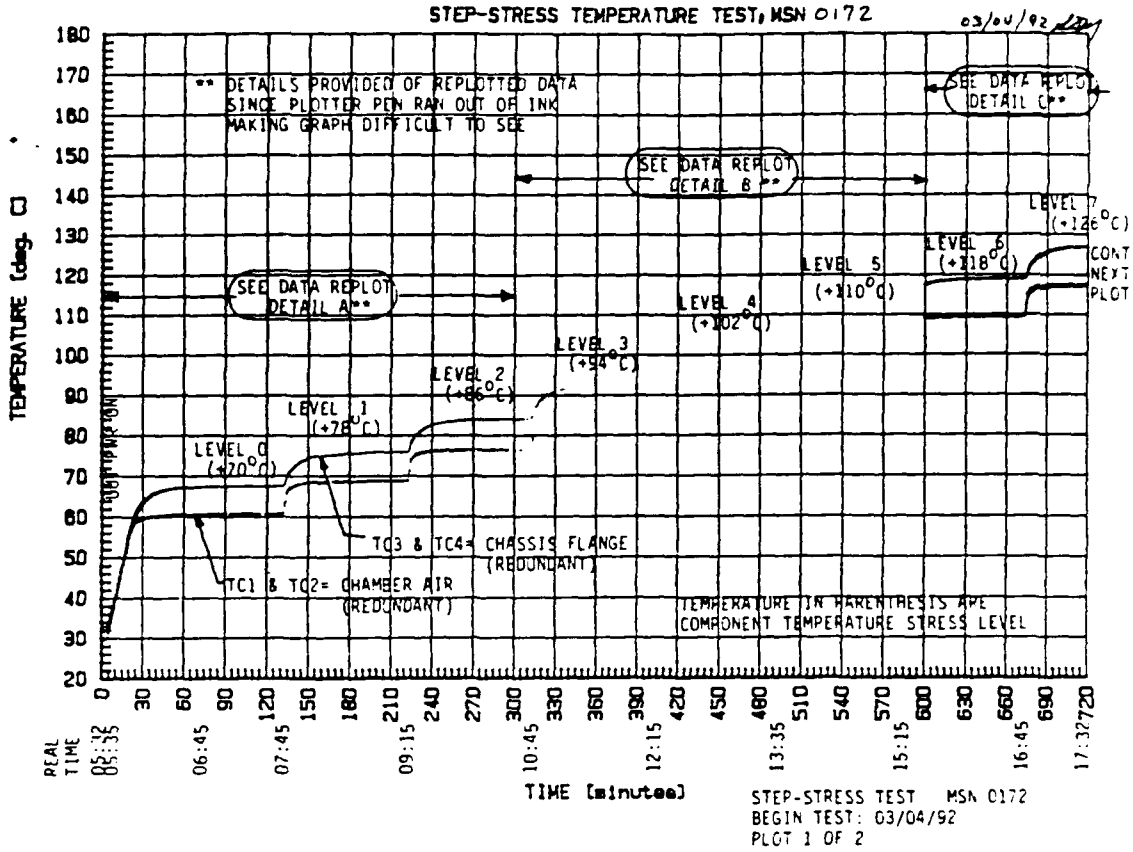
DATE: [redacted] TIME: [redacted]
03/02/92 15:52

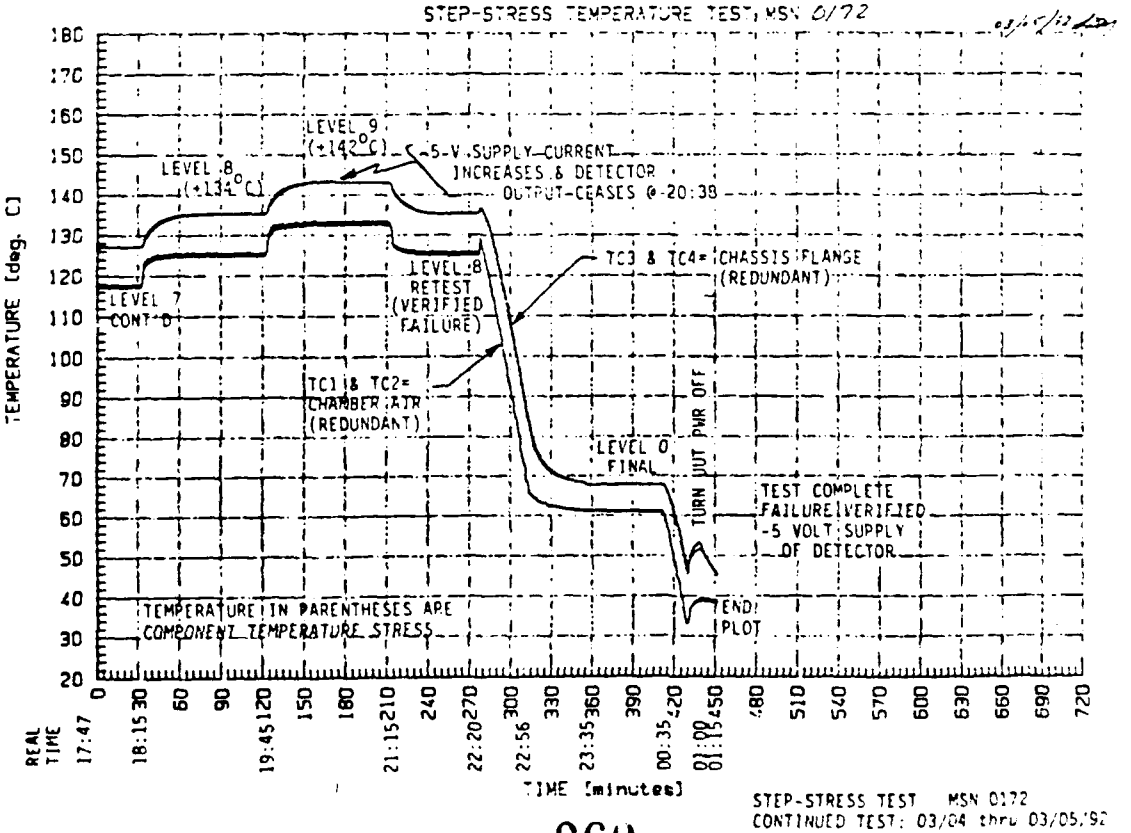
STEP-STRESS TEST
CALIBRATION DATA
(CABLES J8 & J12)

ESD S2466 TEST

Synth_ref= 1499930
Freq_mod_ref= 9999930
Sp_clock_output = 0
Phase_lo_output = 1.12
Phase_if_output = 0
Up_dn_conv_lo = 3.37
313.75_lo = 14.9 dBm /313.75177E6MHz

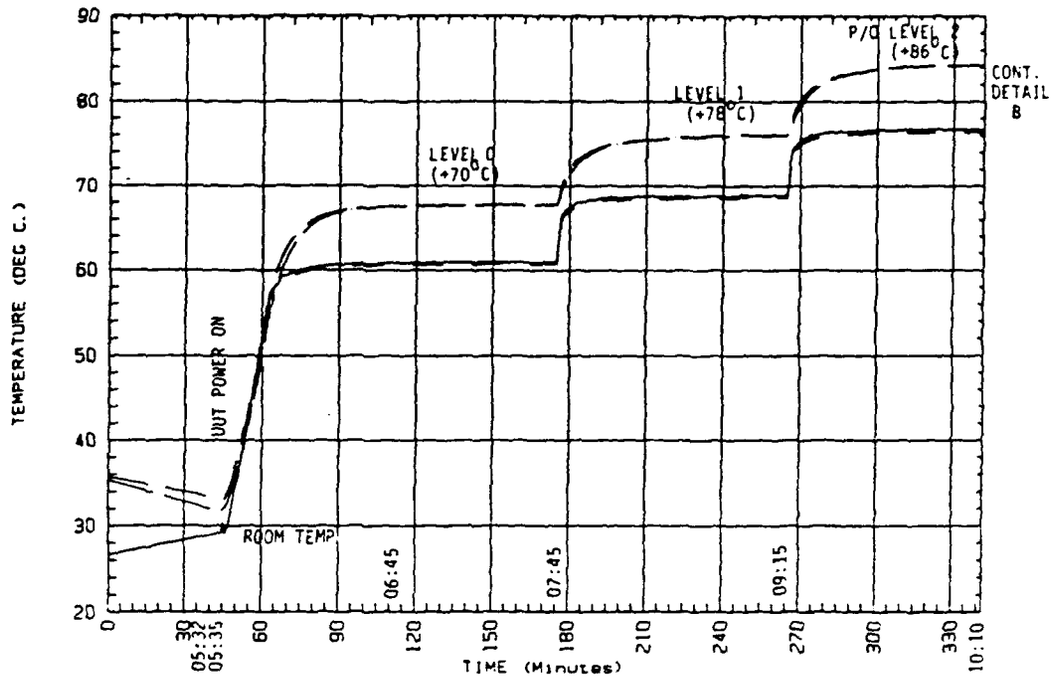
Channel	Freq	Dn_conv_output	Synth_lo_output	Hit_sgnl_t_o
50	634	1.2	1.27	2.17
49	637	1.19	1.17	2.13
48	640	1.18	1.12	2.11
47	643	1.21	1.23	2.11
46	646	1.28	1.37	2.03
45	699	1.34	1.4	1.92
44	702	1.33	1.3	1.89
43	705	1.44	1.32	1.95
42	708	1.41	1.39	1.96
41	711	1.37	1.4	1.83
40	714	1.32	1.36	1.88
39	717	1.32	1.43	1.92
38	720	1.38	1.59	1.91
37	723	1.43	1.67	1.82
36	726	1.45	1.66	1.75
35	729	1.44	1.63	1.79
34	732	1.41	1.71	1.88
33	735	1.33	1.76	1.89
32	738	1.32	1.74	1.79
31	741	1.31	1.74	1.8
30	744	1.36	1.81	1.84
29	747	1.45	1.92	1.84
28	750	1.47	1.95	1.71
27	753	1.44	1.9	1.69
26	756	1.44	1.93	1.82
25	759	1.44	2	1.83
24	762	1.43	2	1.83
23	765	1.44	1.95	1.78
22	768	1.51	1.97	1.8
21	771	1.62	2.1	1.82
20	774	1.67	2.13	1.76
19	777	1.66	2.14	1.7
18	825	1.84	2.32	1.69
17	828	1.77	2.23	1.67
16	831	1.72	2.29	1.73
15	834	1.69	2.29	1.78
14	837	1.69	2.31	1.73
13	892	1.65	2.88	1.64
12	895	1.7	2.86	1.65
11	898	1.69	2.87	1.58
10	891	1.72	2.85	1.48
9	994	1.76	2.82	1.51
8	897	1.79	1.99	1.52
7	900	1.71	1.98	1.5
6	903	1.59	1.95	1.43
5	906	1.6	1.89	1.49
4	909	1.66	1.9	1.56
3	912	1.65	1.88	1.53
2	915	1.55	1.91	1.45
1	918	1.52	1.89	1.44
0	921	1.58	1.79	1.53


STEP-STRESS TEMPERATURE TEST, MSN 0172
03/04/92
** DETAILS PROVIDED OF REPLOTTED DATA SINCE PLOTTER PEN RAN OUT OF INK MAKING GRAPH DIFFICULT TO SEE
SEE DATA REPLOT DETAIL A**
SEE DATA REPLOT DETAIL B**
SEE DATA REPLOT DETAIL C**
LEVEL 0 (+20°C)
LEVEL 1 (+78°C)
LEVEL 2 (+86°C)
LEVEL 3 (+94°C)
LEVEL 4 (+102°C)
LEVEL 5 (+110°C)
LEVEL 6 (+118°C)
LEVEL 7 (+126°C)
CONT. NEXT PLOT
TC3 & TC4= CHASSIS FLANGE (REDUNDANT)
TC1 & TC2= CHAMBER AIR (REDUNDANT)
TEMPERATURE IN PARENTHESIS ARE COMPONENT TEMPERATURE STRESS LEVEL
TEMPERATURE [deg. C]
TIME [minutes]
REAL TIME
STEP-STRESS TEST MSN 0172
BEGIN TEST: 03/04/92
PLOT 1 OF 2


STEP-STRESS TEMPERATURE TEST, MSN 0172
LEVEL 9 (+142°C)
LEVEL 8 (+134°C)
-5-V SUPPLY CURRENT INCREASES & DETECTOR OUTPUT CEASES @ 20:38
LEVEL 7 CONT'D
LEVEL 8 RETEST (VERIFIED FAILURE)
TC3 & TC4= CHASSIS FLANGE (REDUNDANT)
TC1 & TC2= CHAMBER AIR (REDUNDANT)
LEVEL 0 FINAL
TURN UUT PWR OFF
TEST COMPLETE FAILURE VERIFIED -5 VOLT SUPPLY OF DETECTOR
END PLOT
TEMPERATURE IN PARENTHESES ARE COMPONENT TEMPERATURE STRESS
TEMPERATURE [deg. C]
TIME [minutes]
REAL TIME
STEP-STRESS TEST MSN 0172
CONTINUED TEST: 03/04 thru 03/05/92
PLOT 2 OF 2

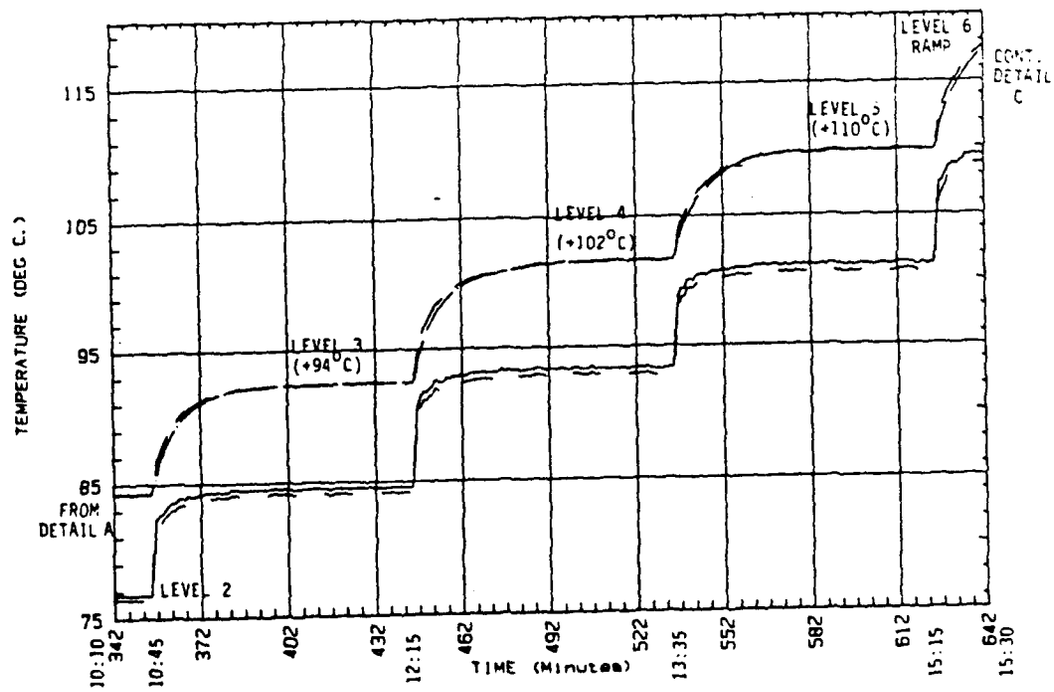
DETAIL A: MSN 0172 (PLOT 1; DISK 1; 03/4/92)

TC1 CHAMBER AIR
TC2
TC3 CHASSIS FLANGE
TC4



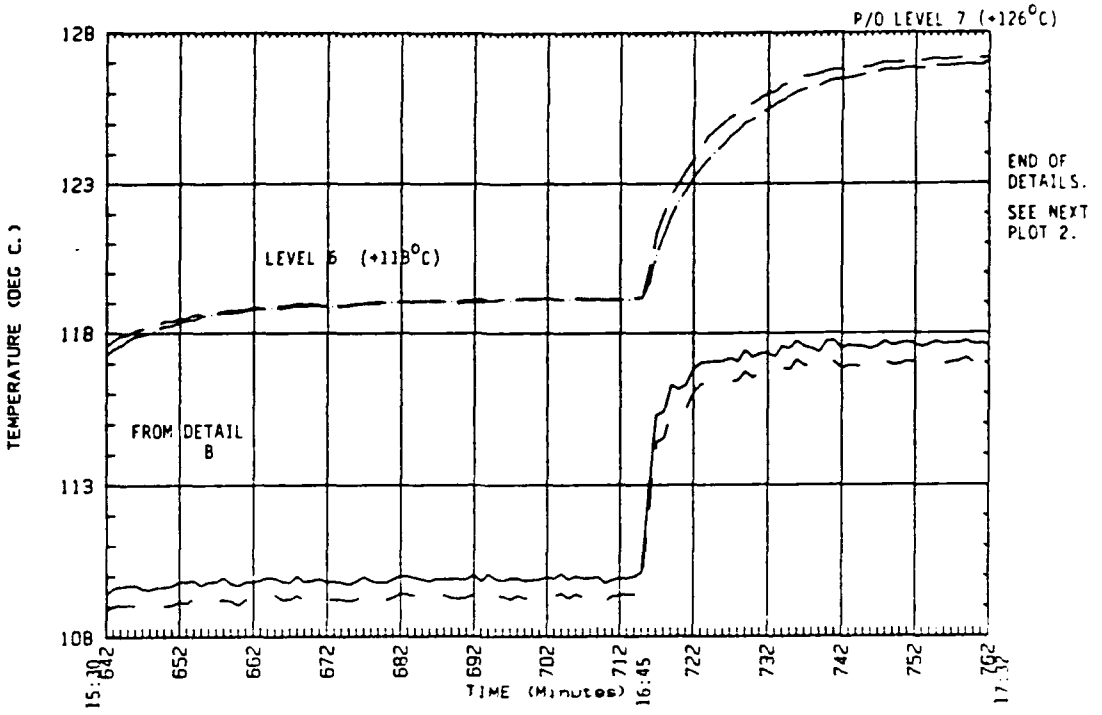
DETAIL B: MSN 0172 (PLOT 1; DISK 1; 03/04/92)

TC1 CHAMBER AIR
TC2
TC3 CHASSIS FLANGE
TC4



DETAIL C: MSN 0172 (PLOT 1; DISK 1; 03/04/92)

TC1 CHAMBER AIR
TC2
TC3
TC4 CHASSIS FLANGE



Test Data Cont'd: Date: 03/04/92

RECEIVE UNIT MSN 172 FOR TEST.

04:40 - Begin to LOAD PLOT PROGRAM & SETUP UUT IN CHAMBER

ESTABLISH: CH.1 AS TC1 (CHAMBER AIR FARSIDE)
CH.2 TC2 (" NEAR DOOR)
CH.3 TC3 (FLANGE NEAR DOOR/J11 & J12)
CH.4 TC4 (" FARSIDE/J5 & J4)

05:30 - SETUP COMPLETE. TURN UUT POWER ON.

05:35 - BEGIN RAMP TO LEVEL 0 (+61°C SET-PT) FROM ROOM TEMP (PROG#1 INTVL#1)

06:45 Dwell @ 61°C Start test stress level 0
07 45 Step stress level 0 complete start ramp to level 1
07 15 Dwell @ 69°C Start test stress level 1
09 15 Step stress level 1 Complete start ramp to level 2
09 45 Dwell @ 77°C start test stress level 2
10 45 step stress level 2 complete start ramp to level 3
11 15 Dwell @ 85°C start test
11 45 Step stress level 3 Complete start ramp to level 4
12 45 Dwell @ 94°C start test
13 45 Step stress level 4 Complete start ramp to level 5
14 15 Dwell @ 102°C start test
15 15 Step stress level 5 Complete start ramp to level 6
15 45 Dwell @ 111°C. Start test. 1 SDS pulse @ 2026
16:45 Step Stress Level 6 Complete Start ramp to Level 7
17:15 Dwell @ 119°C. Start test.
17:32 720 scans complete Plot 1

Data Recorder

Page 15

Test Data Cont'd: STEP-STRESS TEST MSN 0172 Date: 03/04/92

17:47 - PLOT 2, DATA DISK #2 BEGINS.
TC ASSIGNMENT SAME AS BEFORE.
B. ARMSTRONG TO REPLOT PLOT 1 DATA FOR MSN 0172 SINCE PEN HAD DRIED OUT (LEVEL 3 TO LEVEL 5) AND DATA POINTS ARE VERY FAINT.

18:15 Step-Stress Level 7 Complete (+119°C)
Ramp to Level 8.

18:45 Dwell @ +127 °C Level 8.

19:45 Step-Stress Level 8 Completed. Both Synths have strong output power & are locked at a fixed frequency. This is a known ANOMALY
Ramp to Level 9.

20:15 Dwell @ Level 9 (+135°C Setting)

20:39 After testing Detector 1 & 2 CH00 I & Q-bits -5V Supply values went from -6.80 Vdc to -0.977 Vdc and was drawing 2.91 Amp vs. less than 99.6 mA. Both Synthesizers seemed unaffected, yet were probably at a different frequency from normal. Auxiliary Supply current was 85.8 mA.

21:15 Completed Level 9 Dwell. Manually ramp down to Level 8 (+127°C).

21:45 Dwell @ Level 8. -5V Supply at -0.948 Vdc and 2.826 Amp. Disconnected Detector connector from Station to trouble shoot.

21:50 Detector Power Connector disconnected at station. Supply goes to -6.64 Vdc and 44.6 mA. Detector FAILURE Verified. Leave disconnected.

22:20 Verification complete. Ramp to Level 0 (+61°C) Prog#3, Intvl#1, Reduce V-stresses.

23:35 - Begin 1-hour dwell @ LEVEL 0 FINAL

03/05/92
00:35 - END LEVEL 0 FINAL TEST Failure Reverified (-5V @ DETECTOR)

Data Recorder: [signature]

Page 16

27.3

Test Data Cont'd: STEP-STRESS TEST MSN #172 Date: 03/05/92

01:00 Unit @ Room Temp. Turn all UUT power off.

01:15 END PLOT #2. Data DISK # 2. OPEN CHAMBER.

TEST COMPLETE.

Data Recorder: JSM

17

HUGHES
HUGHES AIRCRAFT COMPANY

STEP-STRESS
1 PROJECT NAME

TROUBLE & FAILURE REPORT

FAIL CLASS | TEST TYPE | TEST ENV | FAIL CAUSE | RELEV

FAM CODE

SYST CODE

NO. Z7393

2 THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE ☒ FAILURE — LEVEL 9

ORIGINATOR

3 SYSTEM SUBSYSTEM NAME	P N	S N	4 TIMER COUNTER READINGS	5 DATE	35 REFERENCES
T/R MODULE	part no -103	172	TIME: 20:38 ELAPSED HRS	03 04 82 MO DAY YR	

6 REPORTING FACILITY	7 REPORTED BY	ORG CODE	OPERATING LOG NO
STEP-STRESS TEST C/O MUELLER (GSS 82-6E TEST)	A. D. Mueller 82/04/82	1A 72 30	

8 TROUBLE FAILURE OBSERVED WAS (TEST CONDITIONS SYMPTOMS SEVERITY ETC. INCLUDING "IS" AND "SHOULD BE" DATA)

LEVEL 9 (+142°C Comp/+133°C CHMBR/±6.8V & ±17.7V) -5V SUPPLY OF DETECTOR CCA INCREASED TO 2.9 Amps @ -0.9 Volts (typically 97mA @ -6.8V). NO DETECTOR I&Q BIT OUTPUTS HALF WAY THROUGH TEST. (BEGAN @ 20:28; NO OUTPUT @ 20:38). LEVEL B & D TESING CONFIRMS IT IS AT DETECTOR. (-5V AUX SUPLY & R4/VA1 MOD SEEMS UNAFFECTED) SEE TEST DATA SHEETS FOR ADDITIONAL COMMENTS. NO VISUAL PERFORMED AT INITIAL REPORT.

TFR CONTINUATION USED ☐

9 TROUBLE FAILURE OCCURRED DURING
(A) ☒ ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE-FLIGHT OR CURSORY CHECK

10 ACTION TAKEN TO CORRECT TROUBLE FAILURE
(A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 - 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 - 20)

11 ITEM REPLACED NAME	P N	S N	12 ITEM INSTALLED NAME	P N	S N	13 DISPOSITION OF REPLACED ITEM

14 WERE OTHER TROUBLES FAILURES NOT RELATED TO ORIGINAL NOTED?
(A) ☐ NO (B) ☐ YES LIST ON NEW TFR - TFR NO _____

15 WAS REPORTED TROUBLE FAILURE VERIFIED?
(A) ☐ YES (B) ☐ NO (CHECK 15 B AND EXPLAIN)

VERIFICATION

16 FAILED ITEM NAME	P N	S N	REF DESIG	MANUFACTURER

17 NEXT HIGHER ASSY NAME	P N	S N	REF DESIG	MANUFACTURER

18 A ☐ REWORK REQUIRED IS B ☐ REWORK IS NOT REQUIRED BECAUSE

19 VENDOR REWORK ANALYSIS IS REQUIRED ☐
ITR _____ C.A.R _____

20 DISPOSITION OF ITEM IF NOT REWORKED

21 AUTHORIZATION BY ORG CODE DATE

REWORK & RETEST

22 LIST BELOW ALL PARTS REPLACED REPAIRED OR ADJUSTED

A CIRCUIT SYMBOL	B PART NUMBER	C S N	D MANUFACTURER	E DEFECT	F REWORK ACTION TAKEN	G REEL LOT NO	H APPROVED PARTS YES	H APPROVED PARTS NO	PRI FAIL

23 OTHER REWORK ACTION

24 REWORKED BY	ORG CODE	25 RETESTED BY	ORG CODE	26 RETEST RESULTS APPROVAL	DATE

27 RETEST RESULTS REPAIRED ITEM IS ACCEPTABLE FOR
☐ UNRESTRICTED USE ☐ RESTRICTED USE ☐ NOT ACCEPTABLE EXPLAIN IN BLOCK 30

28 DISPOSITION OF ITEM AFTER RETEST

29 Q C

ENGINEERING

30 CAUSE OF FAILURE - COMMENTS (IF ANALYSIS NOT PERFORMED EXPLAIN)

31 BASIC CAUSE OF TROUBLE FAILURE (SELECT FROM BLOCK I ON REVERSE SIDE)

32 SIGNATURE ORG CODE DATE

33 CORRECTIVE ENGINEERING ACTION TAKEN (IF NONE JUSTIFY) - CONCLUSIONS

REF DOCUMENT IMPLEMENTING CORRECTIVE ACTION ECO ECR ETC IS NO.

34 SIGNATURE ORG CODE DATE

11020 CS MAR 66

USE TFR CONTINUATION SHEET IF ADDITIONAL SPACE IS NEEDED

FOR RELIABILITY ANALYSIS AND FOLLOW UP SEE REVERSE SIDE OF COPY 4

Z7393

STEP-STRESS TEST DATA NOTEBOOK

UNIT UNDER TEST: MSN 0815

TEST STATUS: FAILURE CONFIRMED

(DURING LEVEL 10 DWELL)

TEST SUMMARY

STEP-STRESS		START DWELL	ANOMALY/ FAILURE	END DWELL
		5-Mar-92		
LEVEL	0	8:45		9:45
LEVEL	1	10:15		11:15
LEVEL	2	11:45		12:45
LEVEL	3	13:15		14:15
LEVEL	4	14:45		15:45
LEVEL	5	16:15		17:15
LEVEL	6	17:45		18:45
LEVEL	7	19:15		20:15
LEVEL	8	20:45		21:45
LEVEL	9	22:15		23:15
LEVEL	10	23:45	Anomaly	0:45
		5-Mar-92		6-Mar-92
FAILURE:			23:55	
Retest	9	1:15		1:45
Final Test	0	3:05		4:05
				6-Mar-92

STEP-STRESS TEST DATA SHEET

Sheet 1 of 6

UUT Serial Number (enter NSN): 815

Test Date: 3/5/92

Tester: (Name & rank/title)

STEP-STRESS Level (enter 0 - 10): 0

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 08:05 (TIME HR MIN)

Start DWELL: 08:45 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 60.7 (°C) Set @ 61°C
(Chamber thermocouple reading)

Flange Temperature: 66.5 (°C)
(Thermocouple reading)

STEP-STRESS Level Component Temperature: ____ (°C)
(refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: +5V (Vdc) - 5 Volts dc: -5 (Vdc)

+15 Volts dc: +15 (Vdc) -15 Volts dc: -15 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 08:45 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1214 (mA) - 5 Volts dc: 81 (mA)

+15 Volts dc: 115 (mA) -15 Volts dc: 495 (mA)

End TEST: 08:46 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 6

UUT Serial Number (enter NSN): 815

Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or 1FE STEP-STRESS Level.

Start TEST: 08:46 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	461.44/961.44	48.8	4.84/961.44	50	t / ← T →
	I > Q	"	"	461.44/961.44	48.8	
	I + Q > 0	"	"	481.44/961.44	50	
	Q > 0	"	"	"	"	
Other Specify -72 (dBm)	I > 0	461.44/961.44	48.8			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	illegible		961.44/961.44	50	
	I > Q	961.44/961.44	48.8	461.44/961.44	48.8	
	I + Q > 0	"	"	481.44/961.44	50	
	Q > 0	"	"	481.44/961.44	50	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 815 Test Date: 7/5/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Lowest T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L(usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.6us/9.6us	48.5	4.8us/9.6us	50	
	I > Q	"	"	4.6us/9.6us	48.8	
	I + Q > 0	"	"	4.8us/9.6us	50	
	Q > 0	"	"	"	"	
Other Specify -72 (dBm)	I > 0	4.6us/9.6us	48.8			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.6us/9.6us	47.7	4.8us/9.6us	50	
	I > Q	4.6us/9.6us	47.7	4.8us/9.6us	48.8	
	I + Q > 0	"	"	4.8us/9.6us	50	
	Q > 0	"	"	"	"	

End TEST: 09:00 (TIME HR MIN)

TEST continued next page

2511

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 815 Test Date: 7/5/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 09:00 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *amount for cable losses
50 (hex)	684	11.47	684	11.27	
35 (hex)	729	10.13	729	9.93	
18 (hex)	825	11.65	825	9.73	
00 (hex)	921	9.4	921	9.1	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 09:10 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 09:45 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

UUT Serial Number (enter MSN): 815

Test Date: 3/5/02

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

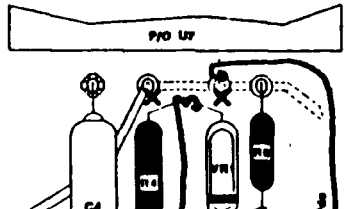
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

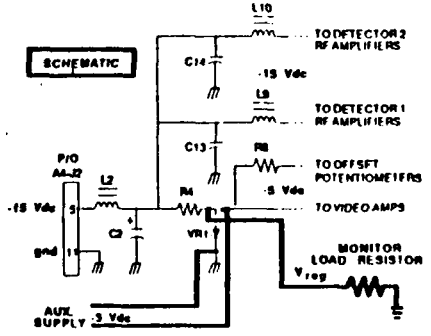
Start TEST: 09:10 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.15 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 09:11 (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





3/5/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Synth ref. 14.515...
Stress level 0
J5 output

****

Power at J5 is 5.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 6.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Pow at J5 is 8.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Po at J5 is 3.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.2 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is-11.4 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 11.2 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.2 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is-11.4 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/5/92
Sun Ref #815
Stress level 0
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 3.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is less than 687.0 MHz which is below the specified frequency.
Power at J12 is 1.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than 690.0 MHz which is below the specified frequency.
Power at J12 is 4.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than 693.0 MHz which is below the specified frequency.
Power at J12 is 3.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 705.0 MHz which is above the specified frequency.
Power at J12 is 6.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 708.0 MHz which is above the specified frequency.
Power at J12 is 6.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than 711.0 MHz which is below the specified frequency.
Power at J12 is 6.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is less than 714.0 MHz which is below the specified frequency.
Power at J12 is 2.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 723.0 MHz which is above the specified frequency.
Power at J12 is 5.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Frequency is less than 729.0 MHz which is below the specified frequency.
Power at J12 is 6.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is less than 765.0 MHz which is below the specified frequency.
Power at J12 is 5.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 768.0 MHz which is above the specified frequency.
Power at J12 is-1.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Frequency is less than 771.0 MHz which is below the specified frequency.
Power at J12 is 7.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 831.0 MHz which is above the specified frequency.
Power at J12 is .7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 834.0 MHz which is above the specified frequency.
Power at J12 is 6.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is less than 837.0 MHz which is below the specified frequency.
Power at J12 is-1.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Frequency is less than 882.0 MHz which is below the specified frequency.
Power at J12 is 5.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 885.0 MHz which is above the specified frequency.
Power at J12 is 4.2 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 888.0 MHz which is above the specified frequency.
Power at J12 is 5.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 891.0 MHz which is above the specified frequency.
Power at J12 is-4.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 894.0 MHz which is above the specified frequency.
Power at J12 is 6.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).

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Power at J12 is 6.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 909.0 MHz which is above the specified frequency.
Power at J12 is 3.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is less than 915.0 MHz which is below the specified frequency.
Power at J12 is .8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 10.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is .8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 815

Test Date: 3/5/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 1

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 09:45 (TIME HR MIN)

Start DWELL: 10:15 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 65.8 °C (Chamber thermocouple reading) 64.64

Flange Temperature: 24.6 °C (Thermocouple reading)

STEP-STRESS Level Component Temperature: 76 °C (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: +5.2 (Vdc) - 5 Volts dc: -5.2 (Vdc)

+15 Volts dc: +15.3 (Vdc) -15 Volts dc: -15.3 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 10:22 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1253 (mA) - 5 Volts dc: 34 (mA)

+15 Volts dc: 117 (mA) -15 Volts dc: 4.03 (mA)

End TEST: 10:26 (TIME HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 815

Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 10:23 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	466 ns/966 ns	48.3	466 ns/966 ns	48.5	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	4.8 us/9.6 us	50	
	Q > 0	"	"	"	"	
Other Specify -12 (dBm)	I > 0	466 ns/966 ns	48.3			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		4.8 us/9.6 us	50	
	I > Q	466 ns/966 ns	48.8	466 ns/966 ns	48.5	
	I + Q > 0	"	"	4.8 us/9.6 us	50	
	Q > 0	"	"	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q Bits	Detector 1 Lowest T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	463n/966n	48.8	463n/966n	48.8	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	482n/966n	50	
	Q > 0	"	"	"	"	
Other Specify -.71 (dBm)	I > 0	463n/966n	48.8			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1.16 noisy		4.63n/966n	48.8	
	I > Q	463n/966n	48.8	463n/966n	48.8	
	I + Q > 0	"	"	482n/966n	50	
	Q > 0	"	"	"	"	

End TEST: 10:54 (TIME HR MIN)

TEST continued next page

28?

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST. At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 1034 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *account for cable losses
50 min	684	11.47	684	11.27	[illegible] >+6dBm
35 min	729	10.93	729	9.63	
18 min	825	11.32	825	9.53	
00 min	921	8.8	921	8.7	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT L (Check here)

End TEST: 10:55 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at the STEP-STRESS Level.

End DWELL: 11:15 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 915

Test Date: 3/5/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 4): 1

UUT PERFORMANCE TEST DATA — PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

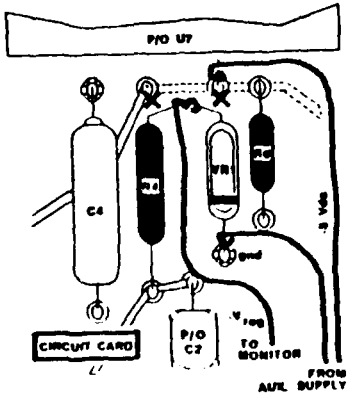
Start TEST: 1055 (Hour Min Sec)

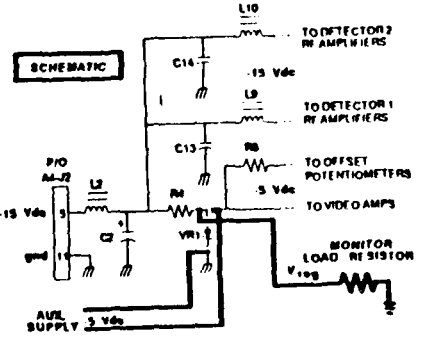
Voltage across LOAD RESISTOR: -5.16 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 1056 (Hour Min Sec)

2986

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





7/5/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

SN/Qty H 815
Stress level 1
J5 output

****

Power at J5 is 6.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.2 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 5.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

7/5/92
Syn 1Ref. 4815
Stress level 1
J12 output

****

Power at J12 is 3.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than 693.0 MHz which is below the specified frequency.
Power at J12 is 1.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is less than 696.0 MHz which is below the specified frequency.
Power at J12 is-1.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is less than 699.0 MHz which is below the specified frequency.
Power at J12 is 3.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 702.0 MHz which is above the specified frequency.
Power at J12 is 1.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 744.0 MHz which is above the specified frequency.
Power at J12 is 6.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 750.0 MHz which is above the specified frequency.
Power at J12 is 7.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Frequency is less than 759.0 MHz which is below the specified frequency.
Power at J12 is 5.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Frequency is less than 762.0 MHz which is below the specified frequency.
Power at J12 is 2.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 777.0 MHz which is above the specified frequency.
Power at J12 is 6.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 825.0 MHz which is above the specified frequency.
Power at J12 is-4.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 828.0 MHz which is above the specified frequency.
Power at J12 is 6.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 834.0 MHz which is above the specified frequency.
Power at J12 is 4.3 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is less than 885.0 MHz which is below the specified frequency.
Power at J12 is 4.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 888.0 MHz which is above the specified frequency.
Power at J12 is-.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is less than 891.0 MHz which is below the specified frequency.
Power at J12 is 6.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is less than 918.0 MHz which is below the specified frequency.
Power at J12 is-1.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 921.0 MHz which is above the specified frequency.

****

FULL PRINT-OUT OF Power Output and Frequency [redacted]er. 8

Power at J12 is 10.2 dBm @ 634.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

UUT Serial Number: 815 Test Date: 3/5/92

STEP-STRESS Level: 2 Tester:

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 11:15 Start DWELL: 11:45

STEP-STRESS Level Chamber Air Temperature: 76.6 (°C) Flange Temperature: [illegible] (°C)

STEP-STRESS Level Component Temperature: 82.77 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp, Increment Voltage to STEP-STRESS Level

Supply Voltages: +5 Volts dc: +5.4 (Vdc) -5 Volts dc: -5.4 (Vdc)

+15 Volts dc: +15.6 (Vdc) -15 Volts dc: -15.6 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 11:45

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1322 (mA) -5 Volts dc: 88 (mA)

+15 Volts dc: 118 (mA) -15 Volts dc: 513 (mA)

End TEST: 11:46

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 815 Test Date: 3/5/92

STEP-STRESS Level: 2

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 11:46

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	416 / 960	98.5	416 / 960	98.5	
	I > Q	"	"	456 / 960	47.5	
	I + Q > 0	"	"	480 / 960	50	
	Q > 0	"	"	"	"	
Other: Specify -71 (dBm)	I > 0	416 / 960	50			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		480 / 960	50	
	I > Q	456 / 960	48.5	468 / 960	48.8	
	I + Q > 0	"	"	492 / 960	50	
	Q > 0	"	"	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	453ns/84ns	48.8	456ns/84ns	48.8	
	I > Q	"	"	456ns/84ns	47.5	
	I + Q > 0	"	"	456ns/84ns	50	
	Q > 0	"	"	"	"	
Other Specify	I > 0	456ns/84ns	50			
-N (dBm)	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify	I > 0					
	I > Q					
(dBm)	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noisy		456ns/84ns	50	
	I > Q	456ns/84ns	48.8	456ns/84ns	48.8	
	I + Q > 0	"	"	456ns/84ns	50	
	Q > 0	"	"	"	"	

End TEST 1156 (HHMM MS only)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 1156 (HHMM MS only)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)
50 min	684	11.37	684	11.17
35 min	729	10.63	729	9.23
18 min	825	10.72	825	9.12
00 min	921	9.4	921	8.8

Observation: *constant for cable losses

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check box)

End TEST: 12 10 (HHMM MS only)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 1145 (HHMM MS only)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 815

Test Date: 3/5/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

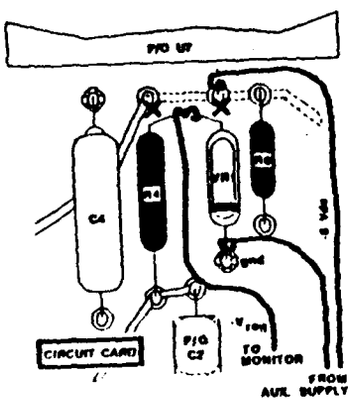
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

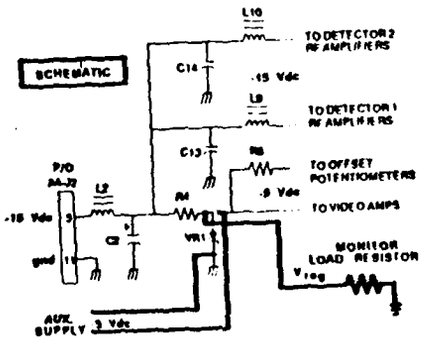
Start TEST: 12.10 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.18 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 12 11 (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





3/5/92
sag/Det 4815
stress level 2
JS output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at JS is 2.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at JS is 6.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at JS is 4.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at JS is 8.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at JS is 6.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at JS is 2.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at JS is 1.6 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at JS is-4.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at JS is .0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at JS is-4.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at JS is 8.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at JS is .6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at JS is 8.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at JS is 6.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at JS is 6.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at JS is-3.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at JS is 5.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at JS is 6.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at JS is 8.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at JS is 5.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at JS is 5.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at JS is 4.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at JS is 2.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at JS is 4.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at JS is-5.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at JS is 2.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.4 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at JS is 4.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted]. #

Power at JS is 11.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at JS is 2.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at JS is 6.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at JS is 4.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at JS is 8.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at JS is 6.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at JS is 2.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at JS is 1.6 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at JS is-4.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at JS is .0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at JS is-4.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at JS is 8.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at JS is .6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at JS is 9.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at JS is 8.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at JS is 6.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at JS is 6.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at JS is-3.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at JS is 7.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at JS is 6.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at JS is 8.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at JS is 5.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at JS is 4.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at JS is 2.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at JS is 4.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at JS is-5.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at JS is 2.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at JS is 3.4 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at JS is 4.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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3/5/92
Sn/Det #815
stress level 2
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 4.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is .5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-9.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is less than 702.0 MHz which is below the specified frequency.
Power at J12 is 3.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than 711.0 MHz which is below the specified frequency.
Power at J12 is 2.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is less than 714.0 MHz which is below the specified frequency.
Power at J12 is 2.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 717.0 MHz which is above the specified frequency.
Power at J12 is 3.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is less than 723.0 MHz which is below the specified frequency.
Power at J12 is-10.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 735.0 MHz which is above the specified frequency.
Power at J12 is 5.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 738.0 MHz which is above the specified frequency.
Power at J12 is 5.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 741.0 MHz which is above the specified frequency.
Power at J12 is 3.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Frequency is less than 744.0 MHz which is below the specified frequency.
Power at J12 is 6.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 753.0 MHz which is above the specified frequency.
Power at J12 is 6.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 756.0 MHz which is above the specified frequency.
Power at J12 is 4.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 759.0 MHz which is above the specified frequency.
Power at J12 is 6.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 762.0 MHz which is above the specified frequency.
Power at J12 is .7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 765.0 MHz which is above the specified frequency.
Power at J12 is 3.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Frequency is less than 771.0 MHz which is below the specified frequency.
Power at J12 is 5.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 774.0 MHz which is above the specified frequency.
Power at J12 is-8.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 777.0 MHz which is above the specified frequency.
Power at J12 is 1.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is less than 831.0 MHz which is below the specified frequency.
Power at J12 is-3.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 837.0 MHz which is above the specified frequency.
Power at J12 is-2.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Frequency is less than 882.0 MHz which is below the specified frequency.
Power at J12 is 2.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 885.0 MHz which is above the specified frequency.
Power at J12 is-4.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is less than 891.0 MHz which is below the specified frequency.
Power at J12 is 5.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Frequency is less than 900.0 MHz which is below the specified frequency.
Power at J12 is 3.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is less than 906.0 MHz which is below the specified frequency.
Power at J12 is 3.1 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 909.0 MHz which is above the specified frequency.
Power at J12 is-5.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 912.0 MHz which is above the specified frequency.
Power at J12 is-8.4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 915.0 MHz which is above the specified frequency.
Power at J12 is 2.4 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-9.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is-10.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is .4 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is-8.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 909.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number: 815 Test Date: 5/5/92

Tester:

STEP-STRESS Level (enter 0 - 10): 3

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 12:45 (TIME HR MIN) Start DWELL: 13:15 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 84.2 / 84.95 (°C) (Chamber thermocouple reading) Flange Temperature: 90.9 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 94 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: 4.56 (Vdc) - 5 Volts dc: -5.6 (Vdc)

+15 Volts dc: +15.9 (Vdc) -15 Volts dc: -15.9 (Vdc)

Ave. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 13:15 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1335 (mA) - 5 Volts dc: 91 (mA)

+15 Volts dc: 120 (mA) -15 Volts dc: 53.2 (mA)

End TEST: 13:16 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number: 815 Test Date: 5/5/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 13:16 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4640/9280	50	4560/9280	49.1	
	I > 0	"	"	4560/9280	49.1	
	I + Q > 0	"	"	"	"	
	Q > 0	"	"	"	"	
Other Specify -71 (dBm)	I > 0	4560/9280	50			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	0015 4		4560/9280	50	
	I > Q	4640/9280	49.5	4640/9280	49.1	
	I + Q > 0	"	"	4560/9280	50	
	Q > 0	"	"	"	"	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L(usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L(usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	464/464	48.3	464/464	48.5	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	454/464	50	
	Q > 0	"	"	"	"	
Other: Specify -71 (dBm)	I > 0	464/464	50			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	NOISY		464/464	50	
	I > Q	464/464	48.5	464/464	48.5	
	I + Q > 0	"	"	454/464	50	
	Q > 0	"	"	"	"	

End TEST 13:35 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at the STEP-STRESS Level.

Start TEST: 13:26 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *amount for cable loss
50 min	684	11.37	684	11.37	
35 mm	729	10.23	729	9.13	
18 min	525	11.12	525	9.12	
00 min	921	7.18	921	8 C	

Additional Testing (OPTIONAL); **RADIO FREQUENCY OUTPUT TEST**: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number, STEP-STRESS Level, Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST 13:48 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at the STEP-STRESS Level

End DWELL 14:15 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 815

Test Date: 5/5/92

Tester: (Name & initials)

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

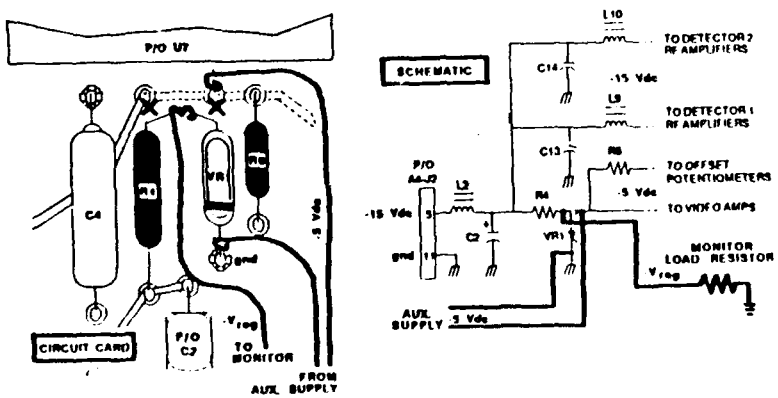
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 13 48 (HHMM HR MIN)

Voltage across LOAD RESISTOR: -5.19 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 13 49 (HHMM HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/5/92
Syn Ref #815
Stats level 3
J5 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 3.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is .9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.0 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 2.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] #

Power at J5 is 10.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is .9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

7/15/92
Sun Ref. #815
Stress level 3
J12 output

****

Power at J12 is 4.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is less than 693.0 MHz which is below the specified frequency.
Power at J12 is 4.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-7.2 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 702.0 MHz which is above the specified frequency.
Power at J12 is 3.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 714.0 MHz which is above the specified frequency.
Power at J12 is 5.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 717.0 MHz which is above the specified frequency.
Power at J12 is 5.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 723.0 MHz which is above the specified frequency.
Power at J12 is 7.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 735.0 MHz which is above the specified frequency.
Power at J12 is 3.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 741.0 MHz which is above the specified frequency.
Power at J12 is 3.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 744.0 MHz which is above the specified frequency.
Power at J12 is 6.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 762.0 MHz which is above the specified frequency.
Power at J12 is 1.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 765.0 MHz which is above the specified frequency.
Power at J12 is 1.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 768.0 MHz which is above the specified frequency.
Power at J12 is 3.6 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 774.0 MHz which is above the specified frequency.
Power at J12 is 4.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 777.0 MHz which is above the specified frequency.
Power at J12 is 3.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Frequency is less than 825.0 MHz which is below the specified frequency.
Power at J12 is 5.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is less than 828.0 MHz which is below the specified frequency.
Power at J12 is 5.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 831.0 MHz which is above the specified frequency.
Power at J12 is 2.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 837.0 MHz which is above the specified frequency.
Power at J12 is 4.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 882.0 MHz which is above the specified frequency.
Power at J12 is 2.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is less than 891.0 MHz which is below the specified frequency.
Power at J12 is 4.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 900.0 MHz which is above the specified frequency.
Power at J12 is 5.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 903.0 MHz which is above the specified frequency.
Power at J12 is 2.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 906.0 MHz which is above the specified frequency.
Power at J12 is 5.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 909.0 MHz which is above the specified frequency.
Power at J12 is 3.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 912.0 MHz which is above the specified frequency.
Power at J12 is 4.1 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 915.0 MHz which is above the specified frequency.
Power at J12 is 3.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is less than 918.0 MHz which is below the specified frequency.
Power at J12 is 5.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 10.9 dBm @ 634.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-7.2 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 915.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/5/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 4

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 14:15 (HOUR HR MIN) Start DWELL: 14:45 (HOUR HR MIN)

STEP-STRESS Level Chamber Air Temperature: 95.1 (°C) (Chamber thermocouple reading) Flange Temperature: 94.7 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 102 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +5.8 (Vdc) -5 Volts dc: -5.9 (Vdc)

+15 Volts dc: +16.2 (Vdc) -15 Volts dc: -16.2 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 14:45 (HOUR HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1406 (mA) -5 Volts dc: 94 (mA)

+15 Volts dc: 122 (mA) -15 Volts dc: 542 (mA)

End TEST: 14:46 (HOUR HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 14:46 (HOUR HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	468/960	48.8	468/960	48.8	
	I > Q	"	"	456/960	47.5	
	I + Q > 0	"	"	480/960	50	
	Q > 0	"	"	"	"	
Other Specify -11 (dBm)	I > 0	1441/960	150			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1439/960	50	480/960	50	
	I > Q	469/960	48.8	4.24/960	48.8	
	I + Q > 0	"	"	480/960	50	
	Q > 0	"	"	480/960	50	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/5/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L (max) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (max) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.6us/4.6us	48.8	4.6us/4.6us	48.3	
	I > Q	"	"	"	"	
	I + Q > 0	"	"	4.6us/4.6us	50	
	Q > 0	"	"	"	"	
Other: Specify -71 (dBm)	I > 0	4.6us/4.6us	50			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	0.6us		4.6us/4.6us	50	
	I > Q	4.6us/4.6us	48.8	"	"	
	I + Q > 0	"	"	"	"	
	Q > 0	"	"	"	"	

End TEST: 14:59 (TIME: HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 815 Test Date: 3/4/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 14:50 (TIME: HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	684	11.07	684	11.07	
35 min	729	10.93	729	9.0	
18 min	825	10.02	825	9.02	
00 min	921	* 7.3	921	7.3	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT 1 (Check here)

End TEST: 15:16 (TIME: HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 15:45 (TIME: HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (same as DUT): 515

Test Date: 3/5/12

Tester: (Please & stamp for later)

STEP-STRESS Level (zero & up): 4 last

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

RESISTOR/ZENER DIODE MODIFICATION: *At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level*

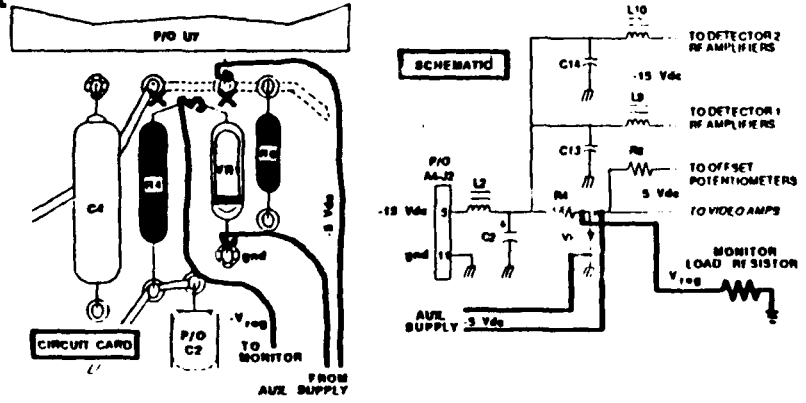
Start TEST: 15:11 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.21 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 15:17 (TIME HR:MIN)

301

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/5/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

synthesizer HE15

****

Power at J5 is-2.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 2.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is .4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-5.6 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Nr. 8

Power at J5 is 10.6 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.5 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is .4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.6 dBm @ 921.0 MHz (Spec=+9dBm minimum).

302

3/5/92
syn/Det #815
Stress level 4
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 4.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 687.0 MHz which is above the specified frequency.
Power at J12 is 2.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 699.0 MHz which is above the specified frequency.
Power at J12 is 4.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is less than 702.0 MHz which is below the specified frequency.
Power at J12 is 3.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 714.0 MHz which is above the specified frequency.
Power at J12 is 5.8 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Frequency is less than 726.0 MHz which is below the specified frequency.
Power at J12 is-3.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 729.0 MHz which is above the specified frequency.
Power at J12 is 5.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Frequency is less than 732.0 MHz which is below the specified frequency.
Power at J12 is-4.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 735.0 MHz which is above the specified frequency.
Power at J12 is 4.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 738.0 MHz which is above the specified frequency.
Power at J12 is 3.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 741.0 MHz which is above the specified frequency.
Power at J12 is 2.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 747.0 MHz which is above the specified frequency.
Power at J12 is-2.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Frequency is less than 756.0 MHz which is below the specified frequency.
Power at J12 is 4.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 759.0 MHz which is above the specified frequency.
Power at J12 is 3.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 762.0 MHz which is above the specified frequency.
Power at J12 is 2.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 765.0 MHz which is above the specified frequency.
Power at J12 is 3.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 771.0 MHz which is above the specified frequency.
Power at J12 is 3.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 777.0 MHz which is above the specified frequency.
Power at J12 is 2.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 828.0 MHz which is above the specified frequency.
Power at J12 is 2.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 834.0 MHz which is above the specified frequency.
Power at J12 is 3.[illegible] dBm @ 837.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 837.0 MHz which is above the specified frequency.
Power at J12 is 4.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 882.0 MHz which is above the specified frequency.
Power at J12 is 2.3 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is less than 885.0 MHz which is below the specified frequency.
Power at J12 is 3.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).

30.3

Frequency is greater than 891.0 MHz which is above the specified frequency.
Power at J12 is 3.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Frequency is less than 894.0 MHz which is below the specified frequency.
Power at J12 is 2.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 897.0 MHz which is above the specified frequency.
Power at J12 is-.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Frequency is less than 900.0 MHz which is below the specified frequency.
Power at J12 is-.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 903.0 MHz which is above the specified frequency.
Power at J12 is 3.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 906.0 MHz which is above the specified frequency.
Power at J12 is .9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 909.0 MHz which is above the specified frequency.
Power at J12 is 4.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is less than 918.0 MHz which is below the specified frequency.
Power at J12 is 2.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

STEP-STRESS TEST DATA SHEET

UUT Serial Number: 815 Test Date: 03/05/92

Tester: [signature]

STEP-STRESS Level: 5

Note: Calibration Data retained from 03/02/92 @ 15:52

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 15:45 Start DWELL: 16:15

STEP-STRESS Level Chamber Air Temperature: +101.0 (°C) (TC1) Flange Temperature: +108.0 (°C) (TC3)

Sat @ +102 °C

STEP-STRESS Level Component Temperature: +110 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level

Supply Voltages: +5 Volts dc: +6.00 (Vdc) -5 Volts dc: -6.00 (Vdc)

+15 Volts dc: +16.50 (Vdc) -15 Volts dc: -16.50 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1092 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level

Start TEST: 16:15

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 2412.6 (mA) -5 Volts dc: 96.2 (mA)

+15 Volts dc: 124.2 (mA) -15 Volts dc: 557.0 (mA)

End TEST: 16:16

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 815 Test Date: 03/05/92

STEP-STRESS Level: 5

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input From 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 16:16

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	456/960	47.5	468/960	48.8	8 d.o. / 120 usec
	I > Q	"	47.5	"	48.8	
	I + Q > 0	468/960	48.8	480/960	50.0	
	Q > 0	456/960	47.5	"	50.0	FLF
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	512/960	53.3	484/960	50.8	
	I > Q	464/960	48.3	"	50.8	6 d.o. / 60 usec
	I + Q > 0	"	48.3	480/960	50.0	
	Q > 0	"	48.3	480/960	50.0	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.68/5.60	48.8	4.80/9.60	50.0	
	I > Q	4.56/9.60	47.5	4.68/9.60	48.8	8 b.e. (1.20 µsec)
	I + Q > 0	4.68/5.60	48.8	4.80/9.60	50.0	
	Q > 0	4.52/9.60	47.5	4.80/9.60	50.0	TEFL
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.68/9.60	50.8	4.68/9.60	50.8	
	I > Q	4.72/9.60	49.2	"	50.8	4 b.e. (1.60 µsec)
	I + Q > 0	"	49.2	"	50.8	
	Q > 0	4.64/9.60	48.3	4.80/9.60	50.0	

End TEST: 16:27 (Time HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 16:28 (Time HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	6840	+11.0	6840	+11.2	Checked over Decreasing power out
35 min	7290	+10.7	7290	(+8.4)	All frequencies accurate for
18 min	8254	(+8.8)	8249	(+8.4)	
00 min	9210	(+5.0)	9209	(+7.0)	No Failure

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input to Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT (Check here)

End TEST: 16:48 (Time HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level

Continue w/ LEVEL 6 End DWELL 17:15 (Time HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 815

Test Date: 03/05/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

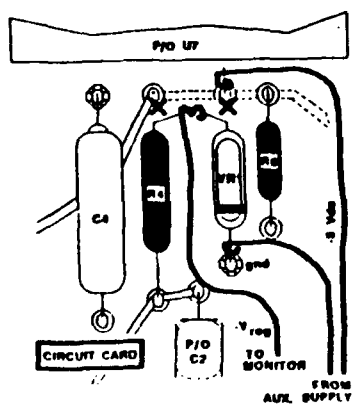
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

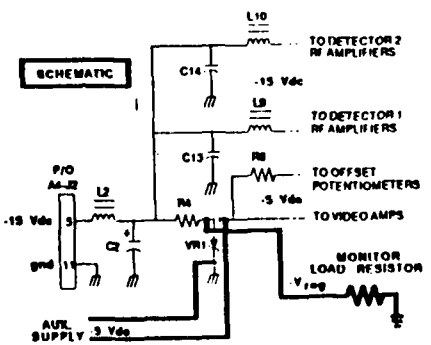
Start TEST: 16:48 (Time HR MIN)

Voltage across LOAD RESISTOR: -5.2312 (Vdc) (refer to Appendix D: nominally -5 Vdc)

End TEST: 16:49 (Time HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 815 J5

LEVEL 5
03/05/92

Power at J5 is 10.3 dBm @ 684.0 MHz (Spec=+9dBm minimum). Measured +11.0 dBm
Power at J5 is-6.9 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.1 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 729.0 MHz (Spec=+9dBm minimum). +10.7 max (max hold)
Power at J5 is 7.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is .2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.1 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 825.0 MHz (Spec=+9dBm minimum). Meas. +8.8 dBm
Power at J5 is-3.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is .9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is(.1 dBm @ 921.0 MHz (Spec=+9dBm minimum). Measured = +5.0 dBm

Noise present while observed actual Peak measurement of analyzer used in subroutine

30

STEP-STRESS TEST

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 815 J12

LEVEL 5
03/05/92

+11.2 dBm (max hold)
Power at J12 is 10.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 729.0 MHz (Spec=+9dBm minimum). +8.4 dBm max (max hold)
Power at J12 is-1.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.1 dBm @ 825.0 MHz (Spec=+9dBm minimum). +8.4 dBm max
Power at J12 is-1.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.2 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-12.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.6 dBm @ 921.0 MHz (Spec=+9dBm minimum). +7.0 dBm max

Noise may change actual measured peak value

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 6

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 17:15 (TIME HR MIN) Start DWELL: 17:45 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +109.8 (°C) (Chamber thermocouple reading) Flange Temperature: +117.3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +118 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.20 (Vdc) -5 Volts dc: -6.20 (Vdc)

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.1093 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 17:48 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1454.0 (mA) -5 Volts dc: 98.9 (mA)

+15 Volts dc: 134.9 (mA) -15 Volts dc: 57.10 (mA)

End TEST: 17:49 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (τ/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 17:51 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Data	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	476/960	48.8	480/960	50.0	
	I > 0	456/	47.5	456/	47.5	8 dev (1 sample)
	I + Q > 0	456/	47.5	480/	50.0	
	Q > 0	456/	47.5	468/	48.8	7 of 8 + 1 lo
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	512/960	53.3	480/960	50.0	
	I > 0	472/	49.2	484/	50.0	6 dev (1 sample)
	I + Q > 0	472/	49.2	484/	50.8	
	Q > 0	480/	50.0	480/	50.0	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 815 Test Date: 03/05/92

STEP-STRESS Level: 6

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued.

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Lowest T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Lowest T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	468/960	48.8	480/960	50.0	
	I > Q	468/	48.8	468/	48.8	
	I + Q > 0	468/	48.8	480/	50.0	
	Q > 0	468/	48.8	480/	50.0	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	888/960	50.8	504/960	50.0	
	I > Q	432/	45.2	432/	45.2	
	I + Q > 0	432/	45.2	480/	50.0	
	Q > 0	432/	45.2	480/	50.0	

End TEST: 17:58

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 815 Test Date: 03/05/92

STEP-STRESS Level: 6

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 18:06

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *minimum for cable losses
50 min	6840	+10.9	433.1	-3.0	(A) Harmonic components
			945.4	-6.8 (A)	
			1245.8	-15.0 (A)	
35 min	728.9	+10.4	477.3	+11.3	Synth #2 (J12) is pulled off freq
			1032	-15.0 (A)	
18 min	824.9	(+7.4)	752.5	+17.0	J5 KNOWN ANOMALY
			1129	-18 (A)	SPECTRUM LOOKS GOOD J12
00 min	920.9	(+2.2)	823	+12.6	SPECTRUM NOISY FOR J5.
	ACCEPT	Low Power	ACCEPT	ANOMALY	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT: ✓ (Check here) 2 runs J5 (okay) 1 run J12

NO FAILURES

End TEST: 18:34

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUE ON TO LEVEL 7 End DWELL 18:45

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 815 Test Date: 03/05/92

Tester (Please & stamp below): [signature]

STEP-STRESS Level (enter 0 - VII): 6

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

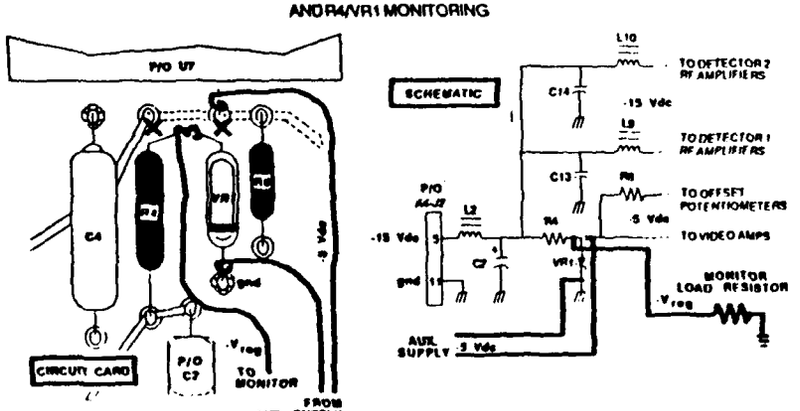
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

Start TEST: 17:49 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.2475 (Vdc) (refer to Appendix D, nominally -5 Vdc)

End TEST: 17:50 (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 815

Power at J5 is 10.2 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.1 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.0 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is-10.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.7 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-13.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-13.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is -5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

LEVEL 6
@ J5
03/05/92 18:09
(1ST RUN)

Noisy
see test data sheet

311

Frequency is greater than .0 MHz which is above the specified frequency.

STEP-STRESS TEST

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 815

Power at J5 is 11.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.8 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is .6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is-8.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is .3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is .7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is-9.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is .8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is .7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.4 dBm @ 921.0 MHz (Spec=+9dBm minimum).

LEVEL 6
@ J5
03/05/92 18:12
(2ND RUN)

Noisy
see test data sheet

STEP STRESS TEST

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 815

Power at J12 is-61.5 dBm @ 694.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.9 dBm @ 697.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.2 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-67.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.3 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is-64.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is-58.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.6 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.7 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.5 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.3 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.9 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.0 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is-59.5 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is-58.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.2 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-59.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is-59.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-66.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is-59.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is-62.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is-66.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

LEVEL 6
@ J12 (ESQ 97456 11-1)
03/05/92 18:17
(ONLY RUN)

PULLED OFF FREQ
(see test data sheet)

3/9?

STEP-STRESS TEST DATA SHEET

Sheet 1 of 6

UUT Serial Number (enter MSN): 815

Test Date: 03/05/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 7

A.R. Mueller

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 18:45 (TIME HR MIN)

Start DWELL: 19:15 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +117.6 (°C) (Chamber thermocouple reading) Soak @ +119 °C

Flange Temperature: +125.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +126 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +6.40 (Vdc) -5 Volts dc: -6.40 (Vdc)

+15 Volts dc: +17.10 (Vdc) -15 Volts dc: -17.10 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1093 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 19:30 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 149.2 (mA) -5 Volts dc: 100.3 (mA)

+15 Volts dc: 142.3 (mA) -15 Volts dc: 585.7 (mA)

End TEST: 19:32 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 6

UUT Serial Number (enter MSN): 815

Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input From 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 19:33 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 I (msec) / T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 I (msec) / T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.64/9.60	48.8	4.80/9.60	50.0	Pd. 1.8 msec/
	I > Q	4.56/	47.5	4.56/	47.5	
	I + Q > 0	4.65/	48.8	4.84/	50.0	
	Q > 0	4.64/	48.8	4.68/	48.8	
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	5.12/9.60	53.3	4.84/9.60	50.0	
	I > Q	4.88/	50.8	4.80/	50.0	6 dr. 1.6 msec/
	I + Q > 0	4.72/	49.2	4.80/	50.0	
	Q > 0	4.72/	49.2	4.80/	50.0	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/96 (FRI)

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 604 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q -Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.68/5.60	48.8	4.80/5.60	50.0	
	I > Q	4.68/	48.8	4.68/	48.8	5.0 us 120 pulses
	I + Q > 0	4.80/	50.0	4.80/	50.0	
	Q > 0	4.68/	48.8	4.80/	50.0	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.80/5.60	50.0	4.80/5.60	50.0	
	I > Q	4.80/	50.0	4.80/5.60	50.0	
	I + Q > 0	4.80/	50.0	4.80/	50.8	6.0 us 1.60 pulses
	Q > 0	4.80/	50.0	4.80/	50.0	

End TEST: 15:40 (HOUR MIN MSN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/96 (FRI)

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 19:41 (HOUR MIN MSN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *measure for cable losses
50 min (68)	616.0	-9.6 (6)	624.0	-8.1	Both Synths are tracking each other and voltages appear OKAY /DM
35 max (68)	660.9	+7.9 (6)	667.8	+10.4	
18 min (88)	736.7	+12.1 (66)	737.0	+12.4	
00 max (115)	805.6	+11.6 (12)	799.4	+12.6	

JS KNOWN ANOMALY

Additional Testing (OPTIONAL); **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT (Check here) NO. off freq --

End TEST: 20:01 (HOUR MIN MSN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUE ON TO LEVEL 8 End DWELL: 20:15 (HOUR MIN MSN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter SSN): 815

Test Date: 03/05/92

Tester: (Name & rating below)

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

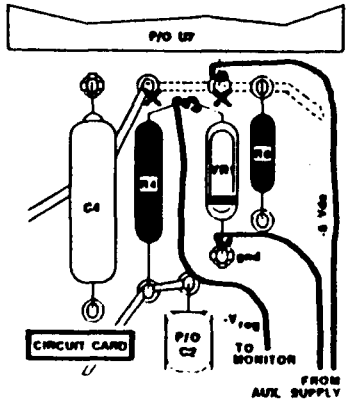
Start TEST: 19:32 (TIME RELIABILITY)

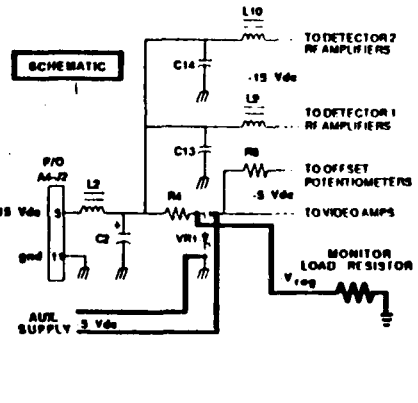
Voltage across LOAD RESISTOR: -5.2615 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 19:32 (TIME RELIABILITY)

315

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





Reload plot routine from 20:00 to 20:10
Begin Plot 2, Disk 2

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 8

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 20:15 (hour hr min)

Start DWELL: 20:45 (hour hr min)

STEP-STRESS Level Chamber Air Temperature: +125.4 (°C) (Chamber thermocouple reading) Safe +127 °C

Plenge Temperature: +133.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +134 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: -6.60 (Vdc)

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: -17.40 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1093 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 20:48 (hour hr min)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1541.7 (mA) -5 Volts dc: 89.2 (mA) decreased 11 mA

+15 Volts dc: 1307 (mA) decreased 11.6 mA -15 Volts dc: 597.4 (mA)

End TEST: 20:50 (hour hr min) KNOWN ANOMALY

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 20:52 (hour hr min)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.64/960	48.8	4.64/960	48.8	8 div 1.20 usec/div
	I > 0	480/	50.0	4.64/	47.5	
	I + Q > 0	480/	50.0	480/	50.0	
	Q > 0	4.64/	48.8	480/	50.0	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.96/960	Anomaly 51.7	4.64/960	50.8	6 div 1.60 usec/div
	I > 0	480/	50.0	4.64/	48.3	
	I + Q > 0	480/	50.0	4.96/	51.7	
	Q > 0	480/	50.0	4.72/	49.2	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Lissnt T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Lissnt T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/5.60	50.0	4.80/5.60	50.0	
	I > Q	4.68/	48.8	4.68/	48.8	8 div
	I < Q > 0	4.80/	50.0	4.80/	50.0	
	Q > 0	4.80/	50.0	4.80/	50.0	
Other Specify (dBm)	I > 0					
	I > Q					
	I < Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I < Q > 0					
	Q > 0					
-75 dBm	I > 0	4.96/9.60	51.7	4.80/9.60	50.0	
	I > Q	4.80/	50.0	4.56/	50.8	6 div
	I < Q > 0	4.80/	50.0	4.80/	50.0	
	Q > 0	4.96/	51.7	4.96/	51.7	

End TEST: 21:01 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST. At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 21:02 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*corrected for cable losses)
50 min	606.6	-15.9	610.5	-16.1	(A) 2nd Pass
35 mm	772.4 (A)	65.7	758.4 (A)	+12.6	
18 mm	721.2	+11.8	716.4	+11.9	
00 mm	702.3	+11.6	768.7	+12.6	

KNOWN ANOMALY

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT (Check block) NO

Used frequency sweep test #2 to exercise. Both Synths are sweeping & are locked (21:24)

End TEST: 21:28 (TIME HR MIN) NO FAILURES

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at the STEP-STRESS Level.

UUT is operating very well given Stress Levels. Proceed to next Level 9. End DWELL 21:45 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 815

Test Date: 03/05/92

Tester: (Name & organization)

STEP-STRESS Level (enter 0 - 10): 8

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

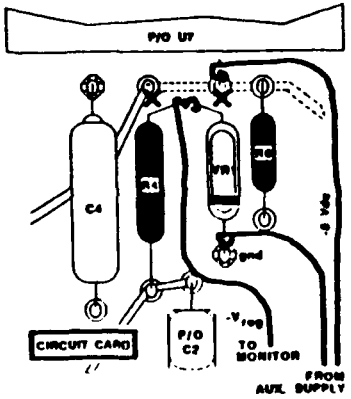
RESISTOR/ZENER DIODE MODIFICATION: At Depot: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

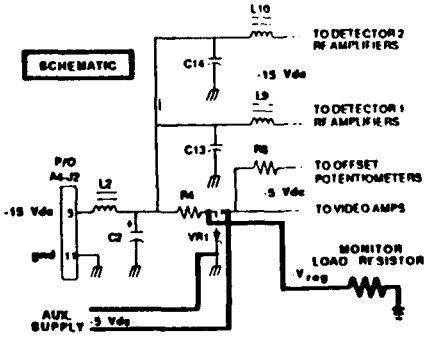
Start TEST: 20:51 (TYME HR:MIN)

Voltage across LOAD RESISTOR: -5.2775 (Vdc) ✓ (refer to Appendix D, nominally -5 Vdc)

End TEST: 20:51 (TYME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

Tester: (Name & many below)

STEP-STRESS Level (enter 0 - 10): 9

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 21:45 (Hour Hr Min) Start DWELL: 22:15 (Hour Hr Min)

STEP-STRESS Level Chamber Air Temperature: +133.3 (°C) Soak @ +135°C (Chamber thermocouple reading) Plenum Temperature: +141.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +142 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp, Increment Voltage to STEP-STRESS Level (Record settings in box)

Supply Voltages: +5 Volts dc: +6.80 (Vdc) -5 Volts dc: -6.80 (Vdc)

+15 Volts dc: +17.70 (Vdc) -15 Volts dc: -17.70 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1094 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 22:20 (Hour Hr Min)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 407.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 160.35 (mA) -5 Volts dc: 93.4 (mA) Steady increasing again

+15 Volts dc: 112.8 (mA) -15 Volts dc: 608.3 (mA)

End TEST: 22:22 (Hour Hr Min) decreased another 19.9 mA KNOW ANOMALY

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 22:23 (Hour Hr Min)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 407.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50.0	468/960	48.8	
	I > 0	468/	48.8	480/	47.5	
	I + Q > 0	468/	48.8	480/	50.0	
	Q > 0	468/	48.8	480/	50.0	
Other: Specify 72 (dBm)	I > 0	496/960	51.7			
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify ___ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0	Noisy See above				
-75 dBm	I > 0	[illegible]	[illegible]	480/960	46.7	* use Data bit Q > 0 being measured
	I > 0	480/	50.0	480/	50.0	
	I + Q > 0	480/	50.0	496/	51.7	
	Q > 0	448/	46.7	480/	50.0	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L(usec) T(usec)	Detector 1 Duty Cycle (percent)	Detector 2 L(usec) T(usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	492/960	51.2	4.68/9.60	48.8	8 div 1.20 usec/div
	I > Q	4.68	48.8	4.80	50.0	
	I + Q > 0	4.80	50.0	4.92 / 9.60	51.2	
	Q > 0	4.68	48.8	4.80	50.0	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	5.12/9.60	53.3	4.92/9.60	51.7	6 div 1.60 usec/div
	I > Q	4.72	49.2	4.80	50.0	
	I + Q > 0	4.80	50.0	5.12	53.3	
	Q > 0	4.68	46.7	4.80	50.0	

End TEST: 22:34 (HHMM HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/05/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 22:35 (HHMM HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	5900 / 885 @ 1180	-26.7 / -5.0	5920 / 880.9	-24.9 / +2.4 @ 1181 -45	KNOWN ANOMALY
35 min	6334 / 950.6	-2.1 / -7.0	6343 / 952.8	-1.9 / +2.8 @ 1268 -47	
18 min	6973 / 1046.0	+11.1 / -37	6890 / 1035	+11.6 / -36	SYNTH'S SHIFTED LOW IN FREQUENCY BY VOLTAGE APPLIED. POWER OUTPUT STRONG WHEN WITHIN BANDPASS OF FILTER & DO TUNE RANGE
00 min	747.1 / 1121	+11.6 / -48	730.6 / 1096	+12.0 / -45	

Additional Testing (OPTIONAL); **RADIO FREQUENCY OUTPUT TEST**: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check Y/N)

Use Test Sweep Test #2 to Exercise Synth @ 12:54 BOTH STILL HAPPING NO FAILURES

End TEST: VERY WELL 23:15 (HHMM HR MIN)

SIGNALS ARE STABLE ALSO SINGLE FREQ ANOMALY YET.

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

UUT STILL WORKING WELL THIS LEVEL. MONITOR UNTIL END OF DWELL THEN INCREASE TO NEXT LEVEL TO ALL DETECTOR BITS STILL PRESENT J.R. Mueller 23:15

End DWELL: 23:15 (HHMM HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 815

Test Date: 03/05/92

Tester: (Name & ramp button)

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

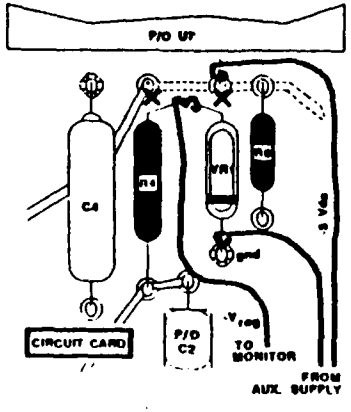
Start TEST: 22:22 (THHR MN:MIN)

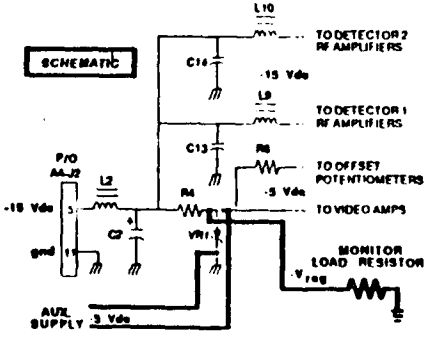
Voltage across LOAD RESISTOR: -5.2923 (Vdc) (refer to Appendix D: nominally 1 Vdc)

End TEST: 22:22 (THHR MN:MIN)

321

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

UUT Serial Number: 815 Test Date: 03/05/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 10

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 23:15 (HR:MIN) Start DWELL: 23.45 (HR:MIN)

STEP-STRESS Level Chamber Air Temperature: +140.8 (°C) (Chamber thermocouple reading) Soak @ +143 °C

Flange Temperature: +149.5 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +150 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +7.00 (Vdc) -5 Volts dc: -7.00 (Vdc)

+15 Volts dc: +18.00 (Vdc) -15 Volts dc: +18.00 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1094 (Vdc)

Turned Down Synth 37 clock down 5 more steps to 30 MHz 23:20

22 MHz @ 23:37
30 MHz @ 23:46

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 23:47 (HR:MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1663.0 (mA) -5 Volts dc: 105.4 (mA)

+15 Volts dc: 126.7 (mA) -15 Volts dc: 620.9 (mA)

End TEST: 23:50 (HR:MIN)

Near limit B values Still 15 bad bits Word value 2 bits

KNOW ANOMALY

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 815 Test Date: 03/05/92 - 03/06/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (L/T) for each UUT Digital Output. Repeat with setting for Channels 30 at this STEP-STRESS Level.

Start TEST: 23:51 (HR:MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig (Input)	I & Q Bits	Detector 1 L (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	460/960	50.0	468/960	48.8	
	I > 0	468/	48.8	468/	48.8	8 dBm
	I + Q > 0	468/	48.8	468/	48.8	1.20 μsec/div
	Q > 0	480/	50.0	468/	48.8	REFL
Other Specify	I > 0	UNIT JUST EXPERIENCED SUPPLY ANOMALY @ 23:55 DETECTOR BITS GONE. SEE ABOVE DATA BELOW				
-72 (dBm)	I > 0					
	I + Q > 0					SUPPLIES AT P00:03 03/06/92 +7.00V 1625.8 mA; -0.89V 293 Amps; +18.00V 1067 mA; -18.00V 603.7 mA; AUX -5.1094V 46.2 mA; LOAD -5.3285
	Q > 0					
Other Specify	I > 0					
	I > 0					
(dBm)	I + Q > 0			+5.46 Vdc		
	Q > 0	SEE ABOVE				LEAVE POWER CONNECTED UNTIL END OF DWELL
-75 dBm	I > 0	VLP/960 NOISY		/960	+5.74 Vdc	
	I > 0	/	+5.60 Vdc	/	+5.74 Vdc	60 ns
	I + Q > 0	/	+5.60 Vdc	/	+5.53 Vdc	@ 23:58
	Q > 0	/	+5.67 Vdc	/	+5.53 Vdc	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 1 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/06/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 484 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 Rm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	1660		1560		
	I > Q	1		1		8 div 1.20 msec/div
	I + Q > 0	1		1		
	Q > 0	1		1		
Other Specify (dBm)	I > 0					SEE SHEET 2 FOR ANOMALY
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1060		1560		
	I > Q	1		1		6 div 1.60 msec/div
	I + Q > 0	1		1		
	Q > 0	1		1		

End TEST: (HHMM MM MM)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/06/92

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 00:05 (HHMM MM MM) * ANOMALY WITH -5V SUPPLY STILL PRESENT HERE & THROUGH END OF DWELL

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *account for cable losses
50 min	765.0	+10.8	765.2	+12.2	
35 min (A)	766.7	+10.8 (A)	765.3	+12.2 (A)	BOTH OUTPUTS ARE FIXED IN FREQUENCY. WILL NOT HOP
18 min	791.2	+12.0	812.2	+9.2	
00 min	864.7 (B)	+5.1 (B)	831.2 (B)	+11.2 (B)	-5V SUPPLY MAY BE AFFECTING OPERATION THERE MAY BE ASCILLATION OR HARMONIC

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this **STEP-STRESS TEST DATA SHEET**. Label attachment with ULT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

Use Frequency Survey Test #2 to Observe @ Execution @ 00:18 BOTH SYNTH'S NOW HOPPING AT A FEW FREQUENCIES, VISIBLE FROM 750 to 850 MHz ONLY.

End TEST: 00:30 (HHMM MM MM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

REDUCE STRESS TO CHECK -5V ANOMALY & VERIFY SYNTHS ARE UNAFFECTED. GO TO LEVEL 0 & RETEST

End DWELL 00:45 (HHMM MM MM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 815

Test Date: 03/05/92

Tester: (Name & signature below)

STEP-STRESS Level (enter 0 - 10): 10

L.D. Mueller

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

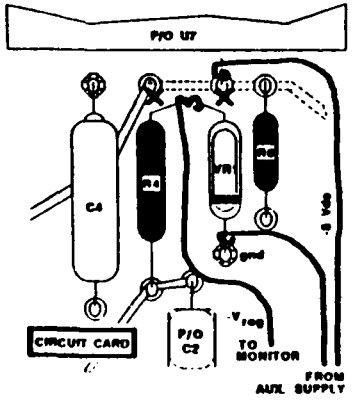
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

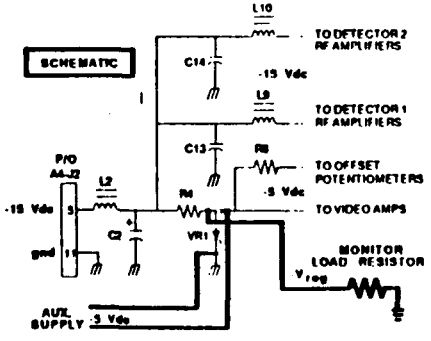
Start TEST: 23:50 (military time)

Voltage across LOAD RESISTOR: -5.3085 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 23:51 (military time)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/06/92

Tester: (Name & name below)

STEP-STRESS Level (enter 0 - 10): 9 (RETEST)

* DATA WITH ANOMALY PRESENT (FROM 01:16 TO 01:23)

** DATA WITH DETECTOR CONNECTOR J2 DISCONNECTED FROM STATION 10J3. (FROM 01:23 TO)

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 00:45 (TIME HR:MIN) (Manual Mode) ANOMALY MAINTAINED FOREMAN RAMP Start DWELL: 01:15 (TIME HR:MIN)

STEP-STRESS Level Chamber Air Temperature: +133.5 (°C) (Chamber thermocouple reading) Set to +135°C Flange Temperature: +141.6 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +142 (°C) (refer to Appendix D Table)

32J3

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.80 *** (Vdc) -5 Volts dc: -6.89 *** (Vdc) ← 01:23 (-0.847 *)

+15 Volts dc: +17.70 *** (Vdc) -15 Volts dc: -17.70 *** (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1096 *** (Vdc) -5.1102

Aux Current 46.7 * 01:18

27.3 ** 01:28

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 01:16 * 01:25 ** (TIME HR:MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1475.2* 1490 ** (mA) -5 Volts dc: 2.82A * 37.6 ** (mA)

+15 Volts dc: 98.6 * 60.9 ** (mA) -15 Volts dc: 594.1 * 234 ** (mA)

End TEST: 01:18 * 01:27 ** (TIME HR:MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/06/92

STEP-STRESS Level (enter 0 - 10): 9 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell, Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -.75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 01:19 * (TIME HR:MIN)

* DATA WITH ANOMALY PRESENT

** DETECTOR CONNECTOR J2 DISCONNECTED

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -.75 dBm

Rev Sig Input	I & Q -Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	+5.46 Vdc		+5.60 Vdc		Measure Output Voltage Levels only *
	I < 0	+5.53 Vdc		+5.60 Vdc		
	I + Q > 0	+5.53 Vdc		+5.53 Vdc		
	Q > 0	+5.53 Vdc		+5.53 Vdc		
Other Specify (dBm)	I > 0					Measure Output * ** 01:25
	I < 0					
	I + Q > 0			+1.75 Vdc offset add Bits		
	Q > 0					
Other Specify (dBm)	I > 0					
	I < 0					
	I + Q > 0					
	Q > 0					
-.75 dBm	I > 0					
	I < 0					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: B15 Test Date: 03/06/92

STEP-STRESS Level: 9 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued.

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					SEE SHEET 2
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: 01:23 (HH:MM:SS MM) = DISCONNECT ** AND LEAVE UNTIL COMPLETION OF LEVEL 9 TEST, THIS LITTLE BLEEDER IS NECESSARY TO REMAIN AT AT LEVEL 9 FINAL.

TEST continued next page

3261

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: B15 Test Date: 03/06/92

STEP-STRESS Level: 9 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST. At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 01:31 (HH:MM:SS MM) ** DATA WITH DETECTOR CONNECTOR J8 DISCONNECTED @ STATION

Channel	Synthesizer 1 (J3) Frequency (MHz)	Synthesizer 1 (J3) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *comments for cable losses
50 min	how 662.9	+8.3	how 661.3	+9.4	Need to verify @ Level 0 FINAL
35 min	637.9	-0.53	639.0	+1.2	
	960	-9.0	958.2	-5.4	
18 min	703.0	+11.2	696.1	+12.1	
00 min	756.5	+11.5 (power good)	742.7	+12.2 (power good)	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST. At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

End TEST: 01:41 (HH:MM:SS MM) **

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS. The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

LEAVE DETECTOR DISCONNECTED AT STATION & REDUCE CHAMBER TEMP TO LEVEL 0 FOR FINAL

End DWELL: 01:45 (HH:MM:SS MM) (ELAPSED DWELL 00:30 HRS MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (xxxx-xxxx): 815 — Test Date: 03/06/92

Tester: (Name & stamp below)

STEP-STRESS Level (xxxx-0 - 9): 9 (RETEST)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Depot: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 01:18 # / 01:28 ## (hours min sec)

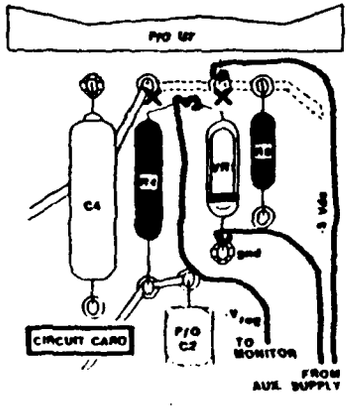
Voltage across LOAD RESISTOR: -5.315 # / +1.696 ## (Vdc) (refer to Appendix D; nominally -1 Vdc)

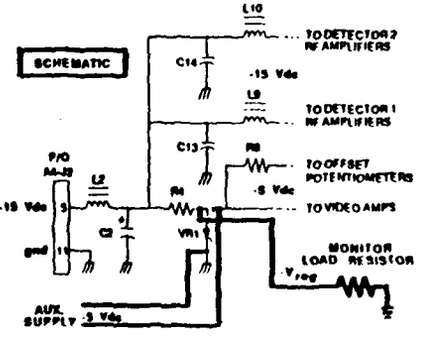
End TEST: 01:18 # / 01:30 ## (hours min sec)

S/B -5 V 1/2 IS Supplied by detector connector J104

3271

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND P4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/06/92

Tester: (Name & stamp below) L.D. Mueller (ESS 92466)

STEP-STRESS Level (enter 0 - 10): 0 FINAL

** DETECTOR CONNECTOR J2 DISCONNECTED AT STATION 10J3

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 01:45 (HHMM HR MIN) (Prog = 3 (1 Loop)) Ramp = 36 min Start DWELL: 03:05 (HHMM HR MIN)

STEP-STRESS Level Chamber Air Temperature: +61.3 (°C) (Chamber thermocouple reading) Set at +61°C

Flange Temperature: +65.1 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +70 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: ** +5 Volts dc: +5.00 (Vdc) -5 Volts dc: -5.00 (Vdc) (Recount @ 03 22 -0.800 vdc)

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.00 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1103 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 03:06 (HHMM HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: ** +5 Volts dc: 1129.4 (mA) -5 Volts dc: 39.6 (mA) (Recount @ 03 22 2.94 Amps)

+15 Volts dc: 57.7 (mA) -15 Volts dc: 193.5 (mA)

End TEST: 03:07 (HHMM HR MIN)

Disconnect J2 10J3 again @ 03 23

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 815 Test Date: 03/06/92 (ESS 92466)

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: FAILURE (HHMM HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bus	Detector 1 t (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	1/960		1/960		5 d.u. 1.80 usec/d.u.
	I > 0	1		1		
	I + Q > 0	1		1		
	Q > 0	1		1		
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1/960		1/960		4 d.u. 160 usec/d.u.
	I > 0	1		1		
	I + Q > 0	1		1		
	Q > 0	1		1		

— NO TEST — -5V Supply FAILURE ASSOCIATED w/ DETECTOR

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): B15 Test Date: 03/06/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Limit T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	660		660		8 div @ 1.20 μsec/
	I > Q	1		1		
	I + Q > 0	1		1		
	Q > 0	1		1		
Other Specify (dBm)	I > 0	1				SEE SHEET 2
	I > Q	1				
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0			1		
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1560		1560		6 div @ 1 μsec/
	I > Q	1		1		
	I + Q > 0	1		1		
	Q > 0	1		1		

End TEST: FAILURE (HHMM MS MSS)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): B15 Test Date: 03/06/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 03:08 (HHMM MS MSS)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *measure for cable losses
50	684.0	+11.6	684.0	+12.0	NO SYNTHESIZER FAILURES FOUND
35	729.0	+12.5	729.0	+12.5	
18	825.0	+13.2	825.0	+13.2	
00	921.0	+11.4	921.0	+12.8	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level Tester Name & Date. ATTACHMENT (Check here)

End TEST: 03:20 (HHMM MS MSS)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

FAILURE HAD OCCURRED AT LEVEL 10 End DWELL: 04:05 (HHMM MS MSS)

SEE REPORT #27387. 03/06/92

STEP-STRESS LEVEL COMPLETE

Ramp to Room Temp

UUT POWERED OFF AT 04:30 03/06/92

(J2 DISCONNECTED @ 03 25)

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: B15 Test Date: 03/06/92

Tester: (Name & stamp below)

STEP-STRESS Level: 0 FINAL

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Depot: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 03:22 (Reconnect to monitor)

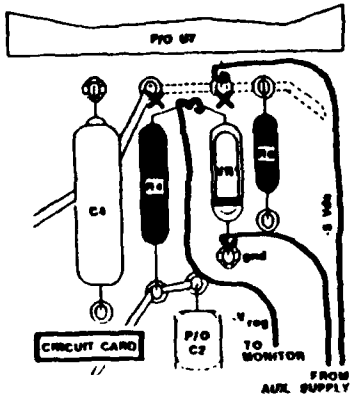
Voltage across LOAD RESISTOR: -5.1542 (Vdc) (refer to Appendix D; normally 5 Vdc)

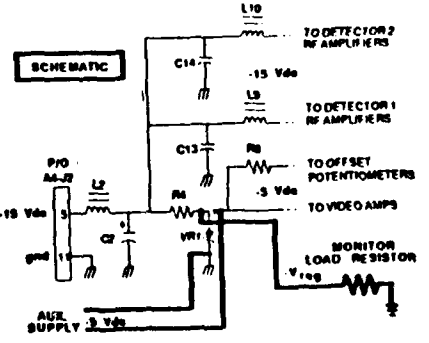
End TEST: 03:23

Disconnect from P 03:23

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 185 @ J5

STEP-STRESS TEST
LEVEL Ø FINAL
03/06/92 03:13
(CCC 92466 TEST) dBm
(J2 DETECTOR FOR DISCONNECTED @ 10 J3 DUE TO FAILURE)

Power at J5 is 11.6 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.0 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.1 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 13.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 921.0 MHz (Spec=+9dBm minimum).

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 815 @ J12

STEP-STRESS TEST
LEVEL Ø FINAL
03/06/92 03:18
(SSB 92466 TEST) dBm
(J2 DETECTOR FOR DISCONNECTED @ 10 J3 DUE TO FAILURE)

Power at J12 is 12.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.1 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.2 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 13.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

TEST EQUIPMENT & CALIBRATION LOG

Maintain Log for testing conducted 03/02/92 through 03/06/92

Item	DESCRIPTION	Manuf. & Part No.	ID NUMBER	LAST CAL*	CAL* DUE	Item Notes
01	T/R Test Station	HAC; SPECIAL	F-A15223		NCR	G-132043
02	Control Panel	HAC; SPECIAL	G-132290		NCR	
03	Signal Generator	HP; 8660C	G-128061	12-17-91	01-13-93	
04	Auxiliary Section	HP; 866318	G-128062		NCR	PN ITEM 03
05	RF Section	HP; 86603A	G-128063	12-17-91	01-13-93	PN ITEM 03
06	Spectrum Analyzer	HP; 8568A w/ Opt E16	G-132082	12-11-91	10-30-92	
07	FET Probe	HP; 1120A	G-132055	12-14-90	04-30-92	PER CAL
08	Power Meter	HP; 436A	G-128036	06-18-91	11-24-92	"
09	Power Sensor	HP; 8482A	G-128059	09-09-91	10-21-92	"
10	Oscilloscope	HP; 1980B	G-132049	09-24-91	08-11-92	
11	Digital Multimeter	SystronDonner; 7344A	G-127998	06-06-91	08-18-92	
12	Digital Multimeter	HP; 3478A	H-A53624	09-06-91	06-25-92	
13	Power Splitter	MiniCkts; ZFSC-2-5	No ID ✓		NCR	
14	Power Splitter	MiniCkts; ZFSC-2-5	No ID ✓		NCR	
15	Reg. Power Supply	Lambda; LP-531-FM	G-132292		NCR	+15V
16	Reg. Power Supply	Lambda; LP-531-FM	"		NCR	-15V
17	Reg. Power Supply	Lambda; LP-530-FM	G-132291		NCR	+5V
18	Reg. Power Supply	Lambda; LP-520-FM	"		NCR	-5V
19	Computer	HP; 9845B	G-128012		NCR	
20	Flex. Disk Memory	HP; 9895A	G-133309		NCR	
21	Signal Generator					
22	Oscilloscope	Tektronix; 2465				
23	Digital Multimeter					
24	Digital Multimeter					
25	Digital Multimeter					
26	Thermal Chamber	Thermotron; S-4 w/Cntl	H-B07567	09-10-91	09-02-92	
27	Data Acqtn Cntl Unit	HP; 3497A	H-428499	11-14-91	07-29-93	
28	Computer	HP; Model 85	H-A64429		NCR	
29	Power Supply, AUX.	HP; 6299A	H-357054		NCR	-5.1V
30	PLOTTER	HP; 7470A	H-512478		NCR	
31	PRINTER	HP; THINKJET	E-A08763		NCR	
32						
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						

*NCR = Non Calibration Required

CALIBRATION ROUTINE PERFORMED: 03-02-92; 15:52 PRIOR TO TESTING

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DATA RETAINED FOR TEST OF MSN 0815 03/05/92 rev 03/06/92

DATE: [redacted] 03/02/92 TIME: [redacted] 15 52

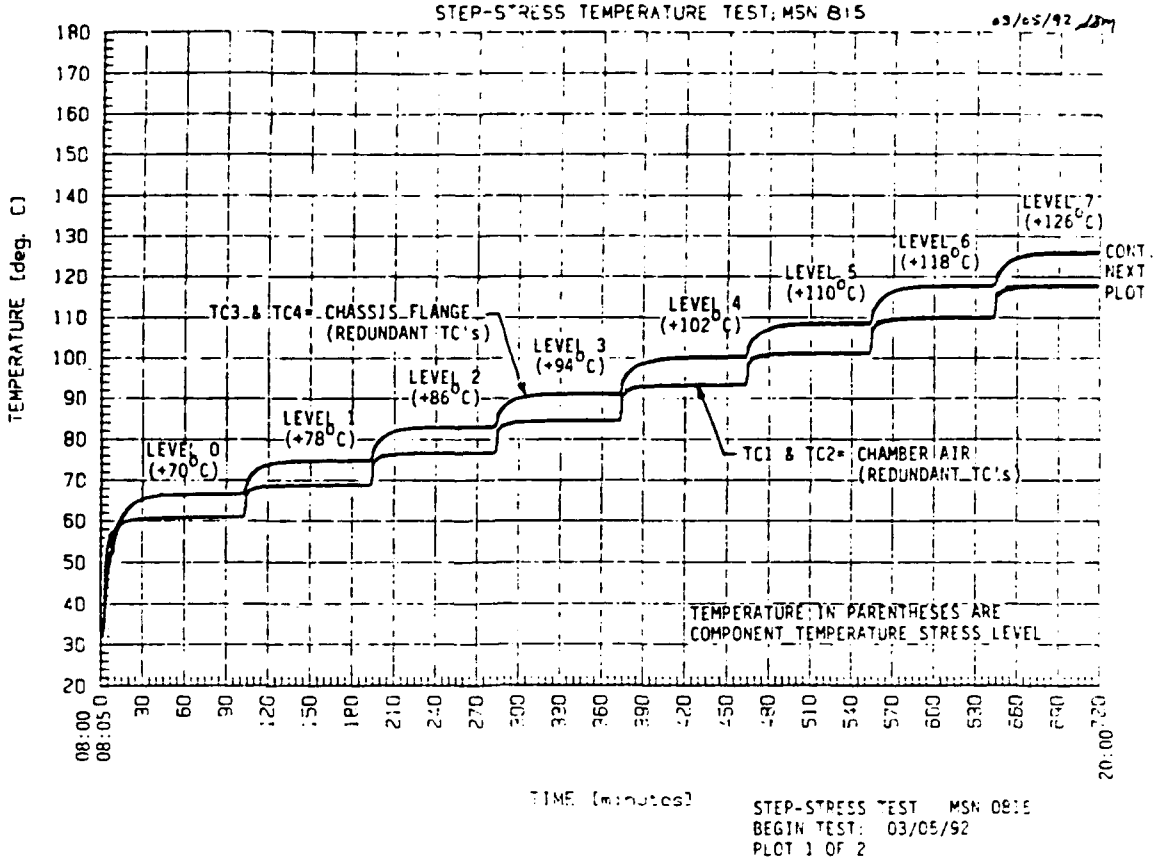
STEP-STRESS TEST CALIBRATION DATA

(CABLES J8 & J12)

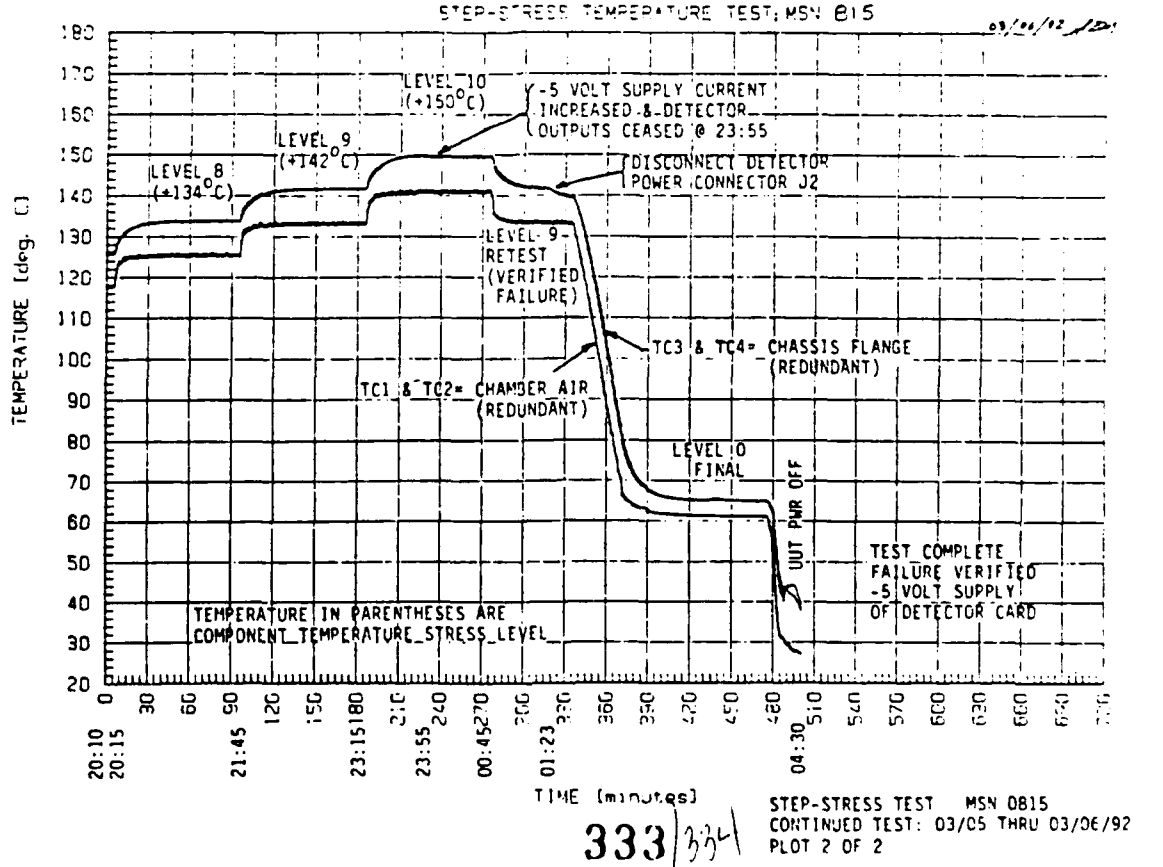
ESR 15246 TEST

Synth_ref = 1433930
Freq_mod_ref = 3339930
Sc_clock_output = 0
Phase_lo_output = 1.12
Phase_if_output = 0
Up_dn_conv_lo = 3.37
317.75_lo = 14.9 dBm /313.75177EEMHz

Channel	Freq	Dn_conv_output	Synth_lo_output	Mit_sgnl_i_o
(50)	684	1.2	1.27	2.17
49	687	1.19	1.17	2.13
48	690	1.18	1.12	2.11
47	693	1.21	1.23	2.11
46	696	1.29	1.32	2.03
45	699	1.34	1.4	1.92
44	702	1.39	1.3	1.89
43	705	1.44	1.32	1.95
42	708	1.41	1.39	1.96
41	711	1.37	1.4	1.83
40	714	1.32	1.36	1.83
39	717	1.32	1.43	1.92
38	720	1.38	1.59	1.91
37	723	1.43	1.67	1.92
36	726	1.45	1.66	1.75
(35)	729	1.44	1.63	1.79
34	732	1.41	1.71	1.85
33	735	1.39	1.76	1.93
32	738	1.32	1.74	1.73
31	741	1.31	1.74	1.8
30	744	1.36	1.81	1.84
29	747	1.45	1.92	1.84
28	750	1.47	1.95	1.71
27	753	1.44	1.9	1.69
26	756	1.44	1.93	1.82
25	759	1.44	2	1.83
24	762	1.43	2	1.83
23	765	1.44	1.95	1.78
22	768	1.51	1.97	1.8
21	771	1.62	2.1	1.92
20	774	1.67	2.18	1.76
19	777	1.66	2.14	1.7
(18)	825	1.84	2.32	1.63
17	828	1.77	2.23	1.67
16	831	1.72	2.29	1.73
15	834	1.69	2.29	1.78
14	837	1.69	2.31	1.73
13	882	1.65	2.08	1.64
12	885	1.7	2.06	1.65
11	888	1.69	2.07	1.58
10	891	1.72	2.05	1.49
9	894	1.76	2.02	1.51
8	897	1.79	1.93	1.52
7	900	1.71	1.99	1.5
6	903	1.59	1.95	1.43
5	906	1.6	1.83	1.49
4	909	1.66	1.9	1.56
3	912	1.65	1.98	1.53
2	915	1.55	1.91	1.45
1	918	1.52	1.89	1.44
(H)	921	1.54	1.79	1.53



STEP-STRESS TEST MSN 0815
BEGIN TEST: 03/05/92
PLOT 1 OF 2



STEP-STRESS TEST MSN 0815
CONTINUED TEST: 03/05 THRU 03/06/92
PLOT 2 OF 2

*MSN 815 LOG

Test Data Cont'd: STARTS THIS PAGE Date: 03/05/92

RECEIVE MSN 1029 FOR STEP-STRESS TEST

UUT SET UP IN CHAMBER, POWERED ON, ADJUSTED VOLTAGES & VERIFIED OPERATIONAL. CHAMBER READIED AT PROGRAM # 1.

05:00 – KINCG ASSISTED IN FORMATING NEW DATA DISK. WAS HAVING PROBLEMS. FORMATTED 2 QTY DISKS

05:20 – SETUP PLOT ROUTINE WITH THERMOCOUPLES AS:

CH 1 = TC1 (CHAMBER AIR; FAR SIDE) SUSPENDED
CH 2 = TC2 (" ; NEAR DOOR)
CH 3 = TC3 (CHASSIS FLANGE; NEAR DOOR/SIDE J2)
CH 4 = TC4 (" ; FAR SIDE/J5 & J4)

D.M. Mueller 03/05/92
@ 05:29

07:00 – Turn Air on Syn/Det # 1029. Start Prgm # 1 Int # 2
07:40 – Fan failed on J5 output
07:50 – Back to ambient & removed Syn/Det # 1029
* 08:00 – Installed Syn/Det #815 Same setup as above D.M. Mueller 03/05/92
08:05 – Start Prog # 1 Int # 2
9:45 – Start Program # 2 Int # 1 Start test step thru 0
9:45 – Step stress level 0 Complete Begin ramp to level 1
10:15 – Dwell @ 69°C
11:15 – Step stress level 1 Complete Begin ramp to level 2
11:45 – Dwell @ 71°C
12:45 – Step stress level 2 Complete Begin ramp to level 3
13:15 – Dwell @ 85°C
14:15 – Step stress level 3 Complete Begin ramp to level 4
14:45 – Dwell @ 94°C
15:45 – LEVEL 4 Complete Ramp to Level 5

Data Recorder: Jam

Test Data Cont'd: MSN 815 STEP-STRESS TEST Date: 03/05/92

16:15 – Dwell LEVEL 5 (+102°C Setting)
17:15 – Level 5 Complete. Ramp to Level 6
17:45 – Dwell LEVEL 6 (+111°C Setting)
18:45 – Level 6 Complete. Ramp to Level 7
19:15 – Dwell LEVEL 7 (+119°C Setting)
20:15 – Level 7 Complete. Ramp to Level 8
20:00 770 scans complete. Plot 1 ends. Reload Routine. Plot 2, Disk 2 begins ~~20:05~~ 20:10
20:45 – Dwell LEVEL 8 (+127°C Setting)
21:45 – Level 8 Completed. Ramp to Level 9.
22:15 – Dwell LEVEL 9 (+135°C Setting)
23:15 – Level 9 Completed. UUT is very stable Both Detectors & Synthesizers are working remarkably well! Ramp to Level 10.
23:45 – Dwell LEVEL 10 (+143°C Chamber Setting).
23:55 – ANOMALY WITH -5 VOLT SUPPLY S/B AT STRESS OF -7.00 VDC IS -0.89 VOLTS AND DRAWING 2.93 AMPERES. DETECTOR J U Q BITS ALL HIGH. NO DUTY CYCLE. SYNTHS STILL HOP. COMPLETE THROUGH END OF DWELL 00:45
00:45 – MANUAL MODE GO TO RETEST AT LEVEL 9 (+135°C)
01:15 – TROUBLE-SHOOT AT LEVEL 9 DWELL
01:23 – ISOLATED FAILURE TO DETECTOR # DISCONNECTED POWER @ STATION CONNECTOR 10 J13.
01:45 – END LEVEL 9 RETEST. RAMP (Prg # 3 Int # 1) TO LEVEL 0 FOR FINAL TEST. Ramp for 36 minutes
03:05 – Start Dwell LEVEL 0 FINAL (+61°C)
04:05 – END LEVEL 0 FINAL. Ramp to Room Temp
04:30 – UUT POWERED OFF. END PLOT 2.

Data Recorder: _____

333 594

HUGHES

HUGHES AIRCRAFT COMPANY

STEP-STRESS TROUBLE & FAILURE REPORT

1 PROJECT NAME

FAM CODE | SYST CODE

FAIL CLASS	TEST TYPE	TEST ENV	FAIL CAUSE	RELEV

NO. Z 7387

2 THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE ☒ FAILURE

ORIGINATOR

3 SYSTEM SUBSYSTEM NAME	P N	S/N	4 TIMER COUNTER READINGS	5 DATE FAILED	35 REFERENCES
R/T MODULE	part no-103	815	TIME 23.25 LEVEL CLASS D: 15:50:10 (HOURS / CYCLES)	03 (MO) 05 (DAY) 92 (YR)	

6 REPORTING FACILITY	7 REPORTED BY	ORG CODE	OPERATING LOG NO
STEP-STRESS TEST c/o S D MUELLER	Steven D Mueller (SIGN) 3/06/92	1A 72 30	

8 TROUBLE FAILURE OBSERVED WAS (TEST CONDITIONS SYMPTOMS SEVERITY ETC INCLUDING "IS" AND "SHOULD BE" DATA) — TFR CONTINUATION USED ☐

AT LEVEL 10, 10-MIN INTO DWELL, DETECTOR CAUSED -5 VOLT SUPPLY TO DRAW 2.93 AMPS AND VOLTAGE TO DROP TO -0.89 Vdc (S/B -7.00Vdc ; 93 mA typical). OBSERVED WHEN I&Q BITS LOST ANY DUTY CYCLE AND WENT TO +5 VOLT RAIL. R4/VR1 MODIFICATION FOR TEST SEEMS UNAFFECTED BY FAILURE. UUT WAS AT +140.6°C CHAMBER AIR, +149.5°C FLANGE & +150°C typical COMPONENT AIR TEMP. FAILURE RETESTED AT LEVEL 9 & LEVEL 0 FINAL. SYNTHESIZER 1&2 ARE UNAFFECTED. NO VISUAL INSPECTION MADE AT THIS TIME.

9 TROUBLE FAILURE OCCURRED DURING	10 ACTION TAKEN TO CORRECT TROUBLE FAILURE
(A) ☒ ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE-FLIGHT OR CURSORY CHECK	(A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 - 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 - 20)

11 ITEM REPLACED NAME	P N	S N	12 ITEM INSTALLED NAME	P N	S N	13 DISPOSITION OF REPLACED ITEM

VERIFICATION

14 WERE OTHER TROUBLES FAILURES, NOT RELATED TO ORIGINAL NOTED? (A) ☐ NO (B) ☐ YES LIST ON NEW TFR - TFR NO _____

15 WAS REPORTED TROUBLE FAILURE VERIFIED? (A) ☐ YES (B) ☐ NO (CHECK 16 B AND EXPLAIN)

16 FAILED ITEM NAME	P N	S N	REF DESIG	MANUFACTURER

17 NEXT HIGHER ASSY NAME	P N	S N	REF DESIG	MANUFACTURER

18 (A) ☐ REWORK REQUIRED IS (B) ☐ REWORK IS NOT REQUIRED BECAUSE

19 VENDOR REWORK ANALYSIS IS REQUIRED ☐ ITR _____ CAR _____

20 DISPOSITION OF ITEM IF NOT REWORKED

21 AUTHORIZATION BY ORG CODE DATE

REWORK & RETEST

22 LIST BELOW ALL PARTS REPLACED REPAIRED OR ADJUSTED

A CIRCUIT SYMBOL	B PART NUMBER	C S N	D MANUFACTURER	E DEFECT	F REWORK ACTION TAKEN	G RECEIVING LOT NO	H APPROVED PARTS (YES / NO)	PRI FAIL

23 OTHER REWORK ACTION

24 REWORKED BY	ORG CODE	25 RETESTED BY	ORG CODE	26 RETEST RESULTS APPROVAL	DATE

27 RETEST RESULTS REPAIRED ITEM IS ACCEPTABLE FOR ☐ UNRESTRICTED USE ☐ RESTRICTED USE ☐ NOT ACCEPTABLE EXPLAIN IN BLOCK 30

28 DISPOSITION OF ITEM AFTER RETEST

29 D C

ENGINEERING

30 CAUSE OF FAILURE - COMMENTS (IF ANALYSIS NOT PERFORMED EXPLAIN)

31 BASIC CAUSE OF TROUBLE FAILURE (SELECT FROM BLOCK 1 ON REVERSE SIDE)

32 SIGNATURE ORG CODE DATE

33 CORRECTIVE ENGINEERING ACTION TAKEN (IF NONE JUSTIFY) - CONCLUSIONS

REF DOCUMENT IMPLEMENTING CORRECTIVE ACTION ED ECR ETC IS NO.

34 SIGNATURE ORG CODE DATE

11020 CS MAR 66

USE TFR CONTINUATION SHEET IF ADDITIONAL SPACE IS NEEDED

FOR RELIABILITY ANALYSIS AND FOLLOW UP SEE REVERSE SIDE OF COPY 4

Z736

STEP-STRESS TEST DATA NOTEBOOK

UNIT UNDER TEST: MSN 1029

TEST STATUS: FAILURE CONFIRMED

(DURING LEVEL 7 DWELL)

TEST SUMMARY

STEP-STRESS		START DWELL	ANOMALY/ FAILURE	END DWELL
		10-Mar-92		
LEVEL	0	7:45		8:45
LEVEL	1	9:15		10:15
LEVEL	2	10:45		11:45
LEVEL	3	12:15		13:15
LEVEL	4	13:45		14:45
LEVEL	5	15:15		16:15
LEVEL	6	16:45		17:45
LEVEL	7	18:15	Anomaly	19:15
FAILURE:			18:31	
Retest	6	19:45		20:45
Final Test	0	22:00		23:00
				10-Mar-92

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/16/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 0

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 0700 (TIME HR MIN) Start DWELL: 0745 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 60.1 (°C) Flange Temperature: 66.5 (°C)
(Chamber thermocouple reading) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 70 (°C)
(refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 15 (Vdc) -5 Volts dc: -5 (Vdc)

+15 Volts dc: 15 (Vdc) -15 Volts dc: -15 (Vdc)

Aux. Constant - 5 Volts dc Setting: -511 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 0745 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1243 (mA) -5 Volts dc: 50 (mA)

+15 Volts dc: 106 (mA) -15 Volts dc: 50 (mA)

End TEST: 0745 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/16/92

STEP-STRESS Level (enter 0 - 10): C

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 0746 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Data	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	496/976	50	496/976	49.8	t / T
	I > Q	486/976	49.8	"	"	
	I + Q > 0	496/976	50	496/976	50	
	Q > 0	"	"	486/976	49.8	
Other Specify (dBm)	I > 0	496/976	50			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1.116 noisy		546/976	56.5	
	I > Q	546/976	56.5	"	"	
	I + Q > 0	496/976	51	"	"	
	Q > 0	"	"	496/976	51	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/16/12

STEP-STRESS Level (enter 0 - 10): C

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q -Bits	Detector 1 L (msec) T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 L (msec) T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.64m/9.6m	48.3	4.64m/9.6m	48.3	
	I > Q	"	"	"	"	
	I + Q > 0	4.64m/9.6m	50	4.64m/9.6m	50	
	Q > 0	"	"	4.64m/9.6m	48.3	
Other: Specify -72 (dBm)	I > 0	4.92m/9.6m	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1.1/12 msec		5.04m/9.6m	52.5	
	I > Q	4.92m/9.6m	51.2	4.92m/9.6m	51.2	
	I + Q > 0	4.54m/9.6m	50	5.04m/9.6m	52.5	
	Q > 0	4.64m/9.6m	48.3	4.92m/9.6m	51.2	

End TEST: 09 15 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/12

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 08 15 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations
50 min	684	10.37	634	11.87	*measured for cable losses
35 min	729	10.67	729	12.07	
18 min	825	10.27	825	11.77	
00 min	921	9.25	921	10.05	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 09 30 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: Test Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 09 45 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (same MSN): 109

Test Date: 3/10/9✓

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

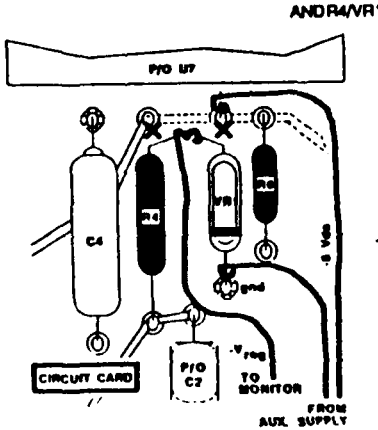
Start TEST: 09:30 (Hour, min, sec)

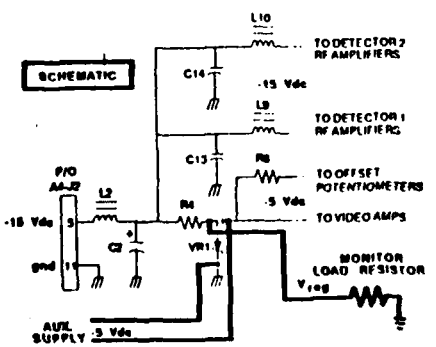
Voltage across LOAD RESISTOR: -5.15 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 09:31 (Hour, min, sec)

343

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





7/10/92
Syn 1 Ref A1029
Stress level C
J5 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 5.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 3.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.1 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is .9 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is .3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 892.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.3 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is .9 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is .3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 892.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/10/92
Syn/Oct #1029
Stress level 0
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 8.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than 698.0 MHz which is below the specified frequency.
Power at J12 is 5.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 703.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 711.0 MHz which is above the specified frequency.
Power at J12 is 8.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 823.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 823.0 MHz which is above the specified frequency.
Power at J12 is 9.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

34.5

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.5 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 703.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 1

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 08:45 (TIME HR:MIN) Start DWELL: 09:15 (TIME HR:MIN)

STEP-STRESS Level Chamber Air Temperature: 64.4 (°C) (Chamber thermocouple reading) Flange Temperature: 75.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 21.69 18 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 5.2 (Vdc) -5 Volts dc: -5.2 (Vdc)

+15 Volts dc: +15 (Vdc) -15 Volts dc: _____ (Vdc)

Aux. Constant -5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 09:50 (TIME HR:MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 130.3 (mA) -5 Volts dc: 85 (mA)

+15 Volts dc: 16.9 (mA) -15 Volts dc: 5.6 (mA)

End TEST: 09:51 (TIME HR:MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 09:51 (TIME HR:MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	468ns/1.66	48.5	444ns/1.66	48.5	
	I > Q	"	"	"	"	
	I + Q > 0	456ns/1.66	50	456ns/1.66	50	
	Q > 0	"	"	948ns/1.66	47.5	
Other: Specify -12 (dBm)	I > 0	492ns/1.66	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1 Hz noisy		492ns/1.66	51.2	
	I > Q	540ns/1.66	32.5	"	"	
	I + Q > 0	456ns/1.66	50	"	"	
	Q > 0	1.85us/1.66	48.1	"	"	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1629 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Bits	Detector 1 Linear T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 Linear T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	496u/496u	49.5	496u/496u	49.7	
	I > Q	"	"	"	"	
	I + Q > 0	496u/496u	50	496u/496u	50	
	Q > 0	"	"	496u/496u	49.1	
Other: Specify -72 (dBm)	I > 0	496u/496u	51 ✓			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1/16 496u		496u/496u	51.2	
	I > Q	496u/496u	51 ✓	"	"	
	I + Q > 0	496u/496u	50	"	"	
	Q > 0	496u/496u	49.1	496u/496u	50	

End TEST: 10:05 (TYPE HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1629 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 10:05 (TYPE HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measured for cable losses
50 min	684	10.27	684	11.97	
35 min	729	10.57	729	11.78	
18 min	825	11.37	825	12.47	
00 min	921	9.15	921	10.25	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 10:04 (TYPE HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 10:15 (TYPE HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1029

Test Date: 3/12/97

Tester: (Please ID stamp below)

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

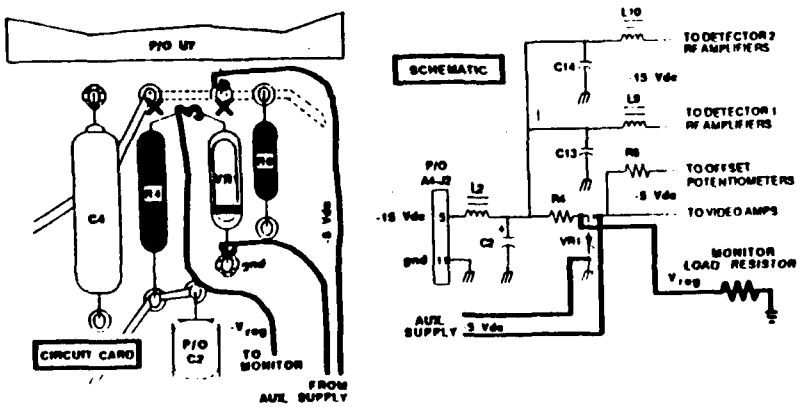
RESISTOR/ZENER DIODE MODIFICATION: At Depot: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 10:04 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.16 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 10:65 (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/10/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

sample # 1029
stress level 1
J5 output

****

Power at J5 is 3.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 2.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 9.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.0 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.6 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.1 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is-6.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/10/92
Syn Det #1029
Stress level 1
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 1.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than 690.0 MHz which is below the specified frequency.
Power at J12 is 5.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 693.0 MHz which is above the specified frequency.
Power at J12 is 6.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 696.0 MHz which is above the specified frequency.
Power at J12 is 4.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 711.0 MHz which is above the specified frequency.
Power at J12 is 7.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 823.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is less than 903.0 MHz which is below the specified frequency.
Power at J12 is 6.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.5 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is .6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/92

Tester: (Name & ramp below)

STEP-STRESS Level (enter 0 - 10): 2

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 10:15 (TIME HR MIN) Start DWELL: 10:45 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 76.2 (°C) Flange Temperature: 82.5 (°C)
(Chamber thermocouple reading) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 86 (°C)
(refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 4.54 (Vdc) -5 Volts dc: -5.0 (Vdc)

+15 Volts dc: +15.6 (Vdc) -15 Volts dc: -15.6 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 11:00 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1320 (mA) -5 Volts dc: 91 (mA)

+15 Volts dc: 109 (mA) -15 Volts dc: 52.1 (mA)

End TEST: 11:01 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs For Channel 00. Decrease Received Signal Input From 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 11:01 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 t (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.64 µs/9.6 µs	48.3	4.62 µs/9.6 µs	48.2	
	I > Q	"	"	"	"	
	I + Q > 0	4.8 µs/9.6 µs	50	4.8 µs/9.6 µs	50	
	Q > 0	"	"	4.6 µs/9.6 µs	48.8	
Other: Specify -71 (dBm)	I > 0	4.92 µs/9.6 µs	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.64 µs/9.6 µs	48.3	4.92 µs/9.6 µs	51.2	
	I > Q	5.04 µs/9.6 µs	52.5	"	"	
	I + Q > 0	4.8 µs/9.6 µs	50	"	"	
	Q > 0	4.42 µs/9.6 µs	49.8	4.8 µs/9.6 µs	50	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter NSN): 1029 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L (nsec) T (sec)	Detector 1 Duty Cycle (percent)	Detector 2 L (nsec) T (sec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	46ns/916ns	49.8	46ns/916ns	48.8	
	I > Q	"	"	"	"	
	I + Q > 0	49ns/916ns	50	49ns/916ns	50	
	Q > 0	"	"	46ns/916ns	49.5	
Other: Specify -71 (dBm)	I > 0	49ns/916ns	48.8			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	little noise		49ns/916ns	51.2	
	I > Q	51.4ns/916ns	52.5	"	"	
	I + Q > 0	48ns/916ns	50	"	"	
	Q > 0	46ns/916ns	48.5	48ns/916ns	50	

End TEST: 11:15 (HHMP HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter NSN): 1029 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 11:15 (HHMP HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *comment for cable losses
50 min	684	10.17	684	11.67	# Rcv is low -1n >41.1hm
35 min	729	10.67	684	11.27	
18 min	825	11.37	825	12.57	
00 min	921	8.85	921	9.55	

Additional Testing (OPTIONAL); RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 11:25 (HHMP HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 11:45 (HHMP HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSPE): 1029

Test Date: 3/10/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

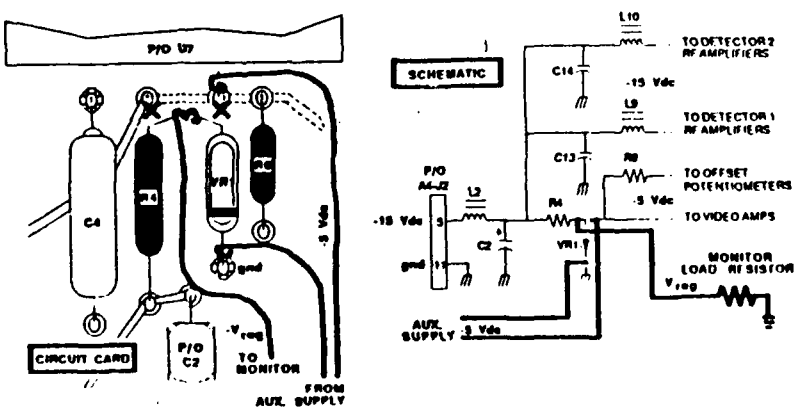
RESISTOR/ZENER DIODE MODIFICATION: At Dock: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

Start TEST: 11:25 (Time: HR:MIN)

Voltage across LOAD RESISTOR: -5.14 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 11:26 (Time: HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/10/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

54M Slot #1 10.29

Step level 2

J5 output

****

Power at J5 is 3.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 5.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.3 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/10/92
Sig. Det. #1029
Stress level 2
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 6.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 690.0 MHz which is above the specified frequency.
Power at J12 is 2.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 693.0 MHz which is above the specified frequency.
Power at J12 is 4.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 696.0 MHz which is above the specified frequency.
Power at J12 is 7.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 717.0 MHz which is above the specified frequency.
Power at J12 is 4.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is .3 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 888.0 MHz which is above the specified frequency.
Power at J12 is 4.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 921.0 MHz which is above the specified frequency.

****

FULL PRINT-OUT OF Power Output and Frequency [redacted].

Power at J12 is 11.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.6 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.0 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is .3 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is .7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter HEX): 1029 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 3 Tester: (Name & stamp below)

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 11:45 (HHMM HR MIN) Start DWELL: 12:15 (HHMM HR MIN)

STEP-STRESS Level Chamber Air Temperature: 84.6 (°C) (Chamber thermocouple reading) Flange Temperature: 77.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 84.55 / 84 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp, Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 5.6 (Vdc) -5 Volts dc: -5.6 (Vdc)

+15 Volts dc: +15.9 (Vdc) -15 Volts dc: -15.9 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 12:25 (HHMM HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 134.7 (mA) -5 Volts dc: 96 (mA)

+15 Volts dc: 112 (mA) -15 Volts dc: 53.3 (mA)

End TEST: 12:26 (HHMM HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter HEX): 1029 Test Date: 3/11/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 or 100 at this STEP-STRESS Level.

Start TEST: 12:26 (HHMM HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	469/956	49.1	468/956	48.8	
	I > Q	"	"	"	"	
	I + Q > 0	480/960	50	480/960	50	
	Q > 0	"	"	468/960	48.5	
Other Specify -71 (dBm)	I > 0	492/960	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	492/960	51.2	492/960	51.2	
	I > Q	504/960	52.5	"	"	
	I + Q > 0	480/960	50	"	"	
	Q > 0	"	"	480/960	50	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (msec)	Detector 1 Duty Cycle (percent)	Detector 2 t (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.6ms/9.6ms	48%	4.6ms/9.6ms	48.5	
	I > Q	"	"	"	"	
	I + Q > 0	4.6ms/9.6ms	50	4.6ms/9.6ms	50	
	Q > 0	"	"	4.6ms/9.6ms	48.5	
Other: Specify -11 (dBm)	I > 0	4.6ms/9.6ms	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0			1		
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Missed		4.92ms/9.6ms	51.2	
	I > Q	4.6ms/9.6ms	52.5	"	"	
	I + Q > 0	4.6ms/9.6ms	50	4.6ms/9.6ms	50	
	Q > 0	4.6ms/9.6ms	48.8	"	"	

End TEST: 12:50 (HH:MM AM/PM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 12:50 (HH:MM AM/PM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *account for cable losses
50 (HEX)	684	9.97	684	11.57	
35 (HEX)	729	9.67	729	11.42	
18 (HEX)	825	10.07	825	10.67	
00 (HEX)	921	8.05	921	9.45	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level, Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: _____ (HH:MM AM/PM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at the STEP-STRESS Level

End DWELL: 17:15 (HH:MM AM/PM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter SERN): 1029

Test Date: 3/10/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

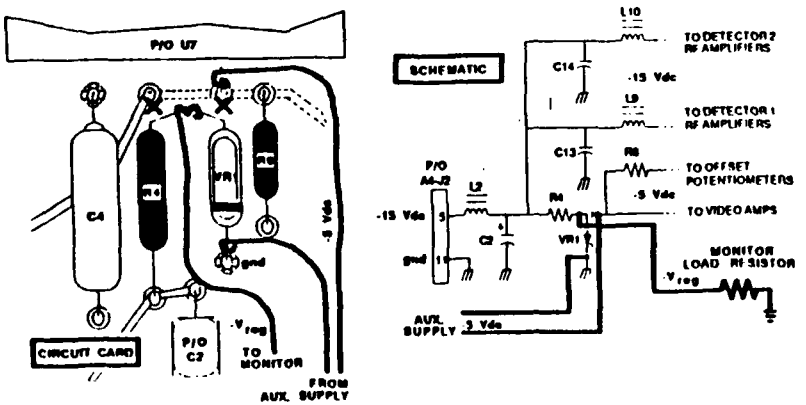
Start TEST: 13 05 (HHMM MN MMM)

Voltage across LOAD RESISTOR: -5.19 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 13 06 (HHMM MN MMM)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/10/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders. 549 Ref. # 1029

stress level 3

J5 output

****

Power at J5 is 2.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is-1.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is .8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.5 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.8 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 5.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is .4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-10.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 9.1 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is .8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.5 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.7 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.8 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.1 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.9 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is .4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is-10.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3/10/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Sn. Unit # 1025

Stress level 3

J12 output

****

Power at J12 is 4.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 687.0 MHz which is above the specified frequency.
Power at J12 is .3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Frequency is less than 690.0 MHz which is below the specified frequency.
Power at J12 is 4.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 702.0 MHz which is above the specified frequency.
Power at J12 is-2.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 705.0 MHz which is above the specified frequency.
Power at J12 is 6.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is less than 711.0 MHz which is below the specified frequency.
Power at J12 is 2.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 823.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 906.0 MHz which is above the specified frequency.
Power at J12 is 5.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Frequency is less than 912.0 MHz which is below the specified frequency.
Power at J12 is 4.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 915.0 MHz which is above the specified frequency.
Power at J12 is 5.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 11.2 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is .3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.5 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.6 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.6 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

3601

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter NSN): 1029

Test Date: 3/16/92

Tester: (Name & comp badge)

STEP-STRESS Level (enter 0 - 10): 4

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 13:15 (military time)

Start DWELL: 13 45 (military time)

STEP-STRESS Level Chamber Air Temperature: 92.8 / 90.6 (°C) (Chamber thermocouple reading)

Flange Temperature: 100.7 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 101 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +5.8 (Vdc) -5 Volts dc: -5.E (Vdc)

+15 Volts dc: +16.2 (Vdc) -15 Volts dc: -16.2 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level

Start TEST: 13 56 (military time)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 426 (mA) -5 Volts dc: 97 (mA)

+15 Volts dc: 115 (mA) -15 Volts dc: 596 (mA)

End TEST: 13 57 (military time)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter NSN): 1029

Test Date: 3/16/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 as the STEP-STRESS Level.

Start TEST: 13 57 (military time)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input (dBm)	I & Q Bits	Detector 1 t (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	448ns/96ns	48	472ns/96ns	50	
	I > Q	"	"	"	"	
	I + Q > 0	472ns/96ns	50	"	"	
	Q > 0	"	"	96ns/96ns	48	
Other Specify -71 (dBm)	I > 0	496ns/96ns	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	noisy		496ns/96ns	51.2	
	I > Q	472ns/96ns	51.2	"	"	
	I + Q > 0	448ns/96ns	50	"	"	
	Q > 0	"	"	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 484 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.62u/4.6u	48.8	4.6u/4.6u	48.5	
	I > Q	4	1/	11	11	
	I + Q > 0	4.62u/4.6u	50	4.6u/4.6u	90	
	Q > 0	11	11	4.6u/4.6u	48.1	
Other Specify -11 (dBm)	I > 0	4.62u/4.6u	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	noisy		4.62u/4.6u	48.8	
	I > Q	5.08u/4.6u	52.5	11	11	
	I + Q > 0	4.62u/4.6u	50	11	11	
	Q > 0	4.62u/4.6u	48.4	4.62u/4.6u	50	

End TEST 1407 (enter HHMM)

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 1407 (enter HHMM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measure for cable losses
50 min	684	9.77	684	11.61	
35 min	729	9.97	729	11.47	
18 min	825	9.47	825	9.91	
00 min	921	7.55	921	9.15	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 1425 (enter HHMM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL 1445 (enter HHMM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1029 Test Date: 3/10/92

Tester: (Please print clearly below)

STEP-STRESS Level (range 0 - 4): 4

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

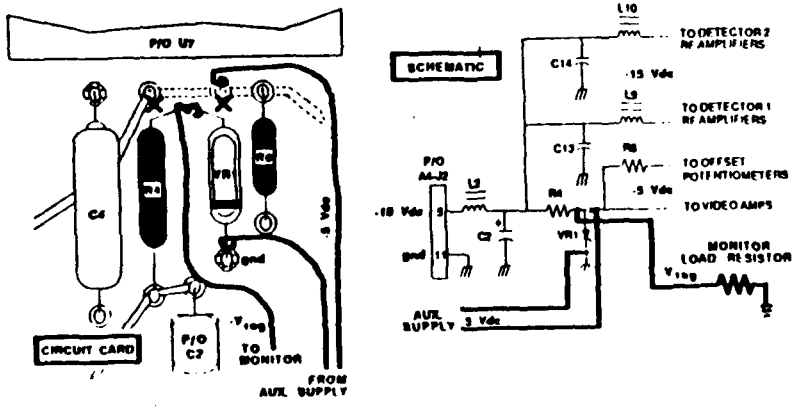
RESISTOR/ZENER DIODE MODIFICATION: As Built: For the modified resistor/zener diode subcircuit record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 10:45 (military time)

Voltage across LOAD RESISTOR: -5.2 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 10:46 (military time)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/10/92
Sn/Ant #1029
Stress level 2
JS output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 9.0 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is .9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is .2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is .6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.2 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.1 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.4 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 6.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 3.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 1.9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 2.4 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 4.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.0 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is .6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is .6 dBm @ 921.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.

****

FULL PRINT-OUT OF Power Output and Frequency [redacted]

3/10/92
SN01 Ref #1029
steer level 4
J12 output

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is .1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 702.0 MHz which is above the specified frequency.
Power at J12 is 6.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 711.0 MHz which is above the specified frequency.
Power at J12 is 1.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 714.0 MHz which is above the specified frequency.
Power at J12 is 4.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 885.0 MHz which is above the specified frequency.
Power at J12 is-2.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 903.0 MHz which is above the specified frequency.
Power at J12 is 2.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 918.0 MHz which is above the specified frequency.
Power at J12 is 2.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted]ar. *

Power at J12 is 11.0 dBm @ 634.0 MHz (Spec=+9dBm minimum).
Power at J12 is .1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is .5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.5 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.4 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.5 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.1 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 4 digits): 1029 Test Date: 3/10/92

Tester: (Name & comp below)

STEP-STRESS Level (enter 0 - 10): 5

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 14:45 (TIME HR MIN) Start DWELL: 15:15 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +100.5 Ref (°C) (Chamber thermocouple reading) Flange Temperature: +110.2 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 116 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.00 (Vdc) -5 Volts dc: -6.00 (Vdc) Verified

+15 Volts dc: +16.50 (Vdc) -15 Volts dc: -16.50 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc) -5.1096

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 15:20 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 143.9 (mA) -5 Volts dc: 97.5 (mA)

+15 Volts dc: 117.9 (mA) -15 Volts dc: 560.5 (mA)

End TEST: 15:23 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 4 digits): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 30 at this STEP-STRESS Level.

Start TEST: 15:25 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50.0	480/960	50.0	
	I > Q	4.68 /	48.8	4.68 /	48.8	
	I + Q > 0	4.80 /	50.0	4.80 /	50.0	
	Q > 0	4.80 /	50.0	4.56 /	47.5	
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	480/960	50.0	492/960	51.2	
	I > Q	4.92 /	51.2	4.92 /	51.2	
	I + Q > 0	4.80 /	50.0	4.92 /	51.2	
	Q > 0	4.80 /	50.0	4.80 /	50.0	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 464 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.68/9.60	48.8	4.80/9.60	50.0	
	I > Q	4.80/	50.0	4.68/	48.8	
	I + Q > 0	4.80/	50.0	4.80/	50.0	
	Q > 0	4.80/	50.0	4.92/	47.5	
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.80/9.60	50.0	4.92/9.60	51.2	
	I > Q	4.68/	48.8	4.80/	50.0	
	I + Q > 0	4.80/	50.0	4.92/	50.0	
	Q > 0	4.80/	50.0	4.92/	51.2	

End TEST: 15:37 (HHMM 24 HR)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 15:37 (HHMM 24 HR)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations
50 min	639.3 UNLK	-2.0	684.0	+11.6	
35 min	685.4 UNLK	+7.2	729.0	+11.9	
18 min	772.7 UNLK	+7.6	826.0	+10.2	
00 min	858.3 UNLK	+4.9	921.0	+7.45	

*measure for cable losses

UNLOCKED

Observations: cleaning and gain; Synth 1 (J5) on pulsed low in frequency and locked at mid & 1/2 of frequencies (0, 6, 7, 1, 45)

50% UNLOCKED KNOWN ANOMALY

MAJORITY OF FREQ LOCKED TOP UNLOCKED ON SUBSEQUENT RUNS

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here) (J12 only)

End TEST: 16:13 (HHMM 24 HR)

KNOWN ANOMALIES NO FAILURE

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

End DWELL: 16:15 (HHMM 24 HR)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 1029 Test Date: 03/10/92

Tester: (Name & comp be info)

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

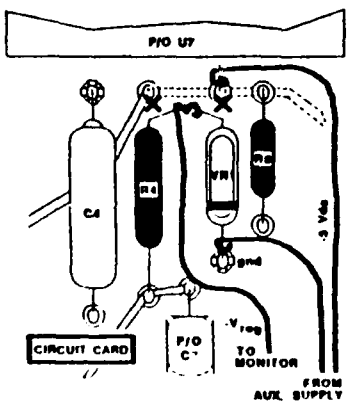
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

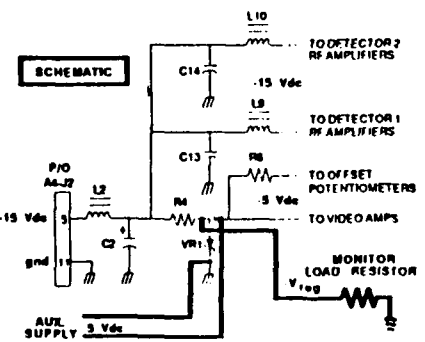
Start TEST: 15:23 (Time: Hr. Min)

Voltage across LOAD RESISTOR: -5.2198 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 15:24 (Time: Hr. Min)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND P4/VR1 MONITORING





03/10/92.

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 1029 (01466 1151)

STEP-STRESS TEST
LEVEL 5
DATA J12 ONLY

Power at J12 is 11.0 dBm @ 694.0 MHz (Spec=+9dBm minimum).
Power at J12 is-23.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.2 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is-59.7 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.6 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-46.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-37.6 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.4 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is-50.9 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.1 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is-37.7 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-64.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.5 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is-63.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-27.8 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is-61.2 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is-41.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is-60.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.8 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is-7.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

UUT Serial Number (enter 4 digits): 1029 Test Date: 03/10/92

Tester: (Please PRINT name below)

STEP-STRESS Level (enter 0 - 10): 6

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 16:15 (TIME HR MIN) Start DWELL: 16:45 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +109.2 (°C) Flange Temperature: +118.1 (°C)

(Chamber thermocouple reading) (Thermocouple reading)

STEP-STRESS Level Computed Temperature: +118 (°C)

(refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp, Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.20 (Vdc) -5 Volts dc: -6.20 (Vdc)

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1097 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 16:47 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1490.3 (mA) -5 Volts dc: 102.3 (mA)

+15 Volts dc: 131.0 (mA) -15 Volts dc: 5780 (mA)

End TEST 16:49 (TIME HR MIN)

TEST continued next page

3.70

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number (enter 4 digits): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Level from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 30 at this STEP-STRESS Level.

Start TEST: 16:51 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	430/860	50.0	430/860	50.0	
	I > Q	465/	48.8	463/	48.8	
	I + Q > 0	448/	48.8	430/	50.0	1.20 μsec
	Q > 0	430/	50.0	413/	47.5	
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	504/860	52.5	504/860	52.5	
	I > Q	480/	50.0	492/	51.2	
	I + Q > 0	465/	48.8	492/	51.2	1.20 μsec
	Q > 0	430/	50.0	413/	48.8	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 484 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.50/3.60	50.0	4.64/3.96	48.8	
	I > 0	4.68/	48.8	4.56/	47.5	
	I + Q > 0	4.80/	50.0	4.92/	51.2	
	Q > 0	4.92/	51.2	4.68/	48.8	
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.80/3.60	50.0	4.92/3.96	51.2	
	I > 0	4.80/ 4.68	50.0 48.8	4.92/	51.2	
	I + Q > 0			4.92/	51.2	
	Q > 0	4.80/	50.0	4.92/	51.2	

End TEST: 16:58 (HHMM HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 16:59 (HHMM HR MIN)

Channel	Freq Δ	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Freq Δ	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *account for cable losses
50 mm	476	6364	-1.43	484	6380	-2.93	Both Synths pulled off frequency. Both Synths are locked. Solidly on freq when queried. See data book
35 mm	352	6938	+10.5	341	6949	+12.1	
18 mm	58	767.0	+11.6	56	771.4	+12.7	
00 mm	68.2	852.8	+9.4	68	857.8	+11.1	

KNOWN ANOMALIES

paused at wrong frequency see sheet 4 of 4 @ 20:37

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO OFF FREQ

Use Test #2 Frequency Sweep to Exercise & Monitor (Check here)

End TEST: 17:21 (HHMM HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 17:45 (HHMM HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 1029

Test Date: 03/10/92

Tester:

STEP-STRESS Level: 6

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell, For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

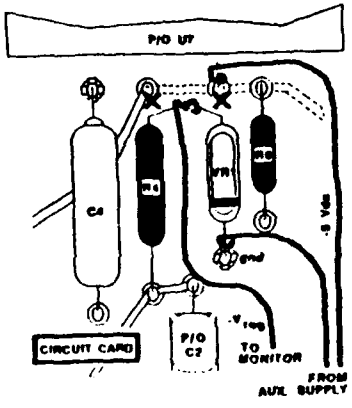
Start TEST: 16:49 (TIME HR MIN)

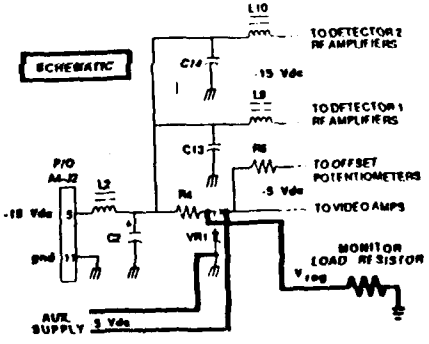
Voltage across LOAD RESISTOR: -5.2348 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 16:49 (TIME HR MIN)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 7

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 17:45 (TIME HR:MIN) Start DWELL: 18:15 (TIME HR:MIN)

STEP-STRESS Level Chamber Air Temperature: +117.3 / +116.7 / Soak @ +119 (°C) (Chamber thermocouple reading)

Flange Temperature: +127.6 / +127.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +126 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.40 (Vdc) -5 Volts dc: Slow -6.40 (Vdc)

+15 Volts dc: +17.10 (Vdc) -15 Volts dc: -17.10 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1098 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 18:19 (TIME HR:MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1520.9 (mA) -5 Volts dc: 98.3 (mA)

+15 Volts dc: 117.8 (mA) -15 Volts dc: 592.7 (mA)

End TEST: 18:21 (TIME HR:MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA — CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 18:21 (TIME HR:MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	492/960	47.5	484/961	50.0	8 div
	I > Q	490/	50.0	464/	48.8	1.20 usec/div
	I + Q > 0	492/	50.0	492/	51.2	
	Q > 0	492/	51.2	451/	47.5	
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify -57 (dBm)	I > 0	Very Noisy @ -60 dBm use -57 dBm		512/960	53.3	ANOMALY SEEN DETECTOR #2
	I > Q			512/960	53.3	10 dB Limit Line
	I + Q > 0			512/960	53.3	
	Q > 0			496/960	51.7	
-75 dBm	I > 0	512/960 NOISY	53.3	None/960		Due to noise 6 div
	I > Q	480/	50.0	None/	NO OUTPUT CYCLE HERE	1.60 usec/div
	I + Q > 0	496/	51.7	None/		
	Q > 0	496/	51.7	None/		

TEST Continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 484 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L(max) T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 L(max) T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	468/840	48.8	492/660	51.2	8 div
	I > Q	480/	50.0	468/	48.8	1.20 usec/div
	I + Q > 0	480/	50.0	492/	51.2	
	Q > 0	492/	51.2	444/	48.8	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify -60 (dBm)	I > 0	Use -60dBm		51.2/540	53.3	
	I > Q			5.28/	55.0	ANOMALY STILL HERE
	I + Q > 0			5.28/	55.0	Δ = 15dB Suspected Limit
	Q > 0			456/	51.7	
-75 dBm	I > 0	456/840	51.7	None/660		
	I > Q	480/	50.0	None/	NO DUTY CYCLE HERE	6 div 1.6 usec/div
	I + Q > 0	480/	50.0	None/		
	Q > 0	432/	49.2	None/		

End TEST: 18:40 (HHMM MS MM)

NEED TO VERIFY IS dB LOSS WITH DETECTOR # 2

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 18:40 (HHMM MS MM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *Increase for cable losses
50 min	1018	-12.9	1005	-12.1	Both synths lock fundamental > -5 dBm only third log output with harmonic above 1000 MHz
35 min	1015 Same		1005 Same		
18 min	1015 Same		1005 Same		
00 min	1018 Same		1005 Same		

ANOMALY BOTH SYNTH'S. NEED TO VERIFY AT PRIOR LEVEL SINCE MARGINS IS ONLY 3 dB

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: (HHMM MS MM)

ANOMALY NEED TO BE VERIFIED BOTH SYNTH'S

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

RETURN TO LEVEL 6 FOR ANOMALY VERIFICATION

End DWELL 19:15 (HHMM MS MM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1029

Test Date: 03/10/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

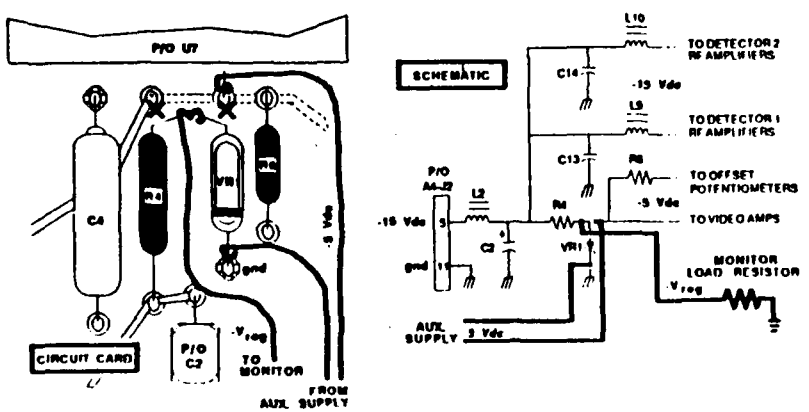
RESISTOR/ZENER DIODE MODIFICATION: At Dock: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 18:21 (Hour Hr Min)

Voltage across LOAD RESISTOR: -5.2519 (Vdc) (refer to Appendix D, nominally -5 Vdc)

End TEST: 18:21 (Hour Hr Min)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION FOR AUX. CONSTANT -5 Vdc SUPPLY AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

Tester: (Please fill in name below)

STEP-STRESS Level (enter 0 - 10): 6 (RETEST)

√ = compares with previous Level 6 test data

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 19:15 (TTMP HR MIN) Start DWELL: 19:45 (TTMP HR MIN)

STEP-STRESS Level Chamber Air Temperature: +10 (°C) Flange Temperature: +12 (°C)

(Chamber thermocouple reading)

STEP-STRESS Level Component Temperature: +11 (°C)

(refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: +6.20 (Vdc) -5 Volts dc: -6.20 (Vdc)

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1097 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 19:51 (TTMP HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1529.5 (mA) Δ = +39.2 mA -5 Volts dc: 1028 (mA) Δ = +0.5 mA

+15 Volts dc: 131.5 (mA) Δ = +0.5 mA -15 Volts dc: 576.9 (mA) Δ = -1.1 mA

End TEST: 19:54 (TTMP HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 1 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 6 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input Power from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or 100 STEP-STRESS Level.

Start TEST: 19:56 (TTMP HR MIN) DETECTOR #2 ANOMALY VERIFICATION BEING CHECKED HERE

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

FOR REF ONLY

Rcv Sig Input	I & Q Bits	Detector 1 L (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.64/9.60	48.8	4.80/9.60	50.0	
	I > 0	4.64/	48.8	4.64/	48.8	5 div
	I + Q > 0	4.80/	50.0	4.80/	50.0	1.20 usec/div
	Q > 0	4.80/	50.0	4.64/	48.8	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify -60 (dBm)	I > 0			4.96/9.60	51.7	VERIFIED 15 dB GAIN SENSITIVITY LOSS
	I > 0	NOT SAME AS PRIOR LEVEL 6		5.12/9.60	53.3	
	I + Q > 0			5.12/9.60	53.3	
	Q > 0			4.60/9.60	47.9	
-75 dBm	I > 0	4.32/9.60	50.0	NONE/9.60		6 div
	I > 0	4.80/	50.0	NONE/		1.20 usec/div
	I + Q > 0	4.80/	50.0	NONE/		
	Q > 0	4.80/	50.0	NONE/		

TEST Continued next page

FAILURE VERIFIED

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number: 1029 Test Date: 03/10/92

STEP-STRESS Level: 6 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

FOR REF ONLY

Rev Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/9.60	50.0 ✓	4.80/9.60	50.0 ✓	(CHECK ANOMALY)
	I > Q	4.80/	50.0 ✓	4.68/	48.8	8 div
	I + Q > 0	4.94	51.2	4.80/	50.0	1.20 μsec/div
	Q > 0	4.92/	51.2 ✓	4.64/	48.8 ✓	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify -60 (dBm)	I > 0			4.96/9.60	51.2	
	I > Q			4.96/9.60	53.3	LOSS OF 15dB GAIN SENSITIVITY VERIFIED
	I + Q > 0			4.96/9.60	51.7	NOT SAME AS PRIOR LEVEL 6
	Q > 0			4.64/9.60	48.3	
-75 dBm	I > 0	4.96/9.60	51.7 (>50.0)	None/9.60	51.2	LOSS OF LEVEL
	I > Q	4.80/	50.0 ✓	None/	51.2	6 div
	I + Q > 0	4.80/	50.0	None/	51.2	1 μsec/div
	Q > 0	4.80/	50.0 ✓	None/	51.2	

End TEST: 20:17 (HHMM MS MM) Continue w/ SYNTH CHECKS

FAILURE VERIFIED

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number: 1029 Test Date: 03/10/92

STEP-STRESS Level: 6 (RETEST)

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 20:19 (HHMM MS MM)

✓ = compares well to prior Level 6 data

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*minimum for cable losses)
50 min	636.0 ✓	-1.8 ✓	635.6 ✓	-3.0 ✓	Both synths. are low in frequency but are locked and stable w/ good power.
35 min	651.4 CORRECT	+9.7 ✓	652.0 CORRECT	+11.8	
18 min	766.4 ✓	+11.6 ✓	770.9 ✓	+12.7 ✓	
00 min	851.8 ✓	+9.3 ✓	857.1 ✓	+11.1 ✓	## below passband

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO

Monitor after Steady Test #2 Frequency Sweep

End TEST: 20:36 (HHMM MS MM)

NO Synthesizer Failure Observed @ Retest

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

ANOMALY OF DETECTOR #2 GAIN HAS BEEN CONFIRMED AS FAILURE. RETURN TO LEVEL 0 FINAL

End DWELL: 20:45 (HHMM MS MM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 1029

Test Date: 03/10/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 6 (RETEST

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

Start TEST: 19:54 (TIME HR:MIN)

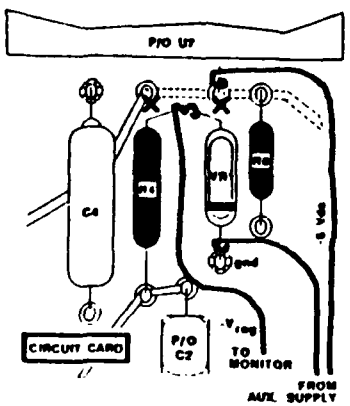
Voltage across LOAD RESISTOR: -5.2372 (Vdc) (refer to Appendix D, nominally 1 Vdc)

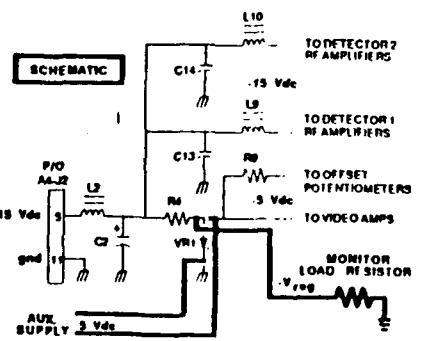
End TEST: 19:55 (TIME HR:MIN)

$\Delta = +0.0024$ V

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter NSN): 1029 Test Date: 03/10/92

Tester: (Name & agency below) D.D. Mueller

STEP-STRESS Level (enter 0 - 10): 0 FINAL

FAILURE OCCURRED AT LEVEL 7
& VERIFIED AT LEVEL 6 RETEST

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 20:45 (hr:min) (Ramp # 5, Total # 1 Ramp of 35 minutes) Stabilize using TC data +63 TC!

Start DWELL: 22:00 (hr:min) TC 3, unused TC 3 is bad overload

STEP-STRESS Level Chamber Air Temperature: +61.0 TC (°C) Stable @ +61°C (Chamber thermocouple reading)

Flange Temperature: +68.9 TC +70 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +70 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below) Decreased through ramp.

Supply Voltages: +5 Volts dc: +5.00 (Vdc) -5 Volts dc: -5.00 (Vdc)

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.00 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1096 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 22:02 (hr:min)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1281.8 (mA) Δ = +39 mA -5 Volts dc: 84.3 (mA) Δ = +1 mA

+15 Volts dc: 106.0 (mA) Δ = 0 mA -15 Volts dc: 496.8 (mA) Δ = -3 mA

End TEST 22:04 (hr:min)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter NSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 as this STEP-STRESS Level.

Start TEST: 22:05 (hr:min)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 3 T (usec)	Detector 3 Duty Cycle (percent)	Observations
0 dBm	I > 0	484/968	50.0 ✓	484/968	50.0 ✓	8 div 1.20 μsec/div
	I > Q	484/	50.0 ✓	468/	48.8 ✓	
	I + Q > 0	484/	50.0 ✓	468/	48.8 ✓	
	Q > 0	484/	50.0 ✓	456/	47.2	
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					DETECTOR #2 FAILS
	Q > 0					
Other Specify 5000 pulses - 75 dBm 00 -57 (dBm) IN 1dB STEPS	I > 0	18 dB Loss	-57dBm	512/968	53.3	6 div DET #2 1.60 μsec/div
	I > Q		-58dBm VERY NOISY	496/	51.7	
	I + Q > 0		-57dBm	484/	50.0	
	Q > 0		-57dBm	464/	48.3	
-75 dBm	I > 0	492/968	51.2 ✓		NONE	8 div DET #1
	I > Q	484/	50.0		NONE	
	I + Q > 0	484/	50.0 ✓		NONE	
	Q > 0	464/	48.8 ✓		NONE	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -.75 dBm

Rev Sig (enter)	I & Q (Bits)	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50.0	467/960	48.8 ✓	
	I > Q	467/	48.8 ✓	467/	48.8 ✓	8 div
	I + Q > 0	480/	50.0 ✓	492/	51.2 (50.0)	1.20 usec/div
	Q > 0	492/	51.2 (50.0)	467/	48.8 ✓	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify -75 dBm to -55 (dBm) in 1 dB steps	I > 0	20dB Loss < -55dBm		492/960	46.7	
	I > Q	-57dBm VERY NOISY		496/	51.7	6 div DET #2
	I + Q > 0	-57dBm 18dB Loss		480/	50.0	1.60 usec/div
	Q > 0	-58dBm		480/	50.0	
-75 dBm	I > 0	492/960	51.2 ✓ (50.2)	NONE		
	I > Q	480/	50.0 ✓	NONE		8 div DET #1
	I + Q > 0	480/	50.0 ✓ (49.8)	NONE		1.20 usec/div
	Q > 0	492/	51.2	NONE		

End TEST: 22:24 (TIME HR MIN) DETECTOR #2 FAILS

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 22:24 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations
50 min	6840	+9.0	6839	+10.3	*measure for cable losses
35 min	729.0	+10.9	728.9	+11.6	
18 min	825.0	+10.1	825.0	+10.8	
00 min	920.9	+10.8	921.0	+12.0	

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 22:45 (TIME HR MIN)

STEP STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

Report # 17388 TESTING COMPLETE DETECTOR #2 FAILURE RETURN TO ROOM TEMP End DWELL 23:00 (TIME HR MIN)

UUT POWER OFF 23:50

STEP-STRESS LEVEL COMPLETE

PLOT #2 ENDED 0:00 03/11/92

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 1029 Test Date: 03/10/92

Tester: (Please 4 stamp below)

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA PERFORMANCE MONITOR PMO

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level

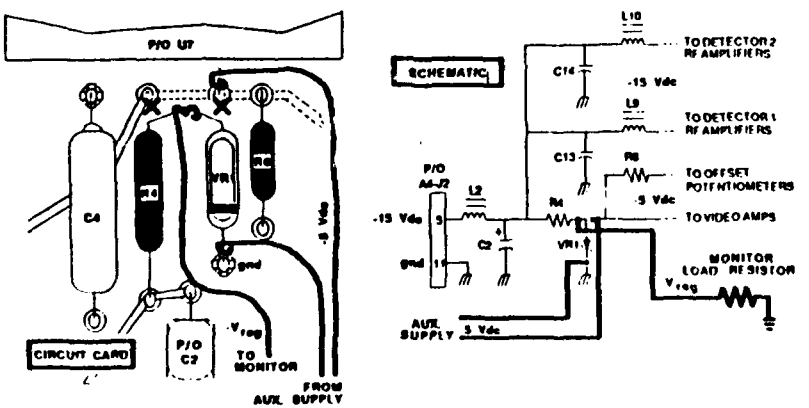
Start TEST: 22:04 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.1476 (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: 22:04 (TIME HR:MIN)

391

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 1029

Meas +9.0

LEVEL 2 FINAL

03/10/92 P22:29

Power at J5 is 6.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is .4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 729.0 MHz (Spec=+9dBm minimum). Meas +10.9
Power at J5 is 5.8 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.4 dBm @ 825.0 MHz (Spec=+9dBm minimum). Meas +10.1
Power at J5 is 3.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.9 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6-dBm @ 919.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.8 dBm @ 921.0 MHz (Spec=+9dBm minimum). Meas +10.8

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J5 is 6.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is .4 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.7 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.3 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 8.9 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.9 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.9 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.7 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.8 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.4 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is-4.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.9 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-1.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-2.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 918.0 MHz (Spec=+9dBm minimum).

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STEP-STRESS TEST

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 1029

Meas +10.3

Power at J12 is 6.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.4 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 729.0 MHz (Spec=+9dBm minimum). Meas +11.6
Power at J12 is 4.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is .3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.8 dBm @ 825.0 MHz (Spec=+9dBm minimum). Meas +10.3
Power at J12 is 6.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.2 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.1 dBm @ 921.0 MHz (Spec=+9dBm minimum). Meas +12.0

LEVEL Ø FINAL

03/10/92 @ 22:41

[redacted]

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

Power at J12 is 6.9 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 739.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is .3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.6 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.2 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 915.0 MHz which is above the specified frequency.
Power at J12 is 2.1 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 918.0 MHz which is above the specified frequency.

****

TEST EQUIPMENT & CALIBRATION LOG

Maintain Log for testing conducted 03/02/92 through ~~03/04/92~~ Same through 03/13/92

Item	DESCRIPTION	Manuf. & Part No.	ID NUMBER	LAST CAL*	CAL* DUE	Item Notes
01	T/R Test Station	HAC; SPECIAL	F-A15223		NCR	G-132043
02	Control Panel	HAC; SPECIAL	G-132290		NCR	
03	Signal Generator	HP; 8660C	G-128061	12-17-91	01-13-93	
04	Auxiliary Section	HP; 86631B	G-128062		NCR	7/6 ITEM 03
05	RF Section	HP; 86603A	G-128063	12-17-91	01-13-93	7/6 ITEM 03
06	Spectrum Analyzer	HP; 8568A w/ Opt E16	G-132082	12-11-91	10-30-92	
07	FET Probe	HP; 1120A	G-132055	12-14-90	04-30-92	FOR CAL
08	Power Meter	HP; 436A	G-128036	06-18-91	11-29-92	"
09	Power Sensor	HP; 8482A	G-128059	09-09-91	10-21-92	"
10	Oscilloscope	HP; 1980B	G-132049	09-29-91	08-11-92	
11	Digital Multimeter	SystronDonner; 7344A	G-137998	06-06-91	08-18-92	
12	Digital Multimeter	HP; 3478A	H-A53624	09-06-91	06-25-92	
13	Power Splitter	MiniCkts; ZFSC-2-5	NO ID ✓		NCR	
14	Power Splitter	MiniCkts; ZFSC-2-5	NO ID ✓		NCR	
15	Reg. Power Supply	Lambda; LP-531-FM	G-132292		NCR	+15V
16	Reg. Power Supply	Lambda; LP-531-FM	"		NCR	-15V
17	Reg. Power Supply	Lambda; LP-530-FM	G-132291		NCR	+5V
18	Reg. Power Supply	Lambda; LP-520-FM	"		NCR	-5V
19	Computer	HP; 9845B	G-128012		NCR	
20	Flex. Disk Memory	HP; 9895A	G-133309		NCR	
21	Signal Generator					
22	Oscilloscope	Tektronix; 2465				
23	Digital Multimeter					
24	Digital Multimeter					
25	Digital Multimeter					
26	Thermal Chamber	Thermotron; S-4 w/Cntl	H-B07567	09-18-91	09-02-92	
27	Data Acqtn Cntl Unit	HP; 3497A	H-428499	11-14-91	07-29-93	
28	Computer	HP; Model 85	H-A864Z9		NCR	
29	Power Supply, AUX.	HP; 6219A	H-357054		NCR	-5.1V
30	PLOTTER	HP; 7470A	H-512478		NCR	
31	PRINTER	HP; THINKJET	E-A08763		NCR	
32						
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						

*NCR = No Calibration Required

CALIBRATION ROUTINE PERFORMED: 03-02-92; 15:52 PRIOR TO TESTING

38.4

use with MSN 1029

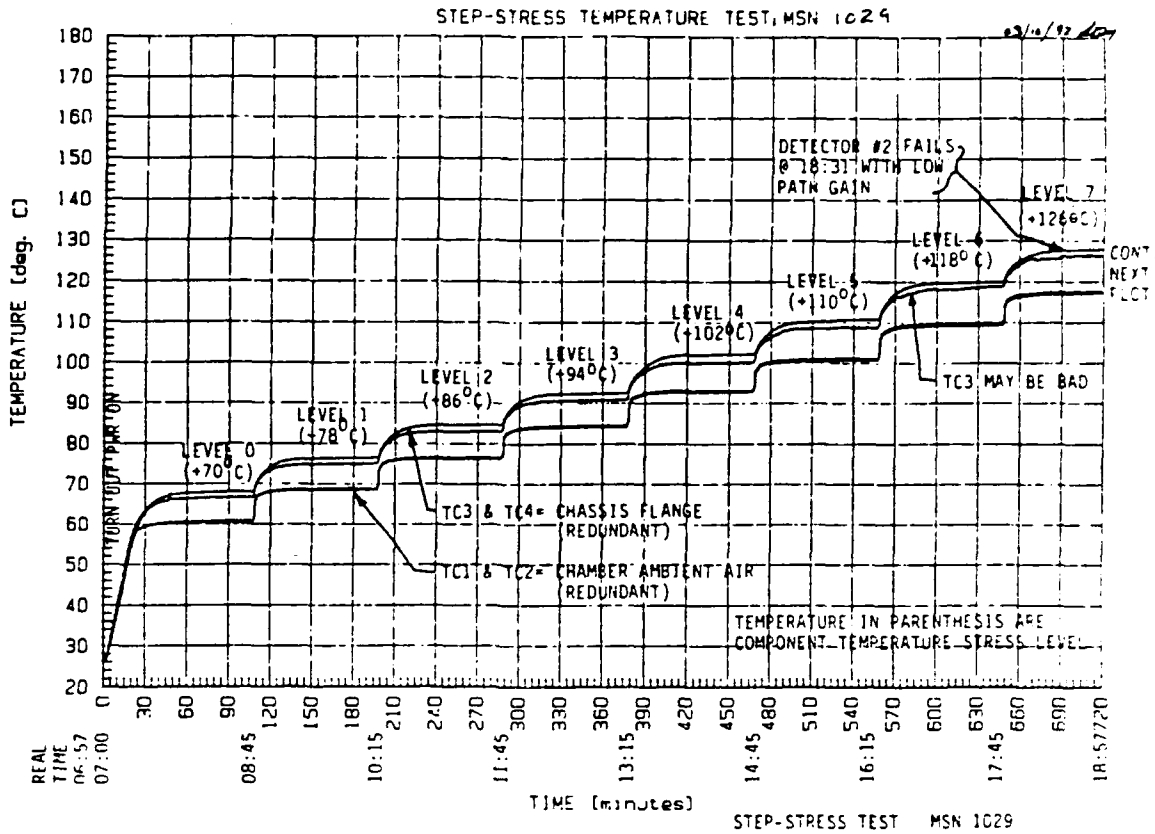
DATE: [redacted] TIME: [redacted]

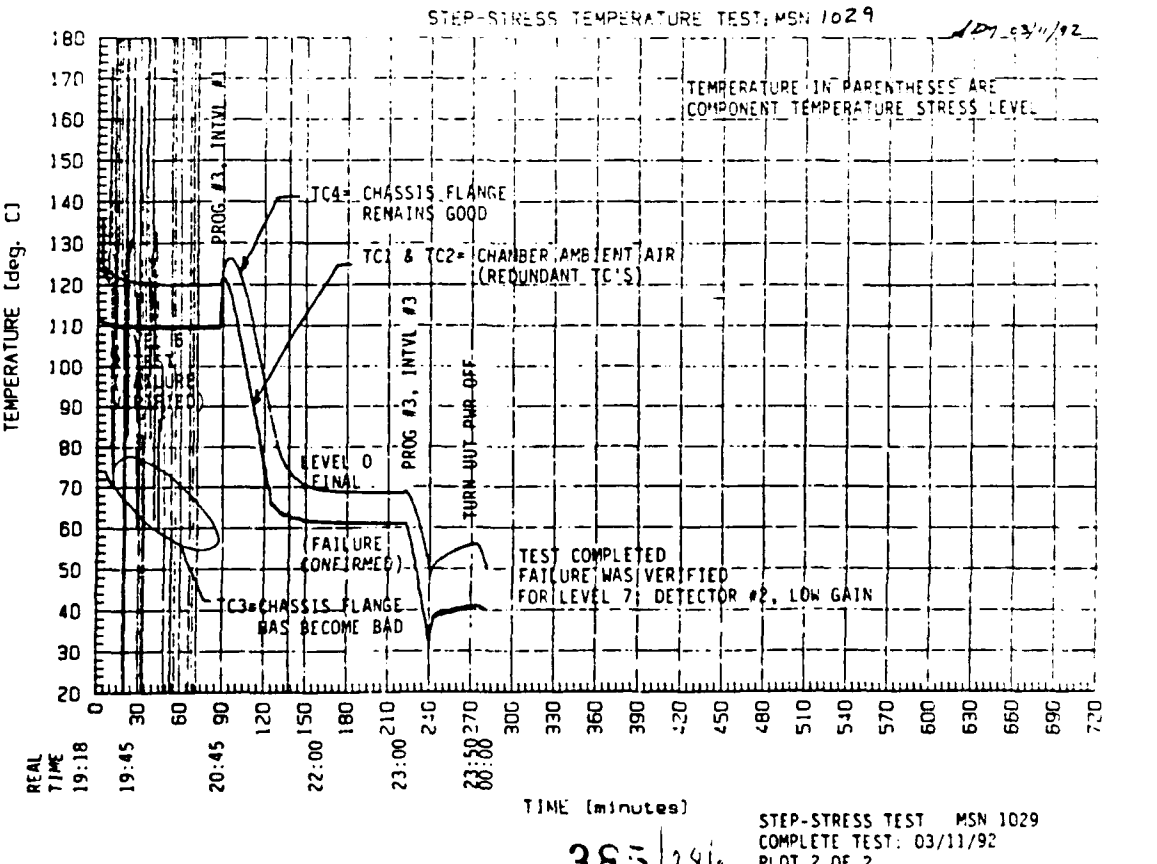
03/09/92

STEP-STRESS CALIBRATION DATA

```
Synth_ref= 2562698
Freq_mod_ref= 11603780
Sp_clock_output = 0
Phase_lo_output = 1.16
Phase_if_output = 0
Up_dn_conv_lo = 3.44
313.75_lo = -72.8 dBm /314.91116E6MHz
```

Channel	Freq	Dn_conv_output	Synth_lo_output	Hit_sgnl_l_o
50	684	1.17	1.17	2.18
49	687	1.2	1.31	2.07
48	690	1.28	1.4	2.07
47	693	1.33	1.3	2.07
46	696	1.33	1.18	2.03
45	699	1.34	1.23	1.95
44	702	1.38	1.37	1.96
43	705	1.38	1.41	2.01
42	708	1.39	1.35	1.98
41	711	1.42	1.42	1.85
40	714	1.45	1.53	1.82
39	717	1.46	1.53	1.9
38	720	1.42	1.44	1.96
37	723	1.4	1.49	1.92
36	726	1.43	1.71	1.83
35	729	1.44	1.87	1.82
34	732	1.45	1.84	1.86
33	735	1.42	1.69	1.83
32	738	1.42	1.69	1.74
31	741	1.39	1.82	1.79
30	744	1.39	1.83	1.94
29	747	1.41	1.83	1.98
28	750	1.46	1.94	1.81
27	753	1.49	2.1	1.72
26	756	1.49	2.11	1.8
25	759	1.45	1.93	1.86
24	762	1.45	1.86	1.81
23	765	1.48	2.01	1.78
22	768	1.52	2.13	1.85
21	771	1.6	2.12	1.94
20	774	1.68	2.07	1.86
19	777	1.72	2.14	1.74
18	825	1.76	2.27	1.8
17	828	1.74	2.31	1.73
16	831	1.7	2.39	1.68
15	834	1.7	2.33	1.74
14	837	1.76	2.27	1.74
13	882	1.7	2.07	1.55
12	885	1.66	2.02	1.61
11	888	1.7	2.01	1.67
10	891	1.76	2.02	1.6
9	894	1.7	2.07	1.54
8	897	1.68	2.09	1.53
7	900	1.72	2.02	1.54
6	903	1.74	1.91	1.46
5	906	1.64	1.87	1.42
4	909	1.52	1.89	1.48
3	912	1.53	1.86	1.58
2	915	1.61	1.86	1.59
1	918	1.6	1.86	1.51
0	921	1.52	1.85	1.47


STEP-STRESS TEMPERATURE TEST; MSN 1029
TEMPERATURE [deg. C]
TIME [minutes]
REAL TIME
TURN OUT PWR ON
LEVEL 0 (+70°C)
LEVEL 1 (+78°C)
LEVEL 2 (+86°C)
LEVEL 3 (+94°C)
LEVEL 4 (+102°C)
LEVEL 5 (+110°C)
LEVEL 6 (+118°C)
LEVEL 7 (+126°C)
DETECTOR #2 FAILS @ 18:31 WITH LOW PATH GAIN
CONT. NEXT PLOT
TC3 MAY BE BAD
TC3 & TC4= CHASSIS FLANGE (REDUNDANT)
TC1 & TC2= CHAMBER AMBIENT AIR (REDUNDANT)
TEMPERATURE IN PARENTHESIS ARE COMPONENT TEMPERATURE STRESS LEVEL
STEP-STRESS TEST MSN 1029
BEGIN TEST: 03/10/92
PLOT 1 OF 2


STEP-STRESS TEMPERATURE TEST; MSN 1029
TEMPERATURE [deg. C]
TIME [minutes]
REAL TIME
TEMPERATURE IN PARENTHESES ARE COMPONENT TEMPERATURE STRESS LEVEL
PROG #3, INTVL #1
PROG #3, INTVL #3
TURN OUT PWR OFF
TC4= CHASSIS FLANGE REMAINS GOOD
TC1 & TC2= CHAMBER AMBIENT AIR (REDUNDANT TC'S)
LEVEL 0 FINAL
(FAILURE CONFIRMED)
TC3=CHASSIS FLANGE HAS BECOME BAD
TEST COMPLETED
FAILURE WAS VERIFIED
FOR LEVEL 7; DETECTOR #2, LOW GAIN
STEP-STRESS TEST MSN 1029
COMPLETE TEST: 03/11/92
PLOT 2 OF 2

Test Data Cont'd: step stress test MSN # 1029 Date: 3/10/92

07:00 Begin temperature Plot. Turned power on UUT & began transition to 61°C

07:45 Dwell @ 61°C start test level D

08:45 stress level D Complete. Start ramp to level 1

09:15 Dwell @ 69°C

10:15 Stress test level 1 Complete. Start ramp to level 2

10:45 Dwell @ 77°C

11:45 stress level 2 Complete. Start ramp to level 3

12:15 Dwell @ 85°C

13:15 stress level 3 Complete. Start ramp to level 4

13:45 Dwell @ 94°C (LEVEL 4) 03/10/92

14:45 stress level 4 Complete. Start ramp to level 5

15:15 Dwell @ LEVEL 5 (+102°C) S.D. Mueller 92466

16:15 LEVEL 5 Complete. Ramp to LEVEL 6

16:45 Start Dwell @ LEVEL 6 (+111°C)

17:45 LEVEL 6 Complete. Ramp to LEVEL 7 (+119)

18:31 Anomaly with Detector #2 is -57dBm in (S/B-75dBm)

18:40 Anomaly with both Synth's. Only a harmonic, fixed frequency present.

18:57 Plot #1 Complete. Begin Reloading plot

19:15 Ramp to LEVEL 6 (+111°C) from LEVEL 7 just Completed (+119°C). This to verify Anomalies. Plot #2 still being reloaded.

19:18 Plot #2 begins (3 minutes into ramp to Level 6 Retest).

19:45 Begin LEVEL 6 RETEST

20:17 DETECTOR #2 FAILURE CONFIRMED DET #1 and Both Synth's appear OKAY. Return to FINAL TEST Level at end of Dwell.

Data Recorder: [illegible] 3/10/92

20

Test Data Cont'd: STEP-STRESS TEST MSN 1029 Date: 03/10/92

20:45 LEVEL 6 RETEST Dwell Complete. Ramp to LEVEL Ø for FINAL using program #3 Interval #1 (36 minutes)

NOTE: See data printouts TC3 has gone bad since beginning of new plot 2. Overload condition w/ TC3 noted as early as 20:16

22:00 UUT stabilized. Start Dwell LEVEL Ø FINAL (+61°C)

22:24 DETECTOR #2 STILL FAILS @ LEVEL Ø FINAL

23:00 END LEVEL Ø FINAL DWELL OF 1-HOUR
Ramp to ROOM TEMP (Prog #3, Intvl #3)

23:50 UUT powered OFF.

00:00 PLOT ENDED. TEST COMPLETE
03/11/92

Data Recorder: S.D. Mueller 92466

21

HUGHES
HUGHES AIRCRAFT COMPANY

STEP-STRESS
1 PROJECT NAME

TROUBLE & FAILURE REPORT

FAIL CLASS	TEST TYPE	TEST ENV	FAIL CAUSE	RELEV

NO. Z 7388

FAM CODE

SYST CODE

2 THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE ☐ FAILURE

ORIGINATOR

3 SYSTEM SUBSYSTEM NAME / P N / S N: R/T MODULE / Yuteno -103 / 1029

4 TIMER, COUNTER READINGS: TOTAL: 89.4 LEVEL 4 ELAPSED 11.3 LEVEL 7 HOURS CYCLES

5 DATE: 03 (MO) 10 (DAY) 92 (YR)

35 REFERENCES

6 REPORTING FACILITY: STEP-STRESS TEST c/o S.D. MUELLER

7 REPORTED BY: S.D. Mueller 03/10/92 ORG CODE: 1A 72 30

OPERATING LOG NO

8 TROUBLE FAILURE OBSERVED WAS (TEST CONDITIONS SYMPTOMS SEVERITY ETC INCLUDING "IS" AND "SHOULD BE" DATA):

DETECTOR #2 LOW IN GAIN BY 15dB TO 20dB. Should RECEIVE AT -75dBm Is ONLY OPERATING TO -58dBm TO -55dBm INPUT LEVEL. NO PROBLEM AT HIGH INPUT LEVEL OF 0dBm. UUT FAILED AT LEVEL 7 (+117°C CHAMBER AIR; +126°C FLANGE; +126°C Component AMB AIR TEMP; ± 6.4 Vdc; ± 17.1 Vdc). FAILURE VERIFIED AT LEVEL 6 & LEVEL 0 RETEST.

TFR CONTINUATION USED ☐

9 TROUBLE FAILURE OCCURRED DURING (A) X ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE-FLIGHT OR CURSORY CHECK

10 ACTION TAKEN TO CORRECT TROUBLE FAILURE (A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 20)

11 ITEM REPLACED NAME / P N / S N

12 ITEM INSTALLED NAME / P N / S N

13 DISPOSITION OF REPLACED ITEM

VERIFICATION

14 WERE OTHER TROUBLES FAILURES NOT RELATED TO ORIGINAL NOTED? (A) ☐ NO (B) ☐ YES LIST ON NEW TFR - TFR NO

15 WAS REPORTED TROUBLE FAILURE VERIFIED? (A) ☐ YES (B) ☐ NO (CHECK 16 B AND EXPLAIN)

16 FAILED ITEM NAME / P N / S N / REF DESIG / MANUFACTURER

17 NEXT HIGHER ASSY NAME / P N / S N / REF DESIG / MANUFACTURER

18 A ☐ REWORK REQUIRED IS B ☐ REWORK IS NOT REQUIRED BECAUSE

19 VENDOR REWORK ANALYSIS IS REQUIRED ☐ ITR / CAR

20 DISPOSITION OF ITEM IF NOT REWORKED

21 AUTHORIZATION BY / ORG CODE / DATE

REWORK & RETEST

22 LIST BELOW ALL PARTS REPLACED REPAIRED OR ADJUSTED

A CIRCUIT SYMBOL	B PART NUMBER	C S N	D MANUFACTURER	E DEFECT	F REWORK ACTION TAKEN	G REFERENCE DOC NO	H APPROVED PARTS (YES / NO)	PRI FAIL

23 OTHER REWORK ACTION

24 REWORKED BY / ORG CODE

25 RETESTED BY / ORG CODE

26 RETEST RESULTS APPROVAL / DATE

27 RETEST RESULTS REPAIRED ITEM IS ACCEPTABLE FOR ☐ UNRESTRICTED USE ☐ RESTRICTED USE ☐ NOT ACCEPTABLE EXPLAIN IN BLOCK 30

28 DISPOSITION OF ITEM AFTER RETEST

29 S C

ENGINEERING

30 CAUSE OF FAILURE - COMMENTS IF ANALYSIS NOT PERFORMED EXPLAIN

31 BASIC CAUSE OF TROUBLE FAILURE (SELECT FROM BLOCK 1 ON REVERSE SIDE)

32 SIGNATURE / ORG CODE / DATE

33 CORRECTIVE ENGINEERING ACTION TAKEN IF NONE JUSTIFY - CONCLUSIONS

REF DOCUMENT IMPLEMENTING CORRECTIVE ACTION ECO ECR ETC IS NO.

34 SIGNATURE / ORG CODE / DATE

11020 CS MAR 66

USE TFR CONTINUATION SHEET IF ADDITIONAL SPACE IS NEEDED

FOR RELIABILITY ANALYSIS AND FOLLOWUP SEE REVERSE SIDE OF COPY A

Z7388

STEP-STRESS TEST DATA NOTEBOOK

UNIT UNDER TEST: MSN 0993

TEST STATUS: FAILURE CONFIRMED

(5-MINUTES PRIOR TO LEVEL 10 DWELL)

TEST SUMMARY

STEP-STRESS		START DWELL	ANOMALY/ FAILURE	END DWELL
		12-Mar-92		
LEVEL	0	7:45		8:45
LEVEL	1	9:15	Anomaly	10:20
Retest	0	10:50		11:20
LEVEL	2	11:50	Anomaly	12:50
Retest	1	13:20	Anomaly	13:35
Retest	0	14:05		14:20
LEVEL	3	14:50		15:50
LEVEL	4	16:20		17:20
LEVEL	5	17:50		18:50
LEVEL	6	19:20		20:20
LEVEL	7	20:50		21:50
LEVEL	8	22:20		23:20
LEVEL	9	23:50		0:50
		12-Mar-92		13-Mar-92
FAILURE:			1:15	
LEVEL	10	1:20		2:20
Final Test	0	3:45		4:45
				13-Mar-92

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number: 993 Test Date: 3/12/92

Tester:

STEP-STRESS Level (enter 0 - 10): 0

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 07:00 (THUR HR MIN) Start DWELL: 07 45 (THUR HR MIN)

STEP-STRESS Level Chamber Air Temperature: 60.1 (°C) (Chamber thermocouple reading) Plenum Temperature: 67.1 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 70 (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 5 (Vdc) -5 Volts dc: -5 (Vdc)

+15 Volts dc: 15 (Vdc) -15 Volts dc: -15 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 07.45 (THUR HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1234 (mA) -5 Volts dc: 85 (mA)

+15 Volts dc: 111 (mA) -15 Volts dc: 497 (mA)

End TEST: 07 46 (THUR HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number: 993 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 07:46 (THUR HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	9.6us/9.6us	50	9.6us/9.6us	50	
	I > 0	4.8us/9.6us	49.8	4.8us/9.6us	49.8	
	I + Q > 0	4.8us/9.6us	50	4.92us/9.6us	51.2	
	Q > 0	"	"	4.8us/9.6us	50	
Other Specify -11 (dBm)	I > 0	4.92us/9.6us	51.2			
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	noisy		5.04us/9.6us	52.5	
	I > 0	4.80us/9.6us	49.8	4.8us/9.6us	49.8	
	I + Q > 0	5.28us/9.6us	55	5.16us/9.6us	53.75	
	Q > 0	5.16us/9.6us	53.75	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): C

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	48 / 96	50	46.8 / 96	48.8	
	I > Q	47 / 96	48.8	"	"	
	I + Q > 0	49.2 / 96	51.2	49.2 / 96	51.2	
	Q > 0	48 / 96	50	48 / 96	50	
Other: Specify -11 (dBm)	I > 0	50.4 / 96	52.5			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q				1	
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	noise		50.4 / 96	52.5	
	I > Q	48 / 96	50	48 / 96	50	
	I + Q > 0	52.8 / 96	55	51.6 / 96	53.75	
	Q > 0	50.4 / 96	52.5	"	"	

End TEST: 08 08 (HHMM MS MSM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): C

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST. At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 08 08 (HHMM MS MSM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *comment for cable losses
50 min	684	10.87	684	10.52	# Rcv is low still > -2dBm
35 min	729	10.77	729	10.47	
18 min	825	9.07	825	10.97	
00 min	921	#7.85	921	9.45	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check here)

End TEST: 08:20 (HHMM MS MSM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 08:45 (HHMM MS MSM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (from MBR): 993 Test Date: 3/12/92

STEP-STRESS Level (enter 0, -5, etc): 0 Tester: (Name & stamp below)

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

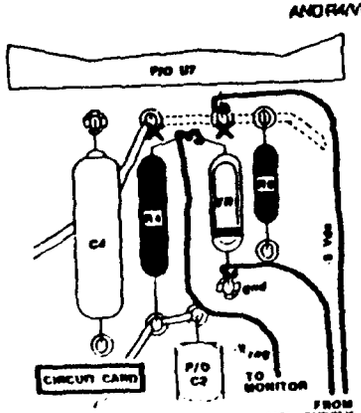
RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

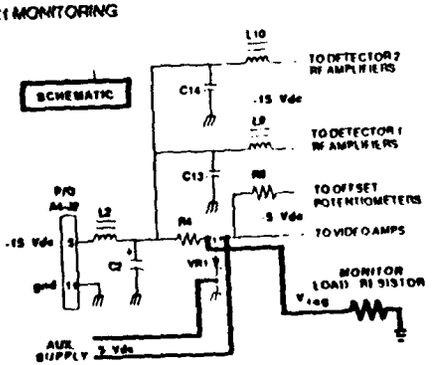
Start TEST: 08:21 (HOUR MINUTE)

Voltage across LOAD RESISTOR: -5.16 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 08:22 (HOUR MINUTE)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION FOR AUX. CONSTANT -5 Vdc SUPPLY AND R4/VR1 MONITORING





3/12/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

54A/Ref #993

stress level 0

J5 output

****

Power at J5 is 7.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 7.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is-3.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 3.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
Power at J5 is 1.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 6.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.1 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Frequency is greater than .0 MHz which is above the specified frequency.
Power at J5 is 4.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-10.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is-7.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).
Frequency is less than .0 MHz which is below the specified frequency.
****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J5 is 10.7 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.6 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.1 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is-.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is-3.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.0 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.1 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.5 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is-1.4 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 8.0 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.3 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 9.2 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.6 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.4 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.4 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 7.7 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is-5.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 5.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.3 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.1 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.8 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.4 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.1 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 3.0 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 6.2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 1.1 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.6 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 4.4 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is-10.3 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 2.9 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is-7.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

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STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter NSN): 913 Test Date: 3/12/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 1

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 08 45 (TIME HR MIN) Start DWELL: 09 15 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 68.3 (°C) (Chamber thermocouple reading) Plenge Temperature: 75.5 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 71 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 5.2 (Vdc) -5 Volts dc: -5.2 (Vdc)

+15 Volts dc: 15.3 (Vdc) -15 Volts dc: -15.3 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 09 32 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1303 (mA) -5 Volts dc: 515 (mA)

+15 Volts dc: 117 (mA) -15 Volts dc: 510 (mA)

End TEST: 09 33 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter NSN): 913 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 09 53 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz: Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	496/976	50	496/976	50	
	I > Q	476/976	48.8	476/976	48.8	
	I + Q > 0	492/976	51.2	492/976	51.2	
	Q > 0	"	"	"	"	
Other Specify -71 (dBm)	I > 0	492/976	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	noisy		516/976	52.5	
	I > Q	476/976	48.8	496/976	48.8	
	I + Q > 0	536/976	55	516/976	53.5	
	Q > 0	564/976	57.75	"	"	

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 993 Test Date: 3/12/92

STEP-STRESS Level: 1

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 484 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Level T (max)	Detector 1 Duty Cycle (percent)	Detector 2 Level T (max)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.9us/5.6us	50	4.65us/5.6us	48.8	
	I > Q	4.65us/5.6us	48.8	"	"	
	I = Q > 0	4.9us/5.6us	51.2	4.9us/5.6us	51.2	
	Q > 0	4.9us/5.6us	50	4.5us/5.6us	50	
Other Specify -71 (dBm)	I > 0	4.9us/5.6us	51.2			
	I > Q					
	I = Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q				1	
	I = Q > 0					
	Q > 0					
-75 dBm	I > 0	noisy		5.4us/5.6us	52.5	
	I > Q	4.65us/5.6us	48.8	4.65us/5.6us	48.8	
	I = Q > 0	5.4us/5.6us	51.75	5.4us/5.6us	51.75	
	Q > 0	5.4us/5.6us	52.5	"	"	

End TEST: 10:00 (Time per this unit)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 993 Test Date: 3/12/92

STEP-STRESS Level: 1

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 10:00 (Time per this unit)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *measured for cable losses
50 min	498	+10.98	698	10.97	(J5)
35 min	667	+10.87	729	10.97	
18 min	567	+10.87	805	9.97	(J5) CH 50 is ok.
00 min	808	+11.15	921	9.15	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT No (Check here)

End TEST: 10:19 (Time per this unit)

Went back to stress level 0 to check manually @ J12. 0.10 W

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL: 11:26 (Time per this unit)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter SSN): 997 Test Date: 2/12/97

STEP-STRESS Level (enter 0 - 10): 1 Tester: (Please print clearly)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

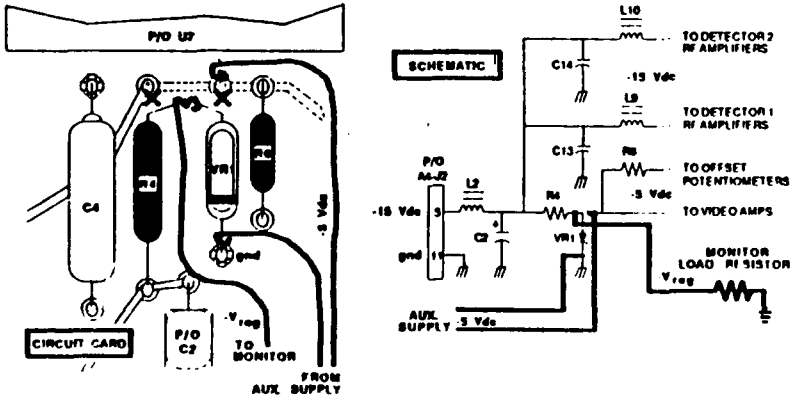
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 10:19 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.17 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 10:20 (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



3/12/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Sun Unit # 793 ...
Stress level 1
J12 output

****

Power at J12 is 8.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 702.0 MHz (Spec=+9dBm minimum)
Power at J12 is 3.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 705.0 MHz which is above the specified frequency.
Power at J12 is 5.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is .3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is .8 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 10.4 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.9 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.7 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.6 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.1 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is .3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.9 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.9 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.8 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.2 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.6 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.2 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.6 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 10.0 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is .2 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.8 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.5 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.5 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (xxxx MSN): 993 Test Date: 3/12/92

Tester: (Name & signature)

STEP-STRESS Level (xxxx 0 - 10): 0

Anomaly @ J12 from level 1 + to be checked @ level 0

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 10:20 (hour hr min) Start DWELL: 10 50 (hour hr min)

STEP-STRESS Level Chamber Air Temperature: 60.8 (°C) (Chamber thermocouple reading) Soak

Flange Temperature: 25.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 30 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: 15 (Vdc) - 5 Volts dc: -5 (Vdc)

+15 Volts dc: 115 (Vdc) -15 Volts dc: -15 (Vdc)

Aux. Constant - 5 Volts dc Setting: -511 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 10 50 (hour hr min)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1273 (mA) - 5 Volts dc: 81 (mA)

+15 Volts dc: 112 (mA) -15 Volts dc: 496 (mA)

End TEST: 10 51 (hour hr min)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (xxxx MSN): 993 Test Date: 3/12/92

STEP-STRESS Level (xxxx 0 - 10): 0 Retest of syn #2 only

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: (Hour hr min)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input (dBm)	I & Q Bits	Detector 1 L (usec) T (usec)	Detector 1 Duty Cycle (t/T)	Detector 2 L (usec) T (usec)	Detector 2 Duty Cycle (t/T)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/10/12

STEP-STRESS Level (enter 0 - 10): D Retest of synth 2 only

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: (TYMP HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/12

STEP-STRESS Level (enter 0 - 10): D Retest synth 2

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 10 51 (TYMP HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *measured for cable losses
50 (min)	(49) 684	10.17	(641) 684	10.87	J12 tested @ 642
35 (min)	729	10.17	729	11.27	Power OK
18 (min)	825	9.87	825	10.77	No Failure Found
00 (min)	921	9.25	921	9.35	* Freq measured w/ @ 685 MHz when retuned Pot.

Please check freq lab y correctly & USB power & plot on station.

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT no (Check here)

End TEST: ~~11:05~~ 11:20 (TYMP HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level

No failure found Continue to level 2

End DWELL: ~~11:05~~ 11:20 (TYMP HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter ASN): 993 Test Date: 5/13/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0 Restart of cycle 2 only

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

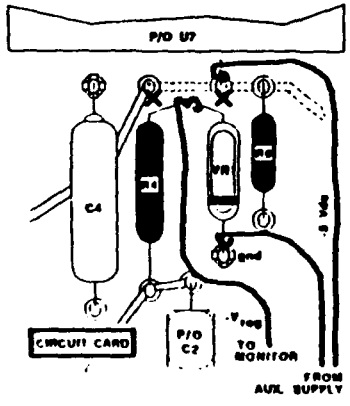
Start TEST: _____ (TIME HR MIN)

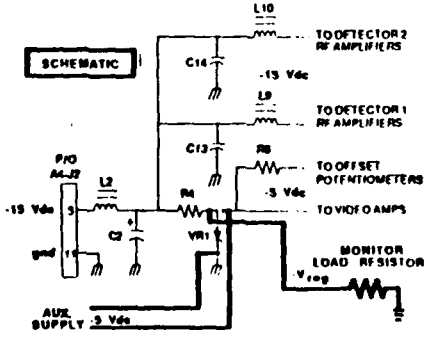
Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D; nominally 5 Vdc)

End TEST: _____ (TIME HR MIN)

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DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 2

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 10:20 (TIME HR MIN) Start DWELL: 10:50 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 76.1 / 24.7 (°C) (Chamber thermocouple reading) Flange Temperature: 57.5 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: ___ (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record settings below)

Supply Voltages: +5 Volts dc: 15.4 (Vdc) -5 Volts dc: -5.4 (Vdc)

+15 Volts dc: +15.6 (Vdc) -15 Volts dc: -15.6 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA *TESTS MAY BE PERFORMED IN ANY ORDER*

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 12:20 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1317 (mA) -5 Volts dc: 84 (mA)

+15 Volts dc: 115 (mA) -15 Volts dc: 5.7 (mA)

End TEST: 12:21 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 30 at this STEP-STRESS Level.

Start TEST: 12:21 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.1us/8.0us	50	4.0us/8.0us	50	
	I > Q	4.0us/8.0us	48.5	3.8us/8.0us	47.5	
	I + Q > 0	4.1us/8.0us	50	4.2us/8.0us	51.2	
	Q > 0	"	"	4.0us/8.0us	50	
Other Specify -70 (dBm)	I > 0	4.2us/8.0us	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ___ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	NOISY		5.0us/8.0us	52.5	
	I > Q	4.0us/8.0us	48.8	3.9us/8.0us	48.8	
	I + Q > 0	5.4us/8.0us	55	5.1us/8.0us	53.75	
	Q > 0	5.1us/8.0us	53.75	"	"	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number (enter NSN): 993 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Limit T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	482ns/96ns	50	485ns/96ns	49.5	
	I > Q	484ns/96ns	49.8	"	"	
	I + Q > 0	4.5ns/96ns	50	491ns/96ns	51.2	
	Q > 0	"	"	493ns/96ns	50	
Other: Specify -71 (dBm)	I > 0	491ns/96ns	51.2			
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	484ns/96ns	50	514ns/96ns	52.5	
	I > Q	484ns/96ns	50	486ns/96ns	49.8	
	I + Q > 0	522ns/96ns	55	514ns/96ns	53.75	
	Q > 0	504ns/96ns	52.5	"	"	

End TEST: 12:30 (Hour Min Unit)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number (enter NSN): 993 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): 2

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at the STEP-STRESS Level.

Start TEST: 12:37 (Hour Min Unit)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*measure for cable losses)
50 min	1972.16	-4.00	684	10.27	J5 output is unlocked
35 min	664.24	+10.67	727	10.51	U CHSL
18 min	346.46	+13.17	825	9.17	U Hit + set CHSL with RF Test
00 min	811.65	+11.55	921	7.85	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NA ✓ (Check here) to J12

End TEST: 12:45 (Hour Min Unit)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at the STEP-STRESS Level.

Need to verify accurately for J5 output (10 to 20 min level 1 @ 12:50

End DWELL: 12:50 (Hour Min Unit)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 993

Test Date: 3/12/92

Tester: (Please print name below)

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA — PERFORMANCE MONITORING

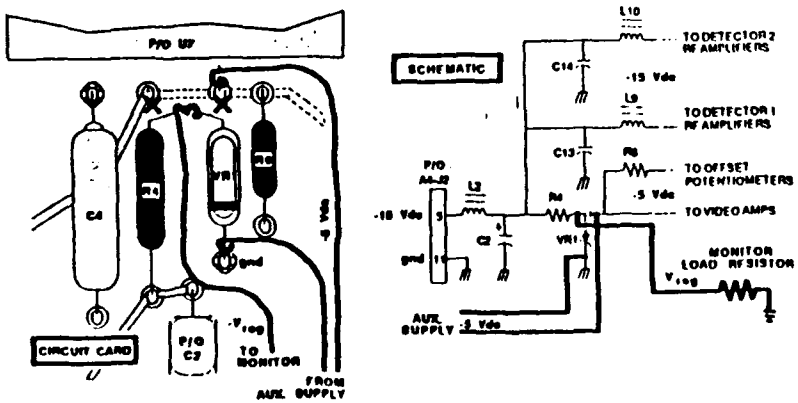
RESISTOR/ZENER DIODE MODIFICATION: A4 Detector: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 12:45 (HOUR MIN AM/PM)

Voltage across LOAD RESISTOR: -5.19 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 12:46 (HOUR MIN AM/PM)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION FOR AUX. CONSTANT -5 Vdc SUPPLY AND R4/VR1 MONITORING



3/12/93

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Sym Ref # 493

Stress level 2

T12 output

****

Power at J12 is 4.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 777.0 MHz which is above the specified frequency.
Power at J12 is 4.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 903.0 MHz which is above the specified frequency.
Power at J12 is-1.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 9.7 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.5 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.9 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.3 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.0 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.3 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.9 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.2 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.9 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.0 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.4 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.7 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.4 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.2 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is-6.0 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.8 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.3 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.0 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.1 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.9 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.7 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 921.0 MHz (Spec=+9dBm minimum).

STEP-STRESS TEST DATA SHEET

UUT Serial Number: 993 Test Date: 3/12/93

STEP-STRESS Level: 1 Tester:

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 12:50 Start DWELL: 13:20

STEP-STRESS Level Chamber Air Temperature: 65.8 (°C) Plenge Temperature: 76.1 (°C)

STEP-STRESS Level Component Temperature: 78 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level.

Supply Voltages: +5 Volts dc: +5.2 (Vdc) -5 Volts dc: -5.2 (Vdc)

+15 Volts dc: 115.3 (Vdc) -15 Volts dc: -15.3 (Vdc)

Ave. Constant -5 Volts dc Setting: -511 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for the STEP-STRESS Level.

Start TEST: 13:20

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1302 (mA) -5 Volts dc: 85 (mA)

+15 Volts dc: 117 (mA) -15 Volts dc: 51 (mA)

End TEST: 13:21

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 993 Test Date: 3/12/93

STEP-STRESS Level: 1 Retest of sys. #1 only

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST:

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L (spec) T (spec)	Detector 1 Duty Cycle (actual)	Detector 2 L (spec) T (spec)	Detector 2 Duty Cycle (actual)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 947 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): 1 Retest synth Ref # 1 only

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST (HHMM MS MSM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 947 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): 1

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 13 21 (HHMM MS MSM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*minimum for cable losses)
50 min	*931.45 807.6	11.77 -55?	684	10.27	*J5 still unlocked
35 min	668.	9.47	729	10.97	
18 min	744.4	15.27	825	4.87	
00 min	505.20	12.05	921	9.15	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT No (Check Here)

End TEST: 13 54 (HHMM MS MSM)

STEP STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

J7 still unlocked. Never verify Manually @ stress level 0

End DWELL: 13 35 (HHMM MS MSM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 993 Test Date: 3/12/92

Tester: (Name & comp below)

STEP-STRESS Level (enter 0 - 10): 1 Retest run # 1 only

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

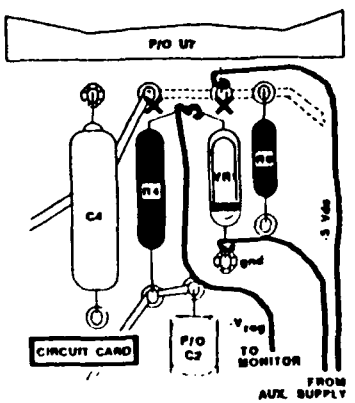
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

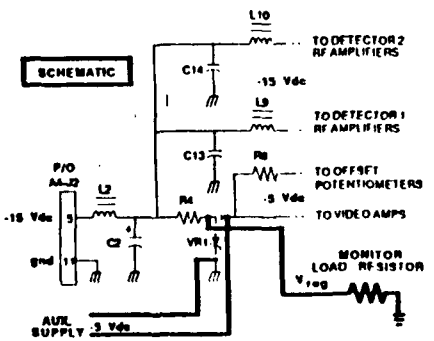
Start TEST: _____ (Time HR MIN)

Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: _____ (Time HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/97

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 0

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 13:35 (THUR HR MIN) Start DWELL: 14:05 (THUR HR MIN)

STEP-STRESS Level Chamber Air Temperature: 60.9 (°C) (Chamber thermocouple reading) Flange Temperature: 65.4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 72 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 4.5 (Vdc) -5 Volts dc: -5.0 (Vdc)

+15 Volts dc: +15.0 (Vdc) -15 Volts dc: -15.0 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 14:09 (THUR HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00. Synth Sig (J7 & J9) = 921 MHz. Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 238 (mA) -5 Volts dc: 81 (mA)

+15 Volts dc: 112 (mA) -15 Volts dc: 501 (mA)

End TEST: 14:10 (THUR HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/97

STEP-STRESS Level (enter 0 - 10): 0 total synth 1 only

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: (THUR HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz. Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 t (usec)	Detector 1 T (usec)	Detector 1 Duty Cycle (t/T)	Detector 2 t (usec)	Detector 2 T (usec)	Detector 2 Duty Cycle (t/T)	Observations
0 dBm	I > 0							
	I > Q							
	I + Q > 0							
	Q > 0							
Other: Specify (dBm)	I > 0							
	I > Q							
	I + Q > 0							
	Q > 0							
Other Specify (dBm)	I > 0							
	I > Q							
	I + Q > 0							
	Q > 0							
-75 dBm	I > 0							
	I > Q							
	I + Q > 0							
	Q > 0							

TEST Continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter NSN): 993 Test Date: 3/12/96

STEP-STRESS Level (enter 0 - 10): 0 Retest synth 1 only

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 L(max) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L(max) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: (HHMM HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter NSN): 993 Test Date: 3/12/96

STEP-STRESS Level (enter 0 - 10): 0

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 14 10 (HHMM HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *measure for cable losses
50 min	684	10.77	684	10.37	Pwr & Freq
35 min	729	10.97	729	11.05	will OK.
18 min	835	10.37	835	11.27	No Failures!
00 min	921	10.95	921	11.15	

Additional Testing (OPTIONAL); **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level Tester Name & Date. ATTACHMENT 94 (Order here)

End TEST: 14 20 (HHMM HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level. 3

Just Tpr. output OK Ramping to stress Tpr End DWELL 14 20 (HHMM HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 993 Test Date: 7/12/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - Vdc): 0 Retest spec # 1 only

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

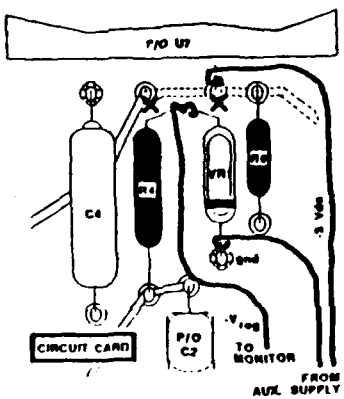
RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

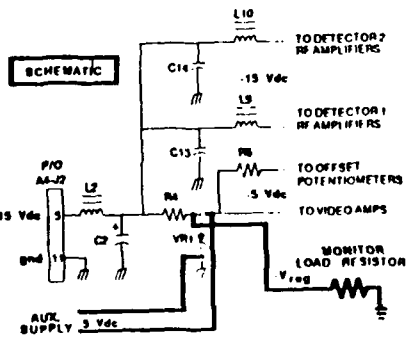
Start TEST: _____ (TIME HR MIN)

Voltage across LOAD RESISTOR: _____ (Vdc) (refer to Appendix D; normally 1 Vdc)

End TEST: _____ (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/92

Tester: (Name & many beside)

STEP-STRESS Level (enter 0 - 10): 3

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 14:20 (TIME HR MIN) Start DWELL: 14:50 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: 85.6 (°C) (Chamber thermocouple reading) Flange Temperature: 91.7 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: 94 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: 15.6 (Vdc) -5 Volts dc: -5.6 (Vdc)

+15 Volts dc: 15.9 (Vdc) -15 Volts dc: -15.9 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.11 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 15:05 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1356 (mA) -5 Volts dc: 87 (mA)

+15 Volts dc: 117 (mA) -15 Volts dc: 559 (mA)

End TEST: 15:06 (TIME HR MIN)

TEST continued next page

411-a

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/92

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with setting for Channels 30 or this STEP-STRESS Level.

Start TEST: 15:06 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.8us/96us	50	4.8us/96us	50	
	I > 0	4.6us/96us	48.8	4.6us/96us	48.8	
	I + Q > 0	4.8us/96us	50	4.9us/96us	51.2	
	Q > 0	"	"	4.8us/96us	50	
Other Specify -70 (dBm)	I > 0	5.0us/96us	52.5			
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify ___ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	NOISY		5.0us/96us	52.5	
	I > 0	4.6us/96us	48.8	4.6us/96us	48.8	
	I + Q > 0	5.2us/96us	55	5.2us/96us	54.55	
	Q > 0	5.0us/96us	52.5	5.16us/96us	53.75	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 993 Test Date: 7/12/97

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 Limit T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	92.5 kHz/9.6 kHz	50	4.6 kHz/9.6 kHz	48.8	
	I > Q	4.6 kHz/9.6 kHz	48.8	"	"	
	I + Q > 0	4.6 kHz/9.6 kHz	50	4.6 kHz/9.6 kHz	50	
	Q > 0	"	"	"	"	
Other: Specify -71 (dBm)	I > 0	5.6 kHz/9.6 kHz	52.5			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	120 Hz		5.6 kHz/9.6 kHz	53.75	
	I > Q	4.6 kHz/9.6 kHz	48.8	4.6 kHz/9.6 kHz	48.8	
	I + Q > 0	5.6 kHz/9.6 kHz	55	5.6 kHz/9.6 kHz	53.75	
	Q > 0	5.6 kHz/9.6 kHz	52.75	"	"	

End TEST: 15:20 (HOUR MIN GMT)

TEST continued on next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/97

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 15:21 (HOUR MIN GMT)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *account for cable losses
50 min	10 912.86	-4.27	0 684	10.27	✓ Known Good Unit Level ±
35 min	669.52	10.97	729	10.37	
18 min	716.90	12.99	825	10.47	No Failure
00 min	812.50	11.75	921	8.81	Ran Digital Out test for CH50 Clock on Pattern was set up correct freq was on Test 4

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT V (Check here) J12 output only

End TEST: 15:31 (HOUR MIN GMT)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at the STEP-STRESS Level.

End DWELL: 1550 (HOUR MIN GMT)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter N/A if n/a): 793

Test Date: 3/17/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 3

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

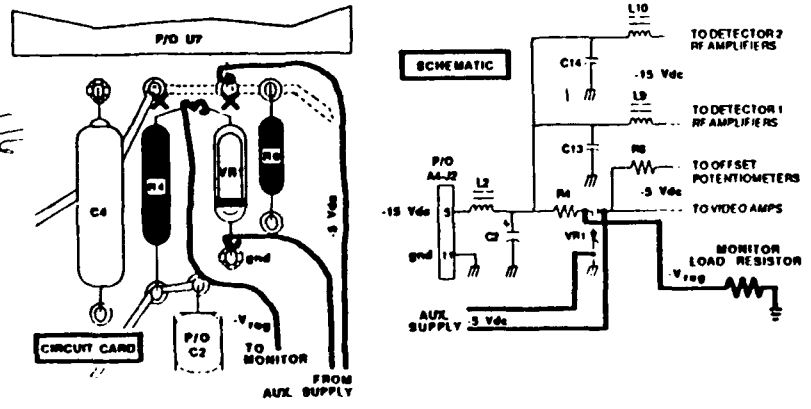
Start TEST: 1530 (Hour Minutes)

Voltage across LOAD RESISTOR: -519 (Vdc) (refer to Appendix D: nominally 5 Vdc)

End TEST: 1521 (Hour Minutes)

A15

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION FOR AUX. CONSTANT -5 Vdc SUPPLY AND R4/VR1 MONITORING



3/12/92

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

Sun Ref. 4993

Stress level 3 J12 output

****

Power at J12 is 7.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-8.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 696.0 MHz which is above the specified frequency.
Power at J12 is 2.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-12.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.0 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 825.0 MHz which is above the specified frequency.
Power at J12 is 5.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Frequency is less than 831.0 MHz which is below the specified frequency.
Power at J12 is 5.2 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 903.0 MHz which is above the specified frequency.
Power at J12 is-.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Frequency is less than 906.0 MHz which is below the specified frequency.
Power at J12 is 3.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 921.0 MHz (Spec=+9dBm minimum).
Frequency is greater than 921.0 MHz which is above the specified frequency.
****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #

Power at J12 is 9.8 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.1 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is-8.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.9 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.0 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 4.0 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.2 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is-4.0 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.5 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is-12.2 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 9.8 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is-1.1 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.8 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.1 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.6 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 8.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is-3.0 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.5 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is-2.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 6.7 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.3 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.4 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 2.7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.0 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.8 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is-5.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.7 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is-.1 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 3.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 1.0 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 5.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 7.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is .9 dBm @ 921.0 MHz (Spec=+9dBm minimum).

41.7

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 993 Test Date: 3/12/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 4

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level: Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 15:50 (THUR HR MIN)

Start DWELL: 16:20 (THUR HR MIN)

STEP-STRESS Level Chamber Air Temperature: +93.0 TC1 +92.3 TC2 (°C) Sat @ 92 °C (Chamber thermocouple reading)

Flange Temperature: +101.6 TC3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +102 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +5.80 (Vdc) -5 Volts dc: -5.80 (Vdc)

+15 Volts dc: +16.20 (Vdc) -15 Volts dc: -16.20 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1100 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level

Start TEST: 16:20 (THUR HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 139.4 (mA) -5 Volts dc: 86.6 (mA)

+15 Volts dc: 117.5 (mA) -15 Volts dc: 551.2 (mA)

End TEST: 16:21 (THUR HR MIN)

TEST continued next page

418

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 993 Test Date: 03/12/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input From 0 dBm to -75 dBm and record Duty Cycle (I/T) for each UUT Digital Output. Repeat with sensing for Channels 50 at this STEP-STRESS Level.

Start TEST: 16:23 (THUR HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 I (msec) / T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 I (msec) / T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	480/960	50.0	448/960	46.8	Bad-get 20 more/
	I > 0	456/	47.5	456/	47.5	
	I + Q > 0	490/	50.0	492/	51.2	
	Q > 0	492/	51.2	484/	50.0	
Other: Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	544/960	56.7	496/960	51.7	
	I > 0	464/960	48.8	416/	48.3	Bad-get 10 more/
	I + Q > 0	544/960	56.7	496/	51.7	
	Q > 0	512/960	53.3	512/	53.3	
Other: Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					

TEST Continued next page.

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 993 Test Date: 03/12/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 L (nsec) T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	450/960	50.0	456/960	47.5	
	I > Q	468/	48.8	11/	47.5	
	I + Q > 0	492/	51.2	492/	51.2	
	Q > 0	450/	50.0	480/	50.0	
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	490/960 NOISE	51.7	490/960	51.7	
	I > Q	480/960	50.0	464/	48.3	
	I + Q > 0	528/960	55.0	496/	51.7	
	Q > 0	512/960	53.3	512/	53.3	

End TEST 16:41 (HHMM MS MSM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 993 Test Date: 03/12/92

STEP-STRESS Level (enter 0 - 10): 4

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 16:42 (HHMM MS MSM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *minimum for cable losses
50 (HEX)	420.3 (harm 950.4)	-17.3 below Band pass -4.0	683.4 (harm 1366)	+10.0 -35dBm	Search Span 100MHz Sp 1.6GHz Sig#1 all freq Low. Sig#2 all freq ok, but noisy for that
35 (HEX)	667.6	+9.4	728.9	+7.9	
18 (HEX)	745.0	+12.4	824.9	+8.4 Low power	
00 (HEX)	811.2 OFF FREQ, RADIAN ANOMALY	+12.0 Pwr Good	920.9 Low Power, on FREQ ACCEPT	+5.7 low power	

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level Tester Name & Date. ATTACHMENT ✓ (Check here) J12 ONLY

End TEST 17:10 (HHMM MS MSM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUE TO LEVEL 5 End DWELL 17:20 (HHMM MS MSM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 993 Test Date: 03/12/92

Tester: J. D. Mueller

STEP-STRESS Level: 4

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Depot: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

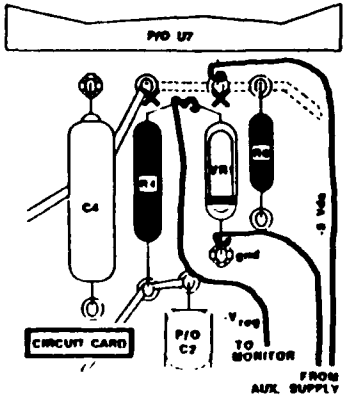
Start TEST: 16:21 (HOUR MIN)

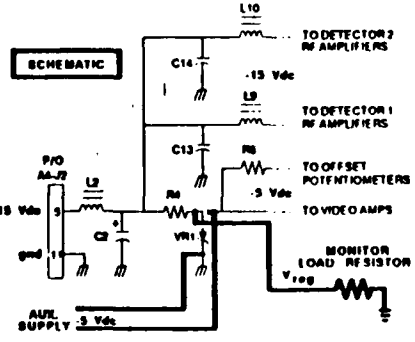
Voltage across LOAD RESISTOR: -5.2016 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 16:21 (HOUR MIN)

420

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





FAIL DATA (if any) of Power Output requirements will be printed between the starred borders. STEP-STRESS LEVEL 4

****

Power at J12 is 8.6 dBm @ 684.0 MHz (Spec=+9dBm minimum). MSN 993 J12 ONLY

Power at J12 is .0 dBm @ 687.0 MHz (Spec=+9dBm minimum). 03/12/92 @ 17:09

Power at J12 is .6 dBm @ 690.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 690.0 MHz which is above the specified frequency.

Power at J12 is 4.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).

Power at J12 is-1.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).

Frequency is less than 696.0 MHz which is below the specified frequency.

Power at J12 is 3.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 699.0 MHz which is above the specified frequency.

Power at J12 is 4.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 705.0 MHz which is above the specified frequency.

Power at J12 is .3 dBm @ 708.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 717.0 MHz which is above the specified frequency.

Power at J12 is 4.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 729.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 729.0 MHz which is above the specified frequency.

Power at J12 is 5.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.6 dBm @ 744.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 744.0 MHz which is above the specified frequency.

Power at J12 is 5.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 768.0 MHz which is above the specified frequency.

Power at J12 is 4.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).

Power at J12 is-6.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.5 dBm @ 777.0 MHz (Spec=+9dBminimum).

Frequency is less than 777.0 MHz which is below the specified frequency.

Power at J12 is .3 dBm @ 825.0 MHz (Spec=+9dBm minimum).

Power at J12 is-1.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).

Frequency is less than 831.0 MHz which is below the specified frequency.

Power at J12 is 4.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.5 dBm @ 882.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 885.0 MHz which is above the specified frequency.

Power at J12 is 1.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 897.0 MHz which is above the specified frequency.

Power at J12 is 2.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 900.0 MHz which is above the specified frequency.

Power at J12 is-.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).

Power at J12 is .3 dBm @ 909.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 909.0 MHz which is above the specified frequency.

Power at J12 is-.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).

Power at J12 is .5 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Power at J12 is-10.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.2 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 993 LEVEL 4

Power at J12 is 8.6 dBm @ 684.0 MHz (Spec=+9dBm minimum). Meas +10.0

Power at J12 is .0 dBm @ 687.0 MHz (Spec=+9dBm minimum).

Power at J12 is .6 dBm @ 690.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.8 dBm @ 693.0 MHz (Spec=+9dBm minimum).

Power at J12 is-1.9 dBm @ 696.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.7 dBm @ 699.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.5 dBm @ 702.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.4 dBm @ 705.0 MHz (Spec=+9dBm minimum).

Power at J12 is .3 dBm @ 708.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.1 dBm @ 714.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 717.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.2 dBm @ 720.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.9 dBm @ 723.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 729.0 MHz (Spec=+9dBm minimum). Meas +9.9

Power at J12 is 5.9 dBm @ 732.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 738.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.8 dBm @ 741.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.6 dBm @ 744.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.1 dBm @ 747.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.3 dBm @ 753.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.0 dBm @ 756.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.5 dBm @ 765.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.0 dBm @ 768.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.2 dBm @ 771.0 MHz (Spec=+9dBm minimum).

Power at J12 is-6.3 dBm @ 774.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.5 dBm @ 777.0 MHz (Spec=+9dBm minimum).

Power at J12 is .3 dBm @ 825.0 MHz (Spec=+9dBm minimum). Meas +3.4

Power at J12 is-1.6 dBm @ 828.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.5 dBm @ 831.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.0 dBm @ 834.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.0 dBm @ 837.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.5 dBm @ 882.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.2 dBm @ 885.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.9 dBm @ 888.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.7 dBm @ 894.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.3 dBm @ 897.0 MHz (Spec=+9dBm minimum).

Power at J12 is 2.7 dBm @ 900.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.6 dBm @ 906.0 MHz (Spec=+9dBm minimum).

Power at J12 is .3 dBm @ 909.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.5 dBm @ 912.0 MHz (Spec=+9dBm minimum)

Power at J12 is .5 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Power at J12 is-10.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.2 dBm @ 921.0 MHz (Spec=+9dBm minimum). Meas +5.2

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter 3 digits): 993 Test Date: 03/12/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 5

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 17:20 (HH:MM MR MSN) Start DWELL: 17:50 (HH:MM MR MSN)

STEP-STRESS Level Chamber Air Temperature: +99.7 (+186.7 °F) (°C) (Chamber thermocouple reading)

Flange Temperature: 102.7 (195.3 °F) (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +110 (°C) (refer to Appendix B Table)

Sole +112°C

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.00 (Vdc) -5 Volts dc: -6.00 (Vdc)

+15 Volts dc: +16.50 (Vdc) -15 Volts dc: -16.50 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1101 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 18:08 (HH:MM MR MSN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1427.9 (mA) -5 Volts dc: 88.3 (mA)

+15 Volts dc: 120.3 (mA) -15 Volts dc: 562.8 (mA)

End TEST: 18:09 (HH:MM MR MSN)

TEST continued next page

422

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter 3 digits): 993 Test Date: 03/12/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -.75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 50 at this STEP-STRESS Level.

Start TEST: 18:13 (HH:MM MR MSN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -.75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.20/4.60	50.0	4.68/5.60	45.8	
	I > 0	4.32/	47.5	4.44/	46.2	Edge / Square
	I + Q > 0	4.80/	50.0	4.92/	51.2	
	Q > 0	4.80/	50.0	4.92/	51.2	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-.75 dBm	I > 0	5.28/5.60 Noise	55.0	5.12/5.60	53.3	
	I > 0	4.80/	50.0	4.44/	46.7	Edge / Square
	I + Q > 0	5.28/	55.0	5.12/	53.3	
	Q > 0	5.12/	53.3	11/	53.3	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 993 Test Date: 03/12/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Level	I & Q Data	Detector 1 L(max) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L(max) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	430/960	50.0	432/960	47.5	8 dio @ 1.30 μsec/div
	I > Q	468/	48.8	"/	47.5	
	I + Q > 0	493/	51.2	480/	50.0	
	Q > 0	480/	50.0	492/	51.2	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	512/960	53.3	512/960	53.3	
	I > Q	480/	50.0	448/	46.7	6 dio @ 1.60 μsec/div
	I + Q > 0	544/	55.6	496/	51.7	
	Q > 0	512/	53.3	512/	53.3	

End TEST: 18:25 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 993 Test Date: 03/12/92

STEP-STRESS Level (enter 0 - 10): 5

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 18:26 (TIME HR MIN)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *account for cable losses
50 min	616.4 / 924.5	bel no BP / -20.3 / -4.6	684.0	+8.6 Low	Sig-1 dropped out Sig-2 dropped out Both locked & stable
35 mm	6632	+7.4	729.0	+10.3	NO FAILURES
18 mm	739.3	+12.2	824.9	+8.2 Low	
00 max	805.6	+11.7	921.0	+6.6 Low	

805.6 ANOMALY FREQ SHIFTED — Same as previous LEVEL

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT ✓ (Check box) J12 only

End TEST: 18:45 (TIME HR MIN)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

End DWELL 18:50 (TIME HR MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number: 993 Test Date: 03/12/92

Tester: A. D. Mueller

STEP-STRESS Level: 5

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

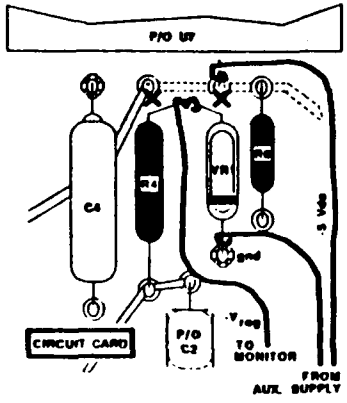
Start TEST: 18:10 (TIME HR:MIN)

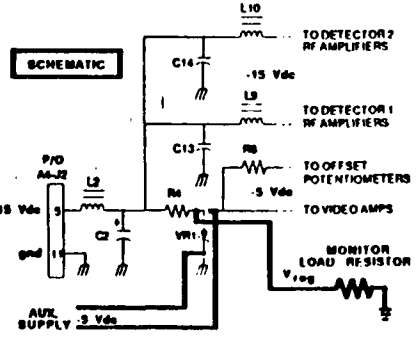
Voltage across LOAD RESISTOR: -5.2126 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 18:10 (TIME HR:MIN)

42.4

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





FAIL DATA (if any) of Power Output requirements will be printed between the starred borders. STEP-STRESS LEVEL 5

****

Power at J12 is 2.2 dBm @ 684.0 MHz (Spec=+9dBm minimum). J12 only MSN 993

Power at J12 is 6.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.5 dBm @ 690.0 MHz (Spec=+9dBm minimum). 03/12/97 (97466) (CSI)

Power at J12 is 5.3 dBm @ 693.0 MHz (Spec=+9dBm minimum). 0[illegible]43

Power at J12 is 8.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).

Power at J12 is-1.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.8 dBm @ 729.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).

Power at J12 is-2.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.4 dBm @ 741.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).

Power at J12 is-64.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).

Frequency is less than 759.0 MHz which is below the specified frequency.

Power at J12 is 4.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).

Power at J12 is-1.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).

Power at J12 is-6.8 dBm @ 825.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.2 dBm @ 834.0 MHz (Spec=+9dBm minimum).

Power at J12 is-5.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 885.0 MHz which is above the specified frequency.

Power at J12 is 4.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).

Power at J12 is .6 dBm @ 891.0 MHz (Spec=+9dBm minimum).

Frequency is greater than 891.0 MHz which is above the specified frequency.

Power at J12 is 5.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).

Power at J12 is-59.6 dBm @ 897.0 MHz (Spec=+9dBm minimum).

Frequency is less than 897.0 MHz which is below the specified frequency.

Power at J12 is .8 dBm @ 900.0 MHz (Spec=+9dBm minimum).

Power at J12 is .1 dBm @ 903.0 MHz (Spec=+9dBm minimum).

Power at J12 is .1 dBm @ 906.0 MHz (Spec=+9dBm minimum).

Frequency is less than 906.0 MHz which is below the specified frequency.

Power at J12 is-3.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).

Frequency is less than 912.0 MHz which is below the specified frequency.

Power at J12 is-1.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Power at J12 is-2.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).

Frequency is less than 918.0 MHz which is below the specified frequency.

Power at J12 is 4.8 dBm @ 921.0 MHz (Spec=+9dBm minimum).

****

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FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 993 LEVEL 5

Power at J12 is 2.2 dBm @ 684.0 MHz (Spec=+9dBm minimum). Meas +6

Power at J12 is 6.3 dBm @ 687.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.5 dBm @ 690.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.3 dBm @ 693.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.0 dBm @ 696.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.8 dBm @ 699.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.4 dBm @ 702.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.2 dBm @ 705.0 MHz (Spec=+9dBm minimum).

Power at J12 is-1.1 dBm @ 708.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.5 dBm @ 714.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.4 dBm @ 717.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.7 dBm @ 723.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.7 dBm @ 726.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.8 dBm @ 729.0 MHz (Spec=+9dBm minimum). Meas +10.3

Power at J12 is 6.0 dBm @ 732.0 MHz (Spec=+9dBm minimum).

Power at J12 is-2.8 dBm @ 735.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.3 dBm @ 738.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.4 dBm @ 741.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.5 dBm @ 747.0 MHz (Spec=+9dBm minimum).

Power at J12 is 6.5 dBm @ 750.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.6 dBm @ 753.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).

Power at J12 is-64.3 dBm @ 759.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.0 dBm @ 762.0 MHz (Spec=+9dBm minimum).

Power at J12 is 7.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.4 dBm @ 768.0 MHz (Spec=+9dBm minimum).

Power at J12 is 8.5 dBm @ 771.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.8 dBm @ 774.0 MHz (Spec=+9dBm minimum).

Power at J12 is-1.4 dBm @ 777.0 MHz (Spec=+9dBm minimum).

Power at J12 is-6.8 dBm @ 825.0 MHz (Spec=+9dBm minimum). Meas +5.2

Power at J12 is 5.8 dBm @ 828.0 MHz (Spec=+9dBm minimum).

Power at J12 is 1.8 dBm @ 831.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.2 dBm @ 834.0 MHz (Spec=+9dBm minimum).

Power at J12 is-5.6 dBm @ 837.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).

Power at J12 is 3.6 dBm @ 885.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.0 dBm @ 888.0 MHz (Spec=+9dBm minimum).

Power at J12 is .6 dBm @ 891.0 MHz (Spec=+9dBm minimum).

Power at J12 is 5.4 dBm @ 894.0 MHz (Spec=+9dBm minimum).

→ Power at J12 is-59.6 dBm @ 897.0 MHz (Spec=+9dBm minimum). May be missing

Power at J12 is .8 dBm @ 900.0 MHz (Spec=+9dBm minimum).

Power at J12 is .1 dBm @ 903.0 MHz (Spec=+9dBm minimum).

Power at J12 is .1 dBm @ 906.0 MHz (Spec=+9dBm minimum).

Power at J12 is-3.8 dBm @ 909.0 MHz (Spec=+9dBm minimum).

Power at J12 is-.3 dBm @ 912.0 MHz (Spec=+9dBm minimum).

Power at J12 is-1.5 dBm @ 915.0 MHz (Spec=+9dBm minimum).

Power at J12 is-2.3 dBm @ 918.0 MHz (Spec=+9dBm minimum).

Power at J12 is 4.8 dBm @ 921.0 MHz (Spec=+9dBm minimum). Meas +6.6

STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter MSN): 993 Test Date: 03/12/92

Tester: (Name & initials below)

STEP-STRESS Level (enter 0 - 10): 6

Reload plot from 18:57 to 19:05

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 18:50 (TIME HR MIN) Start DWELL: 19:20 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: Tc1 Tc2 (°C) (Chamber thermocouple reading) Set @ +111 °C

Flange Temperature: Tc3 Tc4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +118 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.20 (Vdc) -5 Volts dc: +6.20 (Vdc)

+15 Volts dc: +16.80 (Vdc) -15 Volts dc: -16.80 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1101 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 19:22 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rec Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents +5 Volts dc: 1467.4 (mA) -5 Volts dc: 91.4 (mA)

+15 Volts dc: 128.6 (mA) -15 Volts dc: 577.0 (mA)

End TEST: 19:23 (TIME HR MIN)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter MSN): 993 Test Date: 03/12/92

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with settings for Channels 50 at this STEP-STRESS Level.

Start TEST: 19:27 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rec Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rec Sig Input	I & Q Bits	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.56/9.60	50.0	4.80/9.60	50.0	
	I > Q	4.68/	48.8	4.56/	47.5	1.2 usec/
	I + Q > 0	4.80/	50.0	4.92/	51.2	
	Q > 0	" /	50.0	" /	51.2	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	5.28/9.60	55.0	5.28/9.60	55.0	
	I > Q	4.80/	50.0	4.64/	48.3	1.60 usec/
	I + Q > 0	5.12/	53.3	5.12/	53.3	
	Q > 0	4.96/	51.7	5.12/	53.3	
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 993 Test Date: 03/12/92

STEP-STRESS Level: 6

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 404 MHz. Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Inject -Bits	I & Q -Bits	Detector 1 Count T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 Count T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/960	50.0	4.80/960	50.0	
	I > 0	480 / 494	50.0	4.56 / 4.80	47.5	8 d.i. 1 response
	I + Q > 0		51.2		50.0	
	Q > 0	4.80 / 4.80	50.0	4.80 / 4.80	50.0	
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	5.12/960	53.3	4.96/960	51.7	
	I > 0	480 / 5.28	50.0	4.64 / 5.12	48.3	6 d.i. 1 response
	I + Q > 0		55.0		53.3	
	Q > 0	4.96 / 4.96	51.7	4.96 / 4.96	51.7	

End TEST: 19:37 (HHMM MM MM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

UUT Serial Number: 993 Test Date: 03/12/92

STEP-STRESS Level: 6

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 19:47 (HHMM MM MM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*request for cable losses)
50 min (below band)	6099 (now 919.9)	-22.5 / -5.0	626.8 (now 940.2)	-6.4 / -3.8	below bandpass
35 min	6554 (now 983.2)	+1.8 / -19.5	671.9	+8.4	
18 min	725.1	+11.8	751.6	+11.6	Both Synth's PULLED LOW IN FREQUENCY KNOWN ANOMALY
00 min	793.0	+11.5	827.0	+10.7	

Additional Testing (OPTIONAL); RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

Used Test #2 Freq Sweep to Exercise Further

End TEST: 20:12 (HHMM MM MM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUE ON WITH LEVEL 7 End DWELL: 20:20 (HHMM MM MM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 993

Test Date: 03/12/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 6

UUT PERFORMANCE TEST DATA — PERFORMANCE MONITORING

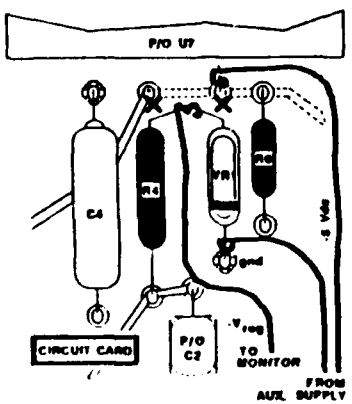
RESISTOR/ZENER DIODE MODIFICATION: At Duett: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level

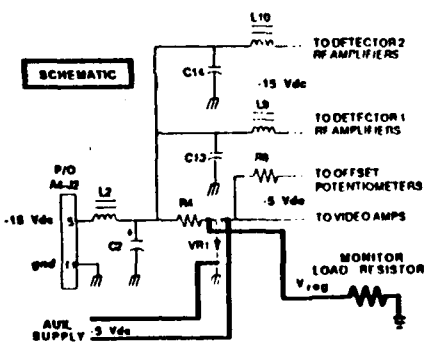
Start TEST: 19:23 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.2230 (Vdc) (refer to Appendix D, nominally -5 Vdc)

End TEST: 19:24 (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter NSN): 993 Test Date: 03/12/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 7

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 20:20 (THUR HR MIN)

Start DWELL: 20:50 (THUR HR MIN)

STEP-STRESS Level Chamber Air Temperature: +46.3 (°C) (Chamber thermocouple reading) — +117.2 rel; Sole -119 °C

Flange Temperature: +27.4 (°C) (Thermocouple reading) — +126.9 rel

STEP-STRESS Level Component Temperature: +126 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: + 5 Volts dc: +6.40 (Vdc) - 5 Volts dc: -6.40 (Vdc)

+15 Volts dc: +17.10 (Vdc) -15 Volts dc: -17.10 (Vdc)

Asm. Constant - 5 Volts dc Setting: -5.1101 (Vdc)

UUT PERFORMANCE TEST DATA — TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (other) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 20:55 (THUR HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: + 5 Volts dc: 1505.2 (mA) - 5 Volts dc: 89.5 (mA) slight dynamic delay

+15 Volts dc: 127.3 (mA) slight dynamic delay -15 Volts dc: 588.5 (mA)

End TEST: 20:57 (THUR HR MIN)

TEST continued next page

42:9

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter NSN): 993 Test Date: 03/12/92

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 as this STEP-STRESS Level.

Start TEST: 20:58 (THUR HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.92/9.60	51.2	4.80/9.60	50.0	
	I > Q	4.68/	48.8	4.56/	47.5	
	I + Q > 0	4.80/	50.0	4.92/	51.2	
	Q > 0	" /	50.0	4.92/	51.2	
Other: Specify -72 (dBm)	I > 0	5.12/9.60	53.3			
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	—/9.60	None See above	5.12/9.60	53.3	
	I > Q	4.80/	50.0	4.64/	48.3	
	I + Q > 0	5.28/	55.0	5.12/	53.3	
	Q > 0	5.12/	53.3	5.12/	53.3	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 5 of 6

UUT Serial Number: 993 Test Date: 03/12/92

STEP-STRESS Level: 7

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q Bits	Detector 1 Limit T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/5.60	50.0	4.64/5.60	48.8	
	I > Q	4.68/	48.8	4.56/	47.5	8 d.i.
	I + Q > 0	4.92/	51.2	4.92/	51.2	1.2 usec/d.i.
	Q > 0	4.80/	50.0	4.80/	50.0	
Other: Specify (dBm)	I > 0	5.60				
	I > Q	/				
	I + Q > 0	/	48m			
	Q > 0	/				
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	4.96/5.60	51.7	4.96/5.60	51.7	
	I > Q	4.64/	48.3	4.64/	48.3	6 d.i.
	I + Q > 0	5.28/	55.0	5.12/	53.3	1.6 usec/d.i.
	Q > 0	4.96/	51.7	11 /	53.3	

End TEST: 21:09 (HHMM MS MM)

TEST continued next page

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STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 6 of 6

UUT Serial Number: 993 Test Date: 03/12/92

STEP-STRESS Level: 7

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 21:11 (HHMM MS MM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations (*measure for cable losses)
50 min 41.8	602.2	-25.2	621.1	-8.9	: below Prob 6 - 1 of 100 # failed
	nom 9:35	-4.2	nom 9:35	-2.0	
35 min 46.2	644.8	-3.1	664.6	-16.4	: Synth #1 20 min below Synth #2
	nom 978.0	-15.2	nom 997.0	-30.5	
18 min 145	715.5	+11.8	740.6	+11.7	
00 min 145.1	772.3	+11.6	808.1	+10.8	

KNOW ANOMALY

BOTH SYNTHS HAVE NEXT FREQ. BOTH SYNTHS TRACK EACH OTHER NOW.

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 21:29 (HHMM MS MM)

21:35 Bumped pen and caused plotter error. Could not continue. SB Malbi 03/12/92

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUED ON TO NEXT HIGHER LEVEL, 8. End DWELL: 21:50 (HHMM MS MM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter NSN): 993

Test Date: 03/12/92

Tester: (Please fill stamp below)

STEP-STRESS Level (enter 0 - 10): 7

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

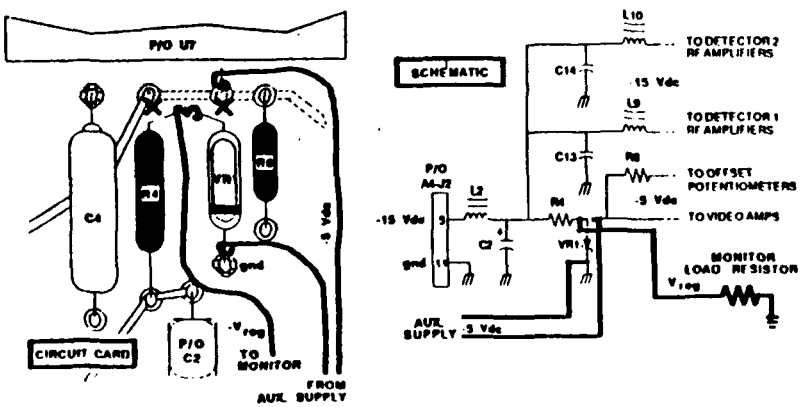
RESISTOR/ZENER DIODE MODIFICATION: At Depot: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

Start TEST: 20:57 (TIME HR MIN)

Voltage across LOAD RESISTOR: -5.2352 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 20:57 (TIME HR MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number: 993 Test Date: 03/12/92

Tester: [signature]

STEP-STRESS Level: 8

21:55 Started Plot #3 by request from operator error with pen plotter. [signature] 03/12/92

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 21:50 (HHMM MM MM)

Start DWELL: 22:20 (HHMM MM MM)

STEP-STRESS Level Chamber Air Temperature: +126.0 (°C) +125.0 TC1 Set @ +127°C

Plenge Temperature: +135.0 (°C) +139.8 °C TC3

STEP-STRESS Level Component Temperature: +134 (°C)

VOLTAGE STEP-STRESS: During Temperature Ramp; Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.60 (Vdc) -5 Volts dc: -6.60 (Vdc)

+15 Volts dc: +17.40 (Vdc) -15 Volts dc: -17.40 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1162 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 22:26 (HHMM MM MM)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1562.2 (mA) -5 Volts dc: 86.6 (mA) slight continued decrease

+15 Volts dc: 119.7 (mA) decreased once -15 Volts dc: 600.1 (mA)

End TEST: 22:29 (HHMM MM MM)

KNOWN ANOMALIES

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number: 993 Test Date: 03/12/92

STEP-STRESS Level: 8

[signature]

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 or 99 at this STEP-STRESS Level.

Start TEST: 22:33 (HHMM MM MM)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rev Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L (msec) / T (msec)	Detector 1 Duty Cycle (percent)	Detector 2 L (msec) / T (msec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.80/9.60	50.0	4.68/9.60	48.8	
	I > 0	4.68/	~~50.8~~ 48.8	4.56/	47.5	
	I + Q > 0	4.80/	50.0	4.92/	51.2	
	Q > 0	" /	50.0	4.80/	50.0	
Other: Specify -72 (dBm)	I > 0	5.44/9.60	56.7			
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Noise/9.60	Separate	4.56/9.60	51.7	
	I > 0	4.80/	50.0	4.80/	50.0	
	I + Q > 0	5.04/	56.7	5.28/	55.0	
	Q > 0	5.28/	55.0	5.28/	55.0	

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number: 993 Test Date: 03/12/92

STEP-STRESS Level: 8

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q Bits	Detector 1 Limit T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	490/560	50.0	488/560	48.8	
	I > Q	488/	48.8	488/	48.8	
	I + Q > 0	492/	51.2	492/	51.2	
	Q > 0	0/	51.2	480/	50.0	
	I > 0	496/560	51.7	Mostly above		
Other: Specify -72 (dBm)	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	Noise/960	See above	512/960	53.3	
	I > Q	496/	51.7	480/	50.0	
	I + Q > 0	512/	53.3	512/	53.3	
	Q > 0	512/	53.3	0/	53.3	

End TEST: 22:44 (HHMM MS MM)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number: 993 Test Date: 03/12/92

STEP-STRESS Level: 8

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 22:44 (HHMM MS MM)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations
50	550.1	-31	610.8	-14.5	*Same as data on 03/10/92
35	634.6	-10.6	653.6	+3.6	
18	698.1	+10.6	724.1	+11.2	
00	748.9	+11.3	784.3	+10.7	

In addition: Used TONIC Freq Sweep to Exercise & Monitor other frequencies

KNOWN FREQ. SHIFT ANOMALIES

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here)

End TEST: 23:20 (HHMM MS MM)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

CONTINUE TO LEVEL 9 End DWELL 23:20 (HHMM MS MM)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (xxx-xxx): 993 Test Date: 03/12/92

Tester: (Please fill in and sign below)

STEP-STRESS Level (xxx 0 - 10): 8

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at the STEP-STRESS Level.

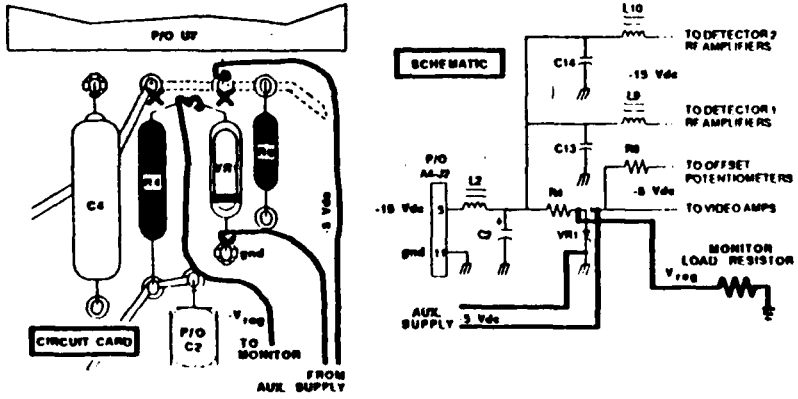
Start TEST: 22:31 (Hour Minute)

Voltage across LOAD RESISTOR: -5.2483 (Vdc) (Refer to Appendix D; nominally -5 Vdc)

End TEST: 22:32 (Hour Minute)

434

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter HEX): 993 Test Date: 03/12/92

Tester: (Name & comp below)

STEP-STRESS Level (enter 0 - 10): 9

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level. Stabilize, and Start Dwell at STEP-STRESS Level.

03/12/92

Begin RAMP: 23:20 (HOUR HR MIN)

Start DWELL: 23:50 (HOUR HR MIN)

STEP-STRESS Level Chamber Air Temperature: +132.8 TC1 +131.7 TC2 (°C) Soak @ +135°C (Chamber thermocouple reading)

Plenum Temperature: +134.5 TC4 +133.2 TC3 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +142 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +6.80 (Vdc) -5 Volts dc: -6.80 (Vdc)

+15 Volts dc: +17.70 (Vdc) -15 Volts dc: -17.70 (Vdc)

Aux. Constant - 5 Volts dc Setting: -5.1102 (Vdc)

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 23:50 (HOUR HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1624.0 (mA) -5 Volts dc: 94.7 (mA) Increasing after Repeat Accuracy

+15 Volts dc: 120.0 (mA) -15 Volts dc: 611.6 (mA)

End TEST: 23:53 (HOUR HR MIN) very slight increase beginning

TEST continued next page

433

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 1 of 4

UUT Serial Number (enter HEX): 993 Test Date: 03/12/92

STEP-STRESS Level (enter 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (t/T) for each UUT Digital Output. Repeat with setting for Channels 30 or this STEP-STRESS Level.

Start TEST: 23:53 (HOUR HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig Input	I & Q	Detector 1 t (usec) / T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 t (usec) / T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	496/960	50.0	496/960	48.8	Adv @ 1.20 usec/
	I > Q	468/	48.8	456/	47.5	
	I + Q > 0	480/	50.0	480/	50.0	70 F
	Q > 0	480/	50.0	480/	50.0	(Thermal Transient test)
Other Specify -72 (dBm)	I > 0	523/960	55.0	→ -70 : Same		
	I > Q					
	I + Q > 0	504/960	56.7			
	Q > 0					
Other Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
.75 dBm	I > 0	Noisy/960	Same	464/960	48.3	Adv @ 1.60 usec/
	I > Q	512/	53.3	464/	48.3	
	I + Q > 0	504/	56.7	496/	51.7	
	Q > 0	512/	53.3	512/	53.3	

TEST Continued next page

00:02 03/13/92

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (xxx MSN): 993 Test Date: 03/13/92

STEP-STRESS Level (xxx 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

00:02

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q -Bits	Detector 1 L (xxx) T (xxx)	Detector 1 Duty Cycle (percent)	Detector 2 L (xxx) T (xxx)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	4.92/9.60	51.2	4.68/9.60	48.8	
	I > Q	4.80/	50.0	4.68/	48.8	8 div @ 1.20 msec/
	I + Q > 0	4.92/	51.2	4.80/	50.0	
	Q > 0	4.80/	50.0	4.80/	50.0	
Other Specify -72 (dBm)	I > 0	4.96/9.60	51.7	Most low power @ -72dBm		
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify ____ (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	None 5.12/9.60	53.3	4.92/5.10	51.7	
	I > Q	4.96/	51.7	4.80/	50.0	6 div @ 1.60 msec/
	I + Q > 0	5.44/	56.7	5.12/	53.3	
	Q > 0	4.96/	51.7	5.12/	53.3	

End TEST: 00:08 (HH:MM MM:SS)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (xxx MSN): 993 Test Date: 03/13/92

STEP-STRESS Level (xxx 0 - 10): 9

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 00:08 (HH:MM MM:SS)

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *comment for cable losses
50	115.5 568.7	-35.7	584.6	-29.1	
	853.1	+0.1	883.8	+1.0	
35	115.6 612.8	-20.3	91.2 637.8	-2.5	STILL BEHAVING LIKE KNOWN ANOMALY
	921.7	-6.7	956.9	-15.3	
18	92.6 672.4	+5.4	700.1	+10.6	BOTH SYNTH'S STILL TRACK EACH OTHER & OTHER UNITS
	1008.7	-3.4	1050.7	-4.0	
00	85.6 712.8	+10.9	748.1	+11.0	
	1069.6	-4.5	1122.4	-4.9	

Additional Testing (OPTIONAL); **RADIO FREQUENCY OUTPUT TEST**: At Dwell: Set UUT Frequency Word Input to Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STEP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check here) OSC FREQ

End TEST: 00:34 (HH:MM MM:SS)

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

BOTH SYNTHS & DETECTOR ARE ACCEPTABLE. RECORD TO COMPLETE

End DWELL: 00:50 (HH:MM MM:SS)

03/13/92

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter last 3 digits): 993	Test Date: 03/13/92
STEP-STRESS Level (enter 0 - 10): 9	Tester: (Name & stamp below)

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

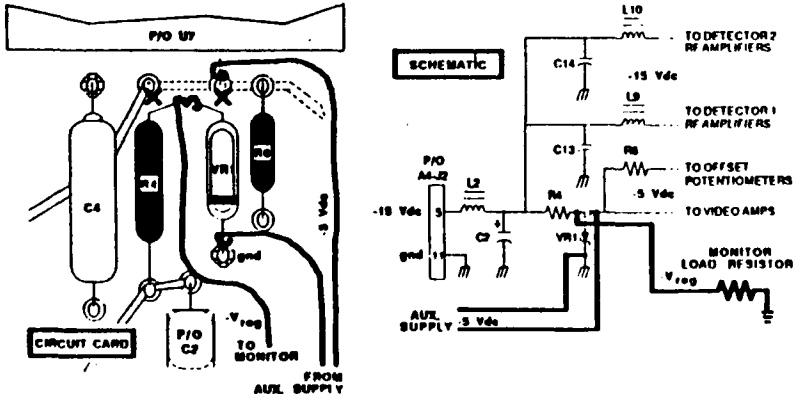
Start TEST: 00:37 (TIME: HR MIN)

Voltage across LOAD RESISTOR: -5.2587 (Vdc) (refer to Appendix D, nominally -5 Vdc)

End TEST: 00:38 (TIME: HR MIN)

437

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number: 998 Test Date: 03/13/92

Tester: D.D. Mueller (9346 TEST)

STEP-STRESS Level: 10

STEP-STRESS LEVEL DATA

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 00:50 (TIME HR MIN) Start DWELL: 01:20 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +139.2 TE1 +139.2 TE2 (°C) (Chamber thermocouple reading) Soak +143 °C

Flange Temperature: +150.4 TE3 +151.1 TE4 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +150 (°C) (refer to Appendix D Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level. (Record settings below)

Supply Voltages: +5 Volts dc: +7.00 (Vdc) -5 Volts dc: -7.00 (Vdc) See Note below

+15 Volts dc: +18.00 (Vdc) -15 Volts dc: -18.00 (Vdc)

Adj. Constant - 5 Volts dc Setting: -5.1102 (Vdc)

TE1 +140.9 TE2 +139.2 TE3 +150.4 TE4 +151.1 @ 01:18

NOTE 01:15 : 25 Minutes into Ramp and Stabilization prior to Level 10 Dwell. -5V Supply voltage (was +7.00) went to -0.91 V @ 2.91 Amps. Continued with Stabilization and LEVEL 10 Dwell. (9346 TEST) 03/13/92 D.D. Mueller

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell; Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 01:26 (TIME HR MIN)

Settings: Freq Word (J1-01 & J3-01) = CH 00; Synth Sig (J7 & J9) = 921 MHz; Rec Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1635.5 (mA) -5 Volts dc: 2.87 Amps (Now @ -0.89 Vdc) See Note above

+15 Volts dc: 116.4 (mA) -15 Volts dc: 607.7 (mA)

End TEST: 01:29 (TIME HR MIN)

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number: 993 Test Date: 03/13/92

STEP-STRESS Level: 10 (9346 TEST)

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell; Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 30 at this STEP-STRESS Level.

Start TEST: Since 01:15 (TIME HR MIN) -5V Supply Short

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rec Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rec Sig Input	I & Q Bits	Detector 1 T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	1560		1620		
	I > 0	1		1		
	I + Q > 0	1		1		
	Q > 0	1		1		
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > 0					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	1560		1660		
	I > 0	1		1		
	I + Q > 0	1		1		
	Q > 0	1		1		

RAILED HIGH NO OUTPUTS BOTH DETECTORS. KNOWN FAILURE AS WITH MSN 0172 & 0815 01:32 (9346 TEST) 03/13/92 D.D. Mueller

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (xxxx MSN): 993 Test Date: 03/13/92

STEP-STRESS Level (xxxx 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Input	I & Q Bits	Detector 1 L(xxxx) T (xxxx)	Detector 1 Duty Cycle (percent)	Detector 2 L(xxxx) T (xxxx)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0	/960		/960		
	I > Q	/		/		
	I + Q > 0	/		/		
	Q > 0	/		/		
Other: Specify (dBm)	I > 0					SEE SHEET 2
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0	/960		/960		
	I > Q	/		/		
	I + Q > 0	/		/		
	Q > 0	/		/		

End TEST: 01:32 (HH:MM MM:SS) FAILURE MODE KNOWN

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (xxxx MSN): 993 Test Date: 03/13/92

STEP-STRESS Level (xxxx 0 - 10): 10

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 01:33 (HH:MM MM:SS)

Channel	Synthesizer 1 (J3) Frequency (MHz)	Synthesizer 1 (J3) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observation *comment for cable losses
50 (xxx)	837.5	+3.4	763.0	+10.1	Same frequency for each Synthesizer
35 (xxx)	837.4	+3.4	766.3	+10.3	Suspect all frequencies Measured are really their harmonics & Carrier is far below bandpass
18 (xxx)	858.4	+1.7	815.7	+8.5	
00 (xxx)	923.4	+1.6	872.5	+5.2	

DIFFERENT

Additional Testing (OPTIONAL): **RADIO FREQUENCY OUTPUT TEST** At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT NO (Check box)

~~Need to Check Synth Anomaly at LEVEL 9 (tested)~~

End TEST: 02:05 (HH:MM MM:SS)

Using Test #2 Frequency Sweep, Synth #1 Apps at 4 pts & Synth #2 Apps at 4 pts of 6 points.

ANOMALY IS KNOWN. OCCURRED WITH NEW UUT 03/6/92 at LEVEL 10. 03/13/92

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

RETURN TO LEVEL 0 TO VERIFY FAILURE End DWELL 02:20 (HH:MM MM:SS)

WITH -5V Supply.

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 993

Test Date: 03/13/92

Tester: (Name & stamp or initials)

STEP-STRESS Level (enter 0 - 10): 10

UUT PERFORMANCE TEST DATA (PERFORMANCE MONITORING)

RESISTOR/ZENER DIODE MODIFICATION: At Dwell: For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

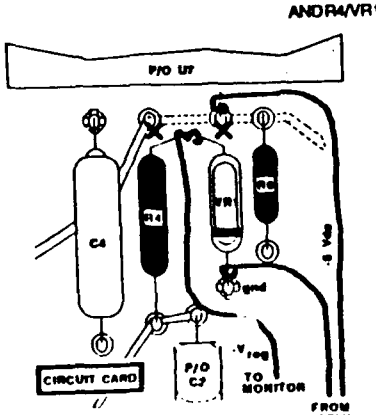
Start TEST: 01:29 (TIME HR MIN)

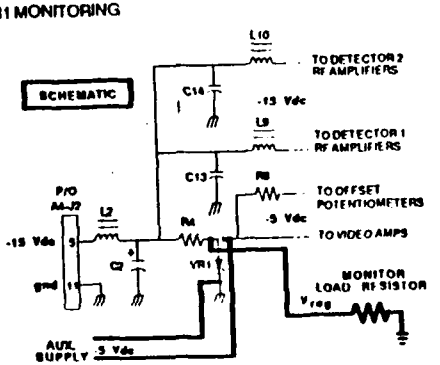
Voltage across LOAD RESISTOR: -5.2943 (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 01:29 (TIME HR MIN)

4-10

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING





STEP-STRESS TEST DATA SHEET

Sheet 1 of 4

UUT Serial Number (enter SERN): 993 Test Date: 03/13/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0 FINAL

Document voltage through decreasing transition to LEVEL 0 from LEVEL 10.
02:35 Disconnect J01J3 to determine J2 at station to allow documenting of supply voltages.
Confirms that -5V supply short is located with DETECTOR

STEP-STRESS LEVEL DATA

02:55 Reconnect J01J3 to DETECTOR J2 to allow FAILURE & DETECTOR OPERATION DURING QUALIFICATION TESTING.

TEMPERATURE STEP-STRESS: Ramp Chamber Temperature to STEP-STRESS Level; Stabilize, and Start Dwell at STEP-STRESS Level.

Begin RAMP: 02:20 (TIME HR MIN) (40 minutes 03:00 ramp) (30 minutes 03:30 stabilize) Start DWELL: 03:45 (TIME HR MIN)

STEP-STRESS Level Chamber Air Temperature: +61.1 (°C) (Chamber thermocouple reading) Flange Temperature: +68.5 (°C) (Thermocouple reading)

STEP-STRESS Level Component Temperature: +70 (°C) (refer to Appendix B Table)

VOLTAGE STEP-STRESS: During Temperature Ramp: Increment Voltage to STEP-STRESS Level (Record readings below)

Supply Voltages: +5 Volts dc: +5.00 (Vdc) -5 Volts dc: -5.00 (Vdc) S/B @ IS -0.787 Vdc 03:40

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.00 (Vdc)

Aux. Constant -5 Volts dc Setting: -5.1100 (Vdc)

991

UUT PERFORMANCE TEST DATA TESTS MAY BE PERFORMED IN ANY ORDER

UUT CURRENT TEST: At Dwell: Set UUT Frequency Word, Synthesized Signal, & Received (0 dBm) Signal Inputs for Channel 00. Record UUT Currents for this STEP-STRESS Level.

Start TEST: 03:45 (TIME HR MIN) SEE ALSO SHEET 4

Settings: Freq Word (J1-01 & J3-01) = CH 00: Synth Sig (J7 & J9) = 921 MHz Rcv Sig (J8) = 607.35 MHz at 0 dBm

UUT Currents: +5 Volts dc: 1204.1 (mA) -5 Volts dc: 2822 (mA) FAILURE

+15 Volts dc: 99.7 (mA) -15 Volts dc: 489.5 (mA)

End TEST: 03:47 (TIME HR MIN) FAILURE RAMP @ 27350

TEST continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 2 of 4

UUT Serial Number (enter SERN): 993 Test Date: 03/13/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA CONTINUED

UUT DIGITAL OUTPUT TEST: At Dwell: Set UUT Synthesized Signal and Received Signal Inputs for Channel 00. Decrease Received Signal Input from 0 dBm to -75 dBm and record Duty Cycle (T/T) for each UUT Digital Output. Repeat with setting for Channels 50 or this STEP-STRESS Level.

Start TEST: 03:48 (TIME HR MIN)

Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm

Rcv Sig (SERN)	I & Q Bits	Detector 1 L (usec) T (usec)	Detector 1 Duty Cycle (percent)	Detector 2 L (usec) T (usec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					NO DETECTOR I & Q WITH J2/101J3 CONNECTED. -5 VOLT SUPPLY SHORTED ON DETECTOR
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

TEST Continued next page

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 3 of 4

UUT Serial Number (enter MSN): 993 Test Date: 03/13/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

ADM

UUT PERFORMANCE TEST DATA CONTINUED

DIGITAL OUTPUT TEST: Continued. (Refer to Procedure on previous page)

Channel 50: Settings: Synth Sig (J7 & J9) = 484 MHz Rev Sig (J8) = 370.35 MHz at 0 to -75 dBm

Rev Sig Level	I & Q	Detector 1 Limit T (nsec)	Detector 1 Duty Cycle (percent)	Detector 2 Limit T (nsec)	Detector 2 Duty Cycle (percent)	Observations
0 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					SEE SHEET 2
	I > Q					
	I + Q > 0					
	Q > 0					
Other: Specify (dBm)	I > 0					
	I > Q				1	
	I + Q > 0					
	Q > 0					
-75 dBm	I > 0					
	I > Q					
	I + Q > 0					
	Q > 0					

End TEST: 03:51 (HHMM MS MIN) DETECTOR -5V SUPPLY LINE FAILURE

TEST continued next page

442

STEP-STRESS TEST DATA SHEET (CONTINUED)

Sheet 4 of 4

UUT Serial Number (enter MSN): 993 Test Date: 03/13/92

STEP-STRESS Level (enter 0 - 10): 0 FINAL

ADM

UUT PERFORMANCE TEST DATA CONTINUED

RADIO FREQUENCY OUTPUT TEST: At Dwell: Set UUT Frequency Word Input to Channel 50. Record the Synthesizer Mixer Port Output Frequency & Power. Repeat with settings for Channels 35, 18, and 00 at this STEP-STRESS Level.

Start TEST: 03:52 (HHMM MS MIN) DISCONNECT FAILING DETECTOR -5V SUPPLY LINE AT STATION 10133 SINCE IT AFFECTS SYNTHESIZER OPERATION

Channel	Synthesizer 1 (J5) Frequency (MHz)	Synthesizer 1 (J5) Power* (dBm)	Synthesizer 2 (J12) Frequency (MHz)	Synthesizer 2 (J12) Power* (dBm)	Observations *current for cable losses
50 (HEX)	664.0	+10.7	684.0	+10.5	10133/DET J3 DISCONNECTED
35 (HEX)	729.0	+12.5	729.0	+12.3	+5V 1151.8 mA
18 (HEX)	825.0	+11.9	825.0	+12.2	-5V 39.7 mA OK
00 (HEX)	921.0	+11.0	921.0	+11.2	+15V 58.8 mA
		PASSES			-15V 193.5 mA

Additional Testing (OPTIONAL): RADIO FREQUENCY OUTPUT TEST — At Dwell: Set UUT Frequency Word Input at Channel 50 thru Channel 00 and measure Synthesizer Mixer Port Output Power at each Frequency.

ATTACH the Data Printout (copy) to this STEP-STRESS TEST DATA SHEET. Label attachment with UUT Serial Number & STREP-STRESS Level. Tester Name & Date. ATTACHMENT (Check here)

End TEST: 04:11 (HHMM MS MIN) DETECTOR CONNECTOR 10133 REMAINS DISCONNECTED FOR REMAINDER OF TESTING

STEP-STRESS LEVEL DATA CONTINUED

TEMPERATURE STEP-STRESS: The Dwell will have a duration of 1-hour at this STEP-STRESS Level.

RETURN TO ROOM TEMPERATURE
TURN UUT POWER OFF AT 05:25

LEVEL 0 FINAL
End DWELL: 04:45 (HHMM MS MIN)

STEP-STRESS LEVEL COMPLETE

SUPPLEMENTAL (APPENDIX D)
STEP-STRESS TEST DATA SHEET

Sheet 1 of 1

UUT Serial Number (enter MSN): 993 Test Date: 03/13/92

Tester: (Name & stamp below)

STEP-STRESS Level (enter 0 - 10): 0 FINAL

UUT PERFORMANCE TEST DATA PERFORMANCE MONITORING

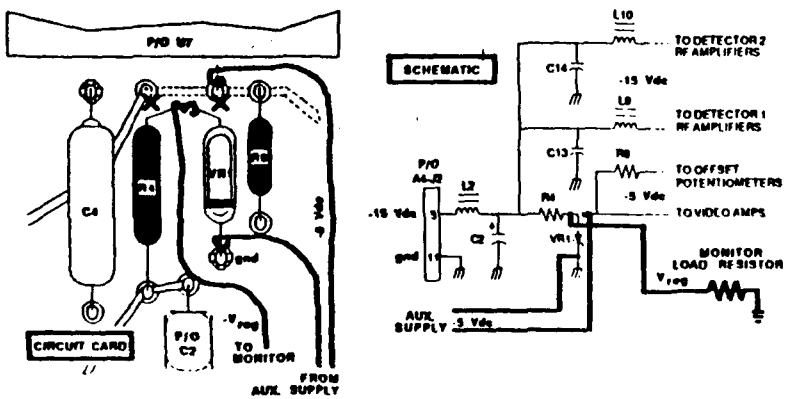
RESISTOR/ZENER DIODE MODIFICATION: At Dwell; For the modified resistor/zener diode subcircuit, record the voltage across the LOAD RESISTOR at this STEP-STRESS Level.

Start TEST: 03:47 (TIME HR:MIN)

Voltage across LOAD RESISTOR: -5.176V (Vdc) (refer to Appendix D; nominally -5 Vdc)

End TEST: 03:48 (TIME HR:MIN)

DETAILS: A4 DETECTOR CIRCUIT CARD MODIFICATION
FOR AUX. CONSTANT -5 Vdc SUPPLY
AND R4/VR1 MONITORING



FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

STEP-STRESS TEST LEVEL 0

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. # 993 FINAL

03/13/92 @ 04:00

Power at J5 is 10.7 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J5 is 10.7 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.3 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.1 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.2 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.5 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.6 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.4 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.6 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.8 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.9 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.8 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.7 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J5 is 12.8 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.9 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.7 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.4 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.1 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.5 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.3 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.2 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J5 is 11.0 dBm @ 921.0 MHz (Spec=+9dBm minimum).

J5

Detector 10133/J2 is Disconnected for this test

FAIL DATA (if any) of Power Output requirements will be printed between the starred borders.

****

STEP-STRESS TEST LEVEL 0

FULL PRINT-OUT OF Power Output and Frequency [redacted] Ser. #993 FINAL

03/13/92 @ 04:09

Power at J12 is 10.5 dBm @ 684.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.0 dBm @ 687.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.3 dBm @ 690.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.5 dBm @ 693.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.4 dBm @ 696.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.4 dBm @ 699.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.7 dBm @ 702.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.6 dBm @ 705.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.8 dBm @ 708.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.8 dBm @ 711.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.8 dBm @ 714.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.8 dBm @ 717.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.7 dBm @ 720.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.8 dBm @ 723.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 726.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 729.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 732.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 735.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 738.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 741.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 744.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.2 dBm @ 747.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 750.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.4 dBm @ 753.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.4 dBm @ 756.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 759.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 762.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.2 dBm @ 765.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 768.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 771.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.2 dBm @ 774.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 777.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.2 dBm @ 825.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.2 dBm @ 828.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.3 dBm @ 831.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 834.0 MHz (Spec=+9dBm minimum).
Power at J12 is 12.1 dBm @ 837.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.8 dBm @ 882.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.7 dBm @ 885.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.6 dBm @ 888.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.7 dBm @ 891.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.8 dBm @ 894.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.7 dBm @ 897.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.6 dBm @ 900.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.6 dBm @ 903.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.5 dBm @ 906.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.5 dBm @ 909.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.5 dBm @ 912.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.4 dBm @ 915.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.4 dBm @ 918.0 MHz (Spec=+9dBm minimum).
Power at J12 is 11.2 dBm @ 921.0 MHz (Spec=+9dBm minimum).

J12

Detector connected 10/13/J2 disconnected for this test

TEST EQUIPMENT & CALIBRATION LOG

Maintain Log for testing conducted 03/03/92 through [redacted] Same through 03/13/92

Item	DESCRIPTION	Manuf. & Part No.	ID NUMBER	LAST CAL*	CAL* DUE	Rem Notes
01	T/R Test Station	HAC; SPECIAL	E-A15223		NCR	G-132043
02	Control Panel	HAC; SPECIAL	G-132290		NCR	
03	Signal Generator	HP; 8660C	G-128061	07-17-91	01-13-93	
04	Auxiliary Section	HP; 86631B	G-128062		NCR	7% ITEM 03
05	RF Section	HP; 86603A	G-128063	12-17-91	01-13-93	7% ITEM 03
06	Spectrum Analyzer	HP; 8568A w/ Opt E16	G-132082	12-11-91	10-30-92	
07	FET Probe	HP; 1120A	G-132055	12-14-90	04-30-92	PER CAL
08	Power Meter	HP; 436A	G-128036	06-18-91	11-24-92	"
09	Power Sensor	HP; 8482A	G-128059	09-09-91	10-21-92	"
10	Oscilloscope	HP; 1980B	G-132044	09-24-91	08-11-92	
11	Digital Multimeter	SystronDonner; 7344A	G-127998	06-06-91	08-18-92	
12	Digital Multimeter	HP; 3478A	H-A53624	09-06-91	06-25-92	
13	Power Splitter	MiniCkts; ZFSC-2-5	No ID ✓		NCR	
14	Power Splitter	MiniCkts; ZFSC-2-5	No ID ✓		NCR	
15	Reg. Power Supply	Lambda; LP-531-FM	G-132292		NCR	+15V
16	Reg. Power Supply	Lambda; LP-531-FM	"		NCR	-15V
17	Reg. Power Supply	Lambda; LP-530-FM	G-132291		NCR	+5V
18	Reg. Power Supply	Lambda; LP-520-FM	"		NCR	-5V
19	Computer	HP; 9845B	G-128012		NCR	
20	Flex. Disk Memory	HP; 9895A	G-133309		NCR	
21	Signal Generator					
22	Oscilloscope	Tektronix; 2465				
23	Digital Multimeter					
24	Digital Multimeter					
25	Digital Multimeter					
26	Thermal Chamber	Thermotron; S-4 w/Cntl	H-B07567	09-18-91	09 02 92	
27	Data Acqtn Cntl Unit	HP; 3497A	H-428499	11-14-91	07-29-93	
28	Computer	HP; Model 85	H-A64429		NCR	
29	Power Supply, AUX.	HP; 6299A	H-357054		NCR	-5.1V
30	PLOTTER	HP; 7470A	H-512478		NCR	
31	PRINTER	HP; THINKJET	E-A08763		NCR	
32						
33						
34						
35						
36						
37						
38						
39						
40						
41						
42						

*NCR - Non Calibration Required

CALIBRATION ROUTINE PERFORMED 03-02 92; 15.52 PRIOR TO TESTING

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Retain Data for MSN 933 03/12-03/13/92

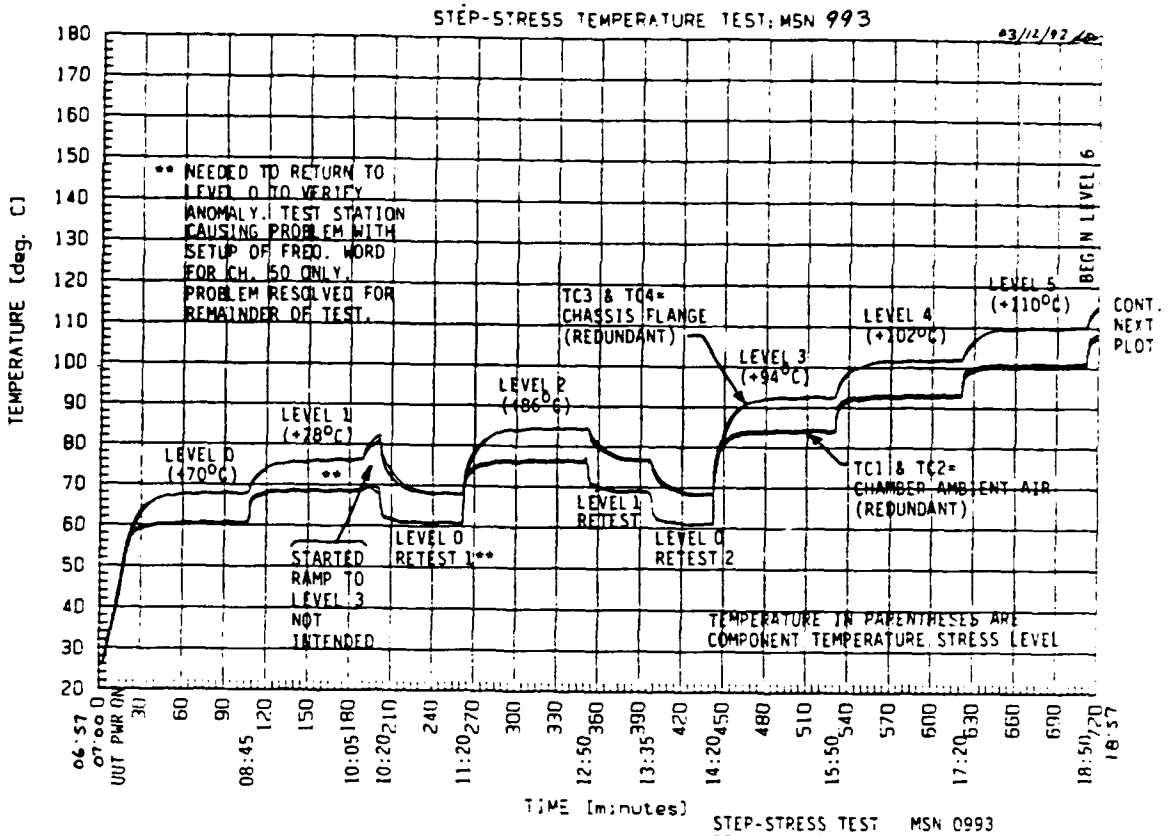
DATE: [redacted] TIME: [redacted]

03/09/92

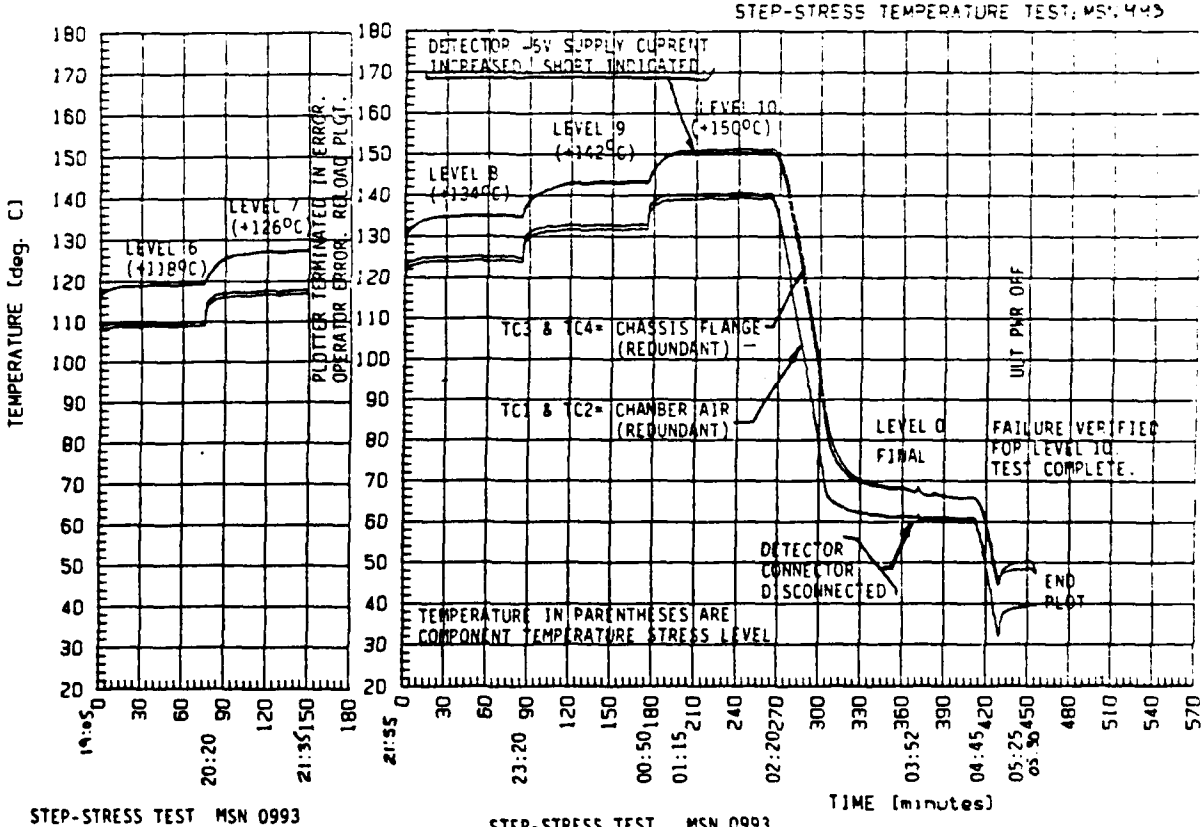
STEP-STRESS CALIBRATION D

```
Synth_ref= 2562650
Freq_mod_ref= 11603700
Sp_clock_output = 0
Phase_lo_output = 1.16
Phase_if_output = 0
Up_dn_conv_lo = 3.44
313.75_lo = -72.8 dBm /314.91116E6MHz
```

Channel	Freq	Dn_conv_output	Synth_lo_output	Hit_sgnl_l_o
50	684	1.17	1.17	2.10
49	687	1.2	1.31	2.07
48	690	1.28	1.4	2.07
47	693	1.33	1.3	2.07
46	696	1.33	1.18	2.03
45	699	1.34	1.23	1.95
44	702	1.38	1.37	1.96
43	705	1.38	1.41	2.01
42	708	1.39	1.35	1.98
41	711	1.42	1.42	1.85
40	714	1.45	1.53	1.82
39	717	1.46	1.53	1.9
38	720	1.42	1.44	1.96
37	723	1.4	1.49	1.92
36	726	1.43	1.71	1.83
35	729	1.44	1.87	1.82
34	732	1.45	1.84	1.86
33	735	1.42	1.69	1.83
32	738	1.42	1.69	1.74
31	741	1.39	1.82	1.79
30	744	1.39	1.83	1.94
29	747	1.41	1.83	1.98
28	750	1.46	1.94	1.81
27	753	1.49	2.1	1.72
26	756	1.49	2.11	1.8
25	759	1.45	1.93	1.86
24	762	1.45	1.86	1.81
23	765	1.48	2.01	1.78
22	768	1.52	2.13	1.85
21	771	1.6	2.12	1.94
20	774	1.68	2.07	1.86
19	777	1.72	2.14	1.74
18	825	1.76	2.27	1.8
17	828	1.74	2.31	1.73
16	831	1.7	2.39	1.68
15	834	1.7	2.33	1.74
14	837	1.76	2.27	1.74
13	882	1.7	2.07	1.55
12	885	1.66	2.02	1.61
11	888	1.7	2.01	1.67
10	891	1.76	2.02	1.6
9	894	1.7	2.07	1.54
8	897	1.68	2.09	1.53
7	900	1.72	2.02	1.54
6	903	1.74	1.91	1.46
5	906	1.64	1.87	1.42
4	909	1.52	1.89	1.49
3	912	1.53	1.86	1.58
2	915	1.61	1.86	1.59
1	918	1.6	1.86	1.51
0	921	1.52	1.95	1.47



STEP-STRESS TEST MSN 0993
BEGIN TESTING: 03/12/92
PLOT 1 OF 3



STEP-STRESS TEST MSN 0993
CONT'D TEST 03/12/92
PLOT 2 OF 3

STEP-STRESS TEST MSN 0993
CONTINUED: 03/12/92 THRU 03/13/92
PLOT 3 OF 3

Test Data Cont'd: STEP-STRESS TEST MSN 993 Date: 3-11-92

16:00 hrs: Set UP Thermal Program for upcomming test of MSN 993. TR3 had broken & was replaced. BA

07:00 Turn Pwr on Unit #993 start Prog #1 Int #1
07:45 Start Prog #2 Int #1 Dwell @ 61°C
08:45 Stress level 0 Complete. Ramp to level 1
09:15 Dwell @ 69°C
10:05 Anomally seen on J2 output
10:20 Return back to stress level 0
10:50 Dwell @ 61°C
10:55 No failure found
11:20 Ramp to level 2
11:50 Dwell @ 77
12:40 Anomally seen on J5 output (unlocked)
12:50 Return back to stress level 1
13:20 Dwell @ 69°C
13:35 J5 still unlocked Return to stress level 0
14:05 Dwell @ 61°C
14:20 J5 output ok. No failures Ramp to stress level 3
14:50 Dwell @ 85°C
15:50 Completed LEVEL 3. Ramp to LEVEL 4 (Set @ +94°C). AB Mueller 02/06
16:20 Start LEVEL 4 Dwell
17:20 Completed LEVEL 4. Ramp to LEVEL 5 (Set @ +102°C)
17:50 Start LEVEL 5 Dwell
18:50 Completed LEVEL 5. Ramp to LEVEL 6 (Set @ +111°C)

Data Recorder: [signature]

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Test Data Cont'd: STEP-STRESS TEST MSN 993 Date: 03/12/92

18:57 - PLOT 1, DATA TAPE #1 complete 720 scans. Begin Reloading for PLOT 2, DATA TAPE #2
19:05 - PLOT 2, DATA TAPE #2 Begins 1st scan
19:20 - Start LEVEL 6 Dwell
20:20 - Completed LEVEL 6. Ramp to LEVEL 7 (Set @ +119°C)
20:50 Start LEVEL 7 Dwell
21:35 - * Bumped pen when observing plotter causing voltage error with plotter. Could not continue plot.
21:41 - Restart by LOAD "XXXLOG" RS Start Plot #3 DISK #3.
21:50 - Completed LEVEL 7. Ramp to LEVEL 8 (Set @ +132°C)
21:55 - * PLOT #3 Started DISK #3
22:20 - Start LEVEL 8 Dwell.
23:20 - Completed LEVEL 8. Ramp to LEVEL 9 (Set @ +145°C)
23:50 - Start LEVEL 9 Dwell.
03/13/92
00:50 - Complete. LEVEL 9. Ramp to LEVEL 10 (Set @ +153°C)
01:15 - 25-minutes into Ramp & stabilization -5V Supply Voltage went from -7.00V to -8.91V and 2.91 Amps. Continue through LEVEL 10
01:20 - Start LEVEL 10 Dwell FAILURE IN PROGRESS
02:05 - Anomaly with Synths #1 & #2 has been seen before with MSN 0815. Can Return to ZERO Ø for Analysis of -5V FAILURE
02:20 - LEVEL 10 Complete. Return to LEVEL Ø FINAL
02:35 - Disconnected Detector J3 at station 101J3 to allow documenting of Supply Voltages.
02:55 - Connector 101J3 reconnected for stabilization period
03:45 - Begin Dwell @ LEVEL Ø FINAL
03:47 - Failure @ Detector -5V Supply line Verified

Data Recorder: [signature] 02/16

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Test Data Cont'd: STEP-STRESS TEST MSN 993 Date: 03/13/92

03:52 Disconnect DETECTOR 10113 TO PERFORM SYNTHESIZER TESTING. SYNTH'S PASS

04:11 TESTS COMPLETE. DETECTOR 10113 TO REMAIN DISCONNECTED TO COMPLETION.

04:45 LEVEL OF FINAL DWELL PERIOD completed Ramp to Room Ambient.

05:25 UUT POWER OFF

05:30 END PLOT #3, TAPE #3. TESTING COMPLETE

Data Prepared By: ADM 92466

2-1

HUGHES

HUGHES AIRCRAFT COMPANY

STEP-STRESS (1 PROJECT NAME)

TROUBLE & FAILURE REPORT

NO. Z7390

FAIL CLASS	TEST TYPE	TEST ENV	FAIL CAUSE	RELEV

RAW CODE

S-ST CODE

2 THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE ☒ FAILURE

ORIGINATOR

3 SYSTEM SUBSYSTEM NAME: R/T MODULE | P/N: test no -103 | S/N: 993

4 TIMER COUNTER READING: TIME: 0:15 (HOURS) CYCLES: 1,390 LEVEL 10 | 5 DATE: 03 (MO) 13 (DAY) 92 (YR)

35 REFERENCES

6 REPORTING FACILITY: STEP-STRESS TEST c/o S.D. MUELLER

7 REPORTED BY: S.D. Mueller (92665) 03/13/92 | ORG CODE: V1A 72 30

OPERATING LOG NO

8 TROUBLE FAILURE OBSERVED WAS (TEST CONDITIONS SYMPTOMS SEVERITY, ETC. INCLUDING "IS" AND "SHOULD BE" DATA)

-5V SUPPLY SHORT AT DETECTOR OCCURRED 25 MINUTES (OF 30 MINUTES TOTAL) INTO RAMP AND STABILIZATION AT LEVEL 10, PRIOR TO DWELL. THERMAL & VOLTAGE CONDITIONS REMAINED UNCHANGED AT TIME OF FAILURE AND BEGINNING OF DWELL (+140°C CHAMBER, +151°C FLANGE, +150 AVG COMPONENT, ±7V, ±18V). AT FAILURE 28 Q-BIT DUTY CYCLE & OUTPUT CEASED TO EXIST, GOING TO HIGH STATE ONLY. -5V SUPPLY (S/B -7.00V) WENT TO -0.9V @ 2.9 AMPS. NO VISUAL INSPECTION AT THIS TIME. REF ALSO TEST DATA SHEETS (NOT ATTACHED). DOT PROVIDED HERE.

FOR CONTINUATION USED ☐

9 TROUBLE FAILURE OCCURRED DURING (A) ☒ ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE FLIGHT OR CURSORY CHECK

10 ACTION TAKEN TO CORRECT TROUBLE FAILURE (A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 - 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 - 20)

11 ITEM REPLACED NAME	P/N	S/N	12 ITEM INSTALLED NAME	P/N	S/N	13 DISPOSITION OF REPLACED ITEM

VERIFICATION

14 WERE OTHER TROUBLES FAILURES, NOT RELATED TO ORIGINAL NOTED? (A) ☐ NO (B) ☐ YES LIST ON NEW TFR - TFR NO _____

15 WAS REPORTED TROUBLE FAILURE VERIFIED? (A) ☐ YES (B) ☐ NO (CHECK 'B' AND EXPLAIN)

16 FAILED ITEM NAME	P/N	S/N	REF DESIG	MANUFACTURER

17 NEXT HIGHER ASSY NAME	P/N	S/N	REF DESIG	MANUFACTURER

18 (A) ☐ REWORK REQUIRED IS (B) ☐ REWORK IS NOT REQUIRED BECAUSE

19 VENDOR REWORK ANALYSIS IS REQUIRED ☐ ITP _____ CAR _____

20 DISPOSITION OF ITEM IF NOT REWORKED

21 AUTHORIZATION BY | ORG CODE | DATE

REWORK & RETEST

22 LIST BELOW ALL PARTS REPLACED REPAIRED OR ADJUSTED

A CIRCUIT SYMBOL	B PART NUMBER	C S/N	D MANUFACTURER	E DEFECT	F REWORK ACTION TAKEN	G RECEIVING INSP NO	H APPROVED BASELINE YES	H APPROVED BASELINE NO	PRI FAIL

FOR ECP USE

23 OTHER REWORK ACTION

24 REWORKED BY | ORG CODE | 25 RETESTED BY | ORG CODE | 26 RETEST RESULTS APPROVAL | DATE

27 RETEST RESULTS REPAIRED ITEM IS ACCEPTABLE FOR ☐ UNRESTRICTED USE ☐ RESTRICTED USE ☐ NOT ACCEPTABLE EXPLAIN IN BLOCK 30

28 DISPOSITION OF ITEM AFTER RETEST | 29 G O C

ENGINE

30 CAUSE OF FAILURE - COMMENTS (IF ANALYSIS NOT PERFORMED EXPLAIN)

31 BASIC CAUSE OF TROUBLE FAILURE (SELECT FROM BLOCK 1 ON REVERSE SIDE)

32 SIGNATURE | ORG CODE | DATE

CORRECTIVE ENGINEERING ACTION TAKEN IF NONE JUSTIFY - CONCLUSIONS

REF DOCUMENT IMPLEMENTING CORRECTIVE ACTION ED ECR ETC IS NO.

34 SIGNATURE | ORG CODE | DATE

11020 CS MAR 66

USE TFR CONTINUATION SHEET IF ADDITIONAL SPACE IS NEEDED

FOR RELIABILITY ANALYSIS AND FOLLOW UP SEE REVERSE SIDE OF COPY 4

Z7390

THERMAL TEST EQUIPMENT OPERATING PROCEDURE

TEMPERATURE MONITORING OF
STEP-STRESS RELIABILITY UUT's
(February 27 1992)

THERMAL TEST EQUIPMENT OPERATING PROCEDURE

TEMPERATURE MONITORING OF
STEP-STRESS RELIABILITY UUT's
(February 27 1992)

INTRODUCTION

The following procedure is a set of instructions that will enable the test technician or test engineer to operate the thermal data logger and computer. Its intent is to be "cook-book" and, if followed carefully, successful operation will be realized. However, the software is not very "user-friendly" and once a mistake occurs, the procedure will have to be repeated. If any problems occur during the test or you have any questions, please contact myself or J. DeBellis.

B. Armstrong	732-3071
J. DeBellis	732-7743
Laboratory	732-4987

TEST EQUIPMENT

The following equipment constitutes the Thermal Data Acquisition System;

A) HP No. 3497 Data Logger
B) HP No. 85 Computer
C) HP Think-Jet Printer
D) HP 7470A Plotter
E) "Logger" program cartridge (3M DC-1000, 20MB-type)
F) Blank data cartridges (1 per each 12 hr. period)
G) Type "T" (copper/constantan) high temperature insulated thermocouples

Included are:
1) Loading Procedure
2) Re-Loading Procedure
3) Layout of HP-85 computer keyboard
4) Copies of program pages off HP-85 screen
5) Copy of Formated Temperature Plot

LOADING PROCEDURE

1. Place either "[redacted]LOG1" or "[redacted]LOG2" tape cartridge into HP85 drive.

2. Type LOAD "[redacted]LOG". Press <ENDLINE> key.
(Screen will be blank for 1-2 min.'s while program is loading).

3. When screen cursor returns, press <RUN> key. (Page 1 will now appear on the screen).

4. Press <SET> key (K3). (Page 2 will appear on the screen).

5. Press <GET> key (K3).

6A. Press <RET> key (K8) to return to Page 1.
6B. If MSN information needs to be changed, press <COM> key (K2). Enter the new information then press <ENDLINE> to get back to Page 1.

7. Press <RUN> key (K4). (Page 3 will appear).

8. If computer clock needs to be reset, press <TIME> key (K1) and verify that the real time is correct. If not, press <ENTER> key (K1) and input new time. Then press <SET> (K8) to set new time and to return to Page 3.

9. Remove "[redacted]LOG1" OR "[redacted]LOG2" program cartridge and replace it with a new blank data cartridge.

10. Press <START> key (K4).
Enter **720** and <ENDLINE> to "Number of times to run exp 01".
(The temperature will be monitored for 720 minutes).

11. Enter **5** and <ENDLINE> to "Scans per print out". (The PRINTER will print every 5 minutes).

At this point, the computer will now start to format the data tape. If the tape was initially unformatted, this process will take 5-10 minutes. If the data tape has been previously formated, an error will initially be flagged (see attached example). Simply press the continue <CONT> key and the computer will begin to re-format the tape. This may take 30-60 seconds.

12. Upon completion of of the formating, the plotter will now graph the temperature plot including a header. See attached example.

13. Enter **4** and <ENDLINE> to "No. of channels you wish to plot".

14. Enter:

    1 and <ENDLINE> to "Channel 1 is...". (Chamber)
    2 and <ENDLINE> to "Channel 2 is...". (Chamber,Red't)
    3 and <ENDLINE> to "Channel 3 is...". (Flange)
    4 and <ENDLINE> to "Channel 4 is...". (Flange, Red't)

You are now set up to:

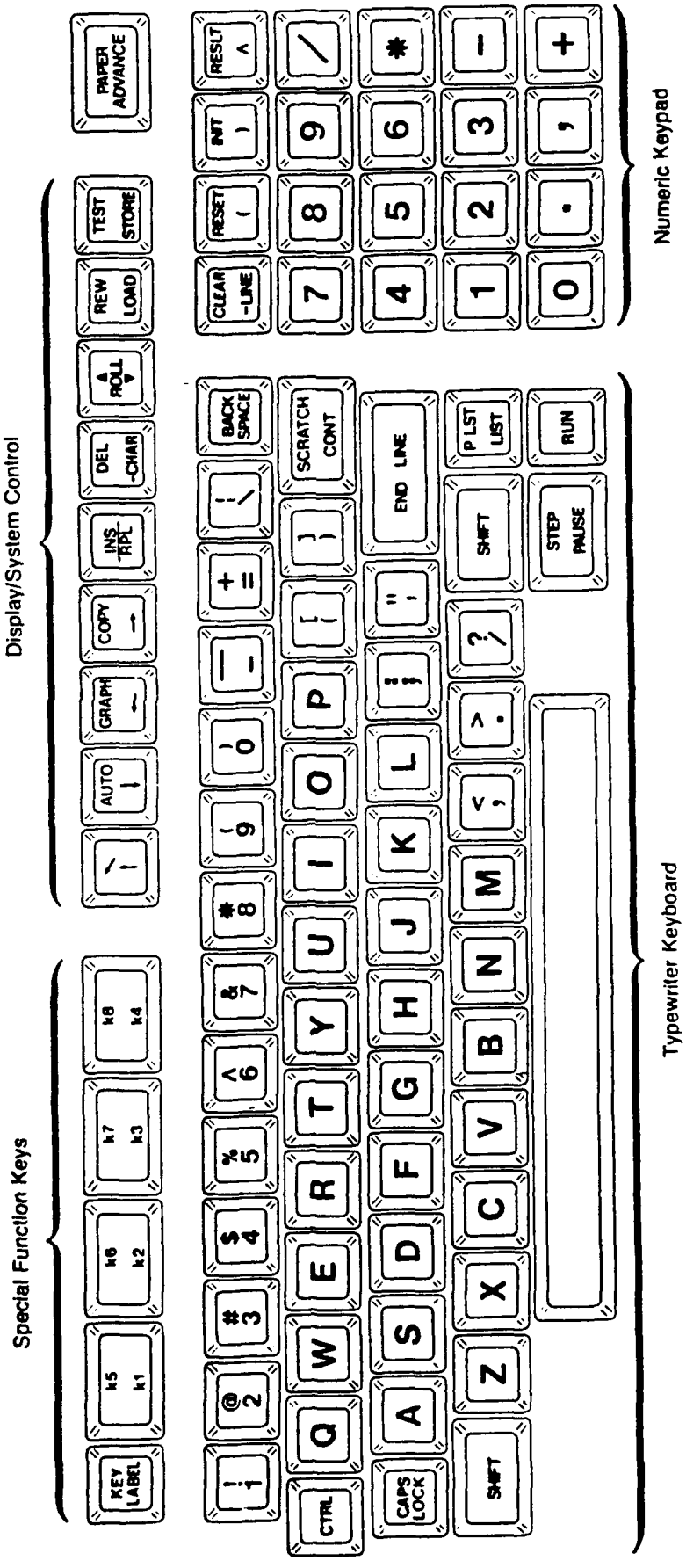
A. Plot temp. data every minute.
B. Store temp. data every minute.
C. Print out temp. data every 5 minutes.
D. Perform these measurements for 12 hours (720 minutes).

RE-LOADING PROCEDURE

1. At end of 12 hours, Page 3 will automatically appear on the HP-85 screen. Exchange plot paper for a fresh sheet. Make sure that there is an adequate supply of print out paper.

2. Remove old data tape and exchange it with "[redacted]LOG1" or "[redacted]LOG2".

3. Go to Step 3 of **"LOADING PROCEDURE"** and repeat the remaining steps.


HP-85 Keyboard
Special Function Keys
Display/System Control
Typewriter Keyboard
Numeric Keypad
KEY LABEL
k5 k1
k6 k2
k7 k3
k8 k4
AUTO
GRAPH
COPY
INS RPL
DEL CHAR
ROLL
REW LOAD
TEST STORE
PAPER ADVANCE
BACK SPACE
SCRATCH CONT
END LINE
P LST LIST
RUN
SHIFT
STEP PAUSE
CAPS LOCK
CTRL
CLEAR -LINE
RESET
INT
RESULT

DATA LOGGER PAGE 1

EXP--set experiment number
COM--comment to be recorded
PRT--print data is ENABLED
REC--record data is ENABLED
SET--setup channels, functions, timing
RUN--log data
REV--review recorded data
END--experiment complete.

PRT	REC	REV	END
EXP	COM	SET	RUN

DATA LOGGER SETUP PAGE 2

ADD---new channels/functions
EDIT--change old chan/func
GET---recall the last setup
SAVE--store this setup
T/I---set timing interval
LIST--print channel setup
RET---return to PAGE 1.

T/I		LIST	RET
ADD	EDIT	GET	SAVE

Mo DAY HRS(GMT) MIN. SEC

Current time is 02:27:08:47:33

ENTER--input new time
SET----return to RUN (PAGE 3)

			SET
ENTER			

DATA LOGGER (RUN) PAGE 3

TIME--set current time
SING--single scan
STEP--channel step mode
START-scan at interval
RET---return to PAGE 1

			RET
TIME	SING	STEP	START

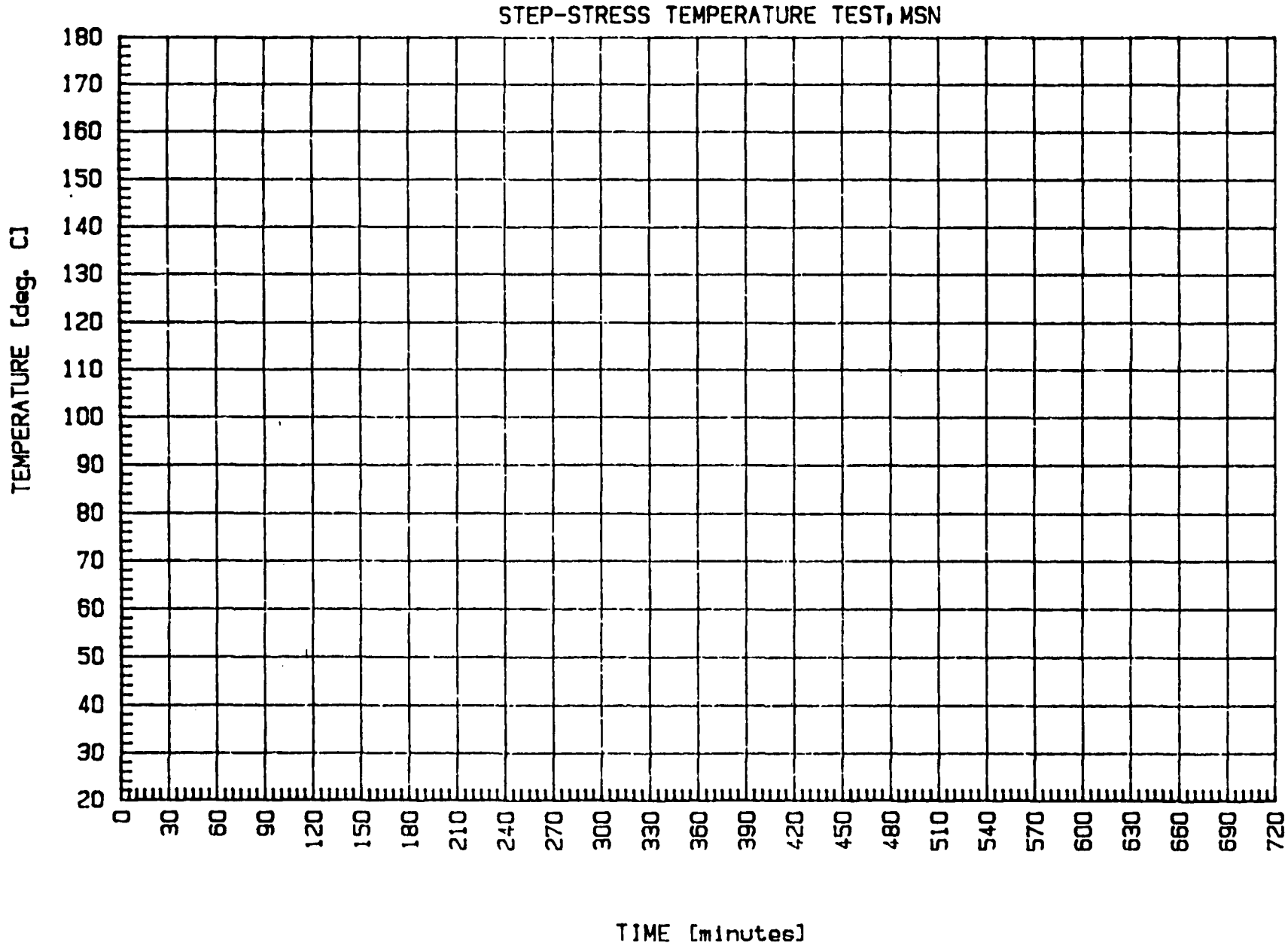
MAKE SURE THIS READS "01", NOT "-1"

Number of times to run (EXP.01)
(1 - 900)
?

ENTER "720", <ENDLINE>

DL error 3
ERRN= 63 ERRL= 3005
Press [CONT] to resume

WILL OCCUR WHEN TRYING TO FORMAT PREVIOUSLY FORMATED DATA TAPE. JUST PRESS [CONT] KEY AND THE TAPE WILL BE FORMATED MUCH QUICKER THAN IF NOT FORMATED ORIGINALLY.


STEP-STRESS TEMPERATURE TEST, MSN
TEMPERATURE [deg. C]
180
170
160
150
140
130
120
110
100
90
80
70
60
50
40
30
20
0
30
60
90
120
150
180
210
240
270
300
330
360
390
420
450
480
510
540
570
600
630
660
690
720
TIME [minutes]

APPENDIX E

Failure Analyses

HUGHES AIRCRAFT COMPANY

INTERDEPARTMENTAL CORRESPONDENCE

TO: Dept ENB
ORG: 1A-72-10

cc: Project Distribution

DATE: 29 May 1992
REF: 92/1A72.30/005

SUBJECT: **Step-Stress Test UUT Failure Analysis**
Production R/T Modules

FROM: S. D. Mueller
BLDG: 600 MAIL STA: G156
EXT: 1-8360 ORG.CODE: 1A-72-30

ABSTRACT: Step-Stress testing per contract F30602-89-D-100/009 was performed on seven production (fielded) configuration Receiver/Transmitter (R/T) modules; UUT serial numbers MSN's 1030, 1023, 1028. 0172, 0815, 1029, and 0993. Of the seven R/T modules, four (4) UUTs are chargeable as FAILURES through LEVEL 10 of the Step-Stress Test. Their serial numbers are MSN 0172, 0815, 1029, and 993. MSN 1030 was failure free through LEVEL 10 (non-chargeable), and was increased to a test LEVEL 11 to provide data useful in validating the selected design limits of the test. The information contained in this engineering notebook (ENB) consists of the Trouble & Failure Reports (TFR), Failure Analysis Data Sheets, and Historical Record Tags (HRT) for each MSN under analysis. The contents herein shall be furnished to the customer upon request.

The contents of this ENB is as follows:

Failure Analysis Notebook	**Unit Under Test: MSN 0172** **Failure at Level 9**	page 02
Failure Analysis Notebook	**Unit Under Test: MSN 0815** **Failure at Level 10**	page 11
Failure Analysis Notebook	**Unit Under Test: MSN 1029** **Failure at Level 7**	page 18
Failure Analysis Notebook	**Unit Under Test: MSN 0993** **Failure at Level 10**	page 29
Failure Analysis Notebook	**Unit Under Test: MSN 1030** **Non-chargeable Level 11**	page 36

The following individuals have contributed photographic services to this ENB:

R. Cantu and K. G. Mohr.

ENB Project Distribution: * Abstract only

R. A. Doctor*	(Dept. Manager)	R. Cantu*	(Product Oper.)
S. R. Burnett*	(Reliability Engineer)	K. G. Mohr*	(FA/DPA Lab)
D. Huch	(Program Manager)		
L. E. James	(Project Manager)		
S. D. Mueller	(Design Engineer)		

STEP-STRESS TEST

FAILURE ANALYSIS NOTEBOOK
Unit Under Test: MSN 0172

FAILURE SUMMARY

FAILURE LEVEL:	LEVEL 9
FAILURE MODE(S):	TANTALUM CAPACITOR, A4-C4, INTERNAL SOLDER FLOW RESULTED IN -5 VOLT SUPPLY LINE SHORT.
AFFECTED PART(S):	A4-C4; P/N M39003-1-2255.

FIXED STEP DWELL TIME:	1 HOUR
FIXED RAMP & STABILIZATION:	30 MINUTES
TOTAL ELAPSED TIME TO FAILURE: (FROM END OF LEVEL 0 DWELL)	12 HOURS: 53 MINUTES
ANOMALY TEST TIME: (INCLUDED IN TOTAL ABOVE)	NONE

HUGHES
HUGHES AIRCRAFT COMPANY

STEP-STRESS TROUBLE & FAILURE REPORT

1. PROJECT NAME

FAIL CLASS	TEST TYPE	TEST ENV	FAIL CAUSE	RELEV

NO. Z7393

FAM CODE | SYST CODE

2. THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE ☒ FAILURE LEVEL 9

ORIGINATOR

3. SYSTEM, SUBSYSTEM NAME	P/N	S/N	4. TIMER COUNTER READINGS	5. DATE	35. REFERENCES
T/R MODULE	part no -103	172	TME: 20:38 ELAPSED HRS	03 04 92	

6. REPORTING FACILITY	7. REPORTED BY	ORG CODE	OPERATING LOG NO
STEP-STRESS TEST C/O MUELLER (SSS 1S2-26)	A. J. Mueller 03/04/92	1A 72.30	

8. TROUBLE, FAILURE OBSERVED WAS: (TEST CONDITIONS, SYMPTOMS, SEVERITY, ETC., INCLUDING "IS" AND "SHOULD BE" DATA) — TFR CONTINUATION USED ☐

LEVEL 9 (+142°C Comp / +133°C CUMBR / ±6.8V & ±17.7V - 5V SUPPLY OF DETECTOR CCA INCREASED TO 2.9 Amps @ -0.9 Volts (typical 97mA @ -6.8V). NO DETECTOR I&Q BIT OUTPUTS HALF WAY THROUGH TEST. (BEGAN @ 20:28; NO OUTPUT @ 20:38). LEVEL 8 & 0 TESTING CONFIRMS IT IS AT DETECTOR. (-5V AUX SUPPLY & R4/VR1 MOD SEEMS UNAFFECTED) SEE TEST DATA SHEETS FOR ADDITIONAL COMMENTS. NO VISUAL PERFORMED AT INITIAL REPORT.

9. TROUBLE/FAILURE OCCURRED DURING (A) ☒ ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE-FLIGHT OR CURSORY CHECK

10. ACTION TAKEN TO CORRECT TROUBLE/FAILURE (A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 - 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 - 29)

11. ITEM REPLACED NAME	P/N	S/N	12. ITEM INSTALLED NAME	P/N	S/N	13. DISPOSITION OF REPLACED ITEM

VERIFICATION

14. WERE OTHER TROUBLES/FAILURES NOT RELATED TO ORIGINAL NOTED? (A) ☒ NO (B) ☐ YES LIST ON NEW TFR - TFR NO _____

15. WAS REPORTED TROUBLE/FAILURE VERIFIED? (A) ☒ YES (B) ☐ NO (CHECK 18 B AND EXPLAIN)

16. FAILED ITEM NAME	P/N	S/N	REF DESG	MANUFACTURER
CAPACITOR, FIXED, TANTALUM	M39003-01-2255	N/A	A4C4	MIL-C-39003/1

17. NEXT HIGHER ASSY NAME	P/N	S/N	REF DESG	MANUFACTURER
DETECTOR CKT CARD ASSY	N/A	0016	A4	05869

18. (A) ☒ REWORK REQUIRED IS (B) ☐ REWORK IS NOT REQUIRED BECAUSE

19. VENDOR REWORK ANALYSIS IS REQUIRED ☐ ITR _____ C.A.R. _____

REMOVE A4C4 FROM CCA (CUT LEADS) & TEST ASSEMBLY. BAG & TAG REMOVED PART. REF HRT=401982. X4 PHOTO TAKEN. A. J. Mueller 03/11/92 (SSS 1S2-26) (TEST)
REPLACE DEFECTIVE PART PRIOR TO SECOND STEPSTRESS TEST RUN IF APPLICABLE.

20. DISPOSITION OF ITEM IF NOT REWORKED | 21. AUTHORIZATION BY | ORG CODE | DATE

REWORK & RETEST

22. LIST BELOW ALL PARTS REPLACED, REPAIRED OR ADJUSTED

(A) CIRCUIT SYMBOL	(B) PART NUMBER	(C) S/N	(D) MANUFACTURER	(E) DEFECT	(F) REWORK ACTION TAKEN	(G) RECEIVING LOT NO	(H) APPROVED PARTS YES	NO	PRI. FAIL
A4C4	M39003-1-2255			INTERNAL SOLDER FLOW	CUT LEADS. REMOVE				

DO NOT USE

23. OTHER REWORK ACTION: RETEST A4 PERFORMANCE ROOM TEMP TO VERIFY A4C4 DEFECTIVE.

24. REWORKED BY	ORG CODE	25. RETESTED BY	ORG CODE	26. RETEST RESULTS APPROVAL	DATE
	1A 72.30	A. J. Mueller	1A 72.30	A. J. Mueller	03/11/92

27. RETEST RESULTS, REPAIRED ITEM IS ACCEPTABLE FOR ☐ UNRESTRICTED USE ☒ RESTRICTED USE ☐ NOT ACCEPTABLE (EXPLAIN IN BLOCK 30)

28. DISPOSITION OF ITEM AFTER RETEST: HOLD FOR 2ND RUN AFTER REPLACEMENT (SSS 1S2-26) (TEST)

NO. Z7393

ENGINEERING

30. CAUSE OF FAILURE - COMMENTS (IF ANALYSIS NOT PERFORMED EXPLAIN)

SHORT CIRCUIT -5V SUPPLY LINE DETECTOR A4 DUE TO INTERNAL SOLDER FLOWING FROM CAPACITOR A4C4. REMOVED (CUT LEADS) OF DEFECTIVE C4 & VERFIED ASSEMBLY PERFORMANCE IS PASSING. PART RATED TO +125°C (DF=4%) & 10Vdc. EXPOSURE AT FAILURE WAS +142°C & -6.8Vdc LEVEL 9.

31. BASIC CAUSE OF TROUBLE/FAILURE (SELECT FROM BLOCK I ON REVERSE SIDE) ENVIRONMENTAL EFFECTS (SSS 1S2-26) (TEST)

32. SIGNATURE A. J. Mueller | ORG CODE 1A 72 30 | DATE 03/11/92

33. CORRECTIVE ENGINEERING ACTION TAKEN (IF NONE, INDICATE CONCLUSIONS) DOCUMENT FOR EVALUATION OF STEP-STRESS SCREEN TEST APPROACH. REF ENB (IDC# 92/1A72.30/005).

REF. DOCUMENT IMPLEMENTING CORRECTIVE ACTION (EO, ECR, ETC.) IS NO. | 34. SIGNATURE [redacted] | ORG CODE | DATE

11020 CS MAR 66

USE TFR CONTINUATION SHEET IF ADDITIONAL SPACE IS NEEDED 03

FOR RELIABILITY ANALYSIS AND FOLLOW UP SEE REVERSE SIDE OF COPY 4

Z73

1

HRI# [illegible]982
MSN [illegible]

HUGHES AIRCRAFT CO.
GROUND SYSTEMS GROUP

1377644/B449141 REF. NO. 401982

MODEL LEVEL

HISTORICAL RECORD TAG

SYST. NOMEN.

PART OR ASSEMBLY NAME: R/T MODULE
PART OR ASSEMBLY NO.: [redacted]-103
I.T.R. CHANGE
PLANNING CHANGE #
DEPT. ORIGINATED
NEXT ASSEMBLY NO.
HAC MFG. SERIAL NO.
EFFECTIVE AMENDING DOCUMENTS: 4326 LTR 22000
W/O NO.
SERIAL NO.: 172

ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
		7/18/91	Fails FIT output J4 J5 Locks up at 838MHz 5B 921MHz for mode 4.	
	(GSG 95196 TEST)	7/20/91	T00/1/A2 J4 & J5 fail Synth Freq sweep test	(GSG 95196 TEST) 10/14/91
		7/20/91	T02/1/A4 Passed Detector Sensitivity test.	7/20/91
		9/20/91	T00/1/A3 Passed Synth Tests.	9/20/91
	(GSG 95196 TEST)	10/7/91	T01/1/A2/Q3/4192800-206 Band C is internal leakage	
		10/14/91	T00 Syn/Det functional test complete	10/14/91
		10/25/91	Complete 6 Cycle Temp Screen	
		10/31/91	Post Temp functional test completed	10/31/91

FORM 29-4932-GS REV. 11-90

CONT. OTHER SIDE

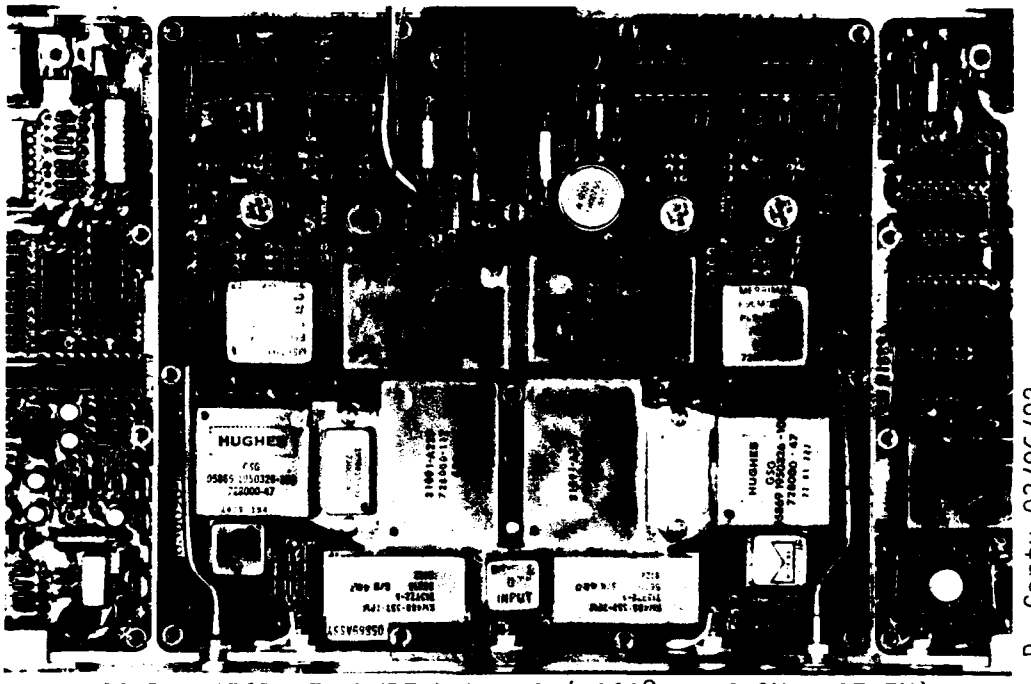
12/2 Visual Inspection after Step-Stress Test [illegible] 12/4/91

ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
ENGR	NOTE		UUT STEP-STRESS TESTED 03/04/92 THRU 03/05/92 TO LEVEL 9 AND INCURRED FAILURE. -5V SUPPLY OF DETECTOR INCREASED TO 2.9A @ -0.9V. NO I&Q OUTPUTS. SEE TFR# Z7393. REFERENCE TEST PLAN CDRL# J003-001 OF F30602-89-D-0100/009.	(GSG 92466 TEST) 03/11/92
		03/9/92	Sent to FA for X-photo of A4C4 solder flow	03/11/92
	(GSG 92466 TEST)	03/11/92	Cut leads of capacitor, tantalum A4C4 after verifying short with ohmmeter. Short on -5V line removed with A4C4 out of circuit. Retested Detector A4 performance (Supply current, I-&-Q-bits) at room temp. TS & PASS limits. FAILURE CONFIRMED. Bad & Tag'd Part.	(GSG 92466 TEST) 03/11/92
	(GSG 92466 TEST)	03/11/92	DR Replace A4C4 P/N M39003-01-2255 & verify Detector Alignment prior to 2nd Step-Stress Test run.	

04

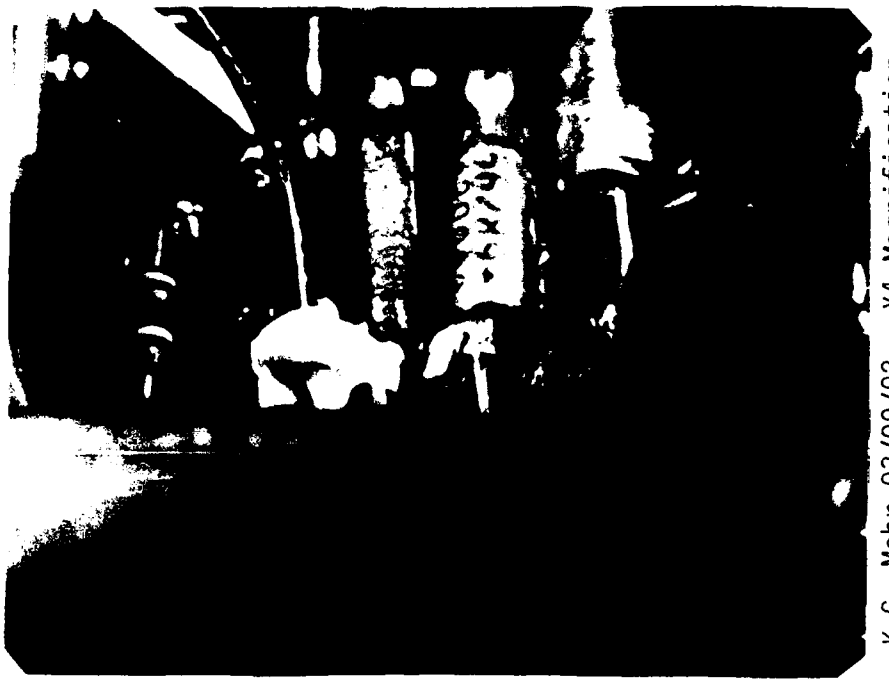
FAILURE ANALYSIS DATA SHEET
STEP – STRESS TEST ATTACHMENT 1 of 6

MSN 0172 ASSY A4
ENGR D. Mueller DATE 03/92



R. Cantu 03/06/92

A4 DETECTOR; FAILURE LEVEL 9 (+142°C, ±6.8V, ±17.7V)



K.G. Mohr 03/09/92 X4 Magnification

A4-C4 TANTALUM CAPACITOR FAILURE;
SOLDER FLOW RESULTING IN -5V SUPPLY SHORT

FAILURE ANALYSIS DATA SHEET | MSN 0172 ASSY A2, A3, A4
STEP – STRESS TEST ATTACHMENT 2 of 6 | ENGR [signature] DATE 03/06/92

TFR# Z7393; HRT# 401982

VISUAL ASSEMBLY INSPECTION NOTES:

A2 SYNTHESIZER (S/N 1987) See Attachment detail.

1 The PWB is an older board and uses green solder mask which is covered with conformal coating. The surface of the PWB is dirty throughout. This condition existed prior to Step-Stress testing.

2 Stresses to LEVEL 9 has only slightly yellowed conformal coating throughout. One component, U11 of this card, has the darkest discoloring of the three cards. U11 is a medium caramel brown after Stress-Step testing. The area around Q4 through Q6 and Q9, show some darkening also.

3 Deep test probe marks found at components R51 thru R53, and C23. These marks were present prior to Step-Stress testing.

4 Cracked solder found at C9 tantalum capacitor, positive lead.

A3 SYNTHESIZER (S/N 1984) See Attachment detail.

5 Over most of PWB conformal coating is uniform. The exception is the board area between U11 and the chassis nearest J11. In this area the conformal coating is not uniform, probably due to touch-up; and the surfaces are dirty. This condition existed prior to Step-Stress testing.

6 Stresses to LEVEL 9 has only slightly yellowed conformal coating throughout.

7 Deep test probe marks found at components CR1 through CR4, CR7 and CR8, R32, R40 and R41. These marks were present prior to Step-Stress testing.

A4 DUAL DETECTOR (S/N 0016) See Attachment detail.

8 PWB is older board and is covered in green solder mask. Conformal coating has been applied in a light coat. Board surfaces are dirty throughout. Condition existed prior to Step-Stress test.

9 Stresses to LEVEL 9 have only slightly discolored conformal coating. Coating has slightly yellowed.

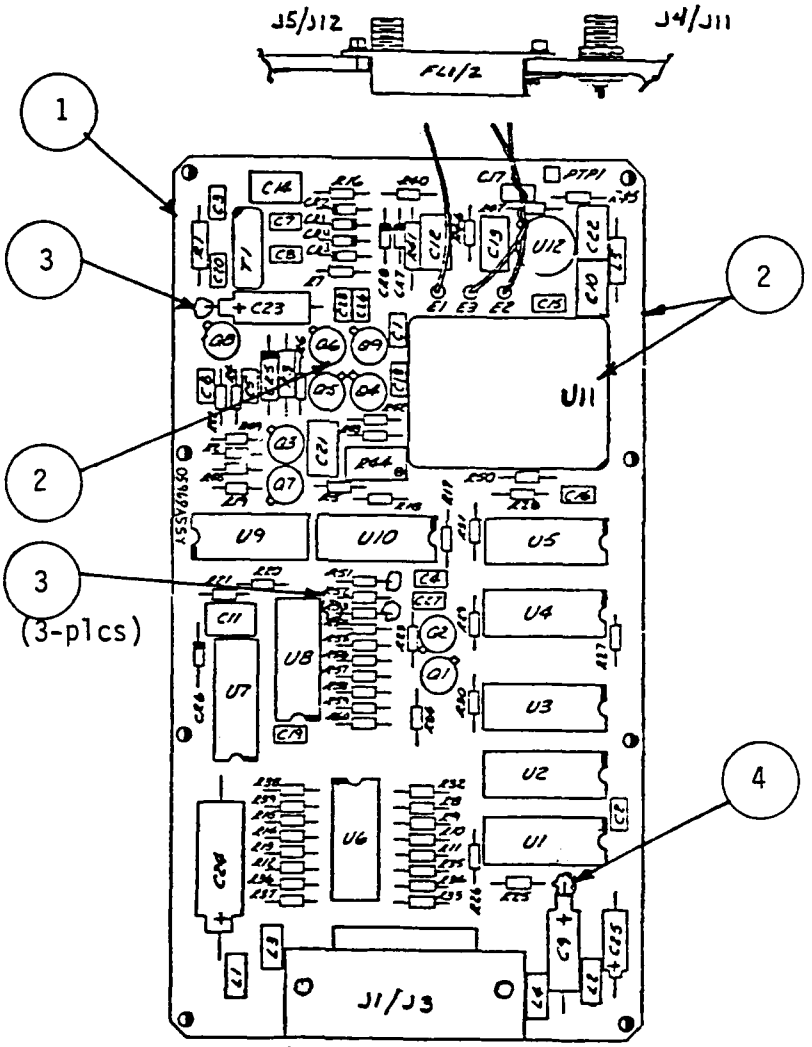
10 Excessive test probe marks found at junctions of R50 and C34, R44 and C33, R33 and C31, and R34 and C32. Existed prior to testing.

11 Unattached solder ball in vicinity of R4 and C2.

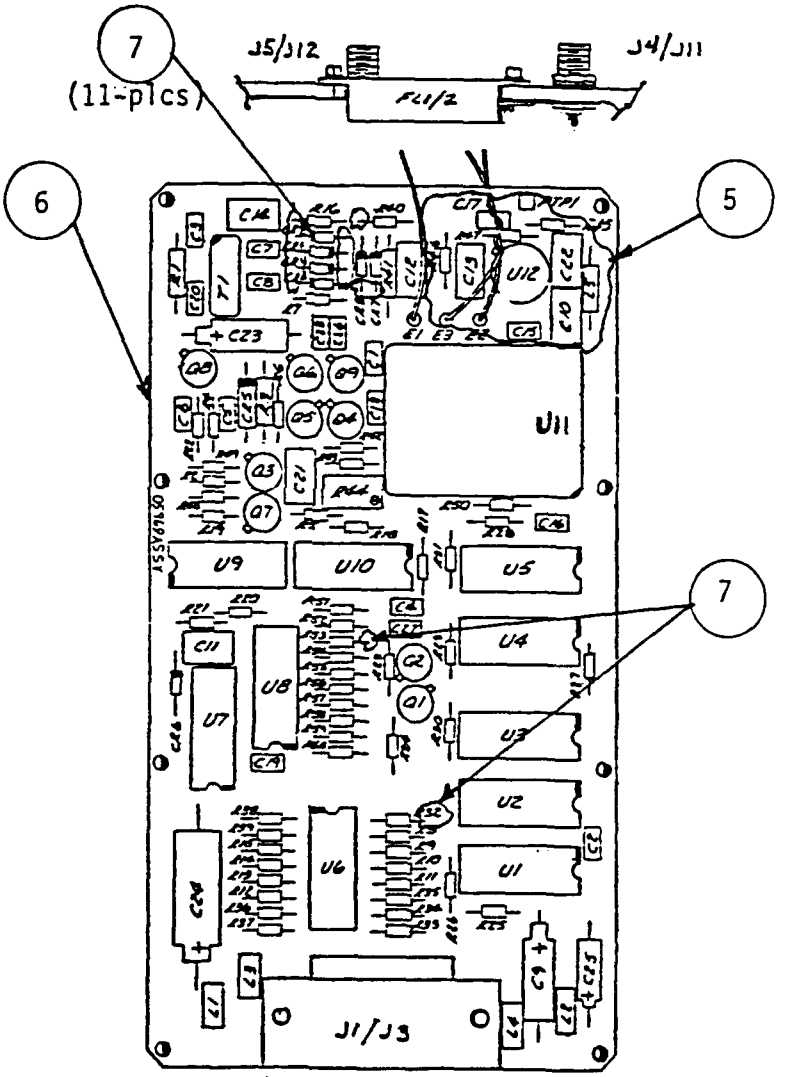
12 Solder ball formed at positive terminal of C4. Solder flowed from within case and continues to PWB surface. Small area of contact is made with R4 body. The conformal coating on C4 is darker than other tantalum capacitors and is a light caramel brown in color.

13 body of R4 has changed from black overall to show some patches of ashen grey from heat. Diode VR1 is glass encapsulated and appears unaffected.

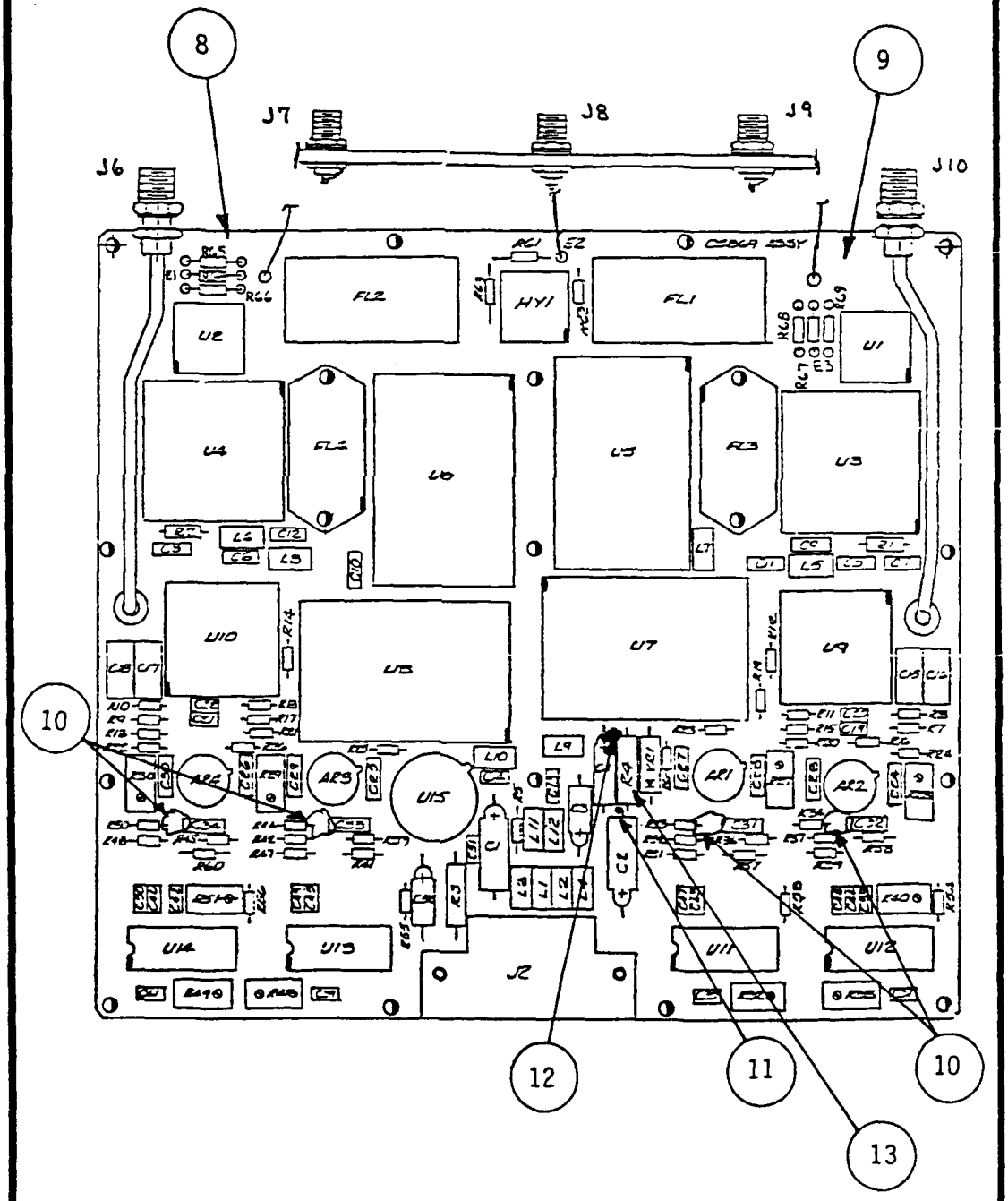
FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 3 of 6	MSN 0172 ASSY A2 (1987) ENGR [signature] DATE 03/06/92



FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 4 of 6	MSN 0172 ASSY A3 (1984) ENGR [signature] DATE 03/06/92



FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 5 of 6	MSN 0172 ASSY A4 (0016) ENGR L.D. Mueller DATE 03/06/92



FAILURE ANALYSIS DATA SHEET

ATTACHMENT 6 of 6

UUT Serial Number (enter MSN): 0172
HRT# 401982
Analysis Date: 03/11/92
Engineer: (Name & stamp below) A.D. Mueller
Test Conducted at Room Temperature
SPECIAL CONDITIONS: Removed supply filter capacitor A4-C4 from circuit -5V line. Capacitor was shorted to ground. Repeat testing. Data below:

DETECTOR VOLTAGE SETTINGS:

Supply Voltages: + 5 Volts dc: +5.00 (Vdc) - 5 Volts dc: -5.00 (Vdc)

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.00 (Vdc)

Aux. - 5 Volt Setting: -5.1075 (Vdc) R_{LOAD} Voltage: -5.344 (Vdc)

DETECTOR CURRENT MEASUREMENTS:

UUT Currents: + 5 Volts dc: 132.8 (mA) - 5 Volts dc: 45.1 (mA)

+15 Volts dc: 73.9 (mA) -15 Volts dc: 312.4 (mA)

DETECTOR DIGITAL OUTPUT MEASUREMENTS:

Rcv Sig Input	I & Q -Bits	DETECTOR 1 t (usec) T (usec)	DETECTOR 1 Duty Cycle (percent)	DETECTOR 2 t (usec) T (usec)	DETECTOR 2 Duty Cycle (percent)	COMMENTS
Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm						
0 dBm	I > 0	4.68/9.60	48.8	4.80/9.60	50.0	Noise & jitter increased slightly with removal of C4 capacitor for test.
	I > Q	"	48.8	"	50.0	
	I + Q > 0	4.80/9.60	50.0	"	50.0	
	Q > 0	4.68/9.60	48.8	4.68/9.60	48.8	
-75 dBm	I > 0	4.92/9.60	51.2	4.80/9.60	50.0	8div @ 1.20μsec)
	I > Q	4.80/9.60	50.0	"	50.0	
	I + Q > 0	"	50.0	"	50.0	
	Q > 0	"	50.0	4.68/9.60	48.8	
Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm						
0 dBm	I > 0	~~4.68~~ 4.68/9.60	48.8	4.80/9.60	50.0	
	I > Q	4.80/9.60	50.0	"	50.0	
	I + Q > 0	"	50.0	"	50.0	
	Q > 0	4.68/9.60	48.8	4.68/9.60	48.8	
-75 dBm	I > 0	4.80/9.60	50.0	4.80/9.60	50.0	
	I > Q	"	50.0	"	50.0	
	I + Q > 0	"	50.0	"	50.0	
	Q > 0	4.68/9.60	48.8	"	50.0	

STEP-STRESS TEST

FAILURE ANALYSIS NOTEBOOK
Unit Under Test: MSN 0815

FAILURE SUMMARY

FAILURE LEVEL:	LEVEL 10
FAILURE MODE(S):	TANTALUM CAPACITOR, A4-C4, INTERNAL SOLDER FLOW RESULTED IN -5 VOLT SUPPLY LINE SHORT.
AFFECTED PART(S):	A4-C4; P/N M39003-1-2255.

FIXED STEP DWELL TIME:	1 HOUR
FIXED RAMP & STABILIZATION:	30 MINUTES
TOTAL ELAPSED TIME TO FAILURE: (FROM END OF LEVEL 0 DWELL)	14 HOURS: 10 MINUTES
ANOMALY TEST TIME: (INCLUDED IN TOTAL ABOVE)	NONE

HUGHES
HUGHES AIRCRAFT COMPANY

STEP-STRESS
1 PROJECT NAME

TROUBLE & FAILURE REPORT

FAIL CLASS	TEST TYPE	TEST ENV.	FAIL CAUSE	RELEV

FAM CODE | SYST CODE

NO. Z 7387

2 THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE ☒ FAILURE

ORIGINATOR

3 SYSTEM, SUBSYSTEM NAME	P N	S N	4 TIMER COUNTER READINGS	5 DATE FAILED	35 REFERENCES
R/T MODULE	part no-103	615	TIME 23.25 LEVEL CLOSED VS 10 HOURS EXCESS	03 MO 05 DAY 92 YR	

6 REPORTING FACILITY	7 REPORTED BY	ORG CODE	OPERATING LOG NO
STEP-STRESS TEST c/o S.D. MUELLER	Steven D. Mueller 3/06/92	1A 72 30	

8 TROUBLE/FAILURE OBSERVED WAS: (TEST CONDITIONS SYMPTOMS SEVERITY ETC., INCLUDING "IS" AND "SHOULD BE" DATA) — TFR CONTINUATION USED ☐

AT LEVEL 10, 10-MIN INTO DWELL, DETECTOR CAUSED -5 VOLT SUPPLY TO DRAW 2.93 AMPS AND VOLTAGE TO DROP TO -6.89 VDC (S/B -7.00 VDC ; 43 mA HIGHER). OBSERVED WHEN I&D BITS LOST ANY DUTY CYCLE AND WENT TO +5 VOLT RAIL. R4/VR1 MODIFICATION FOR TEST SEEMS UNAFFECTED BY FAILURE. UUT WAS AT +140.6°C CHAMBER AIR, +149.5°C FLANGE & +150°C typical COMPONENT AIR TEMP. FAILURE RETESTED AT LEVEL 9 & LEVEL 0 FINAL. SYNTHESIZER I&C ARE UNAFFECTED. NO VISUAL INSPECTION MADE AT THIS TIME.

9 TROUBLE/FAILURE OCCURRED DURING	10 ACTION TAKEN TO CORRECT TROUBLE/FAILURE
(A) ☒ ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE-FLIGHT OR CURSORY CHECK	(A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 - 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 - 29)

11 ITEM REPLACED NAME	P N	S N	12 ITEM INSTALLED NAME	P N	S N	13 DISPOSITION OF REPLACED ITEM

VERIFICATION

14 WERE OTHER TROUBLES/FAILURES, NOT RELATED TO ORIGINAL NOTED? (A) ☒ NO (B) ☐ YES LIST ON NEW TFR - TFR NO. _____

15 WAS REPORTED TROUBLE/FAILURE VERIFIED? (A) ☒ YES (B) ☐ NO (CHECK 18 (B) AND EXPLAIN)

16 FAILED ITEM NAME	P N	S N	REF DESIG	MANUFACTURER
CAPACITOR, FIXED, TANTALUM	M39003-01-2255	N/A	A4C4	MIL-C-39003/1

17 NEXT HIGHER ASSY: NAME	P N	S N	REF DESIG	MANUFACTURER
DETECTOR CKT CARD ASSY	N/A	0553	A4	05869

18 (A) ☒ REWORK REQUIRED IS (B) ☐ REWORK IS NOT REQUIRED BECAUSE

19 VENDOR REWORK ANALYSIS IS REQUIRED ☐ TFR _____ C.A.R. _____

REMOVE A4C4 FROM CCA (CUT LEADS) & TEST ASSEMBLY.

BAG & TAG REMOVED PART. REF HRT# 401986. X4 PHOTO TAKEN. [signature] 03/11/92

REPLACE DEFECTIVE PART PRIOR TO ADDITIONAL STEP-STRESS TEST RUN IF APPLICABLE.

20 DISPOSITION OF ITEM IF NOT REWORKED | 21 AUTHORIZATION BY | ORG CODE | DATE

REWORK & RETEST

22 LIST BELOW ALL PARTS REPLACED, REPAIRED OR ADJUSTED

(A) CIRCUIT SYMBOL	(B) PART NUMBER	(C) S/N	(D) MANUFACTURER	(E) DEFECT	(F) REWORK ACTION TAKEN	(G) RECEIVING LOT NO	(H) APPROVED PARTS YES	(H) APPROVED PARTS NO	PRI. FAIL.
A4C4	M39003-1-2255			INTERNAL SOLDER FLOW	REMOVE, CUT LEADS				

DO NOT USE

23 OTHER REWORK ACTION
RETEST A4 PERFORMANCE AT ROOM TEMP TO VERIFY A4C4 DEFECT.

24 REWORKED BY	ORG CODE	25 RETESTED BY	ORG CODE	26 RETEST RESULTS APPROVAL	DATE
		[signature] 03/11/92	1A 72 30	[signature]	03/11/92

27 RETEST RESULTS REPAIRED ITEM IS ACCEPTABLE FOR ☐ UNRESTRICTED USE ☒ RESTRICTED USE ☐ NOT ACCEPTABLE (EXPLAIN IN BLOCK 30)

28 DISPOSITION OF ITEM AFTER RETEST | 29 Q C

NO. 1 / 381

ENGINEERING

30 CAUSE OF FAILURE - COMMENTS (IF ANALYSIS NOT PERFORMED EXPLAIN)

SHORT CIRCUIT -5V SUPPLY LINE DETECTOR A4 DUE TO INTERNAL SOLDER FLOWING FROM CAPACITOR A4C4. REMOVED (CUT LEADS) OF DEFECTIVE A4C4 & VERIFIED ASSY PERFORMANCE IS PASSING. PART RATED TO +125°C (DF=4%) & 10Vdc. EXPOSURE AT FAILURE WAS +150°C & -7.0Vdc LEVEL 10.

31 BASIC CAUSE OF TROUBLE/FAILURE (SELECT FROM BLOCK 1 ON REVERSE SIDE)	32 SIGNATURE	ORG CODE	DATE
ENVIRONMENTAL EFFECTS	[signature]	1A72 30	03/11/92

33 CORRECTIVE ENGINEERING ACTION TAKEN (IF NONE JUSTIFY - CONCLUSIONS)
DOCUMENT FOR EVALUATION OF ACCEL STEP-STRESS TEST APPROACH.
REF ENB (IDC# 92/1A72.30/005).

REF. DOCUMENT IMPLEMENTING CORRECTIVE ACTION (EO ECR ETC) IS NO. | 34 SIGNATURE | ORG CODE | DATE

11020 CS MAR 66

USE TFR CONTINUATION SHEET IF ADDITIONAL SPACE IS NEEDED

FOR RELIABILITY ANALYSIS AND FOLLOW-UP SEE REVERSE SIDE OF COPY 4

Z 7387

HUGHES AIRCRAFT CO.
GROUND SYSTEMS GROUP

MSN [redacted]15

1377 B44 B4A1A1

REF. NO. 401986

MODEL LEVEL

HISTORICAL RECORD TAG

SYST. NOMEN.

PART OR ASSEMBLY NAME	PART OR ASSEMBLY NO.	LTR.CHANGE
R/T MODULE	[redacted]103	

PLANNING CHANGE #	DEPT. ORIGINATED	NEXT ASSEMBLY NO.	HAC MFG. SERIAL NO.

EFFECTIVE AMENDING DOCUMENTS	W/O NO.	SERIAL NO.
~~T326-TEG-22000A~~		815

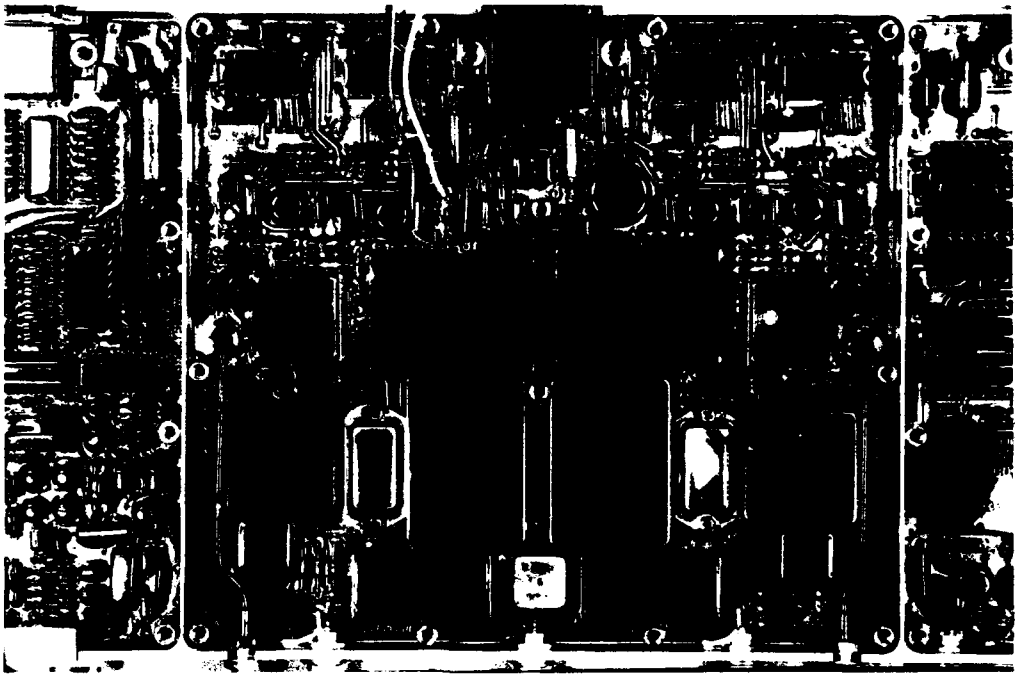
ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
			TOD	
9/23/91			Passed Synth Tests & Detector Sanity.	9/23/91
OCT 9			T TOD PRE TEMP VERIFICATION COMPLETE	
OCT 14 91			T TOD 6 CYCLES TEMP SCREEN COMPLETE	OCT 14 91
10/31/91			TOD Post temp functional test completed	10/31/91
			T TCD @ A3 U9. 15 NO output Replace 725000-181	FEB 28
2/13/92			T TCB @ IF1 Broken -13300 1-1	FEB 28
FEB 18			TOUCH UP C/C REQ'D	
03/06/92			VISUAL INSP FOLLOWING STEP-STRESS TEST	2/25/92
ENGR NOTE			UUT STEP-STRESS TESTED 03/05/92 THRU 03/06/92 TO LEVEL 10 AND INCURRED FAILURE. -5V SUPPLY	

ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
NOTE	CONT.		OF DETECTOR INCREASED TO 2.93A @ -0.89V. NO I&Q OUTPUTS. SEE TFR# Z7387. REFERENCE TEST PLAN PER CDRL# J003-001 OF CONTRACT F30602-89-D-0100/009.	03/11/92
NOTE:		03/09/92	Sent to FA for X-Ray of A4C4 Solder	03/09/92
		03/11/92	Removed capacitor A4C4 from CCA by cutting leads. Verified part shorted with Ohmmeter & that -5V supply line short ckt was corrected w/ C4 removed. Retested DETECTOR SHARLY PAIR & I&Q-bits. ~~Performance is PASSING @ Room Temp~~ Failure confirmed as A4C4 BAD PART.	03/11/92
		03/11/92	NEED to REPLACE A4C4 CAPACITOR (P/N M39003-01-2255) & verify DETECTOR Alignment prior to 2nd attempt of STEP-STRESS TEST.	

CONT. OTHER SIDE

FAILURE ANALYSIS DATA SHEET
STEP – STRESS TEST ATTACHMENT 1 of 4

MSN 0815 ASSY A4
ENGR L.A. Mueller DATE 03/92



R. Cantu 03/06/92

A4 DETECTOR; FAILURE LEVEL 10 (+150°C, ±7.0V, ±18.0V)



K.G. Mohr 03/09/92 X4 Magnification

A4-C4 TANTALUM CAPACITOR FAILURE;
SOLDER FLOW RESULTING IN -5V SUPPLY SHORT

FAILURE ANALYSIS DATA SHEET
STEP – STRESS TEST ATTACHMENT 2 of 4

MSN 0815 ASSY A2,A3,A4
ENGR [signature] DATE 03/06/92

TFR# Z7387; HRT# 401986

VISUAL ASSEMBLY INSPECTION NOTES:

A2 SYNTHESIZER (S/N 1971) No Attachment necessary.

1 Stresses to LEVEL 10 produced yellowing of conformal coating on PWB tending towards a light caramel brown. Conformal coating covering IC's and U11 are discolored to a darker caramel brown. Component markings are still visible through the discolored coating. Coating in general is uniform throughout.

A3 SYNTHESIZER (S/N 1805) No Attachment necessary.

2 PWB is covered with green solder mask coating and therefore conformal coating is not uniform throughout. Board surfaces are also dirty throughout.

3 Stresses to LEVEL 10 have discolored conformal coating. Coating on PWB is yellowed to light caramel brown in areas. Most coating covering components are a dark caramel brown, with U11 darkest. Coating at U11 takes on a reddish brown appearance.

A4 DUAL DETECTOR (S/N 0553) See Attachment detail.

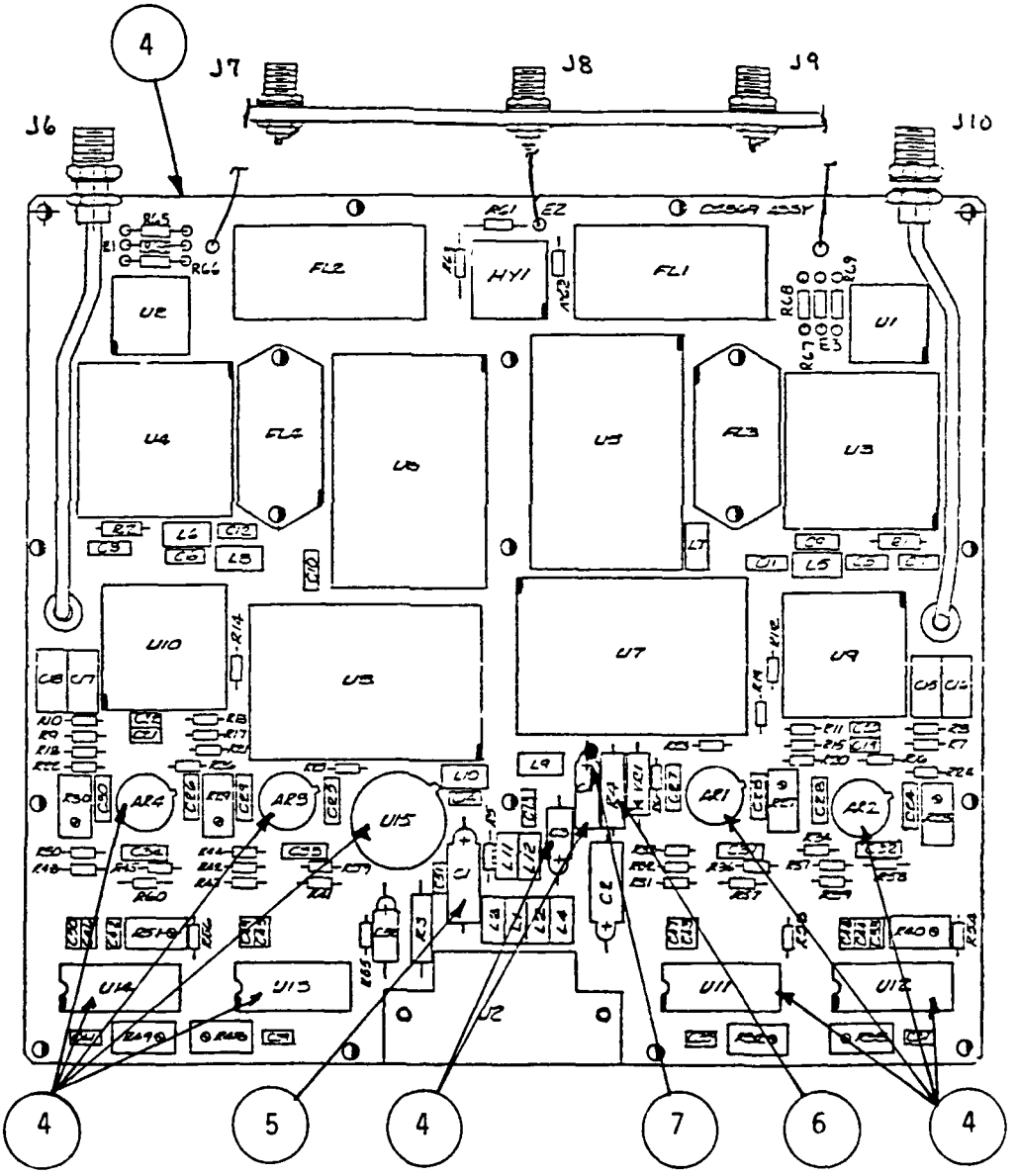
4 Conformal coating is uniform throughout. Stresses to LEVEL 10 have discolored coating to a light caramel brown. Coating in contact with IC's U11-U14, and components U15, AR1 through AR4, U3, C3 and C4 are darker than surrounding PWB and components.

5 Conformal coating on C1 is cracked and could peel.

6 Black case of R4 has turned to an ashen grey color in spots due to excessive heat generated. Adjacent part VR1 appears unchanged.

7 Positive terminal of C4 had solder flowing from component case, forming solder ball on terminal.

FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 3 of 4	MSN 0815 ASSY A4 (0553) ENGR [signature] DATE 03/06/92



FAILURE ANALYSIS DATA SHEET

ATTACHMENT 4 of 4

UUT Serial Number (enter MSN): 0815 Analysis Date: 03/11/92

MRTS# 401986 Engineer: (Name & stamp below) D Mueller 656 92466 TEST

Test Conducted at Room Temperature

SPECIAL CONDITIONS: Supply filter capacitor A4-C4 removed from DETECTOR -5V Supply Line. Was shorted to Ground. Test data below.

DETECTOR VOLTAGE SETTINGS:

Supply Voltages: + 5 Volts dc: +5.00 (Vdc) - 5 Volts dc: -5.00 (Vdc)

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.00 (Vdc)

Aux. - 5 Volt Setting: -5.1088 (Vdc) R_{LOAD} Voltage: -5.0997 (Vdc)

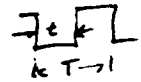
DETECTOR CURRENT MEASUREMENTS:

UUT Currents: + 5 Volts dc: 137.6 (mA) - 5 Volts dc: 47.2 (mA)

+15 Volts dc: 66.1 (mA) -15 Volts dc: 304.7 (mA)

DETECTOR,DIGITAL OUTPUT MEASUREMENTS:

Rcv Sig Input	I & Q -Bits	DETECTOR 1 t (usec) / T (usec)	DETECTOR 1 Duty Cycle (percent)	DETECTOR 2 t (usec) / T (usec)	DETECTOR 2 Duty Cycle (percent)	COMMENTS
Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm						
0 dBm	I > 0	4.80/9.60	50.0	4.68/9.60	48.8	
	I > Q	"	50.0	4.80/9.60	50.0	
	I + Q > 0	4.68/9.60	48.8	"	50.0	
	Q > 0	"	48.8	4.68/9.60	48.8	
-75 dBm	I > 0	4.68/9.60	48.8	4.42/9.60	51.2	
	I > Q	4.80/9.60	50.0	4.80/9.60	50.0	
	I + Q > 0	"	50.0	"	50.0	
	Q > 0	"	50.0	"	50.0	
Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm						
0 dBm	I > 0	4.80/9.60	50.0	4.80/9.60	50.0	
	I > Q	4.68/9.60	48.8	"	50.0	
	I + Q > 0	4.80/9.60	50.0	"	50.0	
	Q > 0	4.68/9.60	48.8	4.68/9.60	48.8	
-75 dBm	I > 0	4.80/9.60	50.0	4.80/9.60	50.0	
	I > Q	"	50.0	4.68/9.60	48.8	
	I + Q > 0	"	50.0	4.80/9.60	50.0	
	Q > 0	4.68/9.60	48.8	"	50.0	



8 div @ 1.20μsec/

Removal of capacitor slightly increased jitter of noise.

STEP-STRESS TEST

FAILURE ANALYSIS NOTEBOOK
Unit Under Test: MSN 1029

FAILURE SUMMARY

FAILURE LEVEL:	LEVEL 7
FAILURE MODE(S):	TEMPERATURE SENSITIVITY OF CIRCUITRY ABOVE +62.5°C TO INCLUDE LIFTED PAD AT INPUT PIN TO A4-FL4 FILTER. RESULTED IN LOSS OF GAIN.
AFFECTED PART(S):	LIFTED PAD AT INPUT OF SAW FILTER A4-FL4 P/N 730000-8.

FIXED STEP DWELL TIME:	1 HOUR
FIXED RAMP & STABILIZATION:	30 MINUTES
TOTAL ELAPSED TIME TO FAILURE: (FROM END OF LEVEL 0 DWELL)	9 HOURS: 46 MINUTES
ANOMALY TEST TIME: (INCLUDED IN TOTAL ABOVE)	NONE

HUGHES
HUGHES AIRCRAFT COMPANY

STEP-STRESS
1. PROJECT NAME

TROUBLE & FAILURE REPORT

FAIL CLASS	TEST TYPE	TEST ENV	FAIL CAUSE	RELEV

NO. Z7388

FAM CODE | SYST CODE

2. THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE ☒ FAILURE

ORIGINATOR

3. SYSTEM, SUBSYSTEM NAME: R/T MODULE | P/N: Partno -103 | S/N: 1029
4. TIMER COUNTER READINGS: TIME: 18.31 LEVEL 7 ELAPSED 11.2 HOURS / CYCLES
5. DATE: 03 (MO) 10 (DAY) 92 (YR)
33. REFERENCES
6. REPORTING FACILITY: STEP-STRESS TEST C/O S.D. MUELLER
7. REPORTED BY: S.D. Mueller 03/10/92 | ORG CODE: IA 72 30
OPERATING LOG NO
8. TROUBLE FAILURE OBSERVED WAS: (TEST CONDITIONS SYMPTOMS, SEVERITY, ETC., INCLUDING "IS" AND "SHOULD BE" DATA)
TFR CONTINUATION USED ☐

DETECTOR #2 LOW IN GAIN BY 15dB TO 20dB. Should RAV SIGNAL AT -75dBm Is ONLY OPERATING TO -58dBm TO -55 dBm INPUT LEVEL. NO PROBLEM AT HIGH INPUT LEVEL OF 0 dBm. UUT FAILED AT LEVEL 7 (+117°C CHAMBER AIR; +126°C FLANGE; +126°C COMPONENT AVG AIR TEMP; ± 6.4 Vdc; ±17.1 Vdc). FAILURE VERIFIED AT LEVEL 6 & LEVEL 0 RETEST.

9. TROUBLE FAILURE OCCURRED DURING: (A) ☒ ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE-FLIGHT OR CURSORY CHECK
10. ACTION TAKEN TO CORRECT TROUBLE FAILURE: (A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 - 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 - 29)

11. ITEM REPLACED NAME	P/N	S/N	12. ITEM INSTALLED NAME	P/N	S/N	13. DISPOSITION OF REPLACED ITEM

VERIFICATION

14. WERE OTHER TROUBLES FAILURES, NOT RELATED TO ORIGINAL NOTED? (A) ☒ NO (B) ☐ YES LIST ON NEW TFR - TFR NO. _____
15. WAS REPORTED TROUBLE FAILURE VERIFIED? (A) ☐ YES (B) ☐ NO (CHECK 16 B AND EXPLAIN)

16. FAILED ITEM NAME	P/N	S/N	REF DESIG	MANUFACTURER

17. NEXT HIGHER ASSY NAME	P/N	S/N	REF. DESIG	MANUFACTURER
DETECTOR, CKT CARD ASSY	na	0577	A4	05869

18. (A) ☐ REWORK REQUIRED IS (B) ☐ REWORK IS NOT REQUIRED BECAUSE
19. VENDOR REWORK ANALYSIS IS REQUIRED ☐ ITR _____ C.A.R _____

VERIFY BY TEST AT ROOM TEMP DET #2 LOW GAIN. USE DET #1 FOR COMPARISON. PERFORM VIDEO GAIN, LIMITING LEVEL, AND NOISE LEVEL TESTS IN ADDITION TO I & O-BIT TESTS. T/S LIM AMPS U6 & U8, AND THEN U4 RF AMP HYBRIDS (MOST PROBABLE CAUSE) 03/13/92. TESTING ABOVE +25°C TO +70°C WILL BE REQUIRED TO VERIFY. S.D. Mueller 03/15/92 (68[illegible])

20. DISPOSITION OF ITEM IF NOT REWORKED: SEE RETEST BELOW 03/29/92 & 05/26/92
21. AUTHORIZATION BY _____ ORG CODE _____ DATE _____

REWORK & RETEST

22. LIST BELOW ALL PARTS REPLACED, REPAIRED OR ADJUSTED

(A) CIRCUIT SYMBOL	(B) PART NUMBER	(C) S/N	(D) MANUFACTURER	(E) DEFECT	(F) REWORK ACTION TAKEN	(G) RECEIVING LOT NO.	(H) APPROVED PARTS YES	(H) APPROVED PARTS NO	PRI. FAIL.	DO NOT USE
INPUT PAD A4-FL4				LIFTED						
A4-FL4	730000-8	4383	05869	AFFECTED INPUT						

23. OTHER REWORK ACTION: AT +25°C PERFORMED TESTS ABOVE. NO ADJUSTMENTS. (68[illegible] 03/15/92) RETEST +25°C TO +80°C AT PTP2. VALIDATED FAILURE. S.D.M 05/26/92 (92466) 05/28 & RETEST PART BY PART AT TEMP (DETECTOR 2 LIMITER CHAIN HY1, FL2, U2, U4, FL4, U5, U8) 05/29/92

24. REWORKED BY	ORG. CODE	25. RETESTED BY	ORG. CODE	26. RETEST RESULTS APPROVAL	DATE
		S.D. Mueller 03/29/92	IA 7230	S.D. Mueller (68[illegible])	03/29/92

27. RETEST RESULTS REPAIRED ITEM IS ACCEPTABLE FOR: ☐ UNRESTRICTED USE ☒ RESTRICTED USE ☐ NOT ACCEPTABLE (EXPLAIN IN BLOCK 30)
28. DISPOSITION OF ITEM AFTER RETEST: REWORK A4-FL4
29. E C

ENGINEERING

30. CAUSE OF FAILURE - COMMENTS (IF ANALYSIS NOT PERFORMED EXPLAIN): PERFORMED VIDEO GAIN, LIMITING LEVEL & NOISE LEVEL, AND I&O-BIT TESTS BOTH DET #1 & #2. FAILURE COULD NOT BE VERIFIED AT +25°C. FURTHER TESTING AT ELEVATED TEMP STILL REQUIRED. 05/26/92 RETEST AND VALIDATED FAILURE AT +62.5°C PLUS. WORST LOSS AT +69°C (92466) 05/28-05/29/92 RETEST & REPEATED. FOUND FL4 SENSITIVE TO TEMP & PRESSURE AFFECTING LOSS. U4 SLIGHTLY SENSITIVE. INSPECT SOLDER SIDE & FOUND LIFTED PAD AT FL4 INPUT PIN. PART BY PART TROUBLE-SHOOTING COULD NOT PINPOINT DEFECT. A4-FL4 PAD COULD CAUSE IMPEDANCE MISMATCH. (68[illegible] 05/29/92)

31. BASIC CAUSE OF TROUBLE FAILURE (SELECT FROM BLOCK 1 ON REVERSE SIDE): ENVIRONMENTAL EFFECTS
32. SIGNATURE: S.D. Mueller (68[illegible]) | ORG CODE: IA 7230 | DATE: 05/29/92
33. CORRECTIVE ENGINEERING ACTION TAKEN (IF NONE, JUSTIFY CONCLUSION): DOCUMENT FOR ACCELERATED STEP-STRESS APPROACH REF ENGR'G NOTEBOOK (IDC# 92/1A72.30/005).

REF. DOCUMENT IMPLEMENTING CORRECTIVE ACTION (EO ECR ETC) IS: NO.
34. SIGNATURE | ORG. CODE | DATE

11020 CS MAR 66

USE TFR CONTINUATION SHEET IF ADDITIONAL SPACE IS NEEDED

FOR RELIABILITY ANALYSIS AND FOLLOW-UP ACTION SEE REVERSE SIDE OF COPY 4

19

Z7388

NO. Z7388

1

HUGHES AIRCRAFT CO.
GROUND SYSTEMS GROUP

PAGE 1 OF ____

HRT# 401[illegible]
MSN 1029

MODEL LEVEL: P/N 7720444-3448191
132 GLTB 220003

REF. NO. 401984

HISTORICAL RECORD TAG

SYST. NOMEN.

PART OR ASSEMBLY NAME	PART OR ASSEMBLY NO.	LTR. CHANGE
	[redacted] 103	

PLANNING CHANGE #	DEPT. ORIGINATED	NEXT ASSEMBLY NO.	HAC MFG. SERIAL NO.

EFFECTIVE AMENDING DOCUMENTS	W/O NO.	SERIAL NO.
132-GTB-220001		1029

ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
			Two	
9/23/91			Passed Synth Tests & Detector Staircase Tests	9/24/91
	GSG 92466 TEST		I TOO FREE TEMP VERIFICATION COMPLETE	OCT 5 '91
	S402 TEST		I TOO 6 CYCLES TEMP SCREEN COMPLETE	
10/3/91			Bst temp functional test completed	10/31/91
			-1 TCB (1) UE1 Broken 417601-66	
			TOUCH UP C/C DEN'D	7/25/92
			T TOO C62 FLI Test complete	2/25/92
2/28/92			T TCB (1) FLI Broken - Replace 773001-1	
3/9/92				

FORM NO. 4932-GS REV. 11-85

CONT. OTHER SIDE

ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
MGR	NOTE		UUT STEP-STRESS TESTED 03/10/92 TO LEVEL 7 AND INCURRED FAILURE. DETECTOR #2 LOW IN GAIN BY 15dB TO 20dB. RCV INPUTS TO -55dBm AND S/B -75dBm. SEE TFR# Z7388. REFERENCE TEST PLAN PER CDR# J003-001 OF F30602-89-D-0100/009.	GSG 92466 TEST 03/11/92
ENG	NOTE		ISSUE INSPECTION FOUND NO STRESS RELATED PROBLEM	03/13/92
	GSG 92466 TEST		03/5/92 WITH COVER REMOVED, TESTED DET A1 #1 & #2 FOR CURRENT A I & Q-BIT DUTY CYCLE ROOM TEMP. NO FAILIT FOUND w/ PERFORMNCE TEST, USE AUTO TP TO CHECK & COMPARE DET #1 & #2 VIDEO GAIN, LIA & NOISE LEVEL FOR AR3, H10, U8 (HTC2), U6 & U4 LOW GAIN TROUBLE COULD'S BE DETERMINED @ +25°C. WILL REQUIRE FURTHER T/S AT ELEVATED TEMPERATURE(S) FOR DET #2 LOW GAIN TO BE VERIFIED	03/15/92
	GSG 92466 TEST	05/26/92	SOLDERED TEST CABLE AT TP2 TO MONITOR CHANGE IN LIMITER GAIN OVER TEMP RANGE +2°C TO +50°C. VALIDATED & REPEATED FAILURE OBSERVED DURING STEP-STRESS TEST. I & Q SENSITIVITY 12dB LOSS AT +62.5°C WITH 19dB CHAIN LOSS @ +69°C AND CONSTANT > +76°C. NEED T/S COMPONENTS	GSG 92466 TEST 05/26/92
	GSG 92466 TEST		05/28/92 AT +69°C FLY SENSITIVE TO ALCOHOL SWAB @ PRESSURE [redacted] U4 AND SOMEWHAT SENSITIVE TO SHAKE. REMOVE A1 DETECTOR FROM CHASSIS. LIFTED LEAD AT FLY INPUT PIN & DISTURBED SOLDER AT OUTPUT. SOLDER TEST CABLE TO TRACES AT INPUT/OUTPUT OF FLY U4, U6, U8, U2. REPLACE J8 & J7 WITH TEST SOLDER WIRES TO C8 TO PROVIDE -15V TO HYB	CABLE 92466 TEST IDS 05/28/92
	690 92466 TEST		05/29/92 TROUBLE-SHOOTING COMPONENTS COULD NOT LOCATE SINGLE CONTRIBUTOR OF 19dB LOSS OVER TEMP. SOLDERING & REMOVAL FROM CHASSIS MAY HAVE ALLEVIATED DEFECT. HOWEVER FLY INSPECTION & PRIOR OBSERVATIONS ARE SUGGESTIVE OF FAILURE DUE TO IMPEDANCE MISMATCH & SUSCEPTIBILITY TO LINEAR REGION OF OPERATION OF HYI, FL2, U2, U4 & FL4. COULD NOT REPEAT FAILURE AFTER T/S EXERCISE	GSG 92466 TEST 05/29/92
	GSG 92466		05/29/92 Replace C/Clean FLY Repair Lifted Pad & Touch up Solder Detector 2 limiter chain. T/U C. Crandall Hampton	

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FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 1 of 8	MSN 1029 ASSY A2,A3,A4 ENGR DB Mueller DATE 03/13/92

TFR# Z7388; HRT#

VISUAL ASSEMBLY INSPECTION NOTES:

A2 SYNTHESIZER (S/N 2027) No Attachment necessary.

1 Stresses to LEVEL 7 produced yellowing of conformal coating on PWB with slight darkening on active components. Coating in general is uniform throughout. Surfaces are very clean throughout.

A3 SYNTHESIZER (S/N 2024) No Attachment necessary.

2 Stresses to LEVEL 7 produced yellowing of conformal coating on PWB with slight darkening on active components. Coating in general is uniform throughout. Surfaces are very clean throughout.

A4 DUAL DETECTOR (S/N 0577) See Attachment detail.

3 Stresses to LEVEL 7 has yellowed conformal coating throughout. PWB is covered with green solder mask coating and therefore conformal coating is not uniform throughout. Board surfaces are also dirty throughout.

4 Conformal coating is sparce and/or peeling in areas indicated..

5 Conformal coating is missing from component U2, U4, U6, U8, U10 FL4, and HY1 of Detector #2 side of circuit card.. Condition existed prior to Step-Stress test.

6 Conformal coating covering R4 has turned to a darkened caramel brown color.

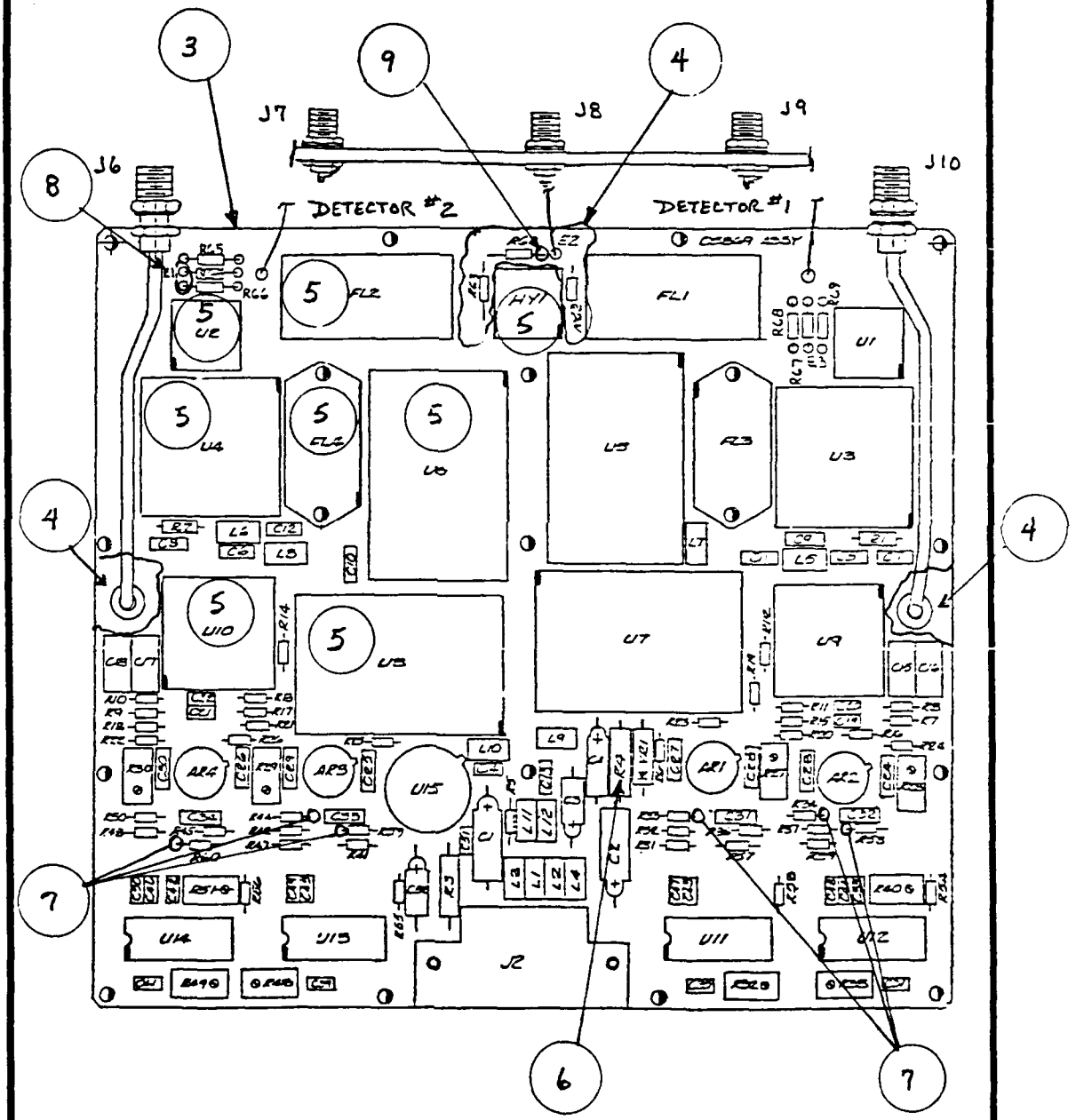
7 Deep test probe marks found at R33, R34, 44, R53, R59, and R60. Condition existed prior to Step-Stress test.

8 Trace and pad are lifting with epoxy used for Engineering change at E1.

9 Solder void at pad of R61. DBM 03/13/92

FAILURE ANALYSIS DATA SHEET
STEP – STRESS TEST ATTACHMENT 2 of 8

MSN 1029 ASSY A4 (0577)
ENGR D. Mueller DATE 03/13/92



FAILURE ANALYSIS DATA SHEET

UUT Serial Number (enter MSN): 1029 +24 °C

Analysis Date: 03/15/92

Engineer: (Name & stamp below) A.D. Mueller GSC 92466 TECH

Test Conducted at Room Temperature

SPECIAL CONDITIONS: Bench tested @ Room Temp. Cover Removed. Detector #2 had Failed @ LEVEL 7 & 0 03/10/92. Low CH. gain.

DETECTOR VOLTAGE SETTINGS:

Supply Voltages: +5 Volts dc: +5.00 (Vdc) -5 Volts dc: -5.00 (Vdc)

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.00 (Vdc)

Aux. -5 Volt Setting: -5.094 (Vdc) R_{LOAD} Voltage: 5.1184 (Vdc)

DETECTOR CURRENT MEASUREMENTS:

UUT Currents: +5 Volts dc: 146.0 (mA) -5 Volts dc: 48.8 (mA)

+15 Volts dc: 55.7 (mA) -15 Volts dc: 305.4 (mA)

DETECTOR,DIGITAL OUTPUT MEASUREMENTS:

Rcv Sig Input	I & Q -Bits	DETECTOR 1 t (usec) / T (usec)	DETECTOR 1 Duty Cycle (percent)	DETECTOR 2 t (usec) / T (usec)	DETECTOR 2 Duty Cycle (percent)	COMMENTS
Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm						
0 dBm	I > 0	4.68/9.60	48.8	4.68/9.60	48.8	8 div @ 1.20 μsec/div
	I > Q	4.80/9.60	50.0	4.80/9.60	50.0	
	I + Q > 0	4.68/9.60	48.8	"	50.0	
	Q > 0	"	48.8	4.56/9.60	47.5	
-75 dBm	I > 0	4.80/9.60	50.0	4.92/9.60	51.2	
	I > Q	"	50.0	"	51.2	
	I + Q > 0	4.92/9.60	51.2	"	51.2	
	Q > 0	4.80/9.60	50.0	"	51.2	
Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm						
0 dBm	I > 0	4.80/9.60	50.0	4.68/9.60	48.8	
	I > Q	"	50.0	4.80/9.60	50.0	NO DETECTOR #2 GAIN PROBLEM OBSERVED @ ROOM TEMP.
	I + Q > 0	"	50.0	"	50.0	
	Q > 0	4.68/9.60 NOISIER	48.8	4.56/9.60	47.5	
-75 dBm	I > 0	4.92/9.60	51.2	4.92/9.60	51.2	
	I > Q	4.80/9.60	50.0	4.80/9.60	50.0	
	I + Q > 0	4.92/9.60	51.2	4.92/9.60	51.2	
	Q > 0	4.68/9.60	48.8	"	51.2	

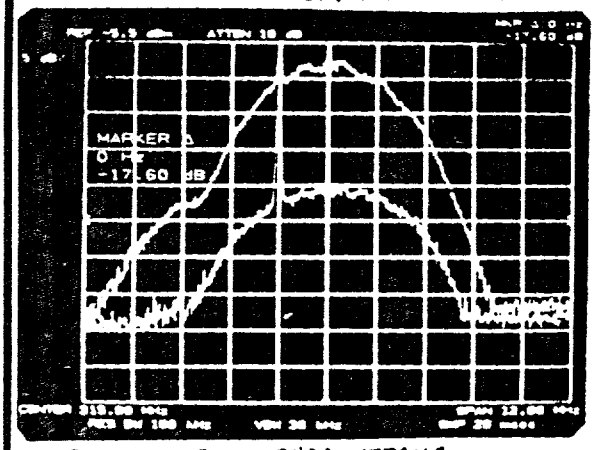
VALIDATE FAILURE AT TEMPERATURE

FAILURE ANALYSIS DATA SHEET
STEP – STRESS TEST ATTACHMENT 4 of 8

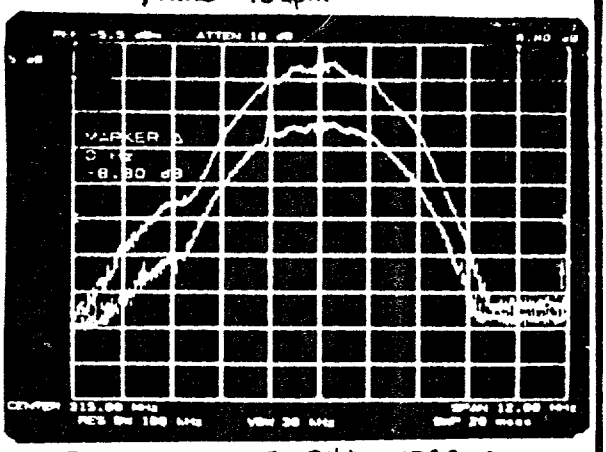
MSN 1029 ASSY A4 DETECTOR 2
ENGR [illegible] (GSO 92466 TEST) DATE 05/26/92

IN CHASSIS; OPEN COVER; NOMINAL VOLTAGES. VERIFICATION RUN

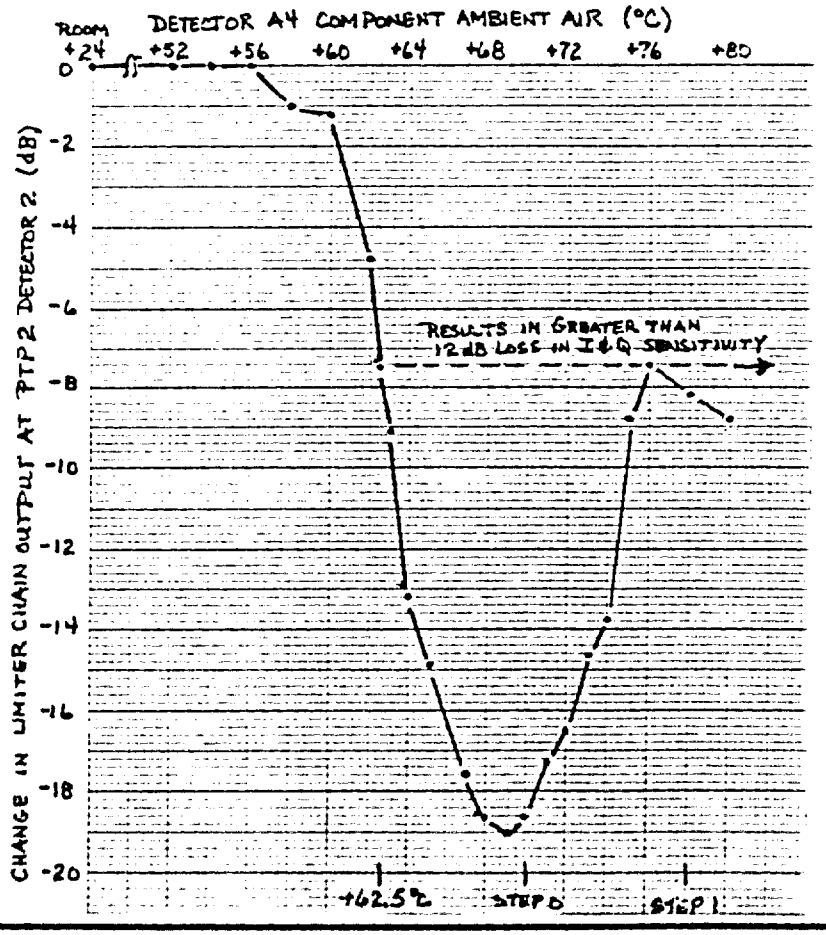
DETECTOR # 2 LIMITER CHAIN BANDPASS AT TEST POINT PTP2 OVER TEMP
SWEPT INPUT SIGNAL 591 TO 621 MHz, FIXED -75 dBm



ROOM TEMP OF +24°C VERSUS
CHANGE AT +67°C (-17.6 dB)
315 MHz OUTPUT



ROOM TEMP OF +24°C VERSUS
CHANGE AT +75°C (-8.8 dB)
315 MHz OUTPUT



J7 @ 921 MHz CW, +10dBm
J6 @ 313.75 MHz CW, +11dBm
J8 @ 606 MHz SWEPT 15 MHz; -75 dBm
CH 00
DETECTOR #2

TEMP °C	ΔPTP2 dB	
+24	0.0 REF.	
+52	0.0	
+54	0.0	
+56	0.0	
+58	-1.0	
+60	-1.2	
+62	-4.8	
+62.5	-7.4	
+63	-9.1	I&Q BITS DROP OUT
+64	-13.2	
+65	-14.8	
+67	-17.6	
+68	-18.6	
+69	-19.0	MAX
+70	-18.6	
+71	-17.3	
+72	-16.5	
+73	-14.6	
+74	-13.8	
+75	-8.8	
+76	-7.4	
+78	-8.2	
+80	-8.8	

TROUBLE-SHOOTING NOTES

FAILURE ANALYSIS DATA SHEET
STEP-STRESS TEST ATTACHMENT 5 of 8

MSN 1029 ASSY A4 DETECTOR
ENGR [illegible] DATE 05/28 - 05/29/92

On 05/26/92 a verification run was made to validate the 12 to 15 dB of loss that was indicating a FAILURE at LEVEL 7, 6, and 0 of the STEP-STRESS TEST reported in TFR # Z7388 of 03/10/92. Room temperature testing conducted on 03/15/92 could not validate the observed FAILURE.

The cover was removed from the UUT and a test cable soldered to PTP2 at the output of the limiter chain, detector 2. The loss through the chain was recorded as a delta relative to the output at room temperature, +24°C. The UUT's Detector 2 was run over temperature to +80°C. Two polaroids were taken at +67°C and +75°C showing the incurred loss. Also attached is a plot of data recorded. This shows Detector 2, I & Q bits lose ≈ 12dB of sensitivity at greater than +62.5°C and indicates a maximum differential loss of 19dB at +69°C (below the specified operating temperature of +70°C). The loss above +69°C is recovered in part by the wealth of gain inherent in the limiter chain. However, full recovery of the losses experienced are never realized and seem to hold constant above +76°C. The FAILURE IS VALID and REPEATABLE ABOVE +62.5°C.

The investigation continued 05/28 thru 05/29/92 to pin point the FAILING component. Originally TFR # Z7388 suspected lim amps U6, U8, or RF amp U4. With the unit still in the chassis, the UUT was heated to +69.0°C and allowed to stabilize again. The output at PTP2 again was monitored with identical results. A cotton swab with alcohol was used to cool each of the components when the chamber door was opened. FL4 when cooled was extremely sensitive and the losses were nearly recovered. A wood stick was used to apply pressure to each component. Again FL4 was sensitive to touch, with U4 slightly sensitive. U6 and U8 limiter amps were unaffected by either attempt.

The A4 Detector was removed from its chassis and semi rigid test cables soldered between components on the pin side of the printed wiring board. The center point of connecting traces were used for the contact point of the test cables to avoid disturbing or reflowing solder at the component pins. This was important since upon visual inspection of the solder side of FL4, a lifting pad was evident at the SAW Filter input pin (output of RF amp U4) which could explain the observed sensitivity noted above. See photo taken.

With the A4 Detector card removed from the chassis; loss of ground, component isolation, lack of test points, and high gain of chain becomes a problem. The soldering of test cables to traces helps the trouble-shooting effort, but adds mismatch losses to the measurements. Double terminating each 50 ohm impedance component input and output will contribute approximately 3dB (per connection) of loss, which must be considered in the resulting measurement. Relative measurements were practical, and concentration was placed primarily on observing the component which would have the greatest delta change over the temperature range of +24°C through +80°C.

CONTINUED NEXT PAGE

FAILURE ANALYSIS DATA SHEET
STEP – STRESS TEST ATTACHMENT 6 of 8

MSN 1029 ASSY A4 DETECTOR 2
ENGR S.D. Mueller DATE 05/28-05/29/92

CONTINUED

PICTURES OF EACH component's gain/loss characteristics were taken over the +24°C to +80°C range using a swept source producing a 315 MHz centerfrequency and 12 MHz span. The measured results are recorded below:

PIC #1 A4-FL4 FILTER (730000-8) 17.5 dB LOSS -6 dB TERM ≈ 11.5 dB LOSS SPEC IS -15 dB ± 1 dB LOSS. MEASURED IS ≈ 4 dB BETTER THAN SPEC WHICH IS ACCEPTABLE SINCE SAW FILTERS IMPEDANCES(E) ARE 10 OHMS OF 5:1 VSWR. IN A 50 OHM SYSTEM ANOTHER 3 dB DEVIATION WOULD NOT BE UNEXPECTED USING TEST CABLES SOLDERED TO THE INTERCONNECT TRACES. OVER TEMP RANGE NO CHANGE IN OUTPUT WAS OBSERVED. STILL SUSPECT LIFTING PAD AT INPUT.

PIC #2 A4-U4 RF AMP (728000-47) +16.9 dB GAIN +6 dB TERM ≈ 22.9 dB GAIN. SPEC IS +24 dB ± 1 dB GAIN. THIS SEEMS TO BE WITHIN SPEC AND NO CHANGE EXPERIENCED OVER TEMP.

PIC #3 A4-U6 LIM AMP (728000-112) +29.8 dB GAIN + 6 dB TERM ≈ 35.8 dB GAIN FOR LINEAR OPERATION. SPEC IS +41 dB ± 2 dB LINEAR GAIN. STILL ONLY 3 dB to 7 dB LOW IN GAIN, BUT ONLY 2 dB CHANGE IN LINEAR GAIN OBSERVED FROM +24°C TO +80°C. LIMITED OUTPUT IS +2.4 dBm + 6 dB TERM ≈ + 8.4 dBm. SPEC is +6 dBm ± 2 dB LIMITED OUTPUT. U6 IS WITHIN SPEC FOR LIMITING.

PIC #4 A4-U8 LIM AMP (728000-48) + 24.2 dB GAIN + 6 dB TERM ≈ 30.2 dB GAIN FOR LINEAR OPERATION. SPEC IS + 34 dB ± 1 dB LINEAR GAIN. STILL IS 3dB to 5dB LOW IN GAIN, BUT ONLY 1 dB CHANGE IN LINEAR GAIN OBSERVED AT TEMPERATURE EXTREMES. LIMITED OUTPUT LEVEL IS + 2.6 dBm + 6 dB TERM ≈ 8.6 dBm. SPEC IS +6 dBm ± 2 dB. U8 APPEARS OKAY FOR LIMITED OUTPUT AND IS CONSISTANT WITH MEASUREMENT ACCURACY OF U6 ABOVE.

PIC #5 TESTED TOGETHER J8, HY1, FL2, and U2 (POWER DIVIDER 722466-2, BP FILTER 713772-1, DBL-BALANCED MIXER 723112-10) WITH SWEPT INPUT AT J8 OF 600 MHz to 612 MHz & LO OF 921 MHz. LOSS RECORDED WAS 14 dB - 3 dB TERM ≈ 11 dB LOSS TOTAL. SPECS TOTAL TO LOSS OF 12 dB ± 1 dB. OBSERVED RESULTS ARE WITHIN SPEC AND NO MORE THAN 1 dB CHANGE OBSERVED OVER TEMP.

PIC #6 REPEATED A4 DETECTOR LIMITER CHAIN FROM J8 INPUT TO PTP2 AT TEMP. FINAL VERIFICATION ONLY SHOWED DELTA CHANGE AT +62.5°C OF 2.1 dB (NOT 19 dB AS WHEN IN CHASSIS). OUTPUT LEVELS ARE RELATIVELY UNCHANGED FROM 05/26/92 EXCEPT IN THE 309 MHz TO 312 MHz REGION. THE FAILURE MODE IS NO LONGER EVIDENT.

CONTINUE NEXT PAGE

TROUBLE-SHOOTING NOTES

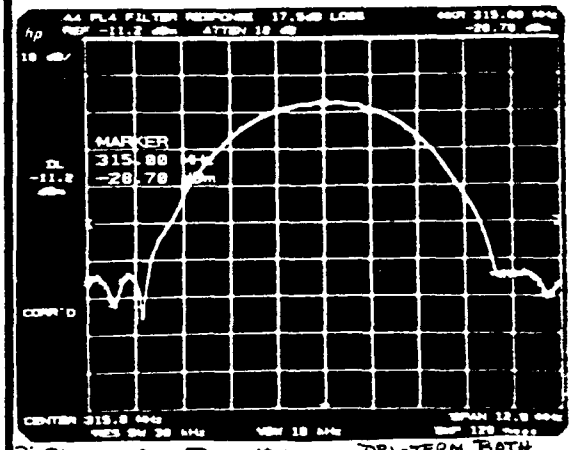
FAILURE ANALYSIS DATA SHEET

STEP – STRESS TEST ATTACHMENT 7 of 8

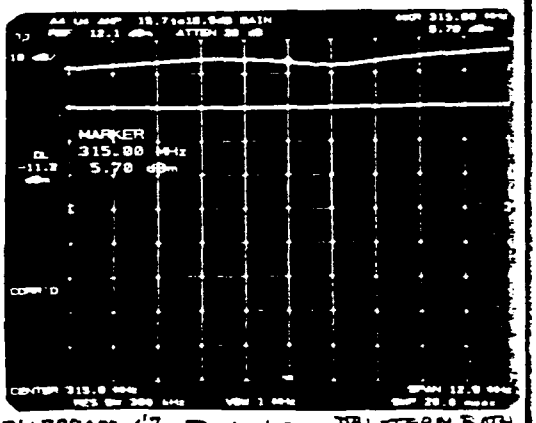
MSN 1029 ASSY A4 DETECTOR 2

ENGR S.M. Muller DATE 05/28 – 05/29/92

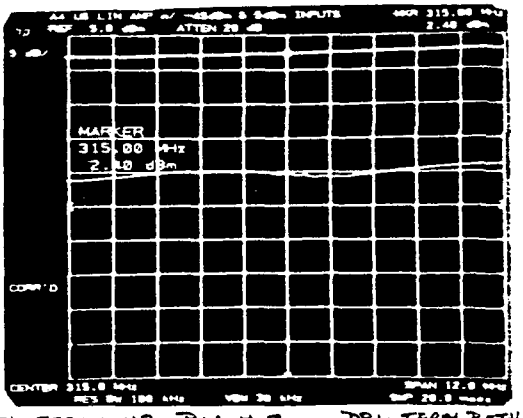
UUT REMOVED FROM CHASSIS TO TROUBLE-SHOOT AT TEMP (+24°C TO +80°C)



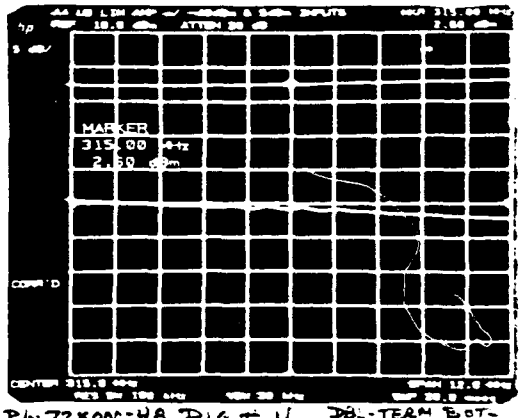
P/N 730000-8 PIC #1 DBL-TERM BOTH ENDS ≈ 6dB



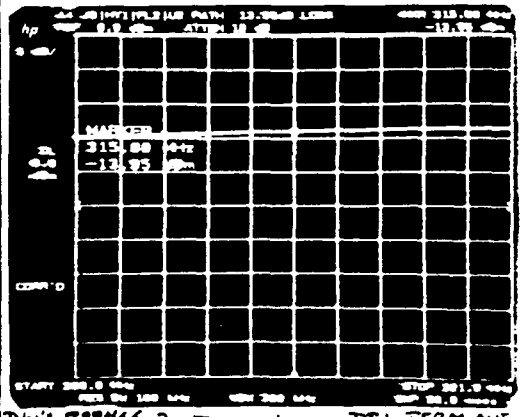
P/N 728000-47 PIC #2 DBL-TERM BOTH ENDS ≈ 6dB



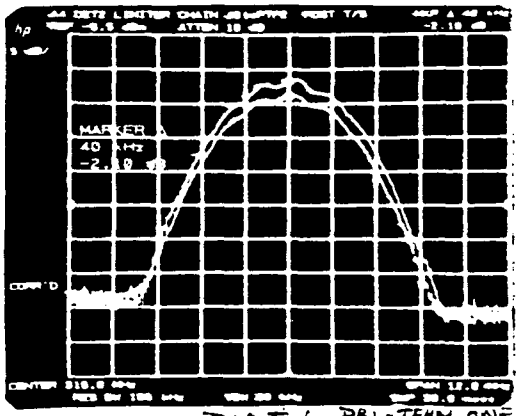
P/N 728000-112 PIC #3 DBL-TERM BOTH ENDS ≈ 6dB



P/N 728000-48 PIC #4 DBL-TERM BOTH ENDS ≈ 6dB



P/N's 728666-2, 713772-1, 723112-10 PIC #5 DBL-TERM ONE END ≈ 3dB



LIM CHAIN FINAL RUN J8 to PTP2 PIC #6 DBL-TERM ONE END ≈ 3dB

CONTINUED NEXT PAGE

FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 8 of 8	MSN 1029 ASSY A4 DETECTOR 2 ENGR L.D. Mueller DATE 05/28-05/29/92

CONTINUED

SUMMARY OF ANALYSIS:

1. FAILURE IDENTIFIED AT STEP-STRESS TEST LEVEL 7 (+126°C) AND REMAINED PRESENT AT LEVEL 6 (+118°C) AND LEVEL 0 (+70°C). TROUBLE FAILURE REPORT Z7388 (03/10/92).
2. FAILURE MODE DOES NOT OCCUR AT ROOM TEMPERATURE (03/15/92). SUSPECT LIM AMPS U6 AND U8, OR RF AMP U4.
3. FAILURE VALIDATED AND REPEATED (05/26/92) BY MONITORING CHANGE IN LIMITER CHAIN OUTPUT AT PTP2 OVER TEMPERATURE RANGE OF +24°C TO +80°C. PHOTOS AND PLOTS OF DATA.
4. FAILURE REPEATED AT 62.5°C AND EVALUATED AT 69°C FOR COMPONENT SENSITIVITY TO COOLING (ALLOHOL SWAB) AND PRESSURE TO CASE (WOOD STICK). DETECTOR 2 LIMITER CHAIN'S SAW FILTER FL4 VERY SENSITIVE TO BOTH, WITH NEAR FULL RECOVERY OF LOSSES. RF AMPLIFIER U4 ALSO SLIGHTLY SENSITIVE (05/28/92).
5. COMPONENT BY COMPONENT TROUBLE-SHOOTING OF LIMITER CHAIN: FL4, U4, U6, U8, HY1, FL2, U2 DID NOT YIELD SINGLE COMPONENT CAUSING FAILURE. VISUAL INSPECTION ON SOLDER SIDE OF PRINTED WIRING BOARD SHOWED A LIFTED PAD AT SAW FILTER INPUT PIN. THIS IS CONNECTED BY CIRCUIT TRACE TO U4 OUTPUT AND COULD EXPLAIN SENSITIVITY TO TEMPERATURE AND PRESSURE OF ITEM 4 ABOVE. (05/28/92 - 05/29/92). PHOTOS OF DATA.
6. FAILURE MODE OF 12 dB TO 15 dB LOSS (19 dB MAX MEASURED) APPEARS TO OCUR IN THE LINEAR RANGE OF THE LIMITER CHAIN. THIS WOULD RULE OUT U6 AND U8 LIMITER AMPLIFIER. USING THE OBSERVATIONS AND DATA GATHERED, FL4 AND U6 ARE THE PRIMARY SUSPECTS WITH THE LIFTED PAD AT FL4'S INPUT A REASONABLE FAILURE MODE AFFECTING THE IMPEDANCE BETWEEN THE LINEAR OPERATING COMPONENTS FL4 AND U4. THE SAW FILTERS IMPEDANCE IS TYPICALLY A POOR 50-OHM MATCH. (05/29/92)

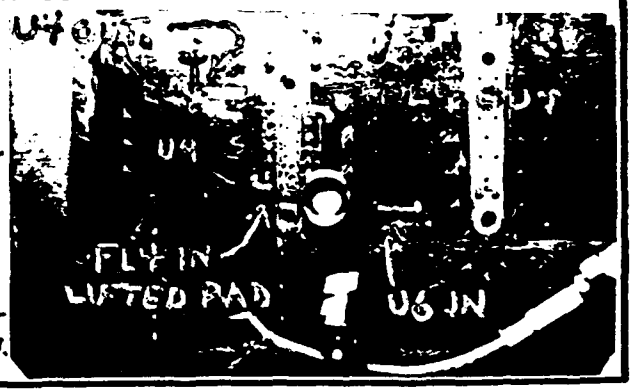


PHOTO SHOWING LIFTED PAD AT FL4 INPUT PIN. FL4 IS A SAW FILTER. BRAID RUNNING THE LENGTH OF FILTER REQUIRED TO IMPROVE INPUT TO OUTPUT ISOLATION.

GSC S2466 TECT

STEP-STRESS TEST

FAILURE ANALYSIS NOTEBOOK
Unit Under Test: MSN 0993

FAILURE SUMMARY

FAILURE LEVEL: LEVEL 10

FAILURE MODE(S): TANTALUM CAPACITOR, A4-C4, INTERNAL SOLDER FLOW RESULTING IN -5 VOLT SUPPLY LINE SHORT.

AFFECTED PART(S): A4-C4; P/N M39003-1-2255.

FIXED STEP DWELL TIME:	1 HOUR
FIXED RAMP & STABILIZATION:	30 MINUTES
TOTAL ELAPSED TIME TO FAILURE: (FROM END OF LEVEL 0 DWELL)	16 HOURS: 30 MINUTES
ANOMALY TEST TIME: (INCLUDED IN TOTAL ABOVE)	2 HOURS: 30 MINUTES

HUGHES
HUGHES AIRCRAFT COMPANY

STEP-STRESS
1. PROJECT NAME

TROUBLE & FAILURE REPORT

FAIL CLASS	TEST TYPE	TEST ENV	FAIL CAUSE	RELEV

FAM CODE | SYST CODE

NO. Z 7390

2. THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE ☒ FAILURE

ORIGINATOR

3. SYSTEM / SUBSYSTEM NAME: R/T MODULE | P/N: part no. -103 | S/N: 993
4. TIMER COUNTER READINGS: TIME: 01:15 LEVEL; ELAPSED: N30 10 (HOURS / CYCLES) | 5. DATE: 03 (MO) 13 (DAY) 92 (YR)
35. REFERENCES
6. REPORTING FACILITY: STEP-STRESS TEST C/O S.D. MUELLER
7. REPORTED BY: S.D. Mueller 03/13/92 (SIGN / DATE) | ORG. CODE: 1A 72 30
OPERATING LOG NO
8. TROUBLE / FAILURE OBSERVED WAS: (TEST CONDITIONS, SYMPTOMS, SEVERITY, ETC., INCLUDING "IS" AND "SHOULD BE" DATA)
TFR CONTINUATION USED ☐

-5V SUPPLY SHORT AT DETECTOR OCCURRED 25 MINUTES (OF 30 MINUTES TOTAL) INTO RAMP AND STABILIZATION AT LEVEL 10, PRIOR TO DWELL. THERMAL & VOLTAGE CONDITIONS REMAINED UNCHANGED AT TIME OF FAILURE AND BEGINNING OF DWELL (+140°C CHAMBER, +15.1°C PLATE, +150 AMB COMPONENT, I?!, =18V). AT FAILURE I&Q-BIT DUTY CYCLE & OUTPUT CEASED TO EXIST, GOING TO HIGH STATE ONLY. -5V SUPPLY (S/B -2.00V) WENT TO -0.9V @ 2.9 AMPS. NO VISUAL INSPECTION AT THIS TIME. REF ALSO TEST DATA SHEETS (NOT ATTACHED). NOT PROVIDED HERE.

9. TROUBLE / FAILURE OCCURRED DURING: (A) ☒ ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE-FLIGHT OR CURSORY CHECK
10. ACTION TAKEN TO CORRECT TROUBLE / FAILURE: (A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 - 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 - 29)

11. ITEM REPLACED NAME	P/N	S/N	12. ITEM INSTALLED NAME	P/N	S/N	13. DISPOSITION OF REPLACED ITEM

VERIFICATION

14. WERE OTHER TROUBLES, FAILURES, NOT RELATED TO ORIGINAL NOTED? (A) ☒ NO (B) ☐ YES — LIST ON NEW TFR - TFR NO. _____
15. WAS REPORTED TROUBLE FAILURE VERIFIED? (A) ☒ YES (B) ☐ NO (CHECK 18 B AND EXPLAIN)

16. FAILED ITEM NAME	P/N	S/N	REF. DESIG.	MANUFACTURER
CAPACITOR, FIXED, TANTALUM	M39003-01-2255	n/a	A4-C4	MIL-C-39003/1

17. NEXT HIGHER ASSY: NAME	P/N	S/N	REF. DESIG.	MANUFACTURER
DETECTOR, CCA	n/a	0559	A4	05869

18. (A) ☒ REWORK REQUIRED IS (B) ☐ REWORK IS NOT REQUIRED BECAUSE
19. VENDOR REWORK ANALYSIS IS REQUIRED ☐ — ITR _____ C.A.R. _____

CLIP C4 FROM SUPPLY LINE & TEST VERIFY ASSY.
PHOTO x4, THEN REMOVE (CLIP LEADS) BAG & TAG PART. REF HRT# 401983.
WILL NEED TO REPLACE A4-C4 PRIOR TO ADDITIONAL STEP-STRESS TESTING (IF REQ'D).

20. DISPOSITION OF ITEM IF NOT REWORKED
21. AUTHORIZATION BY S.D. Mueller — ORG. CODE 1A 72 30 — DATE 03/13/92

REWORK & RETEST

22. LIST BELOW ALL PARTS REPLACED, REPAIRED OR ADJUSTED

(A) CIRCUIT SYMBOL	(B) PART NUMBER	(C) S/N	(D) MANUFACTURER	(E) DEFECT	(F) REWORK ACTION TAKEN	(G) RECEIVING LOT NO	(H) APPROVED PARTS YES	(H) APPROVED PARTS NO	PRI. FAIL.	DO NOT USE
A4-C4	M39003-01-2255			SOLDER FLOW, SHORT	CLIP LEAD					

23. OTHER REWORK ACTION
RUN VERIFICATION TEST TO CONFIRM DEFECT C4 (Current and I&Q-bit tests).

24. REWORKED BY — ORG. CODE
25. RETESTED BY S.D. Mueller 03/15/92 (SSG 92-005) — ORG. CODE 1A 72 30
26. RETEST RESULTS APPROVAL S.D. Mueller — DATE 03/15/92
27. RETEST RESULTS. REPAIRED ITEM IS ACCEPTABLE FOR ☐ UNRESTRICTED USE ☒ RESTRICTED USE ☐ NOT ACCEPTABLE (EXPLAIN IN BLOCK 30)
28. DISPOSITION OF ITEM AFTER RETEST
29. [illegible]

NO. Z 7390

ENGINEERING

30. CAUSE OF FAILURE - COMMENTS (IF ANALYSIS NOT PERFORMED EXPLAIN)

A4-C4 CAPACITOR IS DEFECTIVE CAUSING SHORT CIRCUIT DUE TO INTERNAL SOLDER FLOW.
REMOVING C4 FROM CIRCUIT CORRECTED -5V SUPPLY LINE SHORT CITED. TEST VERIFIED AS PASS.
C4 RATED AT +125°C / 10VDC AND WAS EXPOSED TO +150°C / -7.0VDC AT LEVEL 10 STRESS.

31. BASIC CAUSE OF TROUBLE FAILURE (SELECT FROM BLOCK I ON REVERSE SIDE): ENVIRONMENTAL EFFECTS
32. SIGNATURE S.D. Mueller (SSG 92-005) — ORG. CODE 1A 72 30 — DATE 03/15/92
33. CORRECTIVE ENGINEERING ACTION TAKEN (IF NONE, LIST REASONS / CONCLUSIONS): DOCUMENT FOR ACCELERATED STEP-STRESS APPROACH REF ENGR'G NOTEBOOK (IDC# 92/1A72 30/005).

REF. DOCUMENT IMPLEMENTING CORRECTIVE ACTION (EO, ECR, ETC.) IS: NO.
34. SIGNATURE — ORG. CODE — DATE

11020 CS MAR 66

USE TFR CONTINUATION SHEET IF ADDITIONAL SPACE IS NEEDED

FOR RELIABILITY ANALYSIS AND FOLLOW-UP SEE REVERSE SIDE OF COPY 4.

Z 733

1

HUGHES AIRCRAFT
GROUND SYSTEMS GROUP

1377B44 34A141 REF. NO. 401983

MODEL LEVEL

HISTORICAL RECORD TAG

SYST. NOMEN.

PART OR ASSEMBLY NAME: R/T MODULE
PART OR ASSEMBLY NO.: [redacted]-103
LTR.CHANGE

PLANNING CHANGE #
DEPT.ORIGINATED
[redacted] NO.
HAC MFG.SERIAL NO.

EFFECTIVE AMENDING DOCUMENTS: ~~1326 LTR 220006~~
W/O NO.
SERIAL NO. 993

ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
			TUU	
		9/23/91	Passed Synth. Tests & Detector Staircase tests	9/23/91
	GSG 92466 TEST	OCT 5 91	T TUU PRE TEMP VERIFICATION COMPLETE	OCT 5 91
	GSG 92466 TEST	OCT 14 91	T TUU 6 CYCLES OF TEMP SCREEN COMPLETE	OCT 14 91
			TUU	
		10/31 91	Post Temp Functional test complete	10/31/91
		03/13/92	VISUAL INSPECTION FOLLOWING A STEP-STRESS TEST	03/13/92
ENGR	NOTE		UUT STEP-STRESS TESTED 03/12/92 THRU 03/13/92 TO LEVEL 10 AND INCURRED FAILURE. DETECTOR -5V SUPPLY LINE SHORTED TO GROUND. SEE TFR# Z7390. REFERENCE TEST PLAN PER CDR# J003-001 OF CONTRACT F30602-89-D-0100/009.	GSG 92466 TEST 03/13/92
	GSG 92466 TEST		03/15/92 CLIPPED A4-C4 CAPACITOR LEAD AT -5V SUPPLY SIDE & VERIFIED C4 SHORTED WITH OHMETER. RAN BOTH CURRENT & I/Q-BIT TESTS AND VERIFIED UNIT IS PASSING. C4 DEFECT VERIFIED.	GSG 92466 TEST 03/15/92
	GSG 92466 TEST		03/15/92 BAG & TAG PART REMOVED AFTER PHOTO	GSG 92466 TEST
	GSG 92466 TEST		03/15/92 REPLACE A4-C4 (M39003-01-2255) & RE-ALIGN DETECTOR PRIOR TO FURTHER STRESS TEST'G	

FORM NO. 4932-03 REV. 11-89

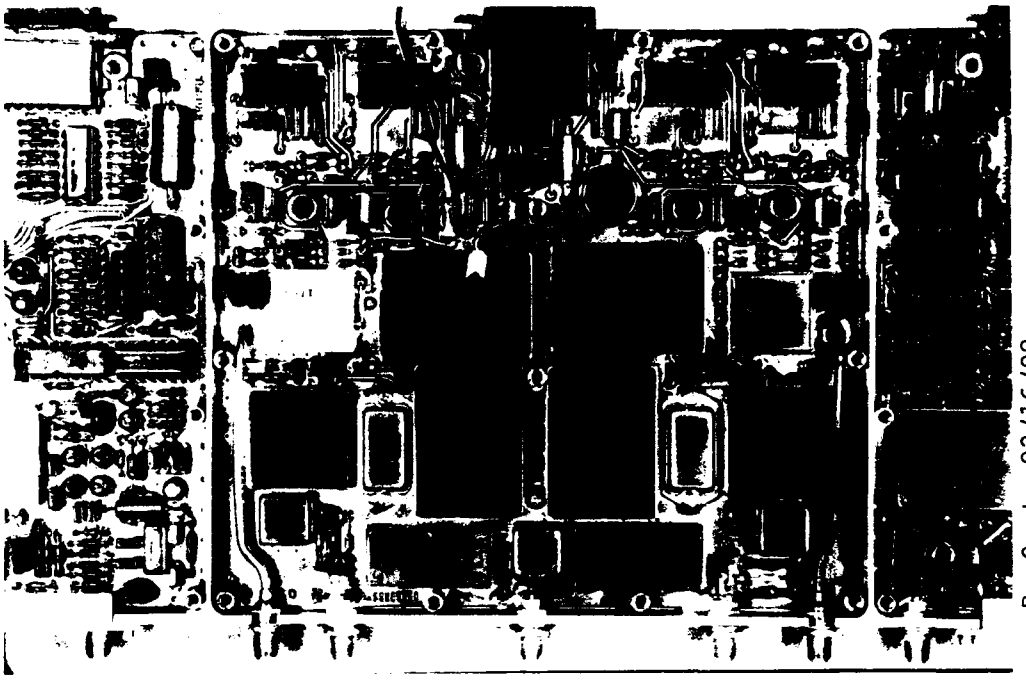
(CONTINUED OTHER SIDE)

MSN 0933

ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
	GSG 92466 TEST	03/16/92	SENT UUT TO DPA LAB FOR X-Y PHOTO C4.	03/16/92 GSG 92466 TEST

FAILURE ANALYSIS DATA SHEET
STEP – STRESS TEST ATTACHMENT 1 of 4

MSN 0993 ASSY A4
ENGR L.D. Mueller DATE 03/92



R. Cantu 03/16/92

A4 DETECTOR; FAILURE LEVEL 10 (+150°C, ±7.0V, ±18.0V)



K.G. Mohr 03/16/92
X4 Magnification

A4-C4 TANTALUM CAPACITOR FAILURE;
SOLDER FLOW RESULTING IN -5V SUPPLY SHORT

FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 2 of 4	MSN 0993 ASSY A2, A3, A4 ENGR L.D. Mueller DATE 03/13/92

GSG 92466 TEST

TFR# Z7390; HRT# 401983

VISUAL ASSEMBLY INSPECTION NOTES:

A2 SYNTHESIZER (S/N 1909) No Attachment necessary.

1 The PWB is an older board and uses green solder mask which is covered with conformal coating. Stresses to LEVEL 10 has discolored the conformal coating to a light caramel brown overall.

2 Components U9, U10, and U11 are void of conformal coating on top of case, but are coated on sides and exposed pins.

3 Cracked and peeling coating found on U8 top surface. Cracked coating on C9.

A3 SYNTHESIZER (S/N 1955) No Attachment necessary.

4 Stresses to LEVEL 10 has discolored the conformal coating to a light caramel brown overall.

5 Components U7, U10, and U11 are void of conformal coating on top of case, but are coated on sides and exposed pins.

6 Chipped conformal coating on C19 case.

7 PWB surface is dirty in area bounded by U9, U7 and edge of PWB.

A4 DUAL DETECTOR (S/N 0559) See Attachment detail.

8 Stresses to LEVEL 10 have discolored conformal coating to a light caramel brown.

9 Excessive test probe marks found at R11. Existed before Step-Stress test.

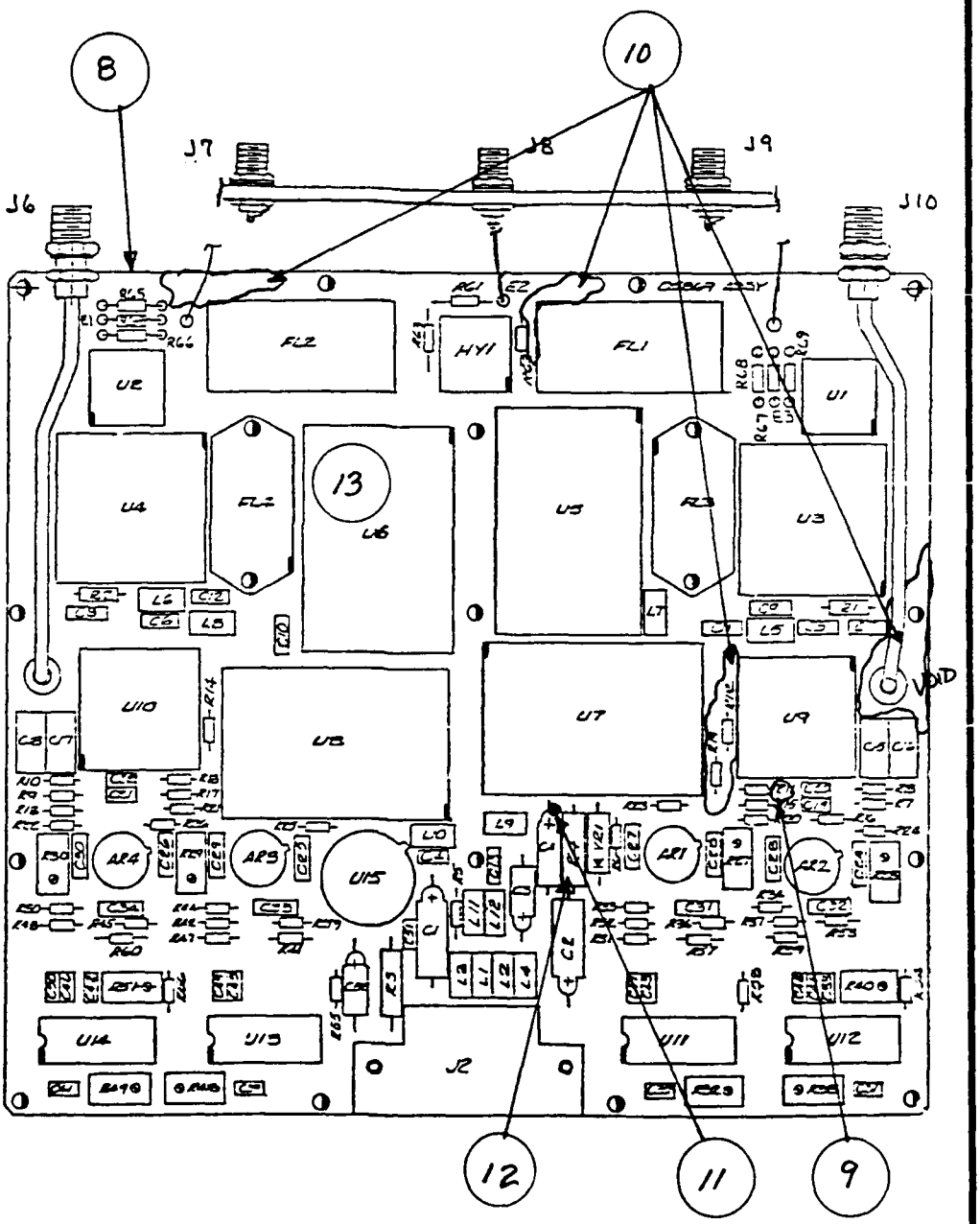
10 Voids in conformal coating in area shown. Some peeling exists.

11 Solder ball formed at positive terminal of C4. Solder flowed from within case.

12 Body of R4 has changed from black overall to show some patches of ashen grey from heat. Diode VR1 appears unaffected.

13 Component U6 is void of conformal coating on top of case..

FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 3 of 4	MSN 0993 ASSY A4 (0559) ENGR D Mullin DATE 03/13/92



FAILURE ANALYSIS DATA SHEET

ATTACHMENT 4 of 4

UUT Serial Number (enter MSN): 0993
HEN#41983; TREX 27390
Analysis Date: 03/15/92
Engineer: (Name & stamp below) J.D. Mueller GSG 92466
Test Conducted at Room Temperature
SPECIAL CONDITIONS: -5V Supply line capacitor C4 clipped away from circuit to allow testing. (Photos still required C4 not disturbed)

DETECTOR VOLTAGE SETTINGS:

Supply Voltages: + 5 Volts dc: +5.00 (Vdc) - 5 Volts dc: -5.00 (Vdc)

+15 Volts dc: +15.00 (Vdc) -15 Volts dc: -15.08 (Vdc)

Aux. - 5 Volt Setting: -5.1089 (Vdc) R_{LOAD} Voltage: -5.1452 Vdc)

DETECTOR CURRENT MEASUREMENTS:

UUT Currents: + 5 Volts dc: 139.8 (mA) - 5 Volts dc: 48.9 (mA)

+15 Volts dc: 60.3 (mA) -15 Volts dc: 303.8 (mA)

DETECTOR DIGITAL OUTPUT MEASUREMENTS:

Rcv Sig Input	I & Q -Bits	DETECTOR 1 t (usec) / T (usec)	DETECTOR 1 Duty Cycle (percent)	DETECTOR 2 t (usec) / T (usec)	DETECTOR 2 Duty Cycle (percent)	COMMENTS
Channel 00: Settings: Synth Sig (J7 & J9) = 921 MHz; Rcv Sig (J8) = 607.35 MHz at 0 to -75 dBm						
0 dBm	I > 0	4.80/9.60	50.0	4.56/9.60	47.5	8 div @ 1.20 μsec/div
	I > Q	4.68/9.60	48.8	4.68/9.60	48.8	
	I + Q > 0	4.80/9.60	50.0	4.80/9.60	50.0	t / T
	Q > 0	4.68/9.60	48.8	4.68/9.60	48.8	
-75 dBm	I > 0	5.04/9.60	52.5	4.92/9.60	51.2	
	I > Q	4.80/9.60	50.0	4.80/9.60	50.0	Same
	I + Q > 0	4.92/9.60	51.2	5.04/9.60	52.5	
	Q > 0	4.92/9.60	51.2	5.04/9.60	52.5	Alignment & loss inputs could be improved by adjustment
Channel 50: Settings: Synth Sig (J7 & J9) = 684 MHz; Rcv Sig (J8) = 370.35 MHz at 0 to -75 dBm						
0 dBm	I > 0	4.80/9.60	50.0	4.80/9.60	50.0	
	I > Q	4.68/9.60	48.8	4.80/9.60	50.0	
	I + Q > 0	4.80/9.60	50.0	4.80/9.60	50.0	same
	Q > 0	4.68/9.60	48.8	4.68/9.60	48.8	
-75 dBm	I > 0	4.92/9.60	51.2	4.92/9.60	51.2	
	I > Q	4.68/9.60	48.8	4.92/9.60	51.2	
	I + Q > 0	5.04/9.60	52.5	5.16/9.60	53.8	Same
	Q > 0	4.92/9.60	51.2	4.92/9.60	51.2	A little more noise sensitivity w/ C4 gone.

STEP-STRESS TEST

FAILURE ANALYSIS NOTEBOOK
Unit Under Test: MSN 1030

FAILURE SUMMARY

FAILURE LEVEL: *PASSED LEVEL 10 (NON-CHARGEABLE LEVEL 11)

FAILURE MODE(S): TESTED BEYOND DESIGN LIMIT. VCO HYBRID, A3-U11, SHORTED INTERNAL PIN 7 RESULTING IN -15 VOLT SUPPLY LINE SHORT. NUMEROUS SOLDER BALLS FORMED.

AFFECTED PART(S): A3-U11; P/N 728000-174.
ALSO AFFECTED MAY BE A3-U1 THRU U6, U8 & U10.

FIXED STEP DWELL TIME: 1 HOUR

FIXED RAMP & STABILIZATION: 30 MINUTES

TOTAL ELAPSED TIME TO FAILURE:
(FROM END OF LEVEL 0 DWELL)
20 HOURS: 46 MINUTES THRU LEVEL 10
FAILURE FREE
24 HOURS: 21 MINUTES THRU LEVEL 11

ANOMALY TEST TIME:
(INCLUDED IN TOTAL ABOVE)
5 HOURS: 46 MINUTES THRU LEVEL 10
7 HOURS: 26 MINUTES THRU LEVEL 11

*THIS UNIT PASSED TEN LEVELS OF STEP-STRESS TESTING. THE UNIT WAS STEPPED TO LEVEL 11 TO VALIDATE THE SELECTED DESIGN LIMITS OF THE TEST EFFORT WHICH WERE ESTABLISHED AT LEVEL 10. DESIGN LIMITS WERE CONFIRMED.

PRESS HARD - USE BALLPOINT PEN

HUGHES
HUGHES AIRCRAFT COMPANY

STEP-STRESS TROUBLE & FAILURE REPORT

1. PROJECT NAME: STEP-STRESS

FAIL CLASS	TEST TYPE	TEST ENV.	FAIL CAUSE	RELEV.

NO. Z7386

FAM CODE | SYST CODE

2. THIS REPORT COVERS A ☐ REWORK ACTION ☐ TROUBLE ☒ FAILURE

ORIGINATOR

3. SYSTEM/SUBSYSTEM NAME: T/R MODULE | P/N: (part number - 103) | S/N: 1030
4. TIMER/COUNTER READINGS: TIME ELAPSED 25:31 HOURS | LEVEL 11 TO 10 CYCLES
5. DATE: 01 (MO) 23 (DAY) 92 (YR)
35. REFERENCES
6. REPORTING FACILITY: STEP-STRESS TEST (C/: L. Tsukamoto)
7. REPORTED BY: S.D. Mueller S.D. Mueller 01/31/92 | ORG. CODE: 1A, 72, 30
OPERATING LOG NO
8. TROUBLE/FAILURE OBSERVED WAS: (TEST CONDITIONS, SYMPTOMS, SEVERITY, ETC., INCLUDING "IS" AND "SHOULD BE" DATA)
TFR CONTINUATION USED ☐

-15V supply short A3 Synth (J12-side). Occurred 25 minutes into decreasing ramp from Level 11 (+145°C Chamber air, +160°C Flange, ±7.2V, ±18.3V, +151°C Strt) to Level 10 (+140.5°C Chamber air, +148.5°C Flange, +143°C Strt, w/ voltages yet unchanged from Level 11) 5 minutes prior to stabilized dwell. -15V total supply @ -2.23 Vdc, 3.94 A was 632 mA at Level 11. Initial visual: Solder balls on various component leads.

9. TROUBLE/FAILURE OCCURRED DURING: (A) ☒ ASSIGNED USE R&D (B) ☐ SCHEDULED MAINTENANCE (C) ☐ UNSCHEDULED MAINTENANCE (D) ☐ PRE-FLIGHT OR CURSORY CHECK
10. ACTION TAKEN TO CORRECT TROUBLE FAILURE: (A) ☐ REPLACED ITEM (COMPLETE BLOCKS 11 - 13) (B) ☐ REPAIRED ITEM (COMPLETE BLOCKS 14 - 29)

11. ITEM REPLACED NAME	P/N	S/N	12. ITEM INSTALLED NAME	P/N	S/N	13. DISPOSITION OF REPLACED ITEM

VERIFICATION

14. WERE OTHER TROUBLES/FAILURES, NOT RELATED TO ORIGINAL NOTED? (A) ☐ NO (B) ☒ YES — LIST ON NEW TFR - TFR NO. _____
15. WAS REPORTED TROUBLE/FAILURE VERIFIED? (A) ☒ YES (B) ☐ NO (CHECK 18 (B) AND EXPLAIN)

16. FAILED ITEM NAME	P/N	S/N	REF. DESIG.	MANUFACTURER
VOLTAGE CNTLD OSCILLATOR	728000-174 03/11/92	1205	A3-U11	31091 (D/C 8824)
17. NEXT HIGHER ASSY: NAME	P/N	S/N	REF. DESIG	MANUFACTURER
SYNTHESIZER, CKT CARD ASSY		2589	A3	05869

18. (A) ☒ REWORK REQUIRED IS (B) ☐ REWORK IS NOT REQUIRED BECAUSE
19. VENDOR REWORK ANALYSIS IS REQUIRED ☐ ITR _____ C.A.R. _____

TROUBLE SHOOT -15V COMPONENTS: C9, L4, C15, U11 (pins 4,7,16,17,22), U12 (pin 4). ISOLATE AS REQUIRED TO VERIFY. BAG & TAG PARTS REMOVED & RECORD ON HRT# 401988. S.D. Mueller 03/09/92

20. DISPOSITION OF ITEM IF NOT REWORKED
21. AUTHORIZATION BY | ORG. CODE | DATE

REWORK & RETEST

22. LIST BELOW ALL PARTS REPLACED, REPAIRED OR ADJUSTED

(A) CIRCUIT SYMBOL	(B) PART NUMBER	(C) S/N	(D) MANUFACTURER	(E) DEFECT	(F) REWORK ACTION TAKEN	(G) RECEIVING LOT NO.	(H) APPROVED PARTS YES	(H) APPROVED PARTS NO	PRI. FAIL	DO NOT USE
A3C9	M39003-01-2804		MIL-C	NONE (IS GOOD)	CLIP LEADS (REMOVED)	05/09/92				
A3C15	M39014-01-1473		MIL-C	NONE (IS GOOD)	DESOLDER 1-LEAD (GND)	03/11/92				
A3L4	712083-1		05869	NONE (IS GOOD)	DESOLDER 1-LEAD	03/11/92				
A3U11	728000-174	1205	31091	-15V SHRT PIN 7	ISOL PINS / REMOVED	04/08/92				

23. OTHER REWORK ACTION: TRACE FROM U11 (-15V LINE) TO U12 PIN 4 (NEXT TO C15) CUT TO ISOLATE PARTS. PRIOR TO MORE STEP-STRESS TESTING: REPLACE C9, RESOLDER C15 & L4, SRI TRACE AT C15/U12, AND SRI PADS AT U11 (EYELETS). ADDITIONAL TESTING REQUIRED TO VERIFY U8 & SOLDER-BALLS ALL.

24. REWORKED BY | ORG. CODE
25. RETESTED BY S.D. Mueller 03/11/92 | ORG. CODE 1A, 72, 30
26. RETEST RESULTS APPROVAL Steven S. Mueller | DATE 04/08/92
27. RETEST RESULTS: REPAIRED ITEM IS ACCEPTABLE FOR ☐ UNRESTRICTED USE ☐ RESTRICTED USE ☒ NOT ACCEPTABLE (EXPLAIN IN BLOCK 30) (92463)
28. DISPOSITION OF ITEM AFTER RETEST: REWORK & ADDITIONAL TEST REQD
29. Q.C.

NO. Z7386

ENGINEERING

30. CAUSE OF FAILURE - COMMENTS (IF ANALYSIS NOT PERFORMED EXPLAIN)
SUPPLY LINE -15V ELECTRICALLY SHORTED BY VCO HYBRID, A3U11, INTERNAL TO PIN 7. LOCATING FAILURE BY ISOLATING PARTS FROM SUPPLY LINE (1) REMOVED C9, (2) REMOVED SOLDER BALLS @ L4, (3) LIFTED C15, (4) REMOVED SOLDER BALL L4 (REVERSE SIDE), (5) CUT TRACE C15 TO U12 (ISOL U11 FROM U12), (6) LIFT L4, (7) ISOLATE EACH PIN OF U11 (PIN 7 SHORT CKT). IN ADDITION: SOLDER BALLS HAVE FORMED AT U1 THRU U6, U8 & U10(IC'S). IC A3-U8 VISUALLY APPEARS TO BE AFFECTED BY STRESS EXPOSURE & MAY BE ANOTHER FAILURE NOT OBSERVED AT TEST.

31. BASIC CAUSE OF TROUBLE/FAILURE (SELECT FROM BLOCK I ON REVERSE SIDE) ENVIRONMENTAL EFFECTS (92463)
32. SIGNATURE Steven S. Mueller | ORG. CODE 1A 72 30 | DATE 04/08/92
33. CORRECTIVE ENGINEERING ACTION TAKEN (IF NONE, JUSTIFY) - CONCLUSIONS
DOCUMENT FOR EVALUATION OF ACCEL STEP-STRESS TEST APPROACH REF ENB (IDC#).
MSN 1023 WAS ALSO EVALUATED FOR CONFORMAL COATING DISCOLOR DUE TO TEMPERATURE/TIME EXPOSURE PER IDC# 92/1H4323-022 DATED 14 FEB 92. NO DEGRADATION TO COATING FOUND, MSN 1023 TO LEVEL 10 EXPOSURE. MSN 1030 WAS EXPOSED LONGER & TO LEVEL 11 STRESS. IT IS NOTED THAT MSN 1023 & THIS UUT, MSN 1030, DID NOT HAVE COMPONENT FAILURES THRU LEVEL 10.

REF. DOCUMENT IMPLEMENTING CORRECTIVE ACTION (ECO, ECR, ETC.) IS NO. IDC#92/1A72.30/005
34. SIGNATURE STOP AT LEVEL 10 EXPOSURE | ORG. CODE 1A, 72, 30 | DATE 4/8/92

HRT# 401[illegible]
MSN 103[illegible]

HUGHES AIRCRAFT CO.
GROUND SYSTEMS GROUP

MODEL LEVEL: 1377B44B4A1A1 REF. NO. 401988

HISTORICAL RECORD TAG

SYST. NOMEN.

PART OR ASSEMBLY NAME | PART OR ASSEMBLY NO. 103 | LTR.CHANGE

PLANNING CHANGE # | DEPT.ORIGINATED | [redacted] NO. | HAC MFG.SERIAL NO.

EFFECTIVE AMENDING DOCUMENTS 1326-LTB-220001 | W/O NO. | SERIAL NO. 1030

ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
			TOO /1/A2	GSG 92436 TEST
		9/20/91	J4 fail 1.5MHz sideband test.	
			TOO /2/A3 & A4	9/20/91
		9/25/91	Passed Synth & Detector sidecar tests	
			TOO /A2/	
		10/10/91	Trim white wire & readjust wire. Connect to J4	
			TOO	
		10/14/91	Syn/Det functional test complete	10/14/91
			Complete 6 Cycle temp screen	
		10/25/91		10/25/91
			TOO/1/A2	
		10/29/91	J5 fail Freq Sweep test low power output. Suspect bad FLI	
			TOO/1/A2/FLI/73200 1-1	
		10/30/91	FLI fail VSWR test. Replace FLI	

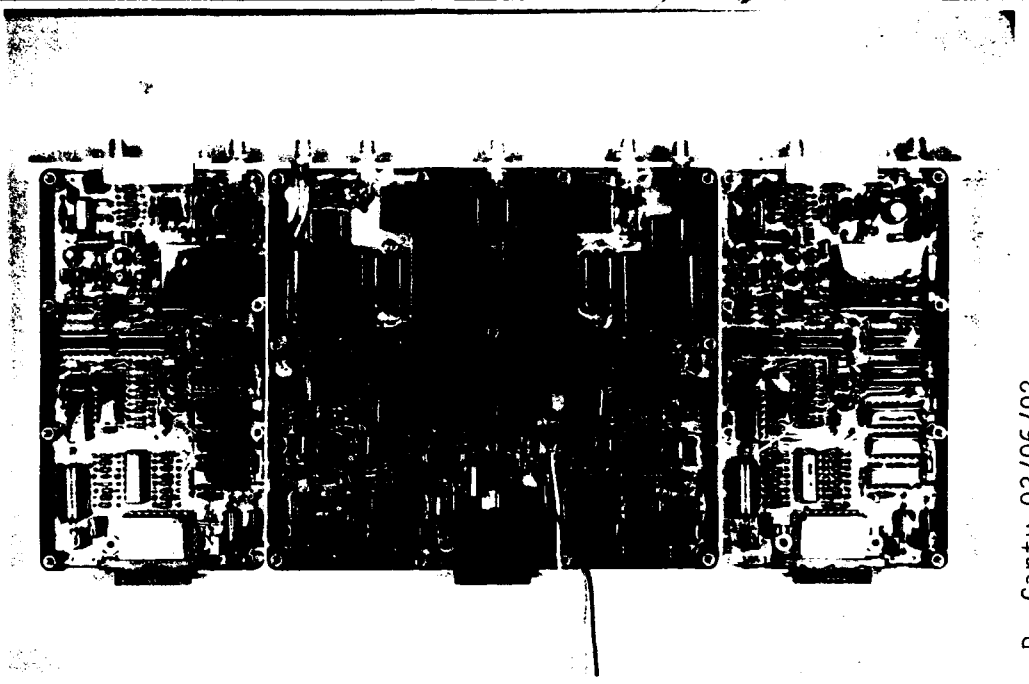
FORM NO. 4932-GS REV. 11-65

CONT. OTHER SIDE

ITEM NO.	ORIG. INSP. STAMP	DATE	DETAILED DESCRIPTION	INSP./TEST ACCEPT.
			TOO	
		10/31/91	Post temp functional test completed.	10/31/91
		01-24-92	Remove cover to visually inspect A3 in completion of STEP-STRESS TEST CONFORMAL COAT DISCOLORED	01-24-92
ENGR	NOTE		UUT STEP-STRESS TESTED 01/22/92 THRU 01/23/92 TO LEVEL 10 AND LEVEL 11. FAILURE OF A3 SYNTH WAS INCURRED WITH -15V SUPPLY SHORTED. SEE TFR# Z7386. REFERENCE TEST PLAN CORL# J003-001 OF CONTRACT F30602-89-D-0100/009.	GSG 92466 TEST 01/23/92
ENGR	NOTE		03-09-92 Sent UUT to be photographed #4. Suspect -15V short of A3 caused by C9, U11, U11 or U12. C15 using this voltage. Remove C9 (clipped leads) & solder balls at both pads of L4. C9 is NOT SHORTED — BAG & TAG. L4 should be okay. FAILURE STILL PRESENT SHORT J3 pin 14 to ground. Work done top side of CKT card.	GSG 92466 TEST 03/09/92
			03/11/92 Break strip hardware & remove A3 from chassis. Found solder ball at close side of L4 but lips not shorting -15V. All traces are clear also. Desoldered GND lead of C15 to isolate. C15 was not shorted. Cut trace from U12 pin 4 to C15 to isolate U12 and U11 (pins 47, 14, 17, 22 common). U12 pin 4 is >2MegΩ to GND & clear. Desolder one side of L4 & isolate. Problem is with U11. U11 Remove Later is required. Reinstall in chassis	GSG 92466 TEST 03/11/92
			04/08/92. REMOVE A3 SYNTH CCA FROM CHASSIS AGAIN. REMOVE U11 VCO HYBRID BUT ISOLATE -15 VOLT PINS ONE AT A TIME. PIN 4 IS GOOD; PIN 7 IS SHORT & PAD LIFTED & NEEDS SRT; PIN 17 IS GOOD >5.5KΩ; PIN 16 IS GOOD >5.4KΩ & PAD LIFTED & NEEDS SRT; PIN 22 IS GOOD 25KΩ. DESOLDER REMAINING LEADS, REMOVE A3-U11 BAG & TAG	GSG 92466 TEST 04/08/92

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FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 1 of 7	MSN 1030 ASSY A2,A3,A4 ENGR [signature] DATE 03/92



R. Cantu 03/06/92

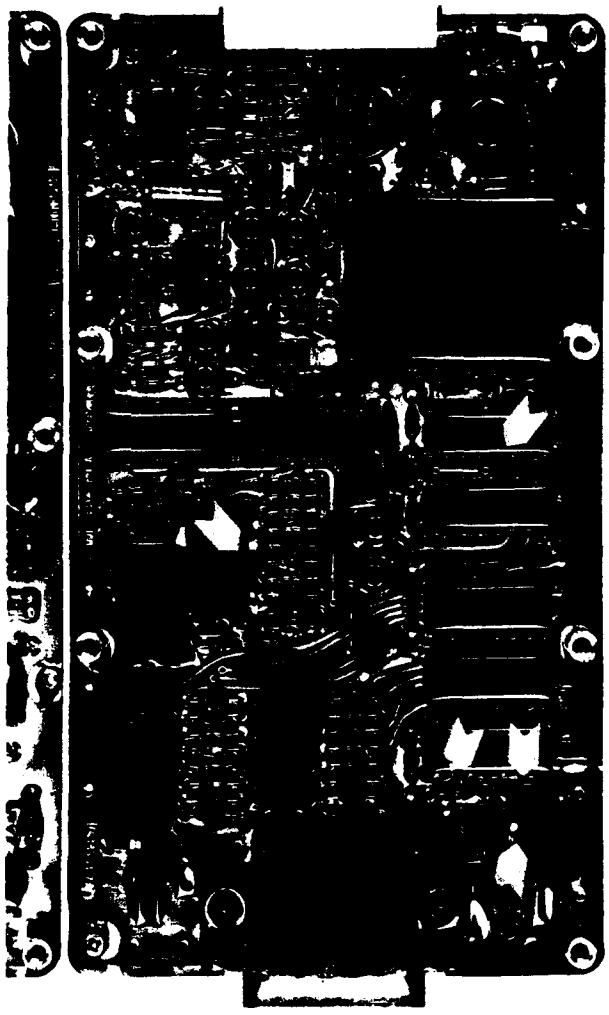
A2 (Lt) & A3 (Rt) SYNTHESIZERS, A4 (Mdl) DETECTOR
FAILURE LEVEL 11 (+158°C, +7.2V, +18.3V); PASSED LEVEL 10



K.G. Mohr 03/09/92 X4 Magnification

A4 DETECTOR- SOLDER BALLS FORMED C3, C4 & R6
COATING BAKED AWAY R4 & VR1

FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 2 of 7	MSN 1030 ASSY A3 ENGR A.M. Muller DATE 03/92

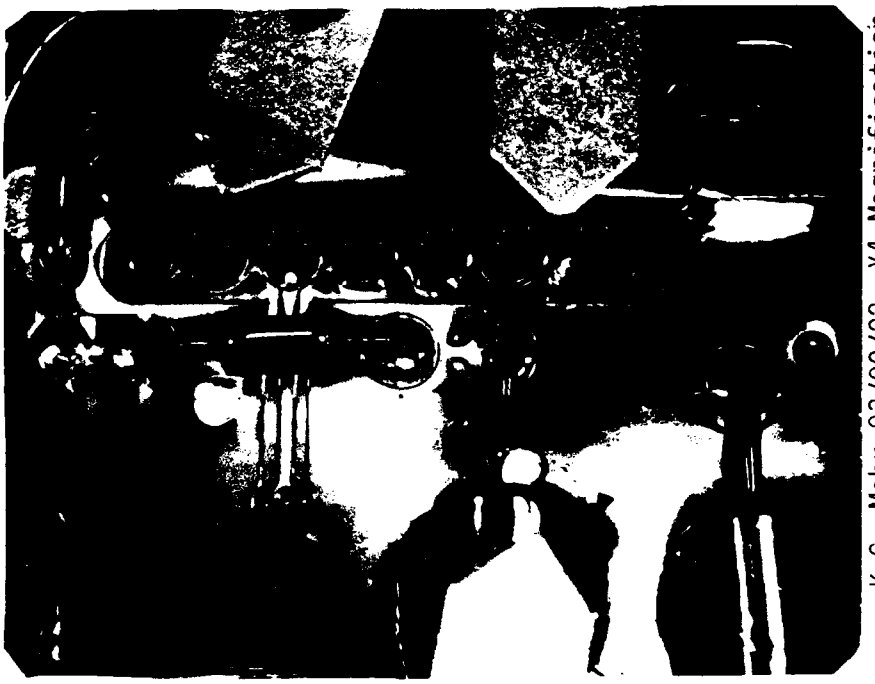


R. Cantu 03/06/92

A3 SYNTHESIZER FAILED LEVEL 11;
VOLTAGE CONTROLLED OSCILLATOR (VCO) HYBRID A3-U11, SHOWN UPPER RIGHT, HAD SHORTED PIN 7 RESULTING IN -15V SUPPLY LINE SHORT. NUMEROUS SOLDER BALLS FORMED THROUGHOUT THE CIRCUIT CARD ASSEMBLY.

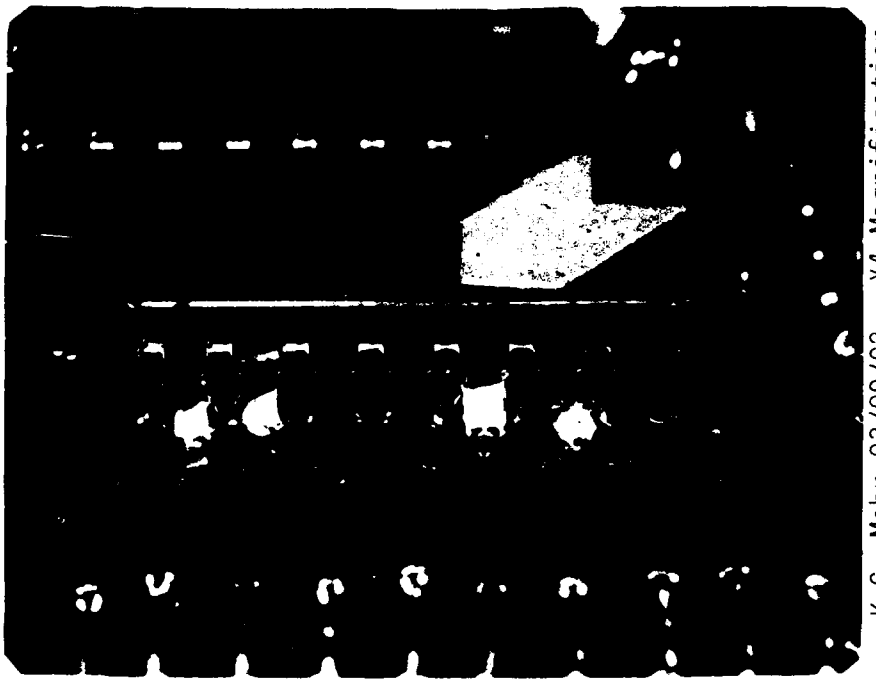
FAILURE ANALYSIS DATA SHEET
STEP – STRESS TEST ATTACHMENT 3 of 7

MSN 1030 ASSY A3
ENGR D. Mullen DATE 03/92



K.G. Mohr 03/09/92 X4 Magnification

SOLDER BALLS FORMED A3-C4 & A3-U1 OF SYNTHESIZER



K.G. Mohr 03/09/92 X4 Magnification

SOLDER BALLS FORMED LEVEL 11 BRIDGING PINS OF A3-U8

FAILURE ANALYSIS DATA SHEET
STEP – STRESS TEST ATTACHMENT 4 of 7

MSN 1030 ASSY A2, A3, A4
ENGR. [signature] DATE 01/24/92

TFR# Z7386; HRT# 401986

VISUAL ASSEMBLY INSPECTION NOTES:

A3
~~A2~~ SYNTHESIZER (S/N 2589) See Attachment detail.

1 Conformal coating stresses to LEVEL 11 and is light to dark caramel brown over entire PWB. U11 is the darkest and has turned a reddish brown color. Overall, conformal coating is fairly uniform.

2 Conformal coating is missing in the area of E1 through E3, probably due to prior rework in this area.

3 Solder balls formed on or at:

A U10 pins 3 and 14.
B Lead of R17.
C Lead of R56.
D U6 pin 14.
E U5 pins 14 and 15.
F U3 pins 7 and 8.
G U1 pins 2, 11, and 17.
H Positive lead of C9 and has one developing under case as well.
I On trace from U10 pin 14 to C4.
J U8 pins 2, 3, between 5 and 6, 7, 13, 15, and 16.
K Trace with feed-thru hole going to R near Q2.
L Lead of R50.
M U4 pin 10.
N U2 pins 7, 10 and 12.
O Lead of R25
P Pass of L4. [signature] 3/9/92. (also reverse side of L4 and at trace to C9 [signature] 3/11/92)

A2
~~A2~~ SYNTHESIZER (S/N 2028) See Attachment detail.

4 Conformal coating stressed to LEVEL 11 is discolored, taking on a dark caramel brown appearance. The coating is darkest at IC's and U11.

5 Conformal coating is missing from the area of E1 thru E3, C13, C17, and R41. This condition existed prior to Step-Stress testing.

A4 DUAL DETECTOR (S/N 0586) See Attachment detail.

6 Pad lifting at E1 of R64.

7 Conformal coating cracked and peeling in areas of prior engineering modification. Coating was touched up in theses areas and exhibit poor bonding to PWB. Part of this area appears void of coating.

8 Conformal coating applied to case of C2 and C4 is peeling.

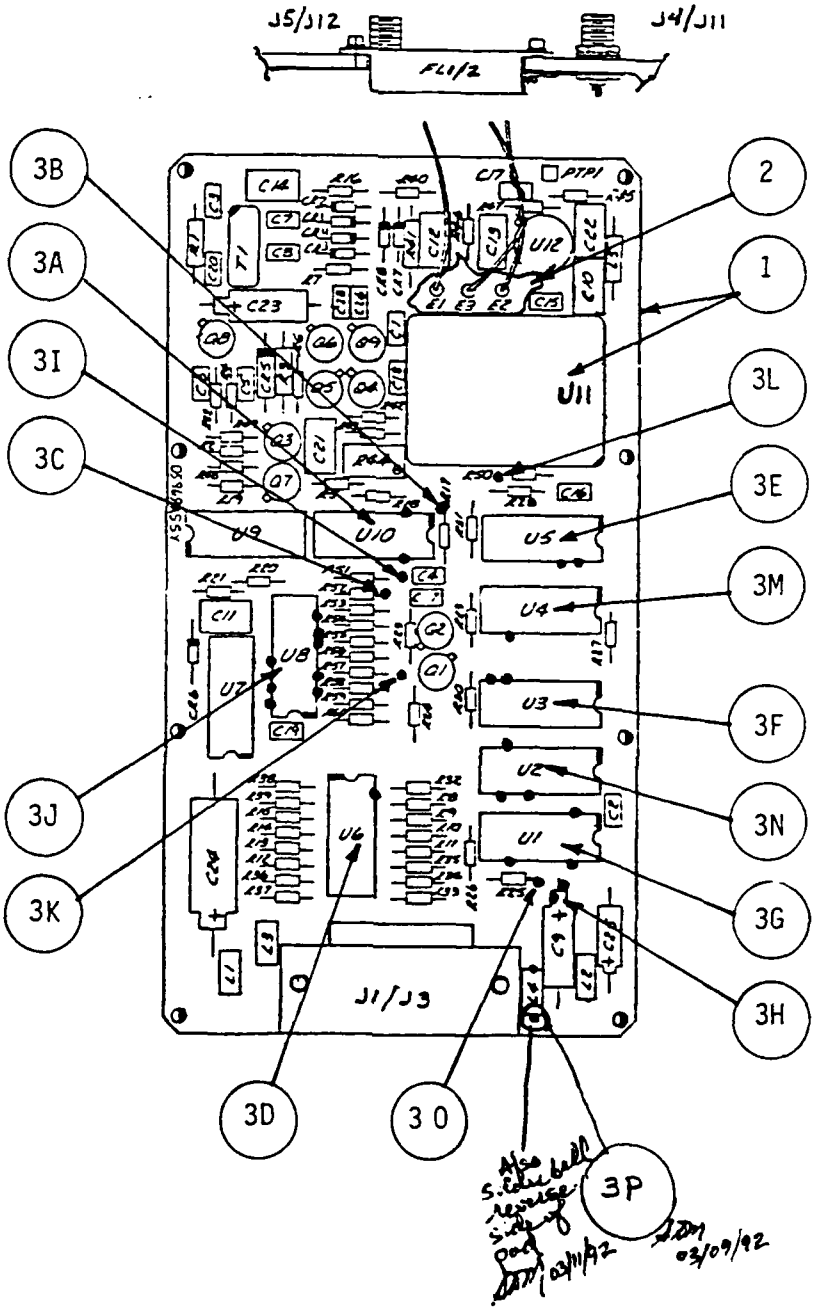
9 Solder balls have formed at:

A Negative lead of C3.
B Negative lead of C4 and exhibits solder flowing.
C Lead of R6.

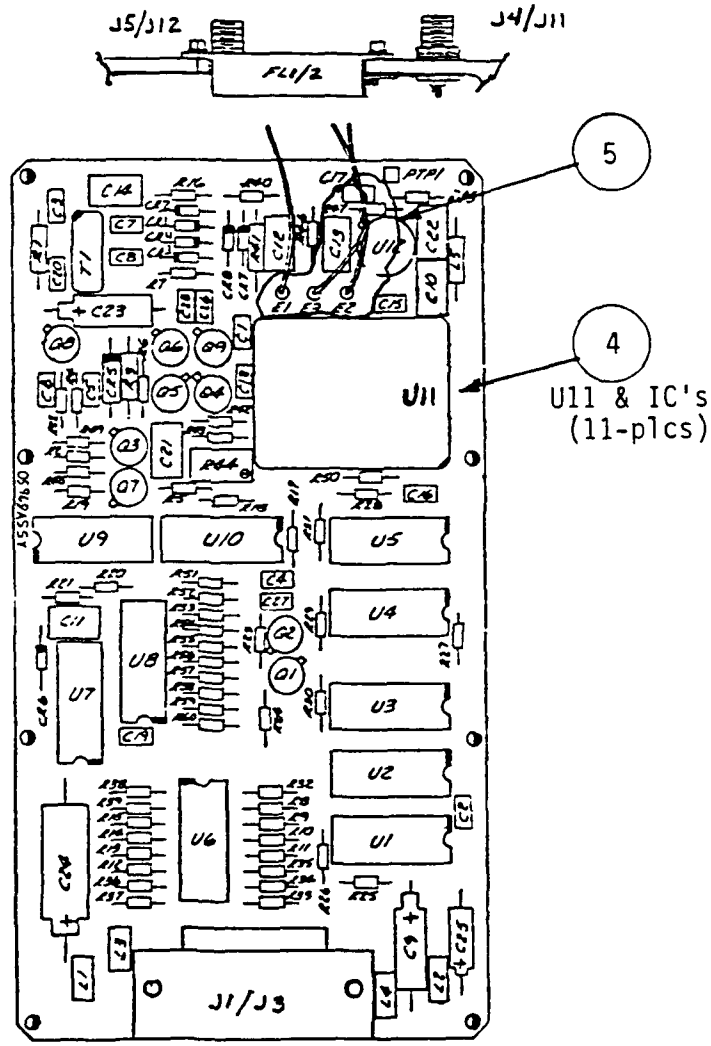
10 Extreme heating has turned parts of R4 and VR1 ashen grey.

11 Excessive test probe marks at R13 existed prior to Step-Stress test.

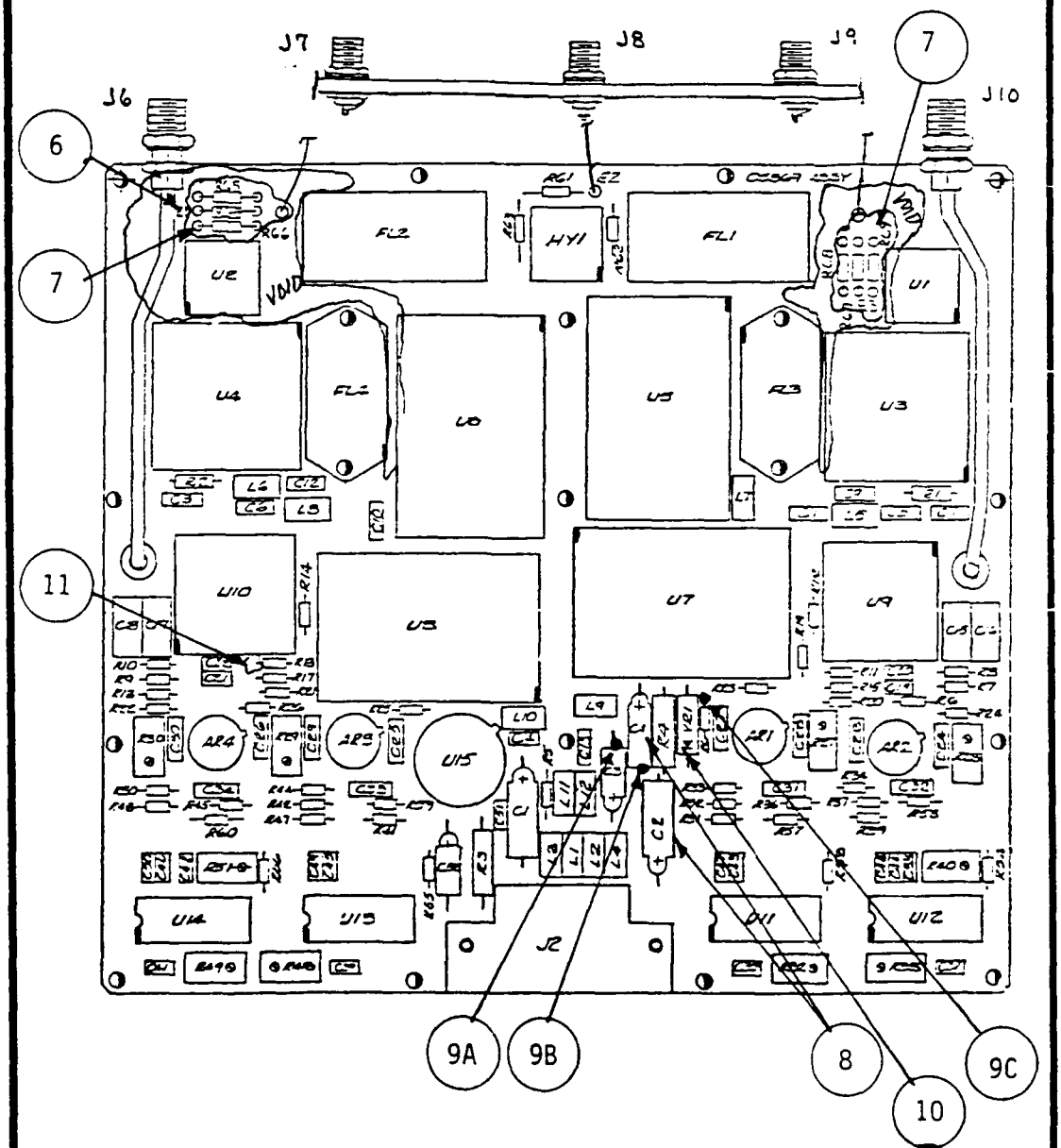
FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 5 of 7	MSN 1030 ASSY A3 (2589) ENGR D.D. Mueller DATE 01/24/92



FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 6 of 7	MSN 1030 ASSY A2 (2028) ENGR D. Mueller DATE 01/24/92



FAILURE ANALYSIS DATA SHEET STEP – STRESS TEST ATTACHMENT 7 of 7	MSN 1030 ASSY A4 (0586) ENGR L.D. Mueller DATE 01/24/92



HUGHES AIRCRAFT COMPANY

INTERDEPARTMENTAL CORRESPONDENCE

TO: **D. Huch** cc: Distribution DATE: 13 February 1992
ORG: 1A-62-XX REF: 92/1A72.30/002

SUBJECT: **Step-Stress Test Units**
Discoloring of Conformal Coating
and Reliability, Post Stress Test

FROM: S. D. Mueller
BLDG: 675 MAIL STA: Z314
EXT: 1-8360 ORG.CODE: 1A-72-30

BACKGROUND: Two (2) out of the seven (7) production R/T modules have been Accelerated Step-Stress tested per the Test & Acceptance Plan. The first unit, MSN 1030, was taken to Level 10 and then Level 11 to reach catastrophic failure. The second unit, MSN 1023, completed Level 10 without failure. Both units tested showed visible discoloring of the conformal coating. The polyurethane coating appears scorched, having a orange-brown color, over the entire unit surface. The appearance is similar to a hot coffee cup being placed upon a coated table and leaving a ring on the furniture's finish. A scrapped circuit board was placed in the thermal chamber with MSN 1023. The board's polyurethane coating began to yellow at the exposure air temperature of Level 9 & Level 10 (+140 °C). The discoloring of the test units is unacceptable to D. Ragle (who is responsible for this hardware), and makes these units depreciate significantly in value.

TASK ASSIGNMENT: Under direction from D. Ragle and D. Huch, engineering was tasks to determine the temperature level where this discoloring would be, at most, minimized to localized areas (allowing spot rework on few component surfaces) or yellowing throughout (also typical of units whose coatings have aged).

ANALYSIS:

R. Patterson (component/material engineer) has tested MSN 1023 and another unit MSN 815 (for comparison) for dielectric strength and coating thickness. The discolored coating of MSN 1023 was found to be acceptable per MIL-SPEC requirements. The unit's polyurethane coating had not carbonized (no burning) and showed no sign of breakdown when subjected to 6000 Volts through its 6 mil thickness. The MIL-SPEC indicates that usage is specified for indefinite operation to +130 °C. Color is not a criteria. D. Hahn (product operations) inspected MSN 1023 and found no defects or imperfections as judged to Hughes workmanship criteria. Again, no requirement for color exists. The exposure of the conformal coating, although in excess of its +130 °C spec, shows no degradation in performance or to its workmanship requirements.

S. Mueller (design & test plan engineer), using the MIL-SPEC +130 °C requirement for operation and the scrapped board's exposure of +140 °C for yellowing, determined that testing of the remaining units would have to be reduced to Step-Stress Level 6 or Level 7 to minimize the discoloring of the polyurethane coating. The attached figures and graphs illustrate these Levels as they apply to the Test & Acceptance Plan for Accelerated Step-Stress Testing.

Component case temperatures will exceed +130 °C at Level 6 (see excerpt Figure 2.3.1). Coating not in direct contact with components will have uniform air temperature exposure of +130 °C by Level 7. At

Level 7, yellowing will have occurred on components due to case temperatures exceeding +140 °C and browning may occur in some locations. The component case temperature information cited was taken from thermocouple data obtained from the Trial Test Runs of 25 November through 27 November 1991 and 17 December 1991. The Trial Test Run of the Step-Stress Test was conducted on a similar unit and provided the basis for the thermal criteria of the Test & Acceptance Plan. This similar unit, MSN -100/349, was not conformally coated and compartment air temperatures will be slightly increased on the -103 configuration units (ie., MSN 1023, 1030, 815, and four others) due to their coating. Above Level 7, browning will continue and be more widespread.

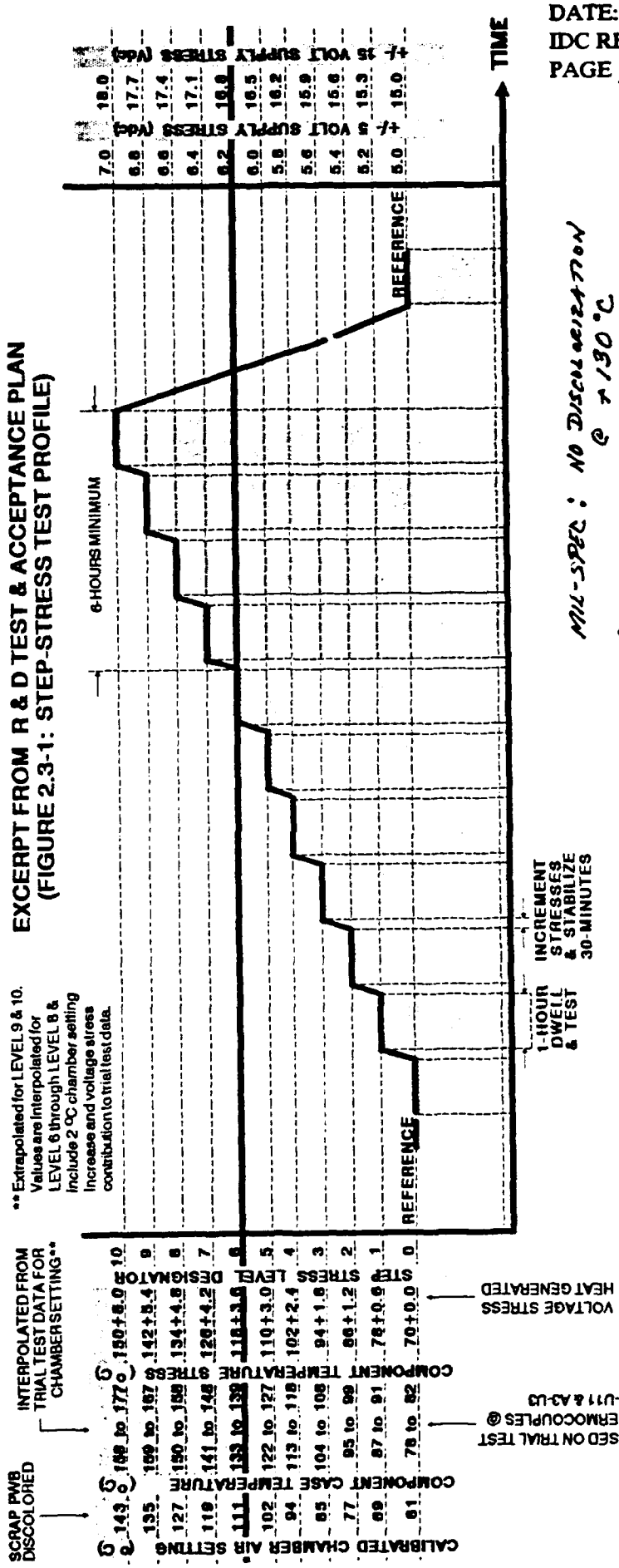
LIMITATIONS ON R & D: Reducing the unit exposure to Level 6 or Level 7 should minimize discoloring of the polyurethane conformal coating on future test units, and alleviate the concerns of D. Ragle and D. Huch. Reduction of the temperature stress will require a change to the Test & Acceptance Plan for future test. Using Level 6 as the maximum stress would only stress 8% of the components to their maximum survival temperature extremes (see excerpt of Figure 2.2-1). With Level 7 used as the extreme, this would increase to include 38% of the components. The original scope of the Test & Acceptance Plan, and the approach guided by the Process Action Team members, was to provide testing up to the units *Design Limit* which at present includes Level 10 and imposes accelerated stress upon 90% of the components. With the reduction of stress to Level 6 or Level 7, we will be repeating the approaches utilized by the prior two test participants (testing only to maximum *operating* specifications rather than *survival* extremes) and contribute little to the research and development of Accelerated Step-Stress Testing.

REMARKS: The browning of the conformal coating of MSN 1023, and likely MSN 1030 (not analyzed), does not indicate a degradation in the ability of the conformal coating to provide its intended function. The question remaining, however, is what the Level 10 stress environment exposure has had upon the component life of these units. By plan, these units were exposed to stresses in excess of their specified operating limits with the intent of subjecting them to extreme stresses that would accelerate failure. These units have not been evaluated, as yet, to determine the extent of damage which may have been sustained during test which could show up during a second pass of the Step-Stress Test or could happen if these units were fielded as production spares in the future. It is recommended that MSN 1023 and 1030 never be used in any situation requiring the same performance reliability as a new production unit.

sdm:sm

Distribution:

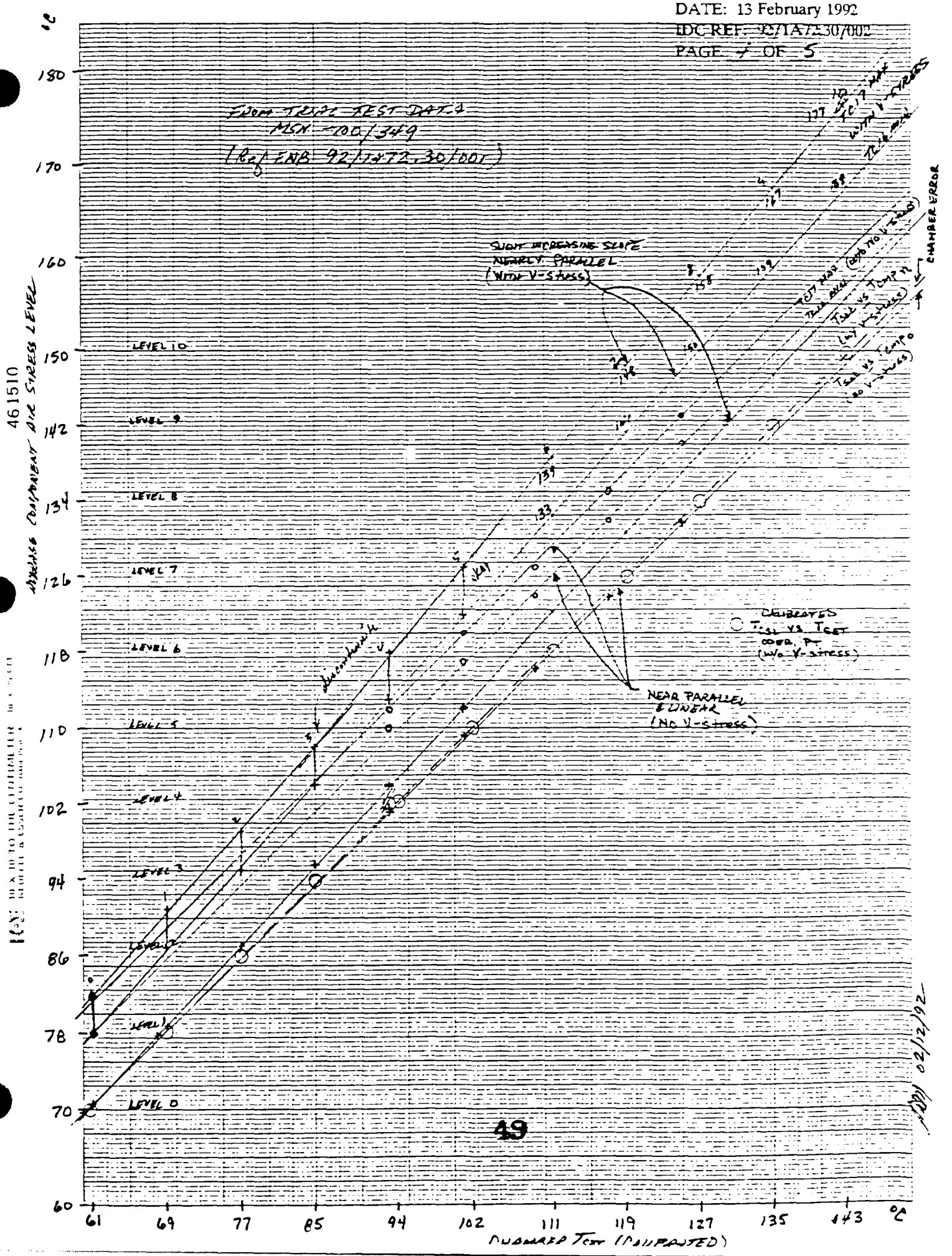
D. H. Ragle
S. R. Burnett
L. E. James
R. F. Patterson
D. T. Hahn
H. W. Homme



MIL-SPEC: NO DISCOLORATION @ +130 °C

SCRAP PWB: SLIGHT YELLOWING @ +140 °C (chamber set @ +143°C)

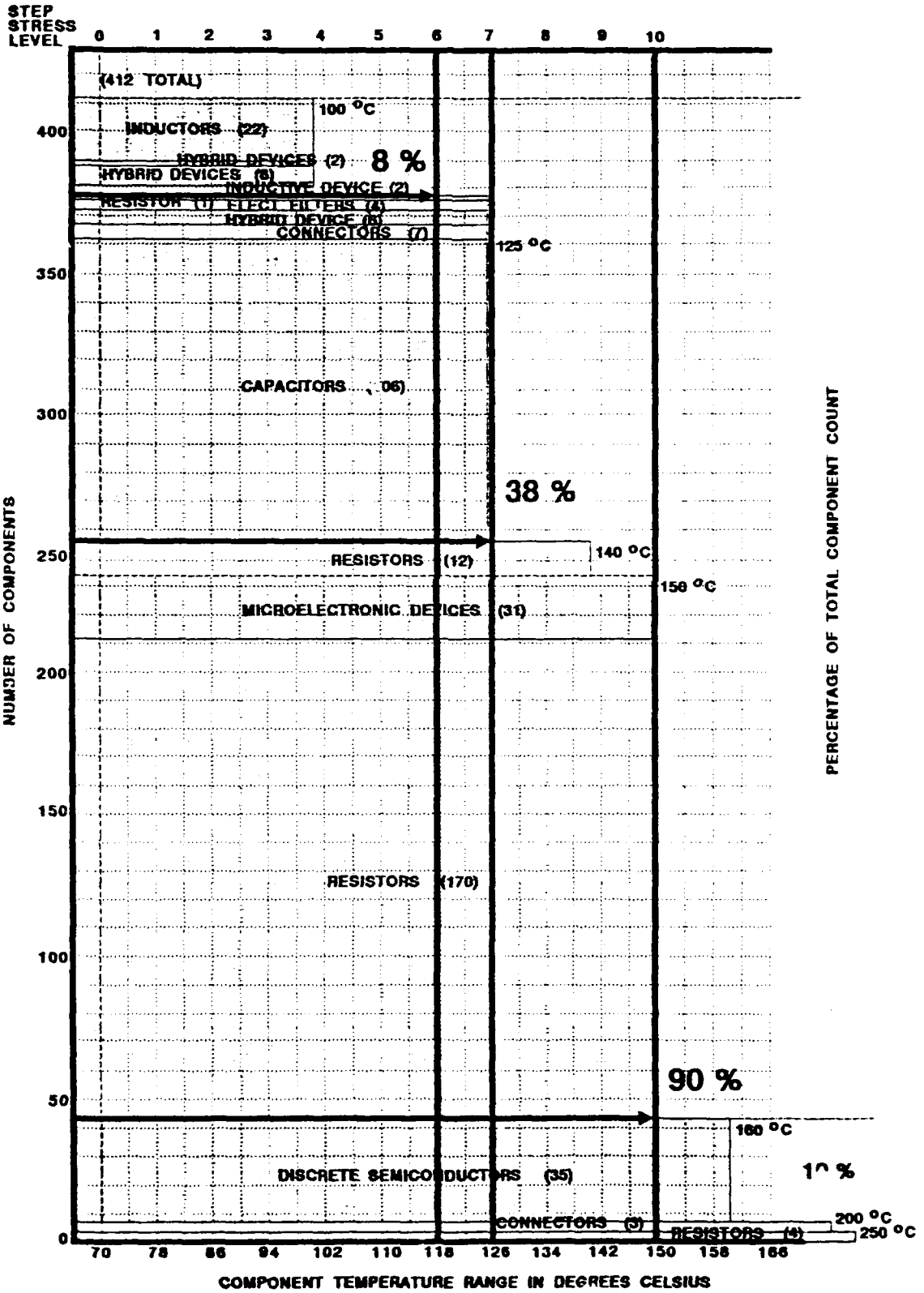
DATE: 13 February 1992
IDC REF: 92/TA/230/002
PAGE 4 OF 5



461510

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EXCERPT FROM R & D TEST & ACCEPTANCE PLAN
(FIGURE 2.2-1: MAXIMUM SURVIVAL TEMPERATURE EXTREMES FOR UUT COMPONENTS BY DEVICE TYPE)



HUGHES AIRCRAFT COMPANY

INTERDEPARTMENTAL CORRESPONDENCE

TO: S. D. Mueller cc: Distribution
D. H. Ragle
ORG: 1A-13
LOC: 675/C311

DATE: 14 February 1992

REF: 92/1H4323-022

SUBJECT: Comments on Conformal Coating Discoloration in [redacted] Module Test

FROM: R. F. Patterson
ORG: 1H-43-23

LOC: FU EXT: 25451
BLDG: 604 M/S: G251

BACKGROUND

A [redacted] synthesizer/detector assembly, P/N [redacted]-103, MSN 1023, that had seen 4 days of burn-in testing was brought to CMED for a diagnostic of the conformal coating which had discolored. A second, identical assembly that had not seen burn-in testing was also brought to CMED for comparison. Two questions were requested to be answered: (1) Was the conformal coating on the burn-in tested assembly deteriorated, and (2) if so, what combinations of time and temperture could the conformal coating withstand without deteriorating? The conformal coating was Conap Conathane 1155A/B per MIL-I-46058, Type UR.

ANALYSIS

To determine whether the discolored conformal coating had deteriorated by becoming less insulative due to the burn-in, the dielectric strength of the discolored coating in place on the assembly was determined in the CMED lab. The usual procedure to do this, according to MIL-I-46058, is to locate an area of the PWB coated at a thickness of .002 ± .001 inch and apply 1500 volts test voltage. However, we could not locate any area thinner than .006 inch on both the burn-in tested assembly and the identical non-tested assembly. Comparable areas of the two assemblies ranged from .006 to .019 inches on the burn-in tested assembly and .006 to .013 inches on the identical non-tested assembly. Therefore, we applied 6000 volts test voltage at the .006 inch thick coated areas of both assemblies. The coating on both assemblies did not break/fail at the 6000 volts, indicating a dielectric strength of at least 1000 volts per mil. The 6000 volts was the maximum for our equipment. Higher voltage testing would require the use of a dielectric fluid immersion tank.

To determine what combinations of time and temperature the conformal coating can withstand, the coating manufacturer's data on continuous operating temperature was addressed first. Conap, Inc. stated 130°C for their Conathane 1155 and Humiseal Div. of Columbia Chase stated 270°F for their 2A64 material. At this temperature for weeks to months (but not presumably for more than 1 or 2 years), the coating, applied as described in MIL-I-46058 for Type UR coated test specimens, would be expected to meet all the requirements of MIL-I-46058, Type UR. We next addressed the times and temperatures that caused the discoloration of the conformal coating on the subject assembly. The accompanying time-temperature chart for the subject MSN 1023 assembly shows stepped temperature increases to 144°C and held for 1 hour with no particular discoloration noticed by the test operators and to 152°C and held for 1 hour with the discoloration results evident on the assembly. This discoloration was deemed to be not serious and to not be cause for rejection per the appearance

MISSION

OF

ROME LABORATORY

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requirements of MIL-I-46058. It was, indeed smooth, homogeneous, transparent, unpigmented, etc., and did not mask or obliterate the identification markings on electronic components, as required for coatings per MIL-I-46058. It was certainly too thick for material qualification test panels, but, as applied to the subject assembly and burn-in tested, the conformal coating material was deemed to have not deteriorated beyond what MIL-I-46058 requires of it. However, we were not able to determine exactly how much, if any, deterioration occurred as compared to the second identical assembly that had not been burn-in tested. What we can surmise, however, is that the dielectric strength obtained, 1000 vpm, is in the range of what the manufacturers say is typical of their coatings. For nominal .002 inch thick coating, Conap 1155 is typically 3000 volts. Since we know that 3 times the thickness does not give 3 times the dielectric strength, we can surmise that a .006 inch thick coating would give only in the range of 6000 to 8000 volts; and this is what we got with the subject burn-in tested assembly.

With the findings obtained thus far, we can make certain assumptions of time and temperture that the polyurethane conformal coating can withstand. Assuming that the temperature would be applied by a series of steps to a final maximum temperature as done in the subject assembly, that the temperature is what a thermocouple actually measures on the surface of the component and that the conformal coating is no more than 6 to 12 mils thick, the conformal coating should be able to withstand the following burn-in time-temperature combinations without the severe discoloration that occurred on the burn-in test assembly:

(1) 143 ± 1°C for 1 hour
(2) 140 ± 1°C for 10 hours
(3) 135 ± 1°C for 10 days
(4) 130 ± 1°C for 10 months

CONCLUSIONS

(1) In terms of harmful deterioration and non-compliance with MIL-I-46058, the only deterioration found on the subject burn-in tested assembly was of the cosmetic/use-as-is variety.

(2) The combinations of time and temperature that the conformal coating should withstand without the severe discoloration found on the subject burn-in tested assembly include those given in the list above subject to the noted assumptions.

OVERALL COMMENTS

The unusually high thicknesses of the conformal coating that were measured indicates a possible problem. The MIL-I-46058 thickness tolerance is .002 ± 001 inch; and the most that is allowed by MIL-STD-275 and other specifications is .003 ± .002 inch. The problem with high coating thickness is that it thermally insulates the component it is covering and hinders the radiation/escape of the heat generated by the component.

R. F. Patterson, Head
Nonmetallics Group
Components and Materials