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...RT DATE	3. REPORT TYPE AND DATES COVERED
28 FEB 1993	Final Technical 1 July 1991-31 Dec 199

4. TITLE AND SUBTITLE
Investigation of a New Concept in Semiconductor Microwave Oscillators: The Contiguous Domain Oscillator

5. FUNDING NUMBERS
AFOSR-91-0224

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AFOSR-TR- 93 0492

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10. SPONSORING/MONITORING AGENCY REPORT NUMBER
2305/A1

DTIC
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11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION AVAILABILITY STATEMENT
unlimited

12b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

In the first phase of this project, we constructed experimental prototypes of the contiguous domain oscillator device. These prototype devices oscillated in the single-domain mode (similar to a lateral Gunn diode), producing signals in the range from 6 to 28 GHz. Contiguous domain operation could not be achieved. We believe this failure was due to the high sheet resistance of our resistive gate. (With the gate resistance high, image charge motion in the gate disrupts the ideal linear gate potential).

The objective of the second phase of research was to produce new devices having lower gate resistance and to demonstrate contiguous-domain operation. These new devices were to be built by ITT Gallium Arsenide Technology Center and were to be delivered to us by mid-1991. Due to a series of problems at ITT, the devices were never delivered. Instead, we have shifted our emphasis to computer simulation, and have developed a new computer model of the device which shows the transition from multiple to single-domain mode as the gate is moved further away from the channel. This new simulation program allows us to study the transition regime and to investigate the range of device parameters over which contiguous-domain operation can be expected.

...ECT TERMS	15. NUMBER OF PAGES
...0, contiguous domain oscillator, resistive gate MESFET	140
93 4 11 078	16. PRICE CODE

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Background

The contiguous domain oscillator (CDO) is a resistive-gate GaAs FET which functions as a voltage-controlled millimeter-wave oscillator. The structure is compatible with planar processing and can be incorporated with standard GaAs FETs in the form of monolithic millimeter-wave integrated circuits (MMICs). The device was first proposed by Cooper and Thornber in 1983, and has been under investigation at Purdue since 1985.

Conventional microwave oscillators (such as the IMPATT, BARITT, and Gunn diodes) generate microwave power by using a mechanism which depends strongly on electric field (e.g. avalanche multiplication or negative differential mobility) to create charge packets or domains. The conventional devices all employ a two-terminal geometry, as shown in Fig. 1, and hence are diodes. Since the internal electrostatic geometry is one dimensional, once a charge packet is introduced, it alters the electric field throughout the device (Fig. 1a) in such a way as to turn off the generation mechanism. The single charge packet then drifts across the device and is extracted by the anode. Once the charge packet has drifted out of the device, the internal field returns to it's original value and the generation process begins again. The entire process is therefore a series of repeated transients, with the oscillation frequency determined by the inverse of the generation time plus the transit time. Clearly, once the device has been built, the transit time (and hence the oscillation frequency) is fixed. In addition, for millimeter-wave operation the drift distance must be made very short, typically less than 1 μm.

In contrast, the contiguous domain oscillator employs a two-dimensional electrostatic geometry, as illustrated in Fig. 1b. In this structure, the electric field within the device is created by the potential drop along a resistive "gate" electrode, and electrons are constrained to drift parallel to the resistive gate by a potential barrier, shown schematically in Fig. 1b. A charge packet or domain in this structure alters the electric field only locally -- outside the packet the field is still determined by the potential gradient in the resistive gate. If electrons are supplied by a source contact and extracted by a drain contact, the structure in Fig. 1b resembles a field-effect transistor with a resistive gate. Computer simulations [1,2] indicate that when the electric field is in the regime of negative differential mobility, charge domains will form spontaneously in the channel near the source and drift along the channel into the drain. In contrast to microwave diodes, the frequency is not determined by the physical length of the device, but rather by the spatial period of the domains in the channel. This spatial period is found to depend upon the average electron density in the channel, which can be controlled by the source to gate voltage.

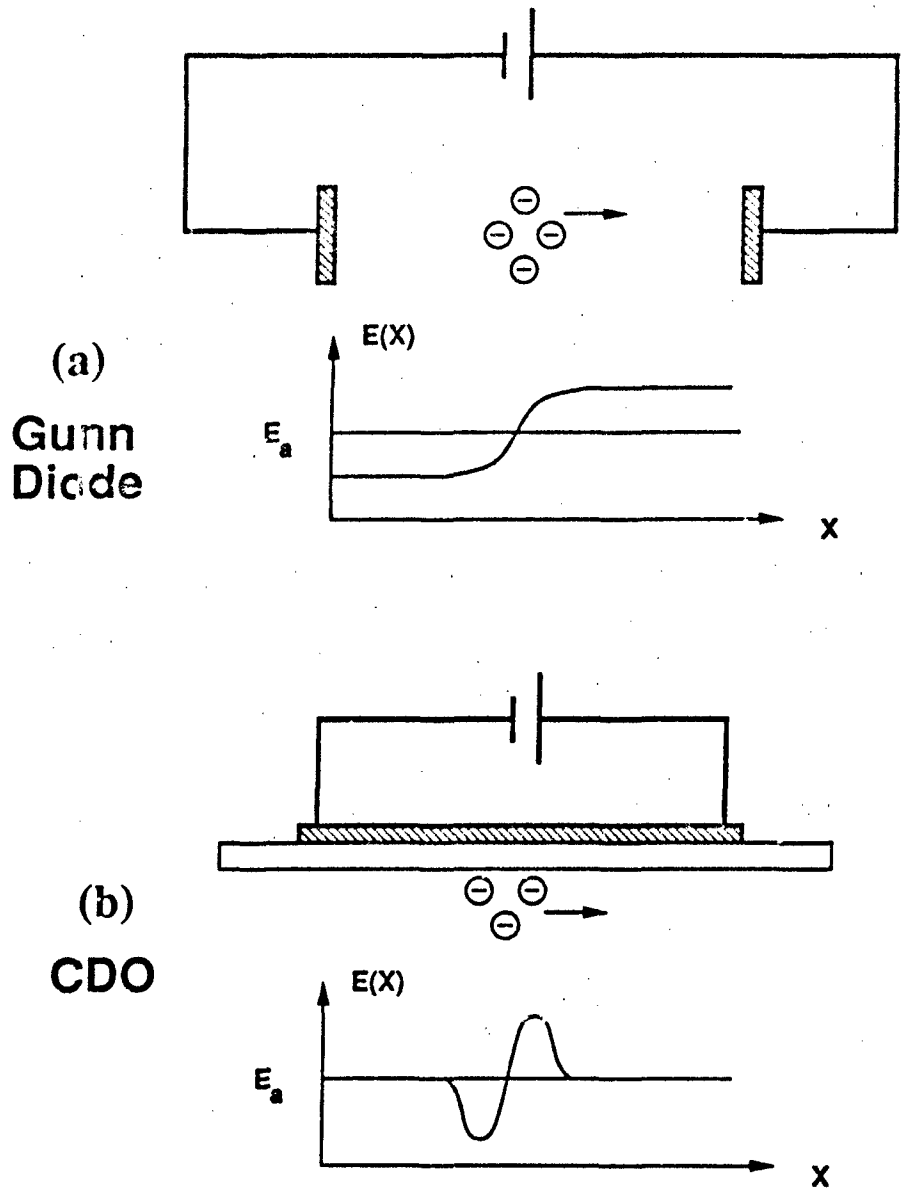


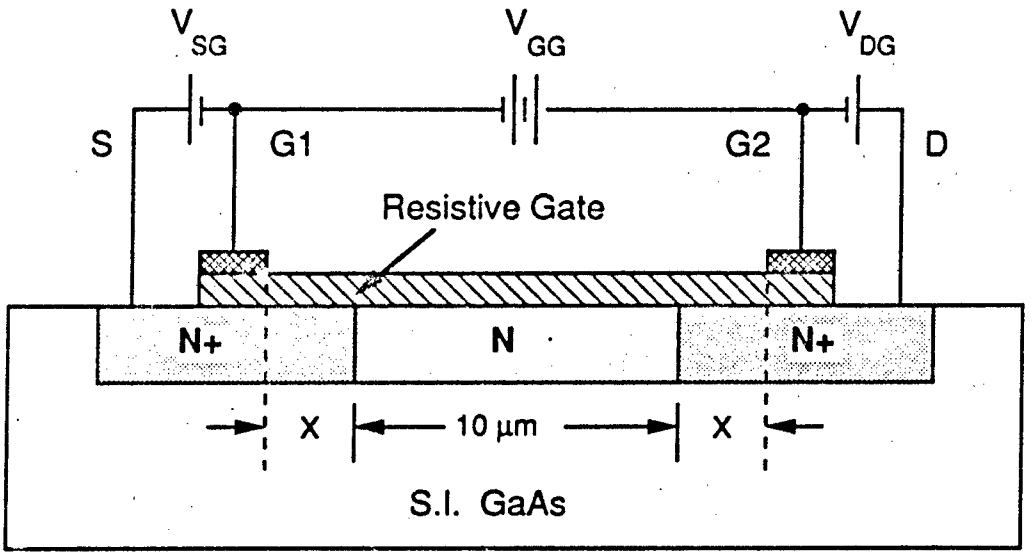
Figure 1. Schematic illustration of the operation of (a) the conventional Gunn diode (top), and (b) the Contiguous Domain Oscillator (bottom). The Gunn diode has a one-dimensional electrostatic geometry, and the presence of a chrage packet perturbs the electric field throughout the device. The CDO has a two-dimensional electrostatic geometry, and the charge packet does not perturb the electric field in the remainder of the device.

Experimental devices were fabricated both at Purdue and by the ITT Gallium Arsenide Technology Center (ITT-GTC) in Roanoke, VA. A schematic cross section of the experimental contiguous domain oscillator device is shown in Fig. 2. The early devices fabricated at Purdue failed to operate, but devices delivered to Purdue by ITT-GTC in February 1988 eventually produced microwave signals in the frequency range between 6 and 28 GHz. Although these frequencies reach almost to the millimeter-wave range, they are too low to be due to contiguous domain oscillation. We were able to show that the device was operating in the single domain mode: in effect, only one domain was forming in the channel at a time, and this domain propagates from source to drain before a new domain can form. The frequency is simply the inverse of the transit time from source to drain, and scales inversely with channel length, as shown in Fig. 3. Some frequency modulation (up to 20%) could be obtained by adjusting the gate-to-source voltage, but not as much as expected from the contiguous-domain mode.

We suspect that the problem in the initial devices was due to the relatively high resistivity of the resistive gate. This could be demonstrated by a simple calculation: We first assume an *ideal* gate, in which the potential increases linearly from source to drain. The operation of this ideal device is simulated, and contiguous domains are observed in the channel, as expected. We then assume that the charge domains in the channel induce equal and opposite image charges on the resistive gate, and that these image charges move along with the domains. The charge motion in the gate constitutes a current flow, and this current multiplied by the gate resistivity results in local voltage drops. When these local potential drops are added to the ideal linear potential drop, the desired linear voltage drop is severely perturbed -- the lateral electric field in the gate, instead of being constant, oscillates sinusoidally with position, and the minimum field actually becomes *negative* at the low point of each cycle! Such a severe perturbation *must* destroy the screening effect of the gate!

The obvious solution was to decrease the resistivity of the resistive gate. The original ITT devices have a WSiN gate with a sheet resistivity of 30 kΩ per square. Our calculations indicated that this needs to be reduced to about 3 kΩ per square to eliminate the local field perturbations. It then became the primary objective of the research to build new devices meeting these specifications

ITT initially agreed to supply six three-inch wafers of CDO devices by mid-1991. All were to have gate resistivity between 1.5 and 3 kΩ per square. However, due to a series of internal problems at ITT, beginning in the summer of 1991, the wafers were delayed. These problems were both technical and (apparently) political. In spite of numerous attempts to stimulate delivery of the samples via phone calls, FAX messages, etc., we were eventually forced to conclude that the devices were not going to be forthcoming.



Resistive Gate: WSiN, 110 nm, 30 kΩ/ □

N Channel: $1.2 \times 10^{17}\ cm^{-3}$, 150 nm

S and D: $5 \times 10^{17}\ cm^{-3}$, 150 nm

Distance X : { 5 µm / 0

Figure 2. Cross section of the experimental devices fabricated by ITT-GTC. The structure is essentially a resistive-gate MESFET, and is compatible with standard GaAs FET processing.

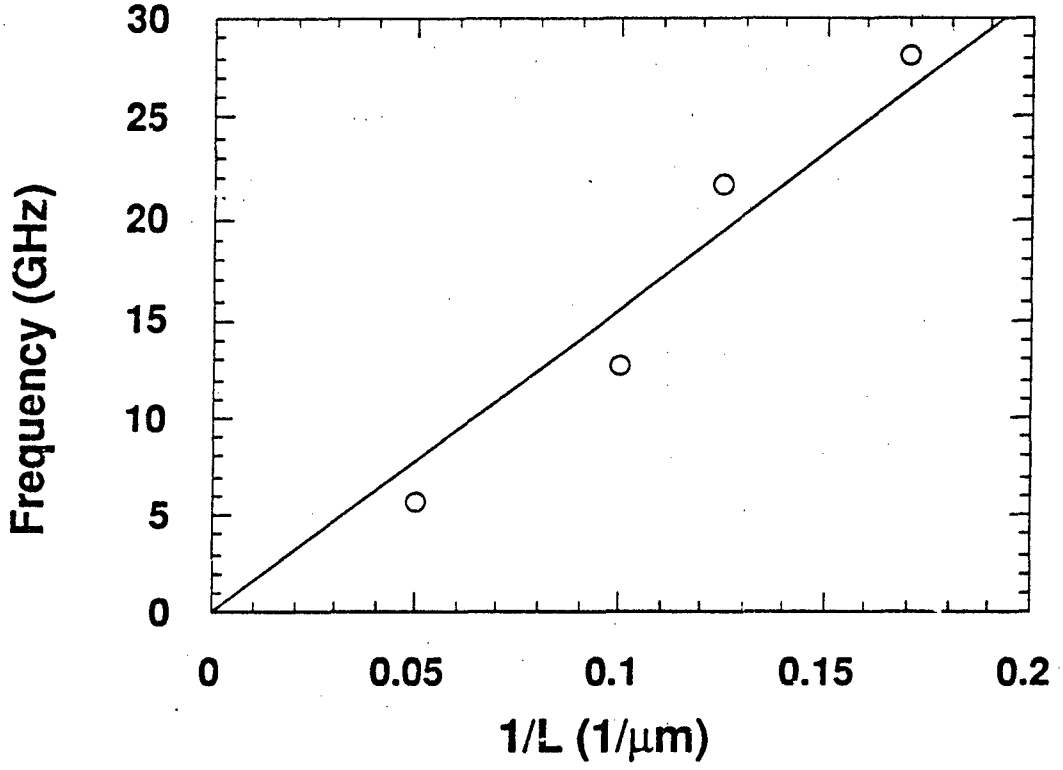


Figure 3. Measaured oscillation frequency plotted vs inverse length. The linear relationship indicates that the frequency is the inverse of the transit time, and proves that the devices are operating in the single-domain mode.

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As a result of ITT's de-facto withdrawal from the project, we redirected the program at Purdue to concentrate on obtaining a more thorough understanding of the operation of the device under circumstances where both the source/drain electric field and the resistive-gate electric field exert competing influences on electron motion in the channel.

Funding History

The original CDO devices were built and tested under grant no. AFOSR-85-0193, which ran from 1 May 1985 through 31 April 1988. A continuation grant (AFOSR-85-0193E) and it's no-cost extension supported one graduate student from 1 May 1988 through 31 January 1990. From 1 February 1990 through 30 June 1991 we conducted this research using local money, primarily a grant from the Indiana Corporation for Science and Technology. With these local funds depleted, we applied for and received the present one-year grant, AFOSR-91-0224. This grant began on 1 July 1991 and terminated on 30 June, 1992. A no-cost extension to 31 December 1992 was requested and approved.

Device Simulation Results

In the original computer program used to simulate the contiguous domain effect, the local potential at each point in the channel is calculated using one-dimensional electrostatics. The potential then depends on only two variables: the local gate voltage and the electron density in the channel at that point. (A non-local correction term is also included to account for fields from adjacent regions having drastically different electron densities -- this eliminates the so-called "gradual channel approximation".)

The original approach is reasonable under the assumption that the channel potential is dominated by the resistive gate, and indeed has been verified experimentally for resistive gate devices in silicon (work performed by the author at Bell Labs prior to 1983). However, this one-dimensional approach is *not* valid in situations where the local potential is influenced by the potentials on the source and drain, i.e. where the gate does *not* dominate. It is precisely these conditions which give rise to single-domain operation. Thus, in order to investigate single-domain operation and the transition between single- and multiple-domain behavior, it was necessary to write a completely new simulation program using a different approach.

The difference between the old and new programs is illustrated by Figs. 4 and 5. In both circuits, the J_i elements at each node i represent the current due to electron motion in the channel. This current is calculated as follows. First, the local channel potential ϕ_i is calculated at each grid node (more about this later). Knowing the local potentials, the electric field between each node is determined. The currents J_i are then calculated based on the nonlinear velocity-field relationship for electrons in GaAs. A time step Δt is taken, and the local electron densities are allowed to change as a result of the currents flowing into and out of each node. The new electron densities are then used to calculate new potentials, and the cycle repeats. If the discretization in space and time are sufficiently small, the difference equations are good approximations to the differential equations governing device operation, and valid results are obtained.

The difference between the old program (Fig. 4) and the new program (Fig. 5) is the manner in which the local potentials ϕ_i are calculated. Although the figures look very similar, the only difference being the inclusion of the lateral semiconductor capacitances C_S in Fig. 5, this difference is extremely important. In fact, the approaches used to calculate the potentials for the two cases are totally different. In the original program (Fig. 4), the local potentials ϕ_i could be calculated from the local gate potentials V_{Gi} and the local electron densities n_i through a simple algebraic equation. In the circuit of Fig. 5, the local channel potentials ϕ_i must be calculated by solving the set of simultaneous equations describing the entire device. This requires the use of a simultaneous linear equation solver at each time step. Since these equations include the source and drain potentials implicitly, the source and drain may dominate over the gate if the element values in the model are of appropriate values.

In the model of Fig. 5, if the coupling between the gate and channel is reduced, for example by moving the gate further away from the channel, the C_D capacitors connecting the gate and channel become small and the channel potential will be dominated by the source and drain potentials. The device then functions as a lateral Gunn diode, and the model produces single-domain oscillation. On the other hand, if the gate is placed in close proximity to the channel, as in the CDO, the gate dominates and the model of Fig. 5 produces the same results as the original model of Fig. 4.

Figure 6 shows the electron density as a function of position for several times for the circuit of Fig. 5 when the gate has been placed at a large distance (600,000 Å) from the channel. Here the device is functioning essentially as a lateral Gunn diode, with the electric field lines from the charge domains terminating on the source and drain, and a single dipole domain propagates along the channel toward the drain. Multiple domains do not form.

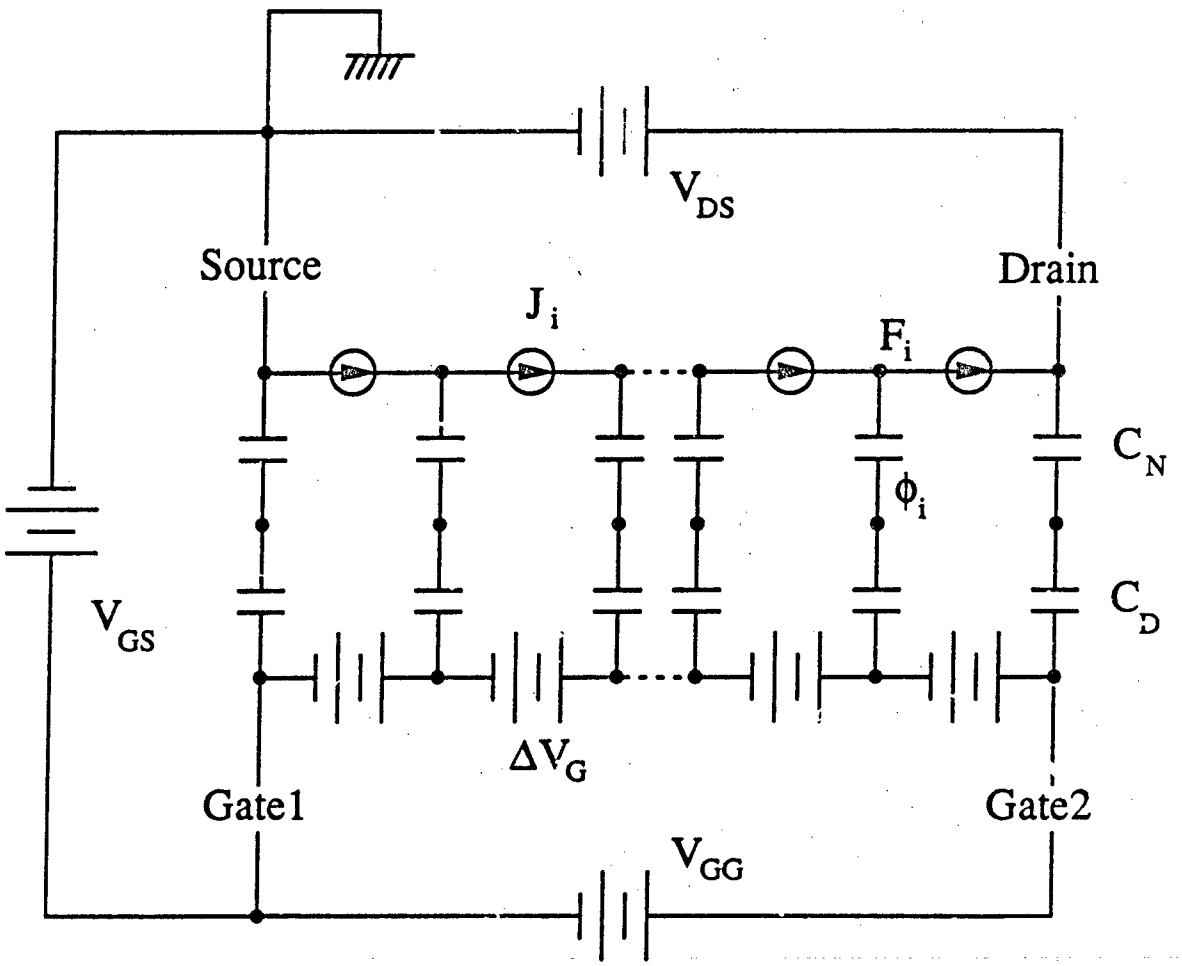


Figure 4. Equivalent circuit illustrating the original program for simulation of the contiguous-domain effect. The full simulation consisted of 256 nodes, not just the five shown here. The channel potential ϕ is calculated at each node, based only on the gate potential and electron density at that node. Once the channel potentials are known, the currents J are calculated and a time step taken.

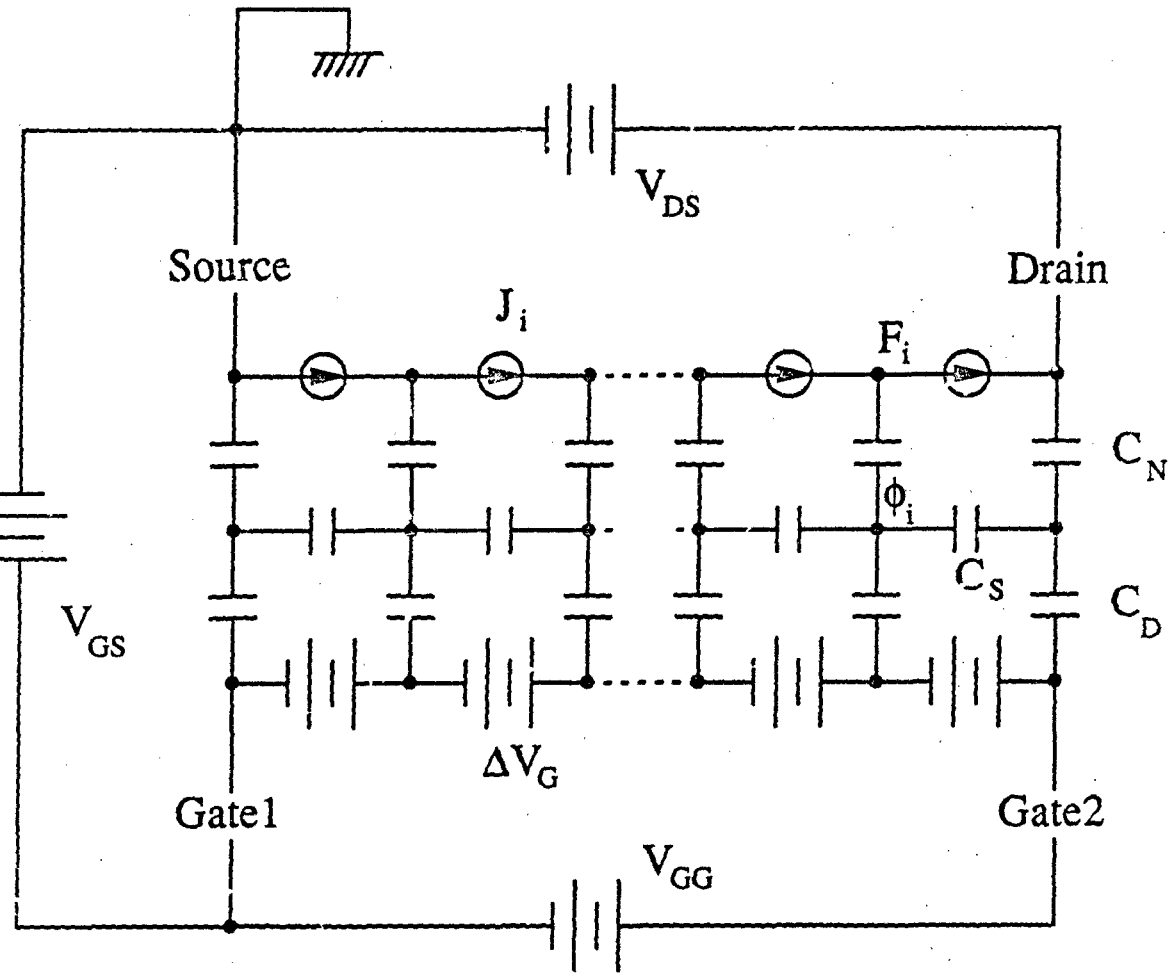


Figure 5. Equivalent circuit illustrating the new simulation program. Here the channel potentials are obtained by simultaneous solution of the node equations of the entire circuit. In this way, the effect of source and drain potentials are included in a natural way. If the coupling capacitance C_D between gate and drain are small compared to the semiconductor capacitances C_S connecting each Δy region of the device, then the source and drain field will dominate and single domain oscillations will be observed.

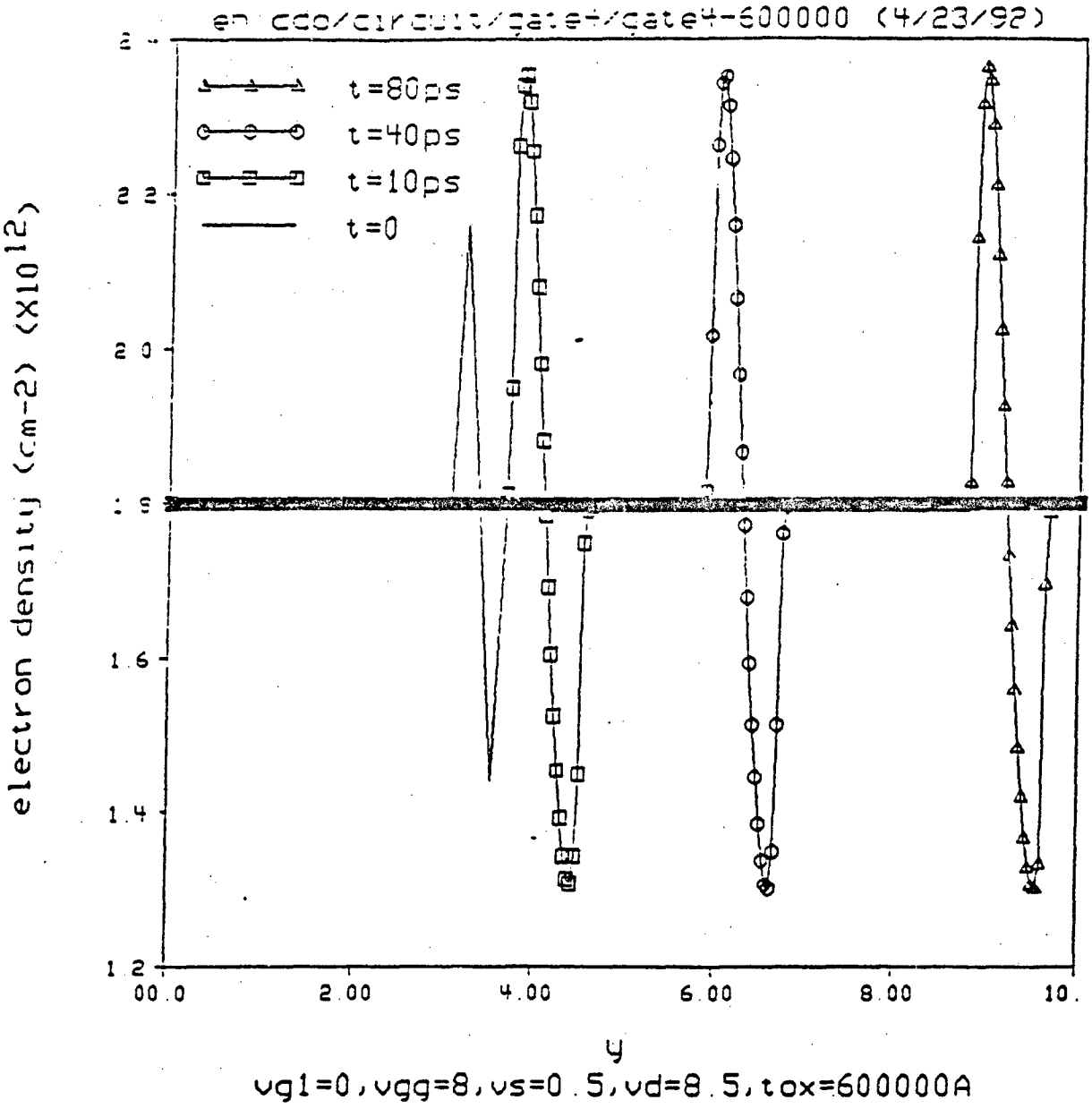


Figure 6. Electron density in the channel as a function of position predicted by the new simulation program when the gate is moved well away from the channel so that the source/drain field dominates. A single dipole domain is established as an initial condition at t=0. This domain stabilizes and drifts along the channel, as shown at t=10, 40 and 80 ps. This type of operation is referred to as the SINGLE DOMAIN MODE.

In contrast, Fig. 7 shows the predictions of the same program when the gate is brought into close proximity to the channel (1050 Å). Here we plot electron density for one particular time, 150 ps after the start of the simulation. The electron distribution in the channel has formed multiple domains in exactly the manner predicted by our original program. The oscillation frequency observed in the drain current for this case is 63.2 GHz.

The new simulation program has been compared with the original program under conditions where the gate dominates the channel potential, and the predicted oscillation frequencies are in very good agreement. This is shown in Fig. 8, where frequency is plotted as a function of the product of electron density n_s and depletion depth x_d. The small symbols are predictions of the original program for a large number of simulation runs, and the large black circles are predictions of the new program for several runs. In spite of differences in the models and the algorithms used to calculate them, the predictions of the two approaches are in quite good agreement. This agreement gives us confidence that both approaches are essentially correct.

Summary

In spite of the failure of ITT-GTC to deliver their devices, we made substantial progress in analyzing the behavior of the CDO device under conditions where the source/drain field competes with the gate field for control of the channel. A major accomplishment was the creation of a new computer code which accounts for both source/drain and gate fields simultaneously. These computer simulations reinforce our belief that single-domain operation observed in the experimental devices is a result of loss of gate control of the channel.

However, no matter how sophisticated the computer analysis, it can never replace a working experimental device. Unfortunately, the goal of experimental verification was not achieved in this project. It is the author's belief that the contiguous domain effect is real and can be observed in properly-designed devices. However, the author also feels that he has personally devoted enough time and effort to this goal, and that any further development work should be carried out by others. He is eager to share his thoughts and calculations with other groups who might be inclined to pick up this research in the future.

The author wishes to express his sincere appreciation to the Air Force Office of Scientific Research, and in particular to Dr. Gerald Witt, for their support of this research. Dr. Witt exhibited a great deal of understanding during difficult periods in this project, and continued to support this work at a low level after the original

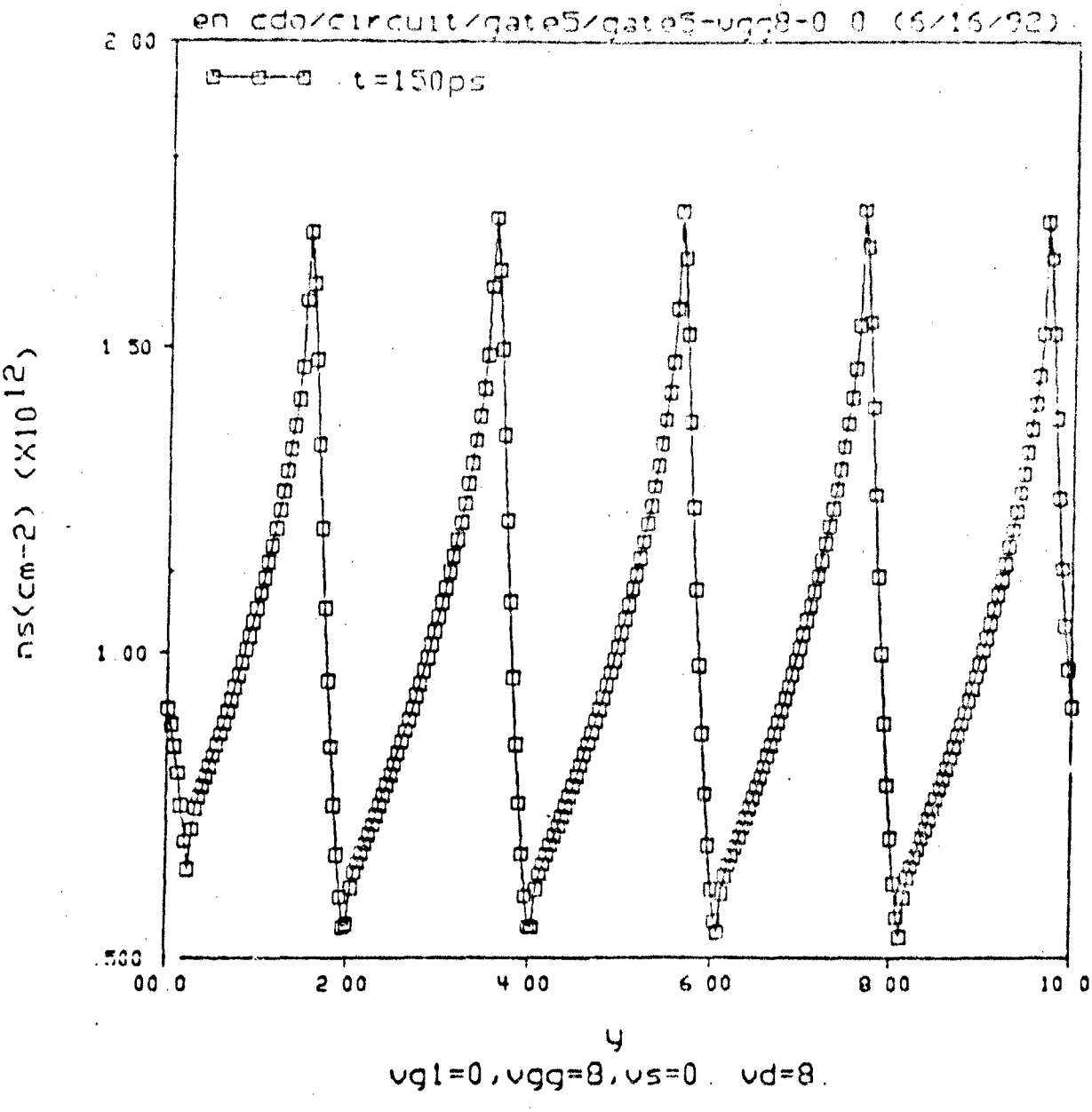


Figure 7. Electron density predicted by the new program when the gate is placed in close proximity to the channel so that the gate field dominates. For an initial condition, we established a single domain in the channel at t=0, but by 10 ps the channel had spontaneously developed multiple domains, and the pattern had reached steady state well before 100 ps. (The distribution pictured here was observed at 150 ps). This represents the CONTIGUOUS-DOMAIN MODE.

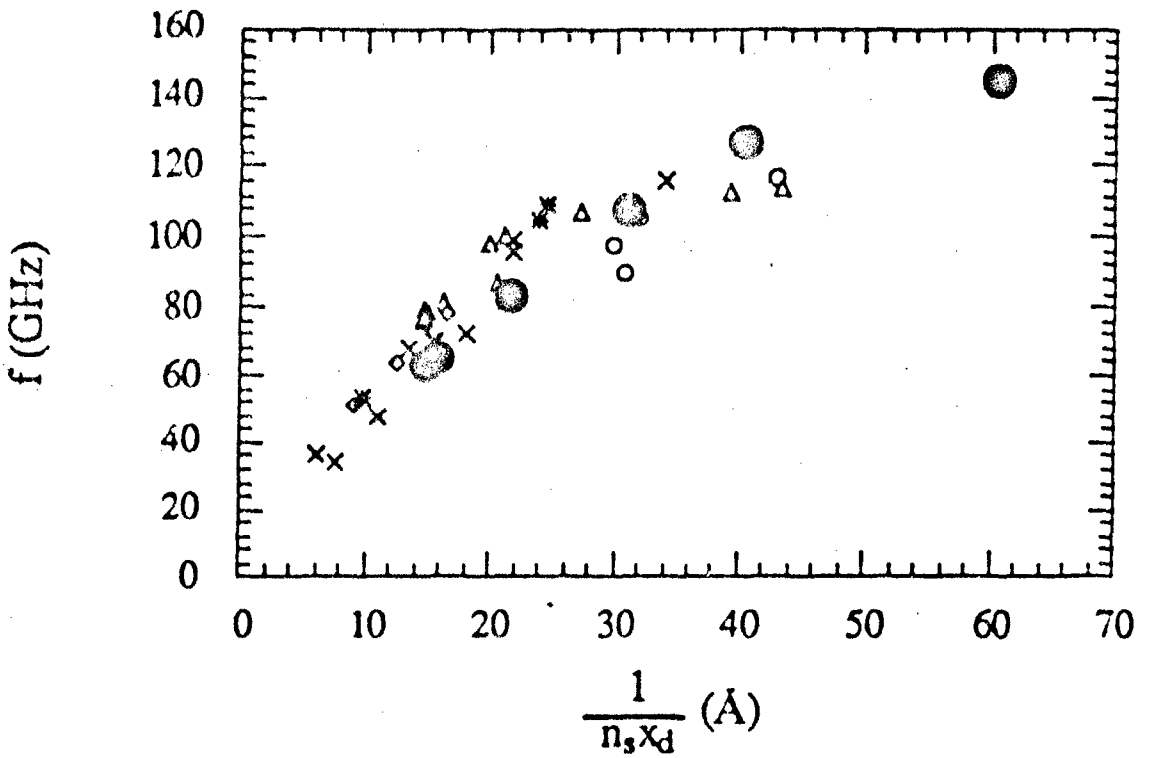


Figure 8. Frequency of oscillation as a function of the parameter $1/(n_s\ x_d)$, where n_s is the average electron density in the channel and x_d is the separation between the centroid of channel charge and the gate electrode. The cross, triangle, star, diamond, and circle symbols represents results from the original CDO simulation program of Fig. 4. The large black circles represent results from the new program for the case where the gate field dominates over the source/drain field. Agreement is very good. This gives us confidence in the predictions of BOTH programs.

grant had expired. As a result of his efforts, two graduate students were able to continue their research and obtain their Ph.D. degrees after the termination of the original grant. Both are now employed in the U.S. semiconductor industry.

References

[1] J. A. Cooper, Jr. and K. K. Thornber, "Screened-Charge Transferred-Electron Oscillators," *IEEE Electron Device Letters*, Vol. EDL-6, pp. 50-53, Jan. 1985.

[2] J. A. Cooper, Jr. and K. K. Thornber, "Contiguous-Domain Transferred-Electron Oscillators," *IEEE International Microwave Symposium*, St. Louis, MO, June 4-6, 1985.

[3] Y. Yin, H. Fu, J. A. Cooper, Jr., M. L. Balzan, and A. E. Geissberger, "Operation of a Resistive Gate MESFET Oscillator in the Single-Domain Transit-Time Mode," *IEEE Electron Device Letters*, Vol. EDL-11, pp. 538-540, November, 1990.

[4] J. A. Cooper, Jr. and M. G. Lamont, "Numerical Simulation of Surface Charge Transport in Silicon and GaAs," TM-83-11156-13, Bell Laboratories, July 18, 1983.

Publications

Here we list all publications since the beginning of the research program in 1985. The work during the last calendar year has not yet been published, but one new paper is now in draft form (item 5 below), and we expect to produce one or two others dealing with new transient simulation results within the next six months.

Serial Journal Papers Since 1985

[1] Y. Yin, J. A. Cooper, Jr., P. G. Neudeck, M. L. Balzan, and A. E. Geissberger, "Negative Transconductance in a Resistive Gate Metal Semiconductor Field Effect Transistor," *Applied Physics Letters*, Vol. 54, pp. 1884-1886, 8 May 1989.

[2] J. A. Cooper, Jr., Y. Yin, M. L. Balzan, and A. E. Geissberger, "Microwave Characterization of a Resistive-Gate MESFET Oscillator," *IEEE Electron Device Letters*, Vol. 10, pp. 493-495, November, 1989.

[3] Y. Yin, H. Fu, J. A. Cooper, Jr., M. L. Balzan, and A. E. Geissberger, "Operation of a Resistive Gate MESFET Oscillator in the Single-Domain Transit-Time Mode," *IEEE Electron Device Letters*, Vol. EDL-11, pp. 538-540, November, 1990.

[4] Y. Yin and J. A. Cooper, Jr., "Simple Equations for the Electrostatic Potential in Buried-Channel MOS Devices," *IEEE Transactions on Electron Devices (Briefs)*, Vol. ED-39, pp. 1770-1772, July, 1992.

[5] H. Fu and J. A. Cooper, Jr., "Steady-State Modeling of Resistive Gate MOSFET's," to be published in *IEEE Transactions on Electron Devices*, 1993.

Conference Presentations Since 1985

[1] Y. Yin, J. A. Cooper, Jr., P. G. Neudeck, M. L. Balzan, and A. E. Geissberger, "Room Temperature Negative Transconductance in a Resistive Gate GaAs FET," *WOCSEMMAD Conference*, Hilton Head, SC, February 20-22, 1989.

[2] J. A. Cooper, Jr., Y. Yin, M. L. Balzan, and A. E. Geissberger, "Microwave Characterization of the Contiguous Domain Oscillator," *IEEE Device Research Conference*, Cambridge, MA, June 19-21, 1989.

[3] J. A. Cooper, Jr., Y. Yin, M. L. Balzan, and A. E. Geissberger, "Experimental Verification of the Contiguous Domain Oscillator Concept," *12th IEEE/Cornell Conference on Advanced Concepts in High Speed Semiconductor Devices and Circuits*, Ithaca, NY, August 7-9, 1989.

Invited Lectures Since 1985

[1] J. A. Cooper, Jr., "A Resistive Gate MESFET Transferred Electron Oscillator," Wright Research and Development Center, WPAFB, Dayton, OH, Dec. 1989.

Theses Since 1985

[1] M. Fang, "Fabrication and Characterization of Thin Metal Films," MS Thesis, Purdue University, December 1985.

[2] John S. Kleine, "Rapid Thermal Annealing of Silicon Implanted Gallium Arsenide," MS Thesis, Purdue University, December 1986.

[3] Robert E. Beaty, "A Bias Tunable Monolithic Microwave Oscillator - The Contiguous Domain Oscillator," Ph.D. Thesis, Purdue University, August 1988.

[4] Yiwen Yin, "Investigation of the MESFET Version Contiguous Domain Oscillator," Ph.D. Thesis, Purdue University, May 1990.

[5] Hua Fu, "Characterization and Simulation of the Contiguous Domain Oscillator," Ph.D. Thesis, Purdue University, December 1992.

Technical Reports Since 1985

[1] J. S. Kleine and J. A. Cooper, Jr., "Rapid Thermal Annealing of Silicon Implanted Gallium Arsenide," TR-EE 86-43, School of Electrical Engineering, Purdue University, December 1986.

[2] Y. Yin, J. A. Cooper, Jr., and H. Fu, "Investigation of a Resistive-Gate MESFET Contiguous Domain Oscillator," TR-EE 90-25, School of Electrical Engineering, Purdue University, April 1990.

Personnel

The following list includes students who have been involved with this project since the inception of AFOSR funding in 1985.

Graduate Students:

Robert E. Beaty
- Began Ph.D. program, January 1984 (prior to the start of AFOSR funding)
- Received Ph.D. August 1988.
- Thesis: "A Bias Tunable Monolithic Microwave Oscillator - The Contiguous Domain Oscillator"
- Employment: Dept. of Electrical Engineering, Auburn University

Ming Fang
- Began MS program, January 1985
- Received MSEE degree, December 1985
- Thesis: "Fabrication and Characterization of Thin Metal Films"
- Employment: RCA, Indianapolis, IN

John S. Kleine
- Began MS program, August 1985
- Received MSEE degree, December 1986
- Thesis: "Rapid Thermal Annealing of Silicon Implanted Gallium Arsenide"
- Employment: Cypress Semiconductor, San Jose, CA

Yiwen (Peter) Yin
- Began Ph.D. program, August 1986
- Received Ph.D., May 1990
- Thesis: "Investigation of the MESFET Version Contiguous Domain Oscillator"
- Employment: National Semiconductor, Salt Lake City, UT

Hua Fu
- Began Ph.D. program, May 1989
- Received Ph.D., December 1992
- Thesis: "Characterization and Simulation of the Contiguous Domain Oscillator"
- Employment: Motorola, Phoenix, AZ

Outside Interactions

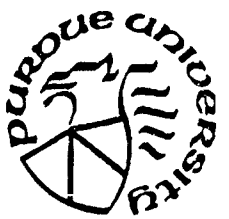
We have collaborated with the ITT Gallium Arsenide Technology Center, Roanoke, VA, in the fabrication and characterization of the initial CDO devices. The devices were designed and masks were fabricated at Purdue. ITT conducted all the fabrication operations and delivered three two-inch CDO wafers to Purdue on 23 February, 1988. After characterization, we determined that the gate resistivity of the original devices was too high, and ITT agreed to fabricate a second lot of devices for delivery in the spring of 1991. Due to problems with the processing line in the spring and summer of 1991, these samples were never delivered.

Over the years, we have been contacted by several groups who have had some level of activity in investigating this device concept. These groups included MIT, Jet Propulsion Laboratory, Columbia University, and Magnavox (Torrance, CA). Both MIT and Columbia stated that they conducted their own computer simulations, and both reported observing microwave oscillations in their simulations. JPL listed a research program on this device in their research summary brochure for a recent year (1990?), but this program is not now believed to be active. Magnavox sent a representative to Purdue several years ago (1986?) to discuss fabricating the device, but we subsequently elected to collaborate with ITT.

There have been no new interactions during the last 12 months.

Appendix:

Characterization and Simulation of the Contiguous Domain Oscillator



Hua Fu and James A. Cooper, Jr.

School of Electrical Engineering
Purdue University
West Lafayette, IN 47907

December, 1992

CHAPTER 1
INTRODUCTION

1.1 Introduction

Since solid state devices were introduced into microwave area, they have proven to be very desirable in terms of reducing the circuit size and cost, enhancing the circuit performance, and increasing the reliability. Consequently, they are constantly replacing microwave tubes and continuing to open up new applications particularly at lower power levels [1]. In many cases, they are the heart and soul of numerous microwave systems. Especially with the integrated circuit techniques extending to the fabrication of microwave circuits, it is now possible to reduce greatly the size of microwave circuits so that complete microwave systems can be put on a single semiconductor chip.

The microwave power generators and local oscillators are essential parts of the microwave system. Remarkable successes in the invention and improvement of the oscillators have been achieved over the last 30 years, among which two types of oscillator are most distinguishable, namely IMPATT and Gunn diode oscillators. Various practically used oscillators have them as the active devices.

To meet the ever growing demands, continuous searches for new devices and new applications are still going on. The development of solid state microwave sources has in general been of two kinds [2]. First of all, we have the steady progress resulting from pushing the upper limiting operation frequency of the existing devices and improving their compatibility with modern VLSI fabrication technology in order to have better circuit performance, low cost and weight. Secondly, we have the more erratic progress resulting from the discovery of new devices working on fundamentally different principles. As for the second category, numerical simulations have come to play an increasingly important role as a tool for exploring new concepts and designing specific devices since realistic modeling of nonlinear behavior, based on purely analytical techniques, is limited.

The current research project is on a potential microwave source with many novel properties. It combines the transferred electron effect in n-type GaAs material together with

the internal two-dimensional electrostatic geometry to offer high frequency operation and high frequency tunability. This device is referred to as the Contiguous Domain Oscillator (CDO) based on the fact that a contiguous sequence of domains can be generated in the channel. The frequency is determined by the spacing between adjacent domains rather than by a transit time. Therefore high frequency operation is achievable without submicron technology. Last but not the least, it has a planar structure and can be easily integrated into the microwave subsystems now under development.

1.2 Comparative Description of Conventional Diodes and the Contiguous Domain Oscillator (CDO)

1.2.1 Conventional Diodes

By conventional diodes, we mean IMPATT and Gunn diodes. The IMPATT diode is a representative of the transit time device family, and the Gunn diode is classified as a transferred-electron device. Although the charge formation mechanism is different for each type of device, they all operate using the effect of a finite carrier transit time as had been done with microwave electron-beam devices of the Klystron and traveling-wave tube type. Therefore they are normally operated into an external resonant circuit to achieve better efficiency, frequency stability and noise.

As shown in Fig 1.1(a), the conventional diodes have one-dimensional geometry. A high electric field, which is above threshold ξ_{th} for the formation of charge packets, is established by applying a voltage V_0 across the two terminals (for IMPATT diode, ξ_{th} is the maximum electric field at breakdown, and for Gunn diode, ξ_{th} is the field where the field-velocity curve peaks). Once a charge packet is generated, the field due to the space-charge and its image is parallel to the applied field which significantly alters the total electric field outside the domain to a level below ξ_{th} and thereby turns off the domain generation mechanism. As a result, only one domain can exist in the channel and drift across the device. By the time the charge domain is removed at the anode, the electric field is back up to the original higher value to cause the formation of a new charge domain at the cathode. And the process of domain build-up, propagation, and extinction is repeated. In this way, transit-time current oscillations are produced which have a fundamental frequency

$$f_\tau = 1/\tau = v_d/L \tag{1.1}$$

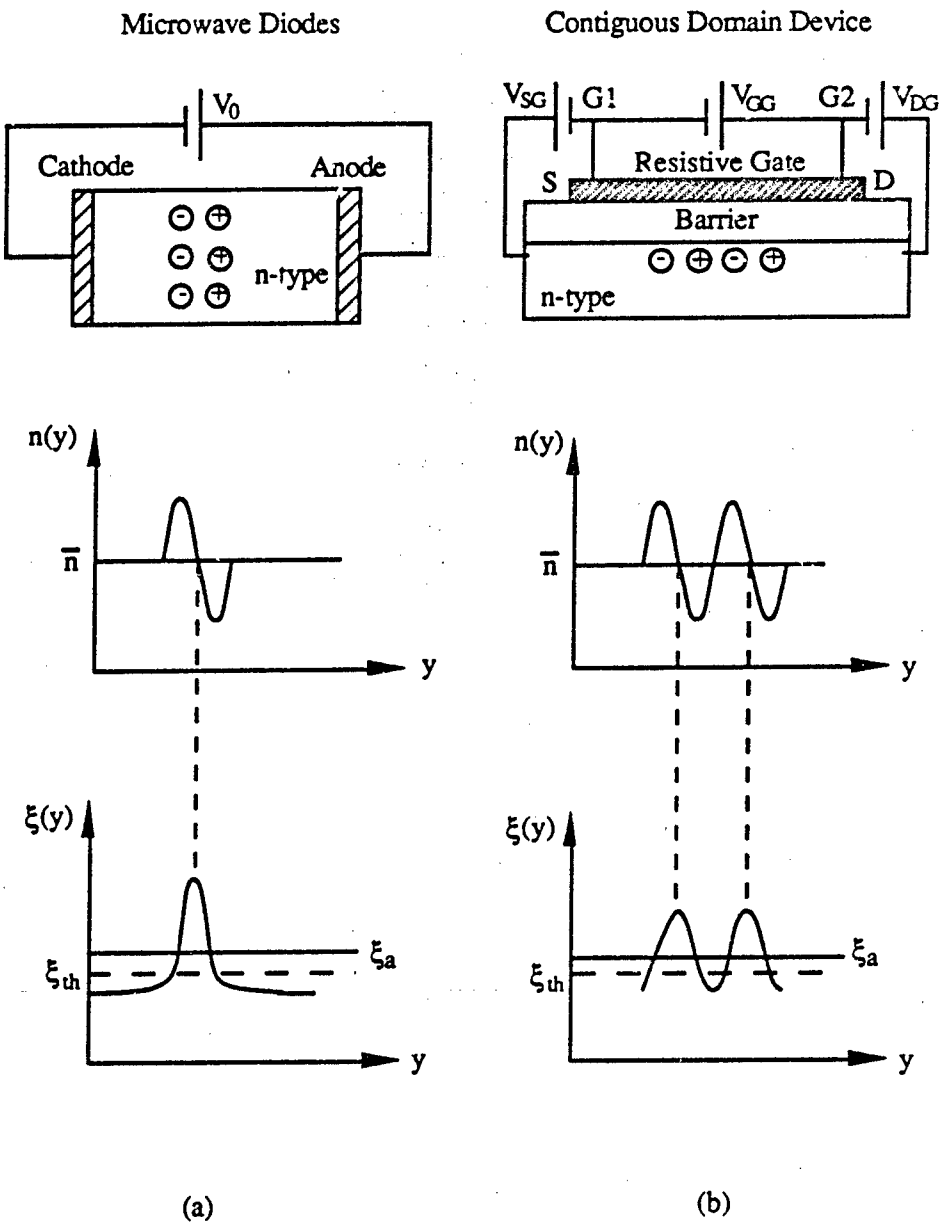


Figure 1.1 Schematic representation of (a) conventional microwave diodes, and (b) the contiguous domain oscillator.
In conventional devices, internal space charge alters the electrical field throughout the device, but in the CDO structure, internal space charge alters the field locally. This leads to the fundamental differences in operation of the two classes of devices [3].

where L is the drifting length. Since the domain drifting velocity v_d is approximately equal to the saturation velocity, the operation frequency is primarily determined by L. Once the device is fabricated, the frequency is not subject to significant change.

When these two-terminal devices are connected to a load circuit, V_0 is no longer constant. Their one-dimensional electrostatics are closely coupled to the voltage excursions in the external circuit. A limited amount of electronic frequency tuning is often achieved by varying circuit reactance using a varactor diode.

At present, all conventional diodes are produced in discrete form and operate in an external resonant circuit. This technology is a major limitation to their widespread use in compact, lightweight, low-cost systems that require a higher degree of integration. Moreover, the device performance depends on both intrinsic properties prior to packaging and its impedance matching in the waveguide circuit through the packaging parasitic circuit elements. Therefore, the application of monolithic fabrication techniques to the oscillators is desired. However, monolithic fabrication of these diodes and their matching, bias, and other passive circuits on the same chip for a fully integrated high performance microwave subsystem is not a easy task. Much research work has been devoted to that area [4-7].

1.2.2 Contiguous Domain Oscillator (CDO)

In order to allow a contiguous sequence of charge domains to coexist in the drifting channel, it is necessary to modify the electrostatic boundary conditions so that the local field of each domain are screened from the rest of the channel. This is the basic difference between the conventional oscillator and the CDO.

By employing a resistive gate on the device, it is possible to achieve space charge screening provided that the resistance of the gate is in the right range. As shown in Fig. 1.1(b), the high electric field provided by the resistive gate voltage V_{GG} biases the device into a region of negative differential mobility and causes charge domain to form. The image charge of the domain resides on the resistive gate, so that nearly all of the space-charge field is normal to the drift direction. Due to this special geometry, the presence of one charge domain does not alter the electric field in the remainder of the device. This permits a number of domains to coexist in the drifting channel simultaneously.

The operation of the CDO is shown in Fig 1.2. The barrier between the resistive gate and the channel enforces that electrons travel along the channel direction. This barrier could be a physical barrier provided by a high band-gap material in a MOSFET structure or a potential barrier provided by positive biases of source/drain with respect to gate1/gate2 in a

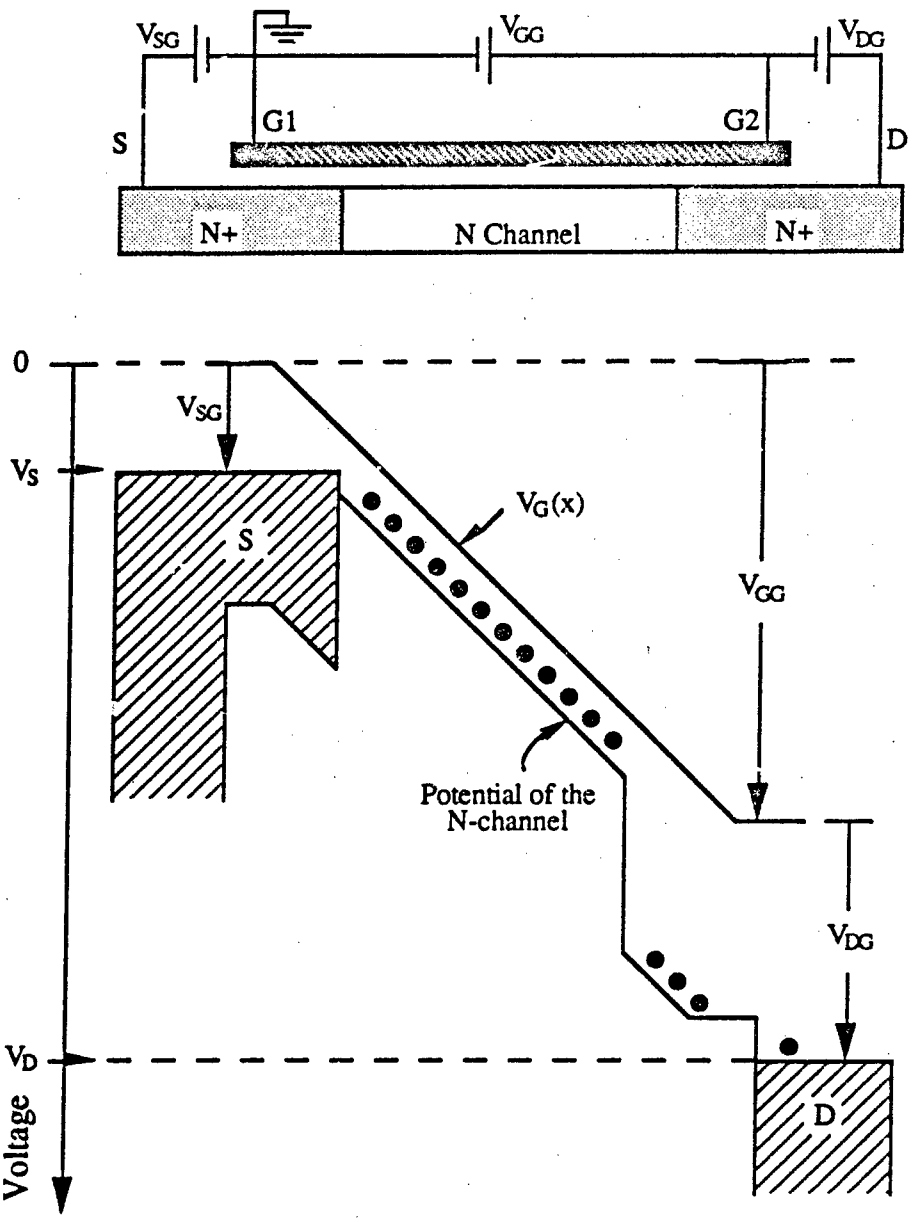


Figure 1.2 The operation of the CDO device.

MESFET structure. Since the CDO has four terminals and three applied voltages, it gives more control over the formation, transportation and extraction of charge packets. The resistive gate is used to provide a constant high electric field V_{GG} / L in the channel and to screen the space charge. The function of the source-to-gate1 voltage V_{SG} is to control the electron injection level. The drain junction at the high voltage end of the gate is biased so to collect any electrons that drift down the channel. With high enough V_{DG}, the current coming out of the drain is insensitive to the potential on the drain, making the device look like a current source. Therefore, no external resonant circuit is required, which greatly simplifies the circuit design.

Fig 1.3(a) shows the electron density under the condition of constant insertion rate (constant V_{SG}) as indicated by the original transient Time-Of-Flight (TOF) program [8]. The charge is distance d away from the gate. The different plots are at different times in the simulation as the charge front drifts from the source end of the channel towards the drain. The oscillation stabilized after several picoseconds. Eventually, the oscillation fills up the whole channel, continuously traveling from the source to the drain. Thus the oscillation is governed by the inherent periodic quasi-steady state transport properties of the carriers themselves.

Frequency tunability is realized by varying source to gate voltage V_{SG} which controls charge injection into the channel. When the electron concentration at the source is changed from one value to a larger value for a period of time and then returned to the original value (Fig. 1.3(b)),the oscillation frequency changes accordingly. This is a strong indication that the oscillation frequency can be electrically tuned instantaneously.

Since the CDO has a planar structure, its integration into the developing monolithic microwave system is straightforward.

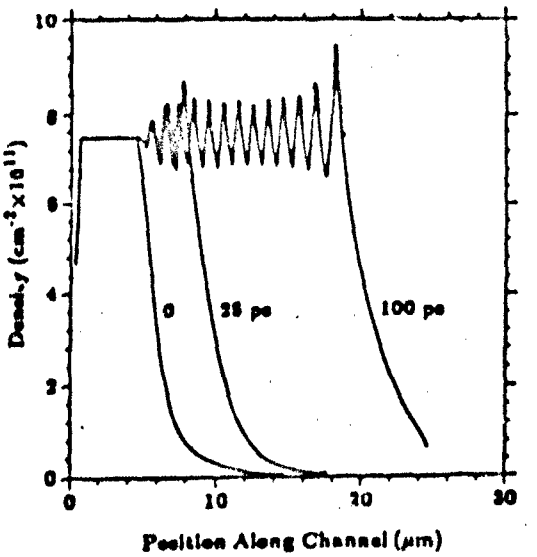


Figure 1.3(a) The time evolution of electron density in the MOSFET channel as electrons are introduced from the source. The source is modeled by a constant surface electron density at $n_s = 7.5 \times 10^{11}$ cm^{-2} from y=0 to y=5 μm. d=500 Å and drift field v_d = 7000 V/cm [8].

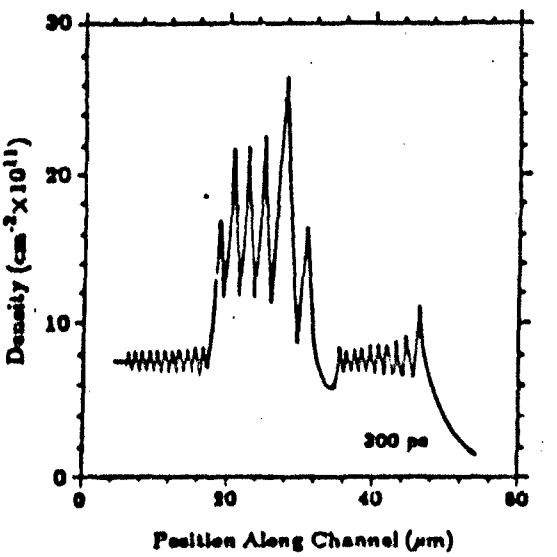


Figure 1.3(b) Effect of a step change in the injection level on the oscillation (MOSFET).The injection level was initially 7.5×10^{11} cm^{-2}, but was increased to 1.5×10^{12} cm^{-2} after 100 ps and returned to 7.5×10^{11} cm^{-2} after 200 ps [8].

1.3 Thesis Overview

The contiguous domain oscillator has great promise to become a useful microwave device for monolithic millimeter-wave integrated circuit (MMICs) applications. The verification of its existence, however, is not a simple task. This thesis is an important part of the continuing effort towards the understanding and realization of the contiguous domain oscillation mode.

This research project has gone through simulation, design, fabrication and characterization stages, but not necessary in that order. Some stages have been gone through several times for further investigation. The thesis is organized in such a way that it gives reader an overall view of the project. The order used does not represent the actual time sequence of the project. Some previous results have also been included for completeness.

Chapter 2 presents the steady-state analysis of the ideal RG-FETs, assuming a constant mobility. The analysis provides useful information about the regions of operation in the ideal RG-FET as well as the uniform channel condition and the pinch-off condition. Chapter 3 summarizes the transient simulations of the ideal RG-FETs with the full velocity-field curve. Oscillations ranging from 20 GHz to 60 GHz are observed. The dependence of frequency and power on electron density in the channel and the distance between gate and channel are presented. Chapter 4 first describes the fabrication procedure of the CDO devices made with the RG-MESFET structure, then presents the IV curve and microwave measurement results. Single domain oscillation mode, rather than contiguous domain mode was observed due to the high gate resistance. Chapter 4 also presents the CrSiO process development for the purpose of modifying the single domain RG-MESFET oscillator. In order to further understand the device, a simple equivalent circuit model is established in chapter 5 to simulate the different oscillation modes in the RG-FET devices. Finally, the conclusion and the recommendation for the future work are given in Chapter 6.

CHAPTER 2
STEADY STATE ANALYSIS OF THE IDEAL RG-FET

2.1 Introduction

In considering the behavior of the resistive-gate MOSFET device, particularly the CDO application, it is important first to understand the carrier behavior inside the device in the DC steady state. This knowlege provides a reference frame for analyzing the transient behavior, and can indicate the proper bias conditions for contiguous domain oscillation.

When the gate-to-gate voltage V_{GG} is set to zero in an RG-FET, it becomes a conventional FET. The static analysis of conventional FET's is well understood [9]. With non-zero V_{GG}, several interesting device states can occur. One of the most interesting is the uniform channel condition, where neither the channel charge per unit area nor the channel electric field vary from source to drain. Unlike the conventional FET device, where the uniform channel exists only when the drain-to-source voltage V_{DS} is zero, Coen and Muller have shown that the RG-MOSFET can have a uniform channel for non-zero V_{DS}, where appreciable drain current is available[10,11].

It is the purpose of this work that the basic I_D - V_D characteristics of the RG-FET device be understood as well as the free-carrier distribution, electric field, potential profile along the channel for all biases. These quantities are important to predict the electric characteristics of the device and lead to an easy physical interpretation of the modes of operation.

Two types of structure are of interest for the simulation: RG-MOSFET structure and RG-MESFET structure. Four basic assumptions employed for the following work are listed here: (1) gradual channel approximation [13] is applied, which states that the rate of change of the electrostatic variables (potential, electric field, etc.) in the channel direction are relatively smaller than the rate of change of the same variables in the vertical direction, (2) the resistive gate is a perfect linear voltage divider, (3) current flow is

parallel to the channel direction, i.e., leakage of electrons from the channel to the gate is negligible, and (4) the velocity - field relation is linear. Despite the above assumptions, the simulation does provide useful insight into the basic physical behavior of the device.

To model the RG-MOSFET, we extend the Pao-Sah model to include the linear potential drop along the resistive gate. This generalized Pao-Sah model is verified by comparison to a Time-Of-Flight transient simulation for the RG-MOSFET. We also derive analytic expressions for the I_D-V_D characteristics which are sufficiently accurate for first-order calculations.

The basic I-V characteristics for the RG-MESFET structure are also examined. This study is obtained by the TOF program. The uniform channel condition and the pinch-off condition are derived in a similar way as for the RG-MOSFET.

2.2 Generalized Pao-Sah Model for the RG-MOSFET

The static IV characteristics of a conventional MOSFET were derived by Pao and Sah [12] based on a one-dimensional model subject to the gradual channel approximation [13]. The same approach can be extended to compute the current-voltage characteristics for the RG-MOSFET.

Fig. 2.1 shows a cross-sectional view of an ideal RG-MOSFET structure, indicating standard terminals and dc voltage designations. As in the conventional MOSFET, carriers enter the structure through the source (S), leave through the drain (D), and are subject to the control or gating action of the gates (G1 & G2). The voltage applied to the source relative to the neutral substrate is V_S, the gate-1 voltage relative to the substrate is V_{G1} and the drain voltage relative to the substrate is V_D. The voltage applied between the gate-1 and gate-2 is V_{GG}. Finally, consistent with the source and drain designations, the drain current I_D for the p-bulk device is taken to be positive when flowing from drain to source inside the device.

2.2.1 Basic Equations

Neglecting the contribution from holes, the drain current of an RG-MOSFET can be related to the electron quasi-Fermi potential gradient, dv_N/dy, and the sheet charge density Q_N, by:

$$I_D = - W Q_N(y) \mu_n \frac{dv_N}{dy} \qquad (2.1)$$

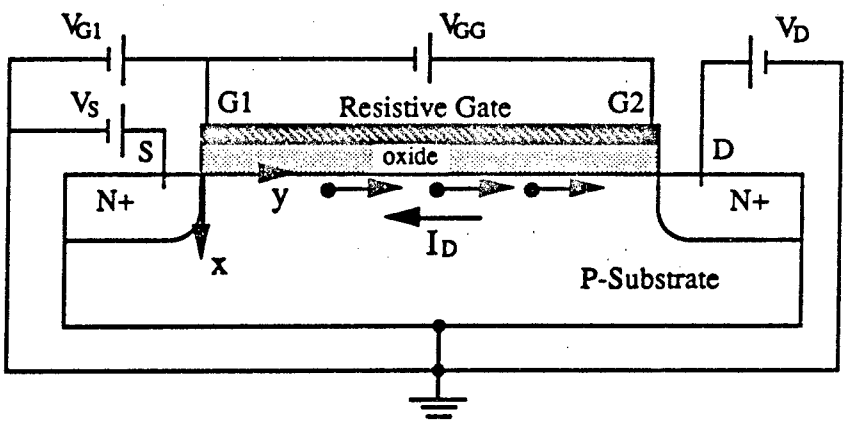


Figure 2.1 Cross-sectional view of the ideal RG-MOSFET structure showing the terminal designations and standard bias condition.

where $v_N = (E_F - F_N) / q$, W is the channel width, and μ_n is the electron effective surface mobility. After introducing dimensionless quantities (see Fig. 2.2) and integrating with respect to y on both sides of (2.1), I_D can be rewritten as:

$$I_D = -\frac{W\mu_n}{L}\frac{k_B T}{q}\int_{U_S}^{U_D} Q_N(\zeta)\, d\zeta \tag{2.2}$$

Here,

$$U_I(x) = [\, E_i(\text{bulk}) - E_i(x)\,] / k_B T \tag{2.3}$$

is the electrostatic potential,

$$U_F = [\, E_i(\text{bulk}) - E_F\,] / k_B T = \ln(N_A / n_i) \tag{2.4}$$

is the doping parameter, and

$$\zeta(y) = [\, E_F - F_N\,] / k_B T = v_N / v_T \tag{2.5}$$

is the quasi-Fermi-level splitting, all normalized to the normal voltage $v_T = k_B T/q$. U_{IS} is the U_I value at oxide-semiconductor interface (x=0), L the channel length, n_i the intrinsic carrier concentration, N_A the substrate doping(assumed uniform), U_S the source voltage in units of v_T, and U_D the drain voltage in units of v_T.

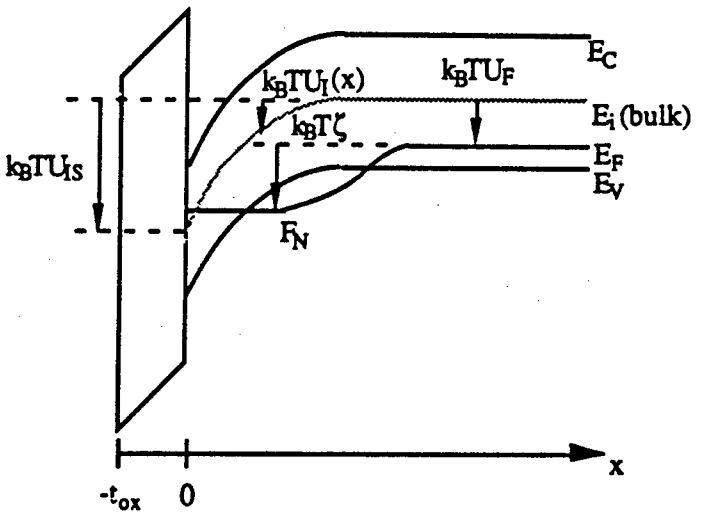


Figure 2.2 Graphical definition of dimensionless variables U_I (x), U_F and ζ_s.

The sheet charge density is expressed as [12]

$$Q_N(y) = - qn_iL_D \int_0^{U_{IS}} \frac{e^{U_I-U_F-\zeta(y)} - e^{-U_F-\zeta(y)}}{F(U_I,U_F,\zeta(y))} dU_I \tag{2.6}$$

where

$$L_D = \sqrt{\varepsilon_s \left(\frac{k_BT}{q}\right) \frac{1}{2qn_i}} \tag{2.7}$$

is the intrinsic Debye length, ε_s is the semiconductor dielectric constant, and

$$F(U_I,U_F,\zeta(y)) = \sqrt{e^{U_F}\left(e^{-U_I}+U_I-1\right) + e^{-U_F}\left(e^{U_I\zeta(y)}-U_I-e^{-\zeta(y)}\right)} \tag{2.8}$$

is the normalized electric field obtained from the 1-D solution of Poisson's equation.

The normalized surface potential U_{IS} in (2.6) is related to the position dependent gate voltage V_G (y) through Kirchoff's voltage law:

$$V_G'(y) = \frac{k_BT}{q}\left[U_{IS} + \text{Sign}(U_{IS}) \frac{\varepsilon_s}{C_{ox}L_D} F(U_{IS}, U_F, \zeta) \right] \tag{2.9}$$

where

$$V_G'(y) = V_G(y) - V_{FB} = V_{G1} + V_{GG}\frac{y}{L} - V_{FB} \tag{2.10}$$

V_{FB} is the flat band voltage, Sign(U_{IS}) the sign of U_{IS}, and C_{ox} the oxide capacitance per unit area. By integrating (2.2) with respect to an arbitrary ζ, the normalized distance along the channel measured from the source, y/L, may be related to ζ:

$$\frac{y}{L} = \frac{\int_{U_s}^{\zeta(y)} Q_N(\zeta)\, d\zeta}{\int_{U_s}^{U_D} Q_N(\zeta)\, d\zeta} \tag{2.11}$$

This relation is not valid in the post-pinch-off region.

2.2.2 Algorithm

Equations (2.2), (2.6), (2.9), (2.10) and (2.11) constitute a complete solution for the current-voltage characteristics of the RG-MOSFET, but they must be solved iteratively. Given V_{G1}, V_{GG}, and I_D, the drain voltage V_D can be calculated by the following steps:

(1) At the source, set y=0 and $V'_G(0) = V_{G1} - V_{FB}$.

(2) Guess a quasi-Fermi potential ζ at that y position and solve (2.9) iteratively for the surface potential U_{IS}.

(3) Substitute the calculated U_{IS} into (2.6) and numerically integrate for the inversion charge Q_N.

(4) Define a difference function $\Delta(y)$ obtained from (2.11) as

$$\Delta = \frac{\frac{W\mu_n}{L}\left(\frac{k_B T}{q}\right)}{I_D} \int_{U_s}^{\zeta(y)} Q_N(\zeta')\, d\zeta' - \frac{y}{L} \tag{2.12}$$

and calculate Δ. If Δ is not negligibly small, choose a different ζ in step (2) and repeat steps (2) through (4) until $\Delta \approx 0$.

(5) Change position y and calculate $V'_G(y)$ using (2.10). Go to step (2).

When V_{GG} is set to zero, the IV characteristics obtained from this generalied Pao-Sah (GPS) model are identical to the IV characteristics obtained using the Pao-Sah model.

2.2.3 Static Simulation Results

All the results shown here are computed for an n-channel RG-MOSFET device with the following parameters: $N_A = 1x10^{14}$ cm $^{-3}$, L =2 μm, W = 1 μm, $\mu_n = 1500$ cm^2 /V-s, $t_{ox} = 500$Å, $n_i = 1.45x10^{10}$ cm^{-3}, $\varepsilon_s = 11.8\ \varepsilon_0$, and $\varepsilon_{ox} = 3.9\ \varepsilon_0$, where $\varepsilon_0 = 8.854x10^{-14}$ F/cm.

2.2.3.1 IV Curves for Different Biases

The simulated I_D - V_D characteristics using the generalized Pao-Sah model are presented in Fig. 2.3 as solid lines. Fig. 2.3(a) is the IV curves for fixed V_S=1V, V_{G1}=6V and different gate-to-gate voltage V_{GG} from 0 to 8V, corresponding to an average electric field from 0 to 40,000V/cm. One can see that the I_D - V_D curves of the RG-MOSFET have the same general shape as the conventional MOSFET (V_{GG}=0), except that the pinch-off voltage V_{DP} and the saturation current I_{Dsat} are increased due to the application of gate-to-gate voltage V_{GG}. We can gain insight into the physical processes taking place in the device by examining the condition along the channel for one specific V_{GG} value. This is done in Fig. 2.4 for V_{GG} = 5V. The solution for V_{GG} = 0 are shown in Fig. 2.5, for comparison. From Fig. 2.4, we first note that at low values of drain current, a nonzero gate-to-gate voltage V_{GG} causes the inversion charge density to increase along the channel. Therefore, the device has a nonuniform channel at V_{DS}=0. If V_S , V_{G1}, and V_{GG} are fixed (Fig. 2.4(a)), the drain current increases with increasing drain bias V_D, corresponding to the line from point A to point U. We shall call this the "pre-uniform" region, where V_D is less than the drain voltage V_{DU} corresponding to the uniform channel condition. In the pre-uniform region, the diffusion current is determined by the slope of the electron density, which is in the opposite direction to the drift current, as shown in Fig. 2.6 (dots). The electron density at the drain is greater than at the source and is reduced by the applied drain voltage, as shown in Fig. 2.4(b). Fig. 2.4(c) shows that the electric field is nearly uniform along the channel.

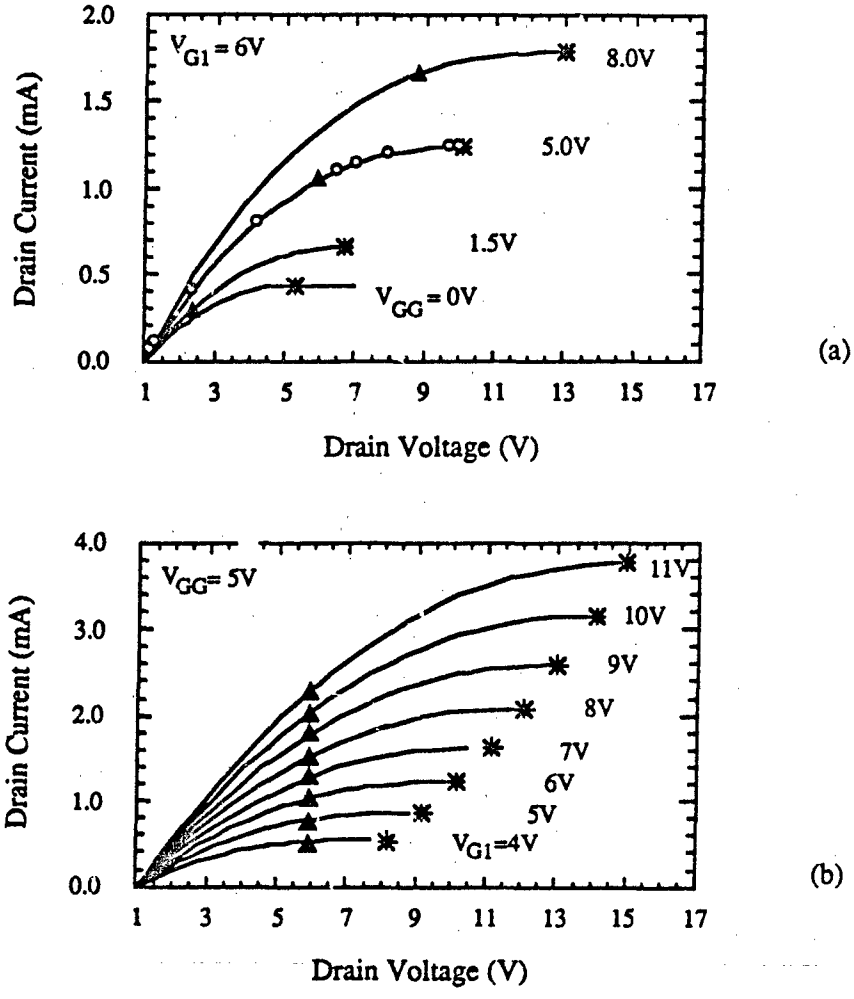


Figure 2.3 I_D-V_D characterisdcs for an RG-MOSFET given by the generalized Pao-Sah model (lines). Bias conditions are: (a) V_S = 1V and V_{G1} = 6V, (b) V_S = 1V, V_{GG} = 5V. Stars indicate pinch-off voltages calculated from (2.21), triangles indicate the uniform channel condition calculated from (2.20), and circles are currents calculated by a one-dimensional TOF transient simulation[6].

When the electron density at the source is just equal to the electron density at the drain, the RG-MOSFET has a uniform channel (point U). The electric field in the channel is now uniform, and the diffusion current is zero (Fig. 2.6, open diamonds). Notice that in the vicinity of V_{DU}, the surface channel acts more or less like a simple resistor.

For $V_D > V_{DU}$, the device is in the "post-uniform" region. The electron density at the drain decreases, reaching zero when $V_D = V_{DP}$. This corresponds to the line from point U to point P in Fig. 2.4(a). The electron density at the drain decreases, reaching zero when $V_D = V_{DP}$. This is referred to as the "pinch-off" condition. The region where $V_D > V_{DP}$ is designated as "pinch-off" region. In this region, the electric field at the source is pinned at its maximum. The diffusion current is now positive and increases dramatically at the drain (Fig. 2.6, open circles).

The reduction of the channel charge caused by increasing the drain bias is counteracted by the increase in channel charge caused by the linear increase of the gate bias. For this reason, pinch-off at the drain is delayed and the saturated drain current is considerably larger than in the MOSFET. The bigger the V_{GG}, the larger the drain current I_D at the same drain bias.

Comparing Fig. 2.4(c) and Fig. 2.5(c), one can see that the nonzero V_{GG} raises the overall electric field in the channel. Therefore, high electric field distribution across the channel can be achieved in the RG-MOSFET structure.

The inverted region of the conventional MOSFET is similar to the pre-uniform region of the RG-MOSFET if electron density distribution is examined. In both case, the drain has more electrons than the source does. However, the drain current is negative in conventional MOSFET.

Fig. 2.3(b) are the IV curves for fixed V_S=1V and V_{GG}=5V, and different gate1 voltage V_{G1} from 4V to 11V. As V_{G1} increases, the channel electron density increases, and drain current increases proportionally.

In Fig. 2.3(a), the results of a one-dimensional finite difference simulation[6] for V_{GG} = 5V are shown as circles. The finite difference simulation not only predicts the same steady-state current as the generalized Pao-Sah model, but gives the same electron density, electric field, and channel potential distributions as well.

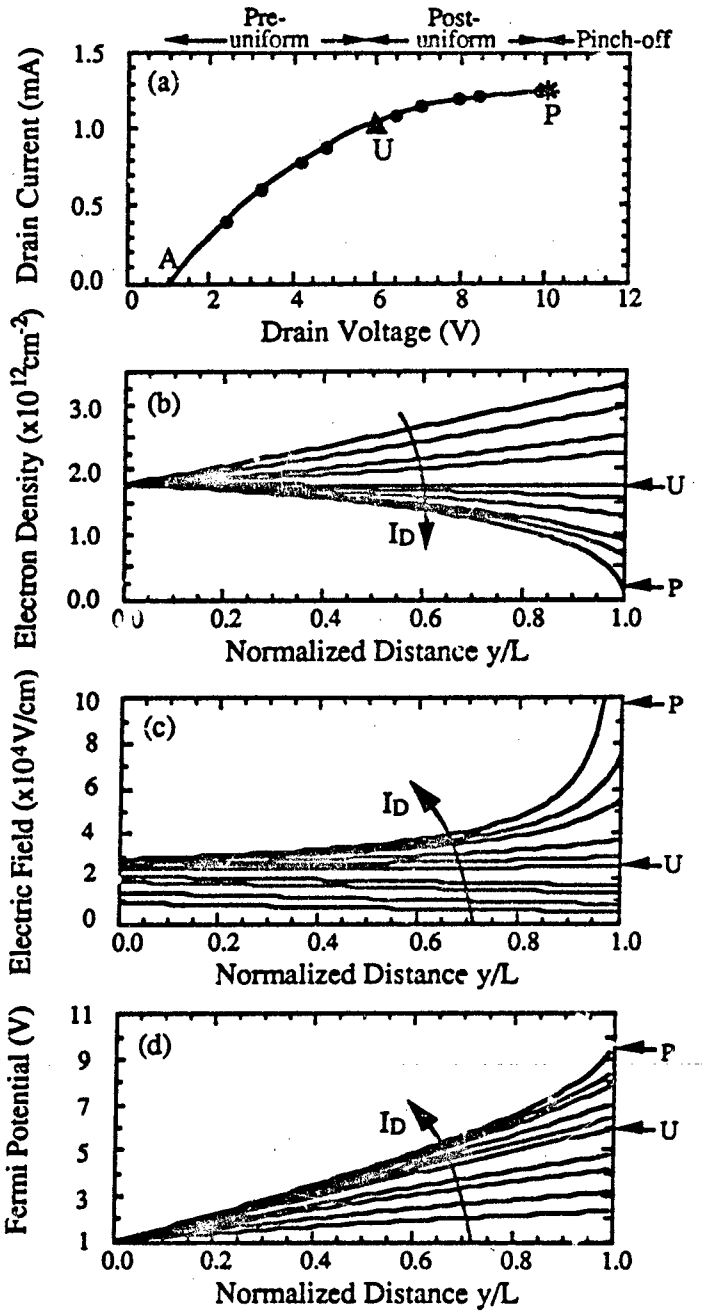


Figure 2.4 (a) I_D-V_D curve, (b) surface electron density n_s, (c) electric field ξ_y, and (d) Fermi potential v_N along the channel for the RG-MOSFET of Fig. 2.3, biased at V_S = 1V, V_{G1} = 6V, and V_{GG} = 5V, calculated using the generalized Pao-Sah model. Dots in (a) correspond to the lines in (b), (c) and (d). "U" and "P" mark the uniform channel and pinch-off conditions, respectively.

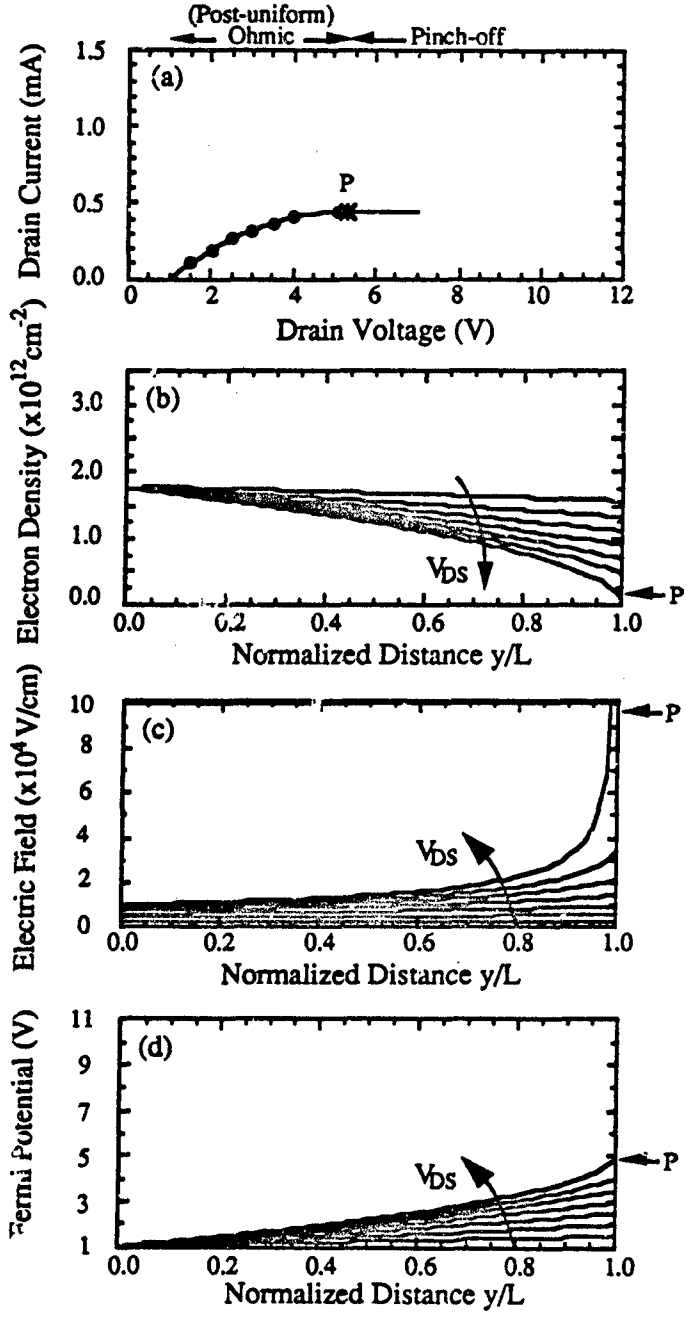


Figure 2.5 (a) I_D-V_D curve, (b) surface electron density n_s, (c) electric field ξ_y, and (d) Fermi potential v_N along the channel for a conventional MOSFET (identical to the RG-MOSFET of Fig. 2.3 except with $V_{GG} = 0$), biased at $V_S = 1V$ and $V_{G1} = 6V$, calculated using the standard Pao-Sah model. Dots in (a) correspond to the lines in (b), (c) and (d).

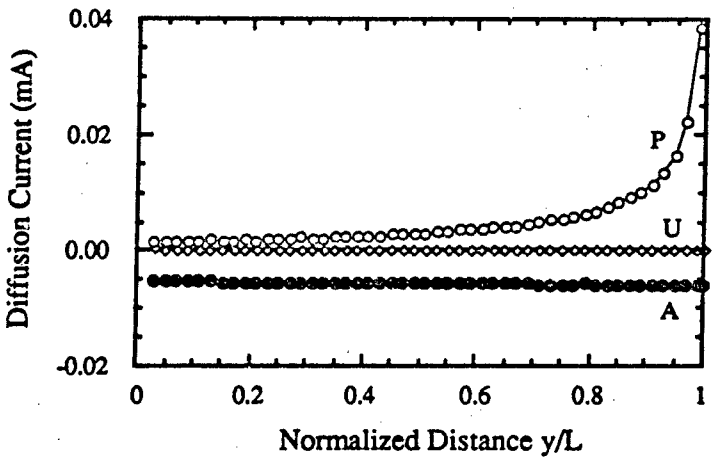


Figure 2.6 Diffusion current components for the RG-MOSFET biased at V_S=1V, V_{G1}=6V and V_{GG}=5V. A, U, and P correspond to Fig. 2.4(a).

2.2.3.2 Electric Field Distribution in the RG-MOSFET

One has to remember that the generalized Pao-Sah simulation is based on the gradual channel approximation. The simulation is only valid when $\xi_x >> \xi_y$. Fig. 2.7 compares the channel electrical field distribution $\xi_y(y)$ with the vertical electrical field distribution in the saturation region for different values of V_{G1} and V_{GG}.

Fig. 2.7 shows that the gradual channel approximation (GCA) is violated at the drain since the channel is first pinched-off there when $I_D=I_{Dsat}$. This violation also occurs for the conventional MOSFET. However, it is more series for non-zero V_{GG}. For fixed gate-to-gate voltage, the violation to the GCA occurs when V_{G1} is small (Fig. 2.7(b)).

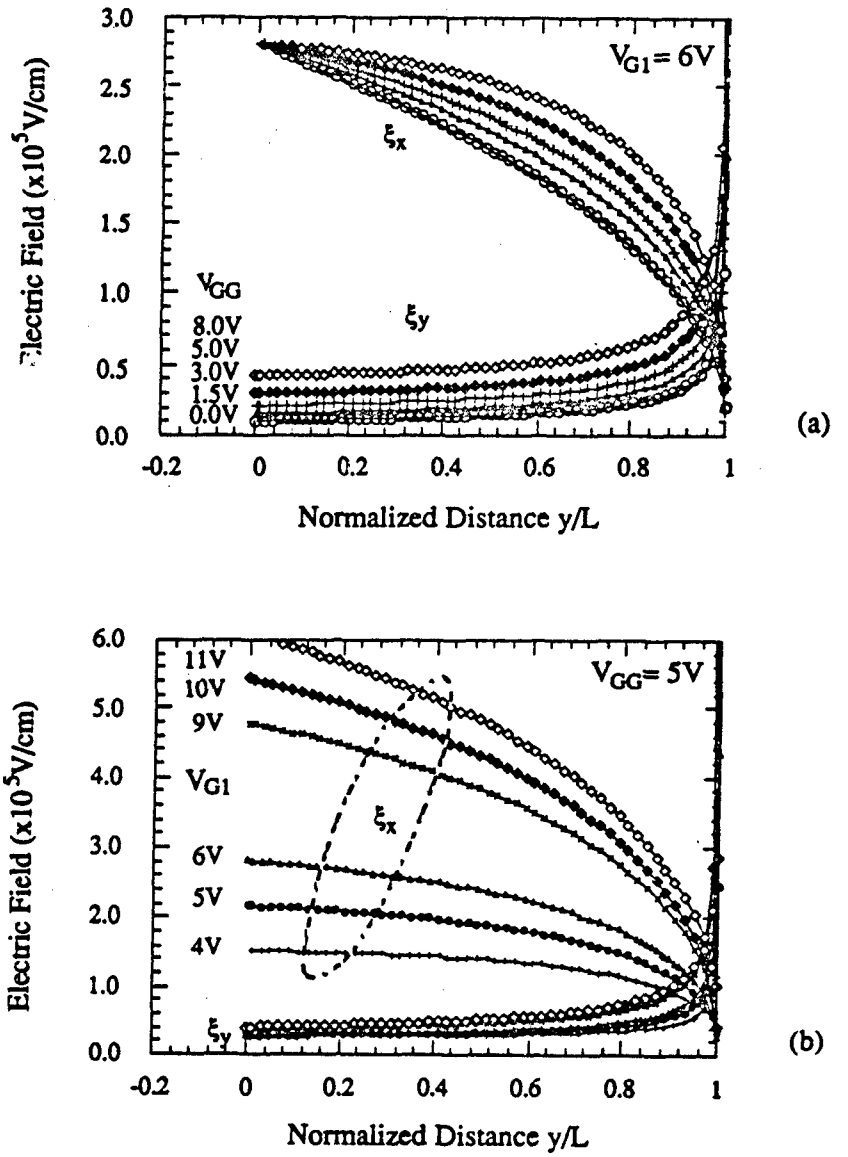


Figure 2.7 Effect of (a) gate-to-gate bias V_{GG}, and (b) gate1 bias V_{G1} on the distribution of electrical fields along the channel (ξ_y) and perpendicular to the channel (ξ_x). $I_D = I_{Dsat}$.

2.2.4 Simple Analytic Model for the RG-MOSFET

2.2.4.1 Uniform Channel Condition and Pinch-off Condition

The analytical equations used to describe the conventional MOSFET can be applied to the resistive gate device, provided that they are modified to account for the potential drop along the gate:

$$V_G(y) = V_{G1} + V_{GG}\frac{y}{L} \tag{2.13}$$

In strong inversion, the surface potential is $2\phi_F+v_N(y)$, where $v_N(y)$ is the quasi-Fermi level splitting and $\phi_F = k_BT/q \ln(N_A/n_i)$ is the Fermi potential of the substrate. Therefore, the sheet electron density is:

$$n_s(y) = \frac{C_{ox}}{q}\left[V_{G1} + V_{GG}\frac{y}{L} - 2\phi_F - v_N(y) - V_{FB} - \sqrt{2V_0}\sqrt{2\phi_F + v_N(y)} \right] \tag{2.14}$$

where

$$V_0 = \frac{\varepsilon_s q N_A}{C_{ox}^2} \tag{2.15}$$

is the body factor. Expanding the square root term of (2.14) around $v_N=V_S$ [15], we have:

$$\sqrt{v_N(y) + 2\phi_F} = \sqrt{V_S + 2\phi_F} + \frac{v_N(y) - V_S}{2\sqrt{V_S + 2\phi_F}} \tag{2.16}$$

Equation (2.14) becomes

$$n_s(y) = \frac{C_{ox}}{q}\left[V_{G1} + V_{GG}\frac{y}{L} - V_T - (1+\gamma)(v_N(y) - V_S) \right] \tag{2.17}$$

where

$$\gamma = \frac{\sqrt{V_0/2}}{\sqrt{2\phi_F + V_S}} \tag{2.18}$$

and

$$V_T = 2\phi_F + V_S + \sqrt{2V_0}\sqrt{2\phi_F + V_S} + V_{FB} \tag{2.19}$$

is the threshold voltage, defined as the gate-1 voltage relative to the bulk which causes a depletion-inversion transition at the source end of the channel.

A uniform channel is obtained when the sheet electron density and the electric field are independent of y. If $v_N(y)$ is taken to be a nearly linear function of position, $v_N(y) = V_S + V_{DS}(y/L)$, the uniform channel condition is derived from (2.17) [10,11]:

$$V_{DU} = V_S + \frac{V_{GG}}{1+\gamma} \tag{2.20}$$

V_{DU} values calculated using (2.20) are indicated by solid triangles in Fig. 2.3. They agree very well with simulated values. Since the above derivation does not involve the characteristics of the velocity-field curve, this uniform channel condition is universally valid.

If the drain current saturation is caused by the pinch-off at the drain, V_{DP} is found by setting y=L and $n_s(L)=0$ in (2.17),

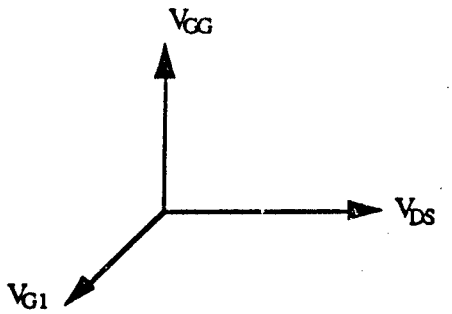
$$V_{DP} = V(L) = V_S + \frac{V_{G1} + V_{GG} - V_T}{1+\gamma} \tag{2.21}$$

Equation (2.21) has a very clear physical meaning. Recall that in the post-uniform region, the RG-MOSFET acts more or less like a MOSFET with a pinch-off voltage equal to $V_S+(V_{G1}-V_T)/(1+\gamma)$. But before this region, $V_{DS} = V_{GG}/(1+\gamma)$ has to be applied to achieve the uniform channel. Therefore, V_{DP} of the RG-MOSFET is bigger than V_{DP} of the MOSFET by an amount equal to $V_{GG}/(1+\gamma)$. (2.21) is used to calculate the pinch-off voltages in Fig. 2.3; these values are marked by stars in the figure. The calculated pinch-off voltage agree well with the onset of current saturation given by the GPS model.

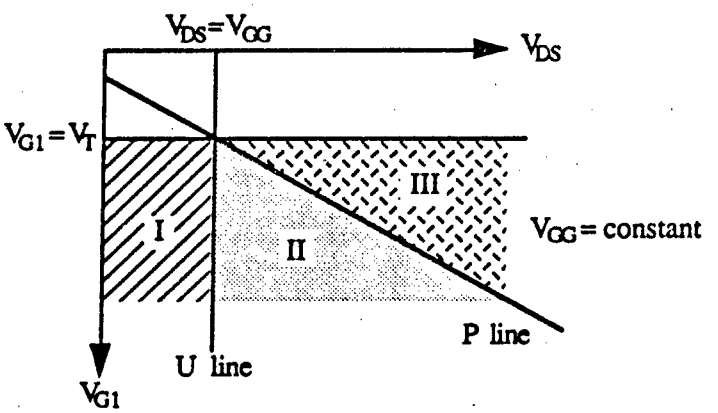
2.2.4.2 Regions of Operation of the RG-MOSFET

As discussed before, the RG-MOSFET has three regions of operation as summarized in Fig. 2.8. For simplicity, γ is set to zero. The U line indicates a uniform channel condition: $V_{DS} = V_{GG}$. The P line indicates a pinch-off condition: $V_{DS}=V_{G1} - V_T + V_{GG}$. All devices experience these three regions when the drain voltage increases. When V_{GG} is fixed (Fig. 2.8(b)), non-zero drain current only occurs for $V_{G1}>V_T$. When V_{G1} is fixed at any value greater than V_T (Fig. 2.8(c)), the U line and P line are parallel to each other. The pre-uniform region does not exist when $V_{GG}=0$, and the uniform channel occurs at $V_{DS}=0$.

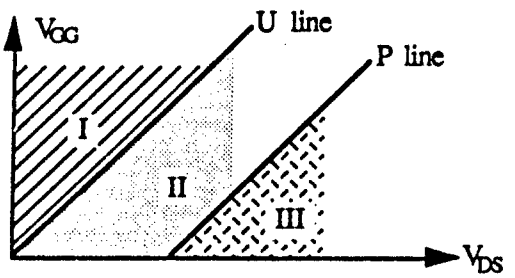
Since the uniform channel condition is universally valid for all shapes of velocity-field curves, the U line is important to the identification of the microwave oscillation in practical RG-MOSFET devices, provided that V_{DU}/L is greater than the threshold field for negative differential mobility.



(a)



(b)



(c)

Figure 2.8 Mode diagram illustrating the regions of operations (γ=0). I is the Pre-uniform region, II is the Post-uniform region, and III is the pinch-off region.
(a) Coordinates used, (b) V_{GG} is fixed,(c) V_{G1} is fixed.
U line: $V_{DS}(U)=V_{GG}$
P line: $V_{DS}(P)=V_{G1}-V_T+V_{GG}$

2.2.4.3 Simplified Analytic Model

An analytic expression for the drain current can be obtained by neglecting diffusion. By analogy with the conventional MOSFET, we may write:

$$I_D = -\frac{W\mu_n}{L}\int_0^L Q_N(y)\frac{dv_N}{dy}dy \tag{2.22}$$

where v_N is the channel Fermi potential. From (2.17), the sheet charge density is

$$\begin{aligned} Q_N(y) &= -C_{ox}[V_G(y) - V_T - (1+\gamma)(v_N(y) - V_S)] \\ &= -C_{ox}[V_{G1} - V_T - (1+\gamma)(v_N(y) - V_S) + V_{GG}\frac{y}{L}] \end{aligned} \tag{2.23}$$

Substituting (2.23) into (2.22) and integrating the right hand side from the source to the drain:

$$I_D = -\frac{W\mu_n C_{ox}}{L}[(V_{G1} - V_T)V_{DS} - \frac{1+\gamma}{2}V_{DS}^2 + \int_0^L \frac{V_{GG}}{L} y \frac{dv_N}{dy}dy] \tag{2.24}$$

The first two terms corresponding to the familar square law equation for the MOSFET [34]. The last term can be evaluated using the chain rule,

$$\begin{aligned} \int_0^L \frac{V_{GG}}{L} y \frac{dv_N}{dy}dy &= \frac{V_{GG}}{L}[\int_0^{LV_D} d(yv_N) - \int_0^L v_N(y)\,dy] \\ &= \frac{V_{GG}}{L}[LV_D - \int_0^L v_N(y)\,dy] \end{aligned} \tag{2.25}$$

As shown in Fig. 2.4(d), for $V_D \le V_{DU}$ the channel Fermi potential $v_N(y)$ can be approximated as a linear function of position:

$$v_N(y) = V_S + V_{DS}(\frac{y}{L}) \qquad , V_D \le V_{DU} \tag{2.26a}$$

For $V_D > V_{DU}$, we approximate $v_N(y)$ with a second-order polynomial:

$$v_N(y) = V_S + V_{DU}(\frac{y}{L}) + (V_{DS} - V_{DU})(\frac{y}{L})^2 \qquad , V_D > V_{DU} \tag{2.26b}$$

Figure 2.9 shows a comparison between the actual potential given by the GPS model and the approximate potentials given by (2.26). Agreement is satisfactory, except at drain biases very near pinch-off, $V_D \approx V_{DP}$.

Using (2.26), (2.25) can be expressed as

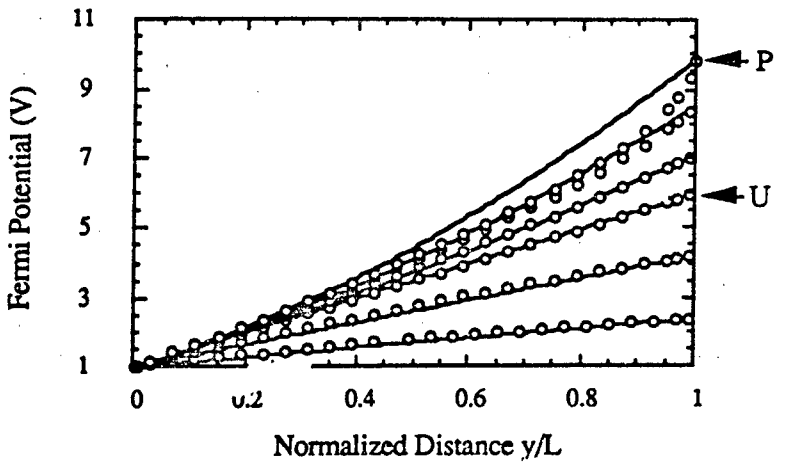


Figure 2.9 Channel Fermi potential given by the GPS model (circles) and by the analytical equations (lines) for the device of Fig. 2.3, biased at $V_S = 1V$, $V_{G1} = 6V$, and $V_{GG} = 5V$. The analytical equations (2.26a&b) provide good agreement with the GPS model except when the drain bias is close to pinch-off.

$$\int_0^L \frac{V_{GG}}{L} y \frac{dV}{dy} dy = \begin{cases} \frac{1}{2} V_{GG} V_{DS} & , V_D \le V_{DU} \\ \frac{2}{3} V_{GG} V_{DS} - \frac{1}{6} V_{GG} V_{DU} & , V_D > V_{DU} \end{cases} \tag{2.27}$$

Therefore, the drain current expression (2.24) becomes

$$I_D^{RG} = I_D^{MOS} - \frac{W\mu_n C_{ox}}{L} \begin{cases} \frac{1}{2} V_{GG} V_{DS} & , V_D \le V_{DU} \\ \frac{2}{3} V_{GG} V_{DS} - \frac{1}{6} V_{GG} V_{DU} & , V_D > V_{DU} \end{cases} \tag{2.28}$$

where

$$I_D^{MOS} = -\frac{W\mu_n C_{ox}}{L} \left[(V_{G1} - V_T) V_{DS} - \frac{(1+\gamma)}{2} V_{DS}^2 \right] \tag{2.29}$$

Equation (2.28) reduces to the familiar MOSFET current equation (2.29) when V_{GG} is set to zero. The drain current given by (2.28) reaches a maximum when V_D equals V_{Dsat} given by

$$V_{Dsat} = V_S + \frac{V_{G1} + \frac{2}{3}V_{GG} - V_T}{(1+\gamma)} \tag{2.30}$$

V_{Dsat} is slightly smaller than the pinch-off voltage given by (2.21). For $V_D > V_{Dsat}$, the drain current is

$$I_{Dsat}^{RG} = -\frac{W\mu_n C_{ox}}{2L}\left[\frac{(V_{G1} + \frac{2}{3}V_{GG} - V_T)^2}{(1+\gamma)} - \frac{1}{3}V_{GG}V_{DU}\right] \tag{2.31}$$

Figure 2.10 shows a comparison between the current predicted by the analytical model of (2.28) - (2.31) and the generalized Pao-Sah model. Agreement is quite reasonable over the whole range of bias voltages investigated, indicating that the analytical model is adequate for first-order calculations.

Note that (2.29) could be expanded to the standard "bulk charge" MOSFET equation [34] if (2.14) were used instead of (2.17) in deriving (2.22):

$$I_D^{MOS} = -\frac{W\mu_n C_{ox}}{L}\left[(V_{G1}-V_{TB})V_{DS} - \frac{1}{2}V_{DS}^2 - \frac{2\sqrt{2V_0}}{3}\left((2\phi_F+V_D)^{\frac{3}{2}} - (2\phi_F+V_S)^{\frac{3}{2}}\right)\right] \tag{2.32}$$

where

$$V_{TB} = 2\phi_F + V_{FB} + V_S \tag{2.33}$$

The drain current I_D^{RG} for a RG-MOSFET is still in the same form as in Equation (2.28). With this "bulk charge" model, I_D^{RG} reaches a maximum when V_D equals V_{Dsat} given by:

$$V_{Dsat} = V_S + \left[V_{G1} - V_{TB} + \frac{2}{3}V_{GG} + V_0 - \sqrt{V_0^2 + 2V_0(V_{G1} - V_{FB} + \frac{2}{3}V_{GG})}\right] \tag{2.34}$$

the corresponding uniform channel condition is:

$$V_{DU} = V_S + V_{GG} - V_1 + V_0 - \sqrt{V_0^2 + 2V_0(V_{GG} - V_1 + 2\phi_F + V_S)} \tag{2.35}$$

where

$$V_1 = -\sqrt{2V_0(2\phi_F + V_S)} \tag{2.36}$$

and the pinch-off voltage is:

$$\begin{aligned} V_{DP} &= V_S - 2\phi_F + \left(\sqrt{\frac{V_0}{2}} - \sqrt{\frac{V_0}{2} + V_{G1} + V_{GG} - V_{FB}}\right)^2 \\ &= V_S + \left[V_{G1} - V_{FB} + V_{GG} + V_0 - \sqrt{V_0^2 + 2V_0(V_{G1} - V_{FB} + V_{GG})}\right] \end{aligned} \tag{2.37}$$

Fig. 2.11 compares V_{DP} calculated from Eqn (2.22) and (2.37) for different doping densities. The approximation of (2.16) is fairly good for the doping densities and gate-to-gate voltages investigated.

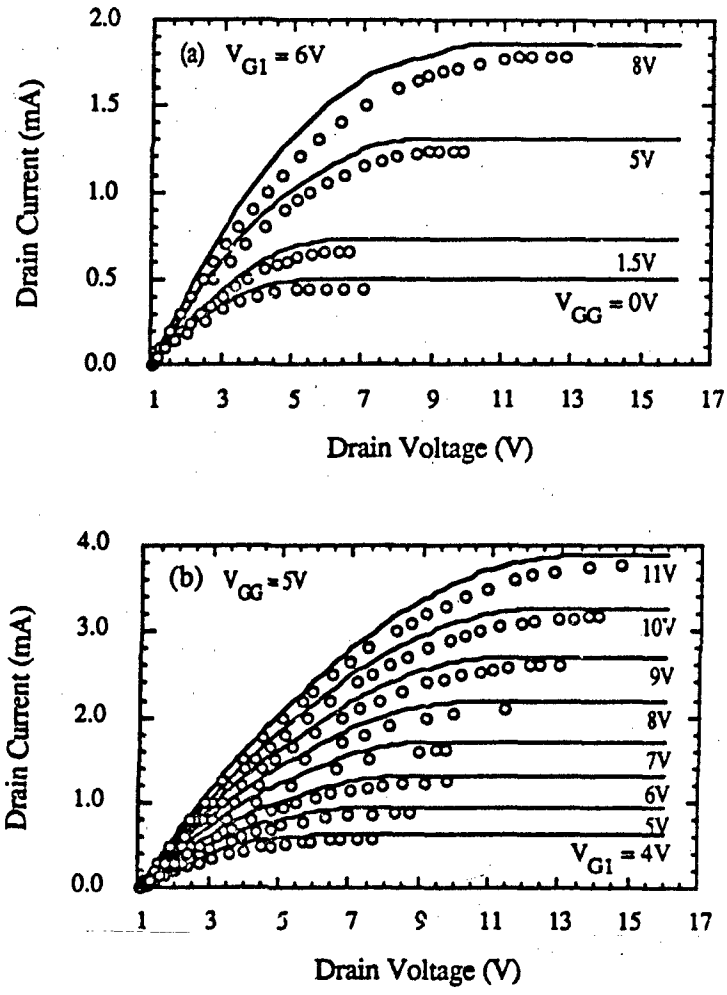


Figure 2.10 I_D-V_D curves given by the GPS model (circles) and the analytic model (lines) for the device of Fig. 2.3. Bias conditions are: (a) V_S = 1V and V_{G1} = 6V, (b) V_S = 1V, V_{GG} = 5V. Agreement is good, indicating the analytical model can be safely used for first-order calculations.

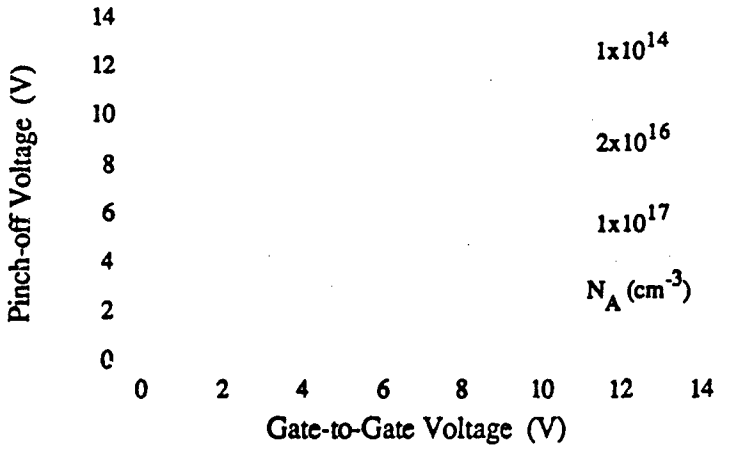


Figure 2.11 Comparison of V_{DP} calculations with and without the approximation of (2.16). Lines are calculated from (2.21), with the approximation. x's are calculated from (2.37), without the approximation. V_S=1V, V_{G1}=6V, and V_T=1.56V.

2.3 Simulation Results for the RG-MESFET

Although different in structure and threshold voltage, the operation of the RG-MESFET is similar to the RG-MOSFET. The conventional coordinate system is used as shown in

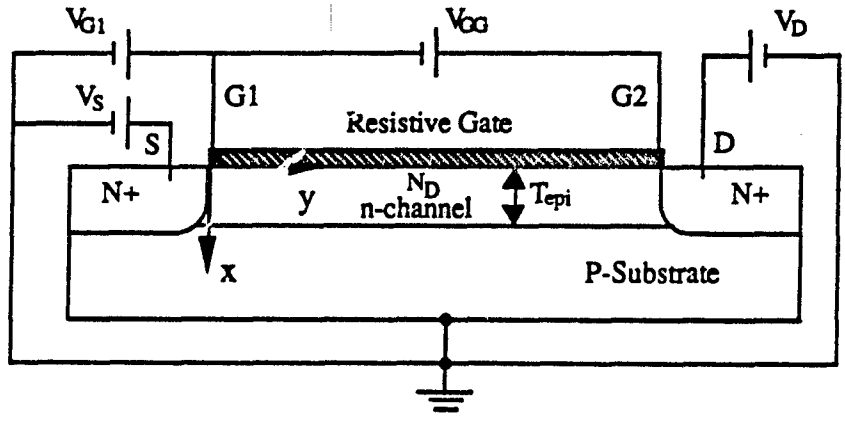


Figure 2.12 Cross section view of the ideal RG-MESFET structure showing the terminal designations and standard bias condition.

Fig. 2.12. The RG-MESFET has a doped channel with length L, width W and a doping density N_D.

2.3.1 IV Curves for the RG-MESFET

All the results shown here are for an n-channel RG-MESFET device with the following parameters: N_D=1.2 x 10^{17} cm^{-3}, L=2μm, W=1μm, μ_n =5200 cm^2 /V-s, T_{epi} =1500Å, and $\varepsilon_s = 12.9\ \varepsilon_0$. The simulations are done using the Time-of-Flight program (for a detailed description of the TOF program, see Chapter 3).

The simulated I_D - V_D characteristics for V_S =0.5V, V_{G1} = 0 and different gate-to-gate bias V_{GG} are presented in Fig. 2.13(a). The curves of non-zero V_{GG} are similar in shape to the conventional MESFET (V_{GG}=0), only the uniform channel and pinch-off voltages are increased due to the same reason as discussed for RG-MOSFET in section 2.2.3.1. The current does not go to zero for non-zero V_{GG} due to the assumption in the program that restrict the current flow only in the channel direction. In the region where V_D<2V, the Schottky diode is forward biased, causing a large amount of electrons to flow from the channel to the gate. The simulation is not valid anymore. When $V_D < V_S$, the drain current is negative for V_{GG}=0.

With V_{GG} fixed at 2V, the IV curves for V_{G1}=0 and different V_S are shown in 2.13(b). Increasing V_S reduces the number of electrons at the source. Consequently, the average electron density in the channel is decreasing.

Fig. 2.14 and 2.15 show the comparison between the RG-MESFET and the conventional MESFET. In the conventional MESFET (Fig. 2.14(b)), uniform channel occurs only when V_D=V_S, and the uniform channel current is zero. In the case of $V_D < V_S$, the drain has more electrons than the source, and electrons flow from the drain to the source, resulting in negative drain current. With non-zero V_{GG} (Fig. 2.14(a)), however, I_D is positive even when the drain voltage is smaller than the source voltage. In other words, the current at V_D=V_S for RG-MESFET is not zero, as pointed by the U point in Fig. 2.14(a).

Again, the non zero V_{GG} raises the overall electric field in the channel (Fig. 2.14(c) & Fig. 2.15(c)). High electric field distribution is achievable with the RG-MESFET structure.

So, the IV curves, electron density, electric field and potential distributions for an ideal RG-MESFET are similar to that of the ideal RG-MOSFET. There are also three regions of operation divided by the uniform channel condition and the pinch-off condition. However, unlike the RG-MOSFET, where the maximum electron density at specific point in the

channel is determined by the gate voltage at that point, the maximum electron density in an RG-MESFET channel is limited by the product of channel doping density and the channel thickness $N_D T_{epi}$.

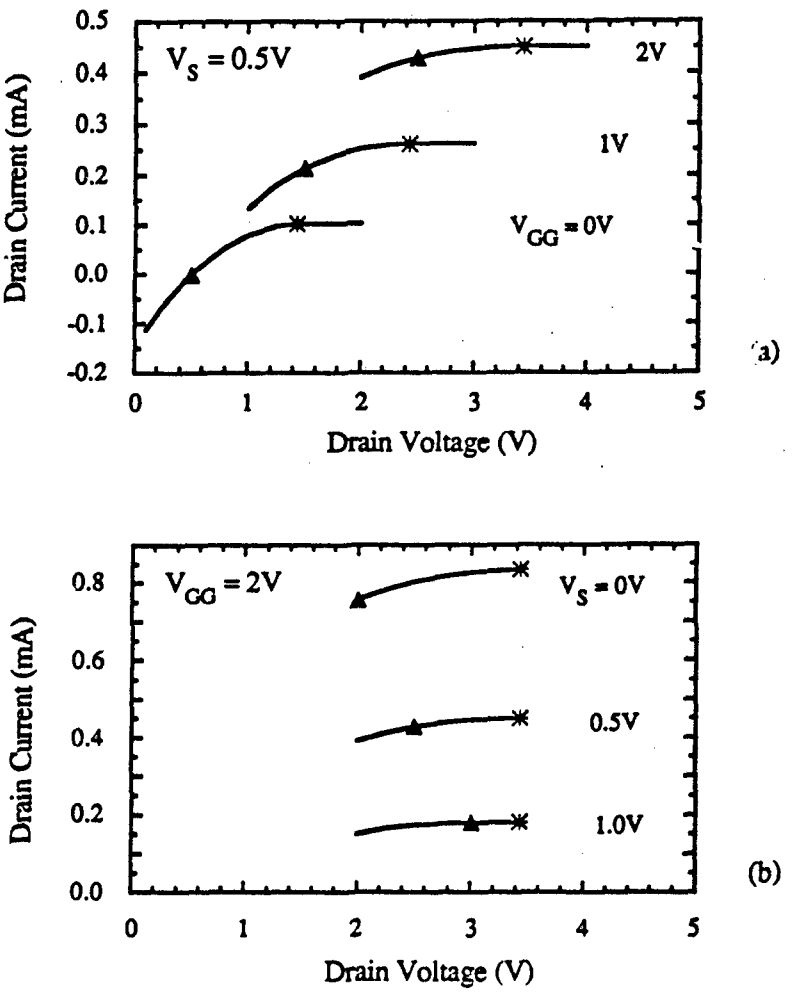


Figure 2.13 I_D-V_D characteristics for an RG-MESFET given by the TOF program (lines).Bias conditions are: (a) $V_S = 0.5V$ and $V_{G1} = 0V$, (b) $V_{G1} = 0V$, $V_{GG} = 2V$. Stars indicate pinch-off voltages calculated from (2.47), triangles indicate the uniform channel condition calculated from (2.46).

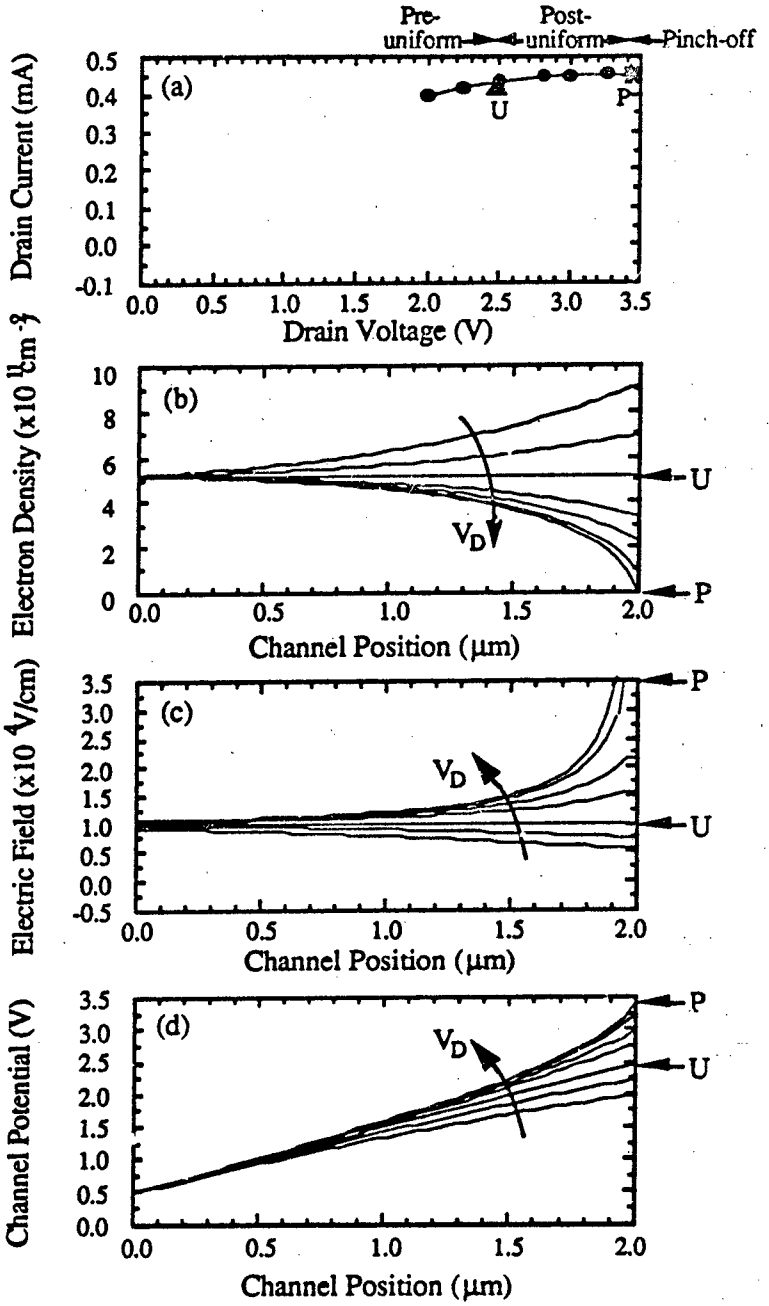


Figure 2.14 (a) I_D-V_D curve, (b) surface electron density n_s, (c) electric field ξ_y, and (d) Fermi potential v_N along the channel for the RG-MESFET of Fig. 2.13, biased at $V_S = 0.5V$, $V_{G1} = 0V$, and $V_{GG} = 2V$, calculated using the TOF program. Dots in (a) correspond to the lines in (b), (c) and (d). "U" and "P" mark the uniform channel and pinch-off conditions, respectively.

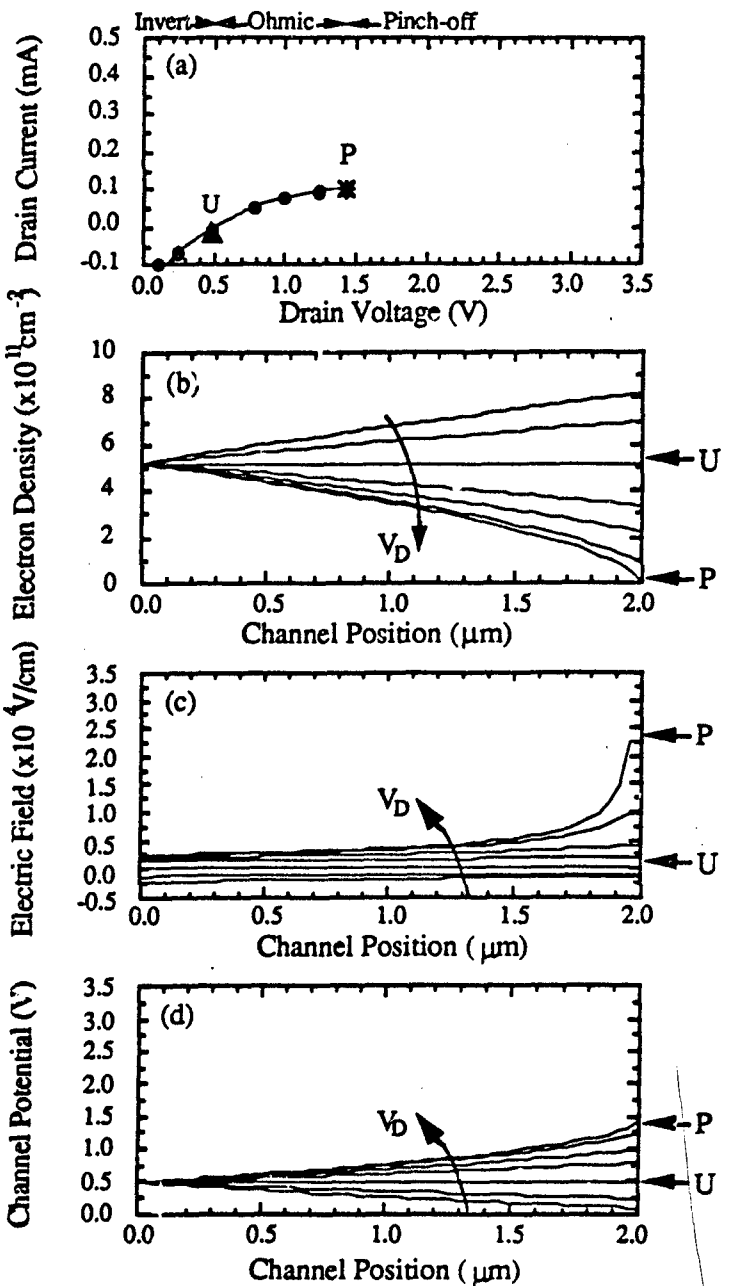


Figure 2.15 (a) I_D-V_D curve, (b) surface electron density n_s, (c) electric field ξ_y, and (d) Fermi potential v_N along the channel for the RG-MESFET of Fig. 2.13, biased at V_S = 1V, V_{G1} = 6V, and V_{GG} = 5V, calculated using the TOF program. Dots in (a) correspond to the lines in (b), (c) and (d). "U" and "P" mark the uniform channel and pinch-off conditions, respectively.

2.3.2 Uniform Channel Condition and Pinch-off Condition for the RG-MESFET

Assuming that the undepleted channel is neutral, the position dependent sheet electron density in a doped RG-MESFET is:

$$n_s(y) = N_D [x_{d2}(y) - x_d(y)] \tag{2.38}$$

where x_d is the depletion width of the Schottky junction, and $T_{epi} - x_{d2}$ is the depletion width in the channel due to channel-substrate junction (Fig. 2.16(a)). If the substrate is semi-insulating,

$$x_{d2} = T_{epi} \tag{2.39}$$

x_d can be calculated by the abrupt p+ n junction expression [16]:

$$x_d(y) = \sqrt{\frac{2\varepsilon_s}{qN_D}(v_N(y) - V_G(y) + V_{bi})} \tag{2.40}$$

where $v_N(y)$ is the channel Fermi potential, relative to the Fermi level in the substrate, and

$$V_{bi} = \phi_{Bn} - \frac{E_C(\text{channel}) - F_N}{q} \tag{2.41}$$

is the built-in potential for a Schottky junction, and ϕ_{Bn} is the barrier height (Fig. 2.16(b)).

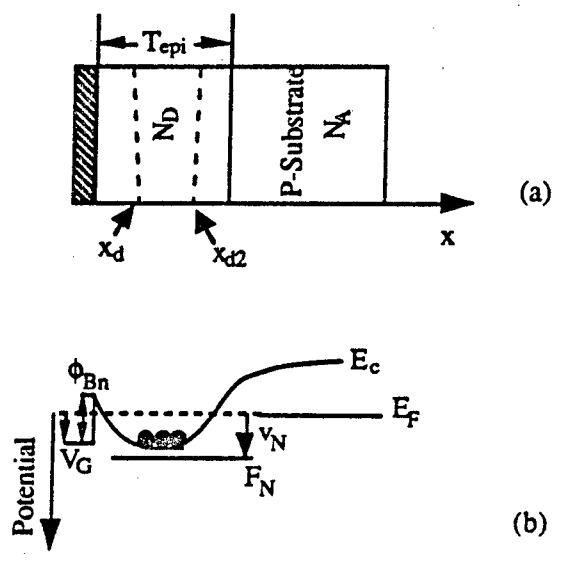


Figure 2.16 Cross sectional view and simple band diagram for a MESFET structure.

For uniform n_s, the quantity inside the square root has to be constant, i.e.,

$$v_N(y) - V_G(y) = \text{const.} \tag{2.42}$$

When the uniform channel forms, the channel Fermi potential is a linear function of the position:

$$v_N(y) = V_S + V_{DS}\frac{y}{L} \tag{2.43}$$

Since

$$V_G(y) = V_{G1} + V_{GG}\frac{y}{L} \tag{2.44}$$

the uniform channel condition is:

$$V_{GG} = V_{DS} \tag{2.45}$$

i.e.,

$$V_{DU} = V_S + V_{GG} \tag{2.46}$$

Equation (2.46) is similar to the uniform channel condition for an RG-MOSFET (Equation (2.20)). Values of V_{DU} calculated from (2.46) are indicated by the triangles in Fig. 2.13.

The pinch-off voltage can be obtained by setting y=L and $x_d = T_{epi}$ in (2.40):

$$V_{DP} = V_{G1} + V_{GG} + \frac{qN_D}{2\varepsilon_s}T_{epi}^2 - V_{bi} \tag{2.47}$$

V_{DP} values calculated from (2.47) are shown as stars in Fig. 2.13.

2.4 Conclusion

By taking into account the gate-to-gate bias V_{GG}, the steady-state simulations of the long channel RG-FET devices with constant mobility have been performed. The simulation from both generalized Pao-Sah model and Time-of-Flight program indicated that the I_D-V_D curve of the RG-FET have the same general shape as that of conventional FET's. However, internally, the operation of the RG-MOSFET experiences three regions for positive current. They are divided by the uniform channel condition and the pinch-off condition. The pre-uniform region is solely caused by the non-zero V_{GG}. The post-uniform region and the pinch-off regions are very similar to the conventional FET's ohmic and pinch-off regions.

With non zero V_{GG}, higher electric field values are obtained across the channel, assuming constant mobility. The CDO operation requires high electric field in the channel With realistic velocity field curve of GaAs, charge oscillation is possible once the electric field distribution exceeds the threshold field ξ_{th} in a resistive gate FET.

The uniform channel condition is universally true in spite of the shape of the velocity-field curve. This condition can be used as an initial biasing point for obtaining the contiguous domain oscillation.

CHAPTER 3
TRANSIENT ANALYSIS OF THE IDEAL FET DEVICE

This chapter summarizes the large-signal operation characteristics of the ideal contiguous domain oscillator, as obtained by the original Time-Of-Flight (TOF) program. This TOF program was developed by J. A. Cooper in 1980 and was used to simulate the high-field velocity of electrons in inversion layers [14, 17]. The detailed procedure of the TOF program is described in section 3.1. Section 3.2 and 3.3 summarize the TOF simulation results for both RG-MOSFET and RG-MESFET contiguous domain oscillators, where the effect of gate control and the sheet electron density in the channel on the oscillation frequencies and amplitudes are presented.

3.1 Description of the Original TOF Program

3.1.1 Basic Assumptions

The basic assumptions used in the TOF program are: (1) ideal gate (perfect linear voltage divider), and (2) one-dimensional current flow along the channel. The full velocity-field curve v - ξ is used in the simulation in order to observe the oscillation behavior.

Although different in structure, both the RG-MOSFET and RG-MESFET can be simulated with the TOF program, which uses a finite difference technique to solve the continuity equation for the electron concentration per unit width $n_l(i)$ along the channel. Fig. 3.1 shows the cross section, charge density, and energy band diagram along the direction perpendicular to the channel for both MOSFET and MESFET.

It can be seen that in MOSFET structure, the electrons (minority carriers) are confined to the interface within a very narrow layer. This allows the removal of the dimension into the substrate. Surface electron density n_s is easily defined and so is the electron density per unit width: $n_l = n_s \Delta y$. In the MESFET structure, electrons (majority carriers) move along the

undepleted portion of the channel (N) region. The assumptions in the TOF program for the MESFET are that the electrons occupy the undepleted portion of the epi-layer with a volume density equal to the doping density. This way, the electron density per unit width can be defined as $n_l = N_D(x_{d2}-x_d)\Delta y$ for each grid point positioned at the center of the charge layer $x_m(i)$. In reality, the doped channel formed by ion-implantation exhibits a Gaussian distribution. One can closely approximate ion implantation profile by using an effective uniform profile [35].

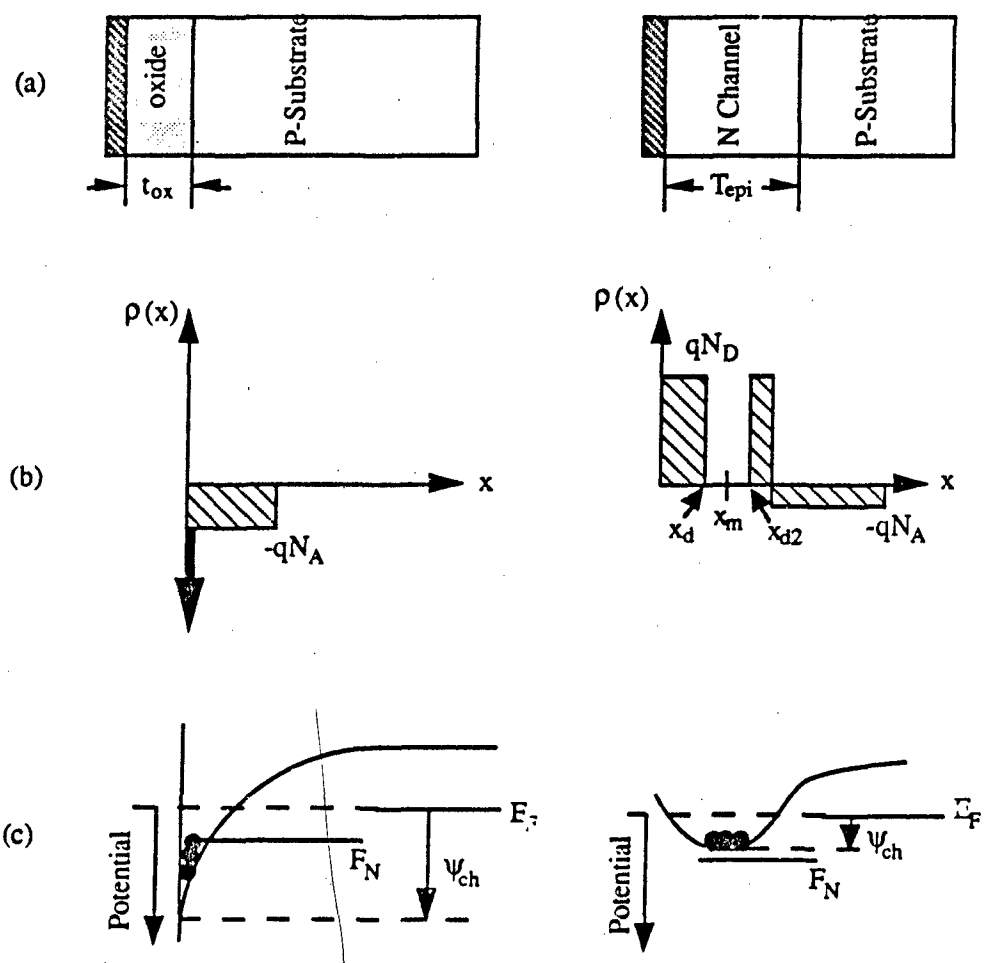


Figure 3.1 (a) Cross section, (b) charge density, and (c) potential from gate to substrate for MOSFET and MESFET structures.

Having made the above assumptions, the numerical treatments of MOSFET and MESFET really are the same, in spite of the fact that the electrostatics are different for the two structures. Fig. 3.2 shows the equivalent circuit of the simulated device corresponding to the cross section in Fig. 2.1 (MOSFET) and Fig. 2.12 (MESFET). The gate is represented by a series of ideal voltage source. The channel is modeled by a series of current sources, each of which is determined by the number of electrons and the electric field at that point.

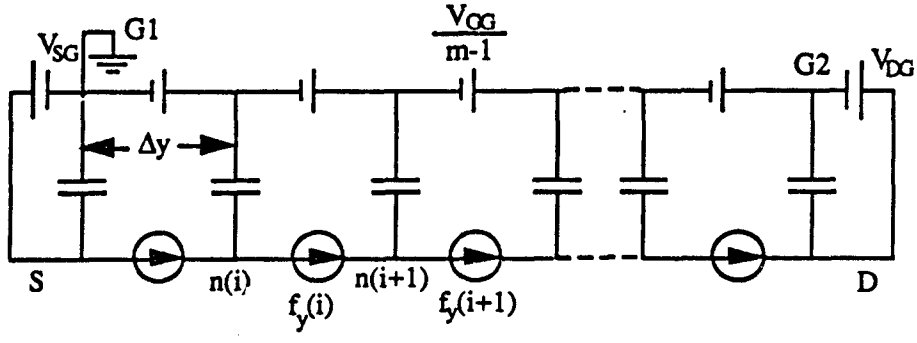


Figure 3.2 Generalized equivalent circuit of the simulated device in the TOF program, corresponding tc the cross section of the MOSFET in Fig. 2.1 and the MESFET in Fig. 2.12.

3.1.2 Basic Equations

Two basic equations describe carrier transport (continuity equation) and space-charge balance (Poisson's equation) in an n-channel FET device. Without the electron-hole generation and recombination, the two equations are:

$$\frac{\partial n_v}{\partial t} - \frac{1}{q} \nabla j_N = 0 \tag{3.1a}$$

$$- \varepsilon_s \nabla^2 \psi_{ch} = \rho \tag{3.1b}$$

with

$$j_N = - q n_v \nu(\nabla \psi_{ch}) + qD(\nabla \psi_{ch}) \nabla n_v \tag{3.2}$$

where n_v is the electron density per unit volume, ψ_{ch} is the electrostatic potential in the channel, referenced to the Fermi level in the substrate as indicated in Fig. 3.1(c), ρ is the net charge density in the channel, $v(\nabla\psi_{ch})$ and $D(\nabla\psi_{ch})$ are the electron velocity and diffusivity, respectively, both are function of electric field. Using assumption (1) and (3), and noting that the channel is in the y direction, the above equations become:

$$\frac{\partial n_v}{\partial t} = \frac{1}{q}\frac{\partial j_{Ny}}{\partial y} \tag{3.3a}$$

$$\frac{\partial^2 \psi_{ch}}{\partial x^2} = -\frac{\rho}{\varepsilon_s} \tag{3.3b}$$

with

$$j_{Ny} = -qn_v\, v\left(\frac{\partial \psi_{ch}}{\partial y}\right) + qD\left(\frac{\partial \psi_{ch}}{\partial y}\right)\frac{\partial n_v}{\partial y} \tag{3.4}$$

Since we work with the electron density per unit width n_l on each grid point, the final form of the continuity equation after discretization is:

$$n_l(i,\, t+\Delta t) = n_l(i,t) + \frac{\Delta t}{W(i)}\left(f_y(i-1,\, t) - f_y(i,t)\right) \tag{3.5}$$

where i is the index for the discretized position along the channel, and Δt is the self-adjustable time interval. For convenience, the electron flux in the channel direction f_y(#/s) is defined to be in the opposite direction of the current densities j_{Ny}

$$\begin{aligned} f_y(i,t) &= -W(i)\,\frac{\int_0^{\infty} j_{Ny}\, dx}{q} \\ &= W(i)\left(n_l(i,t)\,\frac{v(i,t)}{\Delta y} - \frac{(n_l(i+1,t) - n_l(i,t))}{\Delta y}\,\frac{D(i,t)}{\Delta y}\right) \end{aligned} \tag{3.6}$$

Basically, the program solves equation (3.3) - (3.6) at various instants of time during a cycle of oscillation. Given the instantaneous distribution of the electron density and terminal boundary conditions, the program determines the channel potential by solving (3.3b). Knowing the channel potential and the electron concentration, the instantaneous electron particle current (including the dependence of carrier mobility on electric field) can be calculated using (3.4) from which the time derivative of the carrier concentration can be calculated. From the time derivative of the carrier concentration, the program computes the carrier distributions an instant in time later (3.5), and repeats the cycle.

3.1.3 Algorithm

The algorithm used to solve the above equations is a simple forward difference scheme. i.e., the electron densities at time t+Δt are calculated in terms of only quantities at time t as indicated by Equation (3.5). The coupled equations (3.5) and (3.6), controlling the system variables electron concentration and the flux in the channel directions, are updated based on their values of previous time and treated separately. This requires the two equations be coupled closely by small updates of each system variable [18].

Given the bias V_{SG} and V_{DG}, the electron densities at source and drain can be calculated. Electron densities (#/cm) at other nodes $n_l(i)$ can be assumed to be the linear taper from the source to drain at time t = 0. The gate voltage $V_G(i)$ is ideal, and always varies linearly from gate1 to gate2 electrodes. The potential in the channel is a function of the electron density and the gate voltage as determined by 1D Poisson's equation (3.3b). The electric field is the gradient of the potential. From the empirical velocity-field curve and diffusivity-field curve, the flux in the channel f_y can be obtained through Eqns (3.4) and (3.6). At this point, a time step Δt is taken, the electron densities are updated according to Eqn (3.5). If the electron concentration changes more than 0.5% for any node in the channel, the time step is reduced and the electron concentration is recalculated. The new flux can be calculated once the electron density is accepted. If the newly calculated flux differs from the old flux by greater than 1%, the entire electron concentration, potential and the flux calculation are redone with a smaller time step. This keeps the currents (proportional to flux) from changing the electron concentration too quickly and helps to control the simulation. One cycle of the time iteration is done when the flux is accepted.

There are three types of boundary conditions for this 1D problem. One can either (1) fix the electron density at the source and drain, (corresponding to giving V_{SG} and V_{DG} to find drain current I_D), or (2) fix the source electron density and drain current (corresponding to giving V_{SG} and I_D to find V_D), or (3) fix the drain electron density and drain current (corresponding to giving I_D and V_D to find V_{SG}).

The flow chart of the TOF program is shown in Fig. 3.3. The key steps are discussed in depth in the following sections.

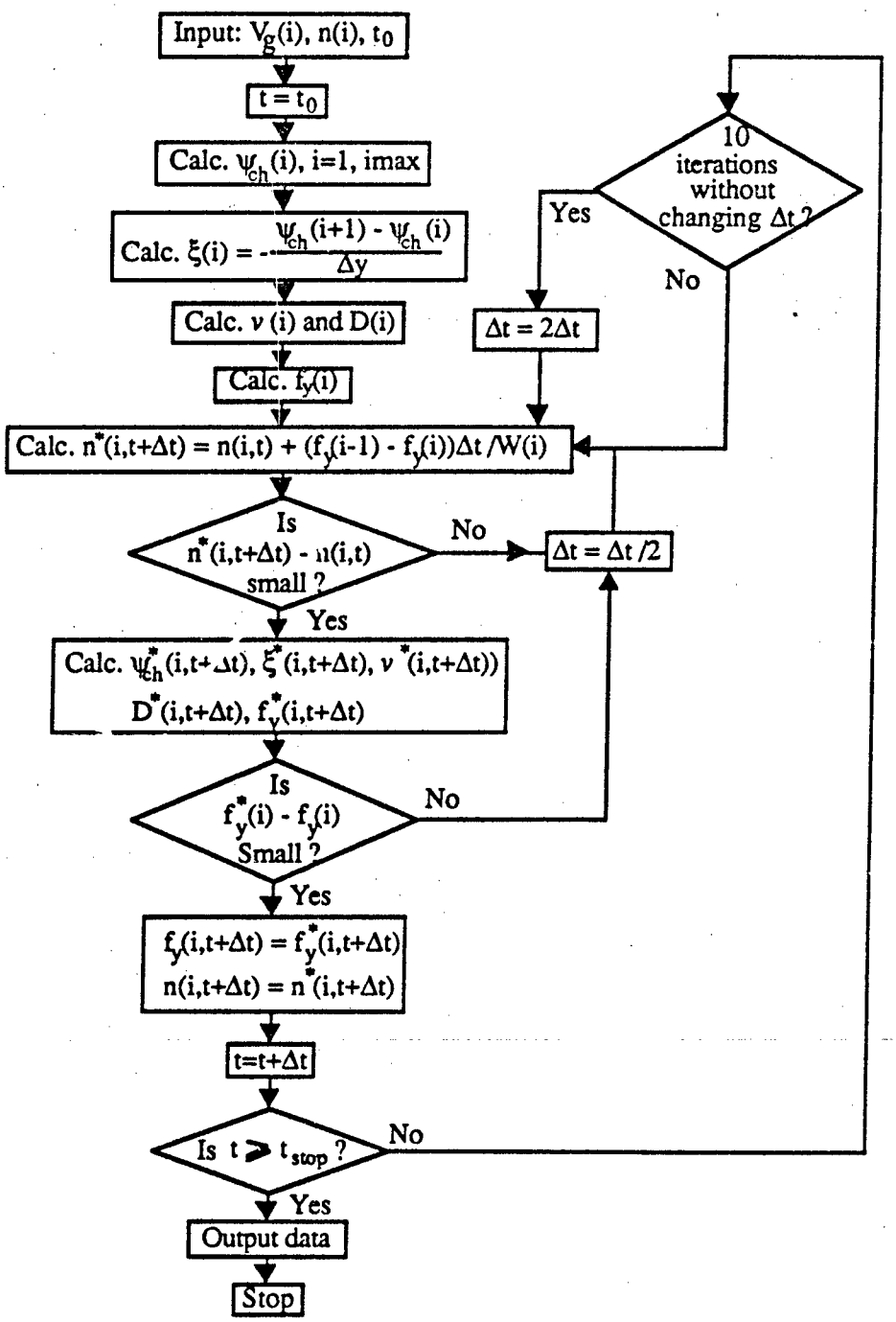


Figure 3.3 Flow chart of the TOF simulation program.

3.1.4 Calculation of Electron Flux Along the Channel

The flux at node i in the channel direction is $f_y(i)$, which consists of a diffusion term and a drift term.

$$f_y(i) = f_y^{diff}(i) + f_y^{drift}(i) \tag{3.7}$$

where

$$f_y^{diff}(i) = D(i)W(i)\frac{n_1(i) - n_1(i+1)}{\Delta y^2} \tag{3.8}$$

and

$$f_y^{drift}(i) = \frac{n_1(i)}{\Delta y} W(i)v(i) \tag{3.9a}$$

for $v > 0$, or

$$f_y^{drift}(i) = \frac{n_1(i+1)}{\Delta y} W(i+1)\, v(i) \tag{3.9b}$$

for $v < 0$, where v is the electron velocity along the channel, which is in the opposite direction of the channel electric field ξ.

The diffusion coefficient D(i) and individual electron velocity $v(i)$ are, in general, nonlinear function of both electric field components in and perpendicular to the channel direction. In the TOF program, only the tangential electric field ξ_y dependence is considered. The drift velocity is:

$$v(i) = -\mu_0 \xi_y(i) \tag{3-10a}$$

$$v(i) = -\frac{\mu_0 \xi_y(i)}{1 + \frac{|\xi_y(i)|}{\xi_c}} \tag{3.10b}$$

$$v(i) = -\frac{\mu_0 \xi_y(i)}{\left[1 + \left(\frac{\mu_0 |\xi_y(i)|}{v_{sat}}\right)^2\right]^{1/2}} \tag{3.10c}$$

for the constant mobility case, the velocity-field curve of Si, and the velocity-field curve of GaAs. Here, ξ_c is the saturation field of the velocity, and v_{sat} is a field dependent coefficient expressed in terms of fitting parameters A_v, B_v, C_v, D_v and F_v:

$$v_{sat} = A_v\, e^{-\frac{\mu_0 |\xi_y|}{B_v}} + \frac{C_v}{1 + \left(\frac{\mu_0 |\xi_y|}{D_v}\right)^{F_v}} \tag{3.11}$$

The diffusion coefficient is:

$$D(i) = D_0 + \Delta D\, e^{-\left(\frac{\ln|\xi_y(i)| - a}{b}\right)^2} \tag{3.12}$$

The electric field in the channel is

$$\xi_y(y) = -\frac{\partial \psi(y)}{\partial y} = -\frac{\psi(i+1) - \psi(i)}{\Delta y} \tag{3.13}$$

where $\psi(y)$ consists of the channel potential ψ_{ch} and a non-local potential correction $\Delta\psi_{ch}$ due to the influence of line charge at neighboring locations in the channel. For the MOSFET structure, ψ_{ch} is the surface potential, while it is the potential of the buried channel for the MESFET structure.

3.1.5 Electrostatics

When the gradual channel approximation (GCA) is employed, one can find the electrostatic potential by either solving the 1D Poisson's equation as done in [19] or working with Green's function [20]. With GCA removed, the Green's function also gives the non-local potential correction. In Appendix A - D, the later method is used to derive the channel potential as well as the non-local potential correction for the RG-MOSFET and RG-MESFET.

3.1.5.1 RG-MOSFET

The RG-MOSFET is a surface channel device. The channel potential and its non-local correction can be found by Green's function (Appendix B, equations (B-6) and (B-9)):

$$\psi_{ch}(y) = V_G'(y) - \frac{qn_s(y)}{C_{ox}} + V_0 - \sqrt{V_0^2 + 2V_0\left(V_G'(y) - \frac{qn_s(y)}{C_{ox}}\right)} \tag{3.14}$$

$$\Delta\psi_{ch} = \frac{q}{2\pi(\varepsilon_s+\varepsilon_{ox})}\int_{-\infty}^{\infty}\left(\ln(y-y')^2 - \frac{2\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\sum_{m=1}^{\infty}\left(\frac{\varepsilon_s-\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\right)^{m-1}\ln[(y-y')^2+4m^2t_{ox}^2]\right)$$

$$(n_s(y') - n_s(y))\, dy' \tag{3.15}$$

Here

$$V_G'(y) = V_G(y) - V_{FB} \tag{3.16a}$$

$$V_G(y) = V_{G1} + V_{GG}\frac{y}{L} \tag{3.16b}$$

$$v_0' = \frac{qN_A\varepsilon_s}{C_{ox}^2} \tag{3.16c}$$

$\Delta\psi_{ch}$ is due to the non-uniform distribution of surface charge in a real MOSFET device. After discretization: y'=jΔy, y=iΔy, $n_l=n_s\Delta y$, and summing k line charges on both sides of the point of interest,

$$\Delta\psi_{ch}(i) = \frac{q}{2\pi(\varepsilon_s+\varepsilon_{ox})}\sum_{j=i-k}^{j=i+k}\left(n_l(j) - n_l(i)\right)\left(\ln((j-i)\Delta y)^2 - \frac{2\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\sum_{m=1}^{M}\left(\frac{\varepsilon_s-\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\right)^{m-1}\ln((j-i)\Delta y)^2+(2mt_{ox})^2\right) \tag{3.17}$$

In the simulation, k and M are picked such that any further increase in k or M does not increase $\Delta\psi_{ch}(i)$ substantially. In the simulation, k is around 7 and M is around 6.

3.1.5.2 RG-MESFET

The RG-MESFET is a buried channel device. The channel potential and its non-local correction can also be found by Green's function (Appendix C, equation (C-10) and (C-11)) assuming the substrate doping N_A=0:

$$\psi_{ch}(y) = V_G'(y) + \frac{qN_D}{2\varepsilon_s}\left(T_{epi} - \frac{n_s(y)}{N_D}\right) \tag{3.18}$$

$$\Delta\psi_{ch}(x,y) = qN_D\int_{-\infty}^{\infty}dy'\int_{x_d(y)}^{x_d(y')}G(x,y,x',y')\,dx' \tag{3-19}$$

where

$$\int_{x_d(y)}^{x_d(y')}G(x,y,x',y')\,dx' = \frac{-1}{4\pi\varepsilon_s}\left[(x-x_d(y))\ln((y-y')^2+(x-x_d(y))^2\right.$$
$$-(x-x_d(y'))\ln((y-y')^2+(x-x_d(y'))^2)$$
$$-(x+x_d(y'))\ln((y-y')^2+(x+x_d(y'))^2)$$
$$\left.+(x+x_d(y))\ln((y-y')^2+(x+x_d(y))^2\right)$$

$$+ 2\,|y-y'|\left(\tan^{-1}\frac{x-x_d(y)}{|y-y'|} - \tan^{-1}\frac{x-x_d(y')}{|y-y'|} - \tan^{-1}\frac{x+x_d(y')}{|y-y'|} + \tan^{-1}\frac{x+x_d(y)}{|y-y'|}\right)\Big] \tag{3.20}$$

T_{epi} is the ion implantation depth of the n-channel, N_D the channel doping density, and n_s the electron density per unit area. If a non-uniform charge distribution (caused only by the variation of the depletion region width, since we assume the channel is neutral) is considered, however, the resulting channel potential varies with the depth of the channel, which contradicts the original assumption that channel potential is only a function of y. Fig. 3.4 plots the channel potential correction calculated using Eqn (3.19) and (3.20) for two different channel depths: the depletion edge x_d and the centroid of the channel x_m. ($L=10\mu m$, $V_{GG}=8V$. The electron density in the channel has an average value of 3.86×10^{11} cm^{-2}, oscillation amplitude of 1.765×10^{11} cm^{-2}, and spatial period of $1.44\mu m$. The uncorrected potential varies from 0.8V to 8.8V). Fortunately, the difference is small.

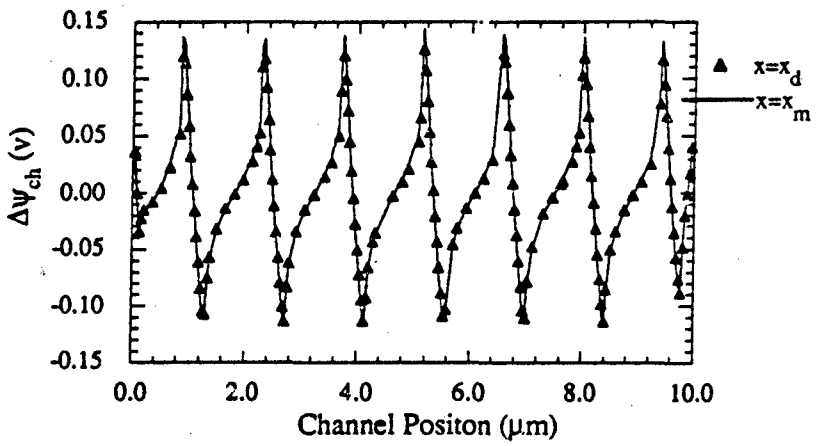


Figure 3.4 Channel potential correction $\Delta\psi_{ch}$ for MES structure calculated using Eqn (3.19) and (3.20) for two different channel depths: $x=x_d$ (edge of the surface depletion) and $x=x_m$ (centroid of the channel).

For further simplification, assume that the channel charge is a δ-function at the centroid

$$x_m = T_{epi} - \frac{n_s}{2N_D} \tag{3.21}$$

The corresponding charge distribution is shown in Fig. 3.5(a). The non-local potential correction can be calculated with the aid of Fig. 3.5(b):

$$\Delta\psi_{ch}(i) = \frac{1}{4\pi\varepsilon_s}\sum_{j=i-k}^{j=i+k}\left(n_1(j) - n_1(i)\right)\ln\left(\frac{D1}{D2}\right)$$

$$= \frac{1}{4\pi\varepsilon_s}\sum_{j=i-k}^{j=i+k}\left(n_1(j) - n_1(i)\right)\ln\left(\frac{(j-i)\Delta y)^2 + \left(\frac{n_1(j)-n_1(i)}{2\Delta y N_D}\right)^2}{(j-i)\Delta y)^2 + \left(2T_{epi} - \frac{n_1(j)+n_1(i)}{2\Delta y N_D}\right)^2}\right) \tag{3.22}$$

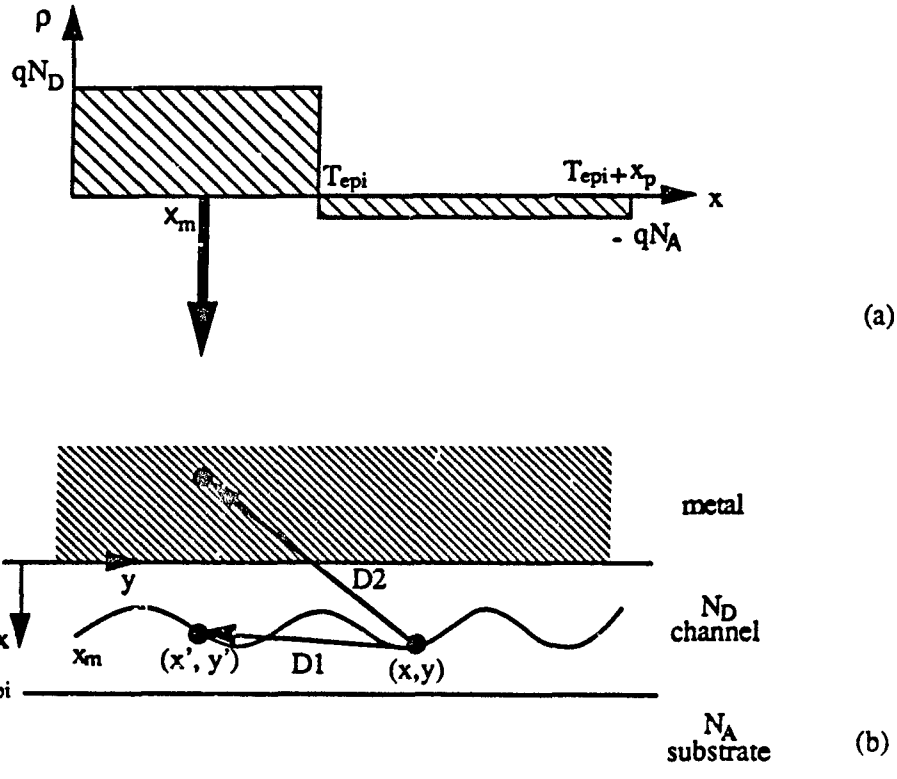


Figure 3.5 (a) Charge distribution in a MESFET assuming the channel charge is a δ-function at the centroid. (b) Calculation of non-local potential correction.

Fig. 3.6 shows the non-local potential correction for the channel centroid, calculated from Eqn(3.22). Comparing Fig 3.4 and Fig. 3.6, one can see that the two methods give approximately the same results. Mathematically, the non-local potential correction using the δ - charge distribution at the centroid is simpler.

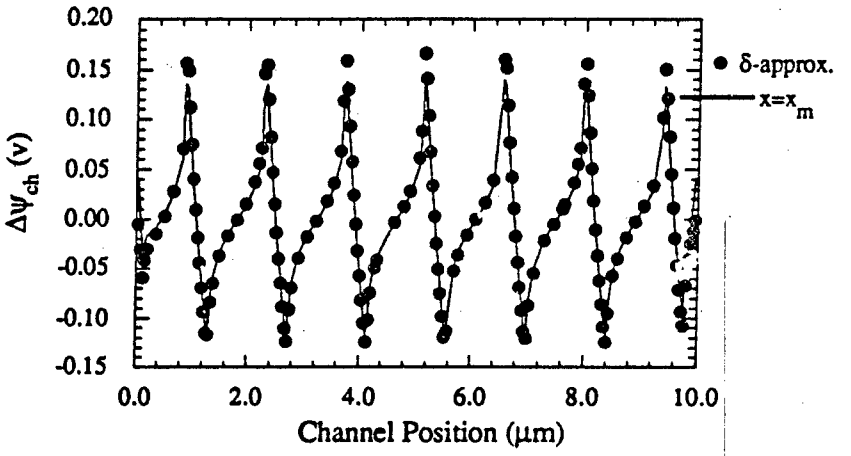


Figure 3.6 Channel potential correction $\Delta\psi_{ch}$ for the MES structure calculated at $x=x_m$ (centroid of the channel), using Green's function approach (3.19) & (3.20), and δ-sheet charge approximation (3.22).

3.2 Simulation Results for MOSFET CDO

The MOSFET CDO simulation has been performed for a range of conditions [21]. Type (1) boundary condition is used, i.e., the electron densities at both source and drain are fixed. The nonlinear velocity field curve expressed in (3.10c) is used with the following parameters: μ_0=5200 cm^2/V-s, $A_v=9.55\times10^7$, $B_v=1.316\times10^7$, $C_v=5.8\times10^7$, $Dv=6.788\times10^5$, F_v=0.316. The constant diffusivity determined by the Einstein ralationship is used.

Fig. 3.7 shows the frequency and normalized peak-to-peak electron density as a function of $(n_s d)^{-1}$. n_s is the average number of electrons per unit gate area in the channel. For the MOSFET structure, the conduction channel is at a constant distance $d=t_{ox}$ from the resistive gate. This relationship implies that if n_s is halved and the d is doubled, the frequency will not change.

It is expected that the lower frequency limit is determined by the maximum charge capacity of the potential well in the devices. For an ideal MOSFET, the inversion electron density can be very high. However, to implement a MOSFET structure in reality using GaAs semiconductor, an AlGaAs/GaAs heterojuction has to be used. The energy barrier provided by band discontinuities is much smaller than that of a ideal insulator. The leakage current across the device (along the x direction) due to thermionic emission, which is inversely proportional to the exponential of the barrier height, will be much greater. As a result, a high inversion electron concentration in the channel is more difficult to obtain.

As indicated in reference [22], the maximum 2DEG density is determined by the doping density of AlGaAs and GaAs and by the conduction band discontinuity at the AlGaAs/GaAs interface. It is limited in the neighborhood of 10^{12} cm^{-2} for AlGaAs doping ranging from $5x10^{17}$ to $10^{19}cm^{-3}$. The thickness of the AlGaAs is chosen so that the surface depletion region overlaps the interface depletion region to allow the gate modulation of the channel so that there are no free carriers in the barrier layer and the channel is modulated by the gate.

The minimum frequency is then determined by the maximum surface electron density in the channel (~$10^{12}cm^{-2}$) and the thickness of AlGaAs (~800Å), which gives 1/(nd)~12.5Å, corresponding to a frequency of about 50GHz.

The maximum frequency can be obtained by examining the rate of change of the charge packet width [23]:

$$\dot{w}_p = 2\frac{\partial n_s}{\partial y}\left(\frac{\bar{\mu}}{C}+\frac{D}{n_s}\right) \tag{3.23}$$

where D is the diffusion constant, $\bar{\mu}$ tne effective differential mobility, and C the capacitance. y is along the channel direction. The first term in (3.23) represents the charge packet expansion due to the electron drifting under the influence of the self-induced electric field. The second term represents the charge packet expansion due to the electron diffusion, which is always positive. When the differential mobility is negative ($\bar{\mu}<0$), w_p could be negative, indicating the charge packet contraction instead of expansion. i.e.,

$$\frac{1}{n_s d} < \frac{q\,|\bar{\mu}|}{\varepsilon_s D} \tag{3.23}$$

For typical values of D=135 cm^2/s ($D=k_BT/q\ \mu_0$, μ_0=5200 cm^2/V-s), $\bar{\mu}$ ~ -850 cm^2/V-s at a field of approximately 1V/μm, $1/(n_sd)_{max}$ ~ 88 Å. From Fig 3.7, however, the oscillation amplitude decreases dramatically as the oscillation frequency increases. Therefore, the practical maximum frequency limit is determined by the oscillation amplitude.

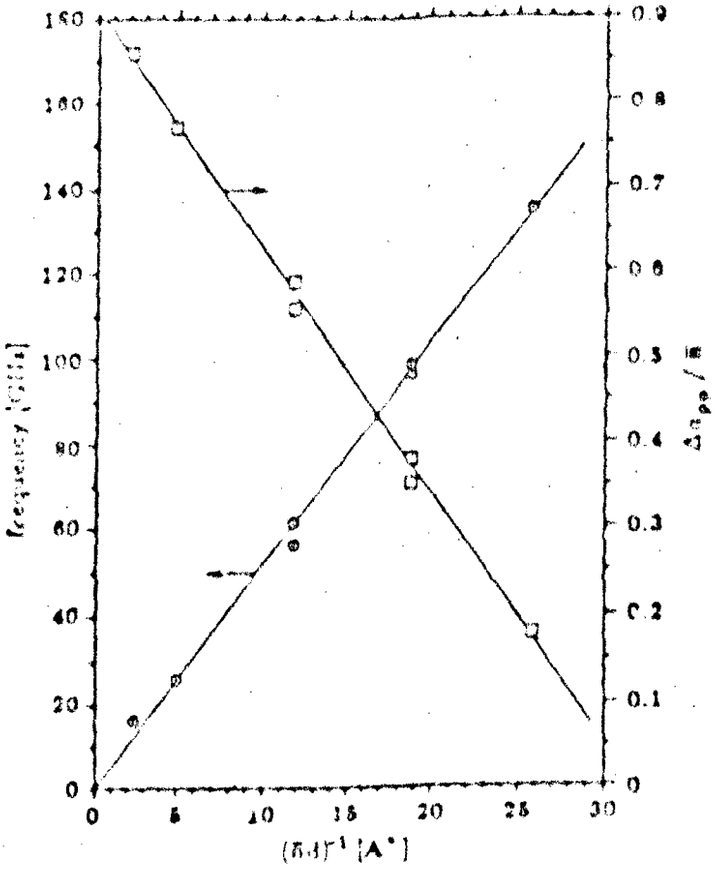


Figure 3.7 Computer simulation results for the MOSFET CDO. Frequency and normalized peak to peak amplitude as a function of the parameter $(\bar{x}d)^{-1}$ for several different operations. Note that the actual amplitude goes as $1/(\bar{x}d)$ at a given fixed frequency [21]

3.3 Simulation Results for the MOSFET CDO

The main results from the MOSFET transient program are shown in Fig. 3.8 for a channel length of $L_{ch} = 1500$ Å. Various doping densities are investigated. The saturation velocity and the velocity field curve are the same as used in the BG MOSFET simulations. Although there exists scatter in the data, the operation frequency is approximately a linear

function of $(n_s d)^{-1}$ up to 26Å and then saturates thereafter. Here $d=x_d$ is the separation distance measured from the edge of the depletion region to the resistive gate/GaAs interface.

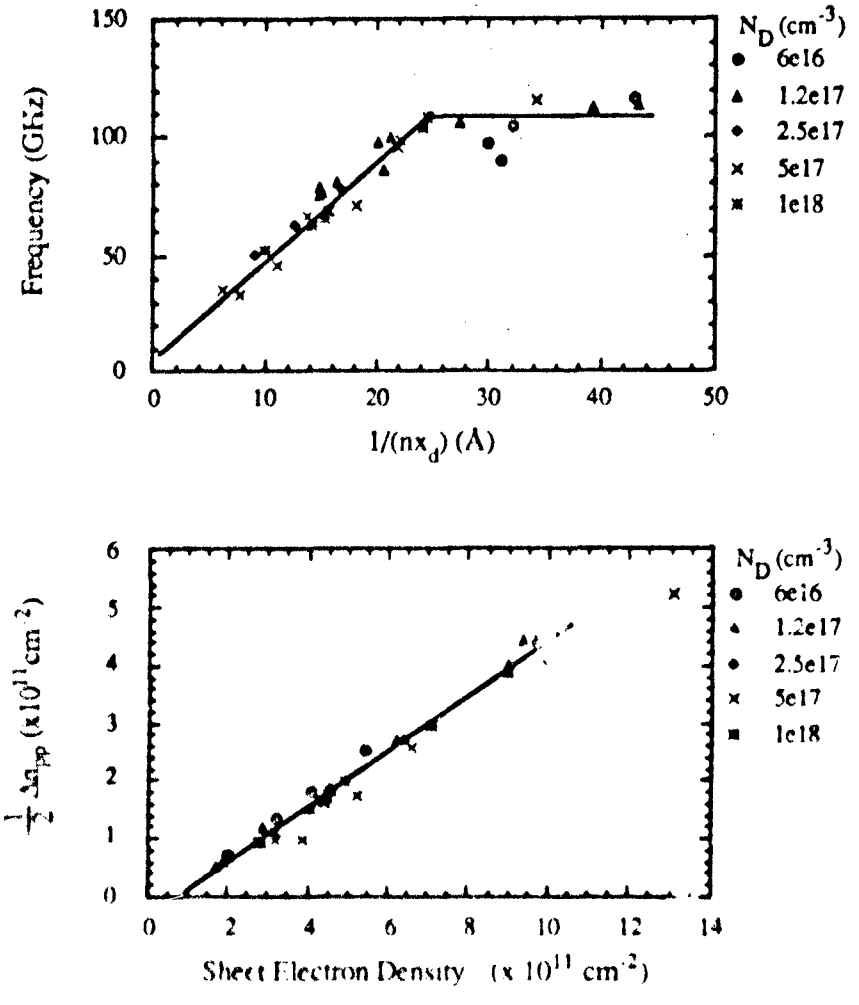


Figure 3.8 Computer simulation results for the MESFET CDO [24].
(a) Frequency as function of the parameter $(nd)^{-1}$ (Å).
(b) Oscillation amplitude as function of n_s (cm^{-2})

Assuming that the charge goes into the channel as a rectangle with height equal to the channel doping, the depletion width moves towards the gate-GaAs interface as the channel gets fuller and away from the interface as n gets smaller. Therefore, x_d oscillates as electron density oscillation occurs, and d is no longer a constant as that in MOSFET device. The computer program utilized the assumption that even though the electrons can redistribute inside channel (along the x direction), the flux or current is still one dimensional (along the y direction).

It seems that the relation is independent of the doping density and it is obvious that the frequency can be modulated in a wide range by varying the average sheet electron density n_s, which is controlled by the source to gate voltage V_{SG}. A high frequency of about 110 GHz is achievable for the MESFET CDO.

The oscillation amplitude $1/2\Delta n_{pp}$ is approximately a linear function of sheet electron density n_s. As the frequency increases, the a.c. output power decreases.

The minimum frequency f_{min} is determined by the maximum n_sd product. Since

$$n_s d = n_s \left(T_{epi} - \frac{n_s}{N_D}\right) \tag{3.24}$$

the maximum value of n_sd (obtained by differentiating (3.24) with respect to n_s) occurs when the channel is "half full" (neglect the zero bias depletion width x_{d0}):

$$n_s = \frac{1}{2} N_D T_{epi} \tag{3.25}$$

Therefore

$$(n_s d)_{max} = \frac{N_D T_{epi}^2}{4} \tag{3.26}$$

and the minimum frequency is:

$$f_{min} = \frac{4}{N_D T_{epi}} A \tag{3.27}$$

where A is the slope of the f vs. $(n_sd)^{-1}$ plot for $1/(nx_d) < 25\text{Å}$. Therefore, f_{min} is determined by the fabrication parameters, N_D and T_{epi}.

The maximum frequency is limited to 110GHz. The reason is not yet known.

3.4 Summary

The one dimensional Time-Of-Flight program is used to simulate the resistive gate FET devices. By combining the transferred electron effect (nonlinear velocity - field curve) in GaAs with the two dimensional geometry of a FET device, a series of contiguous electron packets can be generated in a resistive gate FET. High frequency oscillation in the GHz range can be obtained. The frequency and the oscillation amplitude depend on the channel electron density and the distance between the gate and the channel. The electron density can be changed by changing the source-to-gate1 voltage.

CHAPTER 4
EXPERIMENTS ON THE RESISTIVE GATE MESFET OSCILLATOR

The resistive-gate MESFET structure was first fabricated in order to verify the contiguous domain oscillation concept since it is the most widely used technology for GaAs integrated circuits in industry. The devices were fabricated at ITT (International Telephone and Telegraph) Gallium Arsenide Technology Center based on the design and process developed here at Purdue. Three wafers with exactly the same structure but different channel doping and channel depth were fabricated (CDO-1-3: channel doping = 2.4×10^{17} cm^{-3}, depth = 2000Å; CDO-1-4: channel doping = $6\times10^{16}cm^{-3}$, depth = 1500Å; CDO-1-5: channel doping = 1.2×10^{17} cm^{-3}, depth = 1500Å. Source / drain, doping = 5×10^{17} cm^{-3}, depth = 2000Å for all the samples). Only wafer CDO-1-5, which exhibits microwave oscillation, is considered here. The other two wafers did not oscillate. The information on the other two wafers of device can be found in Ref. [19].

This chapter summarizes the experiments on the Resistive-Gate MESFET devices. The fabrication sequence of the RG-MESFET (CDO-1-5) is covered, followed by dc and the microwave testing results and discussion. Further modification of the ITT devices is also presented.

4.1 Fabrication Procedure of the RG-MESFET CDO

The device structure of a fabricated resistive-gate MESFET oscillator is shown in Fig. 4.1. The basic device dimensions are the channel depth T_{epi}, gate length L_G, gate width W_G, channel length L, channel width W, and the overlap of the resistive gate over the source or drain region X. The origin of X is at the source (drain) - channel junction. When the ohmic contact is on top of the source (drain) region, X is positive. If the ohmic contact is on top of the channel, X is negative.

The complete fabrication of the RG-MESFET device requires eight mask levels, summarized in Table 4.1. The process starts with a two-inch semi-insulating GaAs wafer

with (100) orientation. A 350Å PECVD SiOH layer is first deposited to minimize the channeling effect during the ion implantation. The first lithographic step is the registration mask (REG mask), which defines alignment marks for the subsequent masks. Since the first two steps of the fabrication are ion implantation for the channel and the source/drain, which leave no visible marks on the GaAs wafer, it is necessary to have this registration mask to etch the GaAs before the ion implantation. CF_4 Plasma (200mTorr, 150W, 6mins) was used to etch the SiOH cap and expose the GaAs that was to be subsequently wet etched to form the registration marks.

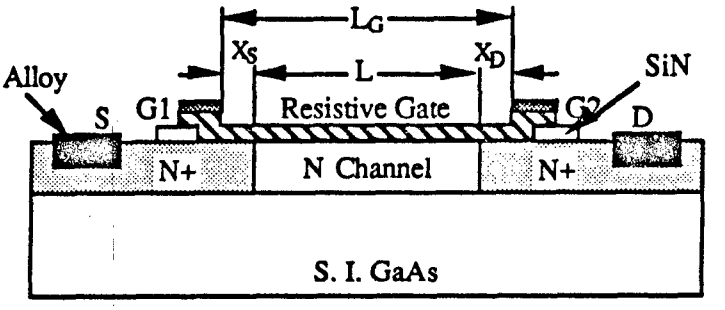


Figure 4.1 Schematic cross section of the RG-MESFET Device.

Table 4.1 RG-MESFET device process summary.

Operation	Mask level (field)
1. 350 Å PECVD SiON ion implant cap deposition	
2. Registration mark etch	REG (dark)
3. Selective channel implant	LFI (dark)
4. Selective source / drain implant	NPI (dark)
5. Anneal cap deposition, anneal, cap removal	
6. 1000 Å PECVD SiN deposition, patterning and etch	SIN (clear)
7. Au/Ge/Ni ohmic contact evaporation, liftoff and alloy	OHM (clear)
8. Resistive gate sputter deposition and liftoff	GAT (clear)
9. Ti/Pd/Au interconnect evaporation and liftoff	MT1 (clear)
10. 2050Å PECVD SiN deposition, patterning and etch	NVA (dark)

The channel was patterned by the second mask (LFI mask) for channel ion implantation. Doubly ionized silicon Si^{++} was first implanted into the GaAs with acceleration energy of 155keV and dose of $3.11x10^{12}cm^{-2}$. The second implantation with a lower acceleration energy (65keV) and lower dose ($5.2x10^{11}cm^{-2}$) was then done to retain the carrier concentration toward the surface. The third mask (NPI mask) defines the source/drain implantation. Si^{++} was implanted into the GaAs with an energy of 200keV and dose of $2x10^{13}cm^{-2}$. Activation is subsequently done in order for Si at interstitial sites to move to substitutional sites and for the wafer to recover from the implantation damage. To achieve a uniform and controllable activation, another cap layer of 2000Å SiOH is deposited before the process and removed with 5% HF for 15 mins after the process. The top view of mask levels 2 and 3 is shown in Fig. 4.2, along with the cross section of the device with the channel and source/drain ion implantation step completed.

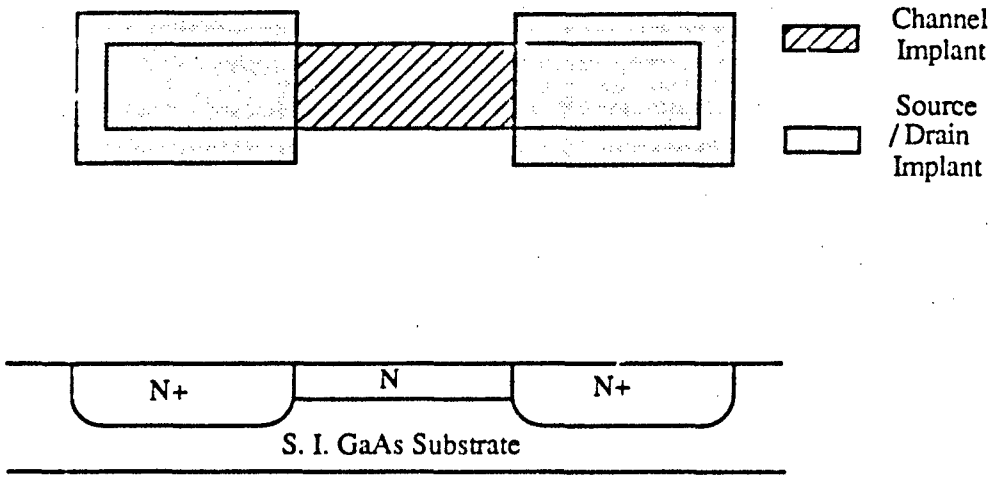


Figure 4.2 (a) Top view of mask 1 (LFI) and mask 2 (NPI). (b) Cross section of the device with channel and source/drain ion implantation completed.

The fourth mask (SIN mask) defines a ring of silicon nitride film around the channel. It reduces the field enhancement at the gate edge to prevent the reduction of the planar breakdown voltage of the gate-channel Schottky diode [19]. The silicon nitride is LPCVD deposited to a thickness of 1100Å. The unwanted part of the silicon nitride is etched away using CF_4 plasma (400mTorr, 6mins). The device with silicon nitride ring formation completed is shown in Fig. 4.3.

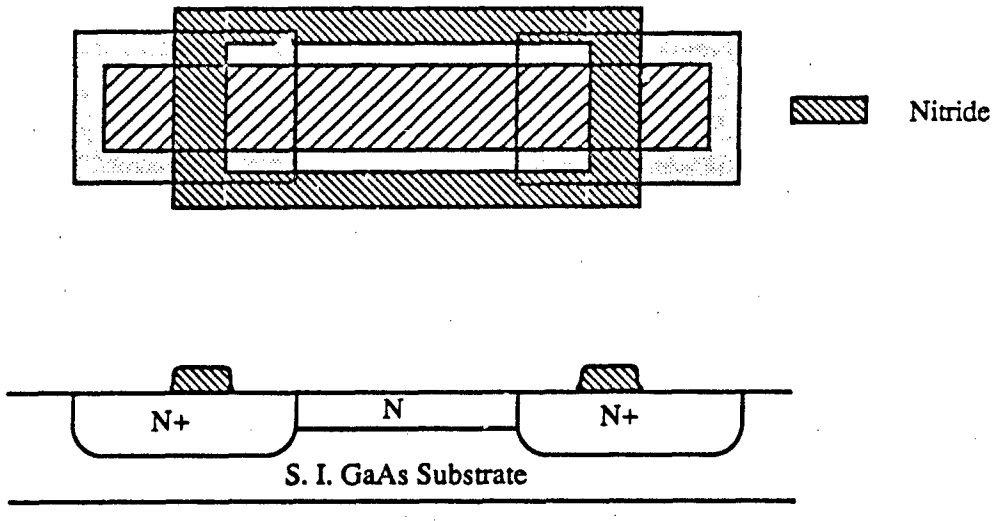


Figure 4.3 (a) Top view of related mask levels. (b) Cross section of the device with silicon nitride ring formation completed

Mask 5 (OHM mask) defines the ohmic contact in the source and drain. The ohmic contact is formed by a Ni/Ge/Au (150/300/2000Å) evaporation and heat pulsed at 390^0C for 20 sec. The device with ohmic contact formation completed is shown in Fig. 4.4.

Mask 6 (GAT mask) defines the resistive gate pattern. The gate, made of WSiN resistive film, is deposited by rf reactive sputtering from pure W and Si targets in an argon and nitrogen (65% partial pressure) atmosphere (power = 1.5kW, pressure = 10 mTorr, time = 65 mins). The resulting film has a sheet resistivity of 30kΩ/square and a thickness of 1100Å. The Schottky contacts were found to have ideality factor of 1.65 and a barrier height of 0.6V. A Lift-off process was used to pattern the resistive gate. The device with resistive gate lift-off step completed is shown in Fig. 4.5.

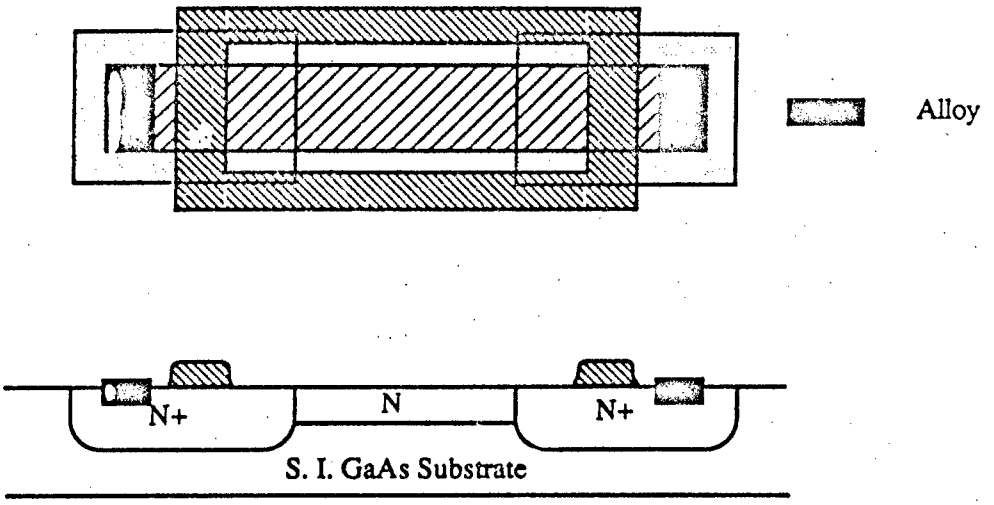


Figure 4.4 (a) Top view of related mask levels. (b) Cross section of the device with ohmic contact formation completed.

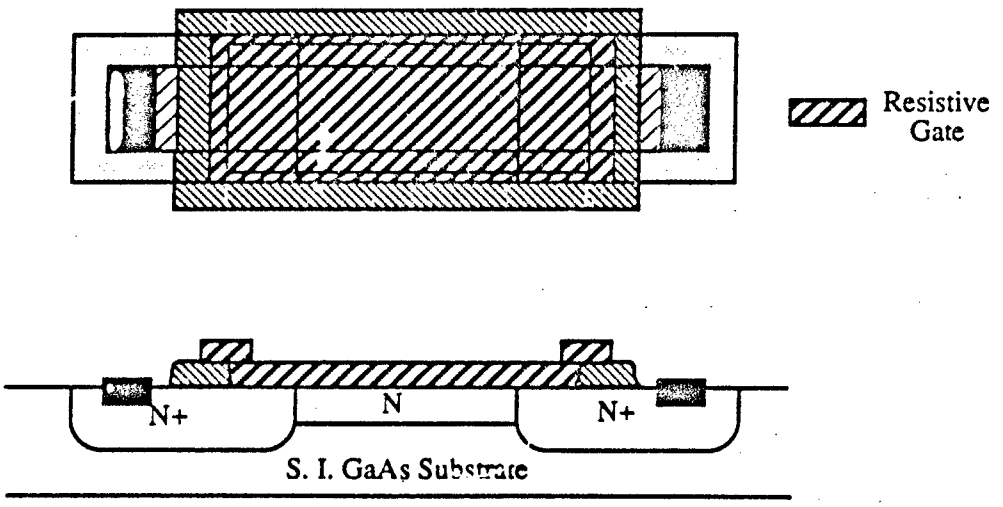


Figure 4.5 (a) Top view of related mask levels. (b) Cross section of the device with resistive gate lift-off step completed.

Mask 7 (MT1 mask) defines the metal connection to the devices. Ti/Pd/Au (500/500/5000Å) is evaporated and patterned by lift-off. The device with Ti/Pd/Au step completed is shown in Fig. 4.6.

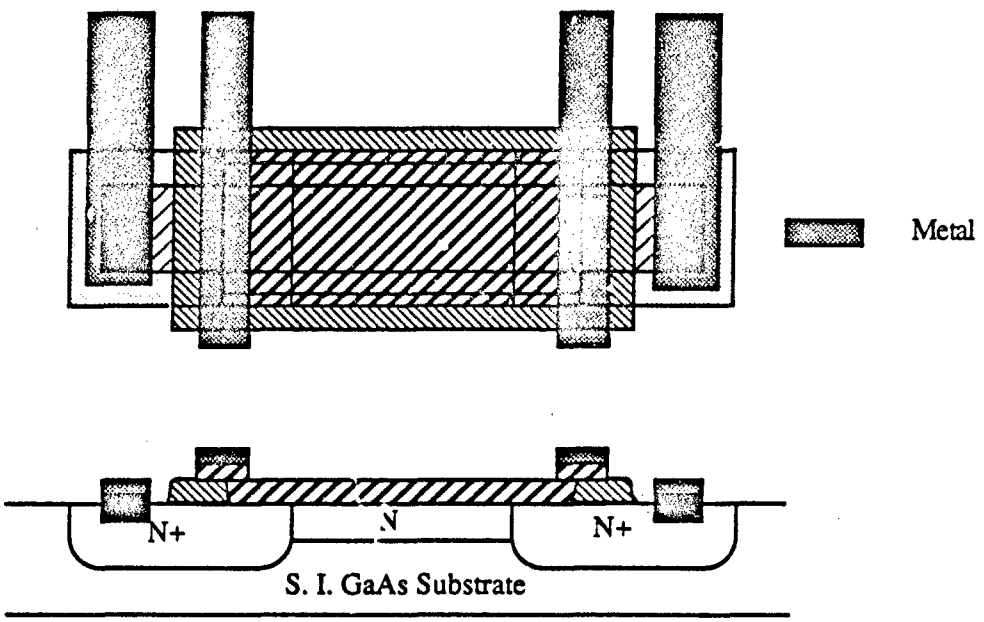


Figure 4.6 (a) Top view of related mask. (b) Cross section of the device with Au/Ge/Ni metalization step completed.

The last layer deposited on the wafer is a cap layer of LPCVD SiN to protect the devices from scratch and contamination. Windows are pattern with CF_4 (400mTorr, 75W, 11mins).

There are eighteen devices on each die with different channel length and width, where L=10, 20, 50 μm and W=10, 20, 50, 200, and 400 μm. The offset X=5 μm on both source and the drain sides. The layout is shown in Fig. 4.7.

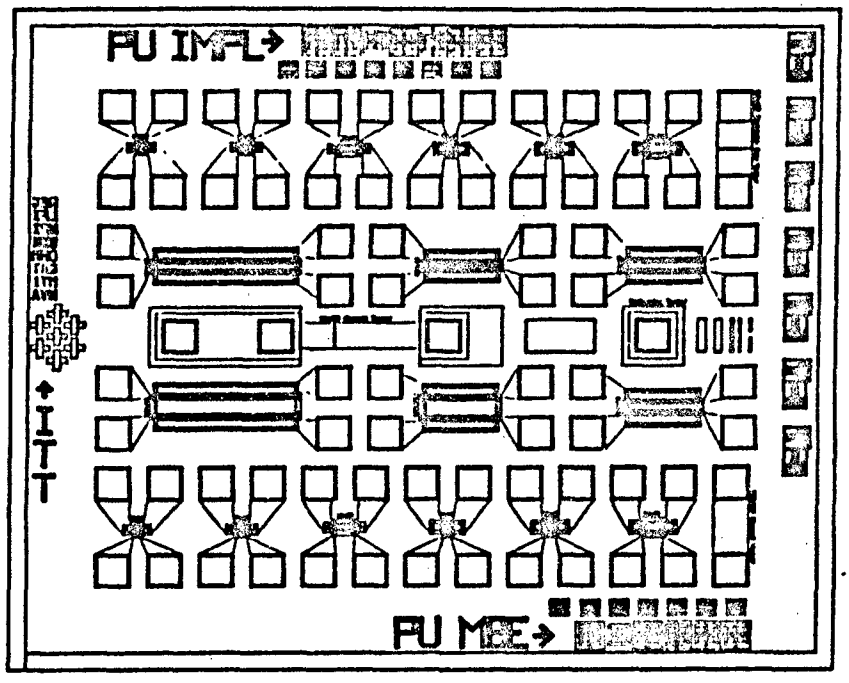


Figure 4.7 The layout of RG-MESFET devices. The channel length and width LxW from left to right for the devices on the top row are: 10x10, 20x10, 50x10, 10x20, 20x20, 50x50. LxW for the devices on the second row are: 20x400, 10x200, 20x200. LxW for the device on the third row are: 50x400, 50x200, 20x200. The device on the forth row are the same as that on the first row. Besides eighteen RG-MESFET devices, there are resistance test patterns for gate, channel and source/drain.

4.2 IV Measurement of the RG-MESFET Devices

The DC electrical testing was conducted for the oscillator devices before any microwave testing. A Hewlet-Packard 4145B semiconductor parameter analyzer is used to measure the gate-to-source and gate-to-drain Schottky diode characteristics and the IV characteristics of the RG-MESFET's. The drain breakdown voltage is found to be around 4.5V. Typical drain current I_D and gate2 current I_{G2} vs. V_{GG} with V_{SG} as parameter are shown in Figure 4.8. Two features can be noticed on these curves: (1) At small V_{GG}, application of V_{SG} delays the turn on of the drain current. (2) A strong negative transconductance (i.e., drain current decreases as gate field increases) is observed at higher V_{GG}. This behavior can be

understood with the help of the DC equivalent circuit [25] as shown in Fig. 4.9 and the schematic potential diagrams for various bias conditions in Fig. 4.10. In the equivalent circuit, R_x denotes the gate resistance between terminal G1 and point x, directly over the edge of the source N+ implant region.

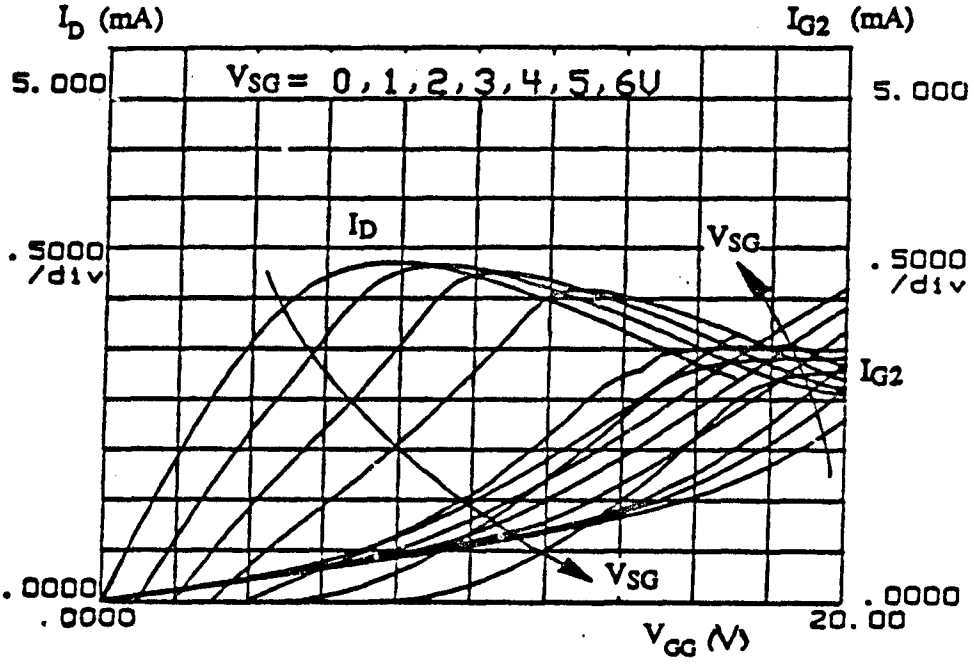


Figure 4.8 The drain current I_D and gate2 current I_{G2} vs. V_{GG} with V_{SG} as parameter. V_{DG} is held at 0 and has little effect on the drain current I_D. V_{SG} increases from 0 to 6V with steps of 1V.

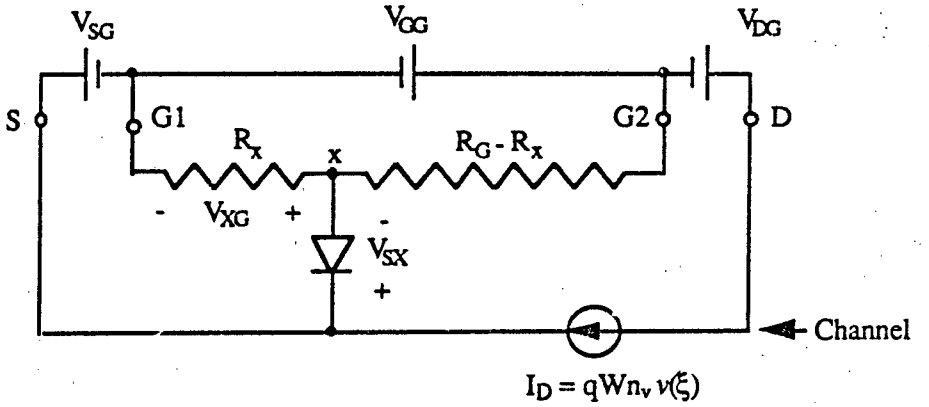


Figure 4.9 DC equivalent circuit for the RG-MESFET. R_X represents the gate resistance between terminal G1 and the edge of the source [25].

Refering to Fig. 4.10(a)-(c), where non zero V_{SG} is fixed at a value less than the channel pinch-off voltage $V_P(ch)$, the drain current I_D is initially less than zero (Fig 4.10(a)), since $V_{DG} = 0$. Here

$$V_p(ch) = \frac{qN_D}{2\varepsilon_s} T_{epi}^2 - V_{bi} \tag{4.1}$$

is defined as the channel pinch-off voltage, where

$$V_{bi} = \phi_{Bn} - \frac{k_B T}{q} \ln\left(\frac{N_C}{N_D}\right) \tag{4.2}$$

is the built - in potential of the Schottky diode, ϕ_{Bn} is the barrier height, and N_C is the effective density of states in the conduction band. With the application of V_{GG}, however, the drain current increases. When $V_{SG} = V_{DG} + V_{GG}$, the drain current is zero (Fig. 4.10(b)). The gate voltage required for this turn on of positive drain current is simply:

$$V_{GG}(on) = V_{SG} - V_{DG} \qquad V_{SG} < V_P(ch) \tag{4.3}$$

For any V_{GG} greater than the above $V_{GG}(on)$, the drain current is positive as shown in Fig. 4.10(c).

Now refer to Fig. 4.10(d)-(g), where V_{SG} is greater than $V_P(ch)$. The channel is pinched off at the source and the drain current is negative when $V_{GG} = 0$ (Fig. 4.11(d)). The application of a gate voltage V_{GG} increases the drain voltage as well as the potential at point x due to the resistance R_x. When

$$V_{GG} = \frac{L_G}{L_G - X_S}(V_p(ch) - V_{DG}) \tag{4.4}$$

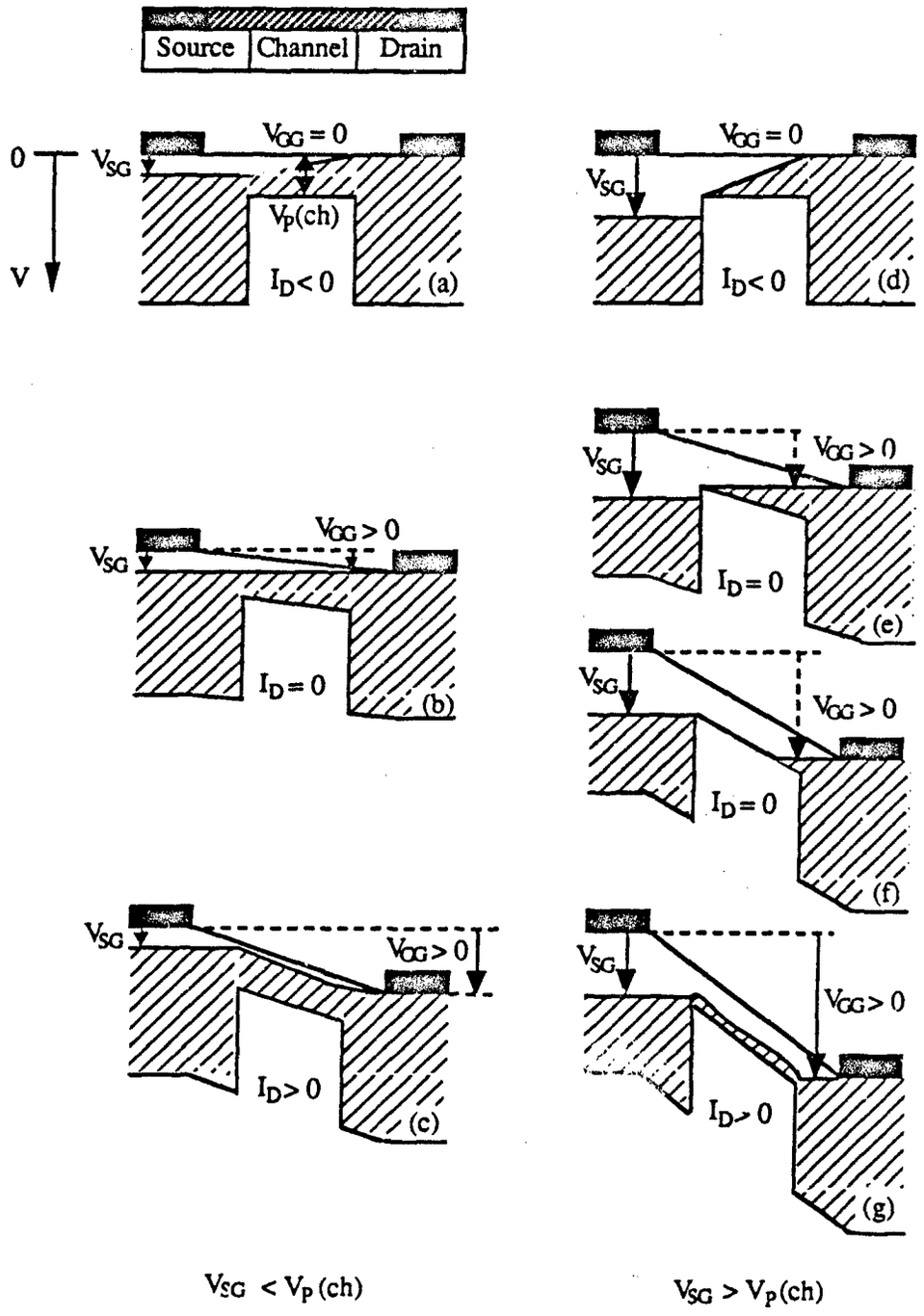


Figure 4.10 Schematic potential diagram for $V_{DG} = 0V$ under different bias conditions.

the drain current becomes zero (Fig. 4.10(c)) and remains zero until the effective reverse bias voltage on the diode V_{XX} becomes

$$V_{XX} = V_{SG} - V_{XG} = V_P(ch) \qquad (4.5)$$

The gate voltage required for this turn on of drain current is (Fig. 4.10(c)),

$$V_{SG}(on) = \frac{I_{XS}}{X_S}(V_{XG} - V_P(ch)) \qquad V_{SG} > V_P(ch) \qquad (4.6)$$

Both equations (4.3) and (4.6) indicate that as V_{SG} is increased, the turn on voltage for V_{GG} is increased.

As V_{GG} is further increased, I_D increases, and eventually V_{XX} become negative, i.e., the Schottky diode at the source end is forward biased. Since channel and the gate can be viewed as a distributed Schottky diode, the distributed currents can flow from the channel to the gate under this circumstances and spillover occurs. The increasing gate current I_{G1} due to spillover results in the decrease in drain current I_D. The negative transconductance of I_D is observed. The high field negative mobility may also contribute to the negative transconductance, but this effect is small since not much negative transconductance is observed once the device is modified to set X_S=0.

In Fig. 4.11, the four terminal currents I_S, I_D, I_{G1}, I_{G2} are shown as functions of the source to gate1 voltage V_{SG} and drain to gate2 voltage V_{DG}. As shown, spillover occurs at the source when $V_{SG} < 4.5V$, which is manifested by a larger I_S than I_D. In this case, the gate to source diode is effectively forward biased. With the increase of V_{SG}, the effective bias voltage across the source/channel diode V_{XS} is reduced and the diode is reverse biased eventually. Further increase of V_{SG} causes I_S and I_D to decrease exponentially. As V_{XS} approaches the breakdown voltage V_{BR}, which is about 6.5V for $N_D = 5\times10^{17}$ cm^{-3} [9], the generation of electron hole pairs through avalanche breakdown occurs.

At the drain end (Fig. 4.11 (b)), I_D below 4.5V is weakly dependent on V_{DG}, showing that the device can be approximated as a current source in this range. For V_{DG} greater than 4.5V, the drain current increases rapidly and the gate2 current decreases, indicating avalanche breakdown of the gate-to drain junction. The lower V_{DG} value where breakdown occurs near the drain (about 4V) than that of V_{SG} where breakdown occurs near the source (about 7V) is caused by the gate overlapping of drain region. Gate overlapping in the drain region effectively biases the gate to drain diode to a higher value than the applied V_{DG}.

From the above discussion, it is shown that the extension of the resistive portion of the gate into the source region has several disadvantages. First, a larger V_{GG} needs to be applied as compared with the same LxW device with X_S=X_D=0 in order to achieve the

same electric field, since the gate is longer. Second, the gate voltage tends to forward bias the gate to source diode due to the voltage drop on R_X. Therefore, a larger V_{SG} is required to ensure the diode is reverse biased. Spillover of electrons from channel to gate can occur when the gate to source Schottky diode is forward biased. Lastly, the effective (internal) V_{SG} is coupled to V_{GG}. The source electron density is determined not only by the external V_{SG} but also by V_{GG}.

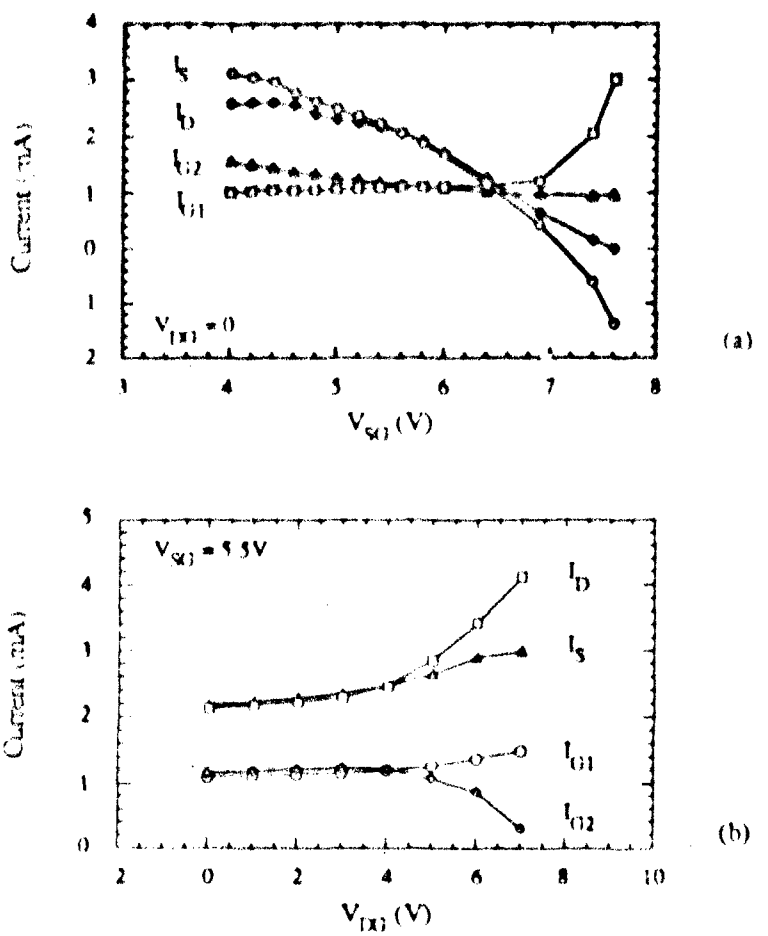


Figure 4.11 Effect of source-to-gate1 voltage V_{SG} and drain-to-gate2 voltage V_{DG} on four terminal currents for a 10x10 (LxW) CDO-1-5 device. A V_{GG}=1.6V is applied, which corresponds to an electric field of 8000V/cm.
(a) I_S, I_{G1}, I_D, I_{G2} vs. V_{SG}.
(b) I_S, I_{G1}, I_D, I_{G2} vs. V_{DG}.

4.3 Microwave Characterization of the RG-MESFET

The schematic bias circuit setup is shown in Fig. 4.12. The sample is mounted on a TO5 can using electric conductive epoxy or silver paint to ensure a good contact. All the connections are made by aluminum wires. The source, gate1, and gate2 leads are brought out the bottom of TO5 can for bias, while the drain lead directly connects to a stripline with characteristic impedance of 50Ω. An SMA connector couples the output current out to a bias tee. The dc output is connected to the DC biasing circuit, and the ac output lead of the bias tee is connected to the spectrum analyzer by coaxial cable for frequency measurement below 21 GHz (internal mixer is used). For frequencies higher than 21GHz, an external waveguide mixer is used via a luncher which connects the signal from the stripline to the waveguide.

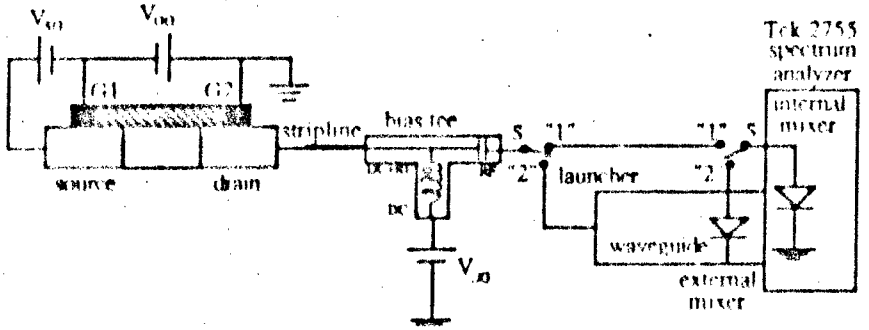


Figure 4.12. Schematic diagram for bias circuit setup.
When switch S is at "1", the signal is directly connected to the internal mixer of the spectrum analyzer. When S is at "2", a luncher and an external waveguide mixer are used between the signal and spectrum analyzer.

To achieve successful operation, proper bias condition is required. First of all, the gate voltage V_{GG} has to bias the channel beyond the threshold for the electron transfer effect. Voltage V_{SG} should be such that it reverse biases the source and gate junction to prevent the spillover of electrons from channel to gate. The higher the reverse bias voltage V_{SG} is across the source-gate1 terminals, the fewer electrons will be injected. The drain and gate 2 junction also needs to be reverse biased in order to isolate the channel and the gate as well as the channel and the drain.

Fig. 4.13 is the power spectrum for a 10x10 device. The fundamental frequency is found to be 12.933 GHz. Oscillation signals are also found at 25.899 GHz and 38.857 GHz, which are the first and second harmonics.

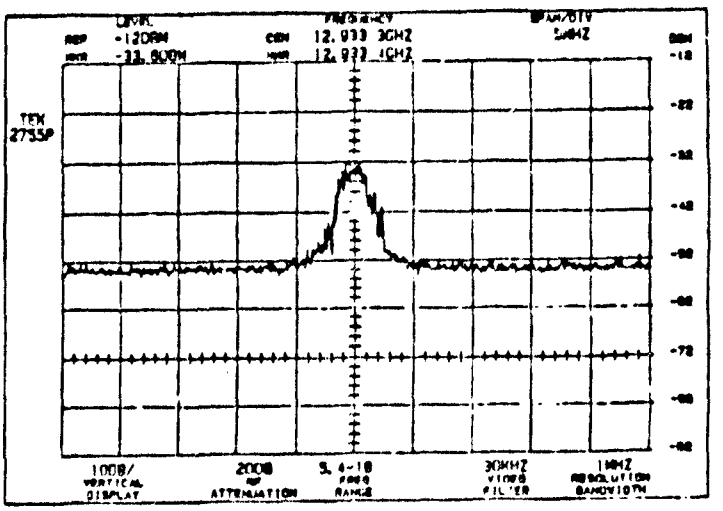


Figure 4.13 Power spectrum for a 10x10 μm RG-MESFET device shown in Fig. 4.1. V_{SG}=5.5V, V_{GG}=16V, V_{DG}=0V. The overlap X_S=X_D=5μm.

The dependence of oscillation frequency and power on bias voltage V_{GG}, V_{SG}, and V_{DG} are shown in Fig. 4.14. It is obvious that both V_{GG} and V_{SG} have strong effects on the device oscillation, while V_{DG} has little effect.

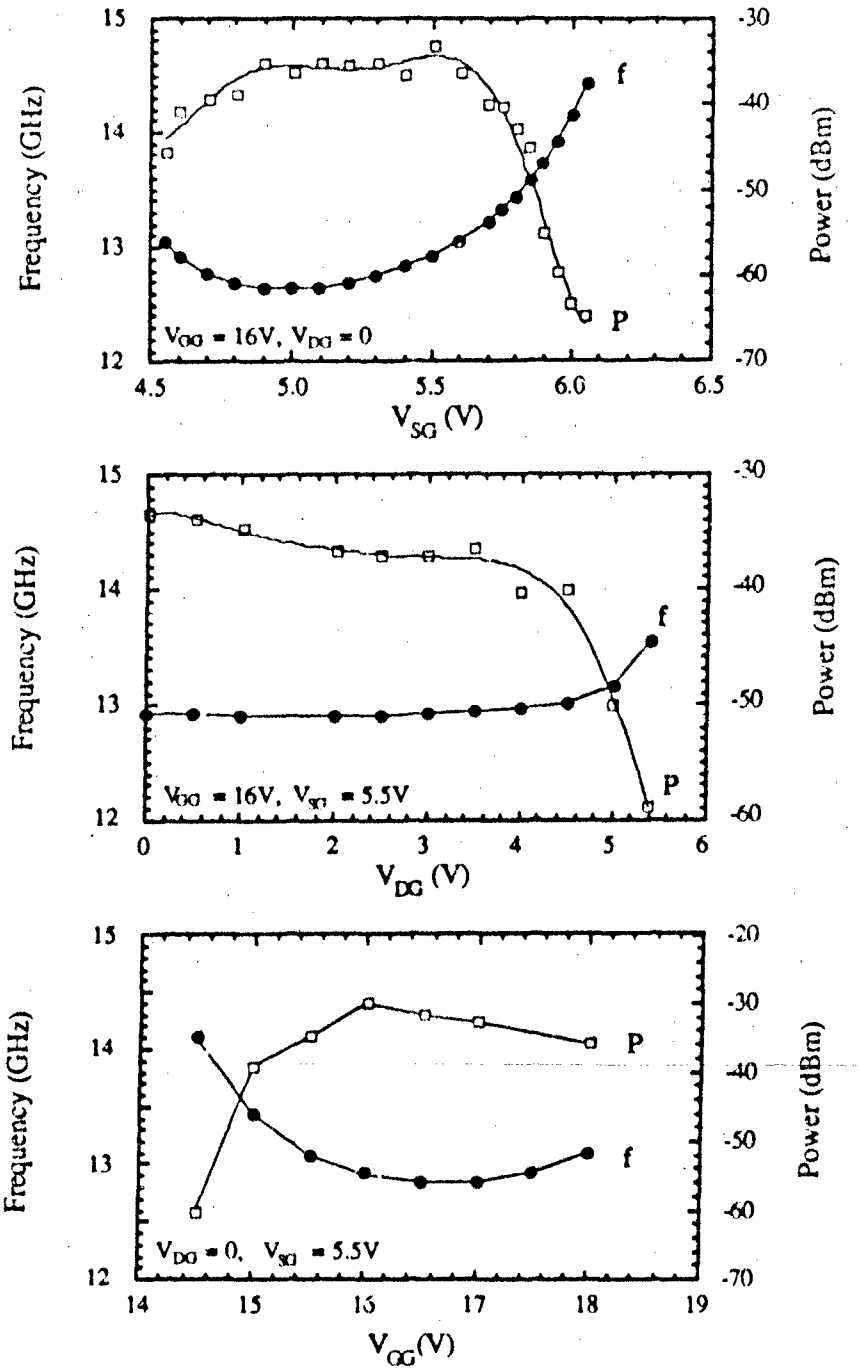


Figure 4.14 Oscillation frequency and power as function of bias voltages.

V_{GG} can affect the operation frequency in two ways. First, any change in V_{GG} will change the electric field along the gate, which changes the drift velocity of electrons in the channel. Second, since the resistive gate overlaps the source, changing V_{GG} causes the internal gate-to-source potential to change in the same direction.

The oscillation frequency varies with V_{SG}, from a minimum of 12.7 GHz at 5V to 14.7 GHz at 6.1V. The frequency tunability is about 2GHz/V.

V_{DG} has very little effect on the oscillation, indicating the device can be viewed as a constant microwave source, consistent with the current measurement results in Fig. 4.11. As shown in Fig. 4.14, the output power of a 10-μm-wide device ranges between 0.1 and 1 μW for frequencies around 13 GHz. This low power is purely due to an exponential decay of the ac current with distance under the large gate2 contact.

The fundamental frequency is in the range of 10-20 GHz, which could be explained by a Gunn diode of 10 μm channel length. In order to identify the oscillation mode, the frequency dependence on the channel length is investigated. The oscillation frequency versus inverse channel length for four devices is shown in Fig. 4.15. The frequency increases linearly with inverse length, having a slope of 1.3×10^7 cm/s. The solid line is calculated from $f = v_d / L$, representing a Gunn diode. The scatter of the data is caused by many factors such as the misalignment of the gate, different injection levels at the source V_{SG} and different applied electric field, V_{GG}/L. The dependence of frequency on the channel length L indicates that the oscillation is due to a single domain rather than multiple domain formation.

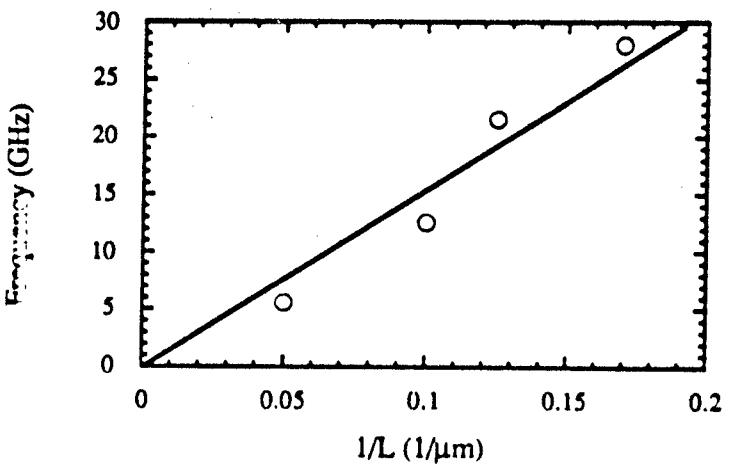


Figure 4.15 Frequency vs. (1/L) plot.

4.4 Discussion

4.4.1 Properties of the RG-MESFET Oscillator

The microwave measurement indicates that the RG-MESFET is operated in a single domain mode. Is this RG-MESFET oscillator simply a Gunn oscillator? The following observations indicate that the answer is no.

Take a device with $X_S = X_D = 0$ and LxW = 20 x 20 μm. Since the gate overlap of the source is eliminated , V_{SG} and V_{GG} are decoupled. Variations in V_{GG} will not affect the electron injection level at the source. To see the effect of V_{GG} on the oscillation, the source-to-gate1 voltage V_{SG} is fixed at 0.5V. Table 4.2 summarizes the observation results.

Notice that in Table 4.2, the effective drain-to-source bias $V_{DS}=V_{GG}+V_{DG}-V_{SG}$ is maintained at 13.5V. Oscillation only occurs when the gate field $V_{GG} / (L+X_S+X_D)$ is in the regime of negative differential mobility for electrons in GaAs, in this case, greater than 10.5V / 20 μm = 5250 V/cm. Therefore, the channel field is not determined by the drain-to-source voltage, but rather by the linear potential drop along the resistive gate.

For the RG-MESFET oscillator, the frequency can be tuned by V_{SG}, although the tunability is not very impressive. The frequency can be changed by changing the electron injection level. The fact that the frequency is not affected by changing V_{DG} proves that the device can be approximated as a constant current source, as expected for the CDO device. The only function of the drain is to remove any electrons which drift down the channel.

Table 4.2 Effect of bias condition on the oscillation behavior. Device parameters: L x W = 20 x 20 μm, $X_S=X_D=0$. The electron injection level is held by applying a constant source-to-gate1 voltage $V_{SG}=0.5V$. V_{GG} is stepped, and V_{DG} is adjusted at each bias to keep V_{DS} constant at 13.5V.

V_{GG} (V)	V_{DG} (V)	V_{DS} (V)	Oscillation?
14	0	13.5	Yes
12	2	13.5	Yes
10.5	3.5	13.5	Yes
10	4	13.5	No
9	5	13.5	No
7	7	13.5	No

4.4.2 Requirement of the Resistive Gate

The natural questions are why there is no contiguous domains forming with the resistive gate on top, and if the resistive gate is really screening the space charge.

In the computer simulation, the linear potential on the gate is always fixed. Any influence of space charge effects on the gate potential distribution is neglected. If this influence is calculated, assuming an ideal gate of uniform sheet resistance, the variation of gate potential distribution is shown in Fig. 4.16 (The simulation is not self consistent, merely to indicate the effect of oscillation on the potential along the gate). The larger the sheet resistance, the larger the variation of voltage along on the gate.

The upper limit of sheet resistance R_S can be estimated by setting

$$\Delta I_G << \bar{I}_G = \frac{\xi_a W_G}{R_S} \tag{4.7}$$

where I_G is the average gate current, ΔI_G is the peak-to-peak variation of I_G, W_G is the gate width, and ξ_a is the applied electric field. That way, the channel potential will retain its linearity and the electric field can be kept constant to ensure that multiple domains occur. In the absence of diode current (no spillover), the variation of gate current is given by the variation in capacitor current i_C:

$$i_C = qW \frac{\partial n_1}{\partial t} \tag{4.8}$$

Therefore,

$$\Delta I_G = i_C = qW\Delta n_s v_d << \frac{\xi_a W_G}{R_S} \tag{4.9}$$

Here, $v_d = \Delta y / \Delta t$ is the domain velocity, W is the channel width, and Δn_s is the peak-to-peak sheet electron density in the channel. The final result for the upper bound of the gate sheet resistance is:

$$R_S << \frac{\xi_a}{q\Delta n_{pp} v_d} \left(\frac{W_G}{W}\right) \tag{4.10}$$

Taking data from the computer simulation result for a device having channel doping $N_D = 1.2 \times 10^{17}$ cm^{-3}, $\Delta n_{pp} = 7 \times 10^{11}$ cm^{-2}, $v_d = 10^7$ cm/s, the upper limit for R_s is equal to 7.1 kΩ per square for an electric field of 8000V/cm.

Too low a resistivity results in an unacceptable amount of heating in the gate and higher resistance allows the gate voltage to be moduled locally by electron domains. To be on the safe side, $R_S = 3k\Omega$ per square will be the target for choosing proper gate material.

Therefore, the present existing RG-MESFET oscillators need to be modified to have a lower gate resistance to be able to screen the space charge in the channel.

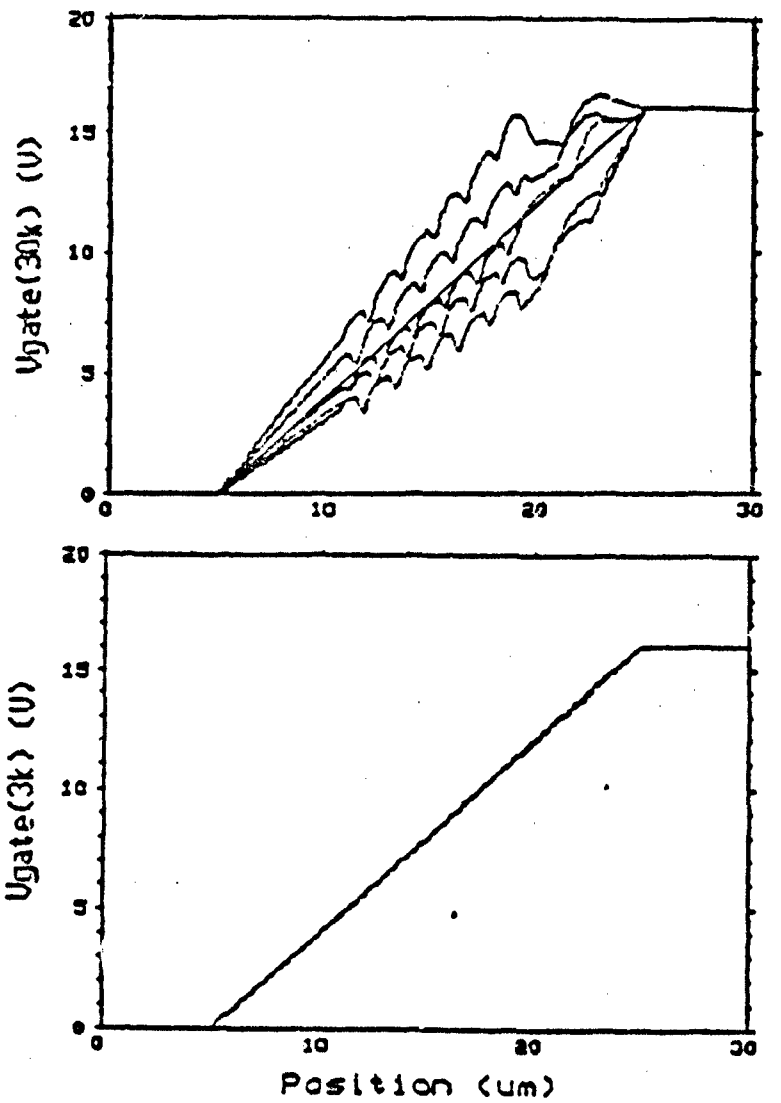


Figure 4.16 Gate voltage variation due to the existence of charge packets in the channel of an RG-MESFET with gate resistance of (a) 30kΩ/square, and (b) 3 kΩ/square [24].

4.5 CrSiO Film as Resistive Gate Material

As discussed in the previous section, the single domain generation and propagation in the RG-MESFET oscillator is caused by the high resistivity of the gate. In order for the contiguous domain oscillation mode to occur, the sheet resistance of the gate has to be around 3kΩ/square. The present resistive gate is made of WSiN and has a thickness of 1100Å and a sheet resistance of 30kΩ/square.

To modify the existing RG-MESFET oscillator, it is necessary to etch away the original resistive gate and deposit a new resistive gate with the right sheet resistance. Keep in mind that since we also want to eliminate the gate overlapping on the source and drain, new gate contacts need to be formed along with a new gate film. There are two ways to accomplish this. Fig. 4.17 (a) shows the sequence of depositing the new gate first and then depositing the contact metal. This process requires two lithography steps. Fig. 4.17(b) is just the opposite, but requires three lithography steps.

The new gate film has to make a low-leakage Schottky contact to the semiconductor. It has to be very uniform to provide a uniform electric field in the RG-MESFET channel. The thickness should be from 1000 to 2000Å. With a resistivity one order of magnitude smaller than the original WSiN gate, the sheet resistance of the material should be from 3kΩ/square to 1.5kΩ/square. In addition, an ohmic contact is required for this film with a very small contact resistance.

Song et al.[26] have fabricated an electron-beam evaporated Cr-SiO /GaAs diode and measured the current-voltage characteristics. According to their result, a very good Schottky-diode characteristics for the Cr-SiO cermet/GaAs diode can be obtained by annealing at 425^0C. The leakage current is nearly two orders of magnitude lower than those of annealed Al and Cr Schottky diodes. Moreover, the annealing temperature and the composition of the film were found to be useful parameters for adjusting the values of the resistivity [27-30]. Therefore, Cr-SiO cermet film is the choice for modifying the RG-MOSFET.

As indicated by Song et al [26], the evaporation temperature of Cr and SiO are relatively low and close to each other, which makes the Cr-SiO cermet a good choice for electron-beam evaporation. The use of a mixture of powders as an evaporation source makes it convenient to change the film composition.

However, due to the different fabrication conditions used and the varying nature of the cermet film, the resistivity of the resulting films needs to be carefully controlled for this particular application. There has been no report on the fabrication of the ohmic contact on

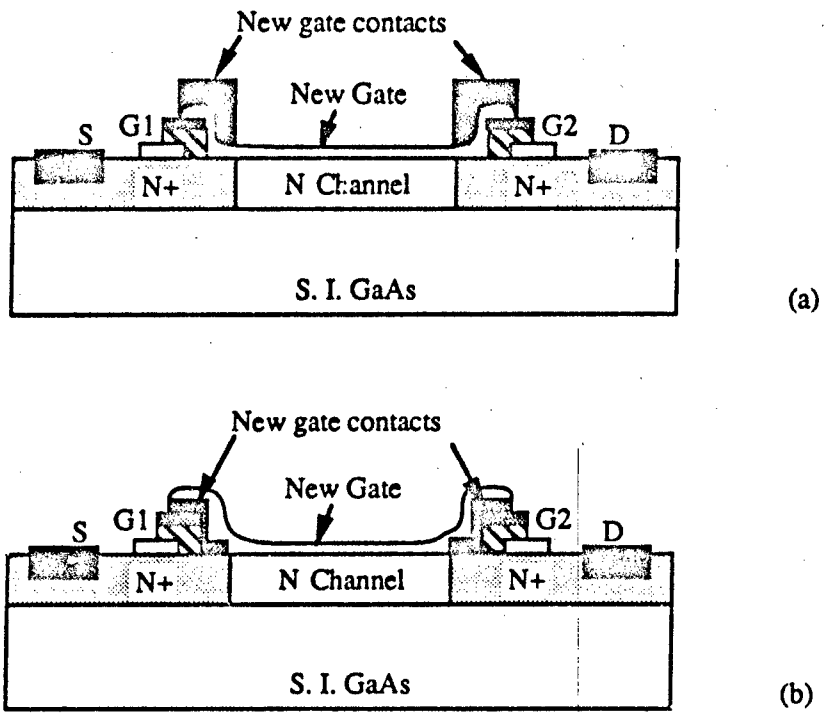


Figure 4.17 Modification of the RG-MESFET oscillator.
The gate of Fig. 4.1 has to be etched away first. Two process sequences can be used. (a) deposit the new gate first and then the gate contacts. (b) deposit the contact metal first and then the new gate film.

the cermet films, which is very critical to us and many other applications, especially when the sheet resistance is low.

To investigate the resistivity, 60 wt.%Cr-40 wt.%SiO and 55 wt.%Cr-45 wt.%SiO resistors were fabricated. Heat treatment was performed the same way as it would be in the modification of the RG-MESFET oscillators for the 60 wt.%Cr-40 wt.%SiO cermet film. Different metalization schemes were investigated in order to reduce the contact resistance. To better control the sheet resistance of the film, plasma etching using CF_4 and O_2 was used. The RG-MESFET oscillators were modified by etching the original gate away.

depositing Cr-SiO cermet film, and contacting it with Ti/Au metal layers. IV measurements indicate that the cermet films basically meet the requirements stated above.

4.5.1 Fabrication of Cermet Resistors

The source of the evaporation was prepared by mixing powders of Cr (50 mesh) and SiO (120 mesh) (both were from Johnson Matthey Inc, Alpha Products, 152 Andover Street, P.O. Box 299, Danvers, MA 01923) into 60 wt.%Cr-40 wt.%SiO and 55 wt.%Cr-45 wt.%SiO compositions.

Si substrates with thermally grown oxide films of about 1500Å thickness (not critical, mainly for insulating purposes) were prepared by degreasing in trichloroethylene, acetone and methanal with ultrasonic agitation for 5 mins each and rinsing with DI water. Positive photoresist (AZ1350J-SF) was spun at 4000 r.p.m. for 30 seconds and optically patterned in preparation for lift-off. The pattern includes resistors with different lengths and widths as well as 1cm x 1cm squares. The former are for measuring the film sheet resistance and contact resistance by probing the contact metal. The latter are for measuring the sheet resistance measurement by 4-point probe. The resistors have two metal pads (200μm by 200μm) on the ends, also formed by lift-off process.

The evaporation of the cermet film is carried out in a Varian E-beam evaporation system with a deposition rate and thickness monitor. The beam voltage of the electron gun is about 6 kV, which is fixed for our system. Because of the high electron gun voltage, the beam current is very small, around 0.01A. The resulting deposition rate is around 20-40 Å/s. The system pressure before evaporation is typically $2x10^{-7}$ torr. The evaporation is monitored to stop when the sheet resistance reaches the desired value.

4.5.2 Film Characterization

Film thickness is measured by an Alpha-Step 200 manufactured by Tencor Instruments, which is a computer controlled stylus instrument. Measurement is carried out by physical contact of stylus and films.

The sheet resistance is measured in two ways. The easy and fast one is by a Digital Resistivity Test System (4-point probe). The other way is to probe the resistors with different length and construct an RW vs. L plot. Here R is the measured resistance of a resistor with length L and width W. The slope of the straight line is the sheet resistance of the film and the intercept derived by W is the total contact resistance $2R_c$, since

$$R = R_s \frac{L}{W} + 2R_c \qquad (4.11)$$

4.5.3 Result and Discussion

4.5.3.1 Sheet Resistance of Cermet

The composition, thickness, sheet resistance, and bulk resistivity of the films at room temper before the thermal annealing are shown in Table 4.3.

Table 4.3 Properties of the evaporated cermet films

Cr wt. %	Sample	Thickness (Å)	R_s at 300°K (kΩ/square)	ρ (x10^{-3}) (Ω-cm)
55 %	CR8	3983	38.88	1.55
	CR9	3433	54.61	1.87
60 %	CR13	2523	9.04	0.23
	CR14	2230	5.57	0.12
	CR15	3440	6.42	0.22
	CR16	1513	5.93	0.09
	B10F	2313	5.22	0.12

Note that the data are scattered. This is because the source is made of powder material with high melting points. The source does not melt, only sublimes during the evaporation [32]. One component might evaporate a little faster than the other. Therefore, during the evaporation, it is important that the timing of each action (turn on high voltage, turn on emission current, open the shatter, etc.) is kept the same for every run to ensure reproducibility. Also, fresh material is desired for each evaporation. One better way is to compress the powder material so that the particles are in contact to each other and the heat transfer is more uniform. As seen in the table, the resistivity of 60 wt.%Cr-40 wt.%SiO cermet is a better choice for the RG-MESFET device modification. Although the resistivity is bigger than the desired value of 0.03 Ω-cm, it is shown later that thermal annealing will reduce the resistivity considerably. A thickness of around 2000Å is desirable since the

relative thickness variation is smaller, which is important for the CDO device. The surface profile of the resistor from the Tencor Alpha-step measurement indicates that the film is fairly uniform.

Annealing of the cermet films is performed in a Marshal furnace. The experimental results are summarized in Fig. 4.18. When exposed to the air, the sheet resistance is higher compared with that under otherwise the same annealing conditions due to the existence of oxygen. In all cases, reduced sheet resistances are measured after annealing. Continued annealing will further reduce the resistivity of the film.

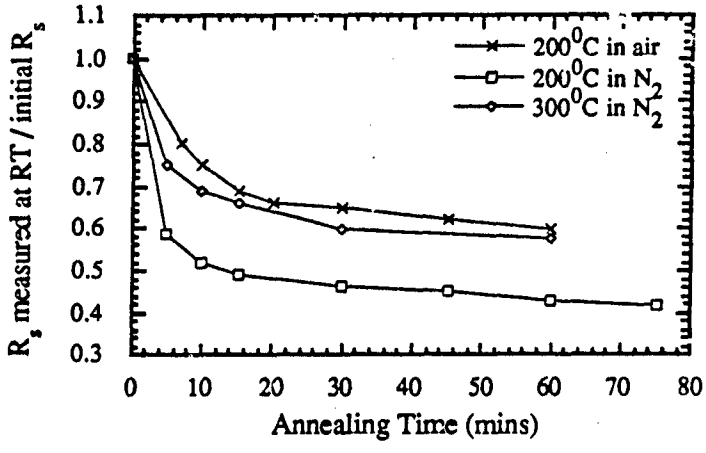


Figure 4.18 Relative resistance of Cr-SiO films (60 wt.%Cr-40 wt.%SiO) as a function of annealing time. The sheet resistance is measured by 4-point probe.

4.5.3.2 The Contact Resistance

The contact resistance between the Cr-SiO film and the metal pad is an important parameter that has to be kept small.

Experimental results show that a plasma clean is necessary right before the cermet evaporation. This is seen in Fig 4.19 for resistors with Ti/Au metal pads (500 Å/1000Å, evaporated in Varian E-beam evaporation system). The Ti/Au pads were evaporated first. If the preclean is omitted, the resistance of the resistor varies considerably (Fig. 4.19 (a)). Although the average slope is close to the sheet resistance from the 4-point probe measurement, the contact resistance is fairly large and nonuniform from resistor to resistor.

Preclean makes the contact resistance smaller and more uniform (Fig. 4.19 (b)). It is believed to remove the residual resist at the surface of the metal pads. The preclean is done using CF_4 in a Technics PE IIA plasma system for 10 sec. with RF power of 40 W and chamber pressure of 400 mTorr.

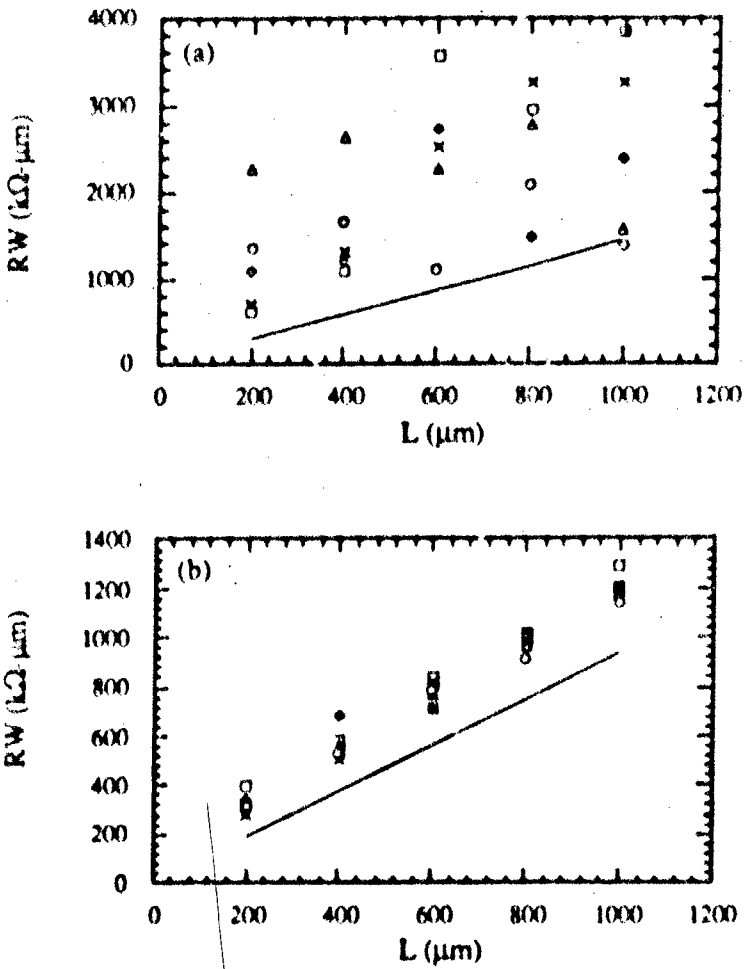


Figure 4.19 Effect of preclean on the contact resistance. Metal is evaporated before the cermet film. Each symbol represents a set of resistors of different length in a die. The solid straight line is the result measured from the 4-point probe.
(a) No precleaning.
(b) Preclean using CF_4 in a Technics plasma system with RF power of 40 W and chamber pressure of 400 mTorr.

As seen, preclean greatly improves the quality of the contacts.

If the order of metal pad and cermet film is interchanged, i.e., Ti/Au is placed on cermet, lower contact resistance is observed (Fig. 4.20). This is because when the cermet is place on Ti/Au pad, the inert nature of the gold prevents adhesion to the cermet layer by chemical bonding. The transition metal titanium promotes the adhesion to both cermet and gold.

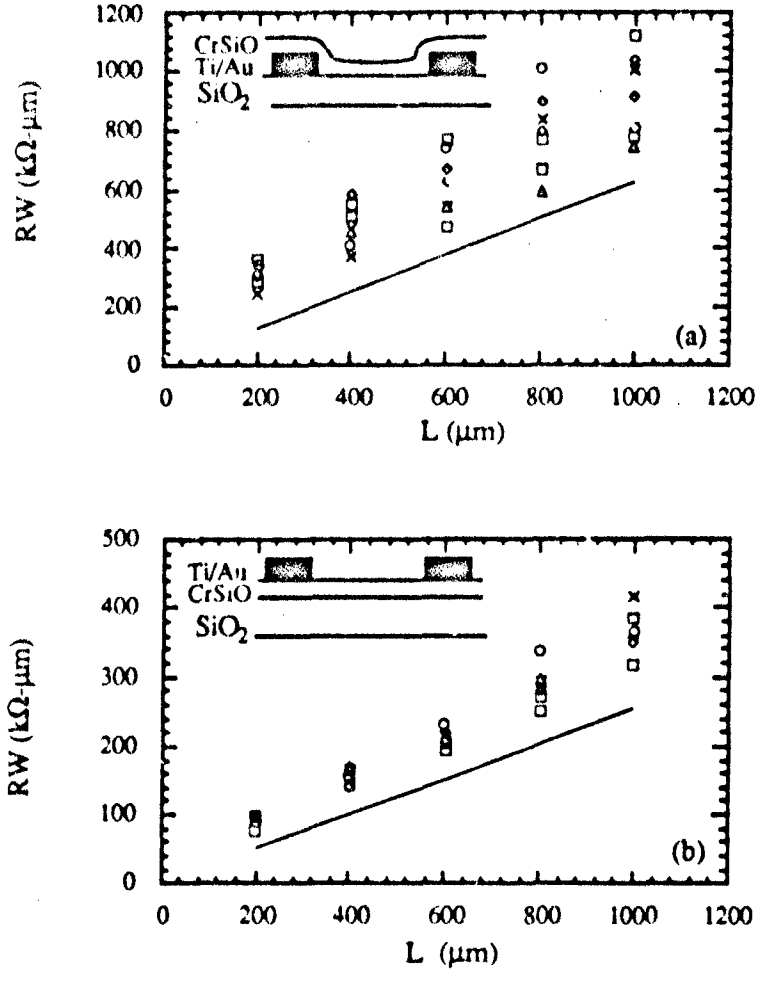


Figure 4.20 Effect of the fabrication sequence of making resistors. Each symbol represents a set of resistors of different length in a die. The solid straight line is the result measured from the 4-point probe.
(a) Cermet on Ti/Au.
(b) Ti/Au on cermet.

Case (b) has a smaller contact resistance and less scattered than that of case (a).

In order to minimize the contact resistance, several metal interconnections were investigated. All the resistors are fabricated by evaporating metal on top of the cermet. Preclean is performed before the metalization. Ti/Au and Ni/Ti/Au are evaporated in a Varian E-beam system with thickness monitor. Al and Cr/Au are evaporated in an NRC system. Thickness is not well controlled. Fig. 4.21 shows the effect of four types of metalization on the contact resistance. Trying to obtain a better contact, a 400^0C annealing in N_2 for 10 minutes is performed on all the resistors. As shown, better ohmic contacts are obtained after annealing except for Cr/Au metalization.

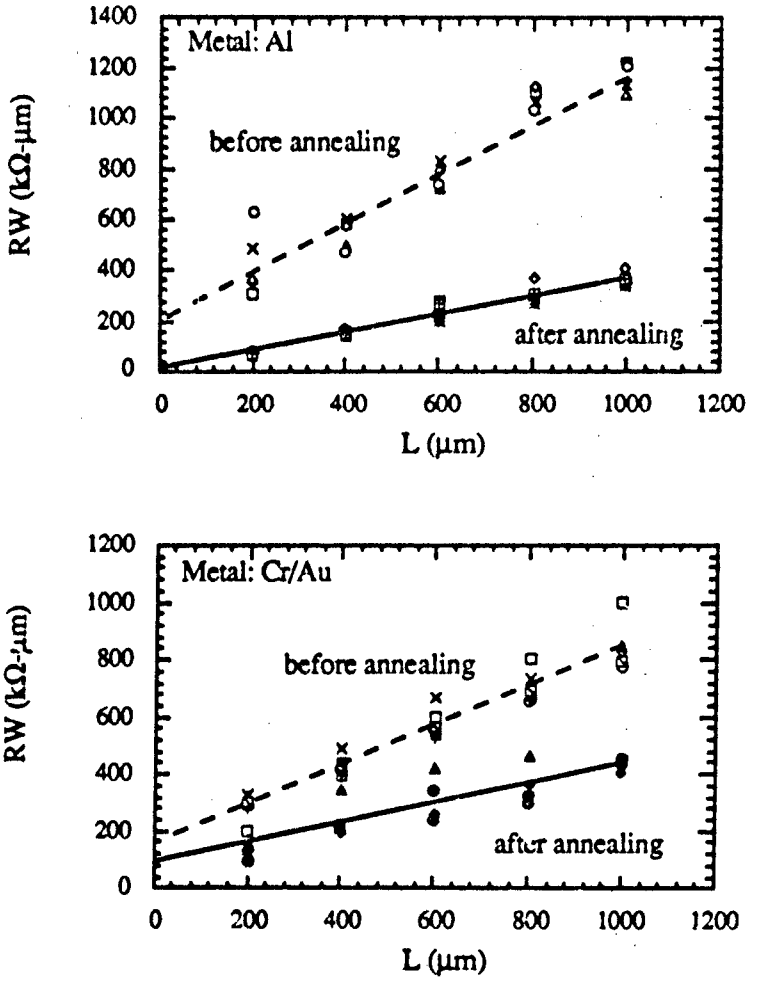


Figure 4.21 Effect of Al, Cr/Al, Ni/Ti/Au, and Ti/Au metalization on the contact resistance. The resistance of all the samples is measured before (open symbols and dased lines) and after (solid symbols and solic lines) thermal annealing at 400^0C in N_2 for 10 min.

After annealing, the contact resistances are all reduced. The data are less scattered after annealing except for the Cr/Au metalization. For Ti/Au metalization, the contact resistance is eliminated entirely.

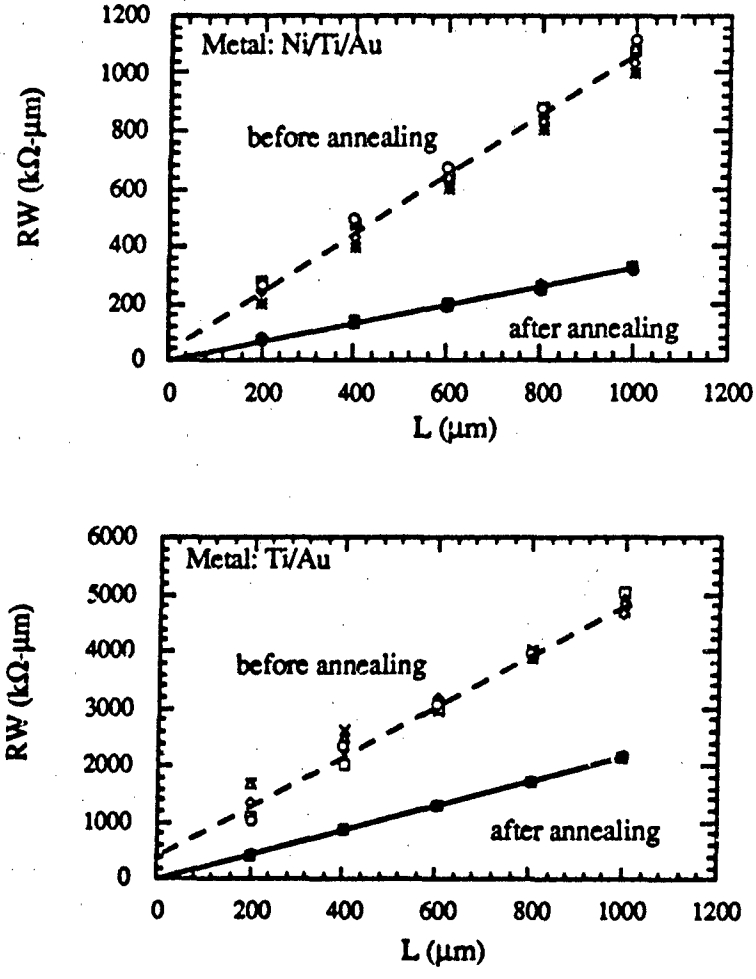


Figure 4.21, continued.

4.5.3.3 Plasma Etch of the Cermet Film

It is desirable to find an etchant for the cermet film if necessary. The etchant gas of CF_4, O_2, N_2 and the mixture of CF_4 and O_2 were tested. Only the mixture of CF_4 and O_2 is able to etch the cermet film. The etch rate is 453Å/min using $100CF_4 : 50O_2$ at a chamber pressure of 400 mTorr and power of 150W in a Branson/IPC barrel etcher. In contrast, the etch rate of Au under the same conditions is 80Å/min.

4.5.4 RG-MESFET Device with 60%Cr-40%SiO Cermet Gate

The result of CrSiO film fabrication indicate that the modification procedure depicted in Fig. 4.17 (a) is a good choice. It requires only two lithogartphy steps. With the Ti/Au metal on top of the CrSiO gate, the contact resistance is minimized.

60 wt.%Cr-40 wt.%SiO cermet film was used to form a resistive gate on an RG-MESFET oscillator. To do that, PMMA positive photoresist was spun on the original RG-MESFET device at 400 r.p.m. for 30 sec. and baked at 160^0C for 4 hours. A window exposing old WSiN was defined by electron-beam direct writing. WSiN was etched away using CF_4 in a Branson/IPC Barrel etcher with power of 150W and chamber pressure of 0.4 torr. A 60 wt.%Cr-40 wt.%SiO cermet film was then evaporated and lifted off. The second lithography defines the metal contacts and Ti/Au metalization to the cermet was e-beam evaporated. As a result of the 4-hour bake at 160^0C and the heat exposure during the metalization in this sequence, the resistivity of the resulting cermet was stabilized. After the metalization, a 10 min anneal at 400^0C was done to reduce the contact resistance. The resulting cermet gate had a sheet resistance of 0.5 kΩ/square. The IV curve is shown in Fig. 4.22. The fact that the gate current I_{G2} varies linearly with respect to the applied gate voltage V_{GG} is a strong indication that the leakage current of the cermet/GaAs Schottky junction is small.

Unfortunately, because the gate resistance was so small, the gate was destroyed before any oscillation was observed. Since this modification process has shown that CrSiO can reduce the gate resistance and form low leakage Schottky contact with GaAs, it is ideal to design new RG-MESFET device and incorporate the CrSiO resistive film process in the fabrication sequence.

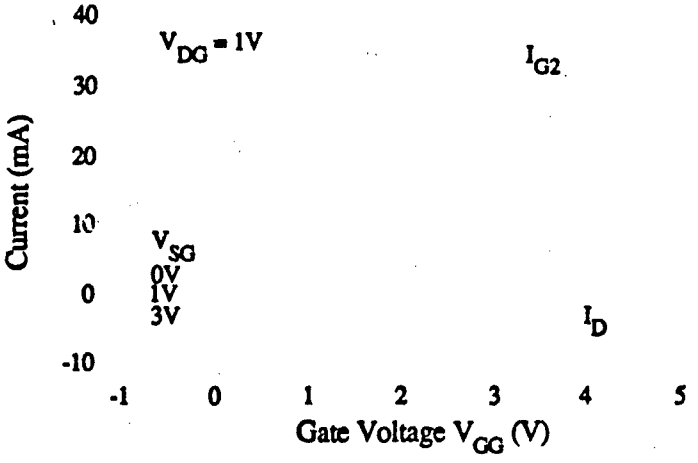


Figure 4.22 IV characteristics of a RG-MESFET device with a 60 wt.%Cr-40 wt.%SiO cermet gate. LxW=10x20.

4.6 Conclusion

The resistive gate MESFET devices have been fabricated to test the contiguous domain concept. The device with channel doping density of 1.2×10^{17} cm^{-3} and channel depth of 1500Å exibits microwave oscillation. The oscillation is identified as single domain oscillation due to the high gate sheet resistance of 30kΩ/square. Preliminary analysis indicates that the gate sheet resistance has to be lowed to about 3kΩ/square to avoid the gate potential variation caused by the channel oscillation. Cermet fabrication process was developed to obtain a desirable resistive film for future fabrication of CDO devices.

CHAPTER 5
EQUIVALENT CIRCUIT SIMULATION OF THE RG-FET

5.1 Introduction

As shown in the last chapter, single domain oscillation is obtained in the RG-MESFET device. However, the TOF program is not able to simulate the single domain since in the TOF program the channel potential is only determined by the gate voltage. The effect of source and drain is neglected. In order to simulate contiguous domain and single domain oscillation, a very simple lumped circuit model is developed. This model demonstrates, for the first time, the oscillation mode transition in a doped channel RG-FET structure.

The equivalent circuit model is established through the equations of state approach [33]. In this approach, one first derives the current-voltage relationships (or in some instance, charge-voltage relations) which describe the internal operation of the device. Next an equivalent circuit is deduced by combining idealized circuit elements in such a manner as to yield the same current-voltage (or charge-voltage) equations.

The equations of state include three basic relationships expressing continuity in semiconductor devices. The change in hole density in a region over a interval of time must equal the excess of flow into the region for that interval plus the excess generation of hole-electron pairs during the interval. A similar relationship applies to electron density. In addition, the changes in potential of a region are related to the charge through Poisson's equation.

Assuming no generation-recombination sources inside the semiconductor, the three continuity equations are:

$$\frac{\partial p_v}{\partial t} + \frac{1}{q}\nabla j_p = 0 \tag{5.1a}$$

$$\frac{\partial n_v}{\partial t} - \frac{1}{q}\nabla j_N = 0 \tag{5.1b}$$

$$-\varepsilon_s \nabla^2 \phi = q\,(p_v - n_v + N_D - N_A) \tag{5.1c}$$

where p_v is the volume density of holes, n_v is the volume density of electrons, and ϕ is the intrinsic Fermi potential in the channel. From Boltzmann transport theory, the total electron and hole current density (AC + DC), j_N and j_P in equation (5.1) can be written as functions of quasi-Fermi levels for electrons and holes, v_N and v_P:

$$j_p = - q\mu_p p_v \nabla v_p \tag{5.2a}$$

$$j_N = - q\mu_n n_v \nabla v_N \tag{5.2b}$$

or alternatively, j_N and j_P can be written as functions of ϕ, n_v and p_v, consisting of drift and diffusion component:

$$j_p = q\mu_p \xi\, p_v - qD_p \nabla p_v \tag{5.3a}$$

$$j_N = q\mu_n \xi\, n_v + qD_n \nabla n_v \tag{5.3b}$$

where μ_n and μ_p are the electron and hole mobilities and D_n and D_p are the electron and hole diffusivities. μ_n, μ_p, D_n and D_p are functions of electric field ξ.

From Eqn (5.1), we can derive an equivalent circuit model for specific device structures. We will work our way through from a very simple one-dimensional semiconductor stub to a doped channel RG-FET structure to show the simplicity and validity of the model.

5.2 Equivalent Circuit Model for a Semiconductor Stub

A semiconductor stub is chosen to illustrate the ideas regarding lumped circuit model. The structure to be simulated is shown in Fig 5.1(a). The problem is one-dimensional, assuming all the quantities are uniform along the x and z directions. Equations (5.1) and (5.2) then become:

$$\frac{\partial p_v}{\partial t} + \frac{1}{q}\frac{\partial j_P}{\partial y} = 0 \tag{5.4a}$$

$$\frac{\partial n_v}{\partial t} - \frac{1}{q}\frac{\partial j_N}{\partial y} = 0 \tag{5.4b}$$

$$- \varepsilon_s \frac{d^2\phi}{dy^2} = q\,(p_v - n_v + N_D - N_A) \tag{5.4c}$$

where

$$j_P = q\mu_p\left(- \frac{\partial \phi}{\partial y}\right) p_v - qD_p \frac{\partial p_v}{\partial y} \tag{5.5a}$$

$$j_N = q\mu_n\left(- \frac{\partial \phi}{\partial y}\right) n_v + qD_n \frac{\partial n_v}{\partial y} \tag{5.5b}$$

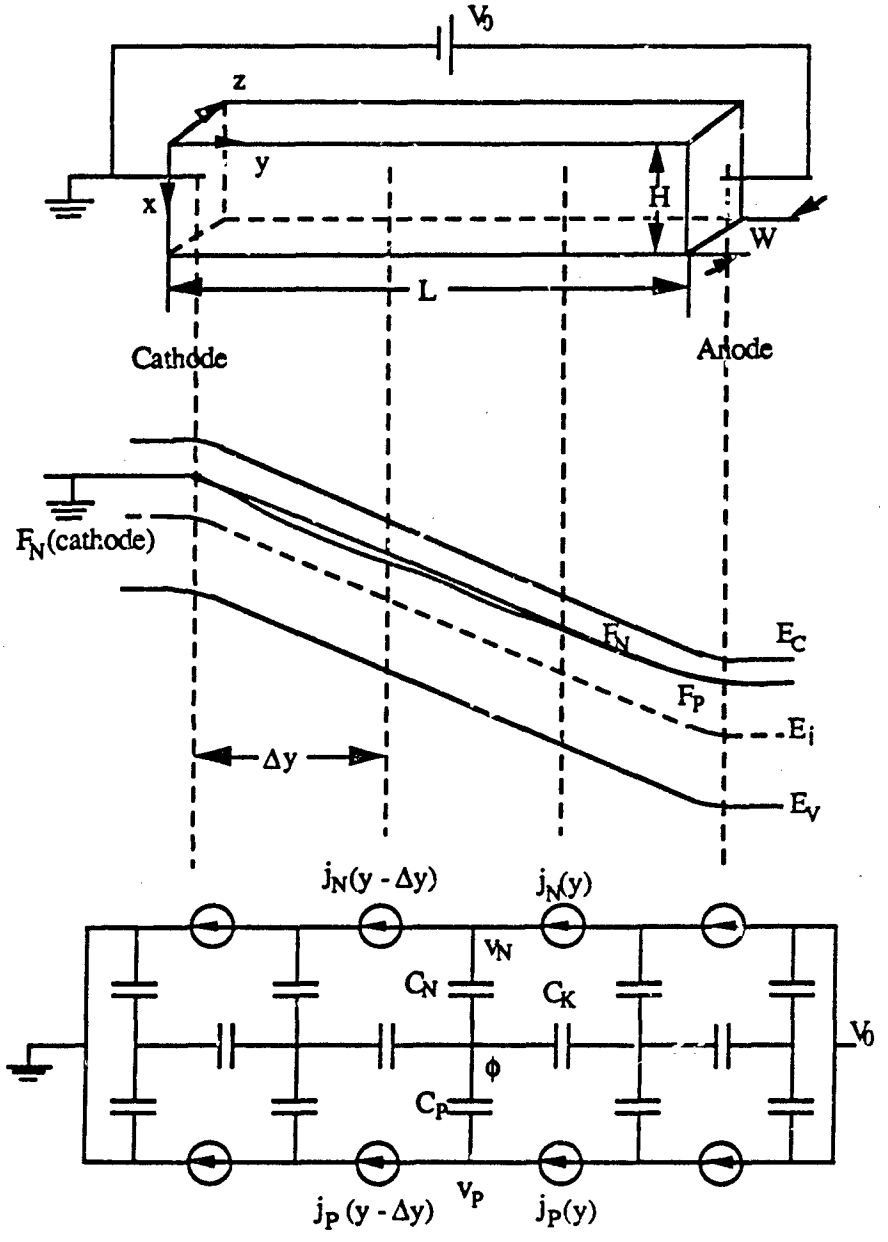


Figure 5.1 (a) Structure, (b) band diagram, and (c) equivalent circuit of the semiconductor stub.

Choosing the potential reference to be the Fermi level at the cathode (Fig. 5.1b), we define:

$$v_p(y) = \frac{F_N(\text{cathode}) - F_p(y)}{q} \tag{5.6a}$$

$$v_N(y) = \frac{F_N(\text{cathode}) - F_N(y)}{q} \tag{5.6b}$$

$$\phi(y) = \frac{F_N(\text{cathode}) - E_i(y)}{q} \tag{5.6c}$$

Hole and electron volume density can be expressed in terms of v_P, v_N and ϕ using Boltzmann statistics,

$$p_v = n_i e^{(E_i - F_P)/k_B T} = n_i e^{q(v_P - \phi)/k_B T} \tag{5.7a}$$

$$n_v = n_i e^{(F_N - E_i)/k_B T} = n_i e^{q(\phi - v_N)/k_B T} \tag{5.7b}$$

The time variation of p_v and n_v can be found by differentiating (5.7):

$$\frac{\partial p_v}{\partial t} = \frac{q}{k_B T} p_v \frac{\partial}{\partial t}(v_p - \phi) \tag{5.8a}$$

$$\frac{\partial n_v}{\partial t} = \frac{q}{k_B T} n_v \frac{\partial}{\partial t}(\phi - v_N) \tag{5.8b}$$

Substituting (5.8a & b) in (5.4a & b), we have

$$\frac{q^2}{k_B T} p_v \frac{\partial}{\partial t}(v_p - \phi) + \frac{\partial j_p}{\partial y} = 0 \tag{5.9a}$$

$$\frac{q^2}{k_B T} n_v \frac{\partial}{\partial t}(v_N - \phi) + \frac{\partial j_N}{\partial y} = 0 \tag{5.9b}$$

The time derivative of (5.4c) yields:

$$-\varepsilon_s \frac{\partial}{\partial t}\frac{d^2\phi}{dy^2} = q\left(\frac{\partial p_v}{\partial t} - \frac{\partial n_v}{\partial t}\right) \tag{5.10}$$

After defining a displacement current

$$j_I = -\frac{\varepsilon_s}{\Delta y}\frac{d\phi}{dt} \tag{5.11}$$

(5.10) becomes:

$$\frac{q^2}{k_B T} p_v \frac{\partial}{\partial t}(\phi - v_p) + \frac{q^2}{k_B T} n_v \frac{\partial}{\partial t}(\phi - v_N) + \frac{\partial j_I}{\partial y} = 0 \tag{5.9c}$$

The governing differential equations (5.9a, b &c) result in a distributed model in nature. The dimensions of the element are infinitesimal. The process of replacing differential equations by difference equations turns the infinitesimal elements into finite lumps. In this case, the semiconductor stub is divided into m small sections. For each section of length Δy, a single value of the pertinent variable - hole density p_v, electron density n_v, and static potential ψ - is selected to represent the whole element. Equations (5.9) become:

$$\frac{q^2}{k_B T} p_v \Delta y \frac{d}{dt}(v_P - \phi) = j_p(y - \Delta y) - j_p(y) \tag{5.12a}$$

$$\frac{q^2}{k_B T} n_v \Delta y \frac{d}{dt}(v_N - \phi) = j_N(y - \Delta y) - j_N(y) \tag{5.12b}$$

$$\frac{q^2}{k_B T} p_v \Delta y \frac{d}{dt}(\phi - v_P) + \frac{q^2}{k_B T} n_v \Delta y \frac{d}{dt}(\phi - v_N) = j_I(y - \Delta y) - j_N(y) \tag{5.12c}$$

Define

$$C_P = \frac{q^2}{k_B T} p_v \Delta y \quad \text{(farads/cm}^2\text{)} \tag{5.13a}$$

$$C_N = \frac{q^2}{k_B T} n_v \Delta y \quad \text{(farads/cm}^2\text{)} \tag{5.13b}$$

$$C_K = \frac{\varepsilon_s}{\Delta y} \quad \text{(farads/cm}^2\text{)} \tag{5.13c}$$

The equations of the state for the semiconductor stub become

$$C_P \frac{d}{dt}(v_P - \phi) = j_p(y - \Delta y) - j_p(y) \tag{5.14a}$$

$$C_N \frac{d}{dt}(v_N - \phi) = j_N(y - \Delta y) - j_N(y) \tag{5.14b}$$

$$C_N \frac{d}{dt}(\phi - v_N) + C_P \frac{d}{dt}(\phi - v_P) = j_I(y - \Delta y) - j_I(y) \tag{5.14c}$$

The form of Equation (5.14) clearly suggests node equations. It can be easily interpreted in terms of the three-line equivalent circuit model (Fig. 5.1c). The top and bottom lines can be thought of as representing the conduction and valence band, respectively. The central line represents the displacement current path [33].

Although Fig. 5.1c looks like a small signal equivalent circuit, the definition of C_P and C_N are in terms of the total hole and electron densities. Using this circuit correctly, we can simulate the large signal response.

5.3 Equivalent Circuit Model for a Gunn Diode

5.3.1 Simulation Procedure

In this section, a procedure for simulating a Gunn Diode (an n-type semiconductor stub) using the established equivalent circuit is described, which is applicable at a later point in the simulation of a doped channel RG-HET. Since we are only interested in the n-type semiconductor, the p-line is dropped out of the picture. The corresponding equivalent circuit is shown in Fig. 5.2.

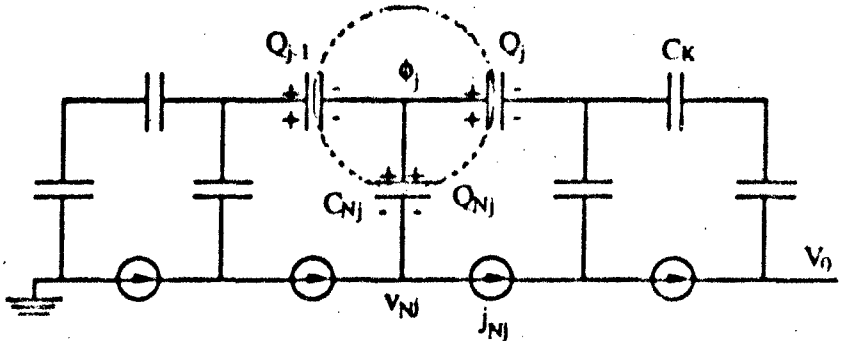


Figure 5.2 Equivalent circuit model for a Gunn Diode.

Given the instantaneous electron distribution and the terminal boundary conditions, the channel potential ϕ can be found by solving a one-dimensional Poisson's equation. In order to get Poisson's equation from the equivalent circuit, we need to work with the charge balance at each node in the I-line. At node j, the total charge on all capacitor plates is zero.

$$Q_j - Q_{j-1} + Q_{Nj} = 0 \tag{5.15}$$

Notice that all the charges Q in the above equation are large signal quantities. Since C_K is a constant capacitor, the total charge is simply the product of the capacitance, the voltage across it, and the related area:

$$Q_j = WH\, C_K (\phi_j - \phi_{j+1}) \tag{5.16}$$

where W and H are the width and height of the stub, respectively. For the voltage dependent C_N, the total charge is obtained by integrating the differential charge $C_N\, d(\phi - v_N)$ over the voltage difference:

$$Q_N = WH \int_{(\phi - v_N)_0}^{(\phi - v_N)} \frac{q^2}{k_B T} \Delta y\, n_v\, d(\phi - v_N)$$

$$= WH \frac{q^2}{k_B T} \Delta y\, n_i \int_{(\phi - v_N)_0}^{(\phi - v_N)} e^{q(\phi - v_N)/k_B T}\, d(\phi - v_N)$$

$$= WH\, q\, \Delta y\, n_i \left(e^{q(\phi - v_N)/k_B T} - e^{q(\phi - v_N)_0/k_B T} \right) \qquad (5.17)$$

where $(\phi - v_N)_0$ is determined by the DC electron charge on the capacitor through the relationship

$$N_D = n_i\, e^{q(\phi - v_N)_0 / k_B T} \qquad (5.18)$$

Therefore,

$$Q_{Nj} = WH\, q\, \Delta y\, (n_{vj} - N_D) \qquad (5.19)$$

Equation (5.15) now becomes:

$$C_K (\phi_{j-1} - 2\phi_j + \phi_{j+1}) = q\, (n_{vj} - N_D)\, \Delta y \qquad (5.20)$$

Recalling that $C_K = \varepsilon_s / \Delta y$, the final charge balance at node j is:

$$\varepsilon_s \frac{\phi_{j-1} - 2\phi_j + \phi_{j+1}}{\Delta y^2} = q\, (n_{vj} - N_D) \qquad (5.21)$$

This is exactly the same as the discretized Poisson's equation

$$\varepsilon_s \frac{d^2\phi}{dy^2} = q\, (n_v - N_D) \qquad (5.22)$$

To simulate the Gunn oscillation, the device is divided into m sections. (5.21) has to be solved numerically for the channel potential ϕ with the appropriate boundary conditions, given the electron density n_v. If ohmic contacts are assumed for the source/drain, the excess charges on the two contacts are zero. Therefore, the volume densities at the source and drain are fixed at the channel doping density, and so are the potentials at the contacts. The boundary conditions for Poisson's equation are:

$$\phi_1 = \frac{k_B T}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{5.23a}$$

$$\phi_m = V_0 + \frac{k_B T}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{5.23b}$$

where n_i is the intrinsic density of the semiconductor. Once the channel potential is obtained, the electric field in the channel is determined by

$$\xi_j = -\frac{\phi_j - \phi_{j-1}}{\Delta y} \tag{5.24}$$

The nonlinear velocity-field curve of (3.10c) is used to determine the velocity of electrons at each grid point:

$$\mu_{nj} = -\frac{\mu_0}{\left[1+\left(\frac{\mu_0 |\xi_j|}{v_{sat}}\right)^2\right]^{1/2}} \tag{5.25a}$$

$$v_{sat} = A_v e^{-\frac{\mu_0 |\xi_j|}{B_v}} + \frac{C_v}{1+\left(\frac{\mu_0 |\xi_j|}{D_v}\right)^{F_v}} \tag{5.25b}$$

and the electron current flow j_N can be calculated from Eqn (5.5b). From the current distribution, the time derivative of the electron concentration is obtained from the continuity equation (5.4b). From this time derivative, the electron density an instant later is computed:

$$n_{vj} = n_{vj}^{old} + \frac{1}{q}\frac{\partial j_N}{\partial y}\Delta t \tag{5.26}$$

with the boundary conditions:

$$n_{v1} = N_D \tag{5.27a}$$

$$n_{vm} = N_D \tag{5.27b}$$

and the cycle repeats [34]. The same algorithm shown in Fig. 3.3 is used here as in the Time-Of-Flight program. The only difference is in the calculation of the potential distribution. Here a set of linear equations has to be solved simultaneously.

5.3.2 Simulation Results

Fig. 5.3 shows the simulation results for a Gunn diode biased at 2V, using the above formuation. The device has a length of 2μm, width of 1μm and height of 1μm. The doping density is $1x10^{17}$ cm^{-3}. The number of grid points is 256. The typical time step Δt is in the femto second range and is self-adjusting. The nonlinear velocity field curve is used to obtain the oscillation. The parameters in (5.25b) are: μ_0=5200 $cm^2/V\text{-}s$, $A_v=9.55x10^7$, $B_v=1.316x10^7$, $C_v=5.8x10^7$, $D_v=6.788x10^5$, and $F_v=0.316$.

At time t=0, the surface electron density ($n_s=n_vH$ at the value N_DH) is constant except in the middle of the device where an arbitrary dipole domain is introduced (Fig. 5.3(a), black dots). As time evolves, this dipole grows, expands and quickly stabilizes. This stabilized dipole travels with a velocity of $9.15x10^6$ cm/s toward the drain, as determined from Fig. 5.3(a).

The applied electric field is V_0/L=10kV/cm without the dipole. With the existance of the introduced small dipole, the electric field inside the dipole increases and the field outside decreases a little. As the dipole grows, the field inside enhances and the field outside decreases further, as shown in Fig. 5.3(b). The same effect can also be seen in Fig. 5.3(c), where the slope of the curves represents the electric field.

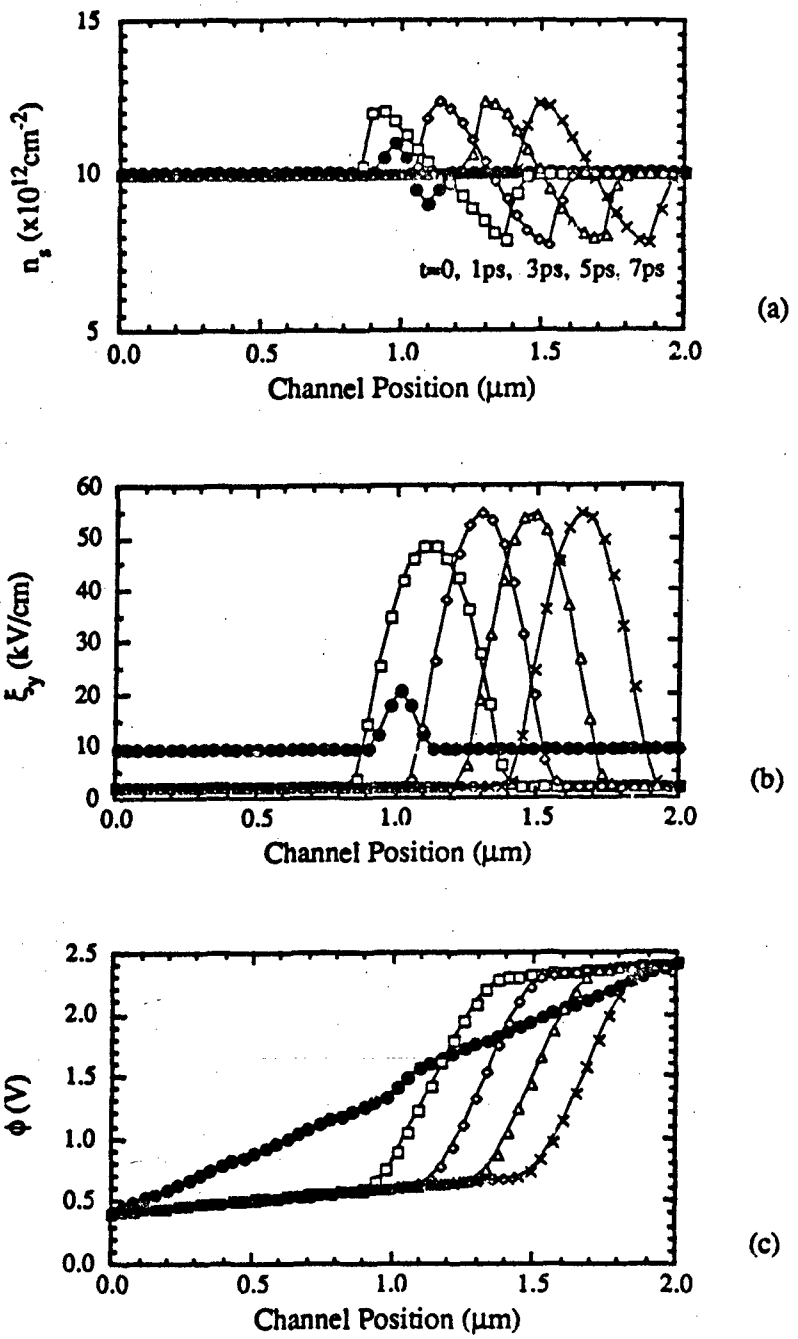


Figure 5.3 Simulation result for a 2 μm long Gunn diode biased at 2V. The doping density is $1x10^{17}$ cm^{-3}.

5.4 Equivalent Circuit Model for a Doped Channel RG-FET

The cross section of a doped channel RG-FET in Fig. 5.4 shows the device to consist of a p-type substrate with an n-diffusion overlaid by an insulator and a resistive gate. The n-diffusion, referred to as the channel region, looks like a "semiconductor stub" with the assumption that it is uniformly doped.

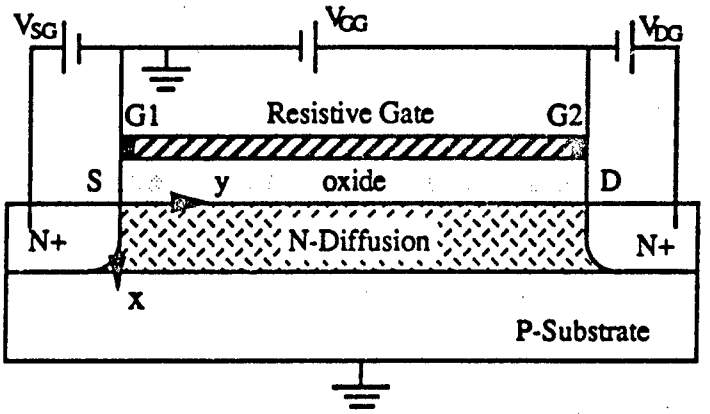


Figure 5.4 Cross section of a doped channel RG-FET.

5.4.1 Effect of the Gate on the Equivalent Circuit Model

Normally, the substrate is very lightly doped, and the depletion region in the channel due to the channel-substrate junction can be treated as zero. In the case of the gradual channel approximation [13], the cross section in the x direction should look, in general, like a regular doped channel MOSFET (Fig5.5a). Current flow in the x direction is zero. The only governing equation is Poisson's equation in x direction:

$$\varepsilon_s \frac{d^2\phi}{dx^2} = q\,(n_v - N_D) \tag{5.28}$$

Fig. 5.5(c) is the band diagram obtained by solving (5.28) for the block charge diagram shown in Fig. 5.5(b). The channel is connected to the gate through two capacitors, C_{ox} and C_D. C_D is the depletion capacitance associated with the depletion region of width x_d. C_{ox} is the insulator capacitance. The voltage across C_D can be determined by the following relationship:

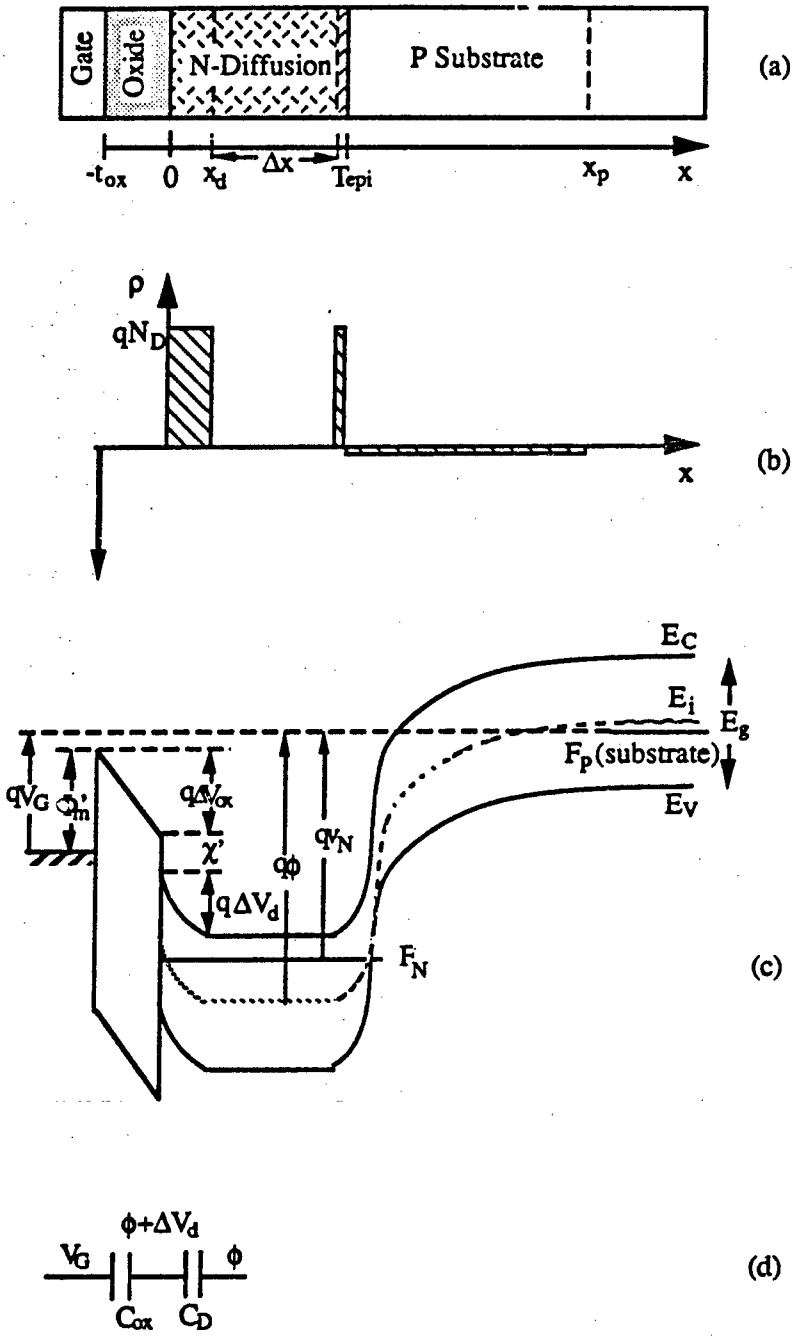


Figure 5.5 (a) Cross section, (b) block charge diagram, (c) band diagram, and (d) equivalent circuit model of a doped-channel MOSFET structure along the x direction, under the gradual channel approximation.

$$\phi - \frac{E_g}{2q} - \Delta V_d - \frac{\chi'}{q} - \Delta V_{ox} + \frac{\Phi'_m}{q} - V_G = 0 \tag{5.29}$$

where Φ'_m and χ' are the effective metal workfunction and electron affinity of the semiconductor, both relative to the conduction band of the oxide. Assuming that the gate charge is equal to the semiconductor bulk charge, the voltage drop on the oxide is:

$$\Delta V_{ox} = \frac{Q_G}{C_{ox}} \approx \frac{Q_B}{C_{ox}} = \frac{qN_D x_d}{C_{ox}} = \sqrt{2V_0}\sqrt{\Delta V_d} \tag{5.30}$$

where

$$V_0 = \frac{\varepsilon_s q N_D}{C_{ox}^2} \tag{5.31}$$

Define:

$$V'_{bi} = \frac{1}{q}(\Phi'_m - \chi' - \frac{E_g}{2}) \tag{5.32}$$

Substituting (5.30) and (5.32) into (5.29), we have:

$$\Delta V_d + \sqrt{2V_0 \Delta V_d} - (\phi + V'_{bi} - V_G) = 0 \tag{5.33}$$

Solving (5.33), the potential associated with the band bending ΔV_d is:

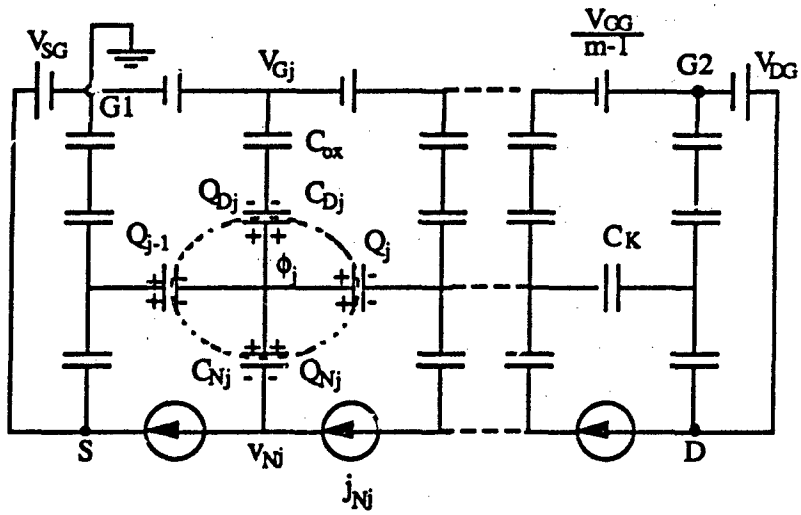
$$\Delta V_d = \phi + V'_{bi} - V_G + V_0 - \sqrt{V_0^2 + 2V_0(\phi + V'_{bi} - V_G)} \tag{5.34}$$

From Fig. 5.5(d), it is seen that the effect of the gate at each point in channel can be modeled by introducing capacitors to connect the channel and the gate. Therefore, the one-dimensional equivalent circuit of Fig. 5.2 can be extended to model an RG-FET. If the resistive gate is assumed to be ideal, i.e., it provides the linear potential drop which is independent of the charge oscillation in the channel, the gate can be modeled as a series of ideal voltage sources as shown in Fig. 5.6(a). When this assumption is removed, the gate can be modeled as a series of resistors, and the equivalent circuit is shown in Fig. 5.6(b).

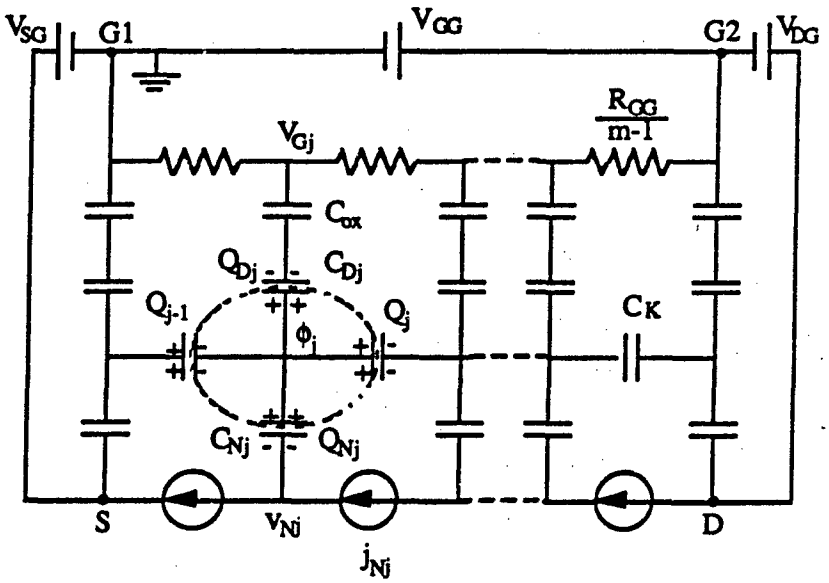
5.4.2 Qualitative Description of the RG-FET Operation

We would like to use the equivalent circuit in Fig. 5.6 to discuss the effects of the resistive gate on the operation of the RG-FET devices.

First of all, an ideal gate is assumed, i.e., the gate provides a linear potential distribution independent of the charge oscillation in the channel. In this case, the gate can



(a)



(b)

Figure 5.6 Equivalent circuit model for an RG-FET with (a) an ideal gate, and (b) a realistic gate.

be modeled as a series of ideal voltage sources (Fig.5.6(a)), sinking or sourcing as much current as need to be. When t_{ox} is small, the gate is placed very close to the channel, the linear gate potential distribution has great control over the channel potential and the gate is able to screen the charge variation in the channel. Contiguous domain oscillation is expected. As the gate is moved farther away, C_{ox} becomes much smaller and the gate is basically isolated from the channel. The source and drain gradually take over and eventually, single domain oscillation is expected.

For a more realistic gate, where the gate is modeled by real resistors (Fig. 5.6(b)), the gate voltage is no longer constant. The gate voltage at each grid point is determined by the channel condition and has to be solved iteratively in the simulation, although the total potential drop on the gate is fixed at V_{GG}. Current loop equations have to be set up for that purpose. As seen in Fig. 5.6(b), as the gate resistance gets bigger, the displacement current flowing into each (C_{Dj}, Cox) branch gets smaller. As the result of this, more displacement current flows along the channel, which means source and drain control of the channel is bigger. Single domain oscillation is more likely to occur. On the other hand, as the gate resistance is reduced, more displacement current would flow into the gate, giving the gate more control over the channel. As long as the displacement current is smaller than the DC current supplied by V_{GG}, the gate potential can be maintained approximately linear. In this case, the contiguous domain oscillation is expected.

5.4.3 Simulation Procedure

In the simulation, (ϕ_j, n_{lj}) is chosen as a set of pertinent variables for the discretized element j, where ϕ_j is the electrostatic potential depicted in Fig. 5.5(d) and n_{lj} is the electron density per unit width in the channel.

For the equivalent circuit model shown in Fig. 5.6, the total charge on all capacitor plates is zero for each node. At node j, the charge balance is:

$$- Q_{j-1} + Q_j + Q_{Nj} + Q_{Dj} = 0 \tag{5.35}$$

Assuming the substrate is semi-insulating, the depletion width due to the charge on the constant capacitor C_K is:

$$Q_j = W \Delta x_j C_K (\phi_j - \phi_{j+1}) \tag{5.36}$$

W is the width of the channel, and $\Delta x_j = T_{epi} - x_{dj}$ is the width of the undepleted channel region. The charge on C_N is derived in a similar way as described in equation (5.17):

$$Q_{Nj} = Wq\,(n_{1j} - N_D T_{epi} \Delta y) \tag{5.37}$$

The total charge on the channel depletion capacitor C_D is the total depletion charge:

$$Q_{Dj} = W\,\Delta y\, qN_D x_{dj} \tag{5.38}$$

Equation (5.34) is used to calculate x_d:

$$x_d = \sqrt{\frac{2\varepsilon_s}{qN_D}\Delta V_d} \tag{5.39}$$

Q_{Dj} in (5.38) is a non-linear function of channel potential ϕ_j. To linearize the Poisson's equation, the charge in the depletion region Q_{Dj} at any instant of time is expressed in terms of the charge at the previous time via the Taylor series. Therefore,

$$Q_{Dj} = W\Delta y\, qN_D x_{dj}^{old} + \frac{\partial Q_{Dj}}{\partial \phi_j}\Big|_{\phi_j=\phi_j^{old}} (\phi_j - \phi_j^{old})$$

$$= W\Delta y\, qN_D x_{dj}^{old} + \frac{\partial Q_{Dj}}{\partial \Delta V_{dj}} \frac{\partial \Delta V_{dj}}{\partial \phi_j}\Big|_{\phi_j=\phi_j^{old}} (\phi_j - \phi_j^{old})$$

$$= W\Delta y \left(qN_D x_{dj}^{old} + \frac{\varepsilon_s}{x_{dj}^{old}} \left[1 - \sqrt{\frac{V_0}{V_0 + 2\,(\phi_j^{old} - V_{Gj} + V_{bi}')}} \right] (\phi_j - \phi_j^{old}) \right)$$

$$= W\Delta y\, [\, qN_D x_{dj}^{old} + C_{Dj}'(\phi_j^{old})\, (\phi_j - \phi_j^{old}) \,] \tag{5.40}$$

ϕ_j^{old} is the channel potential at the previous time and x_{dj}^{old} is the depletion width under the gate evaluated at ϕ_j^{old}.

$$C_{Dj}' = \frac{\varepsilon_s}{x_{dj}} \left(1 - \sqrt{\frac{V_0}{V_0 + 2\,(\phi_j - V_{Gj} + V_{bi}')}} \right) \tag{5.41}$$

Substituting equations (5.36-38) into (5.35), the set of linearized Poisson's equations for a doped channel RG-FET with m elements is:

$$\phi_1 = \phi_{init}$$

$$\vdots$$

$$\alpha_{j-1}\phi_{j-1} - (\alpha_{j-1} + \alpha_j + \beta_j)\,\phi_j + \alpha_j \phi_{j+1} = \Delta y\, qN_D x_{dj}^{old} + q(n_{1j} - N_D T_{epi}\Delta y) - \beta_j \phi_j^{old}$$

$$\vdots$$

$$\phi_m = \phi_{last} \tag{5.42}$$

Where

$$\phi_{init} = V_{G1} + V_{SG} + \frac{k_B T}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{5.43a}$$

$$\phi_{last} = V_{G1} + V_{GG} + V_{DG} + \frac{k_B T}{q} \ln\left(\frac{N_D}{n_i}\right) \tag{5.43b}$$

are the boundary conditions for the Poisson's equation assuming the source and drain contacts are ohmic. α and β are defined as:

$$\alpha_j = C_K \Delta x_j \tag{5.44a}$$

$$\beta_j = C'_{Dj}(\phi_j^{old})\,\Delta y \tag{5.44b}$$

Equation (5.41) can be written in vector notation:

$$A\,x = B \tag{5.45}$$

where A is a tridiagonal matrix. Define $\gamma_j = \alpha_{j-1} + \alpha_j + \beta_j$,

$$A = \begin{bmatrix} 1 & 0 & 0 & 0 & \cdot\cdot & 0 & 0 \\ \alpha_1 & -\gamma_2 & \alpha_2 & 0 & \cdot\cdot & 0 & 0 \\ 0 & \alpha_2 & -\gamma_3 & \alpha_3 & \cdot\cdot & 0 & 0 \\ : & : & : & : & : & : & : \\ : & : & : & : & : & : & : \\ 0 & 0 & 0 & \cdot\cdot & \alpha_{m-2} & -\gamma_{m-1} & \alpha_{m-1} \\ 0 & 0 & 0 & \cdot\cdot & 0 & 0 & 1 \end{bmatrix} \tag{5.46a}$$

$$x = \begin{bmatrix} \phi_1 \\ \phi_2 \\ \phi_3 \\ : \\ : \\ \phi_{m-1} \\ \phi_m \end{bmatrix} \tag{5.46b}$$

$$B = \begin{bmatrix} \phi_{init} \\ q(n_{l2} - N_D T_{epi} \Delta y) + \Delta y\, qN_D x_{d2}^{old} - \beta_2 \phi_2^{old} \\ q(n_{l3} - N_D T_{epi} \Delta y) + \Delta y\, qN_D x_{d3}^{old} - \beta_3 \phi_3^{old} \\ \vdots \\ \vdots \\ q(n_{lm-1} - N_D T_{epi} \Delta y) + \Delta y\, qN_D x_{dm-1}^{old} - \beta_{m-1} \phi_{m-1}^{old} \\ \phi_{last} \end{bmatrix} \quad (5.46c)$$

(5.46) can be easily solved for a given electron density distribution, assuming an initial ϕ distribution. At any instant of time, the ϕ distribution has to be iterated until a consistent ϕ distribution is obtained.

Once the potential distribution is found, the electron flux can be calculted and the new electron density an instant later can be calculated by solving the current continuity equation.

The boundary conditions for the electron densities per unit width are:

$$n_{l1} = \Delta y\, N_D\, (T_{epi} - x_{d1}) \quad (5.47a)$$

$$n_{lm} = \Delta y\, N_D\, (T_{epi} - x_{dm}) \quad (5.47b)$$

where

$$x_{d1} = \sqrt{\frac{2\varepsilon_s}{qN_D} \Delta V_{d1}} \quad (5.48a)$$

$$x_{dm} = \sqrt{\frac{2\varepsilon_s}{qN_D} \Delta V_{dm}} \quad (5.48b)$$

ΔV_{d1} and ΔV_{dm} are obtained by substituting $V_G = V_{G1}$ and $V_G = V_{G1} + V_{GG}$ into (5.36), respectively.

The source code of the simulation program is listed in Appendix E.

5.4.4 Limitations of the RG-FET Equivalent Circuit Model

Examination of (5.35) - (5.38) reveals that if $\phi_{j-1} \approx \phi_j$ (i.e., ϕ is a slowly-varying potential in the channel, such that the gradual channel approximation is appropriate), then

$$n_{lj} \approx N_D \Delta y \, (T_{epi} - x_{dj}) \tag{5.49}$$

This means that the electrons fill the undepleted portion of the channel to equal the donor density N_D. If $\phi_{j-1} \neq \phi_j$ (i.e., ϕ changes significantly between adjacent grid points), then the electron density in the undepleted portion of the channel is

$$n_{lj} = N_D \Delta y \, (T_{epi} - x_{dj}) - \frac{\varepsilon_s}{q \Delta y} (\Delta x_{j-1} \phi_{j-1} - (\Delta x_{j-1} + \Delta x_j) \phi_j + \Delta x_j \phi_{j+1}) \tag{5.50}$$

so

$$n_{vj} = \frac{n_{lj}}{(T_{epi} - x_{dj}) \Delta y} \tag{5.51}$$

does not equal to N_D and the channel is not neutral. Then the channel cannot be represented by a single potential, as in Fig. 5.5, and the lumped equivalent circuit cannot accurately represent conditions inside the device.

Therefore, we have to be aware of the assumption made in calculating the charge Q_D on the depletion capacitor C_D. If the gradual channel approximation is valid, i.e., the gate is dominant, the calculation of Q_{Dj} is accurate. On the other hand, if the source and drain are dominant, the contribution due to Q_D is significantly smaller than the Q_j terms in (5.35), and the inaccurance introduced in calculating Q_D would not affect the calculation. When the Q_D term and the Q_j terms are comparable in magnitude, we might anticipate some error.

5.4.5 Simulation Results

The objective of the equivalent circuit model is to simulate both single domain oscillation and the contiguous domain oscillation. In the single domain mode, the image charge of the domain resides on source and drain, while in the contiguous domain mode, the image charge of the domain resides on the gate. In other words, the channel potential is controlled by the source and drain in the single domain mode, and controlled by the gate in the contiguous domain mode.

The equivalent circuit model for an RG-FET with ideal gate can be used to examine the effect of the oxide thickness on the oscillation mode. The thicker the gate oxide is, the further away the gate is from the channel, the greater control of the channel potential the source and drain have, and more likely the single domain mode oscillation will occur. On the other hand, as the gate oxide thickness is reduced, the contiguous domain oscillation will occur.

The following simulations are done for an RG-FET device of 10μm long and 2μm wide. The channel depth is 1500Å and the doping density is $1.2\times10^{17}cm^{-3}$. The difference between the effective metal workfunction and the electron affinity of the semiconductor $\Phi'_m - \chi'$ is 0.5eV and the bandgap energy is 1.36eV.

5.4.5.1 Gate Dominated Region (tox = 0)

When the gate oxide is zero, the device is an RG-MESFET. For a 10μm long device, a gate-to-gate voltage V_{GG} of 8V has to be applied to bias the channel into the negative mobility region. Fig. 5.7 shows the surface electron density $n_s=n_v*\Delta x$ distribution along the channel at various instants of time. A uniform electron density is assumed initially except in the middle of the channel where a dipole domain is introduced. Very quickly, random oscillation of electron density occurs in the channel. This oscillation travels toward the drain and as time evolves, the oscillation tends to stablize (Fig. 5.7(b), (c) and (d)). After approximately one device transit time $\tau = L/v_{avg}$ = 83ps (v_{avg} is typically 1.2×10^7 cm/s), the oscillation isstablizes, as seen from the flux vs. time plot taken in the middle of the channel (Fig. 5.8). The quasi-steady state electron density, electric field and potential distribution along the channel at time=100ps is shown in Fig. 5.9. In Fig. 5.9(a), contiguous domains of surface electron density are observed. The traveling velocity of the domain can be found by tracing the same domain at two different times, which is 1.3×10^7 cm/s for this case. The oscillation frequency is 100GHz, as determined from Fig. 5.8. As the electron density oscillates, the electric field and the potential also oscillate, as shown in Fig. 5.9(b) and (c).

The oscillation frequency and peak-to-peak amplitude depend on the biases when t_{ox}=0Å. $V_{SG} = V_{DG}$ values varying from 0 to 1.2V have been investigated, while V_{GG} is held at 8V. In Fig. 5.10, the simulation results from the equivalent circuit model (black dots) are superposed to the simulation results for an RG-MESFET from the TOF program (Fig. 3.9), and the two results are very similar, except at higher $1/n_s x_d$ values.

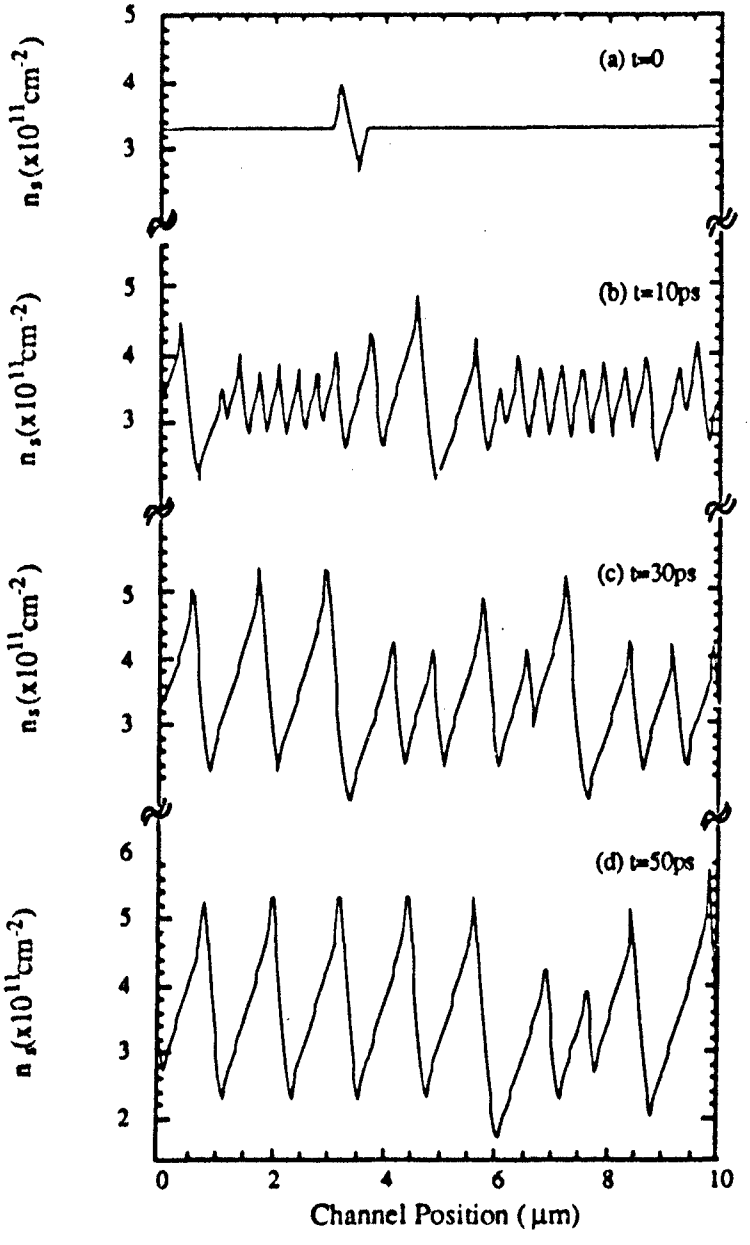


Figure 5.7 The time evolution of electron density in the channel of an RG-MESFET, biased at V_{GG}=8V, V_{G1}=0V, V_{SG}=0.8V, V_{DG}=0.8V.

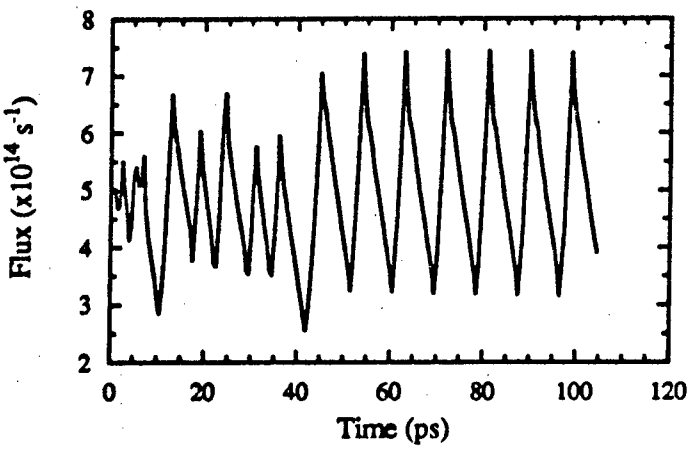


Figure 5.8 Flux vs. time for an RG-MESFET, biased at V_{GG}=8V, V_{G1}=0V, V_{SG}=0.8V, V_{DG}=0.8V.

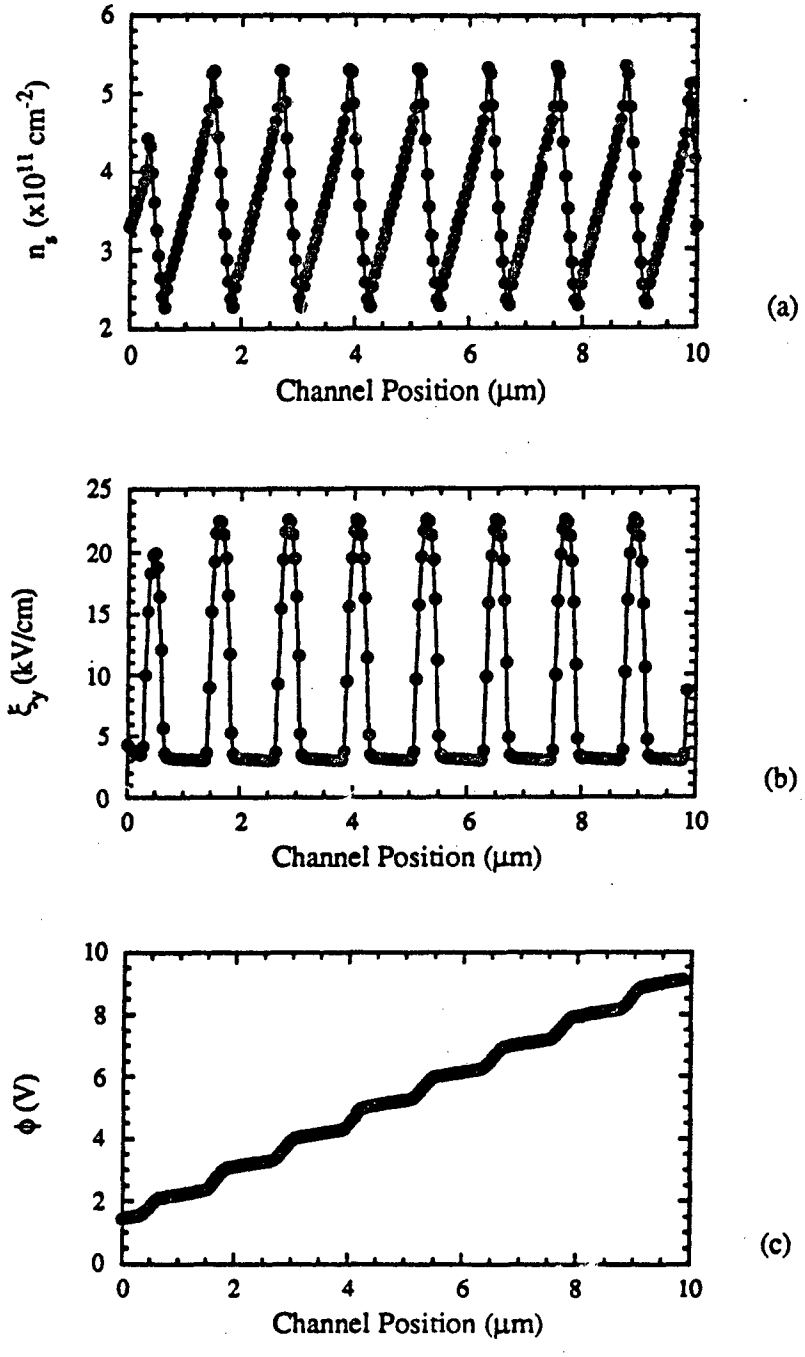


Figure 5.9 Simulation results ((a) n_s, (b) ξ_y, and (c) ϕ along the channel) at t=100ps for an RG-MESFET (t_{ox}=0) using the equivalent circuit model. Bias condition: V_{GG}=8V, V_{G1}=0V, V_{SG}=0.8V, V_{DG}=0.8V.

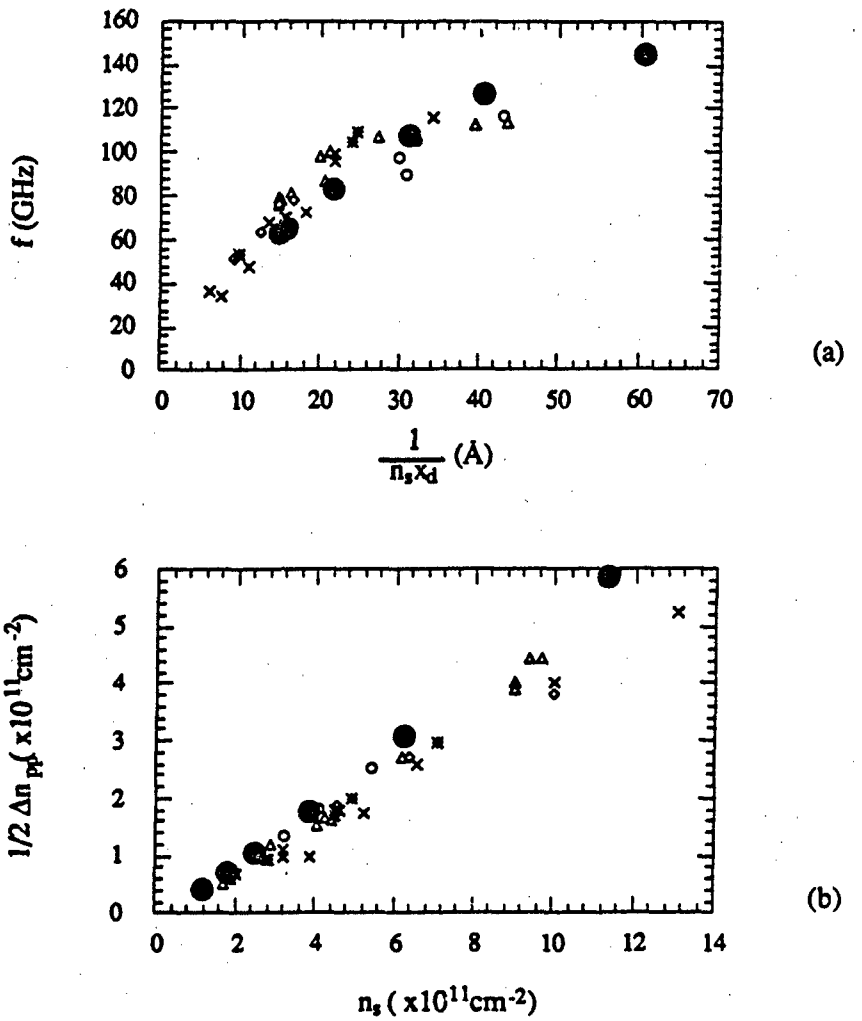
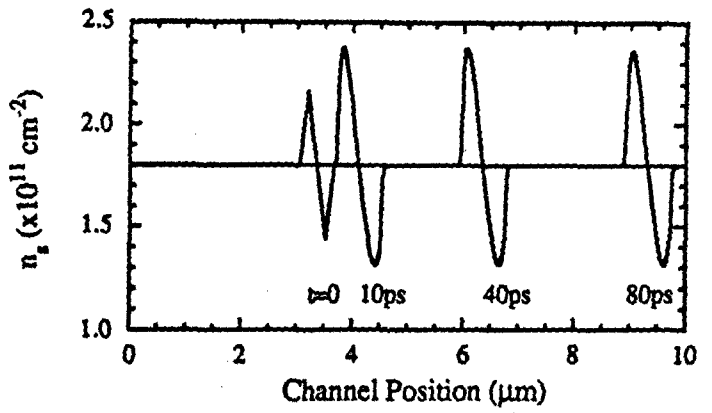


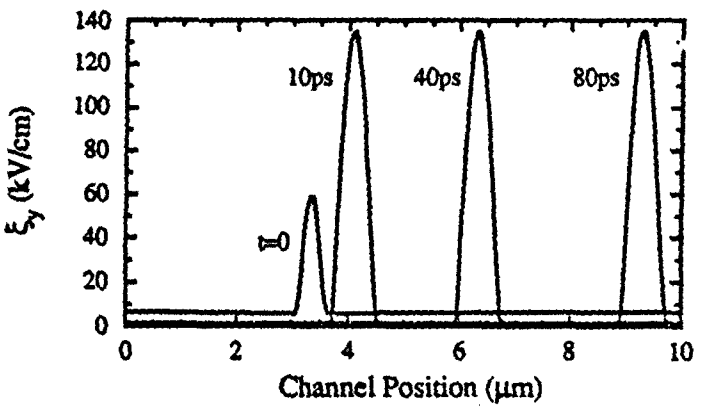
Figure 5.10 Comparison of simulation results using the equivalent circuit model (big black dots) with that of time-of-flight simulation (Fig. 3.9). (a) frequency. (b) amplitude.

5.4.5.2 Source/Drain Dominated Region (t_{ox} >> L)

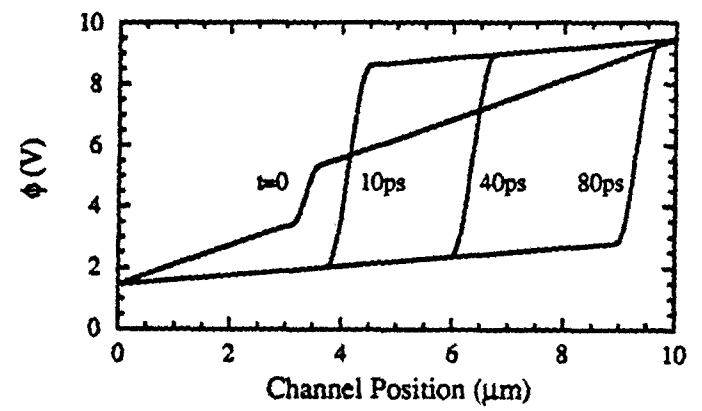
On the other hand, when t_{ox} = 600000Å, the gate is so far away from the channel that it can not influence the channel potential. The channel potential is soley determined by the source and the drain. Only the single domain oscillation is observed in this case. As seen in Fig. 5.11, the curves for t_{ox} = 600000Å are very similar to that of Gunn diode shown in Fig. 5.3. The domain travels with a velocity of about 7.5x10^6 cm/s.



(a)



(b)



(c)

Figure 5.11 Simulation resulats ((a) n_s, (b) ξ_y, and (c) ϕ along the channel) at different times for an RG-MOSFET (t_{ox}=600000Å) using the equivalent circuit model. Bias condition: V_{GG}=8V, V_{G1}=0V, V_{SG}=0.8V, V_{DG}=0.8V.

5.4.5.3 Intermediate t_{ox} Region

The simulation program, when run for intermediate t_{ox} values between 0 and 600000Å, exibits convergence problems. This may be due to the failure of the gradual channel approximation, as discussed in section 5.4.4. If the gradual channel approximation fails, the simple picture of the channel electrostatics given in Fig. 5.5 breaks down, and a more sophisticated modeling approach is needed. It is also possible that the convergence problems may simply be due to the numerical algorithms employed in the simulation. Further investigation of the intermediate t_{ox} region is beyond scope of the present thesis, but is an interesting area for future development.

5.5 Summary

The equivalent circuit model successfully simulates the RG-FET devices in the two extremes: $t_{ox}=0$ and $t_{ox}->\infty$. When the gate is placed very close to the channel, the channel potential is mainly determined by the gate voltage. Contiguous domain oscillation is obtained. On the other hand, when the gate is placed far away from the channel, the channel potential is mainly determined by the source and drain. Single domain oscillation is obtained. This general behavior is consistent with the available experimental results and with expectations based on physical intuition.

CHAPTER 6
CONCLUSION AND RECOMMENDATION

The resistive gate FET devices are unique in many aspects. By applying gate-to-gate voltage on the resistive gate, high and uniform electric field can be obtained. With the right gate sheet resistance, the gate can screen the space charge in the channel and contiguous domain oscillation can occur. This research project provides the unique opportunity to further understand the resistive gate FET devices both experimentally and theoretically.

Experimentally, the fabricated devices have been DC and microwave tested. Microwave oscillations are observed, but only in the single domain mode. Preliminary analysis indicates that the gate sheet resistance has to be reduced to about 3kΩ/square to obtain contiguous domain oscillation. Cermet deposition was investigated to obtain a desirable resistive film for future fabrication of CDO devices.

Theoretically, the steady state simulations of the long channel RG-FET devices with constant mobility have been performed. The results indicate that the operation of the RG-FET experiences three regions for positive current. They are divided by the uniform channel condition and the pinch-off condition. The pre-uniform region is solely caused by the non-zero V_{GG}. The post-uniform region and the pinch-off regions are very similar to the conventional FET's ohmic and pinch-off regions.

Transient simulations of RG-FET devices have also been performed. By combining the transferred electron effect in GaAs with the strong gate control of the channel potential, a series of contiguous electron packets can be generated, as indicated by the one dimensional computer simulations. High frequency oscillation in the GHz range can be obtained. The frequency can be tuned by changing the source to gate1 voltage.

To understand the single domain oscillation observed in experimental RG-MESFET devices, an equivalent circuit model was developed. Two modes of oscillation are obtained. When the gate is placed very close to the channel, the channel potential is mainly determined by the gate voltage, and contiguous domain oscillation is observed. On the other hand, when the gate is placed far away from the channel, the channel potential is mainly determined by the source and drain, and single domain oscillation is observed.

There are still many questions to be answered. The future work should consist of two parts. First of all, new devices should be fabricated with reduced gate sheet resistance. The new devices should eliminate the resistive gate overlapping the source and drain region, so to eliminate the coupling between V_{GG} and V_{SG}. More test structures should be put on the die to better monitor the fabrication process.

The theoretical work is essential to further understanding of the device. Better approximation of the charge on the depletion capacitor C_D should be explored so the model can properly represent the channel when $n_v \neq N_D$ and simulate the intermediate t_{ox} values. Once this step is finished, the equivalent circuit model should be extended to include the resistive gate effect. The finite resistance of the resistive gate tends to alter the gate field, thus alter the electric field in the channel. Upon finishing the resistive gate part, the theoretical work would come to a logical conclusion.

A full 2D simulation program might be needed to correctly model the RG-FET device. However, the commercially available 2D device simulator PISCES also has convergence problems when dealing with the nonlinear velocity-field curve of GaAs.

Appendix A

General Channel Potential Expressions for MOS Structure Using Green's Function

This appendix calculates the channel potential of MOSFET using Green's function[20]. Upon appropriate approximation, it gives the potential in the channel as well as the non-local potential correction.

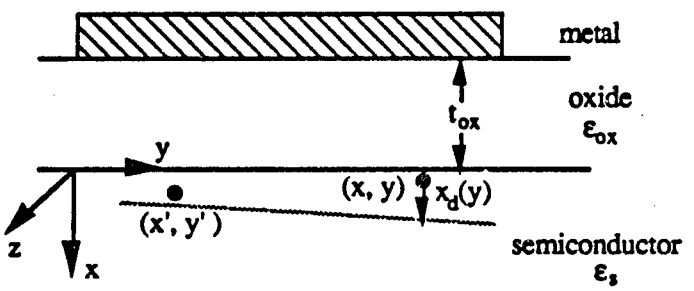


Figure A-1 MOS system. The potential at any point in the semiconductor (x,y) due to a line charge parallel to the z axis at (x',y') is calculated using the method of image.

Consider a MOS structure as shown in Fig. A-1. The potential at any point (x,y) in the semiconductor region (with dielectric constant ε_s) due to a linear charge of unit strength, i.e., 1C/cm, at a point (x',y') parallel to the z-axis can be calculated by the method of images:

$$G(x,y,x',y') = \frac{-1}{4\pi\varepsilon_s}\left\{\frac{\varepsilon_s-\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\ln[(y-y')^2+(x+x')^2]+\ln[(y-y')^2+(x-x')^2]\right\}$$
$$+\frac{\varepsilon_{ox}}{\pi(\varepsilon_s+\varepsilon_{ox})^2}\sum_{m=1}^{\infty}\left(\frac{\varepsilon_s-\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\right)^{m-1}\ln[(y-y')^2+(x+x'+2mt_{ox})^2] \qquad (A\text{-}1)$$

where t_{ox} is the oxide thickness. This potential function is the Green function solution of the two-dimensional Poisson equation of the structure. The metal plane is assumed at

ground potential. Since the boundary conditions at both the insulator-semiconductor interface and insulator-metal interface should be satisfied, an infinite series of image charges are required to calculate the potential function in each region.

Define:

$$C_0 = \frac{\varepsilon_{ox} - \varepsilon_s}{4\pi\varepsilon_s(\varepsilon_s+\varepsilon_{ox})} \tag{A-2a}$$

$$C_m = \frac{\varepsilon_{ox}}{\pi(\varepsilon_s+\varepsilon_{ox})^2}\left(\frac{\varepsilon_s-\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\right)^{m-1} = \frac{\varepsilon_{ox}}{\pi(\varepsilon_s+\varepsilon_{ox})^2}\, q^{m-1} \tag{A-2b}$$

$$a_m = x + x' + 2mt_{ox} \tag{A-2c}$$

Eqn (A-1) can be simplified as:

$$G(x,y,x',y') = \frac{-1}{4\pi\varepsilon_s}\ln[(y-y')^2 + (x-x')^2] + \sum_{m=0}^{\infty} C_m \ln[(y-y')^2 + a_m^2] \tag{A-3}$$

When y' approaches infinity, the potential should be zero. In (A-3), all nature log functions approach infinity at the same rate. The sum of the coefficients can be proven to be zero. i.e:

$$\sum_{m=0}^{\infty} C_m = \frac{1}{4\pi\varepsilon_s} \tag{A-4}$$

Physically, it means that the sum of the real charge and all the image charges is zero.

Appendix B

Electrostatics of the RG-MOSFET

Assuming a MOSFET structure with oxide thickness t_{ox}, substrate (p-type) doping N_A. The surface potential at any surface point (0,y) in a MOSFET is simply the sum of ideal gate voltage V_G', the potential due to the inversion charge and the potential due to the bulk charge (refer to Fig. A-1):

$$\psi_s(y) = V_G'(y) + \int_{-\infty}^{\infty} G(0,y,0,y')(-qn_s(y'))dy' + \int_{-\infty}^{\infty} dy' \int_{0}^{x_d(y')} G(0,y,x',y')(-qN_A)dx' \tag{B-1}$$

where $x_d(y')$ = depletion layer thickness defined by the implicit relationship:

$$\psi_s(x_d,y) = V_G'(y) + \int_{-\infty}^{\infty} G(x_d,y,0,y')(-qn_s(y'))\, dy' + \int_{-\infty}^{\infty} dy' \int_{0}^{x_d(y')} G(x_d,y,x',y')(-qN_A)\, dx' = 0 \tag{B-2}$$

If $n_s(y')$ and $x_d(y')$ are taken to be constants, $n_s(y')$ in second term can be taken out of the integral and the integration with respect to x' and y' can be interchanged in third term. It can be shown that (Appendix D)

$$\int_{-\infty}^{\infty} G(x,y,x',y')\, dy' = \frac{x'}{\varepsilon_s} + \frac{1}{C_{ox}} \qquad x > x'$$

$$= \frac{x}{\varepsilon_s} + \frac{1}{C_{ox}} \qquad x < x' \tag{B-3}$$

Eqn (B-1) and (B-2) become

$$\psi_s = V_G'(y) - \frac{qn_s(y)}{C_{ox}} - \frac{qN_A x_d}{C_{ox}} \tag{B-4}$$

$$V_G'(y) - \frac{qn_s(y)}{C_{ox}} - \frac{qN_A x_d}{C_{ox}} - \frac{qN_A x_d^2}{2\varepsilon_s} = 0 \tag{B-5}$$

Solving x_d from Eqn (B-5), Eqn (B-4) becomes:

$$\psi_s(y) = V_G'(y) - \frac{qn_s(y)}{C_{ox}} + V_0 - \sqrt{V_0^2 + 2V_0\left(V_G'(y) - \frac{qn_s(y)}{C_{ox}}\right)} \tag{B-6}$$

which is exactly the same as the one-dimensional solution of the Poisson equation using the depletion approximation for the MOS structure[9]. Here

$$V'_G(y) = V_G(y) - V'_{FB} = V_{G1} + V_{GG}\frac{y}{L} - V_{FB} \tag{B-7}$$

$$V_0 = \frac{qN_A\varepsilon_s}{C_{ox}^2} \tag{B-8}$$

Since the surface charge in the channel of a real MOSFET is not a constant, the non-local potential correction is:

$$\Delta\psi_s(y) = -q\int_{-\infty}^{\infty} G(0,y,0,y')\,(\,n_s(y') - n_s(y)\,)\,dy'$$

$$= \frac{q}{2\pi(\varepsilon_s+\varepsilon_{ox})}\int_{-\infty}^{\infty}\left(\ln(y-y')^2 - \frac{2\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\sum_{m=1}^{\infty}\left(\frac{\varepsilon_s-\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\right)^{m-1}\ln[(y-y')^2+4m^2t_{ox}^2]\right)$$

$$(\,n_s(y') - n_s(y)\,)\,dy' \tag{B-9}$$

This is accurate so long as the variation in the depletion width is neglected (the depletion width x_d is pinned once the MOSFET enters the inversion region).

Appendix C

Electrostatics of the RG-MESFET

The MES structure has no oxide underneath the gate and there is a doped channel with doping density of N_D and channel depth T_{epi}. Before the channel is pinched off, the cross section of this RG-MESFET can be viewed as a Schottky diode in series with an n^+p junction diode (as shown in Fig. C-1). The electrons fill up in between the two diodes with a volume density equal to the channel doping N_D.

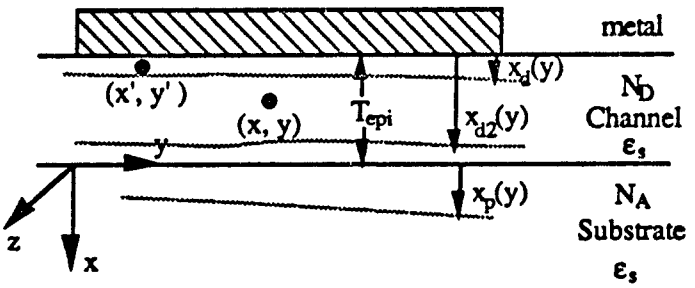


Figure C-1 MES system. The potential at any point in the channel (x,y) due to a line charge parallel to the z axis at (x',y') is calculated using the method of image.

The Green function for a MES structure can be obtained by setting $\varepsilon_s=\varepsilon_{ox}$ and $t_{ox}=0$ in Eqn (A-1) of Appendix A:

$$G(x,y,x',y') = \frac{-1}{4\pi\varepsilon_s}\left[\ln[(y-y')^2+(x-x')^2] - \ln[(y-y')^2+(x+x')^2]\right] \qquad \text{(C-1)}$$

The sum term in Eqn (A-1) is eliminated for there is only on image for each line charge.

The channel potential is the sum of the ideal gate voltage V'_G and potential due to the depleted channel and substrate:

$$\Psi_{ch}(y) = V'_G(y) + \int_{-\infty}^{\infty} dy' \int_{0}^{x_d(y')} G(x',y',x,y)\, qN_D dx'$$
$$+ \int_{-\infty}^{\infty} dy' \int_{x_{d2}(y')}^{T_{epi}} G(x',y',x,y)\, qN_D dx' + \int_{-\infty}^{\infty} dy' \int_{T_{epi}}^{T_{epi}+x_p(y')} G(x',y',x,y)(-qN_A) dx' \quad \text{(C-2)}$$

where

$$V'_G = V_G - \Phi_{Bn} \quad \text{(C-3)}$$

Φ_{Bn} is the barrier height of the Schottky diode, and $x_d(y')$ the depletion layer thickness of the Schottky diode. $x_{d2}(y')$ and $x_p(y')$ are the depletion width of the channel-substrate junction diode.

If $x_d(y')$, $x_{d2}(y')$ and $x_p(y')$ are constants independent of y', i.e. charge in the channel are uniform across the channel, the integration with respect to y' and x' can be interchanged. Using Eqn (B-3), Eqn (C-2)) becomes:

$$\Psi_{ch}(y) = V'_G(y) + \frac{qN_D}{2\varepsilon_s} x_d^2 + \frac{qN_D}{\varepsilon_s} x(T_{epi} - x_{d2}) - \frac{qN_A}{\varepsilon_s} x x_p$$
$$= V'_G(y) + \frac{qN_D}{2\varepsilon_s} x_d^2 \quad \text{(C-4)}$$

The last two terms cancel each other due to the fact that the negative charge in the substrate must be equal to the positive charge in the channel for the channel-substrate junction:

$$N_D(T_{epi} - x_{d2}) = N_A x_p \quad \text{(C-5)}$$

Surface electron density is defined to be:

$$n_s(y) = N_D(T_{epi} - x_d(y) - x_{d2}(y)) \quad \text{(C-6)}$$

By solving Eqn (C-5), (C-6) together with

$$\Psi_{ch}(T_{epi}+x_p) = V'_G(y) + \int_{-\infty}^{\infty} dy' \int_{0}^{x_d(y')} G(x',y',T_{epi}+x_p,y)\, qN_D dx'$$
$$+ \int_{-\infty}^{\infty} dy' \int_{x_{d2}(y')}^{T_{epi}} G(x',y',T_{epi}+x_p,y)\, qN_D dx'$$

$$+\int_{-\infty}^{\infty} dy' \int_{T_{epi}}^{T_{epi}+x_p(y')} G(x',y',T_{epi}+x_p,y)\,(-qN_A)\,dx' = 0 \tag{C-7}$$

x_d is found:

$$x_d = \frac{N_D+N_A}{N_D} t' + \sqrt{\left(\frac{N_D+N_A}{N_D}\right)^2 t'^2 - \frac{N_D+N_A}{N_D} t' + \frac{2\varepsilon_s N_A}{qN_D^2} V_G'} \tag{C-8}$$

where

$$t' = T_{epi} - \frac{n_s}{N_D} \tag{C-9}$$

For a semi-insulating substrate, N_A=0, the channel potential is:

$$\psi_{ch}(y) = V_G'(y) + \frac{qN_D}{2\varepsilon_s}\left(T_{epi} - \frac{n_s(y)}{N_D}\right) \tag{C-10}$$

The non-local potential correction is caused by non-uniform charge in the channel (position dependent $x_d(y)$, $x_{d2}(y)$ and $x_p(y)$). Still assuming that the doping in the substrate is zero, i.e., $x_{d2}(y)=T_{epi}$, the non-local potential will only arise from the variation in $x_d(y)$. Mathematically,

$$\Delta\psi_{ch}(x,y) = qN_D \int_{-\infty}^{\infty} dy' \int_{x_d(y)}^{x_d(y')} G(x,y,x',y')\,dx' \tag{C-11}$$

The integration with respect to x' and y' can no loner be interchanged. The integration with respect to x' is:

$$\begin{aligned}\int_{x_d(y)}^{x_d(y')} G(x,y,x',y')\,dx' = \frac{-1}{4\pi\varepsilon_s}\Big[& (x-x_d(y)) \ln\left((y-y')^2+(x-x_d(y))^2\right) \\ & - (x-x_d(y')) \ln\left((y-y')^2+(x-x_d(y'))^2\right) \\ & - (x+x_d(y')) \ln\left((y-y')^2+(x+x_d(y'))^2\right) \\ & + (x+x_d(y)) \ln\left((y-y')^2+(x+x_d(y))^2\right) \\ & + 2|y-y'|\left(\tan^{-1}\frac{x-x_d(y)}{|y-y'|} - \tan^{-1}\frac{x-x_d(y')}{|y-y'|}\right. \\ & \left. - \tan^{-1}\frac{x+x_d(y')}{|y-y'|} + \tan^{-1}\frac{x+x_d(y)}{|y-y'|}\right)\Big]\end{aligned} \tag{C-12}$$

Appendix D

Proof of Equation (B-3)

Equation (B-3) in Appendix B is:

$$\int_{-\infty}^{\infty} G(x,y,x',y')\,dy' = \frac{x'}{\varepsilon_s} + \frac{1}{C_{ox}} \qquad x > x'$$

$$= \frac{x}{\varepsilon_s} + \frac{1}{C_{ox}} \qquad x < x' \tag{D-1}$$

where G(x,y,x',y') is expressed in Eqn (A-3) of Appendix A, repeated here:

$$G(x,y,x',y') = \frac{-1}{4\pi\varepsilon_s} \ln[(y-y')^2 + (x-x')^2] + \sum_{m=0}^{\infty} C_m \ln[(y-y')^2 + a_m^2] \tag{D-2}$$

with

$$C_0 = \frac{\varepsilon_{ox} - \varepsilon_s}{4\pi\varepsilon_s(\varepsilon_s+\varepsilon_{ox})} \tag{D-3a}$$

$$C_m = \frac{\varepsilon_{ox}}{\pi(\varepsilon_s+\varepsilon_{ox})^2}\left(\frac{\varepsilon_s-\varepsilon_{ox}}{\varepsilon_s+\varepsilon_{ox}}\right)^{m-1} = \frac{\varepsilon_{ox}}{\pi(\varepsilon_s+\varepsilon_{ox})^2}\, q^{m-1} \tag{D-3b}$$

$$a_m = x + x' + 2mt_{ox} \tag{D-3c}$$

First let's calculate a simple integratin:

$$\int_{-\infty}^{\infty} \ln[(y-y')^2 + b^2]\,dy' = \int_{-\infty}^{y} \ln[(y-y')^2+b^2]dy' + \int_{y}^{\infty} \ln[(y-y')^2+b^2]dy'$$

$$= 2\int_0^{\infty} \ln[u^2+b^2]\,du$$

$$= \left[\, 2u\ln(u^2+b^2) - 4u + 4|b| \tan^{-1}\frac{u}{|b|} \,\right]_{u=0}^{u=\infty} \tag{D-4}$$

Apply Eqn (D-4) to (D-2):

$$\int_{-\infty}^{\infty} G(x,y,x',y')dy' = \frac{-1}{4\pi\varepsilon_s}\left[\, 2u\ln[u^2+(x-x')^2] - 4u + 4|x-x'| \tan^{-1}\frac{u}{|x-x'|} \,\right]_{u=0}^{u=\infty}$$

$$+ \sum_{m=0}^{\infty} C_m \left[\, 2u\ln(u^2+a_m^2) - 4u + 4a_m \tan^{-1}\frac{u}{a_m} \,\right]_{u=0}^{u=\infty} \tag{D-5}$$

Note that when y' approaches infinity, all mature log functions approach infinity at the same rate. Using Eqn (A-4) of Appendix A, (D-5) becomes:

$$\int_{-\infty}^{\infty} G(x,y,x',y')dy' = \frac{-1}{4\pi\varepsilon_s}\left(2\pi\,|x-x'|\right) + \sum_{m=0}^{\infty} C_m[\,2\pi(x+x'+2mt_{ox})] \tag{D-6}$$

In the case of $x > x'$

$$\int_{-\infty}^{\infty} G(x,y,x',y')dy' = \frac{-1}{4\pi\varepsilon_s}(2\pi x - 2\pi x') + \sum_{m=0}^{\infty} C_m(2\pi x + 2\pi x' + 4\pi m t_{ox})$$

$$= \frac{x'}{\varepsilon_s} + 4\pi t_{ox}\sum_{m=0}^{\infty} mC_m \tag{D-7}$$

Since

$$\sum_{i=1}^{\infty} a_i\, q^i = \frac{a_1}{1-q}, \tag{D-8}$$

$$\sum_{m=0}^{\infty} mC_m = C_1 + 2C_2 + 3C_3 + \cdots$$

$$= \frac{\varepsilon_{ox}}{\pi(\varepsilon_s+\varepsilon_{ox})^2}\left[\sum_{m=1}^{\infty} q^{m-1} + \sum_{m=2}^{\infty} q^{m-1} + \sum_{m=3}^{\infty} q^{m-1} + \cdots\right]$$

$$= \frac{\varepsilon_{ox}}{\pi(\varepsilon_s+\varepsilon_{ox})^2}\left[\frac{1}{1-q} + \frac{q}{1-q} + \frac{q^2}{1-q} + \cdots\right]$$

$$= \frac{\varepsilon_{ox}}{\pi(\varepsilon_s+\varepsilon_{ox})^2}\frac{1}{1-q}\sum_{m=1}^{\infty} q^{m-1}$$

$$= \frac{\varepsilon_{ox}}{\pi(\varepsilon_s+\varepsilon_{ox})^2}\left(\frac{\varepsilon_s+\varepsilon_{ox}}{2\varepsilon_{ox}}\right)^2$$

$$= \frac{1}{4\pi\varepsilon_{ox}} \tag{D-9}$$

Therefore,

$$\int_{-\infty}^{\infty} G(x,y,x',y')dy' = \frac{x'}{\varepsilon_s} + \frac{t_{ox}}{\varepsilon_{ox}} = \frac{x'}{\varepsilon_s} + \frac{1}{C_{oc}}$$

Case for $x < x'$ can be obtained in a similar way.

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