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FABRICATION TECHNIQUES AND TECHNOLOGIES FOR MISSILE SEEKER MICROELECTRONIC COMPONENTS (FOCUSING ON MULTI-CHIP MODULE SUBSTRATE RELIABILITY)

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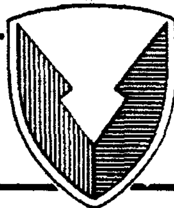

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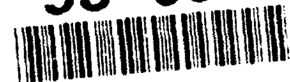

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In the report, recent multi-chip module (MCM) manufacturing technology developments are reviewed. MCMs represent an emerging technology which will provide the Army with high-speed processors for missile seekers in a more compact form than offered by previous generations of electronic packaging. Both ceramic (MCM-C) and deposited dielectric (MCM-D) forms are covered, including those incorporating polyimide and new polymer films. Recent literature is reviewed concerning manufacturing processes and the necessary generic types of equipment under development and in current practice. Promising developments include low-temperature cofired ceramics, polymer dielectrics with low absorptivity of water, new photo-definable polymers, new adhesion promoters, methods for gold thin-film metallization, laser ablation of vias, and controlled extrusion of polymer precursors. Reliability issues are emphasized in the review, particularly in respect of the severe environmental conditions experienced by missiles. A detailed review of the mechanisms of degradation is given. Recommendations are made concerning the need for micromechanical and electrical property measurements of candidate MCM materials.

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1. INTRODUCTION

This is a report of a study of multi-chip module (MCM) substrate technologies, focused on design, fabrication, and other manufacturing issues, particularly as they relate to the reliability of multi-chip modules. MCMs represent an emerging technology which is expected to provide the Army with high-speed processors for missile seekers in a more compact form than offered by previous generations of electronic packaging. By concentrating on MCM substrates, we are addressing a crucial and defining part of MCM technology (though by no means the only source of difficulty or concern). This report reviews recent literature which describes process technologies currently in use for ceramic (MCM-C) and deposited dielectric (MCM-D) forms of multi-chip modules. (Polyimide films have been commonly used for the dielectric in the latter type.) This establishes a context in which we discuss a number of reliability issues important in manufacturing MCM substrates. Special consideration is given to the severe conditions experienced by missile components when they are in storage and in use.

The roots of MCM technology go back forty years to developments of *hybrid* circuits. Such circuits were often realized as cofired ceramic substrates connecting a few small integrated circuits (bare die, or chips) and other electronic components. The purpose was to create integrated devices that for one reason or another could not be realized as single semiconductor integrated circuits at the time the hybrid circuits were designed. While multi-chip modules began with similar substrate technology, the thrust has been more on creating higher density electronics with higher performance, particularly in speed or bandwidth. Higher interconnection density has been achieved in MCM-C by increasing the number of interconnection layers in the ceramic substrates (up to several tens of layers). However, such a large number of layers is costly to produce. Furthermore, it is difficult to achieve good performance at the highest possible data rates (or switching frequencies) because of the relatively high dielectric constants in ceramics and the metallization technology used. As a result, other substrate technologies like MCM-D have been developed to gain additional performance with more affordable processes.

It is not in the scope of this report to provide a basic textbook on MCM technology. Two excellent recent volumes have been issued which serve this purpose [Messner et al. 1992] and [IPC 1992], as well as an earlier compendium [Johnson, Teng, Balde 1992]. There has been a tremendous outpouring of articles in the past year, primarily in conference proceedings. These will be surveyed here particularly as they relate to reliability issues.

While the number of recent publications attests to a high level of interest in MCMs, there is also considerable reassessment of the economic producibility of high density forms of this technology. A significant shake-out in the industry has begun with many companies closing or delaying further development and production of the technology. For some, there is a belief that it is better to wait for wafer scale integration. Others are concentrating on selecting the lowest-possible-cost options for high-density electronics technology necessary to meet selected high volume applications. At a minimum, this means selecting the particular processes and materials to use in MCM-C or -D with low cost as a primary driver. But some are postponing the application of MCMs and using (and extending the performance of) dense chip-on-board technology; i.e., bare IC die directly bonded to circuit boards. This is essentially similar to the related multi-chip module type MCM-L (outside the scope of this report) which uses laminated polymer boards as substrates. These trends in commercial industry may not directly meet DoD needs for high reliability. However, the establishment of viable high-volume applications of high-density electronics will contribute to the industrial infrastructure necessary to support MCMs in general [Balde 1992], and will ultimately support design and production for DoD needs.

In the following three sections, we will describe the most common structural and materials options in MCM-C and MCM-D substrates and the associated manufacturing processes. Then we turn to underlying reliability issues.

2. MANUFACTURING CERAMIC SUBSTRATES (MCM-C)

In MCM-C substrates, the insulating ceramic (or similar) material is strong enough to establish the basic mechanical rigidity of the overall structure. When the electrical and cost performance of MCM-Cs are acceptable, they are often considered a higher reliability option (than MCM-D in the present state of technology) because the structure and its interfaces are more robust. Multilayer MCM-Cs are most frequently cofired, but some conventional thick film substrates are also made.

2.1. Cofired and Conventional Thick Film

Ceramic substrate layers are usually tape cast. The term cofiring refers to processes where green (i.e., unfired) tapes are metallized and stacked in the green state and then fired together. In conventional thick film processes, each ceramic layer is printed and added to the stack green and fired before the next green layer is added. Then these steps are repeated.

Green ceramic tapes are made in sizes up to a few hundred mm square and in thicknesses from around 2 mm down to 0.1 mm in thickness [Schroeder 1992]. More than 60

metallized layers have been stacked and included in a substrate [Francis and Jardine 1992]. Many applications of this technology are implemented with far fewer layers, however.

Alumina and beryllia have been commonly used [IPC 1992] in cofired substrates which are fired at around 1500 °C. These are the basis of so-called High Temperature Cofired Ceramics (HTCCs). Tungsten or molybdenum/manganese metallizations are typical [Bhedwar and Sawhill 1989]. These are applied as screen printed or extruded metal pastes. Preferred minimum conductor widths are in the range 0.1-0.2 mm [IPC 1992] based on screen printing technology, the particle sizes of metallization pastes, alignment accuracy, and the uniformity of layer shrinkage during firing.

2.2. Low Temperature Cofired Ceramics

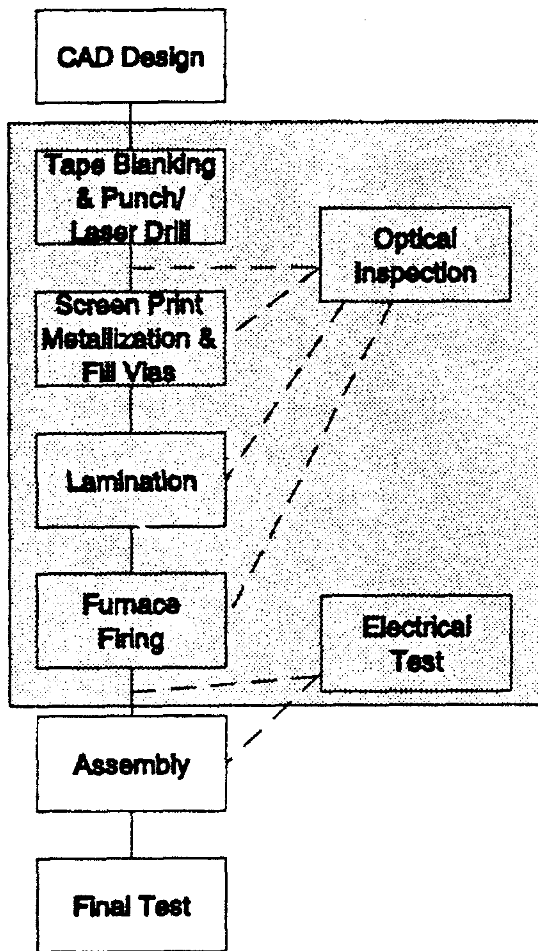
New, alternative low-temperature tapes are made from glass-filled ceramics and fired at 850-950 °C. Higher conductivity metals can be used like gold, platinum gold, palladium gold, silver, platinum silver, palladium silver, palladium platinum silver, copper, and nickel [IPC 1992; Francis and Jardine 1992]. Advantages of Low-Temperature Cofired Ceramics (i.e., LTCCs, vs. HTCCs) include

- Higher electrical conductivity signal lines which reduces line loss;
- Lower dielectric constant (around 5 vs. 10 for HTCC) resulting in higher speed circuits;
- A better match (in some cases) to the coefficient of thermal expansion (CTE) of silicon chips; and
- Processing which is simpler, smaller-scale, and lower cost.

Disadvantages include [Schroeder 1992] lower mechanical strength and lower thermal conductivity for dissipating heat. However, Schroeder [1992] has shown that a test LTCC MCM 46 mm square can survive MIL-STD-883 tests for susceptibility to 10,000 g acceleration, -65 °C to 150 °C temperature cycle, 1500 g shock, and 20-2,000 Hz vibration.

2.3. Manufacturing Processes

A definitive and extensive summary of MCM-C cofired processes, which have been well established for more than a decade, is given by Bhedwar and Sawhill [1989] to which the reader is referred. The following reviews the high points of this account, with the principal steps outlined in Figure 1a.



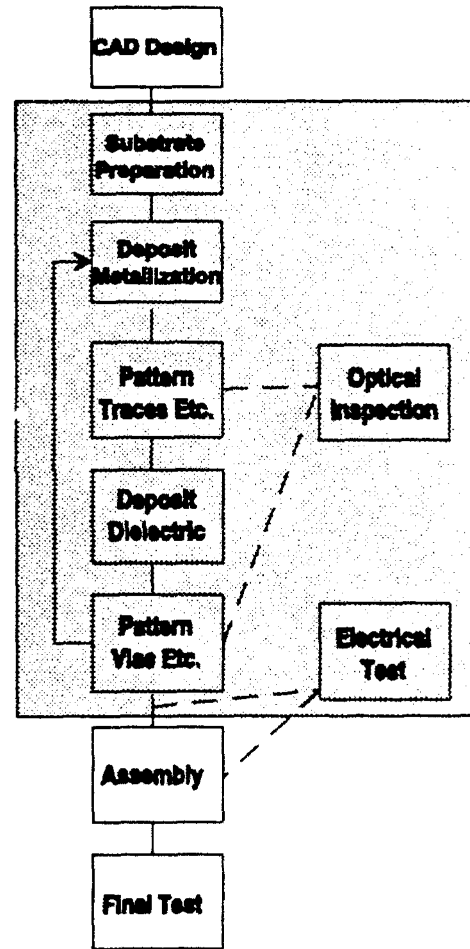


Figure 1. Typical Outline for a) MCM-C and b) MCM-D (Chips Last) Manufacturing Processes. Shaded portions apply to substrate manufacture.

2.3.1. Blanking, Punching, Drilling

Tapes of green ceramic are first removed from the polyester film carrier on which they were tape cast. They are cut to size by a blanking punch and die which also creates registration holes which will be used for alignment later in the lamination stage.

Via holes are made next, either for electrical inter-layer connection or for thermal conduction. These are either punched or laser drilled, typically with a CO_2 laser. Electrical vias are made in diameters down to about 100 - 200 μm [Bhedwar and Sawhill 1992; Schroeder 1992].

2.3.2. Printing

Metallizations are usually screen printed, but occasionally written with an extruding nozzle moved relative to the tape. (Design rules are covered in [IPC 1992].) Conductive pastes comprise about

- 50-70 wt% metal particles,
- 2-10 % glass frits or 1-5 wt% fluxes for binding to the ceramic, and
- 12 to 25 wt% in organic vehicles which facilitate printing.

Via fill pastes are similar but higher in metal content and are separately screen printed. Slightly concave fills are desirable to avoid trouble in later steps.

During printing, the substrate is vacuum held to a printing stage. After each printing step, the substrate is dried.

Optional thick film resisters can be printed from pastes with selected conductivities. They can later be laser trimmed, if necessary, if they are located on or near top layers of the eventual stack.

Optical inspection is used to verify that conductors are accurately sized and located within the tolerances allowed by conductor widths, i.e. to less than 100 μm.

2.3.3. Lamination

Since tapes shrink by slightly different amounts in the machine and transverse tape directions, the orientation of printing is planned so that alternate layers in the stack will have orthogonal machine directions. This gives a more uniform shrinkage in the x- and y-directions. Each layer in the stack is placed on a pressing die whose locating pins mate with the tape's registration holes. Cavity walls constrain the edges of the tape from expanding during pressing. The lamination pressure affects the degree of shrinkage experienced later in

firing, typically around 10-12%. Artwork must be planned allowing for this shrinkage. Following lamination, the stack can be trimmed to size by a variety of methods.

2.3.4. Firing

Firing actually involves two processes: burnout of organic filler in both tape and metallization, and then sintering. The first stage is accomplished at around 350 °C for LTCCs and 500 °C for HTCCs; the second, around 850 °C, and 1500 °C, respectively. LTCCs and HTCCs and their different metallizations require different controlled-gas atmospheres at different stages in the heating cycles. (Refer to [Bhedwar and Sawhill 1989] for details.) Some LTCC processes can be done in air, reducing complexity and cost. After cofiring, the upper layer metallization (and optional overglazing) can be printed and fired. This metal is often built up by plating to make robust pads for connection to chips and external circuits.

2.4. Other Developments

Other materials are under investigation because they have improved CTEs relative to silicon and/or improved thermal conductivity. These include aluminum nitride, silicon carbide, cordierite, and mullite [e.g., Sigliano and Gaughan 1992].

Occasionally, developers have extended the performance of MCM-C substrates by topping them with a few layers of polyimide-insulated thin-film metallization for higher density or higher frequency signal lines [e.g. Collander et al. 1992], in effect, merging the MCM-C and MCM-D technologies. Then the ceramic layers can be devoted to ground, power, and perhaps I/O pads.

A tape transfer method has also been described in which separately fired ceramic layers are bonded together by a tape layer with carefully chosen mechanical properties. It has been possible to have some of the best of both LTCC and HTCC technology and to attain higher resolution signal traces [Danner 1992].

3. MANUFACTURING DEPOSITED DIELECTRIC SUBSTRATES (MCM-D)

3.1. Chips Assembled Last

MCM-D technology was begun later than MCM-C and is now receiving the most developmental attention. Archetypal MCM-Ds are made on a rigid base, often silicon, with the steps outlined in Figure 1b. Thin dielectric and thin-film interconnection layers are deposited on top of the base. Then chips are attached *last* to the upper layer metallization by TAB, by flip-chip soldering (or conductive epoxies), or by wire bonding. A typical MCM-D

has a ground layer, power layer, *only two* signal layers, and an I/O pad layer, as shown in Figure 2. Signal layers with much higher density interconnects can be made, so such MCM-D devices can often be designed to perform the same function as a thirty-layer MCM-C; approximately an order-of-magnitude narrower, finer-pitch traces can be achieved in MCM-D. Since these devices have substantially fewer layers, they cost less to make. Good overviews of this technology are given by Balde [1989] and by Garrou and Turlik [1992].

3.1.1. Base Materials

Issues in the choice of base material include

- Coefficient of Thermal Expansion (CTE) matching;
- Thermal conductivity for efficient heat sinking;
- Flatness, (the ability to be polished flat) to facilitate subsequent lithography; and
- Mechanical rigidity and robustness.

There are other issues depending on the application. The electrical conductivity of the base can matter if metallization is to be applied directly. There must be chemical compatibility between the base and other materials used in the MCM and in processing.

Silicon is probably the most popular material for the rigid base because of the obvious good match in CTE with silicon chips used in the module. Because the interconnection layers are thin, some describe such MCMs as silicon on silicon, although this is something of a misnomer. The heat conductivity of silicon is acceptably high. Silicon's other advantage is that it can be polished to good planarity necessary for high resolution lithographic processing of subsequent layers. However, it is both brittle and apt to bend when bonded to dielectrics with significantly different CTEs [Balde 1989]. As a result, it is sometimes bonded to a reinforcing CTE-matched substrate like aluminum nitride.

Ceramics like aluminum nitride and silicon carbide have appropriate CTEs and sufficient thermal conductivity for base materials [Balde 1989]. Ceramics often require a coating to be applied in order to get the required flatness for lithography.

Metals and insulator-coated metal cores have been used either where the environment is especially mechanically stressful or where heat sinking demands are high. Examples of metals used include steel, copper, copper-clad Invar, and Inconel, [IPC 1992]. Since these bases often have a poor CTE match with other materials in the MCM, special attention is given to intermediate layers offering some degree of compliance or controlled slippage [Balde 1989]. In other cases, the metal structures are engineered to have a tolerable CTE [Garrou and Turlik 1992].

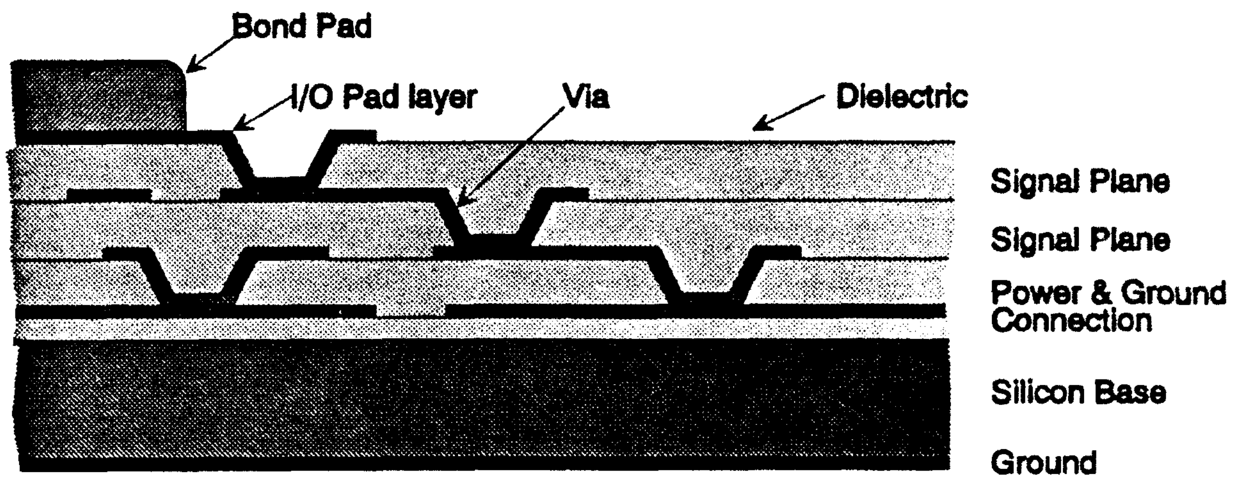


Figure 2. Typical MCM-D Substrate for Chips Assembled Last

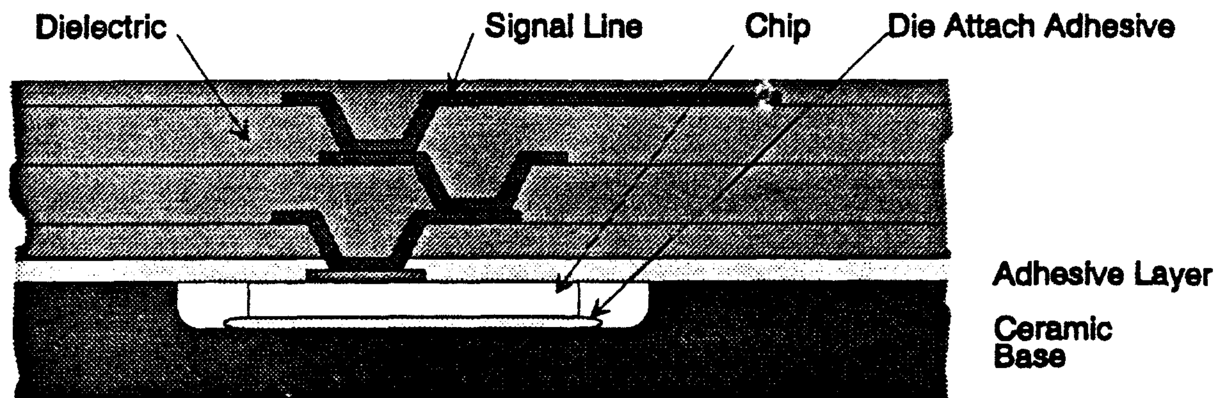


Figure 3. GE HDI Structure for Chips Assembled First

3.1.2. Dielectric Insulators

Two of the most popular insulator materials have been silicon dioxide and polyimide. Considerations in choosing a dielectric include:

- Dielectric constant well matched to the frequency performance expected;
- High thermal conductivity and resistance to thermal degradation during processing and use;
- Matching coefficient of thermal expansion (CTE) and low elastic modulus, which affect interactions with adjoining materials when temperatures change;
- Good planarity (the ability to keep a flat upper surface) to facilitate lithography;
- Good adhesion (and chemical compatibility) between the dielectric and metallization; and
- Low absorption of water.

As one can see from this list, many of these issues are interfacial and depend as much as the other materials and the processes used as on the intrinsic properties of the dielectric. The perfect dielectric has yet to be found.

Silicon dioxide is easily deposited on silicon and is often a lower-cost option than competing polymeric coatings [Kohl 1992]. Around 10 µm thick layers are typically used [Balde 1989; Marella and Tuckerman 1992]. The CTE is better matched to silicon than many alternatives. Aluminum adheres well but problems with copper and gold have inhibited widespread acceptance [Balde 1989]. More will be said about such problems in the next section. It has also been said that silicon dioxide takes up water which affects its dielectric constant [Balde 1989], but high quality material is not as prone to this problem as popular polymers like polyimide. Silicon dioxide does not readily give good top-surface planarity.

Polyimide (PI) films are known for their resistance to thermal degradation and have become the most common polymeric insulators in MCM-D. They are typically applied by spin coating and thermal curing [Balde 1989]. Preferred thicknesses are around 25 µm. Photodefinable PIs are also known [e.g., Schuckert and Fox 1990; Nader et al. 1992] which can, in principle, reduce processing in steps defining vias.

While PIs can be metallized with copper, as well as with aluminum, adhesion is problematic. Sputtering of the metal [Pertsin and Pashunin 1991] and ion bombardment (or similar treatment) before or after metallization [Ruoff et al. 1988; Bachmann and Vasile 1988; Koh et al. 1990; Murali et al. 1992] has been shown to improve conditions thought favorable for adhesion. However, processes like this may have the unfortunate side effect of promoting reactions between PI and copper (particularly) that can adversely affect the dielectric constant

and high frequency performance of signal lines. In addition, residual polyamic acid (from the formation of the PI) can cause corrosion [Balde 1989; Garrou and Turlik 1992]. For that reason copper is often protected by cladding with other metals (e.g., Ni, Cr, Ti) which inhibit reactions and corrosion [Balde 1989; Garrou and Turlik 1992; Shan et al. 1992]. Adema et al. [1990] suggest that nickel and chromium together are more effective than chromium cladding alone in avoiding the formation of copper precipitates in PI. However, they also show that Ni adversely affects line resistivity and high frequency performance. Zhang et al. [1990] have also shown the effectiveness of Ti in avoiding copper diffusion into PI. It is also believed that titanium on copper promotes its adhesion to polyimide.

A further problem with PI is in getting a flat surface when the PI covers a raised metal feature [Balde 1989]. Making additional coatings to make it flatter adds cost.

Moisture absorption in PI is a triple problem. PI can absorb up to around 3% of its weight in water under conditions of relative humidity above 50% and room temperature [Shan 1992]. This not only directly affects the dielectric constant adversely, but it also promotes reaction between the PI and copper metallization *and* causes expansion of the polyimide and unwanted mechanical stress. New polyimides are being developed with much less water absorption (< 1 wt%) [Nader et al. 1992].

Alternative dielectrics are being investigated which have much lower water uptake. One such is a silica-powder-filled polytetrafluoroethylene (PTFE or Teflon®) with a moisture absorption of 0.07% [Arthur et al. 1992]. It has a lower dielectric constant, 2.6 to 2.8 as compared with 3.5 to 4 for PI, and is said to have better copper adhesion. Another promising material is benzocyclobutene (BCB) which has similar water absorptivity and dielectric constant (2.8). A nice feature is that it also gives good planarity [Burdeaux et al. 1990]. A number of other polymers is reviewed in [Garrou and Turlik 1992]. Finally, there have been recent reports that polyquinoline has similar properties to BCB in respect of moisture absorption [Hendricks et al. 1991].

3.1.3. Metallization Materials

Desirable properties in a metallization material include

- High conductivity;
- Low cost;
- Availability of good deposition process(es);
- Good adhesion;
- Bondable, preferably by multiple methods; and
- Resistant to corrosion by adjacent materials and by manufacturing processes.

Patterned metallizations provide power, ground, and signal traces as well as interlayer vias. Processes for patterning, via formation, and deposition will be discussed in later sections. The principal metal candidates, aluminum, copper, and gold, have already been mentioned in the previous section. Table 1 compares their properties.

Table 1. Thin Film Conductors

	Aluminum	Copper	Gold
Resistivity 10^{-6} ohm cm [Garrou and Turlik 1992]	2.7	1.7	2.4
Cost	Low	Low	High >$400/oz.
Deposition processes	Evaporation Sputtering	Evaporation Sputtering Plating	Evaporation Sputtering Plating
Adhesion SiO_2 PI	 Good Fair	 Needs assistance Needs assistance	 Needs assistance Needs assistance
Bonding	Wire bonding Conductive epoxy	Soldering Conductive epoxy	Wire bonding Conductive epoxy
Corrosion resistance	Fair	Needs assistance	Good

Aluminum is popular for low cost and reasonable adhesion, but is generally applied to lower frequency systems because of its lower conductivity [e.g., Murali et al. 1992; Marella and Tuckerman 1992]. Copper is fairly low in cost and high in conductivity but has the problems with adhesion and corrosion already discussed.

Gold is receiving increased attention. Table 1 reflects conventional wisdom that it has significantly better conductivity than aluminum (as indeed it does in the bulk). However, gold and other metals which are deposited by standard thin-film processes often have higher resistivities which depend both on the method and on the substrate. Recent measurements by Darrow and Vilmer-Bagen [1992] show gold deposited by common techniques may have no better resistivity than aluminum.

Gold's clearer property of distinction is superior corrosion resistance. The latter eases concerns with chemical compatibility throughout the process cycle. It is often added by plating to upper layer metallization where bonding to chips and I/O occurs. Cost has often

been cited as a major concern limiting its wide-spread use in substrates, but process simplification may offset these costs. Potential savings relative to copper are in eliminating the need for additional corrosion layers. These directly affect cost through increased processing, and indirectly, through the potential for more problems with yield [Kohl 1992]. The critical missing link is a material to promote adhesion between gold and the dielectric layers. The conventional approach is to find a metal that readily forms oxides and adheres well both to the metallization material and to the dielectric. The problem with this is that it may be conductive and require patterning to match that of the conductor; i.e., additional expensive processing. However, Kohl [1992] has found a proprietary dielectric adhesion promoting agent (on which patent action is pending). Thus, patterning is not required and a reliable, cost-effective gold process may be achievable.

3.2. Chips Assembled First

A significantly different architecture was developed by General Electric [Eichelberger et al. 1988; Cole et al. 1992] (with DARPA funding) and later transferred to Texas Instruments. GE has dubbed the system the High Density Interconnect (HDI) technology. The arrangement, shown in Figure 3, features an alumina (or other satisfactory) substrate that is milled out with wells into which chips are mounted *first* with their interconnect pads on top. The chips are bonded to the alumina substrate with an adhesive which enhances the heat sinking function of the substrate. An adhesive layer is then laid down over the top of the chips and substrate, followed by a layer of polyimide. The connection of the first level metallization to the chip is then initiated by laser drilling through the adhesive and Kapton® polyimide, followed by sputtering and plating a Ti/Cu/Ti metal layer.

Successive layers can be formed by continued lamination of adhesive layers followed by polyimide layers, laser drilling, and metallization. On the other hand, other polymeric layers can be directly deposited successively after the first Kapton layer.

Since the chips are assembled first, disassembly for rework (in case of a bad chip) is a special challenge. In order to remove the interconnect overlay without loosening the adhesive that holds the chips to the substrate, the overlay adhesive must have a relatively low glass temperature (i.e., somewhat above 200 °C). Upper layer dielectrics and any further adhesives must be processed at temperatures below 200 °C. Cole et al. [1992] found that a sequence of polyimides directly deposited was preferable. Agarwal et al. [1992] have modeled and illustrated expected effects from humidity-induced stress. Unfortunately, BCB is not compatible with GE's repair scheme [Cole et al. 1992] because it has a processing temperature above 200 °C and is difficult to dissolve. Thus, it is not a suitable solution to humidity effects.

3.3. Manufacturing Processes

3.3.1. Depositions

Metallization

A recent study by Darrow and Vilmer-Bagen [1992] provides a good overview, and further details are given by Seraphim et al. [1989]. In addition to adhesion and metal thickness, film uniformity, stress, and microstructure are considerations.

Sputtering is often the technique of choice in thin-film metallization since it is one of the more energetic and thereby promotes adhesion to dielectric surfaces [e.g., Murali et al. 1992]. It is a vacuum deposition technique in which an energetic (usually argon) plasma is used to dislodge atoms from the cathode which are later deposited on the dielectric substrates near anode potential. The use of DC magnetrons has reduced problems with substrate heating and film uniformity. Process variables include deposition rate, deposition thickness, inert gas pressure (typically around 10^{-3} torr), and substrate bias. Inert gas can be trapped in a sputtered film, leading to voids and higher resistivity. Annealing will recrystallize the metal surface and release trapped gas.

Sputtering has the property that it can coat surfaces on the substrate that are nearly along the line of sight to the sputter source as well as those which are perpendicular [Turlik and Adema 1992]. Thus, there is good coverage of steps and via walls. Undercut vias can be a problem, however. If a thicker coating is needed on sidewalls, or if one wants to fill in vias with metallization, electroplating or electroless plating can be used.

Evaporation is carried out at a lower pressure (10^{-5} to 10^{-6} torr) and gives line-of-sight coverage from the source. It is less energetic than sputtering and thus gives less adhesion except where there is chemical affinity with the substrate. As a result, it is less used than sputtering. It can, however, be applied to lift-off patterning. Process improvements have come from better heating of the source material by electron beams [Seraphim et al. 1989]. However, the low temperatures of evaporative coatings tend to cause a columnar growth that shadows parts of the surface, leading to microvoids and other defects. As a result, resistivity can suffer [Danner and Vilmer-Bagen 1992].

Danner and Vilmer-Bagen [1992] have also described another vacuum technique called enhanced-ion-plating in which source atoms are ionized and drawn to the substrate near cathode potential. They make the case that this not only can promote adhesion but also can provide superior microstructure and conductivity. More application experience is needed.

Electroplating begins with a seed layer on which the plating will be grown. This is most often sputtered over the entire substrate as a thin film. If the electroplated layer is to be

patterned, then the seed layer must also be patterned, as will be described in the next section. Electroplating is often used to build up top layer metallization where bonding to chips and to I/O occurs. Plating baths are, of course, wet processes and are notoriously difficult to control [Danner and Vilmer-Bagen 1992]. Difficulties are found with impurities and resultant poor films and with maintaining metallization thickness uniformity. Solution pH levels are sometimes incompatible with dielectric layers [Turlik and Adema 1992]. Finally, the need for the seed layer creates several more processes and additional cost.

Electroless plating could be attractive because it is a low-temperature process, but it has seen only limited application (occasionally in via filling, for example) [Turlik and Adema 1992]. The difficulty is in getting solutions which are compatible with the dielectrics in the substrate and in getting high conductivity (due to impurities).

Dielectrics

The process of choice for silicon dioxide [Marella and Tuckerman 1992; Kohl 1992] is plasma-enhanced chemical vapor deposition (PECVD). In a reaction vessel, silane gas (SiH_4) is mixed with an oxidant like oxygen or nitrous oxide, nd these react to form SiO_2 as a precipitant onto the substrate [Hnatek 1987]. By-products are pumped away. Forming a plasma of the reactants serves to enhance dissociation and improve the reaction. An advantage of PECVD is that it creates a SiO_2 film in compressive stress which inhibits crack formation [Marella and Tuckerman 1992]. Atmospheric pressure CVD does the opposite.

Substrates are most frequently coated with polymer layers by spin coating on a turntable. The substrate may first have an adhesion-promoting agent applied. This is followed by dispensing the polymer precursor. The turntable is spun to achieve a uniform film thickness. Then the substrate is thermally cured to drive out solvents and other volatile liquids.

In the case of polyimide, polyamic acid in N-Methyl-Pyrrolidone (NMP) solvent is the common precursor. A great many variations of polyimide exist, with attendant process variations [Garrou and Turlik 1992]. See, for example, [Craig 1989] for process details for generic polyimide.

There are several problems in spin coating polyimides, including:

- High viscosity--difficult to dispense and filter;
- Limited shelf life and low temperature storage (around 0 °C);
- Multiple spin coats needed to get film thicknesses above 10 μm and to achieve planarity;
- The square shape typical of MCMs inhibits uniform coating thickness; and
- Spin coating wastes expensive PI materials.

Snodgrass and Blackwell [1992] discuss these problems and describe an improved PI precursor pump. It is hydraulically actuated and has dual stages for filtering and dispensing. Point of use filtering including elimination of microbubbles is provided. They also describe a linear extrusion nozzle through which PI precursor can be dispensed uniformly on the substrate with no spinning and a minimum of wasted material. Preferred thicknesses of PI around 25 μm can be obtained in one pass. Almost $10/in^2 is spent on PI materials in spin coatings of a five-layer substrate, as compared with $1/in^2 in the case of this extrusion system. Turlik and Adema [1992] make a similar case for spray coating.

Curing processes vary with the polyimide or other polymer used. Polyimide is thermally cured at temperatures between < 200 °C and 450 °C [Cole et al. 1992; Craig 1989] to drive out solvents and initiate imidization. BCB is cured at about 250 °C [Cole et al. 1992]. A gentle increase in temperature of the substrates (over several hours) is helpful in avoiding blisters from outgassing [Charles and Clatterbaugh 1989; Craig 1989; Snodgrass and Blackwell 1992]. In the early phases of this cure cycle, solvent is primarily being driven out. Inadequate removal of solvent can lead to delamination [Murali et al. 1992]. After the maximum cure temperature is reached, a gentle decrease (again, over several hours) serves an annealing function in relieving some stress [Charles and Clatterbaugh 1989]. High stress around vias can lead to cracking and to formation of a raised crown that thins out subsequent metallization and leads to open circuits [Murali et al. 1992]. Proper curing, choice of solvents, and adjustment of design rules are crucial in controlling film stress and defects. It also can prevent unwanted outgassing later in the use of the MCM [Douglas and Smeby 1988].

3.3.2. Patterning (including Lithography and Wet and Dry Etching)

Many, if not most, patterning steps begin with spin coating a photoresist (PR) on the substrate in progress and bake curing. Then a mask of the pattern (positive or negative, depending on the process) is aligned with the substrate and brought into contact with the substrate. The PR is exposed to ultraviolet light through the mask and subsequently developed with an appropriate solvent to remove unexposed PR (negative resist) or exposed PR (positive resist). A second exposure cycle may be needed to remove PR in via wells in mid- to upper-layers of a substrate [Myszka et al. 1992]. A further bake cycle is used to drive out developer solvent and strengthen the PR for the etching process to follow. Lithography is this process of applying and developing a photoresist, followed by one of several etching processes.

Metallization

Patterning of the metallization determines the structure of the signal lines and other features in the substrate. Line widths are being made in the range 10-100 μm with line spacings in each case generally 50 to 100% larger though 1:1 is not uncommon.

If the PR has been developed on a metal film, wet etching can be used to remove the metal that is no longer protected by PR. An acid solution appropriate to the metal to be removed is used to do this. Because the lateral etch rate is about the same as the vertical rate, the metal that is left has a trapezoidal cross-section with 45° sidewalls. After the etch is completed, the remaining PR is removed with a different acid that does not attack the metal or with a solvent, depending on the particular PR.

In what is called a lift-off technique, the PR is developed on a dielectric layer and the necessary metal coating is *evaporated* through the developed photoresist. A nearly rectangular cross-section of metal is obtained because the evaporation source deposits metal on line of sight from the source. Sputtering does not work well in this instance because it tends to coat the sidewalls of the PR [Turlik and Adema 1992].

There are basically two methods of getting patterned metal with electroplating [Turlik and Adema 1992]:

- A subtractive process in which the seed layer is etched away except where plating is to proceed; or
- An additive process in which a photoresist is patterned and developed to expose the seed layer only where electroplating is to proceed.

After electroplating in the additive process, the remaining resist and seed layer are stripped away. Metallizations with nearly rectangular cross-sections are obtained in this way.

Dielectrics

Patterning of dielectric layers is accomplished to form vias or windows to connect or expose layers in the substrate. Vias down to about 10 μm in diameter have been produced [Turlik and Adema 1992]. Both wet and dry processes are available. Photolithography and wet etching can be performed on dielectric layers with analogous steps to those described in the previous section. As with metals, sidewalls are sloped due to nearly isotropic etching. Silicon dioxide can be etched by hydrofluoric acid [Hnatek 1987].

Polyimides [see Charles and Clatterbaugh 1989] are often patterned before they are fully cured. The precursor is soft baked, lithographically treated, etched, and then finish baked. If a negative photoresist is used, the soft baked PI can be removed by aqueous alkaline

solutions. One step can be eliminated if a positive PR is applied because the developer solvent will also etch away the PI. If the PI is fully cured, PI stripper chemicals will perform the etch.

The need for a photoresist can be bypassed altogether for some kinds of polymer dielectric materials. A photosensitive component can be added to the polymer that promotes cross-linking when exposed to ultraviolet light (436 nm line of Hg) [Charles and Clatterbaugh 1989]. This provides a simplified, alternate patterning technique. When photosensitive PI is soft baked and exposed through a mask, it can be developed with solutions similar to those used with negative photoresist. The disadvantage often cited [e.g., Turlik and Adema 1992] is that this form of PI shrinks up to 50% on final cure and makes a lip or crown of PI around the top of vias. As mentioned earlier, this can cause thinness in overlaid metal which may, in turn, lead to open circuits between layers [Garrou and Turlik 1992]. Development continues on improved photosensitive PIs [Schuckert and Fox 1990; Nader et al. 1992]. Other photosensitive polymer dielectrics have also been developed, such as a photosensitive triazine-based blend of polymers [Sweetman 1992] and a photosensitive BCB polymer [Rutter et al. 1992]. There are encouraging indications that lower shrinkage values (in the range 10 - 20%) may be possible with the BCB process [Rutter et al. 1992].

One class of dry etch process involves the use of plasmas [Charles and Clatterbaugh 1989; Turlik and Adema 1992]. The substrate with a top dielectric layer is coated with a plasma-resistant layer and then with a photoresist. The latter is developed and the plasma-resistant layer is etched away where dielectric material is to be removed. PR by itself is not sufficiently resistant to the plasma. After plasma etching, the masking layer is stripped by appropriate etching.

Reactive Ion Etching (RIE) is one form of plasma process in which the plasma ions react chemically with the dielectric being removed. This process is anisotropic and proceeds much faster vertically than laterally, resulting in nearly straight-sided vias. This can be controlled somewhat by plasma pressure and power. Non-reactive plasmas are more isotropic in their etching (and create more heat at the substrate).

In the processing of polyimides by RIE [Charles and Clatterbaugh 1989; Tessier et al. 1991; Turlik and Adema 1992], plasma masks are often made from SiO_2, Si_3N_4, thin metal films, or spin-on glasses. The plasmas are made from O_2 (with some CF_4 or CHF_3 optionally added). Metal masks are later removed by wet etching, and silicon dioxide or glass masks, by a CF_4 or CHF_3 plasma. In the processing of silicon dioxide layers, metal masks are used, and RIE is carried out with a CF_4 or CHF_3 plasma.

Another dry process is afforded by excimer laser ablation. Vias can be made one-at-a-time by direct writing with a programmable steered laser beam, or many vias can be made at once by illuminating through a mask. The latter has higher speed but requires a separate mask

for each layer and application. Such a mask can be photodefined on a deposited metal layer, like those used for RIE, or it can be a non-contact projection mask. Tessier et al. [1991] have shown that masked illumination should have somewhat better throughput than RIE. They also point out the need to clean up ablated soot after the process.

4. MANUFACTURING PROCESSES COMMON TO MCM-C AND MCM-D

4.1. Cleaning

Cleaning is an important topic affecting the reliability of processing and later use of any microelectronics device. Particulates can cause unwanted interference in patterning and can be the start of defect growth. Residues of processes in film or powder form may degrade electrical properties and lead to unwanted chemical corrosion. In printed wiring board assembly, cleaning issues have increased in visibility, particularly because of interest in finding replacements for chlorofluorocarbon (CFC) cleaning agents, so that conference sessions and whole conferences are appearing on the subject. Literature on MCM cleaning seems less well focused. The following comments point out a few cleaning-related issues that arise in the processes already discussed.

Good adhesion depends on clean surfaces. Several authors have commented that mild exposure of polyimide to a plasma is often helpful in removing adsorbed gases [e.g., Bachman and Vasile 1988] or surface damage [Murali et al. 1992]. Ion milling or RF sputter etching are also used [Darrow and Vilmer-Bagen 1992] but possible surface damage from more energetic processes must be considered [Murali et al. 1992].

A technique not covered in the literature reviewed here but likely to be important is the use of cluster tools to reduce contaminants from air and from handling.

Purity of materials is important and filtering improvements in connection to polyimide have already been mentioned.

Patterning involves many kinds of steps which must be followed by cleaning to remove either process chemicals, residual photoresist, or residual materials that have been etched away. Many such steps involve wet cleaning with water rinses, aqueous solutions, or special solvents which are specific to the detailed recipes. Dry processes like laser ablation have similar needs for cleaning as pointed out by Tessier et al. [1991]. An important consideration is to be sure that the cleaning process leaves behind as few residuals as possible, particularly involving water and water salts. This is especially true for MCMs which experience long term storage with considerable temperature cycling, as found in stored missiles.

4.2. In-Process Testing, Feedback, and Process Evaluation

Much work remains to develop in-process testing to the point where it can give meaningful *in-situ* feedback about process conditions and improvement, and little has been written. Mid-process inspections of traces or of electrical properties are occasionally mentioned. These are done when rework can be minimized by early detection of problems. For example, optical inspection of individual layers is practical for MCM-C with its 100 μm traces. Gross [1992] also discusses in-process electrical screening of lower level metallizations.

The approach generally taken is to define and experiment with process variables in conjunction with qualification and reliability testing. As an example, a good account of such a process in recent literature is given by Marella and Tuckerman [1992]. Yang [1992] describes a system-level view of "design for reliability" and qualification testing.

Another approach is to design and build special test-vehicle MCMs as a precursor to manufacturing an MCM product. The test vehicles are useful both for design and process refinement. They incorporate a variety of trace and via geometries for testing design rules for reliable structures. Electrical testing over a wide range of frequencies can be used to determine performance limits of the substrate. The test structures can also carry known heat sources and chips for measuring temperature and stress, and these, in turn, monitor particularly the quality of thermal management. Examples of such studies and related technology are given in [Westling et al. 1991; Chu et al. 1992; Solomon and Reche 1992; Sur et al. 1992; Volfson and Senturia 1992].

4.3. Pre-Assembly Electrical Testing

Yields on MCM substrates have been quoted in the range of 50-90% [Fillion 1992]. It would make no sense to add many high value chips to the substrate without verifying the electrical integrity of the substrate. Fillion [1992] gives a good overview of pre-assembly electrical testing. Such testing is designed to detect:

- Open circuits in vias and traces;
- Shorts between traces and layers;
- Electrical breakdown;
- High resistance in vias and traces; and
- Incorrect values of integral passive component parameters.

Defects of these kinds can arise from

- Incomplete metallization near vias due to dielectric crowning (mentioned above) or undercut and shadowed via walls;
- Particle contaminants present during processing;
- Voids in the dielectric;
- Poor adhesion;
- Contaminated plating baths; and
- Over- or under-etching.

To accomplish the tests, contact is made with the substrate metallization either by individual probes which can make programmed moves relative to the substrate (most common), or by specially designed beds of nails [Taylor 1992]. Environmental screening may precede electrical testing. Note that the GE HDI (chips first) system is not amenable to this kind of testing [Fillion 1992].

Checking for continuity or high resistance is relatively easy with programmable probes because the number of test sites to be visited is low enough to make it practical. Testing for shorts by straightforward means is impractical because the probe must visit on the order of $n^2/2$ pads where the number of such pads n is typically in the thousands. The accepted solution is to measure capacitance [Gross 1992] or equivalent [Shipley and Ritter 1992] at *each* pad and compare this with modeled data or known good signatures. In fact, capacitance can also be used to detect open circuits. Low capacitance shows the opens, and high capacitance, the shorts. By measuring at multiple points along connected pads (or nodes), the location of defects can be determined. Programming of the probe sequence is carried out with the help of CAD data on pad points and design interconnections.

5. STRESSES AND DEGRADATION MECHANISMS

5.1. Fundamentals

5.1.1. Introduction: Materials and Configuration Considerations

Microcircuits are precision, composite structures which involve several different classes of materials. All the various features composing these structures must remain stable during exposure to both operational and storage environments.* Electronic materials are exposed to a range of potential physical (mechanical, electrical, electromagnetic, particle

* See Appendix A for a description of tactical missile environments.

radiation, thermal) and chemical stresses during fabrication, evaluation, storage, and application. A circuit can continue to function electrically only if structural integrity is maintained throughout its desired life.

The use environment of an electronic system is a primary factor affecting durability and reliability. Whereas most consumer products are used soon after they are made and then are used regularly, many of the Army's missile systems could be dormant in storage for many years. The materials degradation evaluation used to determine ultimate reliability factors for a particular technology must appropriately consider the probability of long term dormant storage. One should note that unfortunate degradation mechanisms can, indeed, proceed in electronic systems in storage.

Microcircuit structures typically have large ratios of interface surface area to circuit volume. The characteristics of interfaces (including surfaces) in composite microelectronic structures are critical to the reliability and durability of the electronic circuit. The materials normally used in microcircuit construction are principally chosen with regard to electrical performance coupled with manufacturability characteristics. In fact, many of the materials employed as conductors, dielectrics, and semiconductors in microcircuits turn out to be intrinsically weak as mechanical structural materials. Interface parameters provide critically important mechanical strengthening for circuit structures. The criteria for the selection of materials employed for electronic packaging must first be dictated by electrical functions. Within these electronic criteria, the materials scientist must then provide materials having properties which provide for efficient manufacture and convenient interconnectability while also insuring the long-term protection and stability of the circuit structure. These are occasionally contradictory requirements since some of the materials having the most useful electrical properties happen to have less than desirable mechanical, thermal or environmental characteristics.

The materials and materials configurations of a microcircuit must remain mechanically and chemically stable for the circuit to provide reliable electronic performance. The reliability of MCM structures, as well as other microcircuits, is determined by the specific materials configurations employed, the integrity (consistency or "quality") of the manufacturing processes, and the degradation mechanisms activated or accelerated by the operational or storage environment. Multi-chip modules generate a new level of reliability concern because of their unprecedented combination of size and complexity. Essentially, MCM technologies compound the intricate complexity of the highest density IC technologies by interconnecting large numbers of these high density ICs to create very large and complex interconnection arrangements.

Multi-chip module types outlined earlier are:

MCM-C Multi-chip modules utilizing thick-film technology on ceramic substrates and multilayer ceramic packages.

MCM-D Multi-chip modules with signal lines created by deposition of thin film metal and dielectric materials in multilayer structures.

Anticipated advantages of multi-chip modules include improvements in performance, where speed is enhanced by not having chips in individual packages, reduced size, reduced weight, and ultimately reduced cost.

There already exists a large experience base concerning the reliability of high density ICs and most of the interconnection technologies currently employed and proposed for emerging MCMs. It is, therefore, unlikely that one will often encounter entirely new degradation mechanisms leading to new failure modes in MCMs. However, the extraordinary physical size, enormous numbers of tiny interconnections, high thermal loading, relatively large cost per unit, and uniqueness ("small part count") do, indeed, require a much more comprehensive approach to reliability than has previously occurred.

5.1.2. Materials Evaluations

There are interesting materials trade-offs in MCM design, and consensus has not been reached about the best combinations. For example, considering just some of the proposed MCM conductor materials, we find:

- Copper has good electrical conductivity but requires barrier metals (Cr, Ni, Ti, TiW) when used with polyimide dielectrics.
- Aluminum, the lowest cost metallization, has adequate electrical conductivity and has the additional advantage of the extensive infrastructure of already mature IC fabrication technologies. However, aluminum is highly active and subject to corrosion where its extraordinary natural oxide is compromised.
- Gold has very high cost and well known adhesion problems. However, it does have excellent environmental stability.
- Silver has very good electrical conductivity but also has relatively high cost, is subject to atomic migration, and has well known susceptibility to chemical attack by typical atmospheric contaminants (particularly, sulfur compounds).

In the story of MCM reliability, long lists of issues and parameters are inevitable because of the complexity of the materials and their interfaces found in MCMs. To make systematic progress, one must pull together knowledge of

- Intrinsic material parameters over a wide range of conditions;
- Specific configurations of materials including dimensions and mass distributions;
- Interfacial configurations and phenomena;
- Manufacturing processes, chemicals, environments, and anticipated manufacturing defects;
- Environmental conditions in which MCMs are stored and used, including temperature, humidity, radiation conditions, power excursions;
- Degradation and failure mechanisms and the stresses that drive them; and
- Strategies for ameliorating or preventing degradation.

Each of these topics is complex.

For example, just the intrinsic material parameters and susceptibilities relevant to both current concepts and more advanced future concepts include the following:

- Electrical parameters
  Resistivity - desired low, particularly with fine lines;
  Dielectric constant, dielectric strength (breakdown), etc.;
  Magnetic susceptibility, permeability, etc.;
  Band structures, band gap;
  Mobility;
  Wide range of device characteristics; and
  Contact potentials.
- Chemical parameters
  Chemical activity for processes, degradation;
  Chemical bonding;
  Electron affinity;
  Phase diagrams; and
  Chemical potential.
- Thermal parameters
  Melt point;
  Latent heats of phase transformations (fusion, etc.);
  Thermal expansion;
  Vapor pressure; sublimation;
  Diffusion coefficient;
  Specific heat; and
  Thermal conductivity.
- Mechanical parameters
  Elastic modulus (various);
  Tensile strength;

Elastic-plastic characteristics; yield point, etc.;
Toughness, hardness;
Fatigue durability;
Poisson's ratio;
Acoustical properties;
Mechanical creep; and
Friction, adhesion, wear - particularly at spring connectors.

- Structural parameters
  Single crystal, polycrystal, amorphous, epitaxial, etc.;
  Crystal structure;
  Relevant crystal transformations; and
  Relevant crystal defects.
- Optical parameters
  Fluorescence;
  Reflectivity;
  Refractive index;
  Electroluminescence;
  Birefringence; and
  Dispersion.
- Radiation parameters
  Cross sections; neutron, ionizing radiation;
  X-ray absorption, fluorescence;
  Radiation damage effects; and
  Scattering.
- Cross discipline effects
  Magneto mechanical (magnetostriction);
  Chemomechanical; stress corrosion, corrosion fatigue, etc.;
  Electrochemical;
  Mechano-electric (piezoelectric);
  Electro-optical (photovoltaic, photoelectron, photo electrolysis);
  Electro-optical; laser, led;
  Magneto optical;
  Thermoelectric; and
  Thermomechanical; expansion-contraction, glass transitions.

5.1.3. Degradation and Failure Mechanisms

The *mechanism of failure* is defined in MIL-STD-883C as "the original defect which initiated the microcircuit or device failure or the physical process by which the degradation proceeded to the point of failure, identifying quality defects, internal, structural, or electrical weakness, and, where applicable, the nature of external applied stresses which led to failure."

Correspondingly, the *mode of failure* is also defined in MIL-STD-883C as "the cause for rejection of any failed device or microcircuit as defined in terms of the specific electrical or physical requirement which it failed to meet."

From the materials perspective, *degradation mechanisms* are material processes acting to alter the configuration or properties of the materials in a device structure such that operational characteristics become less desirable. The *failure mechanism* is then the degradation mechanism (or mechanisms) which contributed to device failure.

Operational and storage conditions result in certain types and magnitudes of stresses. It is these stresses which actually induce or accelerate the degradation mechanisms which we are discussing here. Recognizing that seldom is there a single type of stress acting alone in a microcircuit structure, we list below the stress fields of primary concern in relation to tactical missile systems:

- Thermal
  Heating & cooling due to the external ambient conditions;
  Internally imposed for special purposes; and
  Normal Joule heating in operating circuit members.
- Mechanical.
  Residual stresses in circuit materials;
  Differential expansion with temperature;
  Expansion due to water absorption; and
  Inertially derived stresses from vibrating environments or from acceleration due to missile firing or dropping.
- Electrical.
  Potential differences: From applied circuit bias;
  Also derived from galvanic cells from the chemical activity of circuit materials; &
  Current density.
- Chemical.
  Chemical agents existing in the operational or storage environment;
  Residual process chemicals; and
  Chemicals which evolve from circuit materials.
- Optical.
  Incidental or intentional exposure to LASER, IR or UV radiation; and
  Possible ambient exposure to the sun.
- Radiation.
  Ionizing Radiation;
  Nuclear particles; and
  Neutrons, alpha particles, electrons, x-rays, gamma rays, cosmic rays.
- Magnetic fields (derived from motors, power lines, permanent magnets, etc.)
  AC electromagnetism; and
  DC magnetic fields.

Resulting degradation mechanisms likely to be activated in MCM materials include:

- Corrosion; various chemical reactions;
- Formation of specific chemical compounds due to presence of particular chemical agents;
- Chemical dissolution, specific atomic activity;
- Mechanical fatigue, creep, and creep-fatigue;
- Crack initiation/propagation;
- Mechanical overstress with cleavage fracture, excessive creep, etc.;
- High lattice excitation with joule heating elevating temperatures resulting enhanced atomic mobility, melting, etc.;
- Intermetallic, metal-polymer diffusion;
- Interatomic diffusion across the many interfaces in ICs and MCM substrate structure;
- Atomic migration along surfaces, grain boundaries;
- Corrosion fatigue;
- Stress-corrosion cracking;
- Crevice or galvanic corrosion;
- Electric current activated atomic displacement leading to void and hillock growth;
- Electric potential induced atomic transport;
- Modification, decomposition of polymer materials;
- Metal migration/diffusion;
- Moisture diffusion/migration;
- Galvanic potential induced atomic displacement leading to growth of dendrites;
- Electrochemical electromigration;
- Solid state electromigration; and
- Sublimation.

Parenthetically, some of these "degradation mechanisms" also correspond to valuable manufacturing processing mechanisms. For example, one uses chemical dissolution mechanisms to etch away layers to create IC or interconnection traces, and particular chemical reactions are controlled to create dielectric layers. It is thus important to assure that circuit structures are thoroughly cleaned following manufacture in order to insure that residual process chemicals do not remain to degrade the tiny structures which are the circuit interconnections.

In summary, some of the degradation mechanisms, listed above are accelerated by mechanical stresses alone, some by thermal or moisture expansion mechanical stress, and others by either chemical or electrically activated stresses. In the following sections, we will highlight three degradation mechanisms of major importance for MCMs:

- Thermal-cycling induced mechanical fatigue;
- Humidity or moisture induced mechanical fatigue or corrosion; and
- Wear out mechanisms caused by electromigration, an electrically activated stress.

In actual cases of durability problems in microelectronics, one often finds a synergism of multiple stress fields and degradation mechanisms acting.

5.1.4. Stress Concentration Sites

Sharp notches, vias, cracks, voids, precipitates, intermetallic compounds, etc. may serve as mechanical stress concentrators. Fatigue cracks generally grow from such stress concentrators. Fast fracture is propagated after initiation at stress concentrators. Chemical agents--like moisture, for example--migrate to cracks and notches. This causes rapid, local corrosion, and in some cases, also causes either environmental fatigue or stress corrosion cracking.

Differences in thermal expansivities can be as great as the twenty-fold difference between silicon and epoxy resin. The resulting thermal stressing can lead to mechanical failure and may also accelerate other degradation mechanisms.

Fatigue damage in metals is the result of cyclic stresses and strains that produce permanent damage to the material. In microelectronic systems, the differential thermal expansion associated with temperature excursions may induce or accelerate mechanical fatigue degradation mechanisms at certain susceptible sites. Damage is sustained on each cycle and can cause failure at loads well below those necessary to cause failure under non-cyclic conditions. *Thermal-induced mechanical fatigue is a major wear-out mechanism of concern to the complex structures involved in multi-chip modules.*

An empirical expression commonly adapted for applications to evaluate the fatigue performance of metals is the Coffin-Manson equation for fatigue. In its simplest form, the Coffin-Manson equation states:

$$N_f = (A/\varepsilon_p)^{1/m}$$

where N_f is the lifetime in cycles, and ε_p is the plastic component of strain.

The following are some of the important factors affecting fatigue-damage mechanisms:

- Surface roughness;

- Inclusions, voids & formation of intermetallic compounds;
- Available impurities and corrosion agents;
- Temperature;
- Solder joint configurations, composition;
- Relevant interfaces, materials, and parameters bridged;
- Strain rate;
- Strain range;
- Dislocation pinning, interactions with inclusions; precipitates;
- Dislocation pileups at grain boundaries & other interfaces;
- Formation of stable dislocation configurations (cells);
- Stress concentrators;
- Dislocation interactions with other slip bands;
- The formation of intrusions and extrusions by surface and interface slip;
- Deformation twinning;
- Initiation of microcracks;
- Crack multiplication, growth, or joining of microcracks; and
- The microenvironment interactions with surfaces.

5.1.5. Chemical Stresses

Moisture is the second major damaging environmental agent affecting the lifetime of electronic circuits. Moisture is often trapped in circuit cavities and within hermetically sealed microcircuit packages. Moisture can evolve from circuit materials such as polymers used for MCM dielectric layers, die attachments, and plated surfaces. Moisture from the environment will be also be conducted through any polymers used as 'seals' or package materials.

Moisture can cause mechanical problems as well as chemical ones; for example, by the swelling of some materials like polymer dielectrics in the presence of humidity or moisture [Agarwal et al. 1992; Shan et al. 1992]. Moisture can also induce crack growth in package materials to destroy hermetic seals subsequent to screens. Chemical effects come about by moisture activation of impurities--as little as a few monomolecular layers of moisture combined with trace quantities of halogens or other ions degrade metal circuit members in time.

Typical sources of chemical impurities found in microcircuits

- Contaminated incoming materials;
- Residual processing chemicals;
- Chemical agents evolving from polymers;
- Solder fluxes;
- Impurities trapped at interfaces with metallization layers, crevices, etc.;

- Atmospheric impurities;
- Human derived chemical agents (spittle, perspiration, cosmetics, etc.); and
- Moisture.

Atomic mobility is responsible for diffusion, another chemical phenomenon. Metals may not behave strictly as "solids" in the small features and configurations employed in microelectronics. Atomic mobility is typically accelerated by temperature according to the Arrhenius expression. Mobility is accelerated by presence of surfaces, grain boundaries, and lattice defects. Elevated temperature environments are used to screen for manufacturing mistakes that produce defects likely to cause failures because of diffusion-related mechanisms.

5.1.6. Electrical Stresses

Electrochemical electromigration has always been a major concern for electronic assemblies where chemical contamination is possible from either the local environment or from residual process chemicals. Electrochemical electromigration will always represent a major potential degradation concern for MCM structures. Electrochemical electromigration mechanisms are typically activated with the combination of factors:

- Potential differences between circuit conductors;
- Moisture condensed on surfaces;
- Suitable impurity atoms (halogens, alkalis, and other chemical agents); and
- Time.

Solid-state electromigration is one of the most important wear-out mechanisms in thin-film interconnections. Metal atoms are effectively caused to migrate along thin conductors by an 'electron wind' of high current density. This has become significant with the advent of traces at or below 25 μm in dimension after which amp-level currents produce current densities of the order of 10^6 A/cm^2. The electromigration damage rate is much greater for aluminum than for either copper or gold films (and it occurs at significantly higher rates in solder alloys). A number of microstructural and composition adjustments have proven successful for enhancing electromigration lifetimes. These include special grain structures, alloys with certain dopant metals and special interfaces. Electromigration degradation occurs primarily through the growth of voids and hillocks. The voids ultimately accumulate to cause burn-out of thin interconnections while the hillocks may cause shorts between conductor layers. Such phenomena are not likely to be important in missiles themselves which are "in use" for only a short period of time, but we will need to be concerned about this wear-out mechanism in missile related ground equipment which is operated for extended periods of time.

5.1.7. Mechanical Strengthening and Degradation Mechanisms

Interfaces between the materials which are employed to fabricate electronic structures must effectively bridge a number of material discontinuities. Example scenarios would include interfaces between two different metals, a metal and its oxide, a semiconductor and a metal or oxide, or a dielectric material with one of these. Interfaces between two materials must generally be either coherent, or at least, have near atomic-level adhesion integrity for the structure to be able to perform properly with the combined stress fields existing in typical microelectronic circuits. A partial listing of the factors bridged at circuit interfaces includes the following:

- Thermal expansion coefficients.
- Chemical characteristics; metal-metal, metal-polymer, metal inorganic compound, polymer-polymer, etc.
- Elastic moduli.
- Crystallographic structures.
- Crystal lattice parameters.
- Diffusion rates.
- Interfacial energies and surface energies.
- Interfacial coherency, bonding, adhesion.

So the interface between two materials must accommodate differences in these parameters. In addition, impurities are often trapped within real interfaces, and their properties determine important interfacial energies. If the materials at the interface cannot accommodate all of these factors, one simply does not get good adhesion.

Differences in lattice parameters are often accommodated by a network of misfit dislocations being created through mechanisms which allow them to glide into the neighborhood of the interface. Arrays of misfit dislocation networks are determined by the elastic moduli of the materials, the respective Burgers vectors, the difference in lattice parameters, and the interfacial energy.

A dislocation is a linear defect in a crystal lattice. Dislocation multiplication and movement are responsible for plastic deformation in most metals and alloys. Dislocations move on preferred slip planes. For face-centered-cubic (*fcc*) crystals, favored slip planes are (111). Techniques employed to strengthen metals are all based on presenting microstructural barriers to impede the motion of dislocations. A careful evaluation of appropriate dislocation interactions is necessary in the interface structures involved in MCM and other high density microcircuit structures. The interaction range of the internal stress fields created by a

dislocation turns out to be comparable to the physical dimensions of many important microcircuit features. Dislocations affect not only mechanical strengthening and deformation phenomena, but also influence chemical kinetics since dislocations represent high energy features. There are also situations where dislocations influence electrical parameters or performance.

Dislocations interact with:

- Applied shear stresses;
- Chemical agents;
- Each other (work hardening);
- Other lattice defects;
- The lattice;
- Interstitials;
- Dispersions;
- Primary interfaces (surfaces, substrates, dielectrics, etc.);
- Grain boundaries with second phases;
- Intermetallic compounds;
- Precipitates (coherent and particles);

The mechanical strength and deformation behavior of the thin metallization layers employed in circuits are determined by the activation of dislocation dynamics in these structures. It is, therefore, important to briefly review some of the fundamentals of dislocation interactions, particularly with the interface structures mentioned above, in order to have a better understanding of the factors which determine the ultimate integrity of the metallization structures.

The stress field of a dislocation in a solid is long-ranged. It is significant that the fine-line dimensions, of less than 1 μm, now employed in VHSIC devices correspond to the maximum interaction ranges of dislocation stress fields. Even in MCMs where lateral dimensions of features are of the order of 15 - 100 μm, stress fields are relatively significant in size. Dislocations are prone to exit at free surfaces of crystals where they have sufficient mobility. Simply speaking, dislocations exiting at surfaces is the very mechanism of plastic deformation. If dislocations can move and then "exit" under low mechanical stress, then the metallization layer is very weak. However, certain interfaces effectively repel dislocations, and there is an effective barrier to dislocation transport across the interface. This situation is found with dislocation pile-up on a slip plane oriented at an angle to the interface. Dislocation barriers strengthen metals and very efficient dislocation barriers are employed to create the high-strength metals. These mechanisms are particularly important for the very thin

metallization layers which would have very minimal strength if not for the fortunate operation of interface strengthening mechanisms.

The interface configuration relevant to surface coatings has been theoretically modeled by considering individual interactions of the single real dislocation with an infinite series of image dislocations. The interface interaction for thin coatings has been quantitatively investigated both experimentally and theoretically. These calculations show that at large distances from the interface, the dislocation is attracted to the interface as it would be if the interface were a free surface. As a dislocation approaches the interface, the attractive force decreases, which is the opposite situation to that for a free surface. At a particular distance from the surface, based on substrate and coating material characteristics, the dislocation is in equilibrium and the force on the dislocation then becomes repulsive as the dislocation approaches the interface from that point. The maximum repulsive force is determined by factors associated with the region of highly displaced crystal atoms within the dislocation.

All of the current and proposed MCM systems have very high concentrations of such interface systems. As conductor dimensions are further reduced, the image dislocation effects due to the presence of oxide layers and intermetallic interfaces take a dominant role in controlling the structural durability of the thin conductors. Certain high-performance bulk structural alloys have experienced catastrophic failures because particular environmental conditions destroyed barrier coatings provided by the metal's oxide layer. Because of the small dimensions in microelectronic device structures, interface micromechanics have always played a significant role in the operational durability of these circuits. Anything that alters the physical properties of even very thin coatings in microcircuit structures can vastly alter the mechanical strength of the conductor. Such alterations occur from environmental agents (particularly water) interacting with surface coatings and from interface diffusion. These factors have been little understood by most engineers concerned with microcircuit design and fabrication.

Mechanical strengthening in thin structures depends upon such factors as:

- Composition of the metal film.
- Crystal structure of the metal.
- Grain structures (grain size, orientation, etc.).
- Thermodynamic characteristics (melting points, diffusion coefficients, latent heats, surface and interfacial energies).
- Thicknesses, widths of features.
- Interface interactions.

5.2. MCM Substrate Degradation Issues

The substrate systems currently discussed offer widely diverging directions for MCM technology to proceed in the future. The two technologies which appear to have the better chance for accomplishing MICOM objectives are MCM-C and MCM-D. The relative importance of both the fabrication quality issues and the stress-induced degradation mechanisms affecting the reliability of the two general concepts differ somewhat.

A significant experience base is available for the generic materials and process steps for substrates of MCM-C. Many of the materials and processes are borrowed from the mature hybrid microcircuit technology, for which there is more than two decades of literature. The line widths possible for the cofired conductors of MCM-C are limited by the screen printing technology to about 100 μm, which is unfavorably compared to 10 μm line widths for MCM-D.

The substrates of MCM-C concepts are essentially complex ceramic composite structures. The strongest known materials are ceramics, in the form of small diameter fibers. Under large stresses, mechanical energy is stored in the ceramic material by, essentially, perfectly elastic deformation. While certain ceramic members can have extraordinary strength, others are easily fractured. When structural failure occurs in ceramic materials, the fracture has a brittle nature. The key factor is that plastic deformation is not accommodated by the ceramic material's microstructure. The particular ceramic members exhibiting extraordinary strength do not have the types of flaws or other geometrical sites which serve to create stress concentrators. Whereas ductile materials are often found to relieve high stress concentrated sites, such as the tips of micro cracks, brittle materials tend to fracture by cleavage. Stress relief may occur in highly ductile materials by plastic deformation; the mechanism may be the activation of dislocation dynamics in metals, and viscoplasticity in polymers. The energy of the mechanical stress is thereby converted into heat energy within ductile materials. However, the lack of operable plastic deformation mechanisms in brittle ceramic materials causes this energy to, alternately, be directed to the creation of the new surface areas involved in crack propagation through the structure. It also must be understood that structural metals often experience cleavage fractures after having "hardened" during the course of initial plastic deformation. Similar behavior is noted in polymers.

About a century ago, Griffith derived a simple equation providing quantitative criteria for crack growth. He employed the concept that crack propagation was determined by the transfer of elastic energy to the creation of new surfaces. He accordingly developed a relationship between threshold mechanical stress, crack tip radius and surface energy. Griffith's concept remains applicable today and very often provides the basic understanding

for failure mechanisms operating in electronic structures. Griffith's expression clearly illustrates how the introduction of not much more than a monomolecular layer of moisture or other chemical agents accelerates mechanical failure. Essentially, moisture or another active chemical agent simply decreases the surface energy of materials so that the elastic strain energy is more effectively converted in such a way as to produce the new surfaces of fracture.

Cleavage fracture will always be one of the most important threats to the reliability of ceramic circuit structures in MCM-C technologies. The same is true for the ceramic and silicon substrate bases that may be employed for MCM-D technologies. However, because the circuit is geometrically quite complex, an analysis of stress distributions which potentially may support catastrophic microcrack growth is similarly complex. For example, if a substrate is improperly fabricated such that there are sites on it having high residual stress after processing, then crack initiation and propagation may occur. An unfortunate materials match could also provide very high local stress fields during temperature excursions. Similarly, sites of locally poor interfacial adhesion between layers may also generate enormous stress concentration sites. From the previous discussion, the introduction of chemical agents, particularly moisture, to a ceramic circuit where there are exposed microcracks can alter the surface energy sufficiently to change what originally was a fairly robust substrate system into one that is much more susceptible to mechanical failure.

Chip attachment and interconnections can, themselves, create sites where the stresses during temperature cycling can cause cracking. A particular multiple-layer ceramic surface mount board involving leadless chip carrier (LCC) devices was recently examined by one of the authors (Livesay). The construction materials and geometry involved in this board corresponds somewhat with substrate configurations suitable for a very low chip density MCM-C substrate. Some of these boards experienced cracks within the ceramic under the solder pads following temperature cycling (not shock). High local stress from the solder in conjunction with a stress concentrator associated with an inadvertent notch adjacent to the solder pad contributed to the catastrophic crack growth. The board survived temperature cycling after redesign eliminated the notch. Since there is a lack of knowledge concerning the strength and deformation characteristics of the deposited materials of each layer, resolution of this problem required an empirical approach involving considerable time and expense.

Such resolution of structural problems is inadequate for the much greater chip density and much finer traces for MCM-C substrates. The materials properties need to be known for the dimensions involved and much more effective modeling of the board features using finite-element analysis is needed. MCM substrates and chips sets are entirely too expensive

to resolve reliability problems after design and manufacture by empirical approaches. Unfortunately, this approach is not unusual for many current military systems. The relative thermal expansion and compliance of conductors, dielectrics, imbedded passive devices, and attached chips may be principal factors affecting the reliability of these structures.

The drive towards high density is a concern for the MCM-C materials and techniques. The nature of the cofired materials and processes are more susceptible to local discontinuities which have greater significance as circuit density is pushed by decreasing line widths. Not only do such sites affect electrical conductivity, at small sizes, they can have greater significance as mechanical stress concentrators. Another important factor is that ceramic materials tend to have lower thermal conductivity values than do the metals. Even for cases where CTE values are matched, local hot spots may generate differential expansion, thus concentrating the local stress. Crack initiation and growth can be thereby stimulated. It is well known that moisture tends to diffuse into microcracks in materials, stimulating corrosion processes in metals and crack growth in the ceramics. The combination of potentially available moisture during long dormant periods and thermal mechanical stresses present a risk for degradation which must be evaluated for the specific materials configurations of each circuit structure.

Whereas the substrates involved with MCM-C relate with the materials technologies historically associated with hybrid microcircuits, the MCM-D technologies tend to draw extensively from the thin-film deposition and processing methods associated with chip-level metallization and dielectric layers. MCM-D technologies use metallization metals such as Al, Cu, and Au with dielectrics such as SiO_2 and the polyimides. Blood [1991], of Motorola, has outlined how the techniques used to design and personalize ASICs find application to MCM-D substrates.

As is the case with MCM-C, differential expansion represents an important driving force for degradation mechanisms affecting the reliability of MCM-D technologies. CTE values of a number of the materials potentially employed in MCMs are collected in the charts contained in Appendix B. Silicon chips mounted onto a silicon base clearly presents a significant advantage by matching CTE values of chip and substrate. The metal conductors have values of CTE much greater than that of Si. For example, the CTE of aluminum is almost 10 times that of Si. However, vacuum or sputter-deposited metallization layers provide much higher ductility, and therefore "tougher" lines, than can be accomplished in the cofired lines of MCM-C.

Gold is chemically inert under most of the conditions relevant to microelectronics. However, both aluminum and copper metallization layers are susceptible to corrosion. Aluminum is one of the most active of all metals but also forms an extraordinary natural

surface oxide which serves the function of protecting the metal from further attack. Of course, ions which attack aluminum oxide can negate this protection. Both copper and gold atoms tend to be quite mobile with respect to the small dimensions of microelectronic features. The oxide tends to tie down aluminum atoms and thus inhibit aluminum diffusion where the oxide remains coherent. This factor, along with corresponding good adhesion characteristics, accounts for the enormous success the electronics industry has experienced using aluminum metallization on ICs.

Atomic mobility has extraordinary significance when one considers interdiffusion through the many interfaces involved with MCM-D. IC technologies have historically developed certain "barrier" layers to inhibit intermetallic diffusion. Diffusion represents a "wear out" mechanism for microelectronics since, over time, diffusion across an interface can modify the composition of the thin materials, resulting in undesired property modifications. Barrier metals include flash deposited films of Ti, TiW, Mo, V, etc. which may also serve to assist adhesion between the layers. Such layers are required when using either gold or copper, but not with aluminum. The interface structures often provide important mechanical strengthening for the metallization layer. The cyclical thermal mechanical stresses associated with power cycling modify the microstructure of metallization layers where the local stress approaches the yield point of the metal. This phenomena is seen and has been documented for aluminum metallization layers on silicon chips, and can be quite significant after a few thousand deep-temperature cycles. Discussions with personnel working with MCM systems reveal that the actual magnitudes of electric current in MCM substrate lines can be many times greater than that occurring in IC lines. One thus can experience significant current density values in the lines of MCM substrates supporting large numbers of chips. This represents a problem familiar in the fine lines of ICs but not previously a significant concern in the normal printed wiring board structures.

The chart in Appendix B containing electrical resistivities of the various candidate metals shows that copper should serve as an excellent conductor, particularly as conductor cross section is decreased. In addition, recent studies have demonstrated that copper has good durability with regard to solid-state electromigration degradation processes. Pure aluminum is the least durable with Au and Cu being much better. Silver, as seen on the chart, has excellent conductivity but also has a well-deserved reputation for extensive atomic migration and corrosion. The growth of silver whiskers and other mobility-related problems has caused the electronics industry to avoid the use of Ag in recent years.

Copper traces have enjoyed extraordinary success in printed wiring board technologies so that there is a natural desire to extend its application to the MCM-D technology. Coincidentally, work is currently underway in both Japan and the U.S. to

evaluate the application of Cu metallization to high density IC development. The issue is probably a couple of years from resolution since so many factors are involved. Copper is favorable because it has excellent thermal as well as electrical conductivity, is easily available in a highly purified state, and has a stable face-centered-cubic (*fcc*) crystal structure. However, unlike the oxide of aluminum, copper oxides tend to become thick and tend to "flake" off the Cu surface. Unless effectively blocked, copper diffuses across interfaces into the adjoining material. This represents a particular problem for the polyimides where copper ions degrade dielectric performance. In addition, under certain conditions, copper is often found to participate in electrochemical electromigration mechanisms. This is a well-know degradation mechanism for standard printed wiring board systems. Gold can also be subject to electrochemical electromigration.

Polymer dielectrics offer advantages but suffer from a significant problem. Essentially all polymers are conductors of moisture, which affects adhesion and may promote the corrosion of adjacent metallic materials. Some of the otherwise highly-valued polyimide dielectric films also absorb significant quantities of moisture. Moisture adsorption can modify characteristics of these materials. For example, polyimide films can absorb significant quantities of moisture resulting in up to 10 % increases in dielectric constant and in mechanical expansion. Such dielectric constant modifications correspondingly affect speed and the mechanical expansion can introduce added mechanical stress to circuit materials.

Adhesion is also influenced by moisture. Hermetic packaging is clearly desired for Army missile systems which are stored for significant durations, as discussed in Appendix A. Additionally, there is a large body of information concerning the evolution of moisture from polymer circuit materials. Moisture and other chemical agents evolving from circuit materials have, occasionally, induced corrosion of metal conductors. They also may provide the necessary chemical and moisture components needed to support electrochemical electromigration. These factors need to be carefully understood when evaluating reliability factors. There is considerable interest in a Dow Corning inorganic coating material which, apparently, has been under development over the last decade. The concept is that this coating would provide the required "hermeticity" for the circuit. Extensive evaluation is clearly needed to determine if the coating is effective both initially and following extended periods of both operational and environmental stress conditions. An obvious concern for such thin coatings, which may be brittle since they are said to be inorganic, is their mechanical durability with temperature-induced mechanical cycling.

As mentioned in a later section of this report, qualification tests and screening methodologies need to be developed for the new forms of MCM structures. Ample

instrumentation is already available to accomplish the evaluation and failure analysis requirements. However, the significant challenge is found in determining how to apply these techniques to the large and complex MCM substrate configurations.

A special MILSPEC has not yet been generated for multi-chip module technologies. We are in contact with the individuals responsible for addressing the issues needed to develop the MCM specification. Effectively, the Hybrid specification, MIL-H-38534, is being studied for adaptation for the new MCM specification, where appropriate. Several of the relevant documents reviewed in this context are listed below.

MIL-M-38510 General Specifications for Microcircuits
MIL-H-38534 General Specifications for Hybrid Microcircuits
MIL-I-38535 General Specifications for Integrated Circuits (Microcircuits) Manufacturing
MIL-STD-1772 Certification Requirements for Hybrid Microcircuit Facilities and Lines
MIL-STD-883 Test Methods and Procedures for Microelectronics

Georgia Tech was recently invited to participate in a joint effort of DARPA, NASA, Rome Labs, Naval Surface Weapons Center-Crane and US Army LABCOM has established an MCM reliability program called RELTECH. RELTECH "is designed to select MCM technologies with high potential for DoD, NASA, and commercial usage and verify their performance and reliability." It will endeavor to establish a government/industry infrastructure to actively evaluate issues relative to the reliability of MCM. As of this writing, RELTECH is drafting a validation plan which is being reviewed by committee members. A major goal of this group is to discover the major failure mechanisms which operate in MCMs. It appears that initial effort will be devoted to the GE-HDI MCM technology since there are expected to be GE-HDI units available through DARPA funding. To our knowledge, the RELTECH effort represents the first physical attempt to independently evaluate MCM reliability factors.

Mention needs to be made of the rework problem for MCM. As is true for hybrids, MCMs are expected to be much too expensive to discard in case a particular die is bad. The repair must be accomplished without otherwise degrading other chips or the MCM substrate itself. For example, a mistake (mechanical, thermal or chemical) which destroys a single, tiny plating layer on a pad may make it necessary to discard an entire MCM worth, perhaps, thousands of dollars. Clearly, rework represents one of the significant reliability problems to be studied.

5.3. Exposure to Acoustical Radiation During Ultrasonic Cleaning

In an earlier section, a few cleaning processes for MCM substrate manufacturing were reviewed. We will mention here an interesting story that is emerging about another cleaning mechanism that should probably be avoided.

There is a strong drive by the electronics industry to employ ultrasonic (US) cleaners to assist in the removal of active flux chemicals now that chlorofluorocarbon solvents (CFCs) will soon be prohibited. US cleaning is certainly effective for removal of residual chemicals in tight spots. However, the issue of a possible reliability problem has not been fully resolved. About two decades ago, reports of various observations raised questions that the ultrasonic energy employed in flux cleaning operations may also damage microcircuit interconnections, particularly bond wires. The damage reports included a number of SEM micrographs which have been reproduced through the years in trade journals, etc. showing catastrophic mechanical fatigue fractures in wire bonds attributed to exposure in ultrasonic cleaning baths.

The results of experiments reported in the literature during the last three decades have clearly indicated that the application of ultrasonic energy can stimulate atomic movement in metals sufficient to significantly modify microstructural configurations and strongly influence the mechanical performance of metals. Dislocation movement past/through pinning points is apparently assisted by induced lattice vibration in a manner analogous to that of thermally assisted dislocation dynamics. Acoustical energy is preferentially absorbed at lattice defects and other discontinuities in the metal lattice such that acoustical excitation is, energy wise, more efficient for enhancing mechanical deformation than increasing temperature. However, the detailed manner in which ultrasonic energy interacts with lattice defects, voids, dispersions, intermetallic compounds, microcracks, interfaces, and other microstructural features in materials needs to be better defined for the microcircuit interconnections of interest here.

The need to employ processes involving ultrasonic energy-assisted cleaning of MCMs may become an important issue as environmental degradation concerns evolve. However, the normal energy density imparted to electronic materials during US cleaning is apparently considerably less than that imposed during some of the ultrasonic induced deformations investigations just mentioned. Since it is clear that ultrasonic energy does interact with microstructural features, quantitative data are needed concerning possible energy density thresholds and the effective frequency regimes for damage to specific microcircuit structures. The most susceptible circuit features are considered to be wire bonds, fine solder joints, and TAB bonds. However, it is possible that other material features might have susceptibility to ultrasonic excitation damage, such as fine metallization lines, dielectric film materials, chip capacitors, and chip resistors.

5.4. Application of Environmental Stress Screening to MCMs

Environmental stress screens were historically developed around crude trial-and-error methods where large amounts of statistical data were analyzed to determine which screen stress levels and durations demonstrated effective fault detection. However, with the evolution of the enormous complexity and expense of advanced microcircuit structures, greatly improved methods are needed. The large transistor counts of VLSI devices have made necessary the development of entirely new quality assurance test methodologies to detect if even one of the many tens of thousands of circuit features did not function correctly. Small lot sizes and the high value of individual MCMs similarly dictate greatly improved analytical approaches to the entire process of assuring that a completed MCM does not have a latent defect which could cause a disastrous failure of the system in the field. The effective methodologies developed during the last fifteen years to work with VLSI/VHSIC, such as built-in test circuits, other in-process testing, statistical process control, etc. need further development for application to the still more complex MCM structures. Certain non-destructive testing methods, such as optical imaging analysis, scanned-beam x-ray laminography, scanning acoustic microscopy, etc. are proving effective in microcircuit structures relevant to proposed and current MCM substrate level technologies.

However, it is likely that the seemingly primitive methodologies historically associated with environmental stress screening (ESS) will still be required to achieve assurance of MCM reliability. Circuits are simply too complex, with the individual circuit features being very small, and often concealed, to be able to carry out comprehensive inspections of advanced microelectronics. To make ESS for developing microcircuit structures a precise engineering discipline, there is a strong need for comprehensive knowledge of materials including quantitative stress-material-defect response data. This has been appreciated for some time, but data can now be developed much more effectively because of extraordinary advances in analytical instrumentation, computer hardware, and related software.

An efficient environmental stress screen should be designed with the kind of material defects in mind that it is intended to detect. To do this, one must first have knowledge concerning the performance of the relevant materials under a wide range of operating and environmental stresses. The degradation mechanisms which cause device failure must be identified and a fundamental, quantitative understanding developed of these degradation mechanisms. For example, one needs to know the possible stress threshold levels for activation of particular degradation mechanisms, as well as data concerning stress-induced degradation rates with regard to stress level, temperature, etc. Greater precision in materials measurements, combined with statistical design and mathematical modeling, are necessary.

Meaningful screen testing parameters for MCM technologies need to be developed based upon the determination of stress duration levels required to reveal electronic material defects. Fundamental work is needed in several areas summarized below:

- Determine critical magnitudes of defects.
- Chemical reactions - measure stress-induced rates and determine possible thresholds associated with chemical agents in circuit microenvironments.
- Interatomic diffusion-chemically, thermally and electrically motivated. We need knowledge concerning diffusion across the large array of interface structures employed in MCM as well as VLSI/ASIC chip level.
- Effects of the large range of potential materials combinations which currently are available and those newly developed to serve MCM functions.
- Understanding of material degradation mechanisms.
- Film growth, microstructural characteristics for various metals, inorganic compounds, and polymer materials--related to deposition or growth technology and process parameters.
- Fine line defects and degradation mechanisms.
- High density testing.
- Intermetallic bonding.
- High density interconnection technologies - solder configurations, wire bonds, TAB.
- Microfatigue processes in circuit materials.
- Stress modeling and analysis of circuits.
- Thin oxides.
- Electrostatic field induced mechanisms.
- Semiconductor defects.
- Screens relevant to new packaging technologies.
- Develop quantitative data to tailor stress levels to accelerate only defects of critical magnitude to failure in ESS.

In the near term, the Army is likely to employ initially costly and complex MCMs in high performance applications like missile guidance and control. There will still be a critical need for high reliability. It is likely then that the development of new precision ESS methodologies will be required for military MCMs.

6. CONCLUSIONS AND RECOMMENDATIONS

In the remarkable variety of processes used today to make MCMs, it is difficult to pick winners, but it is helpful at least to have a 'theory' of winning. Ours is that progress may happen on two fronts: first in process simplification; second in materials and process quality.

Some of the processes we have reviewed are attractive because they eliminate steps. Fewer steps can minimize cost as well as opportunity for error. Cost reduction is a major factor in making MCM production viable in the U.S. Highlights mentioned in our review are summarized in Table 2.

Table 2 Opportunities for Process Simplification

Opportunity	Remaining Issues for Viability
Low temperature co-fired ceramics for MCM-C	Increasing strength Increasing thermal conductivity
Gold thin-film metallization	Adhesion may be solved but more experience and data needed. More data on electrical performance needed.
Photodefinable polymers	Reducing cure shrinkage
Laser projection ablation of vias	Affordable projection masks

Some additional areas of promise in materials and process quality are

- Polymers with low water absorptivity (and better planarity) e.g., BCB, silica-loaded PTFE, and polyquinolines;
- New adhesion promoters;
- Controlled extrusion or spray coating apparatus for deposition of polymer precursors;
- Better filtering equipment and higher purity materials;
- Use of automated handling and controlled environments, e.g. in cluster tools; and
- Development of *in-situ* process sensing and feedback control.

In order to make progress on any of these, much more systematic materials and process understanding must be achieved. We recommend that the specific process and materials issues listed above be supported for further research. Much fundamental knowledge remains to be gathered concerning even commonplace MCM materials and fabrication techniques. This is illustrated by a comment made by Solomon and Reche [1992] when they compared their 3-D finite-element model of thermal test dies mounted on a substrate with

experimental data on thermal conduction. Though qualitative agreement was found, significant quantitative differences were attributed in part to a lack of thermal conduction data on die attach adhesives. There are a host of missing pieces like this.

Often it is important to make the measurements on materials samples with dimensions like those found in MCMs and microelectronic circuits. The work reported by Darrow and Vilmer-Bagen [1992] on metallization resistivity bears this out. Similarly, extensive recent measurements in Georgia Tech's micromechanics laboratory on solder samples and free-standing metal traces have shown that small thin samples of materials have mechanical properties which are distinctly different from the bulk. We recommend that micromechanical measurements (and where possible electrical property measurements) be extended to dielectric materials. Such measurements should be carried out over the range of temperatures and humidities experienced by missiles in storage and in use.

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APPENDIX A: TACTICAL MISSILE ENVIRONMENTS

Introduction

The material in this appendix was first published in

B. R. Livesay and E. J. Scheibner, "Reliability Factors for Electronic Components in a Storage Environment," Final Technical Report No. DD 14-23, Contract DAAH01-75-C-0782, U.S. Army Missile Command, September 1977.

It is reprinted here with minor editing as a potentially useful reference to the severe environmental conditions to which multi-chip modules in missiles may be exposed.

The environment seen by a tactical missile during storage is critical to long term reliability. The need for an advanced assessment of potential storage degradation makes it essential to develop a knowledge of potential environmental stress parameters. Unfortunately, the environmental conditions expected during the life of an Army tactical missile system can never be clearly defined in advance. While it is generally intended that missiles will be placed in well-protected magazines for storage, military needs often dictate their movement to practically any location on earth for short durations. Therefore, the assessment of potential storage environments of Army missile systems must take into consideration worldwide ambient conditions.

An evaluation of the long-term reliability of U.S. Army tactical missile systems differs significantly from that of non-missile systems, which are normally operating systems. Missile systems may be in storage for periods up to 20 years and for the most part they are dormant or inoperative. The basic requirement is that these systems maintain their operational readiness after long periods of dormancy under a variety of storage conditions. A large body of knowledge is available concerning the reliability of mature generations of electronic systems. However, much less knowledge exists for the behavior of such electronic components in storage. The new materials configuration of multi-chip modules represent challenges for both the storage and the operational environment. A direct approach to missile system reliability considers the fundamental materials degradation processes which would potentially lead to failure of electronic components of missile systems in an extended period of storage as well as operation.

Definition of Storage Environment

The term *storage environment* used here will include all the environmental conditions a missile experiences from the time of its manufacture until it is fired. The term, therefore, takes into account magazine storage, air, land, or sea transportation, dump storage, and temporary deployment to combat units. Some missiles are expected to spend much of their storage lives in earth-covered, concrete magazines, or igloos, where daily temperature variations are small. For example, the temperatures of missiles stored in this type of magazine at the Anniston Army Depot range between 10 °C and 21 °C over the year with daily temperature variations less than 2 °C. However, the relative humidity in the magazines is normally above 70%. Certain missiles may spend considerable time stored under field conditions involving widely varying ambient environments corresponding to their location including such extremes as Arctic, desert or tropical areas. Storage locations sometimes include covered sheds with open sides. All systems are subject to periodic transportation based on military requirements. While the conditions in a magazine are fairly constant, the transportation and field environments may involve wide short-term temperature and humidity variations as well as some mechanical shock. For example, thermocouples implanted in CHAPARRAL missiles revealed that components near the surface can reach maximum temperatures of 75 °C while exposed to solar radiation in Arizona [Mitchell 1973]. Daily temperature cycles greater than 50 °C are, therefore, probable under such conditions. Alternately, the field environment can also include rain, ice, salt spray, and other atmospheric pollutants.

Missile Storage Environments

Storage periods of fifteen years or more are mandatory for any Army systems. While many systems can be stored primarily in the magazine environment mentioned above, others will, by the nature of their mission, have to be exposed to severe ambient conditions for extended periods. Extreme weather conditions, therefore, must be used to guide evaluations of the potential for environmentally-activated degradation processes. Use of recorded weather parameters must be done carefully since certain extreme values do not occur simultaneously and individual extremes may have a low probability for occurrence. Some of the anticipated extremes are summarized in Table A-1.

The data in Table A-1 include extreme measured values for missile storage environments recorded in various published reports. It should be noted that certain of the extreme values may rarely be achieved. For example, the maximum temperature of

Table A-1

Estimated Extreme Storage Environmental Parameters

Environmental	Estimated
a. Maximum Temperature	+ 75 °C *
b. Minimum Temperature	- 50 °C *
c. Temperature Cycling	$\Delta T \approx 70$ °C *
d. Moisture	Up to 100% Humidity
e. Moisture	Direct Contact with Water on Exterior of Missile
f. Atmospheric Pollutants	Sea Spray
g. Atmospheric Pollutants	Industrial and Other Pollution Agents
h. Thermal Shock	Small
i. Mechanical Shock and Vibration Due to Transportation and Handling	≈ 10g
j. Bacteria, Fungus	Heavy Exposure
k. Nuclear Radiation	Not Applicable
l. Electromagnetic Fields	Not Applicable

*These values vary in different parts of a missile structure.

75 °C was measured at the surface of a small missile exposed to solar radiation in the desert. The time at temperature was small. Schafer [1977] states that the use of too wide a temperature range in design specifications "may be one of our most all-pervading errors." This is particularly true where unnecessary costly material substitutions are thereby required. A detailed analysis of the temperatures actually expected in relevant parts of the missile structure should be made prior to final design. For example, Schafer concludes from his data that the design temperature range for a missile motor grain should be more like -30 °C to 55 °C [Schafer].

Many Army missiles are electrically dormant throughout their storage life. This is an essential factor in consideration of the anticipated long-term reliability of these systems. The trend for Army tactical missiles has been toward CERTIFIED ROUNDS which are never tested during storage. Even those missiles which can be electrically checked remain dormant most of the time. A missile system's ground support equipment, however, may be operated more extensively.

A comprehensive study was made by Dantowitz and Hirschberger [Dantowitz, et al. 1971] of field failures in an aircraft weapon system deployed in Southeast Asia and Coastal areas of the United States. Although this study concerned many systems other than missiles, it is useful here because it represents one of the few degradation surveys of modern tactical equipment. They found, for example, that fifty-two percent of approximately 46,000 field failures are identified as having been induced by environmental conditions. Temperature, vibration, and moisture were the major environmental factors found to cause failures. Temperature-cycling increased the failure rate of some equipment by four to eight times that of equipment operating at constant temperatures. A summary of these data is given in Figure A-1. A subsequent report by Hirschberger and Dantowitz [1975] analyzes additional data with regard to failure rates associated with operating equipment under various environmental stresses.

A significant body of information available in government documents provides a guide for specifying the environmental conditions seen by missiles in storage. Although a full review of their data is not practical within the context of this current report, a number of these documents are listed in the bibliography. U.S. Army Regulation AR 70-38 [Department of the Army 1969], "Research, Development, Test and Evaluation of Materiel for Extreme Climatic Conditions," breaks worldwide climatic parameters down into eight categories. Temperature, moisture and solar radiation extremes are tabulated for each of these categories in Table A-2. Comprehensive investigations of worldwide weather parameters are conducted by the Geographic Applications Division, USA ETL at Fort Belvoir, VA. Publications of this group

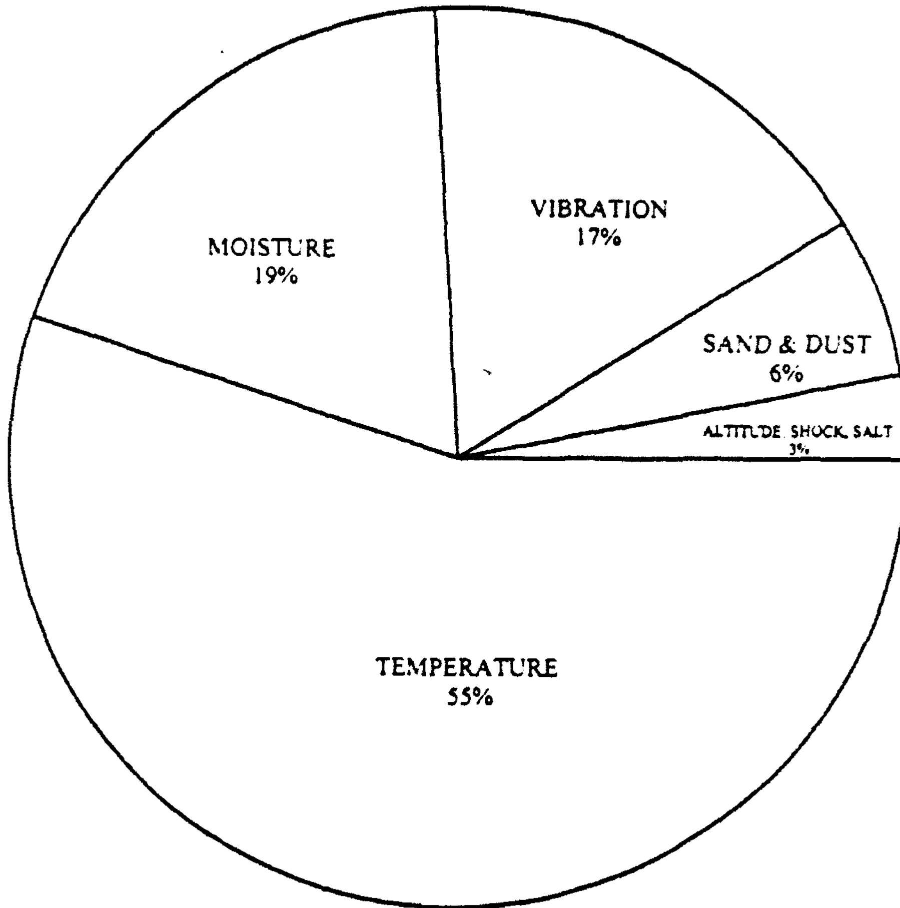


Figure A-1. Distribution of Environmentally Related Costs [Dantowitz, et al. 1971]

TABLE A-2
Summary of Temperature, Solar Radiation, and Relative Humidity Diurnal Extremes (from U.S. Army Regulation AR 70-38)

CLIMATIC CATEGORY	OPERATIONAL CONDITIONS			STORAGE AND TRANSIT CONDITIONS	
	AMBIENT AIR TEMP. °F	SOLAR RADIATION $Btu/ft^2/hr$	AMBIENT RELATIVE HUMIDITY %	INDUCED AIR TEMP. °F	INDUCED RELATIVE HUMIDITY %
1 WET-WARM	Nearly Constant 75	Negligible	95 to 100	Nearly Constant 80	95 to 100
2 WET-HOT	78 to 95	0 to 360	75 to 100	90 to 160	10 to 85
3 HUMID-HOT COASTAL DESERT	85 to 100	0 to 360	63 to 90	90 to 160	10 to 85
4 HOT-DRY	90 to 125	0 to 360	5 to 20	90 to 160	2 to 50
5 INTERMEDI-ATE HOT-DRY	70 to 110	0 to 360	20 to 85	70 to 145	5 to 50
6 INTERMEDI-ATE COLD	-5 to 125	Negligible	Tending toward saturation	-10 to -30	Tending toward saturation
7 COLD	-35 to -50	Negligible	Tending toward saturation	-35 to -50	Tending toward saturation
8 EXTREME COLD	-60 to -70	Negligible	Tending toward saturation	-60 to -70	Tending toward saturation

providing useful background data relevant to missile storage environments include [Riordan 1974; Ohman 1973; Blackford and McPhilimy 1972; Viletto 1973; Williams 1972; and Westbrook 1969]. Other worldwide temperature data are contained in a report by Stokes and Jorgensen [1962]. The military standard for climatic extremes are contained in MIL-STD-210B [Department of Defense 1973] which lists extreme values of quantities such as temperature, absolute and relative humidity, solar radiation, rain, snow, wind, and atmospheric pressure. The data contained in these weather summaries provide a basis for estimating the general environmental conditions of military equipment according to location.

The various elements which influence the temperature of a missile have been assigned the term "thermal forcing functions" by Ulrich and Schafer [1970, 1971, 1977]. Thermal forcing functions considered by these workers include:

- Direct radiation from the sun;
- Reflected solar radiation from the atmosphere;
- Reflected solar radiation from the ground;
- Convective heat from or to the ambient air; and
- Heat transfer resulting from precipitation.

These functions have both directional and time dependence. A missile mass exhibits a "thermal response" to the forcing function in terms of such measured thermal parameters as [Department of the Navy 1975]:

- Maximum surface temperature;
- Temperature-time variation at a few discrete points on and within the body;
- Maximum temperature gradients;
- Average or bulk temperature; and
- Possible local or average heat flux.

Part of the critical information needed for considering potential storage degradation processes in missile materials is the thermal response of the missile mass to the thermal forcing function.

The information in the weather documents referenced above permit correlations to be made between various extremes. For example, very high temperatures and high humidity do not occur simultaneously. The highest temperature at which a 100 percent relative humidity has been recorded over the ground is 84 °F and near the ocean surface only 93 °F. The lowest recorded humidity of 2% occurred at 100 °F [Department of Defense 1973]. The chart shown in Figure A-2 summarizes likely relative humidity values for a range of air temperatures in worldwide environments. MIL-STD-210B

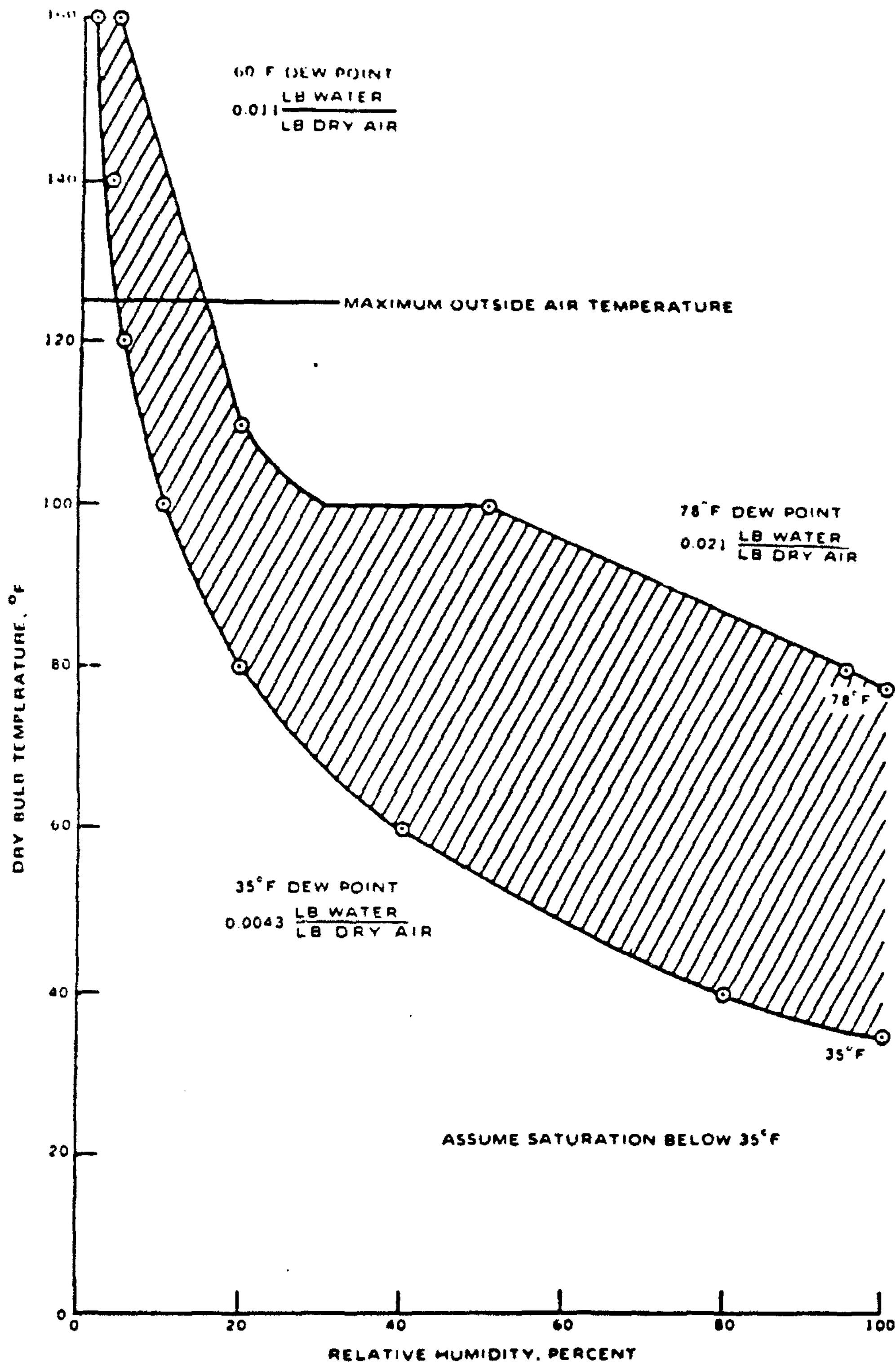


Figure A-2. Worldwide Humidity Environment From "Environmental Criteria and Guidelines for Air-Launched Weapons" [Department of the Navy, 17 June 1975 and Schafer 1968]

provides climatic extremes of military equipment in terms of the possibility that a particular extreme value will occur at a single location anywhere on earth. The highest recorded air temperature is 136 °F or 58 °C. However the 1, 5, and 10 % extreme high temperatures are listed at 120 °F (49 °C), 115 °F (46 °C), and 113 °F (45 °C), respectively. The lowest recorded temperature is -90 °F or -68 °C whereas the 1, 5, and 10 % extreme low temperatures are -78 °F (-61 °C), -70 °F (-57 °C), and -65 °F (-54 °C), respectively. These values would represent thermal forcing functions whereas the all-important thermal response of a particular missile system will be determined by specific structural and materials details. The listed percentages correspond to the relative amount of time the respective temperature extremes will be exceeded in an extreme environment. Equipment is not normally designed to survive extreme environmental values but rather a certain specified percentage criteria.

MIL-STD-1670(A) [Department of the Navy 1975], "Environment Criteria and Guidelines for Air-Launched Weapons," contains valuable design criteria for a wide range of possible environments seen by Navy missiles, much of which are of interest to the Army as well. This document lists the following situation-dependent environments:

1. Temperature
2. Humidity
3. Precipitation
4. Small Particulate Matter
5. Sand and Dirt
6. Wind
7. Pressure
8. Corrosion
9. Dissociated Gases
10. Fungus
11. Solar Radiation
12. Electrostatic

The transportation and storage situations of interest here include:

A. Transportation and Handling
   1. Flatbed Truck (exposed)
   2. Van Truck
   3. Box Car
   4. Flat Car
   5. Handling Equipment

6. Exposure on Deck of Cargo Ship
7. Hold of Cargo Ship
8. Hardstand
9. Cargo Aircraft

B. Storage and Handling

1. Igloo Magazine
2. Uninsulated Sheet Metal Building
3. Roofed Structure with no Sidewalls
4. Dump Storage (exposed)
5. Dump Storage (revetment)
6. Railroad Siding

A severe storage situation occurs when missiles must be kept in an open storage dump. Dump storage is usually necessary when an Army must operate under mobile circumstances or in a new location outside the United States. In addition, the purpose of certain missiles such as HAWK requires some units to be in ready condition at all times. Solar radiation raises the temperature considerably above the ambient air temperature. The daily extremes over a one-year period for the skin of a Navy SPARROW container at China Lake is shown in Figure A-3. The skin temperature is seen to vary more than 100 °F on some days. Even on cold days variations greater than 60 °F are common. Daily temperatures of the skin of a SPARROW Rocket Motor are shown in Figure A-4 for a year. A thermal inertia is associated with the heat capacity of a relatively massive rocket motor. One important consequence of a large thermal mass being located with a container is to introduce a phase difference between the temperatures of the container and the missile. The rocket itself never reaches container extremes. These effects are clearly illustrated in Figure A-5 by Schafer's data showing hourly temperature measurements taken at the container skin, at just inside the motor and at the center of the grain.

Although these curves are not for electronic parts, the temperature, as expected, varies less as measurements are made closer to the center of the mass and are representative of that expected of the guidance control package. Temperature profiles are out of phase so that the propellant achieves its maximum temperatures well after the hottest time of the day. The ideal situation is for the internal missile temperature to have a twelve-hour phase difference with the container skin which is achieved with the container designed for the PATRIOT missile. By directing attention to the rate of heat transfer, radiation, convection, etc., into and out of the container, it should be possible to develop data and procedures for evaluating temperature profiles of ordnance based on surface characteristics and the thermal properties of the missile. The cumulative

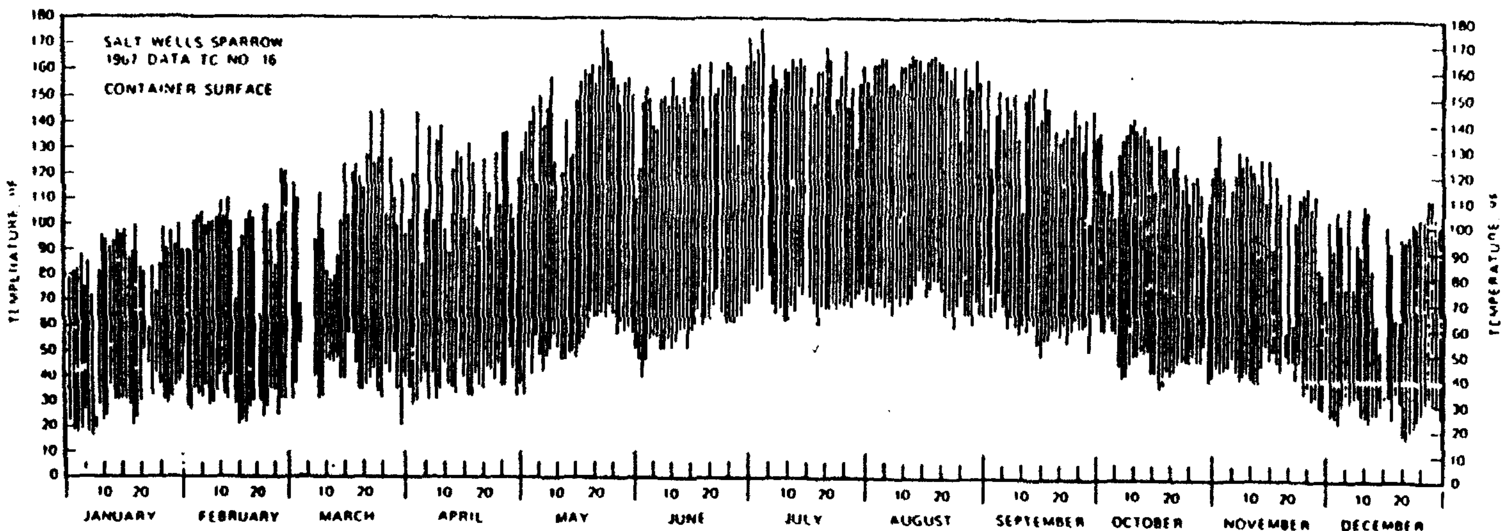


Figure A-3. Temperature Profile of SPARROW Shipping Container Skin Dump-Stored at NWC - 1967 [Schafer, 1972]

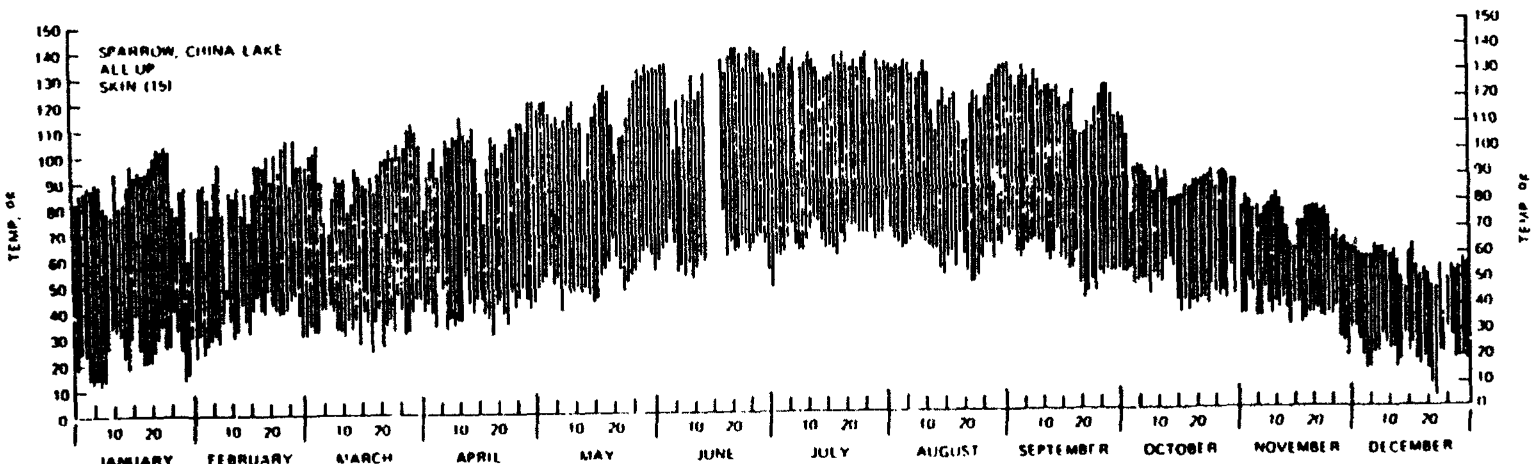


Figure A-4. Temperature Profile of SPARROW Rocket Motor Skin, Dump-Stored at NWC as an All-Up Round - 1968 [Schafer 1972]

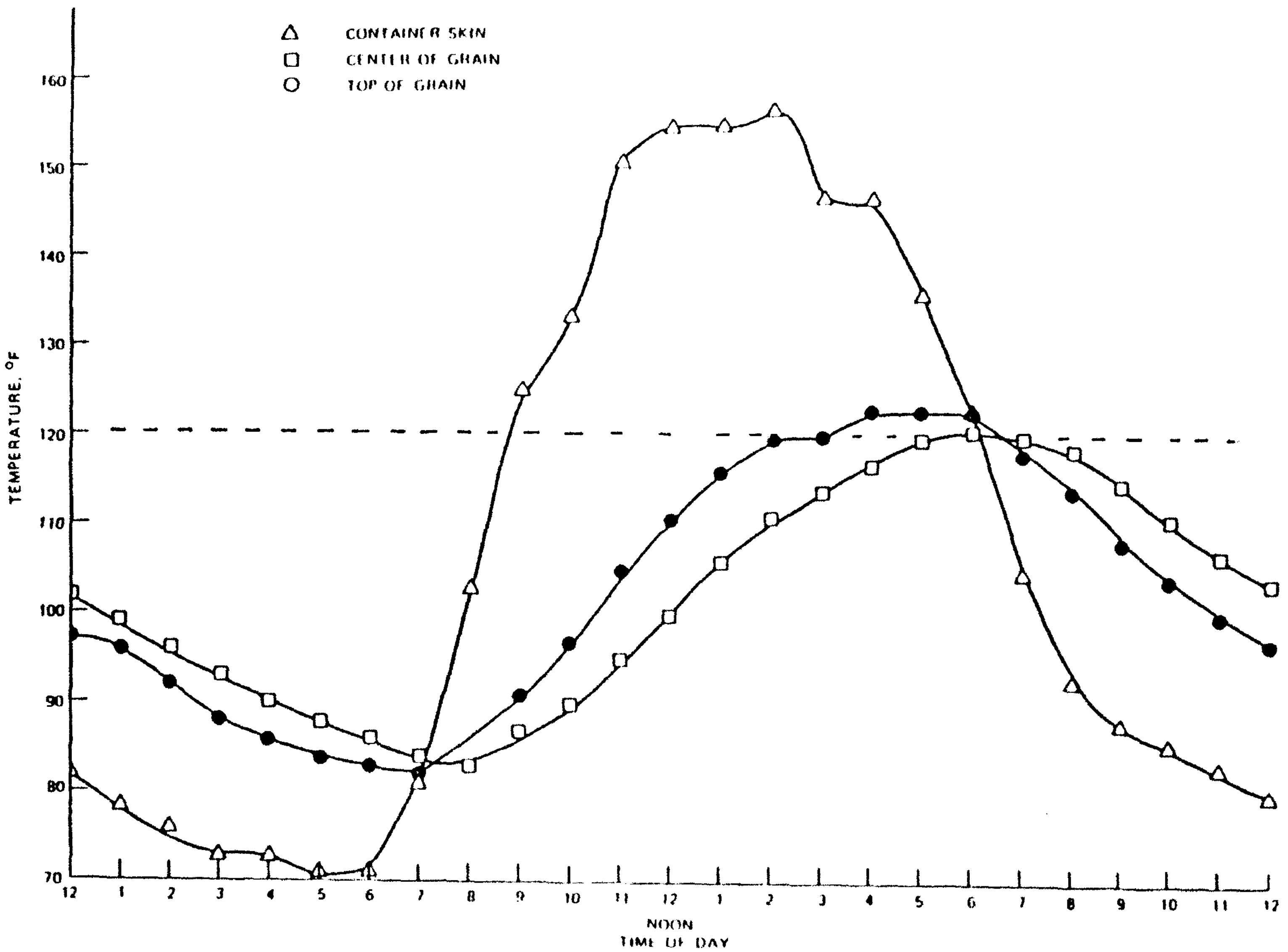


Figure A-5. Temperature Profiles of SPARROW Motor in Shipping Container for 31 July 1969 [Schafer 1972]

distributions over a year of temperatures of a larger (12 inch diameter) missile are shown in Figure A-6 for a missile dump stored in the Philippines. The effect of the missile's large thermal mass is clearly seen in a statistical manner by the relatively lower temperatures experienced within the missile mass.

Temperature profiles for CHAPARRAL missiles exposed to the environment at Yuma, Arizona, have been comprehensively investigated by Mitchell [1973]. Data from the skin of a CHAPARRAL mounted on launch rails are shown in Figure A-7. A comparison of the outer skin and inner temperatures over a single day for an exposed CHAPARRAL near the ground is seen in Figure A-8. The importance of thermal mass and the container is clearly seen by comparing Figure A-8 with the SPARROW data of Figure A-5. The cumulative temperature distribution for a launch rail mounted CHAPARRAL taken at various points within the electronics package is provided in Figure A-9. A summary of Mitchell's CHAPARRAL measurements [1973] showing maximum temperatures achieved on launch rails are provided in Table A-3.

Factors such as the paint color strongly influence weapon temperatures. Schafer compared maximum temperatures for fuel air explosive weapons painted olive drab and white. His data showed that white paint reduced the weapon temperature as much as 30-35 °F. Similar conclusions are well represented in the China Lake data [Schafer 1977] shown in Figure A-10.

Magazine Storage

Almost any type of cover will be a strong aid for protecting equipment from ambient temperature extremes. The insulation of trapped air and heat capacity of the air and stored equipment is effective for moderating diurnal temperature cycling. Earth-covered, concrete magazines are particularly effective due to the additional insulation and large heat capacity of the earth. Earth-covered magazines have been shown to reduce daily temperature amplitudes within the magazine as much as 1/20 of the external ambient amplitude. However, the actual internal temperatures follow the mean external values.

Figure A-11 presents data taken over a several-year period from magazines in Iceland. The average monthly maximum and minimum temperatures are shown as separate curves. The benefit of the earth covering is shown by the almost three to one decrease in temperature variations for earth-covered relative to uncovered magazines.

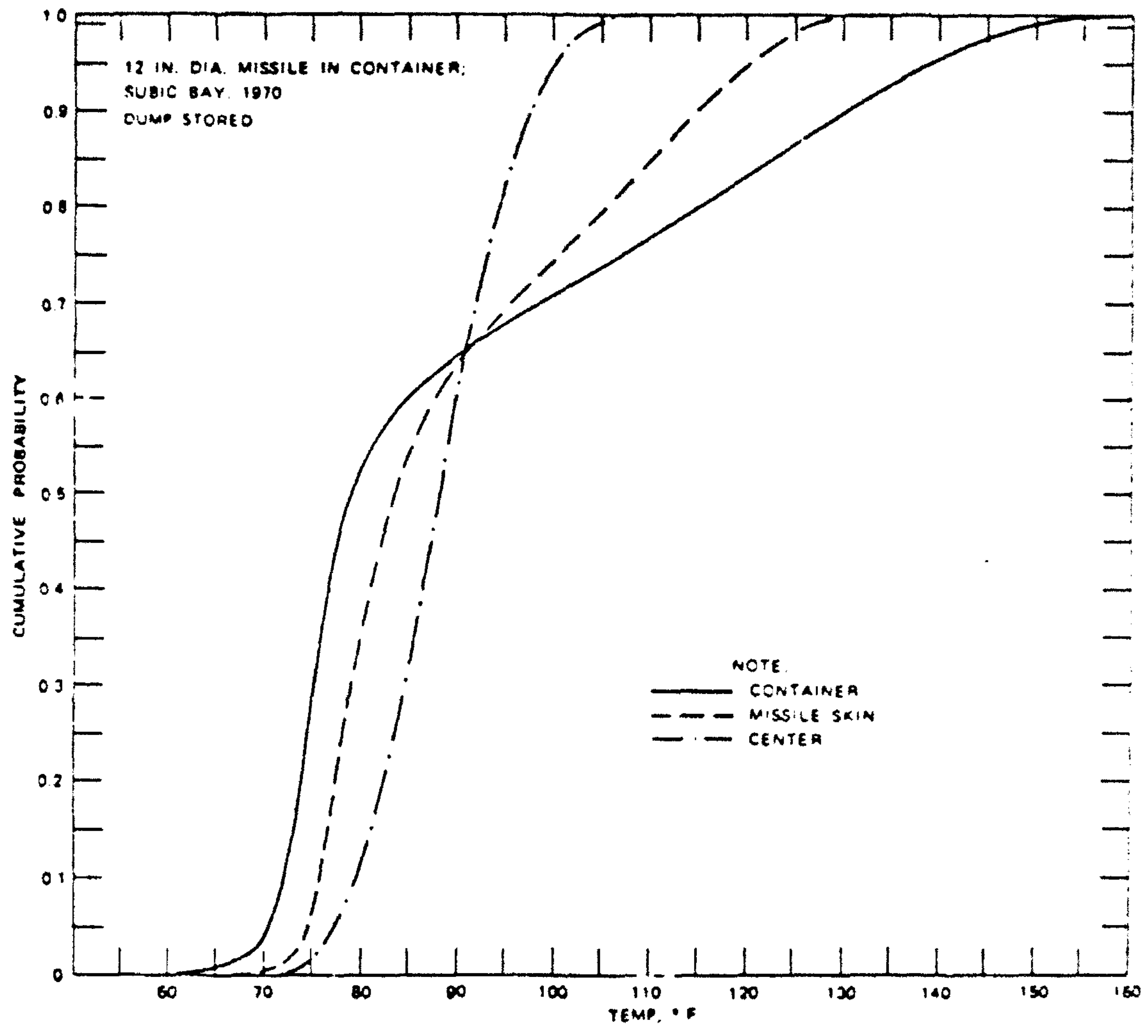


Figure A-6. Cumulative Distribution Summary of Dump Stored ASROC Temperatures at Subic Bay for 1970 [Schafer 1972]

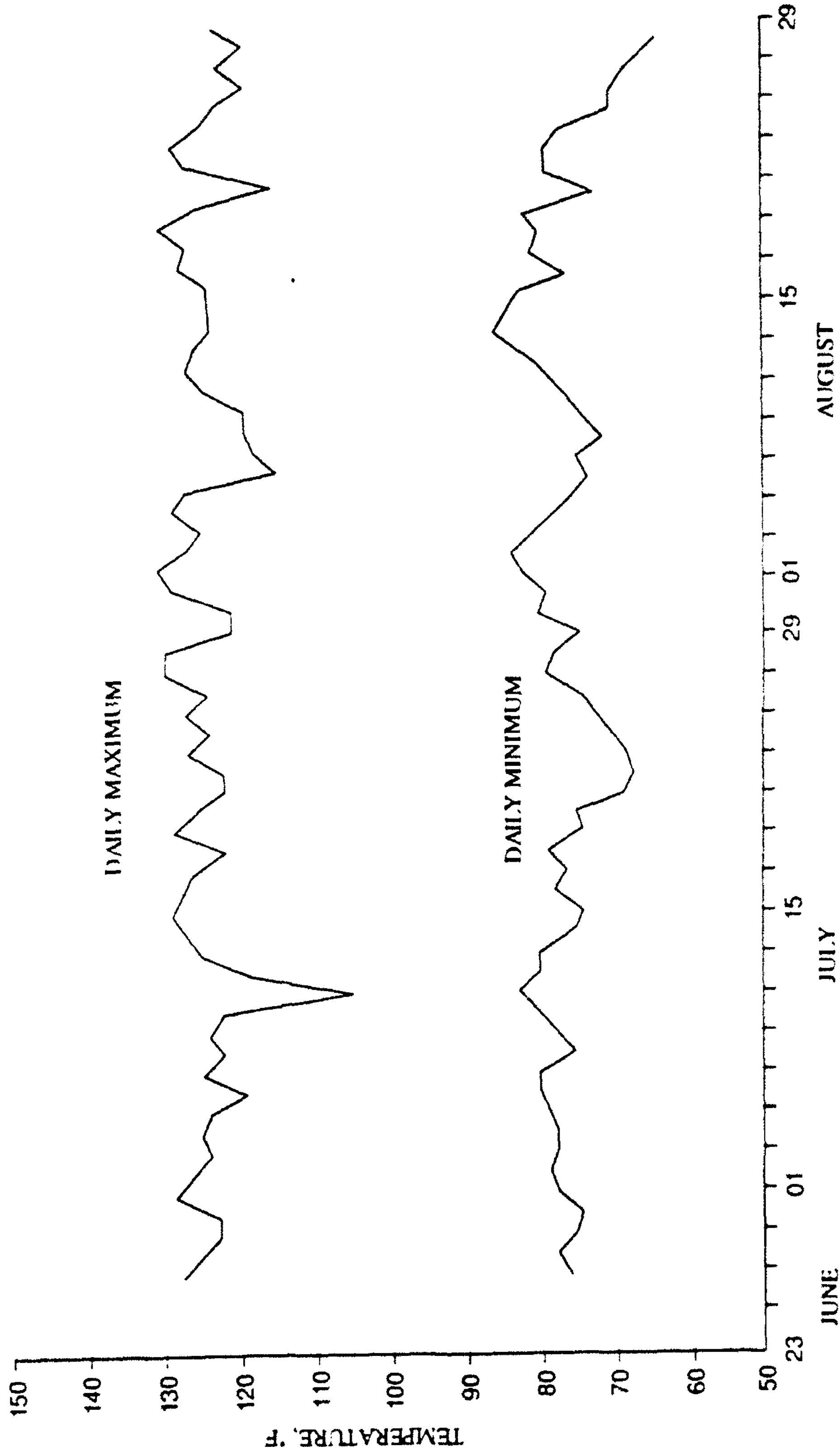


Figure A-7. Temperature Profile of a CHAPARRAL Mi[illegible]le Skin, Eight Inches from Aft Flange, August 1973 [Mitchell 1973]

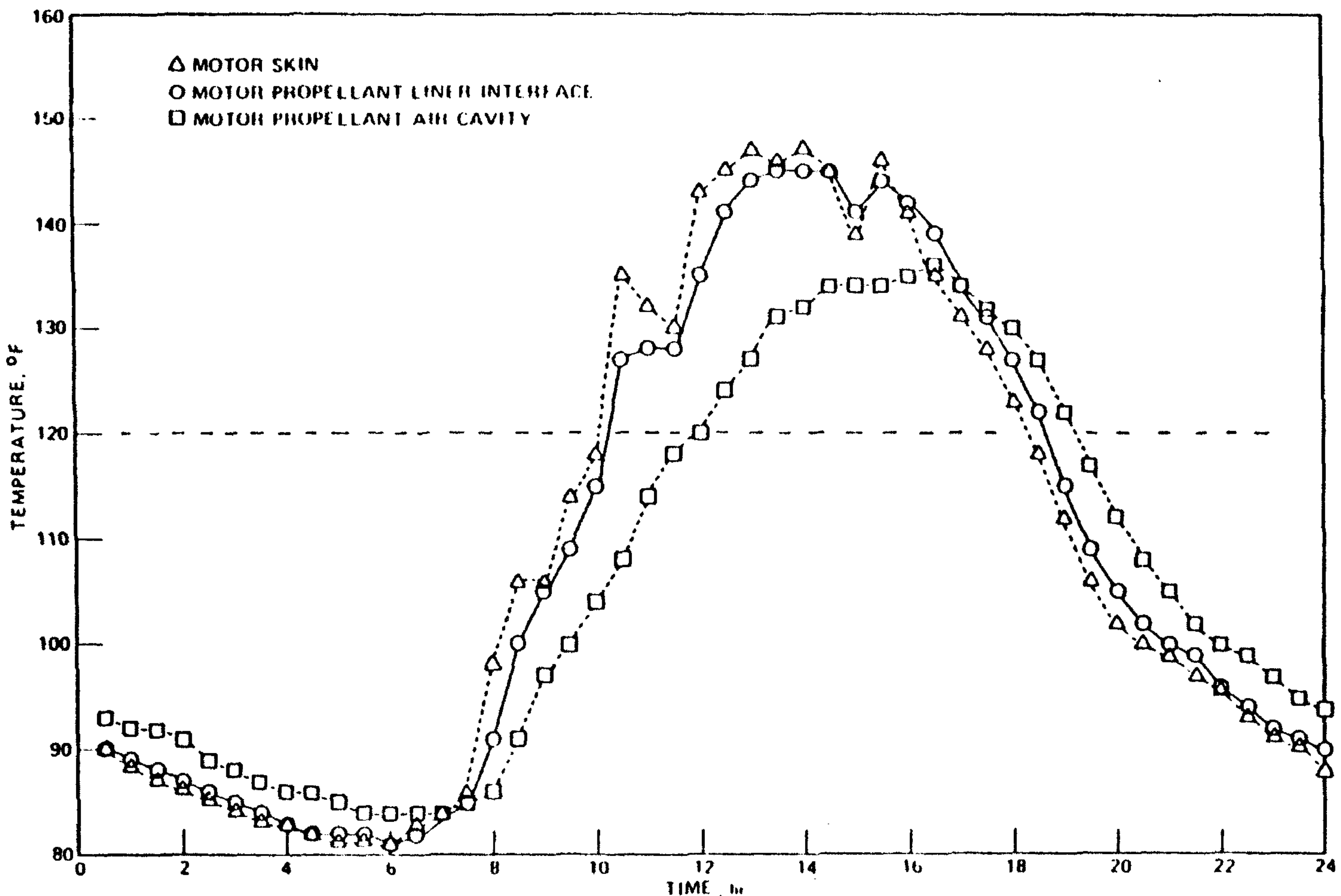


Figure A-8. Diurnal Temperature Cycles of a CHAPARRAL Missile, 1 August 1973. Temperature Readings at Three Indicated Locations [Mitchell 1973]

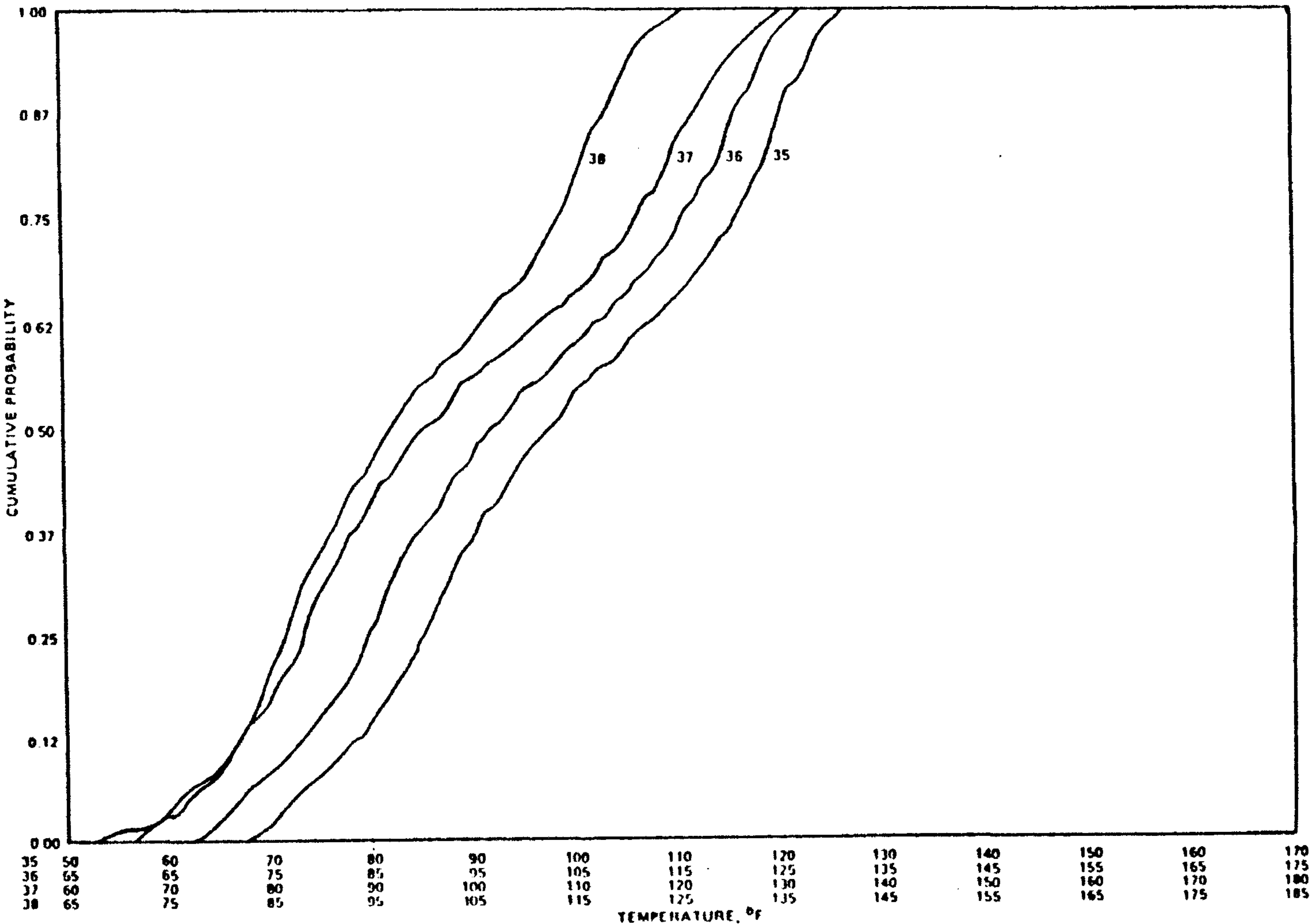


Figure A-9. Cumulative Temperature Distribution for CHAPARRAL Missile at Four Regions: Seeker Section (T.C. 35), Precision Amp Transistor (T.C. 36), Electronic Section, Skin (intrior) (T.C. 37), and Electronics Section, Skin (interior) (T.C. 38) [Mitchell 1973]

TABLE A-3 Maximum Temperatures Recorded for CHAPARRAL Missiles on Launch Rails, Solar Radiation at Yuma, AZ [Mitchell 1973]

Location	T.C. No.	Temperature (°F)	Missile No.	Launcher Position	One Date (1973)
Motor					
Skin	43	140	1	1	Aug 22
Propellant-liner interface	47	136	2	1	Aug 22
Propellant air cavity	51	126	2	1	Aug 22
Warhead					
Skin	89	132	4	1	Aug 1
Explosive-liner interface	68	123	2	2	Aug 1
Explosive center	84	122	3	2	Jul 2
TDD					
Skin	76	132	2	2	Aug 1
GCG, Not Operating					
Skin	77	131	2	2	Aug 1
Seeker sect (flask holder)	35	128	1	4	Aug 11
Precision amp transistor	36	128	1	4	Aug 16
Elect sect skin (interior)	37	129	1	2	Aug 5
Elect sect skin (interior)	38	127	1	4	Aug 11
Elect sect ambient air	39	128	1	2	Aug 27
Elect sect ambient air	40	122	1	1	Aug 18
Servo sect ambient air	41	122	1	4	Aug 11
Cylinder block	42	122	1	4	Aug 11
Elect sect ambient air	16	121	1	4	Aug 11
GCG, Operating					
Seeker sect (flask holder)	35	175	1	3	Aug 7
Precision amp transistor	36	155	1	3	Aug 7
Elect sect skin (interior)	37	138	1	4	Jul 25
Elect sect skin (interior)	38	134	1	4	Jul 25
Elect sect ambient air	39	157	1	2	Aug 1
Elect sect ambient air	40	178	1	3	Aug 7
Servo sect ambient air	41	124	1	4	Jul 25
Cylinder block	42	124	1	2	Aug 1
Elect sect ambient air	16	149	1	3	Aug 7

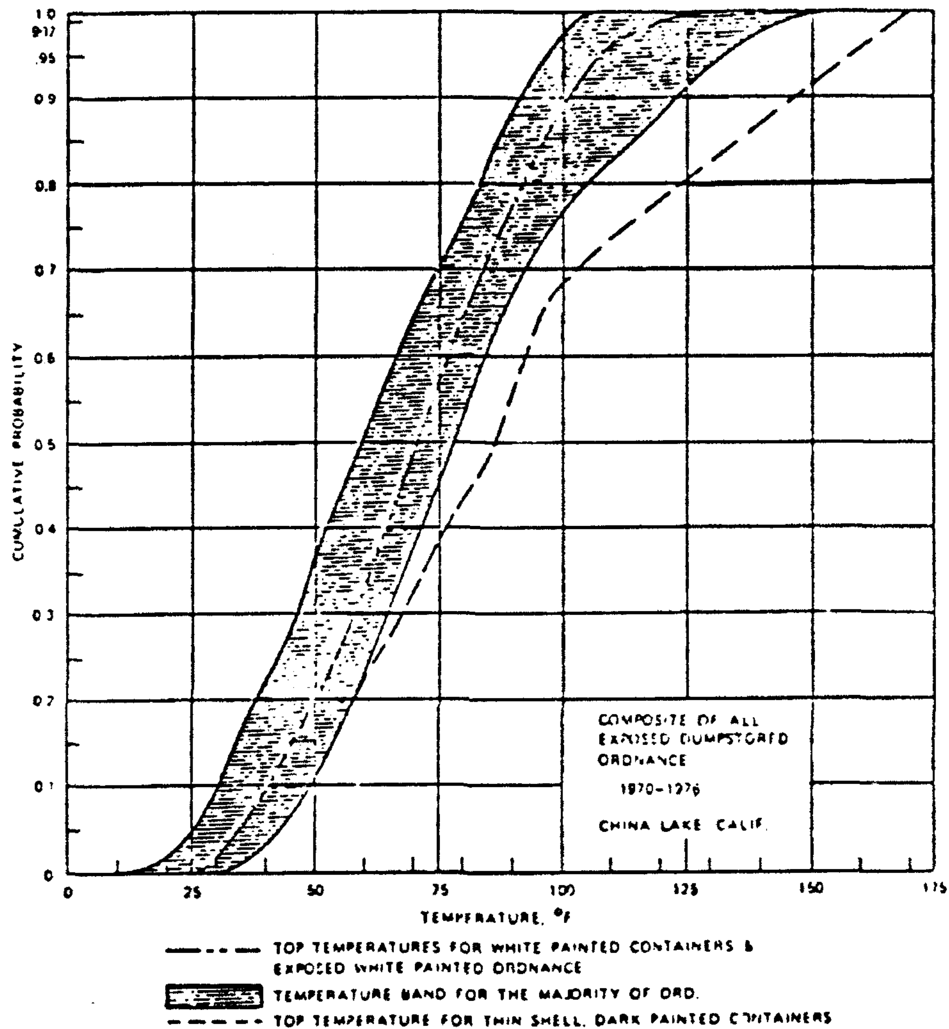
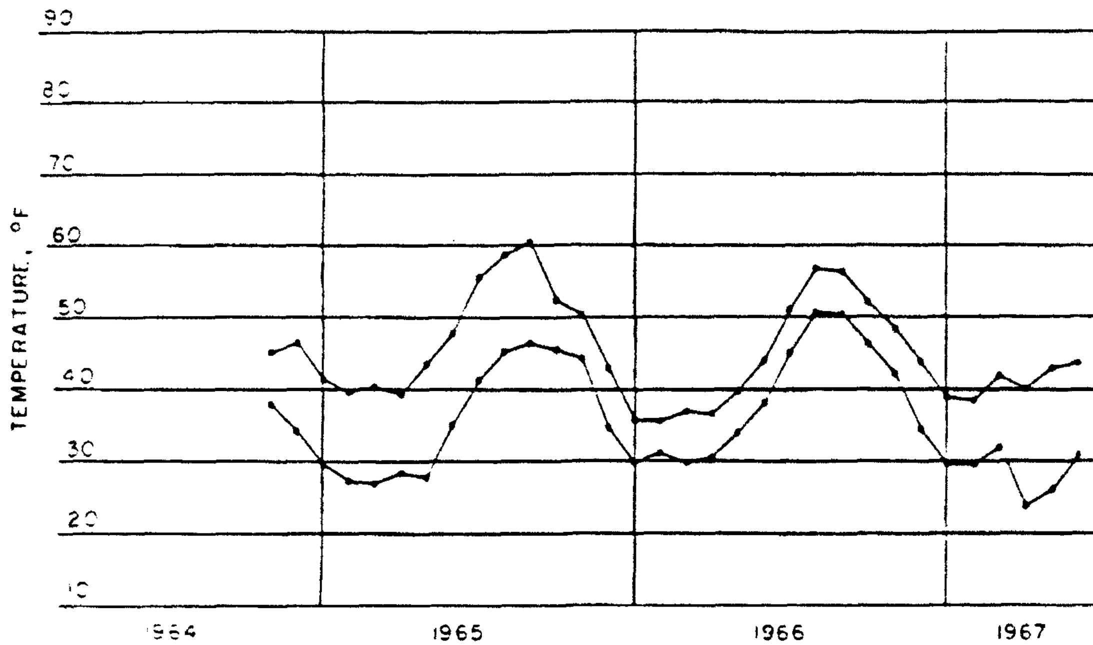
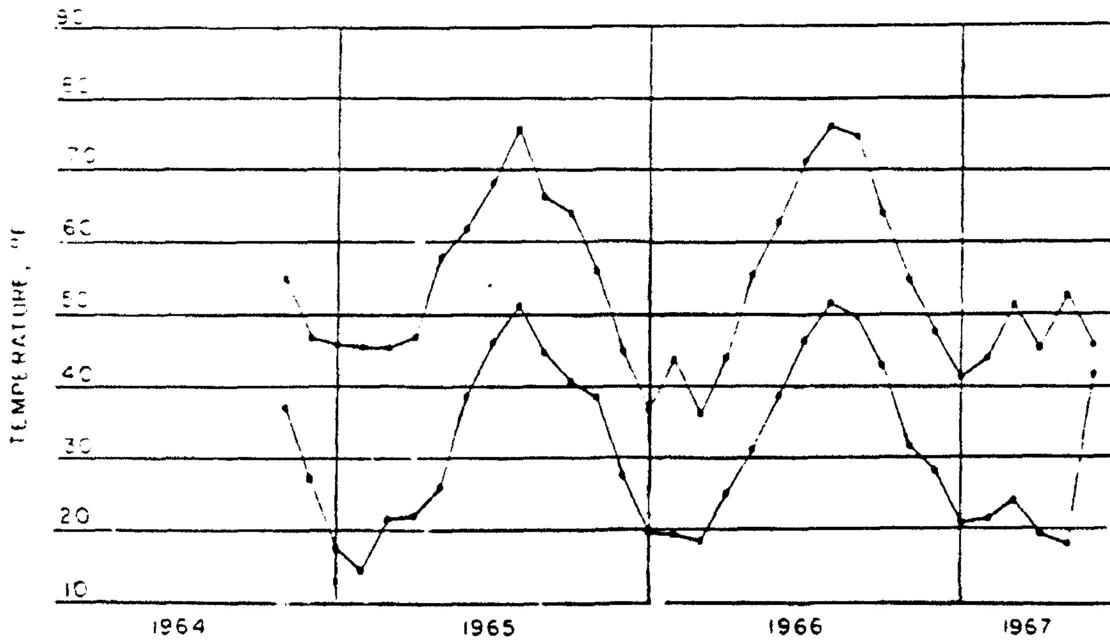


Figure A-10. Composite of All Dump-Stored Ordnance at China Lake NWC, 1970-1976 [Schafer 1977]



The Average Maximum and the Average Minimum Temperatures of Earth-Covered Magazines at NS, Keflavik, Iceland.



The Average Maximum and the Average Minimum Temperatures of Non Earth-Covered Magazines at NS, Keflavik, Iceland

Figure A-11. [Kurotori and Schafer 1970]

Transportation of Missiles

A last major area of concern is the environment seen by a missile during normal transportation. An Army tactical missile may have to be moved to many parts of the world during its storage life. There is no way to predict how often a missile will be moved or to what locations since such movements will be determined by international events.

For missiles transported within the hold of a ship, [Taylor and Schafer 1967 and 1969] temperatures cannot vary greatly because of the stabilizing effect of the ocean. However, the humidity will always be high. Therefore the concern for missiles transported by ship is directed toward the possible introduction of moisture with only moderate temperatures and temperature variation expected.

Studies of temperature profiles of air transported materials also show that temperature problems are not severe. In a case where the heating system of the airplane in very cold conditions was intentionally cut down to simulate partial failure, the temperature of the cargo remained at relatively high values. These data taken from a C-141 flight are shown in Figure A-12. The outside temperature on this flight approached -70 °F but the heat capacity of the cargo, coupled with what heating remained, maintained the cargo within the temperature envelope shown above about 40 ° F. Note that the cargo compartment floor did go down to about 5 °F. Measurements on other flights were less severe as far as lowering the temperature of the cargo due to the flight itself is concerned. Based on these data, it appears that the movement of missiles in normal air transports will not introduce low cargo temperatures anywhere near approaching the very cold values of the outside air at high flying altitudes as indicated in MIL-STD-210B. The recorded temperature of the cargo floor indicates severe extremes will probably never occur. Schafer noted that the lowest cargo temperature measured during his air transportation studies was only 19 °F with a true outside air temperature of -82 °F.

The decreased atmospheric pressure at high altitudes can, however, be a most significant factor. The decreased pressure will create conditions where leakage occurs through the seals of large containers. Upon returning to earth, the large pressure differential has been seen to crush large missile containers [Mitchell]. Apparently it is easier for air to escape from containers than it is to leak back in. In fact, pressure relief valves are often used which let air out when a 5 psi differential pressure occurs [Schafer]. For cases where the geometry of a container does permit air to leak back inside, a secondary problem must be considered, particularly if the landing occurs in a

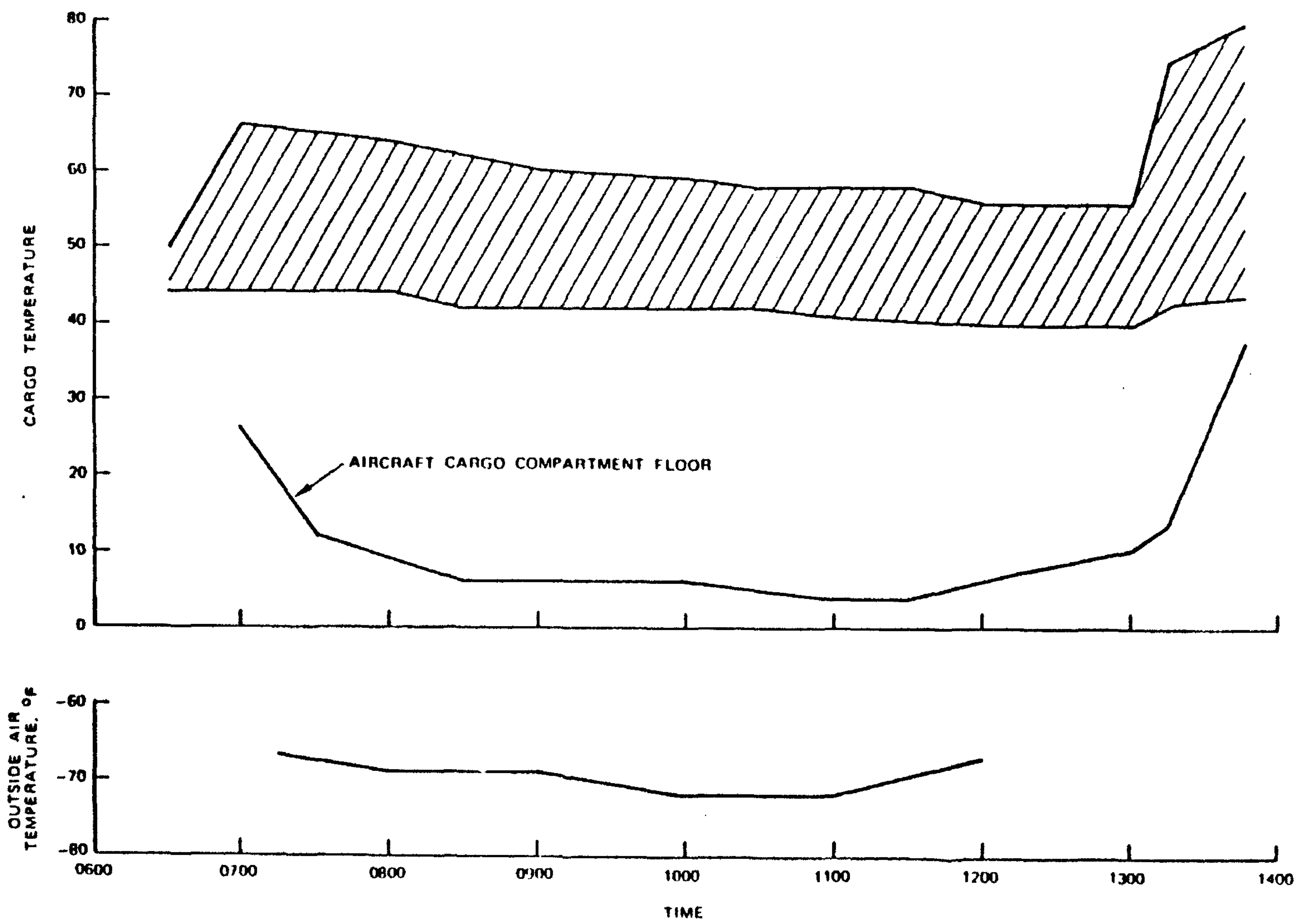


Figure A-12. C-141 Flight from McGuire AFB to Rein-Main, Germany (1/18/69). The Shaded Area is the Material Temperature Envelope [Schafer and Dickus 1970]

humid environment. The air replacing the original dry nitrogen may then contain a large amount of moisture. This effect corresponds to the problem of moisture accumulation inside a container with temperature cycling over sufficiently wide extremes to cause air exchange between the missile container and the outside air. In many cases, the missile will be at a lower temperature when the air is subsequently forced out again. The net effect is that condensation of moisture will occur on the relatively massive missile motor and the air subsequently expelled may be correspondingly lower in moisture content. Schafer has noted large quantities of water collect in sealed containers cycled under humid conditions. This factor should be of major concern for missiles which remain in storage after transportation or storage conditions which cause this water pumping mechanism to develop.

Truck and rail transportation have also been examined by the Naval Weapons Center at China Lake. A study by Martin and Schafer [1970] measured the temperature profiles of truck cargoes under both extremely cold and extremely hot weather conditions. They found that the truck enclosure offers protection from external extremes. For example, in a case where the outside temperature went to about -20 °F, the cargo temperature reached -3 °F. Corresponding extremes for hot weather tests showed that 128 °F outside air temperature resulted in only 116 °F cargo temperatures. These values are probably the most severe temperatures a missile would ever experience during transportation. Additional missile environment investigations are being conducted by personnel of the White Sands Missile Range [Huddleston]. They have been concerned with measurements on production hardware in the field.

Fungus

Fungus can grow and become destructive to missile materials under certain conditions. As living creatures, these organisms must have food, moisture, oxygen, and a favorable temperature range. Clossmyer [private communication] identifies the ideal temperatures as 20-40 °C and the optimum relative humidity as 85-100%. The food may be a contaminant or some ingredient of the missile system. The organisms are practically always present in the atmosphere with densities on the order of millions per cubic inch of air. During growth, the organisms collect minerals and become conductive for small currents. Missile materials are usually made resistant to fungus growth if the potential problem is always kept in mind by the designer and manufacturer. However, fungus problems are encountered with contaminants, improperly cured polymers, wrong paints, and poor storage conditions. Growth can spread from a susceptible material to a normally non-susceptible material [Evans]. For example, where missiles are stored

within a tropical zone under a tree canopy, materials washed from plants onto the missile storage containers by rainwater can initiate fungus attack. The key to avoiding fungus problems in storage is to employ recommended materials for fabrication and keep the missile dry. The organisms certainly will not grow in a nitrogen atmosphere and if the relative humidity is less than 50% inside the missile container, the potential for growth is small [Clossmyer].

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APPENDIX B: MATERIALS PROPERTIES

Figure B-1 COEFFICIENT OF THERMAL EXPANSION FOR SELECTED MCM CANDIDATE MATERIALS

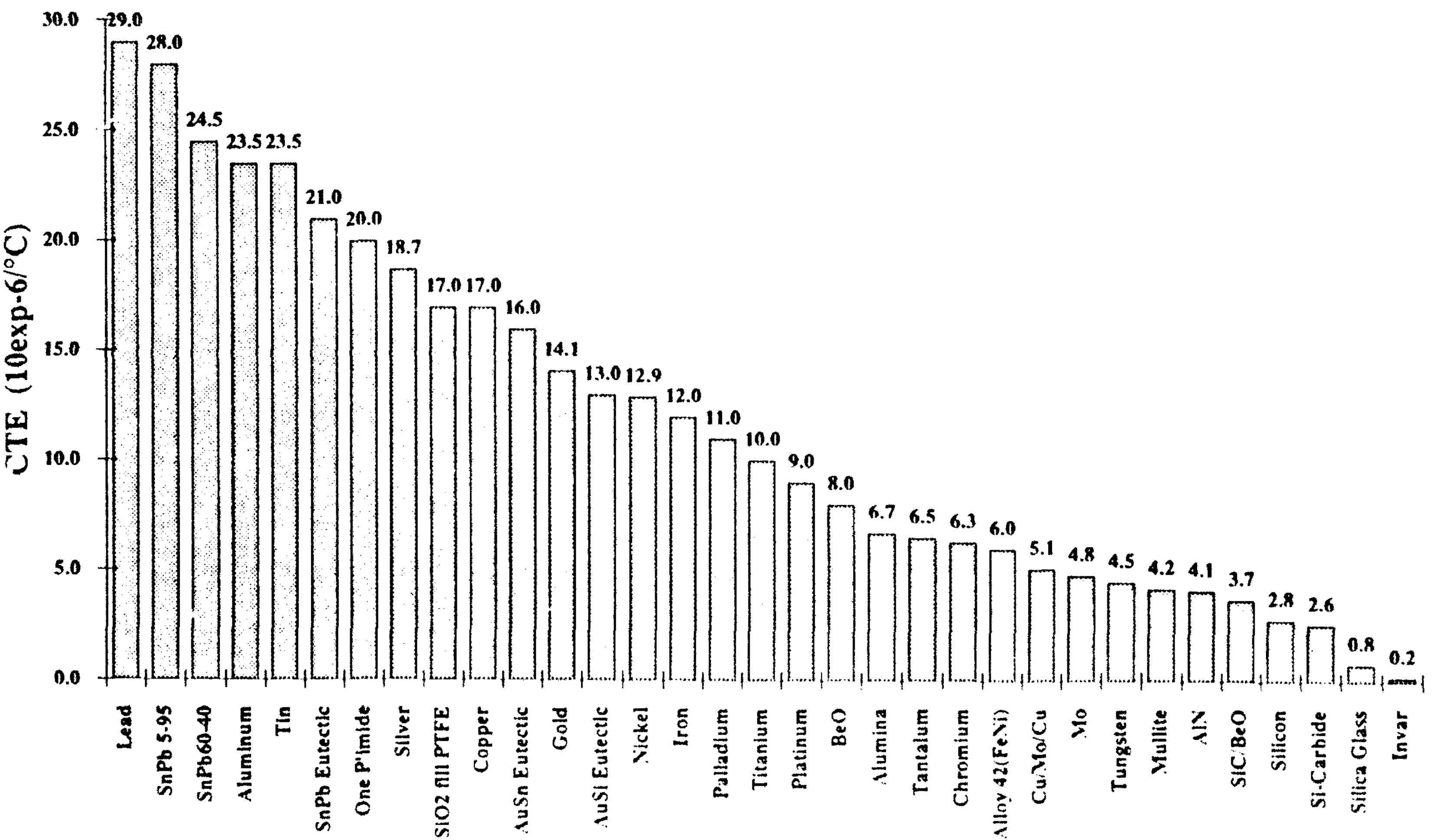


Figure B-2 COEFFICIENTS OF THERMAL EXPANSION OF SEVERAL SEMICONDUCTORS; at 23°C and at 200°C

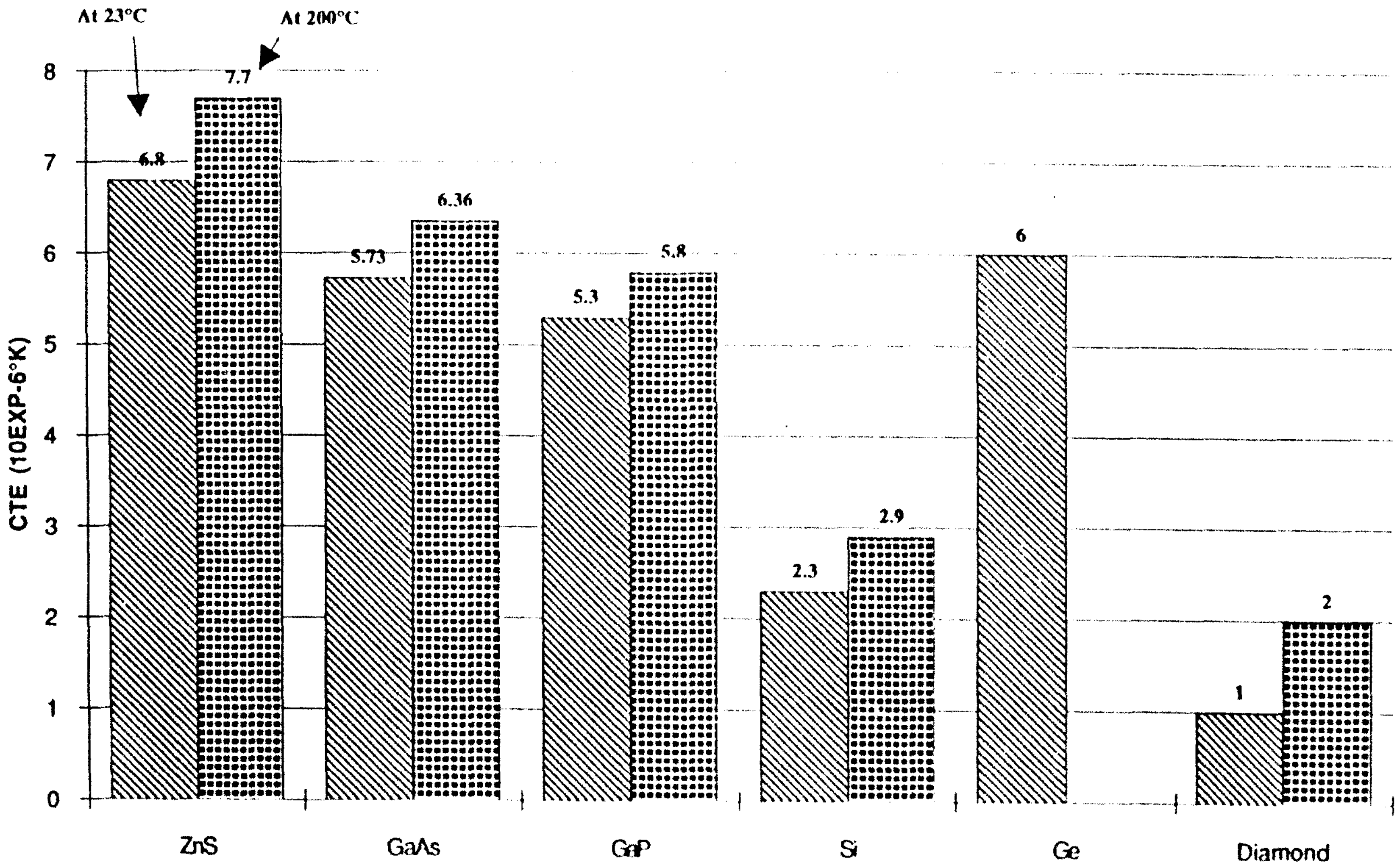


Figure B-3 FLEXURE STRENGTHS OF SEVERAL SEMICONDUCTORS

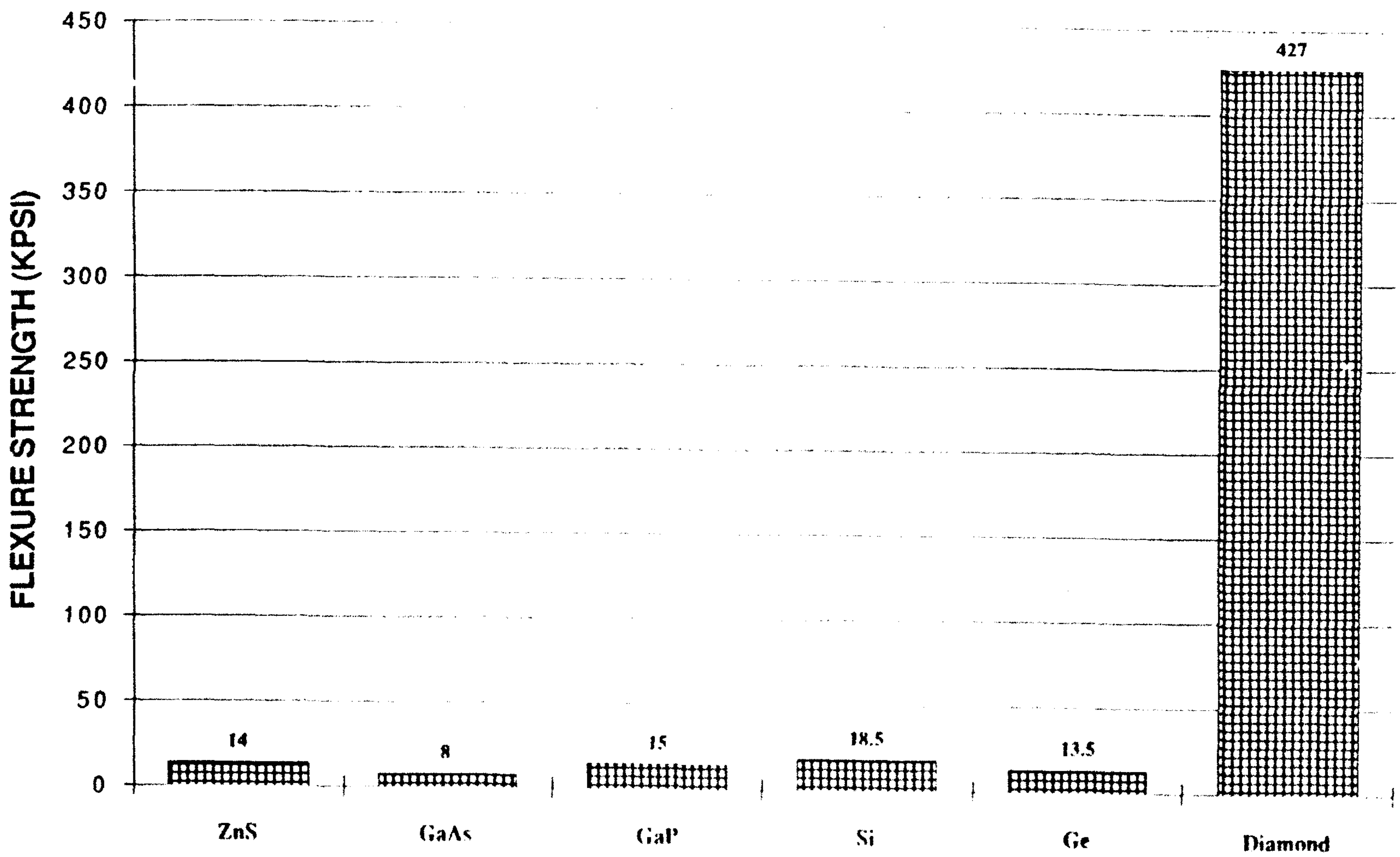


Figure B-4 ELECTRICAL RESISTIVITY OF SELECTED MCM METALS

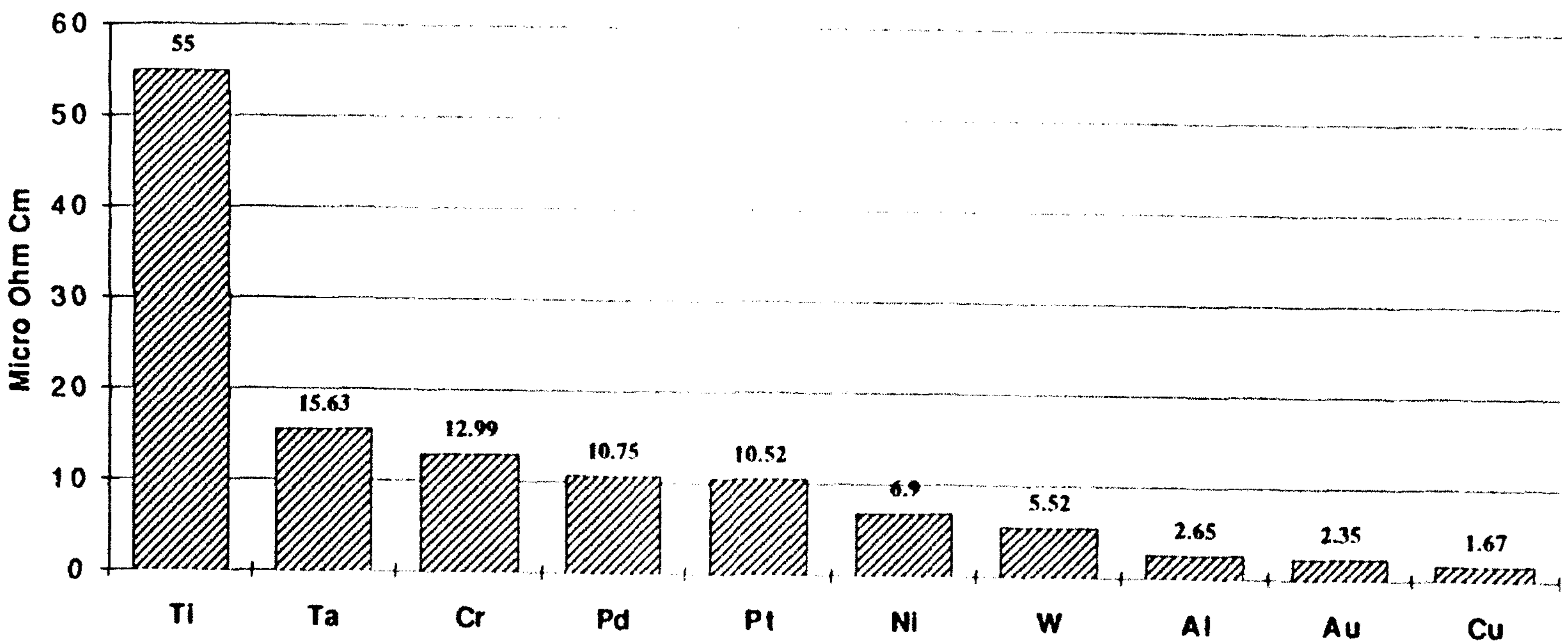


Figure B-5 THERMAL CONDUCTIVITY OF SEVERAL SUBSTRATE MATERIALS

(For comparison, diamond has a thermal conductivity of about 2600 W/m/°K.)

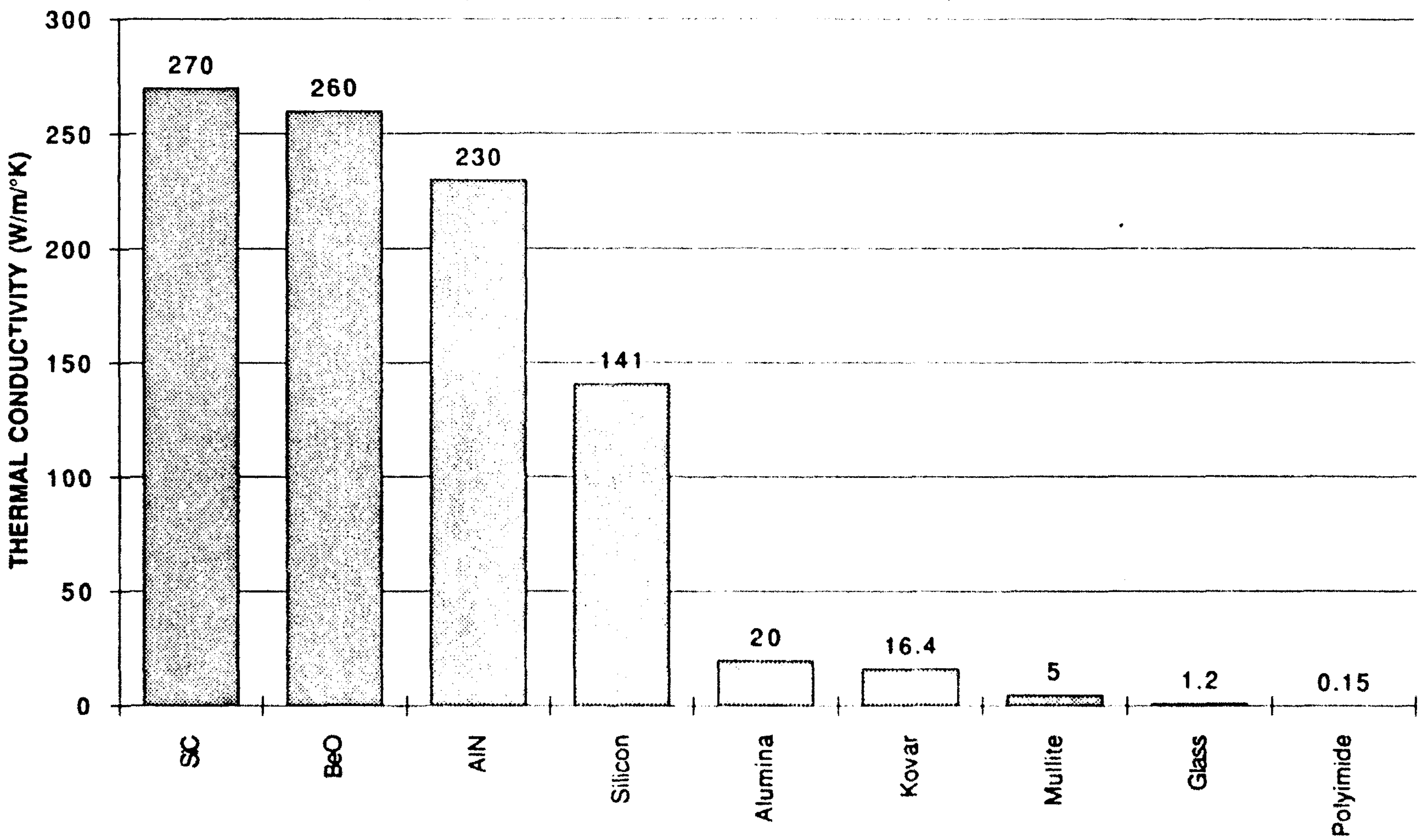
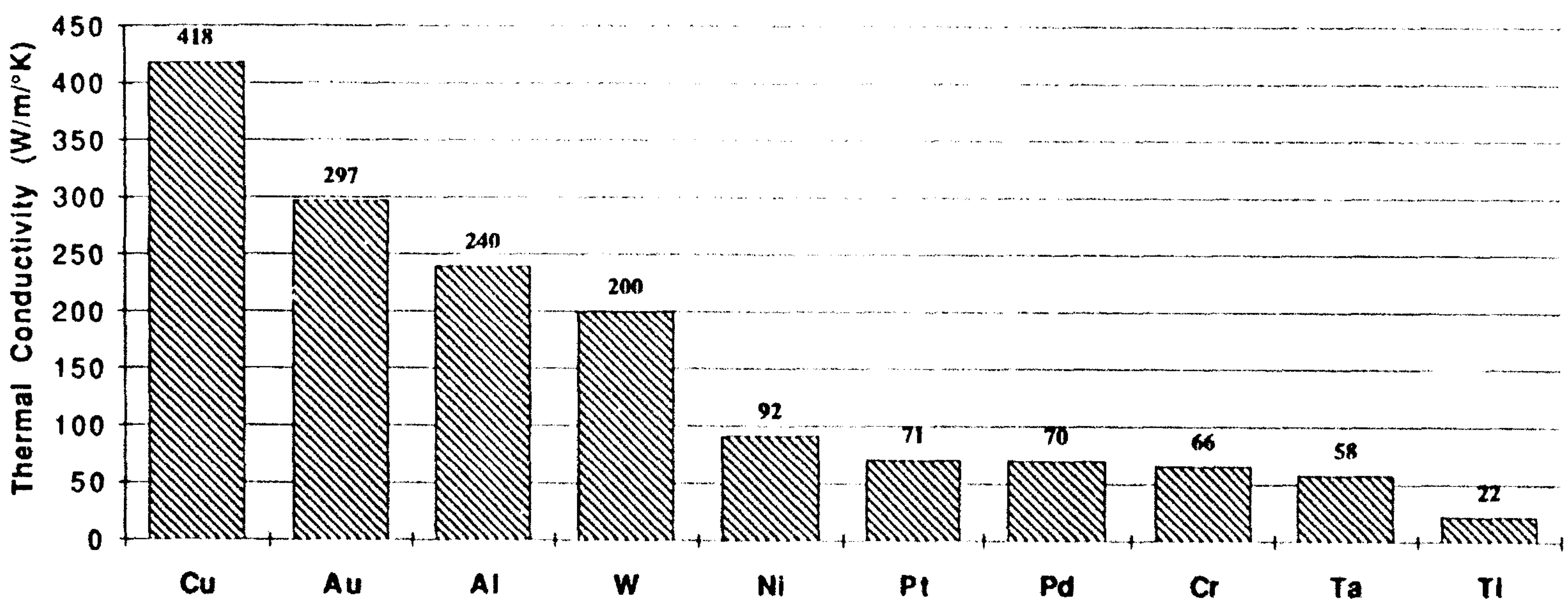


Figure B-6 THERMAL CONDUCTIVITY OF SELECTED METALS EMPLOYED FOR MCM METALLIZATION STRUCTURES



APPENDIX C: RELATED WORK

During the period of performance of the task covered in this report, members of the U.S. Army Missile Command Manufacturing Technology Division were invited to participate in meetings of the Georgia Institute of Technology Manufacturing Research Center faculty and industry affiliates. In the course of such meetings, MICOM personnel received information on an informal and as-available basis. This concerned on-going research bearing on manufacturing of electronics and microelectronics suitable for millimeter wave, infrared, and other electro-optic missile seekers and permitted an assessment by them of promising industry developments. Further appendix information is available on request, under separate cover.

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AMSMI-RD-CS-R	5
AMSMI-RD-CS-T	1
AMCPM-CF	1
AMCPM-TIIS-Q (QA/QG)	1
SFAE-MLS-AM	1
SFAE-MSL-AT	1
SFAE-SML-HD	1
SFAE-MSL-ML	1
SFAE-MSL-TO	1
SFAE-UAV-SR	1
SFAE-ASM-LS	1
SFAE-MSL-NL	1
SFAE-GPL-PA	1