APPLIED RESEARCH, INC.

CAMMS PRE & POST PROCESSING PROTOTYPE DEVELOPMENT AND IMPLEMENTATION

Contract Number:
DAAH01-89-D-0069/0169
Subcontract Task 021
Final Technical Report

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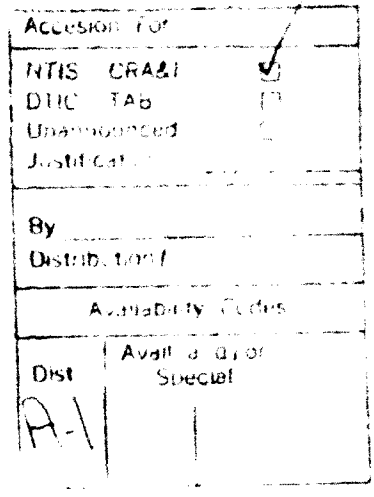

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Submitted To:
U.S. Army Missile Command-UAV
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This final report describes the support provided by ARI to Dr. Richard Sims to help redesign the video A/D system for the CAMMS program. Included in the redesign is the capability to convolve two kernels up to 7x7 size across the input image, the ability to use EE PROMS for the target filter and to post process the output correlation surface.

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1.0 INTRODUCTION

The current CAMMS Automatic Target Recognition(ATR) hardware contains a video A/D front end, a correlation engine and a microprocessor to post process the resulting correlation surface. This "minimal" configuration has been judged to be suitable for initial tests, however it is desired to be able to improve upon this configuration for later tests and analysis against more tactical targets.

Dr. Richard Sims has provided for ARI a description of the desired pre-processing prior to input to the correlation hardware and the post-processing desired after generation of the correlation surface. ARI has used this information to generate a preliminary design of the pre- and post-processing hardware. The initial implementation of this design is desired to be on an AT compatible prototype board and ARI has also supported the layout, prototyping and some fabrication of the desired circuits.

2.0 PRE-PROCESSING OVERVIEW

The preliminary design for the IBM/AT version pre-processor is detailed in the six pages of schematics in Appendix A. The intent of the IBM/AT version of electronics is to allow the user to capture RS170 images under computer control and access the preprocessed (convolved) results for analysis, evaluation and correlation reference filter synthesis. An example layout is shown in Appendix B.

The design processes the following features:

a) differential RS170 video input buffering.

b) sync and blanking generating phased to input video horizontal sync.

c) separate analog and digital grounds.

d) dual 8-bit video signal digitization.

e) real-time histogram computation.

f) microcontroller video "gain" control.

g) dual 7x7 pixel convolution with 8 bit convolution coefficients.

h) real-time modulus computation of convolver results.

i) telemetry video output of digitized video signal.

The processing of the RS170 analog video signal is depicted on page 1 of the schematics. U1 is used to differentially receive the analog video signal with a 75Ω input impedance. Components U2, U2, U8 and U13 perform the basic functions of extracting timing information from the input RS170 video. These functions include write pulse generation (WE), sync extraction (U8), pixel clock generation (U13), and pixel clock buffering and clock distribution (U15 and U16). Components U15 and U16 each show only one output being produced, PIXCLK and PIXCLK*. A total of ten outputs for each signal are available for satisfying the clock distribution requirements of this particular board. It is recommended that the exact number of outputs required of U15 and U16 be determined and defined in the prototype stage of development. Component U8 produces a 6.5 MHz pixel clock that is phased to the signal, CLAMP*, produced from the sync extraction chip, U8.

Component U10 provides the A/D processing required of the histogram chip, U11. Component U10 converts an RS170 signal to an 8-bit unsigned digital format. DC restoration occurs when the signal, CLAMPREG, is asserted. The A/D convertor will convert the DC restored signal spanning the voltage range of REFHI to REFLO. The signals REFHI and REFLO are to be held constant over the operating time of the preprocessor. Component U11 implements a real-time histogram function. The buffered results of U11 are accessible to the on-board micro-controller (U51).

Component, U9, converts the input RS170 video to digital format. Voltage references VREFHI and VREFLO are produced by the micro controller circuitry in a dynamic fashion to produce the variable "gain" feature of the design. The intent of the logic is to tailor the dynamic range of the 8-bit data bus, DVID, to the dynamic range of the input video signal. The data bus, DVID, is further input to the convolvers at U19, U26, U21 and U22.

The horizontal and vertical convolution functions are described on pages 2 and 3 of the electrical schematics. The horizontal convolution is implemented by U19 and U20. Component U19 produces the eight lines of delay required of the convolver at U20. The eight lines of delay are generated inside the component using 8-bit shift resisters configured to produce delays of 256 pixels per line. The delay line chip at U19 is required to be initialized by the micro controller. The component, U20 computes the real-time convolution of the data produced by component U19. The exact size of the convolution is determined when the micro controller preloads the convolution data. The device inherently implements an 8x8 pixel convolution. TO produce a 7x7 pixel convolution the coefficient registers in excess must be loaded with zeroes. The convolution output is produced as a 16-bit result on data bus DH.

The vertical convolution functions are depicted on page 3 of the schematics. The function and processing of the vertical convolution is the same as the horizontal convolution with the exception of the convolution coefficient values. The modulus computer (PDSP163301) computes the modulus of the output of the intermediate RAM buffer.

Page 4 of the schematics details the IBM/AT interface. The component at U27 decodes the address signals SA16 - SA19 and LA17 -LA23 to generate the chip selects required to read the 256x256 16-bit result of the preprocessing. The preprocessing result can be either memory mapped or IO mapped. The modulus RAM at U30-U35 contains the 256x256 16-bit result.

The intermediate memory storage and buffering required to implement the design is depicted on page 5 of the schematics. The right static RAM chips (CY7C191) implement an intermediate buffer between the horizontal and vertical convolution output and the modulus computation.

The micro controller circuitry is depicted on page 6 of the schematics is required to compute the dynamic digitization references VREFHI and VREFLO and the static references REFHI and REFLO for the dual A/D convertors on page 1 of the schematics. The D/A convertor at U54 converts the 8-bit digital word produced by the micro controller to an output voltage spanning 10V to 0V. The precision voltage reference at U52 produces a very precise 10V reference for the D/A convertor which will be stable under temperature. The micro controller at U51 is required for the following functions:

a) Static voltage references REFHI and REFLO.

b) Dynamic voltage references VREFHI and VREFLO.

c) 8-bit delay line initialization at U19 and U20.

d) Convolver coefficient loading and initialization at U20 and U21.

3.0 POST-PROCESSING

This section discusses the hardware necessary to calculate the mean and standard deviation (stdev) of the correlation output data. These computations will be made in real-time from the outputs of the barrel shifter.

The mean calculation involves summing the output values while the stdev involves summing the difference of the outputs and the mean. This often requires the mean calculation be completed before the stdev calculation can begin. However, if the sum of the outputs and the sum of the square of the outputs are calculated in parallel, they can be combined later to complete these calculations. This will allow the mean and stdev to be computed simultaneously with the stdev calculation completed with a few simple arithmetic operations. The square root operations will be performed by the DSP board.

The stdev equation can be manipulated, as shown below, and be expressed in terms of the sum of the outputs and the sum of the square of the outputs. This derivation shows that the stdev is computed by subtracting the square of the mean from the sum of the square of the outputs, divided by the number of outputs.

$$\sigma = \sqrt{\frac{\sum_{i=1}^{N} (x_i - \bar{x})^2}{N}}$$

$$\begin{aligned}
\sigma^2 &= \frac{1}{N}\sum (x_i - \bar{x})^2 \\
&= \frac{1}{N}\sum (x_i^2 - 2\bar{x}\, x_i + \bar{x}^2) \\
&= \frac{1}{N}\sum x_i^2 - \frac{2\bar{x}}{N}\sum x_i + \frac{\bar{x}^2}{N}\sum \\
&= \frac{1}{N}\sum x_i^2 - \frac{2\bar{x}}{N}\sum x_i + \frac{\bar{x}^2}{N}N \\
&= \frac{1}{N}\sum x_i^2 - 2\bar{x}\bar{x} + \bar{x}^2 \\
&= \frac{1}{N}\sum x_i^2 - 2\bar{x}^2 + \bar{x}^2 \\
&= \frac{1}{N}\sum x_i^2 - \bar{x}^2 \\
&= \frac{1}{N}\sum x_i^2 - \frac{\sum x_i}{N}\ \frac{\sum x_i}{N}
\end{aligned}$$

These computations are accomplished in hardware using two Multiply Accumulators (MACs) as shown in Figure 3.0-1. The internal accumulators must be sufficiently large as to allow the summations to be performed without overflow. The MAC used to compute the sum of the outputs requires a 32-bit accumulator. The MAC used to sum the square of the outputs requires a 44-bit accumulator. This is shown with the following calculations. These calculations are based on 256x256/16-bit 2's complement outputs. Although the outputs should neither be all max positive or all max negative, hardware was chosen to accommodate these worst case conditions. Mean and stdev estimations could be performed with current CAMMS hardware.

Sum of the outputs:

256x256x32768 = 2^8*2^8*2^15 = 2^31

256x256x32768x32768 = 2^8*2^8*2^15*2^15 = 2^44

A Cypress CY7C510 MAC is suggested for the first calculation. This part has a 35-bit accumulator and was previously used on the CAMMS A/D board for input image mean subtraction. Latching the upper 16-bits of the 32-bit output effectively performs a division by 256x256. This would immediately provide the mean value.

An LSI Logic L64032 MAC is suggested for the second calculation. This seems to be the only MAC available with an accumulator capable of storing the 44-bit results. This part has a 68-bit accumulator.

If the correlator input images are mean subtracted, then the output data should have zero mean. In this case only one MAC is needed and would compute the sum of the square of the outputs. However, a feature was added to the correlator hardware which clears all negative outputs. In this case, the mean output will be non-zero.

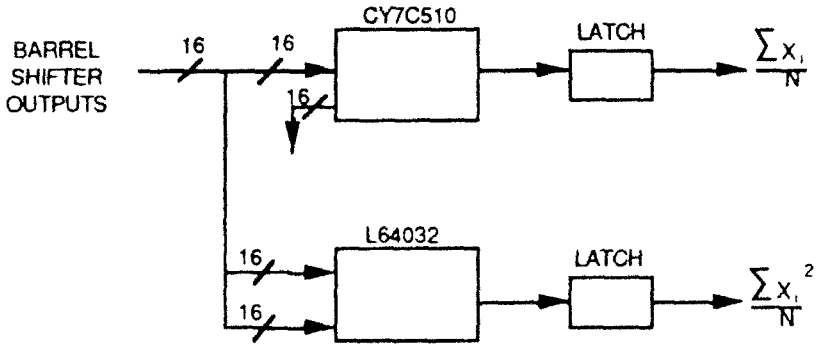


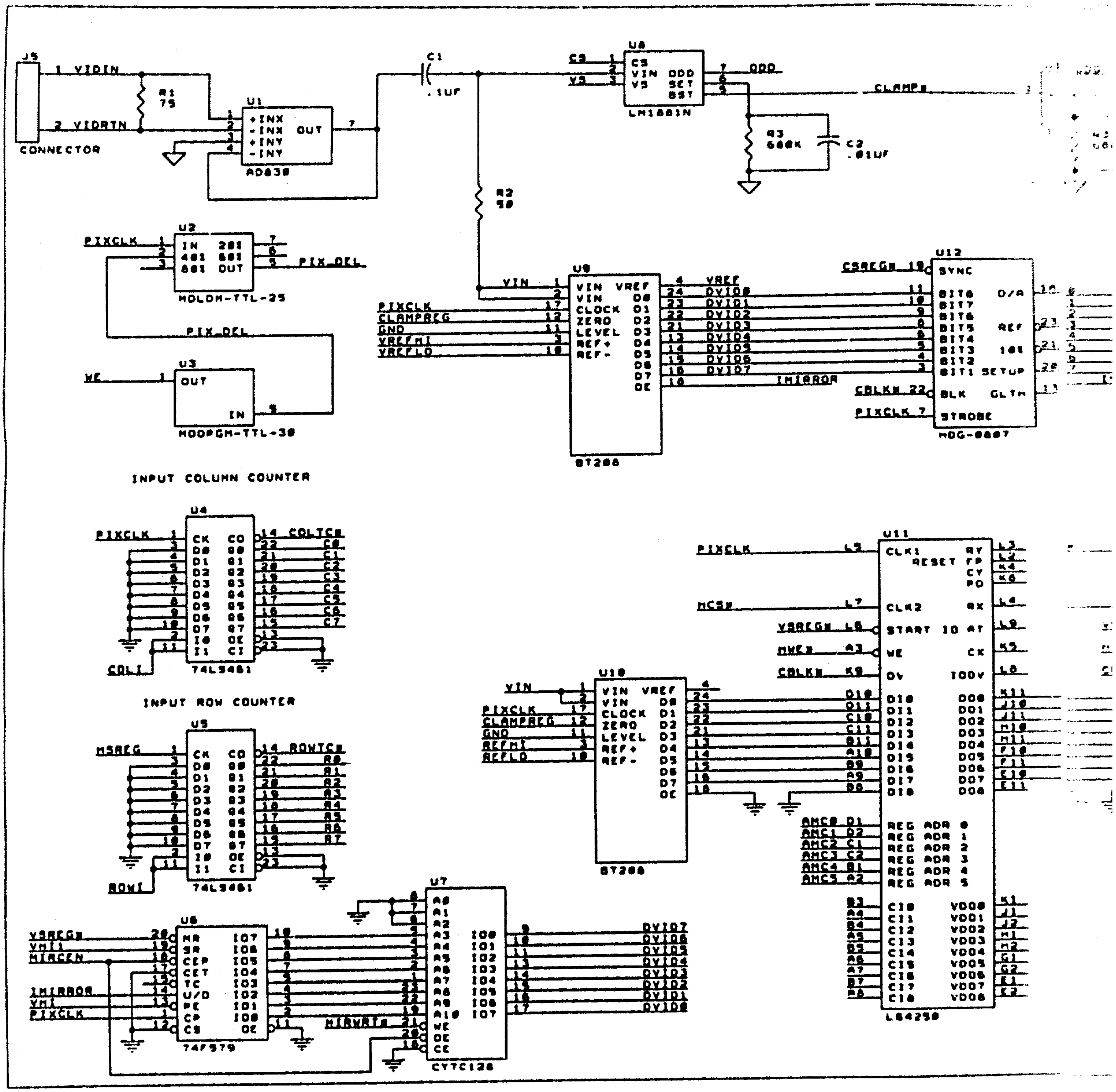
Figure 3.0-1 Computation of Mean and Standard Deviation

4.0 STATUS

The schematics presented in this report will provide the means to initiate prototyping of the preprocessor. The firmware for the logic at U17, U18 U27, U56 and the PAL 20x10's on page 5 remain to be developed. Additionally the micro controller firmware for U51 must be further developed.

APPENDIX A

PREPROCESSOR IBM/AT ELECTRICAL SCHEMATICS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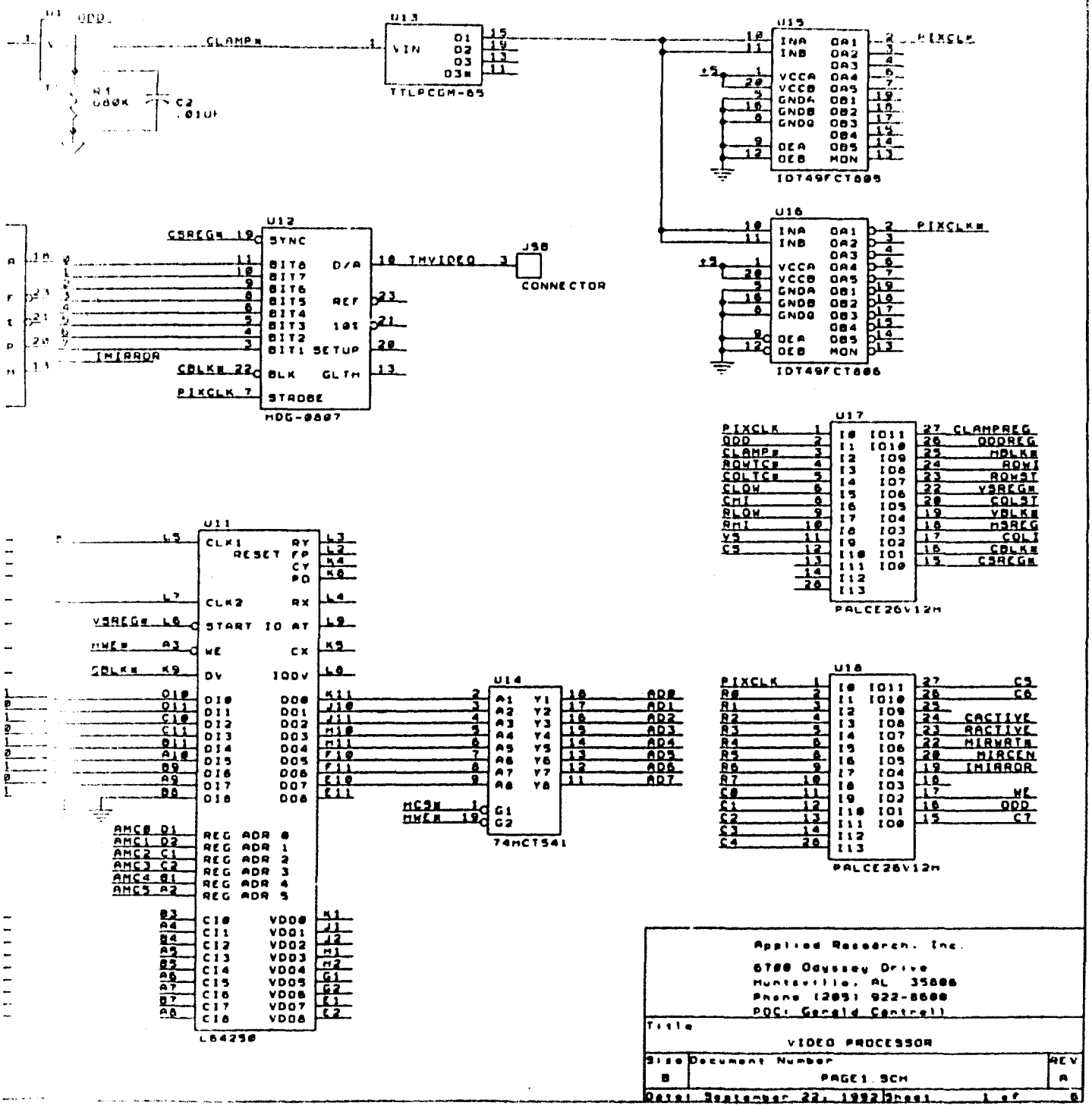
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U11
L64250
U14
74HCT541
U18
PALCE26V12H
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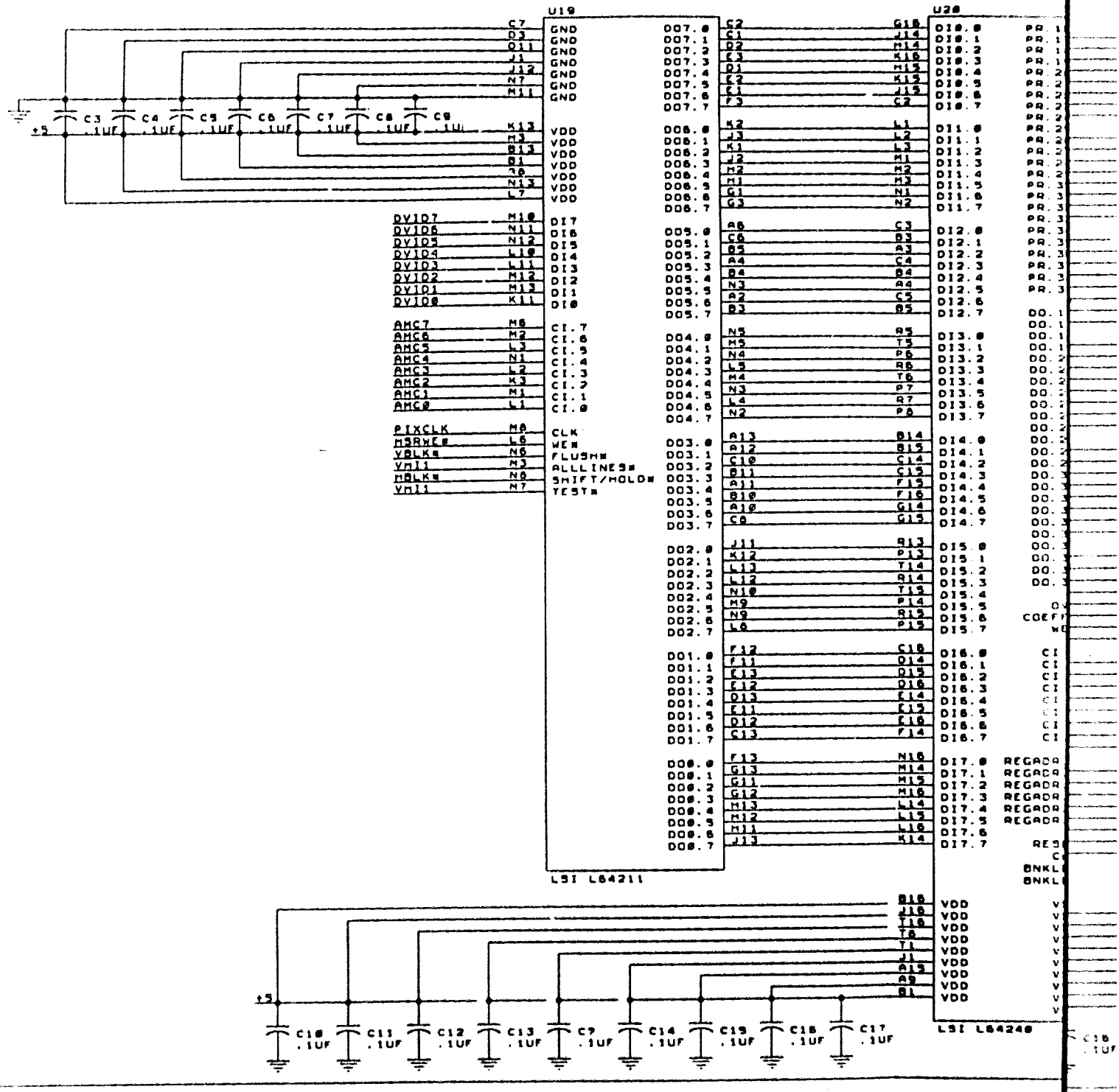
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AMC1
AMC0
PIXCLK
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SHIFT/HOLD#
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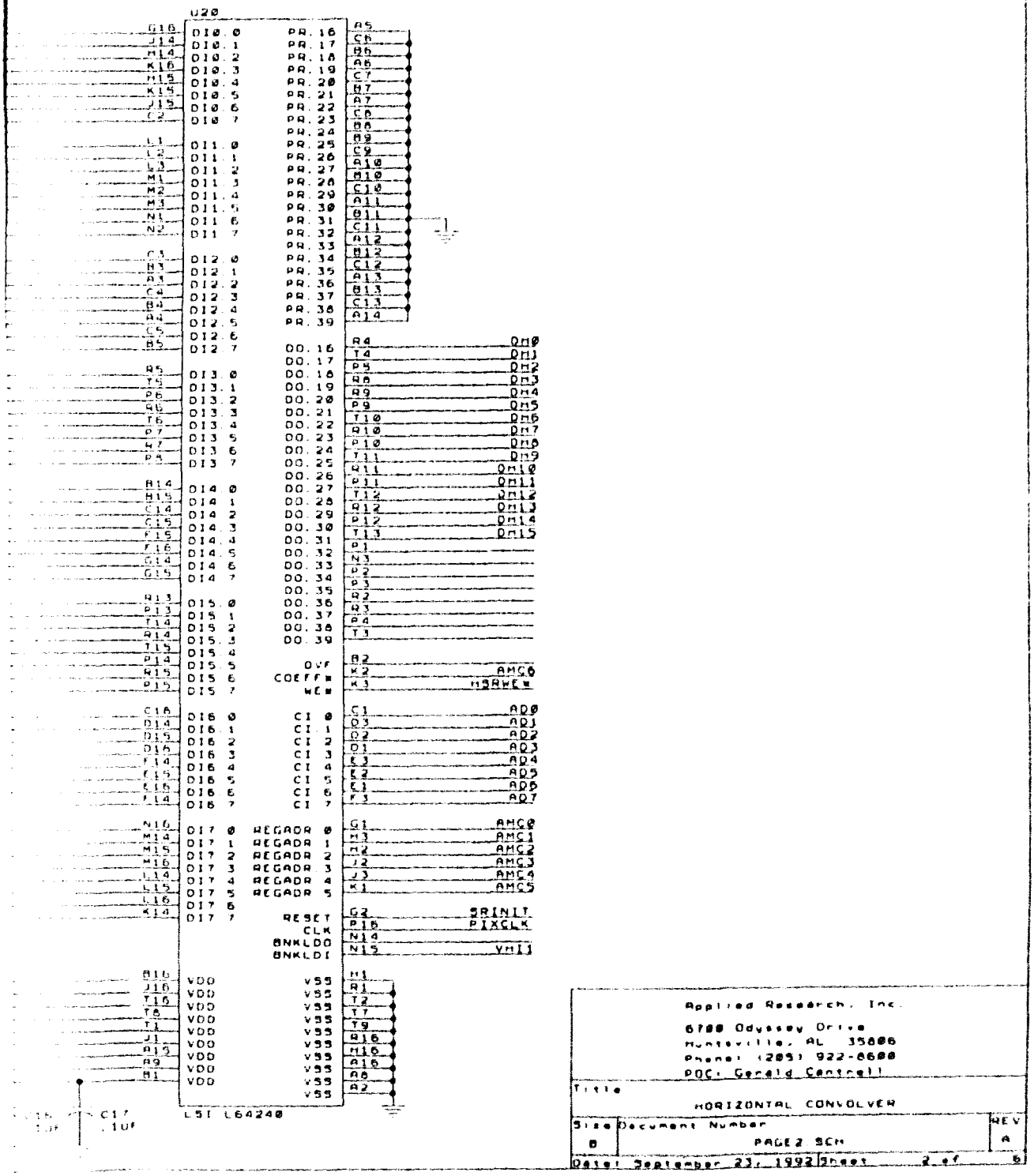

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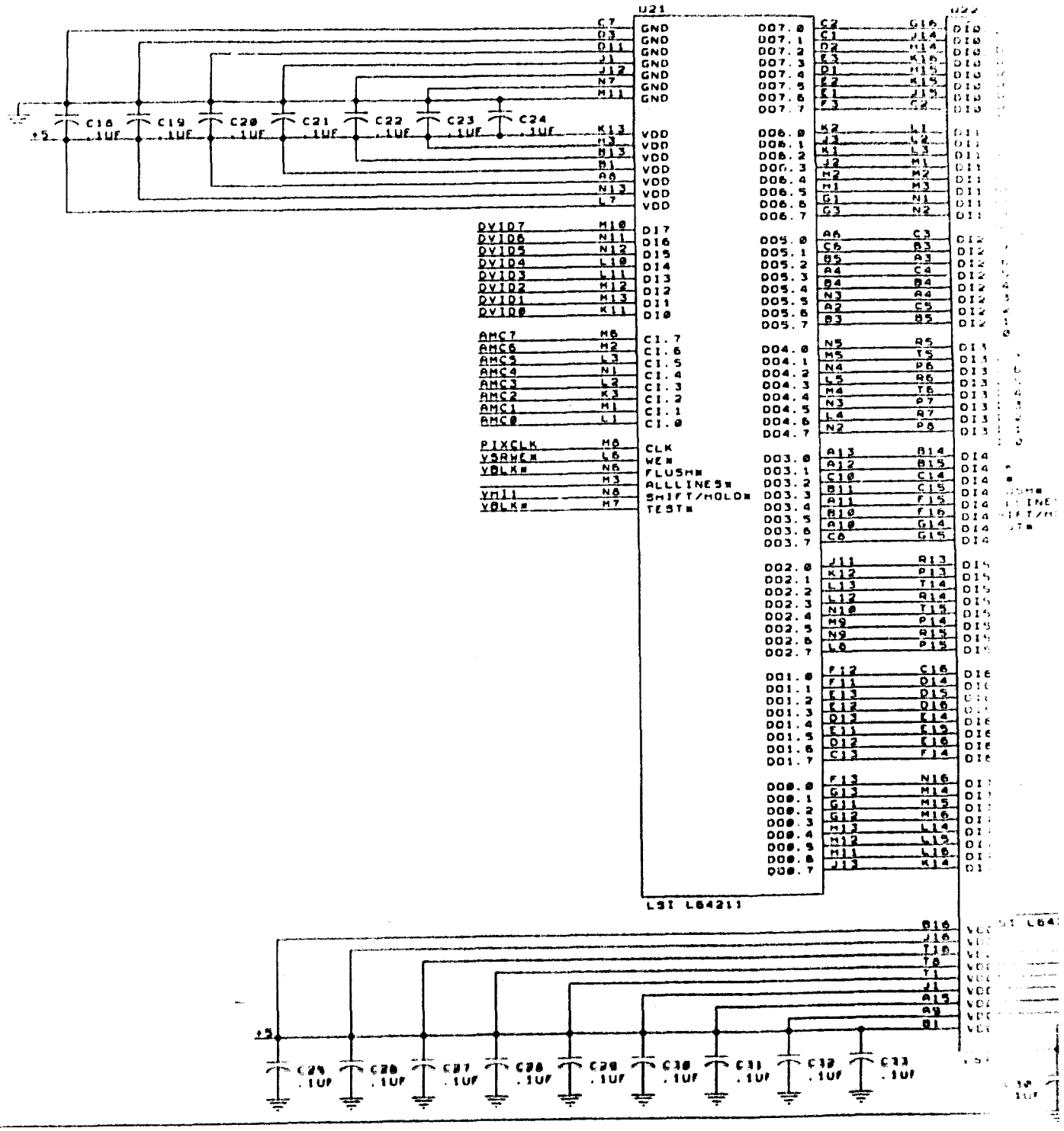
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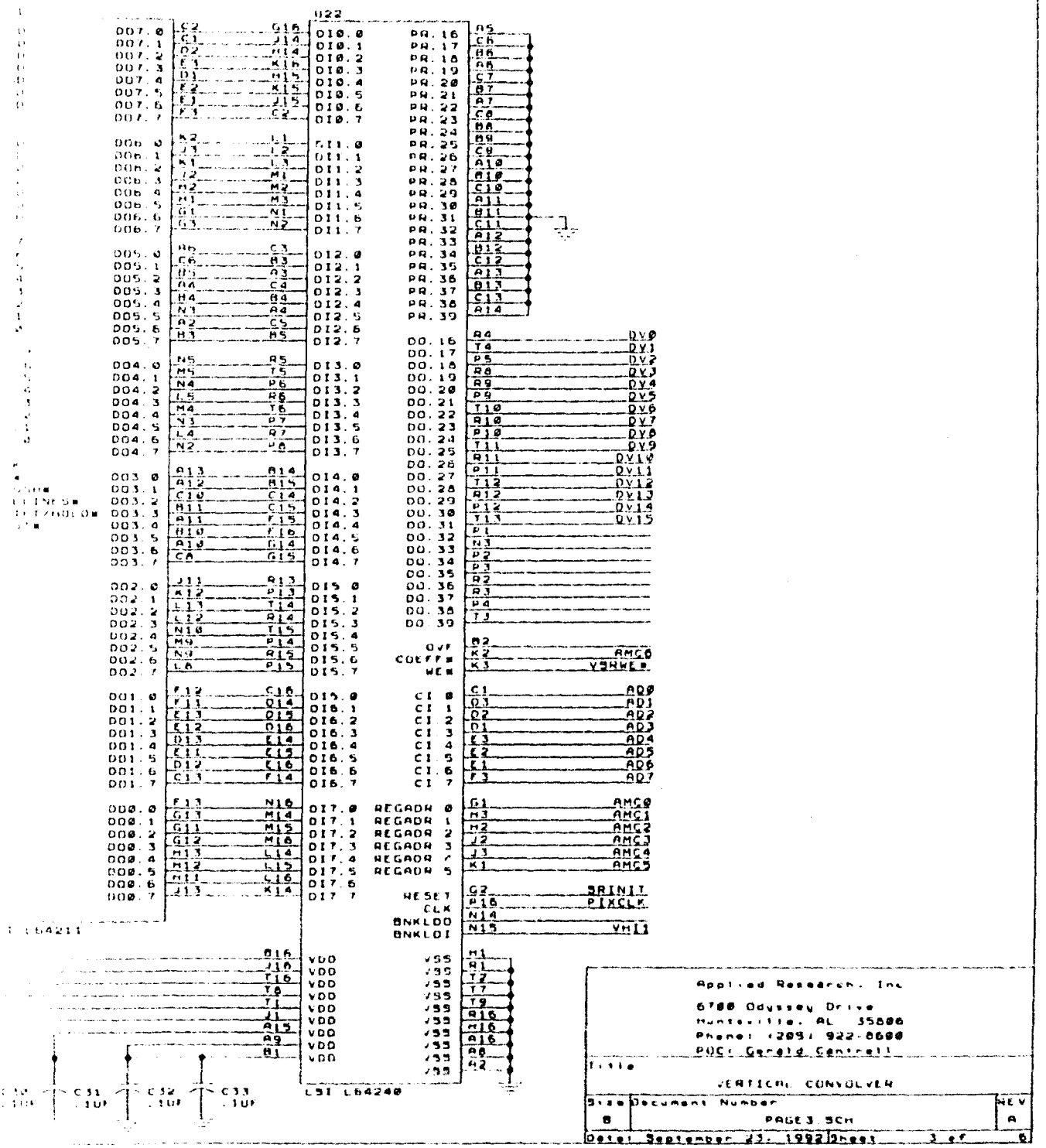
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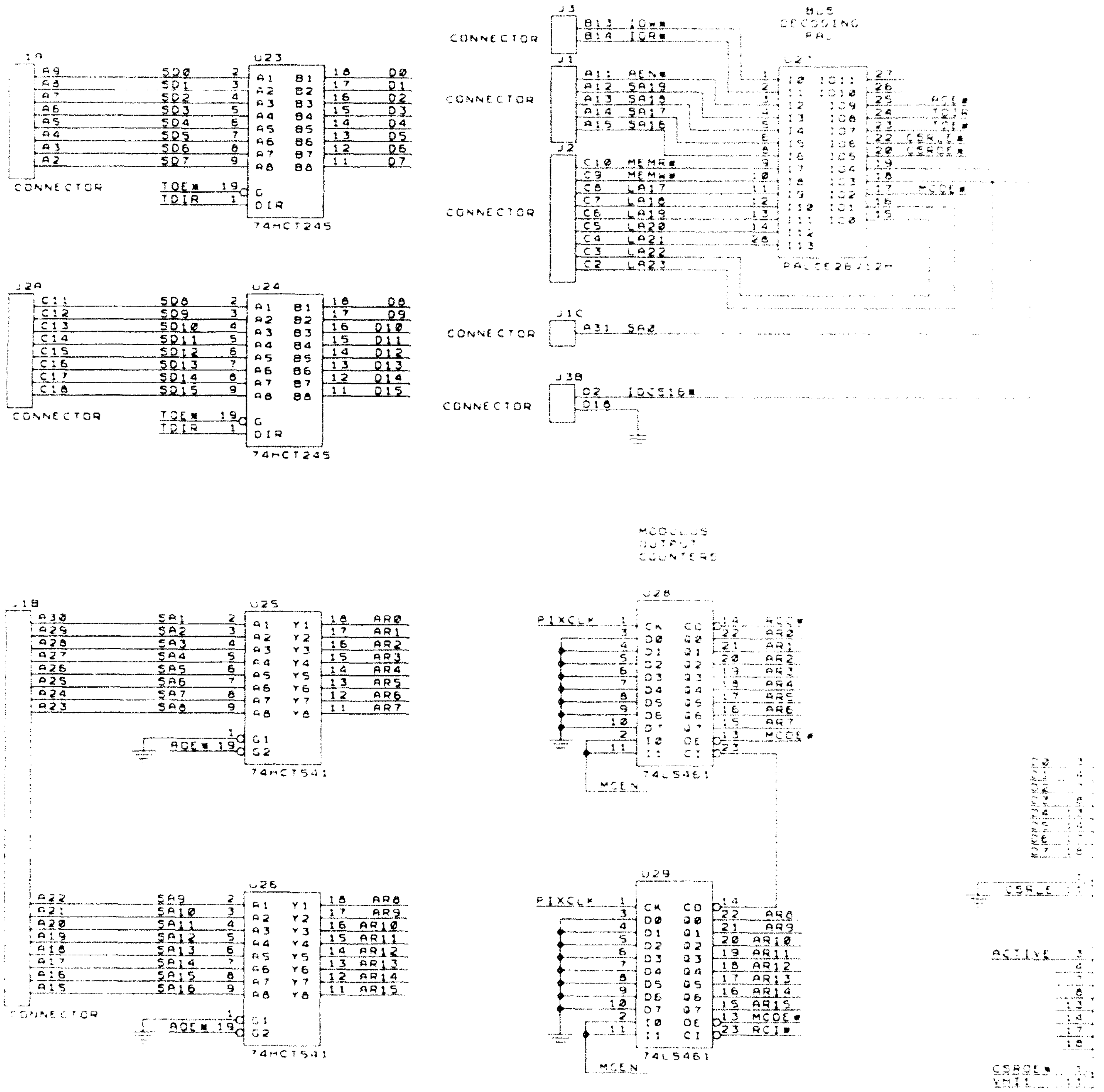
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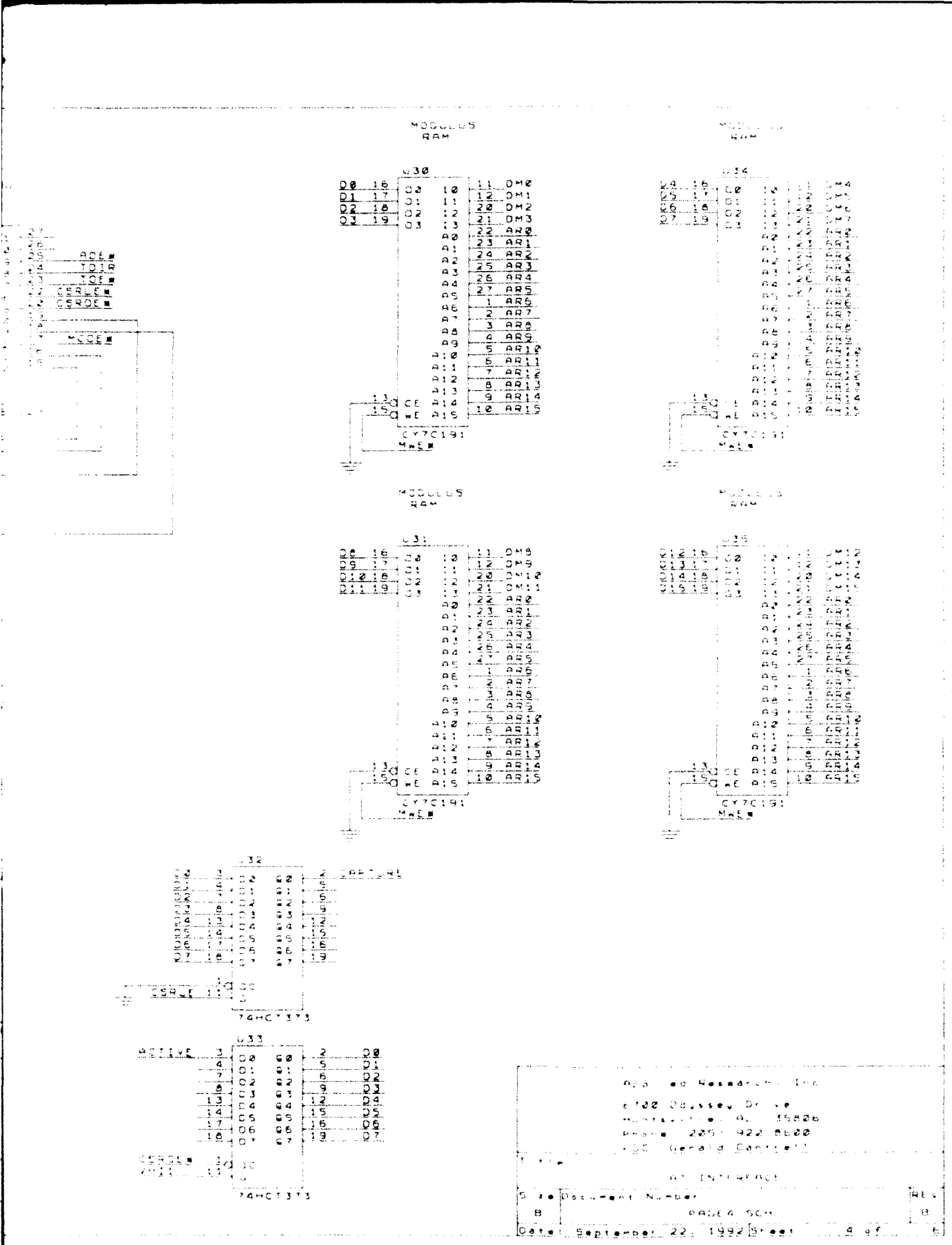
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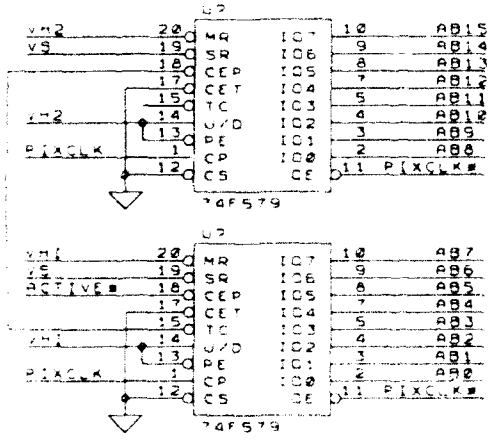
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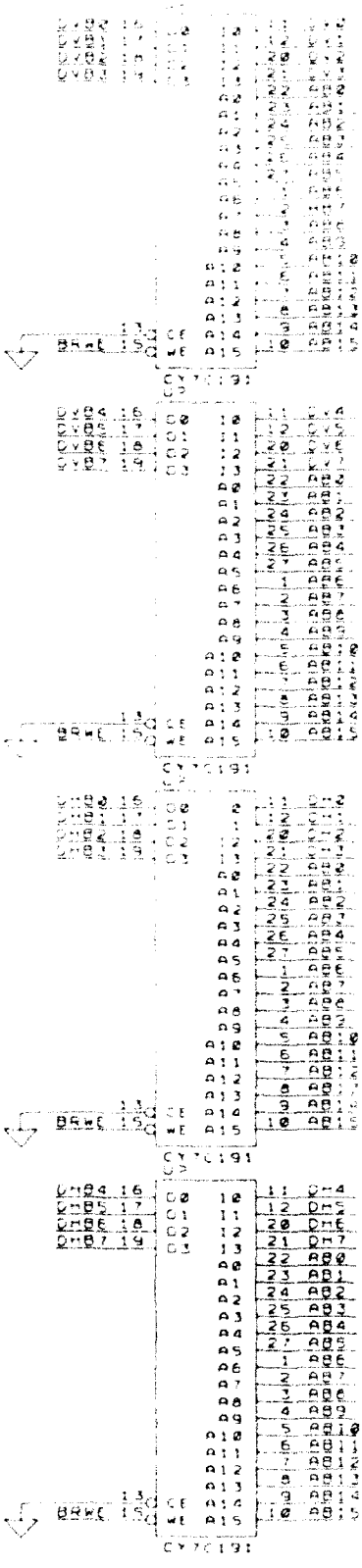

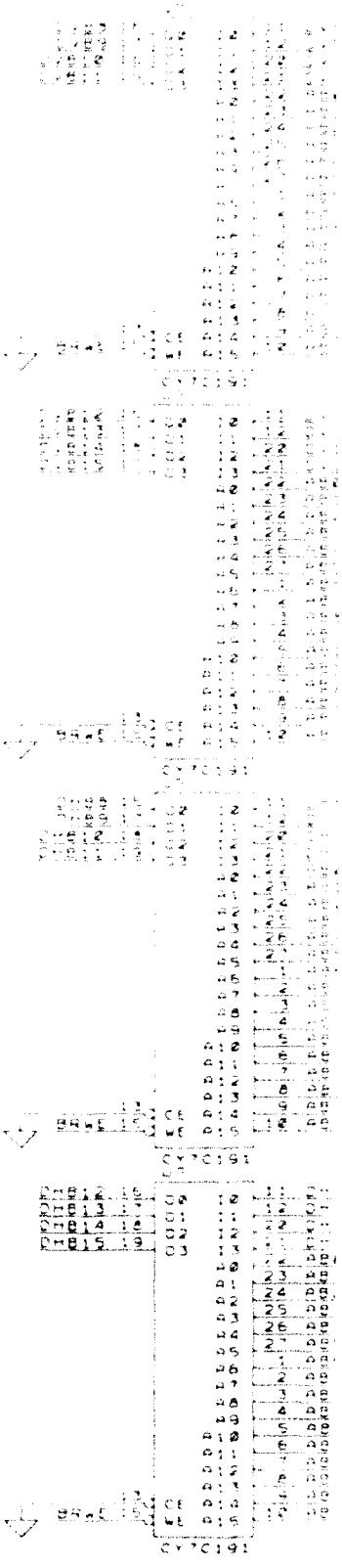

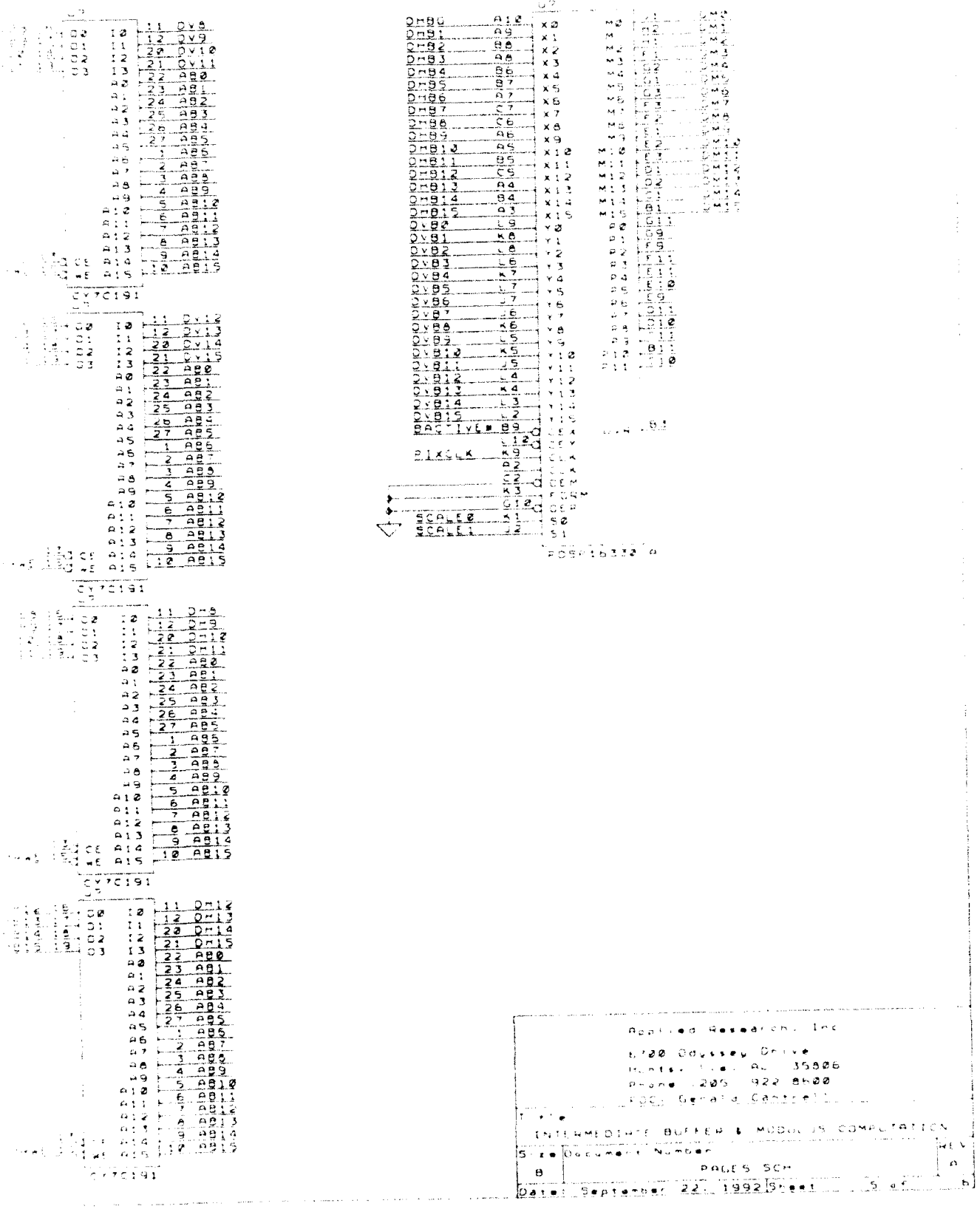

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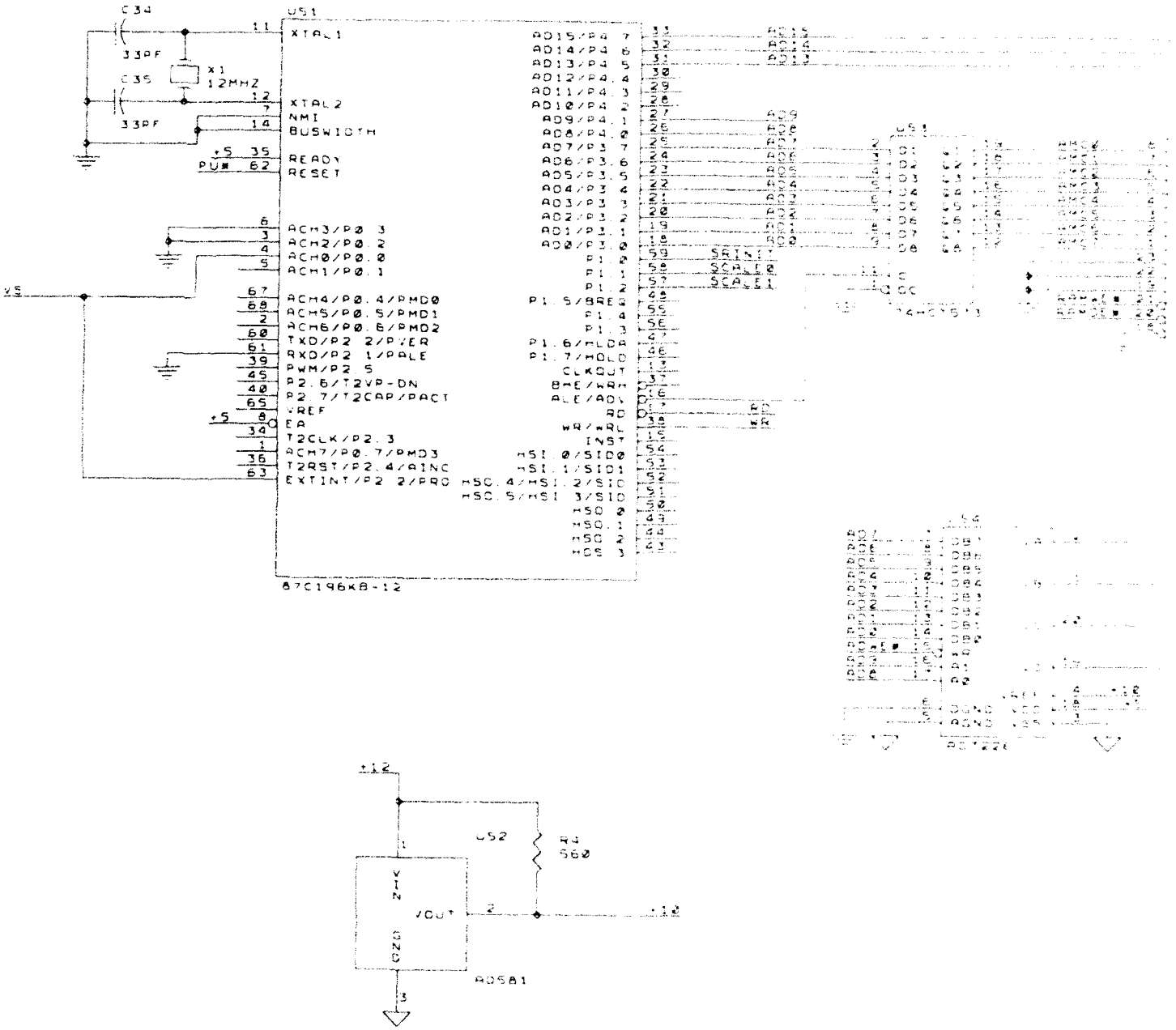
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RXD/P2.1/PALE
PWM/P2.5
P2.6/T2VP-DN
P2.7/T2CAP/PACT
VREF
EA
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T2RST/P2.4/AINC
EXTINT/P2.2/PRO
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AD12/P4.4
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AD10/P4.2
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AD8/P4.0
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AD6/P3.6
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AD1/P3.1
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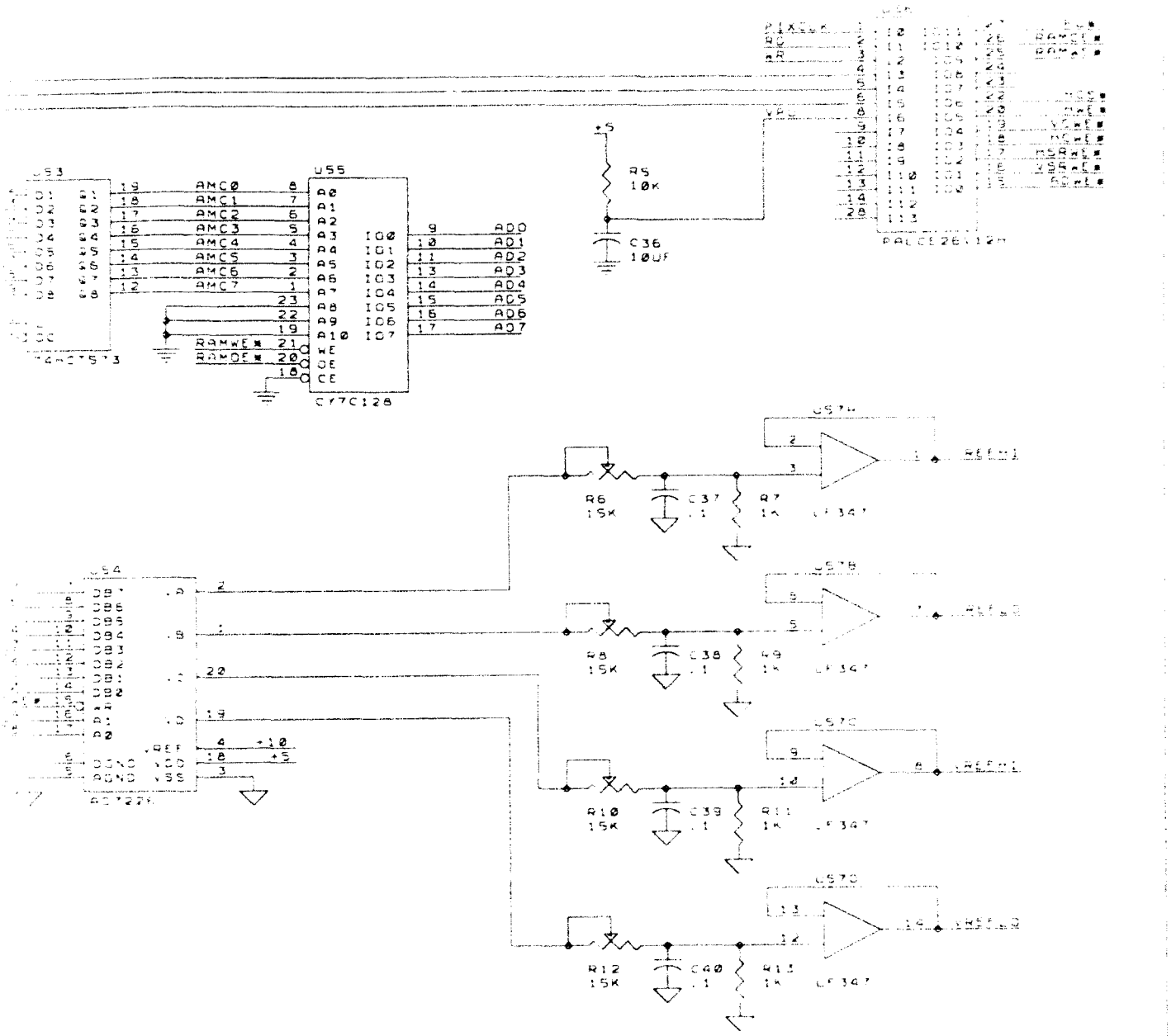

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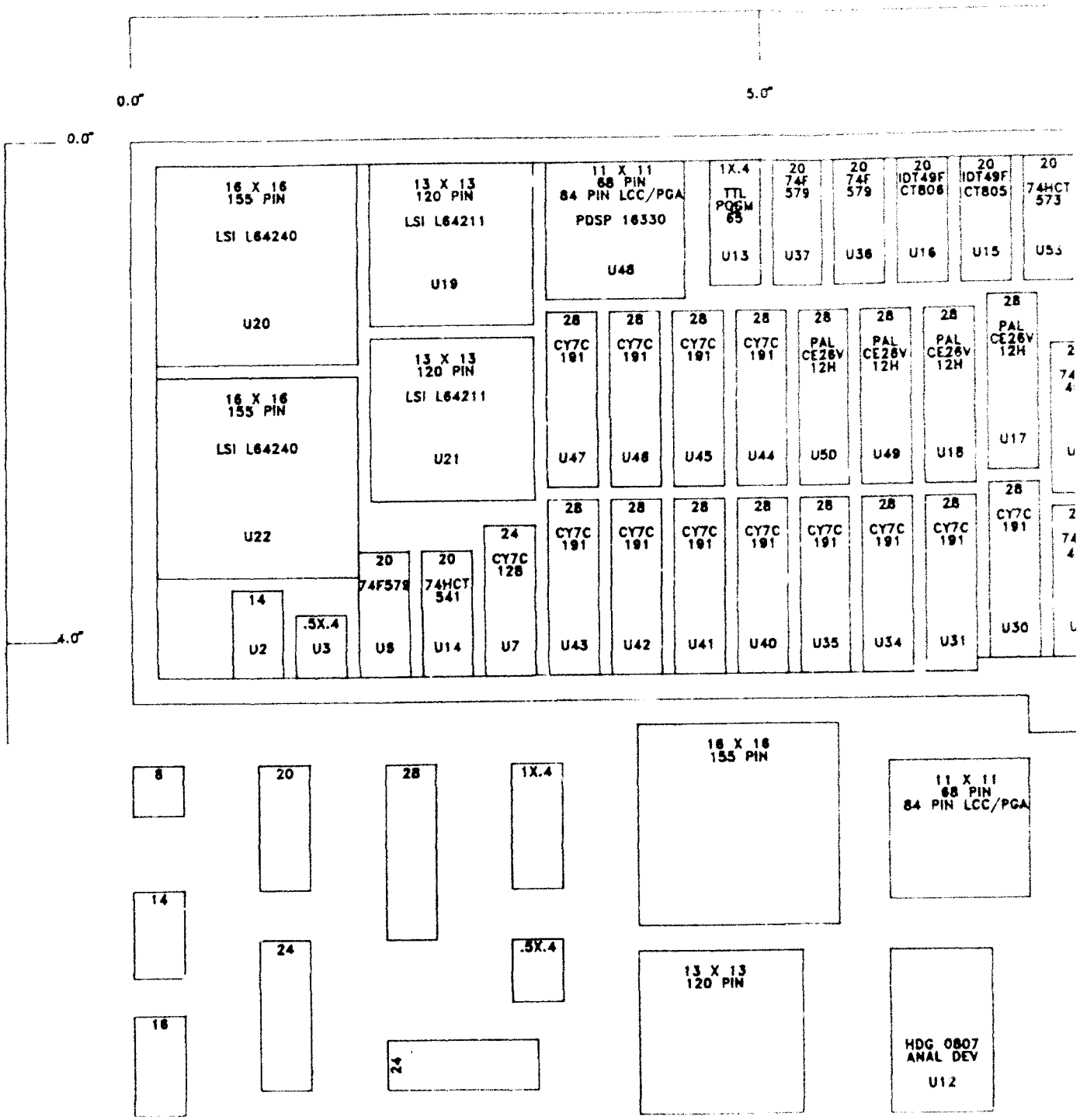
APPENDIX B

PREPROCESSOR LAYOUT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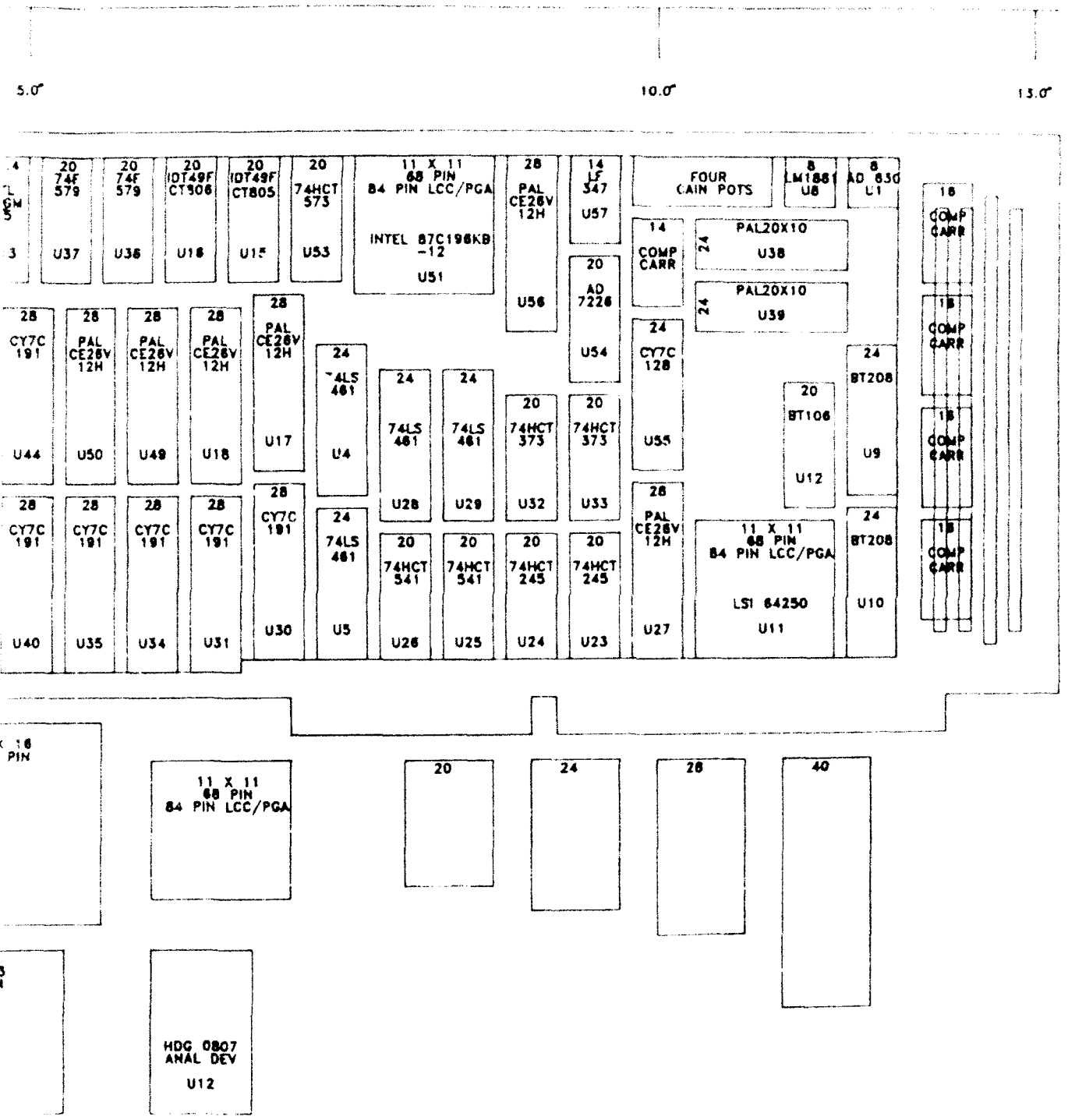
28
PAL
CE26V
12H
U49
28
PAL
CE26V
12H
U18
28
PAL
CE26V
12H
U17
28
CY7C
191
U30
14
U2
.5X.4
U3
20
74F579
U8
20
74HCT
541
U14
24
CY7C
128
U7
28
CY7C
191
U43
28
CY7C
191
U42
28
CY7C
191
U41
28
CY7C
191
U40
28
CY7C
191
U35
28
CY7C
191
U34
28
CY7C
191
U31
8
20
28
1X.4
16 X 16
155 PIN
11 X 11
68 PIN
84 PIN LCC/PGA
14
24
.5X.4
13 X 13
120 PIN
16
24
HDG 0807
ANAL DEV
U12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14 LF 347 U57
FOUR CAIN POTS
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8 AD 630 U1
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