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Dynamic Performance Comparison of the A/D Converters
for the North Warning System

By

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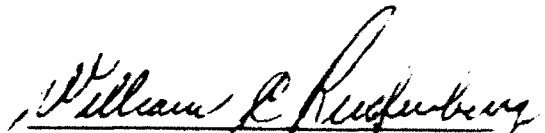
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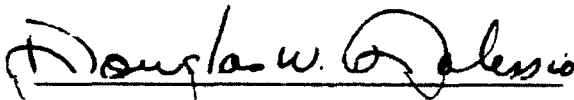


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TABLE OF CONTENTS

SECTION	PAGE
1 Introduction	1
1.1 A/D Converter Tests	1
1.2 Test Definition	5
1.2.1 Signal-to-Noise Ratio	5
1.2.2 Signal-to-Noise-and-Distortion Ratio	5
1.2.3 Effective Number of Bits	6
1.2.4 Spurious-Free Dynamic Range	6
1.2.5 Integral Nonlinearity	6
1.2.6 Differential Nonlinearity	6
1.2.7 Code Edge	8
1.2.8 Monotonicity	8
1.3 Summary and Conclusions	8
1.3.1 System Impact	11
2 Description of Two A/D Converters and the A/D Instrumentation Facility	15
2.1 Characteristics of Two NWS A/D Converters	15
2.2 Description of the Digital Test Bed	15
2.3 Phase-Plane Analysis of Converters with Sine Waves	19
2.3.1 Sine-Wave Estimation	20
2.3.2 Phase-Plane Data Analysis	23
3 Single-Tone Test Results	25
3.1 Test Results for the DDC 12-Bit, 4-MHz A/D Converter	26
3.2 Test Results for the ADC 12-Bit, 4-MHz A/D Converter - Unit 1	38
3.3 Test Results for the ADC 12-Bit, 4-MHz A/D Converter - Unit 2	45
3.4 Summary and Conclusions of Sine-Wave Tests	57
4 Monotonicity Analysis and Test Results	59
4.1 Test Description	59
4.2 Data Analysis	60
4.3 DDC A/D Converter Analysis	61
4.3.1 Histogram Method	61
4.3.2 Code-Mean Method of Analysis	65
4.3.3 Code-Edge Method of Analysis	66
4.4 ADC A/D Converter Monotonicity Analysis - Unit 2	70
4.4.1 Histogram Method	70
4.4.2 Code-Mean Method	73
4.5 Summary and Conclusions of Monotonicity Analysis	73

5	Transient and Overvoltage Recovery Testing Results	77
5.1	Test Description	77
5.2	Test Circuit Description	78
5.3	Data Analysis	81
5.3.1	DDC A/D Converter Overvoltage and Transient Recovery Results	81
5.3.2	ADC A/D Converter Overvoltage and Transient Recovery Results - Unit 2	83
5.4	Beat Frequency Test	86
5.4.1	Test Description	87
5.4.2	DDC A/D Converter Results from the Beat Frequency Test	88
5.5	Summary and Conclusions of Transient and Overvoltage Recovery Tests	90
	List of References	95
Appendix A	Generalized Sine-Wave Estimation Algorithm	97
Appendix B	FORTTRAN Listing of the Program Mono	105
Appendix C	Statistical Analysis	113
	Glossary	129

LIST OF FIGURES

FIGURE	PAGE
1(a) ADC A/D Converter	2
1(b) DDC A/D Converter	2
2 Errors in A/D Converters	7
3 A/D Instrumentation Facility Generic Block Diagram	18
4 A/D Instrumentation Facility	18
5 Noise vs. Input Signal Level for the DDC A/D Converter	27
6 SINAD vs. Input Signal Level for the DDC A/D Converter	27
7 Bits Lost vs. Input Signal Level for the DDC A/D Converter	28
8 SFDR vs. Input Signal Level for the DDC A/D Converter	28
9(a) FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 0.10 MHz; Amplitude of the Signal = Full-Scale)	29
9(b) FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 0.10 MHz; Amplitude of the Signal = -30 dB)	29
9(c) FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 0.27 MHz; Amplitude of the Signal = Full-Scale)	30
9(d) FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 0.27 MHz; Amplitude of the Signal = -30 dB)	30
9(e) FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = Full-Scale)	31
9(f) FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = -30 dB)	31
9(g) FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 1.0 MHz; Amplitude of the Signal = Full-Scale)	32
9(h) FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 1.0 MHz; Amplitude of the Signal = -30 dB)	32

9(i)	FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 1.25 MHz; Amplitude of the Signal = Full-Scale)	33
9(j)	FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 1.25 MHz; Amplitude of the Signal = -30 dB)	33
9(k)	FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 1.5 MHz; Amplitude of the Signal = Full-Scale)	34
9(l)	FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 1.5 MHz; Amplitude of the Signal = -30 dB)	34
9(m)	FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 2.0 MHz; Amplitude of the Signal = Full-Scale)	35
9(n)	FFT Spectral Response for the DDC A/D Converter (Input Signal Frequency = 2.0 MHz; Amplitude of the Signal = -30 dB)	35
10(a)	Errors of DDC A/D Converter (Input Signal Frequency = 101 kHz)	39
10(b)	Errors of DDC A/D Converter (Input Signal Frequency = 271 kHz)	39
10(c)	Errors of DDC A/D Converter (Input Signal Frequency = 544 kHz)	40
10(d)	Errors of DDC A/D Converter (Input Signal Frequency = 997 kHz)	40
10(e)	Errors of DDC A/D Converter (Input Signal Frequency = 1249 kHz)	41
10(f)	Errors of DDC A/D Converter (Input Signal Frequency = 1495 kHz)	41
10(g)	Errors of DDC A/D Converter (Input Signal Frequency = 1991 kHz)	42
11	Noise vs. Input Signal Level for the ADC A/D Converter - Unit 1	43
12	SINAD vs. Input Signal Level for the ADC A/D Converter - Unit 1	43
13	Bits Lost vs. Input Signal Level for the ADC A/D Converter - Unit 1	44
14	SFDR vs. Input Signal Level for the ADC A/D Converter - Unit 1	44
15(a)	FFT Spectral Response for the ADC A/D Converter - Unit 1 (Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = Full-Scale)	46
15(b)	FFT Spectral Response for the ADC A/D Converter - Unit 1 (Input Signal Frequency = 1.25 MHz; Amplitude of the Signal = Full-Scale)	46
16	Noise vs. Input Signal Level for the ADC A/D Converter - Unit 2	48

17	SINAD vs. Input Signal Level for the ADC A/D Converter - Unit 2	48
18	Bits Lost vs. Input Signal Level for the ADC A/D Converter - Unit 2	49
19	SFDR vs. Input Signal Level for the ADC A/D Converter - Unit 2	49
20(a)	FFT Spectral Response for the ADC A/D Converter - Unit 2 (Input Signal Frequency = 0.10 MHz; Amplitude of the Signal = Full-Scale)	51
20(b)	FFT Spectral Response for the ADC A/D Converter - Unit 2 (Input Signal Frequency = 0.10 MHz; Amplitude of the Signal = -30 dB)	51
20(c)	FFT Spectral Response for the ADC A/D Converter - Unit 2 (Input Signal Frequency = 0.27 MHz; Amplitude of the Signal = Full-Scale)	52
20(d)	FFT Spectral Response for the ADC A/D Converter - Unit 2 (Input Signal Frequency = 0.27 MHz; Amplitude of the Signal = -30 dB)	52
20(e)	FFT Spectral Response for the ADC A/D Converter - Unit 2 (Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = Full-Scale)	53
20(f)	FFT Spectral Response for the ADC A/D Converter - Unit 2 (Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = -30 dB)	53
20(g)	FFT Spectral Response for the ADC A/D Converter - Unit 2 (Input Signal Frequency = 1.5 MHz; Amplitude of the Signal = Full-Scale)	54
20(h)	FFT Spectral Response for the ADC A/D Converter - Unit 2 (Input Signal Frequency = 1.5 MHz; Amplitude of the Signal = -30 dB)	54
21(a)	Error vs. Signal Phase for the ADC A/D Converter - Unit 2	56
21(b)	Errors of ADC A/D Converter - Unit 2 at 544 kHz	56
22(a)	Normalized Histogram for the DDC A/D Converter (Decreasing Voltage)	63
22(b)	Normalized Histogram for the DDC A/D Converter (Increasing Voltage)	63
22(c)	Normalized Histogram for the DDC A/D Converter (Combined Slopes)	64
23(a)	Code-Mean Separation for the DDC A/D Converter (Decreasing Voltage)	67
23(b)	Code-Mean Separation for the DDC A/D Converter (Increasing Voltage)	67
23(c)	Code-Mean Separation for the DDC A/D Converter (Combined Voltages)	68
24(a)	Code-Edge Separation for the DDC A/D Converter (Decreasing Voltage)	69

24(b)	Code-Edge Separation for the DDC A/D Converter (Increasing Voltage)	69
25(a)	Normalized Histogram for the ADC A/D Converter - Unit 2 (Decreasing Voltage)	71
25(b)	Normalized Histogram for the ADC A/D Converter - Unit 2 (Increasing Voltage)	71
25(c)	Normalized Histogram for the ADC A/D Converter - Unit 2 (Combined Slopes)	72
26(a)	Mean Code Width for the ADC A/D Converter - Unit 2 (Decreasing Voltage)	74
26(b)	Mean Code Width for the ADC A/D Converter - Unit 2 (Increasing Voltage)	74
26(c)	Mean Code Width for the ADC A/D Converter - Unit 2 (Combined Slopes)	75
27	Pulse Generator Schematic	79
28	Pulse Generator Layout	80
29	Overvoltage Recovery Response of DDC A/D Converter When Pulsed into Positive Saturation (20 nsec Delay)	82
30	Overvoltage Recovery Response of DDC A/D Converter When Pulsed into Positive Saturation (90 nsec Delay)	82
31	Overvoltage Recovery Response of DDC A/D Converter When Pulsed into Positive Saturation on an Expanded Scale (20 nsec Delay)	84
32	Overvoltage Recovery Response of DDC A/D Converter When Pulsed into Positive Saturation on an Expanded Scale (90 nsec Delay)	84
33	ADC A/D Converter - Unit 2 - Pulsed into Positive Saturation	85
34	Overvoltage Recovery Response of ADC A/D Converter - Unit 2 When Pulsed into Positive Saturation on an Expanded Scale (20 nsec Delay)	85
35	Pulse Response of DDC A/D Converter with a Negative Base Voltage and a 1 μ sec Pulse of +3.5V	89
36	Settling Response of DDC A/D Converter with a Negative Base Voltage and a 1 μ sec Pulse of +3.5V on an Expanded Scale	89

37	DDC A/D Converter Overvoltage Recovery Response from a +4.8V Pulse	91
38	DDC A/D Converter Overvoltage Recovery Response from a -1.7V Pulse	91
39	DDC A/D Converter Pulse Response with a Positive Base Voltage and a 1 μ sec Pulse of -3.5V	92
40	DDC A/D Converter Response When Recovering from a -4.4V Pulse	92
C-1	Output Code vs. Input Voltage for an A/D Converter with 0.5 LSB Noise	115
C-2	Probability of Code vs. Input Voltage for an A/D Converter with 0.5 LSB Noise	115
C-3	Ratio of Variance to the Mean of the Occurrences vs. Ratio of Code Width to Noise	116

LIST OF TABLES

TABLE	PAGE
1 UAR Receiver B2 Performance Requirements	3
2 DDC Model ADC 0015-600 A/D Converter Performance Summary	12
3 System SNR Loss Caused by Two A/D Converters	13
4 Summary of the Most Important Characteristics of the A/D Converters	16
5 A/D Instrumentation Capability	19
6 Measured Dynamic Performance of 12-Bit, 4-MHz DDC A/D Converter	36
7 Measured Dynamic Performance of 12-Bit, 4-MHz ADC A/D Converter - Unit 1	47
8 Measured Dynamic Performance of 12-Bit, 4-MHz ADC A/D Converter - Unit 2	55
9 Monotonicity - Differential Nonlinearity Test Results	76
10 Overvoltage and Transient Recovery Performance Comparison of Two A/D Converters for NWS	93

SECTION 1

INTRODUCTION

Currently, the North Warning System (NWS) employs the Analog Devices Corporation (ADC) 12-bit, 4-MHz analog-to-digital (A/D) converter model MOD-1205. During the full-scale development of the AN/FPS-124 Radar, the ADC converter was selected as the only one that met the system performance requirements (six of them are used in the three receiver channels of each radar). This converter has been in operation for three years with no known problems; however, Paramax (formerly Unisys Corporation) is proposing to replace it with model ADC-00115-600, manufactured by Data Device Corporation (DDC). Paramax delivered two ADC converters (referred to as Units 1 and 2) and a DDC converter for our evaluation (shown in figures 1(a) and 1(b)), enabling us to comment on their engineering change proposal.

As part of our assessment and evaluation of the DDC A/D converter, we conducted a series of tests to verify the Unattended Radar (UAR) receiver B2 performance requirements [1] for the baseline ADC unit (identified in table 1). A performance comparison revealed that ADC's Unit 1 was extremely noisy and did not meet spurious-free dynamic range (SFDR) radar B2 specifications. The dynamic test on Unit 2 revealed that it was noisier than Unit 1 and did not meet radar B2 Specifications either (note that both have been in operation for three years). Then, using the ADC tests as a baseline, the relative performance of the DDC unit was assessed and we also verified if it met the B2 requirements. This report presents a detailed analysis of the evaluation and dynamic performance testing of these three converters.

1.1 A/D CONVERTER TESTS

The dynamic performance (nonlinearities and noise) of an A/D converter can be characterized by a spectral analysis test [2,3,4], consisting of a series of sinusoidal signals of different frequencies and amplitudes. The input frequency selected for

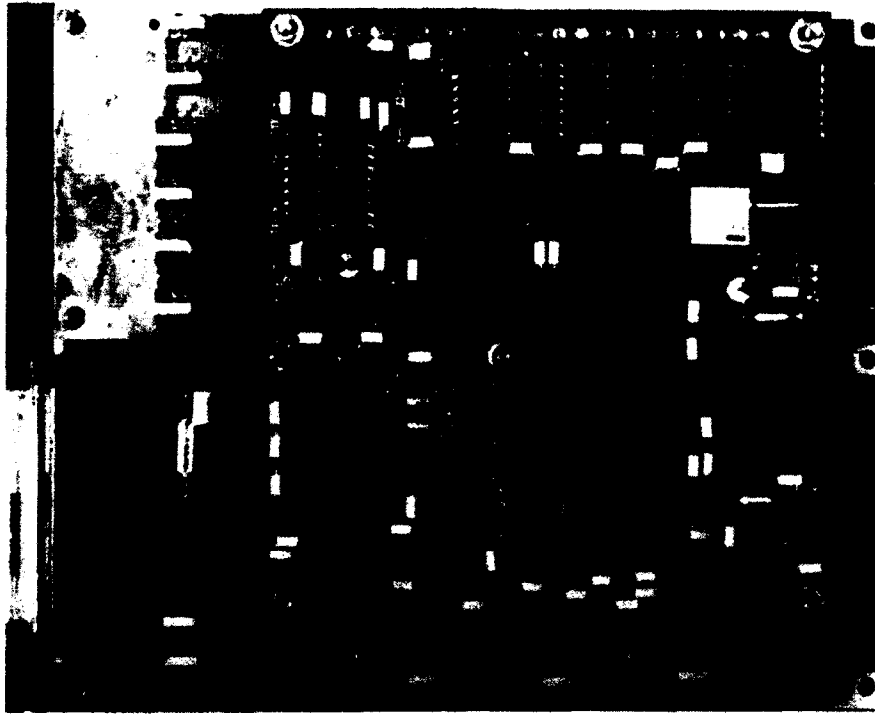


Figure 1(a). ADC A/D Converter

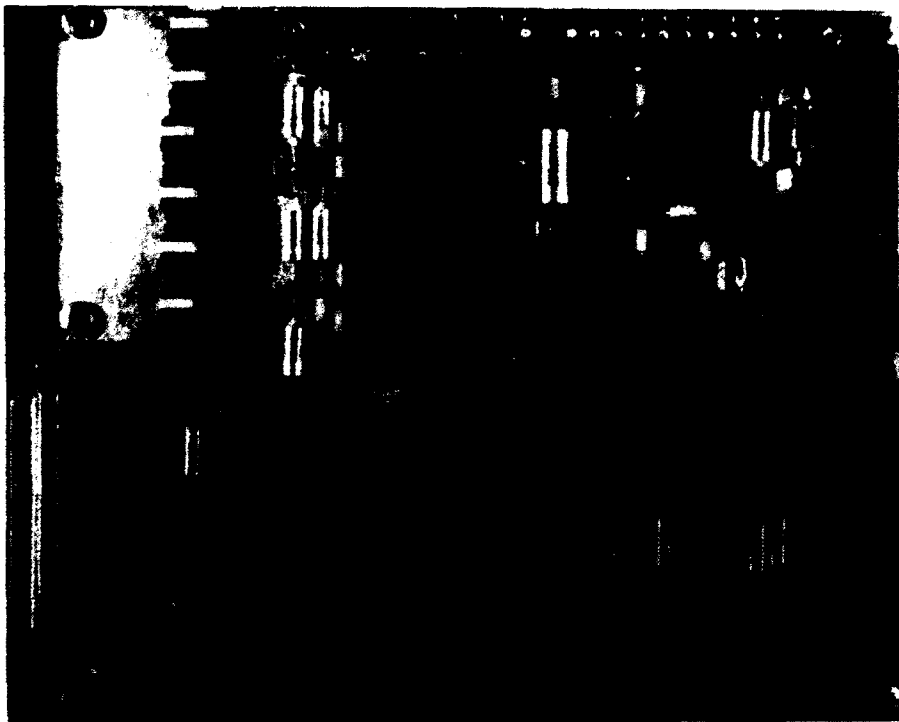


Figure 1(b). DDC A/D Converter

Table 1. UAR Receiver B2 Performance Requirements

Voltage Range	± 2.048 Volts
Conversion Time	Data valid 275 ± 25 nanoseconds after third encode command
Integral Linearity	± 0.1 percent of full-scale ± 0.5 least significant bit (LSB)*
Monotonicity	At 1.25 MHz - no missing codes, each code edge-to-edge width >ten percent, <190 percent of nominal
Alternating Current (ac) Linearity	At 0.54 MHz - spurious 70.0 dB below full-scale
Signal-to-Noise Ratio (SNR)	At 0.54 MHz, 63.0 dB minimum root mean square (RMS) signal-to-RMS noise
Transient Response	Transient response (for full-scale step input): attains full-scale accuracy to ± 5.0 mVolts in 200 nanoseconds maximum
Overvoltage Recovery Time	Overvoltage recovery time (for 2x full-scale input): recovers ± 5.0 mV (millivolts) of 12-bit accuracy within 200 nanoseconds

* NOTE: One LSB is defined as the resolution of an A/D converter, which is equal to $(2^{-N} \times \text{the full-scale voltage of the converter})$, where N = the number of bits of the converter.

the test is representative of the expected signal/clutter frequencies. For our test, we select seven frequencies, two of which are specified in the radar B2 specification [1]. Full-amplitude, single-tone, sine-wave testing is the most stressful test for A/D converters [3] because the full-amplitude signal level maximizes the slew rate of the input, and tests all encoding levels. The results of the spectral analysis test are used to determine the effective number of bits, the SFDR, and the harmonic distortion of the A/D converter.

The B2 specification requires that the A/D converter be tested for monotonicity at a test frequency of 1.25 MHz, and that the separation of all of the code edges between adjacent

codes be 1.0 ± 0.9 least significant bits (LSB), which is a specification of differential linearity. It is difficult to measure monotonicity or code-edge separation with a high-frequency test signal; either special test equipment or elaborate data processing is required. The monotonicity test is usually done at direct current (dc), which does not reflect high-frequency performance. Although it is a variant of the sine-wave test, we employ custom software to perform monotonicity analysis of data obtained with a pure sine-wave input voltage.

The transient and overvoltage recovery performances of the converters are determined by applying a pulsed waveform as input and determining the time required to recover from the pulse. Ideal pulses have no overshoot or ringing, and negligible rise and fall times. Since commercial test equipment used in our test facility is unable to produce a pulse which is clean to 12 bits accuracy with a 400 ohm load, a special test fixture was designed and built (the details are described in section 5).

A systematic approach to characterizing high-speed A/D converters based on sinusoidal testing was developed as part of a MITRE-sponsored research project [4]. To test the A/D converters digitally, a laboratory test facility was constructed. The next section presents the key parameters used to characterize them dynamically.

Section 2 of this report briefly describes the DDC and ADC converters that are tested, the test equipment, and the data analysis algorithm used to characterize them. Section 3 presents the dynamic performance results of the DDC converter (tested at seven frequencies) and the two ADC converters. Section 4 provides the details of the monotonicity performance, while section 5 presents the transient and overvoltage recovery test results. Appendix A presents the general sine-wave estimation algorithm; appendix B is a FORTRAN listing of the simplified sine-wave estimation algorithm; and appendix C presents the statistical analysis which is used in evaluating the monotonicity test results.

1.2 TEST DEFINITION

This section briefly defines the dynamic performance measures [5,6] used to characterize the A/D converters. The quantitative values of the parameters are determined in the frequency domain by performing spectral analysis.

1.2.1 Signal-to-Noise Ratio

A standard measure of A/D converter performance for signal processing applications is the ratio of the signal power to the noise power in the Nyquist frequency band used, usually referred to as the signal-to-noise ratio (SNR)¹. The SNR is defined as

$$SNR = 10 \log(P_s/N_s) \text{ in dB,} \quad (1)$$

where P_s is the signal power, and N_s is the total noise power in the Nyquist frequency band, which extends from the low frequency to half the sampling frequency.

1.2.2 Signal-to-Noise-and-Distortion Ratio

Signal-to-noise-and-distortion ratio (SINAD) is defined as the ratio of the signal power to the total error power. The total error power includes the power in the harmonics as well as the power caused by random noise,

$$SINAD = 10 \log\left(\frac{P_s}{N_s + P_h}\right) \text{ in dB,} \quad (2)$$

where P_s is the signal power, N_s is the noise power, and P_h is the power in the harmonics.

¹ Nyquist bandwidth is $\frac{\text{sampling frequency}}{2}$.

1.2.3 Effective Number of Bits

The theoretical dynamic range for an ideal A/D converter with a full-scale sine-wave input is $6.02 N + 1.76$ dB [5,6], where N is the number of bits (quantization noise is the only noise). For a nonideal A/D converter, the SINAD and the effective number of bits, N_{eff} are directly related by the following equation:

$$N_{eff} = \frac{SINAD \text{ (in dB)} - 1.76}{6.02} \quad (3)$$

The effective number of bits is computed from the SINAD measured in the frequency domain using spectral analysis. The number of bits lost is the difference between the nominal bits of the A/D converter and the effective number of bits. Note that N_{eff} is a function of the input test signal frequency and amplitude; it is merely a different way of expressing the SINAD.

1.2.4 Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) [4] is defined as the ratio of the power of the sine-wave input to the power of the harmonic with the highest amplitude, measured in dB, up to half the sampling frequency and excluding the dc component.

1.2.5 Integral Nonlinearity

The integral nonlinearity, as shown in figure 2, is the maximum deviation of the A/D transfer function from a best-fit straight line.

1.2.6 Differential Nonlinearity

The differential nonlinearity, also shown in figure 2, is a measure of how much the code widths vary from the ideal code width of 1.0 LSB.

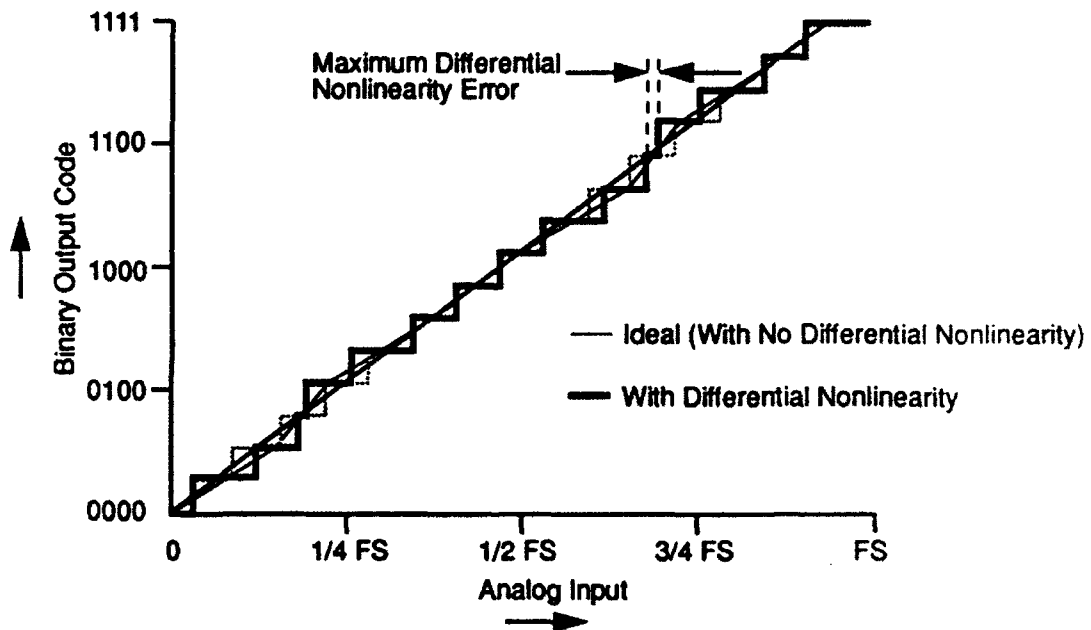
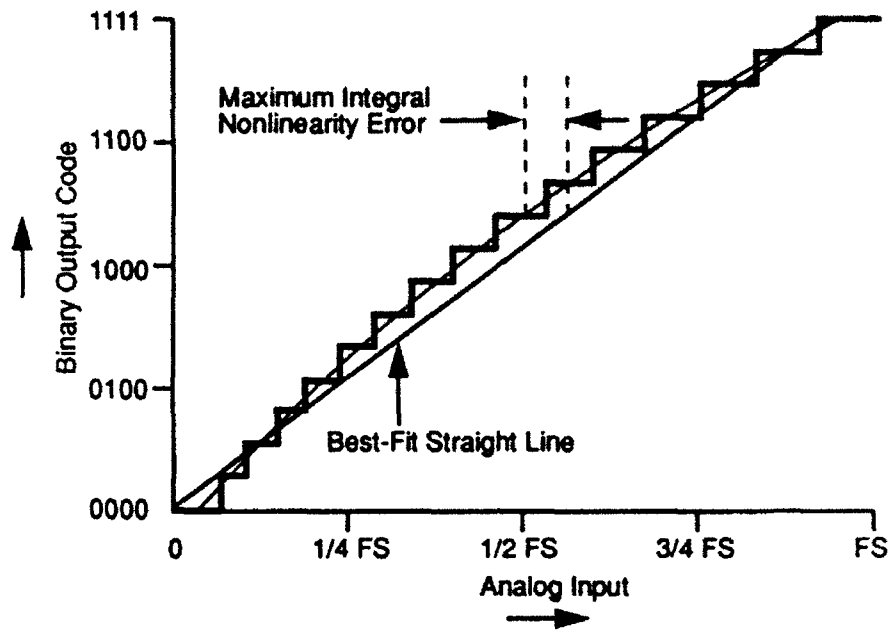


Figure 2. Errors in A/D Converters

1.2.7 Code Edge

We define the code edge [7] of output code i as the lowest input voltage V_i , so that there is at least a 50 percent probability that the output code equals or exceeds i .

1.2.8 Monotonicity

An A/D converter is monotonic [7] if the expected mean output code never decreases for increasing input voltage, and if it never increases for decreasing input voltage. It is strictly monotonic if, for any finite increase (or decrease) of the input, the expected mean output also increases (or decreases). Generally, a monotonic A/D converter is also strictly monotonic unless it has missing codes which cause a finite region of input voltage to produce the same output. The B2 specification requires that the converters for the NWS be strictly monotonic.

1.3 SUMMARY AND CONCLUSIONS

As pointed out in the introduction, we obtained a new DDC A/D converter and two three-year-old operational ADC A/D converters from Paramax which were subjected to an extensive series of dynamic tests. The objective of this study was to assess the DDC A/D converter for the NWS. Using the ADC tests as a baseline, the relative performance of the DDC unit was assessed and we also verified if it met the UAR receiver B2 performance requirements.

This report briefly describes the characteristics of the two A/D converters tested and the digital test bed used to characterize them. We analyze the data in the frequency and phase domains. Based on the spectral analysis test, we evaluate these key A/D converter dynamic parameters: the noise, effective number of bits, SFDR, SNR, and the SNDR for seven different frequencies and eight different amplitude levels at each frequency. The monotonicity of the converters is tested at a frequency of 1.25 MHz [1]. The monotonicity test is sensitive to converter noise, so to reduce the chances of drawing erroneous conclusions, we employ three different methods of analysis (histogram method, code-mean method, and code-edge method) to determine the differential nonlinearity and monotonicity

performance of the converters. The transient and overvoltage recovery tests are performed with a custom-designed pulse generator circuit. As a result of our investigation, we reach the following conclusions:

- The DDC converter exhibits its best noise performance (0.7 to 0.8 LSB RMS noise) at the B2 specified frequency band from 0.54 to 1.25 MHz. For full-amplitude, very low-frequency (i.e., 100 kHz), and high-frequency (i.e., 1.5 MHz) signals, the noise of the converter is 0.95 LSB and 1.0 LSB, respectively. For signals near the Nyquist frequency of 2.0 MHz, the noise is higher at all signal amplitude levels.
- The DDC converter loses approximately 1.3 to 1.5 bits with respect to an ideal 12-bit converter, which corresponds to 10.5 to 10.7 effective bits under most dynamic conditions. However, for full-scale amplitude signals, it loses approximately 2.2 bits at both the high (>1.5 MHz) and low frequency (0.1 MHz).
- The SFDR of this converter is 71.0 to 73.0 dB for large amplitude signals. At other frequencies it is similar to the results at 0.54 and 1.25 MHz, except at very low frequencies of 100 kHz and 270 kHz, where the distortion is higher and the SFDR is 65.0 dB for large signal amplitudes.
- The integral nonlinearity of the DDC converters is (under ± 1.0 LSB) exceptionally good at a nominal frequency of 544 kHz. At two lower frequencies of 101 and 271 kHz the integral nonlinearity is less than ± 1.5 LSB, which is three times better than the B2 specification.
- Since many subranging A/D converters behave differently with positive-going or negative-going signals, we present the monotonicity analysis for positive-going, negative-going, and combined slopes to gain better insight. The DDC converter is strictly monotonic and marginally meets the radar B2 specification requirements; it appears to have several codes which may be slightly wider.

Confirming this with high confidence would require more samples, greater than the 512 K* used in our analysis.

- The DDC converter does not meet the transient and overvoltage recovery B2 performance requirements.
- The two operational three-year-old ADC converter units do not meet most of the radar B2 specifications; however, during qualification testing of the radar three years ago, they did meet them.
- Unit 1 has 1.15 to 1.4 LSB of RMS noise for full-scale input signals, which is an excess of 0.6 LSB of noise in comparison to the DDC converter. This converter loses 2.4 to 2.9 bits for full-scale input signals, and 2.6 to 3.0 bits for signals that are 30 dB below full-scale. The SFDR of this converter is 60 to 65 dB for large signals.
- Unit 2 has 1.1 LSB of RMS noise at most of the frequencies (0.27 MHz, 0.54 MHz, and 1.5 MHz) and for different signal amplitudes at each frequency. However, at a signal frequency of 0.1 MHz, the noise rises appreciably to 3.0 LSB which may be associated with the missing code problem. This converter loses between 2.2 and 2.5 bits at all frequencies and different signal amplitudes at each level. However, for a full-scale amplitude signal with a frequency of 1.5 MHz, it loses 3.5 bits, which may be again due to the missing code problem. The SFDR of this converter is 62 to 66 dB for large signals.
- The spectrum plots of both units show an increase of 6 dB in noise floor over a wideband in the upper half of the Nyquist band, possibly caused by high-order nonlinearity which results from second-stage error correction circuitry not performing properly.

* throughout this report 1 K = 1024 samples.

- The ADC converter is nonmonotonic, it has gross errors (particularly for negative-going voltages), and it does not meet the radar B2 specification.
- The ADC converter does not meet the overvoltage and transient recovery performance B2 requirements which were not a part of the B2 specification during the qualification testing of the radar.
- The results of the Paramax/DDC and MITRE evaluations of the DDC A/D converters are summarized in table 2. The DDC converter meets all B2 performance requirements and exceeds the performance of the two three-year-old ADC units, with the exception of the overvoltage and transient recovery time, which is out-of-specification. This is not expected to present a problem, since the A/D converter in the system (receiver) is preceded by a hard limiter that is set slightly above the maximum full-scale input level. This will prevent the A/D converter from being driven to twice the full-scale input. Since the transient recovery time is only slightly out-of-specification, and the settling characteristic of this converter has a smooth exponential decay, the only system impact is a moderate attenuation of very high-frequency signal/clutter components.

1.3.1 System Impact

In this section we present a preliminary analysis [8,9,10] to evaluate the effect of converter noise on the system. The available dynamic range depends on the sensitivity of the system to harmonics, the noise produced by the A/D converter with typical input signals, and the system noise prior to conversion. For illustrative purposes, we calculate a noise figure, that is, the degradation of the SNR expressed in dB caused by imperfections of the A/D converter. Table 3 shows the effect of the two A/D converters with receiver noise set at 1.5 quanta. As shown, the DDC converter normally produces an additional 0.7 dB due to the internal noise over and above the loss from ideal quantization noise (0.16 dB). However, the three-year-old operational ADC A/D converter produces an additional loss of 1.0 dB compared to the DDC converter.

Table 2. DDC Model ADC 0015-600 A/D Converter Performance Summary

<u>Parameter</u>	<u>Receiver B2 Requirement</u>	<u>Paramax/DDC Measured Performance</u>	<u>MITRE Measured Performance</u>
Voltage Range	± 2.048 volts	Meets Requirement	Meets Requirement
Conversion Time	Data valid 275 ± 25 nanoseconds after third encode	Meets Requirement	Meets Requirement
Integral Linearity	± 0.1 percent of full-scale ± 0.5 LSB	Meets Requirement	Meets Requirement
Monotonicity	No missing codes, each code > ten percent < 190 percent of nominal	Meets Requirement	Meets Requirement
ac Linearity	At 0.54 MHz - spurious 70 dB below full-scale	Meets Requirement	Meets Requirement (-73 dB)
SNR	At 0.54 MHz, 63 dB minimum RMS signal-to-RMS noise	Meets Requirement (70 dB)	Meets Requirement (65 dB)
Transient Response and Overvoltage Recovery Time	Transient response (for full step input): Attains full-scale accuracy to ± 5.0 mV in 200 nanoseconds maximum	Meets Requirement (3.0 LSB)	Does Not Meet Requirement Note 1 (7.0 LSB)
	Overvoltage recovery time (for 2X full-scale input): recovers to ± 5.0 mV of 12-bit accuracy within 200 nanoseconds	Meets Requirement (5.0 LSB)	Does Not Meet Requirement Note 2 (12.0 LSB)

Note 1: 240 nanoseconds 5 LSB

Note 2: 340 nanoseconds 5 LSB

Since the radar is in operation with the ADC converter, and appears to be fully functional despite its converters being out-of-specification, we recommend an additional study to evaluate the system impact of not meeting the specifications.

The new DDC converter meets most the B2 Specifications, as did the ADC converter units during qualification testing of the radar. Our test results revealed that the three-year-old ADC converter units did not meet any of the specifications. We recommend that the DDC converter performance be checked over an extended period of time, after being in operation for roughly three years, to ensure that it will not impact the system performance.

The present test methods for the converter based on sine waves are not adequate because it is difficult to correlate the results with real-world radar performance. Perhaps new test methods employing simulated radar signals may be required to quantify the degradation effects clearly, and provide additional insight showing how a system's parameters will dictate specifications for a converter.

Table 3. System SNR Loss Caused by Two A/D Converters

	<u>Converter Type</u>	
	<u>DDC</u>	<u>Analog Devices</u>
Receiver Noise (in LSB)	1.5	1.5
A/D Converter Noise (in LSB)	0.7-1.3*	1.1-3.0**
Total Noise (in LSB)	1.65-1.98	1.86-3.35
Loss (in dB)	0.86-2.43	1.87-6.98

* Noise is less than 0.8 LSB RMS, except with high-frequency (>1.5 MHz) signals within 5.0 dB of saturation. This is not a normal input condition.

** The 3.0 LSB figure is produced by the errors caused by missing codes, which result from high-frequency (>1.0 MHz) signals with an amplitude near full-scale, which is not a normal input condition.

SECTION 2

DESCRIPTION OF TWO A/D CONVERTERS AND THE A/D INSTRUMENTATION FACILITY

2.1 CHARACTERISTICS OF TWO NWS A/D CONVERTERS

Currently, the NWS uses the ADC 12-bit, 5-MHz A/D converter model MOD-1205, employing a two-stage digital correcting subranging architecture with pipelining. The digital output has a delay of three clock cycles, plus 0.275 microseconds (μsec) after the input is sampled. At a 4-MHz sampling rate, the digital output has a total delay of 1.025 μsec . The converter has a nominal linear range from -2.048 to + 2.047 volts (V), and a resolution of 12 bits (which corresponds to 0.001 volt (one millivolt)). The input impedance is selectable by an external connection to be either 50.0 or 400.0 ohms.

DDC manufactured model ADC-00115-600 as a replacement (illustrated in figure 1(b)). Because it is intended to be a replacement, it is based on a printed circuit board which has the same size, mounting provisions, connector pinout, and location as the ADC unit. However, it is based on a small hybrid circuit assembly which is a complete 12-bit A/D converter. In addition to the hybrid assembly, a few components produce an input/output interface that is identical to the ADC converter. Much of the DDC converter circuit board is empty in comparison to the ADC converter. Table 4 shows the primary specifications of both.

2.2 DESCRIPTION OF THE DIGITAL TEST BED

To study A/D converter limitations on signal processing algorithms used in communication and radar systems, we developed a systematic approach to characterizing high-bandwidth and/or high-resolution A/D converters [4]. The investigation analyzed the technical issues involved in accurately evaluating them in the frequency and phase domains [7], including the construction of a versatile, high-performance, A/D instrumentation facility.

Table 4. Summary of the Most Important Characteristics of the A/D Converters*

<u>Manufacturer</u>	<u>ADC</u>	<u>DDC</u>
Bits	12	12
Conversion Rate (MHz)	5.0	5.0
Full-Scale Range (± 2.098 Volts)	4.096	4.096
Data Output Pipeline Delay (Cycles)	3.0	3.0
Data Output Delay (μsec)	0.275	0.275
Input Impedance (Ohms)	50/400	50/400
Overvoltage Range (Volts)	± 4.0	± 4.0
Supply Voltages	$\pm 15, + 5, -6$	$\pm 15, + 5, -6$
Total Power (W)	13.0	10.0
SNR (dB) for 0.54 MHz Signal	66.0	64.0
SFDR (dB)		
from dc to 1.0 MHz	70.0	70.0
1.0 MHz to 2.5 MHz	65.0	65.0
Transient Recovery Time (μsec)	0.2	0.2
Settling Accuracy (Millivolt)	0.5	0.5

*Based on manufacturer's specification

Digital testing requires taking blocks of digital data from the A/D converter, storing them in real time in a data acquisition memory, and then transferring them to a computer, where various analyses are performed in temporal, spectral, and statistical domains. This prevents

any reconstruction errors that can occur when the digital samples are converted back to analog values via a digital-to-analog (D/A) converter.

Figure 3 illustrates digital testing of an A/D converter in block diagram form. A detailed description of the A/D instrumentation capability at MITRE-Bedford is listed in table 5. The core of the instrumentation facility consists of very high-speed, high-capacity (dual-input or single-interleaved mode) data acquisition memories. One data acquisition memory can log data records up to two megawords (Mwords) in a dual channel mode or four Mwords in an interleaved mode. A second data acquisition memory is expandable up to 16 (dual) or 32 (interleaved mode) Mwords. Each input channel can accept data words up to 16 bits wide at a rate up to 100 Mwords per second (200 in interleaved mode). The two-channel capability is a convenient feature for the characterization of A/D interfaces such as digital radios and radar systems with complex inphase and quadrature outputs. The data acquisition system is supported by two personal computers (PCs) for data analysis and software development. The analog sources shown in figure 3 are just a sample of the type of signal generators available; they represent the kind of analog input signals that the A/D converter might encounter in a real-world communication or radar environment (e.g., narrowband and/or broadband, signal, jammer, noise, or clutter). Their outputs are further conditioned for better noise and/or linearity with passive filters before being applied to the A/D unit under test. A photograph of the A/D instrumentation laboratory is shown in figure 4.

The sine-wave is applied to the A/D converter under test and the resulting digital output is stored in the Tektronix High-Speed Data Cache, a large, fast, sequentially-addressed memory. A Compaq PC controls it via an IEEE-488 bus, employing DADiSP, a general-purpose signal processing program. A macro command entered at the keyboard commands the Data Cache to store 64 K (65536) consecutive data points, and then transfer them to the Compaq PC. The data record is displayed on the screen, and then stored as a file on a floppy disk.

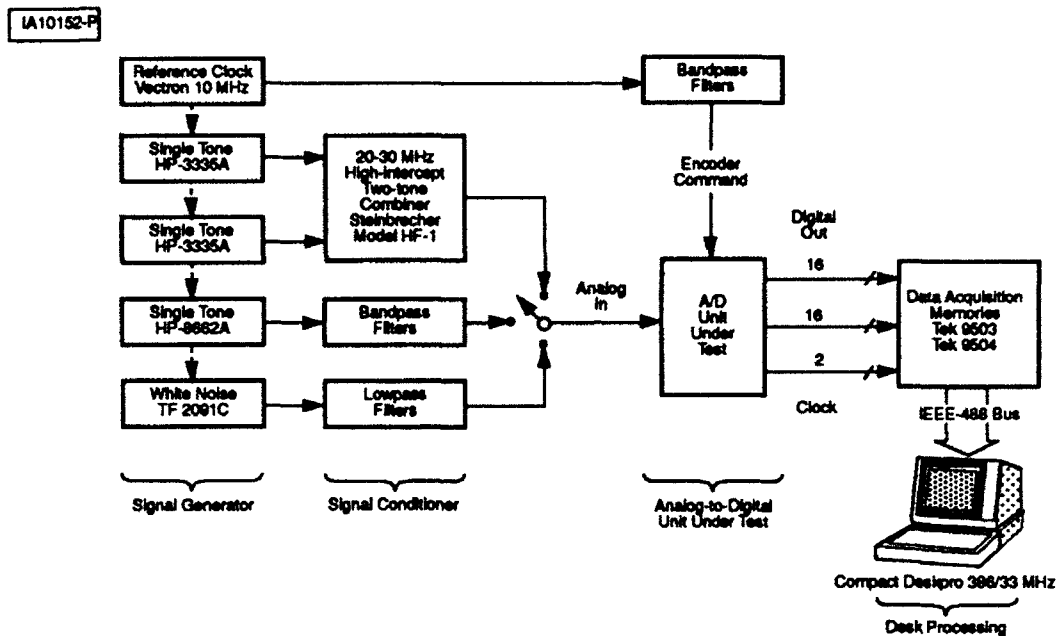


Figure 3. A/D Instrumentation Facility Generic Block Diagram



Figure 4. A/D Instrumentation Facility

Table 5. A/D Instrumentation Capability

<u>Function</u>	<u>A/D Instrumentation Hardware and Software Description</u>
Signal Generator	HP-3335A(2), HP-3325A, TF-2096, HP-8662A, HP-8644A, HP8656B, KH4400A, ...
Signal Conditioner	Passive bandpass and low-pass filters (30, HF-1 high-intercept two-tone combiner)
Data Acquisition	Tek 9503, 100-Msps (ECL), 25-Msps (TTL), 16-bit (two-channel), 2-Mword/channel
	Tek 9504, 100-Msps (ECL), 25-Msps (TTL), 16-bit (two-channel), 16-Mword/channel
	MITRE custom memory, 50-Msps (ECL), 16-bit (one-channel), 4-kword/channel
Data Processing	Compact Deskpro 386/33 MHz, 200-Mb hard disk, 16-Mb RAM
	Compact Deskpro 386S/25 MHz, 80-Mb hard Disk, 16-Mb RAM HP-9386 (2), Laser Printer
Software	Digital Signal Processing Spreadsheet (DADiSP) Excel, Turbo Pascal, Turbo C++, Axum Graphics, IEEE488, ... MITRE custom A/D characterization software and macros

2.3 PHASE-PLANE ANALYSIS OF CONVERTERS WITH SINE WAVES

In many signal processing applications, the dynamic performance of an A/D converter is characterized by the spectral analysis test, which consists of applying a series of sinusoidal signals of different frequencies and different amplitudes, and analyzing the frequency spectrum of the output to characterize the nonlinearities and noise. It does give accurate measurements for the large-scale statistics, such as harmonic distortion and total noise of the A/D converter, but it is difficult to determine the error sources within the device.

Phase-plane analysis [11] evaluates the errors and noise at each code level of the A/D converter and provides insight into the internal behavior of the device. It is a way of manipulating a mass of noisy data so that measurements made under similar input conditions can be correlated. By evaluating statistical properties of small subgroups of the total data, underlying causes of correlations are revealed. This technique is extremely useful with high-resolution A/D converters. A sine wave is applied to the input, and the output data is recorded. Using all of these points, we create an estimator that evaluates the exact instantaneous input voltage associated with each of the measured points.

2.3.1 Sine-Wave Estimation

Given samples of a waveform which is dominated by a sine wave with small additional harmonic distortion and noise, several algorithms can estimate the fundamental sine-wave component. Peetz et al. [12] present a very brief description of a general algorithm for sine-wave curve fitting, requiring an initial estimate of the signal frequency (accurate to five or six significant digits). Frothing et al. [13] simplify the algorithm for the special case where the signal frequency is known precisely. This requires phase-locked oscillators for the test setup, which may not be available. Appendix A presents a general iterative algorithm which is an improved version of Peetz's method, computing the sine wave entirely from the measured data. In our test setup, we employ extremely stable, phase-locked oscillators for the signal and sampling clock. The frequencies of the sine waves are chosen so that there is a prime integer number of complete cycles in a data record, allowing us to use a fast algorithm to estimate the sine wave (a generalization of Frothing's method).

We start with a set of N measurements, V_i , for $i = 1, 2, \dots, N$ for a waveform consisting of a large fundamental component, F_i , plus measurement errors and noise, e_i . The fundamental is determined by four parameters: the offset, M ; amplitude, A ; radian frequency, ω ; and initial phase, θ .

$$F_i = M + A \cos(\omega i + \theta) \quad i = 1, 2, \dots, N \quad (1)$$

$$F_i = M + B \sin(\omega i) + C \cos(\omega i) \quad i = 1, 2, \dots, N \quad (2)$$

where

$$A = \sqrt{B^2 + C^2}; \quad \theta = \tan^{-1}(B/C). \quad (3)$$

$$V_i = F_i + e_i \quad i = 1, 2, \dots, N \quad (4)$$

Let us define K , K_S , and K_C as

$$K = \sum_{i=1}^N V_i \quad (5)$$

$$K_S = \sum_{i=1}^N V_i \sin(\omega i) \quad (6)$$

$$K_C = \sum_{i=1}^N V_i \cos(\omega i). \quad (7)$$

Substituting equations (2) and (4) into equations (4) to (6), and assuming that the e_i 's are uncorrelated with the $\sin(\omega i)$ and $\cos(\omega i)$, results in three simultaneous equations in three unknowns: M , B , and C :

$$K = Ms + Bs_s + Cs_c \quad (8)$$

$$K_S = Ms_s + Bs_{ss} + Cs_{sc} \quad (9)$$

$$K_C = Ms_c + Bs_{sc} + Cs_{cc} \quad (10)$$

where

$$s = \sum_{i=1}^N 1; \quad s_s = \sum_{i=1}^N \sin(\omega i); \quad s_c = \sum_{i=1}^N \cos(\omega i)$$

$$s_{sc} = \sum_{i=1}^N \sin(\omega i) \cos(\omega i); \quad s_{ss} = \sum_{i=1}^N \sin^2(\omega i); \quad s_{cc} = \sum_{i=1}^N \cos^2(\omega i). \quad (11)$$

The three unknowns M , B , and C are determined by solving the three simultaneous equations. However, they require that the errors, e_i , must be uncorrelated.

2.3.1.1 Spectral Analysis Tests

For the spectral analysis tests, the signal amplitude is chosen to maintain the A/D converter within its linear range, and the frequency is chosen so that there is an exact integer number of cycles within the data record. Hence, all of the measured samples are valid, and the s 's can be computed independently of the measurements.

$$s = N; \quad s_s = s_c = s_{sc} = 0; \quad s_{ss} = s_{cc} = N/2 \quad (12)$$

The unknowns M , B , and C are computed from

$$M = \frac{K_s}{s} = \frac{1}{N} \sum_{i=1}^N V_i \quad (13)$$

$$B = \frac{K_s}{s_{ss}} = \frac{2}{N} \sum_{i=1}^N V_i \sin(\omega i) \quad (14)$$

$$C = \frac{K_c}{s_{cc}} = \frac{2}{N} \sum_{i=1}^N V_i \cos(\omega i). \quad (15)$$

2.3.1.2 Monotonicity Tests

For the monotonicity tests of the DDC converter (described in section 4), the signal amplitude is chosen to exercise all possible output codes, and hence drive the A/D converter into saturation; the output is a clipped sine wave, and the errors are large at the signal peaks. In our data analysis we eliminate the saturated samples from the data record, so M, B, and C cannot be computed from equations (13), (14), and (15). The frequency is chosen so that there is an exact integer number of cycles within the data record. The output codes of the unsaturated samples have an absolute value of < 2047 . Using all of the unsaturated samples within the data record, the coefficients M, B, and C are determined by solving the simultaneous equations (8), (9), and (10). The results of the analysis are presented in section 4.

2.3.2 Phase-Plane Data Analysis

For each data point, the input voltage and the phase of the input sine wave are calculated. The measurements and associated errors are resorted in order of the signal phase angle from 0 to 2π , grouping together the measurements made under similar input conditions, but at different times [11]. If multiple data records are available, the data can be combined into this table.

This sorting maintains separation of the two ways of having the same input voltage with positive and negative slopes. By averaging the error over a small region in phase space, we obtain an estimate of the typical error under the input condition at the center of that region. This is a measure of the device distortion at that input signal phase. The spread of the measurement errors within a region, as calculated by their standard deviation, is a measure of the device noise. This allows for the determination of an estimator of the device noise for different signal phases and voltages. It is frequently possible to associate one or more regions of high noise with specific problems in the device's internal construction. The

regions of high noise with specific problems in the device's internal construction. The complete test requires a series of measurements at different frequencies and amplitudes. The results presented in sections 3 and 4 employ the phase-plane analysis.

SECTION 3

SINGLE-TONE TEST RESULTS

As discussed in section 1.1, A/D converter performance is measured at the frequency of interest by sampling a sine wave and performing a fast Fourier Transform (FFT) on the digital output data. It is generally desirable to test an A/D converter at many different signal frequencies and at different signal amplitude levels at each frequency. As the input frequency is increased, the measured SNR of the A/D converter tends to decrease. This high-frequency performance degradation of the SNR is indirectly related to the signal's input slew rate.

Since the sampling rate of the A/D converter is 4.0 MHz, we test both converters with an input signal frequency near the Nyquist frequency. We test the DDC converter at seven different frequencies of 0.1 MHz, 0.27 MHz, 0.54 MHz, 1.0 MHz, 1.25 MHz, 1.5 MHz, and 2.0 MHz, respectively, and at eight different amplitude levels of 0 dB, -1 dB, -3 dB, -6 dB, -12 dB, -18 dB, -24 dB, and -30 dB, relative to a full-amplitude signal that toggles all the bits. The sampling frequency for every case is 4.0 MHz. We test the ADC Unit 1 A/D converter at two different frequencies, and we test the ADC Unit 2 A/D converter at four different frequencies.

Based on the spectrum of the data, we determine the dynamic parameters, effective number of bits, SNR, and SFDR, as discussed in section 1.2. We also compute the dynamic parameters of the converters by generating a mathematically perfect sine wave from the digitized data, as described in section 2. The difference between the digitized data and the perfect sine wave is the error associated with each data point. We then analyze the errors to evaluate distortion, noise, bits lost, and the dependence of the errors upon signal voltage. We present plots of the number of bits lost, SFDR, noise, and SINAD versus input signal level, and some typical FFT spectral responses.

The B2 performance requirements for the baseline converter are identified in table 1. In this section, we are only validating the RMS-signal-to-RMS noise ratio, SFDR, and integral linearity requirements. The other B2 requirements are verified in sections 4 and 5.

3.1 TEST RESULTS FOR THE DDC 12-BIT, 4-MHZ A/D CONVERTER

Our analysis of the test results for the DDC 12-bit, 4-MHz A/D converter at seven different input signal frequencies is presented on the following pages, in the form of plots, as follows: noise versus input signal level under dynamic conditions (figure 5); SINAD versus input signal level (figure 6); bits lost versus input signal level (figure 7); SFDR as a function of input signal level (figure 8); and the FFT spectral response for the full-amplitude and the 30 dB-below-full-amplitude sine-wave signals (figures 9(a) through 9(n)).

Table 6 lists the measured dynamic performance at seven different input signal frequencies. This converter exhibits its best noise performance at the B2 specified frequency band from 0.54 to 1.25 MHz. At these frequencies, the RMS noise is 0.7 to 0.8 LSB for full-scale input. For signal amplitudes 5 dB below the maximum the noise reduces to 0.6 LSB, which is 7.0 dB greater than an ideal 12-bit A/D converter quantization noise. For a signal frequency of 0.27 MHz, the noise performance is 0.7 LSB, independent of signal amplitude. For full-amplitude very-low frequency signals (i.e., 100 kHz), the noise increases to 0.95 LSB. However, for signal amplitude 10 dB below the maximum (at 100 KHz) the noise performance is similar to that at 0.54 MHz (i.e., 0.6 LSB), but at a 1.5 MHz signal frequency, it is almost the same as that of 100 kHz for all amplitude levels except the full-scale amplitude. For full-scale amplitude signals at 1.5 MHz, the noise is slightly higher and is equal to 1.0 LSB. For signals near the Nyquist frequency of 2.0 MHz, the noise is higher at all signal amplitude levels. This is approximately 0.75 LSB for signals less than 15 dB below the maximum and rises smoothly to 1.3 LSB for signals at the maximum amplitude.

Figure 6 shows that the SINAD performance is extremely good at a signal frequency of 0.54 MHz, but somewhat poorer at 1.25 MHz. For small signal amplitudes (15 dB below the maximum) the SINAD is constant at 65 dB for all frequencies and amplitudes. However, for

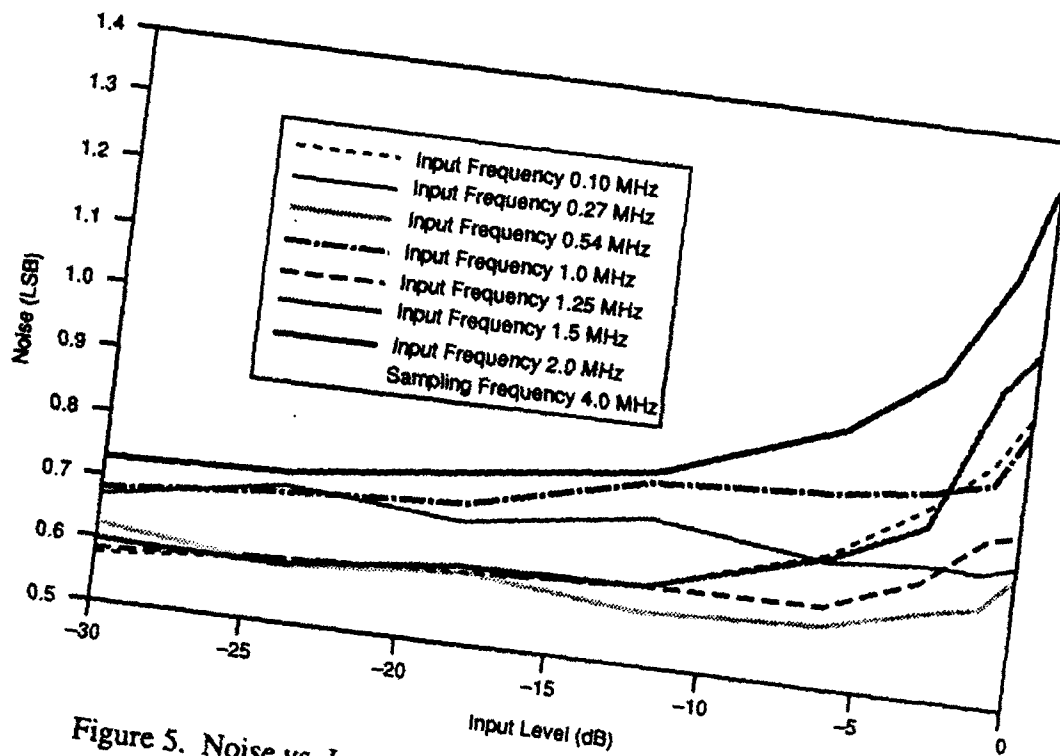


Figure 5. Noise vs. Input Signal Level for the DDC A/D Converter

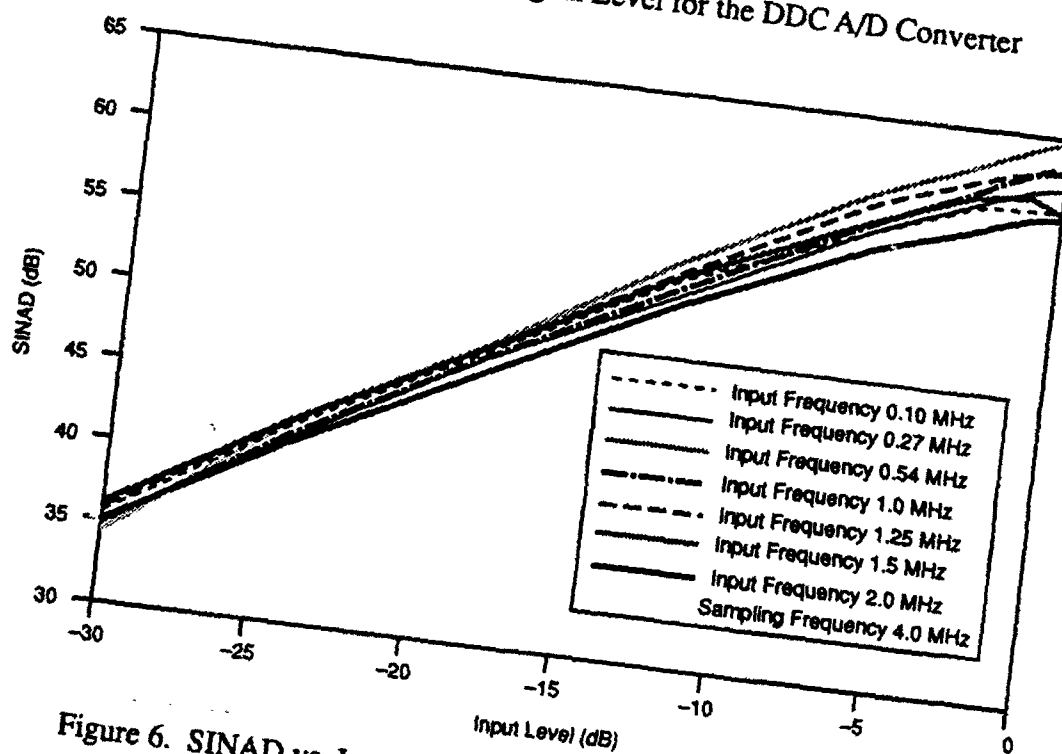


Figure 6. SINAD vs. Input Signal Level for the DDC A/D Converter

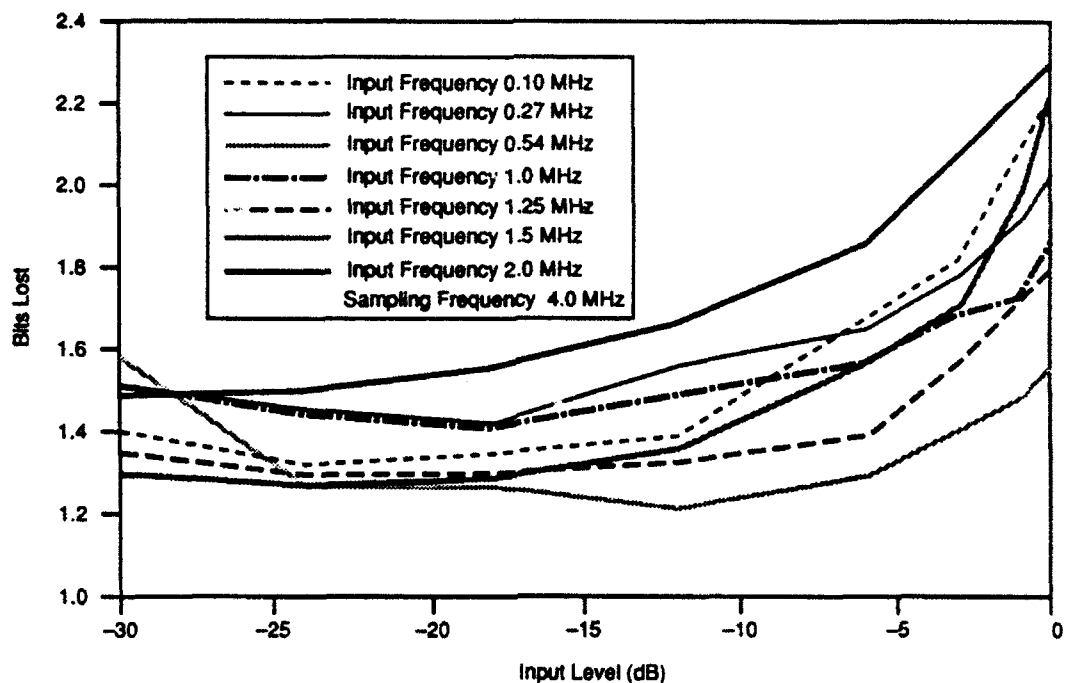


Figure 7. Bits Lost vs. Input Signal Level for the DDC A/D Converter

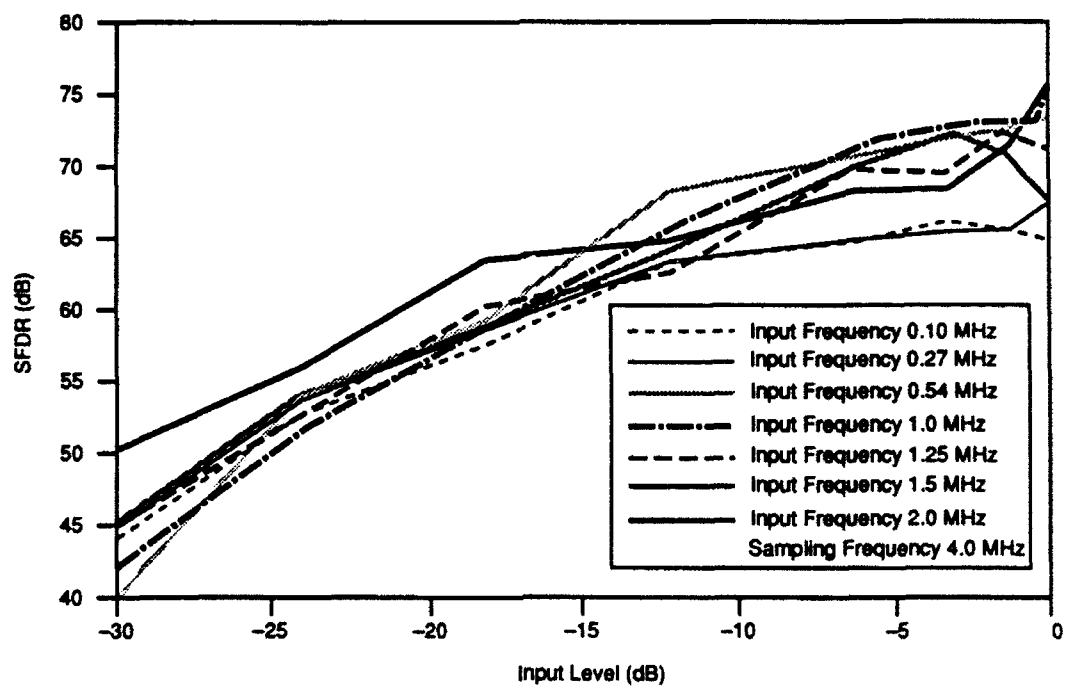


Figure 8. SFDR vs. Input Signal Level for the DDC A/D Converter

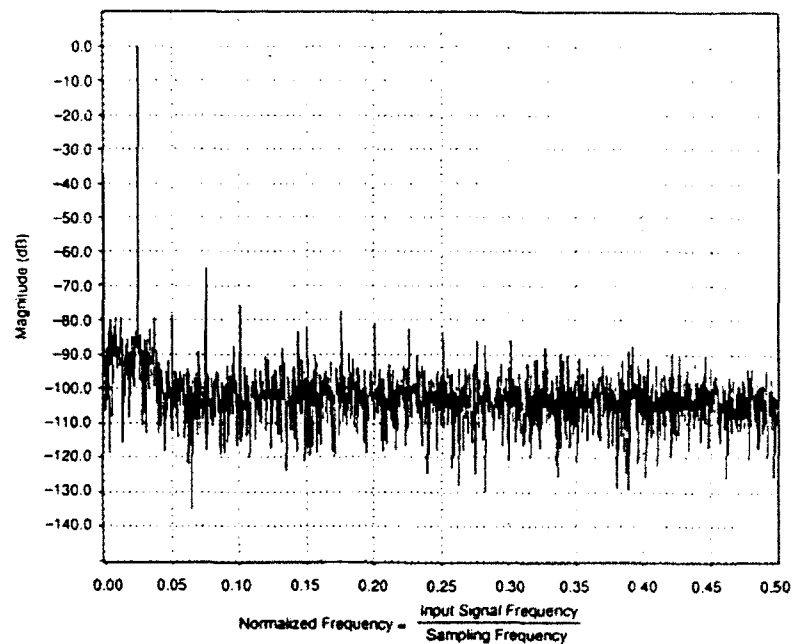


Figure 9(a). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 0.10 MHz; Amplitude of the Signal = Full-Scale)

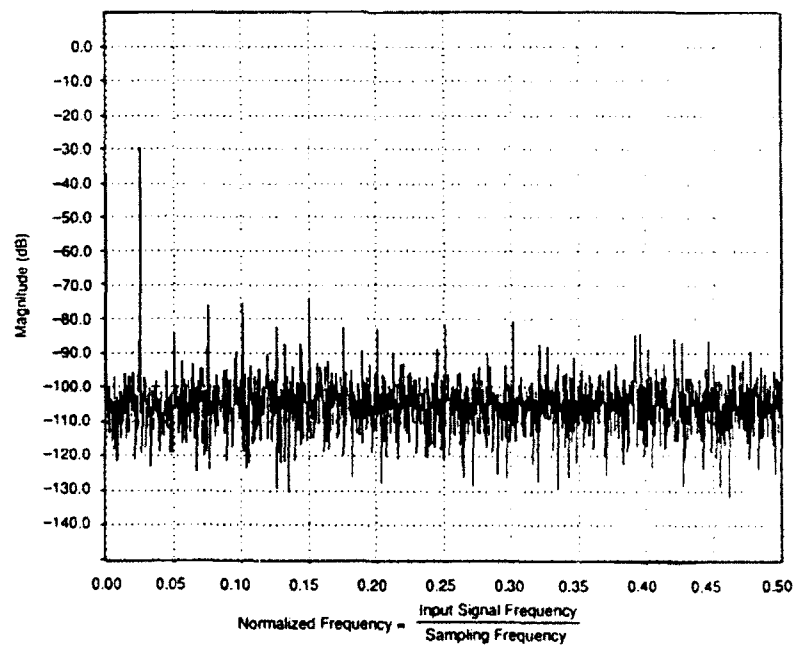


Figure 9(b). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 0.10 MHz; Amplitude of the Signal = -30 dB)

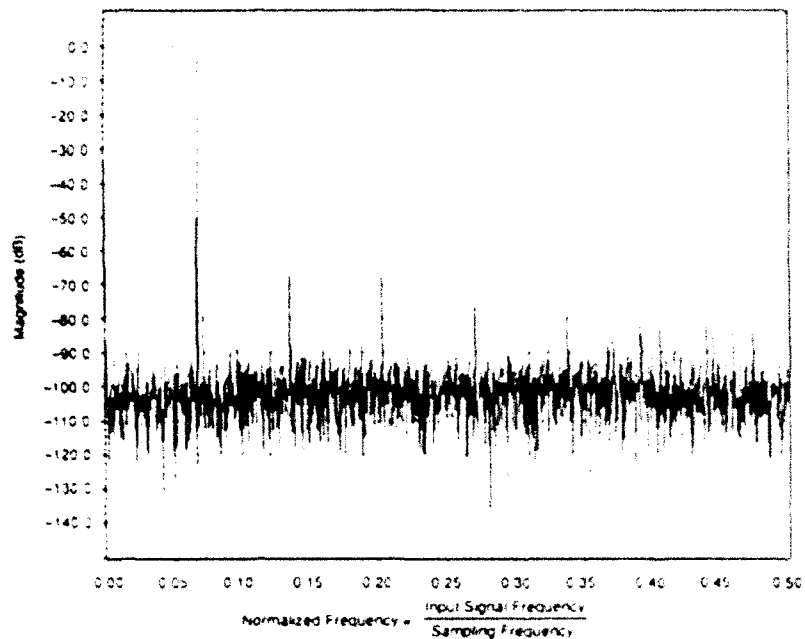


**Figure 9(c). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 0.27 MHz; Amplitude of the Signal = Full-Scale)**

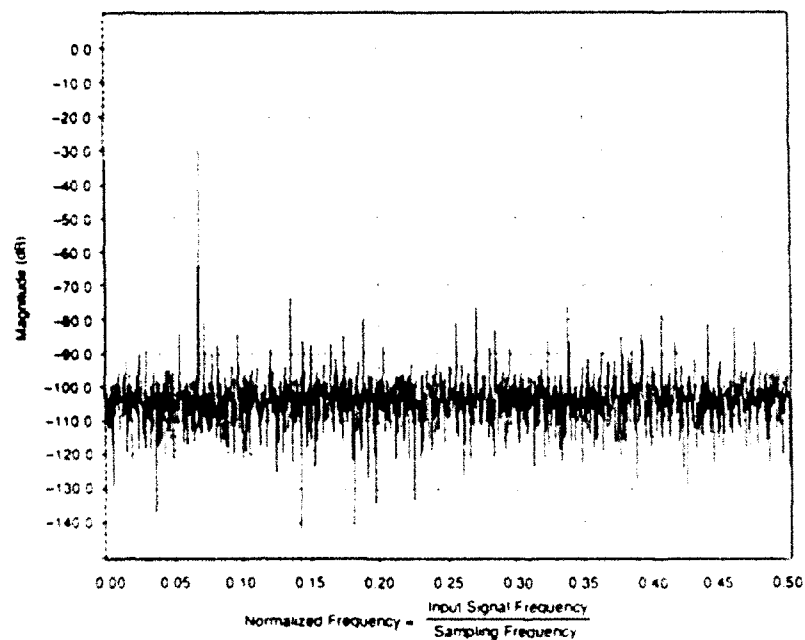


**Figure 9(d). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 0.27 MHz; Amplitude of the Signal = -30 dB)**

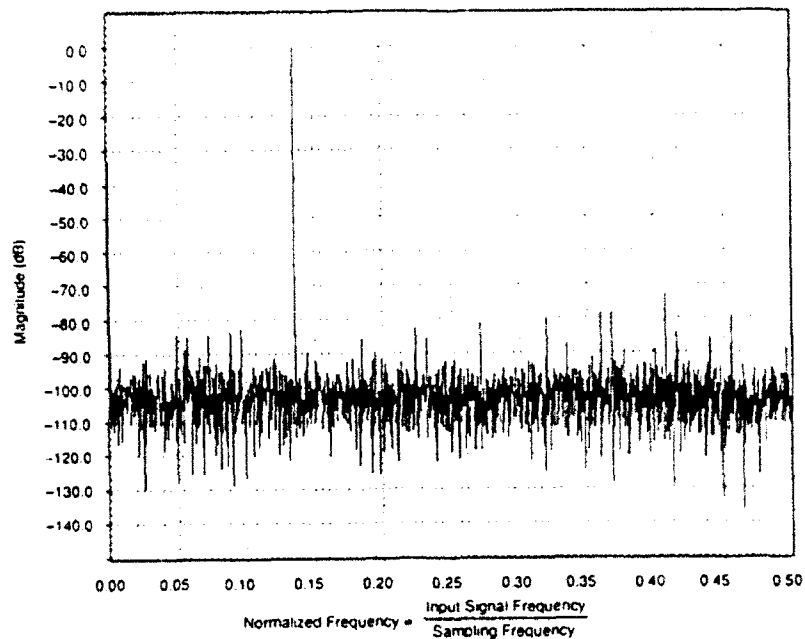


Figure 9(e). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = Full-Scale)

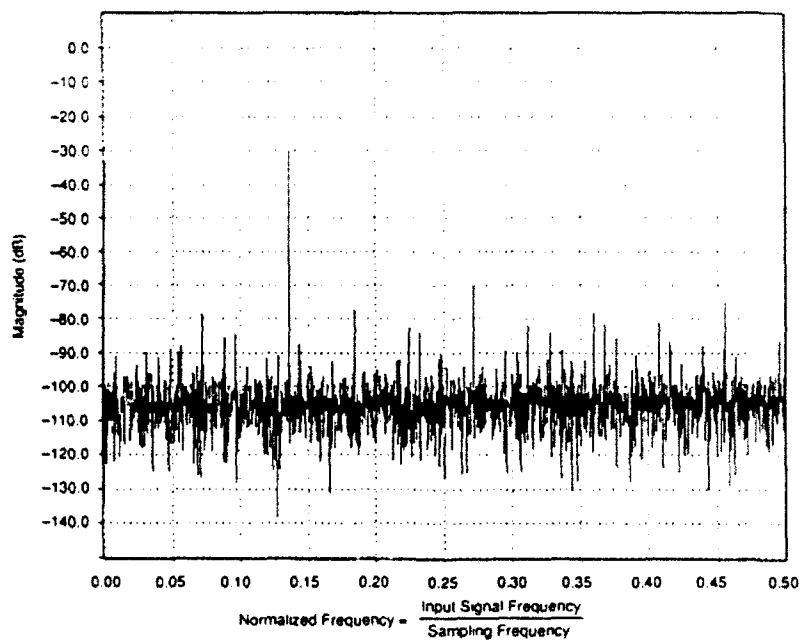


Figure 9(f). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = -30 dB)

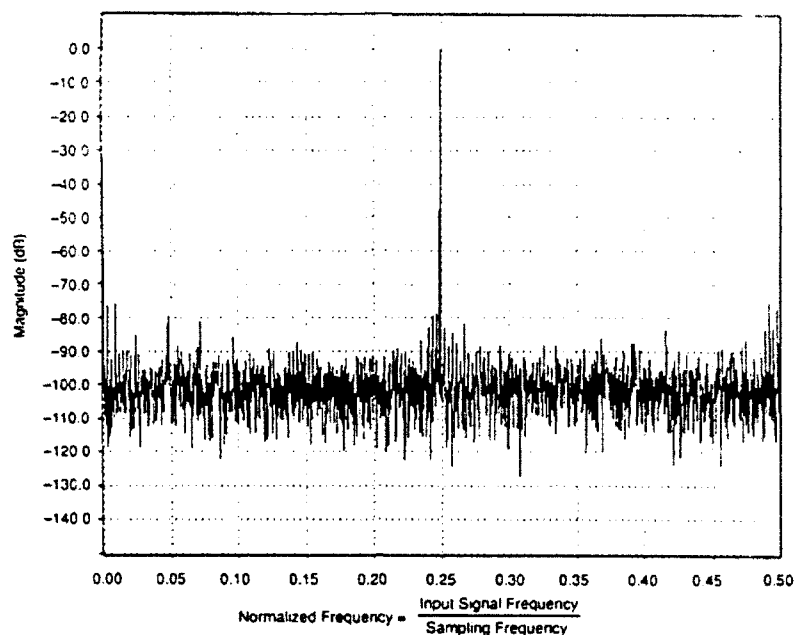


Figure 9(g). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 1.0 MHz; Amplitude of the Signal = Full-Scale)

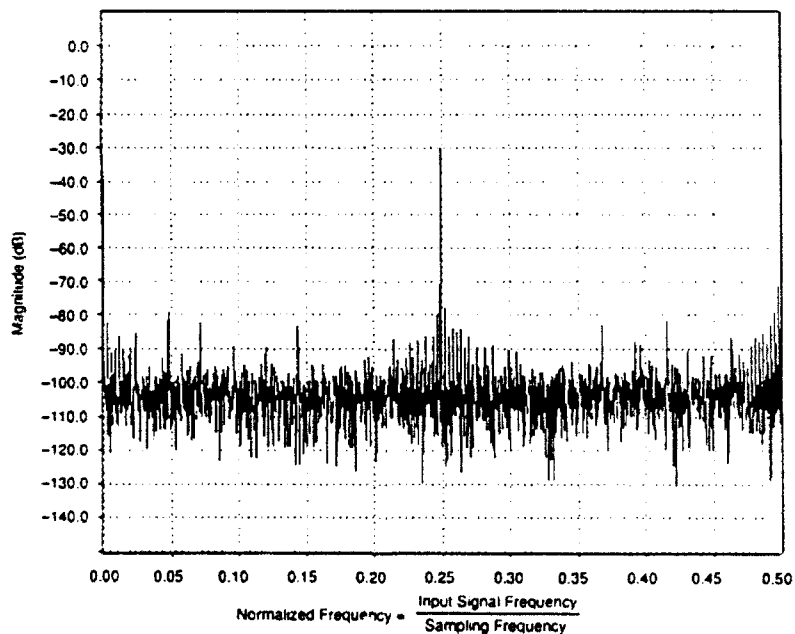


Figure 9(h). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 1.0 MHz; Amplitude of the Signal = -30 dB)

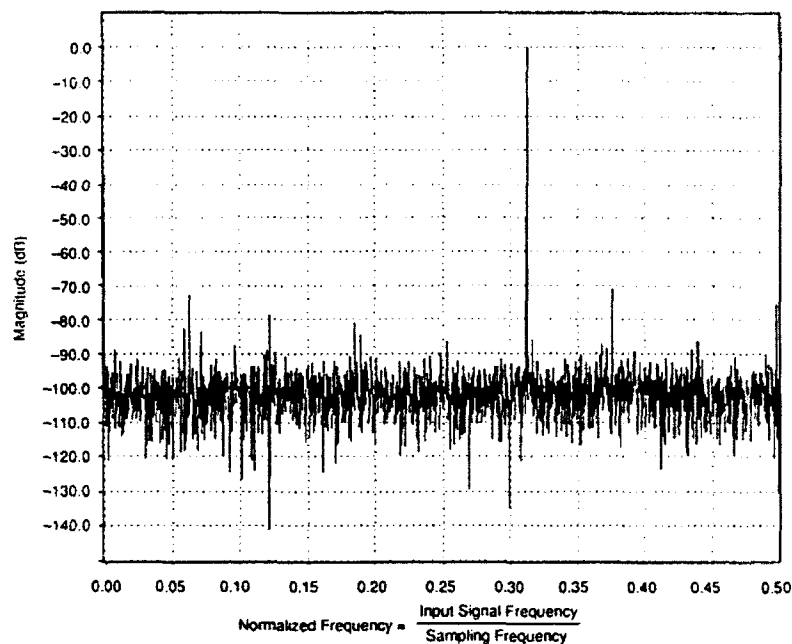


Figure 9(i). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 1.25 MHz; Amplitude of the Signal = Full-Scale)

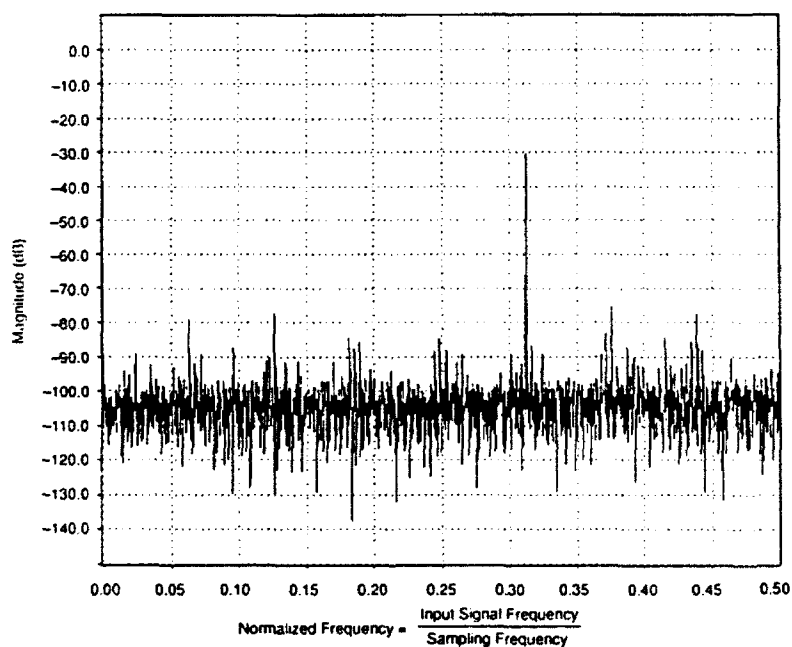


Figure 9(j). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 1.25 MHz; Amplitude of the Signal = -30 dB)

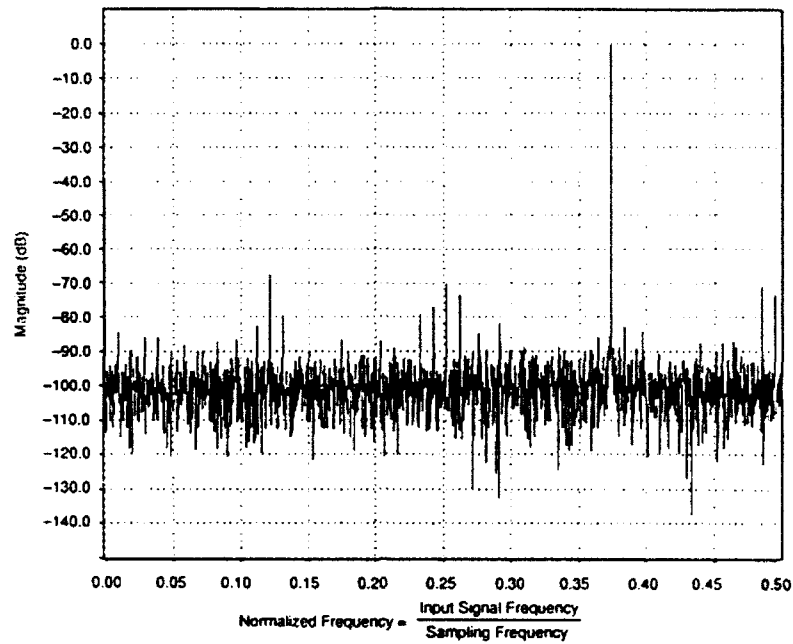


Figure 9(k). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 1.5 MHz; Amplitude of the Signal = Full-Scale)

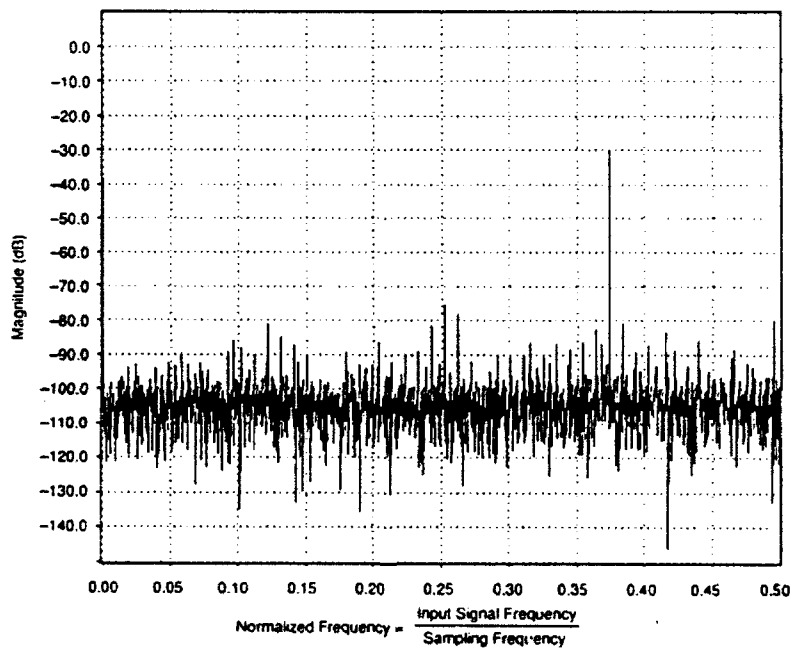


Figure 9(l). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 1.5 MHz; Amplitude of the Signal = -30 dB)

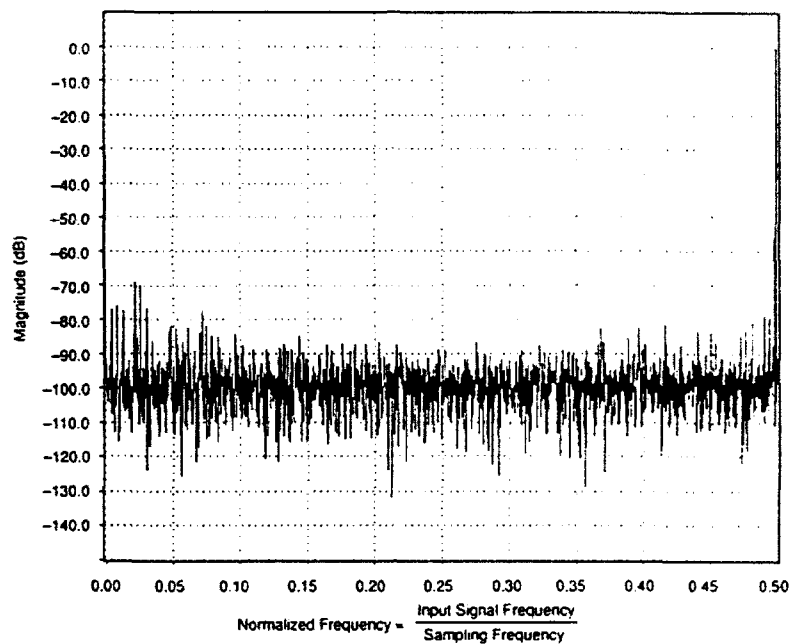


Figure 9(m). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 2.0 MHz; Amplitude of the Signal = Full-Scale)

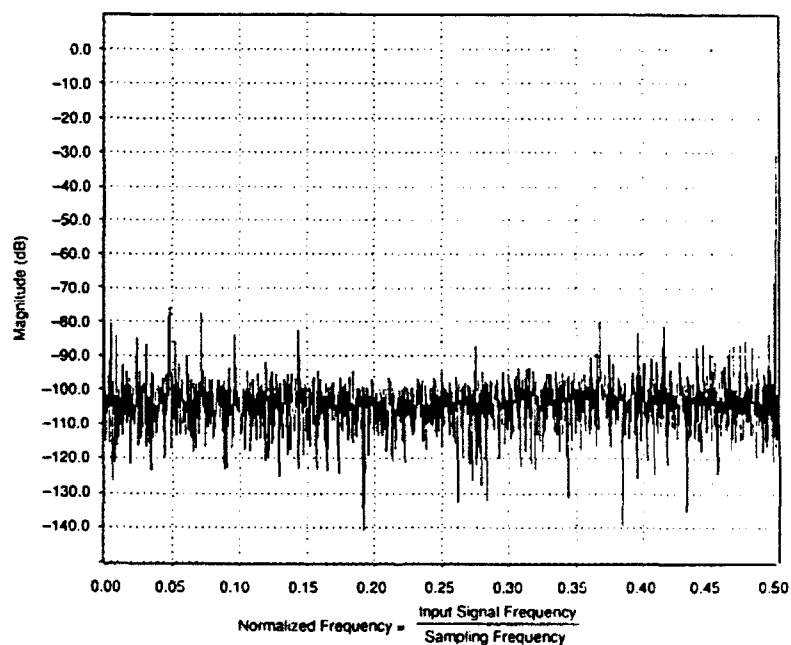


Figure 9(n). FFT Spectral Response for the DDC A/D Converter
(Input Signal Frequency = 2.0 MHz; Amplitude of the Signal = -30 dB)

Table 6. Measured Dynamic Performance of 12-Bit, 4-MHz DDC A/D Converter

Signal Frequency (MHz)	Amplitude (dB)	<u>SNR</u>		Effective Bits	SFDR (dB)
		With Harmonics (dB)	Without Harmonics (dB)		
0.10	0	60.6	63.5	9.8	64.7
0.10	-1	60.4	62.8	9.9	65.3
0.10	-3	60.1	62.1	10.2	65.9
0.10	-6	58.0	59.2	10.3	64.5
0.10	-12	53.7	55.2	10.6	63.0
0.10	-18	47.9	49.5	10.7	57.4
0.10	-24	42.1	43.5	10.7	52.6
0.10	-30	35.6	37.9	10.6	44.2
0.27	0	61.7	65.9	10.0	67.0
0.27	-1	61.5	65.1	10.1	65.4
0.27	-3	60.3	63.1	10.2	65.2
0.27	-6	58.1	60.3	10.4	64.6
0.27	-12	52.7	54.0	10.5	63.3
0.27	-18	47.5	48.5	10.6	58.4
0.27	-24	41.3	42.2	10.6	54.0
0.27	-30	35.0	36.9	10.5	44.1
0.54	0	64.7	66.1	10.5	72.2
0.54	-3	62.6	63.9	10.6	71.6
0.54	-6	60.3	61.4	10.7	70.4
0.54	-12	54.8	55.6	10.8	68.0
0.54	-18	48.5	49.2	10.7	59.0
0.54	-24	42.4	43.4	10.7	53.9
0.54	-30	34.5	37.1	10.4	40.3
1.00	0	62.9	63.6	10.1	76.0
1.00	-1	62.7	63.5	10.3	73.7
1.00	-3	61.0	61.9	10.3	73.4
1.00	-6	58.6	59.2	10.4	72.2
1.00	-12	53.1	53.5	10.5	66.3
1.00	-18	47.6	48.2	10.6	59.2
1.00	-24	41.4	42.3	10.6	51.6
1.00	-30	34.8	36.7	10.5	41.8

Table 6. (Concluded)

Signal Frequency (MHz)	Amplitude (dB)	SNR		Effective Bits	SFDR (dB)
		With Harmonics (dB)	Without Harmonics (dB)		
1.25	0	63.1	65.2	10.2	70.8
1.25	-1	62.7	64.3	10.3	72.2
1.25	-3	61.7	63.3	10.5	69.3
1.25	-6	59.7	61.0	10.6	69.6
1.25	-12	54.1	55.1	10.7	62.5
1.25	-18	48.3	49.2	10.7	60.0
1.25	-24	42.3	43.5	10.7	52.6
1.25	-30	35.9	37.8	10.7	45.2
1.50	0	60.4	62.6	9.7	67.6
1.50	-1	61.1	62.1	10.0	70.4
1.50	-3	60.8	62.4	10.3	71.7
1.50	-6	58.7	60.1	10.5	69.4
1.50	-12	53.9	55.3	10.7	64.0
1.50	-18	48.4	49.5	10.7	58.7
1.50	-24	42.4	43.7	10.7	53.9
1.50	-30	36.2	37.7	10.7	45.5
2.00	0	60.1	60.5	9.7	75.6
2.00	-1	59.7	60.5	9.8	71.4
2.00	-3	58.5	59.7	9.9	68.2
2.00	-6	56.9	57.7	10.1	68.2
2.00	-12	52.1	52.6	10.4	64.6
2.00	-18	46.7	47.0	10.5	63.3
2.00	-24	41.0	41.4	10.5	55.9
2.00	-30	35.1	35.5	10.5	50.2

signal amplitudes near the maximum the SINAD is approximately equal to 65 dB at 0.54 MHz, but at other frequencies it is up to approximately 6 dB less.

Figure 7 shows that for most signal amplitudes and frequencies, the DDC converter loses approximately 1.3 to 1.5 bits with respect to an ideal 12-bit converter, which corresponds to 10.5 to 10.7 effective bits under dynamic conditions. However, for full-scale amplitude signals, it loses approximately 2.2 bits at both the high (>1.5 MHz) and low frequency (0.1 MHz).

The SFDR is 71.0 to 73.0 dB for large signal amplitudes. At other frequencies it is similar to the results at 0.54 and 1.25 MHz, except at very low frequencies of 100 kHz and 270 kHz, where the distortion is higher and the SFDR is 65 dB for large signal amplitudes. The B2 specification specifies that for a signal frequency that is 0.54 MHz near full-scale, the minimum RMS SNR of the converter must be 63 dB. The SFDR (for signal frequencies 0.54 and 1.25 MHz) should be 70 dB below full-scale. Our test results clearly show that the DDC converter meets the B2 SINAD and SFDR specifications.

Figures 10(a) through 10(g) show the absolute values of the errors for seven different frequencies. As shown, the error performance is exceptionally good at a nominal frequency of 544 kHz; integral nonlinearity is under ± 1.0 LSB. However, at two lower frequencies of 101 and 271 kHz, the third-order harmonic distortion is noticeable as evidenced by the S-shape of the curve, although it is higher and it is within the specification. If the noise is visually disregarded (which causes broadening of the curve), the mean output error is less than approximately ± 1.5 LSB.

3.2 TEST RESULTS FOR THE ADC 12-BIT, 4-MHz A/D CONVERTER - UNIT 1

Our analysis of the test results for the ADC 12-bit, 4-MHz A/D converter (Unit 1) (at two different frequencies) is presented on the following pages, in the form of plots, as follows: noise versus input signal level under dynamic conditions (figure 11); SINAD versus input signal level (figure 12); bits lost versus input signal level (figure 13); SFDR versus input

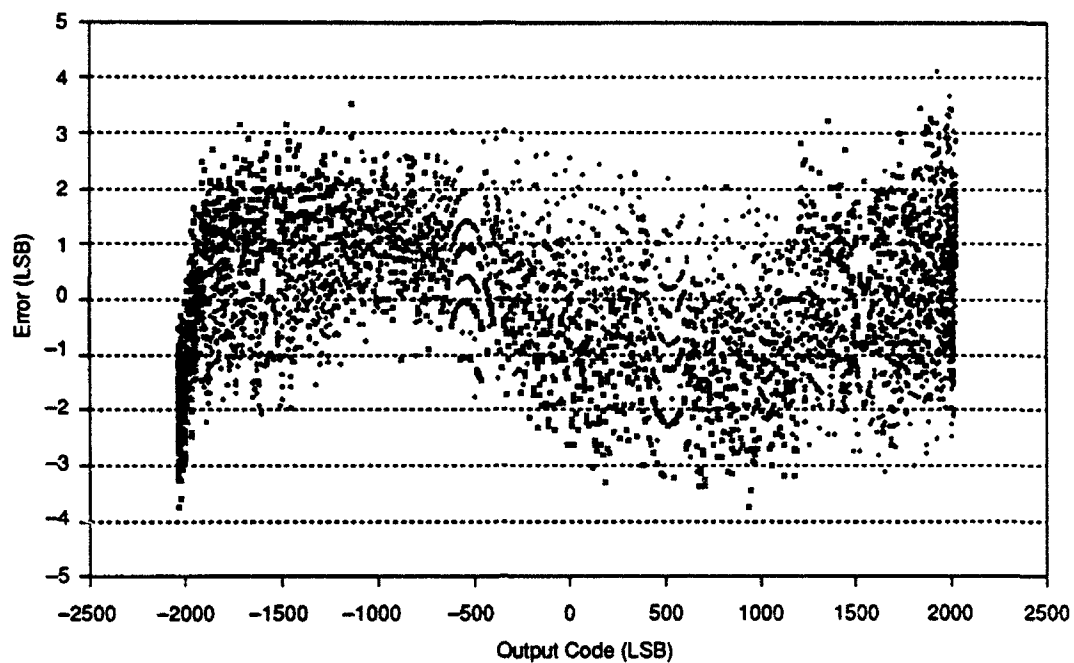


Figure 10(a). Errors of DDC A/D Converter (Input Signal Frequency = 101 kHz)

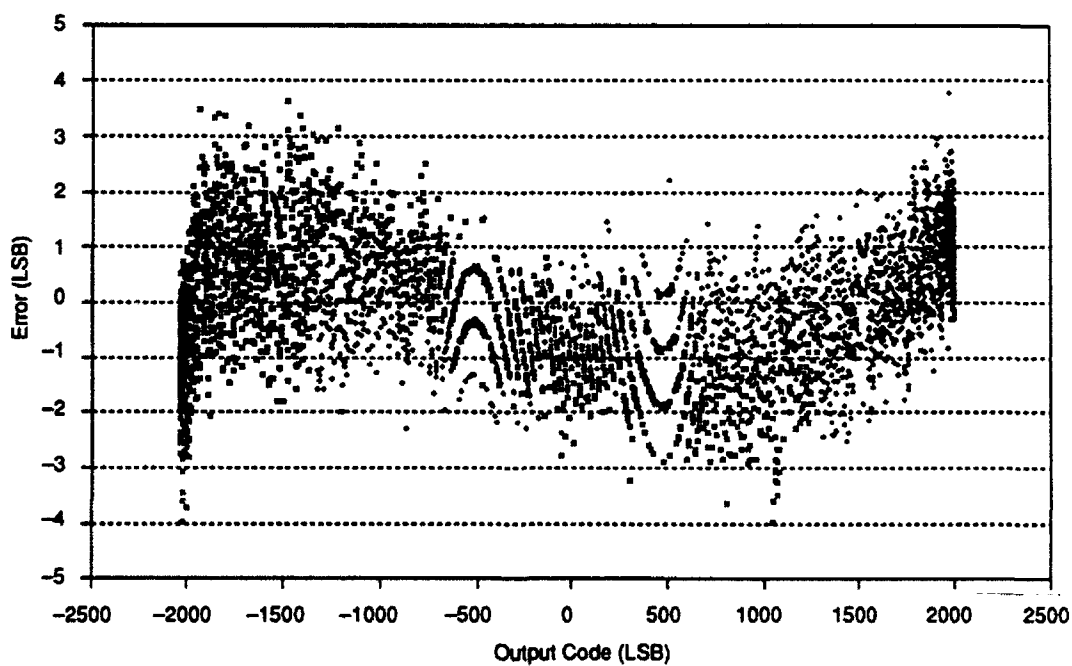


Figure 10(b). Errors of DDC A/D Converter (Input Signal Frequency = 271 kHz)

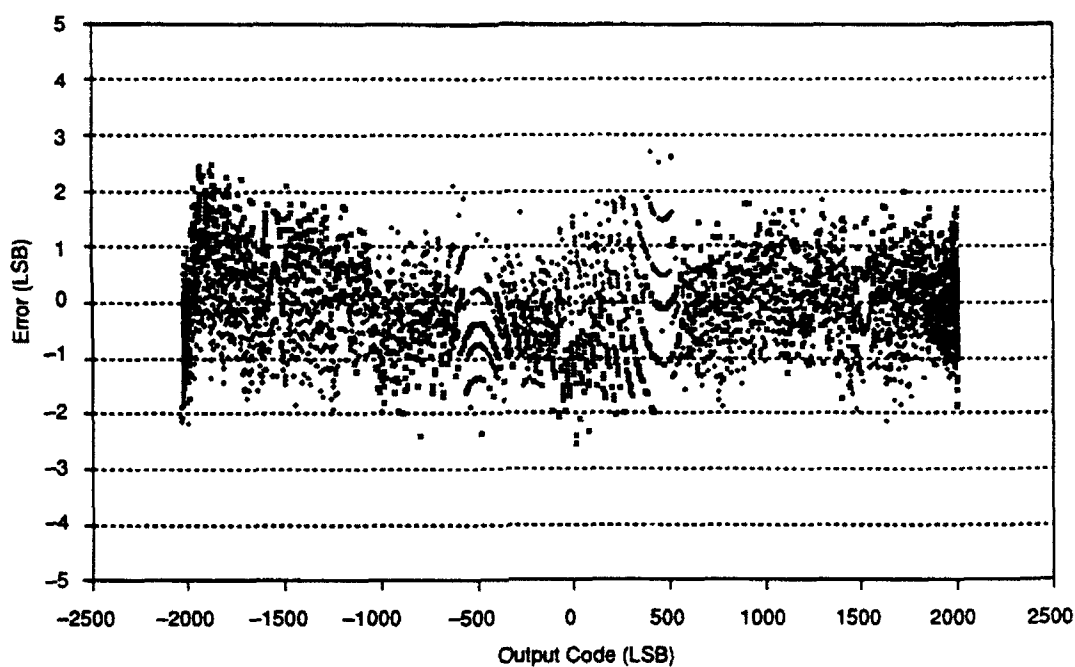


Figure 10(c). Errors of DDC A/D Converter (Input Signal Frequency = 544 kHz)

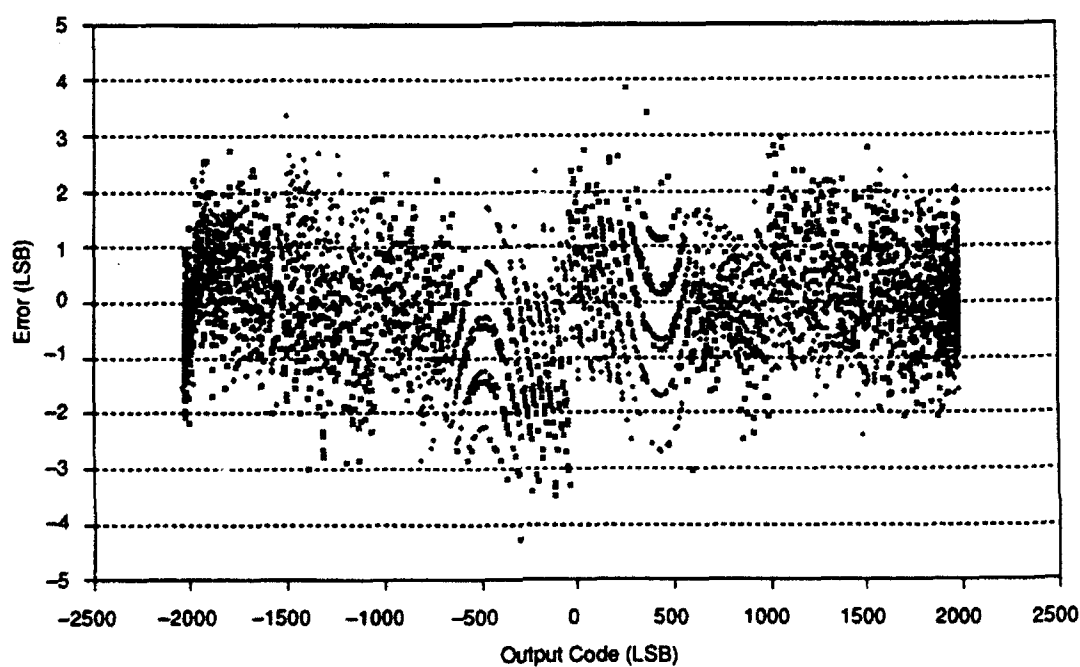


Figure 10(d). Errors of DDC A/D Converter (Input Signal Frequency = 997 kHz)

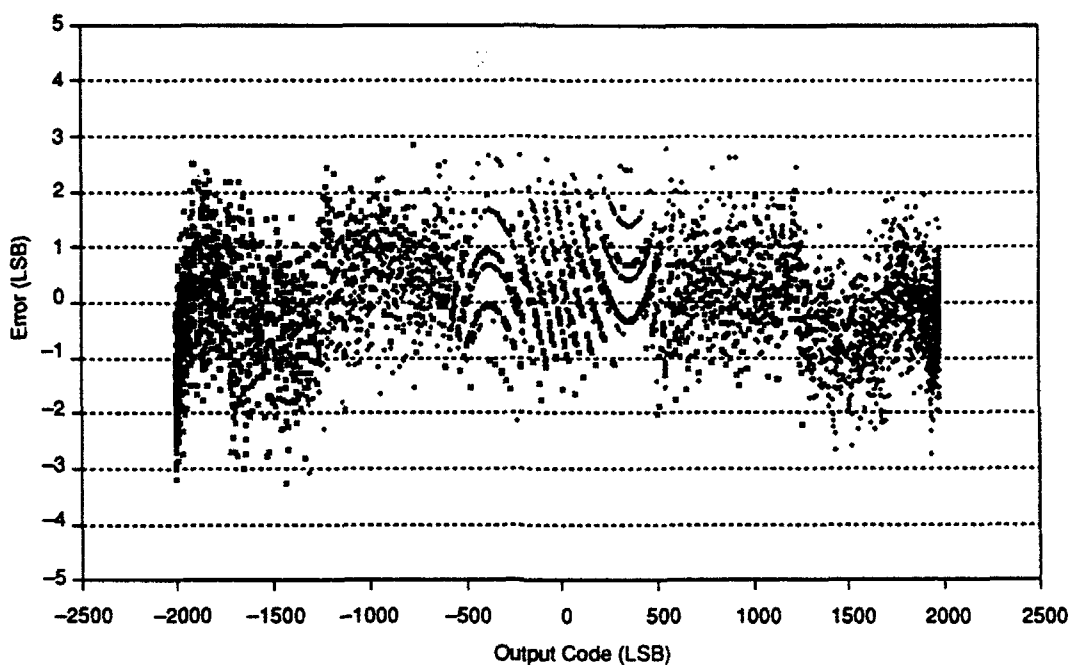


Figure 10(e). Errors of DDC A/D Converter (Input Signal Frequency = 1249 kHz)

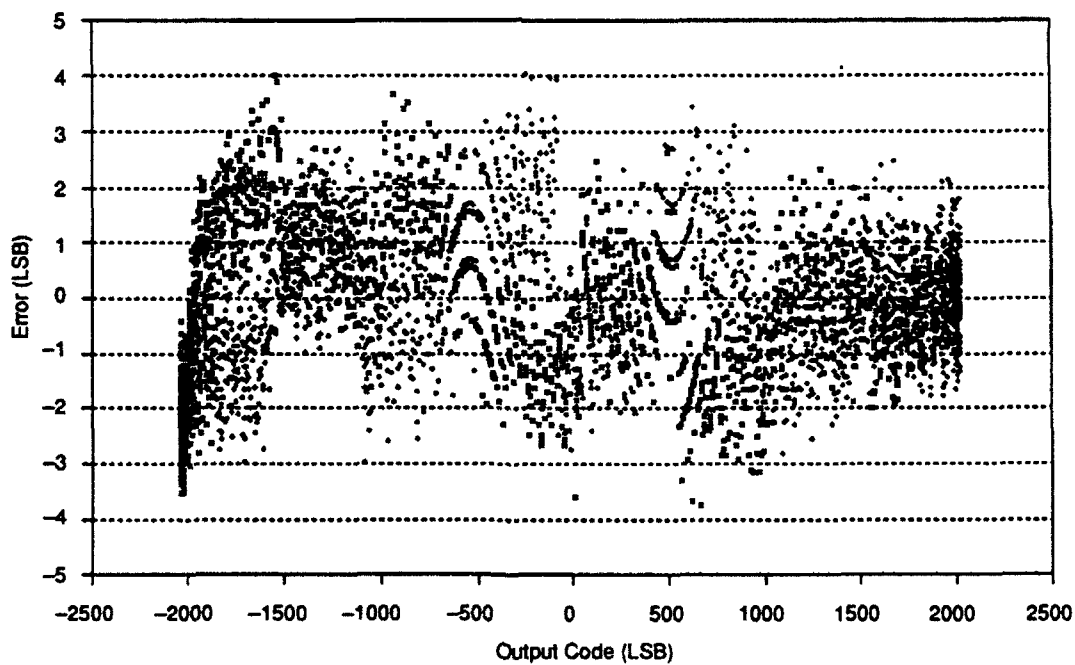


Figure 10(f). Errors of DDC A/D Converter (Input Signal Frequency = 1495 kHz)

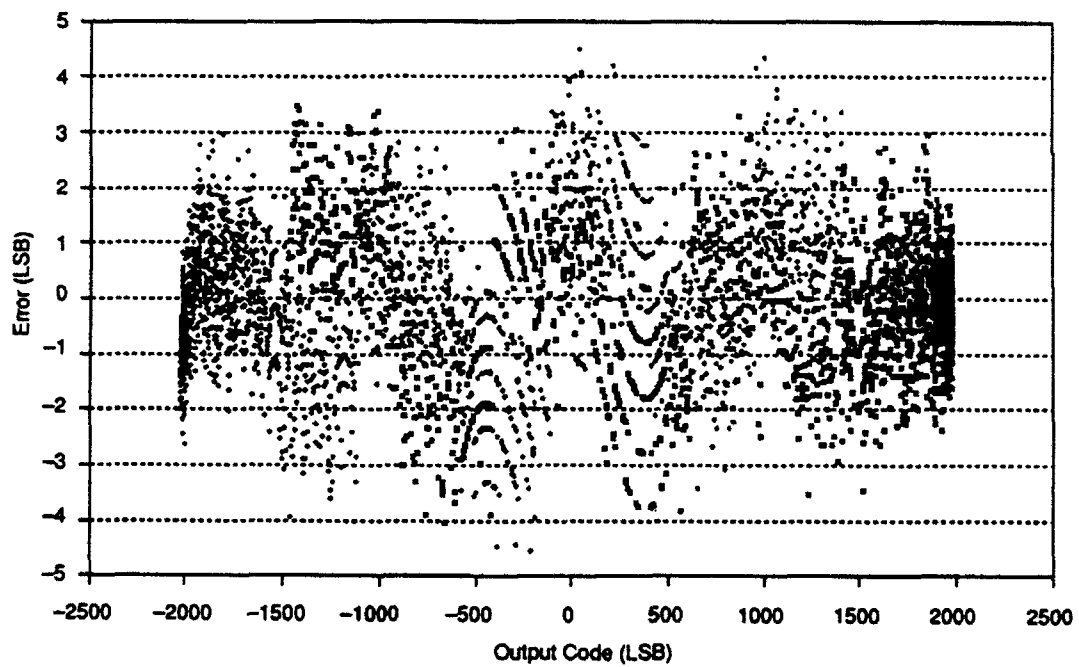


Figure 10(g). Errors of DDC A/D Converter (Input Signal Frequency = 1991 kHz)

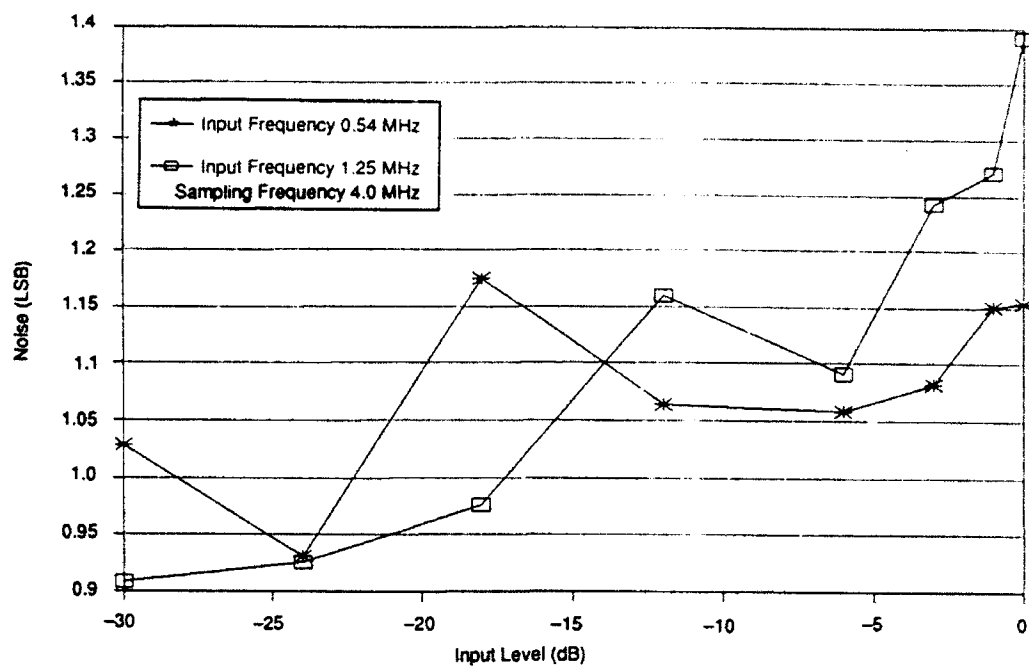


Figure 11. Noise vs. Input Signal Level for the ADC A/D Converter – Unit 1

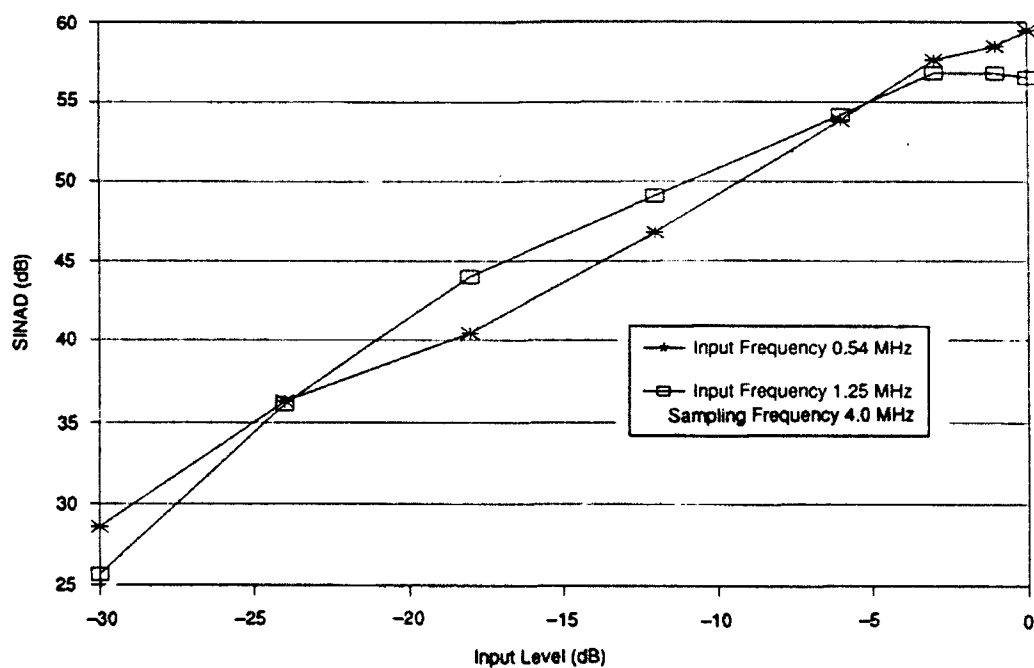


Figure 12. SINAD vs. Input Signal Level for the ADC A/D Converter – Unit 1

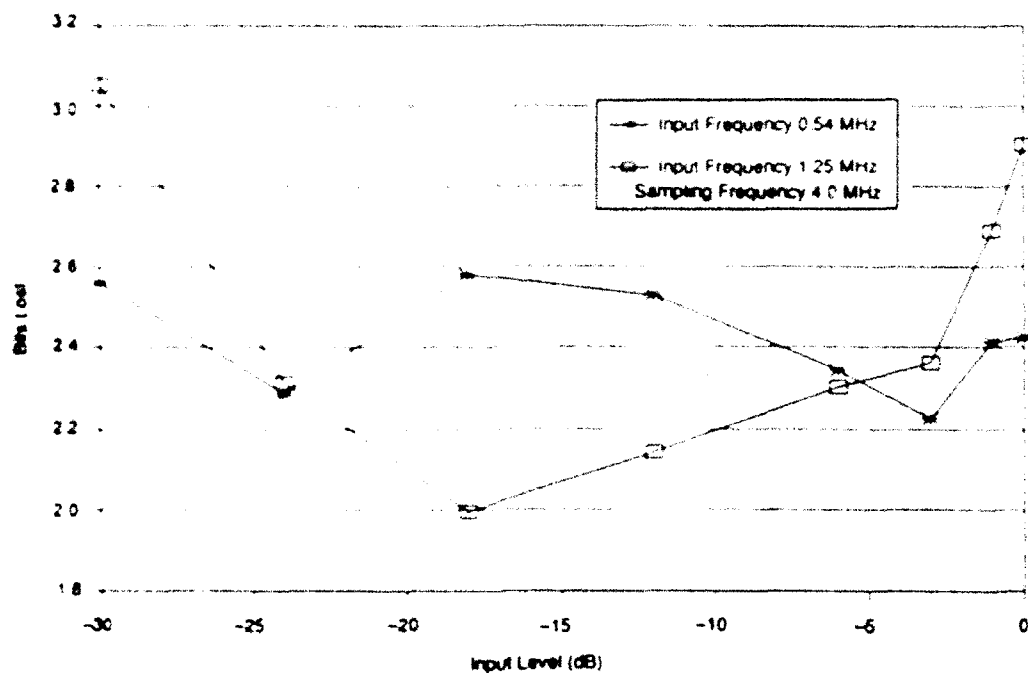


Figure 13. Bits Lost vs. Input Signal Level for the ADC A/D Converter – Unit 1

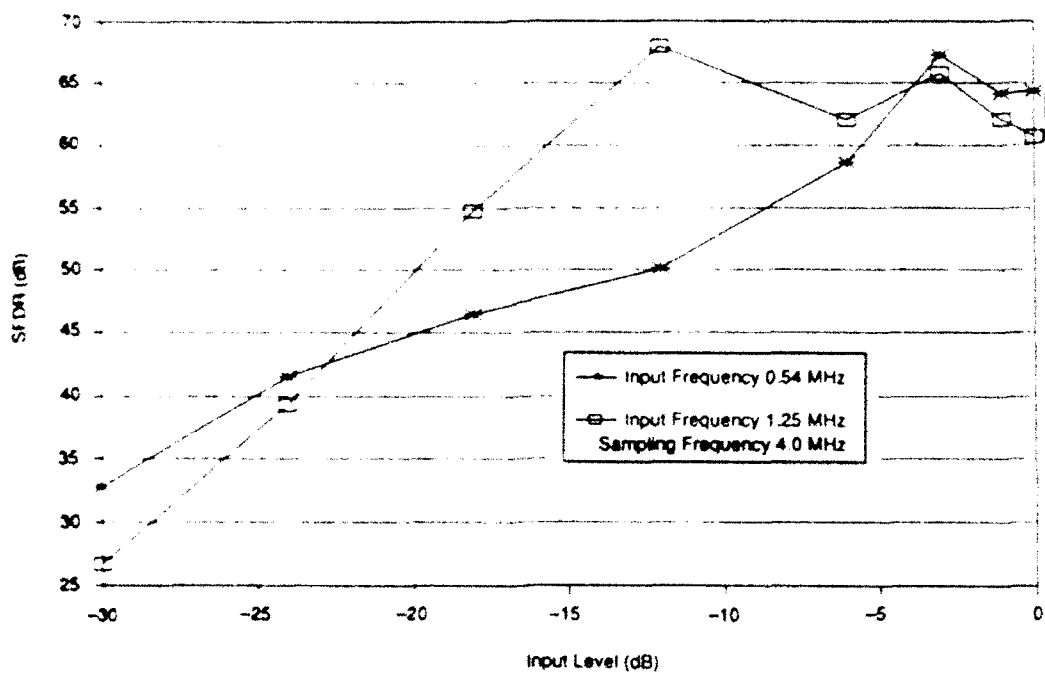


Figure 14. SFDR vs. Input Signal Level for the ADC A/D Converter – Unit 1

signal level (figure 14); and FFT spectral response for a full amplitude signal (figures 15a and 15b).

Table 7 summarizes the measured dynamic performance. The converter has 1.15 to 1.4 LSB of RMS noise for full-scale input signals. Compared to the DDC converter, it has an excess of 0.6 LSB of noise. Figure 13 shows that it loses 2.4 to 2.9 bits for full-scale input signals. However, it loses 2.6 to 3.0 bits for signals that are 30 dB below full-scale. It provides nine effective bits under dynamic conditions. The SFDR of this converter is 60 to 65 dB for large signals.

The spectrum plots (figures 15a and 15b) show an increase of 6 dB in noise floor over a wideband in the upper half of the Nyquist band. This may be caused by high-order nonlinearity which results from the second-stage error correction circuits not performing properly.

Based on the test results, the baseline ADC A/D converter is noisier than the DDC unit and does not meet the SNR and SFDR specifications. Since this unit had such poor performance at the B2 specified frequencies of 0.54 MHz and 1.25 MHz, respectively, we did not test the converter at five other frequencies. However, the baseline ADC unit did meet all the B2 requirements during qualification testing of the radar. Since it has been in operation for three years, perhaps its poor dynamic performance may be due to some component failure in the board. In order to come to a final conclusion, we obtained another ADC operational unit from Paramax and then repeated the measurements. The next section presents the details of the test results on the ADC A/D converter Unit 2.

3.3 TEST RESULTS FOR THE ADC 12-BIT, 4-MHZ A/D CONVERTER - UNIT 2

Our analysis of the test results for the ADC 12-bit, 4-MHz A/D converter (Unit 2) (at four different frequencies) is presented on the following pages, in the form of plots, as follows: noise versus input signal level under dynamic conditions (figure 16); SINAD versus input signal level (figure 17); bits lost versus input signal level (figure 18); SFDR versus input

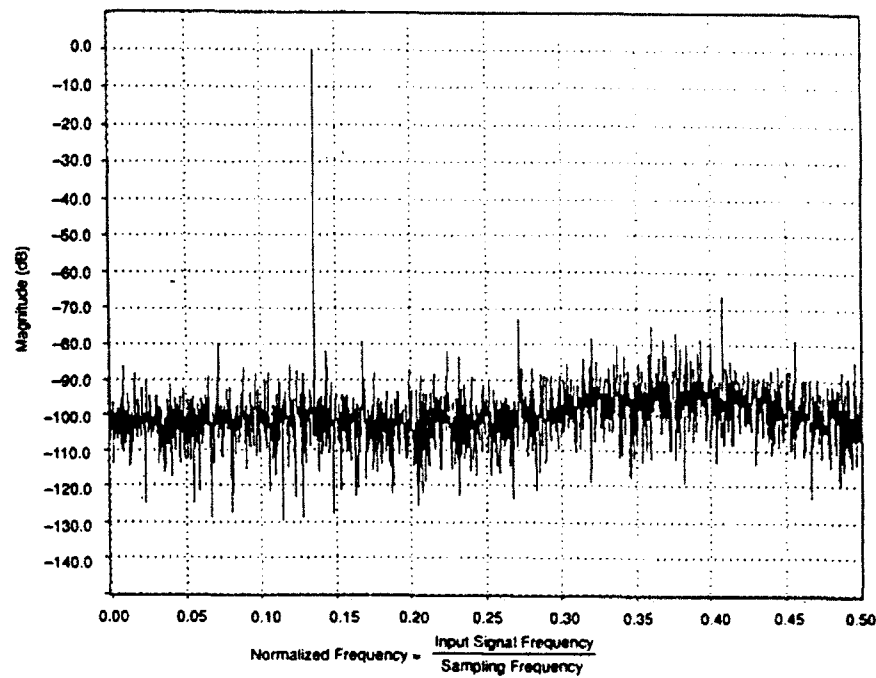


Figure 15(a). FFT Spectral Response for the ADC A/D Converter – Unit 1
(Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = Full-Scale)

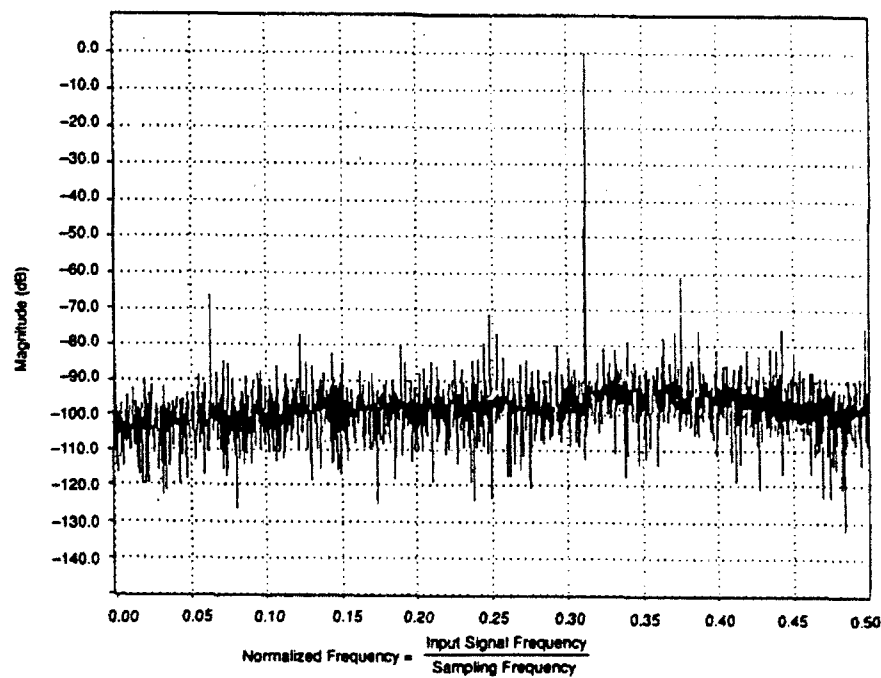


Figure 15(b). FFT Spectral Response for the ADC A/D Converter – Unit 1
(Input Signal Frequency = 1.25 MHz; Amplitude of the Signal = Full-Scale)

Table 7. Measured Dynamic Performance of 12-Bit, 4-MHz ADC A/D Converter - Unit 1

Signal Frequency (MHz)	Amplitude (dB)	SNR		Effective Bits	SFDR (dB)
		With Harmonics (dB)	Without Harmonics (dB)		
0.54	0	59.4	61.7	9.6	64.4
0.54	-1	58.5	60.3	9.6	64.2
0.54	-3	57.6	58.9	9.8	67.2
0.54	-6	59.9	56.1	9.7	58.6
0.54	-12	46.8	50.0	9.5	50.1
0.54	-18	40.5	43.2	9.4	46.5
0.54	-24	36.2	39.1	9.7	41.5
0.54	-30	28.6	32.3	9.4	32.8
1.25	0	56.5	60.1	9.1	60.7
1.25	-1	56.8	59.8	9.3	62.0
1.25	-3	56.8	58.1	9.6	65.8
1.25	-6	54.2	56.2	9.7	62.0
1.25	-12	49.1	49.7	9.9	67.9
1.25	-18	44.0	45.2	10.0	54.8
1.25	-24	36.1	39.6	9.7	39.3
1.25	-30	25.6	33.9	9.0	26.7

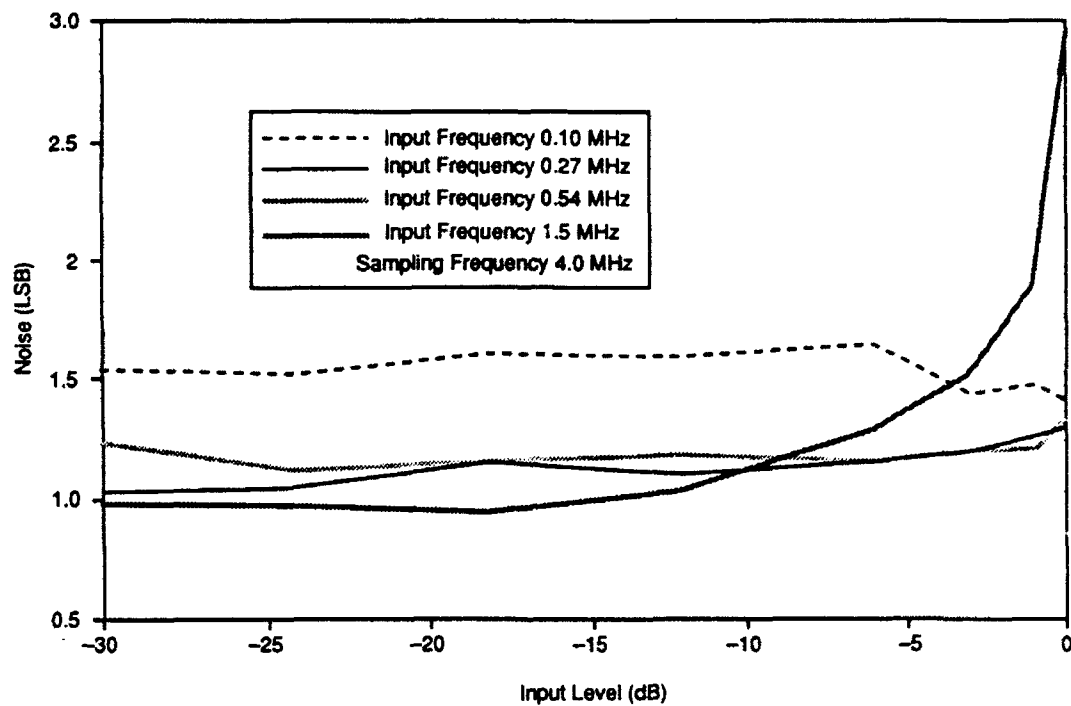


Figure 16. Noise vs. Input Signal Level for the ADC A/D Converter – Unit 2

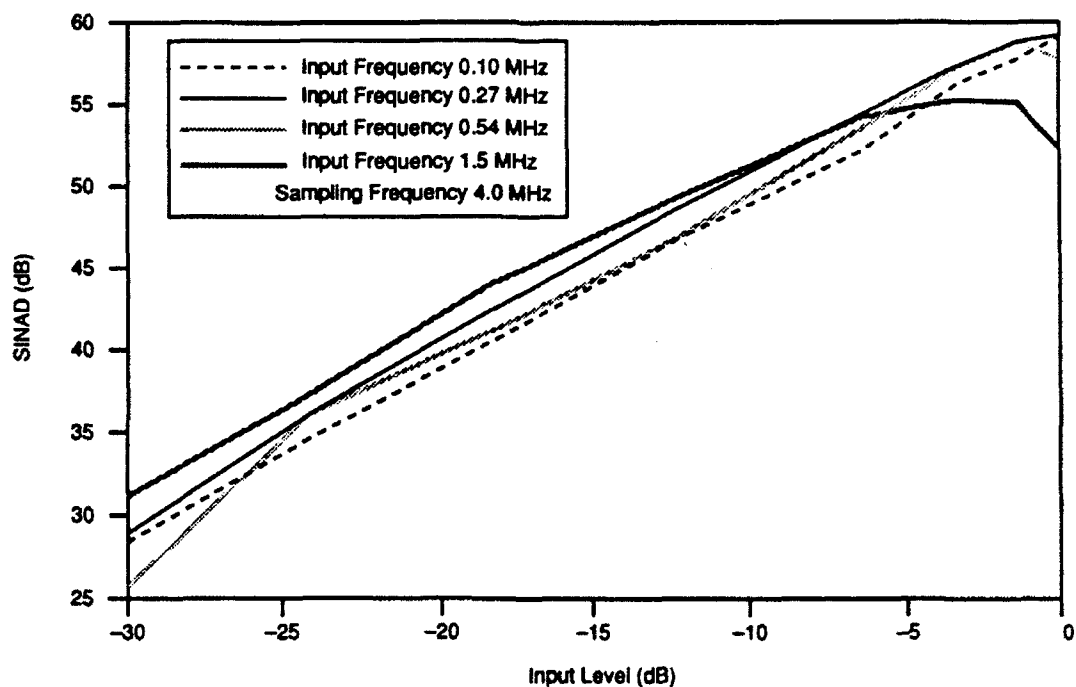


Figure 17. SINAD vs. Input Signal Level for the ADC A/D Converter – Unit 2

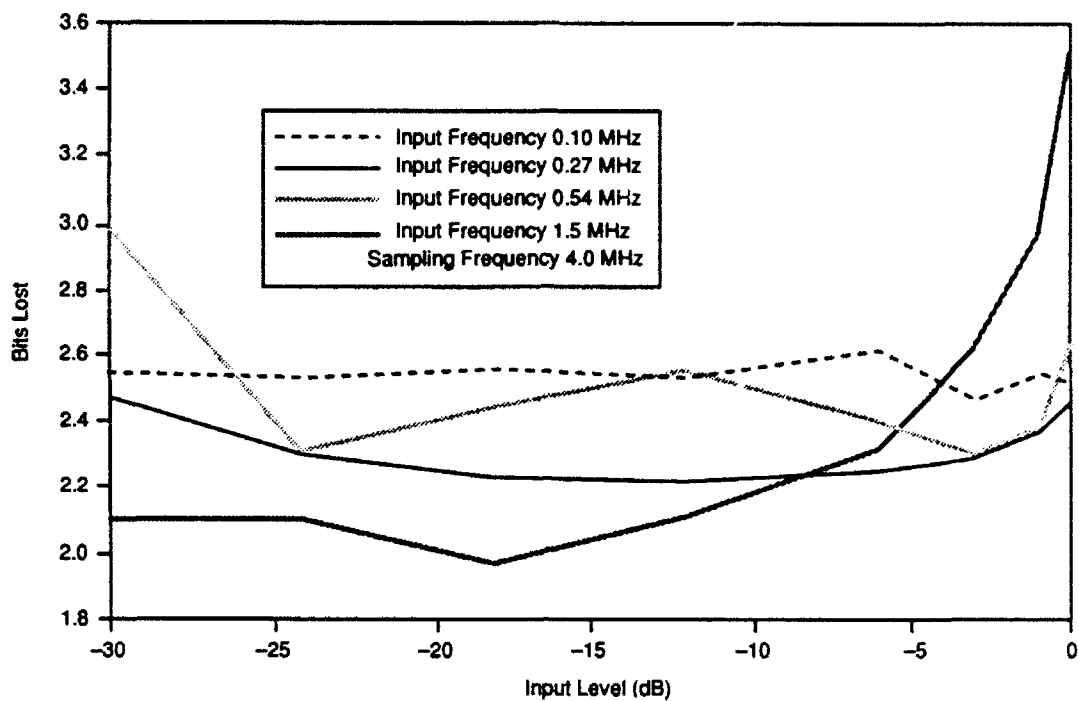


Figure 18. Bits Lost vs. Input Signal Level for the ADC A/D Converter – Unit 2

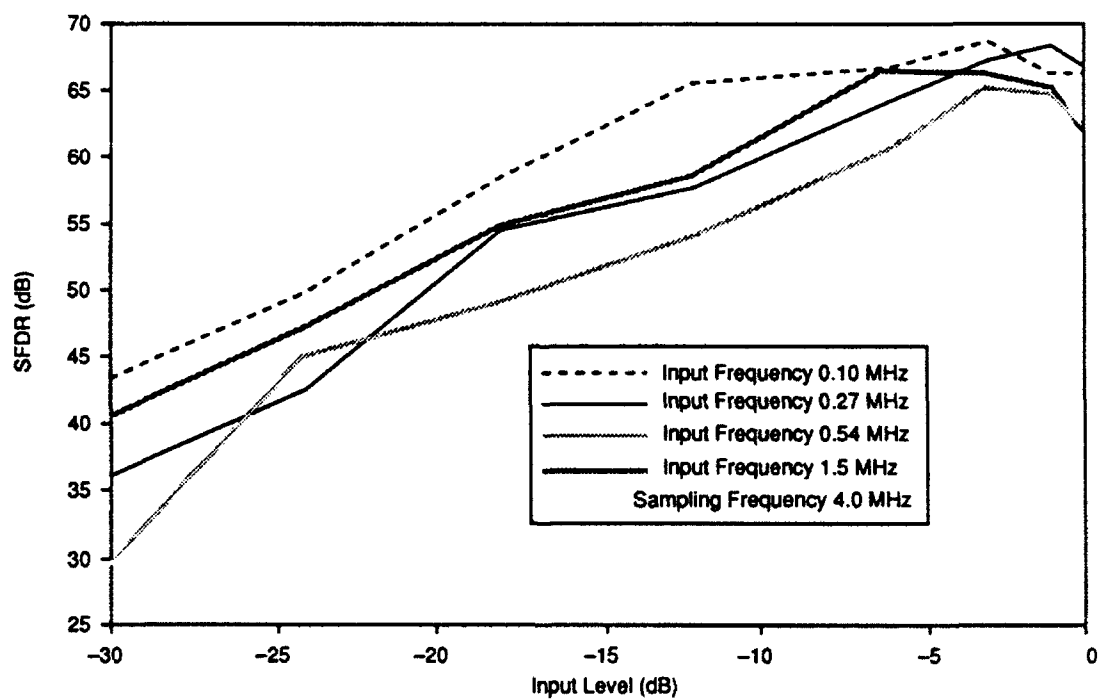


Figure 19. SFDR vs. Input Signal Level for the ADC A/D Converter – Unit 2

signal level (figure 19); and FFT spectral response for a full amplitude signal that is 30.0 dB below full-scale at each frequency (figures 20(a) through 20(h)).

Table 8 summarizes the measured dynamic performance. In general the converter has 1.1 LSB of RMS noise at most of the frequencies and for different signal amplitudes at each frequency. However, at a signal frequency of 0.1 MHz, the noise rises appreciably to 3.0 LSB, which may be associated with the missing code problem that it experiences under these conditions. It loses between 2.2 and 2.5 bits at all frequencies and different signal amplitudes at each level. However, for a full-scale amplitude signal with a frequency of 1.5 MHz, it loses 3.5 bits, which may be again due to the missing code problem. It provides 8.5 to 9.8 effective bits under dynamic conditions. The SFDR is 62 to 66 dB for large signals.

The spectrum plots show an increase of 6 dB in noise floor over a wideband in the upper half of the Nyquist band. This may be caused by high-order nonlinearity which results from the second-stage error correction circuits not performing properly.

Figures 21(a) and 21(b) show the absolute values of the errors of the converter for two different frequencies. Figure 21(a) shows the converter has 3.0 LSB peak-to-peak of second harmonic distortion. The error curve is not symmetrical; it is different for negative-going voltages (zero angles of zero to π) and for positive-going voltages (angles π to 2π). At angles corresponding to the first sample after a positive peak there are large errors up to 20 LSB. On the second conversion after the positive peak, the errors are moderately large (approximately 4.0 LSB). From the scatter of the curve it can be concluded that the RMS noise is slightly greater than 1.0 LSB. Due to the missing codes and large errors, it has errors greater than 5.0 LSB and does not meet the integral nonlinearity specification.

Based on the test results, even Unit 2 is noisier than the DDC unit and does not meet the SNR, SFDR, and integral linearity B2 specifications.

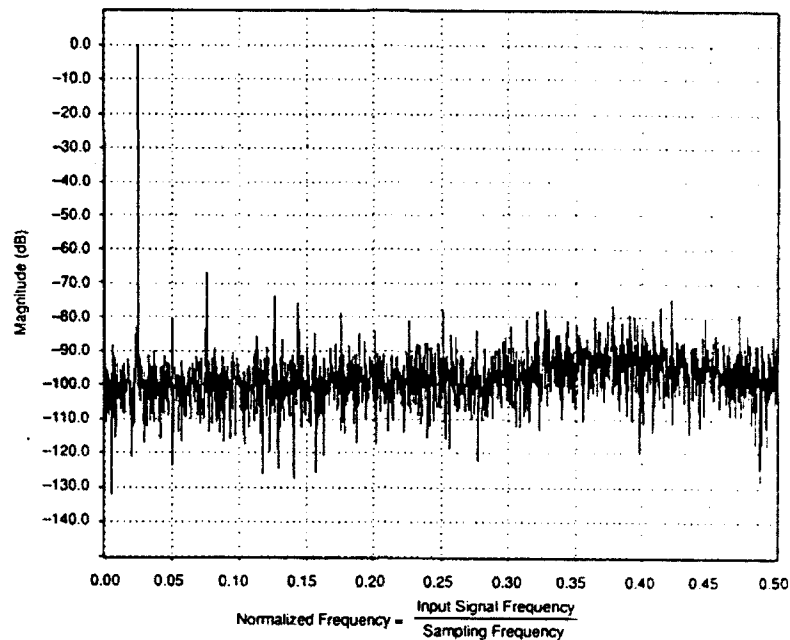


Figure 20(a). FFT Spectral Response for the ADC A/D Converter – Unit 2
(Input Signal Frequency = 0.10 MHz; Amplitude of the Signal = Full-Scale)

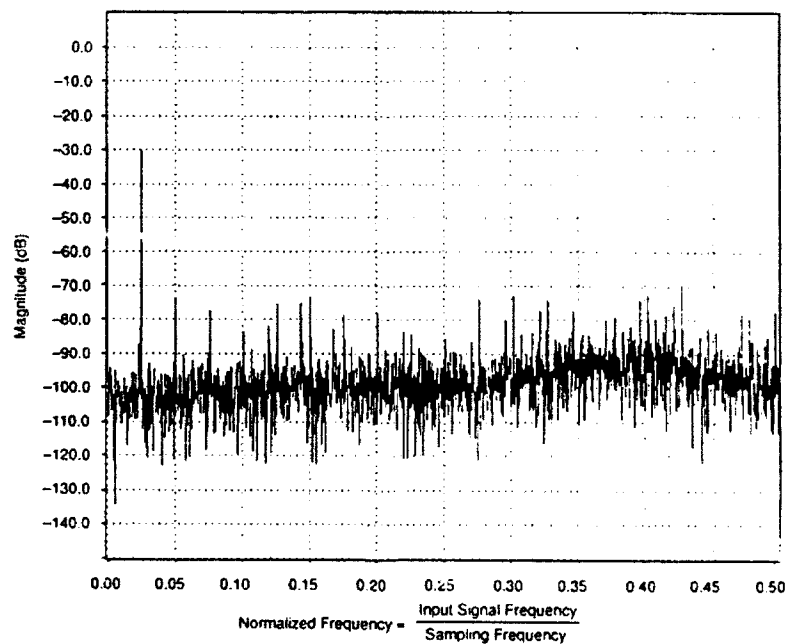


Figure 20(b). FFT Spectral Response for the ADC A/D Converter – Unit 2
(Input Signal Frequency = 0.10 MHz; Amplitude of the Signal = -30 dB)

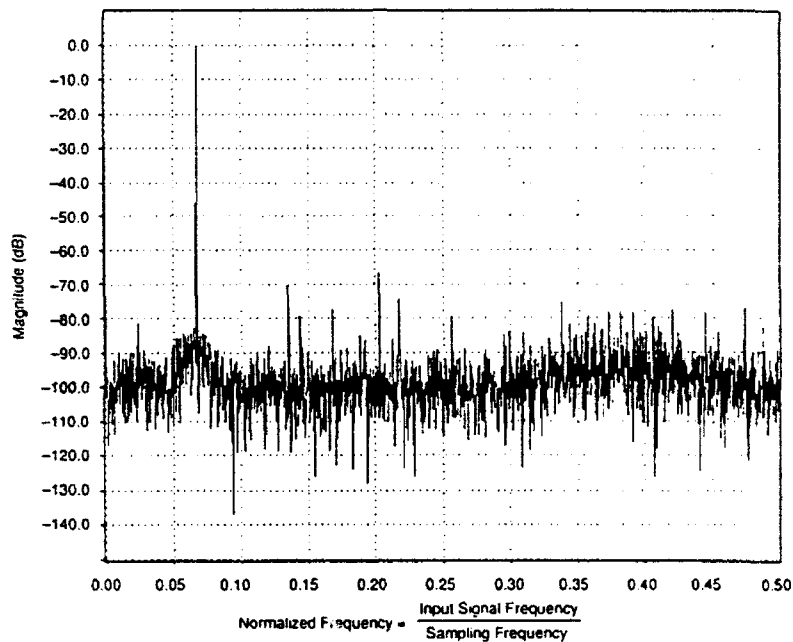


**Figure 20(c). FFT Spectral Response for the ADC A/D Converter – Unit 2
(Input Signal Frequency = 0.27 MHz; Amplitude of the Signal = Full-Scale)**

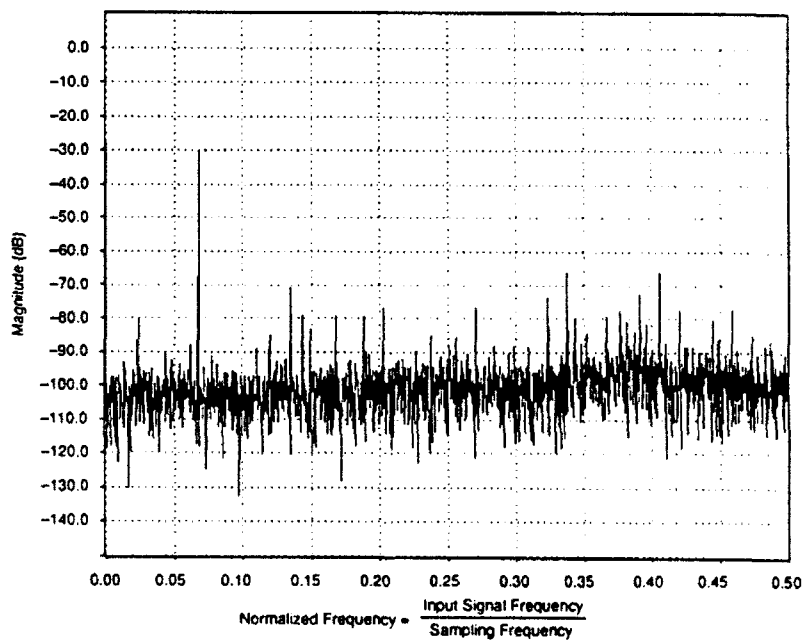


**Figure 20(d). FFT Spectral Response for the ADC A/D Converter – Unit 2
(Input Signal Frequency = 0.27 MHz; Amplitude of the Signal = -30 dB)**

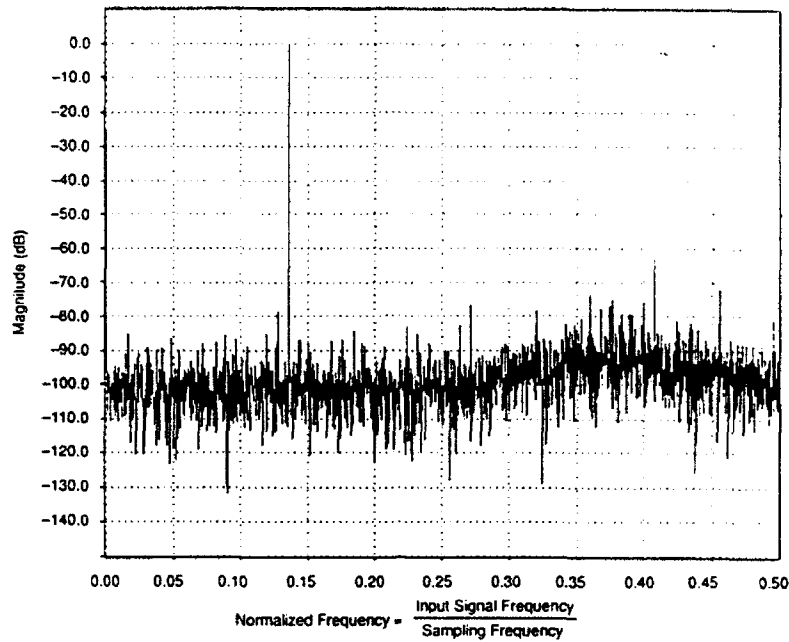


Figure 20(e). FFT Spectral Response for the ADC A/D Converter – Unit 2
(Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = Full-Scale)

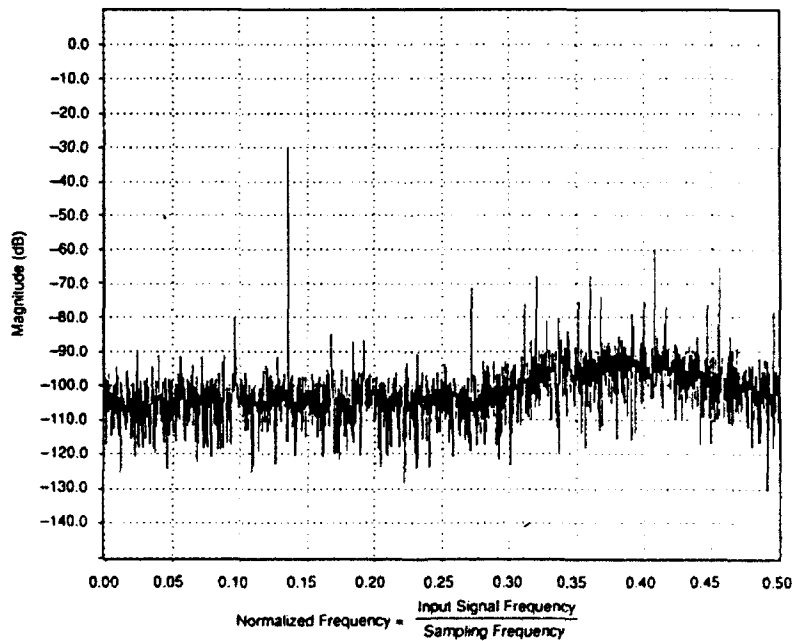


Figure 20(f). FFT Spectral Response for the ADC A/D Converter – Unit 2
(Input Signal Frequency = 0.54 MHz; Amplitude of the Signal = -30 dB)

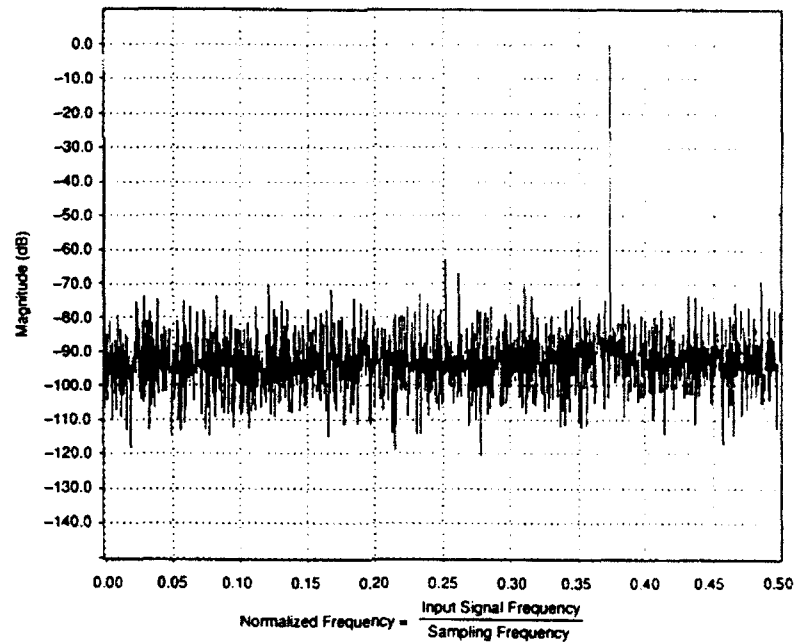


Figure 20(g). FFT Spectral Response for the ADC A/D Converter – Unit 2
(Input Signal Frequency = 1.5 MHz; Amplitude of the Signal = Full-Scale)

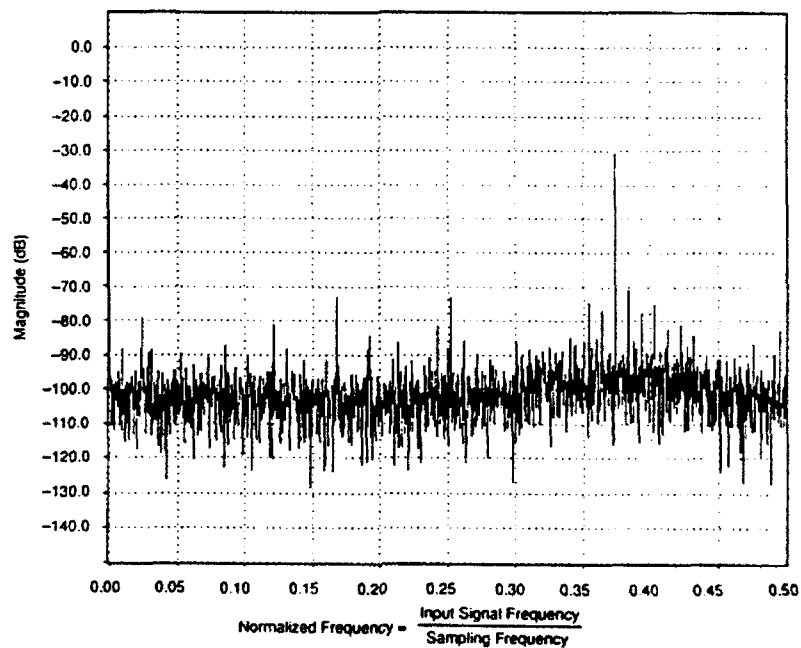


Figure 20(h). FFT Spectral Response for the ADC A/D Converter – Unit 2
(Input Signal Frequency = 1.5 MHz; Amplitude of the Signal = -30 dB)

Table 8. Measured Dynamic Performance of 12-Bit, 4-MHz ADC A/D Converter - Unit 2

Signal Frequency (MHz)	Amplitude (dB)	<u>SNR</u>		Effective Bits	SFDR (dB)
		With Harmonics (dB)	Without Harmonics (dB)		
0.10	0.0	58.8	60.0	9.5	66.5
0.10	-1.0	57.7	58.6	9.5	66.5
0.10	-3.0	56.1	56.8	9.5	68.6
0.10	-6.0	52.2	52.7	9.4	66.6
0.10	-12.0	46.8	47.0	9.5	65.5
0.10	-18.0	40.6	40.9	9.4	58.3
0.10	-24.0	34.8	35.3	9.5	49.6
0.10	-30.0	28.7	29.3	9.5	43.1
0.27	0.0	59.2	60.8	9.5	66.7
0.27	-1.0	58.8	60.2	9.6	68.3
0.27	-3.0	57.2	58.6	9.7	67.2
0.27	-6.0	54.4	55.9	9.7	64.1
0.27	-12.0	48.7	50.3	9.8	57.8
0.27	-18.0	42.6	44.0	9.8	54.7
0.27	-24.0	36.2	38.8	9.7	42.6
0.27	-30.0	29.2	32.9	9.5	36.0
0.54	0.0	58.1	60.6	9.4	62.5
0.54	-1.0	58.6	60.3	9.6	64.8
0.54	-3.0	57.2	58.4	9.7	65.1
0.54	-6.0	53.5	55.8	9.6	60.6
0.54	-12.0	46.7	49.5	9.5	54.2
0.54	-18.0	41.3	43.7	9.6	49.0
0.54	-24.0	36.1	37.8	9.7	44.7
1.50	0.0	52.8	53.6	8.5	62.1
1.50	-1.0	55.2	56.4	9.0	65.3
1.50	-3.0	55.2	56.4	9.4	66.3
1.50	-6.0	54.1	54.9	9.7	66.8
1.50	-12.0	49.3	50.7	9.9	58.5
1.50	-18.0	44.1	45.4	10.0	54.8
1.50	-24.0	37.4	39.0	9.9	47.0
1.50	-30.0	31.4	32.7	9.9	40.6

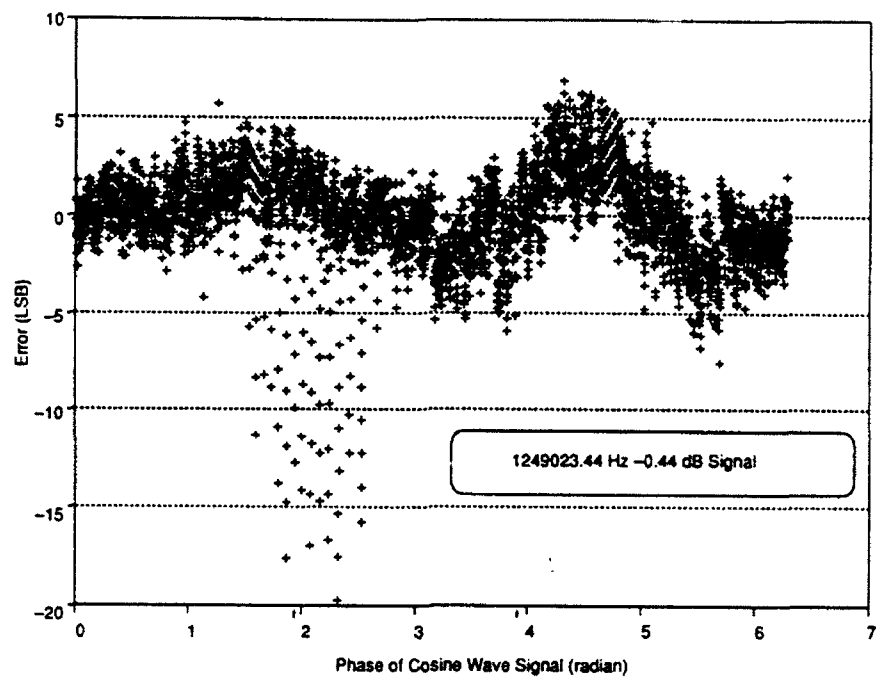


Figure 21(a). Error vs. Signal Phase for the ADC A/D Converter – Unit 2

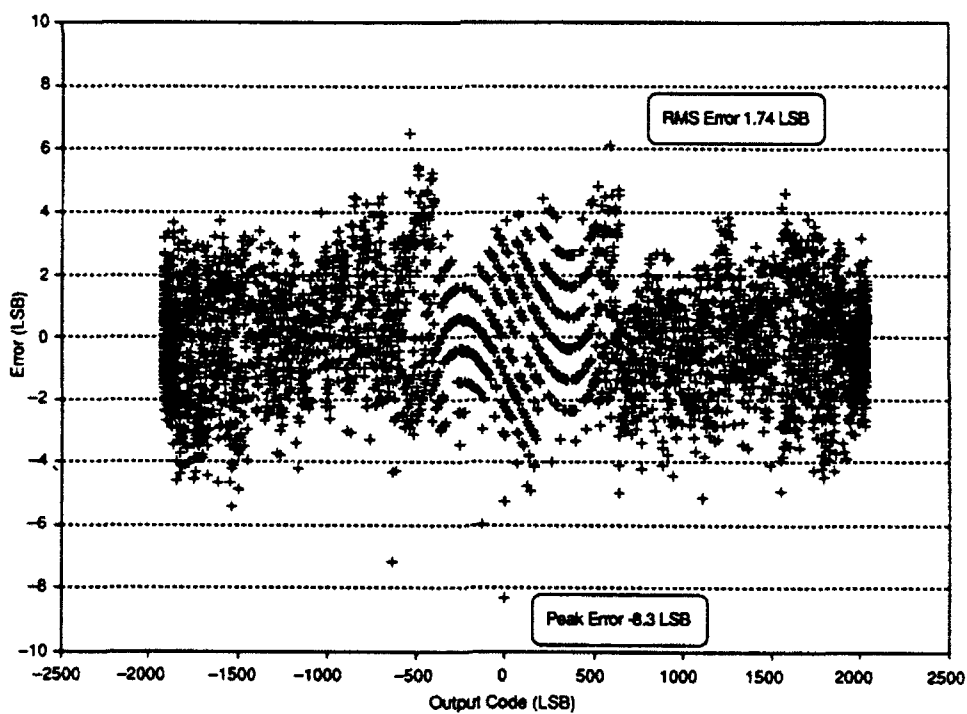


Figure 21(b). Errors of ADC A/D Converter – Unit 2 at 544 kHz

3.4 SUMMARY AND CONCLUSIONS OF SINE-WAVE TESTS

After comparing the dynamic performance of the ADC and DDC converters, we found that the new DDC converter met the integral linearity, SINAD, and SFDR B2 specifications and exceeded the performance of the two three-year-old ADC units.

SECTION 4

MONOTONICITY ANALYSIS AND TEST RESULTS

In section 3, we validated the B2 requirements for the RMS-signal-to-RMS-noise ratio, SFDR, and integral linearity requirements. In this section we validate the monotonicity requirements of both converters. Based on the spectral analysis test results, we concluded that the two ADC converters were defective and not functioning properly. However, for completeness, we present the monotonicity test results for the ADC Unit 2 only.

4.1 TEST DESCRIPTION

The test is a variant of the standard sine-wave test. The test signal is a spectrally pure and low-noise filtered full-scale sine wave at a frequency of 1250061.03 Hz [1]. For the DDC converter, the signal amplitude is 2171 LSB (for this converter, the LSB corresponds to 1 mv), sufficient to drive the A/D converter slightly into saturation. The B2 specification requires measurements of all codes. This amplitude is the smallest that we could generate conveniently which exercises all codes. For the ADC converter, the signal is reduced slightly (to 1990 LSB) to avoid saturation because the spectral analysis test indicated a possible problem near saturation, as discussed in section 3.

The sine wave is applied to the A/D converter under test and the resulting digital 65536 (64 K) consecutive data points are stored as a file on a floppy disk. This is repeated as fast as possible, with a typical interval of about two minutes per record. For each converter, a total of eight data records, representing 512 K measurements, are made. Final data analysis is done using a combination of custom and commercial software running on the mainframe VAX and PCs.

4.2 DATA ANALYSIS

The first step in the data analysis is calculating the input cosine wave from the output data using a FORTRAN program, based upon a sine-wave curve-fitting algorithm described in section 2 [11]. Because the converter is driven into saturation, the program is modified to eliminate the saturated samples prior to fitting the cosine wave to the rest of the data (the FORTRAN source code is listed in appendix B). Each data record of 64 K sample points represents 16384 microseconds of signal. During this interval the signal will have approximately 20481 cycles (actually 20480.99991552 cycles). Since we have an integral number of cycles in the data record, a perfect clipped cosine wave is fitted to the data with a negligible error. For each unsaturated data point, the input voltage, its phase angle, and the error (which is the difference between the estimated input and measured output) are calculated. The data is then separated into two groups, based upon the phase angle of the input. One group consists of measurements of increasing voltage, while the other contains those of decreasing voltage.

Figure 10 shows the actual errors of the DDC converter. For most measurements, the mean error is less than ± 0.5 LSB, and the variation from the mean is also less than ± 0.5 LSB. Many subranging A/D converters behave differently with increasing or decreasing (i.e., positive-going or negative-going) signals; the software separates them into distinct groups which can be analyzed independently, or combined if desired. The two groups are then individually reordered in order of increasing input voltage. The input voltages and output codes of each group are saved as disk files. A second FORTRAN program reads the eight pairs of disk files, combines them, resorts them in order of increasing input voltage, and then writes them to another pair of data files. One of these files contains the input voltages and output codes of all 256 K measurements made with increasing voltage; the other one contains those made with decreasing voltage.

Different records with randomly-determined start times, several minutes apart, will not be phase-coherent. The measured sample points will not repeat exactly between records. Therefore, the combined eight records with 512 K measurements are almost uniformly distributed in phase angle.

The uniform distribution of the measurements, with respect to signal phase angle, causes the distribution of voltage measurements to vary inversely with the sine of the phase angle. The minimum number of measurements per code occurs at the mid-scale of the A/D converter. At signal-zero crossing, there will be approximately 38 measurements² per code made with increasing voltages, and a similar number for decreasing voltages; and there will be more than 100 measurements per code near the saturation points of the converter.

For the case of a noise-free A/D converter, the code edges could be determined to a resolution of 0.03 (i.e., 1/38) LSB by using 512 K data points, but the resolution and accuracy is lower for a real A/D converter with internal noise. To minimize the probability of drawing erroneous conclusions from the noisy data, we employ three different methods to evaluate the code widths: the histogram, the code-mean, and the code-edge methods.

4.3 DDC A/D CONVERTER ANALYSIS

4.3.1 Histogram Method

The histogram is the best possible test method for detecting missing or wide codes, but it does not indicate monotonicity. If the converter is known to be monotonic a priori, then the histogram can be used as an indicator of the uniformity of the code widths. With this method, the derivation of the code widths is based on the number of occurrences of the codes.

A histogram of the number of occurrences of each possible digital output code is created. The histogram is then normalized by multiplying by the absolute value of the sine of the signal phase angle to compensate for the larger number of observations expected near the

² Depends on the number of data samples and the amplitude of the signal. For example, with 512 K samples and the amplitude of the signal equal to 2171.0 LSB,

$$\text{the number of measurements per code} = \left(\frac{512 \times 1024}{2171 \times 2\pi} \right) = 38$$

saturation points. After the normalization, the expected value of the number of occurrences of a code is proportional to the effective width of that code. The normalized histograms of the DDC A/D converter are shown in figures 22(a), 22(b), and 22(c), for decreasing input voltage, increasing input voltage, and combined voltages, respectively. Horizontal dashed lines at the B2 specification limits of 0.10 and 1.90 times the nominal code width are also shown, which correspond to a minimum of four hits and a maximum of 72 hits per code in our histogram analysis.

The histogram shows that there are no missing codes. For negative signal slope, there are no narrow codes, and only three codes are slightly wider than the specification limit. However, for increasing voltages, there is one narrow code and seven wide codes. Generally, most of the codes which are extremely wide or narrow, with signals slewing in one direction, behave more nominally with slopes in the opposite direction. If the two slope polarities are combined, all code widths are in the range of 0.2 to 2.0 LSB, and only one code is slightly wider than the specification.

4.3.1.1 Sensitivity Analysis

The accuracy of the histogram method of analysis is dependent on the number of samples and the noise of the converter, as shown in appendix C. Measurements made on the DDC converter for the spectral analysis test indicate that it has approximately 0.5 LSB of RMS noise.

The number of occurrences of each code is affected by the internal noise of the converter. In appendix C, each number of occurrences is modeled as a random variable with a mean value equal to the product of the code width (expressed in mVolts or LSB) times the density of the sampling (expressed in samples per mVolt). For codes which are narrow compared to the RMS noise level of the converter, the number of occurrences approaches a Poisson distribution, with a variance equal to the mean. However, for codes which are wide compared to the RMS noise of the converter, the variance in the number of occurrences approaches a constant, which is 1.13 times the product of the RMS noise (expressed in mVolts or LSB) times the density of sampling, as shown in figure C-3.

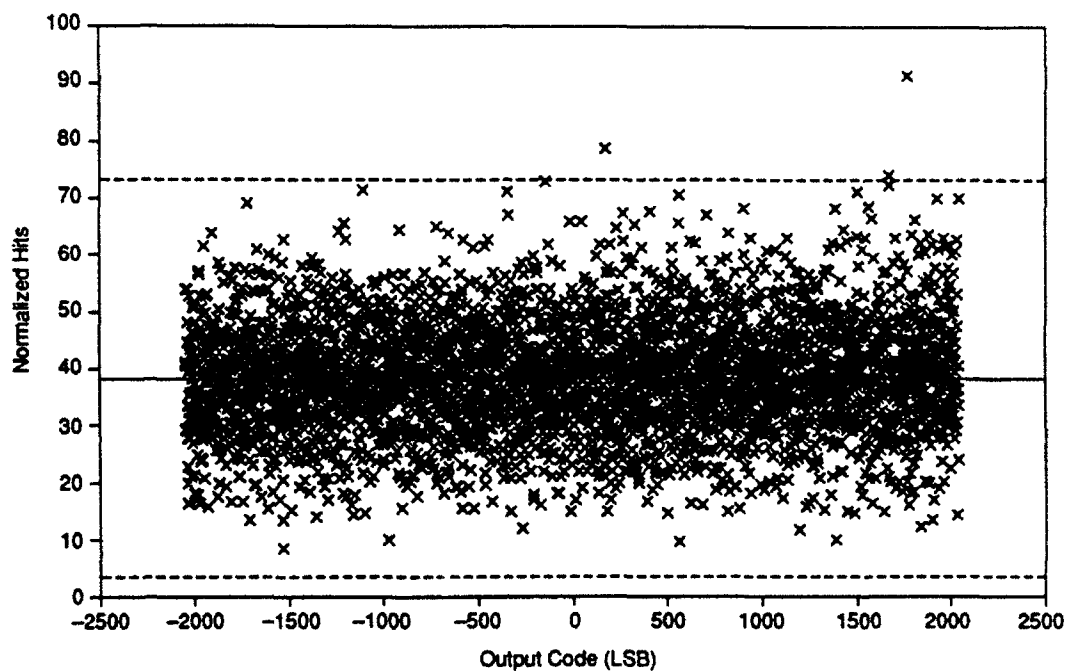


Figure 22(a). Normalized Histogram for the DDC A/D Converter (Decreasing Voltage)

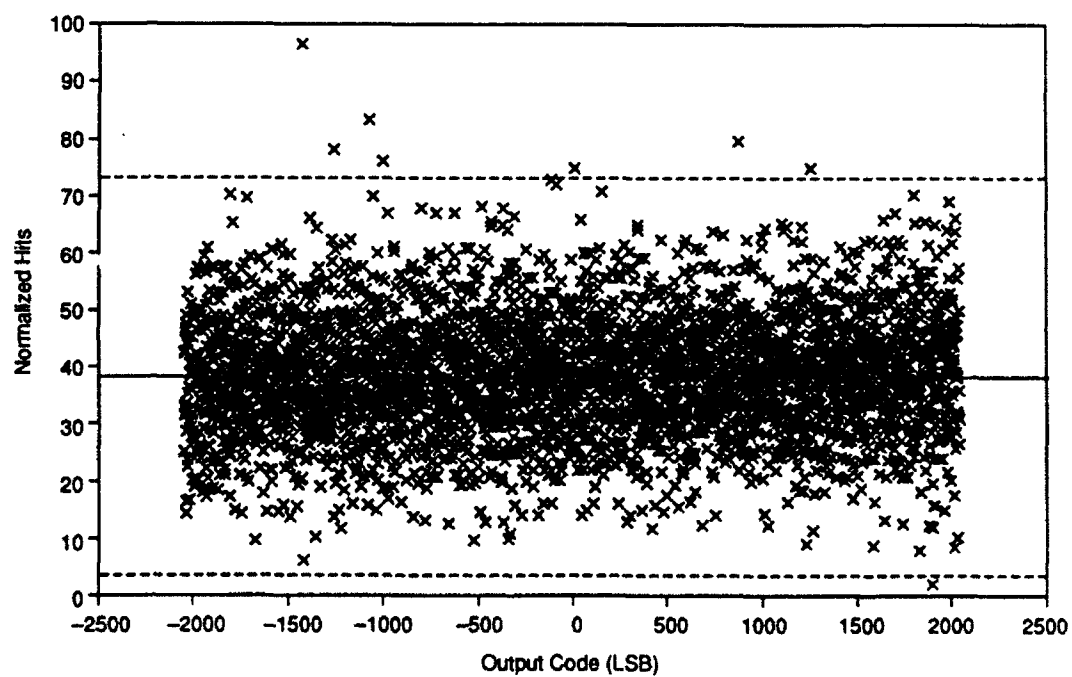


Figure 22(b). Normalized Histogram for the DDC A/D Converter (Increasing Voltage)

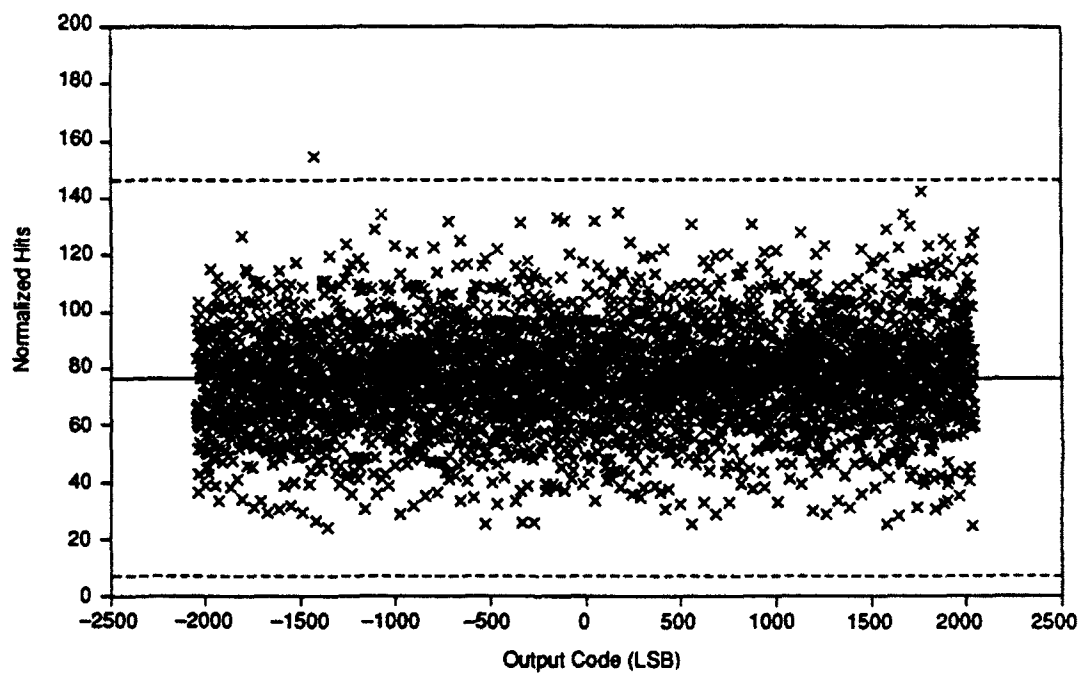


Figure 22(c). Normalized Histogram for the DDC A/D Converter (Combined Slopes)

For the DDC converter the histogram for combined slopes (see figure 22c) shows that the sampling density is 76 occurrences per LSB, and that many of the narrow codes have about 25 occurrences corresponding to $25/76=0.33$ LSB, which is less than the 0.5 LSB noise level of the converter. From figure C-3, we see that the variance of the number of occurrences of narrow codes is 21 (83 percent of the mean). The standard deviation of the narrow codes is 4.6 observations (or $4.6/76=0.06$ LSB); hence, the measurement errors would be ± 0.12 LSB.

Most of the wide codes for the DDC converter have about 133 observations, corresponding to a width for wide codes of $133/76 = 1.75$ LSB. Since this is 3.5 times the (0.5 LSB) RMS noise of the converter, we assume a normal distribution with a variance (see figure B-3) of $43 = (0.32 * 133)$. The standard deviation of the wide codes is 6.6 observations (or $6.6/76=0.09$ LSB). Hence, we can conclude from this analysis that the largest observation of 2.0 LSB observed in the DDC code analysis could have been caused by random variation. Based on the 512 K samples used in the histogram sensitivity analysis, it can be concluded that all code widths of the DDC converter are 1 ± 0.75 LSB, to a measurement accuracy of ± 0.15 LSB.

4.3.2 Code-Mean Method of Analysis

Proving that the output of the converter is a monotonic function of the input, as defined earlier, would require several hundred measurements at every possible input voltage. To simplify the test, we employ a less restrictive definition of monotonicity. For this definition we show that the input is a monotonic function of the discrete output code. For each of the observed output codes, we determine the mean input voltage which produced it. If these code-mean input voltages form a monotonic sequence, then the converter is considered to be monotonic. The separation of the code-mean input voltages is then used to estimate the code widths. If the separation between successive code means is always positive, the converter is monotonic.

For this method of the analysis we calculate the average input voltage associated with each possible output code. All of the calculated code-mean input voltages are a monotonic function of output code for either slope polarity. The separations between successive values

of the code means are shown in figures 23(a), 23(b), and 23(c), for decreasing input voltage, increasing input voltage, and combined slopes, respectively. Horizontal dashed lines at the B2 specification limits of 0.10 and 1.90 times the nominal code width are also shown.

For decreasing voltages, all of the code widths of the DDC converter are within the specification, except for one narrow code. However, for increasing voltages, or for the combined case, all of the code widths are within specification. The minimum spacing between calculated code centers is 0.05 LSB, and the maximum spacing is 1.87 LSB. When both slope polarities are combined, the calculated linearity improves. The distances between code centers are in the range of 0.11 to 1.77 LSB. Based on this analysis, we observe that the DDC A/D converter is strictly monotonic.

4.3.3 Code-Edge Method of Analysis

With this method, we estimate the actual code edges and their spacing. The lower edge of a code is defined as the lowest input voltage which has at least 50 percent probability of producing that code or higher at the A/D converter output. Since each of the 512 K measurements is taken at a unique input voltage, calculating the probability distribution of the output code is complicated. In our analysis we establish a small window of phase angles centered on the code edge. For each code, the window center is adjusted to the lowest center so that more than half of the occurrences are of that code or higher. The width of the sliding window is arbitrary; after evaluating several values, our analysis reveals that a window width of 25 gives optimum results. With the window centered at the code edge, there are 12 measurements with an input slightly larger than the edge, one at the code edge, and 12 slightly below it.

The separation between successive values of the code edges is shown in figures 24(a) and 24(b) for decreasing input voltage and increasing input voltage, respectively. Horizontal dashed lines at the specification limits of 0.10 and 1.90 times the nominal code width are also shown. The measured width of the wide codes is independent of the choice of window width. For the positive slope, there are 37 codes wider than 1.9 LSB — the widest is

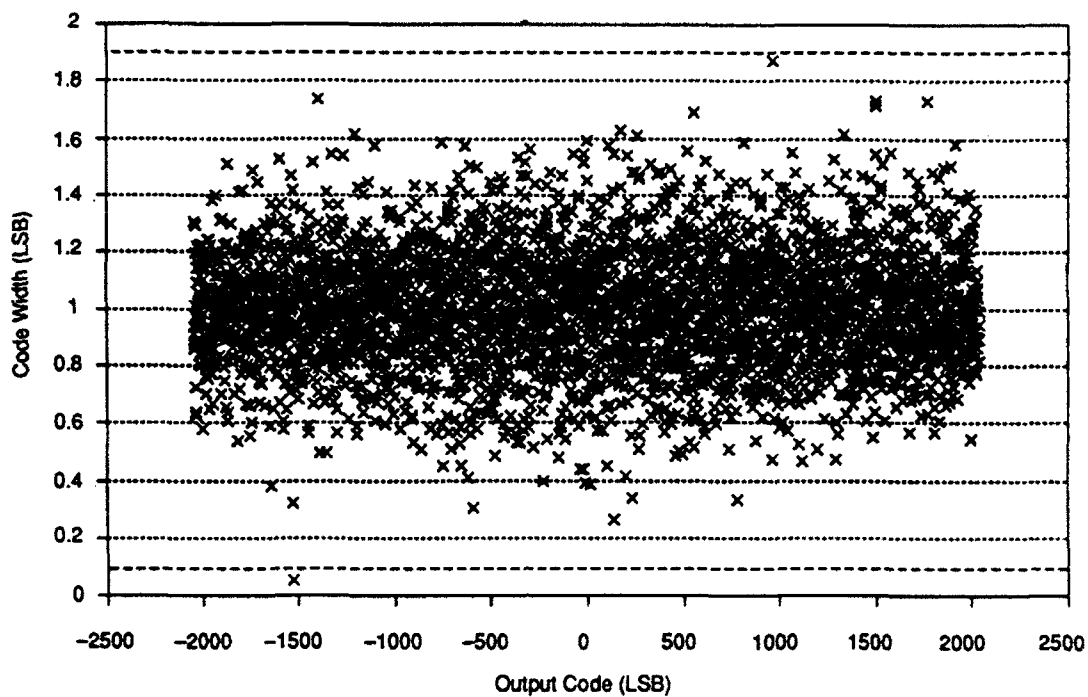


Figure 23(a). Code-Mean Separation for the DDC A/D Converter (Decreasing Voltage)

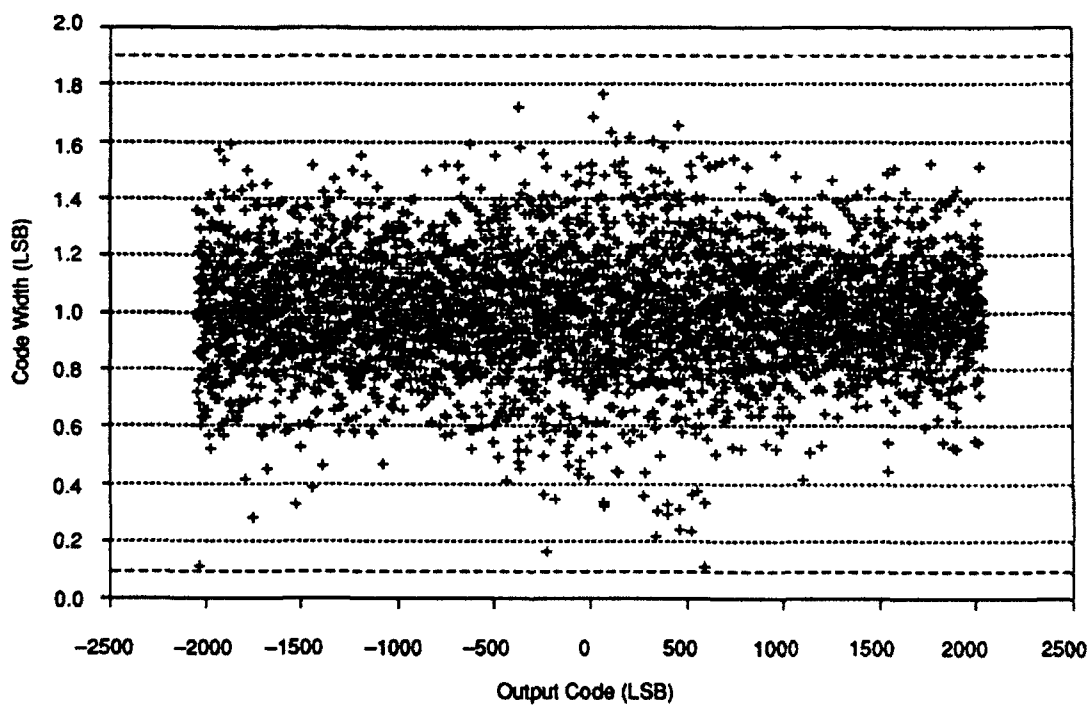


Figure 23(b). Code-Mean Separation for the DDC A/D Converter (Increasing Voltage)

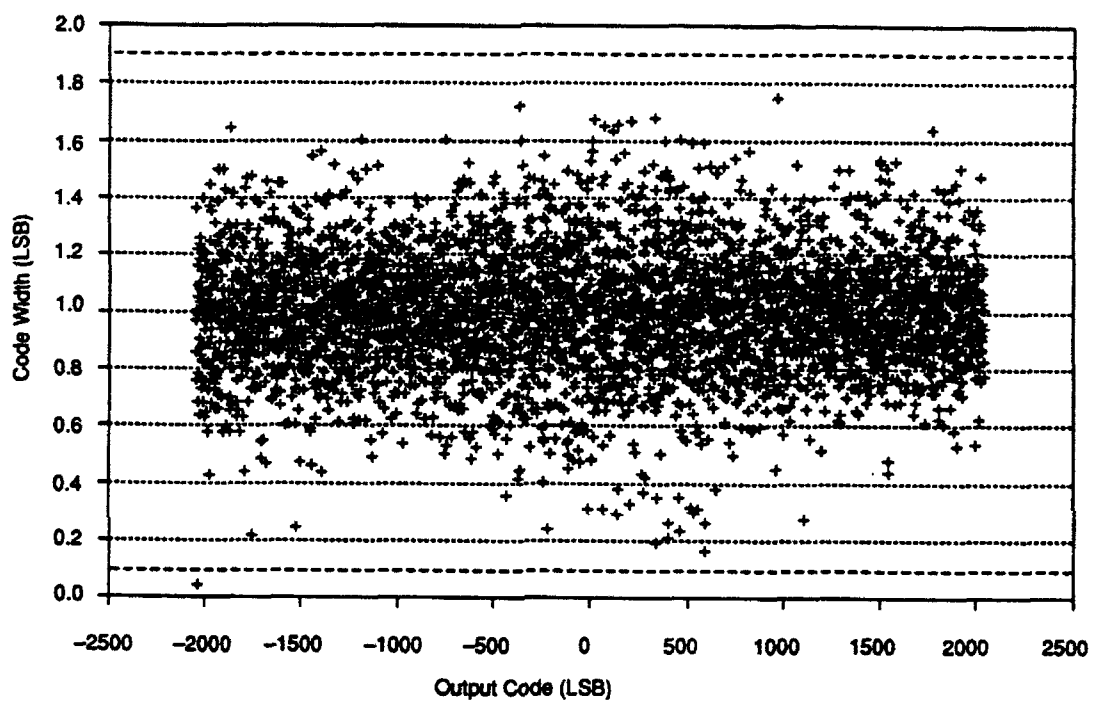


Figure 23(c). Code-Mean Separation for the DDC A/D Converter (Combined Voltages)

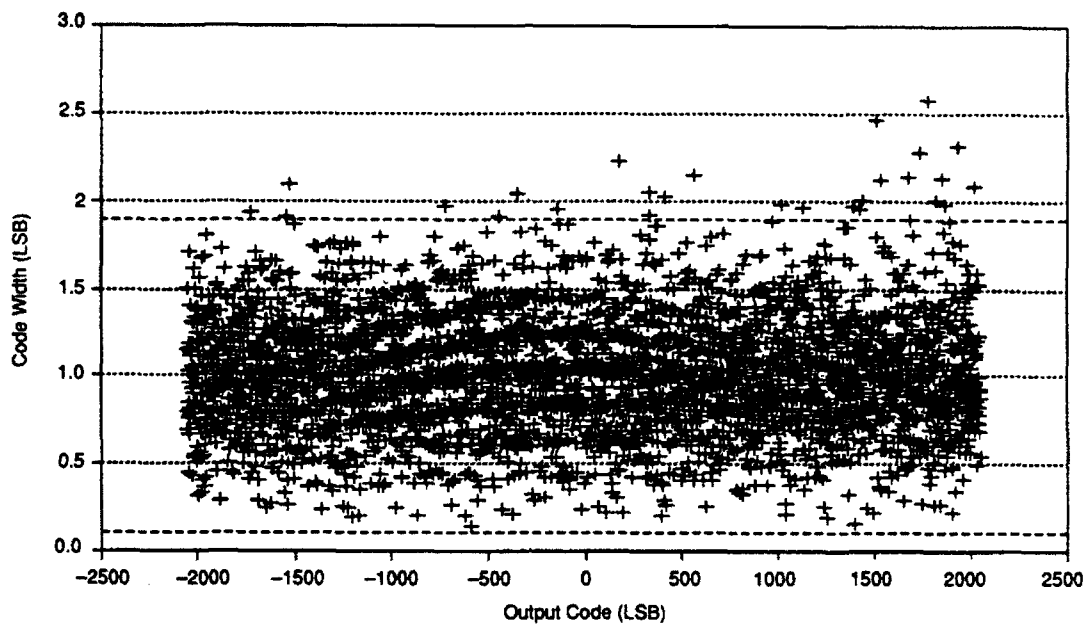


Figure 24(a). Code-Edge Separation for the DDC A/D Converter (Decreasing Voltage)

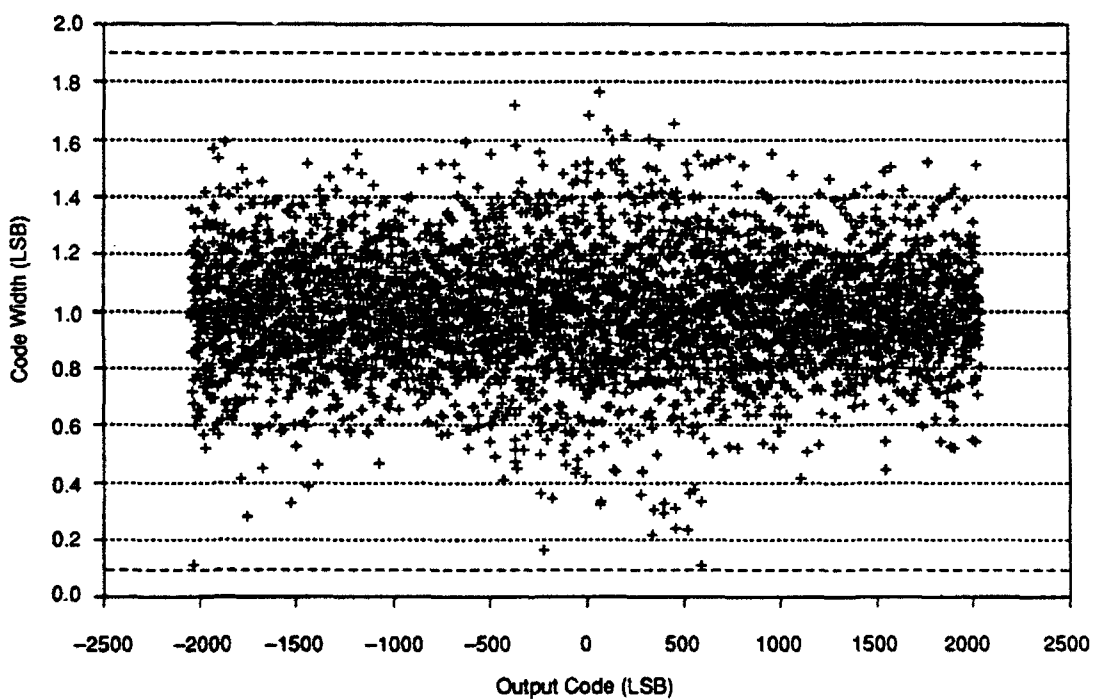


Figure 24(b). Code-Edge Separation for the DDC A/D Converter (Increasing Voltage)

3.01 LSB. For the negative slope, there are 27 codes wider than 1.9 LSB — the widest is 2.58 LSB. Since there are fewer observations of the narrow codes, the effects of noise are greater, and the certainty of conclusions is lower and more dependent on the choice of window width. For the positive slope, there are approximately six codes narrower than 0.1 LSB — the narrowest is 0.007 LSB. For the negative slope, there are no codes that are narrower than 0.1 LSB; the narrowest is 0.14 LSB. With both slopes combined, all codes are wider than 0.04 LSB. Of the three methods described for estimating code width, the code-edge method is the least accurate, and the most susceptible to noise.

4.4 ADC A/D CONVERTER MONOTONICITY ANALYSIS - UNIT 2

The spectral analysis tests of the ADC Unit 2 indicate that it has a serious problem when the input signal is a large amplitude sine wave of more than 1.0 MHz. Whenever the input voltage exceeds 75 percent of positive full-scale, it causes the next conversions to exhibit large blocks of missing codes for negative voltages spaced 128 LSB apart. At 1.25 MHz there are five blocks of more than 15 consecutive missing codes, and peak errors of 20 LSB. Figure 21(a) shows the errors as a function of the input signal phase angle in radians after the positive peak. Hence, prior to performing the monotonicity tests, we already know from the phase-plane error analysis that the converter is not strictly monotonic and that it has gross errors. Because we suspect that the converter errors might be related to signal amplitude exceeding positive saturation, we reduce the test signal amplitude slightly (to 1990 LSB), which is 9 LSB less than saturation because of the converter offset. However, we use the same signal frequency as that used for testing the DDC converter. We now present an analysis using the histogram and code-mean methods.

4.4.1 Histogram Method

Figures 25(a), 25(b), and 25(c) show the normalized histogram for decreasing voltage, increasing voltage, and the combined slope polarities, respectively. The increasing voltage data has a block of three consecutive missing codes which occur on the third sample after the positive peak. Figure 25(a) (decreasing voltage) shows that there are 174 missing codes, grouped into blocks that are spaced 128 LSB apart. The largest block is 17 consecutive

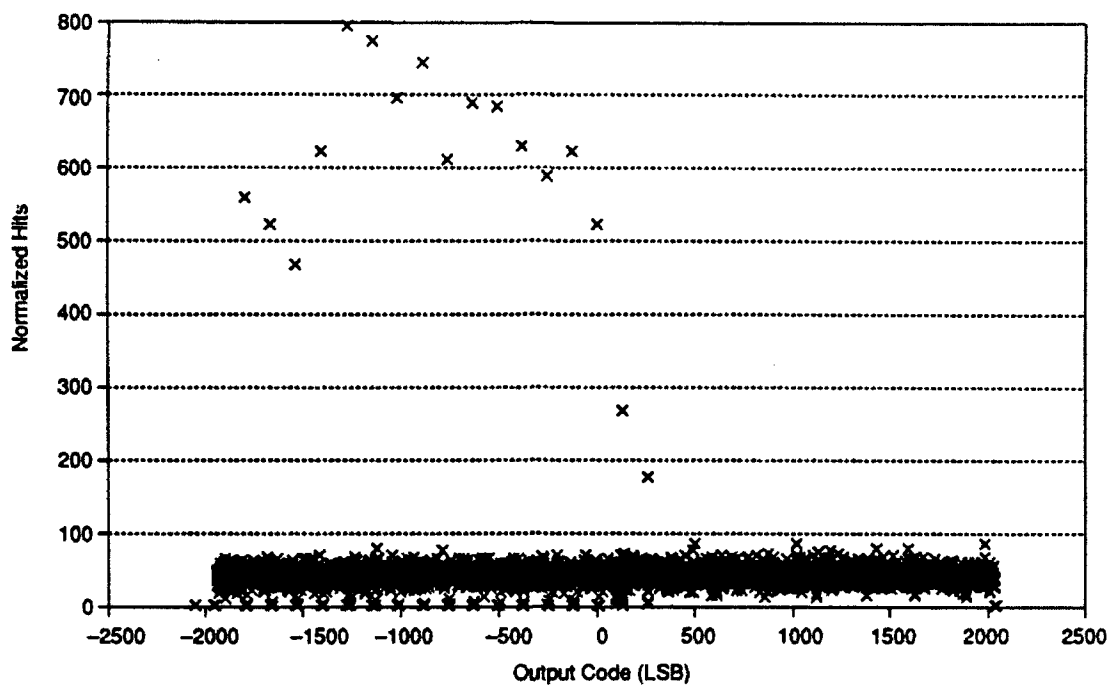


Figure 25(a). Normalized Histogram for the ADC A/D Converter – Unit 2
(Decreasing Voltage)

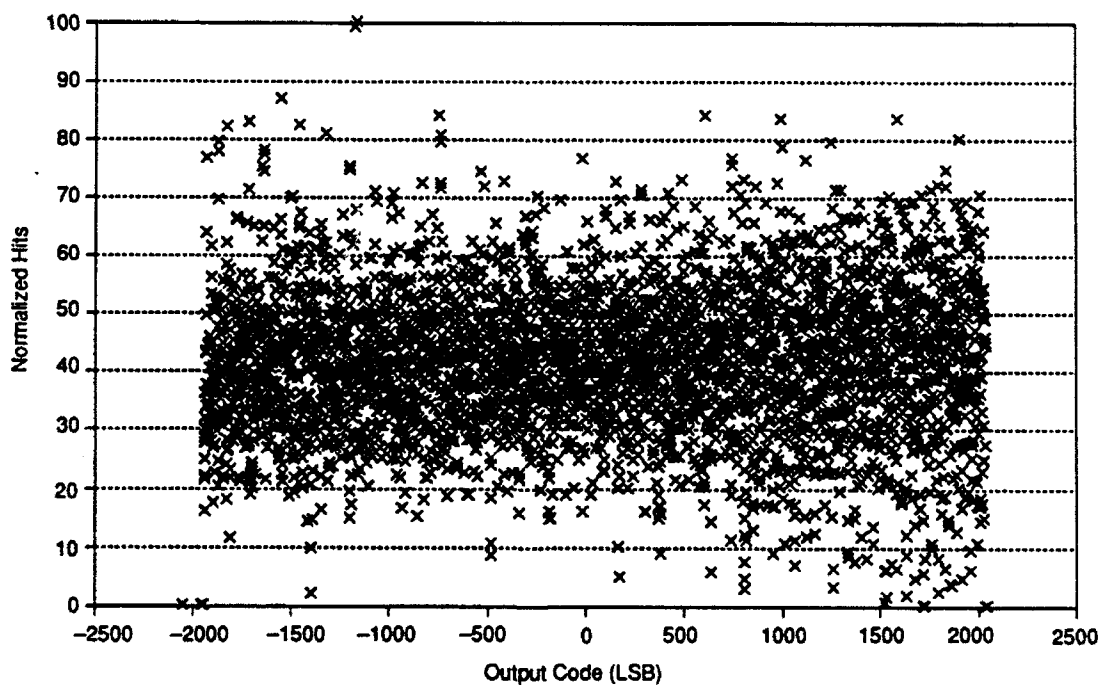


Figure 25(b). Normalized Histogram for the ADC A/D Converter – Unit 2
(Increasing Voltage)

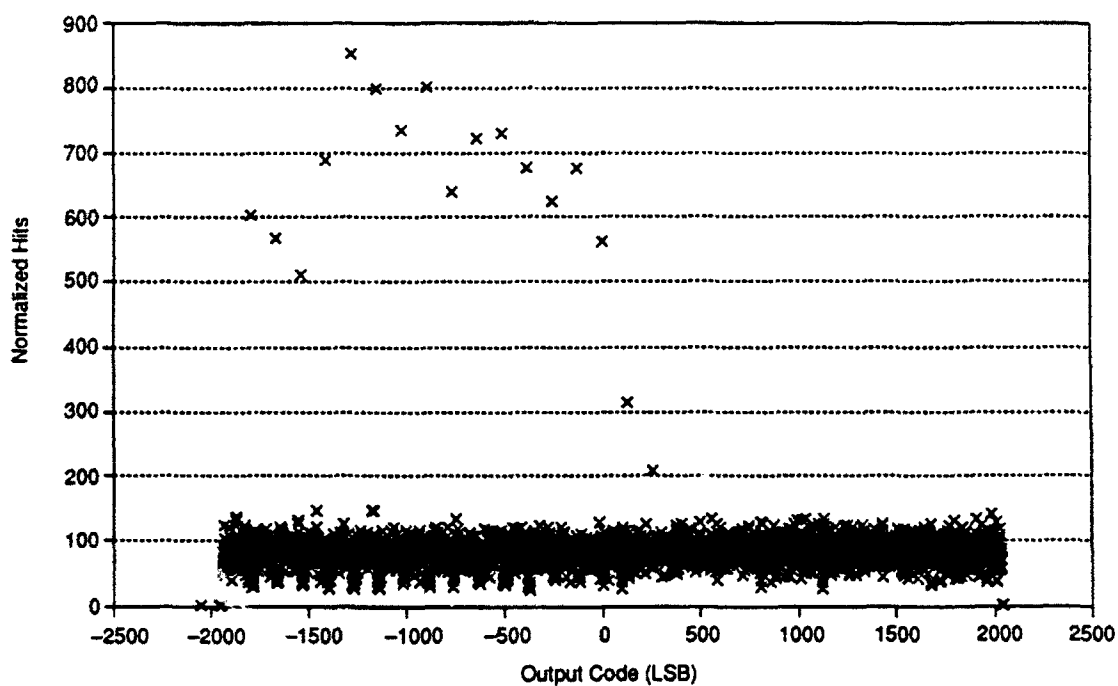


Figure 25(c). Normalized Histogram for the ADC A/D Converter – Unit 2
(Combined Slopes)

missing codes, and the resultant width of the next code is 18 LSB. By combining the positive-going and negative-going data, no missing codes are found.

4.4.2 Code-Mean Method

Figures 26(a), 26(b), and 26(c) show the code widths computed as the difference between successive code means for decreasing voltage, increasing voltage, and the combined slope polarities, respectively. For decreasing voltage, near the edge of the missing codes some codes are not completely missing, but have an abnormally low number of observations. The code-mean voltages calculated for these codes form a non-monotonic sequence, with a minimum code separation of -1.15 LSB. By combining the positive-going and negative-going data, no missing codes are found. The mean-code voltages form a non-monotonic sequence, with a minimum spacing of -8.90 LSB, and a maximum spacing of 10.64 LSB.

This converter illustrates the importance of processing the data according to the phase of the input signal, thereby separating the positive-going measurements from the negative-going ones. Had we combined both slope polarities, there would not have been any missing codes, and we would not have observed an obvious explanation for the extremely nonlinear behavior.

4.5 SUMMARY AND CONCLUSIONS OF MONOTONICITY ANALYSIS

Table 9 summarizes the monotonicity analysis of the converters using the three different methods (the histogram, code-mean, and code-edge methods). Since many subranging A/D converters behave differently with increasing or decreasing (i.e., positive-going or negative-going) signals, we present the analysis for positive-going or negative-going, and combined slopes to gain better insight. Based on our analysis, we conclude that the DDC converter is strictly monotonic and marginally meets the UAR B2 specification requirements. As indicated in table 2, the DDC converter appears to have several codes which may be slightly wider than the B2 specification. Confirming this with high confidence would require many more samples than we used in our analysis (greater than 512 K). The ADC converter is

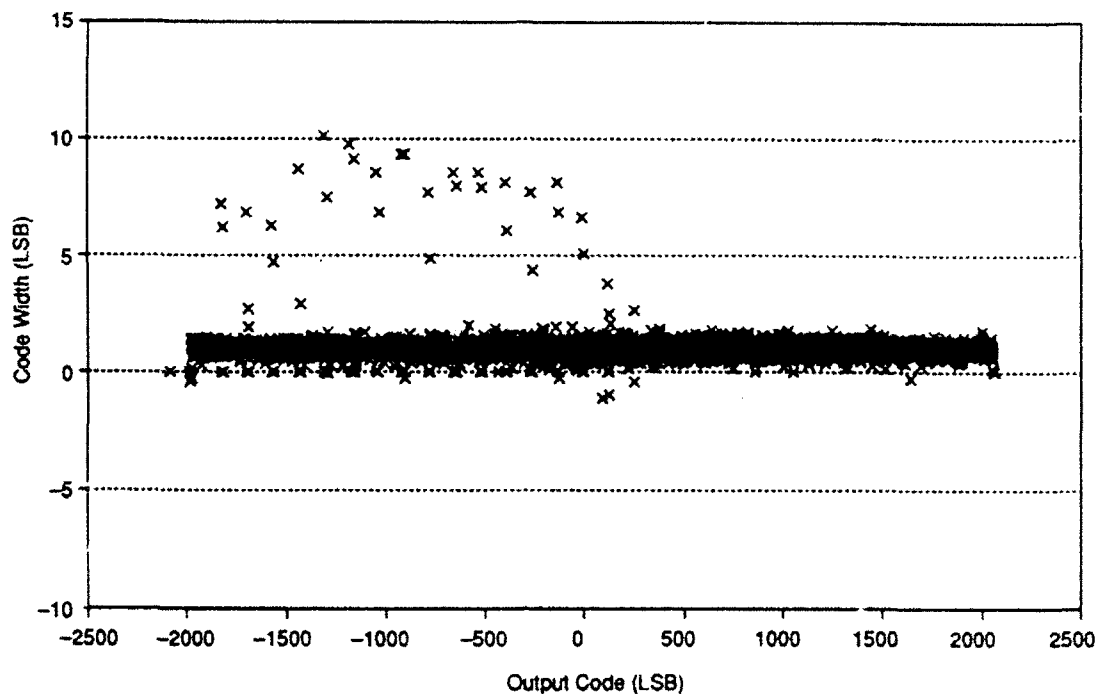


Figure 26(a). Mean Code Width for the ADC A/D Converter – Unit 2
(Decreasing Voltage)

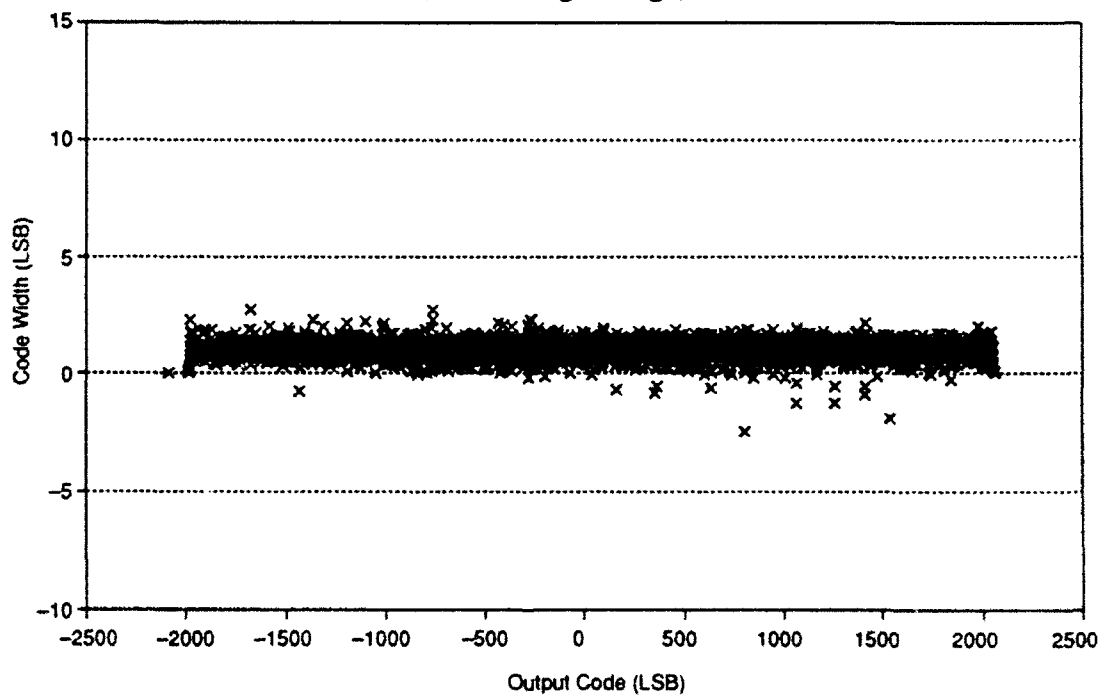


Figure 26(b). Mean Code Width for the ADC A/D Converter – Unit 2
(Increasing Voltage)

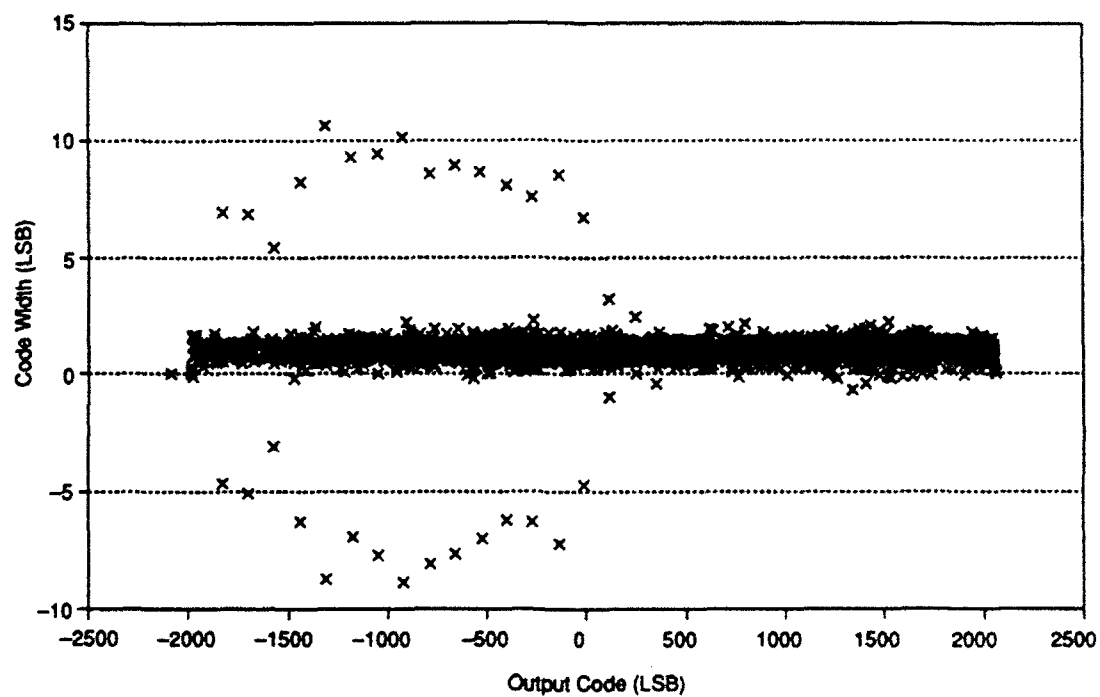


Figure 26(c). Mean Code Width for the ADC A/D Converter – Unit 2
(Combined Slopes)

nonmonotonic and has gross errors, particularly for negative-going voltages, and it does not meet UAR B2 specification requirements.

Table 9. Monotonicity - Differential Nonlinearity Test Results

<u>DDC A/D Converter</u>					
<u>Test Method</u>	<u>Converter Type</u>	<u>Narrower Than Spec</u>	<u>Narrowest Code in (LSB)</u>	<u>Widest Code in (LSB)</u>	<u>Wider Than Spec</u>
Specification	DDC	0	0.10	1.90	0
Histogram Decreasing	DDC	0	0.22	2.38	3
Histogram Increasing	DDC	1	0.05	2.51	7
Histogram Combined	DDC	0	0.31	2.01	1
Code Mean Decreasing	DDC	1	0.05	1.87	0
Code Mean Increasing	DDC	0	0.11	1.77	0
Code Mean Combined	DDC	1	0.04	1.75	0
Code Edge Decreasing	DDC	0	0.14	2.58	27
Code Edge Increasing	DDC	6	0.007	3.00	37
Best Estimate	DDC	0	0.25±0.15	1.75±0.15	0

<u>ADC A/D Converter</u>				
<u>Test Method</u>	<u>Converter Type</u>	<u>Narrower Than Spec</u>	<u>Narrowest Code in (LSB)</u>	<u>Widest Code in (LSB)</u>
Specification	ADC	0	0.10	1.90
Histogram Decreasing	ADC	174	0.00	20.92
Histogram Increasing	ADC	3	0.00	2.64
Histogram Combined	ADC	0	0.30	11.22
Code Mean Decreasing	ADC	174	-1.15	10.11
Code Mean Increasing	ADC	3	-2.50	2.70
Code Mean Combined	ADC	0	-8.90	10.64

SECTION 5

TRANSIENT AND OVERVOLTAGE RECOVERY TESTING RESULTS

In sections 3 and 4, we validated the B2 requirements for the RMS-signal-to-RMS noise ratio, SFDR, and monotonicity requirements. The B2 specification requires that the A/D converter recover from any transient or overrange input condition to an accuracy of ± 5.0 mV within 200 nanoseconds. The converter should be tested for all baseline voltages within its ± 2.047 V linear range, with pulses whose peak voltages span the allowable ± 4.0 V overvoltage input range. In this section, we validate the transient and overvoltage recovery requirements of both converters.

5.1 TEST DESCRIPTION

The test is a variant of the standard sine-wave test described in section 2. The input signal applied to the A/D converter under test is the sum of three signal components: a (dc) level which is close to the saturation point of the converter; a small 70-Hz triangular modulation added to the dc level; and a train of large amplitude pulses superimposed on the two signal components. The pulses are one microsecond wide, repeated with a period of four microseconds. The input signal is applied to the A/D converter under test and the resulting digital output is stored in the Tektronix High-Speed Data Cache (a large, fast, sequentially-addressed memory), and stored as a file on a floppy disk.

Since the pulse repetition period is 16 cycles of the 4-MHz clock, a data record of 64 K measurements includes 4096 pulses. In the absence of external triangular modulation, the measurements repeat exactly, except for the converter and test fixture noise. With a one-microsecond nominal pulsewidth, there are four measurements of the pulse, followed by twelve measurements of the settling between pulses. By applying a small 70-Hz triangular modulation, a full cycle of the modulation is obtained in one data record, allowing investigation of the converter performance over a limited range of input voltages. Note that in this test the voltages of each pulse are modulated, but the relative phase of each measurement in each pulse is the same.

5.2 TEST CIRCUIT DESCRIPTION

As discussed in section 1, we designed and built a test fixture which can generate a pulse to 12 bits accuracy. The schematic diagram of the fixture is shown in figure 27, and the assembly print is shown in figure 28. The details of the test fixture are discussed below.

In normal operation, a square transistor-transistor-logic (TTL) level, 4-MHz clock is applied to the test circuit. The input clock is buffered by integrated circuit Z8, and provided as an output signal to drive the A/D converter. A counter circuit (Z5 and Z6) driven by the input clock produces a digital pulse that is one microsecond (four clock cycles) wide, with a frequency of 250 kHz. The digital pulse is delayed by latch Z7 for an interval which is adjustable via potentiometer P2, then applied to a current switch formed by transistors Q1 to Q6.

The current switch superimposes an analog voltage pulse upon a baseline voltage which is established by operational amplifier Z1. Switches SW1 and SW2 control the polarity and amplitude of the analog pulse, respectively. The baseline voltage consists of a dc component which is set via potentiometer P1, plus an optional small modulation which is an inverted and attenuated replica of a low-frequency signal applied to the external modulation input. The current switch is designed so that the load on Z1 is independent of the state of the switch.

The baseline voltage at the output of amplifier Z1 is bypassed to system ground by a large, low-impedance capacitor network. This prevents it from changing rapidly, and insures that the output voltage is exceptionally clean and stable in the time interval between pulses. The resultant pulse rise and peak are only moderately stable, but the fall to baseline is fast and clean, with no ringing or overshoot. The pulse fall time is completely dominated by a single (resistor-capacitor (RC)) time constant. The effective resistance is 250 ohms, and the total capacitance is approximately 50 picoFarads, which is mainly from the short cable used to connect the test fixture to the A/D converter. The output, therefore, has a time constant of approximately 13 nanoseconds. This means that a 4 V pulse settles to within ± 5.0 mV in 87 nanoseconds, and to ± 2.0 mV in 99 nanoseconds. Smaller pulses settle slightly faster.

170283/VTC370

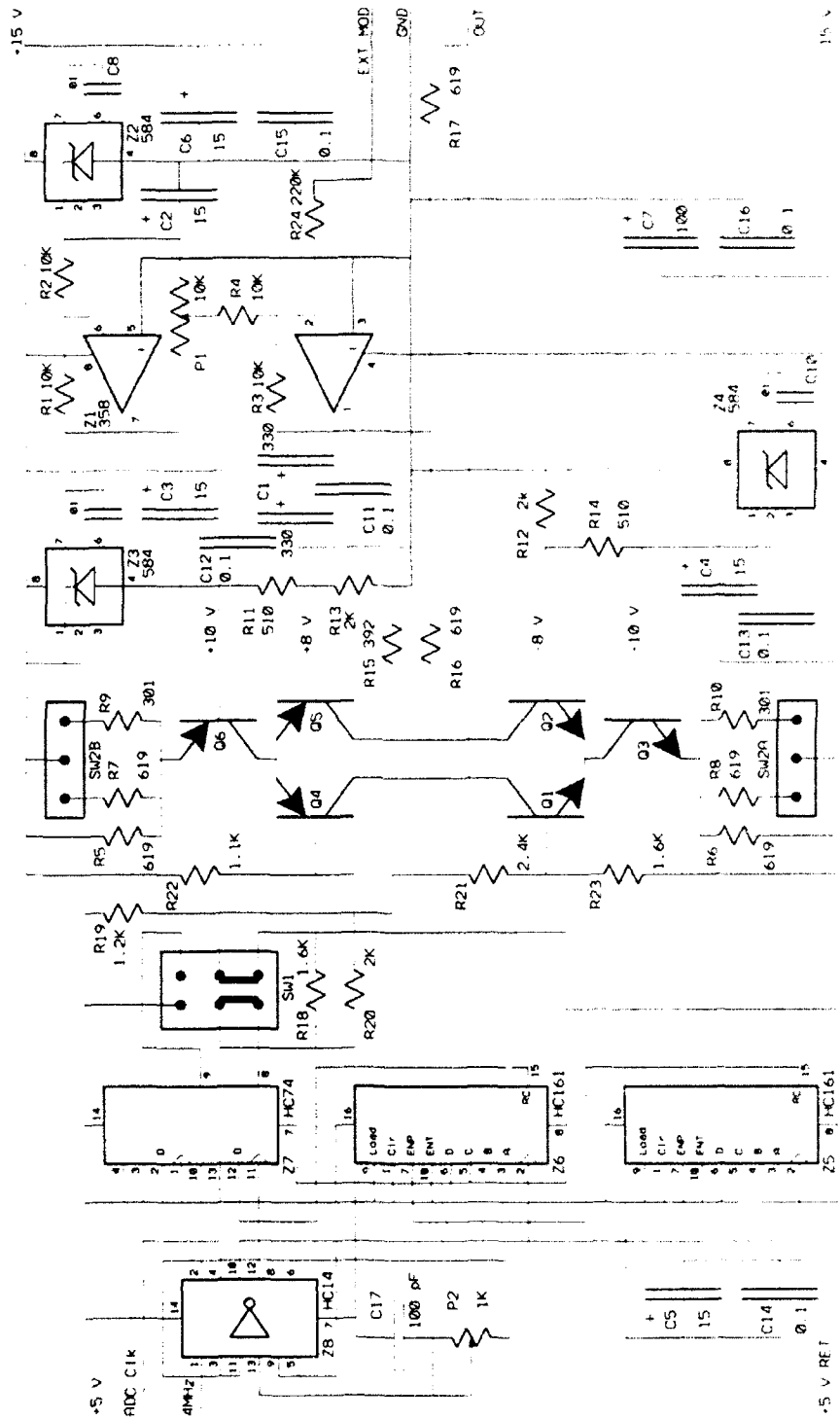


Figure 27. Pulse Generator Schematic

NY0272/VY0339

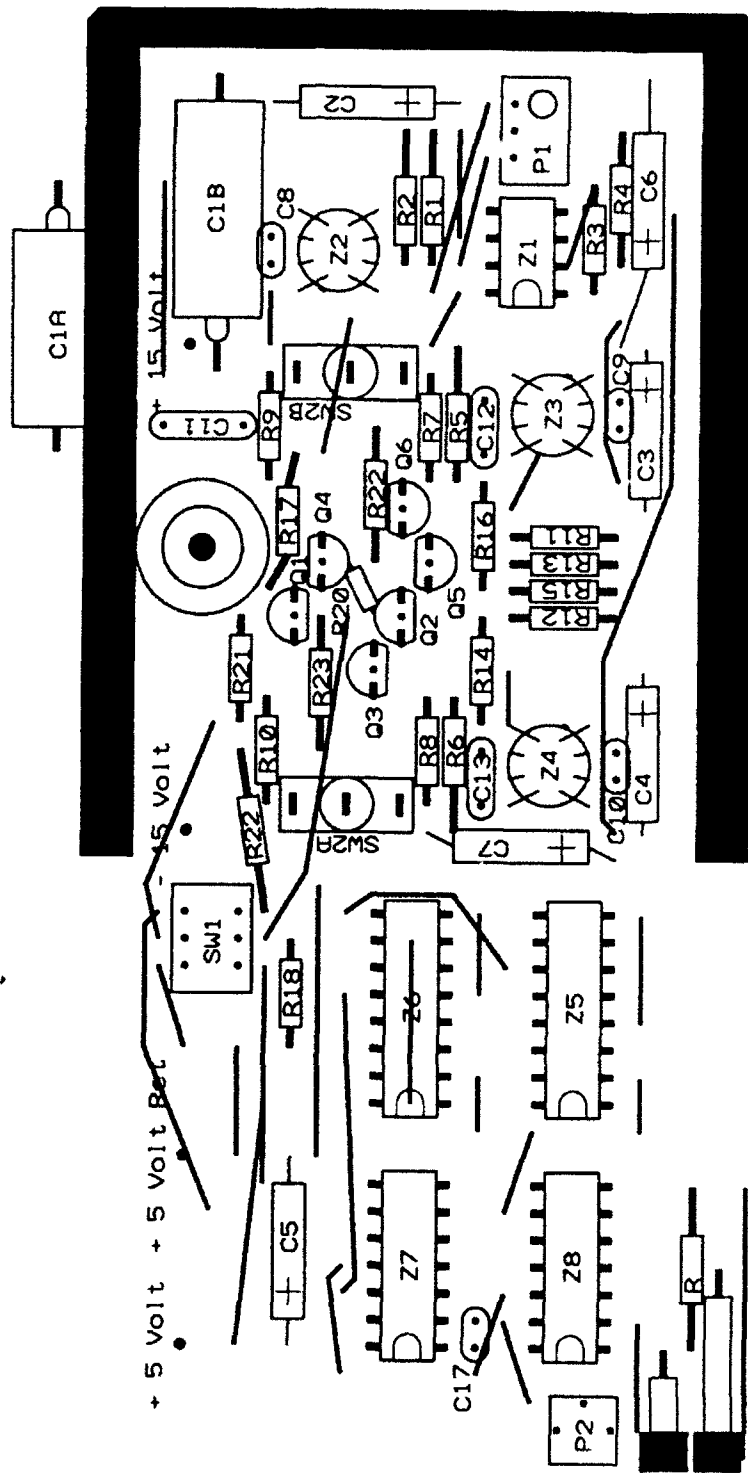


Figure 28. Pulse Generator Layout

5.3 DATA ANALYSIS

The 64 K measured output codes are entered into a computer spreadsheet, and reordered to fill a table of 4096 lines of 16 columns. By reading horizontally along a line, we get 16 sequential measurements of one pulse. By reading the table vertically down, we get measurements made on 4096 pulses, at the same relative phase.

5.3.1 DDC A/D Converter Overvoltage and Transient Recovery Results

Figures 29 and 30 show the performance of the DDC A/D converter with baseline voltages ranging from -1.9 to -2.05 V near the negative saturation, with a 150 mV triangular waveform superimposed. A +4.5 V pulse drives the converter into positive saturation. Using this modulation, the baseline voltage changes by only 0.08 mV per pulse, so effectively we are testing at all input voltages over a 150 mV range. In both figures 29 and 30, the horizontal axis represents the number of the pulse after the start of the record, i.e., four microseconds per pulse. Figures 29 and 30 differ slightly (70 nanoseconds) in the delay between the pulse and the A/D converter clock. In our test, we take data for two different values of circuit delays between the pulse and the A/D converter clock of 20 and 90 nanoseconds. We choose those two delays so that the time available until the next measured sample of the pulse in one case is slightly more than 200 nanoseconds, and in another case it is slightly less than 200 nanoseconds. In figure 29, the nominal start of the pulse occurs 20 nanoseconds after a clock, and 230 nanoseconds before the next A/D converter clock triggers another measurement. In figure 30, the voltage pulse is delayed to 90 nanoseconds after a clock, so it is only 160 nanoseconds before the next A/D converter clock triggers the next measurement.

Each figure has three triangular waves showing the converter output codes. The highest triangle is the first measurement after the end of the pulse. The middle triangle is the next measurement, and the lowest triangle is the last measurement, just prior to the next pulse. In both figures 29 and 30, the triangular outputs are smooth and have uniform separation, which indicates that the converter has no major nonlinearities in this region, and that the settling response is essentially independent of the final voltage. The bottom parts of figures 29 and 30 show the spread between the largest and smallest values of the 11 measurements between

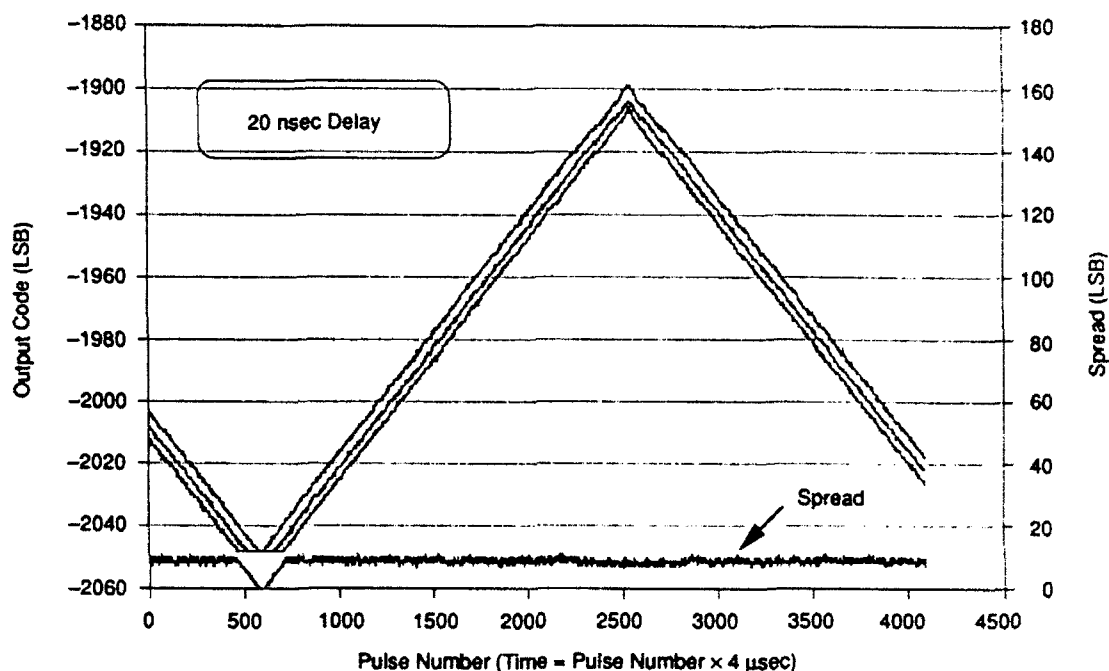


Figure 29. Overvoltage Recovery Response of DDC A/D Converter When Pulsed into Positive Saturation (20 nsec Delay)

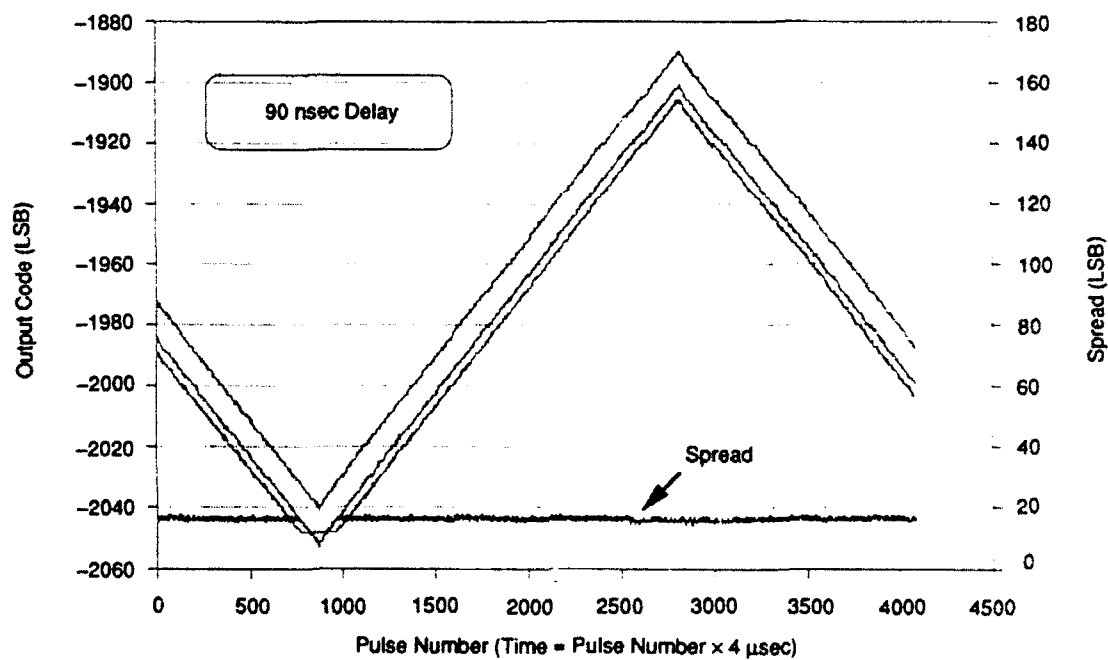


Figure 30. Overvoltage Recovery Response of DDC A/D Converter When Pulsed into Positive Saturation (90 nsec Delay)

consecutive pulses. In figure 29 it is 9 ± 1 mV; however, in figure 30 it is 17 ± 1 mV, since the pulses have less time to settle.

Figures 31 and 32 show the settling response on an expanded scale, when the converter is pulsed into positive saturation for circuit delays of 20 and 90 nanoseconds, respectively. Each figure shows the output codes for 11 consecutive measurements of the settling interval between pulses. Three lines on each figure show the output at intervals separated by 200 microseconds (i.e., 50 pulses, or about 4 mV in input voltage). The bottom curve in figure 31 shows the output code against the compressed full-scale range axis on the right edge of the figure. On this scale, sample number zero is made at an input of about + 300 LSB on the falling edge of a pulse, and sample number 12 is made at about the -900 LSB level of the next pulse. The other samples not shown are all at positive saturation, i.e., + 2047 LSB. With an ideal infinitely fast pulse with zero fall time, we would like all of the measurements between pulses to produce the same output code. However, because the fall time is not infinitely fast and there are delays in the converter, the actual output code decays exponentially to its final value. For the case where the measurement starts 230 nanoseconds after the start of the fall of the pulse (i.e., with a 20-microsecond delay), a sample is taken near the zero crossing of the signal, and sample 12 is taken near the middle of the rise of the next pulse. This shows that sample 1 is 250 nanoseconds after the midpoint of the falling edge of the pulse. As discussed earlier (from figure 3), the output has settled to 9 mV in an additional 250 nanoseconds, whereas the B2 specifies a settling accuracy of ± 5 mV within 200 nanoseconds. Figure 30, showing a settling time of $250 - 70 = 180$ nanoseconds from the midpoint of the falling edge of the pulses, has 17 LSB of decay.

It can be concluded from our analysis that the DDC A/D converter does not meet the overvoltage and transient recovery radar B2 requirements.

5.3.2 ADC A/D Converter Overvoltage and Transient Recovery Results - Unit 2

Figures 33 and 34 show the performance of the ADC Unit 2 with baseline voltages ranging from -1.7 to -2.02 V near the negative saturation, with a 320 mV triangular waveform superimposed. There is a 4.5 V amplitude pulse driving the converter into positive

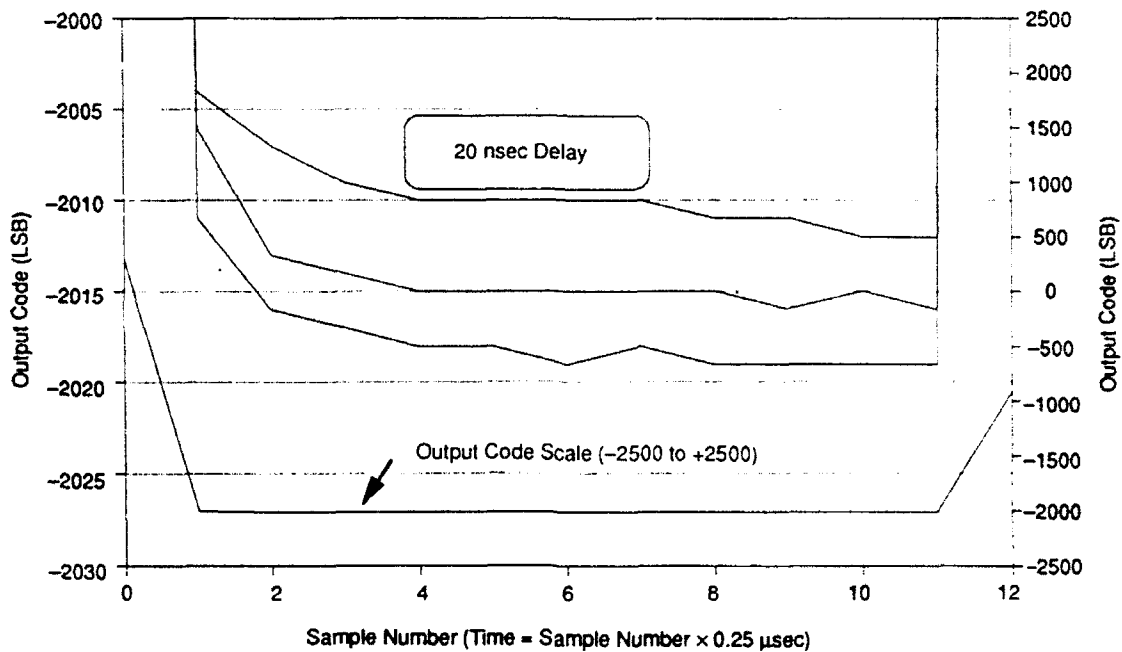


Figure 31. Overvoltage Recovery Response of DDC A/D Converter When Pulsed into Positive Saturation on an Expanded Scale (20 nsec Delay)

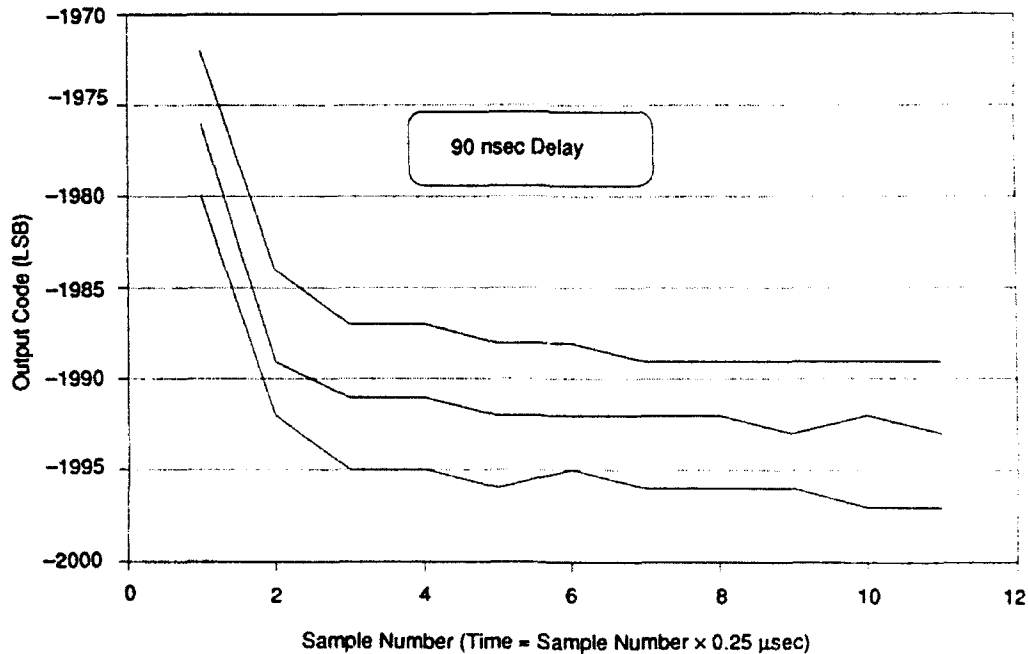


Figure 32. Overvoltage Recovery Response of DDC A/D Converter When Pulsed into Positive Saturation on an Expanded Scale (90 nsec Delay)

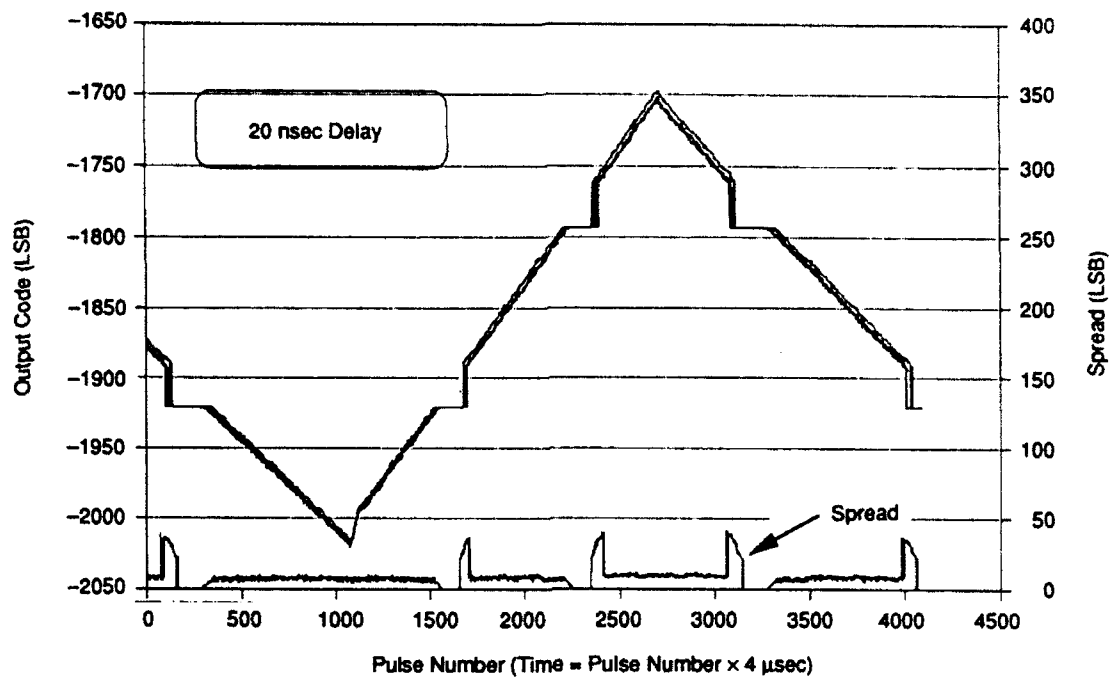


Figure 33. ADC A/D Converter – Unit 2 – Pulsed into Positive Saturation

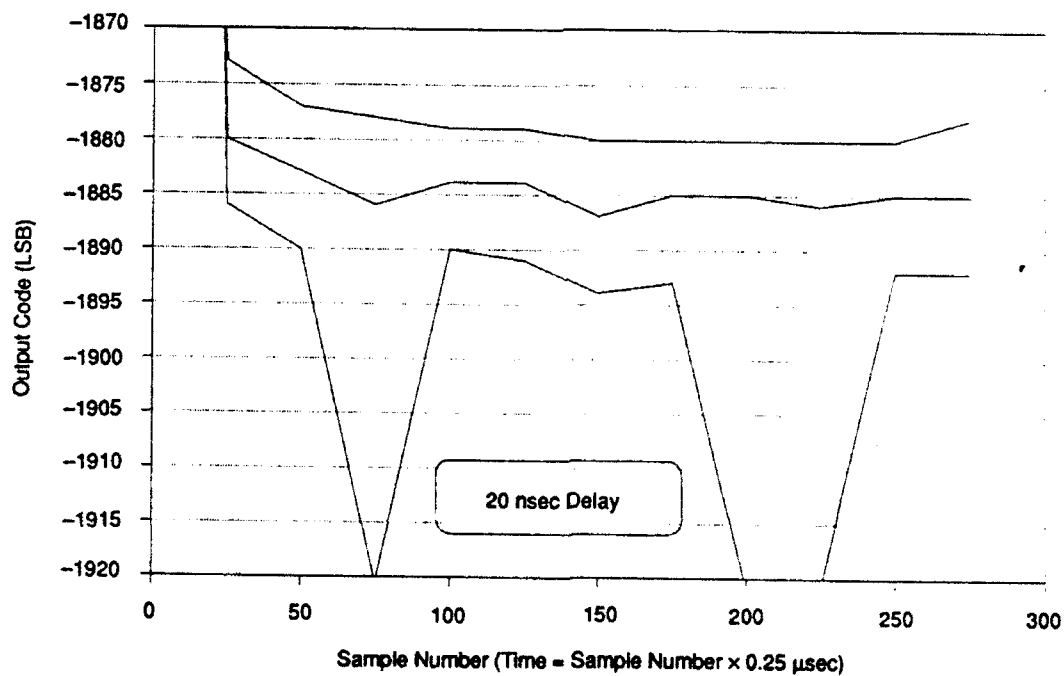


Figure 34. Overvoltage Recovery Reponse of ADC A/D Converter – Unit 2 When Pulsed into Positive Saturation on an Expanded Scale (20 nsec Delay)

saturation. Using this modulation, the baseline effectively changes by only 0.16 mV per pulse, so we are testing at all input voltages over a 320 mV range. Figure 33 shows that this converter has a serious problem, since the output is not a clean triangular waveform. At certain voltages, there are large groups of missing codes spaced 128 LSB apart. The behavior in one of the missing code regions is substantially different from that in the good regions. The peak errors are up to 40 LSB. Even three microseconds after the voltage has stabilized (i.e., reached the unsaturated voltage level) the output codes for this converter are in error and certain codes do not occur.

Figure 34 shows an expanded view of the settling for three different input voltages. The upper two curves, which are in a good input voltage region, show rapid settling to within 5 LSB of the final value. However, the lowest curve, at the edge of a missing code region, shows interesting settling behavior, as indicated in figure 34. The converter starts to function properly on samples 1 and 2, but on sample 3 it suddenly produces an error of -30 LSB. It then recovers, and works correctly for samples 4 through 7. Samples 8 and 9, which are two microseconds after the end of the pulse, again produce an error of -30 LSB. Because the settling problem persists for more than three microseconds after the end of the pulse, changing the pulse delay by another 70 nanoseconds, as done for the DDC converter, will not reveal any additional information. Therefore, we test this converter only for a 20-nanosecond delay between the pulse and the A/D converter clock. A comparison of the DDC and ADC transient overvoltage recovery characteristics clearly indicates that the DDC converter has a better performance.

5.4 BEAT FREQUENCY TEST

In section 5.3, we present the settling response of the converters with a time resolution of 0.25 microsecond per measurement. By combining many different data records taken with different circuit delay times set by the potentiometer P2, it would be possible to determine the settling response to a better time resolution by taking many measurements with various circuit delays and combining the different data records in software. However, the beat frequency test can be used to easily determine the settling response to a fine time resolution.

This test method allows us to obtain a detailed record of the settling response of the converter for one particular input voltage. In the test method described previously, we show that the settling response of the DDC converter is independent of the input voltage. Hence, this measurement technique at one voltage is representative of all other voltages near the negative saturation. In this section we present beat frequency test results for transient recovery and overvoltage recovery time of the converter.

The first two cases are for the transient recovery specification. The dc baseline voltage is set in the linear range near the saturation point (negative and positive voltages, respectively), and then it is pulsed with a signal that drives it near the opposite saturation point. We also perform additional tests which drive the converter into saturation in order to measure the overvoltage recovery time. The next section describes the details of the beat frequency test setup.

5.4.1 Test Description

The beat frequency test uses two clocks, one for the pulse generator test equipment, and another for the A/D converter. They are at slightly different frequencies, so their relative phases change slowly, allowing us to measure all phases of the pulse waveform.

For this test, the A/D converter is clocked at 4.0 MHz by a Hewlett Packard pulse generator. A second pulse generator is phase-locked to the first, and set to produce a slightly higher frequency (4003910.07 Hz). This second pulse generator is then used to drive the test circuit, which produces the signal voltage pulses at 250244.38 pulses per second. This frequency is chosen so that the tester receives 1024 clocks in the time that the A/D converter receives 1023 clocks, and the phase of the signal being sampled will slowly increase. For example, assume that at time zero, both clocks are in phase and samples are being taken every 0.25 microsecond. After 3.99609375 microseconds, the test circuit has received 16 clocks and has produced exactly one cycle of the pulse waveforms so that the waveshape repeats every 3.99609375 microseconds. However, the sixteenth sample is not taken until $(4 - 3.99609375 \text{ microseconds}) = 3.40625 \text{ nanoseconds}$ after we start the second pulse. At this instant the second pulse signal amplitude is equal to the amplitude of the first pulse at 3.9

nanoseconds. When the tester receives 1024 clocks, it produces 64 pulses, and the A/D converter makes 1023 measurements, so it is once again in phase with the tester clock. In the first 1023 microseconds of a 1024 microsecond data record, which includes 4092 A/D converter measurements of 256 pulses, the relative phase of the converter and pulse clocks slowly changes by four clock periods (or one microsecond). Reordering the sequence of measurements is equivalent to measuring four complete cycles of the pulse waveform with a time resolution of 3.90625 nanoseconds.

5.4.2 DDC A/D Converter Results from the Beat Frequency Test

5.4.2.1 Transient Recovery Performance

Figure 35 shows the pulse response of the DDC A/D converter with a large positive pulse, which causes voltage swings from a baseline near the negative limit of -1.75 V to near the positive limit of +1.75 V. The output waveform is extremely clean, with no visible ringing or overshoot.

Figure 36 is an enlarged display of the initial region from zero to 300 nanoseconds of the settling response at the end of the pulse. The output has settled within 5 LSB of its final value in 280 nanoseconds after the end of the pulse. Equivalently the output has settled within 5 LSB of its final value in 240 nanoseconds after the pulse has dropped to mid-scale. If we calculate starting time from when the input pulse has reached 5 LSB of its final value (87 nanoseconds), the converter only requires an additional 193 nanoseconds, which would be within specification. Since the dc baseline voltage is set in the linear range, it can be concluded that the DDC converter recovers from the transient input condition in either 193, 240, or 280 nanoseconds within 5 LSB of its final value; however, the B2 specification requires that it recover in 200 nanoseconds.

5.4.2.2 Overvoltage Recovery Performance

Figure 37 shows the overvoltage recovery performance of the DDC converter when measuring large negative voltages and recovering from a previous measurement in a positive

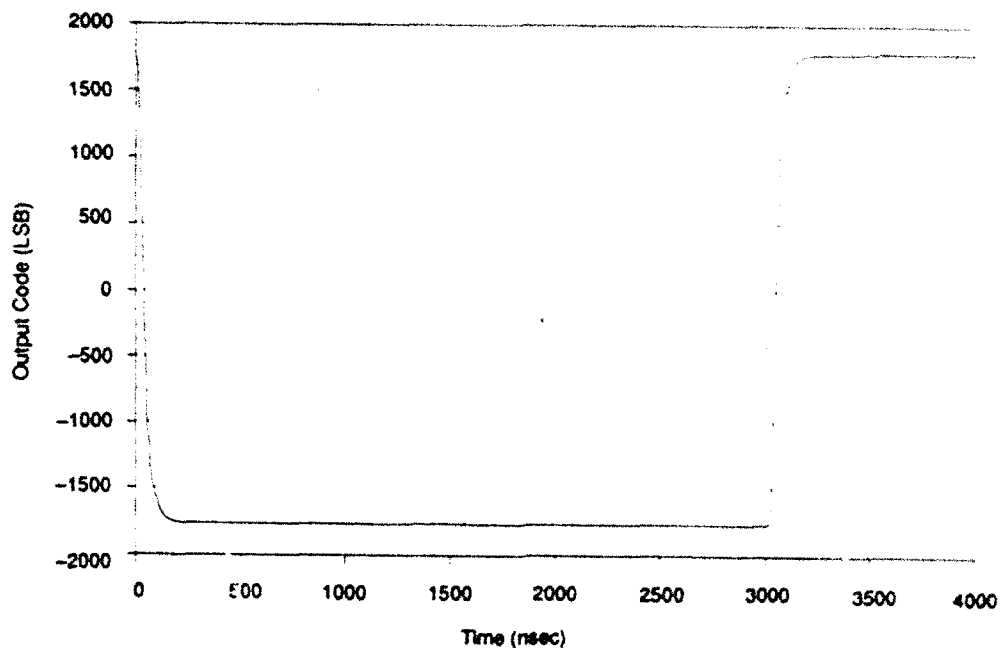


Figure 35. Pulse Response of DDC A/D Converter with a Negative Base Voltage and a 1 μ sec Pulse of +3.5V

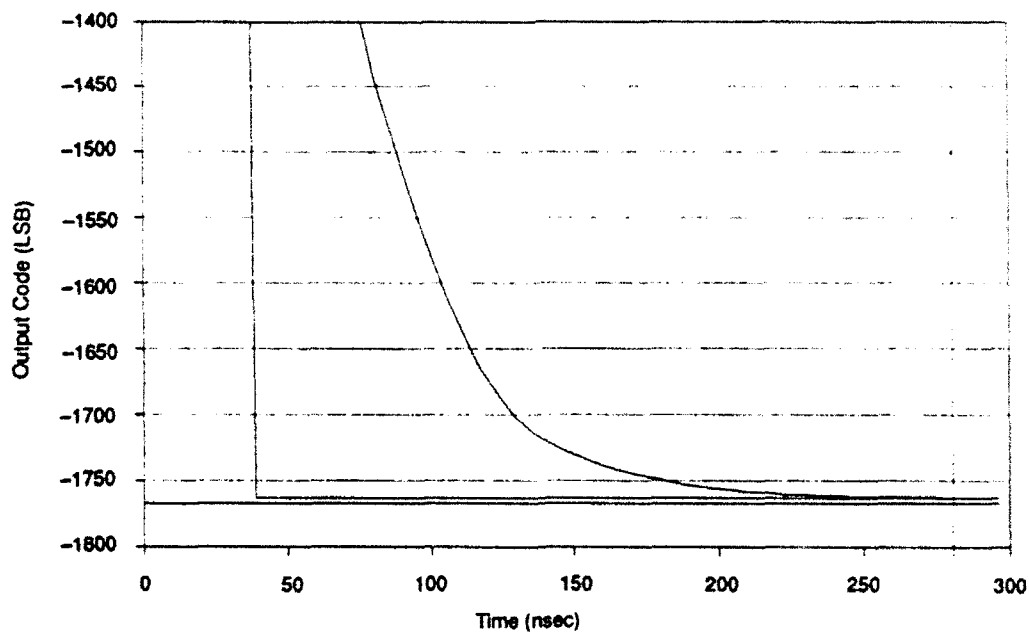


Figure 36. Settling Response of DDC A/D Converter with a Negative Base Voltage and a 1 μ sec Pulse of +3.5V on an Expanded Scale

saturation. In this test the converter recovers from the overrange input condition in 361 nanoseconds from the first unsaturated measurement, within 5 LSB of its final value.

Figure 38 shows the overvoltage recovery performance of the DDC converter when measuring large negative voltages and recovering from a previous measurement in a hard negative saturation. In this case, it recovers in only 155 nanoseconds after it comes out of saturation, within 5 LSB of its final value.

Figure 39 shows the pulse response of this converter for a signal with a dc value set near the positive saturation limit of the converter and pulsed with a -3.5 V negative amplitude pulse to near the negative limit of the converter. Figure 40 shows the recovery response of this converter on an expanded scale recovering from a large negative -4.5 V amplitude pulse which drove the converter into negative saturation. The converter recovers in 354 nanoseconds after the end of saturation, within 5 LSB of its final value. We can model the A/D converter overvoltage recovery response as a simple RC circuit with a time constant of approximately 55 nanoseconds. It can be concluded from the analysis that the DDC converter does not meet the B2 overvoltage recovery requirement of 200 nanoseconds; a time constant of less than 30 nanoseconds would be required.

5.5 SUMMARY AND CONCLUSIONS OF TRANSIENT AND OVERVOLTAGE RECOVERY TESTS

Table 10 compares overvoltage and transient recovery characteristics of the DDC A/D converter and the ADC Unit 2. The characteristics of the DDC converter are better than those of the ADC converter currently in use; however, it does not meet the transient and overvoltage NWS B2 specifications. In this study, we did not evaluate the impact that this will have on the overall system performance. We recommend that the final step in the evaluation be to only reevaluate the impact that this will have on the NWS performance.

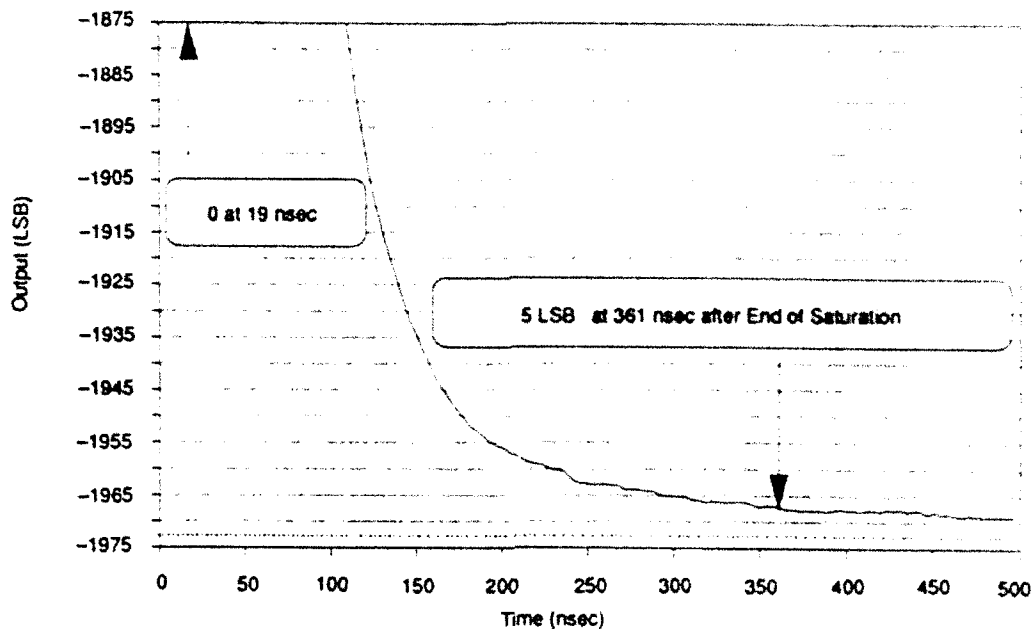


Figure 37. DDC A/D Converter Overvoltage Recovery Response from a +4.8V Pulse

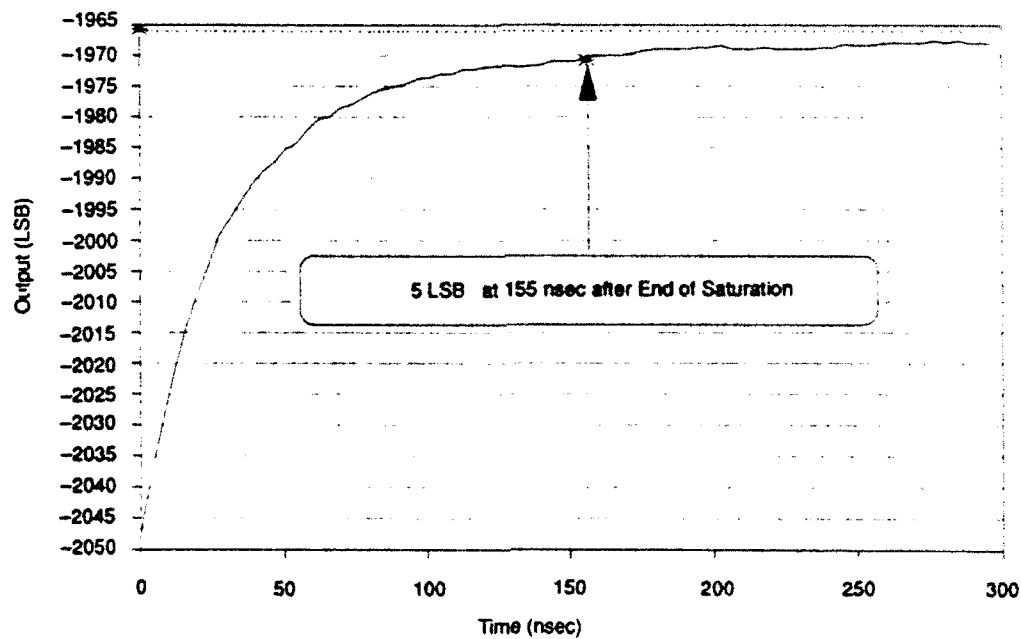


Figure 38. DDC A/D Converter Overvoltage Recovery Response from a -1.7V Pulse

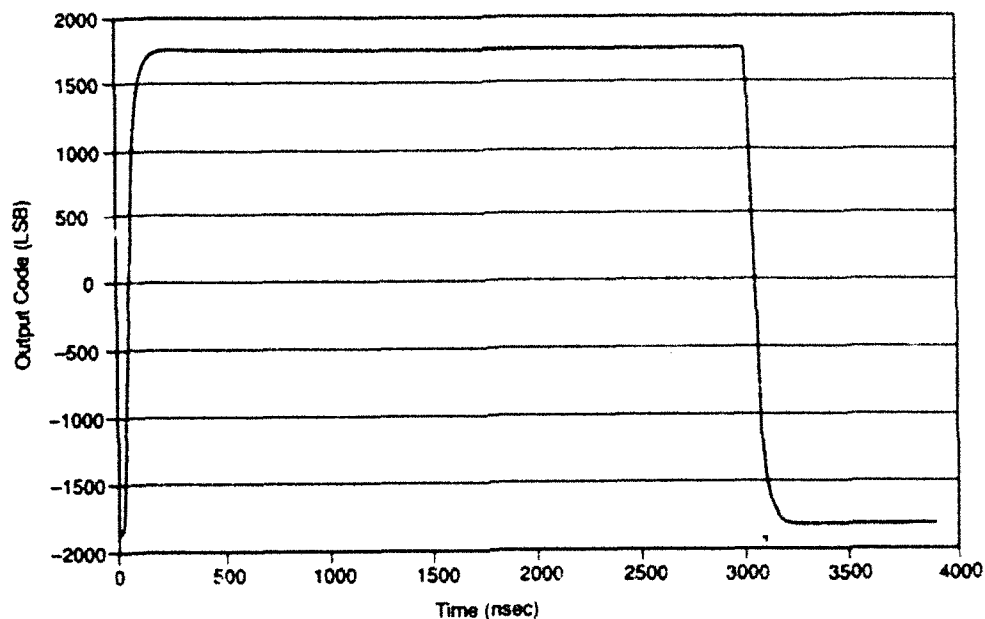


Figure 39. DDC A/D Converter Pulse Response with a Positive Base Voltage and a 1 μ sec Pulse of -3.5V

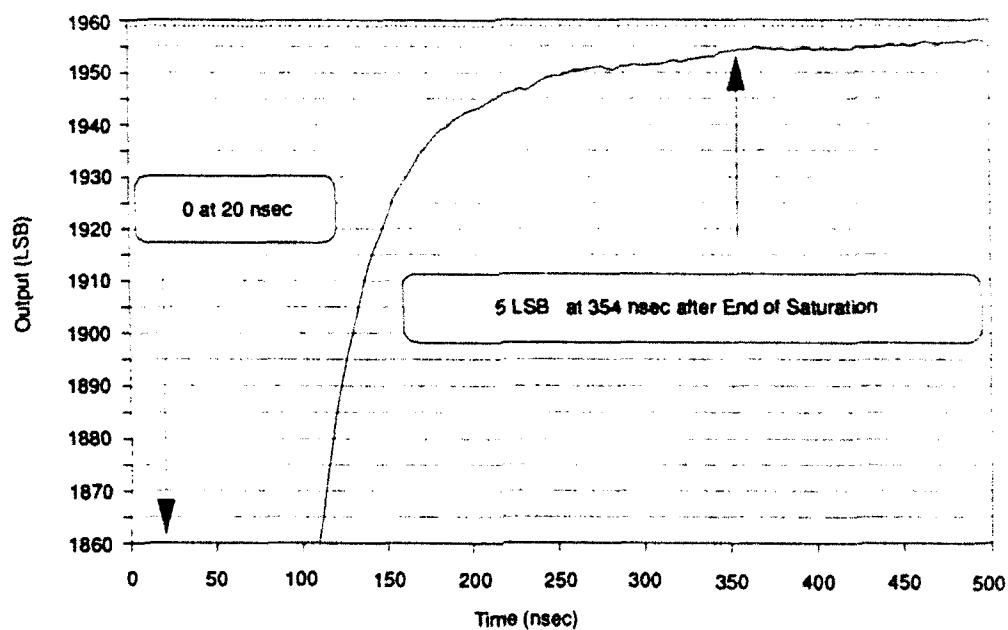


Figure 40. DDC A/D Converter Response When Recovering from a -4.4V Pulse

Table 10. Overvoltage and Transient Recovery Performance Comparison of Two A/D Converters for NWS

B2 Parameters	<u>A/D Converter Type</u>		
	<u>Specification</u>	<u>ADC</u>	<u>DDC</u>
Transient errors (in mV) (0.2 microsecond)	5	40	7
Overvoltage Recovery Error (in mV) (0.2 microsecond)	5	50	12
Transient recovery time to 5 LSB of its final value (in microseconds)	0.2	> 3	0.24 - 0.28
Overvoltage recovery time to 5 LSB of its final value (in microseconds)	0.2	> 3	0.34

LIST OF REFERENCES

1. "Critical Item Development Specification for the Receiver," Specification No. 1208990, 7 February 1986, Specification Change Notice No. 1 (SCM), 30 October 1989.
2. "Dynamic Performance Testing of the A/D Converter," HP Product Note, 1984, Hewlett Packard, Palo Alto, CA.
3. Asta, D., and F. H. Irons, 1989, "Dynamic Error Compensation of Analog-to-Digital Converters," *The Lincoln Laboratory Journal*, Vol. 2, No. 2, MIT Lincoln Laboratory, Lexington, MA.
4. Moulin, D., and B. N. Suresh Babu, 1991, "A/D Converter Characterization for High-Performance Signal Processing Applications," *International Conference on Analogue-to-Digital and Digital-to-Analogue Conversion*, University of Swansea, Wales, United Kingdom.
5. Jayant, N. S., and P. Noll, 1984, *Digital Coding of Waveforms*, Englewood Cliffs, NJ: Prentice-Hall.
6. Gersho, A., July 1978, "Principles of Quantization," *IEEE Transactions on Circuits and Systems*, Vol. CAS-25, No. 7, pp. 427-435.
7. Gordon, Bernard M., and the Analogic Engineering Staff, 1981, *The Analogic Data-Conversion Systems Digest*, Fourth Edition, Analogic Corporation, Wakefield, MA.
8. Suresh Babu, B. N., and C. M. Sorrentino, 1988, "Analog-to-Digital Converter Effects on Airborne Radar Performance," M88-48, The MITRE Corporation, Bedford, MA.
9. Suresh Babu, B. N., and C. M. Sorrentino, 1989, "Analog-to-Digital Converter Effects on Airborne Radar Performance," *IEEE AESS National Radar Conference*, Dallas, Texas.
10. Suresh Babu, B. N., and C. M. Sorrentino, 1992, "Analogue-to-Digital Converter Effects on Airborne Radar Performance," *IEEE Proceedings-F*, Vol. 139, No. 1.
11. Wollman, H. B., and B. N. Suresh Babu, "Phase-Plane Analysis of High-Speed A/D Converters with Sine Waves," *International Conference on Analogue-to-Digital and Digital-to-Analogue Conversion*, University of Swansea, Wales, United Kingdom.
12. Peetz, S. E., A. S. Muto, and J. M. Neil, 1982, "Measuring Waveform Recorder Performance," *HP Journal*, Vol. 33, No. 11, pp. 24, 25.

LIST OF REFERENCES (CONCLUDED)

13. Frothing, B. J., S. E. Peetz, M. A. Unrich, and S. C. Bird, 1988, "Waveform Recorder Design for Dynamic Performance," *HP Journal*, Vol. 39, No. 1, p. 48.

APPENDIX A
GENERALIZED SINE-WAVE ESTIMATION ALGORITHM

A.1 SINE-WAVE ESTIMATION ALGORITHM

Given samples of a waveform which is dominated by a sine wave with small additional harmonic distortion plus noise, it is desirable to develop an algorithm to estimate the signal and noise parameters [11]. We start with a set of N measurements, V_i , for $i = 1, 2, \dots, N$ of a waveform consisting of a large fundamental component, F_i , plus measurement errors and noise, e_i . The fundamental is determined by four parameters: the offset, M ; amplitude, A ; radian frequency, ω ; and initial phase, θ .

$$F_i = M + A \sin(\omega i + \theta) \quad i = 1, 2, \dots, N \quad (\text{A-1})$$

$$V_i = F_i + e_i \quad i = 1, 2, \dots, N \quad (\text{A-2})$$

where e_i is the error in each measurement caused by noise and the higher order harmonics. Given the V_i 's, we derive estimators for the four parameters of the fundamental, plus the root mean square (RMS) value of the measurement noise, e_i . We establish an initial approximation of the parameters, and then refine them by performing several iterations of an algorithm that minimizes the mean squared error. After iteration j , the parameter estimators are M_j , A_j , ω_j and θ_j . The speed and convergence of this iterative algorithm are dependent on the initial estimate.

A.1.1 Initial Estimates

The initial estimates of the offset and amplitude are obtained from the mean and standard deviations of the samples.

$$M_0 = \sum_{i=1}^N V_i / N \quad (\text{A-3})$$

$$A_0 = \sqrt{\frac{2}{N} \sum_{i=1}^N (V_i - M_0)^2} \quad (\text{A-4})$$

$$A_0 = \sqrt{\frac{2}{N} \sum_{i=1}^N (V_i - M_0)^2} \quad (\text{A-4})$$

Once the initial estimate of the offset is found, each of the data points is examined to determine whether it is above or below the offset. The first pair of data points which are on opposite sides of M_0 determines a pair of i values, iF and $iF + 1$. The rest of the data is scanned to determine NC , the number of complete signal cycles in the data record. The last offset crossing determines a pair of i values, iL and $iL + 1$. The pairs of data points can be linearly interpolated to find a zero order estimate of the time of the first and last offset crossings, $FIRST_0$ and $LAST_0$.

$$FIRST_0 = iF + \frac{V_{iF} - M_0}{V_{iF} - V_{iF+1}} \quad (\text{A-5})$$

$$LAST_0 = iL + \frac{V_{iL} - M_0}{V_{iL} - V_{iL+1}} \quad (\text{A-6})$$

The initial estimator for the radian frequency is ω_0 .

$$\omega_0 = 2\pi NC / (LAST - FIRST) \quad (\text{A-7})$$

The parameter estimates are then used to fit a segment of a sine wave through the pair of points surrounding the first offset crossing, and then to solve for the offset crossing of that sine wave, $FIRST_1$. In a similar manner, an improved estimate of the last offset crossing, $LAST_1$, is obtained. These improved crossing estimates are then used in equation (A-7) to obtain an improved estimate of the radian frequency ω_1 .

$$\begin{aligned}
FIRST_1 &= iF' + \omega_0 \sin^{-1} \left(\frac{|V_{iF'} - M_0|}{A_0} \right) \\
LAST_1 &= iL' + \omega_0 \sin^{-1} \left(\frac{|V_{iL'} - M_0|}{A_0} \right)
\end{aligned} \tag{A-8}$$

where

$$\begin{aligned}
iF' &= \begin{cases} iF & \text{for } |V_{iF} - M_0| \leq |V_{iF+1} - M_0| \\ iF+1 & \text{otherwise} \end{cases} \\
iL' &= \begin{cases} iL & \text{for } |V_{iL} - M_0| \leq |V_{iL+1} - M_0| \\ iL+1 & \text{otherwise} \end{cases}
\end{aligned} \tag{A-9}$$

The initial phase θ_1 is estimated from the requirement that the total phase angle at time $FIRST_1$ must be either 0 or π , depending upon the sign of the derivative of the signal.

$$\theta_1 = \begin{cases} \pi - \omega_1 FIRST & \text{for } V_{iF} > V_{iF+1} \\ -\omega_1 FIRST & \text{otherwise} \end{cases} \tag{A-10}$$

A.1.2 Estimation Iteration

Once the parameters of the signal are estimated, we calculate an estimator of the sine wave and the measurement errors of each data point. We then adjust the estimate to minimize the

errors. After the j th iteration, the estimate of the total signal is Y_{ji} , and the error in the estimate is E_{ji} , as given by

$$Y_{ji} = M_j + A_j \sin(\omega_j i + \theta_j) \quad (\text{A-11})$$

$$E_{ji} = Y_{ji} - V_i \quad i = 1, 2, \dots, N. \quad (\text{A-12})$$

Substituting equations (A-1) and (A-2) into (A-12) yields

$$E_{ji} = M_j - M + A_j \sin(\omega_j i + \theta_j) - A \sin(\omega i + \theta) - e_i \quad (\text{A-13})$$

Defining ΔM_j , ΔA_j , $\Delta \omega_j$, and $\Delta \theta_j$ as the errors in the parameter estimates after the j th iteration gives

$$\begin{aligned} \Delta M_j &= M_j - M, & \Delta A_j &= A_j - A, \\ \Delta \omega_j &= \omega_j - \omega, & \Delta \theta_j &= \theta_j - \theta. \end{aligned} \quad (\text{A-14})$$

Expanding equation (A-13) in terms of these errors and using the small-angle approximation for the sine of the phase errors results in the following:

$$E_{ji} \equiv \Delta M_j + \Delta A_j \sin(\omega_j i + \theta_j) + A_j (\Delta \omega_j i + \Delta \theta_j) \cos(\omega_j i + \theta_j) - e_i. \quad (\text{A-15})$$

Equation (A-15) shows that the error in estimating the fundamental can be approximated by an error in the offset, plus a sine wave that is proportional to the error in the amplitude, plus a

cosine wave that is proportional to the sine of the error in the total phase estimate. Calculating the direct current (dc) and fundamental terms of the discrete Fourier transform of Y_{ji} allows estimation of the error in the offset, amplitude, and average phase angle. To avoid introducing errors caused by the partial cycles at the end of the data record, the Fourier transform and correlation coefficient are evaluated only for the data points corresponding to NC full cycles, i.e., for $iF \leq i \leq iL$. We obtain an estimate for ΔM_j , ΔA_j , $\Delta \omega_j$, and $\Delta \theta_j$ from

$$\Delta M_j = \frac{1}{NP} \sum_{i=iF}^{iL} E_{ji} \quad (\text{A-16})$$

$$\Delta A_j = \frac{2}{NP} \sum_{i=iF}^{iL} E_{ji} \sin(\omega_j i + \theta_j) \quad (\text{A-17})$$

$$\Delta \omega_j = \frac{24}{A_j NP^3} \sum_{i=iF}^{iL} E_{ji} (i + \bar{i}) \cos(\omega_j i + \theta_j) \quad (\text{A-18})$$

$$\Delta \theta_j = \frac{24}{A_j NP} \sum_{i=iF}^{iL} E_{ji} \cos(\omega_j i + \theta_j) - \Delta \omega_j \bar{i} \quad (\text{A-19})$$

where the mean value of i is $\bar{i}$, and NP is the number of points.

$$\bar{i} = (iF + iL)/2 \quad (\text{A-20})$$

$$NP = iL - iF + 1 \quad (\text{A-21})$$

At each iteration, the estimate of the signal, Y_{ji} , and the error, E_{ji} , for each data point are calculated with equations (A-11) and (A-12). Equations (A-16) to (A-19) are used to evaluate the errors in the parameter estimators, which are then incremented.

This algorithm works remarkably well for most digitized waveforms. It rapidly converges to a good approximation of the fundamental, and the errors approach zero as j increases. The number of iterations required depends upon the desired accuracy, the signal frequency, and the noise and distortion; but mainly, it depends upon the number of data points. Computer simulations indicate that the results have converged in six iterations for a data record of 64 points, but only two iterations are needed for a data record 4096 points long.

After the sine-wave curve fit has converged, the RMS value of E_{ji} determines the signal-to-noise and distortion ratio of the A/D converter. The harmonic distortions can be computed via the Fourier transform. If these distortion terms are subtracted out, the remainder is the noise of the converter. If the noise squared is correlated with the square of the rate of change of signal voltage, i.e., $\cos^2(\omega i + \theta)$, the correlation coefficient is proportional to the total jitter in the A/D converter plus the test equipment. If the noise is correlated with $(i - \bar{i})^2$, it means that there is a small drift in the relative frequencies of the signal and clock oscillator during the test.

APPENDIX B
FORTRAN LISTING OF THE PROGRAM MONO

```

PROGRAM MONO
C
C   THIS PROGRAM FITS A CLIPPED COSINE WAVE TO 64K
MEASUREMENTS
C
  INTEGER*2 I1(512),Y(65536),YY(65536)
  INTEGER POINT,U,APPEAR1(4096),APPEAR2(4096)
  REAL V(65536),ANG2,PHI
  REAL VV(65536),SUM1(4096),SUM2(4096)
  REAL*8 ANG,DPI,DELTA,W,THETA
  REAL*8 ONE,EIGHT
  DIMENSION A(3,3),AINV(3,3),WKAREA(18)
  CHARACTER*4 LAST(9)
  CHARACTER*12 FNAME(9)
  CHARACTER*5 FILE,COMPANY
C   INITIALIZATION OF STATIC VARIABLES
  ONE=1.0
  EIGHT=8.0
  DPI=EIGHT*DATAN(ONE)
  NPNTS=65536
  HNPNTS=NPNTS/2
  NC=20481
  W=DPI*NC/NPNTS
  LAST(1)='.AS'
  LAST(2)='.DAT'
  LAST(3)='.64'
  LAST(4)='.MEA'
  LAST(5)='.CAL'
  LAST(6)='.D1'
  LAST(7)='.D2'
  LAST(8)='.ONE'
  LAST(9)='.ZER'
  COMPANY='DDC'
  DO I=1,4096
    APPEAR1(I)=0
    APPEAR2(I)=0
    SUM1(I)=0
    SUM2(I)=0
  ENDDO
C
C   OPEN(UNIT=1,FILE='DDC_FILES.DAT',STATUS='OLD')
C
C   READ IN DATA
C
5  READ(1,*,END=99)FILE
  WRITE(6,*)FILE

```

```

C
C      INITIALIZATION OF DYNAMIC VARIABLES
C
      TO=0
      TS=0
      TSS=0
      TC=0
      TCC=0
      TSC=0
      RO=0
      RS=0
      RC=0
      DC=0
      S=0
      C=0
      AMP=0
      PHI=0
      U=0
      DELTA0=0
      ANG=0
      B1=0
      B2=0
      M=0
      DO I=1,NPNTS
        V(I)=0
        VV(I)=0
        Y(I)=0
        YY(I)=0
      ENDDO
      DO J=1,512
        II(J)=0
      ENDDO
C
      FNAME(1)=FILE//LAST(1)
      FNAME(2)=FILE//LAST(2)
      FNAME(3)=FILE//LAST(3)
      FNAME(4)=FILE//LAST(4)
      FNAME(5)=FILE//LAST(5)
      FNAME(6)=FILE//LAST(6)
      FNAME(7)=FILE//LAST(7)
      FNAME(8)=FILE//LAST(8)
      FNAME(9)=FILE//LAST(9)
      OPEN(UNIT=71,FILE=FNAME(3),STATUS='OLD')
C      OPEN(UNIT=73,FILE=FNAME(1),STATUS='NEW',CARRIAGE
CONTROL='LIST')
      OPEN(UNIT=77,FILE=FNAME(2),STATUS='NEW')
      OPEN(UNIT=11,FILE=FNAME(4),STATUS='NEW')
C      OPEN(UNIT=12,FILE=FNAME(5),STATUS='NEW')

```

```

C
C   READ BINARY DATA IN FROM FILE
C   THIS READ FORMAT IS UTILIZED SINCE ORIGINAL DATA
C   IS IN DOS FORMAT

```

```

C
C   DO K=1,128
C       READ(71, '(512A2)') I1
C       DO I=1,512
C           M=(K-1)*512+I
C           Y(M)=I1(I)
C           IF (IABS(I1(I)) .LT. 2047) THEN
C               WRITE(73, *) I1(I)
C               PHI=M*W
C               B1=SIN(PHI)
C               B2=COS(PHI)
C               TO=TO+1
C               TS=TS+B1
C               TSS=TSS + B1*B1
C               TC=TC+B2
C               TCC=TCC + B2*B2
C               TSC=TSC+B1*B2
C               RO=RO+I1(I)
C               RS=RS+I1(I)*B1
C               RC=RC+I1(I)*B2
C           ELSE
C               ENDIF
C       ENDDO
C   ENDDO

```

```

C
C   THE FOLLOWING ROUTINE INVERTS A MATRIX
C

```

```

C   A(1,1)=TO
C   A(1,2)=TS
C   A(1,3)=TC
C   A(2,1)=TS
C   A(2,2)=TSS
C   A(2,3)=TSC
C   A(3,1)=TC
C   A(3,2)=TSC
C   A(3,3)=TCC
C   CALL LINRG(3,A,3,AINV,3)

```

```

C   CALCULATE DC, S AND C

```

```

C
C   DC=AINV(1,1)*RO+AINV(1,2)*RS+AINV(1,3)*RC
C   S= AINV(2,1)*RO+AINV(2,2)*RS+AINV(2,3)*RC
C   C= AINV(3,1)*RO+AINV(3,2)*RS+AINV(3,3)*RC

```

```

C

```

```

C   DETERMINE AMPLITUDE AND PHASE
C
AMP=(S**2+C**2)**0.5
IF (C .LT. 0) THEN
  PHI=ATAN(S/-C) + DPI/2.00
ELSE
  PHI=ATAN(-S/C)
ENDIF
C
C   FIND COSINE WAVE
C
DELTA=DPI/NPNTS
U=PHI/DELTA
DELTAO=PHI-U*DELTA
IF (U .LT. 1) U=NPNTS+U
C   WRITE(11,*)DELTAO
DO I=1,NPNTS
  U=U+NC
  IF (U .GT. NPNTS) U=U-NPNTS
  ANG=DELTA*U+DELTAO
  V(I)=DC+AMP*COS(ANG)
  YY(U)=Y(I)
  VV(U)=V(I)
C   WRITE(12,*)Y(I),V(I),U
ENDDO
C
DO U=1,NPNTS
  WRITE(11,*)YY(U),VV(U)
ENDDO
C
C   DETERMINE AVERAGE,SUM AND OCCURRENCE OF EACH
POINT
C   REAL RANGE IS FROM -2048 TO 2047. INDEX OF ARRAY IS
TO SERVE AS
C   THE SPECIFIC POINT THUS INDEX = POINT +2049 =>
INDEX(1,4096)
C   ALSO TWO LOOPS ARE SETUP TO DISTINGUISH BETWEEN
INCREASING
C   AND DECREASING DATA.
C
DO U=1,HNPNTS
  INDEX=YY(U)+2049
  APPEAR1(INDEX)=APPEAR1(INDEX)+1
  SUM1(INDEX)=SUM1(INDEX)+VV(U)
ENDDO
ISTART=HNNPNTS+1
DO U=ISTART,NPNTS
  INDEX=YY(U)+2049

```

```

        APPEAR2(INDEX)=APPEAR2(INDEX)+1
        SUM2(INDEX)=SUM2(INDEX)+VV(U)
ENDDO
C
C   DATA TO BE PRINTED TO FILE.DAT
C
WRITE(77,*)'COMPANY=',COMPANY
WRITE(77,*)'FILE=',FNAME(3)
WRITE(77,*)'TO=',TO
WRITE(77,*)'TS=',TS
WRITE(77,*)'TSS=',TSS
WRITE(77,*)'TC=',TC
WRITE(77,*)'TCC=',TCC
WRITE(77,*)'TSC=',TSC
WRITE(77,*)'RO=',RO
WRITE(77,*)'RS=',RS
WRITE(77,*)'RC=',RC
WRITE(77,*)'OUTPUT OF INVERTED MATRIX'
WRITE(77,*)AINV(1,1),AINV(1,2),AINV(1,3)
WRITE(77,*)AINV(2,1),AINV(2,2),AINV(2,3)
WRITE(77,*)AINV(3,1),AINV(3,2),AINV(3,3)
WRITE(77,*)'DC=',DC
WRITE(77,*)'S=',S
WRITE(77,*)'C=',C
WRITE(77,*)'AMPLITUDE=',AMP
WRITE(77,*)'PHI=',PHI
GOTO 5
C
C   PRINT OUT SUM, APPEARANCE AND AVERAGE FOR EACH
C   POINT
C
C   OPEN(UNIT=13,FILE=FNAME(6),STATUS='NEW')
C   OPEN(UNIT=14,FILE=FNAME(7),STATUS='NEW')
99  OPEN(UNIT=15,FILE=FNAME(8),STATUS='NEW')
   OPEN(UNIT=16,FILE=FNAME(9),STATUS='NEW')
   OPEN(UNIT=17,FILE='CODES1.DP6',STATUS='NEW')
   OPEN(UNIT=18,FILE='CODES2.DP6',STATUS='NEW')
   OPEN(UNIT=19,FILE='NARROW2.DP6',STATUS='NEW')
   OPEN(UNIT=20,FILE='V.IDE2.DP6',STATUS='NEW')
   ERROR1=0
   ERROR2=0
   DO I=1,4096
     POINT=I-2049
     IF (APPEAR1(I) .NE. 0) SUM1(I)=SUM1(I)/APPEAR1(I)
C     WRITE(13,*)POINT,APPEAR1(I),SUM1(I)
     IF (APPEAR2(I) .NE. 0) SUM2(I)=SUM2(I)/APPEAR2(I)
     ERROR1=SUM1(I)-POINT+ERROR1
     DIFF1=SUM1(I)-SUM1(I-1)

```

```

ERROR2=SUM2(I)-POINT+ERROR2
DIFF2=SUM2(I)-SUM2(I-1)
WRITE(17,*)POINT,DIFF1
WRITE(18,*)POINT,DIFF2
C   WRITE(17,*)POINT,SUM1(I),APPEAR1(I),SUM1(I)-POINT
C   WRITE(18,*)POINT,SUM2(I),APPEAR2(I),SUM2(I)-POINT
C   WRITE(14,*)POINT,APPEAR2(I),SUM2(I)

C   IF (APPEAR1(I) .EQ. 1) WRITE(15,*)1,POINT
C   IF (APPEAR2(I) .EQ. 1) WRITE(15,*)2,POINT
C   IF (APPEAR1(I) .EQ. 0) WRITE(16,*)1,POINT
C   IF (APPEAR2(I) .EQ. 0) WRITE(16,*)2,POINT
C   IF (I .NE. 1) THEN
C       CW1=SUM1(I)-SUM1(I-1)
C       CW2=SUM2(I)-SUM2(I-1)
C       IF (CW1 .LT. 0.1) THEN
C           WRITE(17,*) POINT, APPEAR1(I-1),SUM1(I-1),
C           &           APPEAR1(I),SUM1(I),
C           &           APPEAR1(I+1),SUM1(I+1)/APPEAR1(I+1)
C       ELSE
C           IF (CW1 .GT. 1.9) THEN
C               WRITE(18,*) POINT, APPEAR1(I-1),SUM1(I-1),
C               &           APPEAR1(I),SUM1(I),
C               &           APPEAR1(I+1),SUM1(I+1)/APPEAR1(I+1)
C           ENDIF
C       ENDIF
C   IF (CW2 .LT. 0.1) THEN
C       WRITE(19,*) POINT, APPEAR2(I-1),SUM2(I-1),
C       &           APPEAR2(I),SUM2(I),
C       &           APPEAR2(I+1),SUM2(I+1)/APPEAR2(I+1)
C   ELSE
C       IF (CW2 .GT. 1.9) THEN
C           WRITE(20,*) POINT, APPEAR2(I-1),SUM2(I-1),
C           &           APPEAR2(I),SUM2(I),
C           &           APPEAR2(I+1),SUM2(I+1)/APPEAR2(I+1)
C       ENDIF
C   ENDIF
C   ENDDO
ERROR1=ERROR1/4096
WRITE(17,*)'AVERAGE ERROR=',ERROR1
ERROR2=ERROR2/4096
WRITE(18,*)'AVERAGE ERROR=',ERROR2
CALL EXIT
END

```

APPENDIX C
STATISTICAL ANALYSIS

C.1 INTRODUCTION

For the ideal case of a noise-free analog-to-digital (A/D) converter, from $N = 512K$ collected data points we can determine the code edges of an M bit A/D converter to a resolution of $\pi 2^M / N = 0.03$ least significant bit (LSB). To analyze the data, we sort the observations in order of increasing input signal voltages, and then determine the largest and smallest input voltages corresponding to each possible output code. With this data reordering, a monotonic and noise-free A/D converter would produce a monotonic output code sequence.

For an A/D converter with internal noise, the problem of determining the differential nonlinearity and monotonicity is complicated, as illustrated in figures C-1, C-2, and C-3. For purposes of illustration, we consider an A/D converter with internal noise, and we assume that one of the code edges has an error. The nominal voltage of the lower edge of code 2 is +1.5 mVolts. However, we assume that code 2 has an error of -0.75 mVolt. The heavy line in figure C-1 shows the output code as a function of input signal voltage in the absence of noise. Code 1 is assumed to be narrow, with a width of only 0.25 LSB, while code 2 is assumed to be 1.75 LSB wide. If the internal noise of the A/D converter is assumed to be Gaussian-distributed, the probability that the output code, x , equals or exceeds i is given by

$$P[x \geq i] = F\left[\frac{V_{in} - V_i}{\sigma}\right] \quad (C-1)$$

where x = the output code,
 V_{in} = the input voltage,
 V_i = the lower code edge of code i
 σ = the RMS noise of the A/D converter, and
 F = the cumulative normal error function.

$$F[u] = \frac{1}{\sqrt{2\pi}} \int_{-\infty}^u e^{-z^2/2} dz \quad (C-2)$$

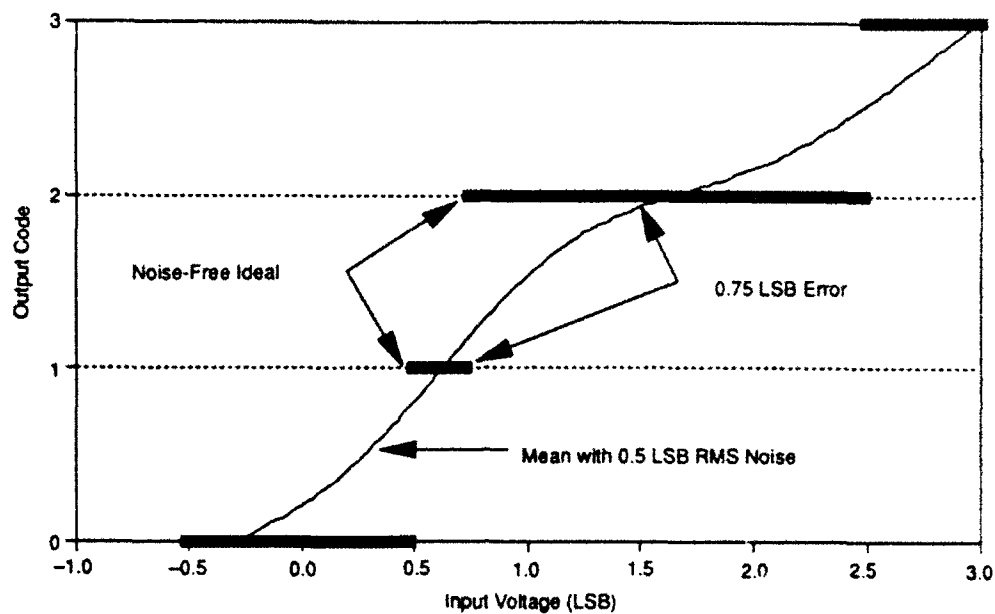


Figure C-1. Output Code vs. Input Voltage for an A/D Converter with 0.5 LSB Noise

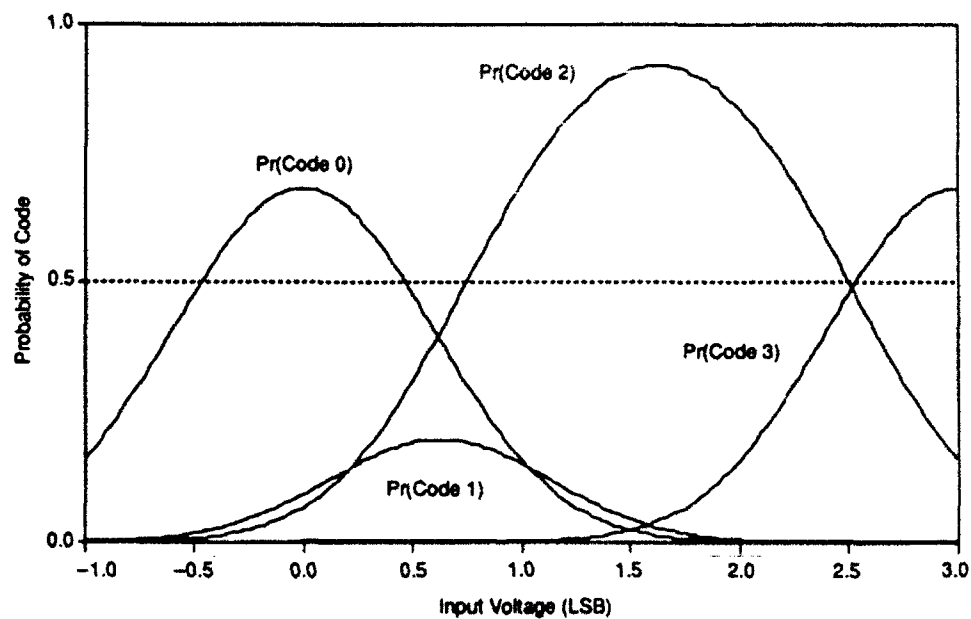


Figure C-2. Probability of Code vs. Input Voltage for an A/D Converter with 0.5 LSB Noise

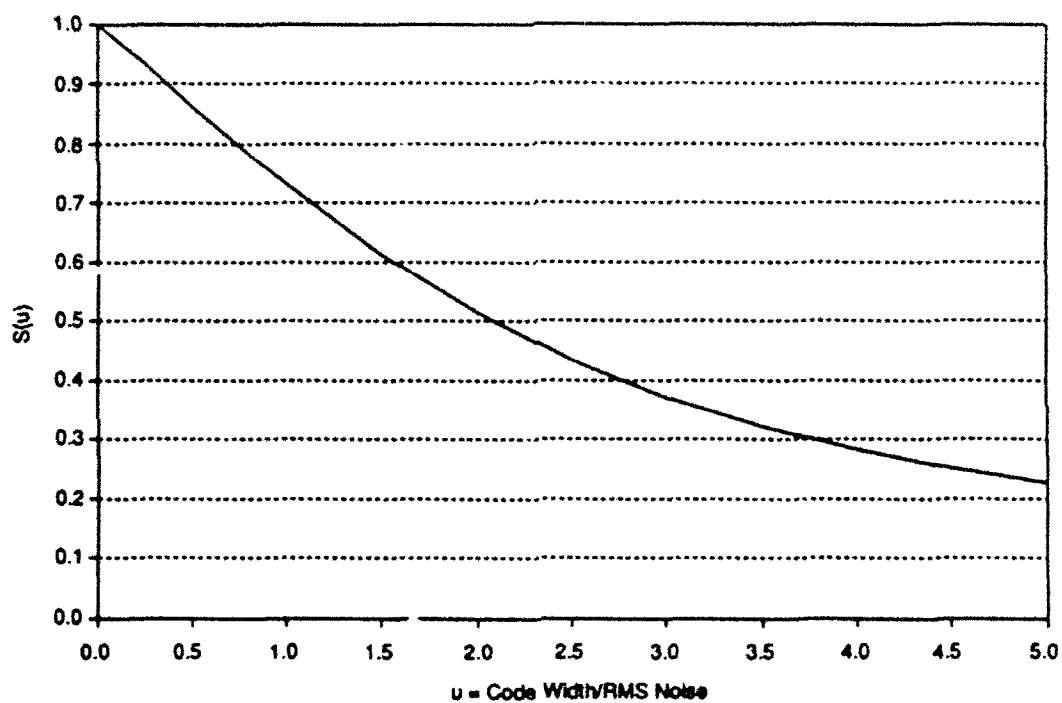


Figure C-3. Ratio of Variance to the Mean of the Occurrences
vs. Ratio of Code Width to Noise

The probability that the output code is i is

$$P[x = i] = P[x \geq i] - P[x \geq i + 1]. \quad (C-3)$$

Figure C-2 shows the probability of outputting various codes as functions of input voltage for the case where the root mean square (RMS) internal noise of the converter is 0.5 LSB. The probability density function of each code is a symmetrical bell-shaped curve, centered at the middle of the code. Codes of nominal width, such as codes 0 and 3 in the example, have a peak probability of 68 percent. Narrow codes have a lower probability, while wide codes have a higher probability and a flattened peak. From the probability functions shown in figure C-2, the expected value of the output code $E[x]$ over all input voltages, V_{in} , is calculated from

$$E[x] = \sum_{i=-2028}^{2047} i P[x = i]. \quad (C-4)$$

For each input voltage V_{in} , the expected or (mean) output code is given by

$$E[x] = \sum_{i=-2048}^{2047} i P[x = i \mid V = V_{in}] \quad (C-5)$$

where $\Pr[x = i \mid V = V_{in}]$ is the conditional probability of occurrence of code i , given the input voltage is V_{in} . The mean output is shown in figure C-1 as a thin line which is nearly straight, except for a slight bump caused by the assumed code-edge error.

The detailed derivation of the expected value and variance of the number of occurrences of code i in a sample of size N of input voltages V_{in} is described in the following sections (written by J. E. Kriegel). The analysis reveals that the expected value of the number of occurrences of code i , $E[H_i]$ is equal to the density of input samples (D in samples/LSB) times the code width ($V_{i+1} - V_i$).

$$E[H_i] = D (V_{i+1} - V_i). \quad (C-6)$$

The variance of the number of occurrences will depend upon the expected value (of the number of occurrences) and the ratio of code width to noise. Let u denote the ratio of code width to noise and $S(u)$ denote the ratio of the variance to the mean of occurrences.

Figure C-3 shows a plot of $S(u)$ versus u .

From the spectral analysis test we determined that the Data Device Corporation (DDC) A/D converter has an RMS random noise of approximately 0.5 LSB. Hence, for any given input voltage the output code can vary randomly over a small range. As a result of the random noise, the data analysis employed, which is based upon statistical methods, will be less precise than for the noise-free case, and will have an associated confidence level of less than 100 percent. The values of code centers and edges calculated from this analysis will have a standard deviation on the order of 0.1 LSB. In our analysis we are calculating 8 K code widths (4 K each for positive- and negative-going signals), half of which are only based on 38 to 50 observations. From this analysis it can be concluded that one or more calculated values of code width may be in error by up to 0.4 or 0.5 LSB.

C.2 STATISTICAL ANALYSIS: THE LOCKED HISTOGRAM TEST METHOD

In the locked histogram test method for an A/D converter, the input sample voltages are derived from a cosine input and form a predetermined set of values in which there is a constant (locked) phase difference between consecutive values. For each input voltage, the converter produces an output code; and for an input set of voltages, a histogram of the number of occurrences of each code can be created. This histogram depends not only on the range and number of input voltages, but also on the design and internal noise of the converter.

C.2.1 INPUT SAMPLE

To evaluate the device, an input sample of N ($= 2^{16}$ say) voltages, V_{in} , is produced by the phase-locked system

$$V_{in} = V_o \cos(\alpha + n 2 \pi / N), \alpha \text{ constant, } n = 0, 1, \dots, N-1. \quad (C-7)$$

A value of $V_o = 2.171$ volts is used in the test. It is assumed that input samples of size N are created; the phase difference between consecutive values of V_{in} in any of the samples is locked at $2 \pi / N$. Without the phase-lock feature, any sample of size N should be regarded as arising from a random process. One such process is

$$V_{in} = V_o \cos(\phi) \quad (C-8)$$

where ϕ is uniformly distributed on $[0, 2 \pi]$.

C.2.2 OUTPUT AND THE A/D CONVERTER

For each input voltage, V_{in} , the A/D converter outputs an integer value (a code) in the range $[-2048, 2047]$. For a particular fixed voltage repeatedly input to the converter, the output code value may vary due to internal noise which is characterized by σ , the RMS noise voltage. The probability of obtaining an output code value $x = i$ for a particular input V_{in} is written

$$P[x = i \mid V_{in}] \quad (C-9)$$

in which V_{in} is to be regarded as an index associated with a particular value of an input voltage. The accepted model for equation (C-2) is

$$\begin{aligned}
P[x = i \mid V_{in}] &= P[x \geq i \mid V_{in}] - P[x \geq i + 1 \mid V_{in}] \\
&= \frac{1}{\sqrt{2} \pi} \int_A^B e^{-t^2/2} dt
\end{aligned} \tag{C-10}$$

where $A = \frac{V_{in} - V_{i+1}}{\sigma}$, $B = \frac{V_{in} - V_i}{\sigma}$ and V_i = the lower code-edge voltage for code i .

Note that V_i has the property that

$$P[x \geq i \mid V_{in} = V_i] = 0.5.$$

It is convenient to assume in this analysis that the initial voltage phase α is zero. The value of α does not play a significant role, and the algebra is significantly reduced for $\alpha = 0$. With $\alpha = 0$, and introducing $\omega = \frac{2\pi}{N}$,

$$\begin{aligned}
A &= A(n \omega) = \frac{1}{\sigma} \{V_O \cos(n \omega) - V_{i+1}\} \\
B &= B(n \omega) = \frac{1}{\sigma} \{V_O \cos(n \omega) - V_i\}
\end{aligned} \tag{C-11}$$

where $V \equiv V_{in} = V_O \cos(n \omega)$, $n = 0, 1, \dots, N - 1$.

C.3 THE OUTPUT CODE HISTOGRAM

The (expected) value $E(i)$ of the histogram height at output code i for repetitions of the input sample of voltages is given by

$$E(i) = \sum_{V_{in}} P[x = i | V_{in}]$$

$$\sum_{n=0}^{N-1} \frac{1}{\sqrt{2\pi}} \int_A^B e^{-t^2/2} dt. \quad (C-12)$$

Setting $H(n\omega) = \frac{1}{\sqrt{2\pi}} \int_A^B e^{-t^2/2} dt$, which is a well-behaved function of $n\omega$,

$$\begin{aligned} E(i) &= \sum_{n=0}^{N-1} H(n\omega) \\ &= \frac{1}{\omega} \sum_{n=0}^{N-1} H(n\omega) \omega \\ &= \frac{N}{2\pi} \sum_{n=0}^{N-1} H(n\omega) \omega. \end{aligned} \quad (C-13)$$

From the definition of a definite integral,

$$\int_0^{2\pi} H(\theta) d\theta = \lim_{N \rightarrow \infty} \sum_{r=0}^{N-1} H(\theta_r) (\theta_{r+1} - \theta_r) \quad (C-14)$$

in which $0 = \theta_0 < \theta_1 \dots < \theta_N = 2\pi$ and $\max_{r=0}^{N-1} (\theta_{r+1} - \theta_r) \rightarrow 0$ as $N \rightarrow \infty$, it follows that, to significant accuracy,

$$E(i) = \frac{N}{2\pi} \int_0^{2\pi} H(\theta) d\theta \quad (C-15)$$

since " θ_r " = $r \omega$, " $\theta_{r+1} - \theta_r$ " = ω , and N is large. Hence,

$$\begin{aligned}
 E(i) &= \frac{N}{\pi} \int_0^\pi \frac{1}{\sqrt{2\pi}} \int_{A(\theta)}^{B(\theta)} e^{-t^2/2} dt d\theta \\
 &= \frac{N}{\pi} \int_{-V_0}^{V_0} \left\{ \frac{1}{\sqrt{2\pi}} \int_{\frac{V-V_{i+1}}{\sigma}}^{\frac{V-V_i}{\sigma}} e^{-t^2/2} dt \right\} \frac{1}{\sqrt{V_0^2 - V^2}} dV.
 \end{aligned} \tag{C-16}$$

Since the interior integral is the difference of two error functions, the interior integral is zero for $V > V_{i+1} + k\sigma$; and $V < V_i - k\sigma$, for $k \geq 5$.

Hence,

$$\begin{aligned}
 E(i) &= \frac{N}{\pi} \int_{-V_0}^{V_0} \left\{ \frac{1}{\sqrt{2\pi}} \int_{\frac{V-V_{i+1}}{\sigma}}^{\frac{V-V_i}{\sigma}} e^{-t^2/2} dt \right\} \frac{1}{\sqrt{V_0^2 - V^2}} dV \\
 &= \frac{N}{\pi} \int_{V_i - k\sigma}^{V_{i+1} + k\sigma} \left\{ \frac{1}{\sqrt{2\pi}} \int_{\frac{V-V_{i+1}}{\sigma}}^{\frac{V-V_i}{\sigma}} e^{-t^2/2} dt \right\} \frac{1}{\sqrt{V_0^2 - V^2}} dV;
 \end{aligned} \tag{C-17}$$

and by the use of a standard mean-value theorem for integrals of products of functions,

$$E(i) = \frac{N}{\pi} \int_{V_i - k\sigma}^{V_{i+1} + k\sigma} \left\{ \frac{1}{\sqrt{2\pi}} \int_{\frac{V-V_{i+1}}{\sigma}}^{\frac{V-V_i}{\sigma}} e^{-t^2/2} dt \right\} K_i dV \tag{C-18}$$

where

$$\min_V \frac{1}{\sqrt{V_o^2 - V^2}} \leq K_i \leq \max_V \frac{1}{\sqrt{V_o^2 - V^2}} \text{ for } V_i - k\sigma \leq V \leq V_{i+1} + k\sigma. \quad (\text{C-19})$$

Note that since $V_o \sim 2$ volts and σ and $V_{i+1} - V_i$ are of the order of a few millivolts, for a given i , K_i is essentially constant. Equation (C-6) can then be written as

$$E(i) = N \frac{K_i}{\pi} \int_{-\infty}^{\infty} \left\{ \frac{1}{\sqrt{2}\pi} \int_{\frac{V-V_{i+1}}{\sigma}}^{\frac{V-V_i}{\sigma}} e^{-t^2/2} dt \right\} dV. \quad (\text{C-20})$$

Introducing $\Delta = \frac{V_{i+1} - V_i}{\sigma}$, and the linear substitutions

$$z = \frac{V}{\sigma}, \quad U = z - \frac{V_i}{\sigma},$$

$$E(i) = N \sigma \left[\frac{K_i}{\pi} \int_{-\infty}^{\infty} \left\{ \frac{1}{\sqrt{2}\pi} \int_{U-\Delta}^U e^{-t^2/2} dt \right\} dU \right]. \quad (\text{C-21})$$

The double integral in the square brackets is a function of Δ only. Omitting the details, the integral can be shown to have the value $\frac{K_i}{\pi} \Delta$ by reversing the order of integration so that

$$E(i) = N \sigma \frac{K_i}{\pi} \Delta = N \frac{K_i}{\pi} (V_{i+1} - V_i). \quad (\text{C-22})$$

This gives substance to the qualitative statement that the probability of occurrence of code i is given by the code density times the code width.

C.3.1 THE VARIANCE ASSOCIATED WITH $E(i)$

The variance $G(i)$ associated with $E(i)$ is given by

$$E(i) = \sum_{V_{in}} P[x=i \mid V_{in}] (1 - P[x=i \mid V_{in}]) \quad (C-23)$$

Following the methods given in section C-3,

$$\begin{aligned} G(i) &= E(i) - N \sigma \frac{K'_i}{\pi} \left[\int_{-\infty}^{\infty} \left\{ \frac{1}{\sqrt{2\pi}} \int_{U-\Delta}^U e^{-t^2/2} dt \right\}^2 dU \right] \\ &= E(i) - N \sigma \frac{K_i}{\pi} I \end{aligned} \quad (C-24)$$

where K'_i and K_i are essentially equal. Note that the integral I in square brackets is a function of Δ only. By differentiating I with respect to Δ , it can be shown that

$$\frac{dI}{d\Delta} = \text{erf}\left(\frac{\Delta}{2}\right) \text{ where } \text{erf}(s) = \frac{2}{\sqrt{\pi}} \int_0^s e^{-u^2/2} du \quad (C-25)$$

and it follows that

$$I = \Delta \text{erf}\left(\frac{\Delta}{2}\right) + \frac{2}{\sqrt{\pi}} e^{-\Delta^2/4} - \frac{2}{\sqrt{\pi}}, \quad (C-26)$$

the constant term being obtained by numerical integration of the integral.¹ For $\Delta > 10$, for example, it is found that $I \sim \Delta - \frac{2}{\sqrt{\pi}}$; hence,

¹ R. L. Fante is gratefully acknowledged for providing an alternative direct method of evaluating I .

$$\begin{aligned}
\frac{E(i)}{N} &= \sigma \frac{K_i}{\pi} \Delta, \Delta = \frac{V_{i+1} - V_i}{\sigma} \\
\frac{G(i)}{N} &= \sigma \frac{K_i}{\pi} \Delta - \sigma \frac{K_i}{\pi} I \\
&= \sigma \frac{K_i}{\pi} \Delta - \sigma \frac{K_i}{\pi} \left(\Delta - \frac{2}{\sqrt{\pi}} \right) \Delta > 10 \\
&= \sigma \frac{K_i}{\pi} \frac{2}{\sqrt{\pi}}, \Delta > 10
\end{aligned} \tag{C-27}$$

So $G(i)$ is independent of Δ for Δ large.

C.4 RESULTS

The ratio $\frac{G(i)}{E(i)}$, referred to in the reference as $S(u)$, $u \equiv \Delta$, is given by $S(\Delta) = 1 - \frac{I}{\Delta}$ from equation (C-26).

Behavior of S as $\Delta \rightarrow 0$

Using L' Hospital's rule, $\lim_{\Delta \rightarrow 0} \frac{I}{\Delta} = \lim_{\Delta \rightarrow 0} \frac{\frac{dI}{d\Delta}}{1} = 0$, so that $S(\Delta) \rightarrow 1$ as $\Delta \rightarrow 0$.

Behavior of S as $\Delta \rightarrow \infty$

From equation (C-27) for $\Delta > 10$,

$$S(\Delta) = \frac{2}{\sqrt{\pi}} \frac{1}{\Delta} \rightarrow 0 \text{ as } \Delta \rightarrow \infty. \tag{C-28}$$

Behavior of the "normalized variance" $\Delta S(\Delta)$ as $\Delta \rightarrow \infty$

$$\begin{aligned}\Delta S(\Delta) &\equiv \Delta \frac{G(i)}{E(i)} \\ &= \Delta \left(\frac{2}{\sqrt{\pi}} \frac{1}{\Delta} \right) \text{ for } \Delta > 10 \\ &= \frac{2}{\sqrt{\pi}} \text{ independent of } \Delta \text{ for } \Delta \text{ large.}\end{aligned}\tag{C-29}$$

The value of $\Delta S(\Delta)$ obtained by simulation for Δ large was 1.13, which is the value of $\frac{2}{\sqrt{\pi}}$.

C.5 EXTENSION FOR NON-PHASE-LOCKED SAMPLES

In other test regimes, similar large input voltage samples are used in which the phase values (and, hence, phase differences) are not deterministically specified. Often the samples are produced by the process

$$V_{in} = V_o \cos(\phi)\tag{C-30}$$

where ϕ is uniformly distributed on $[0, 2\pi]$. The above analysis is easily modified to include such random input samples, and results are consistent with details published in the literature. The additional analysis is omitted here.

C.6 CONCLUSIONS

This appendix presents a general analysis for analyzing the statistics of narrow and wide code widths using the locked histogram test method. Estimates of the mean and variance of

the code widths are dependent on a number of variables which include input sample size as well as the RMS value of the noise voltage of the A/D converter.

The above analysis shows that when the code width is significantly smaller than the noise RMS value, the ratio of the variance and expected mean of the histogram height for an output code approaches 1. However, when the code width is much larger than the RMS noise voltage, this ratio behaves like $\frac{2}{\sqrt{\pi}} \left(\frac{1}{\text{code width}} \right)$. For this method of testing, increasing the size of the input sample does not change the results. However, if the size sample is too small it will not produce results with any significance. The method is general and can be extended to other well-behaved input waveforms.

GLOSSARY

ACRONYMS

ac	alternating current
A/D	analog-to-digital
ADC	Analog Devices Corporation
D/A	digital-to-analog
dc	direct current
DDC	Data Device Corporation
FFT	fast Fourier transform
LSB	least significant bit(s)
Mwords	megawords
NWS	North Warning System
PC	personal computer
RC	resistor-capacitor
RMS	root mean square
SFDR	spurious-free dynamic range
SINAD	signal-to-noise-and-distortion ratio
SNR	signal-to-noise ratio
TTL	transistor-transistor logic
UAR	Unattended Radar