AD-A264 992

JMENTATION PAGE

Form Approved
OMB No. 0704-0188

2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
February 1993	Professional Paper

4. TITLE AND SUBTITLE

BIPOLAR JUNCTION TRANSISTORS FABRICATED IN SILICON-ON-SAPPHIRE

5. FUNDING NUMBERS

In House Funding

6. AUTHOR(S)

E. N. Cartagena, B. Offord, and G. Garcia

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Naval Command, Control and Ocean Surveillance Center (NCCOSC)
RDT&E Division
San Diego, CA 92152–5001

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING/MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Naval Command, Control and Ocean Surveillance Center (NCCOSC)
RDT&E Division
San Diego, CA 92152–5001

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION/AVAILABILITY STATEMENT

Approved for public release; distribution is unlimited.

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 words)*

The effects of processing temperature on collector leakage current in bipolar junction transistors (BJTs) fabricated in silicon-on-sapphire (SOS) were examined. At low process temperatures (850°C) a reduction of five orders of magnitude in the collector leakage current was observed. Excellent I–V characteristics were obtained on both NPN and PNP transistors fabricated at lower temperatures. Measured DC current gain β for the NPN devices was 30, and that of the PNP devices was 40. Additionally, current mode logic (CML) circuits fabricated using these transistors exhibited well behaved DC switching characteristics.

Published in *Electronics Letters*, 21 May 1992, Vol 28. No. 11.

14. SUBJECT TERMS

bipolar junction transistors (BJTs)
silicon-on-sapphire (SOS)

15. NUMBER OF PAGES

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	UNCLASSIFIED	UNCLASSIFIED	SAME AS REPORT

21a. NAME OF RESPONSIBLE INDIVIDUAL	21b. TELEPHONE (Include Area Code)	21c. OFFICE SYMBOL
E. N. Cartagena	(619) 553-5501	Code 554

through the computer simulations that this scheme can provide constant switching frequency and smaller current

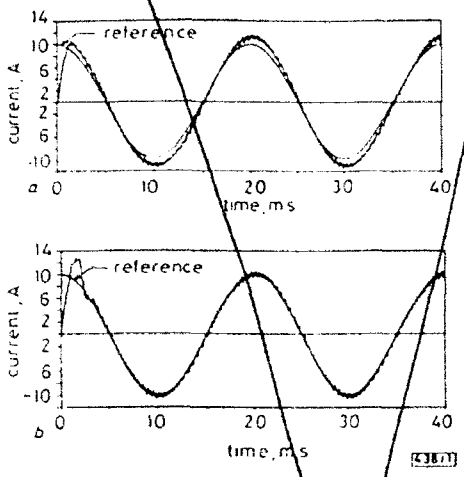

Fig. 1 *Response to step change of reference circuit when $e_a = 50 \cos(100\pi t)$ [V]*
a Predictive current control
b Proposed current control

current control schemes are compared with respect to the sampling periods as shown in Fig. 2. It can be noted that the error of the proposed scheme varies slightly for the large variations in load parameters. Moreover, the current error of the proposed scheme is reduced more rapidly than that of the predictive control scheme as the sampling period is decreased.

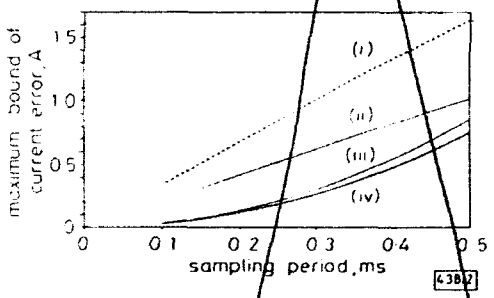

Fig. 2 *Variations of lub $\{\|\Delta i(k)\|\}$ with respect to sampling period*
(i) predictive ($e_a = 50 \cos(100\pi t)$ [V])
(ii) proposed ($e_a = 50 \cos(100\pi t)$ [V])
(iii) predictive ($e_a = 60 \cos(100\pi t)$ [V])
(iv) proposed ($e_a = 60 \cos(100\pi t)$ [V])

Conclusions: A current control scheme with reference voltage estimation for a voltage-fed PWM inverter is proposed. Information on EMF is not required in this scheme. It is shown error than the predictive control scheme with the same switching frequency when the load parameters are mismatched.

18th March 1992

J. W. Jung, K. Y. Cho, D. S. Oh and M. J. Youn (*Department of Electrical Engineering, Korea Advanced Institute of Science & Technology, 373-1, Kusong-Dong, Yusung-Gu, Taejon, 305-701, Korea*)

References

1 OH, D. S., and YOUN, M. J.: 'Automated adaptive hysteresis current control for a voltage-fed PWM inverter', *Electron Lett.*, 1990, **26**, pp. 2044–2046
2 HUY, H. L., and DESSAINT, L. A.: 'An adaptive current control scheme for PWM synchronous motor drives: analysis and simulation', *IEEE Trans.*, 1989, **PRE-4**, pp. 486–495
3 BOWES, S. R., and DAVIES, T.: 'Microprocessor-based development system for PWM variable-speed drives', *IEE Proc. B*, 1985, **132**, (1), pp. 38–45

BIPOLAR JUNCTION TRANSISTORS FABRICATED IN SILICON-ON-SAPPHIRE

E. N. Cartagena, B. Offord and G. Garcia

Indexing terms: Bipolar devices, Transistors, Semiconductor devices and materials

The effects of processing temperature on collector leakage current in bipolar junction transistors (BJTs) fabricated in silicon-on-sapphire (SOS) were examined. At low process temperatures (850°C) a reduction of five orders of magnitude in the collector leakage current was observed. Excellent I–V characteristics were obtained on both NPN and PNP transistors fabricated at lower temperatures. Measured DC current gain β for the NPN devices was 30, and that of the PNP devices was 40. Additionally, current mode logic (CML) circuits fabricated using these transistors exhibited well behaved DC switching characteristics.

Introduction: Advances in silicon-on-sapphire (SOS) processing have increased the lifetime of the material as well as reducing microtwin defects and stacking faults. Processing techniques such as lowering the epitaxy-growth temperature, growing layers on heavily phosphorus-doped layers [1] and using arsenic-doped films [2] have resulted in higher lifetime and therefore lower junction leakage current, in SOS films. The development of double-solid-phase-epitaxy (DSPE) [3] has improved the crystal quality by eliminating the propagation of microtwins and stacking faults which contribute to emitter to collector shorts in bipolar devices. These improvements in processing techniques have made SOS a desirable candidate material for bipolar junction transistors (BJTs).

BJTs in SOS have several distinct advantages over their bulk counterparts. Total isolation between devices can be obtained by etching Si islands into the sapphire substrate. Because the devices are fabricated on an insulating substrate, there is a reduction in collector to substrate capacitance which may give rise to a 12% decrease in ECL gate delay [4]. Because devices are completely isolated from each other, there is no possibility of latch-up. Also, all interconnecting lines are on the insulating substrate, thereby contributing little parasitic capacitance and allowing high-voltage and high-frequency components in close proximity [5]. Additionally, devices fabricated in SOS have shown that radiation-induced photocurrents are three orders of magnitude lower than in bulk silicon, making for a very radiation hard technology [6].

Most of the development of BJTs on SOS has been restricted to lateral BJT devices [7] and epitaxia. BJTs [8]. We report the successful fabrication of vertical diffused NPN and PNP BJTs fabricated in SOS. We have used all implanted base and emitter regions and we compare high-temperature emitter anneals against low-temperature emitter anneals and examine their effect on the resultant device behaviour.

Fabrication: The SOS wafers used had a diameter of 100 mm with an initial intrinsic thickness of 2700 Å. The material was improved by using DSPE techniques to obtain high quality transistors. The initial step in the DSPE process is amorphisation of the silicon at the silicon–sapphire interface. This was accomplished using an implant of Si^{28} at an energy of 185 KeV and a dose of 6×10^{14} ion/cm^2. An anneal in N_2 recrystallised the silicon using the upper layer of silicon as a seed. The second step in the DSPE process is amorphisation of the silicon at the surface accomplished by using a shallow implant of Si^{28} at an energy of 100 KeV and a dose of 10^{15} ion/cm^2. A final anneal in N_2 recrystallised the silicon surface using the bottom layer as a seed thus completing the DSPE process.

Half the wafers were used for NPN devices, the other half for PNP devices. To reduce collector series resistance a buried layer was implanted into the 2700 Å intrinsic silicon material. For the NPN devices the buried layer was formed by ion implantation of phosphorus at 80 KeV with a dose of 3×10^{15} ion/cm^2. The PNP buried layer was formed using a boron implantation at 30 KeV with a dose of 1.5×10^{15} ion/cm^2 followed by another boron dose of 1.5×10^{15} ion/cm^2 at 70 KeV. The NPNs and PNPs were then annealed in separate

furnaces in an N_2 ambient. Subsequently, a 3·0 μm *n*-type epitaxial layer with a nominal doping density of 10^{16} ion/cm^3 was grown on the NPN wafers. Similarly, a 3·0 μm epitaxial *p*-type layer with a nominal doping density of 10^{15} ion/cm^3 was grown on the PNP wafers.

After epitaxial deposition the devices were isolated using a potassium hydroxide etch which removed all silicon between devices. Variations in implant doses and anneal temperatures provided an adequate test matrix in which to analyse temperature-related effects on these devices. The temperatures chosen for the emitter anneal were 850 and 950°C. The implant doses were 5×10^{12} ion/cm^2, 10^{12} ion/cm^2 and 2×10^{12} ion/cm^2. After the implants and emitter anneals, a 5000 Å low temperature oxide was deposited and densified. A metal interconnect using titanium and Al/1%Si provided adequate step coverage and minimised spiking into the narrow emitter junctions.

Results: DC characteristics were measured on NPN and PNP devices with a $1 \times 8\,\mu m^2$ emitter. Measured Gummel plots for NPN devices, shown in Fig. 1, and PNP devices, shown in Fig. 2, display the DC bipolar behaviour. Fig. 1 shows an

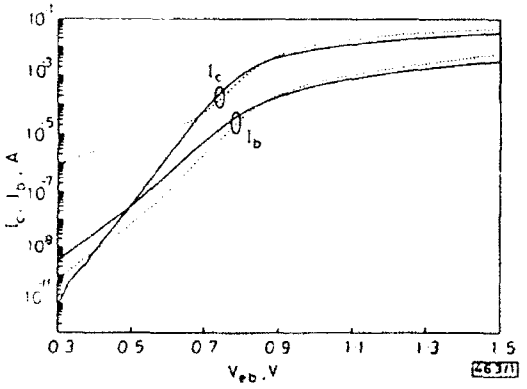

Fig. 1 *Gummel characteristics for NPN transistor with varying emitter anneals*

——— 850°C
- - - - 950°C

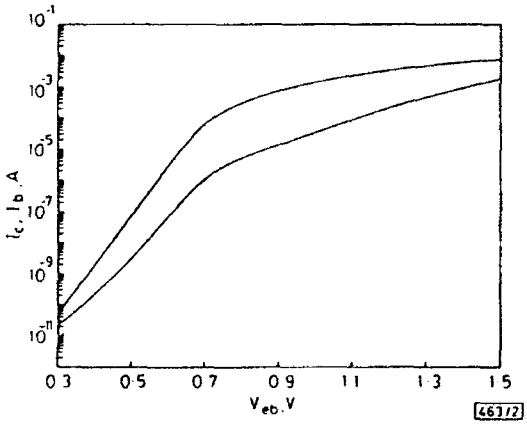

Fig. 2 *Gummel characteristics for PNP transistor with 850°C emitter anneal*

NPN transistor processed at 850°C, device NPN1, superimposed over that of one processed at 950°C, device NPN2. Device NPN2 exhibits five orders of magnitude higher collector leakage current than device NPN1. However, it should be noted that the base current in device NPN1 exhibits higher recombination than device NPN2, as evidenced by the shallower slope of NPN1 at base–emitter voltages less than 0·6 V. This effect is most likely due to the lower processing temperature of device NPN1. The anneal time at 850°C was not long enough to anneal the damage caused by the base and emitter implants. To maintain high current gain and low collector leakage while decreasing the recombination rate, an optimum anneal temperature–time relationship must be developed. The measured current gain for the NPN devices is 80 and that of the PNP devices is 40.

Fig. 3 demonstrates a current mode logic (CML) inverter transfer curve fabricated using NPN transistors from this

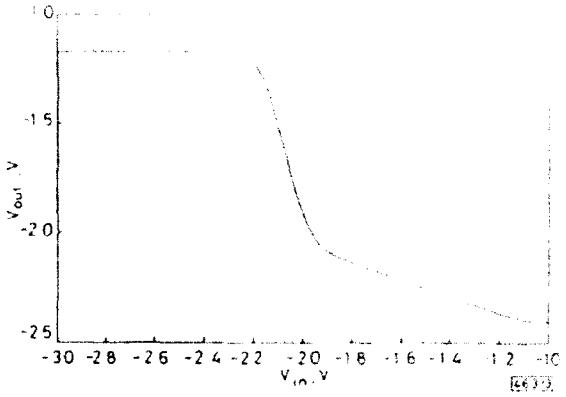

Fig. 3 *Current mode logic transfer curve for inverter fabricated with NPN devices*

process. The transfer curve shows excellent DC transfer characteristics, with a 200 mV input signal driving the output from −1·2 V to −2·2 V indicative of the proper current steering mechanism that is behind CML circuits.

AC measurements were made on NPN transistors with a network analyser. f_t values were obtained for collector current I_c variations of 10, 20, 30, 40, and 50 μA. Collector current variations above this amount could not be performed using these particular test structures without significant damage to the test devices. The data for f_t against I_c are shown in Fig. 4. It can be seen from Fig. 4 that the f_t at 50 μA is 2·1 GHz. However, the curve appears to be on an upward slope and the maximum f_t value is not reached within this set of data.

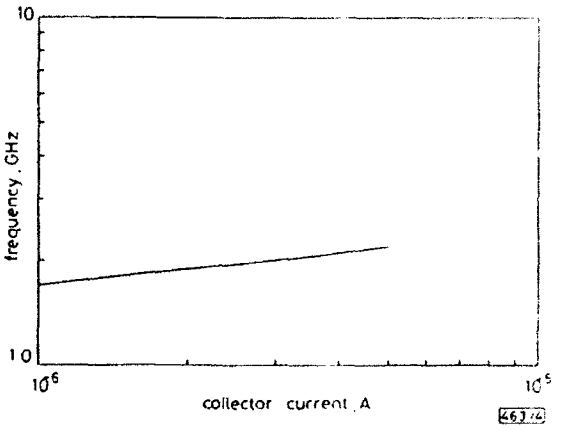

Fig. 4 *Frequency characteristics for NPN transistor*

Conclusions: It has been shown that by using current techniques for SOS processing along with reduced anneal temperatures, BJTs on SOS can be fabricated which exhibit low emitter collector leakage, decent bipolar current gain, and suitable circuit performance. Additionally, it can be said that this was the first demonstrated work in which complementary vertical BJTs on SOS were processed simultaneously using the same processing techniques.

20th March 1992

E. N. Cartagena, B. Offord and G. Garcia (*Naval Command Control and Ocean Surveillance Center, Research, Development, Test and Evaluation Division, Code 553, 271 Catalina Blvd., San Diego, CA 92152, USA*)