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Bonded silicon-on-sapphire wafers and devices

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Silicon-on-sapphire (SOS) has been prepared by direct wafer bonding. The silicon layer was thinned to about 10 μm by mechanical grinding and chemical etching. *P-N* junction diodes were fabricated in the bonded SOS and compared with epitaxially grown SOS. The reverse bias leakage current was almost $15\times$ less in the bonded SOS. A generation lifetime of 10 μs can be estimated from the junction leakage. The effects of processing temperatures on the bonded SOS were also studied.

Wafer bonding has been used to make material both for electronic devices and for micromachined structures.¹ In this work, 100 mm silicon wafers were bonded to 100 mm polished sapphire substrates using standard silicon wafer bonding techniques. The p^+ (boron, $1\times 10^{20}\text{ cm}^{-3}$) silicon device wafers had a lightly doped (boron, $5\times 10^{14}\text{ cm}^{-3}$) epitaxial layer. Prior to bonding, the wafers were treated with a $\text{H}_2\text{O}_2/\text{NH}_4\text{OH}$ solution, rinsed in de-ionized water, and spin dried under nitrogen.² The wafers were bonded under class 10 conditions with the major flats aligned. The initial bond strength was not measured but was strong enough so that it was difficult to separate the wafers without breaking the silicon. The initial bonding process was easy to monitor by observing the interference fringes through the transparent sapphire substrates.

Bonding would take place either with or without a 100 nm thermal oxide on the silicon device wafer. Bonding would not occur when an epitaxial film of silicon was on the sapphire substrate. The epitaxial silicon layer may not be smooth enough for good bonding to occur.³

Prior to thinning, the bonded wafers were heated in air for 2 h at 200 $^\circ\text{C}$ in order to strengthen the bond. Heating the wafers to 250 $^\circ\text{C}$ and higher caused the silicon wafer to crack. The silicon device wafer was thinned to about 100 μm by grinding and most of the remaining p^+ silicon was removed using a 1:6:3 $\text{HF}:\text{HNO}_3:\text{CH}_3\text{CO}_2\text{H}$ etch. The final thinning step was a 1:3:8 $\text{HF}:\text{HNO}_3:\text{CH}_3\text{CO}_2\text{H}$ etch, which is selective to p^+ silicon.⁴ This simple thinning process could be improved using more sophisticated mechanical or chemical techniques, such as precision machining or a different etch stop.

Samples of a bonded SOS film with a thickness of 8 μm were subjected to various temperatures, cleaved, and treated with Wright etch for 20 s.⁵ A sample that was not given any thermal processing other than the anneal prior to thinning was seen by scanning electron microscopy to be dislocation free. Another sample was given a 650 $^\circ\text{C}$ anneal for 1 h in dry oxygen. This caused cracking of the film with

crack spacing on the order of 100 μm . The defect etch highlighted lines of dislocations along the $\langle 111 \rangle$ planes. A third sample, annealed at 850 $^\circ\text{C}$ in dry oxygen for 1 h, also showed cracking. The etch exposed a significantly larger number of dislocations than were seen in the films which were annealed at 650 $^\circ\text{C}$.

The cracking that occurs in large area films after high temperature processing seems to relieve strain in the silicon. Regions were observed in films processed at 600 and 850 $^\circ\text{C}$ that were largely defect free. These regions are always near a large crack in the silicon. This indicates that mesa isolation may be required for these films before any high temperature processing.

As a test of the quality of the bonded silicon material, *P-N* diodes were fabricated in the bonded SOS. The first step in processing was mesa isolation with a KOH etch. A field implant was done next to provide ohmic contacts to the p^- substrate and prevent field inversion. This implant was activated at 850 $^\circ\text{C}$ for 49 min. A masked phosphorus implant formed the diodes with a junction depth of about 1 μm and dopant concentration of $1\times 10^{20}\text{ cm}^{-3}$. A field oxide was then grown in steam at 850 $^\circ\text{C}$ for 89 min, which also served to activate the implant. The processing temperatures were kept low in order to minimize dislocation generation. Contact holes were etched in the oxide, and Al/Si was deposited for metallization. The aluminum was patterned and sintered at 400 $^\circ\text{C}$ in forming gas.

As a comparison, similar diodes were fabricated in epitaxially grown SOS. A 300 nm film of SOS was first improved by double solid phase epitaxy,⁶ and then implanted with boron to form a buried layer. Silicon was then deposited by atmospheric chemical vapor deposition at 950 $^\circ\text{C}$ to a total thickness of 10 μm . The epitaxial SOS used the same subsequent processing temperatures as the bonded material. Diodes were also fabricated in p^- on p^+ bulk silicon wafers for comparison. Implant activation for these wafers was done at 950 $^\circ\text{C}$. All diodes had an active area of 10^{-4} cm^2 . Figure 1 shows schematic drawings of the diodes fabricated in the three materials.

Plots of the reverse bias leakage current versus bias voltage obtained from diodes in the three materials are

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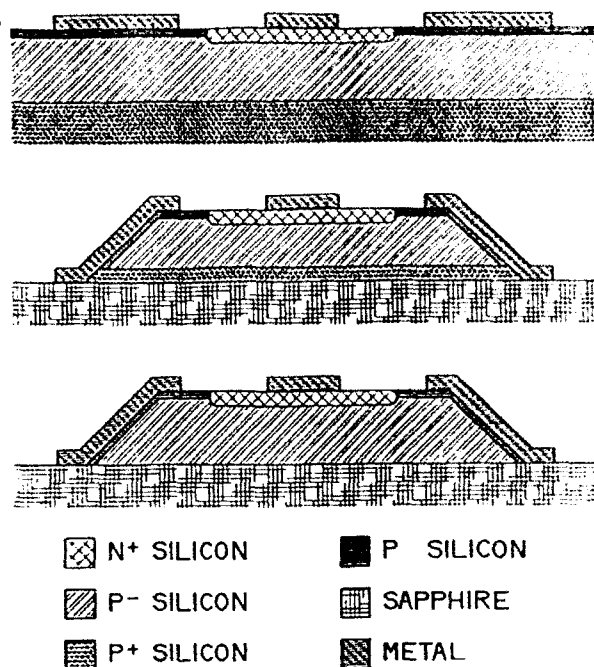


FIG. 1. Schematic drawings of the bulk silicon (top), epitaxially grown SOS (middle), and bonded SOS (bottom) diodes.

shown in Fig. 2. The bulk silicon diode exhibits low leakage as expected, 11 nA/cm^2 at 1 V reverse bias. The leakage current of the epitaxial SOS diode at 1 V is 740 nA/cm^2 , almost seventy times that of the bulk diode. At 1 V reverse bias, the leakage current in the bonded SOS diode is 51 nA/cm^2 , less than five times the leakage of the bulk diode. The unusual increase in leakage of the bonded SOS diode at higher reverse voltages is believed to be caused by carrier generation at the silicon-sapphire interface. The depletion region reaches the interface because of the lack of a heavily doped buried layer in the bonded SOS. At 1 V reverse bias, which in the lightly doped p region produces a depletion depth of $2 \mu\text{m}$, the generation lifetime in the bonded SOS was calculated to be about $10 \mu\text{s}$.

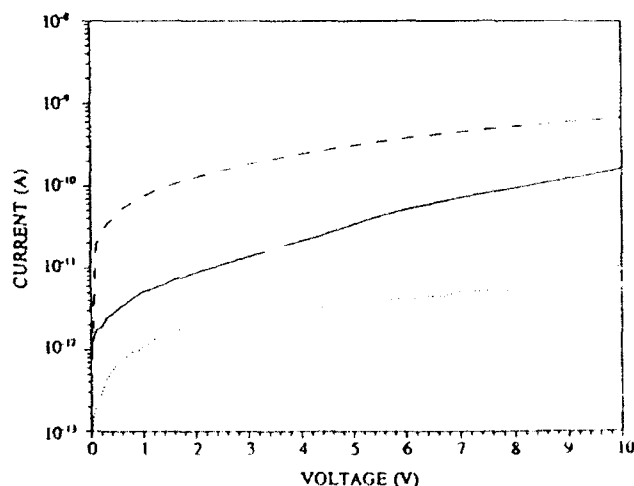


FIG. 2. Leakage current vs reverse bias voltage for bulk silicon (dotted line), bonded SOS (solid line), and epitaxial SOS (dashed line).

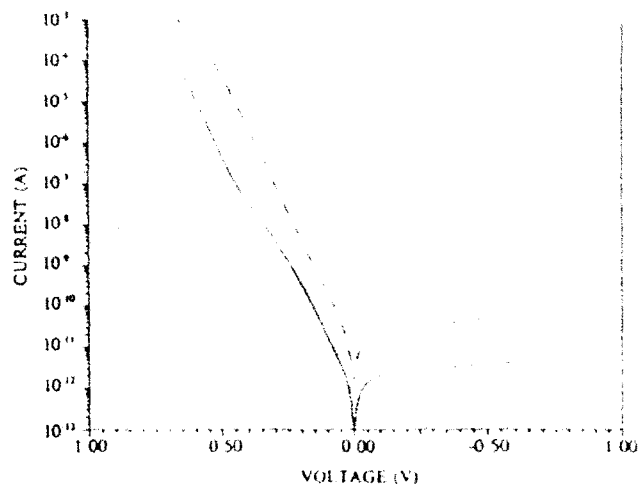


FIG. 3. Forward current vs bias voltage for bulk silicon (dotted line), bonded SOS (solid line), and epitaxial SOS (dashed line).

The forward characteristics of the diodes are shown in Fig. 3. The epitaxial SOS device shows excess current at low forward bias, which is indicative of recombination currents in the space charge region. This current can be associated with microdefects in the material. At small forward currents, the current in the bonded SOS diode is nearly identical to that in the bulk silicon diode. The higher series resistance of the bonded diode, due again to the lack of a highly doped buried layer, is seen in its larger voltage drop at higher currents. The saturation current of the bonded SOS diode is $43.6 \times 10^{-15} \text{ A}$, compared to $8.5 \times 10^{-15} \text{ A}$ in the bulk silicon diode.

Silicon bonded to sapphire is a new semiconductor material which may find applications in minority carrier devices, such as charge coupled devices or bipolar transistors. Diodes fabricated in bonded SOS films are significantly better than diodes in epitaxially grown SOS, and approach the quality of bulk silicon diodes. Problems which need to be addressed are film uniformity, and thermally induced defects. Film uniformity is not as critical for the thick film devices for which this material is intended as it would be for a fully depleted complementary metal-oxide-semiconductor technology. Bonded SOS in conjunction with epitaxial SOS may be particularly suited to a process which uses both bipolar and field effect transistors on SOS.

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¹ K. E. Petersen, *Proc. IEEE* 70, 420 (1982).

² W. P. Maszara, G. Goetz, A. Caviglia, and J. B. McKitterick, *J. Appl. Phys.* 64, 4943 (1988).

³ W. P. Maszara, in *Proceedings of the Fourth International Symposium on Silicon-on-Insulator Technology and Devices*, edited by Dennis Schmidt (The Electrochemical Society, Montreal, 1990), pp. 199-212.

⁴ H. Muraoka, T. Ohashi, and Y. Sumitomo, in *Semiconductor Silicon*, edited by H. R. Huff and R. R. Burgess (The Electrochemical Society Softbound Symposium Series, Princeton, 1973), p. 327.

⁵ M. Wright-Jenkins, *J. Electrochem. Soc.* 124, 757 (1977).

⁶ T. Yoshii, S. Taguchi, T. Inoue, and H. Tango, *Jpn. J. Appl. Phys.* 21, 175 (1982).