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Data are presented demonstrating a design and fabrication process for the realization of low-threshold, high-output vertical-cavity surface-emitting laser diodes with low series resistance. Lateral current confinement is achieved in the laser structures through the use of molecular-beam epitaxial regrowth over a 1000-A-thick patterned layer of low growth temperature AlGaAs incorporated into the p-type top mirror. A maximum cw output power in excess of 5.7 mW, at 300 K is demonstrated for 15-μm-diam devices. With increased top mirror reflectivity (through the addition of dielectric layers), the low series resistance of the design results in a bias voltage on only 1.8 V at a threshold current of 1.9 mA for 10-μm-diam devices.

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Low threshold voltage continuous wave vertical-cavity surface-emitting lasers

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Data are presented demonstrating a design and fabrication process for the realization of low-threshold, high-output vertical-cavity surface-emitting laser diodes with low series resistance. Lateral current confinement is achieved in the laser structures through the use of molecular-beam epitaxial regrowth over a 1000-Å-thick patterned layer of low growth temperature AlGaAs incorporated into the *p*-type top mirror. A maximum cw output power in excess of 5.7 mW, at 300 K is demonstrated for 15-μm-diam devices. With increased top mirror reflectivity (through the addition of dielectric layers), the low series resistance of the design results in a bias voltage of only 1.8 V at a threshold current of 1.9 mA for 10-μm-diam devices.

There has been considerable recent interest in vertical-cavity surface-emitting laser (VCSEL) diodes due to inherent advantages in the device geometry. Though there have been many advances in the reduction of threshold currents for these devices,[1,2] maximum cw output power is still limited in part due to poorly dissipated heat generated within the devices. Commonly used fabrication techniques for the VCSEL result in a device in which the current must flow through ~20 or more pairs of a *p*-type AlAs/(Al)GaAs distributed Bragg reflector (DBR), with a cross-sectional area on the order of 100 μm^2 or less.[3,4] This geometry contributes to resistive power loss and heating of the device. Success in reduction of the series resistance has been achieved through graded superlattices at the DBR heterojunctions,[5] and through periodically locating heavily doped regions about the heterojunctions where the electric field is lowest.[2,6]

Alternative fabrication methods can result in devices in which the current is funneled into the active region and the flow of current is only restricted to a small cross section in the region near the active region.[7–9] Such geometries are inherently less susceptible to high series resistance for small diameter devices. We have previously reported VCSEL devices in which current funneling is achieved through the use of molecular beam epitaxy (MBE) regrowth over a patterned *n*-type current blocking layer placed within the *p*-type top mirror near the active region.[8] However, a considerable amount of leakage current passes through the thin, *n*-type current blocking layers for voltages as low as 4 V.[10] MBE growth of GaAs at temperatures in the vicinity of 200–300 °C has been shown to produce layers exhibiting very high resistivity due to the incorporation of excess As during growth.[11] Recently, a 1-μm-thick, MBE-grown, low growth temperature (LT) GaAs layer has been used for current blocking in an edge-emitting laser.[12] The laser structure was grown by organometallic chemical vapor deposition on a channeled MBE-grown LT-GaAs epilayer. It has been shown that the resistivity on a LT-MBE epilayer can be significantly increased through the use of AlGaAs.[13] In this letter, we report the use of a thin (~1000 Å) LT-AlGaAs layer used for current funneling into an AlGaAs-GaAs-InGaAs VCSEL. As compared to a *pnpn* blocking structure, the highly resistive LT-AlGaAs layer leads to reduced sensitivity to doping levels in and around the current blocking layer, and reduced current leakage through the blocking layer. Compared to other possible insulators, AlGaAs provides good thermal conductivity and a thermal expansion coefficient which matches the rest of the epitaxial structure. By minimizing the thickness of the current blocking layer, planarity of the regrown crystal surface is improved, while device series resistance is reduced.

Figure 1 shows a schematic cross section of the MBE-grown VCSEL structure. The initial epitaxial structure consists of a 0.2 μm *n*-type GaAs buffer layer followed by a 23-pair, *n*-type, AlAs/GaAs quarter-wave stack tuned to 0.98 μm, a quarter-wave layer of *n*-type $Al_{0.67}Ga_{0.33}As$, an active region consisting of three 60 Å $In_{0.2}Ga_{0.8}As$ quantum wells (QWs) separated by 100 Å GaAs barriers in a one-wavelength-thick GaAs cavity, a *p*-type quarter-wave $Al_{0.67}Ga_{0.33}As$ layer, a one-eighth-wavelength-thick *p*-type GaAs layer, a 1000-Å-thick undoped LT-$Al_{0.67}Ga_{0.33}As$ layer, and a *p*-type GaAs layer of one-eighth wavelength in thickness. The QW active region is grown at a substrate temperature of 540 °C, the LT-AlGaAs at 270 °C, and the rest of the structure at 610 °C. An 8-period graded superlattice is placed on both sides of each of the $Al_{0.67}Ga_{0.33}As$ layers surrounding the active region for a reduction in series resistance.

After initial growth, 10, 15, 30, and 60 μm openings are photolithographically defined on the epitaxial surface, and a solution of H_2O_2-NH_3OH with *p*H adjusted to ~7.2 is used to selectively etch through the top GaAs layer. After removing the photoresist, the exposed LT-AlGaAs layer is selectively etched using a dilute HF-H_2O solution, and the samples are returned to the MBE system for regrowth. Delays between etching and regrowth have been as long as a few days, with the wafer stored simply in an atmosphere environment. Before the regrowth, the oxide is desorbed in the MBE system using a standard procedure of monitoring the reflection high-energy electron diffraction pattern. The MBE regrowth layers consist of a *p*-type GaAs layer of one-eighth wavelength in thickness followed by either a 4-pair or a 6-pair *p*-type AlAs/GaAs quarter-

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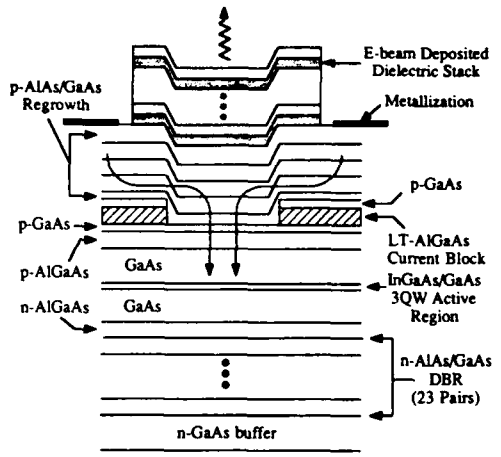

FIG. 1. Schematic cross section of a vertical-cavity surface-emitting laser diode incorporating a patterned LT-AlGaAs layer for lateral definition of the active region.

wave stack. In order to further reduce series resistance in these devices, an 8-period graded superlattice is placed at every AlAs/GaAs heterojunction. After the regrowth, scanning electron microscopy (not shown) reveals that voids may sometimes occur at the edges of etched region, confined internally to the epitaxial layer.

After MBE crystal growth, Cr/Au metallization is deposited on the epitaxial surface with a "lift-off" process used to remove metallization from the area above the openings in the LT-AlGaAs layer. Electrical isolation is achieved by etching ~ 2 μm troughs into the epitaxial layers around each emitter. This leaves square contact pads of ~ 400 μm on a side for each device. The reflectivity of the output (p-side) mirror is then enhanced through electron-beam deposition of successive pairs of quarter-wave ZnSe/CaF_2 dielectric layers.[14] At 300 K, cw lasing is obtained after the deposition of two quarter-wave dielectric pairs. The lasing threshold current, efficiency, and maximum output power reduce with the deposition of additional pairs of dielectric layers.

Figure 2 shows the cw room-temperature lasing characteristics of one of the lower threshold devices. The output mirror for this device consists of a MBE-grown 6-pair

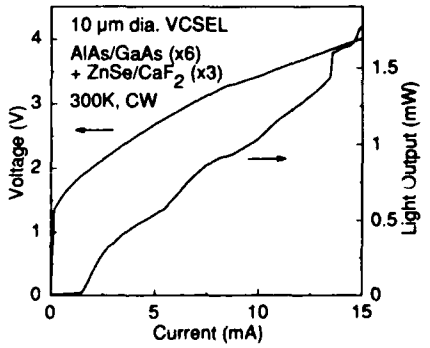

FIG. 2. cw, 300 K, light vs current and voltage vs current for 10-μm-diam VCSEL. The top (output) reflector consists of a MBE-grown 6-pair AlAs/GaAs DBR with a 3-pair ZnSe/CaF_2 DBR deposited on top through electron-beam evaporation.

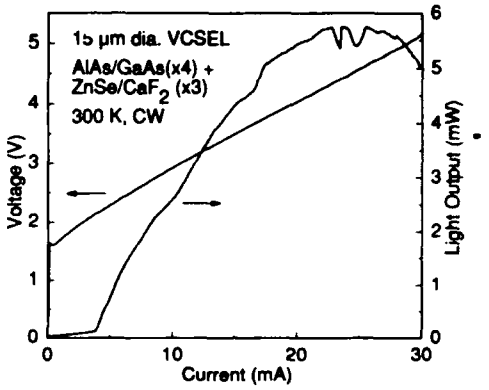

FIG. 3. cw, 300 K, light vs current and voltage vs current for 15-μm-diam VCSEL. The top (output) reflector consists of a MBE-grown 4-pair AlAs/GaAs DBR with a 3-pair ZnSe/CaF_2 DBR deposited on top through electron-beam evaporation.

AlAs/GaAs DBR, and a 3-pair electron-beam deposited dielectric stack. The emitter is nominally 10 μm in diameter, with a 15-μm-diam opening in the metallization around it. The lasing threshold current is measured to be ~ 1.5 mA with a threshold voltage of only 1.9 V, and a series resistance of ~ 110 Ω. The maximum cw output is greater than 1.7 mW at a wavelength of 979 nm. Over 300 devices were tested, and over 95% of the devices exhibited cw lasing. The threshold voltage of a large number of the 10 μm devices measured are found to be in the range of ~ 1.8 V after the deposition of a 4-pair dielectric stack. This threshold voltage is comparable to the best values previously reported for pulsed VCSELs.[9]

When comparing devices with identical ZnSe/CaF_2 dielectric stacks, those with the 4-pair AlAs/GaAs DBR typically exhibit a higher efficiency and greater maximum output than the devices with the 6-pair AlAs/GaAs DBR. However, they also possess, on average, a higher threshold current for lasing. Figure 3 shows the cw room-temperature lasing characteristics of a 15-μm-diam device with a 30 μm opening in the metallization around it. The output mirror for this device consists of a MBE-grown 4-pair AlAs/GaAs DBR, and a 3-pair electron-beam deposited dielectric stack. The lasing threshold current is measured to be ~ 3.7 mA with a voltage of ~ 2.1 V at this current, and a series resistance of ~ 115 Ω. The maximum cw output is greater than 5.7 mW at a wavelength of 989 nm.

The 30 and 60 μm devices show evidence of nonuniform pumping of the active region. By viewing a device with an infrared viewer and a microscope, we note that lasing often focuses in spots near the perimeter of these devices. This can be attributed to a higher current density around the perimeter, as compared to the current density in the center of the device, and results from resistance to lateral current flow caused by the relatively thin layer of conductive material above the current blocking layer. This lateral resistance is also evident in that the series resistance is higher for devices with metallization openings that are much greater than the opening in the current blocking layer.

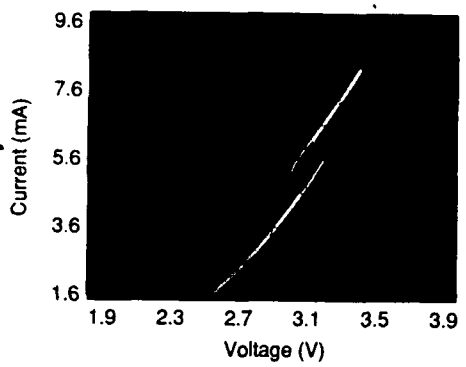

FIG. 4. Photograph from curve tracer showing hysteresis in the current-voltage characteristic for a 30 μm VCSEL diode.

We previously have observed hysteresis and switching in VCSELs which make use of a *pnpn* blocking structure to achieve the current funneling into the device active region.[10] Although we initially thought that the switching must be related to the *pnpn* structure, we later concluded that the bistable behavior might actually be an intrinsic cavity property made evident by leakage currents into the VCSEL active region.[15] That the switching observed is not related specifically to the *pnpn* structure[15] is borne out in characterization of the present devices which make use of the LT-AlGaAs current blocking layer. Pronounced hysteresis is observed in many of the present devices, as shown in the current-voltage characteristics of Fig. 4. As before,[10] the switching behavior is only observed at lasing threshold or with transverse mode hops above threshold, and the hysteresis window is seen to increase if the dielectric stack reflectivity is increased. Leakage currents again seem to be key to observing the bistable behavior, with the behavior being more evident in the larger 30 and 60 μm devices. Though we expect the current leakage through the LT-AlGaAs layers to be negligible, two effective current leakage paths are available to contribute to such behavior. Current spreading due to the separation between the current funneling structure and the active region may be significant for all the devices, and the current flowing into the non-lasing region near the center of the large diameter devices may also represent a significant leakage current. Details of the switching behavior are currently under study.

In summary, through the use of MBE regrowth over a patterned LT-AlGaAs layer for lateral current confinement, we have demonstrated VCSELs with a voltage at lasing threshold of only 1.8 V for 10-μm-diam devices. The low series resistance is a result of current being funneled into the active region through an opening in a very thin current blocking layer as opposed to current being passed through a comparably thick region of small diameter. The use of the insulating AlGaAs current blocking layer avoids thermal expansion mismatches, and provides improved thermal conductivity over other types of insulators.

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